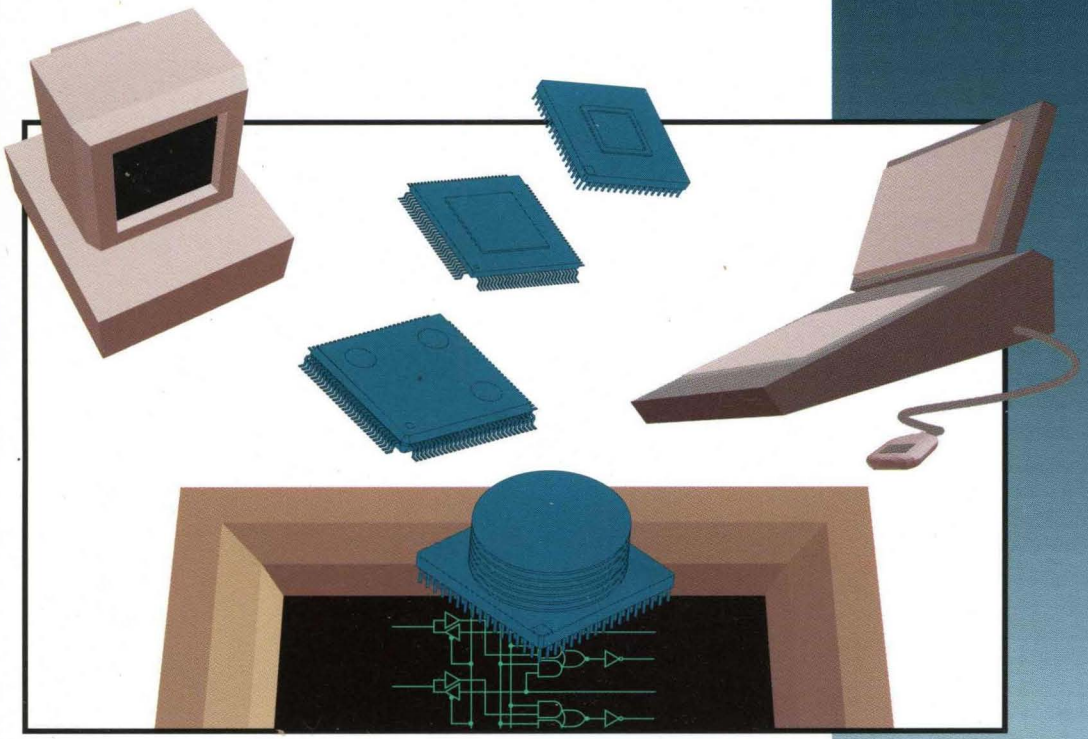
FUJITSU

Channelless Gate Arrays

1990 Data Book and Design Evaluation Guide



Data Book and Design Evaluation Guide

Channelless Gate Arrays

1990

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CMOS Channelless Gate Arrays

1990
Data
Book

Fujitsu Limited
Tokyo, Japan

Fujitsu Microelectronics, Inc.
San Jose, California, U.S.A.

Fujitsu Mikroelektronik GmbH
Frankfurt, F.R. Germany

Fujitsu Microelectronics Pascific Asia PTE Limited
Kowloon, Hong Kong

This document is published by the Publications Department, Fujitsu Microelectronics, Inc.,
3545 North First Street, San Jose, California, 95134–1804; U.S.A.

Printed in the U.S.A.Edition 2.0

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ASIC Packaging Considerations

Preface

Fujitsu Microelectronics introduced its first commercially available gate array, a bipolar chip called the B200, in 1974 (Fujitsu had been making them for internal use since 1972). Over the years it has been so popular that it is regarded as the world's most widely implemented gate array. Since that first array, Fujitsu has produced over 9000 successful bipolar and CMOS custom designs.

Fujitsu designs are successful because they are implemented using the most advanced design verification CAD systems available, allowing the production of chips with 90% cell utilization (more functional logic per chip than the industry standard) and one of the highest performance records in the industry.

This data book provides you with the information necessary to choose an application specific integrated circuit (ASIC) device using Fujitsu's advanced AU and CG21 channelless (sea-of-gates) CMOS gate array technologies. The data book describes Fujitsu's AU and CG21 gate arrays, explains their benefits and specifications, and outlines the process by which logic and circuit designers create a chip. The cell function (unit cell) libraries for the AU and CG21 technologies are included in the second and third sections of this volume. The first volume in this data book series provides the same information for Fujitsu's channeled gate arrays.

Fujitsu has pioneered and maintained a technological lead in the production of bipolar as well as CMOS ASIC devices; data books describing Fujitsu's other ASIC product families, as well as any other technical or sales-related information, may be obtained from any Fujitsu Technical Resource Center or Sales Office listed at the end of this book or by calling or writing Fujitsu Microelectronics Inc., 3545 North First Street, San Jose, CA 94135–1804, (408) 922–9000.

Fujitsu ASIC Products Listing

CMOS Channeled Gate Arrays Data Book

UHB Series High Drive CMOS Gate Arrays — 1.5μ, 0.9 ns typical delay

Description	Name	Device Part Number
336 Gates, 58 I/O	C330UHB	MB625xxx
530 Gates, 64 I/O	C530UHB	MB624xxx
830 Gates, 74 I/O	C830UHB	MB623xxx
1,233 Gates. 88 I/O	C1200UHB	MB622xxx
1,724 Gates, 102 I/O	C1700UHB	MB621xxx
2,220 Gates, 115 I/O	C2200UHB	MB620xxx
3,066 Gates, 140 I/O	C3000UHB	MB606xxx
4,174 Gates, 155 I/O	C4100UHB	MB605xxx
6,000 Gates, 155 I/O	C6000UHB	MB604xxx
8,768 Gates, 188 I/O	C8700UHB	MB603xxx
12,734 Gates, 220 I/O	C12000UHB	MB602xxx

CG10 Series High Drive CMOS Gate Arrays — 0.8μ, 0.5 ns typical delay

3,256 Gates, 108 I/O	CG10272	MBCG10272xxx
4,032 Gates, 123 I/O	CG10342	MBCG10342xxx
5,072 Gates, 148 I/O	CG10492	MBCG10492xxx
6,510 Gates, 163 I/O	CG10572	MBCG10572xxx
7,684 Gates, 163 I/O	CG10692	MBCG10692xxx
11,080 Gates, 188 I/O	CG10103	MBCG10103xxx
14,720 Gates, 220 I/O	CG10133	MBCG10133xxx

CMOS Channelless Gate Arrays Data Book

AU Series CMOS Series Gate Arrays — 1.2μ, 0.6 ns typical delay

10,224 Gates, 108 I/O	C10KAU	MB637xxx
15,486 Gates, 138 I/O	C15KAU	MB636xxx
20,876 Gates, 155 I/O	C20KAU	MB635xxx
31,500 Gates, 178 I/O	C30KAU	MB634xxx
41,184 Gates, 220 I/O	C40KAU	MB633xxx
52,164 Gates, 257 I/O	C50KAU	MB632xxx
75,140 Gates, 300 I/O	C75KAU	MB631xxx
102,144 Gates, 332 I/O	C100KAU	MB630xxx

CG21 Series CMOS Series Gate Arrays — 0.8μ, 370 ps typical delay

10,224 Gates, 108 I/O	CG21103	MBCG21103xxx
15,486 Gates, 142 I/O	CG21153	MBCG21153xxx
20,876 Gates, 155 I/O	CG21203	MBCG21203xxx
31,500 Gates, 178 I/O	CG21303	MBCG21303xxx
41,184 Gates, 220 I/O	CG21403	MBCG21403xxx
52,164 Gates, 245 I/O	CG21503	MBCG21503xxx
75,140 Gates, 284 I/O	CG21753	MBCG21753xxx
102,144 Gates, 332 I/O	CG21104	MBCG21104xxx

Fujitsu ASIC Products Listing (Continued)

BiCMOS Gate Arrays Data Book

BC Series BiCMOS Gate Arrays — 1.5μ/1.4μ, 0.65 ns typical delay

Description	Name	Device Part Number
645 Gates, 52 I/O	BC400	MB211xxx
1,218 Gates, 72 I/O	BC800	MB212xxx
1,872 Gates, 96 I/O	BC1200	MB213xxx
3,240 Gates, 112 I/O	BC2000	MB214xxx

BC-H Series BiCMOS Gate Arrays — 1.0μ/0.5μ, 0.45 ns typical delay

4,312 Gates, 96 I/O	BC4000H	MB221xxx
8,160 Gates, 128 I/O	BC8000H	MB222xxx
11,968 Gates, 160 I/O	BC12000H	MB223xxx
16,720 Gates, 200 I/O	BC16000H	MB224xxx
7,920 Gates, 200 I/O with 40Kb RAM	BC8040HM	MB228xxx

ECL Gate Arrays Data Book

ET Series ECL Gate Arrays — 1.0μ, 220 ps typical delay

1,056 Gates, 64 I/O	ET750	MB121Kxxx
2,112 Gates, 88 I/O	ET1500	MB123Kxxx
4,224 Gates, 120 I/O	ET3000	MB125Kxxx
6,160 Gates, 120 I/O	ET4500	MB128Kxxx
2,640 Gates, 120 I/O with 4.6 Kb RAM	ET2004M	MB181/191xxx
2,640 Gates, 136 I/O, with 9.2 Kb RAM	ET2009M	MB182/192xxx
3,960 Gates, 136 I/O, with 4.6 Kb RAM	ET3004M	MB183/193xxx

H Series ECL Gate Arrays — 0.5μ, 100 ps typical delay

9,856 Gates, 200 I/O	ET10000H	MB147/157xxx
9,856 Gates, 300 I/O	E10000H	MB148/158xxx
4,928 Gates, 200 I/O, with 5.1Kb RAM	E5005HM	MB185/195xxx

Ultra High Performance ECL Gate Arrays 0.5μ, 75 ps typical delay

128 Gates, 23 /I/O	E128H	MB1800
32 Gates, 13 I/O	E32	MB1700
128 Gates 16 I/O	E128	MB1600

VH Series ECL Gate Arrays 0.4μ, 80 ps typical delay

38,948 Gates, 300 I/O	E30000VH	MB162/172xxx
13,440 Gates, 290 I/O, 40Kb RAM	E10040VHM	MB165/175xxx
13,440 Gates, 294 I/O, 160Kb ROM	E10160VHR	MB168/178xxx

CMOS Standard Cell Data Book

AU Series Standard Cells — 1.2μ, 0.6 ns typical delay

AS Series Standard Cells — 0.8μ, 370 ps typical delay

Section 1

Design Information

1

Chapter 1 – Fujitsu CMOS Products

Contents of This Chapter

1.1 Introduction

This section of the data book gives an overview of CMOS technology and introduces the CMOS channelless gate array technology families developed by Fujitsu to implement ASIC designs.

1.2 CMOS Technology for ASICs

ASICs (Application Specific Integrated Circuits) are large scale integrated circuits that provide customers with made-to-order functions. These ICs implement the unique value designed into customer products by producing custom semiconductor designs that allow customers to take advantage of perceived market opportunities in a timely manner. The customized solutions offered by ASICs combine the power of personalized electronics and the advantage of increased system efficiency.

CMOS technology has long been chosen for ASIC applications because of its low power and high density characteristics. Advancing process technology and new production and fabrication techniques have now allowed device speed to increase to the point where it is competitive with bipolar devices. Fujitsu CMOS gate arrays are manufactured using advanced silicon gate technology utilizing two-layer and three-layer metal. This fabrication process yields parts that:

a. require very low power dissipation (typically less than 500 mW per channeled array)
b. operate at speeds equaling existing bipolar technologies
c. feature higher gate densities than competing bipolar devices
d. use a single power supply of 5 volts or less
e. provide top-grade noise immunity and programmable logic levels compatible with TTL and CMOS logic families

1.3 CMOS Gate Array Structure

Fujitsu CMOS gate arrays are configured in a matrix of basic cells in the center of the chip with input-output (I/O) cells on the device periphery. One basic cell is equivalent to a two-input NAND gate. The custom logic function is realized by interconnecting basic cells with double-layer metallization for the channeled and smaller channelless arrays and triple-layer metallization for channelless arrays of over 30K equivalent gates. Fujitsu's gate array products are fabricated using a twin-tub polysilicon CMOS process to produce high-speed, high-density arrays consisting of 300 to 100,000 basic cells.

1.3.1 The Basic Cell

The basic cell of Fujitsu's CMOS gate array is a common building block consisting of one pair of P-channel and one pair of N-channel MOS transistors (represented by the broken-line box in Figure 1–1). Channelless arrays differ from the channeled arrays by the addition of four smaller N-channel transistors also shown in Figure 1–2. The four additional transistors are isolated from the P-and N-channel pairs, have no effect on them when the basic cells are configured as digital logic unit cells, and can be used as

an area to place the metalization that connects the unit cells. The basic cells are assembled in pairs on double-wide columns, and share common terminals of the two sets of four N-channel transistors.

The four additional N-channel transistors are used in conjunction with the "generic" portion of the basic cell to construct RAM and ROM compiled cell modules.

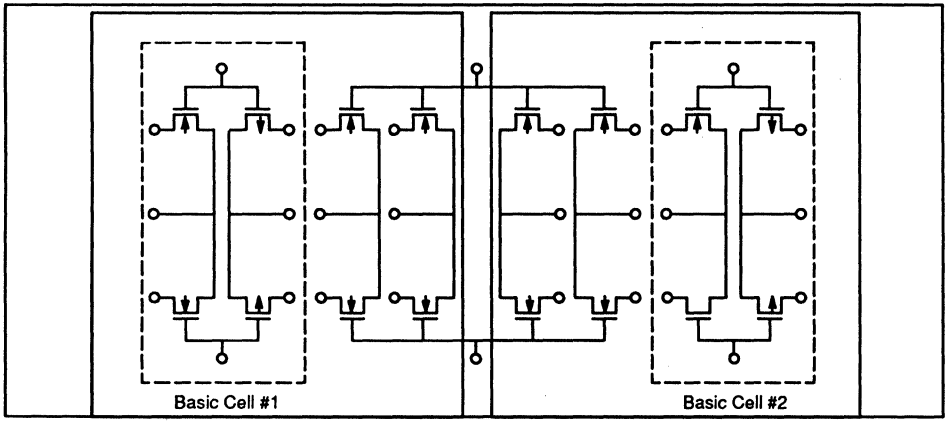


Figure 1–1. The Basic Cell

Since these are "generic" basic cells, no connections are shown to the power supply (+5 volts), to ground, or to the two common control gate terminals of the circuit. These connections are made as required during the metalization phase of the manufacturing process. The basic cell is the building block of all functions of the array and is often used as a unit to describe the size of an array or the complexity of a unit cell (logic function).

Figure 1–2 shows a schematic representation of the basic cell with the addition of the custom metalization required to convert the generic basic cell into a two-input NAND gate.

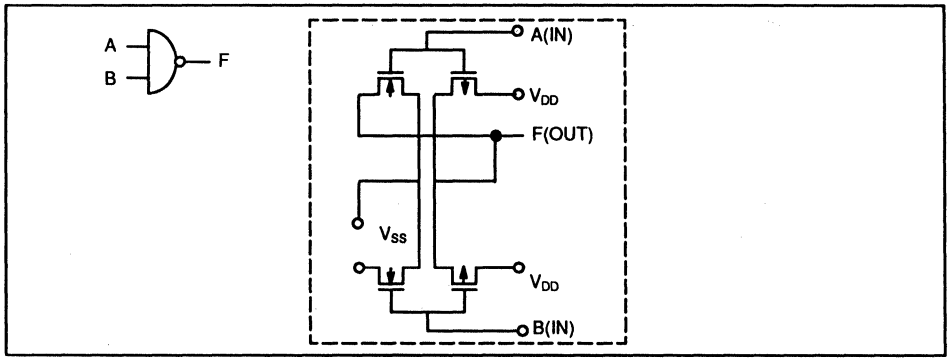


Figure 1–2. The Basic Cell as a 2-Input NAND Gate

1.3.2 Basic Cell Construction

Basic cell construction varies somewhat among Fujitsu's CMOS technologies; however, an explanation based on AV technology provides a good model of how a basic cell is fabricated in any of the CMOS

families. In AV, the basic cell is constructed from an N-type silicon substrate upon which a P-well is deposited. The surface of the substrate is then covered with a thin layer of silicon dioxide (glass) and two strips of polysilicon are deposited perpendicular to the P-well and geometrically parallel. (Polysilicon is a silicon-based compound chemically altered so that it has good electrical conduction properties.) The polysilicon strips serve as the gate control elements of the basic cell and also as the two electrical interconnections between the sources of the P and N transistor pairs. See Figure 1–3.

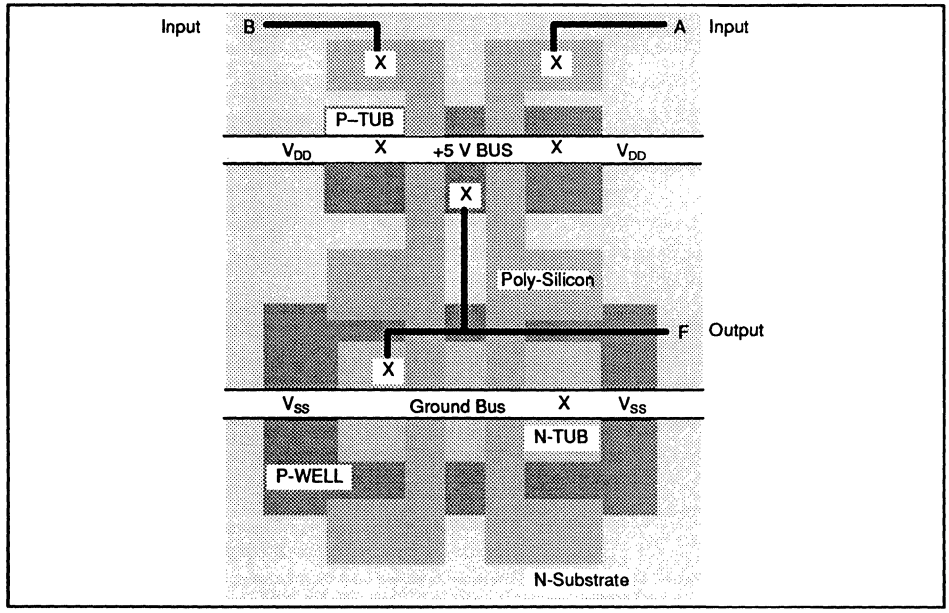


Figure 1–3. Physical Construction of the Unit Cell NAND Gate

The silicon dioxide layer is then stripped away from all areas of the substrate not protected by polysilicon. In two separate steps, the N-type and the P-type material of the twin tubs is diffused onto the substrate.

For the next step, N-type material is diffused or implanted into the P-well that was previously laid down. It straddles the two strips of polysilicon close to their ends. The polysilicon resists the diffusion, which results in the formation of three pads of N-type material separated by the two strips of polysilicon (self-aligned processing). The center pad of N-type material serves as a common drain terminal for both N-channel transistors. The outer pads are the separate source elements.

Then the P-type material is deposited on the the N-type substrate straddling the two polysilicon strips. Similarly the center pad of P-type material forms the common source connection for both P-channel transistors. The basic cell is then converted to a unit cell by application of a custom metalization pattern that connects (or wires) various points of the basic cell, or a number of basic cells, together. NO TAG shows the structure of a basic cell configured as a NAND gate after metalization (represented by the solid bold line connections) has been laid down.

Cell construction in the AU and CG21 technologies requires three layers of metal to be applied. Such layers are separated by an insulating layer of silicon dioxide. Interconnections between the metal layers are made by means of "vias" passing through the glass.

1.3.3 Basic Cell Arrangement

Basic cells can be arranged in any of the following configurations:

a. Unit cells
b. User macros
c. Compiled cells and super macros
d. I/O buffer cells

1.3.4 Unit Cells

Unit cells are the fundamental logic unit or function used for logic design, including digital logic gates, compiled cells, and I/O buffers.

1.3.5 User Macros

User macros are composed of unit cells to form higher level logic block functions (e.g., shift register or decoder). Such blocks are user-defined and may contain any unit cell configuration.

1.3.6 Compiled Cells and SuperMacros

Compiled cells and supermacros are MSI and LSI macros that perform memory functions (RAM and ROM) and such logic functions as adders and multipliers. Compiled cells are automatically generated by Fujitsu using proprietary compilers. Their building block approach and functional compatibility with common MSI and LSI devices can simplify construction of large and complicated designs. These cells are currently available for the AU and CG21 technologies; the status and design requirements of the super macros should be verified with a Fujitsu Sales Office or Technical Resource Center.

Selected compiled cells include:

- Dual-port RAM
- Triple-port RAM
- Single-port RAM
- ROM
- Multiplier
- Barrel shifter
- FIFO compiler

SuperMacros

Fujitsu's next step upward in ASIC functionality is embodied in the concept of supermacros. SuperMacros are large functional organizations implemented as an integral part of a chip. SuperMacros can be large-scale compiled cells or core cells, as well as generic or proprietary LSI functions. Reduction of board space, reduction of cost, and reduction of design cycle time, as well as extended functionality, reliability, performance, and security of design are all advantages of supermacros. Since supermacros are not bound to a particular technology, they may be migrated from one technology to another.

Fujitsu provides customers with gate and behavioral level models, macro symbols, and data sheets/specifications as well as kit parts in order to provide complete support from development to system integration. The supermacros listed below are the first to be developed for Fujitsu's CMOS supermacro library.

Table 1–1. SuperMacro Implementations for CMOS ASIC

Function	Compatible Device	Technology	Gate Complexity
Universal Synchronous/Asynchronous Receiver/Transmitter (USART)	8251A	UHB/AU/CG21	2900
Universal Asynchronous Receiver/Transmitter (UART)	8868	UHB/AU/CG21	TBD
Programmable Interval Timer	8253	UHB/AU/CG21	5680
Programmable Peripheral Interface	8255A	UHB/AU/CG21	784 – 1403[1]
Programmable Interrupt Controller	8259	UHB/AU/CG21	2205
Programmable DMA Controller	8237	UHB/AU/CG21	5100
Clock Generator/Driver	8284	UHB/AU/CG21	99
Bus Controller	8288	UHB/AU/CG21	250
Programmable Internal Timer	8254	UHB/AU/CG21	3500
CRT Controller	6845	UHB/AU/CG21	2843
SCSI Protocol Controller	87030[2]	UHB/AU/CG21	3600
EtherNet Controller[3]	87012[2]	UHB/AU/CG21	~3900
4-bit Arithmetic Logic Unit (ALU) Slice	2901	UHB/AU/CG21	917
Carry Lookahead	2902	UHB/AU/CG21	33
Status and Shift Control	2904	UHB/AU/CG21	~500
12-bit Microprogram Controller	2910	UHB/AU/CG21	1100

[1]Several options are available (Mode 0 is 785 gates)
[2]Full-featured Fujitsu proprietary supermacro
[3]Under consideration

1.3.7 I/O (Input/Output) Buffer Cells

The I/O buffer cell is composed of both external and internal I/O cells. External I/O cells are located on the periphery of the gate array. Internal I/O cells are ordinary unit cells located in the main cell matrix of the gate array. There are a variety of I/O buffer designs including input, output, and bidirectional buffers.

Input buffers convert external voltage levels to internal CMOS levels. Input buffers include:

Low-drive input buffers with pull-up or pull-down resistance

Schmitt trigger input buffers

High-drive clock input buffers

Output buffers convert internal CMOS levels to external voltage levels and are available with 3.2 mA, 8 mA, 12 mA, and 24 mA current sink capability, and optional noise-limiting resistance (edge rate control). Output buffers include:

Output buffers with noise-limiting resistance

3-state output buffers

The bidirectional buffer is a combination of an input buffer and a 3-state output buffer in the same unit cell.

1.3.8 Structure of the Chip

The arrangement of the basic cells on the chip differs according to the technology. The fundamental chip layout is a matrix of basic cells surrounded by a perimeter of I/O cells. In the channeled arrays, basic cells can be arranged in single columns, with the channels between the columns used for routing unit cell interconnections, as in AV, AVB, AVL, and AVM technologies, or in double columns, as in UHB technology. See Figure 1–4. In the channelless or sea-of-gates technologies (AU and CG21), the cells are positioned with no wiring channels between the double columns, allowing the wiring to go over the cells, rather than between the cells. See Figure 1–5.

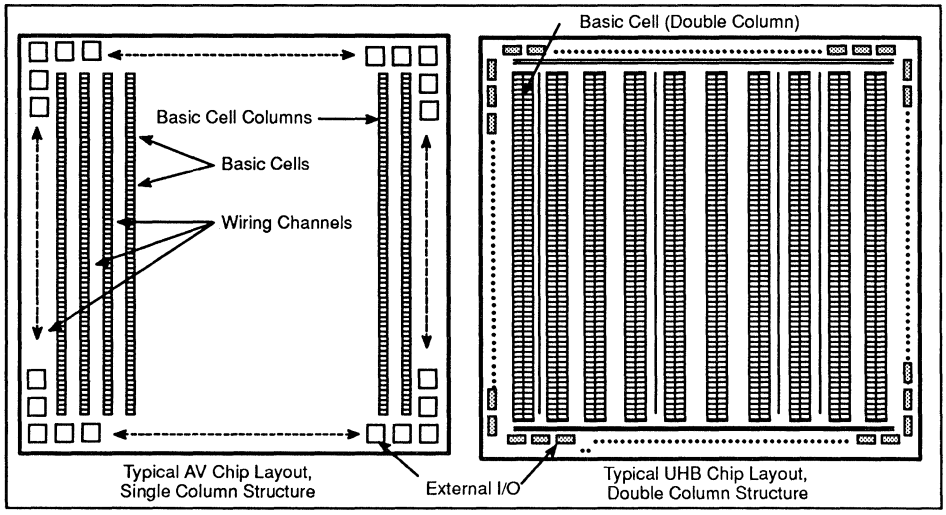


Figure 1–4. Channeled Gate Array Chip Structure

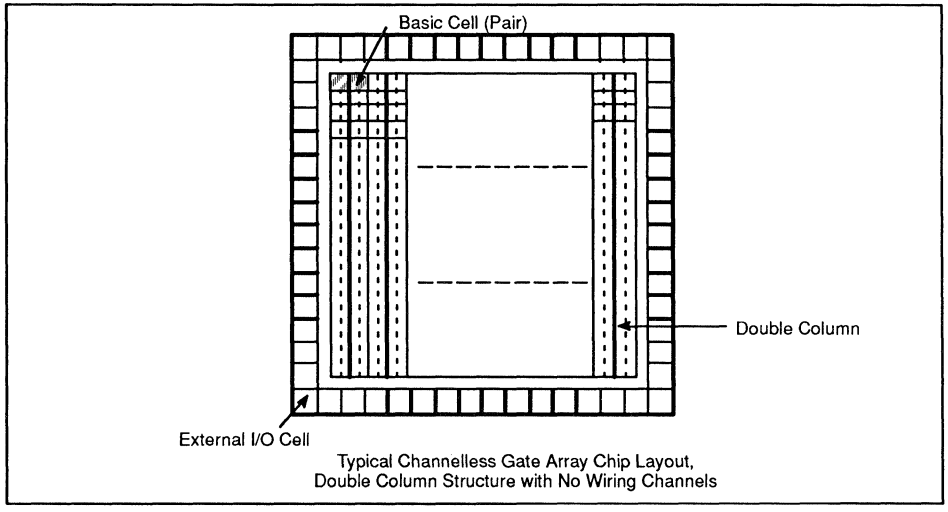


Figure 1–5 Channelless Gate Array Chip Structure

Larger gate arrays depart from the fundamental layout scheme by partitioning the basic cell matrix into four blocks. In some instances the designer may define the size of each block within certain limitations, while in other cases the block size is fixed. The purpose of chip partitioning is to improve speed performance by controlling wire length. Each block can be looked at as a small gate array, with four such gate arrays inside one package. (Smaller arrays exhibit less delay than larger ones.) In the AU and CG21 technologies, a block can be devoted to RAM or ROM for special applications requiring memory.

1.4 Fujitsu's CMOS Gate Arrays

Fujitsu's channelless CMOS gate arrays are described in detail in the data sheet that follows at the end of this chapter. Complete information on Fujitsu's channeled CMOS gate array families is provided in a separate data book.

All offer the same high reliablility, fast turnaround on design, simplified customer interface, full support by Fujitsu ViewCAD system design software if requested, full design support on other major CAE workstations, and a wide variety of packaging options.

The number of gates in relationship to the processing speed of each new CMOS technology is shown in Figure 1–6. Figure 1–7 shows in tabular form the equivalent gate count for each technology family.

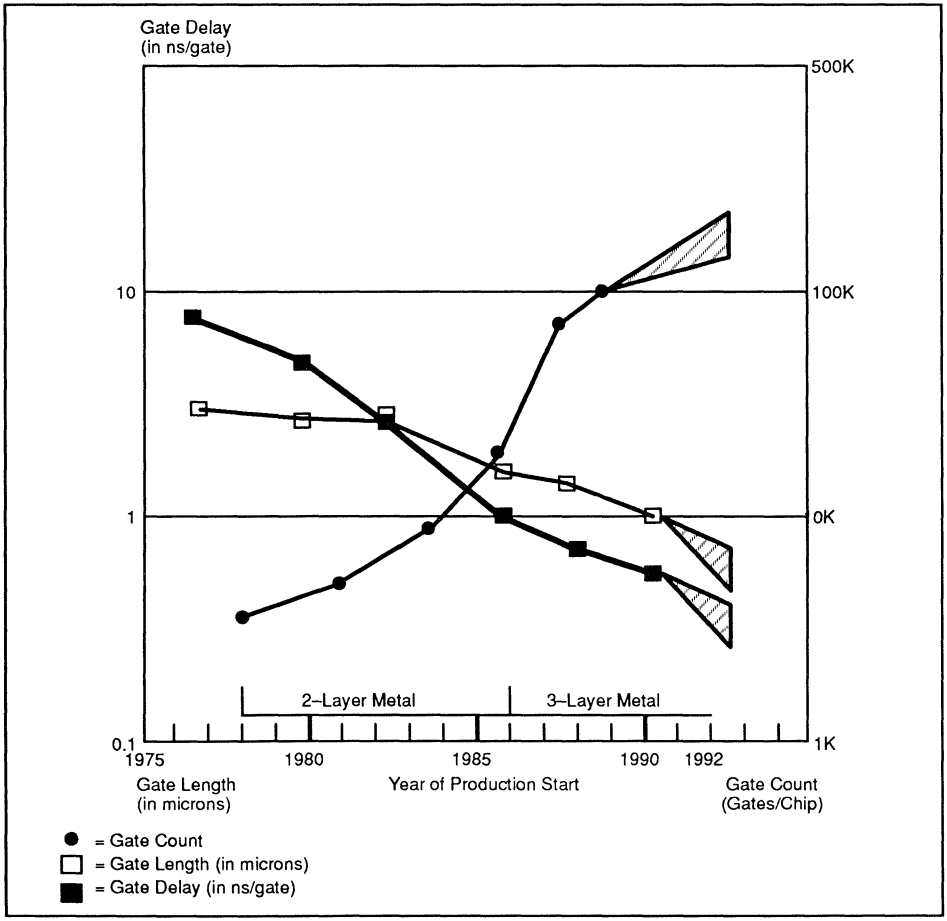


Figure 1–6. Equivalent Gate Count vs. Processing Speed, Fujitsu CMOS Gate Array Technologies

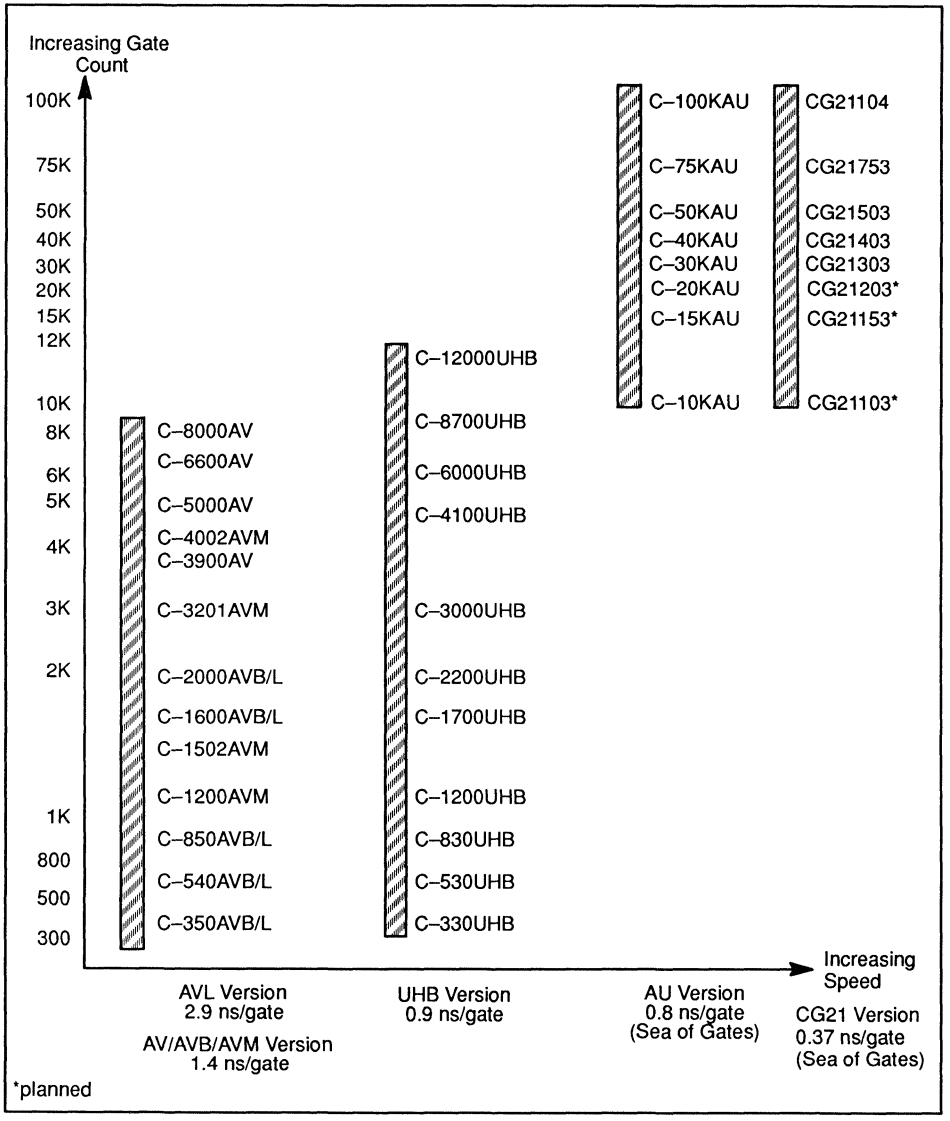


Figure 1–7 Equivalent Gate Count, Fujitsu CMOS ASIC Technology Families

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

AU Series CMOS Gate Arrays

DESCRIPTION

The AU series of 1.2 µm CMOS gate arrays, available in eight device types with from 10K to 100K gates, achieves the ultra fast speed of 0.6 ns per gate. Thanks to the channel-free structure of the AU gate array, AU basic cells can be used for logic cells, memory cells, or wiring area in order to implement the desired functions. The full utilization of the array surface and the three-layer metal interconnect technology produce a 75 percent maximum gate usability ratio.

The logic and I/O cells for the AU series are functionally compatible with Fujitsu's UHB series of gate arrays as well as with the new CG21 arrays to simplify upgrading. User-specifiable RAM and ROM configurations are also available. These gate arrays facilitate the implementation of large-scale devices such as computer and graphic processors on single chips.

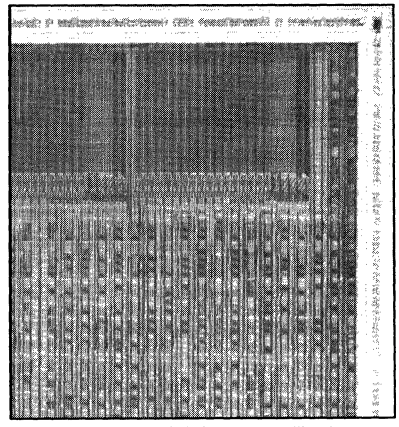
FEATURES

- 1.2 micron CMOS sea-of-gates technology
  –3 layer metal interconnect for C30KAU to C100KAU
  –2-layer metal interconnect for C30KAU to C20KAU
- Ultra high speed
  – 0.8 ns/gate for 2-input NAND
  – 0.6 ns/gate for power 2-input NAND
- High basic cell usage
  – 75% maximum for logic with RAM/ROM
  – 50% maximum for logic only
- High sink current capability
  – sink current up to 24 mA
- Minimum delay clock buffer true option
- High current clock drivers
  –Low-skew clock signal distribution
- Extensive unit cell library (logic cell, RAM, ROM)
  –Unit cells functionally compatible with Fujitsu's UHB gate array series and new CG21 series
- Automatic test pattern generation optional
- On-chip pull-up/pull-down resistors
- High pin count plastic and ceramic packages
- High-density RAM and ROM compilers
  – up to 18K bit RAM compilation
  – up to 64K ROM compilation

1

PRODUCT FAMILY

Device	Part Number	BCs on Chip (2-input gate +4 N-ch Tr)	Usable BCs	Max Signal I/O
C–10KAU	MB637xxx	10,224	75% max. for Logic with RAM,ROM 50% max. for Logic only (Preliminary values, to be upgraded)	108
C–15KAU	MB636xxx	15,486		138
C–20KAU	MB635xxx	20,876		155
C–30KAU	MB634xxx	31,500		178
C–40KAU	MB633xxx	41,184		220
C–50KAU	MB632xxx	52,164		245
C–75KAU	MB631xxx	75,140		300
C–100KAU	MB630xxx	102,144		332



Corner of 100KAU after metallization

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Rating		Symbol	Minimum	Maximum	Unit
Supply Voltage		V_{DD}	V_{SS}[2] –0.5	6.0	V
Input Voltage		V_I	V_{SS}[2] –0.5	V_{DD} +0.5	V
Output Voltage		V_O	V_{SS}[2] –0.5	V_{DD} +0.5	V
Storage Temperature	Ceramic Plastic	T_{stg}	–65 –40	+150 +125	°C
Temperature Under Bias	Ceramic Plastic	T_{bias}	–40 –25	+125 +85	°C

Notes: [1]Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]V_{SS} = 0 V.

1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input High Voltage for Normal Input	V_{IH}	2.2	—	—	V
Input Low Voltage for Normal Input	V_{IL}	—	—	0.8	V
Input High Voltage for CMOS Input	V_{IH}	V_{DD} x 0.7	—	—	V
Input Low Voltage for CMOS Input	V_{IL}	—	—	V_{DD} x 0.3	V
Operating Temperature	T_A	0	—	70	°C

CAPACITANCE (T_A = 25°C, V_{DD} = V_I = VO, F = 1 MHZ)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Pin Capacitance	C_{IN}	—	—	16	pF
Output Pin Capacitance	C_{OUT}	—	—	16	pF
I/O Pin Capacitance	C_{VO}	—	—	16	pF

ELECTRICAL CHARACTERISTICS (Continued)

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Current	I_{DDS}	Steady State[1]	—	—	0.2	mA
Output High Voltage for Normal Output (I_{OL} = 3 mA)	V_{OH}	I_{OH} = –2 mA	4.0	—	V_{DD}	V
Output High Voltage for Driver Output (I_{OL} = 12 mA)	V_{OH}	I_{OH} = –4 mA	4.0	—	V_{DD}	V
Output Low Voltage for Normal Output	V_{OL}	I_{OH} = 3.2 mA	V_{SS}	—	0.4	V
Output Low Voltage for Driver Output	V_{OL}	I_{OH} = 12.0 mA	V_{SS}	—	0.4	V
Input High Voltage for Normal Input	V_{IH}	—	2.2	—	—	V
Input Low Voltage for Normal INput	V_{IL}	—	—	—	0.8	V
Input High Voltage for CMOS Input	V_{IH}	—	V_{DD} x 0.7	—	—	V
Input Low Voltage for CMOS Input	V_{IL}	—	—	—	V_{DD} x 0.3	V
Input Leakage Current	I_{LI}	V_I = 0V – V_{DD}	–10	—	10	µA
Input Leakage Current	I_{LZ}	3-state V_I = 0V – V_{DD}	–10	—	10	µA
Input Pull-up/Down Resistor	R_P	V_{IH} = V_{DD} V_{OL} = V_{SS}	25	50	100	kΩ

Note: [1]V_{IH} = V_{DD}, V_{IL} = V_{SS}, and RAM inactive.

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Rating	Symbol	Minimum	Maximum[2]	Unit
Propagation Delay Time	t_{PLH}	(Typ) x 0.40[1]	(Typ) x 1.60[1]	ns
	t_{PHL}			
Enable Time	t_{PZL}			
	t_{PZH}			
Disable Time	t_{PLZ}			
	t_{PHZ}			

Notes: [1]Values for post-layout simulation, with 0°C < Tj ≤ 70°C (Tj: Estimated Junction Temperature). 0.35 and 1.70 are used for pre-layout simulation.

[2]This value is determined by the junction temperature, which is a function of power dissipation, thermal resistance of the selected package, and operating environment (power supply voltage and ambient temperature). Please refer to Chapter 5 of this section or the Design Manual for the details.

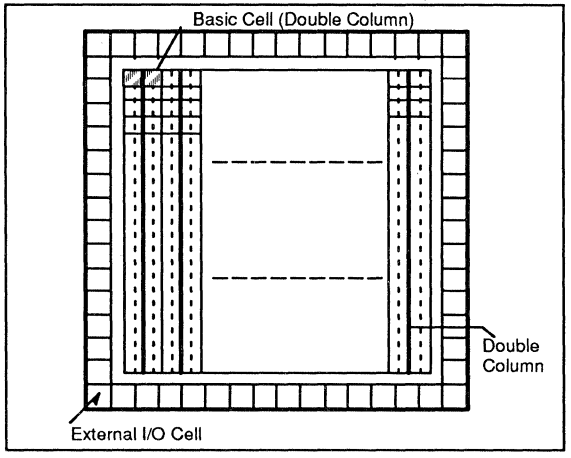
CHIP STRUCTURE

CHIP LAYOUT

On the CG21 gate array chip, the basic cells are configured in a matrix arranged in double parallel columns with no wiring channel between the double columns. External I/O cells are located around the basic cell matrix. Interconnection wires go over and across the columns of basic cells.

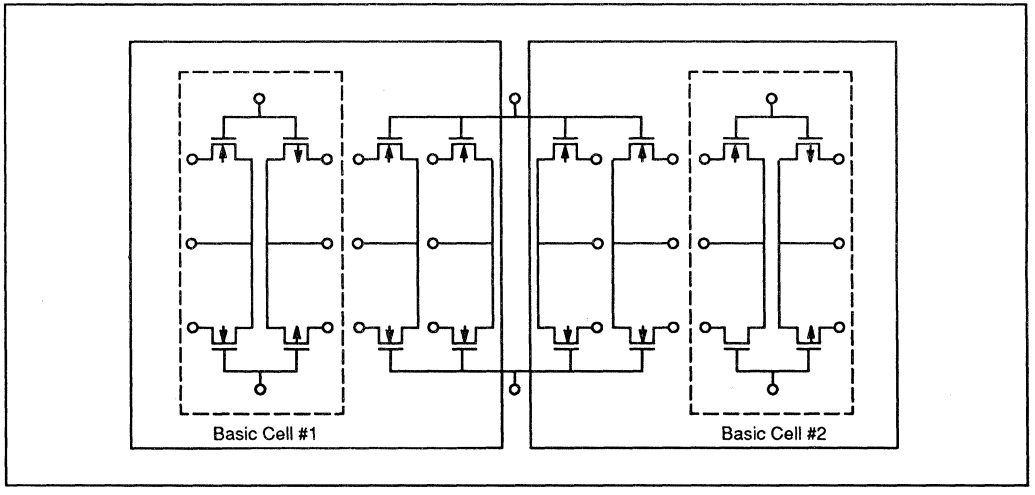
The structure of each device type is as follows:

C–10KAU	48 rows x 213 columns	= 10,224 BC
C–15KAU	58 rows x 267 columns	= 15,486 BC
C–20KAU	68 rows x 307 columns	= 20,876 BC
C–30KAU	84 rows x 375 columns	= 31,500 BC
C–40KAU	96 rows x 429 columns	= 41,184 BC
C–50KAU	108 rows x 483 columns	= 52,164 BC
C–75KAU	130 rows x 578 columns	= 75,140 BC
C–100KAU	152 rows x 672 columns	= 102,144 BC



CELL STRUCTURE

The basic cell is the structural element of the AU gate arrays. One basic cell consists of two pairs of P-channel and N–channel transistors and four small N-channel transistors. One basic cell can form a 2-input gate, 1 bit for RAM or 4 bits for ROM.



UNIT CELL AC CHARACTERISTICS

(Representative Values for Respresentative Unit Cells)

Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Output Transition	Propagation Delays (in ns) NDI (Fan-out) 1	2	3	4	5
Inverter	V1N	1	L → H	0.58	0.83	1.08	1.29	1.48
			H → L	0.55	0.72	0.86	0.97	1.07
Power Inverter	V2B	1	L → H	0.39	0.52	0.66	0.77	0.87
			H → L	0.39	0.52	0.66	0.74	0.80
2-Input NAND	N2N	1	L → H	0.65	0.90	1.15	1.36	1.55
			H → L	0.75	0.96	1.17	1.34	1.51
Power 2-Input NAND	N2B	3	L → H	1.07	1.20	1.34	1.45	1.55
			H → L	1.22	1.28	1.34	1.39	1.43
Power 2-Input NAND	N2K	2	L → H	0.49	0.62	0.76	0.87	0.97
			H → L	0.53	0.67	0.81	0.91	1.00
3-Input NAND	N3N	2	L → H	0.77	1.02	1.27	1.48	1.67
			H → L	0.95	1.24	1.53	1.77	1.99
Power 3-Input NAND	N3B	3	L → H	1.22	1.35	1.49	1.60	1.70
			H → L	1.44	1.50	1.56	1.61	1.65
2-Input NOR	R2N	1	L → H	0.94	1.38	1.82	2.19	2.53
			H → L	0.60	0.75	0.89	1.00	1.10
Power 2-Input NOR	R2B	3	L → H	1.28	1.41	1.55	1.66	1.76
			H → L	1.08	1.14	1.20	1.25	1.29
Power 2-Input NOR	R2K	2	L → H	0.66	0.87	1.08	1.25	1.42
			H → L	0.50	0.59	0.69	0.77	0.84
3-Input NOR	R3N	2	L → H	1.56	2.19	2.82	3.35	3.84
			H → L	0.64	0.81	0.95	1.06	1.16
Power 3-Input NOR	R3B	3	L → H	1.78	1.91	2.05	2.16	2.26
			H → L	1.18	1.24	1.30	1.35	1.39
4-Input NOR	R4N	2	L → H	2.15	2.97	3.79	4.48	5.12
			H → L	0.67	0.85	0.99	1.10	1.20
Power 4-Input NOR	R4B	4	L → H	2.19	2.32	2.46	2.57	2.67
			H → L	1.15	1.21	1.27	1.32	1.36
Non–SCAN Power D FF (CK→ Q)	FD2	7	L → H	1.51	1.64	1.78	1.89	1.99
			H → L	1.60	1.75	1.90	1.99	2.05
SCAN 1-Input D FF with Clock Inhibit (CK → Q)	SDA	12	L → H	2.74	2.87	3.01	3.12	3.22
			H → L	2.59	2.72	2.86	2.93	2.97

Note: Typical at V_{DD} = 5 V and Tj = 25°C
Estimated metal loading for C-30KAU (Level 4, Main Block)

INPUT BUFFER AC CHARACTERISTICS

Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Output Transition	Propagation Delays NDI (Fan-out)				
				1	2	3	4	5
Input Buffer	I2B	4	L → H	0.93	0.99	1.05	1.10	1.14
(True)			H → L	1.55	1.61	1.67	1.72	1.76
Clock Input Buffer	ILB	6	L → H	1.82	1.84	1.86	1.87	1.89
(True)			H → L	2.48	2.50	2.52	2.53	2.55

Note: Typical at V_{DD} = 5 V and Tj = 25°C
Estimated metal loading for C-30KAU

OUTPUT BUFFER AC CHARACTERISTICS

Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Output Transition	Propagation Delays C_L = 10 pF	C_L = 20 pF	C_L = 30 pF	C_L = 40 pF	C_L = 50 pF
Output Buffer	O2B	2	L → H	1.93	2.40	2.87	3.34	3.81
(True)			H → L	2.56	3.59	4.62	5.65	6.68
Power Output Buffer	O2L	2	H → H	2.18	2.50	2.82	3.14	3.46
(True)			H → L	2.37	2.71	3.05	3.39	3.73
3-state Output Buffer	O4T	4	L → H	2.79	3.26	3.73	4.20	4.67
(True)			H → L	3.63	4.66	5.69	6.72	7.75
Power 3-state	O4W	4	L → H	3.02	3.34	3.66	3.98	4.30
Output Buffer (True)			H → L	5.15	5.51	5.87	6.23	6.59

NOTE: Typical at V = 5 V and Tj = 25°C
Estimated metal loading for C-30KAU

AU CMOS Gate Array Package Options

Package Name	Package Material	DEVICE NAME							
		C-10KAU	C-15KAU	C-20KAU	C-30KAU	C-40KAU	C-50KAU	C-75KAU	C-100KAU
PGA-64	Ceramic	●	●	●	—	—	—	—	—
PGA-88	Ceramic	●	●	●	—	—	—	—	—
PGA-135	Ceramic	●	●	●	●	●	●	●	●
PGA-179	Ceramic	—	—	●	●	●	●	●	●
PGA-208	Ceramic	—	—	—	●	●	●	●	●
PGA-256	Ceramic	—	—	—	—	●	●	●	●
PGA-299	Ceramic	—	—	—	—	—	○	○	○
PGA-321	Ceramic	—	—	—	—	—	—	○	○
PGA-361	Ceramic	—	—	—	—	—	—	○	○
PGA-401	Ceramic	—	—	—	—	—	—	—	○
QFP-64	Plastic	●	●	●	—	—	—	—	—
QFP-80	Plastic	●	●	●	—	—	—	—	—
QFP-100	Plastic	●	●	●	—	—	—	—	—
QFP-120	Plastic	●	●	●	●	●	—	—	—
QFP-160	Plastic	—	●	●	●	●	—	—	—
PLCC-68	Plastic	●	●	●	—	—	—	—	—
PLCC-84	Plastic	●	●	●	—	—	—	—	—
SDIP-64	Plastic	●	●	●	—	—	—	—	—

Note: ● = Available
○ = Under Development
— = Not Available

AU CMOS Gate Array Package Descriptions

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
SDIP–64	Plastic	None	70 mil Lead Pitch	None	C–20KAU C–15KAU C–10KAU	80 80 85	50 55 60
PLCC–68	Plastic	None	70 mil Lead Pitch Gull-wing	None	C–20KAU C–15KAU C–10KAU	50 55 60	35 40 40
PLCC–84	Plastic	None	30 mil Lead Pitch Gull-wing	None	C–20KAU C–15KAU C–10KAU	50 50 55	35 35 40
QFP–64	Plastic	None	100 mil Lead Pitch Gull-wing	None	C–20KAU C–15KAU C–10KAU	80 85 90	55 60 65
QFP–80	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	C–20KAU C–15KAU C–10KAU	80 85 90	55 60 65
QFP–100	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	C–20KAU C–15KAU C–10KAU	80 85 90	55 60 65
QFP–120	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	C–40KAU C–30KAU C–20KAU C–15KAU C–10K	65 70	40 50
QFP–160	Plastic	None	0.65 mm Lead Pitch Gull-wing	Yes	C–40KAU C–30KAU C–20KAU C–15KAU	59 70	39 50
PGA–64	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C–10KAU C–15KAU C–20KAU	40	20
PGA–88	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C–10KAU C–15KAU C–20KAU	40	20
PGA–135	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	All AU	30	15
PGA–179	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C–30KAU– C–100KAU C–20KAU	25 30	13 15
PGA–208	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C–30KAU– C–100KAU	23	12

AU CMOS Gate Array Package Descriptions (Continued)

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
PGA–256	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	C–30KAU–C–100KAU	19	9
PGA–299	Ceramic	Down	100 mil Pin Pitch Through hole	Yes	C–50KAU–C–100KAU	19	9
PGA–321	Ceramic	Down	70 mil Stagger Through hole	Yes	C–75KAU–C–100KAU	22-24	11-13
PGA–361	Ceramic	Down	70 mil Stagger Through hole	Yes	C–75KAU–C–100KAU	22-24	11-13
PGA–401	Ceramic	Down	70 mil Stagger Through hole	Yes	C–100KAU	22-24	11-13

FUNCTIONAL INDEX OF UNIT CELL LIBRARY

Note: The load unit (lu) is a normalized loading unit of capacitance representing the input load of an inverter without metal interconnection.

Inverter and Buffer Family				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (lu)**	**Polarity**
V1N	Inverter	1	18	Neg
V2B	Power Inverter	1	36	Neg
V1L	Inverting Clock Buffer	2	55	Neg
B1N	True Buffer	1	18	Pos
BD3	True Delay Buffer (> 5 ns)	5	18	Pos
BD4	Delay Cell (> 4 ns)	4	6	Pos
BD5	Delay Cell (>10 ns)	9	18	Pos
BD6	Delay Cell (>22 ns)	17	18	Pos
Clock Buffer Family				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (lu)**	**Polarity**
K1B	True Clock Buffer	2	36	Pos
K2B	Power Clock Buffer	3	55	Pos
K3B	Gated Clock (AND) Buffer	2	36	Pos
K4B	Gated Clock (OR) Buffer	2	36	Pos
K5B	Gated Clock (NAND) Buffer	3	36	Neg
KAB	Block Clock (OR) Buffer	3	55	Pos
KBB	Block Clock (OR x 10) Buffer	30	55	Pos
KDB	Block Clock (OR x 10) Buffer	32	55	Pos
KEB	Block Clock Buffer	23	55	Pos
NAND Family				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (lu)**	
N2N	2-input NAND	1	18	
N2B	Power 2-input NAND	3	36	
N2K	Fast Power 2-input NAND	2	36	
N3N	3-input NAND	2	14	
N3B	Power 3-input NAND	3	36	
N4N	4-input NAND	2	10	
N4B	Power 4-input NAND	4	36	
N6B	Power 6-input NAND	5	36	
N8B	Power 8-input NAND	6	36	
N9B	Power 9-input NAND	8	36	
NCB	Power 12-input NAND	10	36	
NGB	Power 16-input NAND	11	36	

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

NOR Family				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (Iu)**	
R2N	2-input NOR	1	14	
R2B	Power 2-input NOR	3	36	
R2K	Power 2-input NOR	2	36	
R3N	3-input NOR	2	10	
R3B	Power 3-input NOR	3	36	
R4N	4-input NOR	2	6	
R4B	Power 4-input NOR	4	36	
R6B	Power 6-input NOR	5	36	
R8B	Power 8-input NOR	6	36	
R9B	Power 9-input NOR	8	36	
RCB	Power 12-input NOR	10	36	
RGB	Power 16-input NOR	11	36	
AND Family				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (Iu)**	
N2P	Power 2-input AND	2	36	
N3P	Power 3-input AND	3	36	
N4P	Power 4-input AND	3	36	
N8P	Power 8-input AND	6	36	
OR Family				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (Iu)**	
R2P	Power 2-input OR	2	36	
R3P	Power 3-input OR	3	36	
R4P	Power 4-input OR	3	36	
R8P	Power 8-input OR	6	36	
Exclusive NOR/OR Family (EXOR/EXNOR)				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (Iu)**	**Polarity**
X1N	Exclusive NOR	3	18	Neg
X1B	Power Exclusive NOR	4	36	Neg
X2N	Exclusive OR	3	14	Pos
X2B	Power Exclusive OR	4	36	Neg
X3N	3-input Exclusive NOR	5	14	Neg
X3B	Power 3-input Exclusive NOR	6	36	Neg
X4N	3-input Exclusive OR	5	14	Pos
X4B	Power 3-input Exclusive OR	6	36	Pos

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

AND-OR-Inverter Family (AOI)

Unit Cell Name	Description	Basic Cells	Drive (Iu)	
D23	2-wide 2-AND 3-input AOI	2	14	
D14	2-wide 3-AND 4-input AOI	2	14	
D24	2-wide 2-AND 4-input AOI	2	14	
D34	3-wide 2-AND 4-input AOI	2	10	
D36	3-wide 2-AND 6-input AOI	3	10	
D44	2-wide 2-OR 2-AND 4-input AOI	2	10	

Note: AND-OR-Inverter unit cells are useful in implementing sum-of-products (SOP) expressions.

OR-AND-Inverter Family (OAI)

Unit Cell Name	Description	Basic Cells	Drive (Iu)	
G23	2-wide 2-OR 3-input OAI	2	18	
G14	2-wide 3-OR 4-input OAI	2	10	
G24	2-wide 2-OR 4-input OAI	2	10	
G34	3-wide 2-OR 4-input OAI	2	10	
G44	2-wide 2-AND 2-OR 4-input OAI	2	14	

Note: OR-AND-Inverter unit cells are useful in implementing product-of-sums (POS) expressions.

Multiplexer Family

Unit Cell Name	Type	Description	Basic Cells	Drive (Iu)	Function
T24*	4:1	Power 4, 2 ANDs into 4 NOR Multiplexer	6	36	SOP
T26*	6:1	Power 6, 2 ANDs into 6 NOR Multiplexer	10	36	SOP
T28*	8:1	Power 8, 2 ANDs into 8 NOR Multiplexer	11	36	SOP
T32	2:1	Power 2, 3 ANDs into 2 NOR Multiplexer	5	36	SOP
T33*	3:1	Power 3, 3 ANDs into 3 NOR Multiplexer	7	36	SOP
T34*	4:1	Power 4, 3 ANDs into 4 NOR Multiplexer	9	36	SOP
T42	2:1	Power 2, 4 ANDs into 2 NOR Multiplexer	6	36	SOP
T43	3:1	Power 3, 4 ANDs into 3 NOR Multiplexer	10	36	SOP
T44	4:1	Power 4, 4 ANDs into 4 NOR Multiplexer	11	36	SOP
T54	4:1	Power 2, 2–3–4 ANDs into 4 NOR Multiplexer	10	36	SOP
U24*	4:1	Power 4, 2 OR into 4 NAND Multiplexer	6	36	POS
U26*	6:1	Power 6, 2 OR into 6 NAND Multiplexer	9	36	POS
U28*	8:1	Power 8, 2 OR into 8 NAND Multiplexer	11	36	POS
U32	2:1	Power 2, 3 OR into 2 NAND Multiplexer	5	36	POS
U33*	3:1	Power 3, 3 OR into 3 NAND Multiplexer	7	36	POS
U34*	4:1	Power 4, 3 OR into 4 NAND Multiplexer	9	36	POS
U42	2:1	Power 2, 4 OR into 2 NAND Multiplexer	6	36	POS
U43	3:1	Power 3, 4 OR into 3 NAND Multiplexer	9	36	POS
U44	4:1	Power 4, 4 OR into 4 NAND Multiplexer	11	36	POS

* Convenient for typical multiplexer applications

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Data Selectors/Multiplexers

Unit Cell Name	Type	Description	Basic Cells	Drive (Iu)	Selects	Output	Bit Width
P24*	2:1	Data Selector	12	36	S, XS	Q	4
T2E	2:1	Dual Selector	5	18	S	XQ	2
T2F	2:1	Selector	8	18	S	XQ	4
T2B*	2:1	Selector	2	18	S, XS	XQ	1
T2C*	2:1	Selector	4	18	S, XS	XQ	2
T2D*	2:1	Selector	2	14	S, XS	XQ	1
T5A*	4:1	Selector	5	9	S, XS	XQ	1
V3A*	1:2	Selector	2	14	S, XS	XQ	1
V3B*	1:2	Dual Selector	4	14	S, XS	XQ	2

* These are transmission gate devices whose outputs can be tied because they can be inhibited with true/inverted selects.

Decoders

Unit Cell Name	Type	Description	Basic Cells	Drive (Iu)	Active Level Outputs	Enable	
DE2	2:4	Decoder	5	18	Low	—	
DE3	3:8	Decoder	15	14	Low	—	
DE4	2:4	Decoder	8	14	Low	Low	
DE6	3:8	Decoder	30	18	Low	1 High 2 Low	

Internal Bus Unit Cells

Unit Cell Name	Type Description	Basic Cells	Drive (Iu)	Bus Size	Enable	
B11	1-bit Bus Driver	5	36	1	Low	
B21	2-bit Bus Driver	9	36	2	Low	
B41	4-bit Bus Driver	17	36	4	Low	
B81	8-bit Bus Driver	33	36	8	Low	
B12	1-bit Block Bus Driver	7	72	1	Low	
B22	2-bit Block Bus Driver	13	72	2	Low	
B42	4-bit Block Bus Driver	25	72	4	Low	

Data Latch Family

Unit Cell Name	Description	Basic Cells	Drive (Iu)	Enable	Bits	Output	Clear
YL2	Data Latch with TM	5	36	High	1	Q	—
YL4	Data Latch with TM	14	36	High	4	Q	—
LTK	Data Latch	4	18	Low	1	Q, XQ	Async
LTL	Data Latch with Clear	5	18	Low	1	Q, XQ	Async
LTM	Data Latch with Clear	16	18	Low	4	Q, XQ	—
LT1	S-R Latch with Clear	4	18	Low	1	Q, XQ	Async
LT4	Data Latch	14	18	Low	4	Q, XQ	—

Note: Y-type latches incorporate inhibit inputs and transparent mode (TM) to facilitate scan implementation.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Scan Flip-flop Family (Positive-Edge Triggered)

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Output	Clear	Preset	Clock Inhibit
SDH	Scan D Flip-flop with 2:1 Multiplexed inputs	14	36	1	Q, XQ	Async	—	Yes
SDJ	Scan D Flip-flop with 4:1 Multiplexed inputs	15	36	1	Q, XQ	Async	—	Yes
SDK	Scan D Flip-flop with 3:1 Multiplexed inputs	16	36	1	Q, XQ	Async	—	Yes
SJH	Scan J–K Flip-flop	16	36	1	Q, XQ	Async	—	Yes
SDD	Scan DFlip-flop with 2:1 Multiplexed inputs	16	36	1	Q, XQ	Async	Async	Yes
SDA	Scan 1-input D Flip-flop	12	36	1	Q, XQ	—	—	Yes
SDB	Scan 1-input D Flip-flop	42	36	4	Q, XQ	—	—	Yes
SHA	Scan 1-input D Flip-flop	68	18	8	Q, XQ	—	—	Yes
SHB	Scan 1-input D Flip-flop	62	18	8	Q	—	—	Yes
SHC	Scan 1-input D Flip-flop	62	18	8	XQ	—	—	Yes
SHJ	Scan D Flip-flop with 2:1 Multiplexed inputs	78	18	8	Q, XQ	—	—	Yes
SHK	Scan D Flip-flop with 3:1 Multiplexed inputs	88	18	8	Q, XQ	—	—	Yes
SFDM	Scan 1-input D Flip-flop	10	18	1	Q, XQ, SO	—	—	Yes
SFDO	Scan 1-input D Flip-flop	11	18	1	Q, XQ, SO	Yes	—	Yes
SFDP	Scan 1-input D Flip-flop	12	18	1	Q, XQ, SO	Yes	Yes	Yes
SFDR	Scan 4-input D Flip-flop	36	18	4	Q, XQ, SO	Yes	—	Yes
SFDS	Scan 4-input D Flip-flop	31	18	4	Q, XQ, SO	—	—	Yes
SFJD	Scan J-K D Flip-flop	14	18	1	Q, XQ, SO	—	—	Yes

Non Scan Flip-flop Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs	Clear	Preset	Clock Edge
FDN	Non-Scan D Flip-flop with Set	7	18	1	Q, XQ	—	Async	Pos
FDM	Non-Scan D F	6	18	1	Q, XQ	—	—	Pos
FDO	Non-Scan D Flip-flop with Reset	7	18	1	Q, XQ	Async	—	Pos
FDP	Non-Scan D Flip-flop with Set and Reset	8	18	1	Q, XQ	Async	Async	Pos
FDQ	Non-Scan D Flip-flop	21	18	4	Q	—	—	Neg
FDR	Non-Scan D Flip-flop	26	18	4	Q	Async	—	Pos
FDS	Non-Scan D Flip-flop	20	18	4	Q	—	—	Pos
FD2	Non-Scan Power D Flip-flop	7	36	1	Q, XQ	—	—	Neg
FD3	Non-Scan Power D Flip-flop	8	36	1	Q, XQ	—	Async	Neg
FD4	Non-Scan Power D Flip-flop	9	36	1	Q, XQ	Async	Async	Neg
FD5	Non-Scan Power D Flip-flop	8	36	1	Q, XQ	Async	—	Neg
FJD	Non-ScanPower J-K Flip-flop	12	36	1	Q, XQ	Async	—	Pos

Note: Synchronous flip-flops may be constructed by adding a simple AND gate (such as N2P) to the input of a flip-flop to create a synchronous clear.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Binary Counter Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs[1]	Load	Clear	Enable	Carry In	Up/ Down
SC7[2]	Scan Synchronous Binary Counter with Parallel Load	62	36	4	Q, XQ, CO (S)	Sync	—	Low	High	Up
SC8[2]	Scan Synchronous Binary Counter with Parallel Load	66	36	4	Q, XQ, CO (S)	Sync	—	High	Low	Down
C11[3]	Non-Scan Flip-flop for Counter	11	18	—	Q, XQ	—	—	—	—	—
C41	Non-Scan Binary Asynchronous Counter	24	18	4	Q, (A)	—	Async	—	—	Up
C42	Non-Scan Binary Synchronous Counter	32	18	4	Q	—	Async	—	—	Up
C43	Non-Scan Binary Synchronous Counter	48	18	4	Q, CO(S)	Sync	Async	High	High	Up
C45	Non-Scan Binary Synchronous Counter	48	18	4	Q, CO	Sync	Sync	High	High	Up
C47	Non-Scan Binary Synchronous Counter	68	18	4	Q, CO	Async	—	Low	Low	Up/Down
SC43[2]	Scan synchronous Binary Counter	59	18	4	Q, CO	Sync	Async	High	High	Up
SC47[2]	Scan synchronous Binary Counter	78	18	4	Q, CO	Async	—	Low	Low	Up/Down

Notes: 1. (S), (A) indicate the counter is (S)ynchronous or (A)synchronous.
2. Scan counters include clock inhibit and high drive (C_{DR} = 36 lu). For non-Scan counters C_{DR} = 18 lu
3. C11 may by used for purposes other than counters.

Shift Register Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bit Width	Load	Outputs	Clock Polarity
FS1	Serial-in Parallel-out Shift Register	18	16	4	Serial-In only	Q-Parallel	Neg
FS2	Shift Register with Synchronous Load	30	16	4	Sync-High	Q-Parallel	Neg
FS3	Shift Register with Asynchronous Load	34	18	4	Async-Low	Q-Parallel	Pos
SR1	Serial-in Parallel-out Shift Register with Scan	36	36	4	Serial-In only	Q-Parallel	Pos

Datapath Operators (Adder, ALU, Parity)

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bit Width	Outputs	Carry In
MC4	Magnitude Comparator	42	18 (=) 10(<,>)	4	A>B, A=B, A<B	A>B,A=B,ALB
A1A	1-bit Half Adder	5	36	1	S, $\overline{CO}$	—
A1N	1-bit Full Adder	8	18	1	S, CO	CI
A2N	2-bit Full Adder	16	14	2	S, CO	CI
A4H	4-bit Binary Full Adder w/Fast Carry	48	18(CO) 14(S)	4	S, CO	CI
PE5	Even Parity Generator/Checker	12	36	5	EVEN, $\overline{ODD}$	—
PO5	Odd Parity Generator/Checker	12	36	5	ODD, $\overline{EVEN}$	—
PE8	Even Parity Generator/Checker	18	18	8	EVEN, $\overline{ODD}$	—
PO8	Odd Parity Generator/Checker	18	18	8	ODD, $\overline{EVEN}$	—
PE9	Even Parity Generator/Checker	22	18	9	EVEN, $\overline{ODD}$	—
PO9	Odd Parity Generator/Checker	22	18	9	ODD, $\overline{EVEN}$	—

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Miscellaneous Cells

Unit Cell Name	Description	Basic Cells			Function	
Z00	0 Clip	0			Tie to V_{SS}	
Z01	1 Clip	0			Tie to V_{DD}	

Input Buffer Family

Unit Cell Name	Description	Basic Cells	Drive (Iu)	Logic Level	Type	Input/ Output Polarity
I1B	Input Buffer	5	36	TTL	Signal	Invert
I1BU	I1B with Pull-up Resistance	5	36	TTL	Signal	Invert
I1BD	I1B with Pull-down Resistance	5	36	TTL	Signal	Invert
I2B	Input Buffer	4	36	TTL	Signal	True
I2BU	I2B with Pull-up Resistance	4	36	TTL	Signal	True
I2BD	I2B with Pull-down Resistance	4	36	TTL	Signal	True
IKB	Clock Input Buffer	4	72	TTL	Clock	Invert
IKBU	Ikb With Pull-up Resistance	4	72	TTL	Clock	Invert
IKBD	IKB with Pull-down Resistance	4	72	TTL	Clock	Invert
ILB	Clock Input Buffer	6	72	TTL	Clock	True
ILBU	ILB with Pull-up Resistance	6	72	TTL	Clock	True
ILBD	ILB with Pull-down Resistance	6	72	TTL	Clock	True
I1C	CMOS Interface Input Buffer	5	36	CMOS	Signal	Invert
I1CU	I1C with Pull-up Resistance	5	36	CMOS	Signal	Invert
I1CD	I1C with Pull-down Resistance	5	36	CMOS	Signal	Invert
I2C	CMOS Interface Input Buffer	4	36	CMOS	Signal	True
I2CU	I2C with Pull-up Resistance	4	36	CMOS	Signal	True
I2CD	I2C with Pull-down Resistance	4	36	CMOS	Signal	True
I1S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	Invert
I1SU	I1S with Pull-up Resistance	8	18	CMOS	Schmitt	Invert
I1SD	I1S with Pull-down Resistance	8	18	CMOS	Schmitt	Invert
I2S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	True
I2SU	I2S with Pull-up Resistance	8	18	CMOS	Schmitt	True
I2SD	I2S with Pull-down Resistance	8	18	CMOS	Schmitt	True
I1R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	Invert
I1RU	I1R with Pull-up Resistance	8	18	TTL	Schmitt	Invert
I1RD	I1R with Pull-down Resistance	8	18	TTL	Schmitt	Invert
I2R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	True
I2RU	I2R With Pull-up Resistance	8	18	TTL	Schmitt	True
I2RD	I2R with Pull-down Resistance	8	18	TTL	Schmitt	True
IKC	Clock Input Buffer	4	200	CMOS	Clock	Invert
IKCU	IKC with Pull-up Resistance	4	200	CMOS	Clock	Invert
IKCD	IKC with Pull-down Resistance	4	200	CMOS	Clock	Invert
ILC	Clock Input Buffer	6	200	CMOS	Clock	True
ILCU	IKC with Pull-up Resistance	6	200	CMOS	Clock	True
ILCD	IKC with Pull-down Resistance	6	200	CMOS	Clock	True

Note: A "U" suffixed to the name of an input buffer indicates pull-up resistance of 50KΩ (typical) and a "D" indicates a pull-down resistance of the equivalent value.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

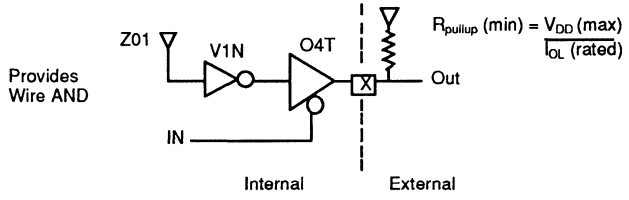
Output Buffer Family

Unit Cell Name	Description	Basic Cells	Drive (I_{OL})	Logic[2] Level	Type	Edge Rate Control	Input/ Output Polarity
O1B	Output Buffer	3	3.2 mA	TTL/CMOS	Standard	No	Invert
O1L	Power Output Buffer	3	12 mA	TTL/CMOS	Standard	No	Invert
O1S	Power Output Buffer	5	12 mA	TTL/CMOS	Standard	Yes	Invert
O2B	Output Buffer	2	3.2 mA	TTL/CMOS	Standard	No	True
O2L	Power Output Buffer	2	12 mA	TTL/CMOS	Standard	No	True
O2S	Power Output Buffer	4	12 mA	TTL/CMOS	Standard	Yes	True
O44[1]	3-state Output Buffer	4	3.2 mA	TTL/CMOS	3-state	No	True
O4W[1]	Power 3-state Output Buffer	4	12 mA	TTL/CMOS	3-state	No	True
O4S[1]	Power 3-state Output Buffer	5	12 mA	TTL/CMOS	3-state	Yes	True
O1R	Output Buffer	5	3.2 mA	TTL/CMOS	Standard	Yes	Invert
O2R	Output Buffer	4	3.2 mA	TTL/CMOS	Standard	Yes	True
O4R[1]	3-state Output Buffer	5	3.2 mA	TTL/CMOS	3-state	Yes	True
O2BF	Output Buffer	2	8 mA	TTL/CMOS	Standard	No	True
O2RF	Output Buffer	4	8 mA	TTL/CMOS	Standard	Yes	True
O4RF	3-state Output Buffer	5	8 mA	TTL/CMOS	3-state	Yes	True
O4TF	3-state Output Buffer	4	8 mA	TTL/CMOS	3-state	No	True

Notes: 1. While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs.

2. Totem pole outputs, such as these buffers have, can drive both TTL and CMOS levels. Voltage margins depend on actual source or sink current (see DC specifications).

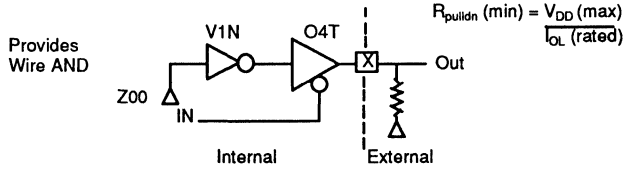
Example of Open Drain Output



R_{pullup} (min) = V_{DD} (max) / $\overline{I_{OL}}$ (rated)

In	X	Out
0	L	L
1	Z	H

Example Of Open Source Output



R_{pulldn} (min) = V_{DD} (max) / $\overline{I_{OL}}$ (rated)

In	X	Out
0	H	H
1	Z	L

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectional I/O Buffers (Buses)

Unit Cell Name	Description	Basic Cells	Drive (I_{OL})	Logic Level	Edge Rate Control	Input/ Output Polarity
H6T	3-state Output and Input Buffer	8	3.2 mA	TTL	No	True
H6TU	H6T with Pull-up Resistance	8	3.2 mA	TTL	No	True
H6TD	H6T with Pull-down Resistance	8	3.2 mA	TTL	No	True
H6W	Power 3-state Output and Input Buffer	8	12 mA	TTL	No	True
H6WU	H6W with Pull-up Resistance	8	12 mA	TTL	No	True
H6WD	H6W with Pull-down Resistance	8	12 mA	TTL	No	True
H6C	3-state Output and Interface Input Buffer	8	3.2 mA	CMOS	No	True
H6CU	H6C with Pull-up Resistance	8	3.2 mA	CMOS	No	True
H6CD	H6C with Pull-down Resistance	8	3.2 mA	CMOS	No	True
H6E	Power 3-state Output and Interface Input Buffer	8	12 mA	CMOS	No	True
H6EU	H6E with Pull-up Resistance	8	12 mA	CMOS	No	True
H6ED	H6E with Pull-down Resistance	8	12 mA	CMOS	No	True
H6S	3-state Output and Schmitt Trigger Input Buffer	12	3.2 mA	CMOS	No	True
H6SU	H6S with Pull-up Resistance	12	3.2 mA	CMOS	No	True
H6SD	H6S with Pull-down Resistance	12	3.2 mA	CMOS	No	True
H6R	3-state Output and Schmitt Trigger Input Buffer	12	3.2 mA	TTL	No	True
H6RU	H6R with Pull-up Resistance	12	3.2 mA	TTL	No	True
H6RD	H6R with Pull-down Resistance	12	3.2 mA	TTL	No	True
H8T	3-state Output and Input Buffer	9	3.2 mA	TTL	Yes	True
H8TU	H8T with Pull-up Resistance	9	3.2 mA	TTL	Yes	True
H8TD	H8T with Pull-down Resistance	9	3.2 mA	TTL	Yes	True
H8W	Power 3-state Output and Input Buffer	9	12 mA	TTL	Yes	True
H8WU	H8W with Pull-up Resistance	9	12 mA	TTL	Yes	True
H8WD	H8W with Pull-down Resistance	9	12 mA	TTL	Yes	True
H8C	3-state Output Buffer and Interface Input Buffer	9	3.2 mA	CMOS	Yes	True
H8CU	H8C with Pull-up Resistance	9	3.2 mA	CMOS	Yes	True
H8CD	H8C with Pull-down Resistance	9	3.2 mA	CMOS	Yes	True

Note: A "U" suffixed to the name of a bidirectional buffer indicates a pull-up resistance of 50Ω (typical) and a "D" indicates a pull-down resistance of the equivalent value.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectional I/O Buffers (Buses) continued

Unit Cell Name	Description	Basic Cells	Drive (I_{OL})	Input Logic Level	Edge Rate Control	Input/ Output Polarity
H8E	Power 3-state Output Buffer and Interface Input Buffer	9	12 mA	CMOS	Yes	True
H8EU	H8E with Pull-up Resistance	9	12 mA	CMOS	Yes	True
H8ED	H8E with Pull-down Resistance	9	12 mA	CMOS	Yes	True
H8S	3-state Output and Schmitt Trigger Input Buffer	13	3.2 mA	CMOS	Yes	True
H8SU	H8S with Pull-up Resistance	13	3.2 mA	CMOS	Yes	True
H8SD	H8S with Pull-down Resistance	13	3.2 mA	CMOS	Yes	True
H8R	3-state Output and Schmitt Trigger Input Buffer	13	3.2 mA	TTL	Yes	True
H8RU	H8R with Pull-up Resistance	13	3.2 mA	TTL	Yes	True
H8RD	H8R with Pull-down Resistance	13	3.2 mA	TTL	Yes	True
H6TF	3-state Output and Schmitt Trigger Input Buffer	8	8 mA	TTL	No	True
H6TFU	H6TF with Pull-up Resistance	8	8 mA	TTL	No	True
H6TFD	H6TF with Pull-down Resistance	8	8 mA	TTL	No	True
H6CF	3-state Output and Input Buffer	8	8 mA	CMOS	No	True
H6CFU	H6CF with Pull-up Resistance	8	8 mA	CMOS	No	True
H6CFD	H6CF with Pull-down Resistance	8	8 mA	CMOS	No	True
H8TF	3-state Output and Input Buffer	9	8 mA	TTL	Yes	True
H8TFU	H8TF with Pull-up Resistance	9	8 mA	TTL	Yes	True
H8TFD	H8TF with Pull-down Resistance	9	8 mA	TTL	Yes	True
H8CF	3-state Output and Input Buffer	9	8 mA	CMOS	Yes	True
H8CFU	H8CF with Pull-up Resistance	9	8 mA	CMOS	Yes	True
H8CFD	H8CF with Pull-down Resistance	9	8 mA	CMOS	Yes	True
H8W2	3-state Output and Input Buffer	8	24 mA	TTL	Yes	True
H8W1	H8W2 with Pull-up Resistance	8	24 mA	TTL	Yes	True
H8W0	H8W2 with Pull-down Resistance	8	24 mA	TTL	Yes	True
H8E2	3-state Output and Input Buffer	8	24 mA	CMOS	Yes	True
H8E1	H8E2 with Pull-up Resistance	8	24 mA	CMOS	Yes	True
H8E0	H8E2 with Pull-down Resistance	8	24 mA	CMOS	Yes	True

Note: While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs, which includes all bidirectional buffers.

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

CG21 Series 0.8-micron CMOS Gate Arrays

DESCRIPTION

The CG21 series of 0.8 µm CMOS gate arrays are currently available in five device types with from 30K to 100K gates. Three more CG21 arrays, ranging from 10K to 20K gates, are now under development. These arrays achieve the ultra fast speed of 0.37 ps per gate. Thanks to the channel-free (sea-of-gates) structure of the CG21 gate array, CG21 basic cells can be used for logic cells, memory cells, or wiring area in order to implement the desired functions. The full utilization of the array surface and the three-layer metal interconnect technology produce a 75 percent maximum gate usability ratio.

The logic and I/O cells for the CG21 series are functionally compatible with Fujitsu's AU, UHB, and CG10 series of gate arrays to simplify upgrading. User-specifiable RAM and ROM configurations are also available. These gate arrays facilitate the implementation of large-scale devices such as computer and graphic processors on single chips.

FEATURES

- 0.8 micron CMOS sea-of-gates technology
  –3 layer metal interconnect
- Ultra high speed
  – 0.37 ns/gate for 2-input NAND with F/O = 2
  – 0.55 ns/gate for power 2-input NAND with F/O = 2
- High basic cell usage
  – 75% maximum for logic with RAM/ROM
  – 45% maximum for logic only
- High sink current capability
  – sink current up to 12 mA, 24 mA planned
- Minimum delay clock buffer true option
- High current clock drivers
  –Low-skew clock signal distribution
- Extensive unit cell library (logic cell, RAM, ROM)
  –Unit cells functionally compatible with Fujitsu's AU, UHB, and CG10 gate array series
- Automatic test pattern generation optional
- On-chip pull-up/pull-down resistors
- High pin count plastic and ceramic packages
- High-density RAM and ROM compilers
  – up to 18K bit RAM compilation
  – up to 64K ROM compilation

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PRODUCT FAMILY

Device	Part Number	BCs on Chip (2-input gate +4 N-ch Tr)	Usable BCs	Max Signal I/O	Available Packages[1]	
					Plastic	Ceramic
CG21103	MBCG21103xxx[3]	10,224	75% max. for Logic with RAM,ROM 45% max. for Logic only (Preliminary values, to be upgraded)	108	SDIP-64, QFP-64, -80, -100, -120, PLCC-68, -84	PGA-64, 88, -135
CG21153	MBCG21153xxx[3]	15,486		142	SDIP-64, QFP-64, -80 -100, -120, -160, PLCC-68, -84	PGA-64, -88, -135
CG21203	MBCG21203xxx[3]	20,876		155	SDIP-64, QFP-64, -80, -100, -120, -160, PLCC-68, -84	PGA-64, -88, -135, -179
CG21303	MBCG21303xxx	31,500		178	QFP-120, -160	PGA-88, -135, -179, 208
CG21403	MBCG21403xxx	41,184		220	QFP-120, -160 SQFP-176[2], -208[2]	PGA-135, -179, 208, -256
CG21503	MBCG21503xxx	52,164		245	QFP-120, -160, -196[2] SQFP-176[2], -208[2]	PGA-135, -179, 208, -256, -299[2]
CG21753	MBCG21753xxx	75,140		284	QFP-196[2], -232[2] SQFP-176[2], -208[2]	PGA-135, -179, 208, -256, -299[2], -321[2], -361[2]
CG21104	MBCG21104xxx	102,144		332	QFP-196[2], -232[2] SQFP-208[2], -256[2]	PGA-135, -179, 208, -256, -299, -321[2], -361, -401[2]

[1]SDIP = Skinny dual in-line package, PGA = Pin grid array, QFP = Quad flat package, PLCC = Plastic leadless chip carrier, SQFP = Skinny quad flat package
[2]Planned
[3]Under development

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Rating		Symbol	Minimum	Maximum	Unit
Supply Voltage		V_{DD}	V_{SS}[2] –0.5	6.0	V
Input Voltage		V_I	V_{SS}[2] –0.5	V_{DD} +0.5	V
Output Voltage		V_O	V_{SS}[2] –0.5	V_{DD} +0.5	V
Storage Temperature	Ceramic Plastic	T_{stg}	–65 –40	+150 +125	°C
Temperature Under Bias	Ceramic Plastic	T_{bias}	–40 –25	+125 +85	°C

Notes: [1]Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]V_{SS} = 0 V.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input High Voltage for Normal Input	V_{IH}	2.2	—	—	V
Input Low Voltage for Normal Input	V_{IL}	—	—	0.8	V
Input High Voltage for CMOS Input	V_{IH}	V_{DD} x 0.7	—	—	V
Input Low Voltage for CMOS Input	V_{IL}	—	—	V_{DD} x 0.3	V
Operating Temperature	T_A	0	—	70	°C

CAPACITANCE (T_A = 25°C, V_{DD} = V_I = VO, F = 1 MHZ)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Pin Capacitance	C_{IN}	—	—	16	pF
Output Pin Capacitance	C_{OUT}	—	—	16	pF
I/O Pin Capacitance	C_{VO}	—	—	16	pF

ELECTRICAL CHARACTERISTICS (Continued)

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Current	I_{DDS}	Steady State[1]	—	—	0.2	mA
Output High Voltage for Normal Output (I_{OL} = 3 mA or 8 mA)	V_{OH}	I_{OH} = –2 mA	4.0	—	V_{DD}	V
Output High Voltage for Driver Output (I_{OL} = 12 mA)	V_{OH}	I_{OH} = –4 mA	4.0	—	V_{DD}	V
Output Low Voltage for Normal Output (I_{OL} = 3 mA or 8 mA)	V_{OL}	I_{OL} = 3.2 mA or 8 mA	V_{SS}	—	0.4	V
Output Low Voltage for Driver Output (I_{OL} = 12 mA)	V_{OL}	I_{OL} = 12.0 mA	V_{SS}	—	0.4	V
Input High Voltage for Normal Input	V_{IH}	—	2.2	—	—	V
Input Low Voltage for Normal INput	V_{IL}	—	—	—	0.8	V
Input High Voltage for CMOS Input	V_{IH}	—	V_{DD} x 0.7	—	—	V
Input Low Voltage for CMOS Input	V_{IL}	—	—	—	V_{DD} x 0.3	V
Input Leakage Current	I_{LI}	V_I = 0V – V_{DD}	–10	—	10	µA
Input Leakage Current	I_{LZ}	3-state V_I = 0V – V_{DD}	–10	—	10	µA
Input Pull-up/Down Resistor	R_P	V_{IH} = V_{DD} V_{OL} = V_{SS}	25	50	100	kΩ

Note: [1]V_{IH} = V_{DD}, V_{IL} = V_{SS}, and RAM inactive.

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Rating	Symbol	Minimum	Maximum[1]	Unit
Propagation Delay Time	t_{PLH}	(Typ) x 0.40[2,3]	(Typ) x 1.55[2] (Typ) x 1.60[3]	ns
	t_{PHL}			
Enable Time	t_{PZL}			
	t_{PZH}			
Disable Time	t_{PLZ}			
	t_{PHZ}			

Notes: [1]This value is determined by the junction temperature, which is a function of power dissipation, thermal resistance of the selected package, and operating environment (power supply voltage and ambient termperature).

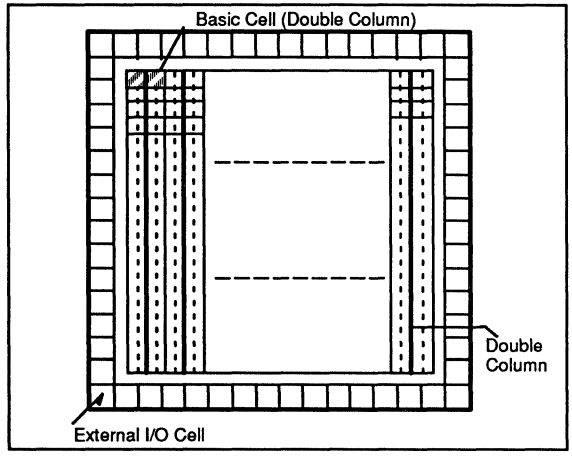
[2]Values for post-layout simulation, with Tj ≤ 70°C (Tj: Estimated Junction Temperature.) 0.35 and 1.70 are used for pre-layout simulation.

[3]Values for post-layout simulation with Tj ≤ 60°C. 0.35 and 1.65 are used for pre-layout simulation.

CHIP STRUCTURE

CHIP LAYOUT

On the CG21 gate array chip, the basic cells are configured in a matrix arranged in double parallel columns with no wiring channel between the double columns. External I/O cells are located around the basic cell matrix. Interconnection wires go over and across the columns of basic cells.

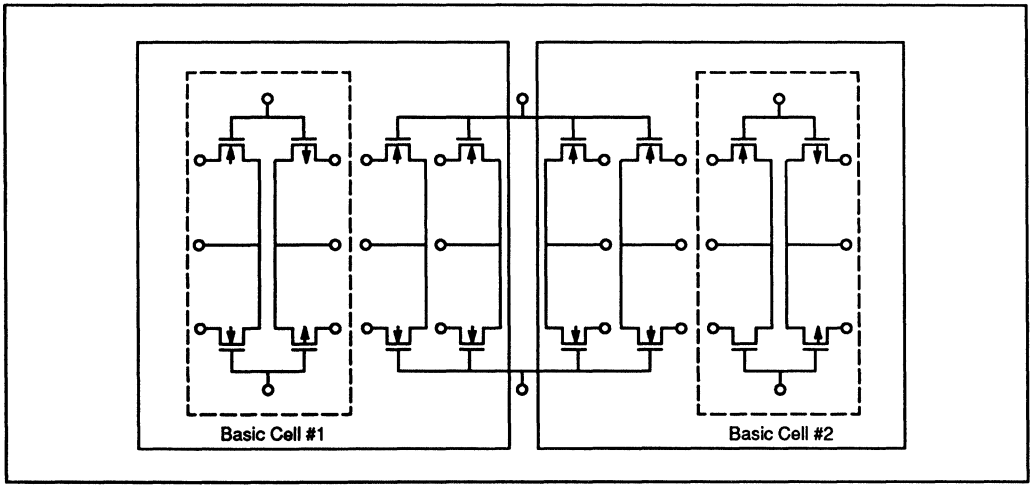


The structure of each device type is as follows:

CG21103	48 rows x 213 columns	= 10,224 BC
CG21153	58 rows x 267 columns	= 15,486 BC
CG21203	68 rows x 307 columns	= 20,876 BC
CG21303	84 rows x 375 columns	= 31,500 BC
CG21403	96 rows x 429 columns	= 41,184 BC
CG21503	108 rows x 483 columns	= 52,164 BC
CG21753	130 rows x 578 columns	= 75,140 BC
CG21104	152 rows x 672 columns	= 102,144 BC

CELL STRUCTURE

The basic cell is the structural element of the CG21 gate arrays. One basic cell consists of two pairs of P-channel and N-channel transistors and four small N-channel transistors. One basic cell can form a 2-input gate, 1 bit for RAM or 4 bits for ROM.



Package Options

Package Name	Package Material	DEVICE NAME								Number of V_{DD}*	Number of V_{SS}*
		CG21103 (10K)	CG21153 (15K)	CG21203 (20K)	CG21303 (30K)	CG21403 (40K)	CG21503 (50K)	CG21703 (75K)	CG21104 (100K)		
PGA-64	Ceramic	●	●	●	—	—	—	—	—	2 (2)	4 (2)
PGA-88	Ceramic	●	●	●	—	—	—	—	—	4 (4)	6 (4)
PGA-135	Ceramic	●	●	●	●	●	●	●	●	8	12
PGA-179	Ceramic	—	—	●	●	●	●	●	●	8	16
PGA-208	Ceramic	—	—	—	●	●	●	●	●	12	18
PGA-256	Ceramic	—	—	—	—	●	●	●	●	16	20
PGA-299	Ceramic	—	—	—	—	—	○	○	○	21	21
PGA-321	Ceramic	—	—	—	—	—	—	○	○	20	32
PGA-361	Ceramic	—	—	—	—	—	—	○	○	24	36
PGA-401	Ceramic	—	—	—	—	—	—	—	○	28	40
QFP-64	Plastic	●	●	●	—	—	—	—	—	2 (2)	4 (2)
QFP-80	Plastic	●	●	●	—	—	—	—	—	2 (2)	6 (4)
QFP-100	Plastic	●	●	●	—	—	—	—	—	4 (4)	8 (4)
QFP-120	Plastic	●	●	●	●	●	—	—	—	6 (4)	12 (8)
QFP-160	Plastic	—	●	●	●	●	—	—	—	8 (6)	14 (12)
QFP-196	Plastic	—	—		—	—	○	○	●	10	18
QFP-232	Plastic	—	—		—	—	—	○	●	14	20
QFP-176	Plastic	—	—	—	—	○	○	○		8	16
QFP-208	Plastic	—	—	—	—	○	○	○	○	12	18
QFP-256	Plastic	—	—	—	—	—	—	—	○	16	20
PLCC-68	Plastic	●	●	●	—	—	—	—	—	2 (2)	4 (2)
PLCC-84	Plastic	●	●	●	—	—	—	—	—	4 (2)	6 (4)
SDIP-64	Plastic	●	●	●	—	—	—	—	—	2 (2)	4 (2)

Notes: ● = Available
○ = Under Development
— = Not Available

*The values in parentheses show the number of V_{DD} and V_{SS} pins provided in the alternate pin assignment (U-type) packages, which have fewer V_{DD}/V_{SS} pins than in normally configured packages.

Package Descriptions

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
SDIP–64	Plastic	None	70 mil Lead Pitch	None	CG21103* CG21153* CG21203*	80 80 85	50 55 60
PLCC–68	Plastic	None	70 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	50 55 60	35 40 40
PLCC–84	Plastic	None	30 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	50 50 55	35 35 40
QFP–64	Plastic	None	100 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP–80	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP–100	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP–120	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	CG21303 CG21403 CG21503 CG21103* CG21153* CG21203*	65 70	40 50
QFP–160	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	CG21303 CG21403 CG21503 CG21153 CG21253	59 70	39 50
QFP–196**	Plastic	None	TBD Gull-wing	None	CG21503 CG21753 CG21104	TBD	TBD
QFP–232**	Plastic	None	TBD Gull-wing	None	CG21753 CG21104	TBD	TBD
QFP–176**	Plastic	None	TBD Gull-wing	None	CG21403 CG21503 CG21753	TBD	TBD
QFP–208**	Plastic	None	TBD Gull-wing	None	CG21403 CG21503 CG21753 CG21104	TBD	TBD
QFP–256**	Plastic	None	TBD Gull–wing	None	CG21104	TBD	TBD

Continued on next page

* planned device
**package under development

Package Descriptions (Continued)

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
PGA–64	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21103* CG21153* CG21203*	40	20
PGA–88	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21103* CG21153* CG21203* CG21303	40	20
PGA–135	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	All CG21	30	15
PGA–179	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21203* CG21303 CG21403 CG21503 CG21753 CG21104	30 25	15 13
PGA–208	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21303 CG21403 CG21503 CG21753 CG21104	23	12
PGA–256	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21403 CG21503 CG21753 CG21104	19	9
PGA–299	Ceramic	Down	100 mil Pin Pitch Through hole	Yes	CG21503 CG21753 CG21104	19	9
PGA–321	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21753 CG21104	22-24	11-13
PGA–361	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21753 CG21104	22-24	11-13
PGA–401	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21104	22-24	11-13

FUNCTIONAL INDEX OF UNIT CELL LIBRARY

Note: The load unit (lu) is a normalized loading unit of capacitance representing the input load of an inverter without metal interconnection.

Inverter and Buffer Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity
V1N	Inverter	1	18	Neg
V2B	Power Inverter	1	36	Neg
B1N	True Buffer	1	18	Pos
BD3	True Delay Buffer (> 5 ns)	5	18	Pos
BD4	Delay Cell (> 4 ns)	4	6	Pos
BD5	Delay Cell (>10 ns)	9	18	Pos
BD6	Delay Cell (>22 ns)	17	18	Pos

Clock Buffer Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity
K1B	True Clock Buffer	2	36	Pos
K2B	Power Clock Buffer	3	55	Pos
K3B	Gated Clock (AND) Buffer	2	36	Pos
K4B	Gated Clock (OR) Buffer	2	36	Pos
K5B	Gated Clock (NAND) Buffer	3	36	Neg
KAB	Block Clock (OR) Buffer	3	55	Pos
KBB	Block Clock (OR x 10) Buffer	30	55	Pos
KDB	Block Clock (OR x 10) Buffer	32	55	Pos
KEB	Block Clock Buffer	23	55	Pos
V1L	Inverting Clock Buffer	2	55	Neg

NAND Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	
N2N	2-input NAND	1	18	
N2B	Power 2-input NAND	3	36	
N2K	Fast Power 2-input NAND	2	36	
N3N	3-input NAND	2	14	
N3B	Power 3-input NAND	3	36	
N4N	4-input NAND	2	10	
N4B	Power 4-input NAND	4	36	
N6B	Power 6-input NAND	5	36	
N8B	Power 8-input NAND	6	36	
N9B	Power 9-input NAND	8	36	
NCB	Power 12-input NAND	10	36	
NGB	Power 16-input NAND	11	36	

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

NOR Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	
R2N	2-input NOR	1	14	
R2B	Power 2-input NOR	3	36	
R2K	Power 2-input NOR	2	36	
R3N	3-input NOR	2	10	
R3B	Power 3-input NOR	3	36	
R4N	4-input NOR	2	6	
R4B	Power 4-input NOR	4	36	
R6B	Power 6-input NOR	5	36	
R8B	Power 8-input NOR	6	36	
R9B	Power 9-input NOR	8	36	
RCB	Power 12-input NOR	10	36	
RGB	Power 16-input NOR	11	36	

AND Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	
N2P	Power 2-input AND	2	36	
N3P	Power 3-input AND	3	36	
N4P	Power 4-input AND	3	36	
N8P	Power 8-input AND	6	36	

OR Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	
R2P	Power 2-input OR	2	36	
R3P	Power 3-input OR	3	36	
R4P	Power 4-input OR	3	36	
R8P	Power 8-input OR	6	36	

Exclusive NOR/OR Family (EXOR/EXNOR)

Unit Cell Name	Description	Basic Cells	Drive (lu)	Polarity
X1N	Exclusive NOR	3	18	Neg
X1B	Power Exclusive NOR	4	36	Neg
X2N	Exclusive OR	3	14	Pos
X2B	Power Exclusive OR	4	36	Neg
X3N	3-input Exclusive NOR	5	14	Neg
X3B	Power 3-input Exclusive NOR	6	36	Neg
X4N	3-input Exclusive OR	5	14	Pos
X4B	Power 3-input Exclusive OR	6	36	Pos

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

AND–OR–Inverter Family (AOI)

Unit Cell Name	Description	Basic Cells	Drive (Iu)
D23	2-wide 2-AND 3-input AOI	2	14
D14	2-wide 3-AND 4-input AOI	2	14
D24	2-wide 2-AND 4-input AOI	2	14
D34	3-wide 2-AND 4-input AOI	2	10
D36	3-wide 2-AND 6-input AOI	3	10
D44	2-wide 2-OR 2-AND 4-input AOI	2	10

Note: AND-OR-Inverter unit cells are useful in implementing sum-of-products (SOP) expressions.

OR–AND–Inverter Family (OAI)

Unit Cell Name	Description	Basic Cells	Drive (Iu)
G23	2-wide 2-OR 3-input OAI	2	18
G14	2-wide 3-OR 4-input OAI	2	10
G24	2-wide 2-OR 4-input OAI	2	10
G34	3-wide 2-OR 4-input OAI	2	10
G44	2-wide 2-AND 2-OR 4-input OAI	2	14

Note: OR-AND-Inverter unit cells are useful in implementing product-of-sums (POS) expressions.

Multiplexer Family

Unit Cell Name	Type	Description	Basic Cells	Drive (Iu)	Function
T24*	4:1	Power 4, 2 ANDs into 4 NOR Multiplexer	6	36	SOP
T26*	6:1	Power 6, 2 ANDs into 6 NOR Multiplexer	10	36	SOP
T28*	8:1	Power 8, 2 ANDs into 8 NOR Multiplexer	11	36	SOP
T32	2:1	Power 2, 3 ANDs into 2 NOR Multiplexer	5	36	SOP
T33*	3:1	Power 3, 3 ANDs into 3 NOR Multiplexer	7	36	SOP
T34*	4:1	Power 4, 3 ANDs into 4 NOR Multiplexer	9	36	SOP
T42	2:1	Power 2, 4 ANDs into 2 NOR Multiplexer	6	36	SOP
T43	3:1	Power 3, 4 ANDs into 3 NOR Multiplexer	10	36	SOP
T44	4:1	Power 4, 4 ANDs into 4 NOR Multiplexer	11	36	SOP
T54	4:1	Power 2, 2–3–4 ANDs into 4 NOR Multiplexer	10	36	SOP
U24*	4:1	Power 4, 2 OR into 4 NAND Multiplexer	6	36	POS
U26*	6:1	Power 6, 2 OR into 6 NAND Multiplexer	9	36	POS
U28*	8:1	Power 8, 2 OR into 8 NAND Multiplexer	11	36	POS
U32	2:1	Power 2, 3 OR into 2 NAND Multiplexer	5	36	POS
U33*	3:1	Power 3, 3 OR into 3 NAND Multiplexer	7	36	POS
U34*	4:1	Power 4, 3 OR into 4 NAND Multiplexer	9	36	POS
U42	2:1	Power 2, 4 OR into 2 NAND Multiplexer	6	36	POS
U43	3:1	Power 3, 4 OR into 3 NAND Multiplexer	9	36	POS
U44	4:1	Power 4, 4 OR into 4 NAND Multiplexer	11	36	POS

* Convenient for typical multiplexer applications

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Data Selectors/Multiplexers

Unit Cell Name	Type	Description	Basic Cells	Drive (lu)	Selects	Output	Bit Width
P24*	2:1	Data Selector	12	36	S, XS	Q	4
T2E	2:1	Dual Selector	5	18	S	XQ	2
T2F	2:1	Selector	8	18	S	XQ	4
T2B*	2:1	Selector	2	18	S, XS	XQ	1
T2C*	2:1	Selector	4	18	S, XS	XQ	2
T2D*	2:1	Selector	2	14	S, XS	XQ	1
T5A*	4:1	Selector	5	9	S, XS	XQ	1
V3A*	1:2	Selector	2	14	S, XS	XQ	1
V3B*	1:2	Dual Selector	4	14	S, XS	XQ	2

* These are transmission gate devices whose outputs can be tied because they can be inhibited with true/inverted selects.

Decoders

Unit Cell Name	Type	Description	Basic Cells	Drive (lu)	Active Level Outputs	Enable	
DE2	2:4	Decoder	5	18	Low	—	
DE3	3:8	Decoder	15	14	Low	—	
DE4	2:4	Decoder	8	14	Low	Low	
DE6	3:8	Decoder	30	18	Low	1 High 2 Low	

Internal Bus Unit Cells

Unit Cell Name	Type Description	Basic Cells	Drive (lu)	Bus Size	Enable	
B11	1-bit Bus Driver	5	36	1	Low	
B21	2-bit Bus Driver	9	36	2	Low	
B41	4-bit Bus Driver	17	36	4	Low	
B81	8-bit Bus Driver	33	36	8	Low	
B12	1-bit Block Bus Driver	7	72	1	Low	
B22	2-bit Block Bus Driver	13	72	2	Low	
B42	4-bit Block Bus Driver	25	72	4	Low	

Data Latch Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Enable	Bits	Output	Clear
YL2	Data Latch with TM	5	36	High	1	Q	—
YL4	Data Latch with TM	14	36	High	4	Q	—
LTK	Data Latch	4	18	Low	1	Q, XQ	Async
LTL	Data Latch with Clear	5	18	Low	1	Q, XQ	Async
LTM	Data Latch with Clear	16	18	Low	4	Q, XQ	—
LT1	S-R Latch with Clear	4	18	Low	1	Q, XQ	Async
LT4	Data Latch	14	18	Low	4	Q, XQ	—

Note: Y-type latches incorporate inhibit inputs and transparent mode (TM) to facilitate scan implementation.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Scan Flip-flop Family (Positive-Edge Triggered)

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Output	Clear	Preset	Clock Inhibit
SDH	Scan D Flip-flop with 2:1 Multiplexed inputs	14	36	1	Q, XQ	Async	—	Yes
SDJ	Scan D Flip-flop with 4:1 Multiplexed inputs	15	36	1	Q, XQ	Async	—	Yes
SDK	Scan D Flip-flop with 3:1 Multiplexed inputs	16	36	1	Q, XQ	Async	—	Yes
SJH	Scan J–K Flip-flop	16	36	1	Q, XQ	Async	—	Yes
SDD	Scan DFlip-flop with 2:1 Multiplexed inputs	16	36	1	Q, XQ	Async	Async	Yes
SDA	Scan 1-input D Flip-flop	12	36	1	Q, XQ	—	—	Yes
SDB	Scan 1-input D Flip-flop	42	36	4	Q, XQ	—	—	Yes
SHA	Scan 1-input D Flip-flop	68	18	8	Q, XQ	—	—	Yes
SHB	Scan 1-input D Flip-flop	62	18	8	Q	—	—	Yes
SHC	Scan 1-input D Flip-flop	62	18	8	XQ	—	—	Yes
SHJ	Scan D Flip-flop with 2:1 Multiplexed inputs	78	18	8	Q, XQ	—	—	Yes
SHK	Scan D Flip-flop with 3:1 Multiplexed inputs	88	18	8	Q, XQ	—	—	Yes
SFDM	Scan 1-input D Flip-flop	10	18	1	Q, XQ, SO	—	—	Yes
SFDO	Scan 1-input D Flip-flop	11	18	1	Q, XQ, SO	Yes	—	Yes
SFDP	Scan 1-input D Flip-flop	12	18	1	Q, XQ, SO	Yes	Yes	Yes
SFDR	Scan 4-input D Flip-flop	36	18	4	Q, XQ, SO	Yes	—	Yes
SFDS	Scan 4-input D Flip-flop	31	18	4	Q, XQ, SO	—	—	Yes
SFJD	Scan J-K D Flip-flop	14	18	1	Q, XQ, SO	—	—	Yes

Non Scan Flip-flop Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs	Clear	Preset	Clock Edge
FDN	Non-Scan D Flip-flop with Set	7	18	1	Q, XQ	—	Async	Pos
FDM	Non-Scan D F	6	18	1	Q, XQ	—	—	Pos
FDO	Non-Scan D Flip-flop with Reset	7	18	1	Q, XQ	Async	—	Pos
FDP	Non-Scan D Flip-flop with Set and Reset	8	18	1	Q, XQ	Async	Async	Pos
FDQ	Non-Scan D Flip-flop	21	18	4	Q	—	—	Neg
FDR	Non-Scan D Flip-flop	26	18	4	Q	Async	—	Pos
FDS	Non-Scan D Flip-flop	20	18	4	Q	—	—	Pos
FD2	Non-Scan Power D Flip-flop	7	36	1	Q, XQ	—	—	Neg
FD3	Non-Scan Power D Flip-flop	8	36	1	Q, XQ	—	Async	Neg
FD4	Non-Scan Power D Flip-flop	9	36	1	Q, XQ	Async	Async	Neg
FD5	Non-Scan Power D Flip-flop	8	36	1	Q, XQ	Async	—	Neg
FJD	Non-ScanPower J-K Flip-flop	12	36	1	Q, XQ	Async	—	Pos

Note: Synchronous flip-flops may be constructed by adding a simple AND gate (such as N2P) to the input of a flip-flop to create a synchronous clear.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Scan Counter Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs[1]	Load	Clear	Enable	Carry In	Up/ Down
SC7[2]	Scan Synchronous Binary Counter with Parallel Load	62	36	4	Q, XQ, CO (S)	Sync	—	Low	High	Up
SC8[2]	Scan Synchronous Binary Counter with Parallel Load	66	36	4	Q, XQ, CO (S)	Sync	—	High	Low	Down
SC43[2]	Scan synchronous Binary Counter	59	18	4	Q, CO	Sync	Async	High	High	Up
SC47[2]	Scan synchronous Binary Counter	78	18	4	Q, CO	Async	—	Low	Low	UpDown

Non-Scan Counter Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bits	Outputs[1]	Load	Clear	Enable	Carry In	Up/ Down
C11[3]	Non-Scan Flip-flop for Counter	11	18	—	Q, XQ	—	—	—	—	—
C41	Non-Scan Binary Asynchronous Counter	24	18	4	Q, (A)	—	Async	—	—	Up
C42	Non-Scan Binary Synchronous Counter	32	18	4	Q	—	Async	—	—	Up
C43	Non-Scan Binary Synchronous Counter	48	18	4	Q, CO(S)	Sync	Async	High	High	Up
C45	Non-Scan Binary Synchronous Counter	48	18	4	Q, CO	Sync	Sync	High	High	Up
C47	Non-Scan Binary Synchronous Counter	68	18	4	Q, CO	Async	—	Low	Low	Up/Down

Notes:
1. (S), (A) indicate the counter is (S)ynchronous or (A)synchronous.
2. Scan counters include clock inhibit and high drive (C_{DR} = 36 lu). For non-Scan counters C_{DR} = 18 lu
3. C11 may by used for purposes other than counters.

Shift Register Family

Unit Cell Name	Description	Basic Cells	Drive (lu)	Bit Width	Load	Outputs	Clock Polarity
FS1	Serial-in Parallel-out Shift Register	18	16	4	Serial-In only	Q-Parallel	Neg
FS2	Shift Register with Synchronous Load	30	16	4	Sync-High	Q-Parallel	Neg
FS3	Shift Register with Asynchronous Load	34	18	4	Async-Low	Q-Parallel	Pos
SR1	Serial-in Parallel-out Shift Register with Scan	36	36	4	Serial-In only	Q-Parallel	Pos

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Datapath Operators (Adder, ALU, Parity)						
Unit Cell Name	**Description**	**Basic Cells**	**Drive (Iu)**	**Bit Width**	**Outputs**	**Carry In**
MC4	Magnitude Comparator	42	18 (=) 10(<>)	4	A>B, A=B, A<B	A>B,A=B,ALB
A1A	1-bit Half Adder	5	36	1	S, CO	—
A1N	1-bit Full Adder	8	18	1	S, CO	CI
A2N	2-bit Full Adder	16	14	2	S, CO	CI
A4H	4-bit Binary Full Adder w/Fast Carry	18(CO) 14(S)	48	4	S, CO	CI
PE5	Even Parity Generator/Checker	12	36	5	EVEN, $\overline{\text{ODD}}$	—
PO5	Odd Parity Generator/Checker	12	36	5	ODD, $\overline{\text{EVEN}}$	—
PE8	Even Parity Generator/Checker	18	18	8	EVEN, $\overline{\text{ODD}}$	—
PO8	Odd Parity Generator/Checker	18	18	8	ODD, $\overline{\text{EVEN}}$	—
PE9	Even Parity Generator/Checker	22	18	9	EVEN, $\overline{\text{ODD}}$	—
PO9	Odd Parity Generator/Checker	22	18	9	ODD, $\overline{\text{EVEN}}$	—
Miscellaneous Cells						
Unit Cell Name	**Description**	**Basic Cells**			**Function**	
Z00	0 Clip	0			Tie to Vss	
Z01	1 Clip	0			Tie to VDD	

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Input Buffer Family

Unit Cell Name	Description	Basic Cells	Drive (Iu)	Logic Level	Type	Input/ Output Polarity
I1B	Input Buffer	5	36	TTL	Signal	Invert
I1BU	I1B with Pull-up Resistance	5	36	TTL	Signal	Invert
I1BD	I1B with Pull-down Resistance	5	36	TTL	Signal	Invert
I2B	Input Buffer	4	36	TTL	Signal	True
I2BU	I2B with Pull-up Resistance	4	36	TTL	Signal	True
I2BD	I2B with Pull-down Resistance	4	36	TTL	Signal	True
IKB	Clock Input Buffer	4	72	TTL	Clock	Invert
IKBU	Ikb With Pull-up Resistance	4	72	TTL	Clock	Invert
IKBD	IKB with Pull-down Resistance	4	72	TTL	Clock	Invert
ILB	Clock Input Buffer	6	72	TTL	Clock	True
ILBU	ILB with Pull-up Resistance	6	72	TTL	Clock	True
ILBD	ILB with Pull-down Resistance	6	72	TTL	Clock	True
I1C	CMOS Interface Input Buffer	5	36	CMOS	Signal	Invert
I1CU	I1C with Pull-up Resistance	5	36	CMOS	Signal	Invert
I1CD	I1C with Pull-down Resistance	5	36	CMOS	Signal	Invert
I2C	CMOS Interface Input Buffer	4	36	CMOS	Signal	True
I2CU	I2C with Pull-up Resistance	4	36	CMOS	Signal	True
I2CD	I2C with Pull-down Resistance	4	36	CMOS	Signal	True
I1S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	Invert
I1SU	I1S with Pull-up Resistance	8	18	CMOS	Schmitt	Invert
I1SD	I1S with Pull-down Resistance	8	18	CMOS	Schmitt	Invert
I2S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	True
I2SU	I2S with Pull-up Resistance	8	18	CMOS	Schmitt	True
I2SD	I2S with Pull-down Resistance	8	18	CMOS	Schmitt	True
I1R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	Invert
I1RU	I1R with Pull-up Resistance	8	18	TTL	Schmitt	Invert
I1RD	I1R with Pull-down Resistance	8	18	TTL	Schmitt	Invert
I2R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	True
I2RU	I2R With Pull-up Resistance	8	18	TTL	Schmitt	True
I2RD	I2R with Pull-down Resistance	8	18	TTL	Schmitt	True
IKC	Clock Input Buffer	4	200	CMOS	Clock	Invert
IKCU	IKC with Pull-up Resistance	4	200	CMOS	Clock	Invert
IKCD	IKC with Pull-down Resistance	4	200	CMOS	Clock	Invert
ILC	Clock Input Buffer	6	200	CMOS	Clock	True
ILCU	IKC with Pull-up Resistance	6	200	CMOS	Clock	True
ILCD	IKC with Pull-down Resistance	6	200	CMOS	Clock	True

Note: A "U" suffixed to the name of an input buffer indicates pull-up resistance of 50KΩ (typical) and a "D" indicates a pull-down resistance of the equivalent value.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

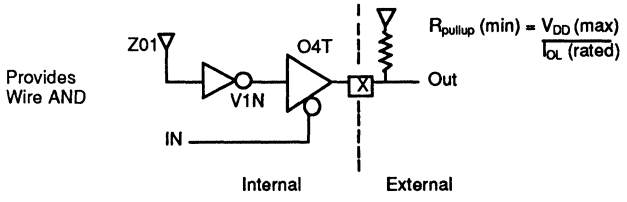
Output Buffer Family

Unit Cell Name	Description	Basic Cells	Drive (I_{OL})	Logic[2] Level	Type	Edge Rate Control	Input/ Output Polarity
O1B	Output Buffer	3	3.2 mA	TTL/CMOS	Standard	No	Invert
O1L	Power Output Buffer	3	12 mA	TTL/CMOS	Standard	No	Invert
O1S	Power Output Buffer	5	12 mA	TTL/CMOS	Standard	Yes	Invert
O2B	Output Buffer	2	3.2 mA	TTL/CMOS	Standard	No	True
O2L	Power Output Buffer	2	12 mA	TTL/CMOS	Standard	No	True
O2S	Power Output Buffer	4	12 mA	TTL/CMOS	Standard	Yes	True
O4[1]	3-state Output Buffer	4	3.2 mA	TTL/CMOS	3-state	No	True
O4W[1]	Power 3-state Output Buffer	4	12 mA	TTL/CMOS	3-state	No	True
O4S[1]	Power 3-state Output Buffer	5	12 mA	TTL/CMOS	3-state	Yes	True
O1R	Output Buffer	5	3.2 mA	TTL/CMOS	Standard	Yes	Invert
O2R	Output Buffer	4	3.2 mA	TTL/CMOS	Standard	Yes	True
O4R[1]	3-state Output Buffer	5	3.2 mA	TTL/CMOS	3-state	Yes	True
O2BF	Output Buffer	2	8 mA	TTL/CMOS	Standard	No	True
O2RF	Output Buffer	4	8 mA	TTL/CMOS	Standard	Yes	True
O4RF	3-state Output Buffer	5	8 mA	TTL/CMOS	3-state	Yes	True
O4TF	3-state Output Buffer	4	8 mA	TTL/CMOS	3-state	No	True
O2S2	Output Buffer	3	24 mA	TTL/CMOS	Standard	Yes	True
O4S2	3-state Output Buffer	4	24 mA	TTL/CMOS	3-state	Yes	True

Notes: 1.While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs.

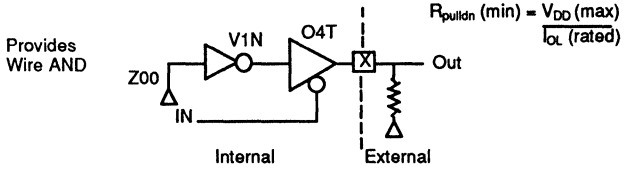
2.Totem pole outputs, such as these buffers have, can drive both TTL and CMOS levels. Voltage margins depend on actual source or sink current (see DC specifications).

Example Of Open Drain Output



In	X	Out
0	L	L
1	Z	H

Example Of Open Source Output



In	X	Out
0	H	H
1	Z	L

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectional I/O Buffers (Buses)

Unit Cell Name	Description	Basic Cells	Drive (I_{OL})	Logic Level	Edge Rate Control	Input/ Output Polarity
H6T	3-state Output and Input Buffer	8	3.2 mA	TTL	No	True
H6TU	H6T with Pull-up Resistance	8	3.2 mA	TTL	No	True
H6TD	H6T with Pull-down Resistance	8	3.2 mA	TTL	No	True
H6W	Power 3-state Output and Input Buffer	8	12 mA	TTL	No	True
H6WU	H6W with Pull-up Resistance	8	12 mA	TTL	No	True
H6WD	H6W with Pull-down Resistance	8	12 mA	TTL	No	True
H6C	3-state Output and CMOS Interface Input Buffer	8	3.2 mA	CMOS	No	True
H6CU	H6C with Pull-up Resistance	8	3.2 mA	CMOS	No	True
H6CD	H6C with Pull-down Resistance	8	3.2 mA	CMOS	No	True
H6E	Power 3-state Output and CMOS Interface Input Buffer	8	12 mA	CMOS	No	True
H6EU	H6E with Pull-up Resistance	8	12 mA	CMOS	No	True
H6ED	H6E with Pull-down Resistance	8	12 mA	CMOS	No	True
H6S	3-state Output and Schmitt Trigger Input Buffer	12	3.2 mA	CMOS	No	True
H6SU	H6S with Pull-up Resistance	12	3.2 mA	CMOS	No	True
H6SD	H6S with Pull-down Resistance	12	3.2 mA	CMOS	No	True
H6R	3-state Output and Schmitt Trigger Input Buffer	12	3.2 mA	TTL	No	True
H6RU	H6R with Pull-up Resistance	12	3.2 mA	TTL	No	True
H6RD	H6R with Pull-down Resistance	12	3.2 mA	TTL	No	True
H8T	3-state Output and Input Buffer	9	3.2 mA	TTL	Yes	True
H8TU	H8T with Pull-up Resistance	9	3.2 mA	TTL	Yes	True
H8TD	H8T with Pull-down Resistance	9	3.2 mA	TTL	Yes	True
H8W	Power 3-state Output and Input Buffer	9	12 mA	TTL	Yes	True
H8WU	H8W with Pull-up Resistance	9	12 mA	TTL	Yes	True
H8WD	H8W with Pull-down Resistance	9	12 mA	TTL	Yes	True
H8C	3-state Output Buffer and CMOS Interface Input Buffer	9	3.2 mA	CMOS	Yes	True
H8CU	H8C with Pull-up Resistance	9	3.2 mA	CMOS	Yes	True
H8CD	H8C with Pull-down Resistance	9	3.2 mA	CMOS	Yes	True

Note: A "U" suffixed tol the name of a bidirectional buffer indicates a pull-up resistance of 50Ω (typical) and a "D" indicates a pull-down resistance of the equivalent value.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectional I/O Buffers (Buses) continued

Unit Cell Name	Description	Basic Cells	Drive (I_{OL})	Input Logic Level	Edge Rate Control	Input/ Output Polarity
H8E	Power 3-state Output Buffer and Interface Input Buffer	9	12 mA	CMOS	Yes	True
H8EU	H8E with Pull-up Resistance	9	12 mA	CMOS	Yes	True
H8ED	H8E with Pull-down Resistance	9	12 mA	CMOS	Yes	True
H8S	3-state Output and Schmitt Trigger Input Buffer	13	3.2 mA	CMOS	Yes	True
H8SU	H8S with Pull-up Resistance	13	3.2 mA	CMOS	Yes	True
H8SD	H8S with Pull-down Resistance	13	3.2 mA	CMOS	Yes	True
H8R	3-state Output and Schmitt Trigger Input Buffer	13	3.2 mA	TTL	Yes	True
H8RU	H8R with Pull-up Resistance	13	3.2 mA	TTL	Yes	True
H8RD	H8R with Pull-down Resistance	13	3.2 mA	TTL	Yes	True
H6TF	3-state Output and Schmitt Trigger Input Buffer	8	8 mA	TTL	No	True
H6TFU	H6TF with Pull-up Resistance	8	8 mA	TTL	No	True
H6TFD	H6TF with Pull-down Resistance	8	8 mA	TTL	No	True
H6CF	3-state Output and Input Buffer	8	8 mA	CMOS	No	True
H6CFU	H6CF with Pull-up Resistance	8	8 mA	CMOS	No	True
H6CFD	H6CF with Pull-down Resistance	8	8 mA	CMOS	No	True
H8TF	3-state Output and Input Buffer	9	8 mA	TTL	Yes	True
H8TFU	H8TF with Pull-up Resistance	9	8 mA	TTL	Yes	True
H8TFD	H8TF with Pull-down Resistance	9	8 mA	TTL	Yes	True
H8CF	3-state Output and Input Buffer	9	8 mA	CMOS	Yes	True
H8CFU	H8CF with Pull-up Resistance	9	8 mA	CMOS	Yes	True
H8CFD	H8CF with Pull-down Resistance	9	8 mA	CMOS	Yes	True

Note: While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs, which includes all bidirectional buffers.

Chapter 2 – Steps Toward Design

Contents of This Chapter

2.1 Introduction

This section of the data book takes a look at the issues that must be considered before a design is ready to be entered on a computer-aided engineering (CAE) workstation.

2.2 Choosing Fujitsu as Your ASIC Manufacturer

The first step in implementing a given ASIC design is to choose the manufacturer that offers semi–conductor processes capable of actualizing the performance requirements of the IC. The manufacturer should also offer consistent and easily accessible customer support, timely transfer of the design into silicon, and a highly reliable end product.

The data sheet and supplementary information in Chapter 1 enable customers to determine whether their requirements fall within the broad range of Fujitsu's technical capability.

The second step is to discuss the design requirements with one of Fujitsu's Field Applications Engineers at either a Regional Sales Office or a Technical Resource Center. Regional Sales Office and Technical Resource Center addresses and telephone numbers are listed at the back of this volume. Fujitsu's Field Applications Engineers work with each customer to determine which technology would be most suitable for a given design, taking into account the factors outlined in more detail below.

Fujitsu's highly developed software tools, high-capacity manufacturing facilities (the largest in the world) and long history of excellence in the field (Fujitsu has been producing custom gate arrays commercially since 1974) enable customers to turn designs into highly reliable products in a cost-effective time frame.

2.3 Choosing A Device

Speed is usually the deciding factor in choosing the technology for a design, but sometimes special requirements such as package availability, on-chip memory (available in the AU and CG21 technologies), or the necessity for battery power (a feature of the AVL technology) influence the final decision.

Usually the device type is a requirement of the design and is chosen before the package size is determined. The size of the package will depend on array size, partitioning, the number of power and ground pins required by the SSOs (simultaneously switching outputs) used in the design, and the high power drive buffers and clock inputs used in the design.

To determine the most suitable device within a given technology, the designer must determine the gate count and pinout requirements from the schematic diagram of the design to be implemented.

The functions in the schematic or logic block diagram may be described using standard logic functions, programmable logic, or Fujitsu's Unit Cell Library.

Gate counts are calculated in terms of how many basic cells make up each component function (unit cell). This number is given for each unit cell in the unit cell library for each technology. By adding up the number of basic cells used in each logic element in a design, a designer can arrive at a good first estimate of the design complexity.

In the double-column channelless array technologies (AU and CG21), unit cells may take up parts of two adjacent columns. It is recommended that no more than 50 percent of the basic cells in a channelless array be used; 75 percent may be used if memory is included on the chip. Respecting this limitation facilitates fully automated layout.

2.4 Choosing a Package

Before the final choice of an array can be made, however, the choice of a package must be considered. The intended use of the IC generally determines the type of package used: packaging issues are discussed in detail in the application note "Choosing the Best Package for Your ASIC Design" included in Chapter 7 of Section 1 of this data book. The types of packages available for Fujitsu's CMOS channelless arrays are shown in the data sheet in Section 1 and in Appendix D of the AU Unit Cell Library (Section 2) and Appendix D of the CG21 Unit Cell Library (Section 3).

The size of the package chosen is regulated by the number of inputs and outputs required, the number of V_{SS} and V_{DD} pins required, and the number of simultaneously switching outputs (SSOs) included in the design.

1

Package Size vs. SSOs

The number of SSOs can influence the size of the package chosen because additional ground pins are sometimes required in a design that has more simultaneously switching outputs than is acceptable for a given package type. Simultaneously switching outputs are those that switch from a logic low or a high impedance (Z) to a logic high or from a logic high or Z state to a logic low within 20 nanoseconds of each other.

A general rule is to use one ground pin for each group of 10 simultaneously switching low power outputs or for 20 non-simultaneous outputs. Chapter 4 of Section 1 of this book and the Package Pin Assignments section of the Design Manuals cover pin requirement issues in more detail.

Although the V_{SS} and V_{DD} pins are preassigned in each package and cannot be changed, alternate packages are available offering varying numbers of power and ground pins.

2.5 Technical Review

When the CMOS technology, the device, and the package have been decided upon, the customer and Fujitsu's Field Applications Engineer hold a technical review to ensure that all the information necessary to implement the design is available and to allow Fujitsu to derive a schedule and price.

2.6 Design Interface Options

The next step is to determine which computer-aided engineering (CAE) workstation will be used to enter the design. The desired result of entering the design on a CAE workstation is the generation of a successful net list or Fujitsu Logic Description Language (FLDL) file and a list of test vectors or Fujitsu Test Description Language (FTDL) file. These two files (which may be generated on any of several different CAE workstation systems) enable Fujitsu's host mainframe to perform automated layout and rigorous test and simulation of the design.

Four popular dedicated CAE workstation systems (Valid, Mentor, Daisy, and the HP 9000) as well as several hardware-independent CAE packages support Fujitsu's design software. In addition, Fujitsu now offers design support on ViewCAD™, a computer-aided engineering system originated by Fujitsu for ASIC designs.

ViewCAD is written in the C programming language and runs on any UNIX™ platform that supports the X Window System™ (such as the Sun 3 or 4 series of workstations). It includes in one package all of the necessary functions for the design, simulation, and analysis of an ASIC design. ViewCAD makes use of a graphics-oriented interface that allows visual examination of all circuits, circuit test data, and simulation results. Its final product is the logic and test data description files (FLDL and FTDL) that are required by the host mainframe computer to process a design.

Through long experience, Fujitsu has found that by far the most efficient way to achieve a trouble-free end product is for customers to implement the design on a workstation themselves. This can be done:

a. on CAD equipment that the customer is already using (Fujitsu provides cell library information files and the expertise to help write a conversion program to produce the FLDL and FTDL files if necessary)

b. on one of the design systems that specifically support Fujitsu software (Daisy, Mentor, Valid, HP 9000) either at the customer's workplace or in one of the Technical Resource Centers

c. on ViewCAD either on the customer's own Sun equipment or at a Technical Resource Center.

Chapter 3 – Design Procedures

Contents of This Chapter

3.1 Introduction

This section of the data book explains the steps necessary to implement an ASIC design in one of Fujitsu's CMOS technologies using a CAE (computer-aided engineering) workstation. Designs can be implemented with Fujitsu's ViewCAD design software or with one of the CAE systems or software applications that support Fujitsu designs.

3.2 ViewCAD Design Procedures

Fujitsu developed the ViewCAD design software to complement a wide range of customer third party design tools. It includes:

- A schematic capture module utilizing the X Window System
- A logic design rule check module that screens for design violations in the areas of fanout and drive, gate count, I/O requirements, etc.
- A test data or waveform entry module for test vector entry
- An interactive simulation module that replicates the Fujitsu mainframe for both functional and timing simulation
- Conversion modules to define the net list and test vectors in the FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Data Description Language) formats required by Fujitsu's host mainframe.

Figure 3–1 shows the ASIC design flow using ViewCAD. This design flow includes the use of schematic capture and test data generated on other workstations as well as on ViewCAD. The numbers on the left side of Figure 3–1 correspond to the numbers of the paragraphs below that explain the corresponding portion of the figure.

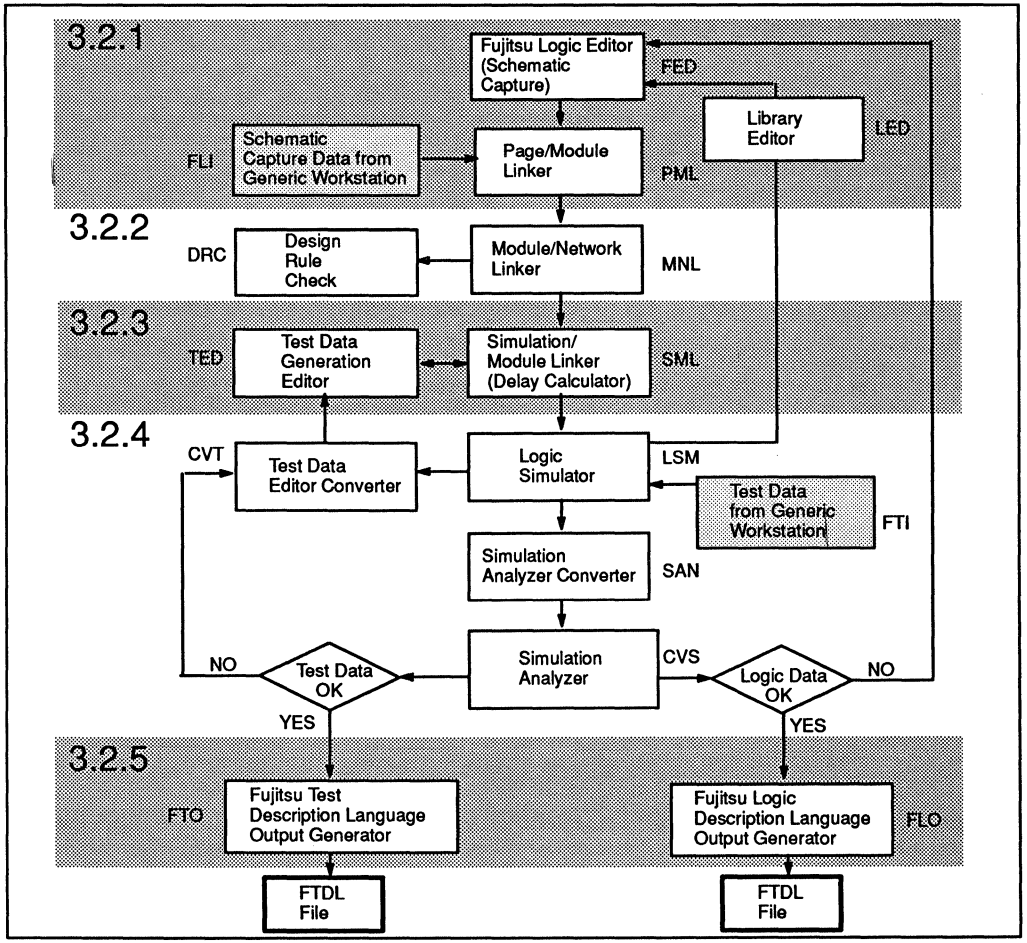


Figure 3–1. ASIC Design Flow with ViewCAD

3.2.1 Schematic Capture

ViewCAD users accomplish logic circuit entry (schematic capture) through the Fujitsu Schematic Editor (FED) module. After running a setup utility requiring the entry of the design name, technology series, and package type, users can insert unit cells and connect them to create circuit diagrams and see a graphic representation of the resulting schematic. The Schematic Editor also provides a basic verification routine. If the schematic has already been entered in another CAE system, it can be converted to ViewCAD-compatible data by the FLDL-to-ViewCAD translator (FLI) module. A Library Editor (LED) module is available to specify design hierarchies, create user macros, and implement blocks in partitioned arrays. ViewCAD allows the user to go back and forth between LED and FED to facilitate the development of complex hierarchical designs.

The designer then uses a Page/Module Linker (PML) module to link pages, ensuring connectivity between the pages of the schematic.

3.2.2 Logic Design Rule Check

DRC, ViewCAD's Design Rule Check module, examines the data files produced by the editor and page linker modules for conformity to the design rules of the CMOS technology in which the design is executed.

Subsequently a Module/Network Linker (MNL) is run on the PML file to expand macros and link the levels of the design hierarchy to prepare the data for the logic simulator.

3.2.3 Circuit Test Data Entry

The designer then provides the Test Data Editor (TED) with test signals for the simulator. Like the schematic capture module, the test data generator displays the data graphically. It allows the user to create and modify signal data and to prepare the data for the simulator module by saving it in a format that the simulator understands. If test data has already been prepared on another CAE system, it can be converted to data usable to the Test Data Editor.

The Simulation Module Linker (SML), which takes the output of the Module/Network Linker and generates the delay estimates for the logic simulator, is run before the logic simulator can be executed.

3.2.4 Simulation and Analysis

The Logic Simulator Module (LSM) reads the data created by SML and combines it with the test information in the TED file to run a simulation of the design.

The Test Data Editor Converter (CVT) then converts the output of the simulation module (LSM) back into a TED file. It provides the path from the simulator back to TED so that output that was previously given an undefined value of "X" can be assigned actual simulated values.

The Simulation Analyzer Converter (CVS) translates the output of the logic simulator (LSM) into an acceptable format for the simulation analyzer.

The Simulation Analyzer Module (SAN) analyzes the output from the simulator to determine whether it performs as intended. SAN allows the user to display the simulation output and manipulate the display to help the user analyze the output.

3.2.5 Data Conversion for Mainframe Interface

The last step in the implementation of an ASIC design on ViewCAD is the generation of the all-important FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Description Language) files.

After any design errors that may have been found by simulation and analysis have been corrected in the schematic capture module, the designer runs the Fujitsu Logic Language Output Generator (FLO) module to convert the schematic data into an FLDL file for use on Fujitsu's host mainframe.

If any errors in test data are discovered during the simulation analysis process, the test data can be sent back to the Test Data Editor Converter Module to be reconverted into a form that the test Data Editor understands (since the errors must be corrected in the Test Data Editor module). After error correction or if no errors are found, the designer sends the test data file to the Fujitsu Test Description Language Output Generator (FTO) module for conversion into an FTDL file for use on the mainframe.

3.3 Generic Workstation Design Procedures

Fujitsu provides ASIC Design Software Kits for designers using some of the popular design tools on generic workstations. The kits offer support for Daisy, Mentor, Valid, and HP9000 and include:

- Fujitsu symbol model libraries for the CAE system's schematic capture module
- A Fujitsu logic design rule check module
- Fujitsu timing model libraries for the system's simulator
- A delay calculator module
- Conversion modules to define the net list and test vectors in the FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Description Language) formats required by host mainframe computer.

In addition, Fujitsu now offers FAME (Fujitsu's ASIC Management Environment), a menu-driven design management program that enables the user to select the technology, the approximate gate count and I/O, pinout, and the package requirements, and to create a design database that is referenced by the other modules to assure correct-by-construction design. FAME includes a test vector module that creates test vectors automatically for complex functions, assists in defining test groupings, cycle times, and strobe settings, and checks created test files against restrictions.

Fujitsu designs are also supported by several high-performance third party CAE tools. These include:

- Verilog-XL™ (Gateway Design Automation) mixed-mode system simulator
- LASAR™ Version 6 (Teradyne) design simulator and test program generator with fault simulation
- HILO® (GenRad) design verification, fault simulation, and test generation tools
- IKOS™ 800 logic validation hardware accelerator
- Synopsys™ Design Compiler™ interactive behavioral/logic synthesizer

Figure 3–2 shows a flowchart of the generic workstation-based design process. Because the function and file names used by each different CAE system may differ, generalized names for each operation are used rather than system-specific names in the following list of steps.

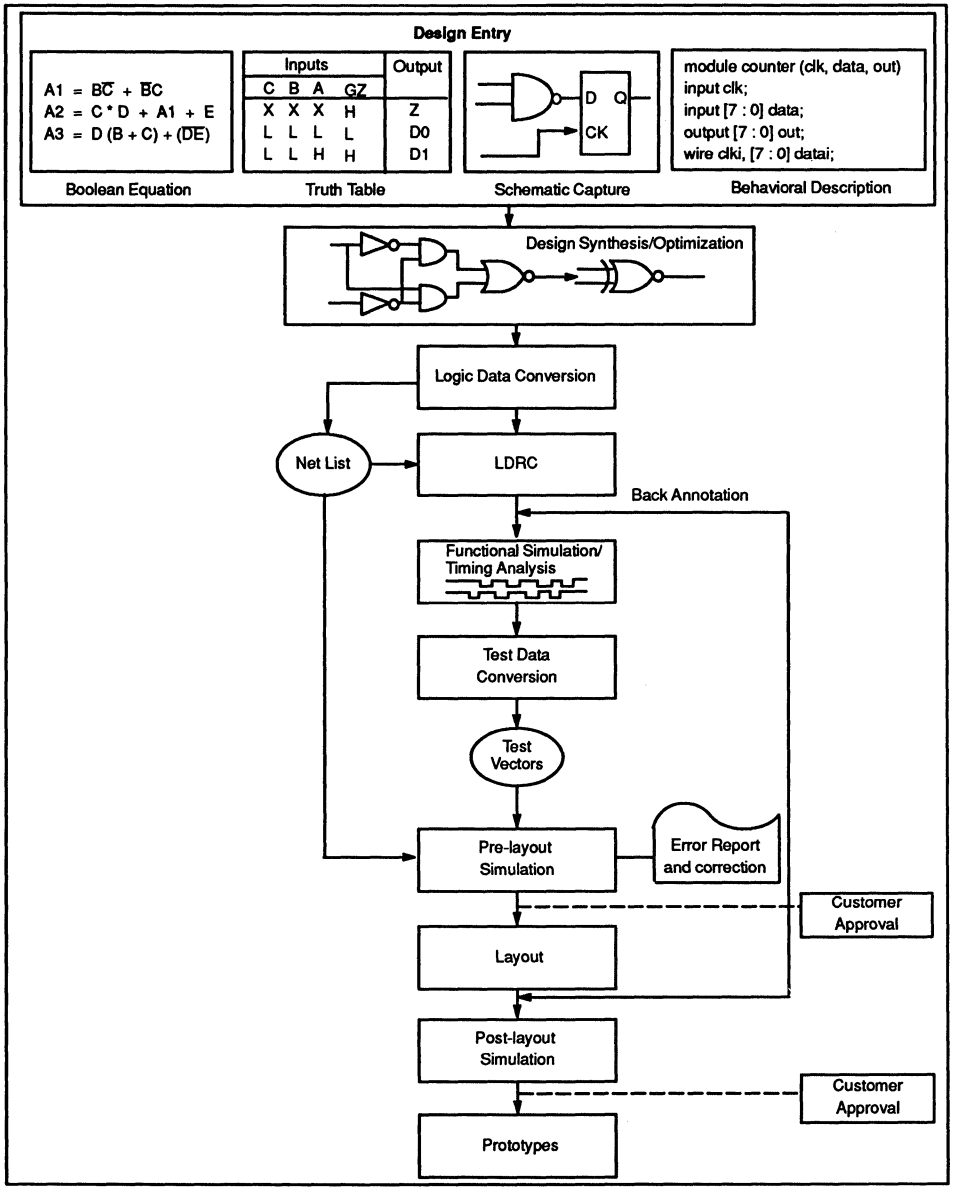


Figure 3–2. Generic Workstation Design Flow

3.3.1 Design Entry

Design entry (schematic capture) is the first step in the generic design automation process. The designer can use the drawing editor program of the applicable workstation software and Fujitsu-supplied symbol

model libraries for schematic capture. In most of the Fujitsu-compatible CAE applications, as in ViewCAD, circuits can be defined as macros, for use as sub-parts of other circuits. Design entry can also be accomplished using Boolean equations, truth tables, or behavioral descriptions.

3.3.2 Logic Design Rule Check

The Logic Design Rule Check (LDRC) module is Fujitsu software, written specifically for each technology to check gate array designs. This program is run before simulation because it catches errors that, undetected under normal workstation design rules, often cannot be tolerated in a Fujitsu gate array. Even a seemingly small design flaw undetected prior to simulation may be severe enough to invalidate the functional simulation of the design and any test signal data that may be generated from as a result. LDRC checks that the design conforms to the logic design rules applicable to all Fujitsu designs, to those unique to a technology and to those required by the chosen package type. When hierarchy is used, LDRC checks for hierarchy violations.

In order to tailor the LDRC to a particular technology, device, and package, the customer enters required information via an LDRC Control File, which supplies the device and package name and sets the LDRC to output information in the form of a report either on all nets or on only nets that contain errors.

LDRC Report

When the LDRC is finished running, it produces a report containing the following information:

a. errors, alarms, and warnings of detected violations

b. chip information such as:
   - number of basic cells used vs. cells available
   - number of unit cells and of different unit cell types
   - total number of unit cell terminals vs. number of connected unit cell terminals
   - total number of nets
   - total number of external input, output, and bus terminals
   - package name
   - signal pins used and maximum number of signal pins available

c. loading unit check list (a list of the load units associated with each input and output signal)

Errors detected during LDRC can now be corrected before the Logic Simulation Program is run.

3.3.3 Functional Simulation

The steps that make up the functional simulation process vary between workstations. For some workstations, functional simulation is all one step, while for others it is three separate steps:

a. logic simulator data base file compilation
b. delay calculation
c. logic simulation

Logic Simulator Data Base File

The logic simulator data base file uses a Fujitsu-supplied library to apply behavioral characteristics such as component functions, delay parameters, loading factors, and minimum pulse width, set-up time, and hold time for flip-flops. These values are supplied by the Fujitsu libraries for the appropriate technology. Input stimulus to the circuit is supplied by the designer in the form of the Control File.

Delay Calculator

Fujitsu provides the program for performing the delay timing calculations. The execution of the program calculates the delay times unique to each net in accordance with the loading condition (fan-out and

hierarchy) in the schematic data file. These calculated delays are representative of pre-layout loading conditions.

The calculations for metal loading are based on the same look-up tables and load equations used in the Design Manual. These loads are subject to change after layout, reflecting the actual metal loads experienced.

Logic Simulator

The event-driven logic simulator evaluates the outputs of each gate as a function of its inputs and displays the results as either a waveform drawing or as a data file. Workstation simulations performed under the influence of the Delay Calculator are vitally important to verification of design functionality and to the creation of successful test vectors. Using in-circuit application stimulus from the Logic Simulator Data Base File, simulations are executed in minimum, nominal, and maximum modes, with timing checks enabled, to ensure that the design is responding as expected and is stable under all conditions. The results are written to a print-on-change file, which is a list of the signals that changed state, their new state, and the time at which they changed.

3.3.4 Logic Conversion (FLDL Generator)

Any errors found by the logic simulation process can be corrected at this point before Fujitsu's Logic Design Language generator (FLDLGEN) program is run on the schematic data file to create the FLDL file. The purpose of the FLDL file is to provide information to the host mainframe for automatic layout and logic simulation. An FLDL control file must be created by the customer containing the customer's name, the workstation type, the revision, the date, and the designer. The FLDLGEN program receives input from the FLDL control file and the schematic data base file created at schematic capture and amended if necessary according to the results of the LDRC and Logic Simulation. The FLDLGEN program can then create a Logic Description (FLDL) file that describes the customer's design for the mainframe software.

3.3.5 Test Data Conversion (FTDL Generator)

The FTDL Generator (FTDLGEN) is a conversion program that translates the Logic Simulator's output file into Fujitsu's Test Description Language. In the process of doing this, it applies Fujitsu tester restrictions to the simulator results. If any signal or timing violations are detected, the operator is informed so that the necessary changes can be made to the data file. The final output file of the FTDL Generator becomes the FTDL File, that is, the test vectors for the mainframe simulator as well as for the LSI tester.

3.4 Post-Design Process

At this point, the customer has gone as far as possible in designing a CMOS gate array on a CAE workstation. Now the design is transferred to the mainframe environment at one of the Technical Resource Centers for mainframe simulation on a Fujitsu M780 35 mips computer. Figure 3–3 describes the post-design process in flowchart form.

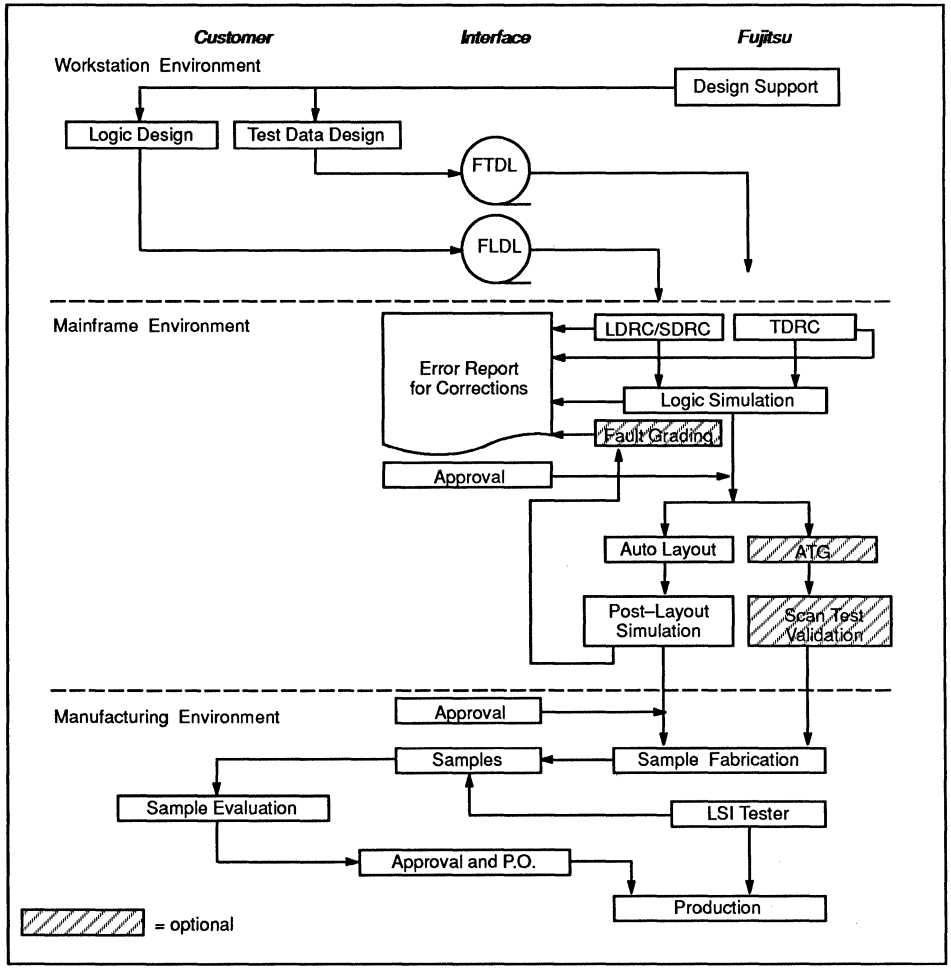


Figure 3–3. Post-workstation Design Process

3.5 Post Design Simulation and Testing

3.5.1 LDRC and TDRC

The FLDL and FTDL files are provided to a Technical Resource Center usually in the form of magnetic tape or floppy disk. On the mainframe, the FLDL is checked by the mainframe's Logic Design Rule Check (LDRC) to confirm the validity of the logic data and for formatting errors, unconnected inputs and outputs, loading conditions, etc. The FTDL file is checked by a similar mainframe program called the Test Data Rule Check (TDRC), which flags any violations of the published test data restrictions.

3.5.2 Pre–layout Simulation

After the LDRC and TDRC have been run successfully on the FLDL and FTDL, the mainframe pre-layout simulation can be performed. This is a logic simulation run at nominal, minimum, and maximum propagation delay times using estimated metalization capacitance values. If there is no discrepancy between simulation results and the expected outputs, the design is presumed to be correct. One of two simulators, LBS6 or ViewCAD, runs functional simulations and timing verification including the checking of set-up and hold time, pulse width, and removal times.

3.5.3 Automatic Layout

After a successful pre-layout simulation has taken place and customer approval has been obtained, a proprietary Fujitsu mainframe application performs automatic placement and metal interconnection routing.

3.5.4 Fault Grading

After post-layout simulation is completed, customers have the option of requesting that Fujitsu subject the test data to a process called fault grading. This CPU-intensive process analyzes the customer's circuit and test data to calculate the percentage of fault coverage. The input test data is analyzed to determine the adequacy of the stimulus patterns to detect any "stuck" (malfunctioning) nodes. The result, a report of all nodes not tested by the stimulus provided, is given to the customer. The customer then has the option of either changing the test vectors or acknowledging that the untested nodes are acceptable.

3.5.5 Post–Layout Simulation

Post-layout simulation, also known as final validation, is again performed at nominal, minimum, and maximum propagation delay times, but using actual calculated capacitance based on the metal interconnection routing resulting from automatic layout.

3.5.6 Sample Fabrication

After a successful post-layout simulation has been performed and customer approval has again been obtained, engineering samples of the array are fabricated for customer evaluation.

3.6 Engineering Sample Testing

3.6.1 LSI Tester

Once sample chips have been fabricated, they are tested on the LSI Tester, a test instrument located at the manufacturing facility. Sample chips are tested with input test patterns and expected outputs obtained from the FTDL file.

One of the most important tasks of post-layout simulation is to validate the test vectors for later use on the LSI Tester. For this reason, simulation is executed under conditions adhering as closely as possible to the conditions imposed by the tester. A device that passes all phases of simulation is likely to pass the LSI tester.

The limitations of the LSI Tester places various restrictions upon test data. These restrictions must be respected when preparing the test data pattern and when creating the (stimulus) Control file for running workstation simulations. A "Summary of Test Data Restrictions" for AU Gate Array technology is included in the AU Design Manual.

Test data restrictions involve such issues at the numbers of test patterns acceptable for each test type, the minimum test cycle length, input signal timing, output strobe timing, bidirectional buffer simulation, input and output cycle timing, tester skew, and the treatment of data signals.

Tests performed on the LSI Tester include the function test, the delay test, the DC test, and the high impedance ("Z function") test. Specific data found in the AU Design Manual must be included in FTDL to perform each of these tests.

3.6.2 Function Test

The function test guarantees the designed function of the gate array by exercising as many of the internal nodes as possible and detecting functional failures. Fujitsu requires the function test because it is the primary means of determining if an ASIC is functioning properly as it comes from manufacturing.

In the course of the function test, input signals are applied in accordance with customer timing specifications, using worst-case input voltage at a clock frequency not to exceed 16 MHz (a period of 63 ns). The dynamic performance of this test also partially verifies the AC characteristics of the device.

The function test may be run in multiple units (blocks), allowing changes to be made in the test vectors to assure thorough testing of the device. The transition from one block to the next requires that the device be powered off, adjustments made to the tester and pins regrouped as required. After all changes have been made, the test is restarted. For this reason, each test block must re-initialize the circuit.

3.6.3 Z–Function Test

The Z-Function test is administered in the last block(s) of the function test. Its purpose is limited to the verification of the high-impedance function of 3-state and bidirectional output buffers. The Z-function test is necessary only when there are two or more logic combinations that can generate the high-impedance state for a given I/O cell. The test can verify all these logic combinations. If only one logic combination generates the high-impedance condition, then the DC test is adequate.

3.6.4 DC Test

The DC test, as its name implies, verifies the DC characteristics of the array. It is not intended to check circuit functionality, but it can be used as a function test of 3-state circuits having only one signal path that generates the high-impedance condition.

The designer supplies the sequence of input signals and expected outputs in the FTDL. These test patterns must generate every possible state for every type of output and input buffer being used (high, low, and high-impedance).

The DC test applies the specified inputs to measure the following DC parameters:

a. Steady state power supply current (I_{DDS})

b. Output high voltage (V_{OH})

c. Output low voltage (V_{OL})

d. Input leakage current (I_{LI})

e. High-impedance output leakage current (I_{LZ})

3.6.5 Delay Test

The delay test is optional. It is used to verify critical paths or as a means to characterize the device by performing this test on a small number of paths. The purpose of the test is to check that signal paths from various inputs of the chip to their respective outputs meet the customer's standards for minimum and/or maximum delay times. The paths may be sequential and/or combinatorial but only the propagation delay, not the toggle frequency, is measured.

3.7 ATG Testing and Scan Design

ATG testing is a special technique that supplements the customer's submitted test patterns (FTDL) to assure both Fujitsu and the customer of a highly reliable gate array by achieving a high degree of fault coverage. ATG testing is implemented by using scan design techniques described at the end of the Design Considerations Chapter. Scan test patterns (both applied input stimulus and expected outputs) are automatically generated by Fujitsu's Automatic Test Generator (ATG) software. ATG is offered by Fujitsu for partitioned arrays of the UHB technology and for all arrays in the channelless gate array technologies.

Chapter 4 – Design Considerations

Contents of This Chapter

4.1 Introduction

Chapter 4 gives an overview of the design hierarchy scheme and the logic and I/O design considerations with which designers need to be familiar in order to optimize a design in Fujitsu's chanelless CMOS Gate Array technologies. This chapter also covers design techniques necessary to implement automated scan path testing of logic circuits and automated testing of compiled cells.

4.2 Basic Cell Usage

In order to benefit from fully automated layout, a designer may use no more than 50 percent of the actual cell count of an AU gate array, 45 percent for CG21 arrays, or 75 percent if the array includes memory or other compiled cells. The actual cell count is the number of basic cells used in the device. AU and CG21 gate arrays utilize internal basic cells as components for I/O buffers; this means that the number of inputs and outputs and therefore input and output buffers required can limit the number of basic cells available for logic design. The utilization guidelines are based on the following formula:

> Basic cells available for unit cells and I/O cells = (total on-chip basic cells – compiled cell basic cells) x 50 percent for AU designs or x 45 percent for CG21 designs.

4.3 Physical Design Considerations

In general, signal delays are caused by the signal having to travel through more gates or over longer distances, especially to enter a different block in gate arrays having block architecture (partitioned arrays) or through thicker interconnect wiring. Delay is proportional to length (and thickness) of interconnection metal along which the signal must travel. The following recommendations are therefore made to optimize overall design speed by minimizing the interconnect metal length and the use of thicker interconnection wiring.

4.3.1 Hierarchical Design

Devices that are partitioned allow the designer to control relative path lengths. AU and CG21 technologies, therefore, require a hierarchical design approach that divides the cells into blocks and the blocks into sub-blocks so that functional groups of unit cells are laid out in close proximity and signals have less far to travel. When it becomes necessary to link blocks, the use of high-power "high-drive" unit cells is recommended to drive signals in the inter-block metal.

The basic cells in the gate arrays are partitioned into as many as eight blocks. Additional blocks are required to accommodate RAM and ROM modules, when used. Blocks of basic cells used exclusively for digital logic gates can have as few as 4,500 basic cells or as many as 10,000.

The physical layout of all AU and CG21 gate arrays is similar. Required block partitioning is a function of software and is not a physical characteristic.

A hierarchical design method not only offers optimal control of path lengths, but also provides a convenient method of design. Hierarchical design allows the designer to divide the circuit into major macro functions and to follow a step-by-step approach in describing their interconnection.

The hierarchical structure is different for unit cells and compiled cells. Figure 4–1 illustrates the hierarchical structure of an AU or CG21 design.

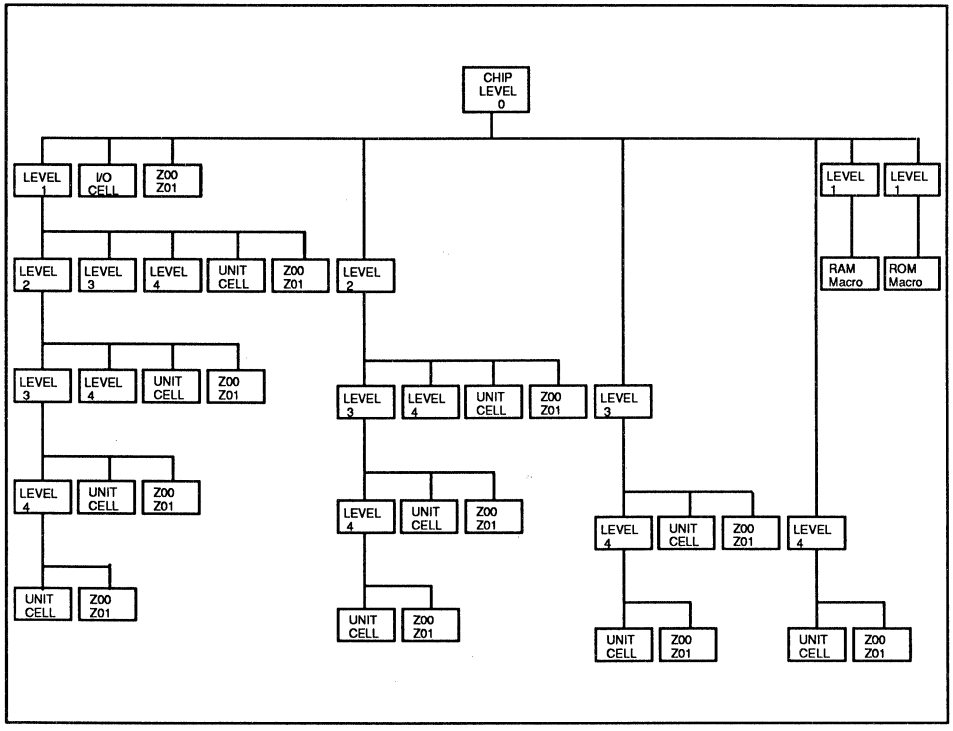


Figure 4–1. Hierarchical Organization of AU/CG21 Designs

4.3.2 The Digital Logic Hierarchical Structure

The CHIP level is the highest level in the hierarchy and represents the entire chip. All I/O cells are defined immediately below the CHIP level, along with any clip cells they may require.

Level 1 blocks must be defined immediately beneath the CHIP level and cannot exceed eight in number (when used for digital logic). Neither unit cells nor compiled cells can be described immediately beneath the CHIP level.

Level 2 is defined beneath the Level 1 blocks, Level 3 beneath Level 2, etc. Levels must always be defined in numerical order. There is no limit to the number of Level 2, Level 3, or Level 4 blocks that may

be used (when defined below a higher block level). Unit cells may be defined beneath Levels 2, 3, or 4, but the lower in the hierarchy the unit cells are defined, the greater the designer's control of delay will be.

Any level may be the first defined under the CHIP level and any of the levels may be omitted; however, the more the designer deviates from the standard structure, the greater the differences between estimated pre-layout delay and actual post-layout delay will be.

The recommended number of basic cells for each hierarchical level is shown in Table 4–1. It is highly recommended that the designer adhere to the guidelines in this table since the tables of estimated metallization load for the cells are based on these block sizes. The basic cell level counts overlap from level to level. The designer may select either of the levels covered by the cell count, but must also use the appropriate table of estimated metallization load for delay calculations.

Table 4–1. Basic Cells per Hierarchy Level

BLOCK under CHIP	Basic Cell Count: AU30K to AU100K CG21303 to CG21104	Basic Cell Count: AU10K to AU20K CG21103 to CG21203
Level 1	4500 to 10,000*	800 to 2500
Level 2	1800 to 5500	300 to 1200
Level 3	400 to 2200	80 to 500
Level 4	maximum 600	maximum 120

*Any block exceeding the recommended maximum of 10,000 basic cells must be designated Level 1.

4.3.3 The Compiled Cell Hierarchical Structure

Each compiled cell (RAM or ROM) must be defined under the level block which resides directly beneath the CHIP level (whether it is a Level 1, 2, 3, or 4). It must be the only cell beneath the level appropriate for the number of basic cells (as defined in Table 4–2) required for that particular compiled cell. The test circuit for a RAM or ROM block cannot be defined in the same block as the RAM or ROM itself. The test circuit should be defined in a block physically close to the RAM or ROM block.

In the CG21 technology, the reccomended number of cell I/Os per block is restricted as shown in Table 4–2. The numbers shown in parentheses in the table is the maximum number of unit cell outputs that can be connected to I/O unit cells (I/O buffers).

Table 4–2. Recommended Maximum I/O Count per Block

Block under CHIP	CG21103 to CG21303	CG21303 to CG21104
Level 1	130 (70)	500 (140)
Level 2	80 (50)	300 (90)
Level 3	50 (90)	100 (60)
Level 4	30 (20)	50 (30)

4.4 Designing for Reliability and Testability

The following general considerations must be made to ensure maximum testability and therefore reliability of a design:

a. External signal paths must be interfaced to the array by an I/O buffer.

b. The outputs of a unit cell other than 3-state bus macros and transmission gates may not be wire-ANDed. Generally, if output functions must be tied together, they must be combined through a logic function.

c. Only one I/O buffer cell can be connected to an external terminal.

d. Inputs to the same cell may not be tied together.

e. Unused inputs must be tied high or low, never left floating.

f. At least one output of a unit cell must be connected.

g. Functions such as one-shots and other monostable or astable circuits cannot be incorporated into a Fujitsu CMOS gate array. All logic state changes detected at the output of the array must be predictable for the purpose of test, and as such, be the direct result of changes of input stimulus. Series inverters must not be used for the purpose of creating a delay.

h. Circuits incorporating sequential devices for instance, flip-flops, counters, shift registers, and so on must have a traceable method of initialization designed into the circuit, independent of feedback loops.

i. No logic function should be incorporated within the array if it cannot be directly or indirectly set or initialized from a primary input. Designers have two choices for initialization:

   1. Supply an external signal for CLEAR, LOAD, etc.

   2. Supply known inputs and allow time for them to propagate through the circuit. If the propagation method is used, UNKNOWN ("X" state) must be an acceptable output state until the initialization is completed.

The information contained in the following sections relates to more detailed aspects of gate array design.

4.5 Clock Networks

A clock network is a circuit used for the efficient distribution of an external clock signal to the clock input of internal sequential and combinatorial unit cells. Skew is the differential delay of a signal as it proceeds through a system. In the context of gate arrays, skew is the effect of a common clock pulse being applied to sequential and combinatorial unit cells at different points in time, because the unit cells are located at different relative positions from the clock pulse origin.

Within a gate array, clock networks may utilize high-frequency and power (HFP), low frequency (LF), or low power (LP) input circuits. Clock networks should be optimized for both internal and inter-chip clock signal distribution applications to minimize skew and to assure high-speed, synchronized operation.

Optimization of clock networks is made possible by the use of the following:

- High-drive input buffers (also called clock input buffers) for HFP and LF input circuits
- Low-drive input buffers (also called data input buffers) for LP input circuits
- Dedicated unit cells (also called clock distribution buffers) driven by HFP, LF, and LP clock input circuits

Up to eight clock input buffers can be used per hierarchical block under the CHIP level and up to 16 clock buffers can be used per design.

4.5.1 High-drive Input Buffers (Clock Input Buffers)

There are two types of high-drive input buffers used for HFP and LF input networks: IKB (an inverting clock input buffer) and ILB (a non-inverting clock input buffer). The IKB and ILB unit cells each have two variations: one incorporates a pull-up resistor on the unit cell input (IKBU and ILBU) and the other features a pull-down resistor (IKBD and ILBD). All have a C_{DR} of 200 lu.

4.5.2 Low-drive Input Buffers

Low-drive input buffers for LP input networks are also available with pull-up and pull-down resistors. Input buffers IB, I1C, I2B, and I2C have a C_{DR} of 36; input buffers I1S, I2S, I1R, I2R feature a Schmitt trigger input and a C_{DR} of 18.

4.5.3 Clock Distribution Buffers

Clock distribution buffers are used to minimize skew by isolating groups of loads from each other and to provide a facility for balancing one group of loads against another. Clock distribution buffers also provide additional drive capability to the clock signal.

Clock distribution buffers must be used immediately following high-drive input buffers in AU and CG21 gate array networks connected to the CK-input of any unit cell.

There are two categories of clock distribution buffer used in AU and CG21 designs: high-drive, with a C_{DR} of 55 and low-drive, with a C_{DR} of 36.

High–drive Clock Distribution Buffers

There are five high-drive clock distribution buffers:

KAB – Block Clock Buffer
KBB – Block Clock (OR x 10) Buffer
KDB – Block Clock (OR x 10) Buffer
K2B – Power\Clock Buffer
V1L – Inverting Clock Buffer

These high-drive clock distribution buffers are restricted to clock signal distribution applications.

These clock distribution buffers must be driven only by the following:

High-drive input buffers (clock input buffers)
Low-drive input buffers (data input buffers)
Schmitt trigger input buffers (maximum signal frequency 13 MHz)

HFP input networks must have KDB clock distribution buffers connected to the outputs of their high-drive input buffers (IKB and ILB) within certain limitations. The maximum number of KDB clock distribution buffers permitted per gate array is also limited by array size. These limitations are set out in full in the

appropriate Design Manual. Use of other clock distribution buffers is unlimited, regardless of the type of input network.

Low-drive Clock Distribution Buffers

There are four low-drive clock distribution buffers (C_{DR} = 36):

K1B – Non-inverting Clock Buffer
K3B – Gated (AND) Clock Buffer
K4B – Gated (OR) Clock Buffer
K5B – Gated (NAND) Clock Buffer

Low-drive clock distribution buffers may be driven by the following:

High-drive input buffers(clock input buffers)
Low-drive input buffers (data input buffers)
Schmitt Trigger input buffers (maximum signal frequency of 13 MHz)
Any other unit cell, including high-drive or low-drive distribution buffers

1

Low-drive clock distribution buffers K1B, K3B, K4B, and K5B may be used in any application, clock or non-clock, that includes regular data signal buffering.

4.6 Internal Bus Circuits

High-performance internal 3-state buses are a feature of AU and CG21 gate arrays using transmission gates for 3-state control. Bus terminator cells are provided to keep the 3-state bus from floating when not being driven. Fujitsu's design software automatically connects the bus terminator cells to the 3-state bus, where they serve to maintain the last logic level applied to the bus prior to the last bus driver's switching to its high-impedance state. This last logic level will be maintained until any bus driver begins to drive the bus line.

The following bus drivers are available:

B11 1-bit Bus Driver
B21 2-bit Bus Driver
B41 4-bit Bus Driver
B81 8-bit Bus Driver
B12 1-bit Block Bus Driver
B22 2-bit Block Bus Driver
B42 4-bit Block Bus Driver

Figure 4–2 shows a typical bus driver cell.

Overall, the total loading factor should be less than the output driving factor for any clock network design. Taking clock skew into consideration, it is recommended to limit the total input loading factor of clock input buffers to 16 lu ($N_{F/O} \leq 16$) and to limit the total input loading factor of clock buffers to 25 lu ($N_{F/O} \leq 25$).

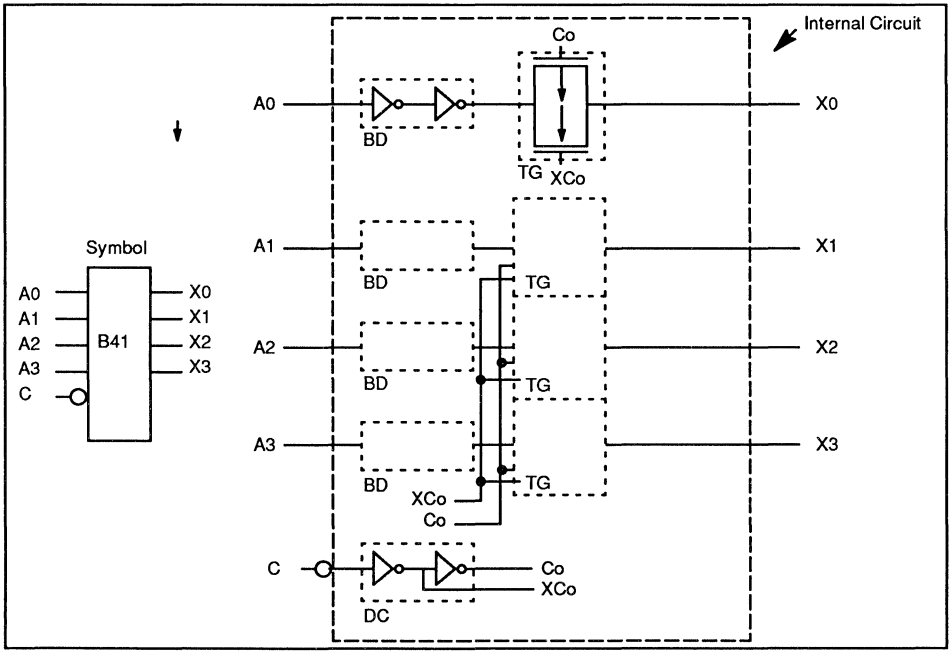


Figure 4–2 Bus Driver Cell, B41

A bus line and associated bus drivers B11, B21, B41, and B81 must reside within the same Level 1 block, immediately below the CHIP level in the design hierarchy. At this time, only a 3-state bus line driven by one of the Block Bus Drivers (B12, B21, and B41) can connect two different blocks. Capacitive loading on bus signal nets is calculated by adding the metal load per the net (N_{DI})and the load factor for all unit cell inputs and bus driver outputs connected to the net where:

N_{DI} = *(number of unit cell inputs) + (Number of bus drivers – 1)*
$N_{F/O}$ = *(sum of $N_{F/O}$s of all unit cells) + (sum of all bus driver Output Load Factors)*

The total load driven by the output of a bus driver must not exceed $2C_{DR}$.

4.7 Transmission Gate Circuits

Transmission gates (TGs) allow the selection of two or more input signals, one at a time, to be extended to the TG output. Certain TGs have more than one output, facilitating the switching of one input of each of two or more groups to each of the respective group outputs. There are, for example, four outputs on the T2F TG. One input of four different input groups can be switched simultaneously to their respective group outputs. Selector terminals on the TGs allow direct control of the internal switches by the designer.

4.8 I/O Pin Assignments

4.8.1 Predetermined I/O Pin Locations

The locations of the following gate array pins are predetermined and cannot be changed:

V_{DD} (+5 volts)
V_{SS} (Ground)
Scan inputs and outputs

The maximum output low current (I_{OL}) must not exceed 70 mA per V_{SS} pin output sink current. All V_{DD} and V_{SS} pins must be connected to power and ground.

If scan testing is included in the design see section 4.9 of this chapter., six scan test pins are assigned predetermined package pin locations.

When scan testing is to be employed, five of the six scan test pins must be dedicated to scan functions and cannot be used or multiplexed with any other signal in the design. If scan testing is not part of the design, the gate array pins otherwise reserved for the scan test pins can be used as inputs.

4.8.2 General I/O Placement Recommendations

The following general parameters apply to the assignment of I/O pins:

a. All V_{SS} pins must be tied to ground.

b. All V_{DD} pins must be tied to 5 volts.

c. Voltage and ground pins are predetermined by the package type and cannot be altered.

d. Pins designated "No Connection" cannot be used.

e. Additional V_{SS} and V_{DD} pins may not be assigned by the designer without first negotiating the change with Fujitsu.

f. Fujitsu recommends that the designer assign the pin numbers to the circuit in the *ASSIGN or *OPTION section of FLDL or submit the complete pin assignment table with the design. It is also possible to allow the Technical Resource Center to do the assignment automatically on the mainframe or manually from a customer-supplied form.

4.8.3 Simultaneously Switching Outputs (SSOs)

Outputs are defined as switching simultaneously when they switch either from a logic low or a high-impedance state. to a logic high, or from a logic high or a high-impedance state. to a logic low within 20 nanoseconds of each other. When an output switches, the gate array either sources current or sinks current, owing to the charge or discharge of the external capacitive load. This charge/discharge current flows through the self-inductance of the power and ground leads of the gate array, producing induced transient voltages across them.

Simultaneously switching outputs increase the momentary charge/discharge current flow at the gate array and cause noise in the form of momentary spikes or ringing in the power and ground lines. The greater the number of SSOs, the greater the noise produced. These spikes and ringing may appear as signals to the CMOS logic, and therefore must be avoided.

When the ground level is raised by the noise, the input threshold voltage of the gates is also raised, relatively, for the duration of the impulse (as illustrated in Figure 4–3). If V_{TH} rises, momentarily, above the V_{IHmin} level, a logic high with a level just above V_{IHmin} will be recognized as a low level for the duration of the spike. Similar problems are experienced when the ground level is depressed by the noise, affecting logic low levels close to V_{ILmax}.

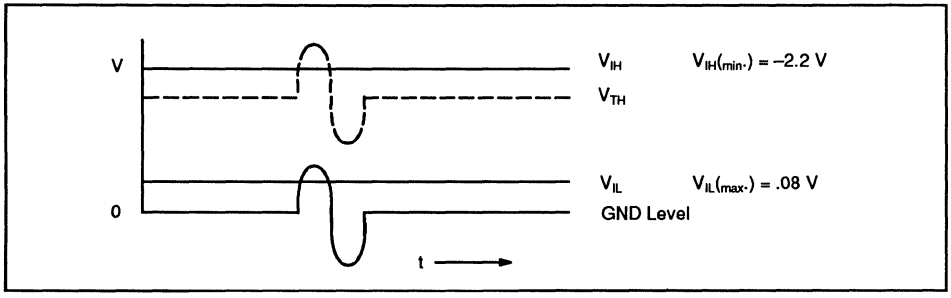


Figure 4–3. SSO–Generated Noise

The severity of the effect of SSOs is determined by:

- The number of SSOs
- The density and distribution of SSOs in the package
- The size of the load capacitance. being driven

The number of SSOs allowed in a package is restricted by the number of ground (V_{SS})pins available, the drive capability of the output buffers, and the location of ground pins on the package (See the Available Package and Pin Assignments section in the appropriate Design Manual). Representative values have been assigned to the effects of output buffers per single ground pin. Output buffers are capable of either 3.2mA or 12mA drive capability, and each may be selected with an optional noise-limiting resistance (NLR) value to minimize generated switching noise. The representative values are given in Table 4.3.

Table 4–3. Representative Value of Output Buffers

Output Buffer	Represenative Values (per Output)
Normal Drive with NLR (IO_L = 3.2 mA)	7
High Drive with NLR (IO_L = 8 mA)	12
High Drive with NLR (IO_L = 12 mA)	14
High Drive with NLR (IO_L = 24 mA)	26
Normal Drive with NLR (IO_L = 3.2 mA)	10
High Drive with NLR (IO_L = 8 mA)	16
High Drive with NLR (IO_L = 12 mA)	20

The sum of the represenative values for each of the SSOs used in a design must not exceed 80 per V_{SS} pin, regardless of the type of package used.

4.8.4 Maximum Load per Ground Pin

The maximum total output load per ground pin is limited as a function of the output switching frequency. The product of the output switching frequency in MHz. and the total output load in pF. per ground pin cannot exceed 12,700 pF x (frequency in MHz), at the maximum junction temperature, T_{jmax}, of 70°C. As the junction temperature increases, the allowable maximum load per ground pin decreases per the following formula:

$$C \times f \leq (12{,}700 \times Kt.)\ pF \times (f_{[MHz]} / (\text{number of ground pins})$$

where C = the output load, in pF

f = the output switching frequency, in MHz

Kt = the junction temperature coefficient of load, a constant determined from Table 4–4.

Table 4–4. Junction Temperature Coefficient of Load

$T_{j(Max.)}$ °C	Kt
70	1.0
85	0.7
100	0.5
125	0.3
150	0.2

4.8.5 Maximum Load per Output Pin

The maximum total output load per output pin is limited as a function of the output switching frequency. The product of the output switching frequency in MHz. and the total output load in pF. of any pin cannot exceed 1200 pF x f_{MHz}, at a maximum junction temperature, $T_{j(max.)}$, of 70°C. As the junction temperature increases, the allowable maximum load per output pin decreases per the following formula:

$$C \times f \leq (1200 \times Kt.)pF \times (f_{[MHz]} / (number\ of\ ground\ pins)$$

where

C = the output load, in pF

f = the output switching frequency, in MHz

Kt = the junction temperature coefficient of load, a constant determined from Table 4–2.

4.8.6 Pin Assignment Guidelines

The locations of all V_{SS} and V_{DD} pins are predetermined and fixed. Since the placement of SSOs on any package is critical, SSOs must be assigned within certain pin groups. Within these pin groups, other restrictions apply regarding the separation of SSOs from each other or their proximity to the V_{SS} pins.

As noted above, the total representative value of any SSO group shown in Table 4–4 must not exceed 80. The SSO pin groups differ between packages. The package outlines and designated grouping of SSO pins for specific devices are shown in the Available Packages and Pin Assignment section of the appropriate Design Manual.

As a general rule, however, the pins available for SSOs between two Vss pins are assigned as follows refer to Figure 4–4.

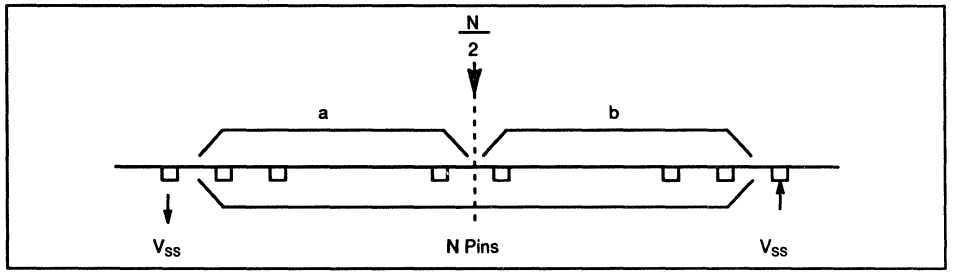


Figure 4–4. SSO Pin Assignments

- Assume that N pins exist between adjacent V_{SS} pins
- Find the center point on the package between the two V_{SS} pins
- There are N/2 pins in the area between the center point and the first V_{SS} pin (part A), and N/2 pins in the area between the center point and the second V_{SS} pin (part B).
- The SSOs must be equally distributed between parts A and B, within ± 1.

4.8.7 The Location of HFP Network Input Buffers

The placement of input buffers for HFP input networks is critical because of the special metalization required. Complete sets of tables in the Available Package and Pins Assignments section of the appropriate Design Manual cover the placement of HFP input buffers, reset, preset, and clear pin assignments.

4.8.8 SSO Pin Placement Summary

The following is a general summary of recommendations for the placement of pins.

a. SSOs must be placed in close proximity to V_{SS} pins.

b. High-drive SSOs should be placed closer to V_{SS} pins than normal-drive SSOs.

c. Asynchronous inputs such as clocks, presets, and clears should be kept away from SSOs. It is preferable that these inputs be placed close to V_{SS} pins, if available, and away from SSOs.

d. Clock, preset, and clear inputs must not be placed on the corners of a package, especially when the array is packaged in a DIP.

e. Output signals to be used as clock, preset, or clear for other devices must be kept away from SSOs and close to a V_{SS} pin.

f. SSOs should not be placed in the outer row of pins of PGA packages.

4.8.9 Test Pins

To facilitate testing, external pins should be provided whenever conditions warrant. The addition of supplementary test pins often allows the reduction of the overall test complexity for a circuit, thus reducing the number of test patterns required and the time necessary to determine functionality of the circuit.

4.9 Scan Test Technology

Scan testing is a supplementary, optional test technique that, when used in conjunction with the function and DC test required of the designer, allows greatly increased fault coverage. This increased fault coverage assures both Fujitsu and the designer of a highly reliable gate array.

4.9.1 Scan Test Design

The designer implements scan testing by arbitrarily connecting all the sequential logic elements to form an enormous shift register. This shift register can contain up to 3000 stages and is formed by connecting the Q-output of one stage to the dedicated scan input (SI)of the next. If the Q-output cannot be used for this purpose, then the XQ-output may be used, but an inverter must be placed between the XQ-output and the SI input of the following state in order that the data not be inverted.

To implement scan testing, designers use special scan-compatible unit cells for all sequential logic functions. With the use of the serial scan method, the difficult problem of testing a logic circuit containing both combinatorial and sequential logic is simplified to testing combinatorial logic and a shift register, as shown in Figure 4–5 below.

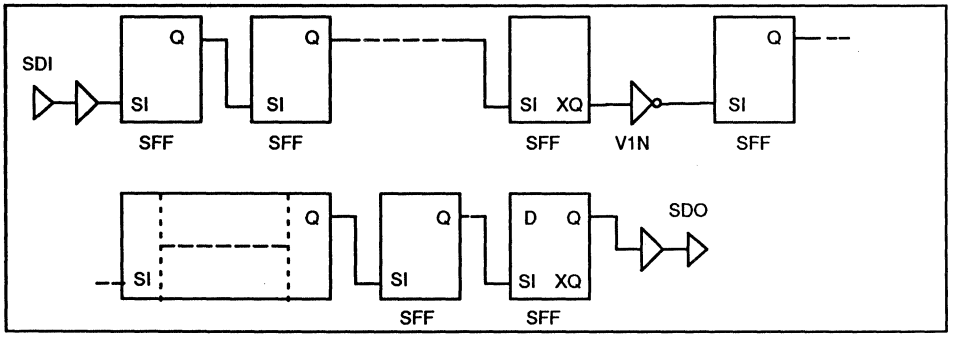


Figure 4–5. Scan Circuit Configuration

Dedicated scan inputs are also used to isolate elements that are not part of the scan test path. Some of these elements can also be tested during the scan test cycle by the use of an alternate scan test mode.

The scan chain design can be considered a data carrier with the ability to carry test input stimulus provided by the LSI tester deep into the design and to apply it to the unit cells under test. Once a unit cell has been tested, its output test result may be stored in the scan data chain and be carried out of the design for comparison to that which was expected. To the designer, can unit cells perform exactly the same as non-scan unit cells, the only difference being the provision of additional basic cells to facilitate the scan test.

Scan testing usually entails an extra 8 to 20% basic cell count, requires the use of seven extra I/O pins, and can cause some degree of propagation delay. Nevertheless, when absolute reliability is the issue, designers find that these considerations are within an acceptable range.

4.9.2 Test Pattern Generation

A circuit that is designed for scan testing in this way allows Fujitsu automatic test pattern generation (ATG) software to generate the scan test patterns automatically (both applied input stimulus and expected outputs). The ATG software uses the logic design data from the FLDL file as input from which it generates the test patterns for scan tests. The process requires that all sequential unit cells be of the scan type with the exception of data latches YL2 and YL4. Inclusion of non-scan sequential circuits constructed with combinatorial logic, (i.e., NAND-gate flip-flops, NOR-gate flip-flops, etc.), are discouraged in a scan design because they reduce the overall fault coverage attainable with scan testing. If their use is unavoidable, they must be disabled or isolated by one of the scan test signals discussed below during the ATG process and the scan test.

Scan testing is optional and is applicable only to digital logic unit cells. Compiled cells such as RAM and ROM are tested using a different technique, which is covered in section 4.10 of this chapter and in the Logic Design section of the appropriate Design Manual.

4.9.3 Scan Test Signals

Scan test implementation requires the assignment of a dedicated output pin and up to seven input pins, six of which are in predefined package locations. The package locations for these pins in each device type are shown in the Available Package and Pin Assignment section of the appropriate Design Manual.

Input Pins ***Description***

1. **XACK** is the scan input, scan output (SISO) A-clock signal. It is generated by the LSI tester and is applied, inverted, to all scan devices at their A-clock input. It writes data from the unit cell's scan input to the master latch.
2. **BCK** is the SISO B-clock signal. It is generated by the LSI tester and is applied, inverted, to all scan devices at their B-clock input. It transfers data between the unit cell's master and slave latches (the output of the device).
3. **XSM** is the SISO mode signal. It is used for set-up of bidirectional buffers, bus drivers, and RAM. If bidirectional buffers or bus drivers are not used, then XSM is not required and need not be included in the design.
4. **XTST** is the scan test signal. It is used to reconfigure the array to make it suitable for scan test and to establish all conditions required for the use of FUjitsu's ATG software. This includes the isolation or removal of certain circuits unsuitable for scan testing, such as non-scan sequential functions and the asynchronous inputs of all sequential elements. (Since they are inaccessible to scan testing, these circuits and disabled functions must, therefore, be tested with user-prepared test patterns.)

   XTST disengages all connections between RAM macro data outputs and RAM macro inputs by inserting scan flip-flops in the paths. It causes the internal compiled cell test circuit to select RAM and ROM address and enable lines and RAM wire enable inputs.

   If all sequential functions utilize scan type unit cells, if no asynchronous functions are employed (including direct sets and clears), and if circuit isolation is not required, then XTST is not required and is not provided for.
5. **XTCK** is the TC mode clock signal. It is generated by the LSI tester. It is applied, inverted, to the IH-inputs of all sequential unit cells.
6. **SDI** is the serial data input port to the first device of the scan path from outside the chip. It is connected to the SI port of the unit cell. Test data entering the SI input subsequent devices in the scan path is derived either from the Q-Output of the immediately previous state or via an inverter from the XQ-output.

   SDI is the only one of the scan test ports that may be used for another function. The designer may also use SDI as a principal input by paralleling the user input with the scan data input.
7. **SDO** is the serial data output port from the last device of the scan-configured shift register to the environment outside the chip. Test data from SDO is taken from the Q-output of the last stage (or from the XQ-output via an inverter) of the giant scan shift register. SDO is the only one of the scan test ports whose location is not fixed; SDO may be placed by the designer at any convenient location.

4.9.4 Scan Test Modes

Scan testing consists of two modes of operation: SISO (Scan input/scan output) mode and TC (test clock) mode. Sequential logic is primarily addressed by SISO and combinatorial logic is addressed by TC; the two modes are alternated during the scan test.

The SISO Mode

This mode causes all elements of the scan path to be written to and read from. In this mode of operation, the following occurs:

a.The scan SISO path is activated by making XSM = 0
b.The scan clocks XACK and BCK are supplied
c.The data to be written is supplied to SDI serial data input
d.The data is read out of SDO and compared with the expected values

These writing and reading operations are performed in parallel.

The TC Mode

This mode tests the array as a normally configured device, but the data is clocked by special clocks provided to the gate array by the LSI tester. In this mode of operation, the following occurs:

a.The scan SISO path is disabled by making XSM = 1.
b. All normal system clocks are disabled, forcing the clock inputs (CK) of all scan unit cells to a logic low.
c. Input signals are applied to normal input pins principal inputs.
d. The TC system clock, XTCK, is applied to the unit cells' IH-inputs.
e. Output signals are read from normal output pins principal output and compared with the expected values.

The alternation of these two modes allows the correct functioning of logic elements not directly accessible from a principal input to be verified. The data scanned in is especially useful in providing control inputs to otherwise difficult-to-control internal logic. Prior to the input of the data to the scan path, some detectable faults can be observed externally by application of inputs to some non-scan external inputs. After data has been clocked into the scan path, other detectable faults can be observed externally. The remaining detectable faults are observable externally after the data has been clocked into the scan path, the TC system clock (XTCK) has been applied, and the resultant data shifted out of the scan path.

4.10 Compiled Cell Testing

Compiled cells (RAM and/or ROM) are tested by accessing the cell I/Os from principal inputs and principal outputs. Some designs may have the data inputs and outputs, the address lines, Read Enable, Write Enable, etc., connected directly to principal inputs and principal outputs, making the test of such macros very straightforward. In most designs, however, some or all of the above are embedded deep in the design, the input signals being derived either from other RAMs or ROMs or from the digital logic unit cells. To gain access to these RAM or ROM I/O ports, the designer must build test access circuits with input and output selectors around the macros.

With the test access circuits in place, Fujitsu prepares the test vectors for all RAM compiled cells.

In the case of ROM compiled cells, Fujitsu tests to determine that the permanently stored data pattern specified by the designer is properly stored and accessible. The designer, therefore, prepares all ROM test vectors.

Test signals from the LSI tester access the RAM and/or ROM macros through principal inputs and principal outputs, and are usually multiplexed with the designer's logic. The multiplexing is accomplished by means of the input selectors and output selectors. Input and output selectors allow the LSI tester to access the designer's logic or the compiled RAM or ROM cells individually to perform the appropriate tests.

Compiled cell testing can take place whether or not scan path testing has been implemented in the design and dedicated scan I/O pins assigned.

Chapter 5 – Delay Estimation Principles

Contents of This Chapter

5.1 Introduction

This section of the data book gives an overview of the delay estimation principles important to the design of an ASIC using Fujitsu's channelless CMOS gate array technologies. Included are the loading rules for AU and CG21 gate arrays and a demonstration of how to estimate the delay through a circuit. In addition to the basic delay equation, this chapter also considers the loading limitations for clock signals and the effects of the operating environment on typical delay figures.

5.2 Choosing Critical Paths

A critical path is a logic path whose timing requirements must be satisfied to ensure proper system function. In an ordinary synchronous circuit, data propagates from one register through combinatorial logic into another register. For the circuit to function properly, the sum of the clock-to-Q delay of the source register, the propagation delay through the logic, and the set-up time on the target register must be less than the worst-case system clock skew. Correct timing of the signal along the critical path guarantees that this condition is met.

Usually, the critical path is the one with the greatest number of gate levels. However, if such a path is speeded up by redesign, another, less complex path may become the new critical path.

For example, in a design in which a path has eight levels of gating, the designer may determine upon inspection that two groups of NAND-NAND structures can be changed to AND-OR inverter cells, an efficient CMOS implementation that noticeably increases the speed of the path. In this case, after applying DeMorgan's theorem and reducing the result, the designer finds that another path is now the critical path.

Since each logic state sensitizes different branches, logic paths must be analyzed using the inputs (rising or falling) that will actually be applied to them (since rising and falling delays are not equal) to determine the longest path that will be sensitized and ensure that it meets critical path requirements.

In this section, a path delay calculation is worked through to show how a designer can analyze each element of a Fujitsu CMOS circuit to make sure the design meets critical path requirements. In this example, the effect of a rising input on the sample circuit is calculated as it would be if this were a critical path and the rising input were forcing the transition of interest.

5.3 Load Units and Loading Guidelines

The Fujitsu CMOS load unit (lu) is the input capacitance of an inverter used as the basic unit for measurement and calculation of capacitive loads presented to unit cells within the gate array. Both the output drive factor of a unit cell and its input load factor are defined in terms of load units.

5.3.1 Output Drive Factor (C_{DR})

The output drive factor (C_{DR}) is a parameter expressing the load driving capability of a unit cell. The output drive factor is provided in the Unit Cell Library for each unit cell in load units. Unit cells can drive loads greater than the output drive factor; however, the performance of CMOS circuits degrades exponentially with increased loading. If too great a load is driven, an exaggerated increase in delay through the unit cell may be experienced.

It is permissible for the load to exceed C_{DR} if the associated additional delays are anticipated and tolerable. Additional calculation factors are required to estimate delays of loads greater than C_{DR}. Figure 5–1 indicates the delays that may be generated when the load exceeds these guidelines.

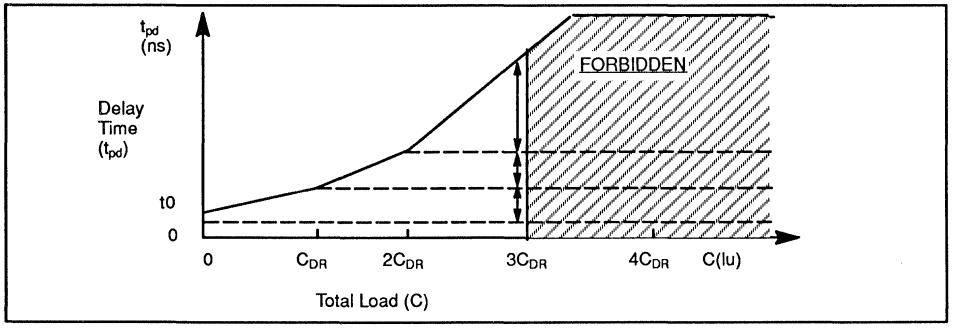


Figure 5–1. Delay Time vs. Loading Factor

5.3.2 Input Load Factor

The input load factor is the value in load units of the load placed on a network by the connection of the input of the unit cell in question. The input load factor for each unit cell is provided in the Unit Cell Library.

5.3.3 Total Input Load Factor ($N_{F/O}$)

The total input load factor or fanout ($N_{F/O}$) is the sum of the input load factor of each of the unit cells connected to the output of the unit cell in question.

5.3.4 Total Unit Cell Load

The delay factor of each unit cell is made up of two types of capacitive loading:

a. Load capacitance inherent in the input of each cell it must drive ($N_{F/O}$)

b. Load capacitance due to the metal interconnection of the unit cells (C_L)

The total load (C) presented by a unit cell is estimated by adding the total cell input load or $N_{F/O}$ (the input loading factors of all other cells connected to the output network of the cell in question) to the total metal load (C_L),

$$or\ C = N_{F/O} + C_L$$

5.3.5 Number of Driven Inputs (N_{DI})

The total metal load (C_L) depends on the number of driven inputs (N_{DI}), that is, the number of other cells to which the output of the unit cell in question is connected. Given the value of N_{DI}, a value for C_L is available from the Estimation Tables for Metal Loading in Appendix C of the applicable Unit Cell Library (reprinted in Sections 2 and 3 of this Data Book). For each value of N_{DI}, C_L varies according to hierarchical level of the cell in question (Level 1, Level 2 etc.) and to its functional logic block status as a main block or a subblock.

5.3.6 Networks

A network or net is considered to be the metal wiring that connects the output of a unit cell to the input(s) of all unit cells that it is driving. Interconnect metal refers to the metal wiring, also called routing metal, that makes up each network. Networks that are not connected to any unit cell clock input are generally classified as data networks and are limited to a maximum load of 3 C_{DR} or 72 lu. It is good design practice to limit loads on data networks to less than 2 C_{DR} during the design phase, otherwise the load may exceed 3 C_{DR} after chip layout.

A network that is connected to the clock input of any unit cell is classified as a clock network and is limited to a maximum load of C_{DR}. A prudent designer will limit loads on a clock network to much less than C_{DR}.

5.3.7 Functional Logic Blocks

In the interest of optimizing critical paths and minimizing interconnect wiring length, logic is divided into functional logic blocks to facilitate unit cell output loading calculation. A block is regarded as a main block or a subblock with respect to a given signal net.

A main block has all of the following:

- the complete network
- the unit cell or block driving the network
- all unit cells or blocks driven by the network

A subblock has some, but not all, of the above characteristics and is a component part of the main block.

The assignment of main block and subblock designations to segments of a circuit facilitates the notation of inter- and intra-hierarchical propagation of signals. The delay values given in the Estimation Tables for Metal Loading (appended to the Unit Cell Libraries) are different for main blocks and subblocks, owing to the difference in the estimated average path lengths encountered in each.

5.4 The Delay Equation

The basic delay equation combines the AC parameters of a cell and its associated capacitive loads to estimate the delay time through the cell. The rise and fall time of a unit cell may not be symmetrical due to differences in the transconductivity of the N and P transistors as well as to differences in the arrangement of the transistors to form unit cells. The same equation is used with different variables for positive-going and negative-going signals at the unit cell output. These signal polarity variables must be considered separately.

$$t_{up} = t_{0up} + K_{CLup}(N_{F/O} + C_L)$$
$$t_{dn} = t_{0dn} + K_{CLdn}(N_{F/O} + C_L)$$

where:

t_{0xx} is the circuit delay through the unit cell under no-load conditions (a value given in ns for each cell in the unit cell library).

K_{CLxx} is the load derating constant or delay time per loading unit conversion factor (ns/pF) (a value defined for each unit cell in the unit cell library).

$N_{F/O}$ is the sum total of the input loads of all unit cells driven in the network (expressed in load units).

C_L is the amount of loading, in load units, on the unit cell output due to interconnect metal (metal load).

5.5 Estimating Gate Delay

1

Figure 5–2 shows a sample circuit for the purposes of demonstrating how the total accumulated delay (tpd) through a short path is estimated.

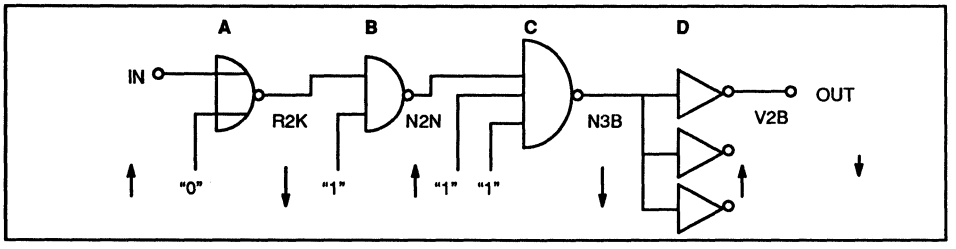


Figure 5–2. Delay Path Sample Circuit

Ordinarily a designer looks up the the specifications of each unit cell in the unit cell library of the applicable technology. For this example, however, all of the necessary specifications have been assembled in Table 5–1, using the values for AU technology.

Table 5–1. AC Parameters of Unit Cells

Cell Function	Cell Name	Basic Cells Used	Input Load Factor	Output Drive Factor	Propagation Delay Time t_{up}		t_{dn}	
					t_0	K_{CL}	t_0	K_{CL}
2-Input NOR	R2K*	2	2	36	0.36	0.11	0.36	0.05
2-Input NAND	N2N	1	1	18	0.30	0.13	0.45	0.11
3-Input NAND	N3B*	3	1	36	1.03	0.07	1.36	0.03
Inverter	V2B	1	2	36	0.20	0.07	0.20	0.04

* These are high drive cells that operate faster than their low drive equivalents under these circumstances.

The delays for rising (t_{up}) and falling (t_{dn}) edges of a pulse can differ widely. Digital pulses are either lengthened or shortened while passing through a unit cell. It is therefore important to calculate the pulse

width variations along the entire signal path to verify that pulse width is sufficient to pass through each gate.

In the example that follows, based on Figure 5–2, calculations are based on a rising pulse entering the input of unit cell A and changing state several times as it proceeds through the sample circuit. To find the total delay for the circuit, it would be necessary to calculate the values resulting from the opposite case, in which a falling pulse enters the circuit at unit cell A.

5.5.1 Delay Parameter for Rising Edge (t_{up})

The unit cell library shows that the delay time (t_0) for an upward transitioning signal at the unit cell output (t_{up}) for R2K, a 2-input NOR, is 0.36. It shows that the load/delay conversion factor for an upward transitioning signal (K_{CLup}) for R2K is 0.11.

5.5.2 Number of Fan-outs ($N_{F/O}$)

The sample schematic in Figure 5–2 shows that the $N_{F/O}$, the number of cells that the R2K must drive, is one (an N2N). The unit cell library shows that the N2N has an input load factor of 1 lu.

5.5.3 Number of Driven Inputs (N_{DI}) and Metal Load (C_L)

The value for C_L is based on the number of inputs the cell in question must drive and is derived from the Estimation Tables for Metal Loading appended in this Data Book to each unit cell library. Table 5–2 is a sample metal load table for a 50KAU device at the sub-block level. Each technology and device has unique load/delay characteristics and the AU and CG21 technologies further divide loading values into main block values and subblock values and then into values for each hierarchical level. Since this sample circuit is very small, it will be assumed to be at a Level 4 in a subblock in the design hierarchy. Because the number of driven inputs (or N_{DI}) for R2K, N2N, and V2B in Table 5–2 is one, the amount of loading due to metallization (C_L) is 1.0 lu. The NDI for N3B in Table 5–2 is three; therefore the C_L is 2.8.

Table 5–2. Estimation Table for Metal Loading

C-50KAU (Subblock)

N_{DI}	C_L(lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	4.7	3.3	2.2	1.0
2	8.6	6.1	3.9	1.9
3	12.6	8.9	5.7	2.8
4	15.2	10.8	7.0	3.4
5	17.2	12.2	7.8	3.8
6	18.8	13.3	8.6	4.2
7	20.6	14.8	9.5	4.7
8	21.8	15.5	9.9	4.9
9	22.5	15.9	10.2	5.0
10	23.1	16.4	10.5	5.2
11	23.1	16.4	10.5	5.2
12	23.4	16.6	10.7	5.2
13	23.9	16.9	10.9	5.3
14	24.5	17.4	11.2	5.5
15	24.5	17.4	11.2	5.5
16 – 30	26.8	19.0	12.2	6.0
31 – 50	31.1	22.1	14.1	7.0
51 – 75	32.1	22.7	14.6	7.2
76 – 100	35.5	25.2	16.1	8.0

The value given for C_L in the Estimation Tables for Metal Loading is an estimate of the loading effect of the metalization capacitance on the output based on Fujitsu's careful statistical analysis of typical designs. Actual metal loading is based on the effect of the routing and therefore may vary from these estimates. To compensate for this uncertainty, Fujitsu incorporates a ±5% variation into the prelayout delay multipliers. After routing, another set of simulations is run to verify the effect of the actual metal routing.

Additional metal loading tables in the Design Manual provide delay values for signals passing between exterior and interior I/O cells and for such signals routed through the heavier metal interconnect wiring required by high frequency signals.

5.6 Estimating Total Circuit Delay

Based on the values from Table 5–1 and Table 5–2, the propagation delay for R2K in the sample circuit is:

$$
\begin{aligned}
t_{dn\,(A)} &= t_{0dn} + K_{CLdn}(N_{F/O} + C_L) \\
t_{dn} &= 0.36 + 0.05\,(1 + 1.0) \\
t_{dn} &= 0.36 + 0.05\,(2.0) \\
t_{dn} &= 0.36 + 0.10 \\
t_{dn} &= 0.46 \\
t_{dn\,(A)} &= 0.5 \quad \textit{(rounded up to the next 0.1 ns)}
\end{aligned}
$$

The propagation delay for N2N, found by following the same procedure, is:

$$
\begin{aligned}
t_{up\,(B)} &= t_{0up} + K_{CLup}(N_{F/O} + C_L) \\
t_{up} &= 0.30 + 0.13\,(1 + 1.0) \\
t_{up} &= 0.30 + 0.13\,(2.0) \\
t_{up} &= 0.30 + 0.26 \\
t_{up} &= 0.56 \\
t_{up\,(B)} &= 0.6 \quad \textit{(rounded up to the next 0.1 ns)}
\end{aligned}
$$

The propagation delay for N3B, found by following the same procedure, is:

$$
\begin{aligned}
t_{dn\,(C)} &= t_{0dn} + K_{CLdn}(N_{F/O} + C_L) \\
t_{dn} &= 1.36 + 0.03\,(3 + 2.8) \\
t_{dn} &= 1.36 + 0.03\,(5.8) \\
t_{dn} &= 1.36 + 0.174 \\
t_{dn} &= 1.534 \\
t_{dn\,(C)} &= 1.6 \quad \textit{(rounded up to the next 0.1 ns)}
\end{aligned}
$$

The propagation delay for V2B, found by following the same procedure, is:

$$
\begin{aligned}
t_{up\,(D)} &= t_{0up} + K_{CLup}(N_{F/O} + C_L) \\
t_{up} &= 0.20 + 0.07\,(1 + 1.0) \\
t_{up} &= 0.20 + 0.07\,(2.0) \\
t_{up} &= 0.20 + 0.14 \\
t_{up} &= 0.34 \\
t_{up\,(D)} &= 4 \quad 0.4 \quad \textit{(rounded up to the next 0.1 ns)}
\end{aligned}
$$

Therefore, the total delay for the sample circuit shown in Figure 5–2 is:

$$
\begin{aligned}
t_{pd} &= t_{dn}\,(A) + t_{up}\,(B) + t_{dn}\,(C) + t_{up}\,(D) \\
t_{pd} &= 0.5 + 0.6 + 1.6 + 0.4 \\
t_{pd} &= 3.1 \text{ ns}
\end{aligned}
$$

5.7 Delay Calculations When Load Exceeds CDR

Fujitsu CMOS gate arrays are capable of driving loads beyond their published Output Drive Factor (*CDR*). It must be emphasized, however, that the delays that result from this practice are considerably increased. Unit cells may be loaded beyond their *CDRS* provided that the increased delay is acceptable.

Anticipation of the effects of loading beyond the published *CDR* requires recalculation of delay. The general formulas for loading beyond *CDR* are listed below; different delay equations must be used depending on the degree that the loading exceeds *CDR*.

The Sea-of-Gates technologies, AU2 and CG21, require two additional parameters to "fine-tune" calculations of unit cell delay under conditions of very light loads. These parameters, *CDR2* and *KCL2* are defined for some selected unit cells.

CDR2: Initial output driving factor—if undefined, then $CDR2 = 0$)

KCL2: Initial delay time per load unit—if undefined, then $KCL2 = 0$)

When *C* is *CDR* or less:

$$tpd = t0 + KCL2 * C$$

When *C* is between *CDR2* and *CDR*:

$$tpd = t0 + KCL2 * CDR2 + KCL * (C - CDR2)$$

When *C* is between *CDR* and *2CDR*:

$$tpd = t0 + KCL2 * CDR2 + KCL * (CDR - CDR2) + 1.5KCL * (C - CDR)$$

When *C* is between *2CDR* and *3CDR*:

$$tpd = t0 + KCL2 * CDR2 + KCL * (CDR - CDR2) + 1.5KCL * CDR + 3KCL * (C - 2CDR)$$

5.8 Clock Loading

It is acceptable, though not a recommended design practice, to load the output of a unit cell that does not carry a clock signal beyond its Output Drive Factor (CDR). To ensure maximum clock accuracy, however, unit cells that output clock signals must never be loaded beyond CDR. Having different loading limitations for clock and non-clock unit cells can lead to "race conditions," in which the clock signal arrives at a flip-flop before the data signal set-up time has elapsed. It is therefore most important, when loading a unit cell beyond CDR, to modify the fundamental delay equation using the extra delay factors explained in the previous section.

5.9 Delay Multipliers

The delay times considered so far are typical delays derived from typical unit cell data. Typical data, however, does not take into account the environmental, thermal, and electrical variations of the real world operating environment. It is necessary, therefore, to simulate worst-case conditions during the simulation and test phases of circuit design. Revised estimates of delay under these harsher circumstances may be arrived at by multiplying the typical delay figures by delay multipliers.

5.9.1 Operating Environment

The operating environment of the array can cause variations from the calculated typical delay figures. Influencing factors include ambient temperature, applied voltage, and variations in the manufacturing processes. Figure 5–3 shows how supply voltage and temperature affect the performance of a sample array when temperature or supply voltage varies beyond the published operating condition specifications for the device. The actual multipliers used depend on the device type.

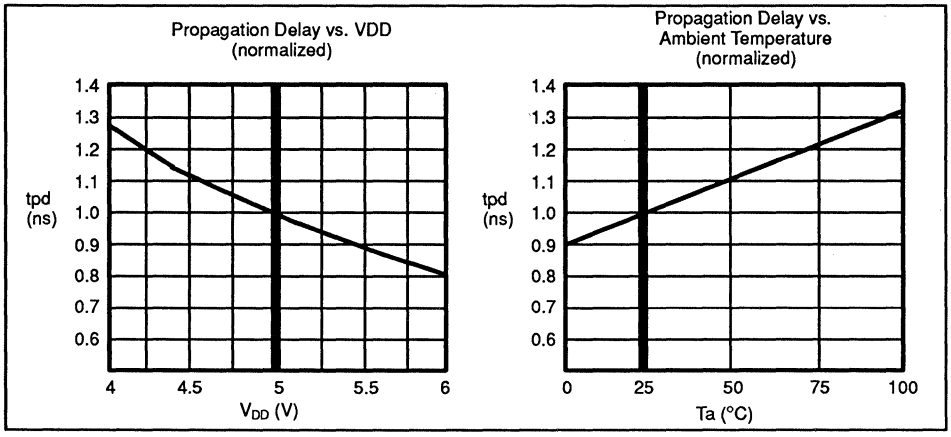


Figure 5–3. Operating Environment Factors Influencing Delay

Maximum and minimum pre-layout simulation delays are derived from delay multipliers applied to the calculated typical delays. Post-layout simulation delay multipliers are based on the capacitance of the actual metalization routing calculated as a function of the layout program.

5.9.2 Minimum and Maximum Delay Factors

Minimum/maximum delay factors for AU and CG21 technologies CMOS gate arrays are as follows:

	Minimum 5 V ±5%, ≥60°C	Maximum 5 V ±5%, ≤60°C
Pre-Layout	0.35	1.65
Post-Layout	0.40	1.55

5.9.3 Factors Affecting Maximum Delay Multipliers

The normal operating temperatures of most arrays, however, will be in excess of 60°C and therefore the delay multipliers for maximum pre- and post-simulation delays must be scaled by junction temperature factors.

Junction temperature is a function of the power dissipated by the array, the thermal resistance of the package selected for the die, and the maximum ambient temperature. The power dissipated by the array becomes a serious consideration in AU and CG21 technology because the gate count and the operating speed of these gate arrays are appreciably higher than those of earlier, channeled arrays.

5.9.4 Calculating Junction Temperature (Tj)

The junction temperature of an array is determined by the following formula:

$$Junction\ Temperature\ (Tj) = T_{aMAX} + \theta ja * Pd\ (°C)$$

The factors affecting junction temperature are as follows:

T_{aMAX} = the maximum expected ambient temperature (°C)

= θja the thermal resistance of the package (°C/W)

= pd the power dissipated by the array (W)

Maximum Ambient Temperature

The maximum expected ambient temperature (Tamax) must be determined by the designer from the application.

Package Thermal Resistance (θja)

The maximum junction temperatures for AU gate array packages are as follows:

Ceramic packages:	150°C
Plastic packages	125°C

The thermal resistance *(θja)* of the chosen package type should be able to dissipate enough power so that the junction temperature (*tj*) does not exceed the maximum junction temperature capability of the package.

Table 5–3 lists the thermal resistances of the larger AU and CG21 gate array PGA packages.

Power Dissipation

The method by which the designer determines the power dissipated by an array is discussed in the following section.

Table 5–3. Package Thermal Resistance In °C/W

Package	Part Number	Array Size	Air Flow (meters/sec.)		
			0	1	3
PGA–135	MB630K MB631K MB632K MB633K MB634K	C–100KAU C–75KAU C–50KAU C–40KAU C–30KAU	30	20	15
PGA–179	MB630K MB631K MB632K MB633K MB634K	C–100KAU C–75KAU C–50KAU C–40KAU C–30KAU	25	19	13
PGA–208	MB630K MB631K MB632K MB633K MB634K	C–100KAU C–75KAU C–50KAU C–40KAU C–30KAU	23	17	12
PGA–256	MB630K MB631K MB632K MB633K	C–100KAU C–75KAU C–50KAU C–40KAU	19	13	9
PGA–299	MB630K MB631K MB632K	C–100KAU C–75KAU C–50KAU	19	13	9
PGA–321	MB630K MB631K	C–100KAU C–75KAU	22 to 24	16 to 18	11 to 13
PGA–361	MB630K MB631K	C–100KAU C–75KAU	22 to24	16 to 18	11 to 13
PGA–401	MB630K	C–100KAU	22 to 24	16 to 18	11 to 13

5.10 Calculation of Array Power Dissipation (P_d) for Delay Multipliers

The worst-case power dissipation of the gate array is the sum of the power dissipations of the individual elemental groups of the array, multiplied by a factor (CV) determined by the power supply variation (tolerance). This factor, CV, is 1.10 for a 5 V ±5% tolerance power supply. The individual elemental groups of the design for which typical power dissipation must be calculated (in mW) are shown in Table 5–4.

Table 5–4. Power Dissipation Calculation Factors

Functional Group	Factor Name
I/O buffers	P_{IO}
Internal logic gates	P_G
RAM (compiled) cells	P_{RAM}
ROM (compiled) cells	P_{ROM}

Typical power dissipation is calculated using the following formula:

$$P_T = P_{IO} + P_G + P_{RAM} + P_{ROM}\ (mW)$$

Worst case power dissipation:

$$Pd = P_T * Cv\ (mW)$$

The formulas used to calculate each of these elements of typical power dissipation (P_T) are listed in the following sections. A table showing values for a representative range of design elements is given following each formula.

I/O Buffer Power Dissipation (*PIO*)

In the calculation of P_{IO}, both AC power dissipation (P_{AC}) and DC power dissipation (P_{DC}) must be considered, as in the following formulation:

$$P_{IO} = P_{AC} + P_{DC}\ (mW)$$

where

P_{AC} is the active (or switching) power dissipation of an I/O buffer and P_{DC} is the power dissipation of an I/O buffer caused by loads sourcing and sinking current external to the array.

Estimation of I/O Buffer AC Power Dissipation (*PAC*)

The AC power dissipation is proportional to the number of I/O buffers switching each cycle at the maximum switching frequency. A decimal factor representing the percentage of buffers switching in each cycle is indicated in the equations below by an asterisk.

In the formulas for the derivation of P_{AC} shown below, 0.20 is used for the percentage of buffers switching in each cycle, reflecting Fujitsu's observation that in the average design, 20 percent of all buffers switch in each cycle. If every buffer switched at the system frequency, this factor would be 1.00.

The AC power dissipation of input buffers = 0.110 mW/MHz

$$P_{ACIN}\ (mW) = 0.11 * (total\ input\ buffer\ count) * f * 0.20$$

where f = the maximum system frequency
0.20 = fraction of buffers switching in each cycle

Table 5–5 shows a representative range of values for P_{ACIN}.

Table 5–5. Input Buffer AC Power Dissipation (PACIN) Examples (in mW)

Average Number of Simultaneously Switching Inputs	Average Input Frequency					
	1 MHz	5 MHz	10 MHz	20 MHz	30 MHz	40 MHz
12	1	7	13	26	40	53
25	3	14	28	55	83	110
50	6	28	55	110	165	220
75	8	41	83	165	248	330
100	11	55	110	220	330	440
125	14	69	138	275	413	550
150	17	83	165	330	495	660

The AC power dissipation of output and bidirectional buffers = 0.030 mW/MHz

$$P_{ACOUT}(mW) = 0.030 * (\text{total output buffer count}) * f * C * 0.20 + 0.030 * (\text{total bidirectional buffer count}) * f * C * 0.20$$

where f = the maximum system frequency
C = the output load capacitance in pF
0.20 = fraction of buffers switching in each cycle

Table 5–6 shows a representative range of values for P_{ACOUT}.

Table 5–6. Output and Bidirectional Buffer AC Power Dissipation (PACOUT) Examples (in mW)

Average Number of Simultaneously Switching Outputs	pF * MHz (per output)*						
	31	63	125	250	500	850	1200
6	5.58	11.34	22.50	45.00	90.00	153.00	216.00
12	11.16	22.68	45.00	90.00	180.00	306.00	432.00
25	23.25	47.25	93.75	187.50	375.00	637.50	900.00
50	46.50	94.50	187.50	375.00	750.00	1275.00	1800.00
75	69.75	141.75	281.25	562.50	1125.00	1912.50	2700.00

*pF *MHz = SUM (loading for each pin in largest SSO group) * SUM (toggle frequency of each output

$$P_{AC} = P_{ACIN} + P_{ACOUT}$$

Estimation of I/O Buffer DC Power Dissipation (P_{DC})

The DC power dissipation of input buffers is so small as to be considered negligible and is not calculated.

The DC power dissipation of output and bidirectional buffers is determined by the following formula:

P_{DC} = Number of Output Buffers ($(V_{IL} * I_{OL} * t_L) + (V_{DD} - V_{OH}) * I_{OH} * t_H$) (Mw)
+ Number of Bidirectional Buffers ($(V_{IL} * I_{OL} * t_L) + (V_{DD} - V_{OH}) * I_{OH} * t_H$) (Mw)

where the terms V_{OL} and $(V_{DD} - V_{OH})$ are typically assumed to be 0.30V, when used for the determination of PDC. The terms t_H and t_L are decimal numbers determined by the duty cycle of the output waveform. They represent, respectively, the waveform's high and low periods.

Table 5–7 shows a representative range of values for PDCOUT.

Table 5–7. Output and Bidirectional Buffer DC Power Dissipation (PDCOUT) Examples* (in mW)

Average Number of Outputs	Output Drive Strength (I_{OL})		
	3.2 mA	8 mA*	12 mA
25	36	80	100
50	72	160	200
75	108	240	300
100	144	320	400
125	180	400	500
150	216	480	600
175	252	560	700

*assuming 50% duty cycle

5.10.2 Internal Gate Power Dissipation

The power dissipation of one internal basic cell is 0.010 mW/MHz.

$$P_G = 0.010 * n * f * 0.20 \text{ (mW)}$$

where

- n = the total number of basic cells used for internal logic design, including internal basic cells for I/O buffers
- f = the maximum system frequency
- 0.20 = factor reflecting Fujitsu's observation that in the average design, 20 percent of all buffers switch in each cycle.

Table 5–8 shows representative range of values for P_G.

Table 5–8. Internal Basic Cell Power Dissipation (P_G) Examples

Active Gates[1]	System Clock Frequency					
	1 MHz	5 MHz	10 MHz	20 MHz	30 MHz	40 MHz
200	2	10	20	40	60	80
400	4	20	40	80	120	160
800	8	40	80	160	240	320
1600	16	80	160	320	480	640
3200	32	160	320	640	960	1280
6400	64	320	640	1280	1920	2560
12800	128	640	1280	2560	3840	5120
25600	256	1280	2560	5120	7680	10240

Note: [1]Active Gate count is typically (Utilized gates)* (Activity Factor) (usually 20%)

5.10.3 RAM Cell Power Dissipation

When the RAM enable input (RE) is at a logic high, the RAM is disabled and the power dissipated by the RAM (P_{RAM}) = 0 mW.

When the RAM enable input is at a logic low, the RAM is enabled and power is dissipated by the RAM. Assuming that half of the address input terminals are switching at the RAM operating frequency f_{RAM}, the power dissipation of a RAM cell is determined by the following formula:

$$P_{RAM} = (0.63 + (0.008 * wp) + (0.036 + (0.045/c)) * bp * f_{RAM} + (7.5) + 01.13/c) * bp * 1.2 \text{ mW}$$

where

- wp = the physical word length (in basic cells) of the RAM
- c = the columnar structure of the RAM (how many physical words wide it is)
- bp = the physical bit size (in basic cells)

Table 5–9 shows a representative range of values for P_{RAM} where f_{RAM} = 25 MHz and c = 2.

Table 5–9. RAM Macro Power Dissipation (PRAM) Examples

Depth	RAM Macro Power Estimate Table		
	Bit Width		
	4	8	16
32	40.45	57.45	91.45
64	43.65	60.65	94.65
128	50.05	67.05	101.05
256	62.85	79.85	113.85
512	88.45	105.45	139.45
1024	139.65	156.65	190.65

5.10.4 ROM Cell Power Dissipation

1

When the ROM enable input (RE) is at a logic high, the ROM is disabled and the power dissipated by the ROM (P_{ROM}) = 0 mW.

When the ROM enable input is at a logic low, the ROM is enabled and power is dissipated by the ROM. Assuming that half of the address input terminals are switching at the ROM operating frequency f_{ROM}, the power dissipation of a ROM cell is determined by the following formula:

$$P_{ROM} = (0.81 + (0.007 * wp) + (0.001 + (0.200/c)) * bp * f_{ROM}$$

where

- wp = the physical word length (in basic cells) of the ROM
- c = the columnar structure of the ROM (how many physical words wide it is)
- bp = the physical bit size (in basic cells)

Table 5–10 shows a representative range of values for P_{ROM} where f_{ROM} = 25 MHz and c = 2.

Table 5–10. ROM Power Dissipation (PROM) Examples (in mW)

Depth	ROM Macro Power Estimate Table		
	Bit Width		
	4	8	16
32	43.075	63.075	103.075
64	45.875	65.875	105.875
128	51.475	71.475	111.475
256	62.675	82.675	1222.675
512	85.075	105.075	145.075
1024	129.875	149.875	189.875

5.10.5 Determination of Maximum Delay Multipliers

Once the maximum junction temperature of the array has been calculated, Table 5–11 must be consulted for the appropriate maximum delay multiplier.

Table 5–11. Maximum Delay Multipliers

Junction Temperature (Tj)	Pre-layout		Post-layout	
	5 V±5%	5 V±10%	5 V±5%	5 V±10%
Tj ≤ 60°C	1.65	1.75	1.55	1.65
60°C < Tj ≤ 70°C	1.70	1.80	1.60	1.70
70°C < Tj ≤ 80°C	1.75	1.85	1.65	1.75
80°C < Tj ≤ 90°C	1.80	1.90	1.70	1.80
90°C < Tj ≤ 105°C	1.85	1.95	1.75	1.85
105°C < Tj ≤ 120°C	1.90	2.00	1.80	1.90
120°C < Tj ≤ 130°C	1.95	2.05	1.85	1.95
130°C < Tj ≤ 140°C	2.00	2.10	1.90	2.00
140°C < Tj ≤ 150°C	2.05	2.15	1.95	2.05

5.10.6 Determination of Minimum Delay Multipliers

The minimum delay multipliers are almost exclusively dependent on the range of ambient temperature. For each ambient temperature range in which the gate array will be used, Table 5–12 shows the minimum delay multiplier. The power supply variation from 5 percent to 10 percent has no noticeable effect.

Table 5–12. Minimum Delay Multipliers

Lowest Ambient Temperature (TA)	Pre-layout		Post-layout	
	5 V±5%	5 V±10%	5 V±5%	5 V±10%
°C < TA < 70°C	0.35	0.35	0.40	0.40
–20°C < TA < 70°C	0.30	0.30	0.30	0.30
–40°C < TA < 70°C	0.25	0.25	0.25	0.25
–40°C < TA < 85°C	0.25	0.25	0.25	0.25
–55°C < TA < 125°C	0.20	0.20	0.25	0.25

5.11 Calculating Delays for Test

5.11.1 Pre-layout Delay Calculations for Delay Test (AC Test)

The min/max delays for the delay test are determined by taking the sum of the typical delays and multiplying it by the appropriate minimum or maximum delay factor. The maximum delay figure must be rounded up to the next highest 0.1 ns, while the minimum delay figure must be rounded down to the next lowest 0.1 ns. The equation shown for typical delay calculation is repeated here and also shown in its modified form. The delay factors used are those for pre-layout in the AU and CG21 technologies. For simplicity's sake, the maximum delay multipliers in this example are unmodified by junction temperature factors. The figures used in this example are those derived from the delay calculations for the sample circuit in Figure 5–2 at the start of this chapter.

Typical delay:

$$t_{pd} = 0.5 + 0.6 + 1.6 + 0.4 = 3.1 \text{ ns}$$

Maximum delay (rounded up to 0.1 ns):

$$t_{pd} = (0.5 + 0.6 + 1.6 + 0.4) \times 1.65 = 5.115 = 5.2 \text{ ns}$$

Minimum delay (rounded down to 0.1 ns):

$$t_{pd} = (0.5 + 0.6 + 1.6 + 0.4) \times 0.35 = 1.085 = 1.1 \text{ ns}$$

5.11.2 Pre-layout Delay Calculations for DC Test, Function Test, and High Impedance Test

The minimum and maximum delays for these tests are determined by multiplying the typical delays for each cell individually by the delay factors. The resulting figures for both maximum and minimum delays are rounded up to the next 0.1 ns for each cell. The final figures for each unit cell of the path are totaled. The delay calculation used earlier is repeated here and is also shown calculated for the DC, Function, and High Impedance tests. The delay factors used are those for pre-layout in the AU and CG21 technologies.

Typical delay (rounded up to 0.1 ns):

$$t_{pd} = 0.5 + 0.6 + 1.6 + 0.4 = 3.1 \text{ ns}$$

Maximum delay (delay for each gate rounded up to the next 0.1 ns):

$$\begin{aligned} t_{pd} &= (0.5 \times 1.65) + (0.6 \times 1.65) + (1.6 \times 1.65) + (0.4 \times 1.65) \\ &= 0.825 + 0.99 + 2.64 + 0.66 \\ &= 0.9 + 1.0 + 2.7 + 0.7 = 5.3 \text{ ns} \end{aligned}$$

Minimum delay (delay for each gate rounded up to the next 0.1 ns):

$$\begin{aligned} t_{pd} &= (0.5 \times 0.35) + (0.6 \times 0.35) + (1.6 \times 0.35) + (0.4 \times 0.35) \\ &= 0.175 + 0.21 + 0.56 + 0.14 \\ &= 0.2 + 0.3 + 0.6 + 0.2 = 1.3 \text{ ns} \end{aligned}$$

Minimum/maximum delays are also calculated this way for minimum clock pulse width, minimum data set-up time, minimum data hold time, preset timing, and clear timing. The values of the maximum and minimum delay multipliers shown above apply to pre-layout calculations only; different factors are used for post-layout analysis.

5.12 Delay Parameters for Compiled Cells

5.12.1 Compiled Cell Construction

The compiled cell is a RAM or a ROM that is automatically generated by Fujitsu-proprietary compilers. It is recommended that no more than four compiled cells be employed within a gate array. Since the compiled cell is a hardware macro, it is important that its dimensions allow it to be placed within the area of the basic cell matrix. It is also required that the remainder of the basic cell matrix be left as close to rectangular as possible (no T- or L-shapes) to facilitate the automatic routing of unit cell interconnections. Space must also be reserved along the outer edges of the macros for internal I/O cells. Unused address inputs of all compiled cells and unused data input terminals of RAM must be tied low to Z00 cells.

5.12.2 Compiled Cell Configuration

The macro's logic parameters must be converted to physical parameters in order that the macro be laid out in the most efficient manner. The resulting compiled cell, or macro, will be physically distributed across a number of columns of basic cells and, within limits, may be one, two, four, or eight words wide, regardless of the number of bits per word.

This columnar configuration (the width of the memory matrix in words) is referred to as the "c" value for the purposes of this discussion. This c value determines the physical (in basic cells) word and bit length (not logical length). In many cases, more than one value of c can be used, allowing alternate configurations of the macro. For example, Table 5–13 below shows the allowable c values for single- and dual-port RAM. For a 256 (word) x 8(bit) RAM, any value (c = 1 through c = 8) can be used.

Table 5–13. Single- and Dual-Port RAM Columnar Configurations

Number of Words	Number of Bits/Word	c Value
4 to 256	8 to 72	1
8 to 512	4 to 36	2
16 to 1024	2 to 18	4
32 to 2048	1 to 9	8

Procedures detailed in the Design Manual allow the size of the physical word, the size of the physical bit, the basic cell count, and the number of address lines needed to be derived from the c value.Table 5–14 below illustrates the calculated parameters for a single-port 256 x 8 RAM.

Table 5–14. Calculated Parameters for Single-Port 256 x 8 RAM

Parameter	Symbol	c Value				Unit
		1	2	4	8	
Physical Word	wp	256	128	64	32	BC
Number of Address Lines	t	8	8	8	8	units
Physical Bit	bp	8	16	32	64	BC
Total Basic Cells	—	6000	4592	4392	5016	BC
X-Dimension	X	20	28	44	76	BC
Y-Dimension	Y	300	164	98	66	BC
Power Dissipation	P	89.9	158.2	302.5	595.0	mW

The optimum configuration must be determined by the requirements of the design itself. As the table above shows, a macro configured with a smaller c value will use more basic cells but will require less power dissipation than a macro configured with a larger c value. The difference in power consumption at each end of the spectrum of possible configurations varies much more widely than does the difference in the number of basic cells used.

If the array design contains compiled cells, additional delay parameters, set out in full in the appropriate Design Manual, must be added to the basic delay equation explained in the previous section. Table 5–15 below shows the delay parameter for a single-port 245 x 8 RAM. As the table shows, the columnar configuration (c value) of a compiled cell has minimal influence on the basic delay times of the macro.

Table 5–15. Delay Parameters for a Single-Port 256 x 8 RAM (AU Series)

Parameter	Symbol	Chosen Value of "c"				
		1	2	4	8	
Read Cycle Time	t_{RC}	21.72	21.44	21.41	21.37	Read Operation
Address Access Time	t_{AA}	20.79	20.64	20.65	20.71	
RAM Enable Access Time	t_{RA}	19.79	19.71	19.68	19.83	
Output Hold from Address Change	t_{OH}	5.95	5.84	5.94	6.34	
Output Hold from Enable Change	t_{RH}	2.85	2.86	2.87	2.90	
Write Cycle Time	t_{WC}	21.72	21.44	21.41	21.37	Write Operation
Enable to End of Write	t_{RW}	15.27	14.94	14.87	14.88	
Address Valid to End of Write	t_{AW}	18.57	18.24	18.17	18.18	
Address Setup Time	t_{AS}	3.30	3.30	3.30	3.30	
Write Pulse Width	t_{WP}	11.82	10.94	10.54	10.38	
Data Setup Time	t_{DW}	10.17	9.28	8.84	8.61	
Write Recovery Time	t_{WR}	3.15	3.14	3.19	3.24	
Data Hold Time	t_{DH}	3.59	3.66	3.81	4.11	

Frequency of Operation: 5MHz

All units are in ns

Chapter 6 – Quality and Reliability

Contents of This Chapter

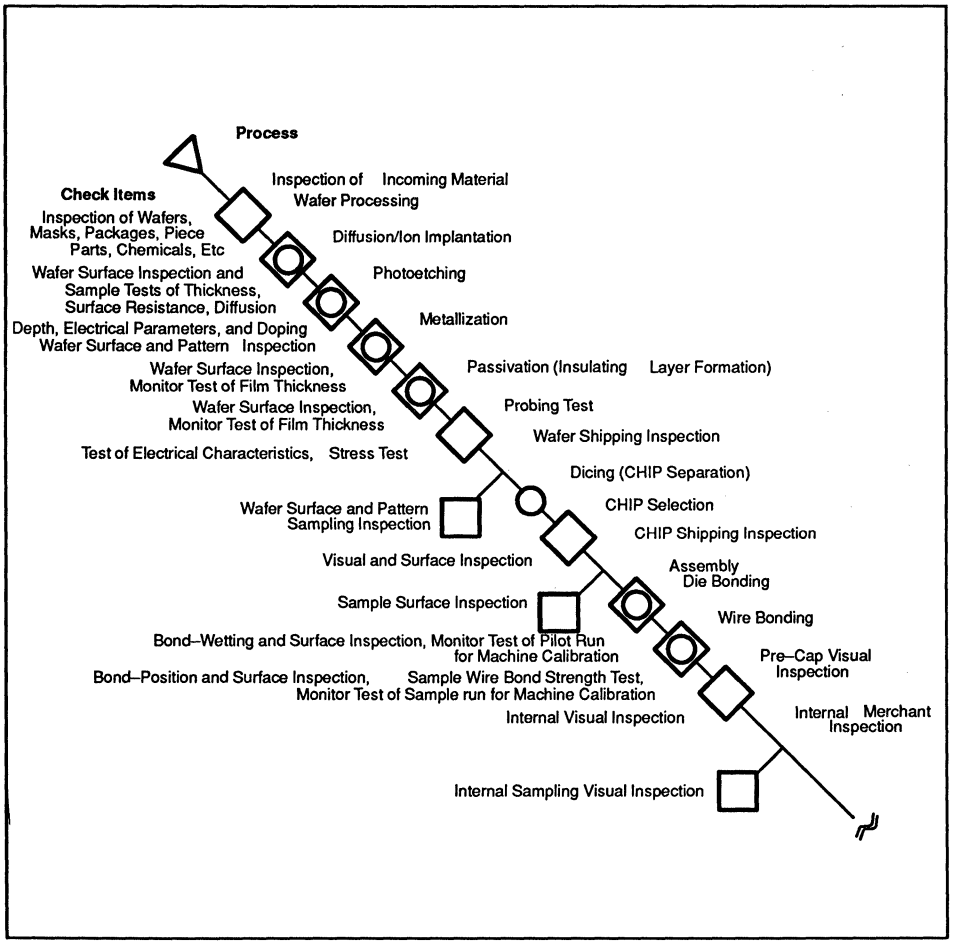
6.1 Introduction

Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

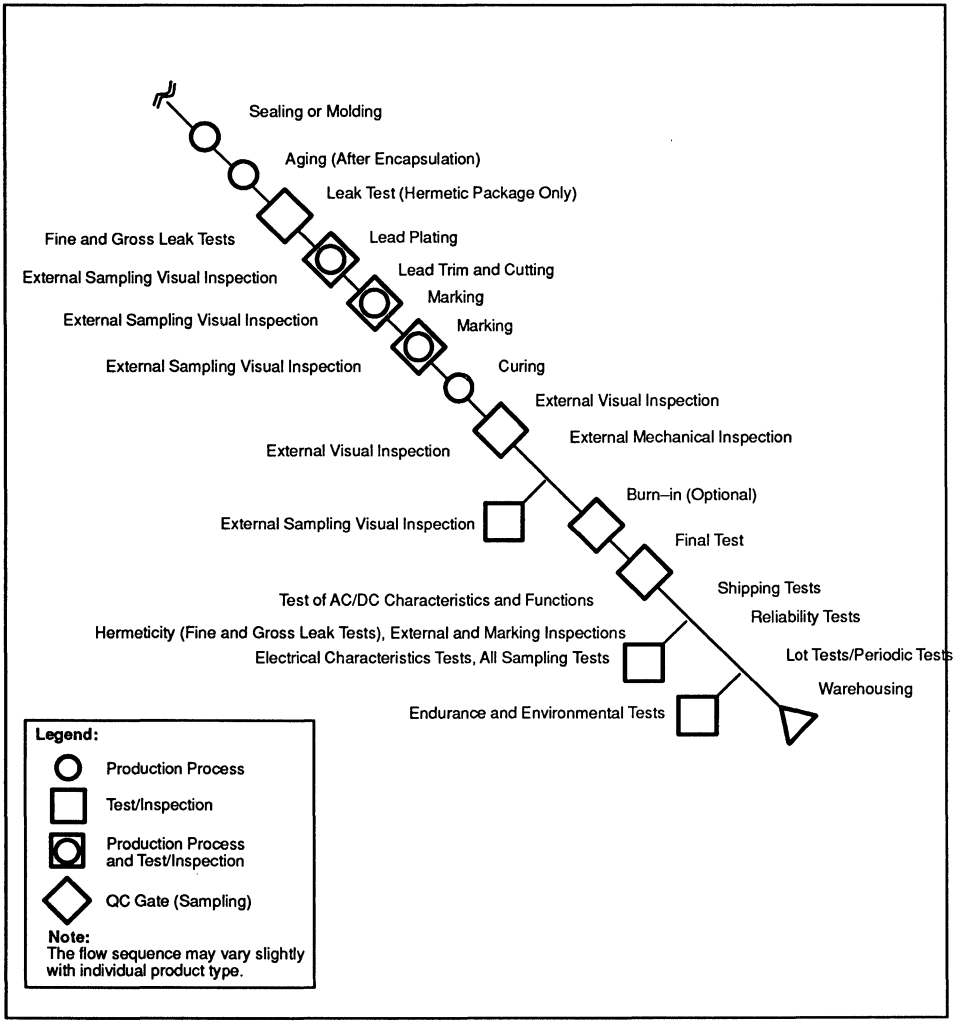
Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.



Quality Control Processes at Fujitsu



Quality Control Processes at Fujitsu (Continued)

6.2 Engineering Testing

Engineering testing is the heart of reliability and quality control. The reliability engineering department plans and performs most engineering testing. Whenever a device is developed, it must undergo engineering approval tests. After the device passes these tests, production engineering approval tests are performed on a representative sample of the device. All factors that could influence production of the device are examined. Only if all conditions are favorable and the device passes thorough testing, can the new device go into production.

Tables 6–1a through 6–1d show a sampling plan for engineering testing. These tests are in compliance with MIL-STD-883, Class B. When a change in production (e.g., a material change) is needed, engineering tests are performed on specific items for the change.

Since the representative samples tested must accurately reflect the reliability of the device, the following conditions must also be satisfied: the functions performed by the same basic circuit; the same processing techniques, materials, parts and packages used; and the same processing followed at the same factory.

Table 6–1a. Sampling Plan for Engineering Testing: Endurance Test

Test Items	MIL-STD-883	LTPD* (%)	Acceptance number**	Note
High-temperature storage 150°C	1008 C	7	1	
High-temperature continuous operation 150°C or 125°C	1005 D	7	1	
High-temperature continuous operation 125°C	1055 D	5	2	
Low-temperature continuous operation –55°C	(1055 C or D)	7	1	As applicable
High-temperature high-humidity storage 85°C, 85% RH	—	7	1	Plastic package only
High-temperature high-humidity continuous operation 85°C, 85% RH	(1005 C or D)	7	1	Plastic package only

* Lot test percent defects

** Number of failures permitted per lot

Table 6–1b. Sampling Plan for Engineering Testing: Environmental and Mechanical Test

Test Items	MIL–STD–883	LTPD (%)	Acceptance number	Note
External visual inspection	2009	15	1	Same sample
Physical dimensions	2016	15	1	
Radiophotography	2012	3 devices	0	
Internal visual inspection	2013	15	0	
Lead integrity: Tension Bending stress Lead fatigue	 2004 A B B	 15 15 15	 0 0 0	Devices which failed in electrical characteristics test are acceptable to this test. Each test is performed on one third of the leads of each sample.
Resistance to soldering heat	—	7	1	Same sample
Temperature cycling	1010 C	7	1	
Thermal shock	1011 A	7	1	
Vibration, variable-frequency	2007 A	10	1	
Mechanical shock	2002 B			
Constant acceleration	2001 D			
Seal: (Fine and gross leak checks)	1014 A C	7 7	1 1	Hermetic package only
Resistance to solvents	2015	40 devices	1	Devices which failed in electrical characteristics test are acceptable to this test.
Solderability (260°C)	2003	15	1	Devices which failed in electrical characteristics test are acceptable to this test.
Solderability (230°C)	—	15	1	Devices which failed in electrical characteristics test are acceptable to this test.
Internal water–vapor content	1018	3 devices	0	Hermetic package only
Electrostatic discharge sensitivity	3015 A	15	1	
Pressure-Temperature-Humidity Storage (PTHS) 121°C, 2 atm.	—	15	1	Plastic package only

The following tests are performed only when required or when requested by the customer.

Table 6–1c. Sampling Plan for Engineering Testing: Environmental and Mechanical Test (Optional)

Test items	MIL-STD-883	LTPD (%)	Acceptance number	Note
Bond strength	2011 D (or C)	15	2 wires	34 wires/4 devices
Die shear strength	2019	3 devices	0	Hermetic package only
Moisture resistance	1004	15	0	
Salt atmosphere (corrosion)	1009 A	15	0	
Vibration fatigue	2005	15	0	
Immersion	1002 B	15	0	
SEM inspection of metallization	2018	3 devices	0	
Particle impact noise detection (PIND) test	2020 B	15	1	Hermetic package only
Lid torque	2024			Frit sealed package only, as applicable
Adhesion of lead finish	2025			As applicable

Table 6–1d. Sampling Plan for Engineering Testing: Continuity Test

Test item	MIL-STD-883	LTPD (%)	Acceptance number	Note
Continuity check	—	5	2	Plastic package only

6.3 In-process Inspection and Quality Control

Every department involved in the manufacturing process is responsible for the quality-control inspection in its sphere of operation. In-process checks, sampling tests, and other inspections are assigned so that each department has certain allotted tasks for which it takes full responsibility. This total control system has rationalized overall operations dramatically.

6.3.1 In-process Checks (Including screening)

In-process checks are performed after each step critical to the next process in wafer processing and assembly. Defective or substandard products are weeded out at an early stage. Testing falls into the following three categories:

(a) Probe testing, chip selection, and final testing. These are defined for each process.

(b) Voluntary checks. These include inspection of the wafer surface after window opening (before the diffusion process) and inspection of the wafer surface after the metallization.

(c) 100 percent screening. This includes the aging and visual inspection performed during wafer processing and assembly.

6.3.2 In-process Sampling Test

The in-process sampling test is performed as a part of process quality control. The Manufacturing and QC departments check randomly drawn samples at key points in the manufacturing process to check process and facility conditions. This helps in maintaining product quality at the customary high level. The following items are checked in these sampling inspections or monitoring:

(a) Surface resistance after diffusion, film thickness, evaporated or sputtered electrode thickness, and device characteristics

(b) Product quality (checked by visual inspection of the chip surface)

(c) Bonding machine calibration, visual inspection and bond strength after wire bonding, product appearance, marking permanency

6.3.3 In-process Inspection

The Manufacturing and QC departments perform stringent quality checks between major processes to ensure the highest quality. The following four types of inspections are performed:

(a) Incoming materials, parts, and chemicals Inspection

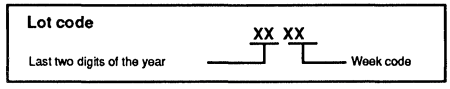
(b) Wafer shipping inspection

(c) Chip shipping inspection

(d) Shipping test

6.3.4 Lot Configuration

A "lot" consists of the same devices produced over a stated period, having the same design and using the same processing techniques, materials, and production line. In addition to the Fujitsu logo, part number, and other markings, each device is marked with a lot code as shown below.



6.4 Reliability Theory

6.4.1 Estimating the Failure Rate

The graph of a component failure distribution is usually a downward–bowed curve, often called the bathtub curve (Figure 6–2). Life tests show that the instantaneous failure rate decreases with time and graphs as a straight line on a Weibull probability chart (Figure 6–3). Shape parameter m, which shows the instantaneous failure rate, is between 0.3 and 0.7. (In an exponential distribution, the instantaneous failure rate does not change and m = 1. As m becomes smaller than 1, the instantaneous failure rate decreases with time.)

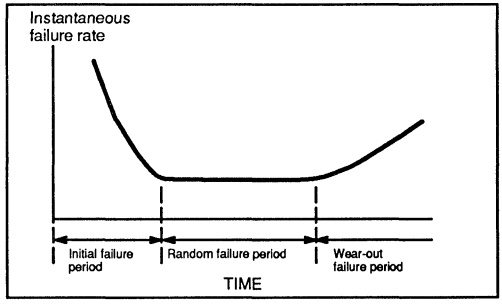


Figure 6–2. Distribution of Component Failure

Usually, the failure rates during the initial and random failure periods are the most important for semiconductors. Figure 6–3 shows an example of life test data graphed on a Weibull probability chart.

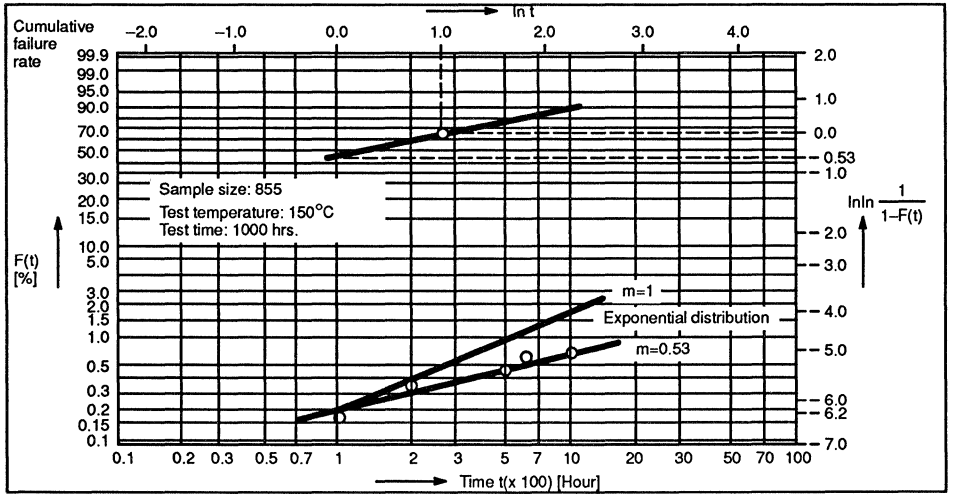


Figure 6–3. Example of Life Test Data on IC

6.4.2 Accelerated Life Test

Modern applications require an extremely low failure rate for semiconductors. To guarantee such strict quality requirements, Fujitsu uses an accelerated life test. There is no fixed acceleration rate for semiconductors but, since semiconductor failure is usually caused by physical and chemical changes in materials, an acceleration rate can be calculated from the Arrhenius equation below for the progress speed of physical and chemical phenomena (assuming the R is proportional to the degradation speed):

$$R = A \exp(-Ea/kT)$$

where:

- R: Reaction rate
- A: Proportionality constant
- E_a: Activation energy
- k: Boltzmann constant
- T: Absolute temperature

The proportionality constant A corresponds to the component reliability. The activation energy, E_a, depends on the component's materials and their combination, but it ranges from 0.3 to 1.35 eV for semiconductors. This equation does not fit the data perfectly because it assumes that the failure rate is affected only by temperature when, in fact, there are many contributing factors. However, the equation does give a good rough fit. Using the equation on data from the accelerated life test, engineers can estimate and guarantee the field failure rate with reasonable accuracy.

The calculation method for the field failure rate is given below for Fujitsu semiconductor products. Although this method is not generally accepted yet, it has been found to be useful.

(1) Calculate the junction temperature (Tj(op)) for actual use from the temperature rise (Tj) and the ambient temperature (Ta) under an average load (do not use the worst–case load), Tj(op) = ΔTj + Ta.

(2) Calculate the junction temperature (Tjt) for a life test. For a high-temperature storage test, Tjt equals Ta (the storage temperature). For a continuous operation test, the temperature rise

under load plus the ambient temperature (25°C except for high-temperature operation) for an operating temperature, Tjt = ΔTj + Ta .

(3) Calculate the acceleration rate (α) from the difference of Tj(op) and Tjt using Figure 6–4.

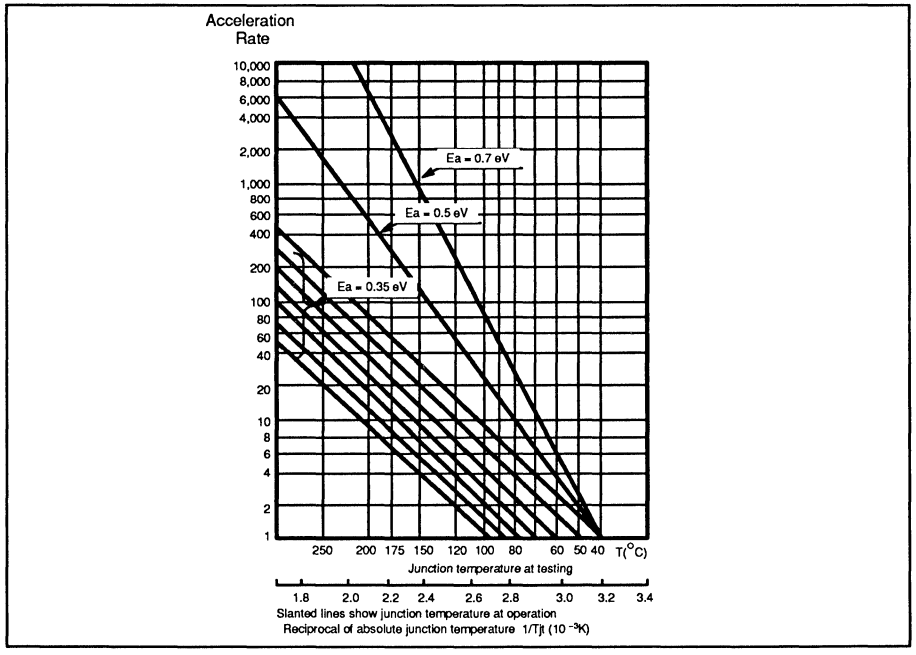


Figure 6–4. Acceleration Rate vs. Junction Temperature

(4) If planning reliability testing or calculating reliability in the field from data obtained in steps (1) to (3), determine the coefficient γ for the 60% confidence level in Table 6–2 from the number of defective units allowed or from the total number of failures found in the test.

$$\text{Reliability} = \frac{n}{\alpha NT} \times \gamma \times 10^9 \text{ [FIT]}$$

where:

N: Number of samples
T: Total test time (hrs)
n: Number of failed samples in test

Table 6–2. Determination of Coefficient

No. of failures	Confidence level	
	60%	90%
0	(0.92)	(2.30)
1	2.02	3.89
2	1.55	2.66
3	1.39	2.23
4	1.31	2.00
5	1.26	1.85
6	1.22	1.76
7	1.20	1.68
8	1.18	1.62
9	1.16	1.58
10	1.15	1.54

The above equation applies only when n/N is equal to or less than 10% for the total test time, T. If n/N exceeds 10 percent, use the following method of calculation: divide the total test duration time, T, into subsections, Δt_i ($i = 1,2, \ldots, m$), so that for each Δt_i the failure rate, $(n_{i+1} - n_i)/(N - n_i)$ (where n_i is the cumulative number of failed samples for Δt_i), does not exceed 10 percent. Calculate $(N - n_i)\,\Delta t_i$ for each time section Δt_i. Calculate the summation $\Sigma(N - n_i)\,\Delta t_i$ for all the time sections in T. The summation $\Sigma(N - n_i)\,\Delta t_i$ must then be substituted for NT in the above equation.

1

6.4.3 Failure and Causes

Circuit format differences, package types, and operating environments can change the mechanisms of IC failures, so it is difficult to foresee which factor will be the most important in a failure mechanism. Figure 6–5 shows specific electrical failures for ICs, their most common causes, and general corrective actions. Causes of IC failures are largely the same as for planar transistor failures, but the following problems are more common or specific to ICs:

(a) Surface degradation

(b) Flaws in an evaporated or sputtered metal film

(c) Contact failures due to an increased number of wire bondings per package

(d) Package failures due to an increased number of external leads

Table 6–3 lists failures with their most common causes, and Table 6–4 shows the relationship between operating environments and failure causes. Test items can be listed only if the failure cause can be pinpointed by the test.

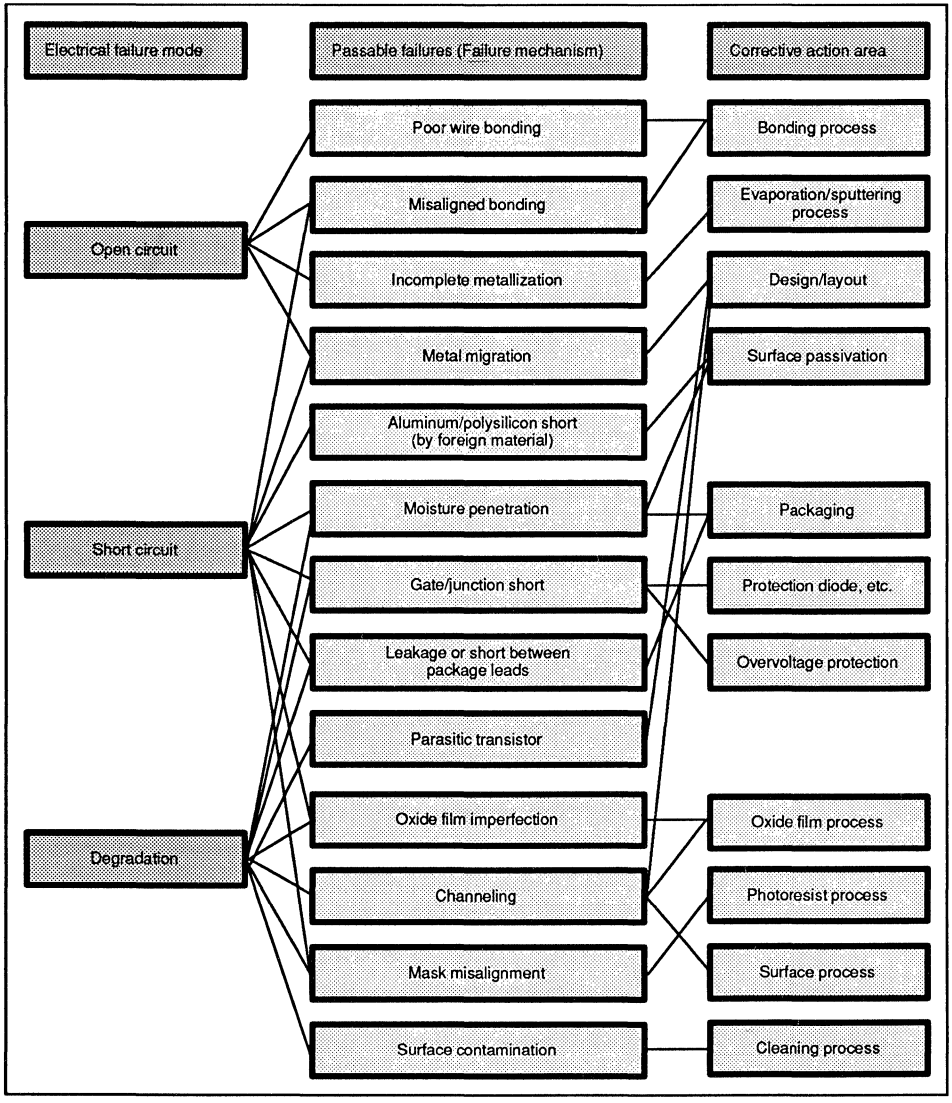


Figure 6–5. Digital IC Failures and Corrective Actions

Table 6–3. Process Defects Analysis

Defect Area	Defect mechanism	Frequency	Source				
			Design	Factory Process Control	Manuf. Tech.	Operator Skill	User Application
Junction (Internal)	Junction failure due to current crowding	High	•				•
	Metal migration	Low	•	•	•	•	
Junction (Surface)	Oxide film imperfection (Pinhole, crack, void, etc.)	Medium		•		•	
	Impurity contamination	High	•	•		•	
Inter-connection	Metal peeling	Medium		•	•	•	
	Mask misalignment	Medium				•	
	Incomplete metallization	Medium		•	•	•	
	Improper metallization	Medium					
	Metal over-stress	High					•
	Aluminum corrosion	Medium		•	•	•	
Wire	Aluminum migration	Medium	•			•	
	Bonding peel	High			•	•	
	Purple plague	Medium	•		•	•	
	Wire over-stress	High				•	•
Package	Particle/wire short	Low				•	
	Leakage	Medium			•	•	
	Die bond failure	Low	•		•	•	
	Lead breakage	Medium			•		•
Others	Package corrosion	Medium	•	•	•		•
	Chip crack	Medium			•	•	•
	Seal contamination	Low		•		•	

Table 6–4. Relationship between Failure Causes and Analytical Test Methods

	Test											
Failure Cause	Solder-ability (2003.2)	Temper-ature Cycling (1010.2)	Thermal shock (1011.2)	Constant Acceleration (2001.2)	Mechanical shock (2002.2)	Vibration, variable frequency (2007.1)	Lead fatigue (2004.2)	Baro-metric pressure reduced (1001)	Moisture resistance (1004.2)	Salt atmos-phere (1009.2)	Vibration fatigue (2005.1)	Vibration noise (2006.1)
Bond integrity (Chip or wire)		•	•	•	•	•					•	•
Cracked chip		•	•		•							•
Internal structural defect					•	•						
Contamination-/ contact-induced short		•		•	•	•					•	•
Wire or chip breakage				•	•	•					•	
Glass crack	•	•	•		•		•	•				
Lead fatigue contamination of junction (Surface)	•	•	•				•					•
Thermal fatigue		•										
Seal integrity		•										
Seal contamination				•	•	•						•
Leakage		•	•				•	•	•	•		
Package/material integrity		•	•		•			•	•	•		

6.5 Reliability Testing

Reliability testing includes three types of tests—lot tests, periodic tests, and "occasional" tests. This section explains the details of each test in turn.

6.5.1 Lot Tests

There are two types of lot tests, Group A and Group B. Group A and Group B tests are performed on items that are tested regularly, usually every week. Table 6–5 lists the specific lot tests.

Details of individual tests vary with the product under test, but all samples are selected at random from every weekly lot. Tests are not performed in any particular order unless specified, but are performed for each device type.

Note that the high-temperature storage and continuous-operation tests for Group B usually take 500 hours, although they may take only 168 hours in special cases. Good samples are returned to their lots after non-destructive testing. No-good samples and samples that have undergone destructive testing are destroyed.

6.5.2 Periodic Tests

Particulars of the periodic tests are also listed in Table 6–5. There are two types of periodic tests: Group C tests and Group D tests. Group C tests are performed on items that are tested regularly, usually every 13 weeks. Group D tests include special reliability tests and very long life tests. The Group D tests are usually done once every 26 weeks.

Details of individual tests vary with the product under test, but all samples are selected at random. Tests are not performed in any particular order unless specified, but are performed for each device type. Note that the high-temperature storage and continuous-operation tests for Group C take 1000 hours and those for Group D take 3000 hours.

Table 6–5. Sampling Plan for Reliability Testing

Group	Subgroup	Device classification		Device group 1		Device group 2	
		Test items		Sampling plan			
A	A1	External visual inspection		100% test of sampled devices (All sampled devices)			
	A2	Electrical Characteristics	Function test	LTPD 5% $A_c = 0$			
	A3		Static characteristics	LTPD 5% $A_c = 0$			
	A4		*Dynamic/Switching characteristics*	LTPD 5% $A_c = 0$			
				Sample size	Acceptance number	Sample size	Acceptance number
	B1	Physical dimensions		9	1	6	1
B	B2	Environmental tests	*Resistance to solvant +temp-cycling*	9	1[8]	9	1[8]
			Thermal shock test	9	1[8]	9	1[8]
	B3		*Mechanical environmental test*	9	1	9	1
	B4-I	Solderability (230°C, 5s)[1]		9	1	3	1
	B4-II	Solderability (260°C, 5s)[1]		9	1	3	1
	B5	Lead integrity[1]		9	1	3	1
		Pressure-temperature-humidity storage[2]		9	1[3]	3	1[3]
	B6	*Pressure-temperature-humidity bias*[2]		9	1[7]	3	1[7]
	B7	Endurance test	*High-temperature storage*	14	1[4]	7	1[4]
	B8		*Continuous operation*	24	1[4]	11	1[4]
	B9		*High-humidity storage 85°C, 85% RH*[2]	24	1[4]	11	1[4]
C	C1		*High-temperature storage*	14	1[5]	7	1[5]
	C2		*Continuous operation*	24	1[5]	11	1[5]
	C3		*High-humidity storage 85°C, 85% RH*[2]	24	1[5]	11	1[5]
D	D1		*High-temperature storage*[6]	14	—	7	—
	D2		*Continuous operation*	24	—	11	—
	D3		*High-humidity storage 85°C, 85% RH*[2,6]	24	—	11	—

Test cycle: Group A and B for every weekly lot, Group C every 13 weeks, Group D every 26 weeks

Notes
[1]*Electrical reject devices can be used in this test.*
[2]*These tests are performed on resin-sealed devices.*
[3]*This test takes 96 hours.*
[4]*These tests normally take 500 hours. But if no defects are found in the first 168 hours, the lot can be passed and the test may be terminated.*
[5]*These tests take 1000 hours.*
[6]*These tests take 3000 hours.*
[7]*This test takes 48 hours.*
[8]*These tests take 100 cycles.*

6.5.3 Occasional Tests

Occasional tests are performed on products whenever necessary. The tests are similar to periodic tests, but their details are specified by the QC/Reliability Engineering Division according to the purpose of the test.

6.6 Test Methods and Criteria

The reliability of Fujitsu ICs is assured by severe environmental and endurance testing. Test methods are usually based on Japan Industrial Standards (JIS), the standards of the Electronic Industrial Association of Japan (EIAJ), and MIL standards.

Reliability tests are performed for two reasons. Firstly, they check or guarantee the reliability of a type or a lot according to specified standards. Secondly, they are used to determine the failure rate or mode. The most appropriate test method is chosen for each test, and test results are processed in the most suitable manner. Fujitsu usually performs the tests listed in Tables 6–6, 6–7, and 6–8.

Table 6–6. Example of Reliability Testing

Test Items	MIL–STD–883	Condition
Resistance to soldering heat	—	260°C, 10s
Temperature cycling	1010 C	–65°C (30 min.) to 150°C (30 min.), 100 cycles
Thermal shock	1011 A	0°C (5 min.) to 100°C (5 min.), 100 cycles
Vibration, variable-frequency	2007 A	20 to 2,000Hz, 20G
Mechanical shock	2002 B	1,500G, 0.5ms
Constant acceleration	2001 E	30,000G, 1 min, Y_1 only
Fine leak[1]	1014 A_1	Using compressed helium 99.5 psig, 4 hrs.
Gross leak[1]	1014 C	Using fluorocarbon 75 psig, 1 hr., 125°C
Solderability	—	230°C, 5s
	2003	260°C, 5s
Lead fatigue	2004 B_2	0.25kgf, 90°, twice
PTHS/PTHB[2]	—	121°C, 2 atm
High-temperature storage	1008 C	150°C, 1,000 hrs.
Continuous operation	1005 A to D	125°C, 1,000 hrs.
High-humidity storage[2]	—	85°C,85%RH, 1,000 hrs.

Notes: 1 Applies to hermetic packages.
2 Applies to plastic packages.

Table 6–7. Example of Electrical Testing

Circuit classification	Characteristics	Bipolar	MOS
Gates	DC AC	V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{CC} (I_{EE}) Function	V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{DD} (I_{sub}) Function
Flip–flops	DC AC	V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{OH}, I_{CC} (I_{EE}) Function	V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{DD} (I_{sub}) Function
Shift registers	DC AC	V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{OH}, I_{CC} (I_{EE}) Function	V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{DD} (I_{sub}) Function
Memories	DC AC	V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{CC} (I_{EE}) Function	V_{OH}, V_{OL}, I_{IH}, I_{IL}, (I_{OH}),(I_{OL}) I_{DD} (I_{sub}) Function
Random–logic devices	DC AC	V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{CC} (I_{EE}) Function	V_{OH}, V_{OL}, I_{IH}, I_{IL}, (I_{OH}),(I_{OL}) I_{DD} (I_{sub}) Function
Analog devices	DC AC	V_{IO}, I_{IO}, I_I, V_{OM}, V_{OH},V_{OL}, A_V, K_{F2}, N_F	—

Table 6–8. Example of Electrical Criteria

Parameter	Limit value (in multiples of the absolute value)	
	Upper	Lower
V_{OH}	—	L x 0.9
V_{OL}	U x 1.1	—
I_{IH}	U x 2 (No leak: U x 1.1)	—
I_{IL}	U x 2 (Leak: U x 2	—
I_{OH} $I_{CC}(I_{EE})$ I_{CC} (I_{SUB})	U x 2 (Leak: U x 2	—

"U" and "L" stand for the upper and lower limits

Chapter 7 – Application Notes

Contents of This Chapter

March 1990
Edition 1.1

APPLICATION NOTE

FUJITSU

CMOS ASIC

Developing Test Patterns That Work with the Physical Tester

by J. Scott Runner

Fujitsu Microelectronics, Inc.

1

Introduction

This application note briefly describes the process of developing test patterns for the simulation and test of Fujitsu CMOS ASIC designs. This information supplements testing information found in the Design Manual for the appropriate Fujitsu CMOS ASIC technology.

Tests to be Created

Fujitsu supports the following five types of test

a. DC test

b. Dynamic function test

c. High impedance test (Z-function test)

d. Delay test (AC test)

e. Scan test (optional for certain Fujitsu technologies)

The DC test measures DC characteristics such as I_{DDS}, V_{OH}, I_{LL} and I_{LZ}, while the function test screens for manufacturing faults (metal and transistor faults, principally). The Z-function test augments the DC test and is required for circuits in which one or more enable signals from a 3-state buffer can be generated by logic deeper than one gate of complexity within the ASIC device. The delay test may be used to verify critical timing paths that are necessary for proper system operation.

Scan test methods are used to simplify the [process of testing for manufacturing defects traditionally uncovered by the function test. Automatic test generation is supported in conjunction with scan testing in the UHB/CG10 and AU/CG21 technologies as an option.

Overview of Test Vector Creation

For each set of test patterns defined as a test block, the customer must specify input states and output states (in either vector or wave format), and the timing of inputs and outputs (with bidirectionals being considered both an input and an output). Many designers rely on one of the Fujitsu-supported CAE workstations when generating test vectors, easing the burden of test pattern development. In these cases, the customer creates input stimuli for the workstation simulator, which then generates a print-on-change file containing the resulting output response and the associated input stimulus previously defined by the designer. The print-on-change file is converted by Fujitsu's workstation software into FTDL (Fujitsu Test Description Language), which is the accepted test pattern description format regardless of the method by which patterns are created.

Developing the Tester Timing Information

Whether or not the patterns are generated on the CAE workstation, it is necessary for the customer to generate in the FTDL file a Common Block file, containing administrative information and the test type, and a Test Block file, containing the timing information for all chip inputs and outputs by group (discussed further in the Design Manual). The definition of this overall timing is critical to the success of the test program itself. For example, input timing defines when input signals will transition, while output timing defines when outputs will be compared with their expected values or measured at a transition point.

The designer is responsible for specifying the following timing parameters for the Test Block, depending on the specific type of test:

a. Test cycle

b. Grouping of inputs and, if necessary, outputs and bidirectionals

c. Delay-to-transition (DT) time for each input group of non-return to zero (NRZ) signals

d. Propagation time (t_P) and pulsewidth (W_P) times for the positive-going pulse (PP) and negative-going pulse (NP) for each input group of return to zero (RTZ) signals

e.* Delay-to-strobe time (STB) point for each output group

f.* DT and STB times for bidirectionals

g.** T time in the SPATH statement for AC tests

*Specified in DC, function, and Z-function tests

**Applicable only to AC tests.

This timing is established for the entire test block and is invariant until another test block is invoked. Therefore, test pattern timing is periodic, that is, a group of inputs may only transition at the time specified in the Test Block, which is relative to the beginning of the test cycle. This delay to transition time for inputs is programmed for each input group with the t_P parameter in the FTDL INTIM or BUSTIM statement.

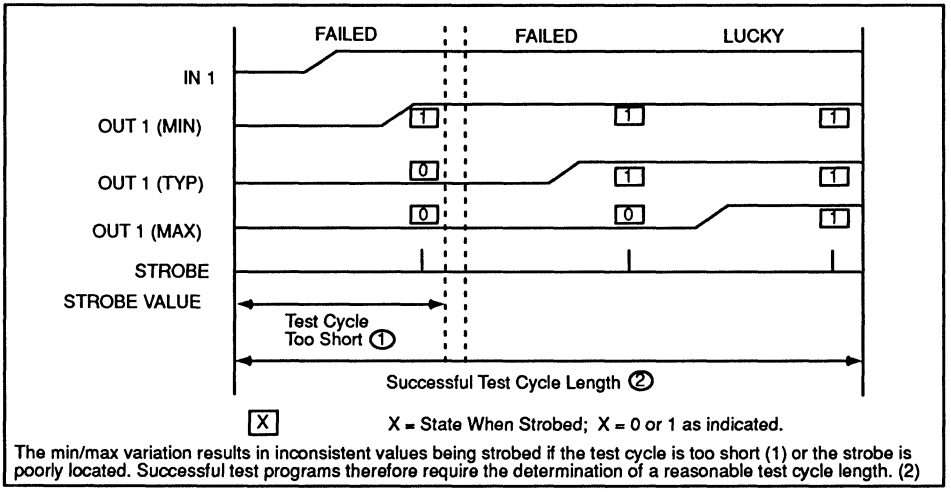
Similarly, common output groups are strobed, or sampled, periodically at a time determined by the test cycle and the delay-to-strobe time specified in the OUTTIM or BUSTIM statement, or the T_P parameter in the FTDL SPATH statement in the case of an AC test.

Determining Input and Output Timing Parameters

During the function test, outputs should stabilize before being strobed. Therefore, the minimum permissible test cycle programmed by the TIMING statement in the Test Block should be set with consideration of the maximum propagation delay from any input to any output, and the respective DT and STB times for those groups should be set far enough apart in time to assure that the outputs are stable under maximum

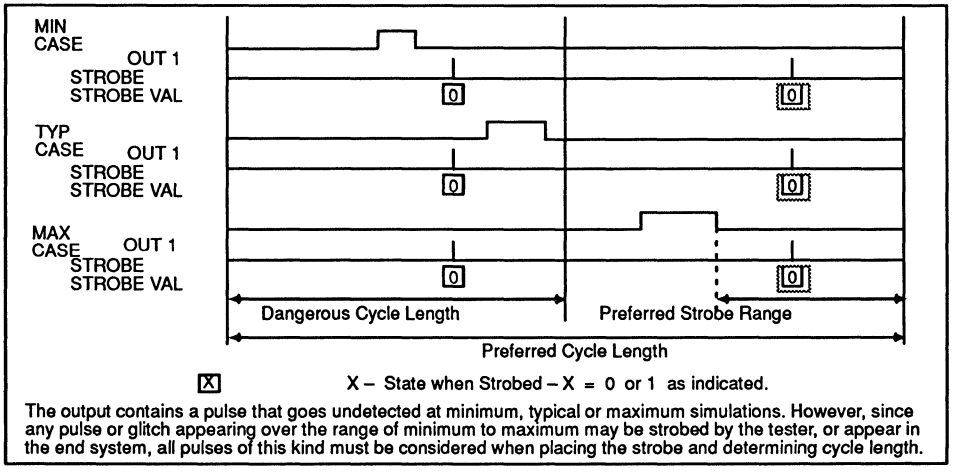
conditions. Similarly, if the output is strobed before the transition, it must be stable under minimum delay conditions.

Test patterns are required to be invariant over minimum and maximum delay conditions. This is verified in simulation by scaling the typical delays by multipliers representing process, temperature, and power supply variations. Similarly, the strobed or expected output states must be identical under typical, maximum, and minimum conditions. If a propagation delay from input to output is greater than the test cycle defined, output states may not fulfill this requirement (see Figure 1). Furthermore, designers should be careful that glitches or short pulses do not occur anywhere within this minimum/maximum window (see Figure 2).



The min/max variation results in inconsistent values being strobed if the test cycle is too short (1) or the strobe is poorly located. Successful test programs therefore require the determination of a reasonable test cycle length. (2)

Figure 1. Determining a Successful Test Cycle Length



The output contains a pulse that goes undetected at minimum, typical or maximum simulations. However, since any pulse or glitch appearing over the range of minimum to maximum may be strobed by the tester, or appear in the end system, all pulses of this kind must be considered when placing the strobe and determining cycle length.

Figure 2. Determining Preferred Cycle Length

Generating Functional Input Stimulus Given Test Pattern Timing

One issue that must be considered when determining test pattern timing is the relationship between input signals, such as clock/data pairs, which must satisfy set-up and hold times. Other considerations guiding the timing definition are dependent on the particular circuit being tested, and on restrictions imposed by the tester. These restrictions are published in the Summary of Test Data Restriction section of Fujitsu's Design Manuals.

Tester Skew and its Compensation of Test Timing

The designer must pay particular attention to the issue of tester skew when determining input and output timing for Test Blocks; otherwise, the timing will not correctly represent the behavior of the device under test. Tester skew, specified for each technology in the Summary of Test Data Restrictions, is a result of the variation in the time at which a given signal generator triggers a transition or a comparator measures an output state. Several timings are affected by this skew.

Input-to-Input Skew

For the purpose of estimating the skew between two signal generators, (one driving data and the other driving its clock, for example), the driver skew, linearity of clocks, clock-to-clock skew, and jitter are collectively called driver accuracy, denoted t_{DSKEW}.

In the case of data/clock pairs, the clocked data may fail either a set-up or hold time, depending on the direction of the skew. Therefore, when determining *DT* and t_p for data/clock pairs, the designer should adjust times to satisfy the following relationships (see Figure 3):

Set-up Time Criteria for Testing: $(t_p(CLOCK) - DT(DATA)) >= t_S(MIN) + 2 * t_{DSKEW}$

Hold Time Criteria for Testing: $(DT(DATA) - t_p(CLOCK)) >= t_H(MIN) + 2 * t_{DSKEW}$

Where $t_S(MIN)$ and $t_H(MIN)$ are the worst case set-up and hold times, respectively, sensitized from the internal circuit to the inputs, t_{DSKEW} is not directly specified in the Summary of Test Data Restriction; however, T_{ACC}, the overall system timing accuracy, is specified and can be substituted for t_{DSKEW} (see Section 7.2).

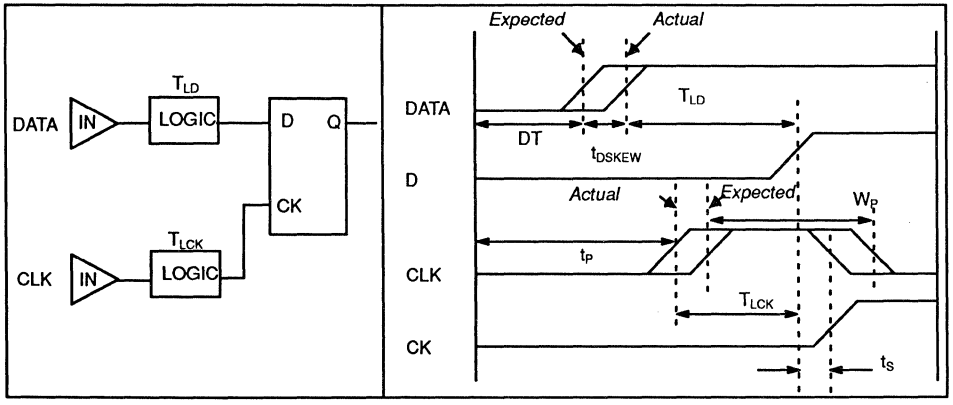


Figure 3. Input-to-Input Skew

Input-to-Output Skew

In addition to the skew incurred by the signal driver, skew is also introduced by the output comparator of the tester. This skew is dependent on the linearity of the strobe, pin-to-pin skew, skew between dual comparators, and the driver-to-comparator timing error. All factors are considered in the overall system timing accuracy, t_{ACC}, which in turn affects output timing as shown in Figure 4.

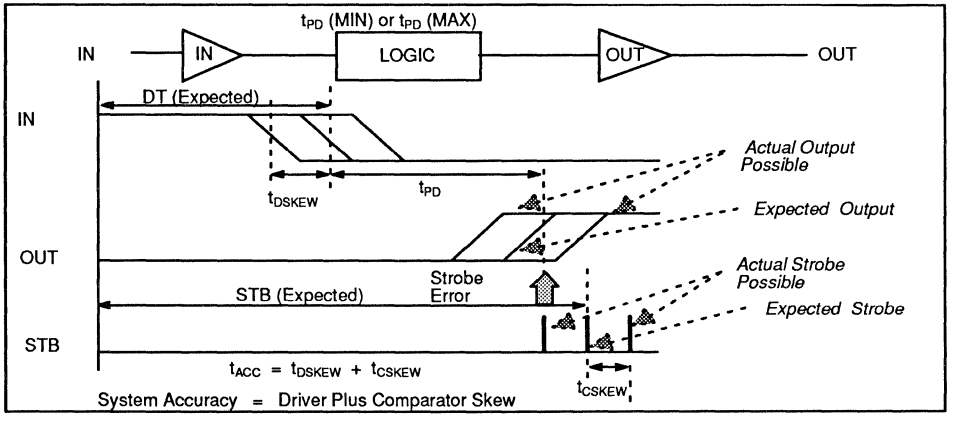


Figure 4. Input-to-Output Skew

Skew Effect on Input/Output Pairs - Minimum Delay Case

The *STB* (or *T* parameter in the SPATH statement) should expect an output transition at a time relative to the stimulated input transition dictated by

$$(STB - DT) >= t_{PD(MIN)} - t_{ACC}$$

where *STB* is the strobe point of the output under consideration, *DT* is the *DT* time of the stimulating input of interest, and $t_{PD(MIN)}$ is the minimum propagation delay from this input to the strobed (or measured) output. In the case of the AC test, the quantity (*STB - DT*) should be replaced by the minimum *T* parameter in the SPATH statement. Note that if the path delay spans a test cycle boundary, *STB* should be set to *STB* plus the test cycle period.

Skew Effect on Input/Output Pairs - Maximum Delay Case

The complementary case occurs for maximum delay measurements, as described by

$$(STB - DT) <= t_{pd(MAX)}) + t_{ACC}$$

Note that these guidelines regarding the specification of test data timing as affected by tester skew apply to DC and Z-function tests as well. In these cases, the same rules apply as for the function test.

Again, for the specific values of t_{ACC}, and t_{DSKEW}, please refer to the Summary of Test Data Restrictions in the Fujitsu Design Manual for the appropriate technology. A designer interested in a methodical approach to the generation and verification of a good set of test vectors must consider the tester hardware on which it is running. Fujitsu has simplified designer responsibility by providing this information as part of the Test Block Information.

However, a lack of implementation and careful analysis of the timing characteristics of the circuit may result in a poor or unfeasible test, resulting in schedule delays or reduced device yield. Therefore, plan a test approach early, design for testability, and consider the effect and operation of the physical tester.

March 1990
Edition 1.1

FUJITSU

APPLICATION NOTE

ASIC Packaging Information

Selecting the Best Package for Your ASIC Design

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1.0 Introduction

The widely varying degrees of complexity (gate count) of Fujitsu's CMOS and BiCMOS devices and the flexibility of their I/O configurations combine to produce devices that take advantage of the broad selection of packages available from Fujitsu. However, the requirements for package selection go far beyond pin count as the sole determinant of the best package. Selection issues include surface mount versus through-hole, plastic versus ceramic, and exotic versus conventional packaging. In fact, Fujitsu offers over 100 packages and 1000 package-die combinations from which to choose. Compounding the selection problem is the effect of increasingly faster outputs coupled with higher drive and wider bus structure, resulting in greater numbers of simultaneously switching outputs (and thereby greater amounts of noise).

The result is that designers are finding ASIC packaging implementation to be an increasingly complex task. This application note provides information about ASIC packaging that is meant to simplify the designer's task. It provides designers with a review of the various Fujitsu packages and their electrical, thermal, and mechanical characteristics, as well as some problem-solving strategies for their use. Sections 2.0 and 3.0 address system requirements and package availability; Sections 4.0 and 5.0 discuss noise and thermal issues.

2.0 How System Requirements Affect Package Choice

Section 2.0 presents considerations involved in the selection of packages from a system designer's perspective. Table 1 lists issues a designer must consider when determining the optimal packaging for an ASIC design.

Table 1. Considerations for Package Selection

Manufacturing and Cost	**Speed Requirements**
Board Integration	Package and Interconnect Delays
Double-sided Component Mounting	The Effect of Package on Noise
Number of Packages	Thermal Considerations
Package Outline Area	
Power Density Limitations	
Producibility	**Quality**
Board Layout	Package Quality and Reliability
Package Construction	Number of Devices
Packaging Complexity	Noise
Manufacturing Flow	Thermal Considerations

2.1 Manufacturing and Cost

The manufacturing-related factors discussed below, although not directly related to the design of the device or the number of power and ground pins it requires, are nonetheless important in the choice of an ASIC package.

2.1.1 Board Area

One of the most important issues is the board area consumed by a circuit. Some of the factors affecting overall board density are:

Integration (gates per square inch of board)

Double-sided mounting capability (integration)

Number of packages

Package outline area

Additional board space required (for spacing, resistors, capacitors, probe areas, etc.)

Power density area (discussed in Section 5.0)

The critical issue in board area reduction, however, is overall integration. For example, surface mount devices (SMDs) can be densely mounted on both sides of the board, making them ideal for systems demanding high package integration. But a large design integrated into a few very large Sea-of-Gates arrays, even if packaged in large, through-hole packages, may well consume less board space than the same design using surface mount plastic J-leaded chip carriers (PLCCs). The PLCC version would require more space because the PLCCs, although small in outline, cannot house as large a die and therefore require the design to be partitioned into a greater number of devices.

Figure 1 illustrates the board area taken up by the outline of each kind of package Fujitsu offers, excluding any area around the package necessary for spacing, decoupling capacitors, series damping resistors, or solder pads.

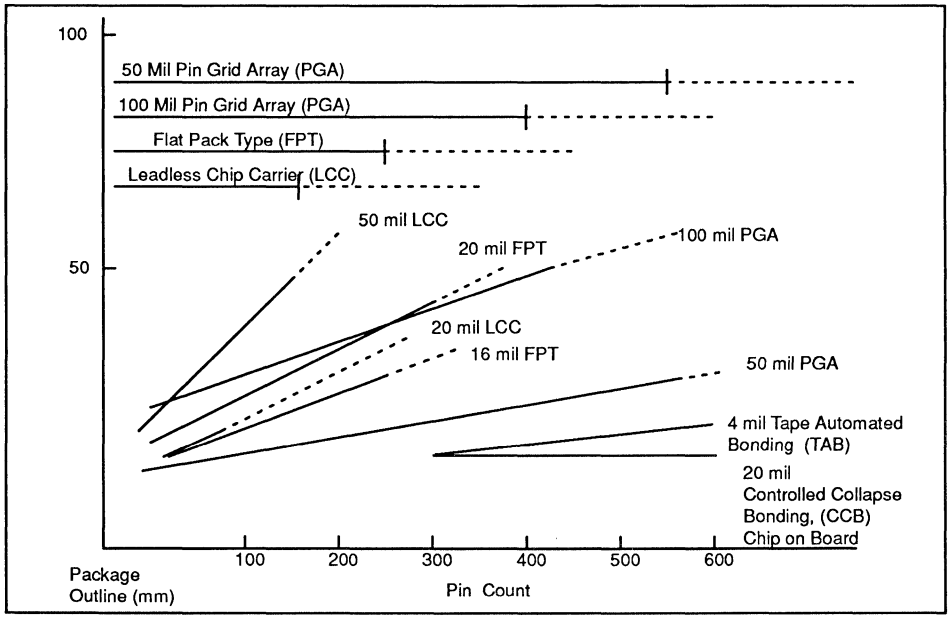


Figure 1. Package Size versus Pin Count

2.1.2 Board Layout

Restrictions in board layout or construction must be identified and resolved early in the design process. For example, a design containing large buses (16 bits or 32 bits or more) must be split up to avoid too high a concentration of simultaneously switching outputs per ground pin. Splitting up the buses, however, may result in variations in signal trace length and require extra care in routing. Similarly, flatpacks, a form of SMDs, are a convenient way to support high pin counts in relatively inexpensive plastic packages. However, with pin pitches as narrow as 15 mils, they demand extremely accurate positioning of solder pads. Dense PGAs, on the other hand, provide a spacious 100-mil pin separation, but because of the number of rows of pins, normally require a large number of board layers.

2.2 Producibility

Though some unusual packages may appear to promise ultra-high speed or dense integration or minimized component/board cost, the designer must always keep manufacturability in mind. The cost of a system is only partially dependent on materials and labor costs per unit; it is also highly dependent on the manufacturing yield of the end product. Therefore, design and production engineers must jointly consider the choice of package in order to guarantee that the chosen package conforms to existing (or purchasable) manufacturing equipment and that the manufacturing process can meet yield goals.

2.3 Speed Requirements

The speed requirements of a system strongly affect package choice. If the interconnect lengths in the system (both inter- and intra-board) can be reduced, system speed may be increased. Reducing interconnect lengths may involve reducing the required number of packages, choosing packages with smaller outlines, changing to double-sided, modular, or piggy-backed mounting, using small form factors, reorganizing boards, and even changing the number of metal routing layers of the board. See Figure 2.

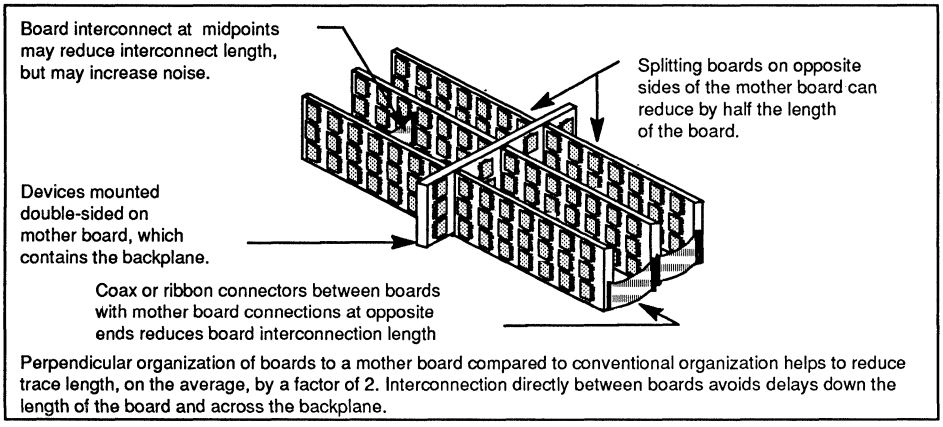


Figure 2. Minimizing Interconnect Length

2.3.1 The Effect of Noise on Speed

There are various sources of noise that can affect an integrated circuit (IC), each with its own effect; all forms of noise influence signal speed, quality, and consequently, system reliability. Certain types of noise arise between a chip I/O and ground or power, while other forms of noise are coupled to the power rails and influence system power and ground lines, propagating noise throughout the entire system. Noise appears to an input buffer (receiver) relative to the receiver's ground. Any noise on this referenced signal is superimposed onto the incoming signal itself, as shown in Figure 3. The V_{IH} or input threshold level of the receiver indicates when the input will switch, if the signal is stable at that level. Therefore, although the input voltage ordinarily would switch 4 ns after the driver switches, when the signal first crosses the threshold, the designer must assume it will not switch until it is stable; in this case at 8 ns, producing a loss of 4 ns due to noise.

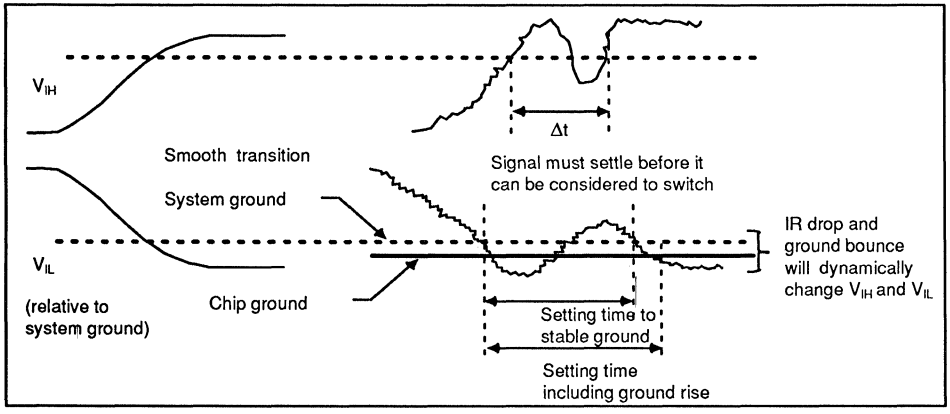


Figure 3. Impact of Noise on Speed

2.3.2 Controlling Noise through Package Selection

Each form of noise is dependent not only on current or its first derivative with respect to time, but also on the real and imaginary components of impedance: resistance (R), inductance (L), and capacitance (C). One solution to noise can be to minimize the package L and R and to locate high drive pins where they will minimize L and R.

2.3.3 The Effect of Thermal Characteristics on Speed

The speed performance of a CMOS or BiCMOS circuit degrades with temperature rise. Therefore, in very high speed systems, it is sometimes necessary to reduce the junction temperature (Tj) or die temperature as a way to improve speed. Certain packages offer better cooling properties than others, making them more suitable for high speed systems. Thermal issues are discussed in Section 5.0.

2.4 Quality

Reliability refers to the defects or failures that appear during the lifetime of a device. Quality, on the other hand, refers to the frequency of occurrence of defects or faults in a device as a result of the manufacturing process. Quality defects are revealed by testing immediately after manufacturing, while reliability defects are revealed by special long-term or intensive test sequences or by time.

2.4.1 How Package Type Affects Quality Testing

Conventional (through-hole) packages lend themselves to simplified testing because it is easy to access the leads in order to force a state (1 or 0) at a node and/or to observe the state of the node. These tests are performed with board-level in-circuit or functional testers. Such tests facilitate the manufacture of high-quality systems by ensuring proper connectivity and function.

Surface mount devices, however, generally provide poor probe access, and are known to occasionally possess faulty joints that make temporary connections during probe. Through-hole packages also have occasional bad solder joints, although their node access is fairly good.

2.4.2 How Device Integration Affects Reliability

Total system reliability is related to the reliability of the individual devices and to their configurations. Systems may be configured as a series in which all devices are interdependent, in which case any one failure will cause overall system failure, or they may be configured in parallel, in which case all devices must fail for the system to fail. Parallel configuration is used in redundant or fault-tolerant systems.

The reliability of a system also depends on the reliability of the devices that comprise the system. The long-term reliability of a single device is defined as an inverse natural log function in a variable lambda, which is the failure rate of the device in the region of lifetime operation characterized by a constant failure rate. In the first hours of a device's life (the infant mortality period), the failure rate declines. The majority of a device's life is characterized by random failures (expressed as lambda), and the end of a device's life exhibits an increasing failure rate. Today's ICs, however, are designed so that wearout does not even begin to occur for at least several hundred years, and can be considered never to occur.

To understand how the partitioning of a system into circuits can affect the reliability of a system, consider a system in which N components are configured in series. Although the density of ASIC devices has increased by two orders of magnitude in the last decade, the reliability of the devices has remained roughly constant. Therefore, it can be assumed that the failure rate of each of the components is constant. The reliability of systems and subsystems in which components are series-dependent is the product of the individual reliability terms for each component. The reliability function of the system just described is therefore:

$$R(t)sys = R(t)1 * R(t)2 * ...R(t)N$$

where

$R(t)N = e - N\lambda t$, t is the independent variable time, and λ is lambda, the failure rate.

Since all components have the same failure rate, the reliability function of the system is:

$$R(t)sys = e - N\lambda t$$

Because the number of packages affects the reliability more than the integration factor does, a designer's goal in constructing a reliable system should be to maximize integration and thereby reduce part count.

The disadvantage is that increased integration may in turn increase the package pin count, requiring a more complex package, which usually costs more than a simpler, smaller package. Additionally, the larger die sizes cost slightly more per gate than the smaller ones, although the total non-recurring engineering charges (NRE) would typically be lower.

2.4.3 How Noise Affects Reliability

Even when Schmitt trigger input buffers are used to receive clock signals, noise may go beyond the hysteresis value of the input buffer and cause a counter to be incorrectly clocked or other circuit malfunction. Noise is in this sense a threat to reliability as well as to speed and must be considered in the package choice as well.

2.4.4 How Thermal Issues Affect Reliability

While the junction temperature of a device affects its speed, it also affects reliability expressed as mean time between failures (MTBF) or the mean time a device will operate in a given environment before failure occurs. Figure 6–4 in the previous chapter, Quality and Reliablility, illustrates this concept by plotting life test failures as a function of junction temperature. System reliability goals, then, restrict the desired maximum junction temperature in a manner that affects the choice of package according to its thermal characteristics, the chosen type of system thermal management (cooling), and the maximum allowable device power dissipation.

2.4.5 How Package Material Affects Reliability

The different materials used in package construction each have distinct thermal and mechanical properties. The most common materials and their characteristics are listed in Table 2 below.

Table 2. Package Material Characteristics

Package Type	Body Material	Thermal Coefficient of Expansion (ppm/5C)	Thermal Conductivity (W/m * 5C)	Dielectric Constant (K)
Ceramic	$Al_2 O_3$ (Alumina)	7.0	20	10
Plastic PGAs	Epoxy Fiberglass	14 – 18	0.16	4.5 – 5.0
Other plastic packages (DIP, PLCC, Flatpack)	Polyimide Epoxy	15 – 18	0.38	4.5 – 5.0

To better understand the different characteristics of plastic and ceramic packages, it is helpful to know something about the way they are constructed. Packages provide electrical connection from the IC to the system and isolate the device from destructive elements of the environment. The choice of materials and construction of a package affect its final dimensions, thermal characteristics, and electrical characteristics, as well as device reliability. Fujitsu carefully determines the most appropriate manufacturing methods for a given package and then performs extensive qualification tests to determine its success.

The largest part of the package is the body, which houses the die. The die may be affixed to a lead frame, which physically supports the die and provides the leads that electrically connect the die to the system by means of bonding wires or tab leads. Alternatively, the die may be supported by a cavity on the body of the package or attached to the bottom of the body by a chip carrier.

The die is attached to the surface of the lead frame or to the metallized surface of the cavity or carrier with gold or silver paste, or eutectic. After the die is attached to the lead frame, cavity, or carrier and the bonding pads are bonded to the leads, the assembly is encapsulated. In plastic packages, an epoxy resin is molded around the assembly. In ceramic packages, a cap is sealed onto the lower part of the body or carrier using a frit glass or metal seal (the metal seal has a higher melting temperature than the glass). A solder seal can be used if the cap is metal.

To ensure that the device is completely isolated from its environment, the surface of the die is then coated with glass (SiO_2) and then polyimide or other coating that prevents gas and moisture from coming in contact with the surface of the die. Figure 4 shows a frontal cross section of the structure of a PLCC package; Figure 5 provides a top view.

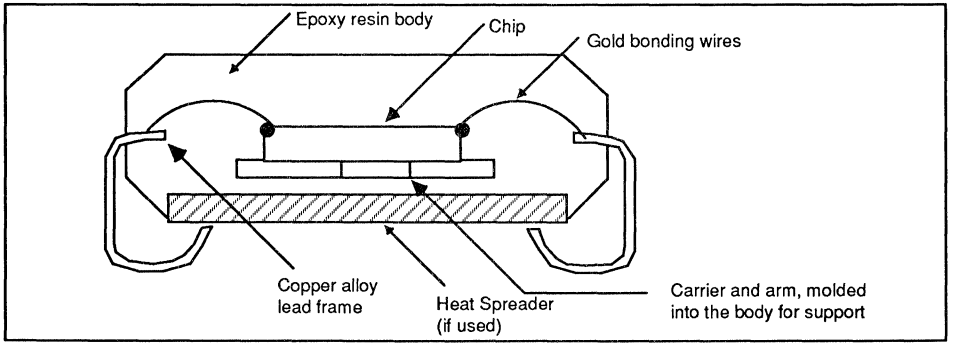


Figure 4. PLCC Package Construction (Front View)

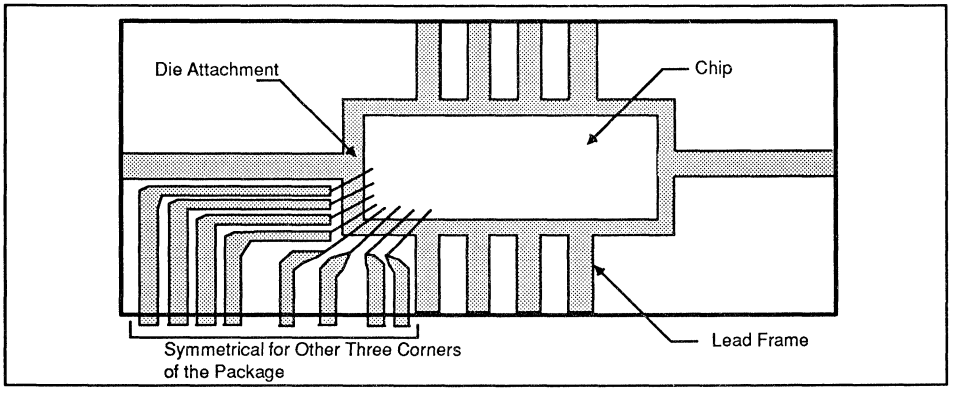


Figure 5. PLCC Lead Frame Construction (Top View)

Each of the various packaging methods has its advantages and disadvantages; for instance each body type and each type of seal has a different maximum case temperature. While plastic packages can tolerate tem-

peratures up to 125°C and high humidity levels with outstanding reliability, ceramic packages are the most reliable for harsh extremes of cold.

Each package type also responds differently to the thermal environment of the board to which the device is attached. Heat can cause thermal stress on the device when different materials expand at different rates, a particularly important factor when surface mount packages are involved.

Different packages also exhibit different electrical characteristics. As the speed and gate densities of CMOS devices rise, the avoidance of electrical parasitics in the form of package delays and noise becomes an increasingly important factor in choosing a package type.

Fujitsu's plastic PGA provides a good example of the tradeoffs involved in package construction. In 1986, Fujitsu introduced the plastic version of its ceramic PGA. The plastic configuration proved to have several advantages over the ceramic version. The body is formed from glass epoxy (VG-10) with an aluminum cap and an epoxy resin sealer. This combination of materials has the same rate of expansion as the PC boards onto which it is mounted; it is also less expensive than ceramic.

Ceramic PGAs have a hermetic seal of solder between the metal lid and the cavity, but plastic PGAs are sealed by filling the cavity with epoxy resin to form an inner seal, then placing a resin sheet over the inner seal to form an outer seal, and then securing an aluminum cap over the outer seal. The aluminum cap provides the necessary rigidity to support the fragile glass epoxy, as well as improving the thermal conductivity of the package.

Connections from the bonding wires to the pins are provided by copper traces designed to minimize mutual and self inductance. Because the plastic PGA is a large package, however, and generally houses a large die, the thermal coefficient of expansion (TCE) difference between the die and the cavity can exert stress on the bonding wires and the die attach. Table 3 lists the package types discussed in this section and the materials used to construct each type.

Table 3. Fujitsu Package Types

Package Type	Lead frame/ Metallization	Lead/Pad	Lead Finish	Cap Material	Body Material	Seal Material
Plastic DIP	Ie-Ni or Cu Alloy Lead frame	Same	Solder Dipped	———	Resin	Resin
Ceramic DIP	Tungsten Metallization	Kovar or Fe–Ni	Au/Sn Plated	Metal or Aluminum	Laminated Alumina	Solder, Glass Frit
CERDIP	Fe-Ni Alloy Lead frame	Fe-Ni	Sn Plated	Alumina	Alumina	Glass Frit
Plastic Flatpack	Fe-Ni Alloy Lead frame	Same	Sn Plated	———	Resin	Resin
Ceramic Flatpack	Fe-Ni or Kovar Lead frame	Same	Au Plated	Metal or Aluminum	Laminated Alumina	Solder or Glass Frit
Cerpack	Fe-Ni Alloy Lead frame	Same	Sn Plated and Solder Dipped	Alumina	Alumina	Glass Frit
Plastic PGA	Cu Conductor on Epoxy glass	Kovar	Ni Plated and Solder Dipped	Aluminum	Epoxy Glass	Resin
Ceramic PGA	Tungsten Metallization	Kovar	Au Plated and Solder Dipped	Metal or Alumina	Laminated Alumina	Glass Frit
Plastic LCC	Cu Alloy Lead frame	Same	Solder Plated	———	Resin	Resin
Ceramic LCC	Tungsten Metallization	Tungsten Metal Pad	Au Plated	Metal or Alumina	Laminated Alumina	Solder, Glass Frit

Note: All above packages are hermetic. Alumina is a ceramic. Solder is PbSn. Fe-Ni is ferrous (iron) nickel. Kovar is an alloy of cobalt, iron, and nickel. Bonding wires are gold in the case of molded packages (epoxy resin PLCCs, DIPs, Flatpacks) and gold or aluminum for the other cases. Cerpack is the ceramic flatpack equivalent of CERDIP.

2.4.6 Package Qualification to Ensure Reliability

Fujitsu performs extensive six-month minimum qualification tests for every package-die combination. After such qualification is performed, the package die-combination is added to a package matrix in the Design Manual for the appropriate technology. The designer can be assured that Fujitsu has considered the issues presented here, as well as others, when releasing an approved package-die combination.

3.0 Package Types

Very large scale integration (VLSI) ASIC devices are supported by a wide variety of packages, of both surface mount and through-hole types. Through-hole devices, including DIPs and PGAs, are a proven technology and are supported by widely available production equipment. The pins of these devices are inserted though holes in the PC board to form electrical contact with traces (usually copper) which are embedded in the board or applied to the surface and are routed to drilled pin holes. Solder applied by reflow or wave technique then completes the connection.

3.1 Through-hole Packages

3.1.1 Dual In-line Packages (DIPs)

DIPs have two rows of pins spaced 300 mils to 900 mils apart, with a pin spacing of 70 to 100 mils. Since the length of the package increases as each pair of pins is added, the size of a DIP tends to be unmanageable over 64 pins. The lead width and length of a DIP varies widely, causing variation in the input and output response of the device and thus, skew. Also, due to their high pin inductance, DIPs tend to be noisy, the degree of noise being a function of the location of outputs and sensitive inputs.

The DIP is relatively simple for manufacturing to support, thanks to a large installed base of well-proven equipment and is one of the least expensive packages available. Furthermore, DIPs, being well established, come in many JEDEC-approved options (see JEDEC Standard 95), and are available in both ceramic and plastic cases.

3.1.2 Pin Grid Arrays (PGAs)

Although PGAs are usually through-hole (Fujitsu also offers SMD versions), they differ from DIPs in that pins are arranged in rows on all four sides. While the pin spacing is usually the same as for DIPs (70 to 100 mils), nesting the pins in rows permits a larger number of pins to be contained within a smaller area allowing PGAs to support high pin counts of more than 300 pins. See Table 4 for a list of Fujitsu PGAs.

Table 4. PGAs Available from Fujitsu

Package	Type	Construction	Number of Pins
PGA – 64C, 64P	Through-hole	Ceramic/Plastic	64
PGA – 88C, 88P	Through-hole	Ceramic/Plastic	88
PGA – 135C, 135P	Through-hole	Ceramic/Plastic	135
PGA – 179C, 179P	Through-hole	Ceramic/Plastic	179
PGA – 208C	Through-hole	Ceramic	208
PGA – 256C	Through-hole	Ceramic	256
PGA – 256C	Surface	Ceramic	256
PGA – 299C	Through-hole	Ceramic	299
PGA – 321C	Staggered	Ceramic	321
PGA – 361C	Staggered	Ceramic	361
PGA – 401C	Staggered	Ceramic	401

Through-hole = 100 mil through–hole
Surface = 50 mil surface mount PGA
Staggered = 71 mil staggered PGA

Although PGAs are generally easy to support from a manufacturing standpoint, they may also raise problems. The PC board designer may find it difficult to route signals to and from the inner rows of the PGA, since it has only 100 mils spacing between pins. Additionally, the large cluster of pins confined to a small area tends to create trace congestion and may require boards of up to six layers to be used to support the PGAs. Manufacturing engineers find the solder joints for the pins of inner rows are difficult to inspect, forcing them to rely on the results of "bed-of-nails" in-circuit testers, or sophisticated inspection techniques such as x-ray or infrared.

Although more expensive than DIPs, PGAs have come down in cost with the introduction of plastic PGAs (previous PGAs were usually ceramic). These plastic PGAs are generally constructed of G-10 glass-type epoxy with the traces routed through the epoxy the way they are routed on a typical PC board. (The electrical characteristics are, of course, tightly controlled). Although the reliability of plastic PGAs was initially in question, Fujitsu built them using special construction techniques employing metal lids and heat spreaders to provide rigidity and heat dissipation. Their excellent reliability history up to this point seems to indicate that plastic PGAs will continue to be popular. The widely-used epoxy thick-film substrate, once a quality and reliability concern, has the same TCE as the most common PC boards, and reduces the stress of expansion and contraction that is typically a concern with larger packages. (The distance of expansion per unit change in temperature increases with the size of the package.)

1

3.1.3 Advances in Through-hole Packaging at Fujitsu

The demand for high pin-count plastic packages cannot be satisfied by merely increasing the number of pins a package supports. As size increases, so do the problems inherent in these lower-cost packages. These problems include greater lead inductance and thermal expansion mismatch between die and package. Ceramic flatpacks can support more pins than plastic packages, but they require special manufacturing capabilities, and are difficult to work with since they may have pin pitches down to 10 mils. Surface mount PGAs (discussed in Section 3.2) can support a large number of pins, but require difficult manufacturing processes.

Fujitsu's answer to these problems, for the customer who wants high levels of integration without the need for exotic manufacturing methods, is the staggered PGA, shown in Figure 6.

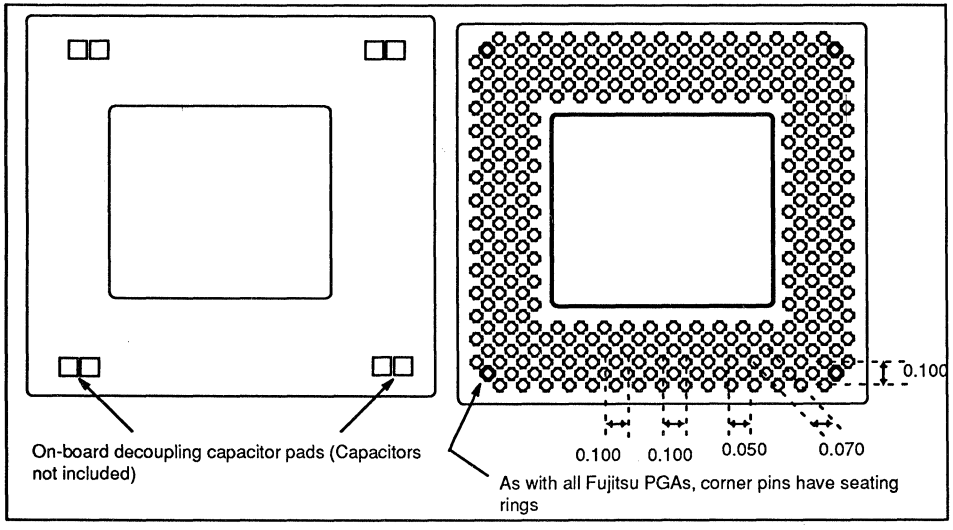


Figure 6. 321-Pin Ceramic Pin Grid Array

Figure 7 illustrates the footprint of the staggered PGA and the method for routing traces through the leads. Note that the routing is oblique, with the traces offset 45 degrees compared to traditional routing. At this angle, the lead spacing is 71 mils, providing the trace density available with standard through-hole devices, while reducing the package outline by approximately 40 percent.

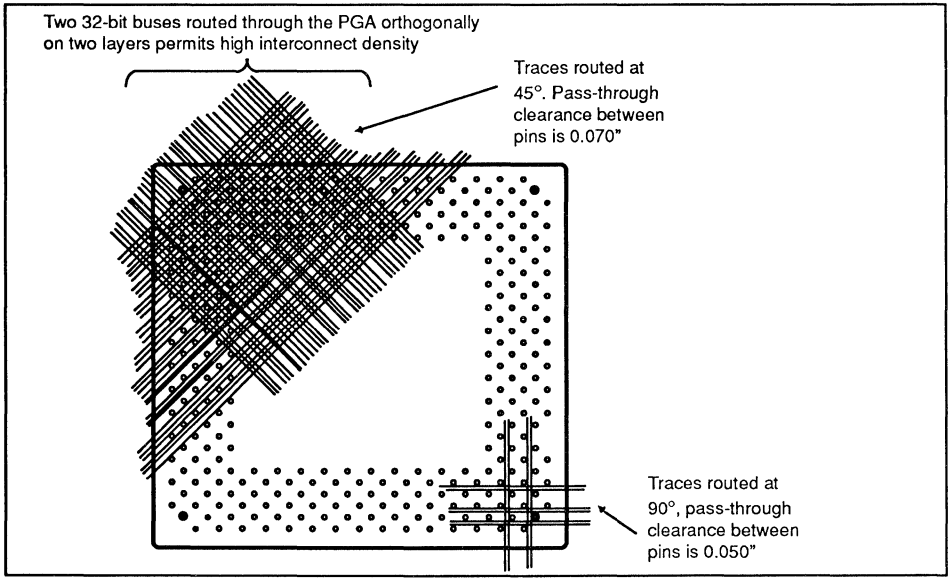


Figure 7. Staggered Pin Grid Array Routing

The lead configuration of a package affects the pin assignment of the ASIC device. For example, Figure 7 shows a situation in which a 32-bit address bus and a 32-bit data bus are routed through the device, with one offset 90 degrees from the other. If you assign consecutive bit significance to the bus, you will notice that the resulting pinout is quite different from an equivalent circuit packaged in a traditional orthogonal PGA. High drive buses can still be distributed around the ground pins, but the associated pads are not concentrated in one specific area of the die, reducing the concentration of SSOs, thereby reducing signal noise.

3.2 Surface Mount Devices (SMDs)

The demands of military applications, space-constrained systems, and boards containing large numbers of memory devices were initially responsible for the development of surface mount technology (SMT). However, the accelerated push for physically reduced systems, the appearance of higher pin count ASICs, and the cost of pin grid arrays have encouraged many more designers to consider surface mount options. Easing the strain of the migration to SMT is the broader availability of pick and place, vapor phase soldering, and other necessary SMT equipment, as well as the availability of SMDs for an increasing percentage of devices on the boards. SMT for VLSI is gaining momentum due to the smaller board area consumption, smaller profile, and proven reliability.

3.2.1 Flatpacks

Plastic flatpacks have been popular for years with manufacturers of peripherals in which the board area is constrained and height is restricted. And recently, the low cost of flatpacks (in plastic) has made them an attractive alternate to PGAs and even to DIPs in cases of higher pin count. As the following figures show,

flatpacks come in several lead type and location configurations. Figure 8a illustrates a small outline integrated circuit (SOIC), with gullwing leads on two sides, Figure 8b illustrates a quad flatpack (QFPT) with gullwing leads on four sides. Flatpacks with axial leads require special assembly, and are generally used only for ECL circuits in which leads may have to be trimmed and formed to tune impedance.

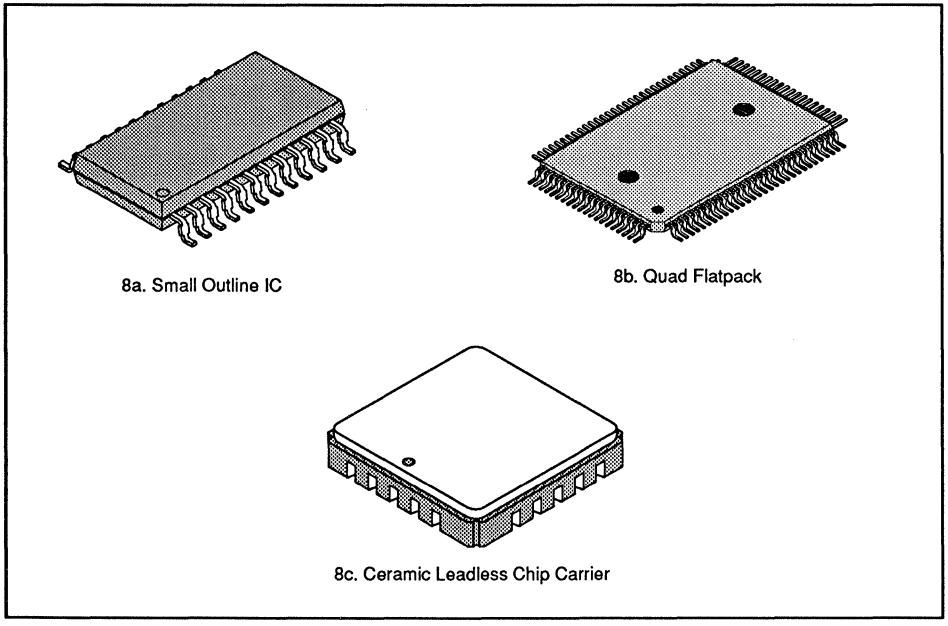


Figure 8. Flatpack Configurations

Because flatpacks feature pin pitches (pin spacing from center to center) down to 10 mils, they can support high pin counts within a small board area. However, the narrow pin spacing means that accuracy in device placement, pad size and placement, and solder paste application tolerance are all more critical. PC board designers also need to determine whether the true package dimensions are in metric or English dimensions, and, when converting between the systems of measure, ensure that enough precision is maintained so that pins on the end of large packages won't roll off due to inaccuracies in pad location.

Probing devices with fine pin pitches can be difficult because the pins do not pierce the bottom of the board, and if probes are attached to the leads, they can easily slip off and short adjacent leads.

3.2.2 Leadless Chip Carriers (LCCs)

Ceramic leadless chip carriers (CLCCs), such as the example shown in Figure 8c, have a long history in surface mount packaging. Ceramic packages perform well in high temperature environments, explaining their popularity in military applications. The term "chip carrier" comes from the process of mounting the die directly to a thick-film chip carrier, which also has pads for external connection on the opposite side of the substrate. This configuration differs from that of the PGA, in which the die is housed in the cavity of the package, or the flatpack, in which the die is held by the lead frame and molded with the package. CLCCs are available in pad counts ranging from 28 to 84 and beyond.

Pads, not leads, are located on the bottom of the carrier and are generally spaced at a 40-mil pitch (standard). Solder paste is applied to the pads on the board to which the device will be mounted, usually by screen printing, and the board is then vapor phase or infrared reflow soldered. Because the pads are lo-

cated beneath the package, they are typically very difficult to probe and are subject to manufacturing defects such as solder voiding (gas bubbles in solder formed during reflow).

The most challenging problem inherent to LCC devices relates to TCE mismatch between the chip carrier and the board to which it is mounted. As the temperature of boards and packages rises, the materials expand at different rates. This difference translates to mechanical shear force at the solder joint. This force temporarily deforms the leads of PLCCs and flatpacks, but CLCCs have no leads. Consequently, the force is directed at the solder joint, tending to promote thermal fractures, (shown in Figure 9).

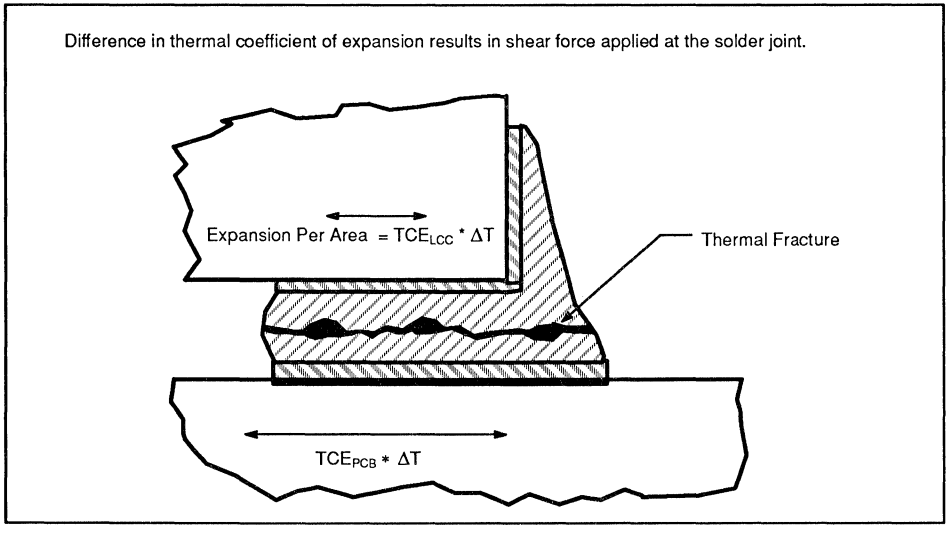


Figure 9. Defect Caused by Difference in Thermal Coefficient of Expansion

Even though CLCC SMDs cost more than equivalent plastic packages, their resistance to high temperatures, availability in hermetically sealed (moisture resistant) packages, and low profile of the CLCC SMDs make them very useful for applications in extreme environments. The TCE mismatch problem affecting LCCs is less severe when they are mounted to ceramic hybrids or PC boards, making their disadvantages acceptable in many circumstances.

3.2.3 Plastic J-leaded Chip Carriers (PLCCs)

If cost and TCE mismatch are a significant deterrent to the use of LCCs, leaded chip carriers may be more attractive. Though the chip is still mounted on a carrier (see Figure 10), the electrical connections of PLCCs are through pins that deform to absorb the TCE-induced thermal stress. Furthermore, while solvents used in the post-soldering cleaning process may be retained beneath the low profile of the CLCC and flatpack, the board offset of the PLCC permits it to remain free of these contaminants. In addition, the LCC in a plastic package costs less than the equivalent CLCC.

When more pins are necessary (in the 44-, 68-, 84-pin packages necessary for ASICs), the LCC is called a PLCC. It is also available in a ceramic body version; both are available in pin counts of 28 to 84 and beyond.

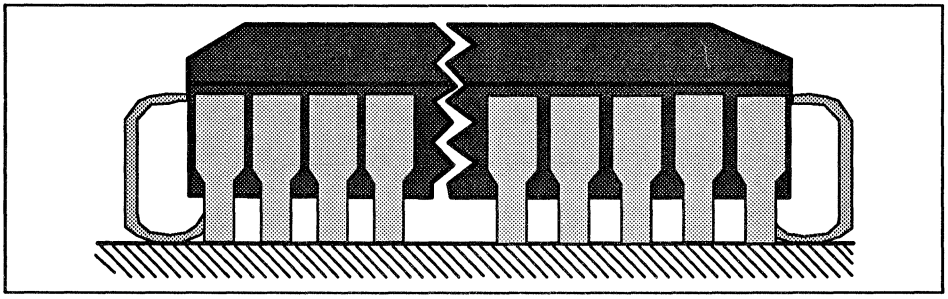


Figure 10. PLCC Package

This package is termed a small outline J-lead (SOJ) when its bent leads are located on only two sides (Figure 11). The leads are bent into the form of a J in order to permit it to be placed on top of the solder pad.

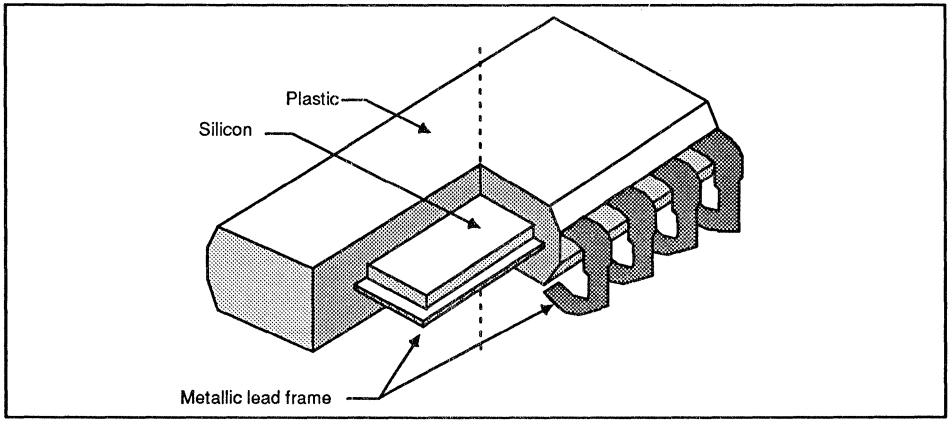


Figure 11. Cross-Section of a Plastic Small-Outline J-lead Package

On the list of drawbacks of the PLCC is its limited ability to withstand high case temperatures, and its unavailability as a hermetic package. It is nevertheless very well suited for industrial and commercial environments. With a 50-mil pin pitch and only slightly greater height and width, the profile of the PLCC is nearly equivalent to the corresponding CLCC.

3.2.4 Advances In Surface Mounted Packages

While smaller process geometries themselves have few disadvantages, the associated increase in integration, speed, power, and particularly pin count place heavy burdens on packaging. The greatest challenges CMOS faces is supporting pin counts in excess of 300 in packages with low lead inductance, capacitance, and resistance.

To respond to these demands, Fujitsu has developed a clever solution in packaging to obtain the highest average pin density per board area yet achieved. This is accomplished with surface mount PGAs, which rely on narrow pin pitch (50 and even 25 mils) in a dense grid of multiple rows of pins. Since through-hole packages cannot effectively support pin pitches narrower than 70 mils, these PGAs must be surface mounted, though they still possess pins (see Figure 12).

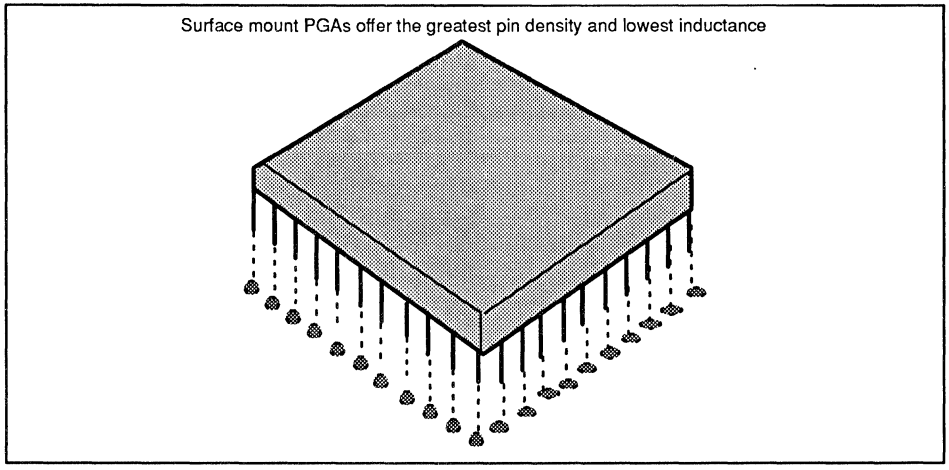


Figure 12. Surface Mount PGA

The surface mount technology also permits traces to run beneath the package leads, increasing available trace density. Figure 13 shows the solder pad design required by these high-pin-density packages.

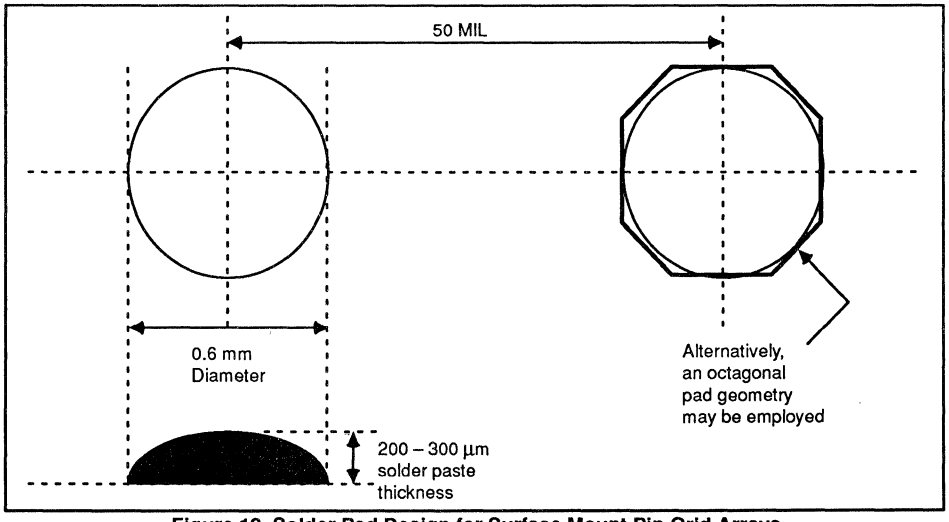


Figure 13. Solder Pad Design for Surface Mount Pin Grid Arrays

Table 5 provides an item-by-item comparison between PGAs, surface mount PGAs, and flatpacks of similar pin counts.

Table 5. Comparison of Critical Features

PACKAGE	TYPE	PIN PITCH	OUTLINE (MAX)	PIN DENSITY (Pins Per Sq Inch)
FPT – 160	Surface	25 mil	1.276" x 1.276" (1.63 sq In)	98
PGA – 256	Through	100 mil	2" x 2" (4 sq In)	64
PGA – 256	Surface	50 mil	1" x 1" (1 sq In)	256
PGA – 321	Staggered	71 mil	1.72" x 1.72" (2.96 sq In)	109
PGA – 401	Staggered	71 mil	1.922" x 1.922" (3.69 sq In)	109

The numerous electrical and mechanical advantages of surface-mount PGAs would seem to outweigh their disadvantages. However, the general state of high volume manufacturing has not kept pace with the rapid advances in semiconductor packaging. This is partly due to the requirement for state-of-the-art manufacturing equipment, which is quite expensive, and also to the need to maintain board yields with such complex devices. Therefore, in order to establish these packages as an attractive alternative, Fujitsu personnel are available to assist customers in the mounting and inspecting of these highly complex packages.

3.3 A Comparison of Through-hole and Surface Mount Devices

SMDs provide improved electrical performance and reduced system size and costs. Furthermore, with plastic flatpacks of up to 160 pins and beyond available, SMDs show promise in supporting the rapidly advancing gate size complexities and high pin count of today's ASIC products at a substantially lower cost than the large ceramic PGAs. However, as the manufacturing complexities that have just been reviewed indicate, surface mounting large ASIC devices may be difficult and risky, and the designer should be cautious in their use.

If board space constraints are not critical, if the economic impact of scaling down the end system is not great, if optimal electrical characteristics in packaging are not a critical concern, then through-hole packaging may be the best solution. On the other hand, if speed and integration requirements dictate the use of very dense gate arrays, PGAs or SMT PGAs provide both through–hole and surface mount alternatives.

3.3.1 Socketing Surface Mount Devices

Some benefits of SMDs are available to manufacturers employing through-hole packages through the use of sockets for SMDs. Sockets are available for QFPTs, small outline packages (SOPs), CLCCs and PLCCs; however, the use of QFPT and SOP sockets is normally restricted to prototyping and burn-in, while low-cost, reliable production sockets are more commonly available for PLCCs and CLCCs. These production sockets house the SMD (they are tightly tailored to the specific package) in one of two ways. Flatpacks and LCCs use low/zero insertion force with a lid that closes down on the package. PLCCs use pressured socket contacts that drive a pin into the underside of the socket. Socket pins are arranged like those of PGAs: they are through-hole, they have 100-mil spacing (generally), and they are most commonly oriented in a grid of two rows.

One advantage of these sockets is that in applications where through-hole packaging is required and the choice of through-hole packages is limited to PGAs, a plastic SM package plus the production socket will cost less than the through-hole PGA. The scenario typically occurs when the required number of pins is between 40 and 84 for PLCCs and LCCs and up to 160 or more for the flatpacks.

Another significant reason to socket SMDs results from the manufacturing difficulties of SMDs that were presented earlier. ASIC devices are usually among the largest in the system, and the most vital and expensive. For the purpose of field maintenance, many companies feel it is more economical and reliable not to risk running an ASIC device through wave or reflow solder and risking stress fractures or other damage. Furthermore, the test probing difficulties alluded to earlier are alleviated with sockets, which usually provide easy access to the contacts. Often, once reliability of the system is proven, the boards are re-laid out with surface mount devices. Therefore, simply because a manufacturing facility isn't geared up for SMT does not mean that SMT devices cannot be used there.

3.3.2 Noise Problems With Sockets

Sockets for SMDs are convenient for manufacturers not yet ready to go to SMT, or for initial prototyping where the device may frequently be removed. Socketing permits the user to gain many of the benefits of SMDs, such as reduced profile and support of high pin counts in plastic, while avoiding the drawbacks, such as special manufacturing equipment and lead probing difficulties. Unfortunately a major electrical advantage of SMDs, low pin inductance, is compromised when sockets are used. The primary result is greatly increased noise, which adversely affects overall speed and signal quality. In fact, a socketed SMD generally has a higher lead inductance than an equivalent through-hole PGA.

3.4 Summary of the Packaging Alternatives

Having reviewed the package selection alternatives presented in Section 2.0 and the various tradeoffs between the packages discussed in this section and summarized in Table 6 below, the designer can weigh the benefits and limitations of the various packages and arrive at an optimal packaging scheme.

Table 6. ASIC CMOS Package Types and their Characteristics

Package Type	Range of Physical Dimensions	Electrical Characteristics[1]	Thermal Characteristics (°C/Watt)	Usable Gates[3]	Relative Cost (per Pin)
Through-Hole DIP	# Pins: 16 to 64 Pin Pitch: 100 mils Body Length: .75" to 2.3" Body Width: .300" to .700"	R: Medium L: High C: Low	**Ceramic/Plastic** θJA[2]: 70 - 40/ 120 - 80	Up to 17K gates	1
Surface Mount SOIC	# Pins: 16 to 28 Pin Pitch: 10 mils Body Length: 50 to 70 mils Body Width: .300" to .400"	R: Medium L: Medium C: Low	**Ceramic/Plastic** θJA[2]: 110 - 80/ 130 - 105	Up to 6500 gates	1
Surface Mount QFPT	# Pins: 48 to 260 Pin Pitch: 10 mils Body Width: .65" to 1.7"	R: Medium L: Medium C: Low	**Plastic** θJA[2]: 95 - 60	Up to 17K gates	1
Surface Mount CLCC	# Pins: 28 to 84 Pin Pitch: 40 to 50 mils Body Width: .45" to .97"	R: Medium L: Medium C: Medium	**Ceramic** θJA[2]: 70 -45	Up to 25K gates	5
Surface Mount PLCC	# Pins: 28 to 84 Pin Pitch: 50 mils Body Width: .49" to 1.19"	R: Medium L: Medium C: Low	**Plastic** θJA[2]: 65 - 50	Up to 17K gates	1.05
Through-Hole PGA	# Pins: 64 to 299 Pin Pitch: .100 mils, 70 mils Body Width: 1.033" to 1.7"	**Ceramic/Plastic** R: Low/Low L: Low/Low C: High/Low	**Ceramic/Plastic** θJA[2] 40 - 19/ 46 - 38	Up to 75K gates	**Ceramic/Plastic** 11/ 3.5-5

Notes: [1]R = Resistance, L = Inductance, C = Capacitance
[2]Assuming Static Airflow
[3]Assuming 1.5μ CMOS Technology

4.0 Electrical Considerations for the Assignment of Signal, Power, and Ground Pins

Driven by the continual demand for high speed systems, CMOS ASICs that exhibit output drive levels, rise and fall times, and propagation delays comparable to yesterday's ECL circuits are now being developed. Consequently, the problems intrinsic to ECL design (even thermal management) are now appearing in CMOS designs. These problems, based on noise and its effect on the device, are introduced in this section and possible solutions are discussed.

4.1 Sources and Magnitude of Noise

CMOS circuits operate by charging and discharging node capacitances through pull-up or pull-down transistor networks constructed of P channel and N channel enhancement mode (normally off) MOSFET transistors. As a result, these circuits generate noise when switching. The following review of basic CMOS circuits and how they work explains this phenomenon in greater depth.

4.1.1 Basic CMOS Circuits

Figure 14 shows a CMOS totem pole output buffer, the typical implementation for CMOS circuits, while Figure 15 illustrates a CMOS-compatible input buffer, and Figure 16 depicts a CMOS input buffer configured to be TTL compatible.

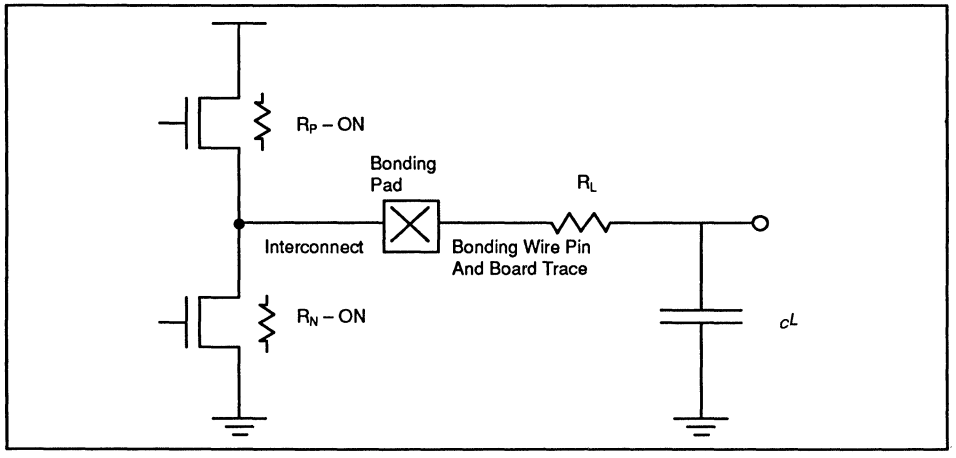


Figure 14. CMOS Output Buffer Model (Totem Pole)

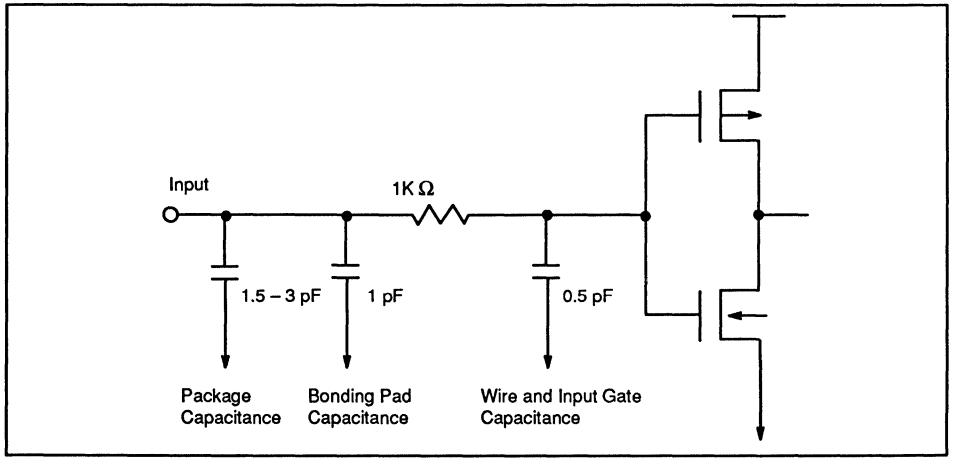
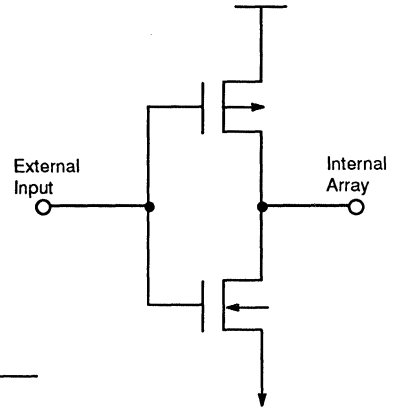


Figure 15. I/O Model, CMOS Input

The switching threshold of an inverter is dependent on the supply voltages and mobility (μ) of the P and N type transistors, as well as the W to L (transistor width to gate length) ratio of the N and P transistors. By varying the effective width (W) of the P and N transistors, it is possible to devise inverters (input buffers) that will switch at TTL levels even though they are implemented with FETs.

$$V_{INV} = \frac{\sqrt{A}\ (V_{DD} - V_{TP}) + V_{TN}}{1 + \sqrt{A}}$$



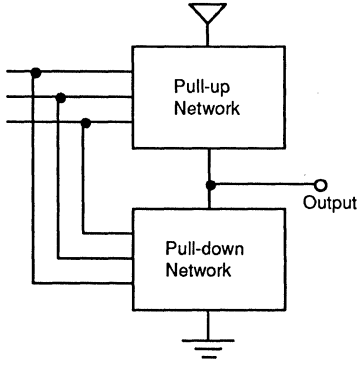
V_{TP}, V_{TN} = Thresholds of P and N transistors

V_{DD} = Supply voltage

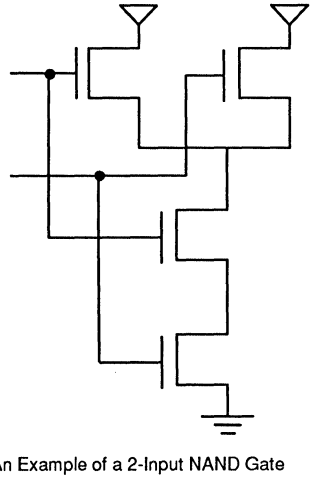
$$A = \frac{\mu_P}{\mu_N} * \frac{W_P * L_N}{L_P * W_N}$$

Figure 16. I/O Model, TTL Input

Internal CMOS circuits, such as the NAND gate shown in Figure 17 are typical of CMOS logic designs, which can be represented as a pull-up network and a pull-down network, each with its own logic and analog characteristics.



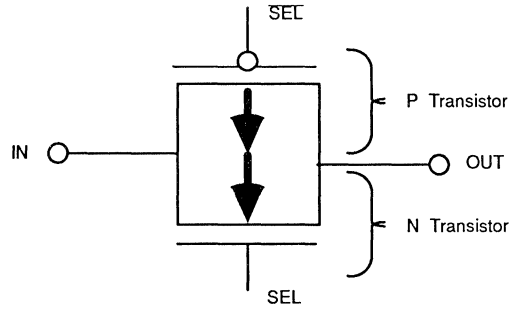
General Structure:
Output Is either pulled up or down. Inputs are never active or inactive simultaneously



An Example of a 2-Input NAND Gate

Figure 17. CMOS Basic Gate Structure: The Pull-up/Pull-down Network

The other type of element used in CMOS circuits is the transmission gate, or T-gate, which is useful for the efficient construction of multiplexers and sequential circuits (D-flops, latches, etc.) as shown in Figure 18.



SEL	OUT	
0	Hi – Z	(floating)
1	IN	(pass)

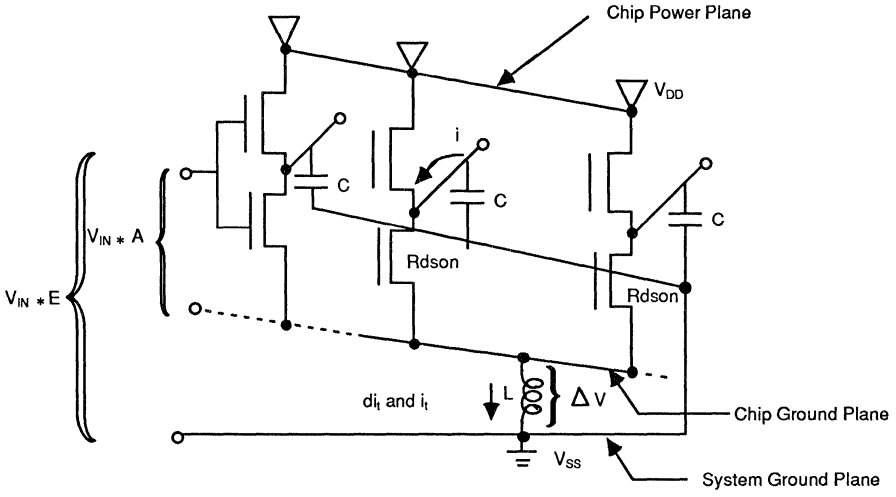
Transmission gates either pass a signal or inhibit it by floating, permitting another, active transmission gate to drive the bus to which multiple transmission gates are often tied. Transmission gates are useful for constructing multiplexers and flip-flops.

Figure 18. CMOS Basic Gate Structure: The Transmission Gate

4.1.2 Output Switching Noise and Simultaneous Switching Outputs (SSOs)

The greatest source of noise in a CMOS circuit is the result of an output switching either high to low or low to high, particularly into or out of a high capacitive load. CMOS outputs drive two types of loads, either CMOS loads, which are high in capacitance but low in leakage current, or TTL loads, which are lower in capacitance but higher in leakage current. Therefore, the AC and DC currents that the buffers see when they switch depend greatly on the type of driven load and its capacitance. When this load discharges through the N-type transistor of the totem pole output, as illustrated in Figure 14, the effect is that of a capacitor discharging through resistance. Consequently, the initial current is high and decreases over time as the output node capacitance becomes charged. Similar currents may be observed when charging the node capacitance, as in the case of a low-to-high transition.

Figure 19 shows the characteristic resistance and capacitance of various parts of the output of an ASIC device.



SSO noise is proportional to the number of SSOs, the current switched by each in a common direction (H to L in this case), and the inductance between the load and the system ground. This is represented as

$$\Delta V \text{ (ground bounce)} = (-L) \quad N \frac{di}{dt} *$$

where N is the number of SSOs, assuming all have the same di/dt.

Figure 19. Electrical Model of Simultaneously Switching Outputs

Although small, the total inductance becomes a critical factor when discharging or charging output capacitance, since the instantaneous current (*i*) is high. Recall that the self-induced voltage in an inductance, (*L*) is expressed by

$$\Delta_{VINDUCED} = \frac{L * di}{dt}$$

where *t* is time and *d* is rate of change.

In a high-drive CMOS device driving high loads, such as 200 pF, through a voltage swing approaching 5 volts with a rise/fall time of < 2 ns, the instantaneous current may be

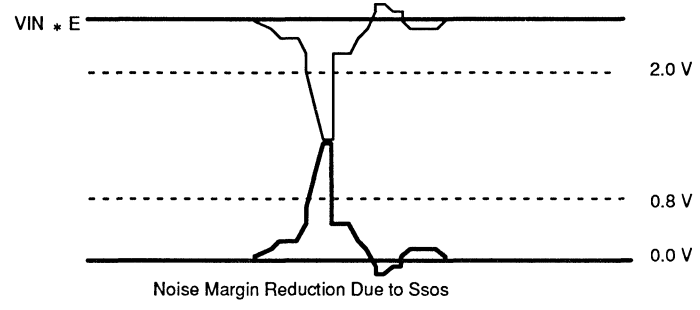
$$i = C * \frac{dv}{dt} \approx C * \frac{\Delta v}{\Delta t} \quad \textit{(average over rise and fall time)}$$

This induced voltage appears as noise on the receiving end of the signal as referenced to the ground. The current on a high-to-low transition is sunk into ground, causing the current to "bounce" or rise relative to other signals referenced to it. This ground bounce phenomenon may also apply to power on low-to-high transitions, yielding a similar noise problem.

Noise on signals may cause false triggering on the input buffer(s) being driven, or at least create a window of ambiguity in the time at which the driven input should switch (see Figure 20). Therefore, noise may result in degradation in speed resulting from adding settling time to a delay and may even result in

functional effects if false triggering occurs. Furthermore, if N multiple outputs under this condition switch simultaneously, the induced voltage is increased as a multiple of the number of outputs

$$nV = N * L * \frac{di}{dt}$$



Noise Margin Reduction Due to Ssos

- In this example, outputs switching H to L result in a ground bounce or rise in the chip ground relative to system ground.
- The rise appears as if the input signal voltage levels are reduced proportionally. If the bounce is too great, the input voltage is below V_{IH} causing false triggering.
- In the L to H case, it is the low input levels (V_{IL}) that are affected.

Figure 20. Effect of SSO Noise on Thresholds

Not only inductance but also characteristic resistance can create noise problems. The following paragraphs summarize the types of noise that exist in CMOS systems and explain how packaging impacts this noise.

4.1.3 Self-Induced Noise

Self-induced noise results when high-speed, high-drive outputs switch and introduce a spike on the signal relative to ground. The SSO effect, discussed previously, is an example of the level of self–induced noise that can occur. It is predicted by

$$\Delta V_{SI} = L \frac{\Delta i}{\Delta t}$$

where L is the inductance between the pin and ground as well as the trace inductance. Δi is the instantaneous current and Δt is the fall/rise time.

4.1.4 Mutually Induced Noise

Mutually induced noise (a form of crosstalk) occurs when a signal trace that has been running parallel to another for some distance switches, inducing a voltage into the adjacent wire. Since both inductive and capacitive coupling occur only during signal transition and propagation, the effect is additive, as the signal propagates down the trace. Resultant noise propagates in both the forward and backward directions down the line. The forward crosstalk has a pulse duration equal to the rise and fall of the signal, with an amplitude equal to the difference between the capacitive and inductive coupling. Backward crosstalk has a pulse duration equal to the transition time down the trace and an amplitude dependent on the sum of the inductive and capacitive coupling as well as the trace length.

4.1.5 Capacitive Coupled Noise

Another form of crosstalk resulting from mutual signal coupling, this noise occurs in proportion to the dielectric constant of the board, the distance of trace separation, and the trace length and width. Acting as two thin parallel plates, these traces couple switching current as integrated over time.

4.1.6 Ringing on Signals

From basic circuit theory, the designer will recall that if the signal line impedance does not match the output impedance of the buffer, then the signal is not naturally dampened. If the impedance of the load is less than that of the buffer, the signal is over-damped and will have a slow rise/fall time. However, if the buffer possesses lower impedance, then the signal is under-damped and may ring, as illustrated by Figure 3. Typically, signal line impedances are in the range of 50 to 250 Ω, while in the past buffers possessed "on" resistances of 500 Ω to 2 KΩ. However, due to the need for higher current sourcing/sinking and faster switching speeds, "on" resistances of output buffers have come down to the 10- to 50- Ω range, requiring the use of special termination techniques, discussed in the Fujitsu Application Note "Interfacing CMOS and BiCMOS VLSIs."

1

4.1.7 iR Drop

Up to this point, the sources of noise discussed have depended on inductance or capacitance. Since the DC current that a ground pin may sink, or that a power supply pin may source can be significant, the familiar voltage drop across a resistor, as current passes through it, is also a source of noise. This iR drop is the phenomenon that limits the sum of source and sink currents through power and ground pins respectively. Ohm's Law describes the effect of this noise source in the following equation defining voltage rise or drop due to iR effects:

$$\Delta V = R * \sum_{n=0}^{N-1} i_n$$

where

R is the output pin-to-ground (sink) resistance, or power pin return-loop (source) resistance (including the "on" resistance of the respective N or P channel device) and

i_n is the current through the nth output pin connected to this common ground or power pin.

4.1.8 Current Spiking or "Crowbar Noise"

As Figure 14 illustrated, a CMOS output buffer is constructed as a totem pole in which the output is taken from the common source (P type) and drain (N type) with the drain of the P type connected to power and the source of the N type connected to ground. When the input to the totem pole (the P and N gates) switches, the Miller capacitance of the gate causes the gates to charge or discharge at some specified time constant. It is possible that both transistors can be on, one in saturation and the other passing through the linear region, creating a current path between power and ground that can damage the device. This is less a concern for internal transistors than it is for the "beefy" transistors at the I/O. This current spiking can not only introduce noise on the power and ground planes, but may damage the device as well. For this reason, Fujitsu has taken precautions in the design of the CMOS output buffers to prevent this problem from occurring.

4.2 Recommended Strategy for Pin Assignment

The assignment of Clock, Scan, and other signals, as well as power and ground, to specific pins on the package affects electrical behavior (speed, noise, reliability, etc.), board manufacturing requirements, and device reliability. Therefore, optimal pin assignment strategies should consider the variables over which the user has control (placement of non-scan inputs, outputs and bi-directionals) and the variables over

which the vendor has control (power, ground and scan signal placement). Out of these relationships a method of placement can be developed, using the following approach:

(a) Prioritize the signals whose placement is most critical.

(b) Establish guidelines for the location of these signals, both in absolute position and relative to other signals.

4.2.1 Prioritization of Signals for Placement

Noise minimization is used to establish signal prioritization. All of the various forms of noise discussed in the last section are dependent on either i or di/dt, and L, M, R, or C. The signals affect i and di/dt, while the package pin location affects L, R and C. Figure 21 provides an illustration of how electrical characteristics vary by pin position.

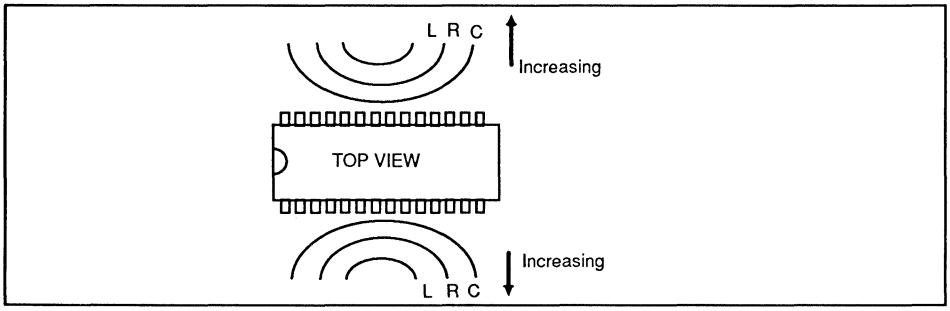


Figure 21. Variation in Inductance, Resistance, and Capacitance as a Function of Pin Position

In general, the further a pin's external contact is from the die connection, the greater its resistance, impedance, and capacitance. Therefore, signal prioritization is established according to current or its time derivative, while location is guided by package pin characteristics. Input signals are classified by their noise sensitivity. If a spike on an input could be disastrous (as with a clock), that signal should be carefully located. Table 7 classifies signal type by electrical characteristics.

Table 7. Electrical Characteristics of Each Signal Type

Signal Type	Current Characteristics (General)
Ground	Highest i, DC, and di/dt
Power	High i, DC, and di/dt
High drive outputs	High di/dt
Clocks	Highest noise sensitivity
Low drive outputs	———
Other Signals	———

4.2.2 Characteristics of Package Pins by Location

The inductance, capacitance, and resistance, all of which are critical to minimizing noise, are related not only to board construction, but also to the pin position on given packages, and the circuit to which the pins are bonded. The pin, lead frame, bonding wires, pads, and buffers (input, output or bi-directional) all influence the characteristic L, R, and C of the line. See Figure 22.

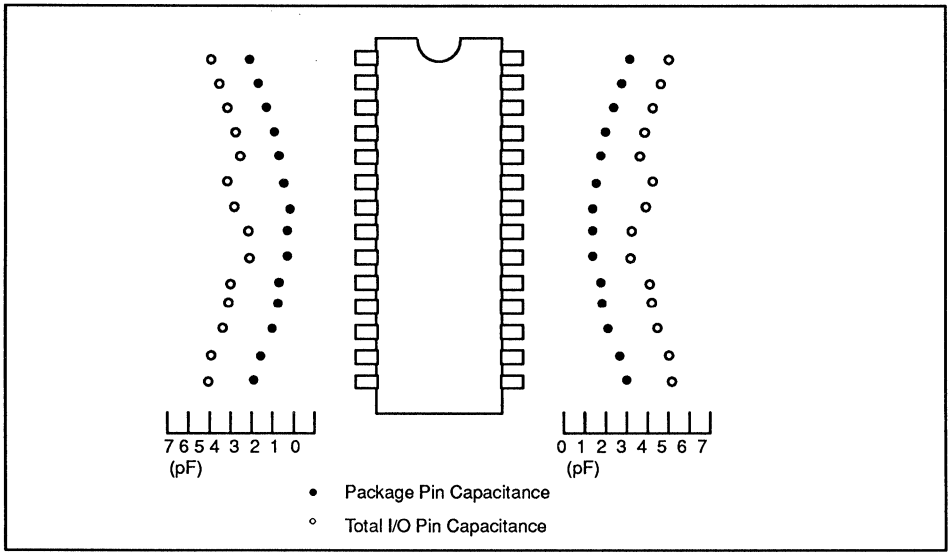


Figure 22. Measured Pin Capacitance by Package Position

4.2.3 Relating Signal Type to Pin Location

Since power and ground pins demand a large DC current (i), iR drops are of great concern. Therefore, Fujitsu assigns power and ground to pins with minimum resistance (and inductance). High-drive outputs exhibit a large di/dt, resulting from high capacitive loading, so the best pins for these signals are those of minimum inductance. Furthermore, adjacent pins possess the greatest M, and thus couple the most M di/dt noise. This means that noise-sensitive inputs, such as clock inputs, should be isolated from pins that handle high di/dt, such as high-drive outputs.

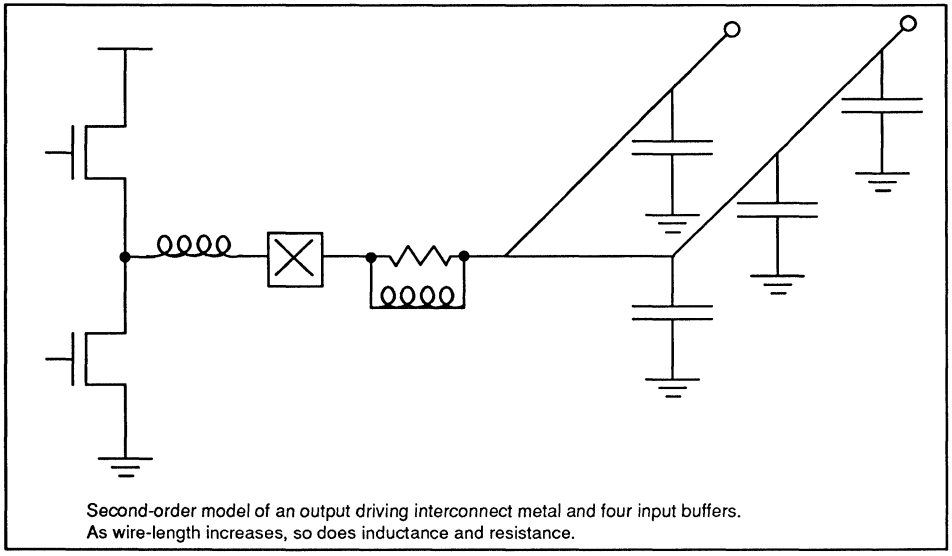
4.2.4 Minimizing iR Drops on Power and Ground Pins

Placement of ground pins is critical because noise on ground affects the voltage level of all signals referenced to it. For this reason, Fujitsu has preassigned power (V_{DD}) and ground (V_{SS}) signals for all packages in a given gate array family according to the electrically optimal locations. Preassigning power pins permits Fujitsu to develop load boards (which interface the packaged device to the tester) advanced enough to carry out high-speed functional testing of devices with high I/O count and to drive devices with relatively low noise. Fujitsu also took into consideration manufacturing issues such as adjacent pin shorting due to probes and package rotation. The predefined power and ground assignments for Fujitsu devices are found in the Package Pin Assignment Guide in the Design Manual for the appropriate gate array family, and are used in conjunction with the Package Matrix to determine pin assignment.

4.2.5 Minimizing the Self-Inductance of a Signal

Fujitsu believes that an ASIC designer concerned about designing a mini-computer, PC, mainframe or other complex system should not have to be concerned with determining specific on-chip noise issues, particularly since board-level noise issues are demanding enough. Therefore, Fujitsu developed a straightforward grouping scheme for the placement of various types of signals relative to their distance from the nearest power and ground pins. As Figure 23 shows, the self-inductance associated with a given signal is

a function of the length of wire between it and its nearest ground (for a falling transition) or power (for a rising transition).



Second-order model of an output driving interconnect metal and four input buffers.
As wire-length increases, so does inductance and resistance.

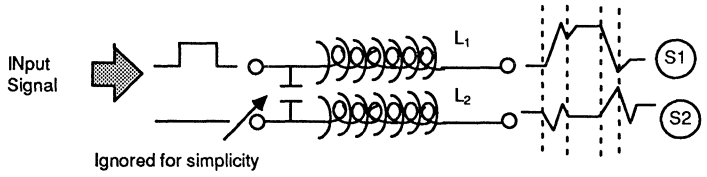
Figure 23. Self-inductance in a Circuit

Since di/dt can vary greatly for outputs within a group, there are some general restrictions relating to SSOs and their total current to the number of grounds on the chip. This is done by summing representative values like those shown in Table 5–4 in Chapter 4, which are weighed depending on the I_{OL} of the given output buffer. Notice that, if the output buffer employs noise limiting circuitry (edge rate grading) then di/dt is less and the representative value is also less, meaning more of these outputs can be supported per ground pin.

In summary, to ensure that the iR drops and the ground bounce effect (L di/dt) are within reasonable limitations, Fujitsu has established guidelines for determining the number of necessary grounds and defining the pinout.

4.2.6 Placement of Clock and Asynchronous Clear/Preset Signals

In addition to causing the ground bounce and iR drops that can deteriorate an output signal's quality and alter the ground reference, output switching can also couple noise into adjacent sensitive inputs by mutual inductance, as shown in Figure 24. For that reason, the designer should ensure that clocks and asynchronous clear and preset signals are not placed near outputs, particularly high drive outputs. To further isolate inputs from noise, the designer should minimize the inductance (length) of the return loop from the input buffer to ground by placing this type of input near a ground pin. The mutual inductance of the input buffer itself can be minimized if it, and any outputs nearby, are not assigned to high inductance pins. As discussed in Section 4.2.1, the center pins of a DIP, flatpack, or PLCC possess the lowest L and R, as do the inner rows of PGAs, making them most suitable for V_{DD}, V_{SS} and high drive outputs. But the edges of the package, while suitable for data signals, should be avoided when placing clock and other sensitive signals, as they exhibit a high mutual inductance and large iR drop.



Noise is introduced on the adjacent lead S2 as S1 is driven in a manner described by Faraday as

$$V_S = -M\frac{di\ S1}{dt}$$

where M is the mutual inductance between the adjacent leads.

If S2 is also being driven, then the mutually induced noise is superimposed on the self induced noise already present, as described by

$$V_{S2} = -M\ \frac{di\ S1}{dt} + L_2\frac{di\ S2}{dt}$$

Figure 24. Causes of Crosstalk

4.3 Summary: Choosing the Package and Assigning the Pins

This discussion of noise as related to packaging and its effect on pinout should help the designer appreciate the care Fujitsu has taken to ensure that noise margins within the device are restricted to maximize system reliability. It should also provide the designer with a basis for establishing optimum pin assignments. A step-by-step procedure for choosing an optimal package and assigning pins to it follows.

4.4 Package Selection Checklist

When selecting a package for an ASIC device, the designer should consider the following points:

a. Define a subset of the Fujitsu packages that can be supported by your company's manufacturing capabilities.

b. Estimate, as closely as possible, the gate and I/O counts of the circuit(s) to be packaged.

c. Determine the number of power and ground pins required by considering the following:

   1. Representative value limitations for SSOs
   2. Limitation of the sum of the sink current (I_{OL}) per ground pin
   3. Limitation of instantaneous current per ground pin to satisfy metal migration restrictions

d. Using the package and pin assignment section of the Design Manual, determine the packages that satisfy the signal, power, and ground pin requirements of the circuit.

e. Make sure that the electrical, mechanical, and thermal properties of the chosen packages are suitable for the application.

f. Check the mechanical dimensions in Fujitsu's ASIC Package Catalog and the power and ground pin assignment tables and grouping charts in the appropriate package and pin assignment tables for the chosen technology. Please contact Fujitsu regarding pricing trade-offs when evaluating packages or partitioning the system.

4.5 Pin Assignment Checklist

a. Follow Fujitsu's pin assignments in the Package and Pin Assignment section of the Design Manuals. Although multiple pinouts of the same package may be offered in some cases, all power and ground signals indicated on the chosen package must be connected on the board.

b. Assign input pins (in excess of 5 MHz) and high power output buffers (I_{OL} = 24 mA) according to the appropriate pin assignment table.

c. Place all high-drive (power and high power) outputs near ground pins; the higher the drive, the closer they should be placed. SSOs should be placed particularly close to ground pins.

d. Place SSOs in groups belonging to given ground pins.

e. Distance noise-sensitive signals such as clock and asynchronous clear and preset signals away from SSOs and high-drive outputs. Also, assign them to pins with low inductance and resistance, preferably near a ground, if one is available away from SSOs or high-drive outputs.

f. Place SSOs on low inductance pins, such as those located on the inner rows and middle position of the PGAs.

These guidelines assist the designer in choosing the best package for the application, resulting in a device with reliable and predictable electrical performance and without harmful DC and AC effects on the system. There are other system interface issues such as device decoupling and termination that should be considered during design. These are discussed in Fujitsu's application note, "Interfacing CMOS and BiCMOS VLSIs."

5.0 Thermal Issues in CMOS ASIC Packaging

CMOS has traditionally been associated with low power, one of the classic advantages it has over ECL. While ECL continually draws high current to supply its internal differential amplifiers and emitter-follower circuits, CMOS draws current primarily when it is switching. The total power dissipation of a CMOS device is dependent on the number of gates, the switching frequency, and the loading on the output of the gates. The revolution in CMOS technology that has resulted in densities of 100K gates has been accompanied by increases in all of the factors influencing power dissipation. Prior to 1985, when Fujitsu introduced the world's first 20,000 gate array, the C20000UH, CMOS gate arrays were not of sufficient integration density to warrant concerns about thermal control, but advancing CMOS technologies have forced this issue to the surface.

Because power is the product of current and voltage, power dissipation is important when defining the necessary power supply currents. Propagation delays and reliability of a device are also dependent on the temperature at which the die operates, as discussed in Sections 2.3.3 and 2.4.4. To ensure that speed and reliability requirements are satisfied, the designer needs to estimate the power dissipation of the device and, from this information, choose appropriate packages and system cooling techniques.

5.1 Estimation of Power Dissipation in CMOS Circuits

There are two constituent factors in the power dissipation of a semiconductor device: the DC power, which is dependent on the steady-state (quiescent) current, and the AC or dynamic power.

5.1.1 Estimation of Dynamic (AC) Power Dissipation

CMOS circuits are constructed of FETs, which possess very small leakage currents. Therefore, CMOS possesses a low quiescent or steady-state current. CMOS dissipates power primarily while it is charging or discharging node capacitance, or drawing switching current, which occurs as a gate changes state. This can be modeled as the familiar pull-up/pull-down circuit discussed in Section 4.1, charging and discharging a node capacitance, C_L (shown in Figure 14). This model holds true whether the node is internal or off-chip.

The switching current is a result of charging and discharging the node capacitance which, for periodic signals, occurs twice a cycle: once while charging the capacitance, and once while discharging it. The energy involved in charging or discharging a capacitance is $1/2(CLV^2)$. The power is the energy divided by the period of time between successive changes (the clock period, T), multiplied by the two transitions that occur per cycle. Therefore, the dynamic or switching current of a CMOS circuit is defined as

$$Pd\text{-}dyn = 2 * \frac{(C_L * V^2)}{2 * T} = (C_L * V^2) * f$$

where V is the supply voltage and f is the frequency of the given signal.

This is the power calculation for a single gate. The power dissipation for entire chip, however is much more complicated, since not all gates are simultaneously active. The degree of switching activity varies greatly within a circuit and depends on the nature of the circuits (synchronous sequential gates tend to switch concurrently, while combinatorial gates switch more randomly), the input stimulus (whether the circuit is stimulated at a periodic interval or asynchronously), and other design-dependent issues. Based on Fujitsu's experience, gate activity is on the average about 20 percent. This same figure is applied to the power estimation for output and input buffers.

1

5.1.2 Estimation of Quiescent (DC) Power Dissipation

There are two sources/sinks of DC current in a CMOS ASIC: the leakage current of the gates (gate leakage) and the DC current that flows through output and bidirectional buffers in output mode. The gate leakage in CMOS devices, even dense ones, is in the range of tens of microamperes, and is negligible. The DC current of the output buffers is the current that the buffer sources or sinks in steady state. This current level depends on the leakage currents of the driven loads, but for simplicity will be assumed to be equivalent to the I_{OL} and I_{OH} rating of the buffers. The DC power can be estimated for each output buffer by analyzing:

a. the product of source current times the voltage difference from the power rail ($V_{DD} - V_{OH}$), and

b. the sink current times the low-level voltage (V_{OL}).

This calculation is valid provided the duty cycle, or the portion of the cycle in which the output is low versus the portion of the cycle in which the output is high, weighs the sum of the two components. The total DC power may be determined by extending this method to each output and bidirectional buffer.

5.1.3 Estimation of Total Power Dissipation

The total power dissipation of a circuit is the sum of the DC and AC components. I/O buffers dissipate both DC and AC power when switching, while internal gates may be considered for the sake of simplicity, to dissipate only AC. The theory behind CMOS power dissipation is simple; however, the task of calculating the power dissipation can be tedious and prone to error. Therefore, Fujitsu has devised methods for estimating the power dissipation for each CMOS technology. These methods are presented in the Design Manual for the appropriate technology, available through the Field Applications Engineers at local Fujitsu Sales Offices or Technical Resource Centers.

5.2 The Relationship Between Power Dissipation and Temperature

A device draws current through the power supply pins and the I/O buffers. As it does so, it dissipates thermal energy proportional to the power dissipated in the device. Assuming that the power dissipation of a device has been estimated as P_d, using the method described in Section 5.1.1, how can one relate this power to the temperature of the die and the package, and also determine the warming effect on the surrounding environment?

The answer lies with two principles of heat transfer: conduction and convection. When an object is in a state of thermal equilibrium it is isothermal, seeing a constant temperature across its body. As the tem-

perature of one end of the object is raised by the introduction of energy, it is no longer in equilibrium; heat begins to flow from the warmer region to the cooler region through the process of conduction.

When a lake in winter is filled with water at a constant temperature, just above 32°F, it may still freeze. It will freeze at the surface, however, not the bottom. This is because heat is drawn from the water into the air through convection, the act of cooling by a gas.

These same mechanisms, conduction and convection, act upon a packaged semiconductor device and determine its junction temperature, the package or case temperature, and the warming effect on the surroundings.

5.2.1 Determining the Junction Temperature of a Device

Figure 25 shows the paths through which heat flows in a packaged device. Each interface of materials with different properties of thermal conduction must be considered when determining the flow of heat from the die to the surroundings. The back side of the die is attached to a lead frame or slug, usually by means of a eutectic bond (material heat bonded with some conductive material, such as silver). Heat flows through this path from the die to the package, then from the package to the surrounding air.

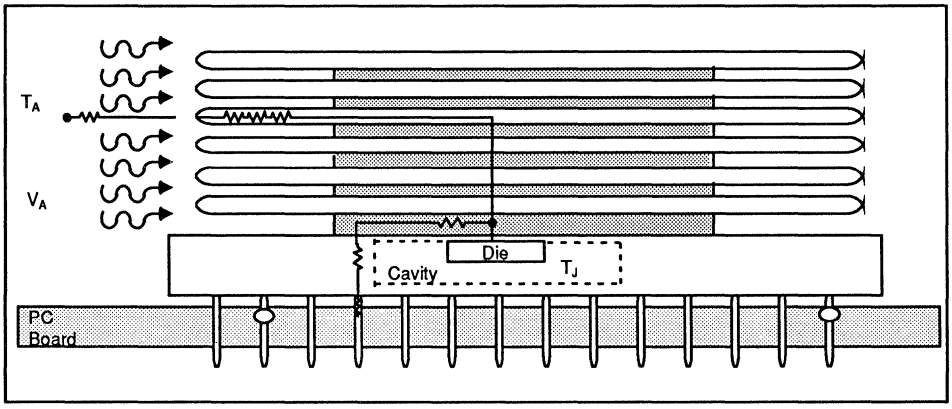


Figure 25. Heat Flow through a Cavity-down Ceramic PGA with an Annular Fin Heat Sink

From the die junction to the package, there is some associated thermal impedance (or resistance to the flow of heat). This impedance can be calculated, but may also be estimated in the following way. Operate a device and determine its power dissipation. Then, using some mechanism such as a thermal diode, whose forward bias voltage tracks linearly with temperature, determine the junction temperature. Then, after measuring the case temperature, determine the thermal impedance along the path from the die junction to the case (package body) using the following equation:

$$\theta jc = \frac{(Tc - Tj)}{P_d}$$

where Tc and Tj are the case and junction temperatures, respectively.

A similar procedure is followed when determining the thermal impedance between the junction and the ambient environment, except that the case temperature is replaced by the measurement of the ambient temperature

$$\theta ja = \frac{(Ta - Tj)}{P_d}$$

While θ_{jc} relies on conduction as its cooling mechanism, θ_{ja} reflects convective cooling. Therefore, θ_{ja} varies with airflow and is specified at a given airflow, or as static (= 0).

Since thermal impedance depends on the heat conduction path between the die and some other interface, it can be modeled the same way as current flowing through real impedance or resistance. Therefore, as in circuit theory, when multiple interfaces are oriented in parallel, the thermal impedance is lowered. However, the situation is different from circuit theory in that when a very low impedance interface, such as a heat sink, is placed in the conduction path the flow capacity is increased, with the heat sink pulling heat out at a faster rate, lowering the thermal impedance.

5.2.2 Using Thermal Impedance Data

Thermal impedance information and power dissipation information are used to estimate junction temperature and ambient temperature rise. Which impedance figure to use is based on how the device is to be cooled. If the device is air cooled (convective), then θ_{ja} should be applied, while θ_{jc} should be used if conductive techniques such as heat pipes or cold plates are employed. For example, the junction temperature may be obtained by multiplying the power dissipation of the device by the appropriate Θja and adding the ambient temperature. It is not surprising that this indicates that a small thermal impedance is desirable to achieve a low junction temperature.

Junction temperature is used to determine worst case delay multipliers and the package options for Fujitsu's CMOS AU (Sea-of-Gates) family. The junction temperature also indicates whether reliability goals are being met. The designer can trade off packages (which exhibit varying thermal impedances) with cooling techniques (such as varying the amount of airflow in a system) to achieve the desired junction temperature and consequently, worst case delay multiplier and reliability targets.

5.3 Summary of Thermal Issues

Although thermal factors in CMOS design have not previously been an issue, the increased frequency and density of current generations of CMOS devices require such considerations to be made. This section has surveyed some of the issues involved in applying thermal analysis to CMOS devices and using the information gained from such analysis to determine the appropriate packaging and cooling techniques.

6.0 Summary of the Note

As VLSI circuits increase in complexity, pin count and die size increase as well, placing greater demands on packaging, board layout, and manufacturing. Fujitsu has addressed these problems with exotic forms of packaging such as the surface mount PGA and the staggered PGA, while also stressing the importance of other surface mount packages. But simply making these packages available is not enough; Fujitsu must also provide the technical support necessary to ensure that these packages can be used successfully by our customers. Field Applications support in the local sales offices, technical information such as this Application Note, and packaging consultants at Fujitsu's San Jose headquarters all provide this support.

References

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Hoshino, H. and K. Gotanda. *Reliability of Surface Mount ICs.* Fujitsu Limited, 1987.

Kane, Jim. *Surface Mount Technology.* Santa Clara: Fujitsu Microelectronics Inc.; August 1986.

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Vest, Roger. "How to Design a Fine Pitch Footprint." *Nepcon East*: 1988.

AU Series CMOS Gate Array Unit Cell Library

Unit Cell Specification Information

This section contains specifications for all the unit cells available for the CG21 Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates. A basic cell contains one pair of P-channel and one pair of N-channel transistors (and two pairs of smaller N-channel resistors used for compiled cell construction).

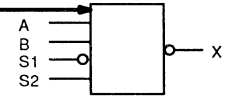
How to Read a Unit Cell Specification

The following paragraphs numbered 1–10 explain how the information given in the CG21 Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

1. The unit *cell name* appears in the upper left corner of the page.
2. The unit cell *function* is given on the same line as the unit cell name.
3. The *number of basic cells (BC)* or equivalent that make up the unit cell is shown in the upper right corner of the page.
4. *Propagation delay parameters* for the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t_0) is given in ns. K_{CL}, the delay constant for the cell (delay time per load unit) is given in ns/pF. K_{CL2} and C_{DR2} are a delay constant and an output driving factor used to calculate delay when a unit cell is loaded beyond its published output driving factor (C_{DR}).
5. The *cell symbol* (logic symbol) is shown in the top left box under the cell name.
6. Clock *parameters* (in ns) for unit cells such as flip-flops and counters that make use of clock signals are given in a table directly below the propagation delay parameters.
7. The *input loading factor* of each input of the unit cell are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
8. The *output drive factor* of each output of the unit cell is shown directly under the input loading factor. The output drive factor is the maximum number of load units the unit cell can drive while performing at published specifications.
9. The *function table* (truth table), if applicable, is shown in a box at the lower left side of the page.
10. The unit cell schematic, or *equivalent circuit*, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		AU Version
Cell Name	Function	Number of BC
T2D	2:1 Selector	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.50	0.15	0.56	0.10			A,B → X
0.54	0.15	0.41	0.10			S → X

Parameter	Symbol	Typ (ns)*

Pin Name	Input Loading Factor (lu)
A,B	1
S	1

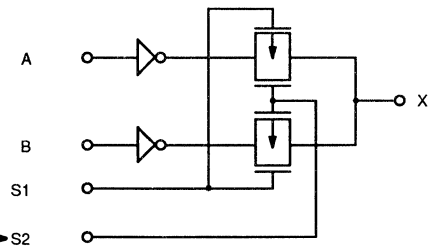
Pin Name	Output Driving Factor (lu)
X	14

* Minimum values for the typical operating conditon. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs				Output
A	B	S1	S2	X
L	X	L	H	H
H	X	L	H	L
X	L	H	L	H
X	H	H	L	L
L	H	L	L	INHIBIT
L	H	H	H	INHIBIT
H	L	L	L	INHIBIT
H	L	H	H	INHIBIT

Equivalent Circuit



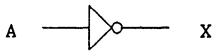
AU–T2D–E2 Sheet 1/1 Page 17–17

Inverter, Buffer Family

Page	Unit Cell Name	Function	Basic Cells
2–7	V1N	Inverter	1
2–8	V2B	Power Inverter	1
2–9	V1L	Inverting Clock Buffer	2
2–10	B1N	True Buffer	1
2–11	BD3	Delay Cell	5
2–12	BD4	Delay Cell	4
2–13	BD5	Delay Cell	9
2–14	BD6	Delay Cell	17

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
V1N	Inverter	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.23	0.13	0.28	0.07	0.10	4	A → X

Parameter	Symbol	Typ(ns)*

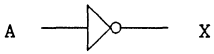
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
V2B	Power Inverter	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.20	0.07	0.20	0.04	0.07	7	A → X

Parameter	Symbol	Typ(ns)*

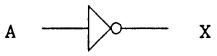
Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
V1L	Inverting Clock Buffer	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.28	0.03	0.54	0.03			A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	4

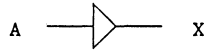
Pin Name	Output Driving Factor (ℓu)
X	55

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-V1L-E2	Sheet 1/1	Page 1-3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
B1N	True Buffer	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.47	0.13	0.55	0.07			A → X

Parameter	Symbol	Typ(ns)*

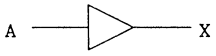
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
BD3	Delay Cell	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
4.27	0.13	3.77	0.10	0.11	4	A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
BD4	Delay Cell	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.85	0.46	3.28	0.25	0.29	4	A → X

Parameter	Symbol	Typ(ns)*

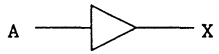
Pin Name	Input Loading Factor (ℓu)
A	4

Pin Name	Output Driving Factor (ℓu)
X	6

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
BD5	Delay Cell	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
8.74	0.13	8.28	0.08	0.12	4	A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
BD6	Delay Cell	17

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
17.6	0.14	17.46	0.07	0.11	4	A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	18

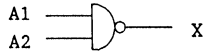
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

NAND Family

Page	Unit Cell Name	Function	Basic Cells
2–17	N2N	2-input NAND	1
2–18	N2B	Power 2-input NAND	3
2–19	N2K	Power 2-input NAND	2
2–20	N3N	3-input NAND	2
2–21	N3B	Power 3-input NAND	3
2–22	N4N	4-input NAND	2
2–23	N4B	Power 4-input NAND	4
2–24	N6B	Power 6-input NAND	5
2–25	N8B	Power 8-input NAND	6
2–26	N9B	Power 9-input NAND	8
2–27	NCB	Power 12-input NAND	10
2–28	NGB	Power 16-input NAND	11

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N2N	2-input NAND	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.30	0.13	0.45	0.11			A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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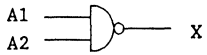
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N2B	Power 2-input NAND	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.88	0.07	1.14	0.03			A → X

Parameter	Symbol	Typ(ns)*

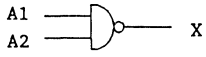
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N2K	Power 2-input NAND	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.30	0.07	0.35	0.06	0.07	7	A → X

Parameter	Symbol	Typ(ns)*

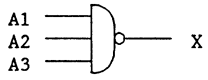
Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N3N	3-input NAND	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.42	0.13	0.55	0.15			A → X

Parameter	Symbol	Typ(ns)*

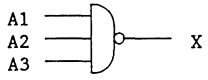
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N3B	Power 3-input NAND	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.03	0.07	1.36	0.03			A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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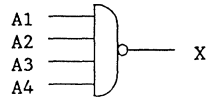
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N4N	4-input NAND	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.50	0.13	0.59	0.19			A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	10

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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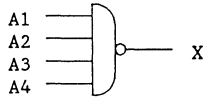
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N4B	Power 4-input NAND	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.11	0.07	1.52	0.03			A → X

Parameter	Symbol	Typ(ns)*

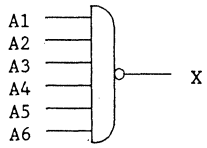
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N6B	Power 6-input NAND	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.10	0.07	1.62	0.03	0.06	7	A → X

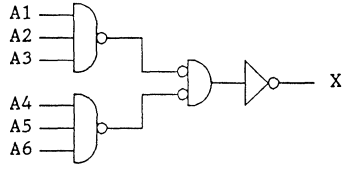
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

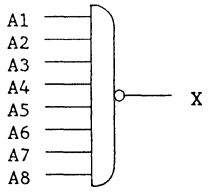
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N8B	Power 8-input NAND	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.07	1.77	0.03	0.06	7	A → X

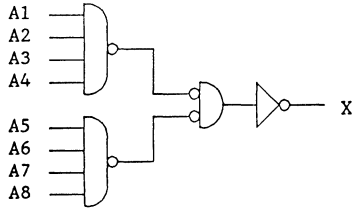
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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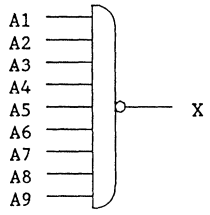
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N9B	Power 9-input NAND	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.14	0.07	2.13	0.04	0.07	7	A → X

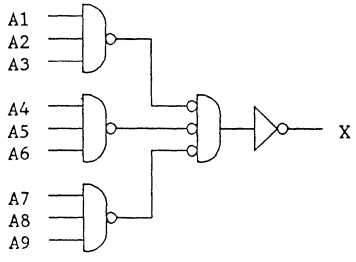
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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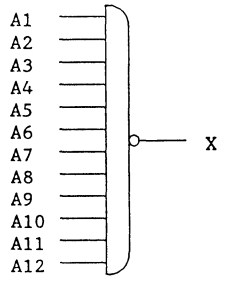
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
NCB	Power 12-input NAND	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.22	0.07	2.29	0.04	0.07	8	A → X

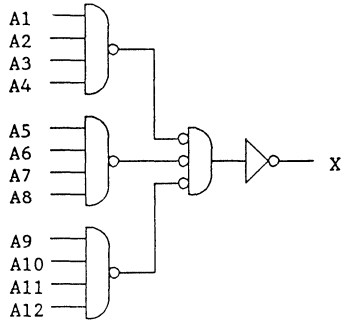
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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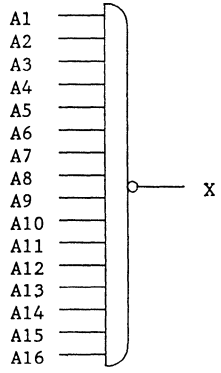
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
NGB	Power 16-input NAND	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.23	0.07	2.78	0.05	0.07	8	A → X

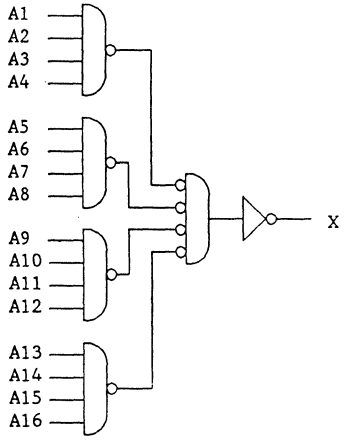
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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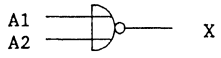
NOR Family

Page	Unit Cell Name	Function	Basic Cells
2–31	R2N	2-input NOR	1
2–32	R2B	Power 2-input NOR	3
2–33	R2K	Power 2-input NOR	2
2–34	R3N	3-input NOR	2
2–35	R3B	Power 3-input NOR	3
2–36	R4N	4-input NOR	2
2–37	R4B	Power 4-input NOR	4
2–38	R6B	Power 6-input NOR	5
2–39	R8B	Power 8-input NOR	6
2–40	R9B	Power 9-input NOR	8
2–41	RCB	Power 12-input NOR	10
2–42	RGB	Power 16-input NOR	11

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R2N	2-input NOR	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.32	0.23	0.35	0.07	0.09	4	A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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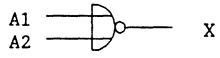
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R2B	Power 2-input NOR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.09	0.07	1.00	0.03			A → X

Parameter	Symbol	Typ(ns)*

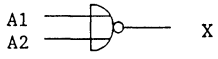
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R2K	Power 2-input NOR	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.36	0.11	0.36	0.05			A → X

Parameter	Symbol	Typ(ns)*

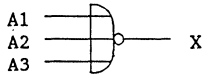
Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R3N	3-input NOR	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.67	0.33	0.37	0.07	0.10	4	A → X

Parameter	Symbol	Typ(ns)*

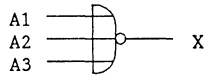
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	10

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R3B	Power 3-input NOR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.59	0.07	1.10	0.03			A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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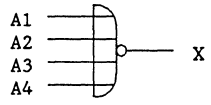
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R4N	4-input NOR	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.99	0.43	0.37	0.07	0.11	4	A → X

Parameter	Symbol	Typ(ns)*

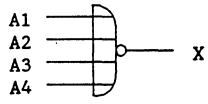
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	6

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R4B	Power 4-input NOR	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.00	0.07	1.07	0.03			A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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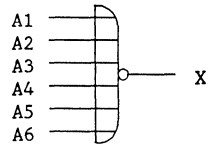
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R6B	Power 6-input NOR	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.80	0.07	1.19	0.03			A → X

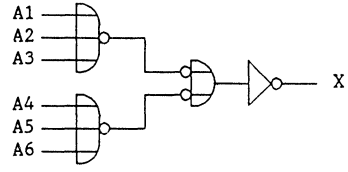
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

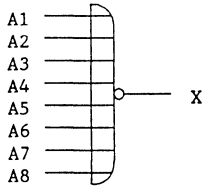
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R8B	Power 8-input NOR	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.27	0.07	1.21	0.03			A → X

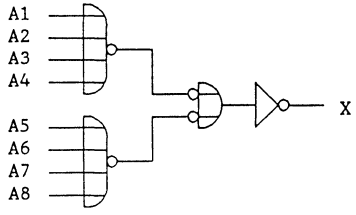
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

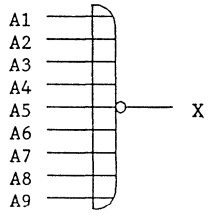
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R9B	Power 9-input NOR	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99	0.07	1.35	0.03			A → X

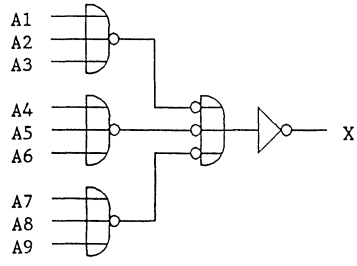
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

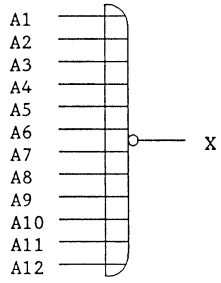
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
RCB	Power 12-input NOR	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.19	0.07	1.40	0.03			A → X

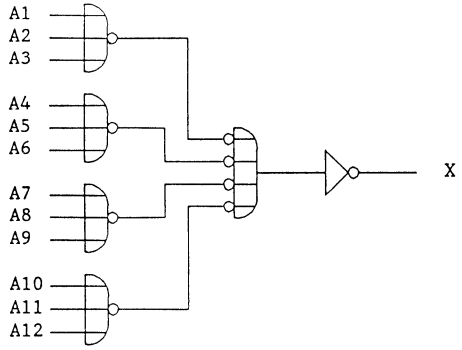
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

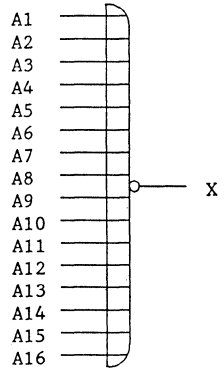
Equivalent Circuit



AU-RCB-E2	Sheet 1/1	Page 3-11

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
RGB	Power 16-input NOR	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.75	0.07	1.46	0.03			A → X

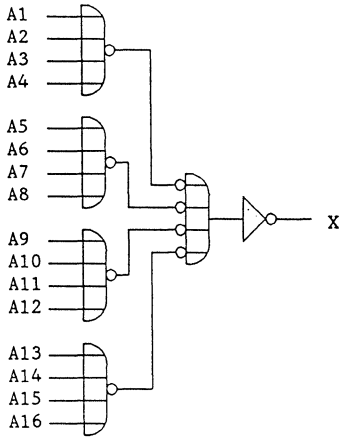
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



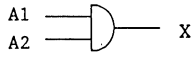
AU-RGB-E2	Sheet 1/1	Page 3-12

AND Family

Page	Unit Cell Name	Function	Basic Cells
2–45	N2P	Power 2-input AND	2
2–46	N3P	Power 3-input AND	3
2–47	N4P	Power 4-input AND	3
2–48	N8P	Power 8-input AND	6

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N2P	Power 2-input AND	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.81	0.07	0.69	0.03	0.05	7	A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

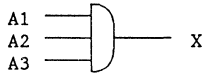
Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-N2P-E2	Sheet 1/1	Page 4-1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N3P	Power 3-input AND	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.06	0.07	0.86	0.03	0.05	7	A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

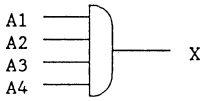
Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-N3P-E2	Sheet 1/1	Page 4-2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N4P	Power 4-input AND	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.27	0.07	0.95	0.03	0.05	8	A → X

Parameter	Symbol	Typ(ns)*

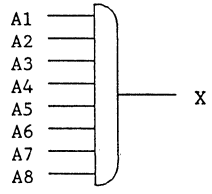
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
N8P	Power 8-input AND	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.38	0.11	1.16	0.03	0.05	8	A → X

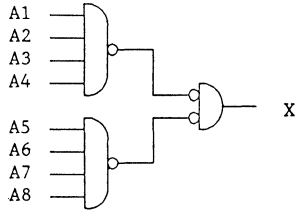
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



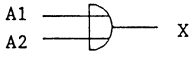
AU-N8P-E2	Sheet 1/1	Page 4-4

OR Family

Page	Unit Cell Name	Function	Basic Cells
2–51	R2P	Power 2-input OR	2
2–52	R3P	Power 3-input OR	3
2–53	R4P	Power 4-input OR	3
2–54	R8P	Power 8-input OR	6

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R2P	Power 2-input OR	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.63	0.07	0.91	0.04	0.06	8	A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

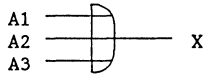
Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-R2P-E2	Sheet 1/1	Page 5-1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R3P	Power 3-input OR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.72	0.07	1.47	0.05	0.07	8	A → X

Parameter	Symbol	Typ(ns)*

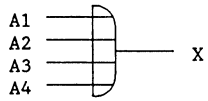
Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R4P	Power 4-input OR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.72	0.07	2.02	0.06	0.08	8	A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

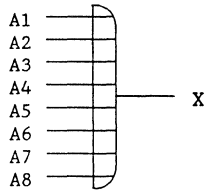
Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-R4P-E2	Sheet 1/1	Page 5-3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
R8P	Power 8-input OR	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.79	0..07	2.15	0.07	0.08	8	A → X

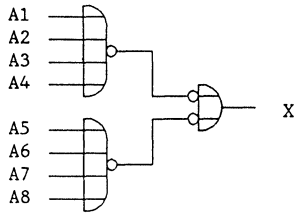
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit

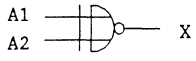


EXNOR/EXOR Family

Page	Unit Cell Name	Function	Basic Cells
2–57	X1N	Exclusive NOR	3
2–58	X1B	Power Exclusive NOR	4
2–59	X2N	Exclusive OR	3
2–60	X2B	Power Exclusive OR	4
2–61	X3N	3-input Exclusive NOR	5
2–62	X3B	Power 3-input Exclusive NOR	6
2–63	X4N	3-input Exclusive OR	5
2–64	X4B	Power 3-input Exclusive OR	6

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
X1N	Exclusive NOR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.93	0.23	0.77	0.11	0.13	4	A → X

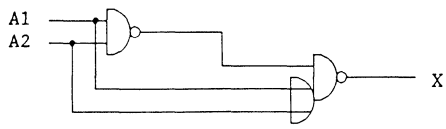
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

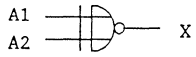
Equivalent Circuit



AU-X1N-E2	Sheet 1/1	Page 6-1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
X1B	Power Exclusive NOR	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.19	0.07	1.42	0.04	0.07	7	A → X

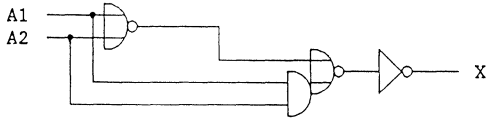
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

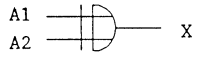
Equivalent Circuit



AU-X1B-E2	Sheet 1/1	Page 6-2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
X2N	Exclusive OR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.89	0.23	0.94	0.11	0.13	4	A → X

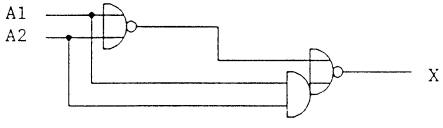
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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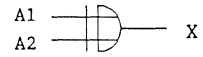
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
X2B	Power Exclusive OR	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.07	1.31	0.04	0.06	7	A → X

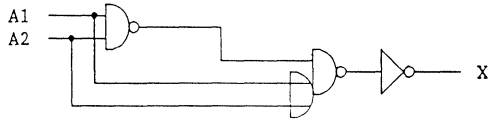
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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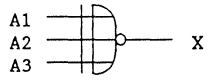
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
X3N	3-input Exclusive NOR	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.18	0.23	1.86	0.11	0.13	4	A → X

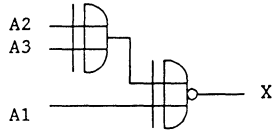
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

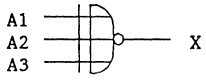
Equivalent Circuit



AU-X3N-E2	Sheet 1/1	Page 6-5

Cell Name	Function	Number of BC
X3B	Power 3-input Exclusive NOR	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.11	0.07	2.71	0.04	0.07	7	A → X

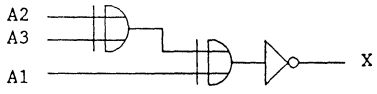
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (&u)
A	2

Pin Name	Output Driving Factor (&u)
X	36

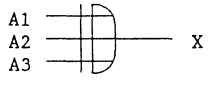
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
X4N	3-input Exclusive OR	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.26	0.23	2.03	0.11	0.13	4	A → X

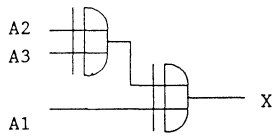
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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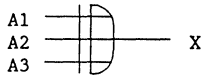
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
X4B	Power 3-input Exclusive OR	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.98	0.07	2.51	0.04	0.06	7	A → X

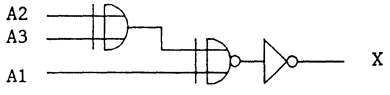
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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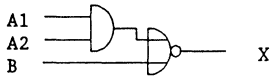
AND–OR–Inverter Family

Page	Unit Cell Name	Function	Basic Cells
2–67	D23	2-wide 2-AND 3-input AOI	2
2–68	D14	2-wide 3-AND 4-input AOI	2
2–69	D24	2-wide 2-AND 4-input AOI	2
2–70	D34	3-wide 2-AND 4-input AOI	2
2–71	D36	3-wide 2-AND 6-input AOI	3
2–72	D44	2-wide 2-OR 2-AND 4-input AOI	2

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
D23	2-wide 2-AND 3-input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	LD2	Path
0.59	0.23	0.55	0.11			A → X
0.30	0.18	0.30	0.07	0.10	4	B → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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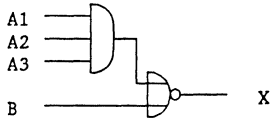
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
D14	2-wide 3-AND 4-input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.72	0.23	0.56	0.15	0.17	4	A → X
0.26	0.16	0.29	0.07	0.10	4	B → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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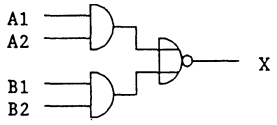
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
D24	2-wide 2-AND 4-input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.43	0.18	0.50	0.11			A → X
0.54	0.18	0.67	0.11			B → X

Parameter	Symbol	Typ(ns)*

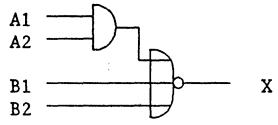
Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
D34	3-wide 2-AND 4-input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.92	0.33	0.59	0.12			A → X
0.50	0.28	0.35	0.07	0.10	4	B → X

Parameter	Symbol	Typ(ns)*

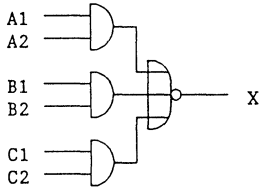
Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	10

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
D36	3-wide 2-AND 6-input AOI	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.62	0.23	0.58	0.11			A → X
0.79	0.23	0.70	0.11			B → X
0.94	0.23	0.82	0.11			C → X

Parameter	Symbol	Typ(ns)*

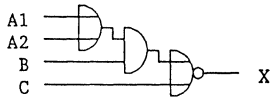
Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (ℓu)
X	10

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
D44	2-wide 2-OR 2-AND 4-input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.83	0.33	0.63	0.11			A → X
0.83	0.33	0.51	0.11			B → X
0.79	0.23	0.39	0.07	0.09	4	C → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (ℓu)
X	10

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

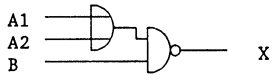
OR–AND–Inverter Family

Page	Unit Cell Name	Function	Basic Cells
2–75	G23	2-wide 2-OR 3-input OAI	2
2–76	G14	2-wide 3-OR 4-input OAI	2
2–77	G24	2-wide 2-OR 4-input OAI	2
2–78	G34	3-wide 2-OR 4-input OAI	2
2–79	G44	2-wide 2-AND 2-OR 4-input OAI	2

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
G23	2-wide 2-OR 3-input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.58	0.23	0.44	0.11			A → X
0.23	0.13	0.44	0.11			B → X

Parameter	Symbol	Typ(ns)*

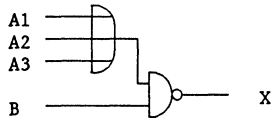
Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
G14	2-wide 3-OR 4-input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.96	0.34	0.52	0.11			A → X
0.20	0.13	0.52	0.11			B → X

Parameter	Symbol	Typ(ns)*

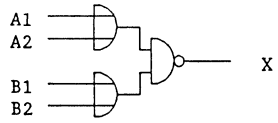
Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	10

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
G24	2-wide 2-OR 4-input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.40	0.23	0.56	0.11			A → X
0.72	0.23	0.48	0.11			B → X

Pin Name	Input Loading Factor (ℓu)
A	1
B	1

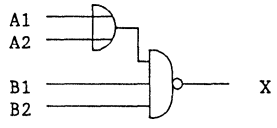
Pin Name	Output Driving Factor (ℓu)
X	10

Parameter	Symbol	Typ(ns)*

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
G34	3-wide 2-OR 4-input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.76	0.23	0.56	0.15			A → X
0.56	0.15	0.36	0.13			B → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	10

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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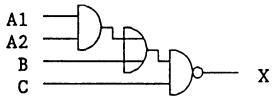
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
G44	2-wide 2-AND 2-OR 4-input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.59	0.23	0.69	0.15			A → X
0.35	0.23	0.50	0.15			B → X
0.40	0.13	0.42	0.11			C → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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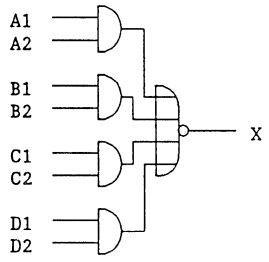
Multiplexer Family

Page	Unit Cell Name	Function	Basic Cells
2–83	T24	Power 2-AND 4-wide Multiplexer	6
2–84	T26	Power 2-AND 6-wide Multiplexer	10
2–85	T28	Power 2-AND 8-wide Multiplexer	11
2–87	T32	Power 3-AND 2-wide Multiplexer	5
2–88	T33	Power 3-AND 3-wide Multiplexer	7
2–89	T34	Power 3-AND 4-wide Multiplexer	9
2–90	T42	Power 4-AND 2-wide Multiplexer	6
2–91	T43	Power 4-AND 3-wide Multiplexer	10
2–92	T44	Power 4-AND 4-wide Multiplexer	11
2–93	T54	Power 4–2–3–2 AND 4-wide Multiplexer	10
2–94	U24	Power 2-OR 4-wide Multiplexer	6
2–95	U26	Power 2-OR 6-wide Multiplexer	9
2–96	U28	Power 2-OR 8-wide Multiplexer	11
2–97	U32	Power 3-OR 2-wide Multiplexer	5
2–98	U33	Power 3-OR 3-wide Multiplexer	7
2–99	U34	Power 3-OR 4-wide Multiplexer	9
2–100	U42	Power 4-OR 2-wide Multiplexer	6
2–101	U43	Power 4-OR 3-wide Multiplexer	9
2–102	U44	Power 4-OR 4-wide Multiplexer	11

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T24	Power 2-AND 4-wide Multiplexer	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.30	0.07	1.22	0.03			A → X
1.44	0.07	1.41	0.03			B → X
1.27	0.07	1.31	0.03			C → X
1.38	0.07	1.51	0.03			D → X

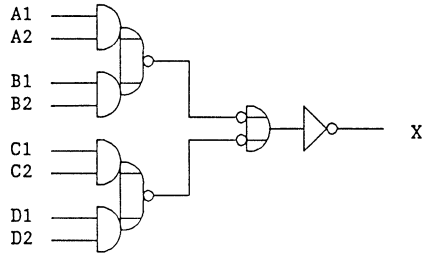
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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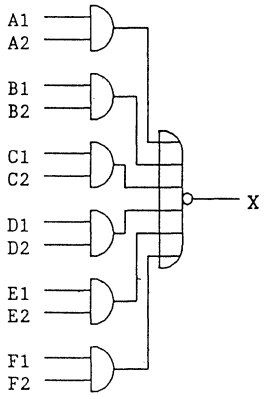
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T26	Power 2-AND 6-wide Multiplexer	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.51	0.07	1.26	0.03			A → X
1.66	0.07	1.45	0.03			B → X
1.51	0.07	1.33	0.03			C → X
1.63	0.07	1.54	0.03			D → X
1.52	0.07	1.47	0.03			E → X
1.65	0.07	1.67	0.03			F → X

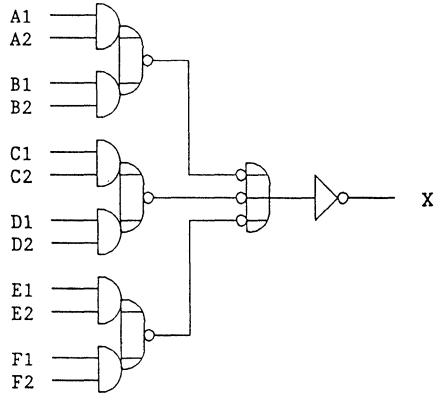
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1
E	1
F	1

Pin Name	Output Driving Factor (ℓu)
X	36

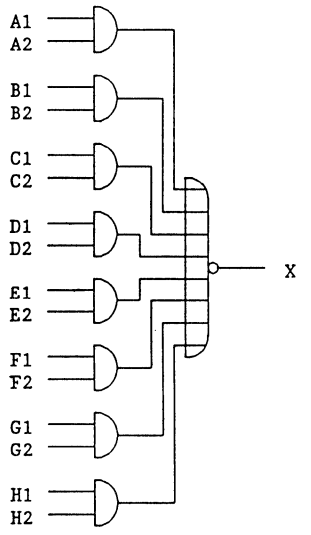
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T28	Power 2-AND 8-wide Multiplexer	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.70	0.07	1.22	0.03			A → X
1.86	0.07	1.44	0.03			B → X
1.70	0.07	1.35	0.03			C → X
1.83	0.07	1.57	0.03			D → X
1.76	0.07	1.73	0.03			E → X
1.89	0.07	1.67	0.03			F → X
1.76	0.07	1.54	0.03			G → X
1.89	0.07	1.75	0.03			H → X

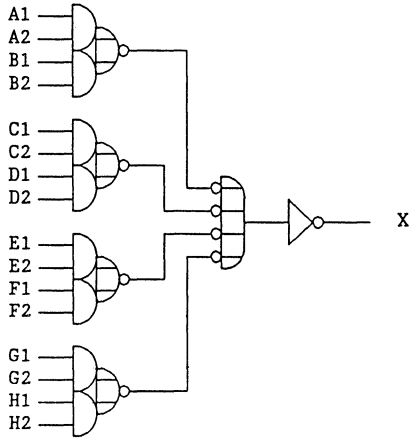
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1
E	1
F	1
G	1
H	1

Pin Name	Output Driving Factor (ℓu)
X	36

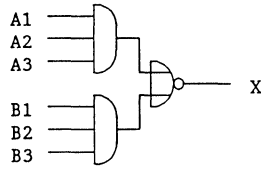
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T32	Power 3-AND 2-wide Multiplexer	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.22	0.07	1.35	0.03			A → X
1.22	0.07	1.44	0.03			B → X

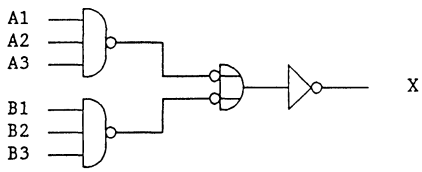
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	36

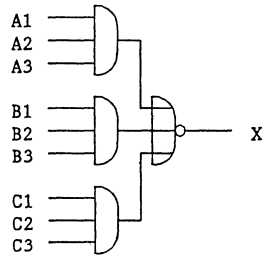
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T33	Power 3-AND 3-wide Multiplexer	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.40	0.07	1.33	0.03			A → X
1.40	0.07	1.43	0.03			B → X
1.40	0.07	1.56	0.03			C → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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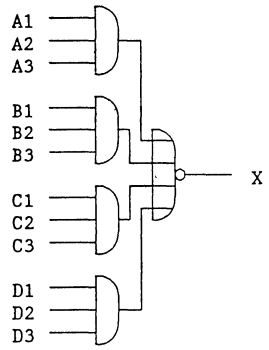
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T34	Power 3-AND 4-wide Multiplexer	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.67	0.07	1.38	0.03			A → X
1.67	0.07	1.51	0.03			B → X
1.75	0.07	1.60	0.03			C → X
1.75	0.07	1.61	0.03			D → X

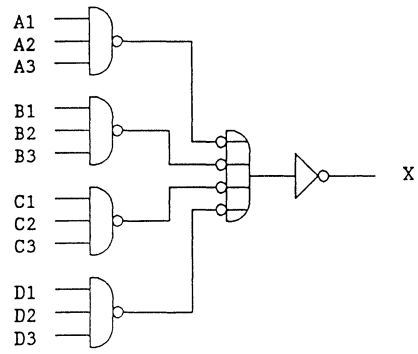
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (ℓu)
X	36

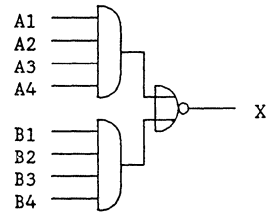
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T42	Power 4-AND 2-wide Multiplexer	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.28	0.07	1.51	0.03			A → X
1.28	0.07	1.60	0.03			B → X

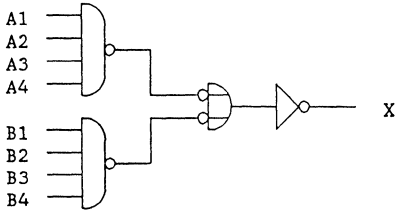
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	36

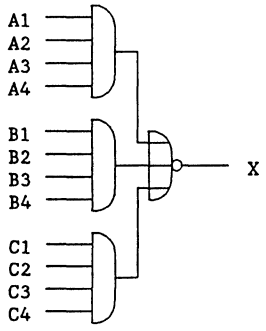
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T43	Power 4-AND 3-wide Multiplexer	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.51	0.07	1.54	0.03			A → X
1.51	0.07	1.63	0.03			B → X
1.51	0.07	1.76	0.03			C → X

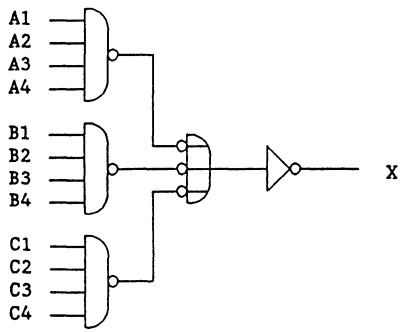
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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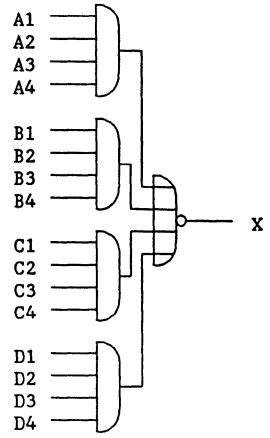
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T44	Power 4-AND 4-wide Multiplexer	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.73	0.07	1.54	0.03			A → X
1.73	0.07	1.31	0.03			B → X
1.73	0.07	1.76	0.03			C → X
1.73	0.07	1.86	0.03			D → X

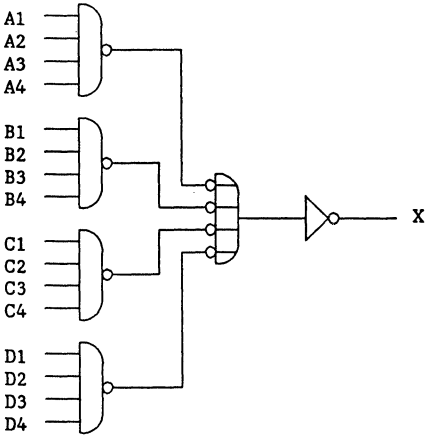
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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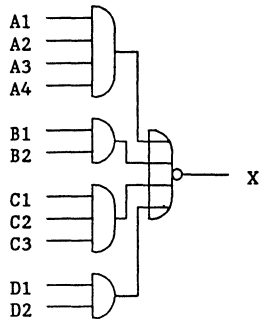
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T54	Power 4-2-3-2 AND 4-wide Multiplexer	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.65	0.07	1.57	0.03			A → X
1.54	0.07	1.31	0.03			B → X
1.65	0.07	1.65	0.03			C → X
1.54	0.07	1.51	0.03			D → X

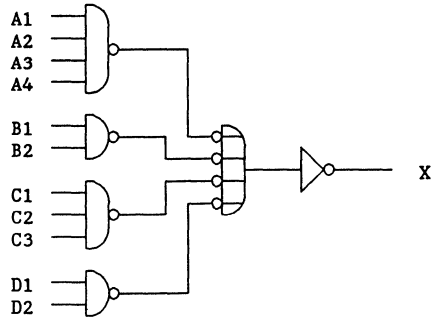
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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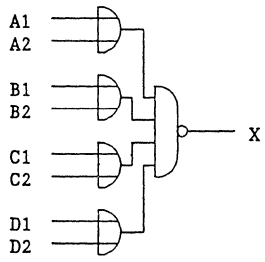
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
U24	Power 2-OR 4-wide Multiplexer	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.60	0.07	1.44	0.04	0.07	7	A → X
1.15	0.07	1.40	0.04	0.07	7	B → X
1.52	0.07	1.43	0.04	0.07	7	C → X
1.11	0.07	1.36	0.04	0.07	7	D → X

Parameter	Symbol	Typ(ns)*

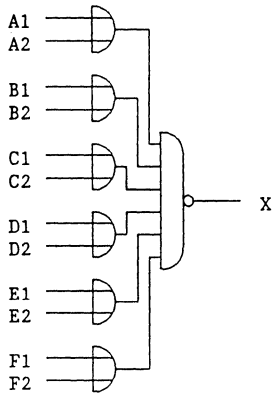
Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
U26	Power 2-OR 6-wide Multiplexer	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.60	0.07	1.87	0.04	0.07	7	A → X
1.24	0.07	1.81	0.04	0.07	7	B → X
1.63	0.07	1.92	0.04	0.07	7	C → X
1.27	0.07	1.92	0.04	0.07	7	D → X
1.31	0.07	2.07	0.04	0.07	7	E → X
1.68	0.07	2.07	0.04	0.07	7	F → X

Parameter	Symbol	Typ(ns)*

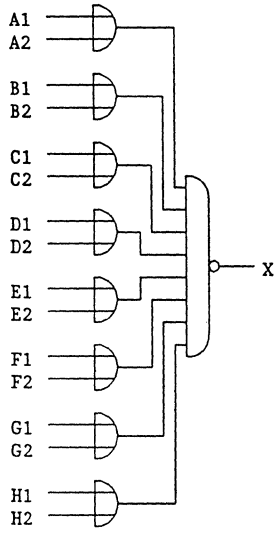
Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1
E	1
F	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
U28	Power 2-OR 8-wide Multiplexer	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.69	0.07	2.55	0.05	0.08	7	A → X
1.24	0.07	2.51	0.05	0.08	7	B → X
1.21	0.07	2.25	0.05	0.08	7	C → X
1.66	0.07	2.29	0.05	0.08	7	D → X
1.69	0.07	2.51	0.05	0.08	7	E → X
1.24	0.07	2.47	0.05	0.08	7	F → X
1.17	0.07	2.03	0.05	0.08	7	G → X
1.63	0.07	2.11	0.05	0.08	7	H → X

Parameter	Symbol	Typ(ns)*

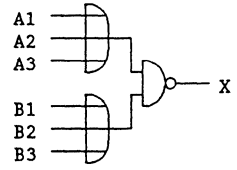
Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1
E	1
F	1
G	1
H	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
U32	Power 3-OR 2-wide Multiplexer	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.72	0.07	1.33	0.04	0.07	7	A → X
1.69	0.07	1.31	0.04	0.07	7	B → X

Parameter	Symbol	Typ(ns)*

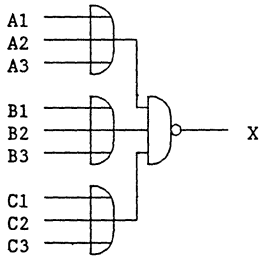
Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
U33	Power 3-OR 3-wide Multiplexer	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.83	0.07	1.83	0.04	0.09	7	A → X
1.80	0.07	1.91	0.04	0.09	7	B → X
1.85	0.07	2.02	0.04	0.08	7	C → X

Parameter	Symbol	Typ(ns)*

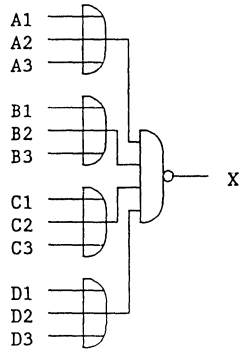
Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
U34	Power 3-OR 4-wide Multiplexer	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.69	0.07	2.39	0.05	0.08	7	A → X
1.71	0.07	2.40	0.05	0.08	7	B → X
1.54	0.07	1.95	0.05	0.08	7	C → X
1.69	0.07	2.15	0.05	0.08	7	D → X

Parameter	Symbol	Typ(ns)*

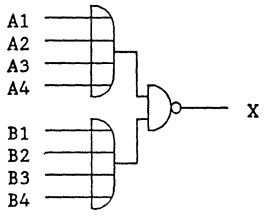
Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
U42	Power 4-OR 2-wide Multiplexer	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.08	0.07	1.37	0.04	0.07	7	A → X
2.03	0.07	1.31	0.04	0.07	7	B → X

Parameter	Symbol	Typ(ns)*

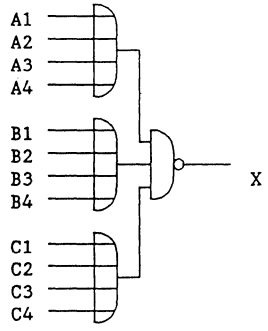
Pin Name	Input Loading Factor (ℓu)
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
U43	Power 4-OR 3-wide Multiplexer	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.06	0.07	1.71	0.05	0.07	7	A → X
2.10	0.07	1.81	0.05	0.07	7	B → X
2.16	0.07	1.91	0.05	0.07	7	C → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1

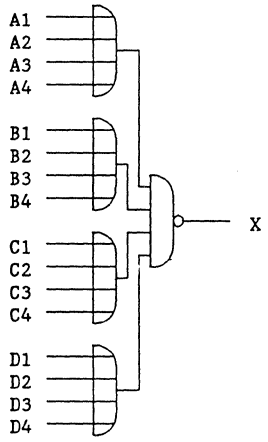
Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-U43-E2	Sheet 1/1	Page 9-19

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
U44	Power 4-OR 4-wide Multiplexer	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.19	0.07	2.40	0.04	0.09	7	A → X
2.18	0.07	2.31	0.04	0.09	7	B → X
2.11	0.07	1.95	0.04	0.09	7	C → X
2.14	0.07	2.15	0.04	0.09	7	D → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Clock Buffer Family

Page	Unit Cell Name	Function	Basic Cells
2–105	K1B	True Clock Buffer	2
2–106	K2B	Power Clock Buffer	3
2–107	K3B	Gated Clock (AND) Buffer	2
2–108	K4B	Gated Clock (OR) Buffer	2
2–109	K5B	Gated Clock (NAND) Buffer	3
2–110	KAB	Block Clock (OR) Buffer	3
2–111	KBB	Block Clock (OR x 10) Buffer	30
2–113	KDB	Block Clock (OR x 10) Buffer	32
2–115	KEB	Block Clock Buffer	23

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
K1B	True Clock Buffer	2

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.58	0.07	0.69	0.03			A → X

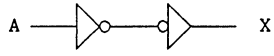
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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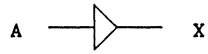
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
K2B	Power Clock Buffer	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85	0.03	0.96	0.03			A → X

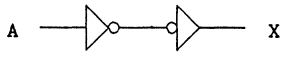
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	55

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

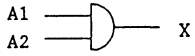
Equivalent Circuit



AU-K2B-E2	Sheet 1/1	Page 10-2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
K3B	Gated Clock (AND) Buffer	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.80	0.07	0.80	0.03			A → X

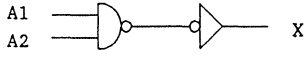
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

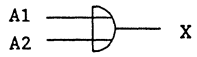
Equivalent Circuit



AU-K3B-E2	Sheet 1/1	Page 10-3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
K4B	Gated Clock (OR) Buffer	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.63	0.07	0.91	0.04	0.06	8	A → X

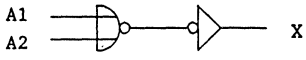
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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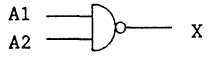
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
K5B	Gated Clock (NAND) Buffer	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.91	0.07	1.19	0.03			A → X

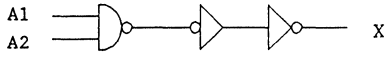
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (&u)
A	1

Pin Name	Output Driving Factor (&u)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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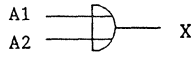
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
KAB	Block Clock (OR) Buffer	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.87	0.03	1.48	0.03			A → X

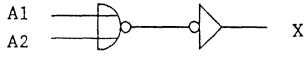
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1

Pin Name	Output Driving Factor (ℓu)
X	55

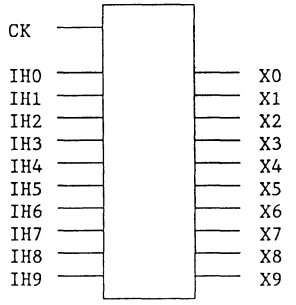
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
KBB	Block Clock Buffer (OR x 10)	30

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.07	0.03	1.67	0.03			CK → X
0.87	0.03	1.48	0.03			IH → X

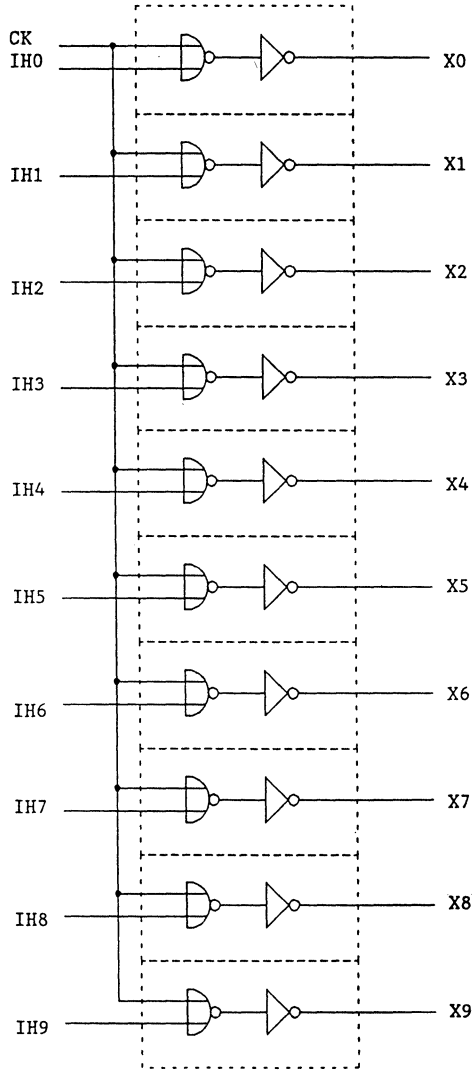
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
CK	10
IH	1

Pin Name	Output Driving Factor (ℓu)
X	55

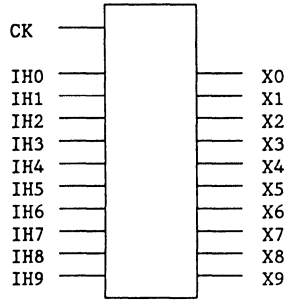
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
KDB	Block Clock Buffer (OR x 10)	32

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.90	0.04	2.80	0.02			CK → X
0.90	0.04	1.85	0.02			IH → X

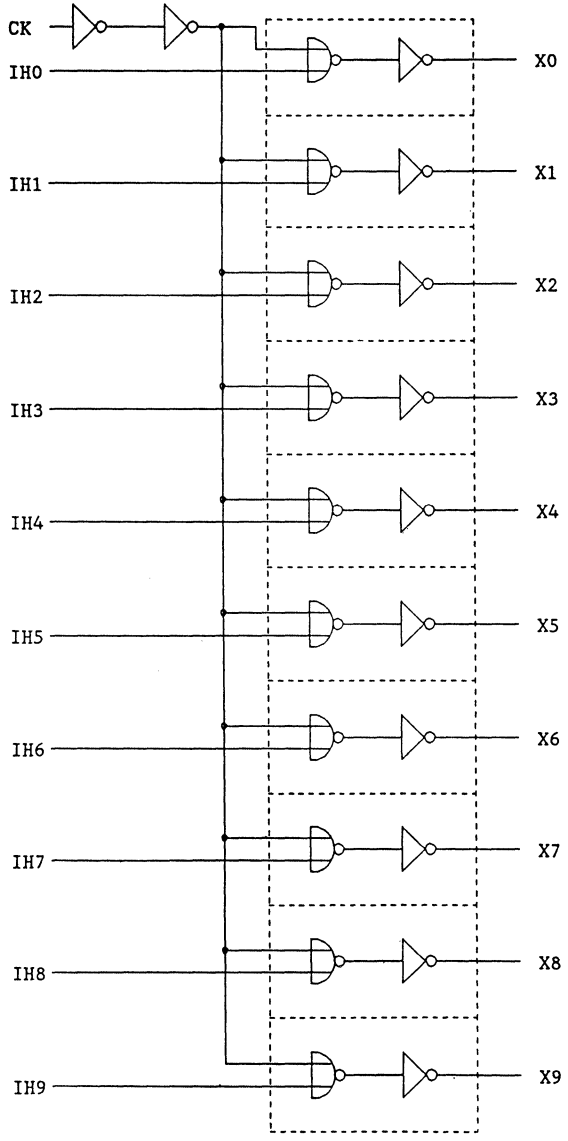
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (&u)
CK	1
IH	1

Pin Name	Output Driving Factor (&u)
X	55

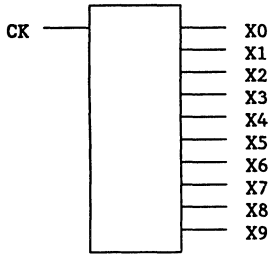
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
KEB	Block Clock Buffer	23

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.25	0.04	1.38	0.02	0.04	18	CK → X

Parameter	Symbol	Typ(ns)*

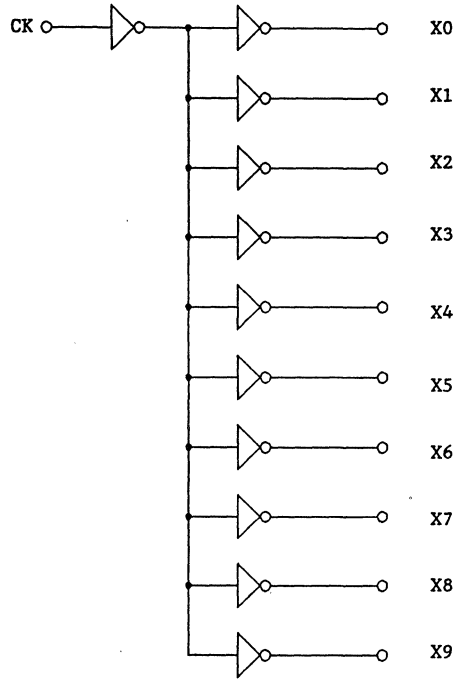
Pin Name	Input Loading Factor (£u)
CK	6

Pin Name	Output Driving Factor (£u)
X	55

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Note: The KEB is an equivalent of the KDB and the KBB, and it must be treated in the same manner as the KBB and the KDB in the logic circuit design.

Equivalent Circuit



Scan Flip-flop (Positive Edge Type) Family

Page	Unit Cell Name	Function	Basic Cells
2–119	SDH	Scan 2-input D Flip-flop with Clear and Clock Inhibit	14
2–122	SDJ	Scan 4-input D Flip-flop with Clear and Clock Inhibit	15
2–125	SDK	Scan 6-input D Flip-flop with Clear and Clock Inhibit	16
2–128	SJH	Scan J–K Flip-flop with Clear and Clock Inhibit	16
2–131	SDD	Scan 2-input D Flip-flop with Clear, Preset, and Clock Inhibit	16
2–135	SDA	Scan 1-input D Flip-flop with Clock Inhibit	12
2–138	SDB	Scan 1-input 4-bit D Flip-flop with Clock Inhibit	42
2–142	SHA	Scan 1-input 8-bit D Flip-flop with Clock Inhibit	68
2–145	SHB	Scan 1-input 8-bit D Flip-flop with Clock Inhibit and Q Output	62
2–148	SHC	Scan 1-input 8-bit D Flip-flop with Clock Inhibit and XQ Output	62
2–151	SHJ	Scan 8-bit D Flip-flop with Clock Inhibit and 2–to–1 Data Multiplexer	78
2–154	SHK	Scan 8-bit D Flip-flop with Clock Inhibit and 3–to–1 Data Multiplexer	88
2–157	SFDM	Scan 1-input D Flip-flop with Clock Inhibit	10
2–160	SFDO	Scan 1-input D Flip-flop with Clear and Clock Inhibit	11
2–163	SFDP	Scan 1-input D Flip-flop with Clear, Preset, and Clock Inhibit	12
2–167	SFDR	Scan 4-input D Flip-flop with Clear and Clock Inhibit	36
2–171	SFDS	Scan 4-input D Flip-flop with Clock Inhibit	31
2–175	SFJD	Scan J-K Flip-flop with Clock Inhibit	14

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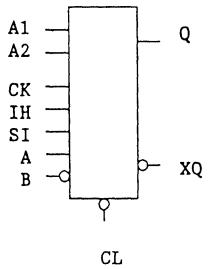
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SDH	SCAN 2-input DFF with Clear & Clock-Inhibit	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.98	0.07	2.39	0.03	0.07	7	CK,IH → Q
1.88	0.07	1.72	0.05	0.10	7	CK,IH → XQ
3.03	0.07	0.86	0.03	0.07	7	CL → Q, XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.4
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	3.0
Data Hold Time	tHD	0.8
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	2.4
Clear Hold Time	tINH	1.2

Pin Name	Input Loading Factor (ℓu)
A1,A2	1
CK	1
IH	1
CL	3
SI	1
A,B	2

Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

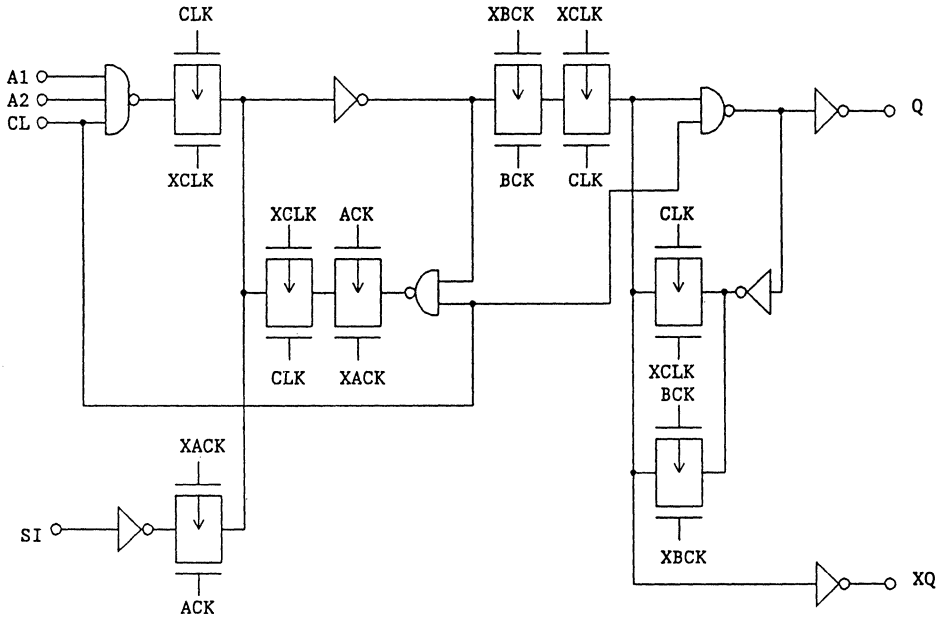
Function Table

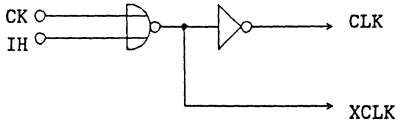
MODE	INPUT						OUTPUT	
	CLK	CL	D	A	B	SI	Q	XQ
CLEAR	X	L	X	X	X	X	L	H
CLOCK	L→H	H	Di	L	L	X	Di	$\overline{Di}$
	H	H	X	L	L	X	Q_0	XQ_0
SCAN	H	H	X	L→H→L	H	Si	Q_0	XQ_0
	H	H	X	L	H→L→H	X	Si	$\overline{Si}$

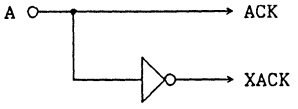
Note : CLK = CK + IH
D = A1 x A2

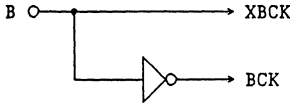
Cell Name
SDH

Equivalent Circuit



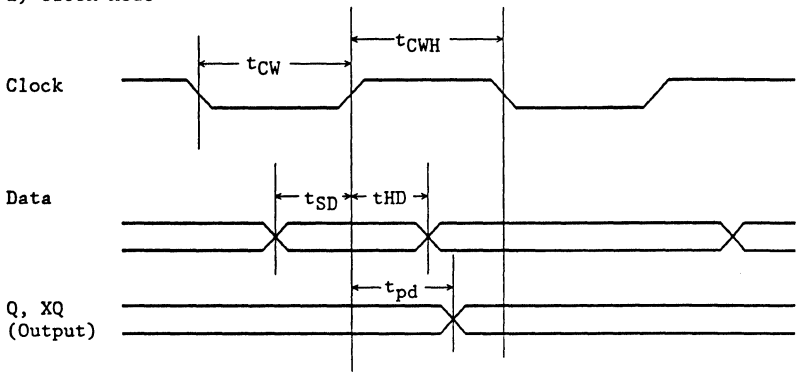




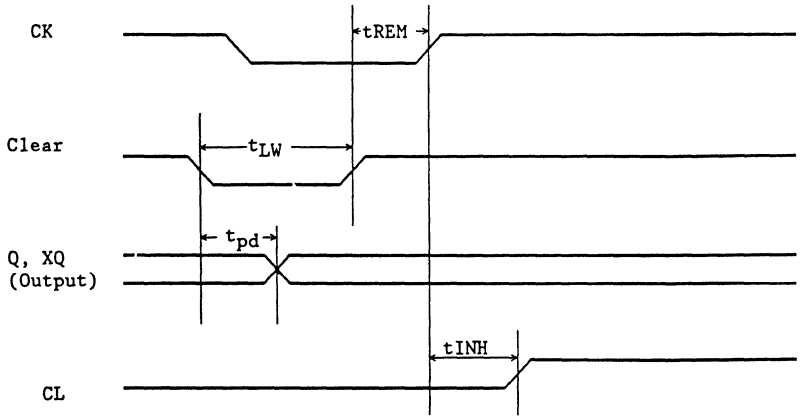


Definitions of Parameters

i) Clock Mode

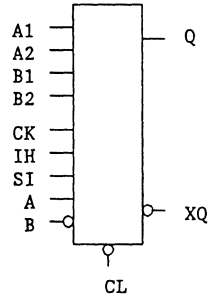


ii) Clear Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SDJ	SCAN 4-input DFF with Clear & Clock-Inhibit	15

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.20	0.07	2.42	0.03	0.07	7	CK,IH → Q
1.89	0.07	1.71	0.05	0.10	7	CK,IH → XQ
2.99	0.07	0.85	0.03	0.07	7	CL → Q, XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.4
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	3.6
Data Hold Time	tHD	0.7
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	2.4
Clear Hold Time	tINH	1.2

Pin Name	Input Loading Factor (ℓu)
A1,A2	1
B1,B2	1
CK	1
IH	1
CL	3
SI	1
A,B	2

Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

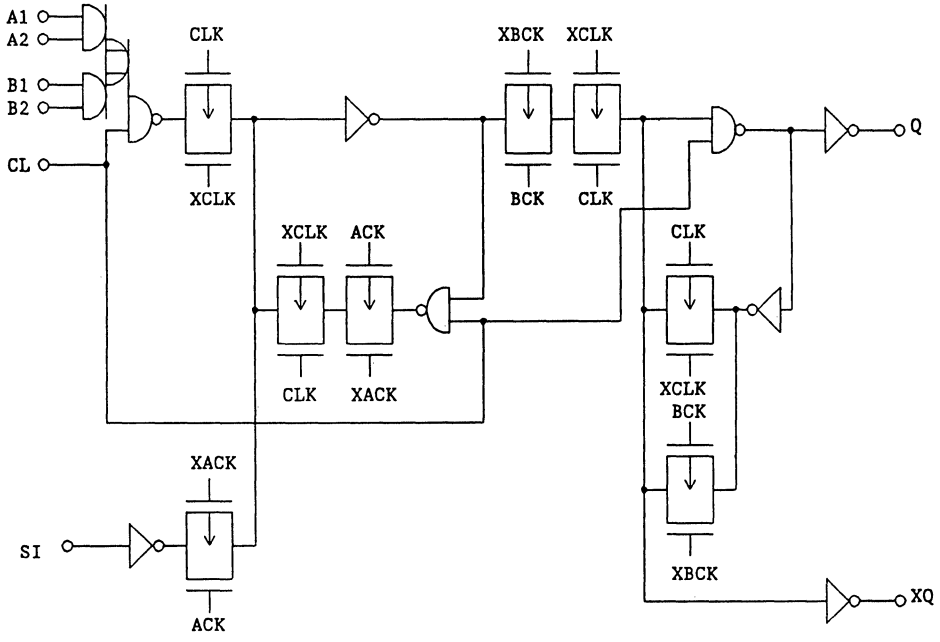
Function Table

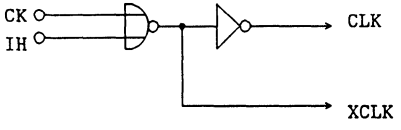
MODE	INPUT						OUTPUT	
	CLK	CL	D	A	B	SI	Q	XQ
CLEAR	X	L	X	X	X	X	L	H
CLOCK	L→H	H	Di	L	L	X	Di	$\overline{Di}$
	H	H	X	L	L	X	Q_0	XQ_0
SCAN	H	H	X	L→H→L	H	Si	Q_0	XQ_0
	H	H	X	L	H→L→H	X	Si	$\overline{Si}$

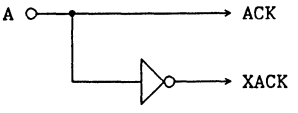
Note : CLK = CK + IH
D = (A1 x A2) + (B1 x B2)

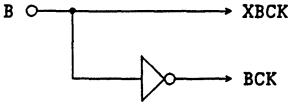
Cell Name
SDJ

Equivalent Circuit



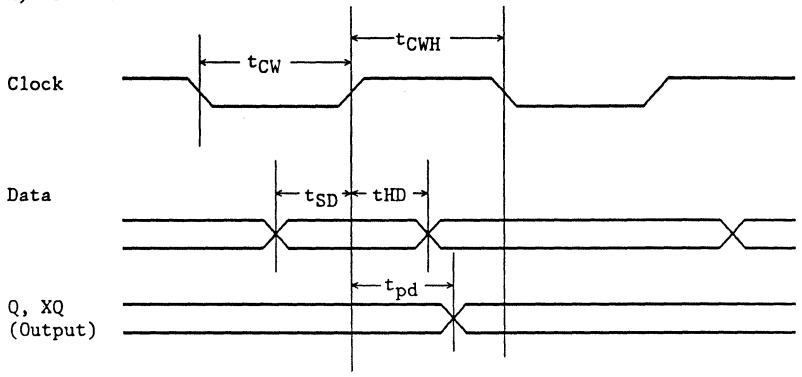






Definitions of Parameters

i) Clock Mode



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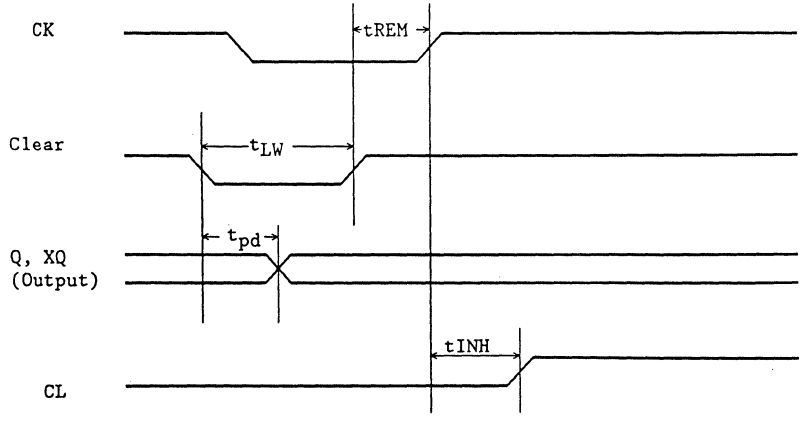
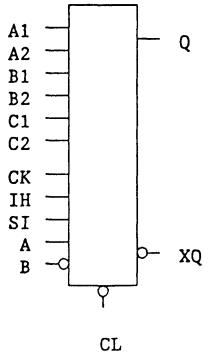
ii) Clear Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SDK	SCAN 6-input DFF with Clear & Clock-Inhibit	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.96	0.07	2.40	0.03	0.07	7	CK,IH → Q
1.86	0.07	1.73	0.05	0.10	7	CK,IH → XQ
2.99	0.07	0.82	0.03	0.07	7	CL → Q, XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.4
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	4.0
Data Hold Time	tHD	0.4
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	2.4
Clear Hold Time	tINH	1.2

Pin Name	Input Loading Factor (Lu)
A1,A2	1
B1,B2	1
C1,C2	1
CK	1
IH	1
CL	3
SI	1
A,B	2

Pin Name	Output Driving Factor (Lu)
Q	36
XQ	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

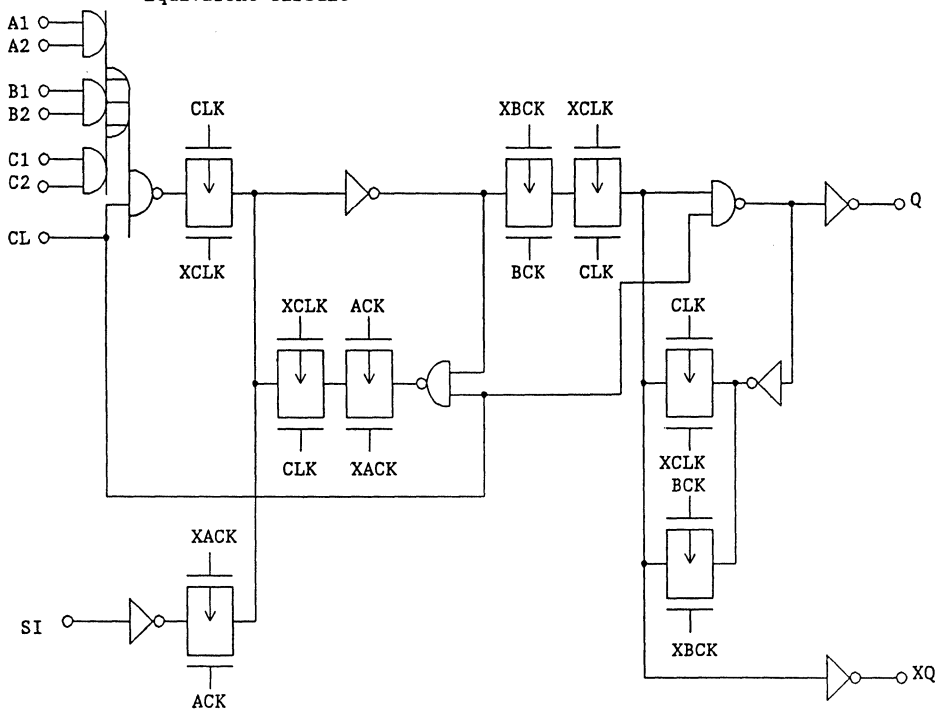
Function Table

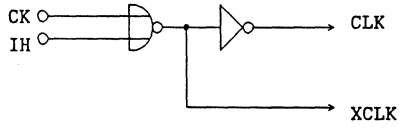
MODE	INPUT						OUTPUT	
	CLK	CL	D	A	B	SI	Q	XQ
CLEAR	X	L	X	X	X	X	L	H
CLOCK	L→H	H	Di	L	L	X	Di	$\overline{Di}$
	H	H	X	L	L	X	Q_0	XQ_0
SCAN	H	H	X	L→H→L	H	Si	Q_0	XQ_0
	H	H	X	L	H→L→H	X	Si	$\overline{Si}$

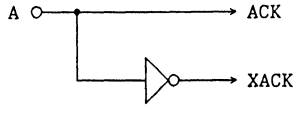
Note : CLK = CK + IH
D = (A1 x A2) + (B1 x B2) + (C1 x C2)

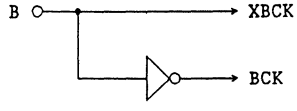
Cell Name
SDK

Equivalent Circuit



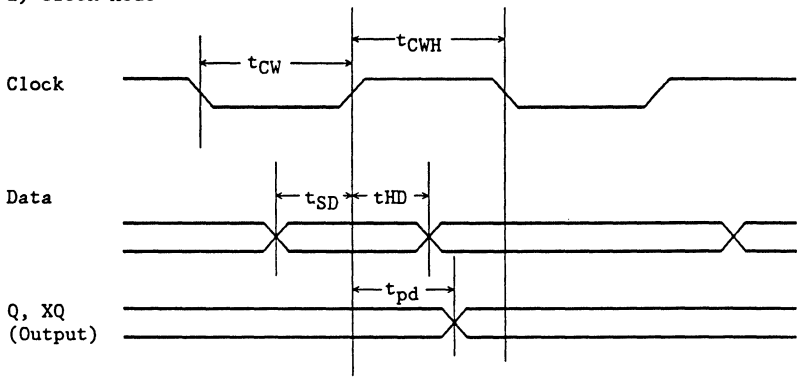




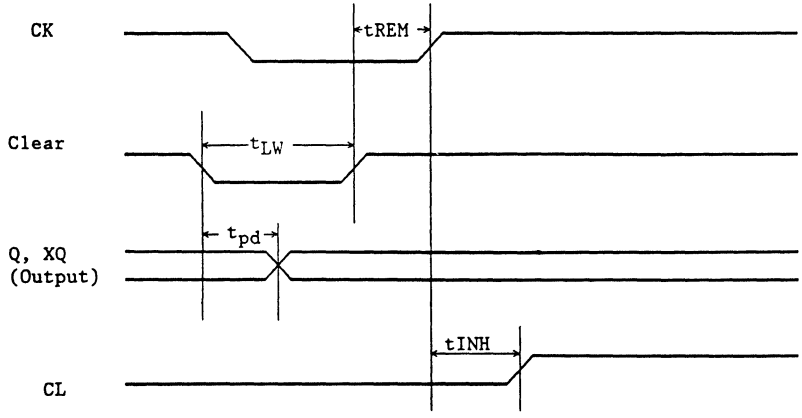


Definitions of Parameters

i) Clock Mode

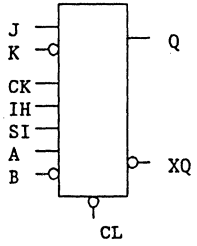


ii) Clear Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SJH	SCAN J-K FF with Clear & Clock-Inhibit	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.39	0.07	2.70	0.03	0.07	7	CK,IH → Q
1.89	0.07	1.73	0.05	0.10	7	CK,IH → XQ
3.01	0.07	1.11	0.03	0.07	7	CL → Q, XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.4
Clock Pause Time	tCWH	4.0
Data Setup Time (J)	tSD	3.6
Data Setup Time (K)	tSD	3.9
Data Hold Time (J,K)	tHD	0.4
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	2.4
Clear Hold Time	tINH	1.2

Pin Name	Input Loading Factor (ℓu)
J,K	1
CK	1
IH	1
CL	3
SI	1
A,B	2

Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

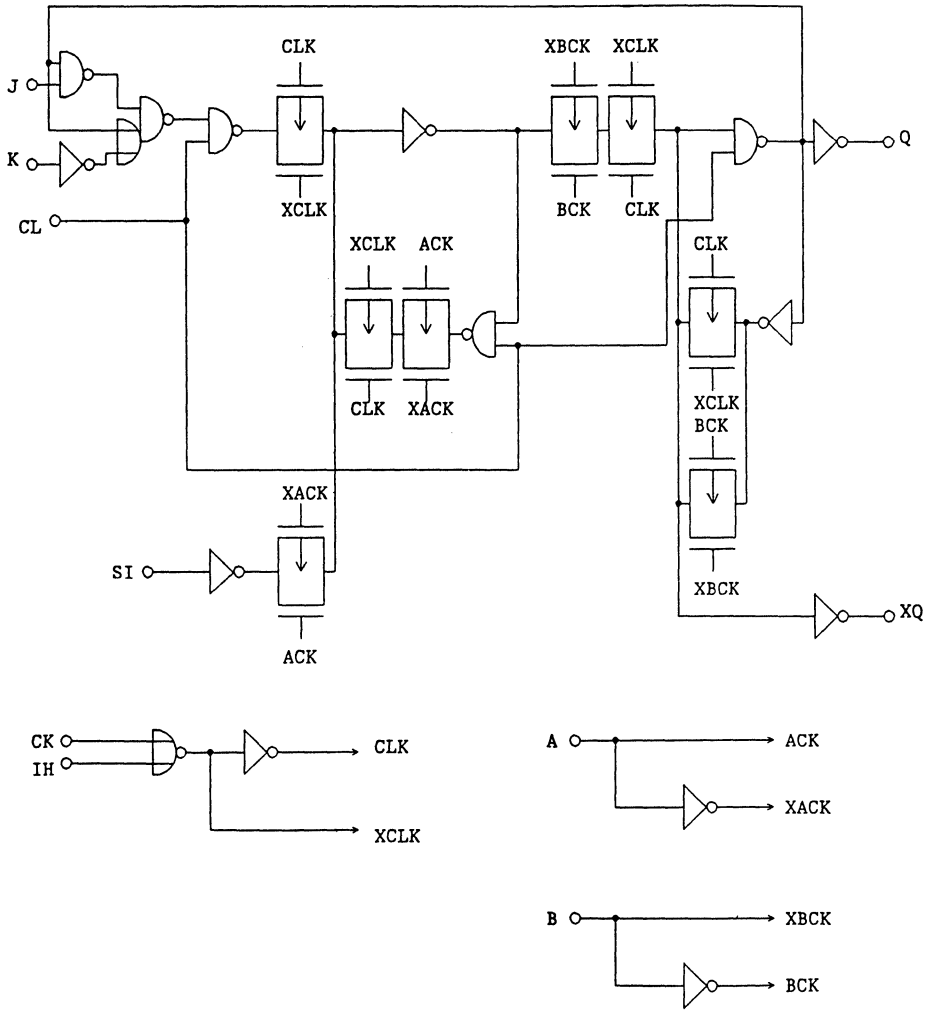
Function Table

MODE	INPUT							OUTPUT	
	CLK	CL	J	K	A	B	SI	Q	XQ
CLEAR	X	L	X	X	X	X	X	L	H
CLOCK	L→H	H	L	L	L	L	X	L	H
	L→H	H	H	H	L	L	X	H	L
	L→H	H	L	H	L	L	X	Q_0	XQ_0
	L→H	H	H	L	L	L	X	XQ_0	Q_0
	H	H	X	X	L	L	X	Q_0	XQ_0
SCAN	H	H	X	X	L→H→L	H	Si	Q_0	XQ_0
	H	H	X	X	L	H→L→H	X	Si	$\overline{Si}$

Note : CLK = CK + IH

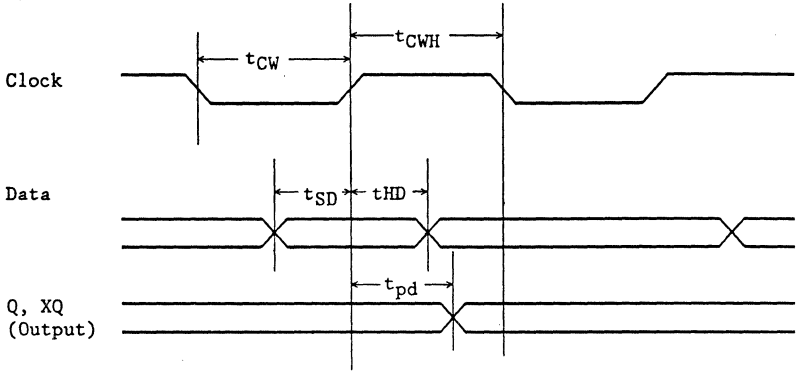
Cell Name
SJH

Equivalent Circuit

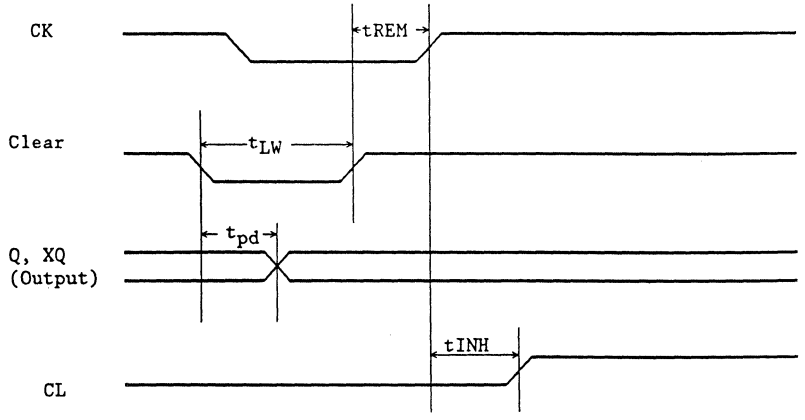


Definitions of Parameters

i) Clock Mode

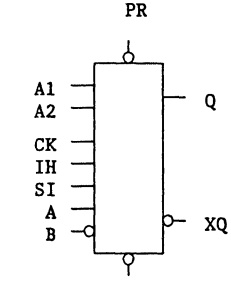


ii) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SDD	SCAN 2-input DFF with Clear, Preset & Clock-Inhibit	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.96	0.07	2.58	0.03	0.07	7	CK,IH → Q
2.12	0.07	1.71	0.05	0.10	7	CK,IH → XQ
3.60	0.07	0.82	0.03	0.07	7	CL → Q, XQ
3.07	0.07	1.88	0.05	0.10	7	PR → Q, XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.4
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	4.4
Data Hold Time	tHD	0.8
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	2.4
Clear Hold Time	tINH	1.2
Preset Pulse Width	tPW	5.5
Preset Release Time	tREM	3.0
Preset Hold Time	tINH	0.8

Pin Name	Input Loading Factor (ℓu)
A1,A2	1
CK	1
IH	1
CL	3
PR	3
SI	1
A,B	2

Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

MODE	INPUT							OUTPUT	
	CLK	CL	PR	D	A	B	SI	Q	XQ
CLEAR	X	L	H	X	X	X	X	L	H
PRESET	X	H	L	X	X	X	X	H	L
CLOCK	L→H	H	H	Di	L	L	X	Di	$\overline{Di}$
	H	H	H	X	L	L	X	Q_0	XQ_0
SCAN	H	H	H	X	L→H→L	H	Si	Q_0	XQ_0
	H	H	H	X	L	H→L→H	X	Si	$\overline{Si}$
CL/PR	X	L	L	X	X	X	X	Prohibited	

Note : CLK = CK + IH
D = A1 x A2

AU-SDD-E4	Sheet 1/4	Page 11-13

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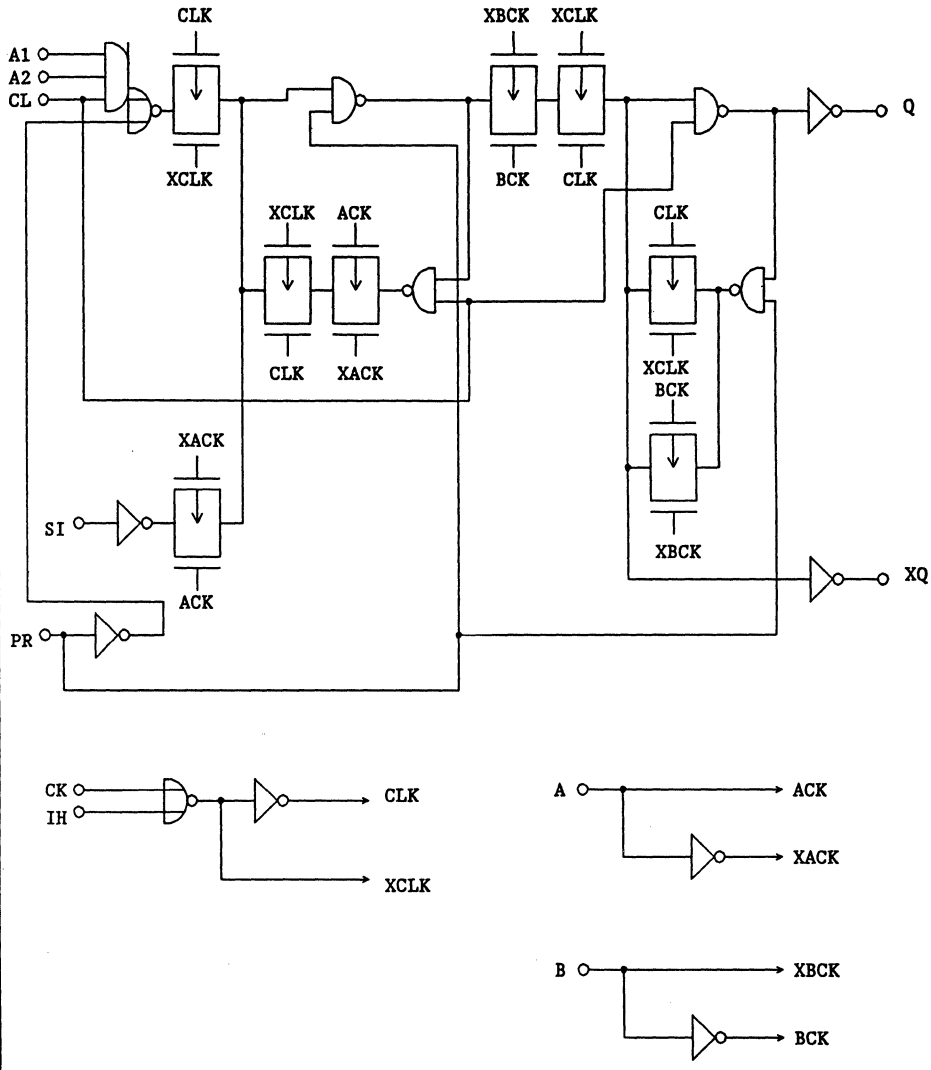
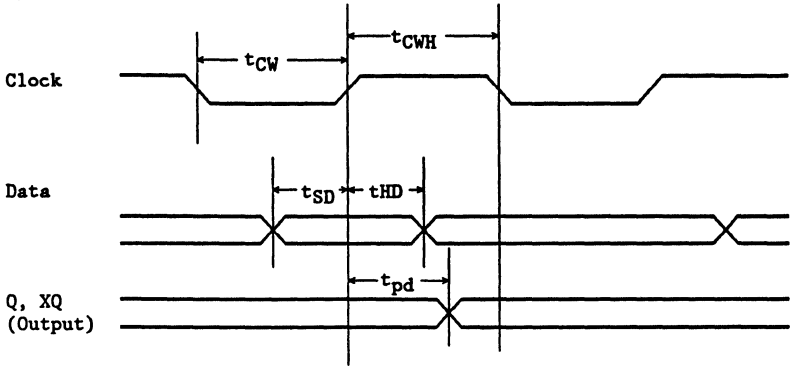
Cell Name
SDD

Equivalent Circuit

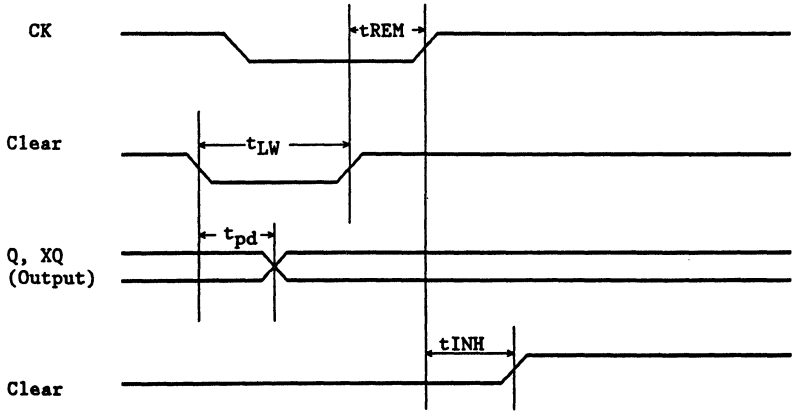


Definitions of Parameters

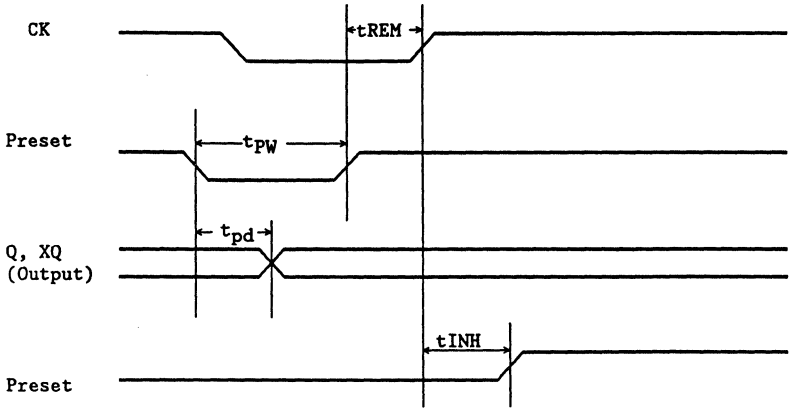
i) Clock Mode



ii) Clear Mode

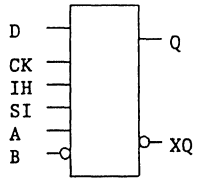


iii) Preset Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SDA	SCAN 1-input DFF with Clock-Inhibit	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.55	0.07	2.40	0.03	0.07	7	CK,IH → Q
1.87	0.07	1.74	0.05	0.10	7	CK,IH → XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.4
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	2.8
Data Hold Time	tHD	1.2

Pin Name	Input Loading Factor (ℓu)
D	1
CK	1
IH	1
SI	1
A,B	2

Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

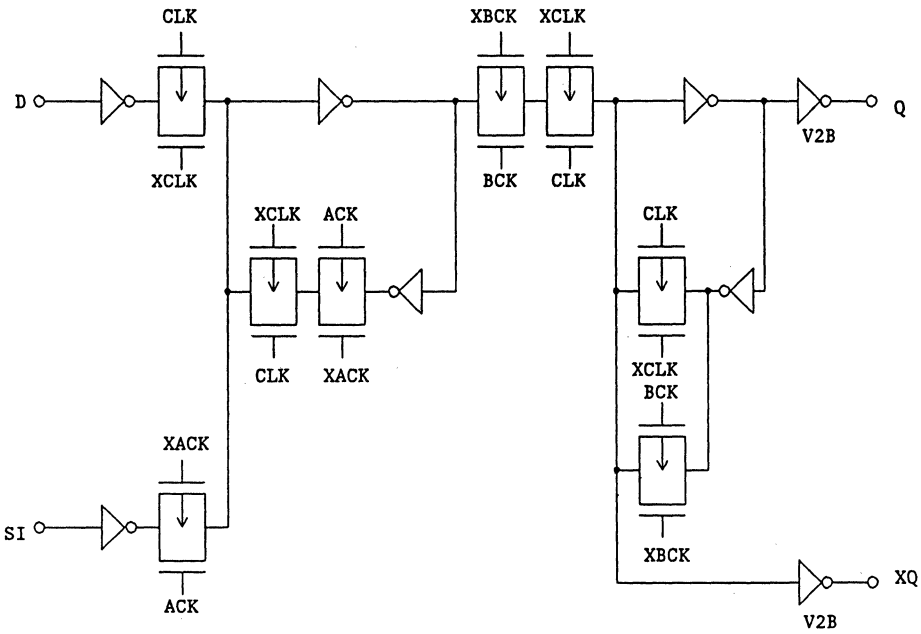
Function Table

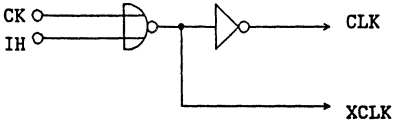
MODE	INPUT					OUTPUT	
	CLK	D	A	B	SI	Q	XQ
CLOCK	L→H	Di	L	L	X	Di	$\overline{Di}$
	H	X	L	L	X	Q_0	XQ_0
SCAN	H	X	L→H→L	H	Si	Q_0	XQ_0
	H	X	L	H→L→H	X	Si	$\overline{Si}$

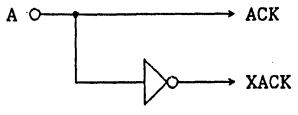
Note : CLK = CK + IH

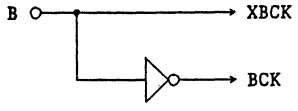
Cell Name
SDA

Equivalent Circuit



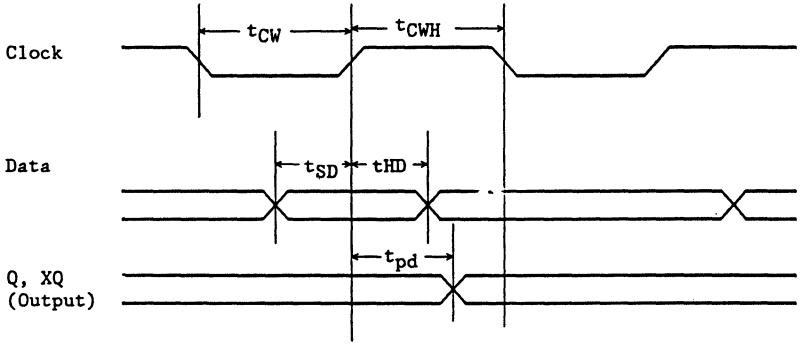






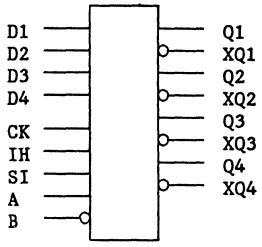
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SDB	SCAN 1-input 4-bit DFF with Clock-Inhibit	42

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.39	0.07	3.15	0.03	0.07	7	CK,IH → Q
2.60	0.07	2.66	0.05	0.10	7	CK,IH → XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	5.5
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	1.8
Data Hold Time	tHD	2.7

Pin Name	Input Loading Factor (ℓu)
D	1
CK	1
IH	1
SI	1
A,B	2

Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

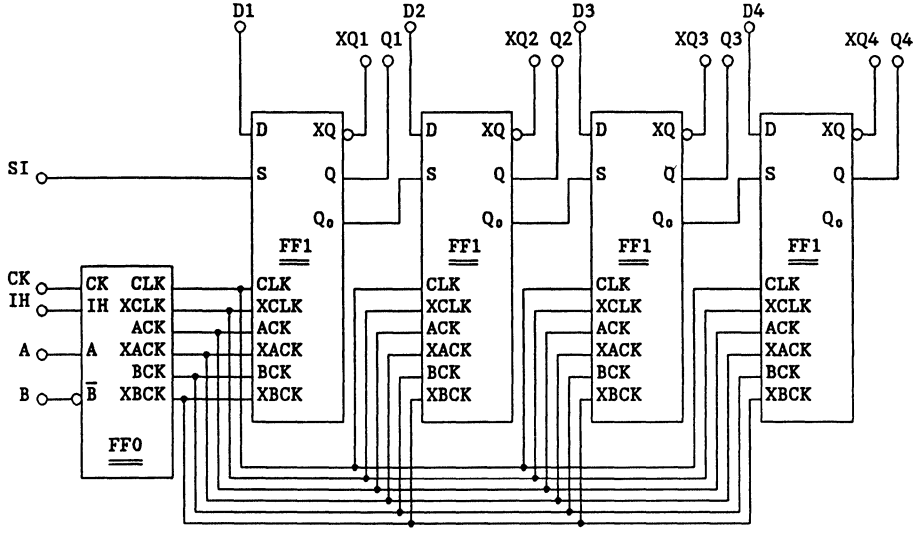
Function Table

MODE	INPUT					OUTPUT	
	CLK	Dn	A	B	SI,Qn-1	Qn	XQn
CLOCK	L→H	Di	L	L	X	Di	$\overline{Di}$
	H	X	L	L	X	Qn°	XQn°
SCAN	H	X	L→H→L	H	Si	Qn°	XQn°
	H	X	L	H→L→H	X	Si	$\overline{Si}$

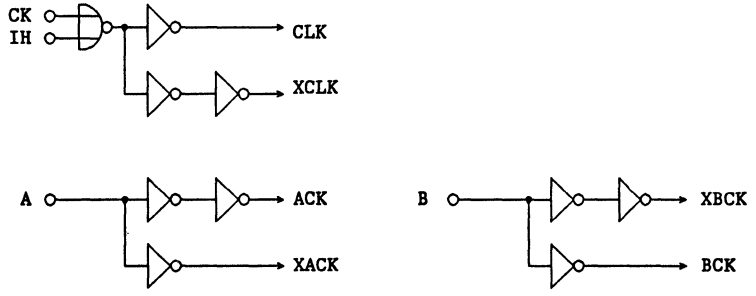
Note : CLK = CK + IH
n = 1 ~ 4

Cell Name
SDB

Equivalent Circuit

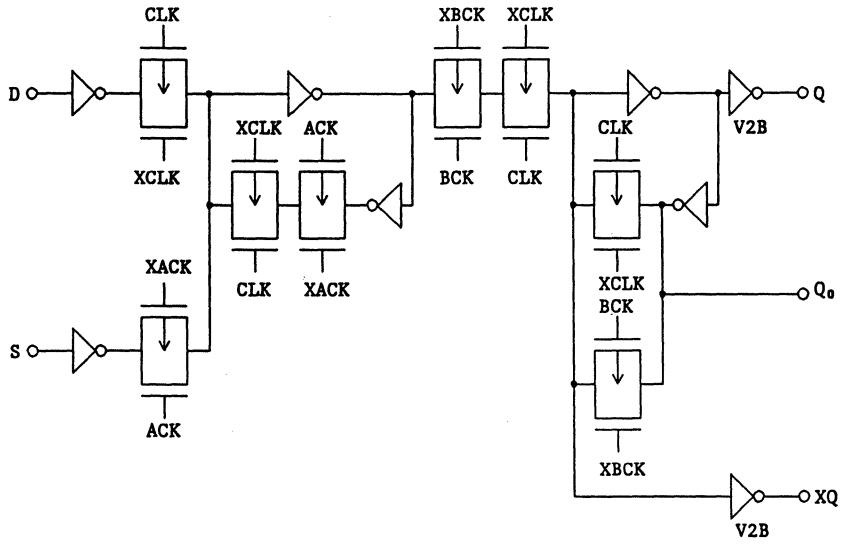


Equivalent Circuit (FF0)



Cell Name
SDB

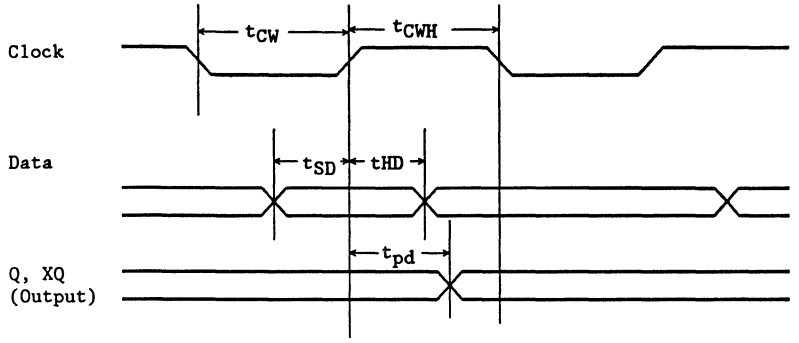
Equivalent Circuit (FF1)



2

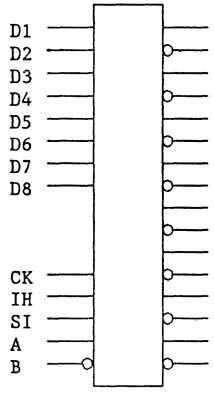
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SHA	SCAN 1-input 8-bit DFF with Clock-Inhibit	68

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.78	0.13	3.78	0.07	0.08	4	CK,IH → Q
3.30	0.13	3.20	0.11	0.15	4	CK,IH → XQ

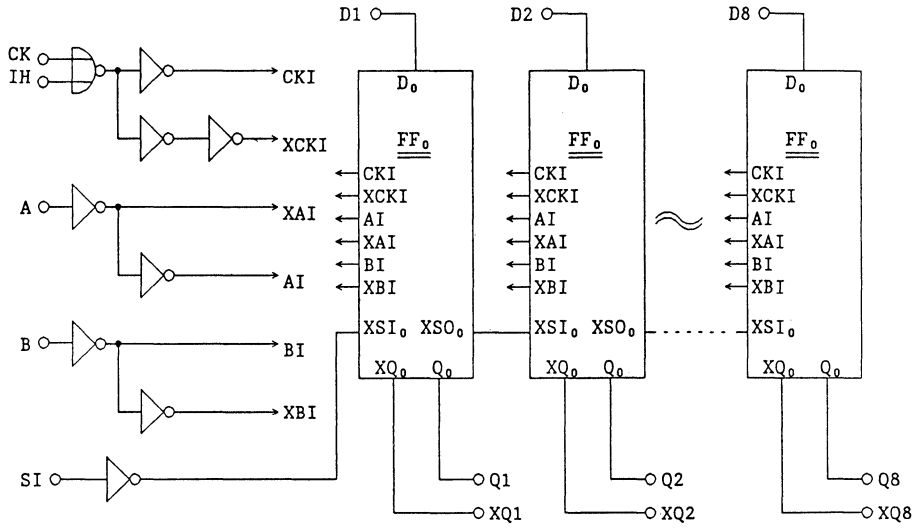
Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	5.8
Clock Pause Time	tCWH	4.4
Data Setup Time	tSD	1.5
Data Hold Time	tHD	2.7

Pin Name	Input Loading Factor (ℓu)
D	1
CK	1
IH	1
SI	1
A	1
B	1

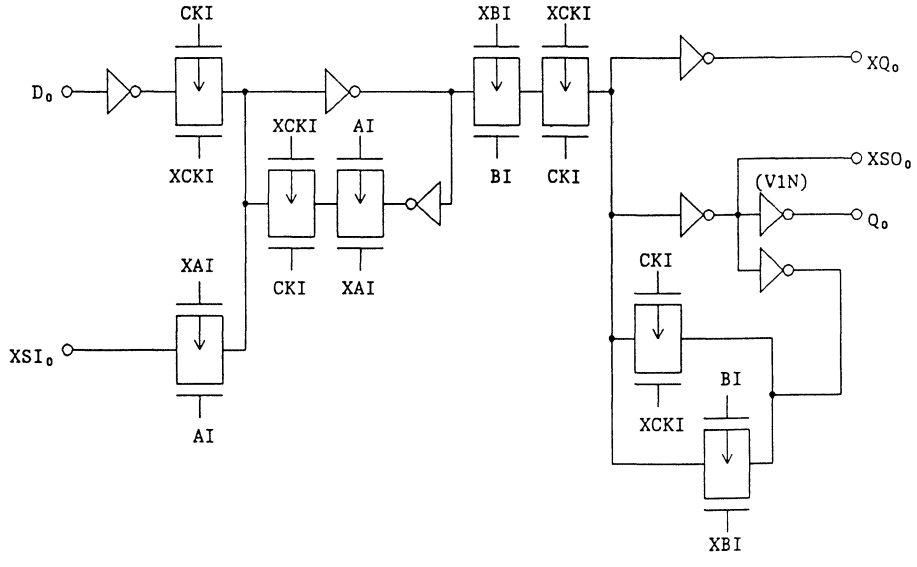
Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



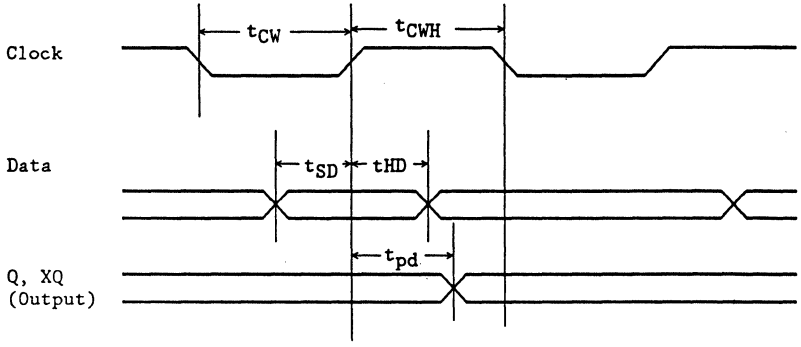
Equivalent Circuit (FF_0)



2

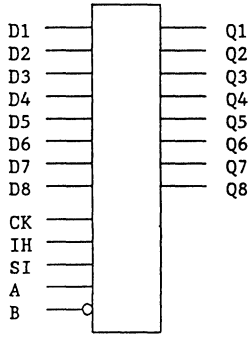
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SHB	SCAN 1-input 8-bit DFF with Clock-Inhibit & Q Output	62

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.46	0.13	3.54	0.07	0.08	4	CK,IH → Q

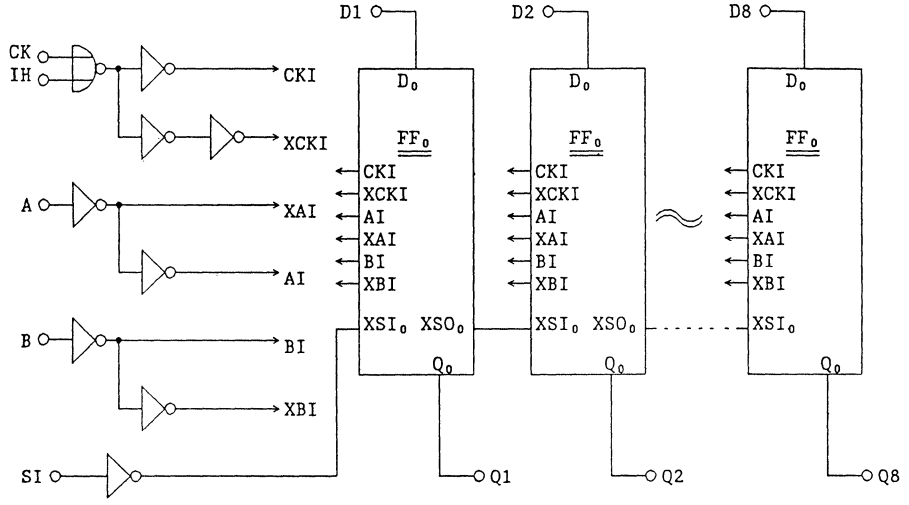
Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	5.8
Clock Pause Time	tCWH	4.4
Data Setup Time	tSD	1.6
Data Hold Time	tHD	2.7

Pin Name	Input Loading Factor (ℓu)
D	1
CK	1
IH	1
SI	1
A	1
B	1

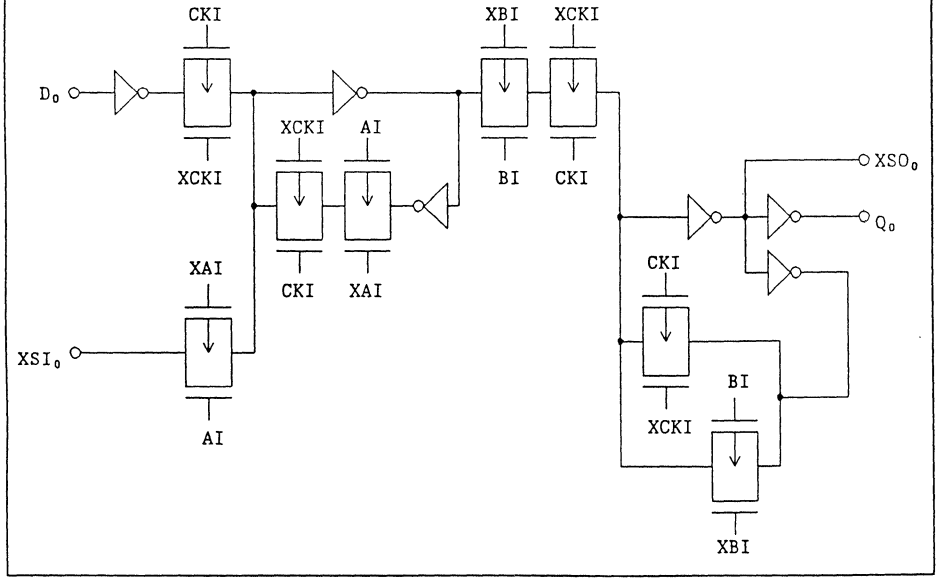
Pin Name	Output Driving Factor (ℓu)
Q	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit

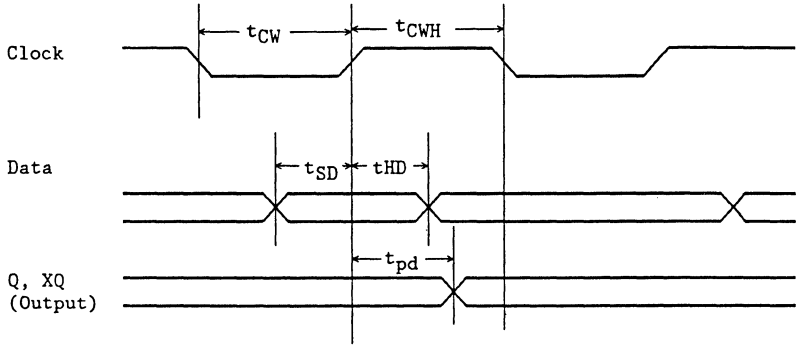


Equivalent Circuit (FF_0)



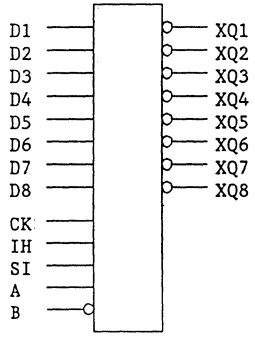
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SHC	SCAN 1-input 8-bit DFF with Clock-Inhibit & XQ Output	62

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.35	0.13	3.28	0.11	0.15	4	CK,IH → XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	5.8
Clock Pause Time	tCWH	4.4
Data Setup Time	tSD	1.6
Data Hold Time	tHD	2.7

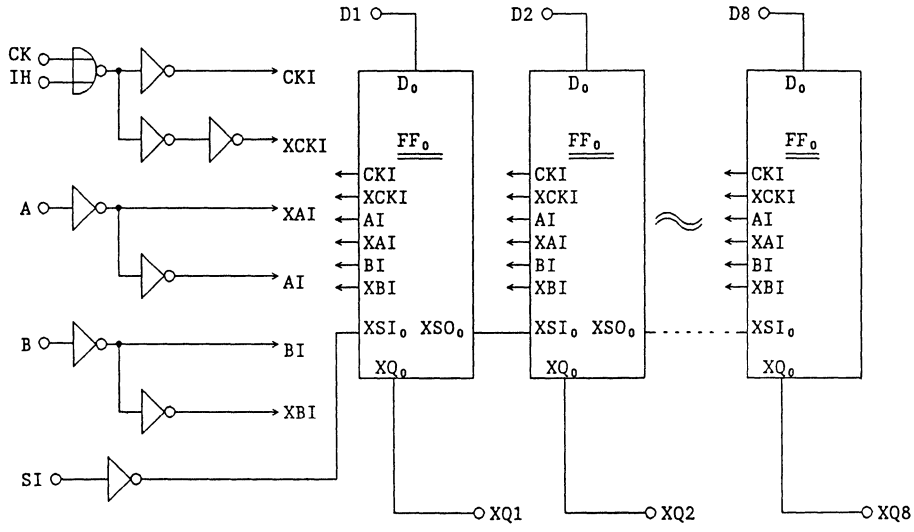
Pin Name	Input Loading Factor (ℓu)
D	1
CK	1
IH	1
SI	1
A	1
B	1

Pin Name	Output Driving Factor (ℓu)
XQ	18

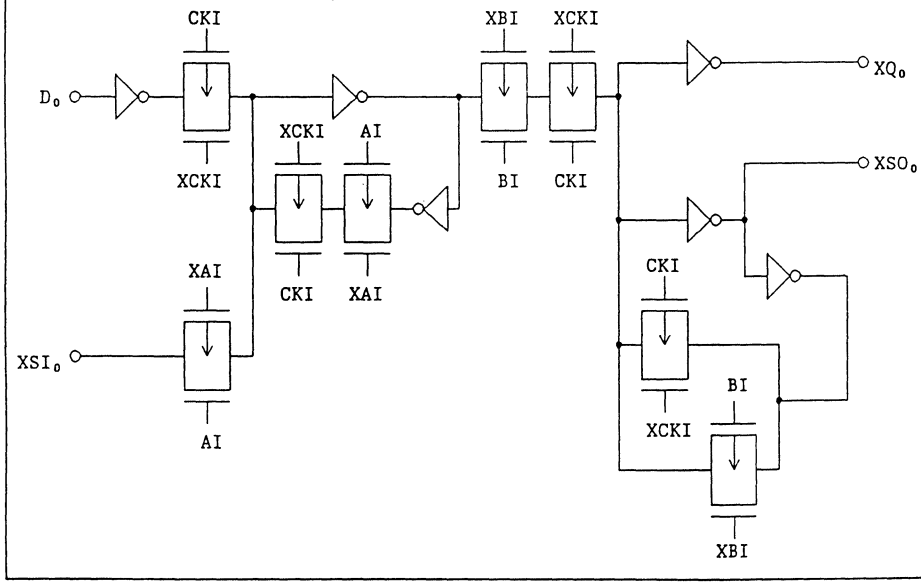
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name
SHC

Equivalent Circuit



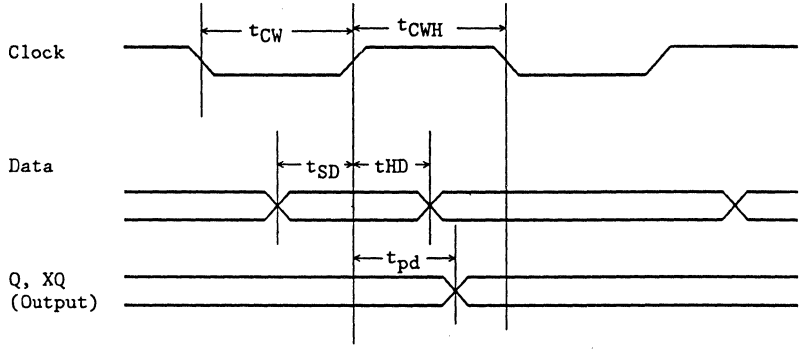
Equivalent Circuit (FF_0)



2

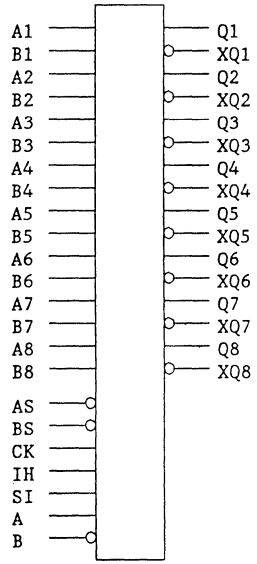
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SHJ	SCAN 8-bit DFF with Clock-Inhibit & 2-to-1 Data Multiplexer	78

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.86	0.13	3.87	0.07	0.10	4	CK,IH → Q
3.30	0.13	3.20	0.09	0.16	4	CK,IH → XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	5.8
Clock Pause Time	tCWH	4.4
Data Setup Time	tSD	2.4
Data Hold Time	tHD	2.5

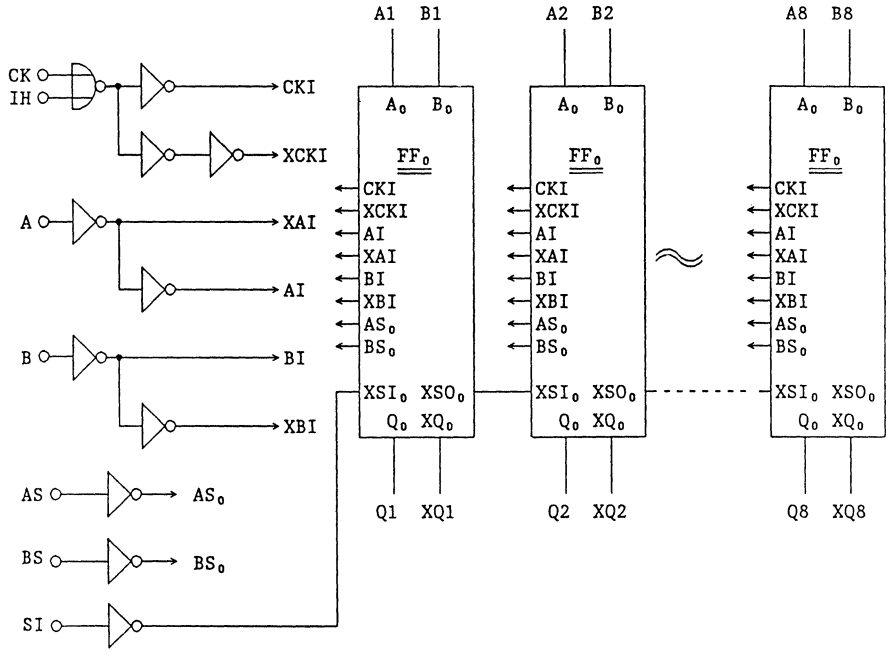
Pin Name	Input Loading Factor (ℓu)
An,Bn (n=1~8)	1
AS,BS	1
CK	1
IH	1
SI	1
A,B	1

Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

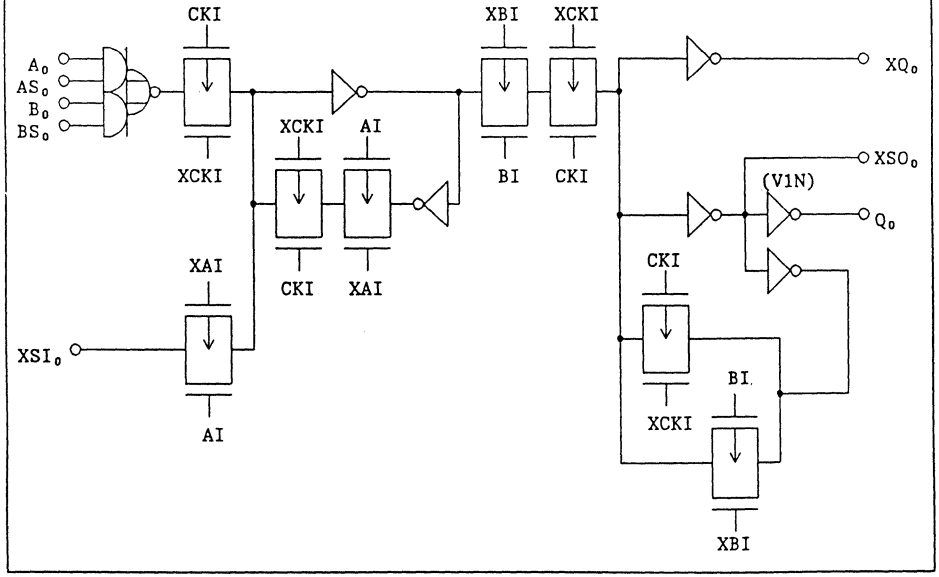
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name
SHJ

Equivalent Circuit

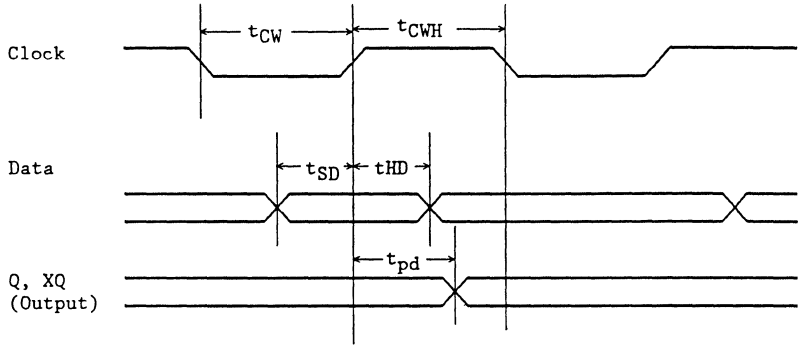


Equivalent Circuit (FF_0)



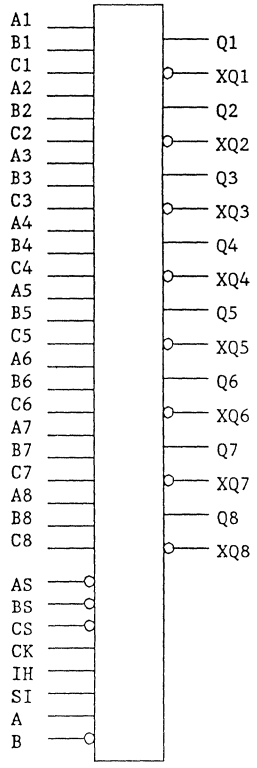
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SHK	SCAN 8-bit DFF with Clock-Inhibit & 3-to-1 Data Multiplexer	88

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.71	0.13	3.68	0.07	0.08	4	CK,IH → Q
3.27	0.13	3.20	0.11	0.15	4	CK,IH → XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	5.8
Clock Pause Time	tCWH	4.4
Data Setup Time	tSD	3.1
Data Hold Time	tHD	2.4

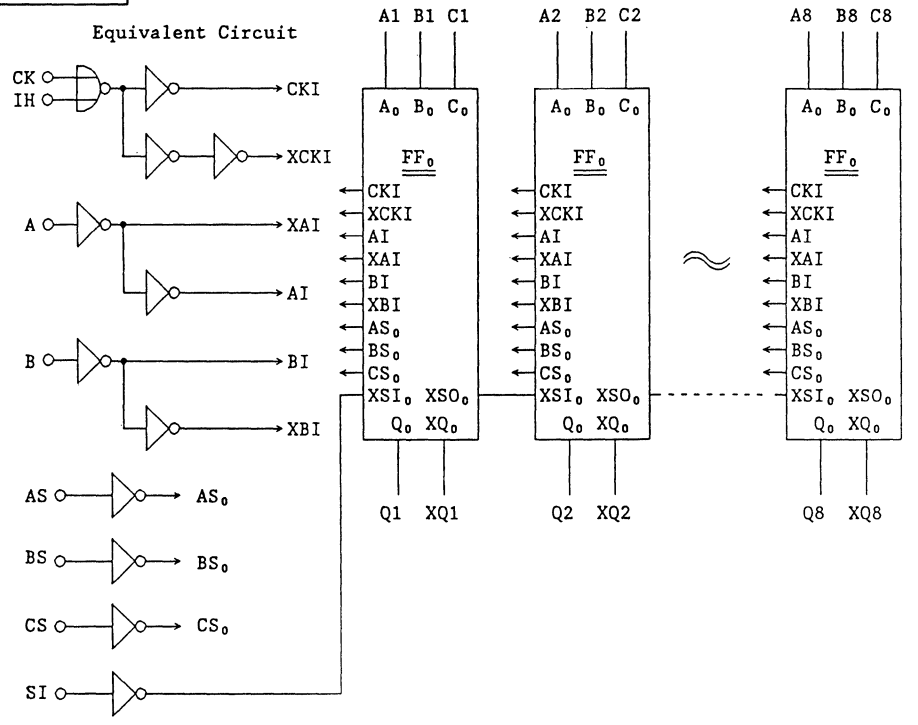
Pin Name	Input Loading Factor (ℓu)
An,Bn,Cn (n=1~8)	1
AS,BS,CS	1
CK	1
IH	1
SI	1
A,B	1

Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

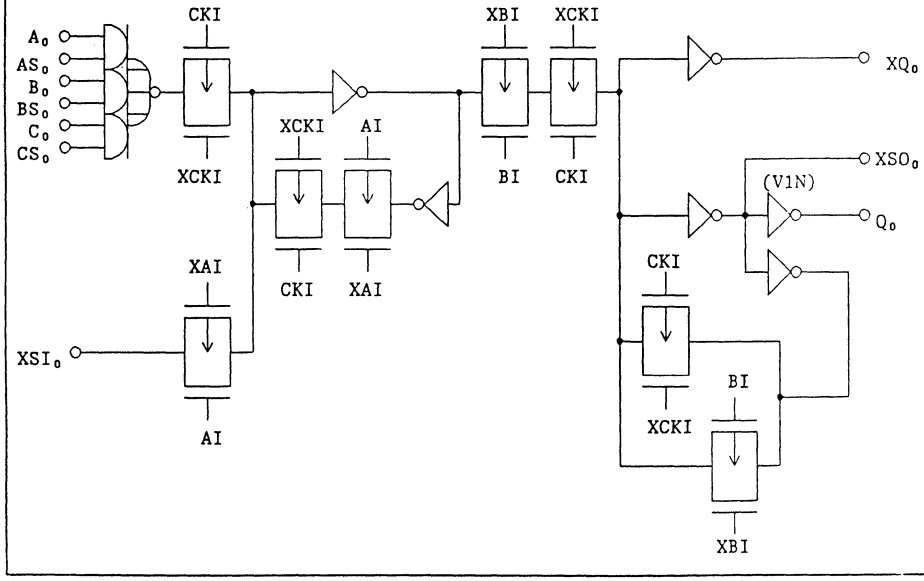
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name
SHK

Equivalent Circuit



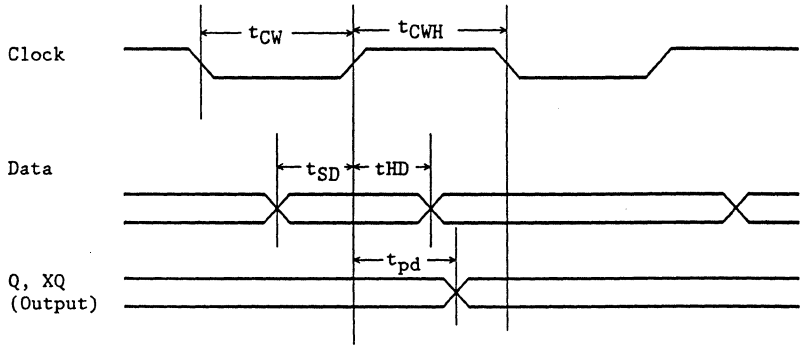
Equivalent Circuit (FF_0)



2

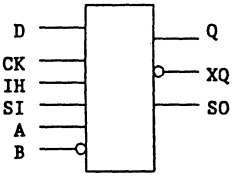
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SFDM	SCAN 1-input DFF with Clock-Inhibit	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.85	0.13	1.90	0.08	0.14	4	CK → Q
2.35	0.13	2.31	0.07	0.08	4	CK → XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	1.3
Data Hold Time	tHD	1.1

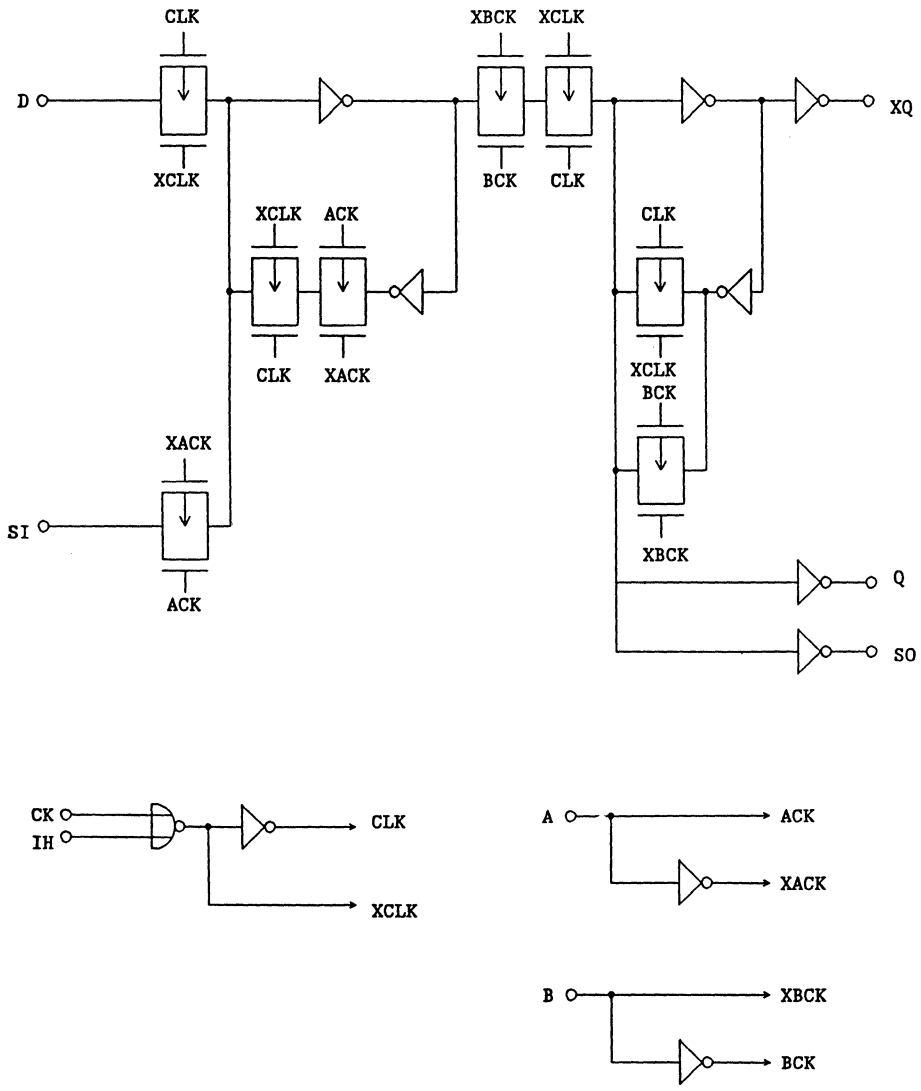
Pin Name	Input Loading Factor (ℓu)
D	2
CK	1
IH	1
SI	2
A,B	2

Pin Name	Output Driving Factor (ℓu)
Q	18
SO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

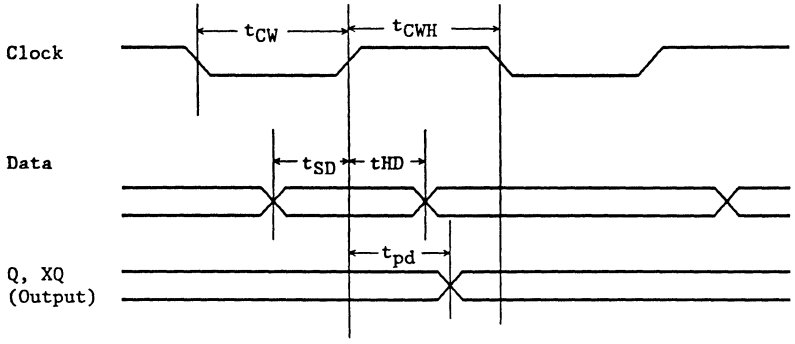
Cell Name
SFDM

Equivalent Circuit



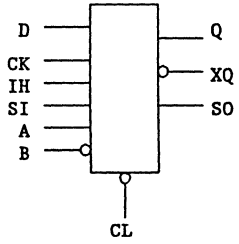
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SFDO	SCAN 1-input DFF with Clear and Clock Inhibit	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.14	0.14	2.04	0.09	0.15	4	CK → Q
2.37	0.13	2.62	0.07	0.08	4	CK → XQ
2.51	0.13	2.18	0.09	0.15	4	CL → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	2.1
Data Hold Time	tHD	1.4
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	1.6
Clear Hold Time	tINH	3.9

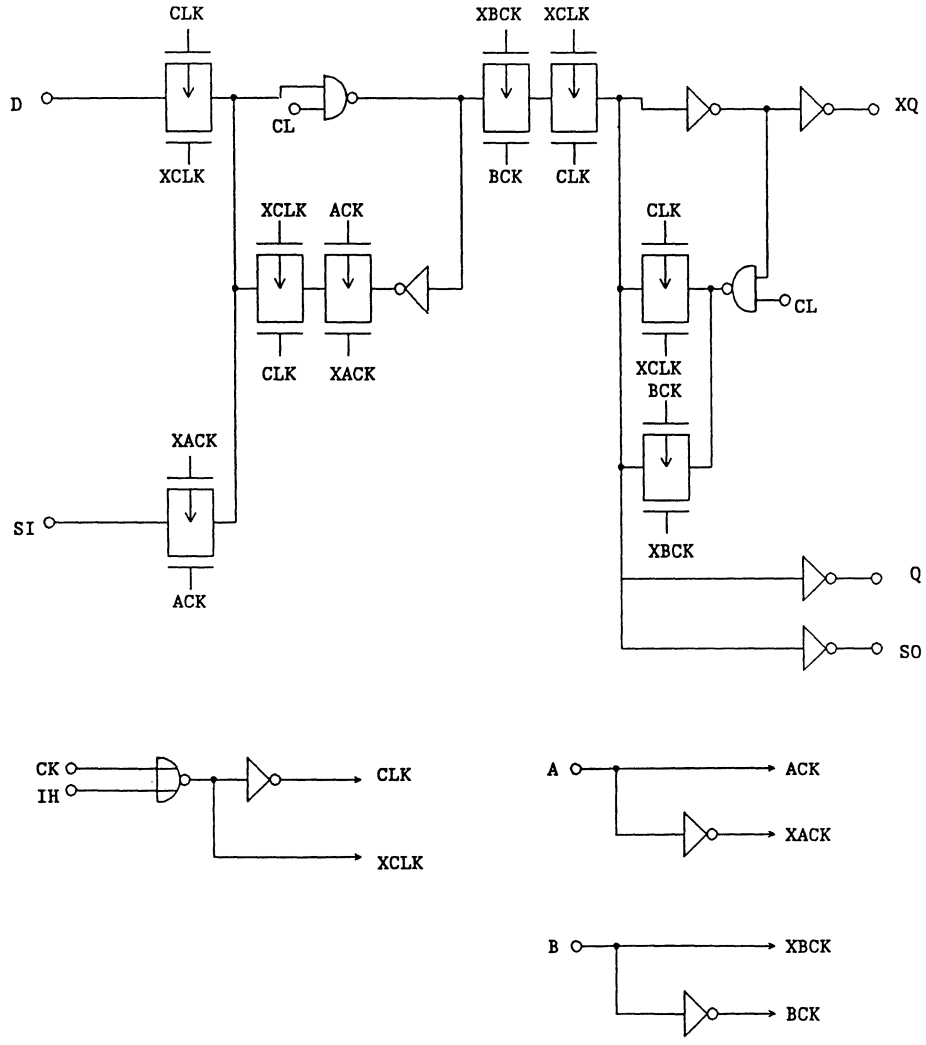
Pin Name	Input Loading Factor (ℓu)
D	2
CK,IH	1
SI	2
A,B	2
CL	2

Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18
SO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

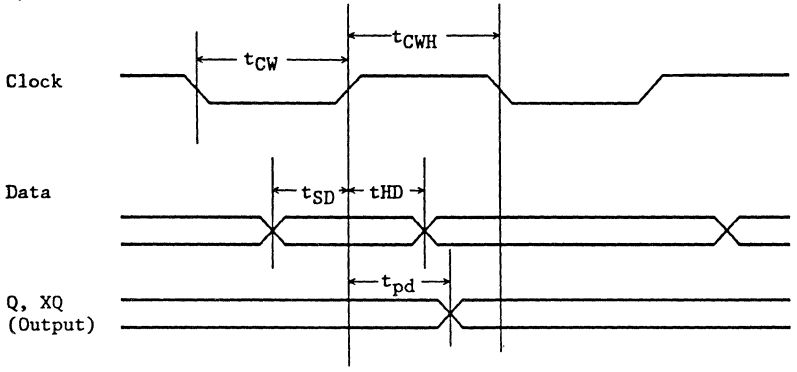
Cell Name
SFDO

Equivalent Circuit

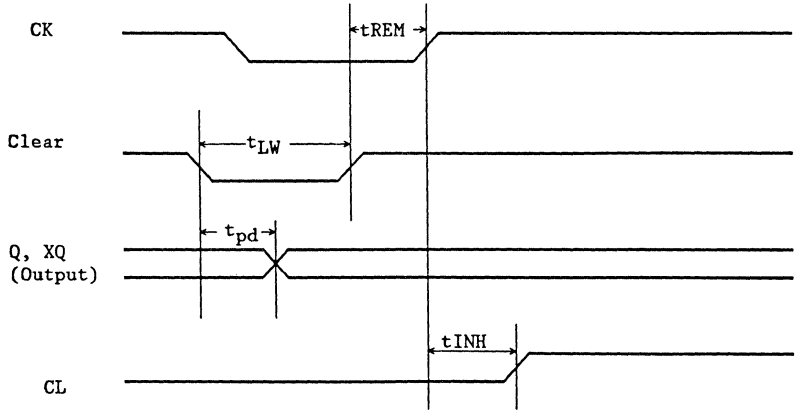


Definitions of Parameters

i) Clock Mode

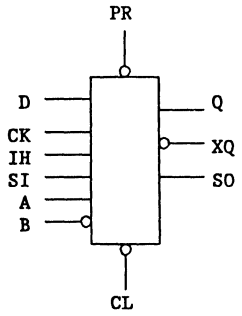


ii) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SFDP	SCAN 1-input DFF with Clear,Preset,and Clock Inhibit	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.16	0.14	2.03	0.09	0.15	4	CK → Q
2.86	0.13	2.62	0.07	0.08	4	CK → XQ
2.91	0.13	2.15	0.09	0.15	4	CL → Q,XQ
3.64	0.14	0.83	0.07	0.08	4	PR → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	2.1
Data Hold Time	tHD	1.4
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	1.6
Clear Hold Time	tINH	3.9
Preset Pulse Width	tPW	4.9
Preset Release Time	tREM	0.8
Preset Hold Time	tINH	4.9

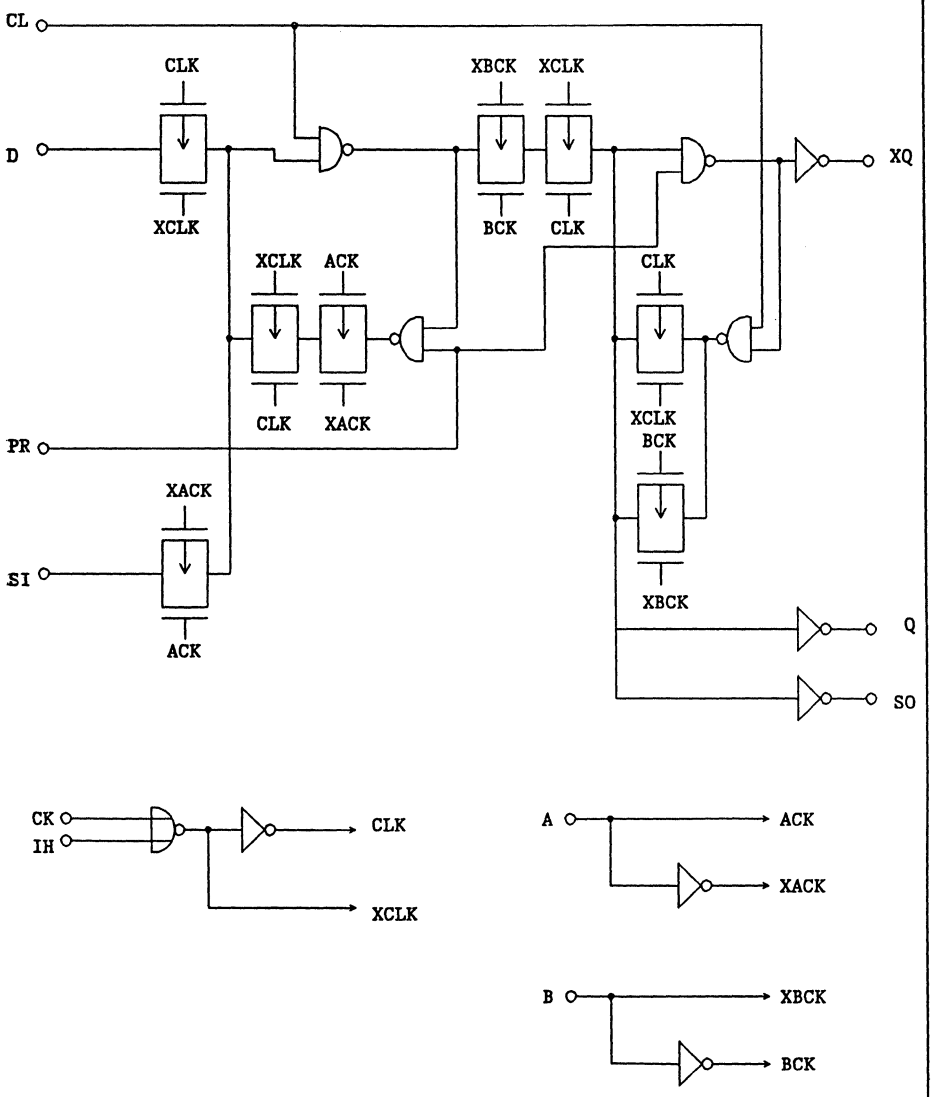
Pin Name	Input Loading Factor (ℓu)
D	2
CK,IH	1
SI	2
A,B	2
CL,PR	2

Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18
SO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

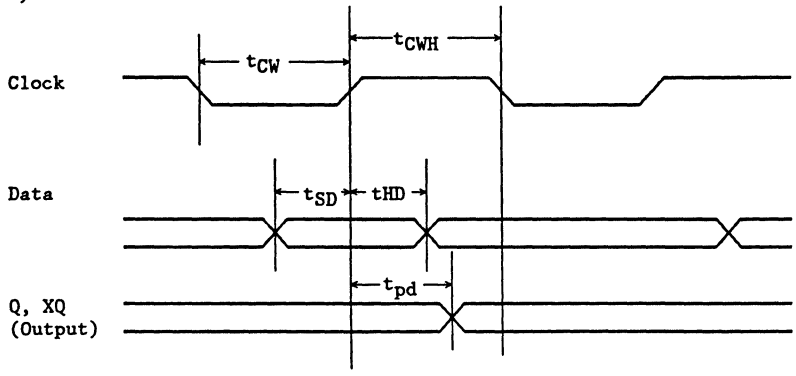
Cell Name
SFDP

Equivalent Circuit

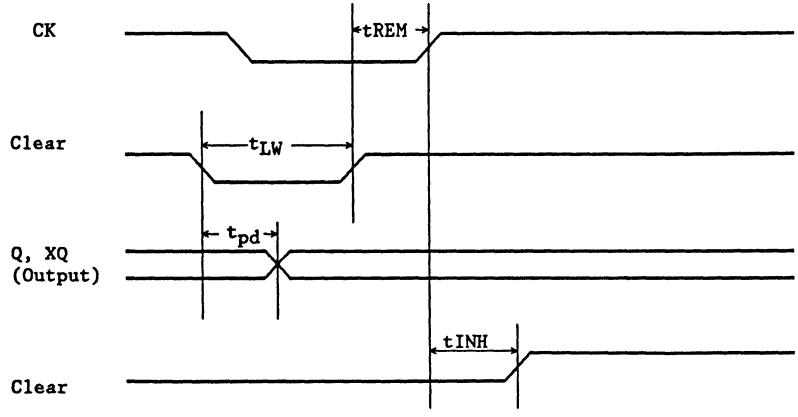


Definitions of Parameters

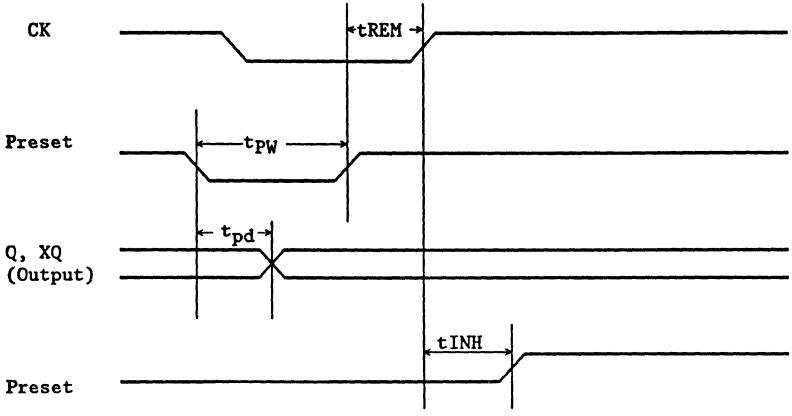
i) Clock Mode



ii) Clear Mode

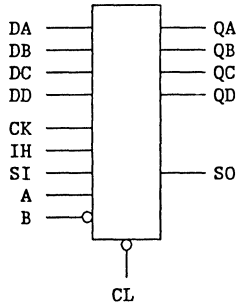


iii) Preset Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SFDR	SCAN 4-input DFF with Clear and Clock Inhibit	36

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.98	0.14	3.00	0.09	0.15	4	CK → Q
-	-	3.07	0.09	0.16	4	CL → Q

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.4
Data Steup Time	tSD	0.9
Data Hold Time	tHD	2.0
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	2.3
Clear Hold Time	tINH	4.6

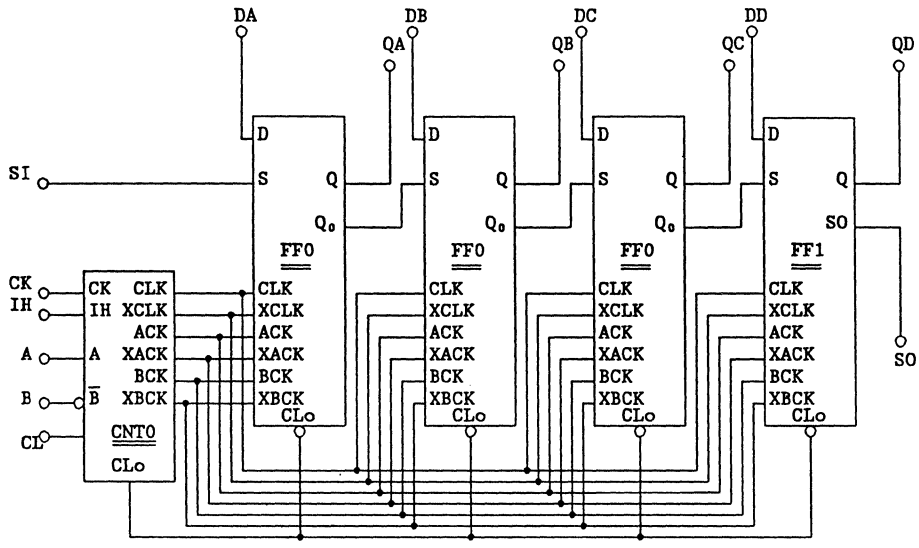
Pin Name	Input Loading Factor (ℓu)
D	2
CK,IH	1
SI	2
A,B	1
CL	1

Pin Name	Output Driving Factor (ℓu)
Q	18
SO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

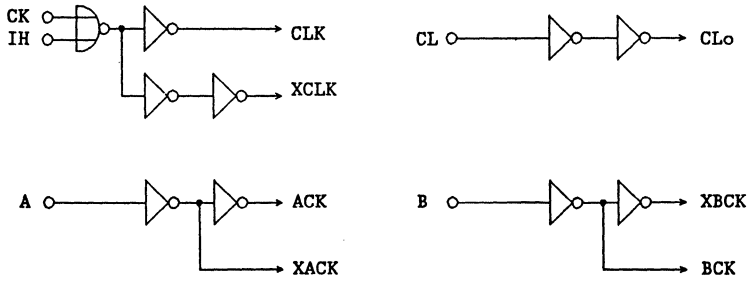
Cell Name
SFDR

Equivalent Circuit

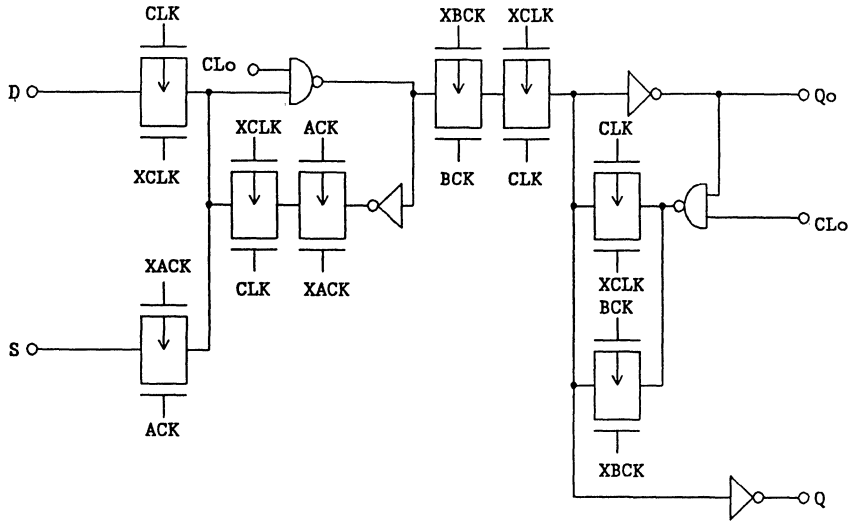


2

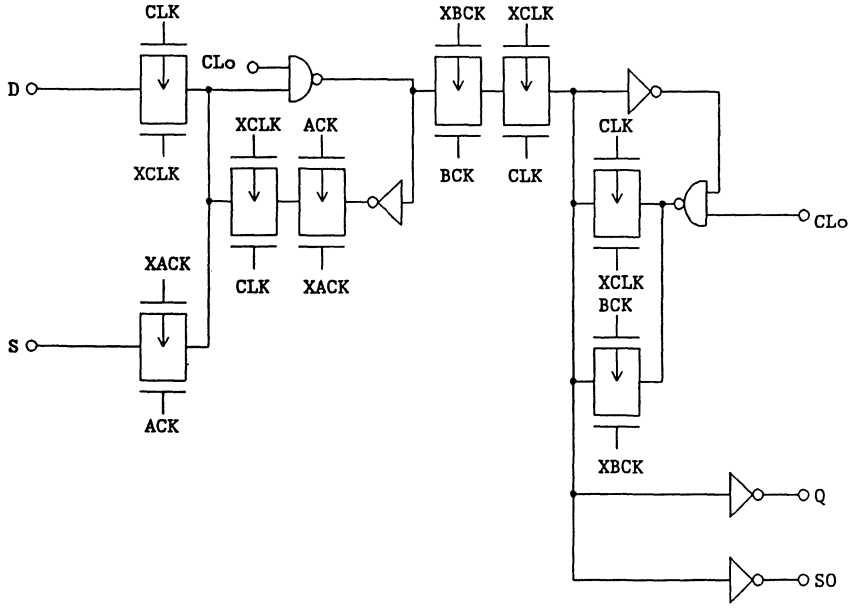
Equivalent Circuit (CNTO)



Equivalent Circuit (FF0)

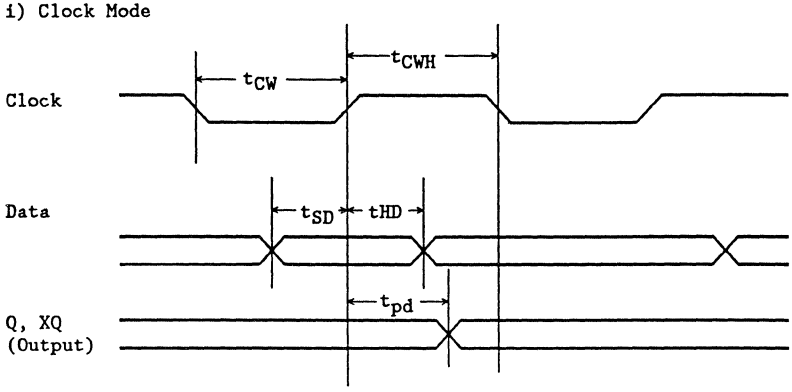


Equivalent Circuit (FF1)

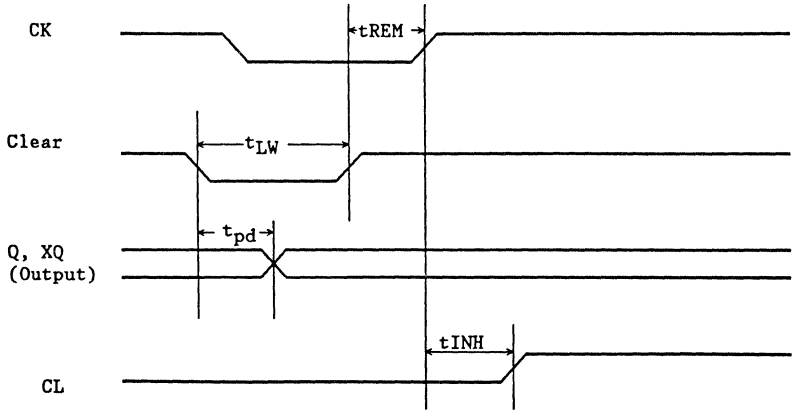


Definitions of Parameters

i) Clock Mode

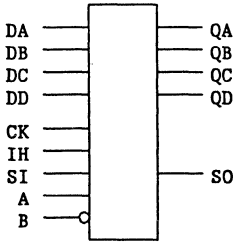


ii) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SFDS	SCAN 4-input DFF with Clock Inhibit	31

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.46	0.13	2.42	0.08	0.13	4	CK → QA~QC
2.63	0.13	2.60	0.08	0.13	4	CK → QD

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	0.0
Data Hold Time	tHD	1.8

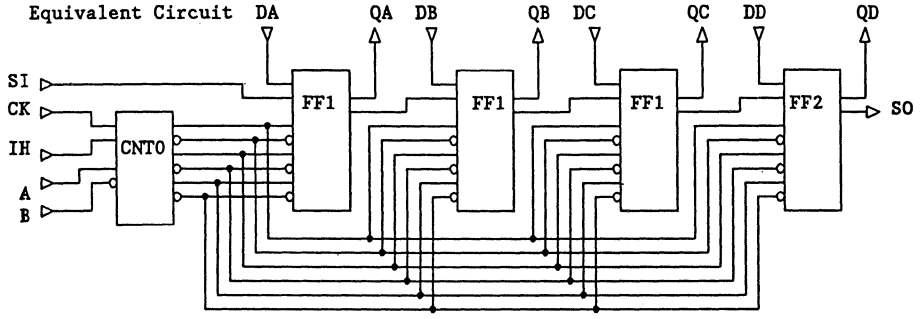
Pin Name	Input Loading Factor (£u)
D	2
CK,IH	1
SI	2
A,B	1

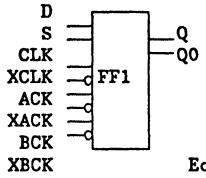
Pin Name	Output Driving Factor (£u)
Q	18
SO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

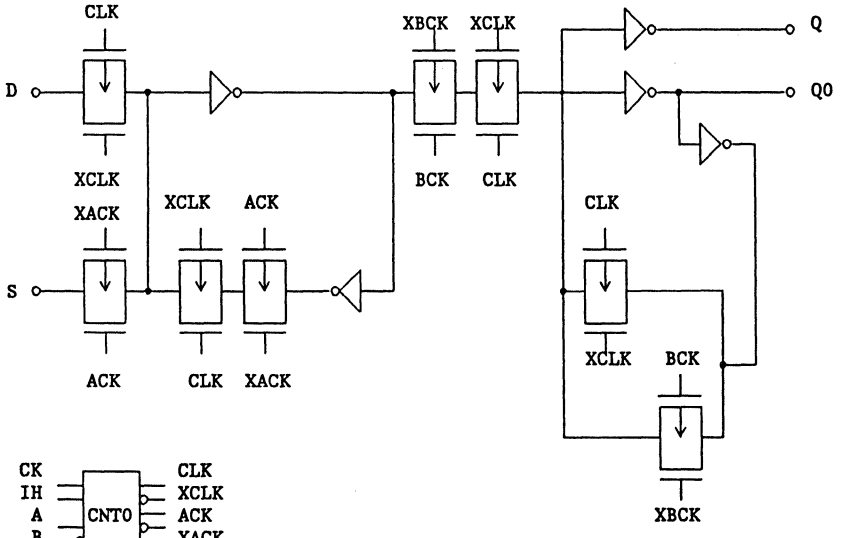
Cell Name
SFDS

Equivalent Circuit

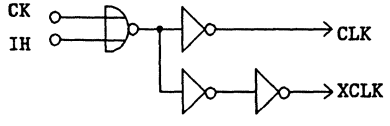


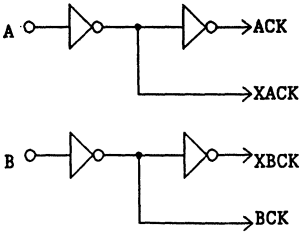


Equivalent Circuit (FF1)

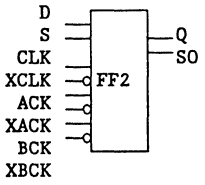


Equivalent Circuit (CNT0)

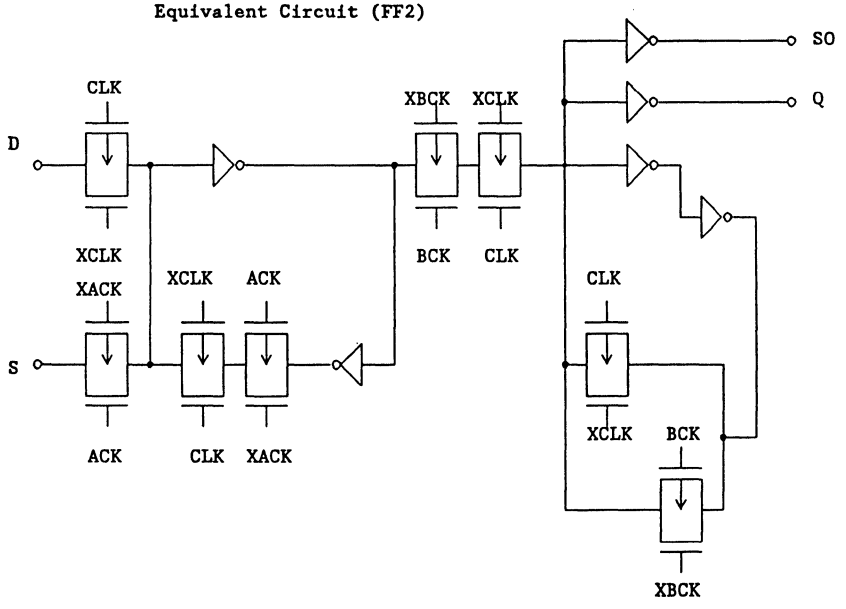




Cell Name
SFDS

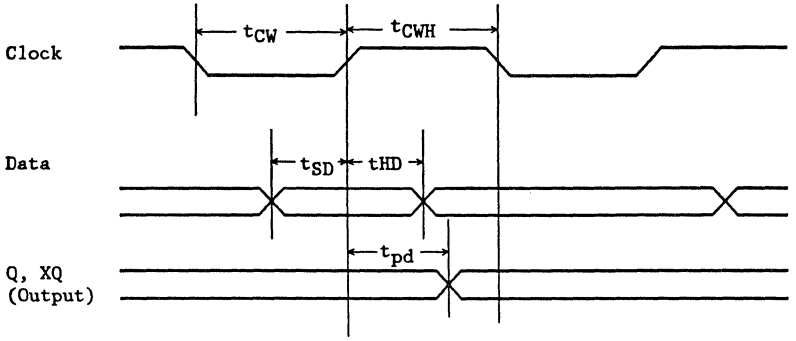


Equivalent Circuit (FF2)



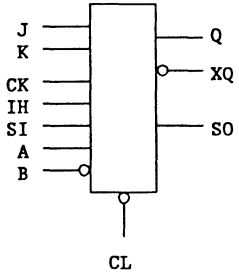
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SFJD	SCAN J-K FF with Clock Inhibit	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.59	0.14	2.40	0.10	0.16	4	CK → Q
2.77	0.13	3.03	0.07	0.08	4	CK → XQ
2.24	0.13	1.98	0.07	0.14	4	CL → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time (J)	tSD	3.0
Data Hold Time (J)	tHD	0.5
Data Setup Time (K)	tSD	2.6
Data Hold Time (K)	tHD	0.1
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	1.6
Clear Hold Time	tINH	3.5

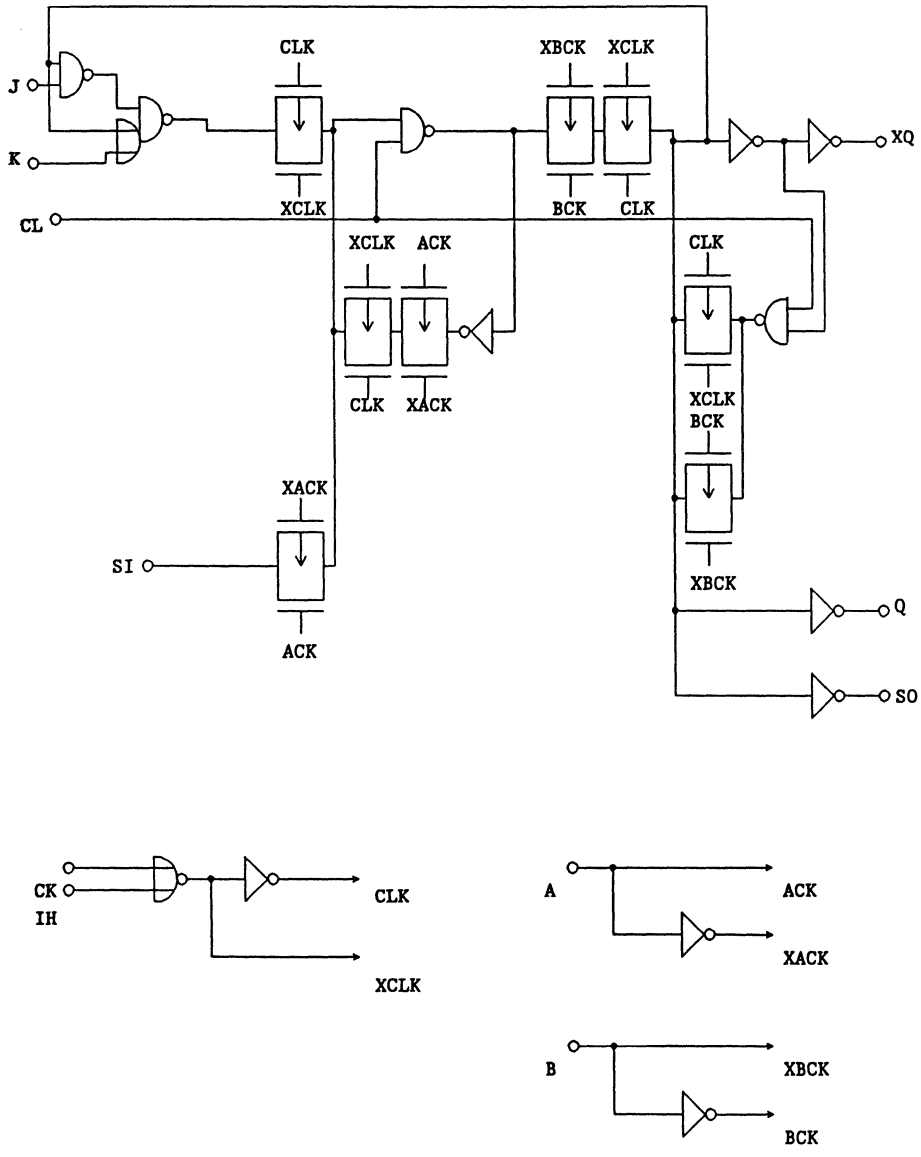
Pin Name	Input Loading Factor (Lu)
J,K	1
CK,IH	1
SI	2
A,B	2
CL	2

Pin Name	Output Driving Factor (Lu)
Q	18
XQ	18
SO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

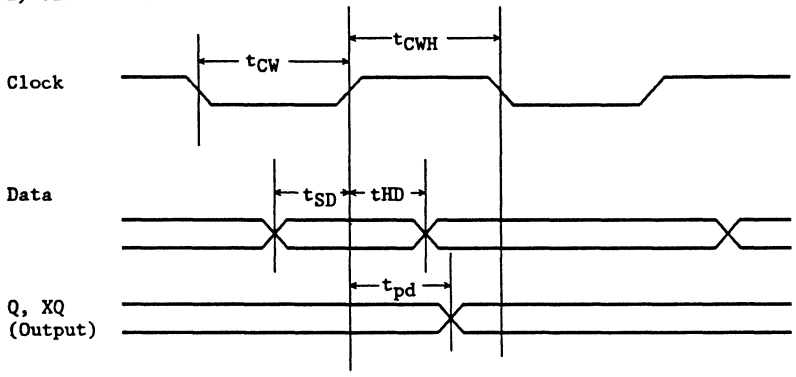
Cell Name
SFJD

Equivalent Circuit

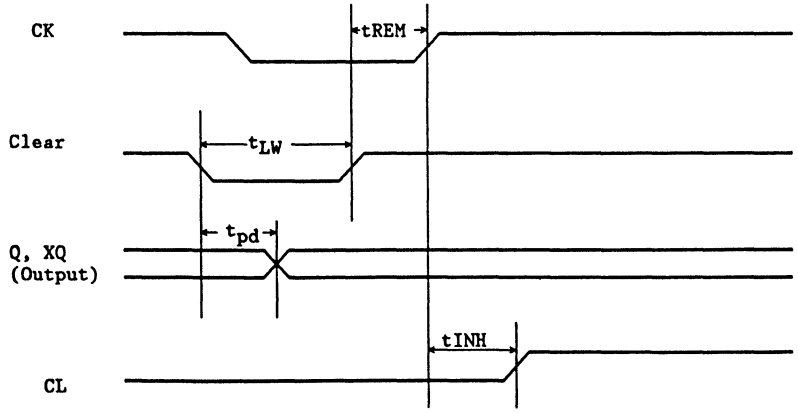


Definitions of Parameters

i) Clock Mode



ii) Clear Mode



2

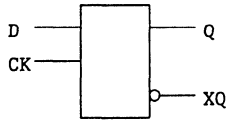
Non Scan Flip-flop Family

Page	Unit Cell Name	Function	Basic Cells
2–181	FDM	Non-Scan D Flip-flop	6
2–183	FDN	Non-Scan D Flip-flop with Set	7
2–185	FDO	Non-Scan D Flip-flop with Reset	7
2–187	FDP	Non-Scan D Flip-flop with Set and Reset	8
2–190	FDQ	Non-Scan 4-bit D Flip-flop	21
2–192	FDR	Non-Scan 4-bit D Flip-flop with Clear	26
2–195	FDS	Non-Scan 4-bit D Flip-flop	20
2–197	FD2	Non-Scan Power D Flip-flop	7
2–199	FD3	Non-Scan Power D Flip-flop with Preset	8
2–201	FD4	Non-Scan Power D Flip-flop with Clear and Preset	9
2–203	FD5	Non-Scan Power D Flip-flop with Clear	8
2–205	FJD	Non-Scan Positive Edge Clocked Power J–K Flip-flop with Clear	12

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FDM	Non-SCAN DFF	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.40	0.13	1.44	0.07			CK → Q
1.73	0.13	1.89	0.07			CK → XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	1.7
Data Hold Time	tHD	1.2

Pin Name	Input Loading Factor (ℓu)
D	2
CK	1

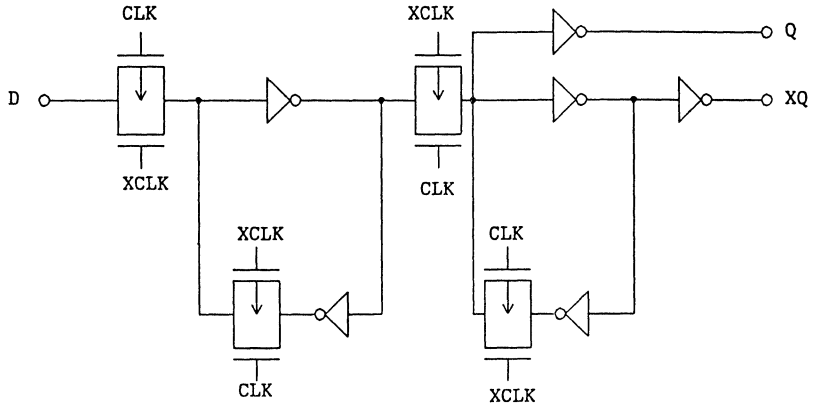
Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

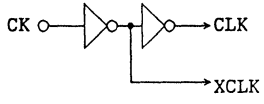
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

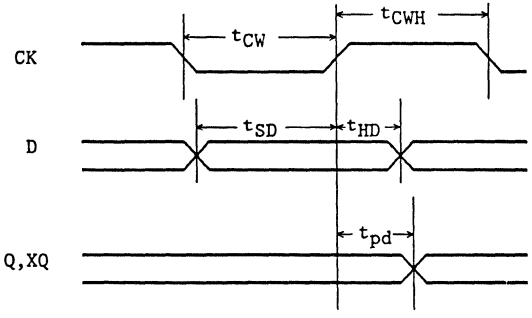
Inputs		Outputs	
D	CK	Q	XQ
H	↑	H	L
L	↑	L	H

Equivalent Circuit



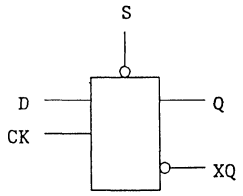


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FDN	Non-SCAN DFF with SET	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.44	0.13	1.40	0.07	0.10	4	CK → Q
1.97	0.13	1.94	0.07			CK → XQ
1.79	0.13	0.86	0.07			S → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	1.7
Data Hold Time	tHD	1.2
Set Pulse Width	tSW	4.0
Set Release Time (S)	tREM	0.3
Set Hold Time	tINH	3.1

Pin Name	Input Loading Factor (£u)
D	2
S	2
CK	1

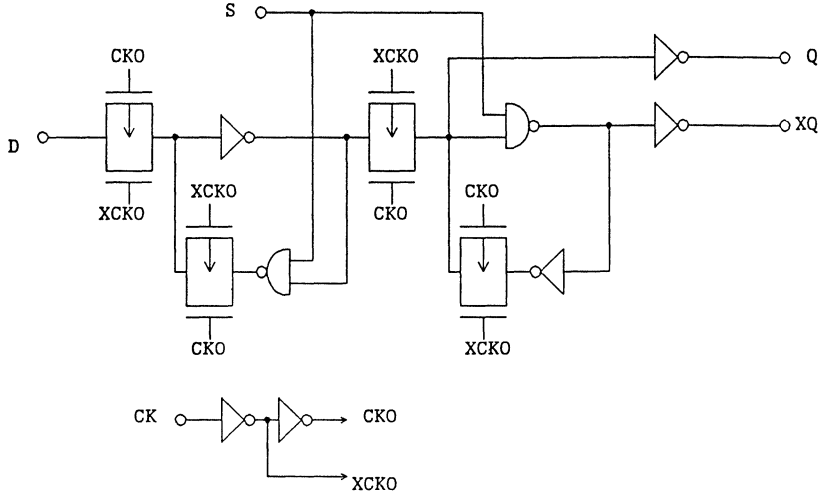
Pin Name	Output Driving Factor (£u)
Q	18
XQ	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

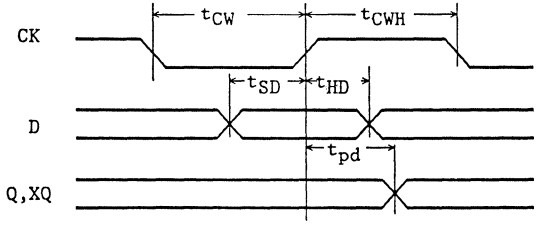
Inputs			Outputs	
S	D	CK	Q	XQ
L	X	X	H	L
H	H	↑	H	L
H	L	↑	L	H

Equivalent Circuit

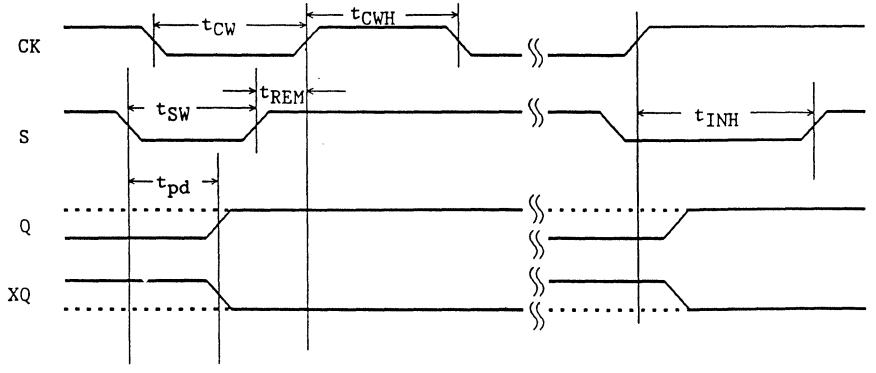


Definition of Parameters

1) t_{CW}, t_{CWH}, t_{SD}, t_{HD} and t_{pd} (CK → Q,XQ)

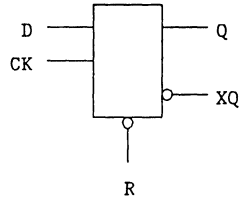


2) t_{SW}, t_{REM}, t_{INH} and t_{pd} (S → Q,XQ)



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FDO	Non-SCAN DFF with RESET	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.55	0.13	1.43	0.08			CK → Q
1.73	0.13	2.07	0.07			CK → XQ
1.60	0.13	1.31	0.08			R → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	1.7
Data Hold Time	tHD	1.2
Reset Pulse Width	tRW	4.0
Reset Release Time (R)	tREM	0.8
Reset Hold Time	tINH	2.7

Pin Name	Input Loading Factor (ℓu)
D	2
R	2
CK	1

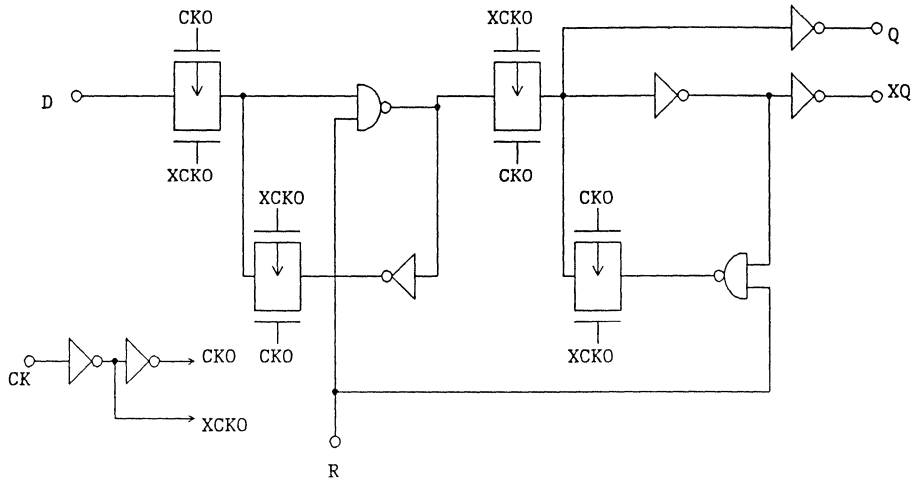
Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

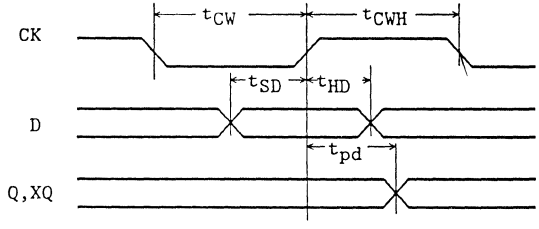
Inputs			Outputs	
R	D	CK	Q	XQ
L	X	X	L	H
H	H	↑	H	L
H	L	↑	L	H

Equivalent Circuit

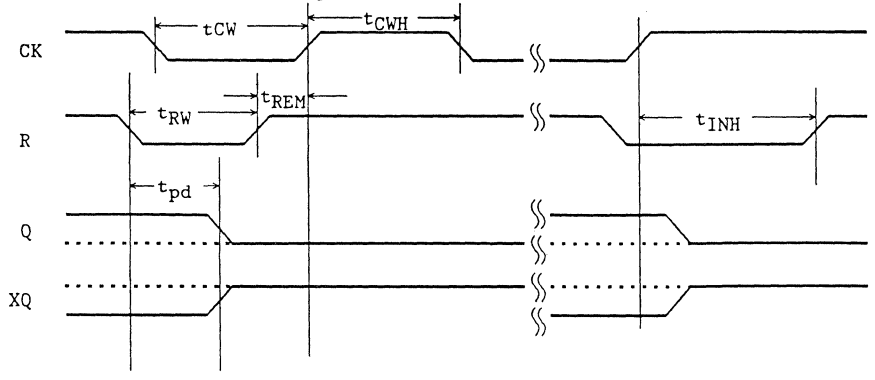


Definition of Parameters

1) t_{CW}, t_{CWH}, t_{SD}, t_{HD} and t_{pd} (CK → Q,XQ)

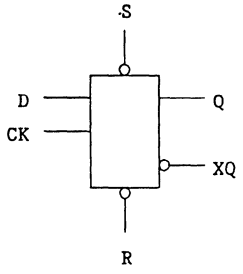


2) t_{RW}, t_{REM}, t_{INH} and t_{pd} (R → Q,XQ)



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FDP	Non-SCAN DFF with Set and Reset	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.57	0.13	1.41	0.08			CK → Q
1.96	0.13	2.00	0.07			CK → XQ
1.79	0.13	1.27	0.08			R → Q,XQ
2.03	0.13	0.81	0.07			S → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	1.7
Data Hold Time	tHD	1.2
Set Pulse Width	tSW	4.0
Set Release Time (S)	tREM	0.3
Set Hold Time	tINH	3.1
Reset Pulse Width	tRW	4.0
Reset Release Time (R)	tREM	0.8
Reset Hold Time	tINH	2.7

Pin Name	Input Loading Factor (ℓu)
D	2
S	2
R	2
CK	1

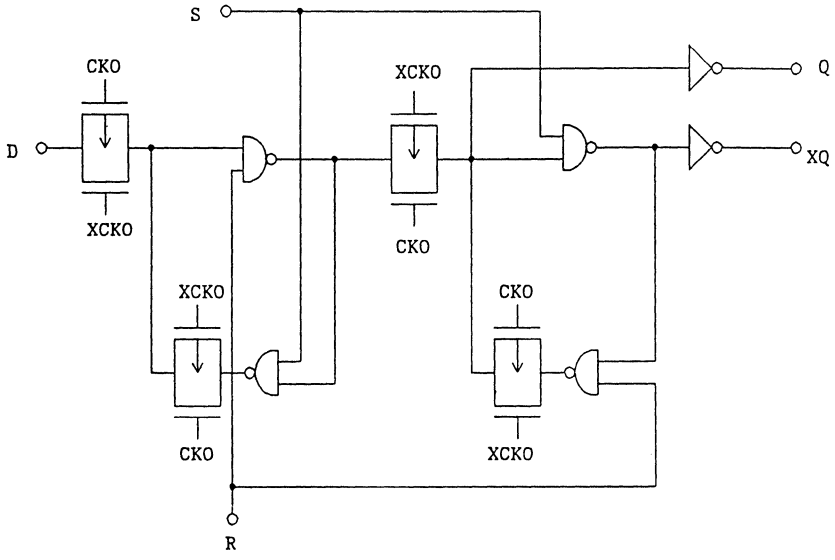
Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

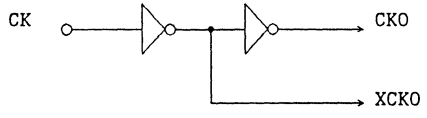
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs				Outputs	
S	R	D	CK	Q	XQ
H	L	X	X	L	H
L	H	X	X	H	L
L	L	X	X	Inhibited	
H	H	H	↑	H	L
H	H	L	↑	L	H

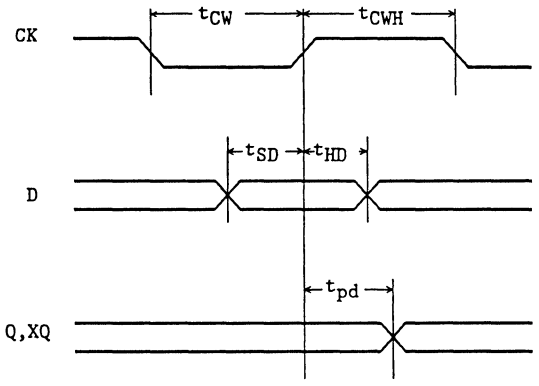
Equivalent Circuit



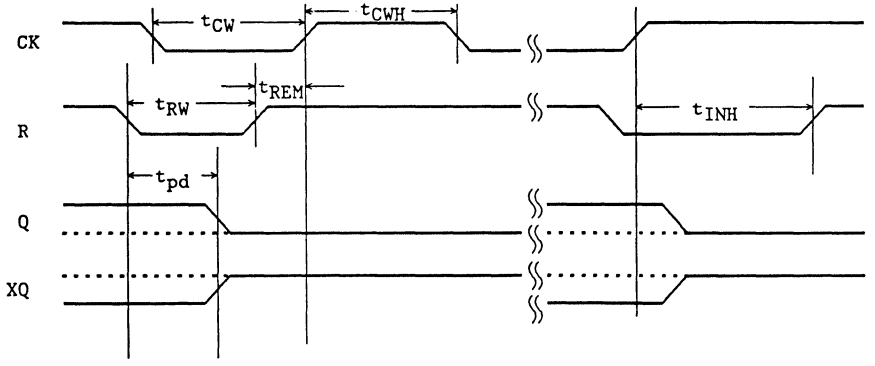


Definition of Parameters

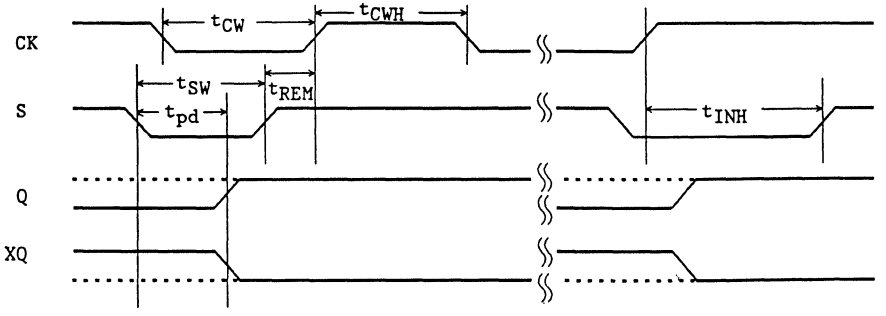
1) t_{CW}, t_{CWH}, t_{SD}, t_{HD} and t_{pd} (CK → Q,XQ)



2) t_{RW}, t_{REM}, t_{INH} and t_{pd} (R → Q,XQ)

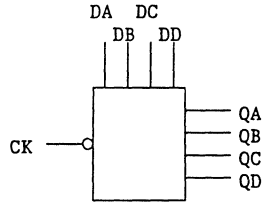


3) tSW, tREM, tINH and tpd (S → Q,XQ)



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FDQ	Non-SCAN 4-bit DFF	21

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.70	0.13	2.19	0.07			CK → Q

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWL	4.0
Data Setup Time	tSD	0.9
Data Hold Time	tHD	2.3

Pin Name	Input Loading Factor (ℓu)
D	1
CK	1

Pin Name	Output Driving Factor (ℓu)
Q	18

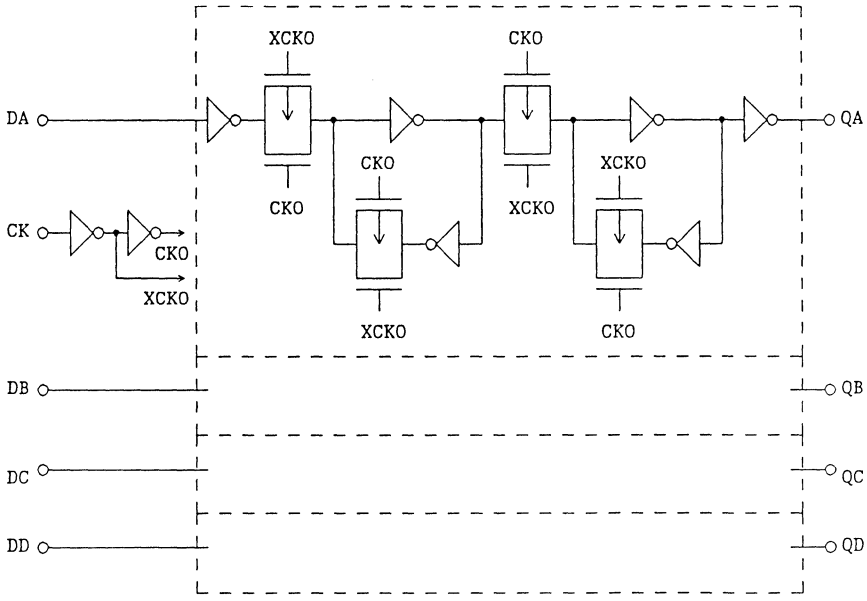
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

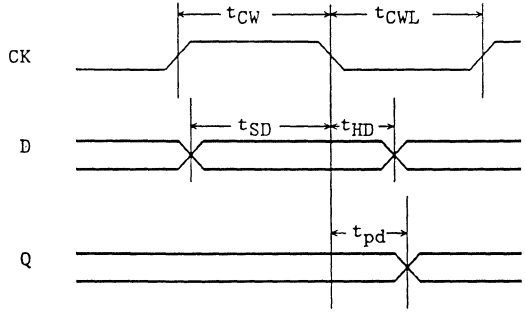
Input		Output
CK	D	Q
↓	H	H
↓	L	L

Cell Name
FDQ

Equivalent Circuit

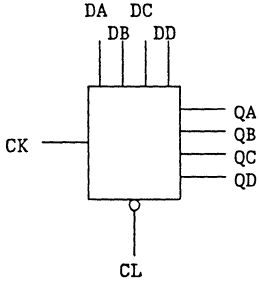


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FDR	Non-SCAN 4-bit DFF with CLEAR	26

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.11	0.13	2.90	0.07			CK → Q
-	-	1.75	0.07			CL → Q

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	0.9
Data Hold Time	tHD	2.3
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	1.2
Clear Hold Time	tINH	3.6

Pin Name	Input Loading Factor (ℓu)
D	1
CK	1
CL	1

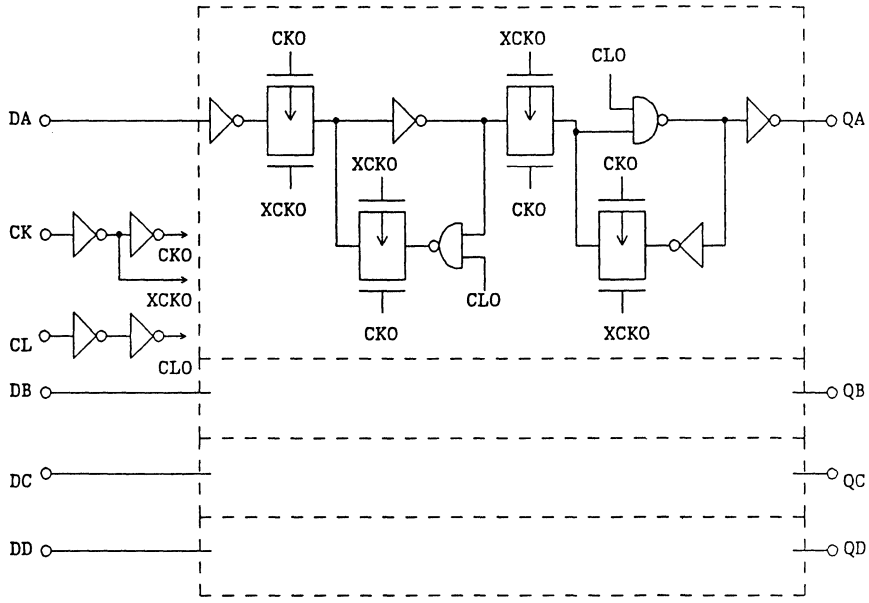
Pin Name	Output Driving Factor (ℓu)
Q	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

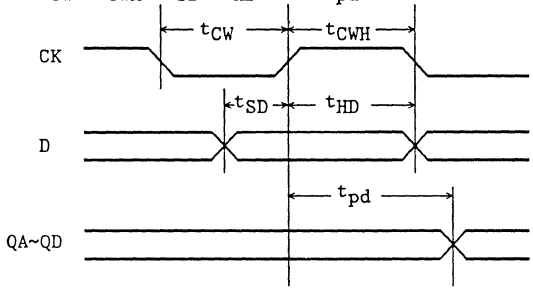
Inputs			Output
CK	D	CL	Q
X	X	L	L
↑	L	H	L
↑	H	H	H

Equivalent Circuit

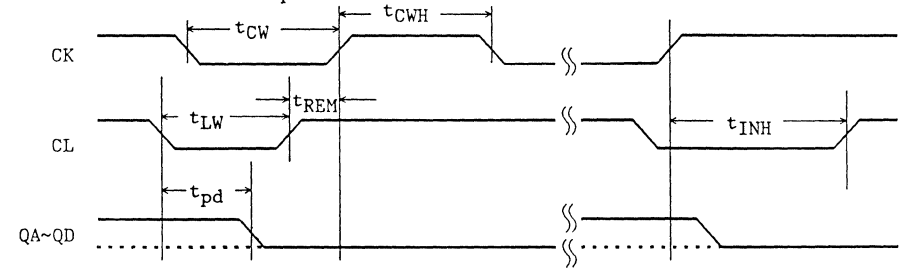


Definition of Parameters

1) t_{CW}, t_{CWH}, t_{SD}, t_{HD}, and t_{pd} (CK→QA~QD)



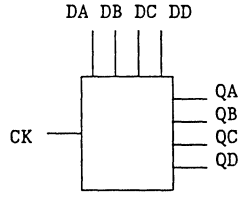
2) t_{LW}, t_{REM}, t_{INH} and t_{pd} (CL → QA~QD)



2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FDS	Non-SCAN 4-bit DFF	20

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.43	0.13	1.96	0.07			CK → Q

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	0.9
Data Hold Time	tHD	2.0

Pin Name	Input Loading Factor (ℓu)
D	2
CK	1

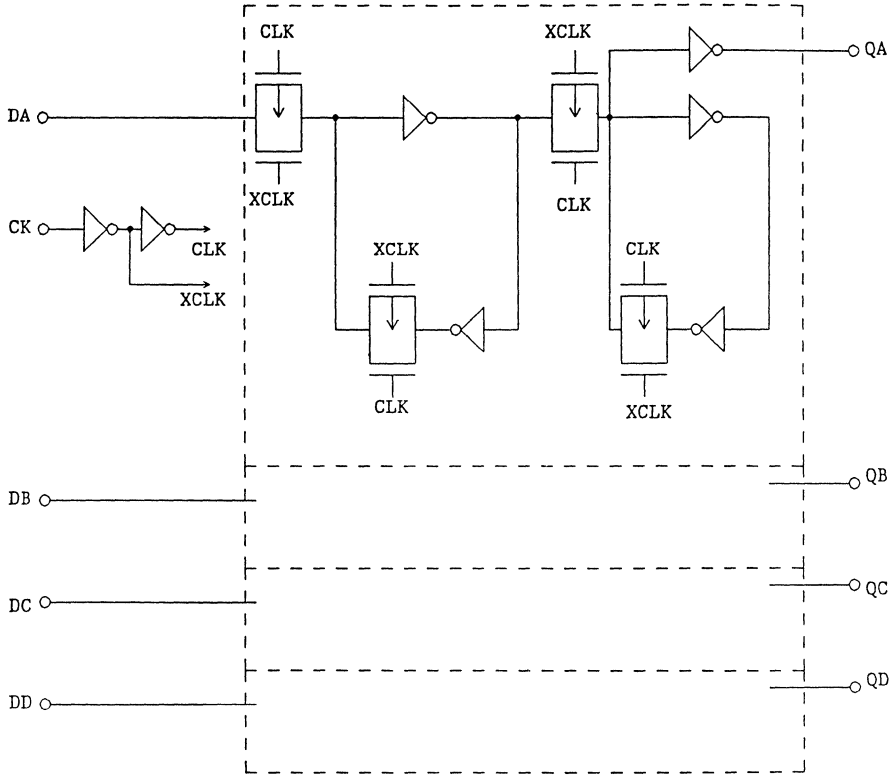
Pin Name	Output Driving Factor (ℓu)
Q	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

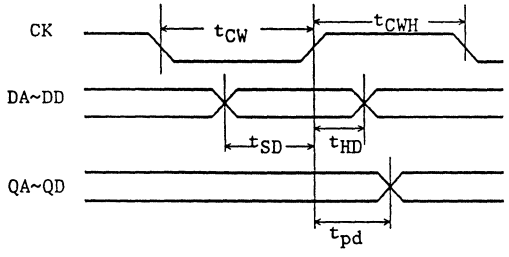
Function Table

Inputs		Outputs
CK	D	Q
↑	L	L
↑	H	H

Equivalent Circuit

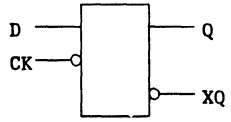


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FD2	Non-SCAN Power DFF	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.32	0.07	1.38	0.04	0.08	7	CK → Q
2.04	0.07	1.87	0.03	0.06	7	CK → XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCW	4.0
Data Setup Time	tSD	1.7
Data Hold Time	tHD	1.2

Pin Name	Input Loading Factor (ℓu)
D	2
CK	1

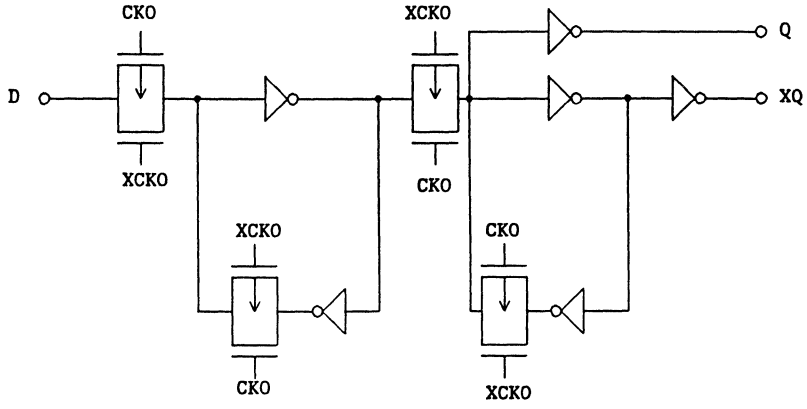
Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

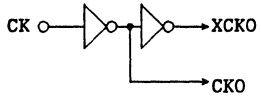
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

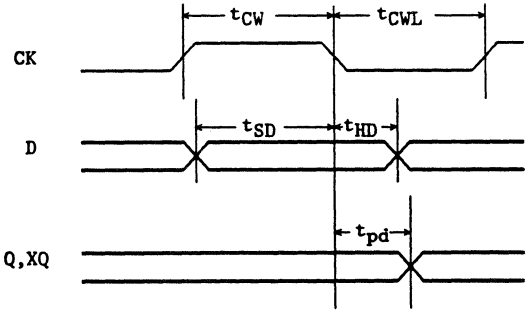
Inputs		Outputs	
CK	D	Q	XQ
↓	H	H	L
↓	L	L	H

Equivalent Circuit



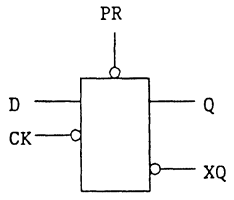


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FD3	Non-SCAN Power DFF with Preset	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.37	0.05	1.39	0.03	0.08	7	CK → Q
2.24	0.05	2.00	0.03	0.06	7	CK → XQ
1.91	0.05	0.73	0.03	0.06	7	PR → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWL	4.0
Data Setup Time	tSD	1.7
Data Hold Time	tHD	1.2
Preset Pulse Width	tPW	4.0
Preset Release Time	tREM	0.3
Preset Hold Time	tINH	3.1

Pin Name	Input Loading Factor (ℓu)
D	2
CK	1
PR	2

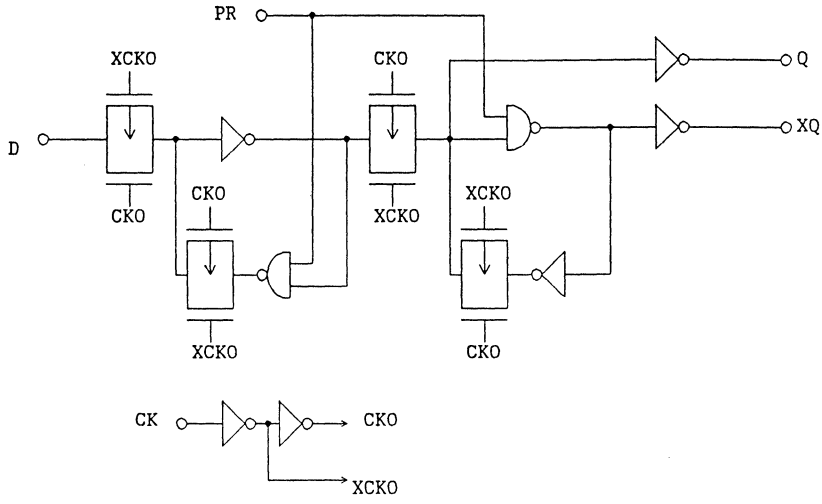
Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

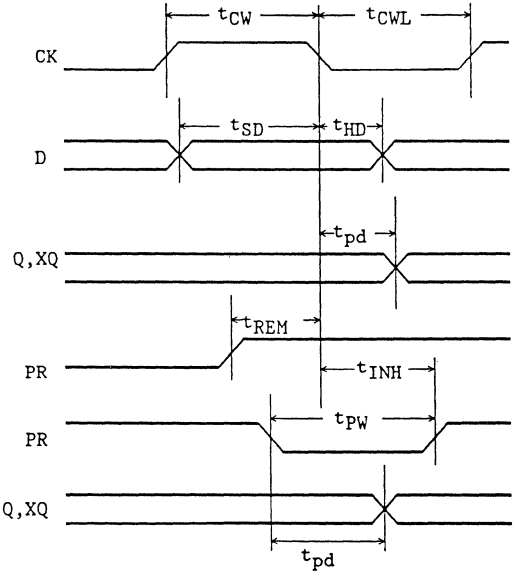
Function Table

Inputs			Outputs	
PR	CK	D	Q	XQ
L	X	X	H	L
H	↓	H	H	L
H	↓	L	L	H

Equivalent Circuit

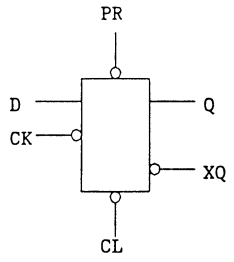


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FD4	Non-SCAN Power DFF with Clear and Preset	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.52	0.06	1.38	0.04	0.08	7	CK → Q
2.25	0.05	2.18	0.03	0.06	7	CK → XQ
1.98	0.05	1.17	0.04	0.08	7	CL → Q,XQ
1.99	0.06	0.74	0.03	0.06	7	PR → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWL	4.0
Data Setup Time	tSD	1.7
Data Hold Time	tHD	1.2
Preset Pulse Width	tPW	4.0
Preset Release Time	tREM	0.3
Preset Hold Time	tINH	3.1
Clear Palse Width	tLW	4.0
Clear Release Time	tREM	0.8
Clear Hold Time	tINH	2.7

Pin Name	Input Loading Factor (ℓu)
D	2
CK	1
CL	2
PR	2

Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

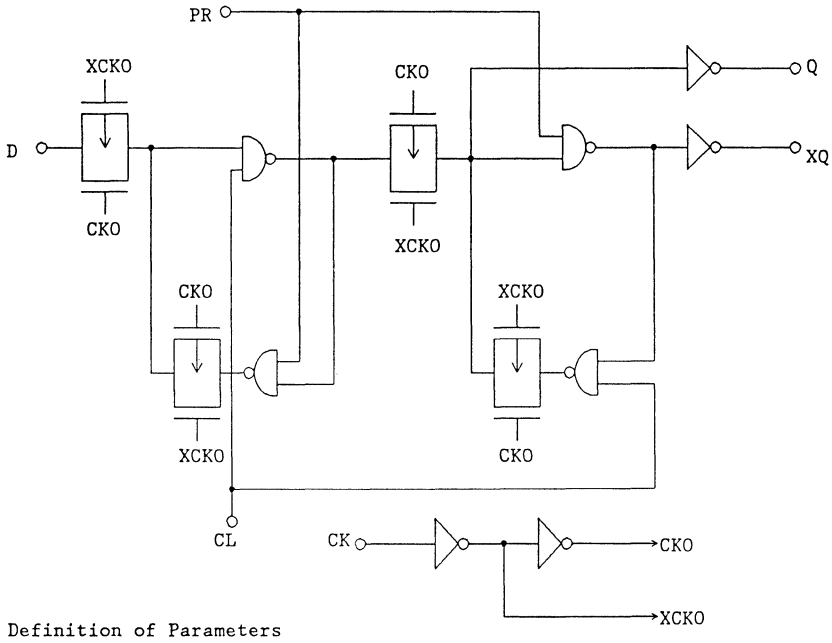
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

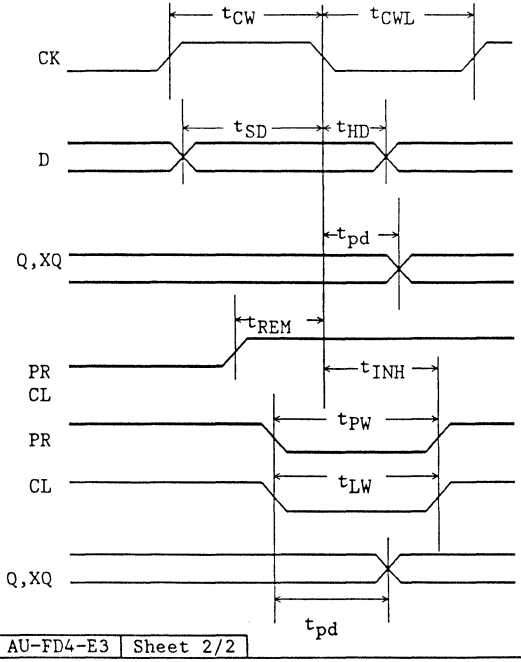
Inputs				Outputs	
PR	CL	CK	D	Q	XQ
L	H	X	X	H	L
H	L	X	X	L	H
H	H	↓	H	H	L
H	H	↓	L	L	H

Cell Name
FD4

Equivalent Circuit

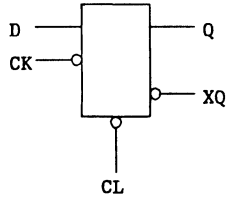


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FD5	Non-SCAN Power DFF with CLEAR	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.51	0.07	1.37	0.04	0.08	7	CK → Q
2.06	0.07	2.06	0.03	0.06	7	CK → XQ
1.89	0.07	1.22	0.04	0.08	7	CL → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWL	4.0
Data Setup Time	tSD	1.7
Data Hold Time	tHD	1.2
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	1.2
Clear Hold Time	tINH	3.6

Pin Name	Input Loading Factor (ℓu)
D	2
CK	1
CL	2

Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

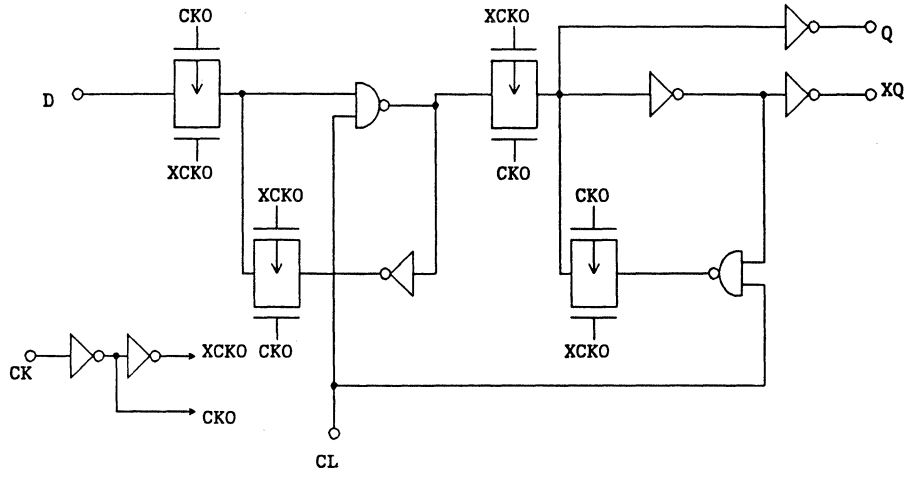
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

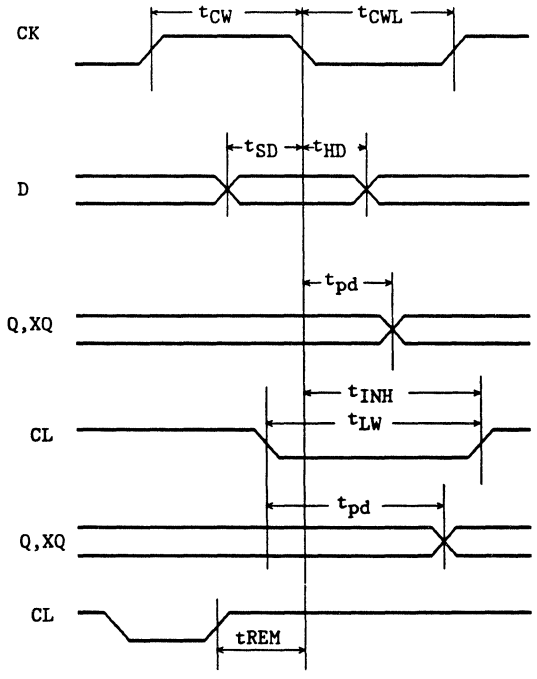
Inputs			Outputs	
CL	CK	D	Q	XQ
L	X	X	L	H
H	↓	H	H	L
H	↓	L	L	H

Cell Name
FD5

Equivalent Circuit

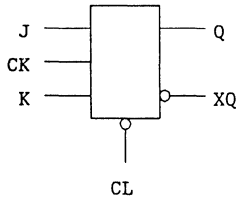


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FJD	Non-SCAN Positive edge clocked Power JKFF with Clear	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.52	0.07	2.37	0.04	0.07	7	CK → Q
3.55	0.07	1.99	0.04	0.07	7	CK → XQ
1.92	0.07	1.03	0.04	0.07	7	CL → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.5
Clock Pause Time	tCWH	4.5
J,K Setup Time	tSD	2.0
J,K Hold Time	tHD	1.0
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	2.0
Clear Hold Time	tINH	3.6

Pin Name	Input Loading Factor (ℓu)
CL	2
J	1
K	1
CK	1

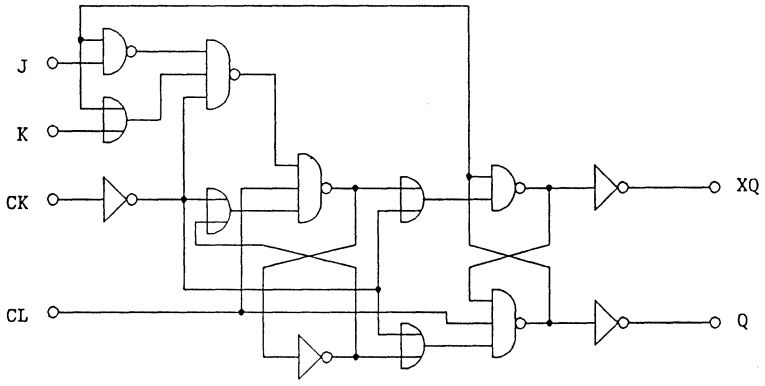
Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

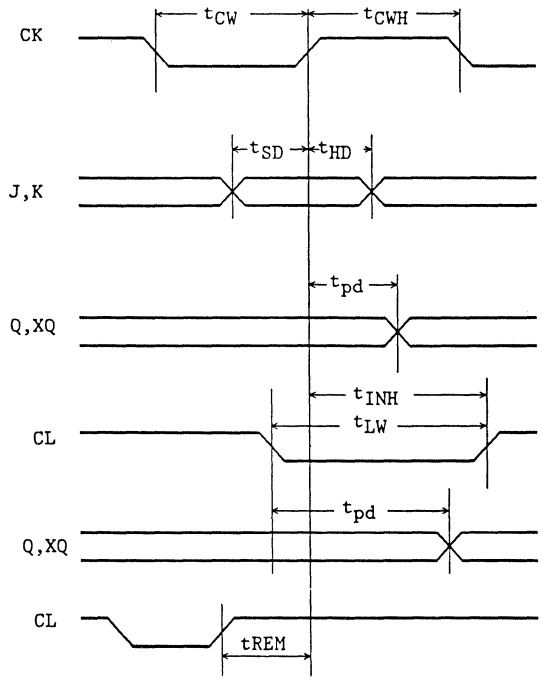
Function Table

Inputs				Outputs	
CL	CK	J	K	Q	XQ
L	X	X	X	L	H
H	↑	L	L	Q_0	XQ_0
H	↑	L	H	L	H
H	↑	H	L	H	L
H	↑	H	H	XQ_0	Q_0

Equivalent Circuit



Definition of Parameters

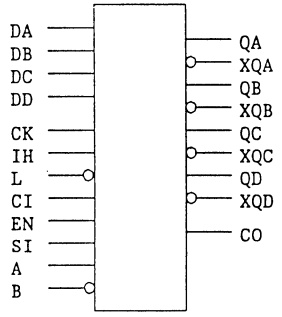


Binary Counter Family

Page	Unit Cell Name	Function	Basic Cells
2–209	SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62
2–214	SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66
2–219	C11	Non-Scan Flip–Flop for Counter	11
2–221	C41	Non-Scan 4-bit Binary Asynchronous Counter	24
2–224	C42	Non-Scan 4-bit Binary Synchronous Counter	32
2–227	C43	Non-Scan 4-bit Binary Synchronous Up Counter	48
2–231	C45	Non-Scan 4-bit Binary Synchronous Up Counter	48
2–235	C47	Non-Scan 4-bit Binary Synchronous Up/Down Counter	68
2–239	SC43	Scan 4-bit Synchronous Binary Up Counter with Asynchronous Clear	59
2–243	SC47	Scan 4-bit Synchronous Binary Up/Down Counter	78

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SC7	SCAN 4-bit Synchronous Binary Up Counter with Parallel Load	62

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.64	0.07	2.44	0.05	0.12	7	CK,IH → Q
4.63	0.07	4.27	0.05	0.12	7	CK,IH → XQ
6.24	0.07	4.19	0.03	-	-	CK,IH → CO
1.60	0.07	0.08	0.03	-	-	CI → CO

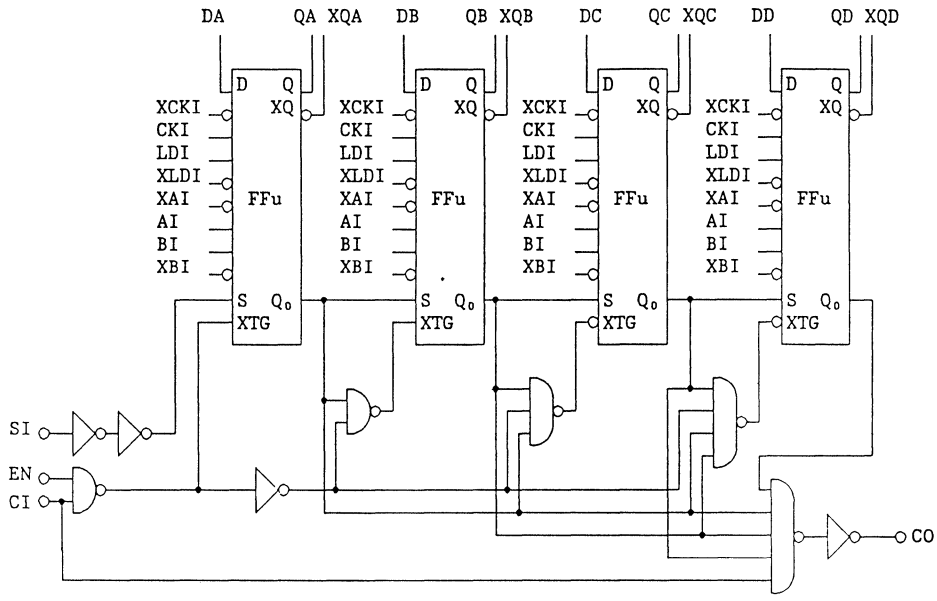
Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	5.8
Clock Pause Time	tCWH	5.8
Data Setup Time	tSD	1.6
Data Hold Time	tHD	2.7
Load Setup Time	tSL	5.1
Load Hold Time	tHL	2.9
CI Setup Time	tSC	5.8
CI Hold Time	tHC	2.2
EN Setup Time	tSE	5.8
EN Hold Time	tHE	2.2

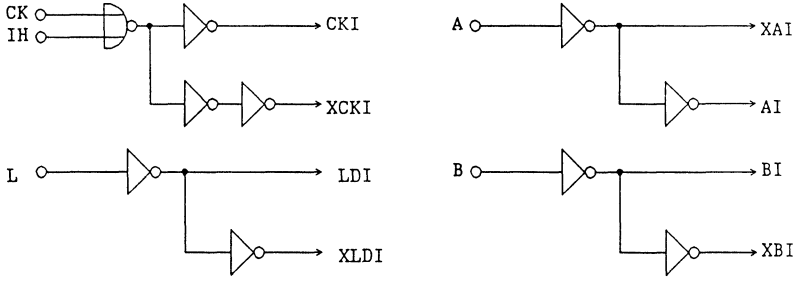
Pin Name	Input Loading Factor (ℓu)
D	1
CK	1
IH	1
L	1
CI	2
EN	1
SI	1
A,B	1

Pin Name	Output Driving Factor (ℓu)
Q	36
XQ	36
CO	36

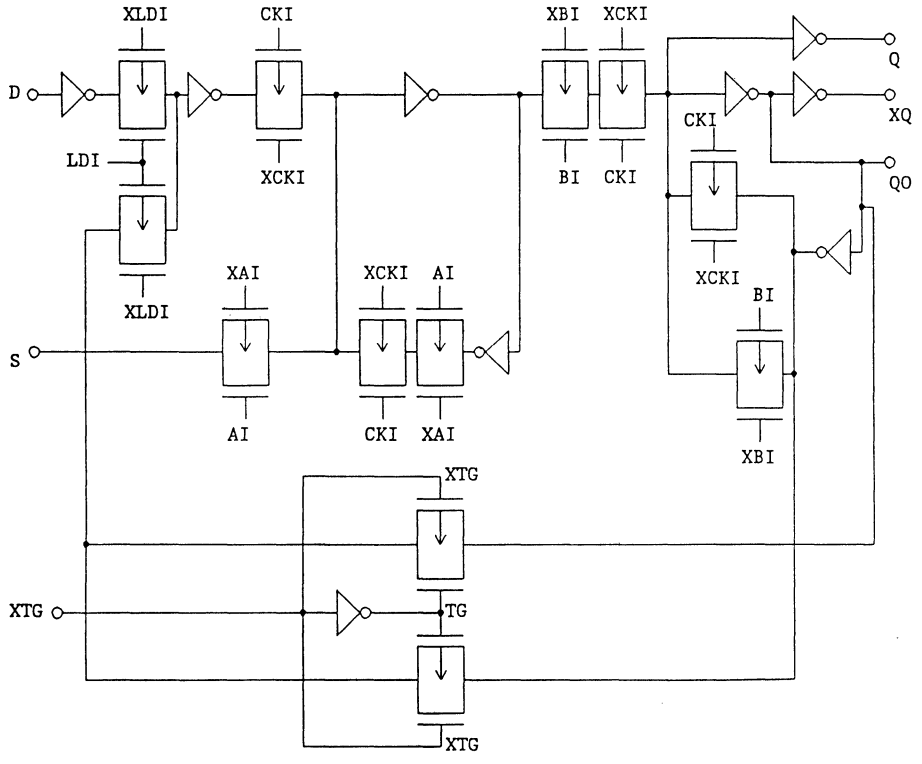
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit





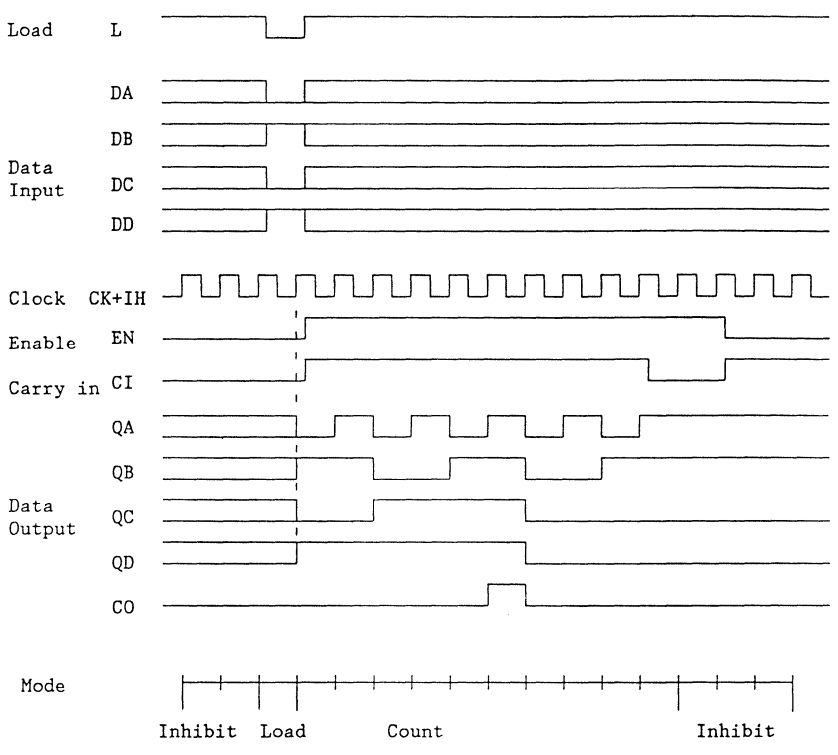
Equivalent Circuit (FFu)



2

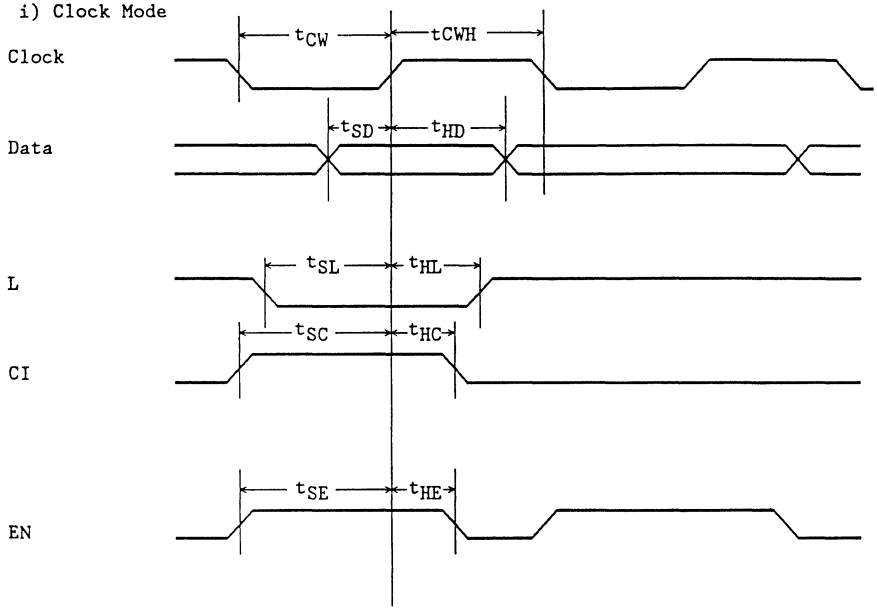
Cell Name
SC7

Function



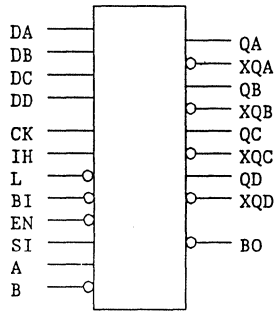
Definitions of Parameters

i) Clock Mode



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SC8	SCAN 4-bit Synchronous Binary Down Counter with Parallel Load	66

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.70	0.06	2.55	0.05	0.11	7	CK,IH → Q
3.52	0.05	3.46	0.03			CK,IH → XQ
5.13	0.07	6.70	0.03			CK,IH → BO
1.19	0.07	1.82	0.03			BI → BO

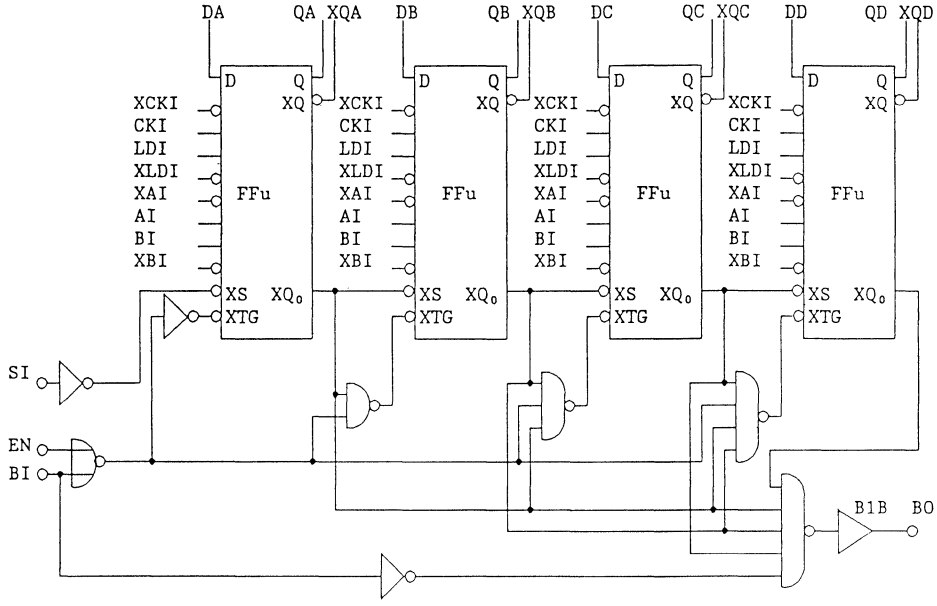
Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	5.5
Clock Pause Time	tCWH	5.5
Data Setup Time	tSD	1.6
Data Hold Time	tHD	2.7
Load Setup Time	tSL	5.1
Load Hold Time	tHL	2.9
EN Setup Time	tSE	6.5
EN Hold Time	tHE	1.5
BI Setup Time	tSB	6.5
BI Hold Time	tHB	1.5

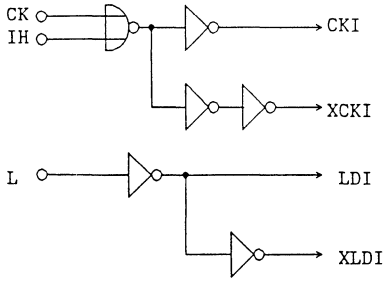
Pin Name	Input Loading Factor (lu)
D	1
CK	1
IH	1
L	1
BI	2
EN	1
SI	1
A,B	1

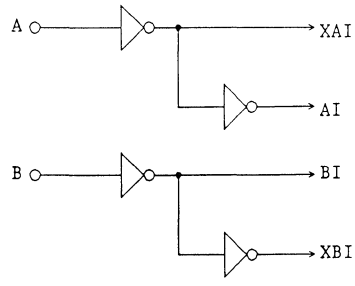
Pin Name	Output Driving Factor (lu)
Q	36
XQ	36
BO	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

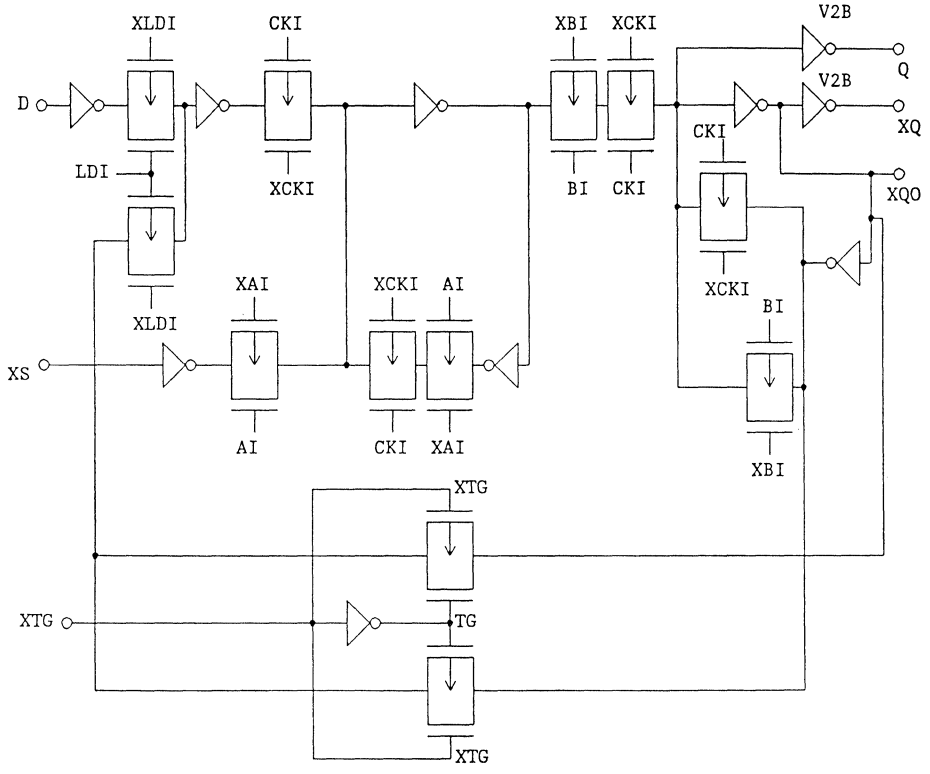
Equivalent Circuit





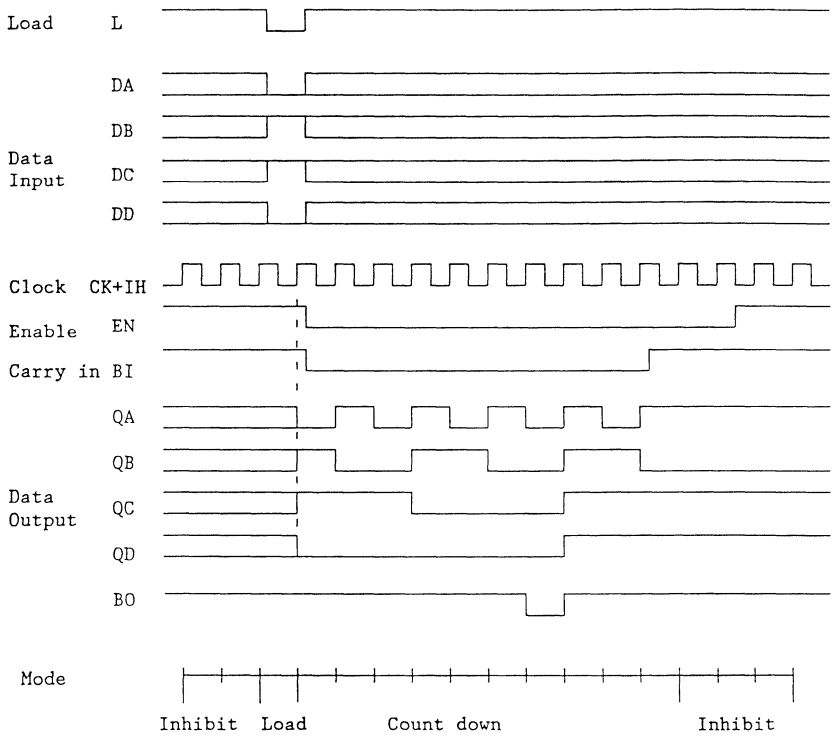


Equivalent Circuit (FFu)



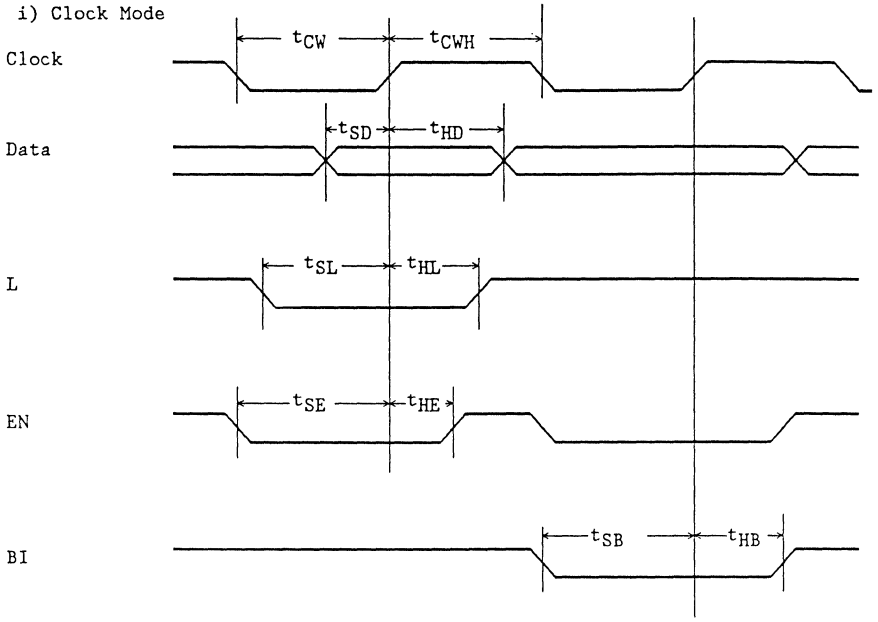
Cell Name
SC8

Function



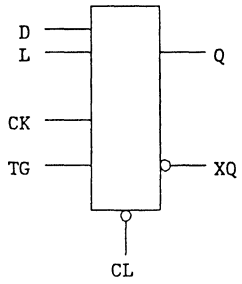
Definitions of Parameters

i) Clock Mode



Cell Name	Function	Number of BC
C11	Non-SCAN Flip-Flop for Counter	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.52	0.13	1.40	0.08			CK → Q
2.03	0.13	2.38	0.08			CK → XQ
2.10	0.13	1.39	0.08			CL → Q,XQ

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	0.8
Clear Hold Time	tINH	0.4
Load Setup Time (CK)	tSL	1.9
Load Hold Time (CK)	tHL	0.4
Data Setup Time (CK)	tSD	2.0
Data Hold Time (CK)	tHD	0.4
TG Setup Time (CK)	tST	2.4
TG Hold Time (CK)	tHT	0.0

Pin Name	Input Loading Factor (ℓu)
L	2
TG	2
CL	2
D,CK	1

Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

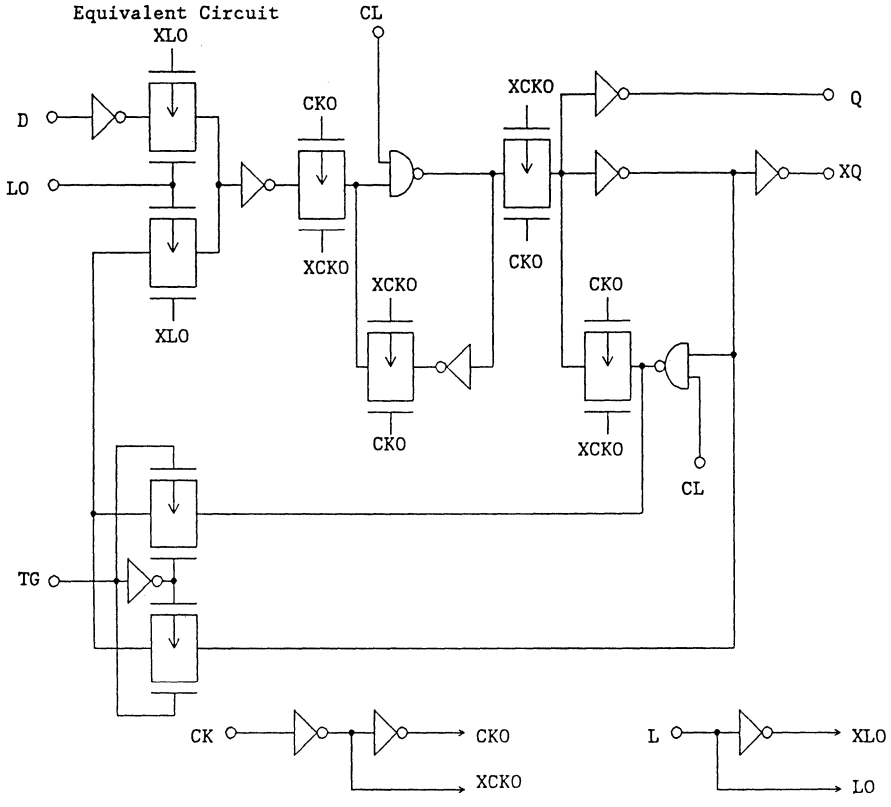
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

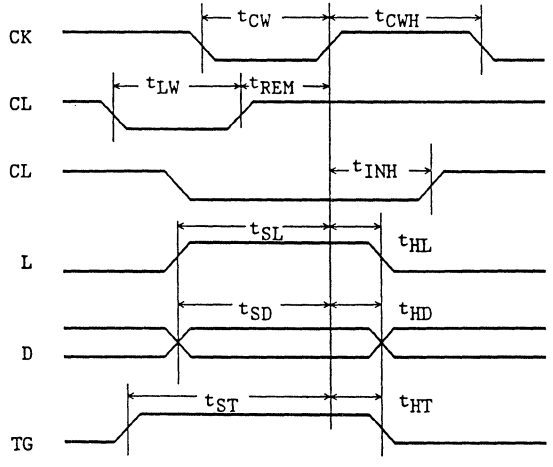
L	D	TG	CL	CK	Q(Q_0)
X	X	X	L	X	L
H	H	X	H	↑	H
H	L	X	H	↑	L
L	X	L	H	↑	Q(Q_0)
L	X	H	H	↑	$\overline{Q}$($\overline{Q_0}$)

Cell Name
C11

Equivalent Circuit

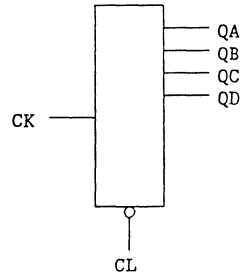


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
C41	Non-SCAN 4-bit Binary Asynchronous Counter	24

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.60	0.11	1.49	0.08	-	-	CK → QA
2.94	0.11	2.63	0.08	-	-	CK → QB
4.11	0.11	3.80	0.08	-	-	CK → QC
5.28	0.11	4.96	0.08	-	-	CK → QD
-	-	3.35	0.08	-	-	CL → Q

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	1.7
Clear Hold Time	tINH	5.4

Pin Name	Input Loading Factor (ℓu)
CK	1
CL	1

Pin Name	Output Driving Factor (ℓu)
Q	18

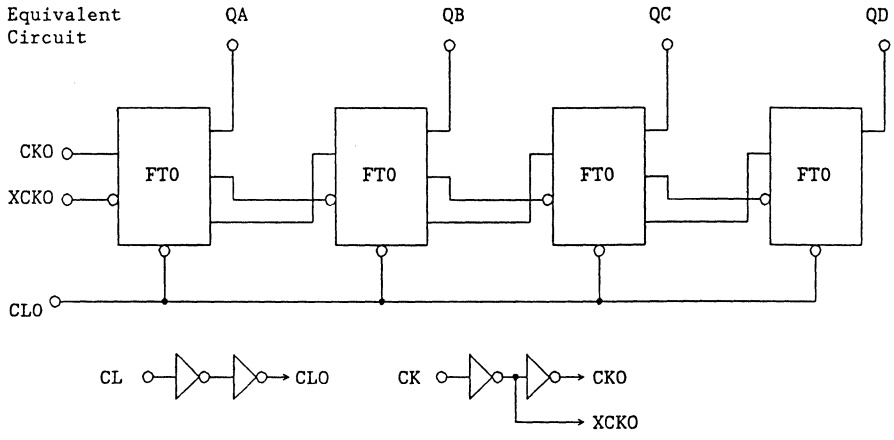
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs		Outputs
CL	CK	Q
H	↑	Count up
L	X	L

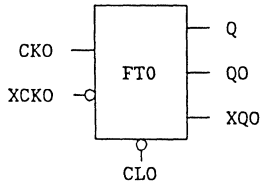
Cell Name
C41

Equivalent Circuit



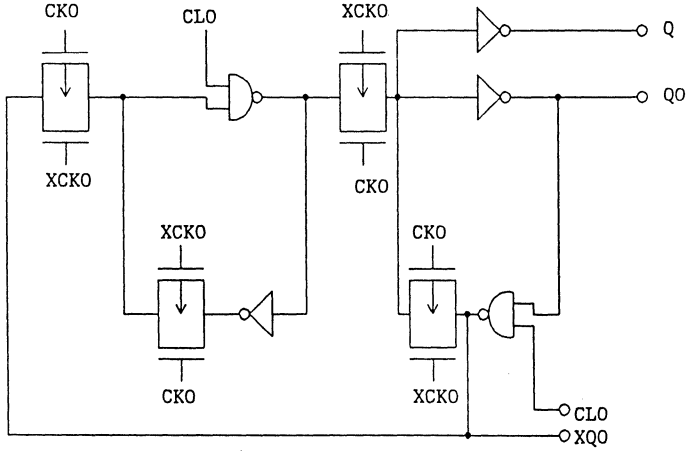
FTO (Flip-Flop for Counter) (not Unit Cell)

Symbol

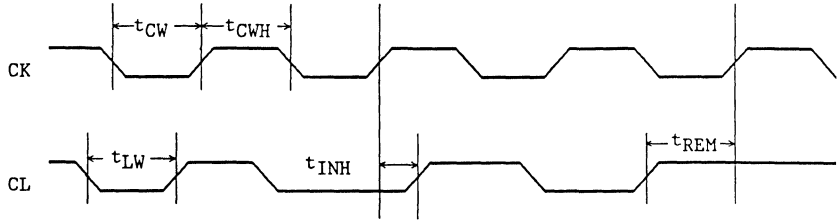


Function Table

CLO	CKO	Q
L	X	L
H	↑	$\overline{Qn-1}$

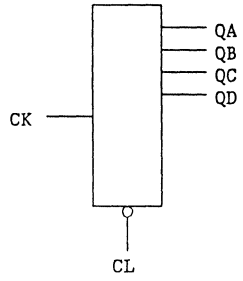


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
C42	Non-SCAN 4-bit Binary Synchronous Counter	32

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.55	0.11	1.87	0.07	0.10	4	CK → Q
-	-	2.69	0.07	0.10	4	CL → Q

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Clear Pulse Width	tLW	4.0
Clear Release Time	tREM	1.7
Clear Hold Time	tINH	5.4

Pin Name	Input Loading Factor (ℓu)
CL	1
CK	1

Pin Name	Output Driving Factor (ℓu)
Q	18

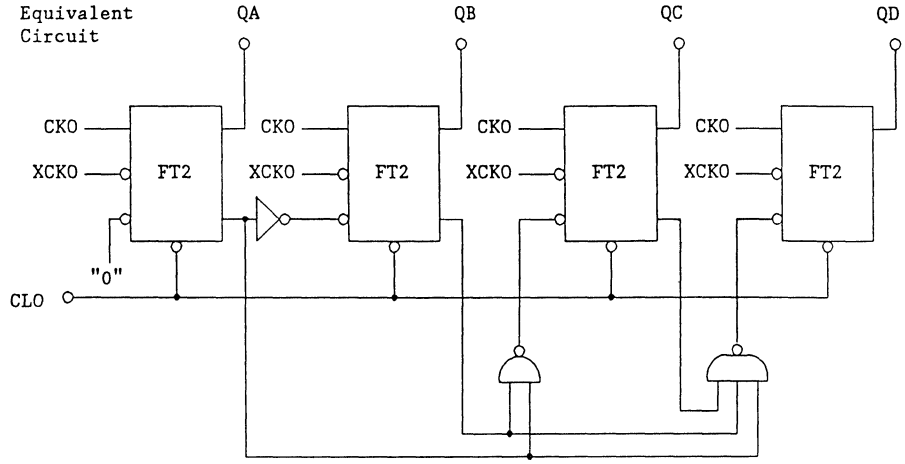
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

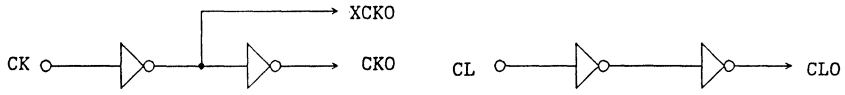
Function Table

Inputs		Outputs
CL	CK	Q
H	↑	Count up
L	X	L

Cell Name
C42

Equivalent Circuit

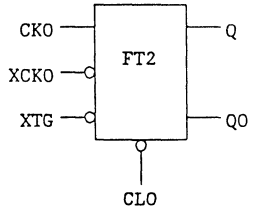




2

FT2 (Flip-Flop for Counter)(not Unit Cell)

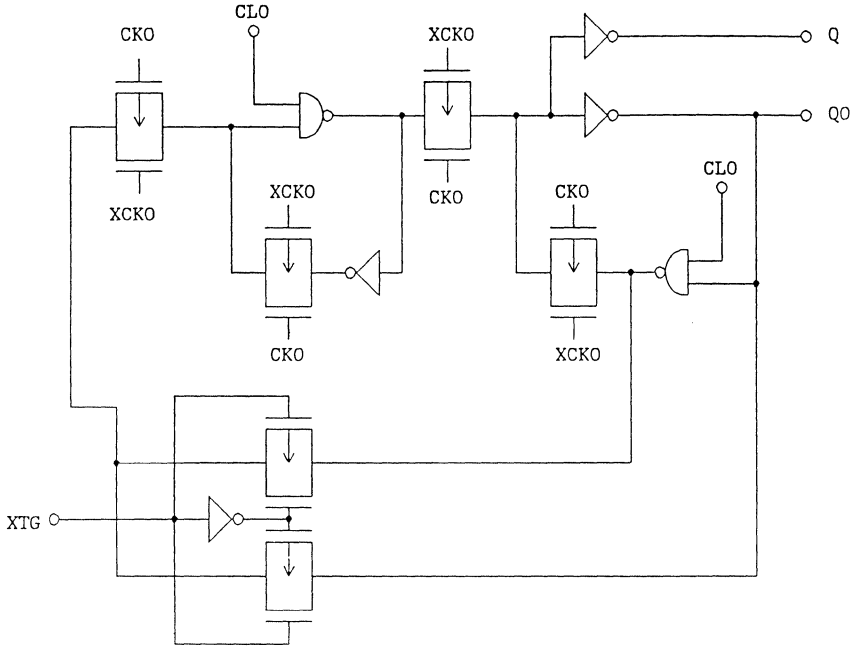
Symbol



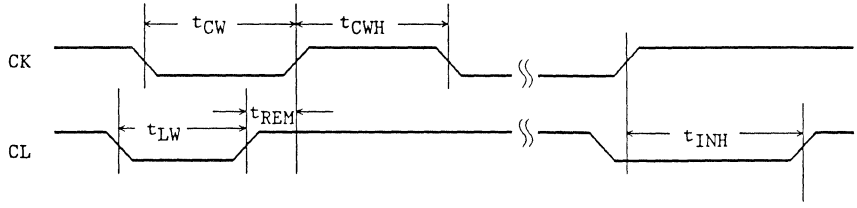
Function Table

Inputs			Output
CLO	XTG	CKO	Q(QO)
L	X	X	L
H	H	↑	Qn-1
H	L	↑	$\overline{Qn-1}$

Equivalent Circuit of FT2

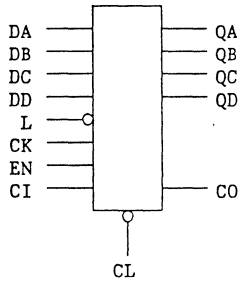


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
C43	Non-SCAN 4-bit Binary Synchronous Up Counter	48

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.37	0.13	1.92	0.07			CK → Q
4.48	0.13	2.85	0.07			CK → CO
1.28	0.13	0.65	0.07			CI → CO
-	-	3.11	0.07			CL → Q
-	-	2.11	0.07			CL → CO

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	5.4
Data Setup Time	tSD	2.1
Data Hold Time	tHD	2.4
Load Setup Time	tSL	3.6
Load Hold Time	tHL	1.1
CI Setup Time	tSC	3.5
CI Hold Time	tHC	0.8
EN Setup Time	tSE	3.5
EN Hold Time	tHE	0.8
Clear Pulse Width	tLW	4.5
Clear Release Time	tREM	1.6
Clear Hold Time	tINH	6.7

Pin Name	Input Loading Factor (ℓu)
D	1
L,EN	1
CK,CL	1
CI	2

Pin Name	Output Driving Factor (ℓu)
Q	18
CO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

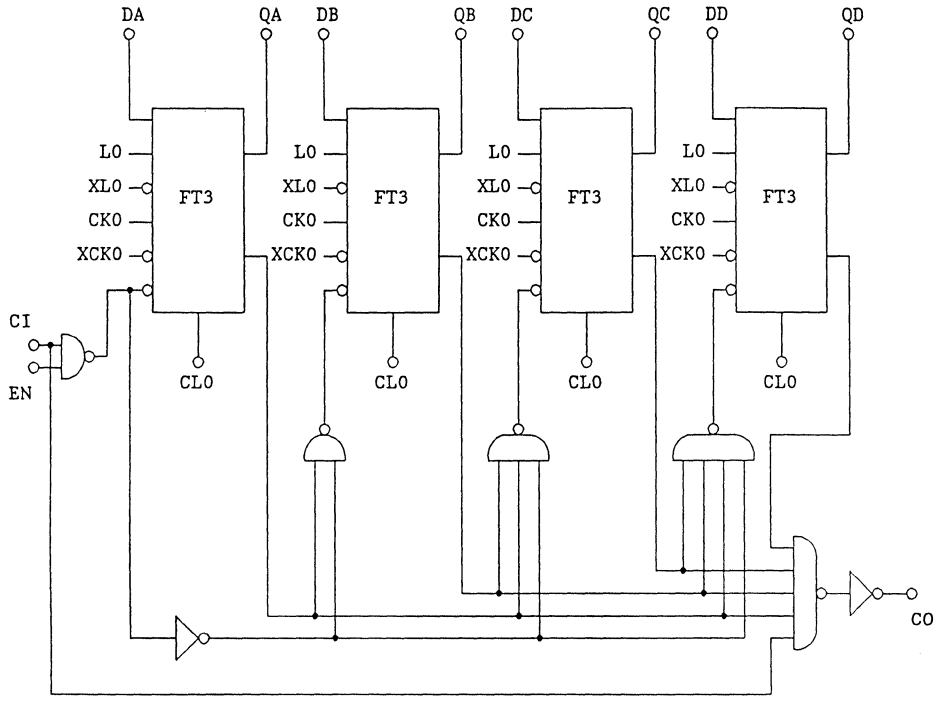
Function Table

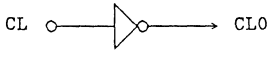
Inputs						Outputs
CL	L	D	EN	CI	CK	Q
L	X	X	X	X	X	L
H	L	H	X	X	↑	H
H	L	L	X	X	↑	L
H	H	X	X	L	X	No Counting
H	H	X	L	X	X	No Counting
H	H	X	H	H	↑	Count up

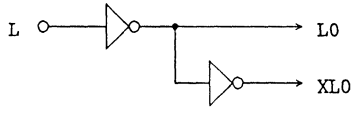
Note : The CO output produces a high level output data when the counter overflows.

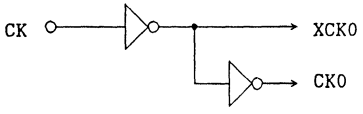
Cell Name
C43

Equivalent Circuit



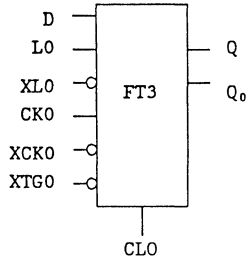






FT3 (Flip-Flop for Counter)(not Unit Cell)

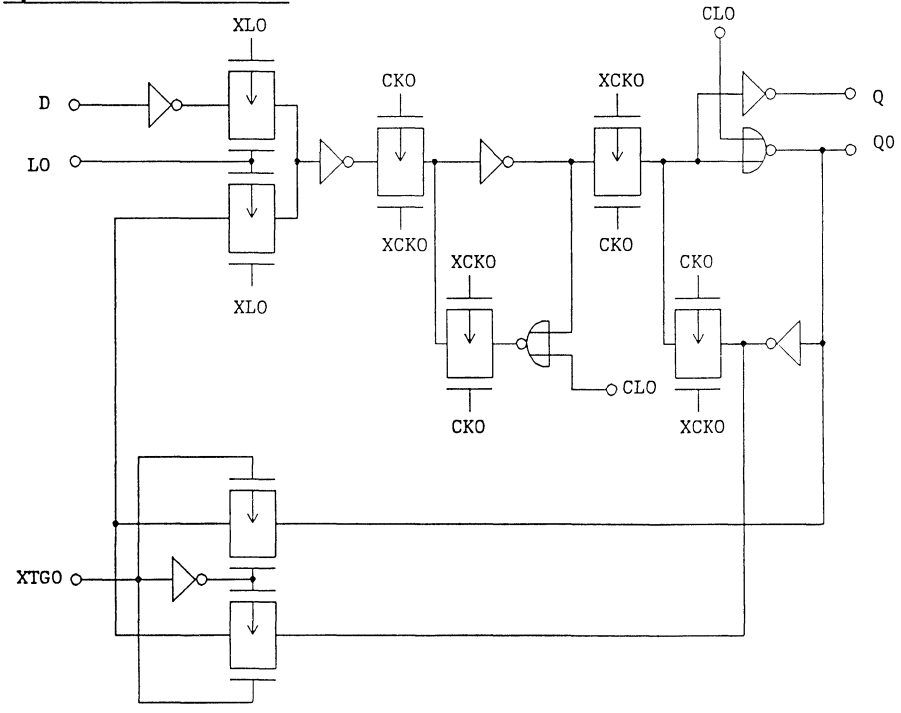
Symbol



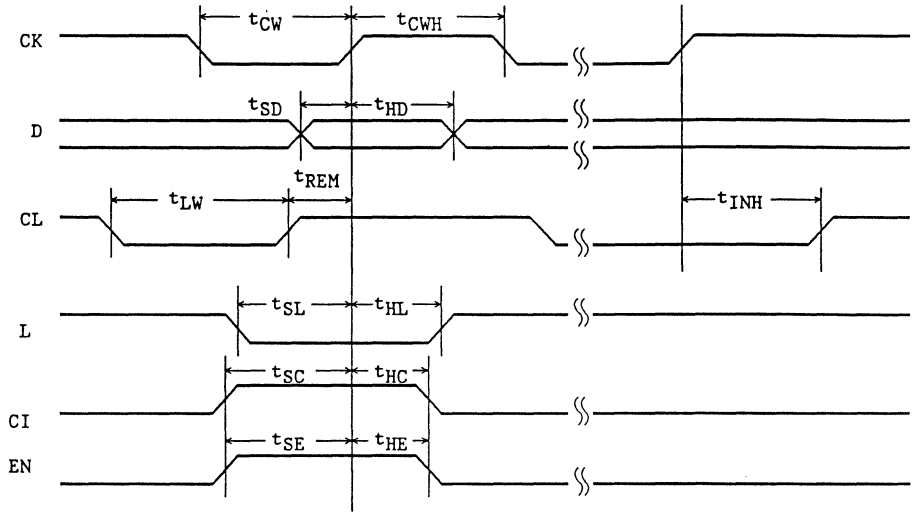
Function Table

LO	D	XTGO	CLO	CK	Q(Q0)
X	X	X	H	X	L
H	H	X	L	↑	H
H	L	X	L	↑	L
L	X	H	L	↑	Q(Q0)
L	X	L	L	↑	$\overline{Q}(\overline{Q0})$

Equivalent Circuit of FT3

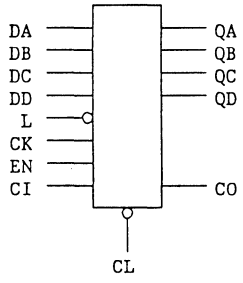


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
C45	Non-SCAN 4-bit Binary Synchronous Up Counter	48

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.14	0.11	1.50	0.07	0.11	4	CK → Q
4.06	0.14	2.26	0.07			CK → CO
1.53	0.14	1.09	0.07			CI → CO

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Data Setup Time	tSD	3.1
Data Hold Time	tHD	1.7
Load Setup Time	tSL	4.0
Load Hold Time	tHL	1.7
CI Setup Time	tSC	5.3
CI Hold Time	tHC	1.6
EN Setup Time	tSE	5.3
EN Hold Time	tHE	1.6
Clear Setup Time	tSR	3.1
Clear Hold Time	tHR	1.6

Pin Name	Input Loading Factor (ℓu)
D	1
L,EN	1
CK,CL	1
CI	2

Pin Name	Output Driving Factor (ℓu)
Q	18
CO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

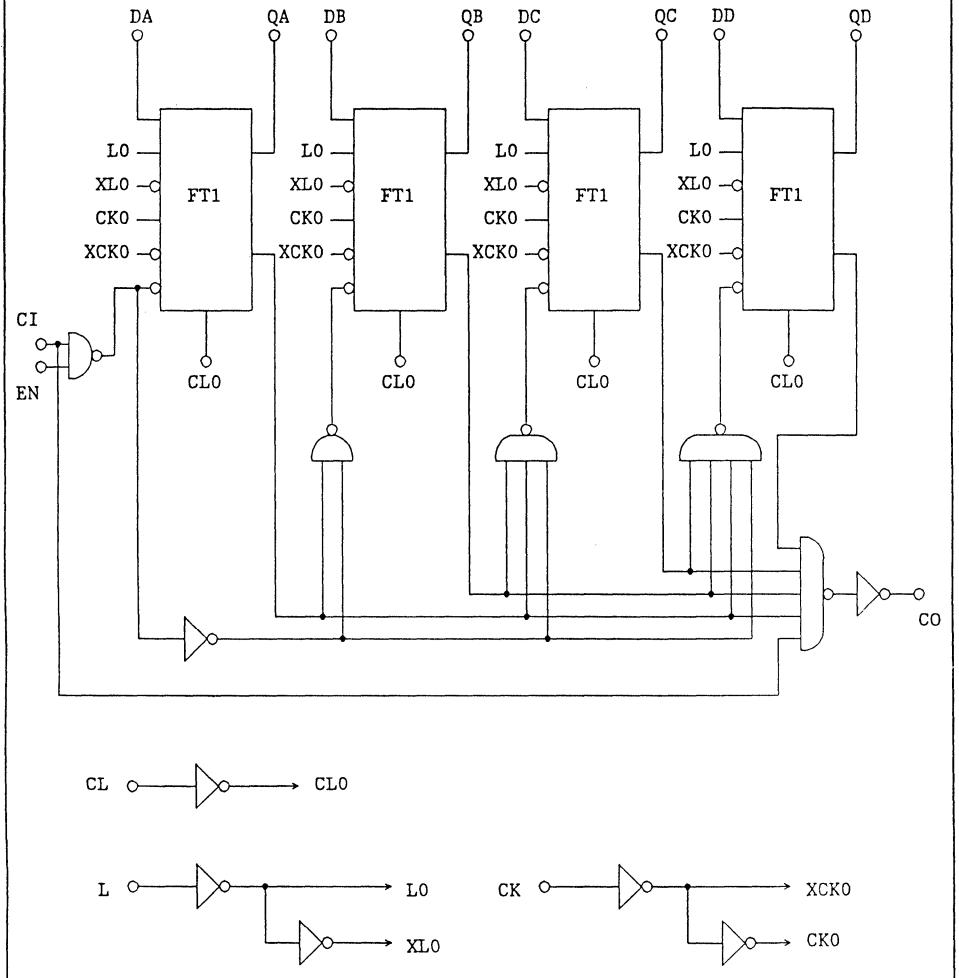
Function Table

Inputs						Outputs
CL	L	D	EN	CI	CK	Q
L	X	X	X	X	↑	L
H	L	H	X	X	↑	H
H	L	L	X	X	↑	L
H	H	X	X	L	X	No Counting
H	H	X	L	X	X	No Counting
H	H	X	H	H	↑	Count up

Note : The CO output produces a high level output data when the counter overflows.

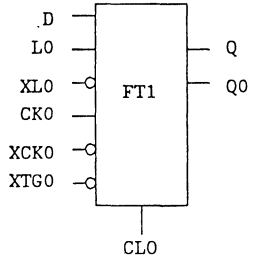
Cell Name
C45

Equivalent Circuit



FT1 (Flip-Flop for Counter)(not Unit Cell)

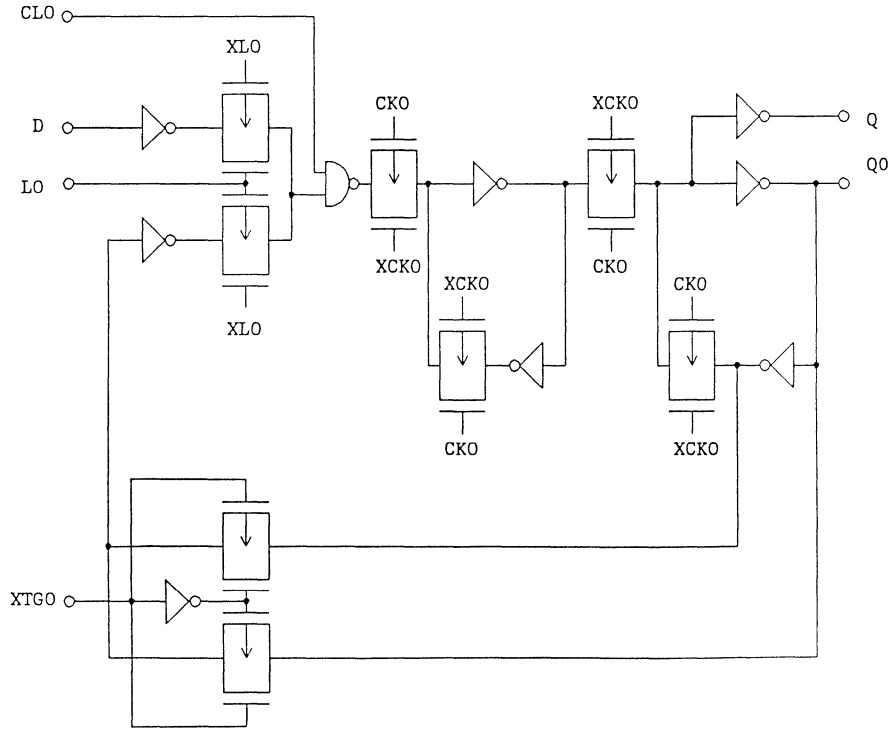
Symbol



Function Table

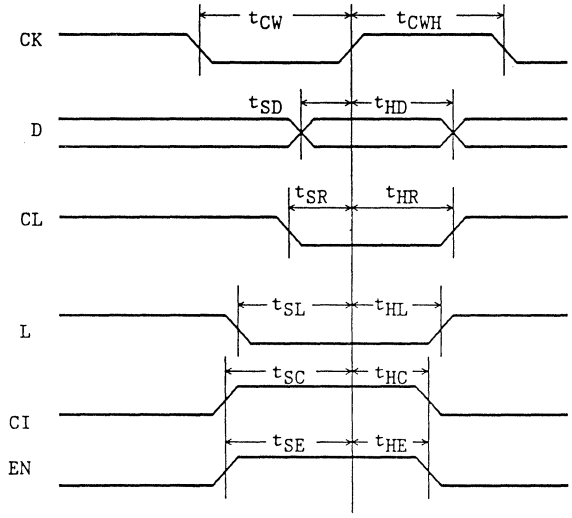
LO	D	XTGO	CLO	CK	Q(QO)
L	X	X	H	↑	L
H	H	X	L	↑	H
H	L	X	L	↑	L
L	X	H	L	↑	Q(QO)
L	X	L	L	↑	$\overline{Q(QO)}$

Equivalent Circuit of FT3



Cell Name
C45

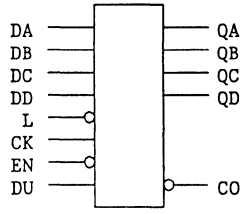
Definition of Parameters



2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
C47	Non-SCAN 4-bit Binary Synchronous Up/Down Counter	68

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.19	0.13	2.87	0.13	0.20	4	CK → Q
4.33	0.09	4.90	0.07			CK → CO
4.01	0.13	4.43	0.13	0.20	4	L → Q
1.98	0.09	2.41	0.07			DU → CO

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.5
Clock Pause Time	tCWH	7.2
Data Setup Time	tSD	0.6
Data Hold Time	tHD	1.5
DU Setup Time	tSU	4.3
DU Hold Time	tHU	0.7
EN Setup Time	tSE	4.0
EN Hold Time	tHE	1.0
Clear Release Time	tREM	1.9
Clear Hold Time	tINH	8.9
Load Pulse Width	tLW	4.0

Pin Name	Input Loading Factor (ℓu)
D	1
L	2
DU	1
CK	1
EN	3

Pin Name	Output Driving Factor (ℓu)
Q	18
CO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

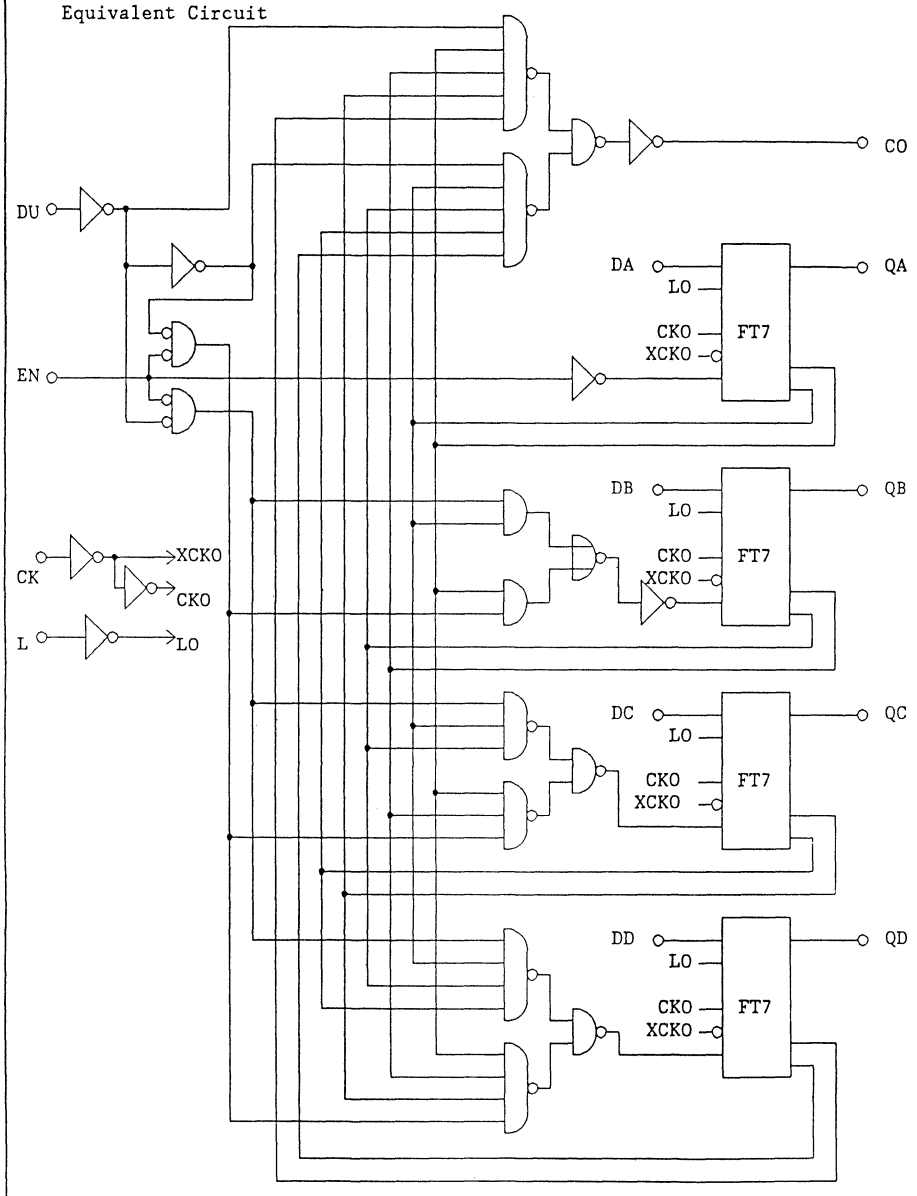
Function Table

Inputs					Outputs
Q	L	EN	DU	CK	Q
H	L	X	X	X	H
L	L	X	X	X	L
X	H	H	X	↑	No Counting
X	H	L	L	↑	Count Up
X	H	L	H	↑	Count Down

Note : The CO output produces a low level output pulse when the counter overflows or underflows.

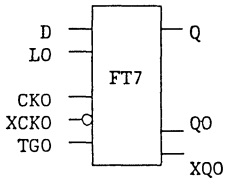
Cell Name
C47

Equivalent Circuit



FT7 (Flip-Flop for Counter)(not Unit Cell)

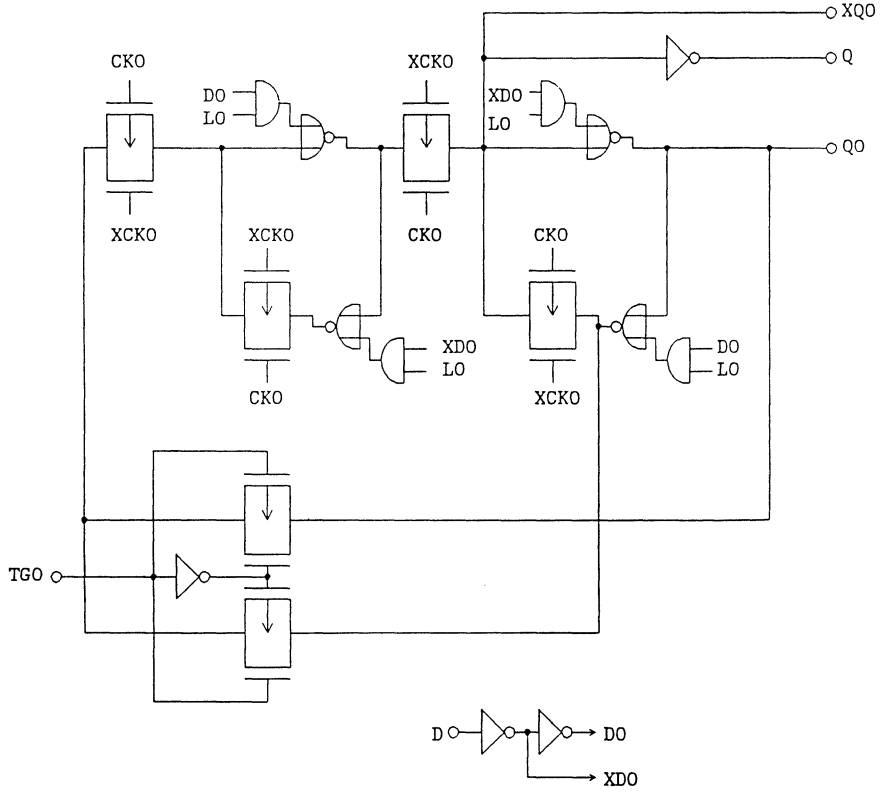
Symbol



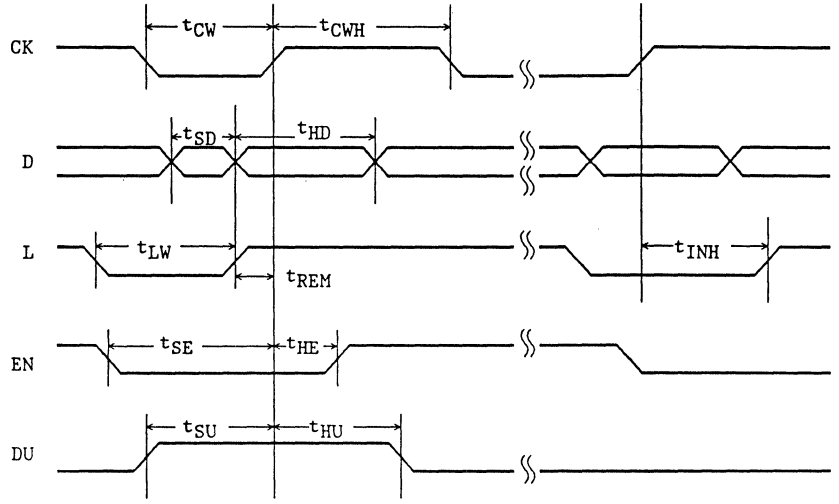
Function Table

Inputs				Outputs	
LO	D	TGO	CKO	QO(Q)	$\overline{Q}$(QO)
H	H	X	X	H	L
H	L	X	X	L	H
L	X	L	↑	Qn-1	$\overline{Qn-1}$
L	X	H	↑	$\overline{Qn-1}$	Qn-1

Equivalent Circuit of FT7

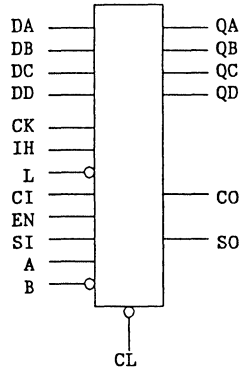


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SC43	SCAN 4-bit Synchronous Binary Up Counter with Asynchronous Clear	59

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.42	0.13	3.29	0.07	0.10	4	CK → Q
4.12	0.13	4.40	0.07	0.10	4	CK → CO
-	-	2.09	0.07	0.10	4	CL → Q
1.46	0.13	1.00	0.07	0.10	4	CI → CO
-	-	2.86	0.07	0.10	4	CL → CO

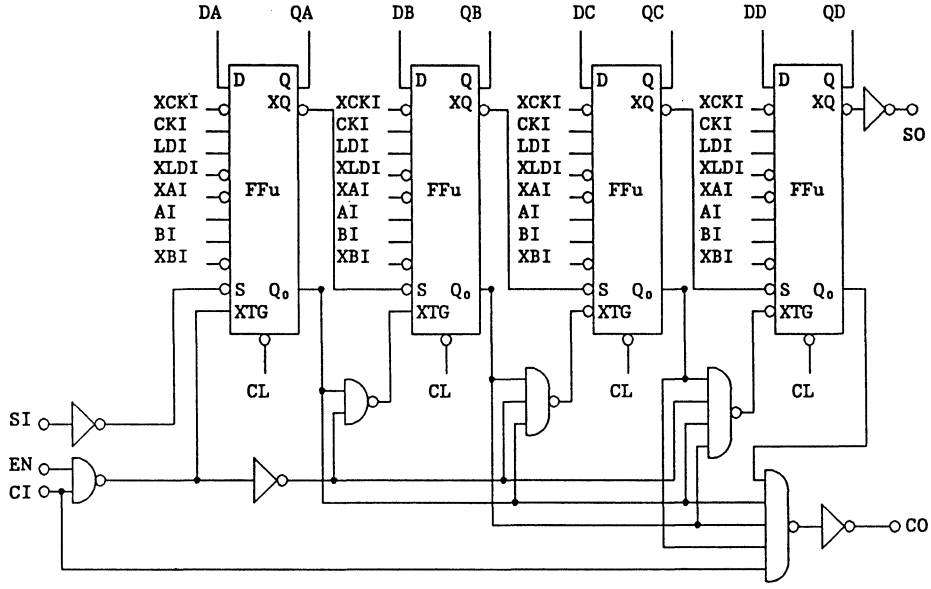
Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.1
Clock Pause Time	tCWH	5.9
Data Setup Time	tSD	1.6
Data Hold Time	tHD	1.7
Load Setup Time	tSL	2.4
Load Hold Time	tHL	2.0
CI Setup Time	tSC	3.2
CI Hold Time	tHC	1.4
EN Setup Time	tSE	3.2
EN Hold Time	tHE	1.4
Clear Pulse Width	tLW	5.0
Clear Release Time	tREM	1.2
Clear Hold Time	tINH	4.6

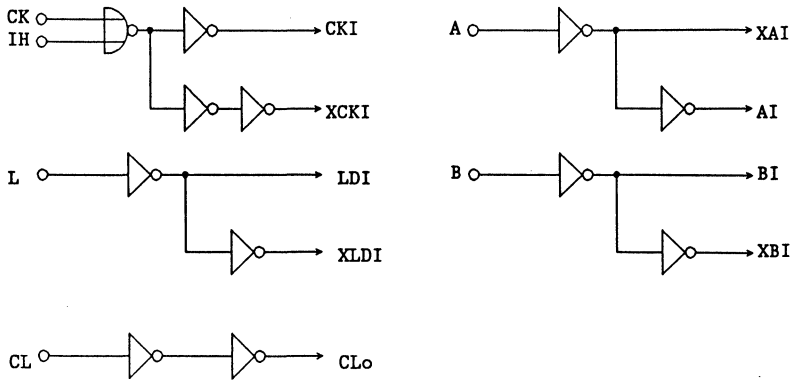
Pin Name	Input Loading Factor (ℓu)
D	2
CK,IH	1
L,CL,SI	1
EN	1
A,B,CI	2

Pin Name	Output Driving Factor (ℓu)
Q	18
CO	18
SO	18

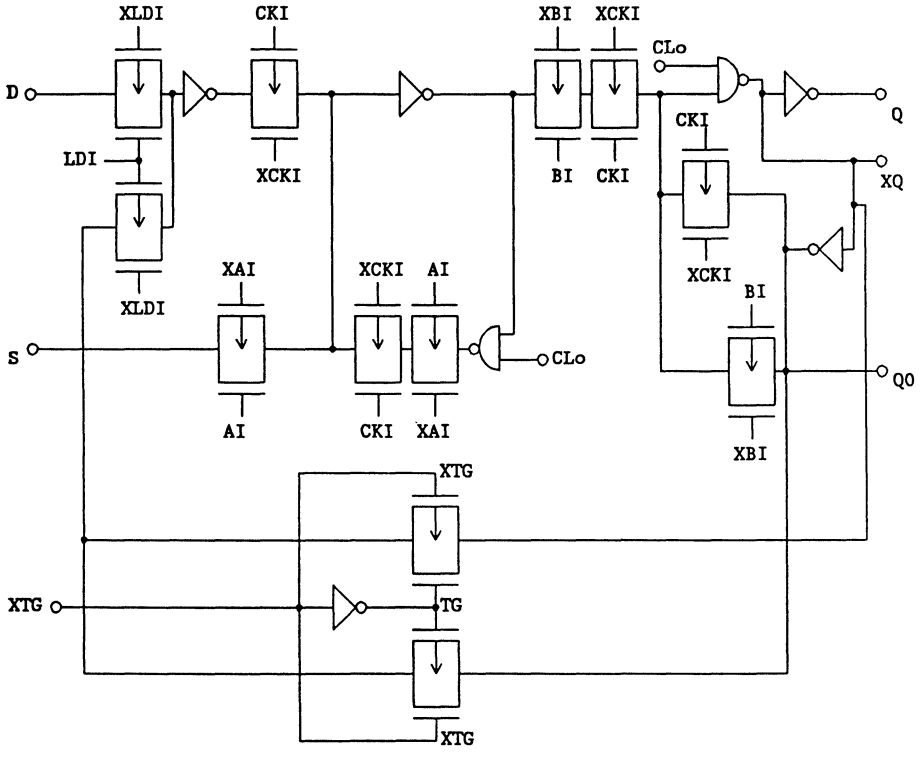
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



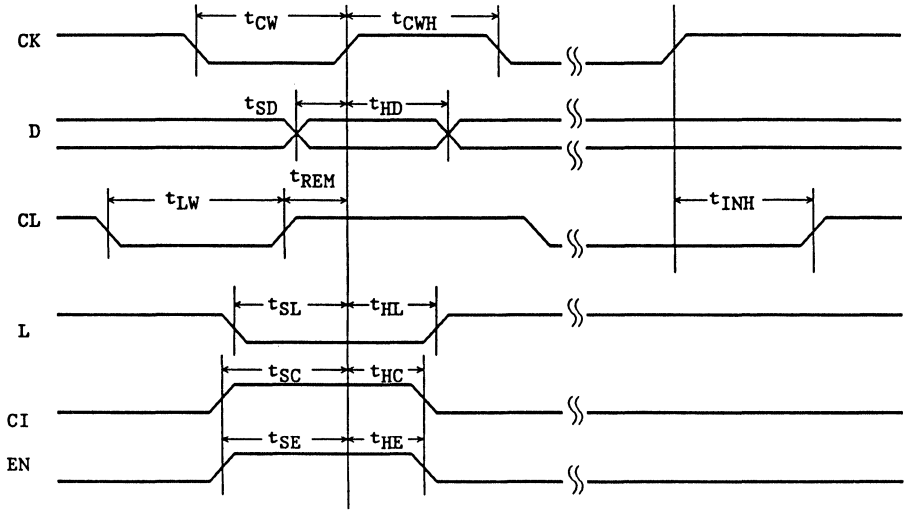


Equivalent Circuit (FFu)



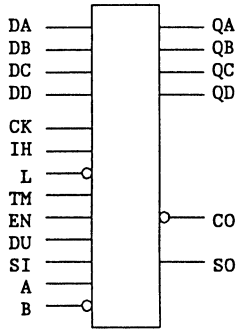
Cell Name
SC43

Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SC47	SCAN 4-bit Synchronous Binary Up/Down Counter	78

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.60	0.13	3.76	0.15	0.20	4	CK → Q
4.90	0.13	6.96	0.07			CK → CO
1.88	0.13	2.35	0.07			DU → CO

Parameter	Symbol	Typ(ns)*
Clock Pulse Width (H)	tCWH	8.8
Clock Pause Time (L)	tCWL	7.3
Data Setup Time	tSD	10.7
Data Hold Time	tHD	1.7
EN Setup Time	tSE	6.3
EN Hold Time	tHE	0.6
DU Input Setup Time	tSU	7.1
DU Input Hold Time	tHU	0.4
Load Pulse Width	tLW	15.4
Load Release Time	tREM	2.9
Load Hold Time	tINH	12.2

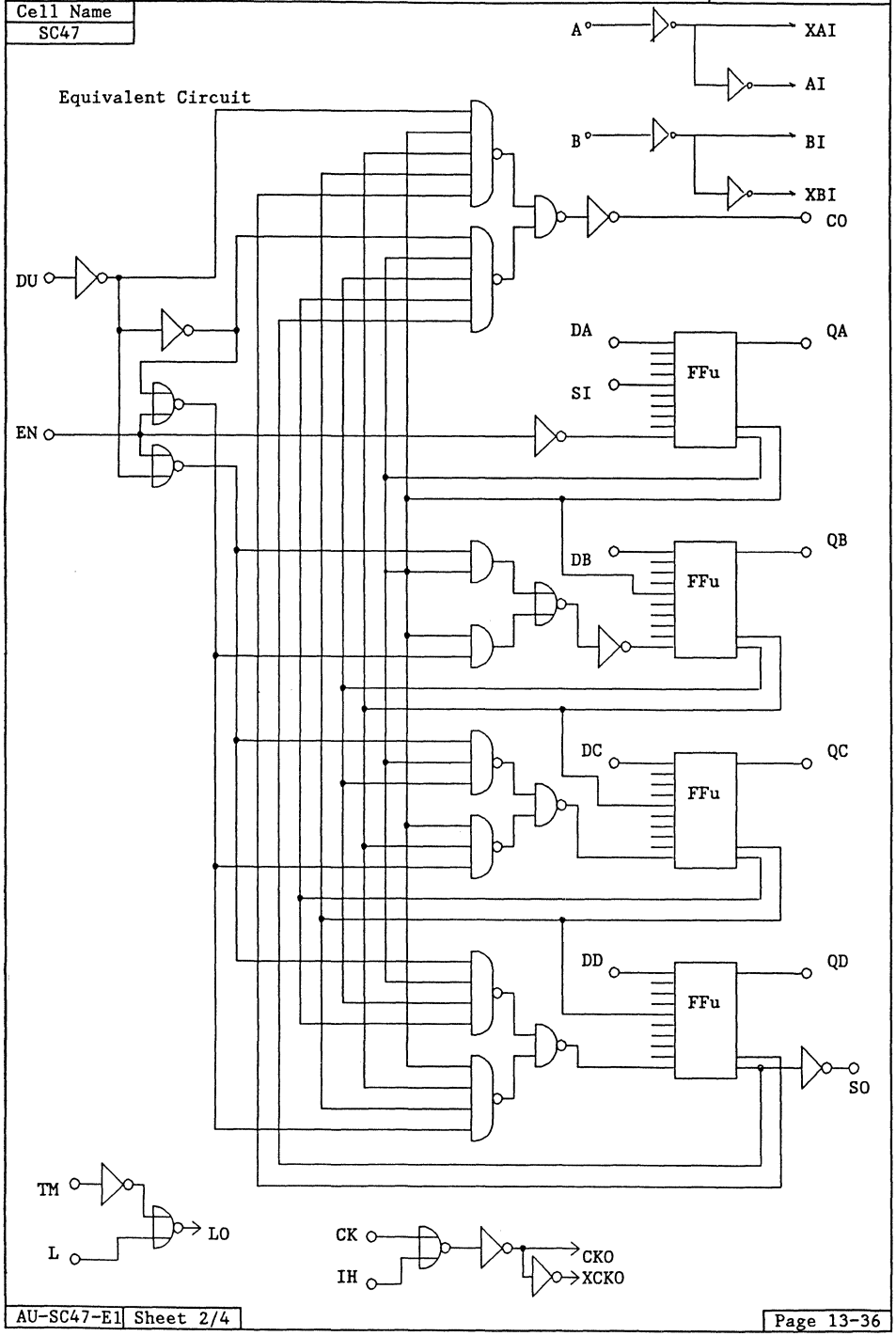
Pin Name	Input Loading Factor (ℓu)
D	2
CK,IH,TM,L	1
EN	3
DU,A,B	1
SI	2

Pin Name	Output Driving Factor (ℓu)
Q	18
SO	18
CO	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

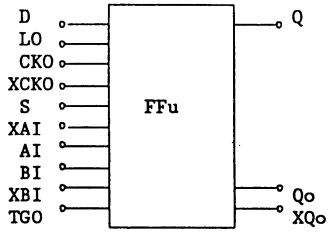
Cell Name
SC47

Equivalent Circuit

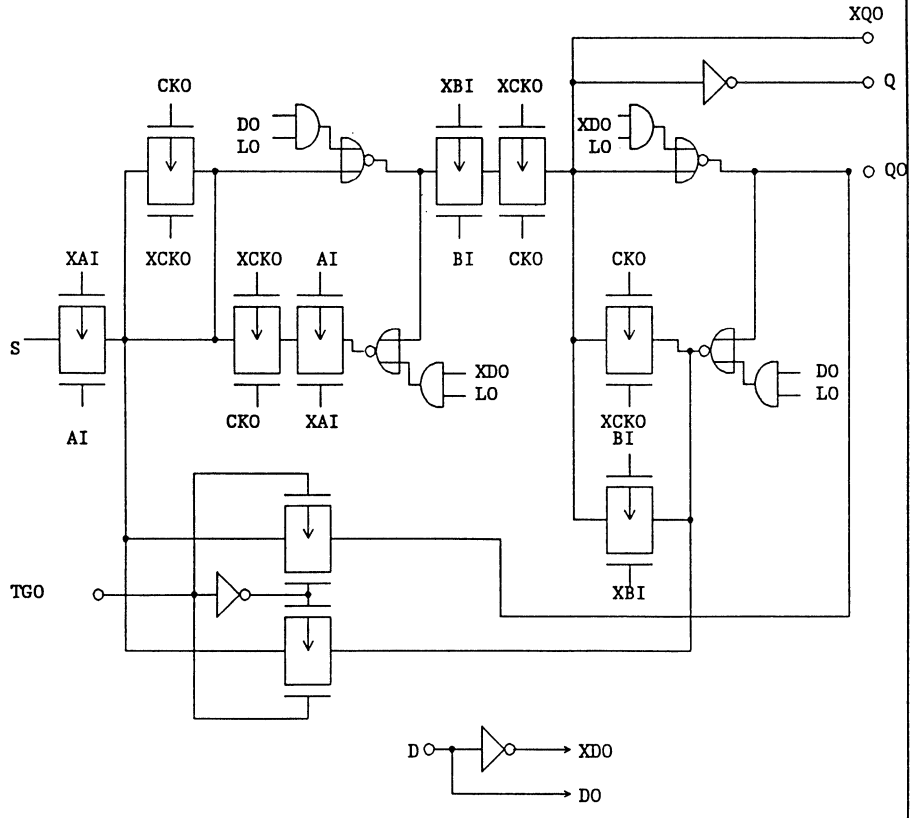


Cell Name
SC47

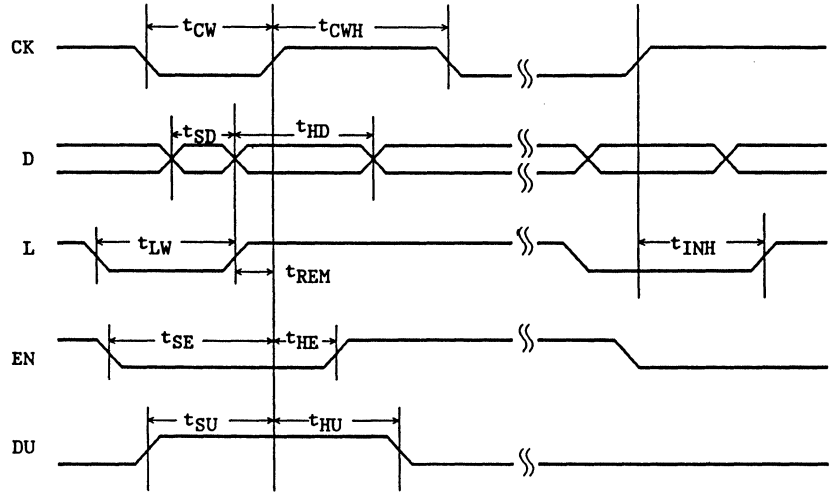
Symbol



Equivalent Circuit (FFu)



Definition of Parameters

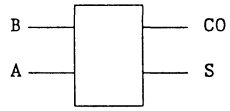


Adder and ALU Family

Page	Unit Cell Name	Function	Basic Cells
2–249	A1A	1-bit Half Adder	5
2–250	A1N	1-bit Full Adder	8
2–251	A2N	2-bit Full Adder	16
2–253	A4H	4-bit Binary Full Adder with Fast Carry	48

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
A1A	1-bit Half Adder	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.98	0.07	1.15	0.03			A → S
0.87	0.07	1.17	0.03			B → S
0.90	0.07	1.00	0.03			A → CO
1.02	0.07	0.92	0.03			B → CO

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2
B	2

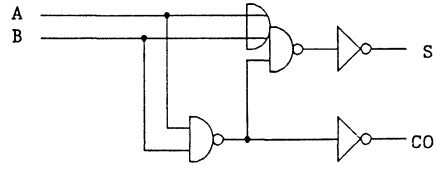
Pin Name	Output Driving Factor (ℓu)
CO	36
S	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

A	B	CO	S
L	L	L	L
L	H	L	H
H	L	L	H
H	H	H	L

Equivalent Circuit



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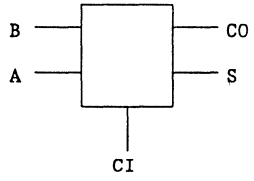
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
A1N	1-bit Full Adder	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.11	0.13	2.52	0.07			A,B → S
1.00	0.13	1.08	0.07			CI → S
2.39	0.13	1.91	0.07			A,B → CO
0.82	0.13	0.94	0.07			CI → CO

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	3
B	3
CI	3

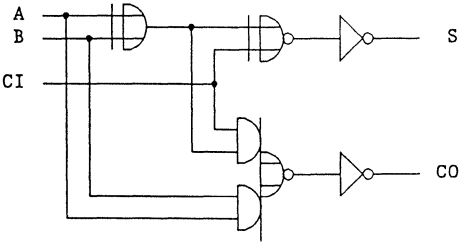
Pin Name	Output Driving Factor (ℓu)
CO	18
S	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

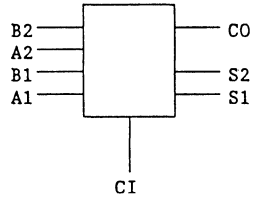
Inputs			Outputs	
A	B	CI	S	CO
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
H	H	L	L	H
L	L	H	H	L
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
A2N	2-bit Full Adder	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.28	0.23	2.25	0.11			A1 → CO
2.19	0.23	2.30	0.11			B1 → CO
1.27	0.23	1.09	0.07	0.10	4	A2 → CO
1.18	0.23	1.09	0.07	0.10	4	B2 → CO
2.23	0.23	2.07	0.11			CI → CO
2.38	0.18	2.20	0.11			A1 → S1
2.38	0.18	2.20	0.11			B1 → S1
0.95	0.18	0.95	0.11			CI → S1
2.26	0.18	2.20	0.11			A1 → S2
2.49	0.18	2.36	0.11			A2 → S2
2.17	0.18	2.25	0.11			B1 → S2
2.49	0.18	2.36	0.11			B2 → S2
2.21	0.18	2.02	0.11			CI → S2

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A,B	2
CI	2

Pin Name	Output Driving Factor (ℓu)
S	14
CO	14

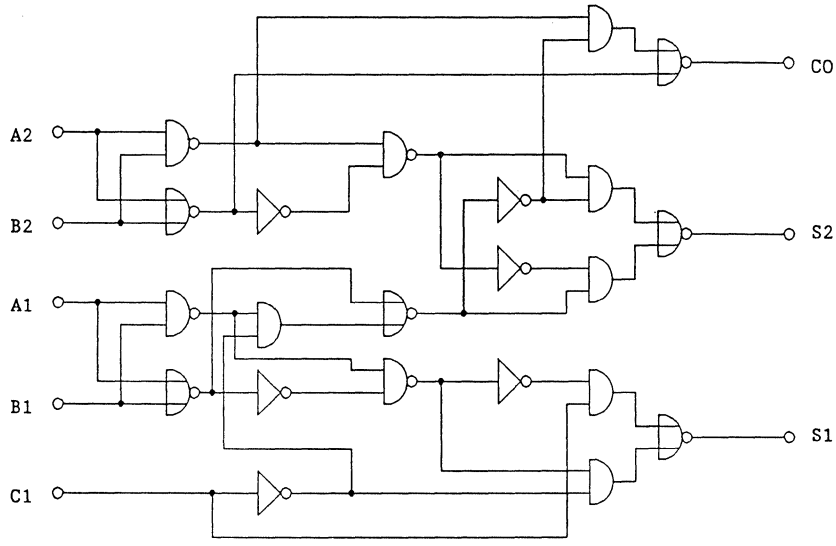
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs				Outputs					
				CI = L			CI = H		
A1	B1	A2	B2	S1	S2	CO	S1	S2	CO
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

Cell Name
A2N

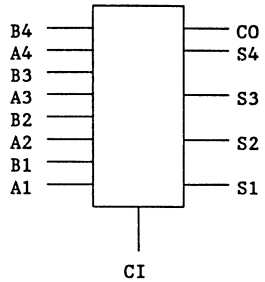
Equivalent Circuit



2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
A4H	4-bit Binary Full Adder with Fast Carry	48

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.95	0.18	1.31	0.11			CI → S1
2.12	0.23	2.46	0.11			CI → S2
2.43	0.23	2.39	0.11			CI → S3
2.51	0.23	2.83	0.11			CI → S4
2.30	0.13	2.57	0.07			CI → CO
3.05	0.18	2.71	0.11			A1,B1 → S1
2.54	0.23	2.47	0.11			A1,B1 → S2
2.74	0.23	3.08	0.11			A1,B1 → S3
3.00	0.23	3.14	0.11			A1,B1 → S4
2.64	0.13	3.03	0.07			A1,B1 → CO
2.47	0.23	2.70	0.11			A2,B2 → S2
2.93	0.23	2.88	0.11			A2,B2 → S3
2.99	0.23	3.24	0.11			A2,B2 → S4
3.10	0.13	3.07	0.07			A2,B2 → CO
2.25	0.23	2.28	0.11			A3,B3 → S3
3.07	0.23	3.23	0.11			A3,B3 → S4
3.04	0.13	3.06	0.07			A3,B3 → CO
2.32	0.18	2.41	0.07	0.10	4	A4,B4 → S4
2.93	0.13	2.81	0.07			A4,B4 → CO

Pin Name	Input Loading Factor (ℓu)
A	2
B	2
CI	2

Pin Name	Output Driving Factor (ℓu)
CO	18
S1,S3,S4	14
S2	18

Function Table

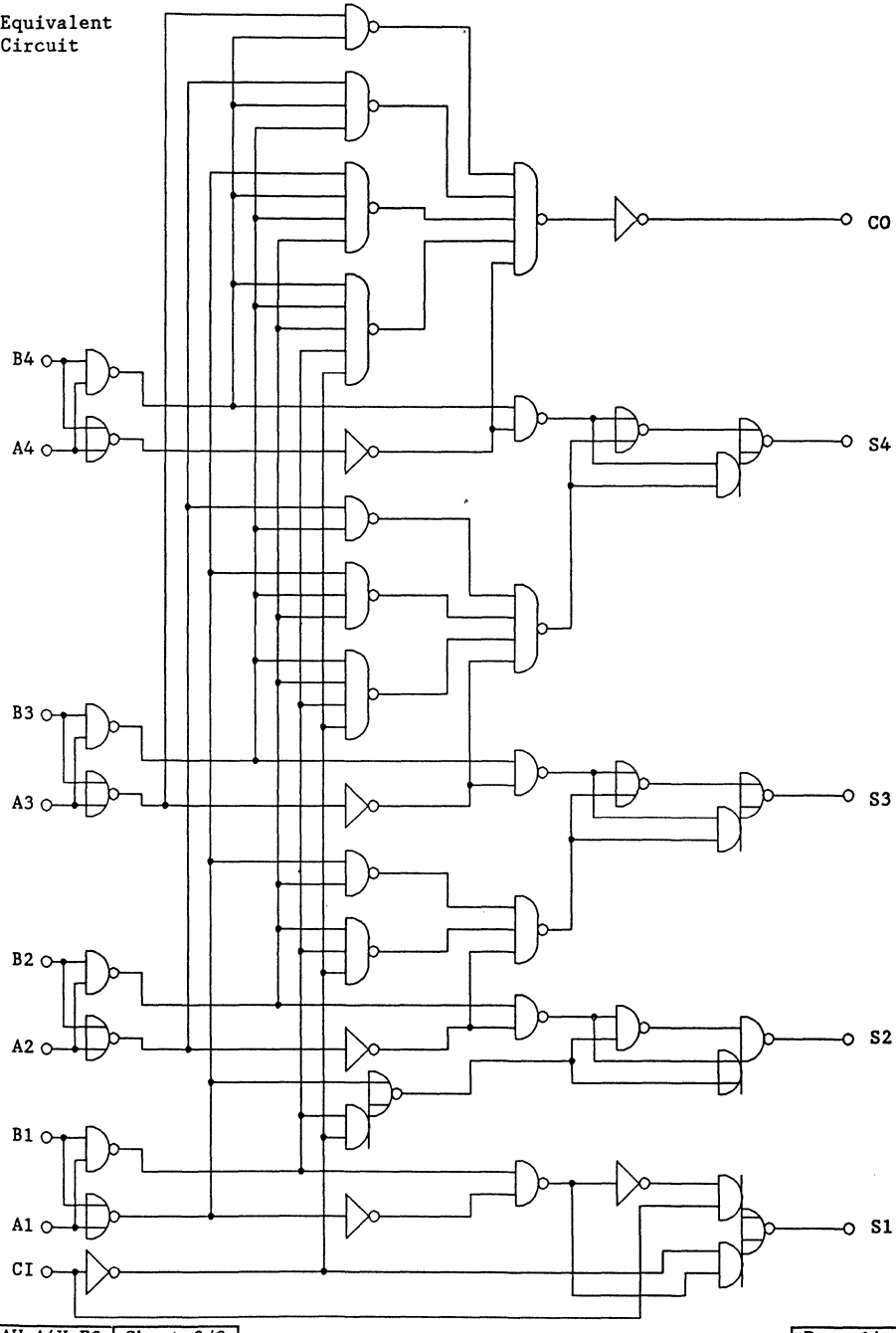
INPUT				OUTPUT					
				CI = L, C2 = L			CI = H, C2 = H		
A1 A3	B1 B3	A2 A4	B2 B4	S1 S3	S2 S4	C2 CO	S1 S3	S2 S4	C2 CO
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

Note :

Input conditions at A1, A2, B1, B2 and CI are used to determine outputs S1 and S2 and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4 and CO.

Cell Name
A4H

Equivalent
Circuit

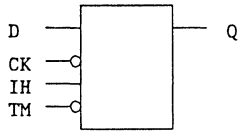


Data Latch Family

Page	Unit Cell Name	Function	Basic Cells
2–257	YL2	1-bit Data Latch with TM	5
2–259	YL4	4-bit Data Latch with TM	14
2–261	LTK	Data Latch	4
2–263	LTL	1-bit Data Latch with Clear	5
2–265	LTM	4-bit Data Latch with Clear	16
2–268	LT1	S–R Latch with Clear	4
2–270	LT4	4-bit Data Latch	14

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
YL2	1-bit Data Latch with TM	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.19	0.07	2.25	0.03			CK,IH → Q
0.93	0.07	1.03	0.03			D → Q

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	5.5
Data Setup Time	tSD	2.6
Data Hold Time	tHD	2.0

Pin Name	Input Loading Factor (ℓu)
D	2
CK	1
IH	1
TM	1

Pin Name	Output Driving Factor (ℓu)
Q	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

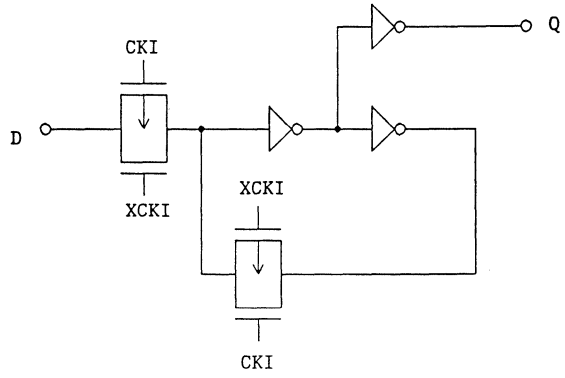
Note :

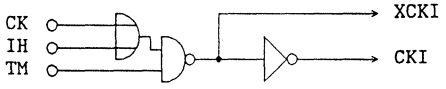
The TM terminal must be kept LOW during the SCAN Mode.

Function Table

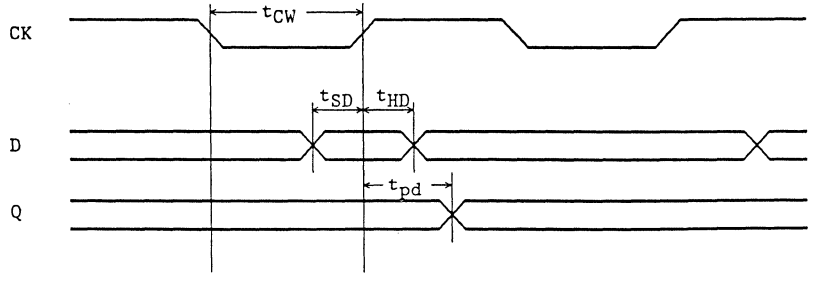
Input				Output	Mode
TM	IH	CK	D	Q	
L	X	X	D	D	SCAN
H	H	X	X	Q_0	LATCH
H	X	H	X	Q_0	
H	L	L	D	D	

Equivalent Circuit



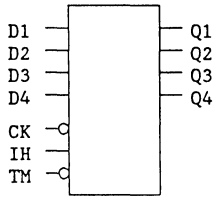


Definitions of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
YL4	4-bit Data Latch with TM	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.67	0.07	2.75	0.03			CK,IH → Q
0.88	0.07	1.03	0.03			D → Q

Parameter		Symbol	Typ(ns)*
Clock Pulse Width	(CK)	tCW	5.8
Data Setup Time	(D)	tSD	1.5
Data Hold Time	(D)	tHD	3.2

Pin Name	Input Loading Factor (ℓu)
D	2
CK	1
IH	1
TM	1

Pin Name	Output Driving Factor (ℓu)
Q	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Note :

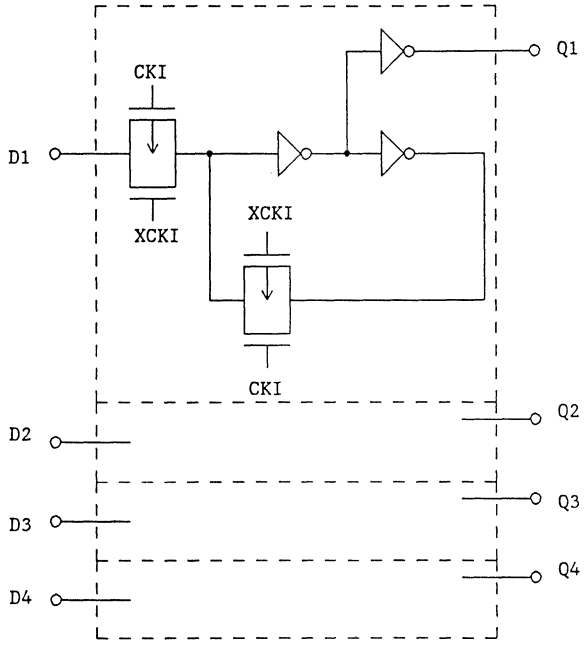
The TM terminal must be kept LOW during the SCAN Mode.

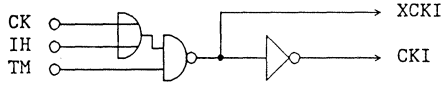
Function Table

Input				Output	Mode
TM	IH	CK	Dn	Qn	
L	X	X	D	D	SCAN
H	H	X	X	Qno	LATCH
H	X	H	X	Qno	
H	L	L	D	D	

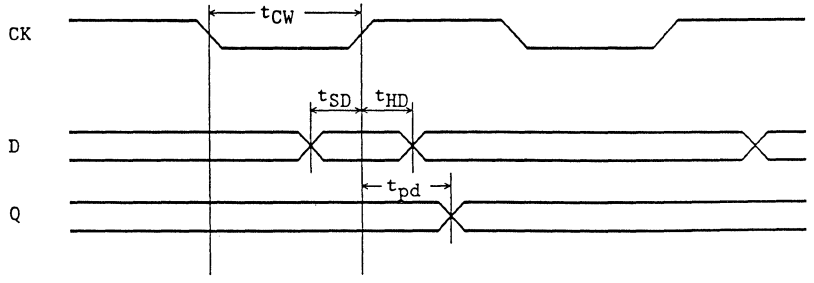
n = 1 ~ 4

Equivalent Circuit



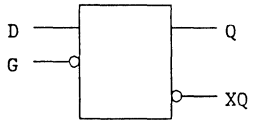


Definitions of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
LTK	Data Latch	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.83	0.13	0.92	0.07			D → Q
1.16	0.13	1.31	0.07			D → XQ
1.40	0.13	1.46	0.07			G → Q
1.70	0.13	1.87	0.07			G → XQ

Parameter	Symbol	Typ(ns)*
G Input Pulse Width	tGW	4.0
Data Setup Time	tSD	1.3
Data Hold Time	tHD	1.9

Pin Name	Input Loading Factor (ℓu)
D	2
G	1

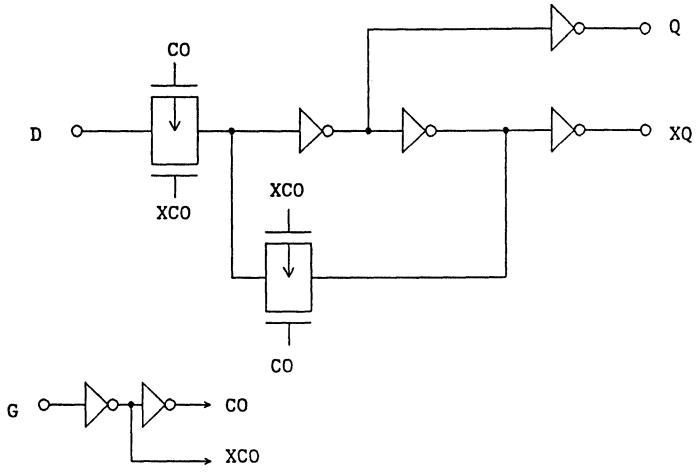
Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs		Outputs	
D	G	Q	XQ
X	H	Q_0	XQ_0
H	L	H	L
L	L	L	H

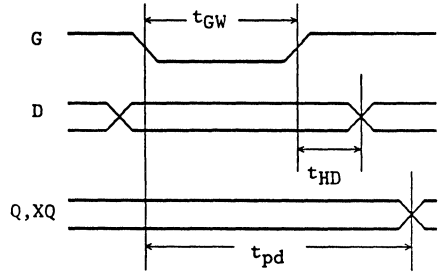
Equivalent Circuit



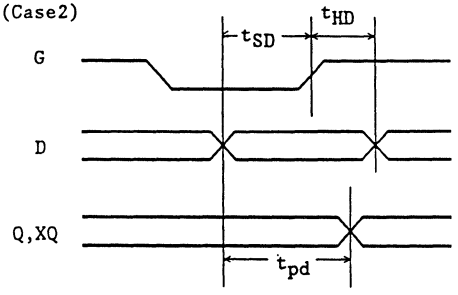
2

Definition of Parameters

(Case1)

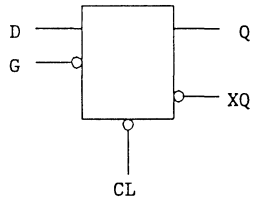


(Case2)



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
LTL	1-bit Data Latch with Clear	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	LD2	Path
1.11	0.13	0.68	0.07			CL → Q,XQ
0.95	0.13	0.98	0.07			D → Q
1.22	0.13	1.37	0.07			D → XQ
1.57	0.13	1.54	0.07			G → Q
1.78	0.13	2.01	0.07			G → XQ

Parameter	Symbol	Typ(ns)*
G Input Pulse Width	tGW	4.0
Data Setup Time	tSD	1.1
Data Hold Time	tHD	0.4
Clear Pulse Width	tLW	4.0

Pin Name	Input Loading Factor (ℓu)
D	2
G	1
CL	1

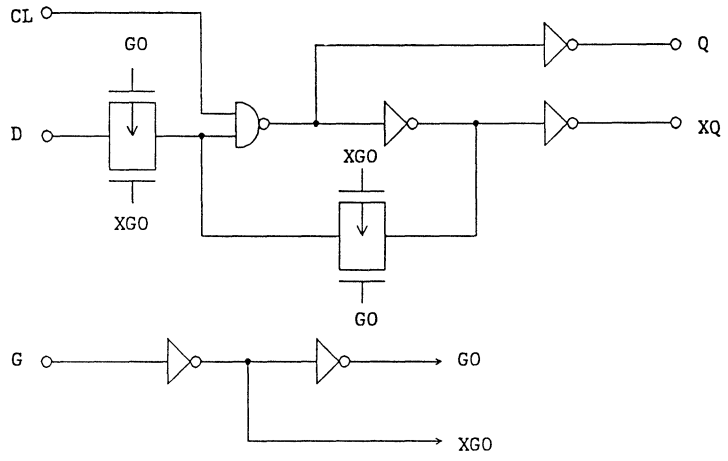
Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Funcion Table

Inputs			Outputs	
CL	D	G	Q	XQ
L	X	H	L	H
H	X	H	Q_0	XQ_0
H	H	L	H	L
H	L	L	L	H

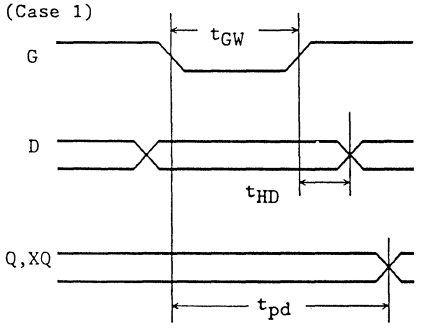
Equivalent Circuit



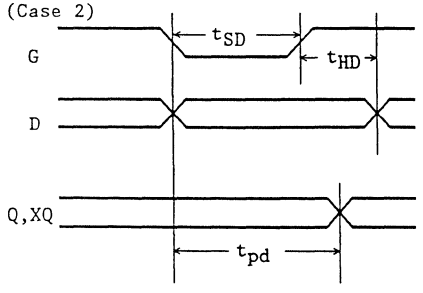
2

Definition of Parameters

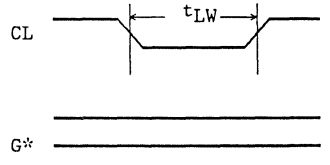
(Case 1)



(Case 2)



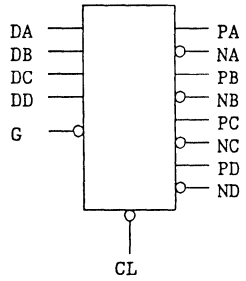
(Case 3)



Note*: G input must be high level at the time this latch is cleared.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
LTM	4-bit Data Latch with Clear	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.23	0.13	0.78	0.07			CL → P,N
0.98	0.13	1.03	0.07			D → P
1.28	0 13	1.43	0.07			D → N
2.09	0.13	1.96	0.07			G → P
2.19	0 13	2.52	0.07			G → N

Parameter	Symbol	Typ(ns)*
G Input Pulse Width	tGW	4.0
Clear Pulse Width	tLW	4.0
Data Setup Time	tSD	1.3
Data Hold Time	tHD	1.9

Pin Name	Input Loading Factor (ℓu)
D	2
G	1
CL	4

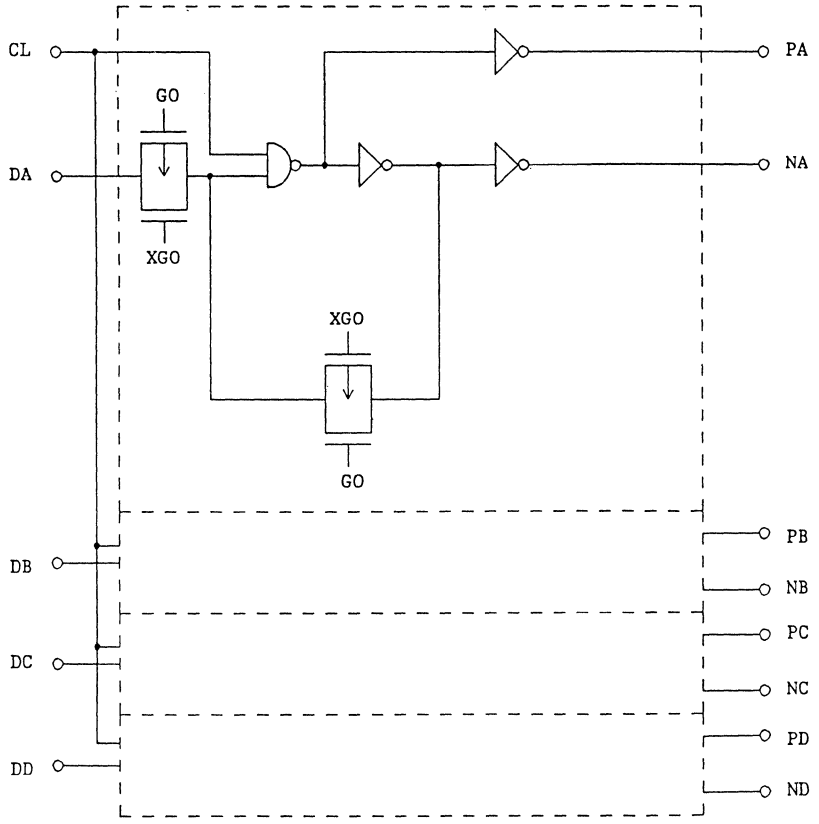
Pin Name	Output Driving Factor (ℓu)
P	18
N	18

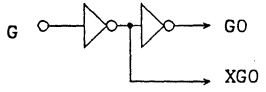
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs			Outputs	
CL	D	G	P	N
L	X	H	L	H
H	X	H	P_0	N_0
H	H	L	H	L
H	L	L	L	H

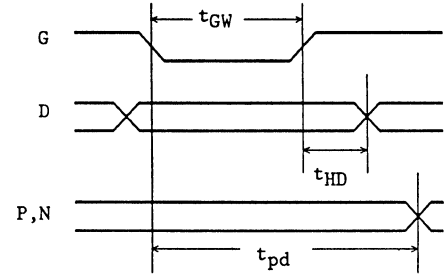
Equivalent Circuit



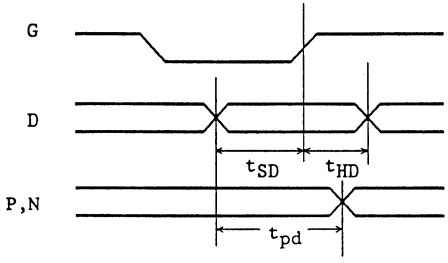


Definition of Parameters

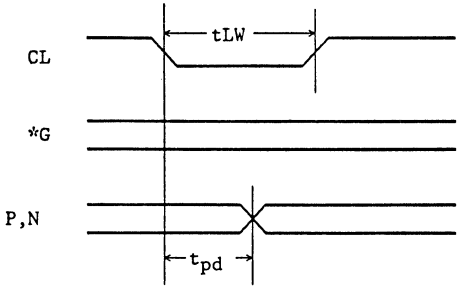
(Case1)



(Case2)



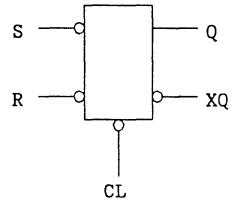
(Case3)



Note *: G input must be high level at the time this latch is cleared.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
LT1	S-R Latch with CLEAR	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.41	0.13	0.71	0.07			S → Q,XQ
1.25	0.13	0.83	0.07			R → Q,XQ
1.15	0.13	0.74	0.07			CL → Q,XQ

Parameter	Symbol	Typ(ns)*
Set Pulse Width	tSW	4.0
Reset Pulse Width	tRW	4.0
Clear Pulse Width	tLW	4.0

Pin Name	Input Loading Factor (ℓu)
S	1
R	1
CL	1

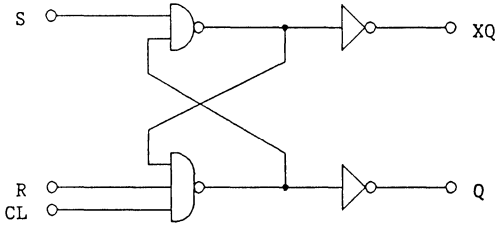
Pin Name	Output Driving Factor (ℓu)
Q	18
XQ	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

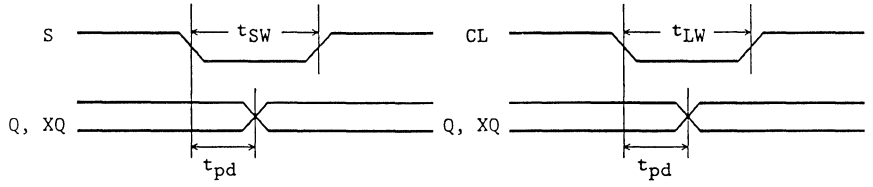
Function Table

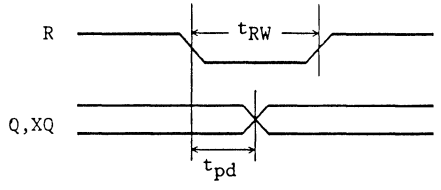
Inputs			Outputs	
CL	S	R	Q	XQ
L	H	H	L	H
H	H	H	Q_0	XQ_0
H	H	L	L	H
H	L	H	H	L
H	L	L	Inhibited	

Equivalent Circuit



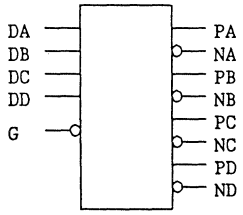
Definition of Parameters





Cell Name	Function	Number of BC
LT4	4-bit Data Latch	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.00	0.13	1.83	0.07			G → P
2.00	0.13	2.44	0.07			G → N
0.84	0 13	0.95	0.07			D → P
1.12	0.13	1.28	0.07			D → N

Parameter	Symbol	Typ(ns)*
G Input Pulse Width	tGW	4.0
Data Setup Time	tSD	1.3
Data Hold Time	tHD	1.9

Pin Name	Input Loading Factor (ℓu)
D	2
G	1

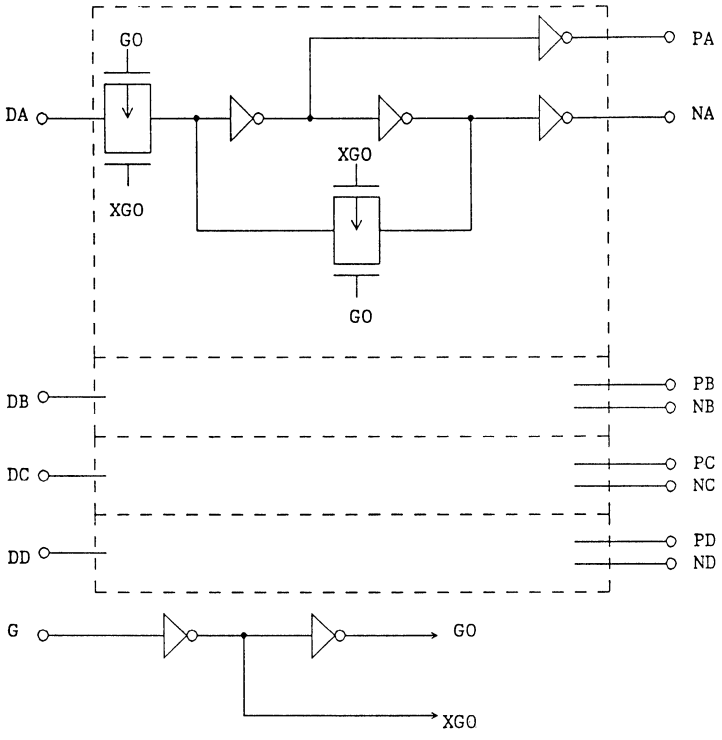
Pin Name	Output Driving Factor (ℓu)
P	18
N	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

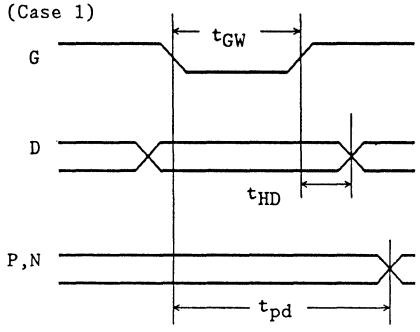
Inputs		Outputs	
D	G	P	N
H	H	P_0	N_0
L	H	P_0	N_0
H	L	H	L
L	L	L	H

Equivalent Circuit

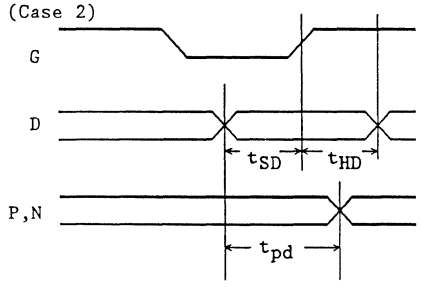


Definition of Parameters

(Case 1)



(Case 2)



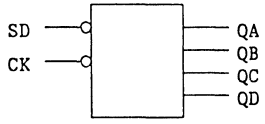
2

Shift Register Family

Page	Unit Cell Name	Function	Basic Cells
2–275	FS1	4-bit Serial-in Parallel-out Shift Register	18
2–277	FS2	4-bit Shift Register with Synchronous Load	30
2–279	FS3	4-bit Shift Register with Asynchronous Load	34
2–282	SR1	4-bit Serial-in Parallel-out Shift Register with Scan	36

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FS1	4-bit Serial-in Parallel-out Shift Register	18

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.94	0.13	2.51	0.07	0.10	4	CK → Q

Parameter		Symbol	Typ(ns)*
Clock Pulse Width		tCW	4.0
SD Setup Time		tSSD	0.5
SD Hold Time		tHSD	0.2
Clock Pause Time	C ≦ 16 ℓu	tCWL**	4.7
	16 < C ≦ 32 ℓu	tCWL**	6.8
	32 < C ≦ 48 ℓu	tCWL**	8.8

Pin Name	Input Loading Factor (ℓu)
SD	1
CK	1

Pin Name	Output Driving Factor (ℓu)
Q	16

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

** The value of tCWL depends on the load(C) connected to the output terminals, QA, QB, QC and QD.

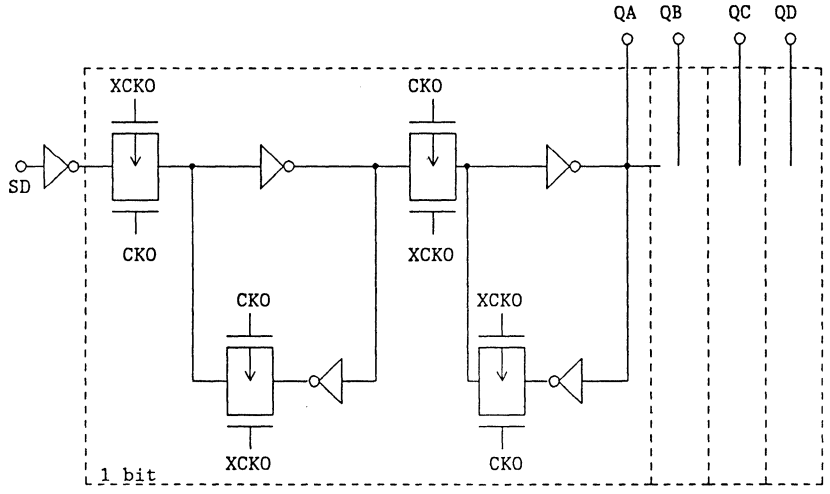
Function Table

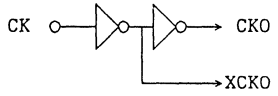
Inputs		Outputs			
SD	CK	QA	QB	QC	QD
SD	↓	$\overline{SD}$	QAn	QBn	QCn

Note: ·SD = H or L

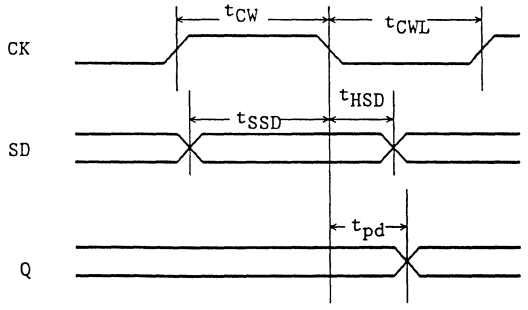
·QAn, QBn and QCn are levels of QA, QB and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

Equivalent Circuit



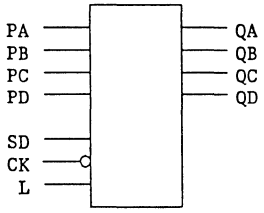


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FS2	4-bit Shift Register with Synchronous Load	30

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.86	0.13	2.51	0.07	0.10	4	CK → Q

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
SD Setup Time	tSSD	2.3
SD Hold Time	tHSD	1.0
Load Setup Time	tSL	3.5
Load Hold Time	tHL	0.4
P Setup Time	tSP	2.9
P Hold Time	tHP	1.2

Pin Name	Input Loading Factor (ℓu)
CK	1
SD	1
L	1
P	1

Pin Name	Output Driving Factor (ℓu)
Q	16

Clock Pause Time		
	C ≦ 16 ℓu	tCWL** 4.7
	16 < C ≦ 32 ℓu	tCWL** 6.8
	32 < C ≦ 48 ℓu	tCWL** 8.8

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

** The value of tCWL depends on the load(C) connected to the output terminals, QA, QB, QC and QD.

Function Table

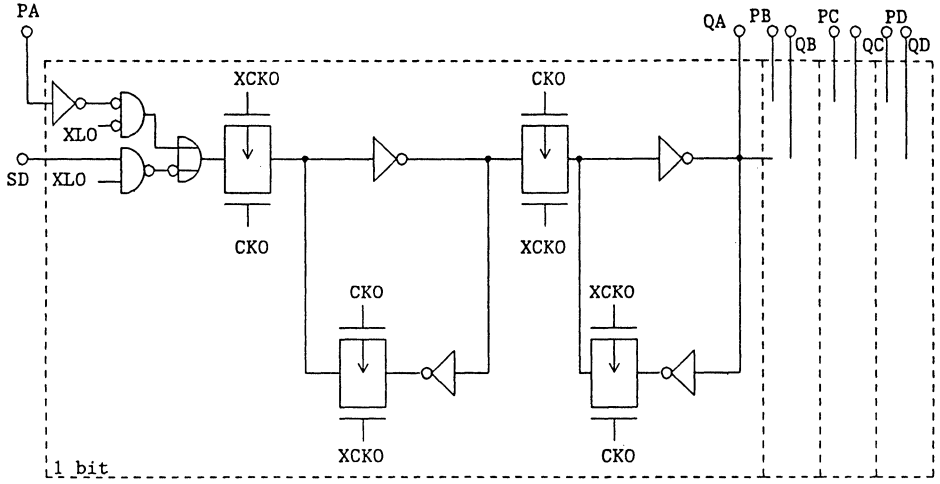
Inputs				Outputs			
SD	L	P	CK	QA	QB	QC	QD
SD	L	X	↓	SD	QAn	QBn	QCn
X	H	P	↓	PA	PB	PC	PD

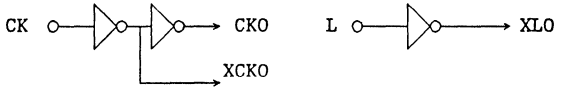
Note: ·SD = H or L

·QAn, QBn and QCn are levels of QA, QB and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

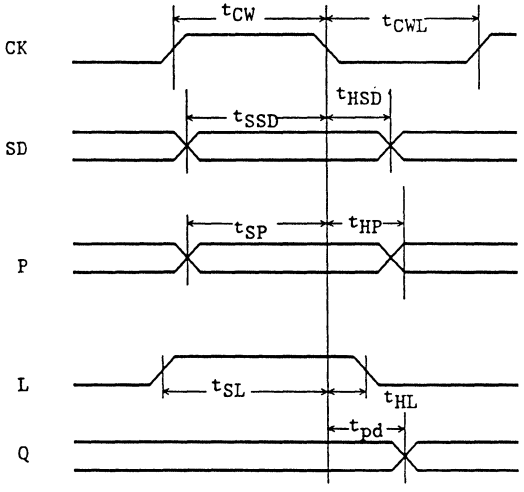
·P represents PA, PB, PC and PD.

Equivalent Circuit



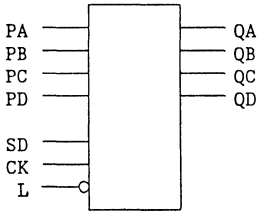


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
FS3	4-bit Shift Register with Asynchronous Load	34

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.83	0.14	1.70	0.09			CK → Q
3.71	0.14	2.80	0.09			L → Q
1.63	0.14	2.42	0.09			P → Q

Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.0
Clock Pause Time	tCWH	4.0
Load Pulse Width	tLW	5.0
SD Setup Time	tSSD	0.8
SD Hold Time	tHSD	1.4
P Setup Time	tSP	0.3
P Hold Time	tHP	1.9

Pin Name	Input Loading Factor (ℓu)
CK	2
SD	2
L	1
P	2

Pin Name	Output Driving Factor (ℓu)
Q	18

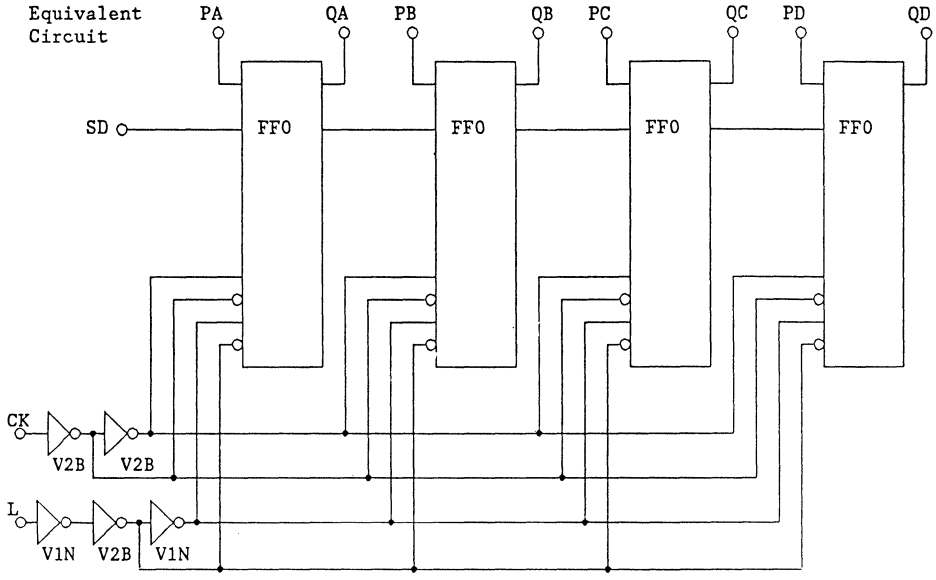
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs				Output
L	P	SD	CK	Q
L	L	X	X	L
L	H	X	X	H
H	X	L	↑	L
H	X	H	↑	H

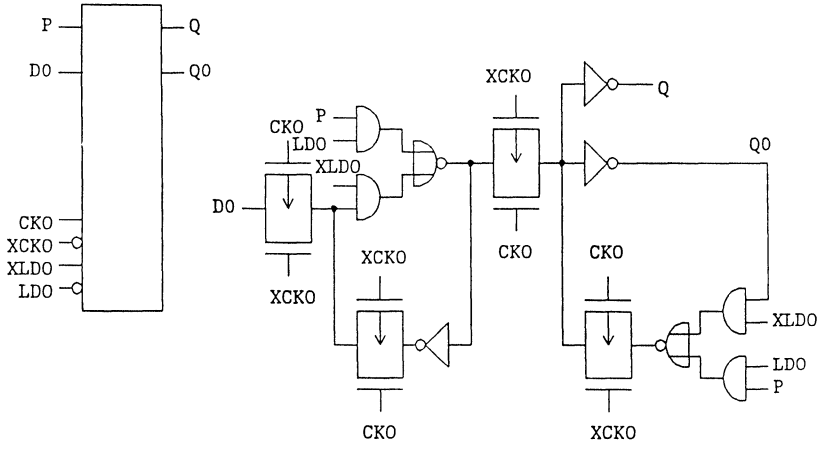
Cell Name
FS3

Equivalent Circuit

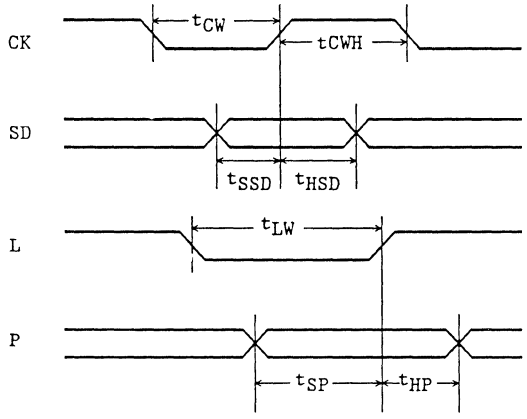


2

Equivalent Circuit of FF0

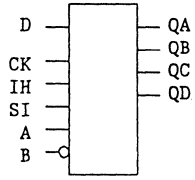


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
SR1	4-bit Serial-in Parallel-out Shift Register with SCAN	36

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.62	0.07	2.70	0.06	0.09	7	CK → Q
2.07	0.07	2.32	0.06	0.09	7	B → Q

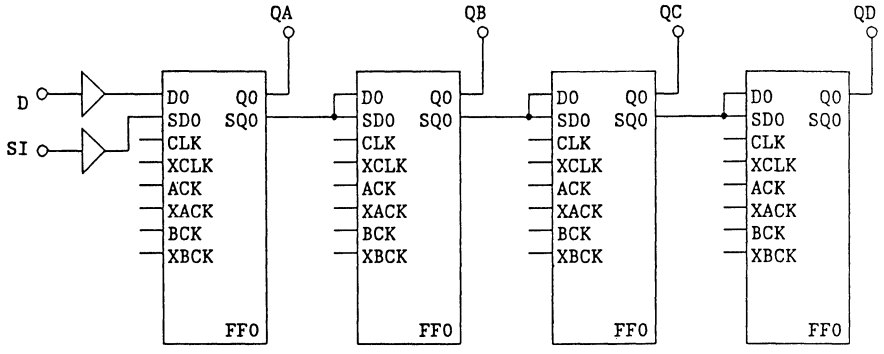
Parameter	Symbol	Typ(ns)*
Clock Pulse Width	tCW	4.4
Clock Pause TIme	tCWH	4.5
Data Setup Time	tSD	2.7
Data Hold Time	tHD	1.2

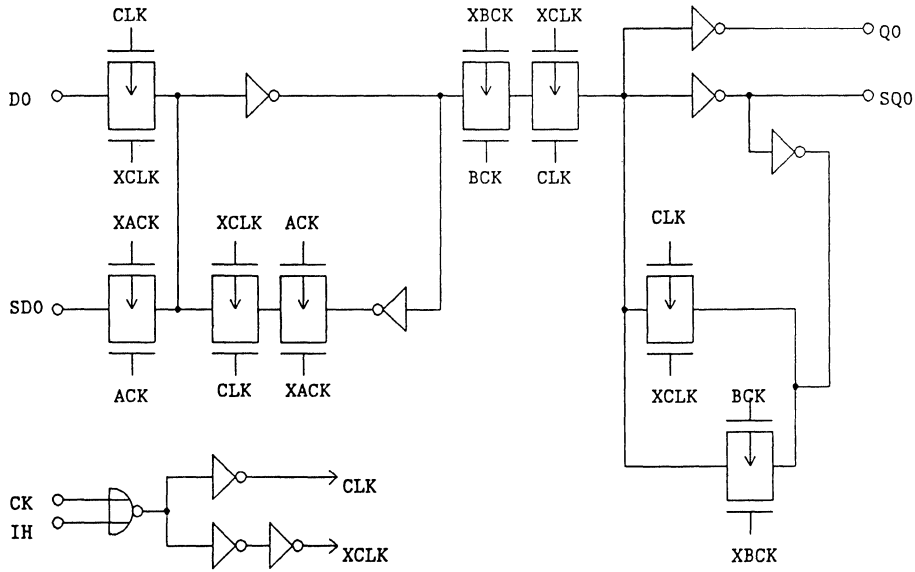
Pin Name	Input Loading Factor (ℓu)
D	1
CK	1
IH	1
SI	1
A,B	1

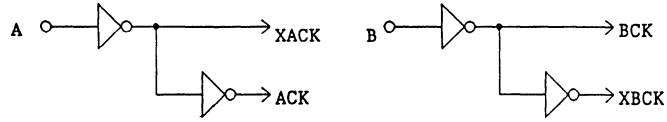
Pin Name	Output Driving Factor (ℓu)
Q	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name
SR1

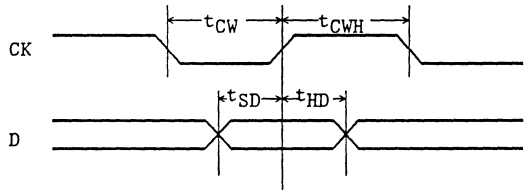






2

Definitions of Parameters

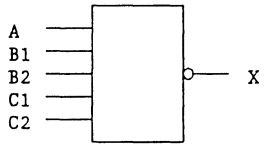


Parity Generator/Selector/Decoder Family

Page	Unit Cell Name	Function	Basic Cells
Parity Generators/Checkers			
2–287	PE5	5-bit Even Parity Generator/Checker	12
2–288	PO5	5-bit Odd Parity Generator/Checker	12
2–289	PE8	8-bit Even Parity Generator/Checker	18
2–290	PO8	8-bit Odd Parity Generator/Checker	18
2–291	PE9	9-bit Even Parity Generator/Checker	22
2–292	PO9	9-bit Odd Parity Generator/Checker	22
Data Selector			
2–293	P24	4-wide 2:1 Data Selector	12
Decoders			
2–294	DE2	2:4 Decoder	5
2–295	DE3	3:8 Decoder	15
2–297	DE4	2:4 Decoder with Enable	8
2–298	DE6	3:8 Decoder with Enable	30
Selectors			
2–300	T2B	2:1 Selector	2
2–301	T2C	Dual 2:1 Selector	4
2–303	T2D	2:1 Selector	2
2–304	T2E	Dual 2:1 Selector	5
2–305	T2F	2:1 Selector	8
2–307	T5A	4:1 Selector	5
2–309	V3A	1:2 Selector	2
2–310	V3B	Dual 1:2 Selector	4
Magnitude Comparator			
2–311	MC4	4-bit Magnitude Comparator	42

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
PE5	5-bit Even Parity Generator/Checker	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.10	0.07	2.73	0.03			A → X
2.10	0.07	2.62	0.03			B → X
3.31	0.07	3.87	0.03			C → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2
B	2
C	2

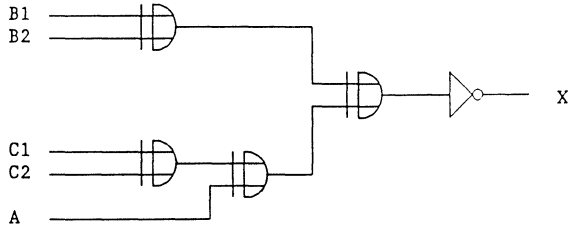
Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Σinput	X
Odd	L
Even	H

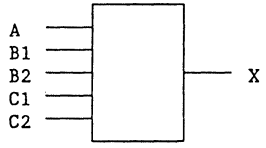
Equivalent Circuit



AU-PE5-E2	Sheet 1/1	Page 17-1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
P05	5-bit Odd Parity Generator/Checker	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.11	0.07	2.46	0.03			A → X
2.29	0.07	2.43	0.03			B → X
3.35	0.07	3.65	0.03			C → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2
B	2
C	2

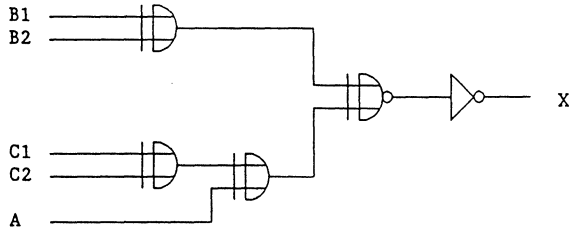
Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Σinput	X
Odd	H
Even	L

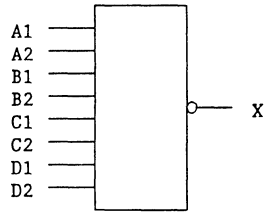
Equivalent Circuit



AU-P05-E2	Sheet 1/1	Page 17-2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
PE8	8-bit Even Parity Generator/Checker	18

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.08	0.13	3.47	0.07			A → X
3.15	0.13	3.54	0.07			B → X
3.15	0.13	3.52	0.07			C → X
3.22	0.13	3.59	0.07			D → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2
B	2
C	2
D	2

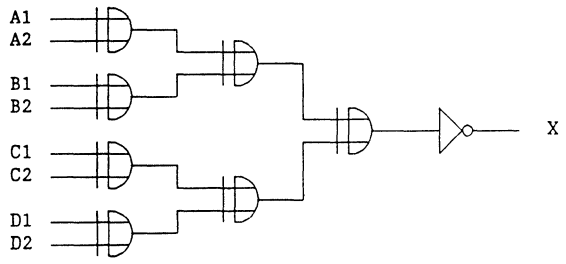
Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

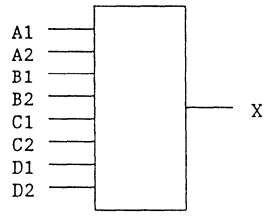
Σinput	X
Odd	L
Even	H

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
P08	8-bit Odd Parity Generator/Checker	18

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.02	0.13	3.43	0.07			A → X
3.09	0.13	3.50	0.07			B → X
3.10	0.13	3.37	0.07			C → X
3.17	0.13	3.41	0.07			D → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2
B	2
C	2
D	2

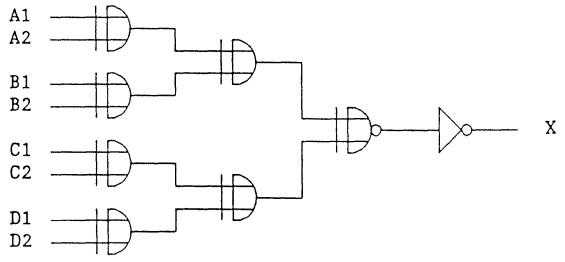
Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

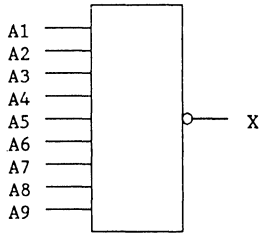
Σinput	X
Odd	H
Even	L

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
PE9	9-bit Even Parity Generator/Checker	22

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
4.23	0.13	4.57	0.07			A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2

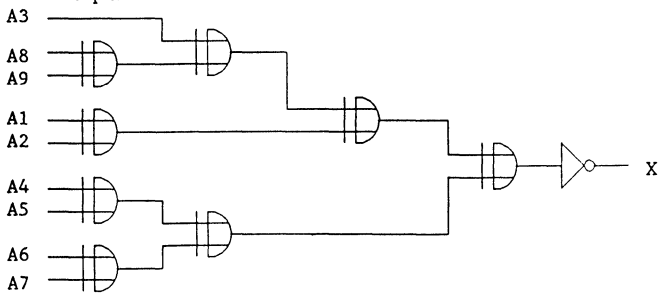
Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Σinput	X
Odd	L
Even	H

Equivalent Circuit



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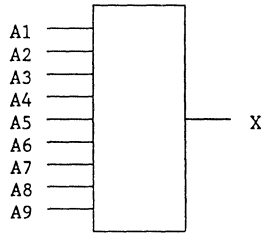
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
P09	9-bit Odd Parity Generator/Checker	22

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
4.16	0.13	4.57	0.07			A → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2

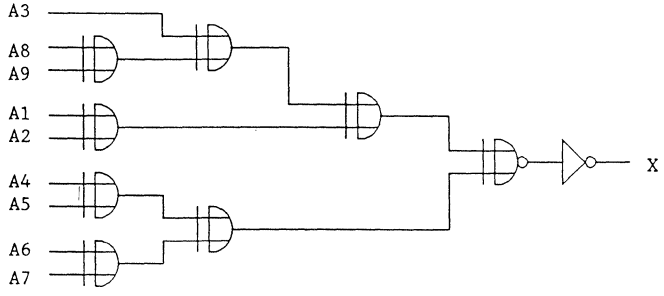
Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Σinput	X
Odd	H
Even	L

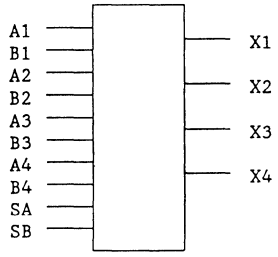
Equivalent Circuit



AU-P09-E2	Sheet 1/1	Page 17-6

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
P24	4-wide 2:1 Data Selector	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.76	0.07	0.67	0.03			A → X
0.93	0.07	0.78	0.03			B → X
0.65	0.07	0.76	0.03			SA → X
0.80	0.07	0.87	0.03			SB → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
S	4

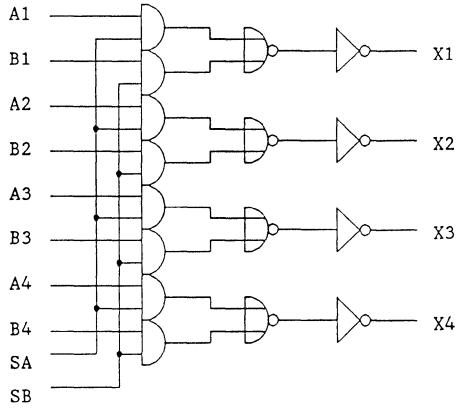
Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

SA	SB	Xn
L	L	L
H	L	An
L	H	Bn
H	H	An+Bn

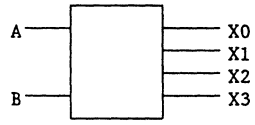
Equivalent Circuit



AU-P24-E2	Sheet 1/1	Page 17-7

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
DE2	2:4 Decoder	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.63	0.13	0.87	0.11			A → X0
0.71	0.13	0.78	0.11			A → X1
0.30	0.13	0.36	0.11			A → X2,X3
0.71	0.13	0.78	0.11			B → X0
0.23	0.13	0.45	0.11			B → X1,X3
0.63	0.13	0.87	0.11			B → X2

Parameter	Symbol	Typ(ns)*

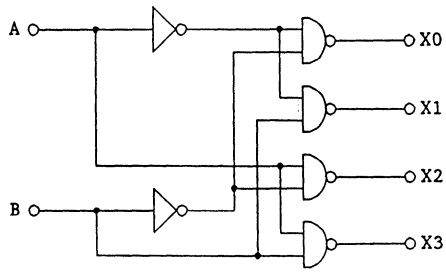
Pin Name	Input Loading Factor (ℓu)
A	3
B	3

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

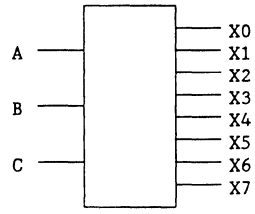
Inputs		Outputs			
A	B	X3	X2	X1	X0
L	L	H	H	H	L
L	H	H	H	L	H
H	L	H	L	H	H
H	H	L	H	H	H



AU-DE2-E2 | Sheet 1/1 | Page 17-8

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
DE3	3:8 Decoder	15

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.13	1.34	0.15			A → X0~X3
1.95	0.13	1.95	0.15			A → X4~X7
1.07	0.13	1.38	0.15			B → X0~X3
1.87	0.13	1.99	0.15			B → X4~X7
0.99	0.13	1.43	0.15			C → X0~X3
1.79	0.13	2.64	0.15			C → X4~X7

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (ℓu)
X	14

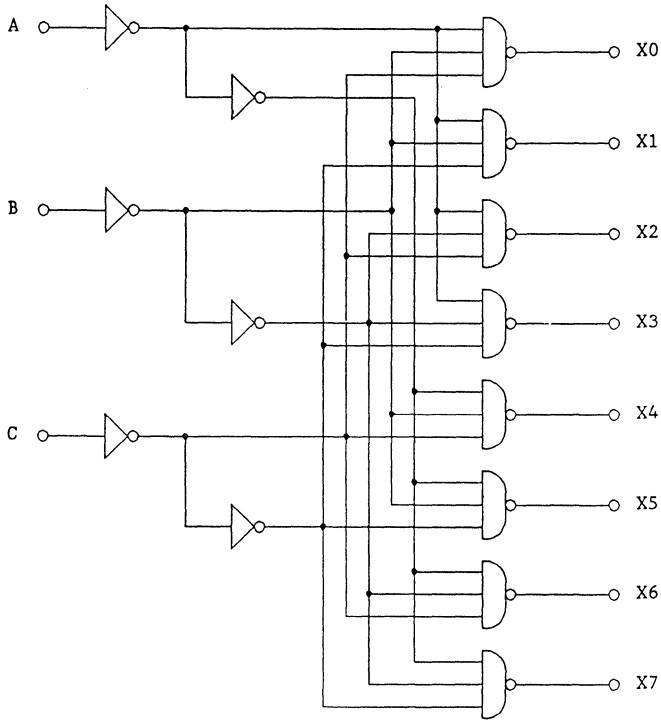
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs			Outputs							
A	B	C	X0	X1	X2	X3	X4	X5	X6	X7
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

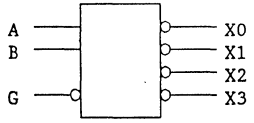
Cell Name
DE3

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
DE4	2:4 Decoder with Enable	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.95	0.13	1.17	0.15			G → X
0.69	0.13	0.89	0.15			A → X
0.86	0.13	0.91	0.15			B → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	3
B	3
G	1

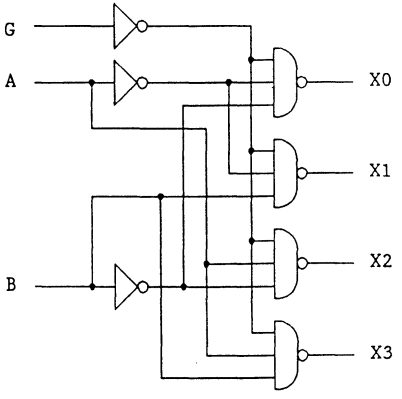
Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

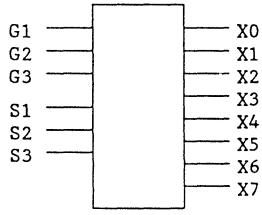
G	A	B	X3	X2	X1	X0
H	X	X	H	H	H	H
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
DE6	3:8 Decoder with Enable	30

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.44	0.13	4.76	0.07			G → X
2.31	0.13	2.63	0.07			S → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
G	1
S	1

Pin Name	Output Driving Factor (ℓu)
X	18

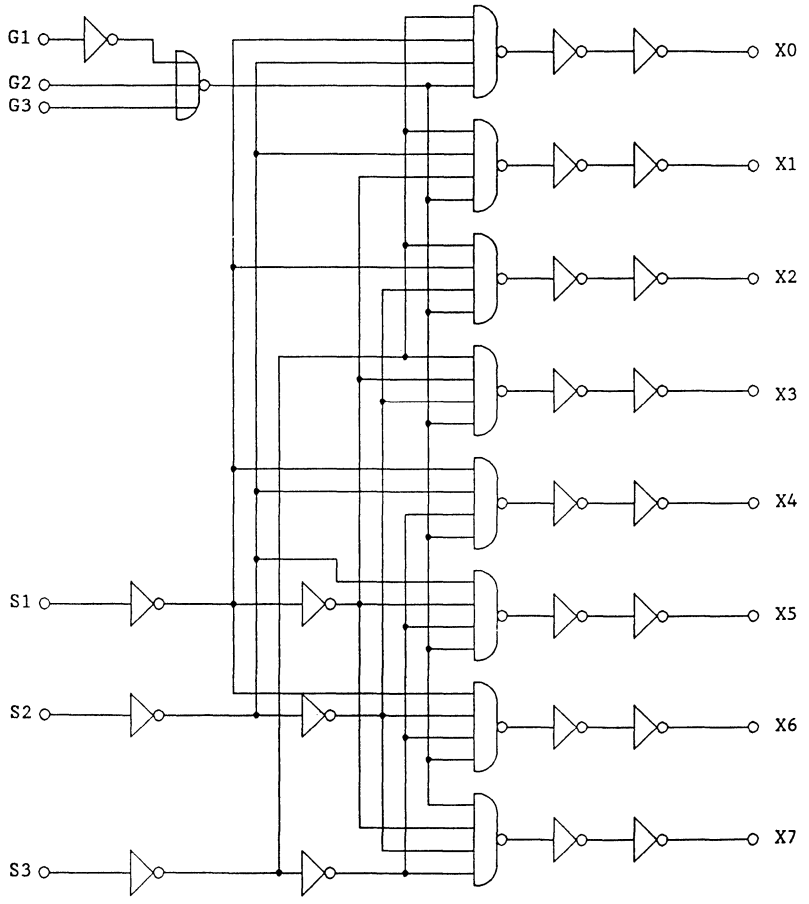
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

G1	G2+G3	S3	S2	S1	X7	X6	X5	X4	X3	X2	X1	X0
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	H	L
H	L	L	L	H	H	H	H	H	H	H	L	H
H	L	L	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	L	H	H	H	H
H	L	H	L	H	H	H	L	H	H	H	H	H
H	L	H	H	L	H	L	H	H	H	H	H	H
H	L	H	H	H	L	H	H	H	H	H	H	H

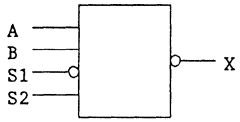
Cell Name
DE6

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T2B	2:1 Selector	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.42	0.13	0.63	0.07			A,B → X
0.49	0.13	0.79	0.07			S → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A,B	2
S	1

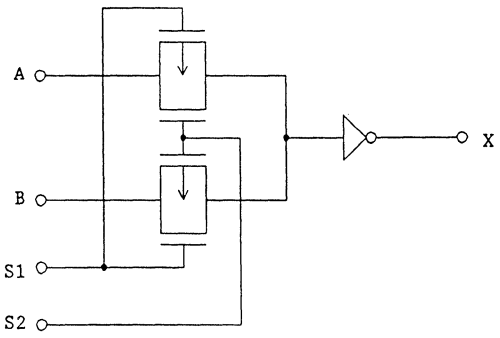
Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs				Output
A	B	S1	S2	X
L	X	L	H	H
H	X	L	H	L
X	L	H	L	H
X	H	H	L	L
H	L	L	L	Inhibit
H	L	H	H	Inhibit
L	H	L	L	Inhibit
L	H	H	H	Inhibit

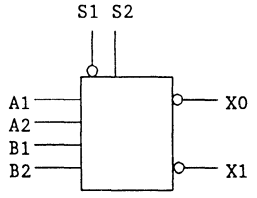
Equivalent Circuit



AU-T2B-E2	Sheet 1/1	Page 17-14

Cell Name	Function	Number of BC
T2C	Dual 2:1 Selector	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.41	0.13	0.62	0.07			A,B → X
0.54	0.13	0.83	0.07			S → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A,B	2
S	2

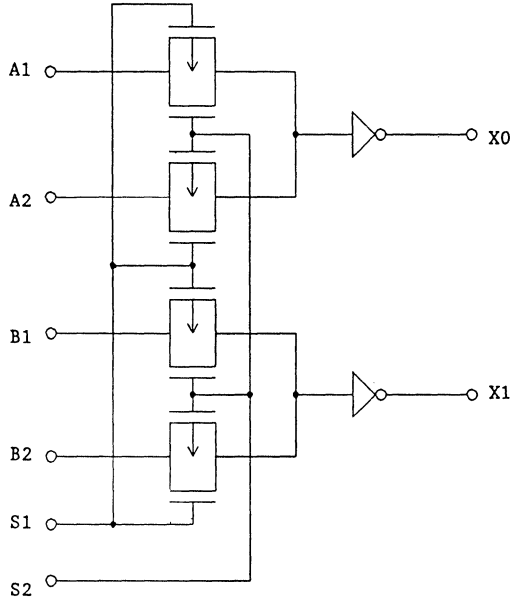
Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

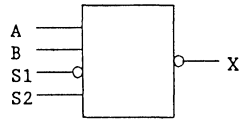
Inputs		Outputs			
A1,B1	A2,B2	S1	S2	X0	X1
L	X	L	H	H	H
H	X	L	H	L	L
X	L	H	L	H	H
X	H	H	L	L	L
L	H	L	L	Inhibit	Inhibit
H	L	L	L	Inhibit	Inhibit
L	H	H	H	Inhibit	Inhibit
H	L	H	H	Inhibit	Inhibit

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T2D	2:1 Selector	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.50	0.15	0.56	0.10			A,B → X
0.54	0.15	0.41	0.10			S → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A,B	1
S	1

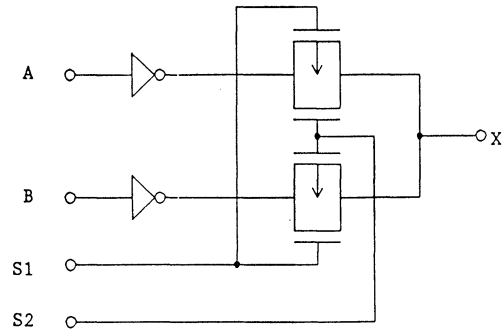
Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs				Output
A	B	S1	S2	X
L	X	L	H	H
H	X	L	H	L
X	L	H	L	H
X	H	H	L	L
L	H	L	L	Inhibit
L	H	H	H	Inhibit
H	L	L	L	Inhibit
H	L	H	H	Inhibit

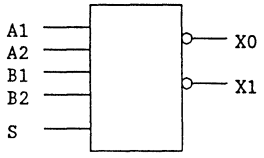
Equivalent Circuit



AU-T2D-E2	Sheet 1/1	Page 17-17

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T2E	Dual 2:1 Selector	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.43	0.13	0.43	0.08	0.11	4	A,B → X
1.31	0.13	1.30	0.08	0.11	4	S → X

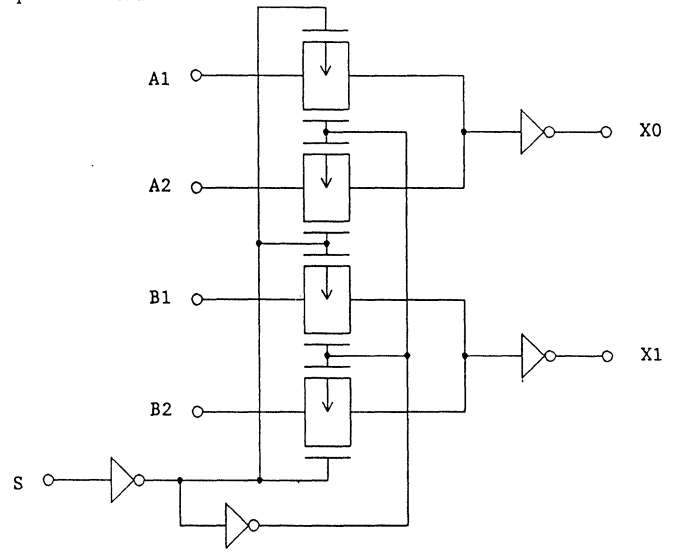
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A,B	2
S	1

Pin Name	Output Driving Factor (ℓu)
X	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

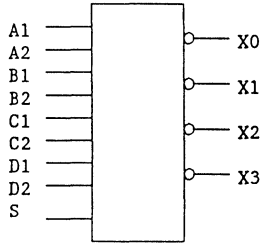
Equivalet Ciruit



AU-T2E-E2	Sheet 1/1	Page 17-18

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T2F	2:1 Selector	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.43	0.13	0.43	0.08	0.11	4	A,B, C,D → X
1.31	0.13	1.30	0.08	0.11	4	S → X

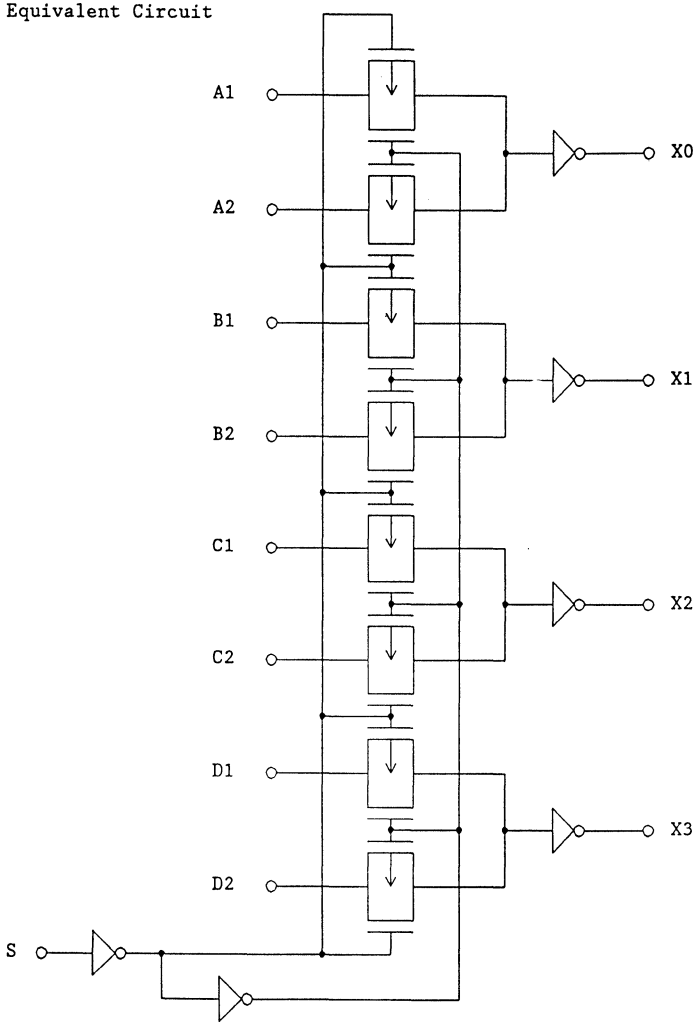
Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A,B,C,D	2
S	1

Pin Name	Output Driving Factor (ℓu)
X	18

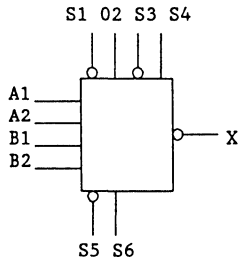
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
T5A	4:1 Selector	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.80	0.19	0.80	0.13			A,B → X
0.80	0.19	0.67	0.13			S1~4 → X
0.45	0.19	0.43	0.13			S5~6 → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A,B	1
S	1

Pin Name	Output Driving Factor (ℓu)
X	9

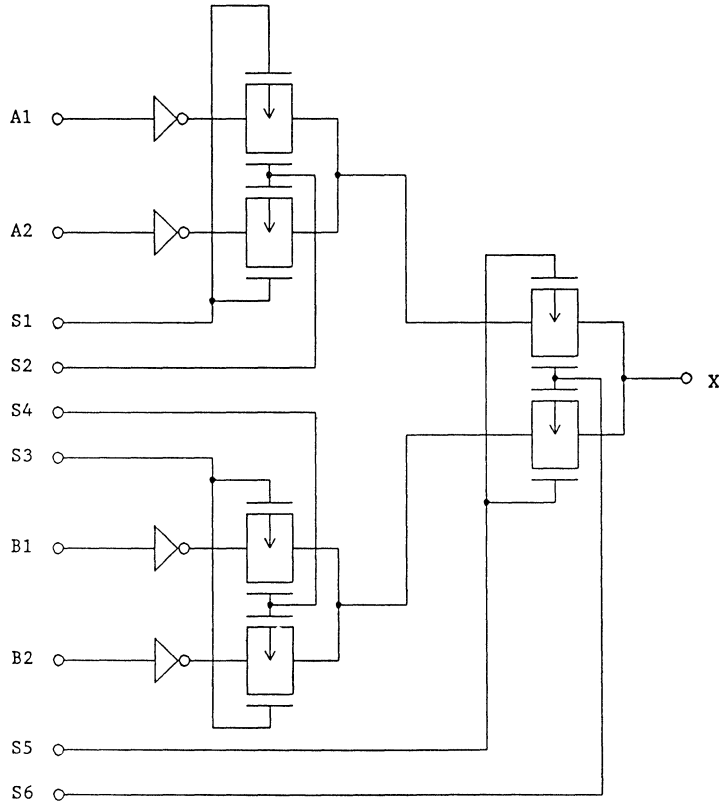
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs										Output
A1	A2	B1	B2	S1	S2	S3	S4	S5	S6	X
L				L	H			L	H	H
H				L	H			L	H	L
	L			H	L			L	H	H
	H			H	L			L	H	L
		L				L	H	H	L	H
		H				L	H	H	L	L
			L			H	L	H	L	H
			H			H	L	H	L	L

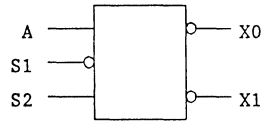
A1≠A2 → S1=S2 or S5=S6 Inhibit
B1≠B2 → S3=S4 or S5=S6 Inhibit
A1,A2≠B1,B2 or S5=S6 Inhibit

Equivalnt Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
V3A	1:2 Selector	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.50	0.15	0.56	0.10			A → X
0.44	0.15	0.36	0.10			S → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
S	1

Pin Name	Output Loading Factor (ℓu)
X	1

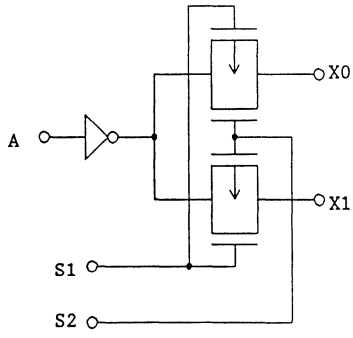
Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

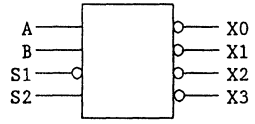
Inputs			Outputs	
A	S1	S2	X0	X1
L	L	L	Inhibit	
L	H	L	X	H
L	L	H	H	X
L	H	H	Inhibit	
H	L	L		
H	H	L	X	L
H	L	H	L	X
H	H	H	Inhibit	

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
V3B	Dual 1:2 Selector	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.51	0.15	0.61	0.10			A,B → X
0.46	0.15	0.39	0.10			S → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	1
B	1
S	2

Pin Name	Output Loading Factor (ℓu)
X	1

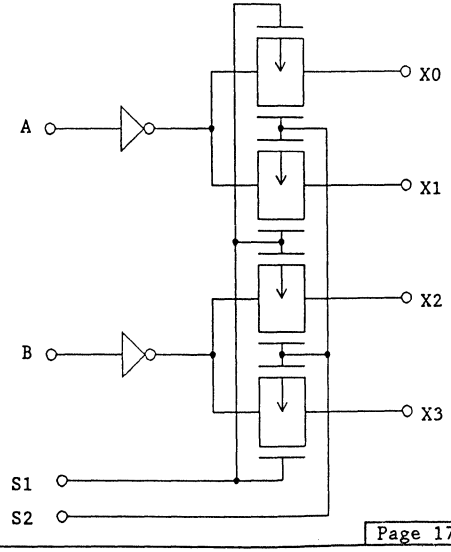
Pin Name	Output Driving Factor (ℓu)
X	14

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

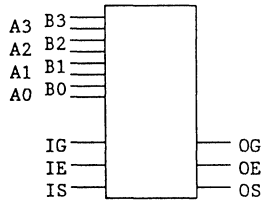
Inputs			Outputs	
A,B	S1	S2	X0, X2	X1, X3
L	L	L	Inhibit	
L	H	L	X	H
L	L	H	H	X
L	H	H	Inhibit	
H	L	L		
H	H	L	X	L
H	L	H	L	X
H	H	H	Inhibit	

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
MC4	4-bit Magnitude Comparator	42

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
4.23	0.23	5.06	0.07	0.09	4	A → OS
4.31	0.23	4.97	0.07	0.09	4	B → OS
1.89	0.23	2.23	0.07	0.09	4	IE → OS
1.55	0.23	1.93	0.07	0.09	4	IG → OS
4.15	0.23	5.23	0.07	0.09	4	A → OG
4.22	0.23	5.14	0.07	0.09	4	B → OG
1.80	0.23	2.39	0.07	0.09	4	IE → OG
1.71	0.23	1.85	0.07	0.09	4	IS → OG
4.55	0.13	3.49	0.07	0.10	4	A → OE
4.47	0.13	3.56	0.07	0.10	4	B → OE
1.71	0.13	1.15	0.07	0.10	4	IE → OE

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	3
B	3
IE	1
IG	1
IS	1

Pin Name	Output Driving Factor (ℓu)
OE	18
OG	10
OS	10

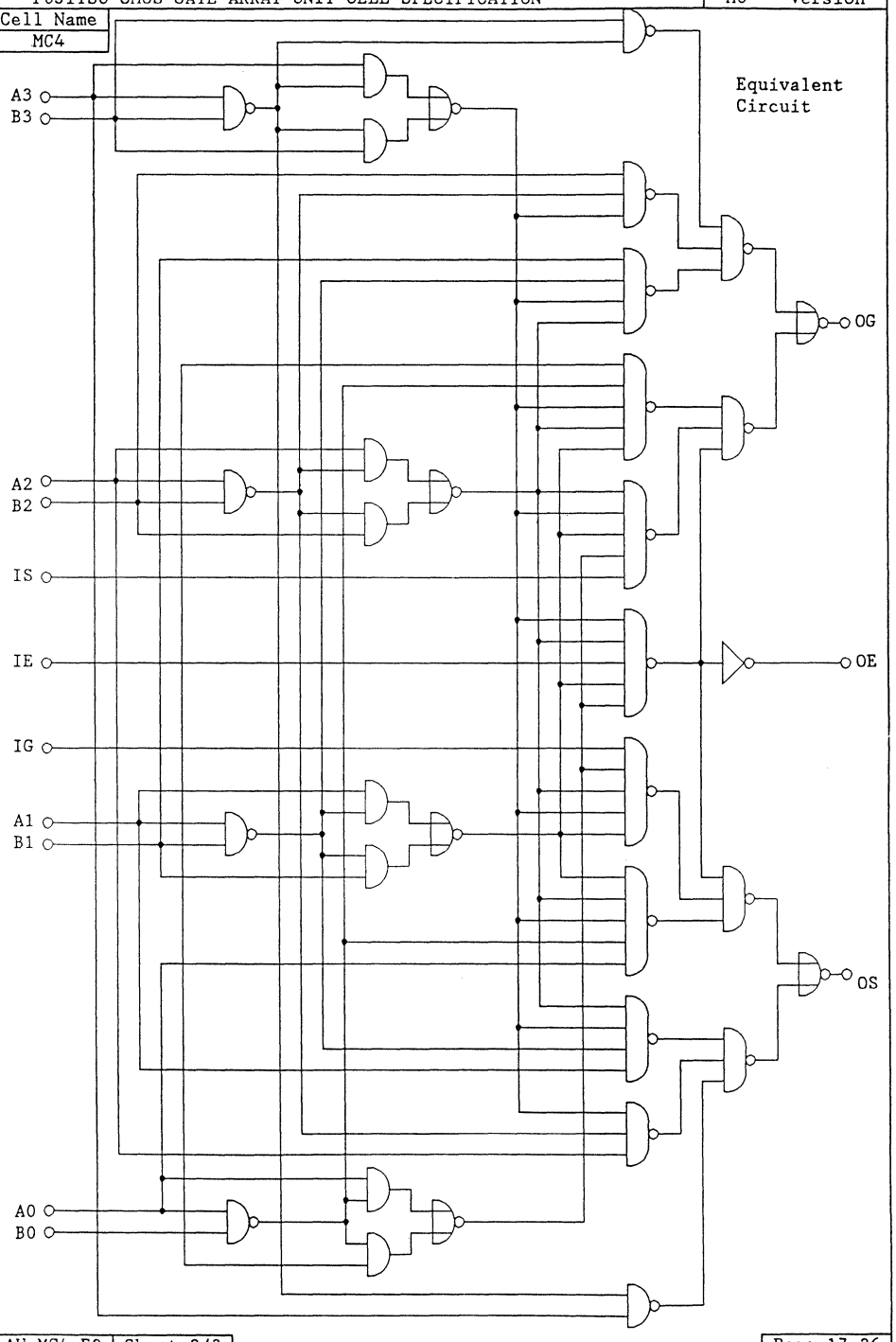
* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3,B3	A2,B2	A1,B1	A0,B0	IG (A>B)	IS (A<B)	IE (A=B)	OG (A>B)	OS (A<B)	OE (A=B)
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

Cell Name
MC4

Equivalent Circuit



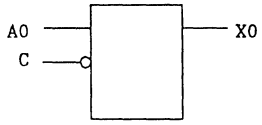
Bus Driver Family

Page	Unit Cell Name	Function	Basic Cells
2–315	B11	1-bit Bus Driver	5
2–316	B21	2-bit Bus Driver	9
2–317	B41	4-bit Bus Driver	17
2–318	B81	8-bit Bus Driver	33
2–319	B12	1-bit Block Bus Driver	7
2–320	B22	2-bit Block Bus Driver	13
2–321	B42	4-bit Block Bus Driver	25

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
B11	1-bit Bus Driver	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.06	1.15	0.04			A → X
1.30	0.06	1.30	0.04			C → X

Parameter	Symbol	Typ(ns)*

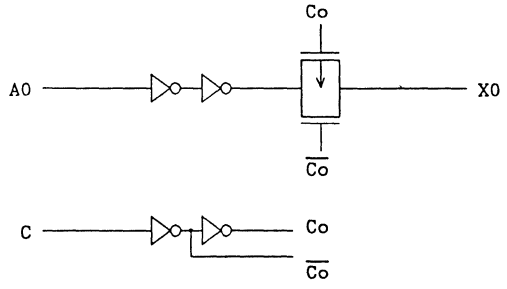
Pin Name	Input Loading Factor (ℓu)
A	1
C	1

Pin Name	Output Loading Factor (ℓu)
X	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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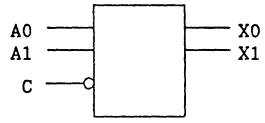
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
B21	2-bit Bus Driver	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.06	1.15	0.04			A → X
2.15	0.06	1.90	0.04			C → X

Parameter	Symbol	Typ(ns)*

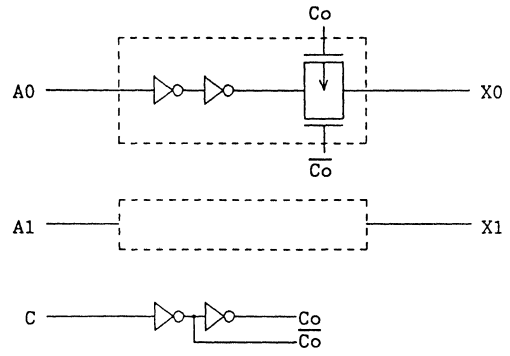
Pin Name	Input Loading Factor (ℓu)
A	1
C	1

Pin Name	Output Loading Factor (ℓu)
X	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

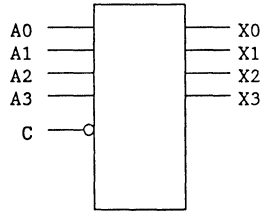
Equivalent Circuit



AU-B21-E1	Sheet 1/1	Page 18-2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
B41	4-bit Bus Driver	17

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.06	1.15	0.04			A → X
3.50	0.06	2.90	0.04			C → X

Parameter	Symbol	Typ(ns)*

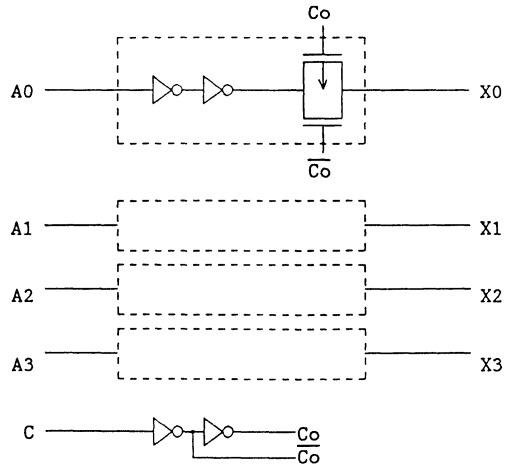
Pin Name	Input Loading Factor (ℓu)
A	1
C	1

Pin Name	Output Loading Factor (ℓu)
X	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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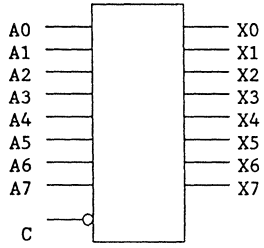
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
B81	8-bit Bus Driver	33

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.06	1.15	0.04			A → X
6.70	0.06	5.50	0.04			C → X

Parameter	Symbol	Typ(ns)*

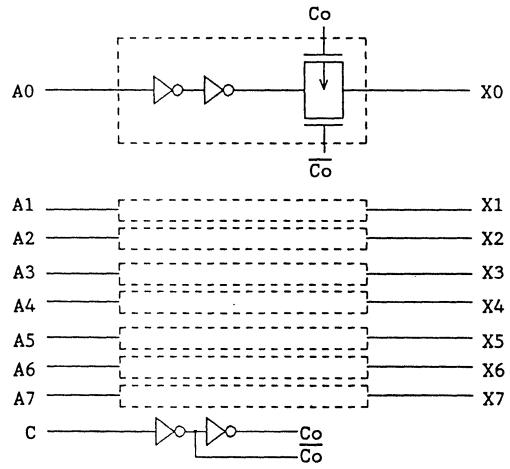
Pin Name	Input Loading Factor (ℓu)
A	1
C	1

Pin Name	Output Loading Factor (ℓu)
X	1

Pin Name	Output Driving Factor (ℓu)
X	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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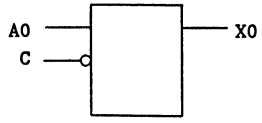
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
B12	1-bit Block Bus Driver	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.04	1.95	0.02			A → X
1.45	0.04	2.45	0.02			C → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2
C	1

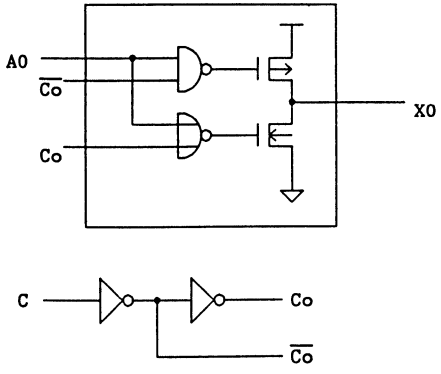
Pin Name	Output Loading Factor (ℓu)
X	2

Pin Name	Output Driving Factor (ℓu)
X	72

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit

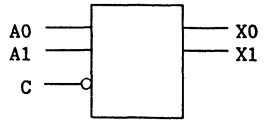
Note : This cell is for inter-block bus under chip level.



AU-B12-E1	Sheet 1/1	Page 18-5

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
B22	2-bit Block Bus Driver	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.04	1.95	0.02			A → X
1.60	0.04	2.80	0.02			C → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
A	2
C	1

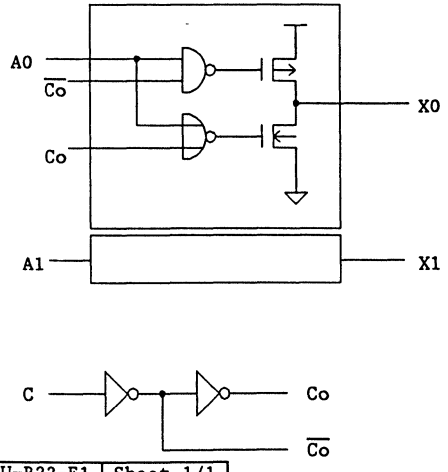
Pin Name	Output Loading Factor (ℓu)
X	2

Pin Name	Output Driving Factor (ℓu)
X	72

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit

Note : This cell is for inter-block bus under chip level.



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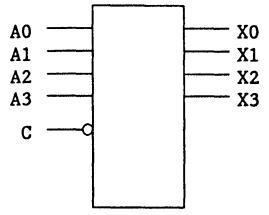
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
B42	4-bit Block Bus Driver	25

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.15	0.04	1.95	0.02			A → X
2.00	0.04	3.10	0.02			C → X

Parameter	Symbol	Typ(ns)*

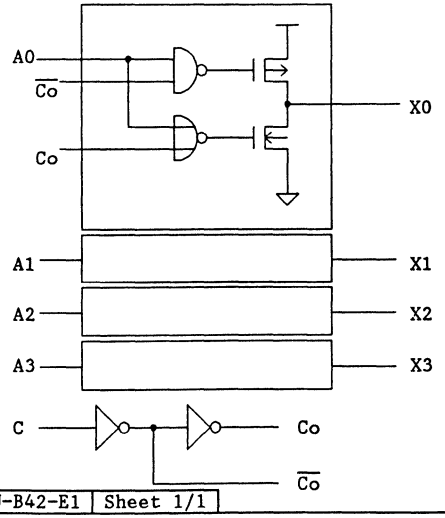
Pin Name	Input Loading Factor (ℓu)
A	2
C	1

Pin Name	Output Loading Factor (ℓu)
X	2

Pin Name	Output Driving Factor (ℓu)
X	72

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



Note : This cell is for inter-block bus under chip level.

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Clip Cell Family

Page	Unit Cell Name		Function	Basic Cells
2–325	Z00	0 Clip		0
2–326	Z01	1 Clip		0

2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
Z00	0 Clip	0

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
X	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
Z01	1 Clip	0

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
X	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

I/O Buffer Family

Page	Unit Cell Name	Function	Basic Cells
2–331	I1B	Input Buffer (Inverter)	5
2–332	I1BU	I1B with Pull-up Resistance	5
2–333	I1BD	I1B with Pull-down Resistance	5
2–334	I2B	Input Buffer (True)	4
2–335	I2BU	I2B with Pull-up Resistance	4
2–336	I2BD	I2B with Pull-down Resistance	4
2–337	IKB	Clock Input Buffer (Inverter)	4
2–338	IKBU	IKB with Pull-up Resistance	4
2–339	IKBD	IKB with Pull-down Resistance	4
2–340	ILB	Clock Input Buffer (True)	8
2–341	ILBU	ILB with Pull-up Resistance	8
2–342	ILBD	ILB with Pull-down Resistance	8
2–343	I1C	CMOS Interface Input Buffer (Inverter)	5
2–344	I1CU	I1C with Pull-up Resistance	5
2–345	I1CD	I1C with Pull-down Resistance	5
2–346	I2C	CMOS Interface Input Buffer (True)	4
2–347	I2CU	I2C with Pull-up Resistance	4
2–348	I2CD	I2C with Pull-down Resistance	4
2–349	I1S	Schmitt Trigger Input Buffer (CMOS Type, Inverter)	8
2–350	I1SU	I1S with Pull-up Resistance	8
2–351	I1SD	I1S with Pull-down Resistance	8
2–352	I2S	Schmitt Trigger Input Buffer (CMOS Type, True)	8
2–353	I2SU	I2S with Pull-up Resistance	8
2–354	I2SD	I2S with Pull-down Resistance	8
2–355	I1R	Schmitt Trigger Input Buffer	8
2–356	I1RU	I1R with Pull-up Resistance	8
2–357	I1RD	I1R with Pull-down Resistance	8
2–358	I2R	Schmitt Trigger Input Buffer (TTL Type, True)	8
2–359	I2RU	I2R with Pull-up Resistance	8
2–360	I2RD	I2R with Pull-down Resistance	8
2–361	O1B[1]	Output Buffer (Inverter)	3
2–362	O1L[2]	Power Output Buffer (Inverter)	3
2–363	O1R[1]	Output Buffer (Inverter) with Noise Limit Resistance	5
2–364	O1S[2]	Power Output Buffer (Inverter) with Noise Limit Resistance	5
2–365	O2B[1]	Output Buffer (True)	3
2–366	O2L[2]	Power Output Buffer (True)	3
2–367	O2R[1]	Output Buffer (True) with Noise Limit Resistance	4
2–368	O2S[2]	Power Output Buffer (True) with Noise Limit Resistance	4
2–369	O4R[1]	3-state Output Buffer (True) with Noise Limit Resistance	5
2–370	O4S[2]	Power 3-state Output Buffer (True) with Noise Limit Resistance	5
2–371	O4T[1]	3-state Output Buffer (True)	6
2–372	O4W[2]	Power 3-state Output Buffer (True)	6
2–373	H6T[1]	3-state Output and Input Buffer (True)	8
2–374	H6TU[1]	H6T with Pull-up Resistance	8
2–375	H6TD[1]	H6T with Pull-down Resistance	8

1. I_{OL} = 3.2 mA
2. I_{OL} = 12 mA

I/O Buffer Family (Continued)

Page	Unit Cell Name	Function	Basic Cells
2–376	H6W[2]	Power 3-state Output and Input Buffer (True)	8
2–377	H6WU[2]	H6W with Pull-up Resistance	8
2–378	H6WD[2]	H6W with Pull-down Resistance	8
2–379	H6C[1]	3-state Output and CMOS Interface Input Buffer (True)	8
2–380	H6CU[1]	H6C with Pull-up Resistance	8
2–381	H6CD[1]	H6C with Pull-down Resistance	8
2–382	H6E[2]	Power 3-state Output and CMOS Interface Input Buffer (True)	8
2–383	H6EU[2]	H6E with Pull-up Resistance	8
2–384	H6ED[2]	H6E with Pull-down Resistance	8
2–385	H6S[1]	3-state Output and Schmitt Trigger Input Buffer (CMOS Type, True)	12
2–386	H6SU[1]	H6S with Pull-up Resistance	12
2–387	H6SD[1]	H6S with Pull-down Resistance	12
2–388	H6R[1]	3-state Output and Schmitt Trigger Input Buffer (TTL Type, True)	12
2–389	H6RU[1]	H6R with Pull-up Resistance	12
2–390	H6RD[1]	H6R with Pull-down Resistance	12
2–391	H8T[1]	3-state Output with Noise Limit Resistance and Input Buffer (True)	9
2–392	H8TU[1]	H8T with Pull-up Resistance	9
2–393	H8TD[1]	H8T with Pull-down Resistance	9
2–394	H8W[2]	Power 3-state Output with Noise Limit Resistance and Input Buffer (True)	9
2–395	H8WU[2]	H8W with Pull-up Resistance	9
2–396	H8WD[2]	H8W with Pull-down Resistance	9
2–397	H8C[1]	3-state Output Buffer with Noise Limit Resistance and CMOS Interface Input Buffer (True)	9
2–398	H8CU[1]	H8C with Pull-up Resistance	9
2–399	H8CD[1]	H8C with Pull-down Resistance	9
2–400	H8E[2]	Power 3-state Output Buffer with Noise Limit Resistance and CMOS Interface Input Buffer (True)	9
2–401	H8EU[2]	H8E with Pull-up Resistance	9
2–402	H8ED[2]	H8E with Pull-down Resistance	9
2–403	H8S[1]	3-state Output and Schmitt Trigger Input Buffer (CMOS Type, True) with Noise Limit Resistance	13
2–404	H8SU[1]	H8S with Pull-up Resistance	13
2–405	H8SD[1]	H8S with Pull-down Resistance	13
2–406	H8R[1]	3-state Output and Schmitt Trigger Input Buffer (TTL Type, True) with Noise Limit Resistance	13
2–407	H8RU[1]	H8R with Pull-up Resistance	13
2–408	H8RD[1]	H8R with Pull-down Resistance	13
2–409	IKC	CMOS Interface Clock Input Buffer (Inverter)	4
2–410	IKCU	IKC with Pull-up Resistance	4
2–411	IKCD	IKC with Pull-down Resistance	4
2–412	ILC	CMOS Interface Clock Input Buffer (True)	6

1. I_{OL} = 3.2 mA
2. I_{OL} = 12 mA
3. I_{OL} = 8 mA

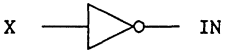
I/O Buffer Family (Continued)

Page	Unit Cell Name	Function	Basic Cells
2–413	ILCU	ILC with Pull-up Resistance	6
2–414	ILCD	ILC with Pull-down Resistance	6
2–415	O2BF[3]	Output Buffer	3
2–416	O2RF[3]	Output Buffer with Noise Limit Resistance	4
2–417	O4TF[3]	3-state Output Buffer (True)	6
2–418	O4RF[3]	3-state Output Buffer (True) with Noise Limit Resistance	5
2–419	H6TF[3]	3-state Output and Input Buffer (True)	8
2–420	H6TFU[3]	H6TF with Pull-up Resistance	8
2–421	H6TFD[3]	H6TF with Pull-down Resistance	8
2–422	H6CF[3]	3-state Output and CMOS Interface Input Buffer	8
2–423	H6CFU[3]	H6CF with Pull-up Resistance	8
2–424	H6CFD[3]	H6CF with Pull-down Resistance	8
2–425	H8TF[3]	3-state Output with Noise Limit Resistance and Input Buffer True)	9
2–426	H8TFU[3]	H8TF with Pull-up Resistance	9
2–427	H8TFD[3]	H8TF with Pull-down Resistance	9
2–428	H8CF[3]	3-state Output Buffer with Noise Limit Resistance and CMOS Interface Input Buffer (True)	9
2–429	H8CFU[3]	H8CF with Pull-up Resistance	9
2–430	H8CFD[3]	H8CF with Pull-down Resistance	9
2–431	O2S2[4]	Output Buffer with Noise Limit Resistance	3
2–432	O4S2[4]	3-state Output Buffer (True) with Noise Limit Resistance	4
2–433	H8W2[4]	3-state Output and Input Buffer with Noise Limit Resistance and Input Buffer (TTL, True)	8
2–434	H8E2[4]	3-state Output and Input Buffer with Noise Limit Resistance and Input Buffer (TTL, True)	8
2–435	H8W1[4]	3-state Output and Input Buffer with Noise Limit Resistance and Input Buffer (TTL, True) with Pull-up Resistance	8
2–436	H8E1[4]	3-state Output and Input Buffer) with Noise Limit Resistance and Input Buffer (CMOS, True) with Pull-up Resistance	8
2–437	H8WO[4]	3-state Output and Input Buffer with Noise Limit Resistance and Input Buffer (TTL, True) with Pull-down Resistance	8
2–438	H8EO[4]	3-state Output and Input Buffer with Noise Limit Resistance and Input Buffer (CMOS, True) with Pull-down Resistance	8

1. I_{OL} = 3.2 mA
2. I_{OL} = 12 mA
3. I_{OL} = 8 mA
4. I_{OL} = 24 mA

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1B	Input Buffer (Inverter)	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.28	0.03	1.23	0.03			X → IN

Parameter	Symbol	Typ(ns)*

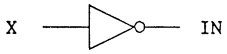
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1BU	Input Buffer (Inverter) with Pull-up Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.28	0.03	1.23	0.03			X → IN

Parameter	Symbol	Typ(ns)*

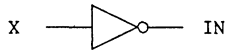
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1BD	Input Buffer (Inverter) with Pull-down Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.28	0.03	1.23	0.03			X → IN

Parameter	Symbol	Typ(ns)*

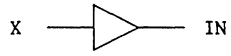
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2B	Input Buffer (True)	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85	0.03	1.47	0.03			X → IN

Parameter	Symbol	Typ(ns)*

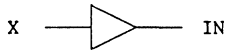
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2BU	Input Buffer (True) with Pull-up Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85	0.03	1.47	0.03			X → IN

Parameter	Symbol	Typ(ns)*

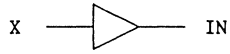
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2BD	Input Buffer (True) with Pull-down Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85	0.03	1.47	0.03			X → IN

Parameter	Symbol	Typ(ns)*

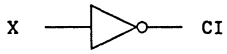
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
IKB	Clock Input Buffer (Inverter)	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.05	0.01	1.88	0.01			X → CI

Parameter	Symbol	Typ(ns)*

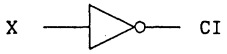
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
IKBU	Clock Input Buffer (Inverter) with Pull-up Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.05	0.01	1.88	0.01			X → CI

Parameter	Symbol	Typ(ns)*

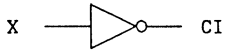
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
IKBD	Clock Input Buffer (Inverter) with Pull-down Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.05	0.01	1.88	0.01			X → CI

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-IKBD-E1	Sheet 1/1	Page 20-9

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
ILB	Clock Input Buffer (True)	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.09	0.01	1.49	0.01			X → CI

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

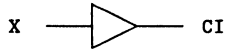
Pin Name	Output Driving Factor (ℓu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-ILB-E2	Sheet 1/1	Page 20-10

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
ILBU	Clock Input Buffer (True) with Pull-up Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.09	0.01	1.49	0.01			X → CI

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

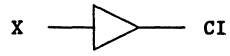
Pin Name	Output Driving Factor (ℓu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-ILBU-E2	Sheet 1/1	Page 20-11

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
ILBD	Clock Input Buffer (True) with Pull-down Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.09	0.01	1.49	0.01			X → CI

Parameter	Symbol	Typ(ns)*

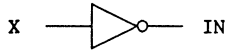
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1C	CMOS Interface Input Buffer (Inverter)	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.65	0.03	0.29	0.03			X → IN

Parameter	Symbol	Typ(ns)*

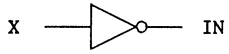
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1CU	CMOS Interface Input Buffer (Inverter) with Pull-up Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.65	0.03	0.29	0.03			X → IN

Parameter	Symbol	Typ(ns)*

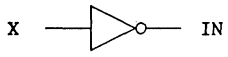
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1CD	CMOS Interface Input Buffer (Inverter) with Pull-down Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.65	0.03	0.29	0.03			X → IN

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

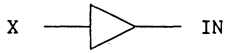
Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-I1CD-E3	Sheet 1/1	Page 20-15

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2C	CMOS Interface Input Buffer (True)	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2CU	CMOS Interface Input Buffer with Pull-up Resistance (True)	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN

Parameter	Symbol	Typ(ns)*

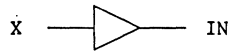
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2CD	CMOS Interface Input Buffer with Pull-down Resistance (True)	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN

Parameter	Symbol	Typ(ns)*

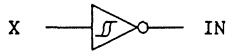
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	36

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1S	Schmitt Trigger Input Buffer (CMOS Type, Inverter)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.12	0.13	2.15	0.07			X → IN

Parameter	Symbol	Typ(ns)*

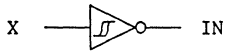
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1SU	Schmitt Trigger Input Buffer (CMOS Type, Inverter) with Pull-up Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.12	0.13	2.15	0.07			X → IN

Parameter	Symbol	Typ(ns)*

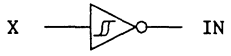
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1SD	Schmitt Trigger Input Buffer (CMOS Type, Inverter) with Pull-down Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.12	0.13	2.15	0.07			X → IN

Parameter	Symbol	Typ(ns)*

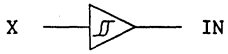
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2S	Schmitt Trigger Input Buffer (CMOS Type, True)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99	0.13	2.47	0.08			X → IN

Parameter	Symbol	Typ(ns)*

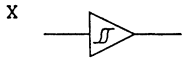
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2SU	Schmitt Trigger Input Buffer (CMOS Type, True) with Pull-up Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99	0.13	2.47	0.08			

Parameter	Symbol	Typ(ns)*

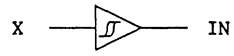
Pin Name	Input Loading Factor (Lu)

Pin Name	Output Driving Factor (Lu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2SD	Schmitt Trigger Input Buffer (CMOS Type, True) with Pull-down Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99	0.13	2.47	0.08			X → IN

Parameter	Symbol	Typ(ns)*

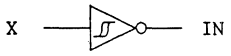
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1R	Schmitt Trigger Input Buffer (TTL Type, Inverter)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.59	0.13	1.89	0.07			X → IN

Parameter	Symbol	Typ(ns)*

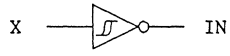
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1RU	Schmitt Trigger Input Buffer (TTL Type, Inverter) with Pull-up Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.59	0.13	1.89	0.07			X → IN

Parameter	Symbol	Typ(ns)*

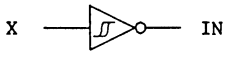
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I1RD	Schmitt Trigger Input Buffer (TTL Type, Inverter) with Pull-down Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.59	0.13	1.89	0.07			X → IN

Parameter	Symbol	Typ(ns)*

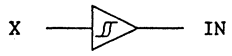
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2R	Schmitt Trigger Input Buffer (TTL Type, True)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.79	0.13	2.98	0.11			X → IN

Parameter	Symbol	Typ(ns)*

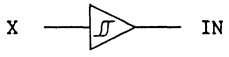
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2RU	Schmitt Trigger Input Buffer (TTL Type, True) with Pull-up Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.79	0.13	2.98	0.11			X → IN

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
I2RD	Schmitt Trigger Input Buffer (TTL Type, True) with Pull-down Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.79	0.13	2.98	0.11			X → IN

Parameter	Symbol	Typ(ns)*

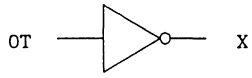
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
IN	18

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
O1B	Output Buffer (Inverter)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.60 (4.42)	0.047	1.63 (7.81)	0.103			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
OT	2

Pin Name	Output Driving Factor (ℓu)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

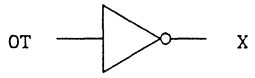
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
O1L	Power Output Buffer (Inverter)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
2.00 (3.92)	0.032	2.13 (4.17)	0.034			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
OT	2

Pin Name	Output Driving Factor (ℓu)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

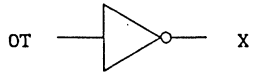
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
O1R	Output Buffer (Inverter) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.75 (6.57)	0.047	6.60 (12.78)	0.103			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
OT	1

Pin Name	Output Driving Factor (ℓu)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

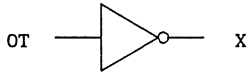
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
O1S	Power Output Buffer (Inverter) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
4.35 (6.33)	0.033	8.69 (11.45)	0.046			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
OT	1

Pin Name	Output Driving Factor (ℓu)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

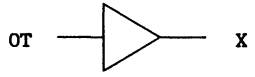
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
02B	Output Buffer (True)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.78 (3.60)	0.047	1.15 (7.33)	0.103			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
OT	6

Pin Name	Output Driving Factor (ℓu)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

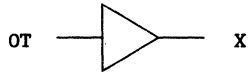
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
02L	Power Output Buffer (True)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.89 (2.81)	0.032	1.26 (3.30)	0.034			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (&u)
OT	6

Pin Name	Output Driving Factor (&u)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

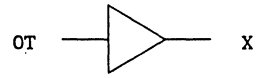
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
O2R	Output Buffer (True) with Noise Limit Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.68 (6.50)	0.047	6.07 (12.25)	0.103			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
OT	2

Pin Name	Output Driving Factor (ℓu)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

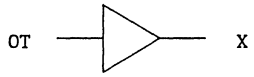
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
02S	Power Output Buffer (True) with Noise Limit Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
4.40 (6.38)	0.033	8.48 (11.24)	0.046			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
OT	2

Pin Name	Output Driving Factor (ℓu)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

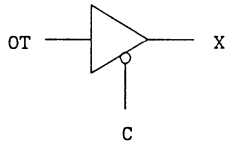
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
04R	Tri-state Output Buffer (True) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.35 (6.41)	0.047	6.26 (12.96)	0.103			OT → X

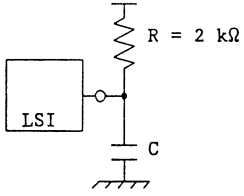
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00 (13.57)	*	6.62 (13.45)	0.105	

H → Z		Z → H		
t0	KCL	t0	KCL	
3.20 (13.57)	*	3.40 (13.45)	0.048	

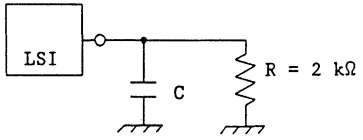
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and Zh are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

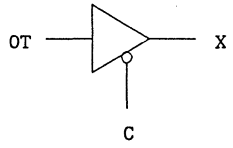
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
04S	Power Tri-state Output Buffer (True) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
4.06 (6.21)	0.033	8.64 (11.63)	0.046			OT → X

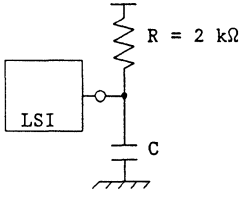
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
3.50 (16.80)	*	8.36 (11.35)	0.046	

H → Z		Z → H		
t0	KCL	t0	KCL	
4.00 (16.80)	*	4.30 (11.35)	0.033	

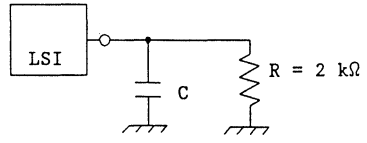
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

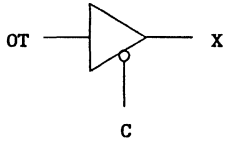
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
04T	Tri-state Output Buffer (True)	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.08 (4.14)	0.047	1.95 (8.65)	0.103			OT → X

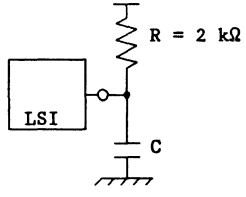
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
1.86 (13.89)	*	2.44 (9.27)	0.105	

H → Z		Z → H		
t0	KCL	t0	KCL	
3.77 (13.89)	*	1.23 (9.27)	0.048	

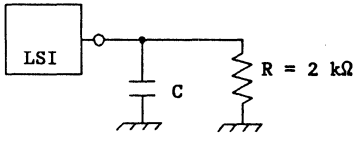
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

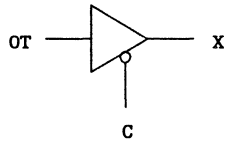
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
O4W	Power Tri-state Output Buffer (True)	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.49 (3.57)	0.032	2.34 (4.68)	0.036			OT → X

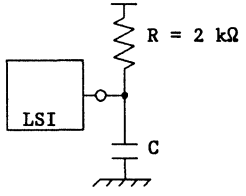
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.62 (15.80)	*	2.53 (4.87)	0.036	

H → Z		Z → H		
t0	KCL	t0	KCL	
4.47 (15.80)	*	1.44 (4.87)	0.033	

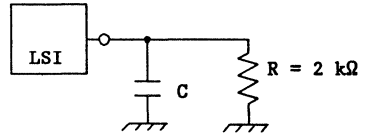
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

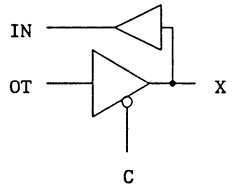
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6T	Tri-state Output & Input Buffer (True)	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 1.08 (5.08)	0.03 0.047	1.47 1.95 (10.71)	0.03 0.103			X → IN OT → X

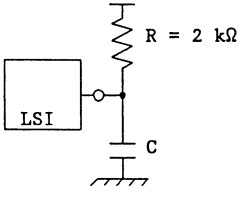
L → Z		Z → L		
t0	KCL	t0	KCL	
1.86 (17.00)	*	2.44 (11.37)	0.105	C → X

H → Z		Z → H	
t0	KCL	t0	KCL
3.77 (17.00)	*	1.23 (11.37)	0.048

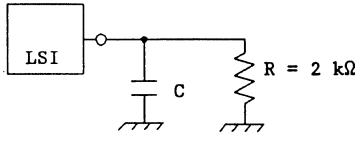
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

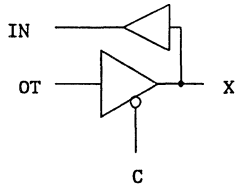
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6TU	Tri-state Output & Input Buffer (True) with Pull-up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 1.08 (5.08)	0.03 0.047	1.47 1.95 (10.71)	0.03 0.103			X → IN OT → X

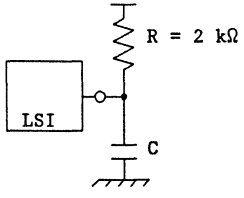
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
1.86 (17.00)	*	2.44 (11.37)	0.105	

H → Z		Z → H	
t0	KCL	t0	KCL
3.77 (17.00)	*	1.23 (11.37)	0.048

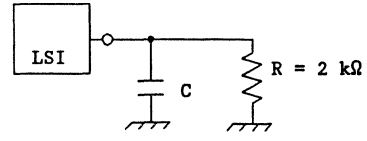
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

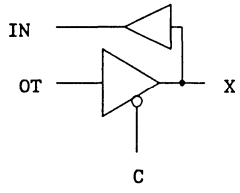
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6TD	Tri-state Output & Input Buffer (True) with Pull-down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 1.08 (5.08)	0.03 0.047	1.47 1.95 (10.71)	0.03 0.103			X → IN OT → X

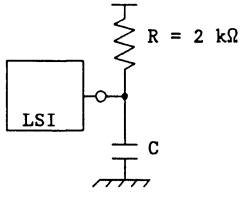
L → Z		Z → L		
t0	KCL	t0	KCL	
1.86 (17.00)	*	2.44 (11.37)	0.105	C → X

H → Z		Z → H	
t0	KCL	t0	KCL
3.77 (17.00)	*	1.23 (11.37)	0.048

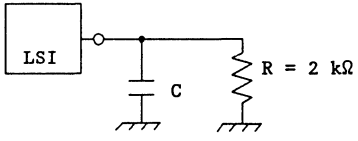
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

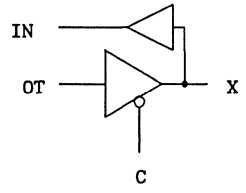
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6W	Power Tri-state Output & Input Buffer (True)	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 1.49 (4.21)	0.03 0.032	1.47 2.34 (5.40)	0.03 0.036			X → IN OT → X

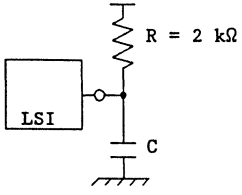
L → Z		Z → L		
t0	KCL	t0	KCL	
2.62 (19.80)	*	2.53 (5.59)	0.036	C → X

H → Z		Z → H		
t0	KCL	t0	KCL	
4.47 (19.80)	*	1.44 (5.59)	0.033	

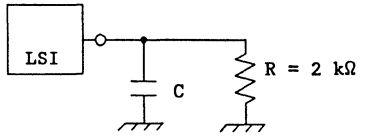
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

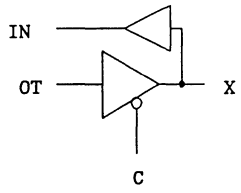
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6WU	Power Tri-state Output & Input Buffer (True) with Pull-up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 1.49 (4.21)	0.03 0.032	1.47 2.34 (5.40)	0.03 0.036			X → IN OT → X

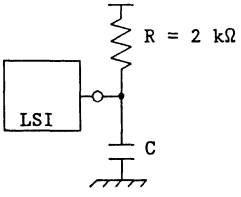
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.62 (19.80)	*	2.53 (5.59)	0.036	

H → Z		Z → H	
t0	KCL	t0	KCL
4.47 (19.80)	*	1.44 (5.59)	0.033

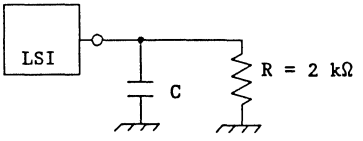
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

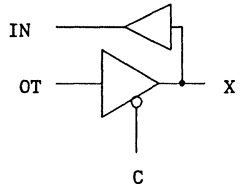
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6WD	Power Tri-state Output & Input Buffer (True) with Pull-down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 1.49 (4.21)	0.03 0.032	1.47 2.34 (5.40)	0.03 0.036			X → IN OT → X

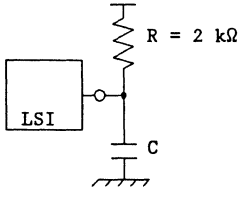
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.62 (19.80)	*	2.53 (5.59)	0.036	

H → Z		Z → H		
t0	KCL	t0	KCL	
4.47 (19.80)	*	1.44 (5.59)	0.033	

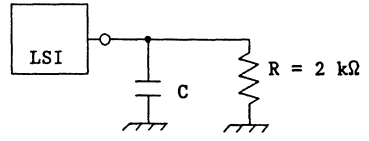
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

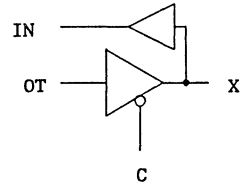
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6C	Tri-state Output & CMOS Interface Input Buffer (True)	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 1.08 (5.08)	0.03 0.047	1.07 1.95 (10.71)	0.03 0.103			X → IN OT → X

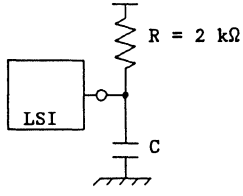
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
1.86 (17.00)	*	2.44 (11.37)	0.105	

H → Z		Z → H	
t0	KCL	t0	KCL
3.77 (17.00)	*	1.23 (11.37)	0.048

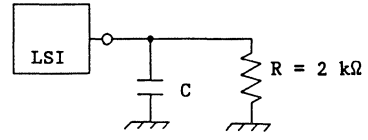
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

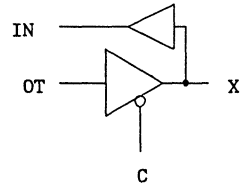
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6CU	Tri-state Output & CMOS Interface Input Buffer (True) with Pull-up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 1.08 (5.08)	0.03 0.047	1.07 1.95 (10.71)	0.03 0.103			X → IN OT → X

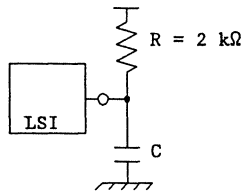
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
1.86 (17.00)	*	2.44 (11.37)	0.105	

H → Z		Z → H	
t0	KCL	t0	KCL
3.77 (17.00)	*	1.23 (11.37)	0.048

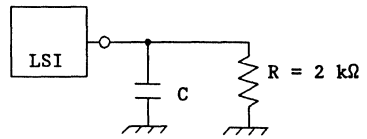
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

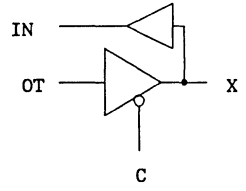
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6CD	Tri-state Output & CMOS Interface Input Buffer (True) with Pull-down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 1.08 (5.08)	0.03 0.047	1.07 1.95 (10.71)	0.03 0.103			X → IN OT → X

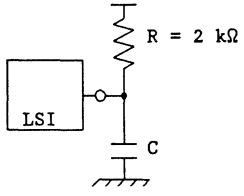
L → Z		Z → L		
t0	KCL	t0	KCL	
1.86 (17.00)	*	2.44 (11.37)	0.105	C → X

H → Z		Z → H	
t0	KCL	t0	KCL
3.77 (17.00)	*	1.23 (11.37)	0.048

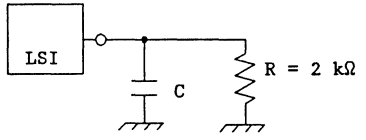
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

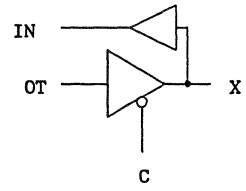
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6E	Power Tri-state Output & CMOS Interface Input Buffer (True)	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 1.49 (4.21)	0.03 0.032	1.07 2.34 (5.40)	0.03 0.036			X → IN OT → X

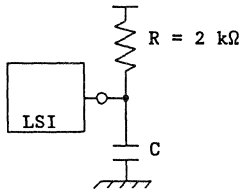
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.62 (19.80)	*	2.53 (5.59)	0.036	

H → Z		Z → H		
t0	KCL	t0	KCL	
4.47 (19.80)	*	1.44 (5.59)	0.033	

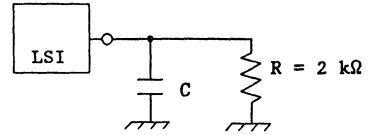
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

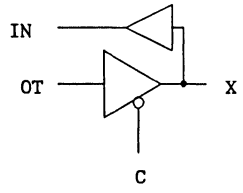
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6EU	Power Tri-state Output & CMOS Interface Input Buffer (True) with Pull-up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 1.49 (4.21)	0.03 0.032	1.07 2.34 (5.40)	0.03 0.036			X → IN OT → X

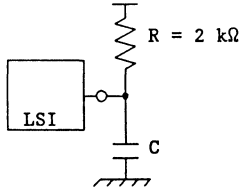
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.62 (19.80)	*	2.53 (5.59)	0.036	

H → Z		Z → H	
t0	KCL	t0	KCL
4.47 (19.80)	*	1.44 (5.59)	0.033

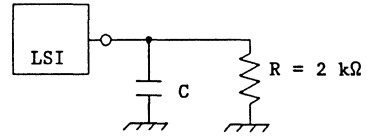
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

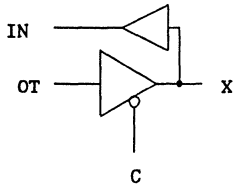
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6ED	Power Tri-state Output & CMOS Interface Input Buffer (True) with Pull-down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 1.49 (4.21)	0.03 0.032	1.07 2.34 (5.40)	0.03 0.036			X → IN OT → X

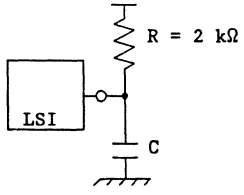
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.62 (19.80)	*	2.53 (5.59)	0.036	

H → Z		Z → H		
t0	KCL	t0	KCL	
4.47 (19.80)	*	1.44 (5.59)	0.033	

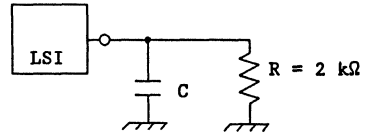
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

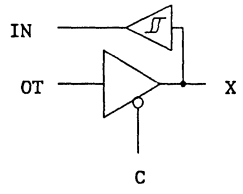
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6S	Tri-state Output & Schmitt Trigger Input Buffer (CMOS Type, True)	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99	0.13	2.47	0.08			X → IN
1.08	0.047	1.95	0.103			OT → X
(5.08)		(10.71)				

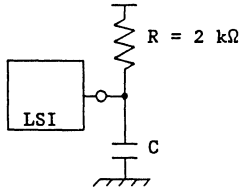
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
1.86		2.44	0.105	
(17.00)	*	(11.37)		

H → Z		Z → H		
t0	KCL	t0	KCL	
3.77		1.23	0.048	
(17.00)	*	(11.37)		

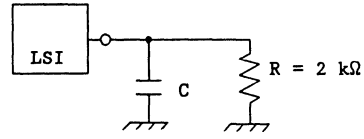
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

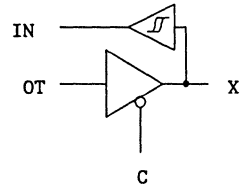
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6SU	Tri-state Output & Schmitt Trigger Input Buffer (CMOS Type, True) with Pull-up Resistance	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99 1.08 (5.08)	0.13 0.047	2.47 1.95 (10.71)	0.08 0.103			X → IN OT → X

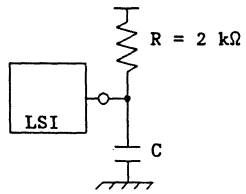
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
1.86 (17.00)	*	2.44 (11.37)	0.105	

H → Z		Z → H		
t0	KCL	t0	KCL	
3.77 (17.00)	*	1.23 (11.37)	0.048	

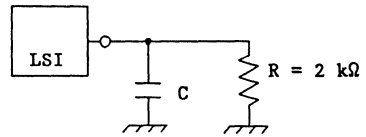
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

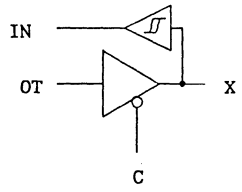
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6SD	Tri-state Output & Schmitt Trigger Input Buffer (CMOS Type, True) with Pull-down Resistance	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99	0.13	2.47	0.08			X → IN
1.08	0.047	1.95	0.103			OT → X
(5.08)		(10.71)				

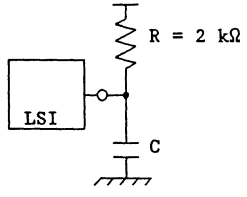
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
1.86		2.44	0.105	
(17.00)	*	(11.37)		

H → Z		Z → H		
t0	KCL	t0	KCL	
3.77		1.23	0.048	
(17.00)	*	(11.37)		

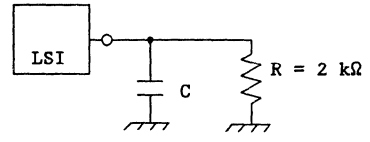
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

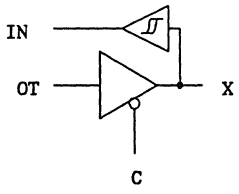
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6R	Tri-state Output & Schmitt Trigger Input Buffer (TTL Type, True)	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.79 1.08 (5.08)	0.13 0.047	2.98 1.95 (10.71)	0.11 0.103			X → IN OT → X

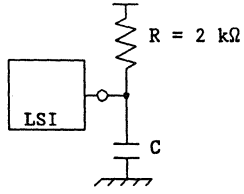
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
1.86 (17.00)	*	2.44 (11.37)	0.105	

H → Z		Z → H		
t0	KCL	t0	KCL	
3.77 (17.00)	*	1.23 (11.37)	0.048	

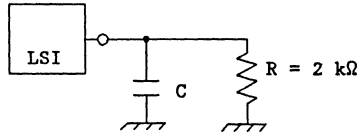
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

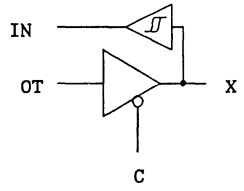
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6RU	Tri-state Output & Schmitt Trigger Input Buffer (TTL Type, True) with Pull-up Resistance	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.79 1.08 (5.08)	0.13 0.047	2.98 1.95 (10.71)	0.11 0.103			X → IN OT → X

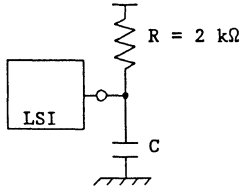
L → Z		Z → L		
t0	KCL	t0	KCL	
1.86 (17.00)	*	2.44 (11.37)	0.105	C → X

H → Z		Z → H	
t0	KCL	t0	KCL
3.77 (17.00)	*	1.23 (11.37)	0.048

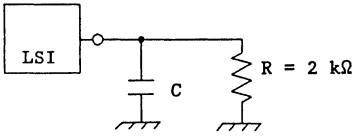
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

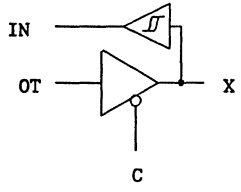
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6RD	Tri-state Output & Schmitt Trigger Input Buffer (TTL Type, True) with Pull-down Resistance	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.79	0.13	2.98	0.11			X → IN
1.08	0.047	1.95	0.103			OT → X
(5.08)		(10.71)				

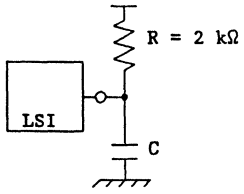
L → Z		Z → L		
t0	KCL	t0	KCL	
1.86		2.44	0.105	C → X
(17.00)	*	(11.37)		

H → Z		Z → H	
t0	KCL	t0	KCL
3.77		1.23	0.048
(17.00)	*	(11.37)	

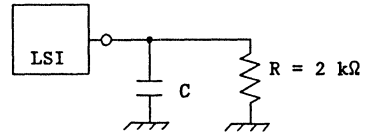
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

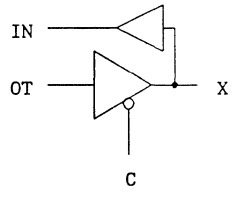
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8T	Tri-state Output with Noise Limit Resistance & Input Buffer (True)	9

Cell Symbol



Propagation Delay Parameter

tup t0	tup KCL	tdn t0	tdn KCL	KCL2	CDR2	Path
0.85	0.03	1.47	0.03			X → IN
3.35	0.047	6.26	0.103			OT → X
(7.35)		(15.02)				

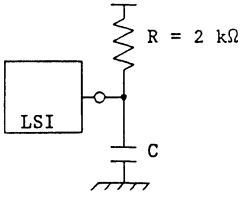
L → Z t0	L → Z KCL	Z → L t0	Z → L KCL	Path
2.00		6.62	0.105	C → X
(16.95)	*	(15.55)		

H → Z t0	H → Z KCL	Z → H t0	Z → H KCL
3.20		3.40	0.048
(16.95)	*	(15.55)	

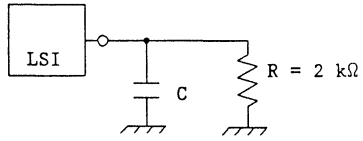
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

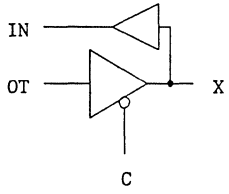
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8TU	Tri-state Output with Noise Limit Resistance & Input Buffer (True) with Pull-up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 3.35 (7.35)	0.03 0.047	1.47 6.26 (15.02)	0.03 0.103			X → IN OT → X

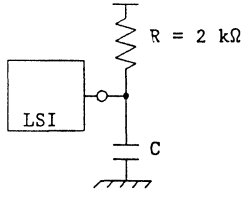
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00 (16.95)	*	6.62 (15.55)	0.105	

H → Z		Z → H	
t0	KCL	t0	KCL
3.20 (16.95)	*	3.40 (15.55)	0.048

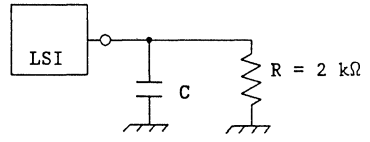
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

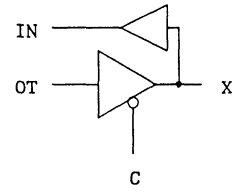
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8TD	Tri-state Output with Noise Limit Resistance & Input Buffer (True) with Pull-down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85	0.03	1.47	0.03			X → IN
3.35	0.047	6.26	0.103			OT → X
(7.35)		(15.02)				

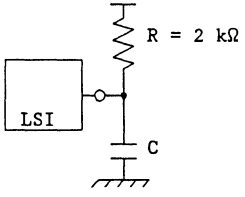
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00		6.62	0.105	
(16.95)	*	(15.55)		

H → Z		Z → H	
t0	KCL	t0	KCL
3.20		3.40	0.048
(16.95)	*	(15.55)	

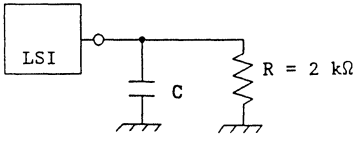
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

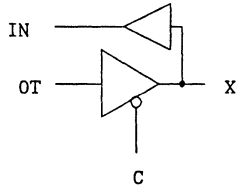
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8W	Power Tri-state Output with Noise Limit Resistance & Input Buffer (True)	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 4.06 (6.87)	0.03 0.033	1.47 8.64 (12.55)	0.03 0.046			X → IN OT → X

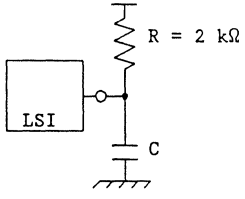
L → Z		Z → L		
t0	KCL	t0	KCL	
3.50 (21.09)	*	8.36 (12.27)	0.046	C → X

H → Z		Z → H	
t0	KCL	t0	KCL
4.00 (21.09)	*	4.30 (12.27)	0.033

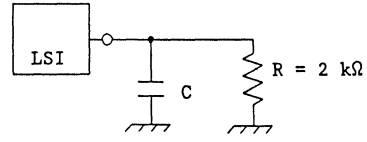
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

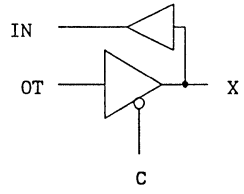
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8WU	Power Tri-state Output with Noise Limit Resistance & Input Buffer (True) with Pull-up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 4.06 (6.87)	0.03 0.033	1.47 8.64 (12.55)	0.03 0.046			X → IN OT → X

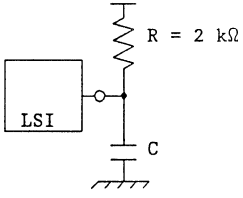
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
3.50 (21.09)	*	8.36 (12.27)	0.046	

H → Z		Z → H	
t0	KCL	t0	KCL
4.00 (21.09)	*	4.30 (12.27)	0.033

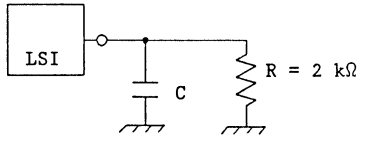
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

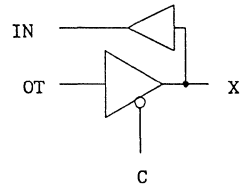
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8WD	Power Tri-state Output with Noise Limit Resistance & Input Buffer (True) with Pull-down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 4.06 (6.87)	0.03 0.033	1.47 8.64 (12.55)	0.03 0.046			X → IN OT → X

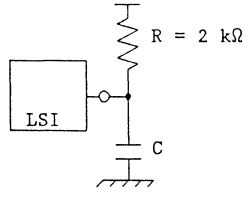
L → Z		Z → L		
t0	KCL	t0	KCL	
3.50 (21.09)	*	8.36 (12.27)	0.046	C → X

H → Z		Z → H	
t0	KCL	t0	KCL
4.00 (21.09)	*	4.30 (12.27)	0.033

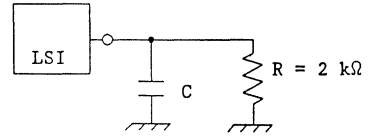
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

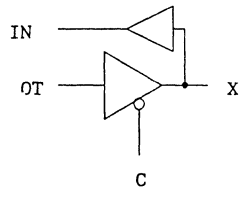
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8C	Tri-state Output Buffer with Noise Limit Resistance & CMOS Interface Input Buffer (True)	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN
3.35	0.047	6.26	0.103			OT → X
(7.35)		(15.02)				

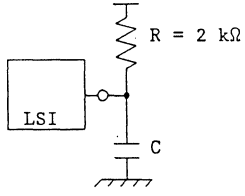
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00		6.62	0.105	
(16.95)	*	(15.55)		

H → Z		Z → H		
t0	KCL	t0	KCL	
3.20		3.40	0.048	
(16.95)	*	(15.55)		

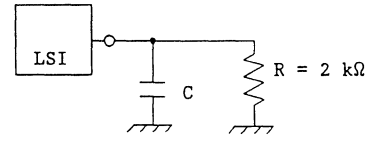
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

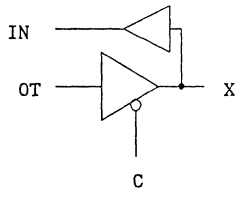
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8CU	Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 3.35 (7.35)	0.03 0.047	1.07 6.26 (15.02)	0.03 0.103			X → IN OT → X

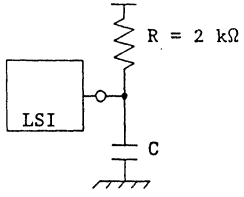
L → Z		Z → L		
t0	KCL	t0	KCL	
2.00 (16.95)	*	6.62 (15.55)	0.105	C → X

H → Z		Z → H		
t0	KCL	t0	KCL	
3.20 (16.95)	*	3.40 (15.55)	0.048	

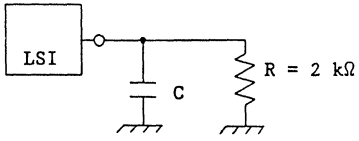
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

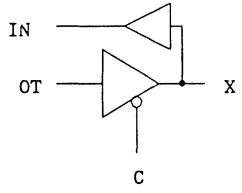
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8CD	Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN
3.35	0.047	6.26	0.103			OT → X
(7.35)		(15.02)				

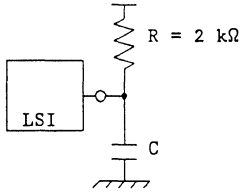
L → Z		Z → L		
t0	KCL	t0	KCL	
2.00		6.62	0.105	C → X
(16.95)	*	(15.55)		

H → Z		Z → H		
t0	KCL	t0	KCL	
3.20		3.40	0.048	
(16.95)	*	(15.55)		

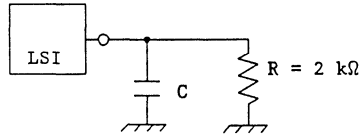
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

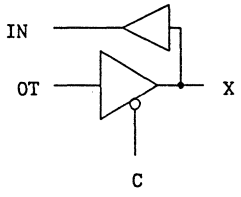
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8E	Power Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True)	9

Cell Symbol



Propagation Delay Parameter

	tup		tdn				
	t0	KCL	t0	KCL	KCL2	CDR2	Path
	0.74	0.03	1.07	0.03			X → IN
	4.06	0.033	8.64	0.046			OT → X
	(6.87)		(12.55)				

	L → Z		Z → L		
	t0	KCL	t0	KCL	
	3.50		8.36	0.046	C → X
	(21.09)	*	(12.27)		

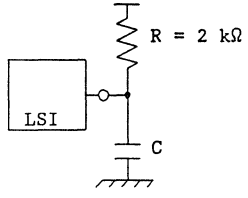
	H → Z		Z → H		
	t0	KCL	t0	KCL	
	4.00		4.30	0.033	
	(21.09)	*	(12.27)		

Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

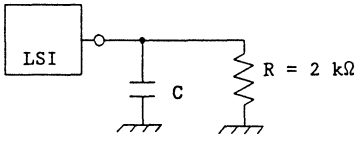
Pin Name	Output Driving Factor (ℓu)
IN	36

2

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

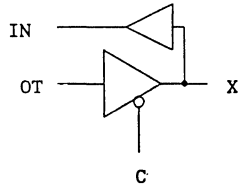
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8EU	Power Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN
4.06	0.033	8.64	0.046			OT → X
(6.87)		(12.55)				

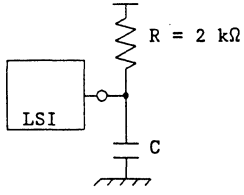
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
3.50		8.36	0.046	
(21.09)	*	(12.27)		

H → Z		Z → H		
t0	KCL	t0	KCL	
4.00		4.30	0.033	
(21.09)	*	(12.27)		

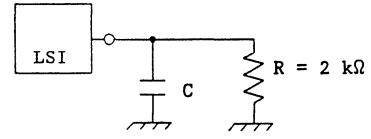
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

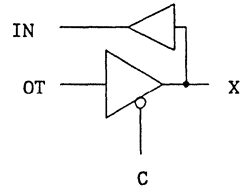
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8ED	Power Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 4.06 (6.87)	0.03 0.033	1.07 8.64 (12.55)	0.03 0.046			X → IN OT → X

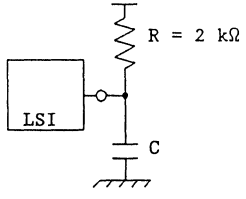
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
3.50 (21.09)	*	8.36 (12.27)	0.046	

H → Z		Z → H		
t0	KCL	t0	KCL	
4.00 (21.09)	*	4.30 (12.27)	0.033	

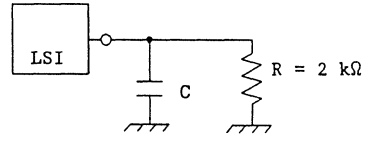
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

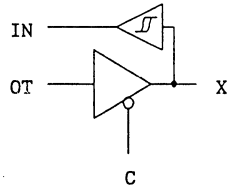
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8S	Tri-state Output & Schmitt Trigger Input Buffer (CMOS Type, True) with Noise Limit Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99 3.35 (7.35)	0.13 0.047	2.47 6.26 (15.02)	0.08 0.103			X → IN OT → X

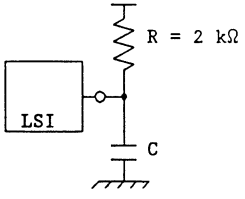
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00 (16.95)	*	6.62 (15.55)	0.105	

H → Z		Z → H	
t0	KCL	t0	KCL
3.20 (16.95)	*	3.40 (15.55)	0.048

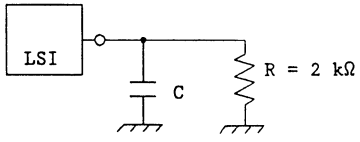
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

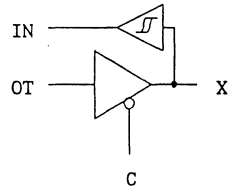
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8SU	Tri-state Output & Schmitt Trigger Input Buffer(CMOS Type ,True) w/ Noise Limit Resistance w/ Pull-up Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99 3.35 (7.35)	0.13 0.047	2.47 6.26 (15.02)	0.08 0.103			X → IN OT → X

L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00 (16.95)	*	6.62 (15.55)	0.105	

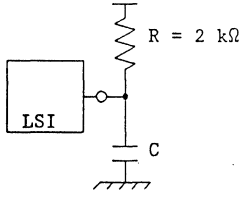
H → Z		Z → H	
t0	KCL	t0	KCL
3.20 (16.95)	*	3.40 (15.55)	0.048

Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

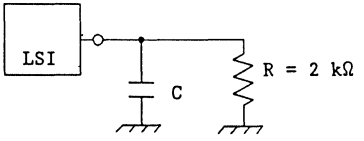
Pin Name	Output Driving Factor (ℓu)
IN	18

2

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

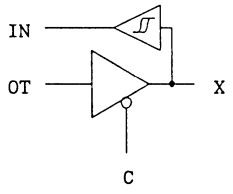
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8SD	Tri-state Output & Schmitt Trigger Input Buffer(CMOS Type ,True) w/ Noise Limit Resistance w/ Pull-down Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.99 3.35 (7.35)	0.13 0.047	2.47 6.26 (15.02)	0.08 0.103			X → IN OT → X

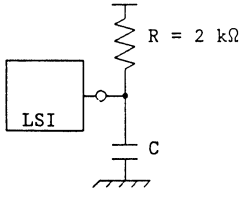
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00 (16.95)	*	6.62 (15.55)	0.105	

H → Z		Z → H		
t0	KCL	t0	KCL	
3.20 (16.95)	*	3.40 (15.55)	0.048	

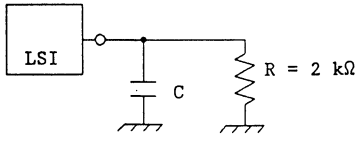
Pin Name	Input Loading Factor (&u)
OT	2
C	2

Pin Name	Output Driving Factor (&u)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

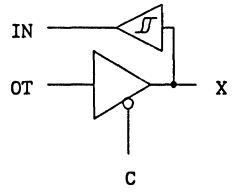
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8R	Tri-state Output & Schmitt Trigger Input Buffer (TTL Type, True) with Noise Limit Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.79 3.35 (7.35)	0.13 0.047	2.98 6.26 (15.02)	0.11 0.103			X → IN OT → X

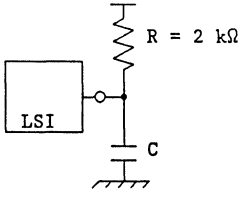
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00 (16.95)	*	6.62 (15.55)	0.105	

H → Z		Z → H	
t0	KCL	t0	KCL
3.20 (16.95)	*	3.40 (15.55)	0.048

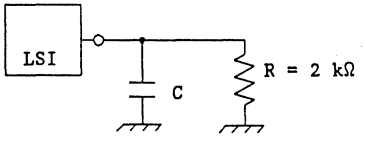
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

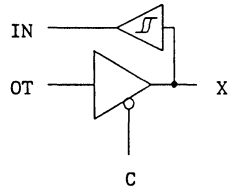
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8RU	Tri-state Output & Schmitt Trigger Input Buffer(TTL Type, True) w/ Noise Limit Resistance w/ Pull-up Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.79 3.35 (7.35)	0.13 0.047	2.98 6.26 (15.02)	0.11 0.103			X → IN OT → X

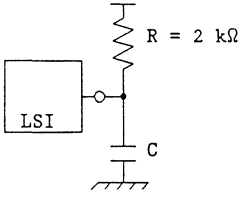
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00 (16.95)	*	6.62 (15.55)	0.105	

H → Z		Z → H	
t0	KCL	t0	KCL
3.20 (16.95)	*	3.40 (15.55)	0.048

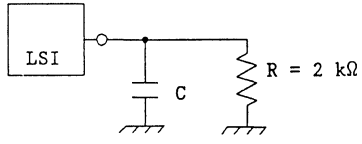
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

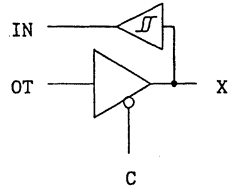
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8RD	Tri-state Output & Schmitt Trigger Input Buffer(TTL Type, True) w/ Noise Limit Resistance w/ Pull-down Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.79	0.13	2.98	0.11			X → IN
3.35	0.047	6.26	0.103			OT → X
(7.35)		(15.02)				

L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.00		6.62	0.105	
(16.95)	*	(15.55)		

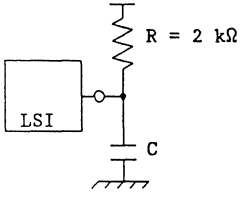
H → Z		Z → H		
t0	KCL	t0	KCL	
3.20		3.40	0.048	
(16.95)	*	(15.55)		

Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

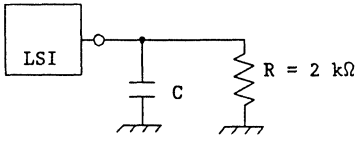
Pin Name	Output Driving Factor (ℓu)
IN	18

2

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

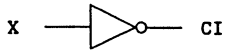
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
IKC	CMOS Interface Clock Input Buffer(Inverter)	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.70	0.01	1.62	0.01			X → CI

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (£u)

Pin Name	Output Driving Factor (£u)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
IKCU	CMOS Interface Clock Input Buffer(Inverter) with Pull-up Resistance	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.70	0.01	1.62	0.01			X → CI

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

AU-IKCU-E1	Sheet 1/1	Page 20-80

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
IKCD	CMOS Interface Clock Input Buffer(Inverter) with Pull-down Resistance	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.70	0.01	1.62	0.01			X → CI

Parameter	Symbol	Typ(ns)*

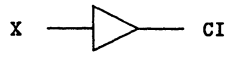
Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
ILC	CMOS Interface Clock Input Buffer(True)	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.53	0.01	2.12	0.01			X → CI

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (Lu)

Pin Name	Output Driving Factor (Lu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
ILCU	CMOS Interface Clock Input Buffer(True) with Pull-up Resistance	6

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.53	0.01	2.12	0.01			X → CI

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)

Pin Name	Output Driving Factor (ℓu)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

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FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
ILCD	CMOS Interface Clock Input Buffer(True) with Pull-down Resistance	6

Cell Symbol

Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.53	0.01	2.12	0.01			X → CI

Parameter	Symbol	Typ(ns)*

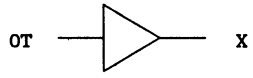
Pin Name	Input Loading Factor (&u)

Pin Name	Output Driving Factor (&u)
CI	200

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
O2BF	Output Buffer (IOL=8mA, True)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.86 (3.68)	0.047	1.09 (4.21)	0.052			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (&u)
OT	6

Pin Name	Output Driving Factor (&u)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

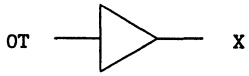
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
02RF	Output Buffer (IOL=8mA, True) with Noise Limit Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.75 (6.57)	0.047	7.21 (10.57)	0.056			OT → X

Parameter	Symbol	Typ(ns)*

Pin Name	Input Loading Factor (ℓu)
OT	2

Pin Name	Output Driving Factor (ℓu)

* Minimum values for the typical operating condition. The values for the worst case operating condition are given by the maximum delay multiplier.

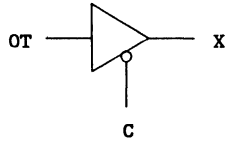
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
04TF	Tri-state Output Buffer (IOL=8mA, True)	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
1.21 (4.27)	0.047	2.09 (5.47)	0.052			OT → X

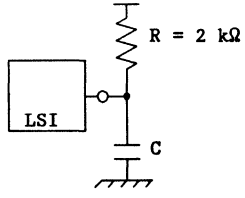
L → Z		Z → L		
t0	KCL	t0	KCL	
2.55 (15.20)	*	2.32 (5.83)	0.054	C → X

H → Z		Z → H		
t0	KCL	t0	KCL	
3.56 (15.20)	*	1.37 (5.83)	0.048	

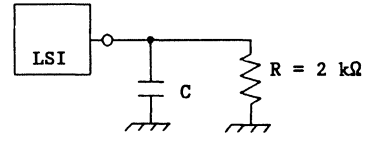
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

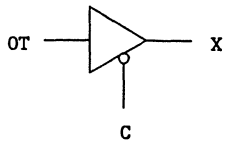
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
O4RF	Tri-state Output Buffer (IOL=8mA, True) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
3.42 (6.48)	0.047	7.64 (11.28)	0.056			OT → X

L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.69 (15.37)	*	7.72 (11.36)	0.056	

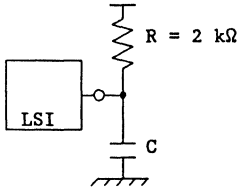
H → Z		Z → H		
t0	KCL	t0	KCL	
2.90 (15.37)	*	3.58 (11.36)	0.047	

Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

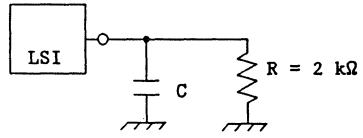
Pin Name	Output Driving Factor (ℓu)

2

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

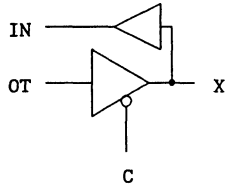
Note: 1. The unit of K_{CL} is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6TF	Tri-state Output & Input Buffer (IOL=8mA, True)	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 1.21 (5.21)	0.03 0.047	1.47 2.09 (6.51)	0.03 0.052			X → IN OT → X

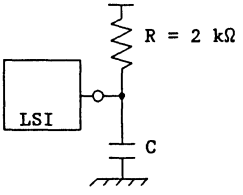
L → Z		Z → L		
t0	KCL	t0	KCL	
2.55 (19.10)	*	2.32 (6.91)	0.054	C → X

H → Z		Z → H	
t0	KCL	t0	KCL
3.56 (19.10)	*	1.37 (6.91)	0.048

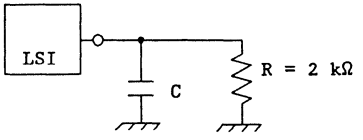
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

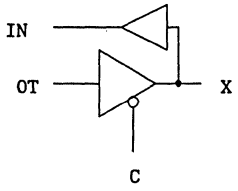
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6TFU	Tri-state Output & Input Buffer (IOL=8mA, True) with Pull-up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85	0.03	1.47	0.03			X → IN
1.21	0.047	2.09	0.052			OT → X
(5.21)		(6.51)				

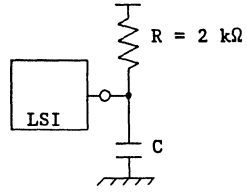
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.55 (19.10)	*	2.32 (6.91)	0.054	

H → Z		Z → H		
t0	KCL	t0	KCL	
3.56 (19.10)	*	1.37 (6.91)	0.048	

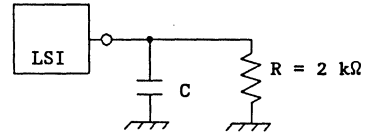
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

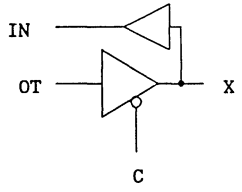
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6TFD	Tri-state Output & Input Buffer (IOL=8mA, True) with Pull-down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85	0.03	1.47	0.03			X → IN
1.21	0.047	2.09	0.052			OT → X
(5.21)		(6.51)				

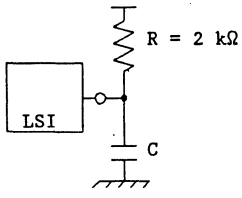
L → Z		Z → L		
t0	KCL	t0	KCL	
2.55		2.32	0.054	C → X
(19.10)	*	(6.91)		

H → Z		Z → H		
t0	KCL	t0	KCL	
3.56		1.37	0.048	
(19.10)	*	(6.91)		

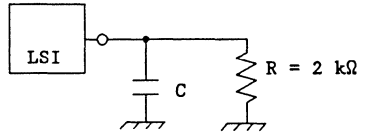
Pin Name	Input Loading Factor (ℓu)
OT	6
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

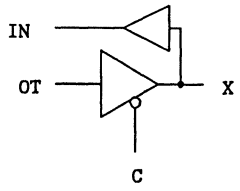
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6CF	Tri-state Output & CMOS Interface Input Buffer (IOL=8mA, True)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 2.39 (6.39)	0.03 0.047	1.07 4.30 (8.64)	0.03 0.051			X → IN OT → X

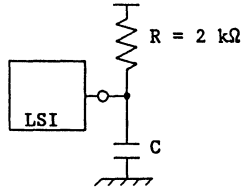
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.63 (18.72)	*	3.93 (8.27)	0.051	

H → Z		Z → H		
t0	KCL	t0	KCL	
3.40 (18.72)	*	2.50 (8.27)	0.047	

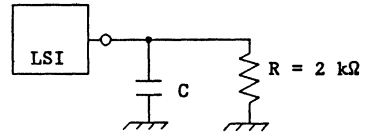
Pin Name	Input Loading Factor (ℓu)
OT	4
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

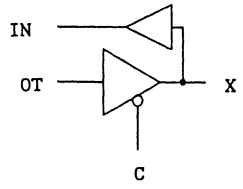
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6CFU	Tri-state Output & CMOS Interface Input Buffer with Pull-up Resistance (IOL=8mA, True)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74 2.39 (6.39)	0.03 0.047	1.07 4.30 (8.64)	0.03 0.051			X → IN OT → X

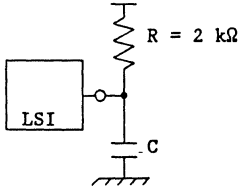
L → Z		Z → L		
t0	KCL	t0	KCL	
2.63 (18.72)	*	3.93 (8.27)	0.051	C → X

H → Z		Z → H	
t0	KCL	t0	KCL
3.40 (18.72)	*	2.50 (8.27)	0.047

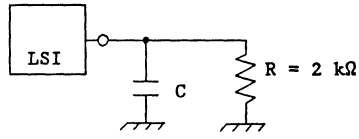
Pin Name	Input Loading Factor (ℓu)
OT	4
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

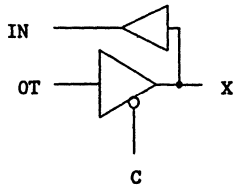
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H6CFD	Tri-state Output & CMOS Interface Input Buffer with Pull-down Resistance (IOL=8mA, True)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN
2.39	0.047	4.30	0.051			OT → X
(6.39)		(8.64)				

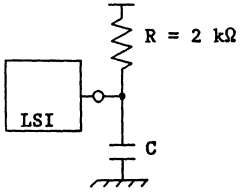
L → Z		Z → L		
t0	KCL	t0	KCL	
2.63		3.93	0.051	C → X
(18.72)	*	(8.27)		

H → Z		Z → H		
t0	KCL	t0	KCL	
3.40		2.50	0.047	
(18.72)	*	(8.27)		

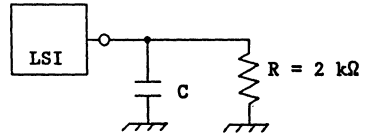
Pin Name	Input Loading Factor (ℓu)
OT	4
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

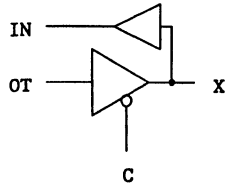
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8TF	Tri-state Output with Noise Limit Resistance & Input Buffer (IOL=8mA, True)	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85	0.03	1.47	0.03			X → IN
3.42	0.047	7.64	0.056			OT → X
(7.42)		(12.40)				

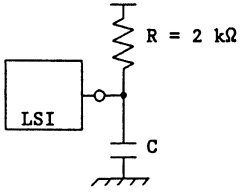
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.69		7.72	0.056	
(19.69)	*	(12.48)		

H → Z		Z → H		
t0	KCL	t0	KCL	
2.90		3.58	0.047	
(19.69)	*	(12.48)		

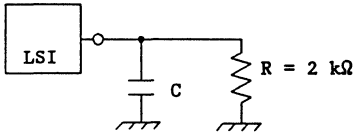
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

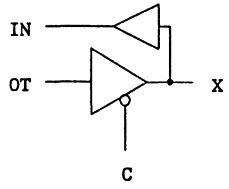
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8TFU	Tri-state Output with Noise Limit Resistance & Input Buffer(IOL=8mA, True) with Pull-up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 3.42 (7.42)	0.03 0.047	1.47 7.64 (12.40)	0.03 0.056			X → IN OT → X

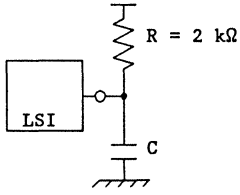
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.69 (19.69)	*	7.72 (12.48)	0.056	

H → Z		Z → H		
t0	KCL	t0	KCL	
2.90 (19.69)	*	3.58 (12.48)	0.047	

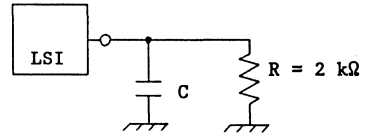
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

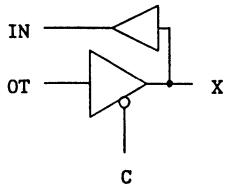
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8TFD	Tri-state Output with Noise Limit Resistance & Input Buffer(IOL=8mA, True) with Pull-down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.85 3.42 (7.42)	0.03 0.047	1.47 7.64 (12.40)	0.03 0.056			X → IN OT → X

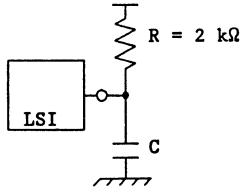
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.69 (19.69)	*	7.72 (12.48)	0.056	

H → Z		Z → H		
t0	KCL	t0	KCL	
2.90 (19.69)	*	3.58 (12.48)	0.047	

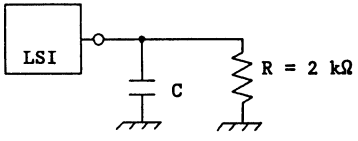
Pin Name	Input Loading Factor (&u)
OT	2
C	2

Pin Name	Output Driving Factor (&u)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

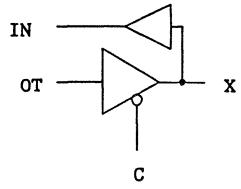
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8CF	Tri-state Output Buffer with Noise Limit Resistance & CMOS Interface Input Buffer (IOL=8mA, True)	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN
3.42	0.047	7.64	0.056			OT → X
(7.42)		(12.40)				

L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.69		7.72	0.056	
(19.69)	*	(12.48)		

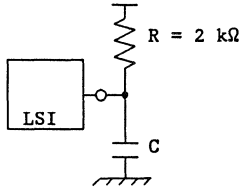
H → Z		Z → H		
t0	KCL	t0	KCL	
2.90		3.58	0.047	
(19.69)	*	(12.48)		

Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

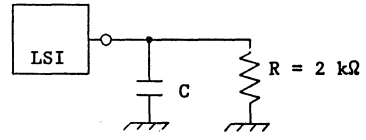
Pin Name	Output Driving Factor (ℓu)
IN	36

2

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

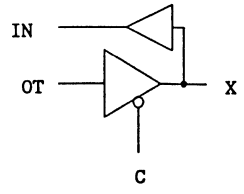
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8CFU	Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer(IOL=8mA, True) w/ Pull-up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN
3.42	0.047	7.64	0.056			OT → X
(7.42)		(12.40)				

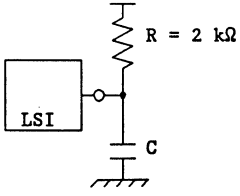
L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.69		7.72	0.056	
(19.69)	*	(12.48)		

H → Z		Z → H		
t0	KCL	t0	KCL	
2.90		3.58	0.047	
(19.69)	*	(12.48)		

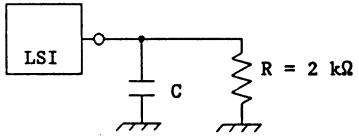
Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

Pin Name	Output Driving Factor (ℓu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

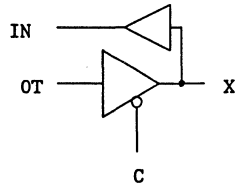
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	Function	Number of BC
H8CFD	Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer(IOL=8mA, True) w/ Pull-down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				
t0	KCL	t0	KCL	KCL2	CDR2	Path
0.74	0.03	1.07	0.03			X → IN
3.42	0.047	7.64	0.056			OT → X
(7.42)		(12.40)				

L → Z		Z → L		
t0	KCL	t0	KCL	C → X
2.69		7.72	0.056	
(19.69)	*	(12.48)		

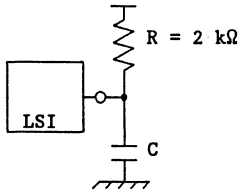
H → Z		Z → H		
t0	KCL	t0	KCL	
2.90		3.58	0.047	
(19.69)	*	(12.48)		

Pin Name	Input Loading Factor (ℓu)
OT	2
C	2

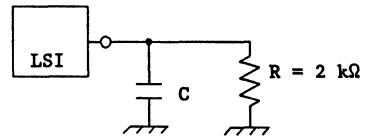
Pin Name	Output Driving Factor (ℓu)
IN	36

2

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

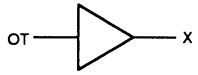
Note: 1. The unit of K_{CL} for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O2S2	Output Buffer (IOL=24mA, True) with Noise Limit Resistance	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
3.60 (5.04)	0.024	7.69 (10.15)	0.041			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	2

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

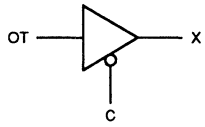
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"AU" Version
Cell Name	**Function**	**Number of BC**
O4S2	Tri-state Output Buffer (IOL=24mA, True) with Noise Limit Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
3.60 (5.16)	0.024	7.90 (10.56)	0.041			OT to X

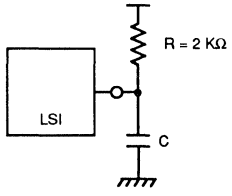
L to Z		Z to L		
t0	KCL	t0	KCL	
3.82 (18.72)	*	8.12 (10.85)	0.042	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
6.43 (18.72)	*	3.83 (10.85)	0.024	

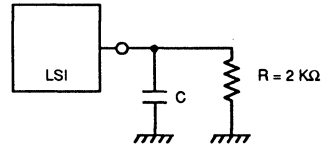
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

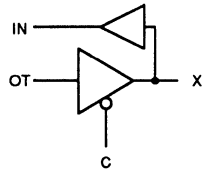
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8W2	Tri–state Output & Input Buffer (IOL=24mA) with Noise Limit Resistance and Input Buffer (TTL, True)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.85 3.60 (5.86)	0.03 0.024	1.47 7.90 (11.39)	0.03 0.041			X to IN OT to X

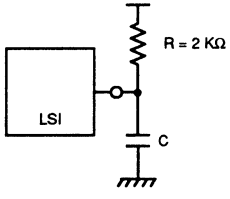
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
3.82 (22.50)	*	8.12 (11.69)	0.042	

H to Z		Z to H		
t0	KCL	t0	KCL	
6.43 (22.50)	*	3.83 (11.69)	0.024	

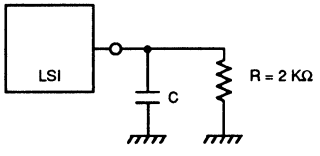
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

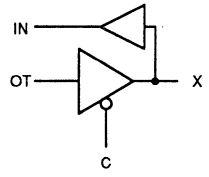
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *AU* " Version
Cell Name	**Function**	**Number of BC**
H8E2	Tri–state Output & Input Buffer (IOL=24mA) with Noise Limit Resistance and Input Buffer (CMOS, True)	8

Cell Symbol



Propagation Delay Parameter

tup

t0	KCL
0.74 3.60 (5.86)	0.03 0.024

tdn

t0	KCL	KCL2	CDR2
1.07 7.90 (11.39)	0.03 0.041		

Path: X to IN, OT to X

L to Z

t0	KCL
3.82 (22.50)	*

Z to L

t0	KCL
8.12 (11.69)	0.042

Path: C to X

H to Z

t0	KCL
6.43 (22.50)	*

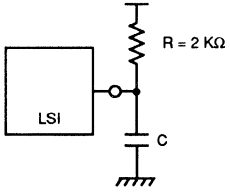
Z to H

t0	KCL
3.83 (11.69)	0.024

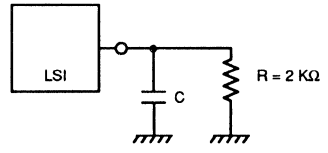
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

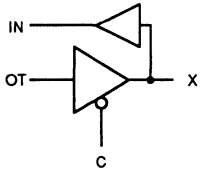
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *AU* " Version
Cell Name	**Function**	**Number of BC**
H8W1	Tri–state Output & Input Buffer (IOL=24mA) with Noise Limit Resistance and Input Buffer (TTL, True) with Pull–up Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.85 3.60 (5.86)	0.03 0.024	1.47 7.90 (11.39)	0.03 0.041			X to IN OT to X

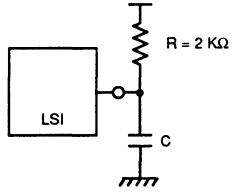
L to Z		Z to L		
t0	KCL	t0	KCL	
3.82 (22.50)	*	8.12 (11.69)	0.042	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
6.43 (22.50)	*	3.83 (11.69)	0.024	

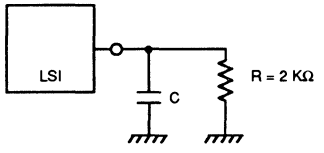
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

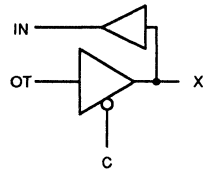
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8E1	Tri–state Output & Input Buffer (IOL=24mA) with Noise Limit Resistance and Input Buffer (CMOS, True) with Pull–up Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.74 3.60 (5.86)	0.03 0.024	1.07 7.90 (11.39)	0.03 0.041			X to IN OT to X

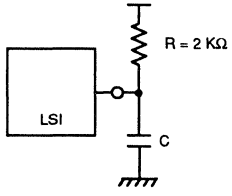
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
3.82 (22.50)	*	8.12 (11.69)	0.042	

H to Z		Z to H		
t0	KCL	t0	KCL	
6.43 (22.50)	*	3.83 (11.69)	0.024	

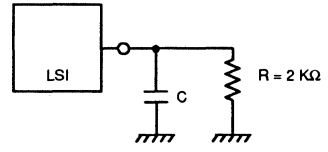
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time
at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

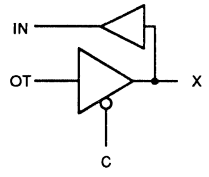
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8W0	Tri–state Output & Input Buffer (IOL=24mA) with Noise Limit Resistance and Input Buffer (TTL, True) with Pull–down Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.85 3.60 (5.86)	0.03 0.024	1.47 7.90 (11.39)	0.03 0.041			X to IN OT to X

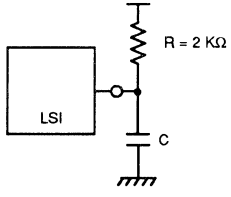
L to Z		Z to L		
t 0	KCL	t 0	KCL	
3.82 (22.50)	*	8.12 (11.69)	0.042	C to X

H to Z		Z to H		
t 0	KCL	t 0	KCL	
6.43 (22.50)	*	3.83 (11.69)	0.024	

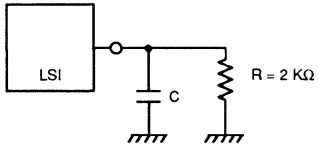
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

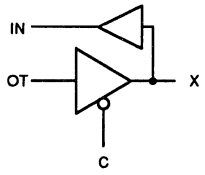
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *AU* " Version
Cell Name	**Function**	**Number of BC**
H8E0	Tri–state Output & Input Buffer (IOL=24mA) with Noise Limit Resistance and Input Buffer (CMOS, True) with Pull–down Resistance	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.74 3.60 (5.86)	0.03 0.024	1.07 7.90 (11.39)	0.03 0.041			X to IN OT to X

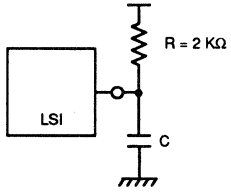
L to Z		Z to L		
t0	KCL	t0	KCL	
3.82 (22.50)	*	8.12 (11.69)	0.042	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
6.43 (22.50)	*	3.83 (11.69)	0.024	

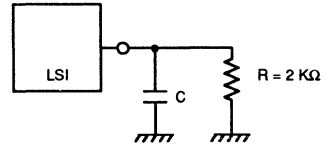
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

SINGLE-PORT RAM SPECIFICATION

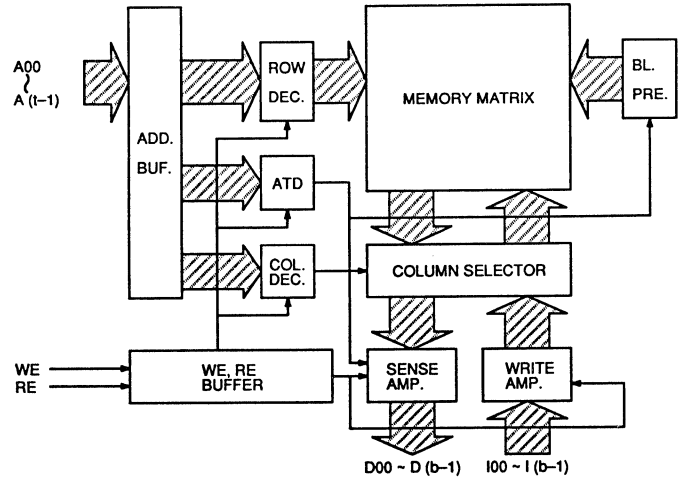
FEATURES

- Configurable size
- Non-clocked static RAM
- 1 address – 1 Read/Write port

SPECIFIC PARAMETERS

- Word size range: 4 to 2K words
- Bit size range: 1 to 72 bits

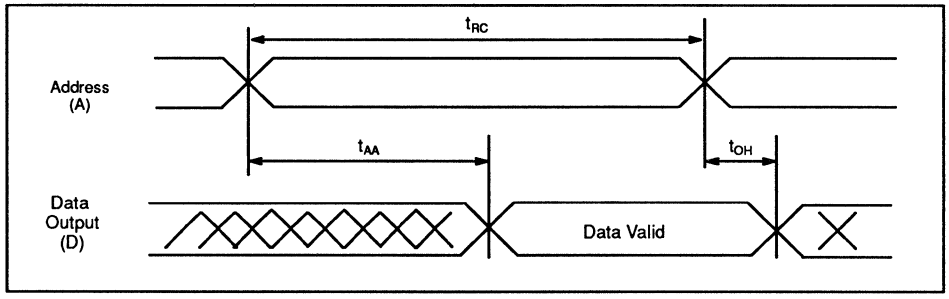
BLOCK DIAGRAM



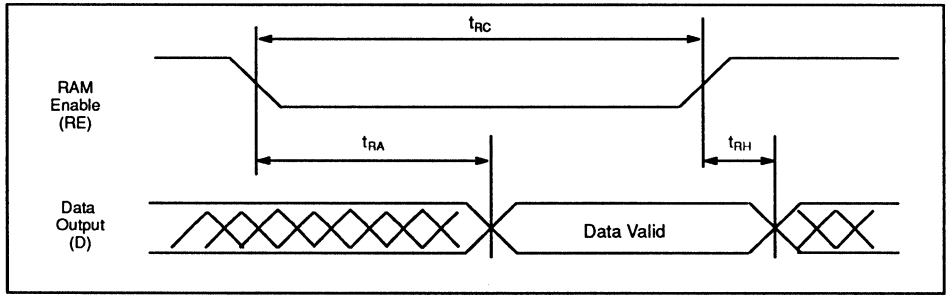
ADD. BUF.	:	Address Buffer	BL. PRE.	:	Bit Line Pre-charge
ROW DEC.	:	Row Decoder	ATD	:	Address Transition Detector
COL. DEC.	:	Column Decoder	RE	:	RAM Enable Input
A00 ~ A (t–1)	:	Address Input	WE	:	Write Enable Input
I00 ~ I (b–1)	:	Data Input	D00 ~ D (b–1)	:	Data Output

TIMING DIAGRAMS

READ CYCLE[1]



Read Cycle: Address Controlled[2]

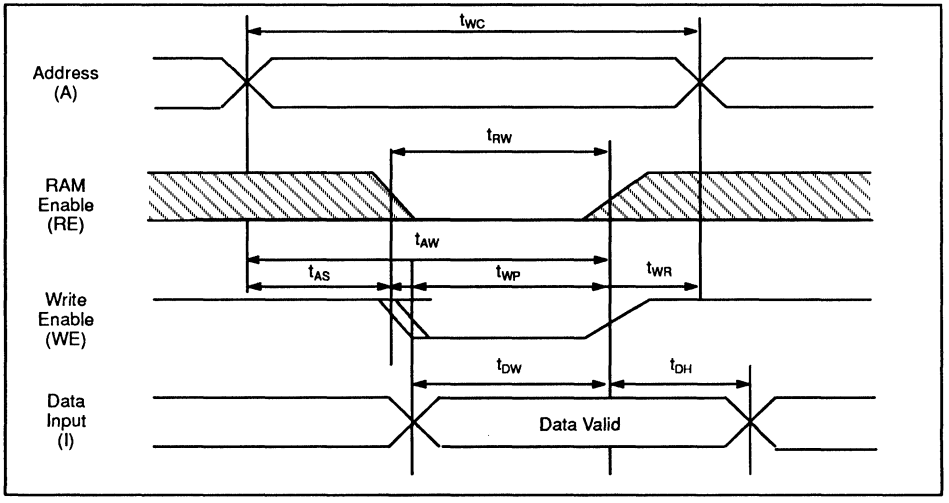


Read Cycle: RE Controlled[3]

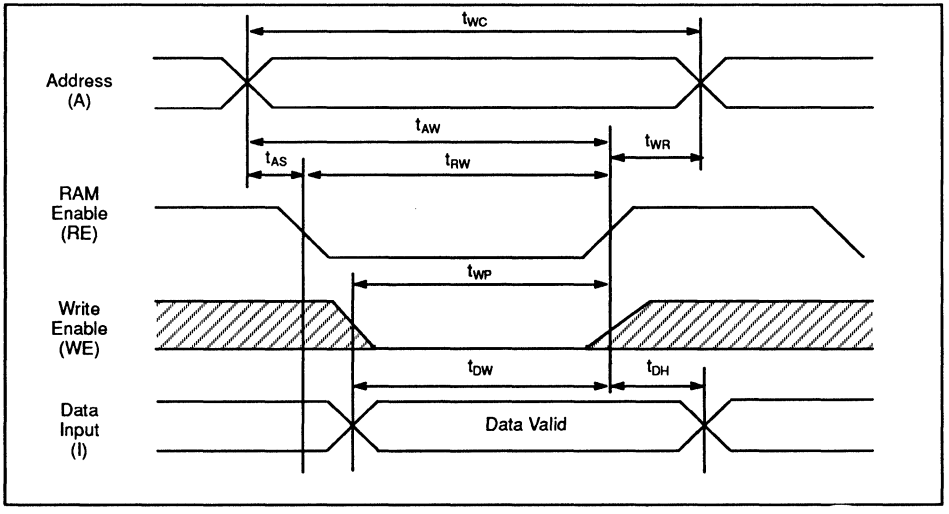
Notes: [1]WE is High for Read Cycle.
[2]RE is Low for Address Controlled Read Cycle.
[3]Address must be valid prior to or coincident with RE transition Low.

TIMING DIAGRAMS (Continued)

WRITE CYCLE[1]



Write cycle: WE Controlled[2]



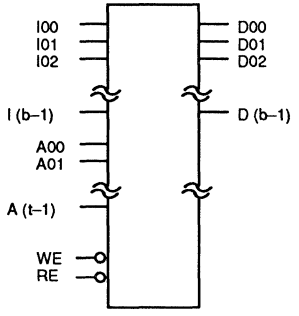
Write cycle: RE Controlled[3]

Notes: [1]The Data Output (D) is invalid in the Write mode.
[2]WE must be high during address transitions.
[3]RE must be high during address transitions.

CELL SYMBOL AND CELL SPECIFICATION

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		AU Version
Cell Name	Function	Number of BC
RAMxx	Single Port SRAM (w word x b bit)	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t_0	K_{CL}	t_0	K_{CL}	K_{CL2}	C_{DR2}	
*	0.07	*	0.04	0.07	7	A → D RE → D

Pin Name	Input Loading Factor (lu)
A4*** I4*** WE RE	1 1 1 1
Pin Name	Output Driving Factor (lu)
D4***	36

Parameter	Symbol	Typ (ns) **
Read Cycle Time	t_{RC}	
Address Access Time	t_{AA}	
RAM Enable Access Time	t_{RA}	
Output Hold from Address Change	t_{OH}	
Output Hold from RAM Enable Change	t_{RH}	
Write Cycle Time	t_{WC}	
RAM Enable to End of Write	t_{RW}	
Address Valid to End of Write	t_{AW}	
Address Setup time	t_{AS}	
Write Pulse Width	t_{WP}	
Data Setup Time	t_{DW}	
Write Recovery Time	t_{WR}	
Data Hold Time	t_{DH}	

* Refer to the Read Mode and Write Mode Tables on the following pages.

** Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.
The values indicated here depend on bit-word organization and are given in the Read Mode and Write Mode Delay Time Tables on the following pages.

*** Pin Name
When b or t ≤ 10, these pin names are described with two characters: e.g., A9.

BASIC DELAY TIME

Read Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t_{RC}	Read Cycle Time	c = 1: 0.0024 * w + 0.0044 * b + 21.07 c = 2: 0.0010 * w + 0.0110 * b + 21.10 c = 4: 0.0006 * w + 0.0176 * b + 21.12 c = 8: 0.0003 * w + 0.0341 * b + 21.02	ns
t_{AA}	Address Access Time	c = 1: 0.0024 * w + 0.0044 * b + 20.14 c = 2: 0.0010 * w + 0.0110 * b + 20.30 c = 4: 0.0006 * w + 0.0176 * b + 20.36 c = 8: 0.0003 * w + 0.0341 * b + 20.36	ns
t_{RA}	RAM Enable Access Time	c = 1: 0.0051 * w + 0.0140 * b + 18.29 c = 2: 0.0006 * w + 0.0077 * b + 19.49 c = 4: 0.0003 * w + 0.0143 * b + 19.49 c = 8: 0.0002 * w + 0.0286 * b + 19.55	ns
t_{OH}	Output Hold from Address Change	c = 1: 0.0018 * w + 0.0140 * b + 5.38 c = 2: 0.0009 * w + 0.0286 * b + 5.38 c = 4: 0.0004 * w + 0.0572 * b + 5.38 c = 8: 0.0002 * w + 0.1140 * b + 5.38	ns
t_{RH}	Output Hold from RAM Enable Change	c = 1: 0.0010 * b + 2.84 c = 2: 0.0020 * b + 2.84 c = 4: 0.0040 * b + 2.84 c = 8: 0.0079 * b + 2.84	ns

Example

To find the delay time for the read-mode parameters for a single-port RAM of 512 words, 16 bits, and c = 4:

t_{RC} = 0.0006 * w + 0.0176 * b + 21.12
= 0.0006 * 512 + 0.0176 * 16 + 21.12
= 21.71 ns

t_{AA} = 0.0006 * w + 0.0176 * b + 20.36
= 0.0006 * 512 + 0.0176 * 16 + 20.36
= 20.95 ns

t_{RA} = 0.0003 * w + 0.0143 * b + 19.49
= 0.0003 * 512 + 0.0143 * 16 + 19.49
= 19.87 ns

t_{OH} = 0.0004 * w + 0.0572 * b + 5.38
= 0.0004 * 512 + 0.0572 * 16 + 5.38
= 6.50 ns

t_{RH} = 0.0040 * b + 2.84
= 0.0040 * 16 + 2.84
= 2.90 ns

BASIC DELAY TIME (Continued)

Write Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t_{WC}	Write Cycle Time	c = 1: 0.0024 * w + 0.0044 * b + 21.07 c = 2: 0.0010 * w + 0.0110 * b + 21.10 c = 4: 0.0006 * w + 0.0176 * b + 21.12 c = 8: 0.0003 * w + 0.0341 * b + 21.02	ns
t_{RW}	RAM Enable to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 14.63 c = 2: 0.0010 * w + 0.0066 * b + 14.63 c = 4: 0.0006 * w + 0.0110 * b + 14.63 c = 8: 0.0003 * w + 0.0220 * b + 14.63	ns
t_{AW}	Address Valid to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 17.93 c = 2: 0.0010 * w + 0.0066 * b + 17.93 c = 4: 0.0006 * w + 0.0110 * b + 17.93 c = 8: 0.0003 * w + 0.0220 * b + 17.93	ns
t_{AS}	Address Setup Time	c = 1: 3.30 c = 2: 3.30 c = 4: 3.30 c = 8: 3.30	ns
t_{WP}	Write Pulse Width	c = 1: 0.0070 * w + 0.0022 * b + 10.01 c = 2: 0.0035 * w + 0.0044 * b + 10.01 c = 4: 0.0018 * w + 0.0088 * b + 10.01 c = 8: 0.0009 * w + 0.0176 * b + 10.01	ns
t_{DW}	Data Setup Time	c = 1: 0.0070 * w 8.38 c = 2: 0.0035 * w 8.38 c = 4: 0.0018 * w 8.38 c = 8: 0.0009 * w 8.38	ns
t_{WR}	Write Recovery Time	c = 1: 0.0011 * b + 3.14 c = 2: 0.0044 * b + 3.14 c = 4: 0.0066 * b + 3.14 c = 8: 0.0121 * b + 3.14	ns
t_{DH}	Data Hold Time	c = 1: 0.0094 * b + 3.51 c = 2: 0.0187 * b + 3.51 c = 4: 0.0374 * b + 3.51 c = 8: 0.0748 * b + 3.51	ns

Example

To find the delay time for the write-mode parameters for a single-port RAM of 512 words, 16 bits, and c = 4:

t_{RC} = 0.0006 * w + 0.0176 * b + 21.12
= 0.0006 * 512 + 0.0176 * 16 + 21.12
= 21.71 ns

t_{RW} = 0.0006 * w + 0.0110 * b + 14.63
= 0.0006 * 512 + 0.0110 * 16 + 14.63
= 15.11 ns

t_{AW} = 0.0006 * w+0.0110 * b + 17.93
= 0.0006 * 512 + 0.0110 * 16 + 17.93
= 18.41 ns

t_{AW} = 3.30 ns

t_{WP} = 0.00 * w + 0.0088 * b + 10.01
= 0.0018 * 512 + 0.0088 * 16 + 10.01
= 11.07 ns

t_{DW} = 0.0018 * w + 8.38
= 0.0018 * 512 + 8.38
= 9.30 ns

t_{WR} = 0.0066 * b + 3.14
= 0.0066 * 16 + 3.14
= 3.25 ns

t_{DH} = 0.0347 * b + 3.51
= 0.0347 * 16 + 3.51
= 4.11 ns

DUAL-PORT RAM SPECIFICATION

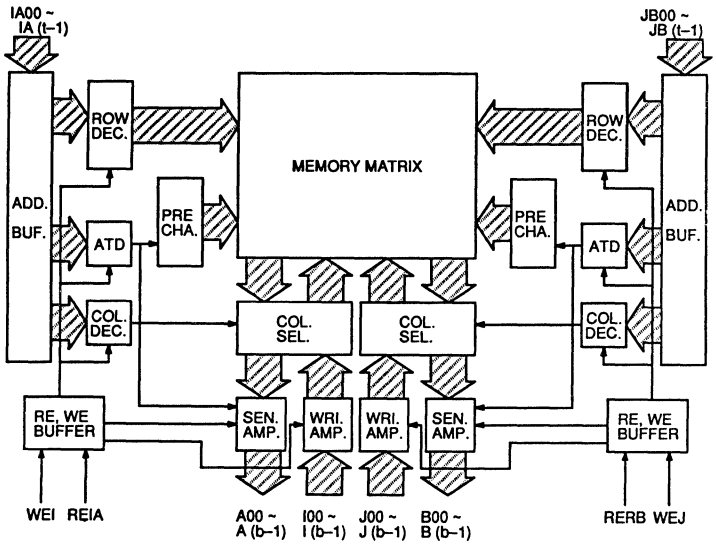
FEATURES

- Configurable size
- Non-clocked Static RAM
- 2 address – 2 Read/Write port

SPECIFIC PARAMETERS

- Word size range: 4 to 2K words
- Bit size range: 1 to 72 bits

BLOCK DIAGRAM

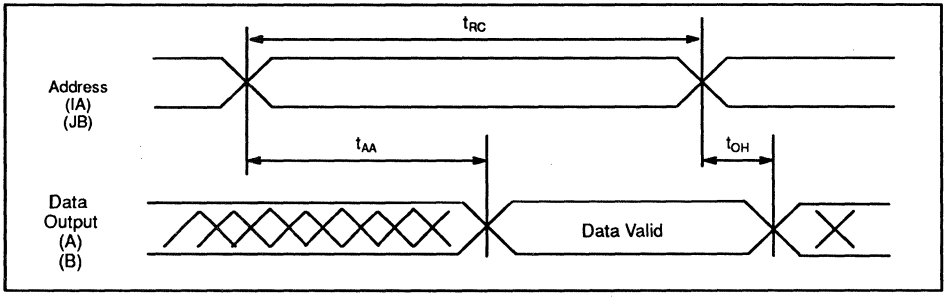


ADD. BUF.	:	Address Buffer	COL. SEL.	:	Column Select
ROW DEC.	:	Row Decoder	SEN. AMP.	:	Sense AMP.
COL. DEC.	:	Column Decoder	WRI. AMP.	:	Write AMP.
IA00 ~ IA (t–1)	:	Address Input	ATD	:	Address Transition Detector
JB00 ~ JB (t–1)	:	Address Input	REIA, RERB	:	RAM Enable Input
PRE CHA.	:	Bit Line Pre–Charge	WEI, WEJ	:	Write Enable Input
A00 ~ A (b–1)	:	Data Output	B00 ~ B (b–1)	:	Data Output
I00 ~ I (b–1)	:	Data Input	J00 ~ J (b–1)	:	Data Input

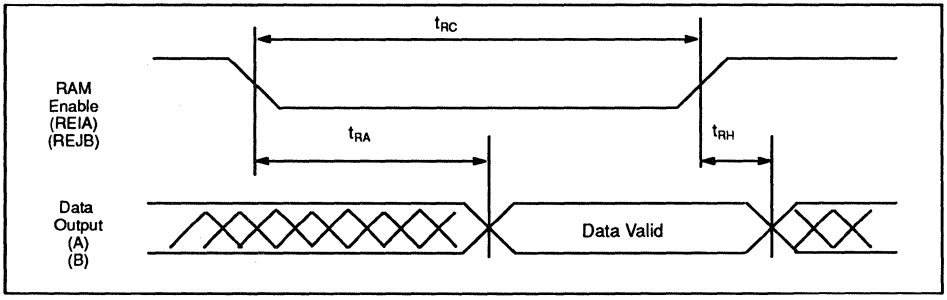
TIMING DIAGRAMS

Only when both ports are in READ mode can one address be accessed by two ports in one cycle.

READ CYCLE[1]



Read Cycle: Address Controlled[2]

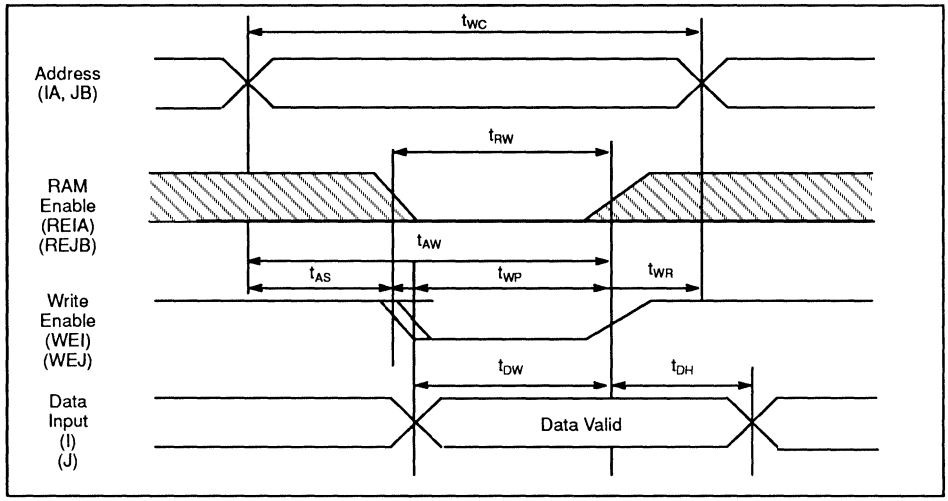


Read Cycle: RE Controlled[3]

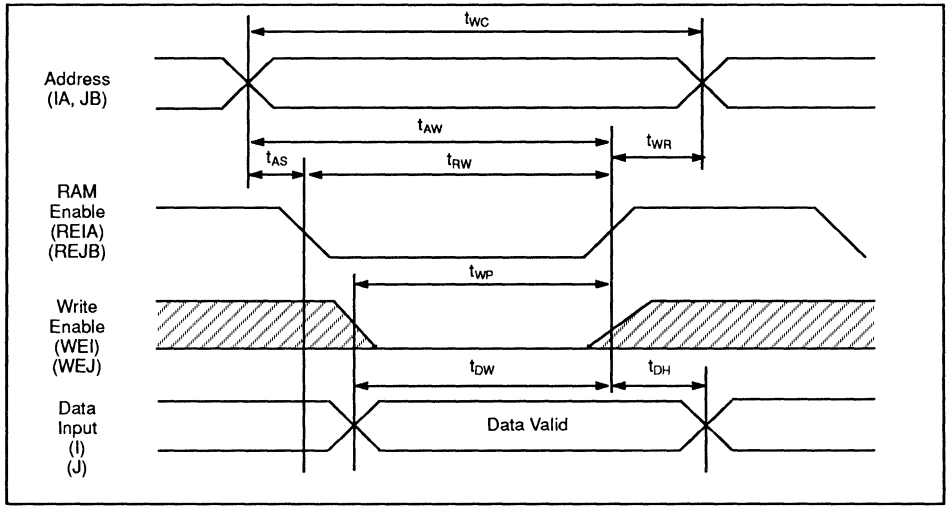
Notes: [1]WE is High for Read Cycle.
[2]RE is Low for Address Controlled Read Cycle.
[3]Address must be valid prior to or coincident with RE transition Low.

TIMING DIAGRAMS (Continued)

WRITE CYCLE[1]



Write cycle: WE Controlled[2]



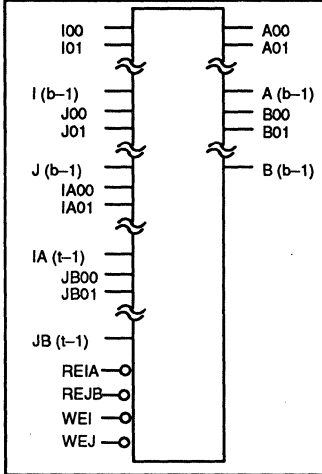
Write cycle: RE Controlled[3]

Notes: [1]The Data Output (D) is invalid in the Write mode.
[2]WE must be high during address transitions.
[3]RE must be high during address transitions.

CELL SYMBOL AND CELL SPECIFICATION

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		AU Version
Cell Name	Function	Number of BC
RAMxx	DUAL Port Static RAM (w word x b bit)	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t_0	K_{CL}	t_0	K_{CL}	K_{CL2}	C_{DR2}	
*	0.07	*	0.04	0.07	7	A → A JB → B REIA →A REJB →B

Pin Name	Input Loading Factor (Iu)
I***	1
J***	1
IA***	1
JB***	1
RE	1
WE	1

Pin Name	Output Driving Factor (Iu)
A***	36
B***	36

Parameter	Symbol	Typ (ns) **
Read Cycle Time	t_{RC}	
Address Access Time	t_{AA}	
RAM Enable Access Time	t_{RA}	
Output Hold from Address Change	t_{OH}	
Output Hold from RAM Enable Change	t_{RH}	
Write Cycle Time	t_{WC}	
RAM Enable to End of Write	t_{RW}	
Address Valid to End of Write	t_{AW}	
Address Setup time	t_{AS}	
Write Pulse Width	t_{WP}	
Data Setup Time	t_{DW}	
Write Recovery Time	t_{WR}	
Data Hold Time	t_{DH}	

* Refer to the Read Mode and Write Mode Tables on the following pages.

** Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.
The values to be indicated here depend on bit-word organization and are given by the Read Mode and Write Mode Delay Time Tables on the following pages.

*** Pin Name
When b or t ≤ 10, these pin names are described with two characters: e.g., A9.

BASIC DELAY TIME

Read Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t_{RC}	Read Cycle Time	c = 1: 0.0024 * w + 0.0044 * b + 22.07 c = 2: 0.0010 * w + 0.0110 * b + 22.10 c = 4: 0.0006 * w + 0.0176 * b + 22.12 c = 8: 0.0003 * w + 0.0341 * b + 22.02	ns
t_{AA}	Address Access Time	c = 1: 0.0024 * w + 0.0044 * b + 21.14 c = 2: 0.0010 * w + 0.0110 * b + 21.30 c = 4: 0.0006 * w + 0.0176 * b + 21.36 c = 8: 0.0003 * w + 0.0341 * b + 21.36	ns
t_{RA}	RAM Enable Access Time	c = 1: 0.0051 * w + 0.0140 * b + 19.29 c = 2: 0.0006 * w + 0.0077 * b + 20.49 c = 4: 0.0003 * w + 0.0143 * b + 20.49 c = 8: 0.0002 * w + 0.0286 * b + 20.55	ns
t_{OH}	Output Hold from Address Change	c = 1: 0.0018 * w + 0.0140 * b + 5.38 c = 2: 0.0009 * w + 0.0286 * b + 5.38 c = 4: 0.0004 * w + 0.0572 * b + 5.38 c = 8: 0.0002 * w + 0.1140 * b + 5.38	ns
t_{RH}	Output Hold from Ram Enable Change	c = 1: 0.0010 * b + 2.84 c = 2: 0.0020 * b + 2.84 c = 4: 0.0040 * b + 2.84 c = 8: 0.0079 * b + 2.84	ns

Example

To find the delay time for the write-mode parameters for a dual-port RAM of 512 words, 16 bits, and c = 4:

t_{RC} = 0.0006 * w + 0.0176 * b + 22.12
= 0.0006 * 512 + 0.0176 * 16+22.12
= 22.71 ns

t_{AA} = 0.0006 * w+0.0176 * b + 21.36
= 0.0006 * 512 + 0.0176 * 16 + 21.36
= 21.95 ns

t_{RA} = 0.0003 * w + 0.0143 * b + 20.49
= 0.0003 * 512 + 0.0143 * 16 + 20.49
= 20.87 ns

t_{OH} = 0.0004 * w + 0.0572 * b + 5.38
= 0.0004 * 512 + 0.0572 * 16 + 5.38
= 6.50 ns

t_{RH} = 0.0040 * b + 2.84
= 0.0040 * 16 + 2.84
= 2.90 ns

BASIC DELAY TIME (Continued)

Write Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t_{WC}	Write Cycle Time	c = 1: 0.0024 * w + 0.0044 * b + 22.07 c = 2: 0.0010 * w + 0.0110 * b + 22.10 c = 4: 0.0006 * w + 0.0176 * b + 22.12 c = 8: 0.0003 * w + 0.0341 * b + 22.02	ns
t_{RW}	RAM Enable to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 15.63 c = 2: 0.0010 * w + 0.0066 * b + 15.63 c = 4: 0.0006 * w + 0.0110 * b + 15.63 c = 8: 0.0003 * w + 0.0220 * b + 15.63	ns
t_{AW}	Address Valid to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 18.93 c = 2: 0.0010 * w + 0.0066 * b + 18.93 c = 4: 0.0006 * w + 0.0110 * b + 18.93 c = 8: 0.0003 * w + 0.0220 * b + 18.93	ns
t_{AS}	Address Setup Time	c = 1: 3.30 c = 2: 3.30 c = 4: 3.30 c = 8: 3.30	ns
t_{WP}	Write Pulse Width	c = 1: 0.0070 * w + 0.0022 * b + 11.01 c = 2: 0.0035 * w + 0.0044 * b + 11.01 c = 4: 0.0018 * w + 0.0088 * b + 11.01 c = 8: 0.0009 * w + 0.0176 * b + 11.01	ns
t_{DW}	Data Setup Time	c = 1: 0.0070 * w 9.38 c = 2: 0.0035 * w 9.38 c = 4: 0.0018 * w 9.38 c = 8: 0.0009 * w 9.38	ns
t_{WR}	Write Recovery Time	c = 1: 0.0011 * b + 3.14 c = 2: 0.0044 * b + 3.14 c = 4: 0.0066 * b + 3.14 c = 8: 0.0121 * b + 3.14	ns
t_{DH}	Data Hold Time	c = 1: 0.0094 * b + 3.51 c = 2: 0.0187 * b + 3.51 c = 4: 0.0374 * b + 3.51 c = 8: 0.0748 * b + 3.51	ns

Example

To find the delay time for the write-mode parameters for a dual-port RAM of 512 words, 16 bits and c = 4:

t_{WC} = 0.0006 * w + 0.0176 * b + 22.12
= 0.0006 * 512 + 0.0176 * 16 + 22.12
= 22.71 ns

t_{RW} = 0.0006 * w + 0.0110 * b + 15.63
= 0.0006 * 512 + 0.0110 * 16 + 15.63
= 16.11 ns

t_{AW} = 0.0006 * w + 0.0110 * b + 18.93
= 0.0006 * 512 + 0.0110 * 16 + 18.93
= 19.41 ns

t_{AS} = 3.30 ns

t_{WP} = 0.0018 * w + 0.0088 * b + 11.01
= 0.0018 * 512 + 0.0088 * 16 + 11.01
= 12.07 ns

t_{DW} = 0.0018 * w + 9.38
= 0.0018 * 512 + 9.38
= 10.30 ns

t_{WR} = 0.0066 * b + 3.14
= 0.0066 * 16 + 3.14
= 3.25 ns

t_{DH} = 0.0347 * b + 3.51
= 0.0347 * 16 + 3.51
= 4.11 ns

TRIPLE-PORT RAM SPECIFICATION

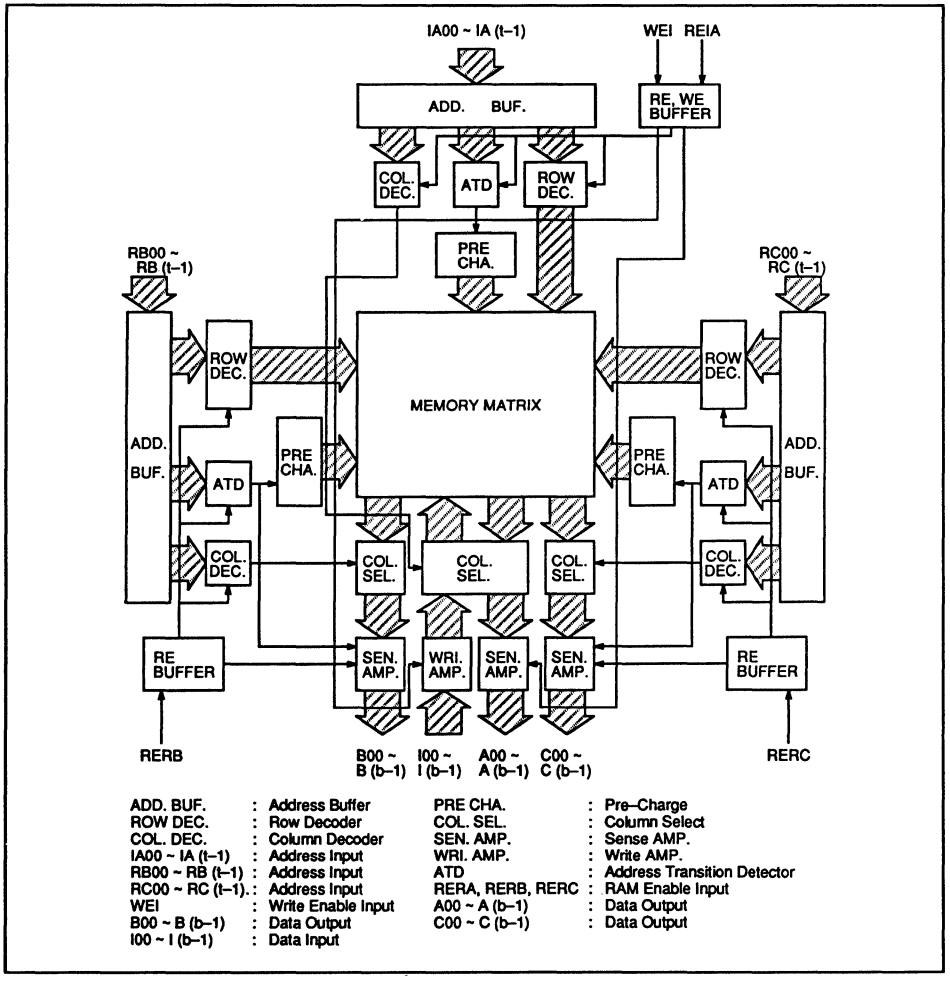
FEATURES

- Configurable word/bit organization
- Non-clocked static RAM
- 3 addresses – 2 Read ports and 1 Read/Write port

SPECIFIC PARAMETERS

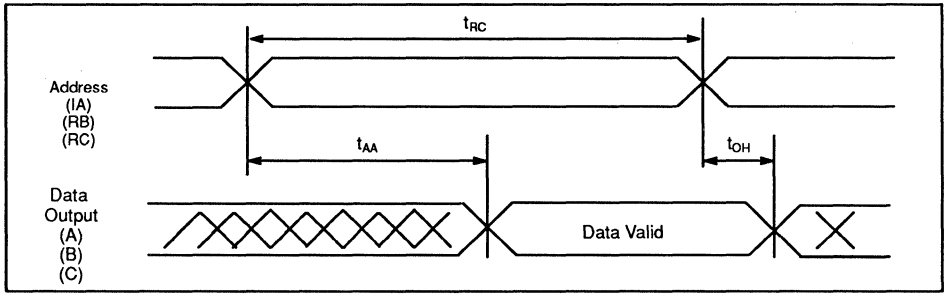
- Word size range: 4 to 2048 words
- Bit size range: 2 to 72 bits
- Total bit size range: 64 to 18K bits

BLOCK DIAGRAM

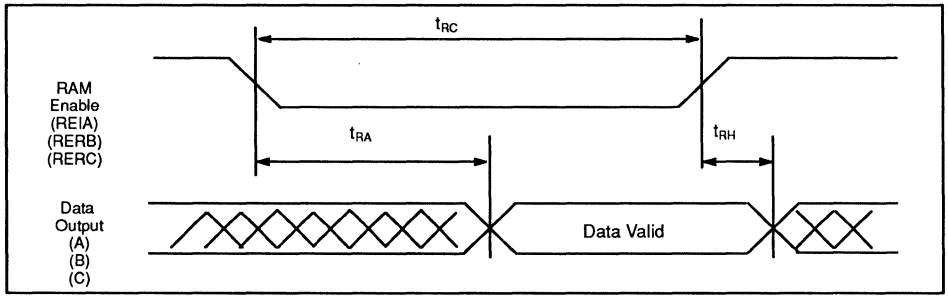


TIMING DIAGRAMS

READ CYCLE[1]



Read Cycle: Address Controlled[2]

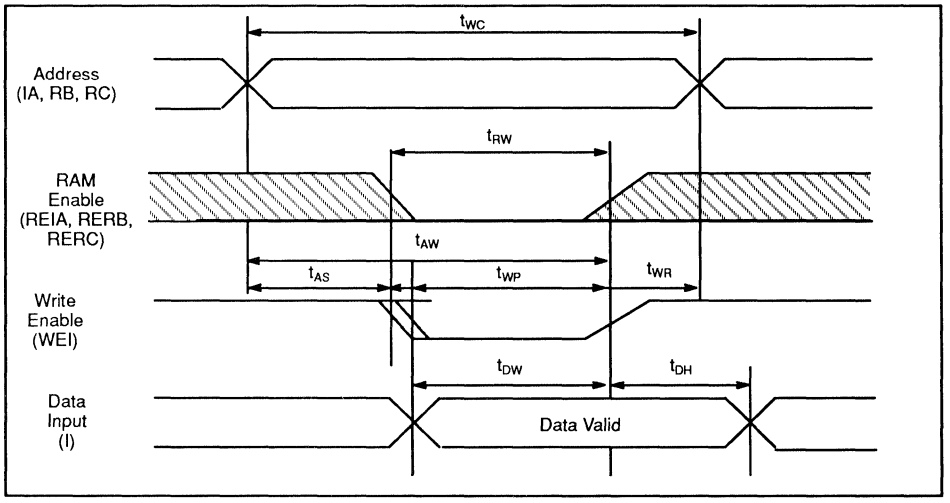


Read Cycle: RE Controlled[3]

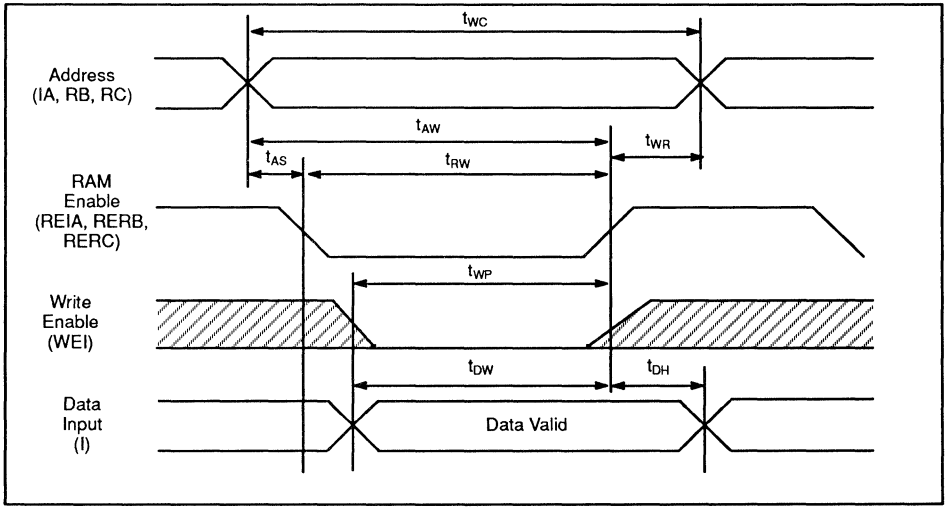
Notes: [1]WEI is High for Read Cycle.
[2]RE is Low for Address Controlled Read Cycle.
[3]Address must be valid prior to or coincident with RE transition Low.

TIMING DIAGRAMS (Continued)

WRITE CYCLE[1]



Write cycle: WE Controlled[2]



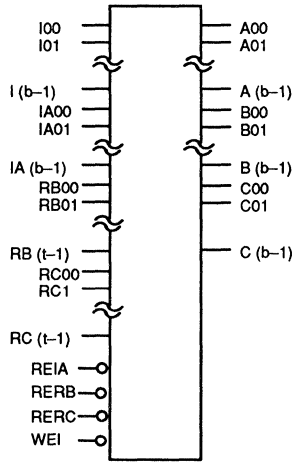
Write cycle: RE Controlled[3]

Notes: [1]The Data Output (A) is invalid in the Write mode.
[2]WE must be high during address transitions.
[3]RE must be high during address transitions.

CELL SYMBOL AND CELL SPECIFICATION

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		AU Version
Cell Name	Function	Number of BC
RAMxx	Triple Port Static RAM (w word x b bit)	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t_0	K_{CL}	t_0	K_{CL}	K_{CL2}	C_{DR2}	
*	0.07	*	0.04	0.07	7	IA → A RB → B RC → C REIA → A RERB → B RERC → C

Pin Name	Input Loading Factor (lu)
I	1
IA	1
RB	1
RC	1
RE	1
WE	1

Pin Name	Output Driving Factor (lu)
A	36
B	36
C	36

Parameter	Symbol	Typ (ns) **
Read Cycle Time	t_{RC}	
Address Access Time	t_{AA}	
RAM Enable Access Time	t_{RA}	
Output Hold from Address Change	t_{OH}	
Output Hold from RAM Enable Change	t_{RH}	
Write Cycle Time	t_{WC}	
RAM Enable to End of Write	t_{RW}	
Address Valid to End of Write	t_{AW}	
Address Setup time	t_{AS}	
Write Pulse Width	t_{WP}	
Data Setup Time	t_{DW}	
Write Recovery Time	t_{WR}	
Data Hold Time	t_{DH}	

* Refer to the Read Mode and Write Mode Tables on the following pages.

** Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.
The values to be indicated here depend on bit-word organization and are given by the Read Mode and Write Mode Delay Time Tables on the following pages.

*** Pin Name
When b or t ≤ 10, these pin names are described with two characters: e.g., A9.

BASIC DELAY TIME

Read Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t_{RC}	Read Cycle Time	c = 1: 0.0024 * w + 0.0044 * b + 22.27 c = 2: 0.0010 * w + 0.0110 * b + 22.30 c = 4: 0.0006 * w + 0.0176 * b+ 22.32 c = 8: 0.0003 * w + 0.0341 * b + 22.22	ns
t_{AA}	Address Access Time	c = 1: 0.0024 * w + 0.0044 * b + 21.34 c = 2: 0.0010 * w + 0.0110 * b + 21.50 c = 4: 0.0006 * w + 0.0176 * b + 21.56 c = 8: 0.0003 * w + 0.0341 * b + 21.56	ns
t_{RA}	RAM Enable Access Time	c = 1: 0.0051 * w + 0.0140 * b + 19.44 c = 2: 0.0006 * w + 0.0077 * b + 20.69 c = 4: 0.0003 * w + 0.0143 * b + 20.69 c = 8: 0.0002 * w + 0.0286 * b + 20.75	ns
t_{OH}	Output Hold from Address Change	c = 1: 0.0018 * w + 0.0140 * b + 5.38 c = 2: 0.0009 * w + 0.0286 * b + 5.38 c = 4: 0.0004 * w + 0.0572 * b + 5.38 c = 8: 0.0002 * w + 0.1140 * b + 5.38	ns
t_{RH}	Output Hold from RAM Enable Change	c = 1: 0.0010 * b + 2.84 c = 2: 0.0020 * b + 2.84 c = 4: 0.0040 * b + 2.84 c = 8: 0.0079 * b + 2.84	ns

Example

To find the delay time for the write-mode parameters for a triple-port RAM of 512 words, 16 bits, and c = 4:

t_{RC} = 0.0006 * w + 0.0176 * b + 22.32
= 0.0006 * 512 + 0.0176 * 16 + 22.32
= 22.91 ns (typ)

t_{AA} = 0.0006 * w+0.0176 * b + 21.56
= 0.0006 * 512 + 0.0176 * 16 + 21.56
= 22.15 ns (typ)

t_{RA} = 0.0003 * w + 0.0143 * b + 20.69
= 0.0003 * 512 + 0.0143 * 16 + 20.69
= 21.08 ns (typ)

t_{OH} = 0.0004 * w + 0.0572 * b + 5.38
= 0.0004 * 512 + 0.0572 * 16 + 5.38
= 6.50 ns (typ)

t_{RH} = 0.0040 * b + 2.84
= 0.0040 * 16 + 2.84
= 2.91 ns (typ)

BASIC DELAY TIME (Continued)

Write Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t_{WC}	Write Cycle Time	c = 1: 0.0024 * w + 0.0044 * b + 22.27 c = 2: 0.0010 * w + 0.0110 * b + 22.30 c = 4: 0.0006 * w + 0.0176 * b + 22.32 c = 8: 0.0003 * w + 0.0341 * b + 22.22	ns
t_{RW}	RAM Enable to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 15.63 c = 2: 0.0010 * w + 0.0066 * b + 15.63 c = 4: 0.0006 * w + 0.0110 * b + 15.63 c = 8: 0.0003 * w + 0.0220 * b + 15.63	ns
t_{AW}	Address Valid to End of Write	c = 1: 0.0024 * w + 0.0033 * b + 18.93 c = 2: 0.0010 * w + 0.0066 * b + 18.93 c = 4: 0.0006 * w + 0.0110 * b + 18.93 c = 8: 0.0003 * w + 0.0220 * b + 18.93	ns
t_{AS}	Address Setup Time	c = 1: 3.30 c = 2: 3.30 c = 4: 3.30 c = 8: 3.30	ns
t_{WP}	Write Pulse Width	c = 1: 0.0070 * w + 0.0022 * b + 11.01 c = 2: 0.0035 * w + 0.0044 * b + 11.01 c = 4: 0.0018 * w + 0.0088 * b + 11.01 c = 8: 0.0009 * w + 0.0176 * b + 11.01	ns
t_{DW}	Data Setup Time	c = 1: 0.0070 * w + 9.38 c = 2: 0.0035 * w + 9.38 c = 4: 0.0018 * w + 9.38 c = 8: 0.0009 * w + 9.38	ns
t_{WR}	Write Recovery Time	c = 1: 0.0011 * b + 3.34 c = 2: 0.0044 * b + 3.34 c = 4: 0.0066 * b + 3.34 c = 8: 0.0121 * b + 3.34	ns
t_{DH}	Data Hold Time	c = 1: 0.0094 * b + 3.51 c = 2: 0.0187 * b + 3.51 c = 4: 0.0374 * b + 3.51 c = 8: 0.0748 * b + 3.51	ns

Example

To find the delay time for the write-mode parameters for a triple-port RAM of 512 words, 16 bits and c = 4:

t_{WC} = 0.0006 * w + 0.0176 * b + 22.32
= 0.0006 * 512 + 0.0176 * 16 + 22.32
= 22.91 ns (typ)

t_{RW} = 0.0006 * w + 0.0110 * b + 15.63
= 0.0006 * 512 + 0.0110 * 16 + 15.63
= 16.12 ns (typ)

t_{AW} = 0.0006 * w + 0.0110 * b + 18.93
= 0.0006 * 512 + 0.0110 * 16 + 18.93
= 19.42 ns (typ)

t_{AS} = 3.30 ns (typ)

t_{WP} = 0.0018 * w + 0.0088 * b + 11.01
= 0.0018 * 512 + 0.0088 * 16 + 11.01
= 12.08 ns (typ)

t_{DW} = 0.0018 * w + 9.38
= 0.0018 * 512 + 9.38
= 10.31 ns (typ)

t_{WR} = 0.0066 * b + 3.34
= 0.0066 * 16 + 3.34
= 3.45 ns (typ)

t_{DH} = 0.0347 * b + 3.51
= 0.0347 * 16 + 3.51
= 4.11 ns (typ)

ROM SPECIFICATION

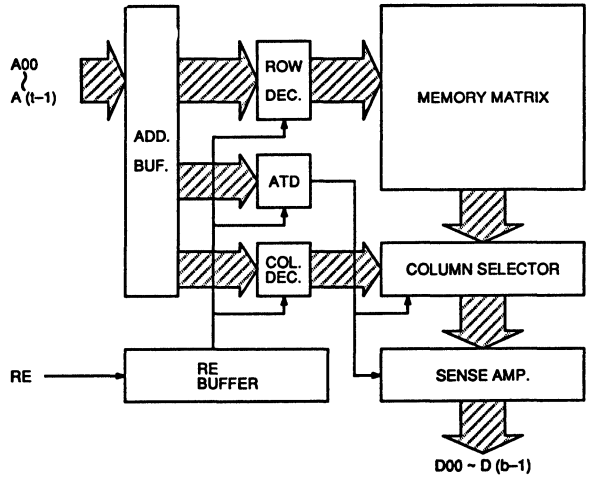
FEATURES

- Configurable size
- Non-clocked static ROM

SPECIFIC PARAMETERS

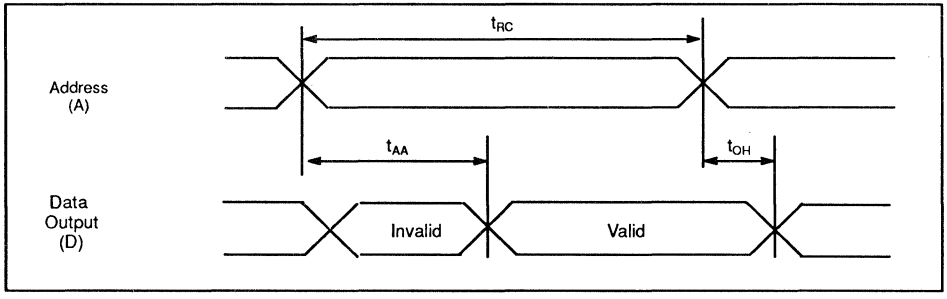
- Word size range: 16 to 2K words
- Bit size range: 4 to 64 bits

BLOCK DIAGRAM

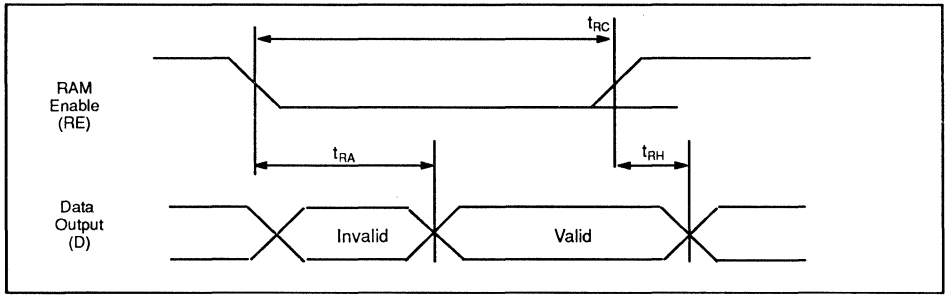


ADD. BUF. : Address Buffer
ROW DEC. : Row Decoder
COL. DEC. : Column Decoder
A00 ~ A (t–1) : Address Input
ATD : Address Transition Detector
RE : ROM Enable Input
D00 ~ D (b–1) : Data Output

TIMING DIAGRAMS



Address Control[1]



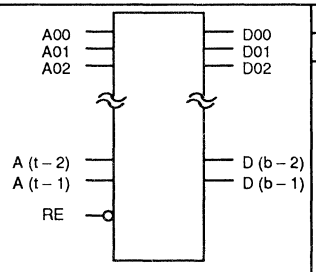
RE Control[2]

Notes: [1]ROM Enable (RE) must be Low in the address control
[2]In RE control, the address must be validated before ROM Enable (RE) becomes low.

CELL SYMBOL AND CELL SPECIFICATION

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		AU Version
Cell Name	Function	Number of BC
ROMxx	Mask ROM (w word x b bit)	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t_0	K_{CL}	t_0	K_{CL}	K_{CL2}	C_{DR2}	
*	0.07	*	0.04	0.07	7	A → D RE → D

Pin Name	Input Loading Factor (lu)
A*** RE	

Pin Name	Output Driving Factor (lu)
D***	36

Parameter	Symbol	Typ (ns) **
Read Cycle Time	t_{RC}	
Address Access Time	t_{AA}	
RAM Enable Access Time	t_{RA}	
Output Hold from Address Change	t_{OH}	
Output Hold from RAM Enable Change	t_{RH}	

* Refer to the Read Mode and Write Mode Tables on the following pages.

** Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.
The values indicated here depend on bit-word organization and are given in the Read Mode Delay Time Table on the following page.

*** Pin Name
When b or t ≤ 10, these pin names are described with two characters: e.g., A9.

BASIC DELAY TIME

Read Mode

Symbol	Parameter	Equation (Typical Value)	Unit
t_{RC}	Read Cycle Time	c = 4: 33.12 c = 8: 33.02	ns
t_{AA}	Address Access Time	c = 4: 0.0161 * w + 0.0226 * b + 16.85 c = 8: 0.0080 * w + 0.0258 * b + 17.81	ns
t_{RA}	RAM Enable Access Time	c = 4: 0.0173 * w + 0.0290 * b + 16.55 c = 8: 0.0091 * w + 0.0487 * b + 16.63	ns
t_{OH}	Output Hold from Address Change	c = 4: 0.0194 * b + 4.36 c = 8: 0.0258 * b + 4.40	ns
t_{RH}	Output Hold from RAM Enable Change	c = 4: 0.0194 * w + 6.76 c = 8: 0.0258 * w + 6.61	ns

Example

To find the delay time for the Read-mode for a ROM of 512 words, 16 bits, and c = 4:

2

t_{RC} = 33.12

t_{AA} = 0.0161 * w + 0.0226 * b + 16.85
= 0.0161 * 512 + 0.0226 * 16 + 16.85
= 25.46 ns

t_{RA} = 0.0173 * w + 0.0290 * b + 16.55
= 0.0173 * 512 + 0.0290 * 16 + 16.55
= 25.88 ns

t_{OH} = 0.0194 * b + 4.36
= 0.0194 * 16 + 4.36
= 4.67 ns

t_{RH} = 0.0194 * b + 6.76
= 0.0194 * 16 + 6.76
= 7.07 ns

Appendix A: General AC Specifications

Simulation Delay Specifications
(Recommended Operating Conditions, Ta = 0 to 70°C, V_{DD} = 5 V±5%

Delay Multipliers	Min.	Max.
Pre-layout Simulation	0.35	t_{maxB}
Post-layout Simulation	0.40	t_{maxA}

Junction Temperature (Tj)	tmaxB	tmaxA
Tj ≤ 60°C	1.65	1.55
60°C<Tj ≤ 70°C	1.70	1.60
70°C<Tj ≤ 80°C	1.75	1.65
80°C<Tj ≤ 90°C	1.80	1.70
90°C<Tj ≤ 105°C	1.85	1.75
105°C<Tj ≤ 120°C	1.90	1.80
120°C<Tj ≤ 130°C[1]	1.95	1.85
130°C<Tj ≤ 140°C[2]	2.00	1.90
140°C<Tj ≤ 150°C[2]	2.05	1.95

NOTES: 1. This condition cannot be applied to devices in some plastic packages. If this condition is required for devices in plastic, please consult Fujitsu.

2. This condition cannot be applied to devices in plastic packages. If this condition is required even for ceramic packages, please consult Fujitsu.

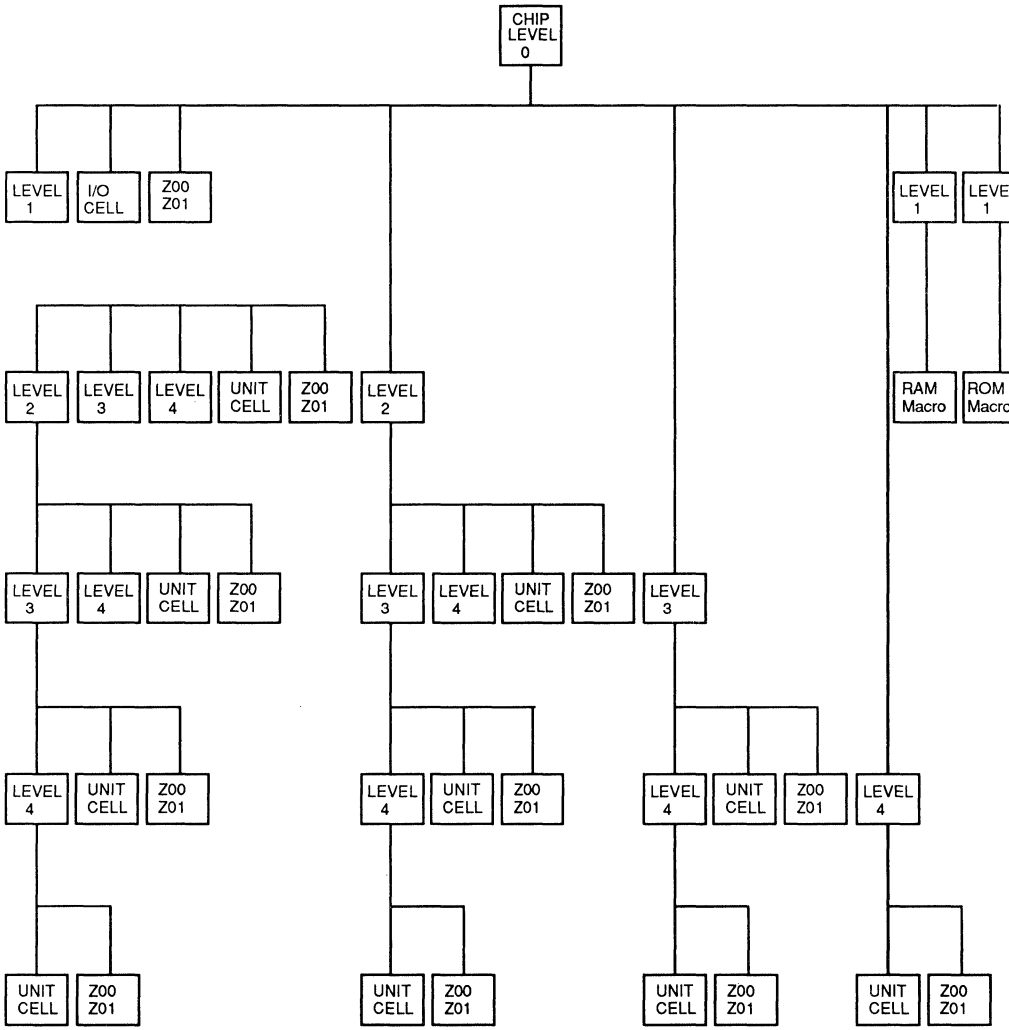
Tj is determined by the following formula:

$$Tj = T_{aMAX} + \theta ja \times Pd\ (°C)$$

where

Pd: Power dissipation (W)
θja: Thermal Resistance (°C/W). This value is determined for each package.
TaMAX: Maximum Ambient Termperature (°C)

Appendix B: Hierarchical Structure



2

Appendix C: Estimation Tables for Metal Loading

C-10KAU (Main Block)

NDI	C_L (lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	4.1	2.8	1.8	1.1	0.6
2	6.2	4.3	2.7	1.7	0.8
3	8.3	5.7	3.7	2.3	1.1
4	9.7	6.7	4.3	2.7	1.3
5	10.7	7.4	4.7	2.9	1.5
6	11.6	8.0	5.1	3.2	1.6
7	12.7	8.8	5.6	3.5	1.7
8	13.2	9.1	5.8	3.6	1.8
9	13.5	9.3	6.0	3.7	1.8
10	13.9	9.6	6.1	3.8	1.9
11	13.9	9.6	6.1	3.8	1.9
12	14.1	9.7	6.2	3.9	1.9
13	14.3	9.9	6.3	3.9	1.9
14	14.6	10.1	6.5	4.0	2.0
15	14.6	10.1	6.5	4.0	2.0
16 – 30	15.8	10.9	7.0	4.3	2.2
31 – 50	18.1	12.5	8.0	5.0	2.5
51 – 75	18.6	12.8	8.2	5.1	2.5
76 –100	20.5	14.1	9.1	5.6	2.8

C-10KAU (Sub Block)

NDI	C_L (lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	1.9	1.2	0.7	0.4
2	3.4	2.1	1.3	0.6
3	4.8	3.1	1.9	0.9
4	5.8	3.7	2.3	1.1
5	6.5	4.1	2.5	1.3
6	7.1	4.5	2.8	1.4
7	7.9	5.0	3.1	1.5
8	8.2	5.2	3.2	1.6
9	8.4	5.4	3.3	1.6
10	8.7	5.5	3.4	1.7
11	8.7	5.5	3.4	1.7
12	8.8	5.6	3.5	1.7
13	9.0	5.7	3.5	1.7
14	9.2	5.9	3.6	1.8
15	9.2	5.9	3.6	1.8
16 – 30	10.0	6.4	3.9	2.0
31 – 50	11.6	7.4	4.6	2.3
51 – 75	11.9	7.6	4.7	2.3
76 – 100	13.2	8.5	5.2	2.6

Appendix C: Estimation Tables for Metal Loading (Continued)

C-15KAU (Main Block)

NDI	C_L (lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	5.1	2.8	1.8	1.1	0.6
2	7.7	4.3	2.7	1.7	0.8
3	10.4	5.7	3.7	2.3	1.1
4	12.1	6.7	4.3	2.7	1.3
5	13.4	7.4	4.7	2.9	1.5
6	14.4	8.0	5.1	3.2	1.6
7	15.8	8.8	5.6	3.5	1.7
8	16.4	9.1	5.8	3.6	1.8
9	16.9	9.3	6.0	3.7	1.8
10	17.3	9.6	6.1	3.8	1.9
11	17.3	9.6	6.1	3.8	1.9
12	17.6	9.7	6.2	3.9	1.9
13	17.8	9.9	6.3	3.9	1.9
14	18.3	10.1	6.5	4.0	2.0
15	18.3	10.1	6.5	4.0	2.0
16 – 30	19.7	10.9	7.0	4.3	2.2
31 – 50	22.6	12.5	8.0	5.0	2.5
51 – 75	23.2	12.8	8.2	5.1	2.5
76 – 100	25.6	14.1	9.1	5.6	2.8

C-15KAU (Sub Block)

NDI	C_L (lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	1.9	1.2	0.7	0.4
2	3.4	2.1	1.3	0.6
3	4.8	3.1	1.9	0.9
4	5.8	3.7	2.3	1.1
5	6.5	4.1	2.5	1.3
6	7.1	4.5	2.8	1.4
7	7.9	5.0	3.1	1.5
8	8.2	5.2	3.2	1.6
9	8.4	5.4	3.3	1.6
10	8.7	5.5	3.4	1.7
11	8.7	5.5	3.4	1.7
12	8.8	5.6	3.5	1.7
13	9.0	5.7	3.5	1.7
14	9.2	5.9	3.6	1.8
15	9.2	5.9	3.6	1.8
16 – 30	10.0	6.4	3.9	2.0
31 – 50	11.6	7.4	4.6	2.3
51 – 75	11.9	7.6	4.7	2.3
76 – 100	13.2	8.5	5.2	2.6

Appendix C: Estimation Tables for Metal Loading (Continued)

C-20KAU (Main Block)

NDI	C_L (lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	5.9	2.8	1.8	1.1	0.6
2	8.9	4.3	2.7	1.7	0.8
3	11.9	5.7	3.7	2.3	1.1
4	13.9	6.7	4.3	2.7	1.3
5	15.4	7.4	4.7	2.9	1.5
6	16.6	8.0	5.1	3.2	1.6
7	18.2	8.8	5.6	3.5	1.7
8	18.9	9.1	5.8	3.6	1.8
9	19.4	9.3	6.0	3.7	1.8
10	19.9	9.6	6.1	3.8	1.9
11	19.9	9.6	6.1	3.8	1.9
12	20.2	9.7	6.2	3.9	1.9
13	20.5	9.9	6.3	3.9	1.9
14	21.0	10.1	6.5	4.0	2.0
15	21.0	10.1	6.5	4.0	2.0
16 – 30	22.7	10.9	7.0	4.3	2.2
31 – 50	26.0	12.5	8.0	5.0	2.5
51 – 75	26.7	12.8	8.2	5.1	2.5
76 –100	29.4	14.1	9.1	5.6	2.8

C-20KAU (Sub Block)

NDI	C_L (lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	1.9	1.2	0.7	0.4
2	3.4	2.1	1.3	0.6
3	4.8	3.1	1.9	0.9
4	5.8	3.7	2.3	1.1
5	6.5	4.1	2.5	1.3
6	7.1	4.5	2.8	1.4
7	7.9	5.0	3.1	1.5
8	8.2	5.2	3.2	1.6
9	8.4	5.4	3.3	1.6
10	8.7	5.5	3.4	1.7
11	8.7	5.5	3.4	1.7
12	8.8	5.6	3.5	1.7
13	9.0	5.7	3.5	1.7
14	9.2	5.9	3.6	1.8
15	9.2	5.9	3.6	1.8
16 – 30	10.0	6.4	3.9	2.0
31 – 50	11.6	7.4	4.6	2.3
51 – 75	11.9	7.6	4.7	2.3
76 – 100	13.2	8.5	5.2	2.6

Appendix C: Estimation Tables for Metal Loading (Continued)

C-30KAU (Main Block)

NDI	C_L(lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	9.9	7.8	5.5	3.5	1.7
2	14.9	11.6	8.3	5.3	2.6
3	20.0	15.6	11.1	7.1	3.5
4	23.4	18.3	13.0	8.3	4.1
5	25.9	20.3	14.4	9.2	4.6
6	27.9	21.9	15.5	9.9	4.9
7	30.6	23.9	17.0	10.9	5.4
8	31.8	24.9	17.6	11.3	5.6
9	32.6	25.5	18.1	11.6	5.7
10	33.4	26.2	18.6	11.9	5.9
11	33.4	26.2	18.6	11.9	5.9
12	33.9	26.5	18.8	12.0	6.0
13	34.4	26.9	19.1	12.2	6.1
14	35.2	27.6	19.6	12.5	6.2
15	35.2	27.6	19.6	12.5	6.2
16 – 30	38.1	29.9	21.2	13.5	6.7
31 – 50	43.6	34.2	24.2	15.5	7.7
51 – 75	44.9	35.1	24.9	15.9	7.9
76 –100	49.3	38.6	27.3	17.5	8.7

C-30KAU (Sub Block)

NDI	C_L(lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	4.7	3.3	2.2	1.0
2	8.6	6.1	3.9	1.9
3	12.6	8.9	5.7	2.8
4	15.2	10.8	7.0	3.4
5	17.2	12.2	7.8	3.8
6	18.8	13.3	8.6	4.2
7	20.6	14.8	9.5	4.7
8	21.8	15.5	9.9	4.9
9	22.5	15.9	10.2	5.0
10	23.1	16.4	10.5	5.2
11	23.1	16.4	10.5	5.2
12	23.4	16.6	10.7	5.2
13	23.9	16.9	10.9	5.3
14	24.5	17.4	11.2	5.5
15	24.5	17.4	11.2	5.5
16 – 30	26.8	19.0	12.2	6.0
31 – 50	31.1	22.1	14.1	7.0
51 – 75	32.1	22.7	14.6	7.2
76 – 100	35.5	25.2	16.1	8.0

Appendix C: Estimation Tables for Metal Loading (Continued)

C-40KAU (Main Block)

NDI	C_L (lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	11.3	7.8	5.5	3.5	1.7
2	17.0	11.6	8.3	5.3	2.6
3	22.8	15.6	11.1	7.1	3.5
4	26.7	18.3	13.0	8.3	4.1
5	29.6	20.3	14.4	9.2	4.6
6	31.9	21.9	15.5	9.9	4.9
7	34.9	23.9	17.0	10.9	5.4
8	36.3	24.9	17.6	11.3	5.6
9	37.3	25.5	18.1	11.6	5.7
10	38.2	26.2	18.6	11.9	5.9
11	38.2	26.2	18.6	11.9	5.9
12	38.7	26.5	18.8	12.0	6.0
13	39.3	26.9	19.1	12.2	6.1
14	40.3	27.6	19.6	12.5	6.2
15	40.3	27.6	19.6	12.5	6.2
16 – 30	43.6	29.9	21.2	13.5	6.7
31 – 50	49.9	34.2	24.2	15.5	7.7
51 – 75	51.3	35.1	24.9	15.9	7.9
76 – 100	56.3	38.6	27.3	17.5	8.7

C-40KAU (Sub Block)

NDI	C_L (lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	4.7	3.3	2.2	1.0
2	8.6	6.1	3.9	1.9
3	12.6	8.9	5.7	2.8
4	15.2	10.8	7.0	3.4
5	17.2	12.2	7.8	3.8
6	18.8	13.3	8.6	4.2
7	20.6	14.8	9.5	4.7
8	21.8	15.5	9.9	4.9
9	22.5	15.9	10.2	5.0
10	23.1	16.4	10.5	5.2
11	23.1	16.4	10.5	5.2
12	23.4	16.6	10.7	5.2
13	23.9	16.9	10.9	5.3
14	24.5	17.4	11.2	5.5
15	24.5	17.4	11.2	5.5
16 – 30	26.8	19.0	12.2	6.0
31 – 50	31.1	22.1	14.1	7.0
51 – 75	32.1	22.7	14.6	7.2
76 – 100	35.5	25.2	16.1	8.0

Appendix C: Estimation Tables for Metal Loading (Continued)

C-50KAU (Main Block)

NDI	C_L (lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	12.7	7.8	5.5	3.5	1.7
2	19.1	11.6	8.3	5.3	2.6
3	25.7	15.6	11.1	7.1	3.5
4	30.1	18.3	13.0	8.3	4.1
5	33.3	20.3	14.4	9.2	4.6
6	35.9	21.9	15.5	9.9	4.9
7	39.3	23.9	17.0	10.9	5.4
8	40.9	24.9	17.6	11.3	5.6
9	41.9	25.5	18.1	11.6	5.7
10	43.0	26.2	18.6	11.9	5.9
11	43.0	26.2	18.6	11.9	5.9
12	43.5	26.5	18.8	12.0	6.0
13	44.2	26.9	19.1	12.2	6.1
14	45.3	27.6	19.6	12.5	6.2
15	45.3	27.6	19.6	12.5	6.2
16 – 30	49.0	29.9	21.2	13.5	6.7
31 – 50	56.1	34.2	24.2	15.5	7.7
51 – 75	57.7	35.1	24.9	15.9	7.9
76 – 100	63.3	38.6	27.3	17.5	8.7

C-50KAU (Sub Block)

NDI	C_L (lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	4.7	3.3	2.2	1.0
2	8.6	6.1	3.9	1.9
3	12.6	8.9	5.7	2.8
4	15.2	10.8	7.0	3.4
5	17.2	12.2	7.8	3.8
6	18.8	13.3	8.6	4.2
7	20.6	14.8	9.5	4.7
8	21.8	15.5	9.9	4.9
9	22.5	15.9	10.2	5.0
10	23.1	16.4	10.5	5.2
11	23.1	16.4	10.5	5.2
12	23.4	16.6	10.7	5.2
13	23.9	16.9	10.9	5.3
14	24.5	17.4	11.2	5.5
15	24.5	17.4	11.2	5.5
16 – 30	26.8	19.0	12.2	6.0
31 – 50	31.1	22.1	14.1	7.0
51 – 75	32.1	22.7	14.6	7.2
76 – 100	35.5	25.2	16.1	8.0

Appendix C: Estimation Tables for Metal Loading (Continued)

C-75KAU (Main Block)

NDI	C_L (lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	15.2	7.8	5.5	3.5	1.7
2	22.8	11.6	8.3	5.3	2.6
3	30.6	15.6	11.1	7.1	3.5
4	35.9	18.3	13.0	8.3	4.1
5	39.7	20.3	14.4	9.2	4.6
6	42.9	21.9	15.5	9.9	4.9
7	46.9	23.9	17.0	10.9	5.4
8	48.8	24.9	17.6	11.3	5.6
9	50.1	25.5	18.1	11.6	5.7
10	51.4	26.2	18.6	11.9	5.9
11	51.4	26.2	18.6	11.9	5.9
12	52.0	26.5	18.8	12.0	6.0
13	52.8	26.9	19.1	12.2	6.1
14	54.1	27.6	19.6	12.5	6.2
15	54.1	27.6	19.6	12.5	6.2
16 – 30	58.6	29.9	21.2	13.5	6.7
31 – 50	67.0	34.2	24.2	15.5	7.7
51 – 75	68.9	35.1	24.9	15.9	7.9
76 – 100	75.7	38.6	27.3	17.5	8.7

C-75KAU (Sub Block)

NDI	C_L (lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	4.7	3.3	2.2	1.0
2	8.6	6.1	3.9	1.9
3	12.6	8.9	5.7	2.8
4	15.2	10.8	7.0	3.4
5	17.2	12.2	7.8	3.8
6	18.8	13.3	8.6	4.2
7	20.6	14.8	9.5	4.7
8	21.8	15.5	9.9	4.9
9	22.5	15.9	10.2	5.0
10	23.1	16.4	10.5	5.2
11	23.1	16.4	10.5	5.2
12	23.4	16.6	10.7	5.2
13	23.9	16.9	10.9	5.3
14	24.5	17.4	11.2	5.5
15	24.5	17.4	11.2	5.5
16 – 30	26.8	19.0	12.2	6.0
31 – 50	31.1	22.1	14.1	7.0
51 – 75	32.1	22.7	14.6	7.2
76 – 100	35.5	25.2	16.1	8.0

Appendix C: Estimation Tables for Metal Loading (Continued)

C-100KAU (Main Block)

NDI	C_L (lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	17.7	7.8	5.5	3.5	1.7
2	26.5	11.6	8.3	5.3	2.6
3	35.6	15.6	11.1	7.1	3.5
4	41.8	18.3	13.0	8.3	4.1
5	46.2	20.3	14.4	9.2	4.6
6	49.9	21.9	15.5	9.9	4.9
7	54.6	23.9	17.0	10.9	5.4
8	56.8	24.9	17.6	11.3	5.6
9	58.2	25.5	18.1	11.6	5.7
10	59.7	26.2	18.6	11.9	5.9
11	59.7	26.2	18.6	11.9	5.9
12	60.5	26.5	18.8	12.0	6.0
13	61.4	26.9	19.1	12.2	6.1
14	62.9	27.6	19.6	12.5	6.2
15	62.9	27.6	19.6	12.5	6.2
16 – 30	68.1	29.9	21.2	13.5	6.7
31 – 50	77.9	34.2	24.2	15.5	7.7
51 – 75	80.1	35.1	24.9	15.9	7.9
76 – 100	88.0	38.6	27.3	17.5	8.7

C-100KAU (Sub Block)

NDI	C_L (lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	4.7	3.3	2.2	1.0
2	8.6	6.1	3.9	1.9
3	12.6	8.9	5.7	2.8
4	15.2	10.8	7.0	3.4
5	17.2	12.2	7.8	3.8
6	18.8	13.3	8.6	4.2
7	20.6	14.8	9.5	4.7
8	21.8	15.5	9.9	4.9
9	22.5	15.9	10.2	5.0
10	23.1	16.4	10.5	5.2
11	23.1	16.4	10.5	5.2
12	23.4	16.6	10.7	5.2
13	23.9	16.9	10.9	5.3
14	24.5	17.4	11.2	5.5
15	24.5	17.4	11.2	5.5
16 – 30	26.8	19.0	12.2	6.0
31 – 50	31.1	22.1	14.1	7.0
51 – 75	32.1	22.7	14.6	7.2
76 – 100	35.5	25.2	16.1	8.0

Appendix D: AU CMOS Gate Array Available Package Types

Package Name	Package Material	DEVICE NAME							
		C-10KAU	C-15KAU	C-20KAU	C-30KAU	C-40KAU	C-50KAU	C-75KAU	C-100KAU
PGA-64	Ceramic	●	●	●	—	—	—	—	—
PGA-88	Ceramic	●	●	●	—	—	—	—	—
PGA-135	Ceramic	●	●	●	●	●	●	●	●
PGA-179	Ceramic	—	—	●	●	●	●	●	●
PGA-208	Ceramic	—	—	—	●	●	●	●	●
PGA-256	Ceramic	—	—	—	—	●	●	●	●
PGA-299	Ceramic	—	—	—	—	—	o	o	o
PGA-321	Ceramic	—	—	—	—	—	—	o	o
PGA-361	Ceramic	—	—	—	—	—	—	o	o
PGA-401	Ceramic	—	—	—	—	—	—	—	o
QFP-64	Plastic	●	●	●	—	—	—	—	—
QFP-80	Plastic	●	●	●	—	—	—	—	—
QFP-100	Plastic	●	●	●	—	—	—	—	—
QFP-120	Plastic	●	●	●	●	●	—	—	—
QFP-160	Plastic	—	●	●	●	●	—	—	—
PLCC-68	Plastic	●	●	●	—	—	—	—	—
PLCC-84	Plastic	●	●	●	—	—	—	—	—
SDIP-64	Plastic	●	●	●	—	—	—	—	—

Note: ● = Available
o = Under Development
— = Not Available

2

Appendix E: TTL 7400 Function Conversion Table

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7400	Quad 2-input NAND	4 x N2N	4
7401	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7402	Quad 2-input NOR	4 x R2N	4
7403	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7404	Hex Inverter	6 x VIN	6
7405	Hex Inverter, Open Collector Outputs	R6B	5
7406	Hex Inverter/Buffer, Open Collector Outputs	R6B	5
7407	Hex Buffer, Open Collector Outputs	2 x N3N into R2N	5
7408	Quad 2-input AND	4 x N2P	8
7409	Quad 2-input AND, Open Collector Outputs	N8P	6
7410	Triple 3-input NAND	3 x N3N	6
7411	Triple 3-input AND	3 x N3P	9
7412	Triple 3-NAND, Open Collector Outputs	T33	7
7413	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7414	Hex Schmitt Trigger Inverter	6 x I1R	48
7415	Triple 3-input AND, Open Collector Outputs	N8P to N2P	8
7418	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7419	Hex Schmitt Trigger Inverter	6 x I1R	48
7420	Dual 4-input NAND	2 x N4N	4
7421	Dual 4-input AND	2 x N4P	6
7422	Dual 4-input NAND, Open Collector Outputs	2 x N4N + N2P	6
7423	Expanded Dual 4-input NOR with Strobe	R4P to D23 + R4P to R2N	9
7424	Quad Schmitt Trigger 2-input NAND	8 x I2R + 4 x N2N	68
7425	Dual 4-input NOR with Strobe	2 x (R4P + R2N)	8
7426	Quad 2-input NAND, High Voltage Output	4 x N2N	4
7427	Triple 3-input NOR	3 x R3N	6
7428	Quad 2-input NOR Buffer	4 x R2N	4
7430	8-input NAND	N8B	6
7432	Quad 2-input OR	4 x R2P	8
7433	Quad 2-input NOR Buffer, Open Collector Outputs	4 x R2N + N4P	7
7434	Hex Noninverter	6 x B1N	6
7435	Hex Noninverter with Open Collector Outputs	2 x N3N into R2N	5
7437	Quad 2-input NAND Buffer	4 x N2B	12
7438/9	Quad 2-input NAND Buffer, Open Collector Outputs	4 x N2N + N4P	7
7440	Dual 4-input NAND Buffer	2 x N4B (N4N if not power)	8(4)
7442	BCD to Decimal Decoder	4 x V2B + 10 x N4N	24
7443	EX3 to Decimal Decoder	4 x V2B + 10 x N4N	24
7444	4 to 10 Line Decoder	4 x V2B + 10 x N4N	24
7445	BCD to Decimal Decoder/driver (30V)	4 x V2B + 10 x N4N	24
7446	BCD to 7-segment Decoder/Driver (30V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7447	BCD to 7-segment Decoder/Driver (15V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7448	BCD to 7-segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7449	BCD to 7-segment, Open Collector Outputs	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7450	Dual 2-input, 2-wide AOI (One Expandable)	D36 + D24	5
7451	AOI	2 x D24	4
7452	Expandable 4-wide AND-OR	N3N + D36 + V1N into N3N	8
7453	Expandable 4-wide AOI	D36 + D23 into N2P	7
7454	4-wide AOI	2 x N3N + 2 x N2N + N4N + V1N	9
7455	2-wide 4-input AOI	T42	6
7460	Dual 4-input Expander	2 x N4P	6
7461	Triple 3-input Expander	3 x N3P	6
7462	4-wide AND-OR Expander	2 x N3N + 2 x N2N + N4N	8
7464	4-2-3-2 AOI	T54	10
7465	4-2-3-2 AOI (Open Collector)	T54	10

Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7470	AND–gated positive-edge JK FF with Preset and Clear	3 x V1N + 2 x N3N + N2N + R2N + FJD	21
	or:	FD4 + 2 x N2N + R2N + V1N + R2P + D24	17
7471	AND–gated RS M/S FF with Preset and Clear	FD4 + 2 x N3N + 2 x D23 + 2 x V1N	19
	or:	LT1+ 2 x N4N + N2P	10
7472	AND–gated JK M/S FF with Preset and Clear	V1N + 2 x N3N + N2N + R2N + FJD	19
	or:	FD4 + N3P + N3N + V1N + D24	17
7473	Dual JK FF with Clear	2 x FJD	24
7474	Dual positive-edge D–FF with Preset and Clear	2 x FDP	16
7475	4–bit Bistable Latch	LTM	16
7476	Dual JK FF with Preset and Clear	2 x (FJD + N2N + R2N + V1N)	30
7477	4–bit Bistable Latch	LTM	16
7478	Dual JK FF with Preset and Common Clear and Clock	2 x (FJD + N2N + R2N + V1N)	30
7480	Gated Full Adder	A1N	8
7482	2–bit Binary Full Adder	A2N	16
7483	4–bit Binary Full Adder with Fast Carry	A4H	48
7484	4–bit Magnitude Comparator	MC4	42
7486	Quad 2-input XOR	4 x X2N	12
7487	4–bit True/Complement Zero/One Element	4 x N2N + V1N + 4 x N2N	17
7489	64–bit (16 x 4) Memory	2 x DE6 + V1N + 16 x LT4 + 5 x (V2B + T5A) + 10 x V2B	298
7490	Decade Counter (Different Implementation)	2 x (FDP + FDO + N2P + N2N + R2N) + V1N 4 x N2P + 2 x R2P + N2N + C41 + LT1	39 41
7491	8–bit Shift Register	2 x FDS + V1N	41
7492	Divide–by–12 Counter	4 x FDO + 2 x V1N + 2 x R2N + N2N	33
7493	4–bit Binary Counter	C41 + N2N (for the resets)	25
7494	4–bit Shift Register, 2 asynchronous Presets 4–bit Shift Register, 2 asynchronous Presets, Full Implementation	FS3 4 x FDP + 4 x D24 + 2 x V1N	34 42
7495	4–bit Parallel-access Shift Register	FS2 + D24 + 2 x V1N	34
7496	5–bit Shift Register	5 x FDP + 5 x N2N + V1N(clock)	46
7497	Synch 6–bit Binary Rate Multiplier	FDR + 2 x FDO + 3 x V1N + 2 x N2N + 2 x N3N + 2 x N4N + 5 x N6B + 3 x N8B + R2B + X2N + 5 x X1B.	122
7498	4–bit Data Selector/Storage Register	FDQ + T2F + 4 x V1N	33
7499	4–bit Universal Shift Register	FS2 + LTK + 2 x D24 + 4 x V1N	42
74100	8–bit Bistable Latch	2 x YL4 + 2 x V1N	30
74101	AO-gated JK Negative-Edge FF, with Preset	FD3 + V1N + 3 x D24	15
74102	AND-gated JK Negative-Edge FF with Preset and Clear	FD4 + D24 + N3P + N3N	16
74103	Dual JK FF with Clear	2 x FJD + 2 x V1N (for clock)	26
	or:	2 x (FD5 + D24 + V1N)	22
74106	Dual JK Negative-Edge FF with Preset and Clear	2 x (FD4 + D24 + V1N)	24
74107	Dual JK FF with Clear	2 x (FJD + 2 x V1N)	22
74108	Dual JK Negative-Edge FF with Preset and Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74109	Dual JK Positive-Edge FF with Preset and Clear	2 x (FDP + V1N + D24)	22
74110	AND-gated JK M/S FF with Data Lockout	FDP + D24 + N3P + N3N	15
74111	Dual JK M/S FF with Data Lockout	2 x (FDP + D24 + V1N)	22
74112	Dual JK Negative-Edge FF with Preset and Clear	2 x (FD4 + D24 + V1N)	24

Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74113	Dual JK Negative-Edge FF with Preset	2 x (FD3 + D24 + V1N)	22
74114	Dual JK Negative-Edge FF with Preset and Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74116	Dual 4–bit Latch with Clear	2 x LTM	32
74120	Dual Pulse Synchronizer/Driver	2 x (N2P + LT1 + 4 x N3N + 2 x N2N + 2 x V1N)	36
74125	Quad Bus Buffer with 3–state Output	B41	9
74126	Quad Bus Buffer with 3–state Output	B41 + 4 x V1N	13
74132	Quad 2–input NAND Schmitt Trigger	4 x (2 x I2R + N2N)	68
74133	13–input NAND	2 x N4N + N3N + N2N into R4P	10
74134	12–input NAND with 3–state Outputs	NCB + O4R	15
74135	Quad 3–input EXOR/EXNOR	4 x X4N	20
74136	Quad 2–input EXOR with Open-Collector Outputs	4 x X2N + R4N	14
74137	3-line to 8–line Decoder with Address Latch	3 x LTK into DE6	42
74138	3-line to 8–line Decoder with Enable	DE6	30
74139	Dual 2-line to 4–line Decoder	2 x DE4	16
74141	BCD–to–Decimal Decoder	4 x V2B + 10 x N4N	24
74145	BCD–to–decimal Decoder	4 x V1N + 10 x N4N	24
74147	10–line to 4–line BCD Priority Encoder	3 x N4N + 3 x N3N + 2 x N2N + 2 x N2P + 3 x R2N + R4N + 13 x V1N	36
74148	8–line to 3–line Octal Priority Encoder	N9B + 2 x N2N + R2P + R4N + 4 x N3N + 2 x N4N + G44 + 12 x V1N	40
74150	1–to–16 Multiplexer	DE3 + 2 x U28 + D24 + 2 x V1N	41
74151	1–to–8 Multiplexer with Strobe	DE3 + U28 + N2N + V1N	28
74152	1–to–8 Multiplexers	DE3 + U28	26
74153	Dual 4–line to 1–line Selector/Multiplexer	DE2 + 2 x U24 + 2 x R2N	19
74154	4–line to 16–line Decoder/Demultiplexer	2 x DE6 + V1N	61
	or:	2 x DE4 + N2P + 16 x R2P	50
74155	Dual 2-line to 4-line Decoder/Demultiplexer (Totem Pole)	8 x N3N + 2 x R2N + 5 x V1N	23
74156	Dual 2-line to 4-line Decoder/Demultiplexer (Open Collector)	8 x N3N + 2 x R2N + 5 x V1N	23
74157	Quad 2-line to 1–line multiplexer	T2F + 4 x R2N + B1N	13
74158	Quad 2-line to 1–line multiplexer (Inverter Data Outputs)	4 x D24 + V1N + 2 x R2N	11
74159	4–line to 16–line Demultiplexer	2 x DE6 + V1N (without open collector)	50
74160	Synchronous 4–bit Counter (Decimal with Direct Clear)	4 x C11 + K1B + 2 x V2B + V1N + B1N+ N2K + 2 x R3N + R4N + 3 x R2N + N2N	62
74161	Synchronous 4–bit Counter (Binary with Direct Clear)	C43	48
74162	Synchronous 4–bit Counter (Decimal with Synchronous Clear)	C45 + D36 + N3P + 2 x R2N + B1N	57
74163	Synchronous 4–bit Counter (Binary with Synchronous Clear)	C45	48
74164	8–bit Parallel Output Serial Shift Register, Asynchronous Clear	2 x FDR + N2P	54
74165	8–bit Shift Register	2 x FDS + 8 x D24 + 11 x V1N + K4B + R2P	71
74166	8–bit Shift Register	2 x FDR + 8 x D24 + 10 x V1N + K4B	80
74168	4–bit Up/Down Synchronous Counter (Decade)	4 x C11 + 4 x T32 + 7 x N2N + 2 x N3N + R2N + 7 x V2B + K1B	85
74169	4–bit Up/Down Synchronous Counter (Binary)	C47	68
74170	4–by–4 Register File	4 x (YL4 + B1N + V1N + U24) + 2 x DE4	104
74171	Quad D–FF with Clear	FDR + 4 x V1N	30
74172	16–bit (8 x 2) Register File	3 x DE6 + 4 x FDS + 16 x (N2N + G34 + + V1N + 2 x R2P + 4 x U28) + 2 x V1N + 2 x R2P	348

Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74173	4–bit D–type Register (3–state Output)	FDR + 2 x R2N + B41 + 6 x V1N + K1B + 4 x D24	53
74174	Hex D–FF (Single Output)	FDR + 2 x FDO	40
74175	Quad D–FF (with Clear)	FDR + 4 x V1N	30
74176	Presettable Decade/Binary Counter	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74177	Presettable Binary Counter	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74178	4–bit Universal Shift Register	FS2	30
74179	4–bit Universal Shift Register (Direct Clear)	FS2 + 9 x N2N + B1N	40
74180	9–bit Odd/Even Parity Checker	PO8 + 2 x D24 + V1N	23
74181	ALU/Function Generator	5 x V1N + 5 x T32 + 4 x D36 + 8 x X2N + 3 x T54 + N6B + N4B + 2 x N2N + 2 x N4P	113
74182	Look–ahead Carry Generator	R4P + 2 x V1N + 2 x T44 + T33 + D24	36
74183	Dual Carry–save Full Adder	2 x A1N	16
74184	BCD–to–binary Code Converter	These devices are ROM based	
74185	Binary–to–BCD Code Converter	These devices are ROM based	
74190	Synch Up/Down Counter (BCD)	4 x FDP + 4 x X2N + K1B + 3 x V1N + 3 x N3N + 9 x N2N + 2 x T32 + T43	
74191	Synch Up/Down Counter (Binary)	C47	68
74192	Up/Down Dual Clock Counter (BCD)	4 x C11 + 4 x V2B + N6B + 2 x N3N + R2N + T32 + T42 + T43	79
74193	Up/Down Dual Clock Counter (Binary)	4 x C11 + 2 x N6B + 4 x V2B + R2N + D24 + T32 + T42	72
74194	4–bit Bidirectional Universal Shift Register	FDR + 6 x V1N + R2N + 4 x D36 + D23 + B1N	48
74195	4–bit Parallel Access Shift Register	FS2 + D24 + 2 x V1N	34
74196	Preset Decade/Binary Counter/Latch	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74197	Preset Binary Counter/Latch	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74198	8–bit Bidirectional Universal Shift Register	2 x FDR + D24 + 10 x V1N + R2N + 8 x D36	89
74199	8–bit Bidirectional Universal Shift Register (JK Serial Input)	2 x FS2 + D24 + 3 x V1N + B1N + R2N + 8 x N2P	83
	or:	2 x FDR + 7 x D24 + T33 + 11 x V1N + R2N	85
74246	BCD–to–7–Segment Decoder/Driver (30V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74247	BCD–to–7–Segment Decoder/Driver (15V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74248	BCD–to–7–Segment Decoder/Driver (Internal Pull–up)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74249	BCD–to–7–Segment Decoder/Driver (Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74260	Dual 5–input NOR	2 x R6B	10
74265	Quad Complementary Output Element	B1N + V1N	
74266	Quad 2–EXNOR, Open Collector	4 x X1N	12
74273	Octal D–type FF with Clear	2 x FDR	52
74276	Quad J–K FF	4 x (FDP + V1N + D24) + 2 x B1N	46
74347	BCD–to–7–Segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53

Appendix F: Alphanumeric Index of Unit Cells

Appendix F: Alphanumeric Index of Unit Cells (Continued)

Appendix F: Alphanumeric Index of Unit Cells (Continued)

Appendix F: Alphanumeric Index of Unit Cells (Continued)

Appendix F: Alphanumeric Index of Unit Cells (Continued)

Appendix F: Alphanumeric Index of Unit Cells (Continued)

Appendix F: Alphanumeric Index of Unit Cells (Continued)

CG21 Series CMOS Gate Array Unit Cell Library

Unit Cell Specification Information

This section contains specifications for all the unit cells available for the CG21 Series CMOS Gate Arrays. The unit cell (gate array) is a functional group of one or more basic cells or gates. A basic cell contains one pair of P-channel and one pair of N-channel transistors (and two pairs of smaller N-channel resistors used for compiled cell construction).

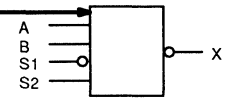
How to Read a Unit Cell Specification

The following paragraphs numbered 1–10 explain how the information given in the CG21 Unit Cell Library is organized. Each of the numbers corresponds to an area of the Unit Cell Library page illustrated on the right.

1. The unit *cell name* appears in the upper left corner of the page.
2. The unit cell *function* is given on the same line as the unit cell name.
3. The *number of basic cells (BC)* or equivalent that make up the unit cell is shown in the upper right corner of the page.
4. *Propagation delay parameters* for the unit cell are given in a table on the upper right side of the page. The basic delay time of the unit cell (t_0) is given in ns. K_{CL}, the delay constant for the cell (delay time per load unit) is given in ns/pF. K_{CL2} and C_{DR2} are a delay constant and an output driving factor used to calculate delay when a unit cell is loaded beyond its published output driving factor (C_{DR}).
5. The *cell symbol* (logic symbol) is shown in the top left box under the cell name.
6. Clock *parameters* (in ns) for unit cells such as flip-flops and counters that make use of clock signals are given in a table directly below the propagation delay parameters.
7. The *input loading factor* of each input of the unit cell are shown in a table directly under the cell symbol box on the left side of the page. The input loading factor is the value of the load placed on a net by the connection of the unit cell input. Unit cell loading factors are shown in load units (lu). The Fujitsu CMOS load unit is the input capacitance of an inverter used for the measurement and calculation of capacitive loads presented to unit cells within the gate array.
8. The *output drive factor* of each output of the unit cell is shown directly under the input loading factor. The output drive factor is the maximum number of load units the unit cell can drive while performing at published specifications.
9. The *function table* (truth table), if applicable, is shown in a box at the lower left side of the page.
10. The unit cell schematic, or *equivalent circuit*, illustrates how discrete components would be connected to perform the unit cell function. It is shown in the lower right corner of the page or on the page following.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		CG21K Version
Cell Name	Function	Number of BC
1 → T2D	2:1 Selector	→ 2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.330	0.069	0.370	0.056			A,B → X
0.357	0.069	0.271	0.056			S → X

Parameter	Symbol	Typ (ns)*

Pin Name	Input Loading Factor (Iu)
A,B	1
S	1

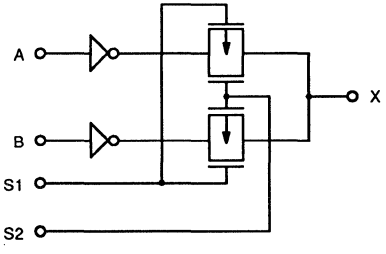
Pin Name	Output Driving Factor (Iu)
X	14

* Minimum values for the typical operating conditon. The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs				Output
A	B	S1	S2	X
L	X	L	H	H
H	X	L	H	L
X	L	H	L	H
X	H	H	L	L
L	H	L	L	INHIBIT
L	H	H	L	INHIBIT
H	L	L	L	INHIBIT
H	L	H	L	INHIBIT

Equivalent Circuit



CG21–T2D–E0 Sheet 1/1 Page 20–17

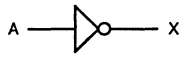
3

Inverter, Buffer Family

Page	Unit Cell Name	Function	Basic Cells
3–7	V1N	Inverter	1
3–8	V2B	Power Inverter	1
3–9	B1N	True Buffer	1
3–10	BD3	Delay Cell	5
3–11	BD4	Delay Cell	4
3–12	BD5	Delay Cell	9
3–13	BD6	Delay Cell	17

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
V1N	Inverter	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.137	0.060	0.203	0.039	0.056	4	A to X

Parameter	Symbol	Typ (ns) *

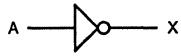
Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
V2B	Power Inverter	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.119	0.032	0.145	0.023	0.039	7	A to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	2

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

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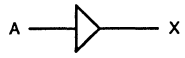
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
B1N	True Buffer	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.310	0.060	0.363	0.039			A to X

Parameter	Symbol	Typ (ns) *

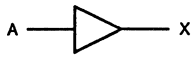
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
BD3	Delay Cell	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.818	0.060	2.488	0.056	0.062	4	A to X

Parameter	Symbol	Typ (ns) *

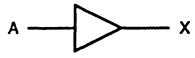
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
BD4	Delay Cell	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.881	0.211	2.165	0.140	0.162	4	A to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	4

Pin Name	Output Driving Factor (lu)
X	6

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
BD5	Delay Cell	9

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
5.769	0.060	5.465	0.045	0.067	4	A to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
BD6	Delay Cell	17

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
11.616	0.064	11.524	0.039	0.062	4	A to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

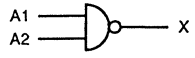
NAND Family

Page	Unit Cell Name	Function	Basic Cells
3–17	N2N	2-input NAND	1
3–18	N2B	Power 2-input NAND	3
3–19	N2K	Power 2-input NAND	2
3–20	N3N	3-input NAND	2
3–21	N3B	Power 3-input NAND	3
3–22	N4N	4-input NAND	2
3–23	N4B	Power 4-input NAND	4
3–24	N6B	Power 6-input NAND	5
3–25	N8B	Power 8-input NAND	6
3–26	N9B	Power 9-input NAND	8
3–27	NCB	Power 12-input NAND	10
3–28	NGB	Power 16-input NAND	11

3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
N2N	2–input NAND	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.179	0.060	0.326	0.062			A to X

Parameter	Symbol	Typ (ns) *

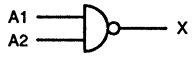
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
N2B	Power 2–input NAND	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.581	0.032	0.753	0.017			A to X

Parameter	Symbol	Typ (ns) *

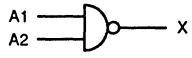
Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
N2K	Power 2–input NAND	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.179	0.032	0.254	0.034	0.039	7	A to X

Parameter	Symbol	Typ (ns) *

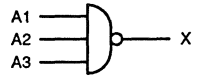
Pin Name	Input Loading Factor (lu)
A	2

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
N3N	3–input NAND	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.250	0.060	0.399	0.084			A to X

Parameter	Symbol	Typ (ns) *

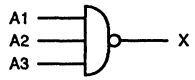
Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
N3B	Power 3–input NAND	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.680	0.032	0.898	0.017			A to X

Parameter	Symbol	Typ (ns) *

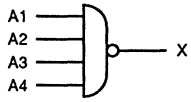
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
N4N	4–input NAND	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.298	0.060	0.428	0.106			A to X

Parameter	Symbol	Typ (ns) *

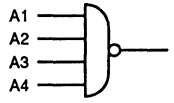
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	10

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
N4B	Power 4–input NAND	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.733	0.032	1.003	0.017			A to X

Parameter	Symbol	Typ (ns) *

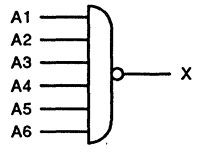
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
N6B	Power 6–input NAND	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.726	0.032	1.069	0.017	0.034	7	A to X

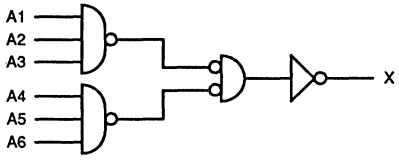
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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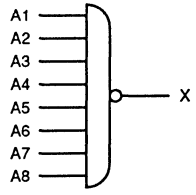
Cell Name	Function	Number of BC
N8B	Power 8–input NAND	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.759	0.032	1.168	0.017	0.034	7	A to X

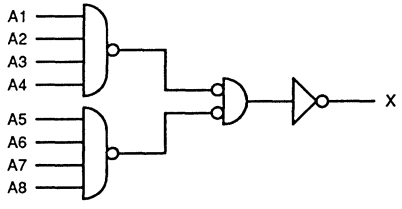
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	36

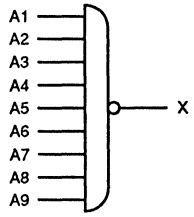
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
N9B	Power 9–input NAND	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.753	0.032	1.406	0.023	0.039	7	A to X

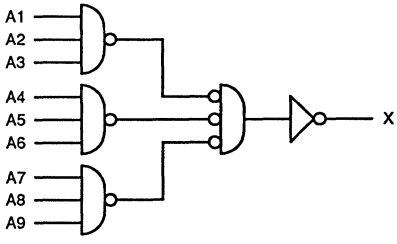
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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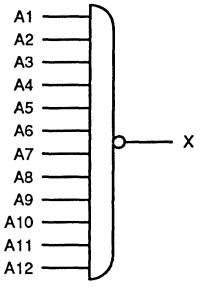
Cell Name	Function	Number of BC
NCB	Power 12–input NAND	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.805	0.032	1.512	0.023	0.039	8	A to X

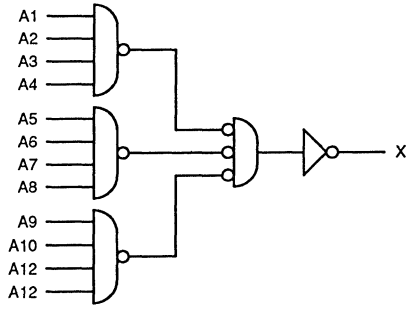
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

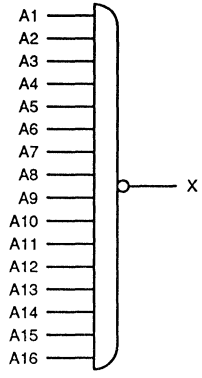
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
NGB	Power 16–input NAND	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.812	0.032	1.835	0.028	0.039	8	A to X

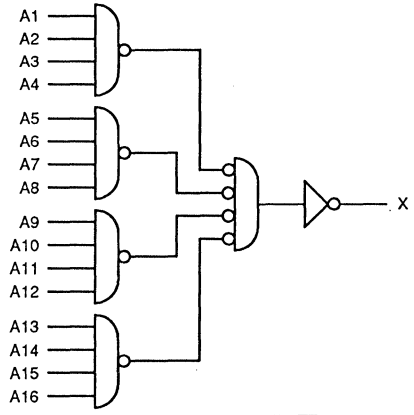
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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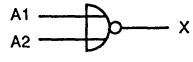
NOR Family

Page	Unit Cell Name	Function	Basic Cells
3–31	R2N	2-input NOR	1
3–32	R2B	Power 2-input NOR	3
3–33	R2K	Power 2-input NOR	2
3–34	R3N	3-input NOR	2
3–35	R3B	Power 3-input NOR	3
3–36	R4N	4-input NOR	2
3–37	R4B	Power 4-input NOR	4
3–38	R6B	Power 6-input NOR	5
3–39	R8B	Power 8-input NOR	6
3–40	R9B	Power 9-input NOR	8
3–41	RCB	Power 12-input NOR	10
3–42	RGB	Power 16-input NOR	11

Cell Name	Function	Number of BC
R2N	2–input NOR	1

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.191	0.106	0.254	0.039	0.050	4	A to X

Parameter	Symbol	Typ (ns) *

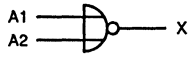
Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R2B	Power 2–input NOR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.720	0.032	0.660	0.017			A to X

Parameter	Symbol	Typ (ns) *

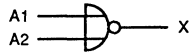
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R2K	Power 2–input NOR	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.214	0.051	0.261	0.028			A to X

Parameter	Symbol	Typ (ns) *

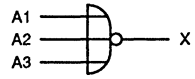
Pin Name	Input Loading Factor (Iu)
A	2

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R3N	3-input NOR	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.399	0.151	0.268	0.039	0.056	4	A to X

Parameter	Symbol	Typ (ns) *

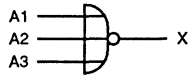
Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	10

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R3B	Power 3–input NOR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.050	0.032	0.726	0.017			A to X

Parameter	Symbol	Typ (ns) *

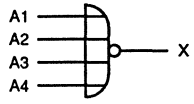
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R4N	4–input NOR	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.589	0.197	0.268	0.039	0.062	4	A to X

Parameter	Symbol	Typ (ns) *

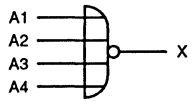
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	6

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
R4B	Power 4–input NOR	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.320	0.032	0.706	0.017			A to X

Parameter	Symbol	Typ (ns) *

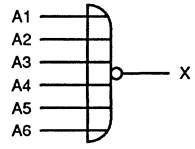
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R6B	Power 6–input NOR	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.188	0.032	0.786	0.017			A to X

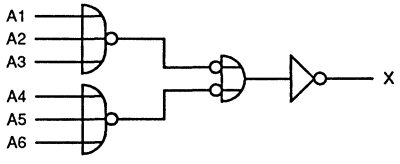
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	36

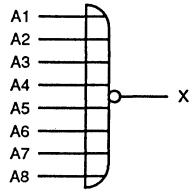
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



Cell Name	Function	Number of BC
R8B	Power 8–input NOR	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.498	0.032	0.799	0.017			A to X

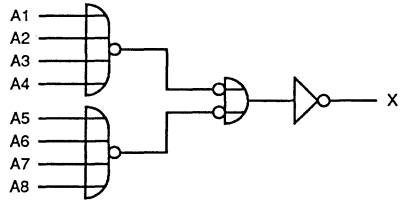
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

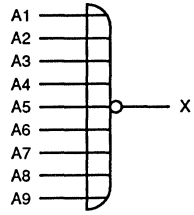
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R9B	Power 9–input NOR	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314	0.032	0.891	0.017			A to X

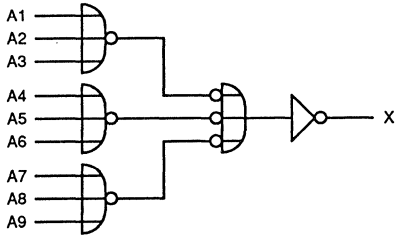
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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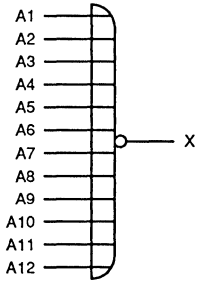
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
RCB	Power 12–input NOR	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.446	0.032	0.924	0.017			A to X

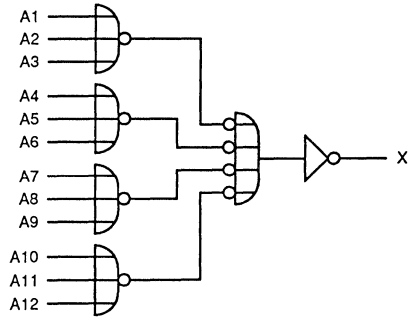
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	36

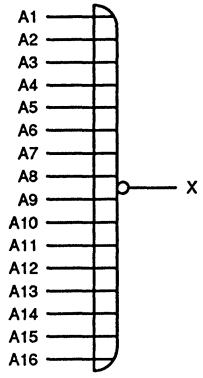
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
RGB	Power 16–input NOR	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.815	0.032	0.964	0.017			A to X

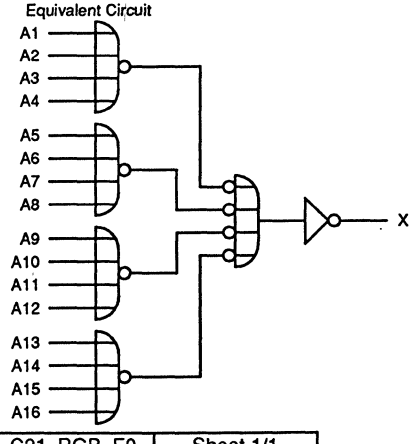
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



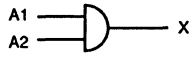
C21–RGB–E0	Sheet 1/1

AND Family

Page	Unit Cell Name	Function	Basic Cells
3–45	N2P	Power 2-input AND	2
3–46	N3P	Power 3-input AND	3
3–47	N4P	Power 4-input AND	3
3–48	N8P	Power 8-input AND	6

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
N2P	Power 2–input AND	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.535	0.032	0.456	0.017	0.028	7	A to X

Parameter	Symbol	Typ (ns) *

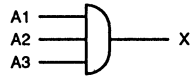
Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
N3P	Power 3–input AND	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.700	0.032	0.568	0.017	0.028	7	A to X

Parameter	Symbol	Typ (ns) *

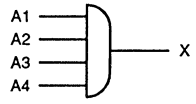
Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
N4P	Power 4–input AND	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.838	0.032	0.627	0.017	0.028	8	A to X

Parameter	Symbol	Typ (ns) *

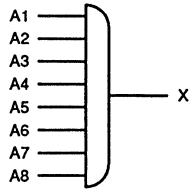
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
N8P	Power 8–input AND	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.911	0.051	0.766	0.017	0.028	8	A to X

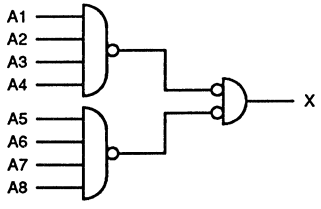
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit

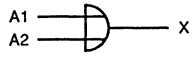


OR Family

Page	Unit Cell Name	Function	Basic Cells
3–51	R2P	Power 2-input OR	2
3–52	R3P	Power 3-input OR	3
3–53	R4P	Power 4-input OR	3
3–54	R8P	Power 8-input OR	6

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R2P	Power 2–input OR	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.416	0.032	0.601	0.023	0.034	8	A to X

Parameter	Symbol	Typ (ns) *

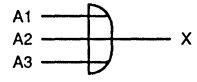
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R3P	Power 3–input OR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.475	0.032	0.970	0.028	0.039	8	A to X

Parameter	Symbol	Typ (ns) *

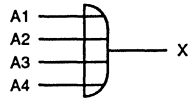
Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
R4P	Power 4–input OR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.475	0.032	1.333	0.034	0.045	8	A to X

Parameter	Symbol	Typ (ns) *

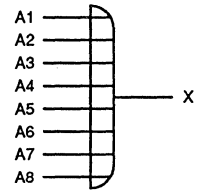
Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
R8P	Power 8–input OR	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.522	0.032	1.419	0.039	0.045	8	A to X

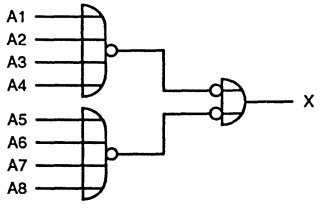
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



C21–R8P–E0	Sheet 1/1

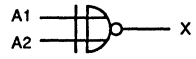
EXNOR/EXOR Family

Page	Unit Cell Name	Function	Basic Cells
3–57	X1N	Exclusive NOR	3
3–58	X1B	Power Exclusive NOR	4
3–59	X2N	Exclusive OR	3
3–60	X2B	Power Exclusive OR	4
3–61	X3N	3-input Exclusive NOR	5
3–62	X3B	Power 3-input Exclusive NOR	6
3–63	X4N	3-input Exclusive OR	5
3–64	X4B	Power 3-input Exclusive OR	6

3

Cell Name	Function	Number of BC
X1N	Exclusive NOR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.614	0.106	0.508	0.062	0.073	4	A to X

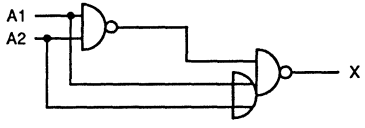
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2

Pin Name	Output Driving Factor (Iu)
X	18

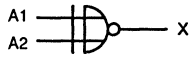
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
X1B	Power Exclusive NOR	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.786	0.032	0.937	0.023	0.039	7	A to X

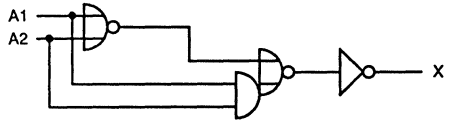
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



C21–X1B–E0	Sheet 1/1

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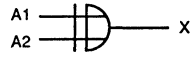
Cell Name	Function	Number of BC
X2N	Exclusive OR	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.588	0.106	0.621	0.062	0.073	4	A to X

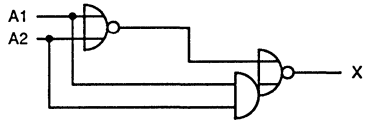
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	2

Pin Name	Output Driving Factor (lu)
X	14

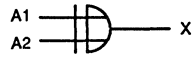
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
X2B	Power Exclusive OR	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.759	0.032	0.865	0.023	0.034	7	A to X

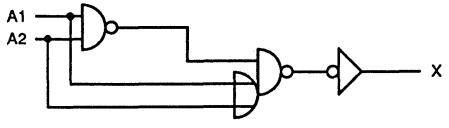
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



C21–X2B–E0	Sheet 1/1

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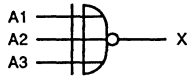
Cell Name	Function	Number of BC
X3N	3–input Exclusive NOR	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.439	0.106	1.228	0.062	0.073	4	A to X

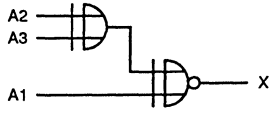
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2

Pin Name	Output Driving Factor (Iu)
X	18

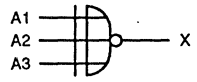
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
X3B	Power 3–input Exclusive NOR	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.393	0.032	1.789	0.023	0.039	7	A to X

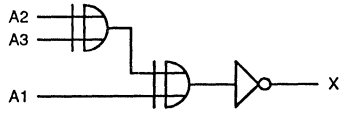
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

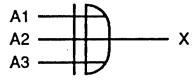
Equivalent Circuit



C21–X3B–E0	Sheet 1/1

Cell Name	Function	Number of BC
X4N	3-input Exclusive OR	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.492	0.106	1.340	0.062	0.073	4	A to X

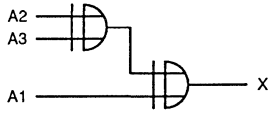
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2

Pin Name	Output Driving Factor (Iu)
X	14

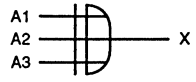
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
X4B	Power 3–input Exclusive OR	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.307	0.032	1.657	0.023	0.034	7	A to X

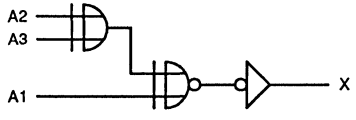
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	2

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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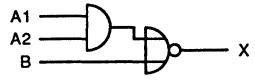
AND–OR–Inverter Family

Page	Unit Cell Name	Function	Basic Cells
3–67	D23	2-wide 2-AND 3-input AOI	2
3–68	D14	2-wide 3-AND 4-input AOI	2
3–69	D24	2-wide 2-AND 4-input AOI	2
3–70	D34	3-wide 2-AND 4-input AOI	2
3–71	D36	3-wide 2-AND 6-input AOI	3
3–72	D44	2-wide 2-OR 2-AND 4-input AOI	2

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
D23	2–wide 2–AND 3–input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.351	0.106	0.399	0.062			A to X
0.179	0.083	0.218	0.039	0.056	4	B to X

Parameter	Symbol	Typ (ns) *

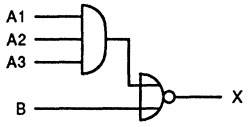
Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
D14	2–wide 3–AND 4–input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.429	0.106	0.406	0.084	0.095	4	A to X
0.155	0.073	0.210	0.039	0.056	4	B to X

Parameter	Symbol	Typ (ns) *

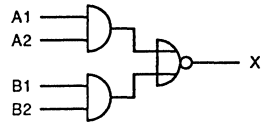
Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
D24	2–wide 2–AND 4–input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.256	0.083	0.363	0.062			A to X
0.322	0.083	0.486	0.062			B to X

Parameter	Symbol	Typ (ns) *

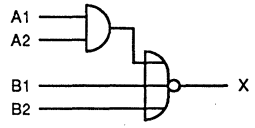
Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
D34	3–wide 2–AND 4–input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.548	0.151	0.428	0.067			A to X
0.298	0.128	0.254	0.039	0.056	4	B to X

Parameter	Symbol	Typ (ns) *

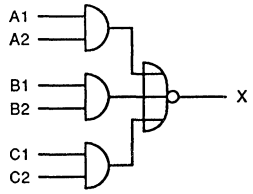
Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	10

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
D36	3–wide 2–AND 6–input AOI	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.369	0.106	0.421	0.062			A to X
0.470	0.106	0.508	0.062			B to X
0.560	0.106	0.595	0.062			C to X

Parameter	Symbol	Typ (ns) *

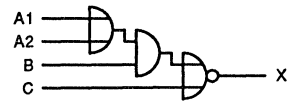
Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (lu)
X	10

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
D44	2–wide 2–OR 2–AND 4–input AOI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.494	0.151	0.457	0.062			A to X
0.494	0.151	0.370	0.062			B to X
0.470	0.106	0.283	0.039	0.050	4	C to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (Iu)
X	10

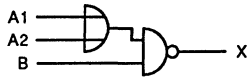
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

OR–AND–Inverter Family

Page	Unit Cell Name	Function	Basic Cells
3–75	G23	2-wide 2-OR 3-input OAI	2
3–76	G14	2-wide 3-OR 4-input OAI	2
3–77	G24	2-wide 2-OR 4-input OAI	2
3–78	G34	3-wide 2-OR 4-input OAI	2
3–79	G44	2-wide 2-AND 2-OR 4-input OAI	2

Cell Name	Function	Number of BC
G23	2–wide 2–OR 3–input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.345	0.106	0.319	0.062			A to X
0.137	0.060	0.319	0.062			B to X

Parameter	Symbol	Typ (ns) *

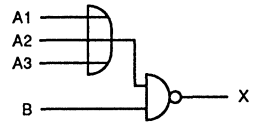
Pin Name	Input Loading Factor (lu)
A	1
B	1

Pin Name	Output Driving Factor (lu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
G14	2–wide 3–OR 4–input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.571	0.156	0.377	0.062			A to X
0.119	0.060	0.377	0.062			B to X

Parameter	Symbol	Typ (ns) *

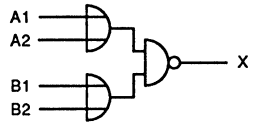
Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	10

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
G24	2–wide 2–OR 4–input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.238	0.106	0.406	0.062			A to X
0.429	0.106	0.348	0.062			B to X

Parameter	Symbol	Typ (ns) *

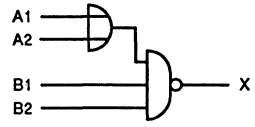
Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	10

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
G34	3–wide 2–OR 4–input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.452	0.106	0.406	0.084			A to X
0.333	0.069	0.261	0.073			B to X

Parameter	Symbol	Typ (ns) *

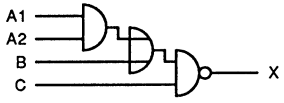
Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	10

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
G44	2–wide 2–AND 2–OR 4–input OAI	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.351	0.106	0.500	0.084			A to X
0.208	0.106	0.363	0.084			B to X
0.238	0.060	0.305	0.062			C to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (lu)
X	14

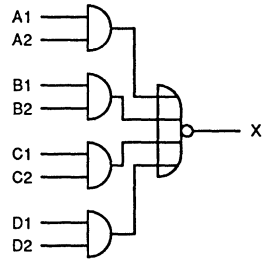
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Multiplexer Family

Page	Unit Cell Name	Function	Basic Cells
3–83	T24	Power 2-AND 4-wide Multiplexer	6
3–84	T26	Power 2-AND 6-wide Multiplexer	10
3–85	T28	Power 2-AND 8-wide Multiplexer	11
3–87	T32	Power 3-AND 2-wide Multiplexer	5
3–88	T33	Power 3-AND 3-wide Multiplexer	7
3–89	T34	Power 3-AND 4-wide Multiplexer	9
3–90	T42	Power 4-AND 2-wide Multiplexer	6
3–91	T43	Power 4-AND 3-wide Multiplexer	10
3–92	T44	Power 4-AND 4-wide Multiplexer	11
3–93	T54	Power 4–3–3–2 AND 4-wide Multiplexer	10
3–94	U24	Power 2-OR 4-wide Multiplexer	6
3–95	U26	Power 2-OR 6-wide Multiplexer	9
3–96	U28	Power 2-OR 8-wide Multiplexer	11
3–97	U32	Power 3-OR 2-wide Multiplexer	5
3–98	U33	Power 3-OR 3-wide Multiplexer	7
3–99	U34	Power 3-OR 4-wide Multiplexer	9
3–100	U42	Power 4-OR 2-wide Multiplexer	6
3–101	U43	Power 4-OR 3-wide Multiplexer	9
3–102	U44	Power 4-OR 4-wide Multiplexer	11

Cell Name	Function	Number of BC
T24	Power 2–AND 4–wide Multiplexer	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.858	0.032	0.805	0.017			A to X
0.951	0.032	0.931	0.017			B to X
0.838	0.032	0.865	0.017			C to X
0.911	0.032	0.997	0.017			D to X

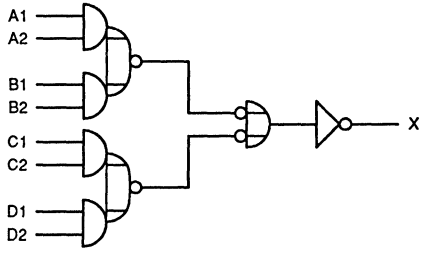
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

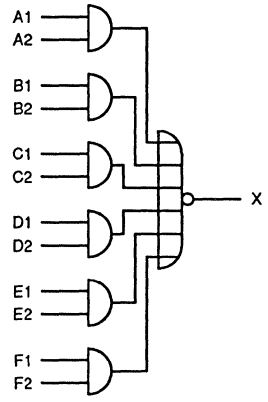
Equivalent Circuit



3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
T26	Power 2–AND 6–wide Multiplexer	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.997	0.032	0.832	0.017			A to X
1.096	0.032	0.957	0.017			B to X
0.997	0.032	0.878	0.017			C to X
1.076	0.032	1.017	0.017			D to X
1.003	0.032	0.970	0.017			E to X
1.089	0.032	1.102	0.017			F to X

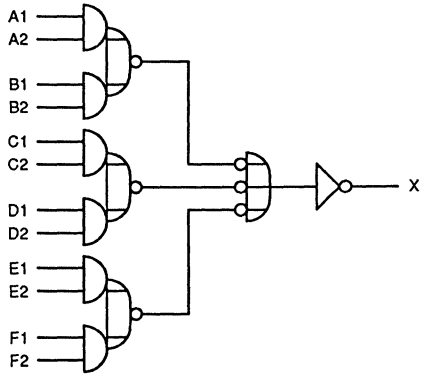
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1
D	1
E	1
F	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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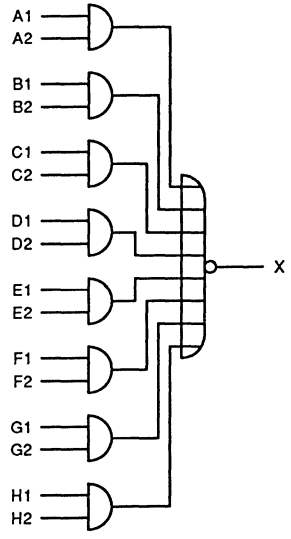
Cell Name	Function	Number of BC
T28	Power 2–AND 8–wide Multiplexer	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.122	0.032	0.805	0.017			A to X
1.228	0.032	0.951	0.017			B to X
1.122	0.032	0.891	0.017			C to X
1.208	0.032	1.036	0.017			D to X
1.162	0.032	1.142	0.017			E to X
1.248	0.032	1.102	0.017			F to X
1.162	0.032	1.017	0.017			G to X
1.248	0.032	1.155	0.017			H to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1
B	1
C	1
D	1
E	1
F	1
G	1
H	1

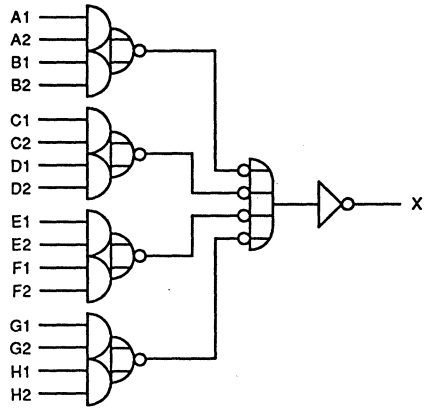
Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name

T28

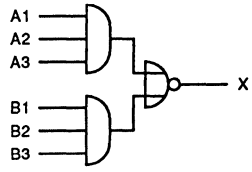
Equivalent Circuit



3

Cell Name	Function	Number of BC
T32	Power 3–AND 2–wide Multiplexer	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.805	0.032	0.891	0.017			A to X
0.805	0.032	0.951	0.017			B to X

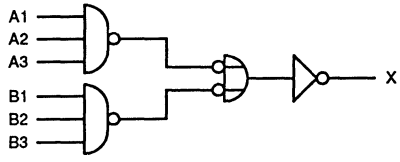
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	36

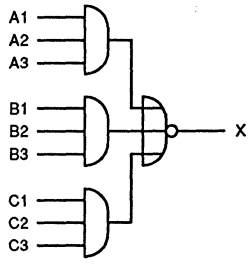
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
T33	Power 3–AND 3–wide Multiplexer	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.924	0.032	0.878	0.017			A to X
0.924	0.032	0.944	0.017			B to X
0.924	0.032	1.030	0.017			C to X

Parameter	Symbol	Typ (ns) *

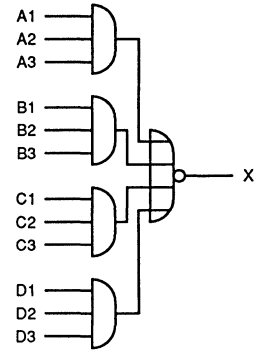
Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
T34	Power 3–AND 4–wide Multiplexer	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.102	0.032	0.911	0.017			A to X
1.102	0.032	0.997	0.017			B to X
1.155	0.032	1.056	0.017			C to X
1.155	0.032	1.063	0.017			D to X

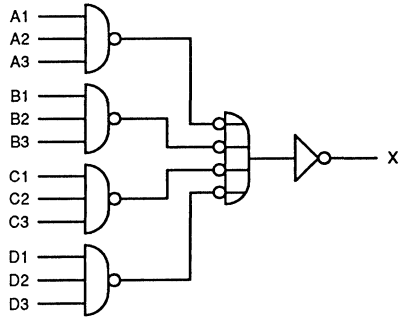
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (lu)
X	36

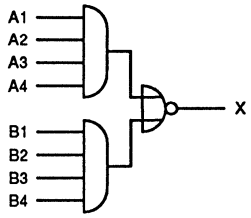
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
T42	Power 4–AND 2–wide Multiplexer	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.845	0.032	0.997	0.017			A to X
0.845	0.032	1.056	0.017			B to X

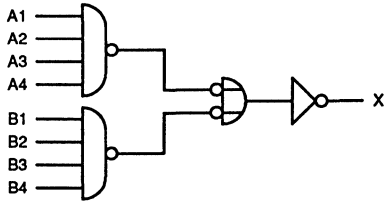
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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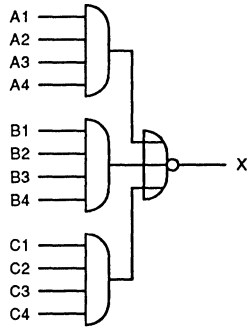
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
T43	Power 4–AND 3–wide Multiplexer	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.997	0.032	1.017	0.017			A to X
0.997	0.032	1.076	0.017			B to X
0.997	0.032	1.162	0.017			C to X

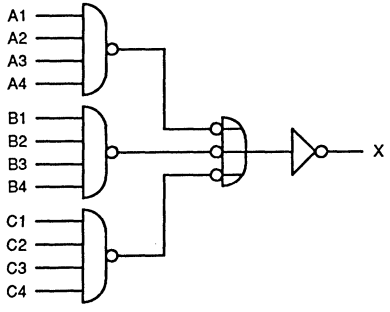
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



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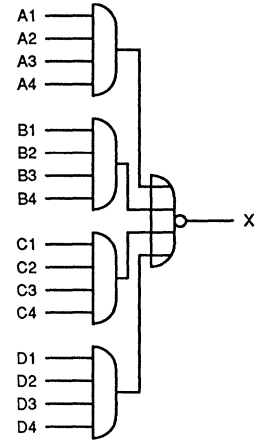
FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
T44	Power 4–AND 4–wide Multiplexer	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.142	0.032	1.017	0.017			A to X
1.142	0.032	0.865	0.017			B to X
1.142	0.032	1.162	0.017			C to X
1.142	0.032	1.228	0.017			D to X

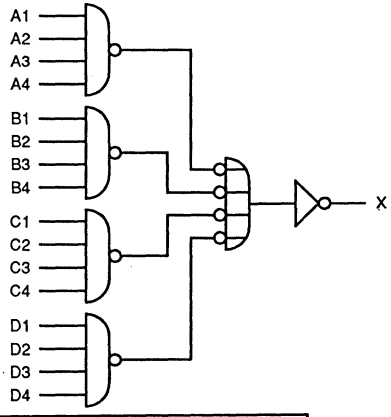
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (lu)
X	36

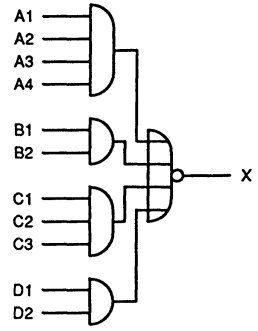
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



Cell Name	Function	Number of BC
T54	Power 4–2–3–2 AND 4–wide Multiplexer	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.089	0.032	1.036	0.017			A to X
1.017	0.032	0.865	0.017			B to X
1.089	0.032	1.089	0.017			C to X
1.017	0.032	0.997	0.017			D to X

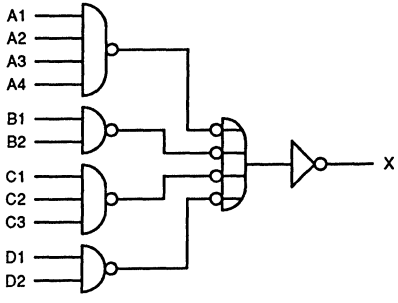
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (lu)
X	36

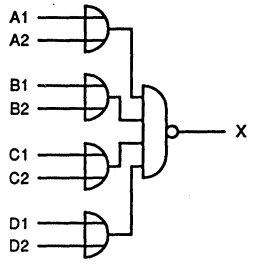
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



Cell Name	Function	Number of BC
U24	Power 2–OR 4–wide Multiplexer	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.056	0.032	0.951	0.023	0.039	7	A to X
0.759	0.032	0.924	0.023	0.039	7	B to X
1.003	0.032	0.944	0.023	0.039	7	C to X
0.733	0.032	0.898	0.023	0.039	7	D to X

Parameter	Symbol	Typ (ns) *

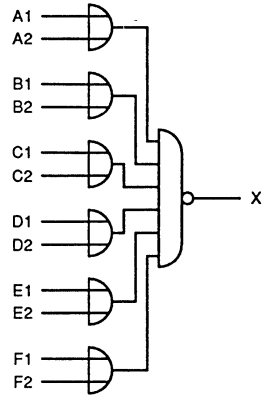
Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
U26	Power 2–OR 6–wide Multiplexer	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
1.056	0.032	1.234	0.023	0.039	7	A to X
0.819	0.032	1.195	0.023	0.039	7	B to X
1.076	0.032	1.267	0.023	0.039	7	C to X
0.838	0.032	1.267	0.023	0.039	7	D to X
0.865	0.032	1.366	0.023	0.039	7	E to X
1.109	0.032	1.366	0.023	0.039	7	F to X

Parameter	Symbol	Typ (ns) *

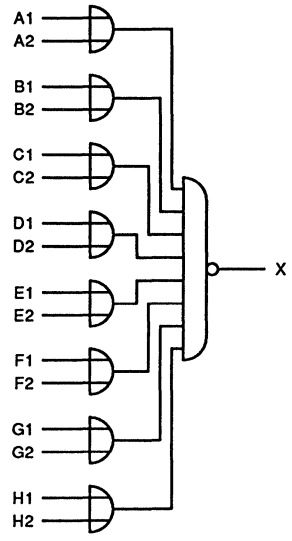
Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1
D	1
E	1
F	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
U28	Power 2–OR 8–wide Multiplexer	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.116	0.032	1.683	0.028	0.045	7	A to X
0.819	0.032	1.657	0.028	0.045	7	B to X
0.799	0.032	1.485	0.028	0.045	7	C to X
1.096	0.032	1.151	0.028	0.045	7	D to X
1.116	0.032	1.657	0.028	0.045	7	E to X
0.819	0.032	1.630	0.028	0.045	7	F to X
0.772	0.032	1.340	0.028	0.045	7	G to X
1.076	0.032	1.393	0.028	0.045	7	H to X

Parameter	Symbol	Typ (ns) *

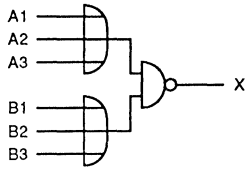
Pin Name	Input Loading Factor (Iu)
A	1
B	1
C	1
D	1
E	1
F	1
G	1
H	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
U32	Power 3–OR 2–wide Multiplexer	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.135	0.032	0.878	0.023	0.039	7	A to X
1.116	0.032	0.865	0.023	0.039	7	B to X

Parameter	Symbol	Typ (ns) *

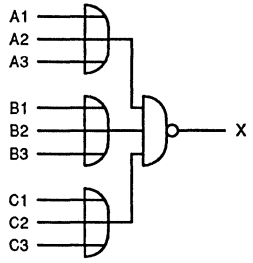
Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
U33	Power 3–OR 3–wide Multiplexer	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.208	0.032	1.208	0.023	0.050	7	A to X
1.188	0.032	1.261	0.023	0.050	7	B to X
1.221	0.032	1.333	0.023	0.045	7	C to X

Parameter	Symbol	Typ (ns) *

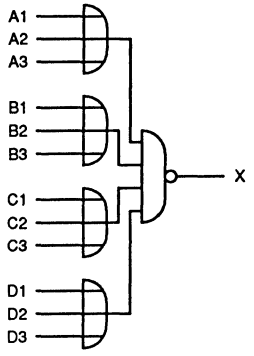
Pin Name	Input Loading Factor (Iu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
U34	Power 3–OR 4–wide Multiplexer	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.116	0.032	1.578	0.028	0.045	7	A to X
1.129	0.032	1.584	0.028	0.045	7	B to X
1.017	0.032	1.287	0.028	0.045	7	C to X
1.116	0.032	1.419	0.028	0.045	7	D to X

Parameter	Symbol	Typ (ns) *

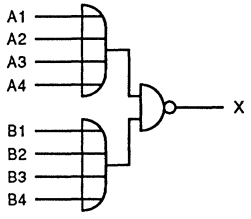
Pin Name	Input Loading Factor (Iu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
U42	Power 4–OR 2–wide Multiplexer	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.373	0.032	0.904	0.023	0.039	7	A to X
1.340	0.032	0.865	0.023	0.039	7	B to X

Parameter	Symbol	Typ (ns) *

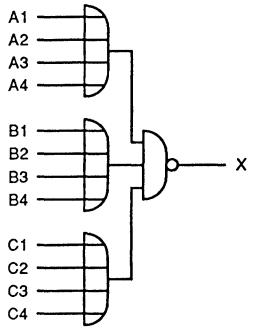
Pin Name	Input Loading Factor (Iu)
A	1
B	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
U43	Power 4–OR 3–wide Multiplexer	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.360	0.032	1.129	0.028	0.039	7	A to X
1.386	0.032	1.195	0.028	0.039	7	B to X
1.426	0.032	1.261	0.028	0.039	7	C to X

Parameter	Symbol	Typ (ns) *

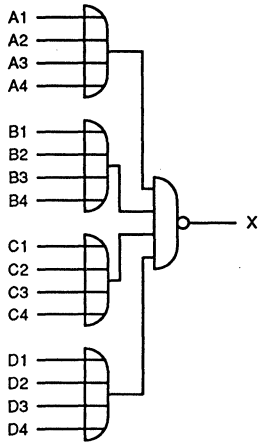
Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
U44	Power 4–OR 4–wide Multiplexer	11

Cell Symbol



Pin Name	Input Loading Factor (lu)
A	1
B	1
C	1
D	1

Pin Name	Output Driving Factor (lu)
X	36

Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
1.446	0.032	1.584	0.023	0.050	7	A to X
1.439	0.032	1.525	0.023	0.050	7	B to X
1.393	0.032	1.287	0.023	0.050	7	C to X
1.413	0.032	1.419	0.023	0.050	7	D to X

Parameter	Symbol	Typ (ns) *

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Clock Buffer Family

Page	Unit Cell Name	Function	Basic Cells
3–105	K1B	True Clock Buffer	2
3–106	K2B	Power Clock Buffer	3
3–107	K3B	Gated Clock (AND) Buffer	2
3–108	K4B	Gated Clock (OR) Buffer	2
3–109	K5B	Gated Clock (NAND) Buffer	3
3–110	KAB	Block Clock (OR) Buffer	3
3–111	KBB	Block Clock (OR x 10) Buffer	30
3–113	KDB	Block Clock (OR x 10) Buffer	32
3–115	KEB	Block Clock Buffer	23
3–117	VIL	Inverting Clock Buffer	2

Cell Name	Function	Number of BC
K1B	True Clock Buffer	2

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.383	0.032	0.456	0.017			A to X

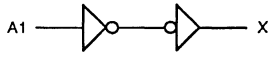
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

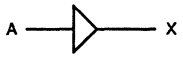
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



Cell Name	Function	Number of BC
K2B	Power Clock Buffer	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561	0.014	0.634	0.017			A to X

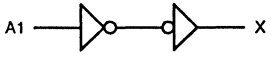
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	55

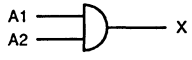
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



Cell Name	Function	Number of BC
K3B	Gated Clock (AND) Buffer	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.528	0.032	0.528	0.017			A to X

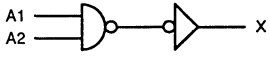
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

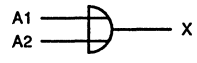
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
K4B	Gated Clock (OR) Buffer	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.416	0.032	0.601	0.023	0.034	8	A to X

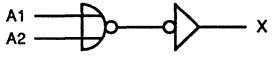
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



C21–K4B–E0	Sheet 1/1

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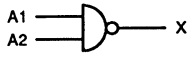
Cell Name	Function	Number of BC
K5B	Gated Clock (NAND) Buffer	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.601	0.032	0.786	0.017			A to X

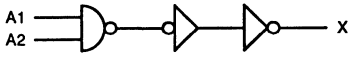
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1

Pin Name	Output Driving Factor (Iu)
X	36

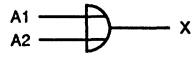
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
KAB	Block Clock (OR) Buffer	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.574	0.014	0.977	0.017			A to X

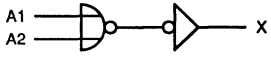
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1

Pin Name	Output Driving Factor (lu)
X	55

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

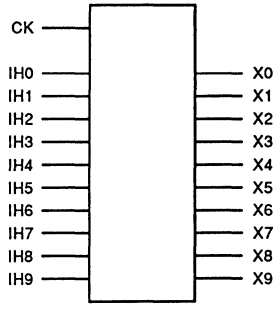
Equivalent Circuit



C21–KAB–E0	Sheet 1/1

Cell Name	Function	Number of BC
KBB	Block Clock Buffer (OR x 10)	30

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.706	0.014	1.102	0.017			CK to X
0.574	0.014	0.977	0.017			IH to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
CK	10
IH	1

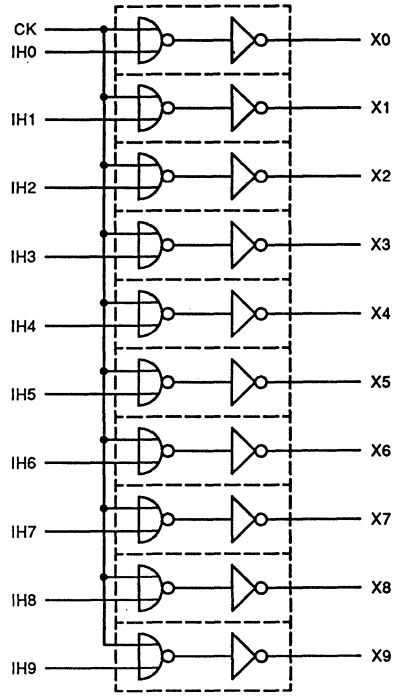
Pin Name	Output Driving Factor (lu)
X	55

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name

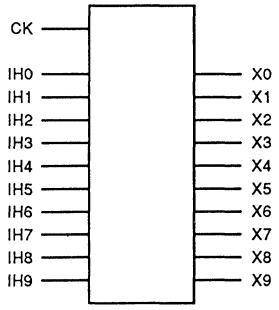
KBB

Equivalent Circuit



Cell Name	Function	Number of BC
KDB	Block Clock Buffer (OR x 10)	32

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.254	0.019	1.848	0.011			CK to X
0.594	0.019	1.221	0.011			IH to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
CK	1
IH	1

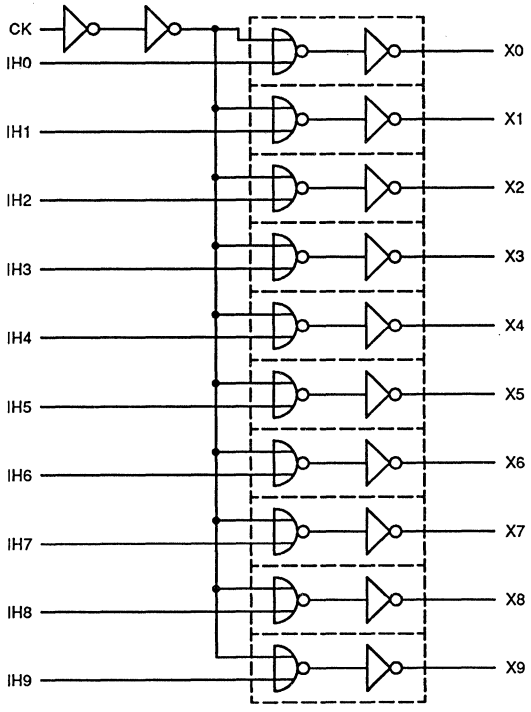
Pin Name	Output Driving Factor (Iu)
X	55

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name

KDB

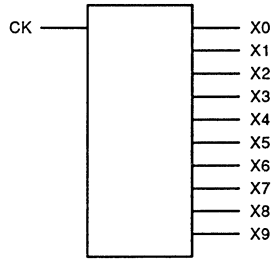
Equivalent Circuit



3

Cell Name	Function	Number of BC
KEB	Block Clock Buffer	23

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.825	0.019	0.911	0.011	0.023	18	CK to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
CK	6

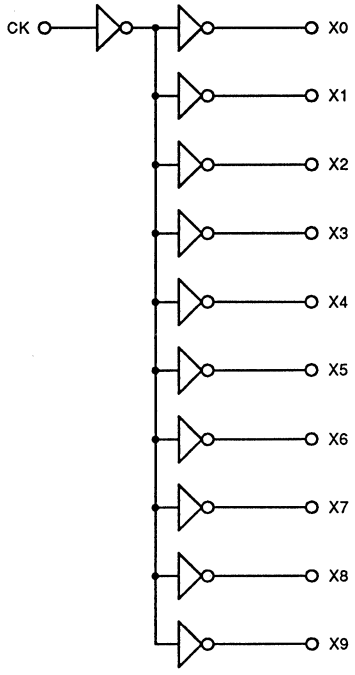
Pin Name	Output Driving Factor (lu)
X	55

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name

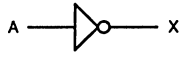
KEB

Equivalent Circuit



Cell Name	Function	Number of BC
V1L	Inverting Clock Buffer	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.167	0.014	0.392	0.017			A to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	4

Pin Name	Output Driving Factor (lu)
X	55

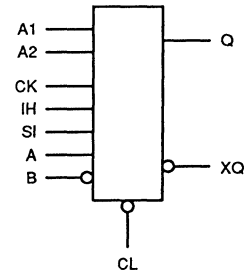
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Scan Flip-flop (Positive Edge Type) Family

Page	Unit Cell Name	Function	Basic Cells
3–121	SDH	Scan 2-input D Flip-flop with Clear and Clock Inhibit	14
3–124	SDJ	Scan 4-input D Flip-flop with Clear and Clock Inhibit	15
3–127	SDK	Scan 6-input D Flip-flop with Clear and Clock Inhibit	16
3–130	SJH	Scan J–K Flip-flop with Clear and Clock Inhibit	16
3–133	SDD	Scan 2-input D Flip-flop with Clear, Preset, and Clock Inhibit	16
3–137	SDA	Scan 1-input D Flip-flop with Clock Inhibit	12
3–140	SDB	Scan 1-input 4-bit D Flip-flop with Clock Inhibit	42
3–144	SHA	Scan 1-input 8-bit D Flip-flop with Clock Inhibit	68
3–147	SHB	Scan 1-input 8-bit D Flip-flop with Clock Inhibit and Q Output	62
3–150	SHC	Scan 1-input 8-bit D Flip-flop with Clock Inhibit and XQ Output	62
3–153	SHJ	Scan 8-bit D Flip-flop with Clock Inhibit and 3-to-1 Data Multiplexer	78
3–156	SHK	Scan 8-bit D Flip-flop with Clock Inhibit and 3-to-1 Data Multiplexer	88
3–159	SFDM	Scan 1-input D Flip-flop with Clock Inhibit	10
3–162	SFDO	Scan 1-input D Flip-flop with Clear and Clock Inhibit	11
3–165	SFDP	Scan 1-input D Flip-flop with Clear, Preset, and Clock Inhibit	12
3–169	SFDR	Scan 4-input D Flip-flop with Clear and Clock Inhibit	36
3–173	SFDS	Scan 4-input D Flip-flop with Clock Inhibit	31
3–177	SFJD	Scan J-K Flip-flop with Clock Inhibit	14

Cell Name	Function	Number of BC
SDH	SCAN 2–input DFF with Clear & Clock–Inhibit	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.967	0.032	1.575	0.017	0.039	7	CK, IH to Q
1.241	0.032	1.135	0.028	0.056	7	CK, IH to XQ
2.000	0.032	0.568	0.017	0.039	7	CL to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	3.2
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	2.2
Data Hold Time	t_{HD}	0.6
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.8
Clear Hold Time	t_{INH}	0.9

Pin Name	Input Loading Factor (lu)
A1, A2	1
CK	1
IH	1
CL	3
SI	1
A, B	2

Pin Name	Output Driving Factor (lu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

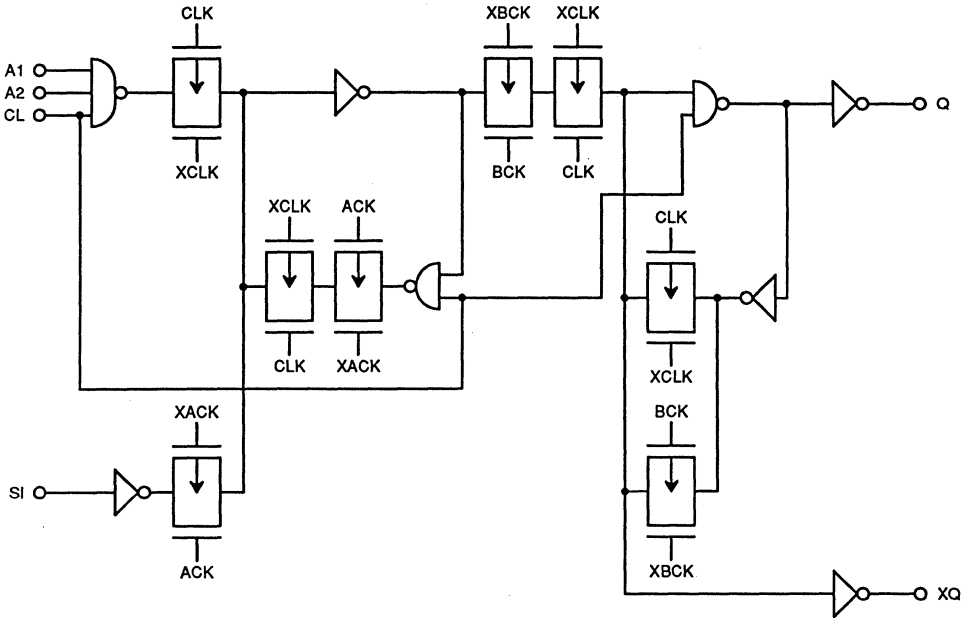
MODE	INPUT						OUTPUT	
	CLK	CL	D	A	B	SI	Q	XQ
CLEAR	X	L	X	X	X	X	L	H
CLOCK	L to X	H	Di	L	L	X	Di	$\overline{Di}$
	H	H	X	L	L	X	Q_0	XQ_0
SCAN	H	H	X	L to H to L	H	Si	Q_0	XQ_0
	H	H	X	L	H to L to H	X	Si	$\overline{Si}$

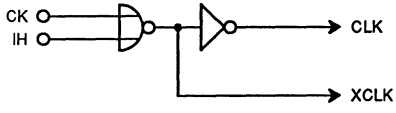
Note : CLK = CK + IH
D = A1 x A2

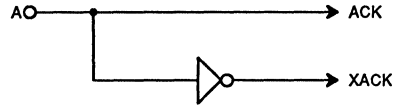
Cell Name

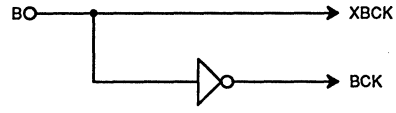
SDH

Equivalent Circuit







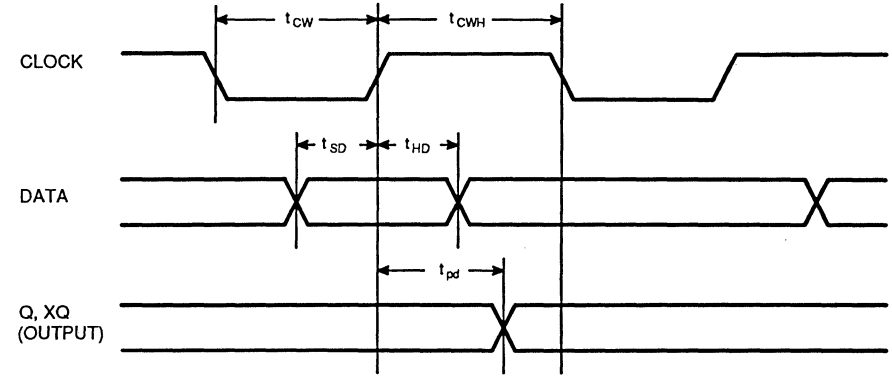


Cell Name

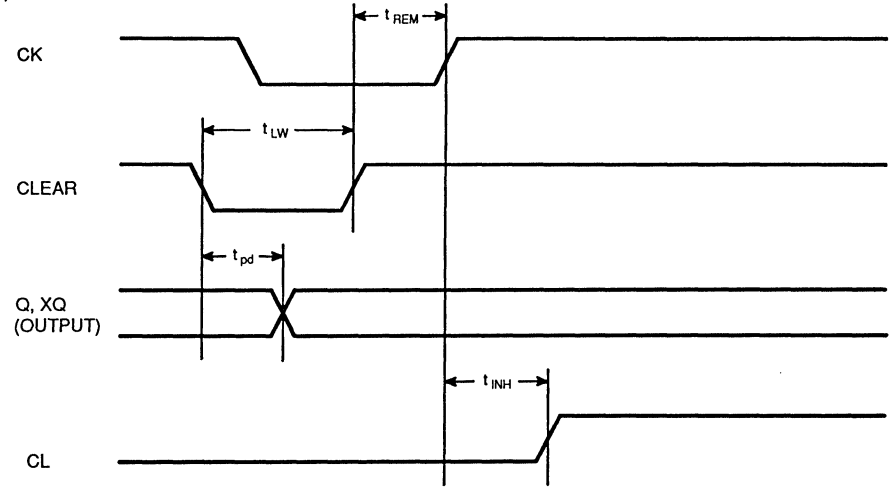
SDH

Definitions of Parameters

i) CLOCK MODE



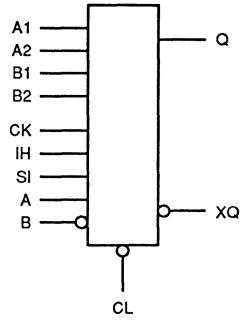
i i) CLEAR MODE



3

Cell Name	Function	Number of BC
SDJ	SCAN 4–input DFF with Clear & Clock–Inhibit	15

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.452	0.032	1.597	0.017	0.039	7	CK, IH to Q
1.248	0.032	1.129	0.028	0.056	7	CK, IH to XQ
1.974	0.032	0.561	0.017	0.039	7	CL to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	3.2
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	2.7
Data Hold Time	t_{HD}	0.5
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.8
Clear Hold Time	t_{INH}	0.9

Pin Name	Input Loading Factor (lu)
A1, A2	1
B1, B2	1
CK	1
IH	1
CL	3
SI	1
A, B	2

Pin Name	Output Driving Factor (lu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

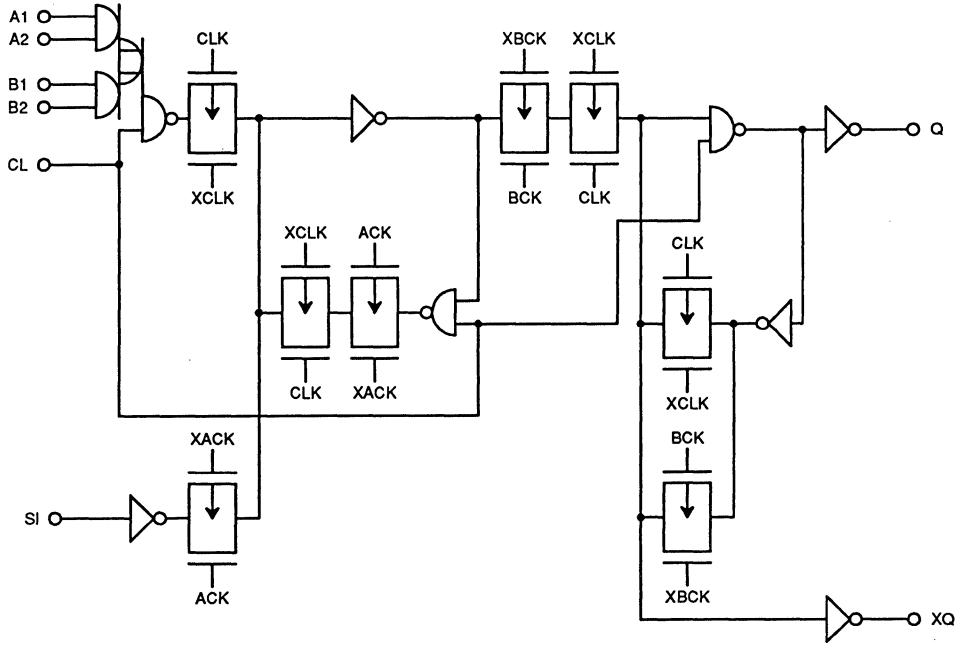
MODE	INPUT						OUTPUT	
	CLK	CL	D	A	B	SI	Q	XQ
CLEAR	X	L	X	X	X	X	L	H
CLOCK	L to H	H	Di	L	L	X	Di	$\overline{Di}$
	H	H	X	L	L	X	Q_0	XQ_0
SCAN	H	H	X	L to H to L	H	Si	Q_0	XQ_0
	H	H	X	L	H to L to H	X	Si	$\overline{Si}$

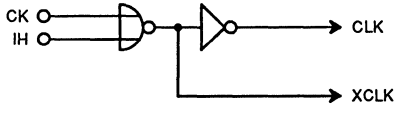
Note : CLK = CK + IH
D = (A1 x A2) + (B1 x B2)

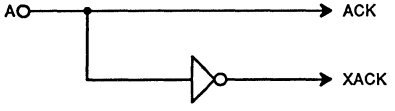
Cell Name

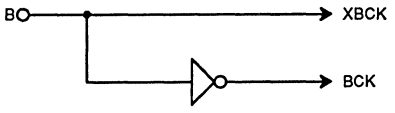
SDJ

Equivalent Circuit









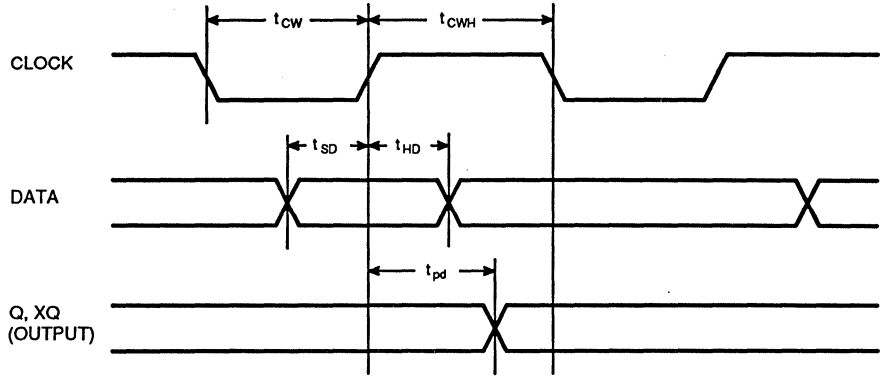
3

Cell Name

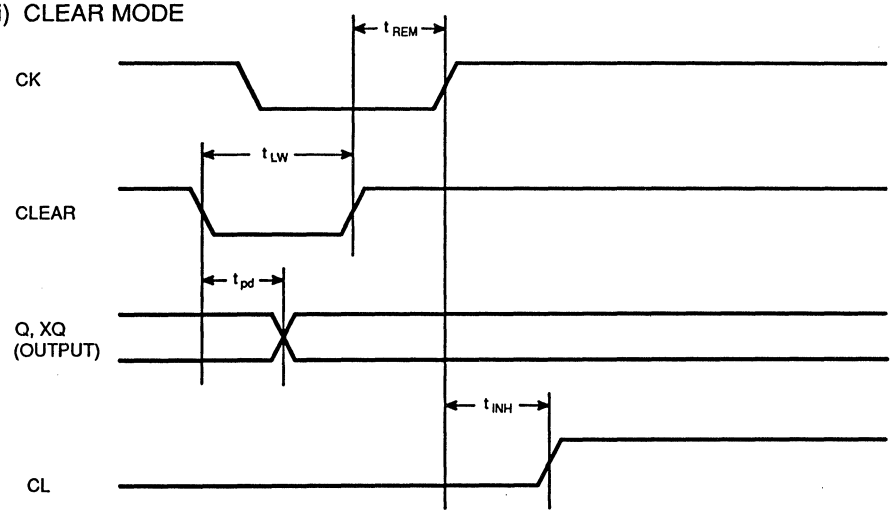
SDJ

Definitions of Parameters

i) CLOCK MODE



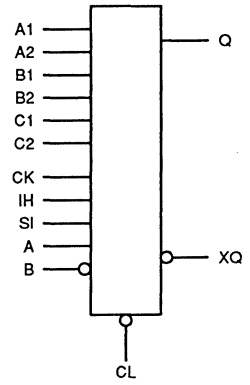
i i) CLEAR MODE



3

Cell Name	Function	Number of BC
SDK	SCAN 6–input DFF with Clear & Clock–Inhibit	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.954	0.032	1.584	0.017	0.039	7	CK, IH to Q
1.228	0.032	1.142	0.028	0.056	7	CK, IH to XQ
1.974	0.032	0.541	0.017	0.039	7	CL to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	3.2
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	2.9
Data Hold Time	t_{HD}	0.3
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.8
Clear Hold Time	t_{INH}	0.9

Pin Name	Input Loading Factor (lu)
A1, A2	1
B1, B2	1
C1, C2	1
CK	1
IH	1
CL	3
SI	1
A, B	2

Pin Name	Output Driving Factor (lu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

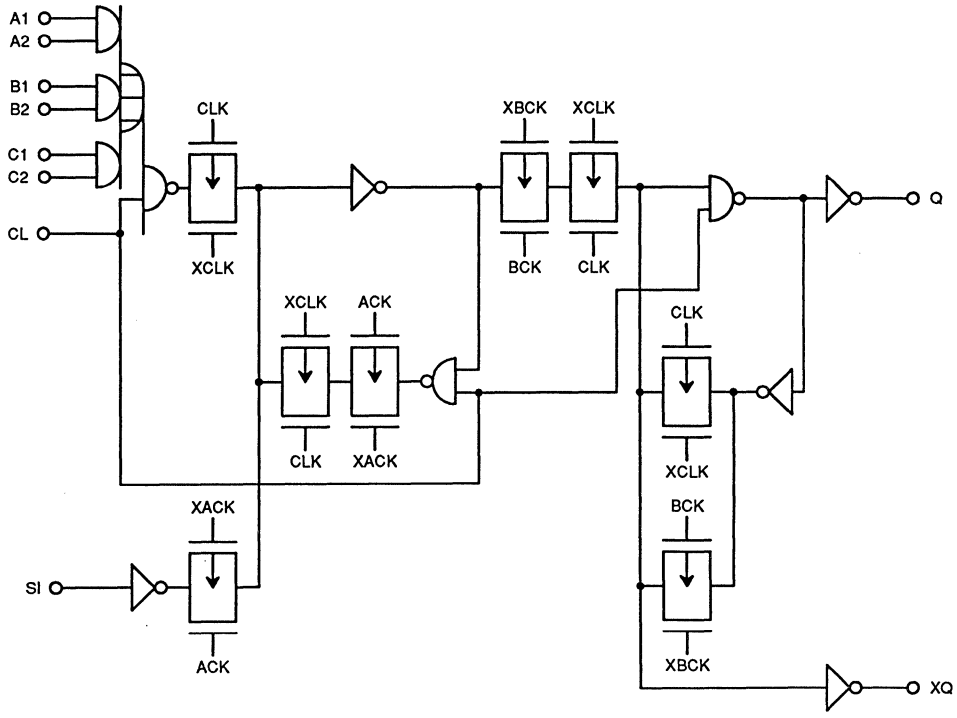
MODE	INPUT						OUTPUT	
	CLK	CL	D	A	B	SI	Q	XQ
CLEAR	X	L	X	X	X	X	L	H
CLOCK	L to H	H	Di	L	L	X	Di	$\overline{Di}$
	H	H	X	L	L	X	Q_0	XQ_0
SCAN	H	H	X	L to H to L	H	Si	Q_0	XQ_0
	H	H	X	L	H to L to H	X	Si	$\overline{Si}$

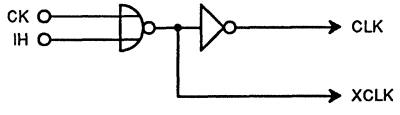
Note : CLK = CK + IH
D = (A1 x A2) + (B1 x B2) + (C1 x C2)

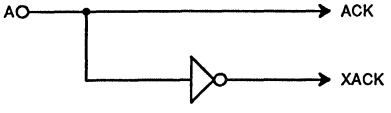
Cell Name

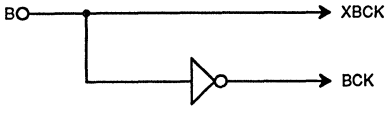
SDK

Equivalent Circuit







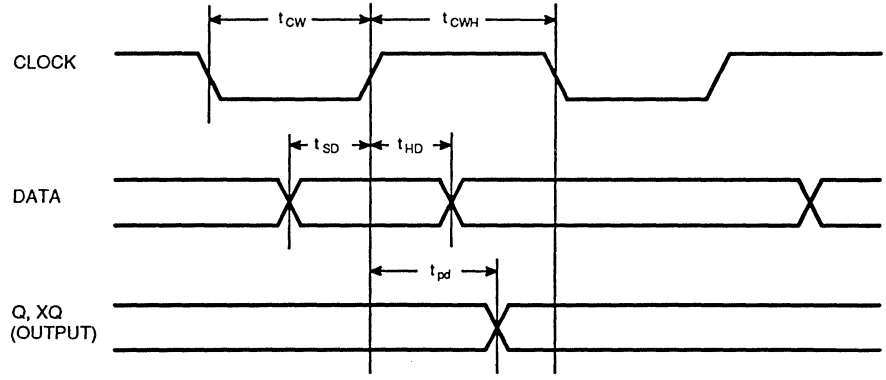


Cell Name

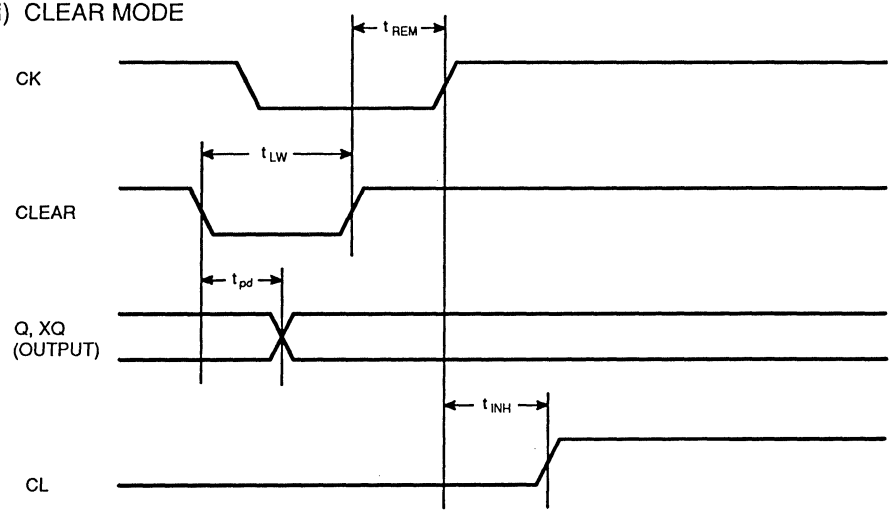
SDK

Definitions of Parameters

i) CLOCK MODE



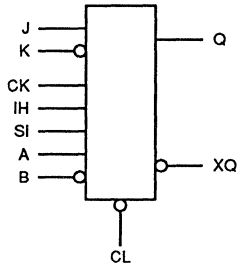
i i) CLEAR MODE



3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"CG21K" Version
Cell Name	**Function**	**Number of BC**
SJH	SCAN J–K FF with Clear & Clock–Inhibit	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.238	0.032	1.782	0.017	0.039	7	CK, IH to Q
1.248	0.032	1.142	0.028	0.056	7	CK, IH to XQ
1.987	0.032	0.733	0.017	0.039	7	CL to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	3.2
Clock Pause Time	t_{CWH}	2.5
Data Setup Time (J)	t_{SD}	2.7
Data Setup Time (K)	t_{SD}	2.9
Data Hold Time (J, K)	t_{HD}	0.3
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.8
Clear Hold Time	t_{INH}	0.9

Pin Name	Input Loading Factor (lu)
J,K	1
CK	1
IH	1
CL	3
SI	1
A, B	2

Pin Name	Output Driving Factor (lu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

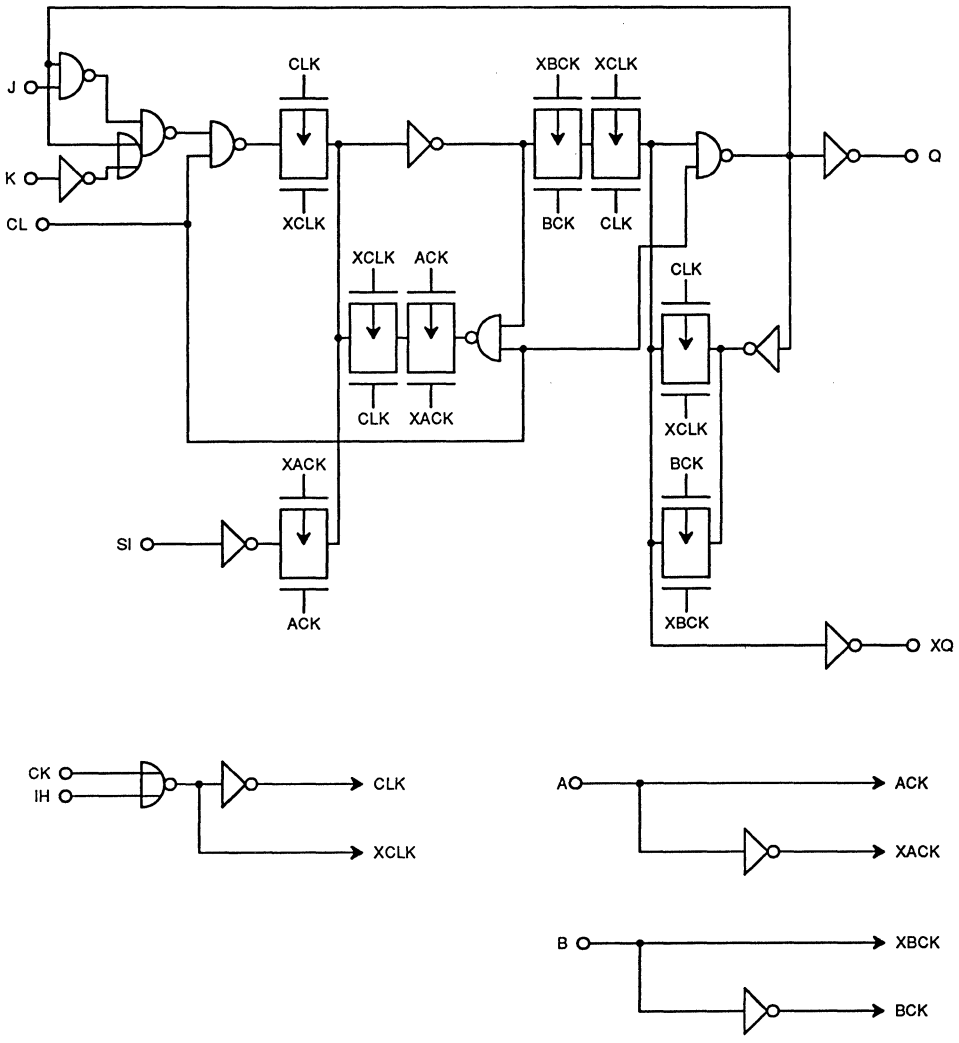
MODE	INPUT							OUTPUT	
	CLK	CL	J	K	A	B	SI	Q	XQ
CLEAR	X	L	X	X	X	X	X	L	H
CLOCK	L to H	H	L	L	L	L	X	L	H
	L to H	H	H	H	L	L	X	H	L
	L to H	H	L	H	L	L	X	Q_0	XQ_0
	L to H	H	H	L	L	L	X	XQ_0	Q_0
	H	H	X	X	L	L	X	Q_0	XQ_0
SCAN	H	H	X	X	L to H to L	H	Si	Q_0	XQ_0
	H	H	X	X	L	H to L to H	X	Si	$\overline{Si}$

Note : CLK = CK + IH

Cell Name

SJH

Equivalent Circuit



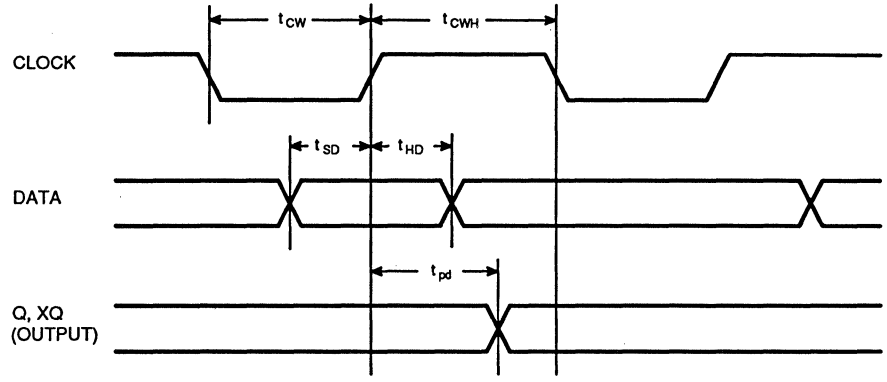
3

Cell Name

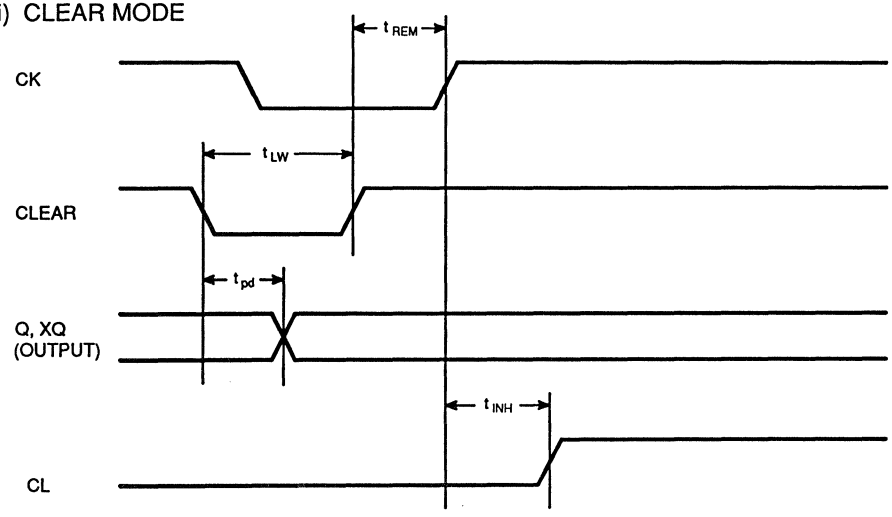
SJH

Definitions of Parameters

i) CLOCK MODE

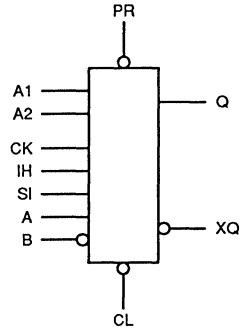


i i) CLEAR MODE



Cell Name	Function	Number of BC
SDD	SCAN 2-input DFF with Clear, Preset & Clock-Inhibit	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.954	0.032	1.703	0.017	0.039	7	CK, IH to Q
1.399	0.032	1.129	0.028	0.056	7	CK, IH to XQ
2.376	0.032	0.541	0.017	0.039	7	CL to Q, XQ
2.026	0.032	1.241	0.028	0.056	7	PR to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	3.2
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	3.2
Data Hold Time	t_{HD}	0.6
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.8
Clear Hold Time	t_{INH}	0.9
Preset Pulse Width	t_{PW}	4.0
Preset Release Time	t_{REM}	2.2
Preset Hold Time	t_{INH}	0.6

Pin Name	Input Loading Factor (lu)
A1, A2	1
CK	1
IH	1
CL	3
PR	3
SI	1
A, B	2

Pin Name	Output Driving Factor (lu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

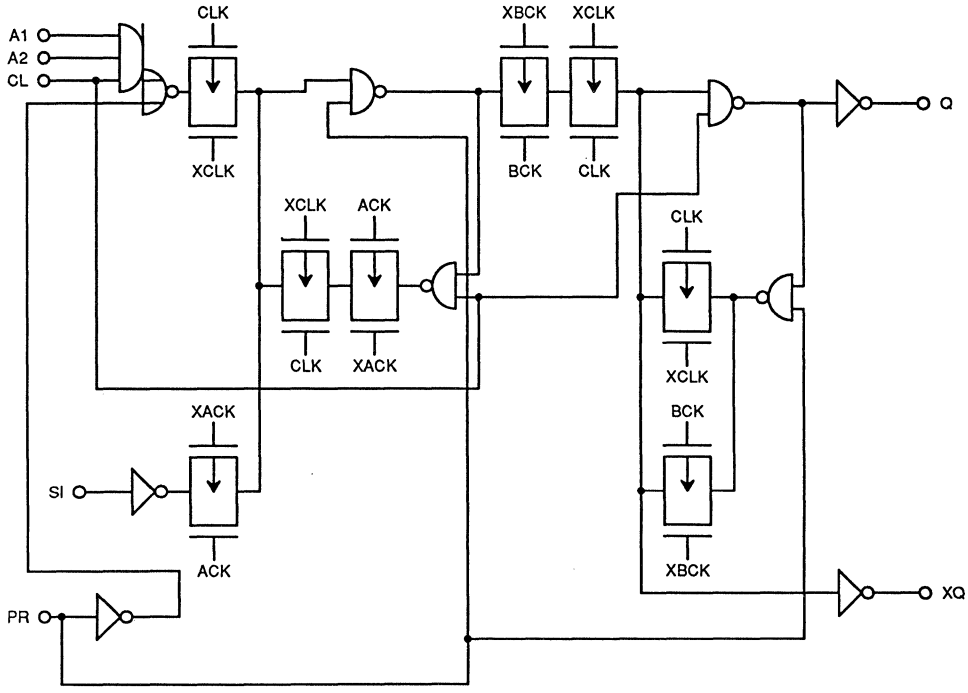
MODE	INPUT							OUTPUT	
	CLK	CL	PR	D	A	B	SI	Q	XQ
CLEAR	X	L	H	X	X	X	X	L	H
PRESET	X	H	L	X	X	X	X	H	L
CLOCK	L to H	H	H	Di	L	L	X	Di	$\overline{Di}$
	H	H	H	X	L	L	X	Q_0	XQ_0
SCAN	H	H	H	X	L to H to L	H	Si	Q_0	XQ_0
	H	H	H	X	L	H to L to H	X	Si	$\overline{Si}$
CL/PR	X	L	L	X	X	X	X	Prohibited	

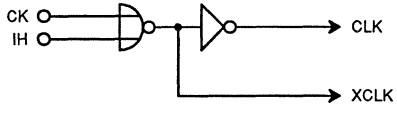
Note : CLK = CK + IH
D = A1 x A2

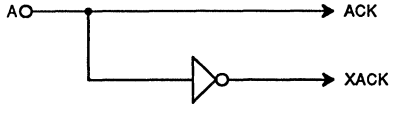
Cell Name

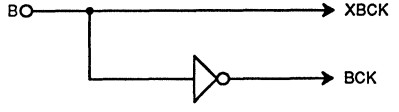
SDD

Equivalent Circuit







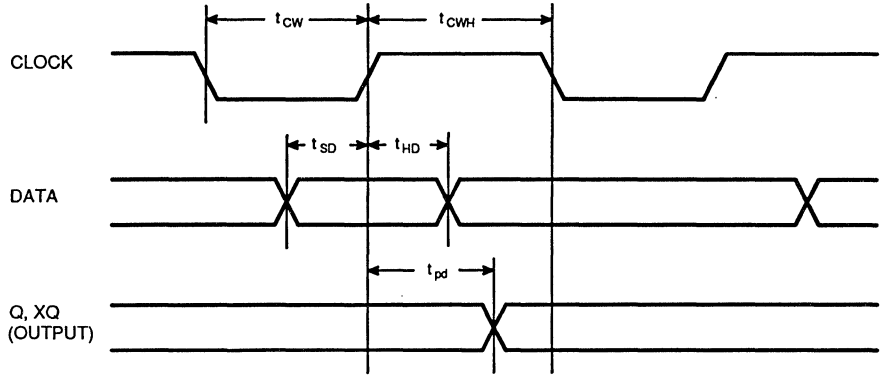


Cell Name

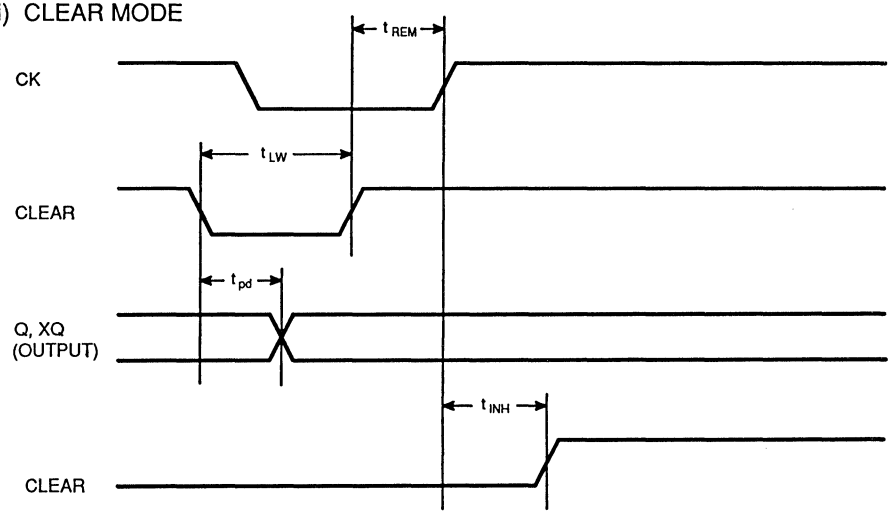
SDD

Definitions of Parameters

i) CLOCK MODE



i i) CLEAR MODE

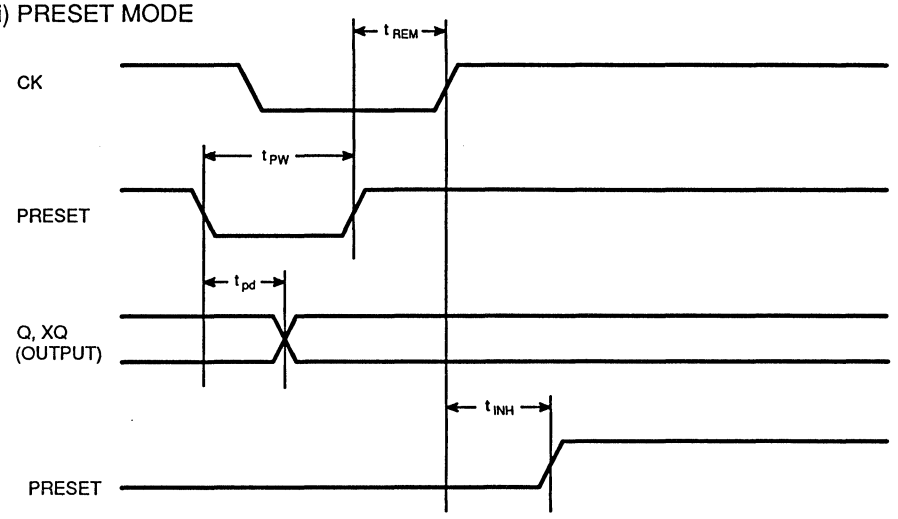


3

Cell Name

SDD

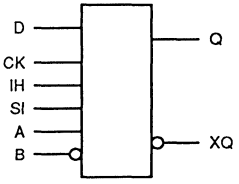
iii) PRESET MODE



3

Cell Name	Function	Number of BC
SDA	SCAN 1–input DFF with Clock–Inhibit	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
1.683	0.032	1.584	0.017	0.039	7	CK, IH to Q
1.234	0.032	1.149	0.028	0.056	7	CK, IH to XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	3.2
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	2.1
Data Hold Time	t_{HD}	0.9

Pin Name	Input Loading Factor (Iu)
D	1
CK	1
IH	1
SI	1
A, B	2

Pin Name	Output Driving Factor (Iu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condltion are given by the maximum delay multiplier.

Function Table

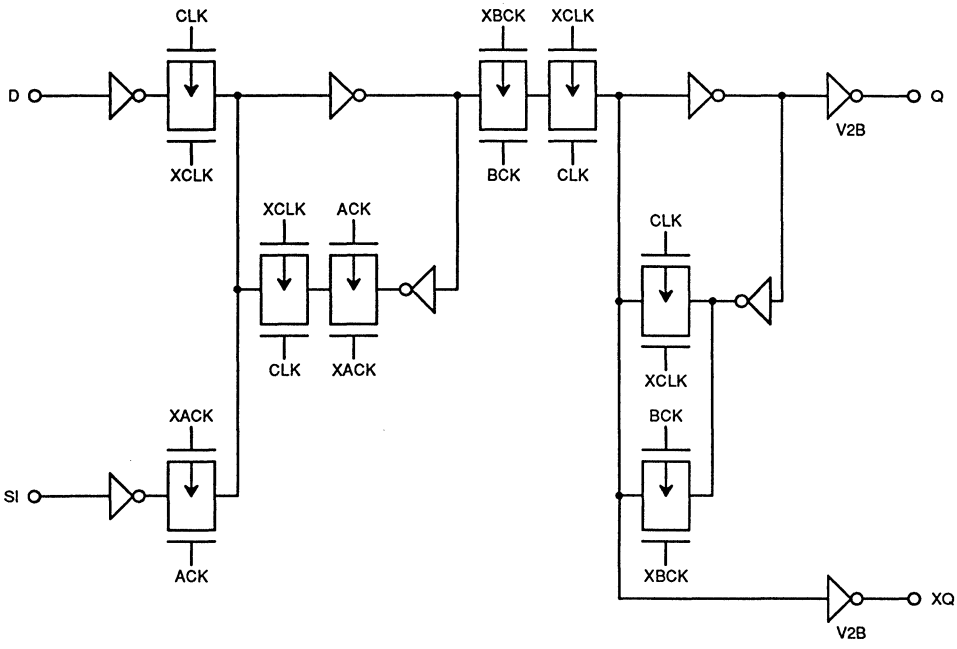
MODE	INPUT					OUTPUT	
	CLK	D	A	B	SI	Q	XQ
CLOCK	L to H	Di	L	L	X	Di	$\overline{Di}$
	H	X	L	L	X	Q_0	XQ_0
SCAN	H	X	L to H to L	H	Si	Q_0	XQ_0
	H	X	L	H to L to H	X	Si	$\overline{Si}$

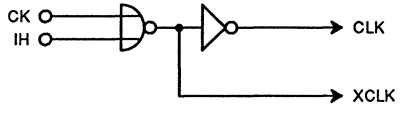
Note : CLK = CK + IH

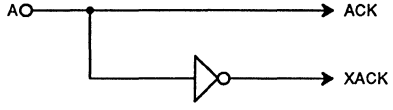
Cell Name

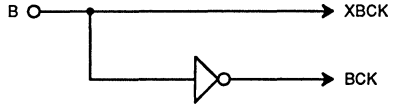
SDA

Equivalent Circuit







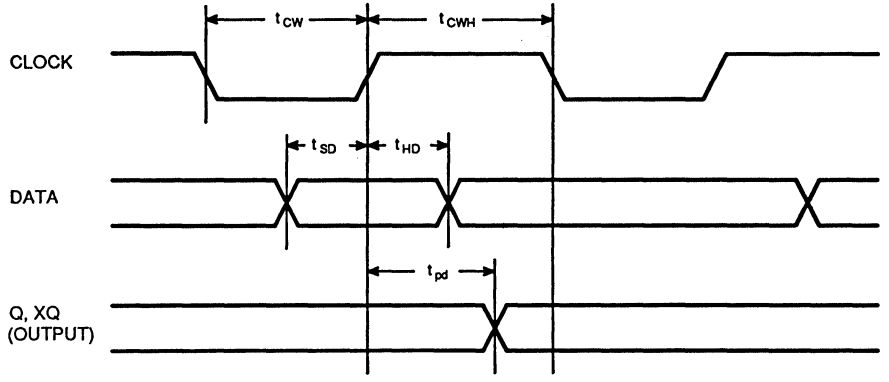


Cell Name

SDA

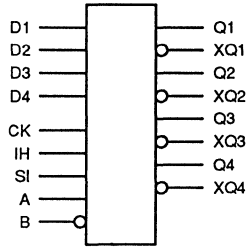
Definitions of Parameters

i) CLOCK MODE



Cell Name	Function	Number of BC
SDB	SCAN 1–input 4– bit DFF with Clock–Inhibit	42

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.238	0.032	2.079	0.017	0.039	7	CK, IH to Q
1.716	0.032	1.756	0.028	0.056	7	CK, IH to XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	4.0
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	1.3
Data Hold Time	t_{HD}	2.0

Pin Name	Input Loading Factor (Iu)
D	1
CK	1
IH	1
SI	1
A, B	2

Pin Name	Output Driving Factor (Iu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

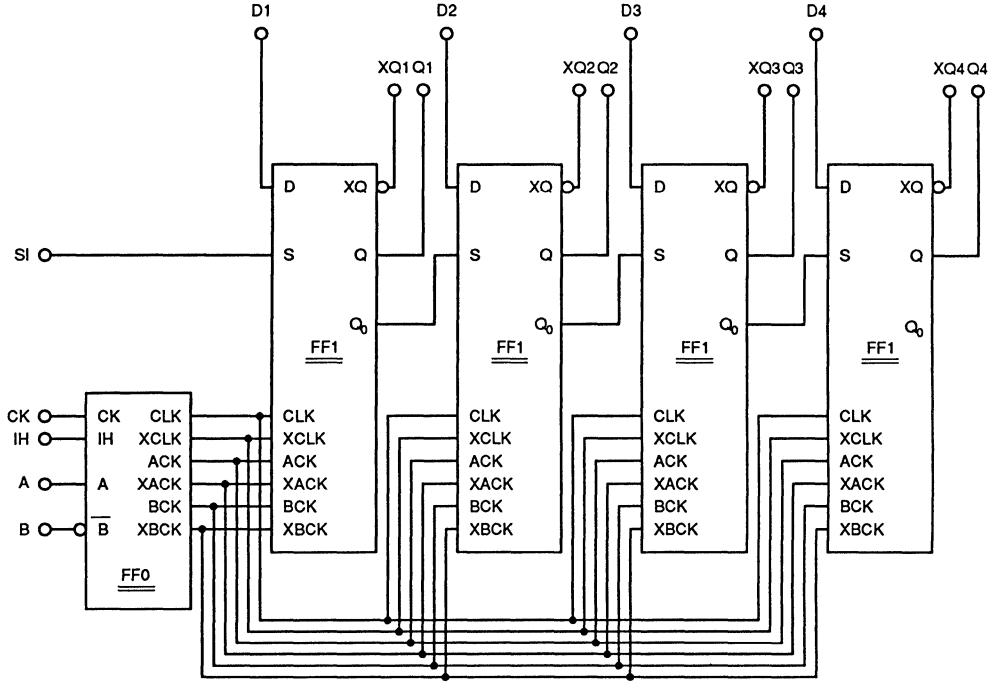
MODE	INPUT					OUTPUT	
	CLK	Dn	A	B	SI, Qn–1	Q	XQn
CLOCK	L to H	Di	L	L	X	Di	$\overline{Di}$
	H	X	L	L	X	Qn_0	XQn_0
SCAN	H	X	L to H to L	H	Si	Qn_0	XQn_0
	H	X	L	H to L to H	X	Si	$\overline{Si}$

Note : CLK = CK + IH
n = 1 ~ 4

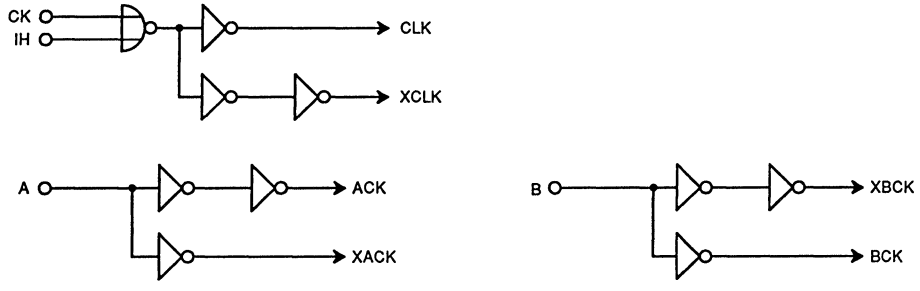
Cell Name

SDB

Equivalent Circuit



Equivalent Circuit (FF0)

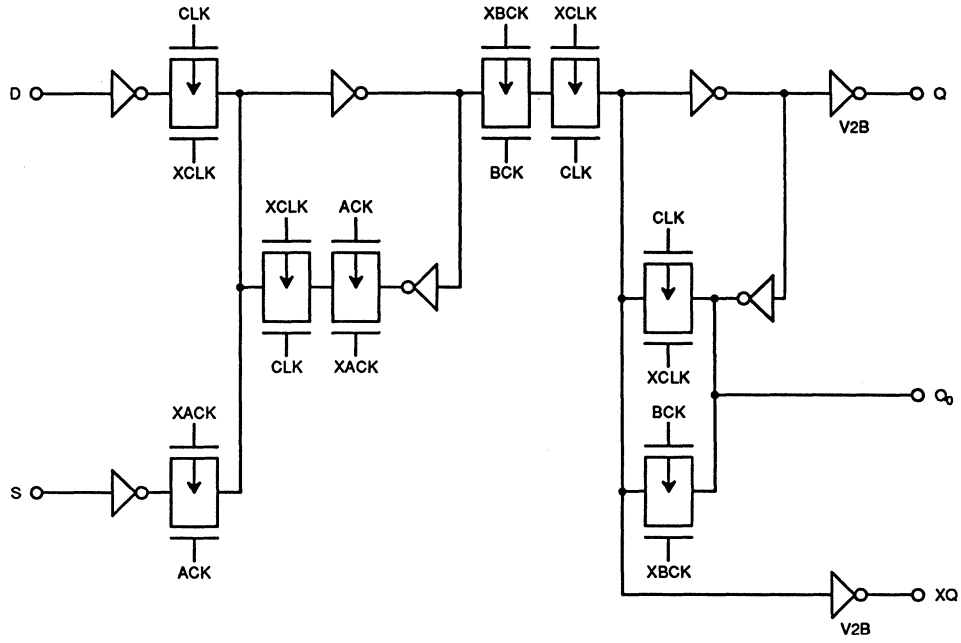


3

Cell Name

SDB

Equivalent Circuit (FF1)



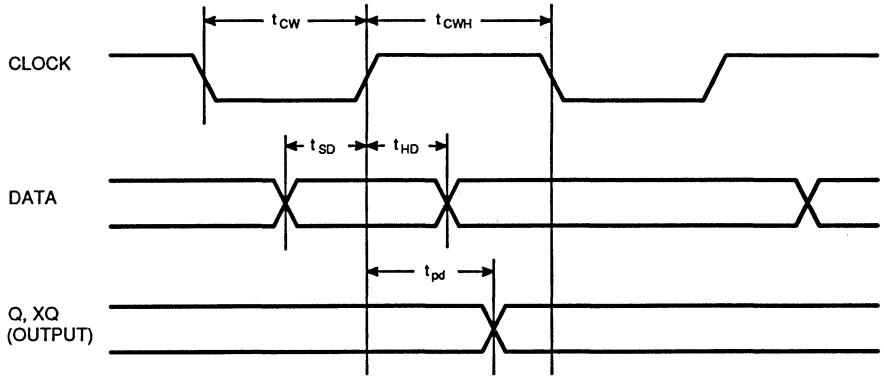
3

Cell Name

SDB

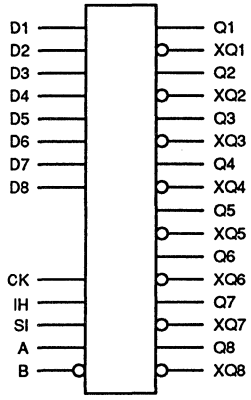
Definitions of Parameters

i) CLOCK MODE



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
SHA	SCAN 1–input 8–bit DFF with Clock–Inhibit	68

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.495	0.060	2.495	0.039	0.045	4	CK, IH to Q
2.178	0.060	2.112	0.062	0.084	4	CK, IH to XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	4.2
Clock Pause Time	t_{CWH}	3.2
Data Setup Time	t_{SD}	1.1
Data Hold Time	t_{HD}	2.0

Pin Name	Input Loading Factor (Iu)
D	1
CK	1
IH	1
SI	1
A	1
B	1

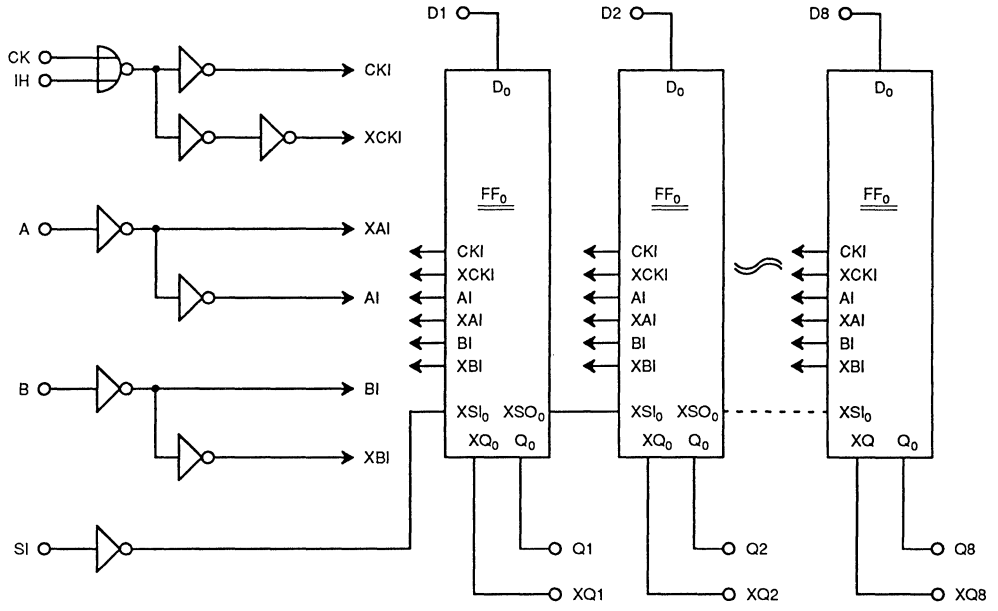
Pin Name	Output Driving Factor (Iu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

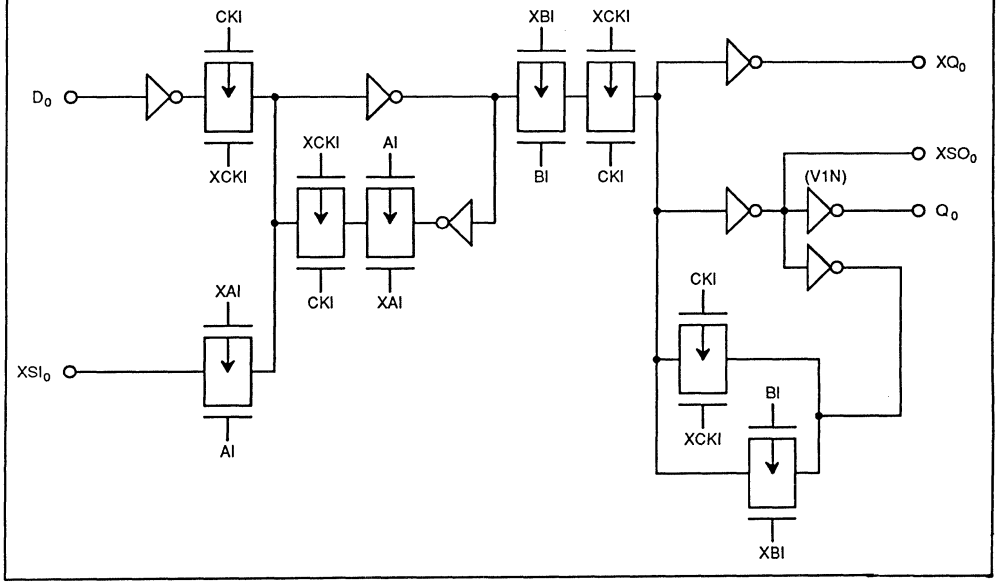
Cell Name

SHA

Equivalent Circuit



Equivalent Circuit (FF0)



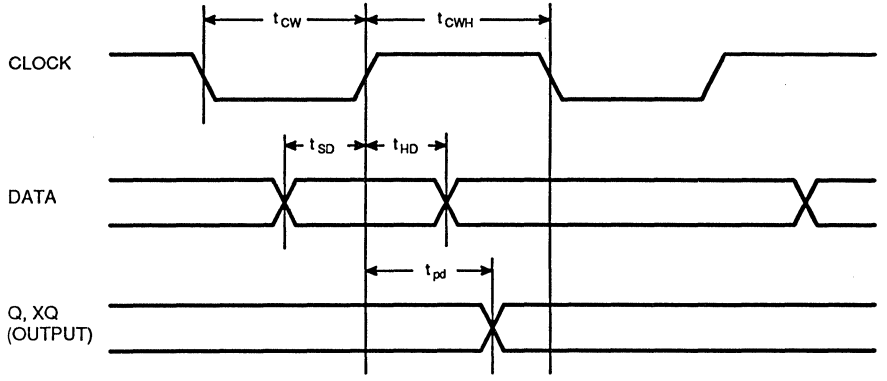
3

Cell Name

SHA

Definitions of Parameters

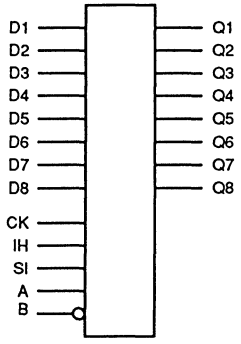
i) CLOCK MODE



3

Cell Name	Function	Number of BC
SHB	SCAN 1–input 8–bit DFF with Clock–Inhibit & Q Output	62

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.284	0.060	2.337	0.039	0.045	4	CK, IH to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	4.2
Clock Pause Time	t_{CWH}	3.2
Data Setup Time	t_{SD}	1.2
Data Hold Time	t_{HD}	2.0

Pin Name	Input Loading Factor (Iu)
D	1
CK	1
IH	1
SI	1
A	1
B	1

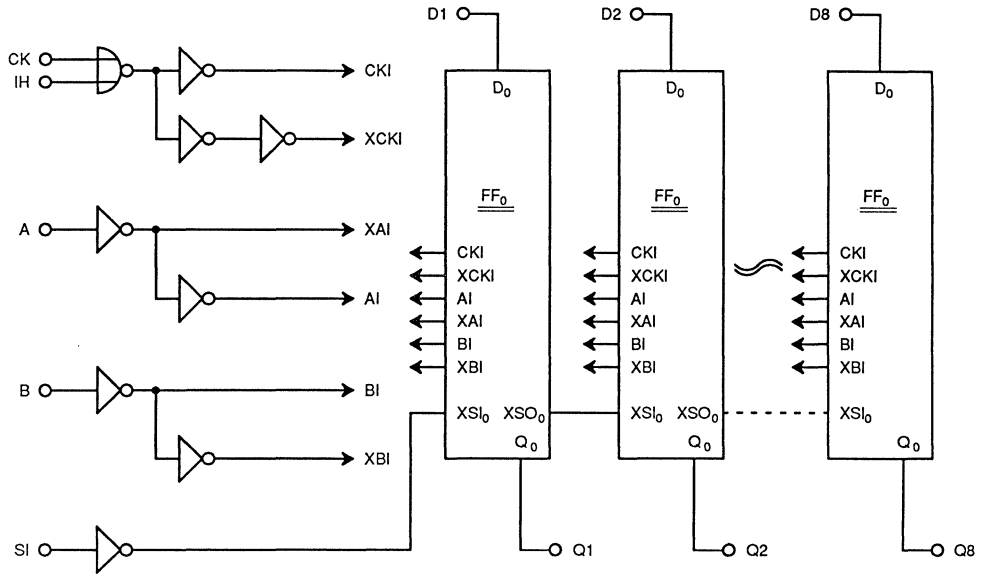
Pin Name	Output Driving Factor (Iu)
Q	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

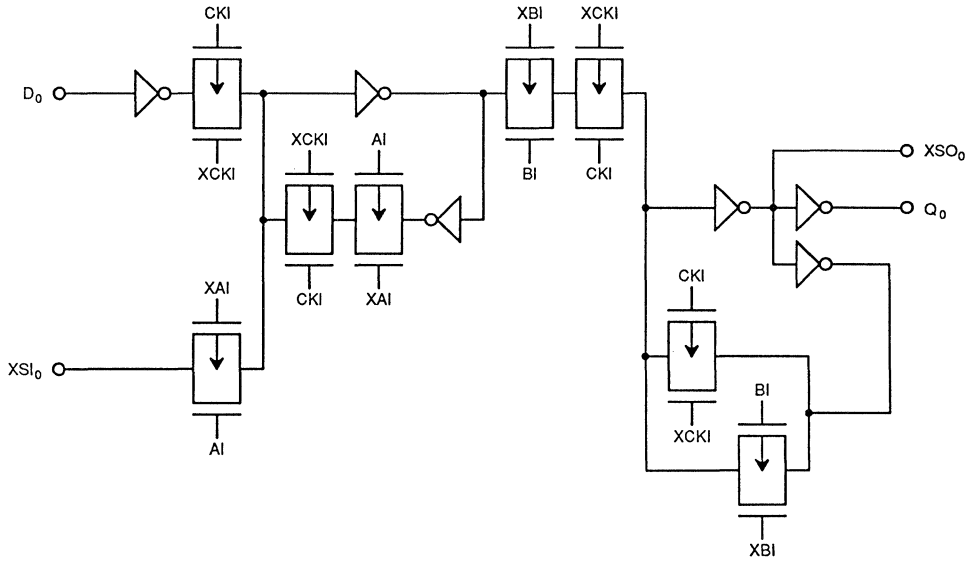
Cell Name

SHB

Equivalent Circuit



Equivalent Circuit (FF0)

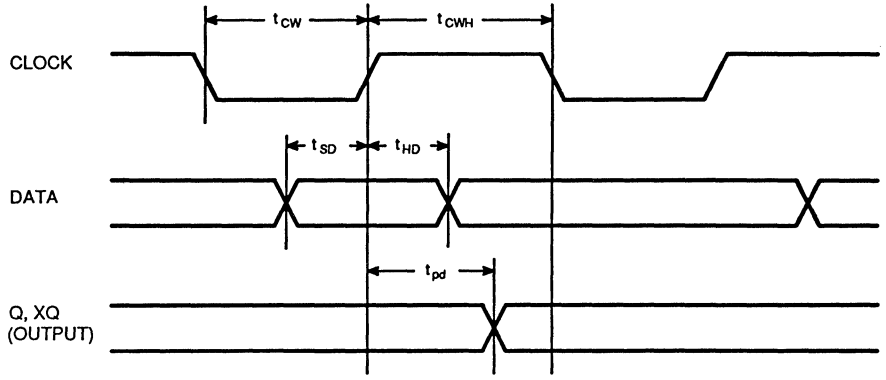


Cell Name

SHB

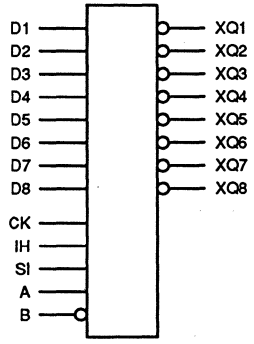
Definitions of Parameters

i) CLOCK MODE



Cell Name	Function	Number of BC
SHC	SCAN 1–input 8–bit DFF with Clock–Inhibit & XQ Output	62

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.211	0.060	2.165	0.062	0.084	4	CK, IH to XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	4.2
Clock Pause Time	t_{CWH}	3.2
Data Setup Time	t_{SD}	1.2
Data Hold Time	t_{HD}	2.0

Pin Name	Input Loading Factor (lu)
D	1
CK	1
IH	1
SI	1
A	1
B	1

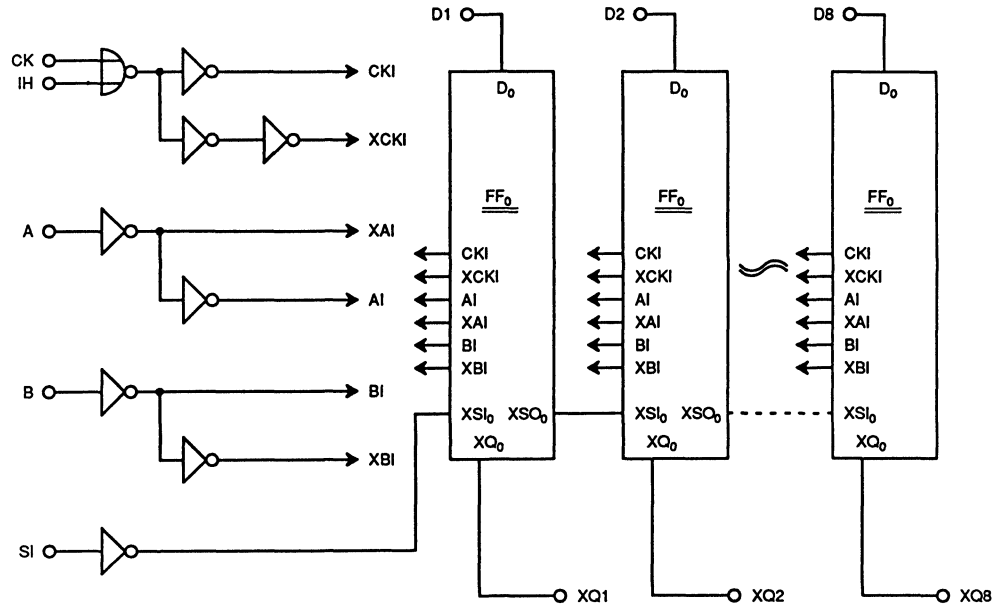
Pin Name	Output Driving Factor (lu)
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

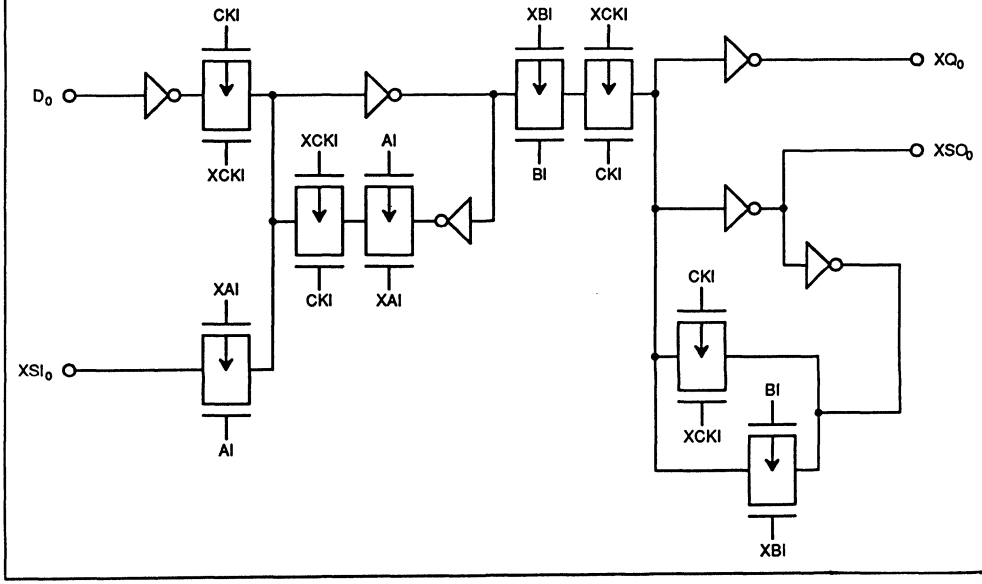
Cell Name

SHC

Equivalent Circuit



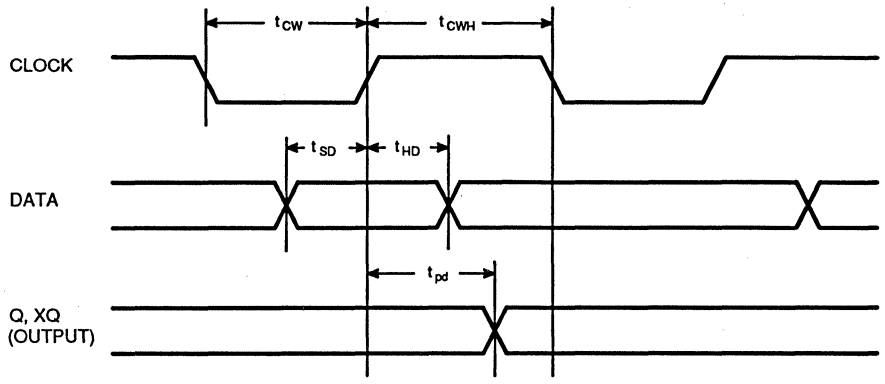
Equivalent Circuit (FF0)



3

Definitions of Parameters

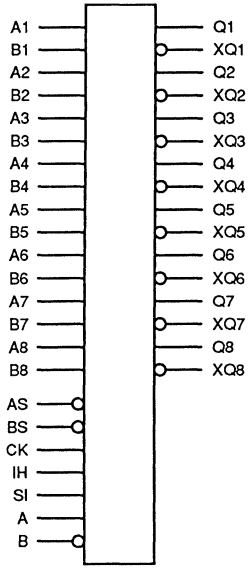
i) CLOCK MODE



3

Cell Name	Function	Number of BC
SHJ	SCAN 8–bit DFF with Clock–Inhibit & 2–to–1 Data Multiplexer	78

Cell Symbol



Pin Name	Input Loading Factor (Iu)
An, Bn (n=1~8)	1
AS, BS	1
CK	1
IH	1
SI	1
A, B	1

Pin Name	Output Driving Factor (Iu)
Q	18
XQ	18

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.548	0.060	2.554	0.039	0.056	4	CK, IH to Q
2.178	0.060	2.112	0.050	0.089	4	CK, IH to XQ

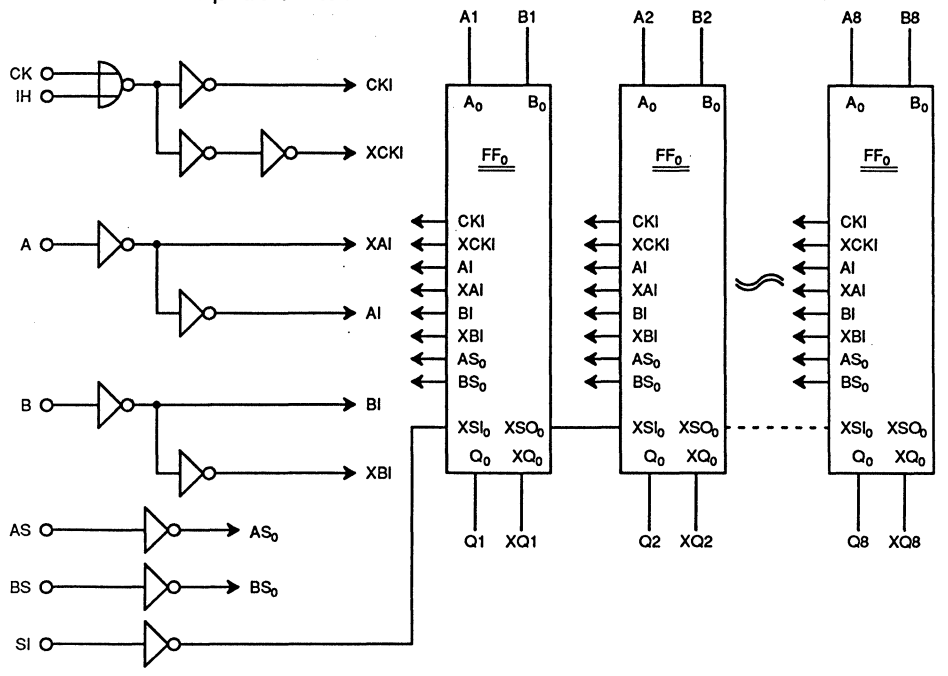
Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	4.2
Clock Pause Time	t_{CWH}	3.2
Data Setup Time	t_{SD}	1.8
Data Hold Time	t_{HD}	1.9

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

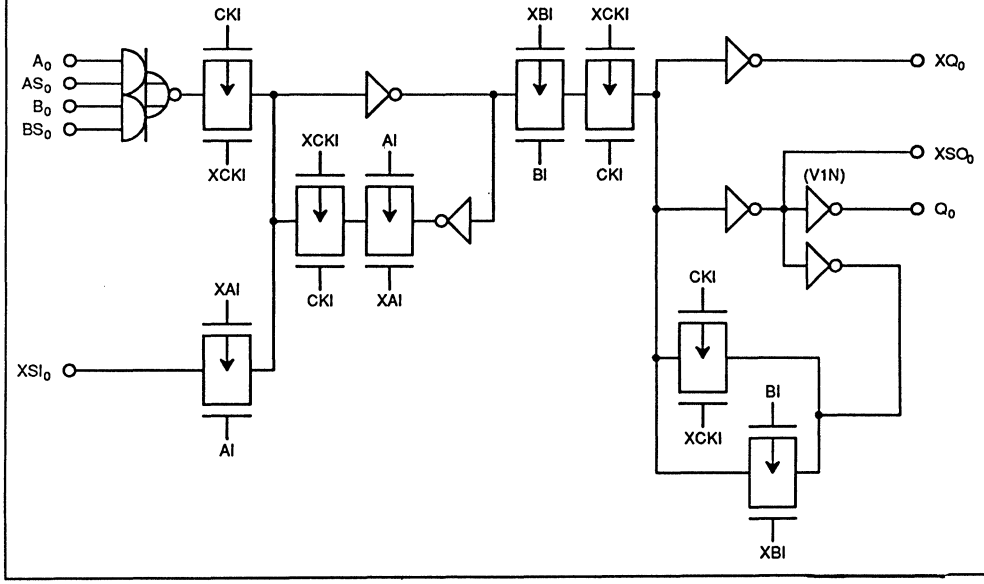
Cell Name

SHJ

Equivalent Circuit



Equivalent Circuit (FF0)

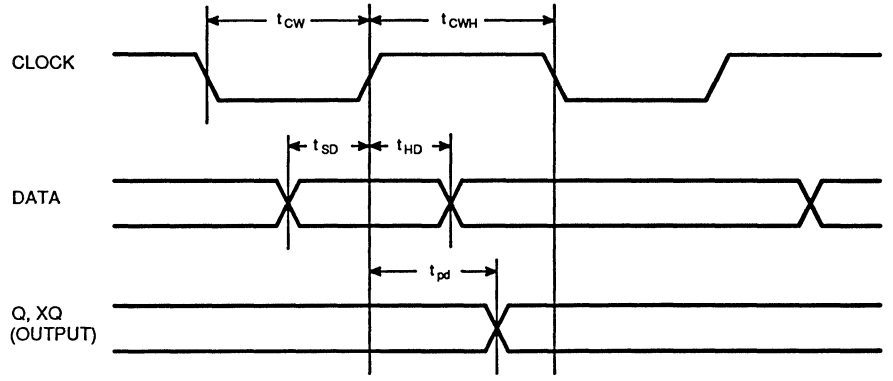


Cell Name

SHJ

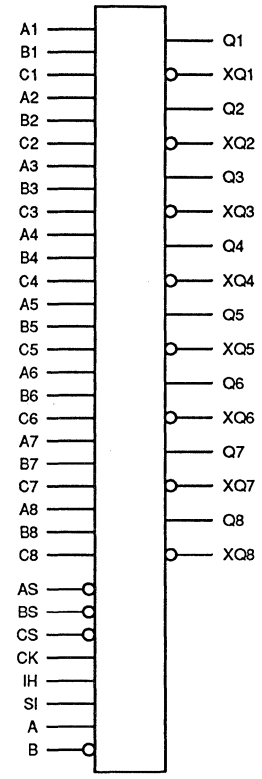
Definitions of Parameters

i) CLOCK MODE



Cell Name	Function	Number of BC
SHK	SCAN 8–bit DFF with Clock–Inhibit & 3–to–1 Data Multiplexer	88

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
2.449	0.060	2.429	0.039	0.045	4	CK, IH to Q
2.158	0.060	2.112	0.062	0.084	4	CK, IH to XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	4.2
Clock Pause Time	t_{CWH}	3.2
Data Setup Time	t_{SD}	2.3
Data Hold Time	t_{HD}	1.8

Pin Name	Input Loading Factor (lu)
An, Bn, Cn (n=1 ~ 8)	1
AS, BS, CS	1
CK	1
IH	1
SI	1
A, B	1

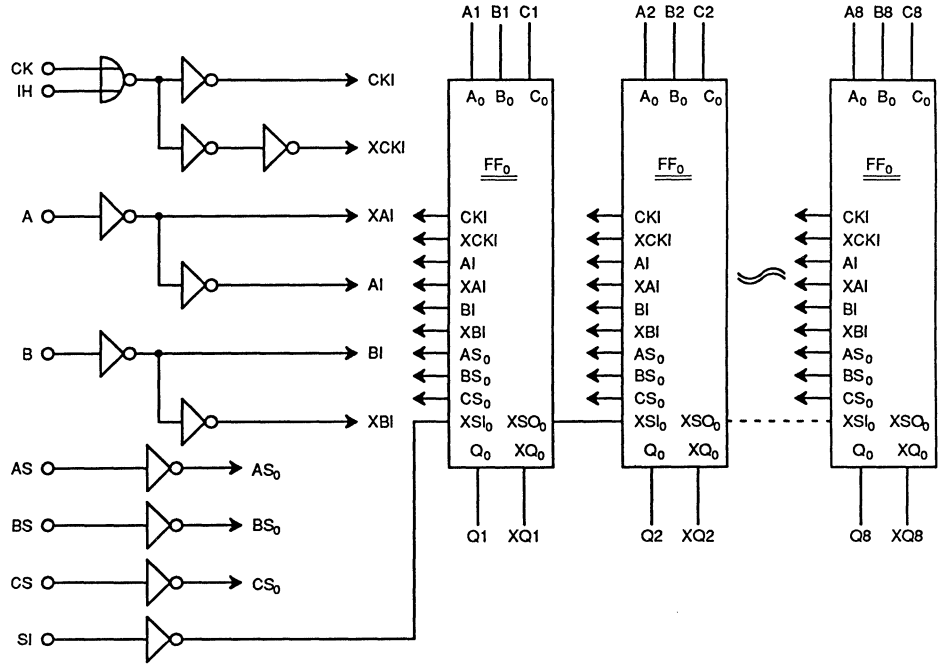
Pin Name	Output Driving Factor (lu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

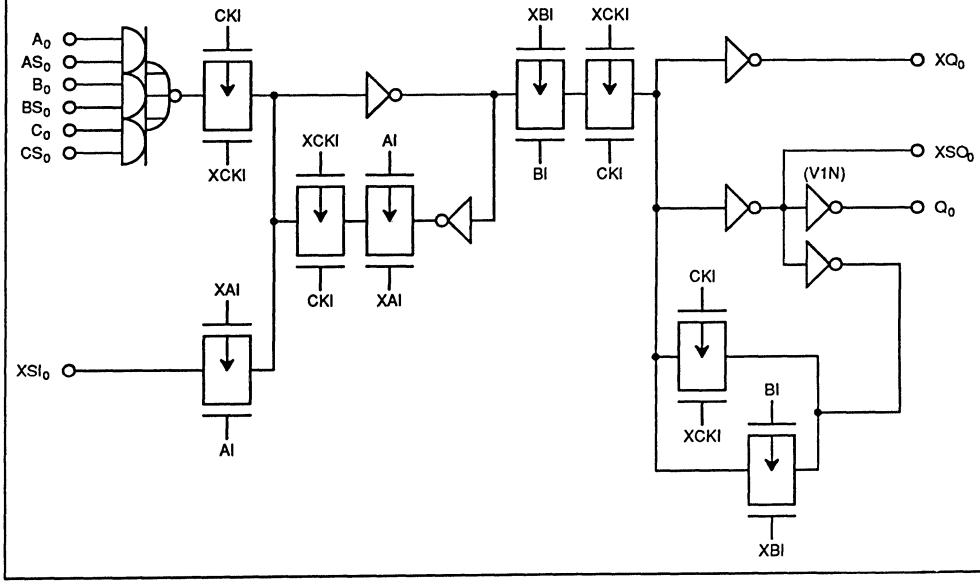
Cell Name

SHK

Equivalent Circuit

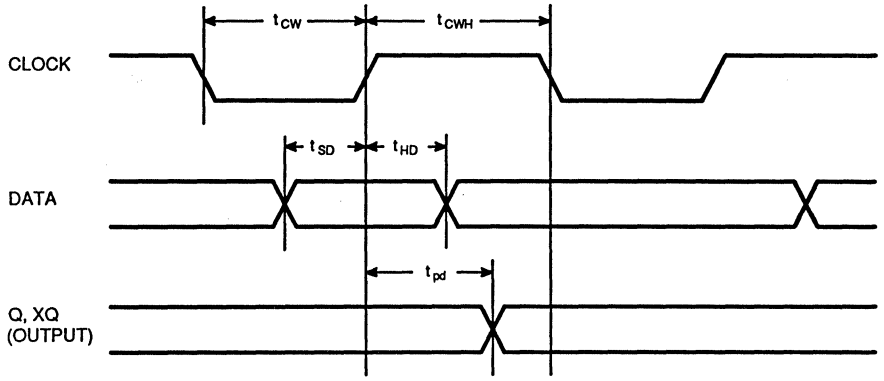


Equivalent Circuit (FF0)



Definitions of Parameters

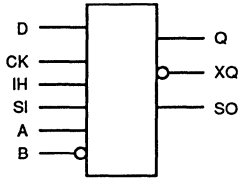
i) CLOCK MODE



3

Cell Name	Function	Number of BC
SFDM	SCAN 1–input DFF with Clock–Inhibit	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.221	0.060	1.254	0.045	0.078	4	CK to Q
1.551	0.060	1.525	0.039	0.045	4	CK to XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	1.0
Data Hold Time	t_{HD}	0.8

Pin Name	Input Loading Factor (Iu)
D	2
CK	1
IH	1
SI	2
A, B	2

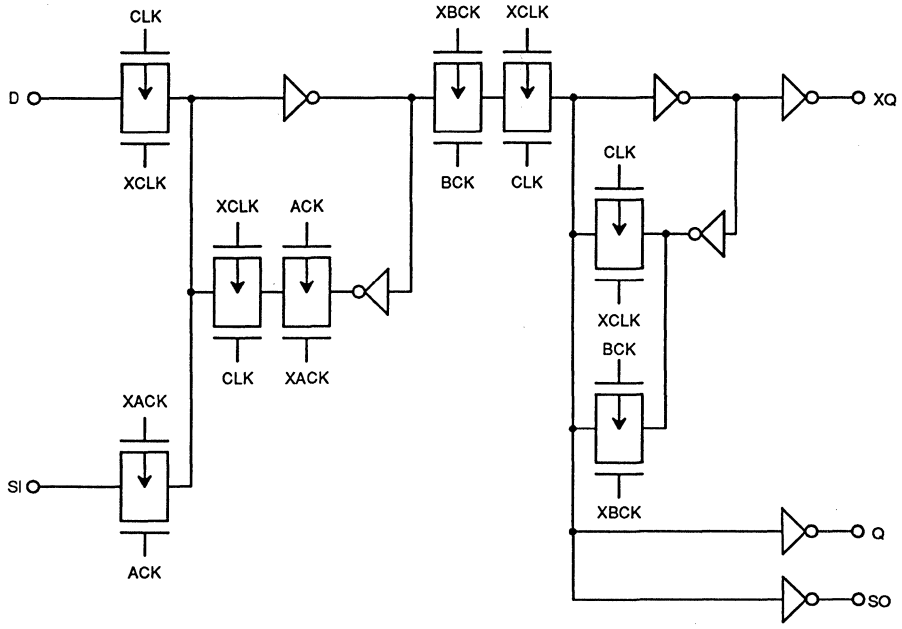
Pin Name	Output Driving Factor (Iu)
Q	18
SO	18

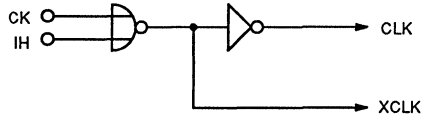
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

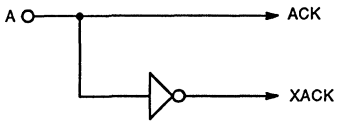
Cell Name

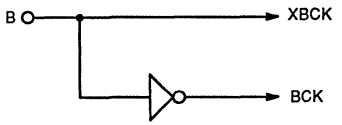
SFDM

Equivalent Circuit







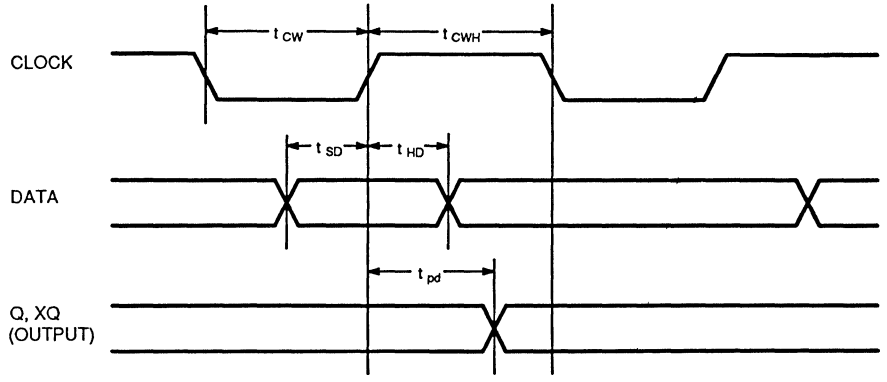


Cell Name

SFDM

Definitions of Parameters

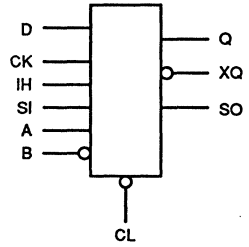
i) CLOCK MODE



3

Cell Name	Function	Number of BC
SFDO	SCAN 1-input DFF with Clear and Clock Inhibit	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.413	0.064	1.347	0.050	0.084	4	CK to Q
1.564	0.060	1.729	0.039	0.045	4	CK to XQ
1.657	0.060	1.439	0.050	0.084	4	CL to Q,XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	1.6
Data Hold Time	t_{HD}	1.1
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.2
Clear Hold Time	t_{INH}	2.9

Pin Name	Input Loading Factor (Iu)
D	2
CK, IH	1
SI	2
A, B	2
CL	2

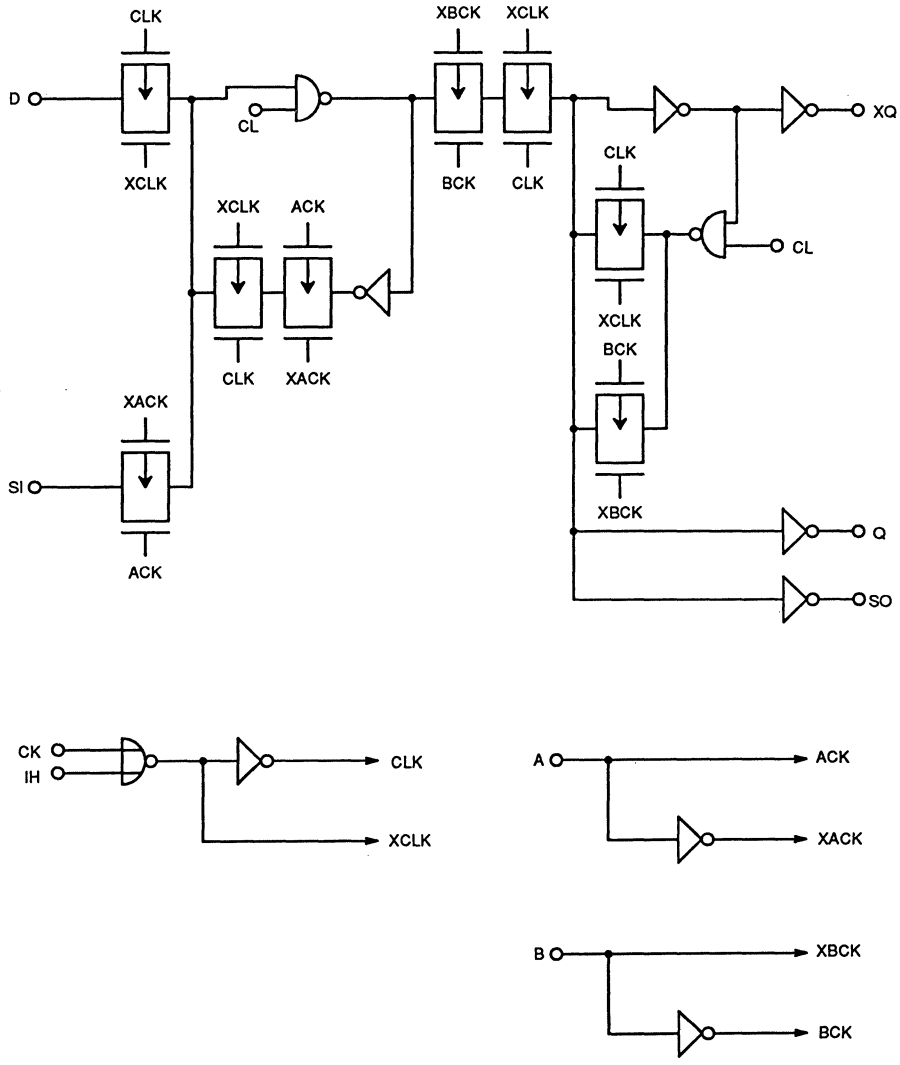
Pin Name	Output Driving Factor (Iu)
Q	18
XQ	18
SO	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name

SFDO

Equivalent Circuit



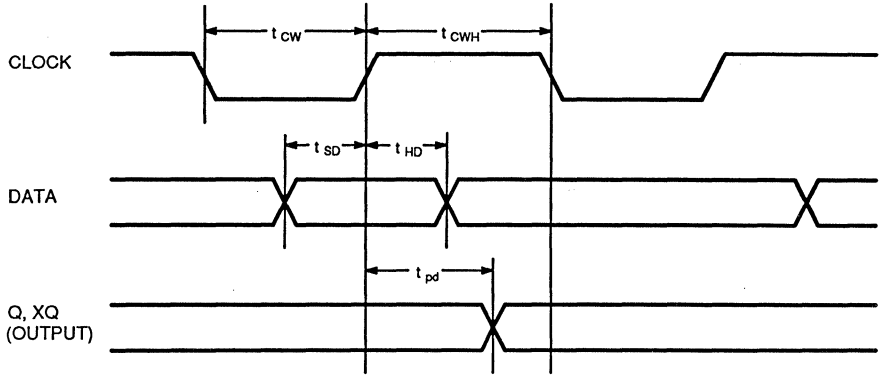
3

Cell Name

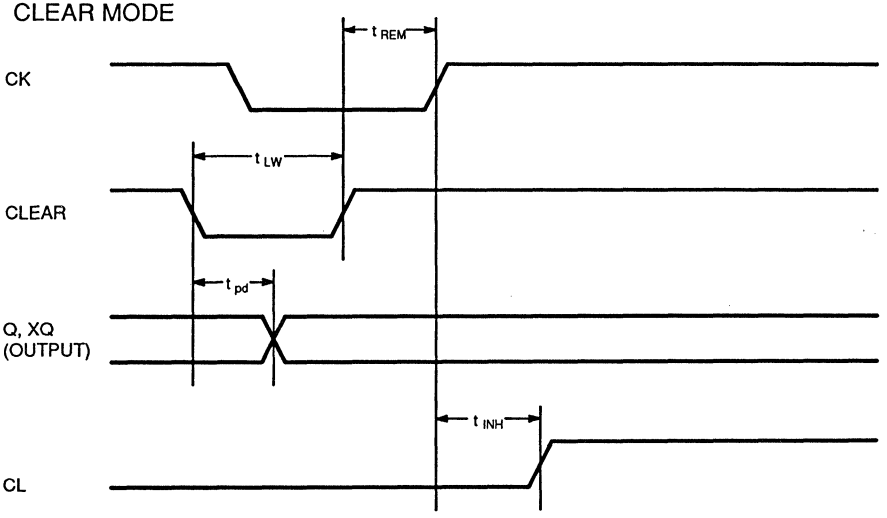
SFDO

Definitions of Parameters

i) CLOCK MODE



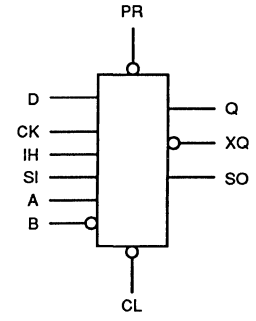
i i) CLEAR MODE



3

Cell Name	Function	Number of BC
SFDP	SCAN 1–input DFF with Clear, Preset, and Clock Inhibit	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.426	0.064	1.340	0.050	0.084	4	CK to Q
1.888	0.060	1.729	0.039	0.045	4	CK to XQ
1.921	0.060	1.419	0.050	0.084	4	CL to Q,XQ
2.403	0.064	0.548	0.039	0.045	4	PR to Q,XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	1.6
Data Hold Time	t_{HD}	1.1
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.2
Clear Hold Time	t_{INH}	2.9
Preset Pulse Width	t_{PW}	3.6
Preset Release Time	t_{REM}	0.6
Preset Hold Time	t_{INH}	3.6

Pin Name	Input Loading Factor (Iu)
D	2
CK, IH	1
SI	2
A, B	2
CL, PR	2

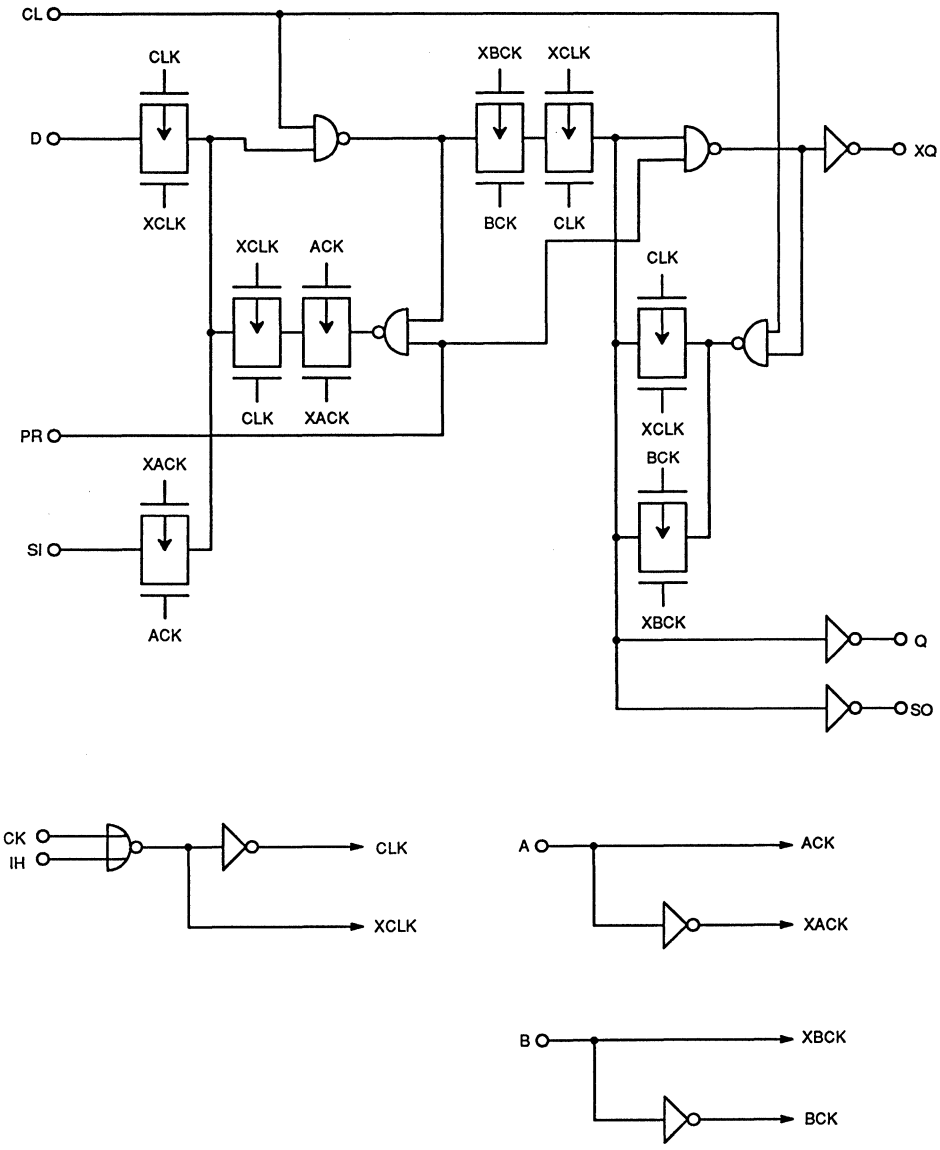
Pin Name	Output Driving Factor (Iu)
Q	18
XQ	18
SO	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name

SFDP

Equivalent Circuit

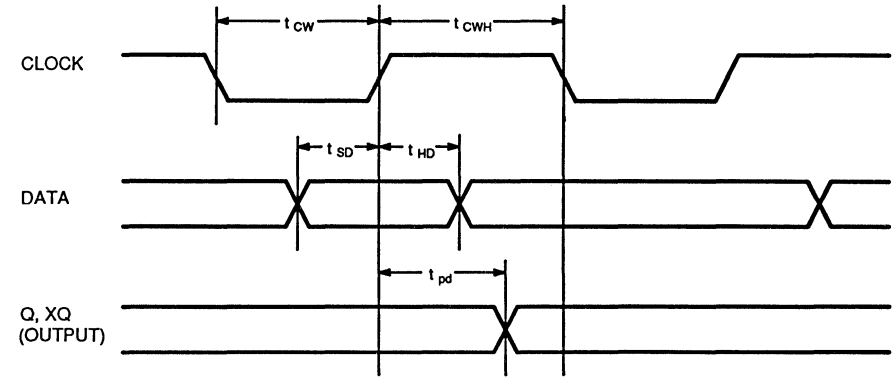


Cell Name

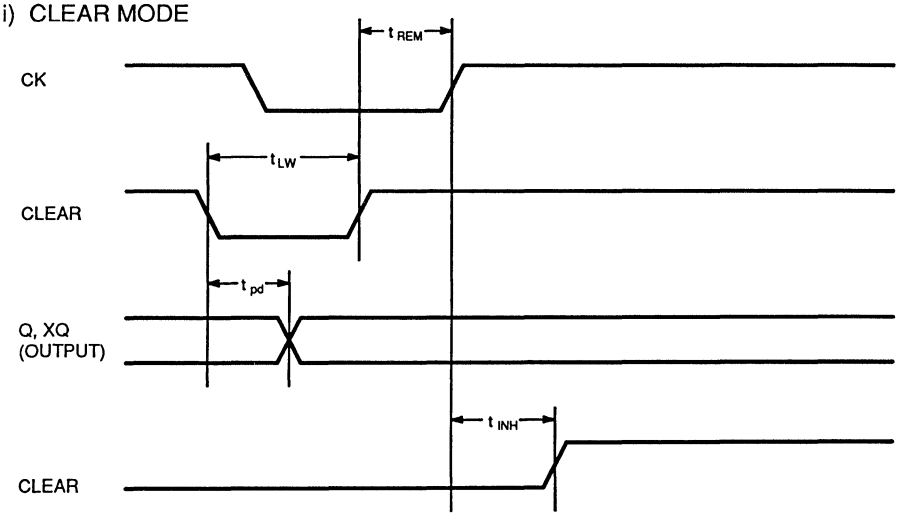
SFDP

Definitions of Parameters

i) CLOCK MODE



i i) CLEAR MODE



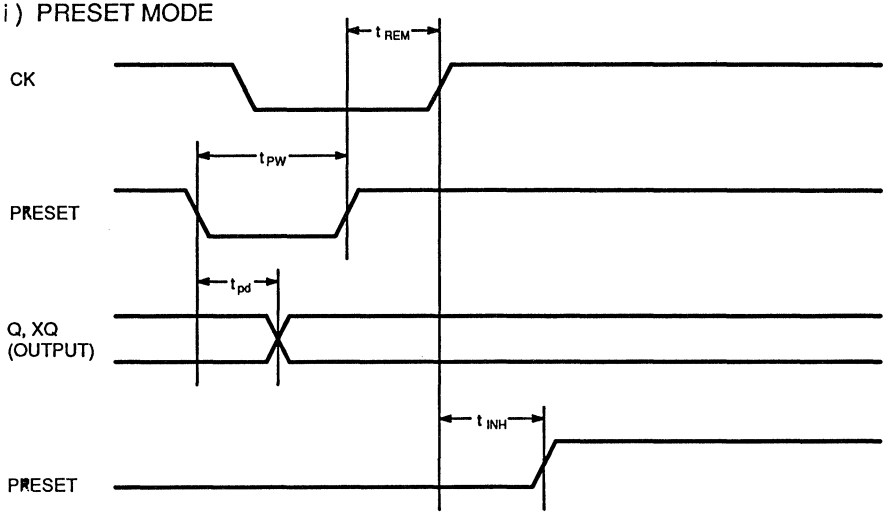
3

Cell Name

SFDP

Definitions of Parameters

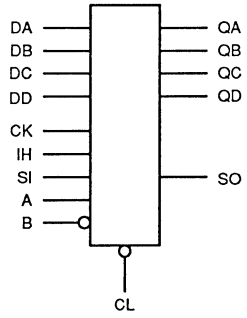
iii) PRESET MODE



3

Cell Name	Function	Number of BC
SFDR	SCAN 4–input DFF with Clear and Clock Inhibit	36

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
1.967	0.064	1.980	0.050	0.084	4	CK to Q
–	–	2.026	0.050	0.089	4	CL to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	3.2
Data Setup Time	t_{SD}	0.7
Data Hold Time	t_{HD}	1.5
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.7
Clear Hold Time	t_{INH}	3.4

Pin Name	Input Loading Factor (lu)
D	2
CK, IH	1
SI	2
A, B	1
CL	1

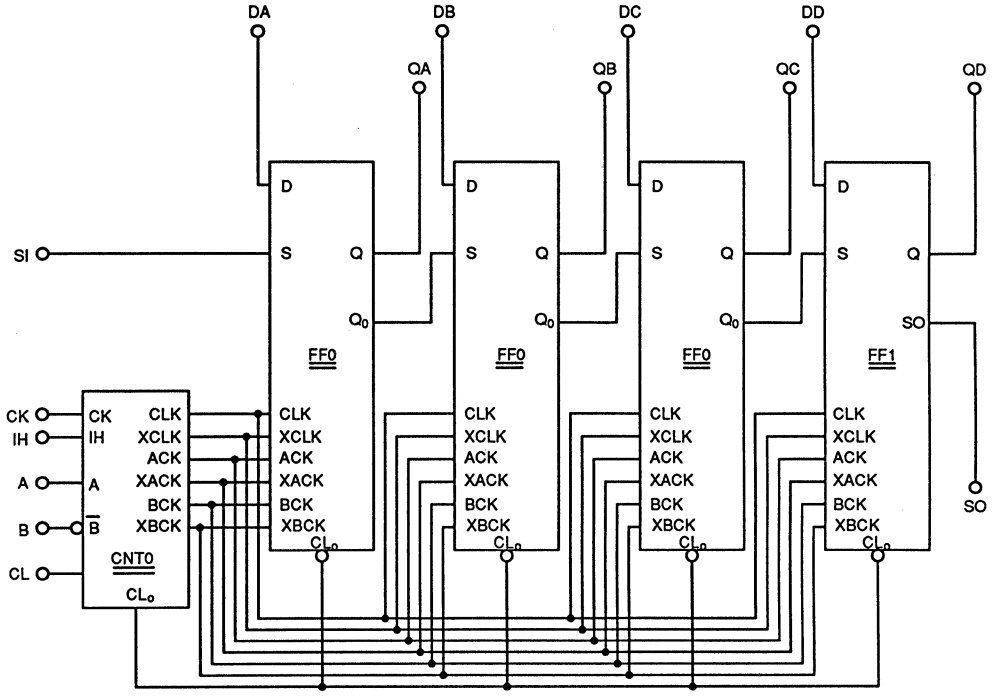
Pin Name	Output Driving Factor (lu)
Q	18
SO	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

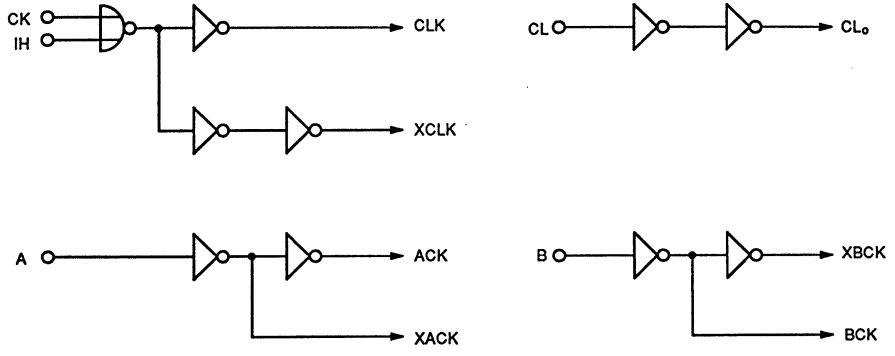
Cell Name

SFDR

Equivalent Circuit



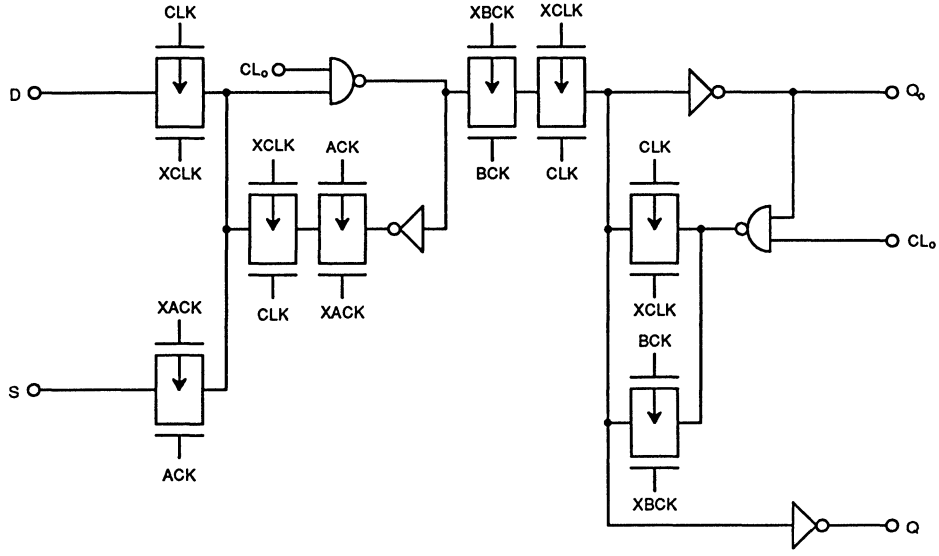
Equivalent Circuit (CNTO)



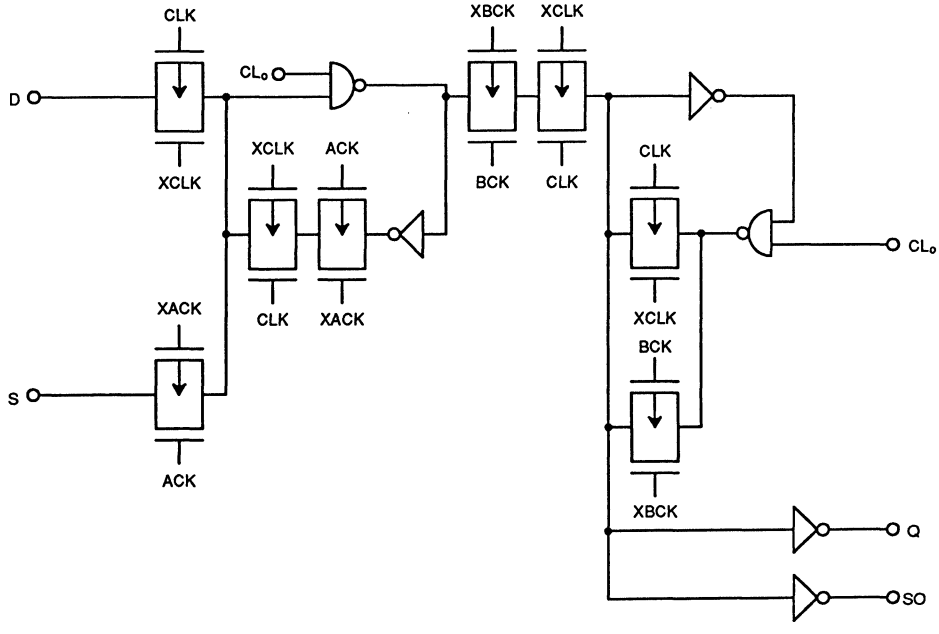
Cell Name

SFDR

Equivalent Circuit (FF0)



Equivalent Circuit (FF1)



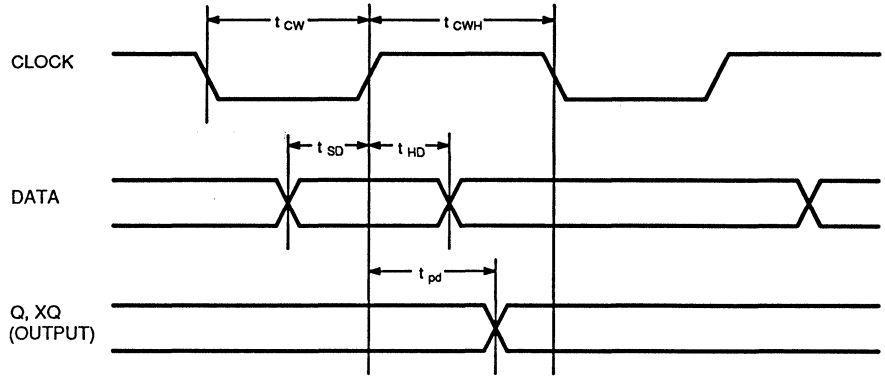
3

Cell Name

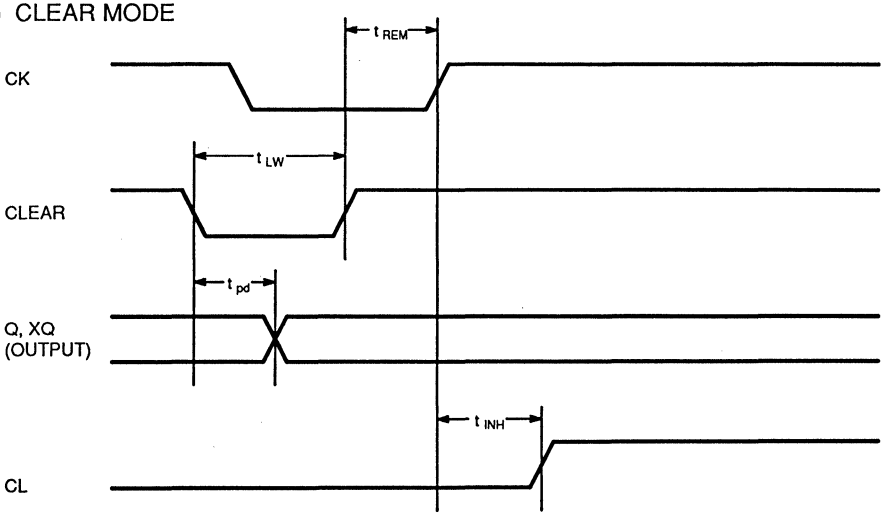
SFDR

Definitions of Parameters

i) CLOCK MODE



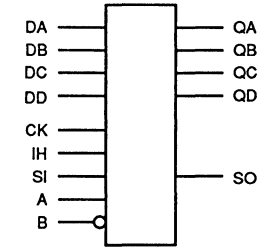
i i) CLEAR MODE



3

Cell Name	Function	Number of BC
SFDS	SCAN 4–input DFF with Clock Inhibit	31

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.624	0.060	1.597	0.045	0.073	4	CK to QA~QC
1.736	0.060	1.716	0.045	0.073	4	CK to QD

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	3.2
Data Setup Time	t_{SD}	0.0
Data Hold Time	t_{HD}	1.3

Pin Name	Input Loading Factor (Iu)
D	2
CK, IH	1
SI	2
A, B	1

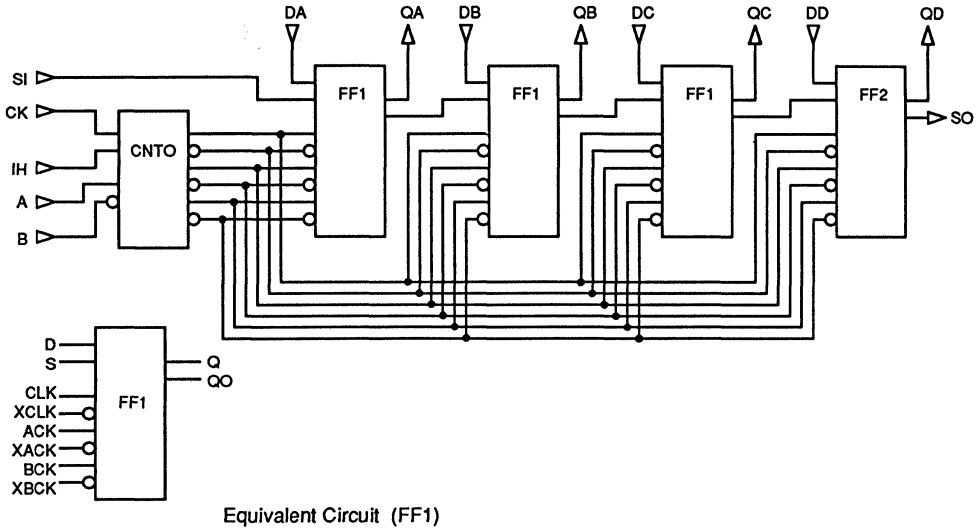
Pin Name	Output Driving Factor (Iu)
Q	18
SO	18

* Minimum values for the typical operating condition.
The values for the worst case operating conditlon are given by the maximum delay multiplier.

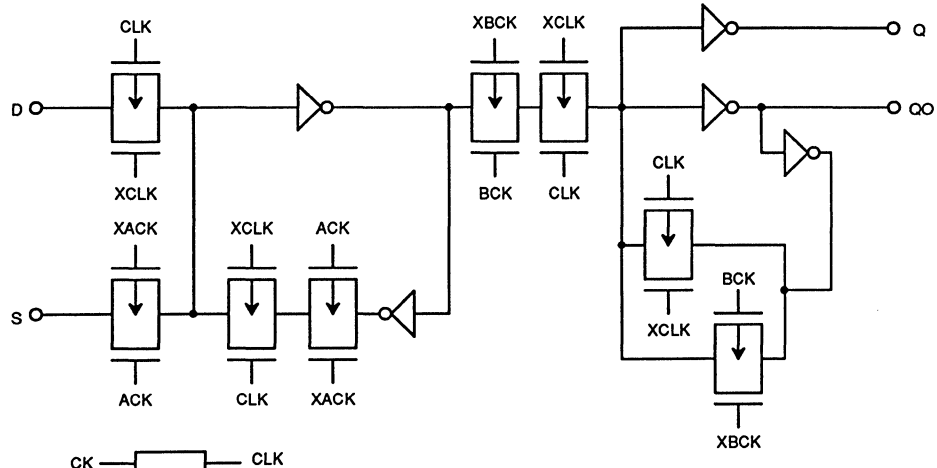
Cell Name

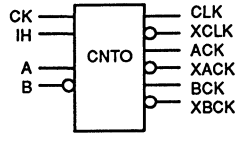
SFDS

Equivalent Circuit

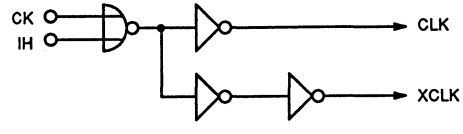


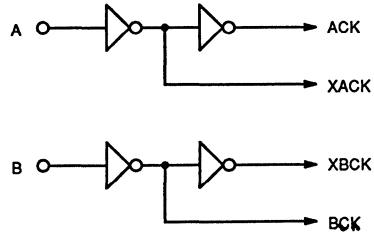
Equivalent Circuit (FF1)





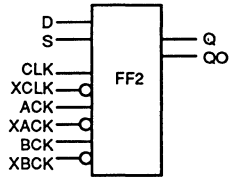
Equivalent Circuit (CNTO)



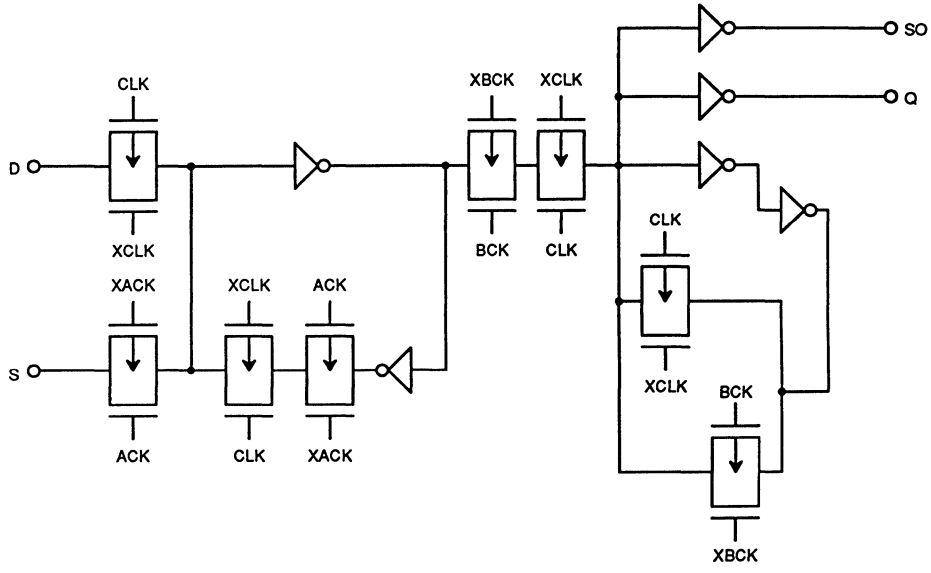


Cell Name

SFDS



Equivalent Circuit (FF2)

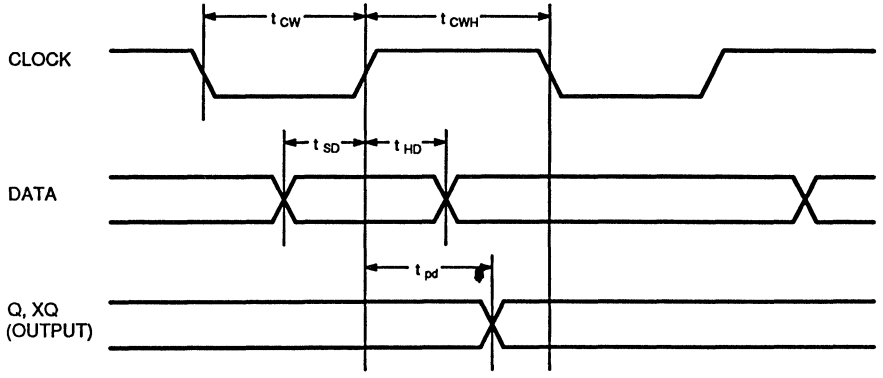


Cell Name

SFDS

Definitions of Parameters

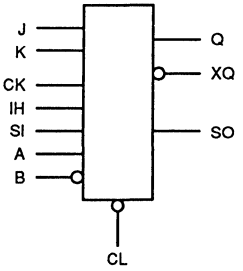
i) CLOCK MODE



3

Cell Name	Function	Number of BC
SFJD	SCAN J–K FF with Clock Inhibit	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.710	0.064	1.584	0.056	0.089	4	CK to Q
1.828	0.060	2.000	0.039	0.045	4	CK to XQ
1.479	0.060	1.307	0.039	0.078	4	CL to Q,XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time (J)	t_{SD}	2.2
Data Hold Time (J)	t_{HD}	0.4
Data Setup Time (K)	t_{SD}	1.9
Data Hold Time (K)	t_{HD}	0.1
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.2
Clear Hold Time	t_{INH}	2.6

Pin Name	Input Loading Factor (lu)
J, K	1
CK, IH	1
SI	2
A, B	2
CL	2

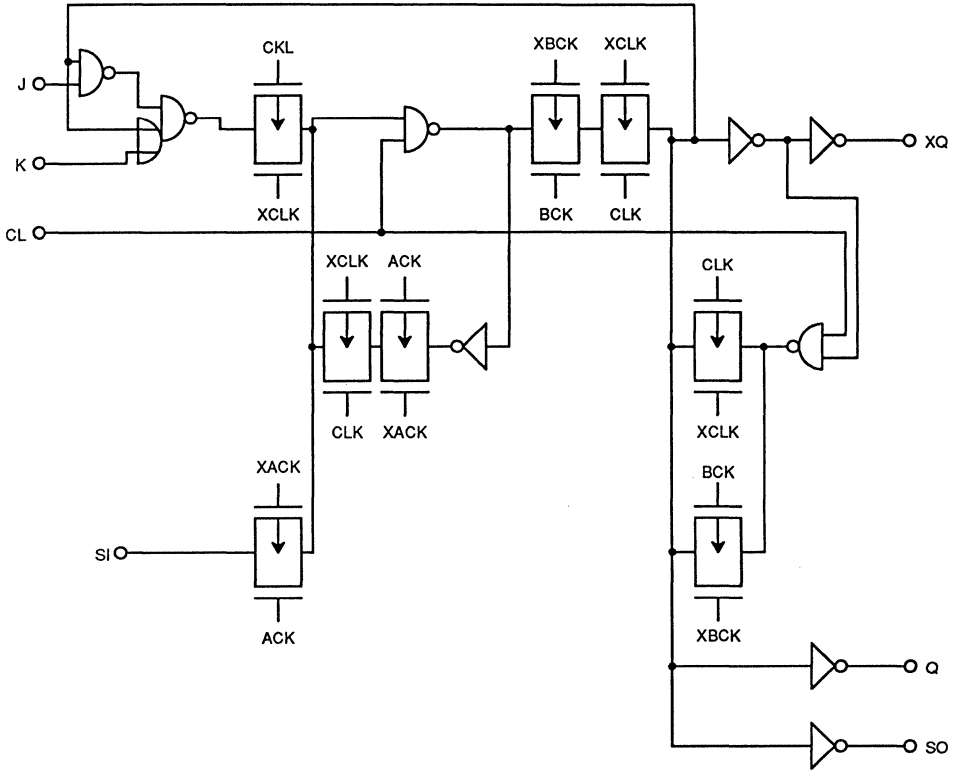
Pin Name	Output Driving Factor (lu)
Q	18
XQ	18
SO	18

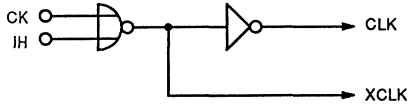
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

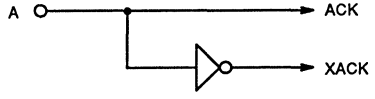
Cell Name

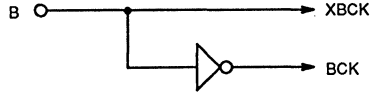
SFJD

Equivalent Circuit







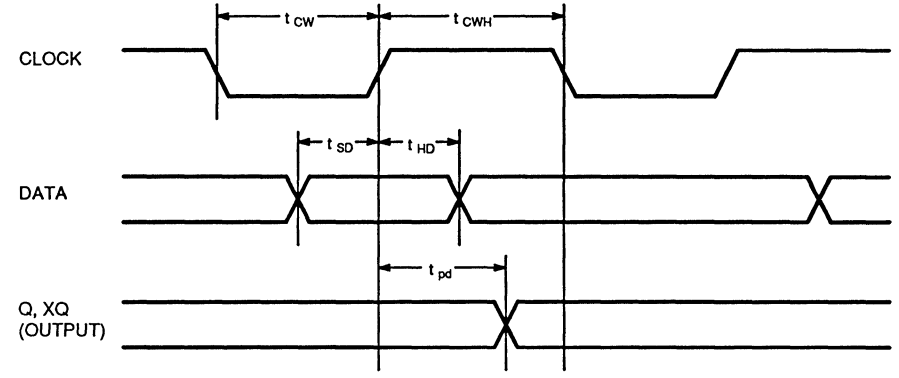


Cell Name

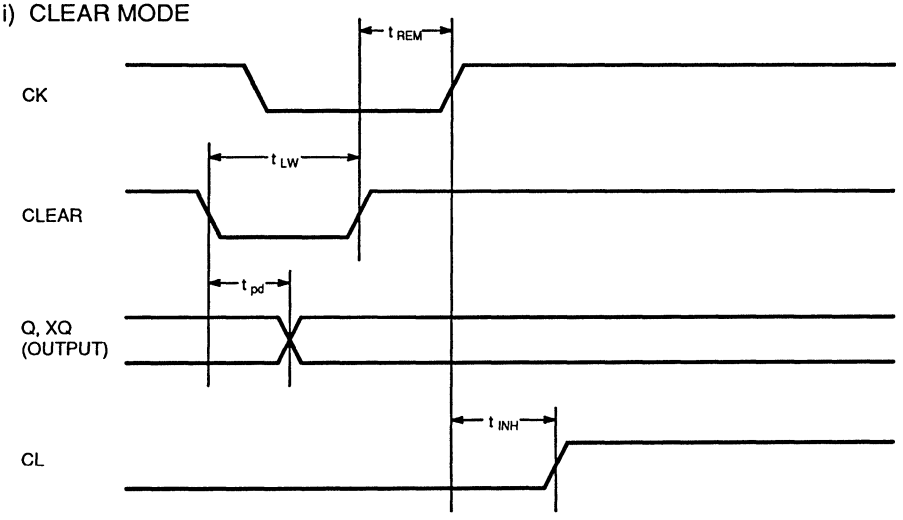
SFJD

Definitions of Parameters

i) CLOCK MODE



i i) CLEAR MODE



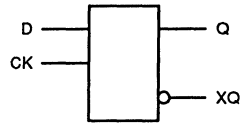
3

Non Scan Flip-Flop Family

Page	Unit Cell Name	Function	Basic Cells
3–183	FDM	Non-Scan D FF	6
3–185	FDN	Non-Scan D FF with Set	7
3–187	FDO	Non-Scan D FF with Reset	7
3–189	FDP	Non-Scan D FF with Set and Reset	8
3–192	FDQ	Non-Scan 4-bit D FF	21
3–194	FDR	Non-Scan 4-bit D FF with Clear	26
3–197	FDS	Non-Scan 4-bit D FF	20
3–199	FD2	Non-Scan Power D FF	7
3–201	FD3	Non-Scan Power D FF with Preset	8
3–203	FD4	Non-Scan Power D FF with Clear and Preset	9
3–205	FD5	Non-Scan Power D FF with Clear	8
3–207	FJD	Non-Scan Positive Edge Clocked Power J–K FF with Clear	12

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
FDM	Non–SCAN DFF	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.924	0.060	0.951	0.039			CK to Q
1.142	0.060	1.248	0.039			CK to XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	1.3
Data Hold Time	t_{HD}	0.9

Pin Name	Input Loading Factor (lu)
D	2
CK	1

Pin Name	Output Driving Factor (lu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

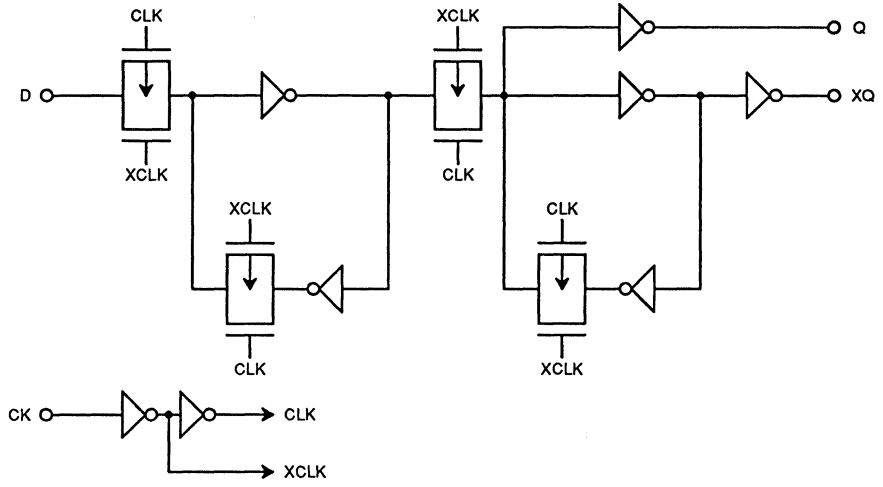
Function Table

Inputs		Outputs	
D	CK	Q	XQ
H	↑	H	L
L	↑	L	H

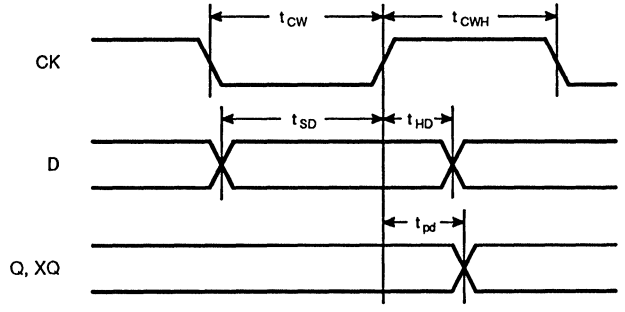
Cell Name

FDM

Equivalent Circuit



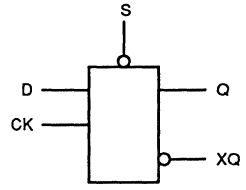
Definitions of Parameters



3

Cell Name	Function	Number of BC
FDN	Non–SCAN DFF with SET	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.951	0.060	0.924	0.039	0.056	4	CK to Q
1.300	0.060	1.281	0.039			CK to XQ
1.182	0.060	0.568	0.039			S to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	1.3
Data Hold Time	t_{HD}	0.9
Set Pulse Width	t_{SW}	2.5
Set Release Time (S)	t_{REM}	0.3
Set Hold Time	t_{INH}	2.3

Pin Name	Input Loading Factor (lu)
D	2
S	2
CK	1

Pin Name	Output Driving Factor (lu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

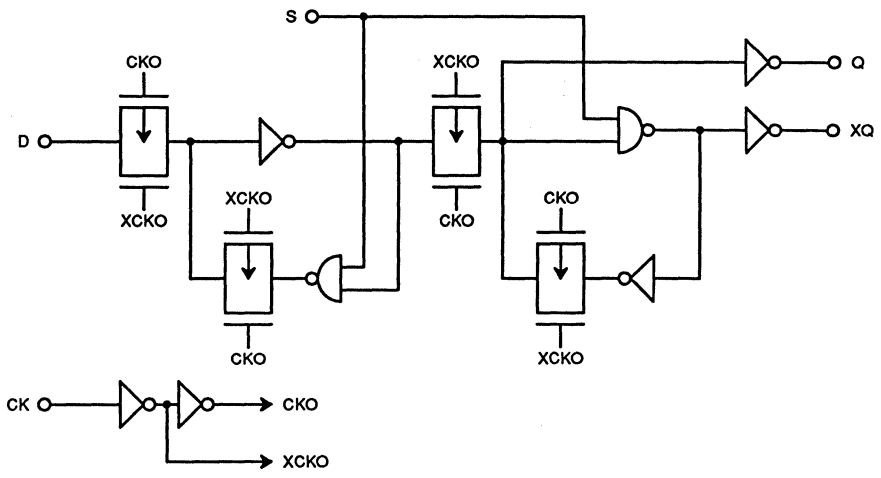
Function Table

Inputs			Outputs	
S	D	CK	Q	XQ
L	X	X	H	L
H	H	↑	H	L
H	L	↑	L	H

Cell Name

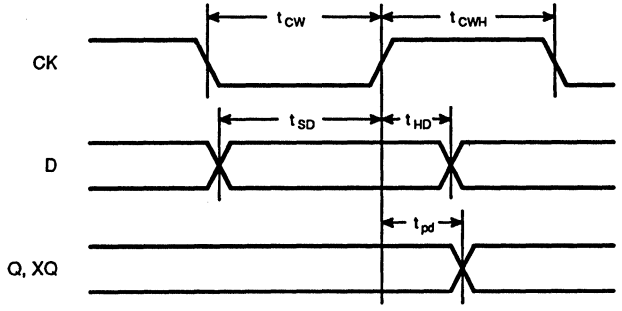
FDN

Equivalent Circuit

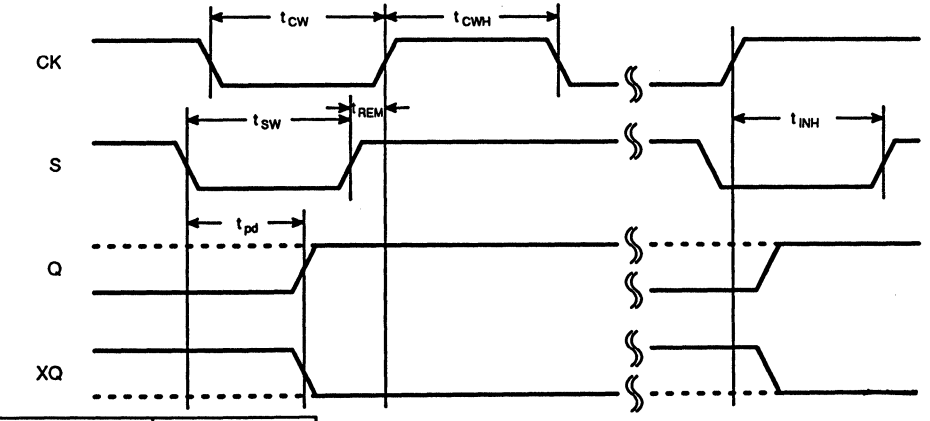


Definitions of Parameters

1) tCW, tCWH, tSD, tHD and tpd (CK Q, XQ)

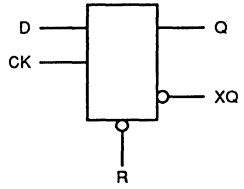


2) tSW, tREM, tINH, and tpd (S Q, XQ)



Cell Name	Function	Number of BC
FDO	Non–SCAN DFF with RESET	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.023	0.060	0.944	0.045			CK to Q
1.142	0.060	1.366	0.039			CK to XQ
1.056	0.060	0.865	0.045			R to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	1.3
Data Hold Time	t_{HD}	0.9
Reset Pulse Width	t_{RW}	2.5
Reset Release Time (R)	t_{REM}	0.6
Reset Hold Time	t_{INH}	2.0

Pin Name	Input Loading Factor (Iu)
D	2
R	2
CK	1

Pin Name	Output Driving Factor (Iu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

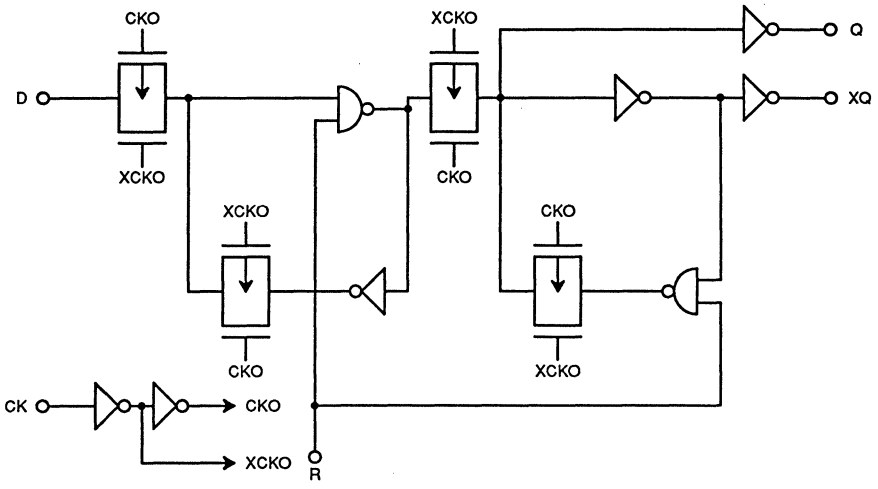
Function Table

Inputs			Outputs	
R	D	CK	Q	XQ
L	X	X	L	H
H	H	↑	H	L
H	L	↑	L	H

Cell Name

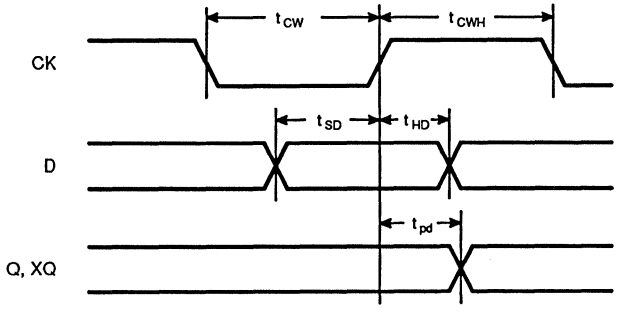
FDO

Equivalent Circuit

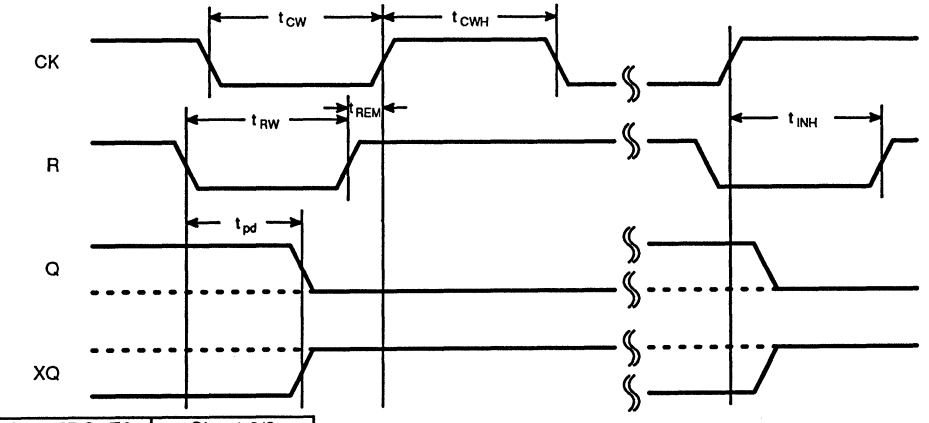


Definitions of Parameters

1) tCW, tCWH, tSD, tHD and tpd (CK Q, XQ)

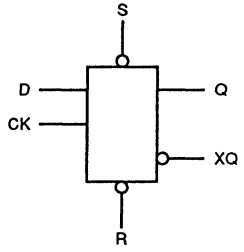


2) tRW, tREM, tINH, and tpd (R Q, XQ)



Cell Name	Function	Number of BC
FDP	Non–SCAN DFF with Set and Reset	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.036	0.060	0.931	0.045			CK to Q
1.294	0.060	1.320	0.039			CK to XQ
1.182	0.060	0.838	0.045			R to Q, XQ
1.340	0.060	0.535	0.039			S to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	1.3
Data Hold Time	t_{HD}	0.9
Set Pulse Width	t_{SW}	2.5
Set Release Time (S)	t_{REM}	0.3
Set Hold Time	t_{INH}	2.3
Reset Pulse Width	t_{RW}	2.5
Reset Release Time (R)	t_{REM}	0.6
Reset Hold Time	t_{INH}	2.0

Pin Name	Input Loading Factor (Iu)
D	2
S	2
R	2
CK	1

Pin Name	Output Driving Factor (Iu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

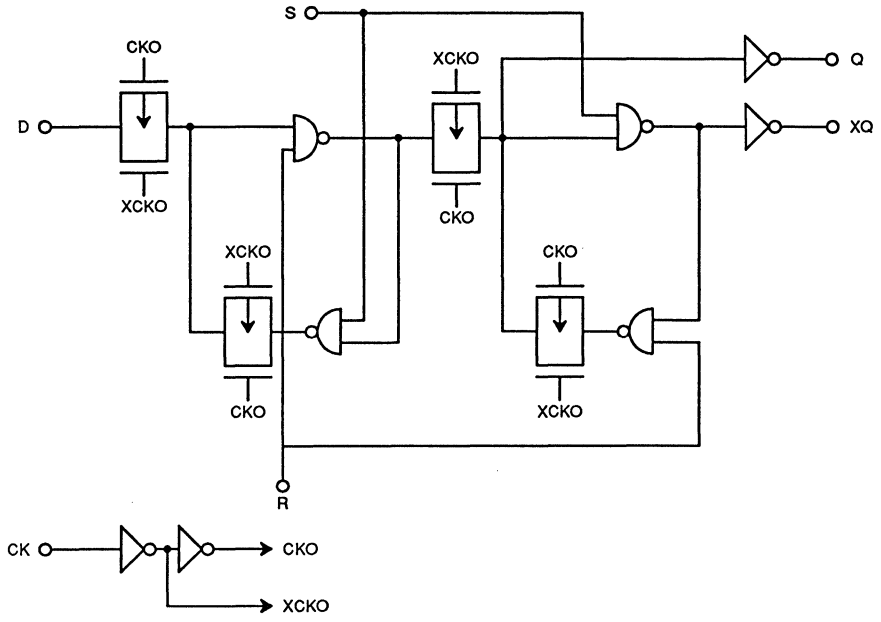
Inputs				Outputs	
S	R	D	CK	Q	XQ
H	L	X	X	L	H
L	H	X	X	H	L
L	L	X	X	Inhibited	
H	H	H	↑	H	L
H	H	L	↑	L	H

3

Cell Name

FDP

Equivalent Circuit



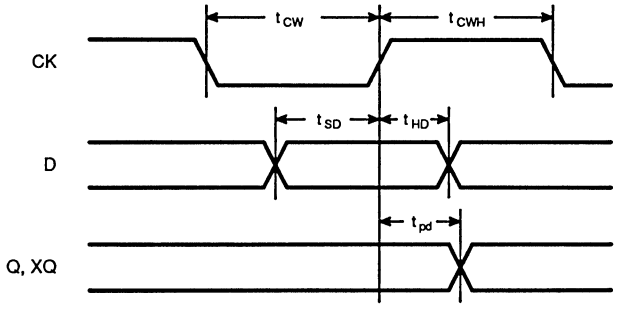
3

Cell Name

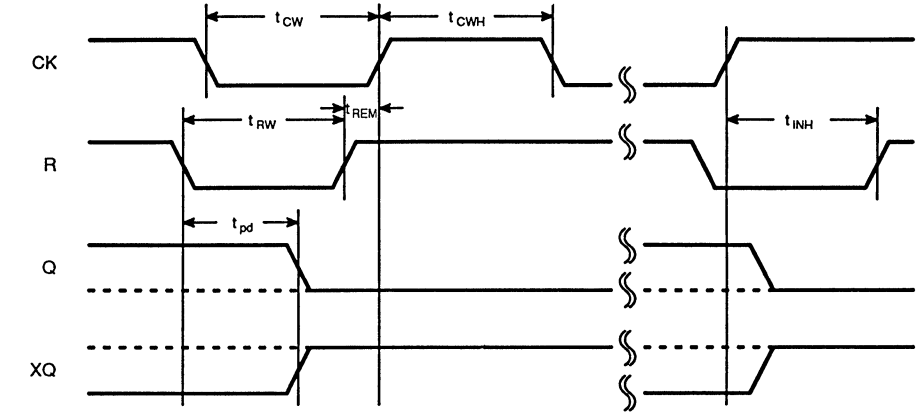
FDP

Definitions of Parameters

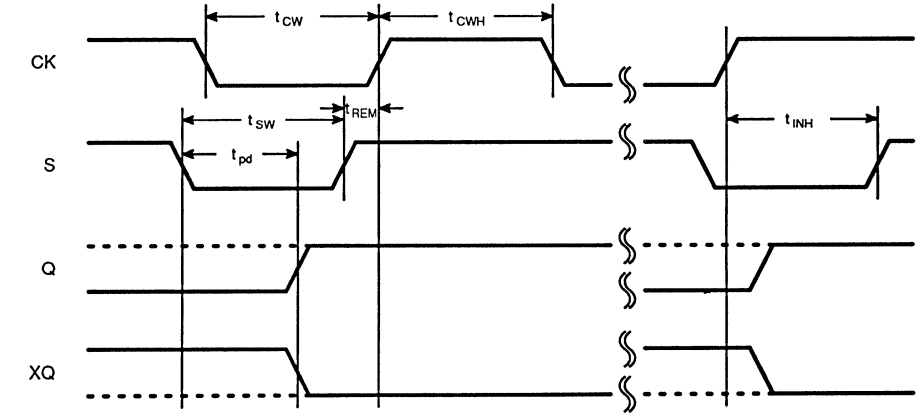
1) tCW, tCWH, tSD, tHD and tpd (CK → Q, XQ)



2) tRW, tREM, tINH, and tpd (R → Q, XQ)



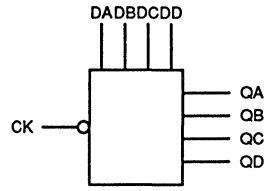
3) tSW, tREM, tINH, and tpd (S → Q, XQ)



3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
FDQ	Non–SCAN 4–bit DFF	21

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.782	0.060	1.446	0.039			CK to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWL}	2.5
Data Setup Time	t_{SD}	0.7
Data Hold Time	t_{HD}	1.7

Pin Name	Input Loading Factor (Iu)
D	1
CK	1

Pin Name	Output Driving Factor (Iu)
Q	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

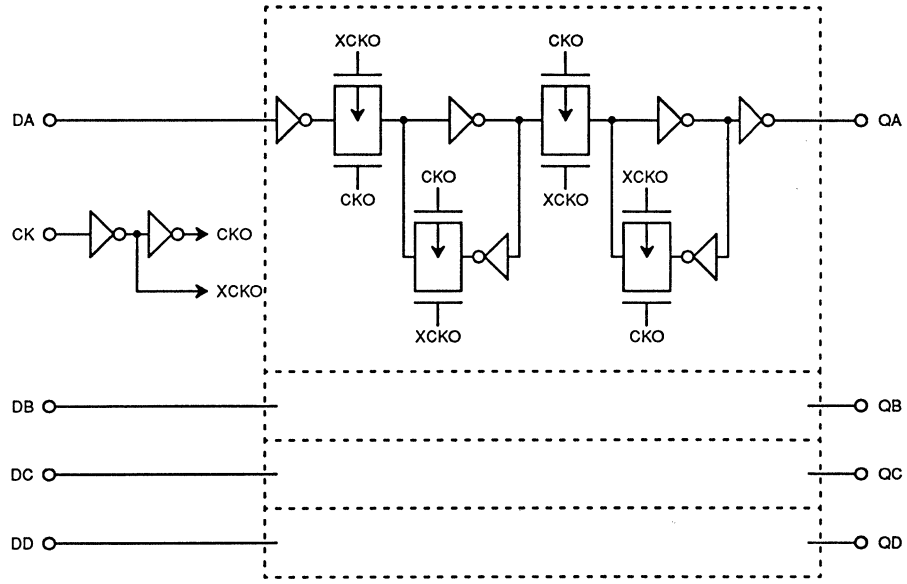
Function Table

Input		Output
CK	D	Q
↓	H	H
↓	L	L

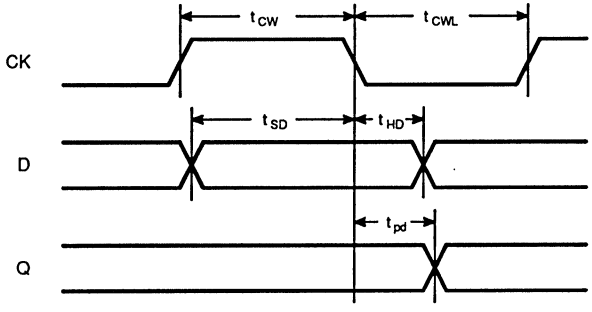
Cell Name

FDQ

Equivalent Circuit



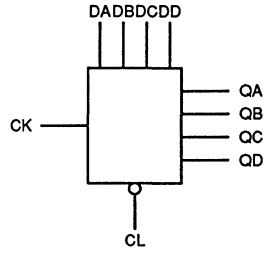
Definitions of Parameters



3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
FDR	Non–SCAN 4–bit DFF with CLEAR	26

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.393	0.060	1.914	0.039			CK to Q
–	–	1.155	0.039			CL to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	0.7
Data Hold Time	t_{HD}	1.7
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	0.9
Clear Hold Time	t_{INH}	2.7

Pin Name	Input Loading Factor (Iu)
D	1
CK	1
CL	1

Pin Name	Output Driving Factor (Iu)
Q	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

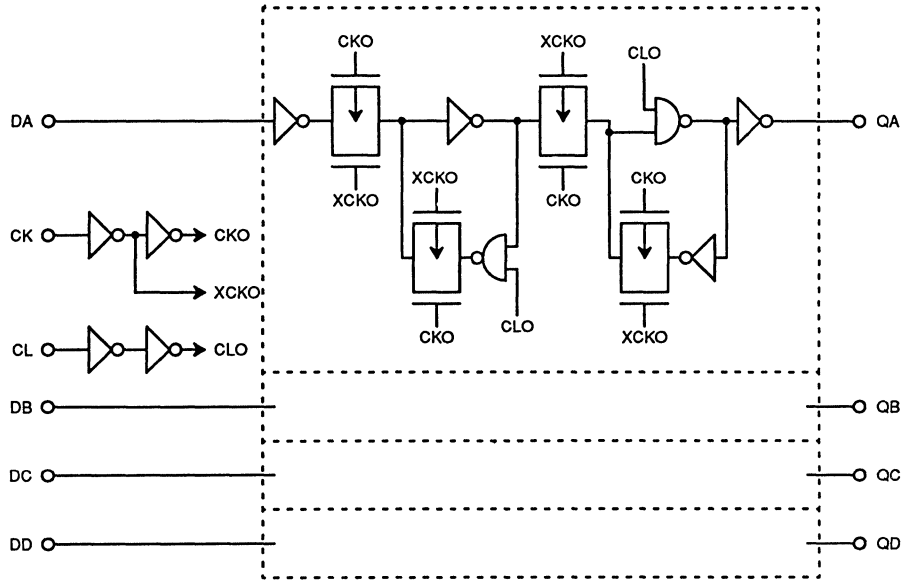
Function Table

Inputs			Output
CK	D	CL	Q
X	X	L	L
↑	L	H	L
↑	H	H	H

Cell Name

FDR

Equivalent Circuit



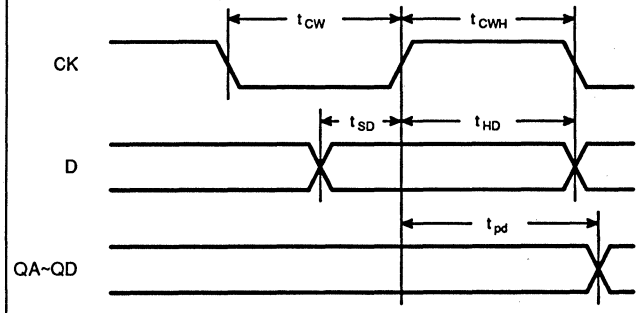
3

Cell Name

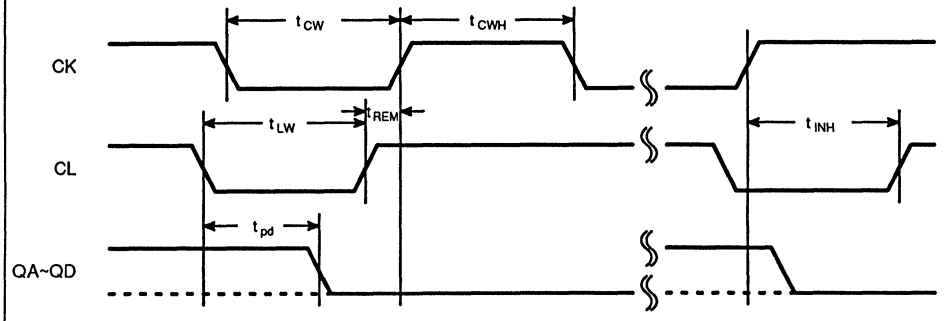
FDR

Definitions of Parameters

1) tCW, tCWH, tSD, tHD and tpd (CK → QA ~ QD)



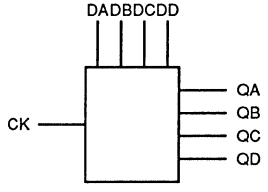
2) tLW, tREM, tINH, and tpd (CL → QA ~ QD)



3

Cell Name	Function	Number of BC
FDS	Non–SCAN 4–bit DFF	20

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.604	0.060	1.294	0.039			CK to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	0.7
Data Hold Time	t_{HD}	1.5

Pin Name	Input Loading Factor (Iu)
D	2
CK	1

Pin Name	Output Driving Factor (Iu)
Q	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

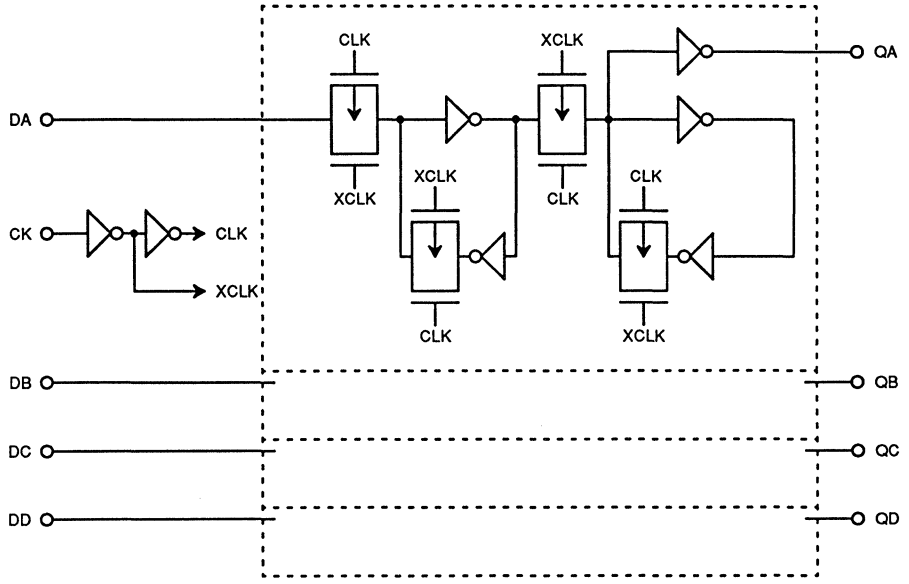
Function Table

Inputs		Outputs
CK	D	Q
↑	L	L
↑	H	H

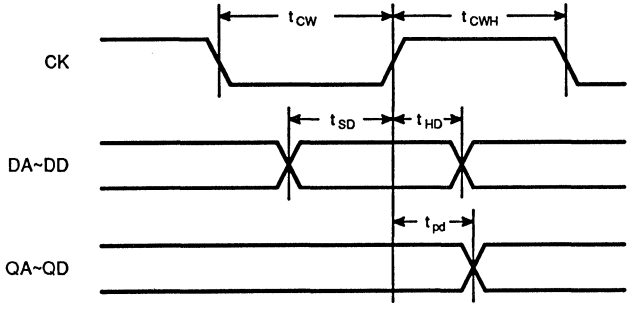
Cell Name

FDS

Equivalent Circuit



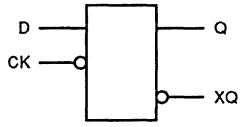
Definitions of Parameters



3

Cell Name	Function	Number of BC
FD2	Non–SCAN Power DFF	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.871	0.032	0.911	0.023	0.045	7	CK to Q
1.347	0.032	1.234	0.017	0.034	7	CK to XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWL}	2.5
Data Setup Time	t_{SD}	1.3
Data Hold Time	t_{HD}	0.9

Pin Name	Input Loading Factor (Iu)
D	2
CK	1

Pin Name	Output Driving Factor (Iu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

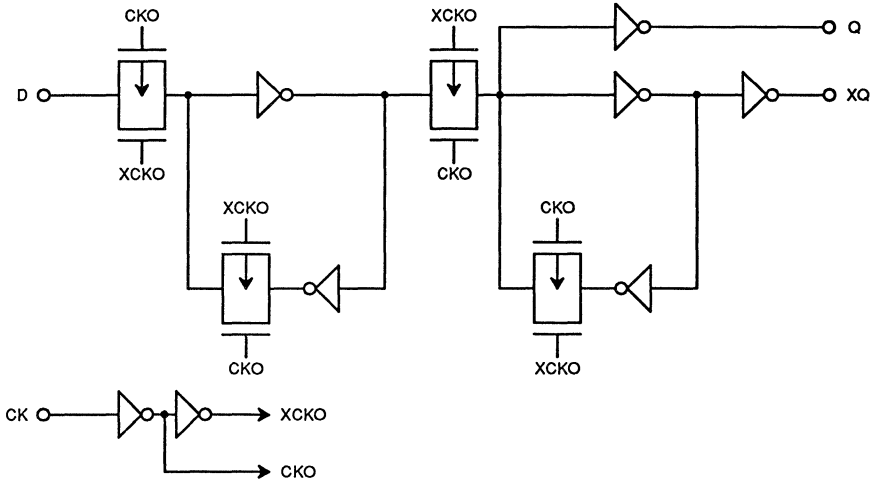
Function Table

Inputs		Outputs	
CK	D	Q	XQ
↓	H	H	L
↓	L	L	H

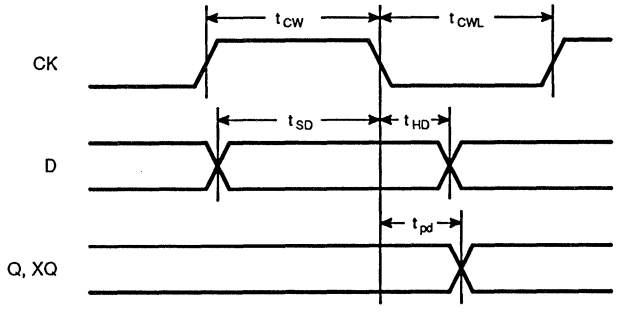
Cell Name

FD2

Equivalent Circuit



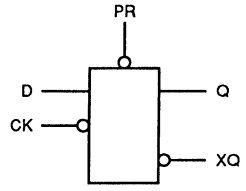
Definitions of Parameters



3

Cell Name	Function	Number of BC
FD3	Non–SCAN Power DFF with Preset	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.904	0.023	0.918	0.017	0.045	7	CK to Q
1.479	0.023	1.320	0.017	0.034	7	CK to XQ
1.261	0.023	0.482	0.017	0.034	7	PR to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWL}	2.5
Data Setup Time	t_{SD}	1.3
Data Hold Time	t_{HD}	0.9
Preset Pulse Width	t_{PW}	2.5
Preset Release Time	t_{REM}	0.3
Preset Hold Time	t_{INH}	2.3

Pin Name	Input Loading Factor (Iu)
D	2
CK	1
PR	2

Pin Name	Output Driving Factor (Iu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

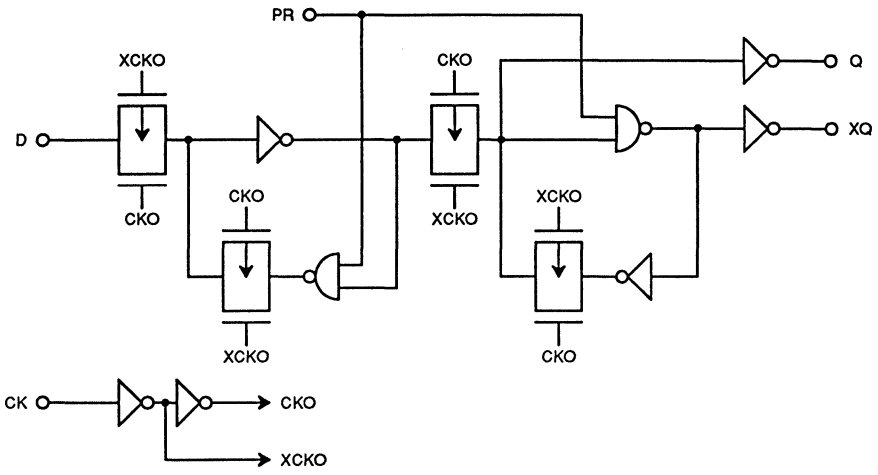
Function Table

Inputs			Outputs	
PR	CK	D	Q	XQ
L	X	X	H	L
H	↓	H	H	L
H	↓	L	L	H

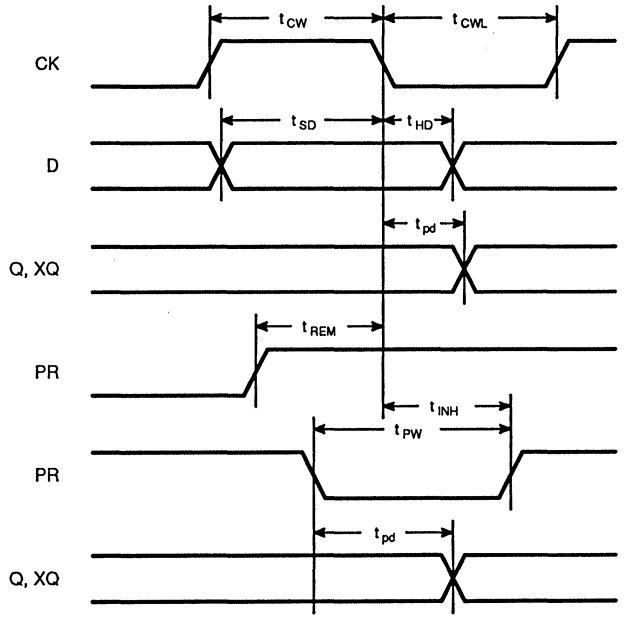
Cell Name

FD3

Equivalent Circuit



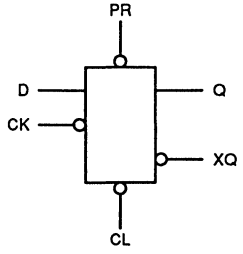
Definitions of Parameters



3

Cell Name	Function	Number of BC
FD4	Non–SCAN Power DFF with Clear and Preset	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.003	0.028	0.911	0.023	0.045	7	CK to Q
1.485	0.023	1.439	0.017	0.034	7	CK to XQ
1.307	0.023	0.772	0.023	0.045	7	CL to Q, XQ
1.314	0.028	0.489	0.017	0.034	7	PR to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWL}	2.5
Data Setup Time	t_{SD}	1.3
Data Hold Time	t_{HD}	0.9
Preset Pulse Width	t_{PW}	2.5
Preset Release Time	t_{REM}	0.3
Preset Hold Time	t_{INH}	2.3
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	0.6
Clear Hold Time	t_{INH}	2.0

Pin Name	Input Loading Factor (Iu)
D	2
CK	1
CL	2
PR	2

Pin Name	Output Driving Factor (Iu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

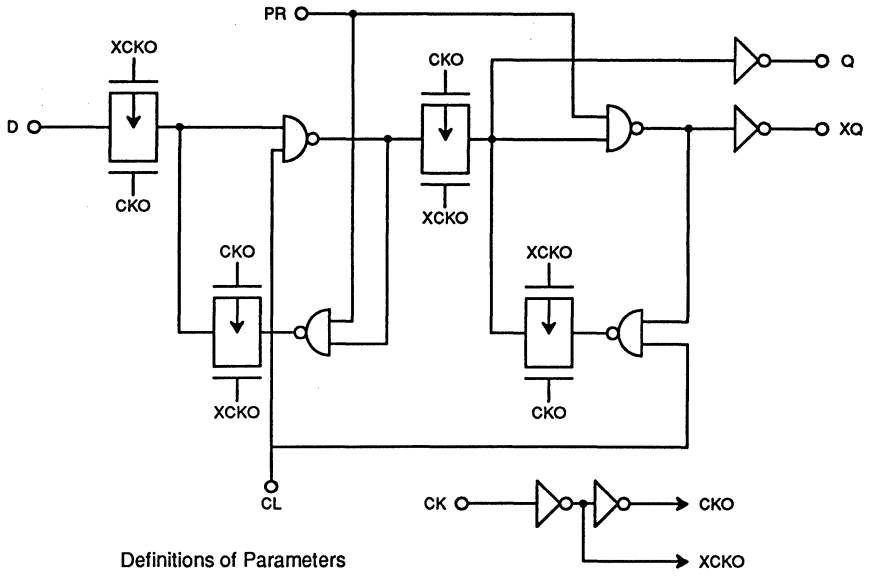
Function Table

Inputs				Outputs	
PR	CL	CK	D	Q	XQ
L	H	X	X	H	L
H	L	X	X	L	H
H	H	↓	H	H	L
H	H	↓	L	L	H

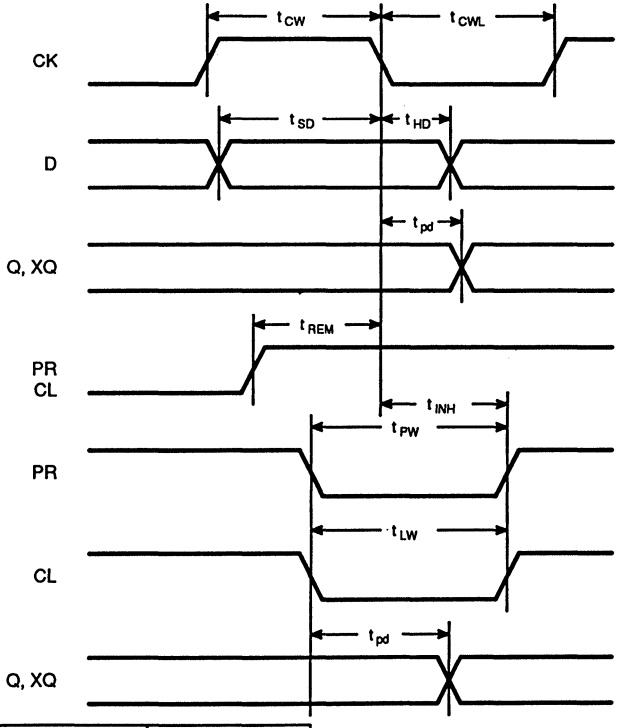
Cell Name

FD4

Equivalent Circuit

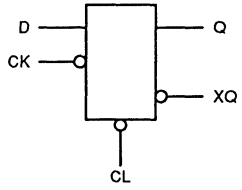


Definitions of Parameters



Cell Name	Function	Number of BC
FD5	Non–SCAN Power DFF with CLEAR	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.997	0.032	0.904	0.023	0.045	7	CK to Q
1.360	0.032	1.360	0.017	0.034	7	CK to XQ
1.248	0.032	0.805	0.023	0.045	7	CL to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWL}	2.5
Data Setup Time	t_{SD}	1.3
Data Hold Time	t_{HD}	0.9
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	0.9
Clear Hold Time	t_{INH}	2.7

Pin Name	Input Loading Factor (Iu)
D	2
CK	1
CL	2

Pin Name	Output Driving Factor (Iu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

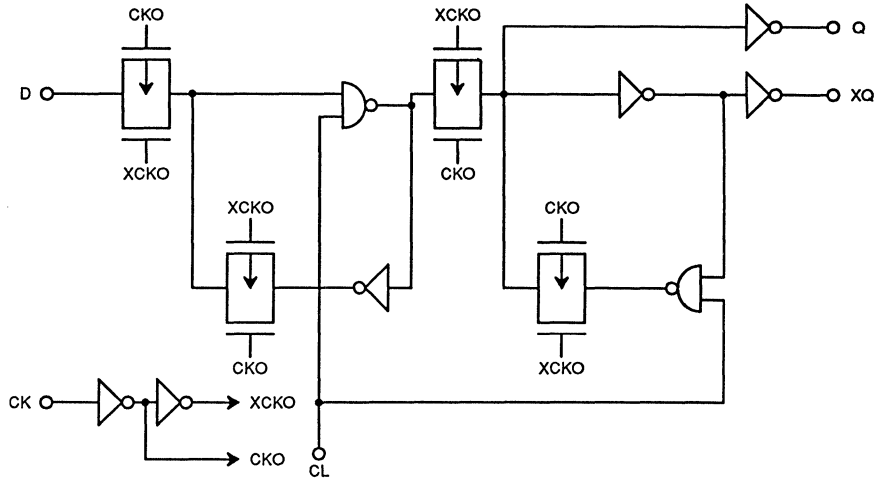
Function Table

Inputs			Outputs	
CL	CK	D	Q	XQ
L	X	X	L	H
H	↓	H	H	L
H	↓	L	L	H

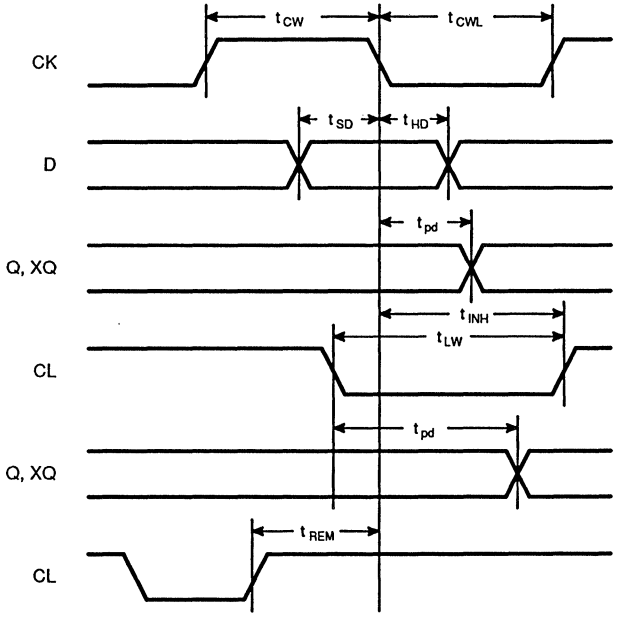
Cell Name

FD5

Equivalent Circuit



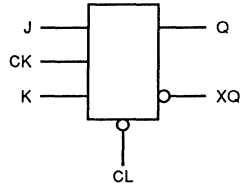
Definitions of Parameters



3

Cell Name	Function	Number of BC
FJD	Non–SCAN Positive edge clocked Power JKFF with Clear	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.323	0.032	1.564	0.023	0.039	7	CK to Q
2.343	0.032	1.314	0.023	0.039	7	CK to XQ
1.267	0.032	0.680	0.023	0.039	7	CL to Q, XQ

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	3.3
Clock Pause Time	t_{CWH}	3.3
J, K Setup Time	t_{SD}	1.5
J, K Hold Time	t_{HD}	0.8
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.5
Clear Hold Time	t_{INH}	2.7

Pin Name	Input Loading Factor (Iu)
CL	2
J	1
K	1
CK	1

Pin Name	Output Driving Factor (Iu)
Q	36
XQ	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

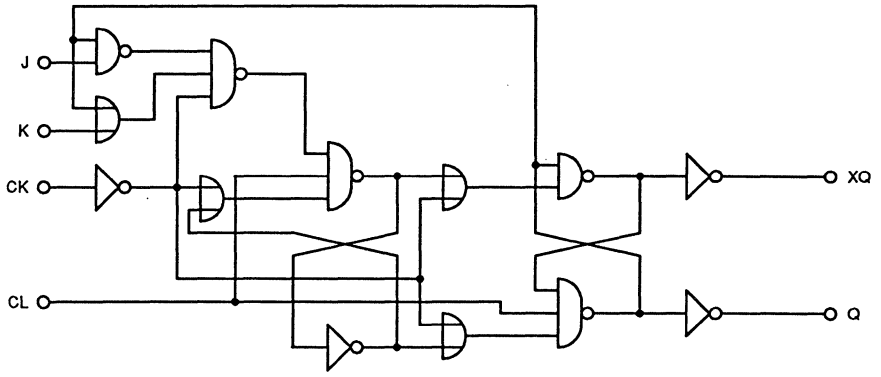
Function Table

Inputs				Outputs	
CL	CK	J	K	Q	XQ
L	H	X	X	L	H
H	↑	L	L	Q0	XQ0
H	↑	L	H	L	H
H	↑	H	L	H	L
H	↑	H	H	XQ0	Q0

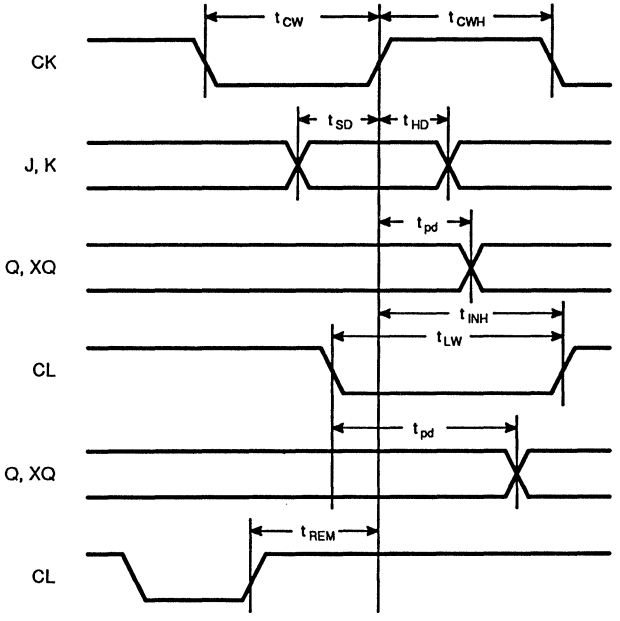
Cell Name

FJD

Equivalent Circuit



Definitions of Parameters



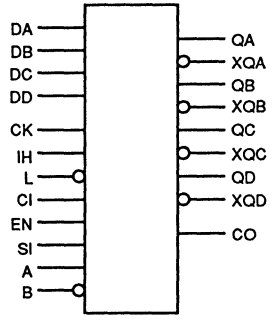
3

Scan Counter Family

Page	Unit Cell Name	Function	Basic Cells
3–211	SC7	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62
3–216	SC8	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66
3–221	SC43	Scan 4-bit Synchronous Binary Up Counter with Asynchronous Clear	59
3–225	SC47	Scan 4-bit Synchronous Binary Up/down Counter	78

Cell Name	Function	Number of BC
SC7	SCAN 4–bit Synchronous Binary Up Counter with Parallel Load	62

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.743	0.032	1.611	0.028	0.067	7	CK,IH to Q
3.056	0.032	2.818	0.028	0.067	7	CK,IH to XQ
4.119	0.032	2.766	0.017	–	–	CK,IH to CO
1.056	0.032	0.053	0.017	–	–	CI to CO

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	4.2
Clock Pause Time	t_{CWH}	4.2
Data Setup Time	t_{SD}	1.2
Data Hold Time	t_{HD}	2.0
Load Setup Time	t_{SL}	3.7
Load Hold Time	t_{HL}	2.1
CI Setup Time	t_{SC}	4.2
CI Hold Time	t_{HC}	1.6
EN Setup Time	t_{SE}	4.2
EN Hold Time	t_{HE}	1.6

Pin Name	Input Loading Factor (Iu)
D	1
CK	1
IH	1
L	1
CI	2
EN	1
SI	1
A,B	1

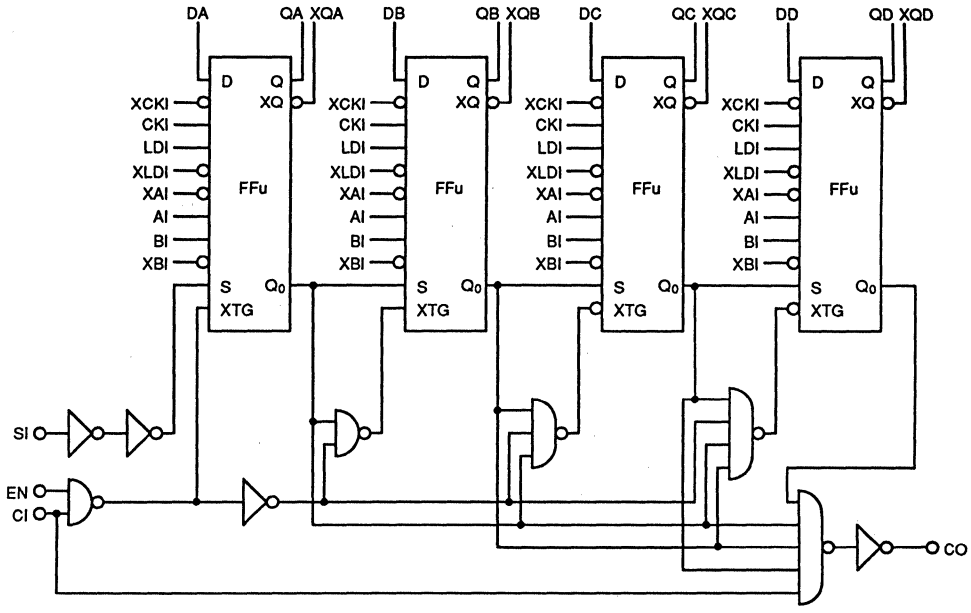
Pin Name	Output Driving Factor (Iu)
Q	36
XQ	36
CO	36

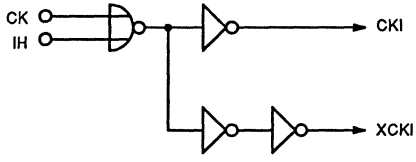
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

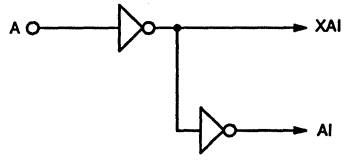
Cell Name

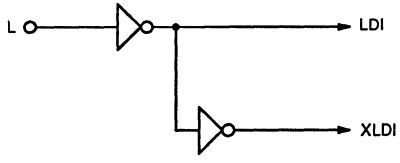
SC7

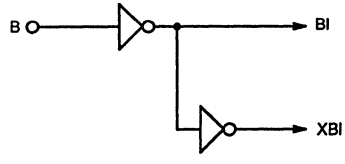
Equivalent Circuit









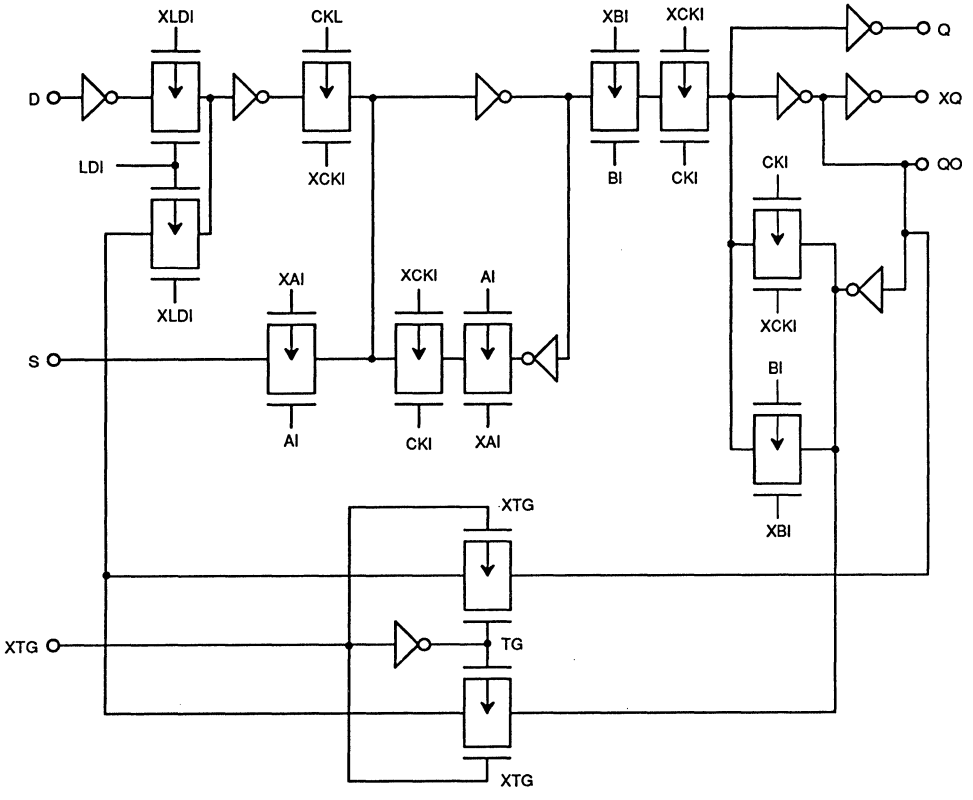


3

Cell Name

SC7

Equivalent Circuit (FFu)

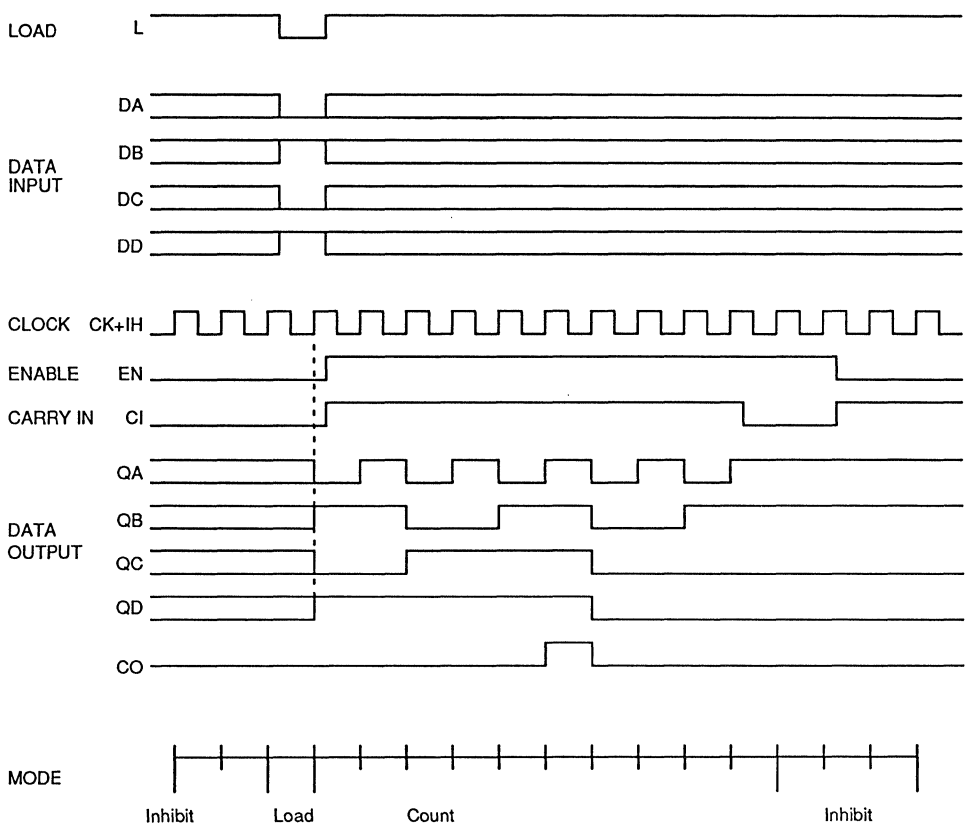


3

Cell Name

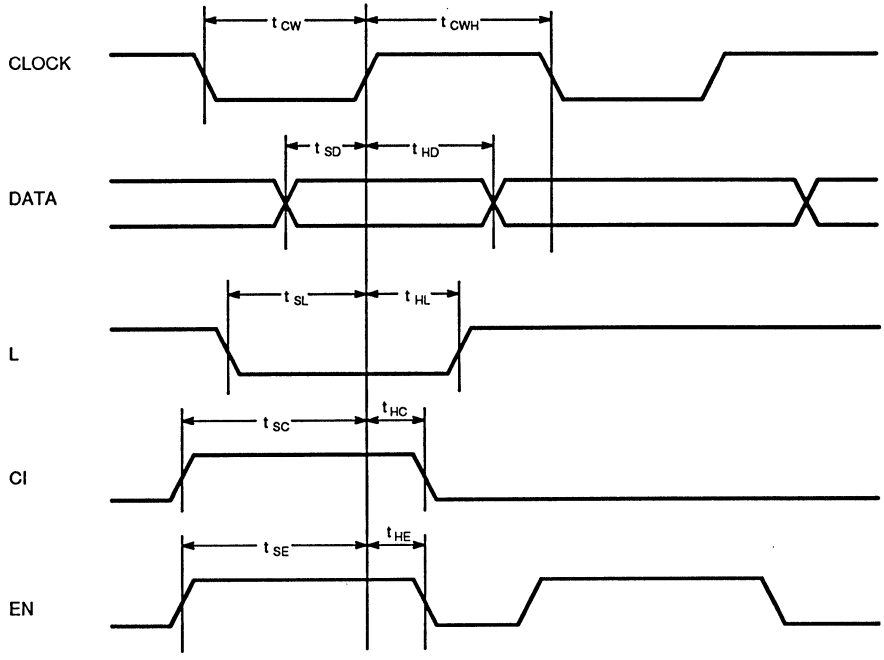
SC7

Function



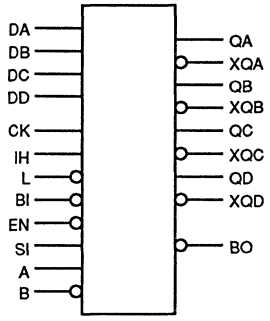
Definitions of Parameters

i) CLOCK MODE



Cell Name	Function	Number of BC
SC8	SCAN 4–bit Synchronous Binaly Down Counter with Parallel Load	66

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
1.782	0.028	1.683	0.028	0.062	7	CK,IH to Q
2.323	0.023	2.284	0.017			CK,IH to XQ
3.386	0.032	4.422	0.017			CK,IH to BO
0.786	0.032	1.201	0.017			BI to BO

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	4.0
Clock Pause Time	t_{CWH}	4.0
Data Setup Time	t_{SD}	1.2
Data Hold Time	t_{HD}	2.0
Load Setup Time	t_{SL}	3.7
Load Hold Time	t_{HL}	2.1
EN Setup Time	t_{SE}	4.8
EN Hold Time	t_{HE}	1.1
BI Setup Time	t_{SB}	4.8
BI Hold Time	t_{HB}	1.1

Pin Name	Input Loading Factor (lu)
D	1
CK	1
IH	1
L	1
BI	2
EN	1
SI	1
A,B	1

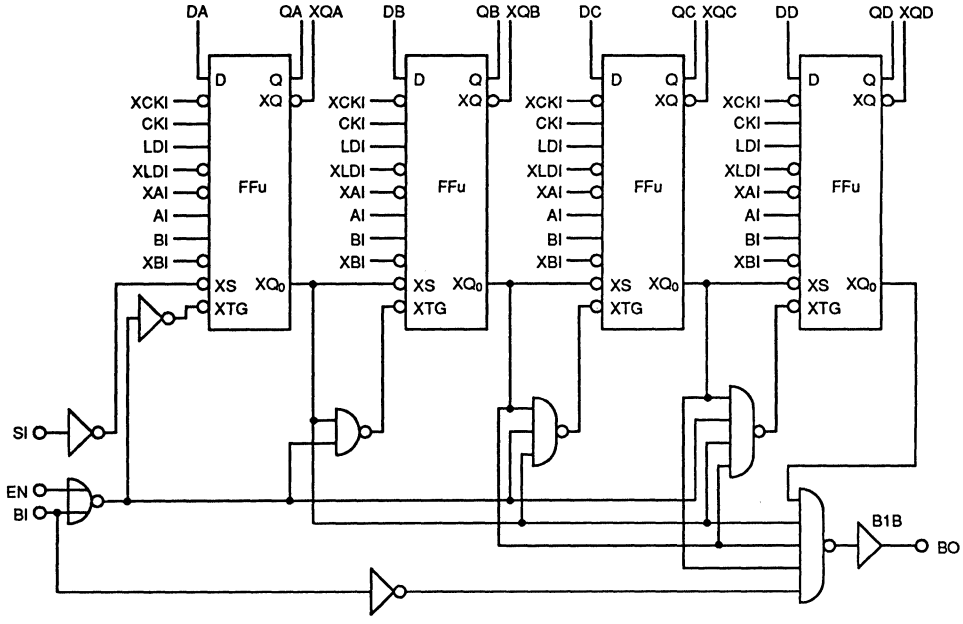
Pin Name	Output Driving Factor (lu)
Q	36
XQ	36
BO	36

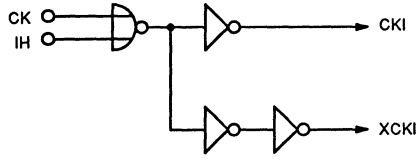
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

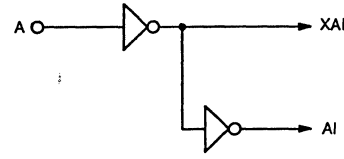
Cell Name

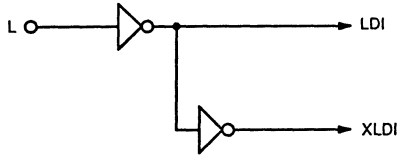
SC8

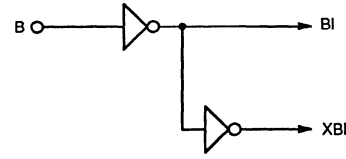
Equivalent Circuit







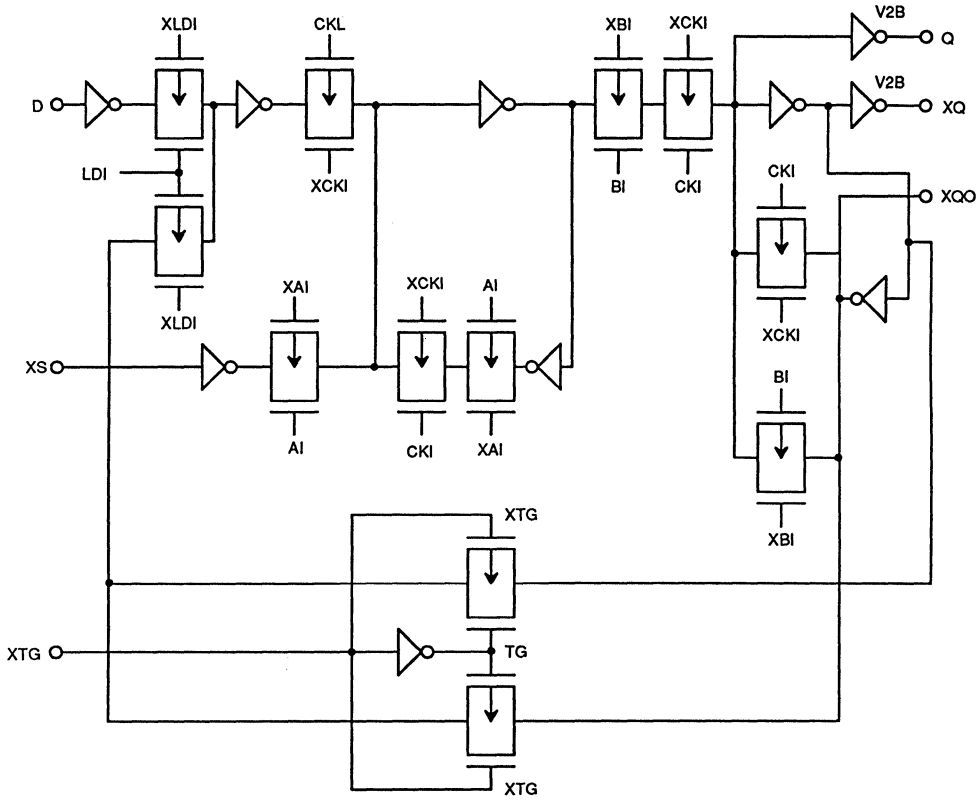




Cell Name

SC8

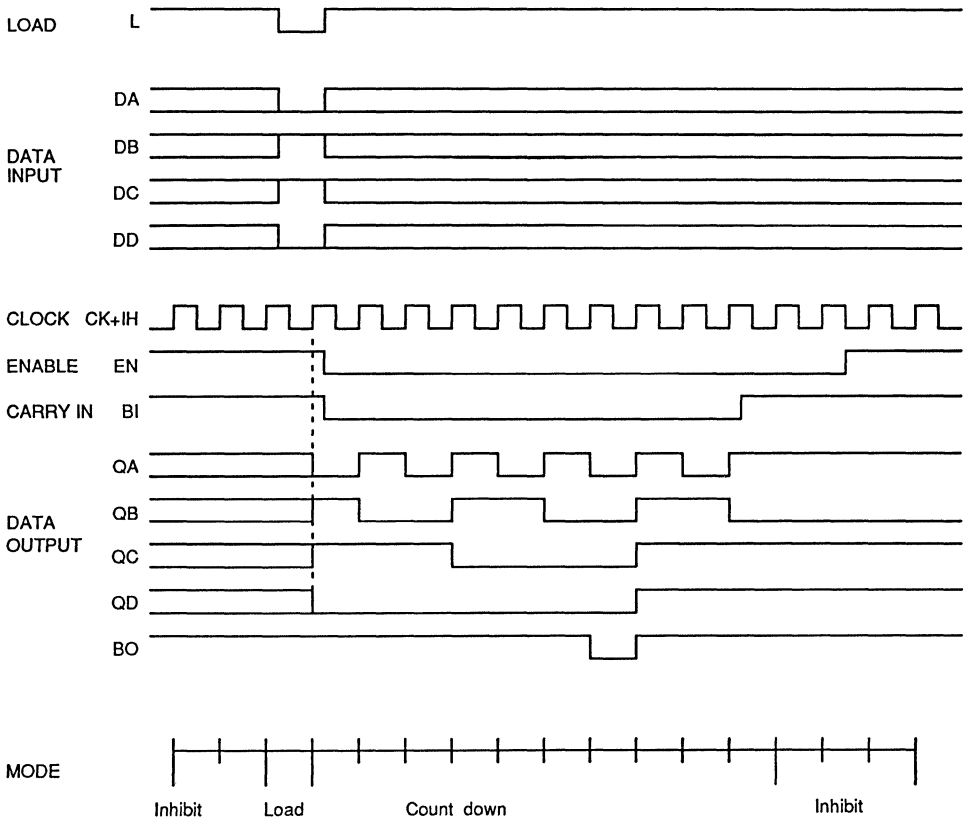
Equivalent Circuit (FFu)



Cell Name

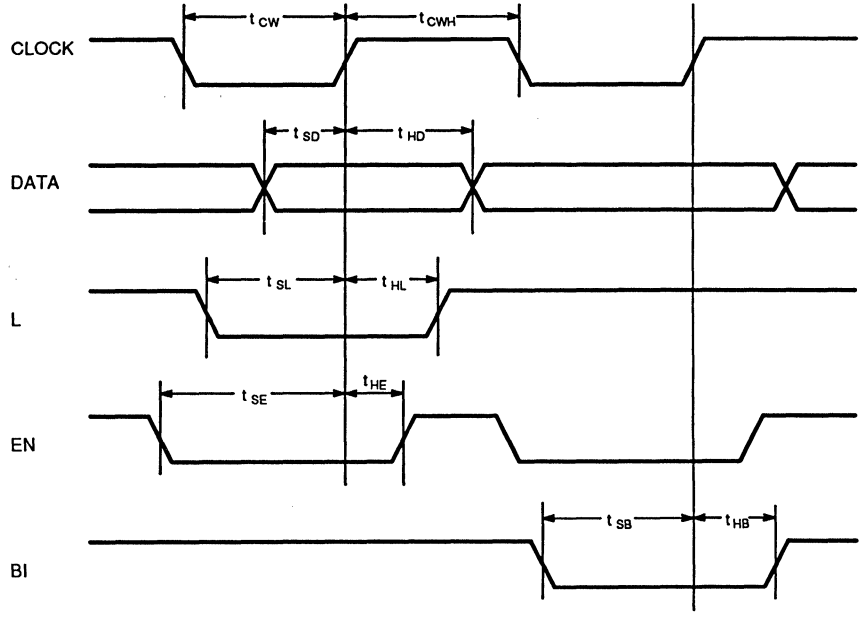
SC8

Function



Definitions of Parameters

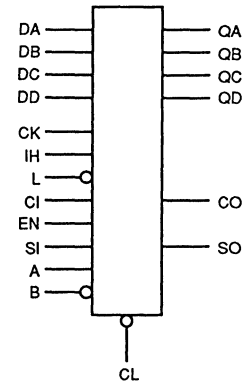
i) CLOCK MODE



3

Cell Name	Function	Number of BC
SC43	SCAN 4–bit Synchronous Binary Up Counter with Asynchronous Clear	59

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
2.257	0.060	2.172	0.039	0.056	4	CK to Q
2.719	0.060	2.904	0.039	0.056	4	CK to CO
–	–	1.380	0.039	0.056	4	CL to Q
0.964	0.060	0.660	0.039	0.056	4	CI to CO
–	–	1.888	0.039	0.056	4	CL to CO

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	3.0
Clock Pause Time	t_{CWH}	4.3
Data Setup Time	t_{SD}	1.2
Data Hold Time	t_{HD}	1.3
Load Setup Time	t_{SL}	1.8
Load Hold Time	t_{HL}	1.5
CI Setup Time	t_{SC}	2.4
CI Hold Time	t_{HC}	1.1
EN Setup Time	t_{SE}	2.4
EN Hold Time	t_{HE}	1.1
Clear Pulse Width	t_{LW}	3.7
Clear Release Time	t_{REM}	0.9
Clear Hold Time	t_{INH}	3.4

Pin Name	Input Loading Factor (lu)
D	2
CK, IH	1
L, CL, SI	1
EN	1
A, B, CI	2

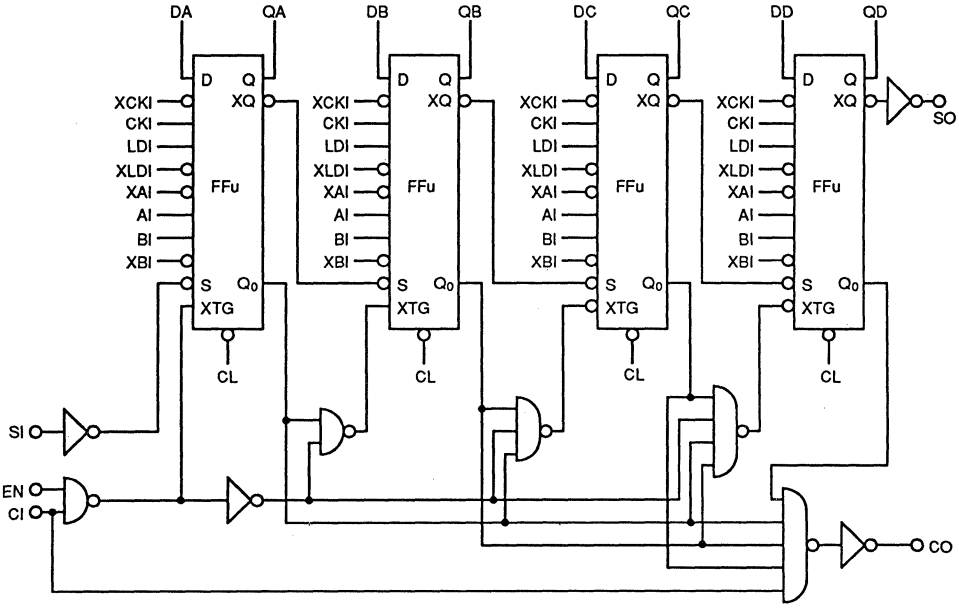
Pin Name	Output Driving Factor (lu)
Q	18
CO	18
SO	18

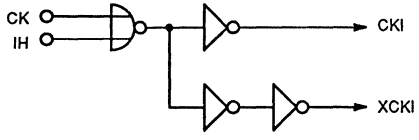
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

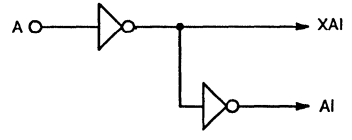
Cell Name

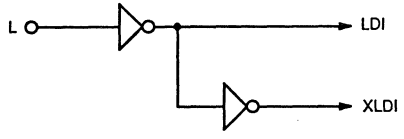
SC43

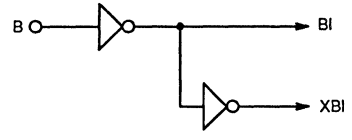
Equivalent Circuit

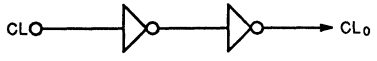








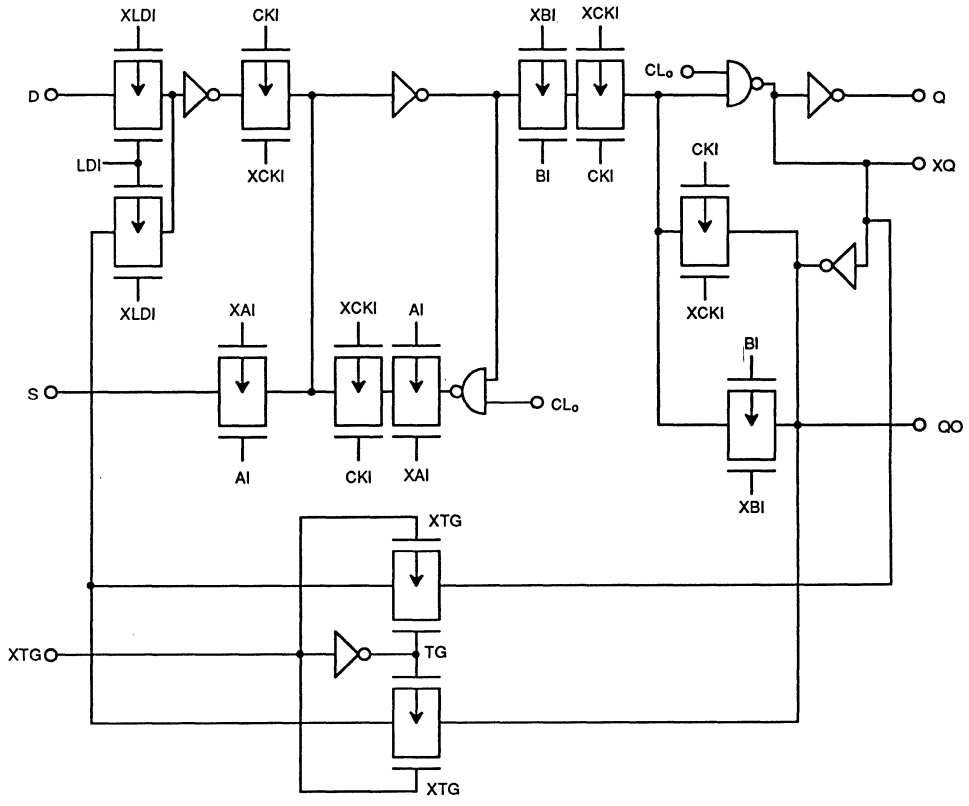




Cell Name

SC43

Equivalent Circuit (FFu)

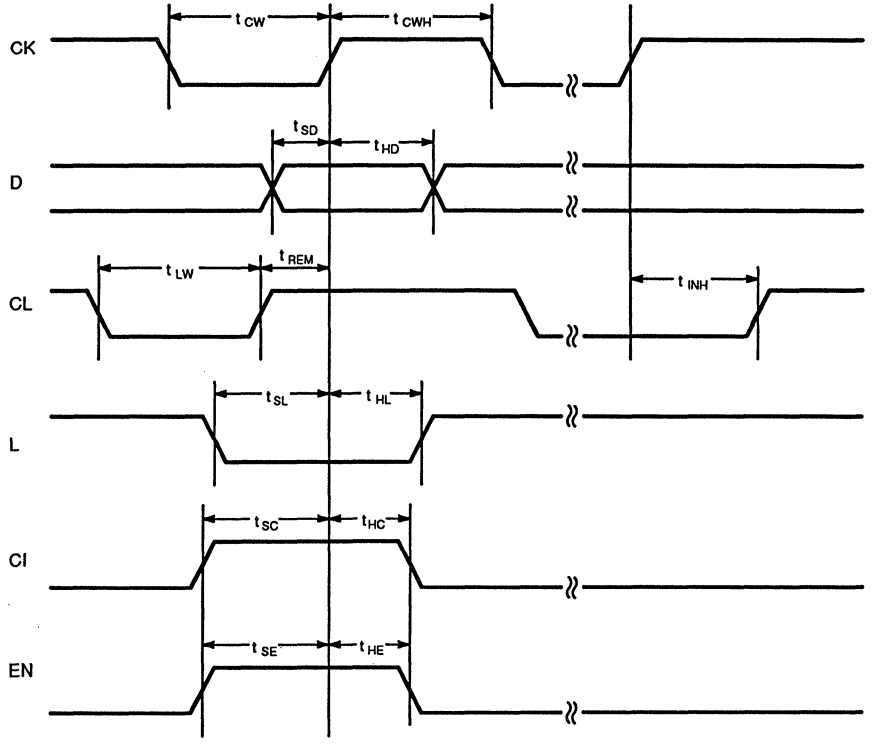


3

Cell Name

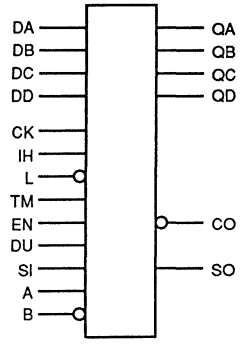
SC43

Definition of Parameters



Cell Name	Function	Number of BC
SC47	SCAN 4–bit Synchronous Binary Up/Down Counter	78

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.376	0.060	2.482	0.084	0.112	4	CK to Q
3.234	0.060	4.594	0.039			CK to CO
1.241	0.060	1.551	0.039			DU to CO

Parameter	Symbol	Typ (ns) *
Clock Pulse Width (H)	t_{CW}	3.0
Clock Pause Time (L)	t_{CWH}	4.3
Data Setup Time	t_{SD}	1.2
Data Hold Time	t_{HD}	1.3
EN Setup Time	t_{SE}	2.4
EN Hold Time	t_{HE}	1.1
DU Input Setup Time	t_{SU}	1.1
DU Input Hold Time	t_{HU}	2.4
Load Pulse Width	t_{LW}	3.7
Clear Release Time	t_{REM}	0.9
Clear Hold Time	t_{INH}	3.4

Pin Name	Input Loading Factor (lu)
D	2
CK, IH, TM, L	1
EN	3
DU, A, B	1
SI	2

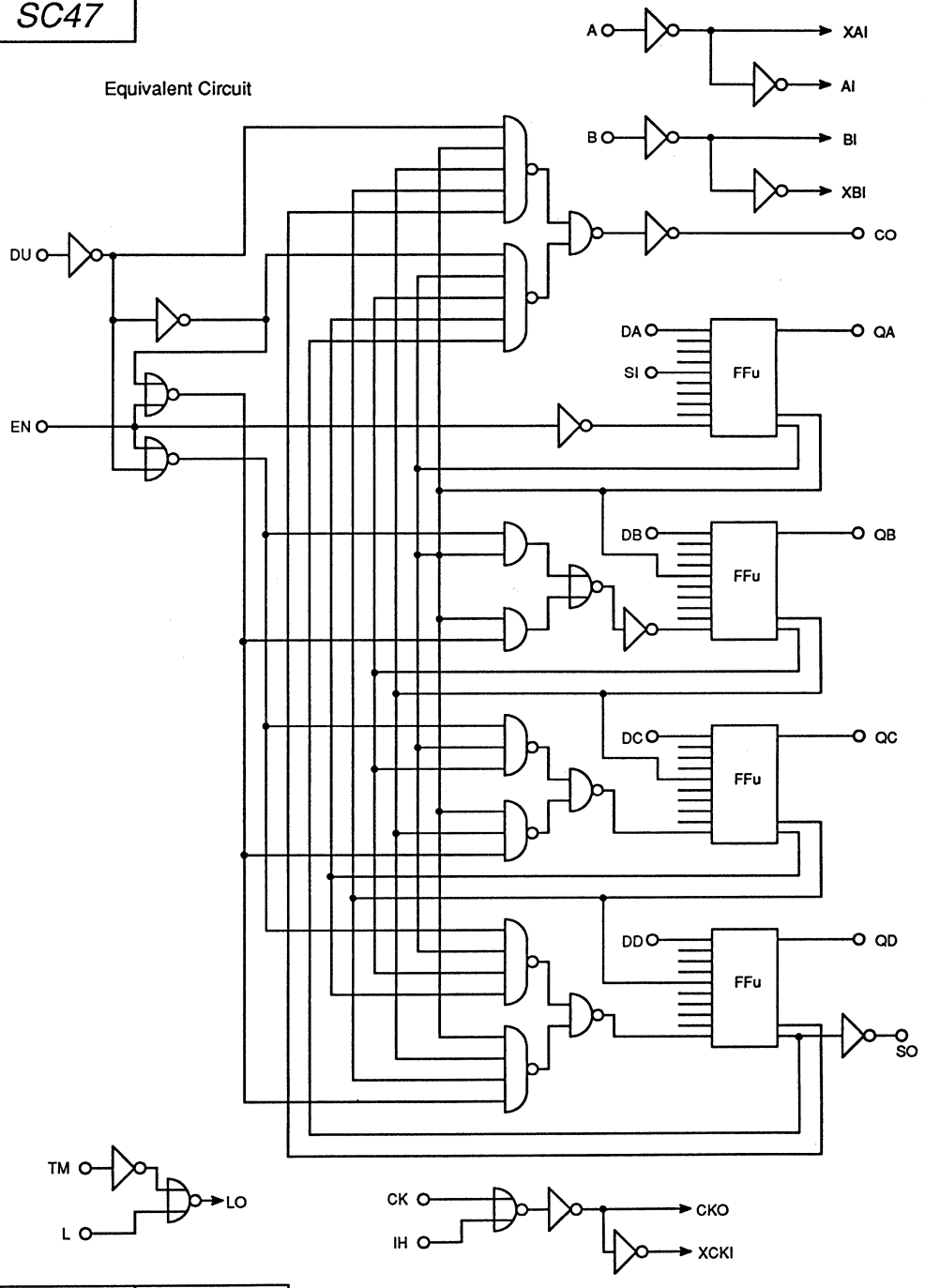
Pin Name	Output Driving Factor (lu)
Q	18
SO	18
CO	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name

SC47

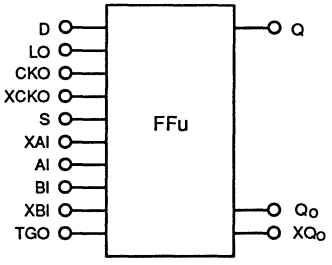
Equivalent Circuit



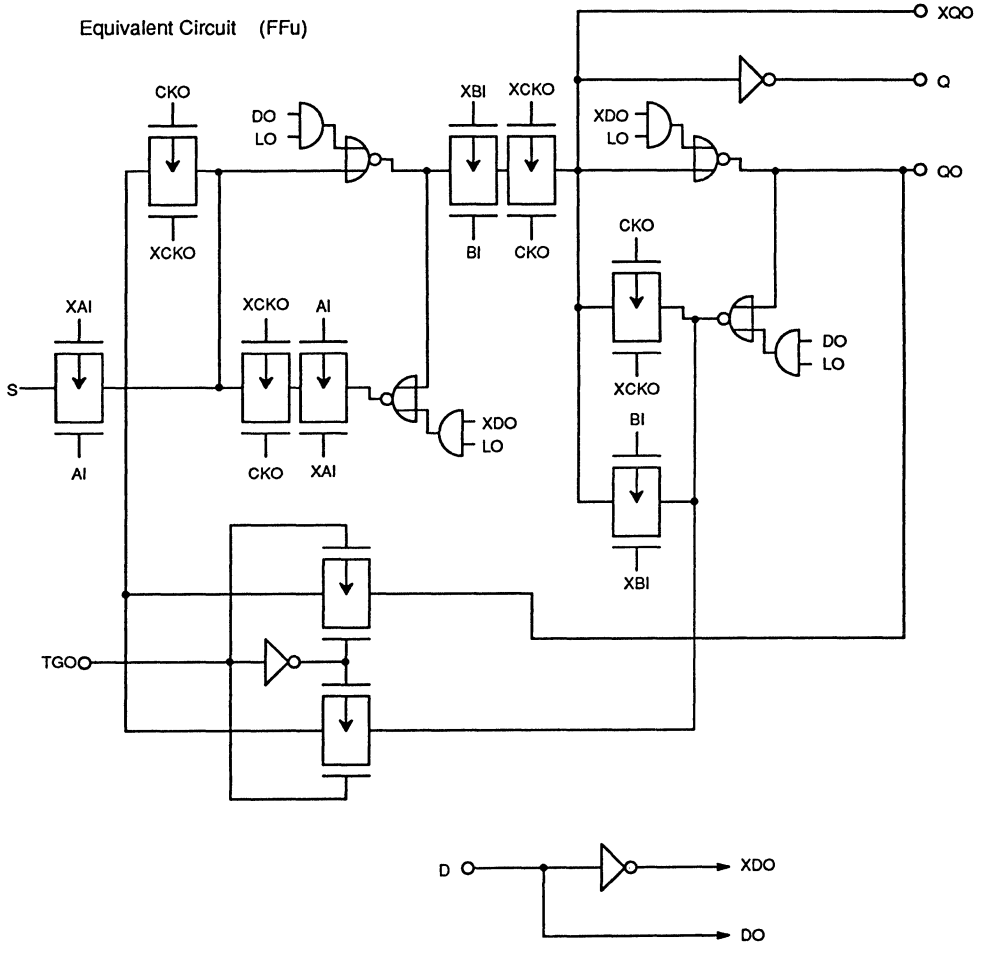
Cell Name

SC47

Symbol

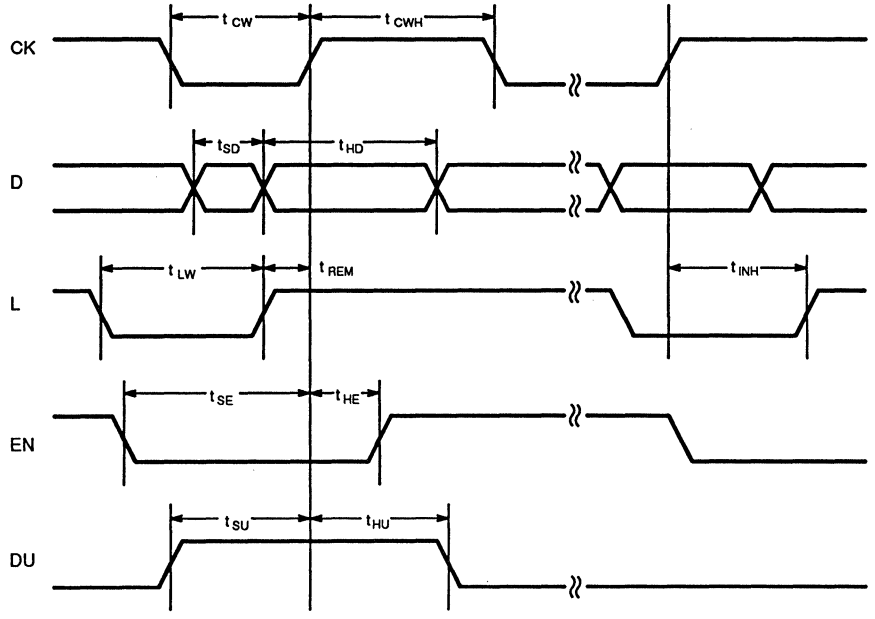


Equivalent Circuit (FFu)



3

Definition of Parameters



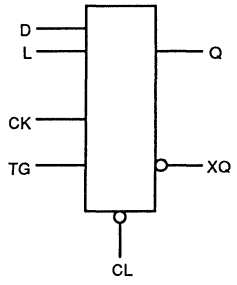
3

Non-Scan Counter Family

Page	Unit Cell Name	Function	Basic Cells
3–231	C11	Non-Scan Flip–Flop for Counter	11
3–233	C41	Non-Scan 4-bit Binary Asynchronous Counter	24
3–236	C42	Non-Scan 4-bit Binary Synchronous Counter	32
3–239	C43	Non-Scan 4-bit Binary Synchronous Up Counter	48
3–243	C45	Non-Scan 4-bit Binary Synchronous Up Counter	48
3–247	C47	Non-Scan 4-bit Binary Synchronous Up/Down Counter	68

Cell Name	Function	Number of BC
C11	Non–SCAN Flip–Flop for Counter	11

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.003	0.060	0.924	0.045			CK to Q
1.340	0.060	1.571	0.045			CK to XQ
1.386	0.060	0.918	0.045			CL to Q,XQ

Parameter		Symbol	Typ (ns) *
Clock Pulse Width		t_{CW}	2.5
Clock Pause Time		t_{CWH}	2.5
Clear Pulse Width		t_{LW}	2.5
Clear Release Time		t_{REM}	0.6
Clear Hold Time		t_{INH}	0.3
Load Setup Time	(CK)	t_{SL}	1.4
Load Hold Time	(CK)	t_{HL}	0.3
Data Setup Time	(CK)	t_{SD}	1.5
Data Hold Time	(CK)	t_{HD}	0.3
TG Setup Time	(CK)	t_{ST}	1.8
TG Hold Time	(CK)	t_{HT}	0.0

Pin Name	Input Loading Factor (lu)
L	2
TG	2
CL	2
D,CK	1

Pin Name	Output Driving Factor (lu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

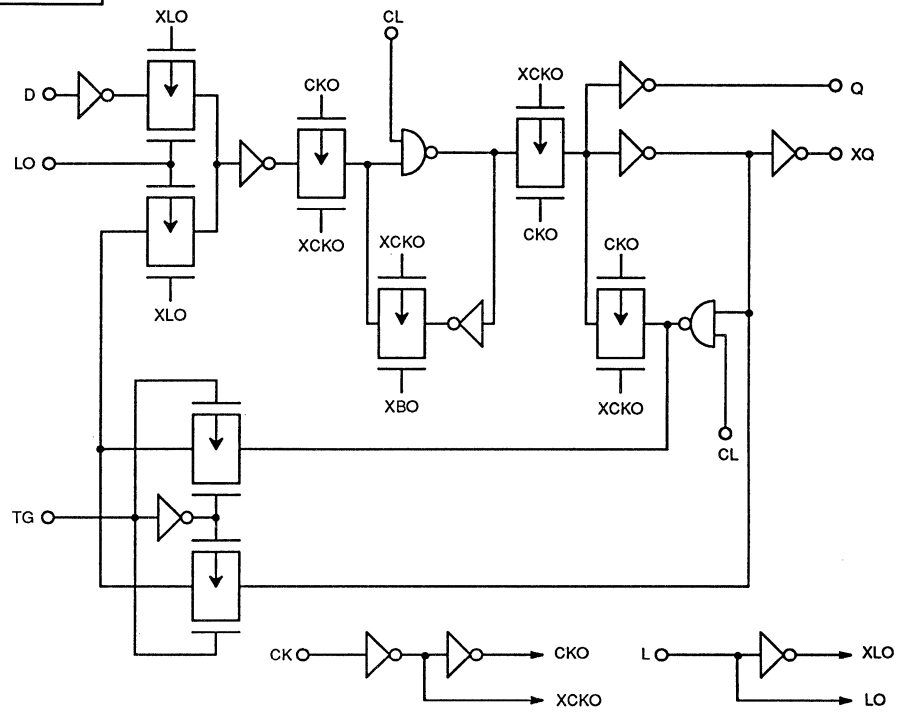
L	D	TG	CL	CK	Q (Q_0)
X	X	X	L	X	L
H	H	X	H	↑	H
H	L	X	H	↑	L
L	X	L	H	↑	Q (Q_0)
L	X	H	H	↑	$\overline{Q}$ ($\overline{Q_0}$)

3

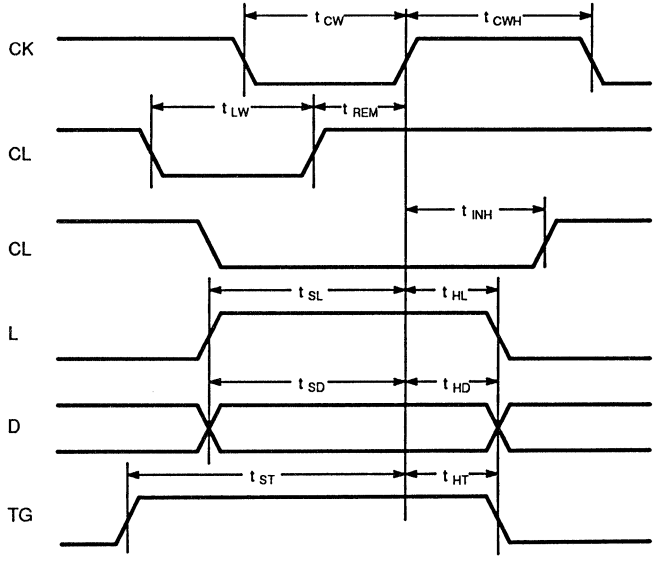
Cell Name

C11

Equivalent Circuit

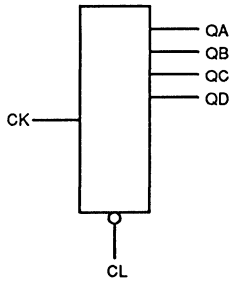


Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
C41	Non–SCAN 4–bit Binary Asynchronous Counter	24

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.056	0.051	0.984	0.045	–	–	CK to QA
1.941	0.051	1.736	0.045	–	–	CK to QB
2.713	0.051	2.508	0.045	–	–	CK to QC
3.485	0.051	3.274	0.045	–	–	CK to QD
–	–	2.211	0.045	–	–	CL to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Clear Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.3
Clear Hold Time	t_{INH}	4.0

Pin Name	Input Loading Factor (lu)
CK	1
CL	1

Pin Name	Output Driving Factor (lu)
Q	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

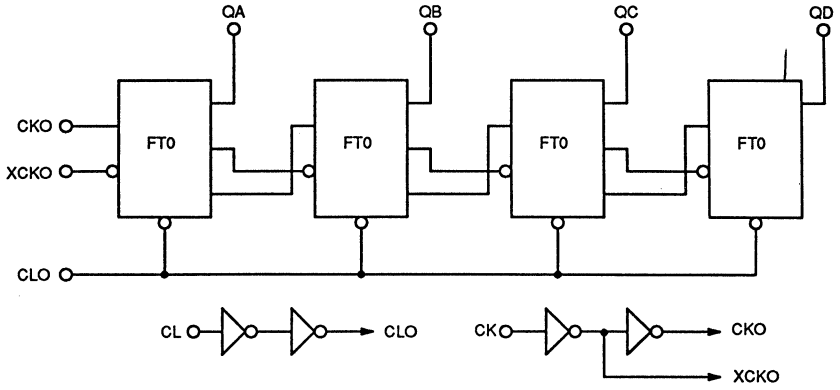
Function Table

Inputs		Output
CL	CK	Q
H	↑	Count up
L	X	L

Cell Name

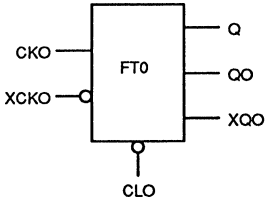
C41

Equivalent Circuit



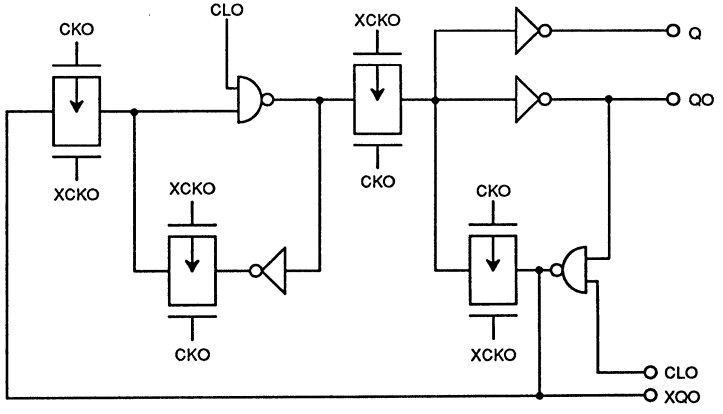
FT0 (Flip–Flop for Counter) (not Uint Cell)

Symbol



Function Table

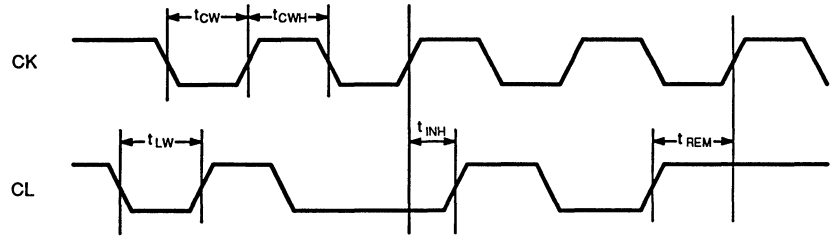
CLO	CKO	Q
L	X	L
H	↑	$\overline{Qn-1}$



Cell Name

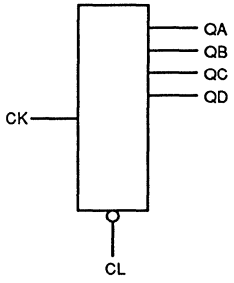
C41

Definition of Parameters



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
C42	Non–SCAN 4–bit Binary Synchronous Counter	32

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.683	0.051	1.234	0.039	0.056	4	CK to Q
–	–	1.776	0.039	0.056	4	CL to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Clock Pulse Width	t_{LW}	2.5
Clear Release Time	t_{REM}	1.3
Clear Hold Time	t_{INH}	4.0

Pin Name	Input Loading Factor (lu)
CL	1
CK	1

Pin Name	Output Driving Factor (lu)
Q	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

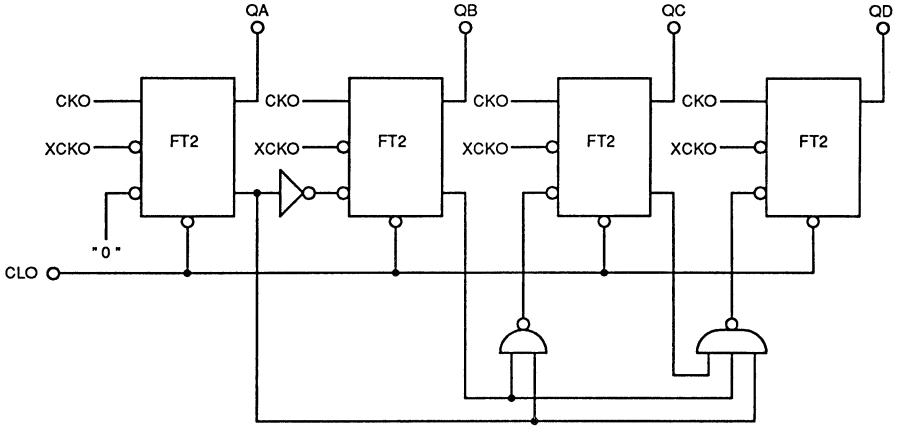
Function Table

Inputs		Outputs
CL	CK	Q
H	↑	Count up
L	X	L

Cell Name

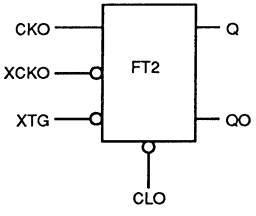
C42

Equivalent Circuit



FT2 (Flip–Flop for Counter) (not Unit Cell)

Symbol



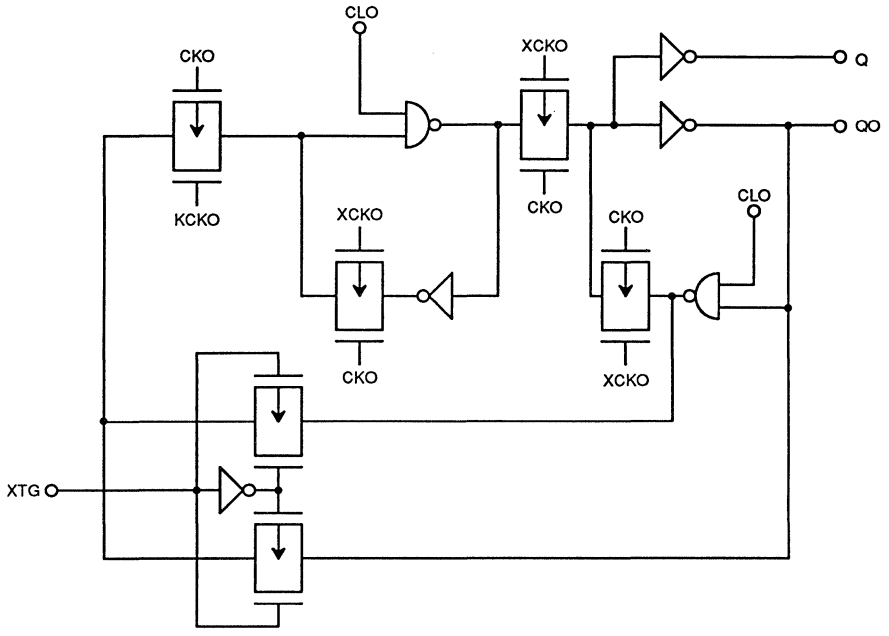
Function Table

Inputs			Outputs
CLO	XTG	CKO	Q (Q_0)
L	X	X	L
H	H	↑	Qn–1
H	L	↑	$\overline{Qn-1}$

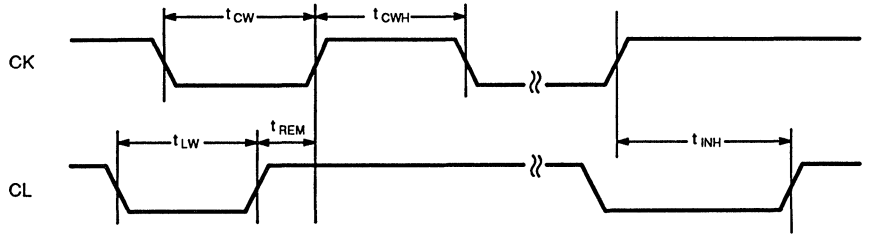
Cell Name

C42

Equivalent Circuit of FT2

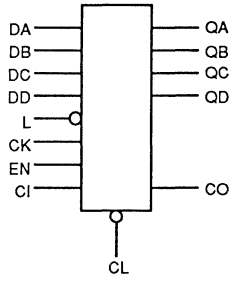


Definition of Parameters



Cell Name	Function	Number of BC
C43	Non–SCAN 4–bit Binary Synchronous Up Counter	48

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.564	0.060	1.267	0.039			CK to Q
2.957	0.060	1.881	0.039			CK to CO
0.845	0.060	0.429	0.039			CI to CO
–	–	2.053	0.039			CL to Q
–	–	1.393	0.039			CL to CO

Pin Name	Input Loading Factor (Iu)
D	1
L,EN	1
CK,CL	1
CI	2

Pin Name	Output Driving Factor (Iu)
Q	18
CO	18

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	4.0
Data Setup Time	t_{SD}	1.6
Data Hold Time	t_{HD}	1.8
Load Setup Time	t_{SL}	2.7
Load Hold Time	t_{HL}	0.8
CI Setup Time	t_{SC}	2.6
CI Hold Time	t_{HC}	0.6
EN Setup Time	t_{SE}	2.6
EN Hold Time	t_{HE}	0.6
Clear Pulse Width	t_{LW}	3.3
Clear Release Time	t_{REM}	1.2
Clear Hold Time	t_{INH}	4.9

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

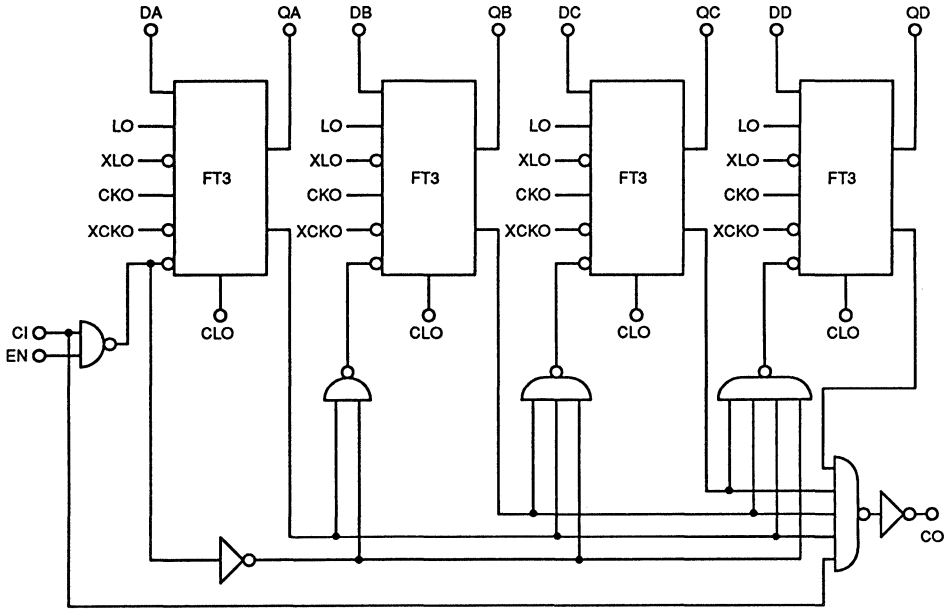
Inputs						Outputs
CL	L	D	EN	CI	CK	Q
L	X	X	X	X	X	L
H	L	H	X	X	↑	H
H	L	L	X	X	↑	L
H	H	X	X	L	X	No Counting
H	H	X	L	X	X	No Counting
H	H	X	H	H	↑	Count up

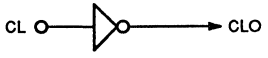
Note : The CO output produces a high level output data when the counter overflows.

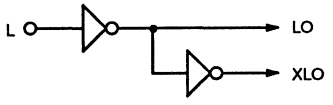
Cell Name

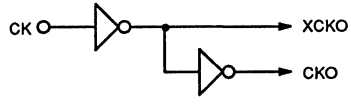
C43

Equivalent Circuit







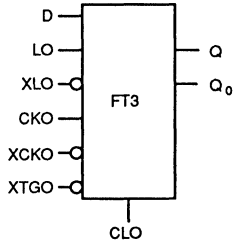


Cell Name

C43

FT3 (Flip–Flop for Counter) (not Unit Cell)

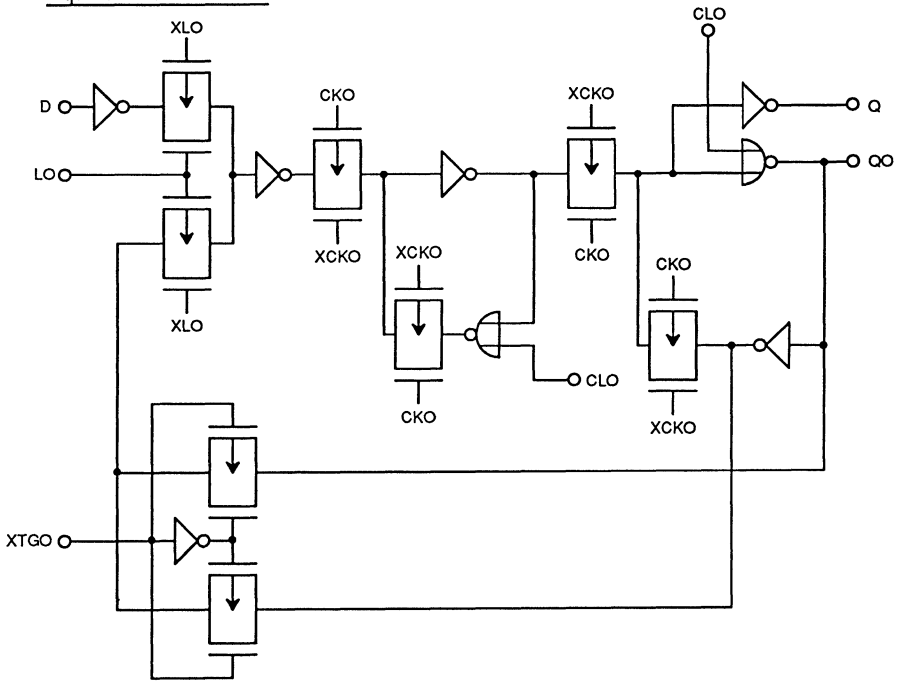
Symbol



Function Table

LO	D	XTGO	CLO	CK	Q (QO)
X	X	X	H	X	L
H	H	X	L	↑	H
H	L	X	L	↑	L
L	X	H	L	↑	Q (QO)
L	X	L	L	↑	$\overline{Q}$ ($\overline{QO}$)

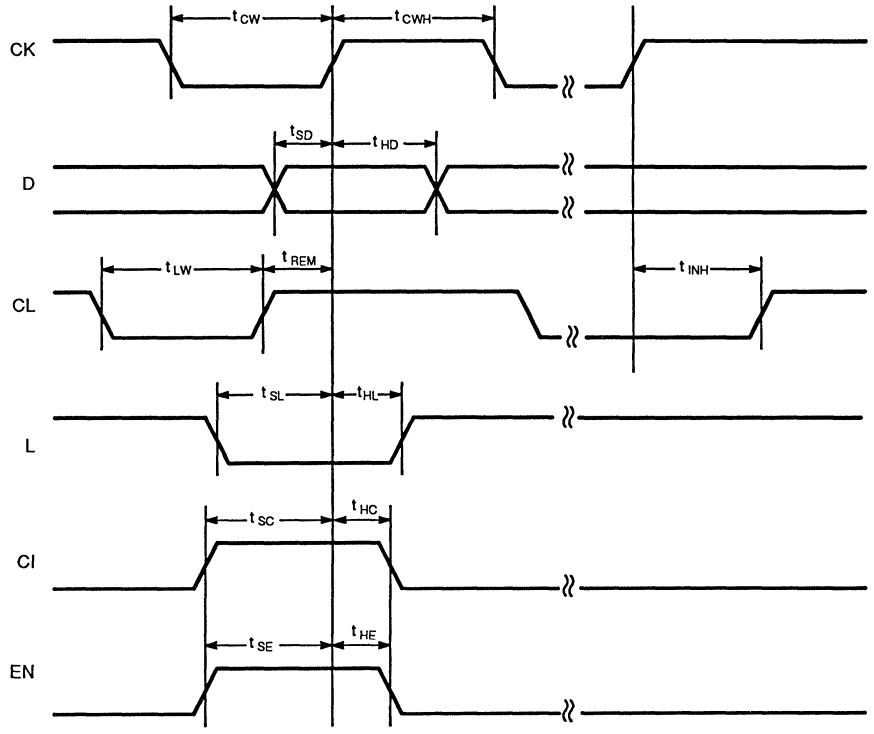
Equivalent Circuit of FT3



Cell Name

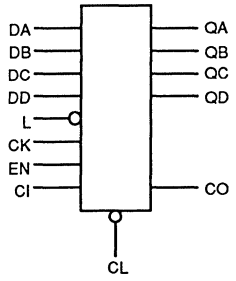
C43

Definition of Parameters



Cell Name	Function	Number of BC
C45	Non–SCAN 4–bit Binary Synchronous Up Counter	48

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.413	0.051	0.990	0.039	0.062	4	CK to Q
2.680	0.064	1.492	0.039			CK to CO
1.010	0.064	0.720	0.039			CI to CO

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Data Setup Time	t_{SD}	2.3
Data Hold Time	t_{HD}	1.3
Load Setup Time	t_{SL}	2.9
Load Hold Time	t_{HL}	1.3
CI Setup Time	t_{SC}	3.9
CI Hold Time	t_{HC}	1.2
EN Setup Time	t_{SE}	3.9
EN Hold Time	t_{HE}	1.2
Clear Setup Time	t_{SR}	2.3
Clear Hold Time	t_{HR}	1.2

Pin Name	Input Loading Factor (lu)
D	1
L,EN	1
CK,CL	1
CI	2

Pin Name	Output Driving Factor (lu)
Q	18
CO	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

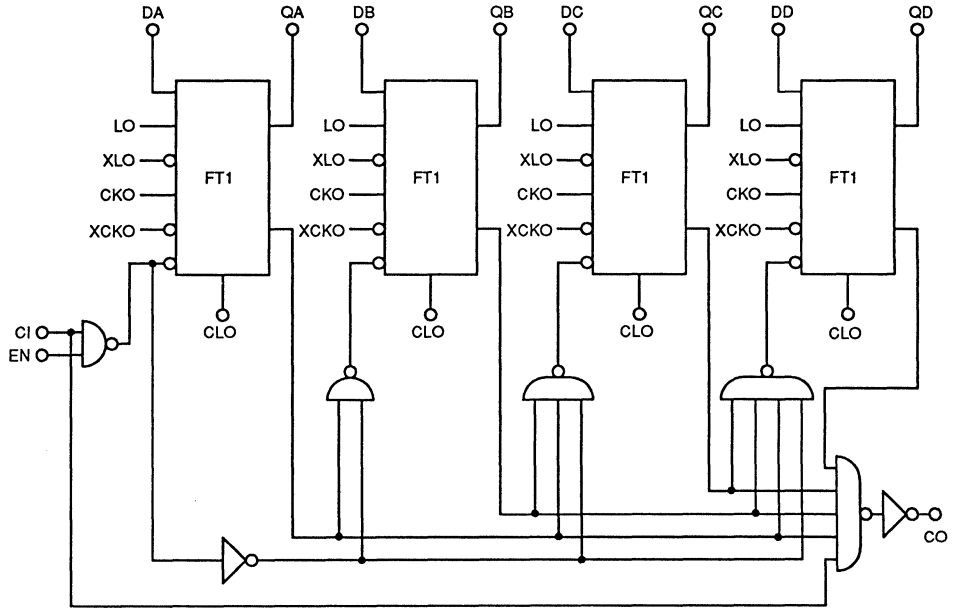
Inputs						Outputs
CL	L	D	EN	CI	CK	Q
L	X	X	X	X	↑	L
H	L	H	X	X	↑	H
H	L	L	X	X	↑	L
H	H	X	X	L	X	No Counting
H	H	X	L	X	X	No Counting
H	H	X	H	H	↑	Count up

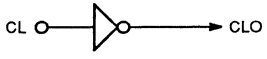
Note : The CO output produces a high level output data when the counter overflows.

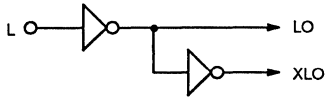
Cell Name

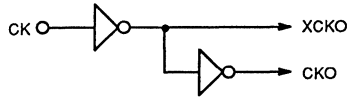
C45

Equivalent Circuit







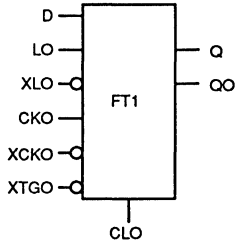


Cell Name

C45

FT1 (Flip–Flop for Counter) (not Unit Cell)

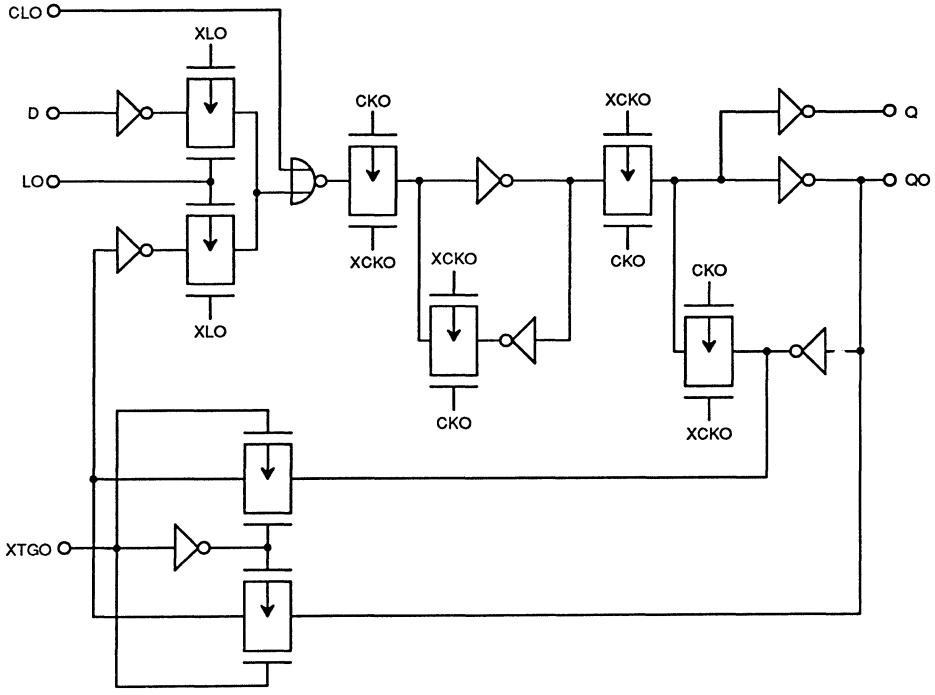
Symbol



Function Table

LO	D	XTGO	CLO	CK	Q (QO)
L	X	X	H	↑	L
H	H	X	L	↑	H
H	L	X	L	↑	L
L	X	H	L	↑	Q (QO)
L	X	L	L	↑	$\overline{Q}$ ($\overline{QO}$)

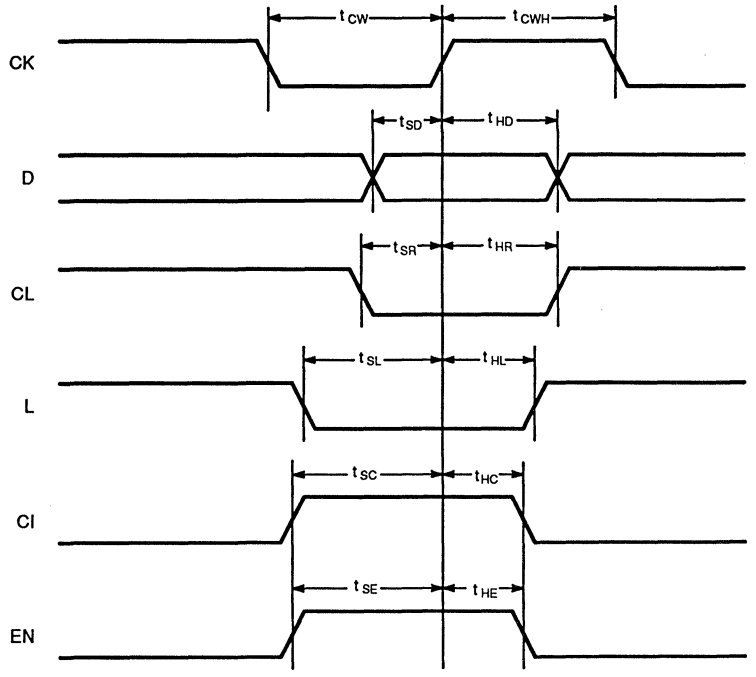
Equivalent Circuit of FT3



Cell Name

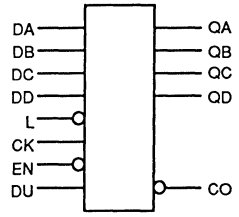
C45

Definition of Parameters



Cell Name	Function	Number of BC
C47	Non–SCAN 4–bit Binary Synchronous Up/Down Counter	68

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.106	0.060	1.894	0.073	0.112	4	CK to Q
2.858	0.041	3.234	0.039			CK to CO
2.647	0.060	2.924	0.073	0.112	4	L to Q
1.307	0.041	1.591	0.039			DU to CO

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	3.3
Clock Pause Time	t_{CWH}	5.3
Data Setup Time	t_{SD}	0.5
Data Hold Time	t_{HD}	1.1
DU Setup Time	t_{SU}	3.2
DU Hold Time	t_{HU}	0.5
EN Setup Time	t_{SE}	2.9
EN Hold Time	t_{HE}	0.8
Load Release Time	t_{REM}	1.4
Load Hold Time	t_{INH}	6.5
Load Pulse Width	t_{LW}	2.5

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Pin Name	Input Loading Factor (lu)
D	1
L	2
DU	1
CK	1
EN	3

Pin Name	Output Driving Factor (lu)
Q	18
CO	18

Function Table

Inputs					Outputs
Q	L	EN	DU	CK	Q
H	L	X	X	X	H
L	L	X	X	X	L
X	H	H	X	↑	No Counting
X	H	L	L	↑	Count Up
X	H	L	H	↑	Count Down

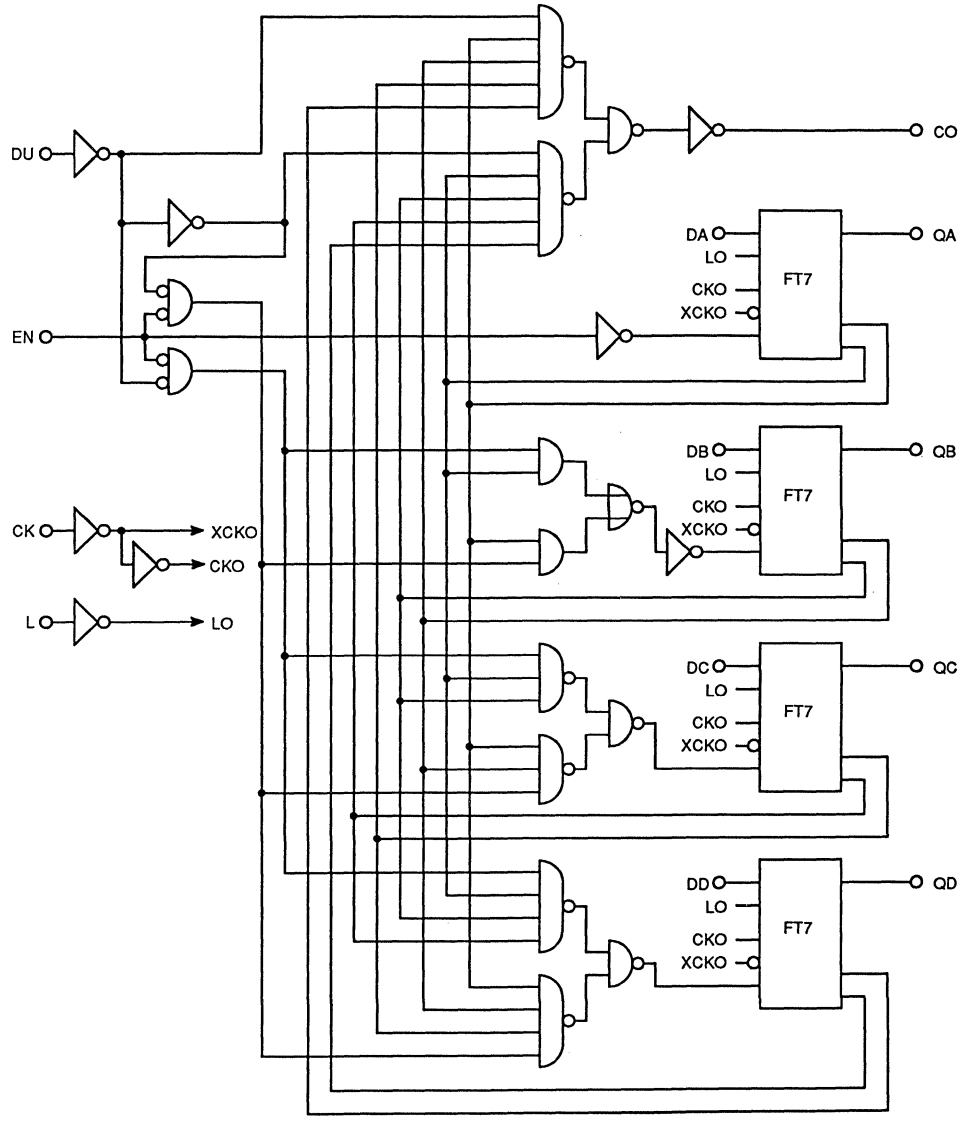
Note : The CO output produces a low level output pulse when the counter overflows or underflows.

3

Cell Name

C47

Equivalent Circuit

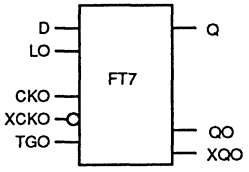


Cell Name

C47

FT7 (Flip–Flop for Counter) (not Unit Cell)

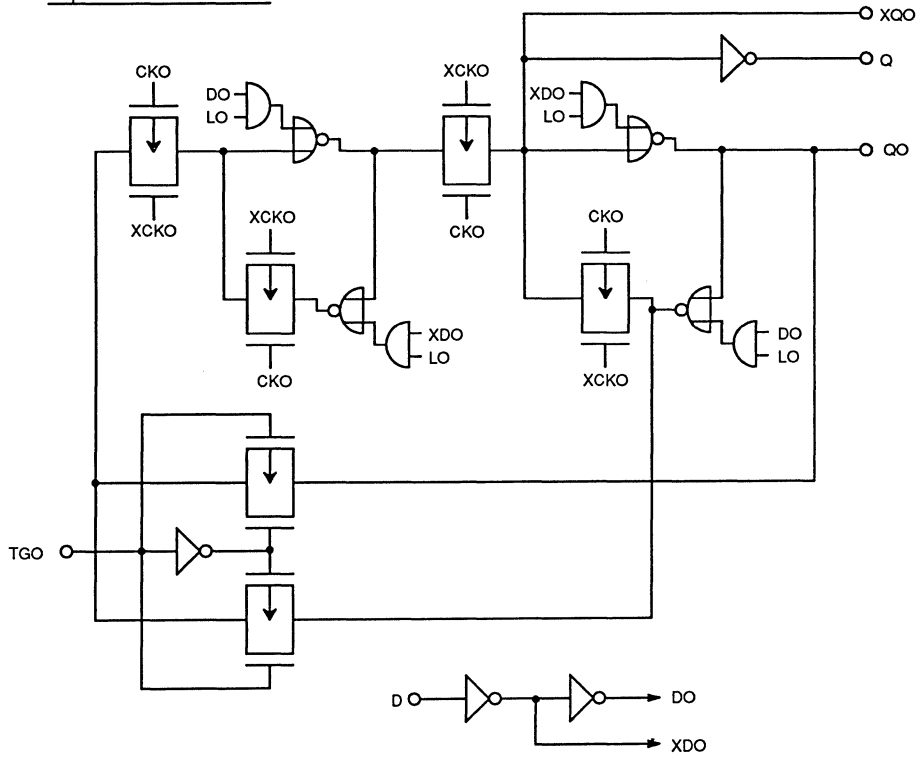
Symbol



Function Table

Inputs				Outputs	
LO	D	TGO	CKO	QO(Q)	$\overline{Q}$(QO)
H	H	X	X	H	L
H	L	X	X	L	H
L	X	L	↑	Qn–1	$\overline{Qn-1}$
L	X	H	↑	$\overline{Qn-1}$	Qn–1

Equivalent Circuit of FT7

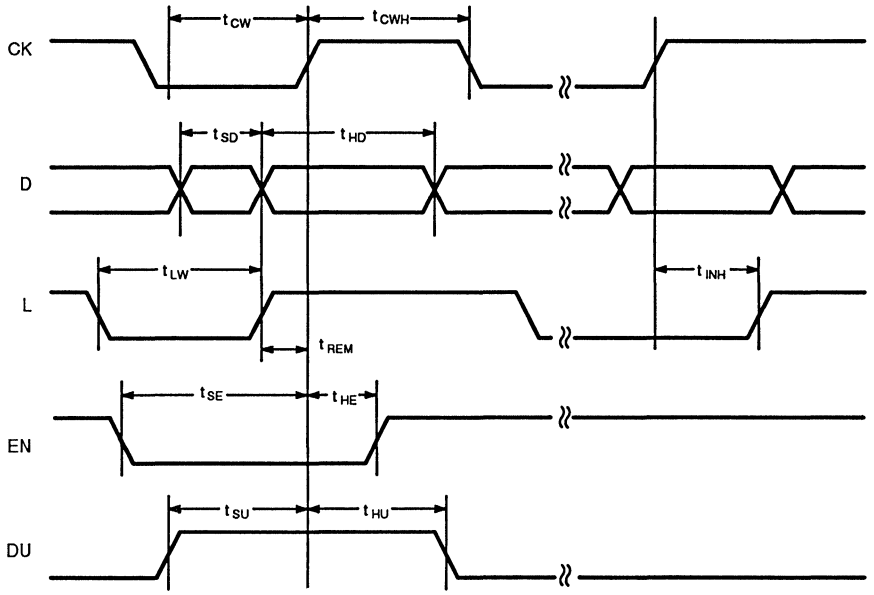


3

Cell Name

C47

Definition of Parameters



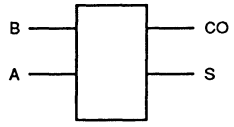
3

Adder and ALU Family

Page	Unit Cell Name	Function	Basic Cells
3–253	A1A	1-bit Half Adder	5
3–254	A1N	1-bit Full Adder	8
3–255	A2N	2-bit Full Adder	16
3–257	A4H	4-bit Binary Full Adder with Fast Carry	48

Cell Name	Function	Number of BC
A1A	1–bit Half Adder	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.647	0.032	0.759	0.017			A to S
0.574	0.032	0.772	0.017			B to S
0.594	0.032	0.660	0.017			A to CO
0.673	0.032	0.607	0.017			B to CO

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2
B	2

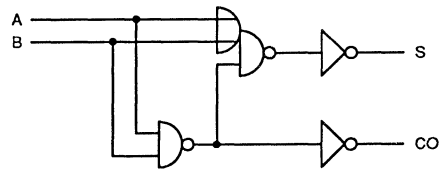
Pin Name	Output Driving Factor (Iu)
CO	36
S	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

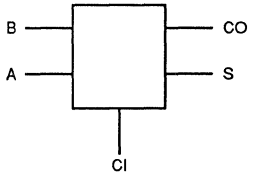
A	B	CO	S
L	L	L	L
L	H	L	H
H	L	L	H
H	H	H	L

Equivalent Circuit



Cell Name	Function	Number of BC
A1N	1–bit Full Adder	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.393	0.060	1.663	0.039			A, B to S
0.660	0.060	0.713	0.039			CI to S
1.578	0.060	1.261	0.039			A, B to CO
0.541	0.060	0.621	0.039			CI to CO

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	3
B	3
CI	3

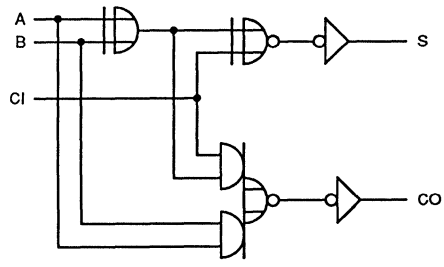
Pin Name	Output Driving Factor (lu)
CO	18
S	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

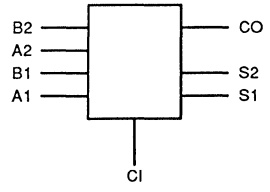
Inputs			Outputs	
A	B	CI	S	CO
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
H	H	L	L	H
L	L	H	H	L
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

Equivalent Circuit



Cell Name	Function	Number of BC
A2N	2-bit Full Adder	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.505	0.106	1.485	0.062	–		A1 to CO
1.446	0.106	1.518	0.062	–		B1 to CO
0.838	0.106	0.720	0.039	0.056	4	A2 to CO
0.779	0.106	0.720	0.039	0.056	4	B2 to CO
1.472	0.106	1.366	0.062	–		CI to CO
1.571	0.083	1.452	0.062	–		A1 to S1
1.571	0.083	1.452	0.062	–		B1 to S1
0.627	0.083	0.627	0.062	–		CI to S1
1.492	0.083	1.452	0.062	–		A1 to S2
1.644	0.083	1.558	0.062	–		A2 to S2
1.432	0.083	1.485	0.062	–		B1 to S2
1.644	0.083	1.558	0.062	–		B2 to S2
1.459	0.083	1.333	0.062	–		CI to S2

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A, B	2
CI	2

Pin Name	Output Driving Factor (lu)
S	14
CO	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

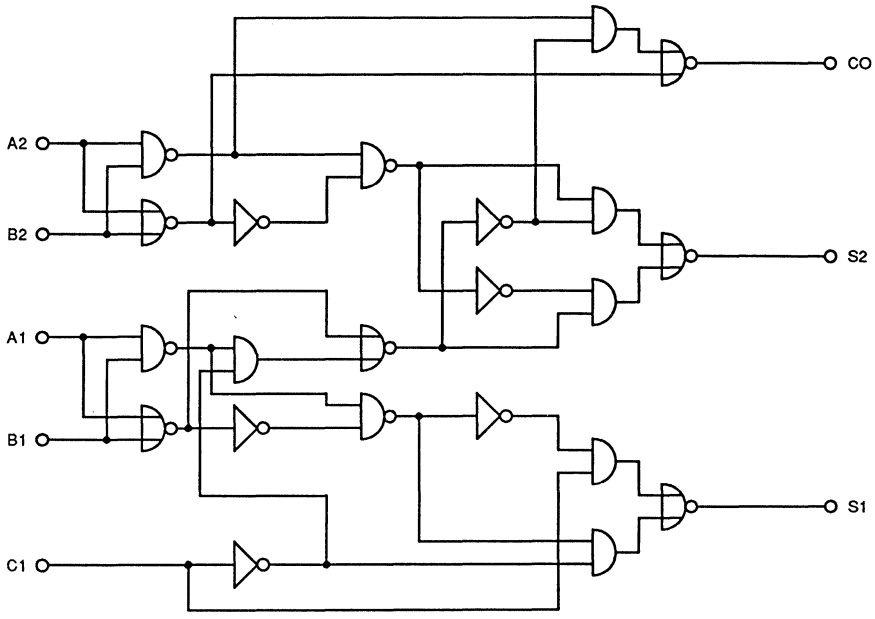
Function Table

Inputs				Outputs					
				CI = L			CI = H		
A1	B1	A2	B2	S1	S2	CO	S1	S2	CO
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

Cell Name

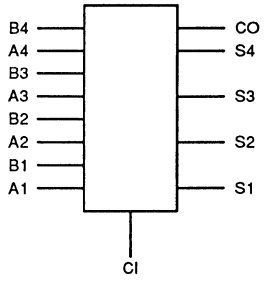
A2N

Equivalent Circuit



Cell Name	Function	Number of BC
A4H	4–bit Binary Full Adder with Fast Carry	48

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.627	0.083	0.865	0.062			CI to S1
1.399	0.106	1.624	0.062			CI to S2
1.604	0.106	1.578	0.062			CI to S3
1.657	0.106	1.868	0.062			CI to S4
1.518	0.060	1.696	0.039			CI to CO
2.013	0.083	1.789	0.062			A1, B1 to S1
1.677	0.106	1.630	0.062			A1, B1 to S2
1.809	0.106	2.033	0.062			A1, B1 to S3
1.980	0.106	2.073	0.062			A1, B1 to S4
1.743	0.060	2.000	0.039			A1, B1 to CO
1.630	0.106	1.782	0.062			A2, B2 to S2
1.934	0.106	1.901	0.062			A2, B2 to S3
1.974	0.106	2.139	0.062			A2, B2 to S4
2.046	0.060	2.026	0.039			A2, B2 to CO
1.485	0.106	1.505	0.062			A3, B3 to S3
2.026	0.106	2.132	0.062			A3, B3 to S4
2.007	0.060	2.020	0.039			A3, B3 to CO
1.531	0.083	1.591	0.039	0.056	4	A4, B4 to S4
1.934	0.060	1.855	0.039			A4, B4 to CO

Pin Name	Input Loading Factor (Iu)
A	2
B	2
CI	2

Pin Name	Output Driving Factor (Iu)
CO	18
S1, S3, S4	14
S2	18

Function Table

Inputs				Outputs					
				CI = L			CI = H		
				C2 = L			C2 = H		
A1	B1	A2	B2	S1	S2	C2	S1	S2	C2
A3	B3	A4	B4	S3	S4	CO	S3	S4	CO
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

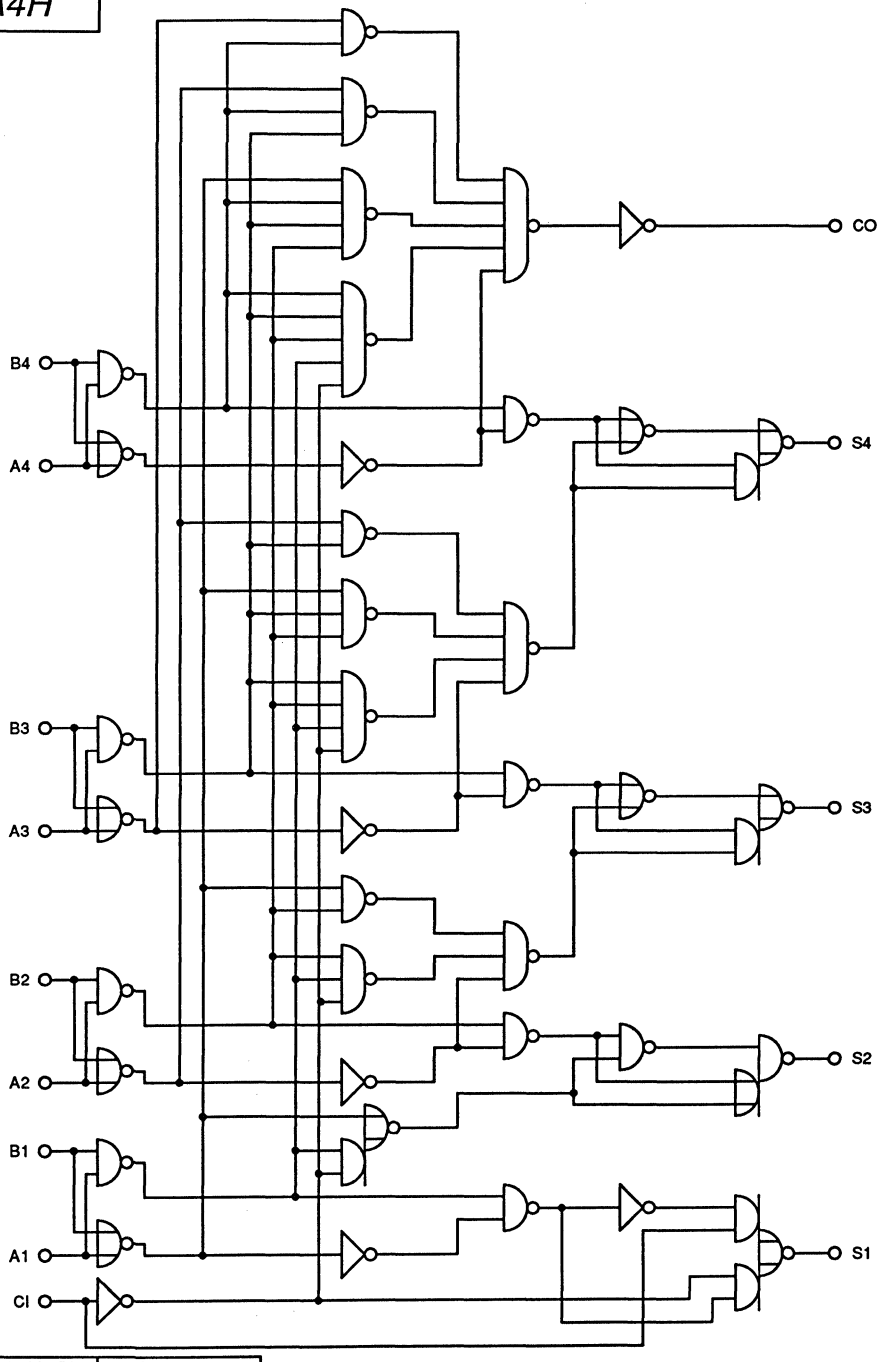
Note :

Input conditions at A1, A2, B1, B2 and CI are used to determine outputs S1 and S2 and the value of the internal carry C2.
The values at C2, A3, B3, A4 and B4 are then used to determine outputs S3, S4 and CO.

Cell Name

A4H

Equivalent Circuit

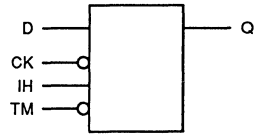


Data Latch Family

Page	Unit Cell Name	Function	Basic Cells
3–261	YL2	1-bit Data Latch with TM	5
3–263	YL4	4-bit Data Latch with TM	14
3–265	LTK	Data Latch	4
3–267	LTL	1-bit Data Latch with Clear	5
3–269	LTM	4-bit Data Latch with Clear	16
3–272	LT1	S–R Latch with Clear	4
3–274	LT4	4-bit Data Latch	14

Cell Name	Function	Number of BC
YL2	1–bit Data Latch with TM	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.446	0.032	1.485	0.017			CK, IH to Q
0.614	0.032	0.680	0.017			D to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse width	t_{CW}	4.0
Data Setup Time	t_{SD}	1.9
Data Hold Time	t_{HD}	1.5

Pin Name	Input Loading Factor (lu)
D	2
CK	1
IH	1
TM	1

Pin Name	Output Driving Factor (lu)
Q	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Note :
The TM terminal must be kept LOW during the SCAN Mode.

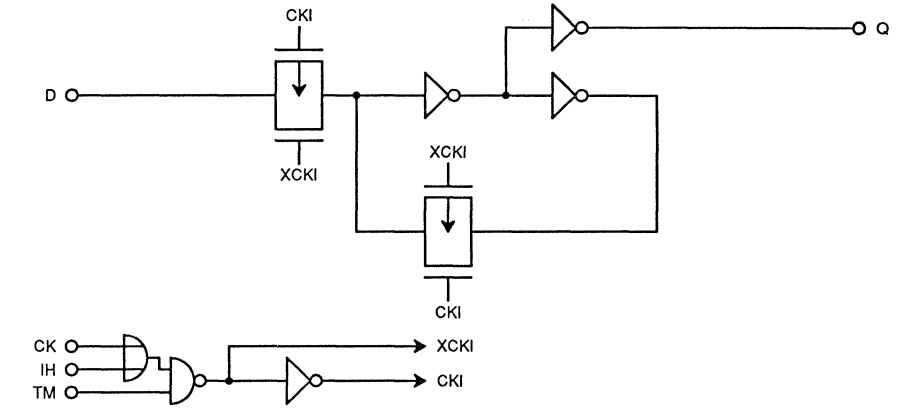
Function Table

Input				Output	Mode
TM	IH	CK	D	Q	
L	X	X	D	D	SCAN
H	H	X	X	Q_0	LATCH
H	X	H	X	Q_0	
H	L	L	D	D	

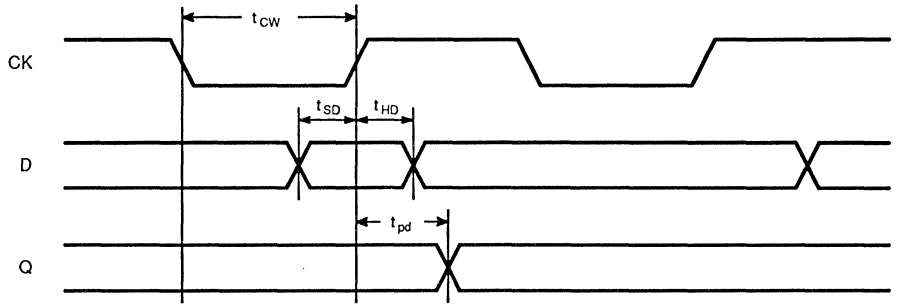
Cell Name

YL2

Equivalent Circuit



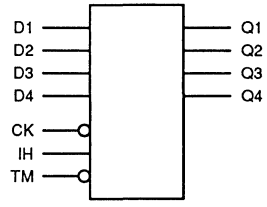
Definitions of Parameters



3

Cell Name	Function	Number of BC
YL4	4–bit Data Latch with TM	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.762	0.032	1.815	0.017			CK, IH to Q
0.581	0.032	0.680	0.017			D to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse width (CK)	t_{CW}	4.2
Data Setup Time (D)	t_{SD}	1.1
Data Hold Time (D)	t_{HD}	2.4

Pin Name	Input Loading Factor (lu)
D	2
CK	1
IH	1
TM	1

Pin Name	Output Driving Factor (lu)
Q	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Note :
The TM terminal must be kept LOW during the SCAN Mode.

Function Table

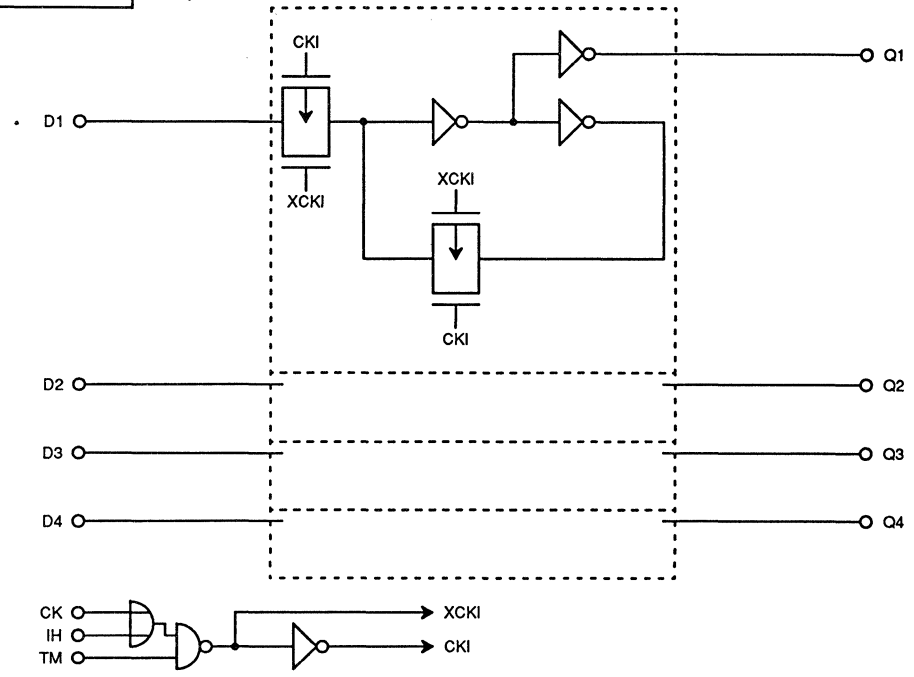
Input				Output	Mode
TM	IH	CK	Dn	Qn	
L	X	X	D	D	SCAN
H	H	X	X	Qn_0	LATCH
H	X	H	X	Qn_0	
H	L	L	D	D	

n = 1 ~ 4

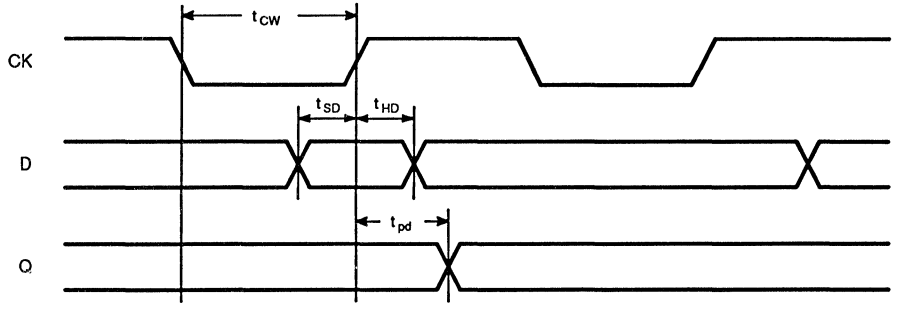
Cell Name

YL4

Equivalent Circuit

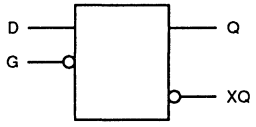


Definitions of Parameters



Cell Name	Function	Number of BC
LTK	Data Latch	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.548	0.060	0.607	0.039			D to Q
0.766	0.060	0.865	0.039			D to XQ
0.924	0.060	0.964	0.039			G to Q
1.122	0.060	1.234	0.039			G to XQ

Parameter	Symbol	Typ (ns) *
G Input Pulse Width	t_{GW}	2.5
Data Setup Time	t_{SD}	1.0
Data Hold Time	t_{HD}	1.4

Pin Name	Input Loading Factor (Iu)
D	2
G	1

Pin Name	Output Driving Factor (Iu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

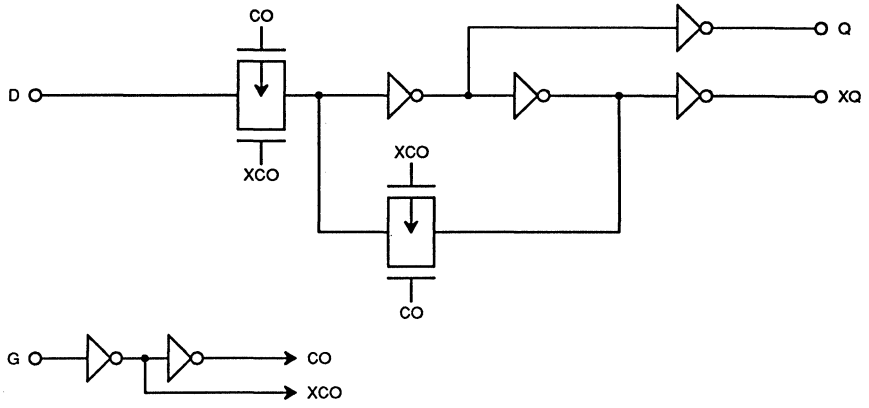
Function Table

Inputs		Outputs	
D	G	Q	XQ
X	H	Q_0	XQ_0
H	L	H	L
L	L	L	H

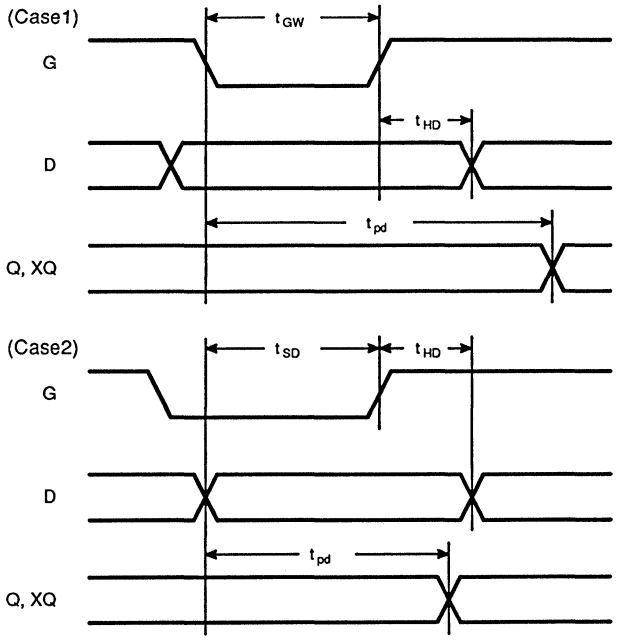
Cell Name

LTK

Equivalent Circuit

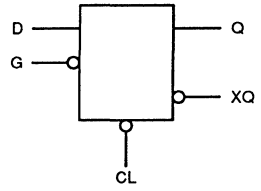


Definitions of Parameters



Cell Name	Function	Number of BC
LTL	1–bit Data Latch with Clear	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.733	0.060	0.449	0.039			CL to Q, XQ
0.627	0.060	0.647	0.039			D to Q
0.805	0.060	0.904	0.039			D to XQ
1.036	0.060	1.017	0.039			G to Q
1.175	0.060	1.327	0.039			G to XQ

Parameter	Symbol	Typ (ns) *
G Input Pulse Width	t_{GW}	2.5
Data Setup Time	t_{SD}	0.8
Data Hold Time	t_{HD}	0.3
Clear Pulse Width	t_{LW}	2.5

Pin Name	Input Loading Factor (lu)
D	2
G	1
CL	1

Pin Name	Output Driving Factor (lu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

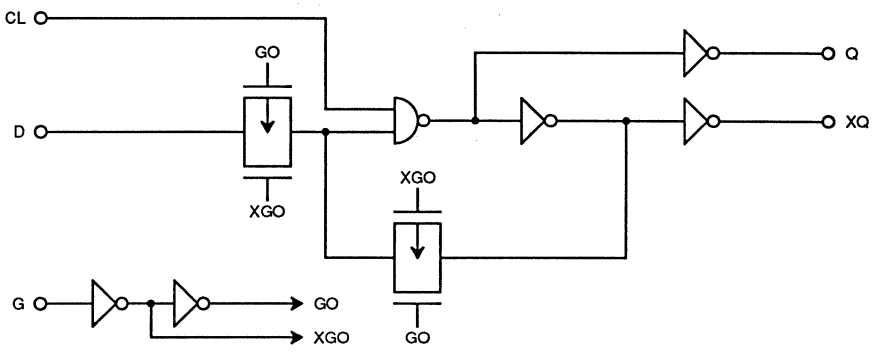
Function Table

Inputs			Outputs	
CL	D	G	Q	XQ
L	X	H	L	H
H	X	H	Q_0	XQ_0
H	H	L	H	L
H	L	L	L	H

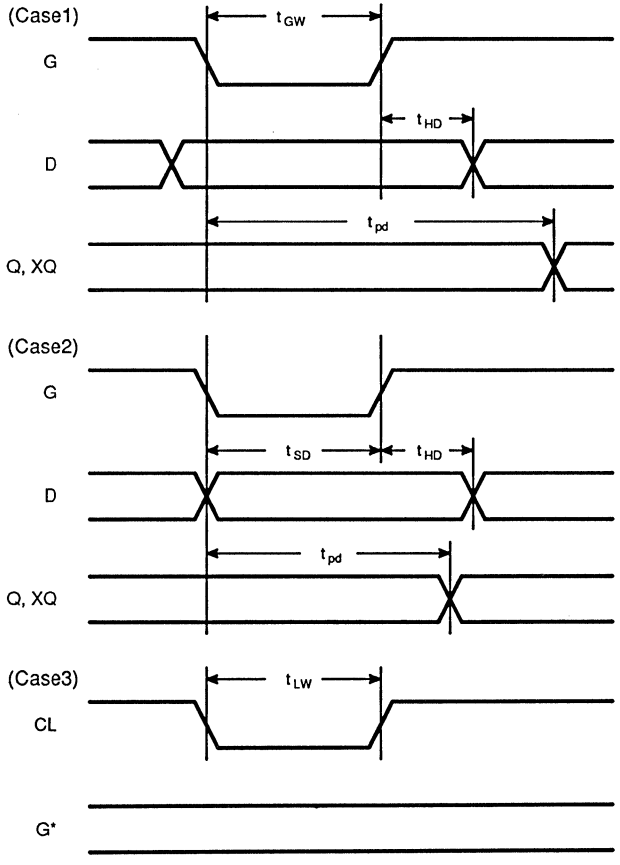
Cell Name

LTL

Equivalent Circuit



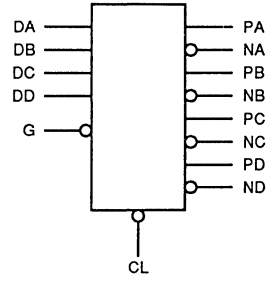
Definitions of Parameters



Note*: G input must be high level at the time this latch is cleared.

Cell Name	Function	Number of BC
LTM	4–bit Data Latch with Clear	16

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.812	0.060	0.515	0.039			CL to P, N
0.647	0.060	0.680	0.039			D to P
0.845	0.060	0.944	0.039			D to N
1.380	0.060	1.294	0.039			G to P
1.446	0.060	1.663	0.039			G to N

Parameter	Symbol	Typ (ns) *
G Input Pulse Width	t_{GW}	2.5
Clear Pulse Width	t_{LW}	2.5
Data Setup Time	t_{SD}	1.0
Data Hold Time	t_{HD}	1.4

Pin Name	Input Loading Factor (Iu)
D	2
G	1
CL	4

Pin Name	Output Driving Factor (Iu)
P	18
N	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

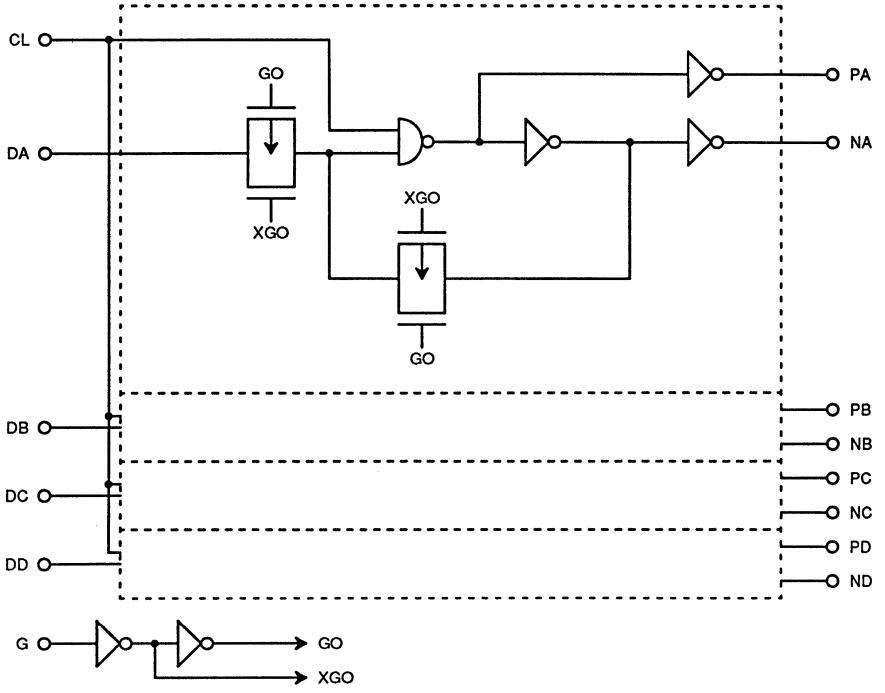
Function Table

Inputs			Outputs	
CL	D	G	P	N
L	X	H	L	H
H	X	H	P_0	N_0
H	H	L	H	L
H	L	L	L	H

Cell Name

LTM

Equivalent Circuit

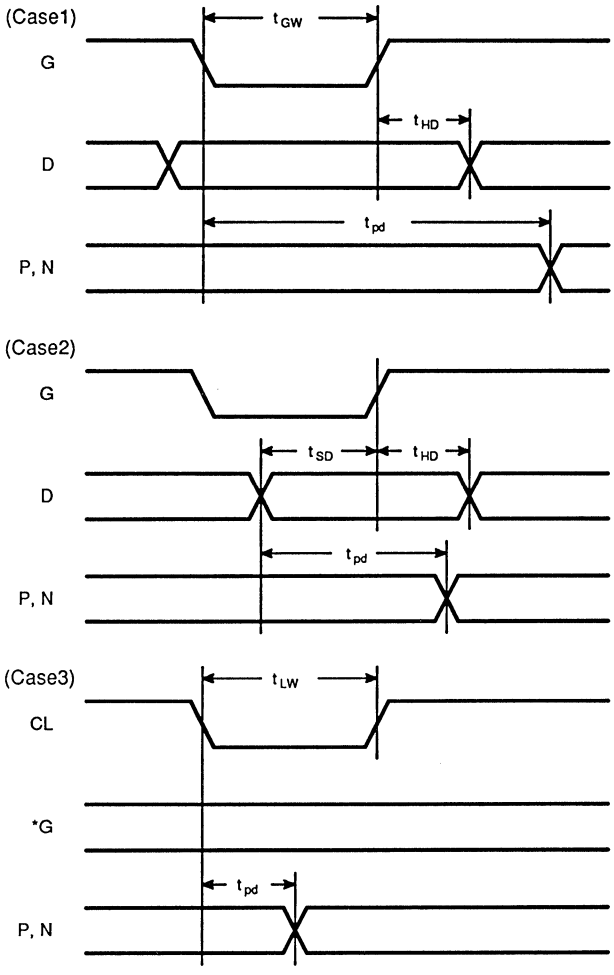


3

Cell Name

LTM

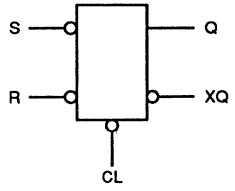
Definitions of Parameters



Note* : G input must be high level at the time this latch is cleared.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
LT1	S–R Latch with CLEAR	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.931	0.060	0.469	0.039			S to Q, XQ
0.825	0.060	0.548	0.039			R to Q, XQ
0.759	0.060	0.489	0.039			CL to Q, XQ

Parameter	Symbol	Typ (ns) *
Set Pulse Width	t_{SW}	2.5
Reset Pulse Width	t_{RW}	2.5
Clear Pulse Width	t_{LW}	2.5

Pin Name	Input Loading Factor (Iu)
S	1
R	1
CL	1

Pin Name	Output Driving Factor (Iu)
Q	18
XQ	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

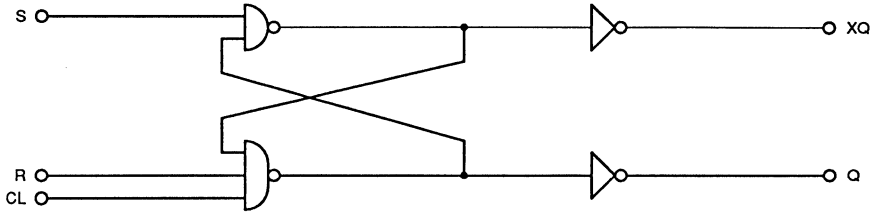
Function Table

Inputs			Outputs	
CL	S	R	Q	XQ
L	H	H	L	H
H	H	H	Q_0	XQ_0
H	H	L	L	H
H	L	H	H	L
H	L	L	Inhibited	

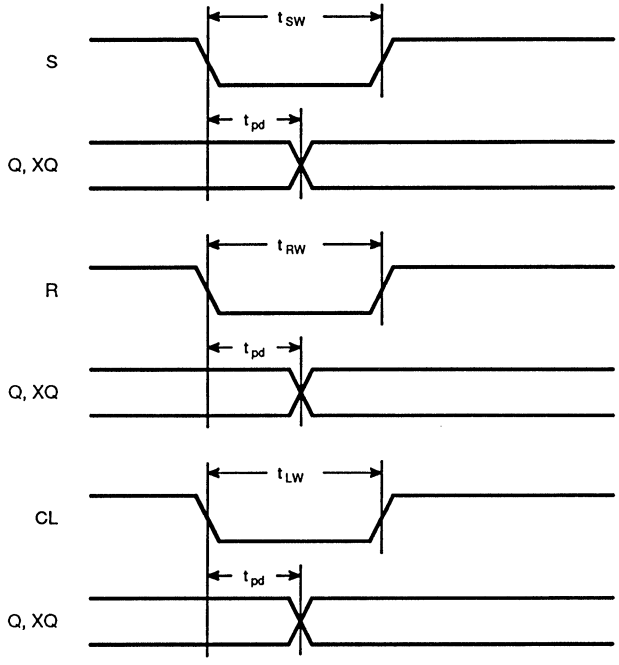
Cell Name

LT1

Equivalent Circuit



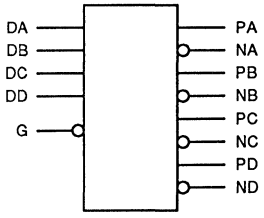
Definitions of Parameters



3

Cell Name	Function	Number of BC
LT4	4-bit Data Latch	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.320	0.060	1.208	0.039			G to P
1.320	0.060	1.611	0.039			G to N
0.555	0.060	0.627	0.039			D to P
0.739	0.060	0.845	0.039			D to N

Parameter	Symbol	Typ (ns) *
G Input Pulse Width	t_{GW}	2.5
Data Setup Time	t_{SD}	1.0
Data Hold Time	t_{HD}	1.4

Pin Name	Input Loading Factor (Iu)
D	2
G	1

Pin Name	Output Driving Factor (Iu)
P	18
N	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

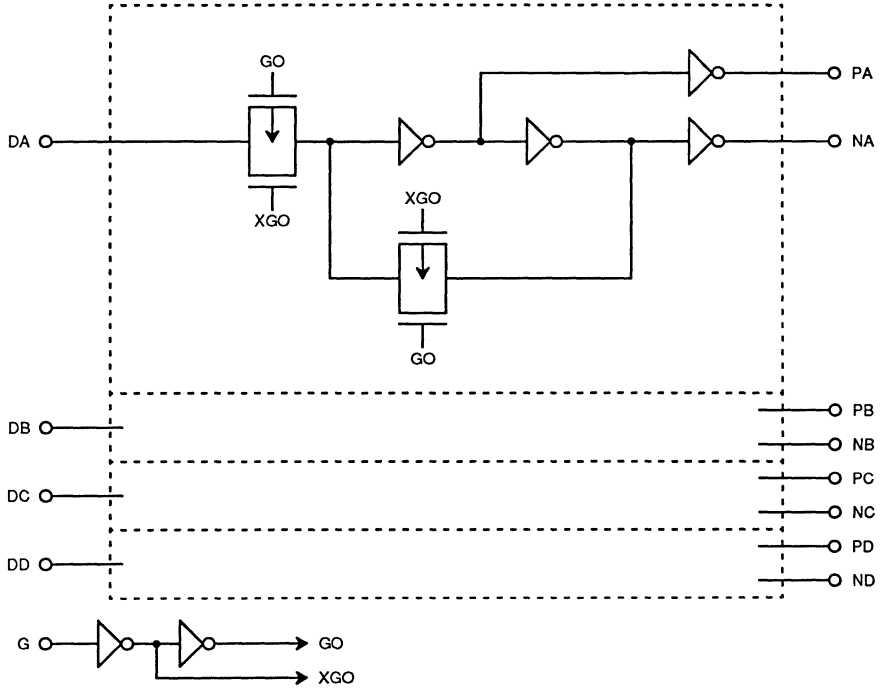
Function Table

Inputs		Outputs	
D	G	P	N
H	H	P_0	N_0
L	H	P_0	N_0
H	L	H	L
L	L	L	H

Cell Name

LT4

Equivalent Circuit

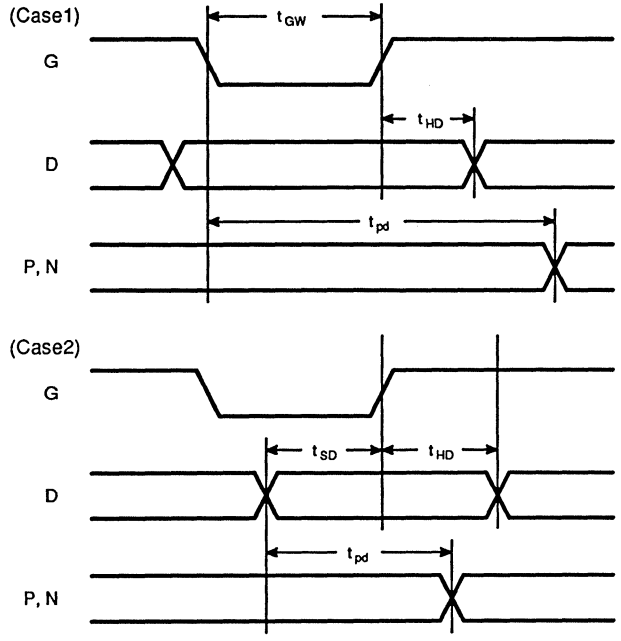


3

Cell Name

LT4

Definitions of Parameters



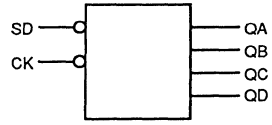
3

Shift Register Family

Page	Unit Cell Name	Function	Basic Cells
3–279	FS1	4-bit Serial-in Parallel-out Shift Register	18
3–281	FS2	4-bit Shift Register with Synchronous Load	30
3–283	FS3	4-bit Shift Register with Asynchronous Load	34
3–286	SR1	4-bit Serial-in Parallel-out Shift Register with Scan	36

Cell Name	Function	Number of BC
FS1	4–bit Serial–in Parallel–out Shift Register	18

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.281	0.060	1.657	0.039	0.056	4	CK to Q

Parameter		Symbol	Typ (ns) *
Clock Pulse Width		t_{CW}	2.5
SD Setup Time		t_{SSD}	0.4
SD Hold Time		t_{HSD}	0.2
Clock Pause Time	C ≦16 lu	t_{CWL}**	3.4
	16 < C ≦32 lu	t_{CWL}**	5.0
	32 < C ≦48 lu	t_{CWL}**	6.4

Pin Name	Input Loading Factor (lu)
SD	1
CK	1

Pin Name	Output Driving Factor (lu)
Q	16

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

** The value of t_{CWL} depends on the load(c) connected to the output terminals, QA, QB, QC and QD.

Function Table

Inputs		Outputs			
SD	CK	QA	QB	QC	QD
SD	↓	$\overline{SD}$	QAn	QBn	QCn

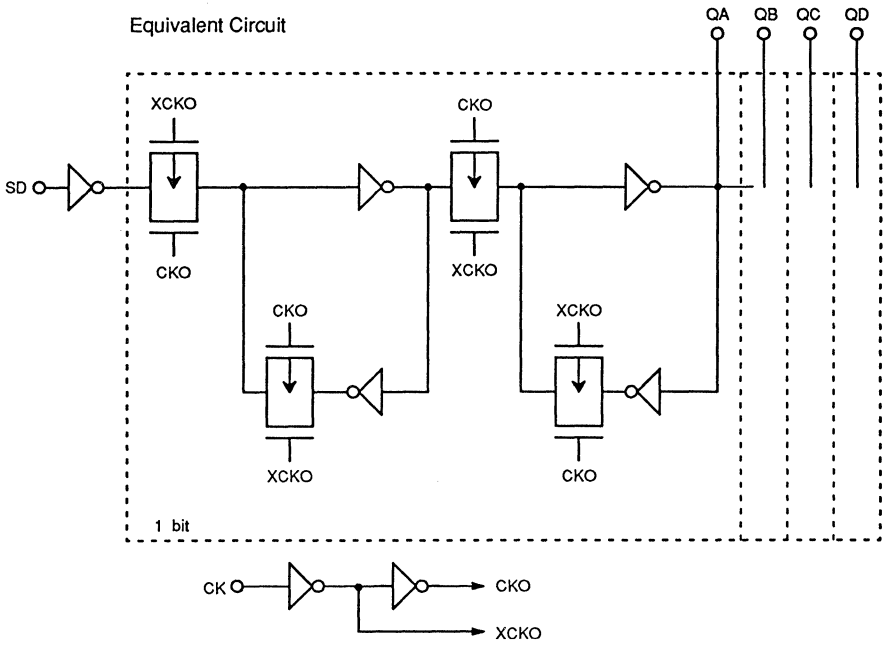
NOTE: • SD = H or L

• QAn, QBn and QCn are levels of QA, QB, and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

Cell Name

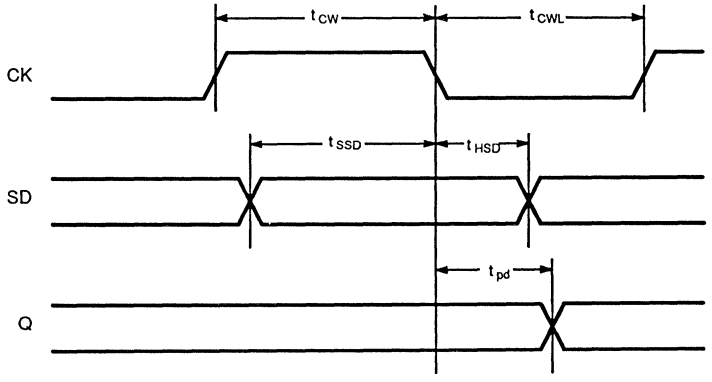
FS1

Equivalent Circuit



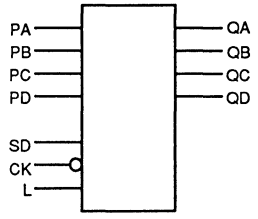
3

Definition of Parameters



Cell Name	Function	Number of BC
FS2	4–bit Shift Register with Synchronous Load	30

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
1.228	0.060	1.657	0.039	0.056	4	CK to Q

Parameter		Symbol	Typ (ns) *
Clock Pulse Width		t_{CW}	2.5
SD Setup Time		t_{SSD}	1.7
SD Hold Time		t_{HSD}	0.8
Load Setup Time		t_{SL}	2.6
Load Hold Time		t_{HL}	0.3
P Setup Time		t_{SP}	2.1
P Hold Time		t_{HP}	0.9
Clock Pause Time	C ≦16 lu	t_{CWL}**	3.4
	16 < C ≦32 lu	t_{CWL}**	5.0
	32 < C ≦48 lu	t_{CWL}**	6.4

Pin Name	Input Loading Factor (lu)
CK	1
SD	1
L	1
P	1

Pin Name	Output Driving Factor (lu)
Q	16

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

** The value of t_{CWL} depends on the load(c) connected to the output terminals, QA, QB, QC and QD.

Function Table

Inputs				Outputs			
SD	L	P	CK	QA	QB	QC	QD
SD	L	X	↓	SD	QAn	QBn	QCn
X	H	P	↓	PA	PB	PC	PD

NOTE: • SD = H or L

• QAn, QBn and QCn are levels of QA, QB, and QC respectively, before the falling edge of CK, i.e. 1 bit shift by the falling edge of CK.

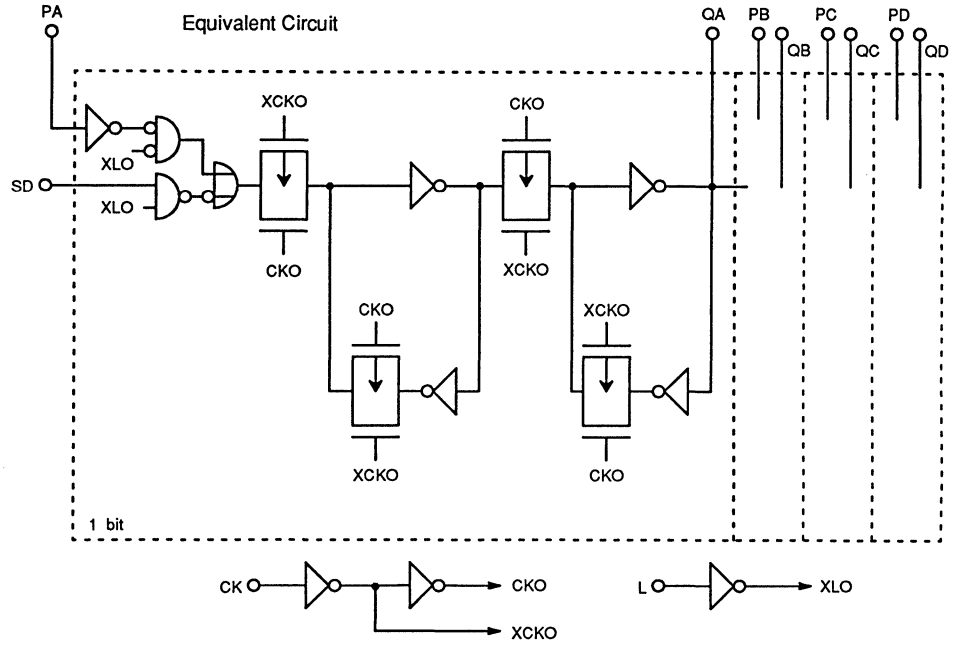
• P represents PA, PB, PC and PD.

3

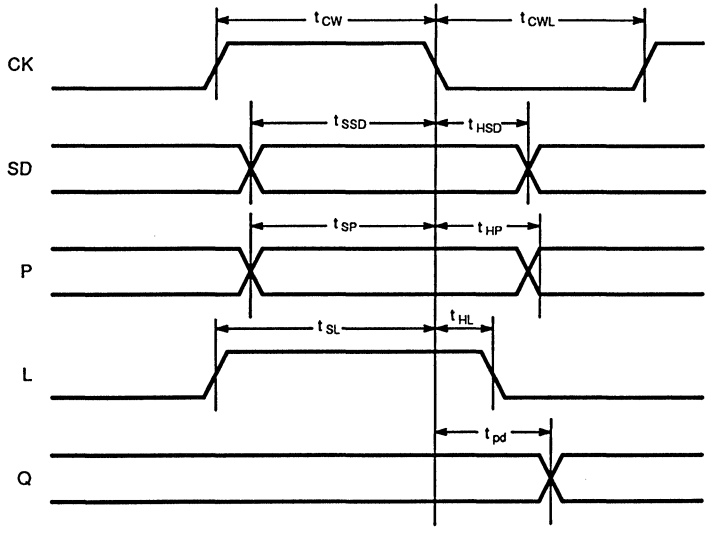
Cell Name

FS2

Equivalent Circuit

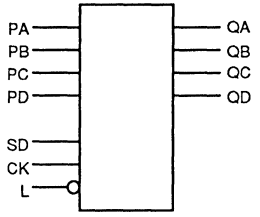


Definition of Parameters



Cell Name	Function	Number of BC
FS3	4–bit Shift Register with Asynchronous Load	34

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.208	0.064	1.122	0.050			CK to Q
2.449	0.064	1.848	0.050			L to Q
1.076	0.064	1.597	0.050			P to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	2.5
Load Pulse Width	t_{LW}	3.7
SD Setup Time	t_{SSD}	0.6
SD Hold Time	t_{HSD}	1.1
P Setup Time	t_{SP}	0.3
P Hold Time	t_{HP}	1.4

Pin Name	Input Loading Factor (lu)
CK	2
SD	2
L	1
P	2

Pin Name	Output Driving Factor (lu)
Q	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

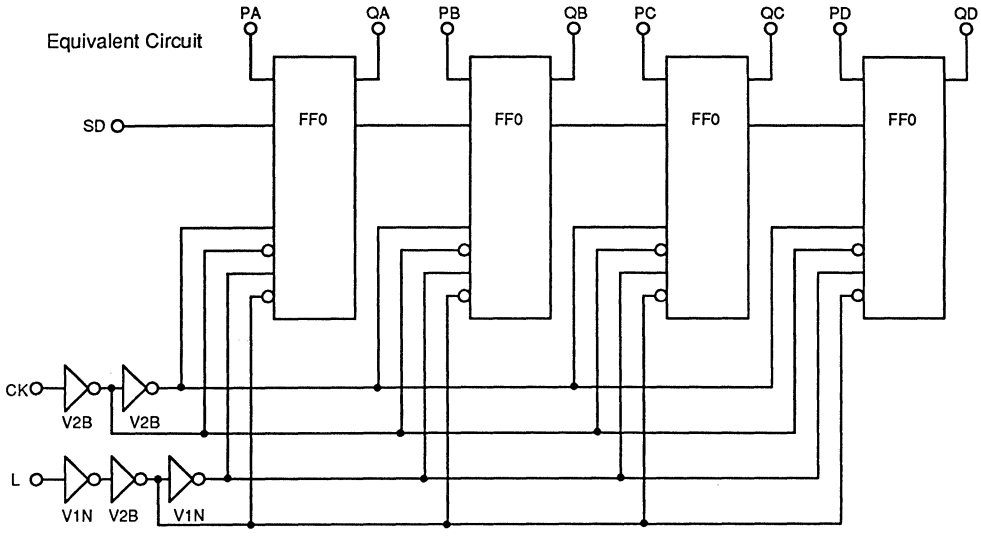
Function Table

Inputs				Outputs
L	P	SD	CK	Q
L	L	X	X	L
L	H	X	X	H
H	X	L	↑	L
H	X	H	↑	H

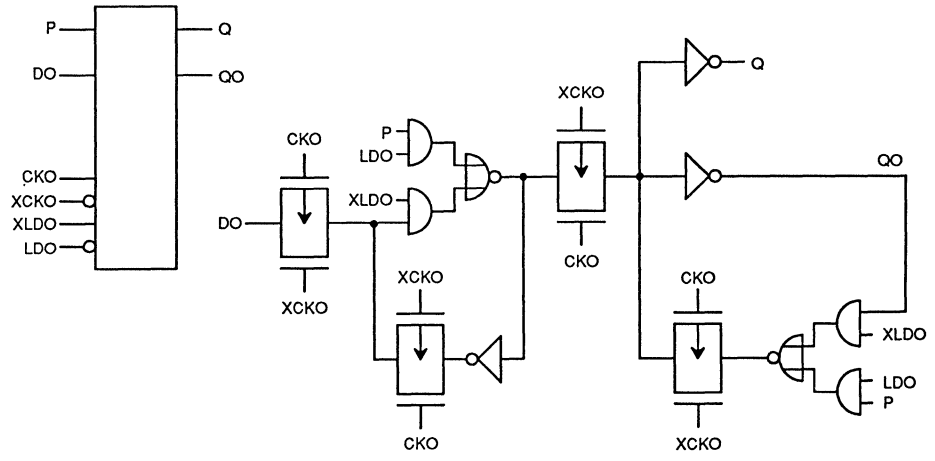
Cell Name

FS3

Equivalent Circuit



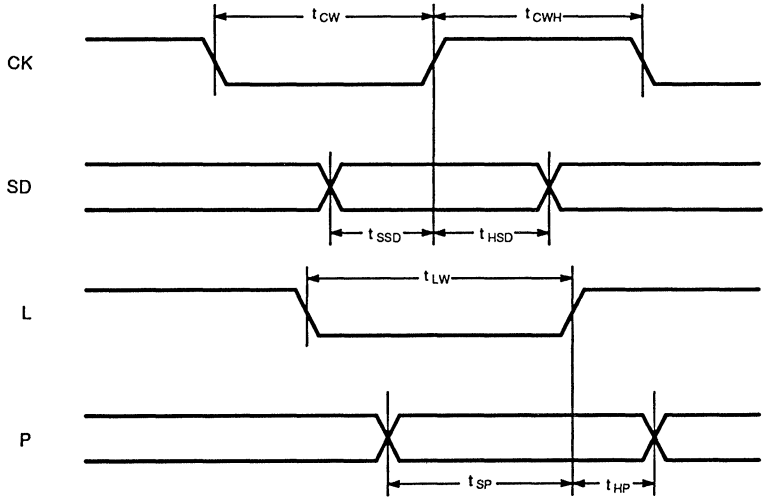
Equivalent Circuit of FFO



Cell Name

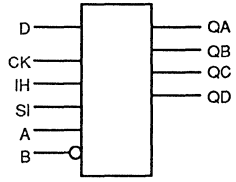
FS3

Definition of Parameters



Cell Name	Function	Number of BC
SR1	4–bit Serial–in Parallel–out Shift Register with SCAN	36

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.729	0.032	1.782	0.034	0.050	7	CK to Q

Parameter	Symbol	Typ (ns) *
Clock Pulse Width	t_{CW}	2.5
Clock Pause Time	t_{CWH}	3.3
Data Setup Time	t_{SD}	2.0
Data Hold Time	t_{HD}	0.9

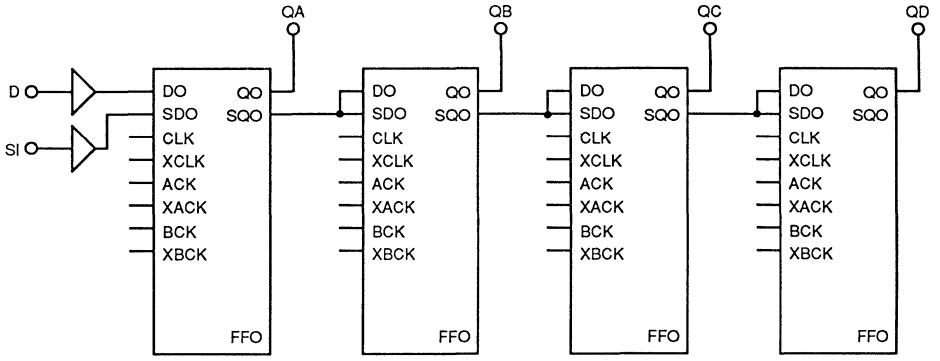
Pin Name	Input Loading Factor (Iu)
D	1
CK	1
IH	1
SI	1
A,B	1

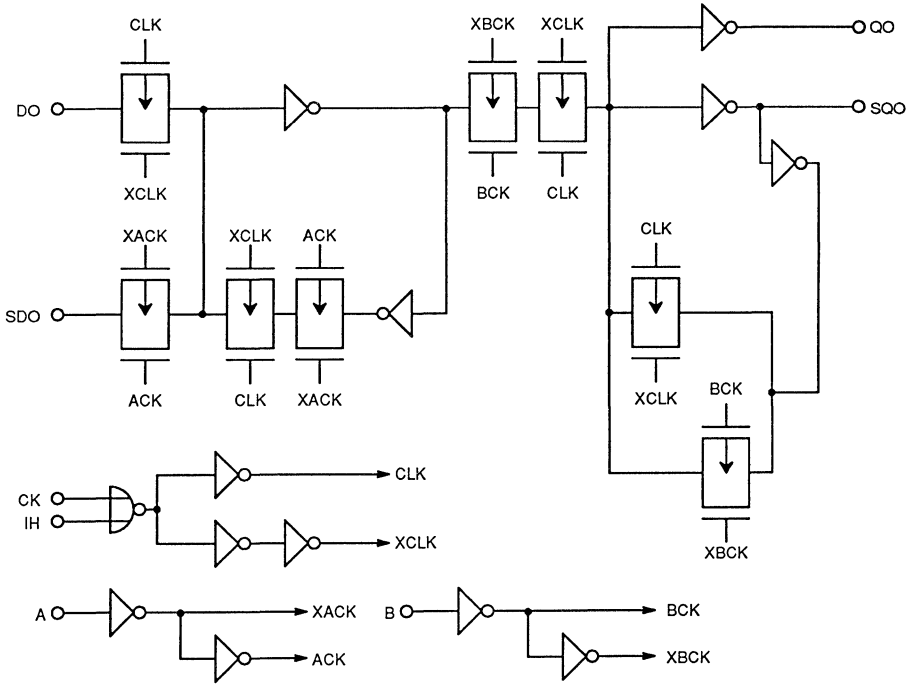
Pin Name	Output Driving Factor (Iu)
Q	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name

SR1

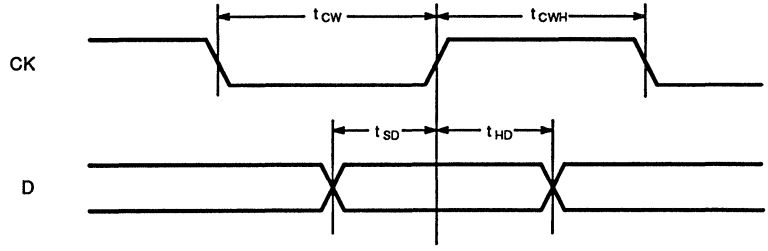




Cell Name

SR1

Definition of Parameters

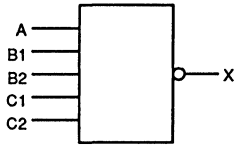


Parity Generator/Selector/Decoder Family

Page	Unit Cell Name	Function	Basic Cells
Parity Generators/Checkers			
3–291	PE5	5-bit Even Parity Generator/Checker	12
3–292	PO5	5-bit Odd Parity Generator/Checker	12
3–293	PE8	8-bit Even Parity Generator/Checker	18
3–294	PO8	8-bit Odd Parity Generator/Checker	18
3–295	PE9	9-bit Even Parity Generator/Checker	22
3–296	PO9	9-bit Odd Parity Generator/Checker	22
Data Selector			
3–297	P24	4-wide 2:1 Data Selector	12
Decoders			
3–298	DE2	2:4 Decoder	5
3–299	DE3	3:8 Decoder	15
3–301	DE4	2:4 Decoder with Enable	8
3–302	DE6	3:8 Decoder with Enable	30
Selectors			
3–304	T2B	2:1 Selector	2
3–305	T2C	Dual 2:1 Selector	4
3–307	T2D	2:1 Selector	2
3–308	T2E	Dual 2:1 Selector	5
3–309	T2F	2:1 Selector	8
3–311	T5A	4:1 Selector	5
3–313	V3A	1:2 Selector	2
3–314	V3B	Dual 1:2 Selector	4
Magnitude Comparator			
3–315	MC4	4-bit Magnitude Comparator	42

Cell Name	Function	Number of BC
PE5	5–bit Even Parity Generator/Checker	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
1.386	0.032	1.802	0.017			A to X
1.386	0.032	1.729	0.017			B to X
2.185	0.032	2.554	0.017			C to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2
B	2
C	2

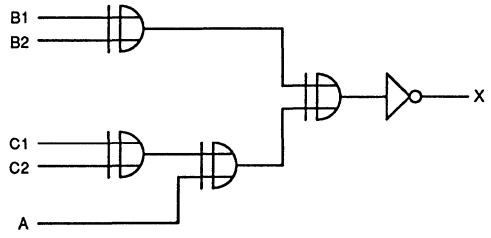
Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

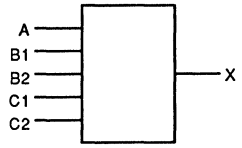
Σinput	X
Odd	L
Even	H

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
PO5	5–bit Odd Parity Generator/Checker	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
1.393	0.032	1.624	0.017			A to X
1.512	0.032	1.604	0.017			B to X
2.211	0.032	2.409	0.017			C to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2
B	2
C	2

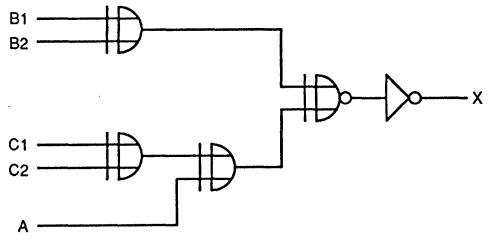
Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Σinput	X
Odd	H
Even	L

Equivalent Circuit



C21–PO5–E0	Sheet 1/1

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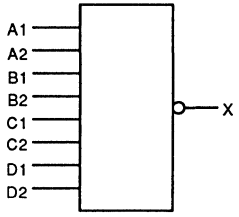
Cell Name	Function	Number of BC
PE8	5–bit Even Parity Generator/Checker	18

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.033	0.060	2.290	0.039			A to X
2.079	0.060	2.337	0.039			B to X
2.079	0.060	2.323	0.039			C to X
2.125	0.060	2.370	0.039			D to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	2
B	2
C	2
D	2

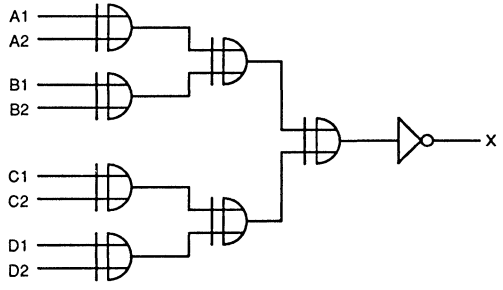
Pin Name	Output Driving Factor (lu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

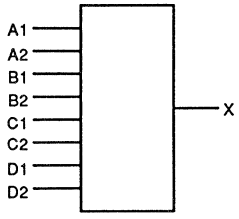
Σinput	X
Odd	L
Even	H

Equivalent Circuit



Cell Name	Function	Number of BC
PO8	8-bit Odd Parity Generater/Checker	18

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.993	0.060	2.264	0.039			A to X
2.040	0.060	2.310	0.039			B to X
2.046	0.060	2.224	0.039			C to X
2.092	0.060	2.251	0.039			D to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2
B	2
C	2
D	2

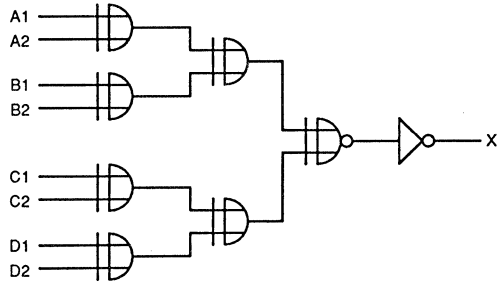
Pin Name	Output Driving Factor (Iu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

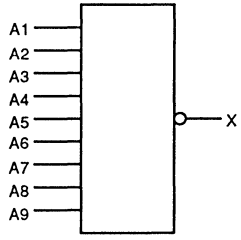
Σinput	X
Odd	L
Even	H

Equivalent Circuit



Cell Name	Function	Number of BC
PE9	9–bit Even Parity Generator/Checker	22

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
2.792	0.060	3.016	0.039			A to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	2

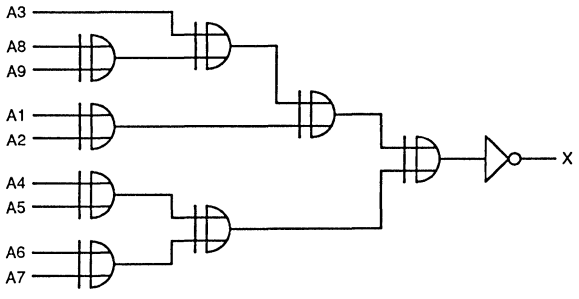
Pin Name	Output Driving Factor (lu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

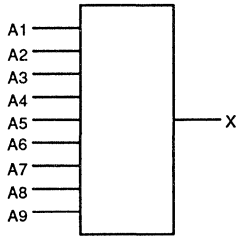
Σinput	X
Odd	L
Even	H

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
PO9	9–bit Odd Parity Generator/Checker	22

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
2.746	0.060	3.016	0.039			A to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	2

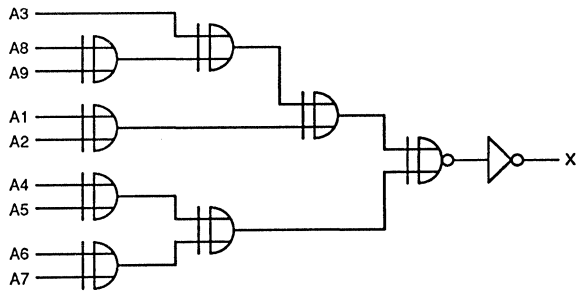
Pin Name	Output Driving Factor (Iu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Σinput	X
Odd	H
Even	L

Equivalent Circuit



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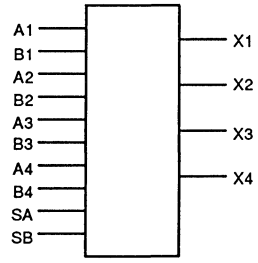
Cell Name	Function	Number of BC
P24	4–wide 2 : 1 Data Selector	12

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.502	0.032	0.442	0.017			A to X
0.614	0.032	0.515	0.017			B to X
0.429	0.032	0.502	0.017			SA to X
0.528	0.032	0.574	0.017			SB to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1
B	1
S	4

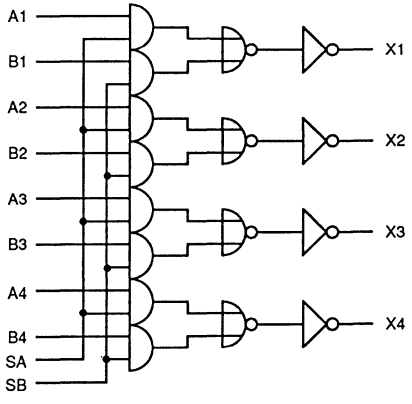
Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

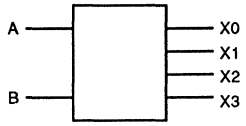
SA	SB	Xn
L	L	L
H	L	An
L	H	Bn
H	H	An+Bn

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
DE2	2 : 4 Decoder	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.416	0.060	0.574	0.062			A to X0
0.469	0.060	0.515	0.062			A to X1
0.198	0.060	0.238	0.062			A to X2,X3
0.469	0.060	0.515	0.062			B to X0
0.152	0.060	0.297	0.062			B to X1,X3
0.416	0.060	0.574	0.062			B to X2

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	3
B	3

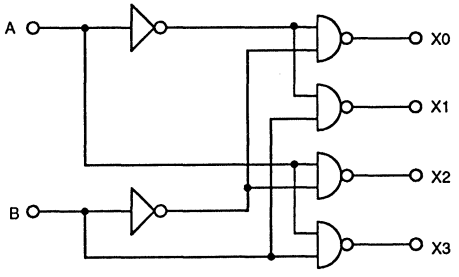
Pin Name	Output Driving Factor (Iu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs		Outputs			
A	B	X3	X2	X1	X0
L	L	H	H	H	L
L	H	H	H	L	H
H	L	H	L	H	H
H	H	L	H	H	H

Equivalent Circuit



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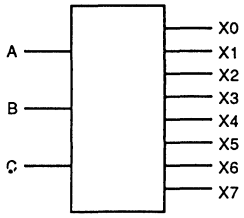
Cell Name	Function	Number of BC
DE3	3 : 8 Decoder	15

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.759	0.060	0.885	0.084			A to X0~X3
1.287	0.060	1.287	0.084			A to X4~X7
0.706	0.060	0.911	0.084			B to X0~X3
1.234	0.060	1.314	0.084			B to X4~X7
0.654	0.060	0.944	0.084			C to X0~X3
1.182	0.060	1.743	0.084			C to X4~X7

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1
B	1
C	1

Pin Name	Output Driving Factor (Iu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

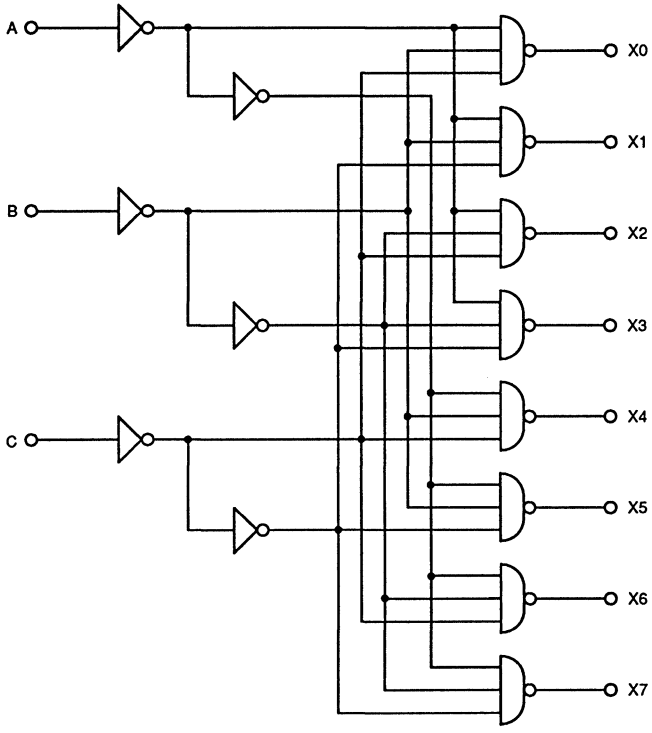
Function Table

Inputs			Outputs							
A	B	C	X0	X1	X2	X3	X4	X5	X6	X7
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

Cell Name

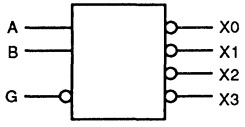
DE3

Equivalent Circuit



Cell Name	Function	Number of BC
DE4	2 : 4 Decoder with Enable	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.627	0.060	0.772	0.084			G to X
0.456	0.060	0.588	0.084			A to X
0.568	0.060	0.601	0.084			B to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	3
B	3
G	1

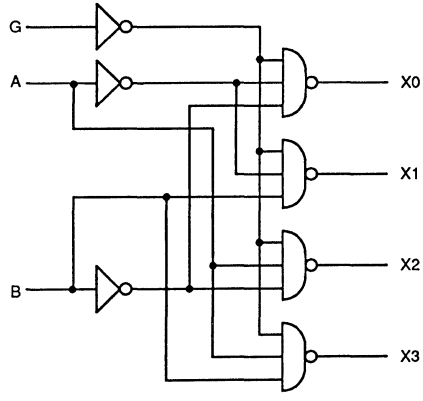
Pin Name	Output Driving Factor (lu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

G	A	B	X3	X2	X1	X0
H	X	X	H	H	H	H
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H

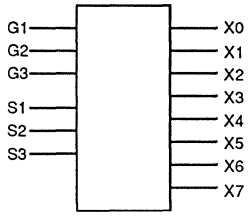
Equivalent Circuit



3

Cell Name	Function	Number of BC
DE6	3 : 8 Decoder with Enable	30

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.611	0.060	3.142	0.039			G to X
1.525	0.060	1.736	0.039			S to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
G	1
S	1

Pin Name	Output Driving Factor (Iu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

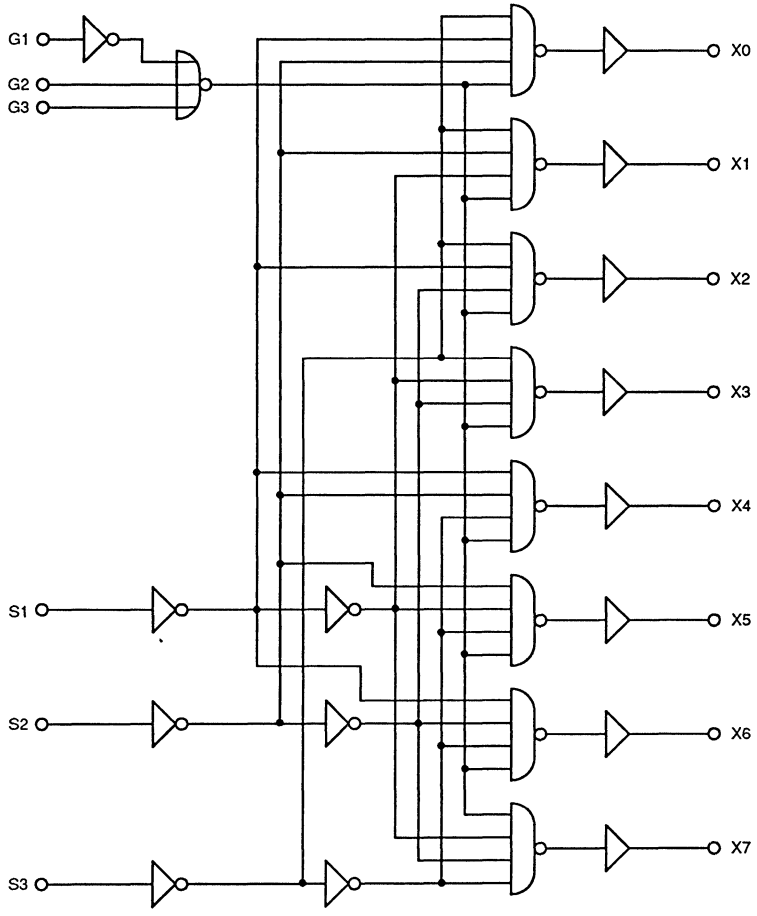
Function Table

G1	G2+G3	S3	S2	S1	X7	X6	X5	X4	X3	X2	X1	X0
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	H	L
H	L	L	L	H	H	H	H	H	H	H	L	H
H	L	L	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	L	H	H	H	H
H	L	H	L	H	H	H	L	H	H	H	H	H
H	L	H	H	L	H	L	H	H	H	H	H	H
H	L	H	H	H	L	H	H	H	H	H	H	H

Cell Name

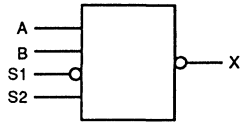
DE6

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
T2B	2 : 1 Selector	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.277	0.060	0.416	0.039			A,B to X
0.324	0.060	0.522	0.039			S to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A,B	2
S	1

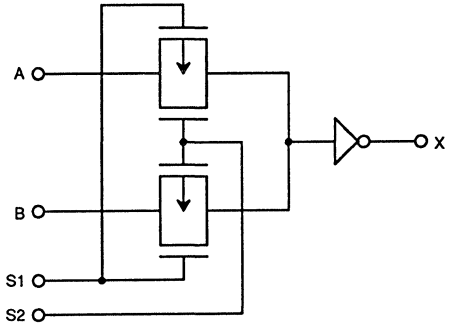
Pin Name	Output Driving Factor (Iu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs				Outputs
A	B	S1	S2	X
L	H	L	H	H
H	H	L	H	L
X	L	H	L	H
X	H	H	L	L
L	H	L	L	Inhibit
L	H	H	H	Inhibit
H	L	L	L	Inhibit
H	L	H	H	Inhibit

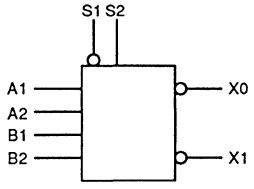
Equivalent Circuit



C21–T2B–E0 | Sheet 1/1

Cell Name	Function	Number of BC
T2C	Dual 2 : 1 Selector	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.271	0.060	0.409	0.039			A,B to X
0.357	0.060	0.548	0.039			S to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A,B	2
S	2

Pin Name	Output Driving Factor (lu)
X	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

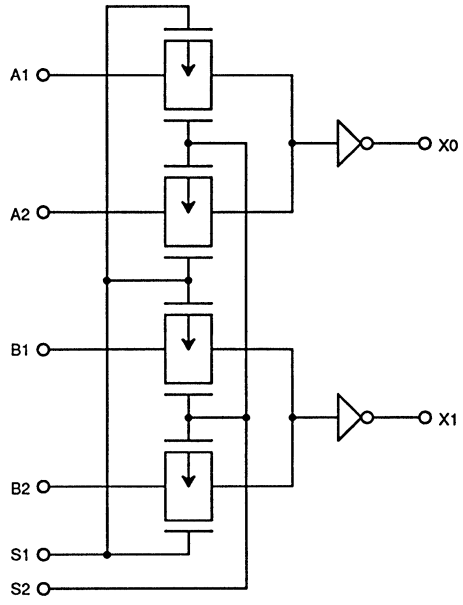
Function Table

Inputs		Outputs			
A1 , B1	A2 , B2	S1	S2	X0	X1
L	X	L	H	H	H
H	X	L	H	L	L
X	L	H	L	H	H
X	H	H	L	L	L
L	H	L	L	Inhibit	Inhibit
H	L	L	L	Inhibit	Inhibit
L	H	H	H	Inhibit	Inhibit
H	L	H	H	Inhibit	Inhibit

Cell Name

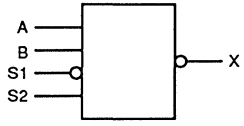
T2C

Equivalent Circuit



Cell Name	Function	Number of BC
T2D	2 : 1 Selector	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.330	0.069	0.370	0.056			A,B to X
0.357	0.069	0.271	0.056			S to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A,B	1
S	1

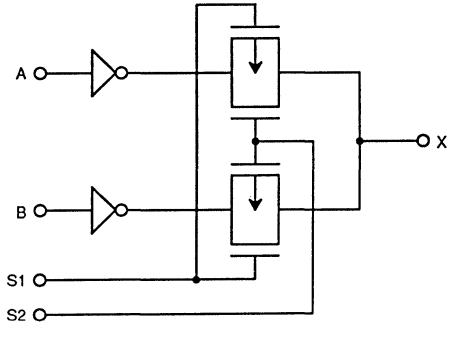
Pin Name	Output Driving Factor (lu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

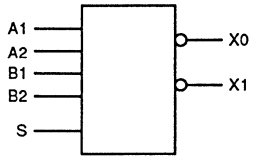
Inputs				Outputs
A	B	S1	S2	X
L	X	L	H	H
H	X	L	H	L
X	L	H	L	H
X	H	H	L	L
L	H	L	L	Inhibit
L	H	H	H	Inhibit
H	L	L	L	Inhibit
H	L	H	H	Inhibit

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
T2E	Dual 2 : 1 Selector	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.284	0.060	0.284	0.045	0.062	4	A,B to X
0.865	0.060	0.858	0.045	0.062	4	S to X

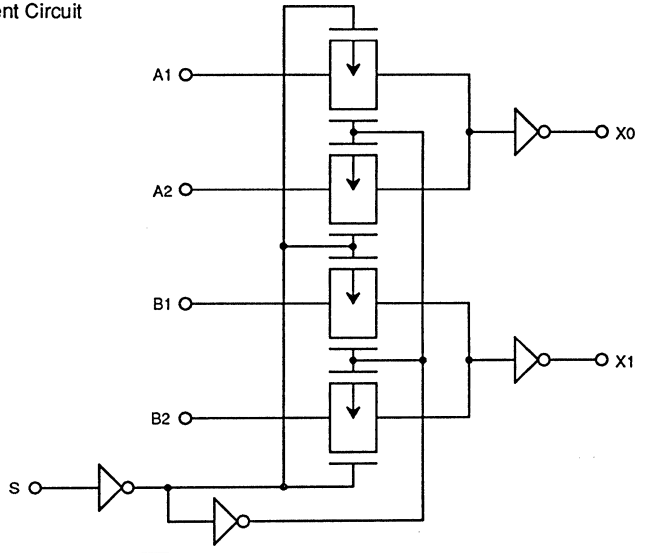
Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A,B	2
S	1

Pin Name	Output Driving Factor (Iu)
X	18

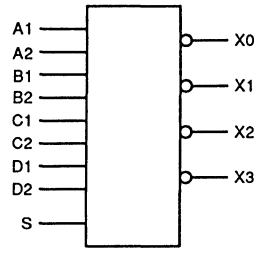
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
T2F	2 : 1 Selector	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.284	0.060	0.284	0.045	0.062	4	A,B,C,D to X
0.865	0.060	0.858	0.045	0.062	4	S to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A,B,C,D	2
S	1

Pin Name	Output Driving Factor (Iu)
X	18

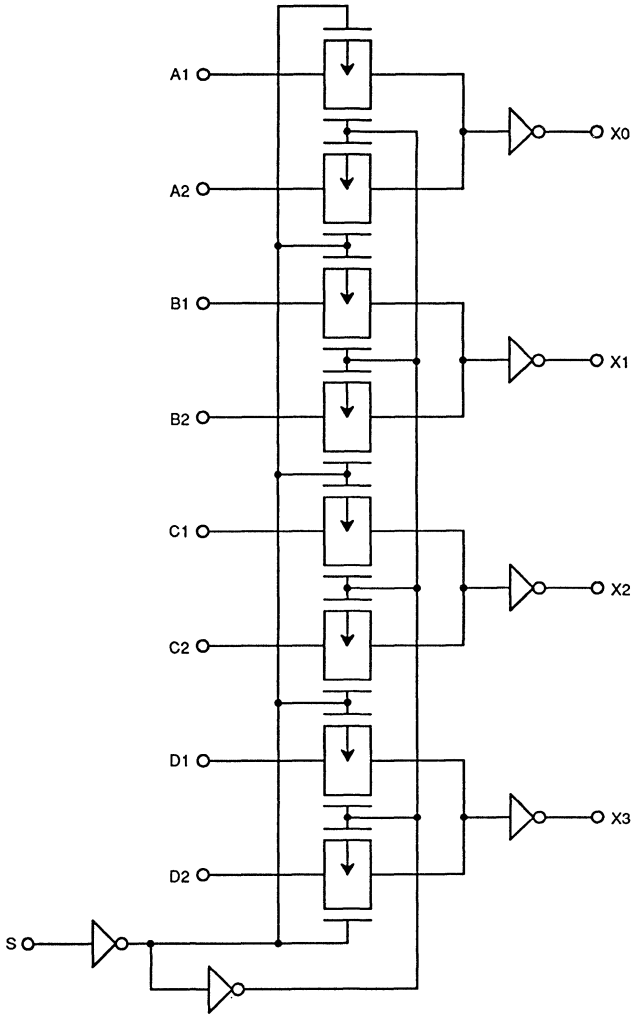
* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

3

Cell Name

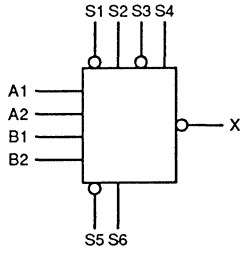
T2F

Equivalent Circuit



Cell Name	Function	Number of BC
T5A	4 : 1 Selector	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.528	0.087	0.528	0.073			A,B to X
0.528	0.087	0.442	0.073			S1~4 to X
0.297	0.087	0.284	0.073			S5~6 to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A,B	1
S	1

Pin Name	Output Driving Factor (Iu)
X	9

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

Inputs										Output
A1	A2	B1	B2	S1	S2	S3	S4	S5	S6	X
L				L	H			L	H	H
H				L	H			L	H	L
	L			H	L			L	H	H
	H			H	L			L	H	L
		L				L	H	H	L	H
		H				L	H	H	L	L
			L			H	L	H	L	H
			H			H	L	H	L	L

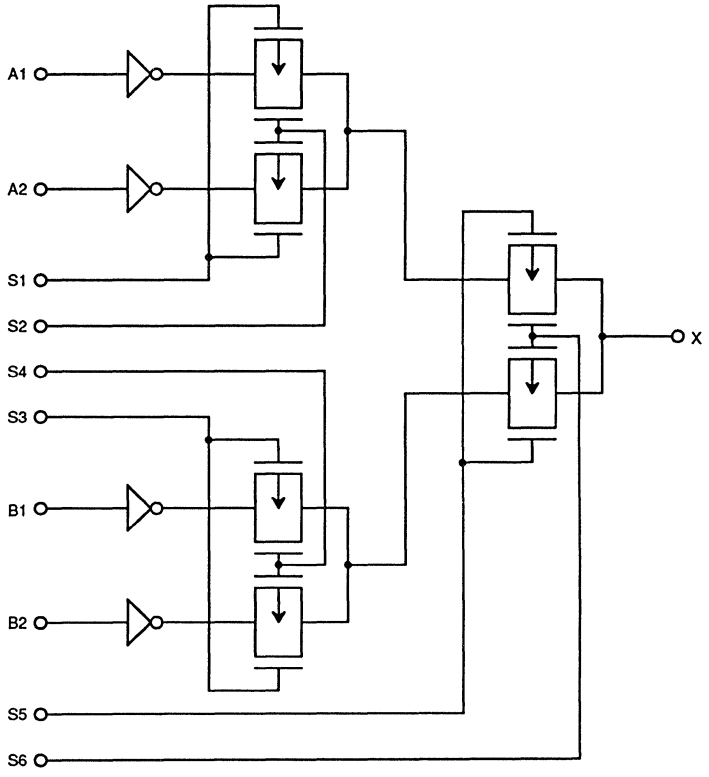
A1≠A2 to S1=S2 or S5=S6 Inhibit
B1≠B2 to S3=S4 or S5=S6 Inhibit
A1,A2≠B1,B2 or S5=S6 Inhibit

3

Cell Name

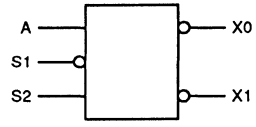
T5A

Equivalent Circuit



Cell Name	Function	Number of BC
V3A	1 : 2 Selector	2

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.330	0.069	0.370	0.056			A to X
0.291	0.069	0.238	0.056			S to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
A	1
S	1

Pin Name	Output Loading Factor (Iu)
X	1

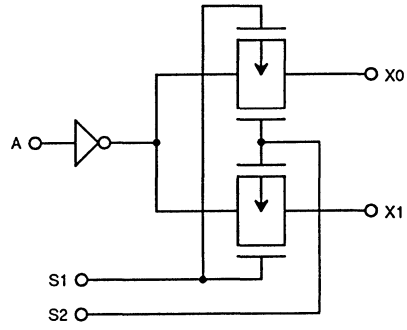
Pin Name	Output Driving Factor (Iu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

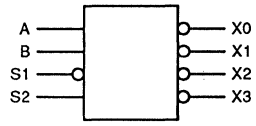
Inputs			Outputs	
A	S1	S2	X0	X1
L	L	L	Inhibit	
L	H	L	X	H
L	L	H	H	X
L	H	H	Inhibit	
H	L	L		
H	H	L	X	L
H	L	H	L	X
H	H	H	Inhibit	

Equivalent Circuit



Cell Name	Function	Number of BC
V3B	Dual 1 : 2 Selector	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.337	0.069	0.403	0.056			A,B to X
0.304	0.069	0.258	0.056			S to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	1
B	1
S	2

Pin Name	Output Loading Factor (lu)
X	1

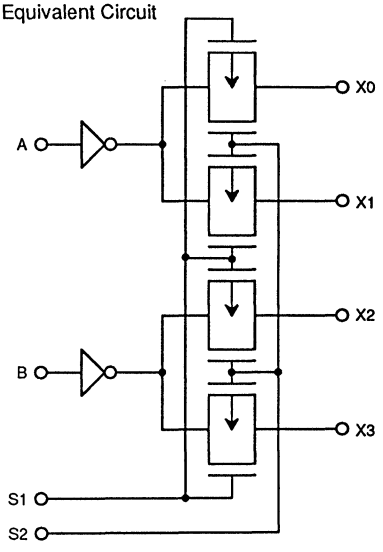
Pin Name	Output Driving Factor (lu)
X	14

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Function Table

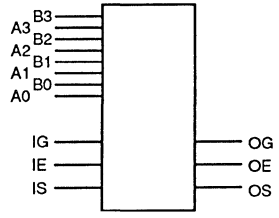
Inputs			Outputs	
A,B	S1	S2	X0, X2	X1, X3
L	L	L	Inhibit	
L	H	L	X	H
L	L	H	H	X
L	H	H	Inhibit	
H	L	L		
H	H	L	X	L
H	L	H	L	X
H	H	H	Inhibit	

Equivalent Circuit



Cell Name	Function	Number of BC
MC4	4–bit Magnitude Comparator	42

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
2.792	0.106	3.340	0.039	0.050	4	A to OS
2.845	0.106	3.280	0.039	0.050	4	B to OS
1.248	0.106	1.472	0.039	0.050	4	IE to OS
1.023	0.106	1.274	0.039	0.050	4	IG to OS
2.739	0.106	3.452	0.039	0.050	4	A to OG
2.785	0.106	3.393	0.039	0.050	4	B to OG
1.188	0.106	1.578	0.039	0.050	4	IE to OG
1.129	0.106	1.221	0.039	0.050	4	IS to OG
3.003	0.060	2.304	0.039	0.056	4	A to OE
2.950	0.060	2.350	0.039	0.056	4	B to OE
1.129	0.060	0.759	0.039	0.056	4	IE to OE

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
A	3
B	3
IE	1
IG	1
IS	1

Pin Name	Output Driving Factor (lu)
OE	18
OG	10
OS	10

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

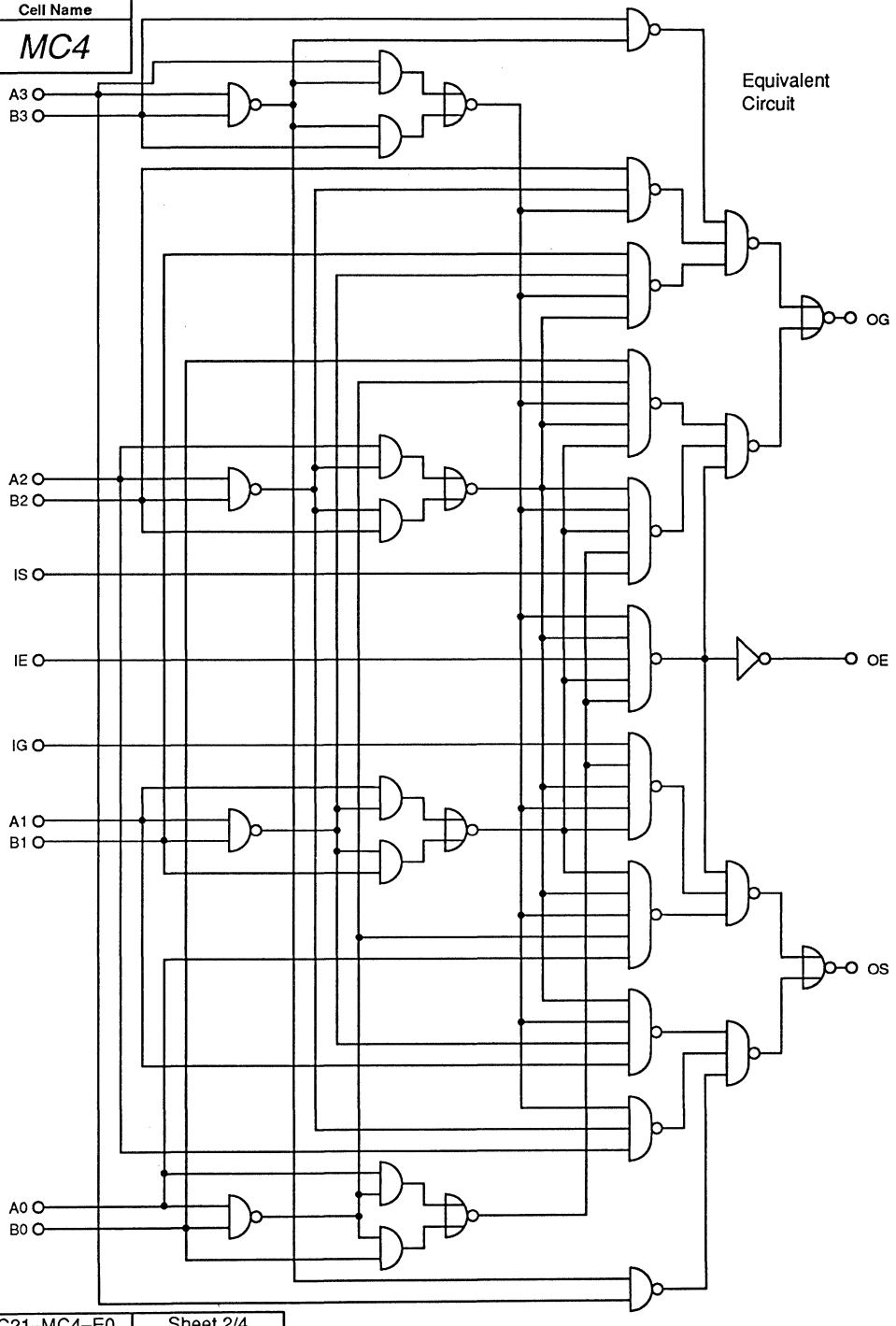
Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	IG (A>B)	IS (A<B)	IE (A=B)	OG (A>B)	OS (A<B)	OE (A=B)
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

Cell Name

MC4

Equivalent Circuit

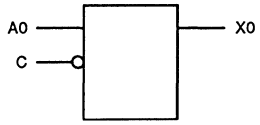


Bus Driver Family

Page	Unit Cell Name	Function	Basic Cells
3–319	B11	1-bit Bus Driver	5
3–320	B21	2-bit Bus Driver	9
3–321	B41	4-bit Bus Driver	17
3–322	B81	8-bit Bus Driver	33
3–323	B12	1-bit Block Bus Driver	7
3–324	B22	2-bit Block Bus Driver	13
3–325	B42	4-bit Block Bus Driver	25

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
B11	1–bit Bus Driver	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.759	0.028	0.759	0.023			A to X
0.858	0.028	0.858	0.023			C to X

Parameter	Symbol	Typ (ns) *

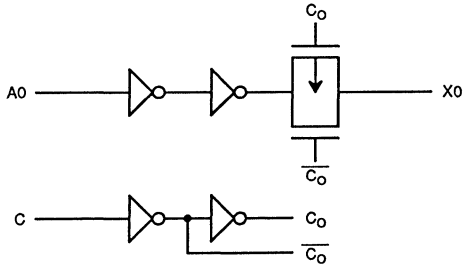
Pin Name	Input Loading Factor (lu)
A	1
C	1

Pin Name	Output Loading Factor (lu)
X	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

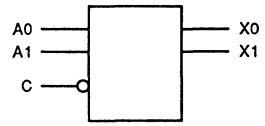
Equivalent Circuit



C21–B11–E0	Sheet 1/1

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		"CG21K" Version
Cell Name	**Function**	**Number of BC**
B21	2–bit Bus Driver	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.759	0.028	0.759	0.023			A to X
1.419	0.028	1.254	0.023			C to X

Parameter	Symbol	Typ (ns) *

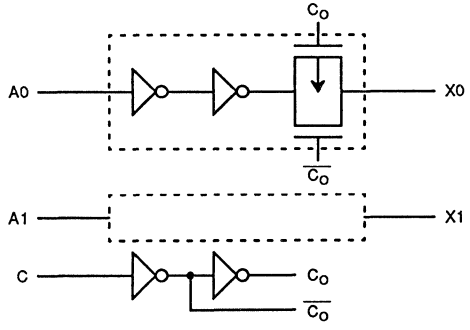
Pin Name	Input Loading Factor (lu)
A	1
C	1

Pin Name	Output Loading Factor (lu)
X	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



C21–B21–E0	Sheet 1/1

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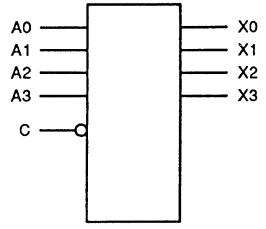
Cell Name	Function	Number of BC
B41	4–bit Bus Driver	17

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.759	0.028	0.759	0.023			A to X
2.310	0.028	1.914	0.023			C to X

Parameter	Symbol	Typ (ns) *

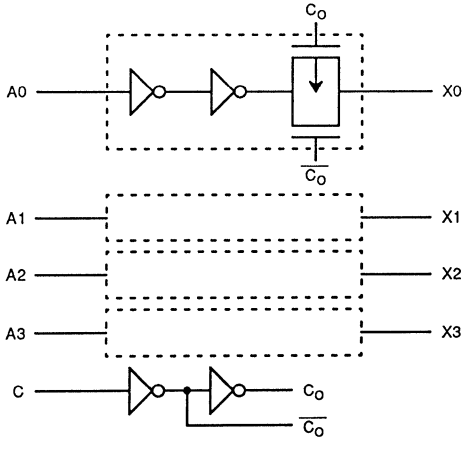
Pin Name	Input Loading Factor (Iu)
A	1
C	1

Pin Name	Output Loading Factor (Iu)
X	1

Pin Name	Output Driving Factor (Iu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

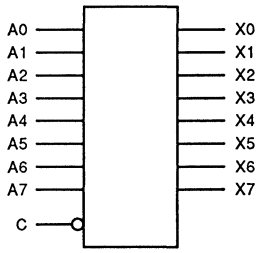
Equivalent Circuit



C21–B41–E0 | Sheet 1/1

Cell Name	Function	Number of BC
B81	8–bit Bus Driver	33

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.759	0.028	0.759	0.023			A to X
4.422	0.028	3.630	0.023			C to X

Parameter	Symbol	Typ (ns) *

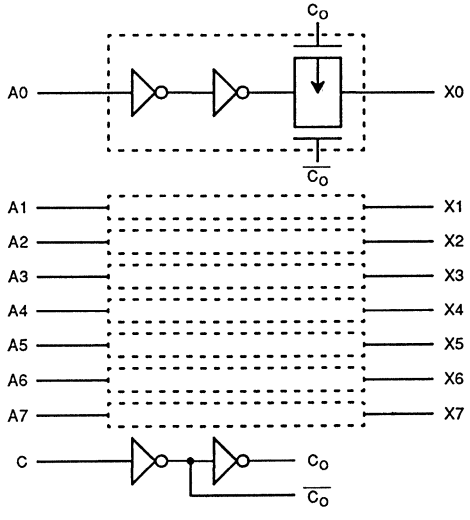
Pin Name	Input Loading Factor (lu)
A	1
C	1

Pin Name	Output Loading Factor (lu)
X	1

Pin Name	Output Driving Factor (lu)
X	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



C21–B81–E0 | Sheet 1/1

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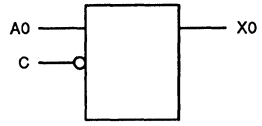
Cell Name	Function	Number of BC
B12	1-bit Block Bus Driver	7

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.759	0.019	1.287	0.011			A to X
0.957	0.019	1.617	0.011			C to X

Parameter	Symbol	Typ (ns) *

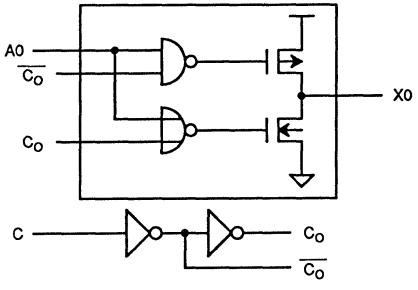
Pin Name	Input Loading Factor (lu)
A	2
C	1

Pin Name	Output Loading Factor (lu)
X	2

Pin Name	Output Driving Factor (lu)
X	72

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

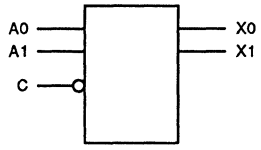
Equivalent Circuit



Note :
This cell is for inter-block bus under chip level.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
B22	2–bit Block Bus Driver	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.759	0.019	1.287	0.011			A to X
1.056	0.019	1.848	0.011			C to X

Parameter	Symbol	Typ (ns) *

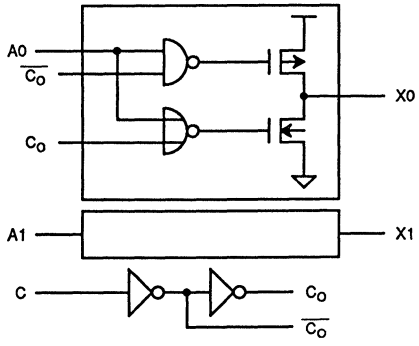
Pin Name	Input Loading Factor (lu)
A	2
C	1

Pin Name	Output Loading Factor (lu)
X	2

Pin Name	Output Driving Factor (lu)
X	72

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



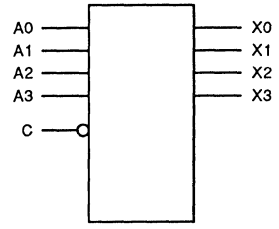
Note :
This cell is for inter–block bus under chip level.

C21–B22–E0 | Sheet 1/1

Page 18–6

Cell Name	Function	Number of BC
B42	4–bit Block Bus Driver	25

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.759	0.019	1.287	0.011			A to X
1.320	0.019	2.046	0.011			C to X

Parameter	Symbol	Typ (ns) *

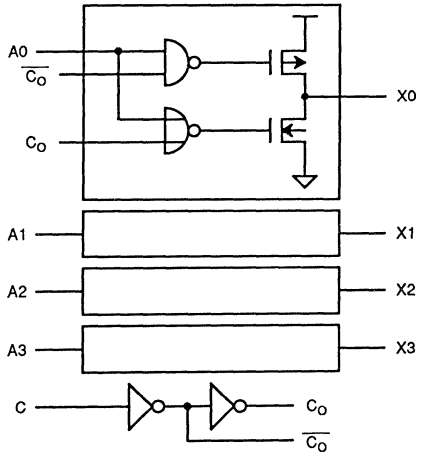
Pin Name	Input Loading Factor (lu)
A	2
C	1

Pin Name	Output Loading Factor (lu)
X	2

Pin Name	Output Driving Factor (lu)
X	72

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Equivalent Circuit



Note :
This cell is for inter–block bus under chip level.

3

Clip Cell Family

Page	Unit Cell Name		Function	Basic Cells
3–329	Z00	0 Clip		0
3–330	Z01	1 Clip		0

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
Z00	0 Clip	0

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
X	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
Z01	1 Clip	0

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
X	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

I/O Buffer Family

Page	Unit Cell Name	Function	Basic Cells
3–335	I1B	Input Buffer (Inverter)	5
3–336	I1BU	I1B with Pull-up Resistance	5
3–337	I1BD	I1B with Pull-down Resistance	5
3–338	I2B	Input Buffer (True)	4
3–339	I2BU	I2B with Pull-up Resistance	4
3–340	I2BD	I2B with Pull-down Resistance	4
3–341	IKB	Clock Input Buffer (Inverter)	4
3–342	IKBU	IKB with Pull-up Resistance	4
3–343	IKBD	IKB with Pull-down Resistance	4
3–444	IKC	CMOS Interface Clock Input Buffer (Inverter)	4
3–445	IKCU	IKC with Pull-up Resistance	4
3–446	IKCD	IKC with Pull-down Resistance	4
3–347	ILB	Clock Input Buffer (True)	8
3–348	ILBU	ILB with Pull-up Resistance	8
3–349	ILBD	ILB with Pull-down Resistance	8
3–350	ILC	CMOS Interface Clock Input Buffer (True)	6
3–351	ILCU	ILC with Pull-up Resistance	6
3–352	ILCD	ILC with Pull-down Resistance	6
3–353	I1C	CMOS Interface Input Buffer (Inverter)	5
3–354	I1CU	I1C with Pull-up Resistance	5
3–355	I1CD	I1C with Pull-down Resistance	5
3–356	I2C	CMOS Interface Input Buffer (True)	4
3–357	I2CU	I2C with Pull-up Resistance	4
3–358	I2CD	I2C with Pull-down Resistance	4
3–359	I1S	Schmitt Trigger Input Buffer (CMOS Type, Inverter)	8
3–360	I1SU	I1S with Pull-up Resistance	8
3–361	I1SD	I1S with Pull-down Resistance	8
3–362	I2S	Schmitt Trigger Input Buffer (CMOS Type, True)	8
3–363	I2SU	I2S with Pull-up Resistance	8
3–364	I2SD	I2S with Pull-down Resistance	8
3–365	I1R	Schmitt Trigger Input Buffer (TTL Type, Inverter)	8
3–366	I1RU	I1R with Pull-up Resistance	8
3–367	I1RD	I1R with Pull-down Resistance	8
3–368	I2R	Schmitt Trigger Input Buffer (TTL Type, True)	8
3–369	I2RU	I2R with Pull-up Resistance	8
3–370	I2RD	I2R with Pull-down Resistance	8
3–371	O1B[1]	Output Buffer (Inverter)	3
3–372	O1BF[2]	Output Buffer (Inverter)	3
3–373	O1L[3]	Power Output Buffer (Inverter)	3
3–374	O1R[1]	Output Buffer (Inverter) with Noise Limit Resistance	5
3–375	O1RF[2]	Output Buffer (Inverter) with Noise Limit Resistance	5
3–376	O1S[3]	Power Output Buffer (Inverter) with Noise Limit Resistance	5
3–377	O2B[1]	Output Buffer (True)	3
3–378	O2BF[2]	Output Buffer	3
3–379	O2L[3]	Power Output Buffer (True)	3
3–380	O2R[1]	Output Buffer (True) with Noise Limit Resistance	4
3–381	O2RF[2]	Output Buffer with Noise Limit Resistance	4

1. I_{OL} = 3.2 mA
2. I_{OL} = 8 mA
3. I_{OL} = 12 mA

I/O Buffer Family (Continued)

Page	Unit Cell Name	Function	Basic Cells
3–382	O2S[3]	Power Output Buffer (True) with Noise Limit Resistance	4
3–383	O4T[1]	3-state Output Buffer (True)	6
3–384	O4TF[2]	3-state Output Buffer (True)	6
3–385	O4W[3]	Power 3-state Output Buffer (True)	6
3–386	O4R[1]	3-state Output Buffer (True) with Noise Limit Resistance	5
3–387	O4RF[2]	3-state Output Buffer (True) with Noise Limit Resistance	5
3–388	O4S[3]	Power 3-state Output Buffer (True) with Noise Limit Resistance	5
3–389	H6T[1]	3-state Output and Input Buffer (True)	8
3–390	H6TU	H6T with Pull-up Resistance	8
3–391	H6TD[1]	H6T with Pull-down Resistance	8
3–392	H6TF[2]	3-state Output and Input Buffer (True)	8
3–393	H6TFU[2]	H6TF with Pull-up Resistance	8
3–394	H6TFD[2]	H6TF with Pull-down Resistance	8
3–395	H6W[3]	Power 3-state Output and Input Buffer (True)	8
3–396	H6WU[3]	H6W with Pull-up Resistance	8
3–397	H6WD[3]	H6W with Pull-down Resistance	8
3–398	H6C[1]	3-state Output and CMOS Interface Input Buffer (True)	8
3–399	H6CU[1]	H6C with Pull-up Resistance	8
3–400	H6CD[1]	H6C with Pull-down Resistance	8
3–401	H6CF[2]	3-state Output and CMOS Interface Input Buffer	8
3–402	H6CFU[2]	H6CF with Pull-up Resistance	8
3–403	H6CFD[2]	H6CF with Pull-down Resistance	8
3–404	H6E[3]	Power 3-state Output and CMOS Interface Input Buffer (True)	8
3–405	H6EU[3]	H6E with Pull-up Resistance	8
3–406	H6ED[3]	H6E with Pull-down Resistance	8
3–407	H6S[1]	3-state Output and Schmitt Trigger Input Buffer (CMOS Type, True)	12
3–408	H6SU[1]	H6S with Pull-up Resistance	12
3–409	H6SD[1]	H6S with Pull-down Resistance	12
3–410	H6R[1]	3-state Output and Schmitt Trigger Input Buffer (TTL Type, True)	12
3–411	H6RU[1]	H6R with Pull-up Resistance	12
3–412	H6RD[1]	H6R with Pull-down Resistance	12
3–413	H8T[1]	3-state Output with Noise Limit Resistance and Input Buffer (True)	9
3–414	H8TU[1]	H8T with Pull-up Resistance	9
3–415	H8TD[1]	H8T with Pull-down Resistance	9
3–416	H8TF[2]	3-state Output with Noise Limit Resistance and Input Buffer True)	9
3–417	H8TFU[2]	H8TF with Pull-up Resistance	9
3–418	H8TFD[2]	H8TF with Pull-down Resistance	9
3–419	H8W[3]	Power 3-state Output with Noise Limit Resistance and Input Buffer (True)	9

1. I_{OL} = 3.2 mA
2. I_{OL} = 8 mA
3. I_{OL} = 12 mA

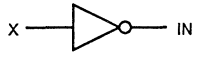
I/O Buffer Family (Continued)

Page	Unit Cell Name	Function	Basic Cells
3–420	H8WU[3]	H8W with Pull-up Resistance	9
3–421	H8WD[3]	H8W with Pull-down Resistance	9
3–422	H8C[1]	3-state Output Buffer with Noise Limit Resistance and CMOS Interface Input Buffer (True)	9
3–423	H8CU[1]	H8C with Pull-up Resistance	9
3–424	H8CD[1]	H8C with Pull-down Resistance	9
3–425	H8CF[2]	3-state Output Buffer with Noise Limit Resistance and CMOS Interface Input Buffer (True)	9
3–426	H8CFU[2]	H8CF with Pull-up Resistance	9
3–427	H8CFD[2]	H8CF with Pull-down Resistance	9
3–428	H8E[3]	Power 3-state Output Buffer with Noise Limit Resistance and CMOS Interface Input Buffer (True)	9
3–429	H8EU[3]	H8E with Pull-up Resistance	9
3–430	H8ED[3]	H8E with Pull-down Resistance	9
3–431	H8S[1]	3-state Output and Schmitt Trigger Input Buffer (CMOS Type, True) with Noise Limit Resistance	13
3–432	H8SU[1]	H8S with Pull-up Resistance	13
3–433	H8SD[1]	H8S with Pull-down Resistance	13
3–434	H8R[1]	3-state Output and Schmitt Trigger Input Buffer (TTL Type, True) with Noise Limit Resistance	13
3–435	H8RU[1]	H8R with Pull-up Resistance	13
3–436	H8RD[1]	H8R with Pull-down Resistance	13

1. I_{OL} = 3.2 mA
2. I_{OL} = 8 mA
3. I_{OL} = 12 mA

Cell Name	Function	Number of BC
I1B	Input Buffer (Inverter)	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.845	0.014	0.812	0.017			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I1BU	Input Buffer (Inverter) with Pull-up Resistance	5

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.845	0.014	0.812	0.017			X to IN

Parameter	Symbol	Typ (ns) *

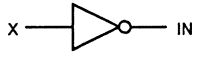
Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I1BD	Input Buffer (Inverter) with Pull–down Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.845	0.014	0.812	0.017			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I2B	Input Buffer (True)	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561	0.014	0.970	0.017			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I2BU	Input Buffer (True) with Pull–pu Resistance	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561	0.014	0.970	0.017			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I2BD	Input Buffer (True) with Pull–down Resistance	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.561	0.014	0.970	0.017			X to IN

Parameter	Symbol	Typ (ns) *

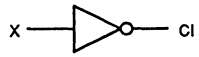
Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
IKB	Clock Input Buffer (Inverter)	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.540	0.004	1.020	0.004			X to CI

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
IKBU	Clock Input Buffer (Inverter) with Pull–up Resistance	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.540	0.004	1.020	0.004			X to CI

Parameter	Symbol	Typ (ns) *

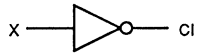
Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
IKBD	Clock Input Buffer (Inverter) with Pull–down Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.540	0.004	1.020	0.004			X to CI

Parameter	Symbol	Typ (ns) *

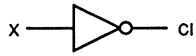
Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
IKC	CMOS Interface Clock Input Buffer (Inverter)	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.310	0.004	0.980	0.004			X to CI

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
IKCU	CMOS Interface Clock Input Buffer (Inverter) with Pull–up Resistance	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.310	0.004	0.980	0.004			X to CI

Parameter	Symbol	Typ (ns) *

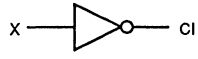
Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
IKCD	CMOS Interface Clock Input Buffer (Inverter) with Pull–down Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.310	0.004	0.980	0.004			X to CI

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *OG21K* " Version
Cell Name	**Function**	**Number of BC**
ILB	Clock Input Buffer (True)	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.560	0.004	1.330	0.004			X to CI

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
ILBU	Clock Input Buffer (True) with Pull-up Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.560	0.004	1.330	0.004			X to CI

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
ILBD	Clock Input Buffer (True) with Pull–down Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.560	0.004	1.330	0.004			X to CI

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
ILC	CMOS Interface Clock Input Buffer (True)	6

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.880	0.004	1.550	0.004			X to CI

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
ILCU	CMOS Interface Clock Input Buffer (True) with Pull–up Resistance	6

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.880	0.004	1.550	0.004			X to CI

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
ILCD	CMOS Interface Clock Input Buffer (True) with Pull–down Resistance	6

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.880	0.004	1.550	0.004			X to CI

Parameter	Symbol	Typ (ns) *

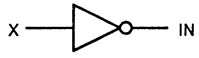
Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
CI	200

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
I1C	CMOS Interface Input Buffer (Inverter)	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.387	0.014	0.210	0.017			X to IN

Parameter	Symbol	Typ (ns) *

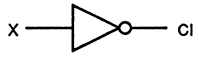
Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I1CU	CMOS Interface Input Buffer (Inverter) with Pull-up Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.387	0.014	0.210	0.017			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I1CD	CMOS Interface Input Buffer (Inverter) with Pull–down Resistance	5

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.387	0.014	0.210	0.017			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I2C	CMOS Interface Input Buffer (True)	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489	0.014	0.706	0.017			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" CG21K " Version
Cell Name	**Function**	**Number of BC**
I2CU	CMOS Interface Input Buffer with Pull–up Resistance (True)	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.489	0.014	0.706	0.017			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I2CD	CMOS Interface Input Buffer with Pull–down Resistance (True)	4

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489	0.014	0.706	0.017			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	36

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
I1S	Schmitt Trigger Input Buffer (CMOS Type, Inverter)	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.059	0.060	1.419	0.039			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I1SU	Schmitt Trigger Input Buffer (CMOS Type, Inverter) with Pull–up Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
2.059	0.060	1.419	0.039			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I1SD	Schmitt Trigger Input Buffer (CMOS Type, Inverter) with Pull–down Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.059	0.060	1.419	0.039			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I2S	Schmitt Trigger Input Buffer (CMOS Type, True)	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314	0.060	1.630	0.045			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
I2SU	Schmitt Trigger Input Buffer (CMOS Type, True) with Pull–up Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314	0.060	1.630	0.045			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I2SD	Schmitt Trigger Input Buffer (CMOS Type, True) with Pull–down Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314	0.060	1.630	0.045			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)

Pin Name	Output Driving Factor (lu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
I1R	Schmitt Trigger Input Buffer (TTL Type, Inverter)	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.370	0.060	1.248	0.039			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I1RU	Schmitt Trigger Input Buffer (TTL Type, Inverter) with Pull–up Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.370	0.060	1.248	0.039			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
I1RD	Schmitt Trigger Input Buffer (TTL Type, Inverter) with Pull–down Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.370	0.060	1.248	0.039			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I2R	Schmitt Trigger Input Buffer (TTL Type, True)	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.182	0.060	1.967	0.062			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
I2RU	Schmitt Trigger Input Buffer (TTL Type, True) with Pull–up Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.182	0.060	1.967	0.062			X to IN

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
I2RD	Schmitt Trigger Input Buffer (TTL Type, True) with Pull–down Resistance	8

Cell Symbol

Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.182	0.060	1.967	0.062			X to IN

Parameter	Symbol	Typ (ns) *

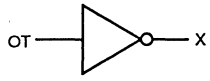
Pin Name	Input Loading Factor (Iu)

Pin Name	Output Driving Factor (Iu)
IN	18

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

Cell Name	Function	Number of BC
O1B	Output Buffer (Inverter)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.790 (2.47)	0.028	1.060 (4.24)	0.053			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	2

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

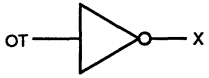
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
O1BF	Output Buffer (IOL=8mA, Inverter)	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.830 (2.51)	0.028	1.070 (3.47)	0.040			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	2

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

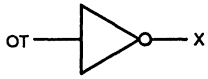
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O1L	Power Output Buffer (Inverter)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.900 (2.10)	0.020	1.240 (2.80)	0.026			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	2

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

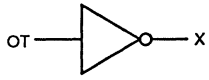
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
O1R	Output Buffer (Inverter) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.730 (3.89)	0.036	4.540 (9.40)	0.081			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	1

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

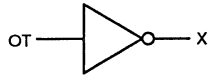
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O1RF	Output Buffer (IOL=8mA, Inverter) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.780 (3.94)	0.036	5.690 (8.57)	0.048			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	1

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

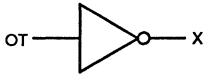
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
O1S	Power Output Buffer (Inverter) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
2.040 (3.48)	0.024	6.720 (9.12)	0.040			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	1

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

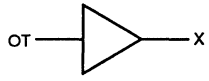
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O2B	Output Buffer (True)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.500 (2.18)	0.028	0.820 (4.00)	0.053			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	6

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

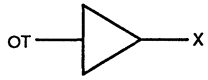
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
O2BF	Output Buffer (IOL=8mA, True)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.560 (2.24)	0.048	0.850 (3.25)	0.040			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	6

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

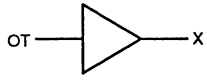
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O2L	Power Output Buffer (True)	3

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.640 (1.84)	0.020	1.020 (2.58)	0.026			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	6

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

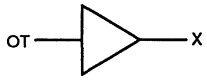
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O2R	Output Buffer (True) with Noise Limit Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.510 (3.67)	0.036	4.400 (9.26)	0.081			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (Iu)
OT	2

Pin Name	Output Driving Factor (Iu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

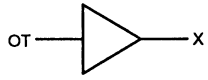
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O2RF	Output Buffer (IOL=8mA, True) with Noise Limit Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.570 (3.73)	0.036	5.600 (8.48)	0.048			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
OT	2

Pin Name	Output Driving Factor (lu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

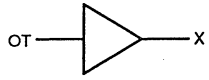
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
O2S	Power Output Buffer (True) with Noise Limit Resistance	4

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.820 (3.26)	0.024	6.560 (8.96)	0.040			OT to X

Parameter	Symbol	Typ (ns) *

Pin Name	Input Loading Factor (lu)
OT	2

Pin Name	Output Driving Factor (lu)

* Minimum values for the typical operating condition.
The values for the worst case operating condition are given by the maximum delay multiplier.

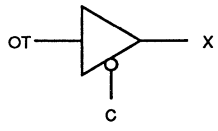
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 60 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O4T	Tri-state Output Buffer (True)	6

Cell Symbol



Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)

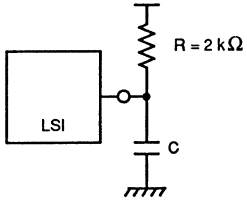
Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.710 (2.53)	0.028	1.460 (4.91)	0.053			OT to X

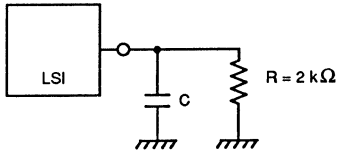
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.000 (15.00)	*	1.550 (5.13)	0.055	

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (15.00)	*	0.740 (5.13)	0.028	

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

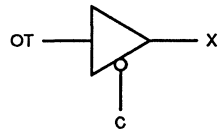


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL is ns/pF.
2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O4TF	Tri-state Output Buffer (IOL=8mA, True)	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.750 (2.57)	0.028	1.480 (4.08)	0.040			OT to X

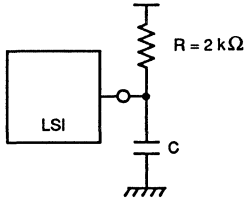
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.200 (15.80)	*	1.650 (4.32)	0.041	

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (15.80)	*	0.750 (4.32)	0.028	

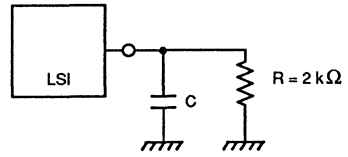
Pin Name	Input Loading Factor (lu)
OT	6
C	2

Pin Name	Output Driving Factor (lu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

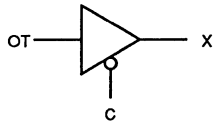
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O4W	Power Tri-state Output Buffer (True)	6

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.860 (2.16)	0.020	1.580 (3.47)	0.029			OT to X

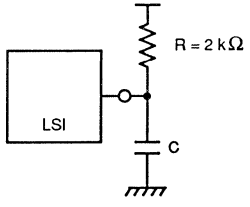
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.800 (16.70)	*	1.550 (3.50)	0.030	

H to Z		Z to H		
t0	KCL	t0	KCL	
3.300 (16.70)	*	0.800 (3.50)	0.020	

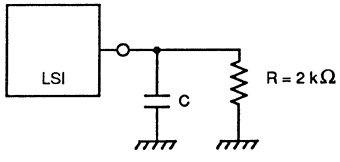
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

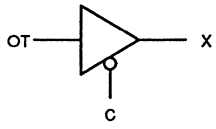
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
O4R	Tri–state Output Buffer (True) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.570 (3.91)	0.036	4.720 (9.99)	0.081			OT to X

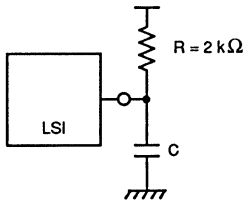
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (14.20)	*	4.600 (9.87)	0.081	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
1.900 (14.20)	*	1.600 (9.87)	0.036	

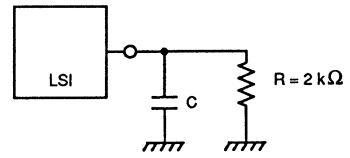
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

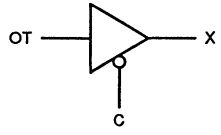
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
O4RF	Tri-state Output Buffer (IOL=8mA, True) with Noise Limit Resistance	5

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.730 (4.07)	0.036	5.950 (9.07)	0.048			OT to X

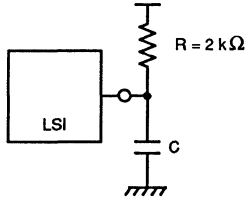
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.100 (16.10)	*	5.650 (8.97)	0.051	

H to Z		Z to H		
t0	KCL	t0	KCL	
2.650 (16.10)	*	1.600 (8.97)	0.036	

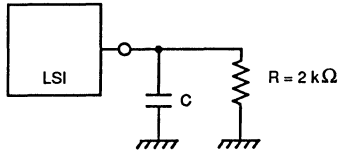
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL is ns/pF.

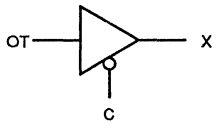
2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

3

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
O4S	Power Tri-state Output Buffer (True) with Noise Limit Resistance	5

Cell Symbol



Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)

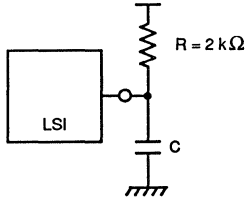
Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
2.170 (3.73)	0.024	6.900 (9.50)	0.040			OT to X

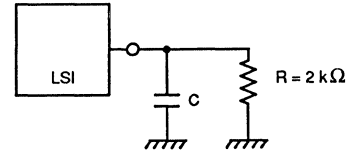
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.500 (16.80)	*	6.750 (9.42)	0.041	

H to Z		Z to H		
t0	KCL	t0	KCL	
3.500 (16.80)	*	1.800 (9.42)	0.025	

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

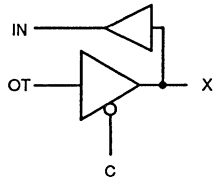
Note: 1. The unit of KCL is ns/pF.

2. Output load capacitance of 65 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6T	Tri-state Output & Input Buffer (True)	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 0.710 (3.09)	0.014 0.028	0.970 1.460 (5.97)	0.017 0.053			X to IN OT to X

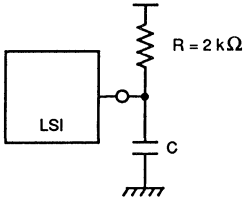
L to Z		Z to L		
t0	KCL	t0	KCL	
2.000 (19.20)	*	1.550 (6.23)	0.055	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (19.20)	*	0.740 (6.23)	0.028	

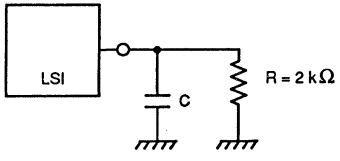
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

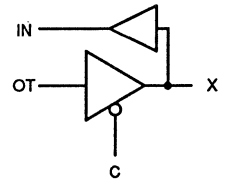
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6TU	Tri-state Output & Input Buffer (True) with Pull-up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 0.710 (3.09)	0.014 0.028	0.970 1.460 (5.97)	0.017 0.053			X to IN OT to X

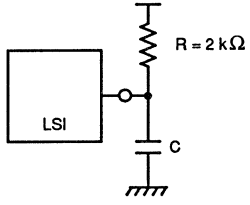
L to Z		Z to L		
t0	KCL	t0	KCL	
2.000 (19.20)	*	1.550 (6.23)	0.055	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (19.20)	*	0.740 (6.23)	0.028	

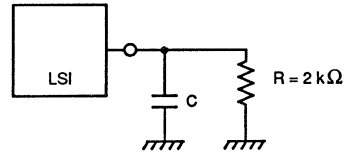
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

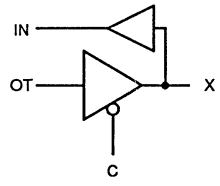
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6TD	Tri–state Output & Input Buffer (True) with Pull–down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 0.710 (3.09)	0.014 0.028	0.970 1.460 (5.97)	0.017 0.053			X to IN OT to X

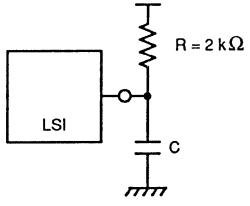
L to Z		Z to L		
t0	KCL	t0	KCL	
2.000 (19.20)	*	1.550 (6.23)	0.055	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
2.600 (19.20)	*	0.740 (6.23)	0.028

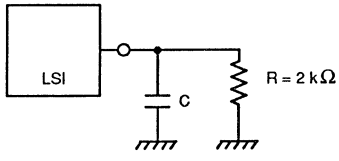
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

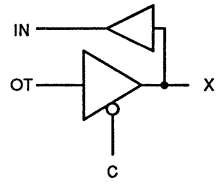
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6TF	Tri–state Output & Input Buffer (IOL=8mA, True)	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 0.750 (3.13)	0.014 0.028	0.970 1.480 (4.88)	0.017 0.040			X to IN OT to X

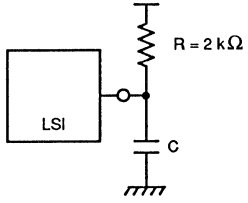
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.200 (20.10)	*	1.650 (5.14)	0.041	

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (20.10)	*	0.750 (5.14)	0.028	

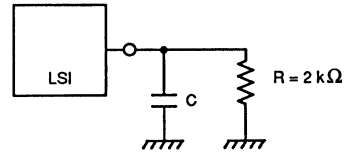
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

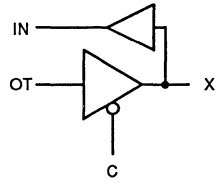
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6TFU	Tri-state Output & Input Buffer (IOL=8mA, True) with Pull-up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 0.750 (3.13)	0.014 0.028	0.970 1.480 (4.88)	0.017 0.040			X to IN OT to X

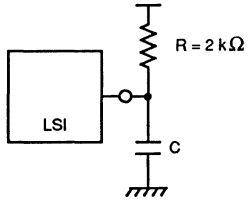
L to Z		Z to L		
t0	KCL	t0	KCL	
2.200 (20.10)	*	1.650 (5.14)	0.041	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (20.10)	*	0.750 (5.14)	0.028	

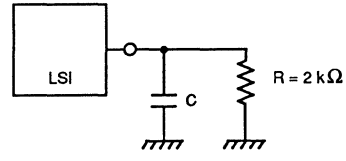
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

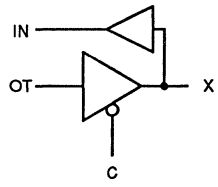
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6TFD	Tri–state Output & Input Buffer (IOL=8mA, True) with Pull–down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 0.750 (3.13)	0.014 0.028	0.970 1.480 (4.88)	0.017 0.040			X to IN OT to X

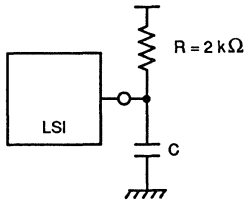
L to Z		Z to L		
t0	KCL	t0	KCL	
2.200 (20.10)	*	1.650 (5.14)	0.041	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (20.10)	*	0.750 (5.14)	0.028	

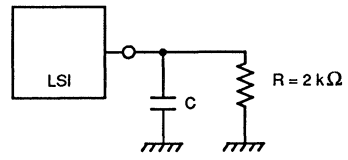
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

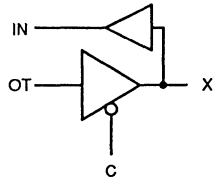
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6W	Power Tri-state Output & Input Buffer (True)	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 0.860 (2.56)	0.014 0.020	0.970 1.580 (4.05)	0.017 0.029			X to IN OT to X

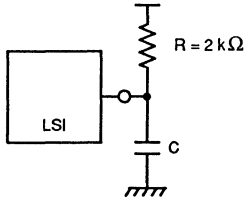
L to Z		Z to L		
t0	KCL	t0	KCL	
2.800 (21.00)	*	1.550 (4.10)	0.030	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
3.300 (21.00)	*	0.800 (4.10)	0.020	

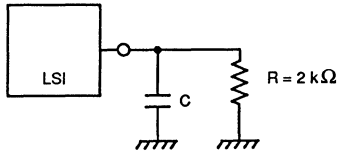
Pin Name	Input Loading Factor (lu)
OT	6
C	2

Pin Name	Output Driving Factor (lu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

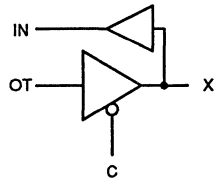
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6WU	Power Tri-state Output & Input Buffer (True) with Pull-up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 0.860 (2.56)	0.014 0.020	0.970 1.580 (4.05)	0.017 0.029			X to IN OT to X

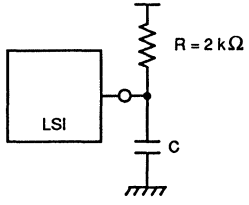
L to Z		Z to L		
t0	KCL	t0	KCL	
2.800 (21.00)	*	1.550 (4.10)	0.030	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
3.300 (21.00)	*	0.800 (4.10)	0.020	

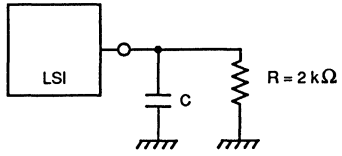
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

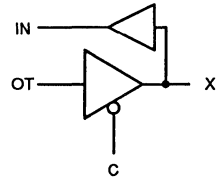


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6WD	Power Tri-state Output & Input Buffer (True) with Pull-down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 0.860 (2.56)	0.014 0.020	0.970 1.580 (4.05)	0.017 0.029			X to IN OT to X

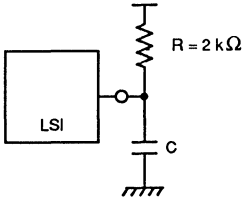
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.800 (21.00)	*	1.550 (4.10)	0.030	

H to Z		Z to H		
t0	KCL	t0	KCL	
3.300 (21.00)	*	0.800 (4.10)	0.020	

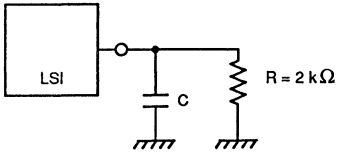
Pin Name	Input Loading Factor (lu)
OT	6
C	2

Pin Name	Output Driving Factor (lu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

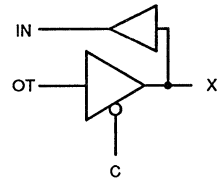
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6C	Tri-state Output & CMOS Interface Input Buffer (True)	10

Cell Symbol



Pin Name	Input Loading Factor (lu)
OT	6
C	2

Pin Name	Output Driving Factor (lu)
IN	36

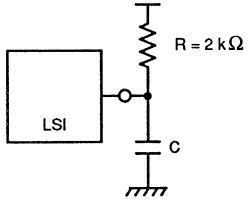
Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 0.710 (3.09)	0.014 0.028	0.706 1.460 (5.97)	0.017 0.053			X to IN OT to X

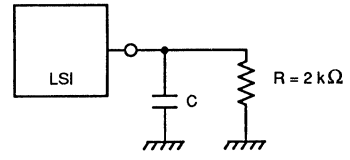
L to Z		Z to L		
t0	KCL	t0	KCL	
2.000 (19.20)	*	1.550 (6.23)	0.055	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (19.20)	*	0.740 (6.23)	0.028	

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

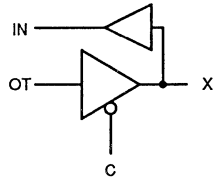


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6CU	Tri–state Output & CMOS Interface Input Buffer (True) with Pull–up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 0.710 (3.09)	0.014 0.028	0.706 1.460 (5.97)	0.017 0.053			X to IN OT to X

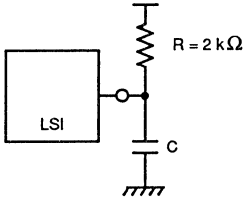
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.000 (19.20)	*	1.550 (6.23)	0.055	

H to Z		Z to H	
t0	KCL	t0	KCL
2.600 (19.20)	*	0.740 (6.23)	0.028

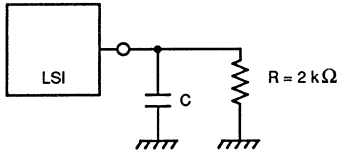
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

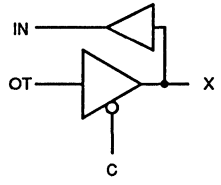
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6CD	Tri–state Output & CMOS Interface Input Buffer (True) with Pull–down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 0.710 (3.09)	0.014 0.028	0.706 1.460 (5.97)	0.017 0.053			X to IN OT to X

L to Z		Z to L		
t0	KCL	t0	KCL	
2.000 (19.20)	*	1.550 (6.23)	0.055	C to X

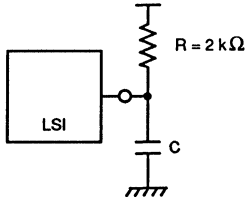
H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (19.20)	*	0.740 (6.23)	0.028	

Pin Name	Input Loading Factor (Iu)
OT C	6 2

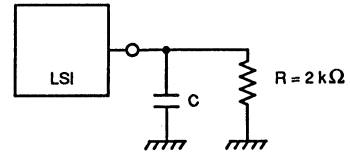
Pin Name	Output Driving Factor (Iu)
IN	36

3

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

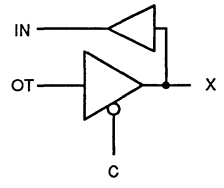
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6CF	Tri-state Output & CMOS Interface Input Buffer (IOL=8mA, True)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 0.750 (3.13)	0.014 0.028	0.706 1.480 (4.88)	0.017 0.040			X to IN OT to X

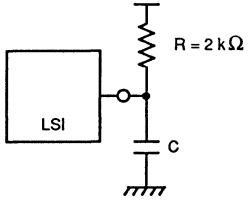
L to Z		Z to L		
t0	KCL	t0	KCL	
2.200 (20.10)	*	1.650 (5.14)	0.041	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (20.10)	*	0.750 (5.14)	0.028	

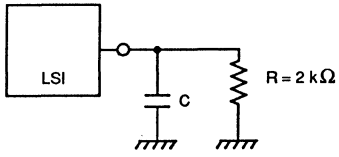
Pin Name	Input Loading Factor (Iu)
OT	4
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

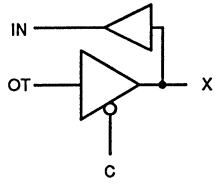
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6CFU	Tri–state Output & CMOS Interface Input Buffer with Pull–up Resistance (IOL=8mA, True)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 0.750 (3.13)	0.014 0.028	0.706 1.480 (4.88)	0.017 0.040			X to IN OT to X

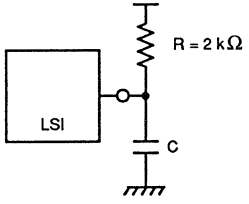
L to Z		Z to L		Path
t0	KCL	t0	KCL	
2.200 (20.10)	*	1.650 (5.14)	0.041	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
2.600 (20.10)	*	0.750 (5.14)	0.028

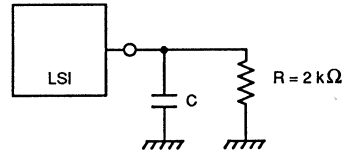
Pin Name	Input Loading Factor (Iu)
OT	4
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

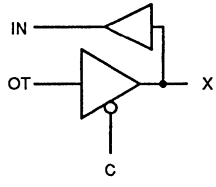
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6CFD	Tri–state Output & CMOS Interface Input Buffer with Pull–down Resistance (IOL=8mA, True)	8

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 0.750 (3.13)	0.014 0.028	0.706 1.480 (4.88)	0.017 0.040			X to IN OT to X

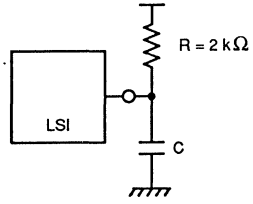
L to Z		Z to L		
t0	KCL	t0	KCL	
2.200 (20.10)	*	1.650 (5.14)	0.041	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
2.600 (20.10)	*	0.750 (5.14)	0.028

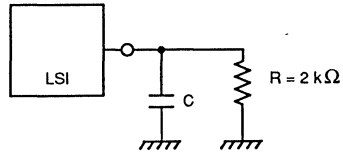
Pin Name	Input Loading Factor (Iu)
OT	4
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

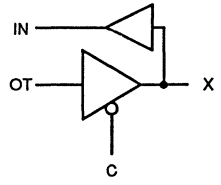
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6E	Power Tri-state Output & CMOS Interface Input Buffer (True)	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 0.860 (2.56)	0.014 0.020	0.706 1.580 (4.05)	0.017 0.029			X to IN OT to X

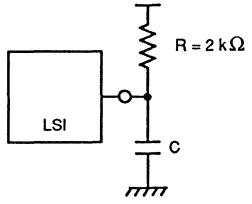
L to Z		Z to L		
t0	KCL	t0	KCL	
2.800 (21.00)	*	1.550 (4.10)	0.030	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
3.300 (21.00)	*	0.800 (4.10)	0.020	

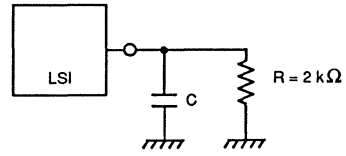
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

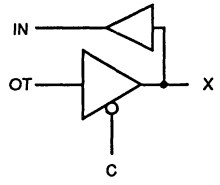
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6EU	Power Tri-state Output & CMOS Interface Input Buffer (True) with Pull-up Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 0.860 (2.56)	0.014 0.020	0.706 1.580 (4.05)	0.017 0.029			X to IN OT to X

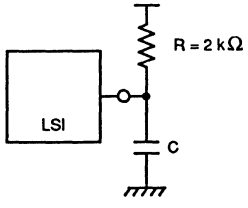
L to Z		Z to L		
t0	KCL	t0	KCL	
2.800 (21.00)	*	1.550 (4.10)	0.030	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
3.300 (21.00)	*	0.800 (4.10)	0.020	

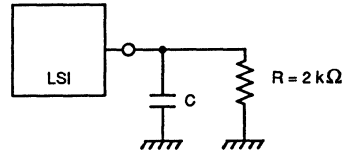
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

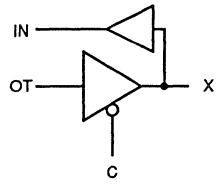
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6ED	Power Tri–state Output & CMOS Interface Input Buffer (True) with Pull–down Resistance	10

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t 0	KCL	t 0	KCL	KCL2	CDR2	
0.489 0.860 (2.56)	0.014 0.020	0.706 1.580 (4.05)	0.017 0.029			X to IN OT to X

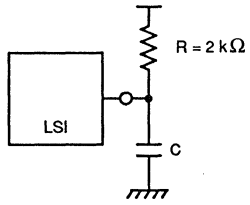
L to Z		Z to L		
t 0	KCL	t 0	KCL	
2.800 (21.00)	*	1.550 (4.10)	0.030	C to X

H to Z		Z to H		
t 0	KCL	t 0	KCL	
3.300 (21.00)	*	0.800 (4.10)	0.020	

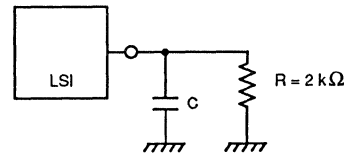
Pin Name	Input Loading Factor (Iu)
OT C	6 2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

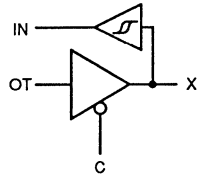
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6S	Tri–state Output & Schmitt Trigger Input Buffer (CMOS Type, True)	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314 0.710 (3.09)	0.060 0.028	1.630 1.460 (5.97)	0.045 0.053			X to IN OT to X

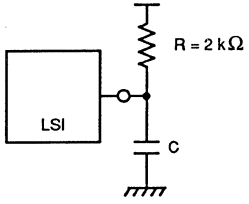
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.000 (19.20)	*	1.550 (6.23)	0.055	

H to Z		Z to H	
t0	KCL	t0	KCL
2.600 (19.20)	*	0.740 (6.23)	0.028

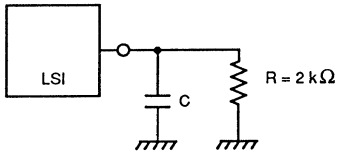
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

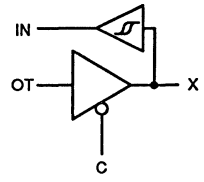
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6SU	Tri–state Output & Schmitt Trigger Input Buffer (CMOS Type, True) with Pull–up Resistance	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314 0.710 (3.09)	0.060 0.028	1.630 1.460 (5.97)	0.045 0.053			X to IN OT to X

L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.000 (19.20)	*	1.550 (6.23)	0.055	

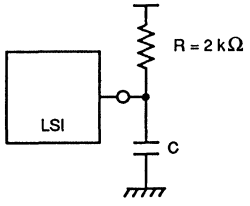
H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (19.20)	*	0.740 (6.23)	0.028	

Pin Name	Input Loading Factor (Iu)
OT	6
C	2

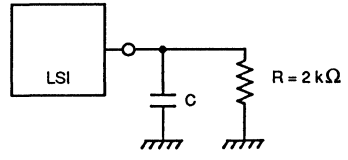
Pin Name	Output Driving Factor (Iu)
IN	18

3

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

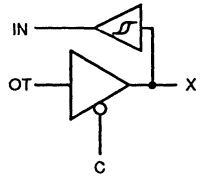
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6SD	Tri–state Output & Schmitt Trigger Input Buffer (CMOS Type, True) with Pull–down Resistance	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314 0.710 (3.09)	0.060 0.028	1.630 1.460 (5.97)	0.045 0.053			X to IN OT to X

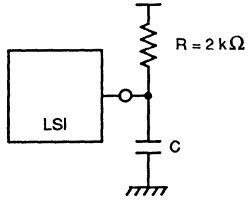
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.000 (19.20)	*	1.550 (6.23)	0.055	

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (19.20)	*	0.740 (6.23)	0.028	

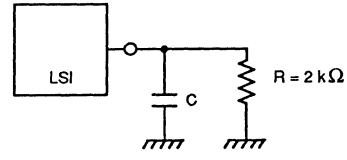
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

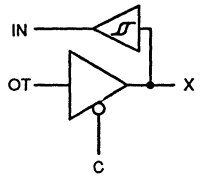
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6R	Tri-state Output & Schmitt Trigger Input Buffer (TTL Type, True)	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.182 0.710 (3.09)	0.060 0.028	1.967 1.460 (5.97)	0.062 0.053			X to IN OT to X

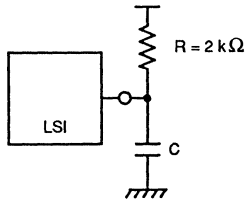
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.000 (19.20)	*	1.550 (6.23)	0.055	

H to Z		Z to H		
t0	KCL	t0	KCL	
2.600 (19.20)	*	0.740 (6.23)	0.028	

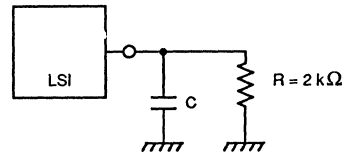
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

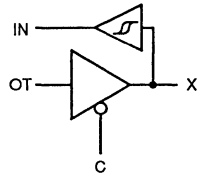


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6RU	Tri–state Output & Schmitt Trigger Input Buffer (TTL Type, True) with Pull–up Resistance	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.182 0.710 (3.09)	0.060 0.028	1.967 1.460 (5.97)	0.062 0.053			X to IN OT to X

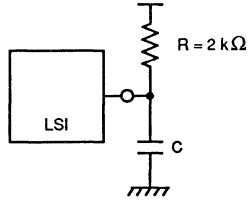
L to Z		Z to L		
t0	KCL	t0	KCL	
2.000 (19.20)	*	1.550 (6.23)	0.055	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
2.600 (19.20)	*	0.740 (6.23)	0.028

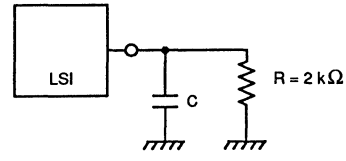
Pin Name	Input Loading Factor (Iu)
OT	6
C	2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

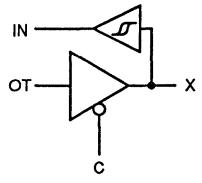
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H6RD	Tri–state Output & Schmitt Trigger Input Buffer (TTL Type, True) with Pull–down Resistance	14

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.182 0.710 (3.09)	0.060 0.028	1.967 1.460 (5.97)	0.062 0.053			X to IN OT to X

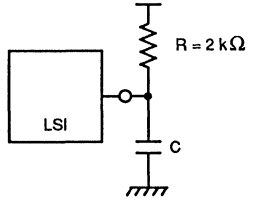
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.000 (19.20)	*	1.550 (6.23)	0.055	

H to Z		Z to H	
t0	KCL	t0	KCL
2.600 (19.20)	*	0.740 (6.23)	0.028

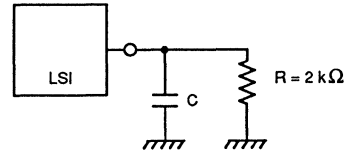
Pin Name	Input Loading Factor (Iu)
OT C	6 2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

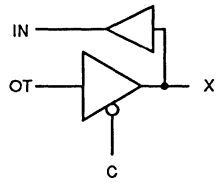
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8T	Tri–state Output with Noise Limit Resistance & Input Buffer (True)	9

Cell Symbol



Propagation Delay Parameter

tup t0	tup KCL	tdn t0	tdn KCL	tdn KCL2	tdn CDR2	Path
0.561 1.570 (4.63)	0.014 0.036	0.970 4.720 (11.61)	0.017 0.081			X to IN OT to X

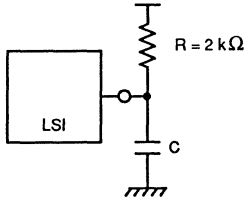
L to Z t0	L to Z KCL	Z to L t0	Z to L KCL	Path
2.100 (18.10)	*	4.600 (11.49)	0.081	C to X

H to Z t0	H to Z KCL	Z to H t0	Z to H KCL
1.900 (18.10)	*	1.600 (11.49)	0.036

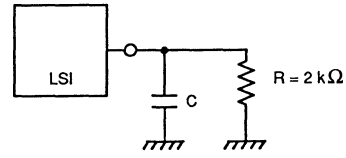
Pin Name	Input Loading Factor (lu)
OT	2
C	2

Pin Name	Output Driving Factor (lu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

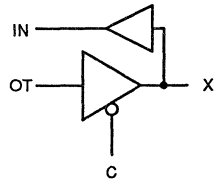
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8TU	Tri–state Output with Noise Limit Resistance & Input Buffer (True) with Pull–up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 1.570 (4.63)	0.014 0.036	0.970 4.720 (11.61)	0.017 0.081			X to IN OT to X

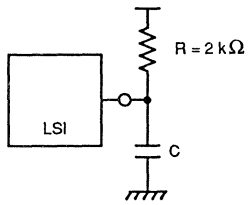
L to Z		Z to L		Path
t0	KCL	t0	KCL	
2.100 (18.10)	*	4.600 (11.49)	0.081	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
1.900 (18.10)	*	1.600 (11.49)	0.036

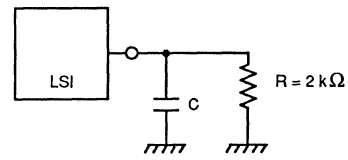
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

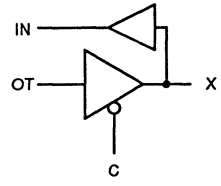
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8TD	Tri–state Output with Noise Limit Resistance & Input Buffer (True) with Pull–down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 1.570 (4.63)	0.014 0.036	0.970 4.720 (11.61)	0.017 0.081			X to IN OT to X

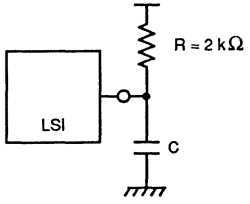
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (18.10)	*	4.600 (11.49)	0.081	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
1.900 (18.10)	*	1.600 (11.49)	0.036	

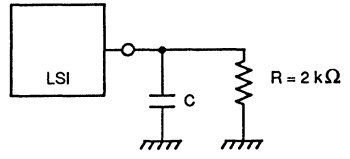
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

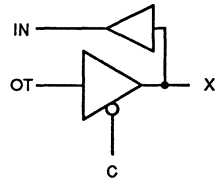
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8TF	Tri–state Output with Noise Limit Resistance & Input Buffer (IOL=8mA, True)	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 1.730 (4.79)	0.014 0.036	0.970 5.950 (10.03)	0.017 0.048			X to IN OT to X

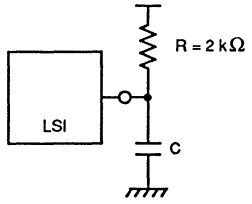
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.100 (20.90)	*	5.650 (9.99)	0.051	

H to Z		Z to H	
t0	KCL	t0	KCL
2.650 (20.90)	*	1.600 (9.99)	0.036

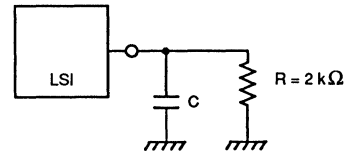
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

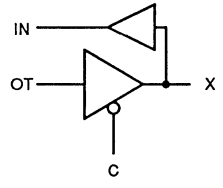
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8TFU	Tri–state Output with Noise Limit Resistance & Input Buffer (IOL=8mA, True) with Pull–up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 1.730 (4.79)	0.014 0.036	0.970 5.950 (10.03)	0.017 0.048			X to IN OT to X

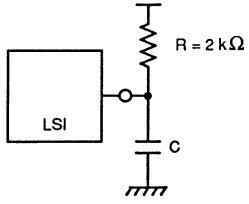
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (20.90)	*	5.650 (9.99)	0.051	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.650 (20.90)	*	1.600 (9.99)	0.036	

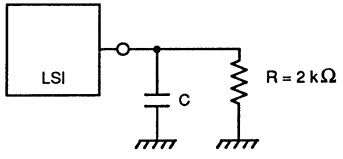
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

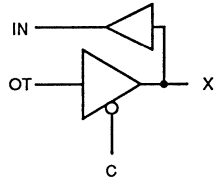
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
H8TFD	Tri-state Output with Noise Limit Resistance & Input Buffer (IOL=8mA, True) with Pull-down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 1.730 (4.79)	0.014 0.036	0.970 5.950 (10.03)	0.017 0.048			X to IN OT to X

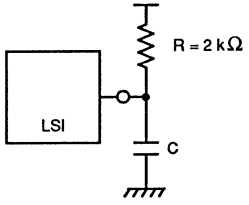
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (20.90)	*	5.650 (9.99)	0.051	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
2.650 (20.90)	*	1.600 (9.99)	0.036

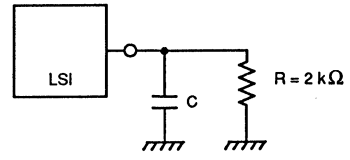
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

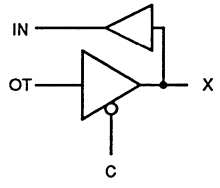
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8W	Power Tri–state Output with Noise Limit Resistance & Input Buffer (True)	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 2.170 (4.21)	0.014 0.024	0.970 6.900 (10.30)	0.017 0.040			X to IN OT to X

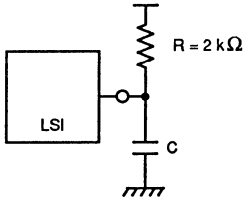
L to Z		Z to L		
t0	KCL	t0	KCL	
2.500 (20.90)	*	6.750 (10.24)	0.041	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
3.500 (20.90)	*	1.800 (10.24)	0.025

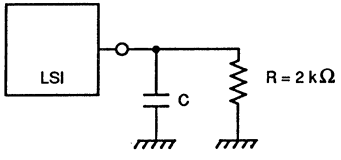
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

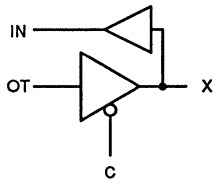
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

FUJITSU CMOS GATE ARRAY UNIT CELL SPECIFICATION		" *CG21K* " Version
Cell Name	**Function**	**Number of BC**
H8WU	Power Tri–state Output with Noise Limit Resistance & Input Buffer (True) with Pull–up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 2.170 (4.21)	0.014 0.024	0.970 6.900 (10.30)	0.017 0.040			X to IN OT to X

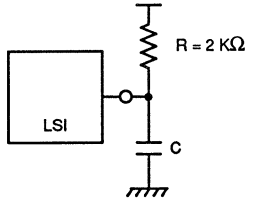
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.500 (20.90)	*	6.750 (10.24)	0.041	

H to Z		Z to H		
t0	KCL	t0	KCL	
3.500 (20.90)	*	1.800 (10.24)	0.025	

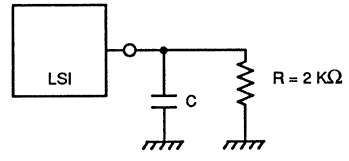
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

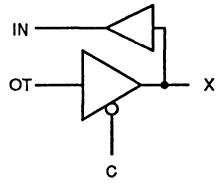
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8WD	Power Tri-state Output with Noise Limit Resistance & Input Buffer (True) with Pull-down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.561 2.170 (4.21)	0.014 0.024	0.970 6.900 (10.30)	0.017 0.040			X to IN OT to X

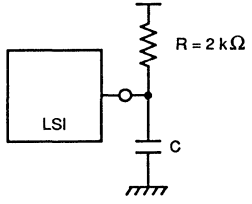
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.500 (20.90)	*	6.750 (10.24)	0.041	

H to Z		Z to H		
t0	KCL	t0	KCL	
3.500 (20.90)	*	1.800 (10.24)	0.025	

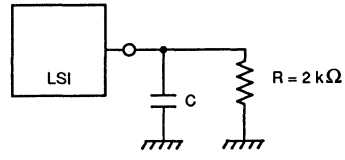
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

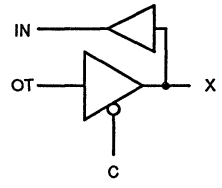
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8C	Tri-state Output Buffer with Noise Limit Resistance & CMOS Interface Input Buffer (True)	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 1.570 (4.63)	0.014 0.036	0.706 4.720 (11.61)	0.017 0.081			X to IN OT to X

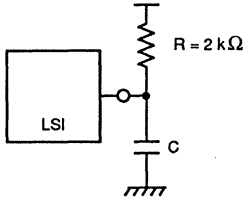
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (18.10)	*	4.600 (11.49)	0.081	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
1.900 (18.10)	*	1.600 (11.49)	0.036

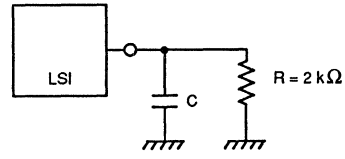
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

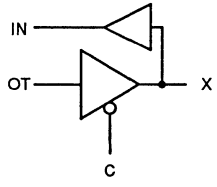
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8CU	Tri–state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull–up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 1.570 (4.63)	0.014 0.036	0.706 4.720 (11.61)	0.017 0.081			X to IN OT to X

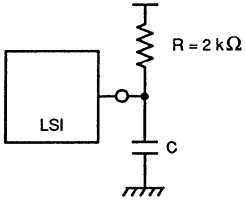
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.100 (18.10)	*	4.600 (11.49)	0.081	

H to Z		Z to H		
t0	KCL	t0	KCL	
1.900 (18.10)	*	1.600 (11.49)	0.036	

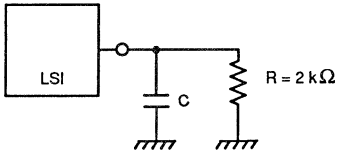
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

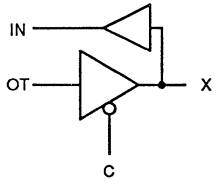
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8CD	Tri–state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull–down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 1.570 (4.63)	0.014 0.036	0.706 4.720 (11.61)	0.017 0.081			X to IN OT to X

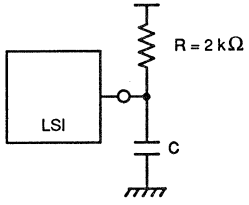
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (18.10)	*	4.600 (11.49)	0.081	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
1.900 (18.10)	*	1.600 (11.49)	0.036	

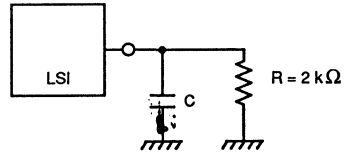
Pin Name	Input Loading Factor (Iu)
OT C	2 2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

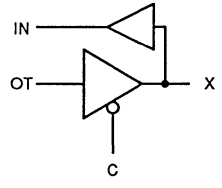


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8CF	Tri–state Output Buffer with Noise Limit Resistance & CMOS Interface Input Buffer (IOL=8mA, True)	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 1.730 (4.79)	0.014 0.036	0.706 5.950 (10.03)	0.017 0.048			X to IN OT to X

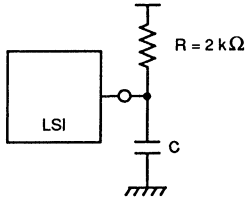
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (20.30)	*	5.650 (9.99)	0.051	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.650 (20.30)	*	1.600 (9.99)	0.036	

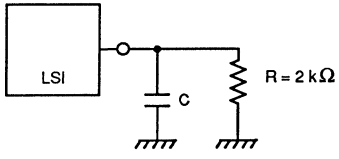
Pin Name	Input Loading Factor (lu)
OT	2
C	2

Pin Name	Output Driving Factor (lu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

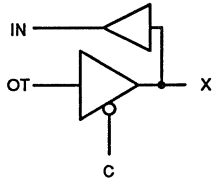
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8CFU	Tri–state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (IOL=8mA, True) w/ Pull–up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 1.730 (4.79)	0.014 0.036	0.706 5.950 (10.03)	0.017 0.048			X to IN OT to X

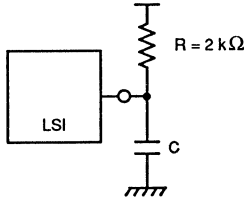
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (20.30)	*	5.650 (9.99)	0.051	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.650 (20.30)	*	1.600 (9.99)	0.036	

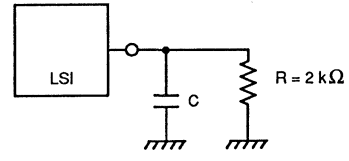
Pin Name	Input Loading Factor (Iu)
OT C	2 2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

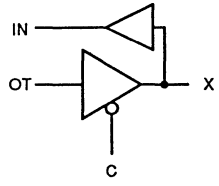
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8CFD	Tri–state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (IOL=8mA, True) w/ Pull–down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 1.730 (4.79)	0.014 0.036	0.706 5.950 (10.03)	0.017 0.048			X to IN OT to X

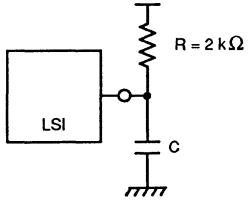
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (20.30)	*	5.650 (9.99)	0.051	C to X

H to Z		Z to H		
t0	KCL	t0	KCL	
2.650 (20.30)	*	1.600 (9.99)	0.036	

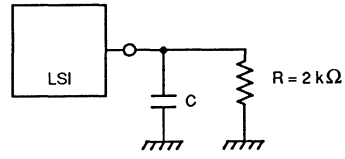
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

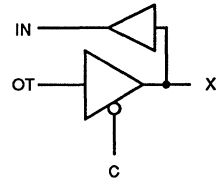
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8E	Power Tri–state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True)	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 2.170 (4.21)	0.014 0.024	0.706 6.900 (10.30)	0.017 0.040			X to IN OT to X

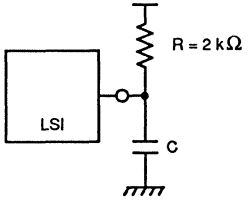
L to Z		Z to L		
t0	KCL	t0	KCL	
2.500 (20.90)	*	6.750 (10.24)	0.041	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
3.500 (20.90)	*	1.800 (10.24)	0.025

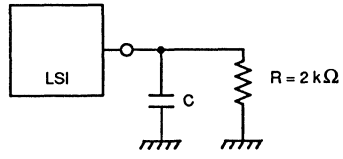
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

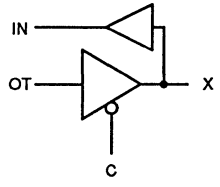


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8EU	Power Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-up Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 2.170 (4.21)	0.014 0.024	0.706 6.900 (10.30)	0.017 0.040			X to IN OT to X

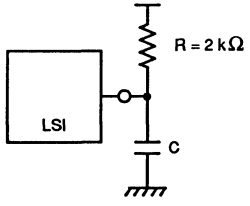
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.500 (20.90)	*	6.750 (10.24)	0.041	

H to Z		Z to H		
t0	KCL	t0	KCL	
3.500 (20.90)	*	1.800 (10.24)	0.025	

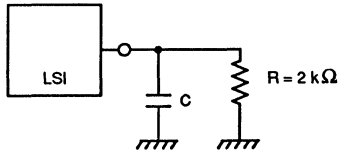
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

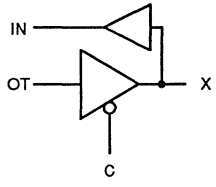
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8ED	Power Tri-state Output Buffer w/ Noise Limit Resistance & CMOS Interface Input Buffer (True) w/ Pull-down Resistance	9

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
0.489 2.170 (4.21)	0.014 0.024	0.706 6.900 (10.30)	0.017 0.040			X to IN OT to X

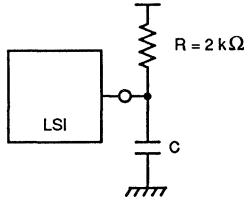
L to Z		Z to L		
t0	KCL	t0	KCL	
2.500 (20.90)	*	6.750 (10.24)	0.041	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
3.500 (20.90)	*	1.800 (10.24)	0.025

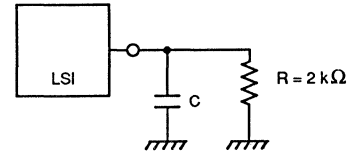
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	36

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

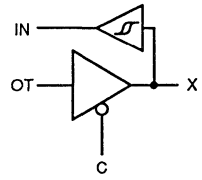
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8S	Tri-state Output & Schmitt Trigger Input Buffer (CMOS Type, True) with Noise Limit Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314 1.570 (4.63)	0.060 0.036	1.630 4.720 (11.61)	0.045 0.081			X to IN OT to X

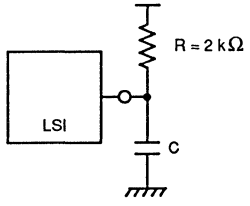
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.100 (18.10)	*	4.600 (11.49)	0.081	

H to Z		Z to H		
t0	KCL	t0	KCL	
1.900 (18.10)	*	1.600 (11.49)	0.036	

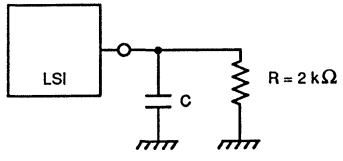
Pin Name	Input Loading Factor (lu)
OT	2
C	2

Pin Name	Output Driving Factor (lu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

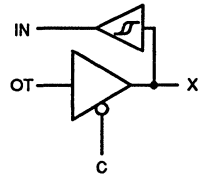
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8SU	Tri-state Output & Schmitt Trigger Input Buffer (CMOS Type , True) w/ Noise Limit Resistance w/ Pull-up Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314 1.570 (4.63)	0.060 0.036	1.630 4.720 (11.61)	0.045 0.081			X to IN OT to X

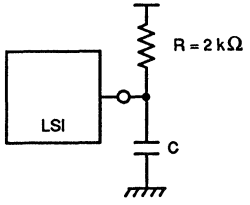
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.100 (18.10)	*	4.600 (11.49)	0.081	

H to Z		Z to H		
t0	KCL	t0	KCL	
1.900 (18.10)	*	1.600 (11.49)	0.036	

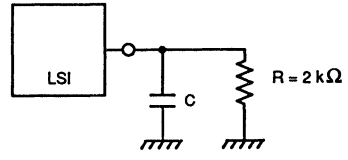
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

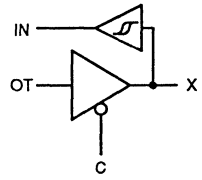


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8SD	Tri–state Output & Schmitt Trigger Input Buffer (CMOS Type , True) w/ Noise Limit Resistance w/ Pull–down Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.314 1.570 (4.63)	0.060 0.036	1.630 4.720 (11.61)	0.045 0.081			X to IN OT to X

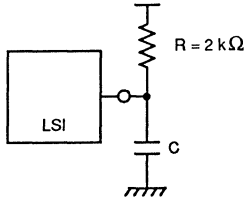
L to Z		Z to L		
t0	KCL	t0	KCL	C to X
2.100 (18.10)	*	4.600 (11.49)	0.081	

H to Z		Z to H		
t0	KCL	t0	KCL	
1.900 (18.10)	*	1.600 (11.49)	0.036	

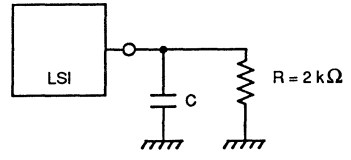
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

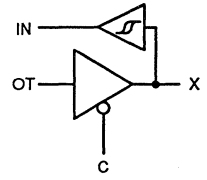
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8R	Tri–state Output & Schmitt Trigger Input Buffer (TTL Type, True) with Noise Limit Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.182 1.570 (4.63)	0.060 0.036	1.967 4.720 (11.61)	0.062 0.081			X to IN OT to X

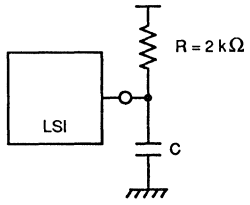
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (18.10)	*	4.600 (11.49)	0.081	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
1.900 (18.10)	*	1.600 (11.49)	0.036

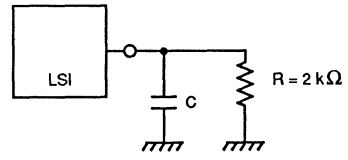
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.

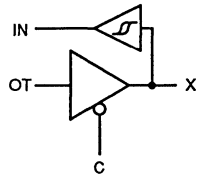


(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.
2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.
3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8RU	Tri–state Output & Schmitt Trigger Input Buffer (TTL Type, True) w/ Noise Limit Resistance w/ Pull–up Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.182 1.570 (4.63)	0.060 0.036	1.967 4.720 (11.61)	0.062 0.081			X to IN OT to X

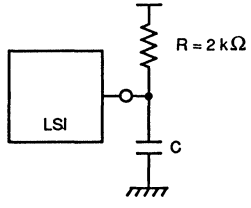
L to Z		Z to L		Path
t0	KCL	t0	KCL	
2.100 (18.10)	*	4.600 (11.49)	0.081	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
1.900 (18.10)	*	1.600 (11.49)	0.036

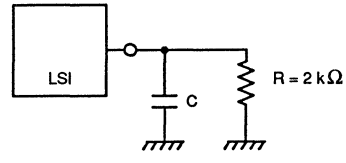
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

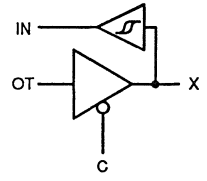
Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Cell Name	Function	Number of BC
H8RD	Tri–state Output & Schmitt Trigger Input Buffer (TTL Type, True) w/ Noise Limit Resistance w/ Pull–down Resistance	13

Cell Symbol



Propagation Delay Parameter

tup		tdn				Path
t0	KCL	t0	KCL	KCL2	CDR2	
1.182 1.570 (4.63)	0.060 0.036	1.967 4.720 (11.61)	0.062 0.081			X to IN OT to X

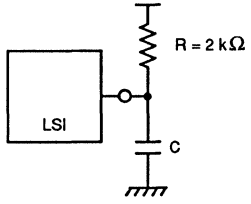
L to Z		Z to L		
t0	KCL	t0	KCL	
2.100 (18.10)	*	4.600 (11.49)	0.081	C to X

H to Z		Z to H	
t0	KCL	t0	KCL
1.900 (18.10)	*	1.600 (11.49)	0.036

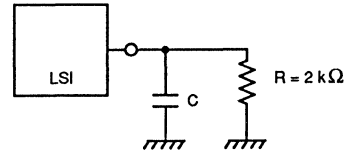
Pin Name	Input Loading Factor (Iu)
OT	2
C	2

Pin Name	Output Driving Factor (Iu)
IN	18

* These values are subject to external loading condition.
Measurement circuits of propagation delay time at LZ, ZL, HZ and ZH are as follows:



(a) Measurement of tpd at LZ and ZL.



(b) Measurement of tpd at HZ and ZH.

Note: 1. The unit of KCL for paths OT, C to X is ns/pF.

2. Output load capacitance of 85 pF is used for Fujitsu's logic simulation.

3. The parameters in parentheses are the values applied to the simulation.

Appendix A: General AC Specifications

Simulation Delay Specifications
(Recommended Operating Conditions, Ta = 0 to 70°C, V_{DD} = 5 V±5%

Delay Multipliers	Min.	Max.
Pre-layout Simulation	0.35	t_{maxB}
Post-layout Simulation	0.40	t_{maxA}

Junction Temperature (Tj)	tmaxB	tmaxA
Tj ≤ 60°C	1.65	1.55
60°C<Tj ≤ 70°C	1.70	1.60
70°C<Tj ≤ 80°C	1.75	1.65
80°C<Tj ≤ 90°C	1.80	1.70
90°C<Tj ≤ 105°C	1.85	1.75
105°C<Tj ≤ 120°C	1.90	1.80
120°C<Tj ≤ 130°C[1]	1.95	1.85
130°C<Tj ≤ 140°C[2]	2.00	1.90
140°C<Tj ≤ 150°C[2]	2.05	1.95

NOTES: 1. This condition cannot be applied to devices in some plastic packages. If this condition is required for devices in plastic, please consult Fujitsu.

2. This condition cannot be applied to devices in plastic packages. If this condition is required even for ceramic packages, please consult Fujitsu.

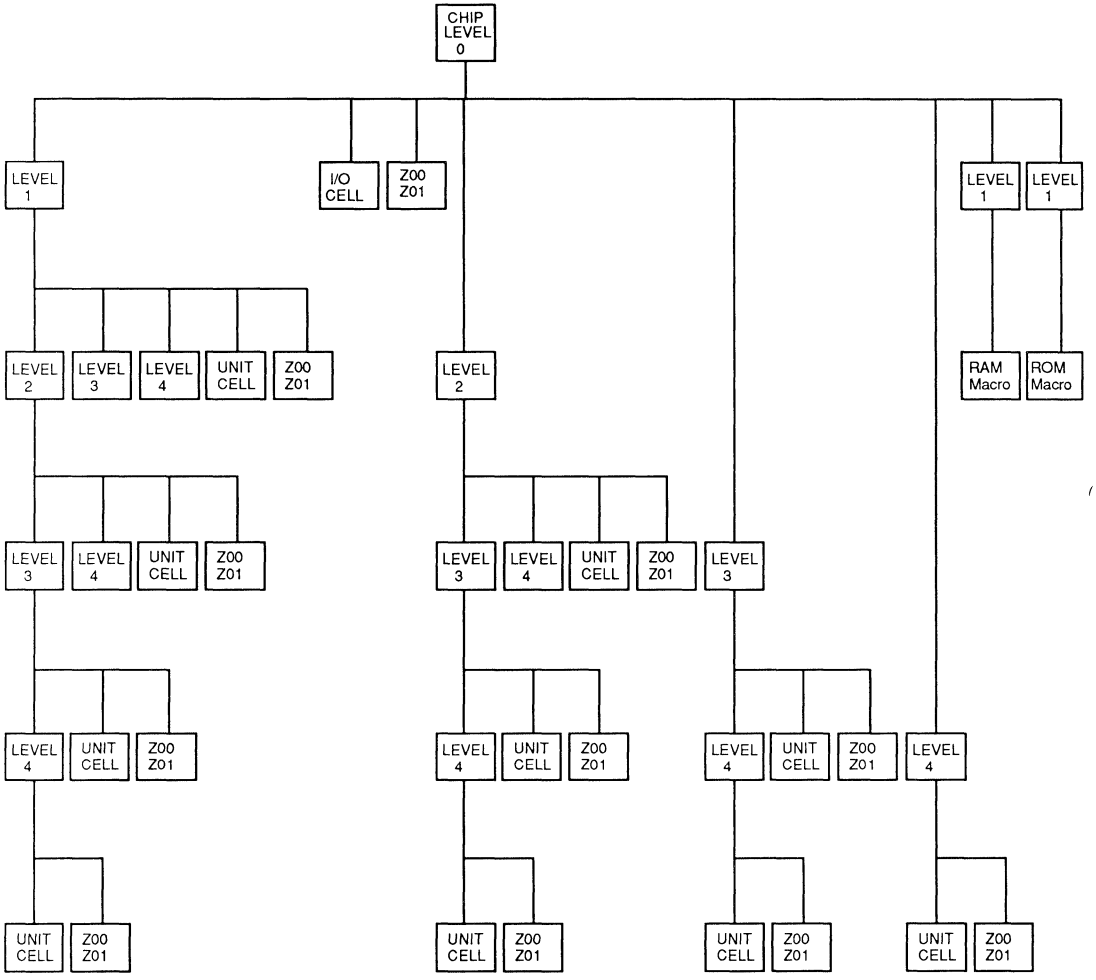
Tj is determined by the following formula:

$$Tj = T_{aMAX} + \theta ja \times Pd\ (°C)$$

where

TaMAX: Maximum Ambient Termperature (°C)
θja: Thermal Resistance (°C/W). This value is determined for each package.
Pd: Power dissipation (W). Please refer to Chapter 5 of Section 1 of this Data Book or the CG21 Design Manual for details.

Appendix B: Hierarchical Structure



Appendix C: Estimation Tables for Metal Loading

CG21303 (30K-gate-device) (Main Block)

NDI	C_L(lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	12.3	9.7	6.8	4.3	2.1
2	18.5	14.4	10.3	6.6	3.2
3	24.8	19.3	13.8	8.8	4.3
4	29.0	22.7	16.1	10.3	5.1
5	32.1	25.2	17.8	11.4	5.7
6	34.6	27.1	19.2	12.3	6.1
7	37.9	29.6	21.1	13.5	6.7
8	39.4	30.9	21.8	14.0	6.9
9	40.4	31.6	22.4	14.4	7.1
10	41.4	32.5	23.0	14.7	7.3
11	41.4	32.5	23.0	14.7	7.3
12	42.0	32.8	23.3	14.9	7.4
13	42.6	33.3	23.7	15.1	7.6
14	43.6	34.2	24.3	15.5	7.7
15	43.6	34.2	24.3	15.5	7.7
16 – 30	47.2	37.0	26.3	16.7	8.3
31 – 50	54.0	42.4	30.0	19.2	9.5
51 – 75	55.6	43.5	30.9	19.7	9.8
76 –100	61.1	47.8	33.8	21.7	10.8

CG21303 (30K-gate-device) (Sub Block)

NDI	C_L(lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	5.8	4.1	2.7	1.2
2	10.7	7.6	4.8	2.4
3	15.6	11.0	7.1	3.5
4	18.8	13.4	8.7	4.2
5	21.3	15.1	9.7	4.7
6	23.8	16.5	10.7	5.2
7	25.2	18.3	11.8	5.8
8	27.0	19.2	12.3	6.1
9	27.9	19.7	12.6	6.2
10	28.6	20.3	13.0	6.4
11	28.6	20.3	13.0	6.4
12	29.0	20.6	13.3	6.4
13	29.6	20.9	13.5	6.6
14	30.4	21.6	13.9	6.8
15	30.4	21.6	13.9	6.8
16 – 30	33.2	23.5	15.1	7.4
31 – 50	38.5	27.4	17.5	8.7
51 – 75	39.8	28.1	18.1	8.9
76 – 100	44.00	31.2	19.9	9.9

Appendix C: Estimation Tables for Metal Loading (Continued)

CG21403 (40K-gate-device) (Main Block)

NDI	C_L(lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	14.0	9.7	6.8	4.3	2.1
2	21.1	14.4	10.3	6.6	3.2
3	28.2	19.3	13.8	8.8	4.3
4	33.1	22.7	16.1	10.3	5.1
5	36.7	25.2	17.8	11.4	5.7
6	39.5	27.1	19.2	12.3	6.1
7	43.2	29.6	21.1	13.5	6.7
8	45.0	30.9	21.8	14.0	6.9
9	46.2	31.6	22.4	14.4	7.1
10	47.3	32.5	23.0	14.7	7.3
11	47.3	32.5	23.0	14.7	7.3
12	47.9	32.8	23.3	14.9	7.4
13	48.7	33.3	23.7	15.1	7.6
14	49.9	34.2	24.3	15.5	7.7
15	49.9	34.2	24.3	15.5	7.7
16 – 30	54.0	37.0	26.3	16.7	8.3
31 – 50	61.8	42.4	30.0	19.2	9.5
51 – 75	63.6	43.5	30.9	19.7	9.8
76 – 100	69.8	47.8	33.8	21.7	10.8

CG21403 (40K-gate-device) (Sub Block)

NDI	C_L(lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	5.8	4.1	2.7	1.2
2	10.7	7.6	4.8	2.4
3	15.6	11.0	7.1	3.5
4	18.8	13.4	8.7	4.2
5	21.3	15.1	9.7	4.7
6	23.3	16.5	10.7	5.2
7	25.5	18.3	11.8	5.8
8	27.0	19.2	12.3	6.1
9	27.9	19.7	12.6	6.2
10	28.6	20.3	13.0	6.4
11	28.6	20.3	13.0	6.4
12	29.0	20.6	13.3	6.4
13	29.6	20.9	13.5	6.6
14	30.4	21.6	13.9	6.8
15	30.4	21.6	13.9	6.8
16 – 30	33.2	23.5	15.1	7.4
31 – 50	38.5	27.4	17.5	8.7
51 – 75	39.8	28.1	18.1	8.9
76 – 100	44.0	31.2	19.9	9.9

Appendix C: Estimation Tables for Metal Loading (Continued)

CG21503 (50K-gate-device) (Main Block)

NDI	C_L(lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	15.7	9.7	6.8	4.3	2.1
2	23.7	14.4	10.3	6.6	3.2
3	31.8	19.3	13.8	8.8	4.3
4	37.3	22.7	16.1	10.3	5.1
5	41.3	25.2	17.8	11.4	5.7
6	44.5	27.1	19.2	12.3	6.1
7	48.7	29.6	21.1	13.5	6.7
8	50.7	30.9	21.8	14.0	6.9
9	51.9	31.6	22.4	14.4	7.1
10	53.3	32.5	23.0	14.7	7.3
11	53.3	32.5	23.0	14.7	7.3
12	53.9	32.8	23.3	14.9	7.4
13	54.8	33.3	23.7	15.1	7.6
14	56.1	34.2	24.3	15.5	7.7
15	56.1	34.2	24.3	15.5	7.7
16 – 30	60.7	37.0	26.3	16.7	8.3
31 – 50	69.5	42.4	30.0	19.2	9.5
51 – 75	71.5	43.5	30.9	19.7	9.8
76 – 100	78.4	47.8	33.8	21.7	10.8

CG21503 (50K-gate-device) (Sub Block)

NDI	C_L(lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	5.8	4.1	2.7	1.2
2	10.7	7.6	4.8	2.4
3	15.6	11.0	7.1	3.5
4	18.8	13.4	8.7	4.2
5	21.3	15.1	9.7	4.7
6	23.3	16.5	10.7	5.2
7	25.5	18.3	11.8	5.8
8	27.0	19.2	12.3	6.1
9	27.9	19.7	12.6	6.2
10	28.6	20.3	13.0	6.4
11	28.6	20.3	13.0	6.4
12	29.0	20.6	13.3	6.4
13	29.6	20.9	13.5	6.6
14	30.4	21.6	13.9	6.8
15	30.4	21.6	13.9	6.8
16 – 30	33.2	23.5	15.1	7.4
31 – 50	38.5	27.4	17.5	8.7
51 – 75	39.8	28.1	18.1	8.9
76 – 100	44.0	31.2	19.9	9.9

Appendix C: Estimation Tables for Metal Loading (Continued)

CG21753 (75-gate-device) (Main Block)

NDI	C_L(lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	18.8	9.7	6.8	4.3	2.1
2	28.2	14.4	10.3	6.6	3.2
3	37.9	19.3	13.8	8.8	4.3
4	44.5	22.7	16.1	10.3	5.1
5	49.2	25.2	17.8	11.4	5.7
6	53.2	27.1	19.2	12.3	6.1
7	58.1	29.6	21.1	13.5	6.7
8	60.5	30.9	21.8	14.0	6.9
9	62.1	31.6	22.4	14.4	7.1
10	63.7	32.5	23.0	14.7	7.3
11	63.7	32.5	23.0	14.7	7.3
12	64.4	32.8	23.3	14.9	7.4
13	65.4	33.3	23.7	15.1	7.6
14	67.0	34.2	24.3	15.5	7.7
15	67.0	34.2	24.3	15.5	7.7
16 – 30	72.6	37.0	26.3	16.7	8.3
31 – 50	83.0	42.4	30.0	19.2	9.5
51 – 75	85.4	43.5	30.9	19.7	9.8
76 – 100	93.8	47.8	33.8	21.7	10.8

CG21753 (75-gate-device) (Sub Block)

NDI	C_L(lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	5.8	4.1	2.7	1.2
2	10.7	7.6	4.8	2.4
3	15.6	11.0	7.1	3.5
4	18.8	13.4	8.7	4.2
5	21.3	15.1	9.7	4.7
6	23.3	16.5	10.7	5.2
7	25.5	18.3	11.8	5.8
8	27.0	19.2	12.3	6.1
9	27.9	19.7	12.6	6.2
10	28.6	20.3	13.0	6.4
11	28.6	20.3	13.0	6.4
12	29.0	20.6	13.3	6.4
13	29.6	20.9	13.5	6.6
14	30.4	21.6	13.9	6.8
15	30.4	21.6	13.9	6.8
16 – 30	33.2	23.5	15.1	7.4
31 – 50	38.5	27.4	17.5	8.7
51 – 75	39.8	28.1	18.1	8.9
76 – 100	44.0	31.2	19.9	9.9

Appendix C: Estimation Tables for Metal Loading (Continued)

CG21104 (100K- gate-device) (Main Block)

NDI	C_L(lu)				
	CHIP	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	21.9	9.7	6.8	4.3	2.1
2	32.8	14.4	10.3	6.6	3.2
3	44.1	19.3	13.8	8.8	4.3
4	51.8	22.7	16.1	10.3	5.1
5	57.2	25.2	17.8	11.4	5.7
6	61.8	27.1	19.1	12.3	6.1
7	67.6	29.6	21.1	13.5	6.7
8	70.4	30.9	21.8	14.0	6.9
9	72.1	31.6	22.4	14.4	7.1
10	74.0	32.5	23.0	14.7	7.3
11	74.0	32.5	23.0	14.7	7.3
12	75.0	32.8	23.3	14.9	7.4
13	76.1	33.3	23.7	15.1	7.6
14	77.9	34.2	24.3	15.5	7.7
15	77.9	34.2	24.3	15.5	7.7
16 – 30	84.4	37.0	26.3	16.7	8.3
31 – 50	96.5	42.4	30.0	19.2	9.5
51 – 75	99.2	43.5	30.9	19.7	9.8
76 – 100	109.0	47.8	33.8	21.7	10.8

CG21104 (100K- gate-device) (Sub Block)

NDI	C_L(lu)			
	LEVEL 1	LEVEL 2	LEVEL 3	LEVEL 4
1	5.8	4.1	2.7	1.2
2	10.7	7.6	4.8	2.4
3	15.6	11.0	7.1	3.5
4	18.8	13.4	8.7	4.2
5	21.3	15.1	9.7	4.7
6	23.3	16.5	10.7	5.2
7	25.5	18.3	11.8	5.8
8	27.0	19.2	12.3	6.1
9	27.9	19.7	12.6	6.2
10	28.6	20.3	13.0	6.4
11	28.6	20.3	13.0	6.4
12	29.0	20.6	13.3	6.4
13	29.6	20.9	13.5	6.6
14	30.4	21.6	13.9	6.8
15	30.4	21.6	13.9	6.8
16 – 30	33.2	23.5	15.1	7.4
31 – 50	38.5	27.4	17.5	8.7
51 – 75	39.8	28.1	18.1	8.9
76 – 100	44.00	31.2	19.9	9.9

Appendix D: Available Package Types

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
SDIP–64	Plastic	None	70 mil Lead Pitch	None	CG21103* CG21153* CG21203*	80 80 85	50 55 60
PLCC–68	Plastic	None	70 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	50 55 60	35 40 40
PLCC–84	Plastic	None	30 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	50 50 55	35 35 40
QFP–64	Plastic	None	100 mil Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP–80	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP–100	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	CG21103* CG21153* CG21203*	80 85 90	55 60 65
QFP–120	Plastic	None	0.8 mm Lead Pitch Gull-wing	None	CG21303 CG21403 CG21503 CG21103* CG21153* CG21203*	65 70	40 50
QFP–160	Plastic	None	0.65 mm Lead Pitch Gull-wing	None	CG21303 CG21403 CG21503 CG21153 CG21253	59 70	39 50
QFP–196**	Plastic	None	TBD Gull-wing	None	CG21503 CG21753 CG21104	TBD	TBD
QFP–232**	Plastic	None	TBD Gull-wing	None	CG21753 CG21104	TBD	TBD
QFP–176**	Plastic	None	TBD Gull-wing	None	CG21403 CG21503 CG21753	TBD	TBD
QFP–208**	Plastic	None	TBD Gull-wing	None	CG21403 CG21503 CG21753 CG21104	TBD	TBD
QFP–256**	Plastic	None	TBD Gull–wing	None	CG21104	TBD	TBD

Continued on next page

* planned device
**package under development

Appendix D: Available Package Types (Continued)

Package	Material	Cavity	Pin Arrangement	Pads for Decoupling Capacitor	Device	θJA (TYP) at 0m/s	(C°/W) at 3 m/s
PGA–64	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21103* CG21153* CG21203*	40	20
PGA–88	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21103* CG21153* CG21203* CG21303	40	20
PGA–135	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	All CG21	30	15
PGA–179	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21203* CG21303 CG21403 CG21503 CG21753 CG21104	30 25	15 13
PGA–208	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21303 CG21403 CG21503 CG21753 CG21104	23	12
PGA–256	Ceramic	Up	100 mil Pin Pitch Through hole	Yes	CG21403 CG21503 CG21753 CG21104	19	9
PGA–299	Ceramic	Down	100 mil Pin Pitch Through hole	Yes	CG21503 CG21753 CG21104	19	9
PGA–321	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21753 CG21104	22-24	11-13
PGA–361	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21753 CG21104	22-24	11-13
PGA–401	Ceramic	Down	70 mil Stagger Through hole	Yes	CG21104	22-24	11-13

Appendix E: TTL 7400 Function Conversion Table

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7400	Quad 2-input NAND	4 x N2N	4
7401	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7402	Quad 2-input NOR	4 x R2N	4
7403	Quad 2-input NAND, Open Collector Outputs	T24 multiplexer	6
7404	Hex Inverter	6 x VIN	6
7405	Hex Inverter, Open Collector Outputs	R6B	5
7406	Hex Inverter/Buffer, Open Collector Outputs	R6B	5
7407	Hex Buffer, Open Collector Outputs	2 x N3N into R2N	5
7408	Quad 2-input AND	4 x N2P	8
7409	Quad 2-input AND, Open Collector Outputs	N8P	6
7410	Triple 3-input NAND	3 x N3N	6
7411	Triple 3-input AND	3 x N3P	9
7412	Triple 3-NAND, Open Collector Outputs	T33	7
7413	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7414	Hex Schmitt Trigger Inverter	6 x I1R	48
7415	Triple 3-input AND, Open Collector Outputs	N8P to N2P	8
7418	Dual 4-input NAND, Schmitt Trigger	2 x (4 x I2R to N4N)	68
7419	Hex Schmitt Trigger Inverter	6 x I1R	48
7420	Dual 4-input NAND	2 x N4N	4
7421	Dual 4-input AND	2 x N4P	6
7422	Dual 4-input NAND, Open Collector Outputs	2 x N4N + N2P	6
7423	Expanded Dual 4-input NOR with Strobe	R4P to D23 + R4P to R2N	9
7424	Quad Schmitt Trigger 2-input NAND	8 x I2R + 4 x N2N	68
7425	Dual 4-input NOR with Strobe	2 x (R4P + R2N)	8
7426	Quad 2-input NAND, High Voltage Output	4 x N2N	4
7427	Triple 3-input NOR	3 x R3N	6
7428	Quad 2-input NOR Buffer	4 x R2N	4
7430	8-input NAND	N8B	6
7432	Quad 2-input OR	4 x R2P	8
7433	Quad 2-input NOR Buffer, Open Collector Outputs	4 x R2N + N4P	7
7434	Hex Noninverter	6 x B1N	6
7435	Hex Noninverter with Open Collector Outputs	2 x N3N into R2N	5
7437	Quad 2-input NAND Buffer	4 x N2B	12
7438/9	Quad 2-input NAND Buffer, Open Collector Outputs	4 x N2N + N4P	7
7440	Dual 4-input NAND Buffer	2 x N4B (N4N if not power)	8(4)
7442	BCD to Decimal Decoder	4 x V2B + 10 x N4N	24
7443	EX3 to Decimal Decoder	4 x V2B + 10 x N4N	24
7444	4 to 10 Line Decoder	4 x V2B + 10 x N4N	24
7445	BCD to Decimal Decoder/driver (30V)	4 x V2B + 10 x N4N	24
7446	BCD to 7–segment Decoder/Driver (30V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7447	BCD to 7–segment Decoder/Driver (15V)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7448	BCD to 7–segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7449	BCD to 7–segment, Open Collector Outputs	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
7450	Dual 2-input, 2-wide AOI (One Expandable)	D36 + D24	5
7451	AOI	2 x D24	4
7452	Expandable 4–wide AND–OR	N3N + D36 + V1N into N3N	8
7453	Expandable 4–wide AOI	D36 + D23 into N2P	7
7454	4–wide AOI	2 x N3N + 2 x N2N + N4N + V1N	9
7455	2–wide 4–input AOI	T42	6
7460	Dual 4–input Expander	2 x N4P	6
7461	Triple 3–input Expander	3 x N3P	6
7462	4–wide AND–OR Expander	2 x N3N + 2 x N2N + N4N	8
7464	4–2–3–2 AOI	T54	10
7465	4–2–3–2 AOI (Open Collector)	T54	10

Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
7470	AND–gated positive-edge JK FF with Preset and Clear	3 x V1N + 2 x N3N + N2N + R2N + FJD	21
	or:	FD4 + 2 x N2N + R2N + V1N + R2P + D24	17
7471	AND–gated RS M/S FF with Preset and Clear	FD4 + 2 x N3N + 2 x D23 + 2 x V1N	19
	or:	LT1+ 2 x N4N + N2P	10
7472	AND–gated JK M/S FF with Preset and Clear	V1N + 2 x N3N + N2N + R2N + FJD	19
	or:	FD4 + N3P + N3N + V1N + D24	17
7473	Dual JK FF with Clear	2 x FJD	24
7474	Dual positive-edge D–FF with Preset and Clear	2 x FDP	16
7475	4–bit Bistable Latch	LTM	16
7476	Dual JK FF with Preset and Clear	2 x (FJD + N2N + R2N + V1N)	30
7477	4–bit Bistable Latch	LTM	16
7478	Dual JK FF with Preset and Common Clear and Clock	2 x (FJD + N2N + R2N + V1N)	30
7480	Gated Full Adder	A1N	8
7482	2–bit Binary Full Adder	A2N	16
7483	4–bit Binary Full Adder with Fast Carry	A4H	48
7484	4–bit Magnitude Comparator	MC4	42
7486	Quad 2-input XOR	4 x X2N	12
7487	4–bit True/Complement Zero/One Element	4 x N2N + V1N + 4 x N2N	17
7489	64–bit (16 x 4) Memory	2 x DE6 + V1N + 16 x LT4 + 5 x (V2B + T5A) + 10 x V2B	298
7490	Decade Counter (Different Implementation)	2 x (FDP + FDO + N2P + N2N + R2N) + V1N	39
		4 x N2P + 2 x R2P + N2N + C41 + LT1	41
7491	8–bit Shift Register	2 x FDS + V1N	41
7492	Divide–by–12 Counter	4 x FDO + 2 x V1N + 2 x R2N + N2N	33
7493	4–bit Binary Counter	C41 + N2N (for the resets)	25
7494	4–bit Shift Register, 2 asynchronous Presets	FS3	34
	4–bit Shift Register, 2 asynchronous Presets, Full Implementation	4 x FDP + 4 x D24 + 2 x V1N	42
7495	4–bit Parallel-access Shift Register	FS2 + D24 + 2 x V1N	34
7496	5–bit Shift Register	5 x FDP + 5 x N2N + V1N(clock)	46
7497	Synch 6–bit Binary Rate Multiplier	FDR + 2 x FDO + 3 x V1N + 2 x N2N + 2 x N3N + 2 x N4N + 5 x N6B + 3 x N8B + R2B + X2N + 5 x X1B.	122
7498	4–bit Data Selector/Storage Register	FDQ + T2F + 4 x V1N	33
7499	4–bit Universal Shift Register	FS2 + LTK + 2 x D24 + 4 x V1N	42
74100	8–bit Bistable Latch	2 x YL4 + 2 x V1N	30
74101	AO-gated JK Negative-Edge FF, with Preset	FD3 + V1N + 3 x D24	15
74102	AND-gated JK Negative-Edge FF with Preset and Clear	FD4 + D24 + N3P + N3N	16
74103	Dual JK FF with Clear	2 x FJD + 2 x V1N (for clock)	26
	or:	2 x (FD5 + D24 + V1N)	22
74106	Dual JK Negative-Edge FF with Preset and Clear	2 x (FD4 + D24 + V1N)	24
74107	Dual JK FF with Clear	2 x (FJD + 2 x V1N)	22
74108	Dual JK Negative-Edge FF with Preset and Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74109	Dual JK Positive-Edge FF with Preset and Clear	2 x (FDP + V1N + D24)	22
74110	AND-gated JK M/S FF with Data Lockout	FDP + D24 + N3P + N3N	15
74111	Dual JK M/S FF with Data Lockout	2 x (FDP + D24 + V1N)	22
74112	Dual JK Negative-Edge FF with Preset and Clear	2 x (FD4 + D24 + V1N)	24

Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74113	Dual JK Negative-Edge FF with Preset	2 x (FD3 + D24 + V1N)	22
74114	Dual JK Negative-Edge FF with Preset and Common Clear and Clock	2 x (FD4 + D24 + V1N)	24
74116	Dual 4–bit Latch with Clear	2 x LTM	32
74120	Dual Pulse Synchronizer/Driver	2 x (N2P + LT1 + 4 x N3N + 2 x N2N + 2 x V1N)	36
74125	Quad Bus Buffer with 3–state Output	B41	9
74126	Quad Bus Buffer with 3–state Output	B41 + 4 x V1N	13
74132	Quad 2–input NAND Schmitt Trigger	4 x (2 x I2R + N2N)	68
74133	13–input NAND	2 x N4N + N3N + N2N into R4P	10
74134	12–input NAND with 3–state Outputs	NCB + O4R	15
74135	Quad 3–input EXOR/EXNOR	4 x X4N	20
74136	Quad 2–input EXOR with Open-Collector Outputs	4 x X2N + R4N	14
74137	3-line to 8–line Decoder with Address Latch	3 x LTK into DE6	42
74138	3-line to 8–line Decoder with Enable	DE6	30
74139	Dual 2-line to 4–line Decoder	2 x DE4	16
74141	BCD–to–Decimal Decoder	4 x V2B + 10 x N4N	24
74145	BCD–to–decimal Decoder	4 x V1N + 10 x N4N	24
74147	10–line to 4–line BCD Priority Encoder	3 x N4N + 3 x N3N + 2 x N2N + 2 x N2P + 3 x R2N + R4N + 13 x V1N	36
74148	8–line to 3–line Octal Priority Encoder	N9B + 2 x N2N + R2P + R4N + 4 x N3N + 2 x N4N + G44 + 12 x V1N	40
74150	1–to–16 Multiplexer	DE3 + 2 x U28 + D24 + 2 x V1N	41
74151	1–to–8 Multiplexer with Strobe	DE3 + U28 + N2N + V1N	28
74152	1–to–8 Multiplexers	DE3 + U28	26
74153	Dual 4–line to 1–line Selector/Multiplexer	DE2 + 2 x U24 + 2 x R2N	19
74154	4–line to 16–line Decoder/Demultiplexer or:	2 x DE6 + V1N 2 x DE4 + N2P + 16 x R2P	61 50
74155	Dual 2-line to 4-line Decoder/Demultiplexer (Totem Pole)	8 x N3N + 2 x R2N + 5 x V1N	23
74156	Dual 2-line to 4-line Decoder/Demultiplexer (Open Collector)	8 x N3N + 2 x R2N + 5 x V1N	23
74157	Quad 2-line to 1–line multiplexer	T2F + 4 x R2N + B1N	13
74158	Quad 2-line to 1–line multiplexer (Inverter Data Outputs)	4 x D24 + V1N + 2 x R2N	11
74159	4–line to 16–line Demultiplexer	2 x DE6 + V1N (without open collector)	50
74160	Synchronous 4–bit Counter (Decimal with Direct Clear)	4 x C11 + K1B + 2 x V2B + V1N + B1N+ N2K + 2 x R3N + R4N + 3 x R2N + N2N	62
74161	Synchronous 4–bit Counter (Binary with Direct Clear)	C43	48
74162	Synchronous 4–bit Counter (Decimal with Synchronous Clear)	C45 + D36 + N3P + 2 x R2N + B1N	57
74163	Synchronous 4–bit Counter (Binary with Synchronous Clear)	C45	48
74164	8–bit Parallel Output Serial Shift Register, Asynchronous Clear	2 x FDR + N2P	54
74165	8–bit Shift Register	2 x FDS + 8 x D24 + 11 x V1N + K4B + R2P	71
74166	8–bit Shift Register	2 x FDR + 8 x D24 + 10 x V1N + K4B	80
74168	4–bit Up/Down Synchronous Counter (Decade)	4 x C11 + 4 x T32 + 7 x N2N + 2 x N3N + R2N + 7 x V2B + K1B	85
74169	4–bit Up/Down Synchronous Counter (Binary)	C47	68
74170	4–by–4 Register File	4 x (YL4 + B1N + V1N + U24) + 2 x DE4	104
74171	Quad D–FF with Clear	FDR + 4 x V1N	30
74172	16–bit (8 x 2) Register File	3 x DE6 + 4 x FDS + 16 x (N2N + G34 + + V1N + 2 x R2P + 4 x U28) + 2 x V1N + 2 x R2P	348

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Appendix E: TTL 7400 Function Conversion Table (Continued)

TTL 7400 Series Name	Function	Fujitsu Basic Cells	Number of Unit Cells
74173	4–bit D–type Register (3–state Output)	FDR + 2 x R2N + B41 + 6 x V1N + K1B + 4 x D24	53
74174	Hex D–FF (Single Output)	FDR + 2 x FDO	40
74175	Quad D–FF (with Clear)	FDR + 4 x V1N	30
74176	Presettable Decade/Binary Counter	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74177	Presettable Binary Counter	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74178	4–bit Universal Shift Register	FS2	30
74179	4–bit Universal Shift Register (Direct Clear)	FS2 + 9 x N2N + B1N	40
74180	9–bit Odd/Even Parity Checker	PO8 + 2 x D24 + V1N	23
74181	ALU/Function Generator	5 x V1N + 5 x T32 + 4 x D36 + 8 x X2N + 3 x T54 + N6B + N4B + 2 x N2N + 2 x N4P	113
74182	Look–ahead Carry Generator	R4P + 2 x V1N + 2 x T44 + T33 + D24	36
74183	Dual Carry–save Full Adder	2 x A1N	16
74184	BCD–to–binary Code Converter	These devices are ROM based	
74185	Binary–to–BCD Code Converter	These devices are ROM based	
74190	Synch Up/Down Counter (BCD)	4 x FDP + 4 x X2N + K1B + 3 x V1N + 3 x N3N + 9 x N2N + 2 x T32 + T43	
74191	Synch Up/Down Counter (Binary)	C47	68
74192	Up/Down Dual Clock Counter (BCD)	4 x C11 + 4 x V2B + N6B + 2 x N3N + R2N + T32 + T42 + T43	79
74193	Up/Down Dual Clock Counter (Binary)	4 x C11 + 2 x N6B + 4 x V2B + R2N + D24 + T32 + T42	72
74194	4–bit Bidirectional Universal Shift Register	FDR + 6 x V1N + R2N + 4 x D36 + D23 + B1N	48
74195	4–bit Parallel Access Shift Register	FS2 + D24 + 2 x V1N	34
74196	Preset Decade/Binary Counter/Latch	4 x FDP + 2 x R2N + 5 x N2N + 4 x N3N + K1B	49
74197	Preset Binary Counter/Latch	4 x FDP + 5 x N2N + 4 x N3N + K1B	47
74198	8–bit Bidirectional Universal Shift Register	2 x FDR + D24 + 10 x V1N + R2N + 8 x D36	89
74199	8–bit Bidirectional Universal Shift Register (JK Serial Input)	2 x FS2 + D24 + 3 x V1N + B1N + R2N + 8 x N2P	83
	or:	2 x FDR + 7 x D24 + T33 + 11 x V1N + R2N	85
74246	BCD–to–7-Segment Decoder/Driver (30V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74247	BCD–to–7-Segment Decoder/Driver (15V, Active Low Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74248	BCD–to–7-Segment Decoder/Driver (Internal Pull–up)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74249	BCD–to–7-Segment Decoder/Driver (Open Collector)	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53
74260	Dual 5–input NOR	2 x R6B	10
74265	Quad Complementary Output Element	B1N + V1N	
74266	Quad 2–EXNOR, Open Collector	4 x X1N	12
74273	Octal D–type FF with Clear	2 x FDR	52
74276	Quad J–K FF	4 x (FDP + V1N + D24) + 2 x B1N	46
74347	BCD–to–7-Segment Decoder/Driver	4 x V1N + 11 x N2N + 10 x N3N + 4 x N3P + 3 x N2P	53

Appendix F: Alphanumeric Index of Unit Cells

Appendix F: Alphanumeric Index of Unit Cells (Continued)

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Appendix F: Alphanumeric Index of Unit Cells (Continued)

Appendix F: Alphanumeric Index of Unit Cells (Continued)

Section 4

Sales Information

Introduction to Fujitsu

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly-owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to three marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The Advanced Products Division (APD) is responsible for the complete product development cycle, from design through operations support and worldwide marketing and sales. Products are the result of both internal development and external relationships, such as joint development agreements, technology licenses, and joint ventures. The SPARC™ RISC processor was developed by both APD and Sun Microsystems, Inc.

In addition to designing and selling a full line of SPARC processors and peripheral chips, APD also designed and is selling the EtherStar™ LAN controller — the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of APD's cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs, FETs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD).

Memory and programmable devices marketed by ICD include the following:

- DRAMs and DRAM Modules
- EPROMs
- EEPROMs
- NOVRAMs
- CMOS masked ROMs
- CMOS SRAMs and CMOS SRAM Modules
- BiCMOS SRAMs
- Bipolar PROMs
- ECL RAMs
- STRAMs (self-timed RAM)
- Hi-Rel PROMs and SRAMs
- Ultra High-speed ECL/ECL—TTL Translator Circuits
- Linear ICs and Transistors

Introduction to Fujitsu (Continued)

ASIC products offered by ICD include the following:

CMOS, ECL, and BiCMOS gate arrays
CMOS standard cells
Design Software Support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose	Gresham
Dallas	Chicago
Atlanta	Boston

Microcomputer and communications products offered by ICD include the following:

4-bit MCUs
8- and 16-bit MPUs
SCSI and controllers
DSPs
Prescalers
PLLs
Memory Cards

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, the Gresham Manufacturing Division began manufacturing ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Components of America**, markets connectors, keyboards, plasma displays, relays, and hybrid ICs.

Fujitsu Mikroelektronik GmbH (European Sales Operation)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a wholly-owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Europe. The wide range of ICs, LSI memories, microprocessors, and ASIC products are noted throughout Europe for design excellence and unmatched reliability. Branch offices are located in Munich, London, Paris, Stockholm, and Milan.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics Ireland, Ltd. (European Production Operation)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in the suburbs of Dublin, as Fujitsu's European Production Center for integrated circuits. FME assembles DRAMs, EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd. (European ASIC Design Operation)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with highly sophisticated CAD systems to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Asia PTE Ltd. (Asian/Oceanian Sales Operation)

Fujitsu Microelectronics Asia PTE Ltd. (FMA) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

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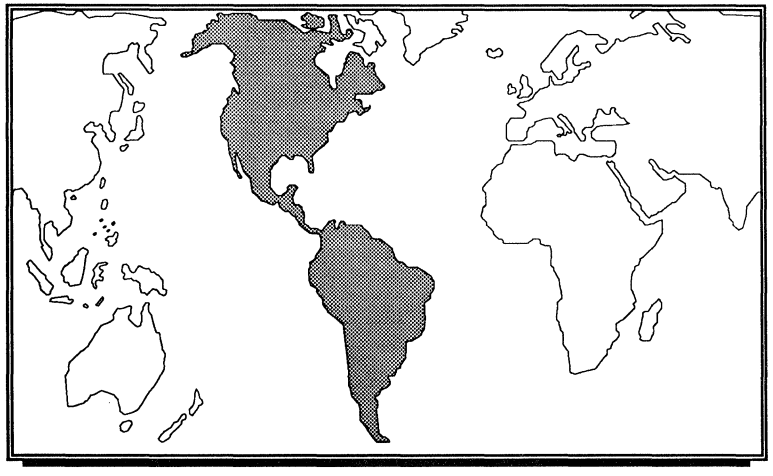

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Newport Beach, CA 92660
Tel: (714) 833–0300
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3350 Scott Blvd.,
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Front Range Marketing
3100 Arapahoe Road
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Connecticut

Conntech Sales, Inc.
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Waterbury, CT 06702
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Semtronic Associates, Inc.
657 Maitland Avenue
Altamonte Springs, FL 32701
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Semtronic Associates, Inc.
3471 NW 55th Street
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Milgray Electronics
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Fairfield, NJ 07006
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Marshall Industries
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Mt. Laurel, NJ 08054
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Milgray Electronics
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Vantage Components, Inc.
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Western Microtechnology, Inc.
387 Passaic Avenue
Fairfield, NJ 07006
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Albuquerque, NM 87107
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Marshall Industries
129 Brown Street
Johnson City, NY 13790
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Rochester, NY 14624
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95 Oser Avenue
P.O. Box 12248
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90–10 Colin Drive
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Marsh Electronics
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Marshall Industries
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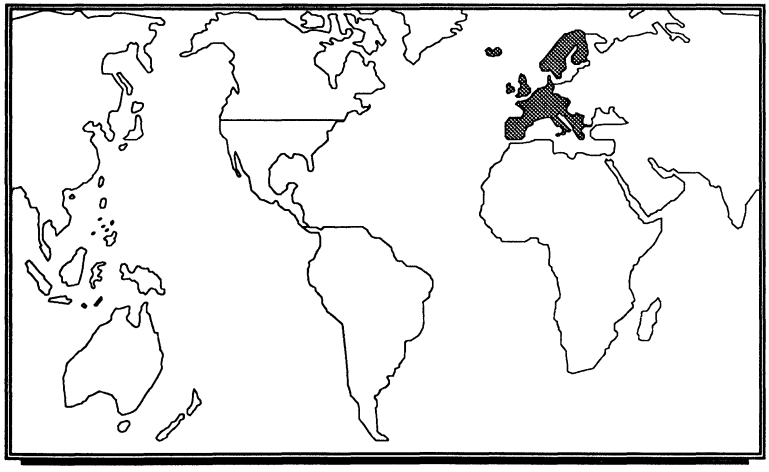

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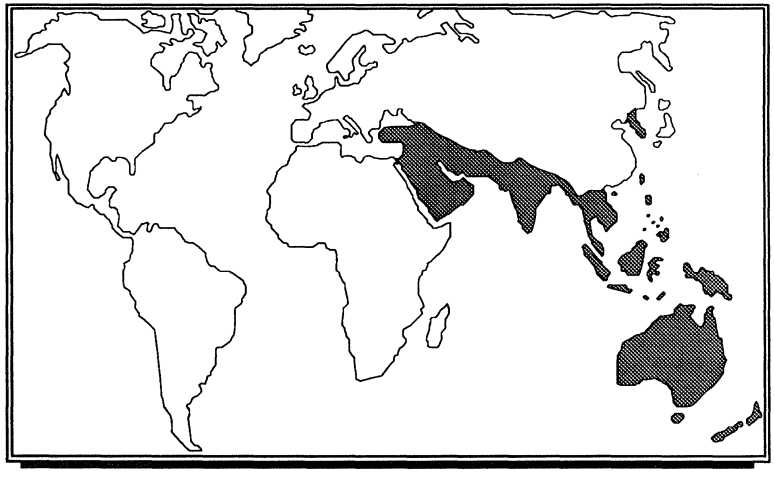

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Printed in USA