Data Book

Linear Products

1988

FUJITSU

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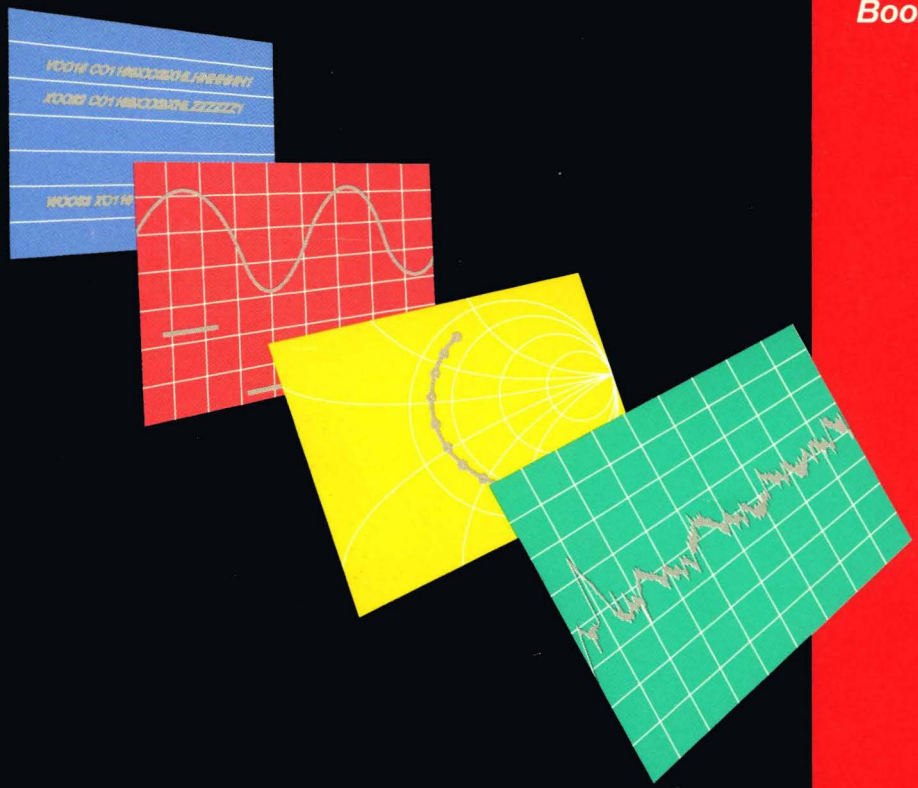
Data
Book



FUJITSU

Price
$10.90

Linear Products

1988 Data Book

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This document is published by the Technical Publications Department, Fujitsu Microelectronics, Inc., 3545 North First Street; San Jose, California, 95134-1804; U.S.A.

Printed in the U.S.A.

Edition 1.0

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Data Conversion D/A

Data Conversion A/D, D/A

Section 8 Other Analog Products

LINEAR PRODUCTS OVERVIEW

Introduction

Fujitsu manufactures a wide range of integrated circuits that include: memories, microprocessors, telecommunication circuits, ASIC, high speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and linear products.

The Linear Product Line offers devices for use in a wide range of applications. These linear products are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

Operational Amplifiers

The functions include well known industry standards and unique products available in standard packaging; e.g., DIP, flat-pack, as well as newer space saving surface mount packaging.

Comparators

Fujitsu's comparators include industry standards and proprietary functions and are available in both standard and surface mount packaging.

Audio

The Audio products represent Fujitsu's considerable capability in automotive radio. The Audio product line-up includes a comprehensive range of single-ended and balanced transformerless power amplifiers, associated pre-amplifiers, and control circuits.

Motor Driver

Motor drive products are useful for low power applications such as camera film transports, and door and access panel operation found in such products as VCRs and audio tape drives.

Disk Drive

Disk Drive products include a range of magnetic recording head amplifiers, head signal drivers, amplifiers, and VFOs.

Data Conversion (A/D)D/A)

The conversion circuits include analog-to-digital, digital-to-analog and circuits which combine both. The Fujitsu line-up includes general purpose multi-channel microprocessor and highspeed video and graphics oriented products. The video and graphics performance-level products include A/Ds with performance up to 60Msps, RAM DACS, triple DACS for color applications, and combined A/D-D/A suitable for use in single chip digital video processing.

Other Linear Products

Other Linear products include special pre-amplifiers for use in basic physics and nuclear research, line drivers and receivers, decoder driver, LED decoder, frequency-to-voltage converters and MOS Analog switch.

Section 1

Operational Amplifiers

Fujitsu Part No.	Description	Features	Equiv. Prod.	Power Supply (V)	Package	No. of Pins
MB3603	Single	Low Offset Wide Common Mode 1/P	µA741	+15, -15	Ceramic DIP Plastic DIP	14 14
MB3609	Single	Low Offset Wide Common Mode 1/P	µA741	+15, -15	Ceramic DIP Plastic DIP	8 8
MB3604	Single	GBW = 300MHz, with Buffer Tr (50mA)	—	+12, -6	Ceramic DIP Plastic DIP	16 16
MB3614	Quad	Wide Common Mode 1/P	LM324	+3 ~ -30	Plastic DIP Ceramic DIP Plastic Flatpak	14 14 14
MB3615	Quad	Low Crossover Distortion	MC3303	+3 ~ +36	Plastic DIP Plastic Flatpak	14 14
MB47082	Dual	JFET Input, Ii = 30pA, SR = 2V/µS	TL082	±1.5 ~ ±15	Plastic DIP Plastic Flatpak SIP	8 8 9
MB47358	Dual	Low Crossover Distortion	LM358	±3 ~ ±30 ±1.5 ~ ±15	Plastic DIP Plastic Flatpak SIP	8 8 9
MB47833	Dual	Low Noise, Low Distortion	LM833	±5 ~ ±15	Plastic DIP Plastic Flatpak SIP	8 8 9

FUJITSU

OPERATIONAL AMPLIFIER

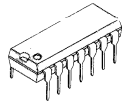
MB3603 MB3609

May 1988
Edition 1.0

OPERATIONAL AMPLIFIER

The Fujitsu MB3603/3609 are high gain monolithic operational amplifiers. The MB3603/3609 are suitable for industrial measurement instrument or controller because of low offset voltage, high input impedance, wide common-mode input voltage range and wide output voltage range.

- Not required frequency compensation
- On-chip protection circuitry
- Adjustable offset voltage
- Wide common-mode input voltage range and wide output voltage range
- Low power dissipation
- No latch up
- Pin assignment: MB3609 same as μA741



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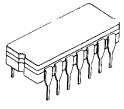

CERAMIC PACKAGE
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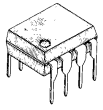
MB3603



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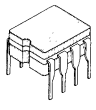

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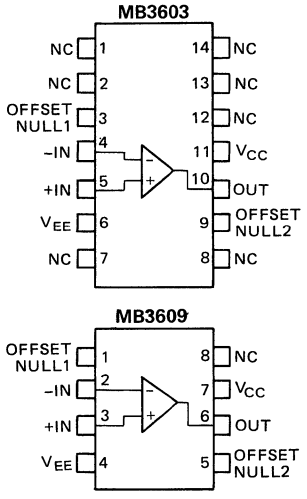
MB3609

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A = 25°C)

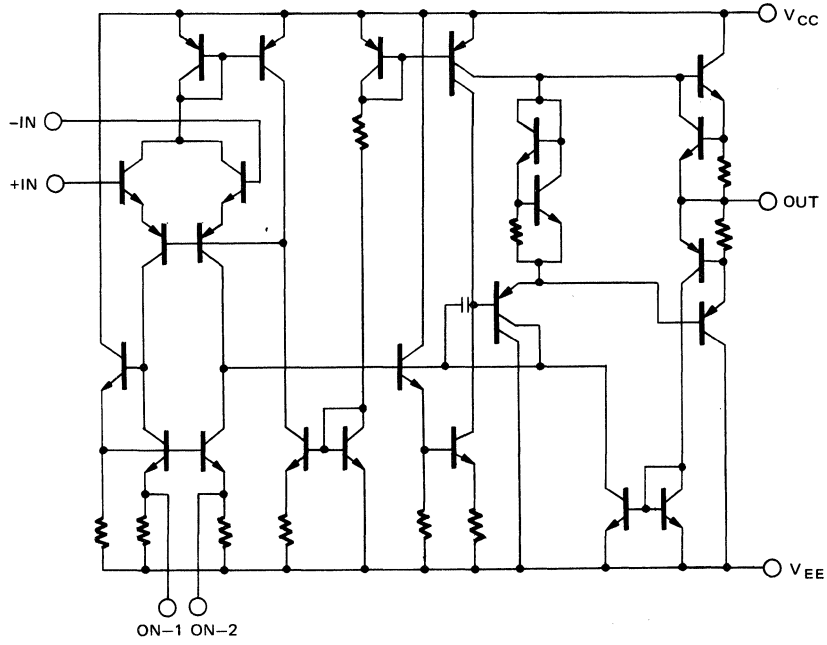
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+18	V
Power Supply Voltage		V_{EE}	−18	V
Differential Input Voltage		V_{ID}	±30	V
Common-mode Input Voltage		V_I	±15	V
Power Dissipation		P_D	500	mW
Storage Temperature	Plastic	T_{STG}	−55 to 125	°C
	Ceramic		−65 to 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB3603/3609 EQUIVALENT CIRCUITS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6 to 15	V
Power Supply Voltage	V_{EE}	−6 to −15	V
Operating Temperature	T_A	−20 to +75	°C

DC CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Input Offset Voltage	V_{IO}	R_S = 10kΩ, V_O = 0		10	mV
Input Offset Current	I_{IO}	V_O = 0		220	nA
Input Bias Current	I_I	V_O = 0		600	nA
Voltage Gain	A_V	R_L = 2kΩ, V_O = ±10V	15,000		
Common-mode Rejection Ratio	CMRR	V_I = ±7.5V	70		dB
Power Supply Rejection Ratio	SVRR	R_S = 10kΩ, ΔV_{CC} = 2.5V, ΔV_{EE} = 2.5V, V_O = 0		150	μV/V
Maximum Output Voltage	V_{OM}	R_L = 2kΩ	±10		V
Common-mode Input Voltage	V_{CM}		±12		V
Power Supply Current	I_{SUP}	V_O = 0		3.1	mA
Input Resistance	R_{IN}		300		kΩ

AC CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, T_A = 25 ± 2°C)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Frequency Bandwidth	BW	R_L = 2kΩ	100		kHz
Slew Rate	SR	R_L = 2kΩ, V_O = ±10V	0.1		V/μs

1

TYPICAL CHARACTERISTICS CURVES

Fig. 2 – OPEN LOOP VOLTAGE GAIN vs. POWER SUPPLY VOLTAGE

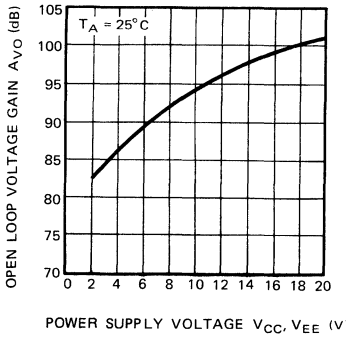


Fig. 3 – OUTPUT VOLTAGE vs. POWER SUPPLY VOLTAGE

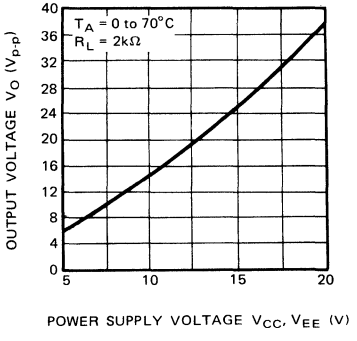


Fig. 4 – COMMON-MODE INPUT VOLTAGE vs. POWER SUPPLY VOLTAGE

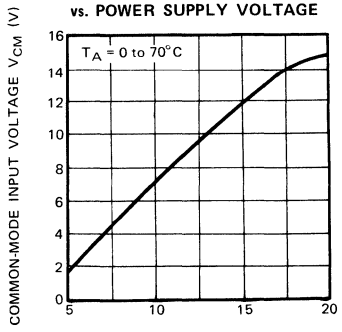


Fig. 5 – INPUT BIAS CURRENT vs. TEMPERATURE

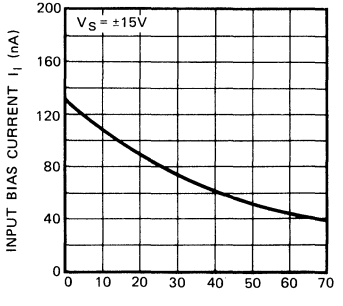


Fig. 6 – INPUT OFFSET CURRENT vs. TEMPERATURE

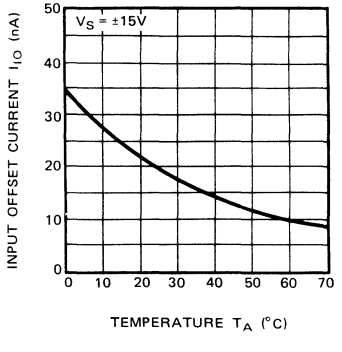


Fig. 7 – OUTPUT VOLTAGE vs. LOAD RESISTANCE

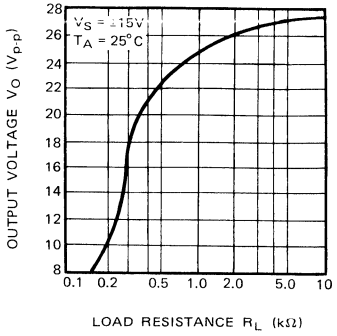


Fig. 8 – OPEN LOOP VOLTAGE GAIN vs. FREQUENCY

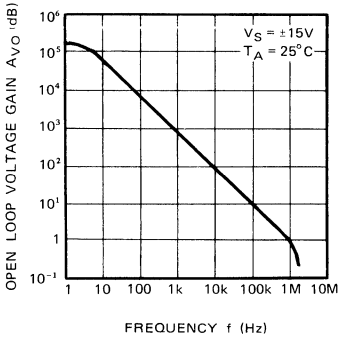


Fig. 9 – OUTPUT VOLTAGE vs. FREQUENCY

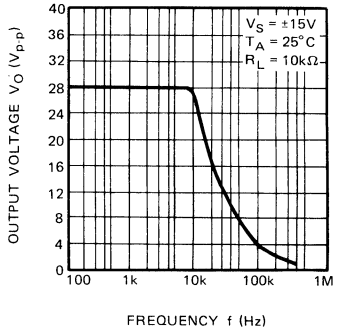
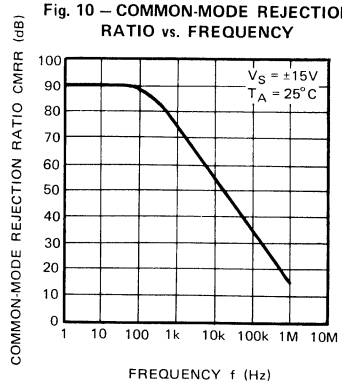


Fig. 10 – COMMON-MODE REJECTION RATIO vs. FREQUENCY



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PACKAGE DIMENSIONS (MB3603)

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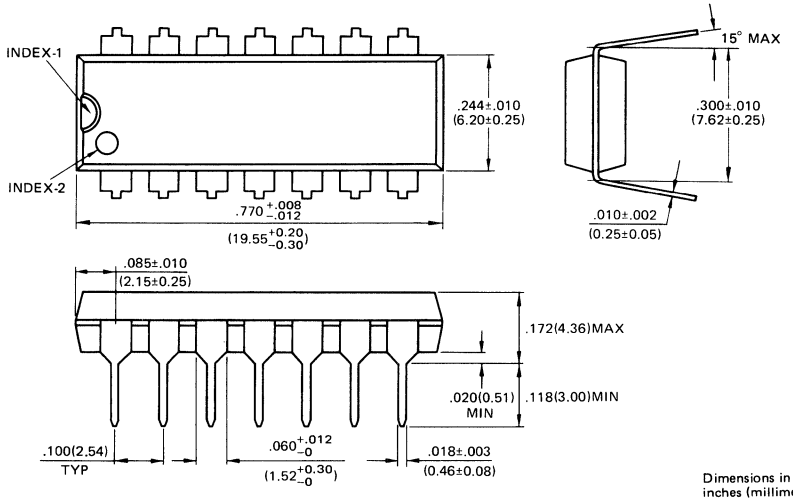

Dimensions in inches (millimeters)

14-LEAD CERAMIC CERDIP DUAL IN-LINE PACKAGE
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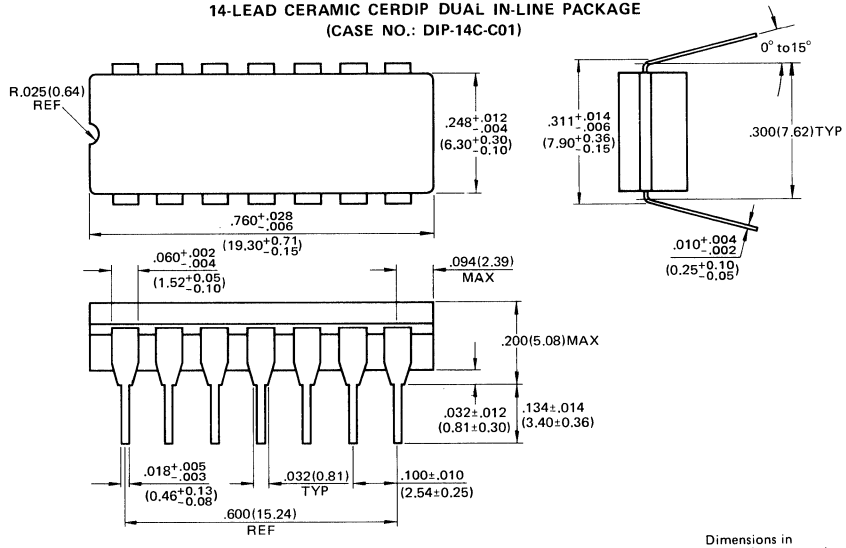

Dimensions in inches (millimeters)

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PACKAGE DIMENSIONS (MB3609)

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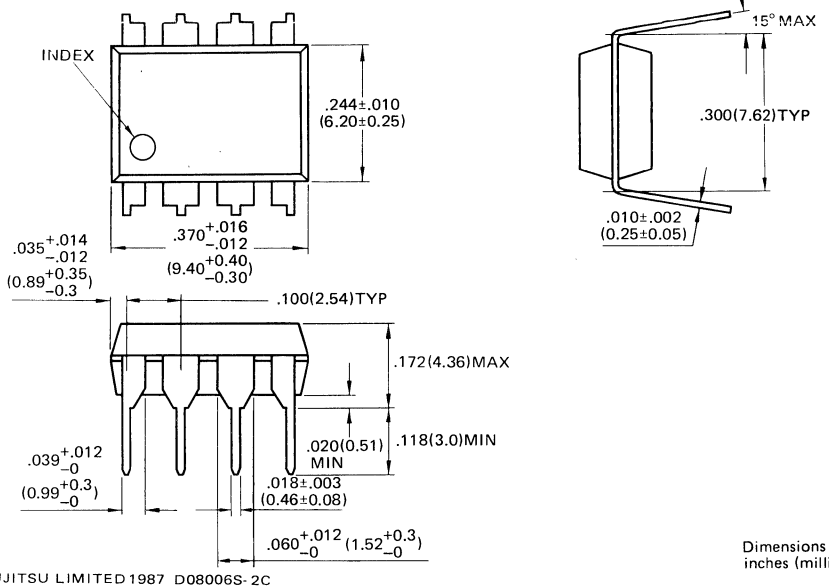

Dimensions in
inches (millimeters)

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PACKAGE DIMENSIONS (MB3609)

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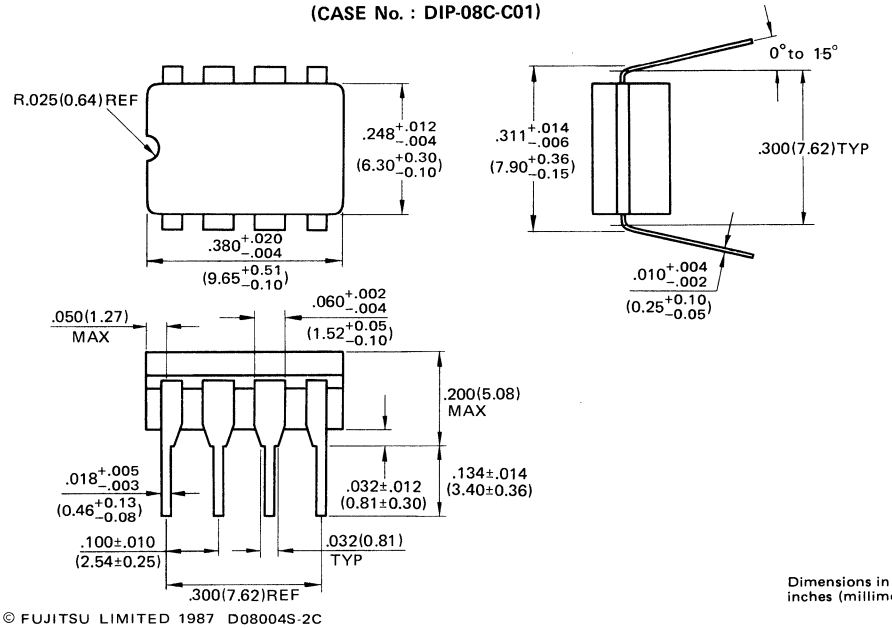

Dimensions in inches (millimeters)

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FUJITSU

HIGH FREQUENCY OPERATIONAL AMPLIFIER

MB3604

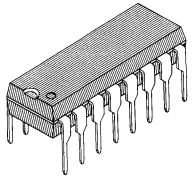
1

December 1987
Edition 1.0

HIGH FREQUENCY OPERATIONAL AMPLIFIER

The Fujitsu MB3604 is a monolithic high frequency operational amplifier fabricated by Fujitsu Bipolar Technology.

The MB3604 has differential inputs, single-end output, and an on-chip buffer transistor for video band use.



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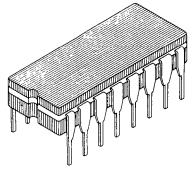

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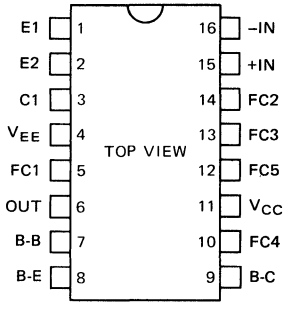


ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A = 25°C)

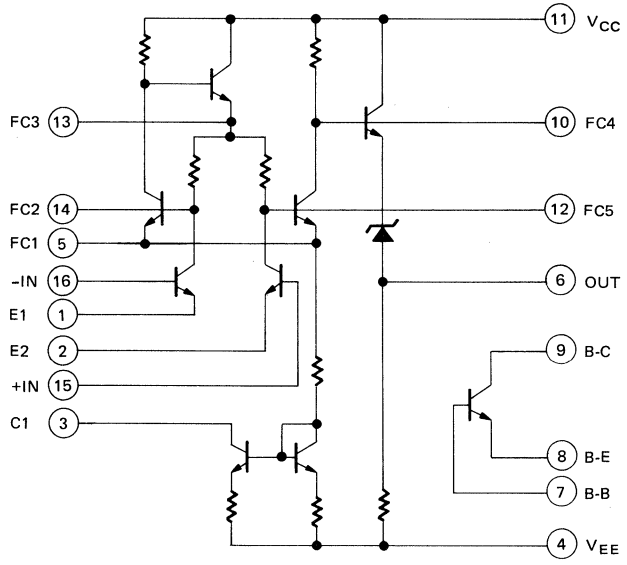
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+14	V
Power Supply Voltage		V_{EE}	−7	V
Differential Input Voltage		V_{ID}	±5	V
Common Mode Input Voltage		V_I	−7 to +1.4	V
Output Current		I_O	10	mA
Collector-Emitter Voltage for Buffer Transistor		V_{CEO}	21	V
Collector Current for Buffer Transistor		I_C	50	mA
Power Dissipation		P_D	500	mW
Storage Temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB3604 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+12±5%	V
Power Supply Voltage	V_{EE}	−6±5%	V
Operating Temperature	T_A	−20 to +75	°C

ELECTRICAL CHARACTERISTICS - I

(V_{CC} = +12V, V_{EE} = -6V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Input Offset Voltage	V_{IO}	R_S = 50Ω		6.0	mV
Input Offset Current	I_{IO}			5.0	μA
Input Bias Current	I_I			20	μA
Voltage Gain	A_V	$R_L \geq 5k\Omega$	60		dB
Common Mode Rejection Ratio	CMRR	R_S = 50Ω	70		dB
Maximum Positive Output Voltage	$V_{OM}(+)$	V_{IN} = 0.1V	4.0		V
Maximum Negative Output Voltage	$V_{OM}(-)$	V_{IN} = 0.1V	5.5		V
0dB Frequency	f_O	R_S = 50Ω, R_L = 50Ω	90		MHz
Input Resistance	R_{IN}	f = 1kHz	3.0		kΩ
Power Supply Current	$I_{SUP}(+)$			9.0	mA
Power Supply Current	$I_{SUP}(-)$			6.7	mA
Collector Cutoff Current for Buffer Transistor	I_{CBO}	V_{CB} = 18V, I_E = 0		2.0	μA
DC Current Gain for Buffer Transistor	h_{FE}	V_{CB} = 6V, I_C = 20mA	40	200	

ELECTRICAL CHARACTERISTICS - II

(V_{CC} = +12V, V_{EE} = -6V, T_A = 25°C)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output Resistance	R_O	f = 1kHz		200	Ω
3dB Frequency	f_C	R_S = 50Ω, R_L = 50Ω	1		MHz
Slew Rate	SR	$A_V \doteq 1$, R_I = 50Ω	10		V/μs
Current Gain-Bandwidth Product for Buffer Transistor	f_T	V_{CE} = 6V, I_C = 20mA	300		MHz
Collector Capacitance for Buffer Transistor	C_{ob}	V_{CE} = 6V, I_E = 0A, f = 1MHz		5	pF

1

MEASUREMENT CIRCUT DIAGRAM

Fig. 2 – 0dB FEEDBACK AMPLIFIER

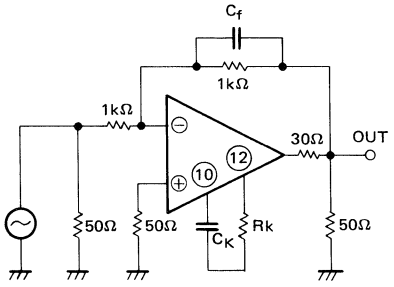


Fig. 3 – 20dB FEEDBACK AMPLIFIER

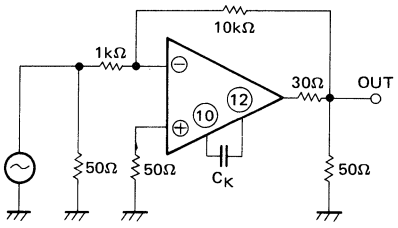
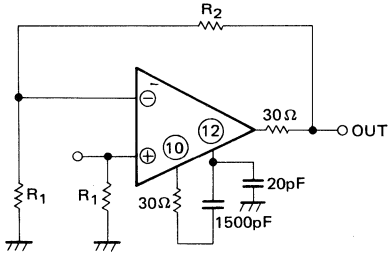


Fig. 4 – LOW FREQUENCY FEEDBACK AMPLIFIER



PIN CONNECTION FOR Fig. 2 to Fig. 5

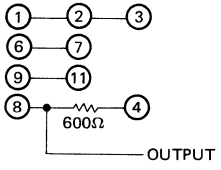


Fig. 5 – FREQUENCY CHARACTERISTICS MEASUREMENT CIRCUIT

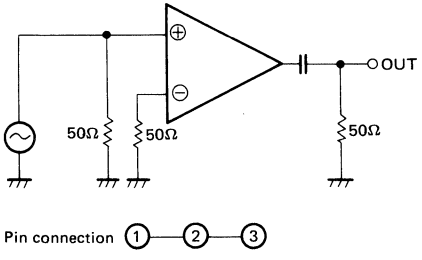
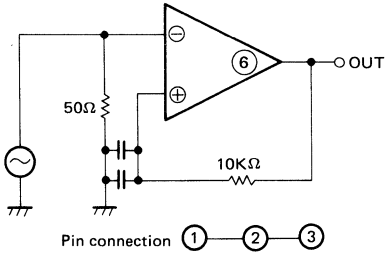


Fig. 6 – POWER SUPPLY VOLTAGE vs. VOLTAGE GAIN MEASUREMENT CIRCUIT



1

ELECTRICAL CHARACTERISTICS CURVES

Fig. 7 – 0dB FEEDBACK AMPLIFIER

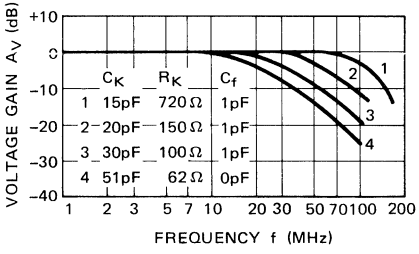


Fig. 8 – 20dB FEEDBACK AMPLIFIER

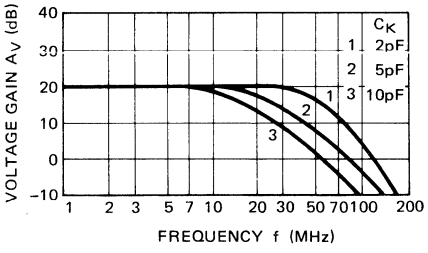


Fig. 9 – LOW FREQUENCY FEEDBACK AMPLIFIER

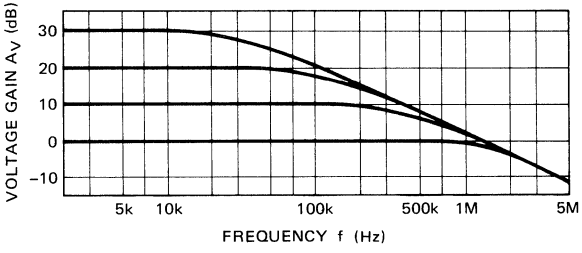


Fig. 10 – FREQUENCY CHARACTERISTICS

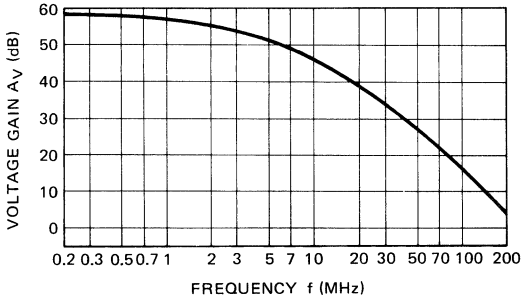
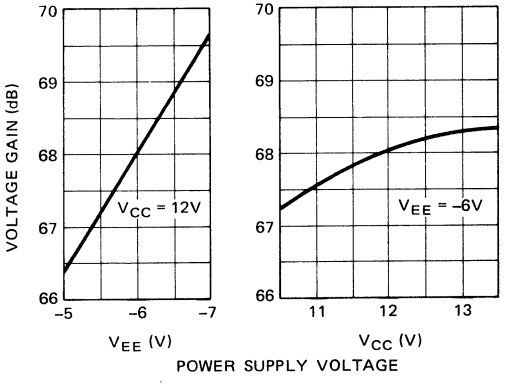


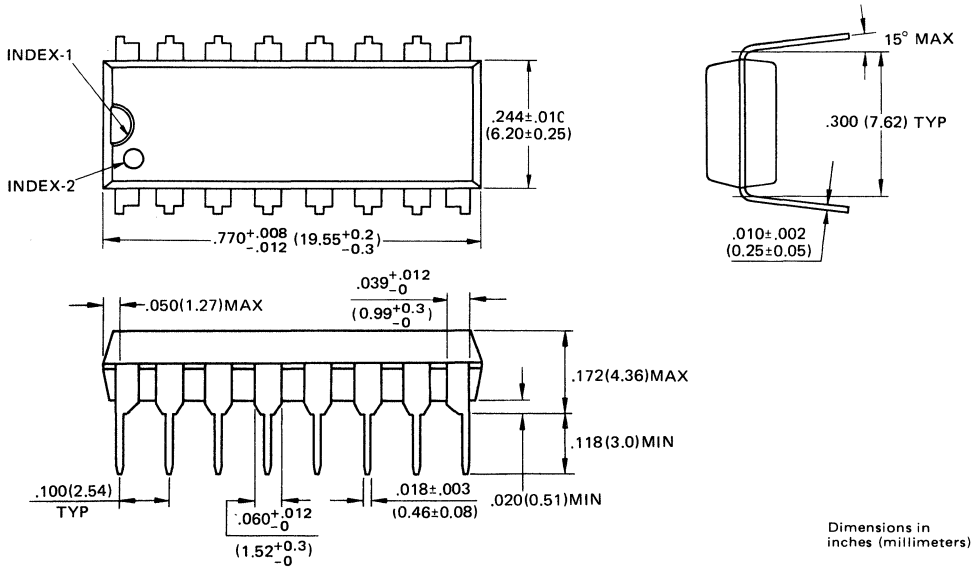
Fig. 11 – POWER SUPPLY VOLTAGE vs. VOLTAGE GAIN



1

PACKAGE DIMENSIONS

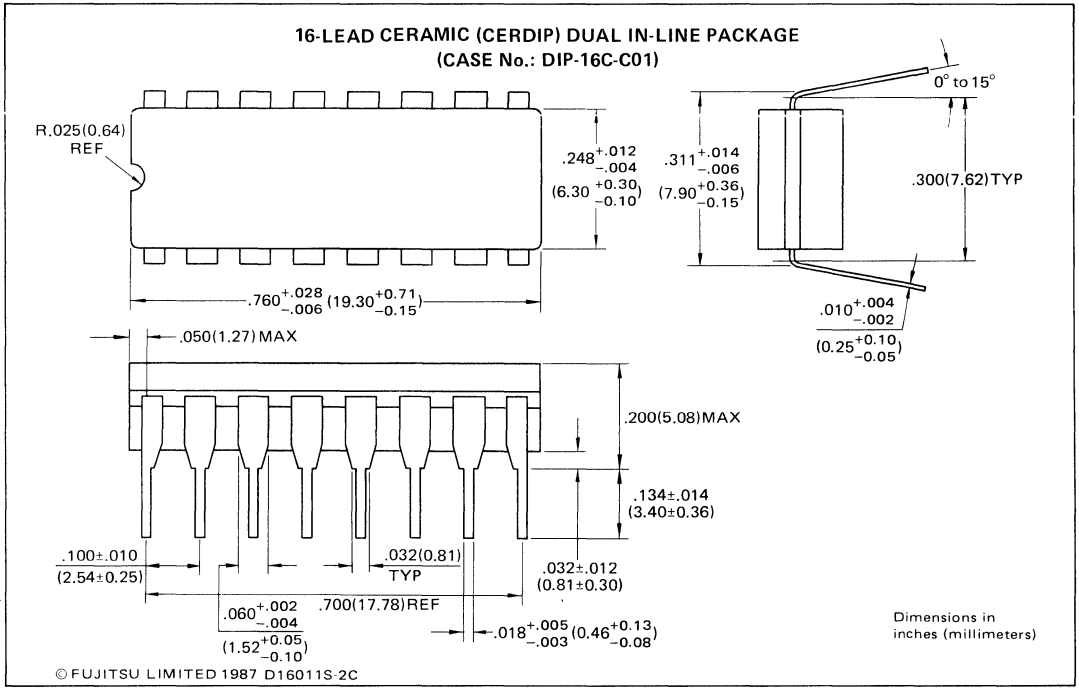
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS



QUAD OPERATIONAL AMPLIFIER

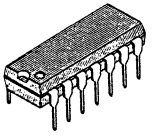
1

The Fujitsu MB3614 is a Quad operational amplifier having a phase compensatory circuit and operates from a single power supply or dual power supplies.
The device has equivalent electrical characteristics of current industrial standard operational amplifier and requires low power supply current.
MB3614 can be high density mounted because it integrates 4 circuits in DIP/FPT 14-pin package.

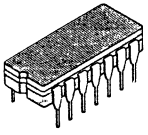
- No phase compensation required
- Wide power supply voltage

  Single power supply : +3 to +30 V

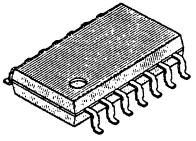
  Dual power supplies : ±1.5 to ±15 V
- Wide input common mode range : 0 to (V_{CC}-1.5) V
- Low power supply current : 0.8 mA typ.
- Low Input Offset Voltage : 2 mV typ.



PLASTIC PACKAGE
DIP-14P-M02

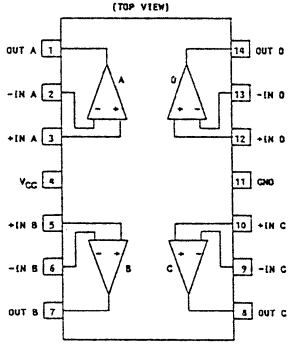


CERAMIC PACKAGE
DIP-14C-C04



PLASTIC PACKAGE
FPT-14P-M01

PIN ASSIGNMENT



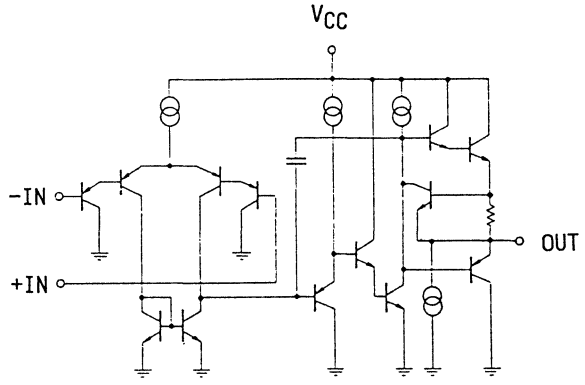
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	32	V
Differential Input Voltage		V_{ID}	32	V
Common Mode Input Voltage		V_I	-0.3 to +32	V
Power Dissipation		P_D	570	mW
Operating Temperature		T_A	-20 to +75	°C
Storage Temperature	Plastic	T_{STG}	-55 to +125	°C
	Ceramic	T_{STG}	-65 to +150	°C

Note:* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.2- EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC}=5V, T_A=25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}			2	7	mV
Input Offset Current	I_{IO}			5	50	nA
Input Bias Current	I_I *			45	250	nA
Power Supply Current	I_{CC}	$R_L = \infty$		0.8	2.0	mA
Input Common Mode Voltage	V_{CM}		0		V_{CC}-1.5	V
Voltage Gain	A_V	$R_L \geq 2k\Omega$	25	100		V/mV
Output Voltage	V_{OH}	V_{CC}=30V, R_L=2kΩ	26	28		V
	V_{OL}	V_{CC}=5V, $R_L \leq 10k\Omega$		5	20	mV
Output Current	I_{SOURCE}	V_{CC}=15V, V_{IN}^+=1V	20	40		mA
	I_{SINK}	V_{CC}=15V, V_{IN}^-=1V	10	20		mA
Common Mode Rejection Ratio	CMRR		65	85		dB
Power Supply Voltage Rejection Ratio	SVRR		65	100		dB
Channel Separation	CS			120		dB

NOTE: * A direction of the input bias current flows from IC because first input transistor consists of PNP.

TYPICAL CHARACTERISTICS CURVES

Fig.3- Power Supply Current vs. Power Supply Voltage

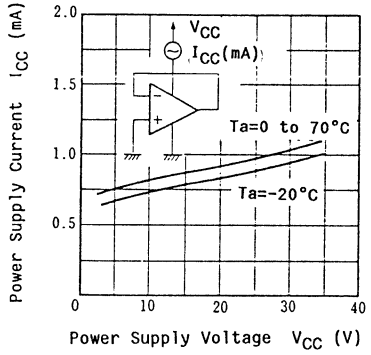


Fig.4-Input Bias Current vs. Temperature

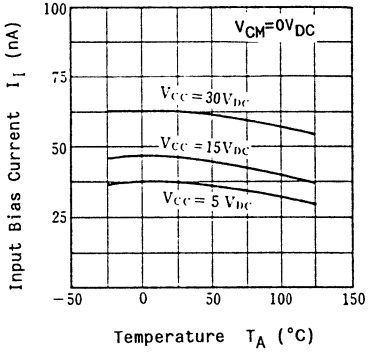


Fig.5- Voltage Gain vs. Power Supply Voltage

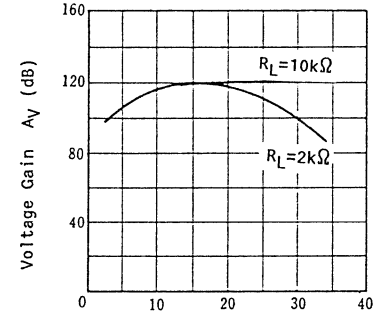


Fig.6- Voltage Gain vs. Frequency

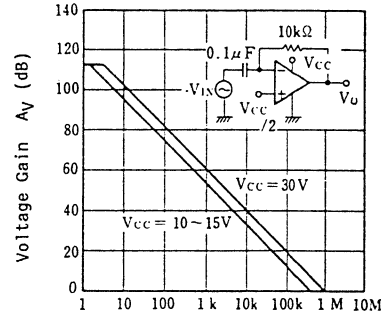


Fig.7- Output Voltage vs. Frequency

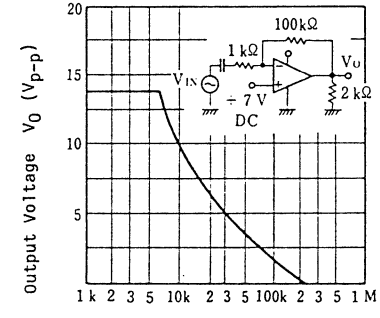
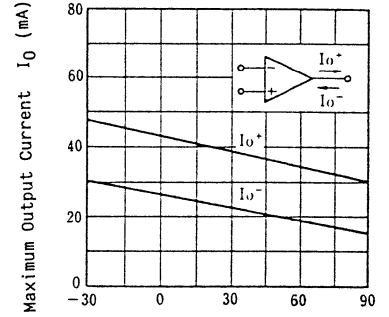
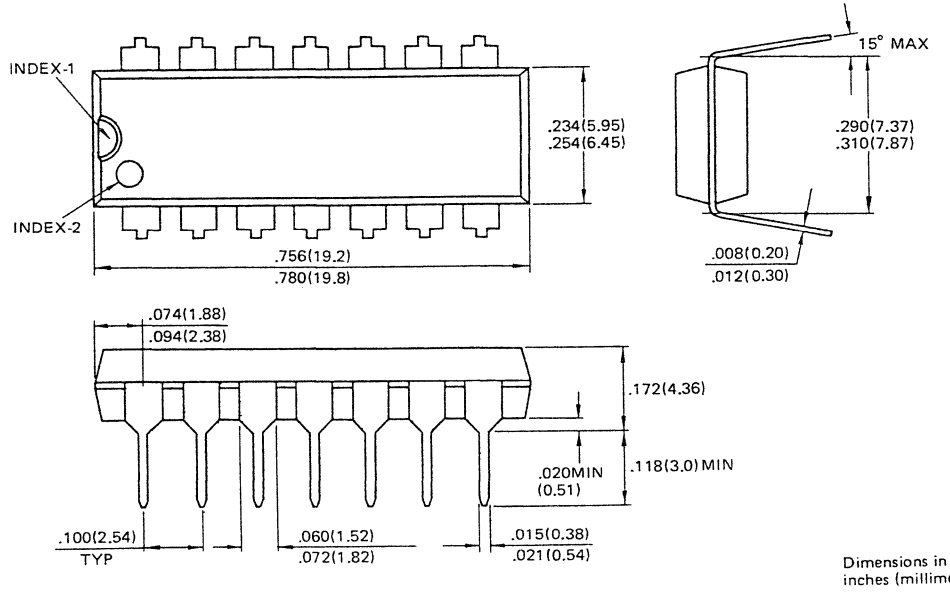


Fig.8- Maximum Output Voltage vs. Temperature



PACKAGE DIMENSIONS

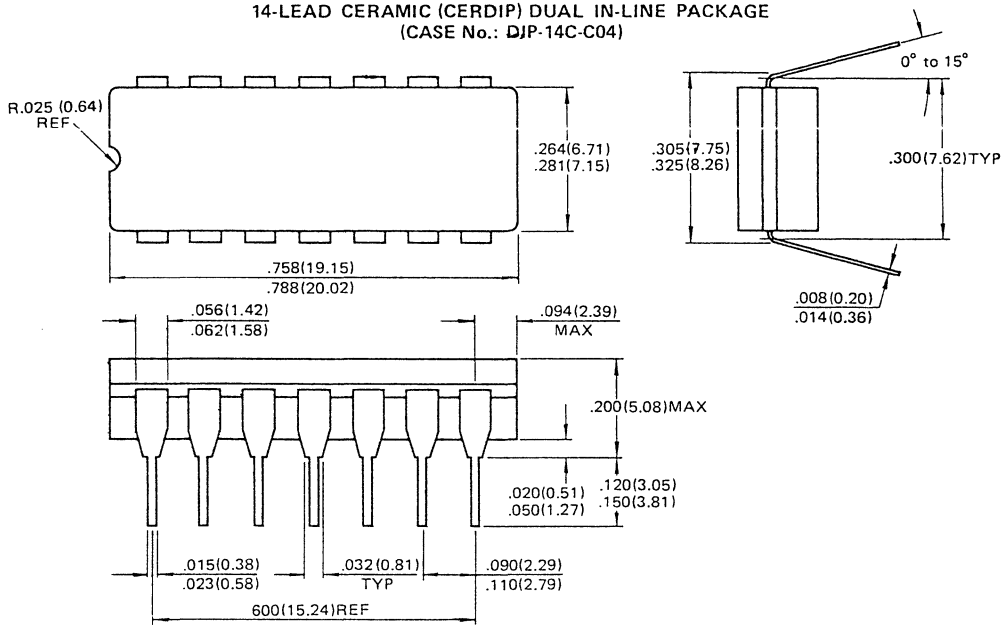
14-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

14-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-14C-C04)



Dimensions in
inches (millimeters)

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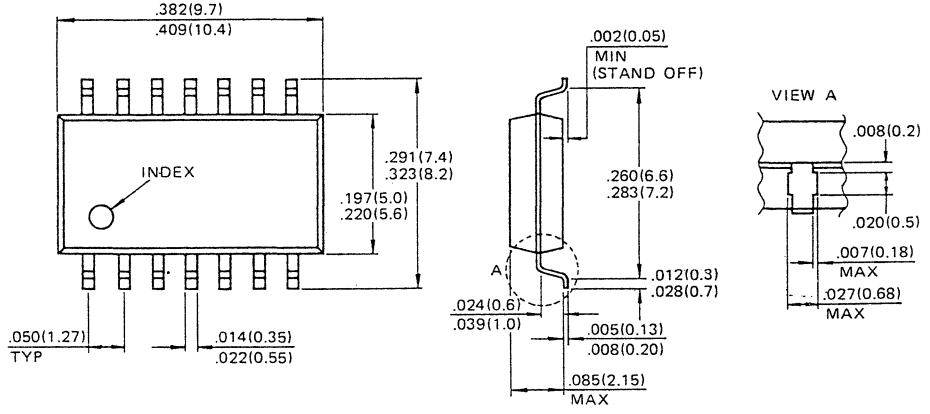
14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



FUJITSU

MB3615

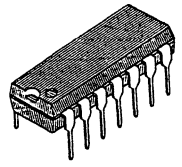
QUAD OPERATIONAL AMPLIFIER

The Fujitsu MB3615 is a Quad operational amplifier having a phase compensatory circuit and operates from a single power supply or dual power supplies.
The device has equivalent electrical characteristics of current industrial standard operational amplifier and requires low power supply current.
MB3615 can be high density mounted because it integrates 4 circuits in DIP-14-pin package. It is taken the countermeasure for cross-over distortion, so can be used for amplifying AC.
The MB3615 is pin compatible with Motorola MC3303.

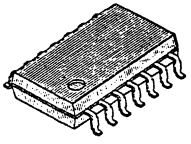
- No phase compensation required
- Wide power supply voltage

  Single power supply : +3 to +36 V

  Dual power supplies : ±1.5 to ±18 V
- Wide input common mode range : V_{EE} to (V_{CC}-1.5) V
- Low power supply current : 2 mA typ.
- Low Cross-over distortion

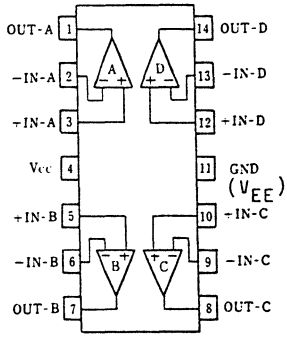


PLASTIC PACKAGE
DIP-14P-M02



PLASTIC PACKAGE
FPT-14P-M01

PIN ASSIGNMENT
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (See NOTE)

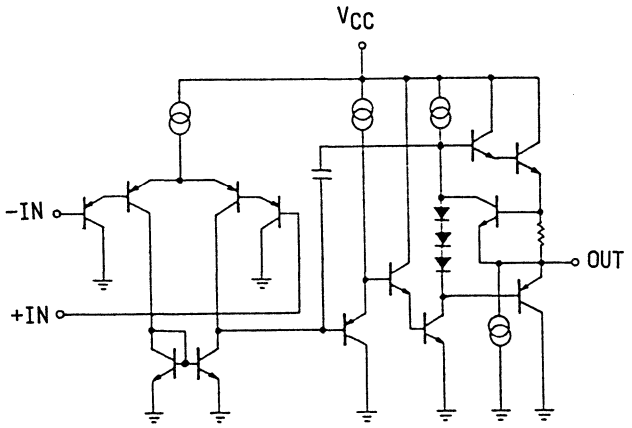
Rating	Symbol	Value	Unit
Power Supply Voltage *	V_{CC}	36	V
Differential Input Voltage *	V_{ID}	36	V
Input Common Mode Voltage *	V_I	-0.3 to +36	V
Power Dissipation	P_D	570	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: * Single Power Supply.

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.2- EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC}=+15V, V_{EE}=-15V, T_A=25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}			2	7	mV
Input Offset Current	I_{IO}			5	50	nA
Input Bias Current	I_I *			45	250	nA
Power Supply Current	I_{CC}	$R_L=\infty$		2.0	4.0	mA
Input Common Mode Voltage	V_{CM}		V_{EE}		V_{CC}-1.5	V
Voltage Gain	A_V	$R_L \geq 2k\Omega$	20	100		V/mV
Output Voltage	V_{OH}	$R_L=2k\Omega$	±10	12		V
	V_{OL}	$R_L=10k\Omega$	±12	13		V
Output Current	I_{SOURCE}		10	40		mA
	I_{SINK}		10	20		mA
Common Mode Rejection Ratio	CMRR		70	85		dB
Power Supply Voltage Rejection Ratio	SVRR		65	100		dB
Channel Separation	CS			120		dB

NOTE: * A direction of the input bias current flows from IC because first input transistor consists of PNP.

1

Fig.3- Power Supply Current vs. Power Supply Voltage

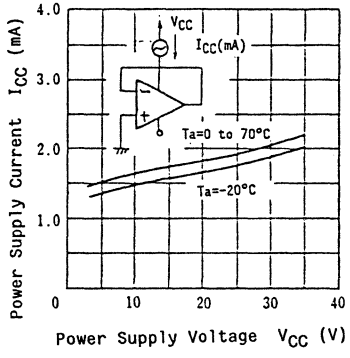


Fig.4-Input Bias Current vs. Temperature

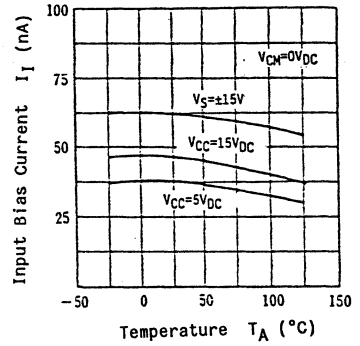


Fig.5- Voltage Gain vs. Power Supply Voltage

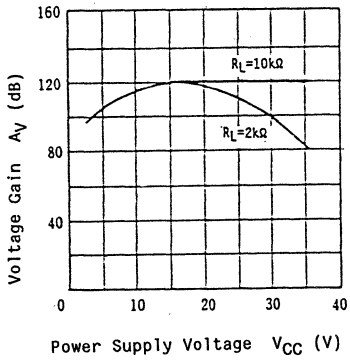


Fig.6- Voltage Gain vs. Frequency

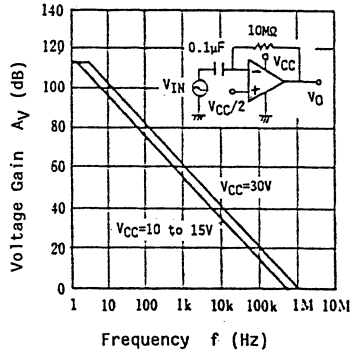


Fig.7- Output Voltage vs. Frequency

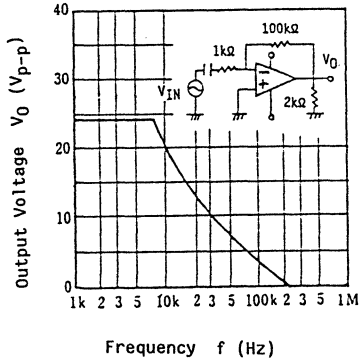
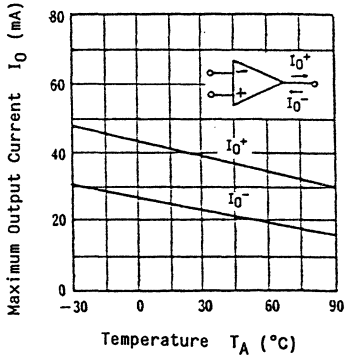
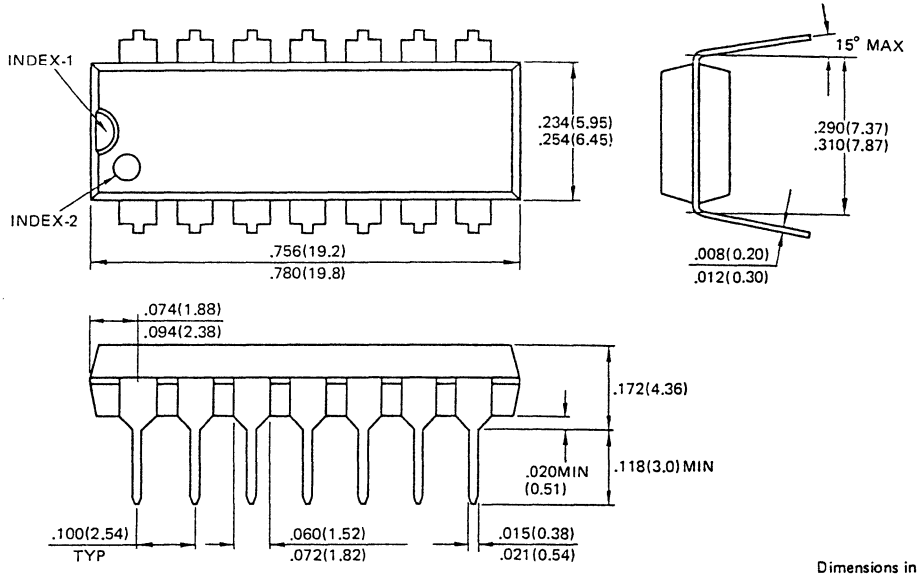


Fig.8- Maximum Output Voltage vs. Temperature



PACKAGE DIMENSIONS

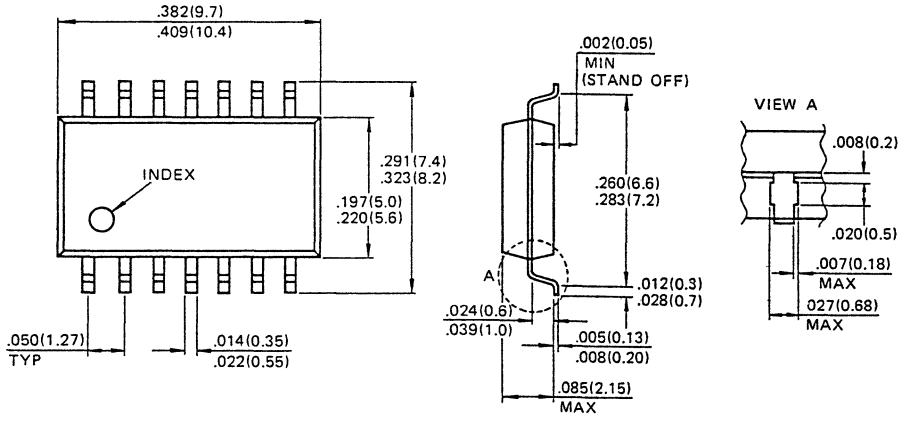
14-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)



Dimensions in
inches (millimeters)

1

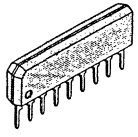
14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



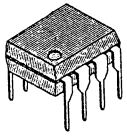
MB47082

J-FET INPUT OPERATIONAL AMPLIFIER

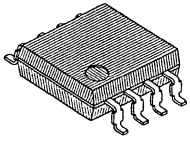
The Fujitsu MB47082 is designed for a dual operational amplifier with P channel-typed J-FET used at the input stage. Its slew rate is faster (more than one figure) comparing with the standard operational amplifier and also its band width is wide because of its high input impedance characteristic and well-built transmission conductance at the input stage comparing with the bipolar transistor.
The MB47082 is suitable for a D/A converter and a Sample & Hold circuit that need to cover from a small singnal amplification to a fast and large signal change.



PLASTIC PACKAGE
SIP-9P-M01



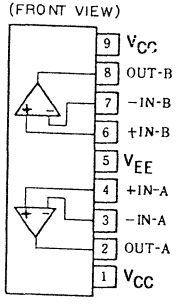
PLASTIC PACKAGE
DIP-8P-M01

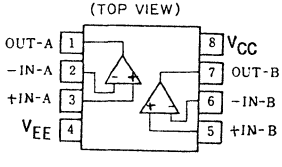


PLASTIC PACKAGE
FPT-8P-M01

- Compatible with TL082
- Wide operating power supply voltage : ±5V to ±15V
- Fast slew rate : 13V/μs typ.
- Low input bias current : 30pA typ.
- Wide frequency bandwidth : 3MHz typ.
- On-chip internal frequency compensation
- Low noise

PIN ASSIGNMENT





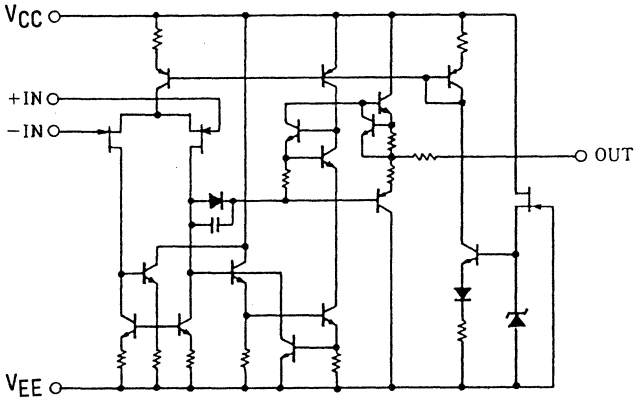
ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A=25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	V
	V_{EE}	−18	V
Differential Input Voltge	V_{ID}	±30	V
Common-mode Input Voltage	V_I	±15	V
Power Dissipation	P_D	350 (TA≤55°C)	mW
Operating Temperature	T_A	−20 to 75	°C
Storage Temperature	T_{STG}	−55 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB47082 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC},V_{EE}	±5 to ±15	V
Operating Temperature	T_A	-20 to +75	°C

RECOMMENDED OPERATING CONDITIONS

(T_A=25°C, V_{CC}=15V, V_{EE}=-15V)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S≤50Ω		5.0	15.0	mA
Input Offset Current	I_{IO}			5	200	pA
Input Bias Current	I_I			30	400	pA
Common-mode Input Voltage	V_{CM}		±10			V
Common-mode. Rejection Ratio	CMRR	R_S≤10kΩ	70	86		dB
Power Supply Voltage Rejection Ratio	SVRR	R_S≤10kΩ	70	86		dB
Voltage Gain	A_V	R_L=2kΩ	25	200		V/mV
Power Supply Current	I_{CC}			3.5	5.6	mA
Maximum Output Voltage	V_{OM}	R_L≥18kΩ	±12	±13.5		V
		R_L≥2kΩ	±10	±12		V
Output Current	I_{SOURCE}	V_O=V_{EE}		-25	-10	mA
	I_{SINK}	V_O=V_{CC}	25	40		mA
Frequency Bandwidth	BW	R_L=2kΩ		3.0		MHz
Slew Rate	SR	R_L=2kΩ,C=100pF,A_V=1		13		V/μs
Channel Separation	CS	f=1kHz		120		dB
Equivalent Input Noise Voltage	V_{NI}	f=1kHz,R_S=100Ω		25		$nV/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS CURVES

FIG.2 - VOLTAGE GAIN VS. FREQUENCY

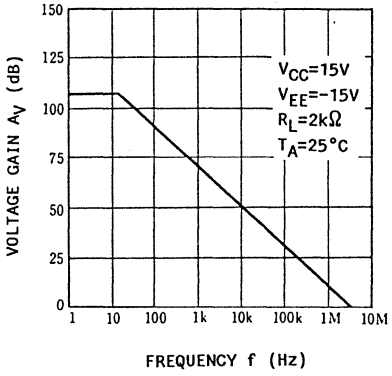


FIG.3 - OUTPUT VOLTAGE VS. FREQUENCY

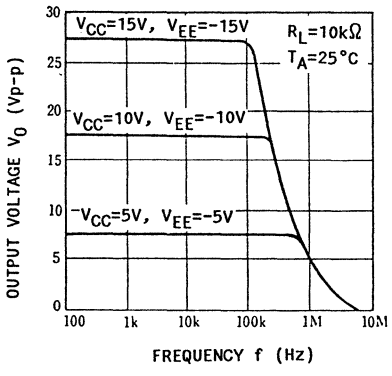


FIG.4 - INPUT BIAS CURRENT VS. COMMON-MODE INPUT VOLTAGE

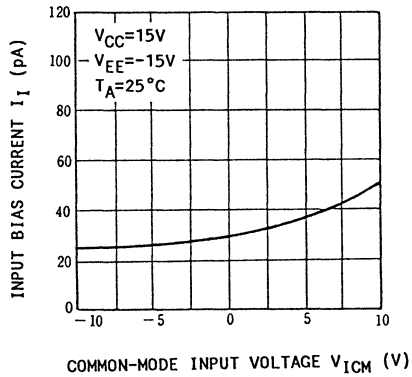


FIG.5 - INPUT BIAS CURRENT VS. TEMPERATURE

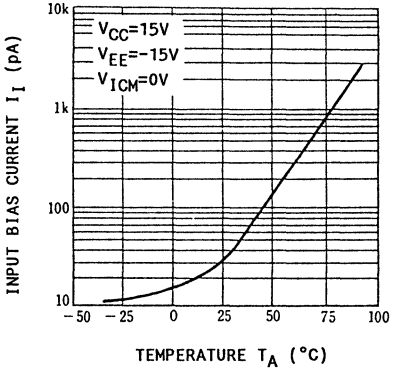


FIG.6 - OUTPUT VOLTAGE VS. POWER SUPPLY VOLTAGE

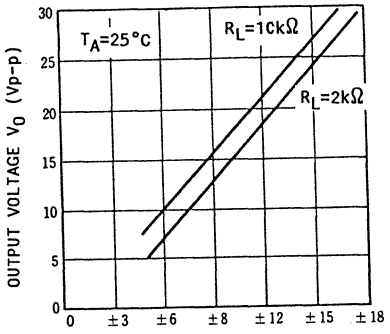
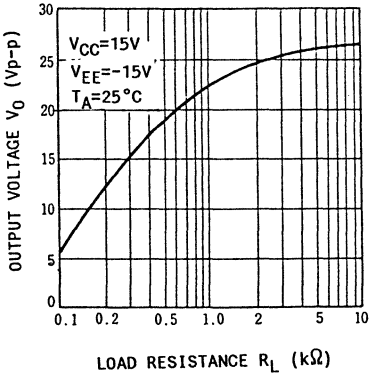


FIG.7 - OUTPUT VOLTAGE VS. LOAD RESISTANCE



ELECTRICAL CHARACTERISTICS CURVES (Continued)

FIG.8 - INPUT NOISE VOLTAGE VS. FREQUENCY

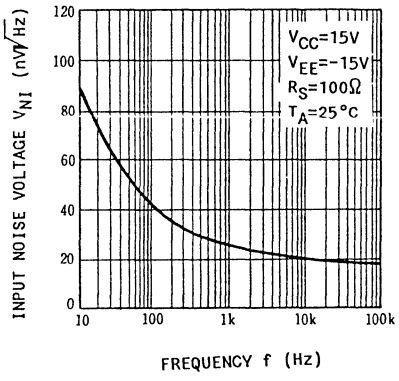


FIG.9 - PULSE RESPONSE

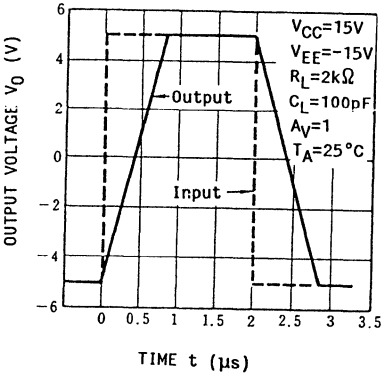


FIG.10- POWER SUPPLY CURRENT VS. POWER SUPPLY VOLTAGE

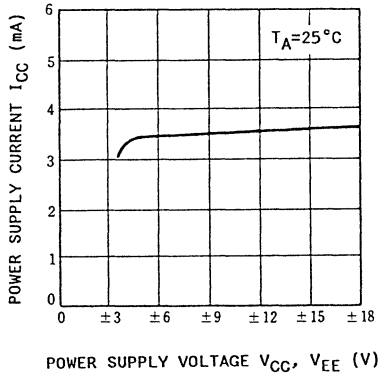
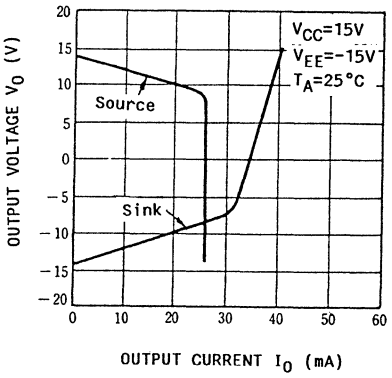
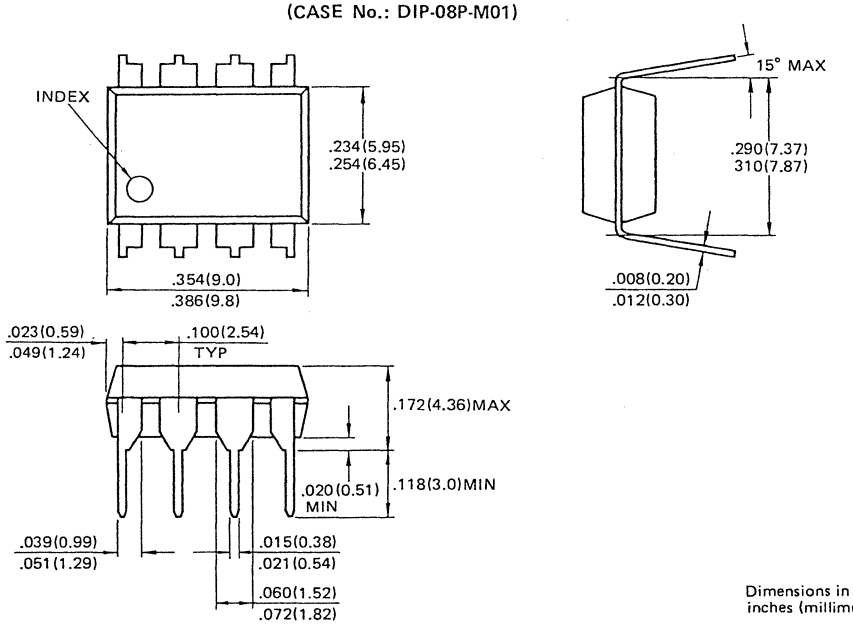


FIG.11 - OUTPUT VOLTAGE VS. OUTPUT CURRENT



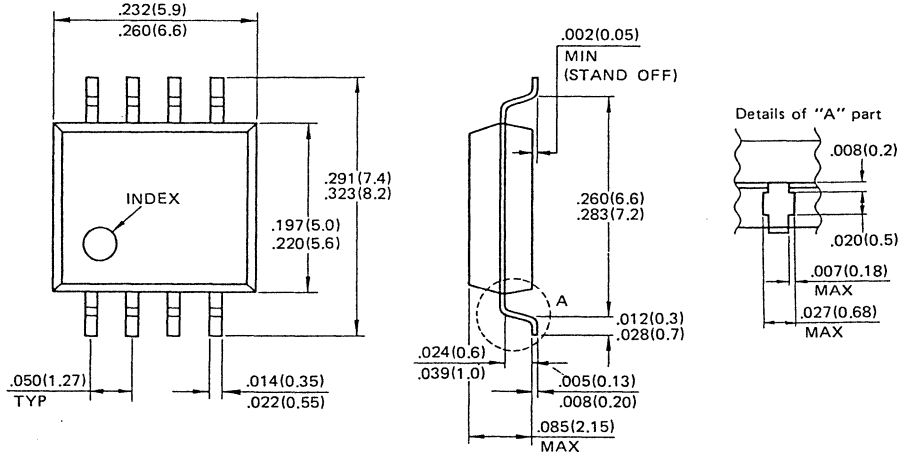
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

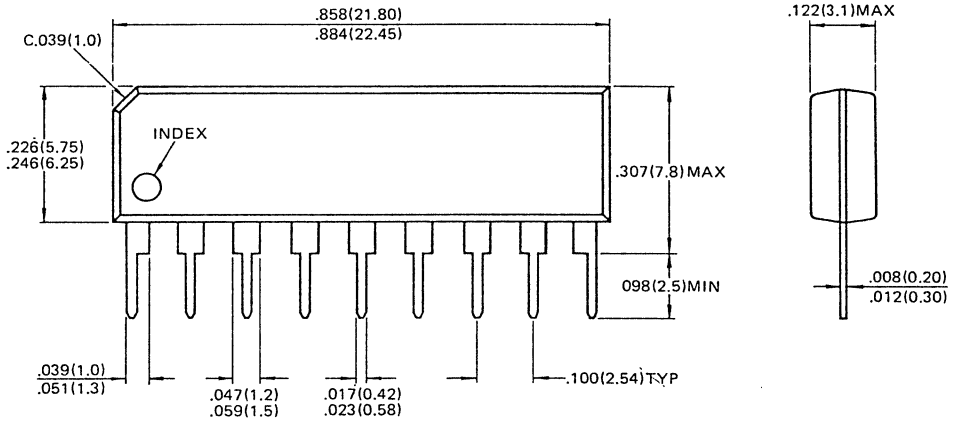
8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

9-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-09P-M01)



Dimensions in
inches (millimeters)

FUJITSU

DUAL OPERATIONAL AMPLIFIER

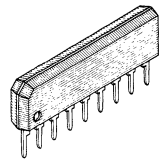
MB47358

July 1988
Edition 2.0

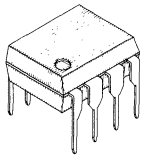
DUAL OPERATIONAL AMPLIFIER

The Fujitsu MB47358 is designed for a general purpose dual operational amplifier with internal frequency compensation and to operate from a single power supply or dual power supplies. The MB47358 is suitable for audio with the fast slew rate and with the reduction of cross-over distortion. The MB47358 fits an application of microcomputer because of its wide output voltage range. The MB47358 is compatible with LM358.

- Not required frequency compensation
- Wide power supply voltage range
  Single power supply: 3V to 30V
  Dual power supplies: ±1.5V to ±15V
- Wide output voltage range
- No cross-over distortion
- Fast slew rate – 2V/μs typ.



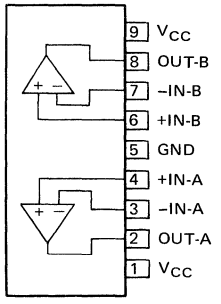
PLASTIC PACKAGE
SIP-09P-M01



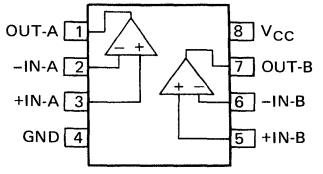
PLASTIC PACKAGE
DIP-08P-M01

FLAT PLASTIC PACKAGE See Page 7

PIN ASSIGNMENT
(FRONT VIEW: SIP)



(TOP VIEW: DIP, FPT)



ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_A = 25°C)

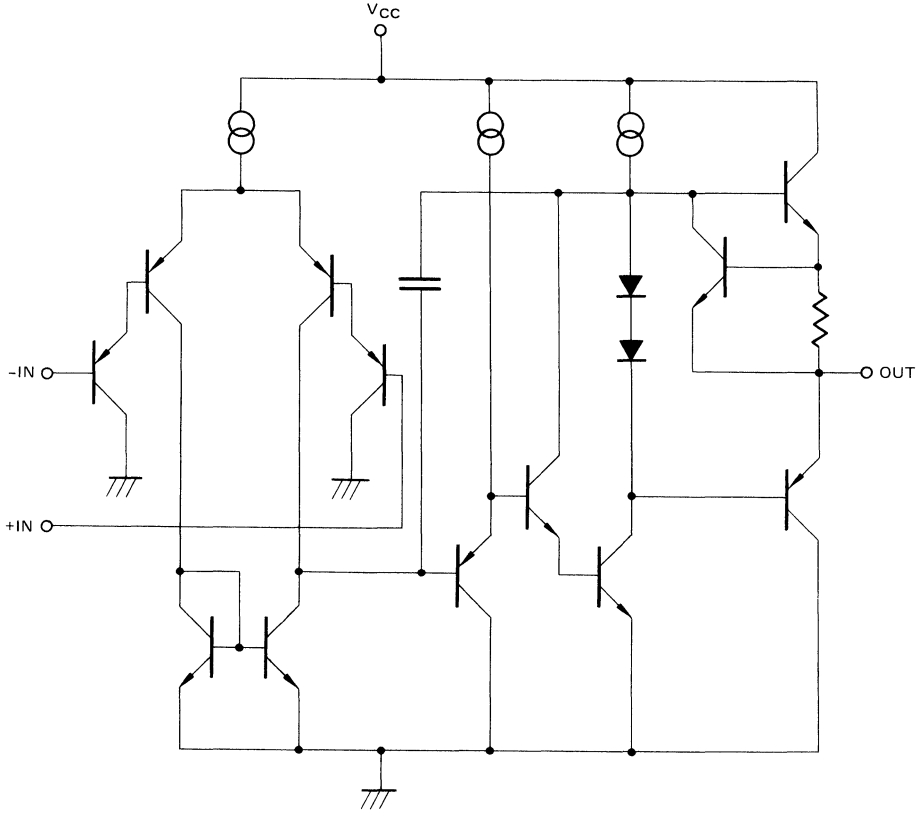
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	36	V
Differential Input Voltage	V_{ID}	36	V
Common-mode Input Voltage	V_{ICM}	-0.3 to +36	V
Power Dissipation	P_D	350 ($T_A \leq 55°C$)	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB47358 EQUIVALENT CIRCUIT



1 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	3 to 30	V
		±1.5 to ±15	
Operating Temperature	T_A	−20 to +75	°C

RECOMMENDED OPERATING CONDITIONS

(T_A = 25°C, V_{CC} = 5V)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}		–	2	7	mV
Input Offset Current	I_{IO}		–	5	50	nA
Input Bias Current	I_I *		–	45	250	nA
Power Supply Current	I_{CC}	$R_L = \infty$, $V_{CC} = 5V$	–	2.0	3.0	mA
Common-mode Input Voltage	V_{ICM}		0	–	V_{CC}−1.5	V
Voltage Gain	A_V	$R_L \geq K\ 2k\Omega$	25	100	–	V/mV
Common-mode Rejection Ratio	CMRR		65	85	–	dB
Power Supply Voltage Rejection Ratio	SVRR		65	100	–	dB
Output Voltage	V_{OH}	$R_L = 2k\Omega$	3.5	4.1	–	V
		$R_L = 10k\Omega$	4.0	4.2	–	V
	V_{OL}	$I_{SINK} \leq 60\mu A$	–	0.2	0.4	V
		$I_{SINK} \leq 2mA$	–	0.8	1.5	V
Maximum Output Voltage	V_{OM}	$R_L \geq 10k\Omega$, $V_{CC} = \pm 15V$	±12	±14	–	V
		$R_L = 2k\Omega$, $V_{CC} = \pm 15V$	±10	–	–	V
Output Current	I_{SOURCE}	$V_{IN+} = 1V$, $V_{IN-} = 0V$, $V_{CC} = 15V$	20	40	–	mA
	I_{SINK}	$V_{IN+} = 0V$, $V_{IN-} = 1V$, $V_{CC} = 15V$	10	20	–	mA
		$V_{IN+} = 0V$, $V_{IN-} = 1V$, $V_O = 0.4V$	60	150	–	μA
Channel Separation	CS	f = 1kHz	–	120	–	dB
Slew Rate	SR	$R_L = 2k\Omega$	–	2	–	V/μs

NOTE: A direction of the input blas current flows from IC because first input transistor consists of PNP.

ELECTRICAL CHARACTERISTICS CURVES

Fig. 2 – POWER SUPPLY VOLTAGE vs. POWER SUPPLY CURRENT

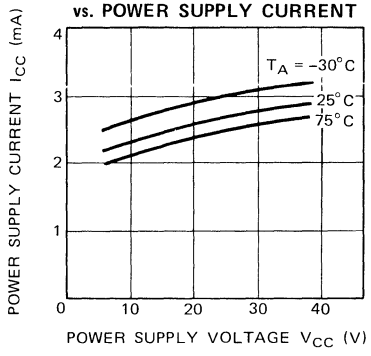


Fig. 3 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

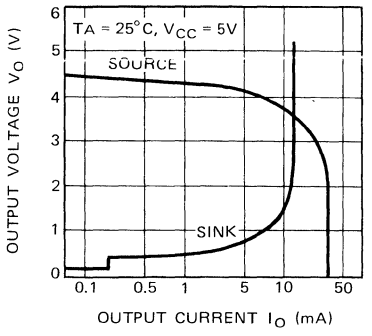


Fig. 4 – TEMPERATURE vs. INPUT BIAS CURRENT

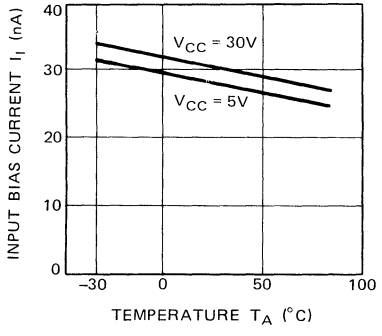


Fig. 5 – FREQUENCY vs. OUTPUT VOLTAGE

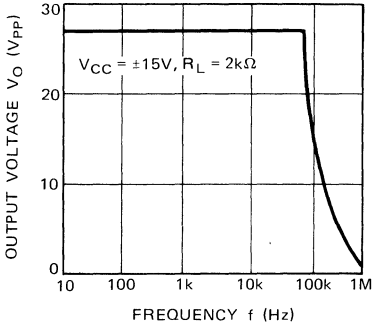
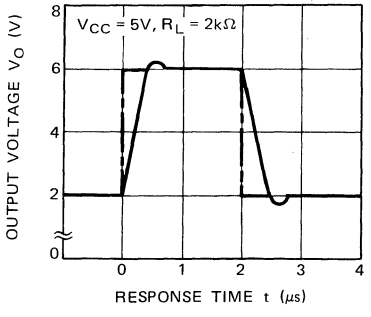
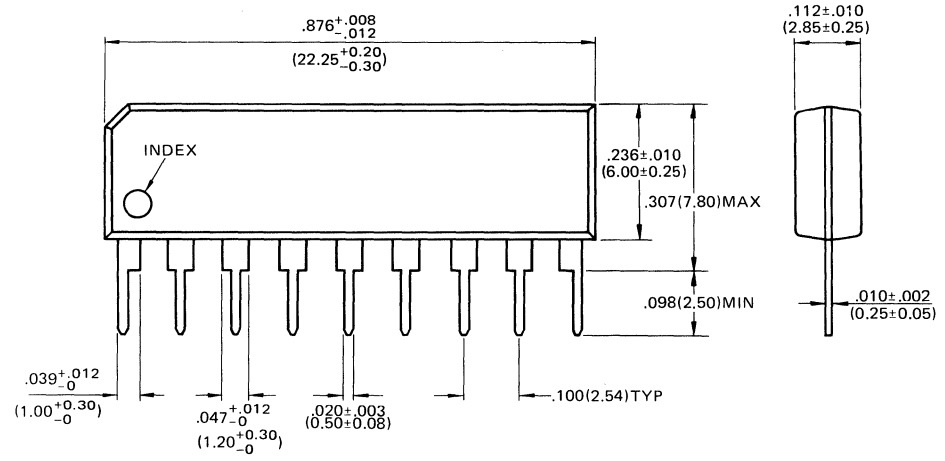


Fig. 6 – PULSE RESPONSE



1 PACKAGE DIMENSIONS

9-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-09P-M01)

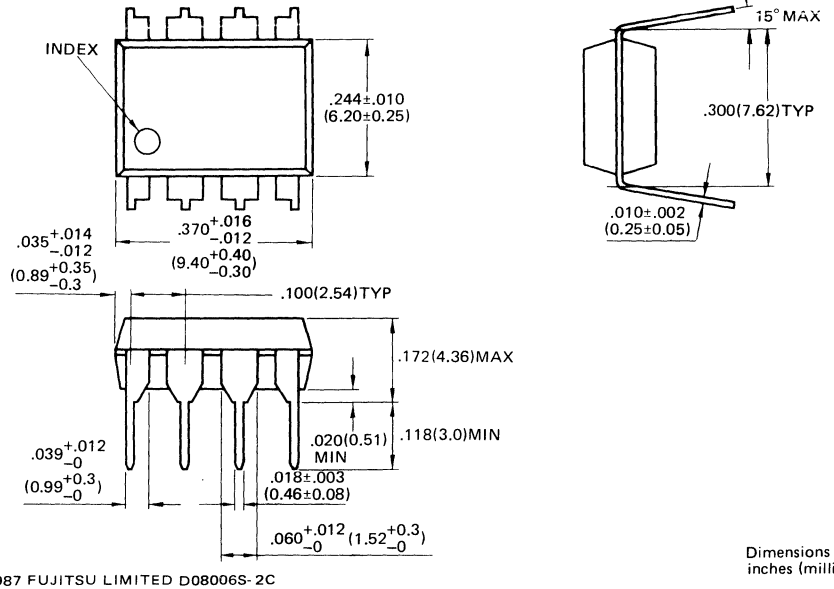


Dimensions in
inches (millimeters)

1

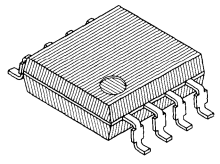
PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



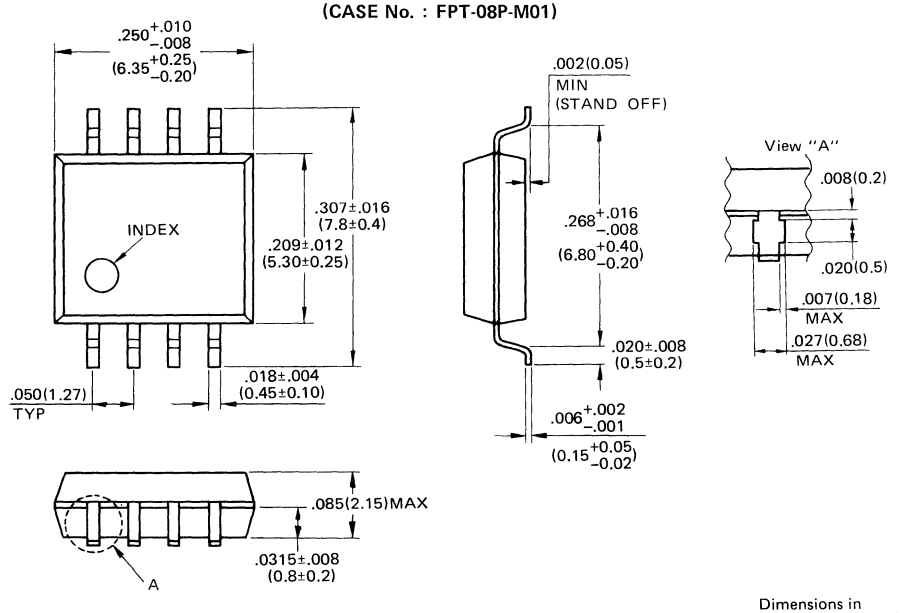
Dimensions in
inches (millimeters)

1



FPT-08P-M01

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in
inches (millimeters)

FUJITSU

LOW NOISE DUAL OPERATIONAL AMPLIFIER

MB47833

May 1988
Edition 1.0

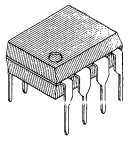
1

LOW NOISE DUAL OPERATIONAL AMPLIFIER

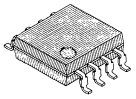
The Fujitsu MB47833 is a dual operational amplifier with a high slew rate, broad bandwidth and low noise characteristics.

The MB47833 is an excellent preamplifier for PCM and high-fidelity audio systems. The device is functionally compatible with the LM833.

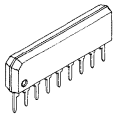
- Wide Power Supply Range: ±1.5V to ±15V
- High Slew Rate: 7 V/μs
- Low Input Noise Voltage: 4.5 nV/$\sqrt{Hz}$
- Wide Gain Bandwidth: 15 MHz
- Internal Phase Compensation



PLASTIC PACKAGE
DIP-08P-M01

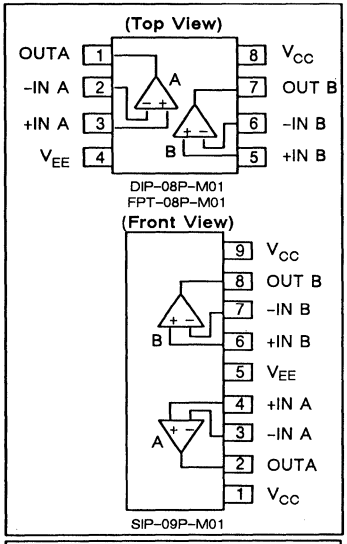


PLASTIC PACKAGE
FPT-08P-M01



PLASTIC PACKAGE
SIP-09P-M01

PIN ASSIGNMENTS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

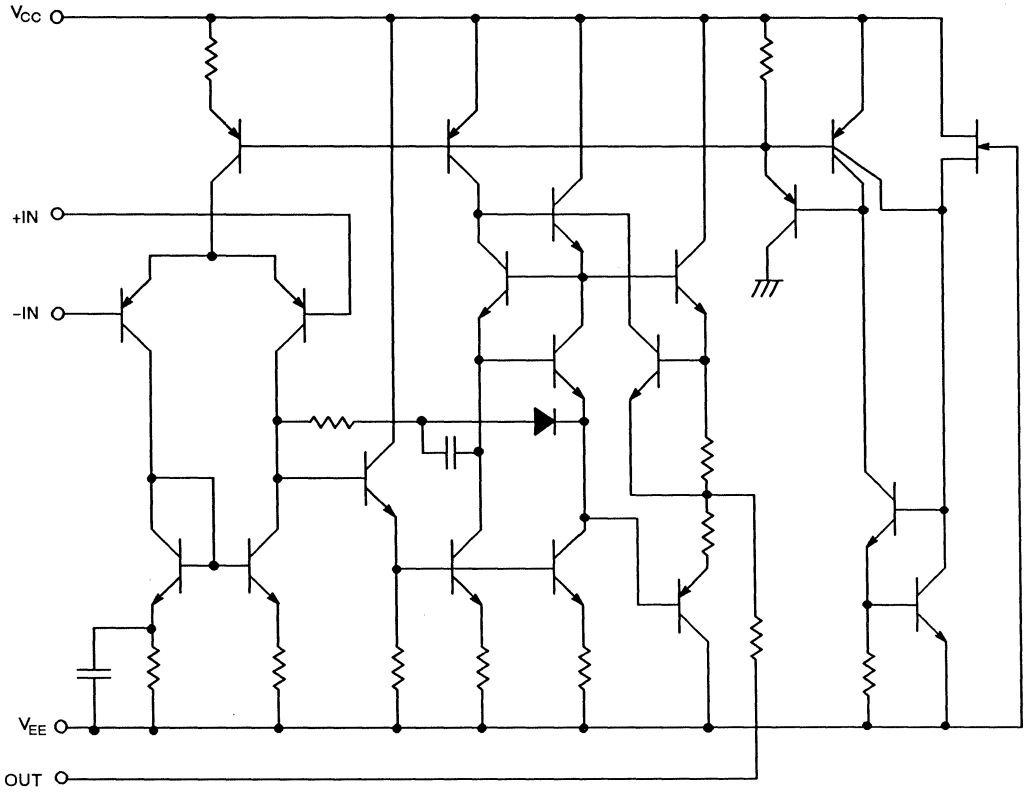
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	V
	V_{EE}	-18	V
Differential Input Voltage	V_{ID}	±30	V
Common Mode Input Voltage	V_I	±15	V
Power Dissipation	P_D	350 ($T_A \leq 55°C$)	mW
Operating Temperature	T_A	-30 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 — EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±1.5 to ±15	V
	V_{EE}		
Ambient Operating Temperature	T_A	-30 to +85	°C

ELECTRICAL CHARACTERISTICS

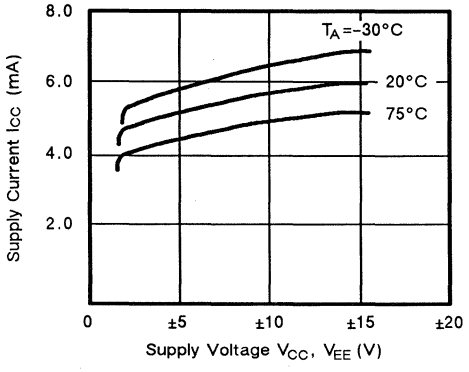
(V_{CC} = +15V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Value			Unit
			Minimum	Typical	Maximum	
Input Offset Voltage	V_{IO}			0.3	5.0	mV
Input Offset Current	I_{IO}			10	200	nA
Input Bias Current	I_{IN}			500	1000	nA
Common Mode Input Voltage	V_{CM}		±12	±14		V
Common Mode Rejection Ratio	CMR		80	100		dB
Supply Voltage Rejection Ratio	SVR		80	100		dB
Voltage Gain	A_V	R_L = 2kΩ	90	110		dB
Power Supply Current	I_{CC}			5.0	8.0	mA
Maximum Output Voltage	V_{OM}	$R_L \geq$ 10kΩ	±12	±13.5		V
		$R_L \geq$ 2kΩ	±10	±13.4		V
Gain Bandwidth Product	GBW	R_L = 2kΩ, f = 100kHz		15		MHz
Slew Rate	SR	R_L = 2kΩ, C = 100pF A_V = 1		7		V/μS
Channel Separation	CS	f = 1kHz		120		dB
Input Noise Voltage	V_{NI}	NAB, JISA RS = 600Ω, f = 1kHz		0.4		μV

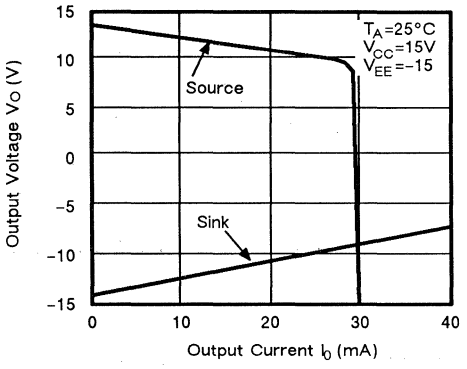
1

TYPICAL PERFORMANCE CHARACTERISTICS

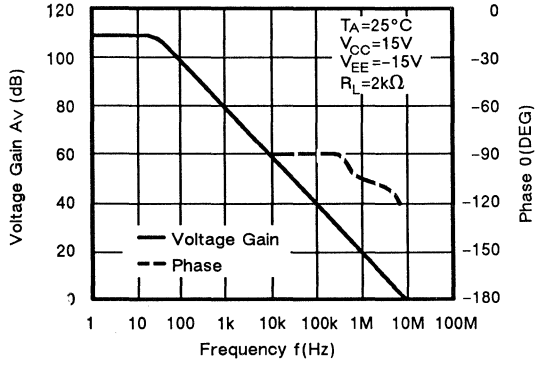
Supply Current vs Supply Voltage



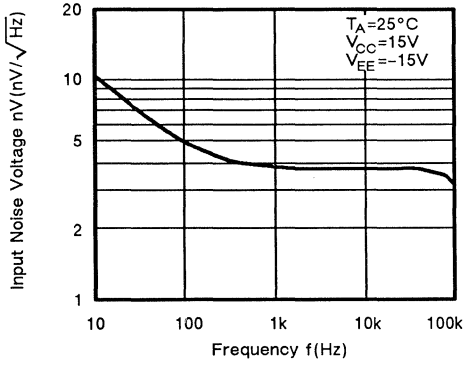
Output Voltage vs Output Current



Voltage Gain vs Frequency



Input Noise Voltage vs Frequency



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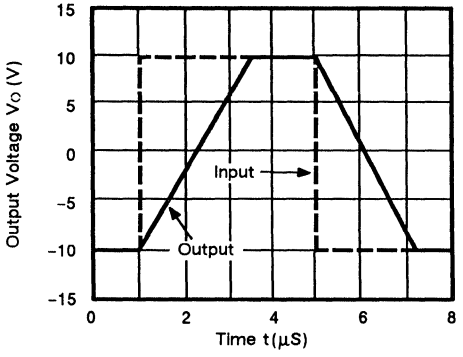
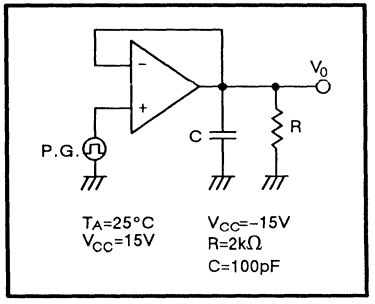
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Pulse Response Characteristics



Pulse Response vs Measurement Circuit



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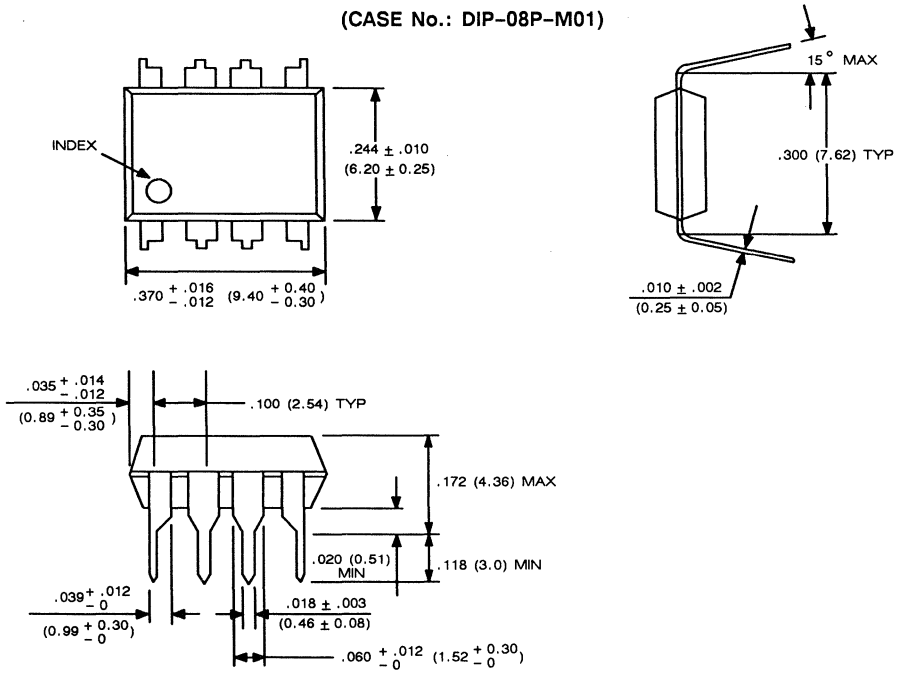
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in
inches (millimeters)

D08006S-2C

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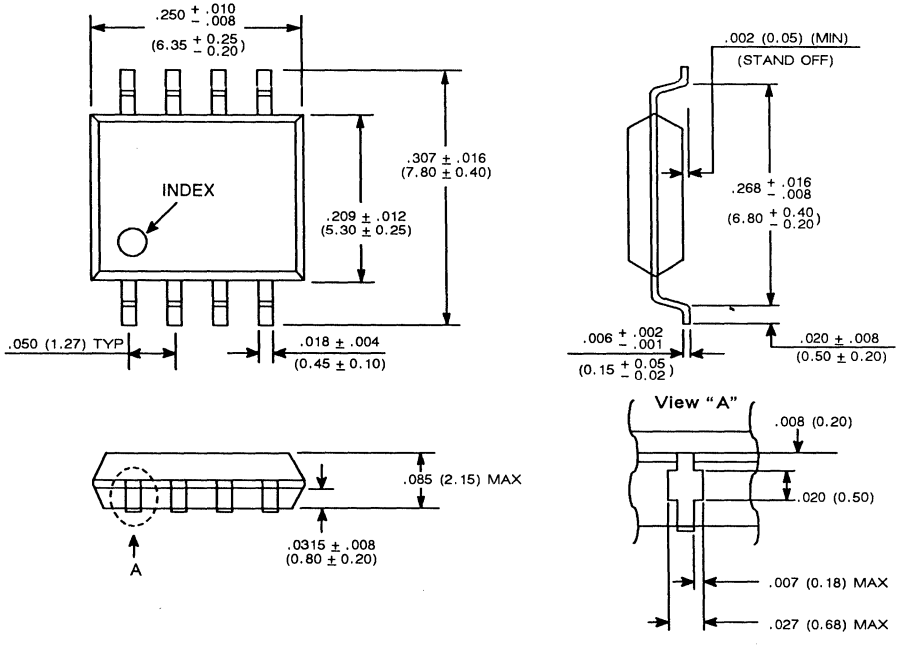
PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
inches (millimeters)

F08002S-2C

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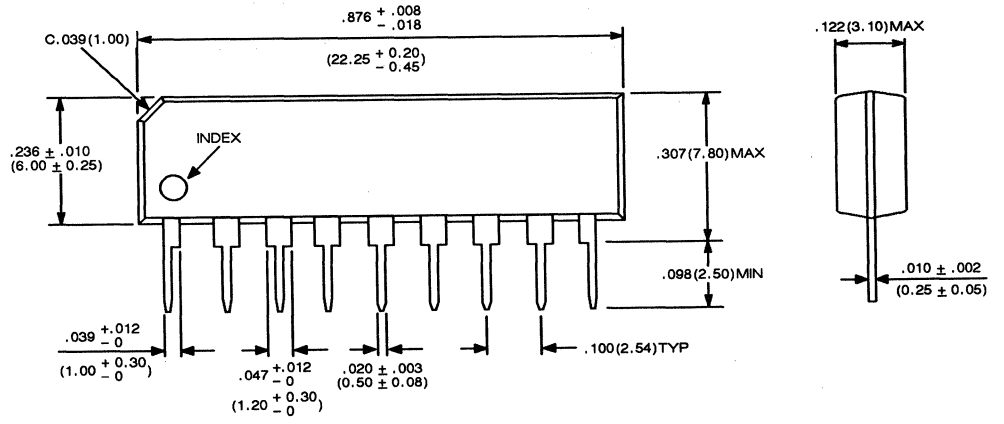
PACKAGE DIMENSIONS (continued)

9-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-09P-M01)



Dimensions in
inches (millimeters)

S09002S-2C

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Printed in USA OV0046-885F1

Section 2

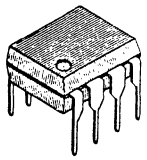
Comparators

Fujitsu Part No.	Description	Features	Equiv. Prod.	Power Supply (V)	Package	No. of Pins
MB4001	Single	High Speed (t_{PD} = 50ns) V_{RO} = 2mV	µA710	±12, -6	Plastic DIP Plastic Flatpak	8 8
MB4002	Single	High Speed (t_{PD} = 25ns) V_{RO} = 1mV	—	±12, -6	Plastic DIP Plastic Flatpak	8 8
MB4204	Quad	Low Power (I_{CC} = 0.8mA),	LM339	+2, ~ +36	Plastic DIP Plastic Flatpak	14 14
MB4205	Single	High Power I_{OL} = 0.5mA with Over Current Limit	—	+6.5 ~ +18	SIP (Heatsink)	8

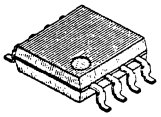
HIGH SPEED COMPARATOR

TS504-B87X
October 1987

The Fujitsu MB4001 is a Monolithic High Speed Comparator. Its single-end output circuit is low impedance and input offset voltage is small, besides the device operation is stable against temperature variation. MB4001 is compatible with μA710.



PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

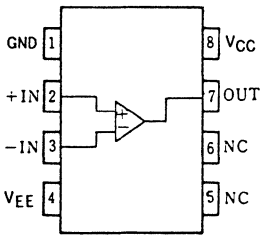
- High Speed --- 50 ns typ.
- Small Input offset voltage
- Low output impedance
- Package

  Plastic 8-pin Dual-In-Line (Suffix: -P)

  Plastic 8-pin FLAT Package (Suffix: -PF)

PIN ASSIGNMENT

(TOP VIEW)



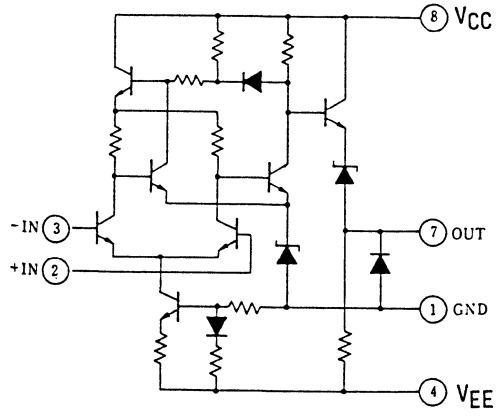
ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A=25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+14	V
Power Supply Voltage	V_{EE}	-7	V
Input Voltage	V_I	±7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Operating Temperature	T_A	-20 to +75	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB4001 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+12V±5%	V
Power Supply Voltage	V_{EE}	-6V±5%	V
Operating Temperature	T_A	-20 to +75	°C

ELECTRICAL CHARACTERISTICS (T_A=25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 200\Omega$, V_O=1.4V		2	5	mV
Input Offset Current	I_{IO}	V_O=1.4V		1		μA
Input Bias Current	I_I	V_O=1.4V		10		μA
Voltage Gain	A_V	f=1kHz, output pin is open	600	1500		
Propagation Delay Time	t_{pd}	V_I=5mV, over driven		50		ns
High-level Output Voltage	V_{OH}	$\Delta V_I \geq 10mV$, I_{IB}=40μA	2.5	3.2		V
Low-level Output Voltage	V_{OL}	$\Delta V_I \geq 10mV$, I_{OL}=1.6μA		-0.5	0.37	V
Power Supply Current	I_{CC}	V_O=1.4V		6		mA
Power Supply Current	I_{EE}	V_O=1.4 V		5		mA

TYPICAL CHARACTERISTICS CURVES

Fig.2 - OUTPUT VOLTAGE vs. INPUT VOLTAGE

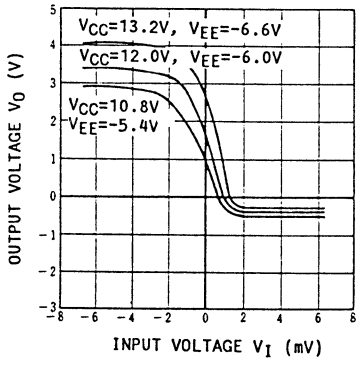


Fig.3 - PULSE RESPONSE

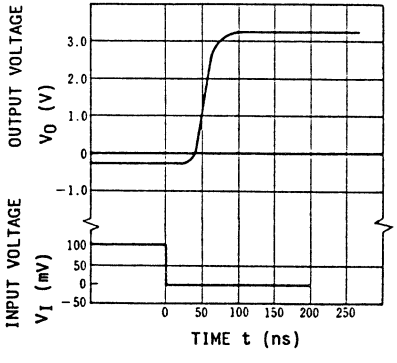
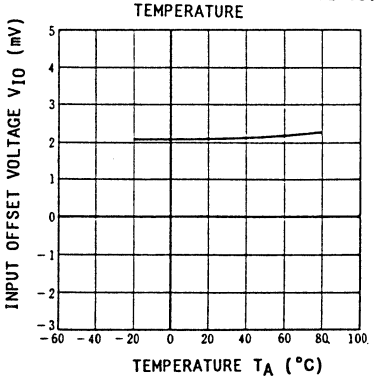
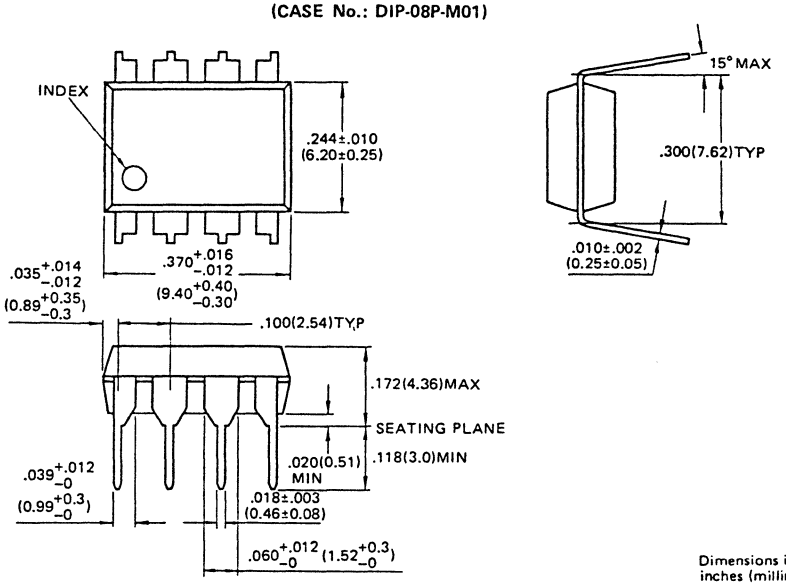


Fig.4 - INPUT OFFSET VOLTAGE vs. TEMPERATURE



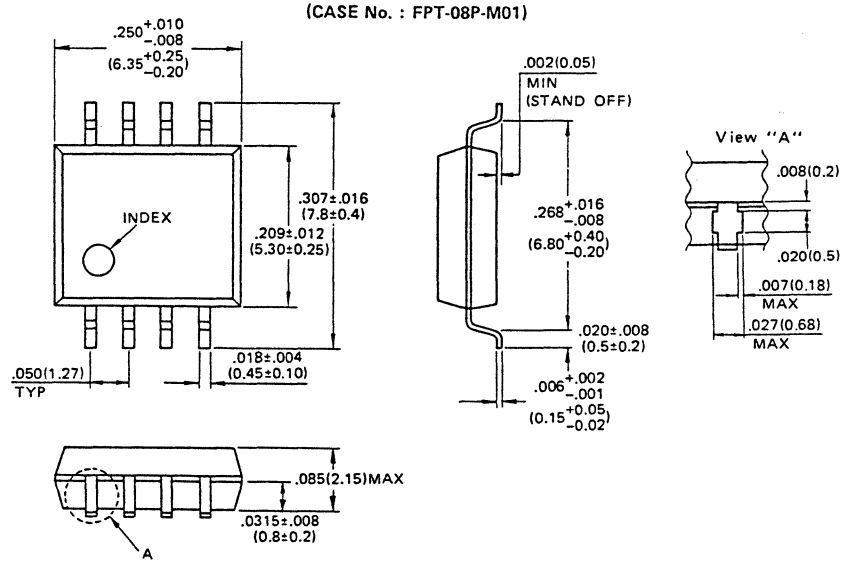
2

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches (millimeters)

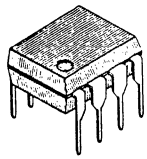
FUJITSU

MB4002

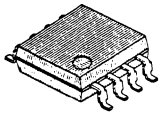
HIGH SPEED COMPARATOR

TS505-B87X
October 1987

The Fujitsu MB4002 is a Unsaturated High Speed Comparator. Its output level is stable against power supply voltage and temperature variation.



PLASTIC PACKAGE
DIP-08P-M01



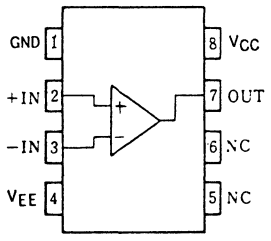
PLASTIC PACKAGE
FPT-08P-M01

- High Speed --- 25 ns typ.
- Small Input Offset Voltage
- Package

  Plastic 8-pin DIP Package (Suffix: -P)

  Plastic 8-pin FLAT Package (Suffix: -PF)

PIN ASSIGNMENT
(Top View)



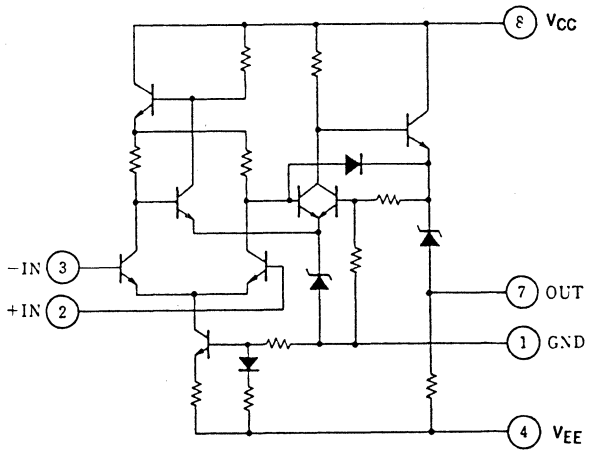
ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A=25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+14	V
Power Supply Voltage	V_{EE}	-7	V
Input Voltage	V_I	±7	V
Operating Temperature	T_A	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB4002 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+12±5%	V
Power Supply Voltage	V_{EE}	-6±5%	V
Operating Temperature	T_A	-20 to +75	°C

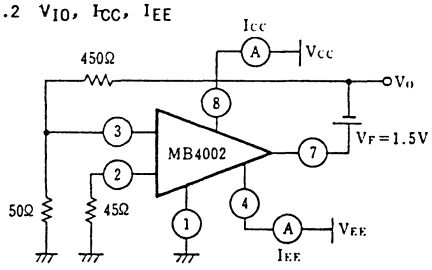
ELECTRICAL CHARACTERISTICS (V_{CC}=12V, V_{EE}=-6V, T_A=25±2°C)

Parameter	Symbol	Condition	Test Circuit	Value			Unit
				Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S≤200Ω, V_O=1.5V	Fig.2		1	5	mV
Input Offset Current	I_{IO}	V_O=1.5V	Fig.3		1	5	μA
Input Bias Current	I_I	V_O=1.5V	Fig.4		10	40	μA
Voltage Gain	A_V	f=1kHz, output pin is open	Fig.5	800	1500		
Propagation Delay Time	t_{pd}	V_I=100mV, 5mV Over Drive	Fig.7		25		ns
High-level Output Voltage	V_{OH}	ΔV_I≥10mV, I_{OH}=40μA	Fig.6	2.8	3.2	3.6	V
Low-level Output Voltage	V_{OL}	ΔV_I≥10mV, I_{OL}=2.0mA	Fig.6	-0.2	0	0.37	V
Power Supply Current	I_{CC}	V_O=1.5V	Fig.2		10.6	13.5	mA
Power Supply Current	I_{EE}	V_O=1.5V	Fig.2		6.8	8.5	mA

2

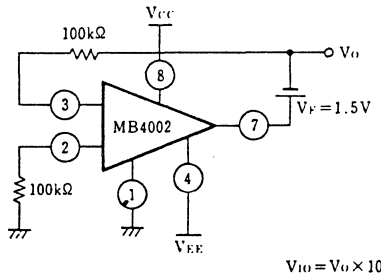
TEST CIRCUIT

Fig.2 V_{IO}, I_{CC}, I_{EE}



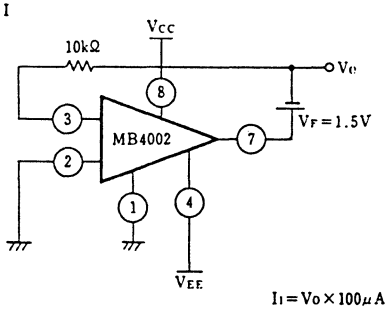
$V_{IO}=V_O\times10^{-1}$mV

Fig.3 I_{IO}



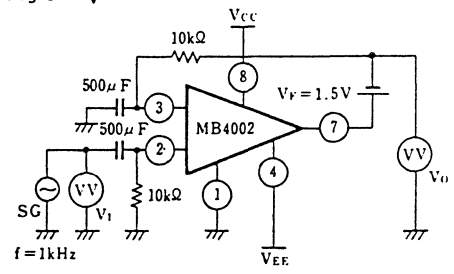
$V_{IO}=V_O\times10\mu A$

Fig.4 I_I



$I_I=V_O\times100\mu A$

Fig.5 A_V



$A_V=V_O/V_I$ V_I=0.5mV

TEST CIRCUIT

Fig.6 V_{OH}, V_{OL}

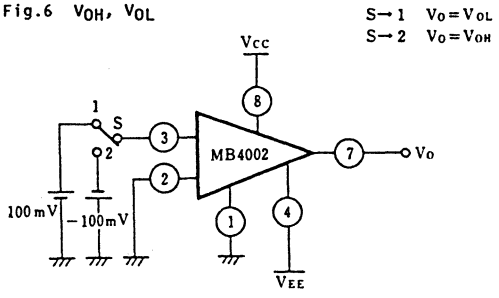
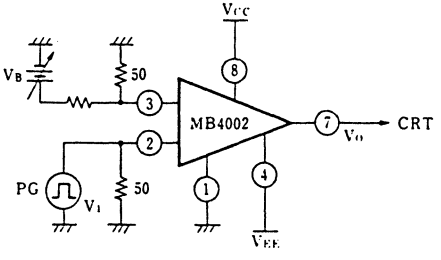
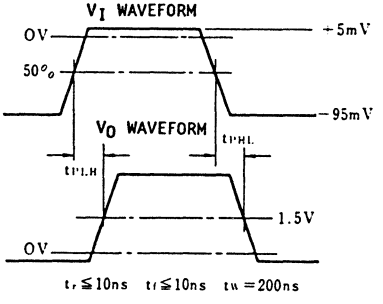


Fig.7 t_{pd}





TYPICAL CHARACTERISTICS CURVES

Fig.8 - INPUT PROPAGATION CHARACTERISTICS

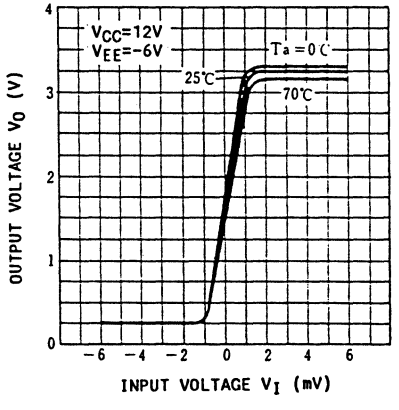


Fig.9 - VOLTAGE GAIN vs. TEMPERATURE

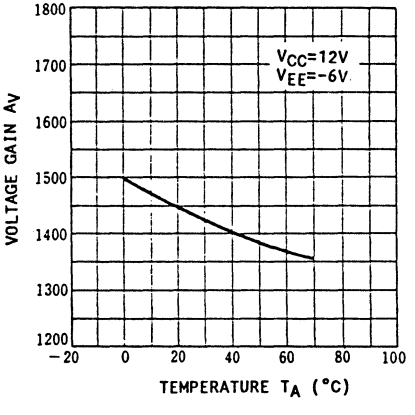


Fig.10 - INPUT BIAS CURRENT vs. TEMPERATURE

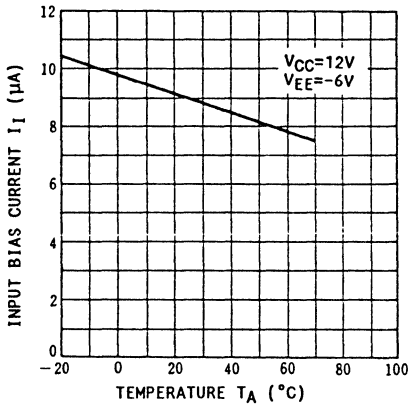


Fig.11 - INPUT OFFSET CURRENT vs. TEMPERATURE

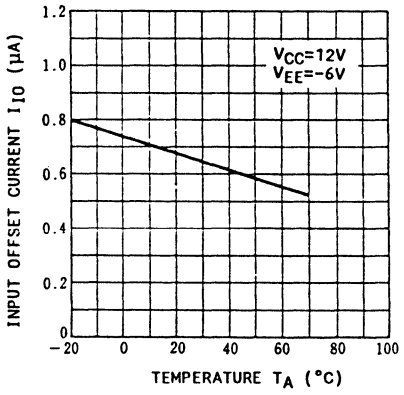


Fig.12 - OUTPUT SINK CURRENT vs. TEMPERATURE

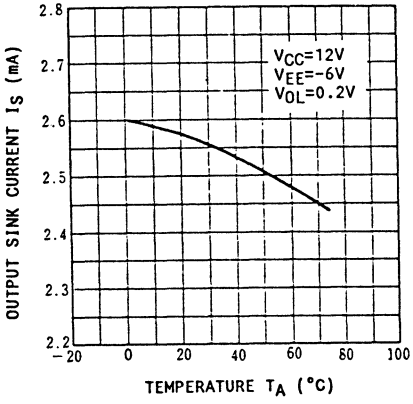


Fig.13 - OUTPUT VOLTAGE vs. TEMPERATURE

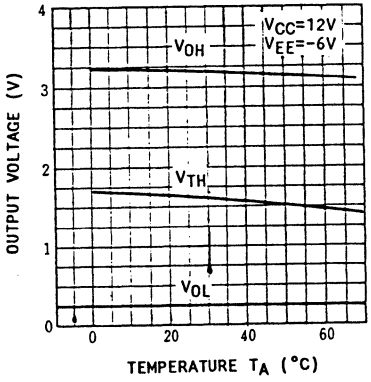


Fig.14 - OUTPUT VOLTAGE vs. POWER SUPPLY VOLTAGE

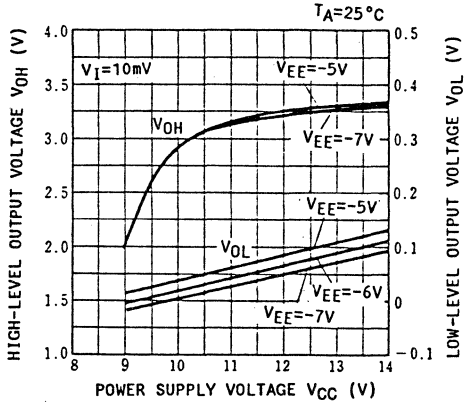


Fig.15 - SWITCHING RESPONSE (1)

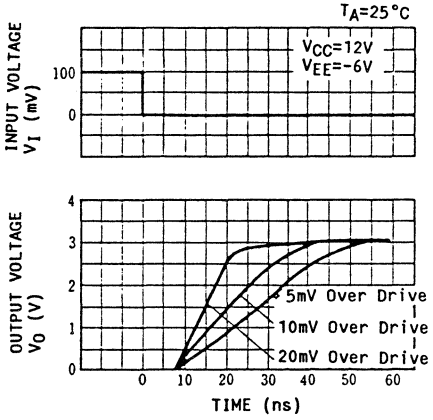


Fig.16 - SWITCHING RESPONSE (2)

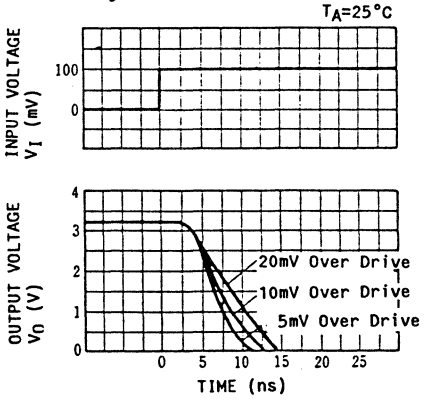
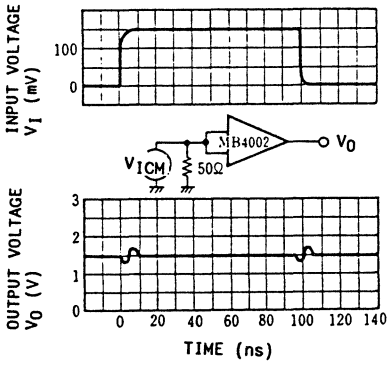
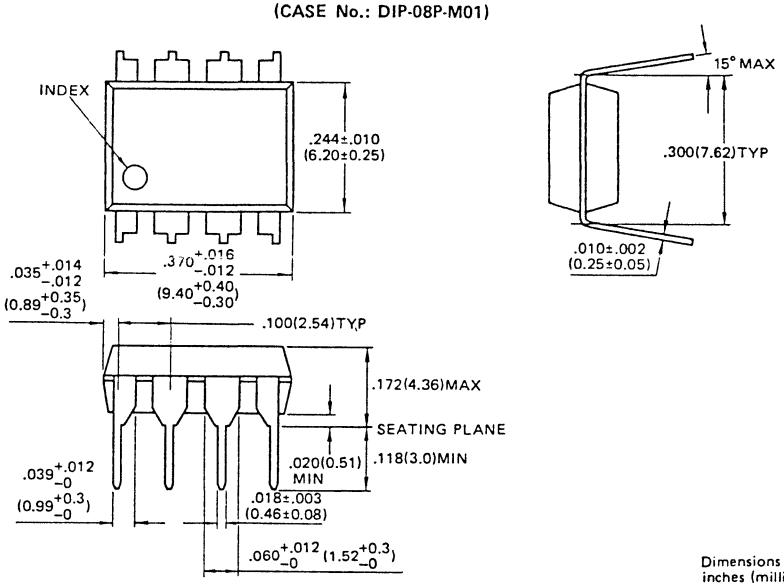


Fig.17 - COMMON MODE INPUT PULSE CHARACTERISTICS

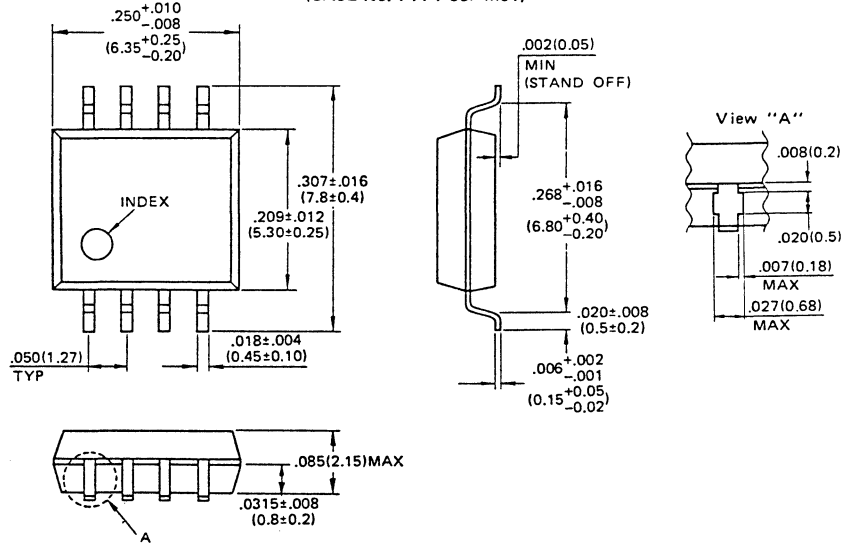


8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches (millimeters)

May 1988
Edition 1.0

2

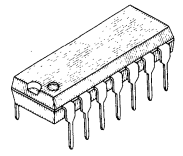
QUAD COMPARATOR

The Fujitsu MB4204 is a Quad Comparator which consists of four independent channels. The MB4204 is designed to operate form either a single power or dual power supplies over a wide range of voltages. The input characteristics is equivalent of current industry standard comparator. Even though operated from a single power supply, the MB4204 is suitably designed to compare multiple signals in parallel and to be operated with battery because its input common mode voltage range includes ground potential and it requires low power supply current.

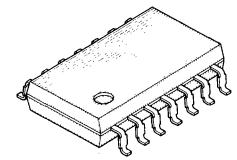
The MB4204 can be high density mounted because it integrates 4 circuits on a chip in DIP/FPT-14-pin package.

The MB4204 is pin compatible with National Semiconductor LM339.

- Wide power supply voltage range: +2 to +36V
- Wide input common mode range: 0 to (Vcc-1.5) V
- Low power supply current: 0.8 mA typ.
- Low input offset voltage: 2mV typ.
- Low input bias current: 25nA typ.
- Open Collectors Output allow to wired-OR Connection
- Package
  - — 14-pin Plastic DIP Package (Suffix: -P)
  - — 14-pin Plastic FPT Package (Suffix: -PF)

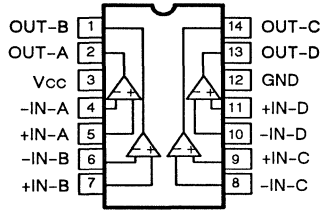


PLASTIC PACKAGE
DIP-14P-M02



PLASTIC PACKAGE
FPT-14P-M01

PIN ASSIGNMENT



(TOP VIEW)

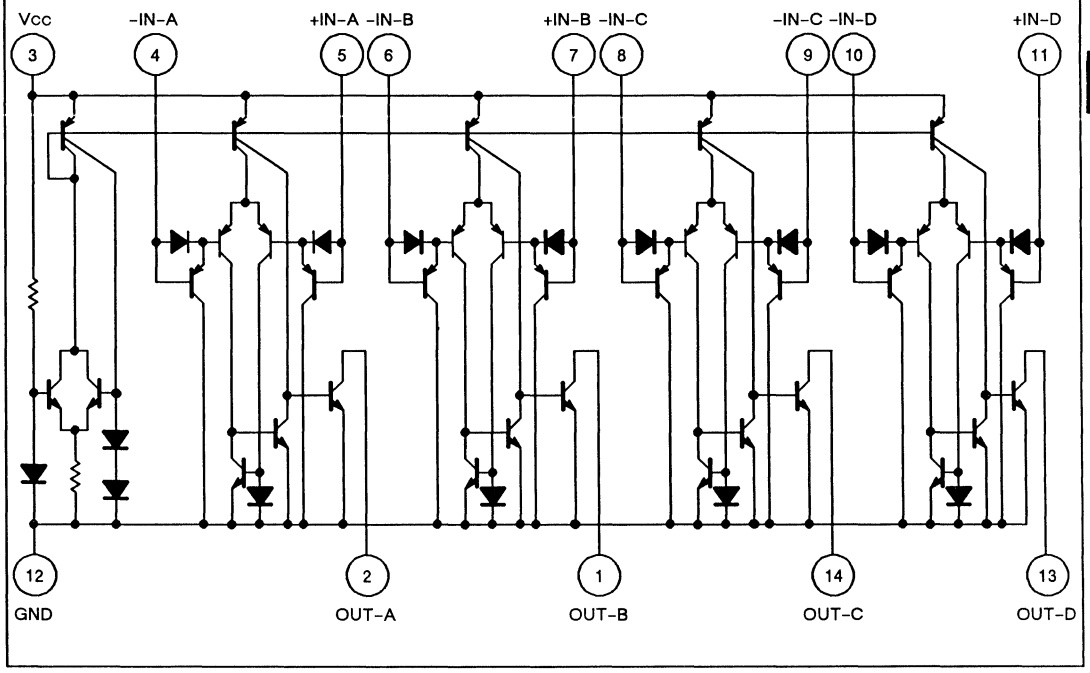
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	Vcc	36	V
Power Dissipation	PD	500	mW
Differential Input Voltage	VID	36	V
Common Mode Input Voltage	VI	-0.3 to +36	V
Output Short Circuit Duration		Infinite	
Operating Temperature	TA	-20 to +75	°C
Storage Temperature	TSTG	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 2 — EQUIVALENT CIRCUIT



2

ELECTRICAL CHARACTERISTICS (V_{CC}=+5V, T_A=25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_O = V_{REF} = 1.4V		2	5	mV
Input Offset Current	I_{IO}			5	50	nA
Input Bias Current	I_I *1			25	250	nA
Input Common Mode Voltage	V_{CM}		0		V_{CC} -1.5	V
Voltage Gain	A_V	R_L=15kΩ		200		V/mV
Transconductance				13		mhos
Large Signal Response Time	*2	R_L=5.1kΩ, V_{RL}=5V		300		ns
Response Time	*3	R_L=5.1kΩ, V_{RL}=5V		1.3		µs
Output Saturation Voltage	V_{OL}	V_{IN-}=1V, V_{IN+}= 0V, I_{SINK}=3 mA		250	400	mV
Output Sink Current	I_{SINK}	V_{IN-} =1V, V_{IN+}=0V, $V_O \leq 1.5V$	6	16		mA
Output Leakage Current	I_{LEAK}	V_{IN+}=1V, V_{IN-}=0V, V_O=5V		0.1		nA
Output Leakage Current	I_{LEAK}	V_{IN+}=1V, V_{IN-}=0V, V_O=30V			1	µA
Power Supply Current	I_{CC}	R_L=∞		0.8	2	mA

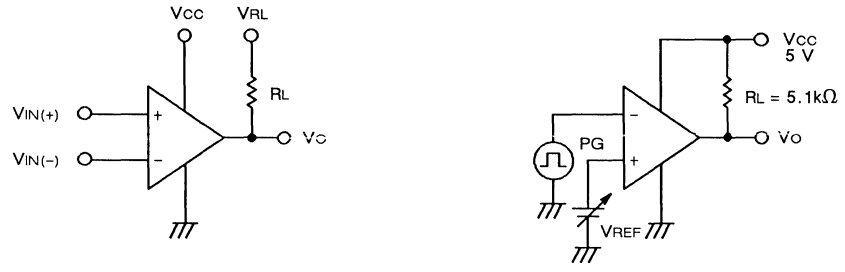
Notes:

*1 The direction of the input bias current flows from IC.

*2 V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V

*3 V_{IN} = 100 mV, Overdrive = 5 mV

Fig. 3 — TEST CIRCUIT



2

TYPICAL CHARACTERISTICS CURVES

Fig. 4 - Power Supply Current vs. Power Supply Voltage

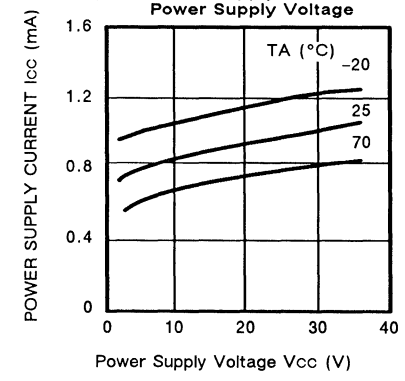


Fig. 5 - Output Saturation Voltage vs. Output Sink Current

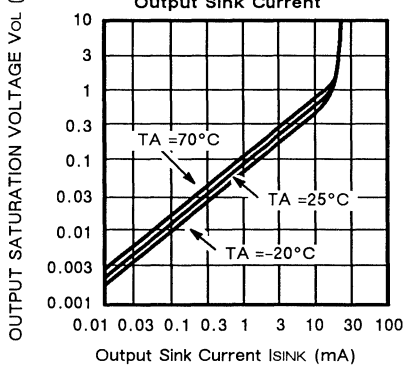


Fig. 6 - Input/Output Voltage vs. Time

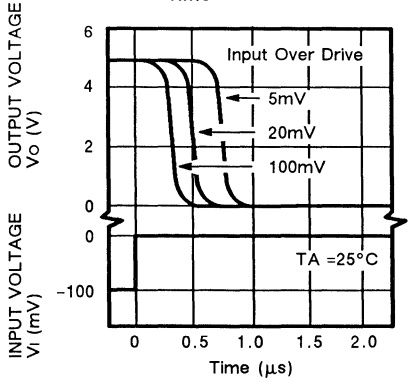
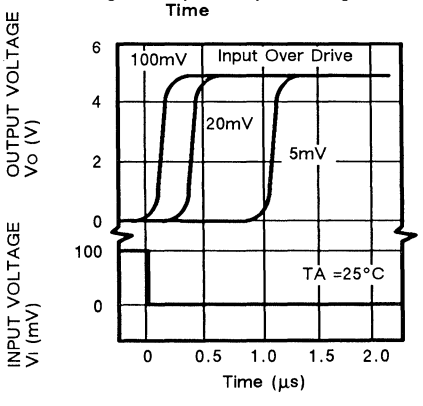


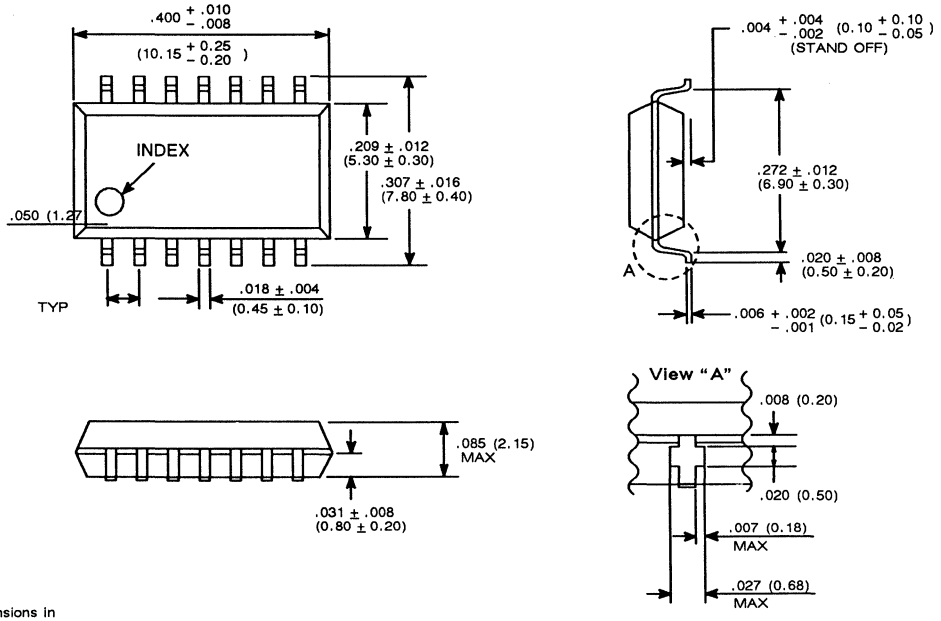
Fig. 7 - Input/Output Voltage vs. Time



PACKAGE DIMENSIONS

2

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)

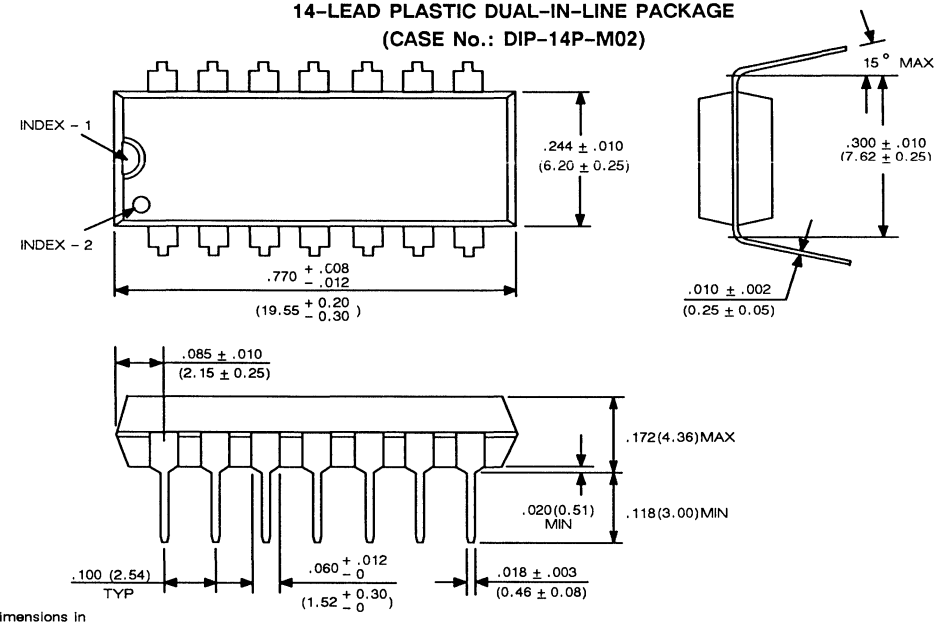


Dimensions in
inches (millimeters)

F14003S-2C

PACKAGE DIMENSIONS (Continued)

14-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)



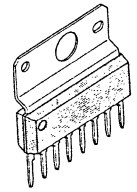
Dimensions in
inches (millimeters)

D14010S-3C

HIGH POWER COMPARATOR

2

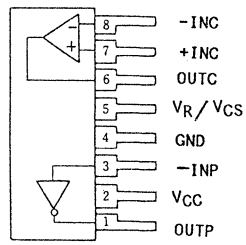
The Fujitsu MB4205 is a comparator which is designed to operate from a single power supply voltage. It is capable of driving a load up to 0.5 A and have the current limiting circuitry, it enables a direct drive warning lamps.
As it is packaged in 8-pin plastic SIP package with heat sink, it enables easy mounting.
It is equipped with the function which turns the output "ON" by force, when the surge is inflicted in the application of automobile, and so on.



PLASTIC PACKAGE
SIP-08P-M01

- PNP transistor input enables input control voltage from 0 V and a single power supply voltage operation
- High output drive capability : 0.5 A
- Resistance comparion is achieved due to on-chip switchable constant-current supply souce (Several hundred Ω to several kilo Ω)
- Hysteresis is set easily because V_{OH} level and V_R level is almost same
- On-chip current limiting circuitry
- Common pin for input control voltage pin V_{CS} and reference voltage output pin V_R

PIN ASSIGNMENT



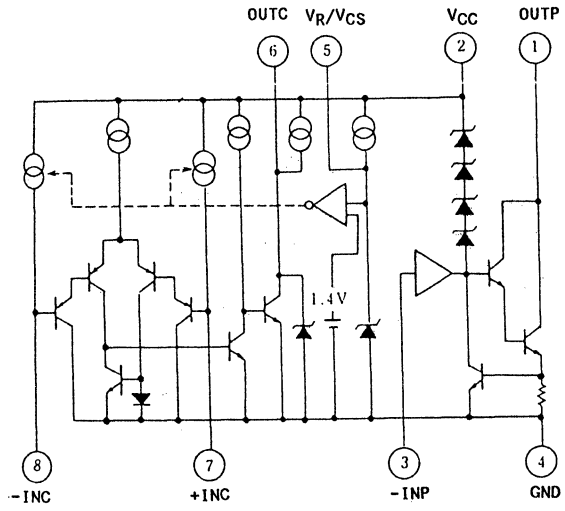
ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A=25°C)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}		18	V
Power Supply Current (Surge)	I_{CCS}	t≤50ms	100	mA
Load Current	I_{OL}		500	mA
Output Voltage	V_{OH}		40	V
Power Dissipation	P_D	T_A≤85°C	1	W
		T_C≤85°C	4	W
Operating Temperature	T_A		-30 to +85	°C
Storage Temperature	T_{STG}		-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB4205 EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS

(T_A=25°C, V_{CC}=13.2V, R_S=220Ω, R_L=54Ω)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{CC}	R_S=0	6.5		18	V
Power Supply Current	I_{CC}	V_{CC}=10V, R_S=0		9	13	mA
Zener Voltage	V_{CCZ}	I_{CC}=50mA	26	30	36	V

2

Comparator section

Input Offset Voltage	V_{IO}	V_{CS}=2.0V		2	10	mV
		V_{CS}=0.8V		5	20	mV
* Input Bias Current	I_I	V_{CS}=2.0V		0.5	3	μA
	I_{IB}	V_{CS}=0.8V	0.6	1.0	1.5	mA
Input Bias Current Ratio	I_{I+}/I_{I-}	V_{CS}=0.8V	0.95	1.0	1.05	
Common-mode Input Voltage Range	V_{CM}		0		V_{CC}-2	V
Output Voltage	V_{OL}	I_{SINK}=3mA		0.1	0.2	V
	V_{OH}	I_R=0.5mA	5.0	5.4	5.8	V
Sink Current	I_{SINK}	V_{OL}≤1V	8	20		mA

Output section

Reference Voltage	V_R	R_L=100kΩ	5.0	5.4	5.8	V
Input Control Current	I_{CS}	V_{CS}=0.8V	0.5	1.0	1.8	mA
Input Bias Current	I_I	V_I=0		3	20	μA
		V_I=5.0V			1	μA
Output Voltage	V_{OL}	V_{IH}=2.0V, I_{OL}=0.2A		0.85	1.0	V
Output Current	I_{OH}	V_{IL}=0.8V, I_{IH}=40V		2	5	mA

Note: Input bias current flows from the IC.

ELECTRICAL CHARACTERISTICS CURVES

FIG.2 - POWER SUPPLY CURRENT VS. POWER SUPPLY VOLTAGE

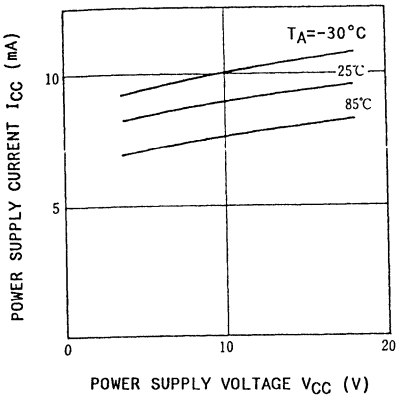


FIG.3 - INPUT BIAS CURRENT VS. POWER SUPPLY VOLTAGE

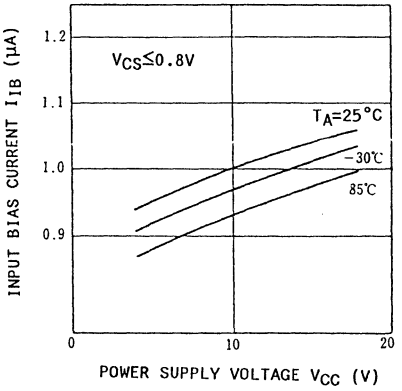


FIG.4 - REFERENCE VLTAGE/OUTPUT VOLTAGE VS. TEMPERATURE

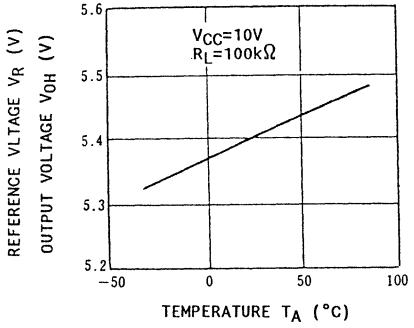


FIG.5 - REFERENCE VOLTAGE VS. LOAD CURRENT
INPUT CONTROL VOLTAGE VS. INPUT CONTROL CURRENT

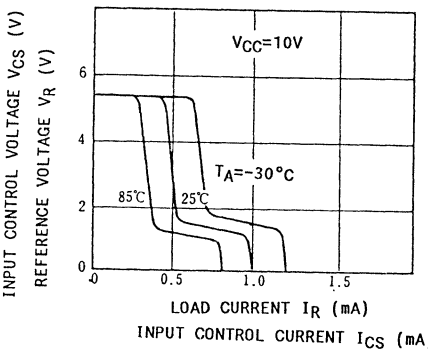


FIG.6 - OUTPUT VOLTAGE VS. INPUT VOLTAGE

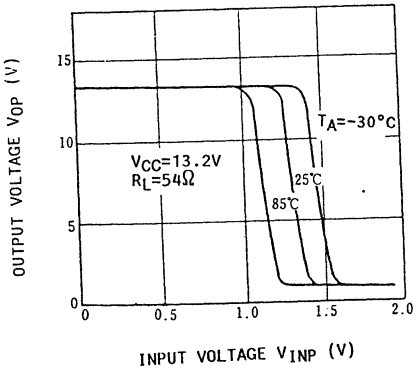


FIG.7 - OUTPUT VOLTAGE VS. OUTPUT CURRENT

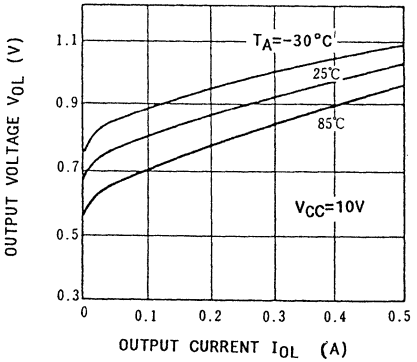


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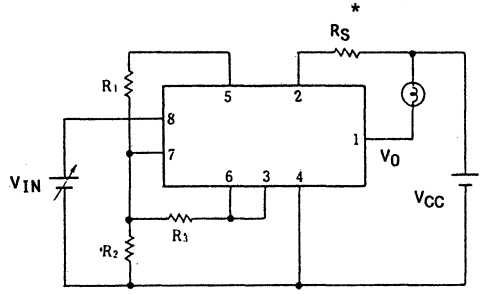
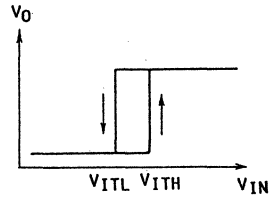
FIG.8



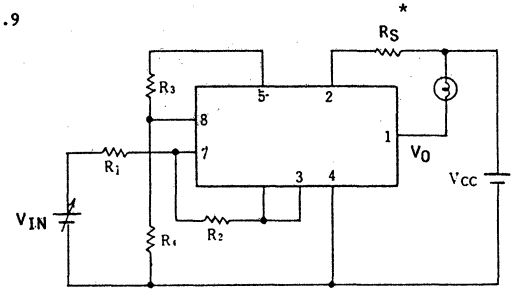
* R_S is not required if surge is not large.

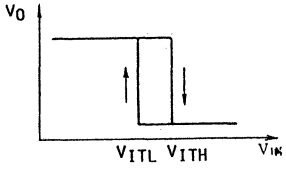


$$V_{ITH} \fallingdotseq \frac{R_2(R_1+R_3)}{R_2(R_1+R_3)+R_1R_3} V_R$$

$$V_{ITL} \fallingdotseq \frac{R_2R_3}{R_2(R_1+R_3)+R_1R_3} V_R$$

FIG.9

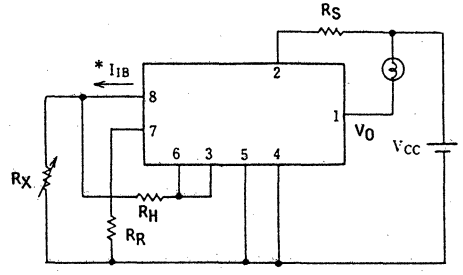




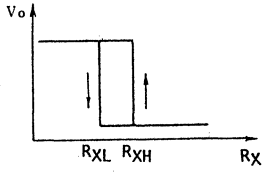
$$V_{ITH} = \left(1 + \frac{R_1}{R_2}\right)\left(\frac{R_4}{R_3+R_4}\right) V_R$$

$$V_{ITL} = V_{ITH} - \frac{R_1}{R_2} V_R$$

FIG.10



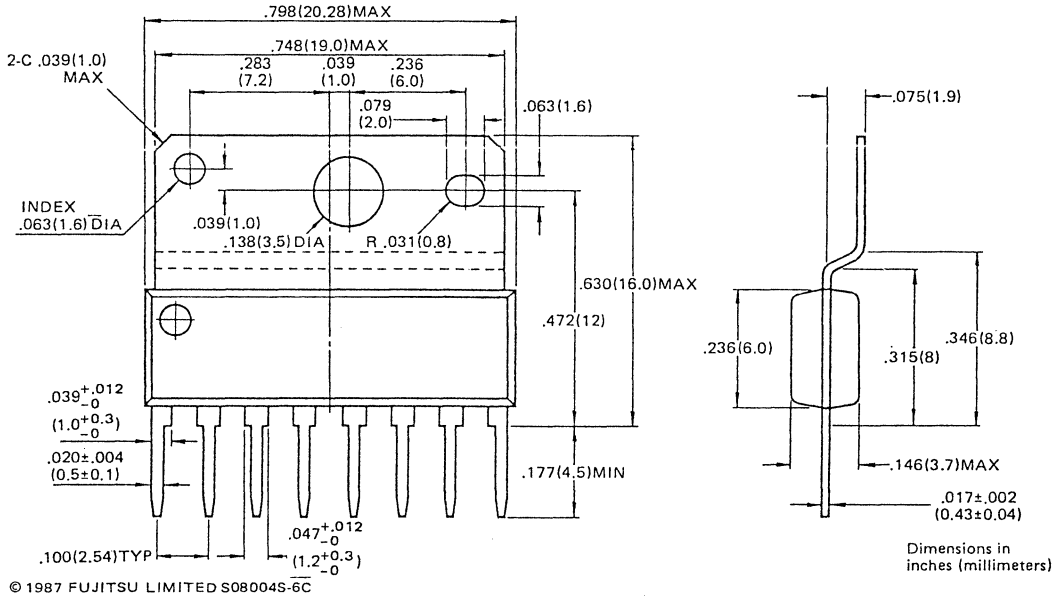
When 5 pin is connected to GND, constant current I_{IB} is generated internally.



$$R_{XH} = \frac{R_R}{1 - \frac{R_R}{R_H}}$$

$$R_{XL} = \frac{R_R}{1 - \frac{R_R}{R_H} + \frac{V_R}{I_{IB}R_H}}$$

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M01)



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Section 3

Automotive Audio

Fujitsu Part No.	Description	Features	Equiv. Prod.	Power Supply (V)	Package	No. of Pins
MB3106	Dual Pre Amp	Low Distortion (0.05%), V_{ND} = 120μV	—	+6 ~ +16	SIP	8
MB3110A	Dual Control Amp	Volume and Balance Control, 20dB Voltage Gain	—	+6 ~ +16	SIP	8
M3714A	6W Power Amp	PO = 6W/4Ω, 10W/2Ω, Audio Mute, Full Protection Circuits	—	+8 ~ +16	SIP (Heatsink)	8
M3715A	6W Power Amp	PO = 6W/4Ω, 10W/2Ω, Audio Mute, Full Protection Circuits	—	+8 ~ +16	SIP (Heatsink)	8
MB3722	Dual Power Amp	PO = 5.8W/4Ω, Audio Mute, Full Protection	—	+8 ~ +16	SIP (Heatsink)	12
MB3730A	Balanced Transformerless (BTL) AMP	PO = 14W/4Ω, Full Protection	—	+8 ~ +16	SIP (Heatsink)	7
MB3731	Balanced Transformerless (BTL) AMP	PO = 18W/4Ω, Audio Mute, Full Protection	—	+8 ~ +16	SIP (Heatsink)	12
MB3732	Balanced Transformerless (BTL) AMP	PO = 14W/4Ω, Audio Mute, Full Protection	—	+8 ~ +16	SIP	7
MB3733	Balanced Transformerless (BTL) AMP	PO = 20W/4Ω, Audio Mute, Full Protection	—	+8 ~ +16	SIP	12
MB3734	Balanced Transformerless (BTL) AMP	PO = 14W/4Ω, Audio Mute, Full Protection	—	+8 ~ +16	SIP (Heatsink)	9
MB3735	Balanced Transformerless (BTL) AMP	PO = 20W/4Ω, DC Mute, Full Protection	—	+8 ~ +16	SIP (Heatsink)	9
MB3736	Balanced Transformerless (BTL)AMP w/ Vcc Standby	PO = 15W/4Ω, Low THD, Full Protection	—	+8 ~ +16	SIP ZIP (Heatsink)	12 12
MB3737	Balanced Transformerless (BTL) AMP w/ Vcc Standby	PO = 25W/4Ω, Low THD, Full Protection	—	+8 ~ +16	SIP ZIP (Heatsink)	12 12
MB4104	FM Stereo Multiplex	Low Distortion .06% @ 300 mil	—	+8 ~ +14	Plastic DIP	16
MB4105	FM Stereo Multiplex	Low Distortion .06% @ 300 mil	—	+8 ~ +14	Plastic DIP	16

FUJITSU

DUAL LOW NOISE PRE-AMPLIFIER

MB3106

October 1987
Edition 1.0

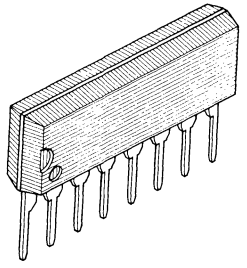
DUAL LOW NOISE PRE-AMPLIFIER

The Fujitsu MB3106 is a dual low noise pre-amplifier housed in a single in-line package for high density mounting on printed circuit boards for automotive audio stereo systems.

The MB3106 has a power supply stabilization circuit for low power supply voltage, and is designed to improve power efficiency at the output stage. Therefore, the MB3106 provides a wide output range, and can stably operate in a wide power supply voltage range and in a wide temperature range.

The MB3106 provides high gain in a low frequency range, because the feedback resistor operates in a wide tolerance condition.

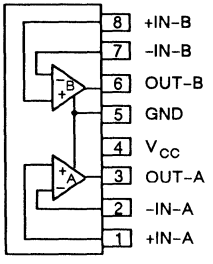
- High open loop gain : 90 dB typical
- Input noise voltage : 1 μV typical
- Protection circuit against over voltage at input stage
- On-chip power supply stabilizer
- Wide power supply range and high ripple rejection
- Package : 8-pin plastic SIP package
- Minimized number of external parts, due to on-chip bias circuit.



PLASTIC PACKAGE
SIP-08P-M03

PIN ASSIGNMENT

(Front View)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

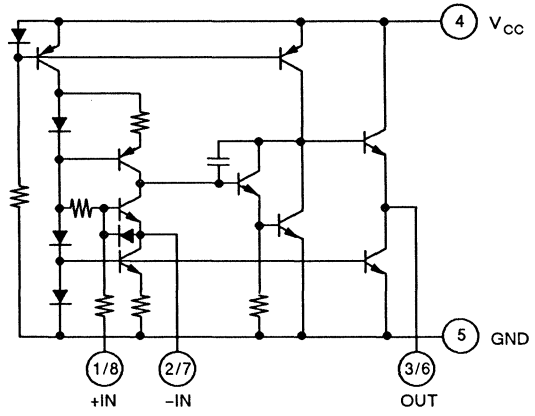
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Dissipation	P_D	200 ($T_A \leq 75$ °C)	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Fig. 1 — EQUIVALENT CIRCUIT (ONE CHANNEL)



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6 to 16	V
Temperature	T_A	-20 to +75	°C

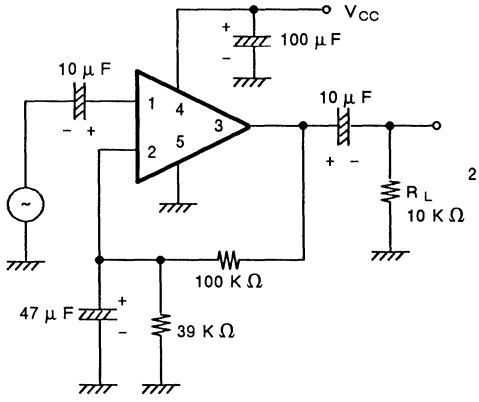
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 6V, f = 1kHz, R_L = 10kΩ)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}	—	—	3	4	mA
Open Loop Voltage Gain	A_{VO}	V_O = 0.8 V	75	90	—	dB
Closed Loop Voltage Gain	A_V	V_O = 0.8 V, NAB	—	42	—	dB
Maximum Output Voltage	V_{OM}	THD = 1%, NAB	1.0	1.6	—	V
Total Harmonic Distortion	THD	V_O = 0.8 V, NAB	—	0.05	0.3	%
Ouput Noise Voltage	V_{NO}	Rg = 2.2K Ω , NAB	—	120	200	μ V
Input Resistance	R_{IN}	NAB	50	150	—	kΩ
Channel Separation	—	V_O = 0.8 V, f = 10 KHz, NAB	—	65	—	dB
Ripple Rejection Ratio	—	f = 100 Hz, Rg = 2.2 KΩ, NAB	—	45	—	dB

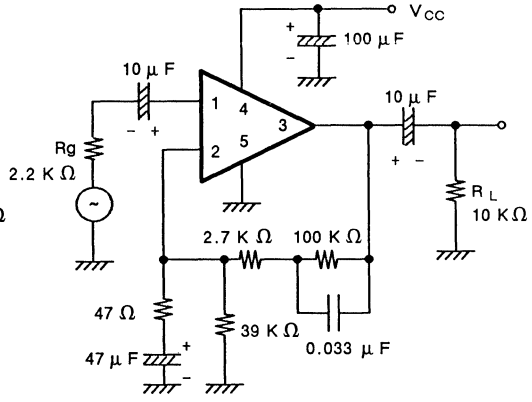
3

Fig. 2 — MEASUREMENT CIRCUITS
(Only one channel is illustrated)

1. I_{CC}, A_{VO}



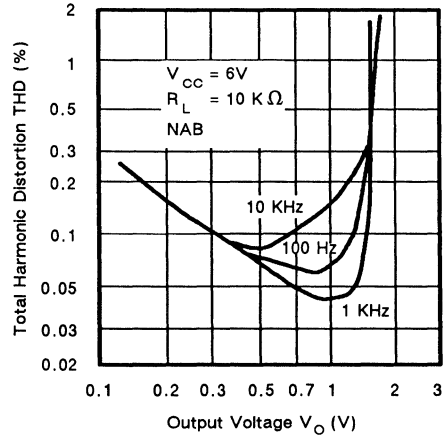
2. A_V, V_{OM}, THD, V_{NO}, R_{IN}



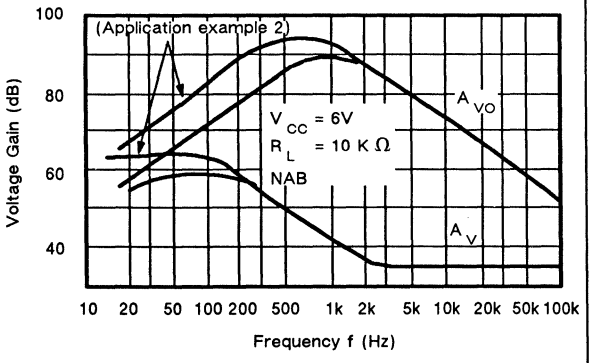
Note: V_{NO} is measured with the Bandpass filter of 30Hz to 30KHz.

TYPICAL PERFORMANCE CHARACTERISTICS

TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



VOLTAGE GAIN vs FREQUENCY



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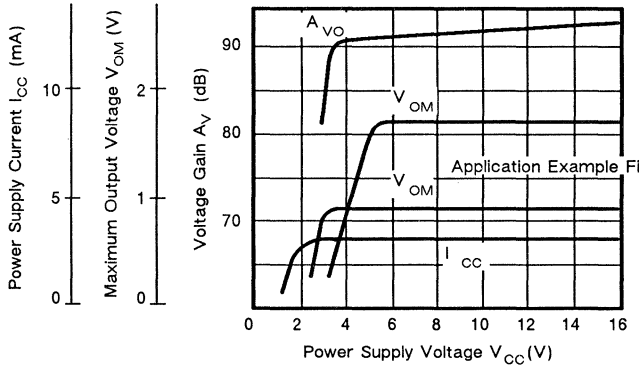
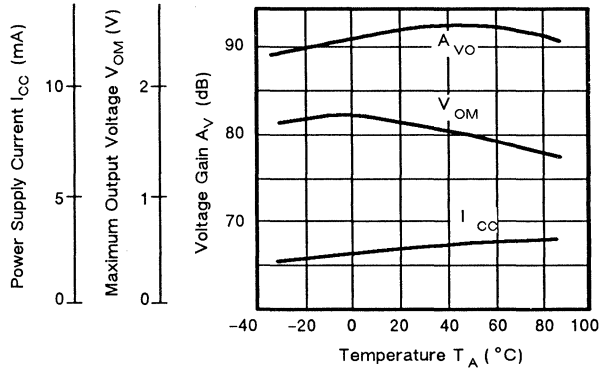
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

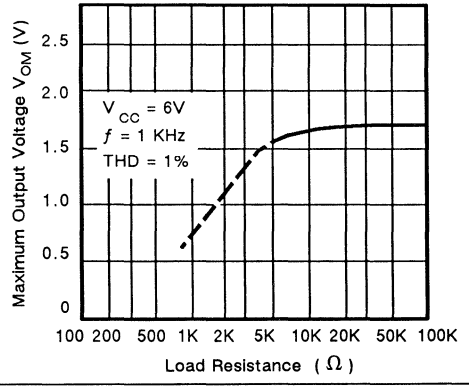
POWER SUPPLY CURRENT, MAXIMUM OUTPUT VOLTAGE, VOLTAGE GAIN vs POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT, MAXIMUM OUTPUT VOLTAGE, VOLTAGE GAIN vs TEMPERATURE



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



RIPPLE REJECTION RATIO vs FREQUENCY

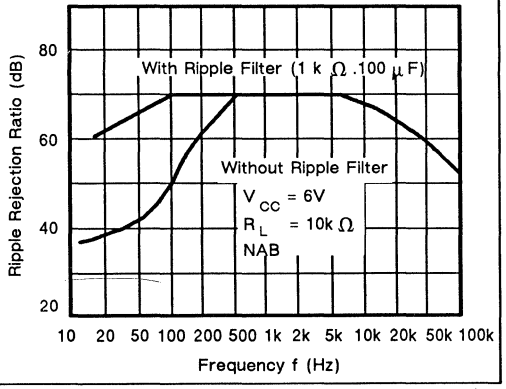
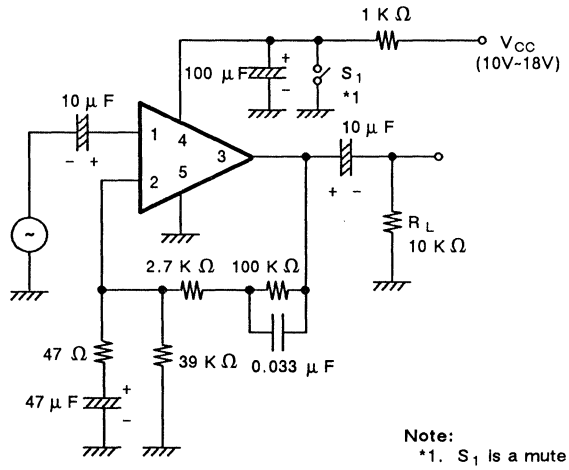
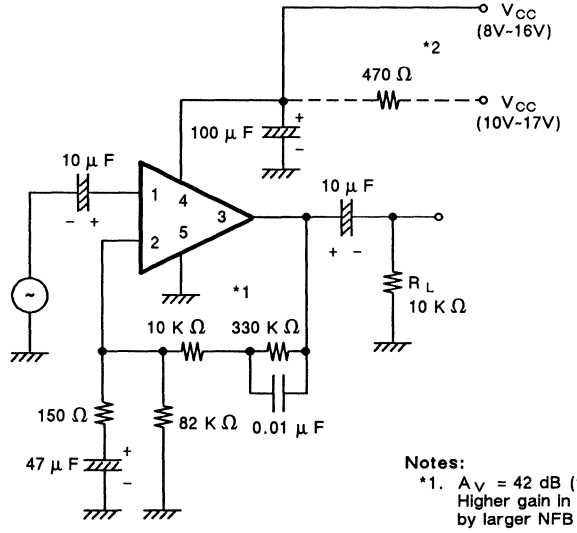


Fig. 3 — TYPICAL APPLICATION CIRCUIT
(Only one channel is illustrated)



Note:
*1. S_1 is a mute switch for the output.

Fig. 4 — HIGH GAIN CIRCUIT
(Only one channel is illustrated)



Notes:
*1. A_V = 42 dB (f = 1 KHz)
Higher gain in low band is obtained by larger NFB constant.

*2. To improve ripple rejection ratio.
(Improved as much as 20 dB at 100 Hz.

3

Fig. 5 — FOR LOW VOLTAGE POWER SUPPLY
(Only one channel is illustrated)

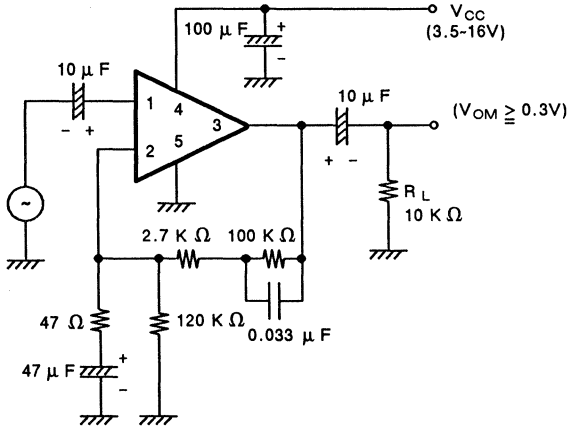
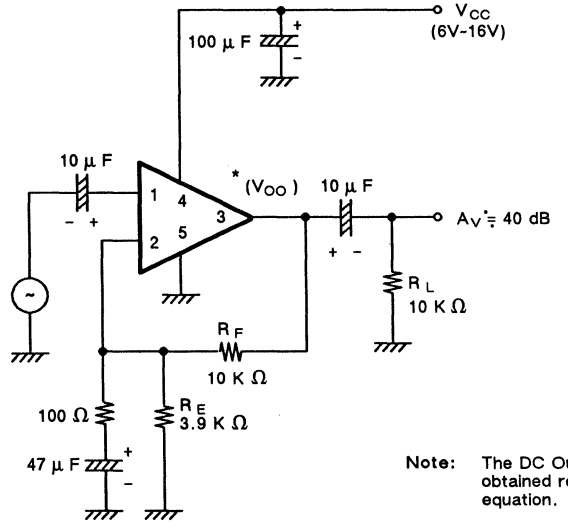


Fig. 6 — FLAT AMPLIFIER CIRCUIT
(Only one channel is illustrated)

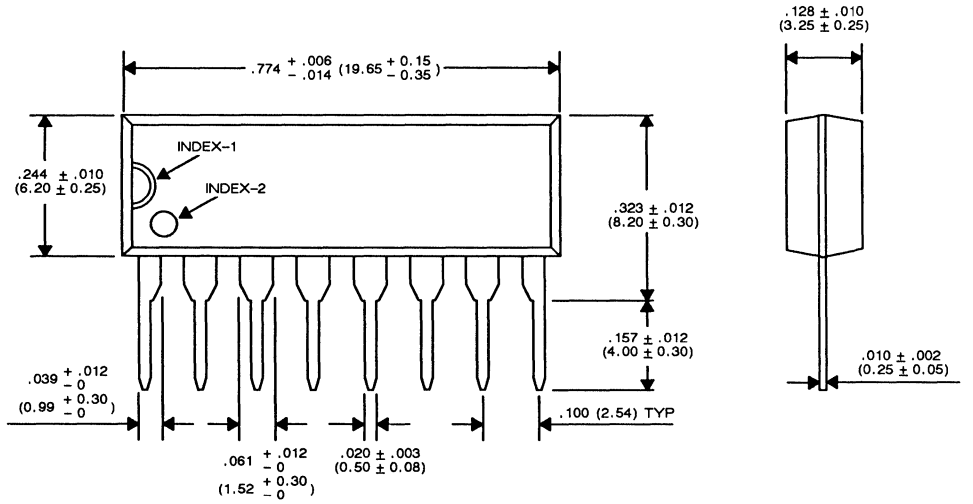


Note: The DC Output Voltage V_{OO} is obtained roughly from the following equation.

$$V_{OO} \simeq 0.75 \left(1 + \frac{R_F}{R_E}\right)$$

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M03)



Dimensions in inches (millimeters)

S08010S-2C

FUJITSU

DUAL CONTROL AMPLIFIER

MB3110A

October 1987
Edition 1.0

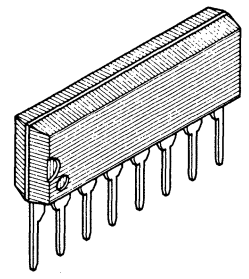
DUAL CONTROL AMPLIFIER

3

The Fujitsu MB3110A is a dual-channel amplifier with separate volume-and-balance controls for both A-and-B channels. Each channel consists of a 20 dB amplifier with symmetrical balance attenuation over a wide range and low distortion of audio frequencies. Thus, the MB3110A is an excellent choice for general-purpose audio work and media reproduction that requires high-fidelity processing. The amplifier circuits are designed to provide optimum performance with a bare minimum of external parts.

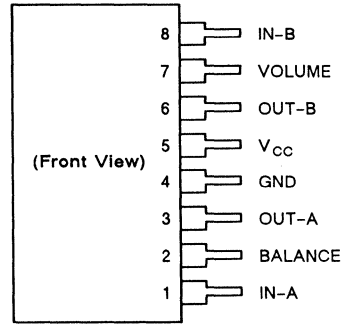
The MB3110A is housed in an 8-pin Single In-Line Package (SIP) that is especially useful where mounting space is limited or in applications where high-density populations are required.

- Voltage gain: 20 dB (typical)
- Input control voltage: OV to V_{CC}
- Maximum volume attenuation: 80 dB (typical)
- Maximum balance attenuation: 80 dB (typical)
- Low noise: 80 μV rms (typical)
- Maximum output voltage: 1.7V rms (typical)
- SIP package



PLASTIC PACKAGE
SIP-08P-M03

PIN ASSIGNMENT



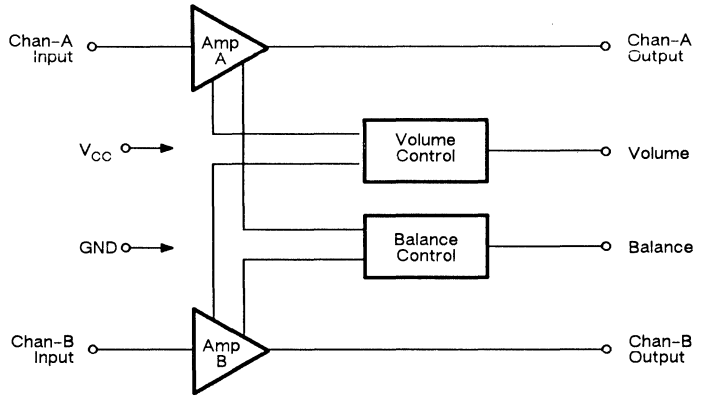
ABSOLUTE MAXIMUM RATINGS — T_A = 25 °C (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	16	V
Input Control Voltage	V_C	0 to V_{CC}	V
Power Dissipation	P_D	530 ($T_A \leq 65$ °C)	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB3110A BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6 to 12	V
Load Resistance	R_L	≥ 32	Ω
Operating Temperature	T_A	-20 to +75	°C

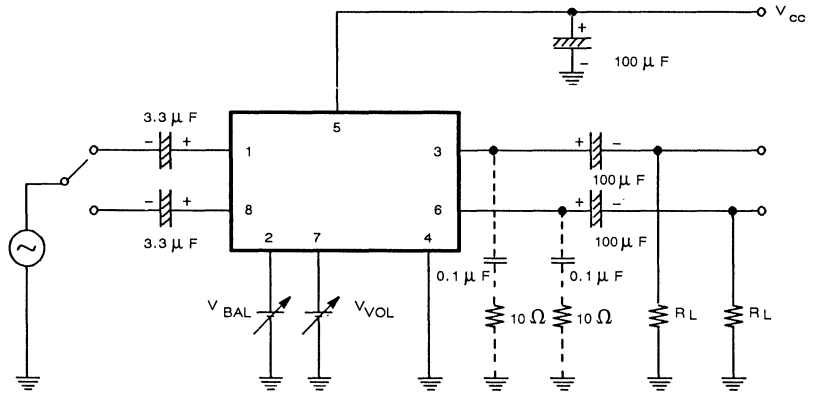
ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS (V_{CC} = 9V, R_L = 100Ω, f = 1kHz, V_{IN} = 50 mV rms, and T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions (Note)	Values				Unit
			V_{VOL} (V)	Min	Typ	Max	
Power Supply Current	I_{CC}	V_{IN} = OV	9.0	—	8	14	mA
Voltage Gain	A_{VO}	—	9.0	18	20	22	dB
Volume Attenuation	A_{VMC}	—	4.0	8.5	10	11.5	dB
Maximum Volume Attenuation	A_{VMM}	—	0	70	80	—	dB
Balance Attenuation at Center Position	A_{BLC}	V_{BAL} = 4.5V	9.0	0.5	2.5	4.0	dB
Maximum Balance Attenuation	A_{BLM}	V_{BAL}= OV/9V	9.0	70	80	—	dB
Channel Balance	CB	—	9.0	-1	0	+1	dB
Channel Separation	CS	—	9.0	—	60	—	dB
Total Harmonic Distortion	THD	—	9.0	—	0.1	0.5	%
Maximum Output Voltage	V_{OM}	THD=1%	9.0	1.2	1.7	—	Vrms
Output Noise Voltage	V_{NO}	Rg = ∞, BW = 20 to 20kHz	0	—	80	200	μVrms
Input Resistance	R_{IN}	—	9.0	15	20	—	kΩ
Volume Control Input Current	I_{7H}	—	9.0	90	150	250	μA
High-level Balance Control Current	I_{2H}	V_{BAL} = 9.0V	9.0	36	60	100	μA
Low-level Balance Control Current	I_{2L}	V_{BAL} = OV	9.0	-100	-60	-36	μA

NOTE: Balance control pin is open unless otherwise specified.

Fig. 2 — TEST CIRCUIT

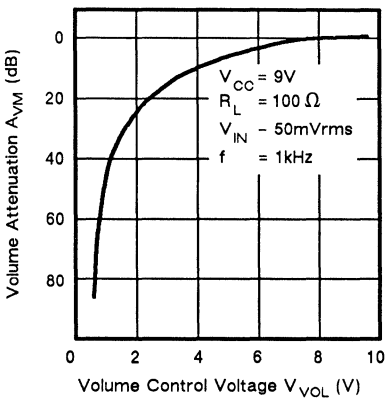


Notes:

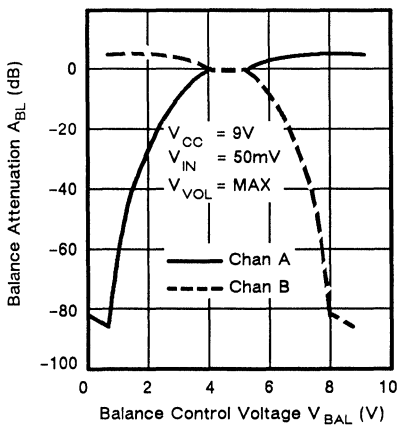
1. When measuring THD and V_{NO} , a bandpass filter with a bandwidth of 20Hz-to-20kHz is required; when measuring CS, a bandpass filter with a center frequency (fc) of 1 kHz is required.
2. Dotted-line components are used to inhibit parasitic oscillations.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLUME RESPONSE



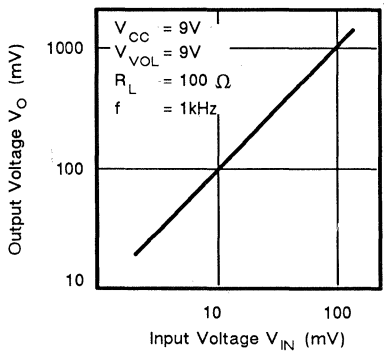
BALANCE RESPONSE



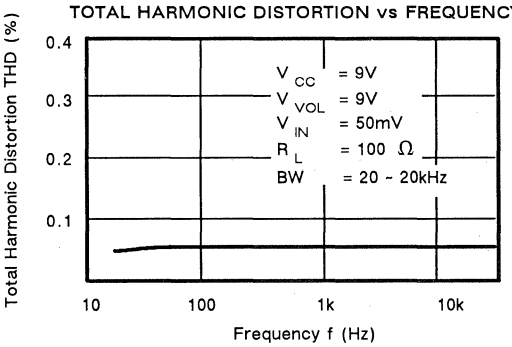
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

3

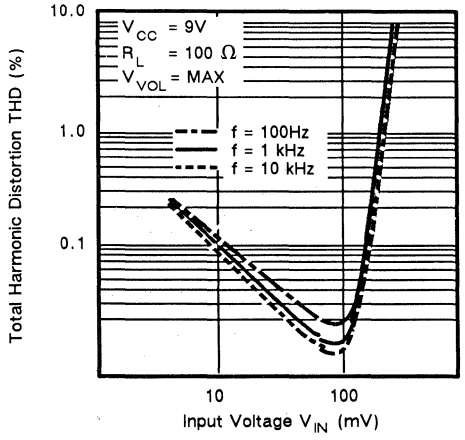
OUTPUT VOLTAGE vs INPUT VOLTAGE



TOTAL HARMONIC DISTORTION vs FREQUENCY

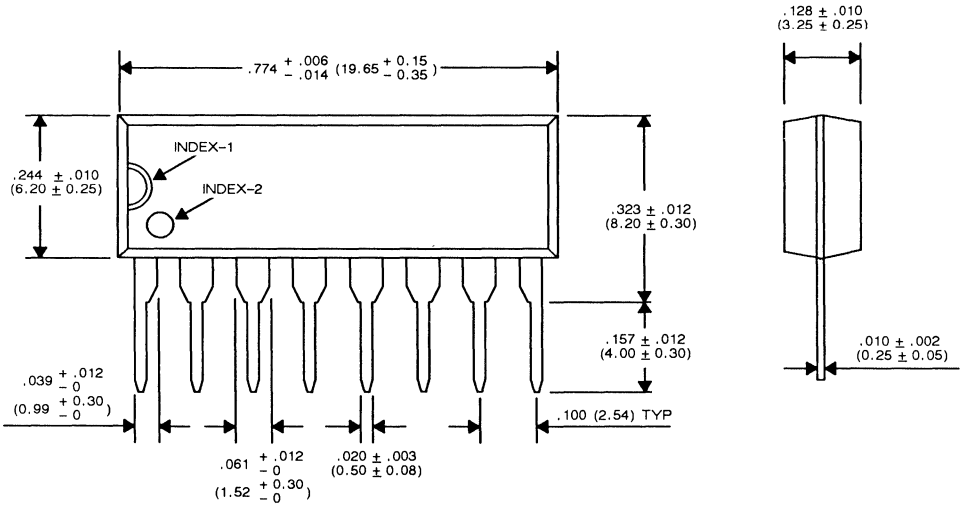


TOTAL HARMONIC DISTORTION vs INPUT VOLTAGE



PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M03)



Dimensions in inches (millimeters)

S08010S-2C

FUJITSU

6 WATT AUDIO AMPLIFIER

MB 3714A MB 3715A

June 1986
Edition 1.0

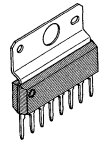
MB 3714A/MB 3715A
6 Watt Audio Amplifier

3

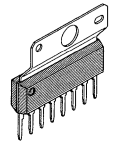
The Fujitsu MB 3714A and MB 3715A are monolithic integrated circuits of 6 Watt audio power amplifiers packaged in plastic single in-line package (SIP) with heat radiation fin.

The MB 3714A/MB 3715A are designed to reduce output distortion and power-on pop noise, working at high gain and high output power.

The MB 3714A and MB 3715A can drive even 2 ohm load and are designed against breakdown by load short and supply voltage surge. The packages are protected to mis-mounting with biased hole on the fin.



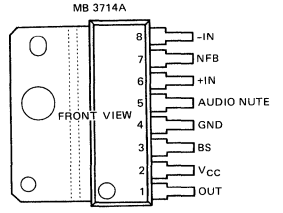
MB 3714A
PLASTIC PACKAGE
SIP-08P-M01

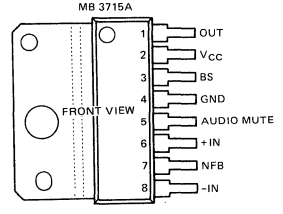


MB 3715A
PLASTIC PACKAGE
SIP-08P-M04

- High Power: 6.0 W typ/4Ω, 10.0 W typ/2Ω
- High Gain: 52.5 dB typ.
- Low Distortion
- Small Plastic 8-pin Single In-Line Package with Easily Heat Radiation and Mis-Mounting-Proof Form
- Minimum External Components
- Low Power-on Pop Noise
- Low Impedance Load: 2Ω Load
- Audio Mute Circuit
- Various Protection Circuits
- Power Supply Surge Protection
- Thermal Protection
- Load Short Protection

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Supply Voltage (Surge) ($t_s \leqq 0.2$ ms, $t_r \geqq 1$ ms)	V_{CCS}	40	V
Output Current (Peak)	I_{OP}	4.5	A
Power Dissipation ($T_C \leqq 75°C$)	P_D	7.5	W
Storage Temperature	T_{STG}	-55 to +150	°C

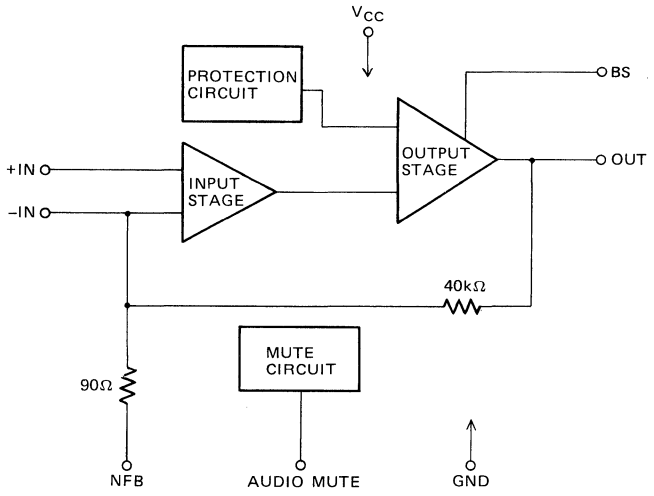
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	8.0		16.0	V
Operating Ambient Temperature	T_A	−20		+75	°C

BLOCK DIAGRAM



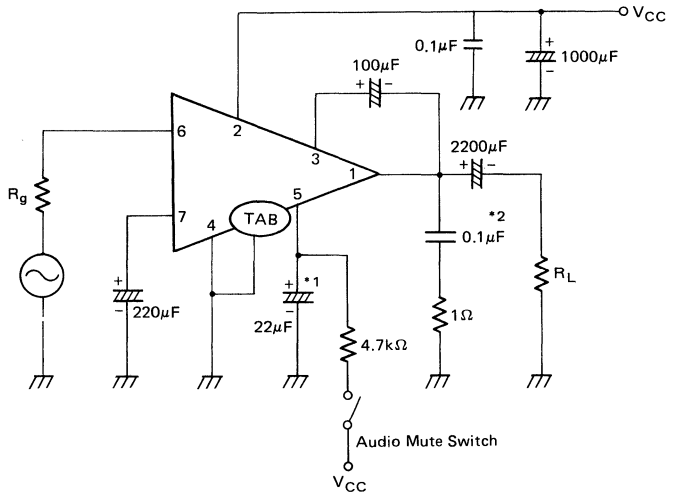
3

ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2 V, R_L = 4 Ω and f = 1kHz, R_g = 600 Ω unless otherwise noted.)

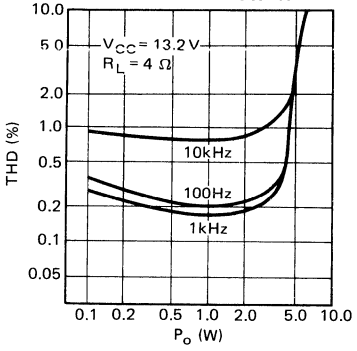
Parameter	Condition	Symbol	Min	Typ	Max	Unit
Quiescent Power Supply Current	V_{IN} = 0	I_Q		30	60	mA
Voltage Gain	P_O = 1 W	A_v	50	52.5	55	dB
Output Power	THD = 10%	P_O	5.5	6.0		W
	THD = 10% R_L = 2 Ω		8.0	10.0		W
Output Noise Voltage	R_g = 10 kΩ BW = 20 to 20 kHz	V_{NO}		1.0	2.0	mV
Total Harmonic Distortion	P_O = 1 W	THD		0.2	1.0	%
	P_O = 1 W R_L = 2 Ω			0.3	1.0	%
Input Resistance		R_{IN}	20	30		kΩ
Attenuation Ratio at Audio Mute Mode		ATT		46		dB

TYPICAL APPLICATION CIRCUIT

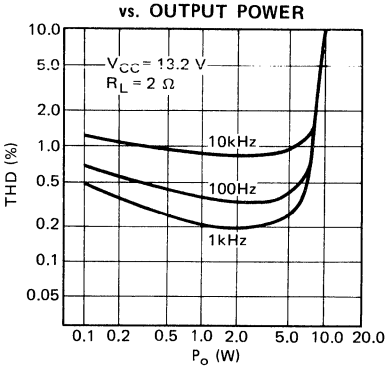


NOTE: *1: For improved ripple reduction, *2: Polyethlen Terephthalate Film Capacitor

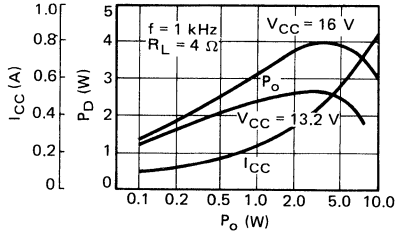
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



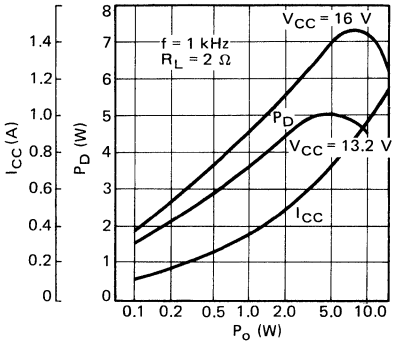
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



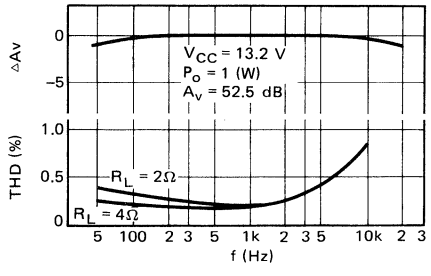
POWER DISSIPATION/SUPPLY
CURRENT vs. OUTPUT POWER



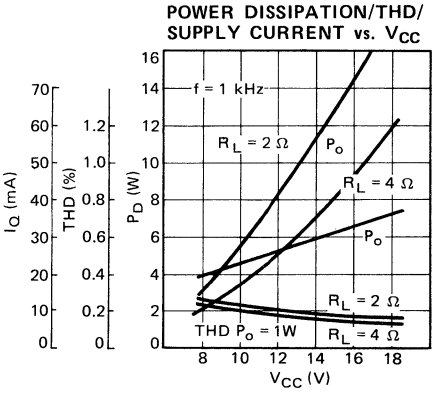
POWER DISSIPATION/SUPPLY
CURRENT vs. OUTPUT POWER



VOLTAGE GAIN/TOTAL HARMONIC
DISTORTION vs. FREQUENCY



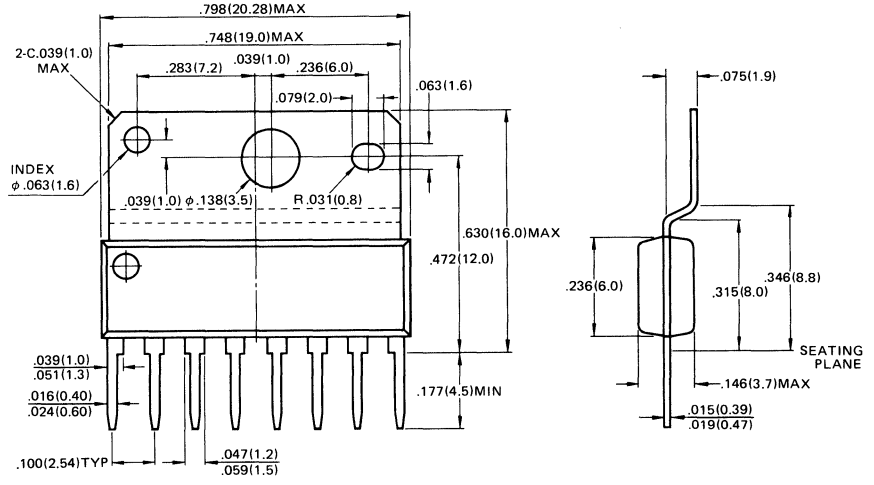
POWER DISSIPATION/THD/
SUPPLY CURRENT vs. V_{CC}



3

PACKAGE DIMENSIONS OF MB 3714A

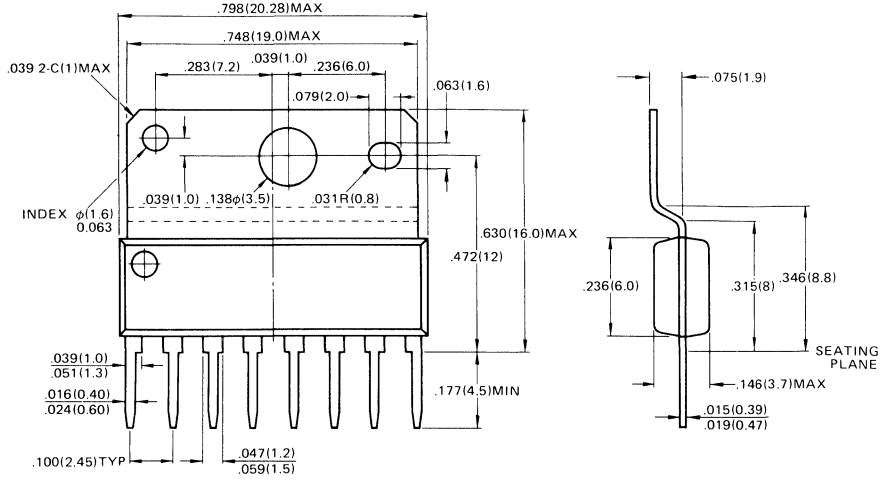
8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M01)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS OF MB 3715A

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M04)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

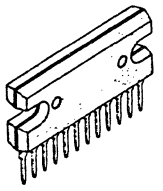
FUJITSU

MB3722

5.8 W DUAL AUDIO POWER AMPLIFIER

TS569-B884
April 1988

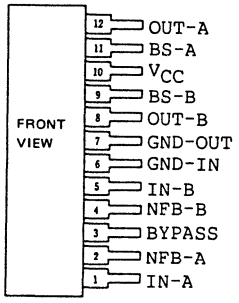
The Fujitsu MB3722 is designed for a dual low-frequency high-power amplifier which is packed in 12 pin single in line plastic package. The MB3722 requires a few external components, this enables high density mounting. Design for heat radiation is easy because thermal resistance is low. The MB3722 is internal power-on pop noise protection circuitry and various protection circuitry. The device is suitable best for car-stereo.



PLASTIC PACKAGE
SIP-12P-M01

- High power output : 5.8 W typ.
- Low Noise Output Voltage : 0.8 mV typ.
- Low Total Harmonic Distortion : 0.2 % typ.
- Minimum external components
- On chip power on pop noise protection circuit
- Audio mute function is provided
- Separated GND pins for Input/Output circuit
- Various protection circuits
  - Over voltage protection
  - Thermal protection
  - Load short protection
  - Output pin-to-DC short protection

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

(T_C = 25°C)

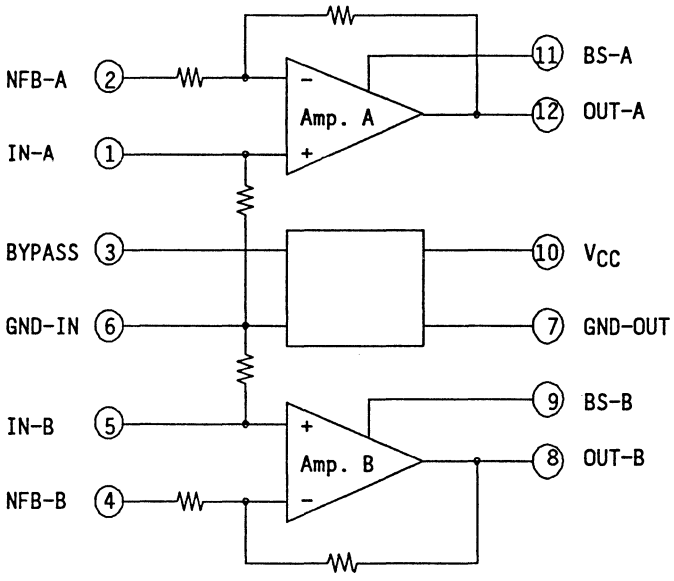
Rating	Symbol	Value	Unit
Power Supply Voltage (No signal)	V_{CCDC}	24	V
Power Supply Voltage (Operation)	V_{CC}	18	V
Power Supply Voltage (Surge)	V_{CCS}	40 *	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature (Case)	T_C	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +150	°C

NOTE: * $t_S \leq 0.2$ sec, $t_r \geq 1$ msec

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB3722 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

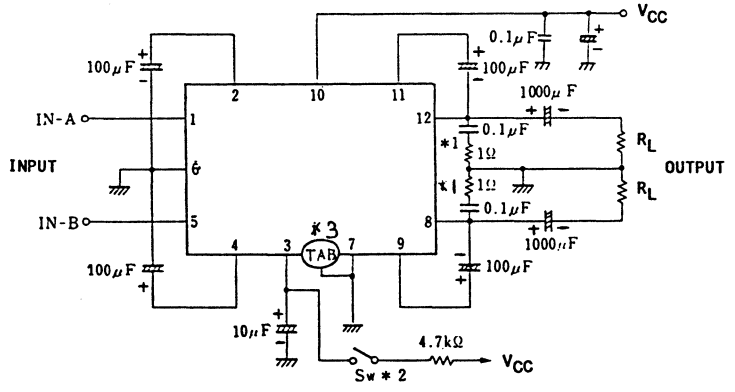
Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Operating Temperature	T_C	-20 to +75	°C
Output Load	R_L	2 to 8 *	Ω

Note : * Dual operation.

ELECTRICAL CHARACTERISTICS (V_{CC}=13.2V, f=1kHz, R_L=4Ω, T_C=25°C, One channel operation)

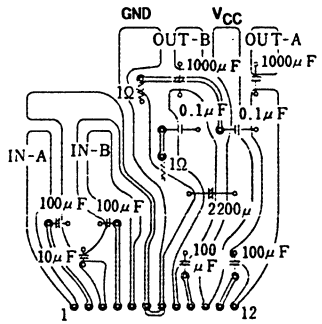
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_Q	V_{IN}=0V, R_L=∞		80	160	mA
Voltage Gain	A_V	P_O=1W	48.5	50.5	52.5	dB
Difference Voltage Gain	ΔA_V	P_O=1W		0	1.5	dB
Output Power	P_O	THD=10%	5.0	5.8		W
Total Harmonic Distortion	THD	P_O=1W		0.2	1.0	%
Output Noise Voltage	V_{NO}	Rg=10kΩ,BW=20 to20kHz		0.8	1.6	mV
Input Resistance	R_{IN}		20	30		kΩ
Cross Talk		Rg=600Ω	40	50		dB
Audio Mute Attenuation		Rg=600Ω		40		dB

Fig. 2 - TYPICAL APPLICATION EXAMPLE



Notes: *1 Please use Mylar condeser.
*2 When V_{CC} is apply to the pin 3, Audio mute (40dB) is available.
*3 The TAB should be connected with the GND.

Fig.3 - TYPICAL APPLICATION CIRCUIT PATTERN (BOTTOM VIEW)



TYPICAL CHARACTERISTICS CURVES

Fig.4 - TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

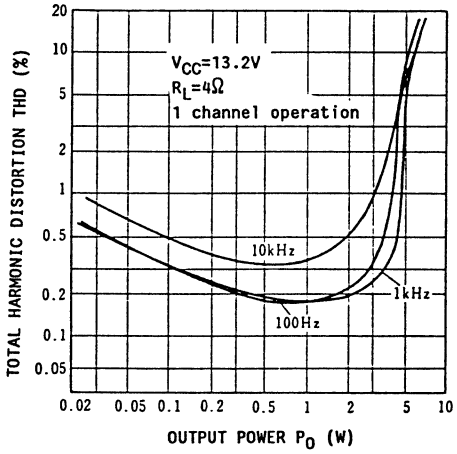


Fig.5 - TOTAL HARMONIC DISTORTION vs. FREQUENCY

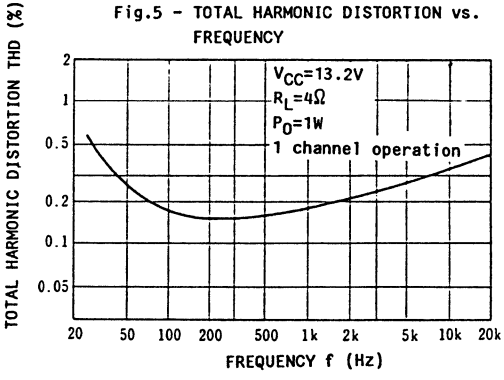
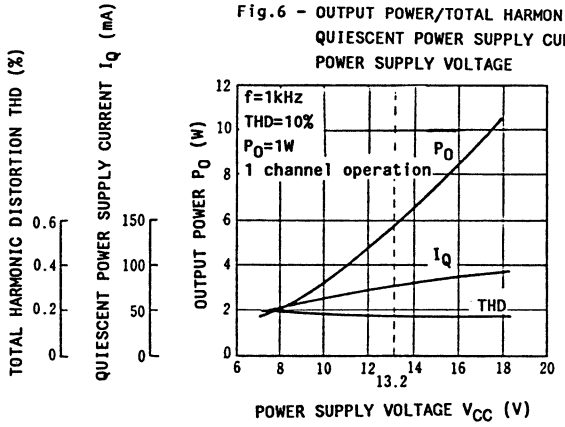
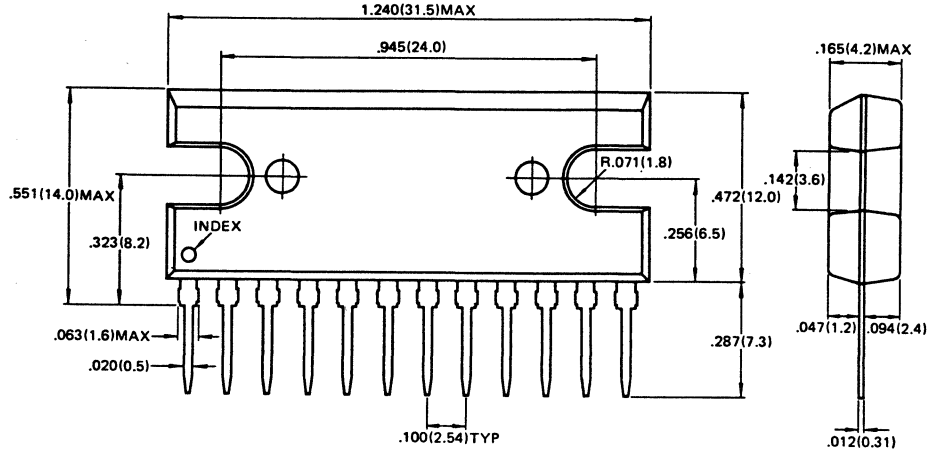


Fig.6 - OUTPUT POWER/TOTAL HARMONIC DISTORTION/ QUIESCENT POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE



PACKAGE DIMENSIONS

12-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE NO.: SIP-12P-M01)



Dimensions in inches (millimeters)

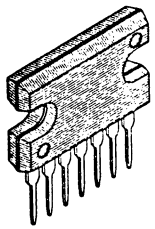
FUJITSU

MB3730A

TS570-A878
August 1987

14 W BTL AUDIO POWER AMPLIFIER

The Fujitsu MB3730A is designed for a low-frequency high-power amplifier with internal BTL(Balanced Transformer Less) circuitry. The MB3730A is packed in 7 pin single in line plastic package and requires a few external components, this enables high density mounting. Design for heat radiation is easy because thermal resistance is low 3°C/W.
The MB3730A is internal power-on pop noise protection circuit and various protection circuits. The device is suitable best for car-stereo.

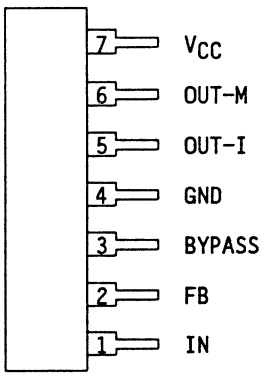


PLASTIC PACKAGE
SIP-7P-M01

- High power output : 14W typ.
- 7-pin Single In Line package
- Minimum external components
- Various protection circuits
  - Over voltage protection
  - Load short protection
  - Thermal protection
  - Output pin-to-DC short protection
- No break-down: between pins is shorted or inverted insertion
- Low thermal resistance : 3°C/W
- On-chip power-on pop noise protection circuit

PIN ASSIGNMENT

(Front View)



ABSOLUTE MAXIMUM RATINGS (See NOTE)

(T_C = 25°C)

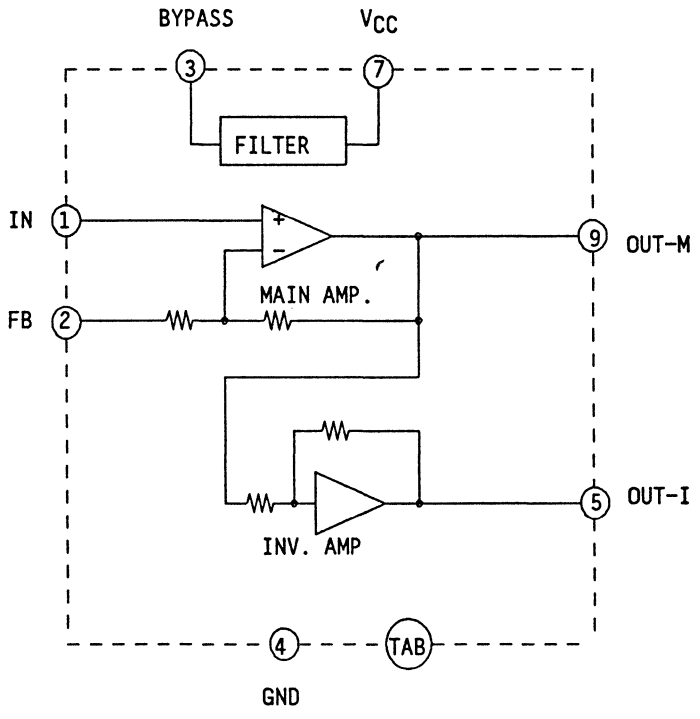
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge)	V_{CCS}	50 *	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note:
* $t_s \leq 0.2$ sec, $t_r \geq 1$ msec

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB3730A BLOCK DIAGRAM



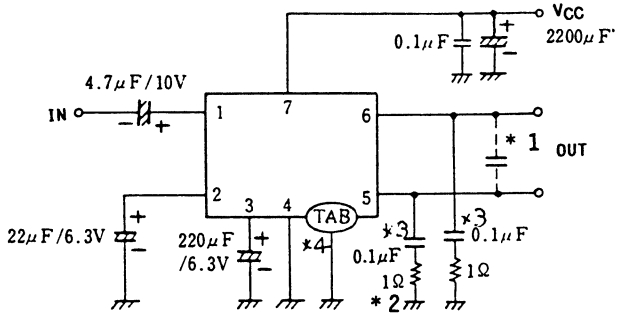
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Operating Temperature	T_A	-20 to +75	°C

ELECTRICAL CHARACTERISTICS (T_C=25°C, V_{CC}=13.2V, R_L=4Ω, f=1kHz)

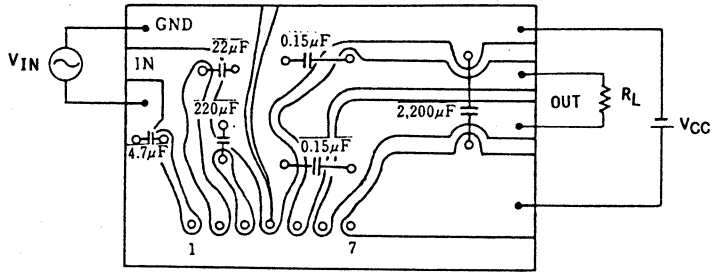
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_Q	V_{IN}=0V, R_L=∞		80	200	mA
Voltage Gain	A_V	P_O=1W	52.5	55	57.5	dB
Output Power	P_O	THD=10%	10	14		W
Total Harmonic Distortion	THD	P_O=1W		0.2	1.0	%
Output Noise Voltage	V_{NO}	Rg=10kΩ,BW=20 to20kHz		1.0	2.0	mV
Input Resistance	R_{IN}		40	70		kΩ
Output Offset Voltage	V_{OO}			0.2	0.4	V

Fig. 2 - TYPICAL CONNECTION EXAMPLE



Notes: *1 Effective to prevent from oscillation depending on printing pattern.
*2 When power supply line is stable, please connect with V_{CC} side, it restrains the oscillation.
*3 Use Mylar Capacitor.
*4 The TAB should be connected with GND.

Fig.3 - RECOMMENDED CONNECTION PATTERN (BOTTOM VIEW)



3

TYPICAL CHARACTERISTICS CURVES

Fig.4 - TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

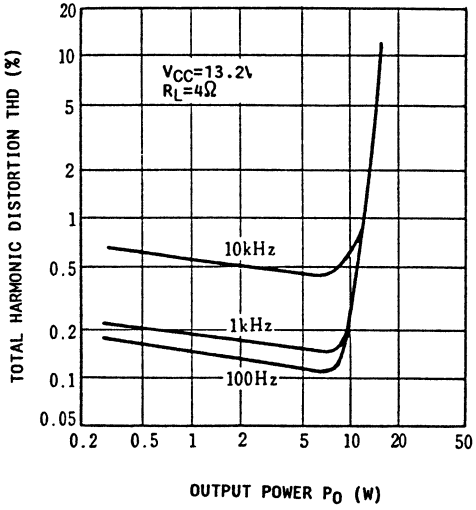


Fig.5 - OUTPUT POWER/TOTAL HARMONIC DISTORTION/ QUIESCENT POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE

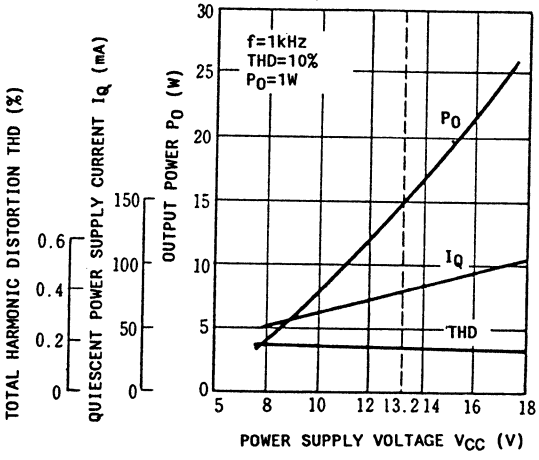


Fig.6 - VOLTAGE GAIN vs. FREQUENCY

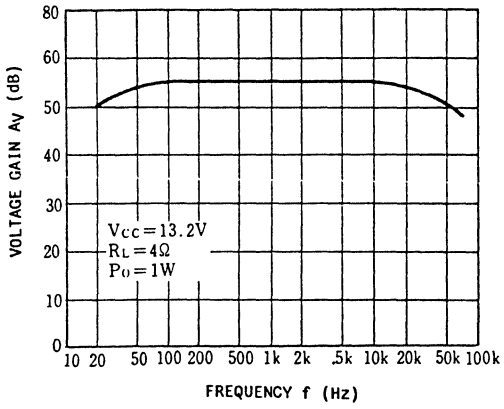
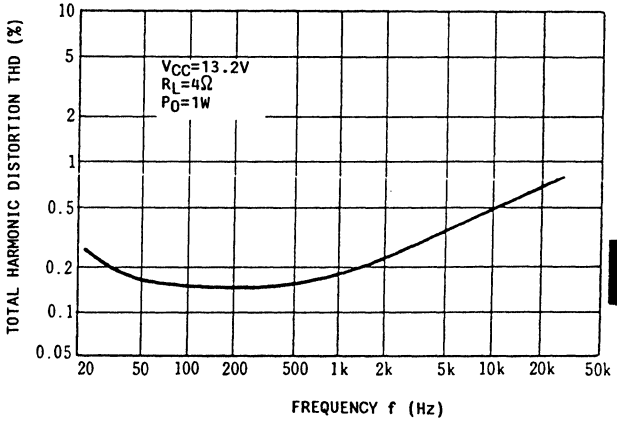
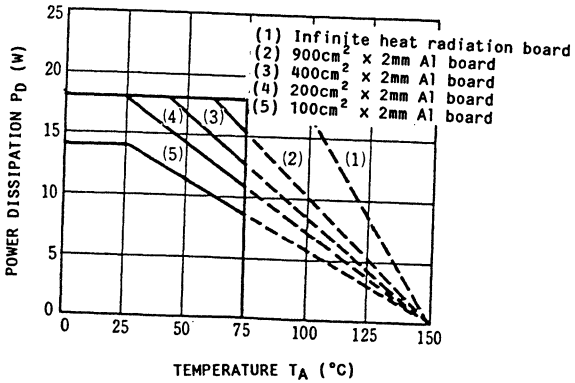


Fig.7 - TOTAL HARMONIC DISTORTION vs. FREQUENCY



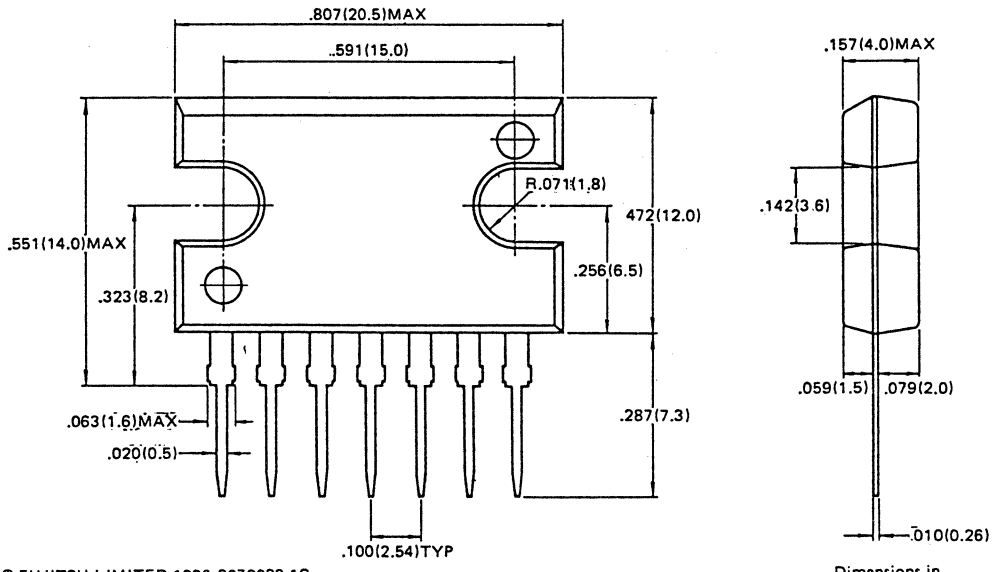
3

Fig.8 - POWER DISSIPATION vs. TEMPERATURE



PACKAGE DIMENSIONS

7-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-07P-M01)



Dimensions in inches (millimeters)

FUJITSU

MB3731

18W BTL POWER AMPLIFIER

The Fujitsu MB3731 is designed for a low-frequency high-power amplifier with internal BTL(Balanced Transformerless) circuitry. The MB3731 is packaged in a small plastic, 12-pin Single-In-Line Package (SIP) which has low thermal resistance, that a design for heat radiation can be performed with low cost.

Also, the MB3731 requres such a few external components can be performed with high density.

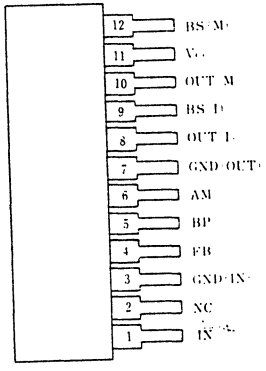
The MB3731 contains a filtering circuitry for power-on pop noise and various protection circuits.

- High Power Output : 18W with R_L = 4Ω
- Minimum External Components
- Small Plastic 12-pin Single-In-Line Package
- Low Thermal Resistance
- Various Protection Curcuitries :

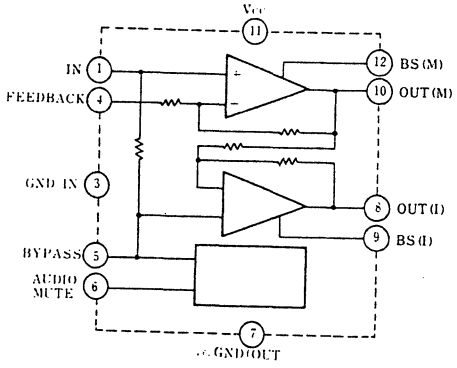
  Power Supply Serge Protection
  Excess Voltage Protection
  Thermal Protection
  Load Short Protection
  DC Short Protection for Output Terminal
  Load-Power Supply Short Protection

- Low Power Pop-noise
- Separated Gound pins for Input and Output
- Audio-mute function

Pin Assignment (FRONT VIEW)



Block Diagram



ABSOLUTE MAXIMUN RATINGS

(Tc=25°C)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge Voltage)	V_{CCS}	40*	V
Peak Output Current	$I_{O(Peak)}$	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature	T_{OP}	-20 to +75	°C
Storage Temperatuer	T_{STG}	-55 to +150	°C

Note : * t_S<0.2 sec., t_r>1 msec.

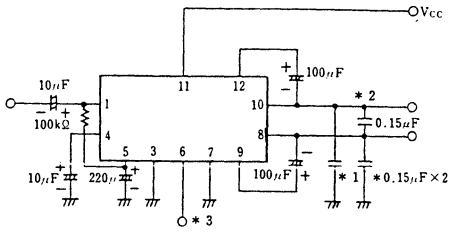
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Operating Temperature	T_{OP}	-20 to +75	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=13.2V, f=1kHz, R_L=4Ω, T_C=25°C)

Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Quescent Power Supply Current	V_{IN}=0V R_L=∞	I_Q	-	80	200	mA
Voltage Gain	P_O=1W	Av	44.5	47	49.5	dB
Output Power	THD=10%	P_O	15	18	-	W
Total Harmonic Distortion	P_O=1W	THD	-	0.1	0.5	%
Output Noise Voltage	R_g=10kΩ, BW=20Hz to 20kHz	V_{NO}	-	0.5	1.0	mV
Input Resistance		R_{IN}	40	70	-	kΩ
Output Offset Voltage	V_{IN}=0	V_{OO}	-	0.2	0.4	V
Audio Mute Attenuation	P_O=1W		-	43	-	dB

TYPICAL APPLICATION EXAMPLE



Note:

*1 Recommended capacitor : Effective capacitance ; 0.15μF+100%/-20% 1 through 10 MHz ESR=0.5Ω to 2Ω. If polyethlen Terephthalate Film Capacitor is used, it is recommended to connect 1Ω resistor in series.

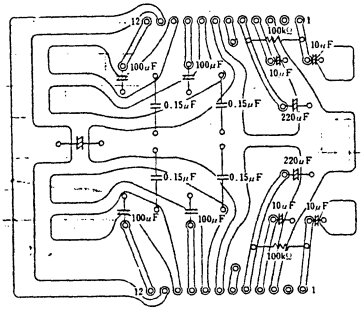
*2 This capacitor's effect depends on the circuit pattern.

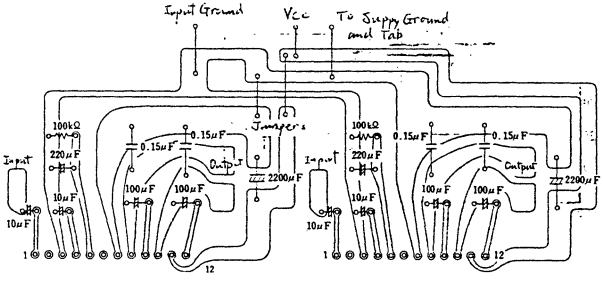
*3 The output can be cut off by grounding the pin 6.

*4 The tab should be connected with the ground.

3

TYPICAL APPLICATION CIRCUIT PATTERN

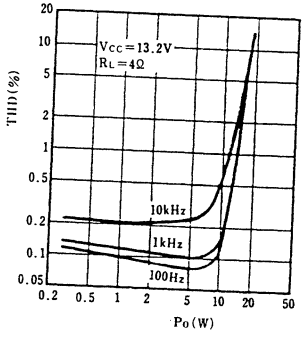




TYPICAL ELECTRICAL CURVES

TOTAL HARMONIC DISTORTION VS. OUTPUT POWER

Total Harmonic Distortion (THD) (%)

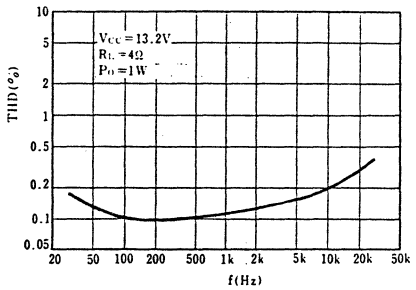


Output Power

TYPICAL ELECTRICAL CURVES (Cont'd)

TOTAL HARMONIC DISTORTION VS. FREQUENCY

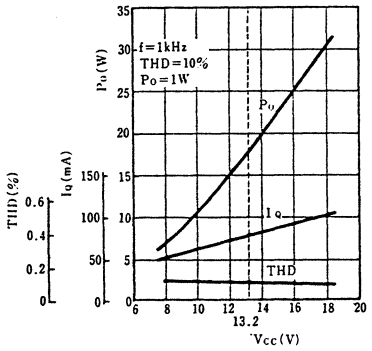
Total Harmonic Distortion (THD) (%)



Frequency f (Hz)

TOTAL HARMONIC DISTORTION, QUIESCENT POWER SUPPLY CURRENT, OUTPUT POWER VS. SUPPLY VOLTAGE

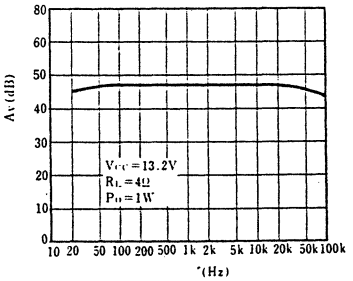
Total Harmonic Distortion (THD) (%)
Quiescent Power Supply Current I_Q (mA)
Output Power P_O (W)



Supply Voltage V_{CC} (V)

VOLTAGE GAIN VS. FREQUENCY

Voltage Gain Av (dB)

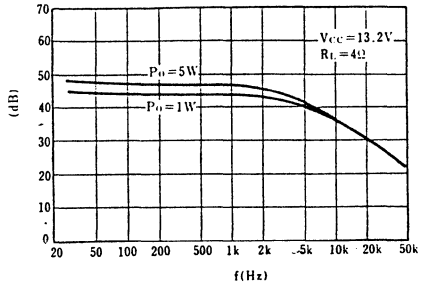


Frequency f (Hz)

TYPICAL ELECTRICAL CURVES (Cont'd)

AUDIO MUTE ATTENATION VS. FREQUENCY

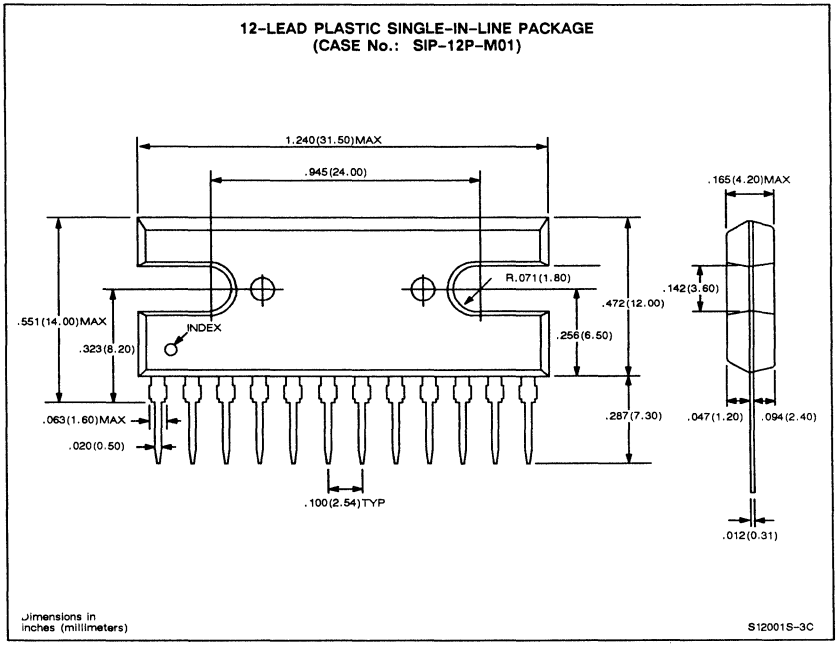
Audio Mute Attenation (dB)



Frequecny f (Hz)

3

Package Dimensions



DSTV83-059

FUJITSU

14W BTL AUDIO POWER AMPLIFIER

MB3732
MB3734

July 1988
Edition 2.0

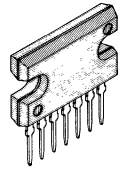
3

14W BTL AUDIO POWER AMPLIFIER

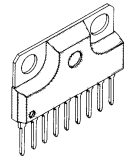
The Fujitsu MB3732 and MB3734 are low-frequency high-power amplifiers with internal BTL (Bridged Output Trans Former-less) circuitry. Suitable for car stereos, the MB3732 and the MB3734 are packed in small plastic packages which have low thermal resistance. Designing for heat radiation can be executed at a low cost. The devices require few external components, so high density mounting is optimized.

The MB3732 and MB3734 comprise various protection functions, including an internal power-on pop noise reduction circuit.

- High power output : 14W typical
- Small plastic package : 7-pin SIP for the MB3732
  9-pin SIP for the MB3734
- Minimum external components
- Low thermal resistance : 3°C/W in the MB3732
  4°C/W in the MB3734
- On-chip power-on pop noise reduction circuit
- No breakdown : between pins is shorted or insertion is inverted
- Low distortion : THD = 0.07% typical
- Various protection circuits :
  Power supply surge protection, Thermal protection
  Load short protection, Over voltage protection
  Output pin-to-DC short protection

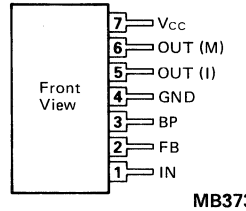


PLASTIC PACKAGE
SIP-07P-M01

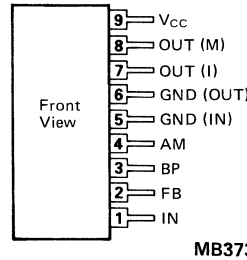


PLASTIC PACKAGE
SIP-09P-M02

PIN ASSIGNMENT



MB3732



MB3734

ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_C = 25°C)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Supply Voltage (Surge)	V_{CCS}	50*	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature (Case)	T_C	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note: $t_s \leq 0.2$ sec, $t_r \geq 1$ msec

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB3732 BLOCK DIAGRAM

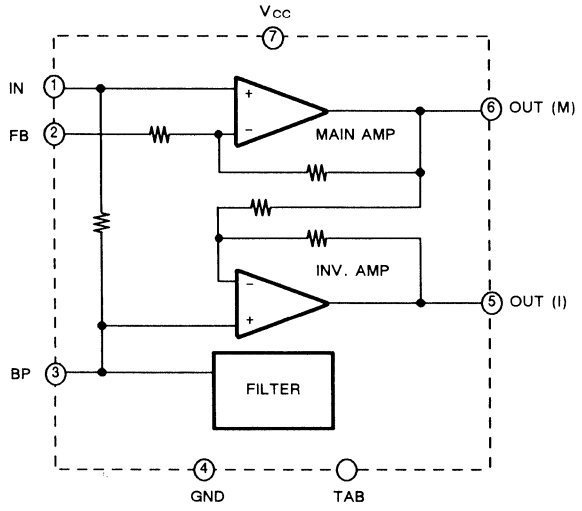
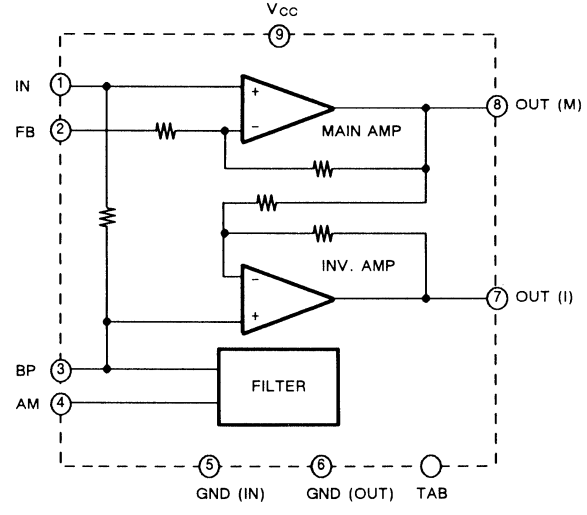


Fig. 2 – MB3734 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Max	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Operating Temperature (Case)	T_C	−20 to +75	°C

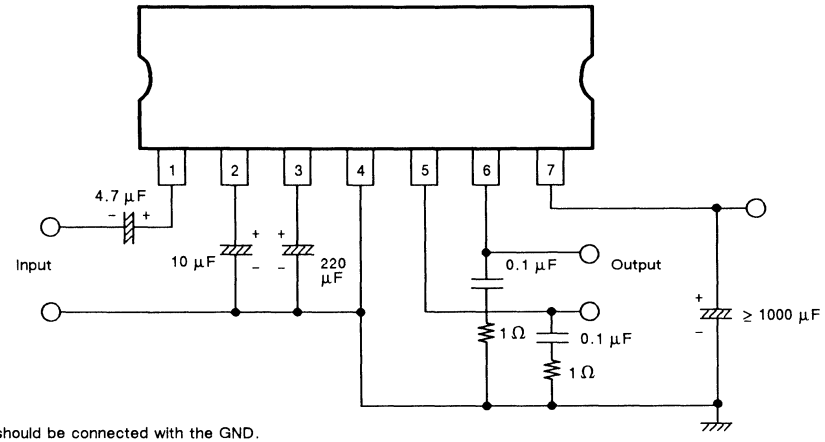
3

ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2V, R_L = 4Ω, f = 1KHz)

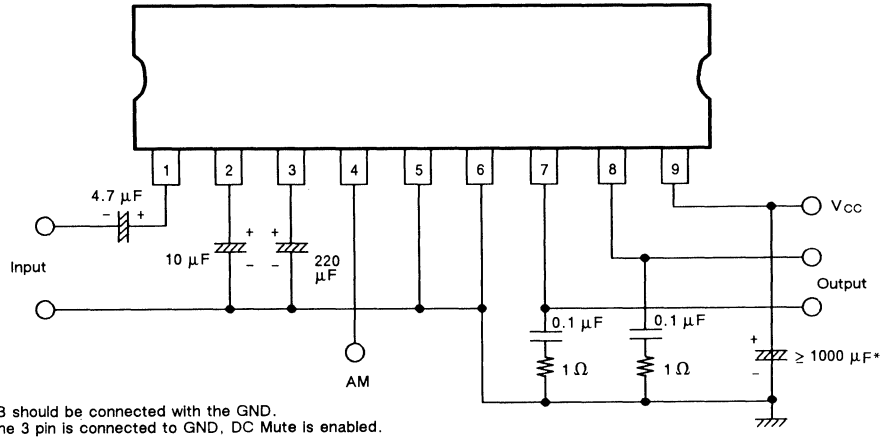
Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_Q	V_{IN} = 0V R_L = ∞	–	80	160	mA
Voltage Gain	A_V	–	45	47	49	dB
Output Power	P_O	THD = 10%	10	14	–	W
		THD = 1%	–	10	–	
Total Harmonic Distortion	THD	P_O = 1W	–	0.07	0.5	%
Output Noise Voltage	V_{NO}	R_g = 0Ω BW = 20Hz to 20KHz	–	0.3	–	mV
		R_g = 10KΩ BW = 20Hz to 20KHz	–	0.5	1.0	
Input Resistance	R_{IN}	–	20	30	–	kΩ
Output Offset Voltage	V_{OFF}	–	–	±0.1	±0.3	V
DC Mute Supply Current	I_{CCQ}	V_{3pin} = 0V	–	15	–	mA
Audio Mute Attenuation	–	MB3734 Only	–	60	–	dB

Fig. 3 – MB3732 TEST CIRCUIT



TAB should be connected with the GND.

Fig. 4 – MB3734 TEST CIRCUIT



TAB should be connected with the GND.
If the 3 pin is connected to GND, DC Mute is enabled.

NOTE: *When operation is unstable due to board design, insert 0.1 F condenser between V_{CC} and GND and between both outputs respectively, so that the unstable operation will be restrained.

3

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 5 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

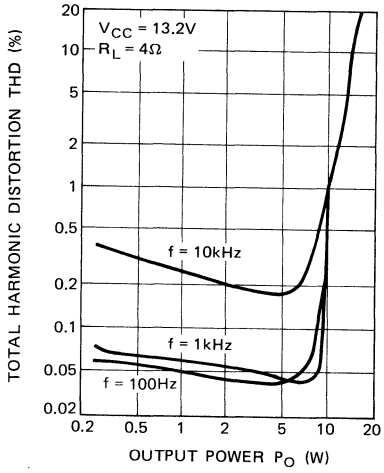


Fig. 6 – TOTAL HARMONIC DISTORTION vs. FREQUENCY

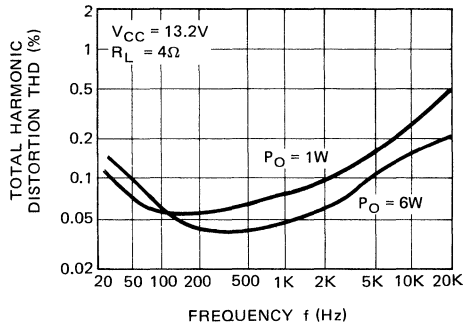


Fig. 7 – OUTPUT POWER vs. FREQUENCY

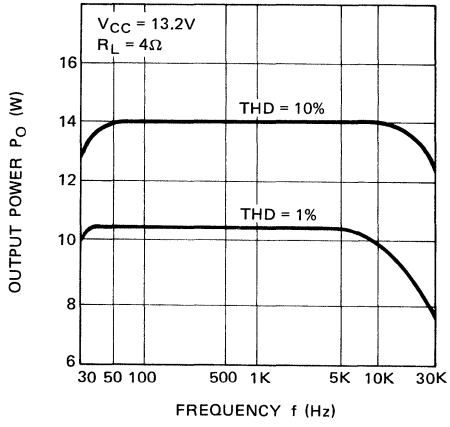
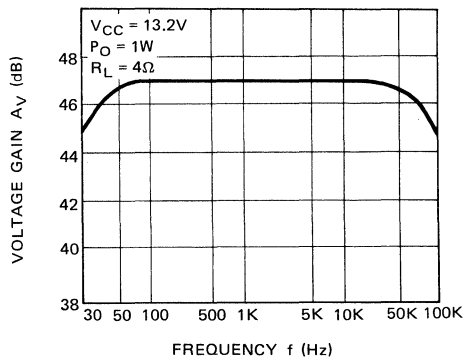


Fig. 8 – VOLTAGE GAIN vs. FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Fig. 9 – POWER DERATING CURVE (MB3732)

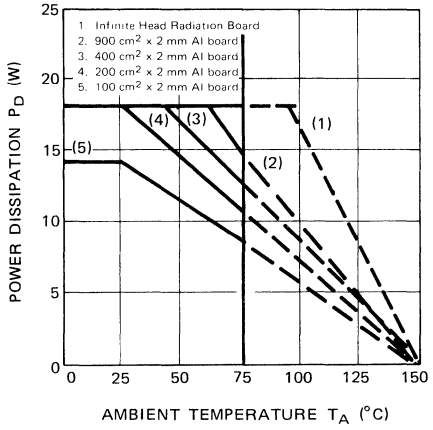
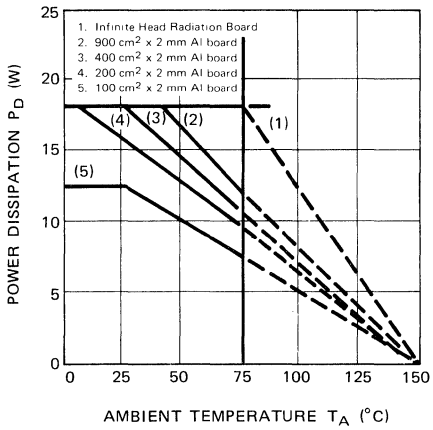


Fig. 10 – POWER DERATING CURVE (MB3734)

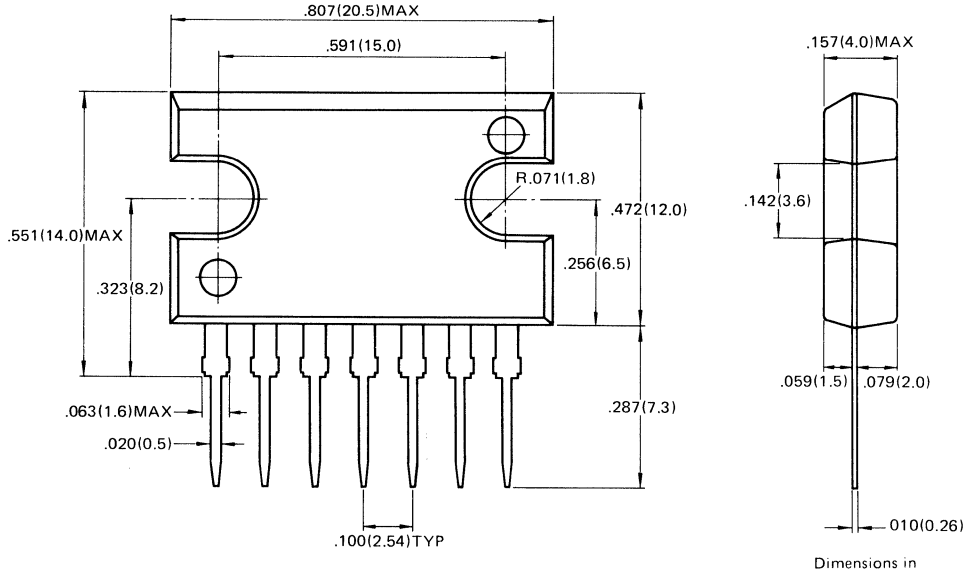


3

3

PACKAGE DIMENSIONS

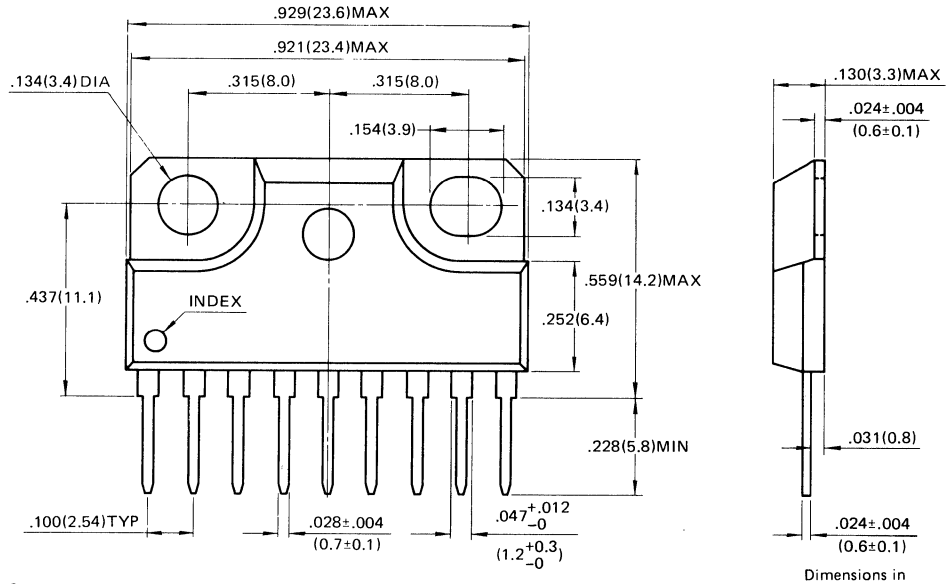
7-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-07P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

9-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-09P-M02)



Dimensions in inches (millimeters)

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Printed in Japan PV0050-887A2

FUJITSU

20 WATT BTL AUDIO POWER AMPLIFIER

MB3733

April 1988
Edition 2.0

20 WATT BTL AUDIO POWER AMPLIFIER

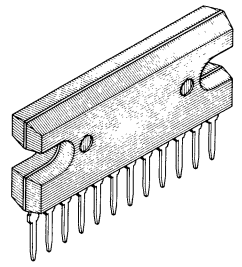
3

The Fujitsu MB3733 is designed for a low-frequency high power amplifier with internal BTL (Balanced Transformer less) circuitry. Suitable for care stereos, the MB3733 is packed in a small plastic 12-pin Single In-Line Package (SIP) which has low thermal resistance. Designing for heat radiation can be executed easily.

The device requires few external components, so high density mounting is optimized.

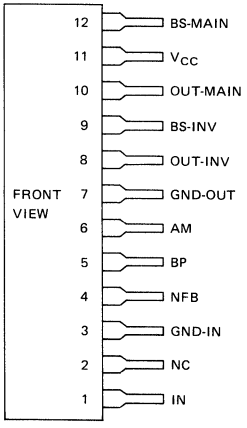
The MB3733 contains a filtering circuitry for power-on pop noise and various protection circuits.

- High Power Output: 20W with $R_L = 4\Omega$
- Minimum External Components
- Samll Plastic 12-pin Single In-Line Package
- Low Thermal Resistance
- Various Protection Circuitries:
  - Power Supply Surge Protection
  - Excess Voltage Protection
  - Load Short Protection
  - DC Short Protection for Outputs, Power Supply pin, and Ground pin
- Low Power-on Pop Noise
- Separated Ground pins for Input/Output
- Audio Mute Function
- Low Total Harmonic Distortion: 0.07% typ.



PLASTIC PACKAGE
SIP-12P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

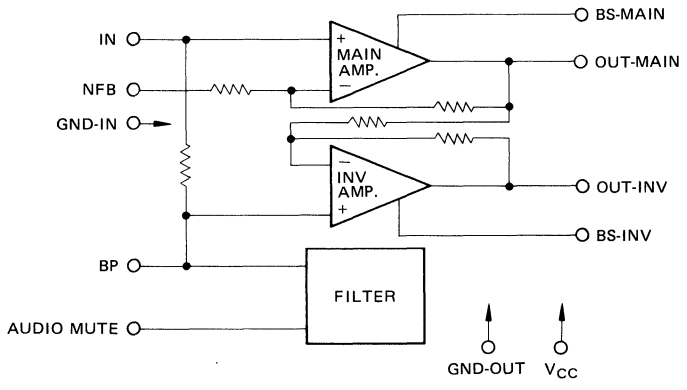
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge Voltage)	V_{CCS}	50*	V
Peak Output Current	I_O (Peak)	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature (Case)	T_C	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +150	°C

NOTE: * $t_s \leq 0.2$ (s), $t_r \geq 1$ (ms)

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB3733 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Operating Temperature (Case)	T_C	-20 to +75	°C

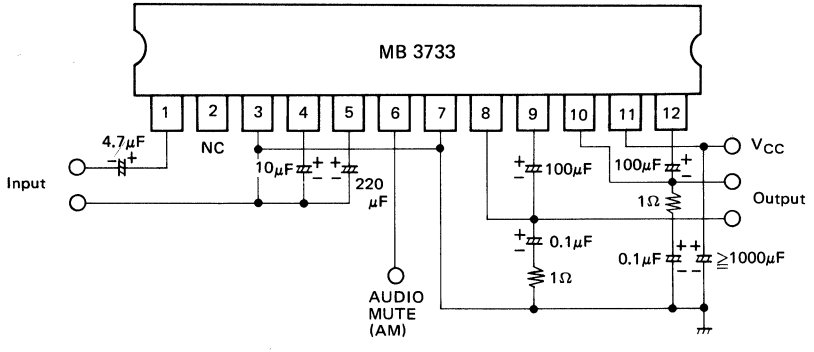
3

ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2V, R_L = 4Ω, f = 1kHz)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	V_{IN} = 0V, R_L = ∞	I_Q		80	160	mA
Voltage Gain		A_V	45	47	49	dB
Output Power	THD = 10%	P_{O1}	16	20		W
	THD = 1%	P_{O2}		14		W
Total Harmonic Distortion	P_O = 1W	THD		0.07	0.5	%
Output Noise Voltage	R_g = 0Ω, BW = 20 to 20kHz	V_{NO1}		0.3		mV
	R_g = 10kΩ, BW = 20 to 20kHz	V_{NO2}		0.5	1.0	mV
Input Resistance		R_{IN}	20	30		kΩ
Output Offset Voltage		V_{OFFSET}		±0.1	±0.3	V
Supply Current in DC MUTE mode	BP = 0V	I_{CCQ}		15		mA
AUDIO MUTE Attenuation	AM = 0V			50		dB

Fig. 2 – MEASUREMENT CIRCUIT



Note: When BP is grounded, DC Muting can be used. When AM is grounded, AUDIO Muting can be used.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

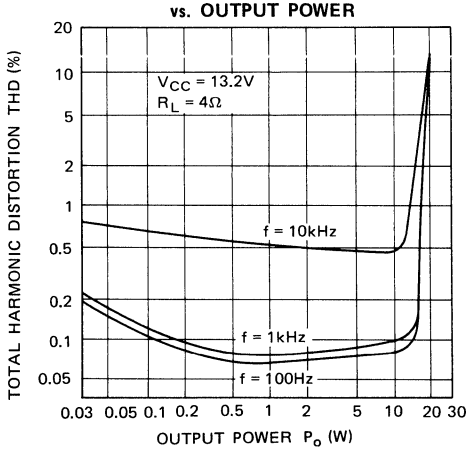


Fig. 4 – TOTAL HARMONIC DISTORTION vs. FREQUENCY

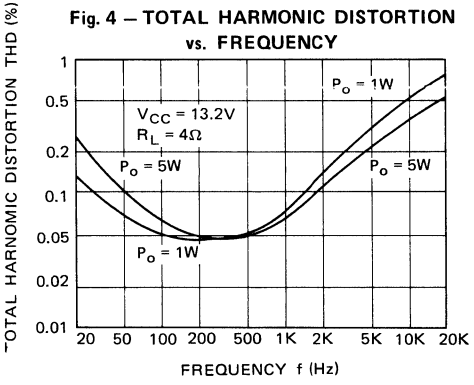


Fig. 5 – VOLTAGE GAIN vs. FREQUENCY

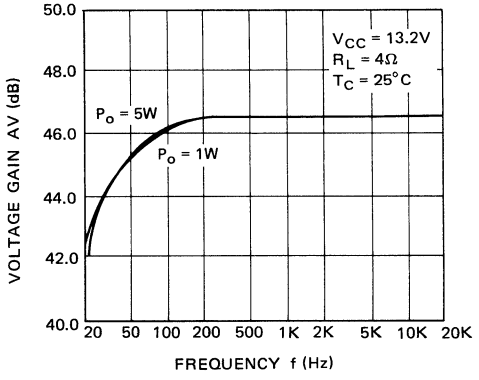
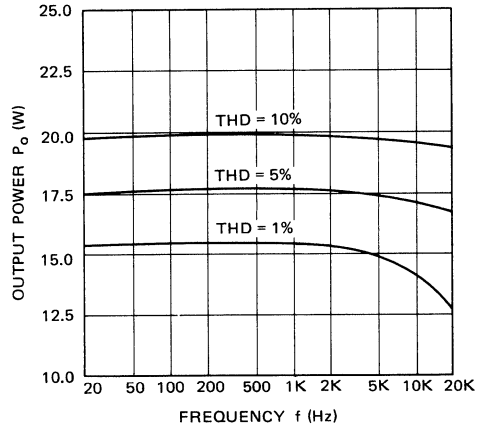


Fig. 6 – OUTPUT POWER vs. FREQUENCY



3

Fig. 7 – POWER DISSIPATION/POWER SUPPLY CURRENT vs. OUTPUT POWER

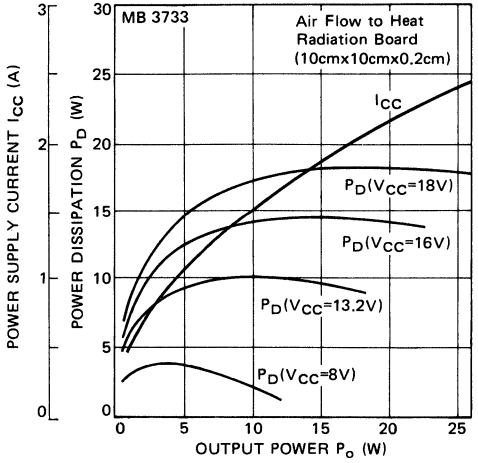
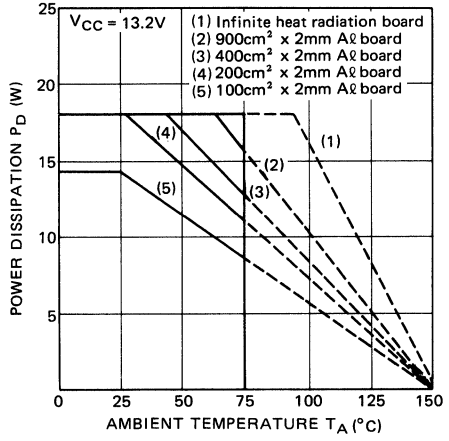


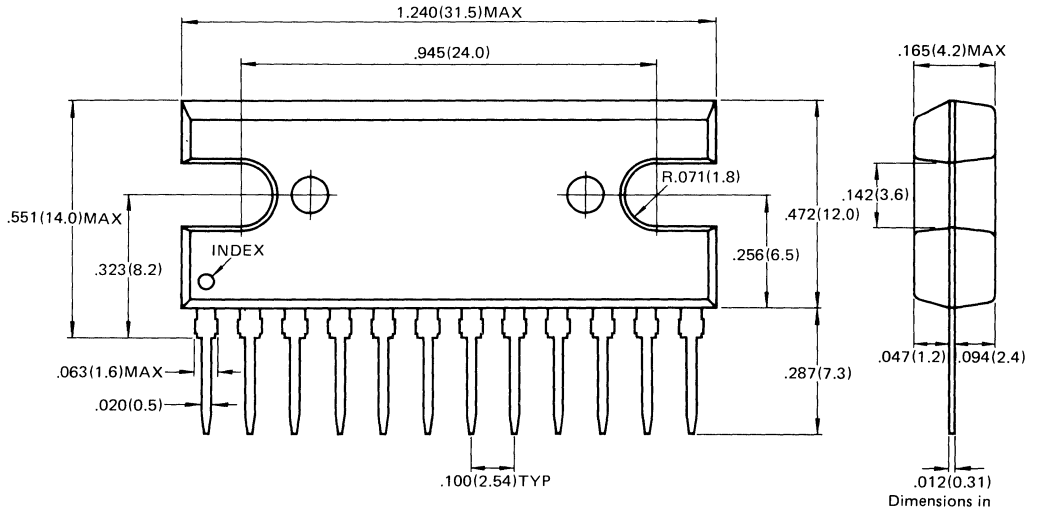
Fig. 8 – POWER DERATING CURVES



3

PACKAGE DIMENSIONS

12-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE NO.: SIP-12P-M01)



FUJITSU

20 WATT BTL AUDIO POWER AMPLIFIER

MB 3735

April 1987
Edition 2.0

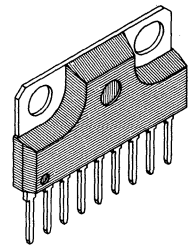
20 WATT BTL AUDIO POWER AMPLIFIER

3

The Fujitsu MB 3735 is designed for a low-frequency high-power amplifier with internal BTL (Balanced Transformer less) circuitry. The MB 3735 is packed in a small plastic 9-pin Single In-Line Package (SIP) which has low thermal resistance, so that a deseign for heat radiation can be performed with low cost.

Also, the MB 3735 requires such a few external components, so that it can be mounted on printed circuit board with high density.

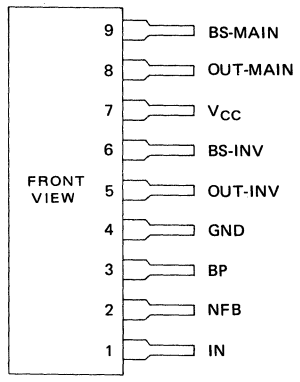
The MB 3735 contains a filtering circuitry for power-on pop noise and various protection circuits.



PLASTIC PACKAGE
SIP-09P-M02

- High Power Output: 20W with $R_L = 4\Omega$
- Minimum External Components
- Small Plastic 9-pin Single In-Line Package
- Low Thermal Resistance
- Various Protection Circuitries:
  - Power Supply Surge Protection
  - Excess Voltage Protection
  - Load Short Protection
  - DC Short Protection for Outputs, Power Supply pin, and Ground pin
- Low Power-on Pop Noise

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

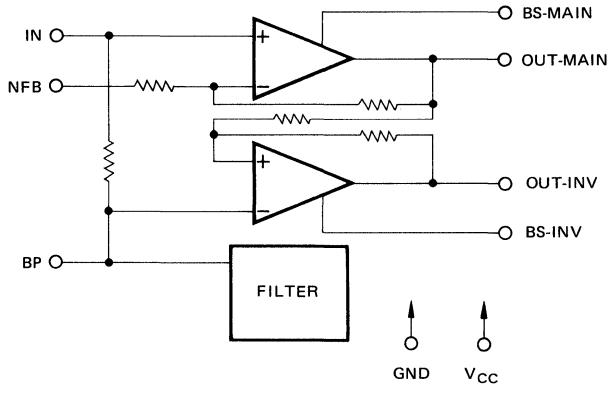
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge Voltage)	V_{CCS}	50*	V
Peak Output Current	$I_{O\,(Peak)}$	4.5	A
Power Dissipation	P_D	18	W
Operation Temperature	T_C	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +150	°C

NOTE: * $t_s \leq 0.2$ (s), $t_r \geq 1$ (ms)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM of MB 3735



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Case Temperature	T_C	−20 to +75	°C

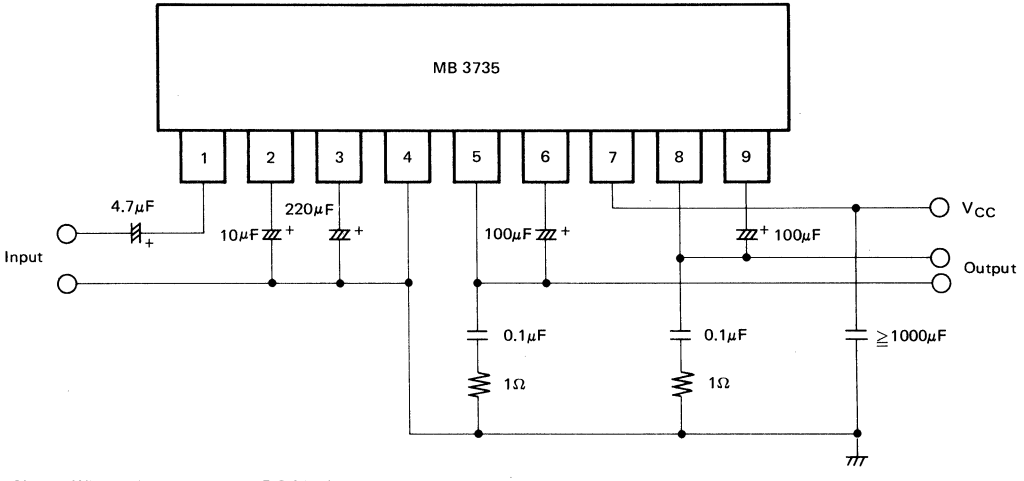
3

ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2V, R_L = 4Ω, f = 1kHz)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Quescent Power Supply Current	V_{IN} = 0V, R_L = ∞	I_Q		80	160	mA
Voltage Gain		A_V	45	47	49	dB
Output Power	THD = 10%	P_{O1}	16	20		W
	THD = 1%	P_{O2}		14		W
Total Harmonic Distortion	P_O = 1W	THD		0.07	0.5	%
Output Noise Voltage	R_g = 0Ω, BW = 20 Hz to 20 kHz	V_{NO1}		0.3		mV
	R_g = 10kΩ BW = 20 Hz to 20 kHz	V_{NO2}		0.5	1.0	mV
Input Resistance		R_{IN}	20	30		kΩ
Output Offset Voltage		V_{OFFSET}		±0.1	±0.3	V
Supply Current in DC MUTE mode	BP = 0V	I_{CCO}		15		mA

Fig. 2 – MEASUREMENT CIRCUIT



Note: When BP is grounded, DC Muting can be used.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

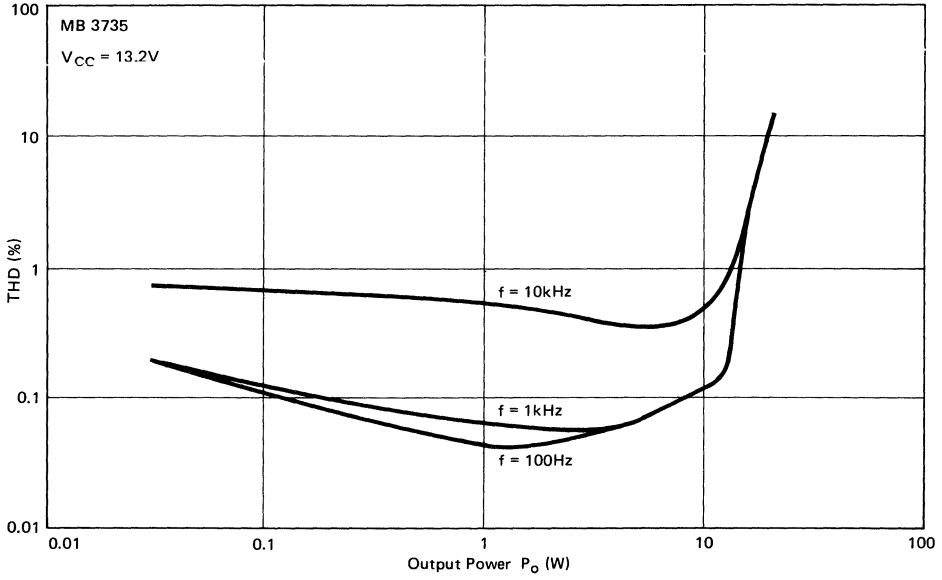
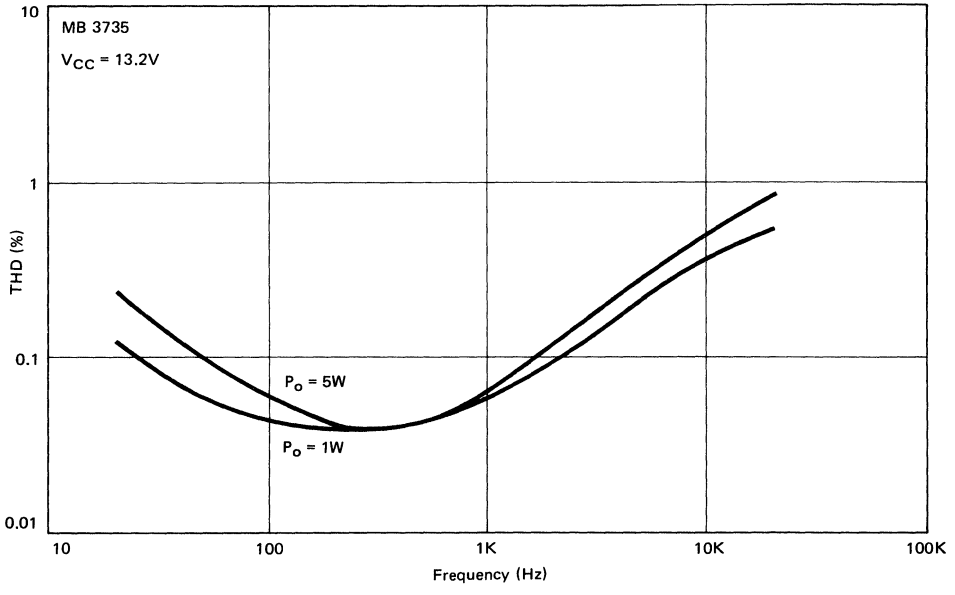


Fig. 4 – TOTAL HARMONIC DISTORTION vs. FREQUENCY



3

Fig. 5 – GAIN vs. FREQUENCY

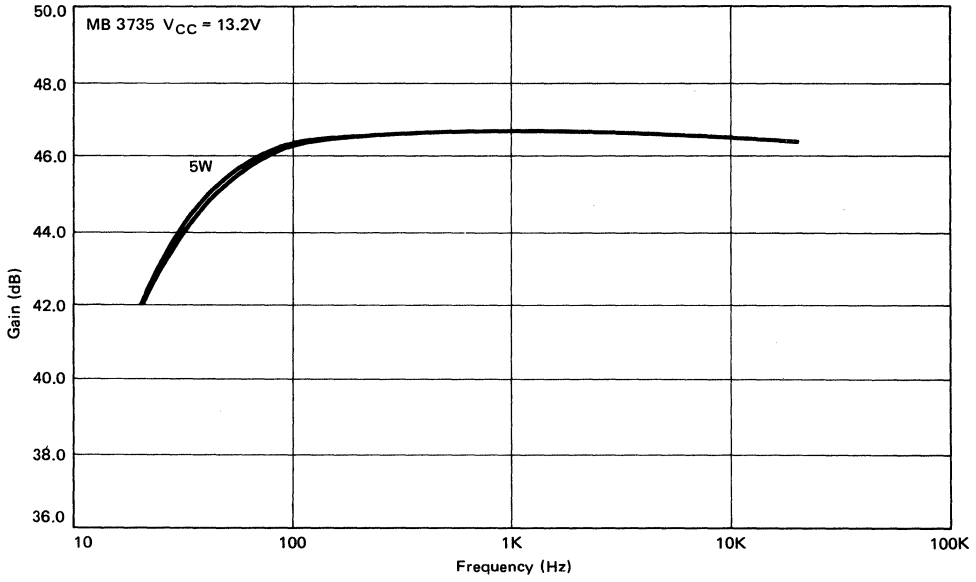
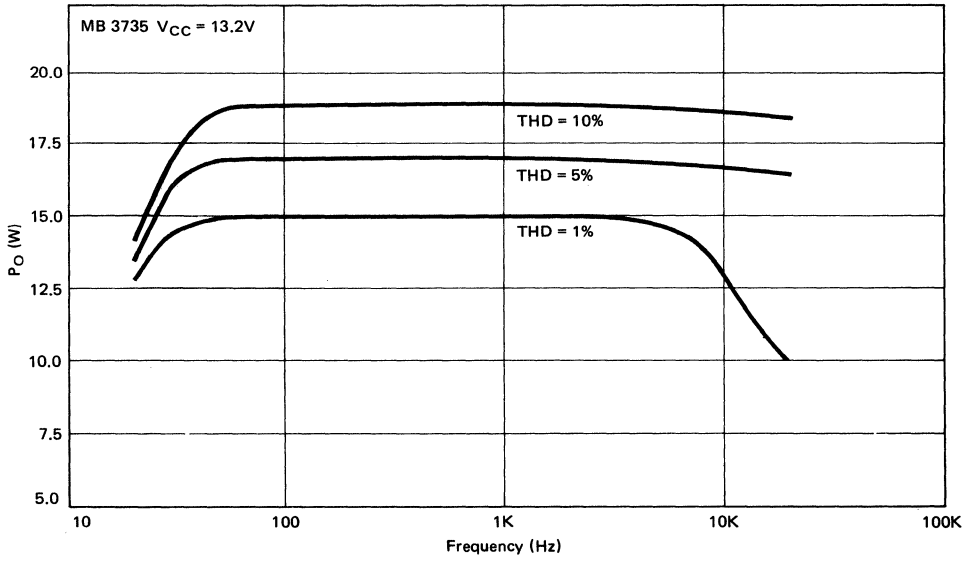
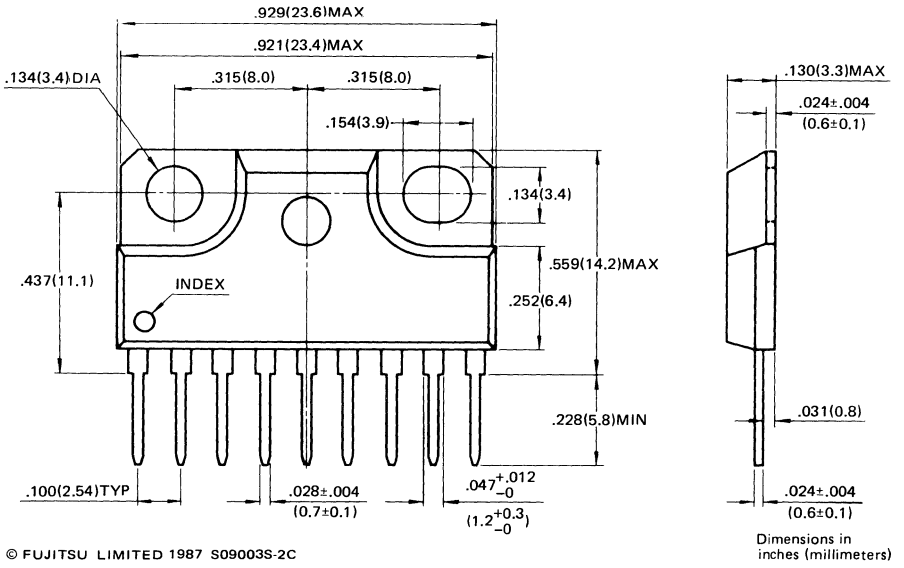


Fig. 6 – POWER BAND WIDTH



PACKAGE DIMENSIONS

9-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-09P-M02)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

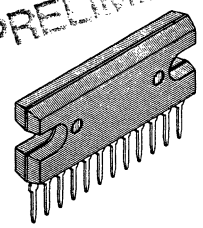
MB3736

TS581-A87Y
November 1987

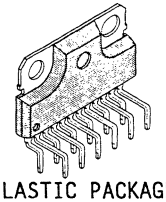
15 W BTL AUDIO POWER AMPLIFIER

PRELIMINARY

The Fujitsu MB3736 is designed for a low-frequency high-power amplifier with internal BTL(Balanced Transformer Less) circuitry. The MB3736 is packed in 12 pin plastic Single in line small package or 12 pin plastic Zigzag in line small package and requires a few external components, this enables high density mounting. Design for heat radiation is easy because thermal resistance is low.
The MB3736 is internal power-on pop noise protection circuitry and various protection circuitry. The device is suitable best for car-stereo.



PLASTIC PACKAGE
SIP-12P-M01



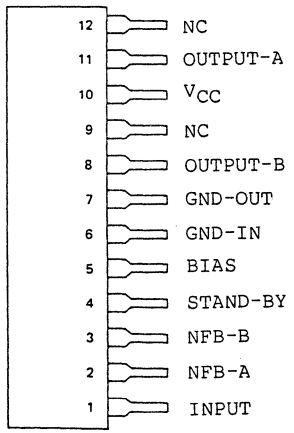
PLASTIC PACKAGE
ZIP-12P-M01

3

- High Power : 15 W typ at 4 Ω
- Minimum External Components
- Stand-by Function (High active)
- Various Protection Circuitry
  - Power Supply Surge Protection
  - Over Voltage Protection
  - Load Short Protection
  - Output pin-to-DC Short Protection
  - Thermal Protection
- Low Power-on Pop Noise
- Low Thermal Resistance
  - 4°C/W SIP Package
  - 3°C/W ZIP Package
- Package
  - 12 pin Plastic SIP package (Suffix:-PS)
  - 12 pin Plastic ZIP package (Suffix:-PSZ)

PIN ASSIGNMENT

(Front View)



ABSOLUTE MAXIMUM RATINGS (See NOTE)

(T_C = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge)	V_{CCS}	50 *	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	30	W
Operating Temperature (Case)	T_C	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note:
* $t_S \leq 0.2$ sec, $t_r \geq 1$ msec

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB3736 BLOCK DIAGRAM

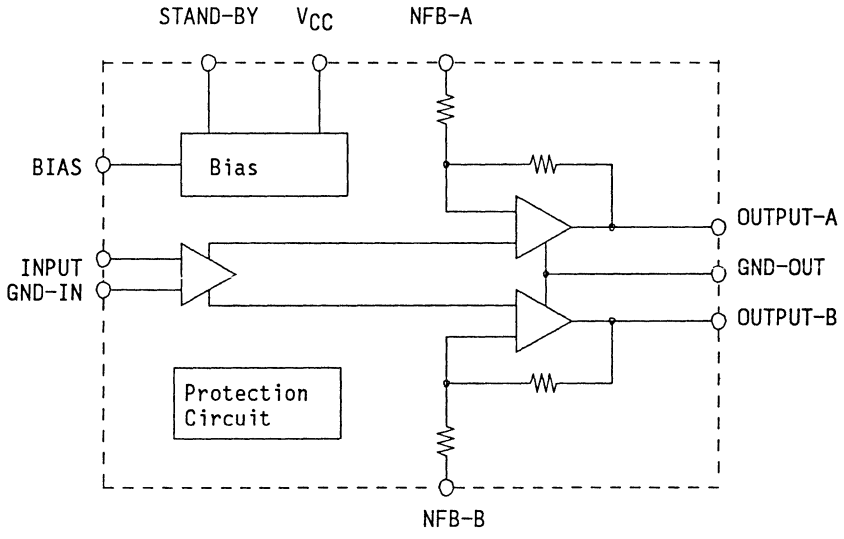
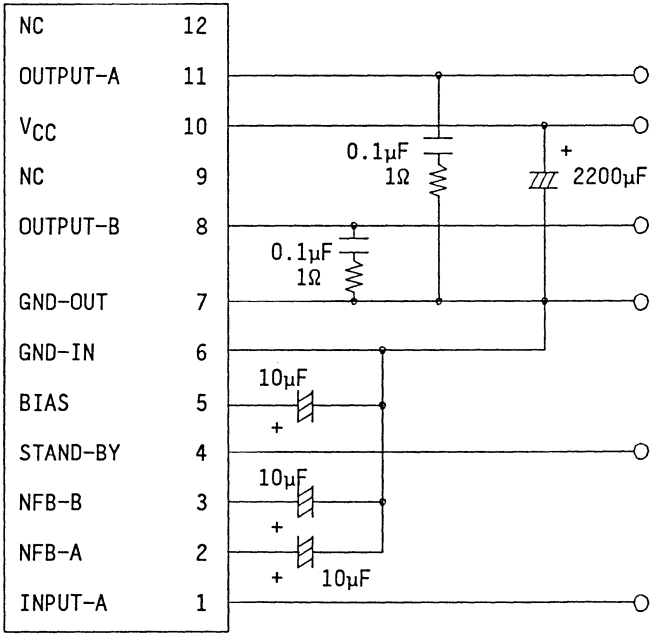


Fig.2 - MB3736 TEST CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	9 to 16	V
Operating Temperature (Case)	T_C	-20 to +75	°C

ELECTRICAL CHARACTERISTICS (T_C=25°C, V_{CC}=13.2V, f=1kHz, R_L=4Ω)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_{CC}	V_{IN}=0V, R_L=∞		100	200	mA
Voltage Gain	A_V		43	45	47	dB
Output Power	P_O	THD=10%, R_L=4Ω	12	15		W
		THD=10%, R_L=2Ω	12			W
Total Harmonic Distortion	THD	P_O=5W		0.04	0.5	%
Output Noise Voltage	V_{NO}	Rg=10kΩ, BW=20 to 20kHz		0.4	1.0	mV
Input Resistance	R_{IN}		20	30		kΩ
Output Offset Voltage	V_{OFF}			±0.1	±0.3	V
Power Supply Current at Stand by mode				1	50	μA
Input Voltage at Stand-by Pin	V_{SBH}	Operation	2.4		V_{CC}	V
	V_{SBL}	Stand-by	0		0.4	V
Ripple Rejection Ratio				50		dB

TYPICAL CHARACTERISTICS CURVES

Fig.3 - TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

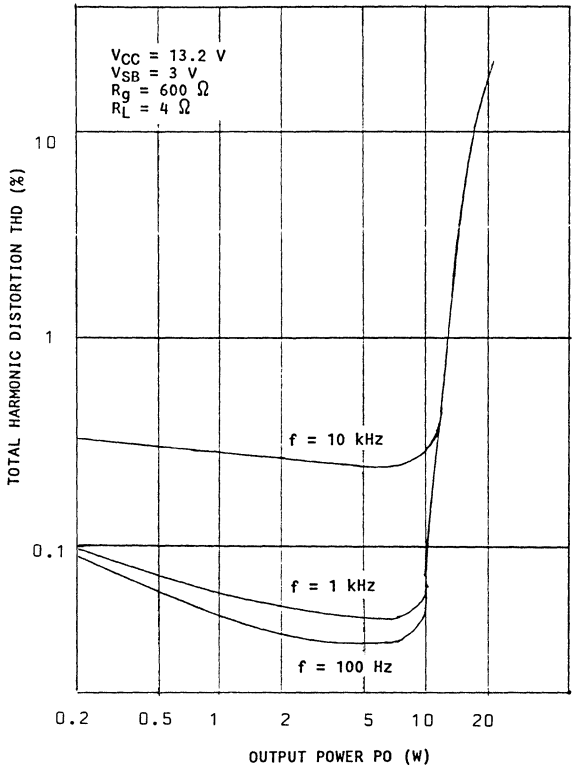


Fig.4 - TOTAL HARMONIC DISTORTION vs. FREQUENCY

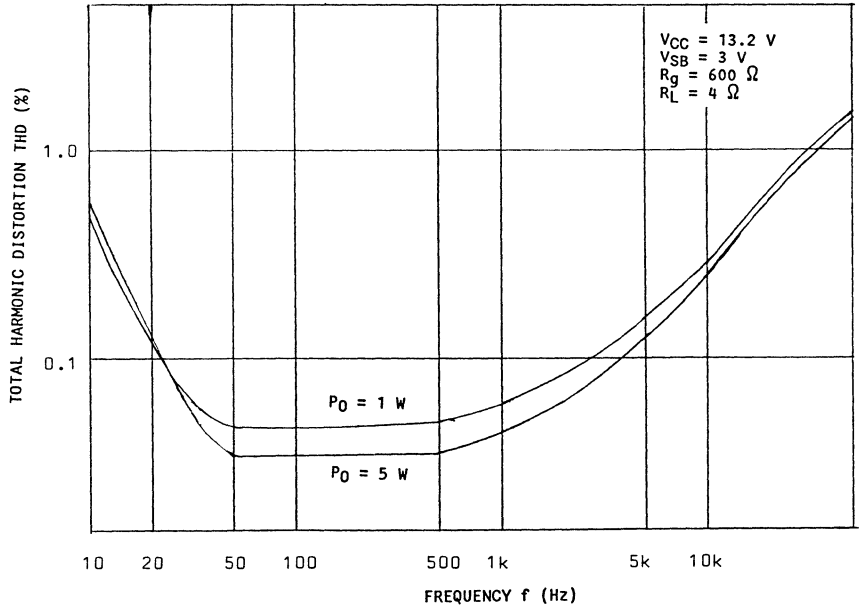


Fig.5 - VOLTAGE GAIN vs. FREQUENCY

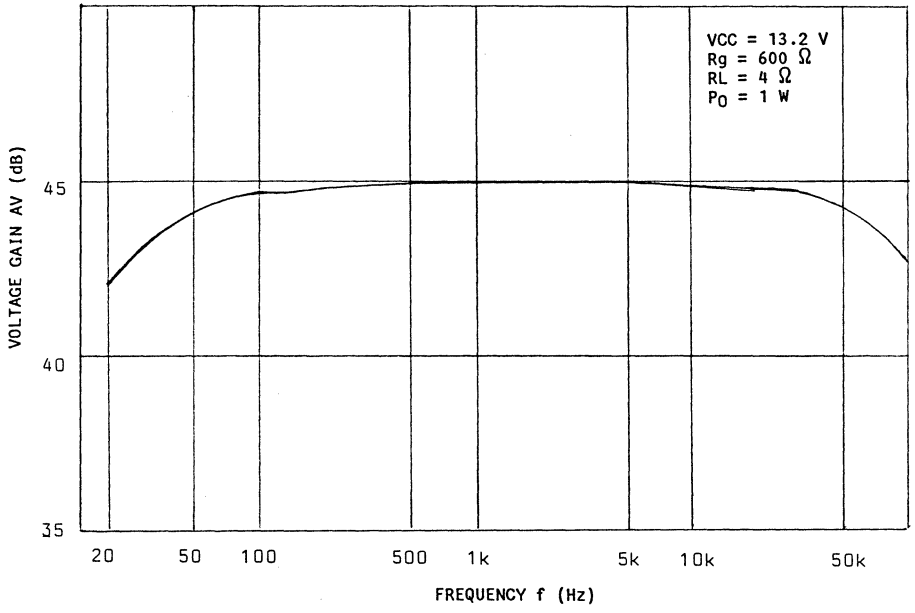


Fig.6 - POWER SUPPLY RIPPLE REJECTION vs. FREQUENCY

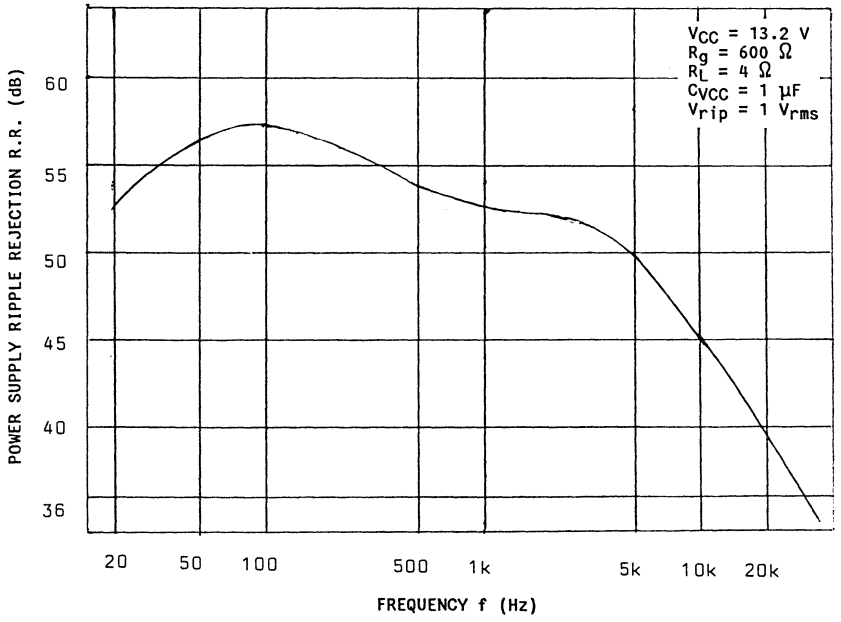


Fig.7 - POWER DISSIPATION vs. OUTPUT POWER

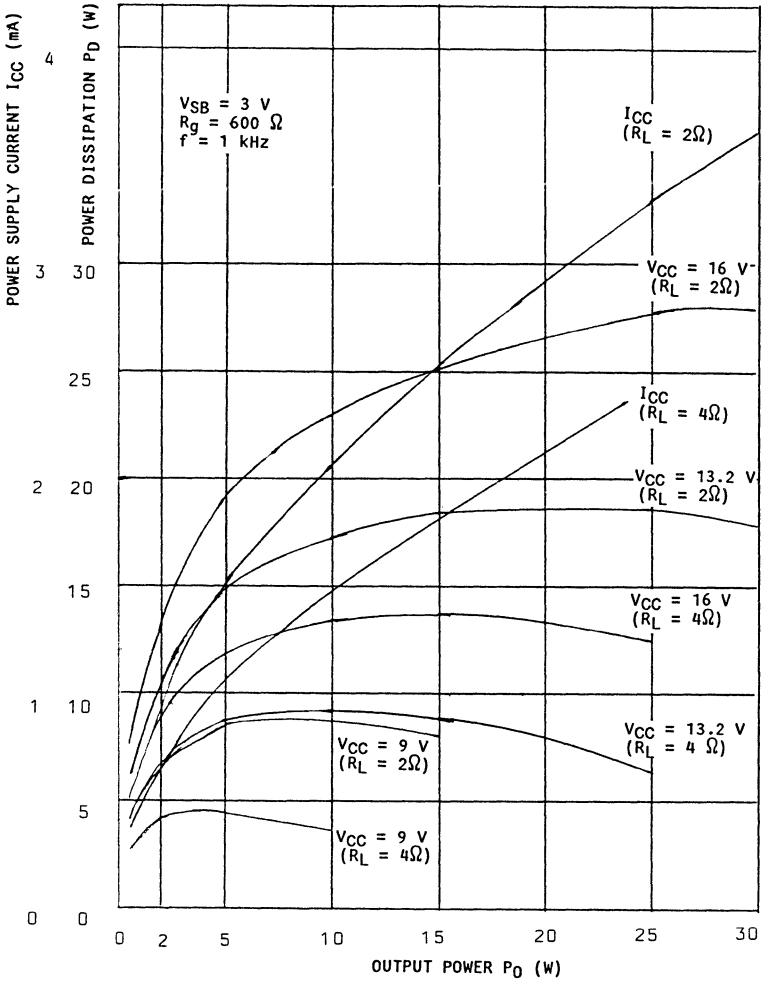


Fig.8 - POWER DERATING CURVES
(SIP-12 PACKAGE)

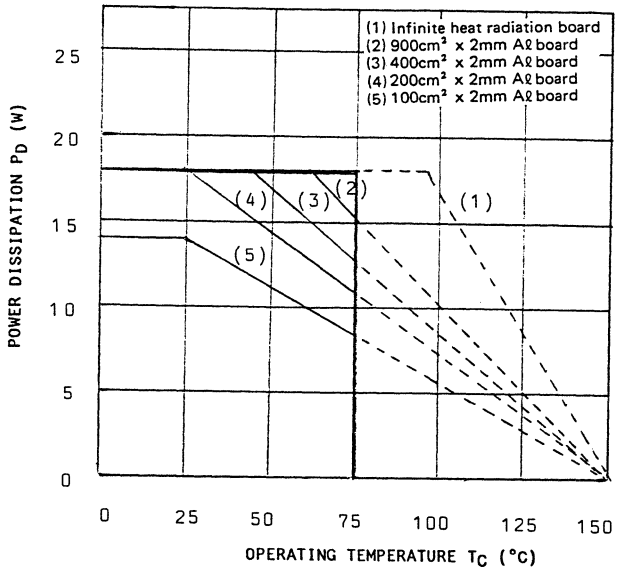
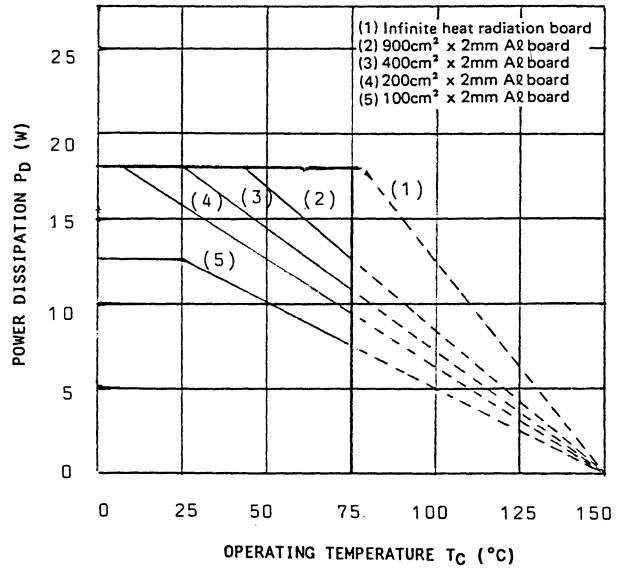
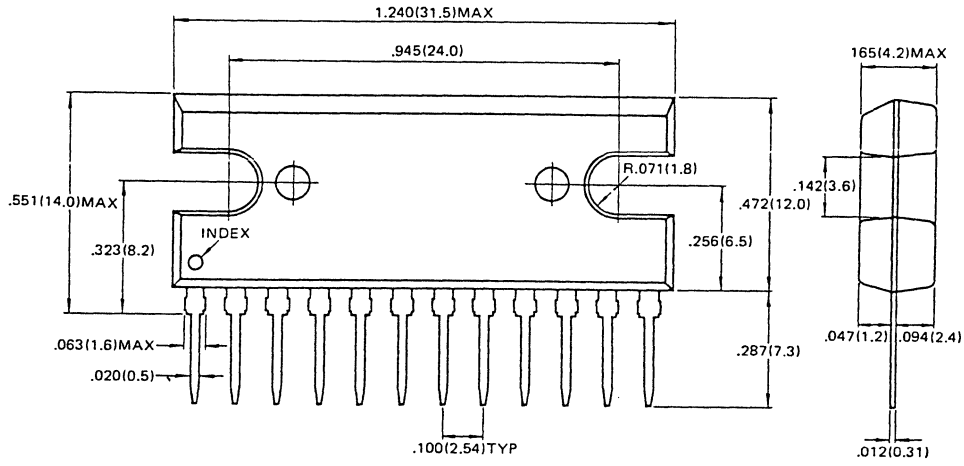


Fig.9 - POWER DERATING CURVES
(ZIP-12 PACKAGE)



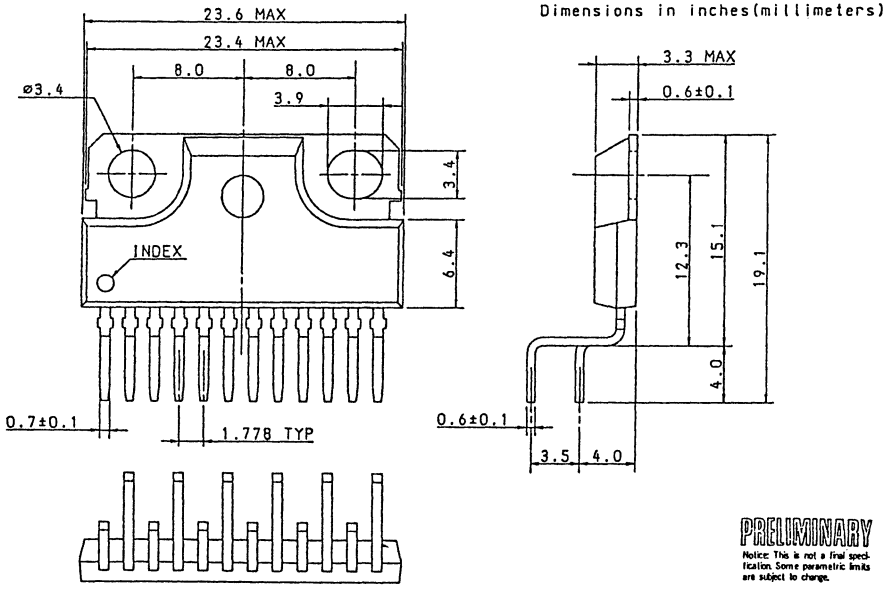
12-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE NO.: SIP-12P-M01)



Dimensions in inches (millimeters)

12 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE.

Dimensions in inches(millimeters)



PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

FUJITSU

MB3737

TS527-C885
May 1988

23 W BTL AUDIO POWER AMPLIFIER

The Fujitsu MB3737 is designed for a low-frequency high-power amplifier with internal BTL(Bridged Output Trans formar-less) Circuitry.

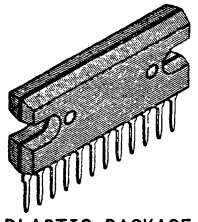
Suitable for car stereos, the MB3737 is packed in 12 pin plastic Single in line small package or 12 pin plastic Zigzag in line small package which has low thermal resistance (SIP: 3°C/W, ZIP: 4°C/W). Design for heat radiation can be executed easily.

The MB3737 requires few external components, so high density mounting is optimized.

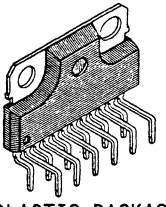
3

The MB3737 contains a power-on pop noise protection circuitry and various protection circuitry.

- High Output Power : 23 W typ at 4 Ω
- Minimum External Components
- Stand-by Function
- Various Protection Circuitry
  - Power Supply Surge Protection
  - Output pin-to-DC Short Protection
  - Over Voltage Protection
  - Load Short Protection
  - Thermal Protection
- Low Power-on Pop Noise
- Package
  12 pin Plastic SIP package (Suffix:-PS)
  12 pin Plastic ZIP package (Suffix:-PSZ)



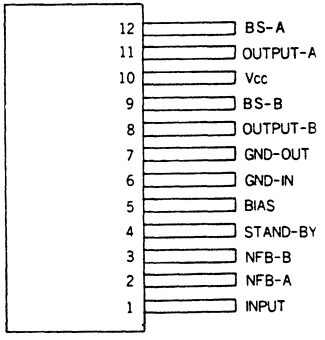
PLASTIC PACKAGE
SIP-12P-M01



PLASTIC PACKAGE
ZIP-12P-M01

PIN ASSIGNMENT

(Front View)



SIP-12P-M01

ZIP pin assignment:
please see page 7

ABSOLUTE MAXIMUM RATINGS (See NOTE)

(T_C = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge)	V_{CCS}	50 *	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	30	W
Operating Temperature (Case)	T_C	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note:
* $t_s \leq 0.2$ sec, $t_r \geq 1$ msec

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB3737 BLOCK DIAGRAM

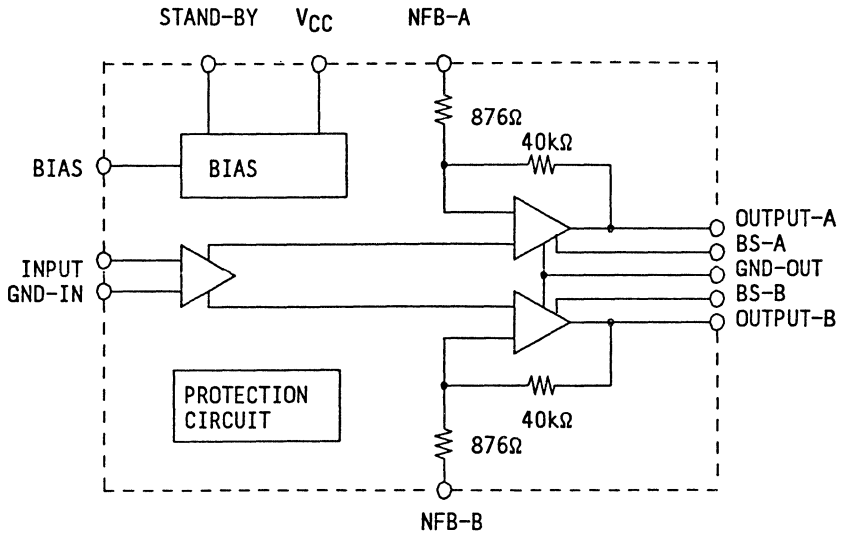
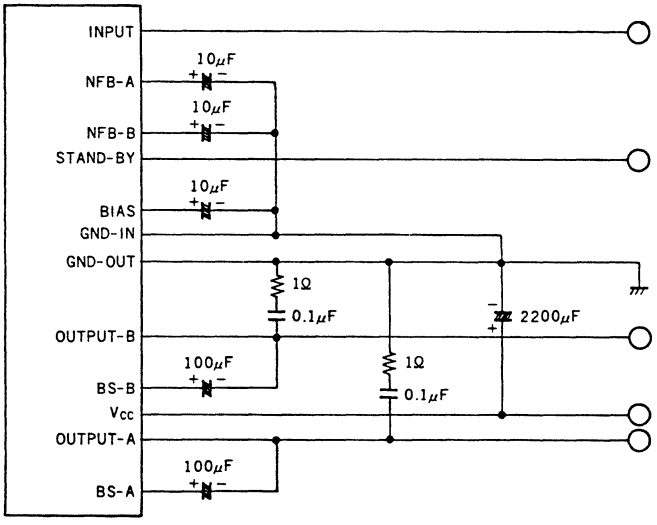


Fig.2 - MB3737 TYPICAL CONNECTION EXAMPLE



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	9 to 16	V
Operating Temperature (Case)	T_C	-20 to +75	°C

ELECTRICAL CHARACTERISTICS (T_C=25°C, V_{CC}=13.2V, f=1kHz, R_L=4Ω)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_{CCQ}	V_{IN}=0V, R_L=∞		100	200	mA
Voltage Gain	A_V		43	45	47	dB
Output Power	P_O	THD=10%, R_L=4Ω	18	23		W
		THD=10%, R_L=2Ω	18	26		W
Total Harmonic Distortion	THD	P_O=5W		0.04	0.4	%
Output Noise Voltage	V_{NO}	Rg=10kΩ, BW=20Hz to 20kHz		0.4	1.0	mV
Input Resistance	R_{IN}		20	30		kΩ
Output Offset Voltage	V_{OFF}			±0.1	±0.3	V
Power Supply Current at Stand by mode	I_{CCS}			1	50	μA
Ripple Rejection Ratio	RR	Vrip=1Vrms, f=1kHz Cpapcitor 1μF is connected between V_{CC} and GND	40	50		dB
Input Voltag, Stand-by Pin	V_{SBH}	Operation mode	2.4		V_{CC}	V
	V_{SBL}	Stand-by mode	0		0.4	V

TYPICAL CHARACTERISTICS CURVES

Fig.3 - TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

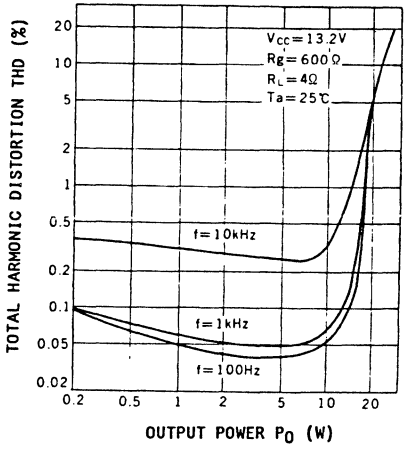


Fig.4 - TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

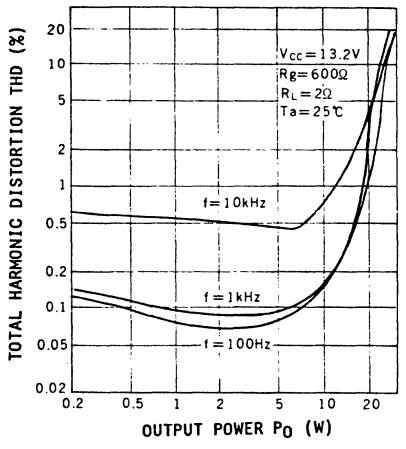


Fig.5 - TOTAL HARMONIC DISTORTION vs. FREQUENCY

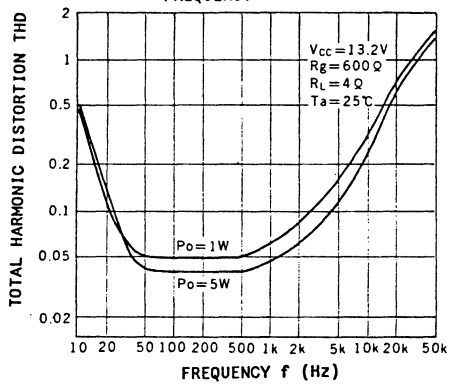


Fig.6 - VOLTAGE GAIN vs. FREQUENCY

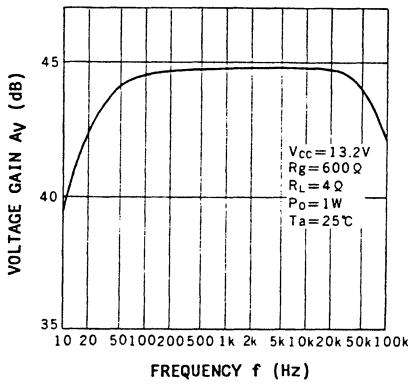


Fig.7 - OUTPUT POWER vs. FREQUENCY

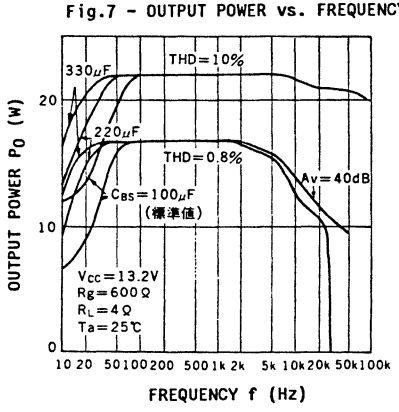


Fig.8 - TOTAL HARMONIC DISTORTION vs. SIGNAL SOURCE IMPEDANCE

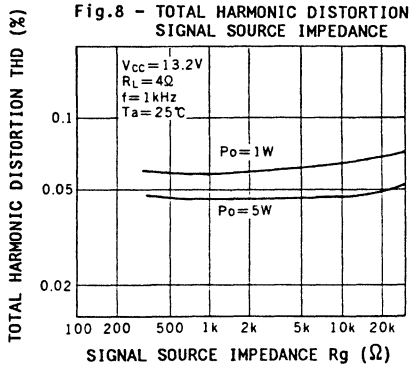


Fig.9 - OUTPUT NOISE VOLTAGE vs. SIGNAL SOURCE IMPEDANCE

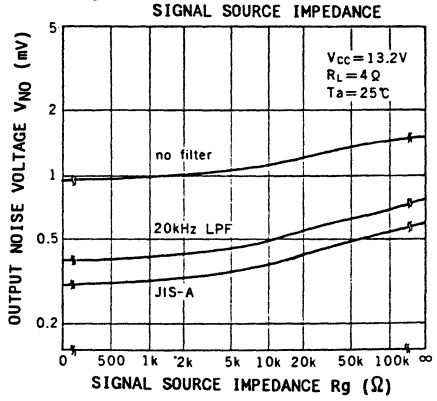


Fig.10 - RIPPLE REJECTION vs. REQUENCY

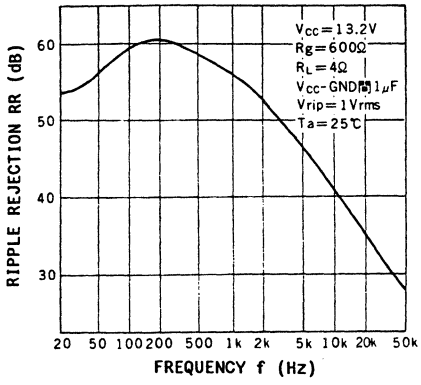


Fig.11 - POWER SUPPLY CURRENT/ POWER DISSIPATION vs. OUTPUT POWER

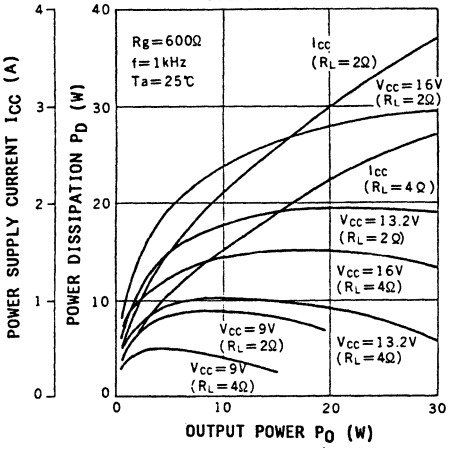


Fig.12 - OUTPUT POWER vs. LOAD RESISTANCE

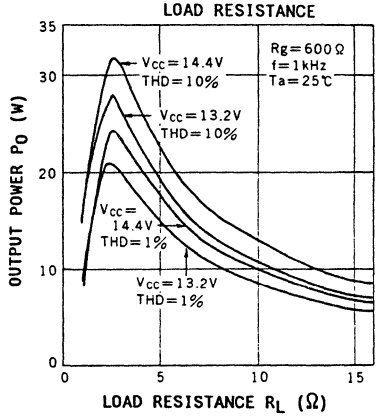


Fig.13 - OUTPUT POWER vs. FREQUENCY

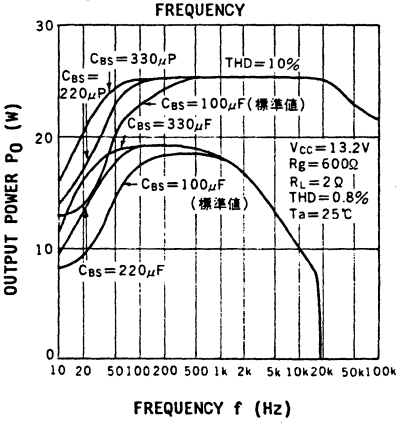
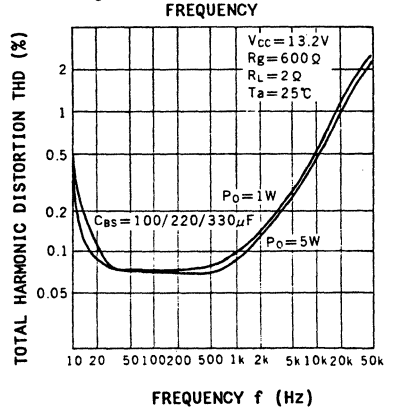
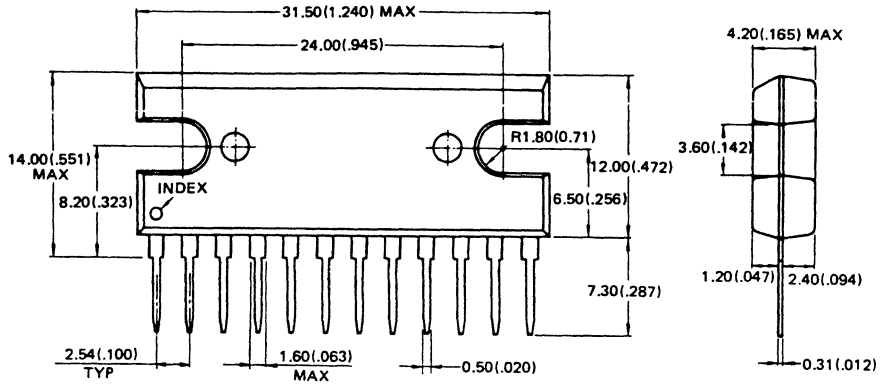


Fig.14 - TOTAL HARMONIC DISTORTION vs. FREQUENCY



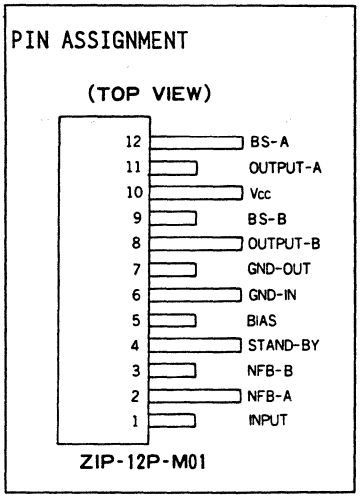
PACKAGE DIMENSIONS

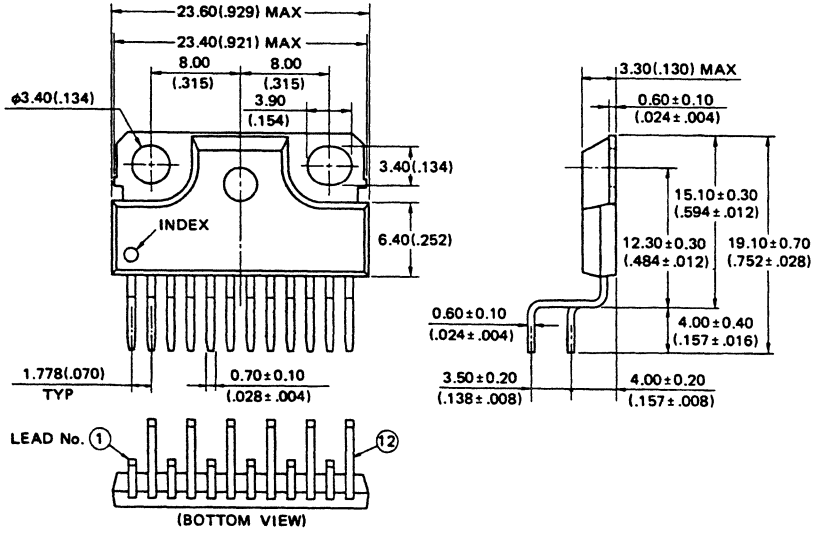


Dimensions in millimetres (inches)

3

PACKAGE DIMENSIONS





Dimensions in millimetres (inches)

FUJITSU

FM STEREO MULTIPLEX DEMODULATOR

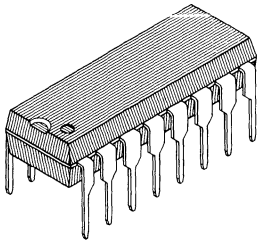
MB4104
MB4105

October 1987
Edition 1.0

FM STEREO MULTIPLEX DEMODULATOR

The Fujitsu MB4104/4105 is a monolithic FM stereo multiplex demodulator fabricated using Fujitsu's advanced bipolar technology. Using PLL circuitry, this device achieves stabie performance against the variance condition of external elements.

- Separation control circuit reduces noise, in a weak electrical field.
- PLL circuitry means less external elements.
- Reduced FM noise in weak electrical fields, with high cut control circuit.
- Low Distortion : 0.06% typical at 300 mV input.
- On-chip forced monaural, forced VCO stop, lamp driver, and audio muting circuits.
- Separate pilot signal and composite signal inputs MB 4105.
- 16-pin plastic DIP package (Suffix: -p)



PLASTIC PACKAGE
DIP-16P-M04

3

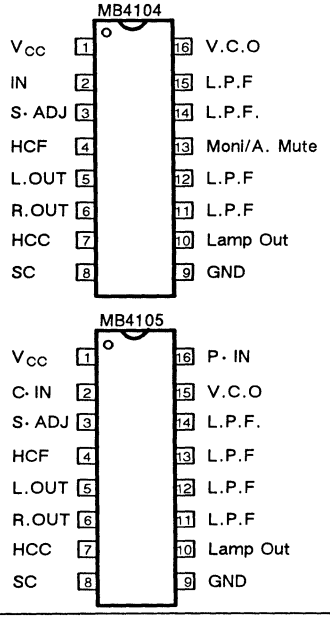
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	16	V
Lamp Drive Current	I_L	75	mA
Power Dissipation	P_D	520	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

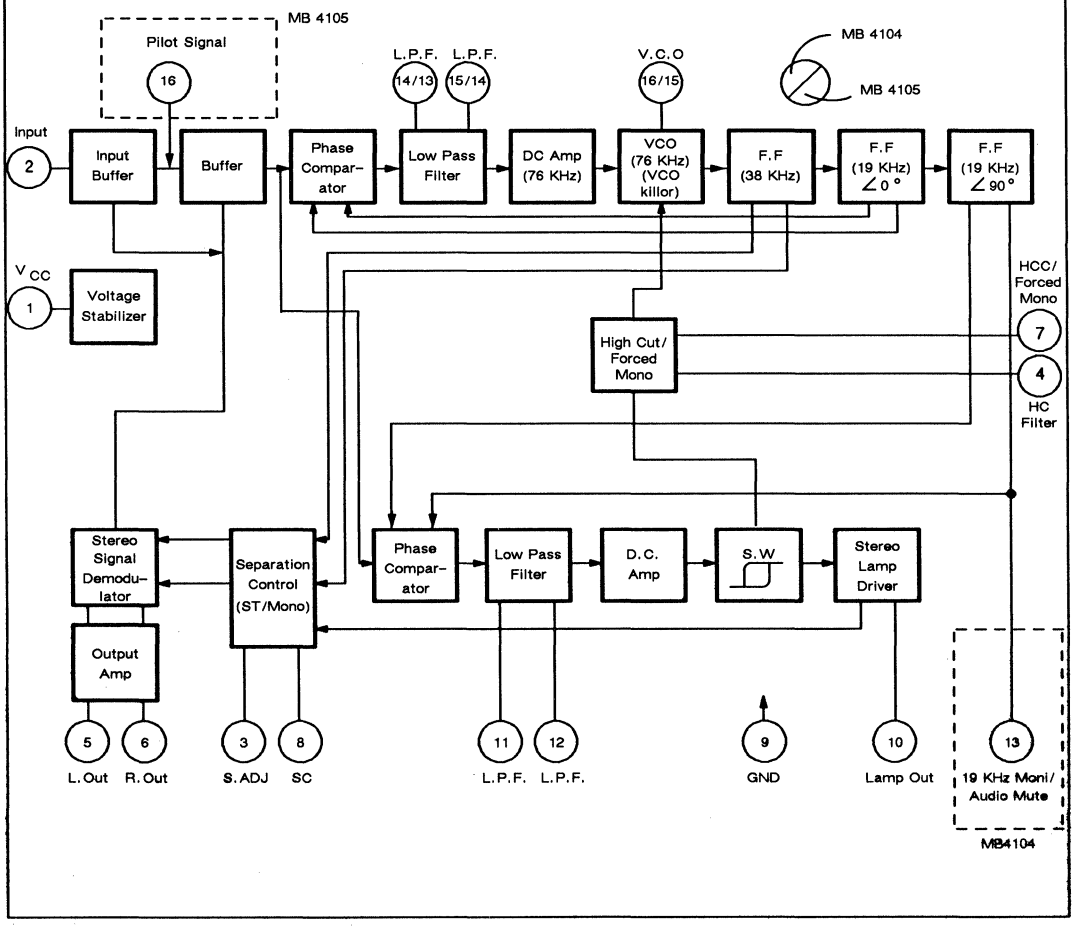
TOP VIEW



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 — MB4104/4105 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

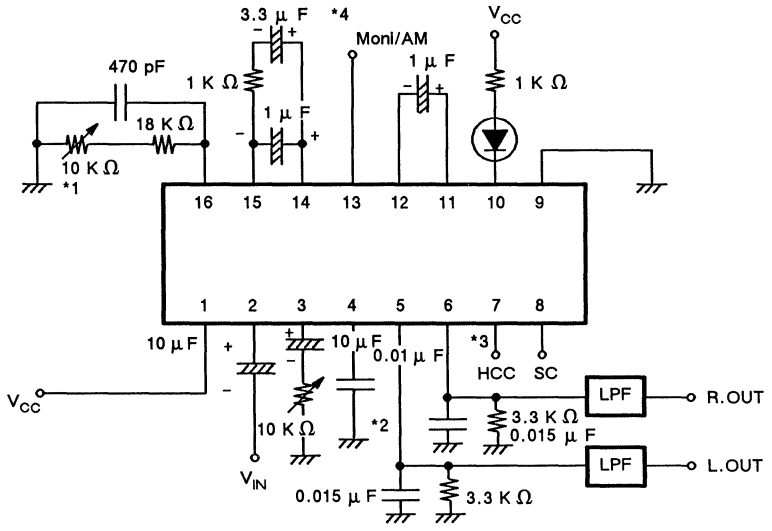
Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 14	V
Operating Temperature	T_A	-20 to +75	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, V_{IN} = 300 mVrms, f = 1 KHz, L + R = 90%, Pilot = 10%, T_A = 25°C)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_Q	V_{IN} = 0V	—	18	25	mA
Channel Separation	CS	—	40	55	—	dB
Total Harmonic Distortion	THD	Stereo	—	0.06	0.3	%
		Mono	—	0.06	0.3	%
Output Voltage	V_O	—	210	300	420	mVrms
Channel Balance	CB	—	—	0	1.5	dB
Lamp Level	—	Pilot Signal	5	8	12	mV
Lamp Hysteresis	—	Pilot Signal	—	4.5	7	dB
SCA Rejection Ratio	—	—	—	80	—	dB
S/N Ration	S/N	—	70	78	—	dB
Input Impedance	R_{IN}	—	20	30	—	kΩ
Capture Range	CR	Pilot = 30 mV	—	±4	—	%
Maximum Input Voltage	$V_{IN(MAX)}$	THD = 1%	600	1000	—	mVrms
SC Output Attenuation	—	V_8 = 0.6 V	-12	-6	-1	dB
SC Output Voltage	—	V_8 = 0.1 V	—	—	5	mV
HCC Output Attenuation 1	—	V_7 = 1.2 V	-3	-1	0	dB
HCC Output Attenuation 2	—	V_7 = 0.6 V	-18	-10	-2	dB
Power Supply Ripple Rejection Ration	R.R.	—	—	35	—	dB
Audio Mute Attenuation MB4104	—	V_{13} = 0.2 V	—	55	—	dB

3

Fig. 2 — MB4104 TEST CIRCUIT



Notes:

*1. VCO Free Running Frequency should be adjusted in order to output 19,000 KHz ± 10 Hz, at pin 13.

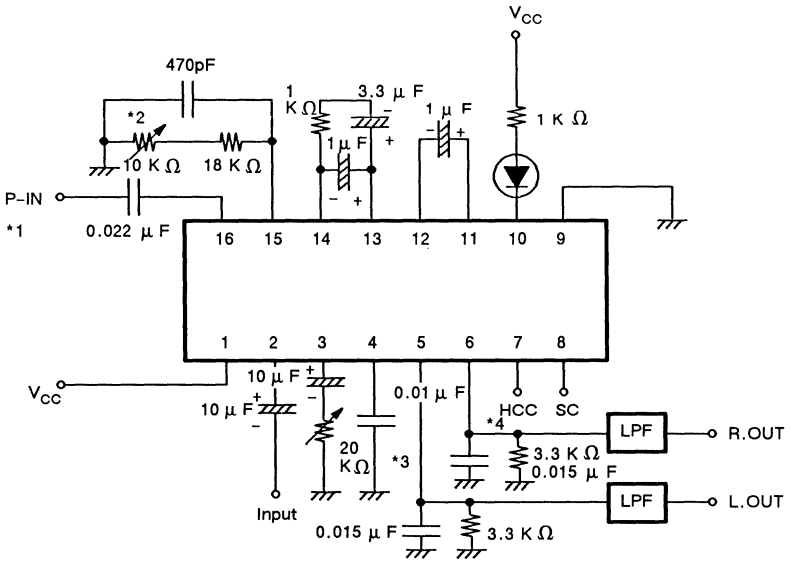
*2. The value is 100 μF when SC and HCC are measured.

*3. When over 7.0 V is applied to pin 7, the device is in forced monaural mode and VCO stops. If a voltage higher than V_{CC} is applied to pin 7, about 10 KΩ should be inserted.

*4. When pin 13 = GND, or is lower than 0.4 V, the device is in audio mute mode.

3

Fig. 3 — MB4105 TEST CIRCUIT



Notes:

*1. The pilot signal can be input to pin 16. Therefore input signal, without the pilot signal input to pin 2, makes the LPF design easier.

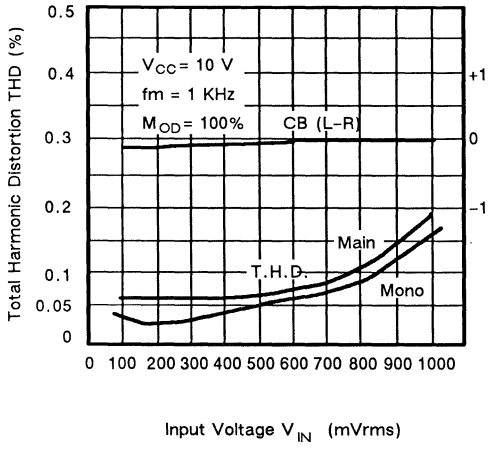
*2. VCO (76 KHz) signal should be adjusted.

*3. The value is 100 μF when SC and HCC are measured.

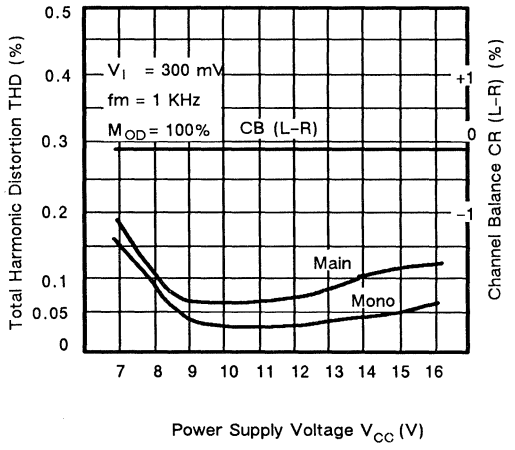
*4. When over 7.0 V is applied to pin 7, the device is in forced monaural mode and VCO stops. If the voltage higher than V_{CC} is applied to pin 7, about 10 KΩ should be inserted.

TYPICAL PERFORMANCE CHARACTERISTICS

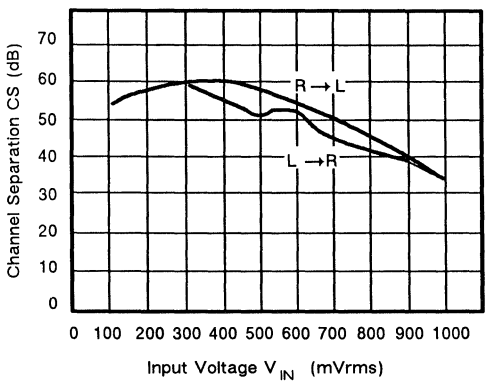
TOTAL HARMONIC DISTORTION (MAIN, MONO)
vs INPUT VOLTAGE



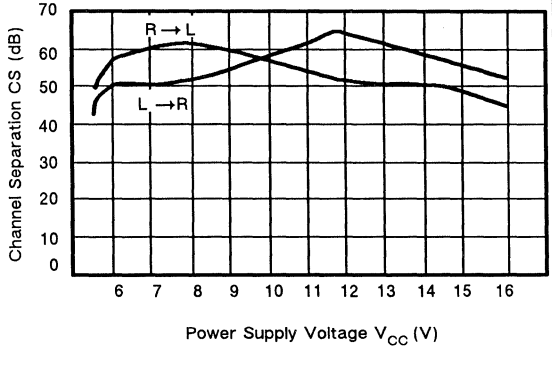
TOTAL HARMONIC DISTORTION (MAIN, MONO)
vs POWER SUPPLY VOLTAGE



CHANNEL SEPARATION
vs INPUT VOLTAGE

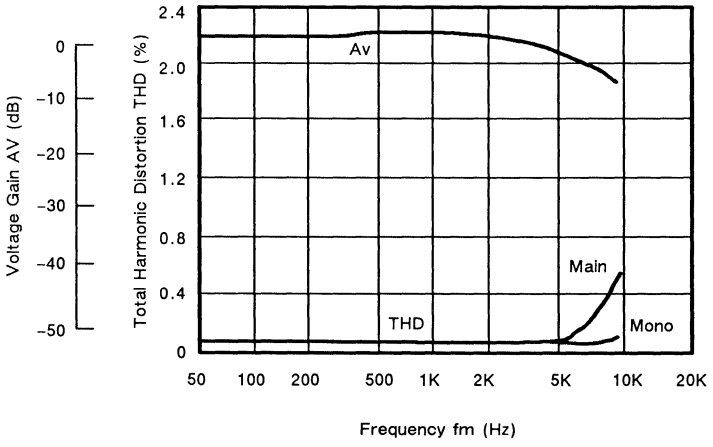


CHANNEL SEPARATION
vs POWER SUPPLY VOLTAGE

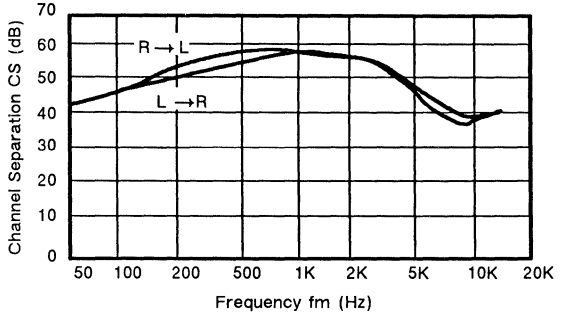


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

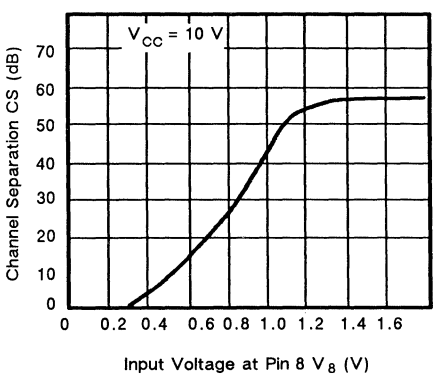
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs FREQUENCY



CHANNEL SEPARATION vs FREQUENCY



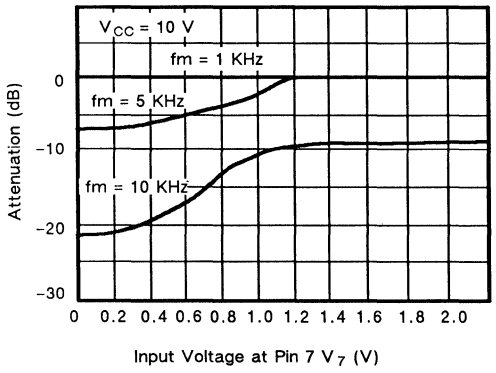
CHANNEL SEPARATION vs INPUT VOLTAGE AT PIN 8



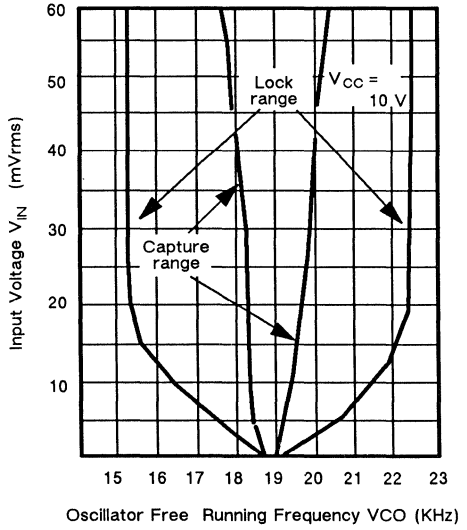
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

3

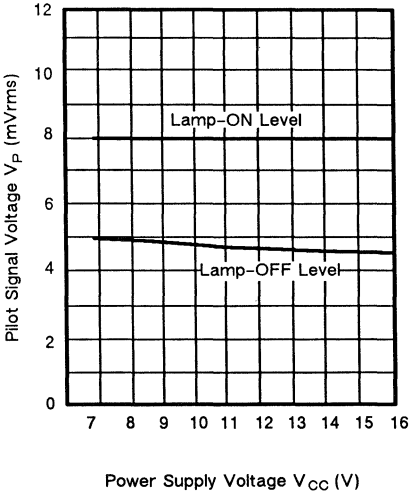
ATTENUATION vs INPUT VOLTAGE AT PIN 7



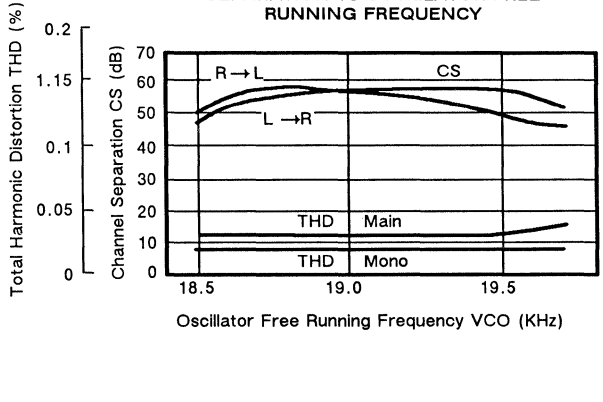
INPUT VOLTAGE vs OSCILLATOR FREE RUNNING FREQUENCY



PILOT SIGNAL VOLTAGE vs POWER SUPPLY VOLTAGE

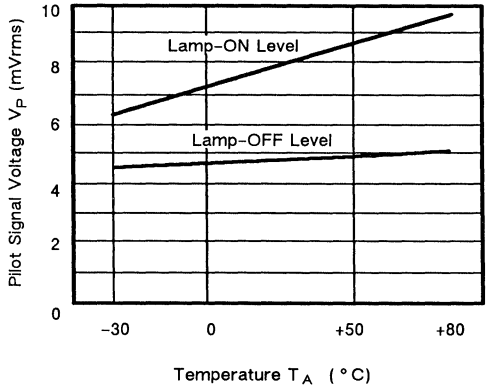


TOTAL HARMONIC DISTORTION, CHANNEL SEPARATION vs OSCILLATOR FREE RUNNING FREQUENCY

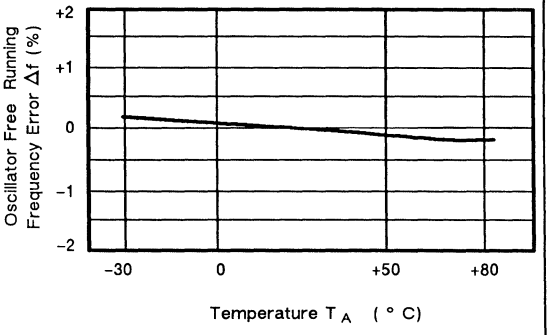


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

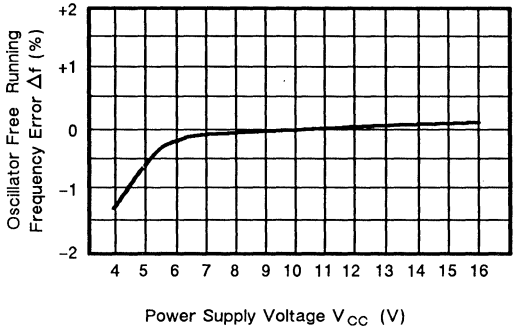
PILOT SIGNAL VOLTAGE vs TEMPERATURE



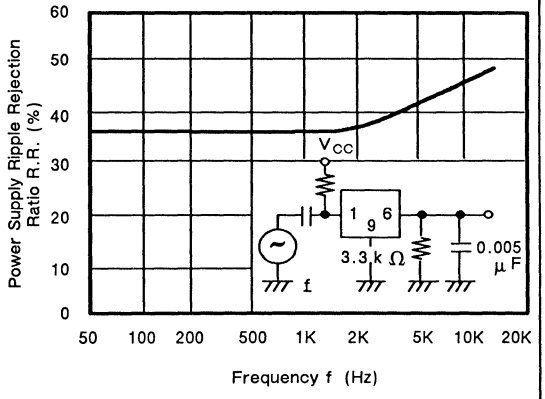
OSCILLATOR FREE RUNNING FREQUENCY ERROR vs TEMPERATURE



OSCILLATOR FREE RUNNING FREQUENCY ERROR vs POWER SUPPLY VOLTAGE

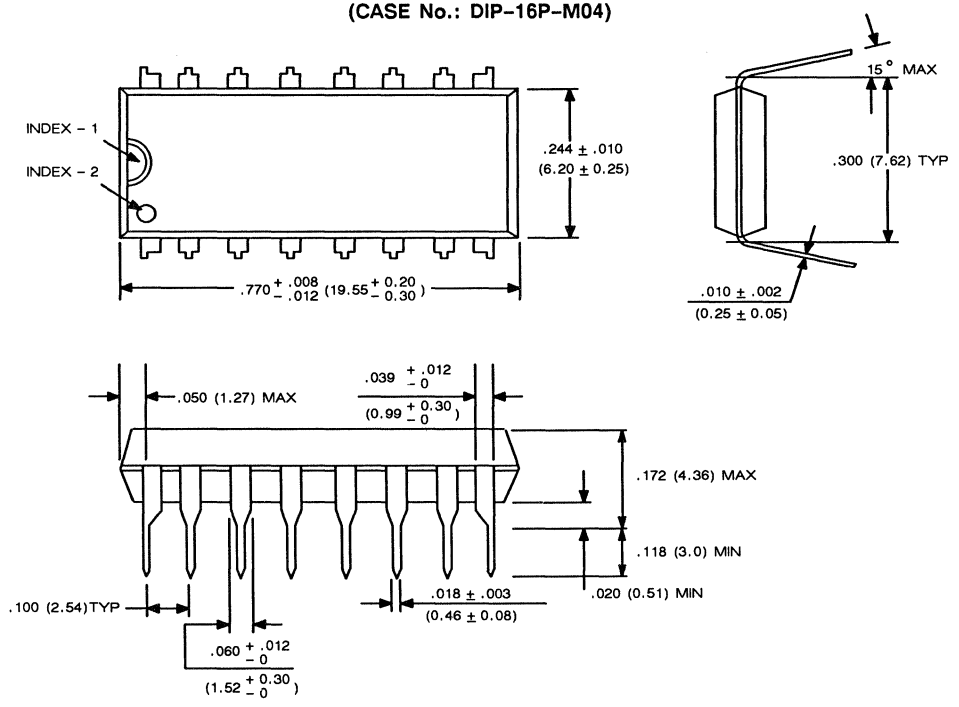


POWER SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

D16033S-2C

Section 4

Power Supply Controls

Fujitsu Part No.	Description	Features	Equiv. Prod.	Power Supply (V)	Package	No. of Pins
MB3752	Series Regulator	Load Regulation = 0.03%	µA723	+9.5 ~ +40	Ceramic DIP Plastic DIP Plastic Flatpak	14 14 14
MB3756	3-Out Series Voltage Regulator	Fixed (250mA), Switchable (200/110mA)	—	+12 ~ +16	SIP (Heatsink)	8
MB3759	PWM Control Circuit Regulator (200KHz)	Low Voltage Malfunction Protection I_D = 200mA Steering Control	TL494	+7 ~ +40	Ceramic DIP Plastic DIP Plastic Flatpak	16 16 16
MB3761	Voltage Detector	Reference 1.2V, I_{CC} = 250mA	—	+2.5 ~ +40	Plastic DIP Plastic Flatpak SIP	8 8 8
MB3769	PWM Control Circuit Regulator	500KHz Switching, I_D = 600mA Max.	UC384	+12 ~ +18	Plastic DIP Plastic Flatpak	16 16
MB3771	Voltage Detector	V_{CC} On/Off Reset, V_{REF} = 1.24 ± 1.5%	—	+3.5 ~ +18	Plastic DIP Plastic Flatpak SIP	8 8 8
MB3773	Voltage Detector	Watchdog for Over-running Protection	—	+3.5 ~ +18	Plastic DIP Plastic Flatpak SIP	8 8 8

FUJITSU

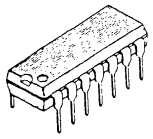
MB3752

VOLTAGE REGULATOR

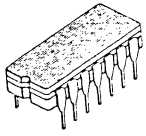
TS567-A878
August 1987

The Fujitsu MB3752 is a monolithic voltage regulator IC. It contains a temperature compensated reference voltage circuit, a surge protected error amplifier and high current protected circuit.
High current regulator, negative power supply regulator, floating regulator and switching regulator are made up by selection of external components.
Constant current limiting or foldback current limiting is selected by selction of external components.
It is suitable both industrial and consumer voltage regulator system.
The high performance makes a lot of application and enables operation with various functions.

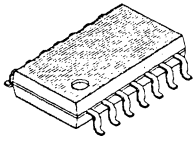
- High Load Regulation : 0.03 % ($1mA \leq I_L \leq 50mA$)
- Wide Input Voltage Range : 40 V max.
- Wide Output Voltage Range : 2 V to 37 V
- Compatible with Fairchild μA723
- Package
  14-pin plastic DIP package (Suffix: -P)
  14-pin ceramic DIP package (Suffix: -Z)
  14-pin plastic Flat package (Suffix: -PF)



PLASTIC PACKAGE
DIP-14P-M02



CERAMIC PACKAGE
DIP-14C-C01



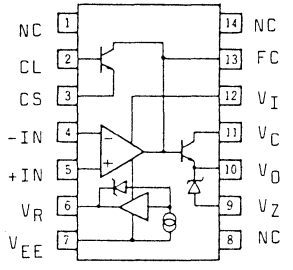
PLASTIC PACKAGE
FPT-14P-M01

4

ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A=25°C)

Rating	Symbol	Value			Unit
		Ceramic	Plastic	Flat	
Storage Temperautre	T_{STG}	-65~+150	-55~+125	-55~+125	°C
Operating Temperature	T_A	-55~+125	-20~+75	-20~+75	°C
Power Dissipation	P_D	1000	800	620 *	mW
Output Current	I_L	150	150	150	mA
Zener Current	I_Z	25	25	25	mA
Current from V_{REF}	I_R	15	15	15	mA
Input Voltage	V_{IN}	40	40	40	V

PIN ASSIGNMENT

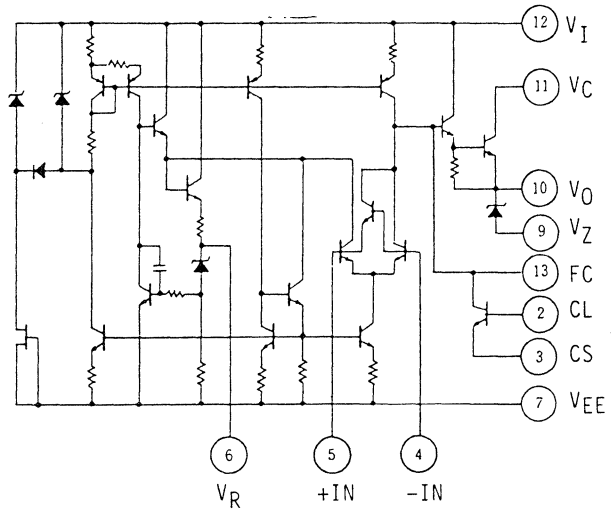


Note: FLAT package is mounted on the epoxy board. (4cm x 4cm x 1.5mm)

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB3752 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	9.5 to 40	V
Load Current	I_L	1 to 50	mA
Operating Temperature	T_A	-20 to 75	°C

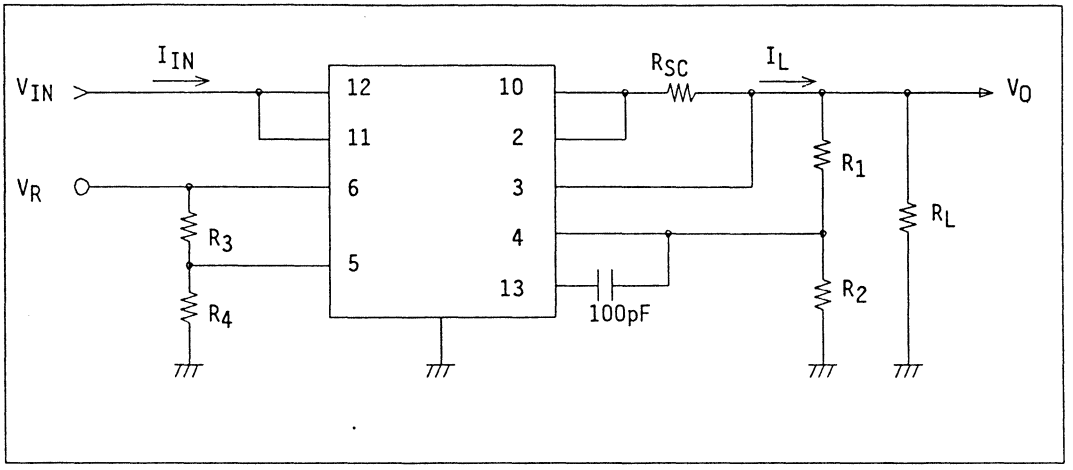
ELECTRICAL CHARACTERISTICS

(V_{IN}=12V, I_L=1mA, R_{SC}=0, V_O=5V, T_A=25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Voltage	V_{IN}		9.5		40	V
Output Voltage	V_O		2.0		37	V
Input-to-output Voltage Differential	V_{IN}-V_O		3.0		38	V
Bias Current	I_I	I_L=0, V_{IN}=30V			4.0	mA
Reference Voltage	V_R		6.80	7.15	7.50	V
Input Regulation 1	R_{IN1}	12V≤V_{IN}≤15V		0.01	0.1	%
Input Regulation 2	R_{IN2}	12V≤V_{IN}≤40V		0.1	0.5	%
Input Regulation 3	R_{IN3}	12V≤V_{IN}≤15V, 0°C≤T_A≤70°C			0.3	%
Load Regulation 1	R_{LD1}	1mA≤I_L≤50mA		0.03	0.2	%
Load Regulation 2	R_{LD2}	1mA≤I_L≤50mA, 0°C≤T_A≤70°C			0.6	%
Temperature Regulation	R_T	0°C≤T_A≤70°C		0.2	1.0	%
Ripple Rejection Ratio	R.R.	f=50Hz to 10kHz, C_R=0		74		dB
		f=50Hz to 10kHz, C_R=5μF		86		dB
Short Circuit Output Current	I_{SC}	V_O=0, R_{SC}=10Ω	60	70	80	mA

4

Fig.2 - MEASUREMENT CIRCUIT



4

i) $2V \leq V_O \leq V_R$ $\quad V_O = V_R \dfrac{R_4}{R_3+R_4}$, $R1 = \dfrac{R_3 \cdot R_4}{R_3+R_4}$, $R_2 = \infty$, $R_3+R_4 \fallingdotseq 7k\Omega$

ii) $V_R \leq V_O \leq 37V$ $\quad V_O = V_R \left(1+ \dfrac{R_1}{R_2}\right)$, $R3 = \dfrac{R_1 \cdot R_2}{R_1+R_2}$, $R_4 = \infty$, $R_2 \fallingdotseq 7k\Omega$

iii) Equations for measurement items

a) $I_B = I_{IN}$ $\quad \left(\begin{array}{l} R_1=1.5k,\ R_3=0,\ I_L=0, \\ R_2=\infty \quad ,R_4=\infty,\ R_L=\infty \end{array}\right)$

b) $R_{IN1} = \dfrac{V_O(15V)-V_O(12V)}{V_O(12V)} \times 100$

c) $R_{IN2} = \dfrac{V_O(40V)-V_O(12V)}{V_O(12V)} \times 100$

d) $R_{LD} = \dfrac{V_O(1mA)-V_O(50mA)}{V_O(1mA)} \times 100$

e) $I_{SC} = I_L \quad (R_L=0)$

f) $R_T = \dfrac{V_O(MAX)-V_O(MIN)}{V_O(25°C)} \times 100$

Note: (b) to (f)
(V_O=5V setting, R_1=1.5kΩ, R_2=∞, R_3=2.15kΩ, R_4=5kΩ, R_L=5kΩ)

Fig.3 - INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL vs. MAXIMUM LOAD CURRENT

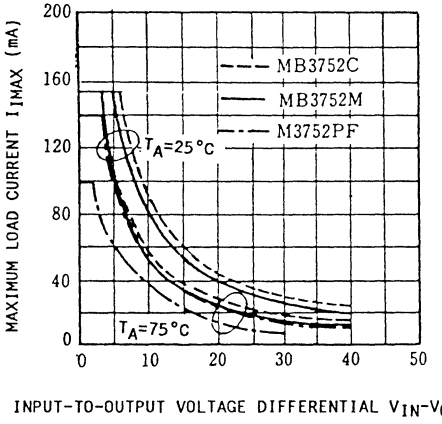


Fig.4 - INPUT VOLTAGE vs. BIAS CURRENT

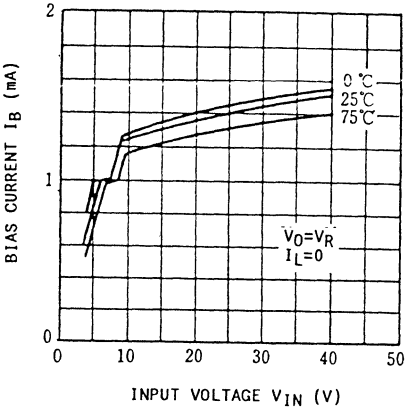


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Fig.5 - LOAD CURRENT vs. LOAD REGULATION

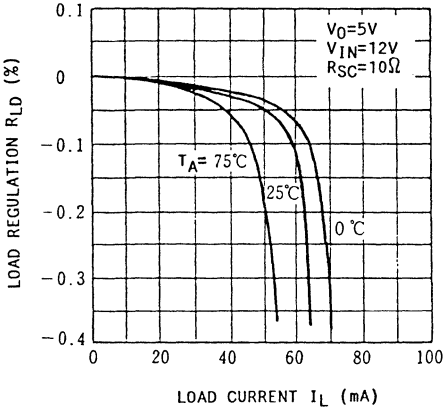


Fig.6 - CURRENT LIMIT

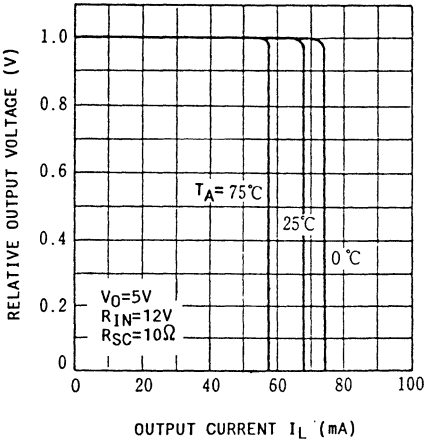


Fig.7 - LOAD CURRENT vs. LOAD REGULATION

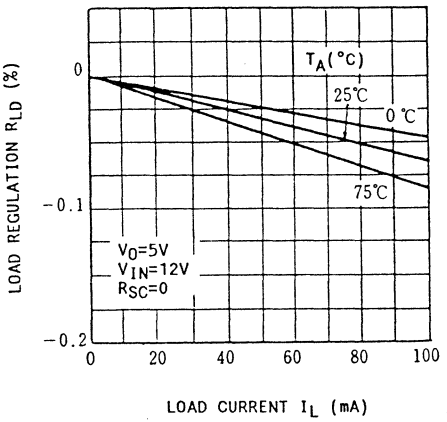


Fig.8 - JUNCTION TEMPERATURE vs. CURRENT LIMIT SENSE VOLTAGE

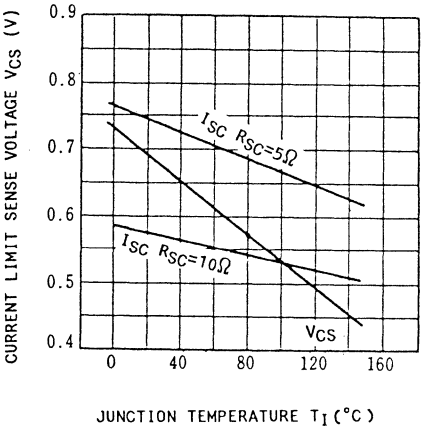


Fig.9 - INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL vs. LINE REGULATION

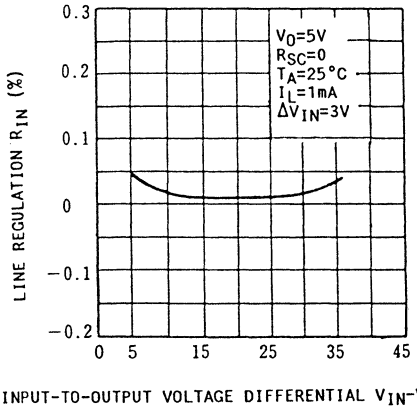
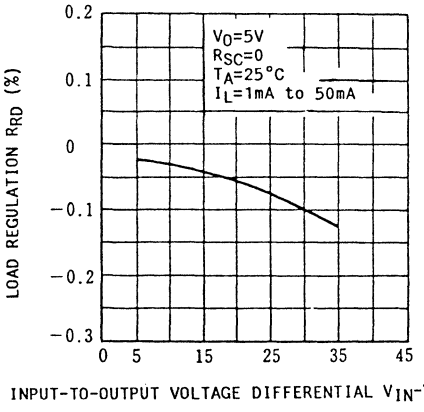


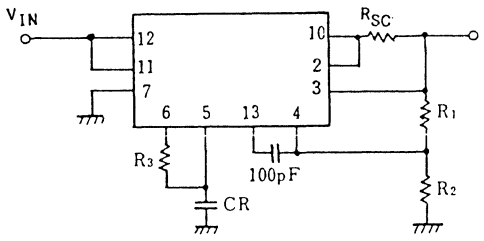
Fig.10 - INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL vs. LOAD REGULATION



APPLICATION EXAMPLES

Fig.11 - BASIC HIGH VOLTAGE REGULATOR

$V_R \leq V_O \leq 37V$

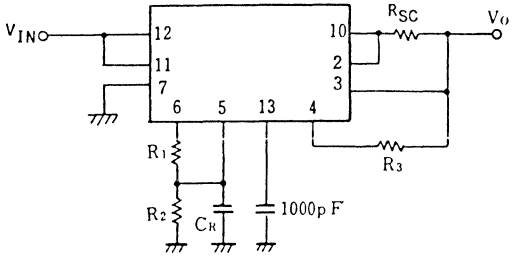


$$V_O = V_R \cdot \frac{R_1+R_2}{R_2}$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1+R_2}$$ for minimum temperature drift

Fig.12 - BASIC LOW VOLTAGE REGULATOR

$2V \leq V_O \leq V_R$

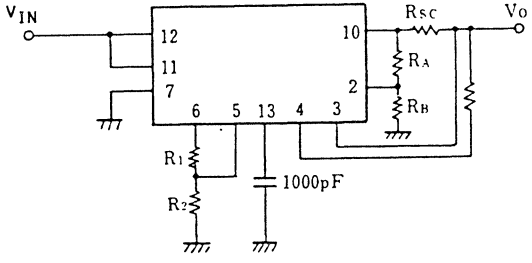


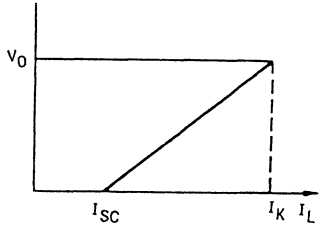
$$V_O = V_R \cdot \frac{R_2}{R_1+R_2}$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1+R_2}$$ for minimum temperature drift

4

Fig.13 - FOLDBACK CURRENT LIMITING REGULATOR





$I_L \leq I_K \quad V_O = V_R \cdot \frac{R_2}{R_1+R_2}$

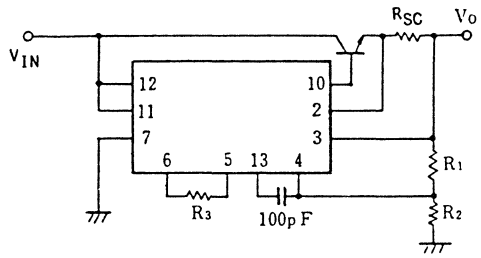
$R_3 = \frac{R_1 \cdot R_2}{R_1+R_2}$ for minimum temperarure drift

$$V_O = \frac{R_B \cdot R_{SC}}{R_A} \cdot I_L - V_{SC}\left(1+\frac{R_B}{R_A}\right)$$

$$I_{SC} = \frac{V_{SC}}{R_{SC}} \cdot \left(1+\frac{R_A}{R_B}\right), \quad V_{SC} \doteq 0.7V$$

$$I_K = I_{SC} + \frac{V_O}{R_{SC}} \cdot \frac{R_A}{R_B}$$

Fig.14 - POSITIVE VOLTAGE REGULATOR
NPN TRANSISTOR

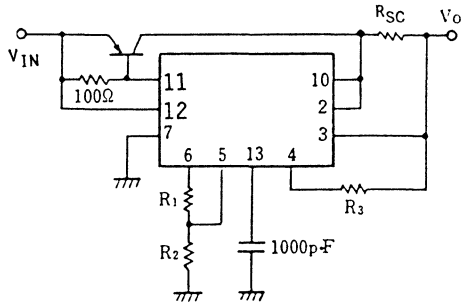


4

$$V_O = V_R \cdot \frac{R_1+R_2}{R_2}$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1+R_2} \text{ for minimum temperature drift}$$

Fig.15 - POSITIVE VOLTAGE REGULATOR
PNP TRANSISTOR

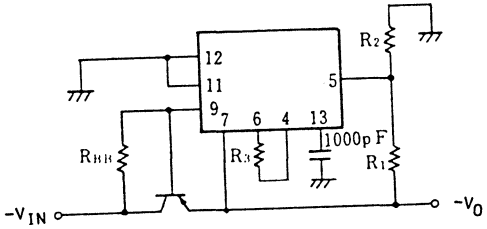


$$V_O = V_R \cdot \frac{R_2}{R_1+R_2}$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1+R_2} \text{ for minimum temperature drift}$$

Fig.16 - NEGATIVE VOLTAGE REGULATOR

$|V_O| \geq 9.5V$

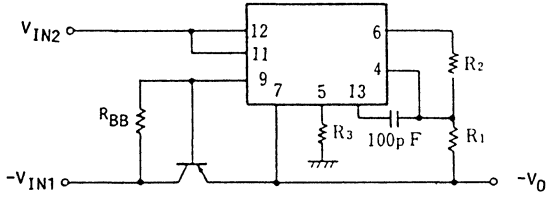


$$V_O = V_R \cdot (1+\frac{R_2}{R_1})$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1+R_2} \text{ for minimum temperature drift}$$

Fig.17 - NEGATIVE VOLTAGE REGULATOR

$0 \leq |V_O| \leq V_R$

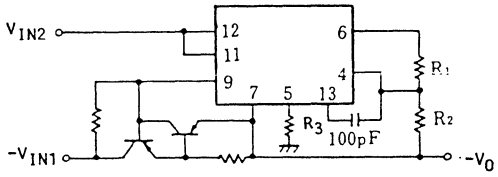


$$V_O = \frac{V_R}{(1+R_2/R_1)}, \quad V_{IN2}+V_O \geq 9.5V$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1+R_2} \text{ for minimum temperature drift}$$

Fig.18 - NEGATIVE VOLTAGE REGULATOR (CURRENT LIMITING)

$0 \leq |V_O| \leq VR$



$$I_L = \frac{V_{CS}}{R_{CS}} \quad (V_{CS} \fallingdotseq 0.7V,\ V_O = 0)$$

$$I_L = \frac{V_R}{(1+R_2/R_1)},\ V_{IN2}+V_O \geq 9.5V$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1+R_2} \text{ for minimum temperature drift}$$

Fig.19 - SWITCHING REGULATOR

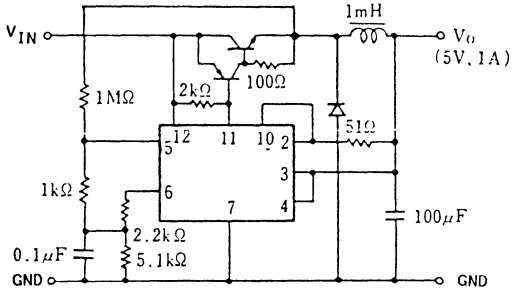


Fig.20 - DUAL TRACKING REGULATOR (CURRENT LIMITING)

$$V_{O1} = V_R \left(1 + \frac{R_1}{R_2}\right) \qquad V_{O1} \geq V_R$$

$$V_{O1}+V_{O2} \geq 40V$$

$$V_{O2} = \frac{R_4}{R_3} V_{O1}$$

$$I_{L1MAX} \fallingdotseq \frac{0.7}{R_5}$$

$$I_{L2MAX} \fallingdotseq \frac{0.6}{R_5}$$

Example for ±15V, ±1A
R_1=8.2kΩ R_2=7.5kΩ R_3=15kΩ R_3=15kΩ R_5=R6=0.39Ω R_7=2kΩ

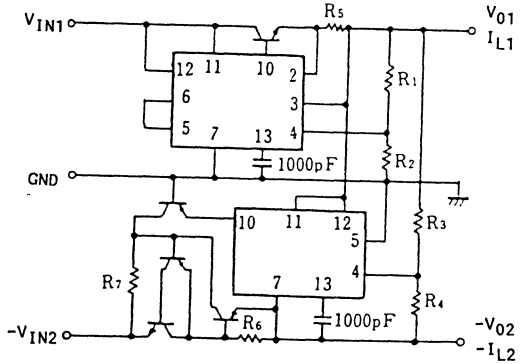
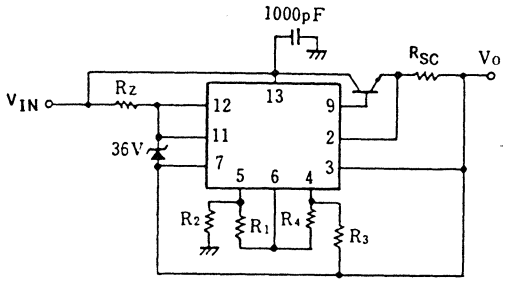


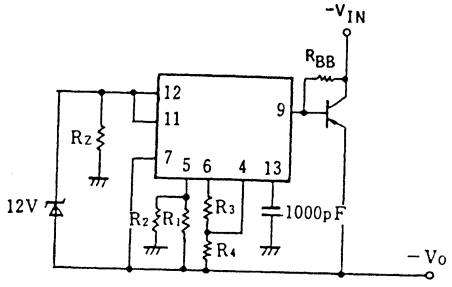
Fig.21 - POSITIVE FLOATING VOLTAGE REGULATOR



$R_3=R_4=3.3k\Omega$

$$V_O = V_R \cdot \frac{R_2-R_1}{2R_1}$$

Fig.22 - NEGATIVE FLOATING VOLTAGE REGULATOR

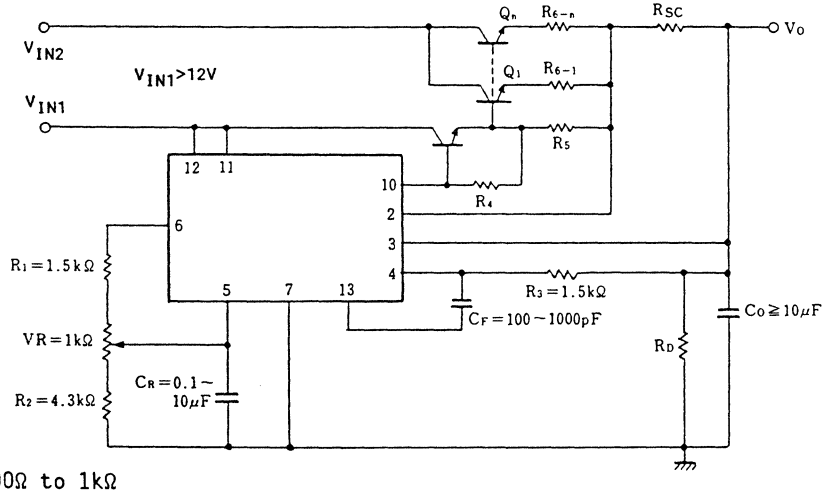


$R_3=R_4=3.3k\Omega$

$$V_O = V_R \cdot \frac{R_1+R_2}{2R_1}$$

4

Fig.23 - 5 V HIGH CURRENT VOLTAGE REGULATOR



$R_4=100\Omega$ to $1k\Omega$
$R_5=10\Omega$ to 100Ω

$$I_{LMAX} = \frac{V_{CS}}{R_{SC}} \quad \left(\begin{array}{l} V_{CS} \fallingdotseq 0.7\ V \text{ at } 25\ °C \\ \Delta V_{CS}/\Delta T_I = -2mV/°C \end{array} \right)$$

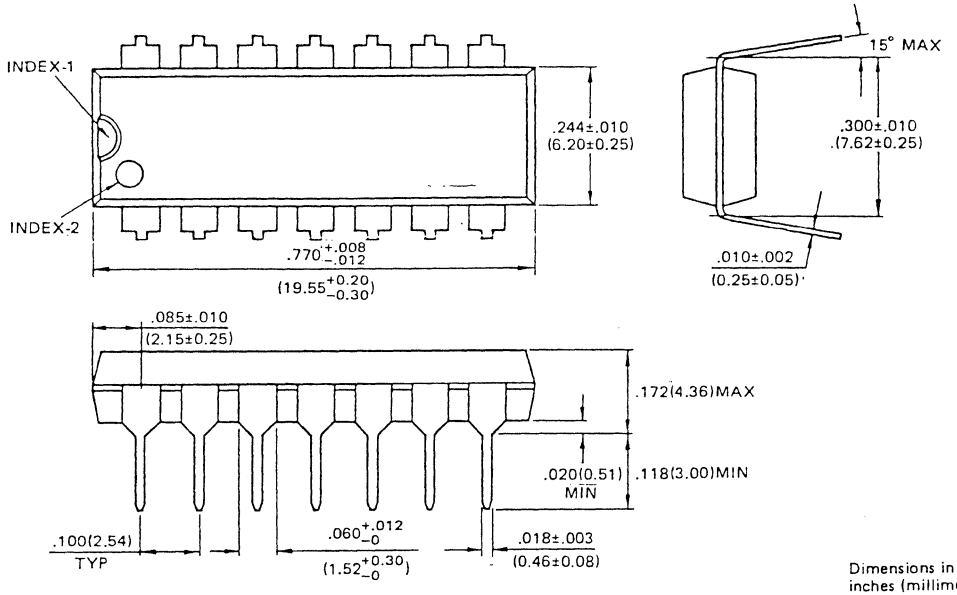
$$V_{IN2} > V_{OMAX} + V_{CESATOUT} + R_{SC} \cdot I_{LMAX} + \frac{1}{n} R_6 \cdot I_{LMAX} + \frac{V_{IN2P}}{2}$$

$V_{CESATOUT}$: Maximum value between Q_1 to Q_n

R_6 : $R_{6-1} = R_{6-2} \cdots\cdots = R_{6-n} = R_6$

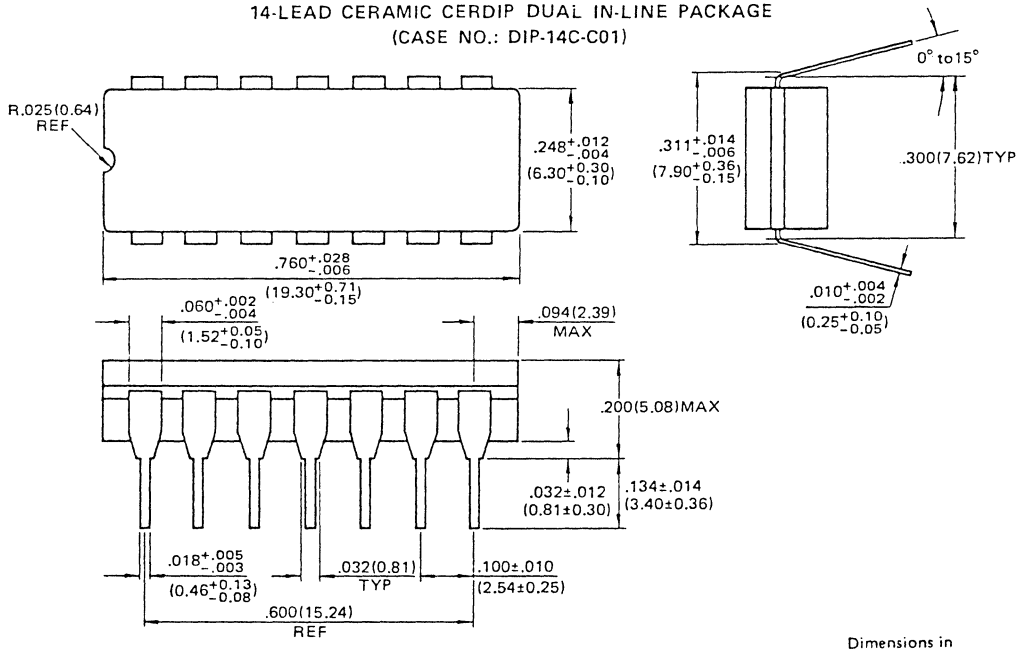
V_{IN2P} : Maximum ripple amplitude of V_{IN2}

14-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)



Dimensions in inches (millimeters).

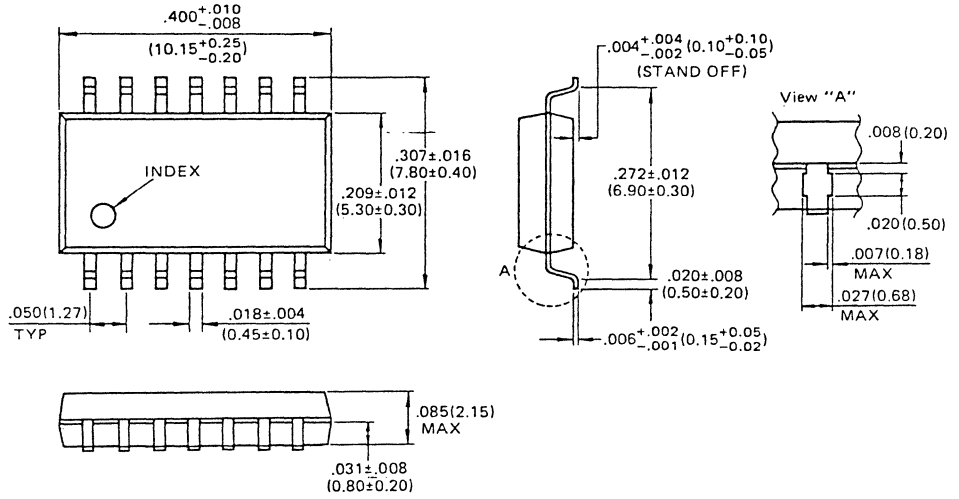
14-LEAD CERAMIC CERDIP DUAL IN-LINE PACKAGE
(CASE NO.: DIP-14C-C01)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



Dimensions in
inches (millimeters)

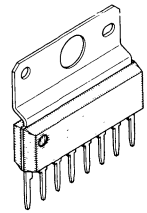
4

October 1987
Edition 1.0

VOLTAGE REGULATOR

The Fujitsu MB3756 monolithic voltage regulator with three outputs is fabricated with a bipolar linear IC technology. Two alternately exchangeable outputs are provided for two stabilized output levels and controlled by an external control signal. Switching noise is prevented by internal circuitry that is suitable for switching between modes such as transmitting and receiving or AM and FM. The MB3756 is packaged in as 8-pin single-in-line package with a heat radiation fin to allow large power consumption.

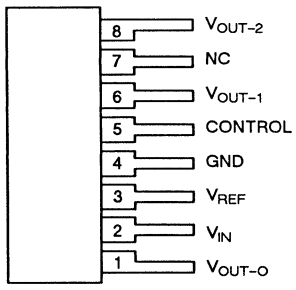
- No need for external components
- Good balance between three outputs
- On-chip noise protection circuitry
- On-chip overload current protection and thermal protection circuitry
- Good mountability
- High output current : 200 mA typical for V_{O2} output
  : 100 mA typical for V_{O0}, V_{O1} outputs



PLASTIC PACKAGE
SIP-08P-M01

PIN ASSIGNMENT

(FRONT VIEW)



ABSOLUTE MAXIMUM RATINGS (see NOTE) TA = 25°C

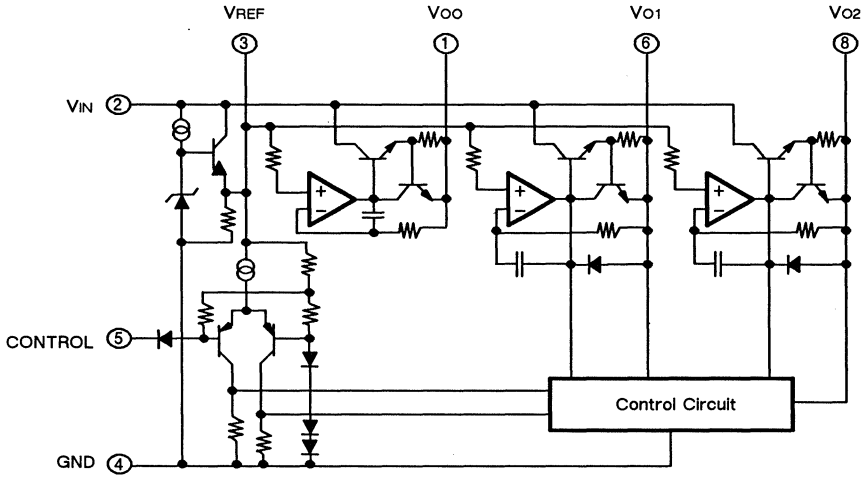
Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	18	V
Power Dissipation	P_D	1 *1	W
		4 *2	W
Operating Temperature	T_C	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Notes: *1 No Heat Sink ($T_A \leq 70°C$)
*2 Infinite Heat Sink ($T_A \leq 70°C$)
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 — MB3756 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Voltage	V_{IN}	11	-	16	V
Load Current	I_{L1} *1	0	-	100	mA
	I_{L2} *2	0	-	200	mA
Operating Temperature	Tc	-20	-	+75	°C

Note : *1 V00, V01
*2 V02

ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{IN} = 14 V, R_{L0} = R_{L1} =200 Ω, R_{L2} = 100 Ω)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Input Voltage	V_{IN}	—	10.6	—	18	V
Output Voltage	V_O	—	7.8	8.2	8.6	V
Input Regulation	—	11 V ≤ V_{IN} ≤ 18 V	—	20	100	mV
Load Regulation	—	(V_{00}, V_{01}) 1 mA ≤ I_L ≤ 100 mA	—	15	80	mV
	—	(V_{02}) 1 mA ≤ I_L ≤ 200 mA	—	20	100	mV
	—	(V_{00}, V_{01}) 1 mA ≤ I_L ≤ 100 mA V_{IN} = 11.5 V	—	20	100	mV
	—	(V_{02}) 1 mA ≤ I_L ≤ 200 mA V_{IN} = 11.5 V	—	30	150	mV
Bias Current	I_B	V_{IN} = 18 V	—	6	10	mA
Ripple Rejection Ratio	—	f = 100 Hz	—	60	—	dB
Output Noise Voltage	—	10 Hz ≤ f ≤ 100kHz, C_R = 10 µF	—	40	—	µV
Input to Output Voltage Differential	V_{IN}–V_O	—	—	1.7	—	V
Temperature Coefficient of Output Voltage	TCV_O	—	—	-0.4	—	mV/C°
Output Voltage Deviation	ΔV_O	—	—	10	50	mV
Short Circuit Output Current	I_{SC}	(V_{00},V_{01})	—	200	—	mA
		(V_{02})	—	350	—	mA
Output Voltage	V_{01L}	V_{IC} = 0.8 V	0	—	0.2	V
	V_{02L}	V_{IC} = 0.8 V	7.8	8.2	8.6	V
	V_{01H}	V_{IC} = 2.0 V	7.8	8.2	8.6	V
	V_{02H}	V_{IC} = 2.0 V	0	—	0.2	V
Control Input Current	I_{IL}	V_{ICL} = 0 V	—	-0.2	-1.0	mA
	I_{IH}	V_{ICH} = 18V, V_{IN} = 18V	—	—	10	µA

4

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 2 — BIAS CURRENT vs INPUT VOLTAGE

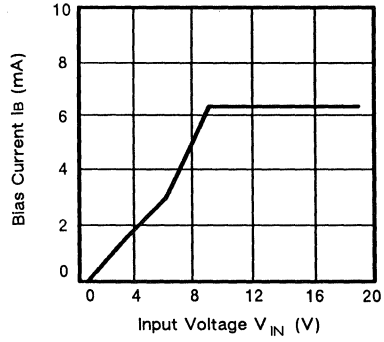


Fig.3 — INPUT TO OUTPUT VOLTAGE DIFFERENTIAL vs JUNCTION TEMPERATURE

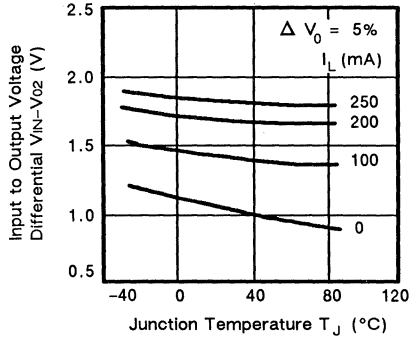


Fig. 4 — OUTPUT NOISE VOLTAGE vs EXTERNAL CAPACITANCE

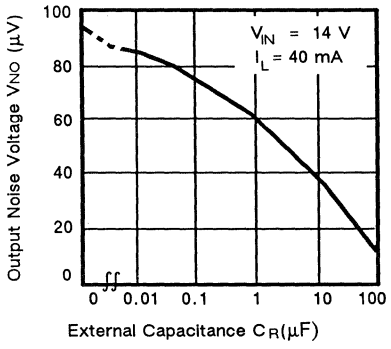
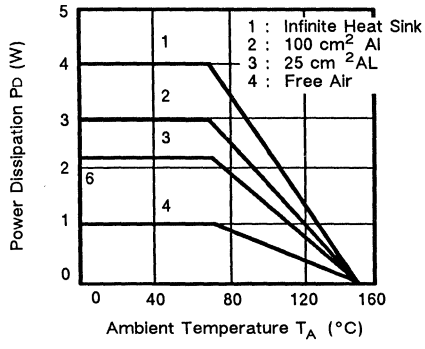


Fig. 5 — POWER DISSIPATION CURVES



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig.6 —OUTPUT VOLTAGE vs INPUT VOLTAGE

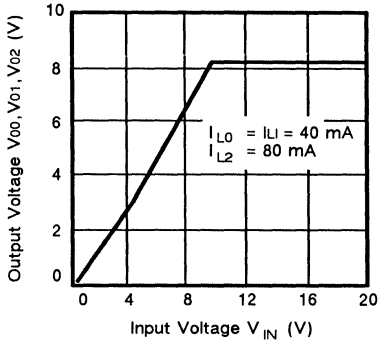


Fig.7 — OUTPUT VOLTAGE DEVIATION vs INPUT VOLTAGE

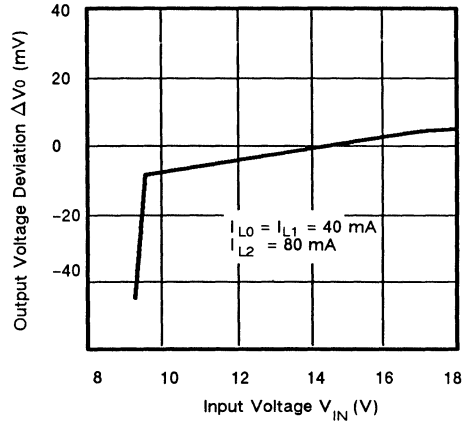


Fig.8 — OUTPUT VOLTAGE vs LOAD CURRENT

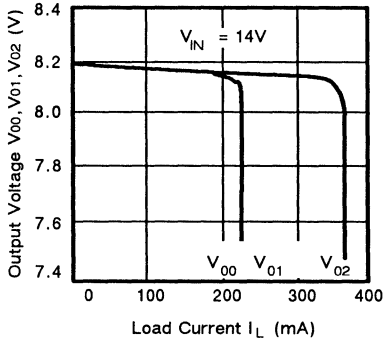
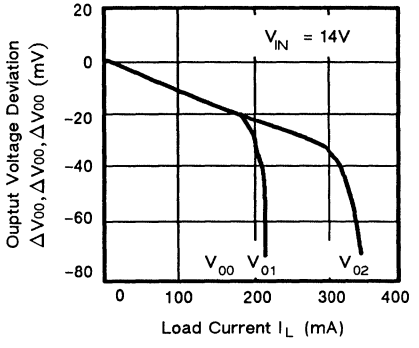


Fig. 9 — OUTPUT VOLTAGE DEVIATION vs LOAD CURRENT



4

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig.10 — OUTPUT VOLTAGE vs CONTROL INPUT VOLTAGE

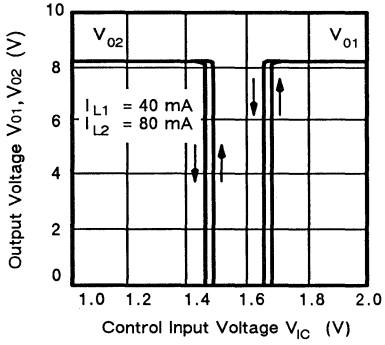


Fig. 11 — CONTROL INPUT CURRENT vs CONTROL INPUT VOLTAGE

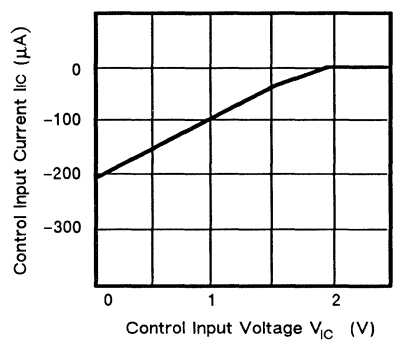
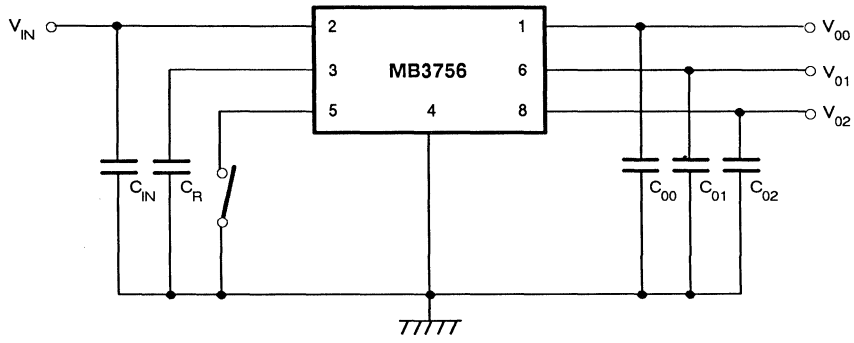


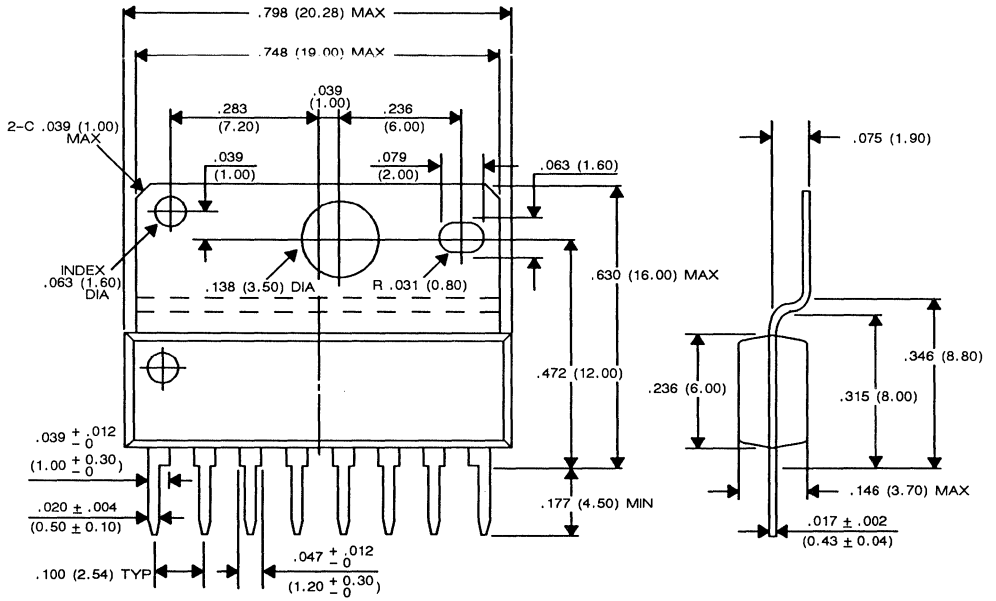
Fig. 12 — APPLICATION CIRCUIT



Note: C_{IN} is required if the regulator is located at a distance from the power supply filter.
C_R improves output noise and ripple rejection.
C_{00}, C_{01}, C_{02} improve transient response.

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-08P-M01)



Dimensions in inches (millimeters)

S08004S-6C

FUJITSU

PULSE-WIDTH-MODULATION CONTROL CIRCUIT

MB 3759

May 1987
Edition 1.0

PULSE-WIDTH-MODULATION CONTROL CIRCUIT

The Fujitsu MB 3759 is complete pulse-width modulation control system on a single monolithic chip. The MB 3759 consists of an internal 5.00V reference, two or-connected amplifiers, externally timed (or synchronized) oscillator and control ramp generator. The MB 3759 provides for either push-pull or single-ended mode of operation with external control of dead-band.
The two NPN output transistors have uncommitted emitters and collectors that can be used to either sink or source up to 200 mA each.

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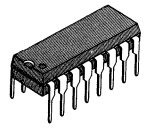
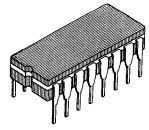
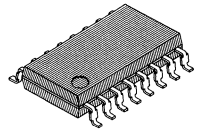
- Complete pulse-width-modulation system with power control circuit
- Either push-pull or single-ended mode of operation
- Internal circuitry prohibits double pulse at either output
- On-chip voltage reference
- Uncommitted output drivers
- Master or slave oscillator control
- Dual error amplifiers
- Under voltage lockout function
- Package: 16-pin Plastic DIP Package
  16-pin Ceramic DIP Package
  16-pin Plastic FPT Package



PLASTIC PACKAGE
DIP-16P-M04

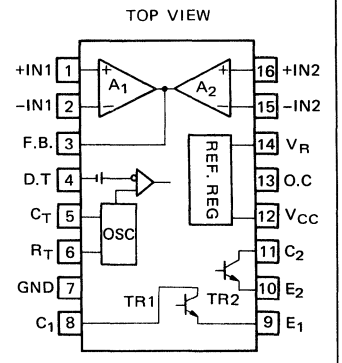


CERAMIC PACKAGE
DIP-16C-C01



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

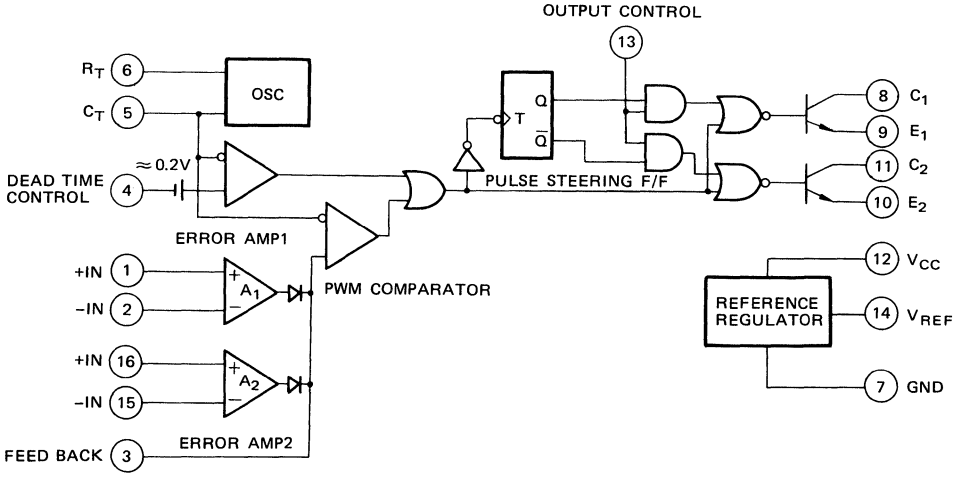
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	41	V
Collector Output Voltage		V_{CE}	41	V
Collector Output Current		I_{CE}	250	mA
Amplifier Input Voltage		V_{IN}	V_{CC} + 0.3	V
Power Dissipation	Plastic DIP	P_D	1000 ($T_A \leq 25°C$)	mW
	Ceramic DIP		800 ($T_A \leq 60°C$)	
	Plastic FPT		620 ($T_A \leq 25°C$)*	
Operating Temperature	DIP	T_A	−20 to 85	°C
	FPT		−20 to 75	
Storage Temperature		T_{STG}	−55 to 125	°C

* PFT package is mounted on the epoxy board. (4 cm x 4 cm x 0.15 cm)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 3759 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	DIP-package			FPT-package			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage	V_{CC}	7	15	32	7	15	24	V
Collector Output Voltage	V_{CE}			40			40	V
Collector Output Current	I_{CE}	5	100	200	5	50	100	mA
Amplifier Input Voltage	V_{IN}	-0.3	0 to V_{REF}	V_{CC}-2	-0.3	0 to V_{REF}	V_{CC}-2	V
FB Sink Current	I_{SINK}			0.3			0.3	mA
FB Source Current	I_{SOURCE}			2			2	mA
Reference Section Output Current	I_{REF}		5	10		3	10	mA
Timing Resistor	R_T	1.8	30	500	1.8	30	500	kΩ
Timing Capacitor	C_T	470	1000	10^6	470	1000	10^6	pF
Oscillator Frequency	f_{OSC}	1	40	300	1	40	300	kHz
Operating Temperature	T_A	-20	25	85	-20	25	75	°C

Note: These recommended operating conditions are based on the standard condition.
When used at higher supply voltage, careful consideration for the ambient temperature, power consumption and so on is necessary.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 15V)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Reference Section						
Output Voltage	V_{REF}	I_O = 1mA	4.75	5.0	5.25	V
Input Regulation	ΔV_{RIN}	7V ≤ V_{CC} ≤ 40V, T_A = 25°C		2	25	mV
Load Regulation	ΔV_{RLD}	1mA ≤ I_O ≤ 10mA, T_A = 25°C		-1	-15	mV
Temperature Stability	$\Delta V_R/\Delta T$	-20°C ≤ T_A ≤ 85°C		±200	±750	μV/°C
Short Circuit Output Current	I_{SC}		15	40		mA
Reference Lockout Voltage				4.3		V
Reference Hysteresis Voltage				0.3		V

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Oscillator Section						
Oscillator Frequency	f_{OSC}	R_T = 30kΩ, C_T = 1000pF	36	40	44	kHz
Standard Deviation of Frequency		R_T = 30kΩ, C_T = 1000pF		±3		%
Frequency Change with Voltage		7V ≤ V_{CC} ≤ 40V, T_A = 25°C		±0.1		%
Frequency Change with Temperature	$\Delta f_{osc}/\Delta T$	−20°C ≤ T_A ≤ 85°C		±0.01	±0.03	%/°C
Dead-Time Control Section						
Input Bias Current	I_D	0 ≤ V_I ≤ 5.25V		−2	−10	μA
Maximum Duty Cycle (Each Output)		V_I = 0	40	45		%
Input Threshold Voltage — 0% Duty Cycle	V_{DO}			3.0	3.3	V
Input Threshold Voltage — Max. Duty Cycle	V_{DM}		0			V
Effor Amplifier Section						
Input Offset Voltage	V_{IO}	$V_{O(pin3)}$ = 2.5V		±2	±10	mV
Input Offset Current	I_{IO}	$V_{O(pin3)}$ = 2.5V		±25	±250	nA
Input Bias Current	I_I	$V_{O(pin3)}$ = 2.5V		−0.2	−1.0	μA
Common-Mode Input Voltage	V_{CM}	7V ≤ V_{CC} ≤ 40V	−0.3		V_{CC}−2	V
Open-Loop Voltage Amplification	A_V	0.5 ≤ V_O ≤ 3.5V	70	95		dB
Unity-Gain Bandwidth	BW	A_V = 1		800		kHz
Common-Mode Rejection Ratio	CMR	V_{CC} = 40V	65	80		dB
Output Sink Current (3 pin)	I_{SINK}	−5V ≤ V_{ID} ≤ −15mV, V_O = 0.7V	0.3	0.7		mA
Output Source Current (3 pin)	I_{SOURCE}	15mV ≤ V_{ID} ≤ 5V, V_O = 3.5V	−2	−10		mA

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ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Output Section						
Collector Leakage Current	I_{CO}	V_{CE} = 40V, V_{CC} = 40V			100	μA
Emitter Leakage Current	I_{EO}	V_{CC} = V_C = 40V, V_E = 0V			-100	μA
Collector Emitter Saturation Voltage (Emitter Grounded)	V_{SATC}	V_E = 0, I_C = 200mA		1.1	1.3	V
Collector Emitter Saturation Voltage (Emitter Follower)	V_{SATE}	V_C = 15V, I_E = -200mA		1.5	2.5	V
Output Control Input Current	I_{OPC}	V_I = V_{REF}		1.3	3.5	mA
PWM Comparator Section						
Input Threshold Voltage	V_{TH}	0% Duty		4	4.5	V
Input Sink Current (3 pin)	I_{SINK}	V_O (pin 3) = 0.7V	0.3	0.7		mA
Total Device						
Power Supply Current	I_{CC}	V4 = 2V, See Fig-2		8		mA
Stand-by Current	I_{CCQ}	$V_{(pin6)}$ = V_{REF}, I/O open		7	12	mA
Switching Characteristics						
Rise Time (Emitter Grounded)	t_R	R_L = 68Ω		100	200	ns
Fall Time (Emitter Grounded)	t_F	R_L = 68Ω		25	100	ns
Rise Time (Emitter Follower)	t_R	R_L = 68Ω		100	200	ns
Fall Time (Emitter Follower)	t_F	R_L = 68Ω		40	100	ns

Fig. 2 – TEST CIRCUIT

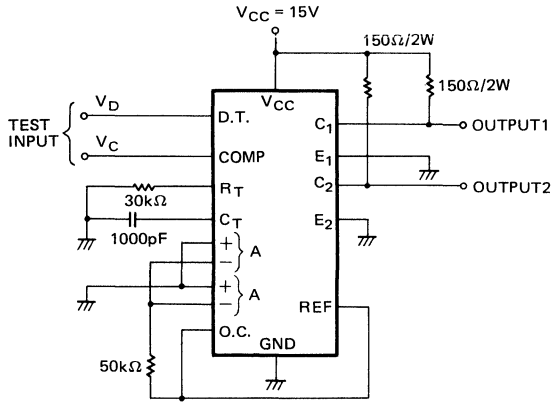
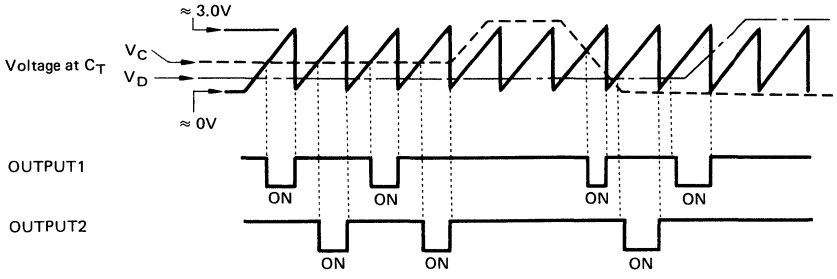


Fig. 3 – OPERATING TIMING



OSCILLATION FREQUENCY

$f_{OSC} \fallingdotseq 1.2/(R_T \cdot C_T)$

R_T : kΩ
C_T : μF
f_{OSC} : kHz

FUNCTION TABLE

Input (Output Control)	Output State
GND	Single-ended or parallel output
V_{REF}	Push-pull

TYPICAL ELECTRICAL CURVES

Fig. 4 – REFERENCE VOLTAGE vs. POWER SUPPLY VOLTAGE

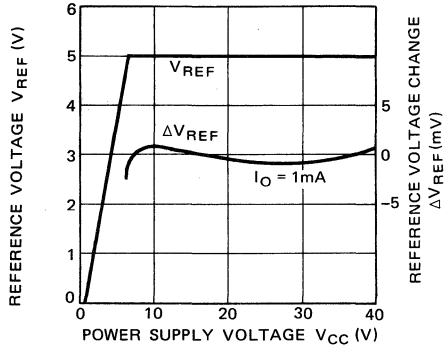


Fig. 5 – REFERENCE VOLTAGE vs. TEMPERATURE

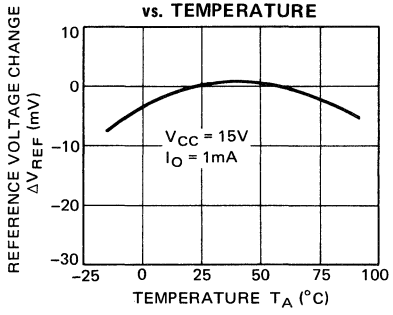


Fig. 6 – OSCILLATOR FREQUENCY vs. R_T, C_T

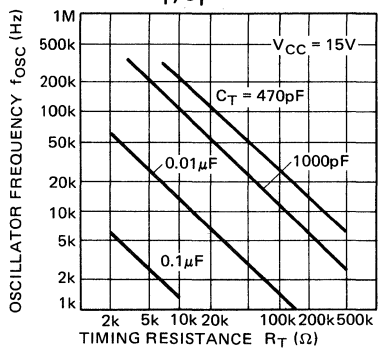


Fig. 7 – DUTY RATIO vs. DEAD TIME CONTROL VOLTAGE

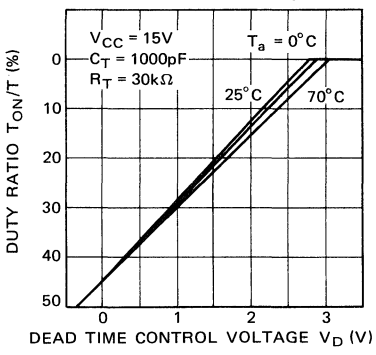


Fig. 8 – OPEN LOOP VOLTAGE AMPLIFICATION vs. FREQUENCY

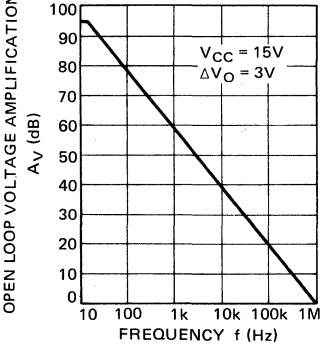
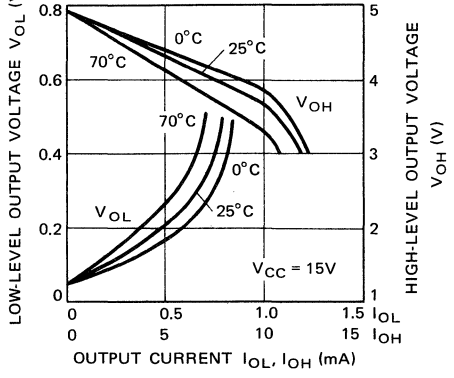


Fig. 9 – OUTPUT VOLTAGE vs. OUTPUT CURRENT (FEED BACK TERMINAL)



TYPICAL ELECTRICAL CURVES (continued)

Fig. 10 – COLLECTOR SATURATION VOLTAGE vs. COLLECTOR OUTPUT CURRENT

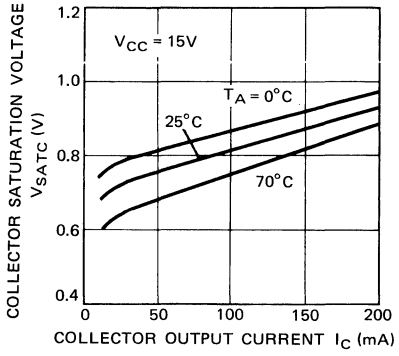


Fig. 11 – EMITTER SATURATION VOLTAGE vs. EMITTER OUTPUT CURRENT

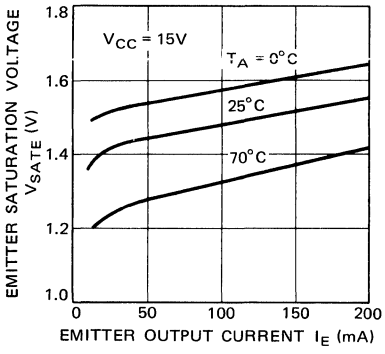


Fig. 12 – OUTPUT VOLTAGE vs. REFERENCE VOLTAGE

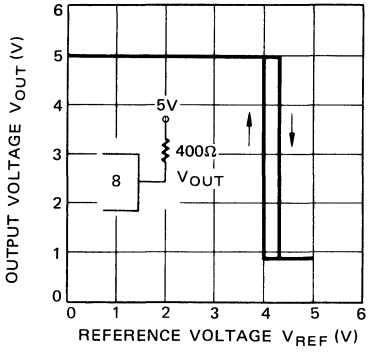


Fig. 13 – POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE

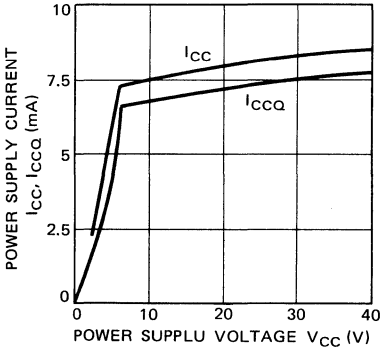
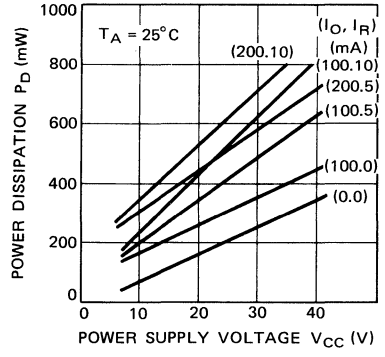
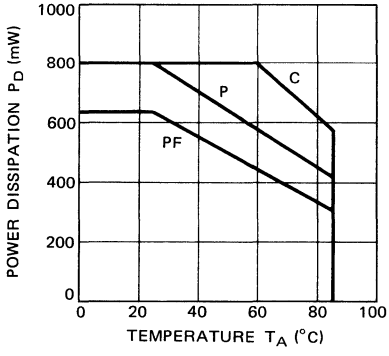


Fig. 14 – POWER DISSIPATION vs. POWER SUPPLY VOLTAGE



Note: I_O is collector output current at emitter grounded mode.

Fig. 15 – AVAILABLE POWER DISSIPATION vs. TEMPERATURE



Note: C (Ceramic DIP) P (Plastic DIP) PF (Plastic FPT)

TYPICAL APPLICATION

Fig. 16 – Chopper

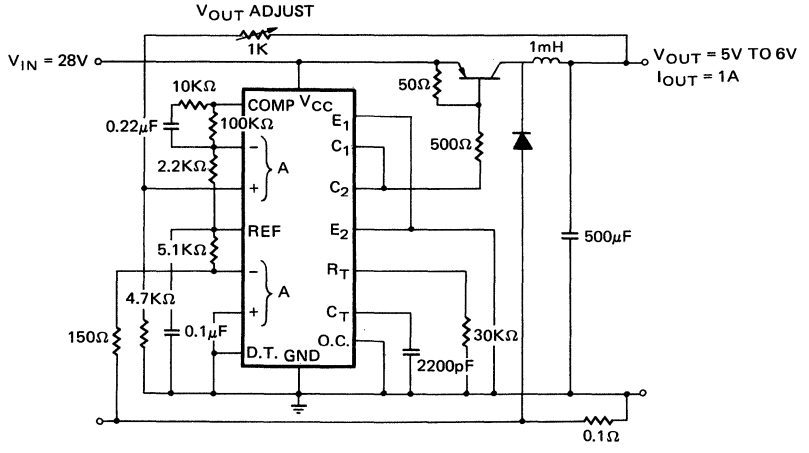
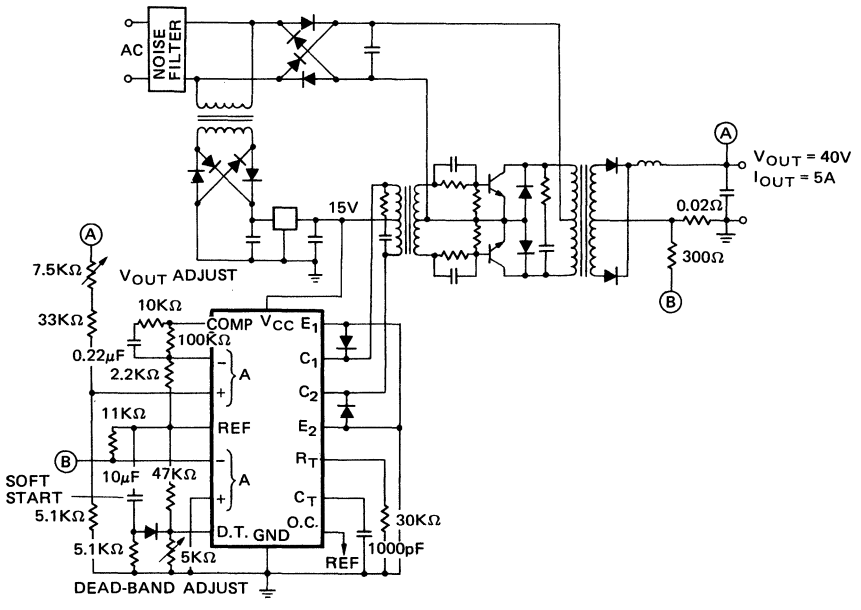
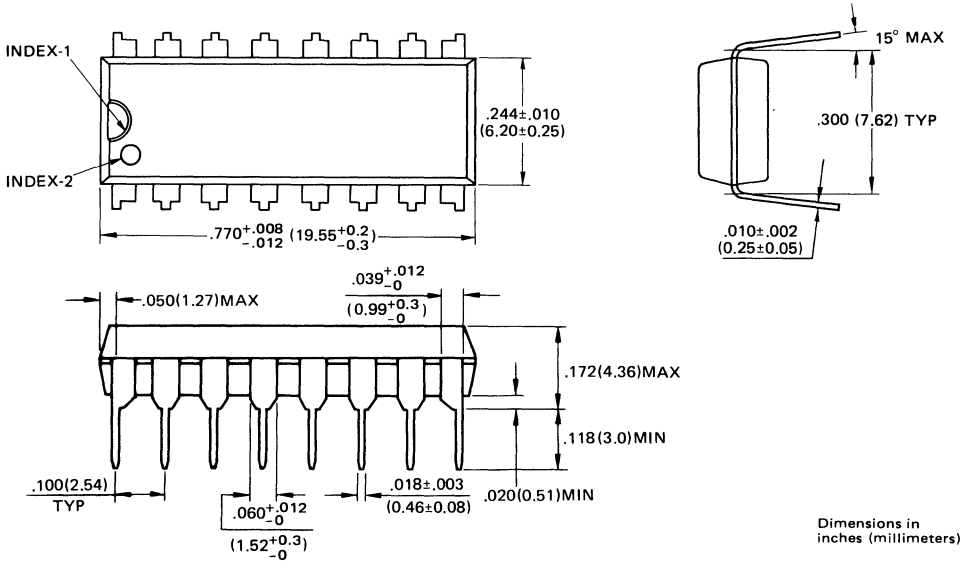


Fig. 17 – Operating from AC line



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)

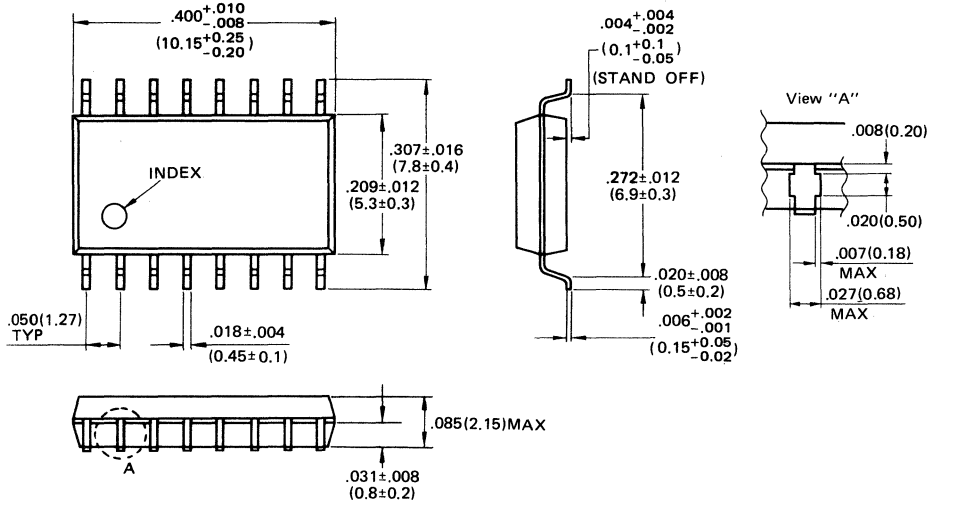


Dimensions in
inches (millimeters)

4

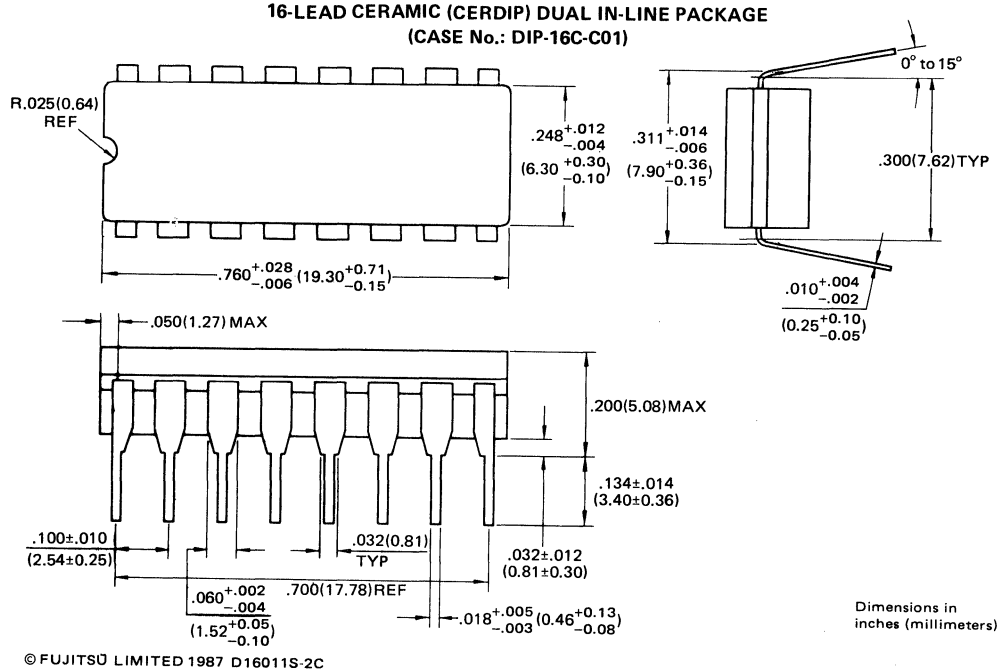
PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in inches (millimeters)

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-C01)



4

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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FUJITSU

VOLTAGE DETECTOR

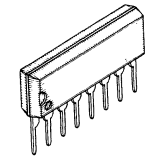
MB3761

October 1987
Edition 1.0

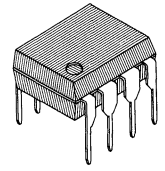
VOLTAGE DETECTOR

Designed for voltage detector applications, the Fujitsu MB3761 is a dual comparator with a built-in high precision reference voltage generator. Outputs are open-collector outputs and enable use of the OR-connection between both channels. Both channels have hysteresis control outputs. Because of a wide power supply voltage range and a low power supply current, the MB3761 is suitable for power supply monitors and battery backup systems.

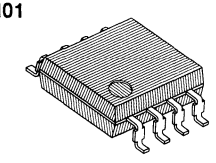
- Wide power supply voltage range: 2.5 V to 40 V
- Low power and small voltage dependency supply current: 250 μA typical.
- Built-in stable low voltage generator: 1.20 V typical.
- Easy-to-add hysteresis characteristics.
- Package: 8-pin Plastic SIP Package (Suffix: -PS)
  8-pin Plastic DIP Package (Suffix: -P)
  8-pin Plastic FPT Package (Suffix: -PF)



PLASTIC PACKAGE
SIP-08P-M03



PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

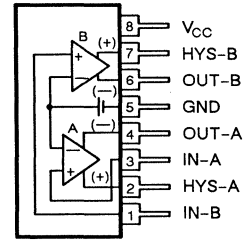
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	41	V
Output Voltage	V_O	41	V
Output Current	I_O	50	mA
Input Voltage	V_{IN}	-0.3 to +6.5	V
Power Dissipation	P_D	350 (TA ≤ 70°C)	mW
Storage Temperature	T_{STG}	-55 to 125	°C

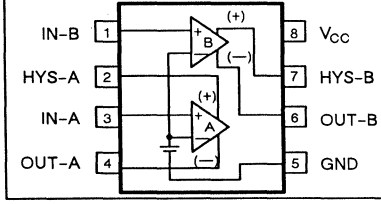
NOTE: Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

(FRONT VIEW)

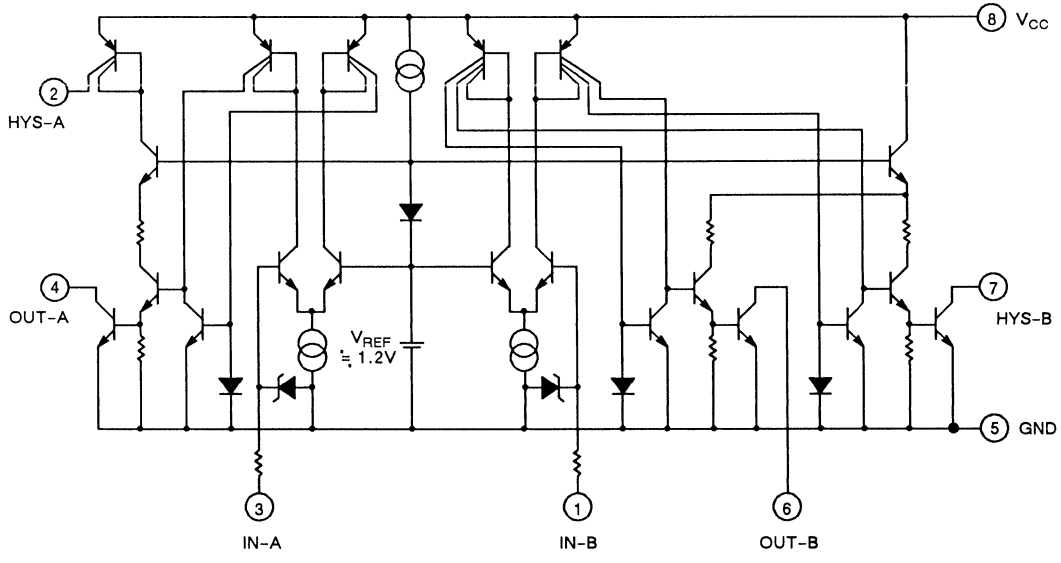


(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Figure 1. MB3761 Equivalent Circuit



4

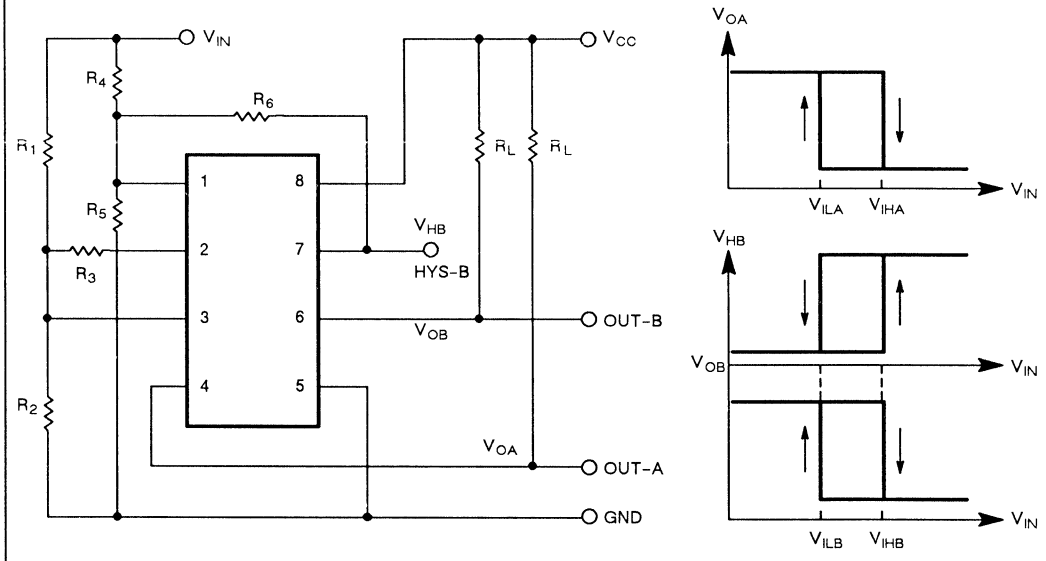
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	2.5 to 40	V
Operating Temperature	T_A	-20 to 75	°C
Output Current at pin 4	I_{O4}	4.5	mA
Output Current at pin 6	I_{O6}	3.0	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5V)

Parameter	Designator	Conditions	Values			Unit
			Min	Typ	Max	
Power Supply Voltage	I_{CCL}	V_{CC} = 40 V, V_{IL} = 1.0 V	—	250	400	µA
	I_{CCH}	V_{CC} = 40 V, V_{IH} = 1.5 V	—	400	600	µA
Threshold Voltage	V_{TH}	I_O = 2 mA, V_O = 1 V	1.15	1.20	1.25	V
Deviation of Threshold Voltage	ΔV_{TH1}	2.5 V ≤ V_{CC} ≤ 5.5 V	—	3	12	mV
	ΔV_{TH2}	4.5 V ≤ V_{CC} ≤ 40 V	—	10	40	mV
Offset Voltage between Outputs	V_{OOSA}	I_{OA} = 4.5 mA, V_{OA} = 2 V I_{HA} = 20 µA, V_{HA} = 3 V	—	2.0	—	mV
	V_{OSSB}	I_{OB} = 3 mA, V_{OB} = 2 V I_{HB} = 3 mA, V_{HB} = 2 V	—	2.0	—	mV
Temperature Coefficient of Threshold Voltage	α	-20°C ≤ T_A ≤ 70°C	—	±0.05	—	mV/°C
Difference Voltage on Threshold Voltage between Channel	ΔV_{THAB}		-10	—	10	mV
Input Current	I_{IL}	V_{IL} = 1.0 V	—	5	—	nA
	I_{IH}	V_{IH} = 1.5 V	—	100	500	nA
Output Leakage Current	I_{OH}	V_O = 40 V, V_{IL} = 1.0 V	—	—	1	µA
Hysteresis Output Leakage Current	I_{HLA}	V_{CC} = 40 V, V_{HA} = 0 V, V_{IL} = 1.0 V	—	—	0.1	µA
	I_{HHB}	V_{HB} = 40 V, V_{IH} = 1.5 V	—	—	1	µA
Output Sink Current	I_{OLA}	V_O = 1.0 V, V_{IH} = 1.5 V	6	12	—	mA
	I_{OLB}	V_O = 1.0 V, V_{IH} = 1.5 V	4	10	—	mA
Hysteresis Current	I_{HHA}	V_H = 0 V, V_{IH} = 1.5 V	40	80	—	µA
	I_{HLB}	V_H = 1.0 WV_{IL} = 1.0 V	4	10	—	mA
Output Saturation Voltage	V_{OLA}	I_O = 4.5 mA, V_{IH} = 1.5 V	—	120	400	mV
	V_{OLB}	I_O = 3.0 mA, V_{IH} = 1.5 V	—	120	400	mV
Hysteresis Saturation Voltage	V_{HHA}	I_H = 20 µA, V_{IH} = 1.5 V	—	50	200	mV
	V_{HLB}	I_H = 3.0 mA, V_{IL} = 1.0 V	—	120	400	mV
Output Delay Time	t_{PHL}	R_L = 5 KΩ	—	2	—	µs
	t_{PLH}	R_L = 5 KΩ	—	3	—	µs

Figure 2. Operational Definitions



$V_{IHA} = (1 + \frac{R_1}{R_2}) V_R$

$V_{ILA} = (1 + \frac{R_1}{R_2 // R_3}) V_R - \frac{R_1}{R_3} V_{CC}$

$V_{IHB} = (1 + \frac{R_4}{R_5 // R_6}) V_R$

$V_{ILB} = (1 + \frac{R_4}{R_5}) V_R$

$V_R \fallingdotseq V_{TH} (\fallingdotseq 1.20V)$

$R_2 // R_3 = \frac{R_2 R_3}{R_2 + R_3}$

$R_5 // R_6 = \frac{R_5 R_6}{R_5 + R_6}$

4

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Power Supply Current vs Power Supply Voltage

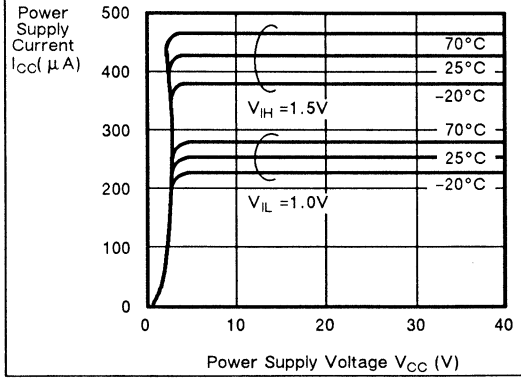
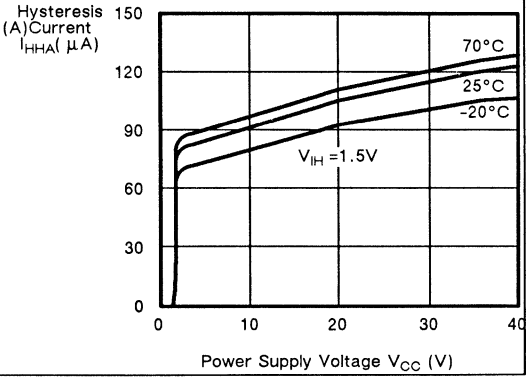


Fig. 4 – Hysteresis (A) Current vs Power Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 5 – Output (A) Voltage vs. Output (A) Current

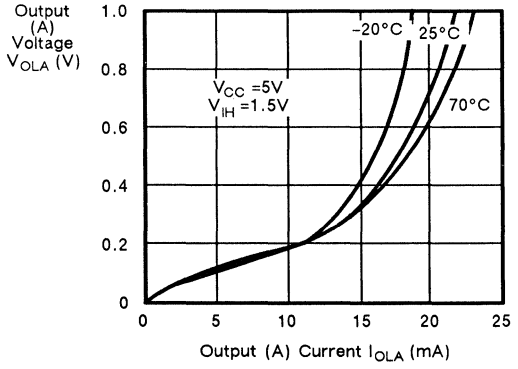


Fig. 6 – Output (B) Voltage vs. Output (B) Current

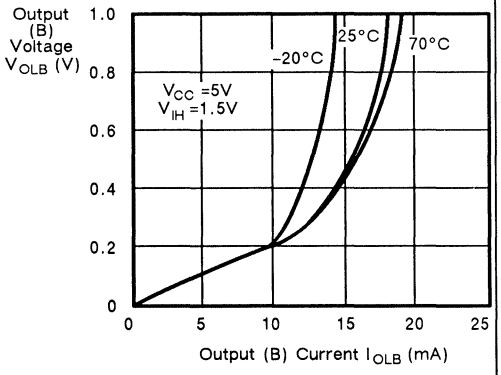


Fig. 7 – Threshold Voltage vs. Power Supply Voltage

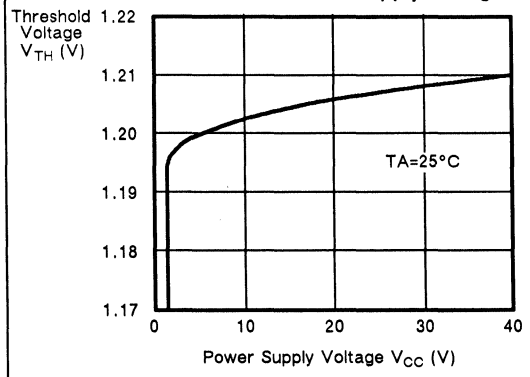
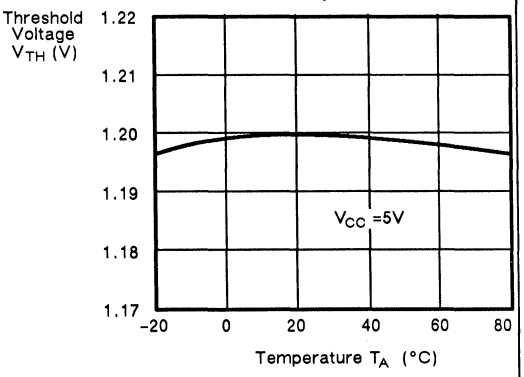
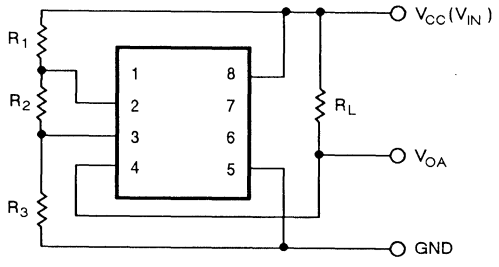


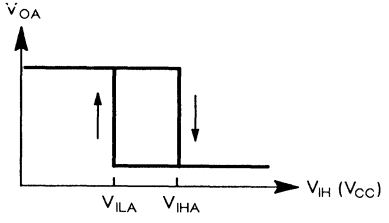
Fig. 8 – Threshold Voltage vs. Temperature



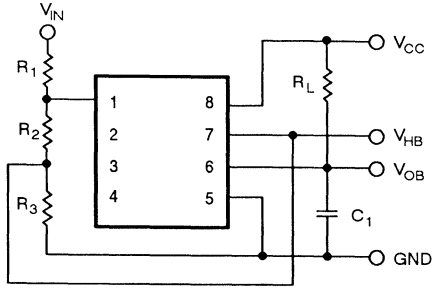
APPLICATION EXAMPLES

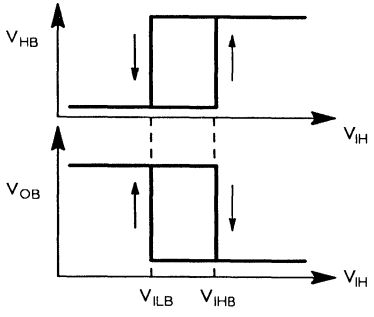
Figure 9. Addition of Hysteresis





$$V_{IHA} = (1 + \frac{R_1 + R_2}{R_3})V_R \qquad V_{ILA} = (1 + \frac{R_2}{R_3})V_R$$



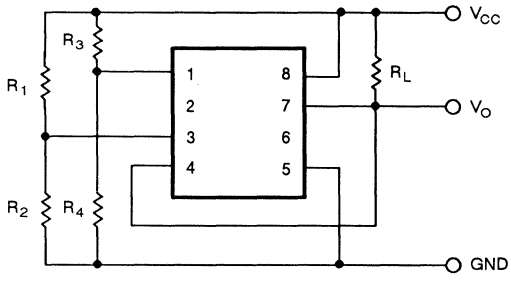


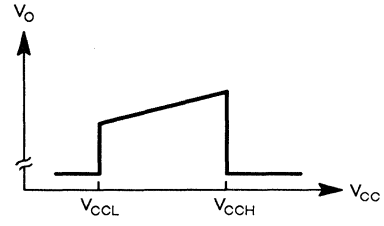
Note: All calculations occur with the output voltage at 0. The hysteresis values are adjusted for load condition and saturation voltage.

$$V_{IHB} = (1 + \frac{R_1}{R_2})V_R \qquad V_{ILB} = (1 + \frac{R_1}{R_2 + R_3})V_R$$

APPLICATION EXAMPLES (Continued)

Figure 10. Voltage Detection for Alarm



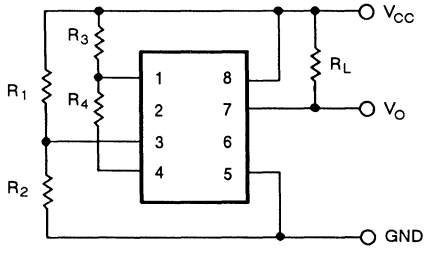


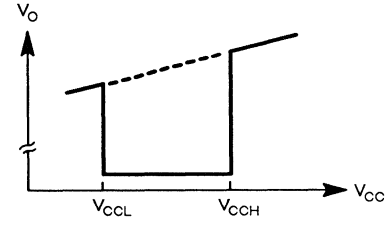
$$V_{CCH} = (1+\frac{R_1}{R_2})V_R \qquad V_{CCL} = (1+\frac{R_3}{R_4})V_R$$

$$V_{CCL} \geqq 2.5V$$

For hysteresis, a positive feedback from pin 2 or 7 is required.

Figure 11. Voltage Detection for Alarm



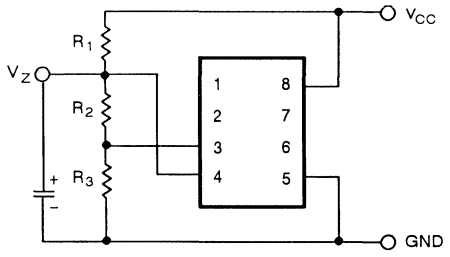


$$V_{CCH} = (1+\frac{R_3}{R_4})V_R \qquad V_{CCL} = (1+\frac{R_1}{R_2})V_R$$

$$V_{CCL} \geqq 2.5V$$

APPLICATION EXAMPLES (Continued)

Figure 12. Programmable Zener

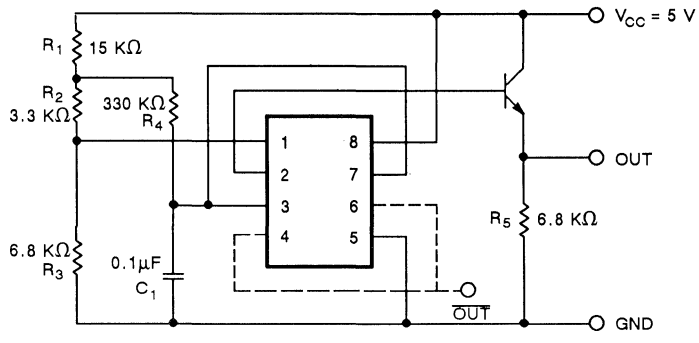


$$V_Z \fallingdotseq (1+\frac{R_2}{R_3})V_R$$

$$\frac{V_Z}{R_2+R_3} \leqq \frac{V_{CC}-V_Z}{R_1} \leqq 6mA$$

Channel B can be used independently.

Figure 13. Recovery Reset Circuit



APPLICATION EXAMPLES (Continued)

Figure 14. DC Characteristics

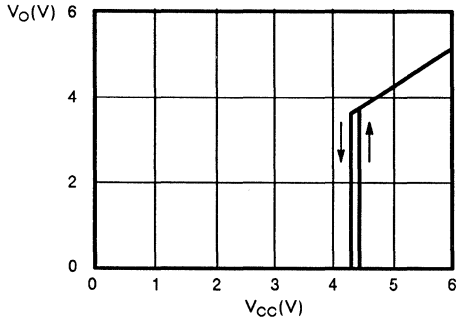
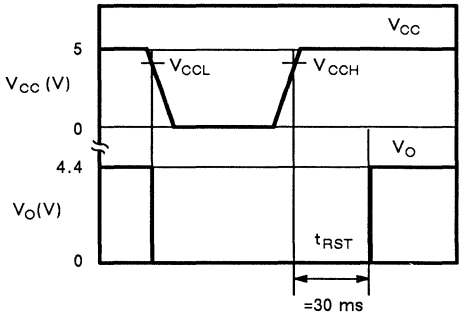


Figure 15. Response Characteristics



- Voltage Threshold Levels (V_{CCL} and V_{CCH}) and Hysteresis Width can be changed by the resistors (R_1 through R_4).

$$V_{CCL} = \frac{R_1 + R_2 + R_3}{R_3} V_{TH}$$

$$V_{CCH} = V_{CCL} + \frac{R_1 (R_2 + R_3)}{R_3 R_4} V_{TH}$$

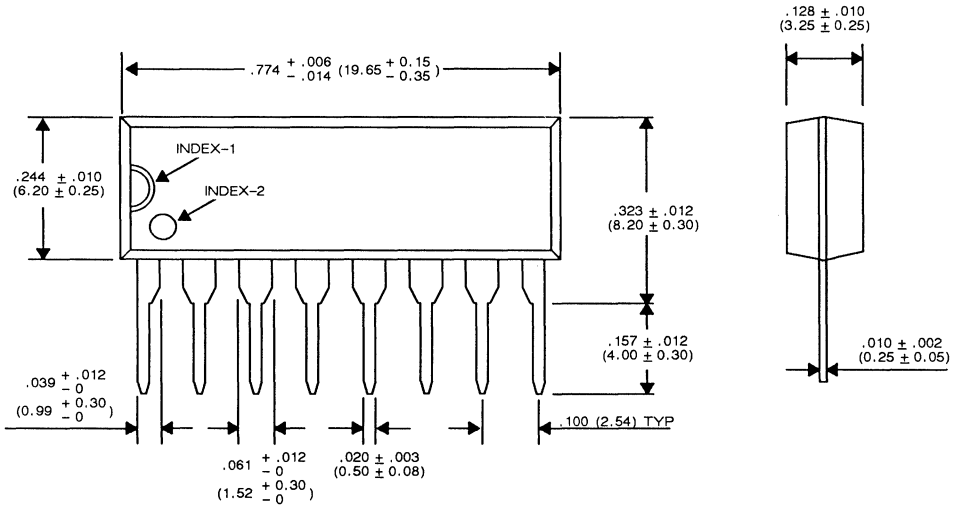
- Power-On Reset Time is provided by the following approximate equation:

$$t_{RST} = {}^{-}C_1 R_4 \cdot 1n \left\{ 1 - \frac{V_{TH}}{V_{CC}} \left(1 + \frac{R_1}{R_2 + R_3} \right) \right\}$$

- The recommended value of h_{FE} of the external transistor is from 50 to 200.
- In the case of an instant power fall, the remaining charge in C_1 effects t_{RST}.
- If necessary, the reversed output is provided on HYS terminal

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-08P-M03)



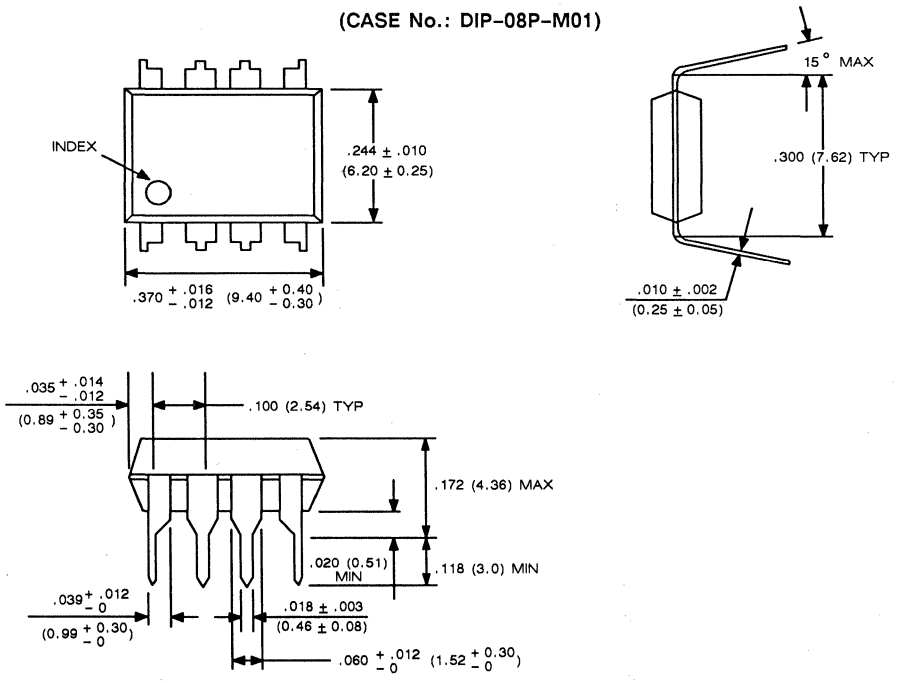
Dimensions in
inches (millimeters)

S08010S-2C

4

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)

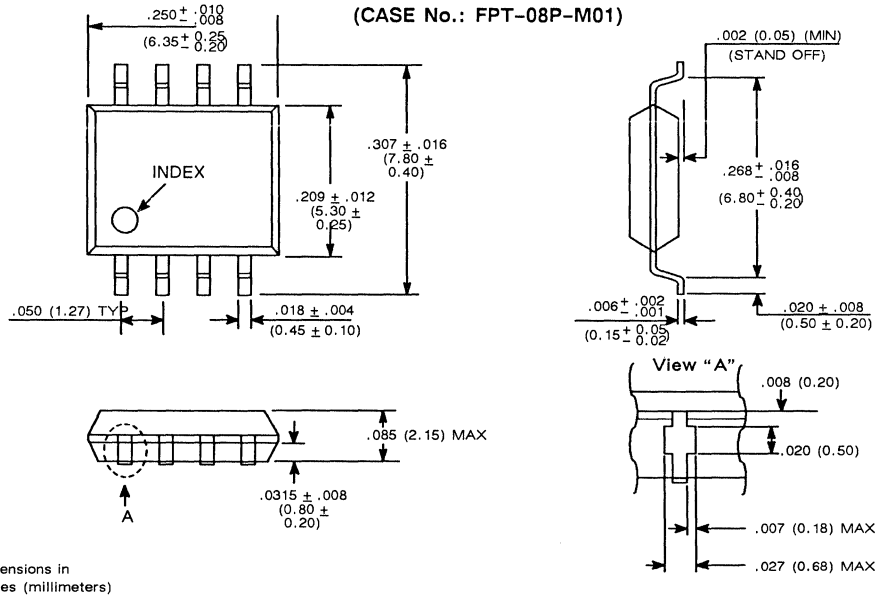


Dimensions in
inches (millimeters)

D08006S-2C

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
inches (millimeters)

F08002S-2C

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Printed in USA OV0019-87XF1

August 1988
Edition 1.0

FUJITSU

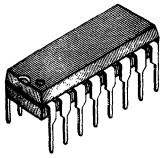
FUJITSU MICROELECTRONICS, INC.

MB3769

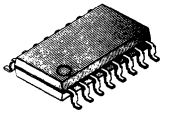
Product Profile

High Speed PWM Control Circuit

This device is a pulse width modulation control monolithic IC with internal high speed comparator and op amp for high frequency switching regulator system (up to 500kHz). It has a totem-pole output to drive power MOS FET, power supply standby mode and primary control functions.



PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

4

Features

- High Frequency Switching Operation (f = 1 ~ 500kHz)
- Internal Wide Band Op Amp (BW = 8MHz typ.)
- Internal High Speed Comparator (t_{pd} = 150ns typ.)
- Low Power Consumption (1.5mA at standby, 8mA at operation)
- High Current Drive with Totem Pole Output (±100mA, ±600mA peak)
- Dead Time Adjustable
- Soft Start and Quick Shutdown Functions
- Protection for a Stable Operation at Low Voltage
- Over Voltage Protection

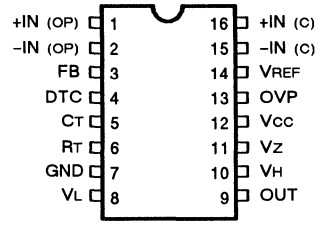
ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Maximum Ratings Values		Unit
		DIP Package	SOP Package	
Supply Voltage	V_{CC}	20	20	V
Output Current	I_O	120 (660*1)	120 (660*1)	mA
Input Voltage for Op Amp	$V_{IN\ (OP)}$	V_{CC} +0.3 (<20)	V_{CC} +0.3 (<20)	V
Power Dissipation	P_D	1000*2	620*3	mW
Operating Temperature	T_{OP}	-20 ~ +80	-20 ~ +75	°C
Storage Temperature	T_{stg}	-55 ~ +125	-55 ~ +125	°C

*1: Duty ≤ 5%
*2: T_A = 25°C
*3: T_A = 25°C, Soldered on Epoxy Board of 40mm x 40mm

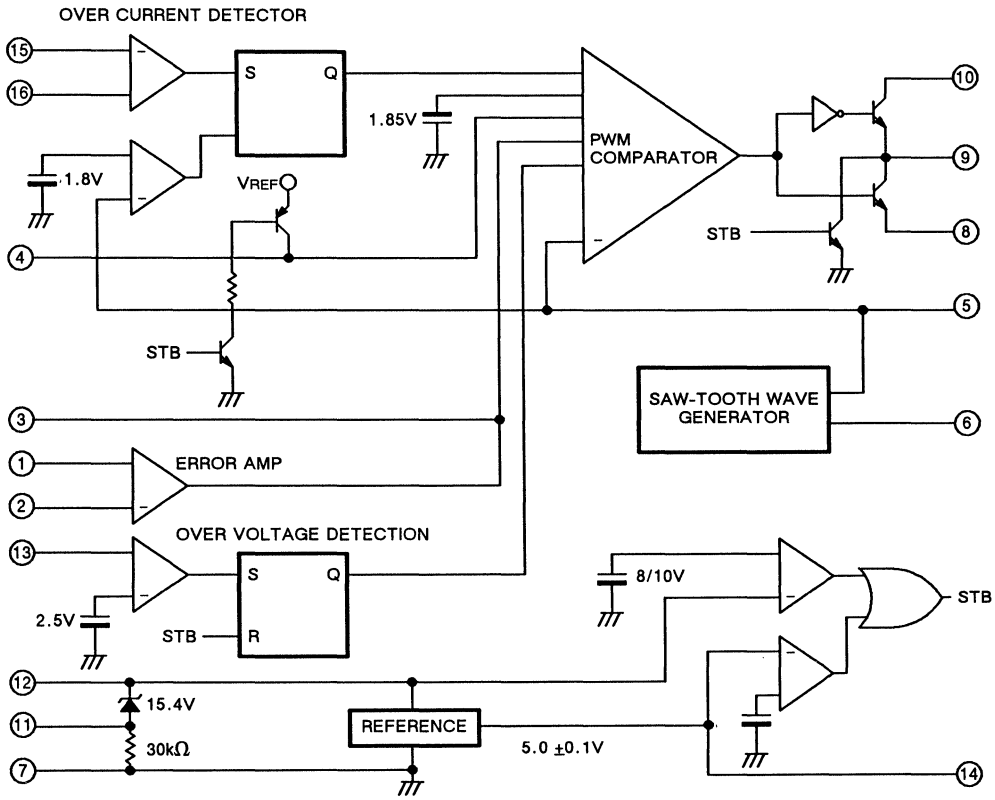
PIN ASSIGNMENT

(TOP VIEW)



4

FUNCTION BLOCK



Recommended Operating Conditions

Item	Symbol	DIP Package			SOP Package			Unit
		Max	Typ	Min	Max	Typ	Min	
Supply Voltage	V_{CC}	12	15	18	12	15	18	V
Output Current (DC)	I_{OUT}	-100	—	100	-100	—	100	mA
Output Current (Peek)	$I_{O\ PEEK}$*	-600	—	600	-600	—	600	mA
Op Amp Input Voltage	$V_{IN\ OP}$	-0.2	0 ~ V_R	V_{CC} - 3	-0.2	0 ~ V_R	V_{CC} - 3	V
FB Sink Current	I_{SINK}	—	—	0.3	—	—	0.3	mA
FB Source Current	I_{SOURCE}	—	—	2	—	—	2	mA
Comparator Input Voltage	V_{IN} C+	-0.3	0 ~ 3	V_{CC}	-0.3	0 ~ 3	V_{CC}	V
	V_{IN} C-	-0.3	0 ~ 2	2.5	-0.3	0 ~ 2	2.5	V
V_{REF} Output Current	I_{REF}	—	5	10	—	2	10	mA
Timing Resistor	R_T	9	18	50	9	18	50	kΩ
Timing Capacitor	C_T	100	680	10^6	100	680	10^6	pF
Oscillator Frequency	f_{OSC}	1	100	500	1	100	500	kHz
Zener Current	I_Z	—	—	5	—	—	5	mA
Operating Temperature	T_{OP}	-20	—	+85	-20	—	+75	°C

*Duty ≤ 5%

Electrical Characteristics

V_{CC} = 6V; T_A = 25°C

Block	Item	Symbol	Condition	Max	Typ	Min	Unit
Reference Voltage	Output Voltage	V_{REF}	I_{REF} = 1mA	4.9	5.0	5.1	V
	Input Stability	ΔV_{RIN}	12V ≤ V_{CC} ≤ 10mA	—	2	15	mV
	Load Stability	ΔV_{RLD}	1mA ≤ I_{REF} ≤ 10mA	—	-1	-15	mV
	Temperature Stability	ΔV_{RTEMP}	-20 °C ~ +85°C	—	±200	±700	μv/°C
	OutputShort Current	I_{SC}	V_{REF} = 0V	15	40	—	mA
Oscillator	Oscillator Frequency	f_{OSC}	R_T = 18kΩ, C_T = 680pF	90	100	110	kHz
	Frequency Stability	$\Delta f_{OSC\ IN}$	V_{CC} = 12 ~ 18V	—	±0.03	—	%
	Temperature Stability	$\Delta f_{OSC}/T$	T_A = -20 ~ +85°C	—	±2	—	%
Output	Output "H" Voltage	V_H	I_{OUT} = -100mA	12.5	13.5	—	V
	Output "L" Voltage	V_L	I_{OUT} = 100mA	—	1.1	1.3	V
	Rise Time	tr	C_L = 1000pF, R_L = ∞	—	60	—	nsec
	Fall Time	tf		—	30	—	nsec

Electrical Characteristics (Continued)

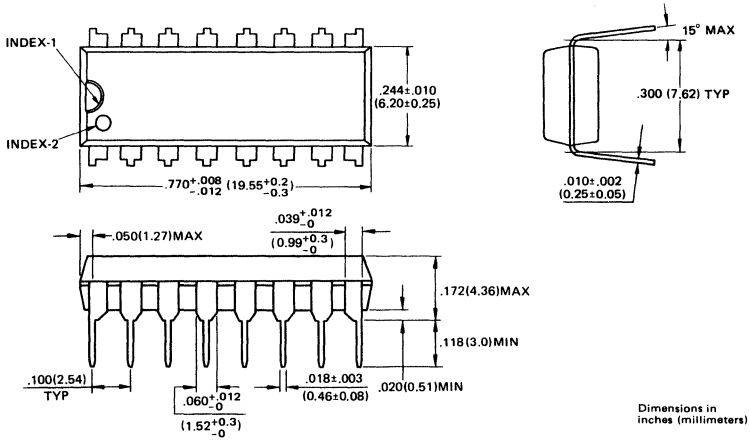
VCC = 6V; TA = 25°C

Block	Item		Symbol	Condition	Max	Typ	Min	Unit
Dead Time Control	Input Bias Current		I_D		—	2	10	μA
	Maximum Duty Cycle		D_{MAX}	V_4 = 1.5V	70	80	90	%
	Input Voltage	0% Duty	V_{DD}		—	3.5	3.8	V
		Max. Duty	V_{DM}		1.55	1.85	—	V
	Discharge Voltage		V_{DH}	V_{CC} = 7V, I_{DTC} = −0.3mA	4.5	—	—	V
Error Amp	Input Offset Voltage		$V_{IO\ (OP)}$	V_3 = 2.5V	—	±2	±10	mV
	Input Offset Current		$I_{IO\ (OP)}$		—	±30	±300	nA
	Input Bias Current		$I_{IB\ (OP)}$		−1	−0.3	—	μA
	Common Input Voltage		$V_{CM\ (OP)}$	12V ≦ V_{CC} ≦ 20V	−0.2	—	V_{CC} − 3	V
	Voltage Gain		$A_{V\ (OP)}$	0.5V ≦ V_3 ≦ 4V	70	90	—	dB
	Gain Band Width		BW	A_V = 1	—	8	—	MHz
	Slew Rate		SR	R_L = 10kΩ, A_V = 1	—	6	—	V/μs
	Common Rejection Ratio		CMR	V_{IN} = 0 ~ 10V	65	80	—	dB
	Output "H" Voltage		V_{OH}	I_3 = −2mA	4.0	4.6	—	V
	Output "L" Voltage		V_{OL}	I_3 = 0.3mA	—	0.1	1.5	V
Current Comparator	Input Offset Voltage		$V_{IO\ (C)}$	V_{IN} = 1V	—	±5	±15	mV
	Input Bias Voltage		$V_{IB\ (C)}$		−5	−1	—	μA
	Common Input Voltage		$V_{CM\ (C)}$		0	—	2.5	V
	Voltage Gain		$A_{V\ (C)}$		—	200	—	V/V
	Response Time		td	50mV over drive	—	150	—	nsec
PWM Comparator Input Voltage	0% Duty Cycle		V_{OPO}	3-pin Voltage	—	3.5	3.8	V
	Maximum Duty Cycle		V_{OPM}	R_T = 18kΩ, C_T = 680pF	1.55	1.85	—	V
Over Voltage Detector	Operating Voltage		V_{OVP}		2.4	2.5	2.6	V
	Input Current		I_{IOVP}	V_{IN} = 1V	−1.0	−0.2	—	μA
Shutdown at Low Supply	OFF → ON		V_{THH}		9.2	10.0	10.8	V
	ON → OFF		V_{THL}		7.2	8.0	8.8	V
Supply Current	Stand-by Mode		I_{CCSTB}	R_T = 18kΩ	—	1.5	2.0	mA
	Operating Mode		I_{CC}		—	8.0	12.0	V
Zener Voltage			V_Z	I_Z = 1mA	—	15.4	—	V
Zener Current			I_Z	V_{11-7} = 1V	—	0.03	—	mA

4

4

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in
inches (millimeters)

FUJITSU

POWER SUPPLY MONITOR

MB 3771

August 1988
Edition 1.1

POWER SUPPLY MONITOR

The Fujitsu MB 3771 is designed to monitor the voltage level of one or two power supplies (+5V and an arbitrary voltage) in a microprocessor circuit, memory board in large-size computer, for example.

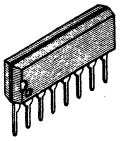
If the circuit's power supply deviates more than a specified amount, then the MB 3771 generates a reset signal to the microprocessor. Thus, the computer data is protected from accidental erasure.

Using the MB 3771 requires few external components. To monitor only a +5V supply, the MB 3771 requires the connection of one external capacitor. The level of an arbitrary dectection voltage is determined by two external resistors.

The MB 3771 is available in an 8-pin Dual In-Line, Signal In-Line Package or space saving Flat Package.

- Precision voltage detection (V_{SA} = 4.1 to 4.3 V)
- User selectable threshold level with hysterisis ($V_{SB} \geqq 1.24$ V)
- Monitors the voltage of one or two power supplies (5 V and an arbitrary voltage, $\geqq 1.23$ V)
- Low voltage output for reset signal (V_{CC} = 0.8 V typ.)
- Minimal number of external components (one capacitor min.)
- Low power dissipation (I_{CC} = 0.35 mA typ., V_{CC} = 5 V)
- Available in a variety of packages
  - 8-pin Dual In-Line Package
  - 8-pin Single In-Line Package
  - 8-pin Flat Package

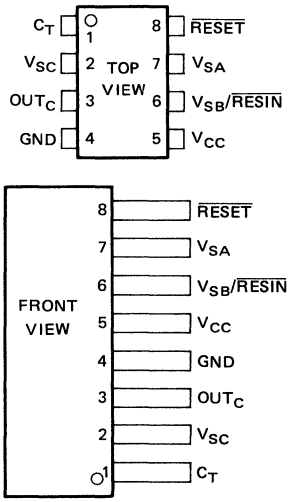
PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
SIP-08P-M03

FPT-08P-M01: See page 20

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

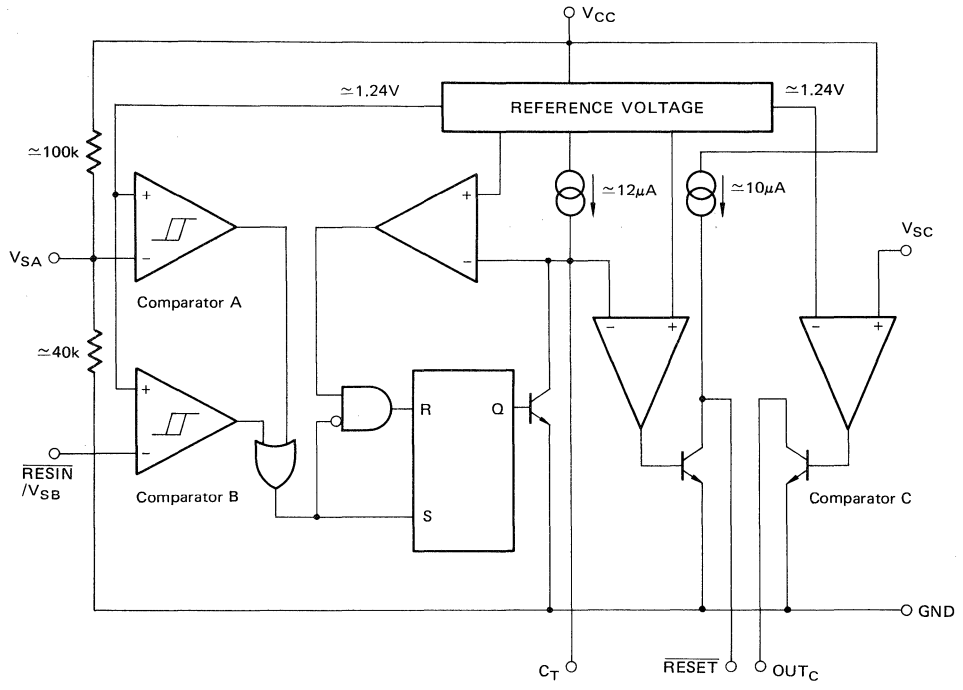
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +20	V
Input Voltage A	V_{SA}	-0.3 to V_{CC}+0.3 (<+20)	V
Input Voltage B	V_{SB}	-0.3 to +20	V
Input Voltage C	V_{SC}	-0.3 to +20	V
Power Dissipation	P_D	200 ($T_A \leqq 85°C$)	mW
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

BLOCK DIAGRAM OF MB 3771



FUNCTIONAL EXPLANATIONS

Detection voltage inputs A and B are connected to the inverting input of Comparators A and B respectively. Both comparators have built-in hysterisis. If either V_{SA} or V_{SB} drops lower than about 1.23V, then $\overline{RESET}$ goes low.

Comparator B is used for the arbitrary preset voltage detection (See Example 3), or as forced reset input for TTL logic level input. (See Example 6)

Comparator C is designed as an open-collector output with inverted polarity input/output characteristics. Comparator C has no hysteresis. It can be used for over-voltage detection (See Example 11), generation of $\overline{RESET}$ signal by positive logic (See Example 7), and generation of reference voltage (See Example 10).

Note that V_{SB} and V_{SC} should be connected with V_{CC} and GND respectively. (See Example 1.)

The MB 3771 can detect about 2μs voltage sag/surge of the power supply. The user can add delayed trigger capacity by connecting a capacitor between inputs V_{SA} and V_{SB}. (See Example 8)

Internal pull-up resistor on the $\overline{RESET}$ line provides for high impedance loading (i.e. CMOS logic).

RECOMMENDED OPERATING CONDITIONS

parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+3.5 to +18	V
Output Current ($\overline{RESET}$)	I_{RESET}	0 to 20	mA
Output Current (OUT_C)	I_{OUTC}	0 to 6	mA
Operating Ambient Temperature	T_A	-40 to +85	°C

ELECTORICAL CHARACTERISTICS

DC Characteristics (V_{CC} = 5V, T_A = 25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Supply Current	V_{SB} = 5V, V_{SC} = 0V	I_{CC1}		350	500	μA
	V_{SB} = 0V, V_{SC} = 0V	I_{CC2}		400	600	μA
Sagging Detection Voltage Falling	V_{CC}	V_{SAL}	4.10	4.20	4.30	V
	V_{CC}, T_A = -40 to +85°C		4.05	4.20	4.35	V
Rising	V_{CC}	V_{SAH}	4.20	4.30	4.40	V
	V_{CC}, T_A = -40 to +85°C		4.15	4.30	4.45	V
Hysterisis Width		V_{HYSA}	50	100	150	mV
Sagging Detection Voltage	V_{SB}	V_{SB}	1.212	1.230	1.248	V
	V_{SB}, T_A = -40 to +85°C		1.200	1.230	1.260	V
Deviation of Detection Voltage	V_{CC} = 3.5 to 18V	$\triangle V_{SB}$		3	10	mV
Hysterisis Width		V_{HYSB}	14	28	42	mV
Input Current	V_{SB} = 5V	I_{IHB}		0	250	nA
	V_{SB} = 0V	I_{ILB}		20	250	nA
High-level Output Voltage	I_{RESET} = -5μA, V_{SB} = 5V	V_{OHR}	4.5	4.9		V
Output Saturation Voltage	I_{RESET} = 3mA, V_{SB} = 0V	V_{OLR}		0.28	0.4	V
	I_{RESET} = 10mA, V_{SB} = 0V			0.38	0.5	V
Output Sink Current	V_{OLR} = 1.0V, V_{SB} = 0V	I_{RESET}	20	40		mA
C_T Charge Current	V_{SB} = 5V, V_{CT} = 0.5V	I_{CT}	9	12	16	μA

ELECTORICAL CHARACTERISTICS (Cont'd)

DC Characteristics (V_{CC} = 5V, T_A = 25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Current	V_{SC} = 5V	I_{IHC}		0	500	nA
	V_{SC} = 0V	I_{ILC}		50	500	nA
Detection Voltage	V_{SC}	V_{SC}	1.225	1.245	1.265	V
	V_{SC}, T_A = −40 to +85°C		1.205	1.245	1.285	V
Deviation of Detection Voltage	V_{CC} = 3.5 to 18V	$\triangle V_{SC}$		3	10	mV
Output Leakage Current	V_{OHC} = 18V	I_{OHC}		0	1	μA
Output Saturation Voltage	I_{OUTC} = 4mA, V_{SC} = 5V	V_{OLC}		0.15	0.4	V
Output Sink Current	V_{OLC} = 1.0V, V_{SC} = 5V	I_{OUTC}	6	15		mA
Reset Operation Minimum Supply Voltage	V_{OLR}=0.4V, I_{RESET}=200μA	V_{CCL}		0.8	1.2	V

AC Characteristics (V_{CC} = 5V, T_A = 25°C, C_T = 0.01μF)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Pulse Width	V_{SA}, V_{SB}	t_{PI}	5.0			μs
RESET Output Pulse Width		t_{PO}	0.5	1.0	1.5	ms
RESET Rising Time	R_L = 2.2kΩ, C_L = 100pF	t_R		1.0	1.5	μs
RESET Falling Time	R_L = 2.2kΩ, C_L = 100pF	t_F		0.1	0.5	μs
Propagation Delay Time	V_{SB}	t_{PD}		2	10	μs
	V_{SC}, R_L = 2.2kΩ, C_L = 100pF	t_{PHL}		0.5		μs
	V_{SC}, R_L = 2.2kΩ, C_L = 100pF	t_{PLH}		1.0		μs

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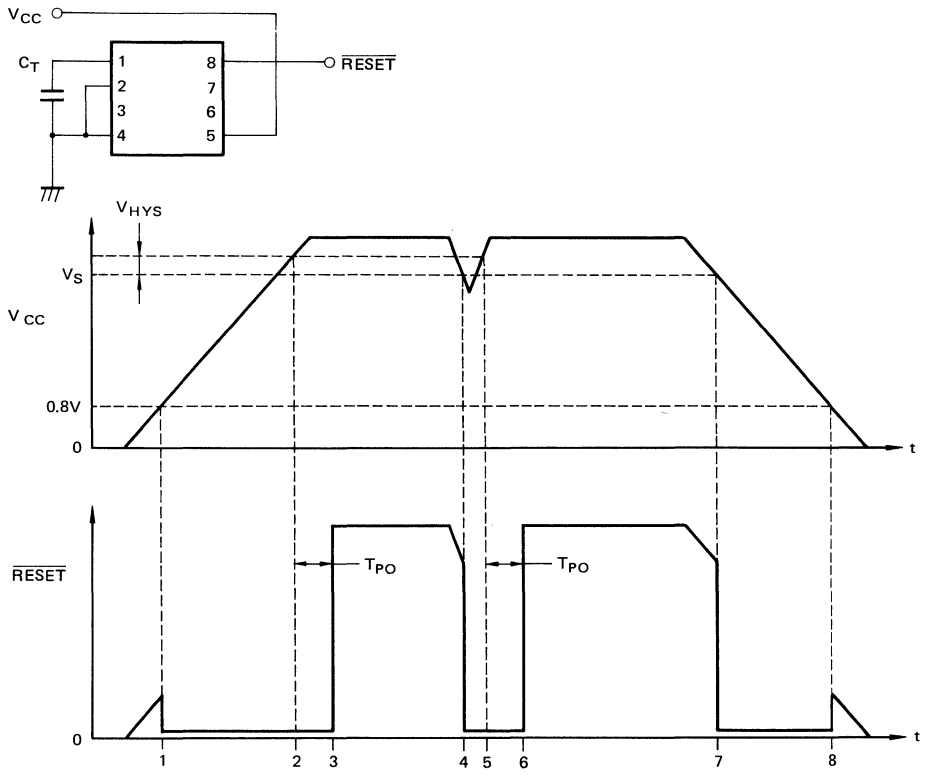
FUNCTION EXPLANATION



Point 1: When V_{CC} rises to about 0.8V, $\overline{RESET}$ goes low.

Point 2: When V_{CC} reaches $V_S + V_{HYS}$, C_T then begins charging. $\overline{RESET}$ remains low during this time.

Point 3: $\overline{RESET}$ goes high when C_T begins charging.

$$T_{OP} \simeq C_T \times 10^5 \text{ [ms]}$$

Point 4: When V_{CC} level drops lower then V_S, then $\overline{RESET}$ goes low and C_T starts discharging.

Point 5: When V_{CC} level reaches $V_S + V_{HYS}$, then C_T starts charging.

In the case of voltage sagging, if the period from the time V_{CC} goes lower than or equal to V_S to the time V_{CC} reaches $V_S + V_{HYS}$ again, is longer than t_{P1}, (as speicified in the AC Characteristics), C_T is discharged and charged successively.

Point 6: After T_{PO} passes, and V_{CC} level exceeds $V_S + V_{HYS}$, then $\overline{RESET}$ goes high.

Point 7: Same as Point 4.

Point 8: $\overline{RESET}$ remains low until V_{CC} drops below 0.8V.

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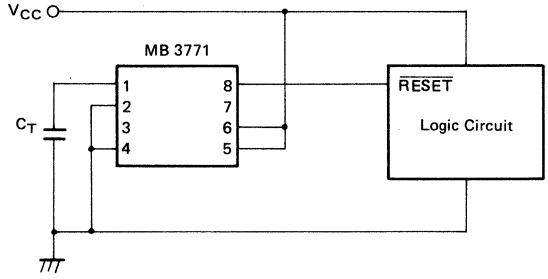
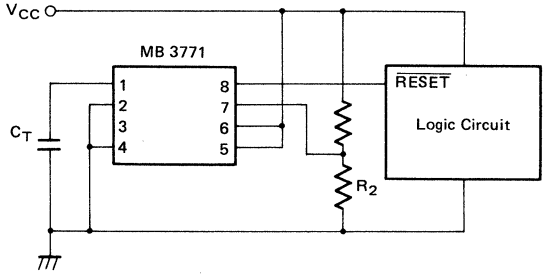
EXAMPLE 1: 5V Power Supply Monitor



NOTE: Monitored by V_{SA}. Detection Threshold Voltage is V_{SAL} and V_{SAH}.

EXAMPLE 2: 5V Power Supply Monitor with external adjust

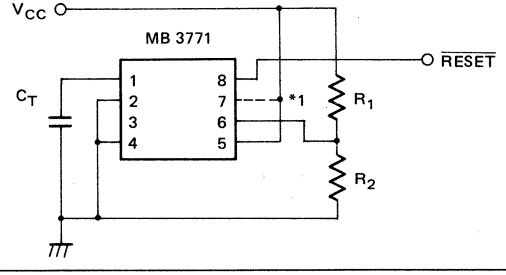


NOTE: Detection voltages can be adjusted as shown below.

R_1 [kΩ]	R_2 [kΩ]	Detection Voltage	
		V_{SAL} [V]	V_{SAH} [V]
10	3.9	4.4	4.5
9.1	3.9	4.1	4.2

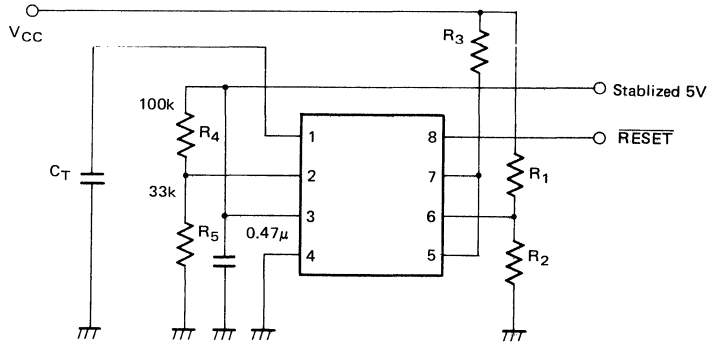
EXAMPLE 3: Arbitrary Voltage Supply Monitor

Example 3a: Case: $V_{CC} < 18V$



EXAMPLE 3: Arbitrary Voltage Supply Monitor

Example 3b: Case: $V_{CC} \geqq 18V$

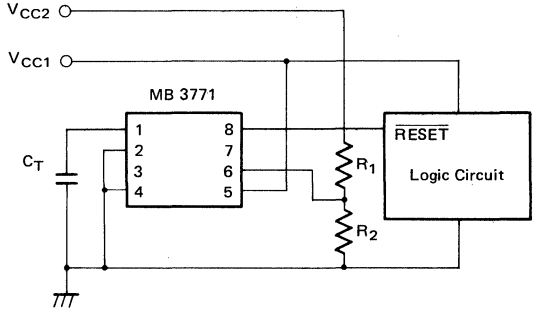


- $\overline{RESET}$ output levels range from 0V to 1V approximately. Device damage may occur if $\overline{RESET}$ exceeds its high level (1V).
- Output voltage and maximum $\overline{RESET}$ voltage levels are determined by resistor R_1 and R_2.
- In this case, the 5V stabilized output can be used to power TTL circuitry.
- Using the chart below, the value of R_3 can be determined with respect to the output current.

V_{CC} [V]	Detection Voltage [V]	Min. V_{CC}* for adequat RESET [V]	R_1 [MΩ]	R_2 [kΩ]	R_3 [kΩ]	Output Current [mA]
140	100	6.7	1.6	20	110	<0.2
100	81	3.8	1.3	20	56	<0.5
40	33	1.4	0.51	20	11	<1.6

NOTE: Resistor values are determined when $I_{OUTC} = 100\mu A$, $V_{OLC} = 0.4V$. All resistor are 1/4W.

EXAMPLE 4: 5V and 12V Power Supply Monitor ($V_{CC1} = 5V$, $V_{CC2} = 12V$)



NOTE: 5V is monitored by V_{SA}. Detection voltage is about 4.2V.

12V is monitored by V_{SB}. When $R_1 = 390k\Omega$ and $R_2 = 62k\Omega$, Detection voltage is about 9.0V. Generally the detection voltage is determined by the following equation.

Detection Voltage = $(R_1 + R_2) \circ V_{SB}/R_2$

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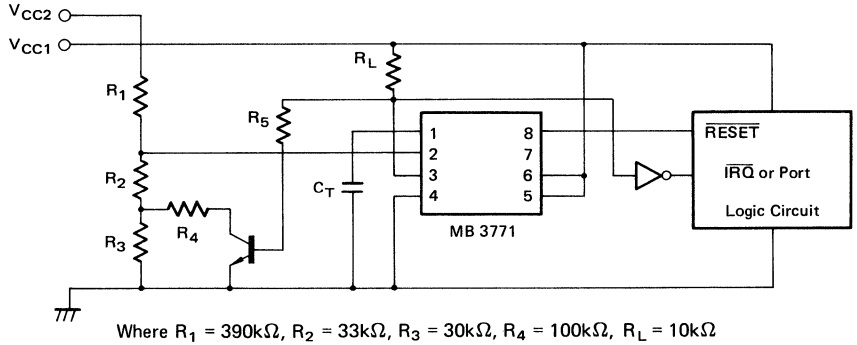
EXAMPLE 5: 5V and 12V Power Supply Monitor
($\overline{\text{RESET}}$ signal is generated by 5V, V_{CC1} = 5V, V_{CC2} = 12V)



Where R_1 = 390kΩ, R_2 = 33kΩ, R_3 = 30kΩ, R_4 = 100kΩ, R_L = 10kΩ

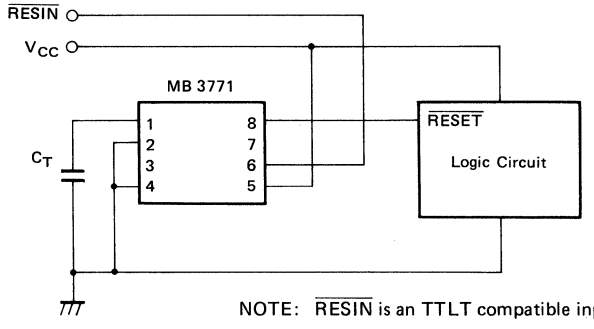
NOTE: 5V is monitored by V_{SA}, and generates $\overline{\text{RESET}}$ signal when V_{SA} detects voltage sagging. 12V is monitored by V_{SC}, and generates its detection signal at OUT_C.

The detection voltage of 12V monitoring and its hysterisis is determined by the following equations.

$$\text{Detection voltage} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} V_{SC} \text{ (8.95 volts in the circuit above)}$$

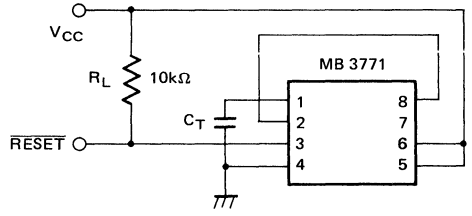
$$\text{Hysterisis width} = \frac{R_1 (R_3 - R_3 \| R_4)}{(R_2 + R_3)(R_2 + R_3 \| R_4)} V_{SC} \text{ (200mA in the circuit above)}$$

EXAMPLE 6: 5V Power Supply Monitor with forced $\overline{\text{RESET}}$ input



NOTE: $\overline{\text{RESIN}}$ is an TTLT compatible input.

EXAMPLE 7: 5V Power Supply Monitor with Non-inverted RESET



NOTE: In this case, Comparator C is used to invert $\overline{RESET}$ signal. OUT_C is an open-collector output. R_L is used as a pull-up resistor.

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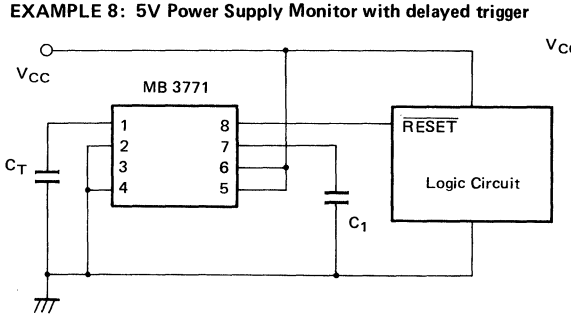
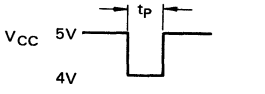
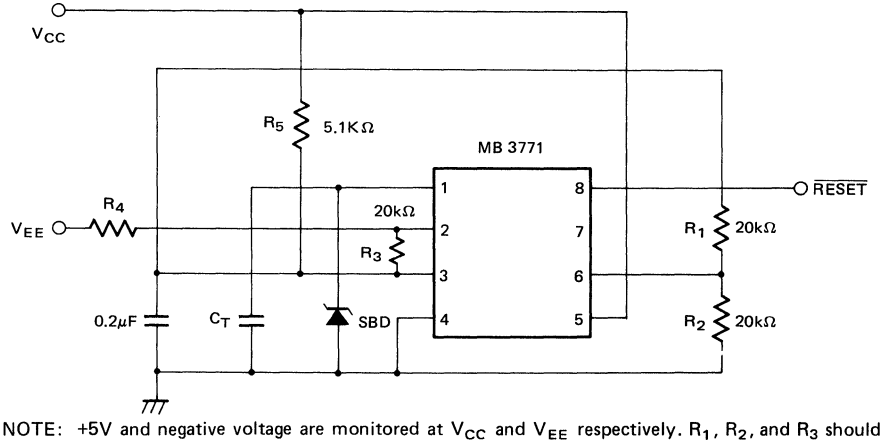
EXAMPLE 8: 5V Power Supply Monitor with delayed trigger





t_P min. = 40μs
when C_1 = 1000pF.

EXAMPLE 9: 5V and arbitrary negative voltage Monitor



NOTE: +5V and negative voltage are monitored at V_{CC} and V_{EE} respectively. R_1, R_2, and R_3 should be the same value. The negative detection voltage is determined by as the following equation.

Detection voltage $V_S = V_{SB} - V_{SB} \cdot R_4/R_3$

Example: When V_{EE} = -5V and R_4 = 91kΩ, V_S = -4.37V.

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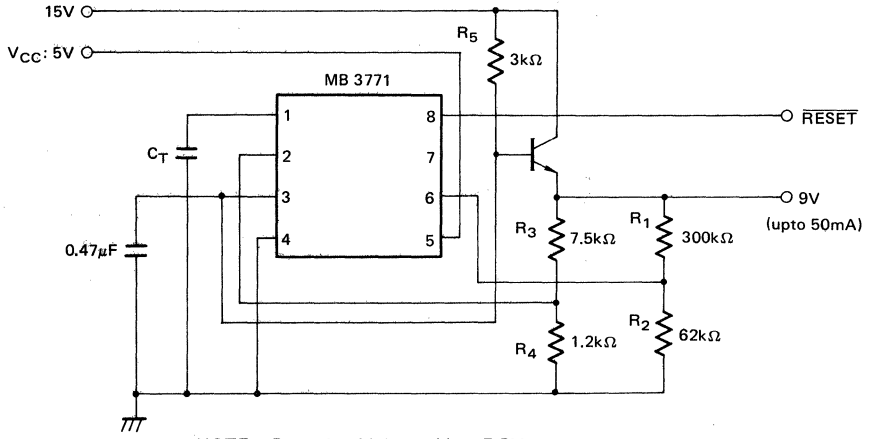
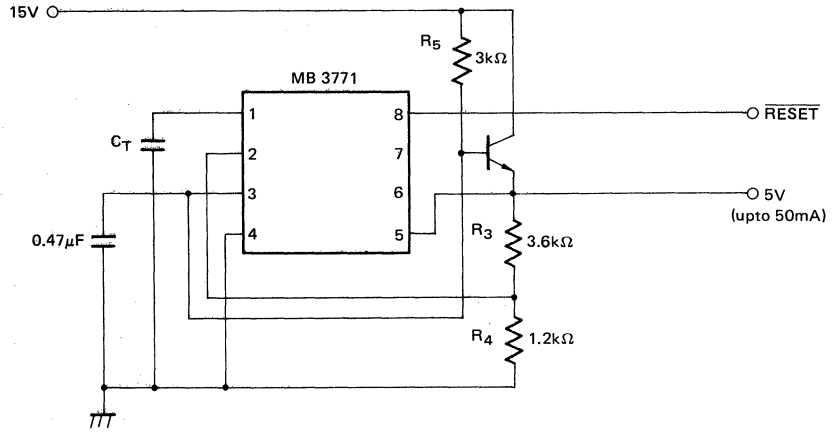
EXAMPLE 10: Reference Voltage Generation and Voltage Sagging Detection

Example 10a: 9V Reference Voltage Generation and 5V/9V Monitoring



NOTE: Detection Voltage: V_S = 7.2V

Example 10b: 5V Reference Voltage Generation and 5V Monitoring



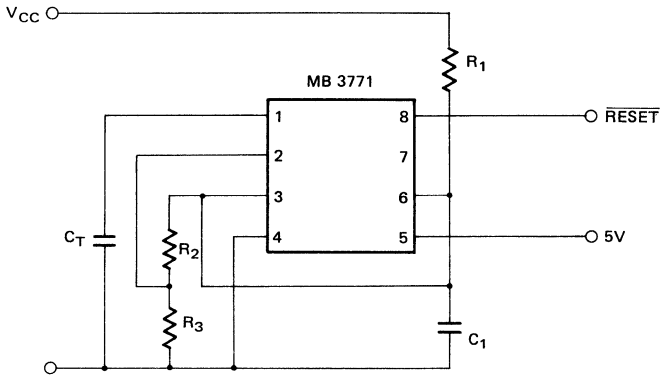
NOTE: Detection Voltage: V_S = 4.2V

NOTE: In the above examples, the output voltage and the detection voltage are determined by the following equations:

Output Voltage: $V_O = (R_3 + R_4) \cdot V_{SC}/R_4$

Detection Voltage: $V_S = (R_1 + R_2) \cdot V_{SB}/R_2$

Example 10c: 5V Reference Voltage Generation and 5V Monitoring

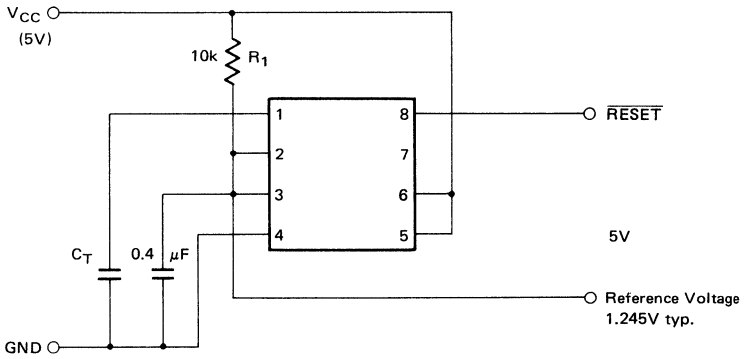


Using the reference table below, the value of R_1 can be determined. Where R_2 is 100kΩ, R_3 is 33kΩ, C_1 is 0.47μF.

Reference Table of R_1, V_{CC}, and the output current

V_{CC} [V]	R_1 [kΩ]	Output Current [mA]
40	11	< 1.6
24	6.2	< 1.4
15	4.7	< 0.6

Example 10d: 1.245V Reference Voltage Generation and 5V Monitoring



NOTE: Resistor R_1 determines Reference current. Using 1.2kΩ as R_1, reference current is about 2mA.

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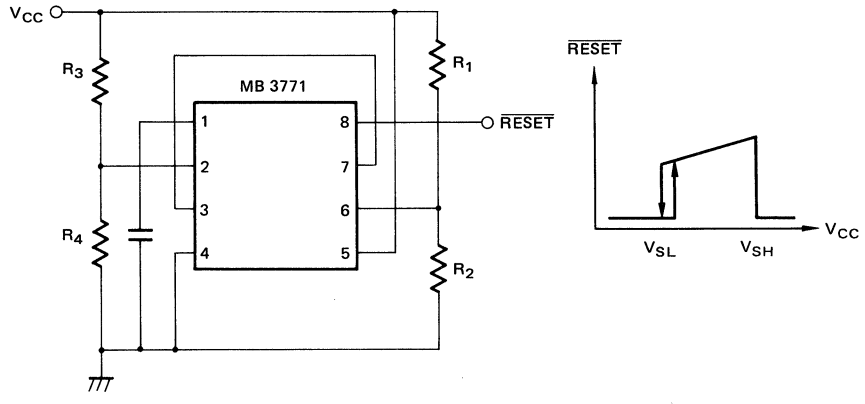
EXAMPLE 11: Low Voltage and Over Voltage Detection



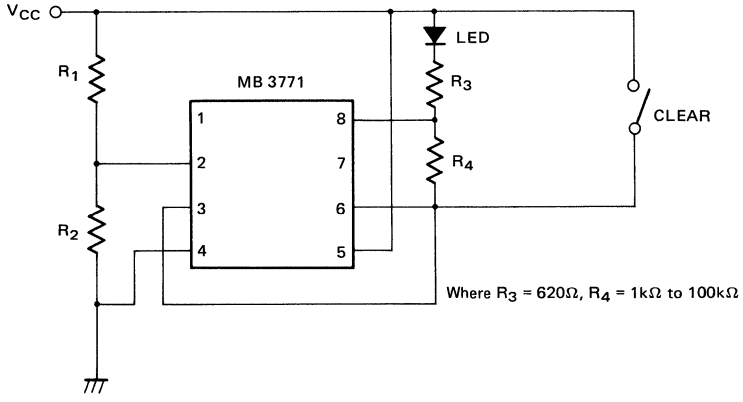
NOTE: V_{SH} has no hysteresis. When over voltage is detected, $\overline{RESET}$ is held in the constant time as well as when low voltage is detected.

$V_{SL} = (R_1 + R_2) \cdot V_{SB}/R_2$

$V_{SH} = (R_3 + R_4) \cdot V_{SC}/R_4$

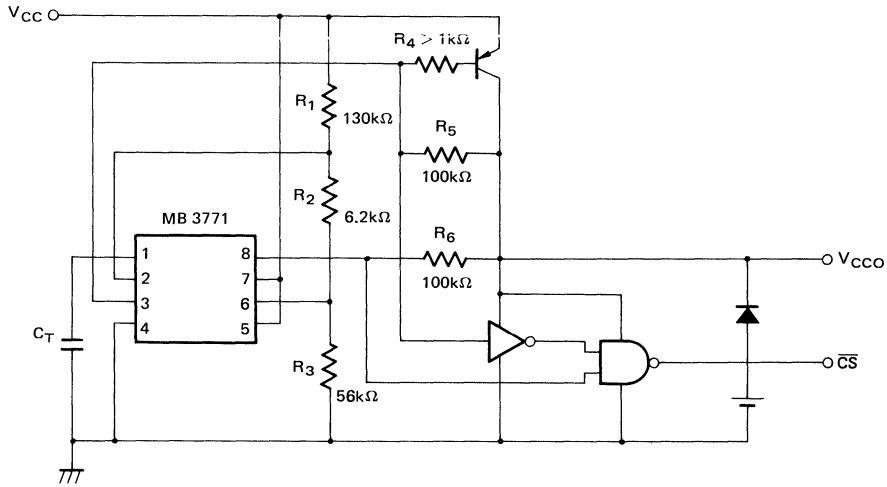
EXAMPLE 12: Detection of Abnormal State of Power Supply System

This example circuit detects abnormal low/over voltage of power supply voltage and is indicated by LED indicator. LED is reset by the CLEAR key.



NOTE: The detection levels of low/over voltages are determined by V_{SA}, and R_1 and R_2 respectively.

EXAMPLE 13: Back-up power supply system (V_{CC} = 5V)



NOTE: Use CMOS Logic and connect V_{DD} of CMOS logic with V_{CCO}.

The back-up battery works after $\overline{CS}$ goes high as $V_2 < V_1$.

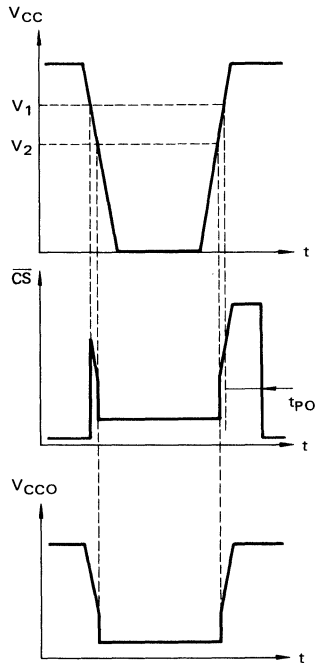
During t_{PO}, memory access is prohibited.

CS's threshold voltage V_1 is determined by the following equation:

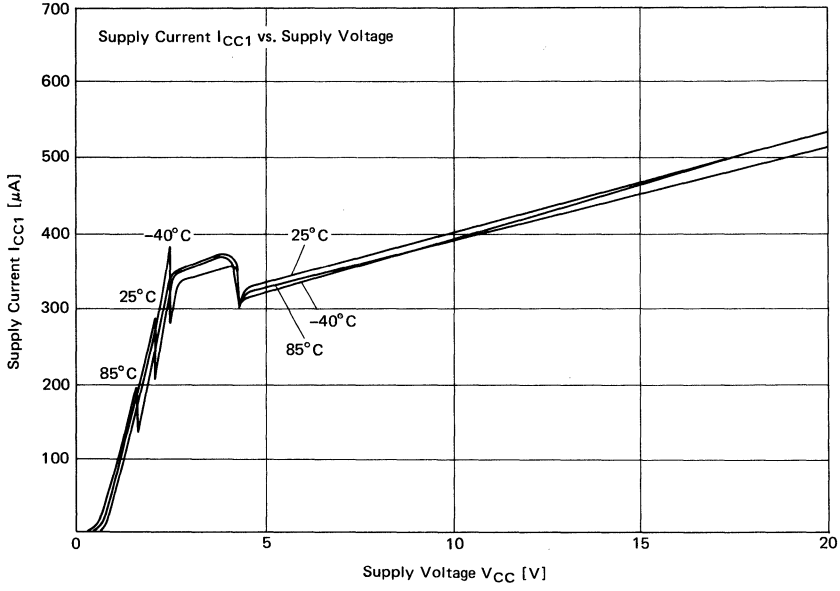
$$V_1 = (R_1 + R_2 + R_3)\ V_{SB}/R_3$$

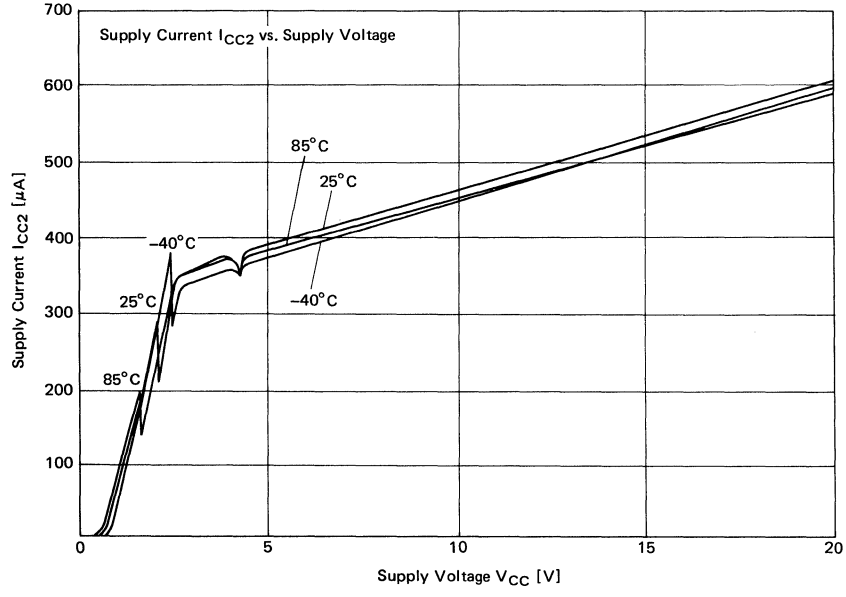
The voltage to change V_2 is provided as the following equation:

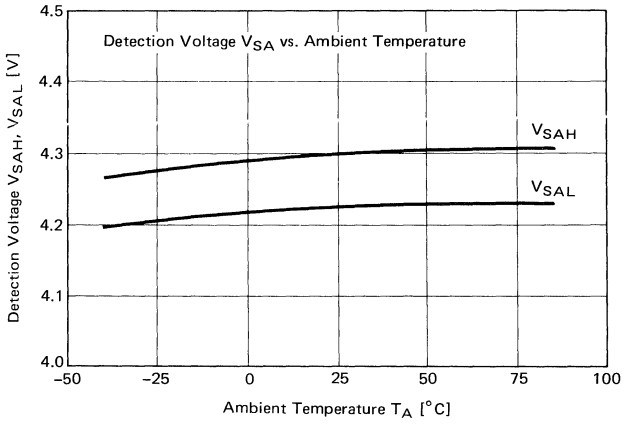
$$V_2 = (R_1 + R_2 + R_3) \cdot V_{SC}/(R_2 + R_3)$$

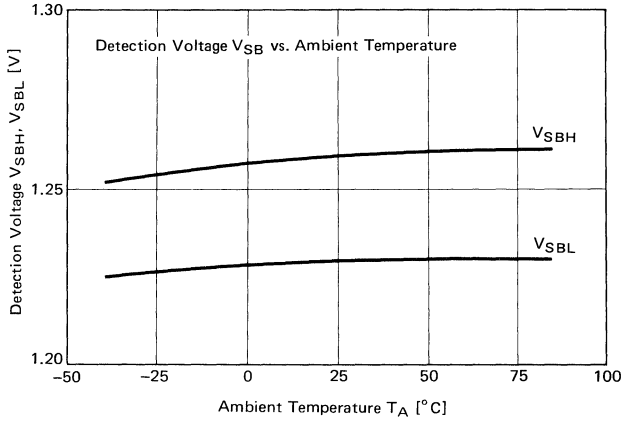


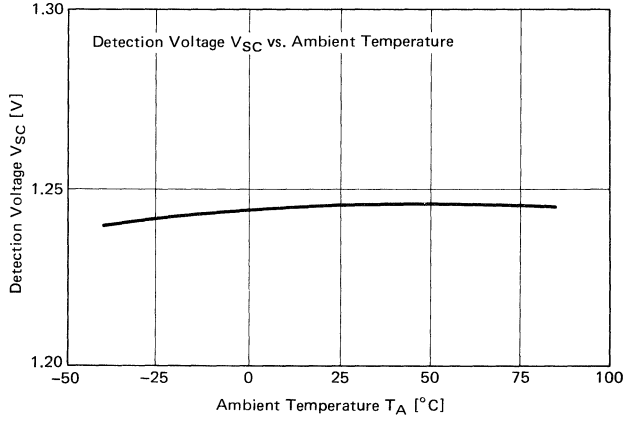
4


Supply Current I_{CC1} vs. Supply Voltage
Supply Current I_{CC1} [μA]
700
600
500
400
300
200
100
0
5
10
15
20
Supply Voltage V_{CC} [V]
-40°C
25°C
85°C
25°C
-40°C
85°C


Supply Current I_{CC2} vs. Supply Voltage
Supply Current I_{CC2} [μA]
700
600
500
400
300
200
100
0
5
10
15
20
Supply Voltage V_{CC} [V]
85°C
25°C
-40°C
-40°C
25°C
85°C

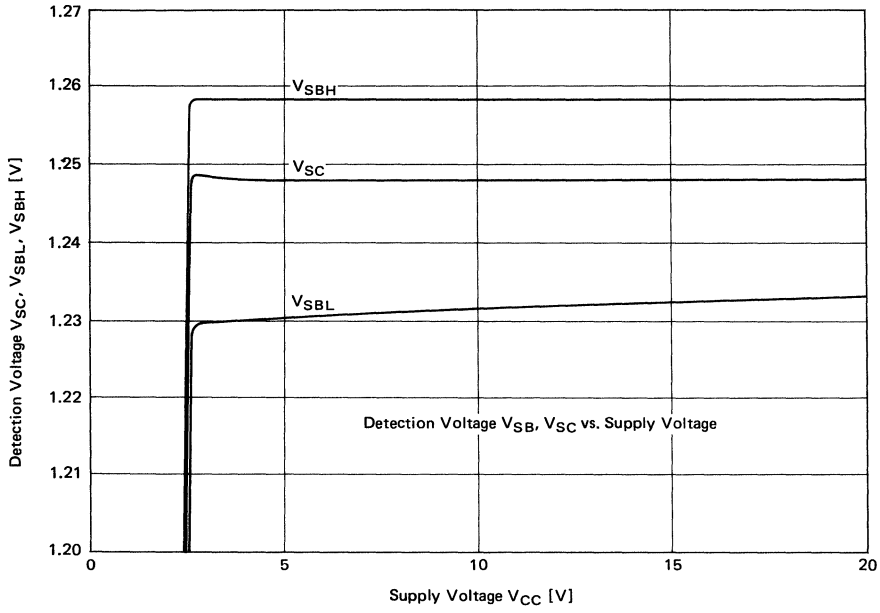

Detection Voltage V_{SA} vs. Ambient Temperature
Detection Voltage V_{SAH}, V_{SAL} [V]
4.5
4.4
4.3
4.2
4.1
4.0
V_{SAH}
V_{SAL}
–50
–25
0
25
50
75
100
Ambient Temperature T_A [°C]

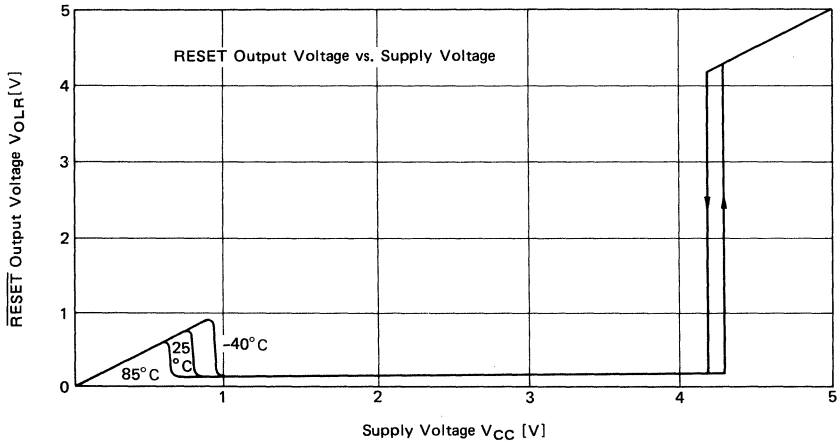

Detection Voltage V_{SB} vs. Ambient Temperature
Detection Voltage V_{SBH}, V_{SBL} [V]
1.30
1.25
1.20
V_{SBH}
V_{SBL}
–50
–25
0
25
50
75
100
Ambient Temperature T_A [°C]

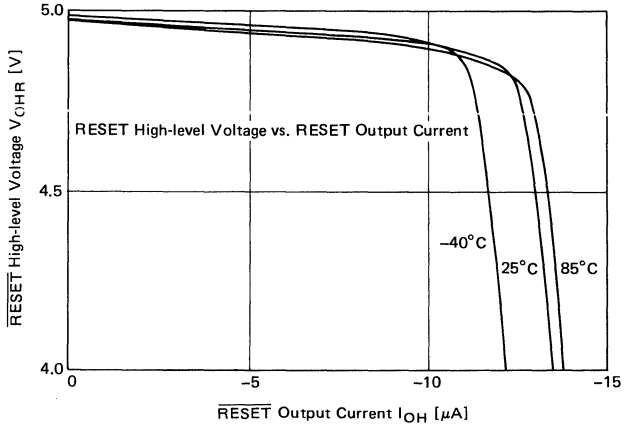

Detection Voltage V_{SC} vs. Ambient Temperature
Detection Voltage V_{SC} [V]
1.30
1.25
1.20
–50
–25
0
25
50
75
100
Ambient Temperature T_A [°C]

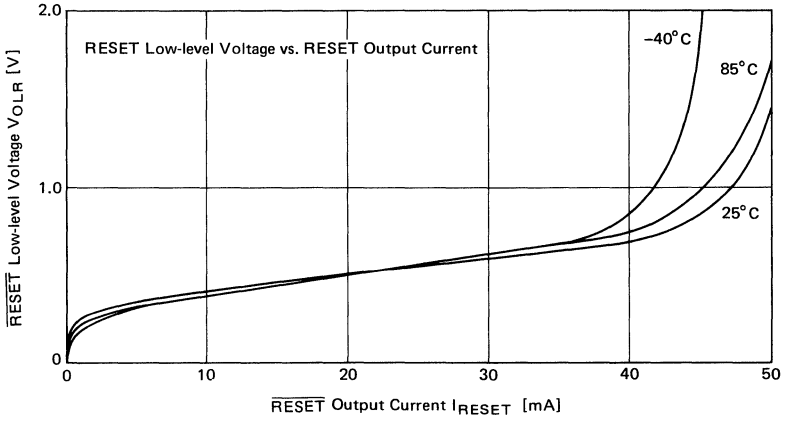
4

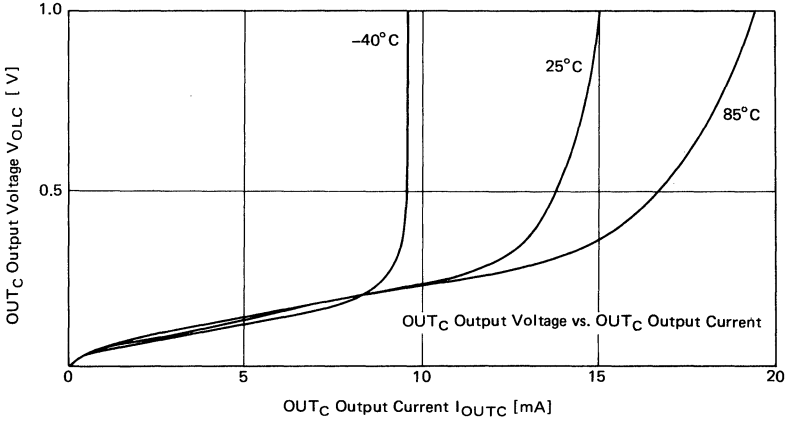
4


1.27
1.26
1.25
1.24
1.23
1.22
1.21
1.20
0
5
10
15
20
V_{SBH}
V_{SC}
V_{SBL}
Detection Voltage V_{SB}, V_{SC} vs. Supply Voltage
Detection Voltage V_{SC}, V_{SBL}, V_{SBH} [V]
Supply Voltage V_{CC} [V]


5
4
3
2
1
0
1
2
3
4
5
RESET Output Voltage vs. Supply Voltage
$\overline{RESET}$ Output Voltage V_{OLR}[V]
85°C
25 °C
-40°C
Supply Voltage V_{CC} [V]

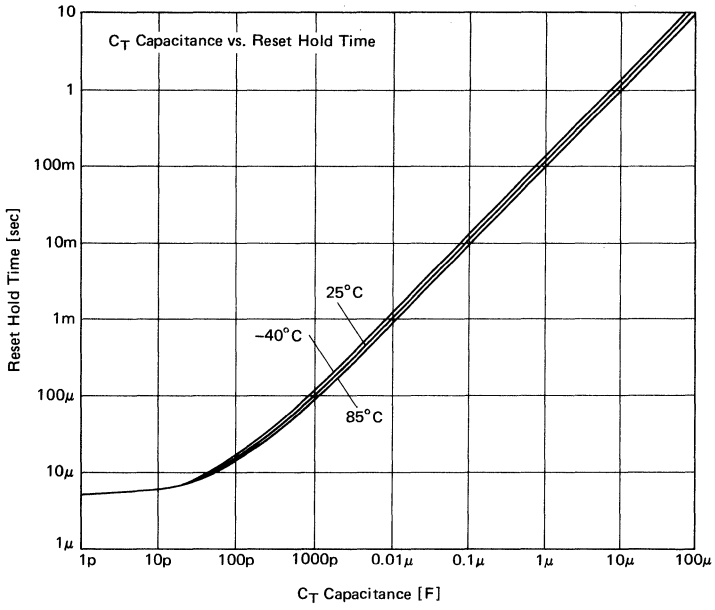

RESET High-level Voltage vs. RESET Output Current
RESET High-level Voltage V_{OHR} [V]
5.0
4.5
4.0
0
-5
-10
-15
-40°C
25°C
85°C
RESET Output Current I_{OH} [μA]

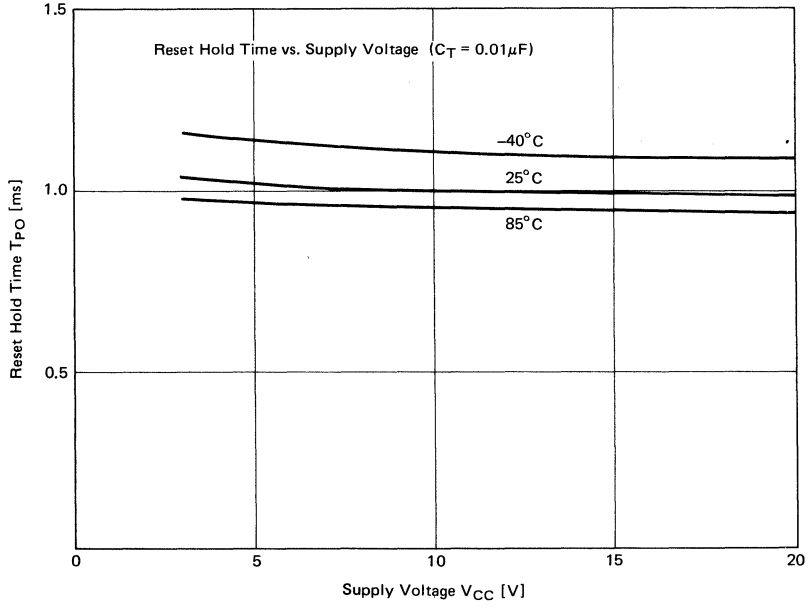

RESET Low-level Voltage vs. RESET Output Current
RESET Low-level Voltage V_{OLR} [V]
2.0
1.0
0
10
20
30
40
50
-40°C
85°C
25°C
RESET Output Current I_{RESET} [mA]


OUT_C Output Voltage vs. OUT_C Output Current
OUT_C Output Voltage V_{OLC} [V]
1.0
0.5
0
5
10
15
20
-40°C
25°C
85°C
OUT_C Output Current I_{OUTC} [mA]

4

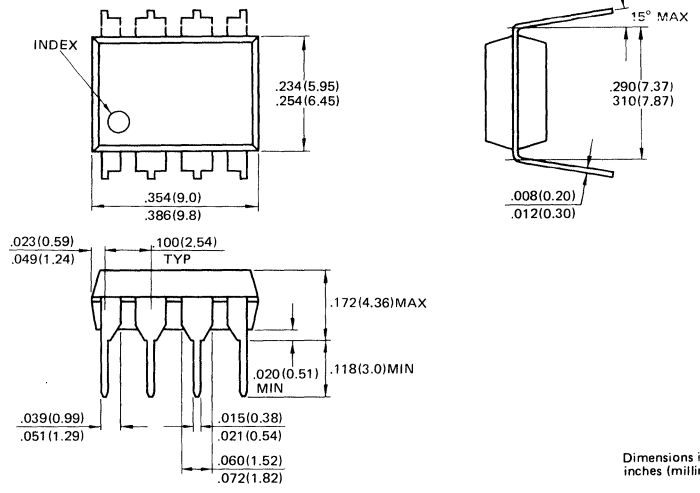
4


C_T Capacitance vs. Reset Hold Time
Reset Hold Time [sec]
10
1
100m
10m
1m
100μ
10μ
1μ
25°C
−40°C
85°C
1p
10p
100p
1000p
0.01μ
0.1μ
1μ
10μ
100μ
C_T Capacitance [F]


Reset Hold Time vs. Supply Voltage (C_T = 0.01μF)
Reset Hold Time T_{PO} [ms]
1.5
1.0
0.5
−40°C
25°C
85°C
0
5
10
15
20
Supply Voltage V_{CC} [V]

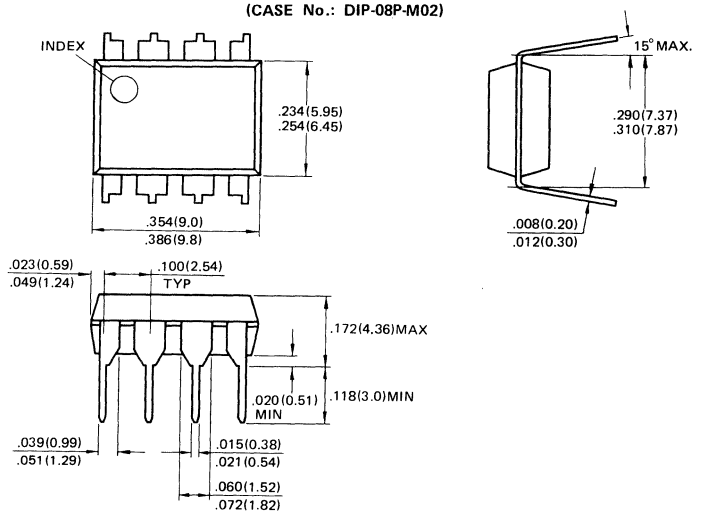
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



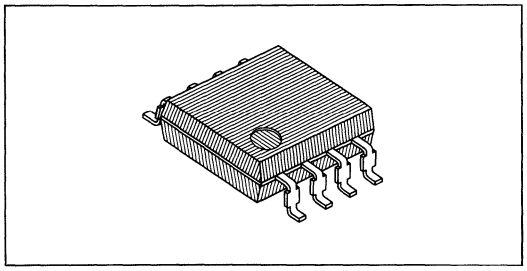
Dimensions in
inches (millimeters)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M02)



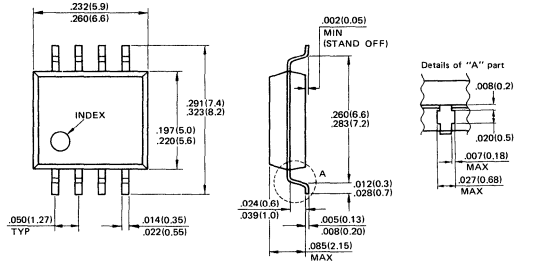
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS



4

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches
(millimeters)

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FUJITSU

POWER SUPPLY MONITOR WITH WATCH-DOG TIMER

MB 3773

October 1986
Edition 1.0

POWER SUPPLY MONITOR WITH WATCH-DOG TIMER

The Fujitsu MB 3773 is designed to monitor the voltage level of a power supply (+5 V or an arbitrary voltage) in a microprocessor circuit, memory board in a large-size computer, for example. The MB 3773 aiso contains a watch-dog timer function to detect uncontrol. Table status of processor and reset system/processor.

If the circuit's power supply deviates more than a specified amount, then the MB 3773 generates a reset signal to the microprocessor. Thus, the computer data is protected from accidental erasure.

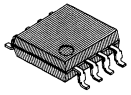
When the MB 3773 does not receive the clock pulse from the processor in the specified period, the MB 3773 generates a reset signal to the mciroprocessor.

Using the MB3773 requires few external components. To monitor only a +5 volt supply, the MB 3773 requires the connection of one external capacitor.

The MB 3773 is available in an 8-pin Dual In-Line package space saving Flat Package, or a Single In-Line Package.

- Precision voltage detection (V_S = 4.2 V ±2.5%)
- Threshold level with hysterisis
- Low voltage output for eset signal (V_{CC} = 0.8 V typ.)
- Precision reference voltage output (V_{REF} = 1.245 V ±1.5%)
- External clock monitor and reset signal generator
- Negative-edge input watch-dog timer
- Minimal number of external components (on capacitor min.)
- Available in a variety of packages
  - 8-pin Dual In-Line Package
  - 8-pin Flat Package
  - 8-pin Single In-Line Package

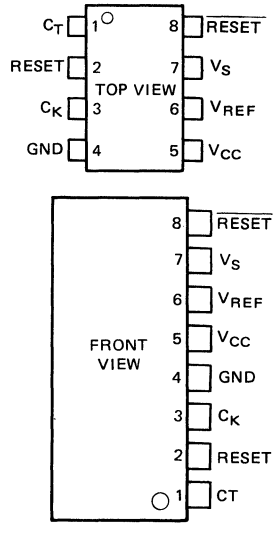
PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PLASTIC PACKAGE
SIP-08P-M03

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

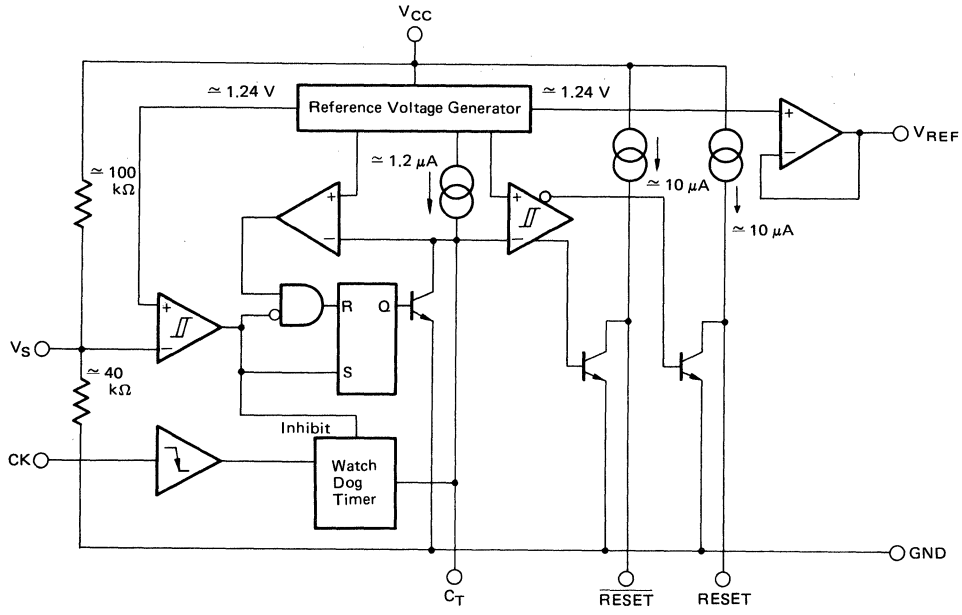
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +18	V
Input Voltage	V_S	-0.3 to +18	V
Power Dissipation ($T_A \leq 85°C$)	P_D	200	mW
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

Fig. 1 – MB 3773 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+ 3.5 to +16	V
Operating Ambient Temperature	T_A	-40 to +85	°C

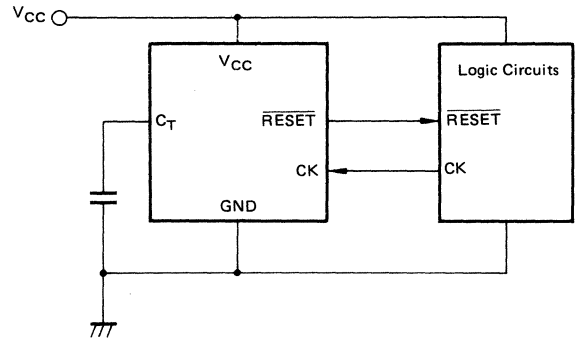
ELECTORICAL CHARACTERISTICS

(V_{CC} = 5 V, T_A = 25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Supply Current		I_{CC}		600	900	μA
High-level Output Voltage	V_S Open. $I_{\overline{RESET}}$ = -5 μA	V_{ON1}	4.5	4.9		V
	V_S = 0 V. I_{RESET} = -5 μA	V_{ON2}	4.5	4.9		
Sagging Detection Voltage	V_{CC} ↘ Falling edge	V_{SAL}	4.10	4.20	4.30	V
	V_{CC} ↗ Rising edge	V_{SAH}	4.20	4.30	4.40	
Reference Voltage		V_{REF}	1.227	1.245	1.263	V
CK Threshold Voltage		V_{CK}		1.25		
CK Pulse Width		T_{CK}	3	—		μs
Input Sink Current	V_S = 0V. $V_{\overline{RESET}}$ = 1.0 V	I_{OL1}	20	45		mA
	V_S Open. V_{RESET} = 1.0 V	I_{OL2}	20	45		
Minimum Supply Voltage for $\overline{RESET}$ output	$V_{\overline{RESET}}$ = 0.4 V $I_{\overline{RESET}}$ = 0.2 mA	V_{CCL}		0.8	1.2	V
Output Saturation Voltage	V_S = 0 V. $I_{\overline{RESET}}$ = 3 mA	V_{OL1}		0.2	0.4	V
	V_S = 0 V. $I_{\overline{RESET}}$ = 10 mA	V_{OL2}		0.3	0.5	
	V_S Open. I_{RESET} = 3 mA	V_{OL3}		0.2	0.4	
	V_S Open. I_{RESET} = 10 mA	V_{OL4}		0.3	0.5	

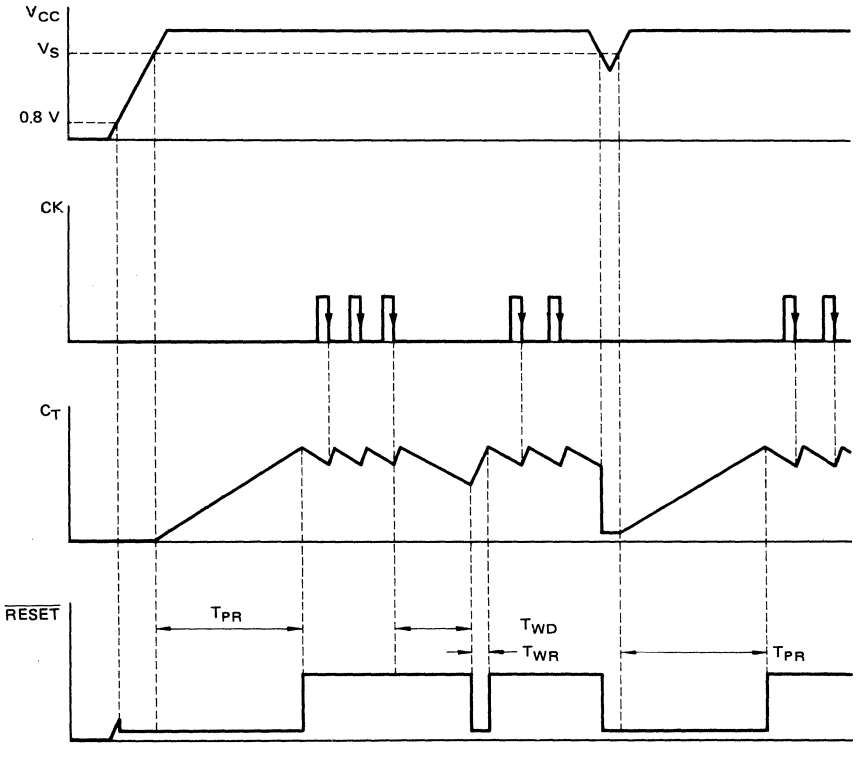
4

Fig. 2 – MB 3773 BASIC OPERATION



C_T = 0.1 μF

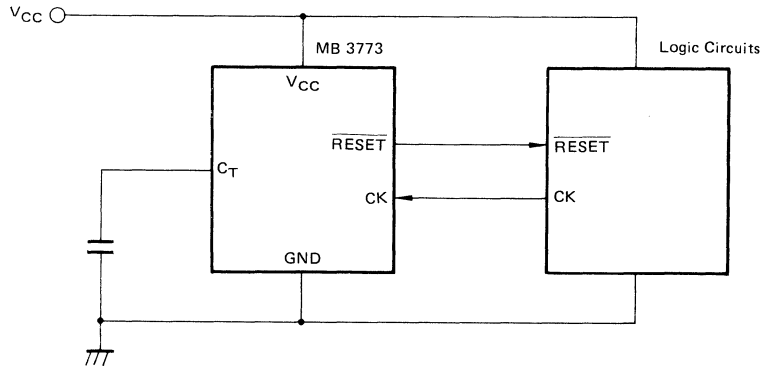
$T_{PR} \fallingdotseq 1000 \cdot C_T$ (μF) (100 ms)
$T_{WD} \fallingdotseq 100 \cdot C_T$ (μF) (10 ms)
$T_{WR} \fallingdotseq 20 \cdot C_T$ (μF) (2 ms)



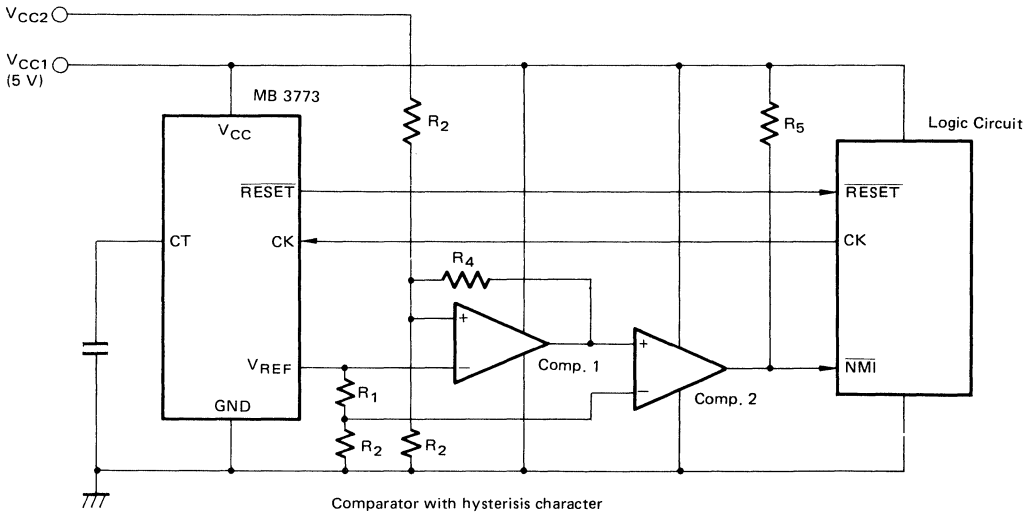
4

Fig. 3 – MB 3773 APPLICATION EXAMPLE

- Sagging Monitor and Watch-Dog Timer



- Monitor for other power system



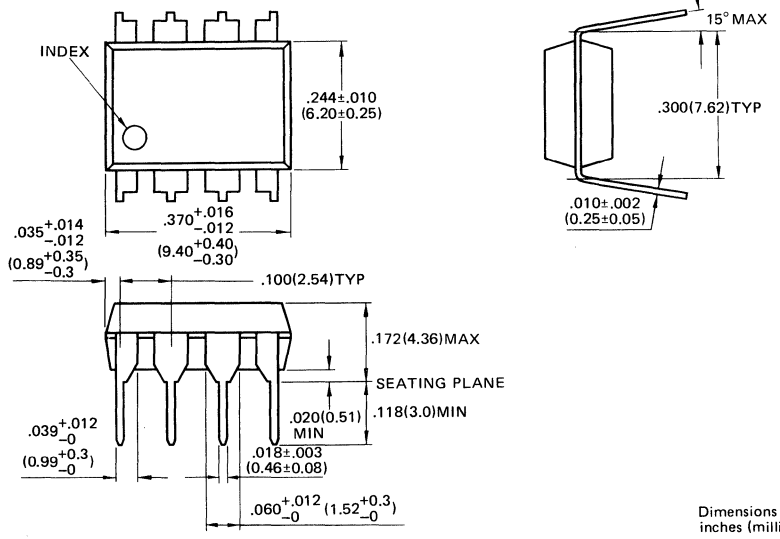
Comparator with hysterisis character

Comp. 1, Comp. 2: MB 4204
MB 47393

NOTE: When V_{CC2} in lower then the specified voltage, NMI low.
If over-voltage detection of V_{CC2}, Swap the inputs of comparator 2.

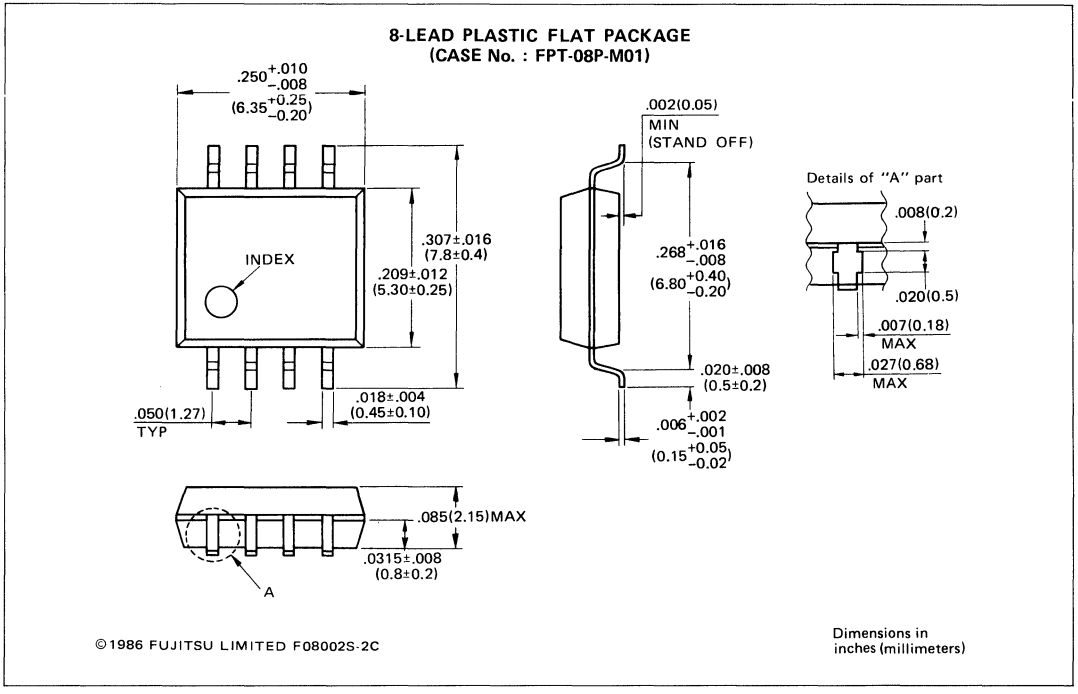
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



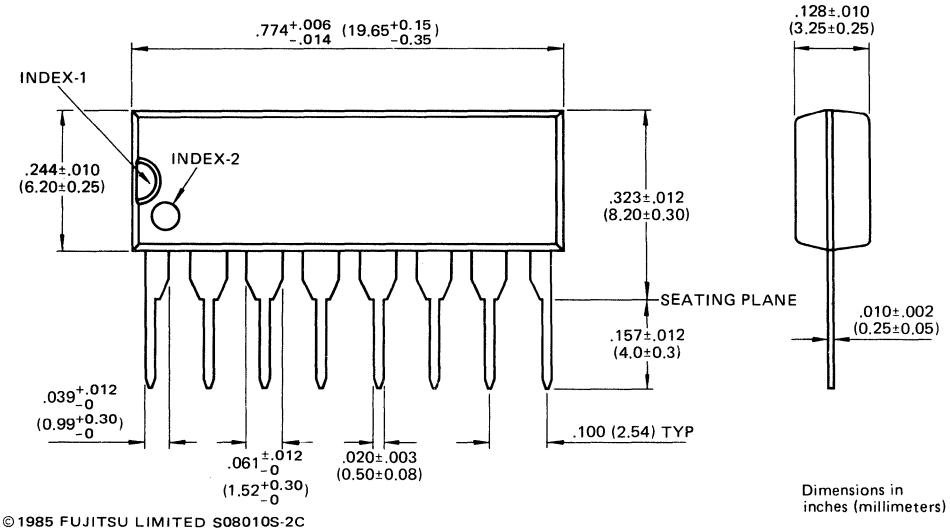
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS



PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M03)



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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Lyoner Straße 44-48 D-6000 Frankfurt 71, F.R. Germany
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Section 5

Motor Drivers

Fujitsu Part No.	Description	Features	Equiv. Prod.	Power Supply (V)	Package	No. of Pins
MB3763	Motor Driver	Io = 180mA, 330mA with heatsink	—	+4 ~ +18	Plastic DIP Plastic Flatpak SIP	8 8 8
MB3854	Motor Driver	Io = 30mA	—	+2.3 ~ +10	Plastic DIP Plastic Flatpak	8 8

FUJITSU

BIDIRECTIONAL MOTOR DRIVER

MB3763

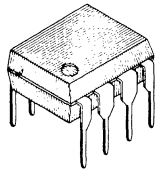
October 1987
Edition 1.0

BIDIRECTIONAL MOTOR DRIVER

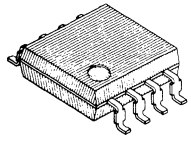
Fujitsu's MB3763 Motor Driver with forward/reverse control capability, is used in applications such as the front-loading mechanism in video tape, or the auto-reverse tape deck, driven by a TTL signal. The MB3763 has 300 mA drive units and braking capability with TTL control.

- Motor Drive Current : 300 mA maximum in a SIP Package
  : 150 mA maximum in a DIP/FPT Package
- Wide Power Supply Voltage Range : 4 V to 18 V
- TTL-control capability
- Standby capability when input is off.
- Brake capability at motor stop mode.
- Built-in diode for surge absorption
- Package : 8-pin plastic SIP package (Suffix: -PS)
  8-pin plastic DIP package (Suffix: -P)
  8-pin plastic FPT package (Suffix: -PF)

PLASTIC PACKAGE
SIP-08P-M01



PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

5

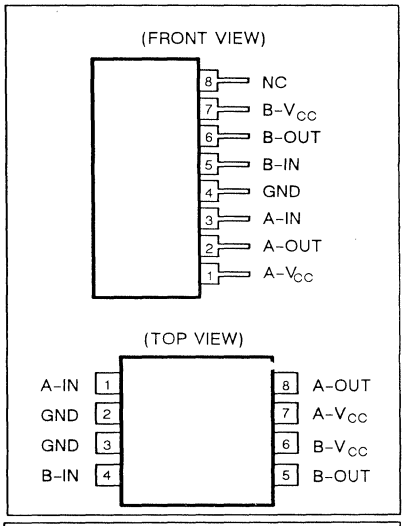
ABSOLUTE MAXIMUM RATINGS[1] (see NOTES)

Parameter	Symbol	Value		Unit
		DIP/FPT (Plastic)	SIP (Plastic)	
Power Supply Voltage	V_{CC}	20	20	V
Output Current	I_O	180 (330[2])	330	mA
Maximum Output Current	I_{OMAX}[4]	1.2	1.2	A
Power Dissipation	P_D	560[3]	1000	mW
Operating Temperature	T_C	-20 to +75	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	-55 to +125	°C

NOTES:

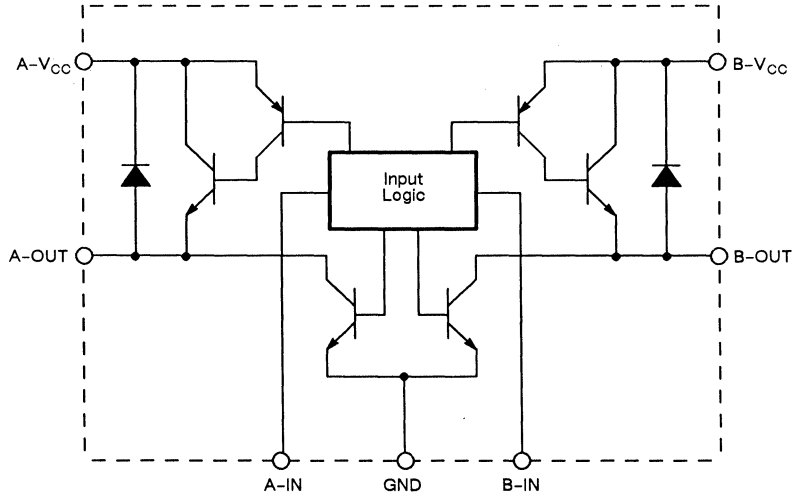
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. $t_{ON} \leq 1$ sec, Duty = 50%
3. $T_A \leq 60°C$
4. $t \leq 5$ ms

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Figure 1. MB3763 Block Diagram



5

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		DIP/FPT (Plastic)	SIP (Plastic)	
Power Supply Voltage	V_{CC}	4 to 18	4 to 18	V
Output Current	I_O	0 to 150 (300 *1)	0 to 300	mA
Input High Voltage	V_{IH} *2	2.4 to V_{CC} + 0.3	2.4 to V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	0 to 0.4	0 to 0.4	V

NOTE: *1 $t_{ON} \leq 1$ sec, Duty = 50%

*2 When $V_{IH} \geq V_{CC}$, $I_{IH} \leq V_{CC} \times 0.2$ mA

ELECTRICAL CHARACTERISTICS FOR DIP AND FPT PACKAGE (PLASTIC) (V_{CC} = 12 V, I_O = 150 mA, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Standby Supply Current	I_{CC0}	V_{CC} = 18 V, V_{IA} = V_{IB} = 0 V	—	—	0.1	mA
Power Supply Current	I_{CC1}	I_O = 0 mA	—	10	20	mA
	I_{CC2}	I_O = 150 mA	—	10	—	mA
	I_{CC3}	I_O = 0 mA, V_{IA} = V_{IB} = 2.4 V	—	15	—	mA
Output High Voltage	V_{OH}	—	11.0	11.2	—	V
Output Low Voltage	V_{OL}	—	—	0.1	0.2	V
Output Saturation Voltage	V_{SAT}	—	—	0.9	1.2	V
Input Current	I_{IH}	V_{IN} = 2.4 V	—	250	400	μA
Input Switching Prohibition Time	T_{OFF}	—	10	—	—	μs

5

ELECTRICAL CHARACTERISTICS FOR SIP PACKAGE (PLASTIC) (V_{CC} = 12 V, I_O = 300 mA, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Standby Supply Current	I_{CC0}	V_{CC} = 18 V, V_{IA} = V_{IB} = 0 V	—	—	0.1	mA
Power Supply Current	I_{CC1}	I_O = 0 mA	—	10	20	mA
	I_{CC2}	I_O = 300 mA	—	15	—	mA
	I_{CC3}	I_O = 0 mA, V_{IA} = V_{IB} = 2.4 V	—	15	—	mA
Output High Voltage	V_{OH}	—	10.8	11.1	—	V
Output Low Voltage	V_{OL}	—	—	0.2	0.5	V
Output Saturation Voltage	V_{SAT}	—	—	1.1	1.7	V
Input Current	I_{IH}	V_{IN} = 2.4 V	—	250	400	μA
Input Switching Prohibition Time	T_{OFF}	—	10	—	—	μs

FUNCTIONAL DESCRIPTIONS

FORWARD/REVERSE MODE (MODE B & C)

In this mode, the transistor pairs Q2-Q3 and Q1-Q4 work alternatively, changing the output current direction.

When the mode B is selected, Q2 and Q3 are active and Q1 and Q4 are inactive. Therefore A-OUT is at low level and B-OUT is at high level, with the current flowing from B-OUT to A-OUT through the motor. On the other hand, when the mode C is selected, the current flows in the reverse direction.

BRAKE/STOP MODE (MODE A)

When the mode A is selected, Q1 and Q3 are inactive and Q2 and Q4 are active. A-OUT and B-OUT are stuck at low-level; terminals of motor are shorted and the motor is forced to stop.

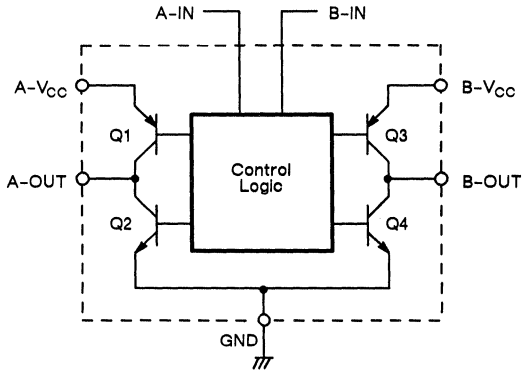
STANDBY MODE (MODE D)

In this mode, all transistors are inactive and the current through the motor does not flow. When the power supply voltage is applied to A-V_{CC} and B-V_{CC}, the supply current is still less than or equal to 0.1 mA.

CONTROL MODE

5

CONTROL BLOCK DIAGRAM

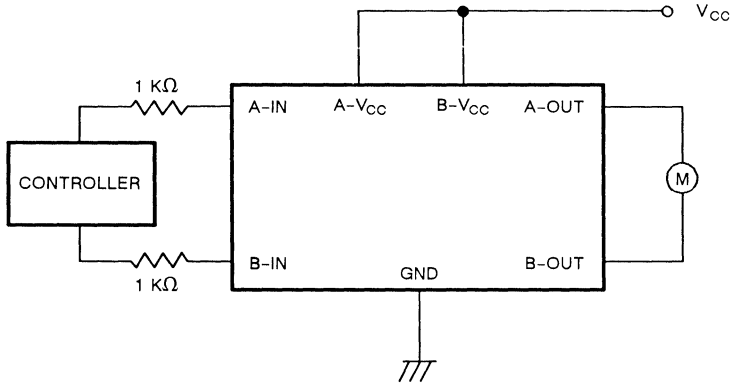


Mode	Input mode		Output mode		Operation
	A-IN	B-IN	A-OUT	B-OUT	
A	1	1	L	L	Short (Brake)
B	1	0	L	H	Forward
C	0	1	H	L	Reverse
D	0	0	-	-	Open (Standby)

NOTES: 1: $\geq$ 2.4 V
0: $\leq$ 0.4 V

TYPICAL APPLICATION

Figure 2. Typical Application Example



NOTE: In the case the control voltage is input when the power supply voltage is not applied because of the time lag between those two voltages, excess current flows into IC from the input terminals. In this case, please connect a resistor ($\geq$ 1K Ω) serially to input pin in order to prevent excess current flow.

5

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Output Current vs Power Supply Current

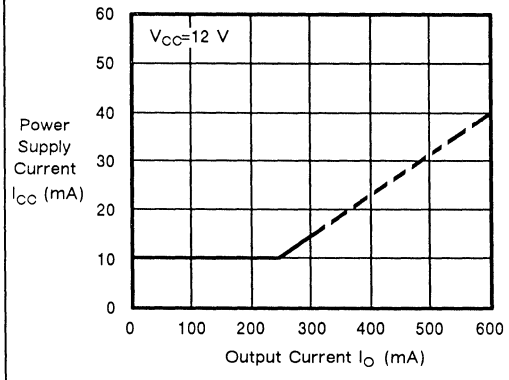
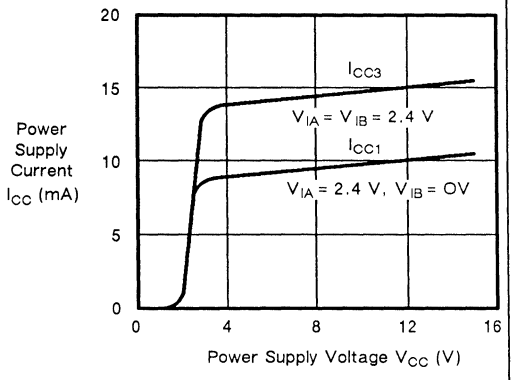


Fig. 4 – Power Supply Voltage vs Power Supply Current



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 5 – Output Current vs Output Voltage

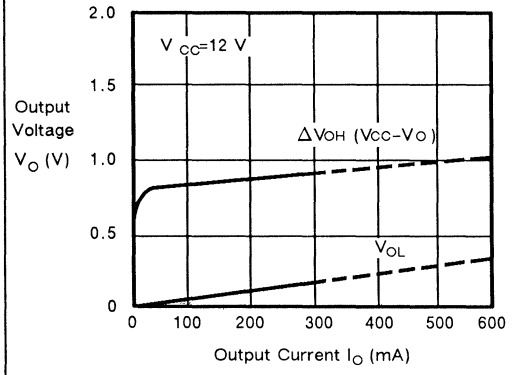
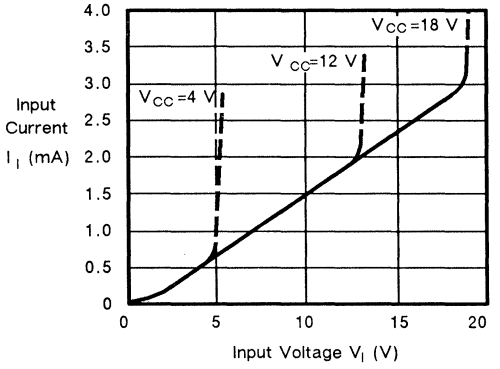
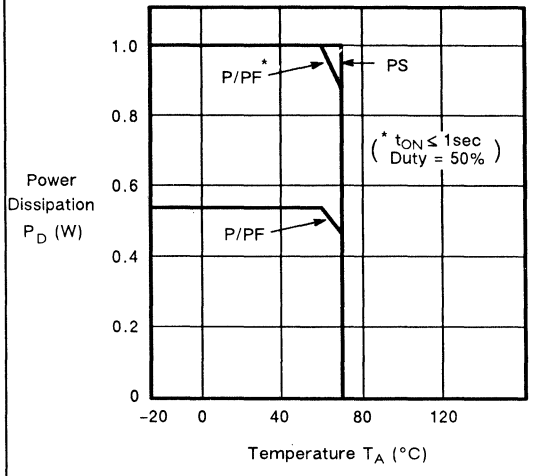


Fig. 6 – Input Voltage vs Input Current



5

Fig. 7 – Temperature vs Power Dissipation



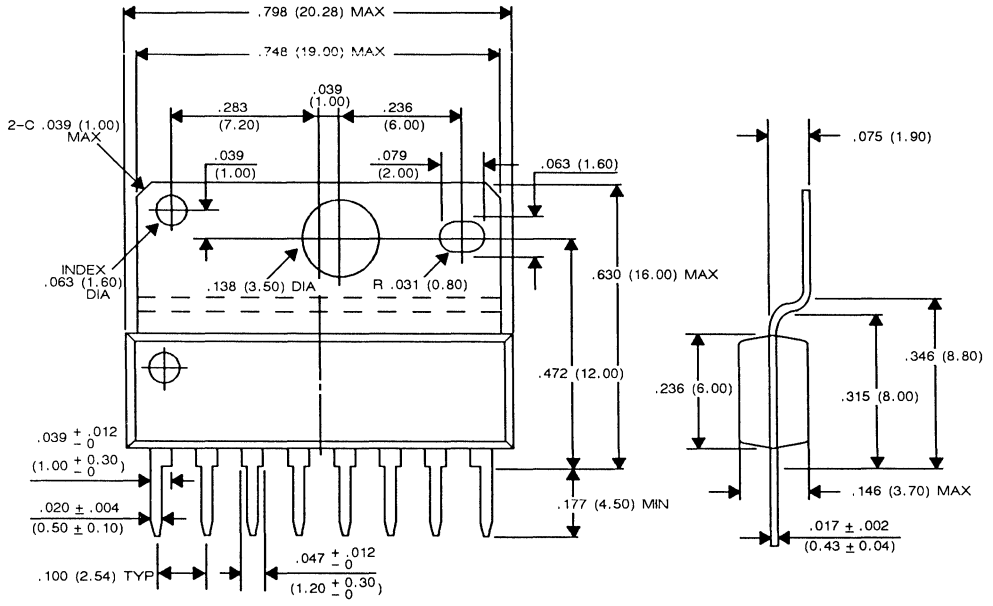
PF'S value is measured on the ceramic board (3.0 cm x 3.0 cm x 0.05 cm)

Notes P : Plastic DIP
PF : Plastic Flat Package
PS : Plastic SIP

Maximum power dissipation must be kept.

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-08P-M01)



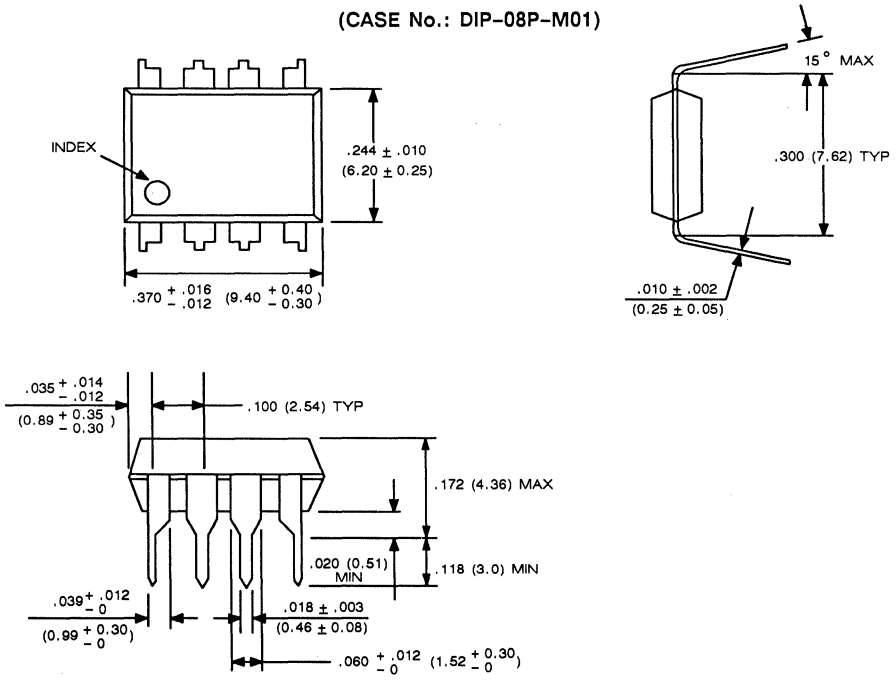
Dimensions in inches (millimeters)

S08004S-6C

5

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



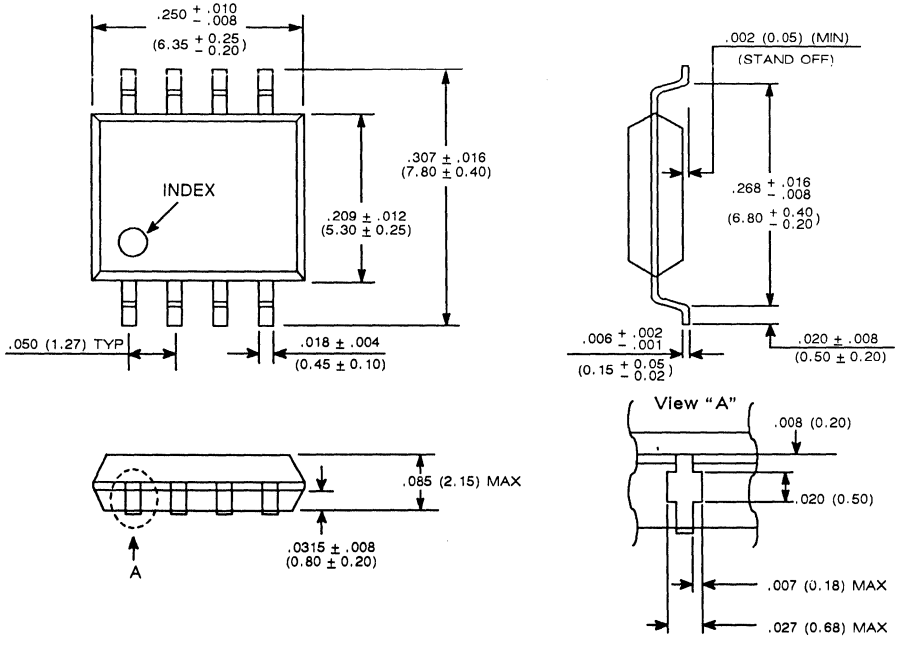
Dimensions in
inches (millimeters)

D08006S-2C

5

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
inches (millimeters)

F08002S-2C

FUJITSU

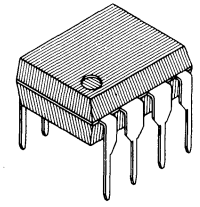
BI-DIRECTIONAL MOTOR DRIVER

MB3854

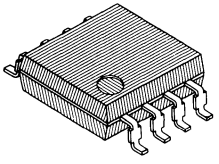
April 1988
Edition 1.0

BI-DIRECTIONAL MOTOR DRIVER

The Fujitsu MB3854 is a low voltage motor driver with forward/reverse control capability for motor in auto focus, film advancing mechanism, in camera, in front loading mechanism in CD player, etc., which is driven by TTL-level signal.
The MB3854 has 300mA drive units and brake capability for stop with TTL control input.



PLASTIC PACKAGE
DIP-08P-M01

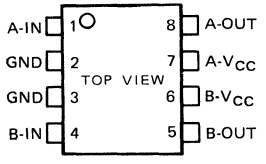


PLASTIC PACKAGE
FPT-08P-M01

- Motor drive current: 300mA max.
- Low power supply voltage operation: 2.3V to 10V
- TTL-control capability
- Standby capability when input is off
- Brake capability at motor stop mode
- Built-in diode for surge absorption
- Plastic 8-pin Dual-In-Line Package (Suffix: -P)
- Plastic 8-pin Flat Package (Suffix: -PF)

5

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

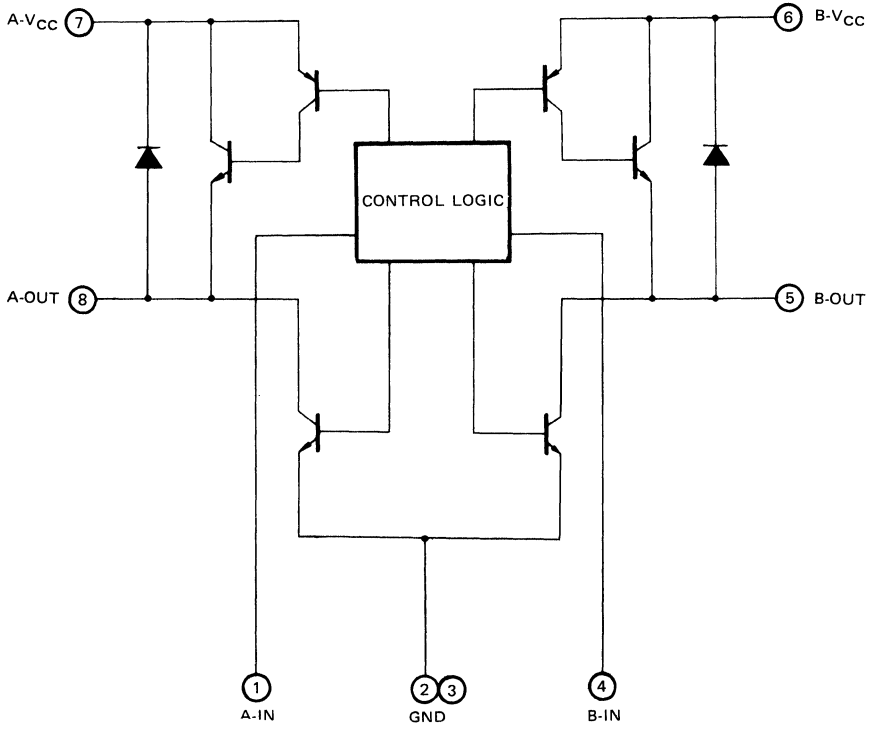
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	12	V
Output Current	I_O	330 (550*1)	mA
Maximum Output Current	I_{OMAX} *2	0.8	A
Power Dissipation	P_D	560*3	mW
Operating Temperature	T_A	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +125	°C

*1 $t_{ON} \leq 1$ sec, Duty = 50%
*2 $t \leq 5$ms
*3 $T_A \leq 60°C$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB3854 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTIONS

According to the control mode, output transistors in Fig. 2 work as follows.

FORWARD/REVERSE MODE

According to the control B/C mode, the transistor pairs Q2-Q3 and Q1-Q4 work alternatively and supply current to motor is changed.

When the mode B is selected, Q2 and Q3 are active. A-OUT is at low level and B-OUT is at high level, current flows from B-OUT to A-OUT through the motor.

On the other hand, when the mode C is selected, the current flows in reverse direction.

BRAKE MODE

When control mode A is selected, Q1 and Q3 are inactive, Q2 and Q4 are active. A-OUT and B-OUT are clamped at low level, terminals of the motor are shorted and the motor is forced to stop.

STAND-BY MODE

When stand-by mode is selected, all transistors are inactive and the current through motor does not flow. In this case, the supply current is less than 100μA.

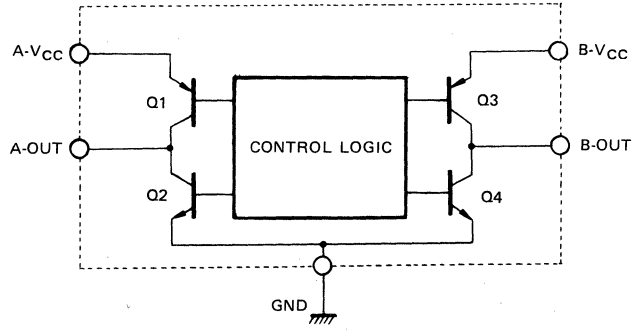
5

Table 1 – CONTROL MODE TABLE

Mode	Input mode		Output level		Operation mode
	A-IN	B-IN	A-OUT	B-OUT	
A	1	1	L	L	Short (Brake)
B	1	0	L	H	Forward
C	0	1	H	L	Reverse
D	0	0	–	–	Open (Stand-by)

Note:
Input mode
1: $\geq$ 2.1V
2: $\leq$ 0.4V

Fig. 2



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	2.3 to 10	V
Output Current	I_O	0 to 300 (500*1)	mA
Input High Voltage	V_{IH}	2.1 to V_{CC}+0.3*2	V
Input Low Voltage	V_{IL}	0 to 0.4	V

Note: *1 $t_{ON} \leq 1$ sec, Duty = 50%
*2 When $V_{IH} \geq V_{CC}$, $I_{IH} \leq V_{CC} \times 0.2$mA

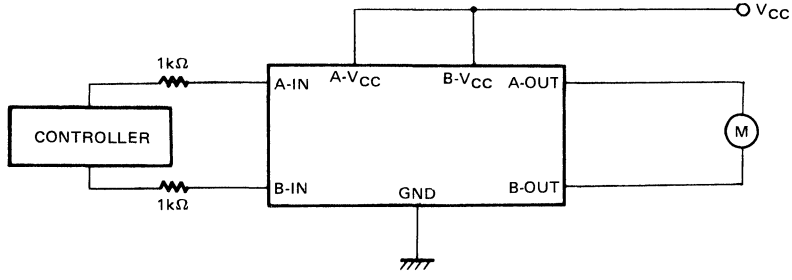
ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V, V_{IH} = 2.4V, I_O = 300mA, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Stand-by Current	I_{CCO}	V_{CC} = 6V, V_{IA} = V_{IB} = 0V			100	μA
Power Supply Current	I_{CC1}	I_O = 0mA		4.5	8	mA
	I_{CC2}	I_O = 300mA		24		mA
	I_{CC3}	I_O = 0mA, V_{IA} = V_{IB} = 2.4V		7		mA
Output High Voltage	V_{OH}		1.85	2.1		V
Output Low Voltage	V_{OL}			0.25	0.35	V
Output Saturation Voltage	V_{SAT}			1.15	1.5	V
Input Current	I_{IH}	V_{IN} = 2.4V		250	400	μA

5

Fig. 3 – APPLICATION EXAMPLE



Note: In the case the control voltage is input when the power supply voltage is not applied because of the time lag between those two voltages, excess current flows into IC from the input terminals.
In this case, please connect a resistor (≥1kΩ) serially to input pin in order to prevent excess current flow.

TYPICAL CHARACTERISTICS CURVES (T_A = 25°C)

Fig. 4 – POWER SUPPLY VOLTAGE vs. POWER SUPPLY CURRENT

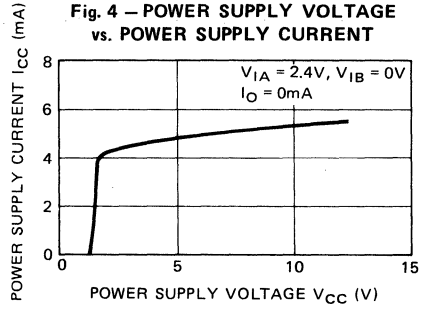


Fig. 5 – POWER SUPPLY VOLTAGE vs. POWER SUPPLY CURRENT (BRAKE MODE)

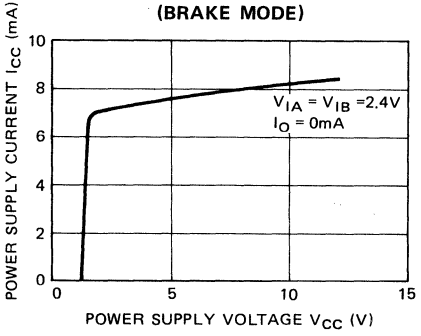


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Fig. 6 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

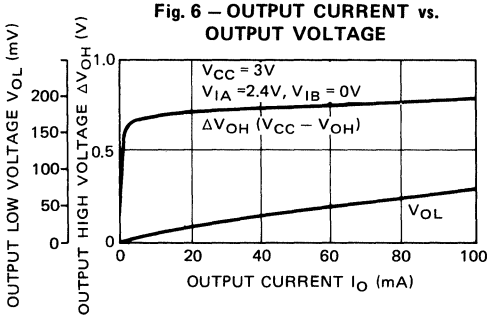
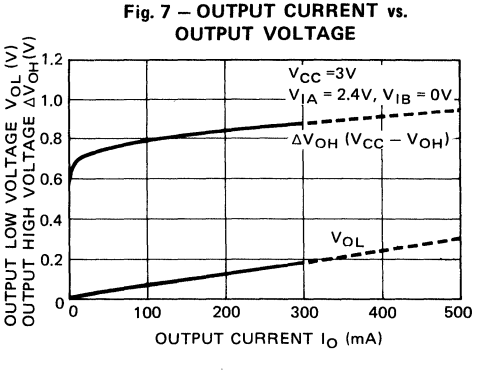


Fig. 7 – OUTPUT CURRENT vs. OUTPUT VOLTAGE



TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 8 – OUTPUT CURRENT vs. POWER SUPPLY CURRENT

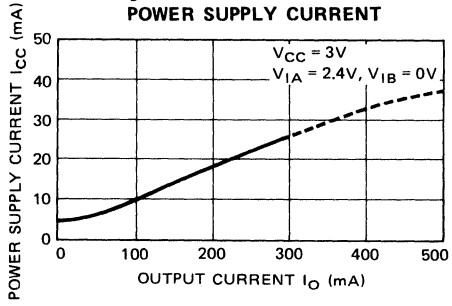


Fig. 9 – INPUT VOLTAGE vs. INPUT CURRENT

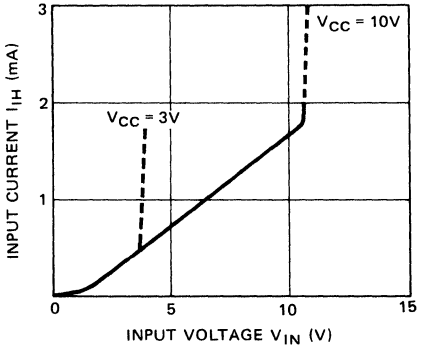


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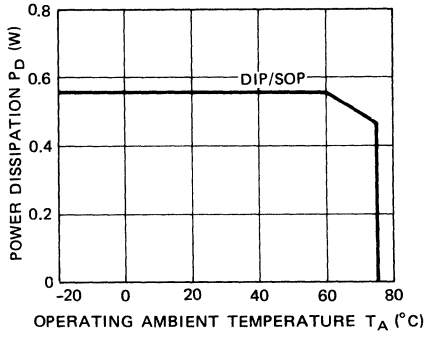
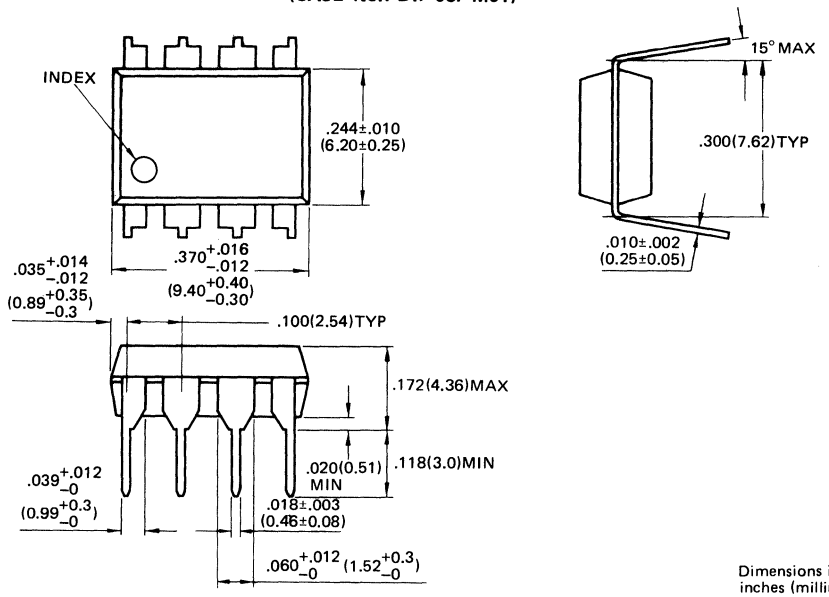
Fig. 10 – POWER DERATING CURVE



Notes: FPT package is mounted on the ceramic board (3.0cm x 3.0cm x 0.05cm).
Maximum power dissipation must be kept.

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)

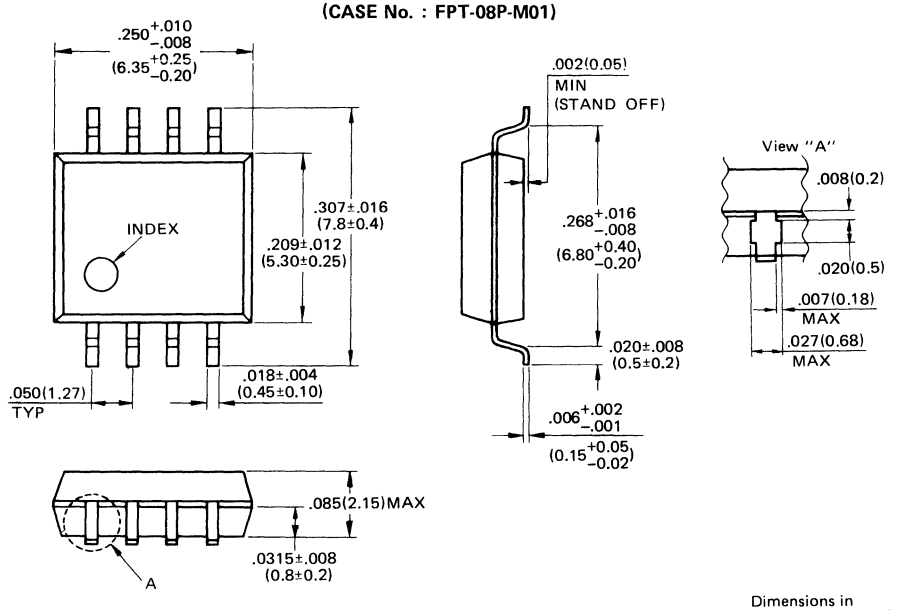


Dimensions in
inches (millimeters)

5

PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in
inches (millimeters)

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Section 6

Disk Drivers

Fujitsu Part No.	Description	Features	Equiv. Prod.	Power Supply (V)	Package	No. of Pins
MB4107	Floppy Disk VFO	VFO with PLL Data Separator, GAP & Mark Detector	—	+5	Plastic DIP Plastic Flatpak	24 24
MB4108	Floppy Disk VFO	VFO with PLL Data Separator, GAP & Mark Detector	—	+5	Plastic DIP Flatpak	24 24
MB4111	Head 4-Ch R/W Amp	AV = 35 V/V, Moving Head	SS1104	+6, -4	Ceramic Flatpak	24
MB4112	Head 4-Ch R/W Amp	AV = 9 V/V, Fixed Head	SS1105	+6, -4	Ceramic Flatpak	24
MB4113	Head 4-Ch R/W Amp	AV = 35 V/V, Moving Head	—	+6, -4	Ceramic Flatpak	24
MB4117-4	Head 4-Ch R/W Amp	AV = 110 V/V,	SS1117	+12, +5	Ceramic Flatpak Plastic Flatpak Plastic DIP	24 24 22
MB4117-6	Head 6-Ch R/W Amp	AV = 110 V/V,	SS1117	+12, +5	Plastic DIP Ceramic Flatpak	28 28
MB4118-4	Head 4-Ch R/W Amp	AV = 100 V/V, Dumping Resistors	SS1118	+12, +5	Ceramic Flatpak Plastic Flatpak Plastic DIP	24 24 22
MB4118-6	Head 6-Ch R/W Amp	AV = 100 V/V, Dumping Resistors	SS1118	+12, +5	Plastic DIP Ceramic Flatpak	28 28
MB4313	Driver/ Receiver	Read/Write Interface	—	-5.2	Ceramic DIP	16
MB4316	Driver/ Receiver for Disk Head Amp	With Write Current Source	—	-5.2 ~ -12	Ceramic DIP	16
MB4319	Head Positions Controller	Head Control	—	+15, -15	Ceramic DIP	16

FUJITSU

FLOPPY DISK VFO

MB 4107

October 1984
Edition 1.0

FLOPPY DISK VFO

The Fujitsu MB 4107 is a variable-frequency oscillator (VFO) IC for use in floppy-disk interfaces. It provides a complete data separation function, with a minimum of external parts and no adjustments, and can be used with a variety of disk controllers. It locks onto the read signal from the disk drive, which normally has jitter due to rotation speed variations and peak shifting, and produces a stable read signal for the controller. It also produces a window signal, which can be used to differentiate the clock and data pulses in the read signal.

The MB 4107 includes functions for sync field detection, automatic loop filter gain switching, and address and index mark detection.

- **The analog VFO (PLL) circuitry allows a wide read margin for the data separator.**
- **Can be connected to both 8-inch and 5-inch floppy disk drives using the same external components.**
- **Handless both double-density (MFM) and single-density (FM) disks.**
- **Can be used with various floppy disk controllers such as the MB 8876A, MB 8877A, FD1791, and μPD 765.**
- **The discrimination function for gap and sync fields prevents incorrect locking on the gap field.**
- **The quick sync function (high gain) in the sync field is automatically switched to the stable tracking function (low gain).**
- **Because the sync pattern detector (data: 00_H, clock: FF_H) and the IBM format mark detector control PLL gain, the index, ID, and data fields can be locked onto without special control signals.**
- **A master clock is generated for the floppy disk controller, to prevent spikes when switching between 8- and 5inch floppy disks.**
- **External circuitry requires very few components, and no adjustments.**
  Internal clock: 7 resistors, 5 capacitor, 1 crystal or ceramic resonator
  External clock: 5 resistors, 3 capacitors

6

Fig. 1 – BLOCK DIAGRAM

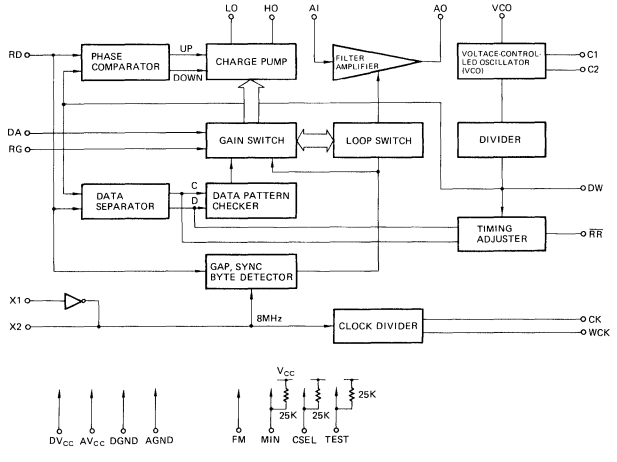


Fig. 2 – PIN ASSIGNMENT

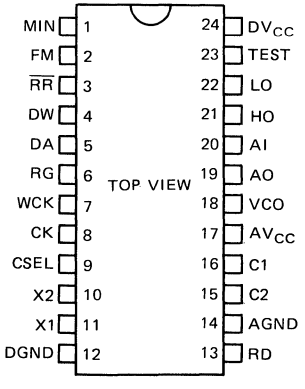


TABLE 1 – PIN FUNCTION

Pin No.	Symbol	Function
1	MIN	Selects type of floppy disk as follows: – 5-inch floppy disk (MIN) High – 8-inch floppy disk (STD) Low
2	FM	Selects the disk density as follows: – Single density (FM system) High – Double density (MFM system) Low
3	$\overline{RR}$	Read data signal for the FDC, including both clock and data pulses.
4	DW	Data window signal for separating the $\overline{RR}$ signal into data and clock pulses.
5	DA	Input for indicating a data field. When DA goes high, the PLL is kept as a low gain. Either RG or DA is used, but not both, and the unused pin is kept low.
6	RG	Read Gate (MB 8877A system) or VCO Sync (μPD765 system) input. When a high signal is applied to this pin, PLL is kept at a low gain.
7	WCK	The μPD 765 system FDC write clock pulse is output from this pin as follow: – 8-inch/MFM T = 1 μs – 8-inch/FM T = 2 μs – 5-inch/MFM T = 2 μs – 5-inch/FM T = 4 μs
8	CK	The FDC clock pulse is output from this pin as follows: – MB 8877A system/8-inch 2 MHz – MB 8877A system/5-inch 1 MHz – μPD 765 system/8-inch 8 MHz – μPD 765 system/5-inch 4 MHz
9	CSEL	Selects the FDC type shown below (an internal pull-up resistor is provided): – MB 8877A, FD 1791 system High – μPD 765 system Low
10	X2	(1) Inverter output for the quartz oscillator (2) This pin is open when a 8-MHz external clock is used.
11	X1	(1) Inverter input for the quartz oscillator (2) Input pin when an 8-MHz external clock is used.
12	DGND	Ground for digital circuits
13	RD	Input for the source read data from the FDD
14	AGND	Ground for analog circuits such as VCO and filter amplifier
15 16	C1 C2	An external capacitor for setting VCO oscillating frequency is connected to these pins.

TABLE 1 – PIN FUNCTION (cont'd)

Pin No.	Symbol	Function
17	AV_{CC}	Power supply for analog circuits such as the VCO and filter amplifier.
18	VCO	VCO control current input.
19	AO	Output pin for the low pass filter (LPF) amplifier in the VFO (PLL) circuit.
20	AI	Input pin for the LPF amplifier in the VFO (PLL) circuit
21	HO	Output pin to be externally connected to the LPF amplifier. This pin is selected at frequency lock after a sync field is detected. A high signal decreases the VCO frequency and a low signal increases it. (High gain)
22	LO	Output pin to be externally connected to the LPF amplifier. This pin is selected after frequency lock, for phase synchronization. A high signal delays the VCO phase, and a low signal advances it. (Low gain)
23	TEST	Used for the LSI function test. It is normally open or pulled up.
24	DV_{CC}	Power supply pin for digital circuits.

TABLE 2 – MAXIMUM RATINGS ($T_A = 25°C$)

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{CC}		7	V
Logic input voltage	V_{IN}		7	V
Power dissipation	P_D	$T \leqq 75°C$	550	mW
Storage temperature	T_{STG}		−55 ~ +125	°C

TABLE 3 – RECOMMENDED OPERATING CONDITIONS

Item	Symbol	MIN	TYP	MAX	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Operating temperature range	T_{OP}	−20	25	75	°C

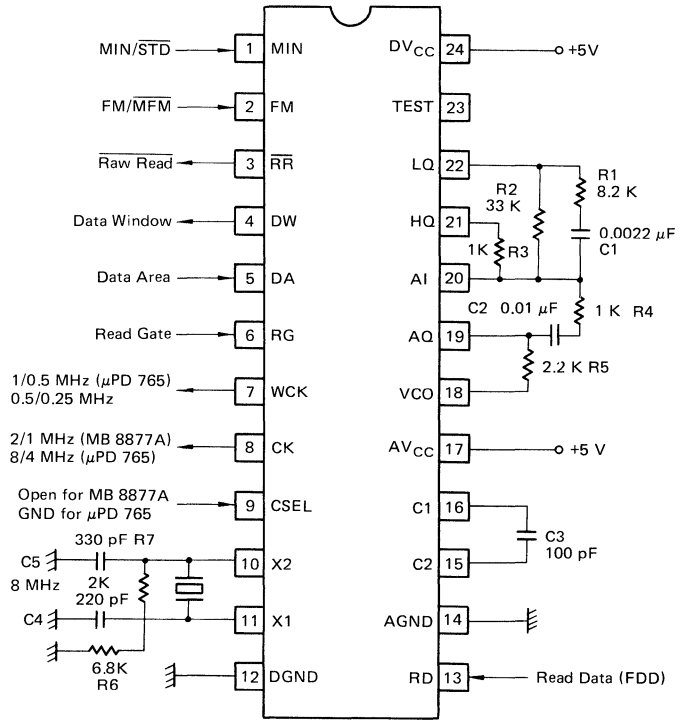
TABLE 4 – ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C)

(Recommended operating conditions unless otherwise noted)

Item	Symbol	Condition	Value			Unit	Applicable pin	Note
			Min	Typ	Max			
Supply current	I_{CC}	V_{CC} = 5.25 V	–	70	100	mA	V_{CC}	–
High level input voltage	V_{IH}	V_{CC} = 4.75 – 5.25 V	2.0	–	–	V	MIN, FM DA, RG CS, X1 RD	*3
Low level input voltage	V_{IL}		–	–	0.8	V		*3
High level input current	I_{IH}	V_{CC} = 5.25 V, V_I = 2.7 V	–	–	20	μA	FM, DA RG, X1 RD	–
Current at maximum input voltage	I_I	V_{CC} = 5.25 V, V_I = 7.0 V	–	–	0.1	mA		–
Low level input current	I_{IL}	V_{CC} = 5.25 V, V_I = 0.4 V	–400	–20	–	μA		–
Open-circuit input voltage	V_{IP}		4.85	5.0	–	V	MIN, CS	–
Low level input current	I_{ILP}	V_I = 0 V	–1.1	–0.6	–	mA		–
High level output voltage 1	V_{OH1}	V_{CC} = 4.75 V, I_{OH} = –1.2 mA	2.7	3.3	–	V	$\overline{RR}$, DW	*1 *3
Low level output voltage 1	V_{OL1}	V_{CC} = 4.75 V, I_{OL} = 12 mA	–	0.28	0.4	V		*2 *3
		V_{CC} = 4.75 V, I_{OL} = 24 mA	–	0.35	0.5	V		
Short-circuit output current 1	I_{OS1}	V_{CC} = 5.25 V	–30	–	–160	mA		*1 *3
High level output voltage 2	V_{OH2}	V_{CC} = 4.75 V, I_{OH} = –0.4 mA	2.7	3.3	–	V	WCK, CK	*1 *3
Low level output voltage 2	V_{OL2}	V_{CC} = 4.75 V, I_{OL} = 4 mA	–	0.28	0.4	V		*2 *3
		V_{CC} = 4.75 V, I_{OL} = 8 mA	–	0.35	0.5	V		
Short-circuit output current 2	I_{OS2}	V_{CC} = 5.25 V	–20	–	–110	mA		*1 *3
High level output voltage 3	V_{OH3}	V_{CC} = 4.75 V, I_{OH} = –0.4 mA	2.7	3.3	–	V	X2	*1 *3
Low level output voltage 3	V_{OL3}	V_{CC} = 4.75 V, I_{OL} = 1 mA	–	0.28	0.4	V		*2 *3
High output voltage	V_{HH}	I_{OH} = –1 mA	3.3	3.7	–	V	HO	*1
Low output voltage	V_{LH}	I_{OL} = 1 mA	–	2.0	2.4	V		*2
High output voltage	V_{HL}	I_{OH} = –0.2 mA	3.8	4.2	–	V	LO	*1
Low output voltage	V_{LL}	I_{OL} = 0.2 mA	–	1.5	1.9	V		*2
VCO free run frequency	f_{FR}		1.6	2.0	2.4	MHz		–

NOTE: *1 The output stage is set high. *2 The output stage is set low. *3 T_A = –20°C to 75°C

Fig. 3 – STANDARD EXTERNAL CIRCUITS (MB 4107)

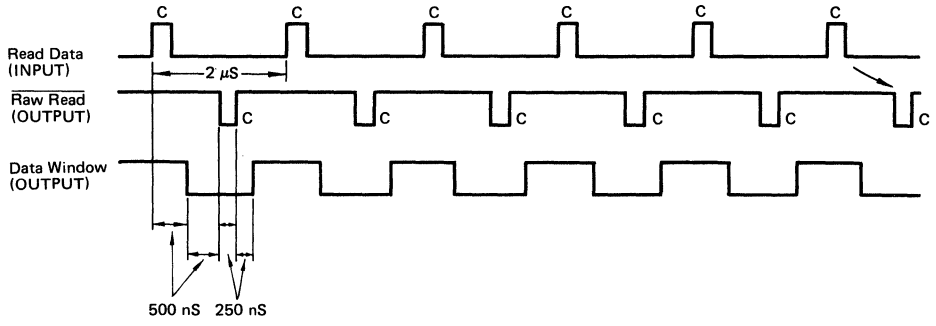


NOTE: 1. C_3 (±5%), R_5 (±1%), otherwise C (±10%), R (±5%)

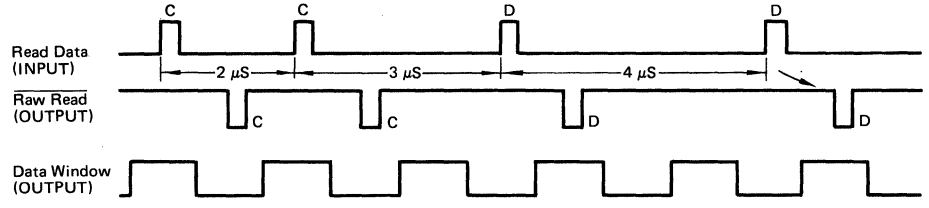
2. Since the 8-MHz internal and 8-MHz external clocks require precision of ±1%, a ceramic resonator can be used when WCK and CK do not require a high precision.

TIMING CHARTS

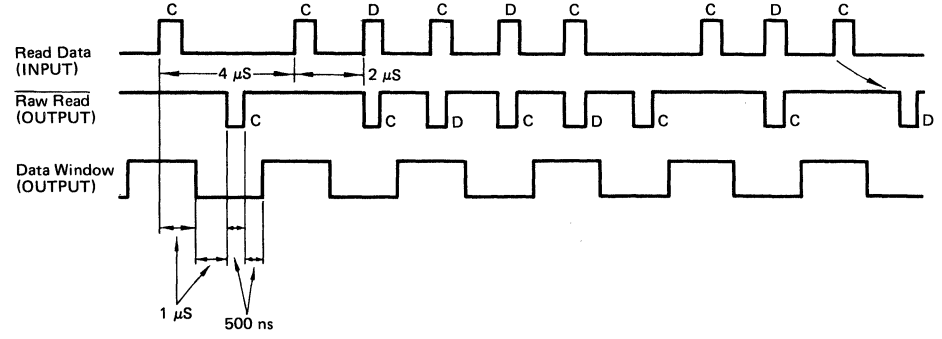
I 8 INCH, MFM, HIGH GAIN (SYNC FIELD)



II 8 INCH, MFM, LOW GAIN



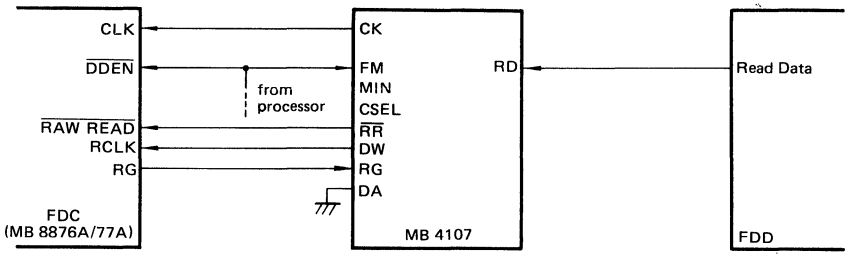
III 8 INCH, FM, LOW GAIN.

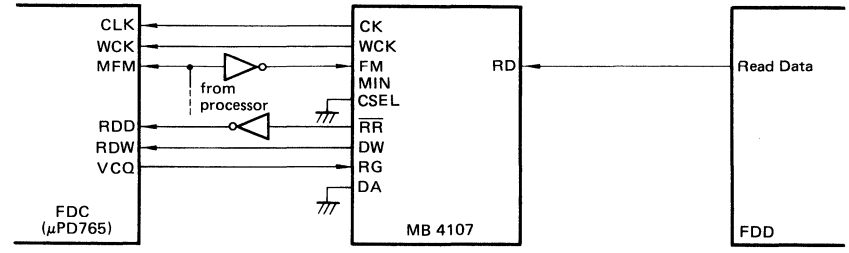


NOTES: 1. The above times are doubled for 5-inch floppy disks.
2. C = clock pulse, D = data pulse

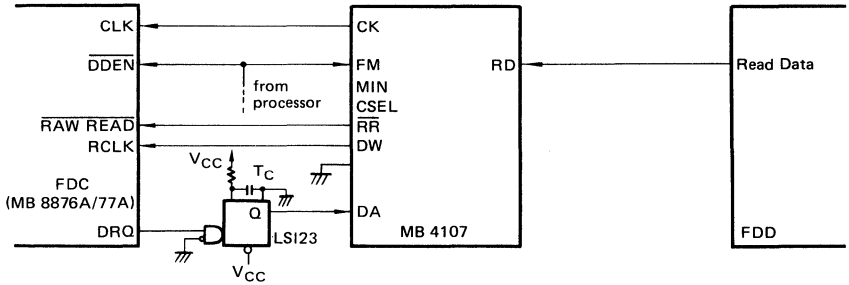
STANDARD CONNECTIONS FDD AND FDC

I READ GATE, VCO SYNC USED

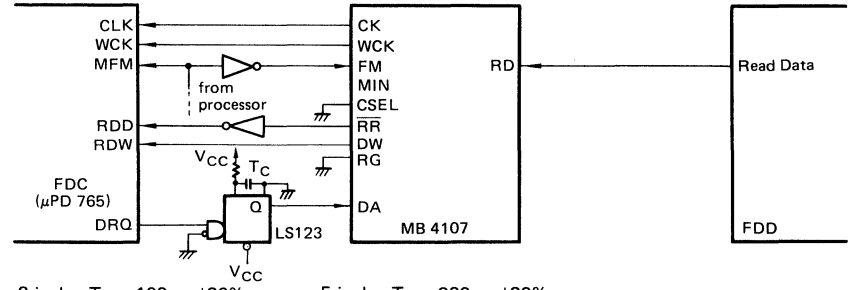




II DATA REQUEST USED



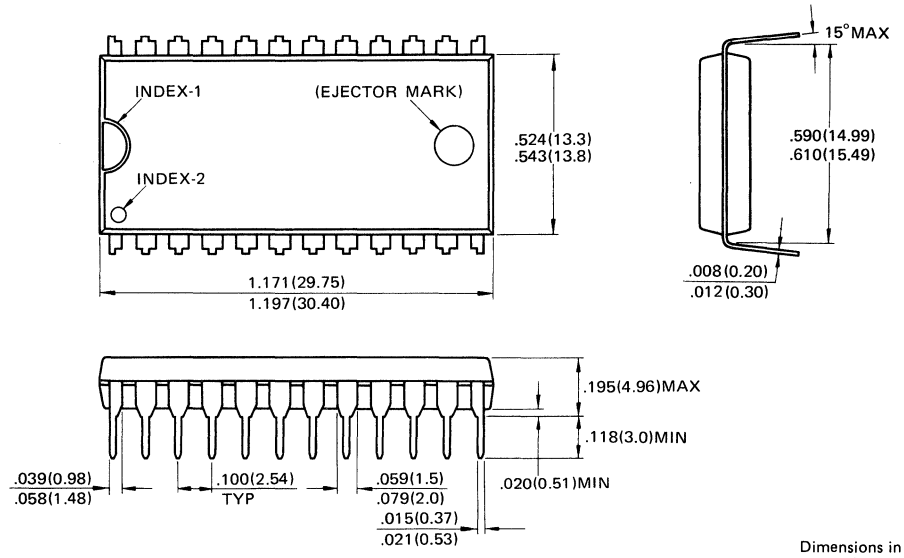
8 inch: T_C = 100 μs ±20% 5 inch: T_C = 200 μs ±20%



8 inch: T_C = 100 μs ±20% 5 inch: T_C = 200 μs ±20%

PACKAGE DIMENSIONS

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M02)



Dimensions in inches (millimeters)

6

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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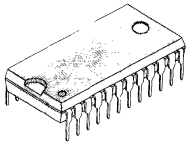
Printed in Japan OV2173-866C

August 1988
Edition 1.0

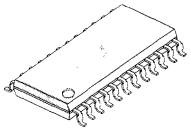
FLOPPY DISK VFO

The Fujitsu MB4108A is variable frequency oscillator (VFO) IC for use in floppy-disk interfaces. It provides a complete data separation function, with a minimum of external parts and no adjustments, and can be used with a variety of disk controllers. It locks onto the read signal from the disk drive, which normally has jitter due to rotation speed variations and peak shifting and produces a stable read signal for the controller. It also produce a window signal which can be used to differentiate the clock and data pulse in the read signal. The MB4108A includes functions for sync field detection, automatic loop filter gain switching and address and index mark detection.

- The analog VFO (PLL) circuitry allows a wide read margin for the data separator.
- Can be connected to both 8-inch and 5-inch floppy disk drives using the same external components.
- Handles both double-density (MFM) and single-density (FM) disks.
- Can be used with various floppy disk controllers such as the MB8876A, MB8877A, FD1791 and μPD765.
- The discrimination function for gap and sync fields prevents incorrect locking on the gap field.
- The quick sync function (high gain) in the sync field is automatically switched to the stable tracking function (low gain)
- Because the sync pattern detector (data: 00H, clock: FFH) and the IBM format mark detector control PLL gain, the index, ID and data fields can be locked onto without special control signals.
- A master clock is generated for the floppy disk controller, to prevent spikes when switching between 8 and 5 inch floppy disks.
- External circuitry requires very few components and no adjustment.
  Internal clock: 7 resistors, 5 capacitors, 1 crystal or ceramic resonator
  External clock: 5 resistors, 3 capacitor

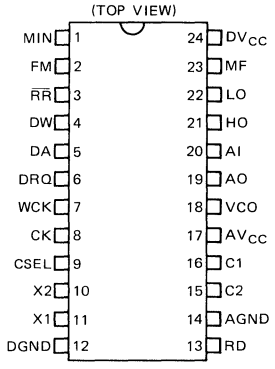


DIP-24P-M02



FPT-24P-M02

PIN ASSIGNMENT



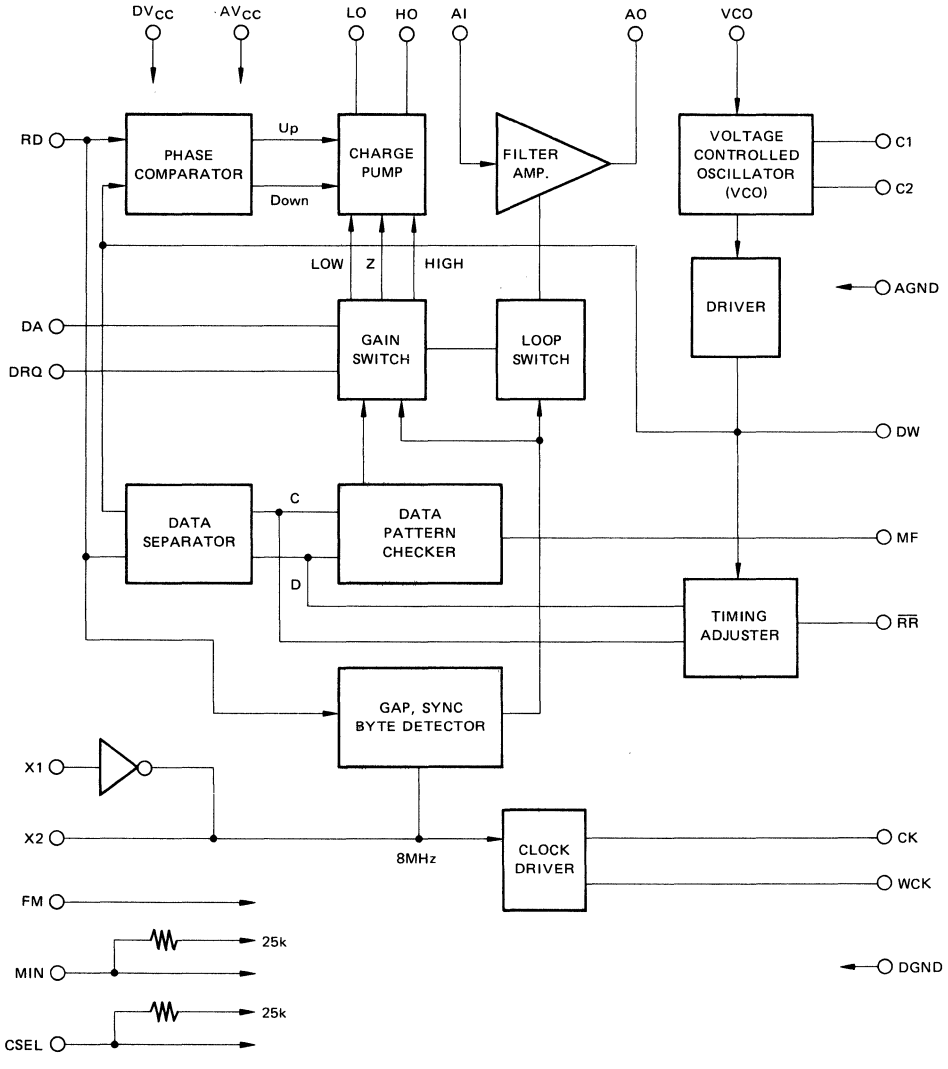
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}		7	V
Input Voltage	V_{IN}		7	V
Power Dissipation	P_D	$T_A \leq 75°C$	550	mW
Storage Temperature	T_{STG}		−55 to +125	°C
MF Input Voltage	V_{MF}		V_{CC}+0.3	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB4108A BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function
1	MIN	Selects type of floppy disk 5-inch floppy disk (MIN): High 8-inch floppy disk (STD): Low
2	FM	Selects the disk density Single density (FM system): High Double density (MFM system): Low
3	$\overline{RR}$	Read data signal for FDC includes clock and data pulse.
4	DW	Data window signal for separating the $\overline{RR}$ signal into data and clock pulses.
5	DA	Input for indicating a data field when there is no DRQ signal. When DRQ = H, the PLL keeps a low gain. Either RG or DA is used, but not both and the unused in is kept low.
6	DRQ	Input for Data Request. After mark is detected, PLL is kept as low gain when DRQ = H (positive edge trigger). 3 bytes data is input, PLL becomes high gain (Free run) when DRQ=L.
7	WCK	The μPD765 system FDC write clock pulse is output from this pin 8-inch/MFM : T = 1μs 8-inch/MF : T = 2μs 5-inch/MFM : T = 2μs 5-inch/MF : T = 4μs
8	CK	The FDC clock pulse is output from this pin MB8877A system/8-inch : 2MHz MB8877A system/5-inch : 1MHz μPD765 system/8-inch : 8MHz μPD765 system/5-inch : 4MHz
9	CSEL	Select the FDC type (On chip pull-up resistor) MB8877A, FD1791 system: High μPD765 system : Low
10	X2	Inverting output of the crystal oscillator The pin is open when 8MHz external clock is used.
11	X1	Inverting input of the crystal oscillator Input pin when 8MHz external clock is used.
12	DGND	Ground of digital circuit
13	RD	Source read data input from FDD
14	AGND	Ground for analog circuit such as VCO, filter amplifier
15 16	C1 C2	An external capacitor is connected to set VCO oscillation frequency
17	AV_{CC}	Power supply for analog circuit such as VCO and filter amplifier.
18	VCO	VCO control current input
19	AO	Low pass filter (LPF) output in the VFO circuit
20	AI	Low pass filter (LPF) input in the VFO circuit
21	HO	Output pin to be externally connected to the LPF amplifier. This pin is selected at frequency lock after a sync field is detected. High signal decreases VCO frequency and Low signal increase it (high gain).
22	LO	Output pin to be externally connected to the LPF amplifier. This pin is selected after frequency lock for phase synchronization. High signal delays the VCO phase and low signal advance it (low gain).
23	MF	When free run mode and high gain mode, MF becomes high. After mark is detected, it becomes low and keeps low level during low gain.
24	DV_{CC}	Power supply for digital circuit

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.75	5.00	5.25	V
Operating Temperature	T_A	-20	+25	+75	°C

DC CHARACTERISTICS

(V_{CC} = 5V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit	Pin name	Note
			Min	Typ	Max			
Power Supply Current	I_{CC}	V_{CC} = 5.25V		70	100	mA	V_{CC}	*1
Input High Voltage	V_{IH}	V_{CC} = 4.75 to 5.25V, T_A = -20 to 75°C	2.0			V	MIN, FM, DA, DRQ, CX, X1, RD	
Input Low Voltage	V_{IL}				0.8	V		
Input High Current	I_{IH}	V_{CC} = 5.25V, V_I = 2.7V			20	μA	FM, DA, DRQ, X1, RD	
Input Current	I_I	V_{CC} = 5.25V, V_I = 7.0V			0.1	mA		
Input Low Current	I_{IL}	V_{CC} = 5.25V, V_I = 0.4V	-400	-20		μA		
Open-circuit Input Voltage	V_{IP}		4.85	5.0		V	MIN, CS	
Input Low Current	I_{ILP}	V_I = 0V	-1.1	-0.6		mA		
Output High Voltage*1	V_{OH1}	V_{CC} = 4.75V, I_{OH} = -1.2mA, T_A = -20 to 75°C	2.7	3.3		V	$\overline{RR}$, DW	*2
Output Low Voltage*1	V_{OL1}	V_{CC} = 4.75V, T_A = -20 to 70°C, I_{OL} = 12mA		0.28	0.4	V		*3
		V_{CC} = 4.75V, T_A = -20 to 70°C, I_{OL} = 24mA		0.35	0.5	V		
Short-Circuit Output Current*1	I_{OS1}	V_{CC} = 5.25V, T_A = -20 to 75°C	-30		-160	mA		*2

Note: *1 AV_{CC} and DV_{CC} are connected together.
*2 The output stage is set high.
*3 The output stage is set low.

DC CHARACTERISTICS

(V_{CC} = 5V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit	Pin name	Note
			Min	Typ	Max			
Output High Voltage*2	V_{OH2}	V_{CC} = 4.75V, I_{OH} = −0.4mA, T_A = −20 to 75°C	2.7	3.3		V	WCK, CK	*2
Output Low Voltage*2	V_{OL2}	V_{CC} = 4.75V, T_A = −20 to 75°C, I_{OL} = 4mA		0.28	0.4	V	WCK, CK	*3
		V_{CC} = 4.75V, T_A = −20 to 75°C, I_{OL} = 8mA		0.35	0.5	V	WCK, CK	*3
Short-Circuit Output Current*2	I_{OS2}	V_{CC} = 5.25V, T_A = −20 to 75°C	−20		−110	mA	WCK, CK	*2
Output High Voltage*3	V_{OH3}	V_{CC} = 4.75V, I_{OH} = −0.4mA, T_A = −20 to 75°C	2.7	3.3		V	X2	*2
Output Low Voltage*3	V_{OL3}	V_{CC} = 4.75V, I_{OL} = 1mA, T_A = −20 to 75°C		0.28	0.4	V	X2	*3
Output Leakage Current	I_{OH4}	V_{CC} = 5.25V, V_O = 5.25V			20	μA	MF	*2
Output Low Voltage	V_{OL4}	V_{CC} = 5.25V, I_O = 1mA, T_A = −20 to 75°C		0.35	0.5	V	MF	*3
Output High Voltage	V_{HH}	I_{OH} = −1mA	3.3	3.7		V	HO	*2
Output Low Voltage	V_{LH}	I_{OL} = 1mA		2.0	2.4	V	HO	*3
Output High Voltage	V_{HL}	I_{OH} = −0.2mA	3.8	4.2		V	LO	*2
Output Low Voltage	V_{LL}	I_{OL} = 0.2mA		1.5	1.9	V	LO	*3
V_{CC} Free Running Frequency	f_{FR}		1.6	2.0	2.4	MHz		

Notes: *2 The output stage is set high.
*3 The output stage is set low.

AC CHARACTERISTICS

(V_{CC} = 5V, f_{X1} = 8MHz)

Pin Name	Parameter	Symbol	Condition		Value Min	Value Typ	Value Max	Unit
CK	Rising Time	t_r	C_L = 25pF			3		ns
	Falling Time	t_f				2		
	Frequency	f_{CK}	CSEL = H MB8876A	MIN = L		2		MHz
				MIN = H		1		
			CSEL = L μPD765	MIN = L		8		
				MIN = H		4		
	Duty Ratio	DR_{CK}	CSEL = H	C_L = 25pF		50		%
			CSEL = L			50		
WCK	Rising Time	t_r	C_L = 25pF			3		ns
	Falling Time	t_f				2		
	Cycle Time	T_{CY}	MIN = L	MFM = H		1		μs
				MFM = L		2		
			MIN = H	MFM = H		2		
				MFM = L		4		
	High level Width	T_{WH}	MIN = L	MFM = H		250		ns
				MFM = L		250		
			MIN = H	MFM = H		500		
				MFM = L		500		

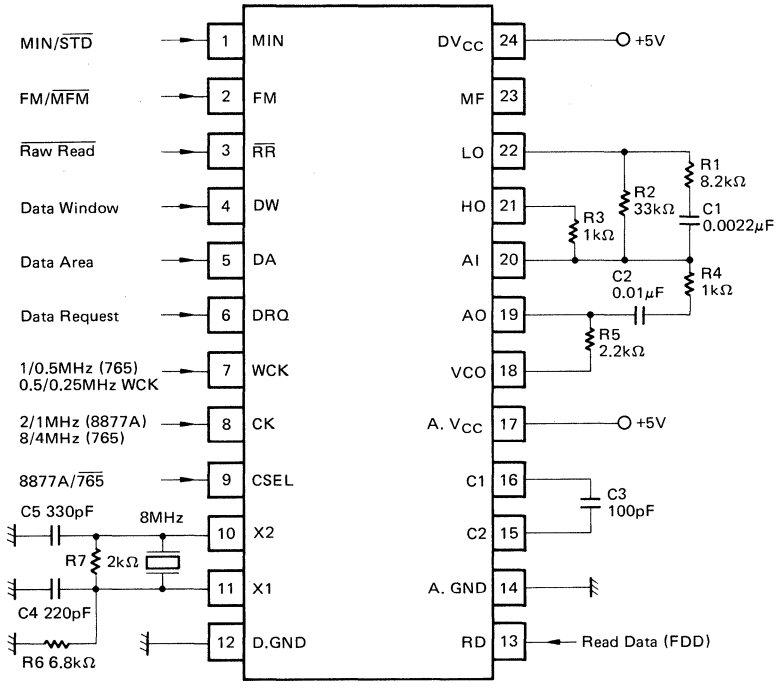
6

(V_{CC} = 5V, f_{X1} = 8MHz)

Pin Name	Parameter	Symbol	Condition		Value			Unit
					Min	Typ	Max	
DW	Rising Time	t_r	C_L = 25pF			3		ns
	Falling Time	t_f				2		
	Window Pulse Width (High level width)	T_W	MIN = L	MFM = H		1		μs
				MFM = L		2		
			MIN = H	MFM = H		2		
				MFM = L		4		
$\overline{RR}$	Rising Time	t_r	C_L = 25pF			3		ns
	Falling Time	t_f				2		
	Low-level Width	T_{WL}	MIN = L	MFM = H		0.25		μs
				MFM = L		0.5		
			MIN = H	MFM = H		0.5		
				MFM = L		1		
	Time Deviation from DW Center	T_D				10		ns
RD	High-level Width	T_{WH}			50			
DRQ	High-level Width	T_{WH}			50			
X1	External Clock Duty Ratio	DXET	f_{X1} = 8MHz/9.6MHz		45	50	55	%

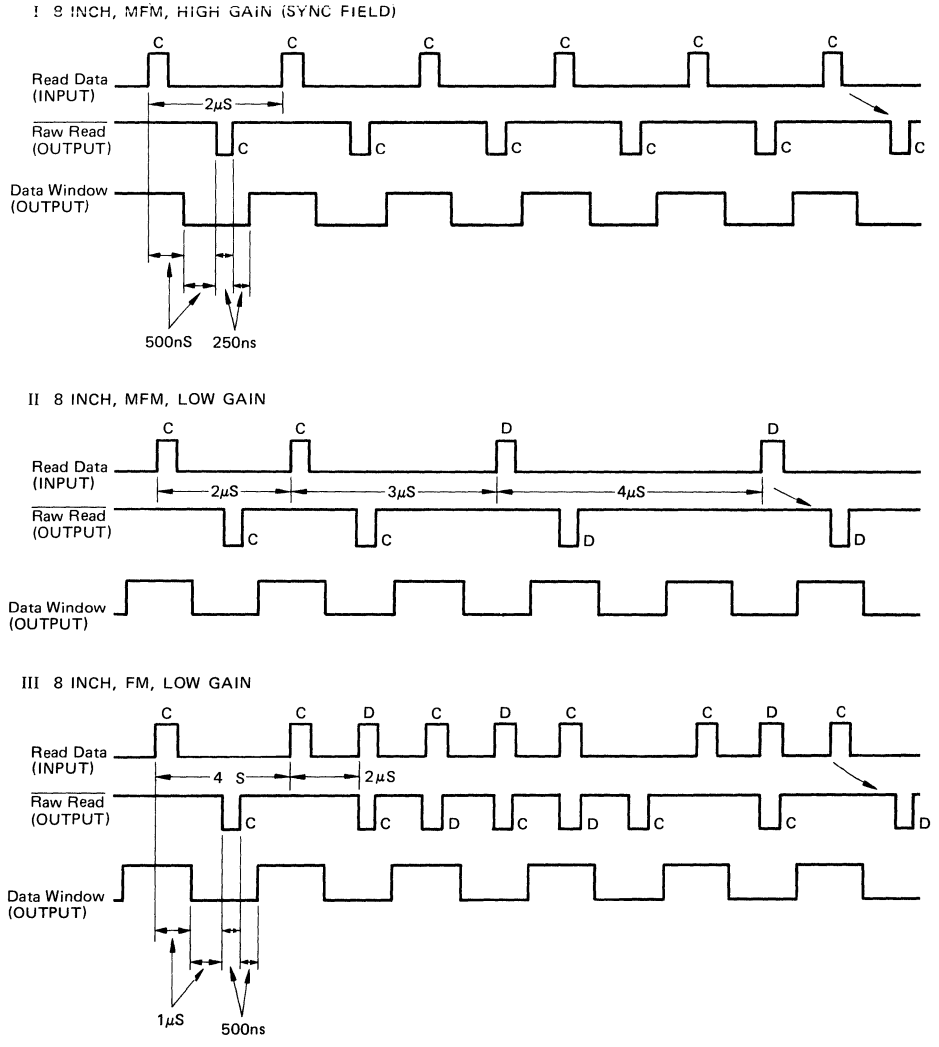
6

Fig. 2 – STANDARD EXTERNAL CIRCUITS



Notes: 1. C_3 (±5%), R_5 (±1%), otherwise C (±10%), R (±5%)
2. Since the 8MHz internal and 8MHz external clocks require precision of ±1%, a ceramic resonator can be used when WCK and CK do not required a high precision.

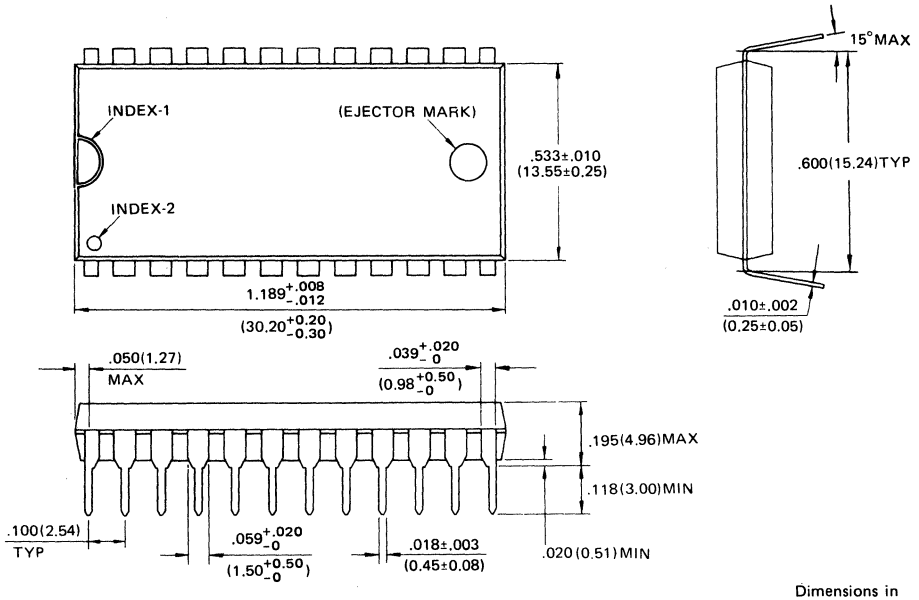
Fig. 3 – TIMING DIAGRAM



Notes: 1. The above times are doubled for 5-inch floppy disks.
2. C = clock pulse, D = data pulse.

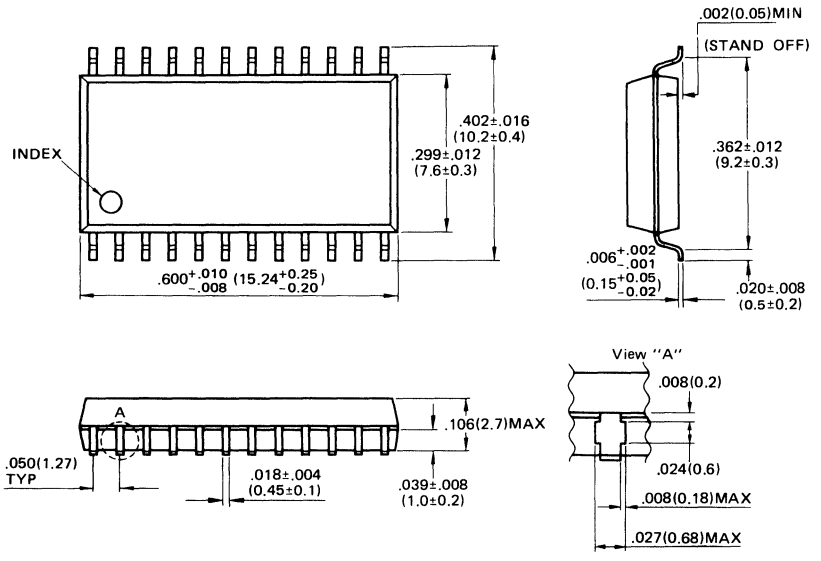
PACKAGE DIMENSIONS

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M02)



Dimensions in
inches (milimeters)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



Dimensions in
inches (millimeters)

FUJITSU

MAGNETIC DISK HEAD AMPLIFIER

MB 4111
MB 4112
MB 4113

March 1984
Edition 2.0

MAGNETIC DISK HEAD AMPLIFIER

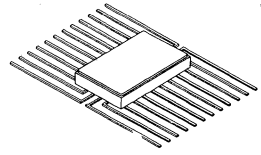
The Fujitsu MB 4111/MB 4112/MB 4113 is a monolithic bipolar integrated circuit optimized for high performance application to disk head systems.

The MB 4111/MB 4112/MB 4113 is featured with the following four major functions to interface with four magnetic heads.

* Write Amplifier Circuit
* Read Amplifier Circuit
* $\overline{RAS}$ (safety) Circuit
* Selection Decode Circuit

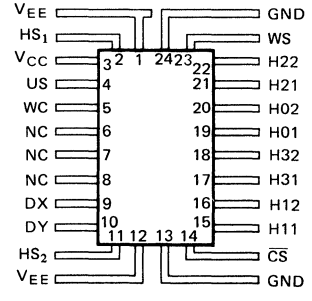
Also, the MB 4111/MB 4112/MB 4113 has three modes, Read, Write and Idle.

The MB 4111/MB 4113 is suitable for mounting directly on the arm of movable disk head.
The MB 4112 is suitable for mounting on the PC board interfacing the fixed disk head.



CERAMIC PACKAGE
FPT-24C-F01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (*: Referenced to ground)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}*	7.0	V
Supply Voltage	V_{EE}*	-5.5	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage (Read/Write/Idle)	V_{CC}	5.7	6.0	6.3	V
Supply Voltage (Read/Write/Idle)	V_{EE}	-4.2	-4.0	-3.8	V

Ambient temperature: 0°C to +70°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN NAMES

No.	Symbol	Name
1	V_{EE}	Supply Voltage
2	HS_1	Head Select 1
3	V_{CC}	Supply Voltage
4	US	Unsafe
5	WC	Write Current
6	NC	Non-connection*
7	NC	Non-connection*
8	NC	Non-connection*

No.	Symbol	Name
9	DX	Data X
10	DY	Data Y
11	HS_2	Head Select 2
12	V_{EE}	Supply Voltage
13	GND	Ground
14	WS	Write Select
15	H11	Head 1
16	H12	

No.	Symbol	Name
17	H31	Head 3
18	H32	
19	H01	Head 0
20	H02	
21	H21	Head 2
22	H22	
23	$\overline{CS}$	Chip Select
24	GND	Ground

Note: NCs should be left open any time.

TEST CONDITIONS

Parameter	Symbol	Mode		Value	Unit
Supply Voltage	V_{CC}	Read/Write/Idle		6.0 ± 1.0%	V
	V_{EE}			-4.0 ± 1.0%	
Head Inductance	L_h	Read/Write	DC	0 (short)	μH
			AC	9.0	
Write Select Voltage	V_{WS}	Write		3.5 ± 1.0%	V
		Read		0.0 ± 0.01	
Chip Select Voltage	V_{CS}	Read/Write		0.0 ± 0.01	V
		Idle		6.0 ± 1.0%	
Unsafe Voltage	V_{US}	Read/Write/Idle		6.0 ± 1.0%	V
Termination Resistor	R_{L1}	Read/Write/Idle		200 ± 1.0%	Ω
	R_{L2}			100 ± 1.0%	
Write Current	I_{WC}	Write		40.0 ± 1.0%	mA
		Read		0.0 ± 0.2	
Ambient Temperature	T_A	Read/Write/Idle		25.0 ± 2.0	°C

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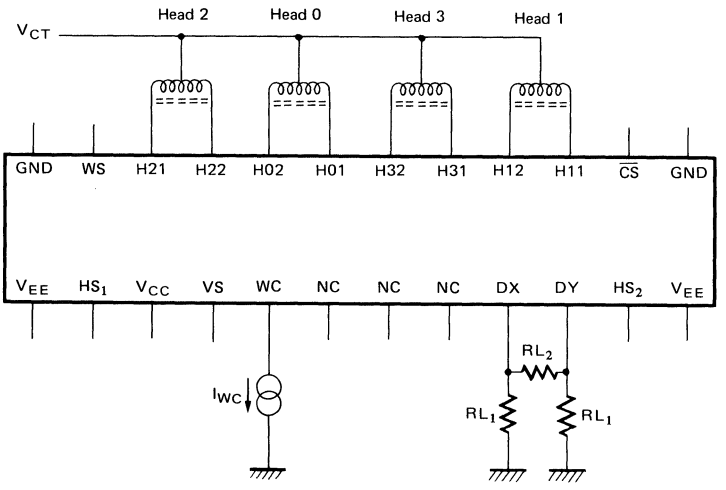
Fig. 1 – TEST CIRCUIT



Note: NCs should be left open.

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Supply Current	I_{CC}	12	16	20	mA	Selected
				100	μA	Non Selected
Supply Current	I_{EE}	-70			mA	Selected
		-45				Non Selected

MODE SELECT

Parameter	Sybmol	Mode	Value			Unit	Note
			Min	Typ	Max		
$\overline{CS}$ Input High Voltage	V_{IHC}	Idle	5.7	6.0	6.3	V	$-50\mu A < I_{CS} < 0\mu A$
$\overline{CS}$ Input Low Voltage	V_{ILC}	Read/Write	0.0	0.35	0.7	V	
$\overline{CS}$ Input High Current	I_{IHC}	Idle	-70			μA	
$\overline{CS}$ Input Low Current	I_{ILC}	Read/Write	-1.3	-1.0	-0.6	mA	V_{CS} = 0V
WS Input High Voltage	V_{IHW}	Write/Idle	3.2	3.5	3.8	V	
WS Input Low Voltage	V_{ILW}	Read/Idle	0	0.1	0.2	V	
WS Input High Current	I_{IHW1}	Write/Idle	0.7		2.8	mA	Transition Unsafe OFF
	I_{IHW2}	Write/Idle	0.7		3.5	mA	Transition Unsafe ON
WS Input Low Current	I_{ILW}	Read/Idle			0.1	mA	
Switching Delay	t_{SD}	All Modes			500	ns	

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TOTAL HEAD INPUT CURRENT

Parameter	Symbol	Mode	Value			Unit	Note
			Min	Typ	Max		
Input Current	I_{I1}	Write			3.0	mA	V_{CT} = 3.5V
Input Current	I_{I2}	Read			0.16	mA	V_{CT} = 0V
Input Current	I_{I3}	Idle			0.5	mA	V_{CT} High or Low

HEAD SELECT

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
HS Input High Voltage	V_{IHH}	T_A = 0°C to +70°C	-0.96		-0.81	V
HS Input Low Voltage	V_{ILH}	T_A = 0°C to +70°C	-1.85		-1.65	V
HS Input High Current	I_{IHH}				240	μA
HS Input Low Current	I_{ILH}				30	μA
Switching Delay	t_{SDH}				100	ns

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HEAD SELECTION TABLE

Head No.	$\overline{CS}$	HS1	HS2
–	High	–	–
0	Low	High	High
1	Low	Low	High
2	Low	High	Low
3	Low	Low	Low

READ MODE

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Differential Gain	MB 4111 MB 4113	A_V	V_{IN} = 1mVp-p, 0V DC, f = 300KHz	22.0	35.0	46.0	V/V
	MB 4112			5.0	9.0	12.5	
Common Mode Rejection Ratio		CMRR	V_{IN} = 5mVp-p, 0V DC, f ≦ 5MHz	45			dB
Power Supply Rejection Ratio		SV_{RR}	V_{IN} = 0V, f ≦ 5MHz	45			dB
Band Width		BW	Z_{IN} = 0Ω (-3dB)	35			MHz
Channel Noise	MB 4111 MB 4113	V_n	V_{IN} = 0V, Z_{IN} = 0Ω, 10MHz Power Band Width			5.4	μV RMS
	MB 4112					20	
Input Current		I_{IN}	V_{IN} = 0V			40	μA
Input Capacitance	MB 4111 MB 4113	C_I				18.8	pF
	MB 4112					16.0	
Differential Input Resistance	MB 4111 MB 4112	R_D		585	750	915	Ω
	MB 4113			380	480	580	
Output Offset Voltage	MB 4111 MB 4113	V_{OFF}		-100		100	mV
	MB 4112			-50		50	
Unsafe Current		I_U	V_{US} = 6.0V, I_{WC} = 45mA	40		45	mA
Dynamic Range	MB 4111 MB 4113	D	DC input voltage where gain is 90% of gain with 0.5 mVp-p input signal	6			mVp-p
	MB 4112			30			
Channel Separation		S_I	See Note	40			dB
Common Mode Output Voltage		V_O		-0.75	-0.60	-0.45	V

Note: V_{IN} = 1mVp-p, f = 300KHz, 3 Channel driven.

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WRITE MODE

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Write Current		I_{WC}				50	mA
Current Gain		A_I	I_{WC} = 50mA	0.95			
Write Current Voltage		V_{WC}	I_{WC} = 45mA	V_{EE}+0.3		V_{EE}+1	V
Differential Input Voltage		V_{IN}		0.225			V
DX DY Input Current		I_{IN}	$-0.75V \leqq V_{DX} \leqq -0.45V$ $-0.75V \leqq V_{DY} \leqq -0.45V$	-2.0		2.0	mA
Unsafe Current		I_{US}	L = 7μH, f = 1.2MHz, I_{WC} = 20mA			0.1	mA
			L = 9μH, f = 0MHz, I_{WC} = 30mA	20			
Head Current Transition Time		t_T	L = 0μH, f = 5MHz I_{WC} = 50mA		5	10	ns
Head Current Hysterisis		t_{HY}	L = 0μH, f = 5MHz I_{WC} = 50mA			2.0	ns
Unselected Head Current		I_{OP}	L = 9μH, f = 2MHz, I_{WC} = 50mA			1.5	mA
Unsafe Switching Delay Time	MB 4111 MB 4112	t_{USD}	L = 9μH, f = 6.0MHz to 0MHz	0.5		4.0	μs
			L = 7μH, f = 0MHz to 1.2MHz			1.0	
	MB 4113		L = 5μH, I_{WC} = 30mA f = 7.5MHz to 0MHz	0.3		4.0	
			L = 3.5μH, I_{WC} = 15mA f = 0MHz to 3.0MHz			1.0	
Differential Head Voltage	MB 4111 MB 4113	V_{DIF}	I_{WC} = 45mA L = 9μH	6.2		7.2	V
	MB 4112		I_{WC} = 45mA L = 9μH	8.0		9.0	

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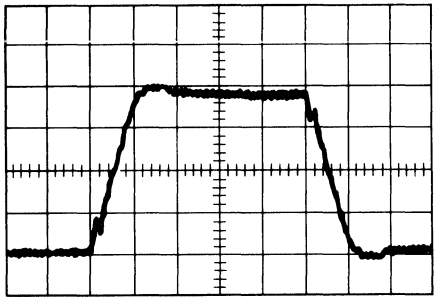
WRITE CURRENT WAVEFORMS

Conditions: L = 9μH, I_{WC} = 40mA

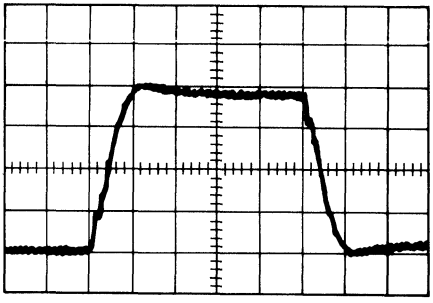
MB 4111



20mA/div

50ns/div

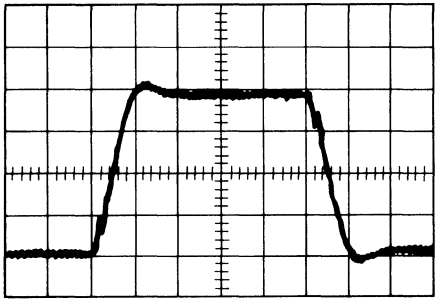
MB 4112



50ns/div

Conditions: L = 7μH, I_{WC} = 40mA

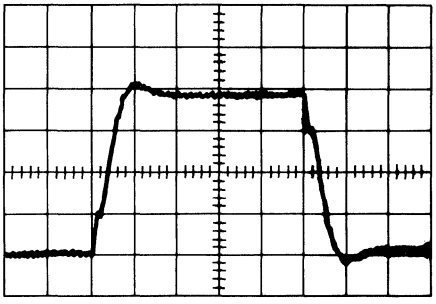
MB 4111



20mA/div

50ns/div

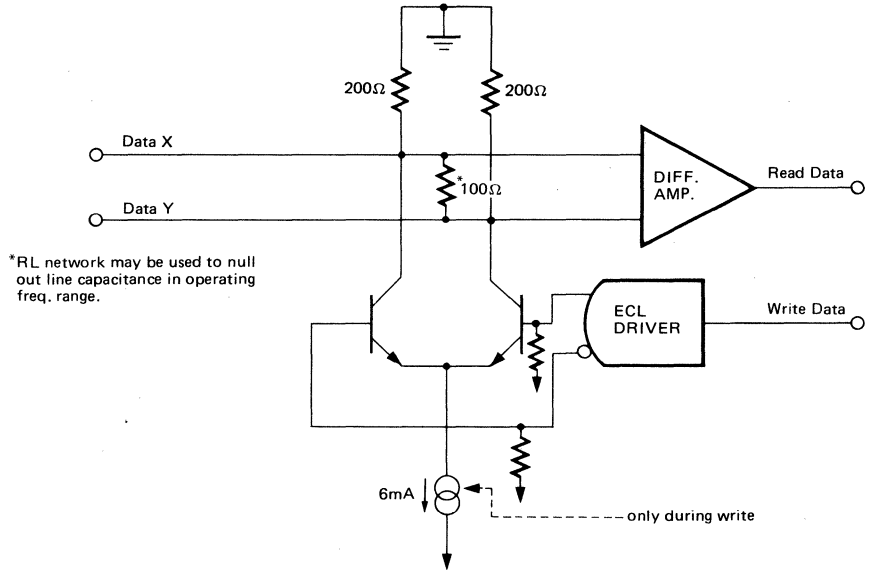
MB 4112



50ns/div

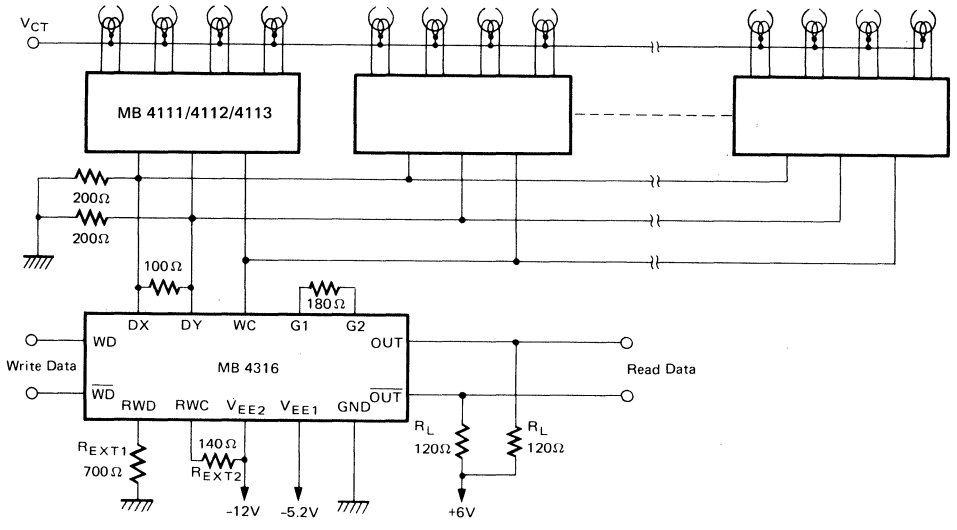
DISK HEAD APPLICATION NOTES

*BIDIRECTIONAL DATA BUS DRIVER



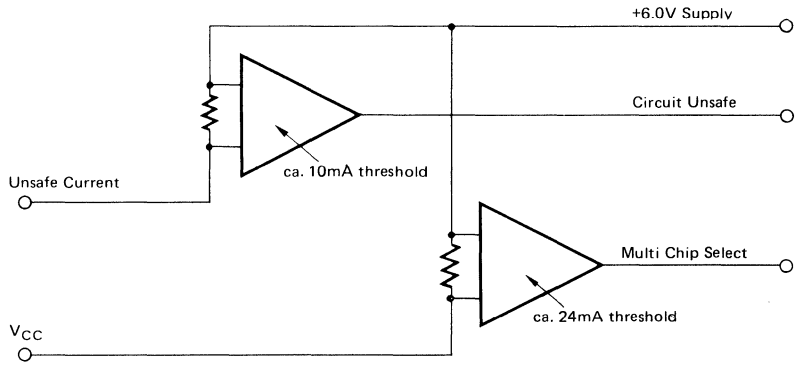
*RL network may be used to null out line capacitance in operating freq. range.

*USAGE IN COMBINATION WITH MB 4316 (BUS SWITCHING CIRCUIT)

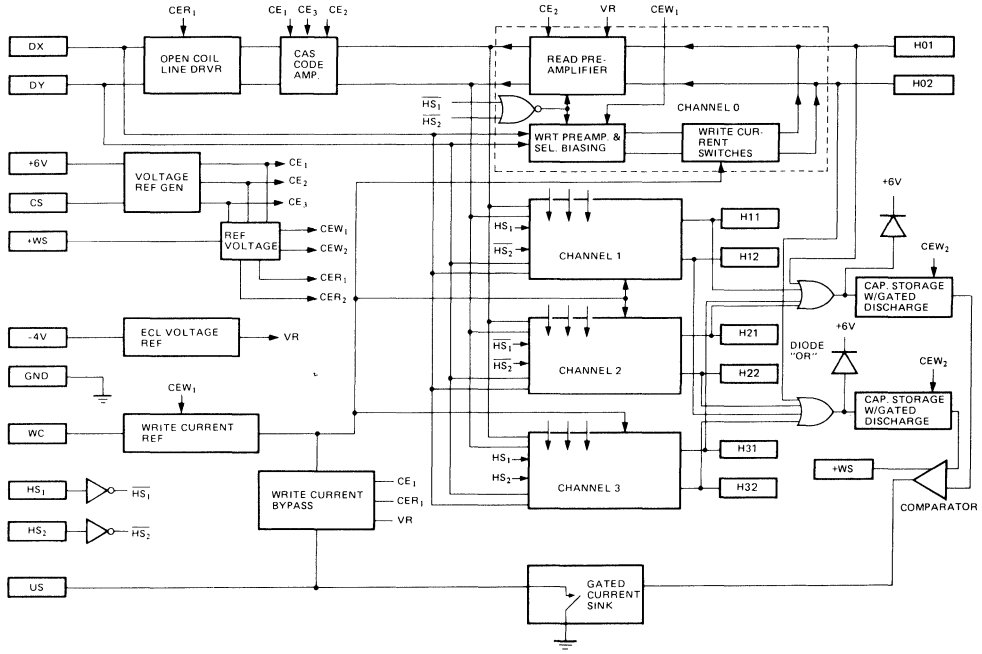


Note: NCs should be left open.

*FAULT DETECTION CIRCUITRY

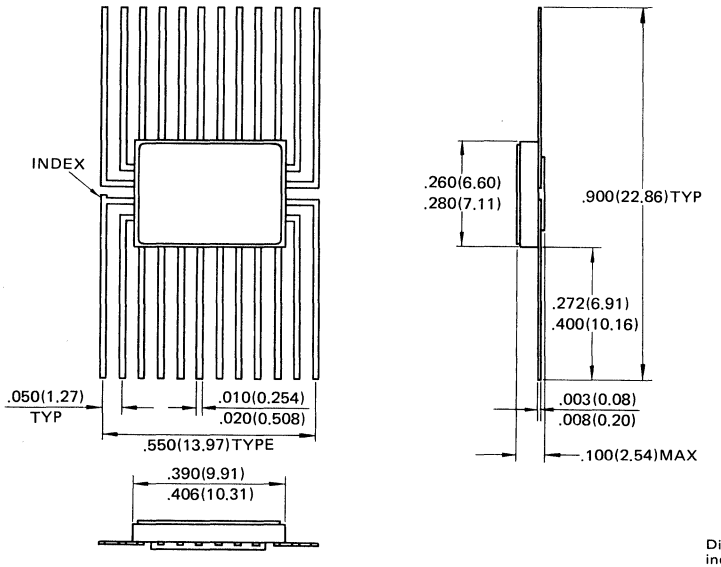


MB 4111/4112/4113 BLOCK DIAGRAM



PACKAGE DIMENSIONS

24-PAD CERAMIC (FRIT SEAL) FLAT PACKAGE
(CASE No. : FPT-24C-F01)



Dimensions in
inches (millimeters)

6

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

MAGNETIC DISK HEAD AMPLIFIER

MB 4117-4
MB 4117-6
MB 4118-4
MB 4118-6

August 1988
Edition 2.1

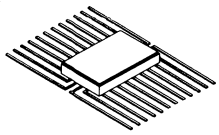
MAGNETIC DISK HEAD AMPLIFIER

The Fujitsu MB 4117-4 and MB 4118-4 are magnetic disk head amplifiers with Zener-zapped write current sourse for 4-channel head, MB 4117-6 and MB 4118-6 for 6-channel.

Their logic interface level is TTL level and their packages are suitable for mounting directly on the arm of movable disk head.

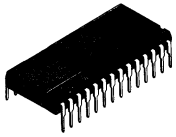
MB 4118 has on-chip dumping resistors for each channel.

- Four major functions to interface with magnetic heads: Write Amplifier/Read Amplifier/$\overline{RAS}$ (safety)/Selection Decode
- Three modes: Read/Write/Idel
- Power Supply Voltage: +5 V and +12 V
- Logic interface level: TTL compatible
- On-chip Zener-zapped write current source.
  Its current can be adjustable with external resistor.
- On-chip dumping resistors (MB 4118 only)



(MB 4117-4/MB 4118-4)
CERAMIC PACKAGE
FPT-24C-F01

DIP-22P-M03: See Page 8
FPT-24P-M02: See Page 9



(MB 4117-6/MB 4118-6)
PLASTIC PACKAGE
DIP-28P-M02

FPT-28C-A01: See Page 11

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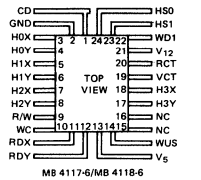
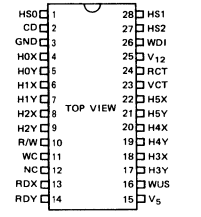
PIN ASSIGNMENT

MB 4117-4/MB 4118-4



MB 4117-6/MB 4118-6



DIP-22P-M03: See Page 8
FPT-24P-M02: See Page 9
FPT-28C-A01: See Page 11

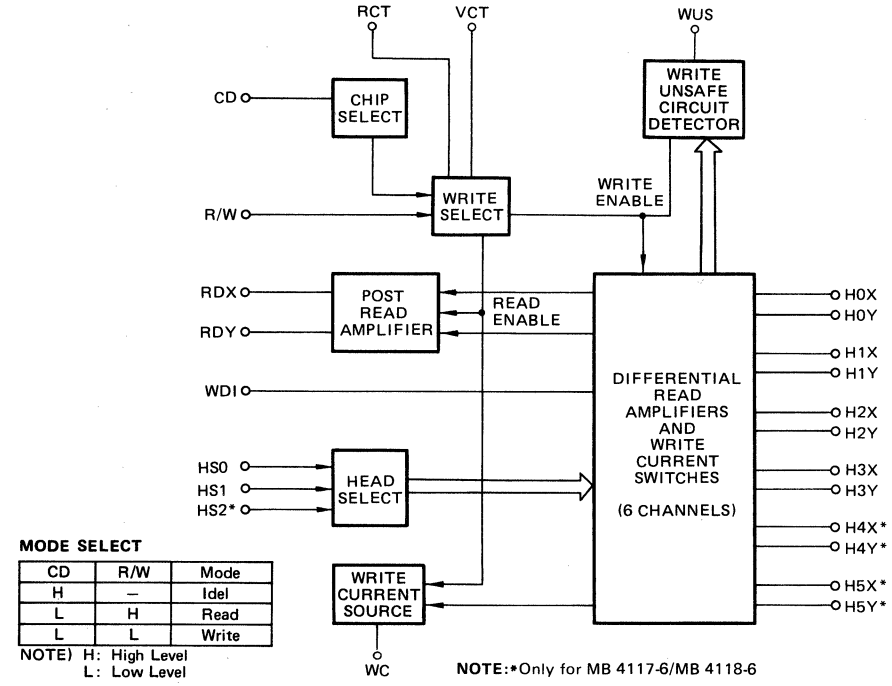
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{12}	14.0	V
Supply Voltage	V_5	6.0	V
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM OF MB 4117/MB 4118



MODE SELECT

CD	R/W	Mode
H	–	Idel
L	H	Read
L	L	Write

NOTE) H: High Level
L: Low Level

NOTE: *Only for MB 4117-6/MB 4118-6

HEAD SELECTION TABLE FOR MB 4117-4/MB 4118-4

Head No.	HS0	HS1
0	Low	Low
1	High	Low
2	Low	High
3	High	High

HEAD SELECTION TABLE FOR MB 4117-6/MB 4118-6

Head No.	HS0	HS1	HS2
0	Low	Low	Low
1	High	Low	Low
2	Low	High	Low
3	High	High	Low
4	Low	Low	High
5	High	Low	High

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage (Read/Write/Idel)	V_{12}	10.8	12.0	13.2	V
Supply Voltage (Read/Write/Idel)	V_5	4.75	5.0	5.25	V
High-level Input Voltage	V_{IH}	2.0		V_5+0.3	V
Low-level Input Voltage	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted.)

Parameter	Symbol	Condition	Mode*	Value			Unit
				Min	Typ	Max	
Power Supply Current	I_{5I}		I	–	17	28	mA
	I_{12I}		I	–	17	28	
	I_{5R}		R	–	14	25	
	I_{12R}		R	–	34	50	
	I_{5W}		W	–	20	30	
	I_{12W}		W	–	20+I_W	30+I_W	
CD Input Current	I_{CDH}	V_{CD} = 2.0 V	I	–	–	0.1	mA
	I_{CDL}	V_{CD} = 0.8 V	R/W	-0.4	-0.2	–	
R/W Input Current	$I_{R/WH}$	$V_{R/W}$ = 2.0 V	I/R	–	–	0.1	mA
	$I_{R/WL}$	$V_{R/W}$ = 0.8 V	I/W	-0.4	-0.2	–	
HS Input Current	I_{HSH}	$V_{HS0,HS0,(HS2)}$ = 2.0 V	I/R/W	–	–	0.1	mA
	I_{HSL}	$V_{HS0,HS1,(HS2)}$ = 0.8 V	I/R/W	-0.4	-0.2	–	
WDI Input Current	I_{WDIH}	V_{WDI} = 2.0 V	I/R/W	–	–	0.1	mA
	I_{WDIL}	V_{WDI} = 0.8 V	I/R/W	-0.4	-0.2	–	
HEAD Input Current	I_{HI}	V_{CD} = 2.0 V	I	–	–	0.1	mA
	I_{HR}	$V_{R/W}$ = 2.0 V	R	–	25	45	μA

NOTE: *I: Idle, R: Read, W: Write

READ MODE

(Recommended operating condition unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Differential Voltage Gain	A_V	V_{IN} = 1 mV_{PP}, f = 300 kHz R_L = 1 kΩ		80	100	120	V/V
Band Width	B_W	V_{IN} = 1 mV_{PP}, R_L = 1 kΩ (–3 dB)		30	–	–	MHz
Input Noise Voltage	V_n	T_A = 25°C, B_W = 1 to 10 MHz		–	–	5.4	μV_{rms}
Input Capacitance	C_I	f = 5 MHz		–	–	23	pF
Differential Input Registance	R_D		MB 4117	2	–	–	kΩ
			MB 4118	525	750	975	Ω
Single-End Output Registance	R_O	f = 5 MHz		–	–	100	Ω
R_{DX}, R_{DY} Output Voltage	V_{RDX}			5.0	–	7.0	V
	V_{RDY}						
Output Offset Voltage	V_{OFF}			-480	–	+480	mV
Dynamic Range	D	f = 5 MHz		6	–	–	mV_{PP}
Common Mode Rejection Ratio	CMRR	f = 5 MHz, V_{IN} = 100 mV_{PP}		50	–	–	dB
Channel Separation	CSP	f = 300 kHz, V_{IN} = 1 mV_{PP}		45	–	–	dB
Power Supply Rejection Ratio	PSRR1	f = 5 MHz, V_5 = 100 mV_{PP}		45	–	–	dB
	PSRR2	f = 5 MHz, V_{12} = 100 mV_{PP}		45	–	–	dB

6

WRITE MODE

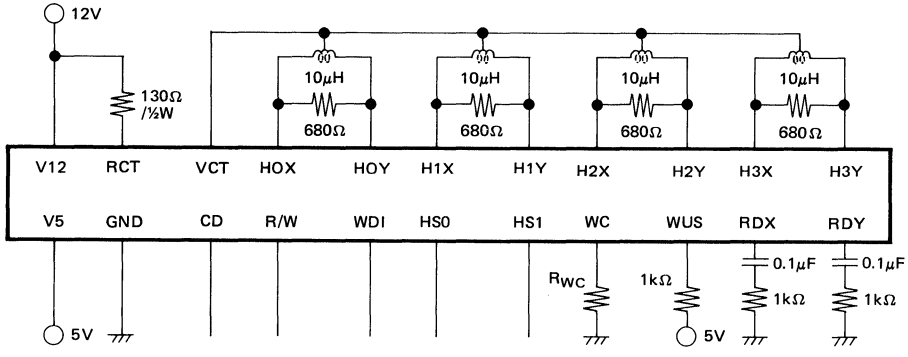
(Recommended operating condition unless otherwise noted.)

Parameter	Symbol	Condition		Value Min	Value Typ	Value Max	Unit
Write Current	I_W		Plastic	8		30	mA
			Ceramic	8		50	
Write Current Constant	K*	I_W = 18 mA, K = $I_W \times R_{WC}$		128	140	152	V
Head Differential Voltage	V_{DIF}	L = 10 μH, I_W = 45 mA		6	8		V
Write Unsafe Switching Output Voltage	V_{USL}	L = 10 μH, I_W = 8 mA f_{WDI} = 2.5 MHz, I_{US} = 8 mA				0.5	V
Write Current Transition Time	t_r t_f	L = 0 μH, I_W = 45 mA				20	ns
Write Unsafe Switching Delay Time	t_{US}	L = 10 μH, I_W = 50 mA f_{WDI} = 5.0 MHz to 0 MHz		1.0		8.0	μs

NOTE: *K = $I_W \times R_{WC}$ (External resistor setting write current.)

6

Fig. 2 – MEASUREMENT CIRCUIT (MB 4117-4)



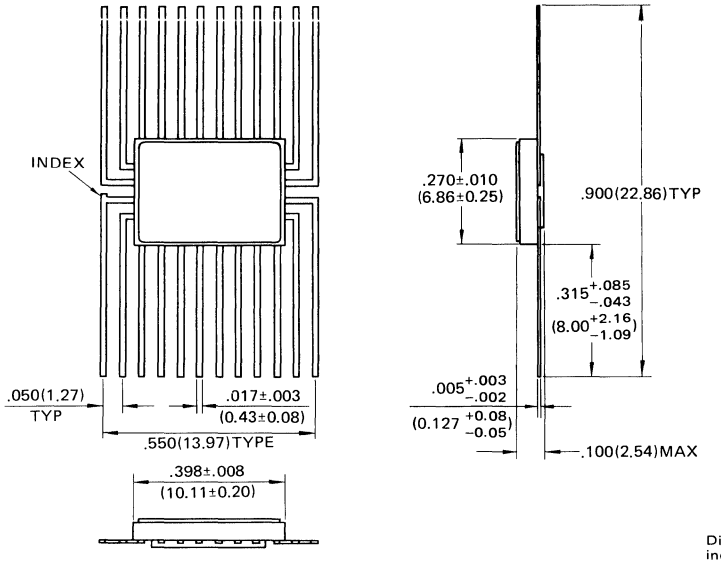
6

MEASUREMENT CONDITIONS

Parameter	Symbol	Condition		Value	Unit
Power Supply Voltage	V_{12}	Read/Write/Idle mode		12 ± 0.24	V
	V_5			5 ± 0.1	
Inductance of Magnetic Head	L_H	Read/Write mode	DC	0	μH
			AC	10	
CD Voltage	V_{CD}	Read/Write mode		0.2 ± 0.2	V
		Idle mode		3.3 to 5.0	
R/W Voltage	$V_{R/W}$	Write/Idle mode		0.2 ± 0.2	V
		Read/Idle mode		3.3 to 5.0	
HS Voltage	V_{HS0} $V_{HS1/(HS2)}$	Read/Write/Idle mode		0.2 ± 0.2	V
				3.3 to 5.0	
WDI Voltage	V_{WDI}	Read/Write/Idle mode		0.2 ± 0.2	V
				3.3 to 5.0	
Ambient Temperature	T_A	Read/Write/Idle mode		25 ± 2.0	°C

PACKAGE DIMENSIONS (MB 4117-4/MB 4118-4)

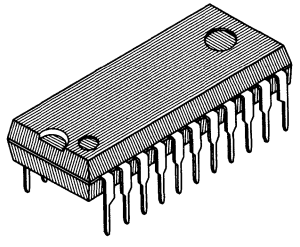
24-PAD CERAMIC (FRIT SEAL) FLAT PACKAGE
(CASE No. : FPT-24C-F01)



Dimensions in
inches (millimeters)

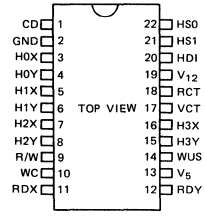
6

PACKAGE DIMENSIONS (MB 4117-4/MB 4118-4)

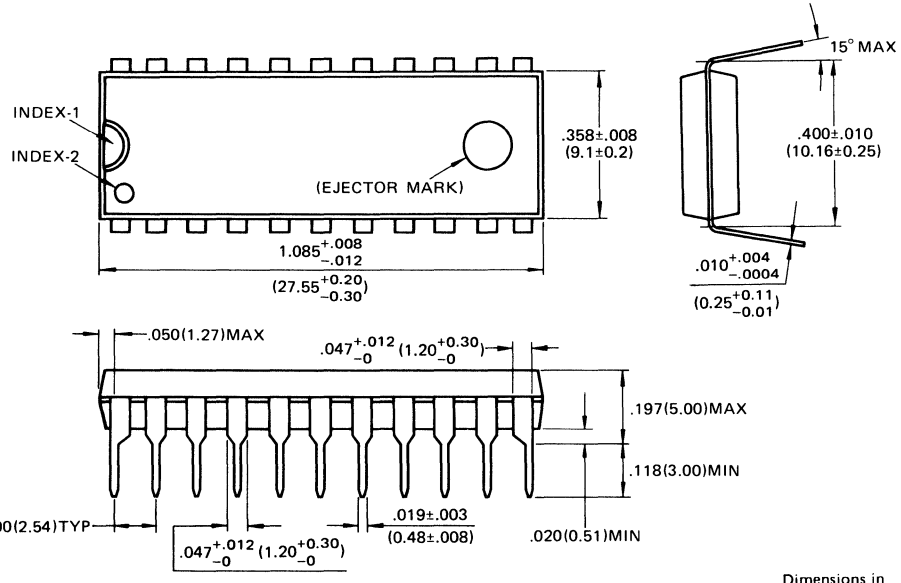


DIP-22P-M03

PIN ASSIGNMENT

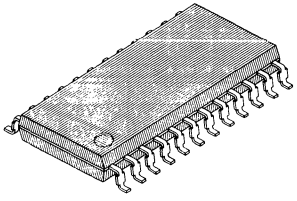


22-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-22P-M03)



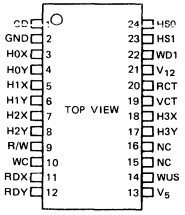
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (MB 4117-4/MB 4118-4)

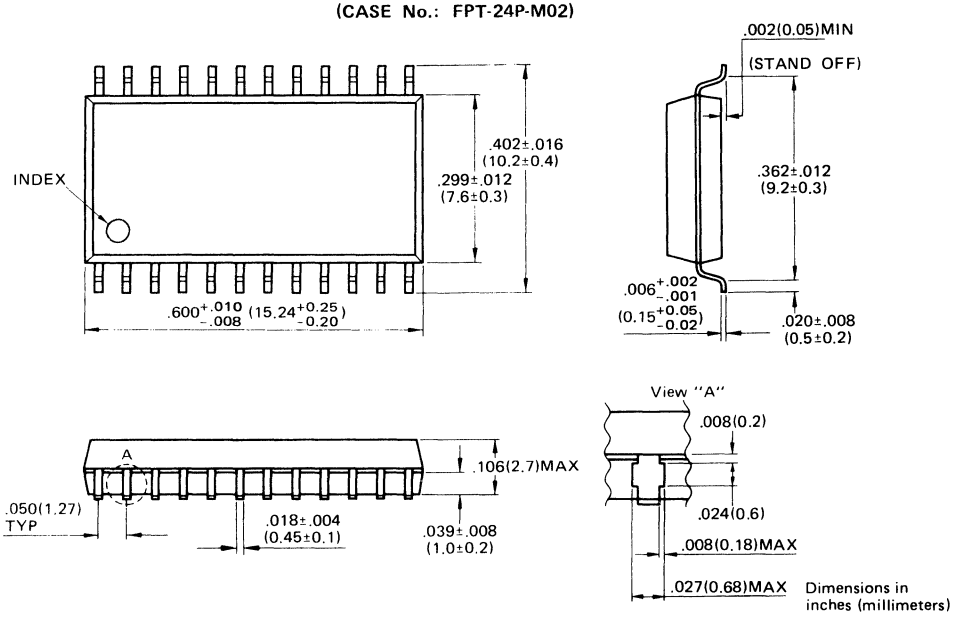


FPT-24P-M02

PIN ASSIGNMENT



24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



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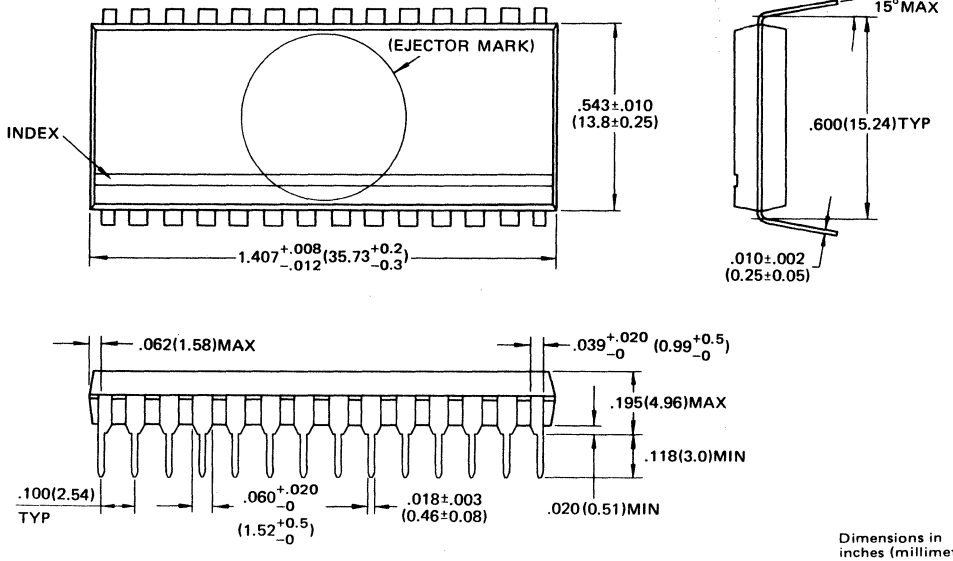
PACKAGE DIMENSIONS (MB 4117-6/MB 4118-6)

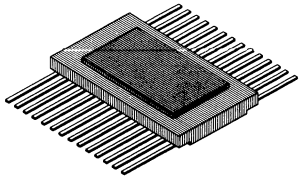
28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)



Dimensions in inches (millimeters)

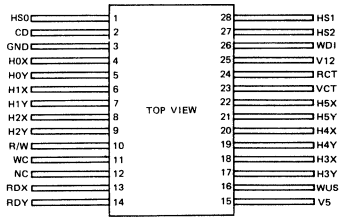
6

PACKAGE DIMENSIONS (MB 4117-6/MB 4118-6)

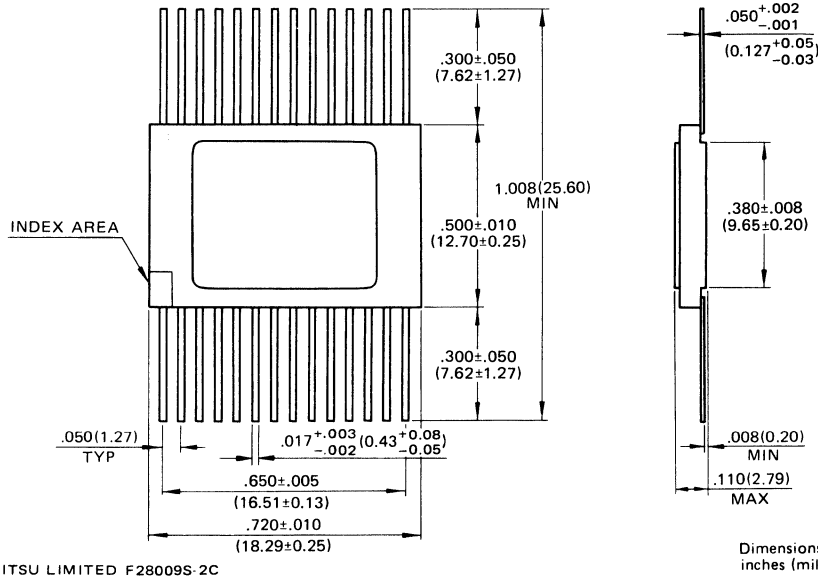


FPT-28C-A01

PIN ASSIGNMENT



28-LEAD CERAMIC (FRIT SEAL) FLAT PACKAGE
(CASE No.: FPT-28C-A01)



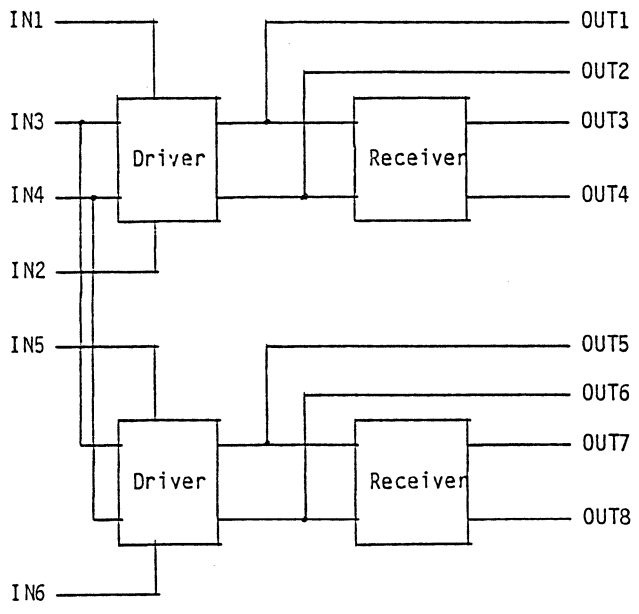
Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

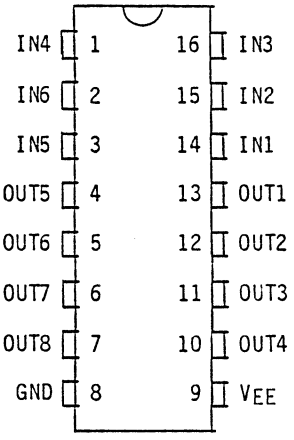
MB4313
READ/WRITE BUS DRIVER/RECEIVER

The Fujitsu MB4313 is designed for driver/receiver as an interface part between magnetic disk drive and control unit. The MB4313 transfers the read-out singal from disk head to control unit, and write signal vice versa.

BLOCK DIAGRAM



PIN ASSIGNMENT
(TOP VIEW)



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INPUT/OUTPUT CONDITIONS

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Input Voltage Pin:1,3,14,16	T_A= 0°C	V_{IN}	-1.87		-0.86	V
	T_A=25°C		-0.85		-0.81	V
	T_A=70°C		-1.825		-0.7	V
Input Current Pin:2,15		I_{IN}			13	mA
Output Current Pin:4,5,12,13		I_{OUT}			5	mA
Supply Voltage		V_{EE}	-5.46	-5.2	-4.94	V
Operating Temperature		T_A	0		+70	°C

ELECTRICAL CHARACTERISTICS
(V_{EE}=-5.2V±5% at T_A=0 to 70 °C, otherwise noted.)

DC Characteristics

(Deviation : ±2%)

Parameter	Conditions	Symbol	Value at T_A=25±2°C			Value at T_A=0 to 70°C			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	$V_{IN1}=V_{IN5}=V_{Hmin}$, $V_{IN3}=V_{Hmax}$, $V_{IN4}=V_{Hmin}$	V_{01H}				-10			mV
		V_{05H}				-10			mV
		V_{03H}		-0.8		-1.0		-0.6	V
		V_{07H}		-0.8		-1.0		-0.6	V

ELECTRICAL CHARACTERISTICS (Cont'd)
(V_{EE}=-5.2V±5% at T_A=0 to 70 °C, otl wise noted.)

DC Characteristics (Cont'd)

(Deviation : ±2%)

Parameter	Conditions	Symbol	Value at T_A=25±2°C			Value at T_A=0 to 70°C			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	$V_{IN1}=V_{IN5}=V_{Hmin}$, $V_{IN3}=V_{Lmin}$, $V_{IN4}=V_{Hmax}$	V_{O2H}				-10			mV
		V_{O6H}				-10			mV
		V_{O4H}		-0.8		-1.0		-0.6	V
		V_{O8H}		-0.8		-1.0		-0.6	V
	$V_{IN1}=V_{IN4}=V_{Lmax}$, $V_{IN5}=V_{IN3}=V_{Hmin}$	V_{O1L}		-0.51		-0.7		-0.4	V
		V_{O3L}		-1.32		-1.6		-1.0	V
	$V_{IN1}=V_{IN3}=V_{Lmax}$, $V_{IN5}=V_{IN4}=V_{Hmin}$	V_{O2L}		-0.51		-0.7		-0.4	V
		V_{O4L}		-1.32		-1.6		-1.0	V
	$V_{IN1}=V_{IN3}=V_{Hmin}$, $V_{IN5}=V_{IN4}=V_{Lmax}$	V_{O5L}		-0.51		-0.7		-0.4	V
		V_{O7L}		-1.32		-1.6		-1.0	V
	$V_{IN1}=V_{IN4}=V_{Hmax}$, $V_{IN5}=V_{IN3}=V_{Lmax}$	V_{O6L}		-0.51		-0.7		-0.4	V
		V_{O8L}		-1.32		-1.6		-1.0	V
Input Current	$V_{IN1}=V_{Hmax}$	I_{IN1}		20				100	µA
	$V_{IN5}=V_{Hmax}$	I_{IN5}		20				100	µA
	$V_{IN3}=V_{Hmax}$, $V_{IN1}=V_{IN4}=V_{Lmin}$	I_{IN3}		20				400	µA
	$V_{IN4}=V_{Hmax}$ $V_{IN1}=V_{IN4}=V_{Lmin}$	I_{IN4}		20				400	µA

ELECTRICAL CHARACTERISTICS (Cont'd)
(V_{EE}=-5.2V±5% at T_A=0 to 70 °C, otherwise noted.)

DC Characteristics (Cont'd)

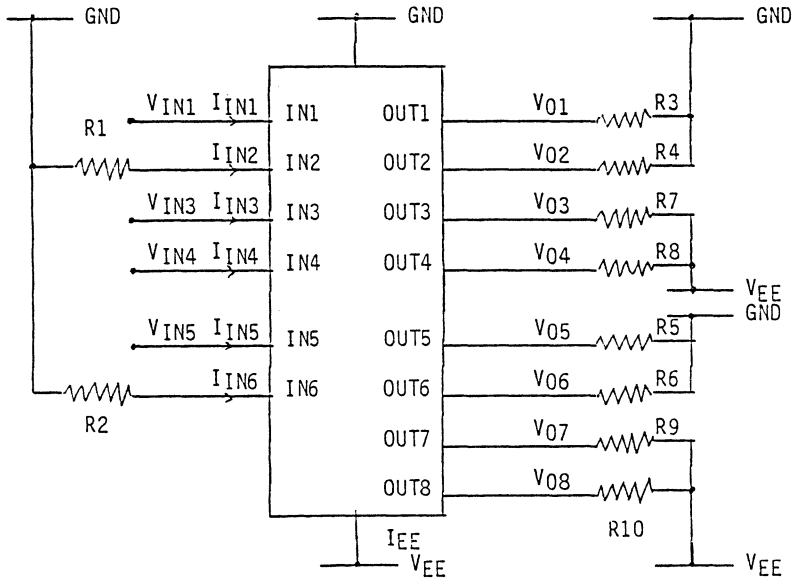
(Deviation : ±2%)

Parameter	Conditions	Symbol	Value at T_A=25±2°C			Value at T_A=0 to 70°C			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Current	R=430Ω±2%	I_{IN2}, I_{IN6}		10.1		8.5		12.1	mA
Supply Current	$V_{IN1}=V_{IN5}=V_{Hmax}$, $V_{IN3}=V_{Hmax}$, $V_{IN4}=V_{Lmax}$	I_{EE}		72				110	mA

AC Characteristics

(Deviation : ±2%)

Parameter	Conditions	Symbol	Value at T_A=25±2°C			Value at T_A=0 to 70°C			Unit
			Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time	$V_{IN1}=V_{IN5}=V_{Lmax}$, V_{IN3}=-1.29V, $V_{IN4}=V_{INA}$, Output Timing : V_{O2},V_{O4},V_{O6},V_{O8} as V_{OUTC}. V_{O1},V_{O3},V_{O5},V_{O7} as V_{OUTC}.	t_{d1}						12	ns
		t_{d2}						12	ns
		t_{d3}						12	ns
		t_{d4}						12	ns
Rise Time		t_{r1}						8	ns
		t_{r2}						8	ns
Fall Time		t_{f1}						8	ns
		t_{f2}						8	ns

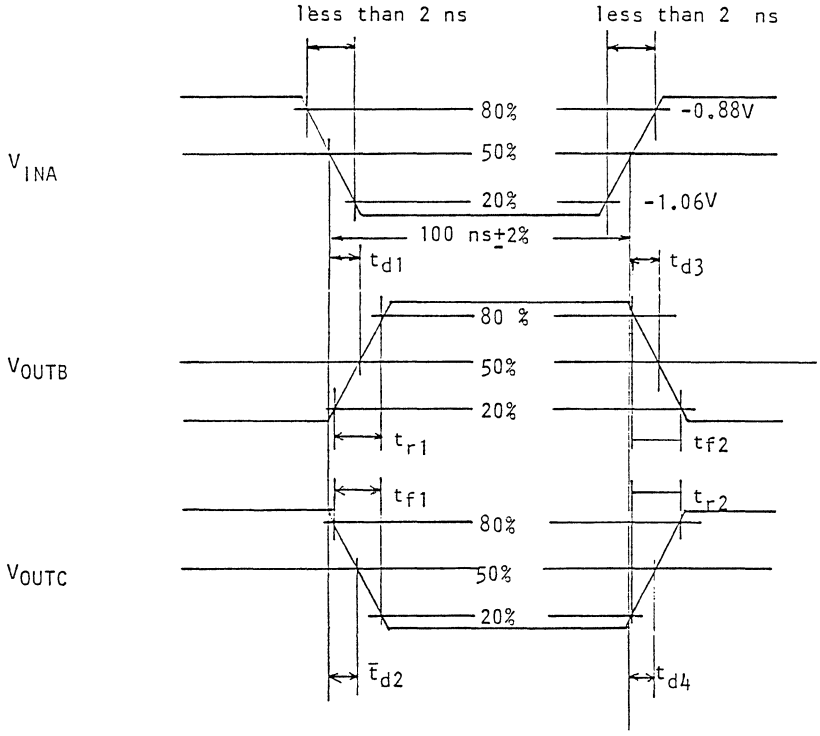


NOTE : R1, R2 : 430 Ω ±2%
R3 thru R6 : 51 Ω ±2%
R7 thru R10 : 1 kΩ ±2%

Test Temperature T_A (°C)	Test Voltage				
	V_{Hmax} (V)	V_{Hmin} (V)	V_{Lmax} (V)	V_{Lmin} (V)	V_{TH}(V)
0	-0.86	-1.155	-1.49	-1.87	-1.32
25	-0.81	-1.105	-1.475	-1.85	-1.29
70	-0.7	-1.035	-1.44	-1.825	-1.22

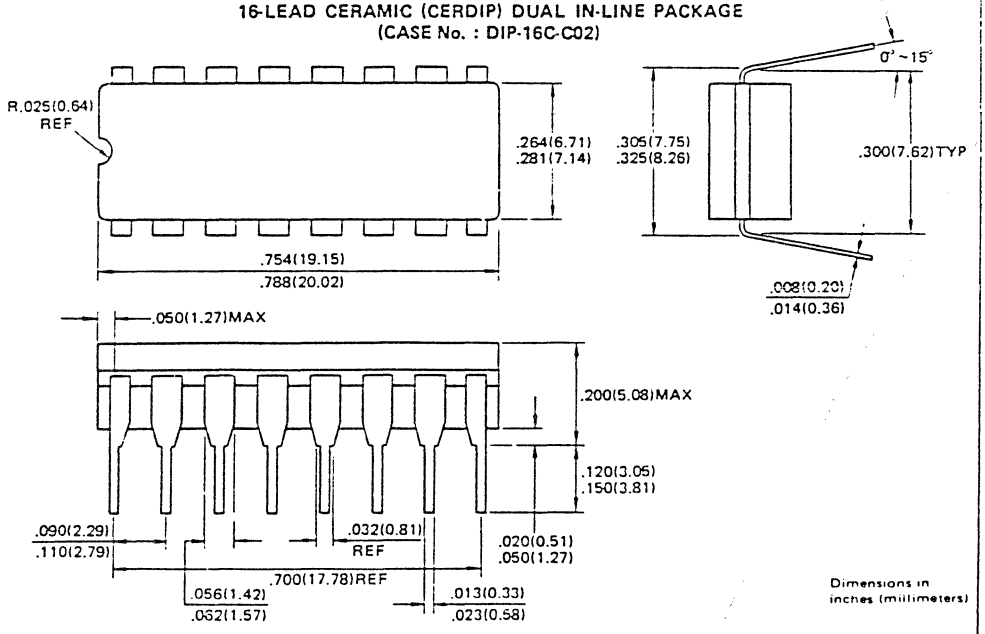
6

TIMING CHART



6

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)



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DSTV84-059

FUJITSU

DSTV83-065
August 1983

MB4316

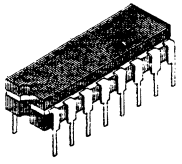
DRIVER/RECEIVER FOR DISK HEAD AMP.

The Fujitsu MB4316 is designed for the MB4111/MB4112 Disk Head Amplifier's Driver/Receiver.

Features

- Data inputs and Control inputs are CML level inputs.
- On-chip Write Current Source which is adjustable by changing an external resister.

Package



CERAMIC PACKAGE
DIP-16C-C02

Maxium Ratings

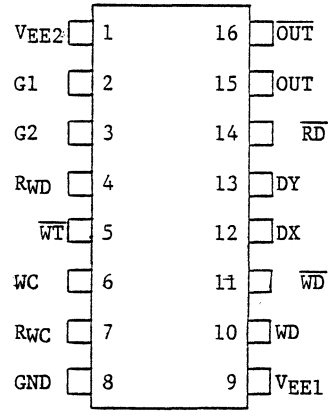
Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE1}	-7.0 - 0	V
	V_{EE2}	-15.0 - 0	V
Output terminal voltage	V_{CC}	0 - 9.0	V
Input voltage	V_{IN}	-5.0 - 0	V
Write Current	I_{WG}	0 - 60	mA
Power Dissipation	P_D	580	mW
Operating Temperature	Ta	0 - 70	°C
Storage Temperature	Tstg	-55 - 150	°C

6

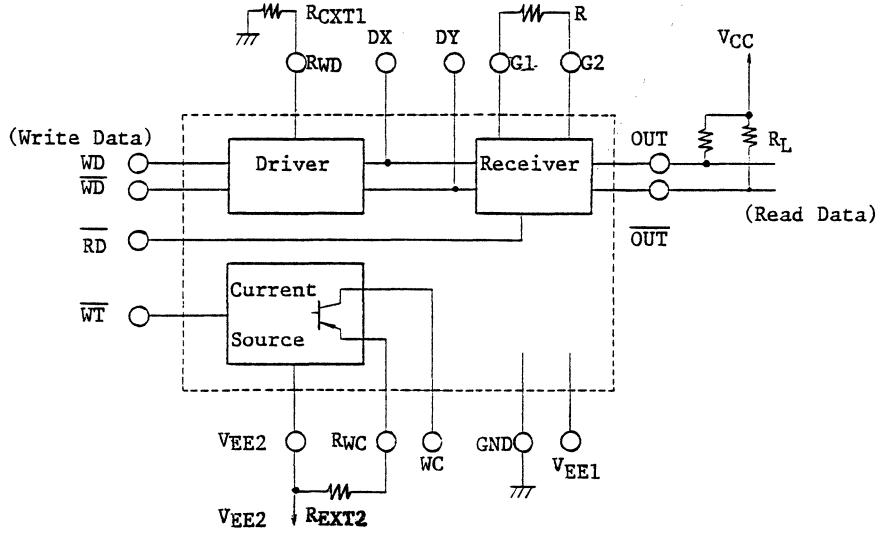
Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{EE1}	-5.2±5%	V
	V_{EE2}	-12.0±5%	V
Output Terminal Voltage	V_{CC}	6.0±5%	V
External Resistance	R_{EXT1}	700±2%	Ω

Pin Assignments



Block Diagram



Pin Function Table

Pin No.	Symbol	Functions
1	V_{EE2}	Power Supply (-12 V)
2	G1	Gain of output Amplifier (Receiver) is specified with an External resister between G1 and G2.
3	G2	
4	R_{WD}	This input specifies Data level in write mode.
5	$\overline{WT}$	WC switch. When it is at CML low level, WC is active.
6	WC	Write Current Source Output
7	R_{WC}	Write Current is specified with resister between R_{WC} and V_{EE2} (See Block Diagram) ($I_{WC} \fallingdotseq 5.4V/R_{EXT2}$)
8	GND	Ground
9	V_{EE1}	Power Supply (-5.2V)
10	WD	Write Data, driven by complementary signal of CML level
11	$\overline{WD}$	
12	DX	Data Bus
13	DY	
14	$\overline{RD}$	Read/Write mode Switch. When it is at CML low level, read mode is selected, and at high level, write mode is selected
15	OUT	Output for read data
16	$\overline{OUT}$	

Electrical Characteristics

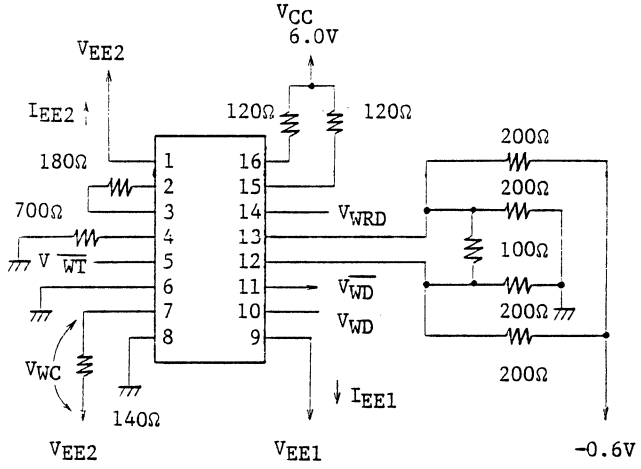
(V_{EE1}=-5.2V.V_{EE2}=-12.0V.Ta=25°C)

Parameters	Symbol	Conditions	Measure-ment Diagram	MIN	TYP	MAX	Unit
Power supply Current	I_{EE1}	V_{EE1}=-5.46V.V_{EE2}=-12.6V	1	-	-	65	mA
	I_{EE2R}		1	-	-	15	mA
	I_{EE2W}		1	-	-	10	mA
Input Current	$I_{I\overline{RD}}$	V_{EE1}=-5.46V, V_{EE2}=-12.6V, $V_{\overline{RD}}$=-0.81V.V $\overline{WT}$=-1.71V	1	-	-	0.2	mA
	I_{IWD}	V_{WD}=-0.81V	1	-	-	0.9	mA
	$I_{I\overline{WD}}$	$V_{\overline{WD}}$=-0.81V	1	-	-	0.9	mA
	$I_{I\overline{WT}}$	$V_{\overline{RD}}$=-1.71.$V_{\overline{WT}}$=-0.81V	1	-	-	0.15	mA
Output Voltage	V_{WC}	$V_{\overline{RD}}$=-0.89V, $V_{\overline{WT}}$=-1.75V	1	4.9	5.4	5.9	V
	V_{DXH}	$V_{\overline{RD}}$=-0.96V, $V_{\overline{WT}}$=-1.65V, $V_{\overline{WD}}$=-0.96V	1	-0.59	-	-0.45	V
	V_{DXL}	V_{WD}=-0.96V	1	-0.75	-	-0.61	V
	V_{DYH}		1	-0.59	-	-0.45	V
	V_{DYL}	$V_{\overline{WD}}$=-0.96V	1	-0.75	-	-0.61	V
DxDy Differencial Output Voltage	$\|V_{XY}\|$	$\|V_{DX}-V_{DY}\|$	1	160	-	-	mV
Voltage Gain	A_V	V_I=100mVpp, f=5MHz	2	0.95	1.1	1.25	V/V
Band Width	BW		2	30	-	-	MHz
Delay Time	t_{PLH1}	$\overline{WT}$ → RWC	3	-	-	350	ns
	t_{PML1}		3	-	-	100	ns
	t_{PLH2}	$\overline{RD}$ → DX, DY	4	-	-	200	ns
	t_{PHL2}		4	-	-	100	ns

6

Measurement Diagram

1.



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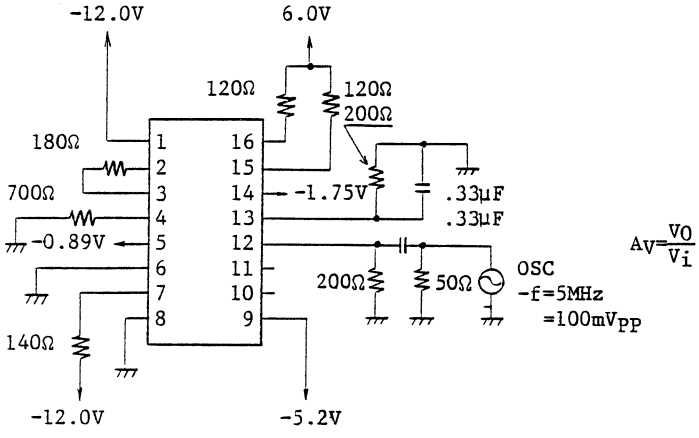

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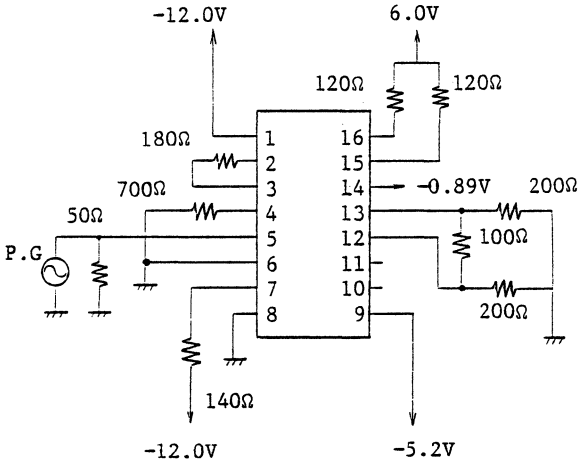
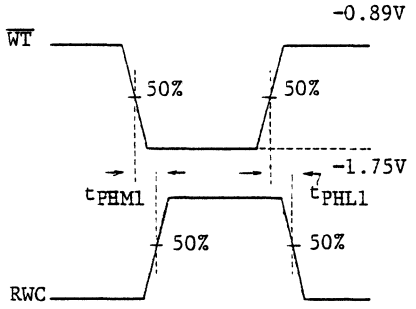
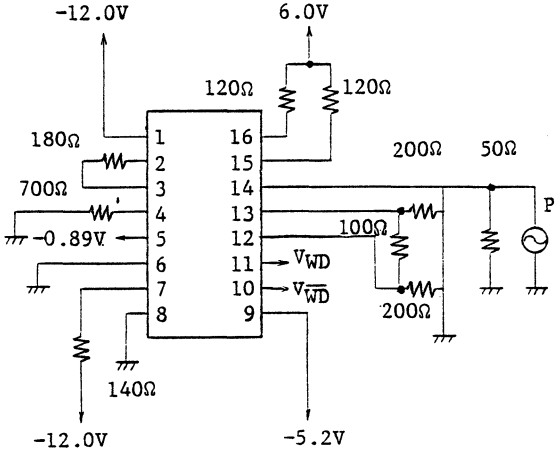
3.





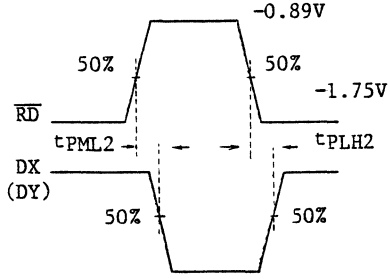
Input :
P.R.R. : 1.5 MHz
tr=tf=10 ns

4.



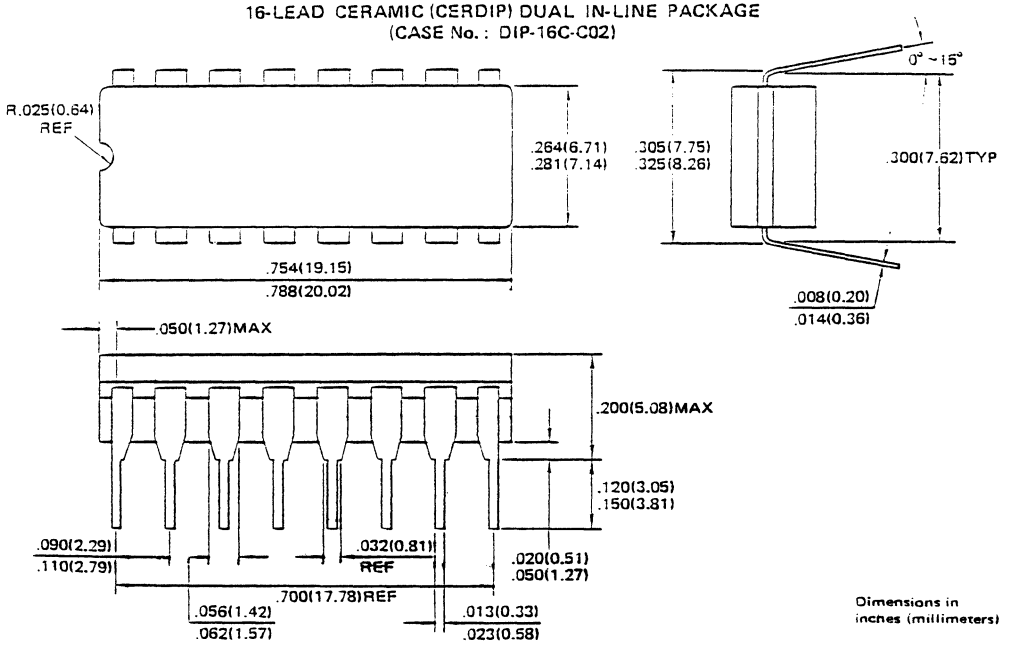
Output	Bias	
	V_{WD}	$V_{\overline{WD}}$
DX	-0.89V	-1.75V
DY	-1.75V	-0.89V

Input ;
P.R.R.:1.5 MHz
tr=tf=10 ns.



Package Dimensions

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)



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DSTV83-065
MB4316

FUJITSU

FUJITSU MICROELECTRONICS, INC.

MB4319

Product Profile

Peakhold IC

The MB4319 is designed to generate the head position signal for head control in magnetic disk unit as illustrated below. (See Fig. 1.)

The MB4319 detects the peak of the servo signals read out from the servo disk via the carrier amplifier and makes its discharge continuously proportional to the head velocity. (See Fig. 2.)

Fig. 1 — THE MB4319 DISK DRIVE APPLICATION

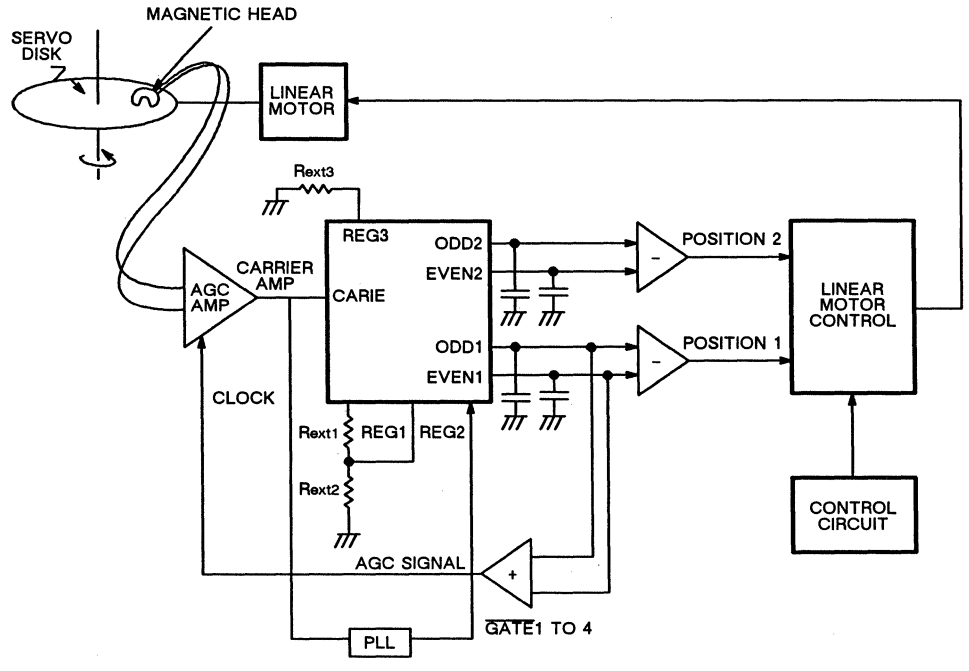


Fig. 2 — TIMING DIAGRAM

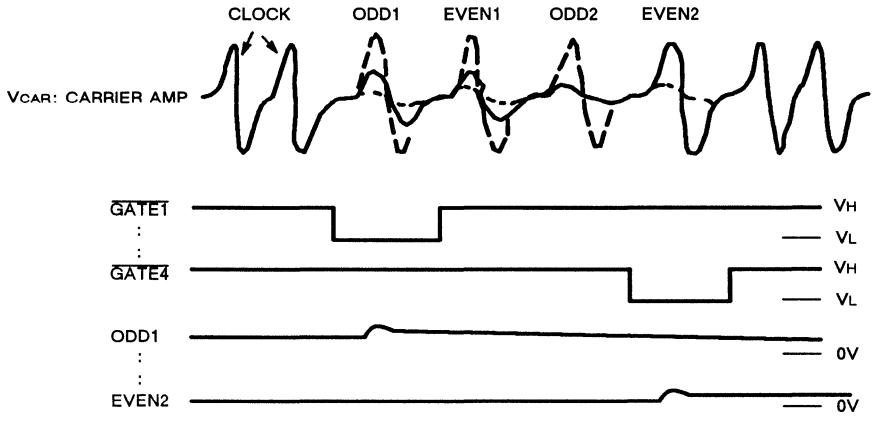
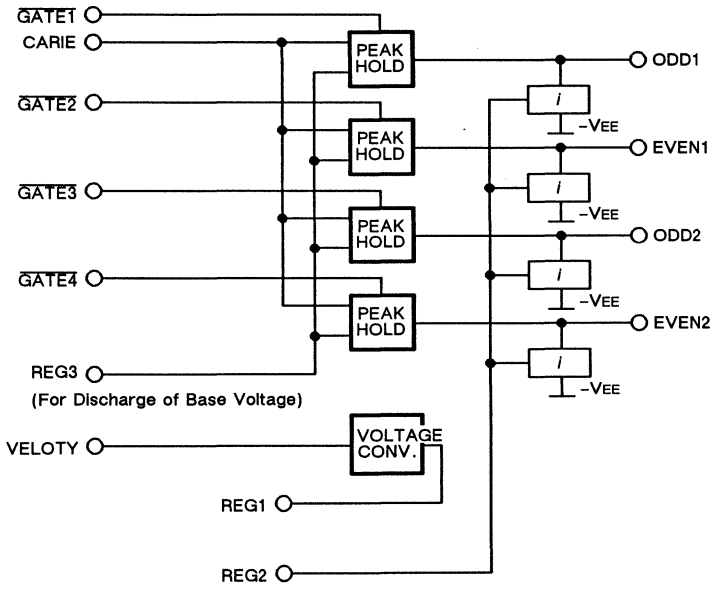


Fig. 3 — BLOCK DIAGRAM



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The Detail of the Operation of MB4319

The MB4319 detects each peak of the high frequency signal and selects the discharge constants externally. The MB4319 comprises four peak-hold circuits in order to control each discharge constant equally.

Sampled signal CARIE, is illustrated in Fig. 5 and has a peak-to-peak value of 9V Max. Gate signals are negative logic and have a 270ns window for positive peak. When Gate is closed, the falling constant α is determined by the function of VELOTY, R_{ext1}, and R_{ext2}. VELOTY is the negative voltage proportional to the velocity of the head, and its range is 0V through -6.0V.

Example: Charge rising constant : 10V/μs
Discharge falling constant : -0.13V/μs at Vv = 0V
: -0.5V/μs at Vv = -5.5V
Condition : C_{ext} = 680pF

As shown in Figure 1, the ODD and EVEN outputs should be buffered from the following stages by high impedance input amplifiers.

Fig. 4 — EQUIVALENT CIRCUIT

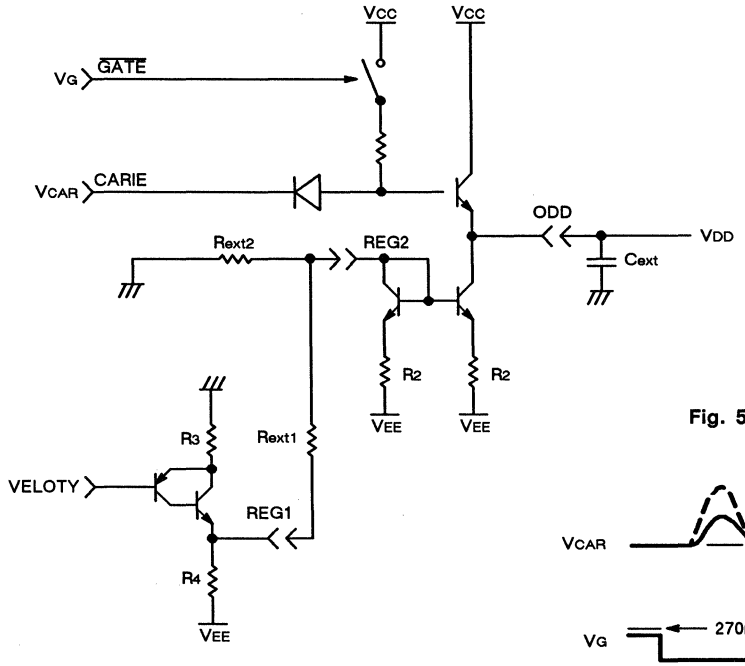
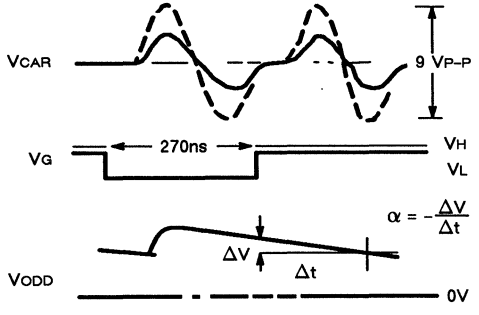
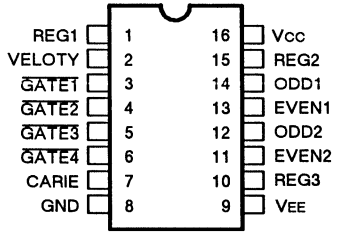


Fig. 5 — TIMING DIAGRAM



PIN ASSIGNMENT
(TOP VIEW)



Absolute Maximum Ratings (TA = 25°C, unless otherwise noted.)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	+15	V
Supply Voltage	V_{EE}	-15	V
Power Dissipation	P_D	580	mW
Operating Temperature	T_{OP}	0 thru 70	°C
Storage Temperature	T_{STG}	-55 thru +150	°C
Input Voltage at CARIE	V_{CAR}	-5.5 thru +5.5	V
Input Voltage at $\overline{GATEn}$	V_G	-0.5 thru +5.5	V
Input Voltage at VELOTY	V_V	V_{EE} thru +3.0	V
Input Current at REG2	I_{REG2}	1	mA
Input Current at REG3	I_{REG3}	5	mA
Output Load Current at ODD1/2 & EVEN1/2	I_{LOAD}	10	mA
Output Load Current at REG1	I_{REG1}	1	mA

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Operating Conditions (TA = 0°C thru +70°C, unless otherwise noted.)

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Supply Voltage	V_{CC}	11.4	12.0	12.6	V	
Supply Voltage	V_{EE}	-12.6	-12.0	-11.4	V	
Input Voltage at CARIE	V_{CAR}	-4.5	—	+4.5	V	
High-level Input Voltage at GATEn	V_{GH}	2.0	—	—	V	
Low-level Input Voltage at GATEn	V_{GL}	—	—	0.8	V	
Input Voltage at VELOTY	V_V	-5.5	—	+0.5	V	Rext1 = 22kΩ
Input Current at REG2	I_{REG2}	—	—	0.4	mA	
Input Current at REG3	I_{REG3}	—	—	2.5	mA	
Output Current at ODD1/2 & EVEN1/2	I_{LOAD}	—	—	1	µA	See Note
Output Current at REG1	I_{REG1}	—	—	0.3	mA	V_V = -5.5V, Rext1 = 22kΩ

Note: I_{LOAD} is defined as illustrated below.

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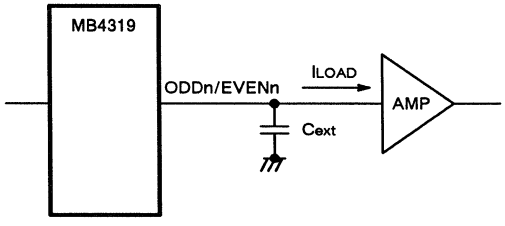

Electrical Characteristics

DC CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = −12V, Tolerance: ±2%, unless otherwise noted.)

(V_{CC} = +12V ±5%, V_{EE} = −12V ±5% when T_A = 0°C thru 70°C as a condition.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Gate High Input Current	I_{G1H}, I_{G2H}, I_{G3H}, I_{G4H}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0V, T_A = 0°C thru 70°C, see Fig. 1.	—	—	100	µA
Gate Low Input Current	I_{G1L}, I_{G2L}, I_{G3L}, I_{G4L}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V, T_A = 25 ±2°C, see Fig. 1.	−1.8	−1.2	−0.6	mA
CARIE Input Current	I_{CAR}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0V, T_A = 0°C thru 70°C, V_{CAR} = +4.0V, see Fig. 1.	—	—	100	mA
CARIE Input Current	I_{CAR}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0V, T_A = 25 ±2°C, V_{CAR} = −0.4V, see Fig. 1.	−2.4	−1.5	−1.0	mA
CARIE Input Current	I_{CAR}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V, T_A = 25 ±2°C, V_{CAR} = +4.0V, see Fig. 1.	−2.9	−2.0	−1.4	mA
CARIE Input Current	I_{CAR}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V, T_A = 25 ±2°C, V_{CAR} = −4.0V, see Fig. 1.	−7.1	−5.1	−3.9	mA
REG2 Input Voltage	ΔV_{REG2}	I_{REG2} = 45µA, see Fig. 2.	0.72	0.86	1.0	V
REG3 Input Voltage	ΔV_{REG3}	I_{REG3} = 1.0mA, see Fig. 2.	1.0	1.5	2.1	V
VELOTY Input Current	I_{VEL}	V_{VEL} = −4.0V, see Fig. 1.	—	0.5	13	µA
REG1 Output Voltage	V_{REG1}	V_{VEL} = 0V, see Fig. 1.	—	—	−11.4	V
REG1 Output Voltage	V_{REG1}	V_{VEL} = −4.0V, see Fig. 1.	−8.0	−6.8	−5.5	V

Electrical Characteristics (Continued)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0V$, $T_A = 25 \pm 2°C$, see Fig. 3. $V_{CAR} = +4.0V$	-1.5	-1.2	-0.8	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0V$, $T_A = 25 \pm 2°C$, see Fig. 3. $V_{CAR} = +2.0V$	-1.5	-1.2	-0.8	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0V$, $T_A = 25 \pm 2°C$, see Fig. 3. $V_{CAR} = 0V$	-1.5	-1.2	-0.8	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0V$, $T_A = 25 \pm 2°C$, see Fig. 3. $V_{CAR} = -4.0V$	-1.5	-1.2	-0.8	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V$, $T_A = 25 \pm 2°C$, see Fig. 3. $V_{CAR} = +4.0V$	4.0	4.3	4.6	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V$, $T_A = 25 \pm 2°C$, see Fig. 3. $V_{CAR} = +2.0V$	2.0	2.3	2.6	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V$, $T_A = 25 \pm 2°C$, see Fig. 3. $V_{CAR} = 0V$	0	0.3	0.6	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V$, $T_A = 25 \pm 2°C$, see Fig. 3. $V_{CAR} = -4.0V$	-1.5	-1.2	-0.8	V
ODD1/2 EVEN1/2 Output Difference Voltage	ΔV_{OUT}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V$, $V_{CAR} = 2.0V$, $T_A = 25 \pm 2°C$ The max difference voltage in the measurement of ODD1/2 & EVEN1/2 Output Voltage, see Fig. 3.	—	—	0.1	V
ODD1/2 EVEN1/2	I_{OL1}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V$, $V_{ODD1} = V_{ODD2} = 2.0V$, $V_{EVEN1} = V_{EVEN2} = 2.0V$, $V_{CAR} = 0V$ $R_{ext1} = R_{ext2}$: Open $T_A = 25 \pm 2°C$, see Fig. 4.	-10	—	10	µA

Electrical Characteristics

AC CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = −12V, Tolerance: ±2%, unless otherwise noted.)

(V_{CC} = +12V ±5%, V_{EE} = −12V ±5% when T_A = 0°C thru 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Rising Time of V_{ODDn}/ $EVEN_n$ when V_{Gn} is ON	t_{rO1}, t_{rO2}, t_{rE1}, t_{rE2}	V_{CAR} = 4 ±0.1V, V_{VEL} = −4 ±0.1V, T_A = 25 +2°C, see Fig. 5.	—	350	500	ns
Rising Time of V_{ODDn}/ $EVEN_n$ when step input is input at V_{CAR}	t_{srO1}, t_{srO2}, t_{srE1}, t_{srE2}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.3V ±0.1V, V_{VEL} = −4 ±0.1V, T_A = 25 ±2°C see Fig. 5.	—	190	300	ns
Falling Time of V_{ODDn}/ $EVEN_n$	t_{fO1}, t_{fO2}, t_{fE1}, t_{fE2}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V, see Fig. 5, V_{VEL} = 0V	50	90	180	µs
Falling Time of V_{ODDn}/ $EVEN_n$	t_{fO1}, t_{fO2}, t_{fE1}, t_{fE2}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8V, see Fig. 5, V_{VEL} = −4 ±0.1V	7	12.5	25	µs
Channel Separation	ΔV_{sp}	Change of VEVEN1 when V_{CAR} = +4.0V, V_{G2} = 0.3V, and V_{G1}, V_{G3}, and V_{G4} are changed from 2.0V to 0.3V at the same time. See Fig. 5.	—	—	0.2	V

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Fig. 1

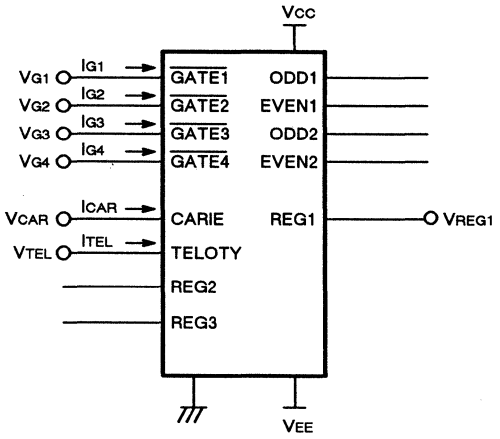


Fig. 2

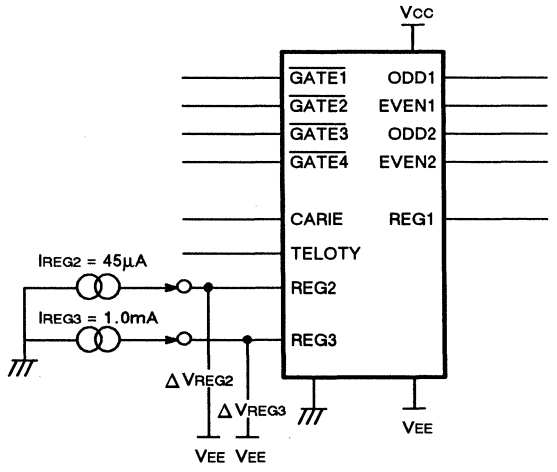


Fig. 3

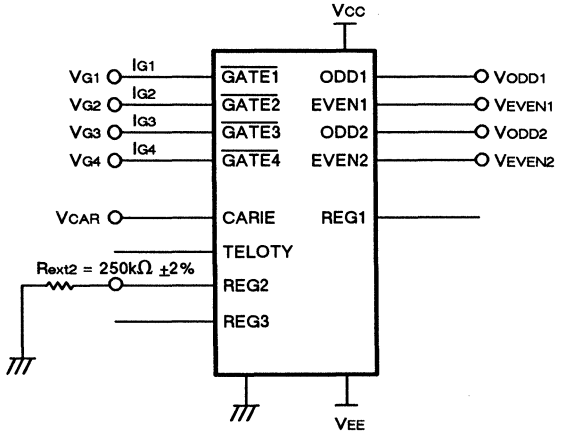


Fig. 4

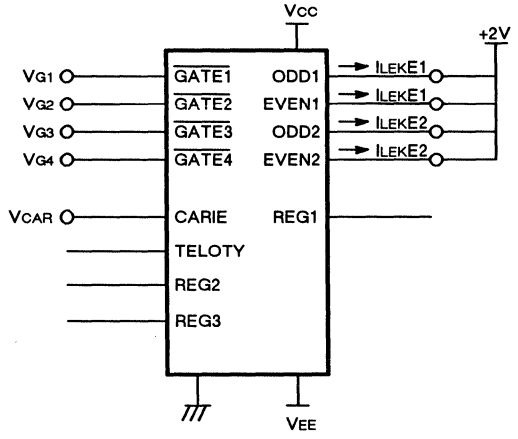
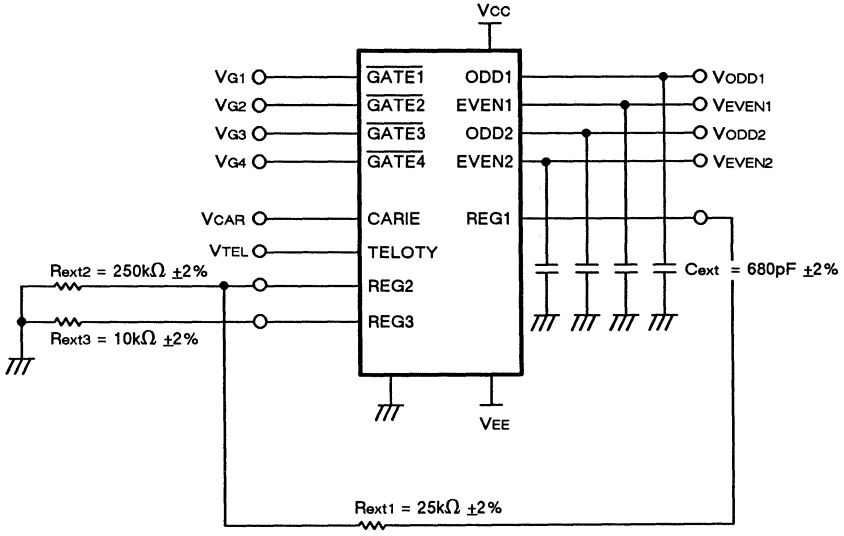
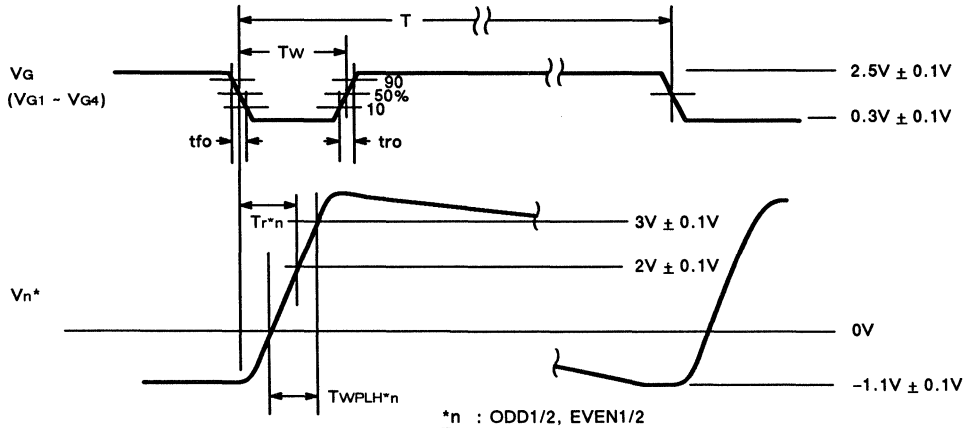

VCC
+2V
VG1
VG2
VG3
VG4
GATE1
GATE2
GATE3
GATE4
ODD1
EVEN1
ODD2
EVEN2
ILEKE1
ILEKE1
ILEKE2
ILEKE2
VCAR
CARIE
REG1
TELOTY
REG2
REG3
VEE

Fig. 5


VCC
VG1
VG2
VG3
VG4
GATE1
GATE2
GATE3
GATE4
ODD1
EVEN1
ODD2
EVEN2
VODD1
VEVEN1
VODD2
VEVEN2
VCAR
CARIE
REG1
VTEL
TELOTY
Rext2 = 250kΩ ±2%
REG2
REG3
Rext3 = 10kΩ ±2%
Cext = 680pF ±2%
VEE
Rext1 = 25kΩ ±2%

6

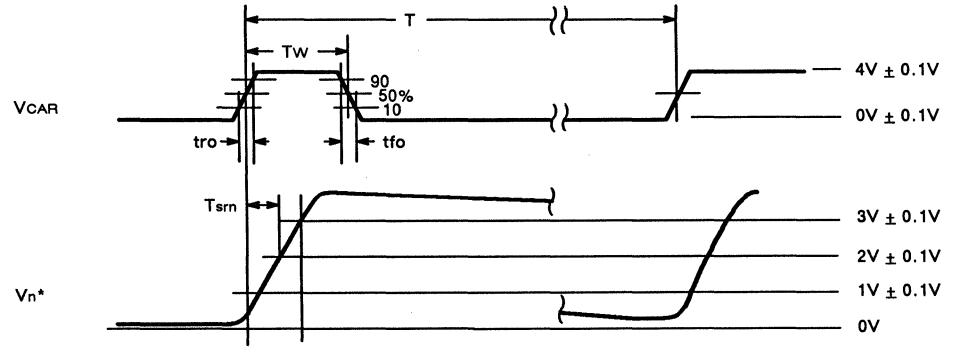
TIME CHART 1.



*n : ODD1/2, EVEN1/2
TW = 500ns ± 10ns
tfo = tro ≤ 10ns
T ≥ 220µs

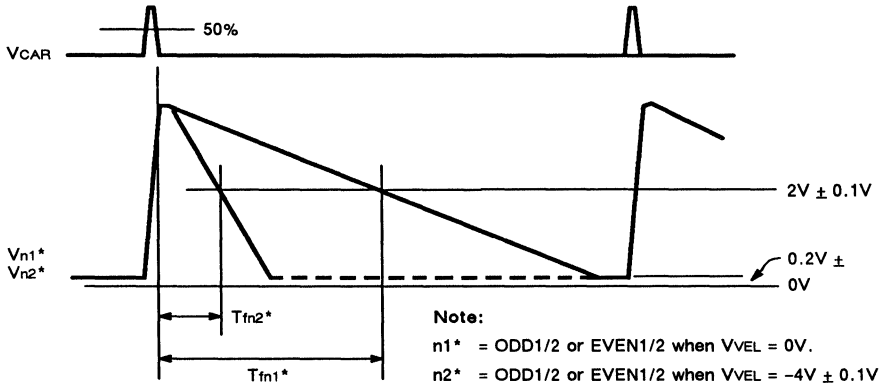
6

TIME CHART 2.



*n : ODD1/2, EVEN1/2
TW = 500ns ± 10ns
tfo = tro ≤ 10ns
T ≥ 220µs

TIME CHART 3.



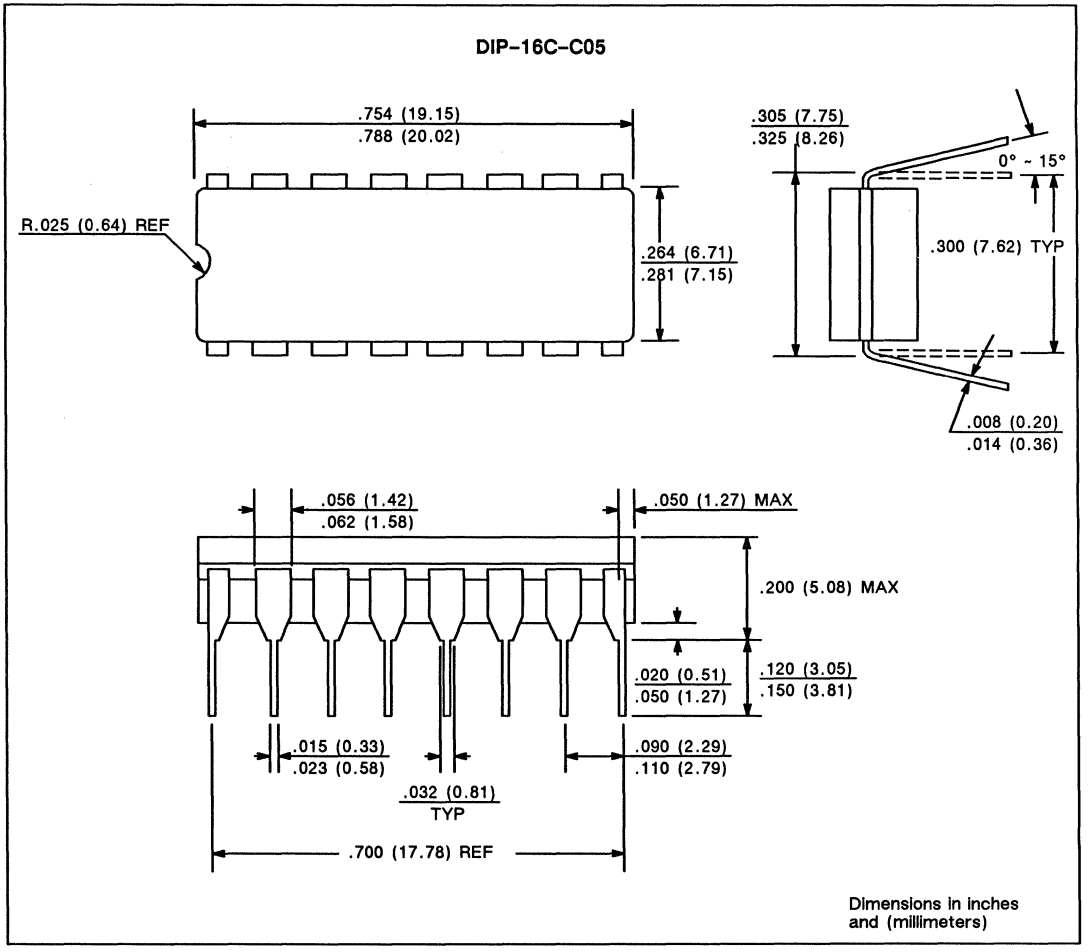
Note:

n1* = ODD1/2 or EVEN1/2 when VVEL = 0V.

n2* = ODD1/2 or EVEN1/2 when VVEL = −4V ± 0.1V

VCAR: As same as Time Chart 2.

6


DIP-16C-C05
.754 (19.15)
.788 (20.02)
R.025 (0.64) REF
.264 (6.71)
.281 (7.15)
.305 (7.75)
.325 (8.26)
0° ~ 15°
.300 (7.62) TYP
.008 (0.20)
.014 (0.36)
.056 (1.42)
.062 (1.58)
.050 (1.27) MAX
.200 (5.08) MAX
.020 (0.51)
.050 (1.27)
.120 (3.05)
.150 (3.81)
.015 (0.33)
.023 (0.58)
.090 (2.29)
.110 (2.79)
.032 (0.81)
TYP
.700 (17.78) REF
Dimensions in inches
and (millimeters)

6

Section 7

Data Conversion

Fujitsu Part No.	Description	Features	Equiv. Prod.	Power Supply (V)	Package	No. of Pins
A/D Converters						
MB4051	8 Ch, 10-bit	100µs/Ch, SAR	—	+5V, +8V, -8V	Plastic DIP	42
MB4052	4 Ch, 8-bit	100µs/Ch,	—	+5V +12V	Ceramic DIP Plastic DIP Plastic Flatpak	16 16 16
MB4053	6 Ch, 8-bit	300µs/Ch,	—	+5V +2V (ref)	Ceramic DIP Plastic DIP Plastic Flatpak	16 16 16
MB4056	8 Ch, 8-bit	100µs/Ch, SAR	—	+12V	Ceramic DIP Plastic DIP	20 20
MB4063	6 Ch, 8-bit	300µs/Ch	—	+5V +2.8V (ref)	Ceramic DIP Plastic DIP Plastic Flatpak	16 16 16
MB40547 -7	1 Ch, 8 bit	Flash Conv, 30Msps	—	-5.2V	Ceramic DIP	24
MB40547 -8	1 Ch, 8 bit	Flash Conv, 30Msps	—	-5.2V	Ceramic DIP	24
MB40576	1 Ch, 8 bit	Flash Conv, 30Msps	—	+5V	Plastic DIP Plastic Flatpak	16 16
MB40578	1 Ch, 8 bit	Flash Conv, 30Msps, 0.2%	—	+5V	Plastic DIP	22
MB40578-7	1 Ch, 8 bit	Flash Conv, 30Msps, 0.4%	—	+5V	Plastic DIP	22
D/A Converters						
MB4072	1 Ch, 8-bit	OC O/P, 85µs	—	+4.5V, +18V	Ceramic DIP Plastic DIP Plastic Flatpak	16 16 16
MB40748 -8	1 Ch, 10 bit	ECL I/O, 30Msps 0.2%	—	-5.2V	Ceramic DIP	24
MB40748 -9	1 Ch, 10 bit	ECL I/O, 30Msps 0.1%	—	-5.2V	Ceramic DIP	24
MB40776	1 Ch, 6 bit	TTL I/O, 30Msps	—	+5V	Plastic DIP Plastic Flatpak	16 16
MB40778	1 Ch, 8-bit	TTL I/O, 30Msps	—	+5V	Plastic DIP	18
MB40788	1 Ch, 10-bit	ECL I/O, 125Msps	—	-5.2V	Ceramic DIP	24
MB40874	1 Ch, 4 bit	TTL I/O, RAM, 50Msps	—	+5V	Ceramic DIP Plastic DIP	20 20
MB40978	3 Ch, 8 bit	TTL I/O, 60Msps	—	+5V +4V (ref)	Plastic DIP Plastic Flatpak	42 44
MB88301A	3 Ch, 6-bit, 6 Ch, 13-bit	Multipurpose	—	+5V	Plastic DIP Plastic Flatpak	16 16
A/D-D/A Converters						
MB40176	1 Ch, 6 bit	Flash A/D & D/A, 30Msps	—	+5V	Plastic DIP Flatpak	28 28
MB87020	1 Ch, 16 bit	SW Cap A/D & DA, 50Ksps	—	±5V	Plastic DIP	40

May 1988
Edition 1.0

FUJITSU

FUJITSU MICROELECTRONICS, INC.

MB4051
Product Profile

8-CH 10-Bit A/D Converter (ADC)

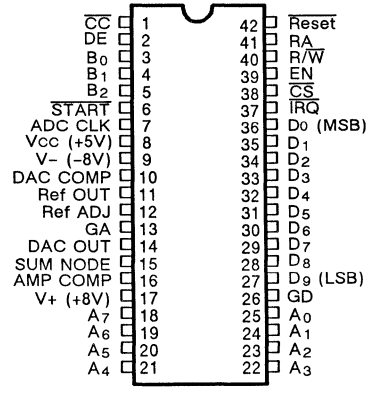
The Fujitsu MB4051 is a general purpose analog-to-digital converter (ADC) which features eight channels of analog inputs, 10-bit parallel data I/O port and programmable control register. Analog input signal on a selected input channel is converted to 10-bit digital data by the successive-approximation technique which provides high-speed conversion. The MB4051 is packaged in a standard 42-pin dual in-line package.

Features

- Multiplex 8-channel Analog Inputs
- Resolution: 10 bits
- Relative Accuracy: 8 bits Min.
- Linearity: ±1/2 LSB
- Successive-Approximation Technique: 25μs/ch Min.
- Analog Input Voltage Range: 0V ~ 6.5V
- Input Impedance: over 500kΩ(for 6.5V Input)
- Built-in High Stabilized Reference Voltage Source
- Directly Connectable to DMA Controller as well as Microprocessor
- TTL Compatible Digital I/O Port
- Standard 42-pin DIP
- Power Supplies: +5V and ±8V
- Power Consumption: 400mW (Typ.)

PIN ASSIGNMENTS

(TOP VIEW)



DIP42

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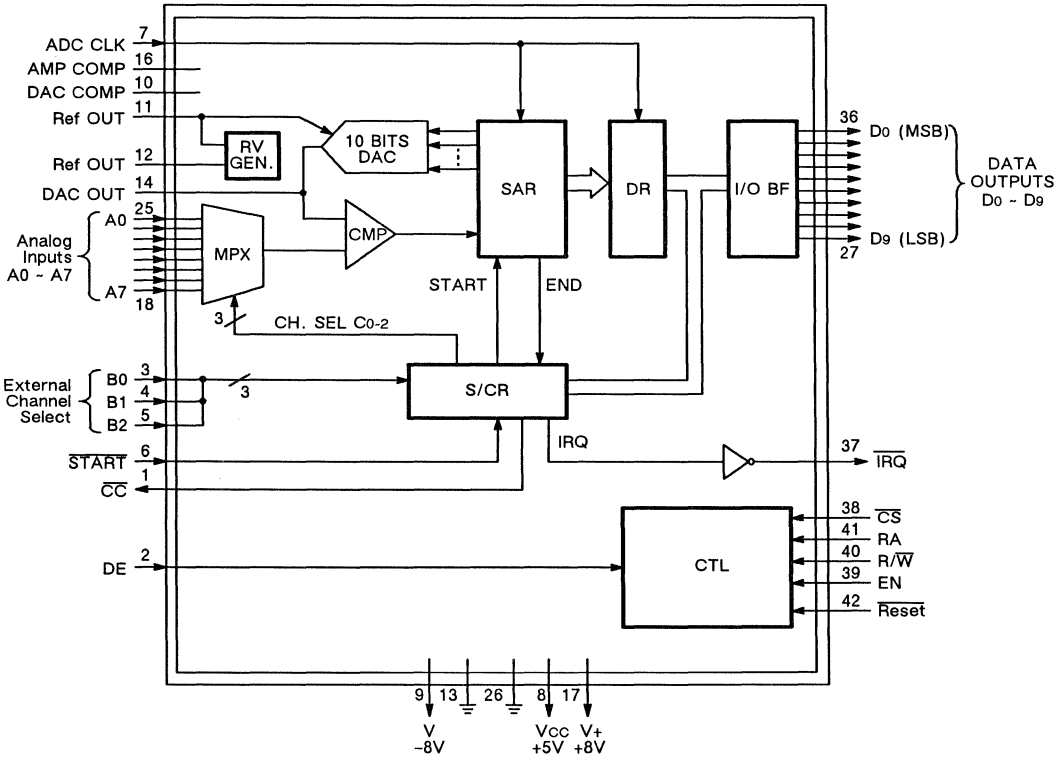
Fig. 1 — MB4051 BLOCK DIAGRAM



Functional Block Descriptions

Symbol	Name	Function
MPX	Multiplexer	Selects one channel from 8-channel analog input signals. Channel assignment is done by the 2nd thru 4th bits of control register which are programmed by the external channel select inputs B_0 thru B_2 or by a data from MPU.
CMP	Comparator	Compares an unknown analog input signal with an output signal of built-in DA converter. The result of comparison is transferred to the successive-approximation register (SAR).
DAC	DA Converter	10-bit digital-to-analog converter. Generates analog signal corresponding to digital signal specified by the SAR.
SAR	Successive-Approximation Register	According to the result from the comparator, generates the next step digital output to be transferred to the DAC and compared in the comparator. Composed of 10-bit register and control logic. After completion of data-conversion, acts as the data register (DR).
SR	Status Register	10-bit register which indicates the status of operations. Indicates the assigned channel by SR-2~4, status of the external control/MPU by SR-5, operation of AD conversion by SR-6 and completion of AD conversion by SR-7. (See Tables 1 and 2)
CR	Control Register	10-bit register which controls the operation of ADC. Assigns a channel by CR-2~4, switches MPU/external control each other by CR-5; initiates AD conversion by CR-6. (See Tables 1 and 2)
DR	Data Register	Stores a 10-bit data at the completion of AD conversion. Outputs the data at DE = 1 during the external control mode (CR-5 = 0). If the DR is selected ($\overline{CS}$ = 0, RA = 0, and R/$\overline{W}$ = 1) during the MPU control mode (CR-5 = 1), the contents can be read by MPU (EN = 1).
I/O BF	Input/Output Buffer	Connected to the data-bus of MPU for sending or receiving the 10-bit data. The output is three-state TTL compatible.
CTL	Control Logic	Controls sending and receiving of data between blocks and is used for initializing.
Ref	Reference Voltage Regulator	Specified the maximum analog input signal level of ADC.

Pin Descriptions

Symbol	Name	Function
A_0-A_7	Analog Input	Analog input terminals of 8 channels one of which is assigned by CR-2-4.
D_0-D_9 (D_0..MSB D_9..LSB)	Data I/O Port	Connected to 10-bit parallel data-bus for transferring 10-bit data between internal registers and MPU.
$\overline{CS}$	Chip Select	Chip-select terminal of ADC which is selected at $\overline{CS}$ = 0.
RA	Register Address	Address input for the internal registers. Selects the data register (DR) at RA = 0 and the control register (CR)/status register (SR) at RA = 1.
R/$\overline{W}$	Read-Write Control	Input for the read-write signal from MPU (MPU read mode at R/$\overline{W}$ = 1).
EN	Enable Signal	Input for the enable signal of MPU system. EN is used as timing for data transfer between MPU and ADC.
$\overline{Reset}$	Reset	Initializes the ADC at $\overline{Reset}$ = 0.
B_0-B_2	External Channel Select Input	When ADC is controlled externally (CR-5 = 0), the inputs from B_0-B_2 are set in CR-2-4 at the falling edge of $\overline{START}$. (See Table 3.)
$\overline{START}$	Start	AD conversion starts at the rising edge of START when the external control mode (CR-5 = 0).
$\overline{CC}$/ $\overline{IRQ}$ (Open Collector)	Conversion Complete/Interrupt Request	Indicates the completion of data conversion. After completion of data conversion, $\overline{CC}$ goes low at the external control mode (CR-5 = 0) or $\overline{IRQ}$ goes low at the MPU control mode (CR-5 = 1). In both cases, they go high after the content of the data register is read.
DE	Data Enable	During DE = 1 at the external control mode, the data in a register assigned by RA are output on D_0-D_9.
ADC CLK	AD Conversion Clock	Clock for AD conversion which is input to the SAR and determines the conversion speed of ADC. A data conversion is completed by 12 cycles of clock. Not required to synchronize with the EN (Enable) signal from MPU system. Minimum cycle time of this clock is 2μs.
Ref OUT/ Ref ADJ	Reference Output/ Reference Adjustment	Terminals for output of reference voltage which specified the full-scale value of analog input signal and for its adjustment.
AMP COMP/ DAC COMP/ DAC OUT/ SUM NODE	Amplifier Compensation/ DAC Compensation/ DAC Output/ Sum Node	Terminals for frequency adjustment of the internal operational amplifier with connected capacitors having specified capacitances. SUM NODE is also used for offset adjustment.
V^+/Vcc/V^-	Terminals for Power Supply	To be supplied +8V, +5V, and -8V, respectively.
GA/GD	Analog Ground/ Digital Ground	Terminals for ground.

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Table 1: BIT CONSTRUCTION OF DR AND S/C R

	RA	R/$\overline{W}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9
DR	0	1 Read	Bit 0 (MSB)	Bit 1	Bit 2	Bit3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9 (LSB)
S/C R	1	1 Read	—	—	Input CH. Select			Mode Control	Busy	IRQ	—	—
		0 Write			C_0	C_1	C_2	INT/EXT	Start	—		

Table 2: CHANNEL SELECT FOR MPU CONTROL

C_2	C_1	C_0	Selected Channel
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

Table 3: CHANNEL SELECT FOR EXTERNAL CONTROL

B_2	B_1	B_0	Selected Channel
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

ADC Operation Modes

According to the status of 5th bit (CR-5) in the built-in control register, ADC has two operation modes: external control mode and MPU control mode.

Just after an initialization ($\overline{\text{Reset}}$ going from low to high), ADC is in the external control mode (designation of channel, start of data conversion and data output are controlled through the external control input terminals). This mode is useful for ADC applications only or for DMA operation independent of MPU.

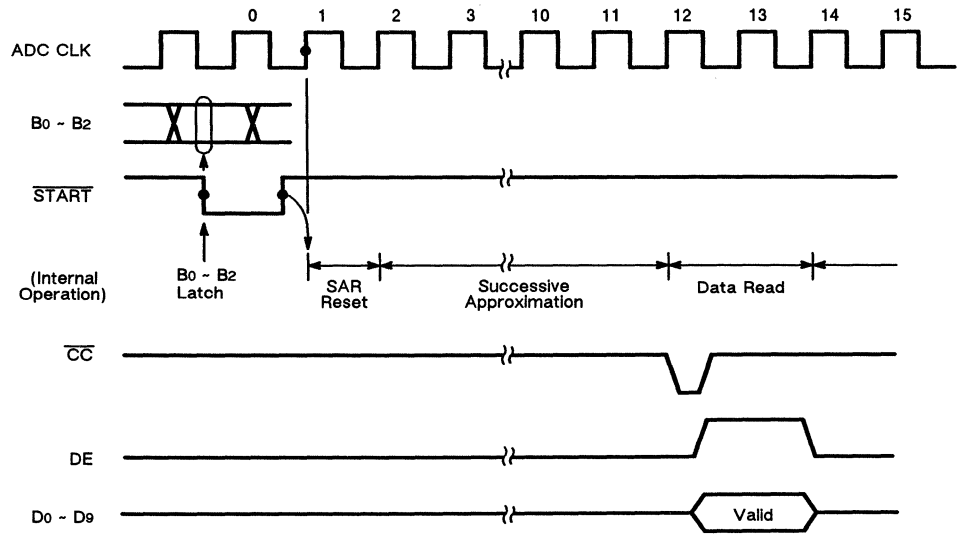
When the MPU control mode is required, set CR-5 of the control register high through MPU.

External Control Mode (CR-5 = 0):

This mode is used when ADC is controlled by the external hardware. An analog input signal channel is designated by B_0-B_2 and the AD conversion starts at the second rising edge of ADC clock after $\overline{\text{START}}$ goes low.

At the completion of 10-bit data conversion, $\overline{\text{CC}}$ (Convert Complete) goes low to notify external devices. The converted data is read after the low state of $\overline{\text{CC}}$ is confirmed and DE goes high.

ADC TIMING FOR EXTERNAL CONTROL MODE



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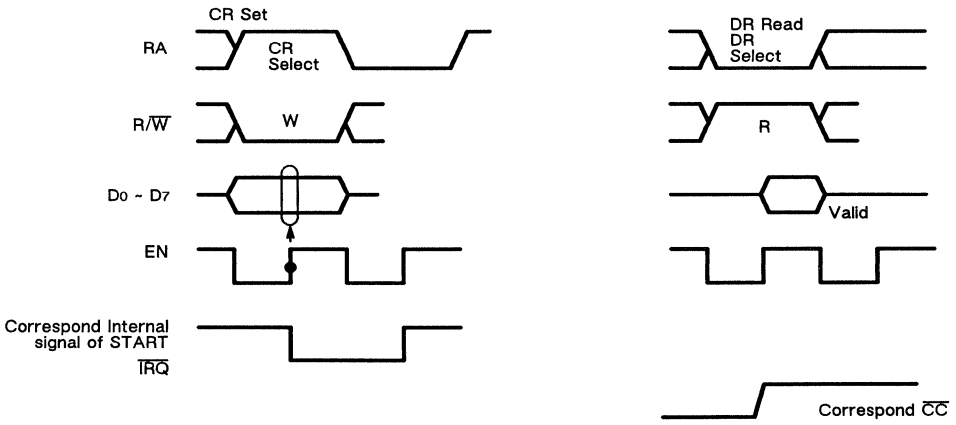
MPU Control Mode (CR-5 = 1):

This mode is used when ADC is controlled by the MPU software. When CR-5 = 0 at initialization, CR-5 should first be set high through MPU. Channel designation of analog input signal is made by CR-2-4, programmed through MPU, and AD conversion starts as CR-6 = 1. After completion of the conversion, CR-7 (IRQ flag) is set high and $\overline{IRQ}$ output goes low to interrupt MPU operation.

After confirming $\overline{IRQ}$ = 0, MPU starts the interrupt routine to select the data register of ADC and reads it. After MPU reads the data register, $\overline{IRQ}$ is reset high. In this mode, all signals on $\overline{START}$ and B_0-B_2 are ignored. When the ADC is required to return to the external control mode, CR-5 is set low through MPU or $\overline{RESET}$ is set low.

ADC TIMING FOR MPU CONTROL MODE



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage 1	V_{CC}	+7	V
Supply Voltage 2	V^+	+10	V
Supply Voltage 3	V^-	-10	V
Digital Input Voltage	V_{ID}	-0.5 ~ +5.5	V
Analog Input Voltage	V_{IA}	-3.0 ~ V^+	V
Operating Temperature	T_A	-35 ~ +90	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage 1	V_{CC}	4.75	5.0	5.25	V	-30°C to +85°C
Supply Voltage 2	V^+	7.6	8.0	8.4	V	
Supply Voltage 3	V^-	-8.4	-8.0	-7.6	V	
Digital Output High Current	I_{OH}	—	—	-0.4	mA	
Digital Output Low Current	I_{OL}	—	—	8	mA	

Electrical Characteristics

ANALOG CIRCUIT CHARACTERISTICS
(V_{CC} = +5V, V^+ = +8V, V^- = -8V, T_A = -30°C ~ +85°C)

Parameter		Value			Unit	Note
		Min	Typ	Max		
Resolution		—	—	10	bit	
Accuracy	Relative Accuracy	8	—	—	bit	
	Gain Error	—	±1	—	% of FSR	Adjustable
	Offset Error	—	±0.03	—	% of FSR	Adjustable
	Differential Linearity Error	—	±0.5	—	LSB	
Drift	Full Scale Voltage	—	60	—	ppm/°C	
	Offset Voltage	—	±0.5	—	ppm of FSR/°C	
Full Scale Power Supply Fluctuation Suppressing Ratio	Positive Power Supply	—	1.0	—	mV/V	8V ±5%
	Negative Power Supply	—	-0.5	—	mV/V	-8V ±5%
Analog Input	Impedance	0.5	20	—	MΩ	V_{IA} = 6.5V
	Conversion Voltage	0	—	6.5	V	
Reference Voltage	Reference Voltage	—	5.0	—	V	
	Drift	—	40	—	ppm/°C	
Supply Current	Positive Power Supply	—	7	12	mA	
	Negative Power Supply	—	-10	-17	mA	
Conversion Cycle Time		2	—	—	µs/bit	

7

Electrical Characteristics (Continued)

DIGITAL CIRCUIT DC CHARACTERISTICS
(V_{CC} = +5V ±5%, V^+ = +8V, V^- = −8V, T_A = −30°C ~ +85°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input High Voltage	V_{IH}		2	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Input Clamp Voltage	V_{IC}	V_{CC} = 4.75V, I_{IC} = −18mA	—	—	−1.5	V
Output High Voltage	V_{OH}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −2.6mA	2.4	—	—	V
Output Low Voltage	V_{OL}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 4mA	—	—	0.4	V
		V_{CC} = 4.75V, V_{IL} = 0.8V, V_{IH} = 2V, I_{OL} = 8mA	—	—	0.5	
Output Current (Off State)	I_{OZ}	V_{IH} = 2V, V_{CC} = 5.25V, V_O = 2.7V, V_{IL} = 0.8V	—	—	20	μA
		V_{IL} = 0.8V, V_{CC} = 5.25V, V_O = 0.4V, V_{IH} = 2V	—	—	−20	
Input High Current	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.25V	—	—	20	μA
		V_{IH} = 7V, V_{CC} = 5.25V	—	—	100	
Input Low Current	I_{IL}	V_{IL} = 0.4V, V_{CC} = 5.25V	—	—	−400	μA
Output Short Current	I_{OS}	V_O = 0V, V_{CC} = 5.25V	−15	—	−95	mA
Supply Current	I_{CC}	A_0 ~ A_7, $\overline{Reset}$ = GND, V_{CC} = 5.25V	30	55	92	mA

7

Electrical Characteristics (Continued)

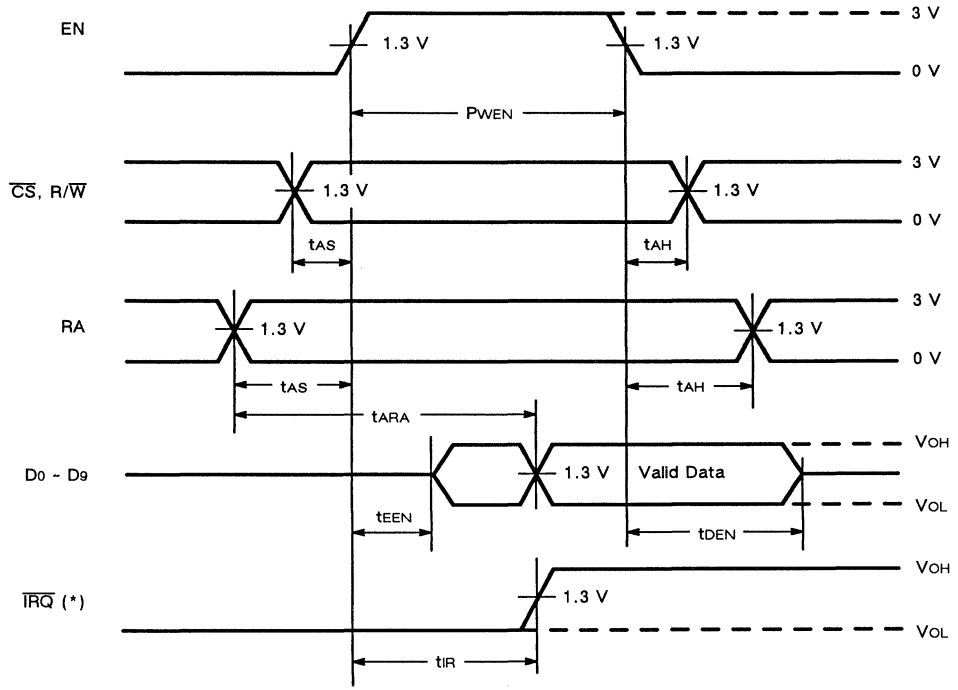
DIGITAL CIRCUIT AC CHARACTERISTICS

(V_{CC} = +5V ±5%, V^+ = +8V, V^- = −8V, T_A = −30°C ~ +85°C)

READ MODE

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
EN Pulse Width	P_{WEN}	—	270	—	—	ns
$\overline{CS}$, R/$\overline{W}$, RA Setup Time	t_{AS}	—	20	—	—	ns
$\overline{CS}$, R/$\overline{W}$, RA Hold Time	t_{AH}	—	10	—	—	ns
Enable Time from EN	t_{EEN}	Figure 2	—	—	160	ns
Access Time from RA	t_{ARA}	Figure 2	—	—	300	ns
Disable Time from EN	t_{DEN}	Figure 2	10	—	120	ns
$\overline{IRQ}$ Recovery Time from EN	t_{IR}	Figure 3	—	—	240	ns

READ TIMING DIAGRAM



*: $\overline{IRQ}$ is reset to "1" when DR is read or $\overline{Reset}$ goes low.

7

Electrical Characteristics (Continued)

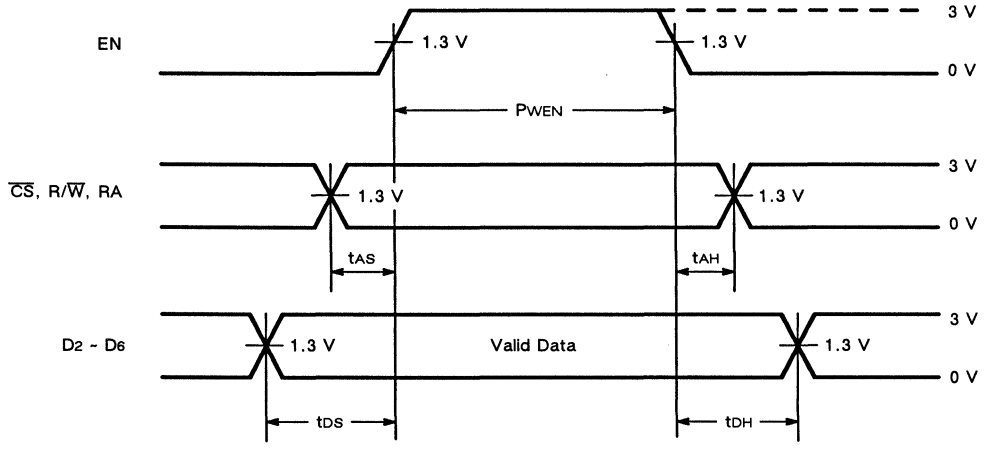
DIGITAL CIRCUIT AC CHARACTERISTICS

(V_{CC} = +5V ±5%, V^+ = +8V, V^- = −8V, T_A = −30°C ~ +85°C)

WRITE MODE

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
EN Pulse Width	P_{WEN}		270	—	—	ns
$\overline{CS}$, R/$\overline{W}$, RA Setup Time	t_{AS}		20	—	—	ns
$\overline{CS}$, R/$\overline{W}$, RA Hold Time	t_{AH}		10	—	—	ns
Data Setup Time	t_{DS}		10	—	—	ns
Data Hold Time	t_{DH}		10	—	—	ns

WRITE TIMING DIAGRAM



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Electrical Characteristics (Continued)

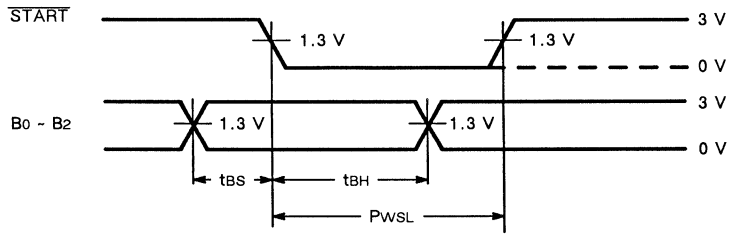
DIGITAL CIRCUIT AC CHARACTERISTICS

(V_{CC} = +5V ±5%, V^+ = +8V, V^- = -8V, T_A = -30°C ~ +85°C)

EXTERNAL CONTROL AD CONVERSION

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
$\overline{START}$ Pulse Width	P_{WSL}		270	—	—	ns
Channel Setup Time	t_{BS}		20	—	—	ns
Channel Hold Time	t_{BH}		270	—	—	ns

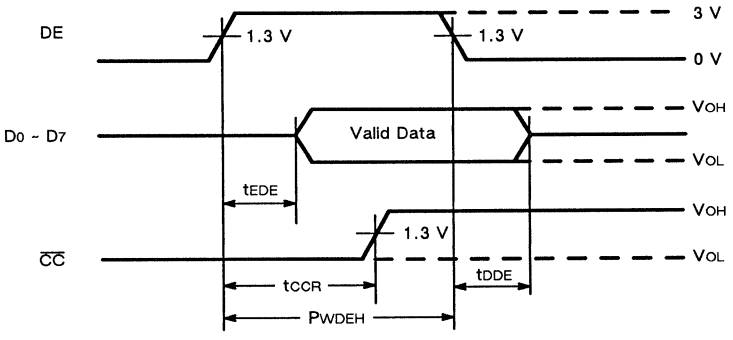
EXTERNAL CONTROL AD CONVERSION TIMING DIAGRAM



EXTERNAL CONTROL READ MODE

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
DE Pulse Width	P_{WDEH}		270	—	—	ns
Enable Time from DE	t_{EDE}	Figure 2	—	—	160	ns
Disable Time from DE	t_{DDE}	Figure 2	10	—	80	ns
$\overline{CC}$ Recovery Time from DE	t_{CCR}	Figure 3	—	—	280	ns

EXTERNAL CONTROL READ TIMING DIAGRAM



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Switching Characteristics Test Conditions

Fig. 2 — 3-STATE OUTPUT LOAD CONDITION

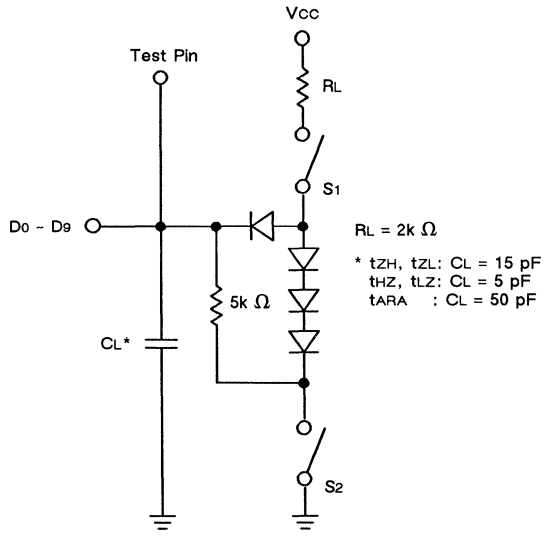

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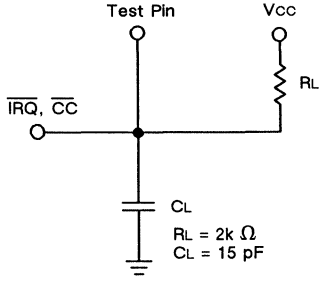
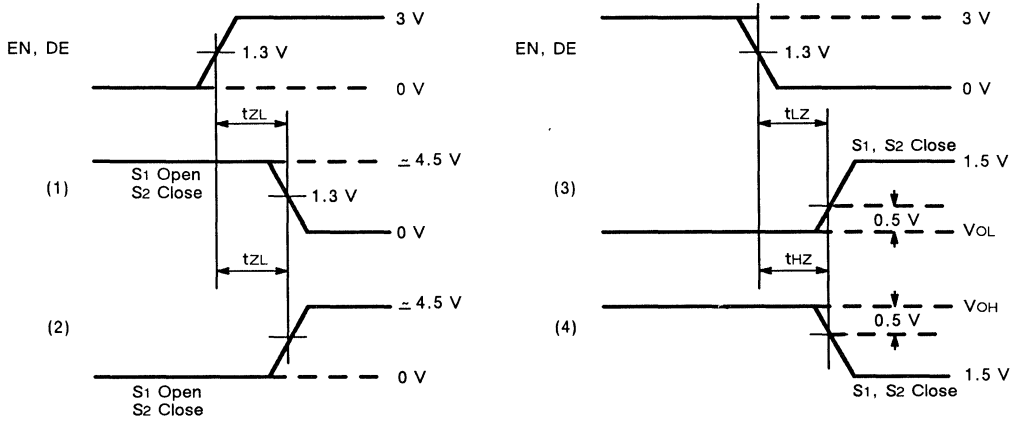
Fig. 3 — O.C. OUTPUT LOAD CONDITION



Switching Waveform

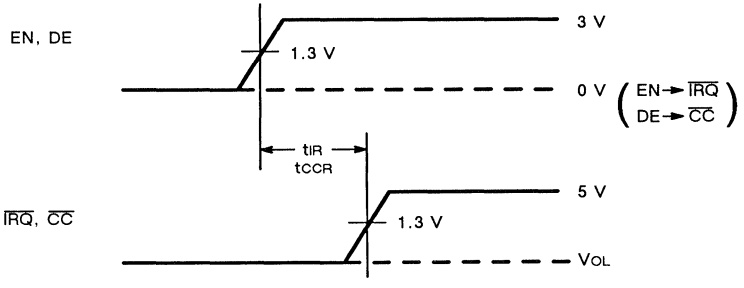
ENABLE, DISABLE TIME (3-STATE OUTPUT)



Note S1, S2: See Fig 2.

7

$\overline{IRQ}$ OR $\overline{CC}$ RECOVERY TIME (OPEN COLLECTOR OUTPUT)



Typical Characteristics Curves

Fig. 4 Output Voltage vs. Input Voltage

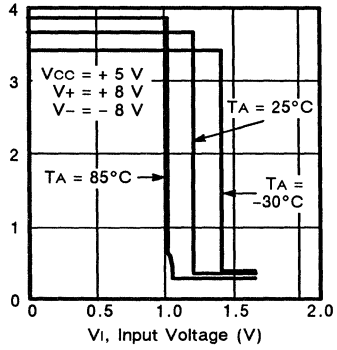


Fig. 5 Output High Voltage vs. Output High Current

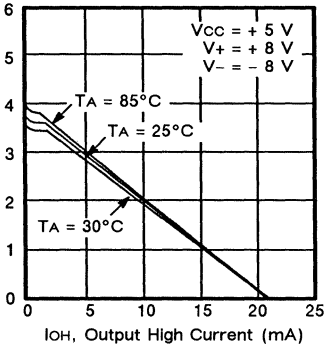


Fig. 6 Output Low Voltage vs. Output Low Voltage

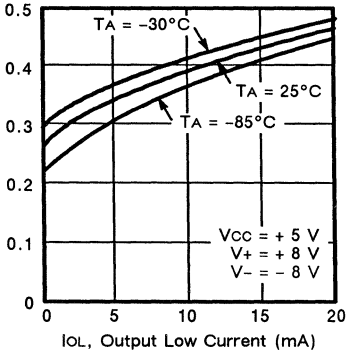


Fig. 7 Input Current vs. Input Voltage (BO Input)

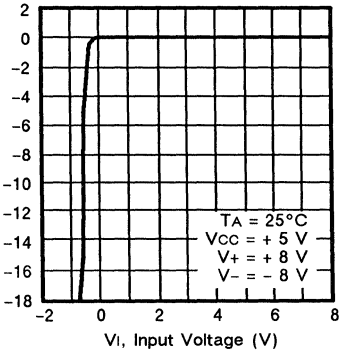


Fig. 8 Delay Time vs. Ambient Temperature

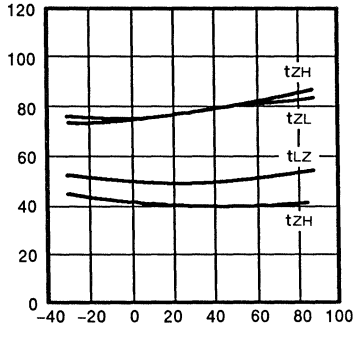
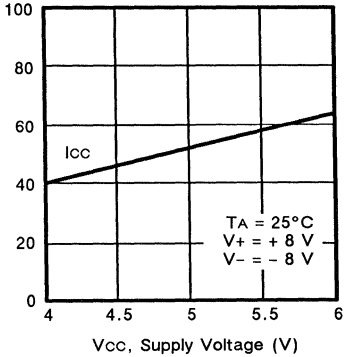


Fig. 9 Supply Current vs. Supply Voltage



7

Typical Characteristics Curves (Continued)

Fig. 10 Supply Current vs. Positive Supply Voltage

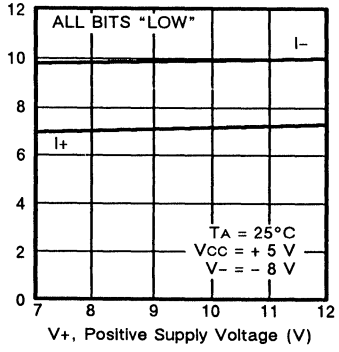


Fig. 11 Supply Current vs. Negative Supply Voltage

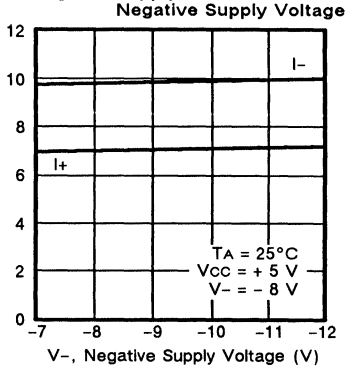


Fig. 12 Full Scale Voltage vs. Reference Voltage Supply Voltage (V+, |V−|)

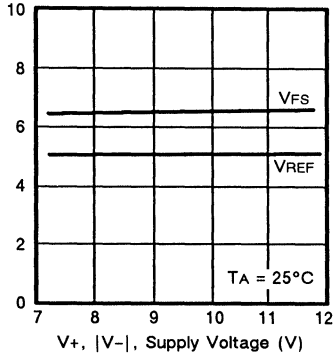
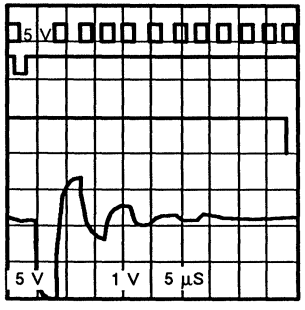


Fig. 13 Operational Waveform



fCLK = 250 KHz

Analog Input Voltage = 2.1646 V
Output Coding = 0101010101

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Technical Information

DEFINITION OF TERMS

Resolution:

The minimum distinguishable analog deviation in AD converter. Since MB4051 is a 10-bit AD converter, it is possible to resolute an analog signal, from 0V to 6.5V (FSR), into 2^{10} = 1024 parts.

Relative Accuracy:

Deviation between a straight line from the zero point of the device (all "0") to the full-scale point (all 'L') and an actual conversion characteristic curve.

Gain Error:

Difference between an ideal input voltage span and an actual input voltage span. In the MB4051, according to the procedure described separately, it is possible to adjust the gain error to zero.

Offset Error:

Difference between an ideal critical input voltage which makes all output bits zero and an actual critical input voltage. In the MB4051, such offset error can be adjusted according to the procedure described separately.

Differential Linearity Error:

Input voltage deviation from an ideal input voltage which is necessary to change the output code as large as 1 LSB. The differential linearity error of ±1/2 LSB means that, when the input signal changes 1/2 LSB ~ 3/2 LSB, digital code varies 1 LSB.

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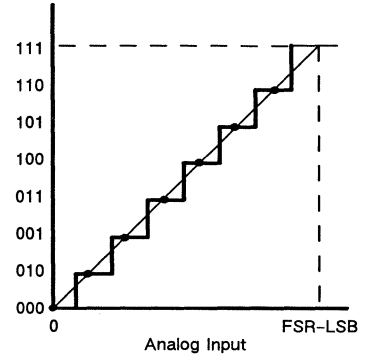
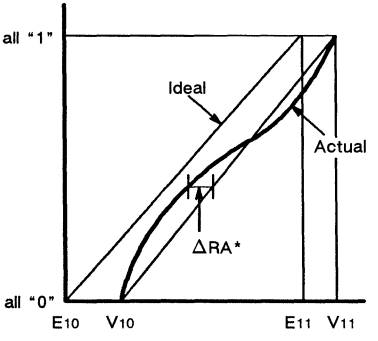
Example of Output Coding

Scale	Input Voltage	MSB	D1	D2	D3	D4	D5	D6	D7	D8	LSB
FS - 1 LSB	6.4937	1	1	1	1	1	1	1	1	1	1
FS/2	3.2500	1	0	0	0	0	0	0	0	0	0
FS/4	1.6250	0	1	0	0	0	0	0	0	0	0
FS/8	0.8125	0	0	1	0	0	0	0	0	0	0
FS/16	0.4063	0	0	0	1	0	0	0	0	0	0
FS/32	0.2031	0	0	0	0	1	0	0	0	0	0
FS/64	0.1016	0	0	0	0	0	1	0	0	0	0
FS/128	0.0508	0	0	0	0	0	0	1	0	0	0
FS/256	0.0254	0	0	0	0	0	0	0	1	0	0
FS/512	0.0127	0	0	0	0	0	0	0	0	1	0
FS/1024 = 1 LSB	0.0063	0	0	0	0	0	0	0	0	0	1
0	0.0000	0	0	0	0	0	0	0	0	0	0

Example of Resolution
(3-bit Resolution)



Relative Accuracy/Gain Error/Offset Error

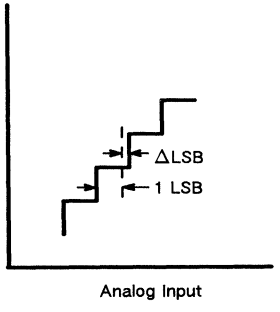


* Relative Accuracy = ΔRA

$$\text{Gain Error} = \frac{(V_{11} - V_{10}) - (E_{11} - E_{10})}{\text{FSR}} \times 100 \text{ (\% of FSR)}$$

$$\text{Offset Error} = \frac{V_{10} - E_{10}}{\text{FSR}} \times 100 \text{ (\% of FSR)}$$

Differential Linearity Error (ΔLSB)

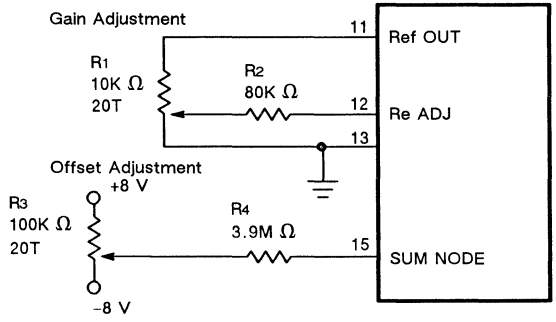


Applications Information

Adjustment of Offset and Gain

In the MB4051, both gain-error and offset-error can be adjusted to zero by trimmers connected as shown below. In this case, potentiometers and resistors for trimmers should have temperature characteristics below 100ppm/C° to ensure long-term stability and less temperature drift.

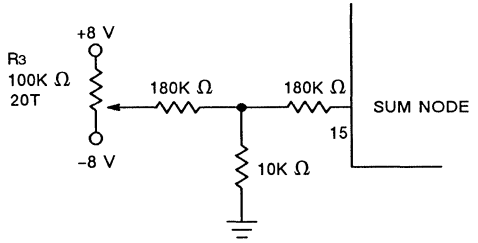
The following external adjustment circuits should be located as near as possible to the package with the 3.9mΩ resistor the closet connection to the package.



Offset Adjustment

By applying the voltage of 1/2 LSB, i.e., 3.2mV to an analog input channel, continuously execute AD conversion of the applied input voltage. Then, adjust potentiometer R3 during the conversion so that the conversion results become "0000000000" and "0000000001", alternatively. The range of adjustment is about ±0.2% of FSR in the circuit shown below.

The R4 resistor for offset adjustment can be replaced with smaller resistors as follows.



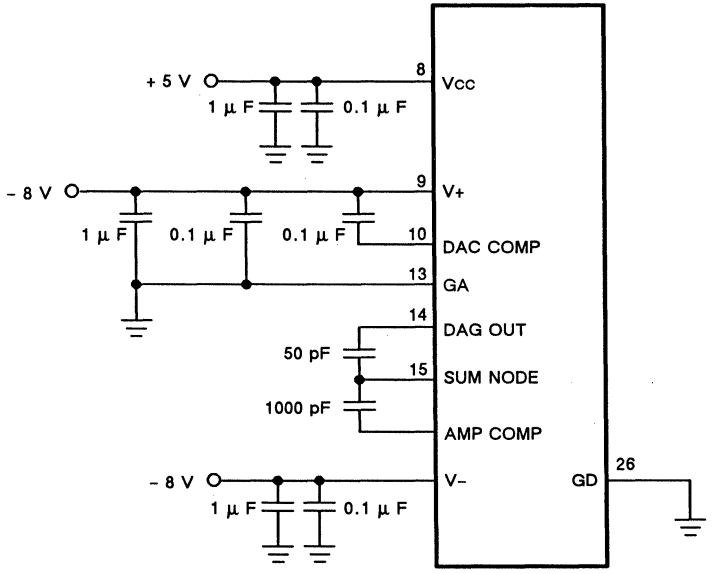
Gain Adjustment

After offset adjustment, by applying FSR - 3/2 LSB (6.4905V) to an analog input, execute AD conversion of the applied input voltage. Then, adjust potentiometer R_1 during the conversion so that the conversion results become "1111111111" and "1111111110", alternatively. The range of adjustment is about -12% ~ +5% of FSR in the circuit shown.

Precautions for Circuit Stabilization

To stabilize the ADC operation and by-pass power supply line noise, connect the external capacitors as shown.

CAPACITORS FOR STABILIZATION AND POWER SUPPLY BYPASS

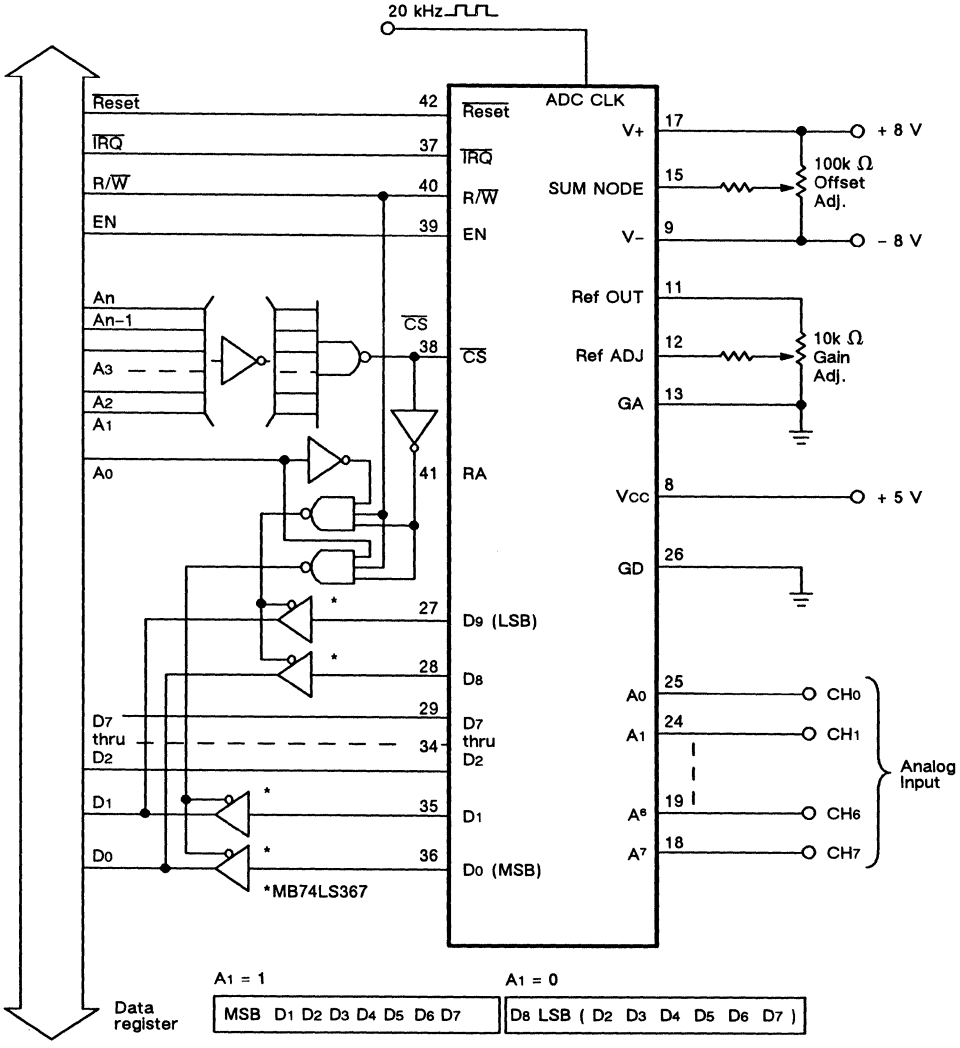


The bypass capacitor for filtering line-noise should have good high-frequency characteristics and should be connected as near as possible to the package.

If a printed circuit board is used, the ground-line should be made as wide as possible and the pattern should be made in such a manner that the analog input signal line does not pick up noise from the digital signal and so on. Unused digital input should be kept in an inactive state as shown below, and unused analog input should be connected to analog ground (GA).

Inactive State	Terminals
"L"	EN, RA, R/$\overline{W}$, DE, B_0 ~ B_2
"H"	$\overline{Reset}$, $\overline{CS}$, $\overline{START}$

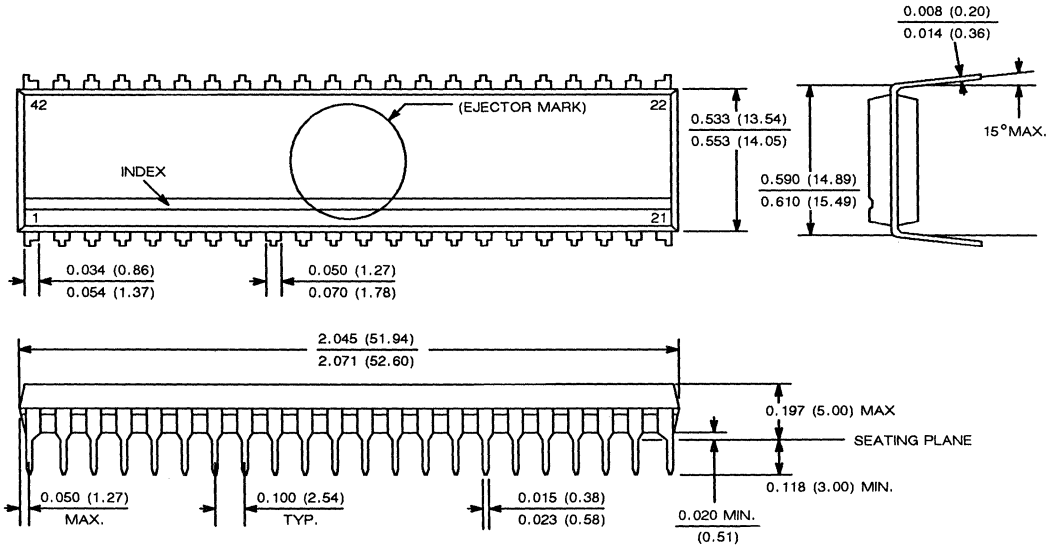
EXAMPLE OF INTERFACE TO 8-BIT MPU
(Provide a Change Circuit for Upper 2-bits)



7

Package Dimensions

42-PIN PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-42P-M01)



Dimension in inches and (millimeters)

7

FUJITSU

4-CHANNEL 8-BIT A/D CONVERTER

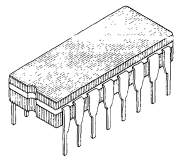
MB4052

July 1988
Edition 4.0

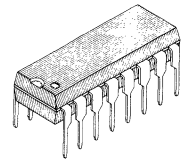
4-CHANNEL 8-BIT A/D CONVERTER SUBSYSTEM

The Fujitsu MB 4052 is an analog-to-digital converter (ADC) for general purpose which features four channels of analog inputs and 8-bit data length of digital output.
Analog input signal is converted to serial 8-bit digital data by the successive-approximation technique which provides high-speed conversion, i.e. many analog data can be converted within a short time.
All digital I/O signals including control inputs are TTL level compatible so as to provide wide application such as in microprocessor-controlled system and so on.

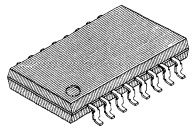
- Single Power Supply;
  DIP: +3.5V to +6.0V or +8.0V to +18V (with Internal Regulator)
  FPT: +3.5V to +6.0V or +8.0V to +13.2V (with Internal Regulator)
- Multiplex 4-Channel Analog Inputs
- Analog Input Voltage Ranges:
  0 to $1/2V_{CC1}$ (Standard mode: RS = 1)
  0 to $1/8V_{CC1}$ (Contracted mode: RS = 0)
  0 to $2V_{CC1}$ (Expanded mode: through built-in Divider)
- Analog Input Bias Current: 250nA Max.
- Resolution: 8 bits
- Linearity: 0.19% Max.
- Successive-Approximation Conversion: 100μs/ch Max. at f_{CLK} = 100 kHz
- Ratio-Metric Conversion by Reference Voltage V_{CC1}
- Serial Data Output (Open-Collector)
- TTL/CMOS Compatible Digital I/O
- Package: DIP-16C-C02
  DIP-16P-M04
  FPT-16P-M03



CERAMIC PACKAGE
DIP-16C-C02

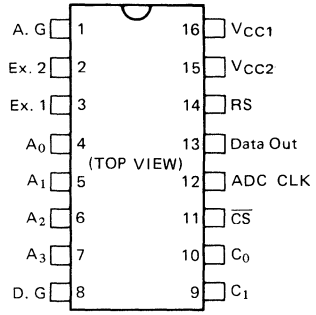


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M03

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (All Voltages referenced to A.G/D.G)

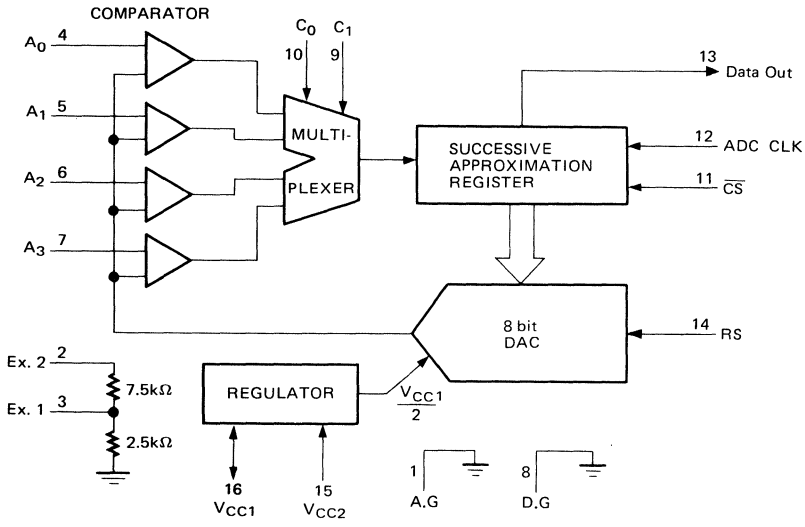
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC1}	+7	V
		V_{CC2}	+20	V
Digital Input Voltage		V_{ID}	−0.5 to +20	V
Digital Output Voltage (Off-State)		V_{OH}	+20	V
Analog Input Voltage		V_{IA}	V_{CC1}+0.5	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−40 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1—MB 4052 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

(T_A = −30°C to +85°C)

Parameter	Symbol		Value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC1}		3.5	5.0	6.0	V
	V_{CC2}	DIP	8.0	12.0	18.0	V
		FPT	8.0	12.0	13.2	V
Digital Output Low Current	I_{OL}		–	–	8	mA
Operating Temperature	T_A		−30	–	+85	°C

PIN DESCRIPTIONS

INPUT FOR VOLTAGE RANGE EXPANSION (EX 2), PIN 2

This input pin is provided to expand the voltage range of analog input signal.
This input pin is connected to the internal one-to-four voltage divider which reduces an analog signal level to one fourth of input level.

OUTPUT FOR VOLTAGE RANGE EXPANSION (EX 1), PIN 3

This output pin is provided to expand the allowable analog input level in co-operation with the above EX 2 pin.
A reduced signal which is divided in the internal divider is output on this pin.
This output pin can be connected to any of standard analog inputs A_0, A_1, A_2 or A_3 so that the EX 2 pin can function as one of 4-channel inputs.

ANALOG INPUTS (A_0 TO A_3), PINS 4, 5, 6 AND 7

These input pins are provided to receive four channels of analog inputs.
One of these four channels is selected by a combination of C_0 and C_1 inputs.

CHANNEL SELECT (C_1 AND C_0), PINS 9 AND 10

These control inputs are used to designate one of four analog inputs as shown in Table 1.

Table 1 CHANNEL SELECTION

C_1	C_0	Channel
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

CHIP SELECT ($\overline{CS}$), PIN 11

This control input pin is used to start analog-to-digital conversion.
When $\overline{CS}$ goes low, the A/D conversion start and the DATA OUT output is enabled.
When an A/D conversion is completed or termination of conversion is required, $\overline{CS}$ is made high.

A/D CONVERSION CLOCK (ADC CLK), PIN 12

This clock signal is input to the internal successive approximation register and used as timing signal for A/D conversion.
The conversion speed of this device is determined by this clock rate.
Ten clock cycles are required for a complete 8-bit conversion.
A precise cycle time is not always required for this clock signal.

DATA OUTPUT (DATA OUT), PIN 13

This output pin is provided to output the A/D conversion results as digital signals.
The converted digital data are serially output in the order of start-bit, MSB (Most Significant Bit), 2SB (Second Significant Bit), . . . , 7SB, LSB (Least Significant Bit) and stop-bit in synchronization with the ADC CLK clock signal.

RANGE SELECT (RS), PIN 14

This control input is provided to select an analog input voltage range as shown in Table 2.
This input must not be changed during an A/D conversion.

Table 2 RANGE SELECTION

RS	Voltage Range
0	0 to 1/8 V_{CC1}
1	0 to 1/2 V_{CC1}

ANALOG GROUND (A.G) AND DIGITAL GROUND (D.G), PINS 1 AND 8

These are terminals for ground.
The analog circuitry and digital circuitry have seperate ground terminals, respectively.

POWER SUPPLIES (V_{CC2} AND V_{CC1}), PINS 15 AND 16

When the device operates within a voltage range of 3.5V to 6.0V, the power source is connected to V_{CC1} which is shorted to V_{CC2}.
When the device operates within a voltage range of 8V to 18V in case of DIP Packages and 8V to 13.2V in case of Flat Package, the power source is connected to V_{CC2}.
In this high voltage operation mode, the V_{CC1} pin is used as an output pin which supplies +5V stabilized voltage and 10mA load current and the supplied voltage is regurated in the internal voltage regurator.
V_{CC1} is used as the reference voltage of A/D conversion regardless any two types voltage.

ANALOG CIRCUIT CHARACTERISTICS FOR PLASTIC DIP PACKAGE

(V_{CC1} = 3.5V to 6.0V, T_A = −30°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution			–	–	–	8	Bit
Linearity Error			V_{CC1} = 5V	–	–	±0.5	LSB
Differential Linearity Error				–	–	±0.9	LSB
Zero Transition Voltage	Contracted Range	V_{ZC}	V_{CC1} = 5V, T_A = 25°C	0	6	16	mV
	Standard Range	V_{ZS}		7	17	27	mV
	Expanded Range	V_{ZE}		22	62	102	mV
Full Scale Transition Voltage	Contracted range	V_{FC}		600	625	650	mV
	Standard Range	V_{FS}		2.475	2.500	2.525	V
	Expanded Range	V_{FE}		9.600	10.000	10.400	V
Comparator Input Current		I_{IC}	V_{CC1} = 5V	–	−100	−250	nA
Divider Input Resistance for Expanded Range		R_{INE}	–	5	10	15	kΩ
Regulator	Output Voltage	V_{OR}	8V ≤ V_{CC2} ≤ 18V	4.5	5.0	5.5	V
	Line Regulation			–	4.0	–	mV/V
	Load Regulation		V_{CC2} = 12V, 0mA ≤ I_{out} ≤ −10mA	–	0.5	–	mV/mA
	Output Voltage Temperature		V_{CC2} = 12V	–	50	–	ppm/°C
Conversion Cycle Time		t_{CYC}	f_{CLK} = 100kHz	–	–	100	μs/ch

A minus sign (−) prefixed to a current value indicates that the current flows from the IC to the external circuit.

ANALOG CIRCUIT CHARACTERISTICS FOR CERAMIC DIP PACKAGE

(V_{CC1} = 3.5V to 6.0V, T_A = −30°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution			–	–	–	8	Bit
Linearity Error			V_{CC1} = 5V	–	–	±0.4	LSB
Differential Linearity Error				–	–	±0.8	LSB
Zero Transition Voltage	Contracted Range	V_{ZC}	V_{CC1} = 5V, T_A = 25°C	0	6	16	mV
	Standard Range	V_{ZS}		7	17	27	mV
	Expanded Range	V_{ZE}		22	62	102	mV
Full Scale Transition Voltage	Contracted range	V_{FC}		610	625	640	mV
	Standard Range	V_{FS}		2.480	2.500	2.520	V
	Expanded Range	V_{FE}		9.760	10.000	10.240	V
Comparator Input Current		I_{IC}	V_{CC1} = 5V	–	−100	−250	nA
Divider Input Resistance for Expanded Range		R_{INE}	–	5	10	15	kΩ
Regulator	Output Voltage	V_{OR}	8V ≤ V_{CC2} ≤ 18V	4.5	5.0	5.5	V
	Line Regulation			–	4.0	–	mV/V
	Load Regulation		V_{CC2} = 12V, 0mA ≤ I_{out} ≤ −10mA	–	0.5	–	mV/mA
	Output Voltage Temperature		V_{CC2} = 12V	–	50	–	ppm/°C
Conversion Cycle Time		t_{CYC}	f_{CLK} = 100kHz	–	–	100	μs/ch

A minus sign (−) prefixed to a current value indicates that the current flows from the IC to the external circuit.

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ANALOG CIRCUIT CHARACTERISTICS FOR PLASTIC FLAT PACKAGE

(V_{CC1} = 3.5V to 6.0V, T_A = −30°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution			–	–	–	8	Bit
Linearity Error			V_{CC1} = 5V	–	–	±0.5	LSB
Differential Linearity Error				–	–	±0.9	LSB
Zero Transition Voltage	Contracted Range	V_{ZC}	V_{CC1} = 5V, T_A = 25°C	0	6	16	mV
	Standard Range	V_{ZS}		7	17	27	mV
	Expanded Range	V_{ZE}		22	62	102	mV
Full Scale Transition Voltage	Contracted range	V_{FC}		600	625	650	mV
	Standard Range	V_{FS}		2.475	2.500	2.525	V
	Expanded Range	V_{FE}		9.600	10.000	10.400	V
Comparator Input Current		I_{IC}	V_{CC1} = 5V	–	−100	−250	nA
Divider Input Resistance for Expanded Range		R_{INE}	–	5	10	15	kΩ
Regulator	Output Voltage	V_{OR}	8V ≤ V_{CC2} ≤ 18V	4.5	5.0	5.5	V
	Line Regulation			–	4.0	–	mV/V
	Load Regulation		V_{CC2} = 12V, 0mA ≤ I_{out} ≤ −10mA	–	0.5	–	mV/mA
	Output Voltage Temperature		V_{CC2} = 12V	–	50	–	ppm/°C
Conversion Cycle Time		t_{CYC}	f_{CLK} = 100kHz	–	–	100	μs/ch

A minus sign (−) prefixed to a current value indicates that the current flows from the IC to the external circuit.

DIGITAL CIRCUIT DC CHARACTERISTICS

(V_{CC1} = 3.5V to 6.0V, T_A = -30°C to +85°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Clamp Voltage	V_{IC}	V_{CC1} = 3.5V, I_{IL} = -18mA	–	–	-1.5	V
High Level Input Current	I_{OH}	V_{CC1} = 3.5V, V_{IH} = 2.0V, V_{IL} = 0.8V, V_{OH} = 20V	–	–	100	μA
Low Level Output Voltage	V_{OL1}	V_{CC1} = 3.5V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 4mA	–	–	0.4	V
	V_{OL2}	V_{CC1} = 3.5V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 8mA	–	–	0.5	V
High Level Input Current	I_{IH1}	V_{CC1} = 6.0V, V_{IH} = 2.7V	–	–	20	μA
	I_{IH2}	V_{CC1} = 6.0V, V_{IH} = 20V	–	–	100	μA
Low Level Input Current	I_{IL}	V_{CC1} = 6.0V, V_{IL} = 0.4V	–	-50	-150	μA
Power Supply Current for V_{CC1}	I_{CC1}	V_{CC1} = 6.0V	–	15*	30	mA
Power Supply Current for V_{CC2}	I_{CC2}	V_{CC1} = Open, V_{CC2} = 20V for DIP Package V_{CC2} = 13.2V for FLAT Package	–	15	25	mA

*Note: This typical value is measured at V_{CC1} = 5.0V and T_A = 25°C.
A minus sign (–) prefixed to a current value indicates that the current flows from the IC to the external circuit.
The values are measured at V_{CC1} = V_{CC2} except the I_{CC2} parameter of .

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DIGITAL CIRCUIT AC CHARACTERISTICS

(V_{CC1} = 3.5V to 6.0V, T_A = -30°C to +85°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
ADC CLK Cycle Time	t_{CY}	10	–	–	μs
ADC CLK H Level Pulse Width	t_{WAC+}	2.5	–	–	μs
ADC CLK L Level Pusle Width	t_{WAC-}	2.5	–	–	μs
$\overline{CS}$ H Level Pulse Width	t_{WCS+}	1.5	–	–	μs
$\overline{CS}$ Set-up Time	t_{SCS}	1	–	–	μs
$\overline{CS}$ Hold Tim.	t_{HCS}	1	–	–	μs
Channel Set-up Time	t_{SCH}	0	–	–	μs
Channel Hold Time	t_{HCH}	1	–	–	μs
Propagation Delay Time	t_{PLH} t_{PHL}	–	800	2,000	ns

Fig. 2 – AC CHARACTERISTICS WAVEFORM

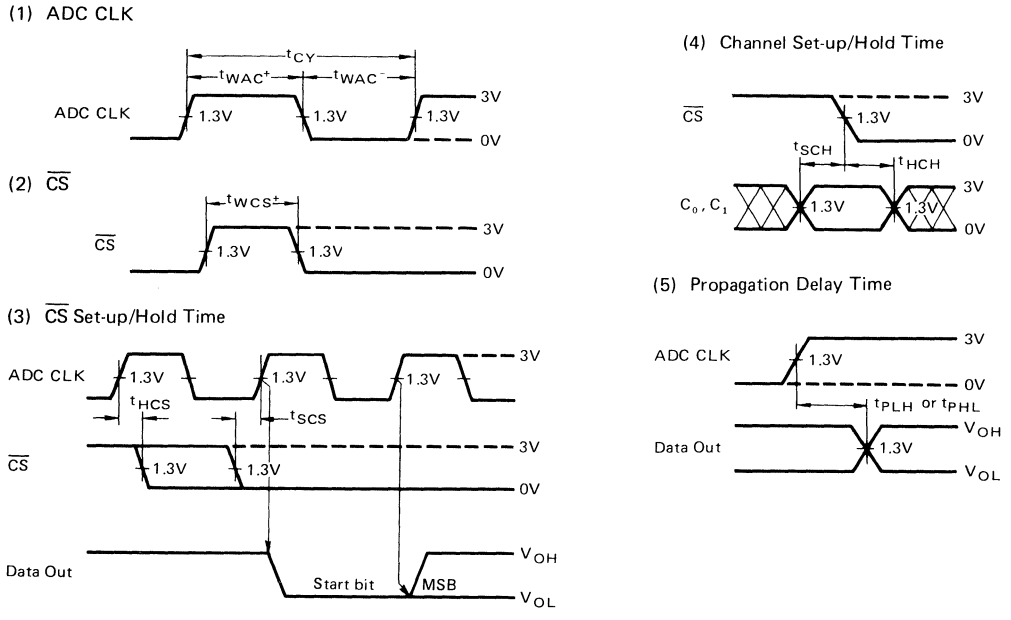
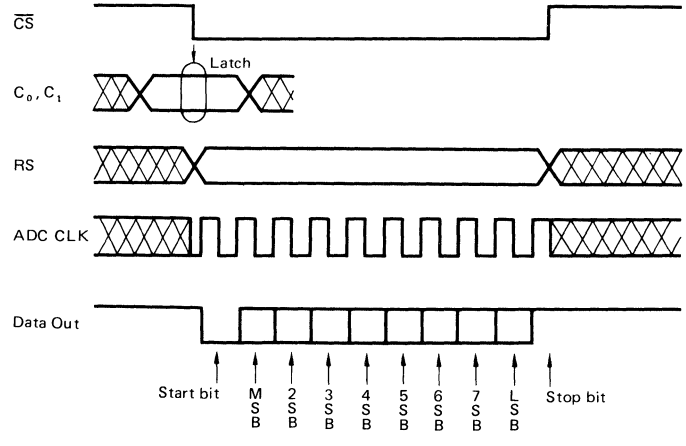
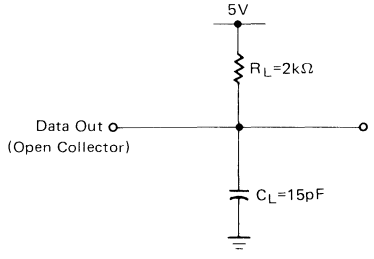


Fig. 3 – TIMING DIAGRAM



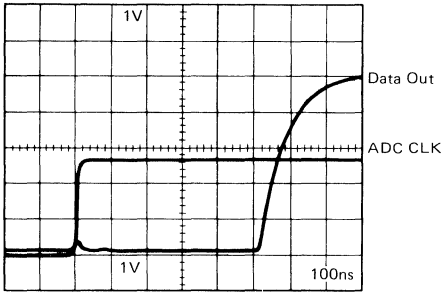
Note: RS should be held to one ranged "1" or "0" until data conversion is completed.

Fig. 4 – LOAD CONDITIONS

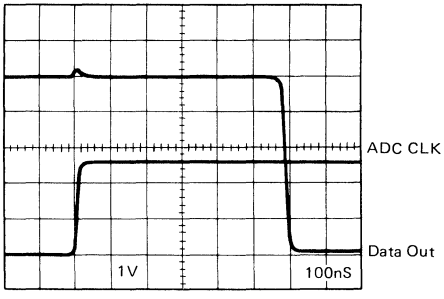


TYPICAL WAVEFORMS OF PROPAGATION DELAY

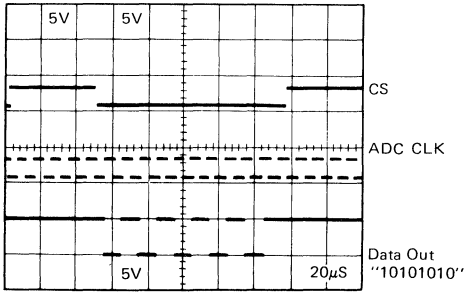
t_{PLH} (Data Out Transition from low-level to high-level)



t_{PHL} (Data Out Transition from high-level to low-level)

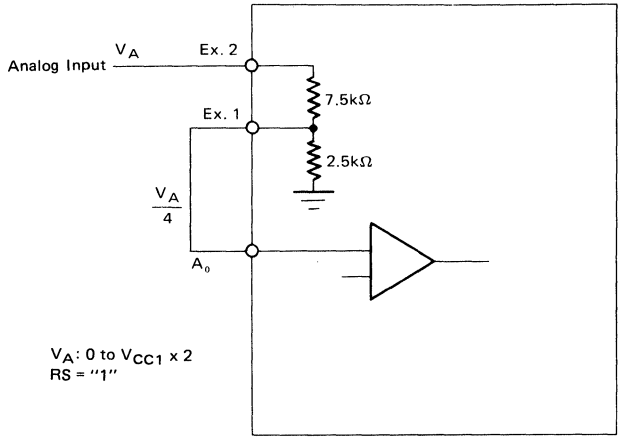


TYPICAL CONVERSION WAVEFORM



Condition
f_{CLK} = 100kHz
V_{CC1} = 5V
Standard Range
V_{IA} ≒ 1663 mV

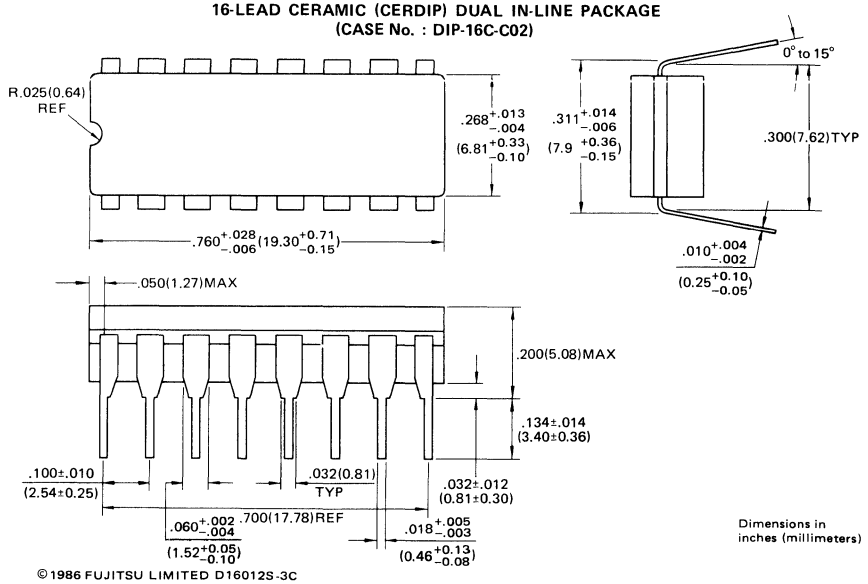
Fig. 5 – EXAMPLE OF EXPAND RANGE MODE CONNECTION



7

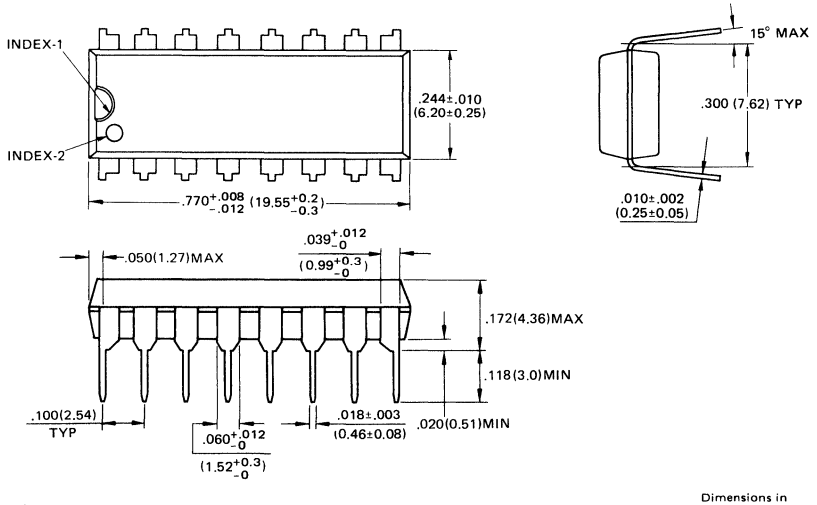
PACKAGE DIMENSIONS

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)



Dimensions in inches (millimeters)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)

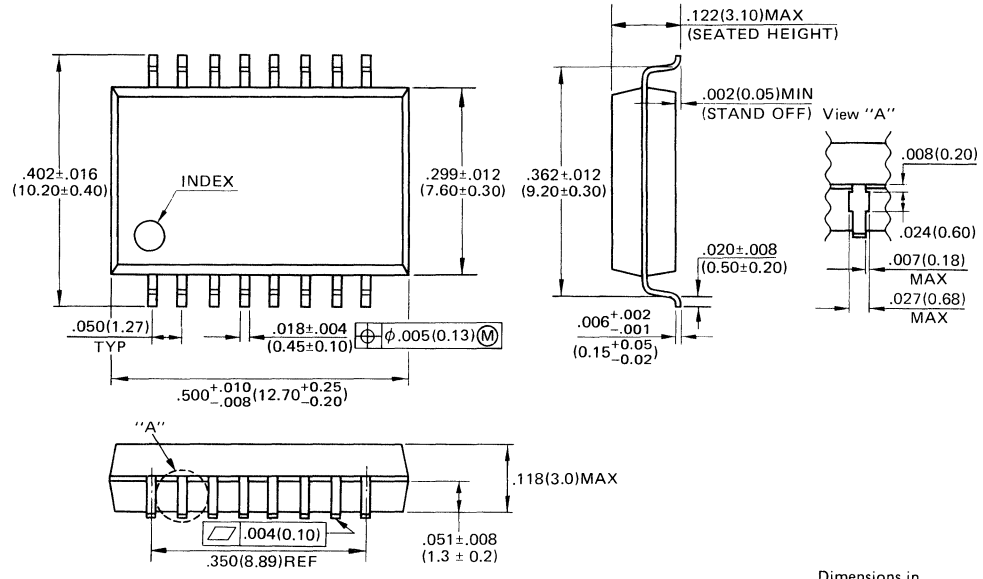


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS (continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M03)



Dimensions in
inches (millimeters)

7

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Printed in Japan PV2078-887A4

FUJITSU

6-CHANNEL 8-BIT AID CONVERTER SUBSYSTEM

MB 4053
MB 4063

August 1988
Edition 3.1

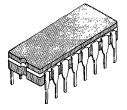
6-CHANNEL 8-BIT A/D CONVERTER SUBSYSTEM

The Fujitsu MB 4053 and MB 4063 are 6-channel, 8-bit, single-slope A/D converter subsystem designed to be used in a microprocessor based data control system. These devices provide the analog functions while the addressing, counting and timing functions are provided by a microprocessor such as the MB 8840/50, MBL 8048, MBL 8086, or MBL 8088.

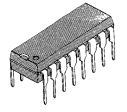
The MB 4053 and MB 4063 are single monolithic bipolar IC providing a 1 of 8 address decoder, 8-channel analog multiplier, sample and hold, constant current generator, ramp integrator and comparator in a 16-pin package.

These A/D converter subsystems are suitable for a wide range of applications. The resolution required by an application can be obtained by arbitrarily selecting a suitable integration time. Also zero offset and full-scale error corrections can be made automatically (auto-zero and auto-calibration) to minimize conversion error.

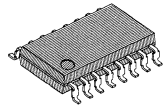
- Microprocessor/TTL compatible
- Zero offset and full-scale error correction capability
- Ratiometric conversion capability
- Available in 16-pin DIP and Flat Pack
- Compatible with MC14443 and μA9708 (DIP package)
- Single power supply : +4.75 V to +15 V
- Excellent linearity : ±0.2% max. error
- Fast conversion time : 300 μs/ch typ.
- Analog input volgage : 0 V to V_{CC} − 2 V (5.25 V max.)
- Power Dissipation : 25 mW typ. at V_{CC} = 5 V
- Standard 16-pin DIP or flat package.



CERAMIC PACKAGE
DIP-16C-C02

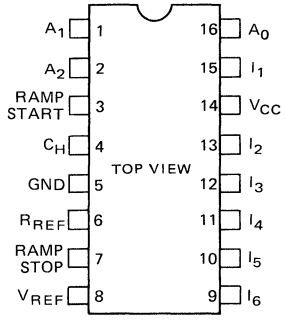


PLASTIC PACKAGE
DIP-16P-M01



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Supply Voltage		V_{CC}	18	V
Digital Input Voltage		V_{ID}	-0.5 to +30	V
Digital Output Voltage when Off		V_{OH}	-0.5 to +18	V
Analog Input Voltage		V_{IA}	-0.5 to +30	V
Output Current		I_O	10	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1a – MB 4053 BLOCK DIAGRAM

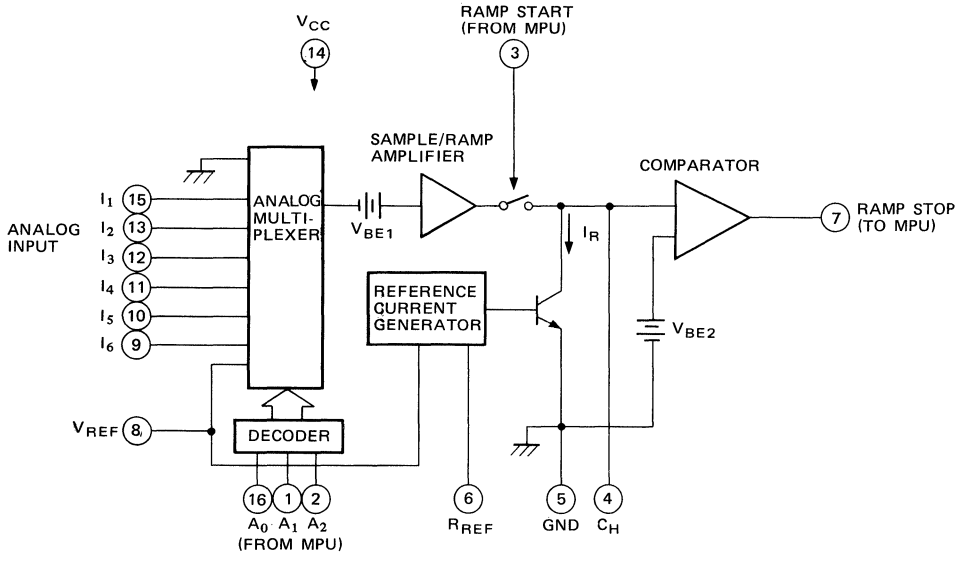
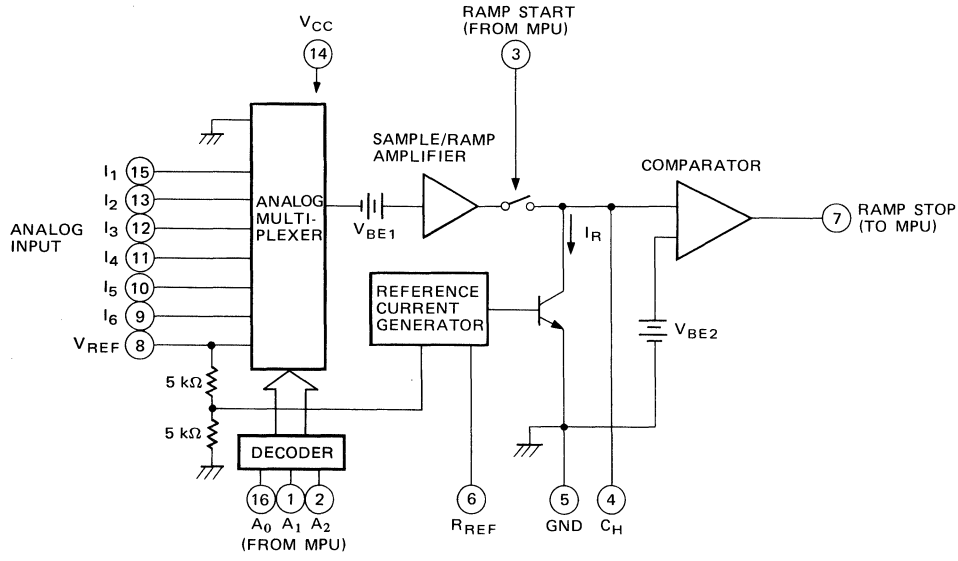


Fig. 1b – MB 4063 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition			Unit
			Min.	Typ.	Max.	
Supply Voltage		V_{CC}	4.75	5.0	15	V
Reference Voltage*	MB 4053	V_{REF}	2.0		5.25	V
	MB 4063		2.8			
Ramp Capacity		C_H	300			pF
Reference Current		I_R	12		50	μA
Analog Input Voltage		V_{IA}	0		V_{REF}	V
Output Current		I_O			1.6	mA
Operating Temperature		T_A	-40		+85	°C

NOTE: *$2V \leqq V_{REF} \leqq V_{CC}$ -2V for MB 4053, $2.8V \leqq V_{REF} \leqq V_{CC}$ -2V for MB 4063

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75 V to 15 V, T_A = −40°C to 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Conversion Error	E_A		±0.2	±0.3	%	†1
Linearity Error	E_R		±0.08	±0.2	%	†2
Analog Input Current	I_B		−50	−250	nA	
Crosstalk Between Any Two Channels	V_{CR}	60			dB	†3
Multiplexer Input Offset Voltage	V_{OSM}		2.0	4.0	mV	
Conversion Time	t_C		296	350	μs/ch	See test circuit Analog input: 0 thru V_{REF} C_H = 3300 pF, I_R = 50 μA
Acquisition Time	t_A		20	40	μs	See test circuit C_H = 1000 pF †4
Acquisition Current	I_A	150			μA	
Ramp Start Delay Time	t_O		100		ns	
Multiplexer Address Time	t_M		1		μs	
Digital High Level Input Voltage	V_{IH}	2.0			V	
Digital Low Level Input Voltage	V_{IL}			0.8	V	
Digital Low Level Input Current	I_{IL}		−5	−15	μA	V_{IL} = 0.4 V
Digital High Level Input Current	I_{IH}			1	μA	V_{IH} = 5.5 V
High Level Output Current	I_{OH}			10	μA	V_{OH} = 15 V
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
Supply Current	I_{CC}		5	10	mA	

A minus sign (−) prefixing a current value indicates that the current flows from the IC to the external circuit.

†1 Conversion error: For all channels, deviation from a straight line between two points obtained by channel addresses 000 (0 scale) and 111 (full scale).

†2 Linearity error: Deviation from a straight line between the 0 and full scale points for each channel.

†3 Crosstalk between channels: Voltage change V_{CH} of C_H terminal occurring when an input voltage of a channel is changed by $\triangle V_I$ while another channel is already charged (RAMP START = 0). This calculated by $20 \log \frac{\triangle V_{CH}}{\triangle V_I}$.

†4 Acquisition time: Sum of multiplexer delay time, RAMP START delay time, and time required to charge the selected input voltage to the ramp capacitor.

7

Fig. 2 – CONVERSION ERROR

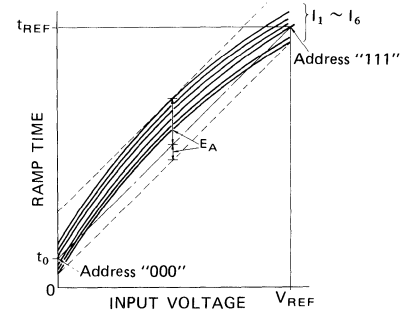


Fig. 3 – LINEARITY ERROR

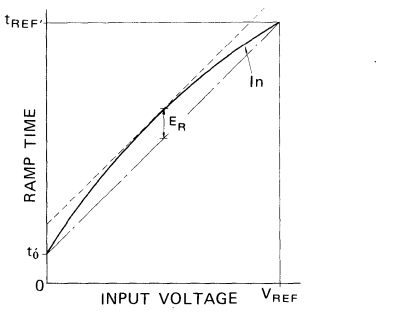
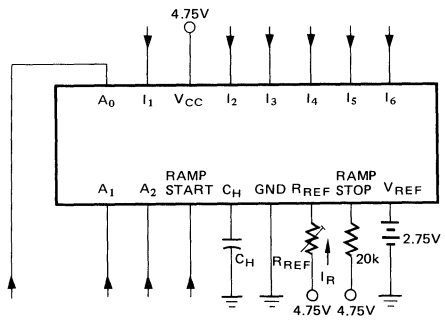


Fig. 4 – ACQUISITION/CONVERSION TIME TEST CIRCUIT

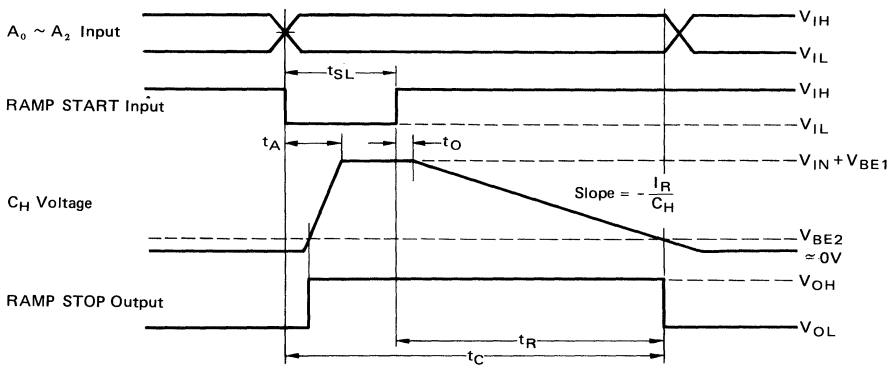


Adjust R_{REF} in the range 40 to 200 kΩ so that I_R is 12 to 50 μA.

CHANNEL SELECTION

Input address line			Selected analog input
A_2	A_1	A_0	
0	0	0	GND
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	V_{REF}

Fig. 5 – TIMING CHART



OPERATION DISCRIPTION

Refer to Fig. 1 MB 4053/MB 4063 BLOCK DIAGRAM, and Fig. 5 Timing Chart. Address inputs A_0 to A_2 are used to select the analog input to be converted, (one of the six analog inputs I_1 to I_6). The RAMP START input is switched from a logic 1 to a logic zero. This causes the external ramp capacitor C_H to charge at a fixed rate. (Note 1) until it reaches the sum of the selected analog input voltage and a constant offset voltage V_{BE1}. The RAMP STOP output (open-collector switches from a logic 0 to logic 1 when the voltage on C_H reaches the comparator reference voltage V_{BE2}. The RAMP START input is switched back to a logic 1 after C_H is completely charged. This disconnects the analog input from C_H and allows it to be gin discharging at a fixed rate (Note 2). When the voltage on C_H reaches the comparator reference voltage V_{BE2} the RAMP STOP output switches back to a logic 0. This completes a conversion cycle for 1 channel.

The time between the RAMP START input switching (0→1) and RAMP STOP output switching (1→0) is the RAMP TIME t_R. This would be directly proportional to the analog input voltage for the ideal situation where there was no comparator switching level error, leakage, switching delay times or effect of the impedance of the internal reference current source. t_R can be calculated for the ideal case as follows:

$$t_R = V_{IN} \times \frac{C_H}{I_R}$$

Where: V_{IN} = Analog input voltage to be measured
C_H = External ramp capacitor

$$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}} \text{ for MB 4053}$$

$$I_R = \frac{V_{REF}}{2 - R_{REF}} \text{ for MB 4063}$$

This ramp time is converted to a digital representation by counting t_R with the microprocessor. If a small error can be tolerated, the A/D conversion software can be reduced and the conversion time minimized by omitting corrections.

NOTE:

*1 Charge slope $= \frac{I_A - I_R}{C_H} \geqq \frac{150\mu A - I_R}{C_H}$

Where: I_A is the acquisition current whose value is determined from the circuit constant in the IC.

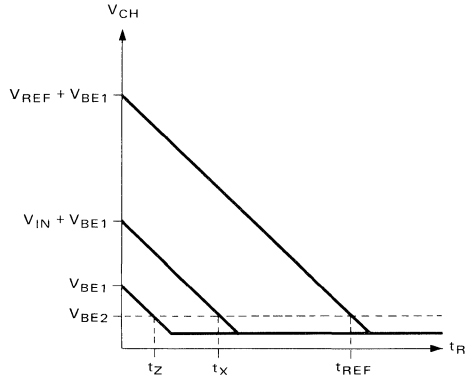
*2 Discharge slope $= -\frac{I_R}{C_H}$

ZERO OFFSET AND FULL-SCALE FACTOR CORRECTIONS

High precision conversions can be achieved by correcting for zero offset and full scale factor as follows:

The channel select address (A_0 to A_2) is set to 000. Ground (GND) is selected (internally) as the analog input and converted. This results in ramp time t_R. Next the address is set to 111. V_{REF} is selected (internally) and converted. This results in ramp time, t_{REF}. Finally the desired analog input (one of I_1 to I_6) is selected and converted. This results in ramp time t_X. This conversion sequence is arbitrary and the GND and V_{REF} conversions are not needed each time a channel is converted but only as required for calibration. The relationships between the inputs and ramp times are shown below.

$$(V_{BE1})_C = t_Z$$
$$(V_{REF} + V_{BE1})_C = t_{REF}$$
$$(V_{IN} + V_{BE1})_C = t_X$$
$$(V_{REF})_C = t_{REF} - t_Z$$
$$(V_{IN})_C = t_X - t_Z$$
$$\frac{(V_{IN})_C}{(V_{REF})_C} = \frac{t_X - t_Z}{t_{REF} - t_Z}$$



The conversion error can then be minimized by using the above results in the expression below to calculate the corrected analog input voltage.

$$(V_{IN})_C = (V_{REF})_C \times \frac{t_X - t_Z}{t_{REF} - t_Z}$$

Where: V_{IN} = Analog input voltage to be measured
V_{REF} = Reference voltage
V_{BE1} = Shift voltage in sample/ramp amplifier
V_{BE2} = Threshold voltage of comparator
V_{CH} = C_H voltage

The GND and V_{REF} conversion sequence is arbitrary, the GND and V_{REF} conversions not being needed each time a channel (I_1 to I_6) is converted.

7

PIN DESCRIPTION

Pin number	Name	Symbol	Function
9 ~ 13 15	Analog input	I_1 thru I_6	Analog inputs for the six channels. One of the 6 is selected by a specific bit pattern on A_0 to A_2.
16 1 2	Channel selection input	A_0 A_1 A_2	Inputs for selecting an analog input channel. Either GND, one of channels I_1 to I_6 or V_{REF} is selected by a specific bit pattern on the 3 inputs.
3	RAMP START signal input	RAMP START	A/D conversion start signal input. RAMP START (1→0) Ramp time start signal input. RAMP START (0→1)
7	RAMP STOP signal output	RAMP STOP	Indicates that C_H is charged over comparator reference voltage V_{BE2}. RAMP STOP (0→1) A/D conversion end signal (C_H discharged to comparator reference voltage). RAMP STOP (0→1)
4	Ramp capacitor pin	C_H	Pin for externally connecting the ramp capacitor. The value of C_H in conjunction with V_{REF} and R_{REF} establishes the ramp time.
8	Reference voltage supply pin	V_{REF}	Reference voltage supply pin. This is the reference voltage source for determining the discharge current and the analog reference voltage for full-scale factor correction. When the channel selection input is set to 111, this pin is selected for channel conversion. The full-scale factor is corrected using the conversion results. The voltage at this pin must be set to (GND + 2 V) to (V_{CC} − 2 V) and 5.25 V or less.
6	Reference resistance pin	R_{REF}	Pin for external reference resistance for setting the discharge current.
			MB 4053: The external resistance is connected between the power source pin (V_{CC}) and the reference resistance pin (R_{REF}). The discharge current is, then, $I_R = (V_{CC} - V_{REF})/R_{REF}$.
			MB 4053: The external resistance is connected between the reference voltage supply pin (V_{REF}) and the reference resistance pin (R_{REF}). The discharge current is, then $I_R = V_{REF}/2R_{REF}$.
14	Power supply	V_{CC}	Power supply pin
5	Ground	GND	Ground pin This pin is grounded. When the channel selection input is set to 000, this terminal is selected for channel conversion. The zero offset is corrected using the conversion results.

NOTES ON USE

1. Since the impedance of th ramp capacitor pin is approximately 30 MΩ (high), a resistance must not be connected in paralleled with this input. A ramp capacitor with no leakage must be used.
2. At V_{IN} = 0 V, t_R has a finite value.
3. Since RAMP STOP is an open collector output, an external pull-up resistor is required. (For example, when a 20 KΩ external pull-up resistor is used.)
4. All digital inputs/output are TTL compatible.
5. The time from RAMP START input switching (0 → 1) to RAMP STOP output switching (1 → 0) is ramp time t_R.
6. $t_{SL} \geqq t_A\ (max) = \dfrac{C_H}{150\ \mu A - I_R} \times (V_{REF} + 0.7\ V)$
7. $t_R \fallingdotseq \dfrac{C_H}{I_R} \times V_{IN}$, $t_R\ (max) \fallingdotseq \dfrac{C_H}{I_R} \times V_{REF}$
8. $I_R = \dfrac{V_{CC} - V_{REF}}{R_{REF}}$ for MB 4053, $I_R = \dfrac{V_{REF}}{2 - R_{REF}}$ for MB 4063
9. $2\ V \leqq V_{REF} \leqq (V_{CC} - 2\ V)$ and $V_{REF} \leqq 5.25\ V$ for MB 4053
   $2.8V \leqq V_{REF} \leqq (V_{CC} - 2\ V)$ and $V_{REF} \leqq 5.25\ V$ for MB 4063
10. While and analog input voltage is being sampled, channel selection signals A_0, A_1, and A_2 must not be changed for (t_{SL}).

TYPICAL CHARACTERISTIC CURVES

7

Fig. 9 – LINEARITY ERROR vs INPUT VOLTAGE

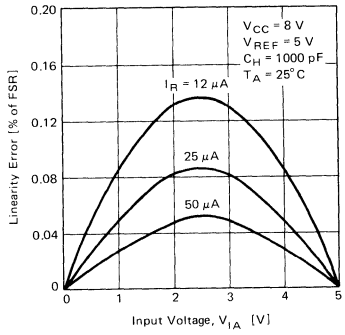


Fig. 10 – PEAK LINEARITY ERROR vs AMBIENT TEMPERATURE TA

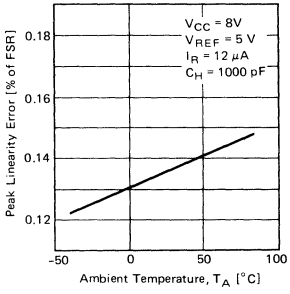
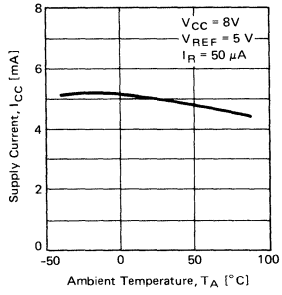


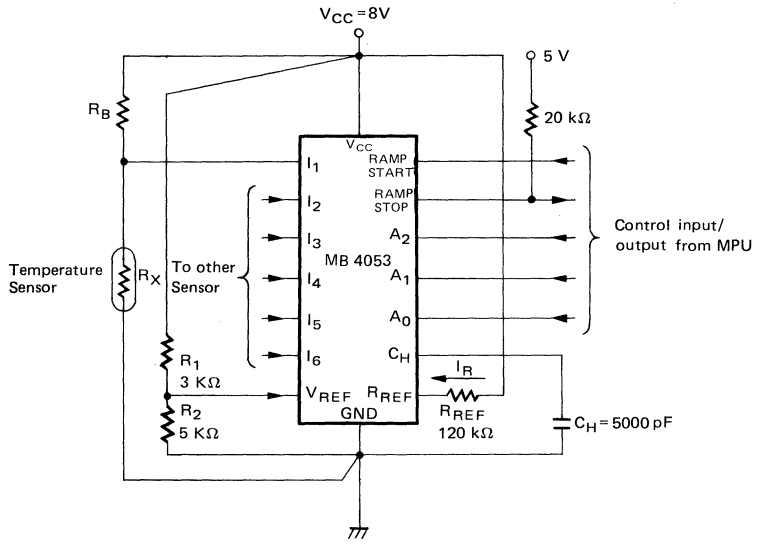
Fig. 11 – SUPPLY CURRENT vs AMBINENT TEMPERATURE



APPLICATION EXAMPLES

Examples of analog voltage (0 - 5V) A/D conversion with 10-bit resolution are shown in Fig.7 and Fig.8.

Fig. 7 — Application Example of MB 4053



Reference Voltage: $V_{REF} = \frac{R_2}{R_1 + R_2} V_{CC}$ 7-1

Ramp Current: $I_R = \frac{R_1}{R_1 + R_2} \cdot \frac{1}{R_{REF}} \cdot V_{CC}$ 7-2

Input Voltage: $V_{IN} = \frac{R_X}{R_X + R_B} \cdot V_{CC}$ 7-3

Ramp Time: $t_R \fallingdotseq V_{IN} \cdot \frac{C_H}{I_R}$

$= \frac{R_X}{R_X + R_B} \cdot (1 + \frac{R_2}{R_1}) \cdot C_H \cdot R_{REF}$ 7-4

$V_{REF} = \frac{5\ k\Omega}{3\ k\Omega + 5\ k\Omega} \times 8\ V = 5\ V$

$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}} = \frac{8\ V - 5\ V}{120\ k\Omega} = 25\ \mu A$

$t_{SL} \geqq \frac{C_H \times V_{REF}}{I_{A(min)} - I_R} = \frac{5000\ pF \times (5\ V + 0.7\ V)}{150\ \mu A - 25\ \mu A} = 228\ \mu s$

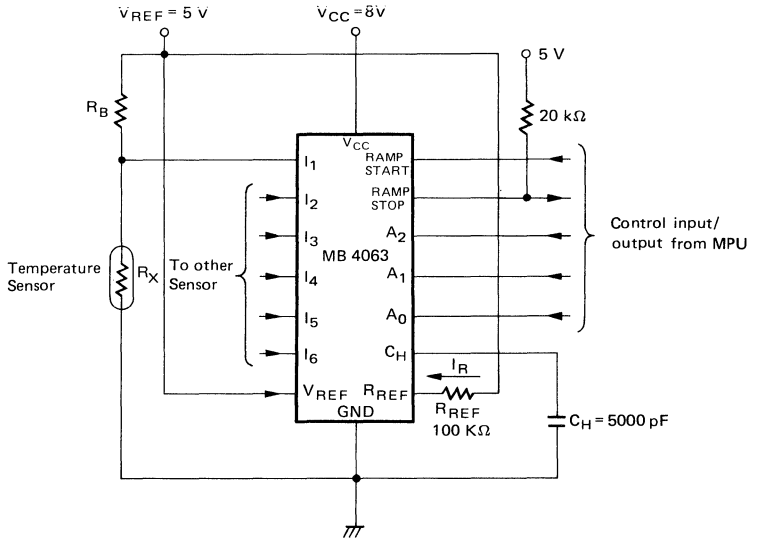
$t_{Rmax} \fallingdotseq \frac{C_H \times V_{REF}}{I_R} = \frac{5000\ pF \times 5\ V}{25\ \mu A} = 1000\ \mu s$

If the ramp time is counted with a 1 MHz clock, the following resolution is obtained.

$$\frac{1000\ \mu s}{1\ \mu s} = 1000 \fallingdotseq 2^{10}$$

As shown in this example, the voltage output of the sensor is proportional to V_{CC} (Eq. 7-3) and V_{REF} is also proportional to V_{CC} (Eq. 7-1), the sensor output conversion results (Eq. 7-4) are not influenced by power supply voltage fluctuation. Such a conversion is called ratio metric conversion and is effective for minimizing the effects of conversion error. Supply voltage fluctuations during discharge do result in error, however.

Fig. 8 — Application Example of MB 4063



Ramp Current: $I_R = \frac{V_{REF}}{2R_{REF}}$ 8-1

Input Voltage: $V_{IN} = \frac{R_X}{R_X + R_B} \cdot V_{REF}$ 8-2

Ramp Time: $t_R \fallingdotseq V_{IN} \cdot \frac{C_H}{I_R}$

$= \frac{R_X}{R_X + R_B} \cdot C_H \cdot 2R_{REF}$ 8-3

$I_R = \frac{V_{REF}}{2R_{REF}} = \frac{5V}{2 \times 100k\Omega} = 25\mu A$

$t_{SL} \geqq \frac{C_H \times V_{REF}}{I_A(min) - I_R} = \frac{5000pF \times (5V + 0.7V)}{150\mu A - 25\mu A} = 228\mu s$

$t_{R\,max} \fallingdotseq \frac{C_H \times V_{REF}}{I_R} = \frac{5000pF \times 5V}{25\mu A} = 1000\mu s$

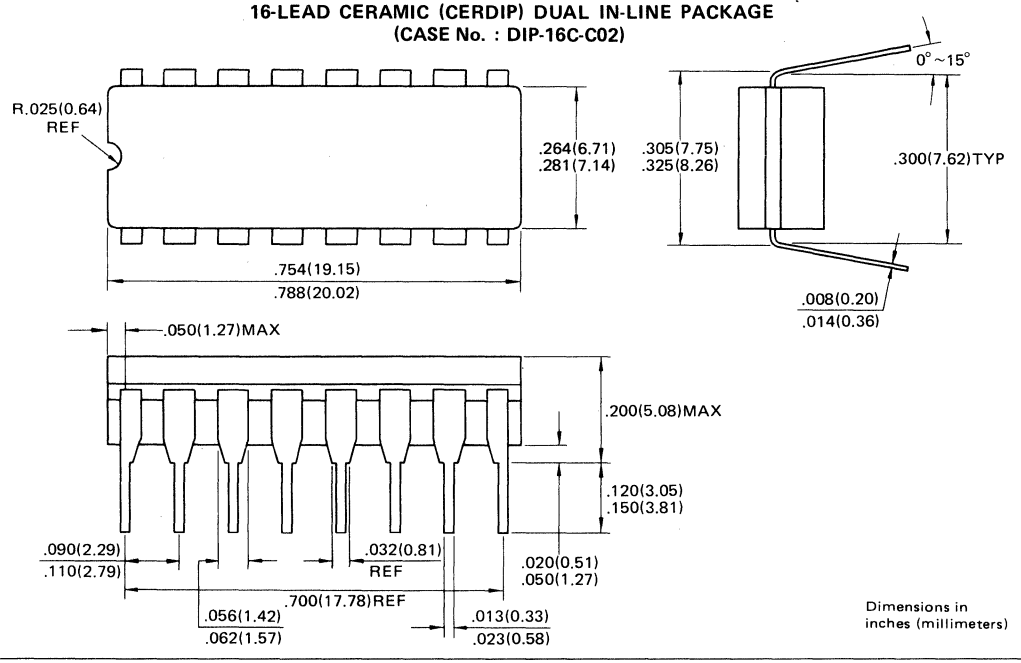
If the ramp time is counted with a 1 MHz clock, the following resolution is obtained.

$$\frac{1000\mu s}{1\mu s} = 1000 \fallingdotseq 2^{10}$$

7

PACKAGE DIMENSIONS

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)

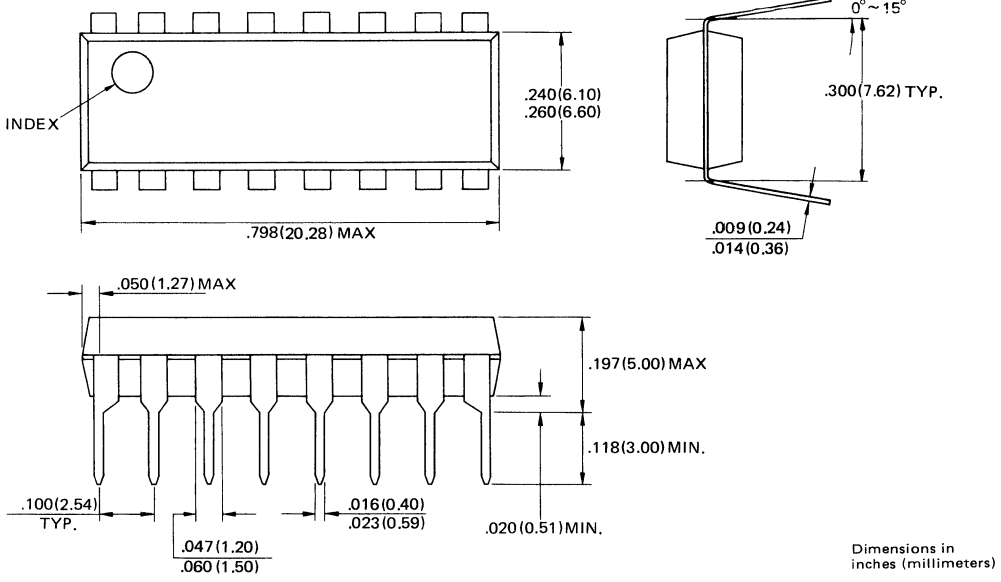


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M01)



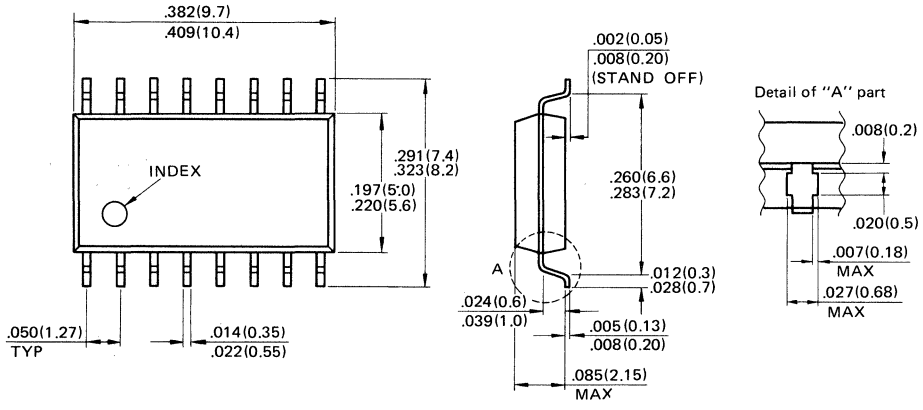
Dimensions in inches (millimeters)

7

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in inches (millimeters)

7

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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 0V2048-865C3

FUJITSU

8-CHANNEL 8-BIT A/D CONVERTER

MB4056

August 1988
Edition 2.1

8-CHANNEL 8-BIT A/D CONVERTER

The Fujitsu MB4056 is an analog-to-digital converter (ADC) for general purpose which features eight channels of analog inputs and 8-bit data length of digital output.

Analog input signal is converted to serial 8-bit digital data by the successive-approximation technique which provides high-speed conversion, i.e. many analog data can be converted within a short time.

Additionally, the MB4056 has dual range conversion capability, which provides sequentially one data of both range, standard and contracted modes, to chose better data between them and to delete the range change time.

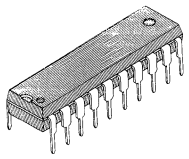
All digital I/O signals including control inputs are TTL level compatible so as to provide wide application such as in microprocessor-controlled system and so on.

- Single Power Supply: +4.75 V to +18 V
- Multiplex 8-Channel Analog Inputs:
- Resolution: 8 bits
- Linearity Error: ±0.19% Max.
- Analog Input Voltage Ranges:
  Automatic Range Change/Dual Range Conversion: 0 to 5 V Standard mode
  0 to 1.25 V Contracted mode
- Successive-Approximation Conversion: 100 μs/ch Max. at f_{CLK} = 100 kHz, S/D = 1
  200 μs/ch Max. at f_{CLK} = 100 kHz, S/D = 0
- Ratio-metric Conversion by Reference Voltage V_{REF}
- Analog Input Bias Current: 250 nA Max.
- TTL/CMOS Compatible Digital I/O
- Power Consumption: 160 mW Typ. at V_{CC} = 8V
- Standard 20-pin Plastic Package: Suffix: -P
  Standard 20-Pin Ceramic Package: Suffix: -Z

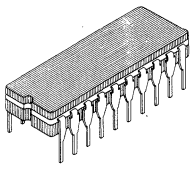
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+20	V
Digital Input Voltage		V_{IH}	+20	V
Digital Output Voltage (Off-State)		V_{OH}	+20	V
Analog Input Voltage		V_{IA}	+20	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic	T_{STG}	−40 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

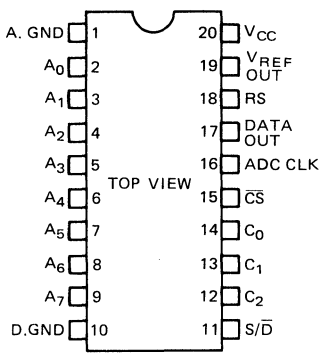


PLASTIC PACKAGE
DIP-20P-M01



CERAMIC PACKAGE
DIP-20C-C03

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1 – MB4056 BLOCK DIAGRAM

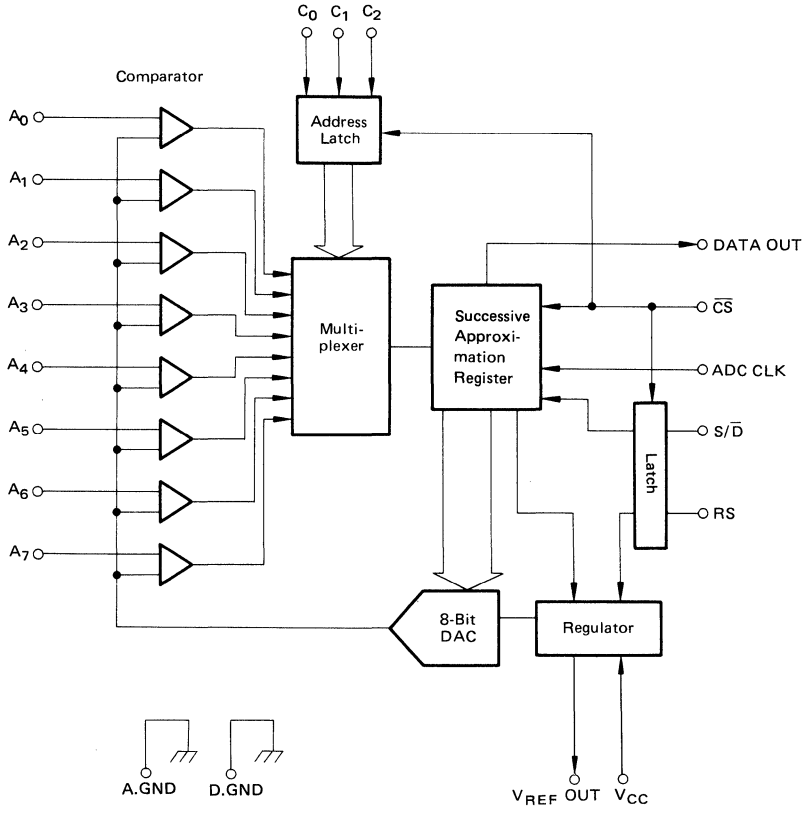


TABLE 1: CONVERSION MODES

S/$\overline{D}$	RS	1st Conversion	2nd Conversion
L	L	Contracted Range	Standard Range
L	H	Standard Range	Contracted Range
H	L	Contracted Range	–
H	H	Standard Range	–

TABLE 2: CHANNEL SELECTIONS

C_2	C_1	C_0	Channel
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

PIN DESCRIPTIONS

Pin Name	Pin No.	Descriptions
A_0 to A_7	2 to 9	**Analog Inputs** These inputs are provided to receive eight channels of analog inputs. One of them is selected by a combination of C_0 to C_2.
S/$\overline{D}$	11	**Conversion Mode Select Input** This control input is provided to select a conversion sequence with RS input as shown in Table 1. When low, analog input voltage is converted in both ranges, and when high, in one range only. This input is latched at the falling edge of $\overline{CS}$.
C_2 to C_0	12 to 14	**Channel Select Inputs** These inputs are used to select one of eight analog input as shown in Table 2. This inputs are latched at the falling edge of $\overline{CS}$.
$\overline{CS}$	15	**Chip Select Input** This control input is used to start analog to digital conversion and to terminate it. When $\overline{CS}$ goes low, the A/D conversion starts and the DATA OUTPUT is enabled. When the A/D conversion is completed or termination of the conversion is required, $\overline{CS}$ is made high.
ADC CLK	16	**A/D Conversion Clock** This clock signal is used for A/D conversion. The conversion speed is determined by this clock rate. But precise stability of the clock rate is no required.
DATA OUT	17	**Data Outputs** This output is provided to output the A/D conversion results as digital signals. The converted digital data are serially output in the order of start-bit, MSB (Most Significant Bit), 2SB (Second Significant Bit), . . . , 7SB, LSB (Least Significant Bit) and stop-bit in synchronous with the ADC CLK.
RS	18	**Range Select Input** This control input is provided to select an analog input voltage as shown in Table 1. This input is latched at the falling edge of $\overline{CS}$.
V_{REF}	19	**Reference Voltage Output** This output provides the regulated 5V when V_{CC} is between 8V and 18V. About 10mA current of the output is supplyed externally.
A. GND D. GND	1 10	Analog Ground Digital Ground
V_{CC}	20	Power Supply Voltage, 4.75V to 18V.

7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.75	12	18	V
Digital output Low Current	I_{OL}			8	mA
Ambient Operating Temperature	T_A	-40		+85	°C

ANALOG CIRCUIT CHARACTERISTICS

(V_{CC} = 4.75 to 18V, T_A = -40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Max	Typ	Max	
Resolution						8	bit
Linearity Error						±0.5	LSB
Differential Linearity Error						±0.9	LSB
Zero Transition Voltage		V_{ZS}	Standard Conversion Mode $8V \leq V_{CC} \leq 18V$		20		mV
Full Scale Transition Voltage		V_{FS}			4980		mV
Zero Transition Voltage		V_{ZC}	Contracted Conversion Mode $4.75V \leq V_{CC} \leq 18V$		5		mV
Full Scale Transition Voltage		V_{FC}			1245		mV
Comparator Input Current		I_{COP}				-250	nA
Regulator	Output Voltage		$8V \leq V_{CC} \leq 18V$	4.5	5.0	5.5	V
	Line Regulation		$8V \leq V_{CC} \leq 18V$		4.0		mV/V
	Load Regulation		V_{CC} = 12V $-10mA \leq I_{OUT} \leq 0mA$		0.5		mV/mA
	Output Voltage Change with Temperature		V_{CC} = 12V		50		PPm/°C
Conversion Time		t_{CYC1}	f_{CLK} = 100kHz, S/D = "1"			100	μs/CH
		t_{CYC0}	f_{CLK} = 100kHz, S/D = "0"			200	μs/CH

DIGITAL CIRCUIT DC CHARACTERISTICS

(V_{CC} = 4.75 to 18V, T_A = −40 to 85°C)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input High Voltage	V_{IH}			2.0			V
Input Low Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IC}	I_{IL} = −18mA				−1.5	V
Output High Current	I_{OH}	V_{IH} = 2V, V_{IL} = 0.8V V_{OH} = 20V				100	μA
Output Low Voltage	V_{OL}	V_{IH} = 2V V_{IL} = 0.8V	I_{OL} = 4mA			0.4	V
			I_{OL} = 8mA			0.5	V
Input High Current	I_{IH}	V_{IH} = 2.7V				20	μA
		V_{IH} = 20V				100	μA
Input Low Current	I_{IL}	V_{IL} = 0.4V			−20	−100	μA
Power Supply Current	I_{CC}	V_{CC} = 20V			20	38	mA

DIGITAL CIRCUIT AC CHARACTERISTICS

(V_{CC} = 4.75 to 18V, T_A = −40 to 85°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
ADC CLK Cycle Time	t_{CY}	10			μs
ADC CLK H level Pulse Width	$t_{WAC}{}^{+}$	2.5			μs
ADC CLK L level Pulse Width	$t_{WAC}{}^{-}$	2.5			μs
$\overline{CS}$ H level Pulse Width	$t_{WCS}{}^{+}$	1.5			μs
$\overline{CS}$ Set-up Time	t_{SCS}	1			μs
$\overline{CS}$ Hold Time	t_{HCS}	1			μs
Channel Set-up Time	t_{SCH}	0			μs
Channel Hold Time	t_{HCH}	1.5			μs
Propagation Delay Time	t_{PLH}		0.8	2	μs
	t_{PHL}		0.8	2	μs

7

Fig. 2 – AC MEASUREMENT CIRCUIT

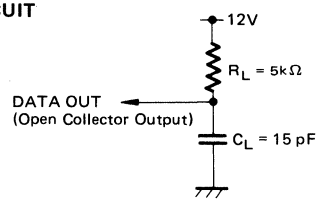


Fig. 3 – AC TIMING DIAGRAM

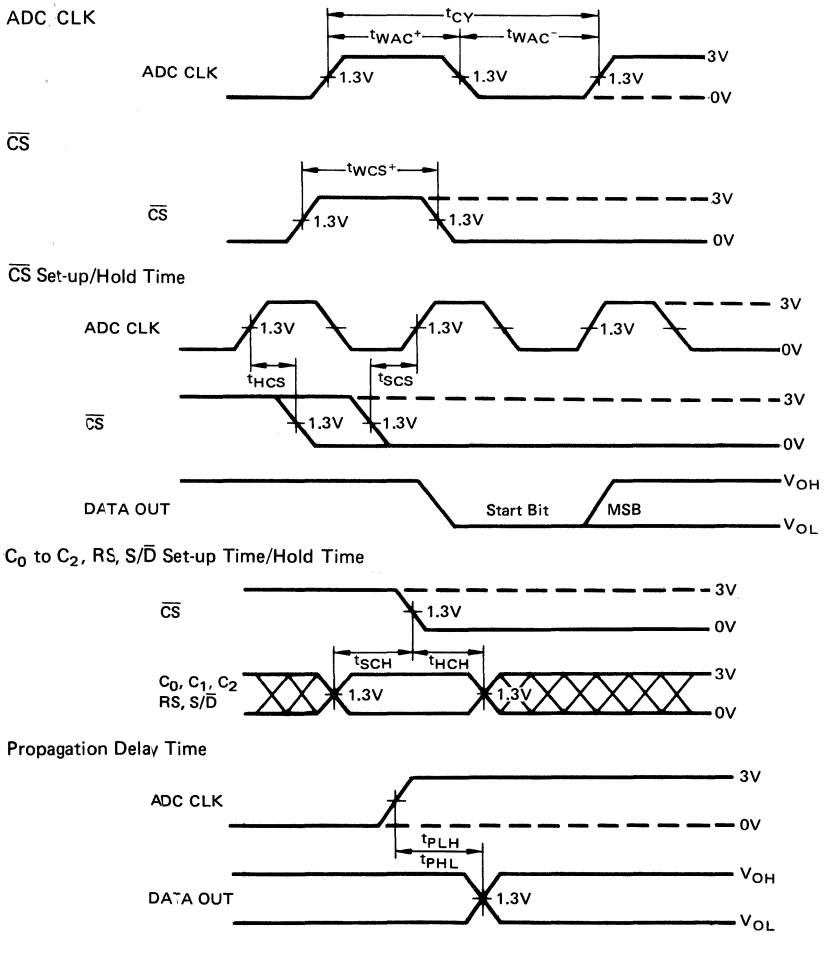


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Fig. 4 – TIMING DIAGRAM (S/$\overline{D}$ = "0")

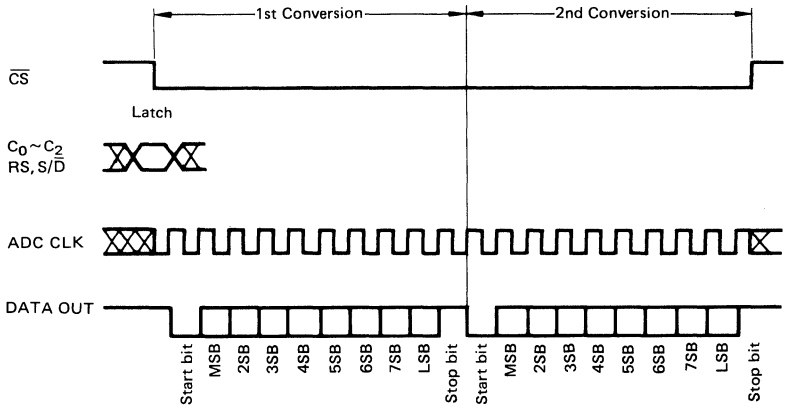
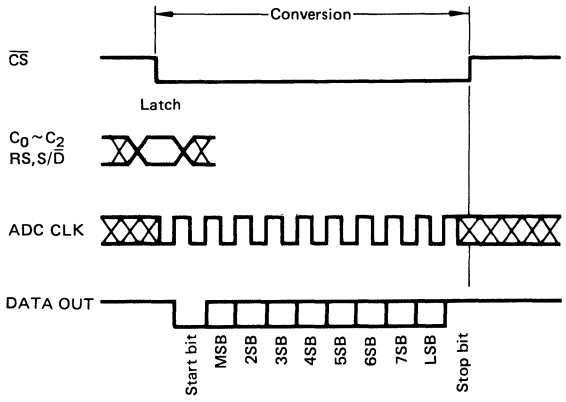


Fig. 5 – TIMING DIAGRAM (S/$\overline{D}$ = "1")



7

TYPICAL CHARACTERISTICS CURVES

Fig. 6 – ALLOWABLE V_{REF} OUT PIN OUTPUT CURRENT vs. POWER SUPPLY VOLTAGE

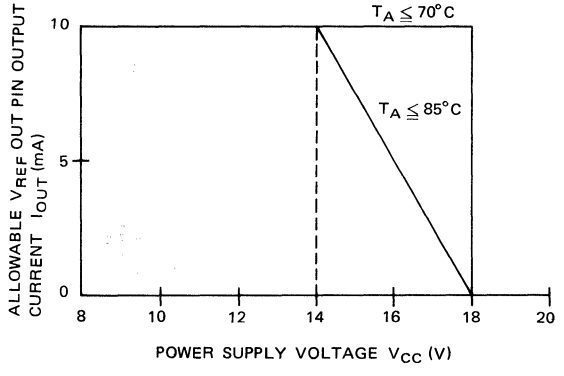
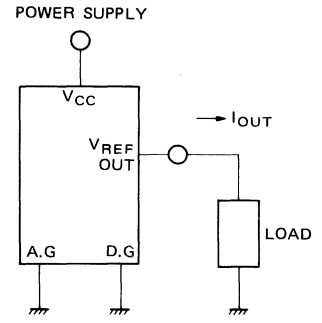


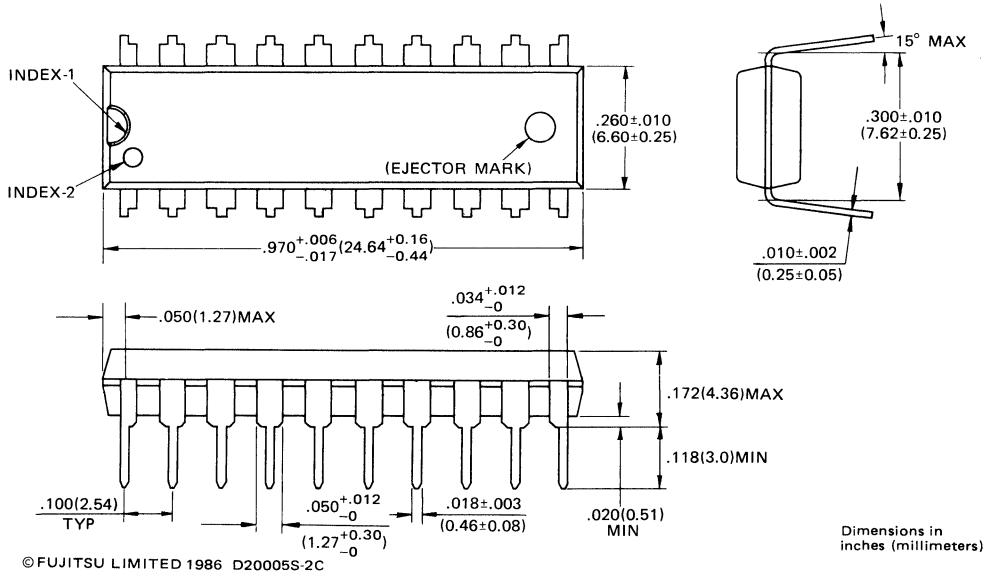
Fig. 7 – MEASUREMENT CIRCUIT



7

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)

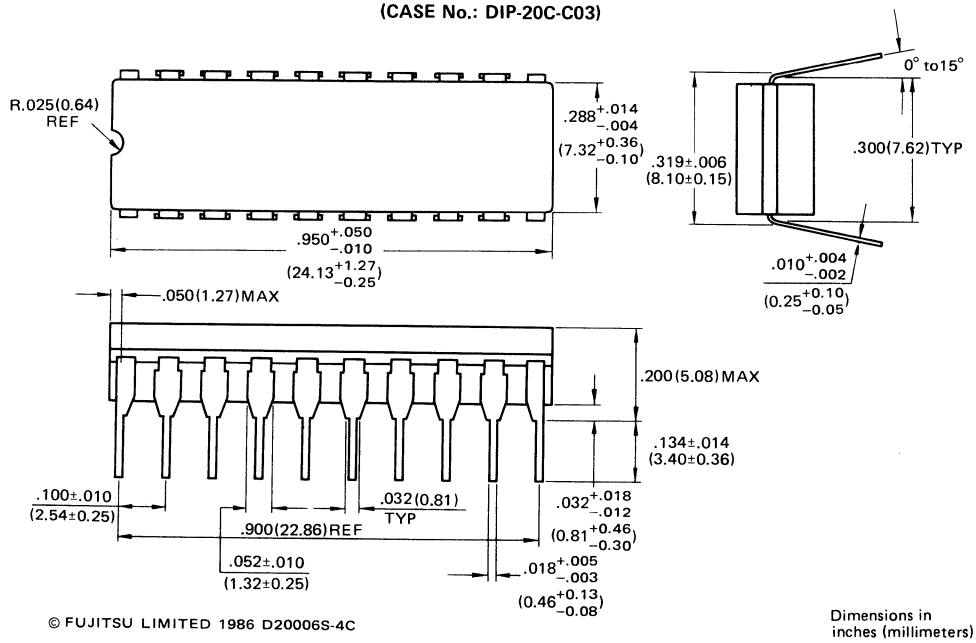


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS (continued)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimensions in
inches (millimeters)

7

FUJITSU

8-BIT ULTRA-HIGH SPEED A/D CONVERTER

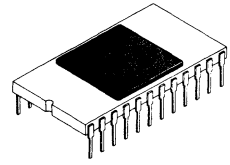
MB 40547-7
MB 40547-8

May 1984
Edition 2.0

8-BIT ULTRA HIGH SPEED A/D CONVERTER

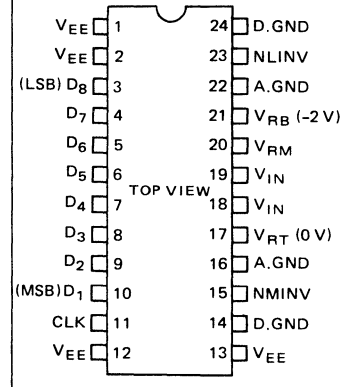
The Fujitsu MB 40547 is an ultra-high A/D converter which is fabricated with Fujitsu Advanced Bipolar Technology. The MB 40547 uses the full-parallel comparision technique (flash method) for high speed conversion and can convert wide-band analog signals such as video to digital signals at a sampling rate from DC to 30 Megasamples/sec. without any sampling/holding circuit. Because of such high-speed operation, the MB 40547 is suitable for applications such as color-TV coding, video processing with computer, or radar signal processing.

- Resolution: 8 bits
- Linearity: MB 40547-7 : ±1 LSB
  MB 40547-8 : ±1/2 LSB
- Conversion Rate: 30 MSPS typ.
- Analog Input Voltage: 0 to -2 V
- No need for external sampling/holding circuit
- Digital I/O level: 10 K ECL level
- Output modes: Binary/2's Complement
- Single Power Supply: -5.2 V
- Power consumption: 900 mW typ.
- Package: Standard 24-pin DIP



CERAMIC PACKAGE
DIP-24C-A01

PIN ASSIGNMENT



7

ABSOLUTE MAXIMUM RATINGS

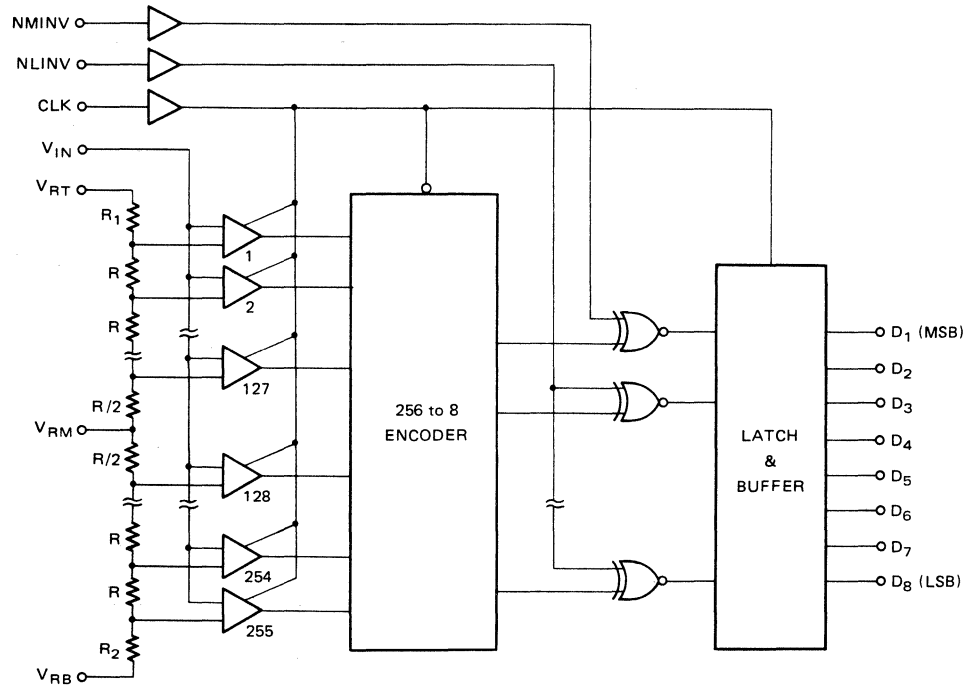
Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{EE}	+0.5 to -7.0	V
Digital Input Voltage	V_{IND}	+0.5 to V_{EE}	V
Analog Input Voltage	V_{INA}	+0.5 to V_{EE}	V
Analog Reference Voltage	V_R	+0.5 to V_{EE}	V
Output Current	I_O	-12*	mA
Storage Temperature	T_{STG}	-55 to +150	°C

* Negative value of current means that the current flows from the device.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{EE}	-5.46	-5.20	-4.94	V
Analog Input Voltage	V_{INA}	-2.0		0	V
Analog Reference Voltage (Top Side)	V_{RT}		0	0.1	V
Analog Reference Voltage (Bottom Side)	V_{RB}	-2.1	-2.0		V
Clock Pulse Width at High level	t_w+	25			ns
Clock Pulse Width at Low level	t_w-	25			ns
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = 0 to +70°C, Output Circuits: See TEST LOAD CIRCUIT)

Parameter		Symbol	Value			Unit
			Max	Typ	Max	
Resolution					8	bits
Linearity Error	MB 40547-7	E_R			±0.4	%
	MB 40547-8				±0.2	
Equivalent Input Resistance		R_{INA}	25			kΩ
Input Capacitance		C_{INA}		130	250	pF
High-level Input Current		I_{IHA}			300	μA
Low-level Input Current		I_{ILA}			290	μA
Reference Current		I_{RB}	-36	-20		mA

AC CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = 0 to +70°C, Output Circuit: See TEST LOAD CIRCUIT)

Parameter	Symbol	T_A (°C)	Value			Unit
			Min	Typ	Max	
High-level Output Voltage	V_{OH}	0	-1.000		-0.840	V
		+25	-0.960		-0.810	
		+70	-0.900		-0.720	
Low-level Output Voltage	V_{OL}	0	-1.870		-1.665	V
		+25	-1.850		-1.650	
		+70	-1.830		-1.625	
High-level Input Voltage	V_{IHD}	0	-1.145			V
		+25	-1.105			
		+70	-1.045			
Low-level Input Voltage	V_{ILD}	0			-1.490	V
		+25			-1.475	
		+70			-1.450	
High-level Input Current	I_{IHD}				220	μA
Low-level Input Current	I_{ILD}				180	μA
Power Supply Current	I_{EE}		-280	-170		mA

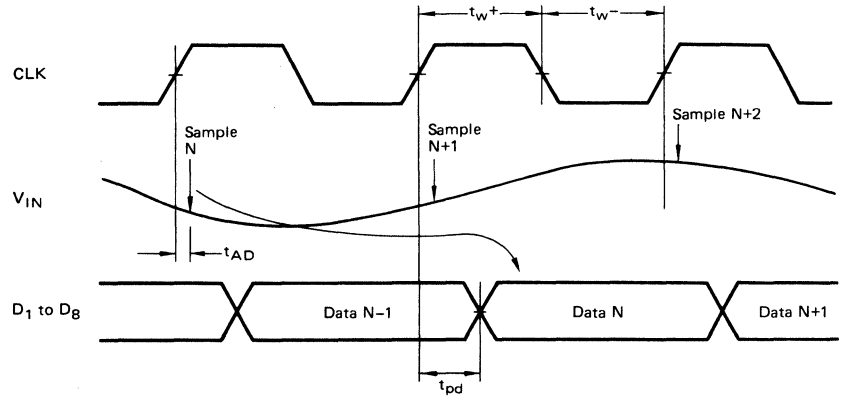
7

SWITCHING CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = +25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Maximum Conversion Rate	FS	20	30		MHz
Aperture Delay	t_{AD}				ns
Digital Output Delay	t_{pd}		15	25	ns

TIMING DIAGRAM



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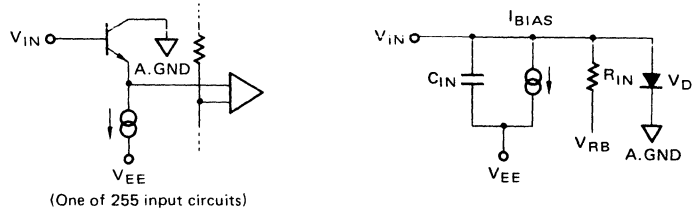
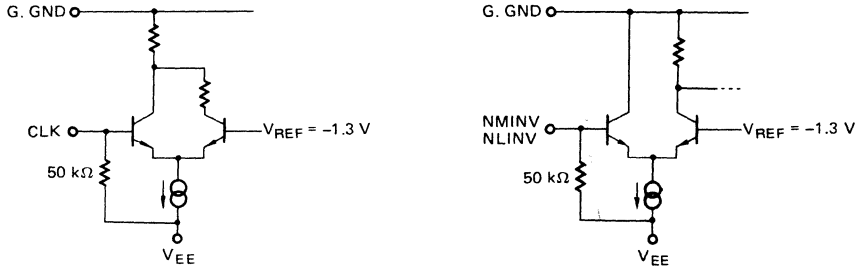
ANALOG INPUT EQUIVALENT CIRCUIT

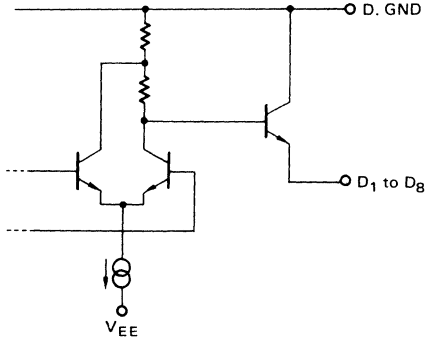


C_{IN}: Non-linear Emitter-follower Junction Capacitance
R_{IN}: Linear Resistance Model for Input Current Transition by Comparator Switching:
Infinite value for $V_{IN} < V_{RB}$ or when CLK = HIGH.
V_{RB}: Voltage at V_{RB} Terminal.
I_{BIAS}: Constant Input Bias Current
V_D: Diode consisting of the base-collector junction of emitter-follower transistor.

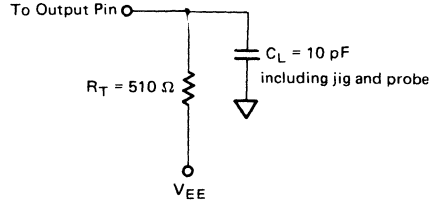
DIGITAL INPUT EQUIVALENT CIRCUIT



DIGITAL OUTPUT EQUIVALENT CIRCUIT



TEST LOAD CIRCUIT



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OUTPUT CODES

(Recommended Operating Conditions unless Otherwise noted, $V_{RT} \fallingdotseq 0V$, $V_{RD} = -1{,}000V$, Positive Logic)

STEP	RANGE		BINARY		OFFSET 2'S COMPLEMENT	
	-2.0000 V FS 7.8431 mV Step*1 (V)	-2.0000 V FS 8.000 mV Step*1 (V)	TRUE NMINV = 1 NLINV = 1	INVERTED NMINV = 0 NLINV = 1	TRUE NMINV = 0 NLINV = 0	INVERTED NMINV = 1 NLINV = 0
000	0.0000	0.0000	00000000	11111111	10000000	01111111
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	-0.9961	-1.0160	01111111	10000000	11111111	00000000
128	-1.0039	-1.0240	10000000	01111111	00000000	11111111
129	-1.0118	-1.0320	10000001	01111110	00000001	11111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
255	-2.0000	-2.0400	11111111	00000000	01111111	10000000

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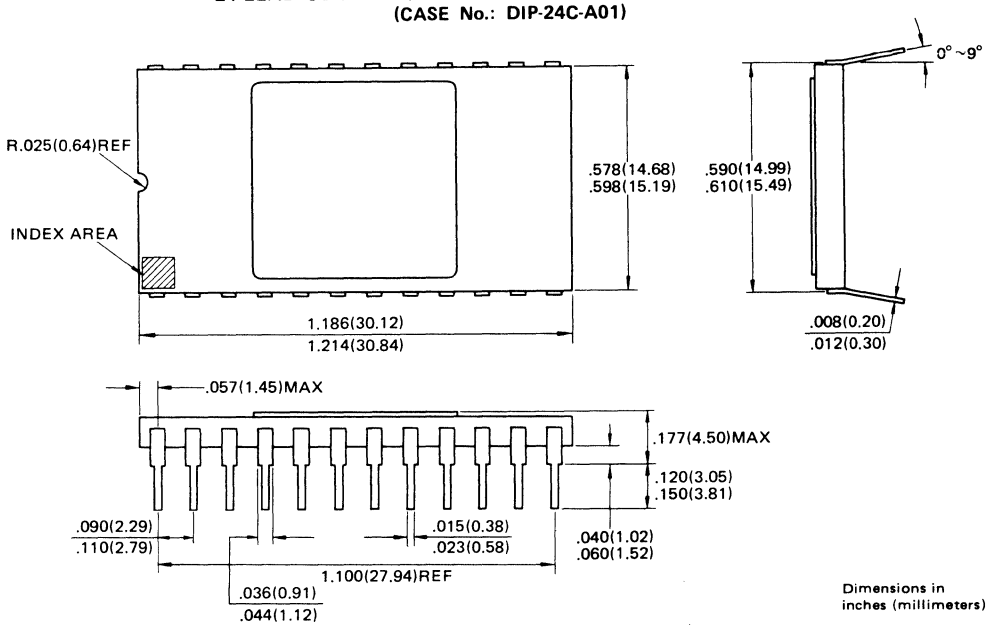
Note *1: Value of analog voltage is defined as value at the center of the step.

PACKAGE DIMENSIONS

24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-A01)



7

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

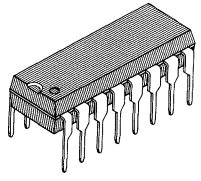
6-BIT ULTRA-HIGH SPEED VIDEO A/D CONVERTER

MB40576

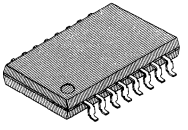
April 1988
Edition 3.0

6-BIT ULTRA HIGH SPEED VIDEO A/D CONVERTER

The Fujitsu MB 40576 is a low power ultra-high speed video A/D converter fabricated with Fujitsu Advanced Bipolar Technology. The MB 40576 also adopts the fully-parallel comparison technique (flash method) for high speed convertion and can convert wide band analog signal such as video signal to digital signal at a sampling rate of DC through 20 Mega-samples/sec. Because of such high-speed operation, the MB 40576 is suitable for digital video applications such as the digital TV, video processing with computer, or radar signal processing.



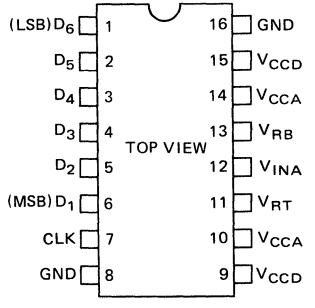
PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M03

- Resolution: 6 bits
- Linearity Error: ±0.8%
- Maximum Conversion Rate: 20 MSPS min.
- Analog Input Voltage: V_{CC} to V_{CC} −2V
- Analog Input Dynamic Range: 1 V
- Digital I/O level: TTL
- Single Power Supply: +5 V
- Power Dissipation: 270 mW typ.
- Package: Standard 16-pin DIP Package (Suffix: -P)
  Standard 16-pin FLAT Package (Suffix: -PF)

PIN ASSIGNMENT



7

ABSOLUTE MAXIMUM RATINGS (See NOTE)

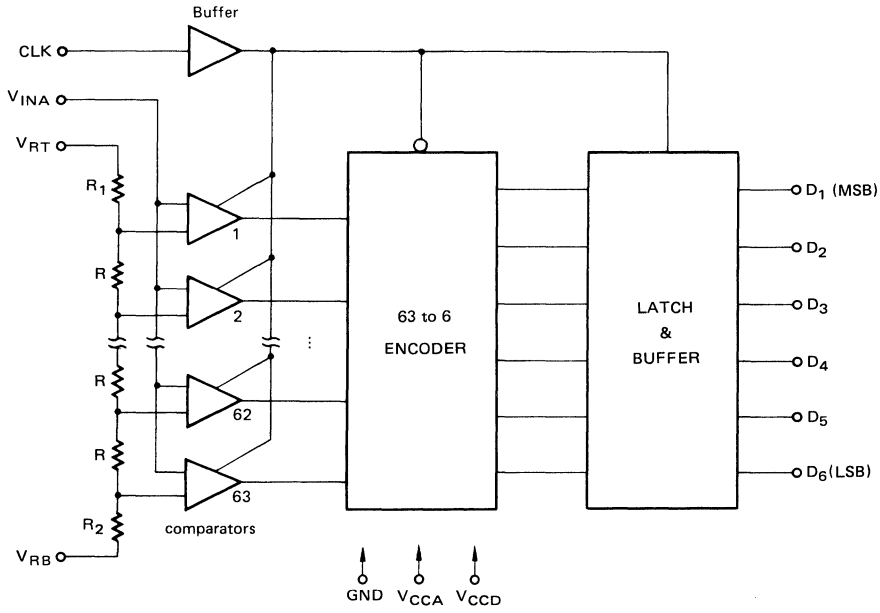
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	-0.5 to +7.0	V
Digital Input Voltage	V_{IND}	-0.5 to +7.0	V
Analog Input Voltage	V_{INA}	-0.5 to V_{CC} + 0.5	V
Analog Reference Voltage	V_{RT}, V_{RB}*	-0.5 to V_{CC} + 0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

* $| V_{RT} - V_{RB} | < 2V$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB40576 BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA} V_{CCD}	4.75	5.00	5.25	V
Analog Input Voltage*	V_{INA}	4		5	V
Analog Reference Voltage (Top side)*	V_{RT}	4	5	5.1	V
Analog Reference Voltage (Bottom side)*	V_{RB}	3	4	4.1	V
Digital High-level Output Current	I_{OHD}	-400			μA
Digital Low-level Output Current	I_{OLD}			4	mA
Clock Pulse Width at High level	t_{w+}	25			ns
Clock Pulse Width at Low level	t_{w-}	25			ns
Operating Temperature	T_A	0		70	°C

NOTE: * $V_{RB} < V_{INA} < V_{RT}$, $V_{RT} - V_{RB} = 1\ V \pm 0.1\ V$
Please keep V_{CCA} and V_{CCD} at the same potential.

7

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution	–				6	bits
Linearity Error	LE	DC			±0.8	%
Equivalent Analog Input Resistance	R_{INA}		100			KΩ
Input Capacitance	C_{INA}			35	65	pF
High-Level Input Current	I_{IHA}				75	μA
Low-Level Input Current	I_{ILA}				73	μA
Reference Current	I_{RB}	V_{RT} = 5 V V_{RB} = 4 V		4	7.2	mA

7

DIGITAL DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Output Voltage	V_{OHD}	I_{OHD} = –400 μA	2.7			V
Low-level Output Voltage	V_{OLD}	I_{OLD} = 1.6 mA			0.4	V
High-level Input Voltage	V_{IHD}		2			V
Low-level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{ID} = 7 V			100	μA
High-level Input Current	I_{IHD}	V_{IHD} = 2.7 V		0	20	μA
Low-level Input Current	I_{ILD}	V_{ILD} = 0.4 V	–400	-40		μA
Power Supply Current	I_{CC}			54	80	mA

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING CHARACTERISTICS

(V_{CC} = 5 V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		20	30		MSPS
Digital Output Delay Time	t_{pd}		5	18	40	ns

TIMING DIAGRAM

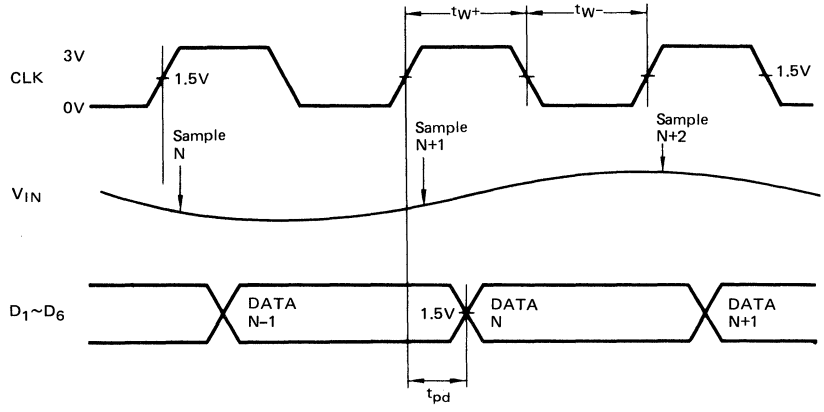

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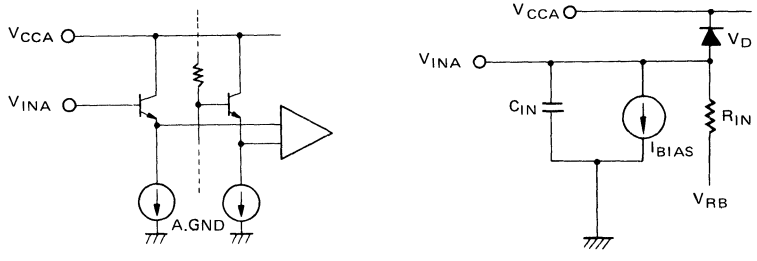
Fig. 2 – ANALOG INPUT EQUIVALENT CIRCUIT



C_{INA}: Non-linear Emitter-follower Junction Capacitance
R_{INA}: Linear Resistance Model for Input Current Transition by Comparator Switching:
Infinit value for $V_{INA} < V_{RB}$ or when CLK = High
V_{RB}: Voltage at V_{RB} terminal.
I_{BIAS}: Constant Input Bias Current
V_D: The base-collector junction diode of emitter-follower transistor.

Fig. 3– DIGITAL INPUT EQUIVALENT

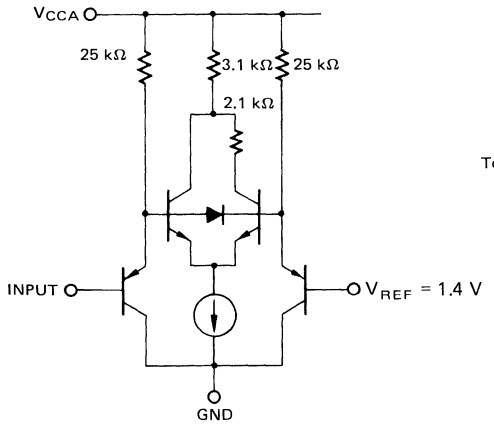
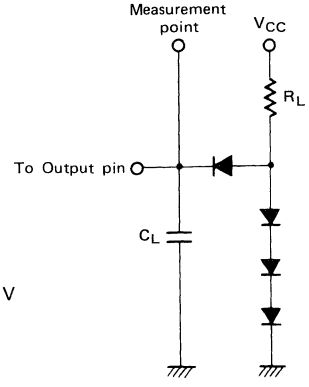


Fig. 4 – LOAD CIRCUIT FOR OUTPUT BUFFER



$R_L = 2k\Omega$
C_L = 15pF including scope and jig capacitance
Diodes : IN 3064 or equivalent.

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OUTPUT CODE

(V_{CC} = 5 V, $V_{RT} \fallingdotseq V_{RB} \fallingdotseq$ 4 V)

Step	Analog Input Voltage	Digital Output Code
0	3.992 V	000000
1	4.008 V	000001
⋮	⋮	⋮
31	4.488 V	011111
32	4.504 V	100000
33	4.520 V	100001
⋮	⋮	⋮
62	4.984 V	111110
63	5.000 V	111111

NOTE: One step of output voltage (I_{LSB}) is 16 mV when V_{FT} is adjusted at 4.992V, and V_{ZT} at 4.000 V by V_{RT} and V_{RB}.
The Analog Input Voltage are the centre value of each step.

Fig. 5 – IDEAL CONVERSION CHARACTERRISTICS

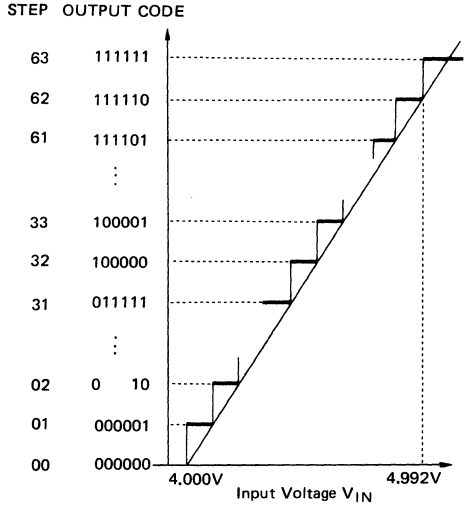
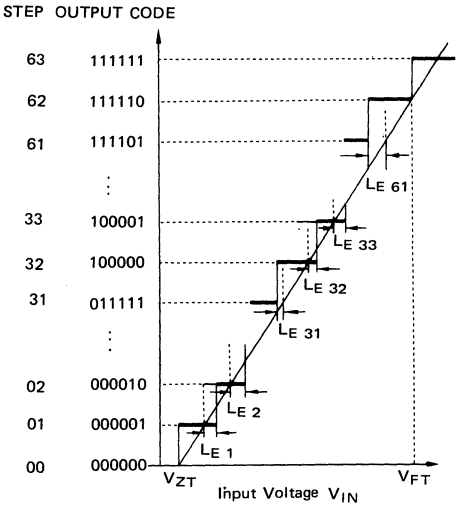


Fig. 6 – PRACTICAL CONVERSION CHARACTERISTICS



$$\text{Linearity Error} = \frac{|\,LEn\,|\,max.}{|\,FS\,|}$$

TYPICAL CHARACTERISTICS CURVES

Fig. 7 – POWER SUPPLY CURRENT vs. TEMPERATURE

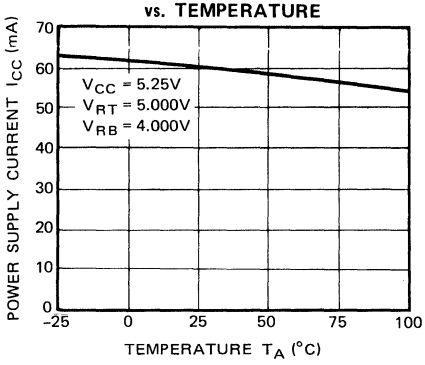


Fig. 8 – LINEARITY ERROR vs. TEMPERATURE

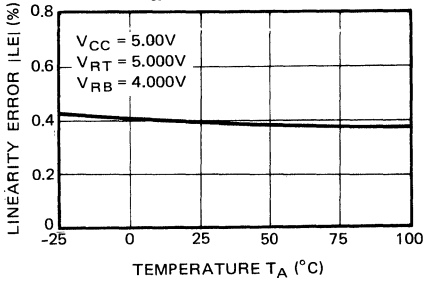


Fig. 9 – REFERENCE CURRENT vs. TEMPERATURE

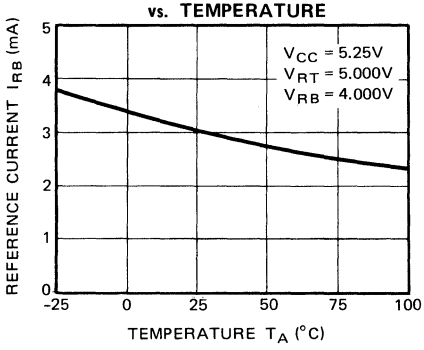


Fig. 10 – DIGITAL HIGH-LEVEL OUTPUT VOLTAGE vs. TEMPERATURE

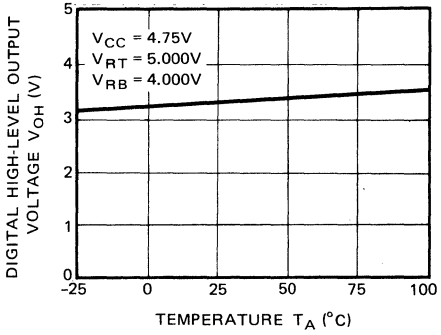
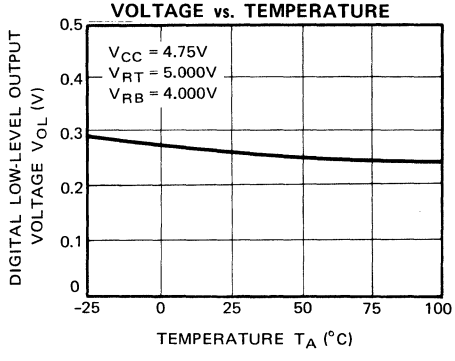


Fig. 11 – DIGITAL LOW-LEVEL OUTPUT VOLTAGE vs. TEMPERATURE



7

Fig. 12 – DELAY TIME vs. TEMPERATURE

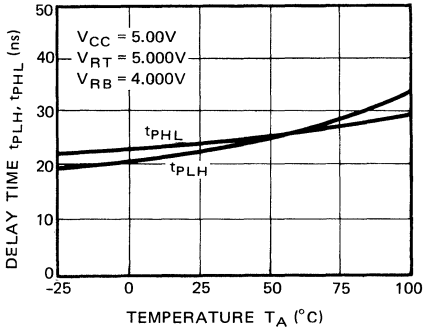


Fig. 13 – DELAY TIME vs. POWER SUPPLY VOLTAGE

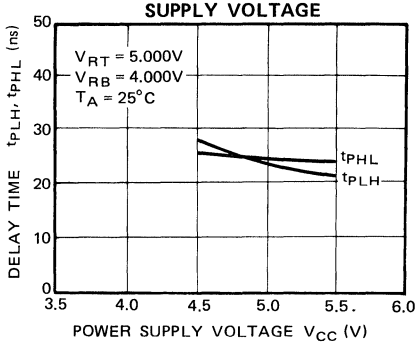


Fig. 14 – CLOCK PULSE WIDTH vs. TEMPERATURE

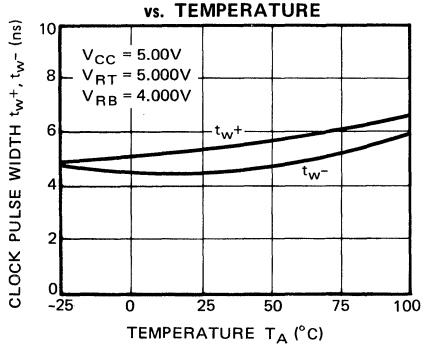


Fig. 15 – CLOCK PULSE WIDTH vs. POWER SUPPLY VOLTAGE

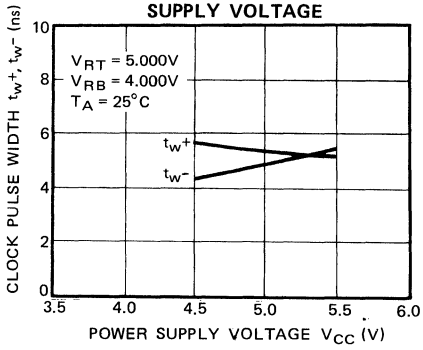
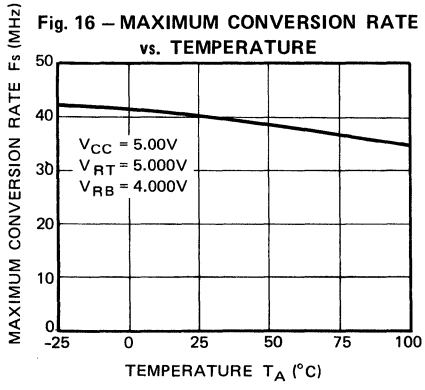
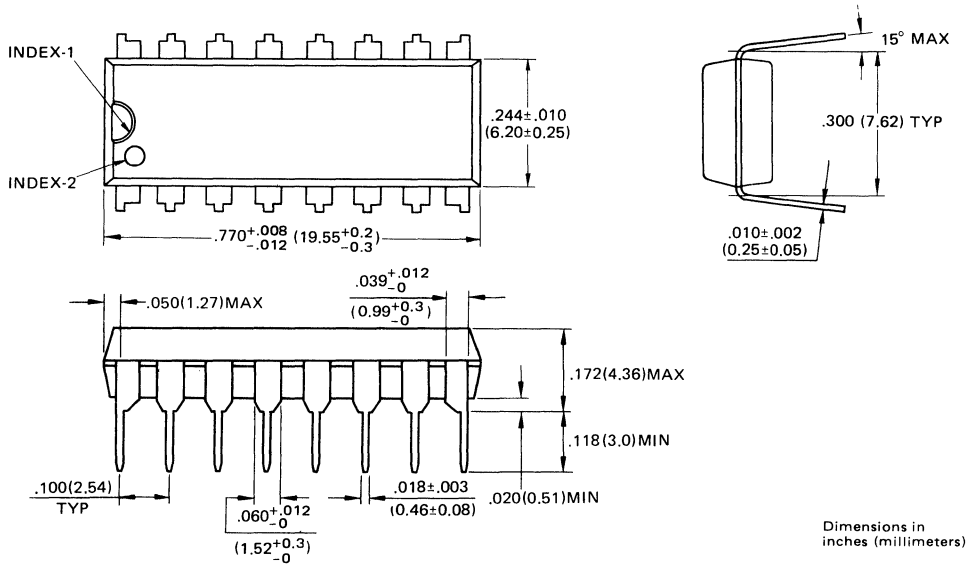


Fig. 16 – MAXIMUM CONVERSION RATE vs. TEMPERATURE



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)

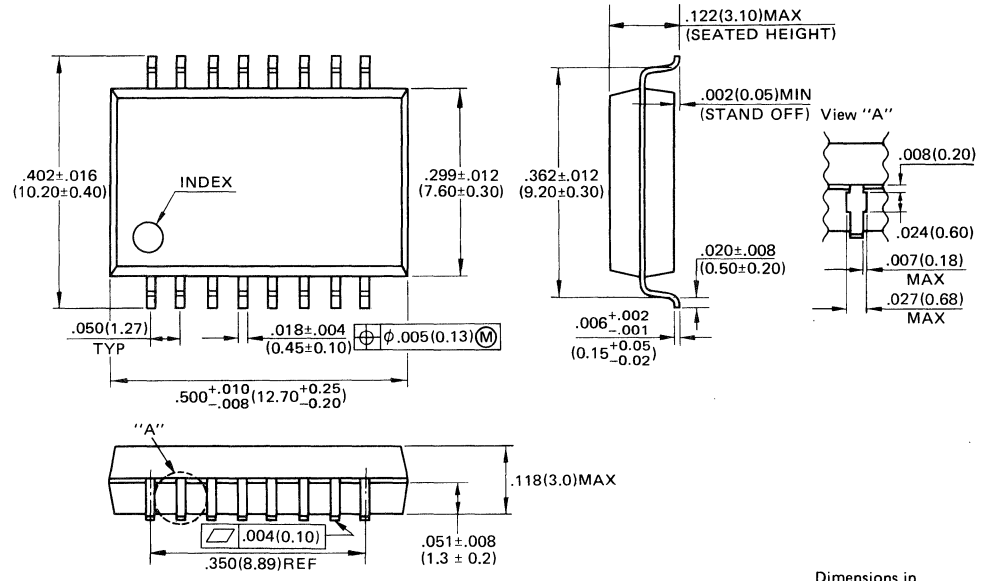


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS (continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M03)



Dimensions in
inches (millimeters)

7

FUJITSU

8-BIT ULTRA-HIGH SPEED VIDEO A/D CONVERTER

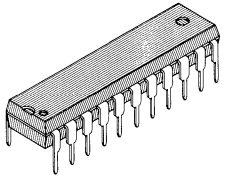
MB40578
MB40578-7

March 1988
Edition 2.0

8-BIT ULTRA HIGH SPEED VIDEO A/D CONVERTER

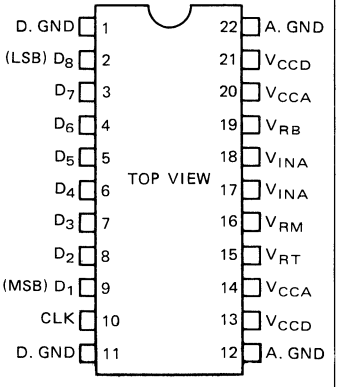
The Fujitsu MB 40578 is a low power ultra-high speed video A/D converter fabricated with Fujitsu Advanced Bipolar Technology. The MB 40578 also adopts the fully-parallel comparison technique (flash method) for high speed conversion and can convert wide band analog signal such as video signal to digital signal at a sampling rate of DC through 20 Mega-samples/sec. Because of such high-speed operation, the MB 40578 is suitable for digital video applications such as the digital TV, video processing with computer, or radar signal processing.

- Resolution: 8 bits
- Linearity Error: ±0.2% (MB40578)
  ±0.4% (MB40578-7)
- Maximum Conversion Rate: 20 MSPS min.
- Analog Input Voltage: 3.0V to 5.0V
- Digital I/O level: TTL
- Single Power Supply: +5V
- Power Dissipation: 480 mW typ.
- Package: Standard 22-pin DIP Package : Suffix : -P



PLASTIC PACKAGE
DIP-22P-M04

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

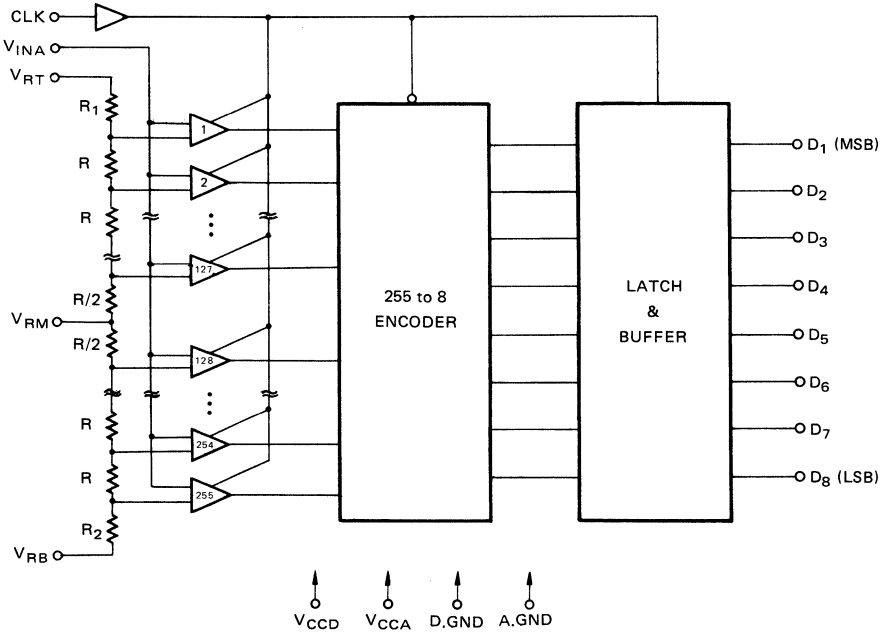
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	−0.5 to +7.0	V
Digital Input Voltage	V_{IND}	−0.5 to +7.0	V
Analog Input Voltage	V_{INA}	−0.5 to V_{CC}+0.5	V
Analog Reference Voltage	V_{RT}, V_{RB}	−0.5 to V_{CC}+0.5	V
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1 – MB 40578 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage *1	V_{CCA} V_{CCD}	4.75	5.00	5.25	V
Analog Input Voltage *2	V_{INA}	3		5	V
Analog Reference Voltage (Top side) *2	V_{RT}		5	5.1	V
Analog Reference Voltage (Bottom side) *2	V_{RB}	2.9	3		V
Digital High-level Output Current	I_{OHD}	-400			μA
Digital Low-level Output Current	I_{OLD}			4	mA
Clock Pulse Width at High Level	t_w^+	25			ns
Clock Pulse Width at Low Level	t_w^-	25			ns
Operating Temperature	T_A	0		70	°C

NOTE: *1 Please keep V_{CCA} and V_{CCD} at the same potential.
*2 $V_{RB} < V_{INA} < V_{RT}$, $V_{RT} - V_{RB} = 2V \pm 0.1V$.

7

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Resolution		–				8	bits
Linearity Error	MB40578	LE	DC			±0.2	%
	MB40578-7					±0.4	
Equivalent Analog Input Resistance		R_{INA}		50			KΩ
Analog Input Capacitance		C_{INA}			120	230	pF
Analog High-Level Input Current		I_{IHA}				150	μA
Analog Low-Level Input Current		I_{ILA}				145	μA
Reference Current		I_{RB}	V_{RT} = 5 V V_{RB} = 3 V	−15	−9		mA

7

DIGITAL DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-Level Output Voltage	V_{OHD}	I_{OH} = −400 μA	2.7			V
Low-Level Output Voltage	V_{OLD}	I_{OL} = 1.6 mA			0.4	V
High-Level Input Voltage	V_{IHD}		2			V
Low-Level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{ID} = 7 V			100	μA
High-Level Input Current	I_{IHD}	V_{IHD} = 2.7 V		0	20	μA
Low-Level Input Current	I_{ILD}	V_{ILD} = 0.4 V	−400	−40		μA
Power Supply Current	I_{CC}			92	160	mA

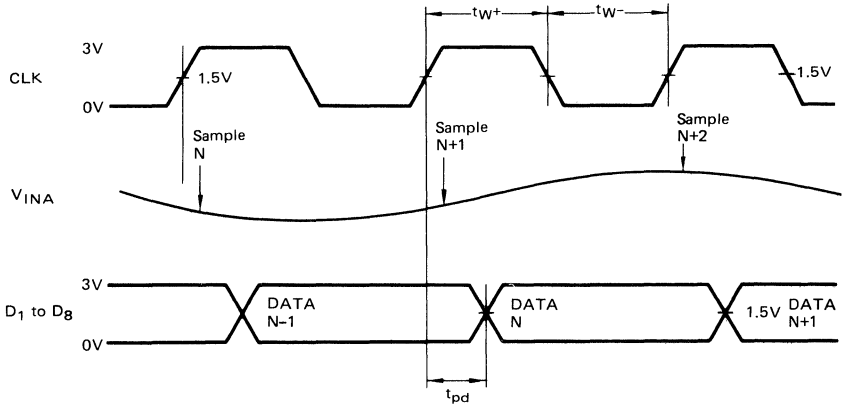
ELECTRICAL CHARACTERISTICS (continued)

SWITCHING CHARACTERISTICS

(V_{CC} = 5 V, T_A = 25°C)

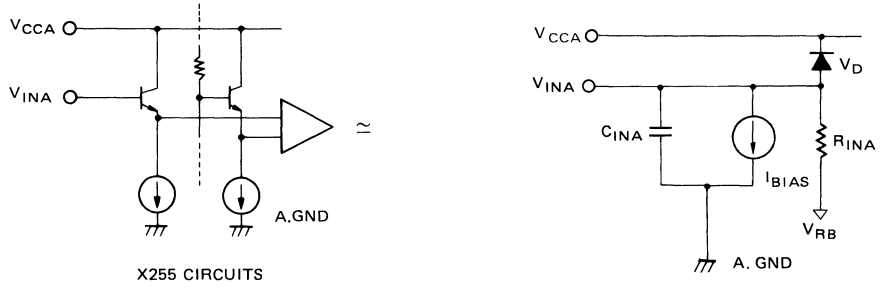
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		20	30		MSPS
Digital Output Delay Time	t_{pd}		5	15	40	ns

TIMING DIAGRAM



7

Fig. 2 – ANALOG INPUT EQUIVALENT CIRCUIT



C_{INA} : Non-linear Emitter-follower Junction Capacitance
R_{INA} : Linear Resistance Model for Input Current Transition by Comparator Switching:
Infinite value for $V_{IN} < V_{RB}$ or when CLK = High
V_{RB}: Voltage at V_{RB} terminal
I_{BIAS}: Constant Input Bias Current
V_D: The base-collector junction diode of emitter-follower transistor.

7

Fig. 3 – DIGITAL INPUT EQUIVALENT

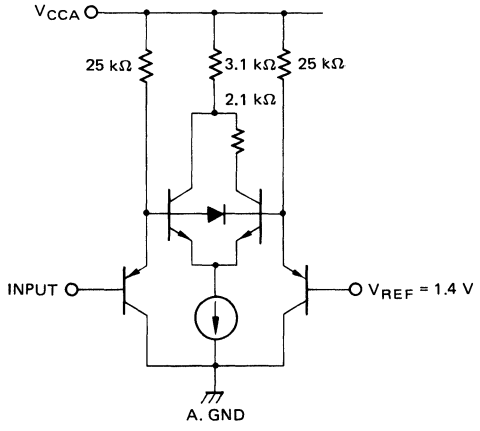
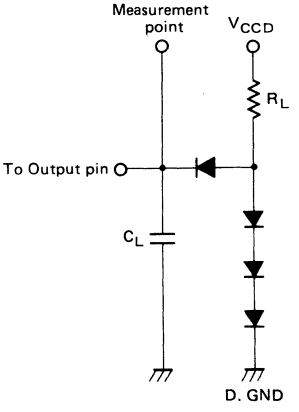


Fig. 4 – LOAD CIRCUIT FOR OUTPUT BUFFER



Note: $R_L = 2k\Omega$
C_L = 15pF including scope and jig capacitance
Diodes: IN3064 or equivalent

OUTPUT CODE

(V_{CC} = 5.0 V, V_{RT} ≒ 5.0V, V_{RB} ≒ 3.0V)

Step	Analog Input Voltage	Digital Output Code
0	2.960 V	00000000
1	2.968 V	00000001
⋮	⋮	⋮
127	3.976 V	01111111
128	3.984 V	10000000
129	3.992 V	10000001
⋮	⋮	⋮
254	4.992 V	11111110
255	5.000 V	11111111

Note: Ajust V_{ZT} = 2.964 V and V_{FT} = 4.996 V with V_{RT} and V_{RB}. The Analog Input Voltage are the center values of each step.

Fig. 5 — IDEAL CONVERSION CHARACTERISTICS

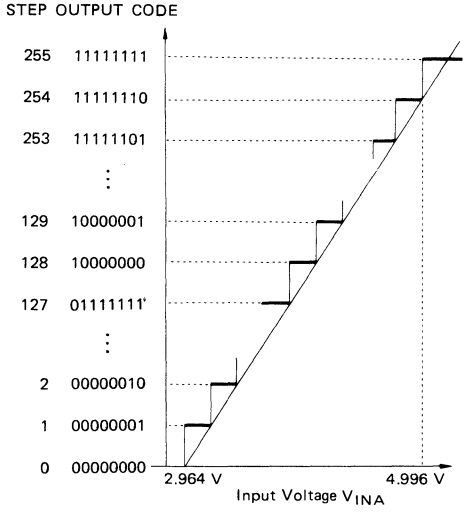
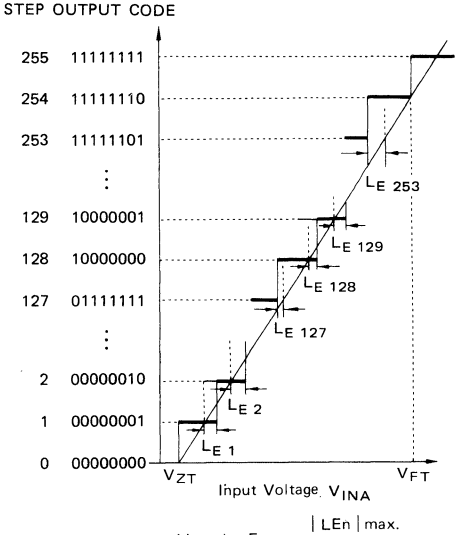


Fig. 6 — PRACTICAL CONVERSION CHARACTERISTICS

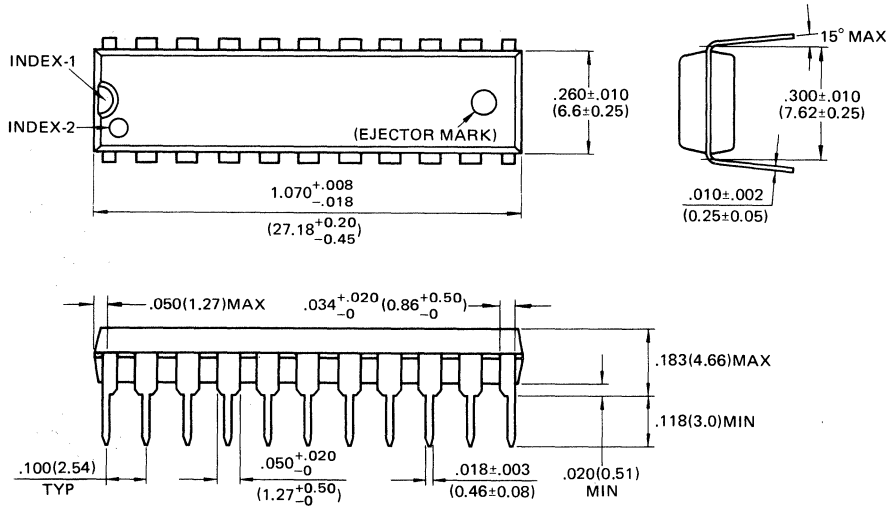


$$\text{Linearity Error} = \frac{|LEn|_{max.}}{|FS|}$$

7

PACKAGE DIMENSIONS

22-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-22P-M04)



Dimensions in
inches (millimeters)

7

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Printed in Japan 0V0001-883A2

FUJITSU

8-BIT MULTIPLYING D/A CONVERTER

MB 4072

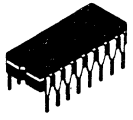
April 1984
Edition 1.0

HIGH-SPEED 8-BIT MULTIPLYING D/A CONVERTER

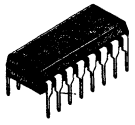
The Fujitsu MB 4072 is a High-Speed Digital to Analog Converter IC. The MB 4072's current outputs are high impedance open-collector, which provide voltage output with a load or current to voltage converter for various applications with operational amplifiers, microcomputers, etc.

Threshold level of digital inputs is variable with the level control input for various interface level.

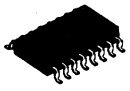
- Settling Time : 85 ns
- Linearity Error : ±0.19% max.
- Full-scale Temperature coefficient : ±10 ppm/°C
- Output Voltage Compliance : -10 V to +18 V
- Multiplying Operation
- True/Complimentary Current Sink Output
- Adjustable Threshold Level of Digital Inputs: Interface directly with TTL, CMOS, ECL, etc.
- Wide Supply Voltage Range : ±4.5 V to ±18 V
- Low Power Consumption : 33 mW at ±5V
- Operation Temperature : -40°C to +85°C
- Package : Standard 16 pin DIP
- Compatible with DAC-08



CERAMIC PACKAGE
DIP-16C-C02



PLASTIC PACKAGE
DIP-16P-M02



PLASTIC PACKAGE
FPT-16P-M02

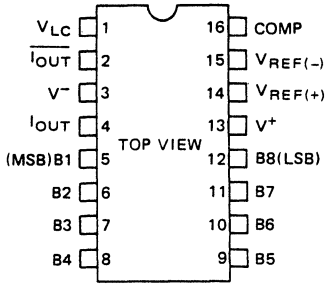
7

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter		Symbol	Ratings	Unit
Supply Voltage		V^+ to V^-	V^- to V^-+37	V
Digital Input Voltage		V_I	37	V
Threshold Control Voltage		V_{LC}	V^- to V^+	V
Reference Input Voltage		$V_{REF}(+)$	V^- to V^+	V
		$V_{REF}(-)$	V^- to V^+	V
Differential Reference Input Voltage		$V_{REF}(+)$ to $V_{REF}(-)$	±18.5	V
Reference Input Current		I_{REF}	5	mA
Power Consumption		P_D	500	mW
Storage Temp.	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	°C

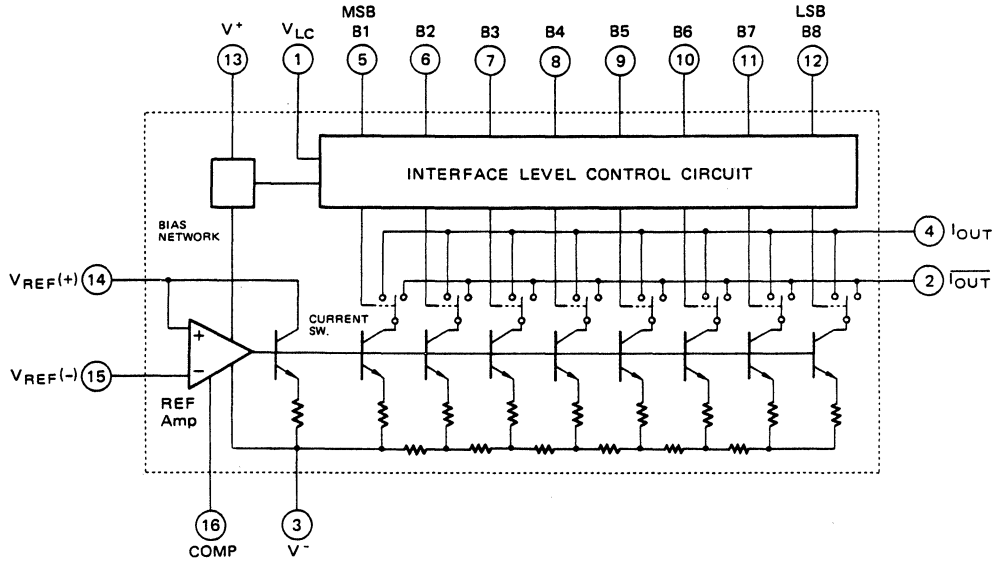
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V^+	+4.5		+18	V
	V^-	-4.5		-18	V
Operating Temperature	T_A	-40		+85	°C

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted. V^+ = +15 V, V^- = -15V, I_{REF} = 2.0 mA, T_A = -40°C to +85°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Resolution		8	8	8	bits
Monotonicity		8	8	8	bits
Linearity Error	LE			±0.19	%(FSR)
Settling Time (Final Value: ±1/2 LSB, T_A=25°C, On/Off Switching for Each bit/All bits)	t_s		85	150	ns
Propagation Delay Time (T_A=25°C, On/Off Switching for Each bit/All bits)	t_{PLH} t_{PHL}		35	60	ns
Temperature coefficient at full-scale	TC_{IFS}		±10	±50	ppm/°C
Output Voltage Range (ΔI_{FS} 1/2 LSB, R_{OUT} 20 MΩ typ.)	V_{OC}	-10		+18	V
Output Current at full-scale (V_{REF} = 10.000 V, R14 = 5.000 kΩ, R15 = 5.000 kΩ, T_A = 25°C)	I_{FS4}	1.94	1.99	2.04	mA
Symmetry at full-scale ($I_{FSS}=I_{FS4}-I_{FS2}$)	I_{FSS}		±1.0	±8.0	μA
Output Current at zero scale	I_{ZS}		0.2	2.0	μA
Output Current Range (R14 = 5.000 kΩ, R15 = 5.000 kΩ, V_{REF} = +15.0 V, V^- = -10 V)	I_{OR1}	2.1			mA
Output Current Range (R14 = 5.000 kΩ, R15 = 5.000 kΩ, V_{REF} = +25.0 V, V^- = -12 V)	I_{OR2}	4.2			mA
Low-level Input Voltage (V_{LC} = 0 V)	V_{IL}			0.8	V
High-level Input Voltage (V_{LC} = 0V)	V_{IH}	2.0			V
Low-level Input Current (V_{LC} = 0V, V_{IN} = -10 V to +0.8 V)	I_{IL}		-2.0	-10	μA
High-level Input Current (V_{LC} = 0 V, V_{IN} = 2.0 V to 18 V)	I_{IH}		0.002	10	μA

7

ELECTRICAL CHARACTERISTICS (Cont'd)

(Recommended Operating Conditions unless otherwise noted. $V^+ = +15$ V, $V^- = -15$ V, $I_{REF} = 2.0$ mA, $T_A = -40°C$ to $+85°C$)

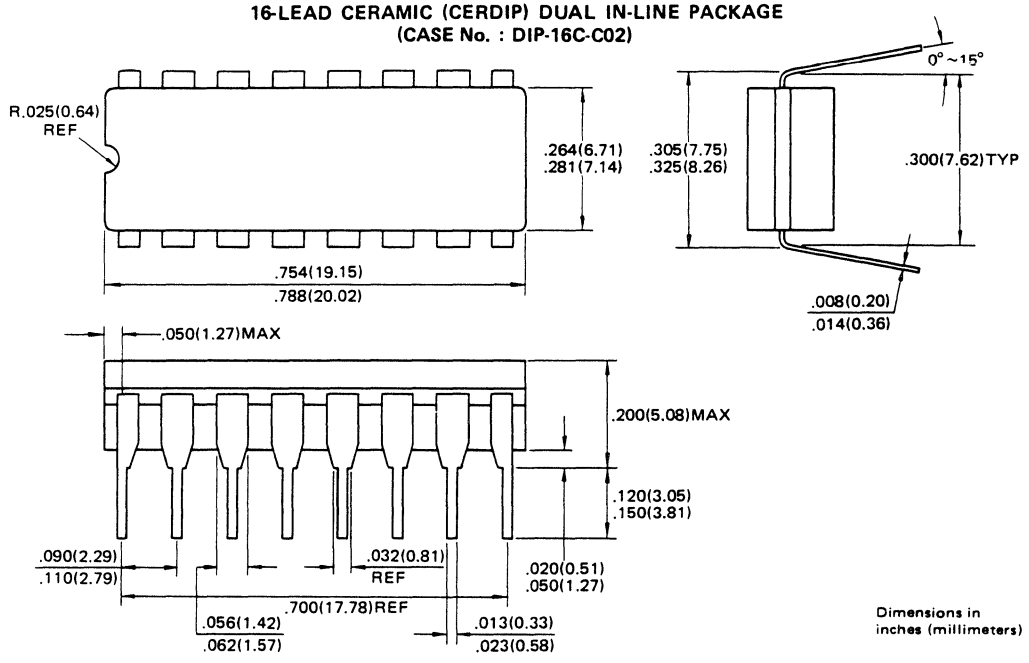
Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Logic Input Voltage Range ($V^- = -15$ V)		V_{IS}	-10		+18	V
Logic Threshold Voltage Rnage ($V^+ = +15$ V, $V^- = -15$ V)		V_{THR}	-10		+13.5	V
Reference Bias Current		I_{15}		-1.0	-3.0	μA
Reference Input Through Rate ($R_{EQ} = 200\ \Omega$, $R_L = 100\ \Omega$, $C_L = 0$ pF)		$\frac{dI}{dt}$	4.0	8.0		mA/μs
Supply Voltage Sensitivity* ($V^+ = +4.5$ V to 18 V, $I_{REF} = 1$ mA)		$PSSI_{FS+}$		±0.0003	±0.01	%/%
Supply Voltage Sensitivity* ($V^- = -4.5$ V to -18 V, $I_{REF} = 1$ mA)		$PSSI_{FS-}$		±0.002	±0.01	%/%
Supply Current	($V^+ = +5$ V, $V^- = -5$ V, $I_{REF} = 1.0$ mA)	I^+		2.3	3.8	mA
		I^-		-4.3	-5.8	mA
	($V^+ = +5$ V, $V^- = -15$ V, $I_{REF} = 2.0$ mA)	I^+		2.4	3.8	mA
		I^-		-6.4	-7.8	mA
	($V^+ = +15$ V, $V^- = -15$ V, $I_{REF} = 2.0$mA)	I^+		2.5	3.8	mA
		I^-		-6.5	-7.8	mA
Power Dissipation	($V^+ = +5$ V, $V^- = -5$ V, $I_{REF} = 1.0$ mA)	P_D		33	48	mW
	($V^+ = 5$ V, $V^- = -15$ V, $I_{REF} = 2.0$ mA)	P_D		103	136	mW
	($V^+ = 15$ V, $V^- = -15$ V, $I_{REF} = 2.0$ mA)	P_D		135	174	mW

*Note: $PSSI_{FS} = (\frac{\Delta I_{FS}}{I_{FS}} \times 100) / (\frac{18 - 4.5}{15} \times 100)$

7

PACKAGE DIMENSIONS

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)

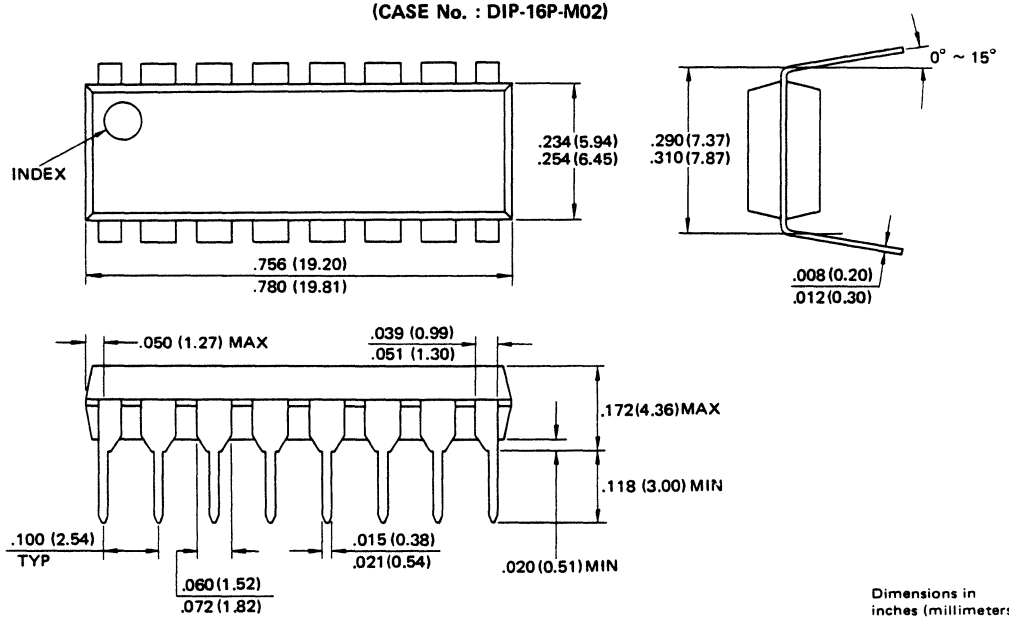


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M02)

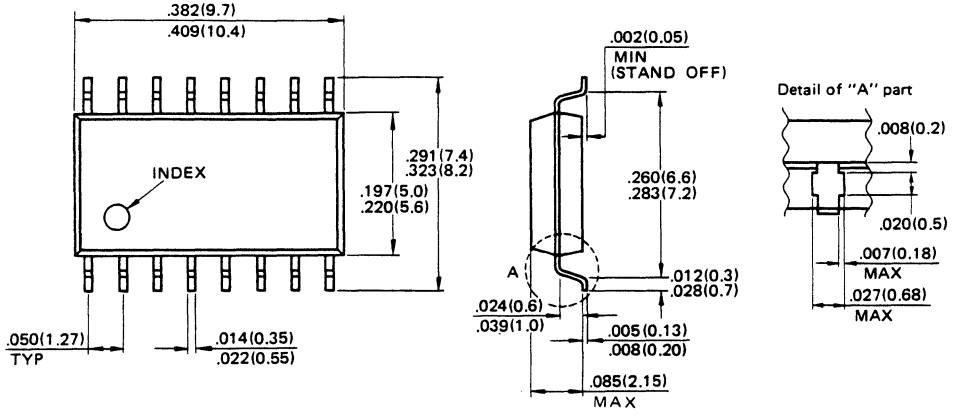


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

7

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

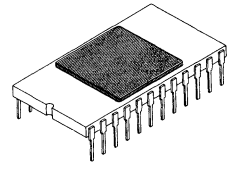
10-BIT HIGH SPEED D/A CONVERTER

MB 40748-8
MB 40748-9

August 1984
Edition 3.0

10-BIT HIGH SPEED D/A CONVERTER

The Fujitsu MB 40748 is a 10 bit Ultra-high speed low-power Digital to Analog Converter which is fabricated with Fujitsu Advanced Bipolar Technology. The device can convert 10-bit digital signals into analog signals from DC to 30 Mega-samples/sec. (MSPS). Because of such high speed operation, the device is suitable for applications such as color television decoding and video processing with computer.

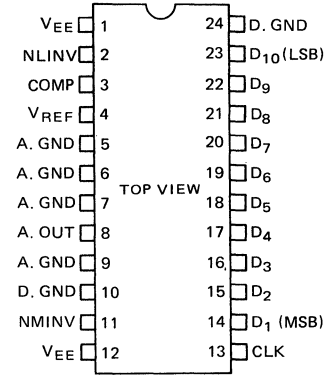


CERAMIC PACKAGE
DIP-24C-A01

- Resolution : 10 bits
- Linearity MB 40748-8 : ± 0.2% max. (8 bit accuracy)
  MB 40748-9 : ± 0.1% max. (9 bit accuracy)
- Conversion Rate : 30 MSPS typ.
- Analog Output Voltage : 0 V to -1 V
- Digital Input Voltage : 10 k ECL level
- Input Code : Binary or 2's complement
- Single Power Supply : -5.2 V
- Power Dissipation : 300 mW Typ.
- Standard 24-pin Dual-in-line Package

7

PIN ASSIGNMENT
(TOP VIEW)



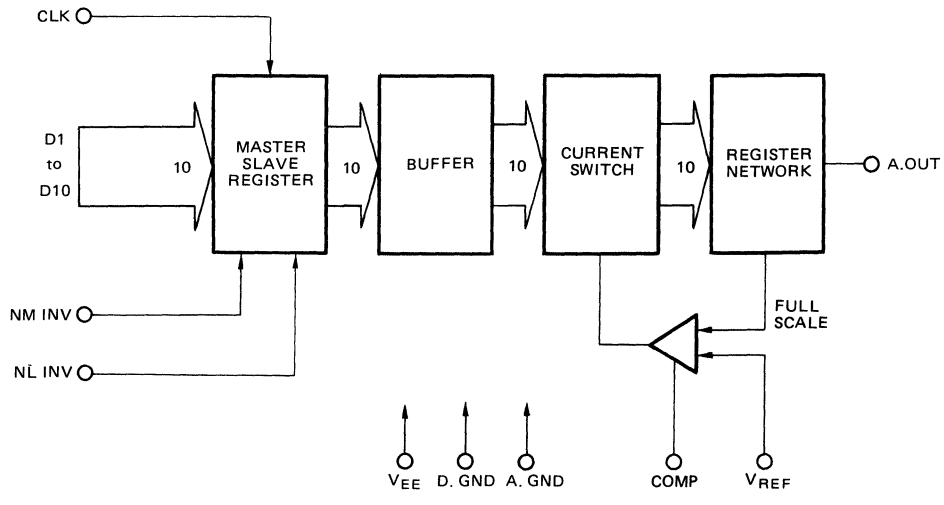
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{EE}	+0.5 to -7.0	V
Digital Input Voltage	V_{IND}	+0.5 to V_{EE}	V
Analog Reference Voltage	V_{REF}	+0.5 to V_{EE}	V
Storage Temperature	T_{STG}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{EE}	-5.46	-5.20	-4.94	V
Analog Reference Voltage	V_{REF}	-1.2	-1.0	-0.8	V
Clock Pulse Width at High-level	t_W^+	15			ns
Clock Pulse Width at Low-level	t_W^-	15			ns
Data Setup Time	t_S	20			ns
Data Hold Time	t_H	0			ns
Operating Temperature	T_A	0		70	°C
Phase Compensation Capacitance*	C_{COMP}	1			μF

Note: The capacitor should be connected between COMP and V_{EE}

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.) (V_{EE} = -5.2 V, T_A = 0 to +70°C)

7

ANALOG DC CHARACTERISTICS

Parameter	Condition & Note	Symbol	Value			Unit
			Min	Typ	Max	
Resolution					10	bits
Linearity Error	MB 40748-8	LE			±0.2	%
	MB 40748-9				±0.1	%
Full-scale Analog Output Voltage	V_{REF} = -1.00 V, A.OUT is open.	V_{OFS}	-1.06	-1.00	-0.94	V
Zero-scale Analog Output Voltage	V_{REF} = -1.00 V, A.OUT is open.	V_{OZS}	-15	0	15	mV
Reference Input Current	V_{REF} = -1.00 V,	I_{REF}			10	μA
Output Impedance	T_A = 25°C	Z_{OUT}	70	80	90	Ω

ELECTRICAL CHARACTERISTICS (Cont'd)

(Recommended Operating Conditions unless otherwise noted.) (V_{EE} = -5.2 V, T_A = 0 to +70°C)

DIGITAL DC CHARACTERISTICS

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
High-level Digital Input Voltage	T_A = 0°C	V_{IHD}	-1.145			V
	T_A = +25°C		-1.105			
	T_A = +70°C		-1.045			
Low-level Digital Input Voltage	T_A = 0°C	V_{ILD}			-1.490	V
	T_A = +25°C				-1.475	
	T_A = +70°C				-1.450	
High-level Digital Input Current		I_{IHD}			250	μA
Low-level Digital Input Current		I_{ILD}	0.5		200	μA
Supply Current	V_{REF} = -1.00 V	I_{EE}	-90	-56		mA

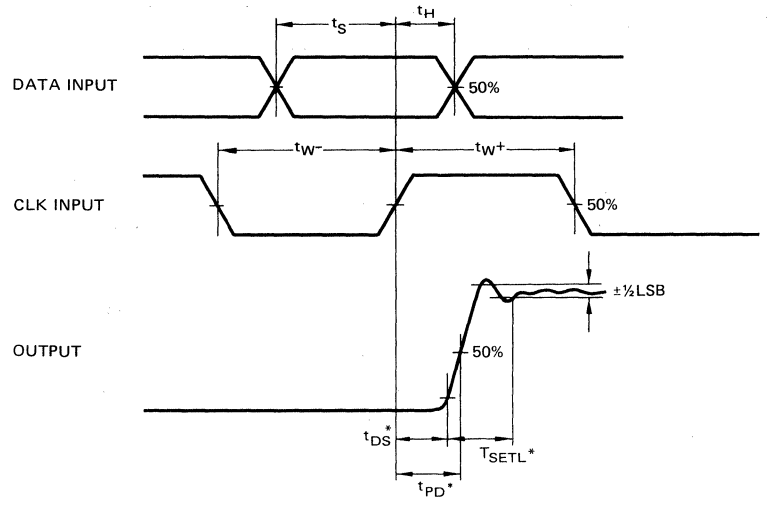
7

SWITCHING CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = +25°C)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Maximum conversion Rate		FS	20	30		MSPS

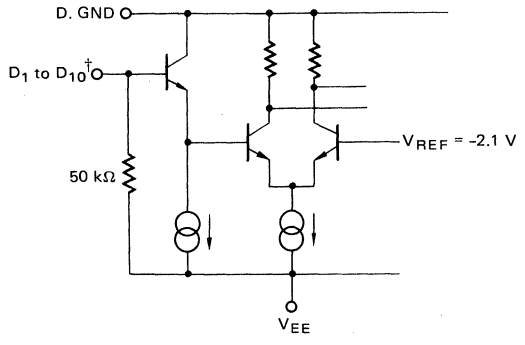
TIMING DIAGRAM



Note: *These values are not specified because they depend on application circuit.

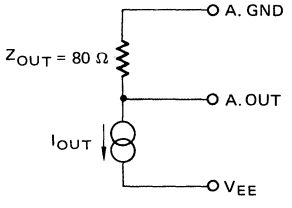
7

EQUIVALENT DIGITAL INPUT CIRCUIT



Note: †V_{TH} = -1.3 V

EQUIVALENT OUTPUT CIRCUIT



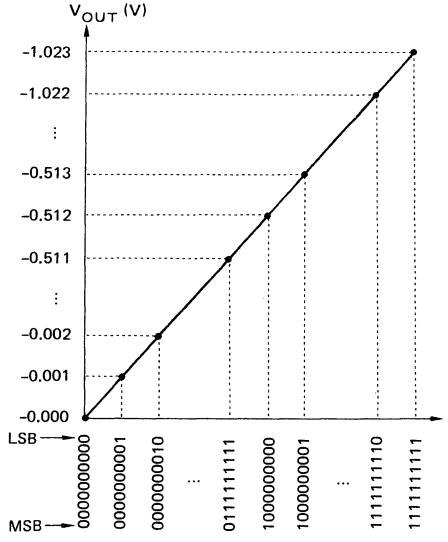
OUTPUT VOLTAGE

(Recommended Operating Conditions unless otherwise noted. V_{REF} = - 1.024 V, Positive Logic) (1 LSB = 1 mV)

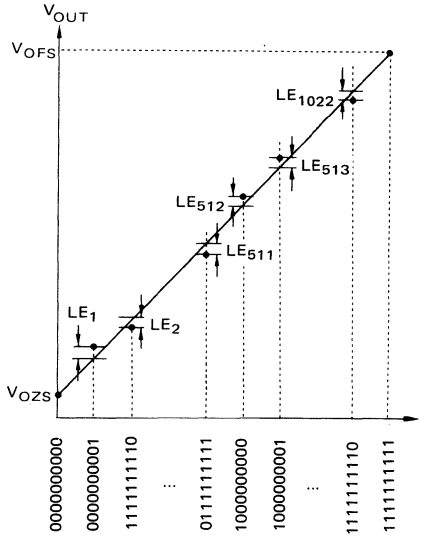
STEP	Digital Input	BINARY		OFFSET 2'S COMPLEMENT		Ideal Output Voltage (V)
		Non-inverting Input	Inverting Input	Non-inverting Input	Inverting Input	
	NMINV	1	0	0	1	
	MLINV	1	0	1	0	
0		0000000000	1111111111	1000000000	0111111111	-0.000
1		0000000001	1111111110	1000000001	0111111110	-0.001
⋮		⋮	⋮	⋮	⋮	⋮
511		0111111111	1000000000	1111111111	0000000000	-0.511
512		1000000000	0111111111	0000000000	1111111111	-0.512
513		1000000001	0111111110	0000000001	1111111110	-0.513
⋮		⋮	⋮	⋮	⋮	⋮
1022		1111111110	0000000001	0111111110	1000000001	-1.022
1023		1111111111	0000000000	0111111111	1000000000	-1.023

7

IDEAL OUTPUT OPERATION



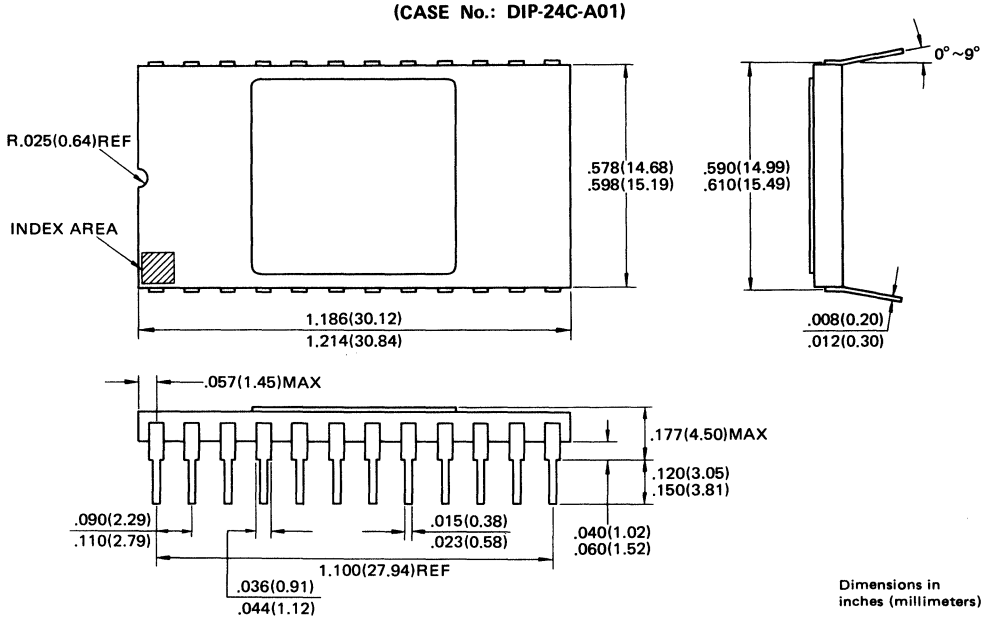
PRACTICAL OUTPUT OPERATION



$$\text{Linearity Error} = \frac{|LE_n|_{max}}{|FS|}$$

PACKAGE DIMENSIONS

24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-A01)



7

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FUJITSU

6-BIT HIGH SPEED D/A CONVERTER

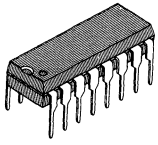
MB40776

December 1987
Edition 4.0

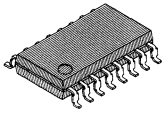
6-BIT HIGH SPEED D/A CONVERTER

The Fujitsu MB 40776 is a 6-bit low power ultra-high speed video D/A converter fabricated with Fujitsu Advanced Bipolar Technology. The MB 40776 can convert 6-bit digital signals into analog signals at a rate of DC to 20 megasamples/sec (MSPS). Because of such high speed operation, the MB 40776 is suitable for applications such as digital color TV, video processing with computer, radar signal processing.

- Resolution : 6 bits
- Linearity : ±0.8%
- Maximum Conversion Rate : 20 MSPS min.
- Analog Output Voltage range : V_{CC} to V_{CC} -1 [V]
- Digital I/O level : TTL
- Single Power Supply : + 5 [V]
- Power Dissipation : 220 [mW] typ.
- Standard 16-pin DIP Package : (Suffix: -P)
  Standard 16-pin FPT Package : (Suffix: -PF)

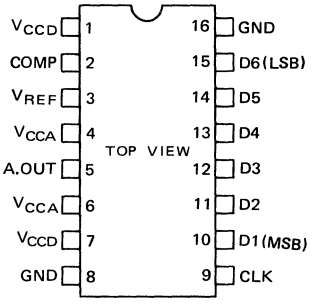


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

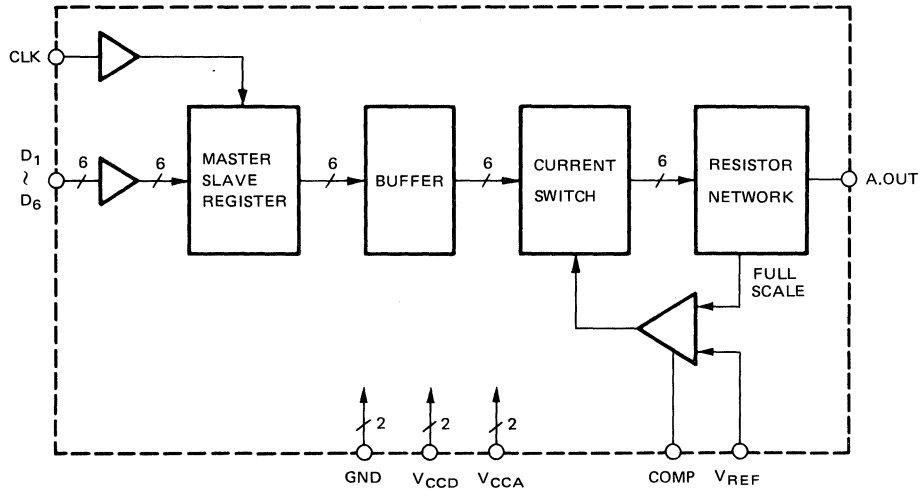
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	-0.5 to +7.0	V
Digital Input Voltage	V_{IND}	-0.5 to +7.0	V
Analog Reference Voltage	V_{REF}	3.70 to V_{CC} + 0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1– MB40776 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA} V_{CCD}	4.75	5.00	5.25	V
Analog Reference Voltage *1	V_{REF}	3.70	4.00	4.30	V
Clock Pulse Width at High level	t_{w+}	25			ns
Clock Pulse Width at Low level	t_{w-}	25			ns
Data Setup Time	t_S	12.5			ns
Data Hold Time	t_H	12.5			ns
Operating Temperature	T_A	0		70	°C
Phase Compensation Capacitance*2	C_{COMP}	1			μF

NOTE: *1: $V_{CC} - V_{REF} \leqq 1.2$ V
*2: The capacitance should be connected between COMP and GND.

7

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					6	bits
Linearity Error	LE	DC			±0.8	%
Full-Scale Analog Output Voltage	V_{OFS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	V_{CCA} -0.015	V_{CCA}	V_{CCA} +0.015	V
Zero-Scale Analog Output Voltage	V_{OZS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	3.932	3.992	4.052	V
Reference Input Current	I_{REF}	V_{REF} = 4.00 V			10	μA
Output Impedance	Z_{OUT}	T_A = 25°C	70	80	90	Ω

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DIGITAL DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

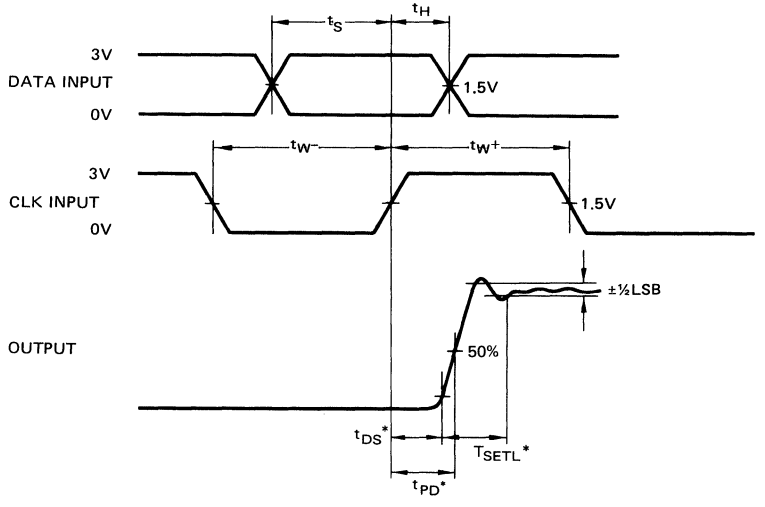
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	V_{IHD}		2.0			V
Low-level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{CC} = 5.25 V V_I = 7.00 V		0	100	μA
High-level Input Current	I_{IHD}	V_{CC} = 5.25 V V_{IHD} = 2.70 V		0	20	μA
Low-level Input Current	I_{ILD}	V_{CC} = 5.25 V V_{ILD} = 0.40 V	-400	-40		μA
Power Supply Current	I_{CC}	V_{REF} = 4.05 V		43*	65	mA

NOTE: * V_{CC} = 5.00 V, V_{REF} = 4.00 V

SWITCHING CHARACTERISTICS (V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		20	30	–	MSPS

TIMING DIAGRAM



Note: *These values are not specified because they depend on application circuit.

7

Fig. 2 – DIGITAL INPUT EQUIVALENT CIRCUIT

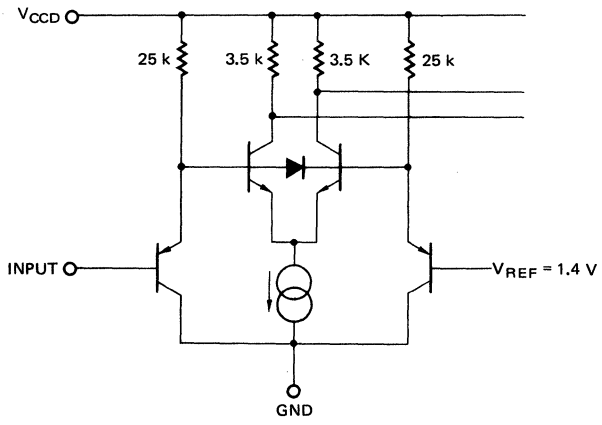
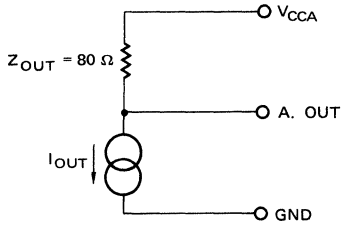


Fig. 3 – OUTPUT EQUIVALENT CIRCUIT



7

OUTPUT VOLTAGE

(V_{CCA} = 5.000 V, V_{REF} = 3.976 V)

Input Code	OUTPUT VOLTAGE (V)
000000	3.992
000001	4.008
•	•
•	•
•	•
011111	4.488
100000	4.504
100001	4.520
•	•
•	•
•	•
111110	4.984
111111	5.000

Note: 1LSB = 16 mV

Fig. 4 — IDEAL OUTPUT OPERATION

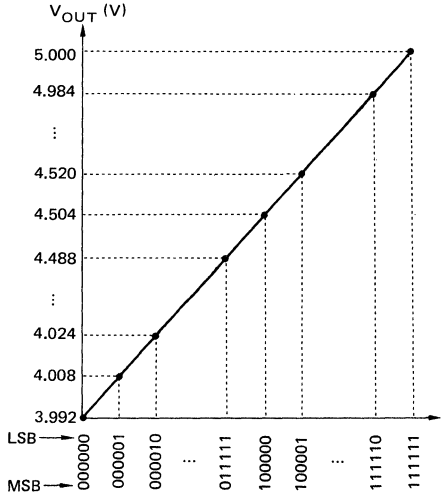
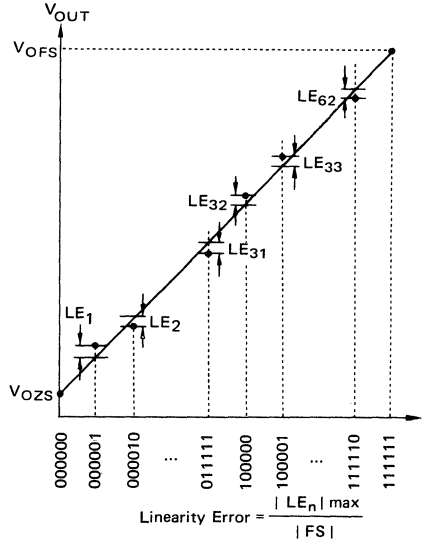


Fig. 5 — PLACTICAL OUTPUT OPERATION



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – POWER SUPPLY CURRENT vs. TEMPERATURE

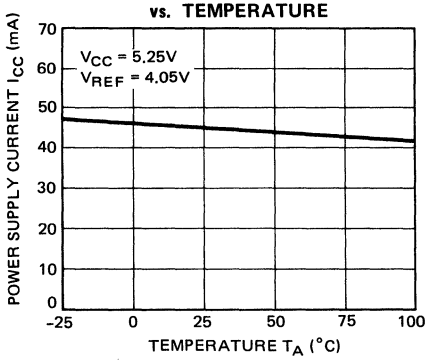


Fig. 7 – LINEARITY ERROR vs. TEMPERATURE

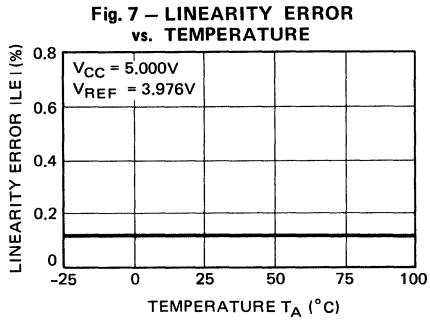


Fig. 8 – OUTPUT IMPEDANCE vs. TEMPERATURE

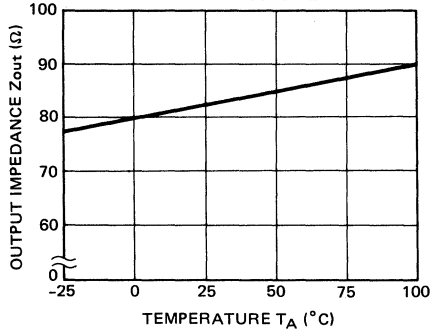


Fig. 9 – ZERO-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE

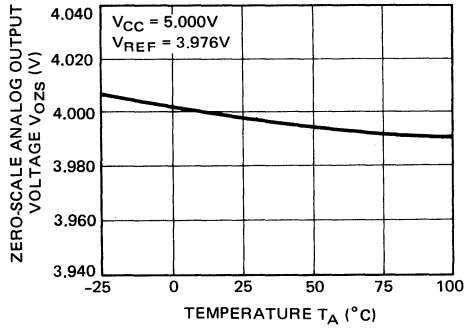
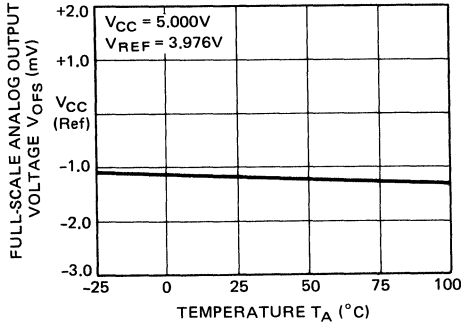


Fig. 10 – FULL-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE



7

Fig. 11 – DELAY TIME vs. TEMPERATURE

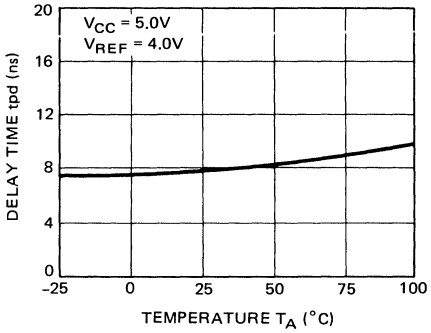


Fig. 12 – DELAY TIME vs. POWER SUPPLY VOLTAGE

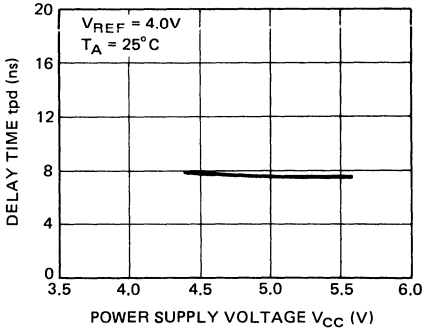


Fig. 13 – CLOCK PULSE WIDTH vs. TEMPERATURE

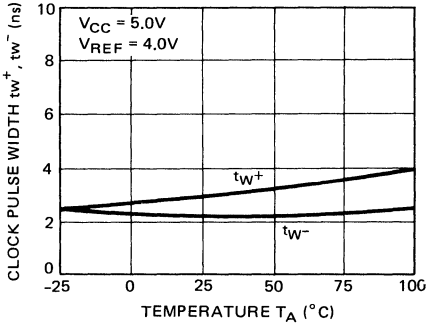


Fig. 14 – CLOCK PULSE WIDTH vs. POWER SUPPLY VOLTAGE

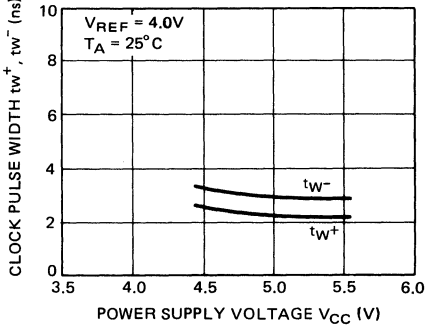
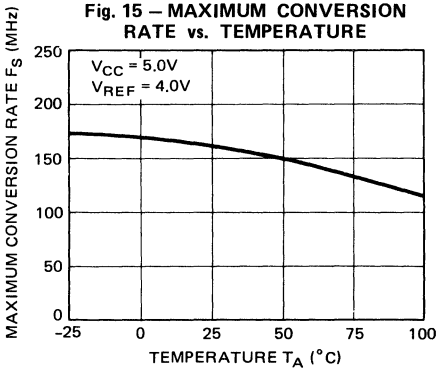


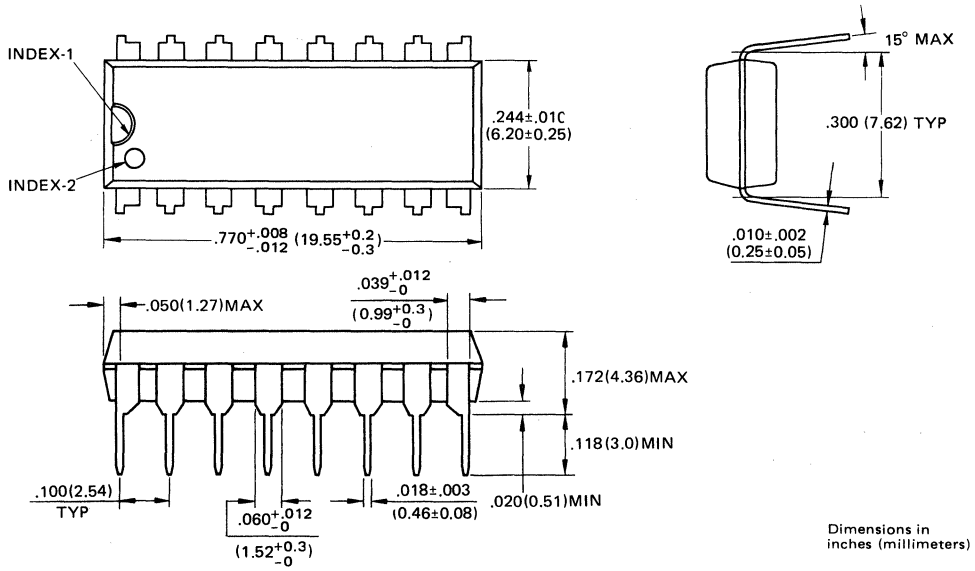
Fig. 15 – MAXIMUM CONVERSION RATE vs. TEMPERATURE



7

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)

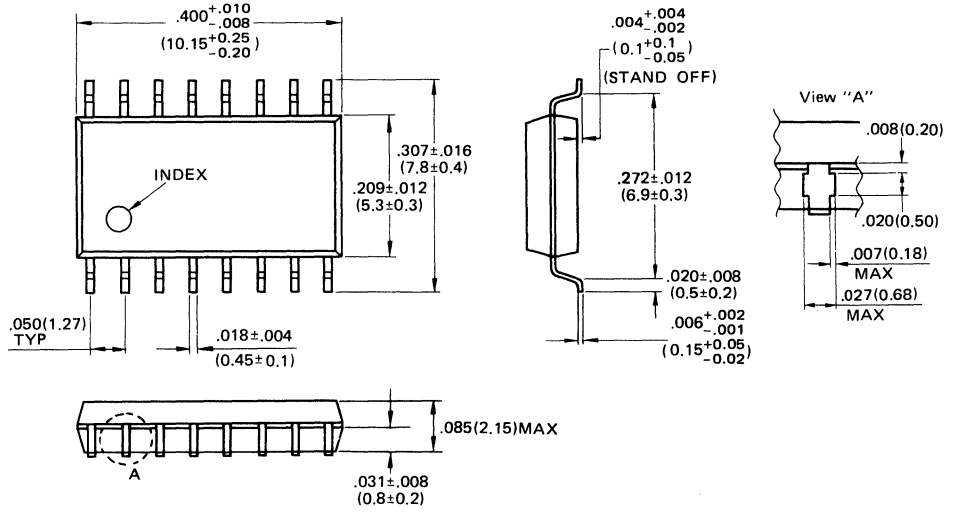


Dimensions in
inches (millimeters)

7

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

7

FUJITSU

8-BIT HIGH SPEED D/A CONVERTER

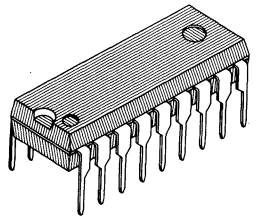
MB40778

December 1987
Edition 3.0

8-BIT HIGH SPEED D/A CONVERTER

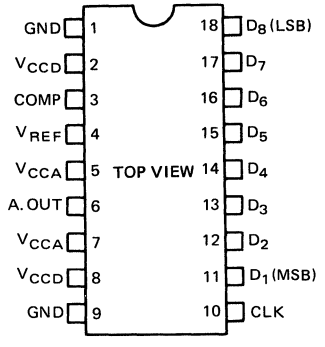
The Fujitsu MB 40778 is a 8-bit low power ultra-high speed video D/A converter fabricated with Fujitsu Advanced Bipolar Technology. The MB 40778 can convert 8-bit digital signals into analog signals at a rate of DC to 20 megasamples/sec (MSPS). Because of such high speed operation, the MB 40778 is suitable for applications such as digital color TV, video processing with computer, radar signal processing.

- Resolution : 8 bits
- Linearity : ±0.2%
- Maximum Conversion Rate : 20 MSPS min.
- Analog Output Voltage range : V_{CC} to V_{CC} −1 [V]
- Digital I/O level : TTL
- Single Power Supply : +5 [V]
- Power Dissipation : 250 [mW] typ.
- Standard 18-pin DIP Package (Suffix: -P)



PLASTIC PACKAGE
DIP-18P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

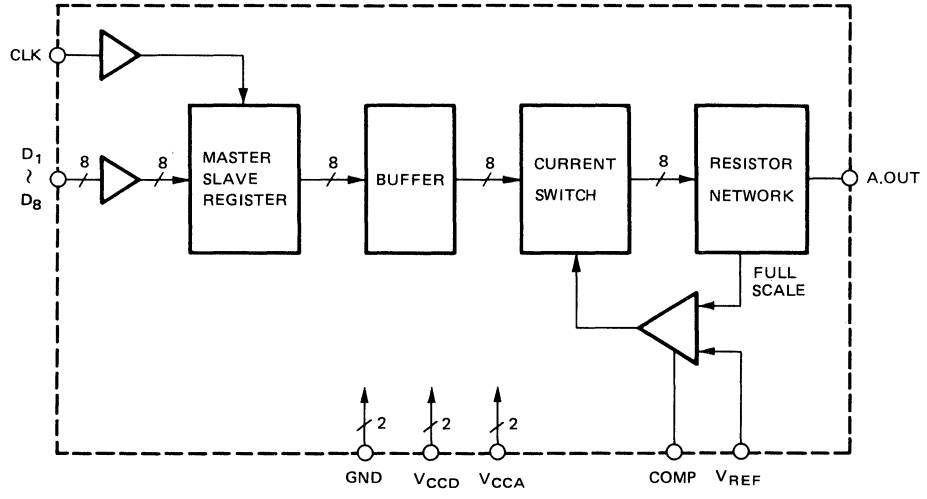
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	-0.5 to +7.0	V
Digital Input Voltage	V_{IND}	-0.5 to +7.0	V
Analog Reference Voltage	V_{REF}	3.70 to V_{CC} + 0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1– MB40778 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA} V_{CCD}	4.75	5.00	5.25	V
Analog Reference Voltage *1	V_{REF}	3.70	4.00	4.30	V
Clock Pulse Width at High level	t_{w+}	25			ns
Clock Pulse Width at Low level	t_{w-}	25			ns
Data Setup Time	t_S	12.5			ns
Data Hold Time	t_H	12.5			ns
Operating Temperature	T_A	0		70	°C
Phase Compensation Capacitance*2	C_{COMP}	1			μF

Note: *1: $V_{CC} - V_{REF} \leqq 1.2$ V
*2: The capacitor should be connected between COMP and GND.

7

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					8	bits
Linearity Error	LE	DC			±0.2	%
Full-Scale Analog Output Voltage	V_{OFS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	V_{CCA} -0.015	V_{CCA}	V_{CCA} +0.015	V
Zero-Scale Analog Output Voltage	V_{OZS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	3.919	3.980	4.042	V
Reference Current	I_{REF}	V_{REF} = 4.00 V			10	μA
Output Impedance	Z_{OUT}	T_A = 25°C	70	80	90	Ω

DIGITAL DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

7

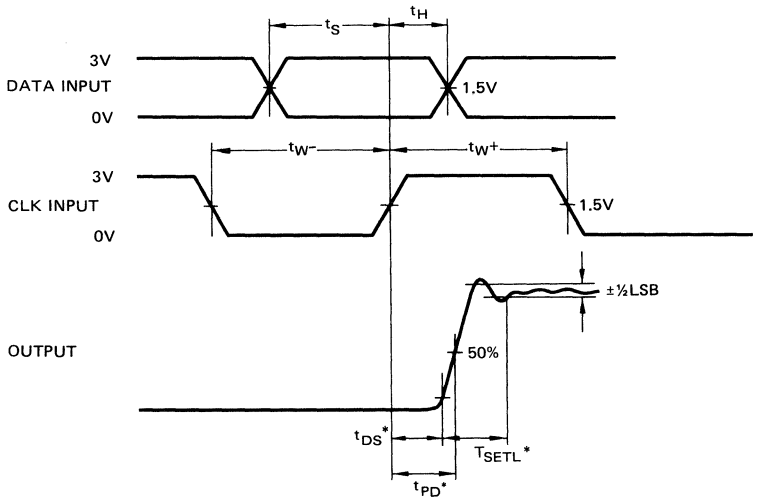
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	V_{IHD}		2.0			V
Low-level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{CC} = 5.25 V V_{ID} = 7.00 V		0	100	μA
High-level Input Current	I_{IHD}	V_{CC} = 5.25 V V_{IHD} = 2.70 V		0	20	μA
Low-level Input Current	I_{ILD}	V_{CC} = 5.25 V V_{ILD} = 0.40 V	-400	-40		μA
Power Supply Current	I_{CC}	V_{REF} = 4.05 V		50*	75	mA

Note: * V_{CC} = 5.00 V, V_{REF} = 4.00 V

SWITCHING CHARACTERISTICS (V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		20	30	–	MSPS

TIMING DIAGRAM



Note: *These values are not specified because they depend on application circuit.

7

Fig. 2 – DIGITAL INPUT EQUIVALENT CIRCUIT

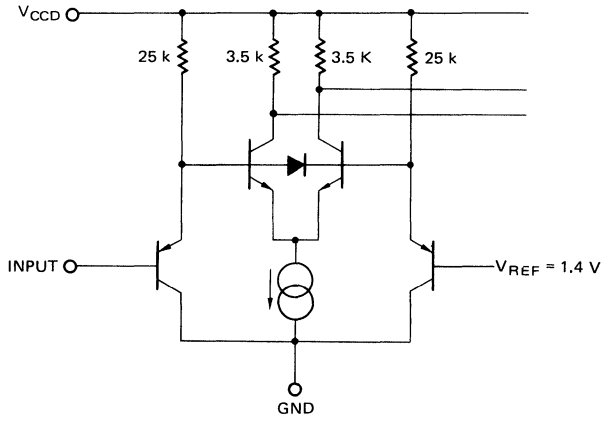
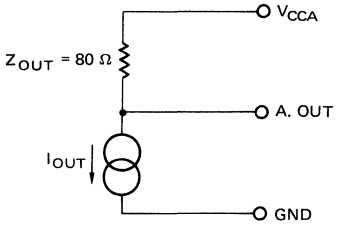


Fig. 3 – OUTPUT EQUIVALENT CIRCUIT



7

OUTPUT VOLTAGE

(V_{CCA} = 5.000 V, V_{REF} = 3.976 V)

Input Code	OUTPUT VOLTAGE (V)
00000000	3.980
00000001	3.984
•	•
•	•
•	•
01111111	4.488
10000000	4.492
10000001	4.496
•	•
•	•
•	•
11111110	4.996
11111111	5.000

Note: 1LSB = 4 mV

7

Fig. 4 — IDEAL OUTPUT OPERATION

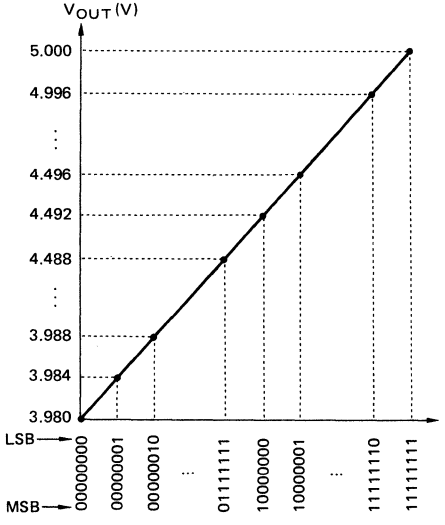
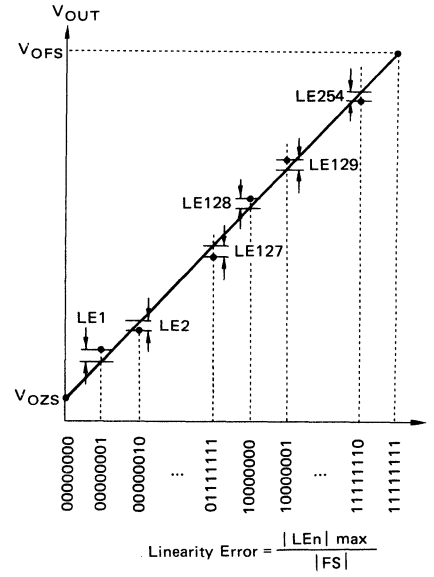


Fig. 5 — PRACTICAL OUTPUT OPERATION



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – POWER SUPPLY CURRENT vs. TEMPERATURE

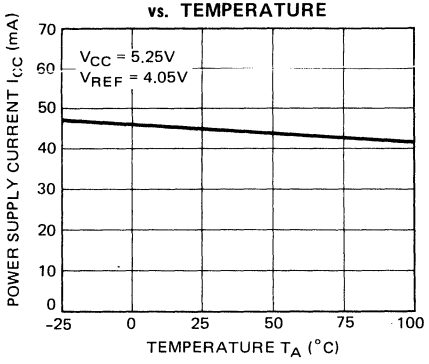


Fig. 7 – LINEARITY ERROR vs. TEMPERATURE

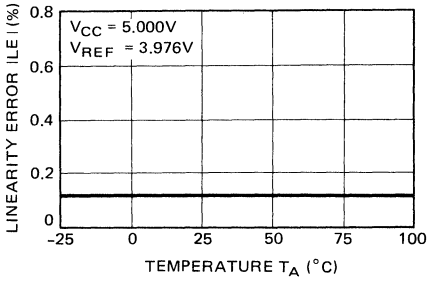


Fig. 8 – OUTPUT IMPEDANCE vs. TEMPERATURE

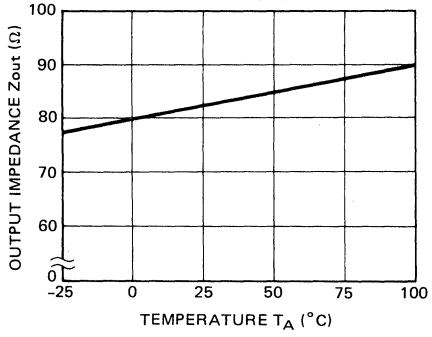


Fig. 9 – ZERO-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE

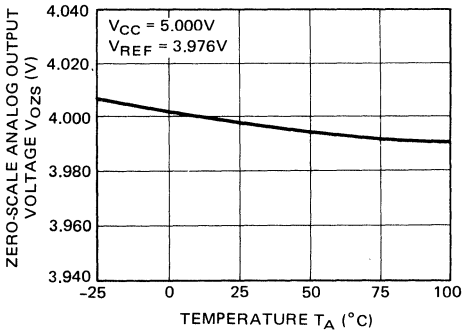
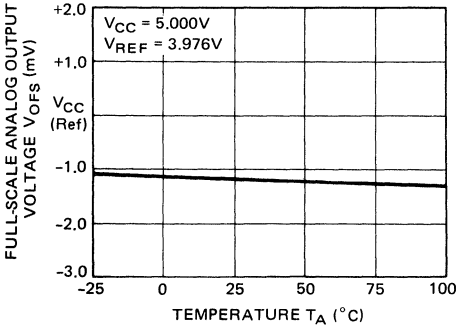


Fig. 10 – FULL-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE



7

Fig. 11 – DELAY TIME vs. TEMPERATURE

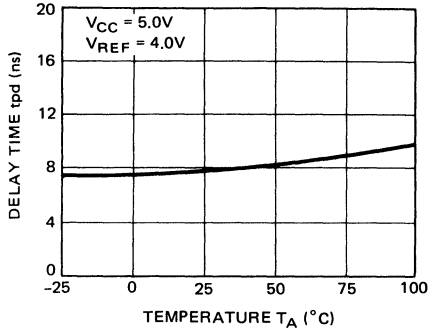


Fig. 12 – DELAY TIME vs. POWER SUPPLY VOLTAGE

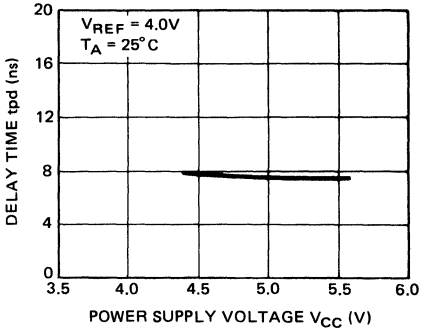


Fig. 13 – CLOCK PULSE WIDTH vs. TEMPERATURE

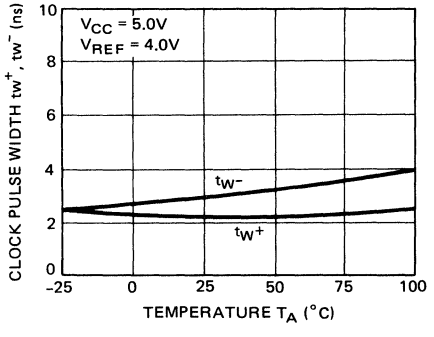


Fig. 14 – CLOCK PULSE WIDTH vs. POWER SUPPLY VOLTAGE

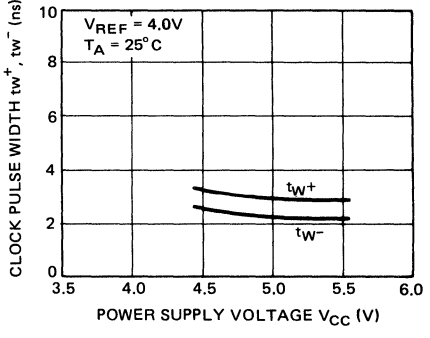
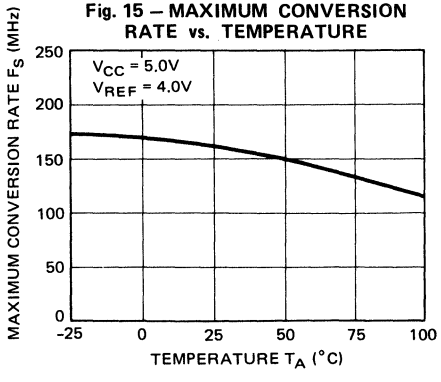
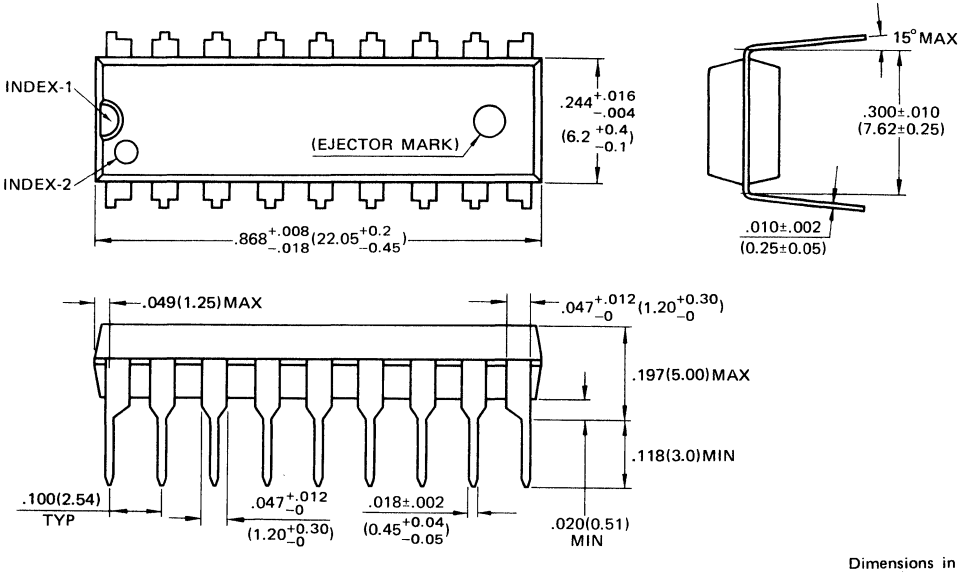


Fig. 15 – MAXIMUM CONVERSION RATE vs. TEMPERATURE



PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M02)



Dimensions in
inches (millimeters)

FUJITSU

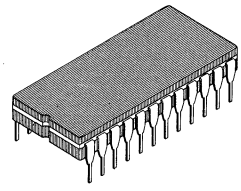
10-BIT ULTRA-HIGH SPEED D/A CONVERTER

MB 40788

September 1984
Edition 4.0

10-BIT ULTRA-HIGH SPEED D/A CONVERTER

The Fujitsu MB 40788 is 10 bit Ultra-high speed low-power Digital to Analog Converter which is fabricated with Fujitsu Advanced Bipolar Technology. The device can convert 10-bit digital signal into analog signal at a rate of DC to 125 Mega-samples/sec. (MSPS). Because of such high speed operation, the device is suitable for applications such as color television decoding system, video processing system with computer, and so on.

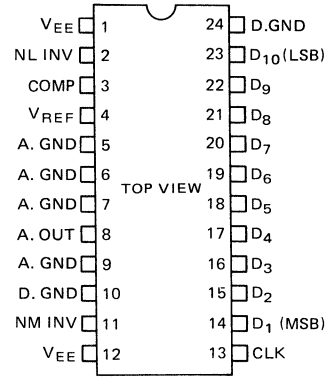


CERAMIC PACKAGE
DIP-24C-C01

- Resolution : 10 bits
- Linearity : ±0.2% max.
- Conversion Rate : 125 MSPS min.
- Analog Output Voltage : 0 V to -1 V
- Digital Input Voltage : 10 k ECL level
- Input Code : Binary or 2's complement
- Single Power Supply (-5.2 V) : -5.2V
- Power Dissipation : 450mW typ.
- Standard 24-pin Dual-in-line Package

7

PIN ASSIGNMENT



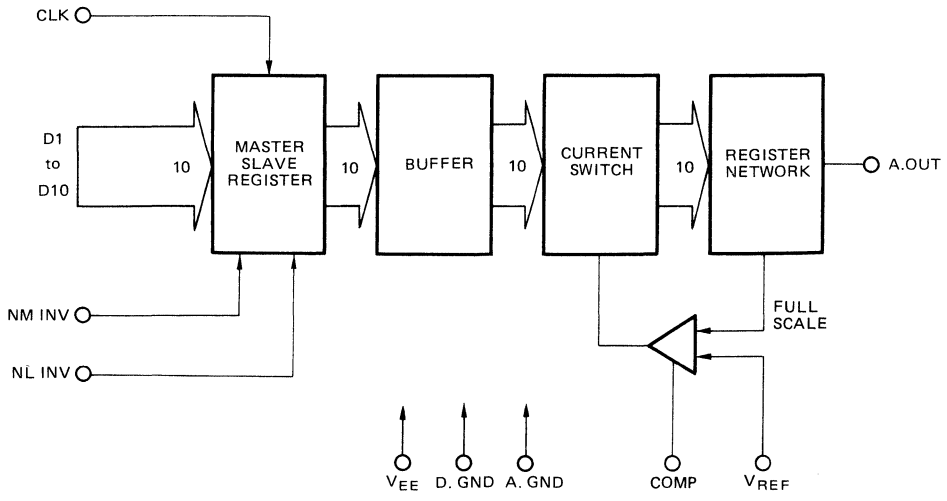
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{EE}	+0.5 to -7.0	V
Digital Input Voltage	V_{IND}	+0.5 to V_{EE}	V
Analog Reference Voltage	V_{REF}	+0.5 to V_{EE}	V
Storage Temperature	T_{STG}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{EE}	-5.46	-5.20	-4.94	V
Analog Reference Voltage	V_{REF}	-1.2	-1.0	-0.8	V
Clock Pulse Width (High-level)	$t_W{}^+$	3.0			ns
Clock Pulse Width (Low-level)	$t_W{}^-$	3.5			ns
Data Setup Time	t_S	3.0			ns
Data Hold Time	t_H	2.4			ns
Operating Temperature	t_A	0		70	°C
Phase Compensation Capacitance*1	C_{COMP}	1			μF

*1: The capacitor should be connected between COMP and V_{EE}

7

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.) (V_{EE} = -5.2 V, T_A = 0 to +70°C)

Parameter	Condition & Note	Symbol	Value			Unit
			Min.	Typ.	Max.	
Resolution					10	bits
Linearity Error	DC	LE			±0.2	%
Full-scale Analog Output Voltage	V_{REF} = -1.00 V Output is open.	V_{OFS}	-1.06	-1.00	-0.94	V
Zero-scale Analog Output Voltage	V_{REF} = -1.00 V Output is open.	V_{OZS}	-15	0	15	mV
Reference Input Current	V_{REF} = -1.00 V	I_{REF}			20	μA
Output Impedance	T_A = 25°C	Z_{OUT}	70	80	90	Ω

ELECTRICAL CHARACTERISTICS (Cont'd)

(Recommended Operating Conditions unless otherwise noted.) (V_{EE} = -5.2 V, T_A = 0 to +70°C)

Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
High-level Digital Input Voltage	T_A = 0°C T_A = +25°C T_A = +70°C	V_{IHD}	-1.145 -1.105 -1.045			V
Low-level Digital Input Voltage	T_A = 0°C T_A = +25°C T_A = +70°C	V_{ILD}			-1.490 -1.475 -1.450	V
High-level Digital Input Current		I_{IHD}		150	500	μA
Low-level Digital Input Current		I_{ILD}	0.5	115		μA
Supply Current	V_{REF} = -1.00 V	I_{EE}	-135	-84		mA

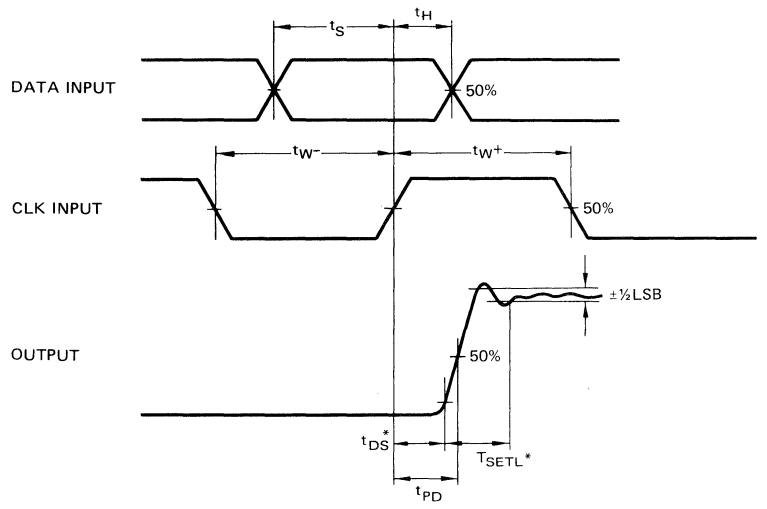
SWITCHING CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = +25°C)

Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Maximum Conversion Rate		FS	125			MSPS
Propagation delay time		t_{PD}	4.5	6.5	8.5	ns

7

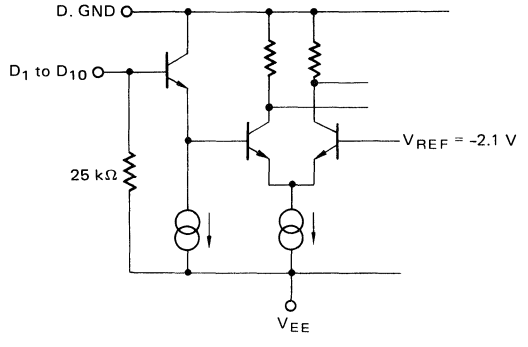
TIMING DIAGRAM



Note: *These values are not specified because they depend on application circuit.

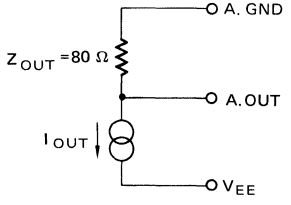
7

EQUIVALENT DIGITAL INPUT CIRCUIT



V_{TH} = -1.30 V

EQUIVALENT OUTPUT CIRCUIT



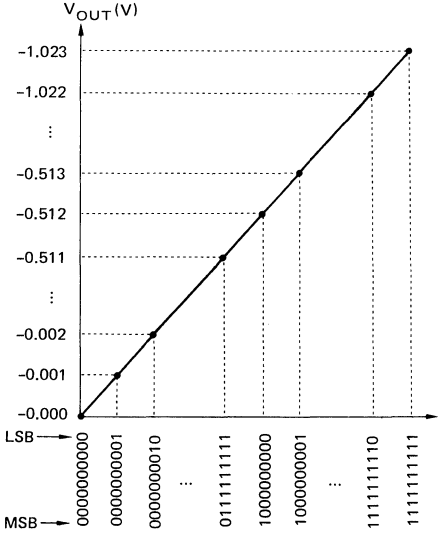
OUTPUT VOLTAGE

(Recommended Operating Conditions unless otherwise noted. V_{REF} = - 1.024 V) (1 LSB = 1 mV)

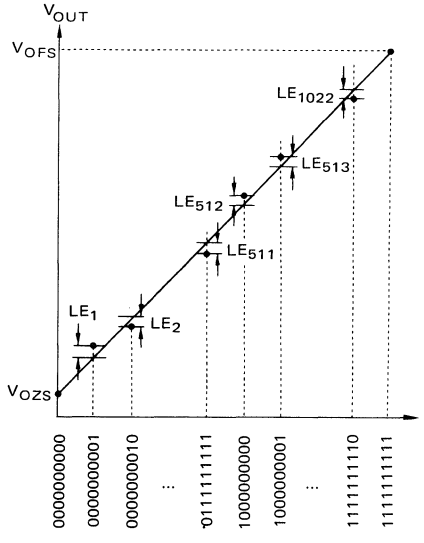
Step		Binary		Offset 2's complement		Output Voltage (V)
	Logic	Positive	Negative	Positive	Negative	
	NMINV	1	0	0	1	
	MLINV	1	0	1	0	
0		0000000000	1111111111	1000000000	0111111111	-0.000
1		0000000001	1111111110	1000000001	0111111110	-0.001
⋮		⋮	⋮	⋮	⋮	⋮
511		0111111111	1000000000	1111111111	0000000000	-0.511
512		1000000000	0111111111	0000000000	1111111111	-0.512
513		1000000001	0111111110	0000000001	1111111110	-0.513
⋮		⋮	⋮	⋮	⋮	⋮
1022		1111111110	0000000001	0111111110	1000000001	-1.022
1023		1111111111	0000000000	0111111111	1000000000	-1.023

7

IDEAL OUTPUT OPERATION



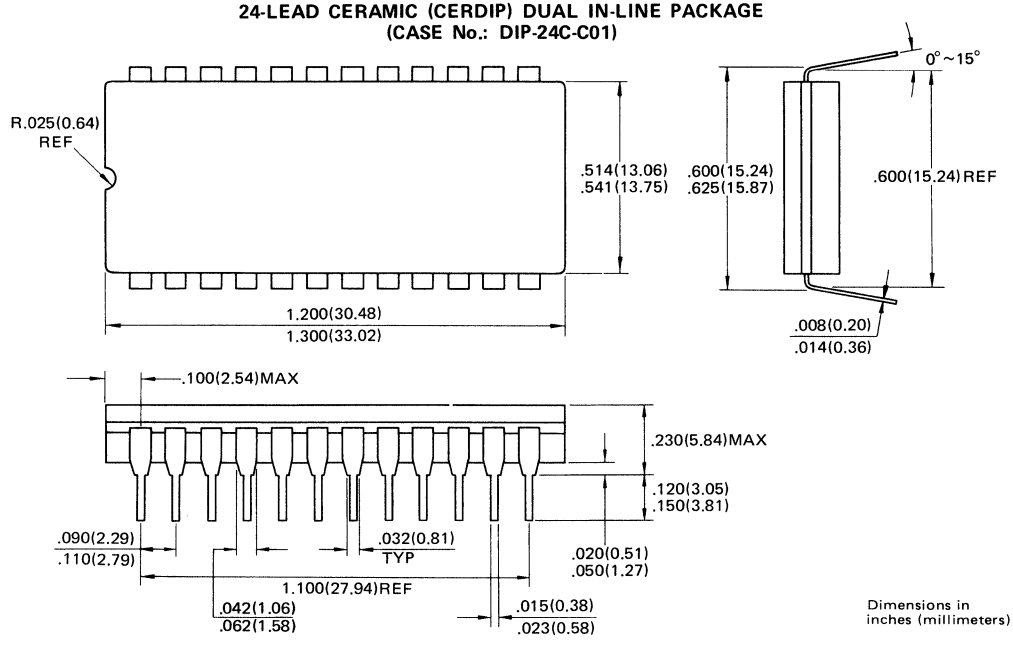
PRACTICAL OUTPUT OPERATION



$$\text{Linearity Error} = \frac{|LE_n|_{max}}{|FS|}$$

PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C01)



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Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

January 1987
TS535-A871

MB40874 4-bit Digital-to-Analog Converter with Look-Up Table

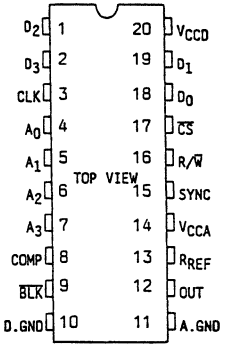
The Fujitsu MB40874 is 50 MSPS (Mega Sample Per Second) 4-bit Analog-to-Digital Converter with Look-up Table. The MB40874 is designed for high-speed video application with video RAM. Look-Up Table (LUT) is 16-word 4-bit memory to store luminance data. Instead of changing video RAM data, LUT data updating makes quick luminance change in monochrome video application, and quick colour change in colour video application.

CERAMIC PACKAGE
DIP-20C-C01

PLASTIC PACKAGE
DIP-20P-M02

- Resolution : 4 bit
- Linearity : ±1/2LSB
- Operation Frequency : 50 MHz min.
- Analog Output Voltage : 4.0 V to 5.0 V
- Digital Input : TTL Compatible
- Power Supply Voltage : +5 V
- Power Dissipation : 430 mW typ.
- 20-pin Ceramic DIP (Suffix: -CZ)
  20-pin Plastic DIP (Suffix: -P)

PIN ASSIGNMENT



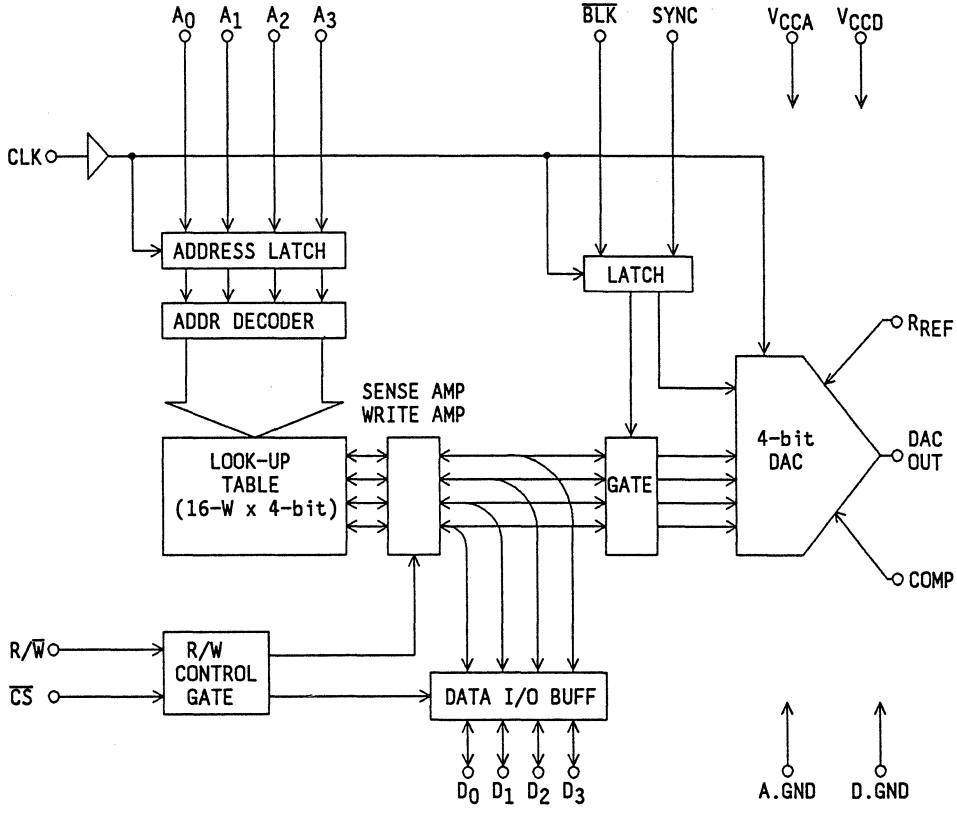
ABSOLUTE MAXIMUM RATINGS (SEE NOTE)

Rating		Symbol	Value	Unit
Power supply voltage		V_{CCA}, V_{CCD}	-0.5 to +7.0	V
Digital input voltage		V_I	-0.5 to +7.0	V
Digital output voltage		V_{OZ}	+5.5	V
Operating temperature		T_A	-55 to +125	°C
Storage temperature	Plastic	T_{STG}	-55 to +125	°C
	Ceramic		-65 to +150	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - BLOCK DIAGRAM



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PIN DESCRIPTION

Pin Name	Description
D_0 to D_3	Data Input/Output to read/write LUT data
CLK	Clock Input for Digital-to-Analog Operation ; Operation Speed is dependent on this input. At the rising edge of this input, A_0 to A_3, $\overline{BLK}$, and SYNC are latched, and converted signal outputs at OUT.
A_0 to A_3	Address Input for LUT ; During displying time, dot data from VRAM is input. During display's flying line period, address is input in order to write or read the data of LUT.
COMP	Terminal for phase compensation capacitance ; Capacitance of 1 µF or more should be inserted between COMP and A.GND.
$\overline{BLK}$	Input to make OUT at blank level ; When $\overline{BLK}$ is at low level, OUT is at blank level. When $\overline{BLK}$ is at high level, content of LUT is converted and outputs at OUT.
A.GND	Ground for Analog circuit
D.GND	Ground for Digital circuit
OUT	Output of digital-to-analog converter ; Load resistance should be inserted between OUT and V_{CCA}.
R_{REF}	Terminal for Reference Resistance ; Reference resistor should be inserted between R_{REF} and V_{CCA}.
SYNC	Input for exclusive-ORed Vertical/Horizontal synchronous signal ; This input is used to obtain composite output. SYNC input should be input while $\overline{BLK}$ is at low level.
R/$\overline{W}$	Mode Switch for Read/Write of LUT This input is effective when $\overline{CS}$ is at low level. When R/$\overline{W}$ is at high level, read mode is selected. When R/$\overline{W}$ is at low level, write mode is selected.
$\overline{CS}$	Chip Select for LUT read/write mode.
V_{CCA}	Power Supply pin for analog circuit
V_{CCD}	Power Supply pin for digital circuit

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CCA}, V_{CCD}	4.75	5.00	5.25	V
Output high current	I_{OH}			-400	μA
Output low current	I_{OL}			8	mA
CLK frequency	f_{CLK}			50	MHz
Phase compensation capacitance	C_{COMP}	1			μF
Operating temperature	T_A	0		70	°C

ELECTRICAL CHARACTERISTICS

Analog DC Characteristics

(V_{CC}=+5.0V±5%, T_A=0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resolution					4	bits
Linear deviation	LE				±1/2	LSB
WHITE level output voltage	V_W		VCCA -15	VCCA	VCCA +15	mV
BLACK level output voltage	V_B	V_{CCA}=5.000V R_{REF}=300Ω Output is pulled up to V_{CCA} at 37.5Ω		4.357		V
BLACK level output voltage	V_{BLANK}			4.286		V
SYNC level output voltage	V_{SYNC}			4.000		V
DAC output voltage	ΔV_{DAC}		0.9	1.0	1.0	V
SYNC output voltage	ΔV_{SYNC}		236	286	336	mV
BLANK output voltage	ΔV_{BLANK}		5	10(71mV)	15	* IRE
GRAY output voltage	ΔV_{GRAY}		85	90(643mV)	95	* IRE

Note: * IRE
The ratio of a reflection signal composition (V_{BLANK} to V_W) and a synchronous signal composition (V_{SYNC} to V_{BLANK}) is 100:40 on EIA RS343A standard.
1/140 of the sum (Reflection signal composition and synchronous signal composition) is named 1IRE which is used as unit of a reflection signal.

Digital DC Characteristics

(V_{CC}=+5.0V±5%, T_A=0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Input high voltage	V_{IH}			2.0			V
Input low voltage	V_{IL}					0.8	V
Input cramp voltage	V_{IC}	V_{CC}=4.75V, I_I=-18mA				-1.5	V
Input high current	I_{IH}	V_{CC}=5.25V	V_I=7V			100	µA
			V_I=2.7V			20	µA
Input low current	I_{IL}	V_{CC}=5.25V, V_I=0.4V				-0.4	mA
Output high voltage	V_{OH}	V_{CC}=4.75V, I_{OH}=-400µA		2.7	3.4		V
Output low voltage	V_{OL}	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
			I_{OL}=8mA		0.35	0.5	V
Output leakage current	I_{OS}	V_{CC}=5.25V		-20		-100	mA
Output current Off condition (Hi-Z)	I_{OZ}	V_{CC}=5.25V	V_O=2.4V			20	µA
			V_O=0.4V			-20	µA
Power supply current	I_{CC}	V_{CC}=5.25V				120	mA

7

SWITCHING CHARACTERISTICS

Video Output

(V_{CC}=+5.0V±5%, T_A=0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
CLK cycle time	t_{CLK}	20			ns
CLK high pulse width	t_{WCLK^+}	7			ns
CLK low pulse width	t_{WCLK^-}	7			ns
Address, $\overline{BLK}$, SYNC high pulse width	t_{WV^+}	18			ns
Address, $\overline{BLK}$, SYNC low pulse width	t_{WV^-}	18			ns
Address, $\overline{BLK}$, SYNC setup time	t_{SV}	6			ns
Address, $\overline{BLK}$, SYNC hold time	t_{HV}	3			ns
Propagation time	t_{PD}			25	ns

LUT Access (Read)

(V_{CC}=+5.0V±5%, T_A=0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ pulse width low level time	t_{WCSR}	100			ns
R/$\overline{W}$ setup time	t_{SRWR}	10			ns
R/$\overline{W}$ hold time	t_{HRWR}	10			ns
$\overline{BLK}$ setup time	t_{SBR}	$2xt_{CLK}+6$			ns
$\overline{BLK}$ hold time	t_{HBR}	$t_{CLK}+3$			ns
Address setup time	t_{SAR}	$2xt_{CLK}+6$			ns
Address hold time	t_{HAR}	$t_{CLK}+3$			ns
Data setup time	t_{DEN}			50	ns
Data hold time	t_{DDIS}	15		50	ns

LUT Access (Write)

(VCC=+5.0V±5%, TA=0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ pulse width low level time	t_{WCSW}	100			ns
R/$\overline{W}$ setup time	t_{SRWW}	10			ns
R/$\overline{W}$ hold time	t_{HRWW}	10			ns
$\overline{BLK}$ setup time	t_{SBW}	$2xt_{CLK}+6$			ns
$\overline{BLK}$ hold time	t_{HBW}	$t_{CLK}+3$			ns
Address setup time	t_{SAW}	$2xt_{CLK}+6$			ns
Address hold time	t_{HAW}	$t_{CLK}+3$			ns
Data setup time	t_{SD}	10			ns
Data hold time	t_{HD}	10			ns

Fig.2 - Video Output Timing Diagram

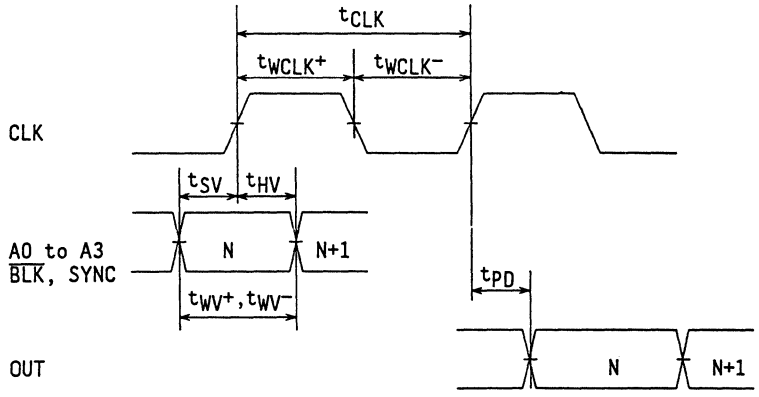


Fig.3 - LUT Access (Read) Timing Diagram

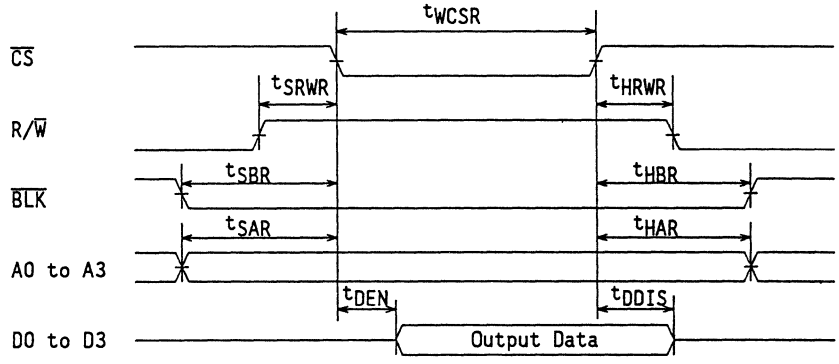


Fig.4 - LUT Access (Write) Timing Diagram

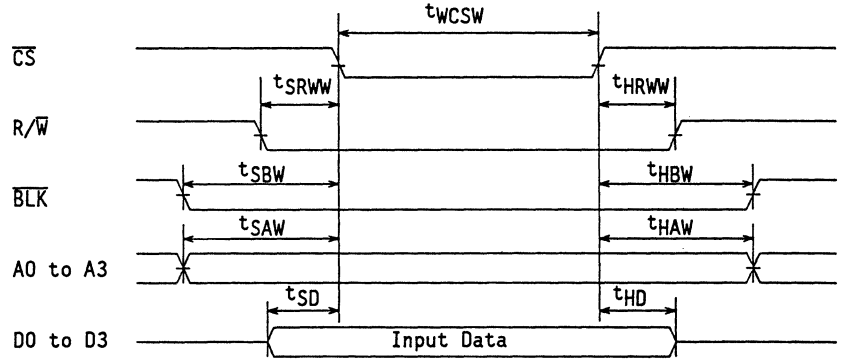
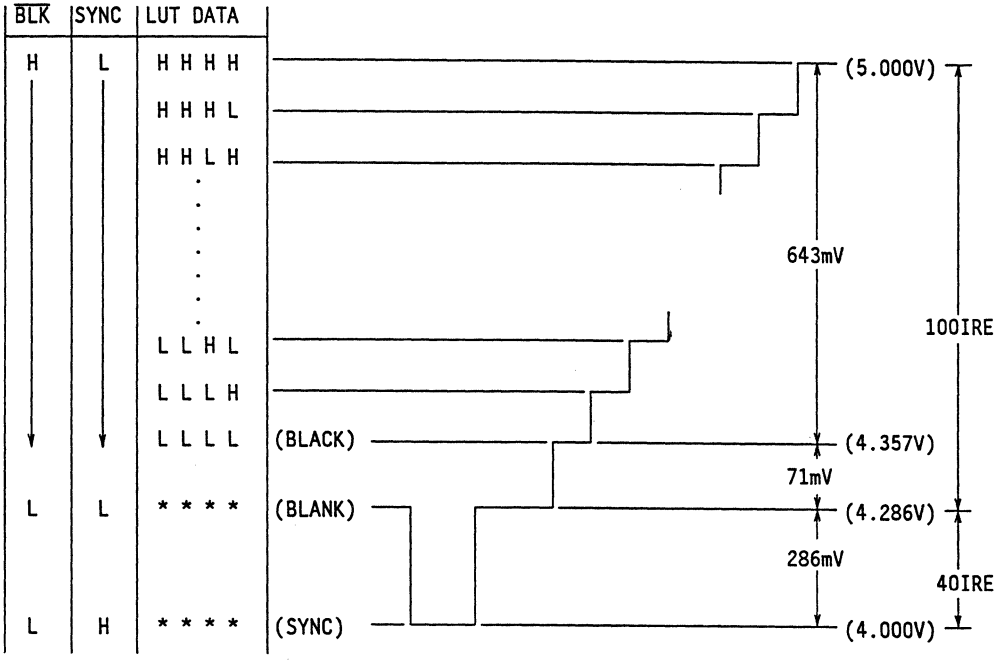


Fig.5 - DAC Output Voltage

MB40874



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Note :
* Don't Care
Output is pulled up to V_{CCA} at 37.5Ω.

Fig.6 - Example of MB40874 Connection Circuit

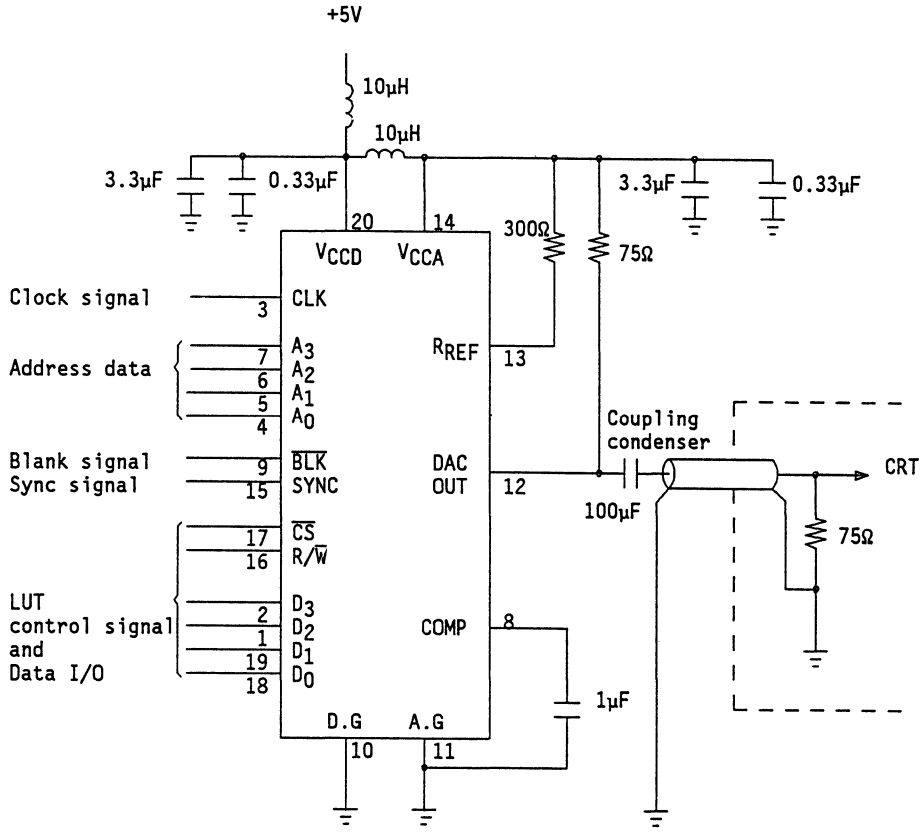

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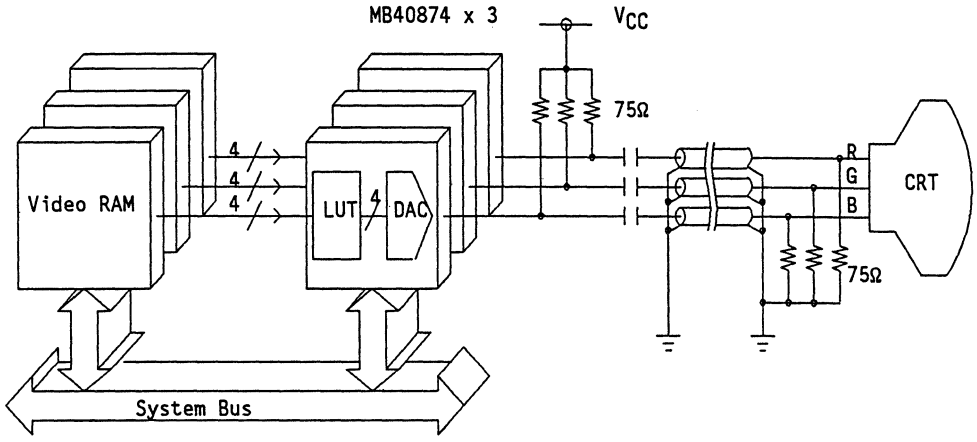
Fig.7 - Application Information



The above application is an example of RGB system using 3 pcs of MB40874. The system allows user to simultaneously display whole 4096 kinds of color defined by the number of bit of LUT and D/A converter and promptly change color tone.

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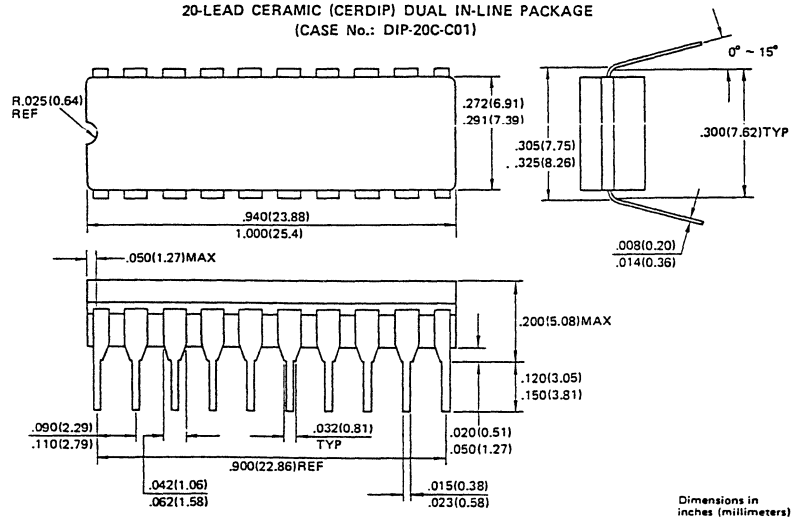
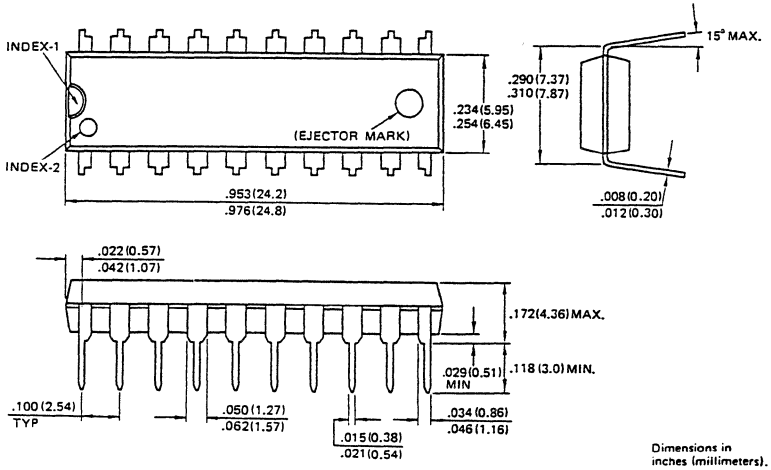
20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C01)



Dimensions in inches (millimeters)

20-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)



Dimensions in inches (millimeters).

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FUJITSU

8-BIT 60MSPS RGB 3-CHANNEL D/A CONVERTER

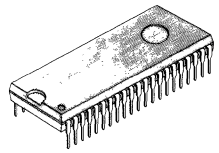
MB40978

July 1988
Edition 2.0

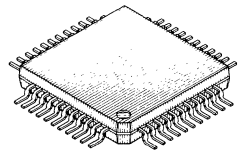
8-BIT 60MSPS RGB 3-CHANNEL D/A CONVERTER

The Fujitsu MB40978 is a 8-bit ultra high speed digital to analog converter for video frequency band fabricated by Fujitsu Advanced Bipolar Technology. Owing to adoption of RGB 3-channel input/output, it is suitable for digital TV, graphic display etc.

- Resolution : 8 bits
- Linearity : ±0.2% max.
- Maximum Conversion Rate : 60 MSPS min.
- Analog Output Voltage Range : V_{CC} to V_{CC}-1V
- Digital Input Voltage : TTL Level
- Single Power Supply Voltage : +5.0V
- Power Dissipation : 350mW typ.
- Package : Plastic DIP Package
  : Plastic Flat Package

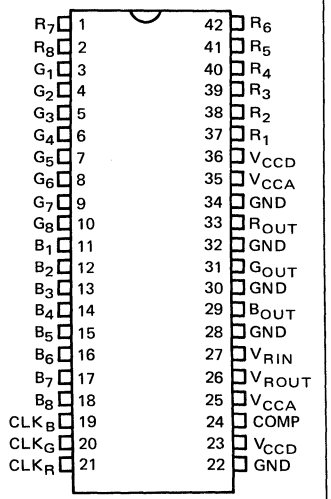


PLASTIC PACKAGE
DIP-42P-M02



PLASTIC PACKAGE
FPT-44P-M01

PIN ASSIGNMENT
TOP VIEW: DIP



TOP VIEW: FPT
See Page 10

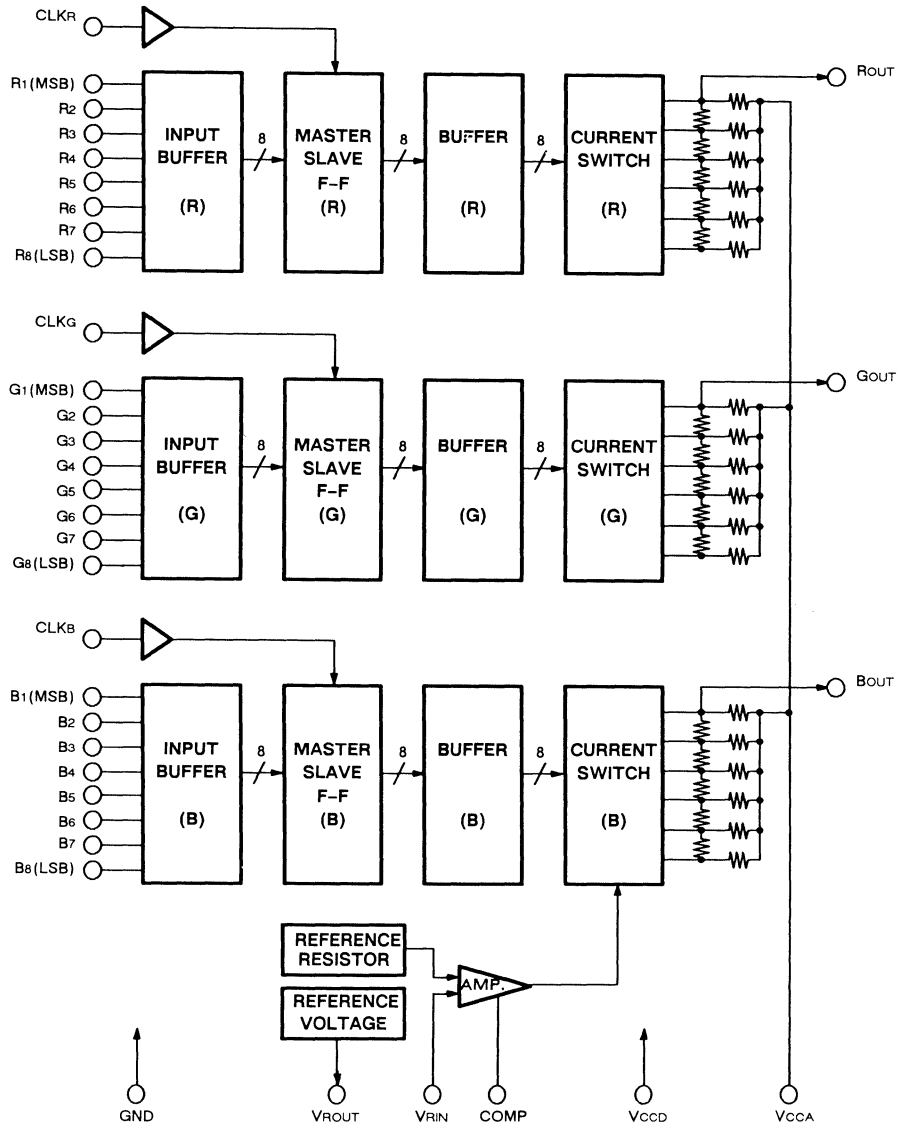
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA}, V_{CCD}	−0.5 to +7.0	V
Digital Input Voltage	V_{ID}	−0.5 to +7.0	V
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB40978 BLOCK DIAGRAM



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PIN DESCRIPTION

Pin Number	Symbol (DIP Pin Assignment)	Descriptions
R_1 to R_8	1, 2, 37 to 42	R-channel Digital Signal Inputs V_{IH} = 2.0V min. V_{IL} = 0.8V max.
G_1 to G_8	3 to 10	G-channel Digital Signal Inputs
B_1 to B_8	11 to 18	B-channel Digital Signal Inputs
R_{OUT}	33	R-channel Analog Signal Output
G_{OUT}	31	G-channel Analog Signal Output
B_{OUT}	29	B-channel Analog Signal Output
CLK_R	21	R-channel Clock Input V_{IH} = 2.0V min. V_{IL} = 0.8V max.
CLK_G	20	G-Channel Clock Input
CLK_B	19	B-channel Clock Input
V_{RIN}	27	Reference Voltage Input V_{CC} = −1.2V min.
V_{ROUT}	26	Reference Voltage Output
COMP	24	This pin is provided to connect a phase compensation capacitance. 1μF min capacitor is connected between GND.
V_{CCA}	25, 35	Power Supply for Analog Circuit 5V ± 5%
V_{CCD}	23, 36	Poer Supply for Digital Circuit 5V ± 5%
GND	22, 28, 30, 32, 34	Ground

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Suppiy Voltage	V_{CCA}, V_{CCD} (V_{CCA}-V_{CCD})	4.75 (−0.2)	5.0	5.25 (0.2)	V
Analog Reference Voltage*	V_{RIN}	3.70	4.00	4.30	V
Digital High-level Input Voltage	V_{IHD}	2.0			V
Digital Low-level Input Voltage	V_{ILD}			0.8	V
Clock Frequency	f_{CLK}			60	MHz
Set-up Time	t_S	10			ns
Hold Time	t_H	4.0			ns
Minimum High Pulse Width	t_{W+}	7.5			ns
Minimum Low Pulse Width	t_{W-}	7.5			ns
Phase Compensation Capacitance	C_{COMP}	1.0			μF
Operating Temperature	T_A	0		70	°C

Note: *$V_{CCA} - V_{REF} \leq 1.2V$

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					8	Bits
Linearity Error	LE				±0.5	LSB
Reference Input Current	I_{RIN}	V_{RIN}, V_{ROUT} Short			10	μA
Reference Output Voltage	V_{ROUT}	V_{CC} = 5.00V	3.900	4.000	4.100	V
Digital High-level Input Current	I_{IHD}	V_{IHD} = 2.7V			20	μA
Digital Low-level Input Current	I_{ILD}	V_{ILD} = 0.4V	−100			μA
RGB Output Voltage Ratio	FSR		0	2	8	%
Full-Scale Output Voltage	V_{OFS}	V_{CC} = 5.00V V_{RIN}, V_{ROUT} Short	V_{CCA} −15	V_{CCA}		mV
Zero-Scale Output Voltage	V_{OZS}	V_{CC} = 5.00V V_{RIN} = 4.00V	3.944	4.004	4.064	V
		V_{CC} = 5.00V V_{RIN}, V_{ROUT} Short	3.884	4.004	4.124	V
Output Resistance	R_O			240		Ω
Power Supply Current	I_{CC}	V_{CC} = 5.25V V_{RIN}, V_{ROUT} Short		*70	102	mA

Note: *V_{CC} = 5.00V

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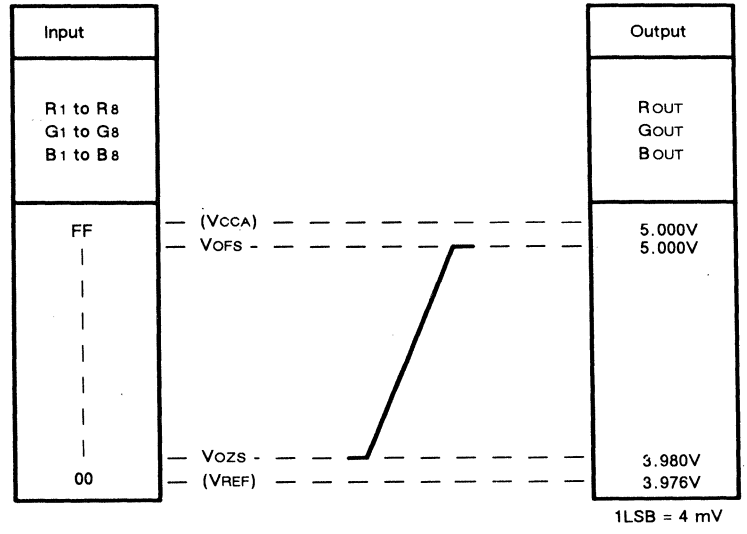
SWITCHING CHARACTERISTICS

(V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Maximum Conversion Rate	F_S	60			MSPS
Output Delay Time	t_{pd}		10		ns
Output Rise Time	t_r		5		ns
Output Fall Time	t_f		5		ns

Fig. 2 – DAC OUTPUT VOLTAGE



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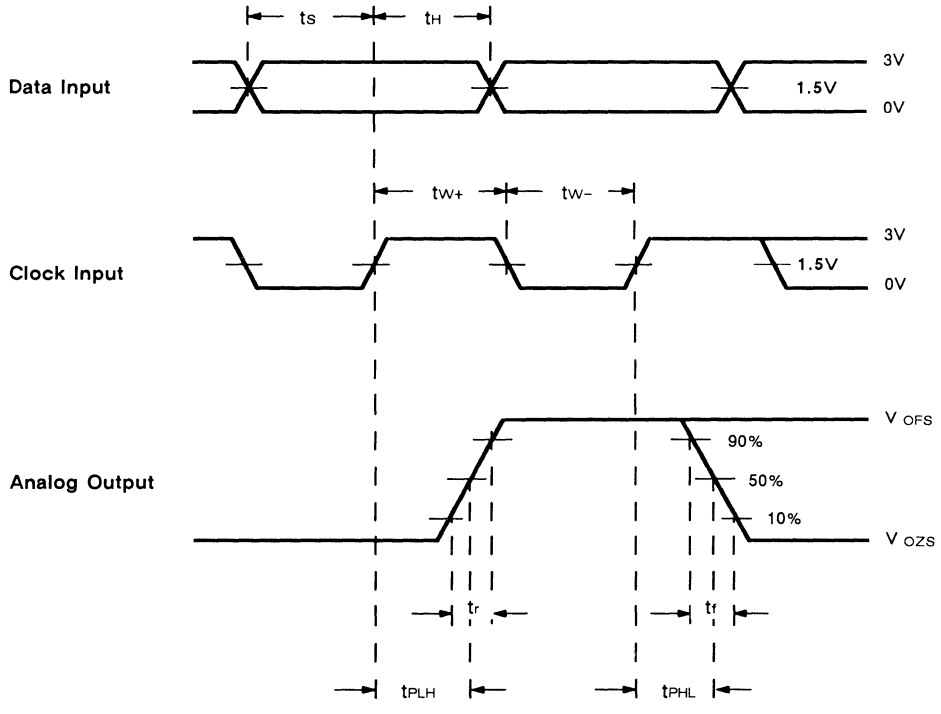
SWITCHING CHARACTERISTICS (continued)

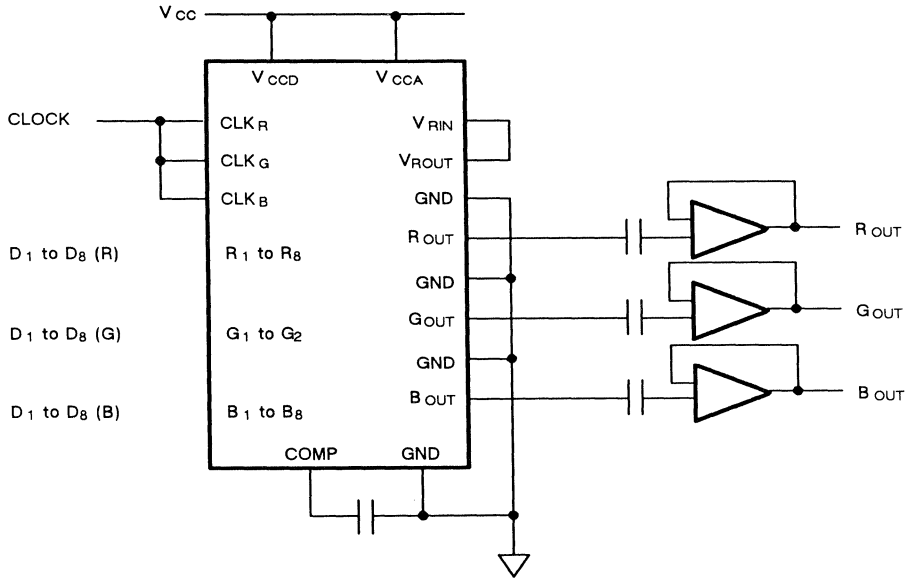
Fig. 3 – TIMING DIAGRAM



7

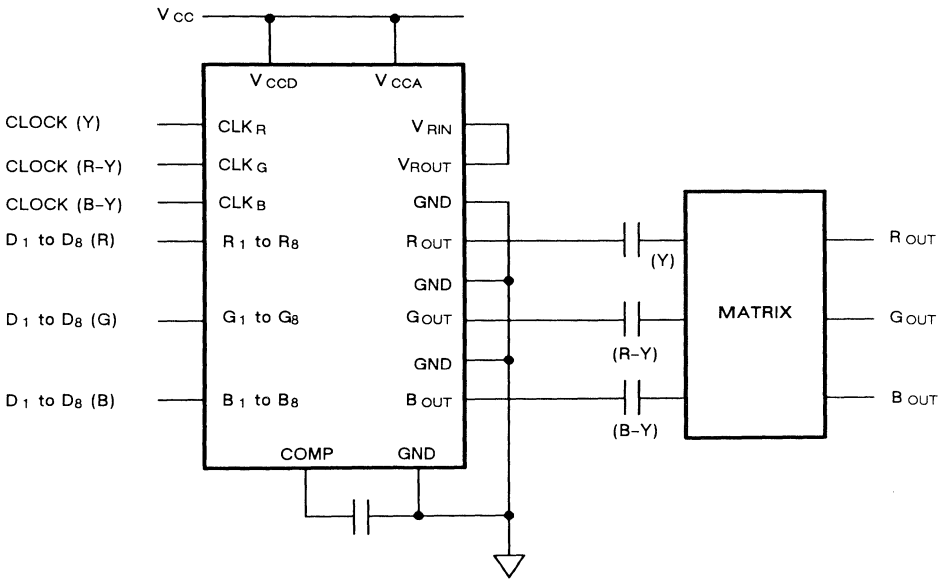
APPLICATION EXAMPLES

Fig. 4 – RGB SIGNAL PROCESS



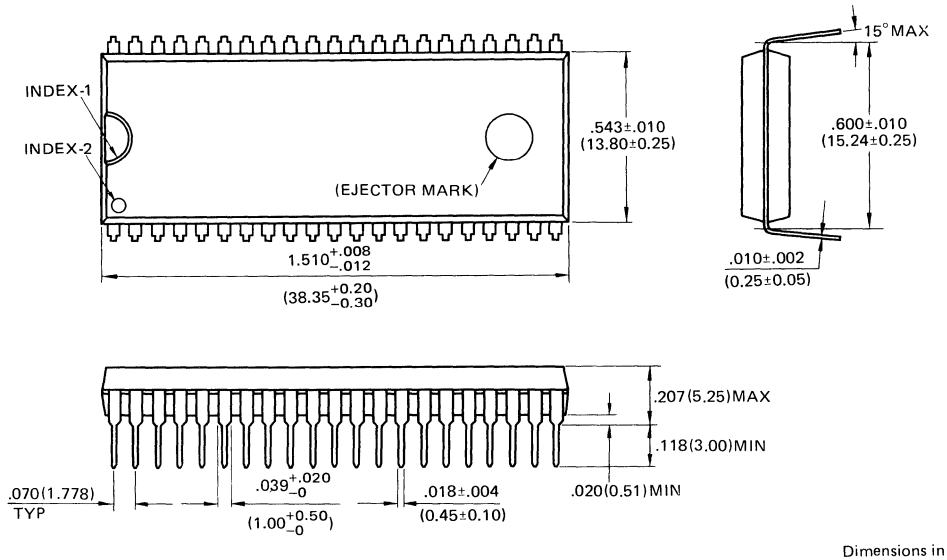
APPLICATION EXAMPLES (continued)

Fig. 5 – COMPONENT SIGNAL PROCESSING



PACKAGE DIMENSIONS

42-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-42P-M02)

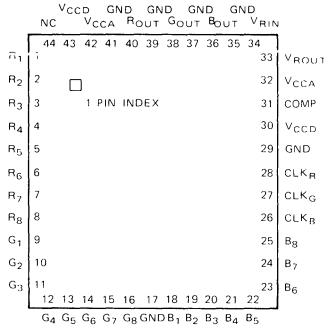


Dimensions in
inches (millimeters)

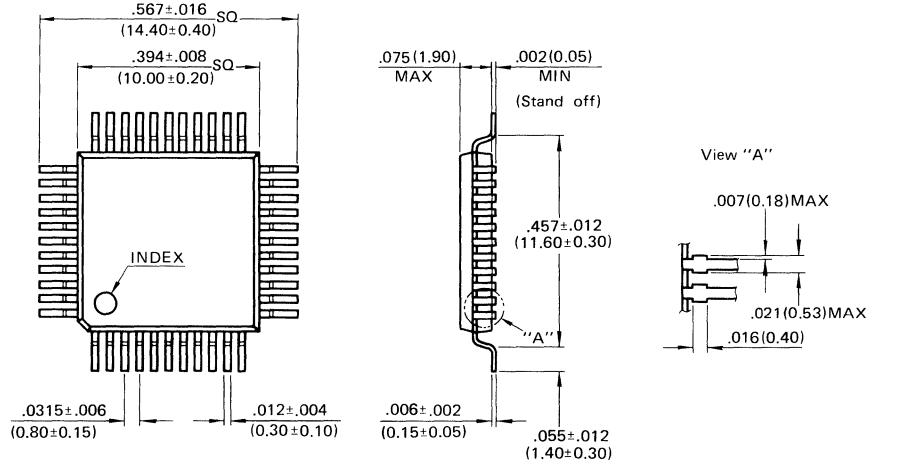
7

PACKAGE DIMENSIONS (continued)

PIN ASSIGNMENT



44-LEAD PLASTIC FLAT PACKAGE
(CASE NO.: FPT-44P-M01)



Dimensions in
inches (millimeters)

FUJITSU

NMOS 13-BIT × 1-CHANNEL, 6-BIT × 3-CHANNEL D/A CONVERTER

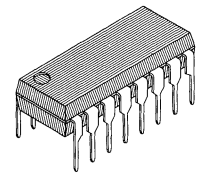
MB88301A

August 1987
Edition 3.2

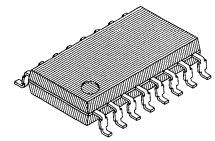
NMOS 13-BIT x 1-CHANNEL, 6-BIT x 3-CHANNEL D/A CONVERTER

The Fujitsu MB 88301A, a pulse width modulation (PWM) type digital-to-analog converter (DAC), is designed for interface with Fujitsu's MB 8840/8850 series and MB 88400/88500 series 4-bit single-ship microcomputers and also with a wide range of general 4-bit and 8-bit microprocessors.

The MB 88301A has four conversion outputs: one 13-bit resolution output and three 6-bit resolution outputs. All outputs generate positive pulse of varying pulse widths. The pulse widths vary in propotion to digital data programmed by the processor in the internal data register. With the connection of external filter circuits to the outputs, the MB 88301A provides an excellent, easy-to-configure DAC.



PLASTIC DIP
DIP-16P-M02

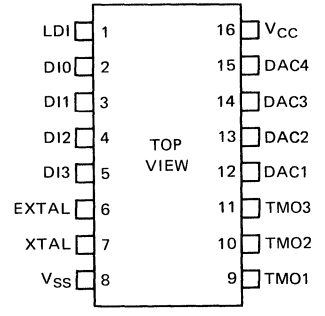


PLASTIC SOP
FPT-16P-M02

FEATURES

- Pulse width modulation D/A converter
- 4-bit parallel address/data loading
- Four on-chip pulse width modulators:
  - 13-bit resolution x 1 channel
  - 6-bit resolution x 3 channels
- On-chip 4 MHz clock generator with external crystal or ceramic resonator
- Clock cycle time / Clock frequency:
  - 0.25μs/4MHz for 13-bit resolution
  - 0.50μs/2MHz for 6-bit resolution
- Three synchronization clock outputs:
  - 2MHz clock output (4MHz divided by 2)
  - 15.625kHz clock output (4MHz divided by 2^8)
  - 488Hz clock output (4MHz divided by 2^{13})
- Single buffered conversion outputs.
- High-voltage open-drain conversion outputs
- Wide operating temperature range: -30°C to +70°C
- Single +5V power supply
- TTL compatible inputs/outputs
- N-channel silicon-gate E/D MOS process
- Two Package Options:
  - 16 pin plastic DIP (Suffix: -P)
  - 16 pin plastic SOP (Suffix: -PF)

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – LOGIC SYMBOL

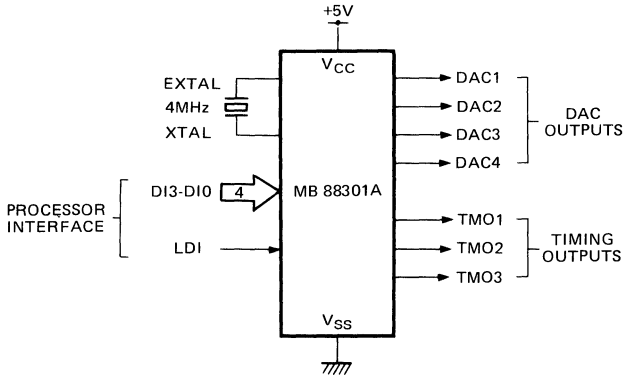
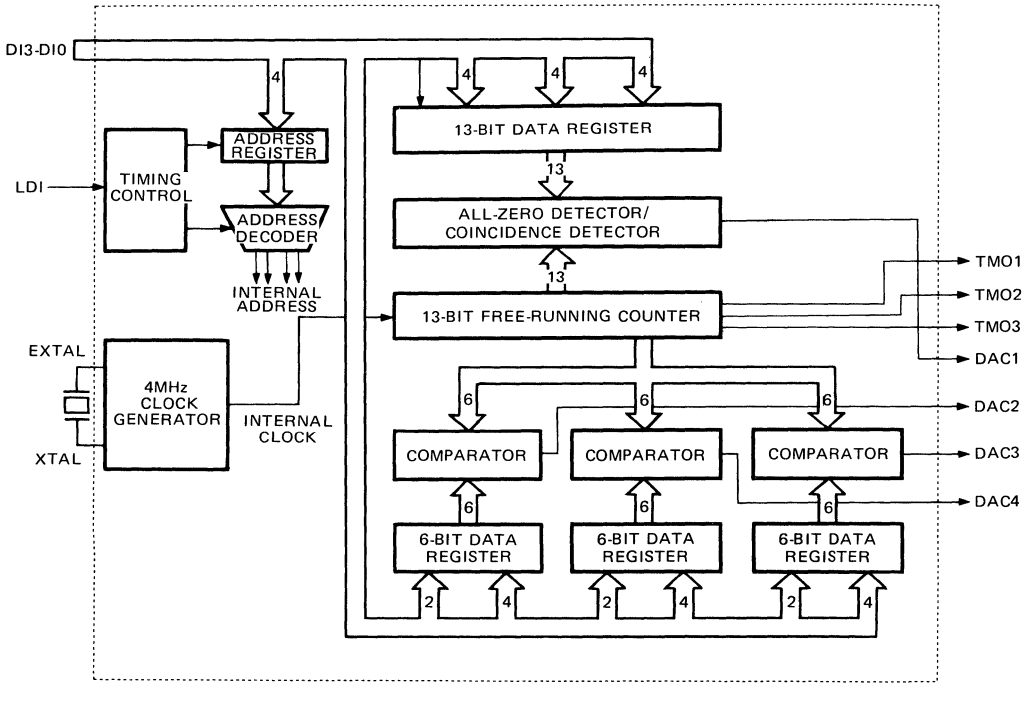


Fig. 2 – BLOCK DIAGRAM



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PIN DESCRIPTION

The MB 88301A has two interfaces: One is the processor interface; D3-D0 and LDI, which are used for the processor to load the MB 88301A device with address and data. Another is the DAC/TIMING interface; DAC4-DAC1 and TM03-TM01, which are used for connection with user-designed external low-pass filter.

Table 1 – PIN DESCRIPTION

Symbol	Pin No.	Type	Function
V_{CC}	16	–	+5V power supply pin.
V_{SS}	8	–	Ground pin.
XTAL	7	–	External 4MHz crystal or ceramic resonator pins for the on-chip clock generator.
EXTAL	6	–	
DI3-DI0	5 to 2	I	4-bit parallel address/data input: The address/data format is that DI3 is the most significant bit (MSB) and that DI0 is the least significant bit (LSB). These inputs are TTL compatible. MSB LSB DI3 | DI2 | DI1 | DI0
LDI	1	I	Write strobe input for a 4-bit address/data: At the leading edge of LDI, a 4-bit address on the ID3 to ID0 inputs is latched into the internal address register. At the trailing edge of LDI, a 4-bit data on the DI3 to DI0 inputs are written into the internal data register designated by the address latched at the leading edge. This input is TTL compatible.
DAC1-DAC4	12 to 15	O	Pulse width modulator outputs (DAC outputs): DAC1: 13-bit resolution (one channel) DAC2-DAC4: 6-bit resolution (three channels) All four outputs are high-voltage open drain.
TMO1-TMO3	9 to 11	O	Synchronization clock outputs (Timing outputs): TMO1: 2MHz (4MHz divided by 2) TMO2: 15.625kHz (4MHz divided by 2^8) TMO3: 488Hz (4MHz divided by 2^{13}) All three clocks have a duty ratio of approximately 50%, and are TTL compatible.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The MB 88301A is a pulse width modulation (PWM) type digital-to-analog converter (DAC). It converts digital data programmed by the processor in the internal data register (13-bit or 6-bit write-only register) into positive pulses. The width of these pulses is propotional to the value of the programmed data, and the cycle time of the pulses is defined by the resolution value (6 or 13 bits). The MB 88301A has four conversion outputs: channel 1 is a 13-bit resolution output DAC1, and channel 2 to 4 are 6-bit resolution outputs DAC2 to DAC4. The converted waveform appears at each DAC output. A user-designed external low-pass filter connected to the DAC output eliminates AC components from the output waveform and converts the waveform into a DC voltage propotional to the pulse width.

DIGITAL DATA INPUT

Fig. 3 shows the input timing of digital data to be converted: Digital data to define the width of the positive pulse is written into the 13-bit and 6-bit internal data registers through the DI3 to DI0 4-bit address/data inputs using the write strobe input LDI. At the leading edge of LDI, a 4-bit address on the DI3 to DI0 inputs is latched into the internal address register. At the trailing edge of LDI, a 4-bit data on the DI3 to DI0 inputs is loaded into the internal data register designated by the address register.

Fig. 4 shows the address/data format: DI3 is the most significant bit (MSB) and DI0 is the least significant bit (LSB).

Fig. 5 shows the internal data register address map: The whole space size is 10 words. Addresses #0 to #3, addresses #4 and #5, addresses #6 and #7, and addresses #8 and #9 are assigned to DAC1, DAC2, DAC3 and DAC4, respectively. Fig. 6 shows the internal data register format: To the DAC1 data register, three 4-bit and one 1-bit digital data must be written. To the DAC2 to DAC4 data registers, one 4-bit and one 2-bit digital data must be written.

Fig. 5 — INTERNAL DATA REGISTER ADDRESS MAP

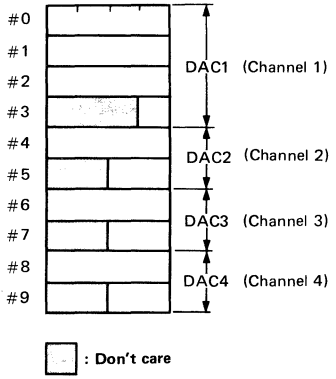


Fig. 3 — ADDRESS/DATA INPUT TIMING

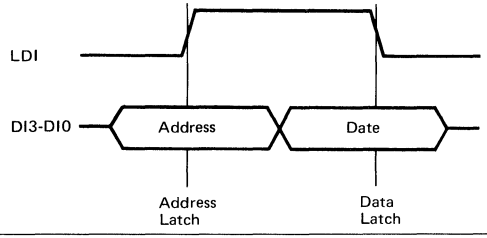


Fig. 4 — ADDRESS/DATA FORMAT

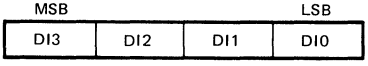
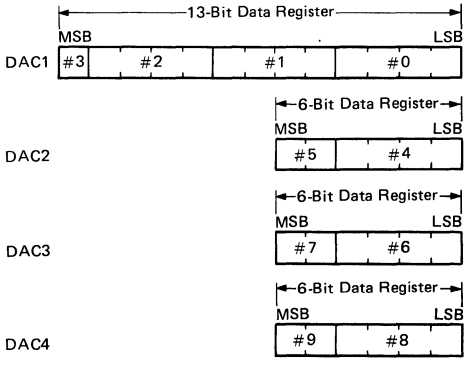


Fig. 6 — INTERNAL DATA REGISTER FORMAT



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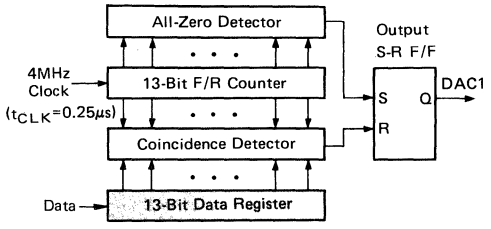
PULSE WIDTH MODULATION/DAC OUTPUT WAVEFORM Fig.

• 13-Bit Resolution D/A Converter: DAC1

Fig. 7 shows the configuration of the 13-bit resolution pulse width modulator: The on-chip clock generater provides 4MHz clock for the 13-bit free-running counter. When all bits of the counter is zero, the all-zero detector sets the output R-R-S flip-flop. The coincidence detector compares the counter with the data register. When they match, the coincidence detector resets the output flip-flop. The waveform appearing at the DAC1 output depends on the data register value, shown in Fig. 8.

Fig. 7 — 13-BIT PULSE WIDTH MODULATOR CONFIGURATION



• 6-Bit Resolution D/A Converters: DAC2 to DAC4

Fig. 9 shows the configulation of the 6-bit resolution pulse width modulator: The 2MHz clock that is the output of Bit 1 of the 13-bit free-running counter drives the 6-bit free-running counter. This 6-bit counter is also part of the 13-bit counter (Bits 2 to 7). The comparator compares the counter with the data register every cycle. When the counter value is equal to or less than the data register value, the comparator outputs a high level at the DAC output. When the counter value exceeds the date register value, the comparator outputs a low level at the DAC output. This produces the waveforms at the DAC2, DAC3, and DAC4 outputs, shown in Fig. 10.

Fig. 9 — 6-BIT PULSE WIDTH MODULATOR CONFIGURATION

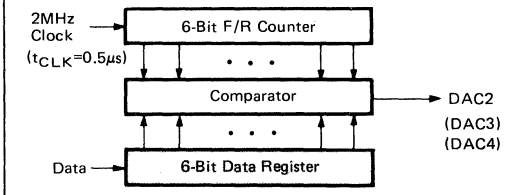


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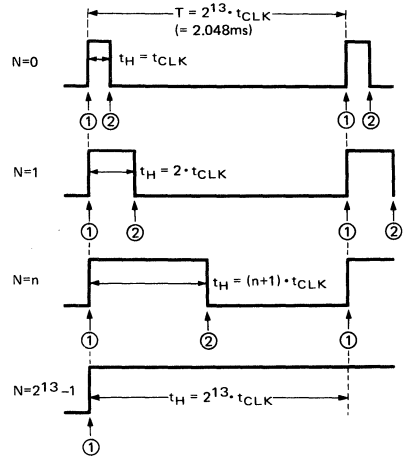
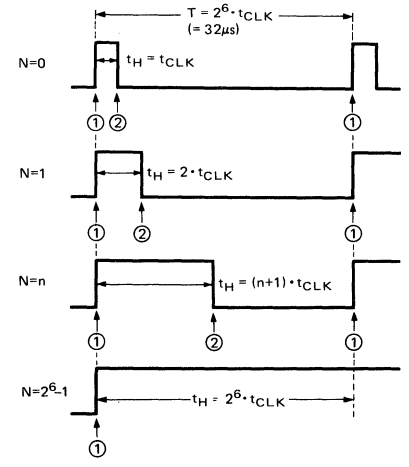
Fig. 8 — DAC1 OUTPUT WAVEFORM



NOTES: N : DATA REGISTER VALUE ($0 \leqq N \leqq 2^{13}-1$)
T : PULSE CYCLE TIME ($T = 2^{13} \cdot t_{CLK}$ = 2.048ms)
t_H : PULSE WIDTH ($t_H = (N+1) \cdot t_{CLK}$)
t_{CLK} : COUNTER CLOCK CYCLE TIME (t_{CLK} = 1/4MHz = 0.25μs)
① : COUNTER IS ZERO.
② : COUNTER MATCHES DATA REGISTER.

Fig. 10 — DAC2/DAC3/DAC4 OUTPUT WAVEFORM



NOTES: N : DATA REGISTER VALUE ($0 \leqq N \leqq 2^6-1$)
T : PULSE CYCLE TIME ($T = 2^6 \cdot t_{CLK}$ = 32μs)
t_H : PULSE WIDTH ($t_H = (N+1) \cdot t_{CLK}$)
t_{CLK} : COUNTER CLOCK CYCLE TIME (t_{CLK} = 1/2MHz = 0.5μs)
① : COUNTER IS ZERO. (OVERFLOW)
② : COUNTER EXCEEDS DATA REGISTER.

EXTERNAL FILTER CONFIGURATION

The on-chip pulse width modulator generates positive pulse waveforms similar to the one shown in Fig. 12 at the DAC outputs (DAC1 to DAC4). The pulse width (t_H) is proportional to the digital data programmed into the data register. The cycle time (T) is determined by the resolution value (6 or 13 bits).

User-designed low-pass filters are required at the DAC outputs to eliminate AC components from the output waveform and to convert the waveform to a DC voltage. Fig. 11 shows an example of a simple output configuration in which an RC integrator is used as the low-pass filter. With this circuit, the DAC waveform shown in Fig. 12 is converted to the V_{OUT} output waveform shown in Fig. 13 Ripple and response time (t_R) depend on the time constant of the RC filter. A longer time constant reduces ripple but increases response time. A time constant that best meets the tradeoff between desired accuracy and response time should be chosen. Also, since the DAC outputs are high-voltage open drain, they can externally be pulled up to a power supply higher than 5V. This prevents the output voltage from attenuating through the external low-pass filters.

Note:
The low-pass filter shown in Fig. 11 is just an example. In actual practice, depending on the user's system design, additional amplifiers, multi-stage filters, and other circuits will be needed for the external low-pass filter.

NOTICE

To change the DC output voltage of the external low-pass filter, the data register value must be updated to vary the positive pulse width (duty ratio) of the DAC output. However, all bits on the data register can not be changed at the same time. They are updated a nibble at a time by the 4-bit parallel data loading. In addition, the DAC output is single buffered. Because of this nibble-by-nibble update and single buffering, the data register value during update may become transient. During this pulse cycle, depending on the transient value, an undesirable duty ratio disturbance may occur at the DAC output, affecting the filter output. It is therefore necessary to design the output filter so that such disturbances in the DAC output waveform will not appear at the filter output. This notice applies to both the 13-bit and 6-bit resolution converters. With the 13-bit resolution converter, however, it is possible to avoid such disturbance by software. This is done by controlling the update timing of the data register value through monitoring of the DAC1 output and the TMO3 output waveforms.

Also, note the following thing when the DAC1 output is used: In the steady state where the DAC1 data register bits are all set (i.e., data is "1FFF") the DAC1 output remains high. But, when the data is updated, there is a possibility that the DAC1 output may become undefined during that output cycle time (less than one cycle time). To avoid this phenomenon, the following method is utilized:

1. Not use data of "1FFF", or
2. Change the DAC1 data register value (i.e., "1FFF") just before the counter become full (i.e., all bits are set). Since in this case an undesired pulse due to the data change may appear at the DAC1 output, the pulse must be eliminated with the external filter.

Fig. 11 — OUTPUT CIRCUIT CONFIGURATION (EXAMPLE)

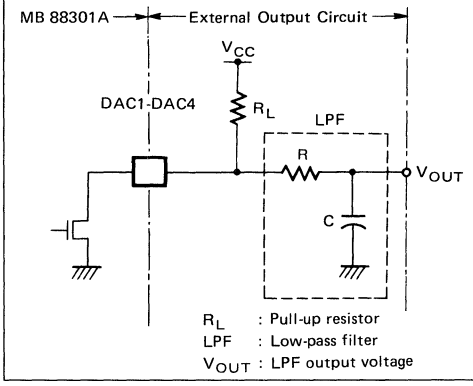


Fig. 12 — DAC OUTPUT WAVEFORM

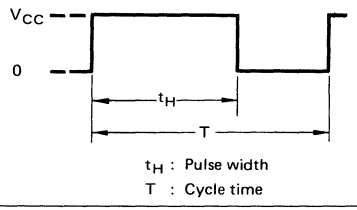
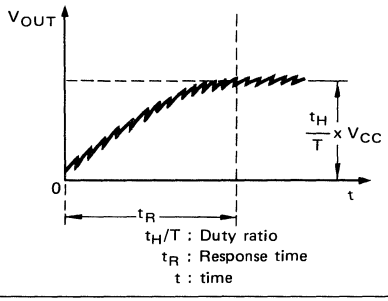


Fig. 13 — V_{OUT} OUTPUT WAVEFORM



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Pins/Conditions	
Supply Voltage	V_{CC}	V_{SS} −0.3 to V_{SS} +8.0	V	V_{CC}	V_{SS} = 0 V
Input Voltage	V_{IN}	V_{SS} −0.3 to V_{SS} +8.0	V	DI0-DI3, LDI, EXTAL, XTAL	
Output Voltage	V_{OUT}	V_{SS} −0.3 to V_{SS} +15.0	V	DAC1-DAC4	
		V_{SS} −0.3 to V_{SS} +8.0		TMO1-TMO3	
Operating Temperature	T_A	−30 to +70	°C	Ambient temperature	
Storage Temperature	T_{stg}	−55 to +150	°C		

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}		0		
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}	− 0.3		0.8	V
Clock Frequency*	f_c	0.5		4.0	MHz
Operating Temperature	T_A	−30		70	°C

NOTE: * Crystal or ceramic resonator should be used. See Fig. 17.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pins/Conditions	Value			Unit
			Min.	Typ.	Max.	
Output High Voltage	V_{OH}	TMO1-TMO3 I_{OH} = −200μA	2.4			V
		DAC1-DAC4	Open Drain			
Output Low Voltage	V_{OL}	TMO1-TMO3 I_{OL} = 1.8mA			0.4	V
		DAC1-DAC4 I_{OL} = 2.0mA, 5kΩ External Pull Up Resistor			0.8	V
Output Leakage Current	I_{LOH}	DAC1-DAC4 V_{OH} = 13.2V, OFF State			50	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, All Outputs Open		15	25	mA

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pins/Conditions	Min.		Max.	Unit
LDI Pulse Width	P_{WLDI}	LDI Fig. 14, Fig. 16	5			μs
LDI Rise/Fall times	t_{rLDI} t_{fLDI}	LDI Fig. 14, Fig. 16			1.5	μs
Address/Data Setup Time	t_S	DI3 - DI0 Fig. 14, Fig. 16	0.5			μs
Address/Data Hold Time	t_H	DI3 - DI0 Fig. 14, Fig. 16	2			μs
TMO Rise/Fall times	t_{rTMO} t_{fTMO}	TM01-TM03 Fig. 15, Fig. 16			0.2	μs

Fig. 14 — ADDRESS/DATA INPUT TIMING

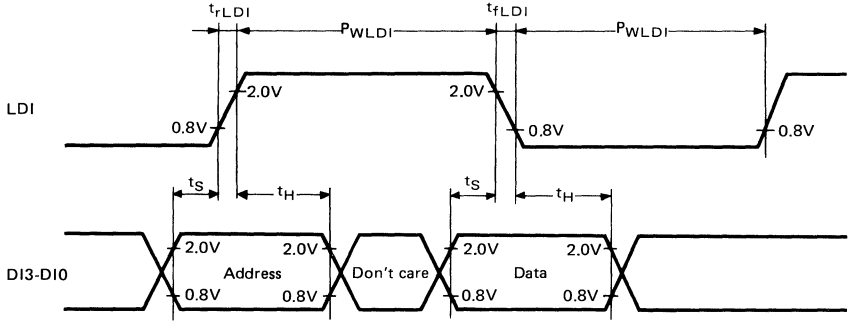

Fig. 15 — SYNCHRONIZATION CLOCK OUTPUT TIMING

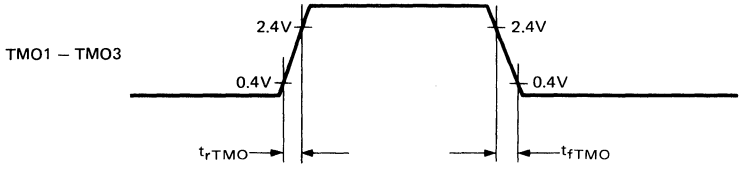

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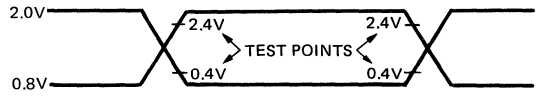
Fig. 16 – AC TEST CONDITIONS

INPUT CONDITIONS

- Input Levels:
  2.0V for a logic "1"
  0.8V for a logic "0"



OUTPUT CONDITIONS

- Timing Reference Levels:
  2.4V for a logic "1"
  0.4V for a logic "0"
- Output Load Circuit:
  C_L = 100pF (including scope and jig capacitances)
  R_L = 4kΩ

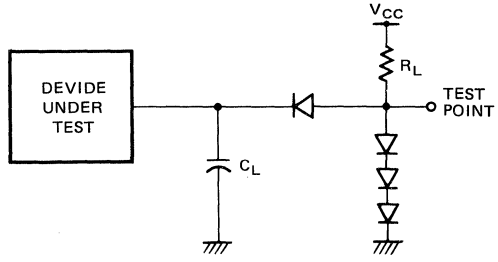


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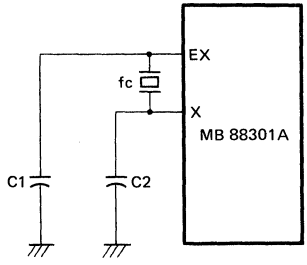
Fig. 17 – CRYSTAL/CERAMIC OSCILLATOR CIRCUIT

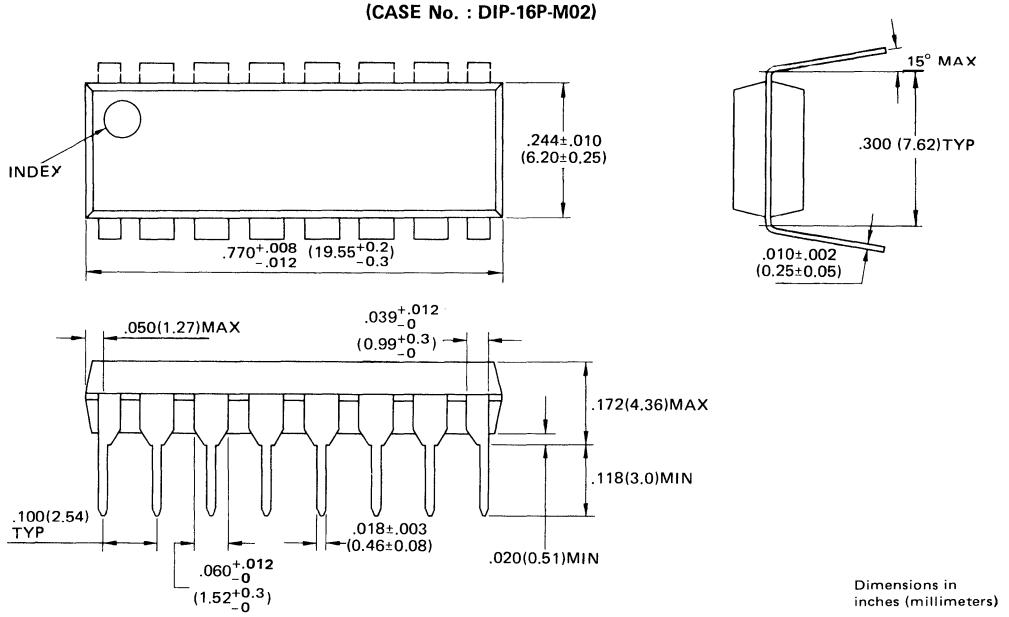


fc = 4MHz
C1 = C2 = 20pF – 60pF

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M02)



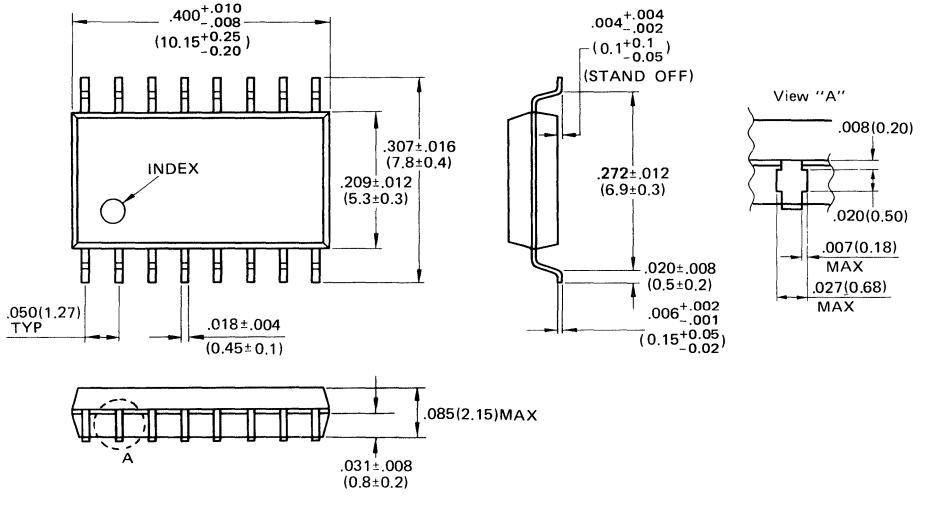
Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS

PLASTIC SOP(Suffix: -PF)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

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March 1988
Edition 1.0

FUJITSU

FUJITSU MICROELECTRONICS, INC.

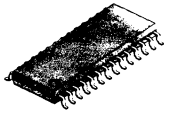
MB40176

Product Profile

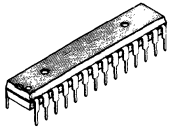
6-Bit AD/DA Converter with Clamp Circuit

The Fujitsu MB40176 is a low power 6-bit AD/DA converter fabricated with Fujitsu Advanced Bipolar Technology.

The MB40176 is suitable for video signal processing with on-chip clamp and reference circuitry.



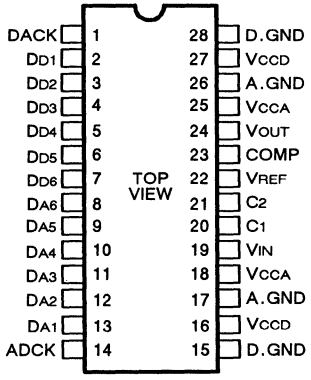
PLASTIC PACKAGE
FPT-28P-M01



PLASTIC PACKAGE
DIP-28P-M04

- Resolution: 6 bits
- Linearity: ±0.8% max.
- Maximum Conversion Rate: 20MHz min.
- Analog Input Voltage Range: 0 to 1.0V
- Digital Output Voltage Range: V_{CC} to V_{CC} -1V
- Digital I/O Level: TTL Level
- Power Supply Voltage: +5V
- Power Dissipation: 300mW typ.
- Package
  28-pin Plastic FLAT Package (Suffix: -PF)
  28-pin Plastic DIP Package (Suffix: -P)

PIN ASSIGNMENTS



ABSOLUTE MAXIMUM RATINGS (See Note)

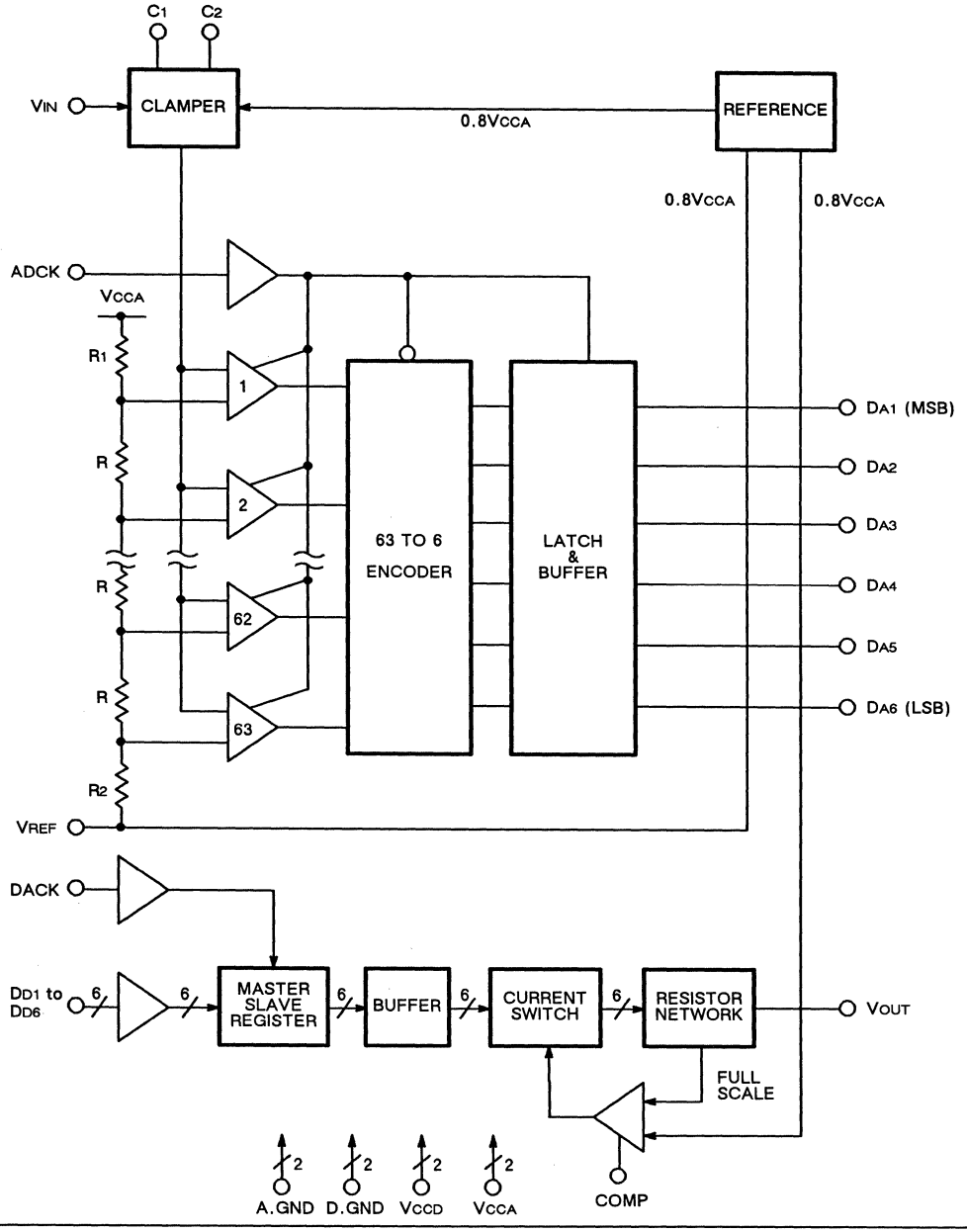
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA}, V_{CCD}	-0.5 to +7.0	V
Digital Input Voltage	V_{IND}	-0.5 to +7.0	V
Analog Input Voltage	V_{INA}	-0.5 to V_{CC} +0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RAT-INGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended peri-ods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1 — MB40176 BLOCK DIAGRAM



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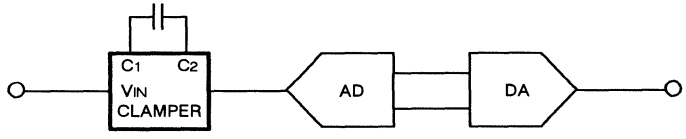
Pin Descriptions

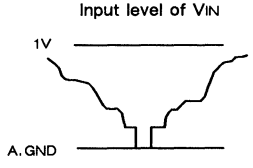
Section	Symbol	Pin No.	Description
A/D	V_{IN}	19	Analog signal input.
	V_{REF}	22	Reference voltage output.
	D_{A1} to D_{A6}	8 to 13	Digital signal outputs.
	C_1, C_2	20, 21	Clamp capacitor is connected between these pins.
	ADCK	14	A/D conversion clock.
D/A	V_{OUT}	24	Analog signal output.
	D_{D1} to D_{D6}	2 to 7	Digital signal inputs.
	COMP	23	Phase compensation capacitor is connected.
	DACK	1	D/A conversion clock input.
Common	V_{CCA}	18, 25	Power supply for analog circuit.
	V_{CCD}	16, 27	Power supply for digital circuit.
	A.GND	17, 26	Ground for analog circuit.
	D.GND	15, 28	Ground for digital circuit.

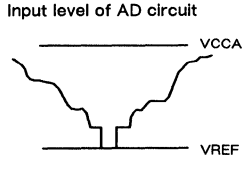
Functional Description

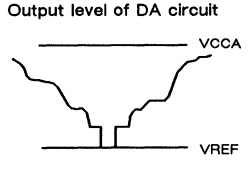
Clamper Operation

The on-chip clamp circuit is a peak detector which limits the sync level at the top of the composite signal. Clamp voltage is common to the reference voltage (0.8Vcc) of AD and DA circuits.









Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA}, V_{CCD}	4.75	5.0	5.25	V
Digital High-level Input Voltage	V_{IHD}	2.0			V
Digital Low-level Input Voltage	V_{ILD}			0.8	V
Clock Frequency	f_{CLK}			20	MHz
Clock Pulse Width at High Level	t_{W+}	20			ns
Clock Pulse Width at Low Level	t_{W-}	20			ns
Set-up Time	t_S	12.5			ns
Hold Time	t_H	12.5			ns
Phase Compensation Capacitance	C_{COMP}	1.0			µF
Clamp Capacitance	C_{CLAMP}	1.0			µF
Reference Voltage Capacitance	C_{VREF}	1.0			µF
Operating Temperature	T_A	0		70	°C

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Electrical Characteristics

ANALOG CIRCUIT DC CHARACTERISTICS
(VCCA = VCCD = 5V±5%, TA = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					6	Bits
Linearity Error	LE	DC			±0.5	LSB
Analog Input Current	IIN		-400			μA
Reference Voltage	VREF*			4.0	4.1	V
Clamp Voltage	VCLP			VREF		V
Full Scale Output Voltage	VOFS			VCCA		V
Zero Scale Output Voltage	VOZ			VREF		V
Output Resistance	RO			240		Ω
Power Supply Current	ICC			60*	90	mA

Note: *VCCA = VCCD = 5.0V

DIGITAL CIRCUIT DC CHARACTERISTICS
(VCCA = VCCD = 5V±5%, TA = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Digital High-level Output Voltage	VOHD		2.7			V
Digital Low-level Output Voltage	VOLD	IOL = 1.6mA			0.4	V
Digital High-level Input Voltage	VIHD		2.0			V
Digital Low-level Input Voltage	VILD				0.8	V
Digital High-level Input Current	IIHD				20	μA
Digital Low-level Input Current	IILD		-100			μA

SWITCHING CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		20			MSPS
Digital Output Delay Time	tPDD			15	30	ns
Analog Output Delay Time	tPDA			13		ns
Analog Output Rise Time	tr			15		ns
Analog Output Fall Time	tf			15		ns

Fig. 2 — APPLICATION CIRCUIT

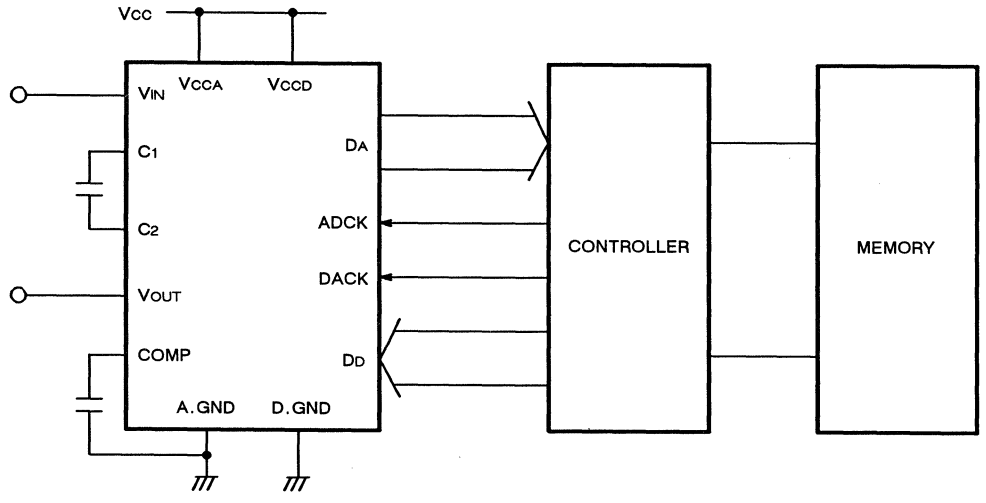

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Fig. 3 — TYPICAL CONNECTION EXAMPLE

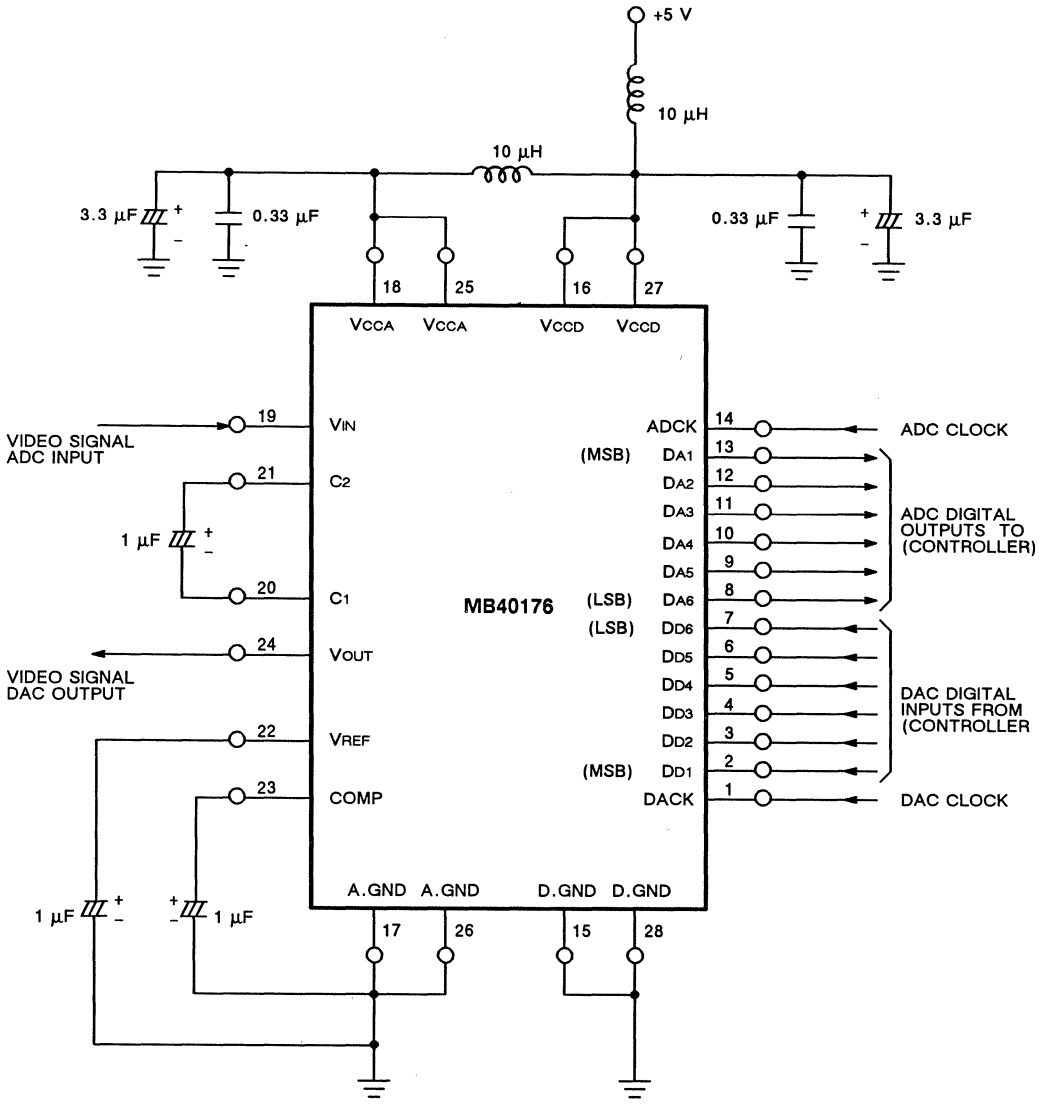
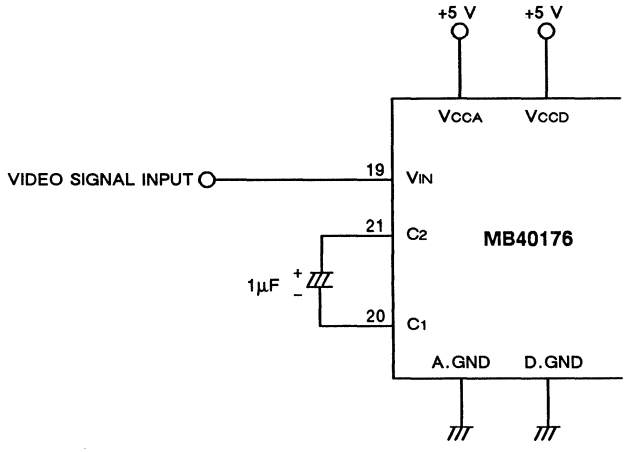
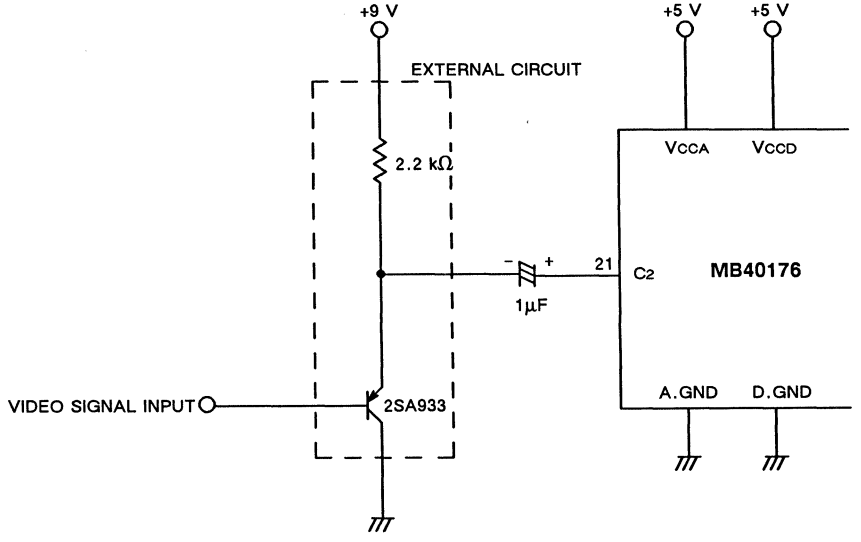


Fig. 4 — CONNECTION EXAMPLE (ON-CHIP INPUT PNP TRANSISTOR IS UTILIZED.)



Note: Input impedance of VIN input pin (19) is about 20 kΩ.

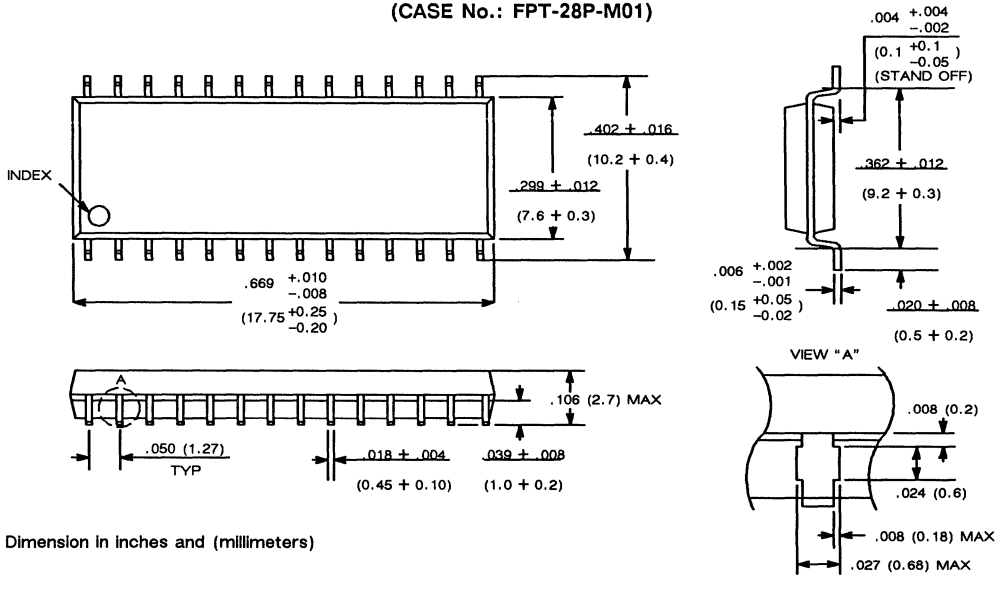
Fig. 5 — CONNECTION EXAMPLE (INPUT PNP TRANSISTOR OF CLAMPER CIRCUIT IS PUT EXTERNALLY.)



Note: Both VIN (19) and C1 (20) are connected with VCCA.

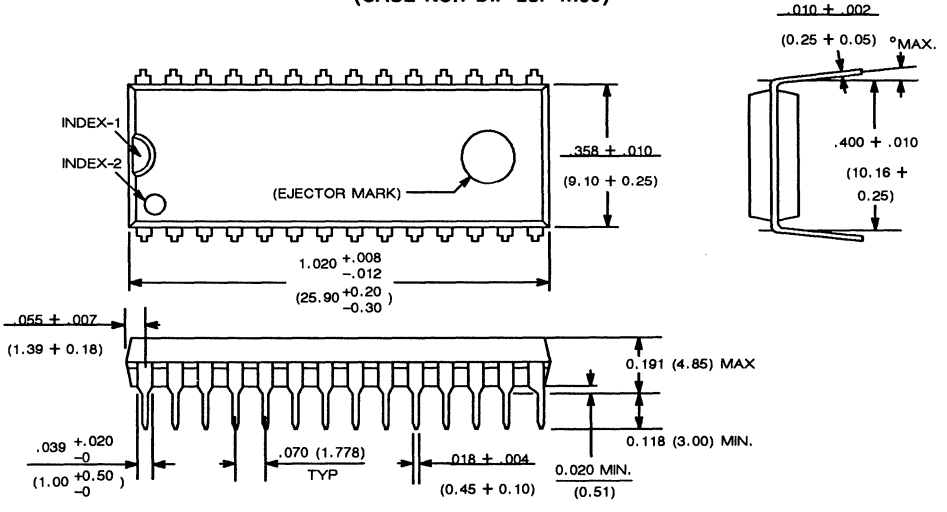
Package Dimensions

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M01)



Dimension in inches and (millimeters)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M03)



Dimension in inches and (millimeters)

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March 1988
Edition 1.0

FUJITSU

FUJITSU MICROELECTRONICS, INC.

MB87020

Product Profile

16-Bit A/D and D/A Combination Converter

The Fujitsu MB87020 is a 16-bit combined Analog-to-Digital and Digital-to-Analog converter with a conversion rate of 50 Kilosamples per second. A/D or D/A mode is selected under control of a MODE input.

The MB87020's 50KHz speed and 16-bit resolution with 12-bit linearity make it ideal for audio applications such as studio quality digital recording.

The selectively synchronous/asynchronous bidirectional 8- and 16-bit data I/O structure allows easy interface to a variety of computing environments. Serial I/O is also available. The need for external circuitry is reduced with on-chip reference voltage generation, analog sample and hold; external reference voltage sources can be used if desired. The low power circuit includes a stand-by power-down mode.

The MB87020 is fabricated with Fujitsu's advanced CMOS technology and is available in a 40-pin plastic DIP.

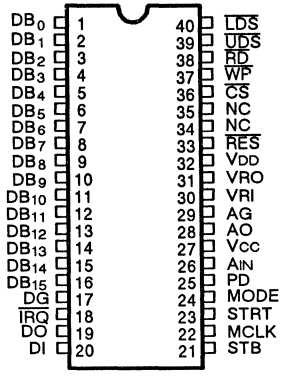
MB87020 Features

- 16-bit A/D and D/A combined in one package
- 12-bit linearity
- 8/16 synchronous/asynchronous parallel I/O
- Serial I/O
- On-chip reference voltage with external reference capability
- On-chip sample and hold circuitry
- ±5V power supplies
- 40 pin plastic package
- External reference

7

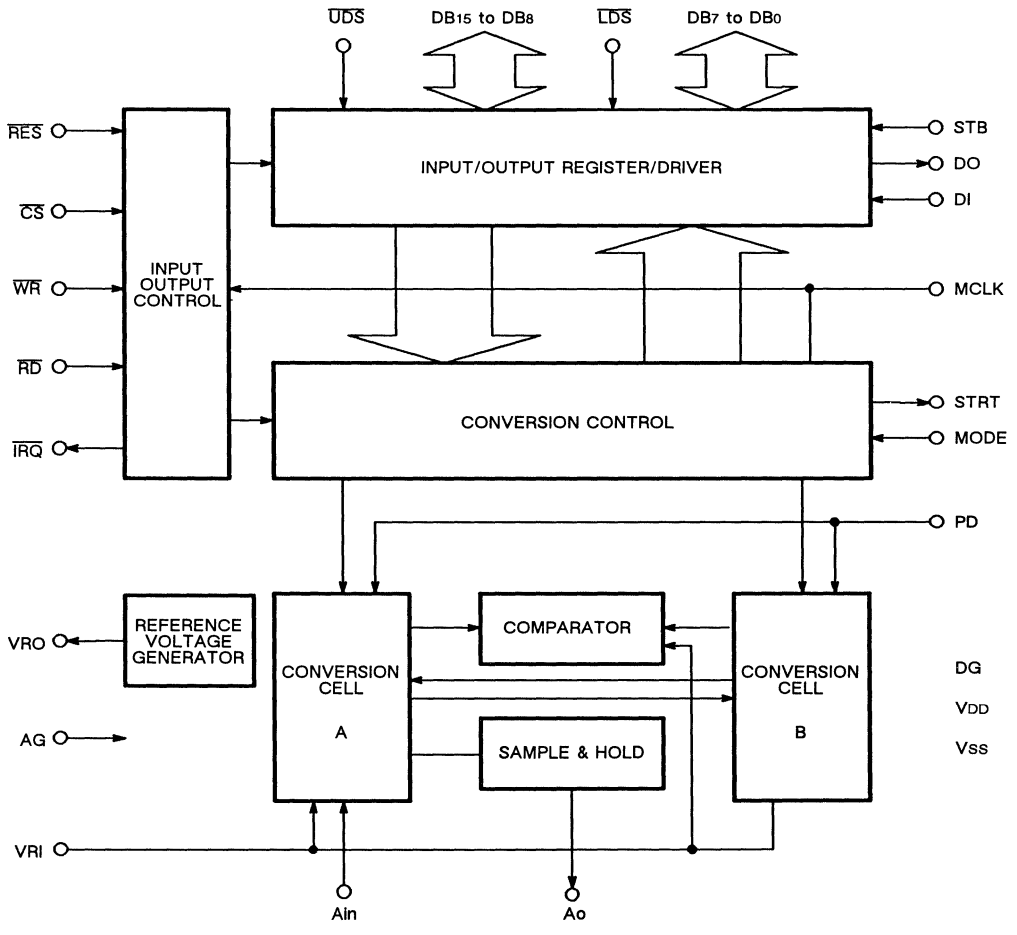
PIN ASSIGNMENTS

(TOP VIEW)



(DIP-40P-M01)

MB87020 BLOCK DIAGRAM



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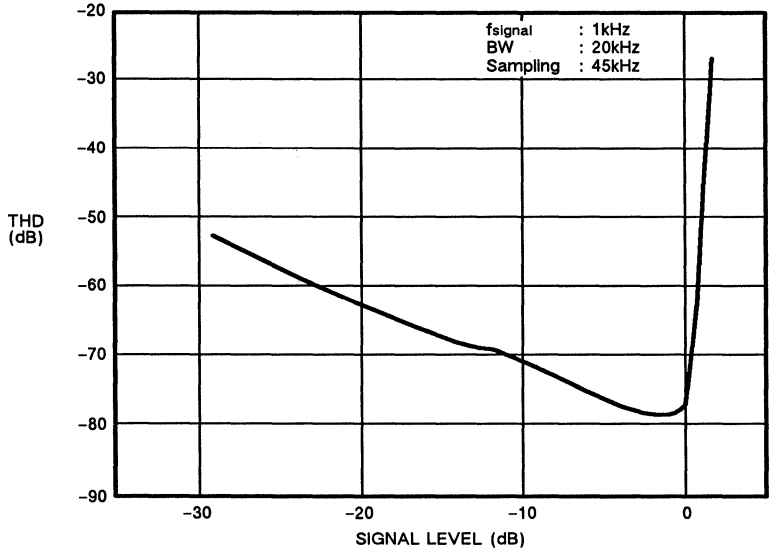
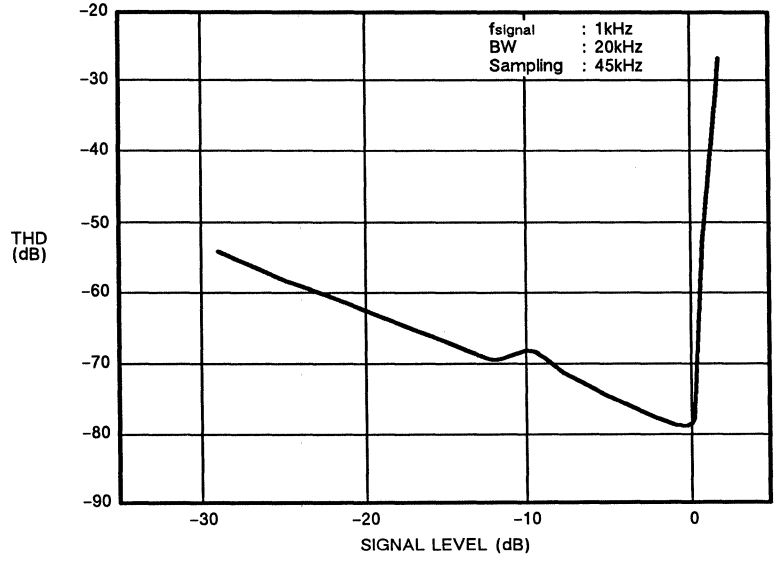
SIGNAL LEVEL vs. DISTORTION (A/D MODE)

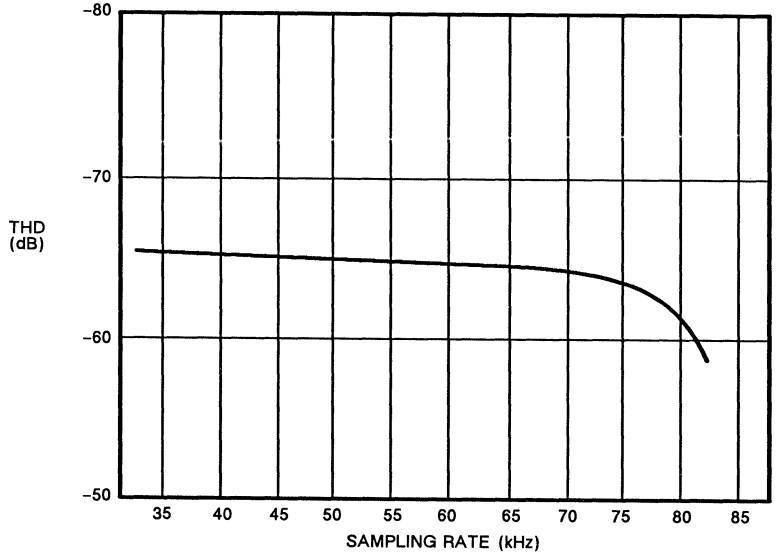


SIGNAL LEVEL vs. DISTORTION (D/A MODE)

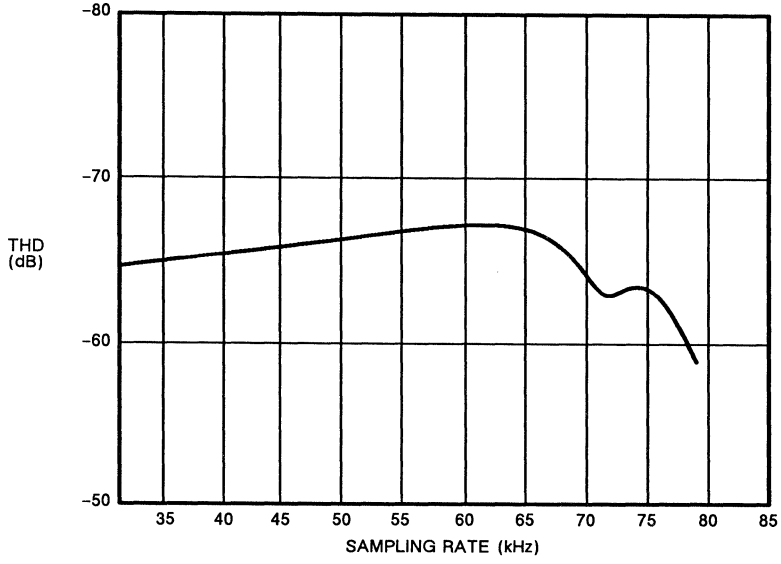


7

SAMPLING RATE vs. DISTORTION (A/D MODE)



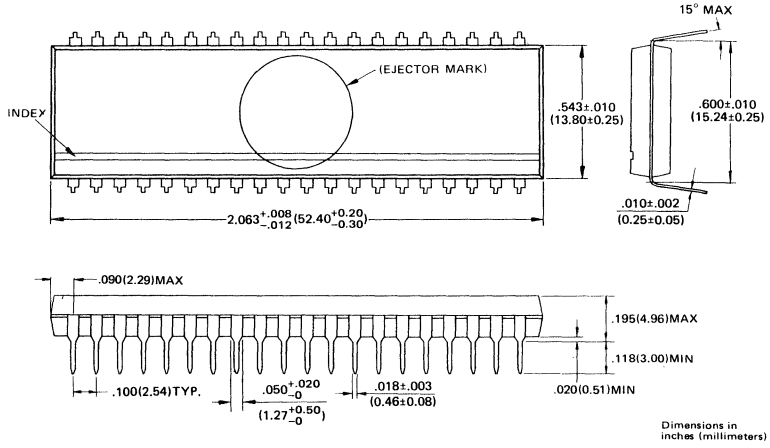
SAMPLING RATE vs. DISTORTION (D/A MODE)



BW = 13.8kHz, f_{signal} = 1kHz, level = FS -20dB)

7

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40P-M01)



Dimensions in inches (millimeters)

7

Section 8

Other Linear Products

Fujitsu Part No.	Description	Features	Equiv. Prod.	Power Supply (V)	Package	No. of Pins
MB412	Dual Differential Line Driver	Three-State Differential Output	—	+5	Plastic DIP	14
MB413	Quad Differential Line Receiver	Differential Inputs, Three-State Output	—	+5	Ceramic DIP	16
MB3501	Wide Band Video Amp	Adj Gain (10 to 400) GBW = 50, 150 MHz	µA733	+9.5 ~ +40	Plastic DIP Plastic Flatpak	14 14
MB3764	9-Level Indicator Driver	Wide Range of Ref. Voltages	—	+18V	Plastic DIP	16
MB4206	Frequency to Voltage Conv	Charge Pump Zener Clamped O/P	—	+12	SIP	8
MB4207	Frequency to Voltage Conv	Charge Pump Zener Clampled O/P	—	+12	SIP	8
MB43458	Quad PreAmplifier	Cascade Amplifier with Feedback		+12	Plastic Flatpak	14
MB43468	Quad Pre-amplifiers	Cascade Amplifier with Feedback	—	±8	Plastic Flatpak	14
MB47201	Quad SPST	J-FET R_{ON} = 100Ω, I_{LEAK} = 0.1nA	DG201	+15	Plastic DIP Plastic Flatpak	16 16

FUJITSU

MB412

DUAL DIFFERENTIAL LINE DRIVER WITH THREE-STATE OUTPUTS

<Outline>

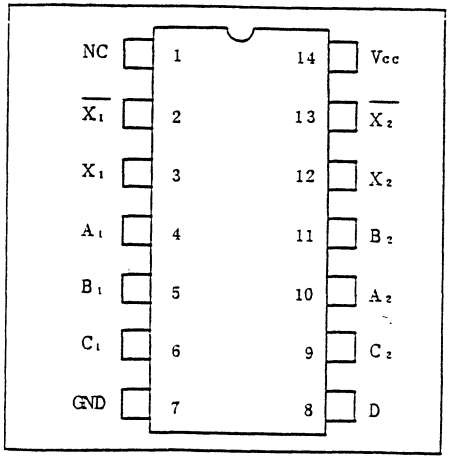
The Fujitsu MB412 is the balanced transmission driver with Schottky TTL technology and is designed to satisfy CCITT recommendation V11.

The three-state control brings output to high impedance state by giving low level to circuit-independent inhibit pin C or common inhibit pin D. Since input pin C has a pull-up resistor, it can be left open when not used.

<Features>

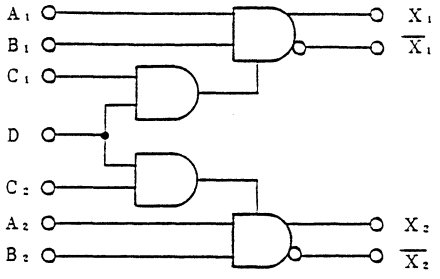
- o Differential output (Three states)
- o Independent and common inhibit pins
- o CCITT recommendation V11 is satisfied.
- o Schottky TTL
- o With input clamp diode
- o Low level output current: 40 mA
- o High level output current: 40 mA

PIN ASSIGNMENT (TOP VIEW)



8

BLOCK DIAGRAM



FUNCTION TABLE

Input				Output	
A	B	C	D	X	$\overline{X}$
H	H	H	H	H	L
H	L	H	H	L	H
L	H	H	H	L	H
L	L	H	H	L	H
※	※	L	※	HZ	HZ
※	※	※	L	HZ	HZ

[Note]
*: Irrelevant level
HZ: High impedance state

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+7.0	V
Input Voltage	V_I	+5.5	V
Output Voltage	V_O	+5.5	V
Operating Temperature	T_A	0～+70	℃
Storage Temperature	T_{stg}	−65～+150	℃

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+4.75～+5.25	V
Output Current	I_{OH}	−40	mA
	I_{OL}	40	mA
Operating Temperature	T_A	0～+70	℃

8

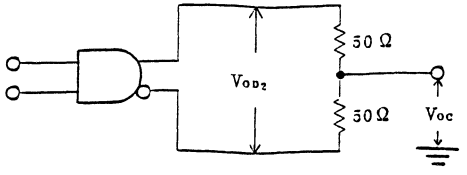
ELECTRICAL CHARACTERISTIC

1. DC Characteristics (T_A = 0°C - +70°C)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Low Level Output Voltage	V_{OL}	V_{CC} = 4.75 V, I_{OL} = 40 mA V_{IH} = 2 V, V_{IL} = 0.8 V	–	0.4	0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = 4.75 V, I_{OH} = −40 mA V_{IH} = 2 V, V_{IL} = 0.8 V	2.5	3.0	–	V
Output Clamp Voltage	V_{OK}	V_{CC} = 5.25 V, I_O = −40 mA	–	–	−1.5	V
Differential Output Voltage	V_{OD1}	V_{CC} = 5.25 V, I_O = 0 mA	–	3.8	$2V_{OD2}$	V
Comolementary Output Terminal Voltage	V_{OD2}	V_{CC} = 4.75 V	2	2.5	–	V
	$\triangle \lvert V_{OD} \rvert$	V_{CC} = 4.75 V	–	0.03	0.4	
Complementary Output Terminal Middle Point Voltage	V_{OC}	V_{CC} = 5.25 V	–	–	3	V
		V_{CC} = 4.75 V	–	–	3	
	$\triangle \lvert V_{OC} \rvert$	V_{CC} = 5.25 V	–	–	0.4	
		V_{CC} = 4.75 V	–	–	0.4	
Output Leakage Current (Power Off)	I_O	V_{CC} = 0 V, V_O = 6 V	–	–	100	μA
		V_{CC} = 0 V, V_O = −0.25 V	–	–	−100	
		V_{CC} = 0 V, −0.25 V ≦ V_O ≦ 6 V	–	–	±100	
Output Leakage Current (High Impedance)	I_{OZ}	V_{CC} = 5.25 V, 0 V ≦ V_O ≦ 5.25 V, T_A = 25°C	–	–	±10	μA
		V_{CC} = 5.25 V, V_O = 0 V, T_A = 70°C	–	–	−20	
		V_{CC} = 5.25 V, V_O = 0.4 V, T_A = 70°C	–	–	±20	
		V_{CC} = 5.25 V, V_O = 2.4 V, T_A = 70°C	–	–	±20	
		V_{CC} = 5.25 V, V_O = 5.25 V, T_A = 70°C	–	–	20	
Input Current — Input A, B, C	I_I	V_{CC} = 5.25 V, V_I = 5.5 V	–	–	1	mA
Input Current — Input D			–	–	2	
Input Current — Input A, B, C	I_{IH}	V_{CC} = 5.25 V, V_I = 2.4 V	–	–	40	μA
Input Current — Input D			–	–	−300	
Input Current — Input A, B, C	I_{IL}	V_{CC} = 5.25 V, V_I = 0.4 V	–	–	−1.6	mA
Input Current — Input D			–	–	−1.8	
Input Clamp Voltage	V_{IK}	V_{CC} = 4.75 V, I_I = −12 mA	–	–	−1.5	V
Output Short Current	I_{OS}	V_{CC} = 5.25 V	−40	–	−150	mA
Power Current (All Input, GND)	I_{CC}	V_{CC} = 5.25 V, T_A = 25°C	–,	31	65	mA

[Note]

1. V_{OD1}: Potential difference between complementary output X and $\overline{X}$
2. $\triangle \lvert V_{OD} \rvert$: V_{OD2} difference when X is set to high and $\overline{X}$ is set to low.
   $\triangle \lvert V_{OC} \rvert$: V_{OC} difference when X is set to high and $\overline{X}$ is set to low.

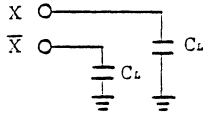


3. Standard value is obtained when V_{CC} = +5.0 V and T_A = 25°C.

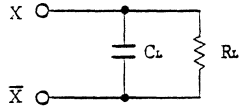
2. Switching Characteristics (V_{CC} = +5.0 V, T_A = 25°C)

Parameter	Symbol	Conditions	Measurement Circuit	Value			Unit
				Min.	Typ.	Max.	
Delay Time	t_{PLH}	C_L = 15 pF, [Note 1]	Fig. 1	–	13.0	20	ns
	t_{PHL}			–	10.2	15	
Delay Time	t_{PLH}	C_L = 30 pF R_L = 100 Ω [Note 2]	Fig. 1	–	13.6	25	ns
	t_{PHL}			–	10.5	20	
Output Rise Time	t_{TLH}			–	10	20	
Output Fall Time	t_{THL}			–	7.1	20	
Output Enable Time	t_{PZH}	C_L = 30 pF, R_L = 180 Ω	Fig. 2	–	7.5	20	ns
	t_{PZL}	C_L = 30 pF, R_L = 250 Ω	Fig. 3	–	18	40	
Output Disable Time	t_{PHZ}	C_L = 30 pF, R_L = 180 Ω	Fig. 2	–	7.4	30	
	t_{PLZ}	C_L = 30 pF, R_L = 250 Ω	Fig. 3	–	8.9	35	
Overshoot Rate		R_L = 100 Ω, [Note 3]	Fig. 1	–	–	10	%

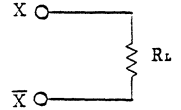
[Note 1]



[Note 2]



[Note 3]



C_L: Including probe and measurement jig capacity

3. Switching Characteristic Measurement Circuit and Switching Waveform

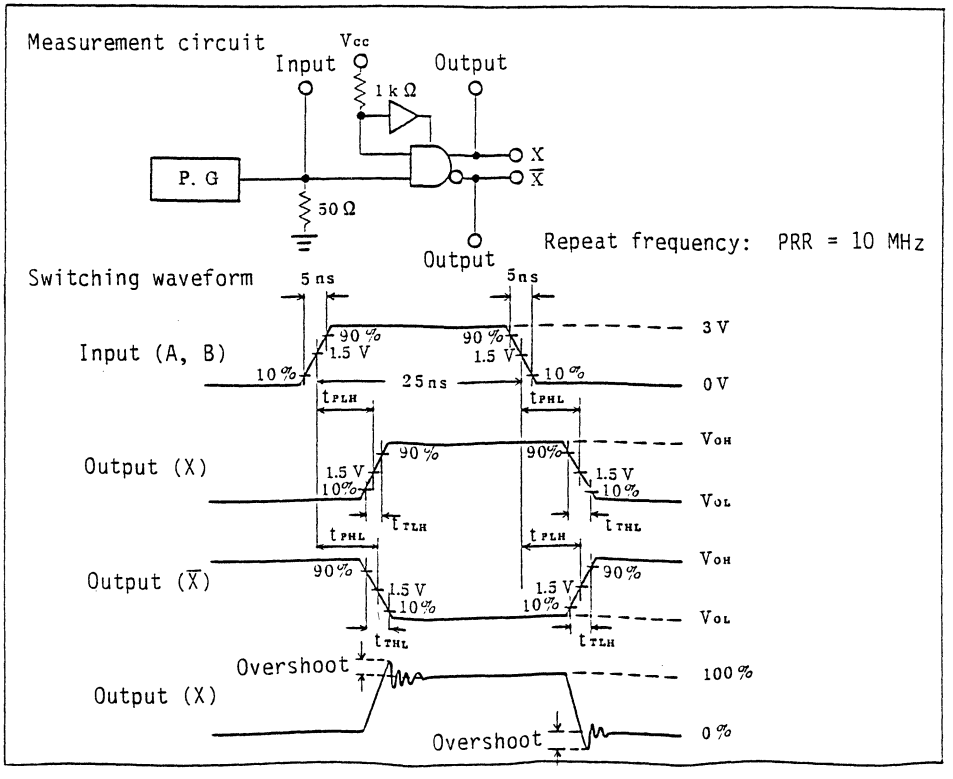


Fig. 1

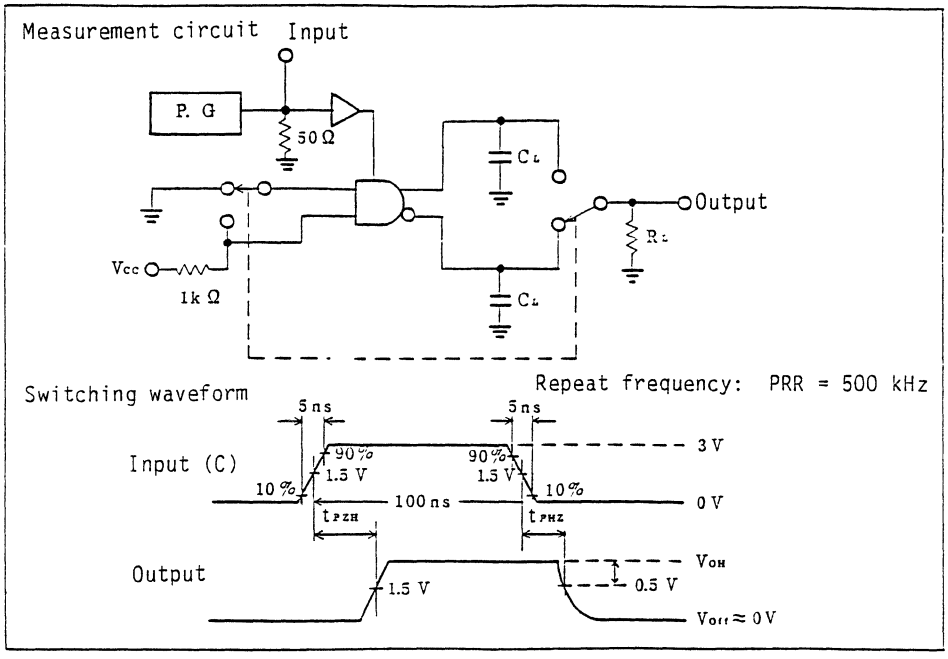

Measurement circuit
Input
P. G
50Ω
CL
Output
RL
Vcc
1kΩ
CL
Switching waveform
Repeat frequency: PRR = 500 kHz
5ns
5ns
Input (C)
90%
1.5 V
90%
1.5 V
3 V
10%
10%
0 V
100ns
tPZH
tPHZ
Output
VOH
1.5 V
0.5 V
VOFF ≈ 0 V

Fig. 2

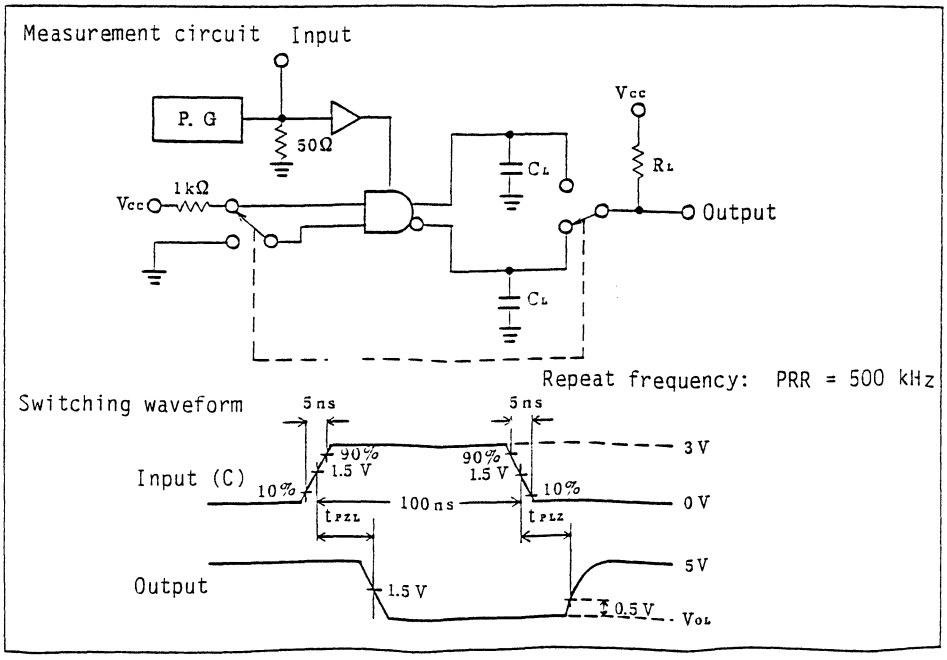
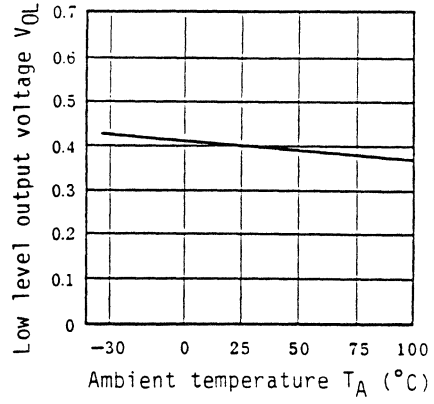

Measurement circuit
Input
P. G
50Ω
Vcc
RL
1kΩ
Vcc
CL
Output
CL
Repeat frequency: PRR = 500 kHz
Switching waveform
5ns
5ns
Input (C)
90%
1.5 V
90%
1.5 V
3 V
10%
10%
0 V
100ns
tPZL
tPLZ
5V
Output
1.5 V
0.5 V
VOL

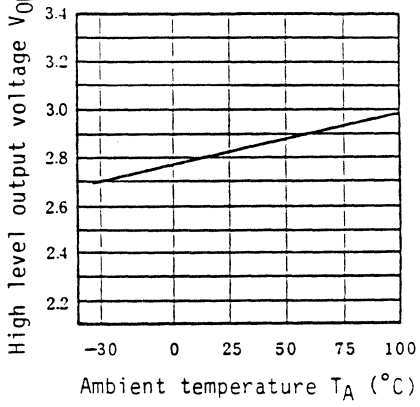
Fig. 3

TYPICAL CHARACTERISTIC CURVE

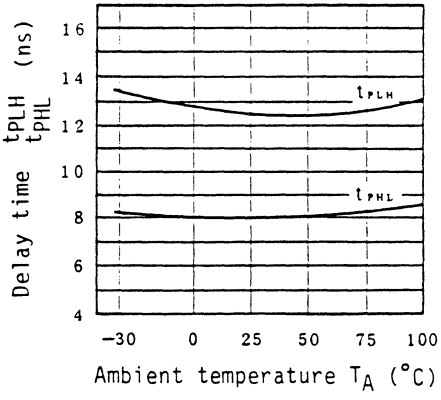
Low level output voltage
- Ambient temperature



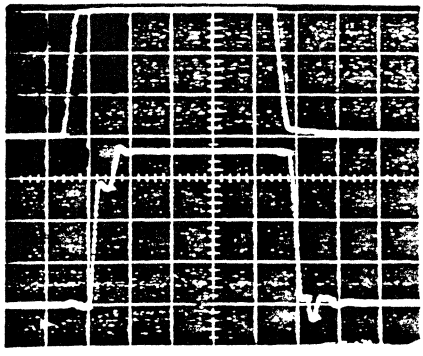
High level output voltage
- Ambient temperature



Delay time - Ambient temperature



Switching waveform
Input A - Output X



H: 20ns/DIV
V: 1V/DIV

8

14-LEAD CERAMIC PACKAGE (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-14C-C02

NOT RELEASED

MB413

QUAD DIFFERENTIAL LINE RECEIVER WITH THREE-STATE OUTPUTS

<Outline>

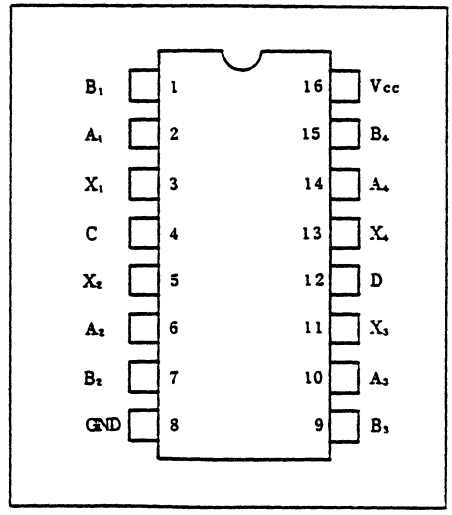
The Fujitsu MB413 is the balanced transmission receiver with Schottky TTL technology and is designed to satisfy CCITT recommendation V11.

Since input pin A has a pull-up resistor and input pin B has a pull-down resistor, output is set to high level when input A and input B are open.

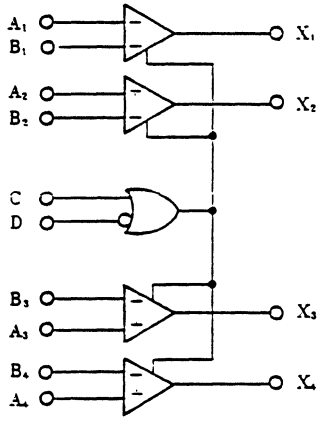
<Features>

- o Differential input
- o Input sensitivity: 300 mV
- o CCITT recommendation is satisfied
- o Output is high level when differential input is open
- o Low power Schottky TTL
- o Three-state outputs

PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



FUNCTION TABLE

Input			Output
C	D	V_{DIFF}	X
H	*	+	H
*	L	+	H
H	*	−	L
*	L	−	L
L	H	*	Hz

[Note]
V_{DIFF} = V_{IA} - V_{IB}
*: Irrelevant level
HZ: High impedance state

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Voltage	V_{CC}	+7	V
In-Phase Input Voltage*	V_{CM}	−25 ~ +25	V
Differential Input Voltage*	$\|V_{DIFF}\|$	0 ~ +25	V
Input Voltage C, D	V_I	+7	V
Output Current	I_O	+50	mA
Operating Temperature	T_A	−25 ~ +125	℃
Storage Temperature	T_{stg}	−65 ~ +165	℃

[Note]
1. Applied voltage (*) should not exceed ±25 V for GND pin.
2. $V_{CM} = \frac{1}{2}(V_{IA} + V_{IB})$,
$|V_{DIFF}| = |V_{IA} - V_{IB}|$

.RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Voltage	V_{CC}	+4.75 ~ +5.25	V
In-phase Input Voltage	V_{CM}	−7 ~ +7	V
Differential Input Voltage	$\|V_{DIFF}\|$	+0.3 ~ +6	V
Operating Temperature	T_A	0 ~ +70	℃

[Note]
2. $V_{CM} = \frac{1}{2}(V_{IA} + V_{IB})$,
$|V_{DIFF}| = |V_{IA} - V_{IB}|$

8

ELECTRICAL CHARACTERISTIC

1. DC Characteristics (T_A = 0°C - +70°C)

Parameter	Symbol	Conditions		Value Min.	Value Typ.	Value Max.	Unit
Threshold Voltage	V_{TH}	V_{CC} = 5.0V ± 5%	$V_{OH} \geqq$ 2.7V, I_{OH} = −440 μA	−	−	0.3	V
Differential Input	V_{TL}	−7V ≦ V_{CM} ≦ 7V	$V_{OL} \leqq$ 0.4V, I_{OL} = 4mA	−0.3	−	−	V
High Level Output Voltage	V_{OH}	V_{CC} = 4.75V, I_{OH} = −440 μA, V_{DIFF} = 0.3 ~ 6V, V_{IC} = 2.0V, V_{ID} = 0.8V		2.7	−	−	V
Low Level Output Voltage	V_{OL}	V_{CC} = 4.75V, V_{DIFF} = −0.3 ~ −6V, V_{IC} = 2.0V, V_{ID} = 0.8V	I_{OL} = 4mA	−	−	0.4	V
			I_{OL} = 8mA	−	−	0.45	
Input Current (Input A, B)	I_I	V_{CC} = 5.25V or V_{CC} = 0V	V_I = 10V	−	−	2.2	mA
			V_I = 3V	0	−	1.0	
			V_I = −3V	−1.0	−	0	
			V_I = −10V	−2.2	−	−	
Input Clamp Voltage (Input C, D)	V_{IK}	V_{CC} = 4.75V, I_I = −18mA		−	−	−1.5	V
Input Current (Input C, D)	I_{IL}	V_{CC} = 5.25V, V_I = 0.4V		−	−	−0.36	mA
Input Current (Input C, D)	I_{IH}	V_{CC} = 5.25V	V_I = 2.7V	−	−	20	μA
			V_I = 5.5V	−	−	100	
Output Leakage Current (High Impedance)	I_{OZ}	V_{CC} = 5.25V, V_{IC} = 0.8V, V_{ID} = 2.0V	V_O = 2.4V	−	−	20	μA
			V_O = 0.4V	−	−	−20	
Output Short Current	I_{OS}	V_{CC} = 5.25V, V_O = 0V		−15	−	−85	mA
Power Current	I_{CC}	V_{CC} = 5.25V, V_I = 0V		−	−	70	mA

[Note]

$V_{CM} = \frac{1}{2}(V_{IA} + V_{IB})$,

$V_{DIFF} = V_{IA} - V_{IB}$

2. Switching Characteristics (V_{CC} = +5.0 V, T_A = 25°C)

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Delay Time	t_{PLH}	C_L = 15 pF, V_{TD} = GND	S_1 : Close, S_2 : Close	–	–	25	ns
	t_{PHL}			–	–	25	
Output Disable Time	t_{PLZ}	C_L = 5 pF	S_1 : Close, S_2 : Close	–	–	30	ns
	t_{PHZ}		S_1 : Close, S_2 : Close	–	–	22	
Output Enable Time	t_{PZL}	C_L = 15 pF	S_1 : Close, S_2 : Open	–	–	22	ns
	t_{PZH}		S_1 : Open, S_2 : Close	–	–	22	

3. Switching Characteristic Measurement Circuit and Switching Waveform

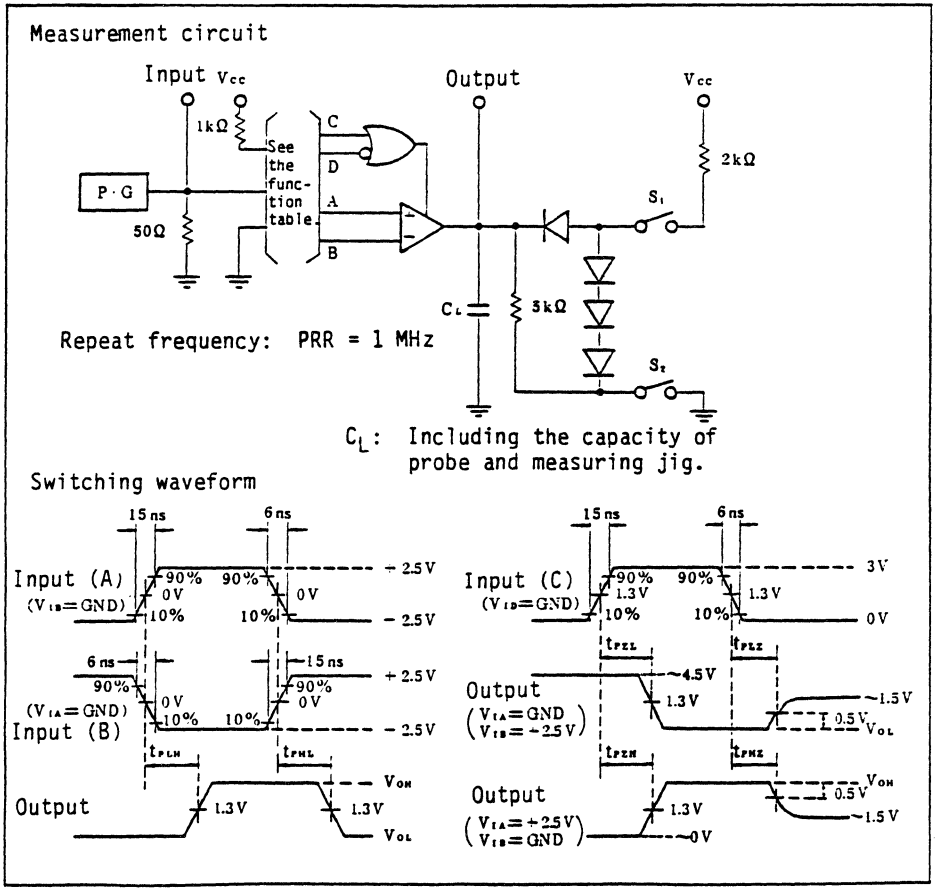
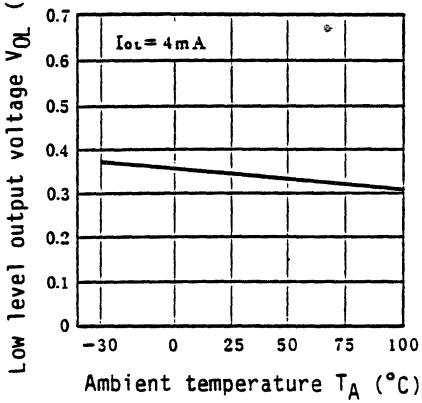


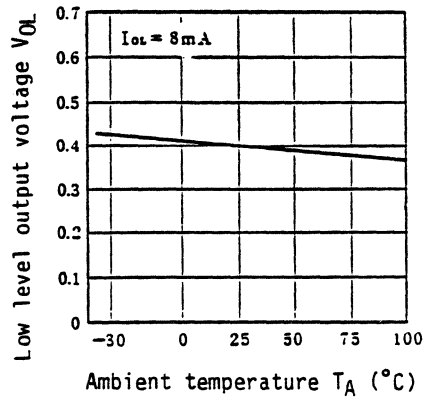
Fig. 1

TYPICAL CHARACTERISTIC CURVE

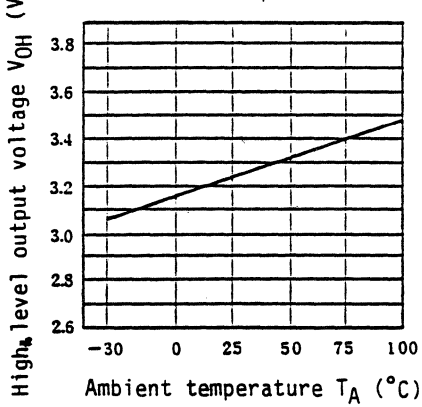
Low level output voltage
- Ambient temperature



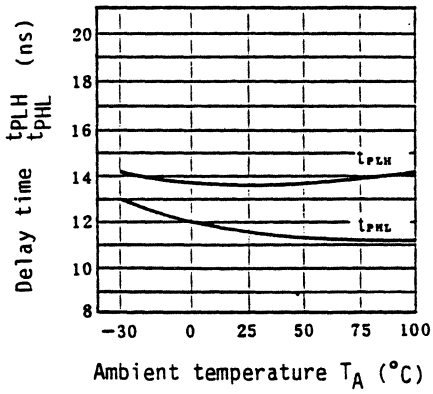
Low level output voltage
- Ambient temperature



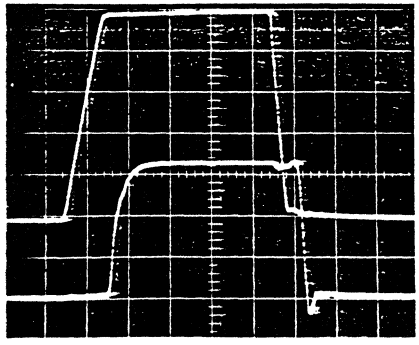
High level output voltage
- Ambient temperature



Delay time - Ambient temperature



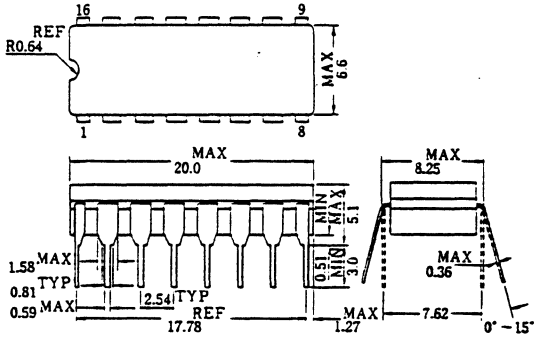
Switching waveform
Input A - Output X



H: 20ns/DIV
V: 1V/DIV

8

DIP-16C-C05



Dimensions in millimeters

8

FUJITSU

WIDE BAND VIDEO AMPLIFIER

MB3501

July 1988
Edition 2.0

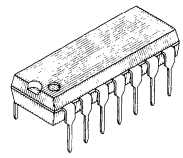
WIDE BAND VIDEO AMPLIFIER

The MB3501 is a monolithic differential input, differential output, wideband video amplifier. Owing to adoption of feedback circuitry, wide bandwidth and gain stability are achieved. Adjustable gain from 10 to 400 are obtained by external resistor without external frequency compensation.

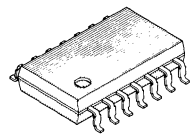
The MB3501 is most suitable for sense-amplifier of magnetic memory equipment, video amplifier and pulse amplifier.

The MB3501 is compatible with μA733.

- Supply Voltage: ±6V
- Wide Bandwidth: 150MHz
- Selectable Gain: 10 to 400
- Frequency Compensation is not required.
- 14-pin DIP Package (Suffix: -P)
  14-pin Flat Package (Suffix: -PF)

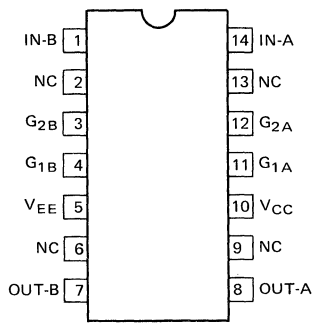


PLASTIC PACKAGE
DIP-14P-M02



PLASTIC PACKAGE
FPT-14P-M01

PIN ASSIGNMENT



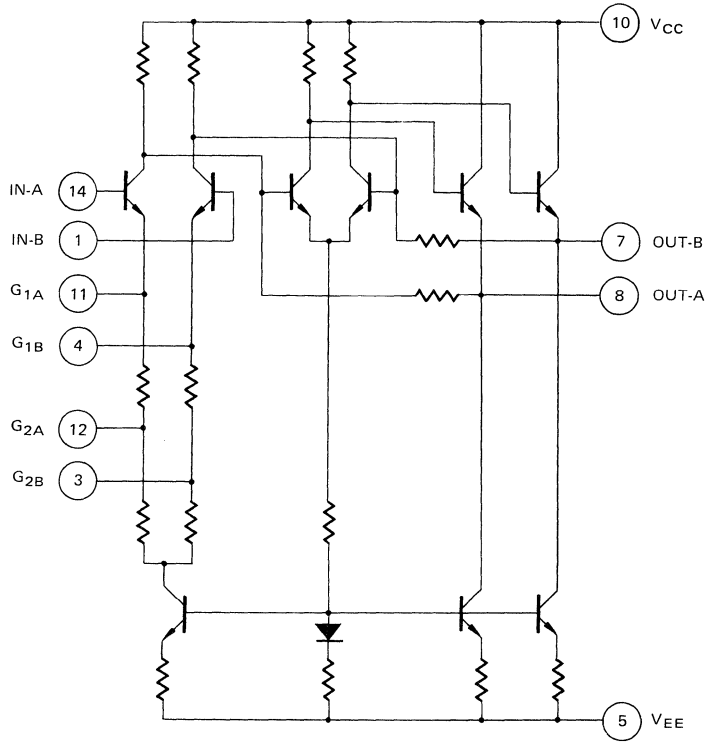
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+8	V
Negative Supply Voltage	V_{EE}	−8	V
Input Voltage	V_{IN}	+1.5 to −5	V
Output Current	I_O	10	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB3501 EQUIVALENT CIRCUIT



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+6±5%	V
Negative Supply Voltage	V_{EE}	–6±5%	V
Operating Temperature	T_A	–20 to +75	°C

DC CHARACTERISTICS

(V_{CC} = 6V, V_{EE} = -6V, T_A = 25°C)

Parameter	Symbol	Condition	Test Circuit	Value			Unit
				Min	Typ	Max	
Output Low Voltage	V_{OL}	ΔV_I = 200mV	Figs 2, 3		0.4	1.0	V
Output High Voltage	V_{OH}	ΔV_I = 200mV	Figs 2, 3	4.8	5.2		V
Output Voltage	V_O	*1	Fig. 4	1.6	2.7	3.9	V
Output Offset Voltage	V_{OFF}	*1	Fig. 4		0.35	1.4	V
Input Offset Current	I_{IO}		Fig. 4		0.4		μA
Input Bias Current	I_I		Fig. 4		9	30	μA
Output Sink Current	I_{SINK}	ΔV_I = 200mV			3.6		mA
Supply Current	I_{CC}	*1	Fig. 4		17	27	mA

AC CHARACTERISTICS

(V_{CC} = 6V, V_{EE} = -6V, T_A = 25°C)

Parameter	Symbol	Condition	Test Circuit	Value			Unit
				Min	Typ	Max	
Voltage Gain	AV_1	f = 1kHz, R_L = 1kΩ*2	Fig. 5	250	400	600	
	AV_2	f = 1kHz, R_L = 1kΩ*3	Fig. 5	80	100	120	
	AV_3	f = 1kHz, R_L = 1kΩ*4	Fig. 5	9	11	14	
Frequency Bandwidth	BW_1	R_S = 50Ω, R_L = 1kΩ*2	Fig. 6		50		MHz
	BW_2	R_S = 50Ω, R_L = 1kΩ*3	Fig. 6	80	110		MHz
	BW_3	R_S = 50Ω, R_L = 1kΩ*4	Fig. 6		150		MHz
Recovery Time	t_{REC}	R_S = 50Ω, R_L = 1kΩ, ΔV_I = 100mV			20		ns
Common Mode Gain	CMG	f ≤ 100kHz*3			-60		dB

Notes: *1 Inputs pins ground.
*2 Pins 4 and 11 connected together.
*3 Pins 3 and 12 connected together.
*4 Gain select pins open.

8

TEST CIRCUIT

Fig. 2 – V_{OL}, V_{OH}

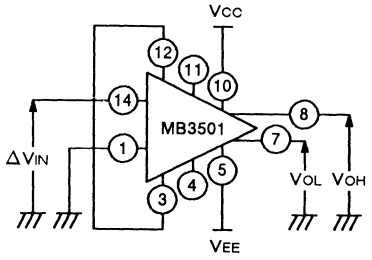


Fig. 3 – V_{OL}, V_{OH}

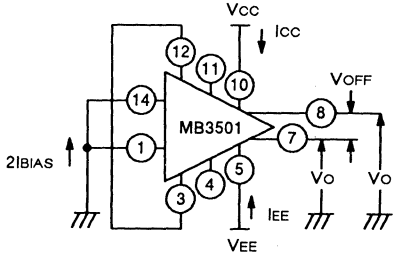


Fig. 4 – V_O, V_{OFF}, I_I

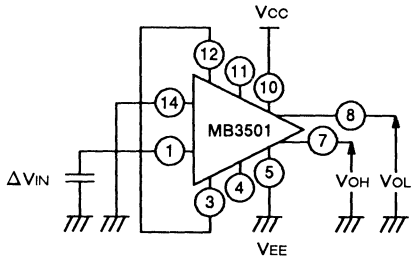
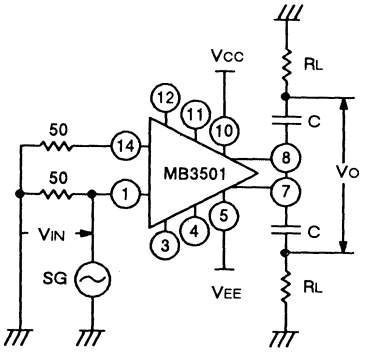
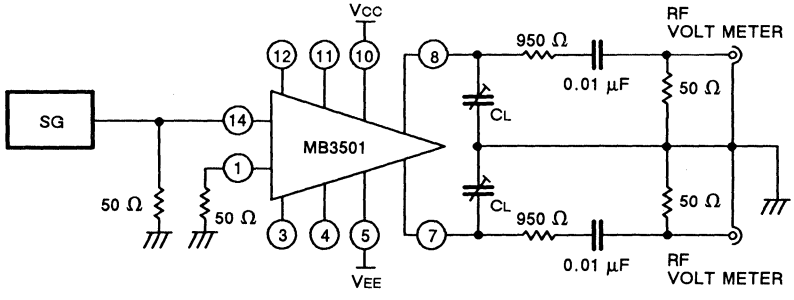


Fig. 5 – AV



AV = VO/VIN
1/ωC < RL

Fig. 6 – BW



8

TYPICAL CHARACTERISTICS CURVES

Fig. 7 – SINGLE VOLTAGE GAIN vs. FREQUENCY

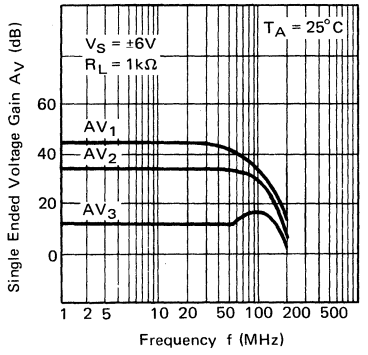


Fig. 8 – SINGLE ENDED VOLTAGE GAIN vs. FREQUENCY

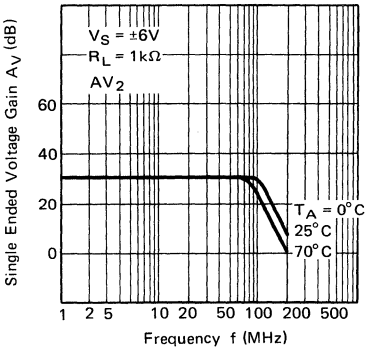


Fig. 9 – SINGLE ENDED VOLTAGE GAIN vs. FREQUENCY

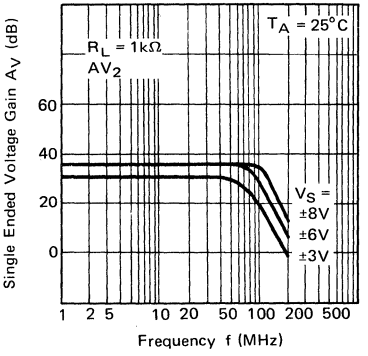


Fig. 10 – PHASE SHIFT vs. FREQUENCY

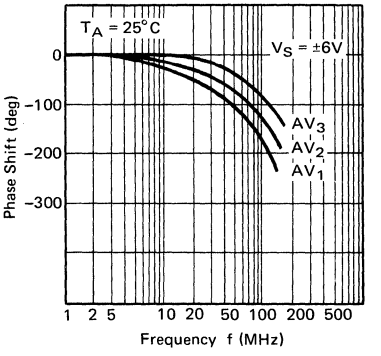


Fig. 11 – RECOVERY TIME vs. DIFFERENTIAL INPUT VOLTAGE

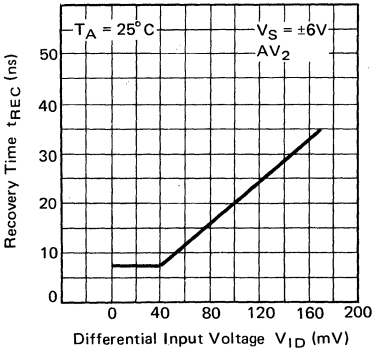
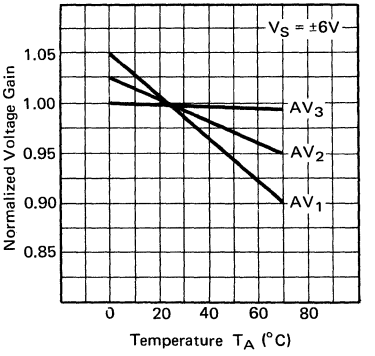


Fig. 12 – NORMALIZED VOLTAGE GAIN vs. TEMPERATURE



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TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 13 – NORMALIZED VOLTAGE GAIN vs. SUPPLY VOLTAGE

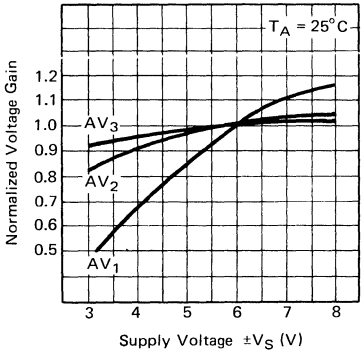


Fig. 14 – COMMON MODE GAIN vs. FREQUENCY

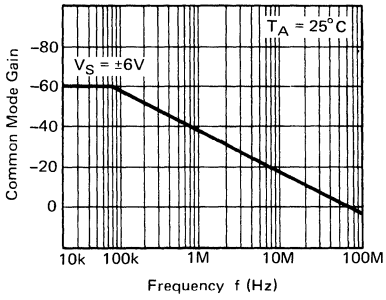
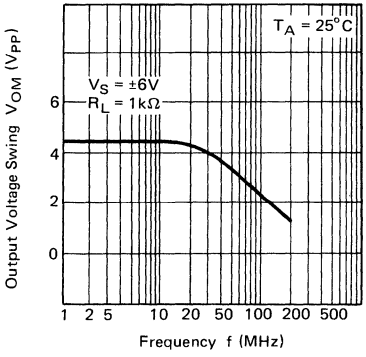


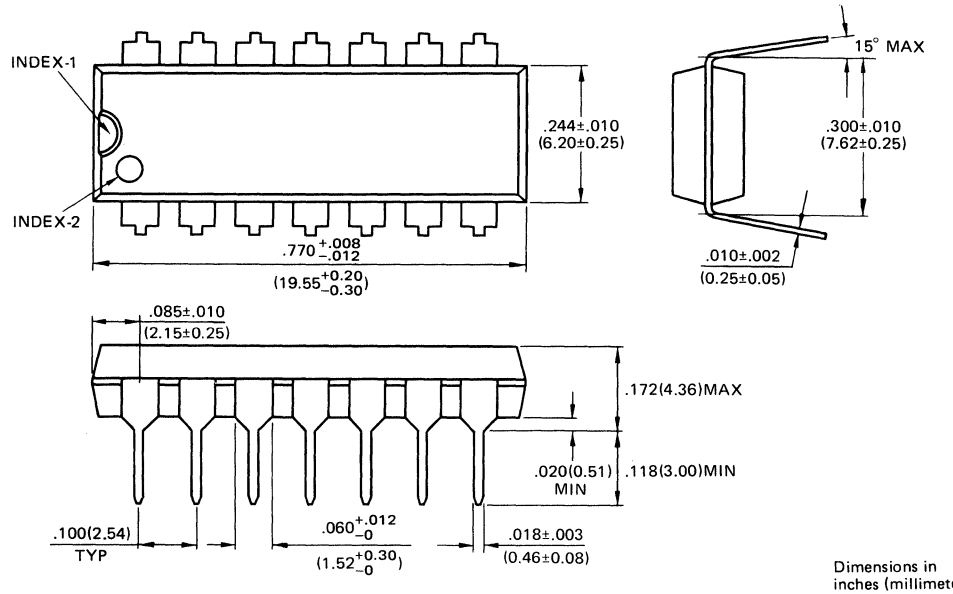
Fig. 15 – OUTPUT VOLTAGE SWING vs. FREQUENCY



8

PACKAGE DIMENSIONS

14-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)

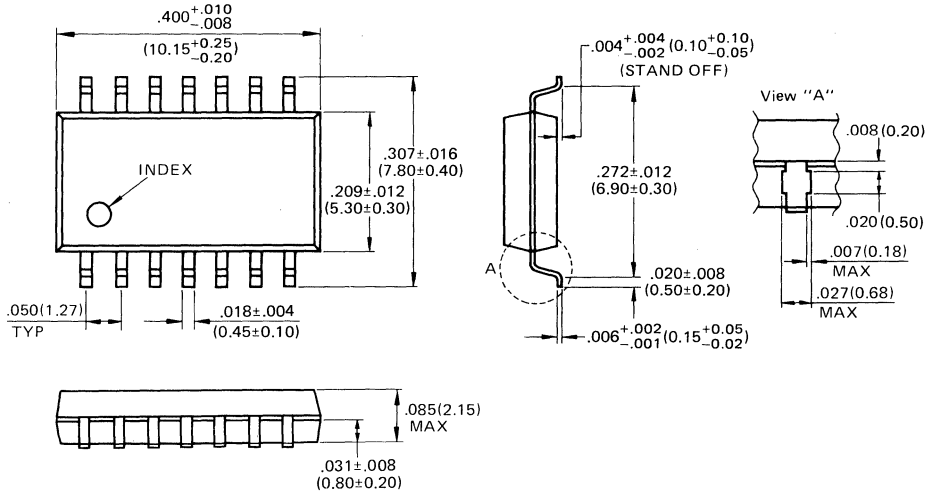


Dimensions in
inches (millimeters)

8

PACKAGE DIMENSIONS (continued)

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



Dimensions in
inches (millimeters)

8

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Printed in Japan PV0079-887A2

FUJITSU

NINE-LEVEL DETECTOR AND DRIVER FOR LEVEL METER

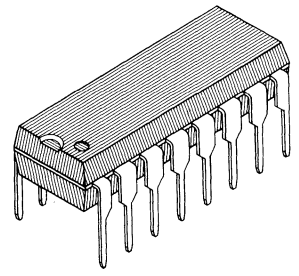
MB3764

September 1987
Edition 1.0

NINE-LEVEL DETECTOR AND DRIVER FOR LEVEL METER

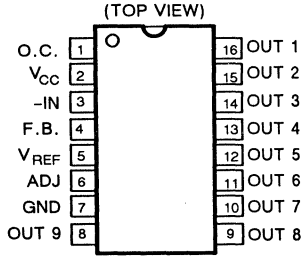
The Fujitsu MB3764 is a nine-level detector and driver for level meters. The MB3764 contains an internal reference voltage generator and an operational amplifier with offset, so it recognizes the extended analog voltage level range, including negative voltage.

- Nine output levels
- Wide range of preset reference voltages: 1.25 V to 13 V
- Reverse phase input operational amplifier with an offset of half a reference voltage.
- High output current: 20 mA max.
- Output enabling. (Output enable time T_{ON} = 120 ns max)



PLASTIC PACKAGE
DIP-16P-M04

PIN ASSIGNMENT



Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

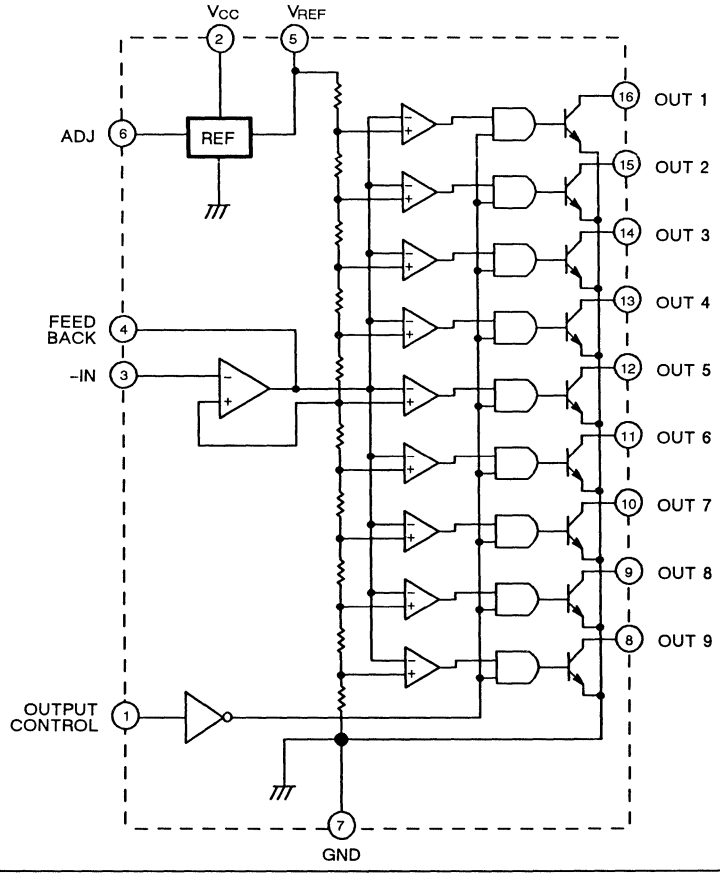
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}	—	18	V
Output Voltage	V_{OH}	—	18	V
Amp Input Voltage	V_{IN}	—	-0.3 to V_{CC}	V
Control Input Voltage	V_{OC}	—	-0.3 to 7.0	V
Power Dissipation	P_D	$T_A \leq 75°C$	710	mW
Storage Temperature	T_{STG}	—	-55 to 125	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8

Figure 1. MB3764 Block Diagram



8

RECOMMENDED OPERATING CONDITIONS

Parameter	Designator	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	3.2	—	16	V
Output Current	I_{OUT}	—	10	20	mA
Feed Back Sink Current	I_{SINK}	—	—	0.5	mA
Feed Back Source Current	I_{SOURCE}	—	—	2	mA
Feed Back Voltage	V_{FB}	—	—	13	V
Reference Voltage Output Current	I_{REF}	0	—	5	mA
Reference Voltage	V_{REF}	1.2	—	13	V
Operating Ambient Temperature	T_A	-20	25	75	°C

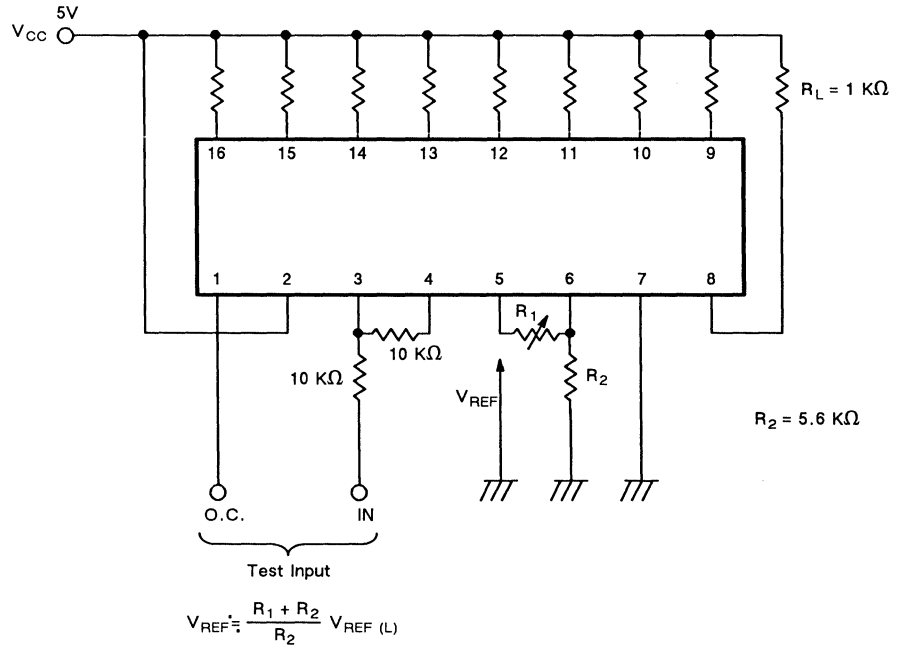
ELECTRICAL CHARACTERISTICS (V_{CC}= 5V, T_A = 25°C, V_{REF} = 2.5V)

Parameter		Designator	Conditions	Values			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	R1=0, R2=∞	—	9	14	mA
Reference Voltage Generator Section	Output Voltage	V_{REFL}	R1=0	1.20	1.25	1.30	V
	Input Voltage Stability	ΔV_{RIN}	4.5 V ≤ V_{CC} ≤ 16 V	—	2	30	mV
	Load Voltage Stability	ΔV_{RLD}	0 ≤ I_{REF} ≤ 5 mA	—	2	30	mV
	Temperature Stability	ΔV_R	-20°C ≤ T_A ≤ 75°C	—	6	40	mV
	Short-circuit Current	I_{SC}	—	—	15	—	mA
Comparator Section	Quantumization Distortion	ϵ	—	—	±0.5	±2	%
	Center Voltage Deviation	V_M	3 and 4 Pins are connected.	1.20	1.25	1.30	V
Error Amplifier Section	Input Bias Current	I_{IB}	V3 = 0	-250	-30	—	nA
	Voltage Gain	A_V	0.5 V ≤ V_O ≤ 2.5 V	60	80	—	dB
	Band Width	BW		—	1	8	MHz
	Slew Rate	SR		—	0.5	—	V/μs
	High Level Output Voltage	V_{OH}	I_{SOURCE} = 2 mA	2.8	3.3	—	V
	Low Level Output Voltage	V_{OL}	I_{SINK} = 0.5 mA	—	0.1	0.3	V
Output Section	Output Saturation Voltage	V_{SAT1}	I_{OUT} = 10 mA	—	0.1	0.4	V
		V_{SAT2}	I_{OUT} = 20 mA	—	0.15	1.0	V
	Output Leakage Current	I_{OH}	V_O = 16V	—	—	10	μA
Control Section	High Level Input Current	I_{IH}	V_{OC} = 5V	—	50	300	μA
	Low Level Input Current	I_{IL}	V_{OC} = 0	-1.0	-0.6	—	mA
	High Level Input Voltage	V_{IH}	-20°C ≤ T_A ≤ 75°C	2.0	—	—	V
	Low Level Input Voltage	V_{IL}	-20°C ≤ T_A ≤ 75°C	—	—	0.8	V
	Delay Time	T_{ON}	R_L = 200Ω	—	40	120	ns
		T_{OFF}	R_L = 200Ω	—	60	—	ns

* $\epsilon = \frac{|\text{Each Threshold Error Voltage}|\ \text{Max}}{|\text{Full Scale Voltage}|}$

8

Figure 2. Measurement Circuit



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Power Supply Current vs Power Supply Voltage

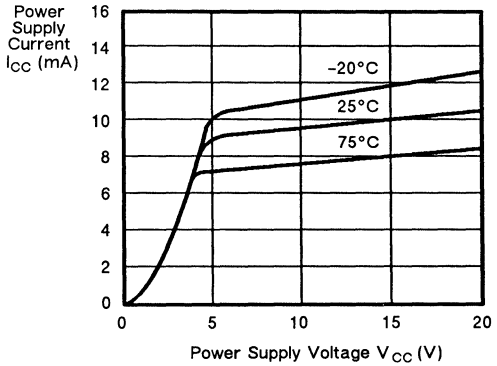
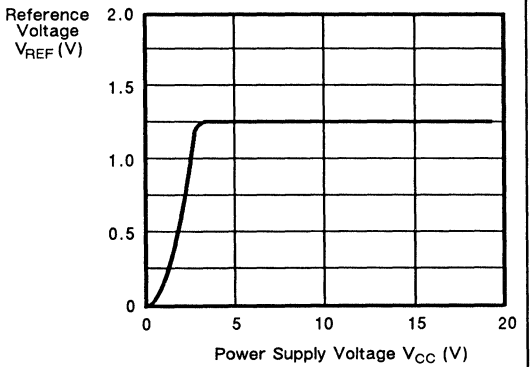


Fig. 4 – Reference Voltage vs Power Supply Voltage



8

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 5 – Reference Voltage Stability vs Ambient Temperature

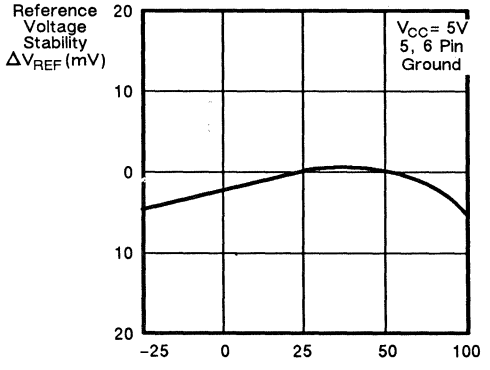


Fig. 6 – Output Voltage vs Op-Amp Output Current

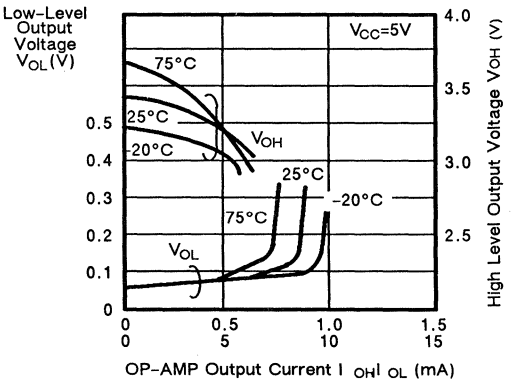


Fig. 7 – Output Saturation Voltage vs Output Current

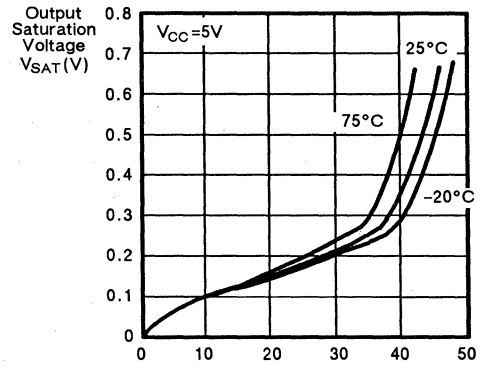
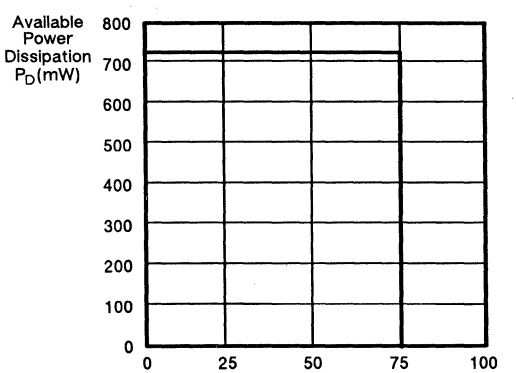


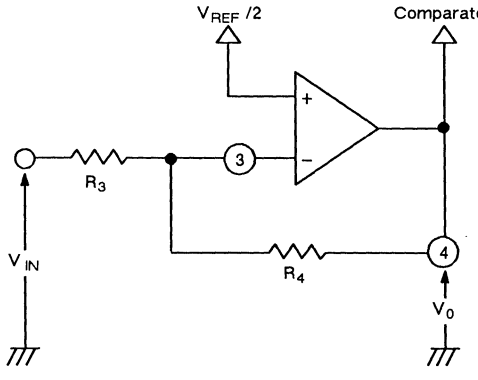
Fig. 8 – Available Power Dissipation vs Ambient Temperature

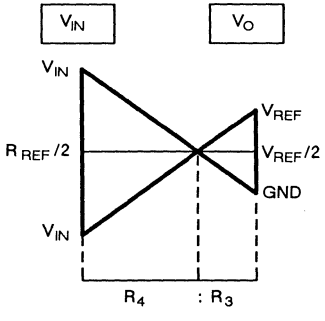


8

APPLICATION EXAMPLES

Figure 9. Voltage Recognition: V_{REF} /2





$$V_{IN} = \frac{V_{REF}}{2} - \frac{R_3}{R_4}\left(V_O - \frac{V_{REF}}{2}\right)$$

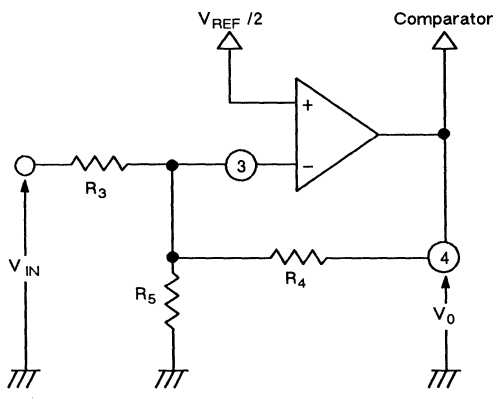
$$V_{IN} = \left(1 + \frac{R_3}{R_4}\right)\frac{V_{REF}}{2}$$

$$V_{IN} = \left(1 - \frac{R_3}{R_4}\right)\frac{V_{REF}}{2}$$

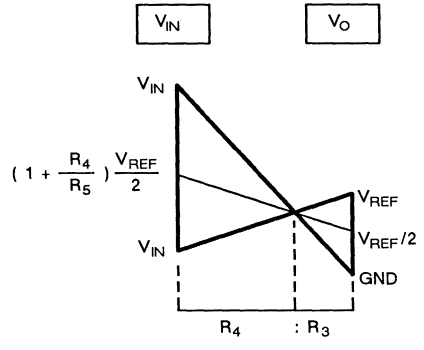
8

APPLICATION EXAMPLES (Continued)

Figure 10. Voltage Recognition: Above V_{REF} /2



$$V_{IN} = \frac{V_{REF}}{2} - \frac{R_3}{R_4}\left(V_O - \left(1 + \frac{R_4}{R_5}\right)\frac{V_{REF}}{2}\right)$$



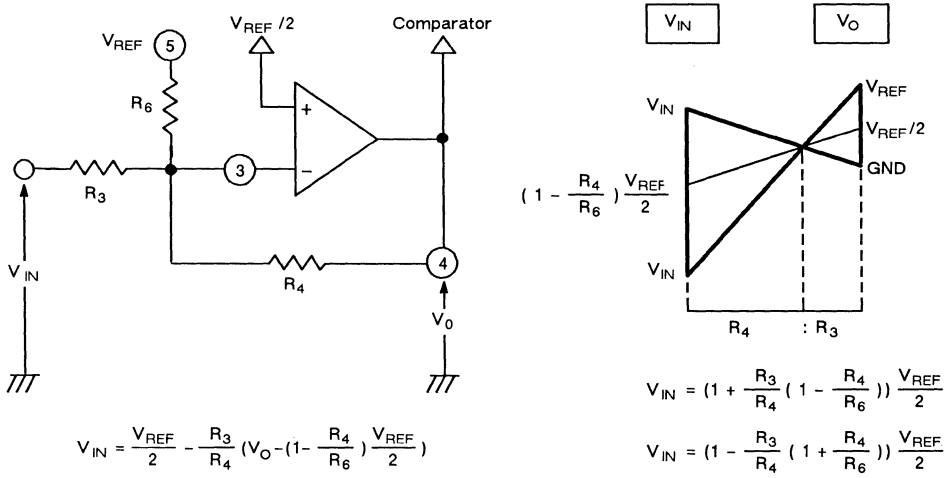
$$V_{IN} = \left(1 + \frac{R_3}{R_4}\left(1 + \frac{R_4}{R_5}\right)\right)\frac{V_{REF}}{2}$$

$$V_{IN} = \left(1 - \frac{R_3}{R_4}\left(1 - \frac{R_4}{R_5}\right)\right)\frac{V_{REF}}{2}$$

8

APPLICATION EXAMPLES (Continued)

Figure 11. Voltage Recognition: Below V_{REF} /2



$$V_{IN} = \frac{V_{REF}}{2} - \frac{R_3}{R_4}\left(V_O - \left(1 - \frac{R_4}{R_6}\right)\frac{V_{REF}}{2}\right)$$

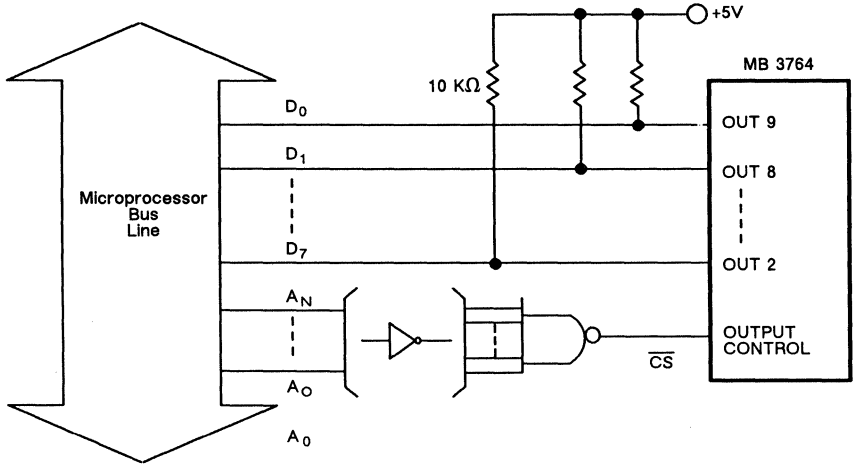
$$V_{IN} = \left(1 + \frac{R_3}{R_4}\left(1 - \frac{R_4}{R_6}\right)\right)\frac{V_{REF}}{2}$$

$$V_{IN} = \left(1 - \frac{R_3}{R_4}\left(1 + \frac{R_4}{R_6}\right)\right)\frac{V_{REF}}{2}$$

8

APPLICATION EXAMPLES (Continued)

Figure 12. Connection with Microprocessor Bus

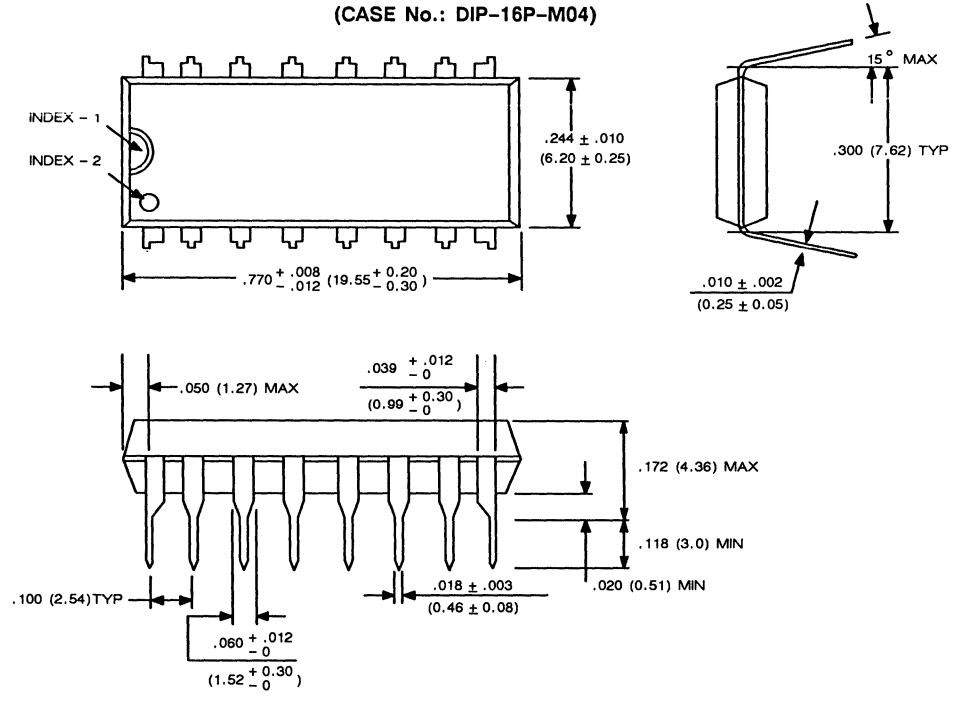


$\overline{CS}$: Chip Select (MB3764 Chip Select Pin, Selected at $\overline{CS}$ = 0)

8

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

D16033S-2C

FUJITSU

FREQUENCY-TO- VOLTAGE CONVERTER

MB4206

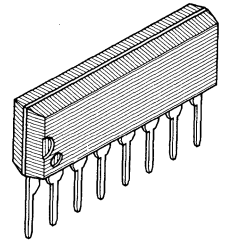
September 1987
Edition 1.0

FREQUENCY-TO-VOLTAGE CONVERTER

The Fujitsu MB4206 is a frequency-to-voltage converter with an on-chip comparator. The MB4206 uses a charge pump driven by a positive-edge Schmitt trigger/flip-flop input so stable operation is achieved against noise signal input. The output of the comparator is zener-clamped to a reference voltage; thus, a precise hysteresis output is obtained. The overall design makes the circuit fairly tolerant of imperfections in the input waveform.

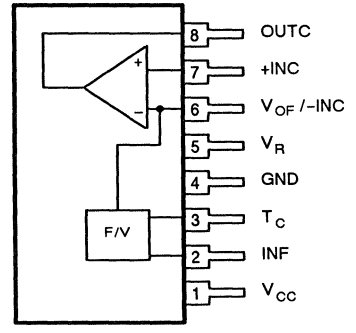
The MB4206 is housed in an 8-pin single inline package (SIP).

- Conversion coefficient determined by RC pair:
  $V_{OF} = F_{IN} \cdot R_T \cdot C_T \cdot V_R$
- Positive edge-triggered frequency input
- Equal internal reference generator high-level ouput and comparator high level output



PLASTIC PACKAGE
(SIP-08P-M03)

PIN ASSIGNMENTS



(Front View)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	24	V
Surge Voltage at VCC	V_{CCS}	40 ($t \leq 50$ ms)	V
Zener Current	I_Z	20	mA
Power Dissipation	P_D	300 ($T_A \leq 85$ °C)	mW
Operating Temperature	T_A	-30 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8

Fig. 1 — MB4206 BLOCK DIAGRAM

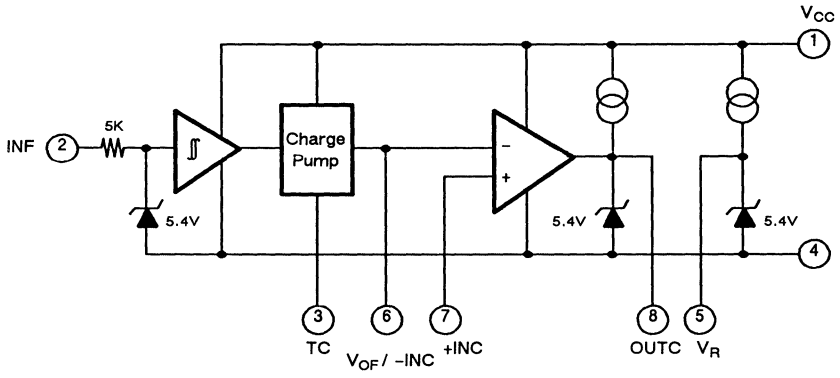
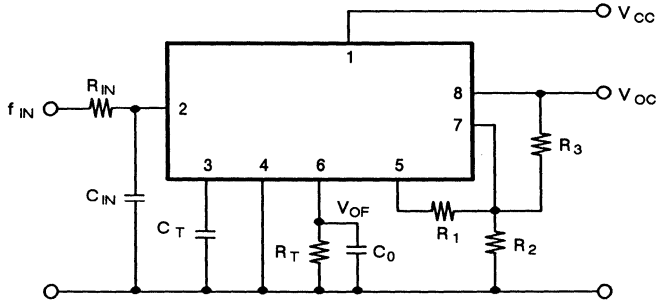
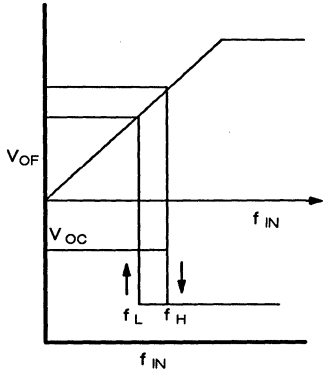


FIG. 2 — TYPICAL HOOKUP AND OPERATING PARAMETERS





The following equations define the operating frequency of the comparator.

$$f_H \cong \frac{1}{C_T R_T} \cdot \frac{R_2}{R_2 + \frac{R_1 R_3}{R_1 + R_3}}$$

$$f_L \cong \frac{1}{C_T R_T} \cdot \frac{R_2 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3}$$

R_{IN} and C_{IN} are needed when input noise is excessive.

8

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12V)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Power Supplies						
Power Supply Current	I_{CC}	—	—	7.0	10.0	mA
Power Supply Voltage	V_{CC}	—	6.5	—	24	V
Reference Voltage	V_R	I_{LR} = 1mA	5.0	5.4	5.8	V
Reference Voltage Temperature Coefficient	—	I_{LR} = 1mA	—	+1.4	—	mV/°C
F/V Converter						
Input High Voltage	V_{IH}	—	2.4	—	24	V
Input Low Voltage	V_{IL}	—	0	—	1.2	V
Positive-edge	—	—	1	—	—	V/ms
Negative-edge	—	—	0.1	—	—	V/ms
Input Current	I_I	V_{IHF} = 24V	—	4	8	mA
		V_{ILF} = 1.2V	—	—	0.1	mA
Output Current	I_O	V_{TC} = 2.5V	0.26	0.4	0.58	mA
F/V Coefficient [1]	K	C_T = 0.1 μF, R_T= 47kΩ, f = 100Hz	0.9	1.0	1.1	—
Linearity [2]	—	C_T = 0.1 μF, R_T= 47kΩ	—	±0.3	—	%
Comparator						
Input Offset Voltage [3]	V_{IO}	—	—	2.0	10	mV
Input Bias Current [4]	I_I	—	—	0.5	3	μA
Common Mode Input Voltage	V_{ICM}	—	0	—	V_R	V
Voltage Gain	A_V	R_L =10kΩ	—	100	—	dB
Output Voltage	V_{OL}	I_{SINK} = 3mA	—	0.1	0.2	V
	V_{OH}	I_L = 0.5mA	5.0	5.4	5.8	V
Sink Current	I_{SINK}	V_{OL} ≥1V	8	22	—	mA

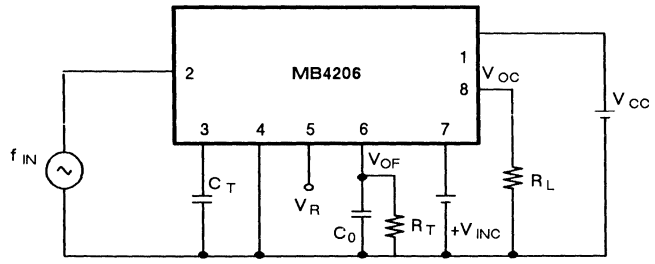
NOTES 1. $V_{OF} = K \cdot V_R \cdot C_T \cdot R_T \cdot f$

2. With f_{IN}= 100Hz as a reference, linearity is defined as the straight-line deviation over an input frequency range of 50 – to – 150 Hz — see TYPICAL PERFORMANCE CHARACTERISTICS.

3. The current flows from IC.

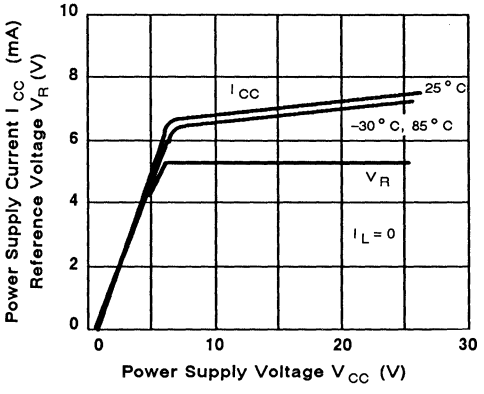
4. If V_{CC} is lower than V_R, use (V_{CC}-2).

Fig. 3 — TEST CIRCUIT

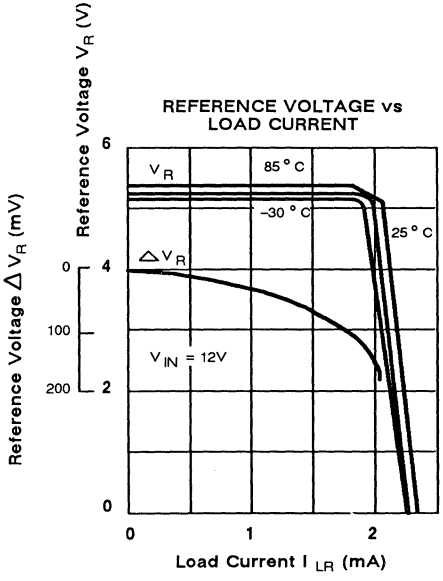


TYPICAL PERFORMANCE CHARACTERISTICS

POWER SUPPLY CURRENT/REFERENCE VOLTAGE vs POWER SUPPLY VOLTAGE



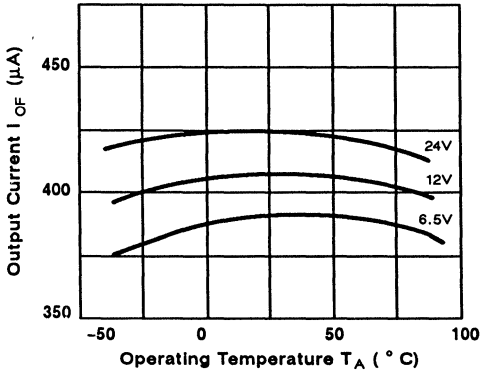
REFERENCE VOLTAGE vs LOAD CURRENT



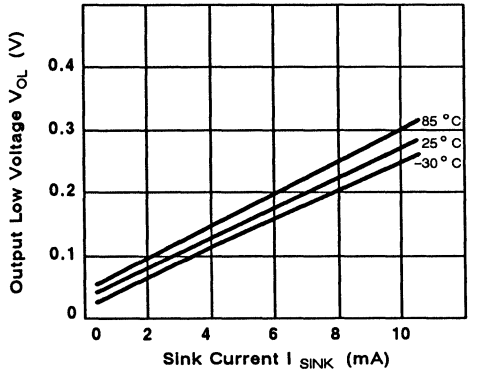
8

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

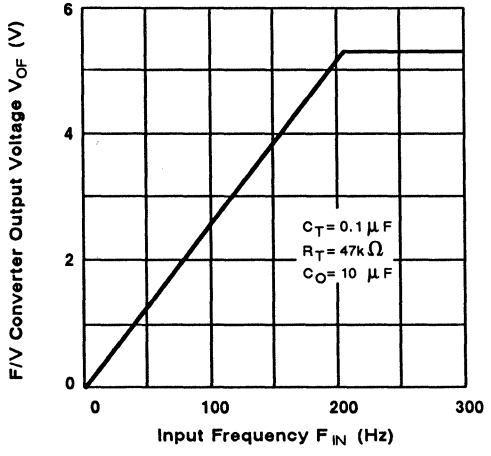
OUTPUT CURRENT vs OPERATING TEMPERATURE



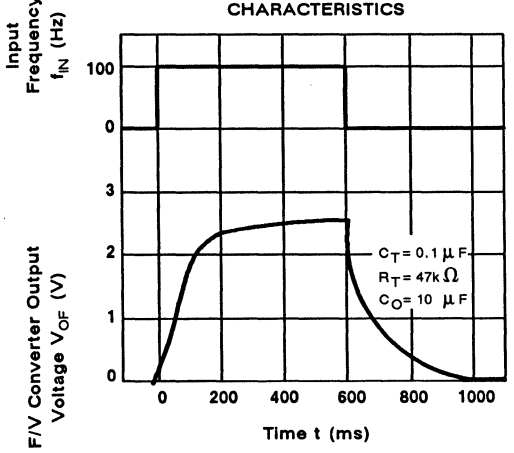
OUTPUT LOW VOLTAGE vs SINK CURRENT



F/V CONVERTER OUTPUT VOLTAGE vs INPUT FREQUENCY



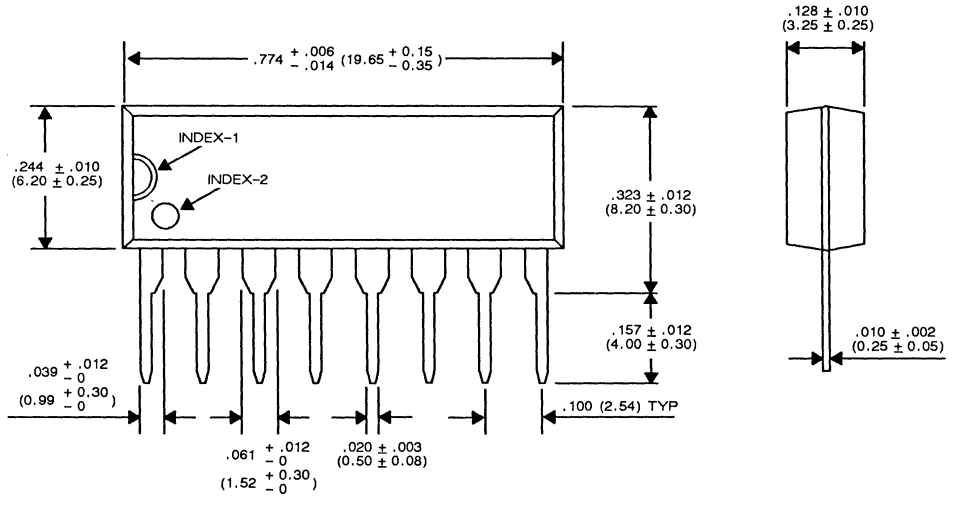
F/V CONVERTER TRANSMISSION CHARACTERISTICS



8

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-08P-M03)



Dimensions in
inches (millimeters)

S08010S-2C

The Fujitsu MB4207 is a single-power-supply frequency to voltage converter with comparator. The MB4207 can operate stably to noisy signal due to using the charge pump driven by a schmitt trigger and flip-flop circuit.

Comparator provides precise hysteresis output due to clamping at the reference voltage with zener diode.

FEATURES

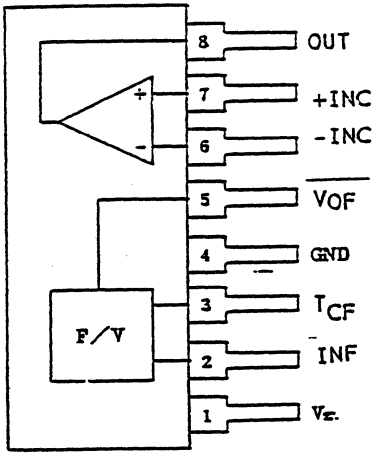
* A RC pair provides the coefficient of the conversion :

$$V_O = \frac{2}{3} \cdot V_Z \cdot C_T \cdot R_T \cdot f_{IN}$$

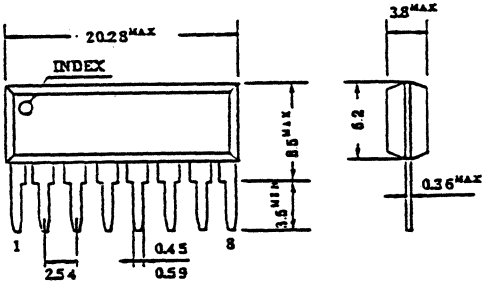
* Output is clamped at the built-in reference voltage (High-level) .

* Positive-edge trigger frequency input

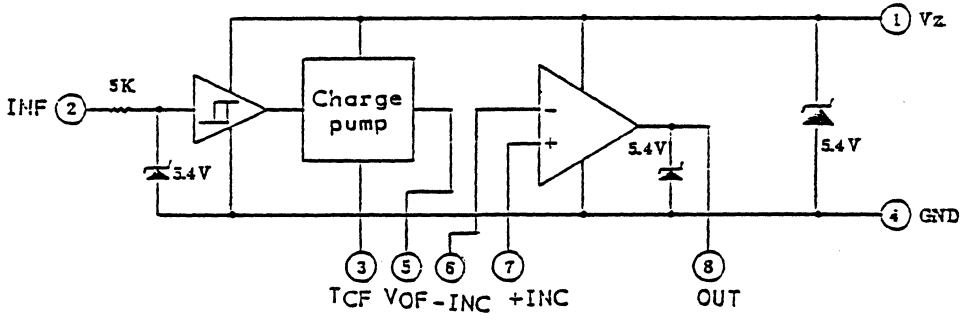
PIN ASSIGNMENT
(FRONT VIEW)



Package Dimension
(Unit : mm)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (T_A = 25°C)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	*24	V
Surge Voltage at V_{CC}	V_{CCS}	**100	V
Zener Current	I_Z	30	mA
Power Dissipation	P_D	***300	mW
Operating Temperature	T_{OP}	-30 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Note :* R_S=680Ω
** t< 50msec, R_S=680Ω
*** T_A<85°C

8

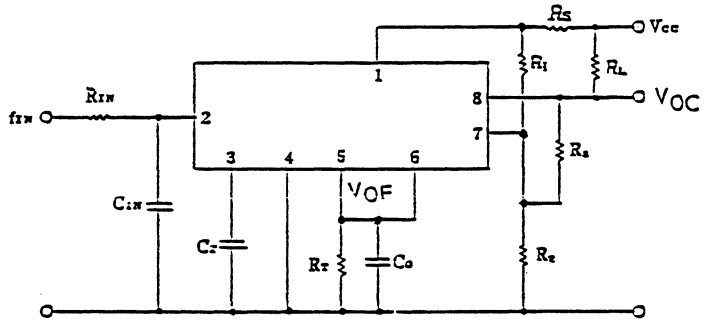
ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC}=12V, R_S=680Ω)

Parameter		Conditions	Symbol	Value			Unit
				Min.	Typ.	Max.	
Suuply Current		R_S=0Ω, V_{CC}=4.8V	I_{CC}	-	3.0	5.0	mA
Reference Voltage		See Fig.2, p.5.	V_Z	5.0	5.4	5.8	V
		V_{CC}=10 to 16 V	ΔV_Z	-	0.05	0.1	V
V/F Converter	Input High-Level		V_{IH}	2.4	-	24	V
	Input Low-level		V_{IL}	0	-	1.2	V
	Positive-edge			1	-	-	V/ms
	Negative-edge			0.1	-	-	V/ms
	Input Current	V_{IHF}=24V	I_{INF}	-	4	8	mA
		V_{ILF}=1.2V		-	-	0.1	mA
	Output Current	V_{TCF}=2.5V	I_{OF}	0.26	0.4	0.58	mA
	F/V Coefficient	C_T=0.1μF, R_T=47kΩ f=100Hz	K *1	0.9	1.0	1.1	
	Linearity Error	C_T=0.1μF, R_T=47kΩ *2		-	±0.3	-	%
Comparater	Input Offset Voltage		V_{IOC}	-	2	10	mA
	Input Bias Current	*3	I_{IBC}	-	0.5	3	μA
	Common Mode Input Voltage		V_{CM}	0	-	3	V
	Voltage Gain	R_L=10kΩ	A_V	-	100	-	dB
	Output Voltage	I_{SINK}=3mA	V_{OLC}	-	0.1	0.2	V
		I_L=0.5mA	V_{OLC}	5.0	5.4	5.8	V
	Sink Current	V_{OLC}≤1V	I_{SINK}	8	20	-	mA

Note : *1 $V_O=(2/3)\cdot K\cdot V_Z\cdot C_T\cdot R_T\cdot f_{IN}$
*2 At 50/100 Hz on the basis at 100 Hz
*3 The current flows ourwards from IC.

8

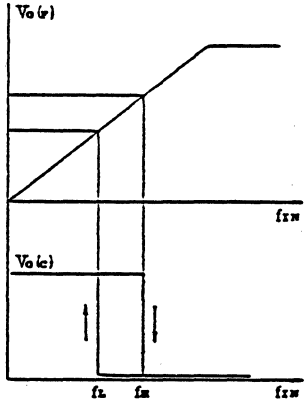
APPLICATION EXAMPLE



Operating frequency of the comparator is provided by the following equations.

$$f_H \fallingdotseq \frac{3}{2 C_2 R_2} \cdot \frac{R_2}{R_2 + R_1 /\!/ R_3}$$

$$f_L \fallingdotseq \frac{3}{2 C_2 R_2} \cdot \frac{R_2 /\!/ R_3}{R_1 + R_2 /\!/ R_3}$$



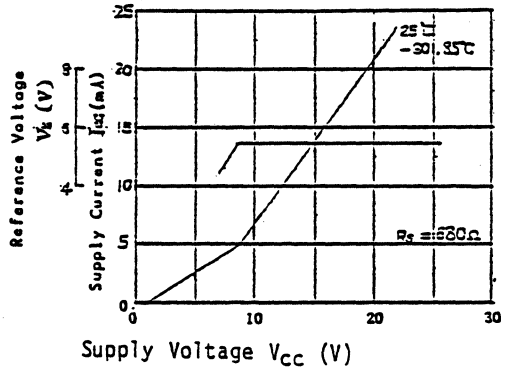
R_{IN} and C_{IN} are needed when the input has chattering noise.

8

SUPPLY CURRENT/REFRENCE VOLTAGE VS. SUPPLY VOLTAGE

Supply Current I_{CC} (mA)

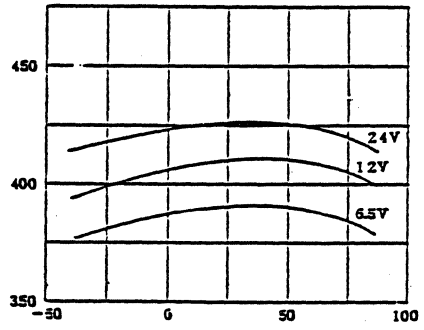
Reference Voltage V_Z (V)



Supply Voltage V_{CC} (V)

OUTPUT CURRENT VS. AMBIENT TEMPERATURE

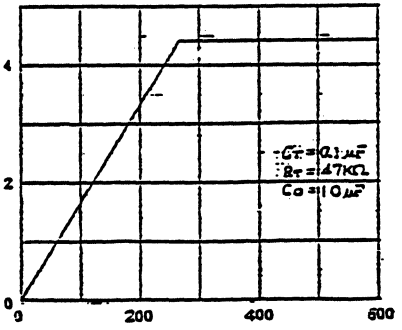
Output Current I_{OF} (μA)



Ambient Temp. T_A (°C)

F/V CONVERTER OUTPUT VOLTAGE VS. INPUT FREQUENCY

F/V Converter Output V_{OF} (V)

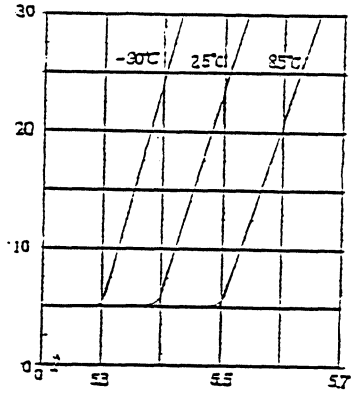


Input Frequency f_{IN} (Hz)

8

ZENER CURRENT VS. REFERENCE VOLTAGE

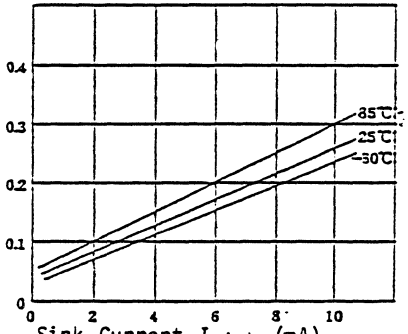
Zener Current I_Z (V)



Reference Voltage V_Z (V)

LOW-LEVEL OUTPUT VOLTAGE VS. SINK CURRENT

Low-Level Ouxput Voltage (V)

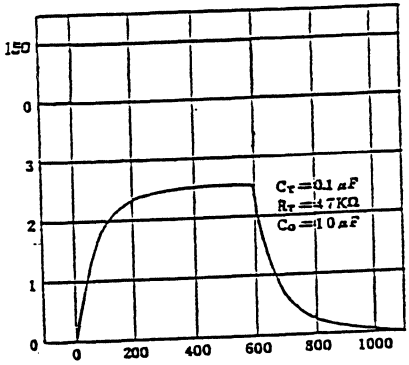


Sink Current I_{sink} (mA)

F/V CONVERTER TRANSITION CHARACTERISTICS

Input Frequency f_{IN} (Hz)

F/V Converter Output Voltage V_{OF} (V)



t (m sec.)

8

DSTV82-061

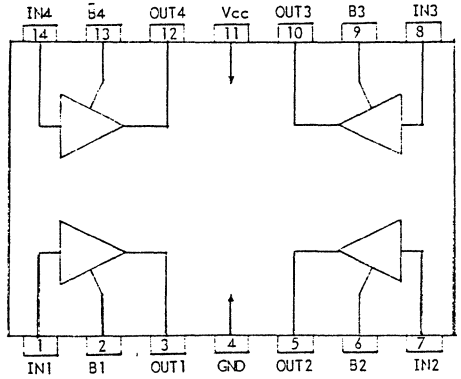
FUJITSU

Quad Preamplifier IC for Vertex Time Projection Chamber Sensor

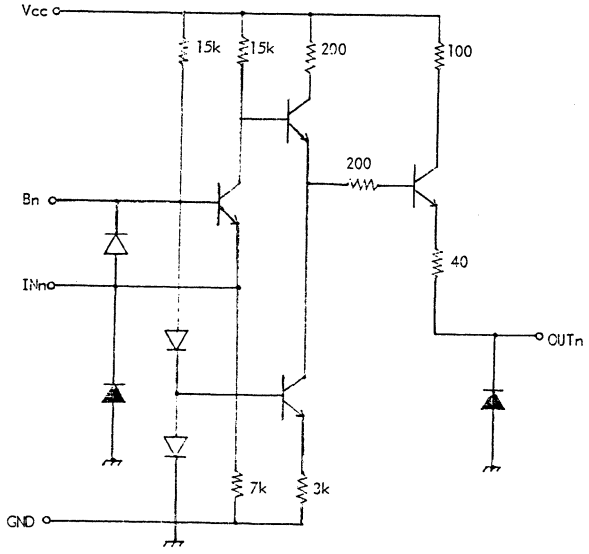
July 1984
DSTV84-062

The Fujitsu MB43458 is a quad preamplifier IC designed for Vertex Time Projection Chamber Sensor by Fujitsu

BLOCK DIAGRAM



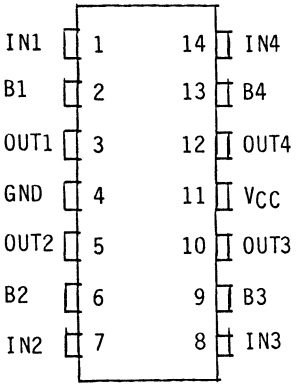
EQUIVALENT CIRCUIT (One Channel)



Note : Protection Diode

Where n is 1, 2, 3 and 4.

PIN ASSIGNMENT (TOP VIEW)



8

ABSOLUTE MAXIMUM RAINGS (T_A=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D *	280 (at $T_A \leq 75°C$)	mW
Operating Ambient Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Note : * Mounted on 5 x 5 cm^2 ceramic board.

RECOMMENDED OPERATING CONDITIONS

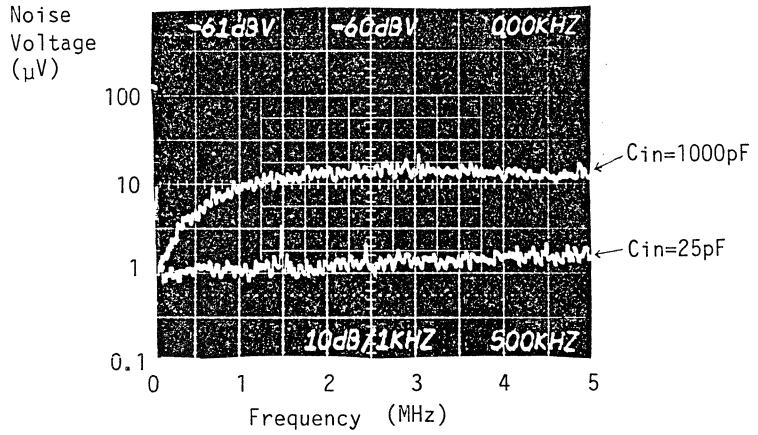
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	11.5	12.0	12.5	V
Operating Ambient Temperature	T_A	-20	+25	+75	°C

ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC}=12V, R_S=680Ω)

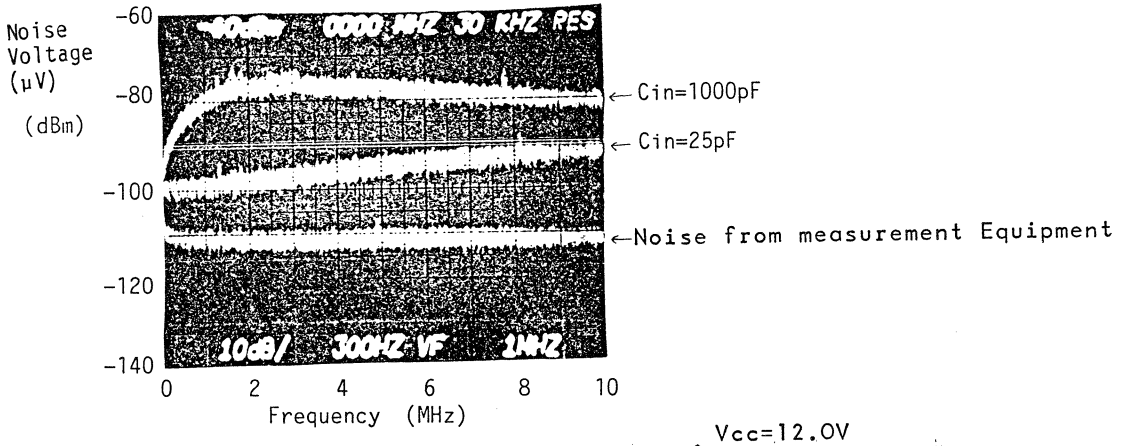
Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Input Voltage	See Fig.1	V_{IN}	1.8	2.2	2.6	V
Output Voltage	See Fig.1	V_{OUT}	4.7	5.7	6.7	V
Bias Voltage	See Fig.1	V_B	2.5	2.9	3.3	V
Supply Current	See Fig.1	I_{CC}	12	16	21	mA
	See Fig.2	1/gm	6.4	7.2	8.0	mV/μA
	See Fig.2	Δ1/gm	94	100		%
Noise Voltage	fq=1MHz, Cin=25pF See Fig.3			20		nV/$\sqrt{Hz}$

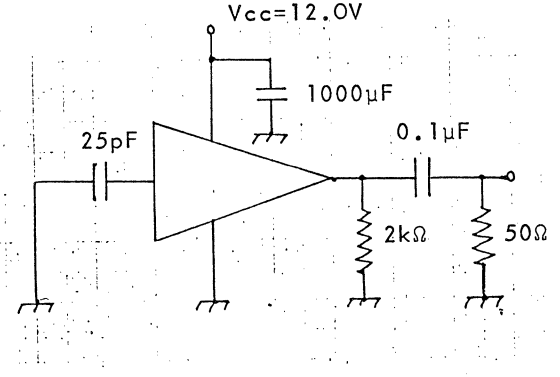
8

Impulse Noise Characteristics



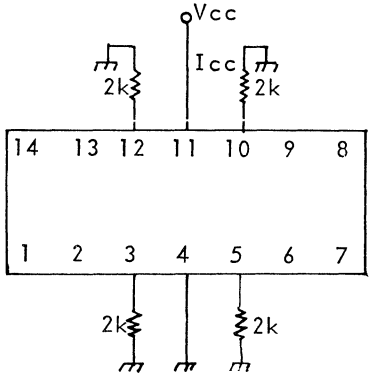
Random Noise Characteristics





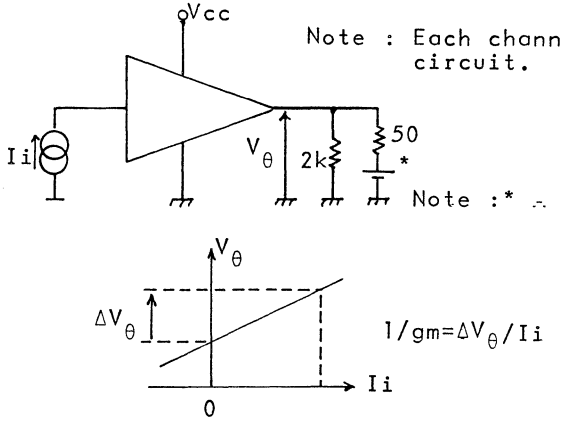
8

Fig.1



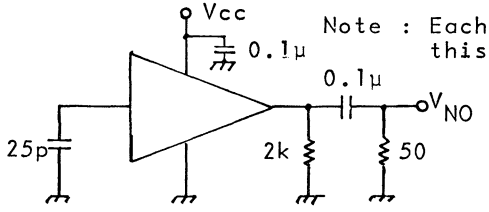
Input Pins : 1,7,8,14
Output Pins: 3,5,10,12
Bias Pins : 2,6,9,13

Fig.2

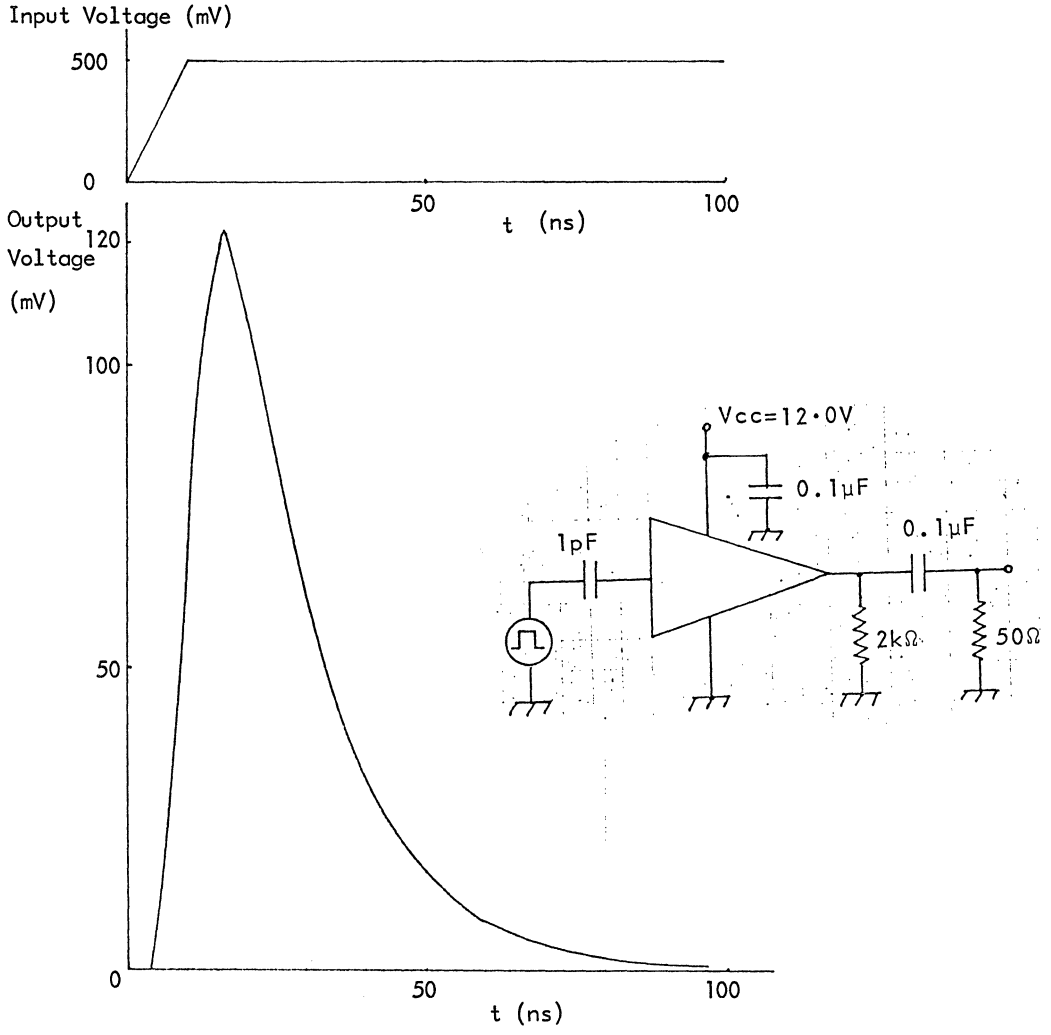


Note : Each channel has this circuit.

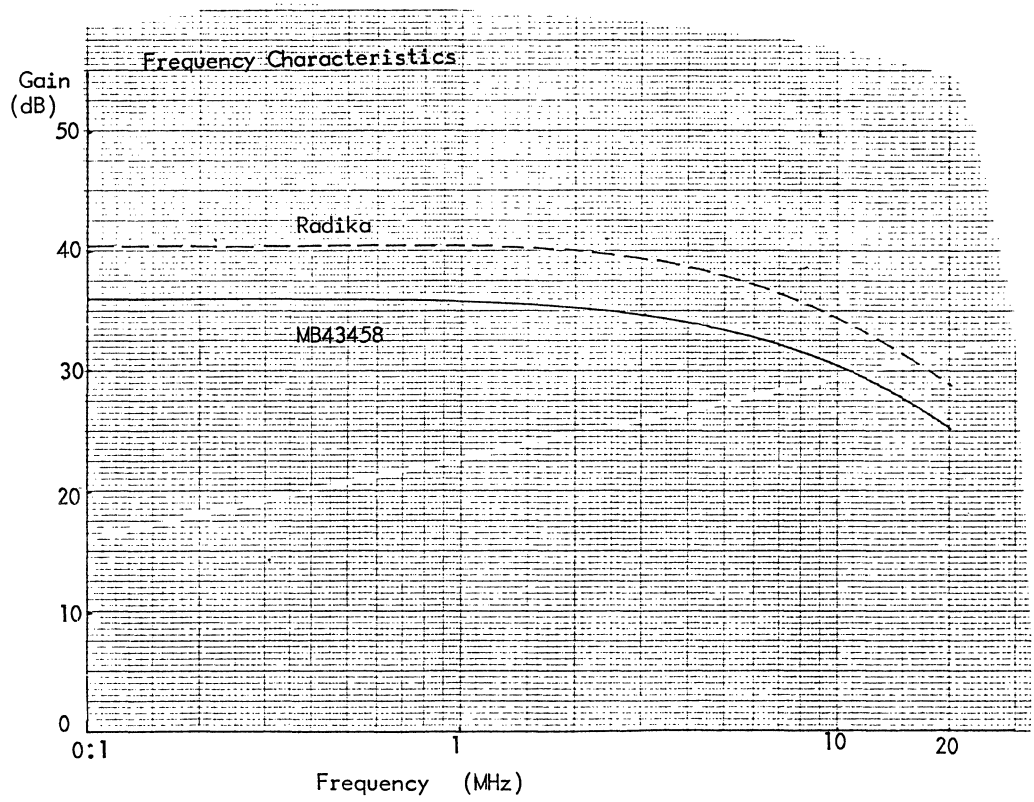
Fig.3

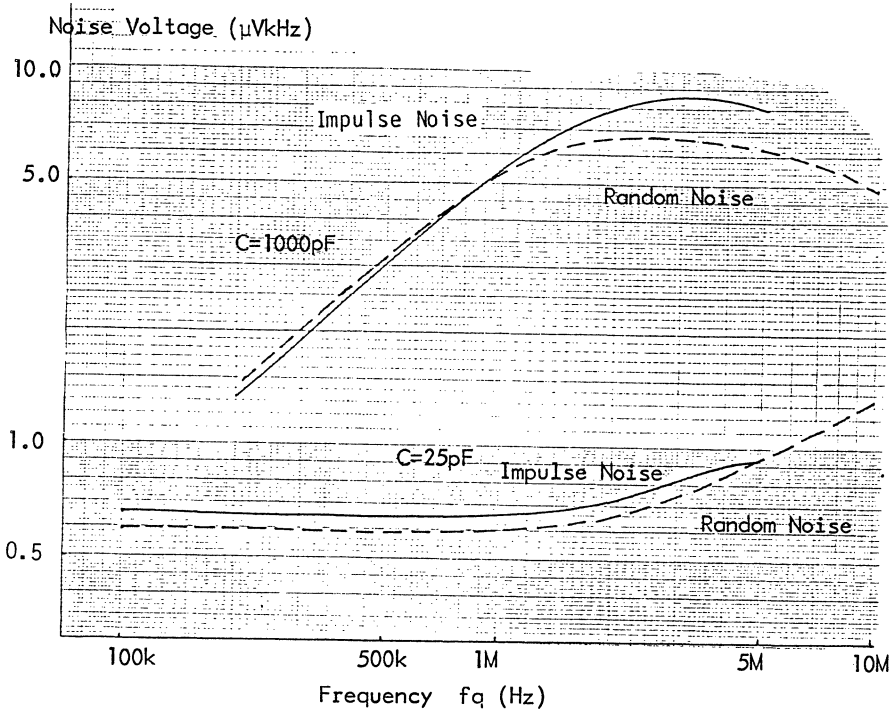


Note : Each channel has the this circuit.


Input Voltage (mV)
500
0
50
100
t (ns)
Output Voltage (mV)
120
100
50
0
50
100
t (ns)
Vcc=12·0V
0.1μF
1pF
0.1μF
2kΩ
50Ω

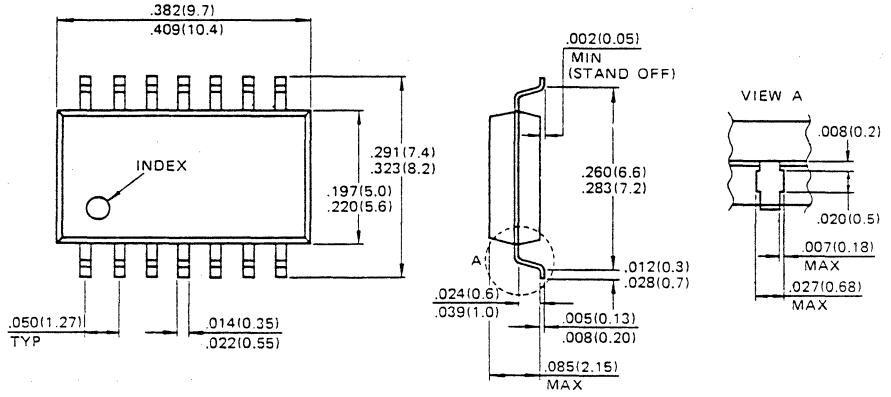
8


Frequency Characteristics
Gain
(dB)
50
40
30
20
10
0
Radika
MB43458
0:1
1
10
20
Frequency (MHz)


Noise Voltage (μVkHz)
10.0
5.0
1.0
0.5
Impulse Noise
Random Noise
C=1000pF
C=25pF
Impulse Noise
Random Noise
100k
500k
1M
5M
10M
Frequency fq (Hz)

8

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)

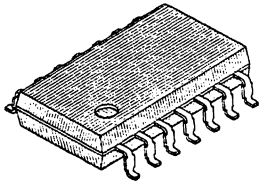


MB43468

QUAD PREAMPLIFIER IC FOR VERTEX TIME PROJECTION CHAMBER

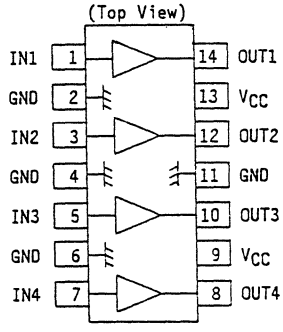
The Fujitsu MB43468 is a Quad preamplifier IC designed for Vertex Time Projection Chamber.

The basic circuit is a cascade amplifier with feedback.



PLASTIC PACKAGE
(FPT-14P-M01)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

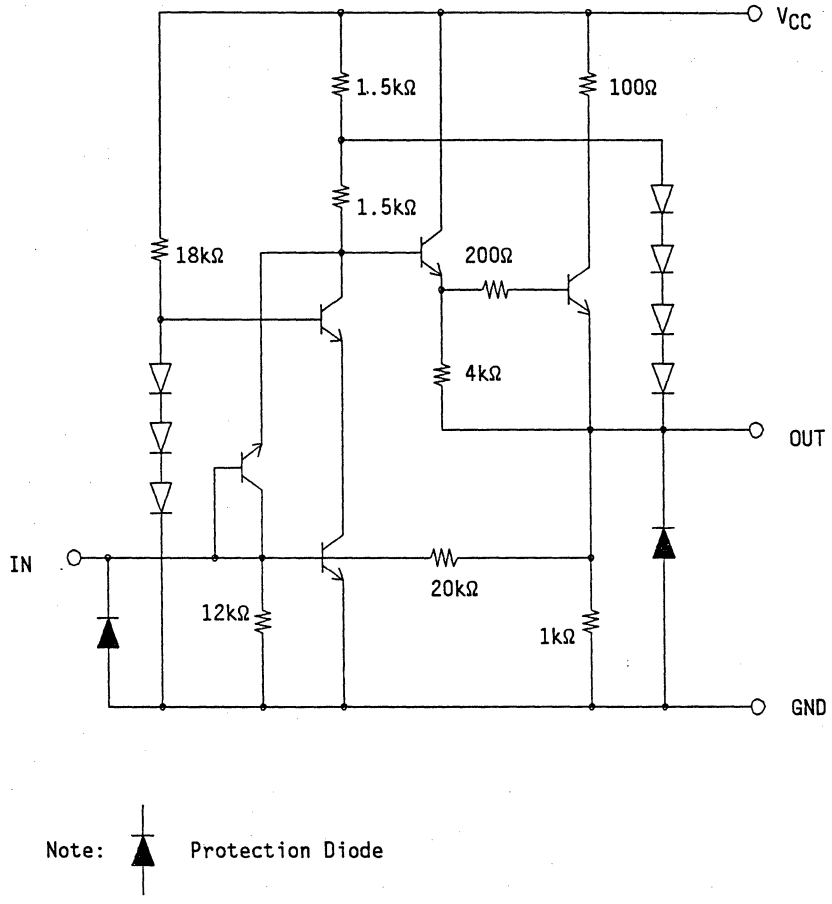
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	16	V
Input Voltage	V_I	-0.3 to (V_{CC}+0.3)	V
Power Dissipation	P_D	250	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

8

Fig.1- MB43468 EQUIVALENT CIRCUIT (1-CHANNEL)



Note: Protection Diode

8

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{CC}		7	8	9	V
Operaing Temperature	T_A		-20	25	75	°C

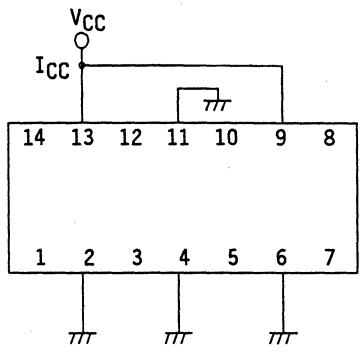
ELECTRICAL CHARACTERISTICS (V_{CC}=+8V, T_A=25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{OC}		10	14	20	mA
Input Voltage	V_I		0.62	0.72	0.82	V
Output Voltage	V_O		1.7	2.1	2.5	V
Transresistance Gain	1/gm	I_I=-10μA	-24	-20	-16	mV/μA
Gain Variation from channel-to-channel	Δ1/gm		94	100		%
Output Noise	VN	C_{IN}=5pF, freg=1MHz		20		nV/$\sqrt{Hz}$

8

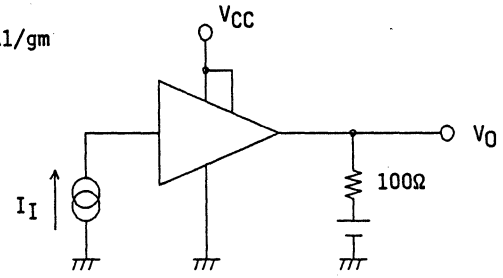
Fig.2 - TEST CIRCUITS

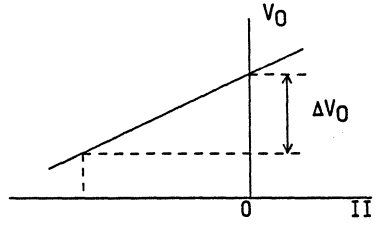
I_{CC}, V_I, V_O



Input Pins: 1, 3, 5, 7
Output Pins: 14, 12, 10, 8

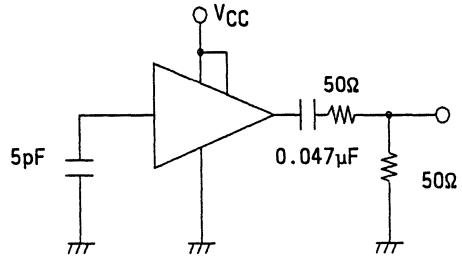
1/gm, Δ1/gm





1/gm = ΔV_O / I_I

VN



8

ELECTRICAL CHARACTERISTICS CURVES

Fig.3 - Gain vs. Frequency

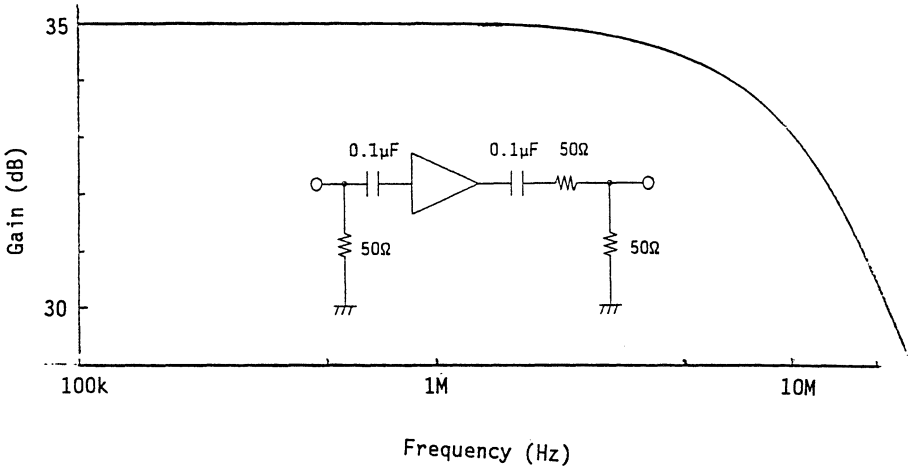
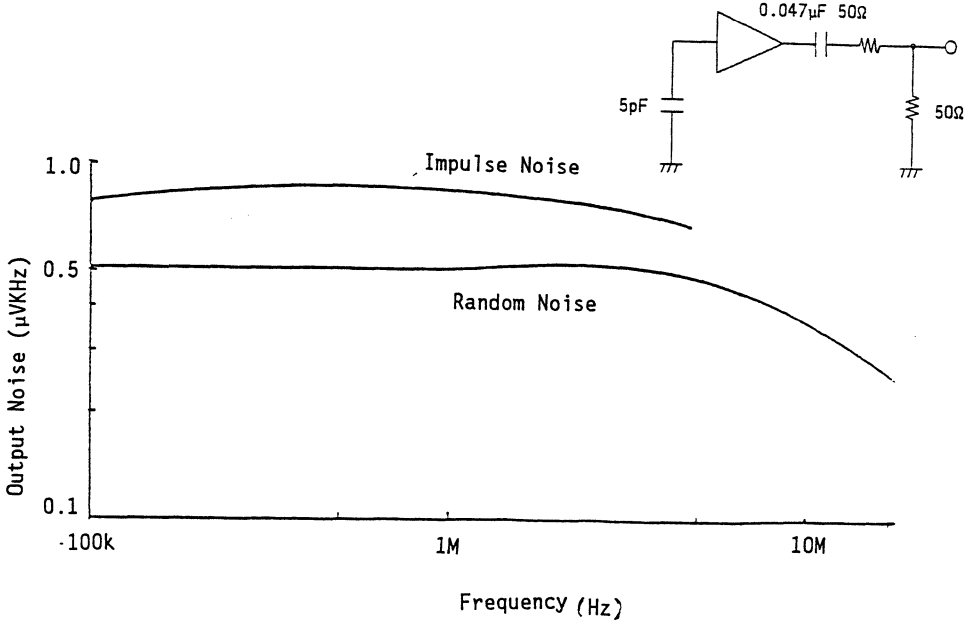


Fig.4 - Output Noise vs. Frequency



8

ELECTRICAL CHARACTERISTICS CURVES (Continued)

Fig.5 - Input Voltage vs. Time

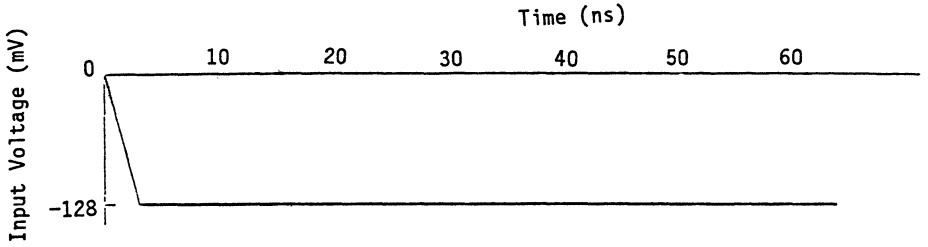
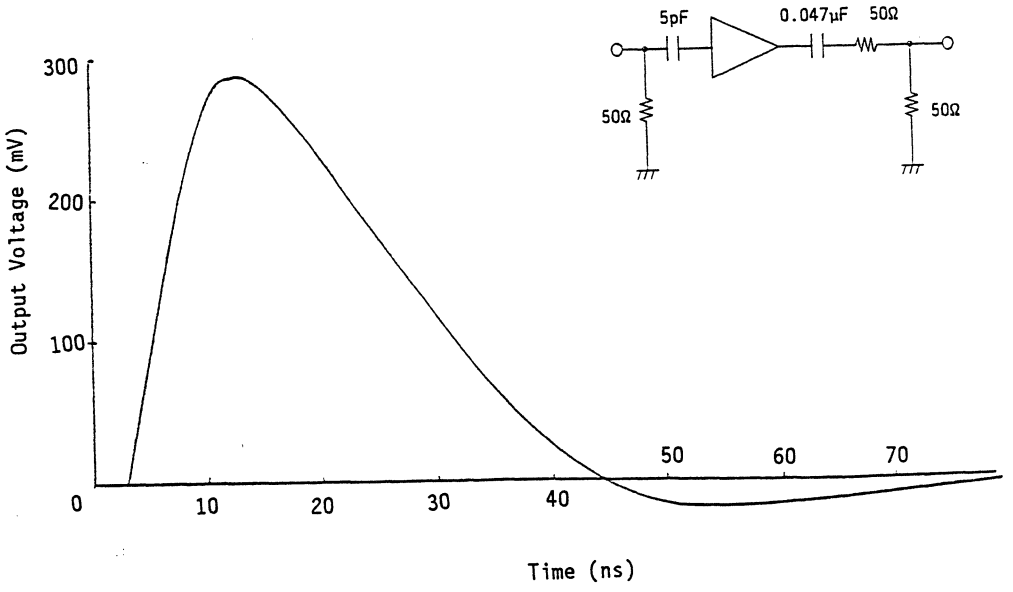


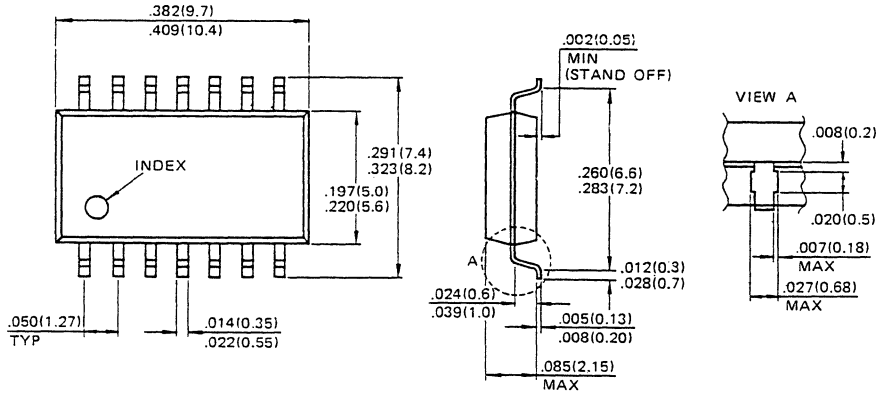
Fig.6 - Output Voltage vs. Time



8

PACKAGE DIMENSIONS

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



8

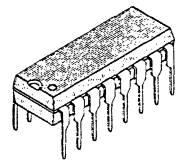
FUJITSU

MB47201

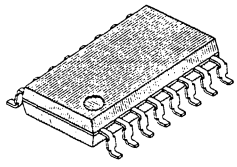
QUAD SPST BI-FET ANALOG SWITCH

TS566-A878
August 1987

The Fujitsu MB47201 is a quad SPST (Single-pole Signal-Throw) BI-FET analog switch manufactured using Fujitsu Advanced Bipolar Technology. The MB47201 has four independent one-input one-output bi-directional analog switch which provides a constant resistance over the wide temperature and input voltage ranges.
The logic level of its input is CMOS and TTL compatible and breake-before-make switching action can be surely operated.



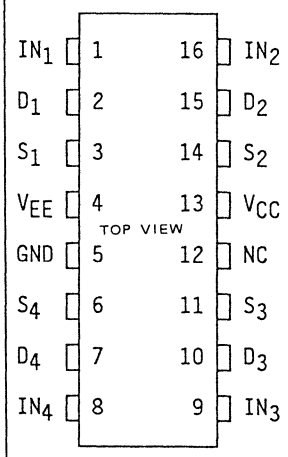
PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

- Low ON resistance : 110 Ω typ.
- Small temperature coefficient of ON resistance : 0.1 %/°C
- Small supply voltage coefficient of ON resistance : 0.4%/V
- High speed switching
- Break-before-make action : $t_{ON} > t_{OFF}$
- Low leakage current : 0.1 nA
- Logic Input level : CMOS/TTL
- Compatible with DG201, LF11201, SW-01

PIN ASSIGNMENT



ABSOLUTE MAXIMIM RATINGS

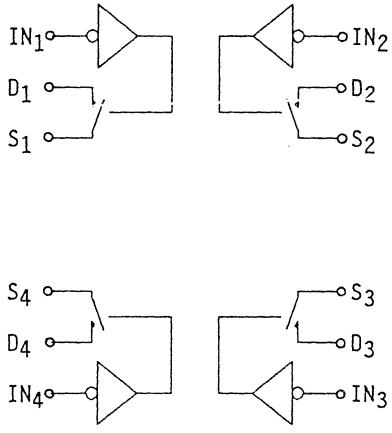
Rating	Symbol	Value	Unit
Power Supply Voltage (Between V_{CC} and V_{EE})		36	V
Positive supply voltage (Between V_{CC} and GND)		36	V
Analog Input Voltage	V_{INA}	V_{EE}-10 to V_{CC}+1	V
Logic Input Voltage	V_{IND}	-4 to V_{CC}, ≥V_{EE}	V
Analog Input Current	I_{INA}	±30	mA
Power Dissipation	P_D	800	mW
Operating Temperature	T_A	-30 to +85	°C
Storage Temperature	TSTG	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

8

Fig.1 - MB47201 BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC}=15V, V_{EE}=-15V, T_A=25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
ON Resistance	R_{ON}	V_{INA}=0V, I_D=1mA		110	150	Ω
ON Resistance Matching		V_A=0, I_D=100μA		4	10	%
Analog Input Voltage	V_{INA}	I_D=1mA	10	11		V
		$\lvert\Delta R_{ON}/R(V_A=0)\rvert$<10%		-13	-10	
ON Resistance Distribution		$\lvert V_A\rvert \leq 10V$, $I_D \leq 1mA$ $\lvert\Delta R_{ON}/R(V_A=0)\rvert$		4	10	%
ON Resistance Coefficient with Temperature		V_A=0, I_D=100μA		0.1		%/°C
Analog Input Current	I_{NA}	$\lvert V_A\rvert \leq 10V$	5	10		mA
Source Current (OFF)	I_{SOFF}	V_S=10V, V_D=-10V		0.1	10	nA
Drain Current (OFF)	I_{DOFF}	V_S=10V, V_D=-10V		0.1	10	nA
OFF Isolation	I_{SOOFF}	f=500kHz, R_L=680Ω		58		dB
Crosstalk Attenuation	X_{CH}	f=500kHz, R_L=680Ω		70		dB
Turn ON Time	t_{ON}	V_S=-5V, R_L=1kΩ		300		ns
Turn OFF Time	t_{OFF}	V_S=-5V, R_L=1kΩ		200		ns
Break-before-make (t_{ON} to t_{OFF})	t_{BBM}			100		ns
Source Input Capacitance	C_{SOFF}	V_A=0		7		pF
Drain Input Capacitance	C_{DOFF}	V_A=0		7		pF
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}				1	μA
Input Low Current	I_{IL}		-10	-1		μA
Positive Supply Current	I_{CC}			6.8	9.5	mA
Negative Supply Current	I_{EE}		-6.0	-3.3		mA
Ground Current	I_{GND}		-5.0	-3.5		mA

Fig.2 - t_{ON}, t_{OFF} MEASUREMENT CIRCUIT

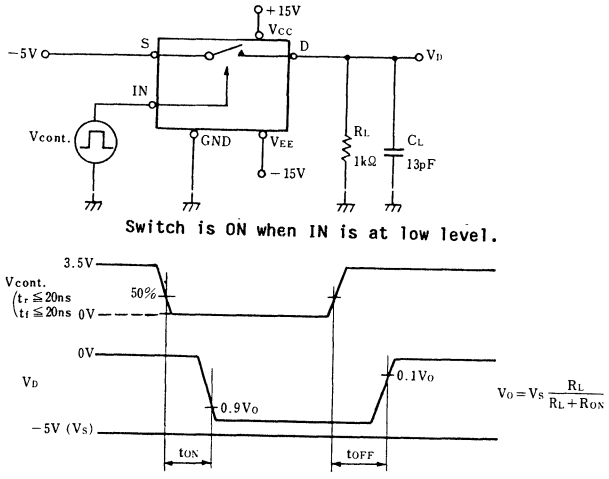


Fig.3 - I_{SOOFF} MEASUREMENT CIRCUIT

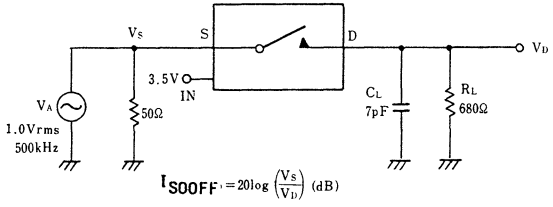
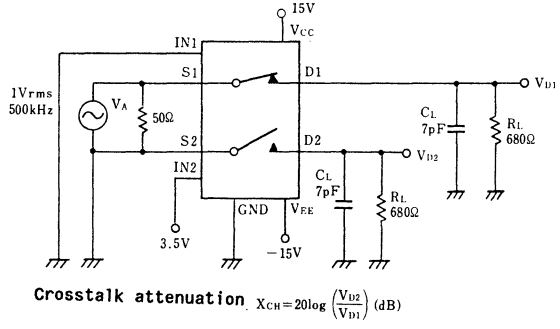


Fig.4 - X_{CH} MEASUREMENT CIRCUIT



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TYPICAL CHARACTERISTICS CURVES

Fig.5 - TURN ON/OFF TIME vs. ANALOG INPUT VOLTAGE

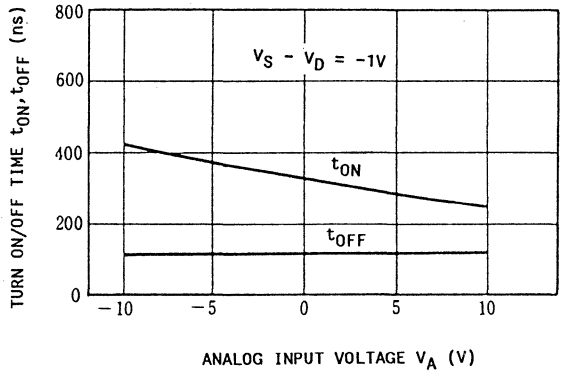

Fig.6 - TURN ON/OFF TIME vs. TEMPERATURE

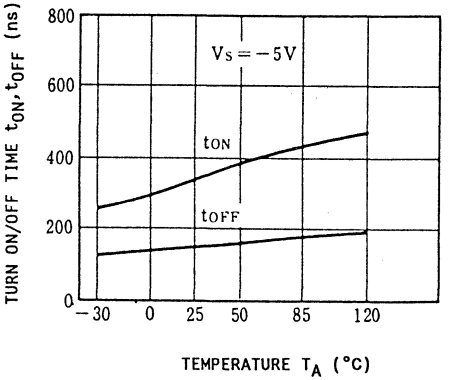

Fig.7 - ON RESISTANCE vs. ANALOG INPUT CURRENT

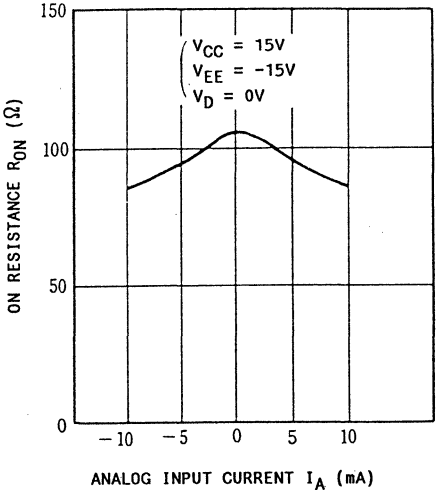

Fig.8 - ON RESISTANCE vs. ANALOG INPUT VOLTAGE

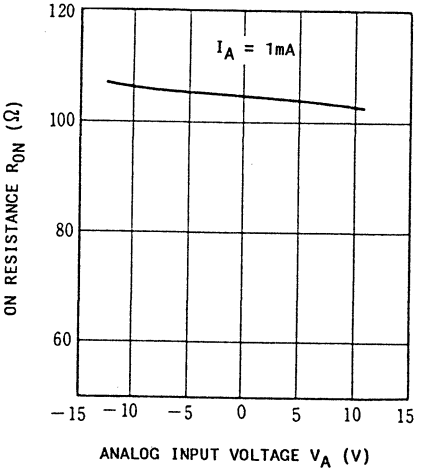

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Fig.9 - ON RESISTANCE vs. TEMPERATURE

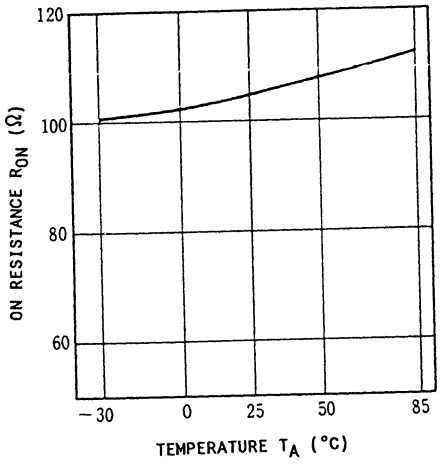


Fig.10 - ON RESISTANCE vs. POWER SUPPLY VOLTAGE

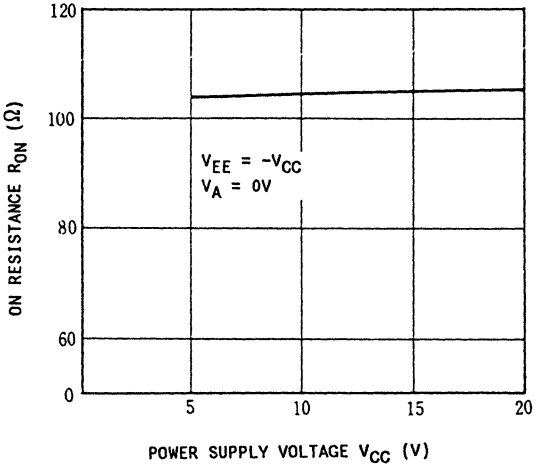


Fig.11 - OFF ISOLATION/CROSSTALK ATTENUATION vs. FREQUENCY

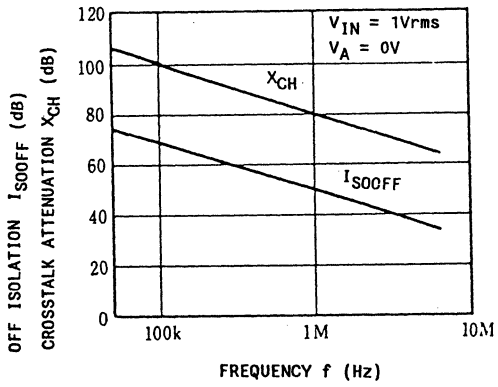
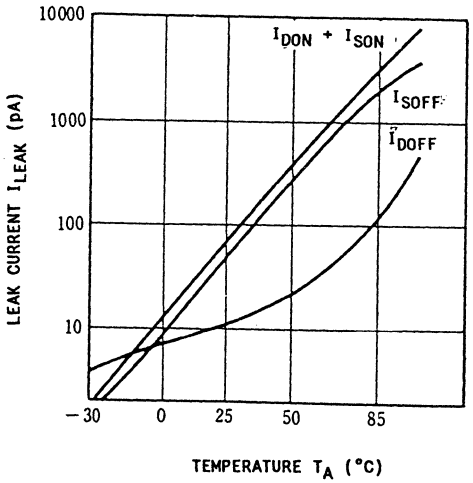


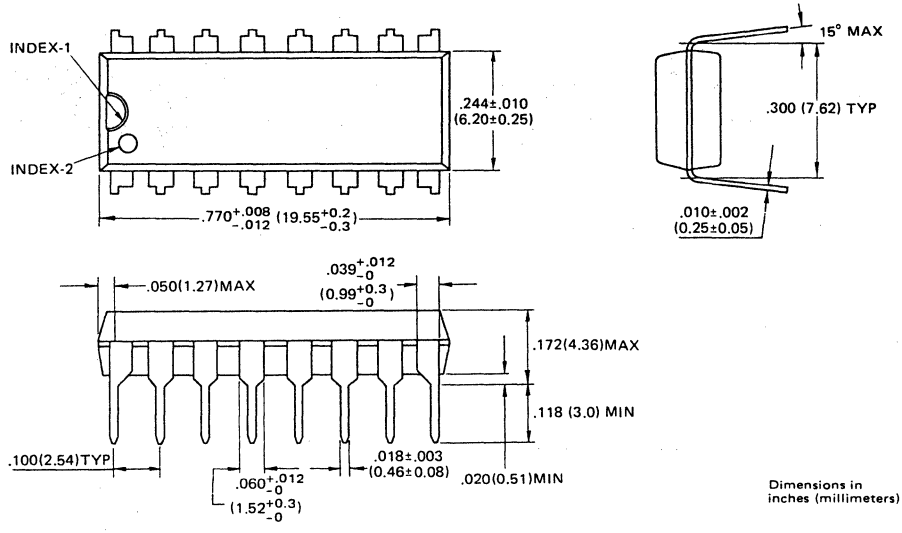
Fig.12 - LEAK CURRENT vs. TEMPERATURE



8

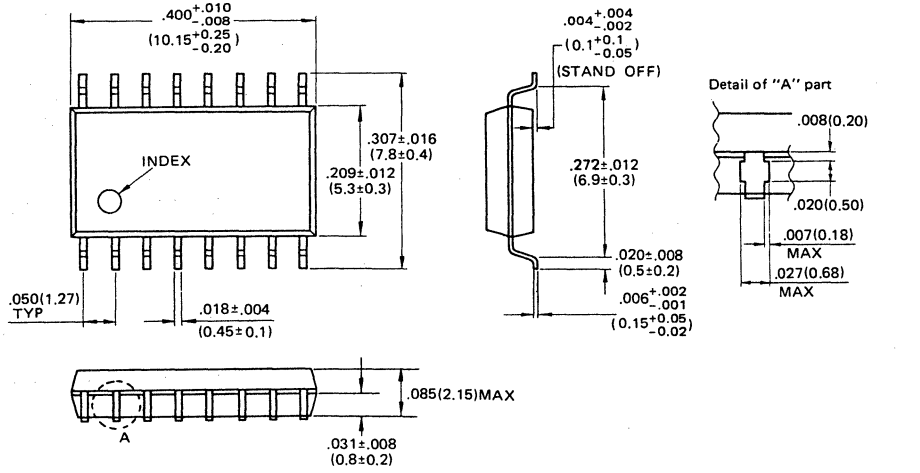
PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in inches (millimeters)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



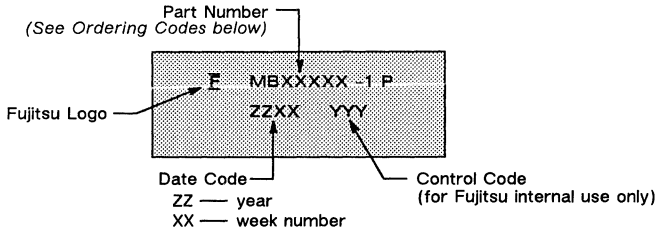
Dimensions in inches (millimeters)

Section 9

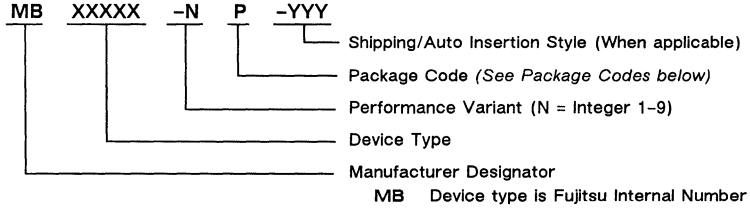
Ordering Information

Ordering Information

Product Marking



Ordering Codes



Note: Regarding ordering code, please contact your Fujitsu Sales Office for more information.

Package Codes

Ceramic	
Package Type	*Package Code*
DIP (Side Brazed)	C, CC
DIP (CERDIP)	Z
Flatpack	CF

Plastic	
Package Type	*Package Code*
LCC (Leaderless Chip Carrier)	PV
DIP (Dual In-line Package)	P, M
Single In-line, Straight Leads	PS
Flatpack	PF
Single In-line, Zig-zag Leads	PSZ

Linear Products by Part Number

with Second Source Cross References

Part Number	*Package*	*Pins*	*Description*	*Alternate Source*	*Section*
MB3106	PS	8	Dual Low Noise Pre-Amp		Sect 3. Audio
MB3110A	PS	8	Dual Control Amplifier		Sect 3. Audio
MB3501	P	14	Wide Band Video Amplifier		Sect 8. Other Analog Products
	PF	14			
MB3603	P	14	High Gain Op Amp	µA741	Sect 1. Operational Amplifiers
	C	14			
MB3604	C	16	High Frequency Op Amp		Sect 1. Operational Amplifiers
	P	16			
MB3607	P	8	Dual Op Amp	MC1458	Sect 1. Operational Amplifiers
	C	8			
	PF	8			
MB3609	P	8	High Gain Op Amp	LM741	Sect 1. Operational Amplifiers
	C	8			
MB3614	M	14	Quad Operational Amplifier	LM324	Sect 1. Operational Amplifiers
	C	14			
	PF	14			
MB3615	M	14	Quad Operational Amplifier	MC3303	Sect 1. Operational Amplifiers
	PF	14			
MB3714A	PS	8	6W Audio Power Amplifier		Sect 3. Audio
MB3715A	PS	8	6W Audio Power Amplifier		Sect 3. Audio
MB3722	PS	12	5.8W Dual Audio Power Amplifier		Sect 3. Audio
MB3730A	PS	7	14W BTL Audio Power Amplifier		Sect 3. Audio
MB3731	PS	12	18W BTL Audio Power Amplifier		Sect 3. Audio
MB3732	PS	7	14W BTL Audio Power Amplifier		Sect 3. Audio
MB3733	PS	12	20W BTL Audio Power Amplifier		Sect 3. Audio
MB3734	PS	9	14W BTL Audio Power Amplifier		Sect 3. Audio
MB3735	PS	9	20W BTL Audio Power Amplifier		Sect 3. Audio
MB3736	PS	12	15W BTL Audio Power Amplifier		Sect 3. Audio
	PSZ	12			
MB3737	PS	12	25W BTL Audio Power Amplifier		Sect 3. Audio
	PSZ	12			
MB3752	M	14	Series Voltage Regulator	µA723	Sect 4. Power Supply Control
	C	14			
	PF	14			
MB3756	PS	8	Series Voltage Regulator, 3 Outputs		Sect 4. Power Supply Control
MB3759	M	16	Pulse Width Control Circuit	TL494	Sect 4. Power Supply Control
	C	16			
	PF	16			
MB3761	P	8	Voltage Detector		Sect 4. Power Supply Control
	PF	8			
	PS	8			
MB3763	M	8	Bi-Directional Motor Driver		Sect 5. Motor Driver
	PF	8			
	PS	8			

Linear Products by Part Number

with Second Source Cross References (Continued)

Part Number	*Package*	*Pins*	*Description*	*Alternate Source*	*Section*
MB3764	P	16	9-Level Detector & D. for Level Meter		Sect 8. Other Analog Products
MB3769	P PF	16 16	High Speed PWM Control Circuit		Sect 4. Power Supply Control
MB3771	P PF PS	8 8 8	Power Supply Monitor		Sect 4. Power Supply Control
MB3773	P PF PS	8 8 8	Power Supply Monitor w/Timer		Sect 4. Power Supply Control
MB3854	P PF	8 8	Bi-Directional Motor Driver		Sect 5. Motor Driver
MB4001	P PF	8 8	High Speed Comparator	µA710	Sect 2. Comparators
MB4002	P PF	8 8	High Speed Comparator	µA710 (Impr)	Sect 2. Comparators
MB4051	M	42	8-Ch 10-Bit A/D Converter		Sect 7. Data Conversion A/D
MB4052	M C PF	16 16 16	4-Ch 8-Bit A/D Converter	TLS07C	Sect 7. Data Conversion A/D
MB4053	M Z PF	16 16 16	6-Ch 8-Bit A/D Converter		Sect 7. Data Conversion A/D
MB4056	P Z	20 20	8-Ch 8-Bit A/D Converter		Sect 7. Data Conversion A/D
MB4063	M Z PF	16 16 16	6-Ch 8-Bit ADC Subsystem	MC14443	Sect 7. Data Conversion A/D
MB4072	M Z PF	16 16 16	8-Bit Multiplying D/A Converter	DAC08	Sect 7. Data Conversion A/D
MB40176	P PF	28 28	6-Bit A/D, D/A Comb. Conv., Video		Sect 7. Data Conversion A/D, D/A
MB40576	P PF	16 16	6-Bit Ultra-High Speed		Sect 7. Data Conversion A/D
MB40547-7	CC	24	8-Bit Ultra-High Speed A/D, 1 LSB		Sect 7. Data Conversion A/D
MB40547-8	CC	24	8-Bit Ultra-High Speed A/D, 1/2 LSB		Sect 7. Data Conversion A/D
MB40578	P	22	8-Bit Ultra-High Speed A/D, 0.2% 1 In		Sect 7. Data Conversion A/D
MB40578-7	P	22	8-Bit Ultra-High Speed A/D, 0.4% 1 In		Sect 7. Data Conversion A/D
MB40748-8	Z	24	10-Bit High Speed D/A Converter		Sect 7. Data Conversion A/D
MB40748-9	Z	24	10-Bit High Speed D/A Converter		Sect 7. Data Conversion A/D
MB40776	P PF	16 16	6-Bit High Speed D/A Converter		Sect 7. Data Conversion A/D

Linear Products by Part Number

with Second Source Cross References (Continued)

Part Number	*Package*	*Pins*	*Description*	*Alternate Source*	*Section*
MB40778	P	18	8-Bit High Speed D/A Converter		Sect 7. Data Conversion A/D
MB40788	Z	24	10-Bit Ultra-High Speed D/A Converter		Sect 7. Data Conversion A/D
MB40874	P Z	20 20	4-Bit D/A with RAM		Sect 7. Data Conversion A/D
MB40978	M PF	42 44	8-Bit, 60MHz 3-Ch D/A Converter, RGB		Sect 7. Data Conversion A/D
MB412	P	14	Dual Diff. Line Drv. w/3S		Sect 8. Other Analog Products
MB413	C	16	Quad Diff. Line Rec. w/3S		Sect 8. Other Analog Products
MB4104	P	16	FM Stereo Multiplex Demodulator		Sect 3. Audio
MB4105	P	16	FM Stereo Multiplex Demodulator		Sect 3. Audio
MB4107	M PF	24 24	Floppy Disk VFO		Sect 6. Disk Drive
MB4108A	M PF	24 24	Floppy Disk VFO		Sect 6. Disk Drive
MB4111	Z CF	24 24	Magnetic Disk Head Amp, 4-Ch, 35V/V	SSI104	Sect 6. Disk Drive
MB4112	Z CF	24 24	Magnetic Disk Head Amp, 4-Ch, 9V/V	SSI105	Sect 6. Disk Drive
MB4113	Z CF	24 24	Magnetic Disk Head Amp, 4-Ch, 35V/V		Sect 6. Disk Drive
MB4117-4	P CF PF	22 24 24	Magnetic Disk Head Amp, 4-Ch, 110V/V	SSI117	Sect 6. Disk Drive
MB4117-6	CF P	28 28	Magnetic Disk Head Amp, 6-Ch, 110V/V	SSI117	Sect 6. Disk Drive
MB4118-4	P CF PF	24 24 24	Magnetic Disk Head Amp, 4-Ch, 110V/V	SSI118	Sect 6. Disk Drive
MB4118-6	P CF	28 28	Magnetic Disk Head Amp, 6-Ch, 110V/V	SSI118	Sect 6. Disk Drive
MB4204	P PF	14 14	Quad Comparator	LM339	Sect 2. Comparators
MB4205	PS	8	High Power Comparator		Sect 2. Comparators
MB4206	M P	8 8	Frequency-to-Voltage Converter		Sect 8. Other Analog Products
MB4207	M P	8 8	Frequency-to-Voltage Converter		Sect 8. Other Analog Products
MB4313	Z	16	Read/Write Bus Driver/Receiver		Sect 6. Disk Drive
MB4316	Z	16	Driver/Receiver Disk Head Amp		Sect 6. Disk Drive
MB4319	Z	16	Peak Detector for Head Posn. Ctrl		Sect 6. Disk Drive
MB43458	PF	14	Quad Preamplifier IC		Sect 8. Other Analog Products
MB43468	PF	14	Quad Preamplifier IC		Sect 8. Other Analog Products

Linear Products by Part Number

with Second Source Cross References (Continued)

Part Number	*Package*	*Pins*	*Description*	*Alternate Source*	*Section*
MB47082	P PF PS	8 8 8	J-FET Operational Amplifier	TL082	Sect 1. Operational Amplifiers
MB47201	P PF	16 16	Quad SPST BI-FET Analog Switch		Sect 8. Other Analog Products
MB47358	P PF PS	8 8 9	Dual Operational Amplifier	LM358	Sect 1. Operational Amplifiers
MB47393	P PF PS	8 8 9	Dual Comparator	LM393	Sect 2. Comparators
MB47833	P PF PS	8 8 9	Low Noise Dual Operational AMP	LM833	Sect 1. Operational Amplifiers
MB87020	P	40	16-Bit A/D, D/A Comb, Conv., Audio		Sect 7. Data Conversion A/D, DA
MB88301A	PF p	16 16	13-Bit x 1-Ch, 6-Bit x 3-Ch D/A Converter		Sect 7. Data Conversion D/A

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Section 10

Sales and Distributors Locations

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc., with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to include: one R&D division, two marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The R&D Division, APD (Advanced Products Division), using U.S.-based engineering, has jointly developed RISC for Sun Microsystems and Ethernet®, a chip set used in local area networks. APD also markets AFP, an adaptive filter processor, and EtherStar™, the first VLSI device to integrate both StarLAN™ and Ethernet protocols into one device.

The Microwave and Optoelectronics Division markets GaAs, FETSs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors. The second marketing division, and the largest FMI division, is ICD (Integrated Circuits Division).

Memory and programmable devices marketed by ICD include: DRAMs, EPROMs, EEPROMs, NOVRAMs, CMOS Masked ROMs, bipolar PROMs, CMOS SRAMs, ECL RAMs, STRAMs (the first Self-timed RAM), high speed ECL Logic, Linear ICs and transistors.

ASIC products offered by ICD include: bipolar Gate Arrays and CMOS Gate Arrays and Standard Cells. Customer support and customer CAE training for ASIC designs is available through FMI's five design centers: San Jose, Dallas, Atlanta, Chicago, and Boston with a sixth design center planned for Newport Beach.

Microcomputer and communications products offered by ICD include: 4-bit MCUs, 8- and 16-bit MPUs, SCSI and controllers, DSPs, prescalers, and PLLs.

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, FMI opened the Gresham Manufacturing Division to manufacture ASIC products. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, Fujitsu Components of America, markets connectors, keyboard, plasma displays, relays, and hybrid ICs.

Fujitsu Mikroelektronik GmbH (European Sales Center)

Fujitsu Mikroelektronick GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a totally owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Western Europe. The wide range of IC products, LSI memories and, in particular, gate arrays are noted throughout Western Europe for design excellence and unmatched reliability. Five branch offices to support Fujitsu's semiconductor operations are located in Munich, London, Paris, Stockholm, and Milan.

Fujitsu Microelectronics Ireland, Ltd (European Production Center)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980 in the suburbs of Dublin as Fujitsu's European Production Center for integrated circuits. FME supplies 64K/256K DRAMs, 64K CMOS/NMOS EPROMs, 256K EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd (European Design Center)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with a highly-sophisticated CAD system to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Pacific Asia Ltd. (Asian/Oceanian Sales Centre)

Fujitsu Microelectronics Pacific Asia Ltd. (FMP) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

Headquarters Locations – Worldwide

WORLD HEADQUARTERS

Fujitsu Limited

Furukawa Sogo Bldg., 6-1
Marunouchi 2-chrome, Chiyoda-ku
Tokyo 100, Japan
Tel: 011-81-3-216-3211
FAX: 781-222-4361
2224361 FT TOR J

NORTH/SOUTH AMERICAN HEADQUARTERS

Fujitsu Microelectronics, Inc.

3545 North First Street
San Jose, CA. 95134-1804
Tel: (408) 922-9000
FAX: (408) 432-9045
TWX: 910-671-4915

EUROPEAN HEADQUARTERS

Fujitsu Mikroelektronik GmbH

Arabella Centre 9, OG./A
Lyoner Strasse 44-48 D-6000
Frankfurt am Main 71, F.R. Germany
Tel: 069-66320
Telex: 411963
FAX: 069-6632122

ASIAN/PACIFIC HEADQUARTERS

Fujitsu Microelectronics Pacific Asia Limited

805 Tsim Sha Tsui Centre
West Wing, 66
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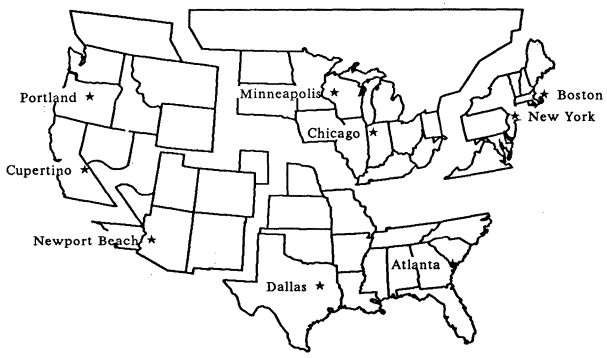

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Printed in USA OV0170-889F1