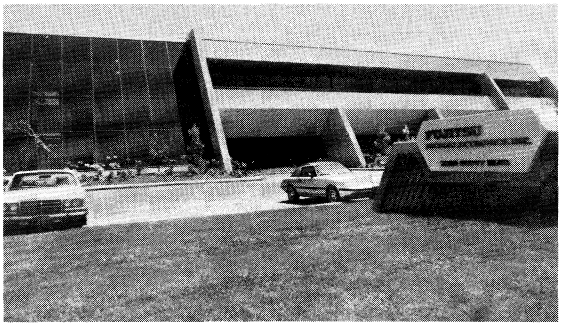
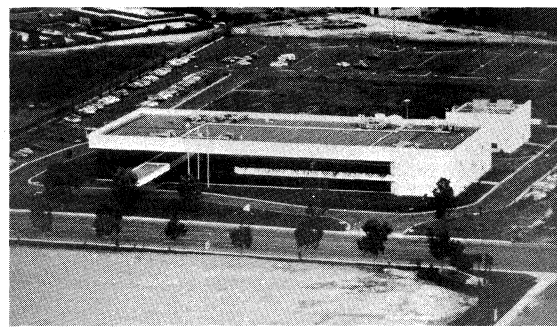
Memory Data Book

1984 Data Book

FUJITSU



FMI's Corporate Headquarters, Santa Clara, California.



FMI's San Diego Test and Assembly Plant.

About Fujitsu

Fujitsu Microelectronics, Inc. is a U.S. subsidiary of Fujitsu Limited of Tokyo. A California Corporation, FMI's IC Division is responsible for the marketing and sales of all semiconductor products in North, Central and South America.

Its parent company, Fujitsu Limited, was established in 1935 as an offshoot of Fuji Electric Co. Ltd's Communications Division. Today, Fujitsu Limited is Japan's leading computer manufacturer and one of the world's largest suppliers of telecommunications systems and semiconductors.

With 12 manufacturing sites and operations in nearly two dozen countries, Fujitsu Limited employs more than 37,000 people and enjoys sales of more than $3.8 billion.

Major product lines include the FACOM computers, and data processing equipment, personal computers, telecommunications switching systems, microwave and lightwave transmission systems, satellite equipment and video, data and telemetering systems, electronic components and semiconductors.

Fujitsu Microelectronics, Inc.

FMI was founded in 1979 as an offshoot of Fujitsu America, the American sales and marketing arm for all other Fujitsu disk drives, magnetic tape units, printers, modems and telecommunications equipment. A separate Component Sales Division (FAI/CSD) headquartered in Chicago, markets the company's bubble memories, relay switches and hybrid ICs.

In 1981, Fujitsu Limited also founded Fujitsu Mikroelectronik GmbH to market semiconductors in Europe and Fujitsu Eire, a semiconductor manufacturing company in Ireland.

The first products FMI offered were dynamic RAMs, soon followed by EPROMS, Static RAMs, ECL RAMs, PROMs, ROMs, as well as special products like microprocessors, transistors and floppy disc controllers.

In 1981 FMI entered the American custom logic market with its first Gate Array. (Fujitsu Limited had been making gate arays for the Japanese market since 1974.)

Fujitsu now offers a complete line of both CMOS and Bipolar Gate Arrays, as well as standard cells and pure custom circuits. FMI also has three regional Gate Array design centers to bring the designing process closer to customer.

Fujitsu's first American test and assembly plant was opened in 1982 in San Diego, California. That plant now produces more than three and a half million RAMs and EPROMs a month for U.S. customers. It also has developed a customized MIL STD 883B process for FMI's parts.

In that same year, FMI's product line expanded again, this time to include sophisticated microwave and optoelectronic components. And, by the end of the year a third division was born, the Professional Microsystems Division, to market Fujitsu's new small business computer, the Micro 16s.

Today, the tradition of selling only the highest quality products is carried on by FMI in its new corporate headquarters. The 90,000 square foot building on Scott Boulevard in Santa Clara unites two of the three divisions under one roof, and offers all divisions the room to grow that they will need to continue to meet the needs of the electronics revolution.

FMI offers its customers the highest quality and most reliable parts on the market today, whether it is memories, microprocessors, power transistors, or custom circuits. In the MOS memory product line, FMI offers dynamic RAMs, static RAMs, Static Column RAMs, EPROMs, and ROMs. In Bipolar technology, FMI has some of the world's most advanced ECL RAMs and PROMs (contact your local sales office for our PROM data book.)

Fujitsu's line of microprocessors and microcomputers, include a wide array of 4-bit, 8-bit and 16-bit NMOS and CMOS products. To accompany its microprocessors, Fujitsu also offers a full line of peripherals including an ETHERNET chip set and floppy disc controllers.

In addition to these LSI products, FMI offers a broad line of linear devices including numerous power and switching transistors (contact your local sales office for our Linear Data Book.)

FUJITSU
MICROELECTRONICS, INC.

Memory Data Book

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Fujitsu Microelectronics' Cross Reference Guide

AMD	FMI
AM9016	MB8116
AM9147	MBM2147
AM10415A	MBM10415A
AM10470A	MBM10470A
AM10474A	MBM10474A
AM100470A	MBM100470A
AM100474A	MBM100474
AM27256	MBM27256
AM27S28	MB7123
AM27S29	MB7124
AM27S32	MB7121
AM27S33	MB7122
AM27S180	MB7131
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Fairchild	FMI
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Harris	FMI
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Hitachi	FMI
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Hitachi	FMI
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HM10422	MBM10422A
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Inmos	FMI
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Motorola	FMI
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SM82S191	MB7138

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NMOS Dynamic RAMs

Quick Guide To Products in This Section

Device	Organization	Access Time (max)	Power Supply Volts	Power Dissipation	Package	Page
MB8117-10	16K x 1	100 nS	+5	182/20 mW	16-pin	1-2
MB8117-12	16K x 1	120 nS	+5	160/20 mW	16-pin	1-2
MB8118-10	16K x 1	100 nS	+5	182/17 mW	16-pin	1-14
MB8118-12	16K x 1	120 nS	+5	160/17 mW	16-pin	1-14
MB8264-15	64K x 1	150 nS	+5	275/22 mW	16-pin	1-23
MB8264-20	64K x 1	200 nS	+5	248/22 mW	16-pin	1-23
MB8264A-10	64K x 1	100 nS	+5	275/22 mW	16-pin	1-34
MB8264A-12	64K x 1	120 nS	+5	248/22 mW	16-pin	1-34
MB8264A-15	64K x 1	150 nS	+5	220/22 mW	16-pin	1-34
MB8264A-12W	64K x 1	120 nS	+5	305/33 mW	16-pin	1-47
MB8264A-15W	64K x 1	150 nS	+5	275/33 mW	16-pin	1-47
MB8265-15	64K x 1	150 nS	+5	275/28 mW	16-pin	1-54
MB8265-20	64K x 1	200 nS	+5	248/28 mW	16-pin	1-54
MB8265A-10	64K x 1	100 nS	+5	275/25 mW	16-pin	1-67
MB8265A-12	64K x 1	120 nS	+5	248/25 mW	16-pin	1-67
MB8265A-15	64K x 1	150 nS	+5	220/25 mW	16-pin	1-67
MB8266A-10	64K x 1	100 nS	+5	275/25 mW	16-pin	1-82
MB8266A-12	64K x 1	120 nS	+5	248/25 mW	16-pin	1-82
MB8266A-15	64K x 1	150 nS	+5	220/25 mW	16-pin	1-82
MB8281-12	64K x 1	120 nS	+5	523*/33 mW	16-pin	1-97
MB8281-15	64K x 1	150 nS	+5	523*/33 mW	16-pin	1-97
MB81256-10	256K x 1	100 nS	+5	385/25 mW	16-pin	1-99
MB81256-12	256K x 1	120 nS	+5	358/25 mW	16-pin	1-99
MB81256-15	256K x 1	150 nS	+5	314/25 mW	16-pin	1-99
MB81257-10	256K x 1	100 nS	+5	385/25 mW	16-pin	1-110
MB81257-12	256K x 1	120 nS	+5	358/25 mW	16-pin	1-110
MB81257-15	256K x 1	150 nS	+5	314/25 mW	16-pin	1-110
MB81416-10	16K x 4	100 nS	+5	303/25 mW	18-pin	1-122
MB81416-12	16K x 4	120 nS	+5	275/25 mW	18-pin	1-122
MB81416-15	16K x 4	150 nS	+5	248/25 mW	18-pin	1-122
MB85101A-10	64K x 4	100 nS	+5	1110/88 mW	22-pin SIP	1-133
MB85101A-12	64K x 4	120 nS	+5	990/88 mW	22-pin SIP	1-133
MB85101A-15	64K x 4	150 nS	+5	880/88 mW	22-pin SIP	1-133
MB85103A-12	64K x 8	120 nS	+5	1980/176 mW	22-pin SIP	1-135
MB85103A-15	64K x 8	150 nS	+5	1760/176 mW	22-pin SIP	1-135
MB85108A-12	256K x 1	120 nS	+5	341/99 mW	22-pin SIP	1-137
MB85108A-15	256K x 1	150 nS	+5	303/99 mW	22-pin SIP	1-137

* Static Mode Power

MB8117-10
MB8117-12

NMOS 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

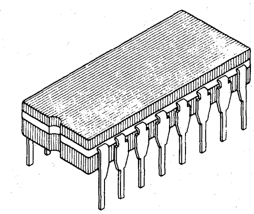
DESCRIPTION

The Fujitsu MB8117 is a fully decoded, dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory peripheral storage and environments where low power dissipation and compact layout are required.

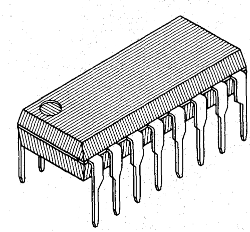
Multiplexed row and column address inputs permit the MB8117 to be housed in a standard 16-pin DIP. Pin outs conform to the JEDEC approved pin out.

The MB8117 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs are TTL compatible; the output is three-state TTL.



CERDIP PACKAGE
DIP-16C-C03

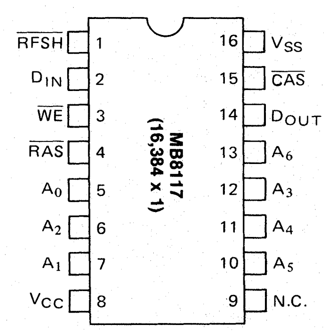


PLASTIC PACKAGE
DIP-16P-M01

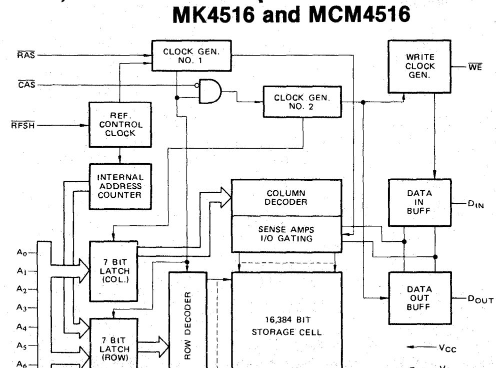
FEATURES

- **16,384 x 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS single-transistor cell**
- **Address access time**
  100 ns max (MB8117-10)
  120 ns max (MB8117-12)
- **Cycle time,**
  235 ns min (MB8117-10)
  270 ns min (MB8117-12)
- **Low power:**
  182 mW max (MB8117-10)
  160 mW max (MB8117-12)
  19.5 mW max (Standby)
- **+5V single power supply, ±10% tolerance**
- **On-chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Pin 1 auto refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Address and Data-in**
- **Offers two variations of hidden refresh**
- **Pin compatible with MK4516 and MCM4516**

PIN ASSIGNMENT



MB8117 BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage high than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} pin relative to V_{SS}		V_{CC}	−1 to +7	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operational should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25 °C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 ~ A_6, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{RFSH}}$	C_{IN2}	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	7	pF

STATIC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB8117-10		MB8117-12		Unit
			Min	Max	Min	Max	
OPERATING CURRENT Average Power Supply Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling; t_{RC} = Min)	1	I_{CC1}	—	33	—	29	mA
STANDBY CURRENT Power Supply Current ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{IH}, D_{OUT} = High Impedance)		I_{CC2}	—	3.5	—	3.5	mA
REFRESH CURRENT 1 Average Power Supply Current ($\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V_{IH}; t_{RC} = Min)	1	I_{CC3}	—	25	—	22	mA
PAGE MODE CURRENT Average Power Supply Current[1] ($\overline{\text{RAS}}$ = V_{IL}, $\overline{\text{CAS}}$ cycling, t_{PC} = Min)	1	I_{CC4}	—	25	—	22	mA
REFRESH CURRENT 2 Average Power Supply Current ($\overline{\text{RFSH}}$ cycling, $\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{IH}; t_{FC} = Min)	1	I_{CC5}	—	28	—	25	mA
INPUT LEAKAGE CURRENT Current, any input (0V ≤ V_{IN} ≤ 5.5V) Input pins not under test = 0V, 4.5V ≤ V_{CC} ≤ 5.5V, V_{SS} = 0V		I_{IL}	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V < V_{OUT} < 5.5V		I_{OL}	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	—	0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5 mA)		V_{OH}	2.4	—	2.4	—	V

Notes: 1 I_{CC} is dependent on output loading. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS NOTES 1, 2, 3

(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 8117-10		MB 8117-12		Unit
			Min	Max	Min	Max	
Time Between Refresh		t_{REF}	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	235	—	270	—	ns
Read-Write Cycle Time		t_{RWC}	285	—	320	—	ns
Page Mode Cycle Time		t_{PC}	125	—	145	—	ns
Access Time from $\overline{\text{RAS}}$	4 5	t_{RAC}	—	100	—	120	ns
Access Time from $\overline{\text{CAS}}$	5 6	t_{CAC}	—	55	—	65	ns
Output Buffer Turn Off Delay		t_{OFF}	0	45	0	50	ns
Transition Time		t_T	3	50	3	50	ns
$\overline{\text{RAS}}$ Precharge Time		t_{RP}	110	—	120	—	ns
$\overline{\text{RAS}}$ Pulse Width		t_{RAS}	115	10000	140	10000	ns
$\overline{\text{RAS}}$ Hold Time		t_{RSH}	70	—	85	--	ns
$\overline{\text{CAS}}$ Prechange Time (all cycles except page mode)		t_{CPN}	50	—	55	—	ns
$\overline{\text{CAS}}$ Precharge Time (Page mode only)		t_{CP}	60	—	70	—	ns
$\overline{\text{CAS}}$ Pulse Width		t_{CAS}	55	10000	65	10000	ns
$\overline{\text{CAS}}$ Hold Time		t_{CSH}	100	—	120	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	7 8	t_{RCD}	25	45	25	55	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t_{CRP}	0	—	0	—	ns
Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	15	—	15	—	ns
Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	15	—	15	—	ns
Column Address Hold Time Referenced to $\overline{\text{RAS}}$		t_{AR}	60	—	70	—	ns
Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
Read Command Hold Time		t_{RCH}	0	—	0	—	ns
Write Command Set Up Time	9	t_{WCS}	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	30	—	35	—	ns
Write Command Hold Time Referenced to $\overline{\text{RAS}}$		t_{WCR}	75	—	90	—	ns
Write Command Pulse Width		t_{WP}	30	—	35	—	ns
Write Command to $\overline{\text{RAS}}$ Lead Time		t_{RWL}	60	—	65	—	ns
Write Command to $\overline{\text{CAS}}$ Lead Time		t_{CWL}	45	—	50	—	ns
Data In Set Up Time		t_{DS}	0	—	0	—	ns
Data In Hold Time		t_{DH}	30	—	35	—	ns
Data In Hold Time Referenced to $\overline{\text{RAS}}$		t_{DHR}	75	—	90	—	ns
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	9	t_{CWD}	55	—	65	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	9	t_{RWD}	100	—	120	—	ns
Read Command Hold Time Referenced to $\overline{\text{RAS}}$		t_{RRH}	20	—	25	—	ns
$\overline{\text{RFSH}}$ Set Up Time Referenced to $\overline{\text{RAS}}$		t_{FSR}	110	—	120	—	ns
RAS to $\overline{\text{RFSH}}$ Delay		t_{RFD}	110	—	120	—	ns
$\overline{\text{RFSH}}$ Cycle Time		t_{FC}	235	—	270	—	ns
$\overline{\text{RFSH}}$ Pulse Width		t_{FP}	100	—	120	—	ns
$\overline{\text{RFSH}}$ Hold Time Referenced to $\overline{\text{RAS}}$	10	t_{FHR}	0	—	0	—	ns
$\overline{\text{RFSH}}$ Precharge Time		t_{FI}	110	—	120	—	ns
$\overline{\text{RFSH}}$ to RAS Delay	10	t_{FRD}	55	—	65	—	ns

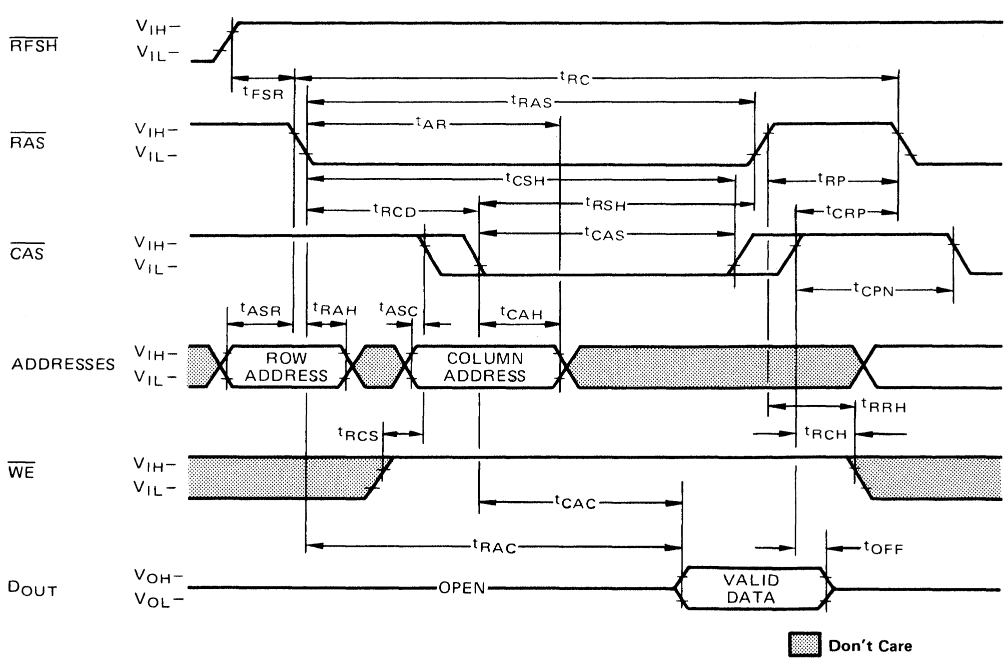
Notes:

1. An initial pause of 200µs is required. Then several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

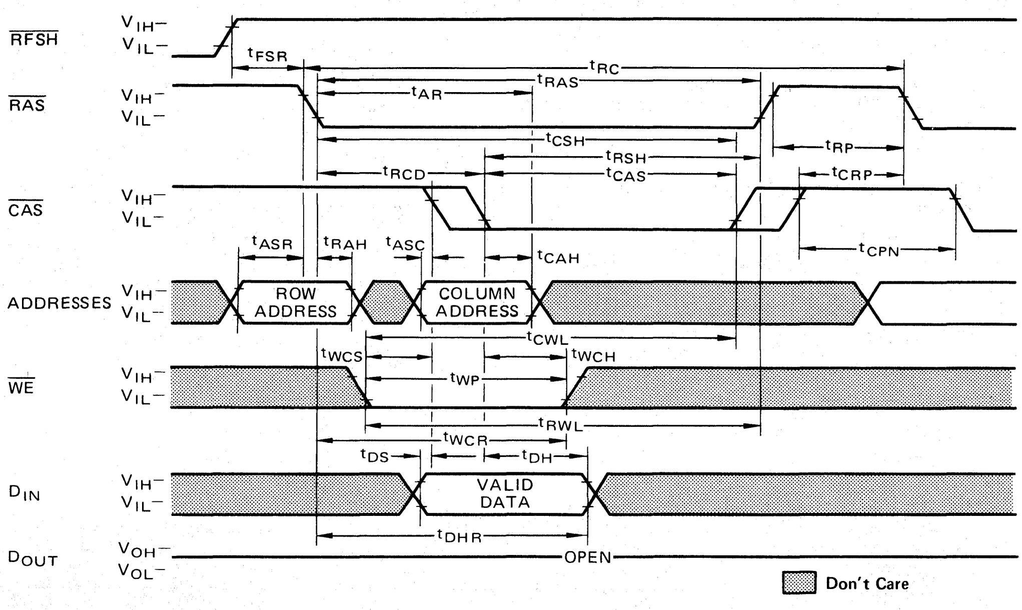
   If internal refresh counter is to be effective, a minimum of 64 active $\overline{RFSH}$ initialization cycles is required. The internal refresh counter must be activated a minimum of 128 times every 2 ms if the $\overline{RFSH}$ refresh function is used.

   Besides $\overline{RFSH}$ must be held high even if the $\overline{RFSH}$ refresh function is not used.
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} < t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} > t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. $t_{RAC}(min) = t_{RAH}(min) + 2t_T + t_{ASC}(min)$.
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} > t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Test mode write cycle only.

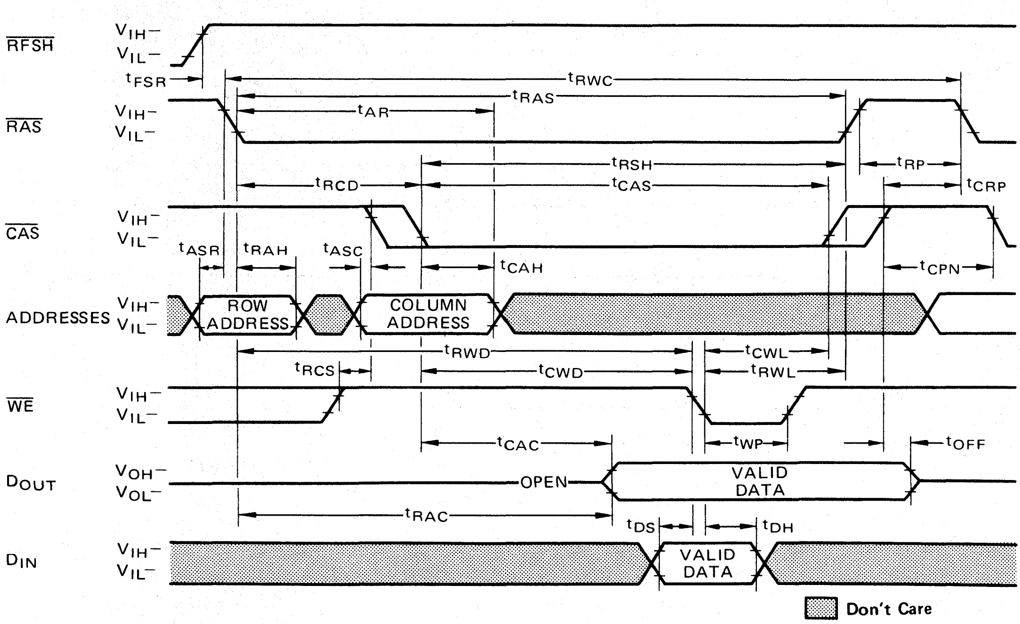
READ CYCLE



WRITE CYCLE (EARLY WRITE)

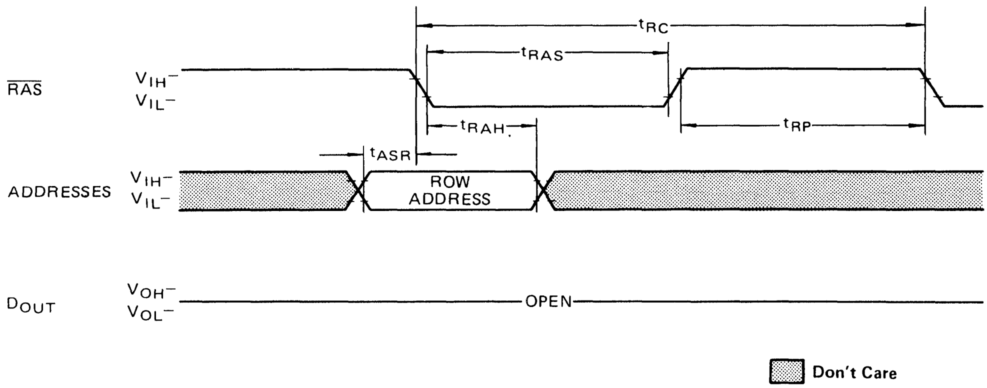


READ-WRITE/READ-MODIFY-WRITE CYCLE

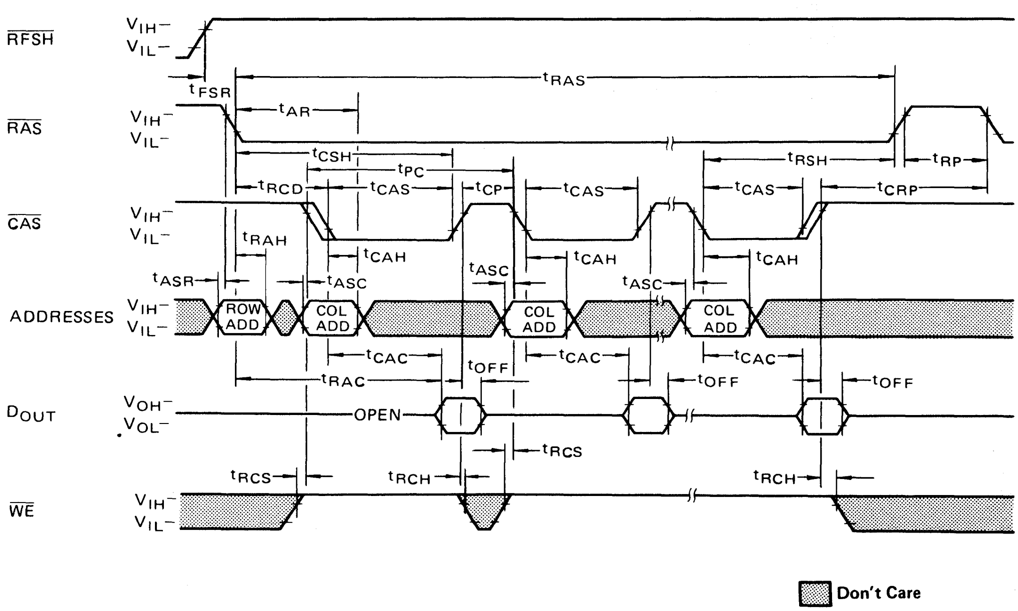


RAS-ONLY REFRESH CYCLE

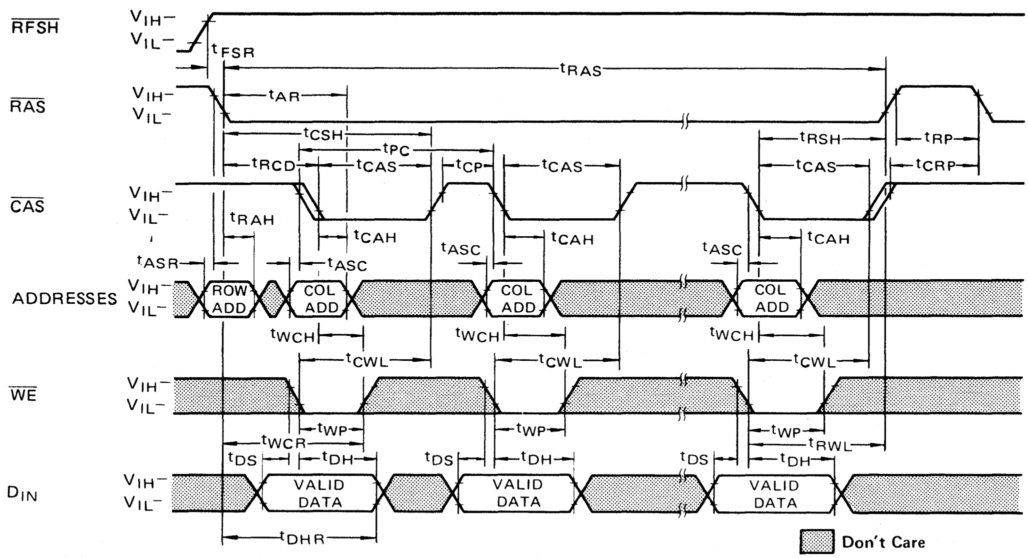
Note: RFSH = V_{IH}, CAS = V_{IH}, WE = Don't Care



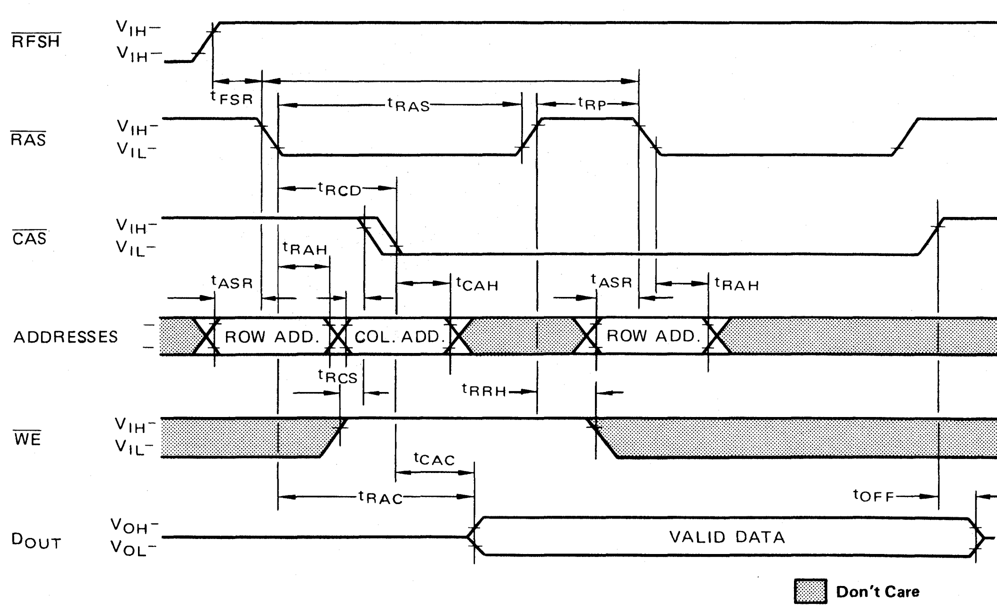
PAGE-MODE READ CYCLE



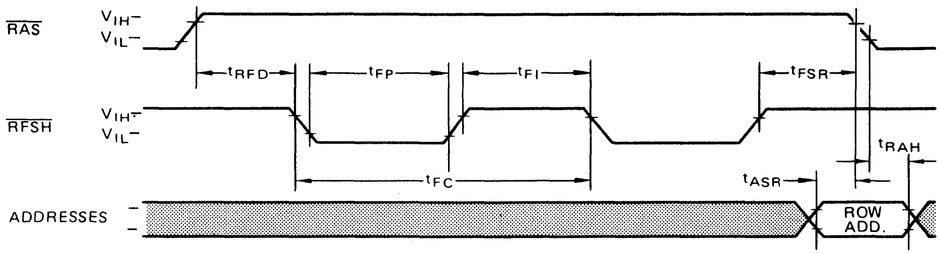
PAGE-MODE WRITE CYCLE



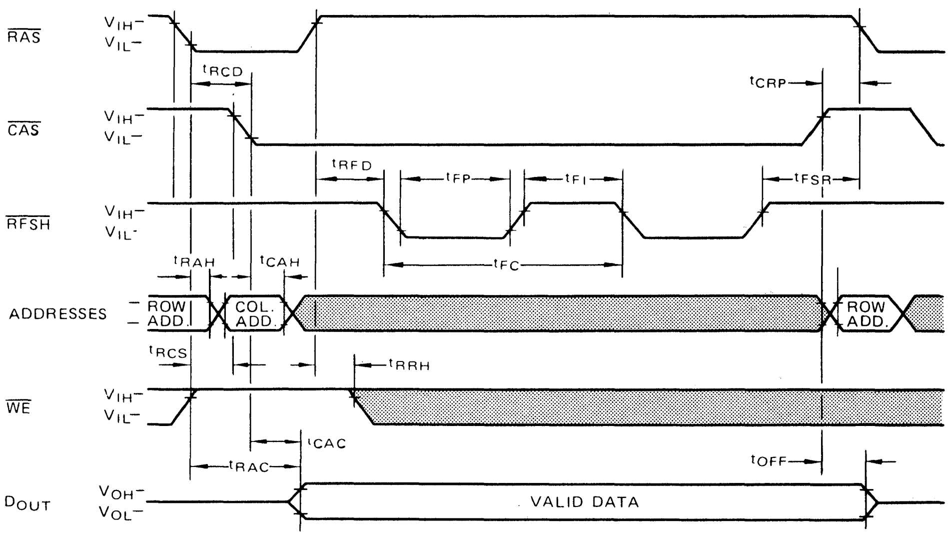
HIDDEN $\overline{\text{RAS}}$-ONLY REFRESH CYCLE



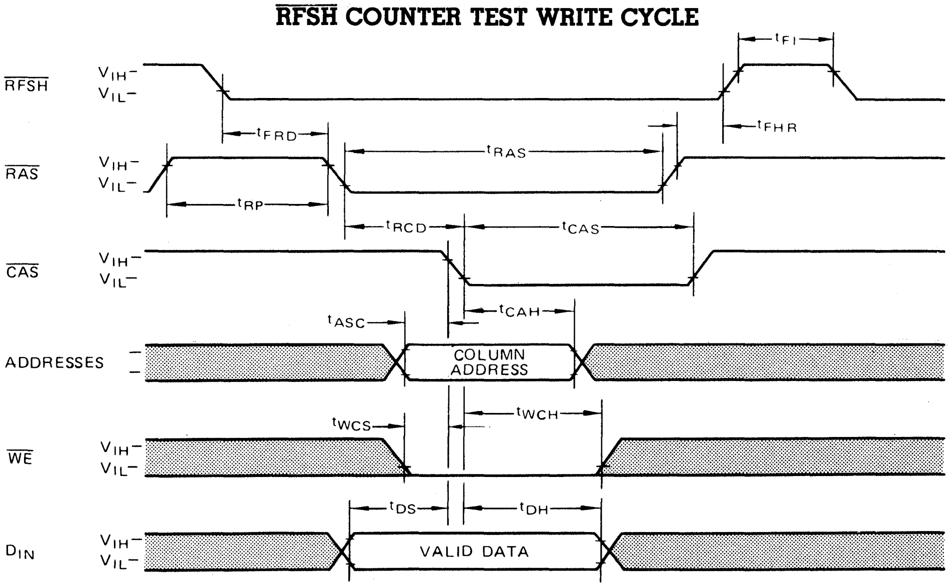
$\overline{RFSH}$ REFRESH CYCLE



HIDDEN $\overline{RFSH}$ REFRESH CYCLE



$\overline{RFSH}$ COUNTER TEST WRITE CYCLE



Don't Care

DESCRIPTION

Address Inputs

A total of fourteen binary input address bits are required to decode any 1 of 16,384 storage cell locations within the MB8117. Seven row-address bits are established on the input pins (A_0 through A_6) and latched with the Row Address Strobe ($\overline{RAS}$). Then seven column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode; logic "low" dictates write mode. Data input is disabled when read mode is selected. $\overline{WE}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input

Data written into the MB8117 during a write or read-write cycle. The last falling-edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits strobing the row-address into the MB8117 while maintaining $\overline{RAS}$ at a logic "low" throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory cell is accomplished by performing a memory cycle at each of the 128 row-addresses at least every two milliseconds. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{RFSH}$ Refresh

$\overline{RFSH}$ type refreshing available on the MB8117 offers an alternate refresh method. When $\overline{RFSH}$ (Pin 1) is brought low and $\overline{RAS}$ is inactive, on-chip refresh control clock generators and a refresh address counter are enabled and an internal refresh operation takes place. When $\overline{RFSH}$ is brought high (inactive) the internal refresh address counter is automatically incremented in preparation for the next $\overline{RFSH}$ cycle. Only $\overline{RFSH}$ activated cycles affect the internal refresh address counter. The use of $\overline{RFSH}$ type refreshing eliminates the need of providing additional external devices to generate refresh addresses.

Hidden Refresh

Hidden Refresh Cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle.

The MB8117 offers two types of Hidden Refresh. They are referred to as Hidden $\overline{RAS}$-Only Refresh and Hidden $\overline{RFSH}$ Refresh.

1) Hidden $\overline{RAS}$-Only Refresh
Hidden $\overline{RAS}$-Only Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing "$\overline{RAS}$-Only" refresh, but with $\overline{CAS}$ held low. $\overline{RFSH}$ has to be held at V_{IH}.

2) Hidden $\overline{RFSH}$ Refresh
Hidden $\overline{RFSH}$ Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RFD}), executing $\overline{RFSH}$ refresh, but with $\overline{CAS}$ held low.

A specified precharge period (t_{CPN}) is required before normal memory Read, Write or Read-Modify-Write cycle after performing either type of Hidden Refresh.

$\overline{RFSH}$ (PIN 1) TEST CYCLE

A special timing sequence using the PIN 1 counter test cycle provides a convenient method of verifying the functionality of the $\overline{RFSH}$ activated circuitry.

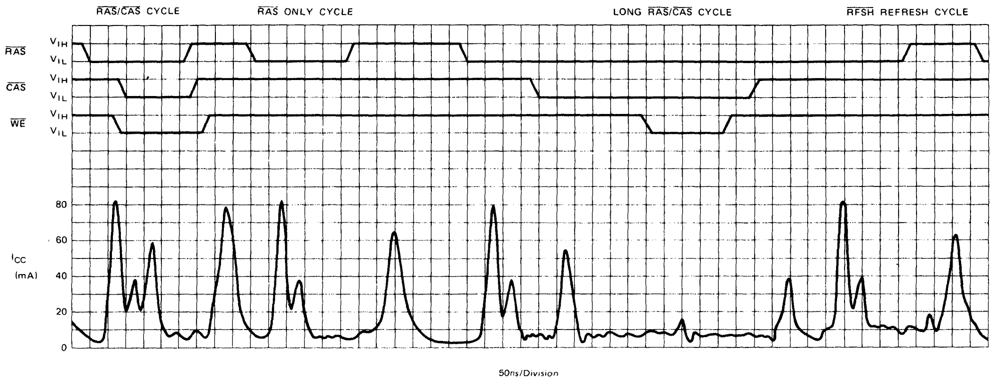
When $\overline{RFSH}$ is activated prior to and remains valid through a normal write cycle, the D_{IN} is written into the memory location defined by the current contents of the on-chip refresh counter and the column address present at the external address pins during the high-to-low transition of $\overline{CAS}$. (See PIN 1 counter test write timing diagram.)

The following test procedure may be used to verify the functionality of the internal refresh counter. There are a multitude of patterns and sequences which may also be used to verify the $\overline{RFSH}$ feature. This test should be performed after it has been confirmed that the device can uniquely address all 16,384 storage locations.

SUGGESTED $\overline{RFSH}$ COUNTER TEST PROCEDURE

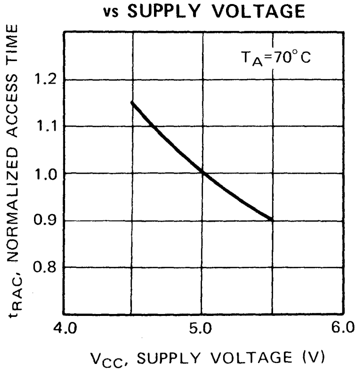
1. Initialize the on-chip refresh counter. 64 cycles are adequate for this purpose.
2. Write a test pattern of zeroes into the memory at a single column address and all row addresses by using 128 $\overline{RFSH}$ (pin 1) refresh counter test write cycles.
3. Verify the data written into the RAM by using the column address used in step 2 and sequence through all row address combinations by using conventional read cycles.
4. Compliment the test pattern and repeat steps 2 and 3.

CURRENT WAVEFORMS (V_{CC} = 5.0V, T_A = 25°C)

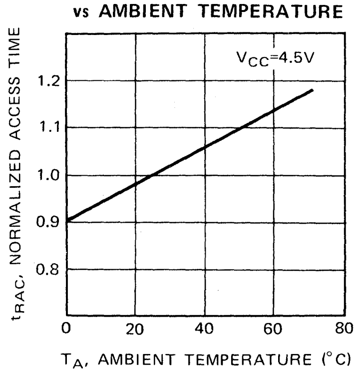


TYPICAL CHARACTERISTICS CURVES

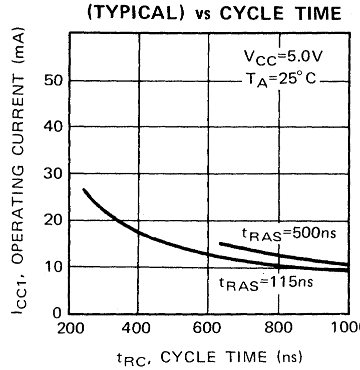
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



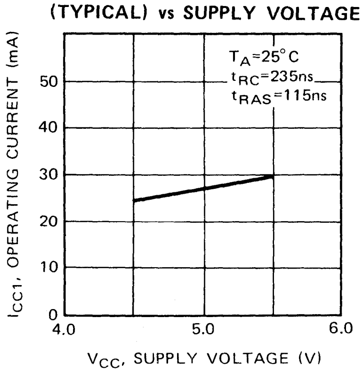
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



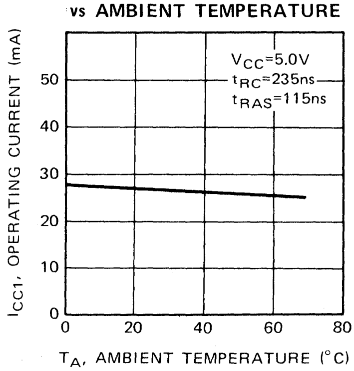
OPERATING CURRENT (TYPICAL) vs CYCLE TIME



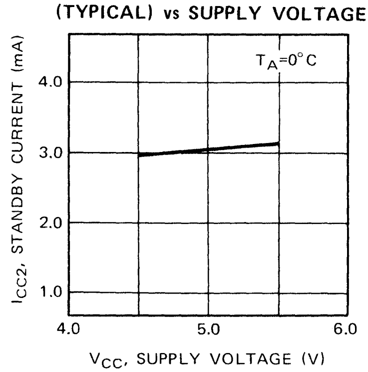
OPERATING CURRENT (TYPICAL) vs SUPPLY VOLTAGE



OPERATING CURRENT (TYPICAL) vs AMBIENT TEMPERATURE

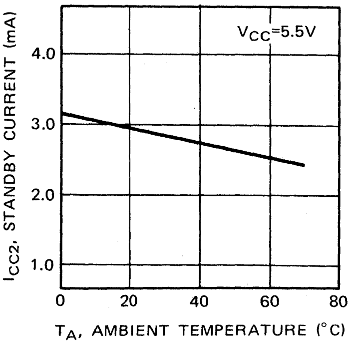


STANDBY CURRENT (TYPICAL) vs SUPPLY VOLTAGE

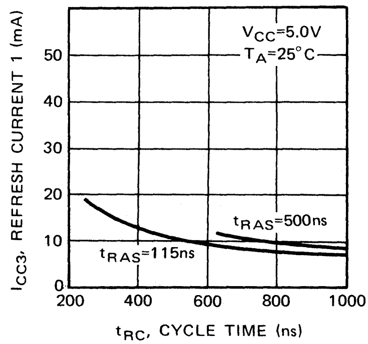


TYPICAL CHARACTERISTICS CURVES. (Continued)

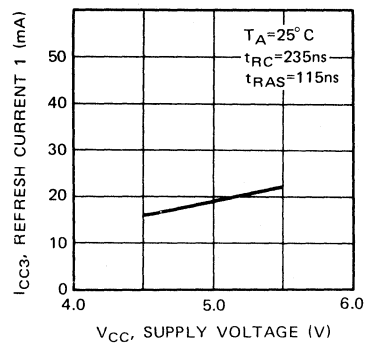
STANDBY CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



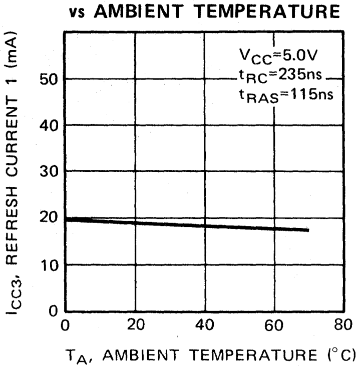
REFRESH CURRENT 1 (TYPICAL) vs CYCLE TIME



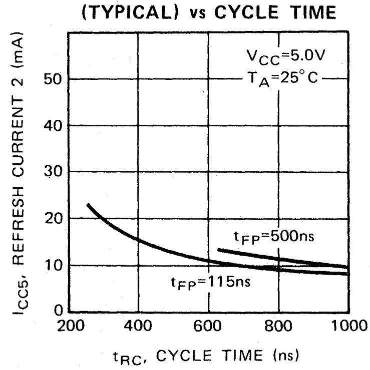
REFRESH CURRENT 1 (TYPICAL) vs SUPPLY VOLTAGE



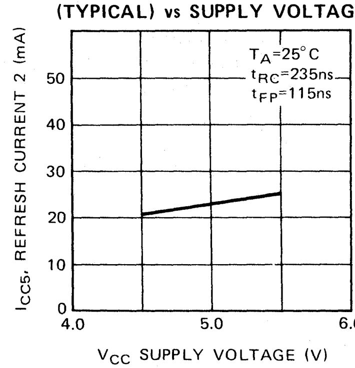
REFRESH CURRENT 1 (TYPICAL) vs AMBIENT TEMPERATURE



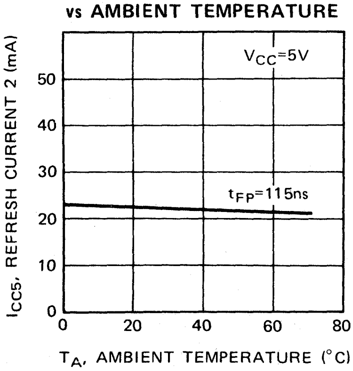
REFRESH CURRENT 2 (TYPICAL) vs CYCLE TIME



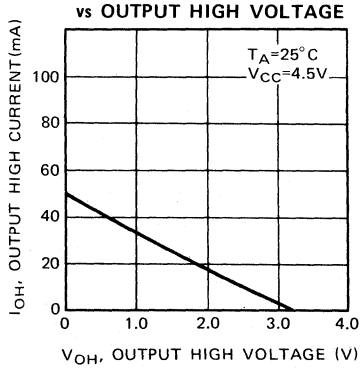
REFRESH CURRENT 2 (TYPICAL) vs SUPPLY VOLTAGE



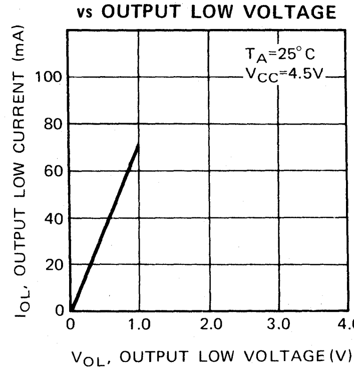
REFRESH CURRENT 2 (TYPICAL) vs AMBIENT TEMPERATURE



OUTPUT HIGH CURRENT vs OUTPUT HIGH VOLTAGE

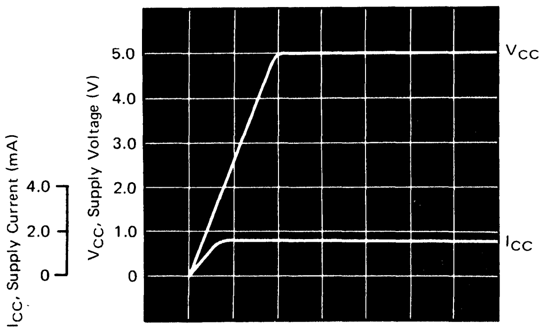


OUTPUT LOW CURRENT vs OUTPUT LOW VOLTAGE



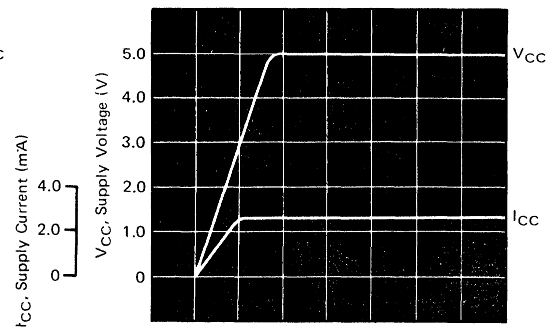
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP

1) $\overline{RAS} = V_{IL}$, $\overline{CAS} = V_{IL}$



500μs/Division

2) $\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IH}$



500μs/Division

FUJITSU
MICROELECTRONICS, INC.

MB8118-10
MB8118-12

NMOS 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

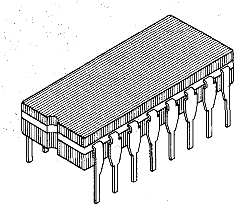
DESCRIPTION

The Fujitsu MB8118 is a fully decoded dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory peripheral storage and environments where low power dissipation and compact layout are required.

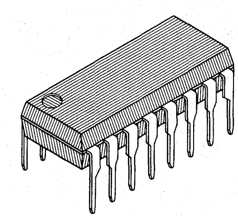
Multiplexed row and column address inputs permit the MB8118 to be housed in a standard 16-pin DIP. Pin outs conform to the JEDEC approved pin out.

The MB8118 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible; the output is three-state TTL.



CERDIP PACKAGE
DIP-16C-C03

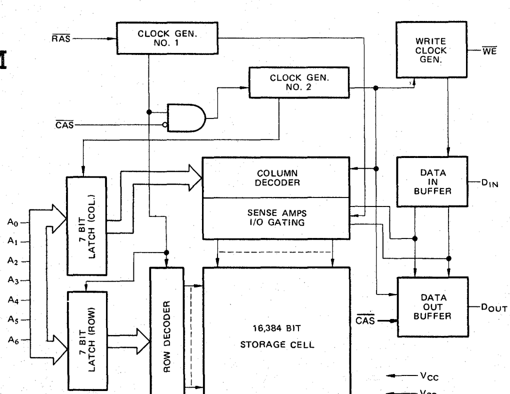


PLASTIC PACKAGE
DIP-16P-M01

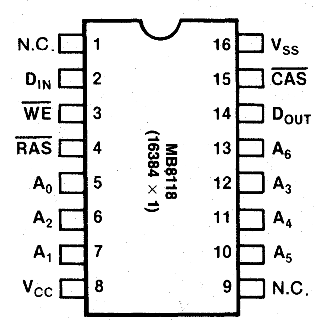
FEATURES

- **16,384 × 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Address access time:**
  100 ns max (MB8118-10)
  120 ns max (MB8118-12)
- **Cycle time:**
  235 ns min (MB8118-10)
  270 ns min (MB8118-12)
- **Low power:**
  182mW max (MB8118-10)
  160mW max (MB8118-12)
  16.5mW max (Standby)
- **+5V single power supply, ±10% tolerance**
- **On chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Hidden refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{\text{RAS}}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-in**
- **Pin compatible with Intel 2118 and MCM4517**

MB8118 BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} pin relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Cerdip	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance $A_0 \sim A_6$, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10		MB8118-12		Unit
			Min	Max	Min	Max	
OPERATING CURRENT Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min)	1	I_{CC1}	—	33	—	29	mA
STANDBY CURRENT Average Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, D_{OUT} = High Impedance)		I_{CC2}	—	3.0	—	3.0	mA
REFRESH CURRENT Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min)	1	I_{CC3}	—	25	—	22	mA
PAGE MODE CURRENT Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min)	1	I_{CC4}	—	25	—	22	mA
INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 5.5) Input pins not under test = 0V, 4.5V ≤ V_{CC} ≤ 5.5V, V_{SS} = 0V		I_{IL}	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	—	0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5 mA)		V_{OH}	2.4	—	2.4	—	V

Note: 1 I_{CC} is dependent on output loading. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS NOTES 1,2,3

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10			MB8118-12			Unit
			Min	Typ	Max	Min	Typ	Max	
Time Between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	235	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	285	—	—	320	—	—	ns
Page Mode Cycle Time		t_{PC}	125	—	—	145	—	—	ns
Access Time from $\overline{RAS}$	[4] [6]	t_{RAC}	—	—	100	—	—	120	ns
Access Time from $\overline{CAS}$	[5] [6]	t_{CAC}	—	—	55	—	—	65	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	45	0	—	50	ns
Transition Time		t_T	3	—	50	3	—	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	110	—	—	120	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	115	—	10000	140	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	70	—	—	85	—	—	ns
$\overline{CAS}$ Prechange Time (all cycles except page mode)		t_{CPN}	50	—	—	55	—	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	60	—	—	70	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	—	10000	65	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100	—	—	120	—	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	[7] [8]	t_{RCD}	25	—	45	25	—	55	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	15	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	15	—	—	15	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	60	—	—	70	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time		t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	[9]	t_{WCS}	0	—	—	0	—	—	ns
Write Command Hold Time		t_{WCH}	30	—	—	35	—	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	75	—	—	90	—	—	ns
Write Command Pulse Width		t_{WP}	30	—	—	35	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	60	—	—	65	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	45	—	—	50	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	30	—	—	35	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	75	—	—	90	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	[9]	t_{CWD}	55	—	—	65	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	[9]	t_{RWD}	100	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	20	—	—	25	—	—	ns

Notes:

[1] An initial pause of 200μs is required. Then several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

[2] Dynamic measurements assume t_T=5ns.

[3] V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

[4] Assumes that $t_{RCD} < t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

[5] Assumes that $t_{RCD} > t_{RCD}$ (max).

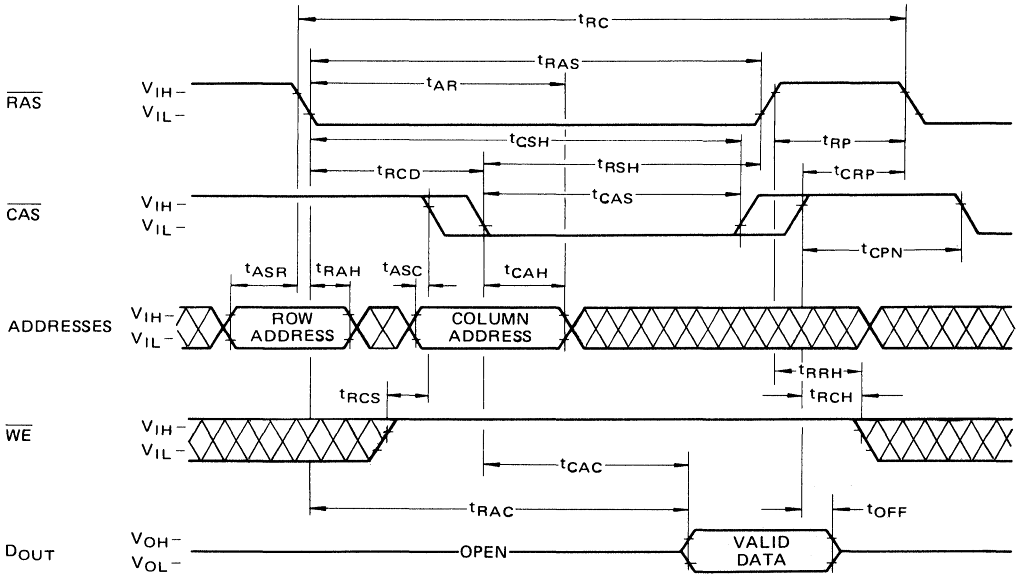
[6] Measured with a load equivalent to 2 TTL loads and 100pF.

[7] Operation within the t_{RCD} (max) limit insures that t_{RCD} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

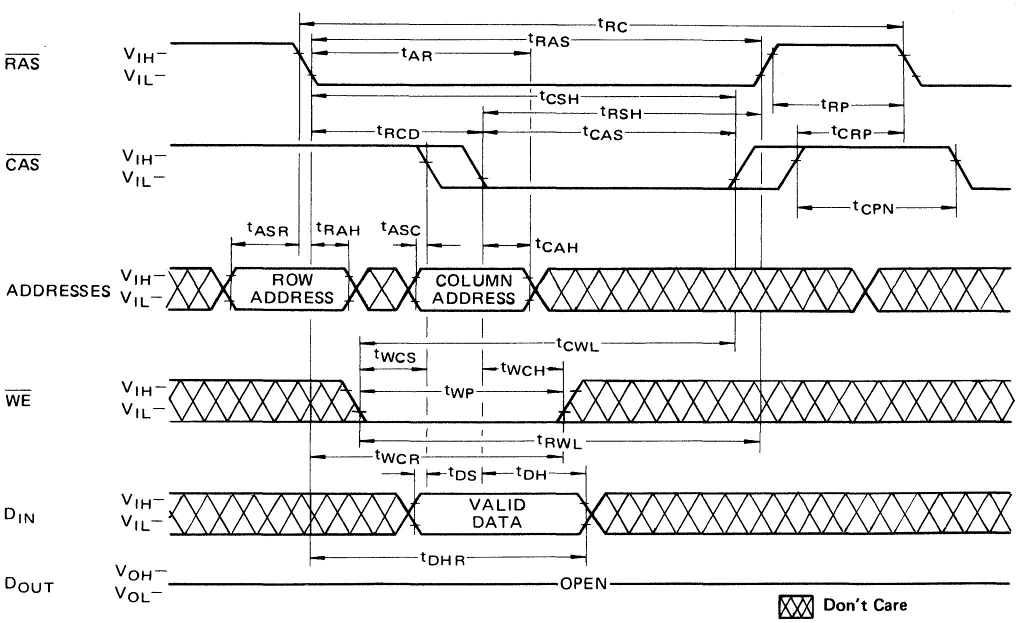
[8] $t_{RCD}(min) = t_{RAH}(min) + 2t_T (t_T = 5ns) + t_{ASC}(min)$.

[9] t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} > t_{CWD}$ (min) and $t_{RWD} > t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

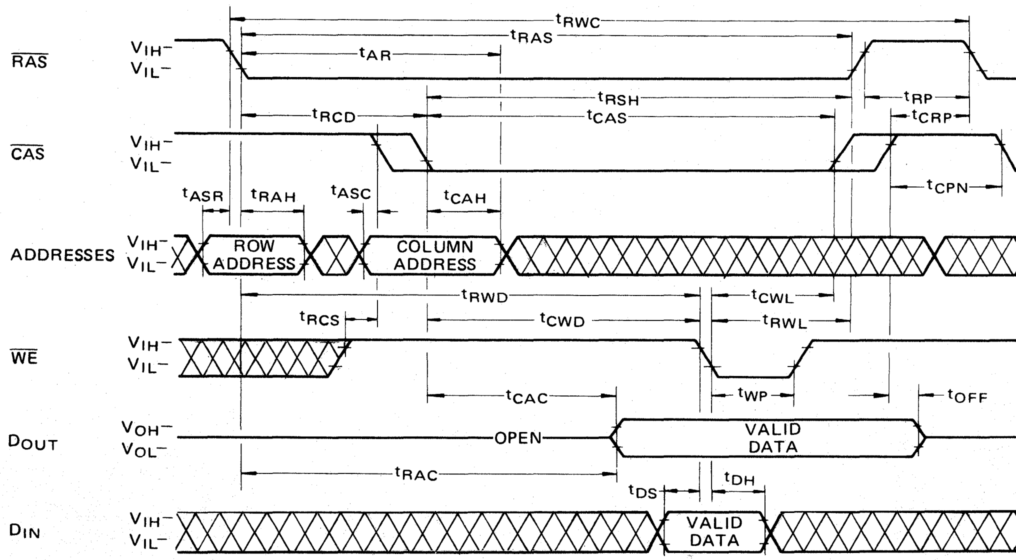
READ CYCLE



WRITE CYCLE (EARLY WRITE)

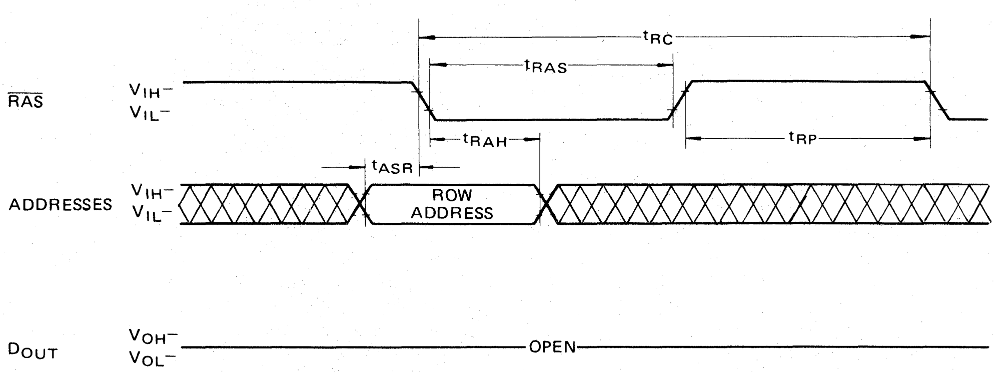


READ-WRITE/READ-MODIFY-WRITE CYCLE



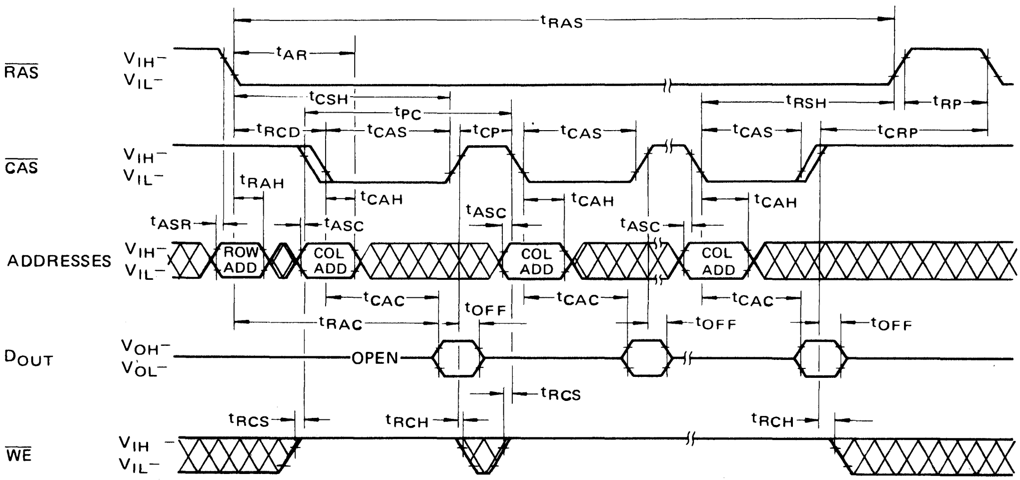
"RAS-ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't care

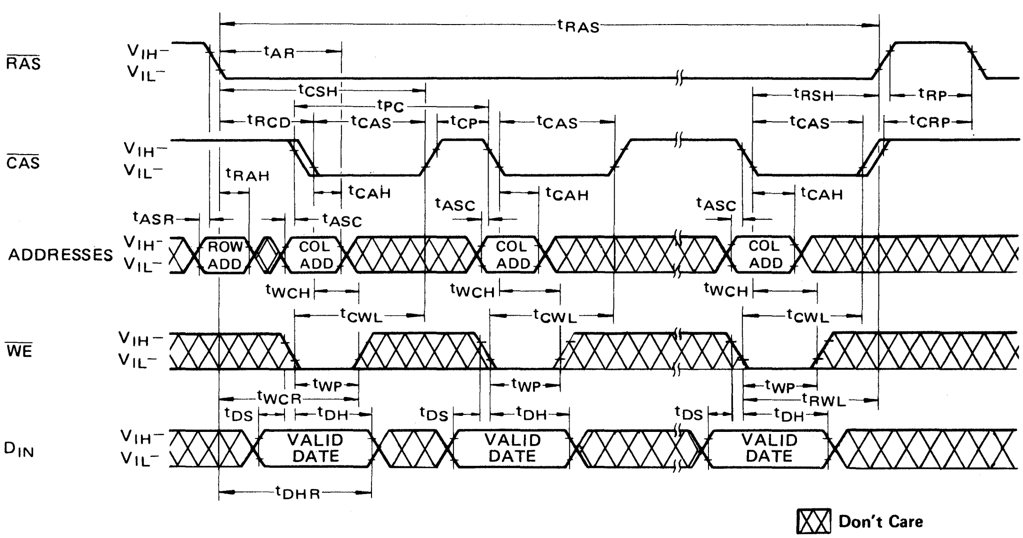


Don't Care

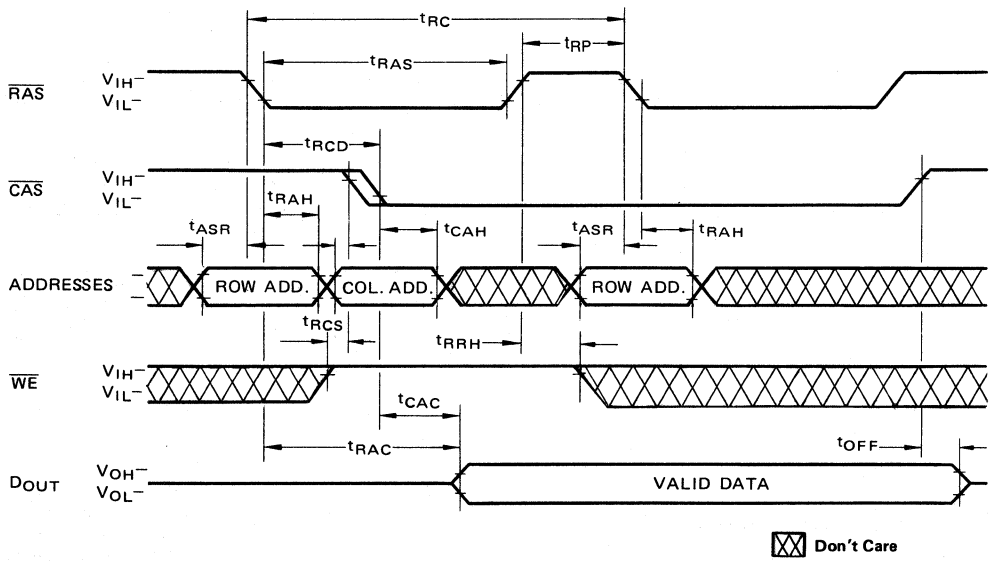
PAGE-MODE READ CYCLE



PAGE-MODE WRITE CYCLE



HIDDEN $\overline{\text{RAS}}$-ONLY REFRESH CYCLE



DESCRIPTION

Address Inputs

A total of fourteen binary input address bits are required to decode any one of 16,384 storage cell locations within the MB8118. Seven row-address bits are established on the input pins (A_0 through A_6) and latched with the Row Address Strobe ($\overline{\text{RAS}}$). Seven column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{\text{CAS}}$). All input addresses must be stable on or before the falling edge of $\overline{\text{RAS}}$. $\overline{\text{CAS}}$ is internally inhibited (or "gated") by $\overline{\text{RAS}}$ to permit triggering of $\overline{\text{CAS}}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{\text{WE}}$ input. A logic "high" on $\overline{\text{WE}}$ dictates read mode; logic "low" dictates write mode. Data input is disabled when read mode is selected. $\overline{\text{WE}}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input:

Data is written into the MB8118 during a write or read-write cycle. The last falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{\text{WE}}$ is brought low (write mode) before $\overline{\text{CAS}}$, D_{IN} is strobed by $\overline{\text{CAS}}$, and the set-up and hold times are referenced to $\overline{\text{CAS}}$. In a read-write cycle, $\overline{\text{WE}}$ will be delayed until $\overline{\text{CAS}}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{\text{WE}}$, and set-up and hold times are referenced to $\overline{\text{WE}}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{\text{CAS}}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{\text{RAS}}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{\text{CAS}}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{\text{CAS}}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits latching the row-address into the MB8118 and maintaining $\overline{\text{RAS}}$ at a logic "low" throughout all successive memory operations in which the row-address doesn't change. This saves the power required by a $\overline{\text{RAS}}$ cycle. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{\text{RAS}}$-Only Refresh

Refresh of the dynamic memory is accomplished by performing a memory cycle at each of the 128 row-addresses at least every two milliseconds. $\overline{\text{RAS}}$-only refresh prevents any output during refresh because the output buffer is in the high impedance state since $\overline{\text{CAS}}$ is at V_{IH}. Strobing each of the 128 row-addresses with $\overline{\text{RAS}}$ will cause all bits in the memory to be refreshed. $\overline{\text{RAS}}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} from a previous memory read cycle. (See Figure 1 below)

FIG. 1 HIDDEN REFRESH

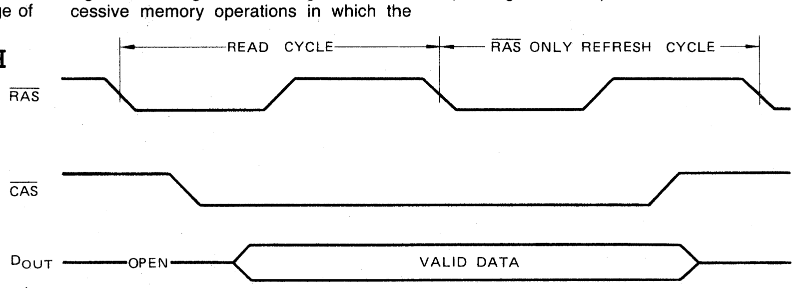
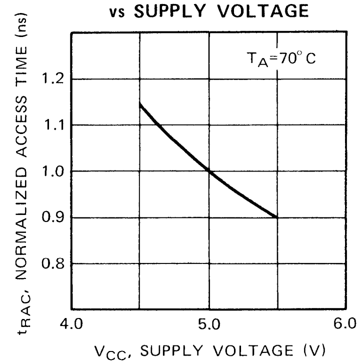


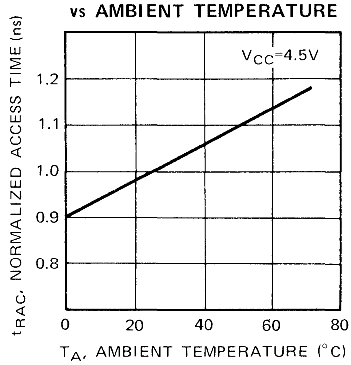
FIG. 2 — CURRENT WAVEFORMS (V_{CC} = 5.0V, T_A = 25°C)

TYPICAL CHARACTERISTICS CURVES

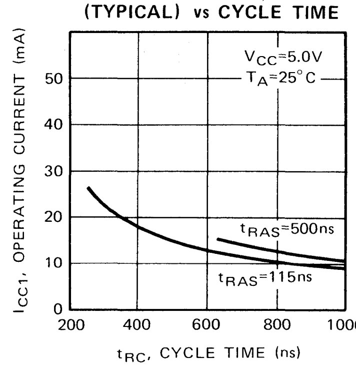
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



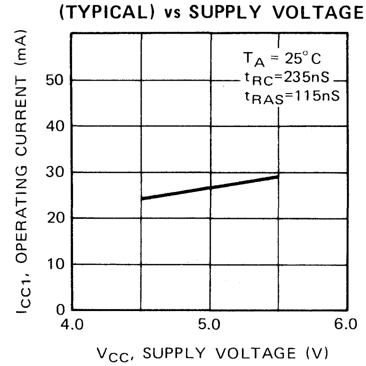
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



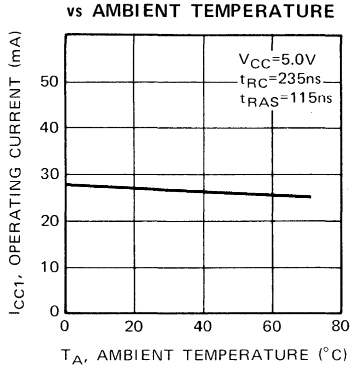
OPERATING CURRENT (TYPICAL) vs CYCLE TIME



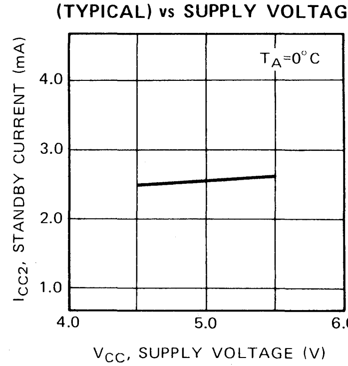
OPERATING CURRENT (TYPICAL) vs SUPPLY VOLTAGE



OPERATING CURRENT (TYPICAL) vs AMBIENT TEMPERATURE

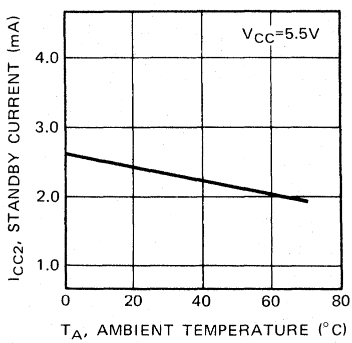


STANDBY CURRENT (TYPICAL) vs SUPPLY VOLTAGE

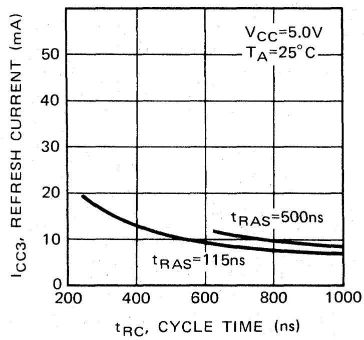


TYPICAL CHARACTERISTICS CURVES (continued)

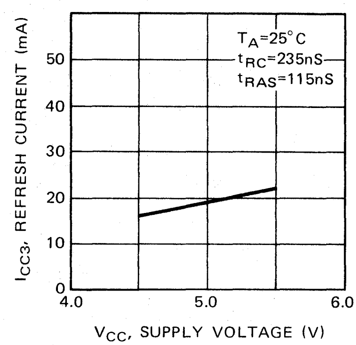
STANDBY CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



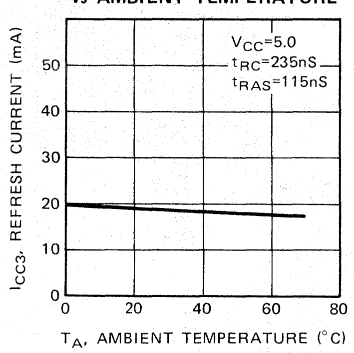
REFRESH CURRENT (TYPICAL) vs CYCLE TIME



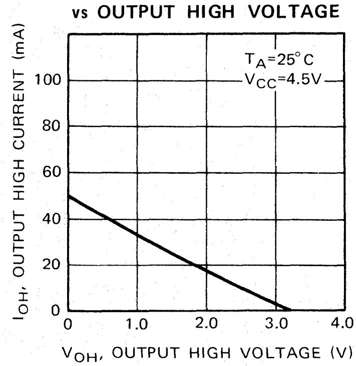
REFRESH CURRENT (TYPICAL) vs SUPPLY VOLTAGE



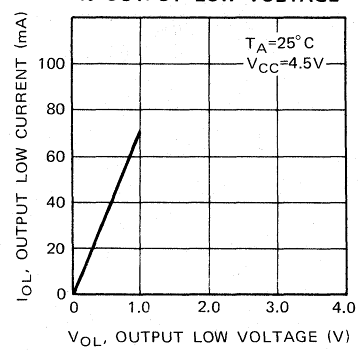
REFRESH CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



OUTPUT HIGH CURRENT vs OUTPUT HIGH VOLTAGE

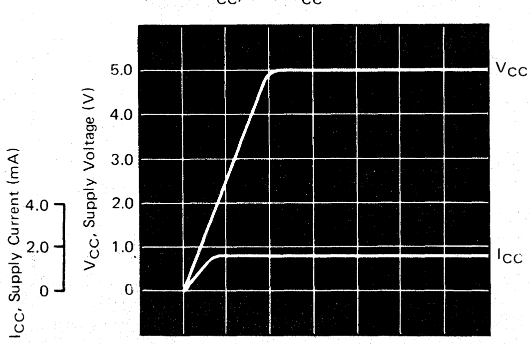


OUTPUT LOW CURRENT vs OUTPUT LOW VOLTAGE



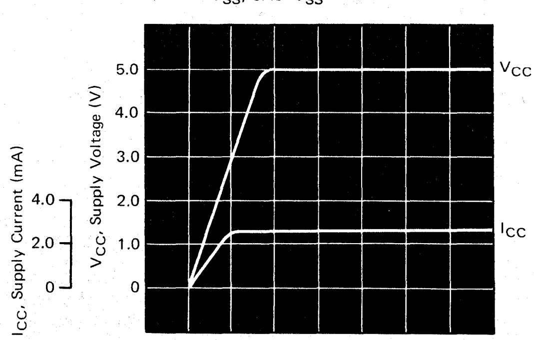
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP

1) $\overline{RAS}=V_{CC}$, $\overline{CAS}=V_{CC}$



500μs/Division

2) $\overline{RAS}=V_{SS}$, $\overline{CAS}=V_{SS}$



500μs/Division

FUJITSU
MICROELECTRONICS, INC.

MB8264-15
MB8264-20

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

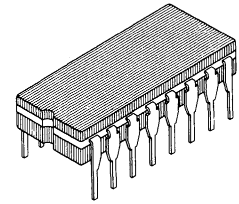
DESCRIPTION

The Fujitsu MB8264 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

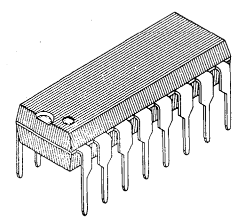
Multiplexed row and column address inputs permit the MB8264 to be housed in a standard 16-pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MB8264 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is ±10%. All inputs/outputs are TTL compatible.



CERAMIC PACKAGE
CERDIP
DIP-16C-C04

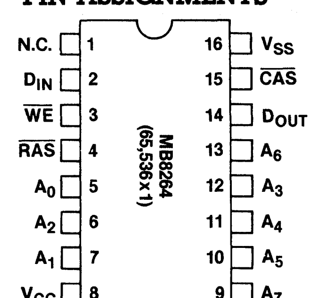


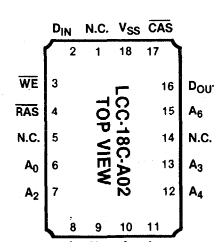
PLASTIC PACKAGE
DIP-16P-M03

FEATURES

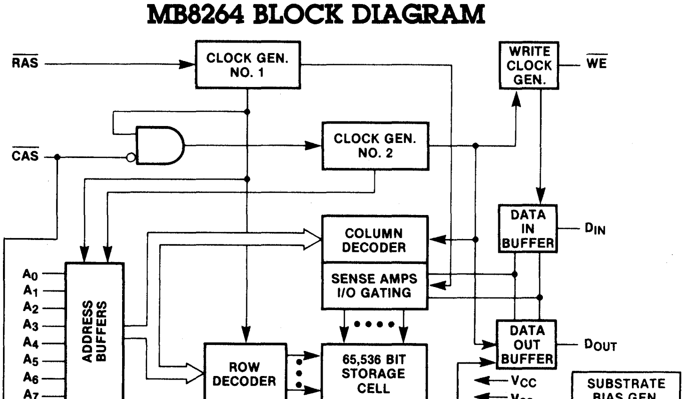
- **65,536 x 1 RAM, 16-pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Row access time:**
  150ns Max (MB8264-15)
  200ns Max (MB8264-20)
- **Cycle time:**
  270ns Min (MB8264-15)
  330ns Min (MB8264-20)
- **Low power:**
  22 mW Max Standby
  275 mW Max Active (MB8264-15)
  248 mW Max Active (MB8264-20)
- **±10% tolerance on +5V Supply**
- **On-chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **"Gated" $\overline{CAS}$**
- **128 refresh cycles**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-in**
- **Hidden Refresh Capability**
- **Pin compatible with HM4864, MK4164, TMS4164, MCM6665, μPD4164 and IMS2600**

PIN ASSIGNMENTS





MB8264 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7.0	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A_0 ~ A_7, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB8264-20	I_{CC1}		45	mA
	MB8264-15		—	50	mA
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	4	mA
REFRESH CURRENT* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min)	MB8264-20	I_{CC3}		36	mA
	MB8264-15		—	42	mA
PAGE MODE CURRENT * Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)		I_{CC4}	—	34	mA
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V) Input pins not under test = 0V, V_{CC} = 5.5V, V_{SS} = 0V		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
OUTPUT LEVEL Output low voltage (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V
OUTPUT LEVEL Output high voltage (I_{OH} = −5mA)		V_{OH}	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS Notes $\boxed{1,2,3}$

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8264-20 Min	MB8264-20 Typ	MB8264-20 Max	MB8264-15 Min	MB8264-15 Typ	MB8264-15 Max	Unit
Time between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	330	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	375	—	—	300	—	—	ns
Page Mode Cycle Time		t_{PC}	225	—	—	170	—	—	ns
Access Time from $\overline{RAS}$	$\boxed{4}$ $\boxed{6}$	t_{RAC}	—	—	200	—	—	150	ns
Access Time from $\overline{CAS}$	$\boxed{5}$ $\boxed{6}$	t_{CAC}	—	—	135	—	—	100	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	50	0	—	40	ns
Transition Time		t_T	3	—	50	3	—	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120	—	—	100	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	—	10000	150	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135	—	—	100	—	—	ns
$\overline{CAS}$ Precharge Time (Page Mode Only)		t_{CP}	80	—	—	60	—	—	ns
$\overline{CAS}$ Precharge Time (All Cycles Except Page Mode)		t_{CPN}	30	—	—	25	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	—	10000	100	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	200	—	—	150	—	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	$\boxed{7}$ $\boxed{8}$	t_{RCD}	30	—	65	25	—	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	20	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	55	—	—	45	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120	—	—	95	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time	$\boxed{10}$	t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	$\boxed{9}$	t_{WCS}	−10	—	—	−10	—	—	ns
Write Command Hold Time		t_{WCH}	55	—	—	45	—	—	ns
Write Command Hold Time Reference to $\overline{RAS}$		t_{WCR}	120	—	—	95	—	—	ns
Write Command Pulse Width		t_{WP}	55	—	—	45	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80	—	—	60	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80	—	—	60	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	55	—	—	45	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120	—	—	95	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	$\boxed{9}$	t_{CWD}	95	—	—	70	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	$\boxed{9}$	t_{RWD}	160	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	$\boxed{10}$	t_{RRH}	25	—	—	20	—	—	ns

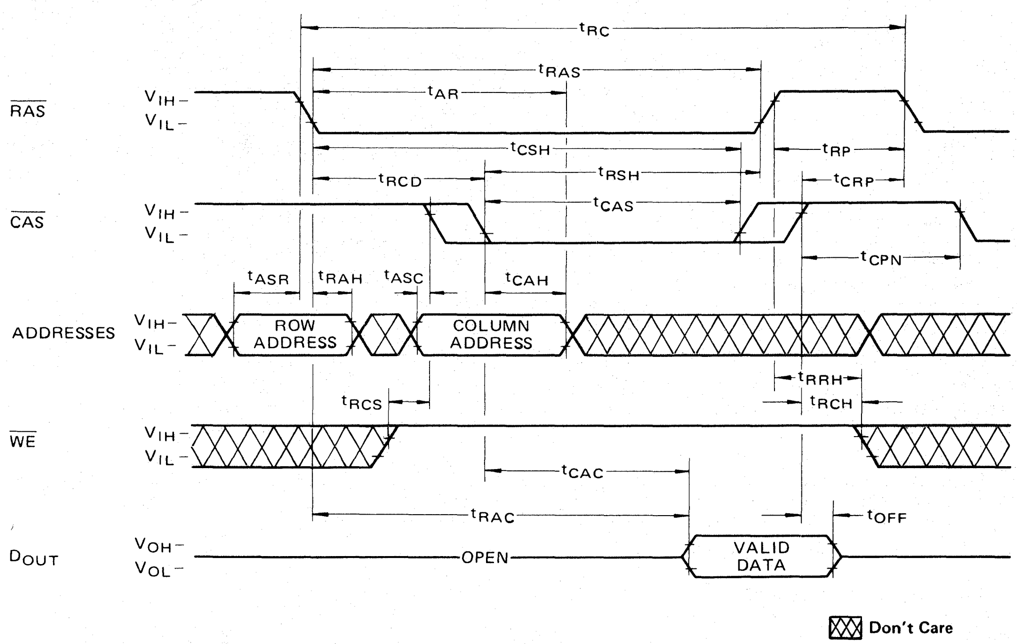
Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD}(min) = t_{RAH}(min) + $2t_T$(t_T = 5ns) + t_{ASC}(min).
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.

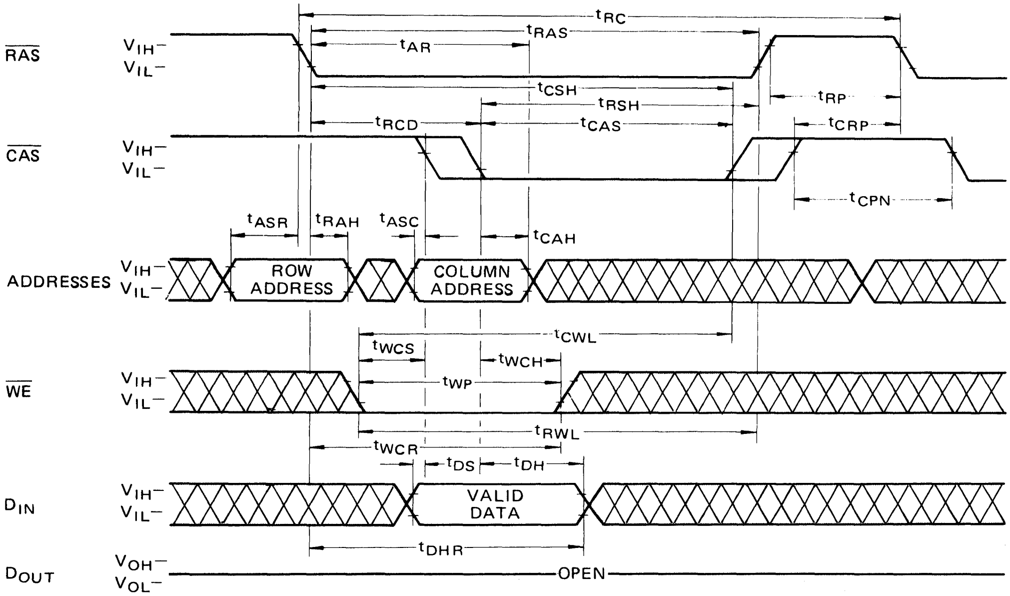
   If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

TIMING DIAGRAMS

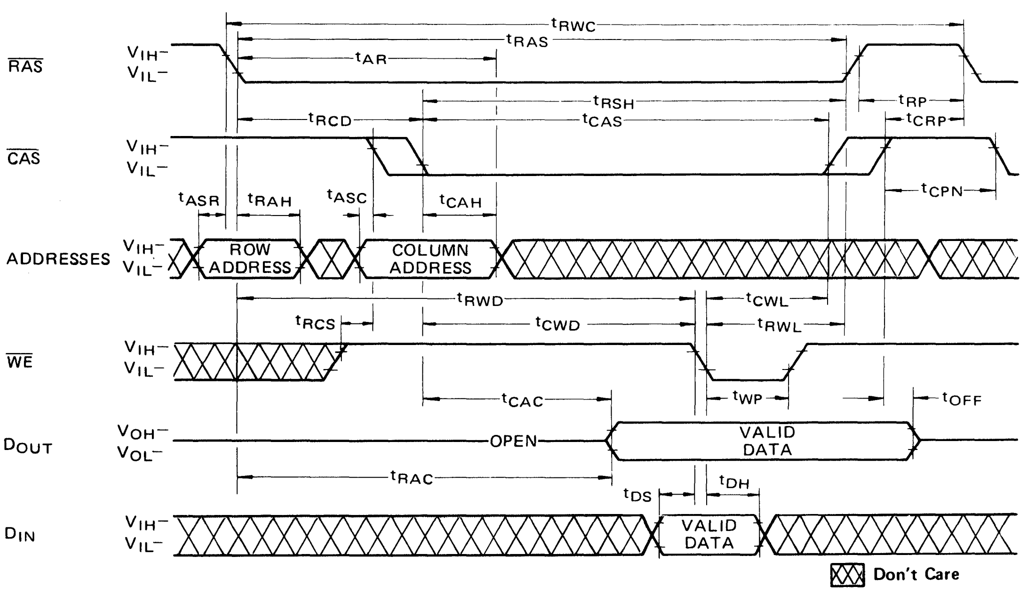
READ CYCLE



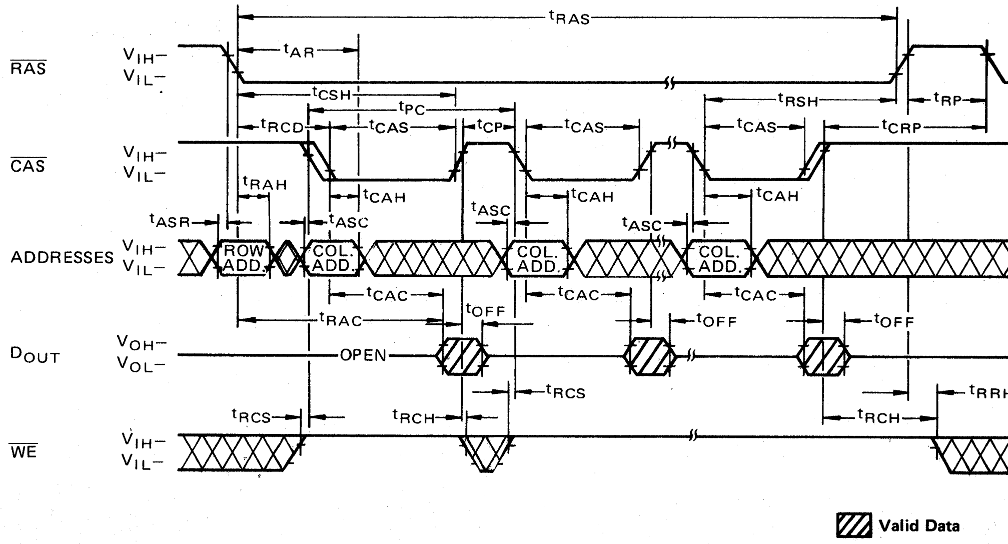
WRITE CYCLE (EARLY WRITE)



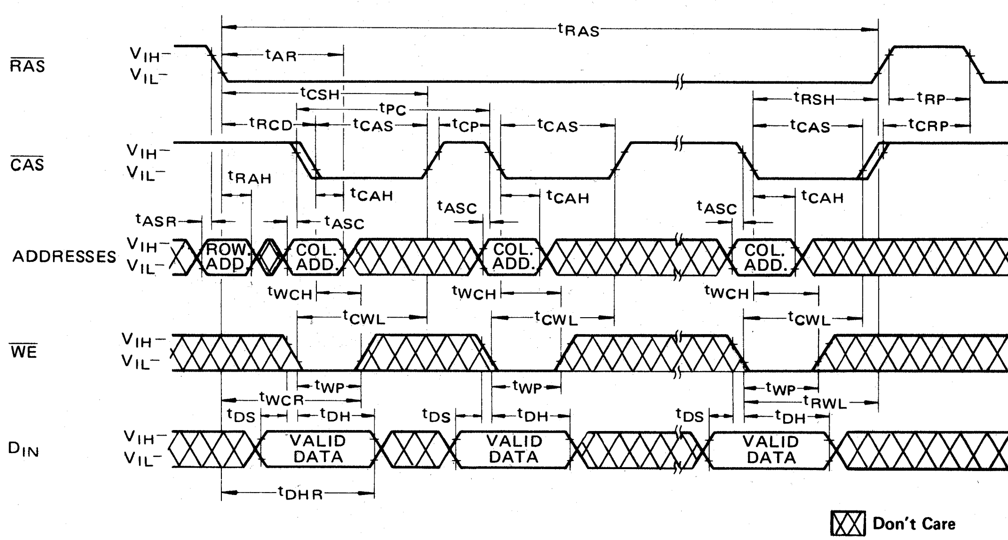
READ-WRITE/READ-MODIFY-WRITE CYCLE



PAGE-MODE READ CYCLE

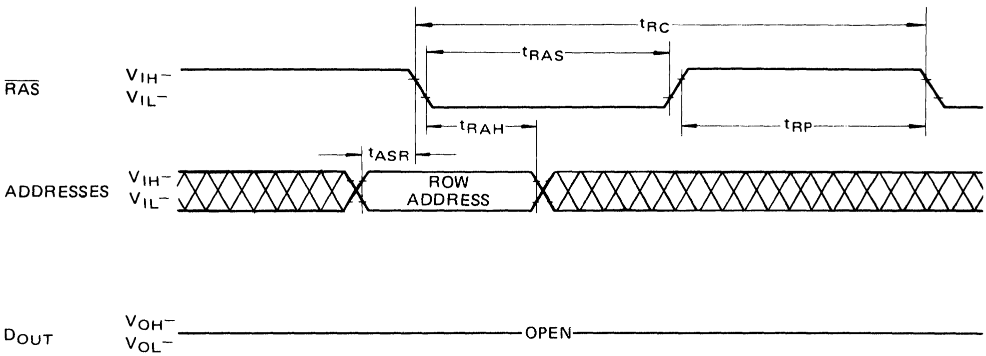


PAGE-MODE WRITE CYCLE

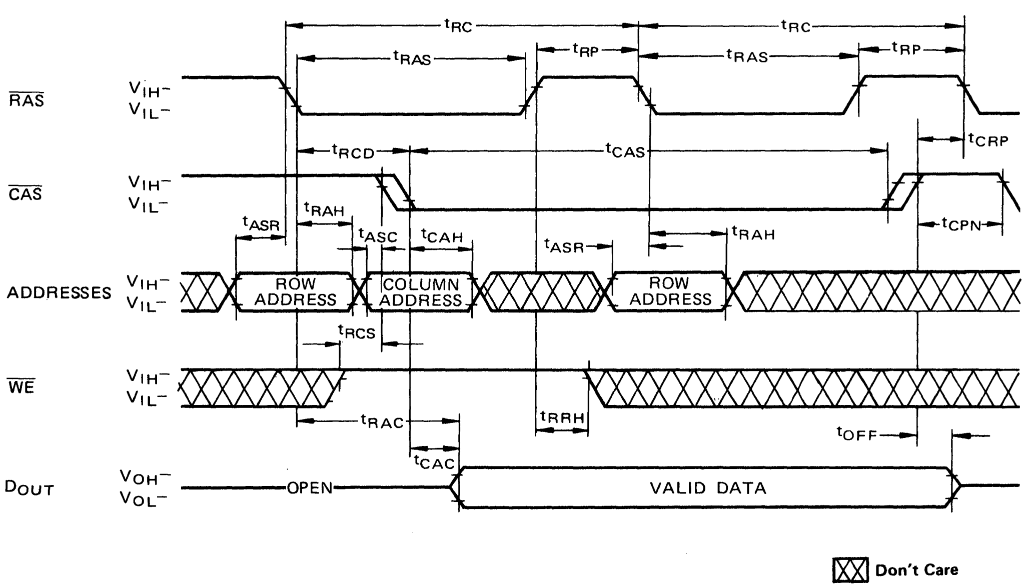


"$\overline{RAS}$-ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't care



HIDDEN "$\overline{RAS}$-ONLY" REFRESH CYCLE



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB8264. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). Then eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8264 during a write or read-write cycle. The last falling-edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits strobing the row-address into the MB8264 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

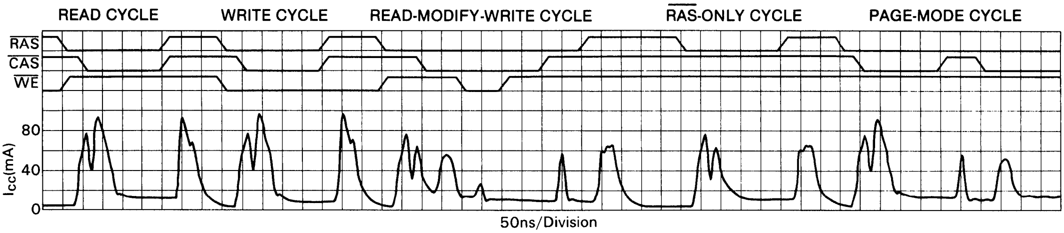
Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

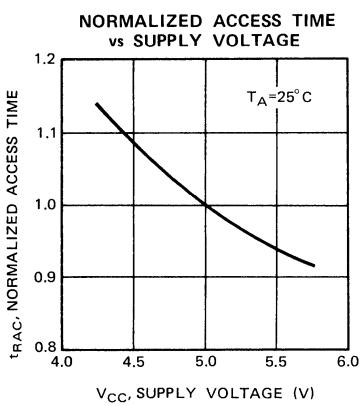
Hidden Refresh

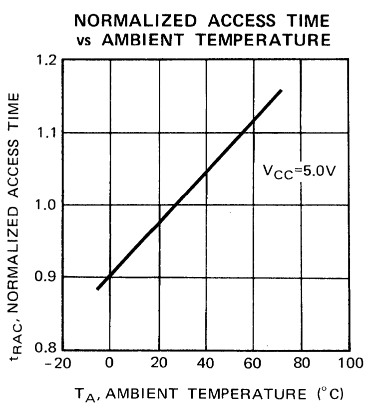
$\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

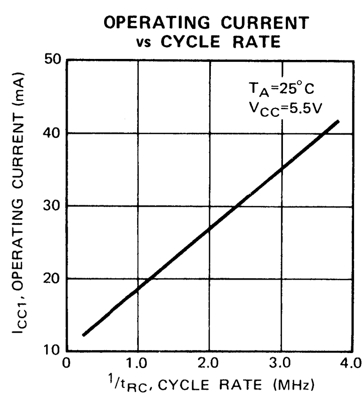
CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

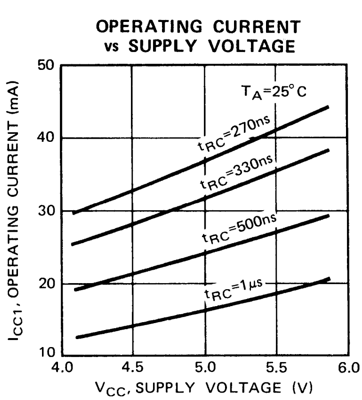


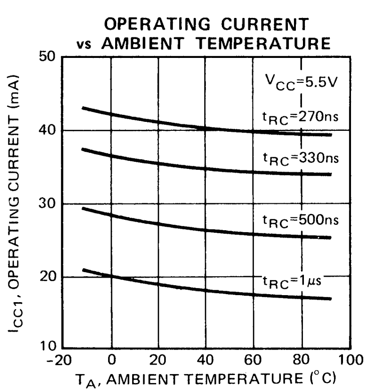
TYPICAL CHARACTERISTICS CURVES

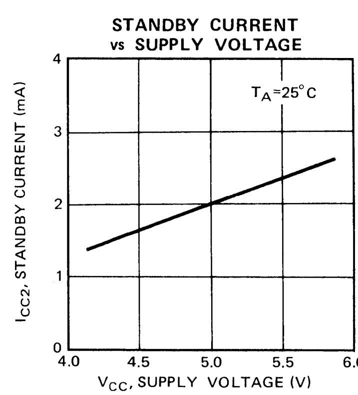






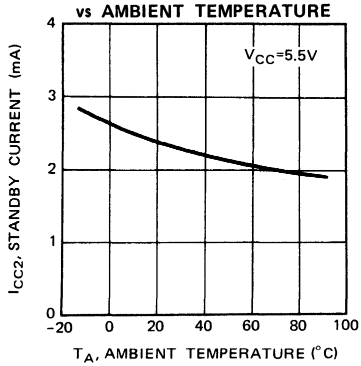




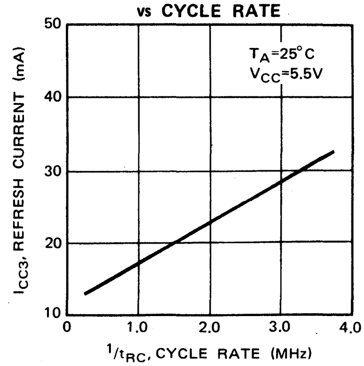


TYPICAL CHARACTERISTICS CURVES (Continued)

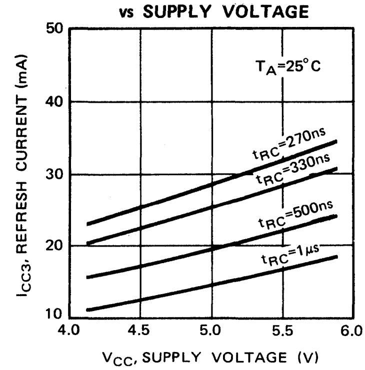
STANDBY CURRENT vs AMBIENT TEMPERATURE



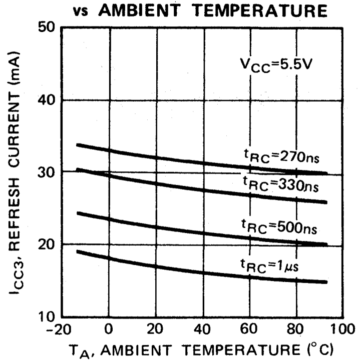
REFRESH CURRENT vs CYCLE RATE



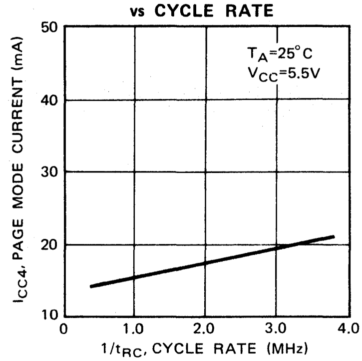
REFRESH CURRENT vs SUPPLY VOLTAGE



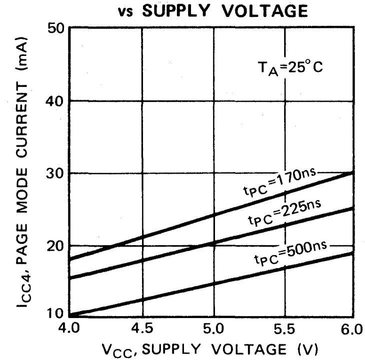
REFRESH CURRENT vs AMBIENT TEMPERATURE



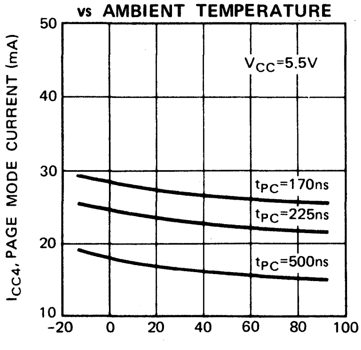
PAGE MODE CURRENT vs CYCLE RATE



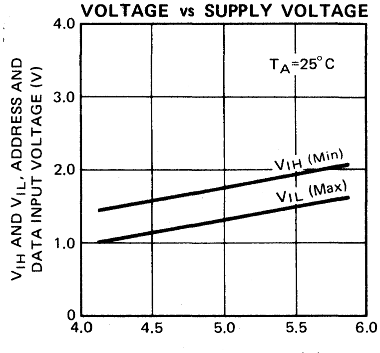
PAGE MODE CURRENT vs SUPPLY VOLTAGE



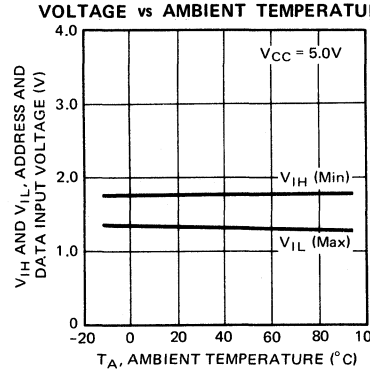
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

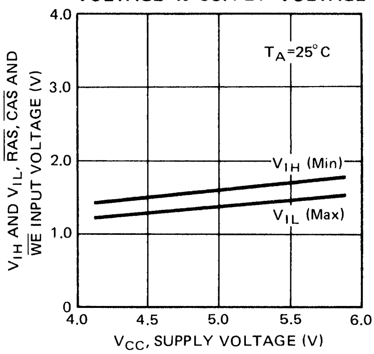


ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

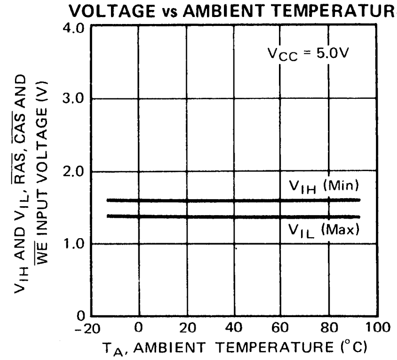


TYPICAL CHARACTERISTICS CURVES (Continued)

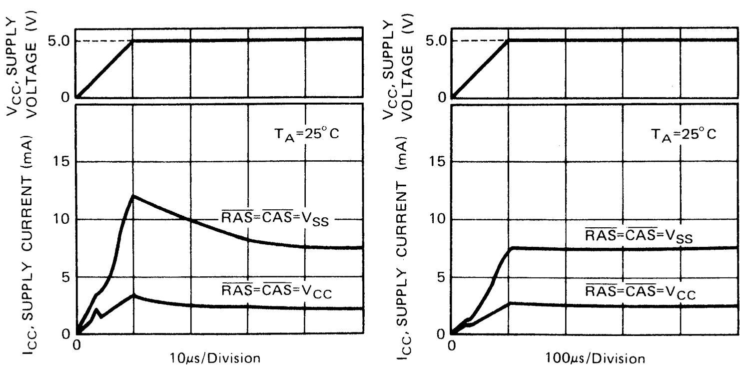
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE



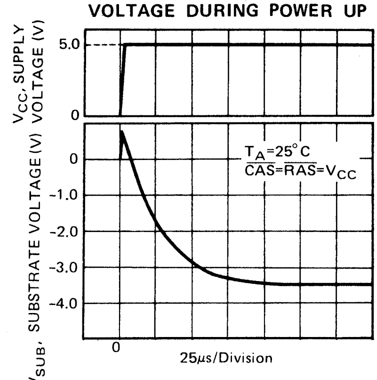
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE



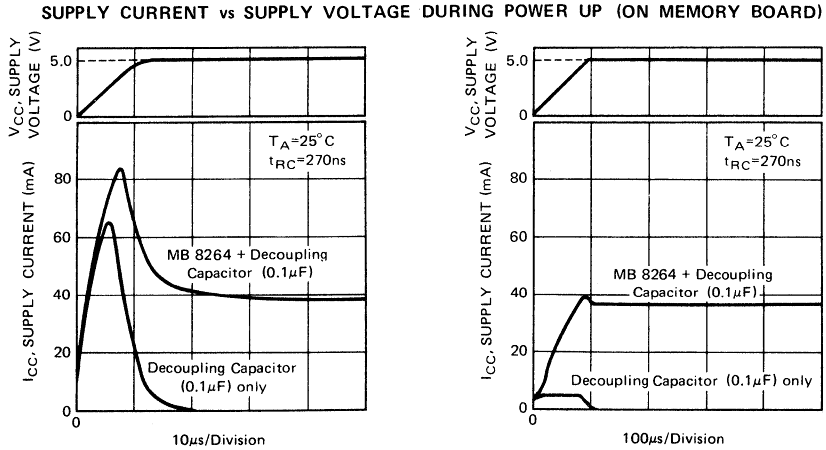
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP



SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE DURING POWER UP



SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP (ON MEMORY BOARD)



FUJITSU
MICROELECTRONICS, INC.

MB8264A-10
MB8264A-12
MB8264A-15

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

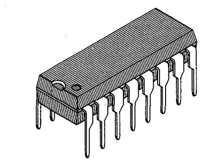
DESCRIPTION

The Fujitsu MB8264A is a fully decoded, dynamic NMOS random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

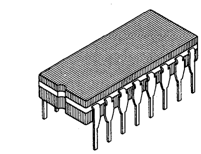
Multiplexed row and column address inputs permit the MB8264A to be housed in a standard 16-pin DIP and 18-pad LCC. With a JEDEC approved pin out.

The MB8264A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including dynamic sense amplifiers.

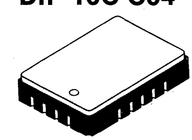
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs and the output are TTL compatible.



PLASTIC PACKAGE
DIP-16P-M03



CERDIP PACKAGE
DIP-16C-C04

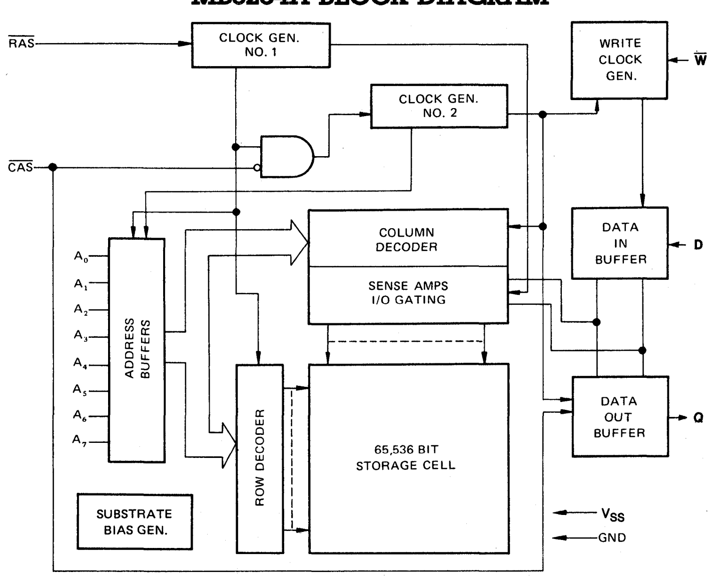


CERAMIC LCC
LCC-18C-F02

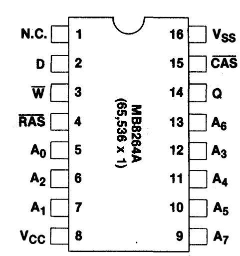
FEATURES

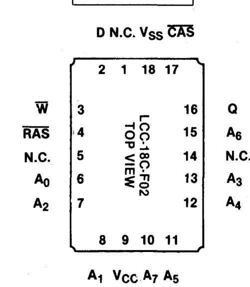
- 65,536 x 1-bit organization
- Row Access Time/Cycle Time
  MB8264A-10 100 ns Max./200 ns Min.
  MB8264A-12 120 ns Max./230 ns Min
  MB8264A-15 150 ns Max./260 ns Min.
- Low Max Power Dissipation (t_{RC} = min)
  MB8264A-10 275 mW (Active)
  MB8264A-12 248 mW (Active)
  MB8264A-15 220 mW (Active)
  All devices 22 mW (Standby) max.
- Single +5V supply voltage, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- RAS only and hidden refresh
- 2ms/128 cycle refresh
- Read-Modify-Write and Page Mode capability
- "Gated" $\overline{CAS}$
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Common I/O capability using "Early Write" operation
- On-chip Address and Data-in latches
- On-chip substrate bias generator
- t_{AR}, t_{WCR}, t_{DHR} eliminated

MB8264A BLOCK DIAGRAM



PIN ASSIGNMENT





NOTE: The following IEEE STD. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7.0	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all Inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all Inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance $A_0 \sim A_7$, D	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}	—	—	8	pF
Output Capacitance Q	C_{OUT}	—	—	7	pF

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8264A-10		MB8264A-12		MB8264A-15		Unit
		Min	Max	Min	Max	Min	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}	—	50	—	45	—	40	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}/\overline{CAS}$ = V_{IH})	I_{CC2}	—	4	—	4	—	4	mA
REFRESH CURRENT* Average Power Supply Current ($\overline{CAS}$ = V_{IH}; $\overline{RAS}$ cycling, t_{RC} = min.)	I_{CC3}	—	38	—	35	—	31	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}	—	35	—	32	—	28	mA
INPUT LEAKAGE CURRENT, any input ($0V \leq V_{IN} \leq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V
OUTPUT LEVEL, Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB8264A-10 Min	MB8264A-10 Max	MB8264A-12 Min	MB8264A-12 Max	MB8264A-15 Min	MB8264A-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV	—	2	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	230	—	265	—	280	—	ns
Page Mode Cycle Time		t_{PC}	TCELCEL	105	—	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	135		155		180		ns
Access Time from $\overline{\text{RAS}}$	(4), (6)	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{\text{CAS}}$	(5), (6)	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		t_{T}	TT	3	50	3	50	3	50	ns
$\overline{\text{RAS}}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{\text{RAS}}$ Pulse Width		t_{RAS}	TRELREH	100	10000	120	10000	150	10000	ns
$\overline{\text{RAS}}$ Hold Time		t_{RSH}	TCELREH	50	—	60	—	75	—	ns
$\overline{\text{CAS}}$ Precharge Time (Page mode only)		t_{CP}	TCEHCEL	45	—	50	—	60	—	ns
$\overline{\text{CAS}}$ Precharge Time (All cycles except page mode)		t_{CPN}	TCEHCEL	25	—	30	—	30	—	ns
$\overline{\text{CAS}}$ Pulse Width		t_{CAS}	TCELCEH	50	10000	60	10000	75	10000	ns
$\overline{\text{CAS}}$ Hold Time		t_{CSH}	TRELCEH	100	—	120	—	150	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	(4), (7)	t_{RCD}	TRELCEL	20	50	20	60	25	75	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t_{CRP}	TCEHREL	0	—	0	—	0	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Reference to $\overline{\text{CAS}}$	(9)	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	(9)	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Write Command Set Up Time	(8)	t_{WCS}	TWLCEL	0	—	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	20	—	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	20	—	25	—	30	—	ns
Write Command to $\overline{\text{RAS}}$ Lead Time		t_{RWL}	TWLREH	35	—	40	—	45	—	ns
Write Command to $\overline{\text{CAS}}$ Lead Time		t_{CWL}	TWLCEH	35	—	40	—	45	—	ns
Data In Set Up Time		t_{DS}	TDVCEL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	20	—	25	—	30	—	ns
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ Delay	(8)	t_{CWD}	TCELWL	40	—	50	—	60	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ Delay	(8)	t_{RWD}	TRELWL	90	—	110	—	120	—	ns

See notes on following page.

*These symbols are described in IEEE Std. 662-1980: IEEE Standard Terminology for Semiconductor memory.

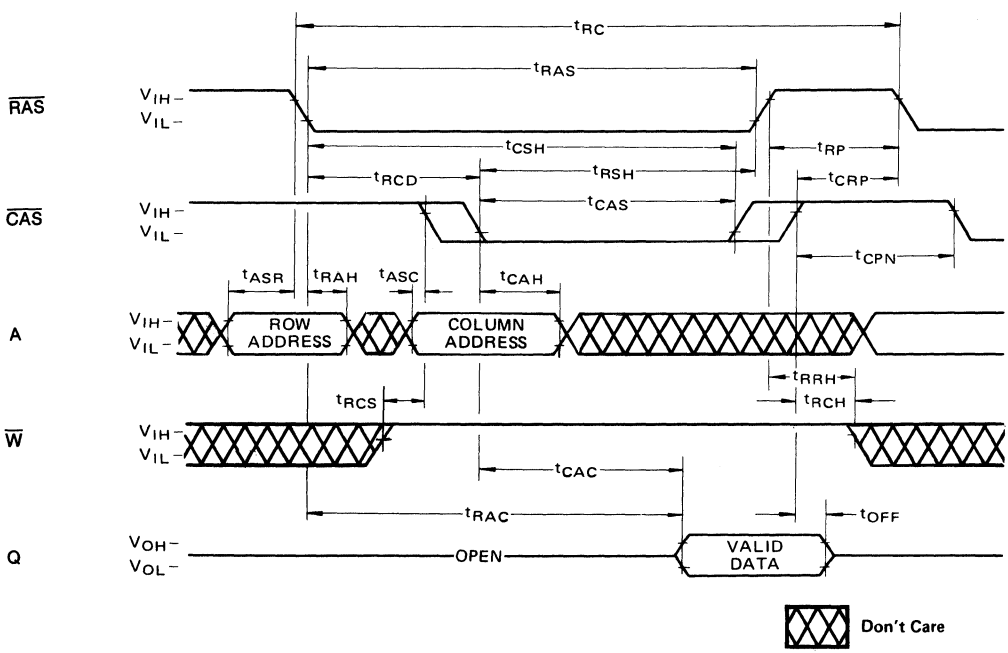
Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 RAS cycles before proper device operation is achieved.
2. AC characteristics assume t_T = 5ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min.) and V_{IL} (max.).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.); t_T = 5ns.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle, and the data out pin will remain open circuit (high impedance) throughout entire cycle.

   If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

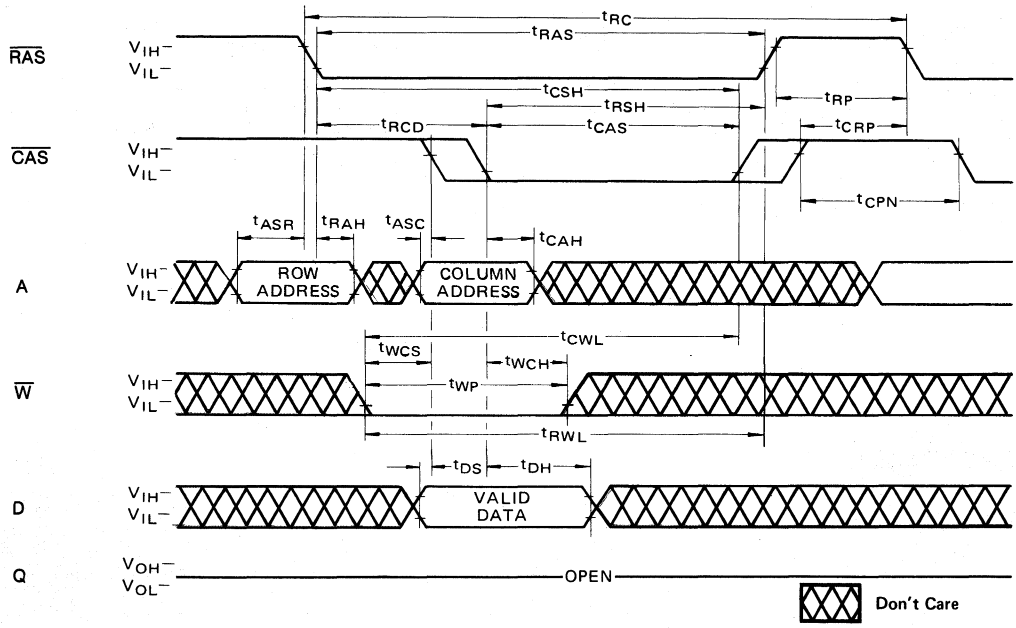
TIMING DIAGRAMS

READ CYCLE

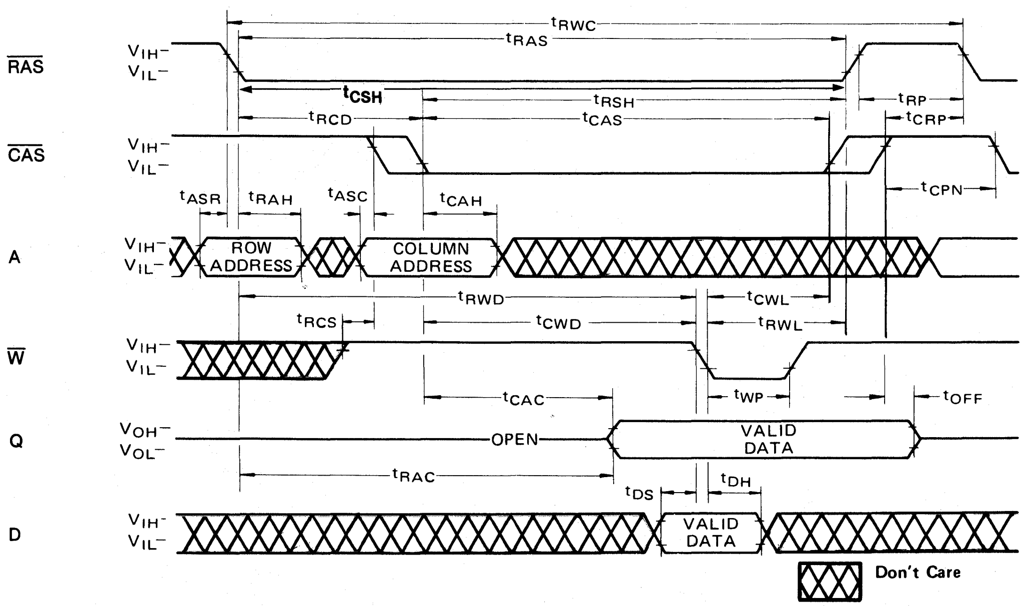


TIMING DIAGRAMS (Continued)

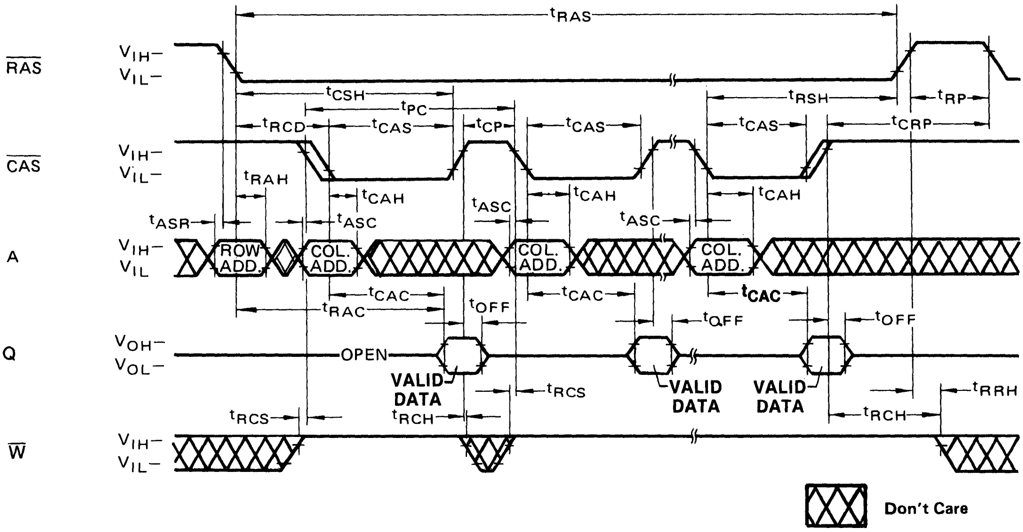
WRITE CYCLE (EARLY WRITE)



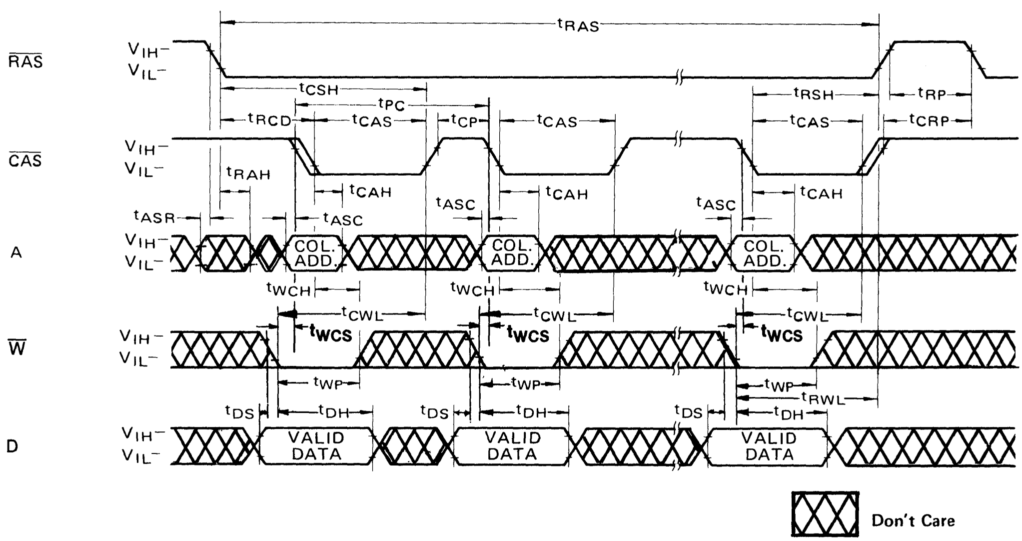
READ-WRITE/READ-MODIFY-WRITE CYCLE



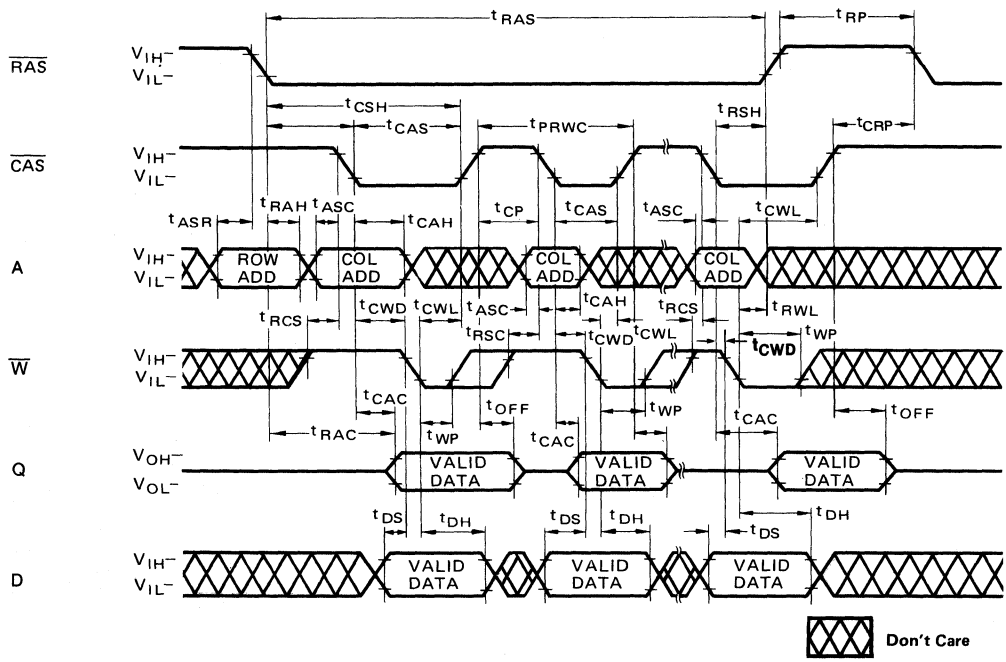
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

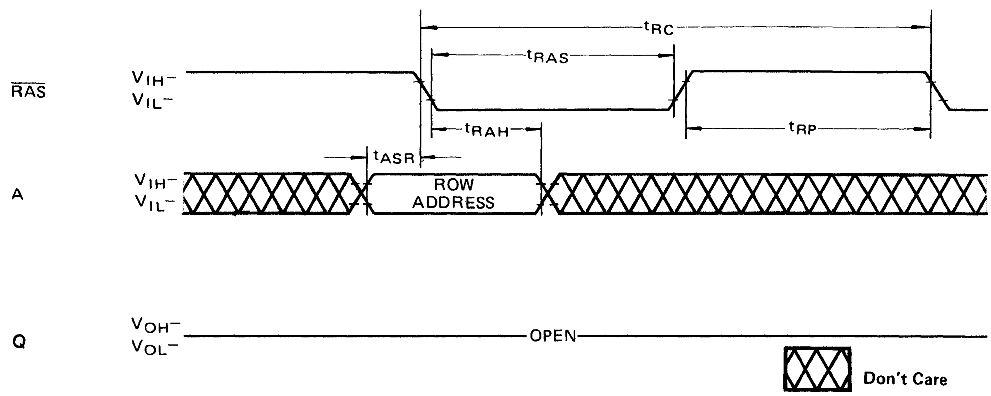


PAGE MODE READ-WRITE CYCLE

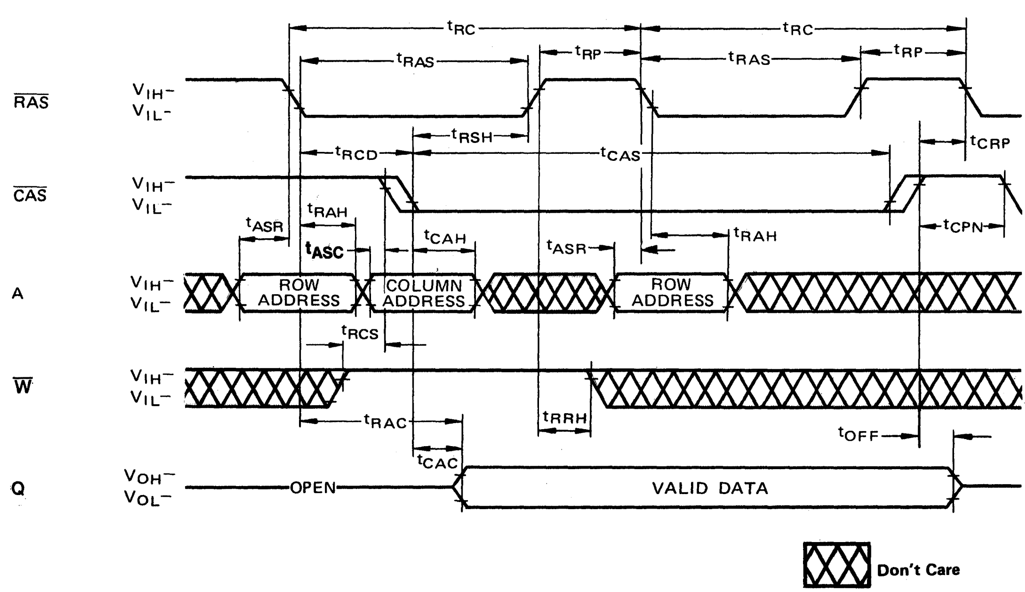


RAS-ONLY REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = Don't Care



HIDDEN RAS-ONLY REFRESH CYCLE



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any one of 65,536 storage cell locations within the MB8264A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic high (1) on $\overline{W}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8264A during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data In (D) register. In a write cycle, if $\overline{W}$ is brought low (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode

Page mode operation permits strobing the row-address into the MB8264A while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh

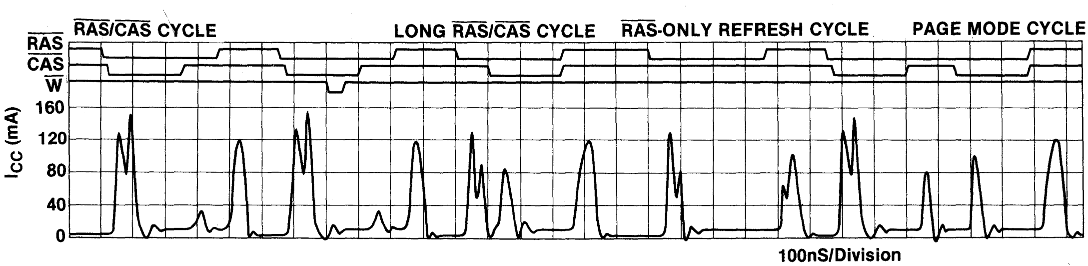
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh

A $\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

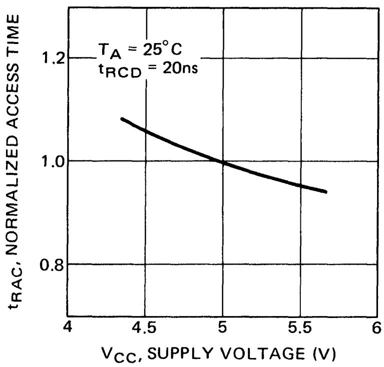
Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} from a previous memory read cycle.

CURRENT WAVEFORM ((V_{CC} = 5.5V, TA = 25 °C)

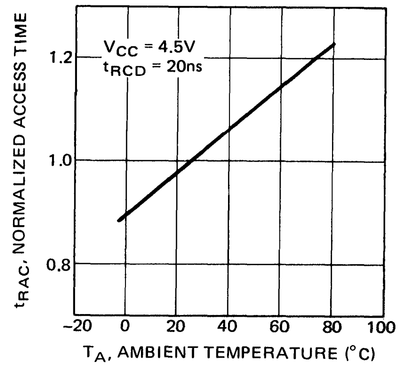


TYPICAL CHARACTERISTICS CURVES

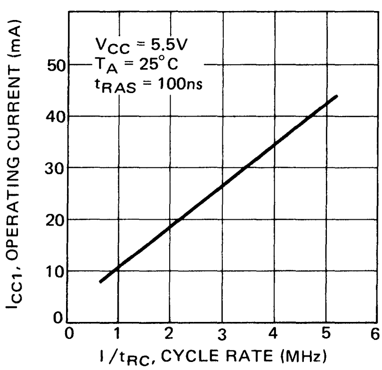
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



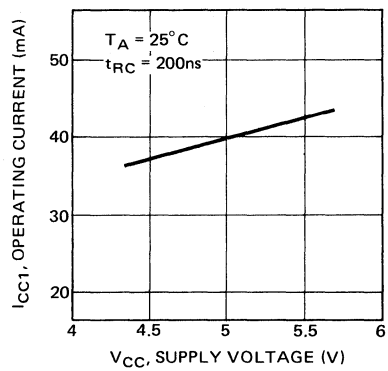
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



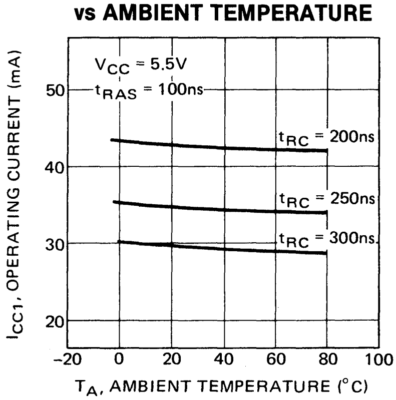
OPERATING CURRENT vs CYCLE RATE



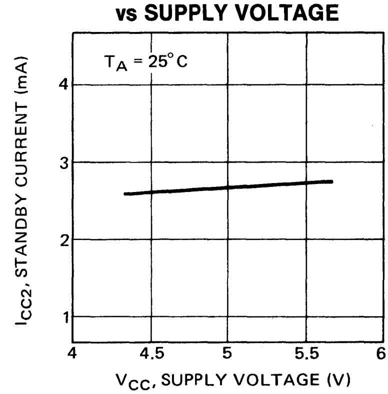
OPERATING CURRENT vs SUPPLY VOLTAGE



OPERATING CURRENT vs AMBIENT TEMPERATURE

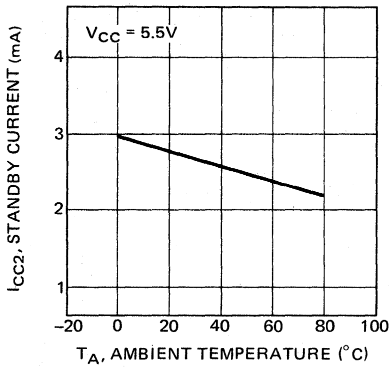


STANDBY CURRENT vs SUPPLY VOLTAGE

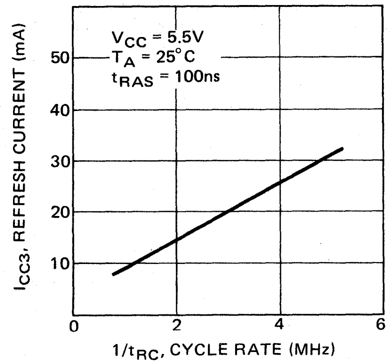


TYPICAL CHARACTERISTICS CURVES (Continued)

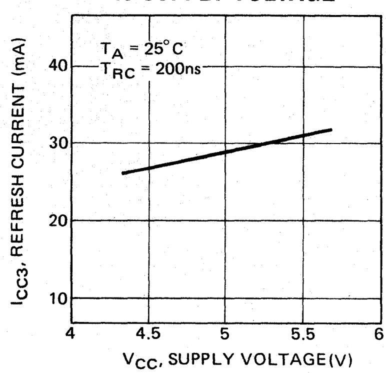
STANDBY CURRENT vs AMBIENT TEMPERATURE



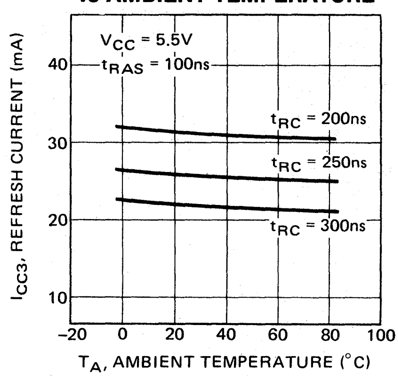
REFRESH CURRENT vs CYCLE RATE



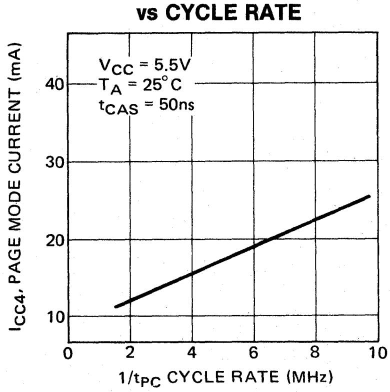
REFRESH CURRENT vs SUPPLY VOLTAGE



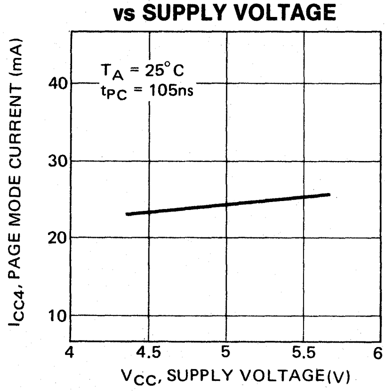
REFRESH CURRENT vs AMBIENT TEMPERATURE



PAGE MODE CURRENT vs CYCLE RATE

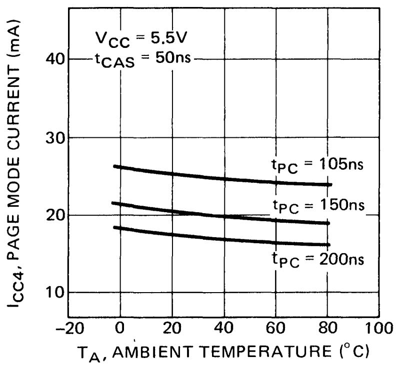


PAGE MODE CURRENT vs SUPPLY VOLTAGE

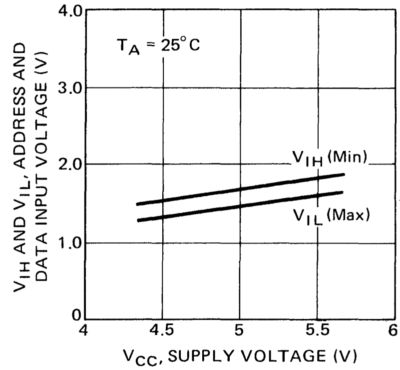


TYPICAL CHARACTERISTICS CURVES (Continued)

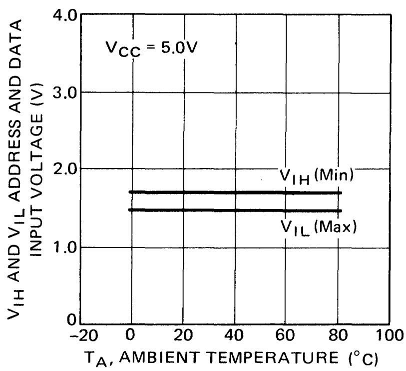
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



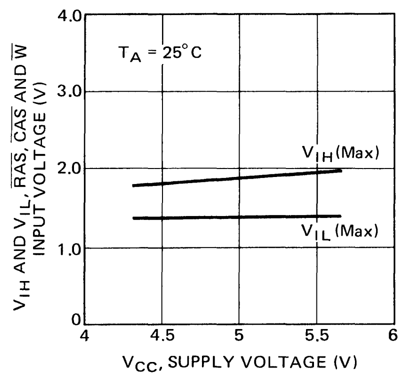
ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE



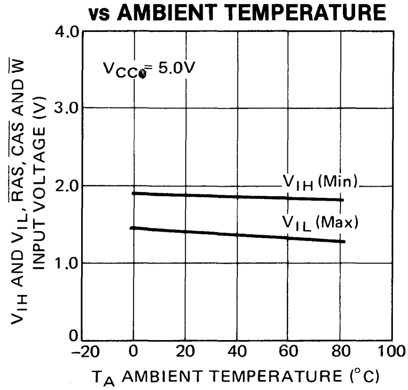
ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

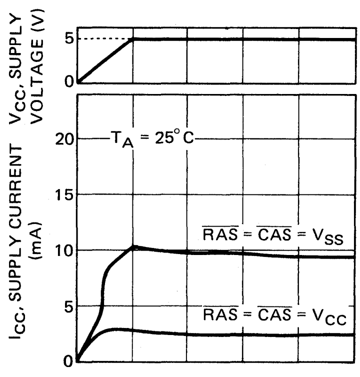


$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ VOLTAGE vs AMBIENT TEMPERATURE

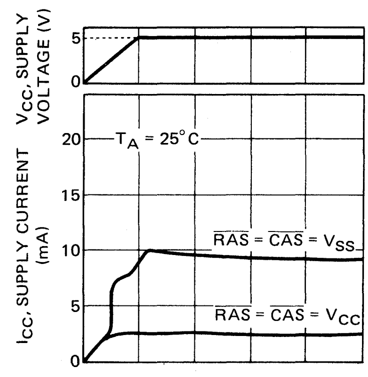


TYPICAL CHARACTERISTICS CURVES (Continued)

CURRENT WAVEFORM DURING POWER UP

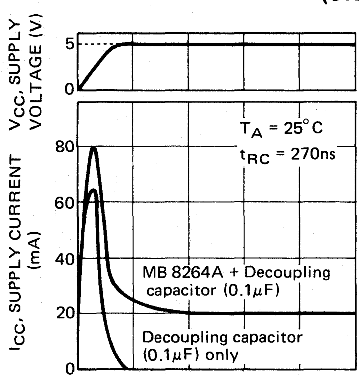


10µs/Division

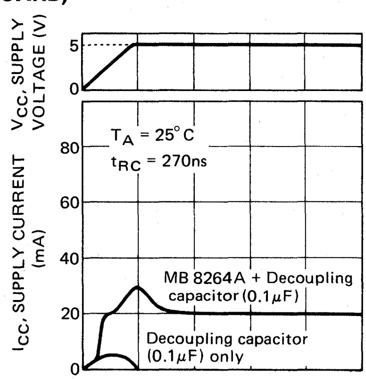


100µs/Division

CURRENT WAVEFORM DURING POWER UP (ON MEMORY BOARD)

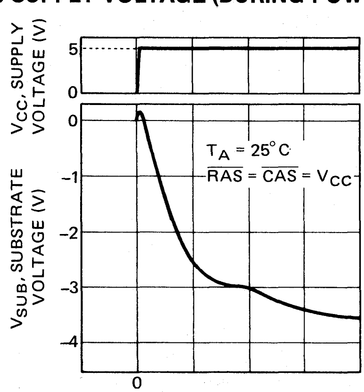


20µs/Division



100µs/Division

SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE (DURING POWER UP)



50µs/Division

Preliminary

MOS Memories

FUJITSU

MB8264A-12-W, MB8264A-15-W
NMOS 65,536-Bit Dynamic Random Access Memory With Wide Temperature Range

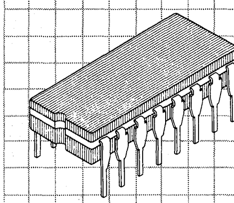
Description

The MB8264A-W is a 64K x 1 dynamic RAM intended for operation over the case temperature range −55°C to 110°C. The part is also available with Fujitsu's 883B high reliability screening.

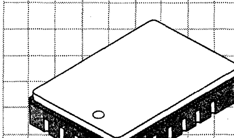
The MB8264A-W design has been optimized for high speed high performance applications such as mainframe memory, buffer memory, and peripheral storage where low power dissipation, compact layout, or wide temperature range operation are required.

The MB8264A-W has fully TTL compatible inputs and output. It operates on a single +5 V ± 10% power supply. An on chip substrate bias generator provides high performance operation. The MB8264A-W contains on-chip latches for the address inputs and for the data input.

The MB8264A-W is fabricated with Fujitsu's advanced silicon gate NMOS double layer polysilicon process. This process along with the use of single transistor storage cells permits maximum circuit density and minimum chip size. Multiplexed row and column addressing allows the MB8264A-W to be packaged in a standard 16-pin DIP.



Cerdip Package
DIP-16C-C04

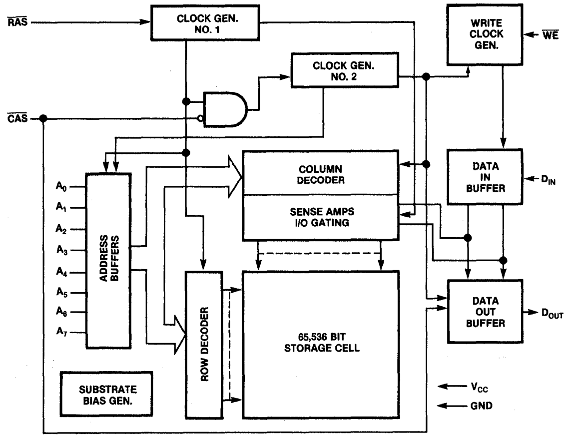


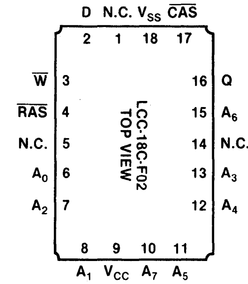
LCC-18C-F02

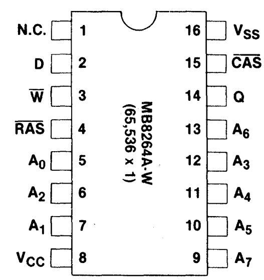
Features

- **Wide Temperature Range**
  TC = −55°C to 110°C
- **65,536 x 1 organization**
- **Row Access Time:**
  120 ns max. (MB8264A-12-W)
  150 ns max. (MB8264A-15-W)
- **Cycle Time:**
  230 ns min. (MB8264A-12-W)
  260 ns min. (MB8264A-15-W)
- **Low Power (Active)**
  305 mW max. (MB8264A-12-W)
  275 mW max. (MB8264A-15-W)
  33 mW max. (Standby)
- **1 ms/128 cycle refresh**
- **$\overline{RAS}$-Only and Hidden Refresh**
- **Read-Modify-Write capability**
- **Page Mode capability**
- **Common I/O capability using the early write operation**
- **Output unlatched at cycle end allows extended page boundary**
- **TAR, TWCR, TDHR are eliminated**
- **883B processing available**

Block Diagram and Pin Assignments







Capacitance
($T_A = 25\,°C$)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**
Input Capacitance $A_0 \sim A_7$, D	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Operating Temperature (case)**
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	−55 °C to +110 °C
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

AC Characteristics
(Recommended operating conditions unless otherwise noted.)
(Notes 1, 2, 3)

Parameter	Notes	Symbol	MB8264A -12-A Min	MB8264A -12-A Max	MB8264A -15-W Min	MB8264A -15-W Max	Unit
Time between Refresh		t_{REF}	—	1	—	1	ms
Random Read/Write Cycle Time		t_{RC}	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	265	—	280	—	ns
Page Mode Cycle Time		t_{PC}	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	155	—	180	—	ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}	—	120	—	150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	—	60	—	75	ns
Output Buffer Turn off Delay		t_{OFF}	0	35	0	40	ns
Transition Time		t_T	3	50	0	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	60	—	75	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	50	—	60	—	ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	30	—	30	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	ns
Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
Read Command Hold Time Reference to $\overline{CAS}$	10	t_{RCH}	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	10	t_{RRH}	20	—	20	—	ns
Write Command Set Up Time	9	t_{WCS}	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	25	—	30	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	40	—	45	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	40	—	45	—	ns
Data In Set Up Time		t_{DS}	0	—	0	—	ns
Data In Hold Time		t_{DH}	25	—	30	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	50	—	60	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	110	—	120	—	ns

Notes:

1) An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2) AC characteristics assume $t_T = 5$ ns.
3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6) Measured with a load equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max) limit insures that t_{RAC} can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{RCD} (min) = t_{RAH} (min) + $2t_T$ ($t_T = 5$ ns) + t_{ASC} (min).
9) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB8264A-12-W	I_{CC1}		55	mA
	MB8264A-15-W			50	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}		6	mA
REFRESH CURRENT* Average Power Supply Current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min)	MB8264A-12-W	I_{CC3}		40	mA
	MB8264A-15-W			35	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = min)	MB8264A-12-W	I_{CC4}		40	mA
	MB8264A-15-W			35	
INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \le V_{IN} \le 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0V)		$I_{I(L)}$	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0 \le V_{OUT} \le 5.5$)		$I_{O(L)}$	−10	10	μA
OUTPUT LEVELS Output High Voltage ($I_{OH} = -5mA$)		V_{OH}	2.4		V
Output Low Voltage ($I_{OL} = 4.2mA$)		V_{OL}		0.4	V

Note *: I_{CC} is dependent on output loading cycle rates. Specified values are obtained with the output open.

Description

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65,536 storage cell locations within the MB8264A-W. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stabled on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates read mode; logic low dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8264A-W during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from the transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode

Page mode operation permits strobing the row-address into the MB8264A-W while maintaining $\overline{RAS}$ at a logic low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

RAS-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

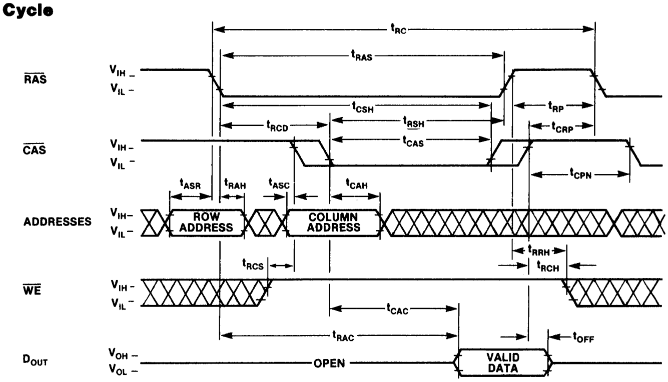
Hidden Refresh

$\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

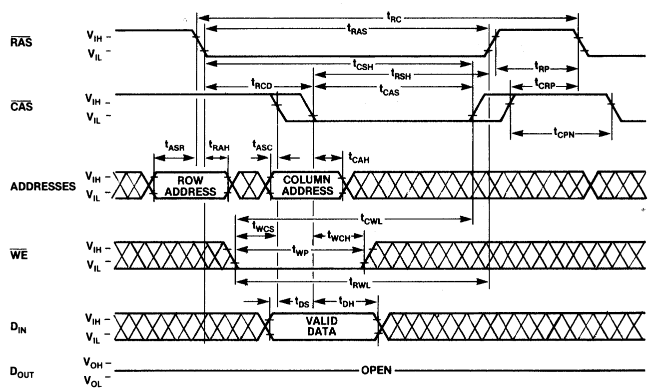
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

Timing Diagrams

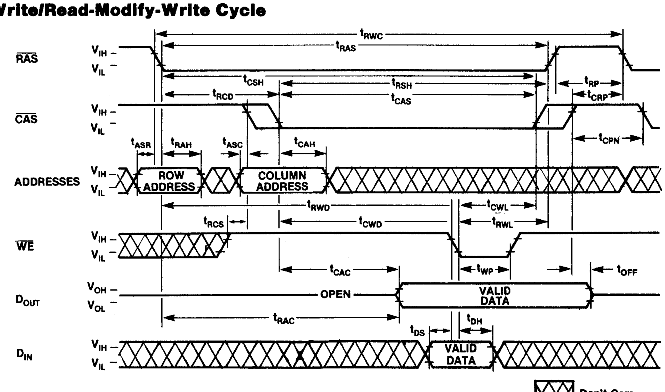
Read Cycle



Write Cycle (Early Write)

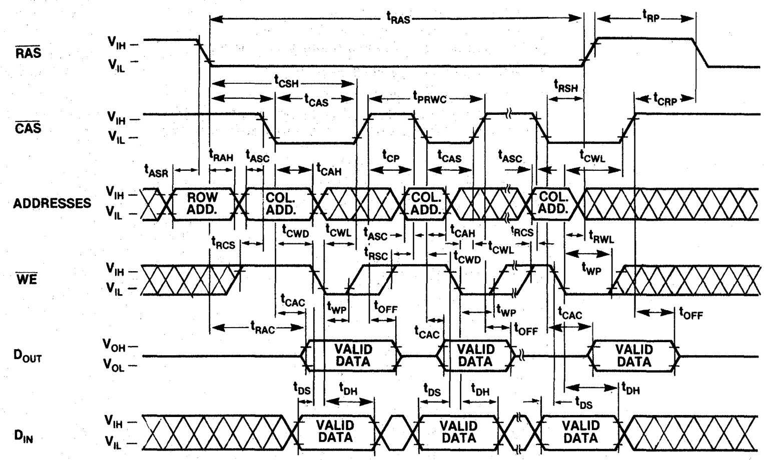


Read-Write/Read-Modify-Write Cycle



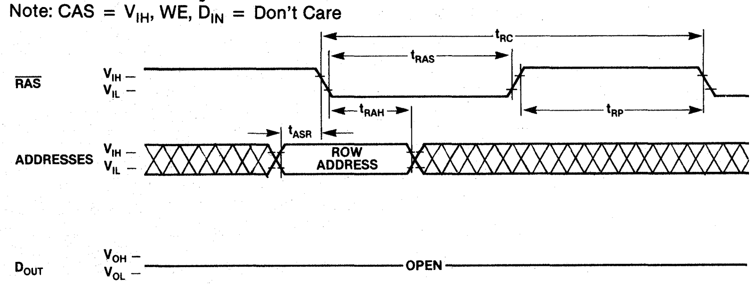
Timing Diagrams, Continued

Page Mode Read-Write Cycle

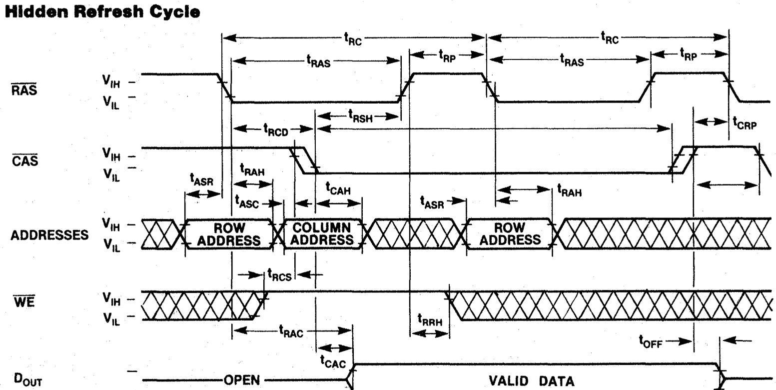


RAS-ONLY Refresh Cycle

Note: CAS = V_{IH}, WE, D_{IN} = Don't Care



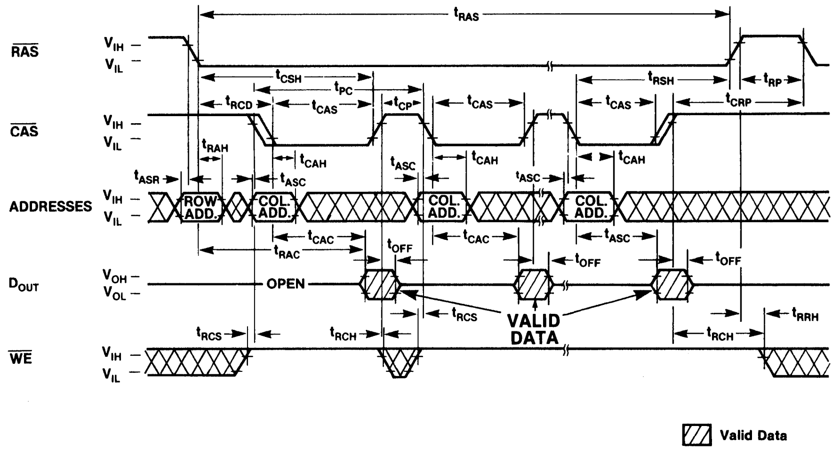
Hidden Refresh Cycle



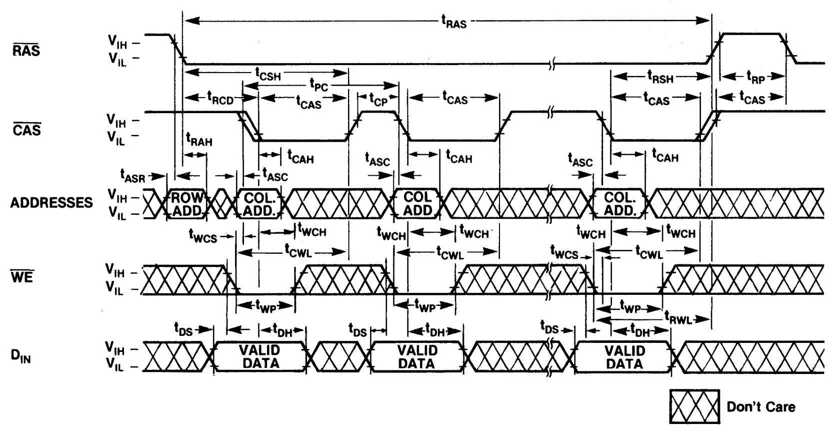
Don't Care

Timing Diagrams, Continued

Page Mode Read Cycle



Page Mode Write Cycle



FUJITSU
MICROELECTRONICS, INC.

MB8265-15
MB8265-20

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

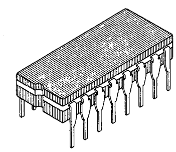
DESCRIPTION

The Fujitsu MB8265 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

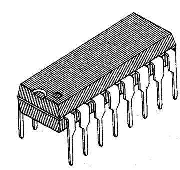
Multiplexed row and column address inputs permit the MB8265 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MB8265 is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

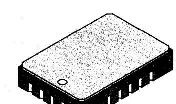
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.



CERAMIC PACKAGE
CERDIP
DIP-16C-C04



PLASTIC PACKAGE
DIP-16P-M03

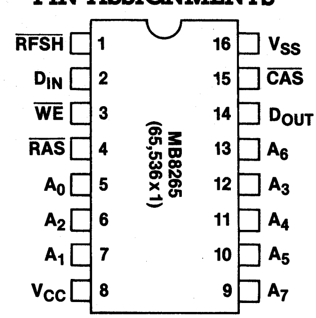


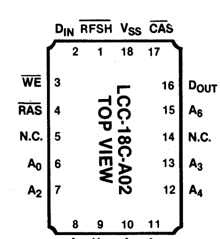
CERAMIC LCC
LCC-18C-A02

FEATURES

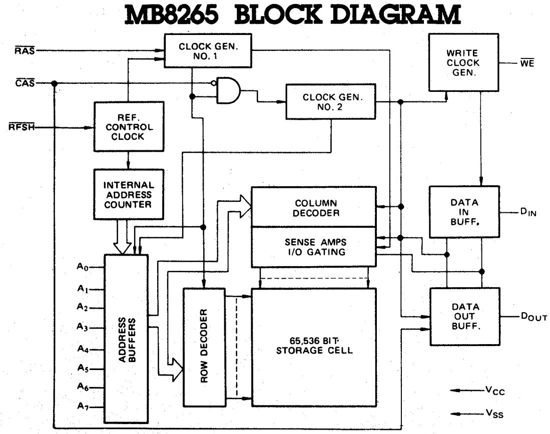
- **65,536 x 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Row access time:**
  150ns Max (MB8265-15)
  200ns Max (MB8265-20)
- **Cycle time:**
  270ns Min (MB8265-15)
  330ns Min (MB8265-20)
- **Low power:**
  275 mW Active, (MB8265-15)
  248 mW Active, (MB8265-20)
  28 mW Standby (Max)
- **+5V Supply, ±10% tolerance**
- **On chip substrate bias generator for high performance**
- **Three-state TTL compatible output**
- **All inputs TTL compatible, low capacitive load**
- **"Gated" $\overline{CAS}$**
- **128 refresh cycles**
- **Pin 1 Refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-in**
- **Offers two variations of hidden refresh**

PIN ASSIGNMENTS





MB8265 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7.0	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance $A_0 \sim A_7$, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB8265-20	I_{CC1}		45	mA
	MB8265-15		—	50	mA
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{RFSH}$ = V_{IH})		I_{CC2}	—	5	mA
REFRESH CURRENT 1 Average power current ($\overline{RAS}$ cycling $\overline{CAS}$ = $\overline{RFSH}$ = V_{IH}; t_{RC} = min)	MB8265-20	I_{CC3}	—	36	mA
	MB8265-15			42	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)		I_{CC4}	—	34	mA
REFRESH CURRENT 2 Average power supply current ($\overline{RFSH}$ cycling; $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, t_{FC} = min)		I_{CC5}	—	46	mA
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V) Input pins not under test = 0V, V_{CC} = 5.5V, V_{SS} = 0V		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
OUTPUT LEVEL Output low voltage (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V
OUTPUT LEVEL Output high voltage (I_{OH} = −5mA)		V_{OH}	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS Notes 1, 2, 3

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8265-20			MB8265-15			Unit
			Min	Typ	Max	Min	Typ	Max	
Time between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	330	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	375	—	—	300	—	—	ns
Page Mode Cycle Time		t_{PC}	225	—	—	170	—	—	ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}	—	—	200	—	—	150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	—	—	135	—	—	100	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	50	0	—	40	ns
Transition Time		t_{T}	3	—	50	3	—	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120	—	—	100	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	—	10000	150	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135	—	—	100	—	—	ns
$\overline{CAS}$ Precharge Time (Page Mode Only)		t_{CP}	80	—	—	60	—	—	ns
$\overline{CAS}$ Precharge Time (All Cycles Except Page Mode)		t_{CPN}	30	—	—	25	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	—	10000	100	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	200	—	—	150	—	—	ns
$\overline{RAS}$ to CAS Delay Time	7 8	t_{RCD}	30	—	65	25	—	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	20	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	55	—	—	45	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120	—	—	95	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time	10	t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	9	t_{WCS}	−10	—	—	−10	—	—	ns
Write Command Hold Time		t_{WCH}	55	—	—	45	—	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	120	—	—	95	—	—	ns
Write Command Pulse Width		t_{WP}	55	—	—	45	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80	—	—	60	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80	—	—	60	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	55	—	—	45	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120	—	—	95	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	95	—	—	70	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	160	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	10	t_{RRH}	25	—	—	20	—	—	ns
$\overline{RFSH}$ Set Up Time Referenced to $\overline{RAS}$		t_{FSR}	120	—	—	100	—	—	ns
$\overline{RAS}$ to $\overline{RFSH}$ Delay		t_{RFD}	120	—	—	100	—	—	ns
$\overline{RFSH}$ Cycle Time		t_{FC}	330	—	—	270	—	—	ns
$\overline{RFSH}$ Pulse Width		t_{FP}	200	—	—	150	—	—	ns
$\overline{RFSH}$ Inactive Time		t_{FI}	120	—	—	100	—	—	ns
$\overline{RFSH}$ to $\overline{RAS}$ Delay	11	t_{FRD}	50	—	—	40	—	—	ns
$\overline{RFSH}$ Hold Time	11	t_{FSH}	20	—	—	15	—	—	ns
$\overline{RFSH}$ Address Set Up Time	11	t_{ASF}	0	—	—	0	—	—	ns
$\overline{RFSH}$ Set Up Time Referenced to $\overline{CAS}$	11	t_{FSC}	50	—	—	40	—	—	ns

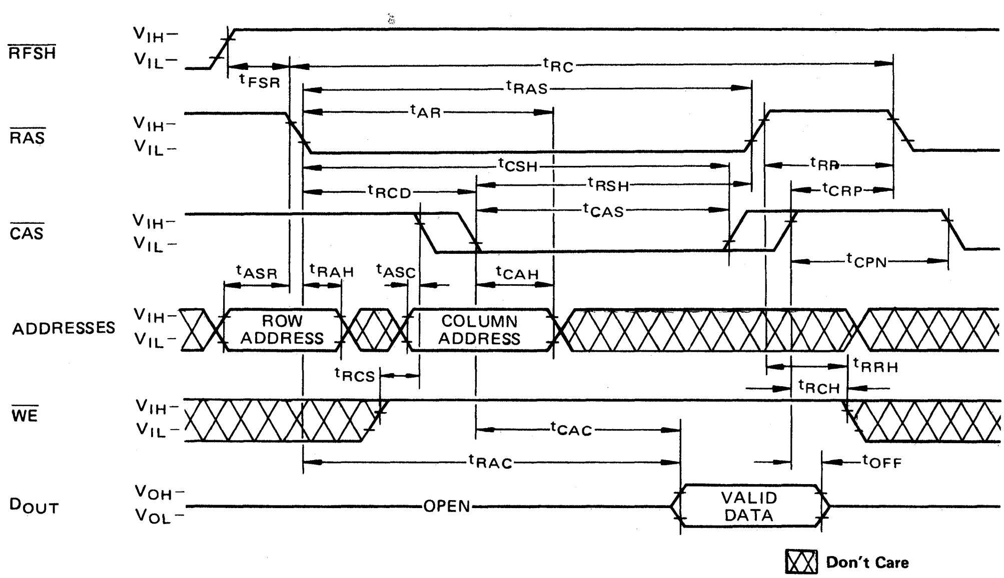
Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 active $\overline{RFSH}$ initialization cycles required. The internal refresh counter must be activated a minimum of 128 times every 2ms if the $\overline{RFSH}$ refresh function is used. The $\overline{RFSH}$ must be held at V_{IH} if the $\overline{RFSH}$ function is not used.
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).
4. Assumes that $t_{RCD} \le t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \ge t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD}(min) = t_{RAH}(min) + $2t_T$ (t_T = 5ns) + t_{ASC}(min).
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \ge t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.

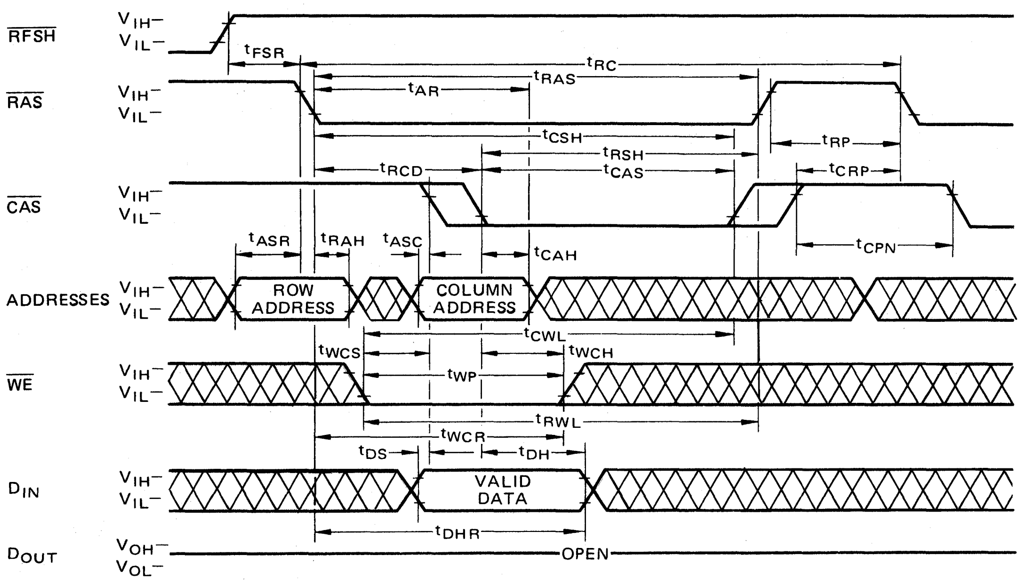
   If $t_{CWD} \ge t_{CWD}$(min) and $t_{RWD} \ge t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{RFSH}$ counter test read/write cycle only.

TIMING DIAGRAMS

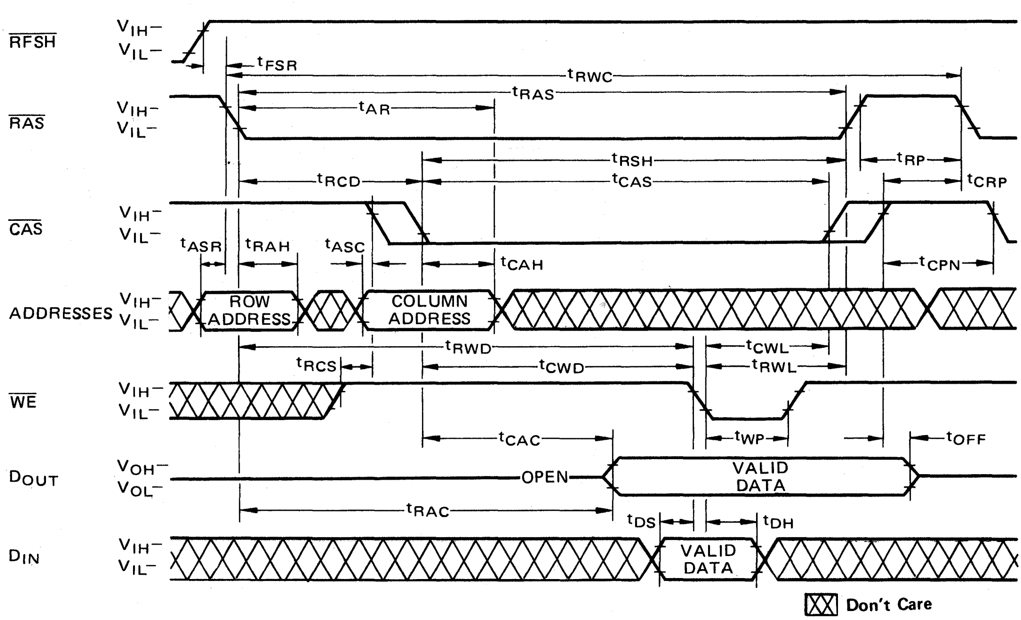
READ CYCLE



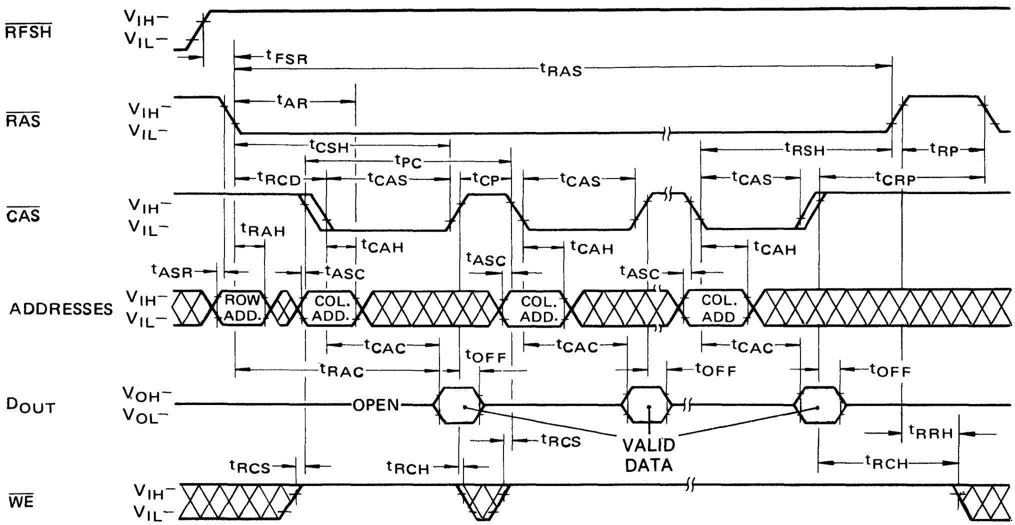
WRITE CYCLE (EARLY WRITE)



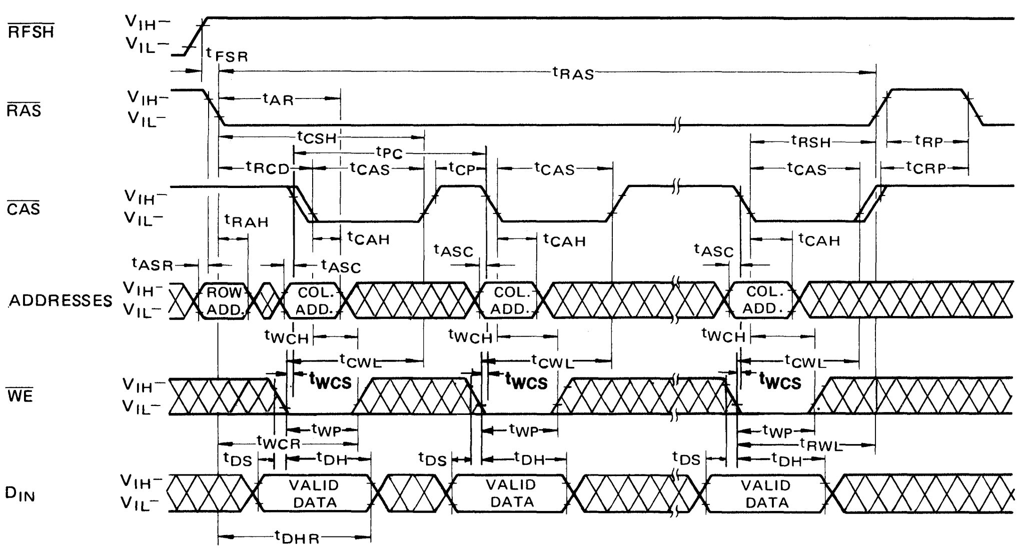
READ-WRITE/READ-MODIFY-WRITE CYCLE



PAGE-MODE READ CYCLE



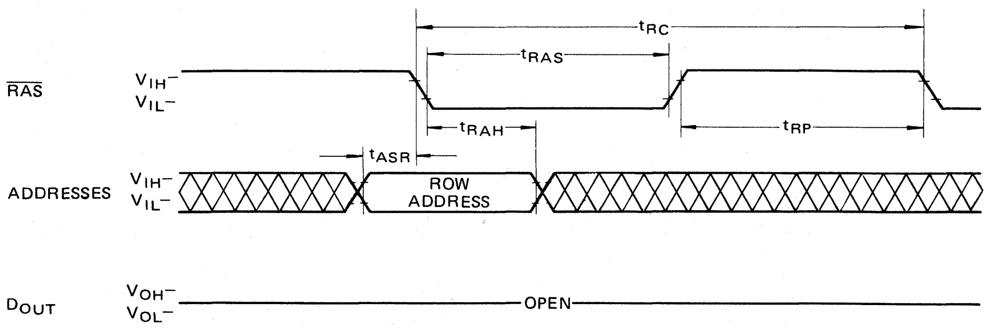
PAGE-MODE WRITE CYCLE



Don't Care

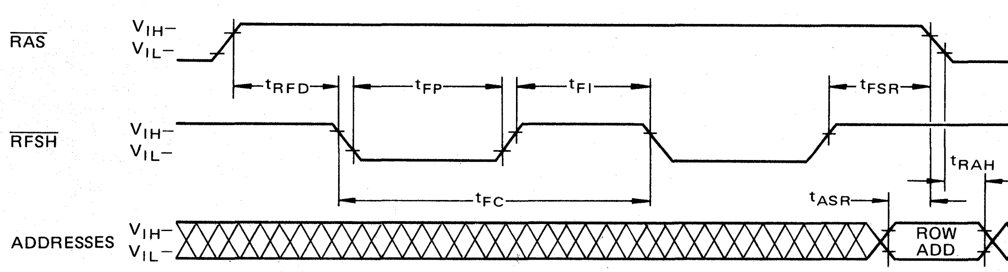
"$\overline{RAS}$-ONLY" REFRESH CYCLE

NOTE: $\overline{RFSH} = V_{IH}$, $\overline{CAS} = V_{IH}$, $\overline{WE}$ = Don't Care

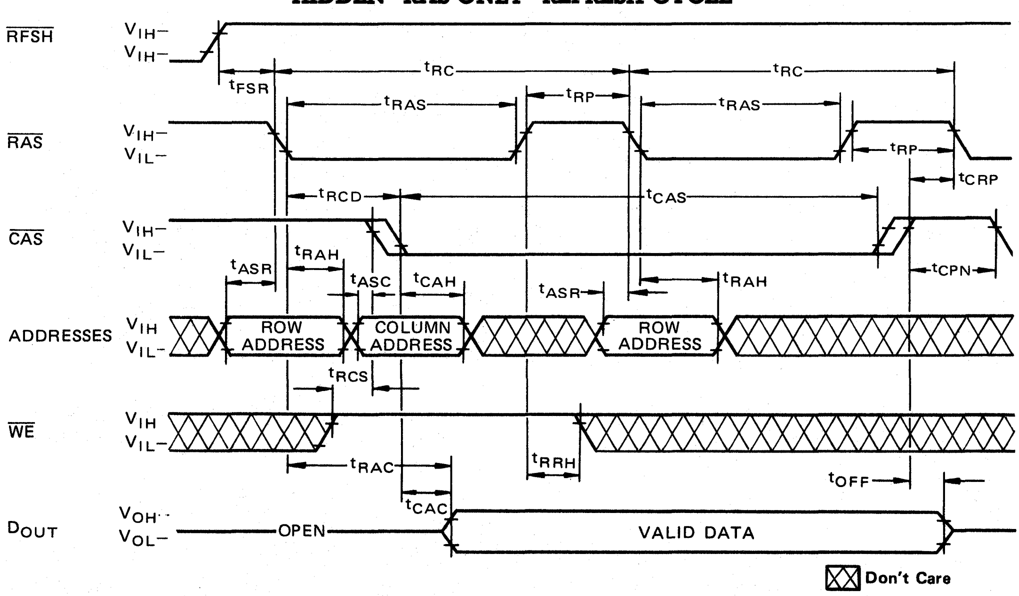


$\overline{RFSH}$ REFRESH CYCLE

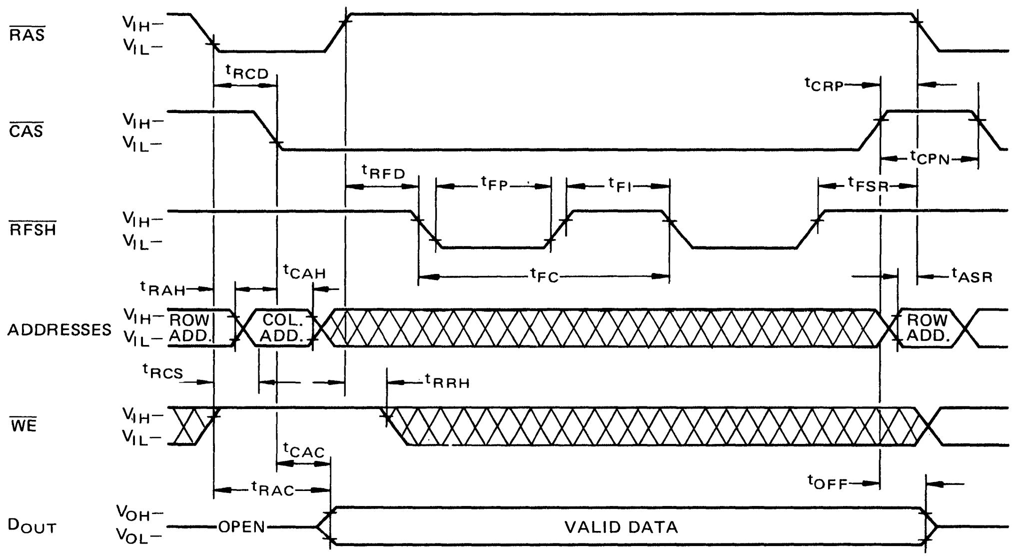
NOTE: $\overline{CAS} = V_{IH}$, $\overline{WE}$ = Don't Care



HIDDEN "$\overline{RAS}$-ONLY" REFRESH CYCLE

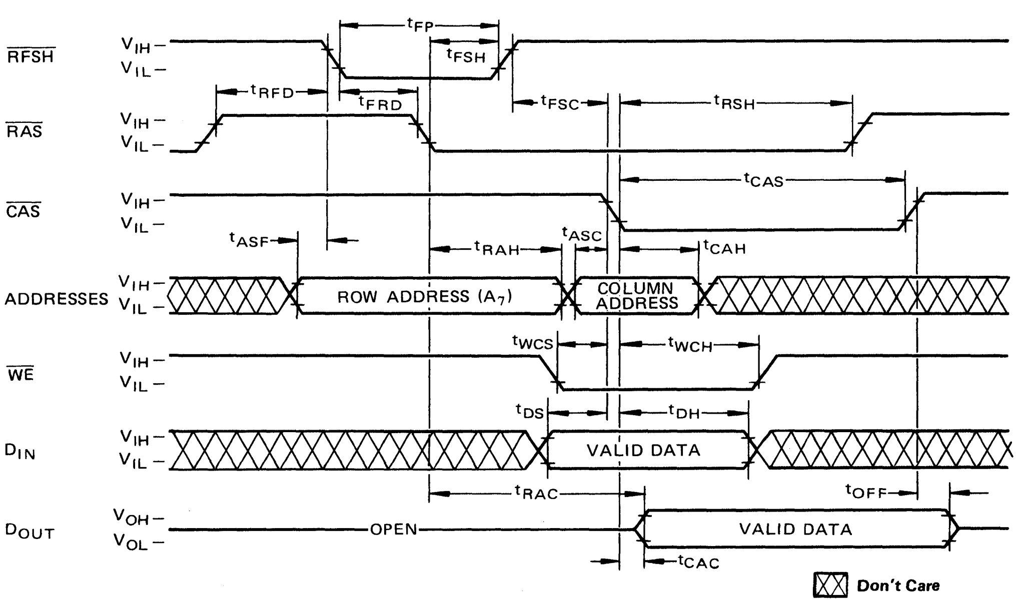


HIDDEN $\overline{RFSH}$ REFRESH CYCLE



$\overline{RFSH}$ COUNTER TEST READ/WRITE CYCLE

Note: D_{OUT} is the waveform in Read-Modify-Write Cycles



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB8265. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data written into the MB8265 during a write or read-write cycle. The last falling-edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to ahigh level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits strobing the row-address into the MB8265 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{RFSH}$ Refresh

$\overline{RFSH}$ type refreshing available on the MB8265 offers an alternate refresh method: (1) When $\overline{RFSH}$ (pin 1) is brought low (active) during $\overline{RAS}$ (Pin 4) is high (inactive), on-chip refresh control clock generators and a refresh address counter are enabled and an internal refresh operation takes place. (2) When $\overline{RFSH}$ is brought high (inactive), the internal refresh address counter is automatically incremented in preparation for the next $\overline{RFSH}$ refresh cycle. Only $\overline{RFSH}$ activated cycles affect the internal refresh address counter.

The use of $\overline{RFSH}$ type refreshing eliminates the need of providing additional external devices to generate refresh addresses.

Hidden Refresh

Hidden Refresh Cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle.

The MB8265 offers two types of Hidden Refresh. They are referred to as Hidden $\overline{RAS}$-Only Refresh and Hidden $\overline{RFSH}$ Refresh.

1) Hidden $\overline{RAS}$-Only Refresh

Hidden $\overline{RAS}$-Only Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing "$\overline{RAS}$-Only" refresh, but with $\overline{CAS}$ held low. $\overline{RFSH}$ has to be held at V_{IH}.

2) Hidden $\overline{RFSH}$ Refresh

Hidden $\overline{RFSH}$ Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RFD}), executing $\overline{RFSH}$ refresh, but with $\overline{CAS}$ held low.

A specified precharge period (t_{CPN}) is required before normal memory Read, Write or Read-Modify-Write cycle after performing either type of Hidden Refresh.

Refresh Counter Test Cycle

A special timing sequence provides a convenient method of verifying the functionality of the $\overline{RFSH}$ activated circuitry.

(A) $\overline{RFSH}$ Test Read/Write Cycle

When $\overline{RFSH}$ is given a signal in timing as shown in timing diagram of $\overline{RFSH}$ counter Test Read/Write Cycle, Read/Write Operation is enabled. A memory cell address (consisting of a row address (8 bits) and a column address (8 bits)) to be accessed can be defined as follows:

* A ROW ADDRESS — Bits $A_0 \sim A_6$ are defined when contents of the internal address counter are latched. The other bit A_7 is defined by latching a level on A_7 pin during $\overline{RFSH}$ = "L" and $\overline{RAS}$ = "H" (t_{RFD}).
* A COLUMN ADDRESS — All the bits $A_0 \sim A_7$ are defined by latching levels on $A_0 \sim A_7$ pins in a high-to-low transition of $\overline{CAS}$.

DESCRIPTION (Continued)

By using a 16-bit address latched into the on-chip address buffers by means of the above operation, any of 64K memory cells can be read/written into/from.

(B) $\overline{\text{RFSH}}$ Test Read-Modify-Write Cycle

Also, Read-Modify-Write Operation (not only the above normal Read/Write Operations) can be used in this $\overline{\text{RFSH}}$ Counter Test Cycle.

(C) Example of Refresh Counter Test Procedure

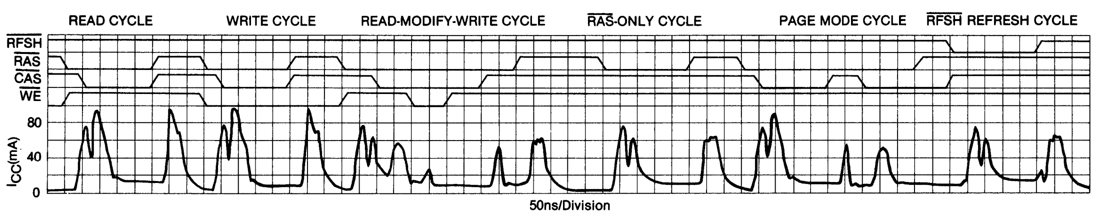
(1) Initialize the internal refresh counter. For this operation, 8 $\overline{\text{RFSH}}$ cycles are required.

(2) Write a test pattern of "0"s into the memory cells at a single column address and 128 row addresses by using 128 RFSH Test Write Cycle or RFSH Test Read-Modify-Write Cycle. (At this time, A_7 (row) must be fixed at "H" or "L".).

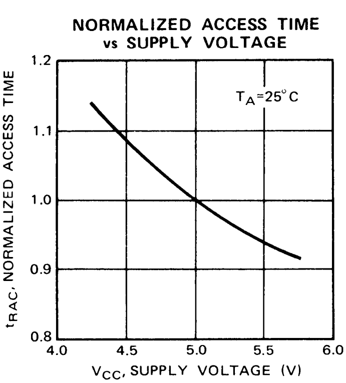
(3) Verify the data written into the memory cells in the above step (2) by using the column address used in step (2) and sequence through 128 row address combinations ($A_0 \sim A_6$) by means of normal Read Cycle. (At this time, A_7 (row) must be fixed at the same level as the above step (3).)

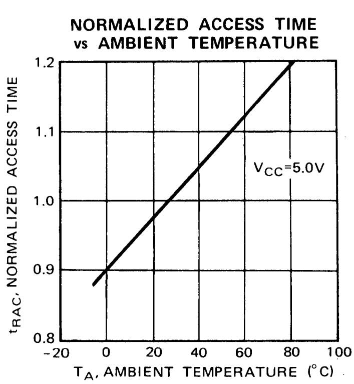
(4) Compliment the test pattern and repeat steps (2) and (3).

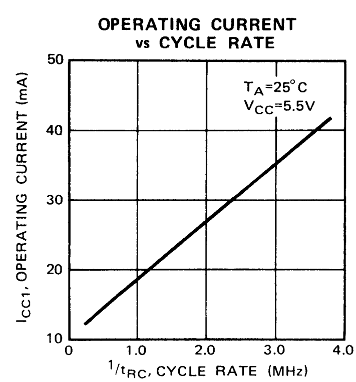
CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

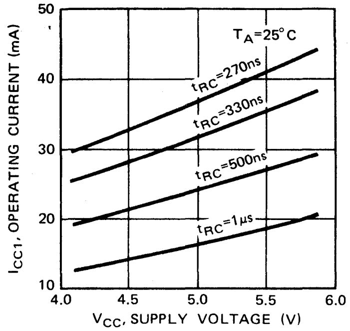




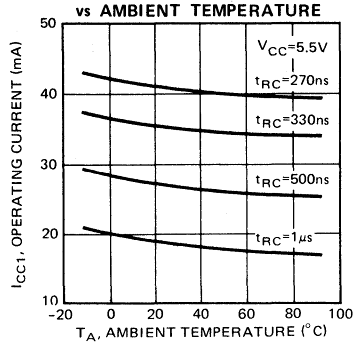


TYPICAL CHARACTERISTICS CURVES (Continued)

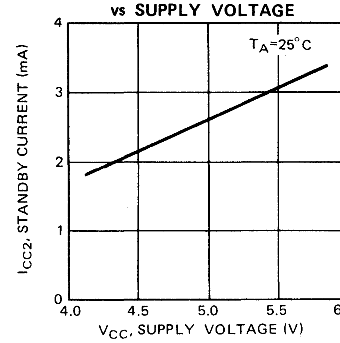
OPERATING CURRENT vs SUPPLY VOLTAGE



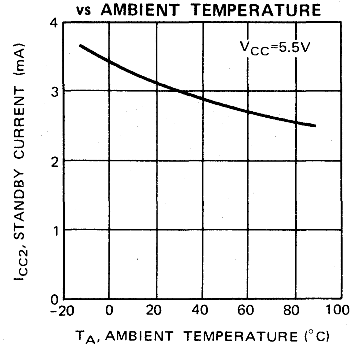
OPERATING CURRENT vs AMBIENT TEMPERATURE



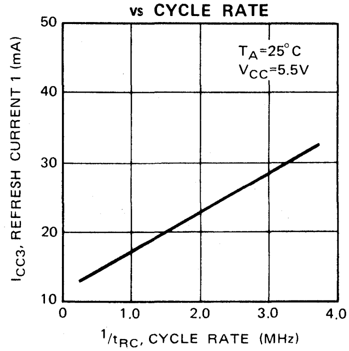
STANDBY CURRENT vs SUPPLY VOLTAGE



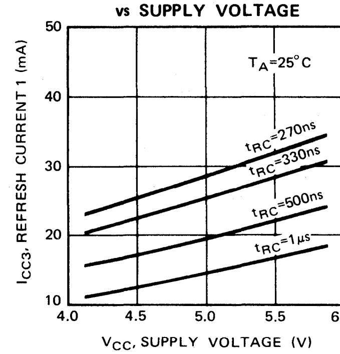
STANDBY CURRENT vs AMBIENT TEMPERATURE



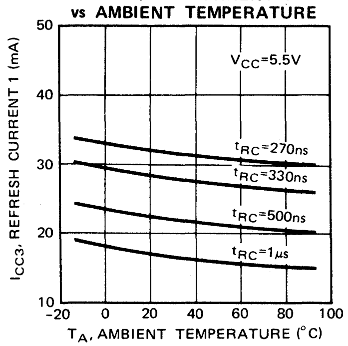
REFRESH CURRENT 1 vs CYCLE RATE



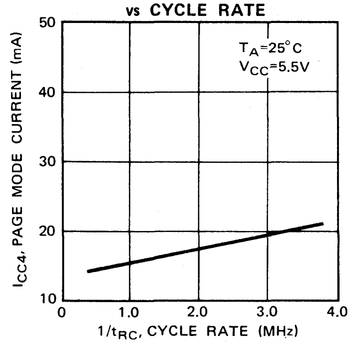
REFRESH CURRENT 1 vs SUPPLY VOLTAGE



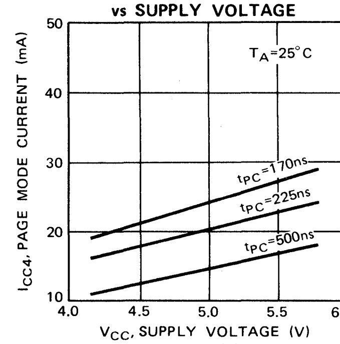
REFRESH CURRENT 1 vs AMBIENT TEMPERATURE



PAGE MODE CURRENT vs CYCLE RATE

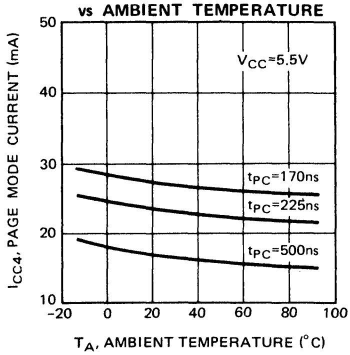


PAGE MODE CURRENT vs SUPPLY VOLTAGE

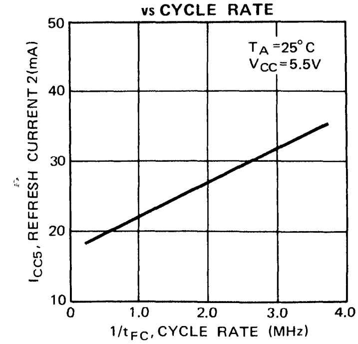


TYPICAL CHARACTERISTICS CURVES (Continued)

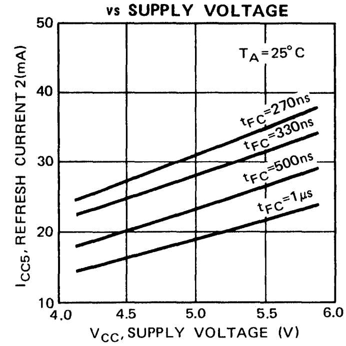
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



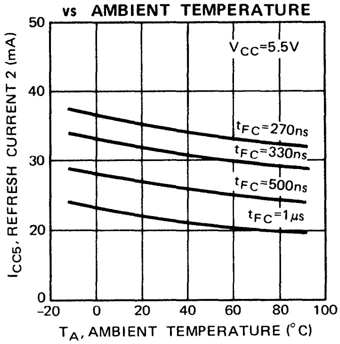
REFRESH CURRENT 2 vs CYCLE RATE



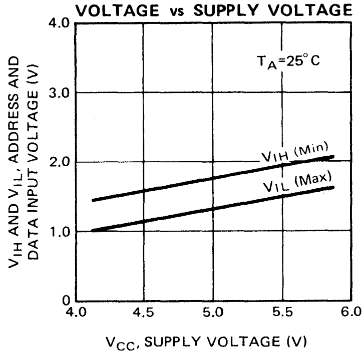
REFRESH CURRENT 2 vs SUPPLY VOLTAGE



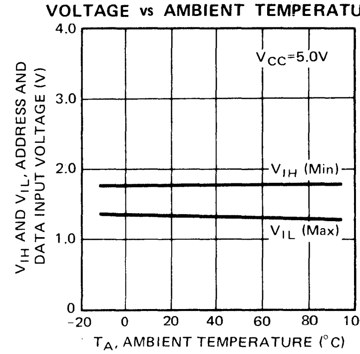
REFRESH CURRENT 2 vs AMBIENT TEMPERATURE



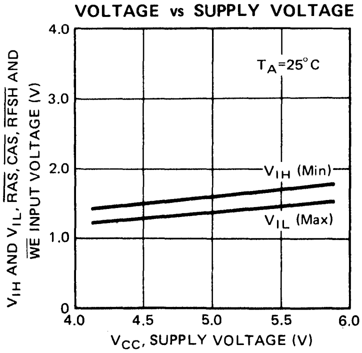
ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE



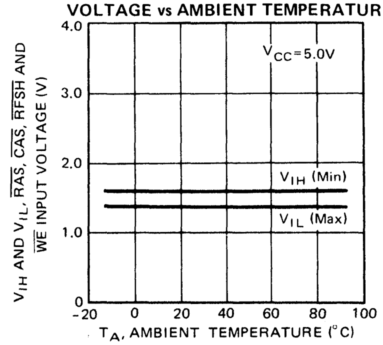
ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$, $\overline{RFSH}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

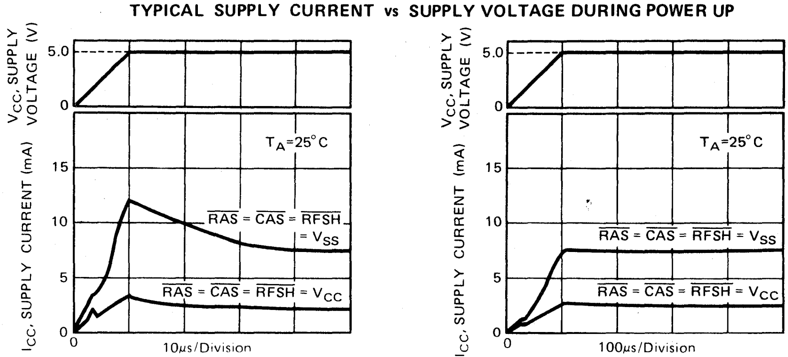


$\overline{RAS}$, $\overline{CAS}$, $\overline{RFSH}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

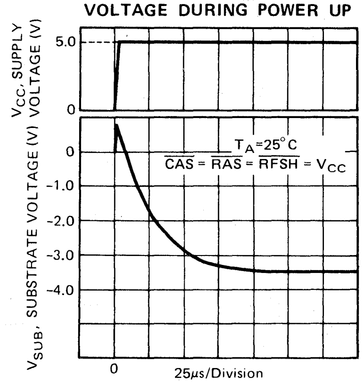


TYPICAL CHARACTERISTICS CURVES (Continued)

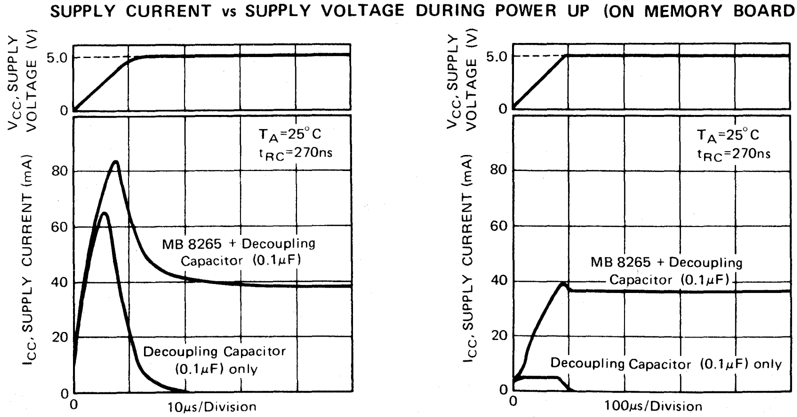
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP



SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE DURING POWER UP



SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP (ON MEMORY BOARD)



FUJITSU
MICROELECTRONICS, INC.

MB8265A-10
MB8265A-12
MB8265A-15

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

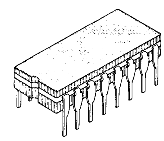
DESCRIPTION

The Fujitsu MB8265A is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

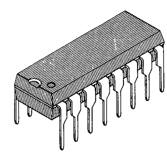
Multiplexed row and column address inputs permit the MB82645 to be housed in a standard 16-pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MB8265A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including dynamic sense amplifiers.

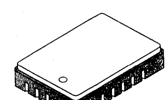
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs and output are TTL compatible.



CERAMIC PACKAGE CERDIP DIP-16C-C04



PLASTIC PACKAGE DIP-16P-M03

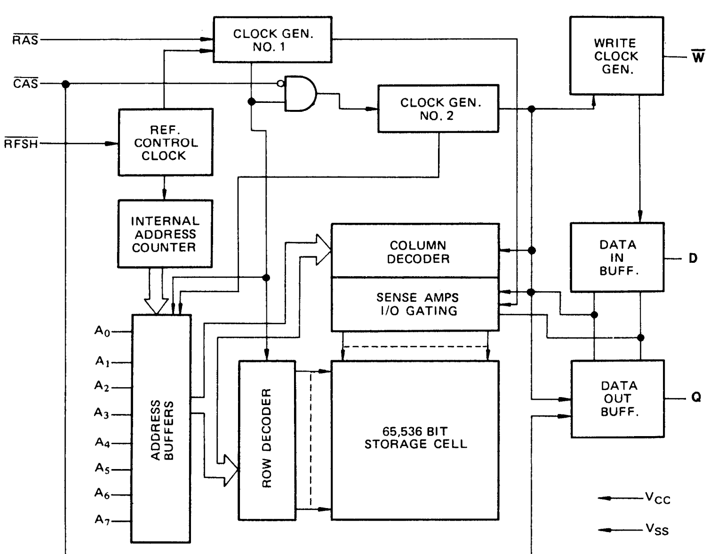


CERAMIC LCC LCC-18C-F02

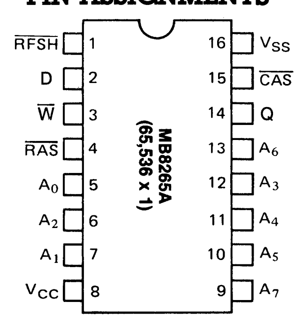
FEATURES

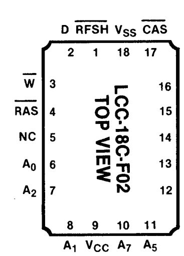
- **65,536 x 1-bit organization**
- **Row Access Time/Cycle Time**
  - **MB8265A-10 100 ns Max./200 ns Min.**
  - **MB8265A-12 120 ns Max./230 ns Min**
  - **MB8265A-15 150 ns Max./260 ns Min.**
- **Low Maximum Power Dissipation**
  - **MB8265A-10 275 mW (Active)**
  - **MB8265A-12 248 mW (Active)**
  - **MB8265A-15 220 mW (Active)**
  - **All devices 25 mW (Standby)**
- **Single +5V supply voltage, ±10% tolerance**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write capability**
- **Page Mode capability for faster access**
- **"Gated" $\overline{CAS}$**
- **On-chip Address and Data-in latches**
- **On-chip substrate bias generator**
- **t_{AR}, t_{WCR}, t_{DHR} eliminated**
- **Pin 1 on-chip refresh**
- **$\overline{RAS}$ only refresh**
- **Hidden refresh**
- **2ms/128 cycle refresh**

MB8265A BLOCK DIAGRAM



PIN ASSIGNMENTS





Note: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data in, $\overline{W}$ = Write Enable, Q = Data Out.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all Inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all Inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance $A_0 \sim A_7$, D	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{RFSH}$	C_{IN2}	—	—	8	pF
Output Capacitance Q	C_{OUT}	—	—	7	pF

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8265A-10		MB8265A-12		MB8265A-15		Unit
		Min	Max	Min	Max	Min	Max	
OPERATING CURRENT* Average power supply current ($\overline{RFSH}$ = V_{IH}, $\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}	—	50	—	45	—	40	mA
STANDBY CURRENT Power supply current ($\overline{RAS}$, $\overline{CAS}$, $\overline{RFSH}$ = V_{IH})	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$, $\overline{RFSH}$ = V_{IH}; $\overline{RAS}$ cycling, t_{RC} = min.)	I_{CC3}	—	38	—	35	—	31	mA
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{RFSH}$ = V_{IH}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}	—	35	—	32	—	28	mA
REFRESH CURRENT 2* Average power supply current ($\overline{RAS}/\overline{CAS}$ = V_{IH}, $\overline{RFSH}$ cycling; t_{FC} = min.)	I_{CC5}	—	42	—	38	—	34	mA
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT HIGH VOLTAGE (I_{OH} = −5 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V
OUTPUT LOW VOLTAGE (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB8265A-10 Min	MB8265A-10 Max	MB8265A-12 Min	MB8265A-12 Max	MB8265A-15 Min	MB8265A-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV	—	2	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	230	—	265	—	280	—	ns
Page Mode Read/Write Cycle Time		t_{PC}	TCELCEL	105	—	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	135	—	155	—	180	—	ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	50	—	60	—	75	—	ns
$\overline{CAS}$ Precharge Time (all cycles except page mode)		t_{CPN}	TCEHCEL	25	—	30	—	30	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	TCEHCEL	45	—	50	—	60	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	100	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	4 7	t_{RCD}	TRELCEL	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	TCEHREL	0	—	0	—	0	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Write Command Set Up Time	8	t_{WCS}	TWLCEL	0	—	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	20	—	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	20	—	25	—	30	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	35	—	40	—	45	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	35	—	40	—	45	—	ns
Data In Set Up Time		t_{DS}	TDVREL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	20	—	25	—	30	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay	8	t_{CWD}	TCELWL	40	—	50	—	60	—	ns
$\overline{RAS}$ to $\overline{W}$ Delay	8	t_{RWD}	TRELWL	90	—	110	—	120	—	ns
$\overline{RFSH}$ Set Up Time Referenced to $\overline{RAS}$		t_{FSR}	TFHREL	90	—	100	—	100	—	ns
$\overline{RAS}$ to $\overline{RFSH}$ Delay		t_{FRD}	TREHFL	90	—	100	—	100	—	ns
$\overline{RFSH}$ Cycle Time		t_{FC}	TFLFL	200	—	230	—	260	—	ns
$\overline{RFSH}$ Pulse Width		t_{FP}	TFLFH	100	—	120	—	150	—	ns
$\overline{RFSH}$ Inactive Time		t_{FI}	TFHFL	90	—	100	—	100	—	ns
$\overline{RFSH}$ to $\overline{RAS}$ Delay	10	t_{FRD}	TREHFL	20	—	30	—	40	—	ns
$\overline{RFSH}$ Hold Time	10	t_{FSH}	TRELFH	30	—	40	—	50	—	ns

See Notes on following page.

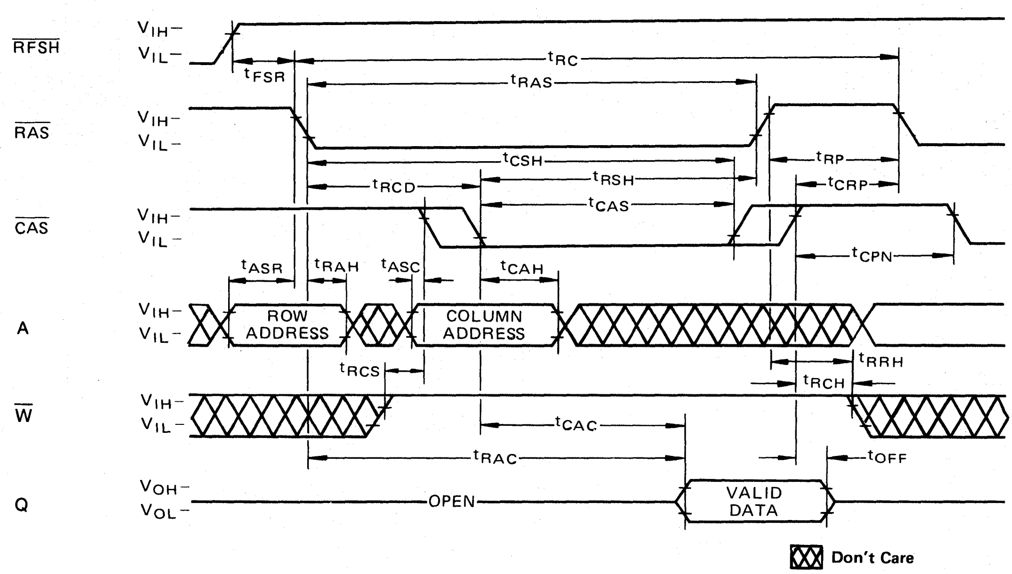
***These symbols are described in IEEE Std. 662-1980: IEEE Standard Terminology for Semiconductor Memory.**

Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RFSH}$ cycles before proper device operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 active $\overline{RFSH}$ initialization cycles are required. The internal refresh counter must be activated a minimum of 128 times every 2ms if the $\overline{RFSH}$ refresh function is used. $\overline{RFSH}$ must be held at V_{IH} if the $\overline{RFSH}$ function is not used.
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max) the specified maximum valve of t_{RAC} (max) can be met. If $t_{RCD} > t_{RCD}$ (max) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5ns) + t_{ASC} (min).
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. $\overline{RFSH}$ counter test read/write cycle only.

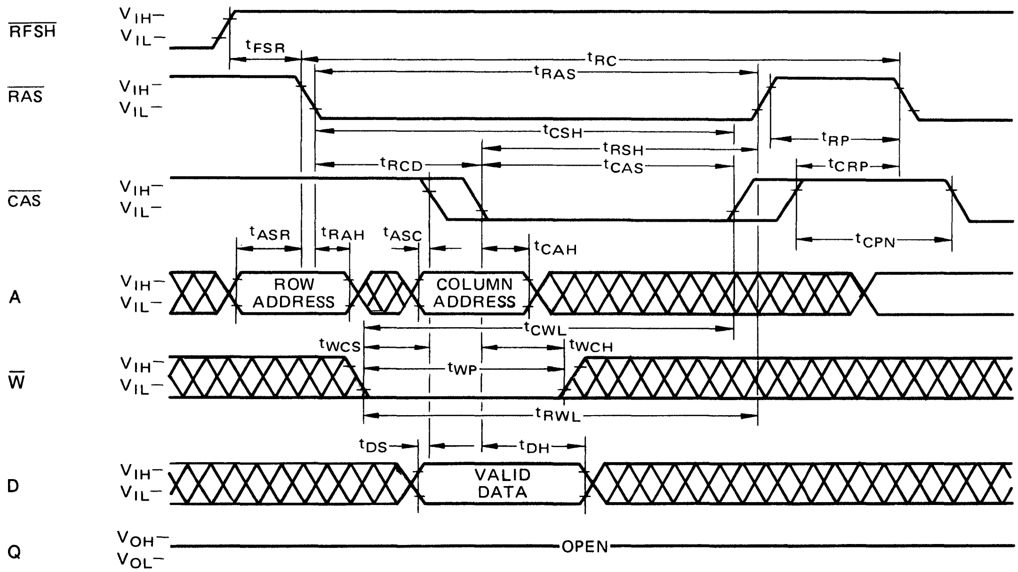
TIMING DIAGRAMS

READ CYCLE

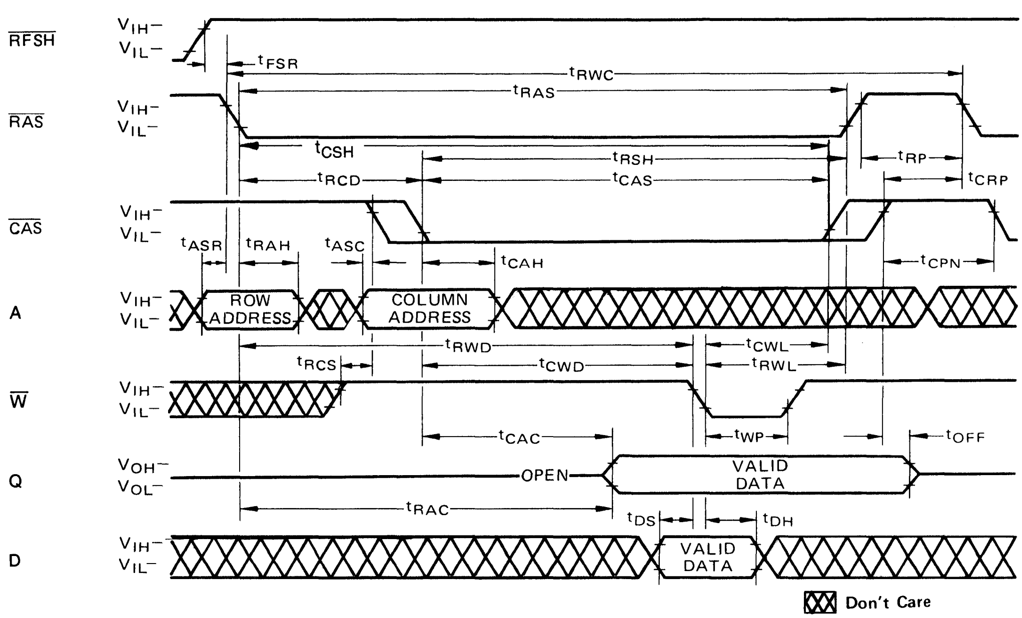


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

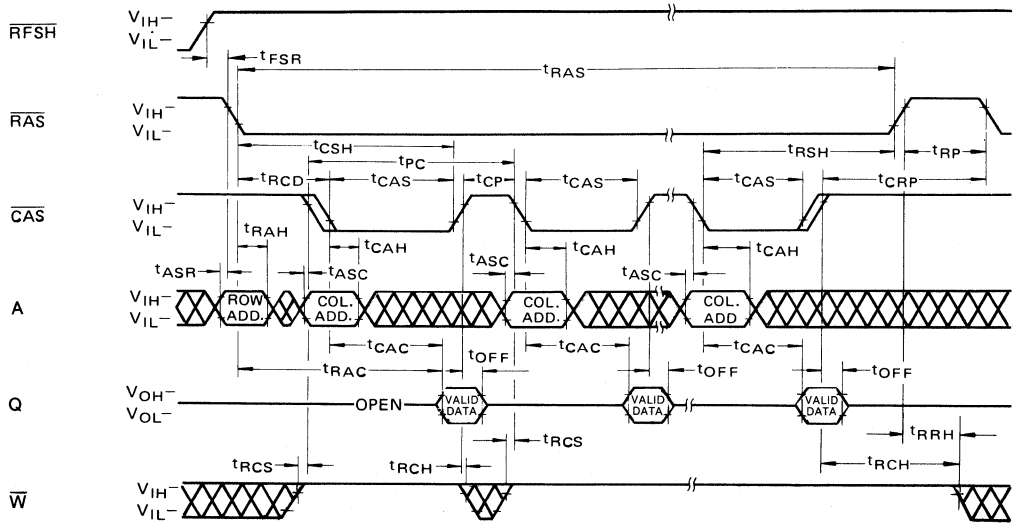


READ-WRITE/READ-MODIFY-WRITE CYCLE

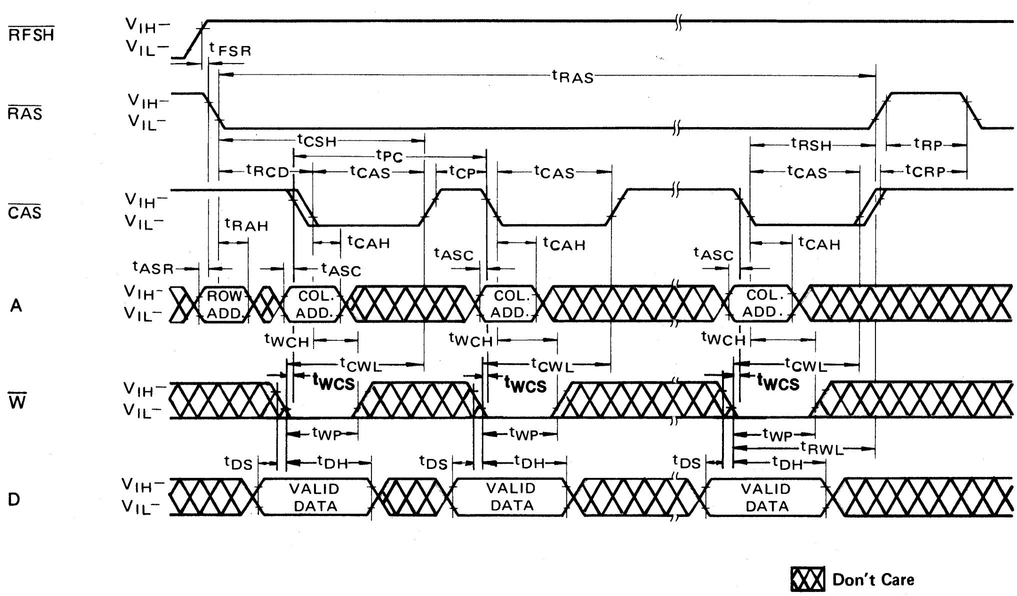


TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE

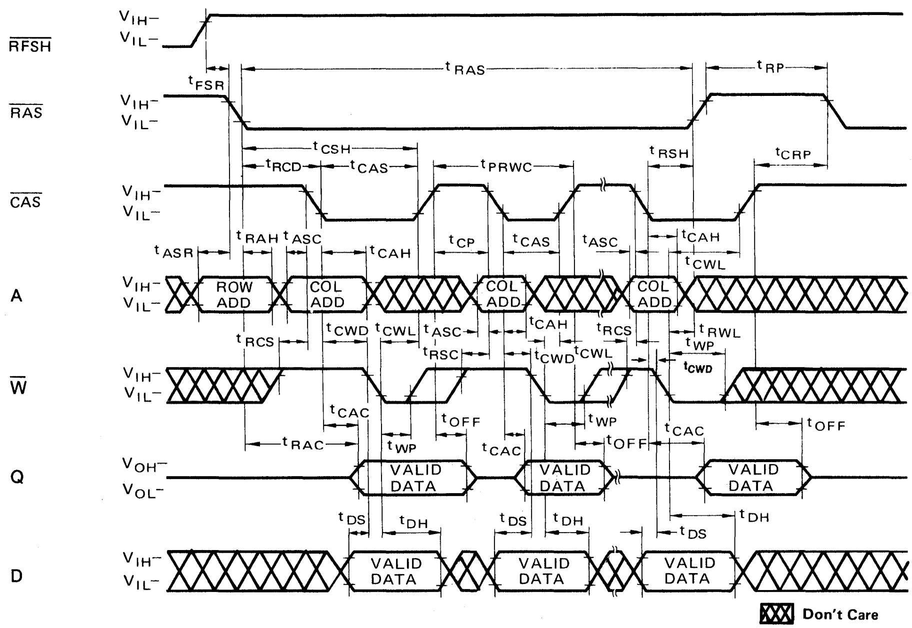


PAGE MODE WRITE CYCLE



TIMING DIAGRAMS (Continued)

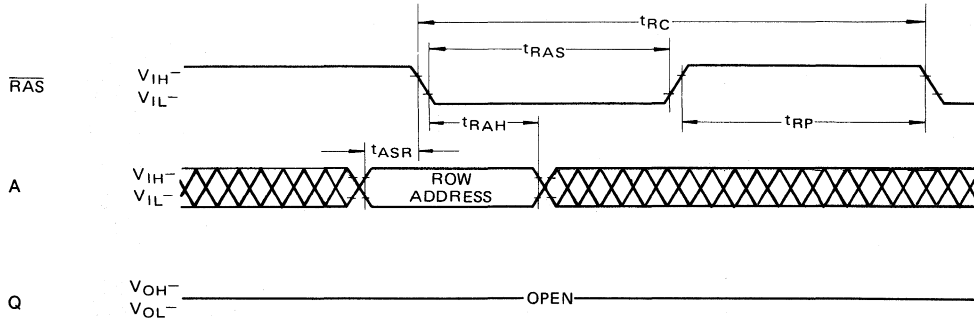
PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

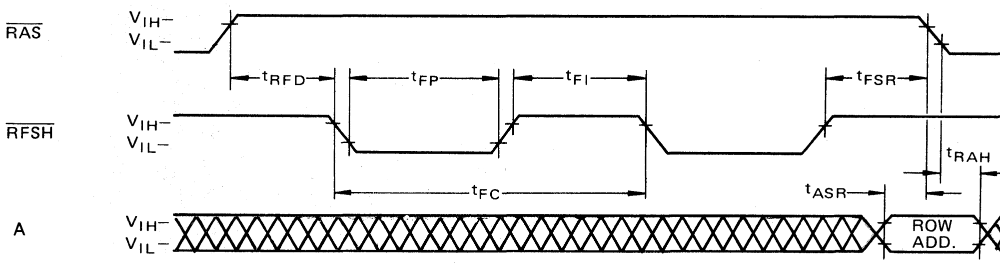
"$\overline{RAS}$-ONLY" REFRESH CYCLE

NOTE: $\overline{RFSH} = V_{IH}$; $\overline{CAS} = V_{IH}$; $\overline{W}$, D = Don't Care

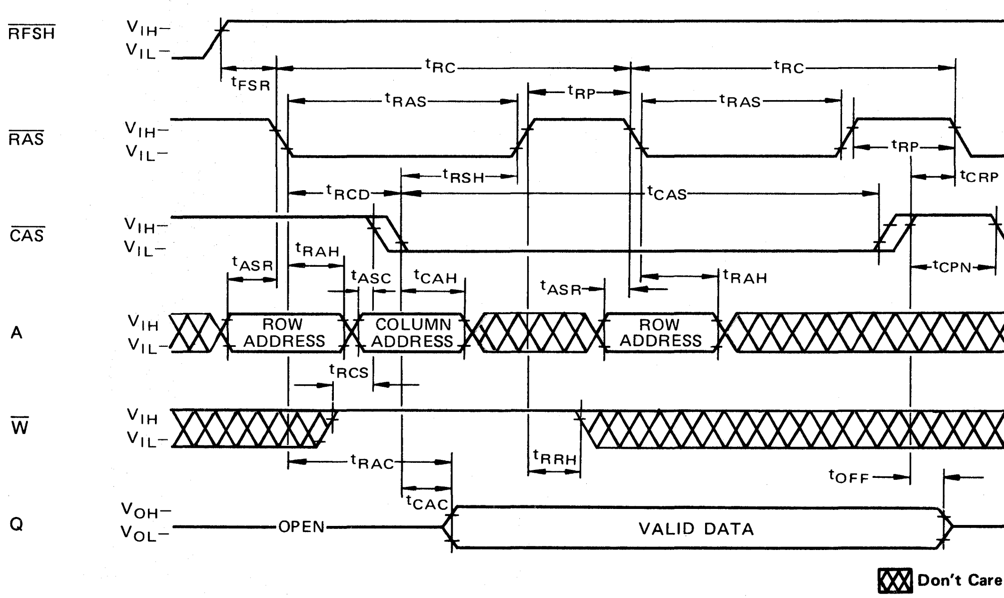


$\overline{RFSH}$ REFRESH CYCLE

NOTE: $\overline{CAS} = V_{IH}$; $\overline{W}$, D = Don't Care; Q = Open

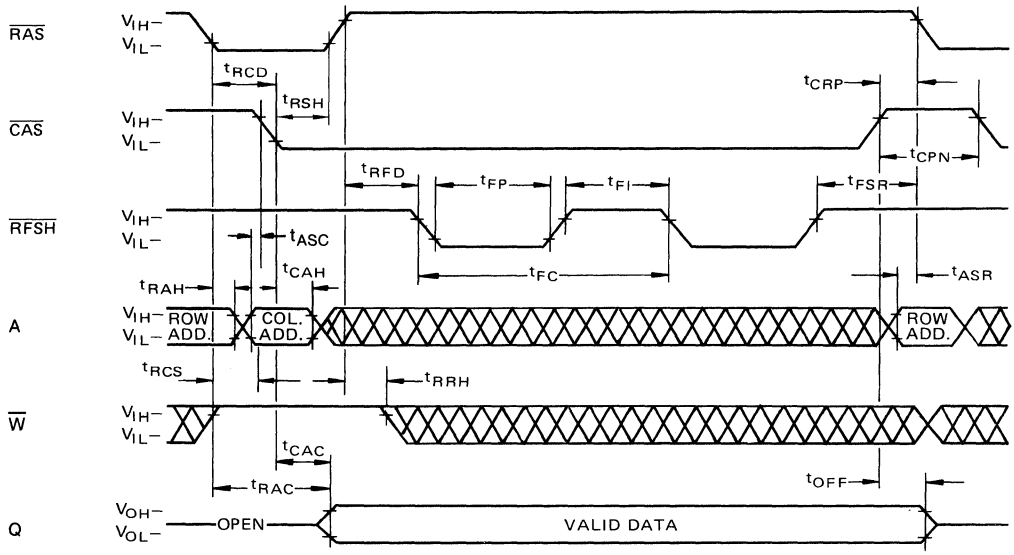


HIDDEN "$\overline{RAS}$-ONLY" REFRESH CYCLE



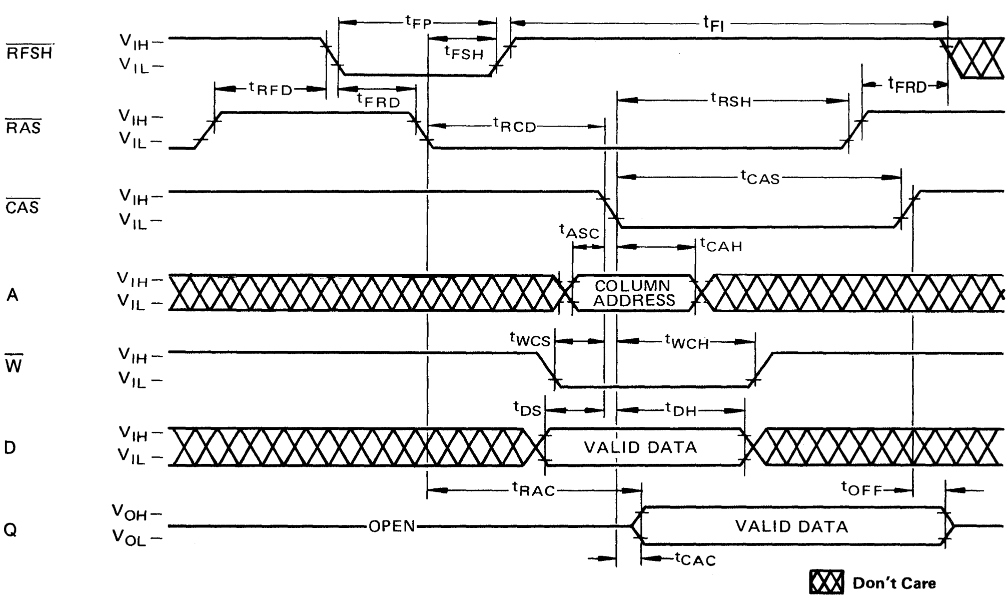
TIMING DIAGRAMS (Continued)

HIDDEN $\overline{RFSH}$ REFRESH CYCLE



$\overline{RFSH}$ COUNTER TEST READ/WRITE CYCLE

NOTE: Q is the waveform in Read or Read-Modify-Write Cycles



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any one of 65536 storage cell locations within the MB8265A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic high (1) on $\overline{W}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8265A during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data In (D) register. In a write cycle, if $\overline{W}$ is brought low (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from the transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode

Page mode operation permits strobing the row-address into the MB8265A while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{RFSH}$ Refresh

$\overline{RFSH}$ type refreshing available on the MB8265A offers an alternate refresh method: (1) When $\overline{RFSH}$ (pin 1) is brought low (active) when $\overline{RAS}$ (Pin 4) is high (inactive), on-chip refresh control clock generators and a refresh address counter are enabled and an internal refresh operation takes place. (2) When $\overline{RFSH}$ is brought high (inactive), the internal refresh address counter is automatically incremented in preparation for the next $\overline{RFSH}$ refresh cycle. Only $\overline{RFSH}$ activated cycles affect the internal address counter.

The use of $\overline{RFSH}$ type refreshing eliminates the need of providing any additional external devices to generate refresh addresses.

Hidden Refresh

A Hidden Refresh Cycle may take place while maintaining valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle.

The MB8265A offers two types of Hidden Refresh. They are referred to as Hidden $\overline{RAS}$-Only Refresh and Hidden $\overline{RFSH}$ Refresh.

1) Hidden $\overline{RAS}$-Only Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing "$\overline{RAS}$-Only" refresh, but with $\overline{CAS}$ held low. $\overline{RFSH}$ has to be held at V_{IH}.

2) Hidden $\overline{RFSH}$ Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RFD}), executing $\overline{RFSH}$ refresh, but with $\overline{CAS}$ held low.

A specified precharge period (t_{CPN}) is required before normal memory Read, Write or Read-Modify-Write cycle after performing either type of Hidden Refresh.

Refresh Counter Test Cycle

A special timing sequence provides a convenient method of verifying the functionality of the $\overline{RFSH}$ activated circuitry.

(A) $\overline{RFSH}$ Test Read/Write Cycle

When $\overline{RFSH}$ is given an input signal as shown in the $\overline{RFSH}$ counter test Read/Write cycle timing diagram, a Read/Write Operation is enabled. A memory cell can be accessed with an address consisting of 8 row and 8 column bits defined as follows:

*ROW ADDRESS—Bits $A_0 \sim A_6$ are defined when the contents of the internal address counter are latched. (The other bit, A_7, is set "low" internally.

*COLUMN ADDRESS—All the bits $A_0 \sim A_7$ are defined by latching levels on $A_0 \sim A_7$ pins in a high-to-low transition of $\overline{CAS}$.

By using a 15-bit address latched into the on-chip address buffers by means of the above operation, any of 32K (in the fixed half cell array) memory cells can be read or written.

(B) $\overline{RFSH}$ Test Using the Read Modify Write Cycle

In addition to the normal read or write operations, a read-modify-write operation can be used in this $\overline{RFSH}$ Counter Test.

(C) Example of the Refresh Counter Test Procedure

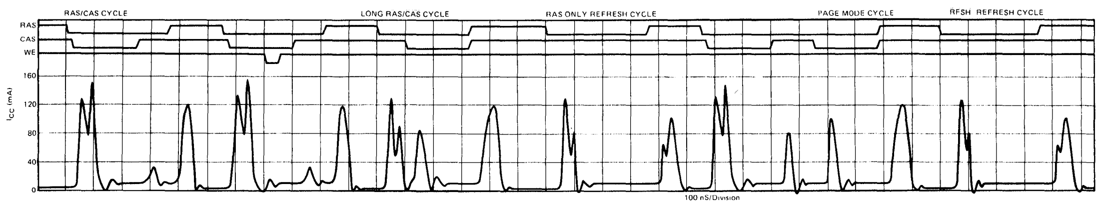
(1) Initialize the internal refresh counter. For this operation, 8 $\overline{RFSH}$ cycles are required.

(2) Write a test pattern of "0"s into memory cells at a single column address and 128 row adresses by using 128 $\overline{RFSH}$ Test Write Cycles or $\overline{RFSH}$ Test Read-Modify-Write Cycles.

(3) Verify the data written into the memory cells in step (2) above by using the column address used in step (2) and sequence through 128 row address combinations ($A_0 \sim A_6$) by means of the normal Read Cycle.

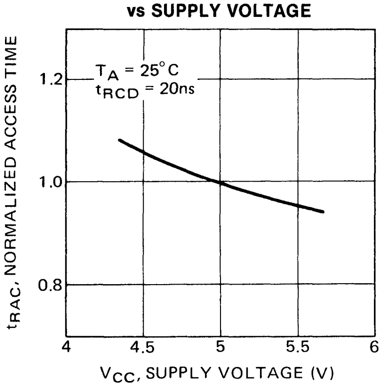
(4) Compliment the test pattern and repeat the steps (2) and (3).

CURRENT WAVEFORM (V_{CC} = 5.5V, TA = 25 °C)

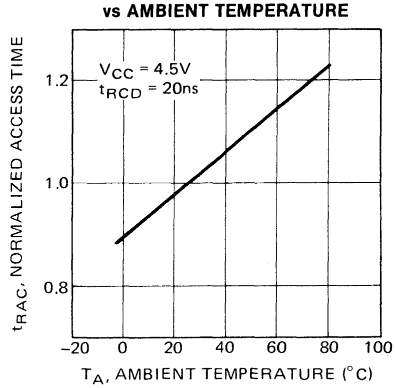


TYPICAL CHARACTERISTICS CURVES

NORMALIZED ACCESS TIME
vs SUPPLY VOLTAGE

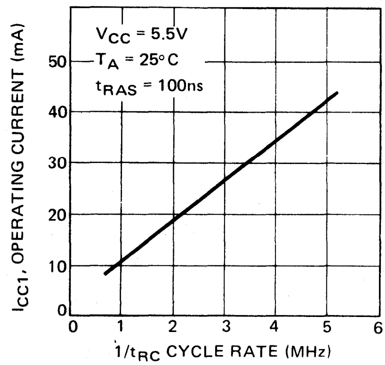


NORMALIZED ACCESS TIME
vs AMBIENT TEMPERATURE

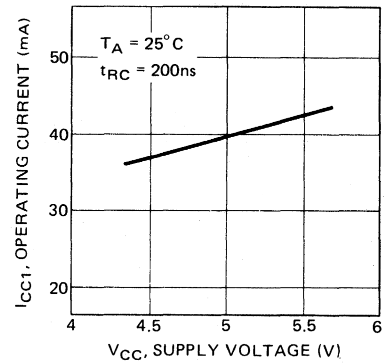


TYPICAL CHARACTERISTICS CURVES (Continued)

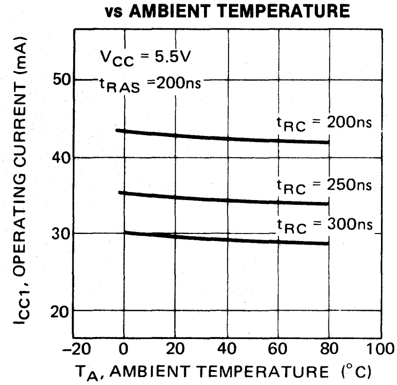
OPERATING CURRENT vs CYCLE RATE



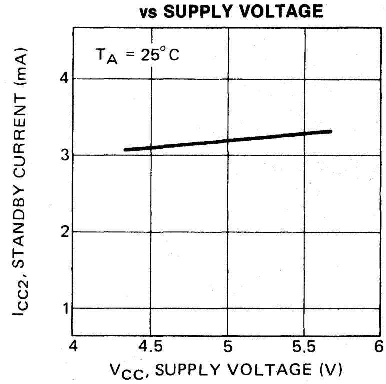
OPERATING CURRENT vs SUPPLY VOLTAGE



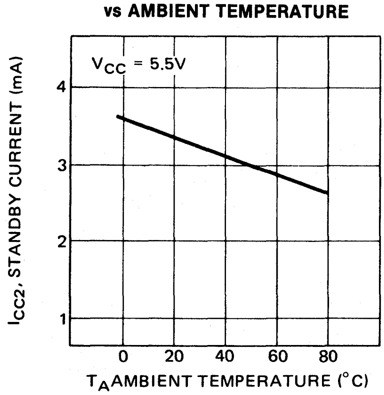
OPERATING CURRENT vs AMBIENT TEMPERATURE



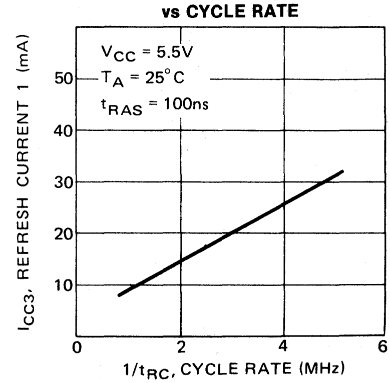
STANDBY CURRENT vs SUPPLY VOLTAGE



STANDBY CURRENT vs AMBIENT TEMPERATURE

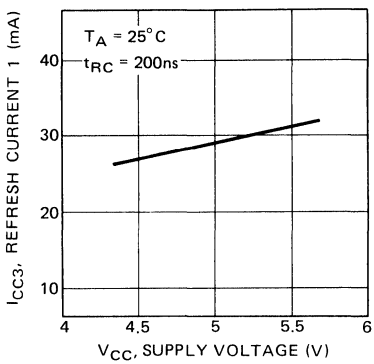


REFRESH CURRENT 1 vs CYCLE RATE

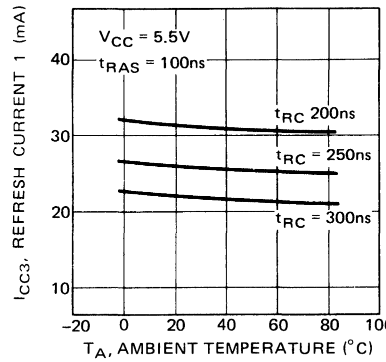


TYPICAL CHARACTERISTICS CURVES (Continued)

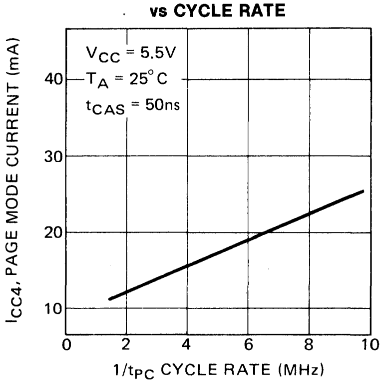
REFRESH CURRENT 1 vs SUPPLY VOLTAGE



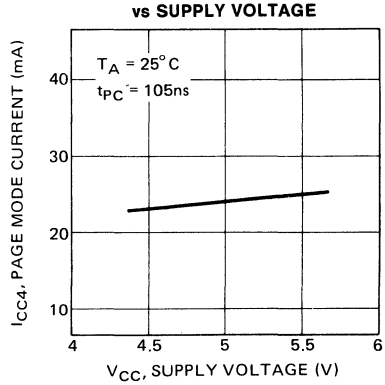
REFRESH CURRENT 1 vs AMBIENT TEMPERATURE



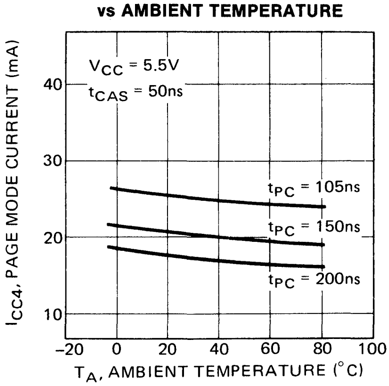
REFRESH CURRENT vs CYCLE RATE



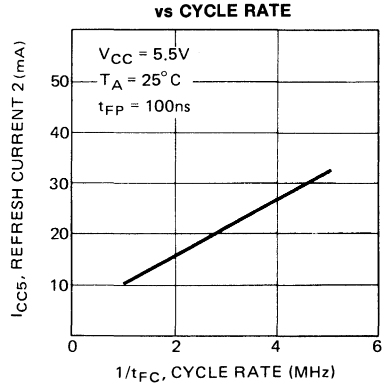
PAGE MODE CURRENT vs SUPPLY VOLTAGE



PAGE MODE CURRENT vs AMBIENT TEMPERATURE

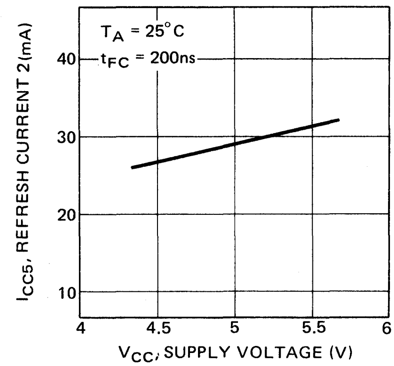


REFRESH CURRENT 2 vs CYCLE RATE

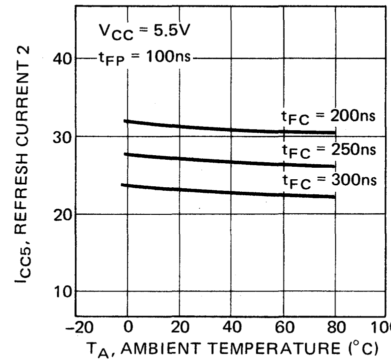


TYPICAL CHARACTERISTICS CURVES (Continued)

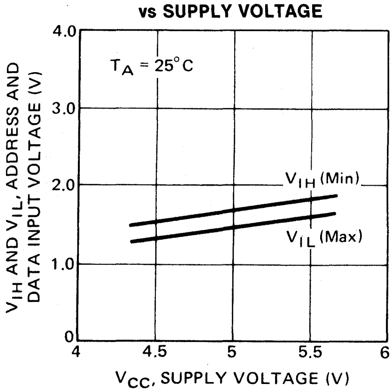
REFRESH CURRENT 2 vs SUPPLY VOLTAGE



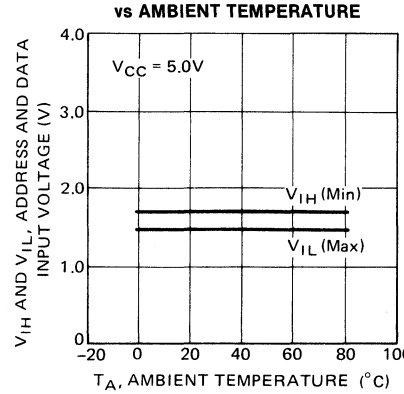
REFRESH CURRENT 2 vs AMBIENT TEMPERATURE



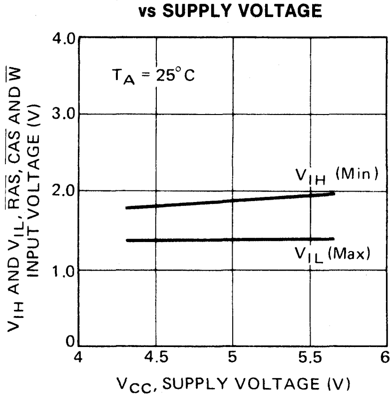
ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE



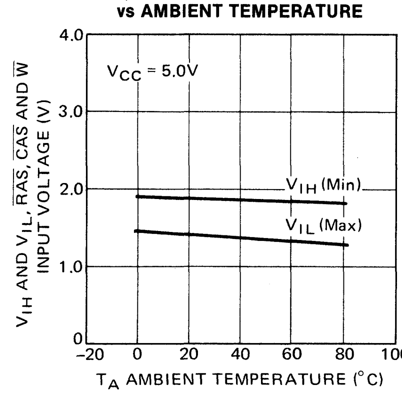
ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

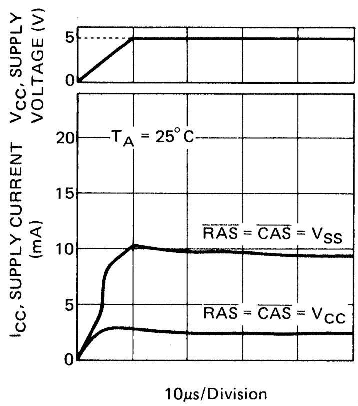


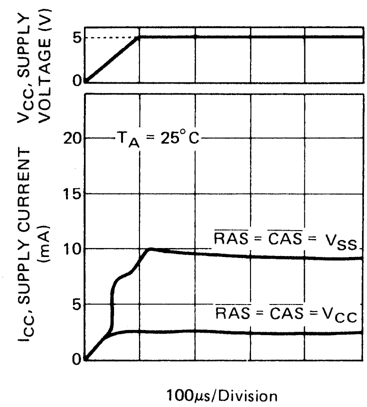
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE



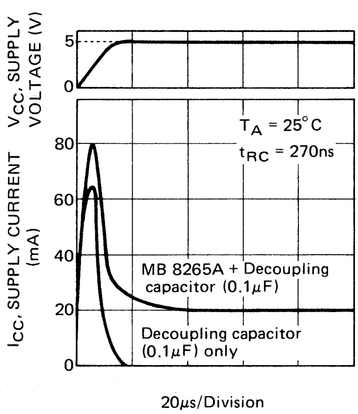
TYPICAL CHARACTERISTICS CURVES (Continued)

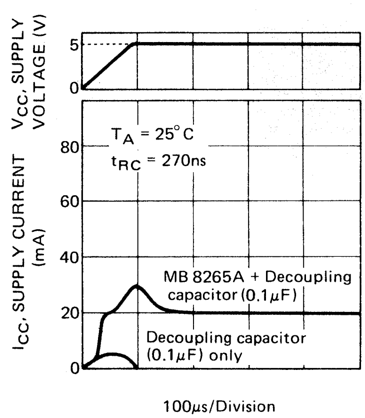
CURRENT WAVEFORM DURING POWER UP



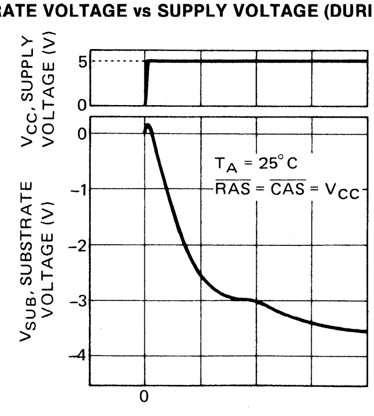


CURRENT WAVEFORM DURING POWER UP (ON MEMORY BOARD)





SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE (DURING POWER UP)



FUJITSU
MICROELECTRONICS, INC.

MB8266A-10
MB8266A-12
MB8266A-15

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

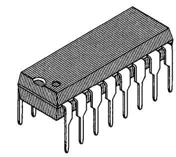
DESCRIPTION

The Fujitsu MB8266A is a fully decoded dynamic NMOS random access memory organized as 65,536 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

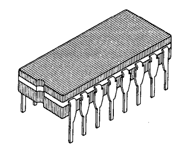
The MB8266A offers new functional enhancements that make it more versatile than previous dynamic RAMS. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability that is compatible with upward expansion to 256K dynamic RAMS, since pin 1 is left as a "no connect". The MB8266A also features Nibble Mode, which allows high speed serial access to up to four bits of data. Multiplexed row and column address inputs permit the MB8266A to be housed in a Jedec standard 16-pin DIP and 18-pad LCC.

The MB8266A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including sense amplifiers.

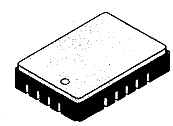
Clock timing requirements are non-critical and the power supply tolerance is very wide. All inputs and output are TTL compatible.



PLASTIC PACKAGE
DIP-16P-M03



CERDIP PACKAGE
DIP-16C-C04

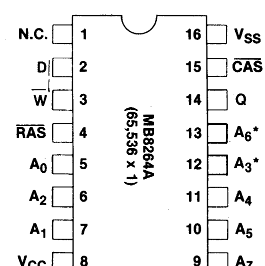


CERAMIC LCC
LCC-18C-F02

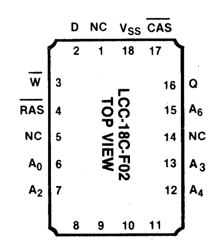
FEATURES

- **65,536 x 1-bit organization**
- **Row Access Time/Cycle Time**
  - **MB8266A-10 100 ns Max./200 ns Min.**
  - **MB8266A-12 120 ns Max./230 ns Min.**
  - **MB8266A-15 150 ns Max./260 ns Min.**
- **Nibble Access Time/Cycle Time**
  - **MB8266A-10 25 ns Max./60 ns Min.**
  - **MB8266A-12 30 ns Max./70 ns Min.**
  - **MB8266A-15 40 ns Max./90 ns Min.**
- **Low Maximum Power Dissipation**
  - **MB8266A-10 275 mW (Active)**
  - **MB8266A-12 248 mW (Active)**
  - **MB8266A-15 220 mW (Active)**
  - **All devices 25 mW (Standby) Max.**
- **Single +5V supply voltage, ±10% tolerance**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Nibble mode capability for faster access**
- **$\overline{CAS}$ before $\overline{RAS}$ on chip refresh**
- **$\overline{RAS}$ only refresh**
- **Hidden $\overline{CAS}$ before $\overline{RAS}$ on chip refresh**
- **2ms/128 cycle refresh**
- **Read-Modify-Write capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows two-dimensional chip select**
- **On-chip Address and Data-in latches**
- **On-chip substrate bias generator**
- **t_{AR}, t_{WCR}, t_{DHR} eliminated**

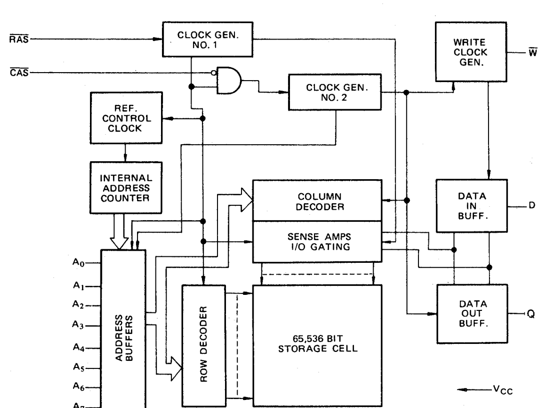
PIN ASSIGNMENTS



***A_3 and A_6 assigned for Nibble Address**



MB8266A BLOCK DIAGRAM



Note: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data in, $\overline{W}$ = Write Enable, Q = Data Out.

ABSOLUTE MAXIMUM RATING (See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short circuit output current		I_{OS}	50	mA

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Ambient Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance $A_0 \sim A_7$, D	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}	—	—	8	pF
Output Capacitance Q	C_{OUT}	—	—	7	pF

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8266A-10		MB8266A-12		MB8266A-15		Unit
		Min	Max	Min	Max	Min	Max	
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	I_{CC1}	—	50	—	45	—	40	mA
STANDBY CURRENT Power supply current ($\overline{RAS}$/$\overline{CAS}$ = V_{IH})	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	I_{CC3}	—	38	—	35	—	31	mA
NIBBLE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min)	I_{CC4}	—	21	—	21	—	21	mA
REFRESH CURRENT 2* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$-before-RAS)	I_{CC5}	—	42	—	38	—	34	mA
INPUT LEAKAGE CURRENT any input ($0 \le V_{IN} \le 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \le V_{OUT} \le 5.5V$)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT HIGH VOLTAGE (I_{OH} = −5 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V
OUTPUT LOW VOLTAGE (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V

Note: I_{CC} is dependent on output loading cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS (Recommended operating conditons unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB8266A-10 Min	MB8266A-10 Max	MB8266A-12 Min	MB8266A-12 Max	MB8266A-15 Min	MB8266A-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV	—	2	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	230	—	265	—	280	—	ns
Access Time from $\overline{\text{RAS}}$	4 6	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{\text{CAS}}$	5 6	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn Off Delay		t_{OFF}	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		t_{T}	TT	3	50	3	50	3	50	ns
$\overline{\text{RAS}}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{\text{RAS}}$ Pulse Width		t_{RAS}	TRELREH	100	10000	120	10000	150	10000	ns
$\overline{\text{RAS}}$ Hold Time		t_{RSH}	TCELREH	50	—	60	—	75	—	ns
$\overline{\text{CAS}}$ Precharge Time		t_{CP}	TCEHCEL	50	—	50	—	55	—	ns
$\overline{\text{CAS}}$ Pulse Width		t_{CAS}	TCELCEH	50	10000	60	10000	75	10000	ns
$\overline{\text{CAS}}$ Hold Time		t_{CSH}	TRELCEH	100	—	120	—	150	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	4 7	t_{RCD}	TRELCEL	20	50	20	60	25	75	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Set Up Time		t_{CRS}	TCEHREL	30	—	30	—	30	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	9	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	9	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Write Command Set Up Time		t_{WCS}	TWLCEL	0	—	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	20	—	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	20	—	25	—	30	—	ns
Write Command to $\overline{\text{RAS}}$ Lead Time		t_{RWL}	TWLREH	35	—	40	—	45	—	ns
Write Command to $\overline{\text{CAS}}$ Lead Time		t_{CWL}	TWLCEH	35	—	40	—	45	—	ns
Data In Set Up Time		t_{DS}	TDVREL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	20	—	25	—	30	—	ns
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ Delay	8	t_{CWD}	TCELWL	40	—	50	—	60	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ Delay	8	t_{RWD}	TRELWL	90	—	110	—	120	—	ns
$\overline{\text{CAS}}$ Set Up Time Referenced to $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)		t_{FCS}	TCELREL	20	—	25	—	30	—	ns
$\overline{\text{CAS}}$ Hold Time Referenced to $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)		t_{FCH}	TRELCEX	20	—	25	—	30	—	ns
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time		t_{RPC}	TREHCEL	20	—	20	—	20	—	ns
Nibble Mode Read/Write Cycle Time		t_{NC}	TCEHCEH	60	—	70	—	90	—	ns
Nibble Mode Read-Write Cycle Time		t_{NRWC}	TCEHCEH	75	—	90	—	120	—	ns
Nibble Mode Access Time		t_{NCAC}	TCELQV	—	25	—	30	—	40	ns
Nibble Mode $\overline{\text{CAS}}$ Pulse Width		t_{NCAS}	TCELCEH	25	—	30	—	40	—	ns
Nibble Mode $\overline{\text{CAS}}$ Precharge Time		t_{NCP}	TCEHCEL	25	—	30	—	40	—	ns
Nibble Mode Read $\overline{\text{RAS}}$ Hold Time		t_{NRRSH}	TCELREH	25	—	30	—	40	—	ns
Nibble Mode Write $\overline{\text{RAS}}$ Hold Time		t_{NWRSH}	TCELREH	35	—	40	—	45	—	ns
Nibble Mode Write Command to $\overline{\text{CAS}}$ Lead Time		t_{NCWL}	TWLCEH	20	—	25	—	35	—	ns
Nibble Mode Write Command Set Up Time		t_{NWCS}	TWLCEL	0	—	0	—	0	—	ns
Nibble Mode $\overline{\text{CAS}}$ to $\overline{\text{W}}$ Delay		t_{NCWD}	TCELWL	15	—	20	—	30	—	ns
Refresh Counter Test Cycle Time	10	t_{RTC}	TRELREL	300	—	350	—	405	—	ns
Refresh Counter Test $\overline{\text{RAS}}$ Pulse Width	10	t_{TRAS}	TRELREH	200	—	240	—	295	—	ns

See Notes on following page.

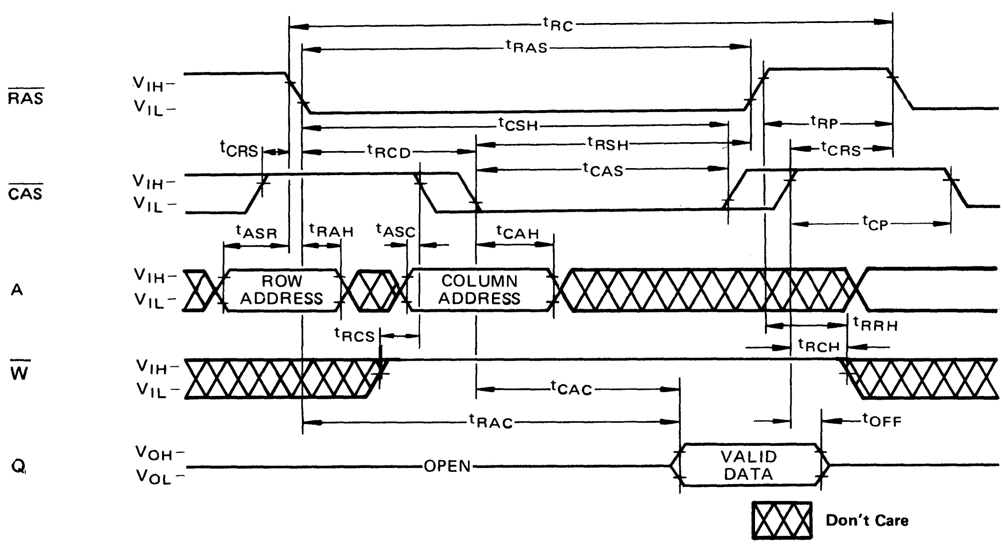
***These symbols are described in IEEE STD 662-1980: IEEE Standard Terminology for Semiconductor Memory.**

Notes:

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. (If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.)
2. Dynamic measurements assume t_T = 5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max) the specified maximum value of t_{RAC} (max) can be met. If $t_{RCD} > t_{RCD}$ (max) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5ns) + t_{ASC} (min).
8. t_{WCS}, t_{CWD} and t_{RWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Refresh counter test cycle only.

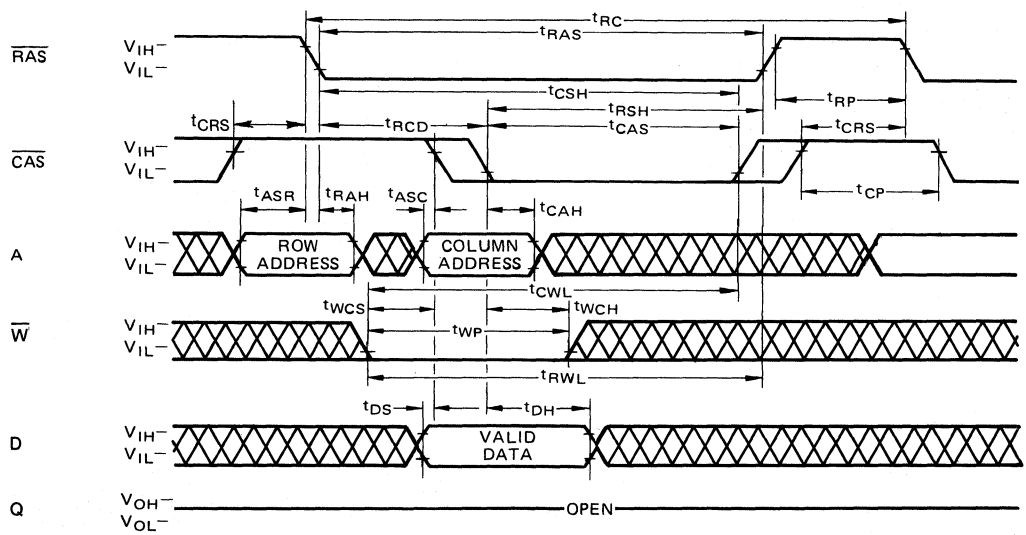
TIMING DIAGRAMS

READ CYCLE

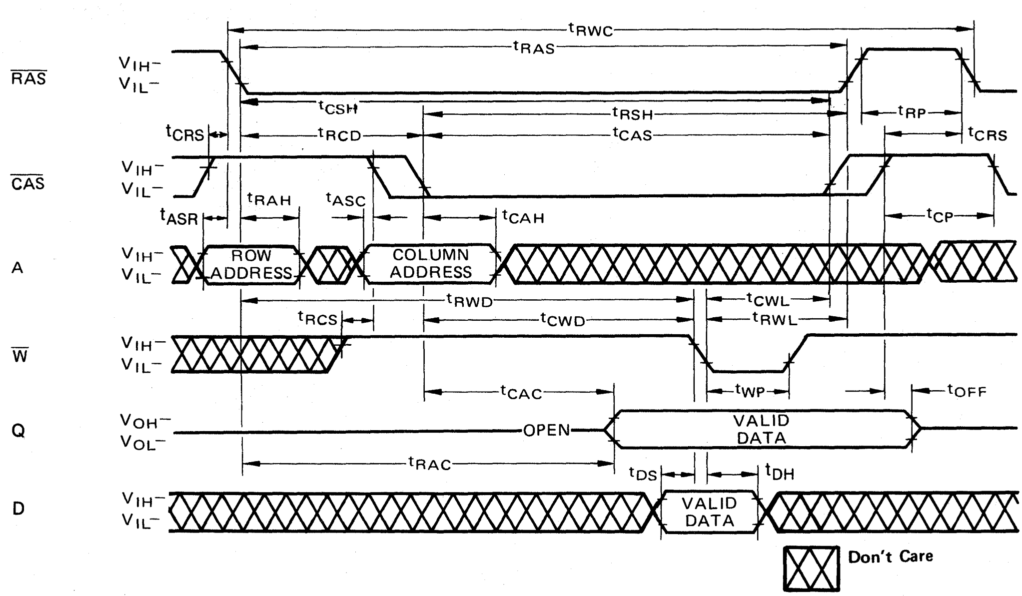


TIMING DIAGRAMS (Continued)

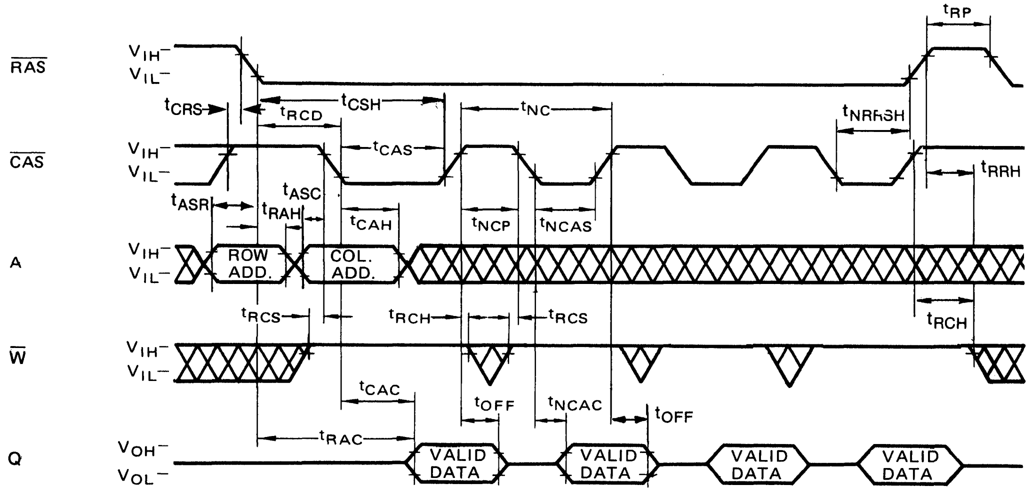
WRITE CYCLE (EARLY WRITE)



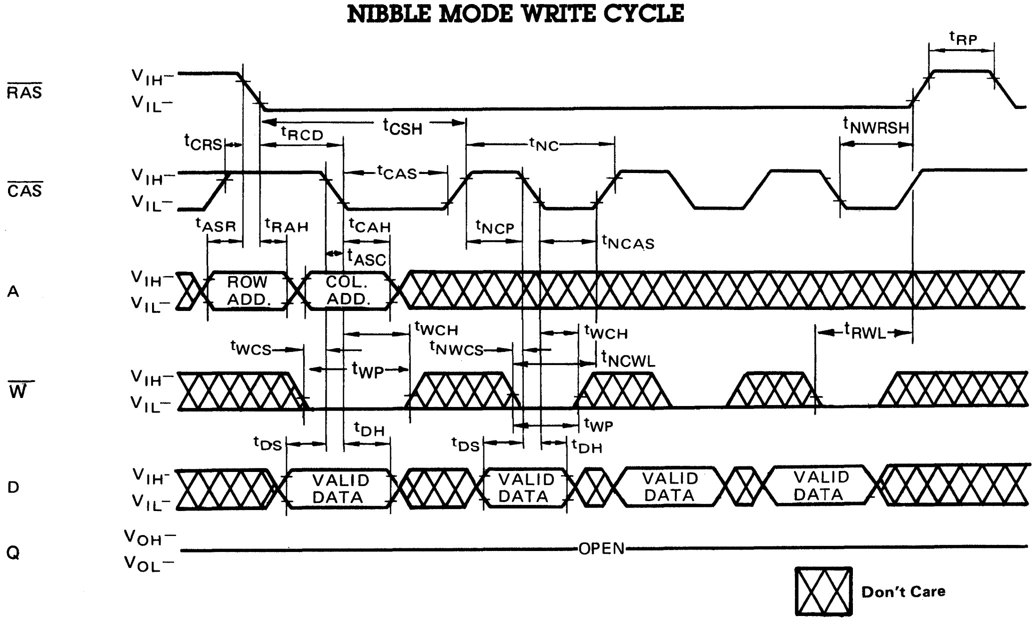
READ-WRITE/READ-MODIFY-WRITE CYCLE



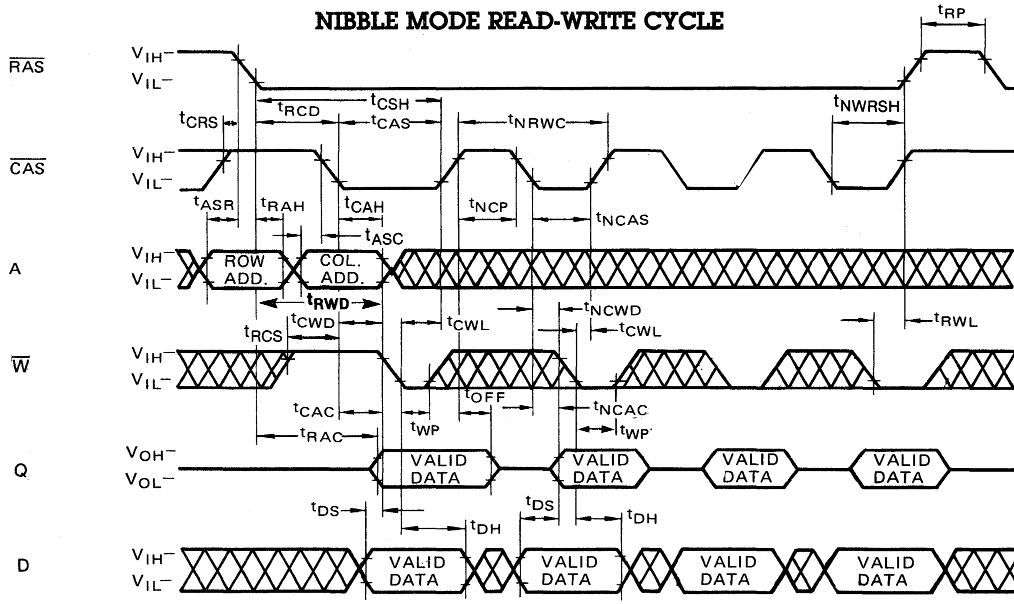
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE

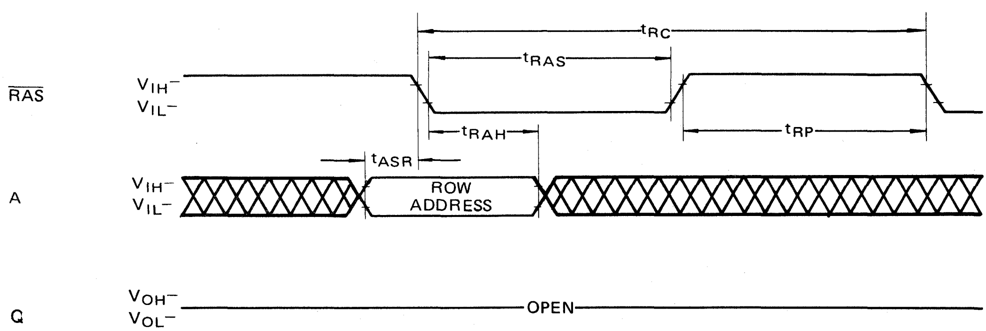


NIBBLE MODE READ-WRITE CYCLE



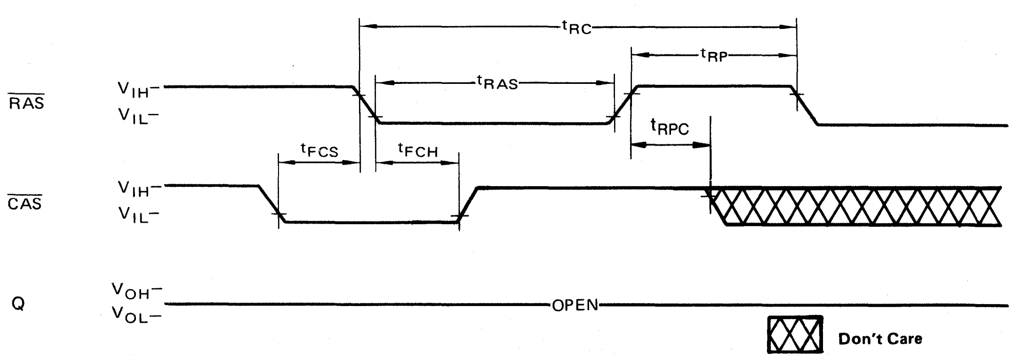
"RAS-ONLY" REFRESH CYCLE

Note: CAS = V_{IH}, W, D = Don't Care



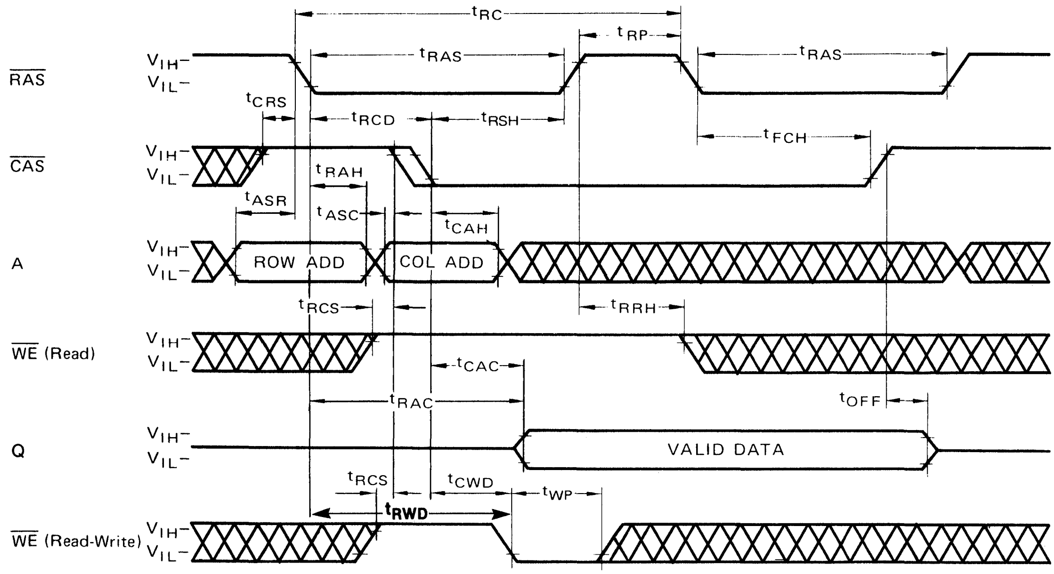
"CAS-BEFORE-RAS" REFRESH CYCLE

Note: A, W, D = Don't Care

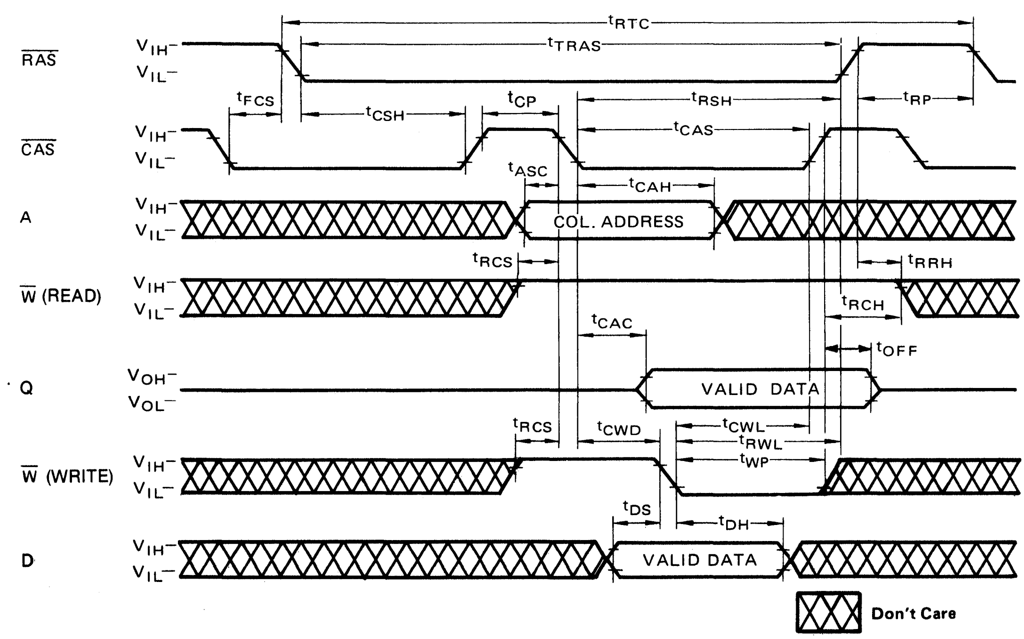


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB8266A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic high (1) on $\overline{W}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8266A during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data In (D) register. In a write cycle, if $\overline{W}$ is brought low (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ must be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Nibble Mode

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and 6 column addresses. The 2 column address bits (A_3, A_6) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes A_6 and A_3 to be incremented internally while all the other address bits are held constant thereby making the next nibble bit available for access. (See Table 1).

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, read, write, and read-modify-write operations may be performed in any desired combination.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB8266A offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh

A Hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ ar tive time. For the MB8266A, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh address as in a normal $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled. A memory cell can be addressed with 8 row address bits and 8 column address bits defined as follows:

- *A ROW ADDRESS—Bits A_0 through A_6 are defined by the refresh counter. The other bit A_7 is set "low" internally.
- *A COLUMN ADDRESS—All the bits A_0 through A_7 are defined by latching levels on A_0 through A_7 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

(1) Initialize the internal refresh counter. For this operation, 8 cycles are required.

(2) Write a test pattern of "low"s into the memory cells at a single column address and 128 row addresses.

(3) Using a read-modify-write cycle, read the "low" written at the last operation (Step (2)) and write a new "high" in the same cycle. This cycle is repeated 128 times, and "high"s are written into the 128 memory cells.

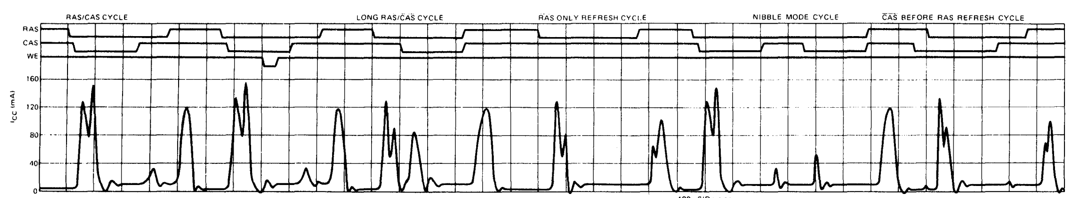
(4) Read the "high"s written at the last operation (Step (3)).

(5) Compliment the test pattern and repeat steps (2), (3) and (4).

NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

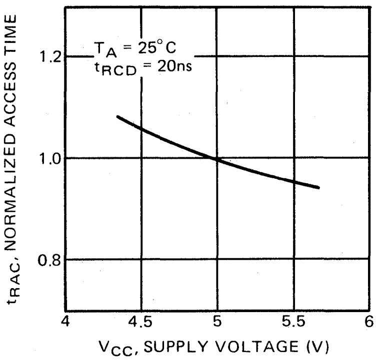
Sequence	Nibble Bit	Row Address	Column Address	A_3	A_6	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	10101010	101010	1	0	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	10101010	101010	1	1	generated internally
toggle $\overline{CAS}$ (nibble mode)	3	10101010	101010	0	0	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	10101010	101010	0	1	generated internally
toggle $\overline{CAS}$ (nibble mode)	1	10101010	101010	1	0	sequence repeats

CURRENT WAVEFORM (V_{CC} = 5.5V, TA = 25°C)

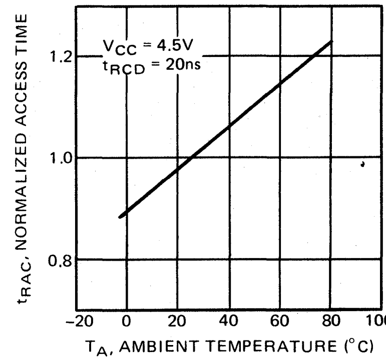


TYPICAL CHARACTERISTICS CURVES

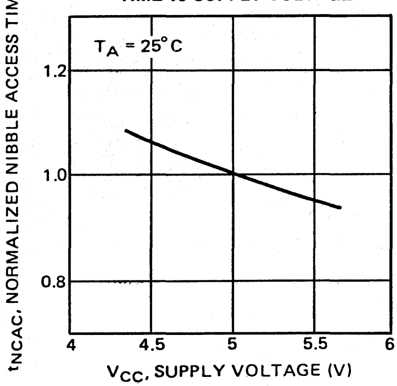
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



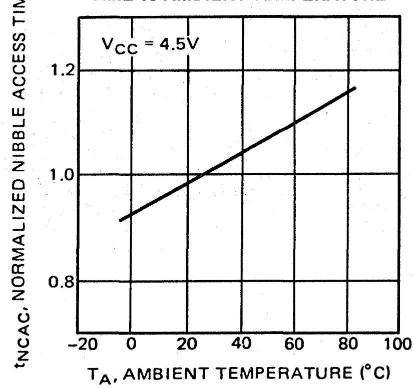
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



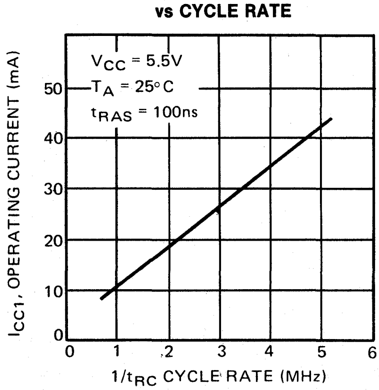
NORMALIZED NIBBLE ACCESS TIME vs SUPPLY VOLTAGE



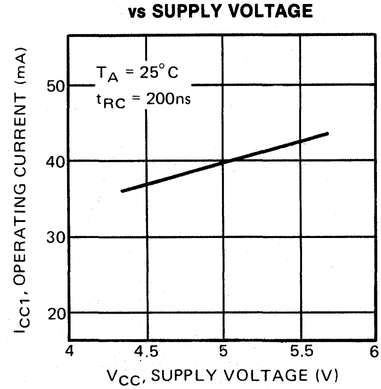
NORMALIZED NIBBLE ACCESS TIME vs AMBIENT TEMPERATURE



OPERATING CURRENT vs CYCLE RATE

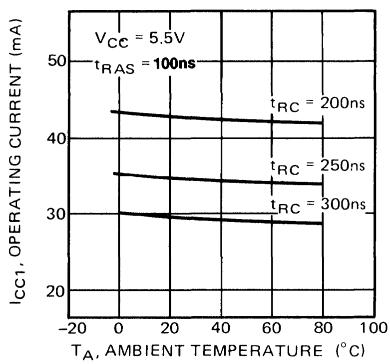


OPERATING CURRENT vs SUPPLY VOLTAGE

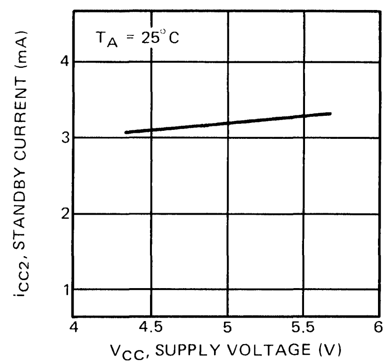


TYPICAL CHARACTERISTICS CURVES (Continued)

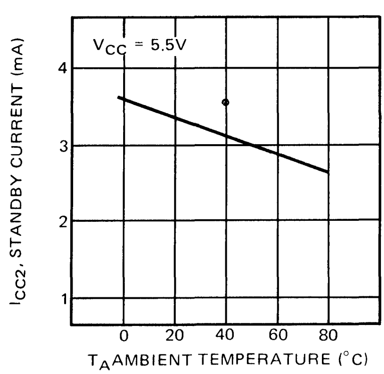
OPERATING CURRENT vs AMBIENT TEMPERATURE



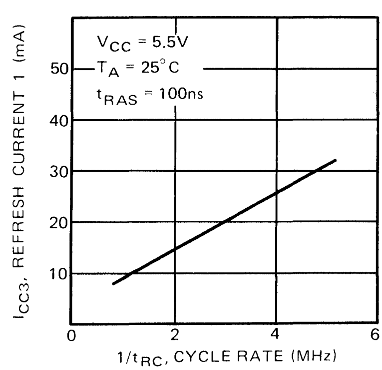
STANDBY CURRENT vs SUPPLY VOLTAGE



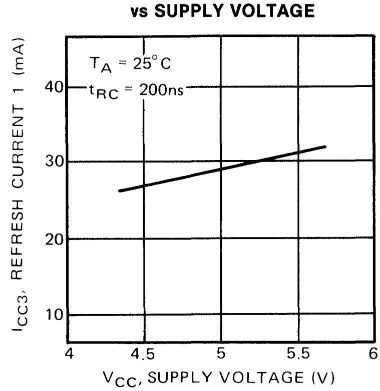
STANDBY CURRENT vs AMBIENT TEMPERATURE



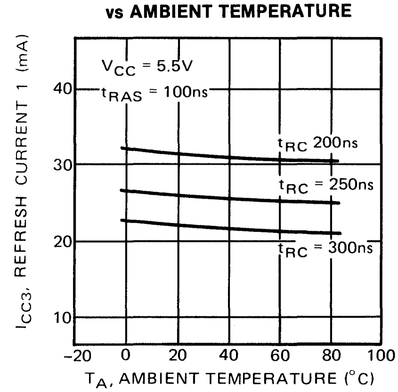
REFRESH CURRENT 1 vs CYCLE RATE



REFRESH CURRENT 1 vs SUPPLY VOLTAGE

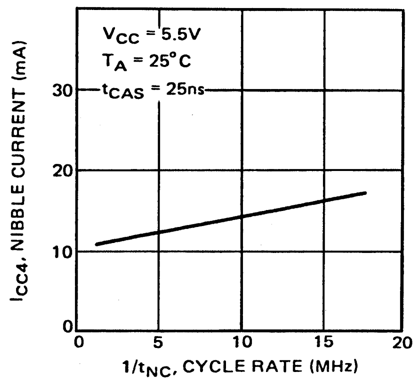


REFRESH CURRENT 1 vs AMBIENT TEMPERATURE

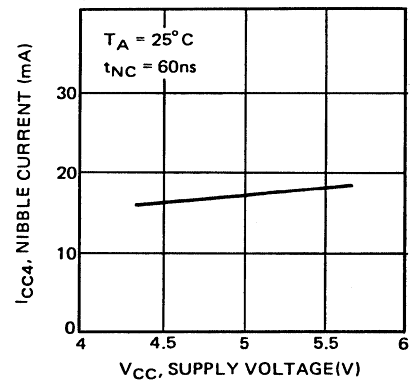


TYPICAL CHARACTERISTICS CURVES (Continued)

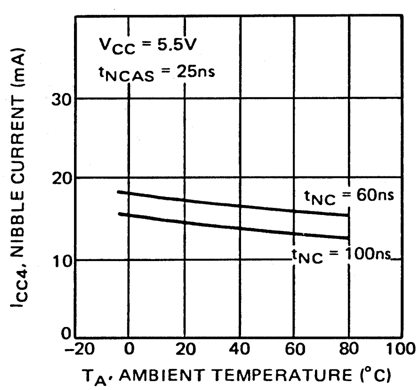
NIBBLE CURRENT vs CYCLE RATE



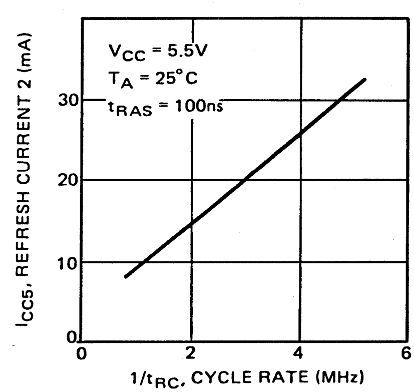
NIBBLE CURRENT vs SUPPLY CURRENT



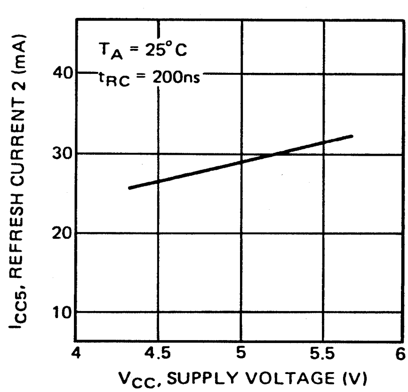
NIBBLE CURRENT vs AMBIENT TEMPERATURE



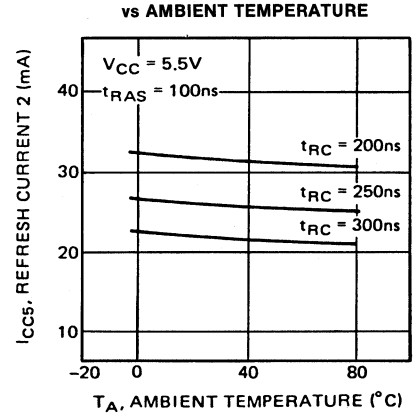
REFRESH CURRENT 2 vs CYCLE RATE



REFRESH CURRENT 2 vs SUPPLY VOLTAGE

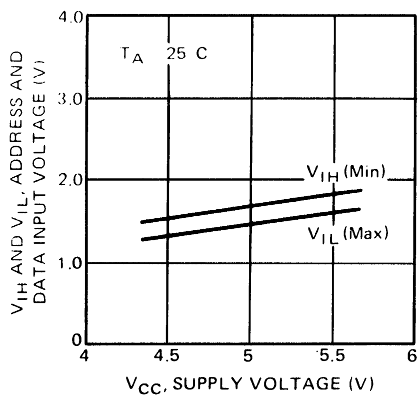


REFRESH CURRENT 2 vs AMBIENT TEMPERATURE

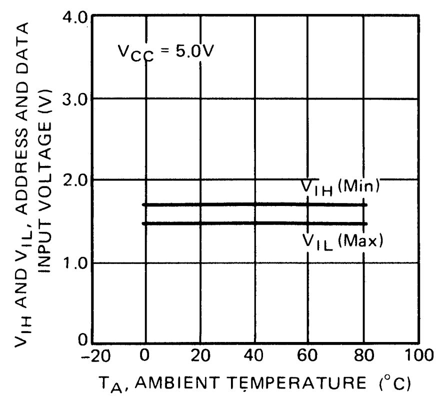


TYPICAL CHARACTERISTICS CURVES (Continued)

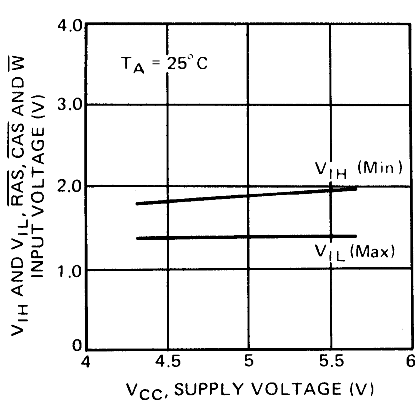
ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE



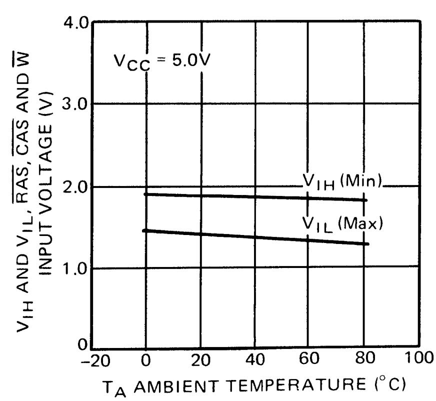
ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

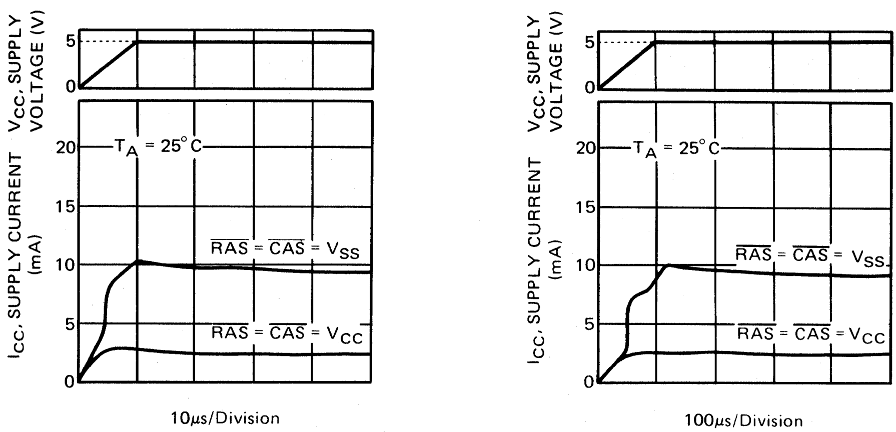


$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

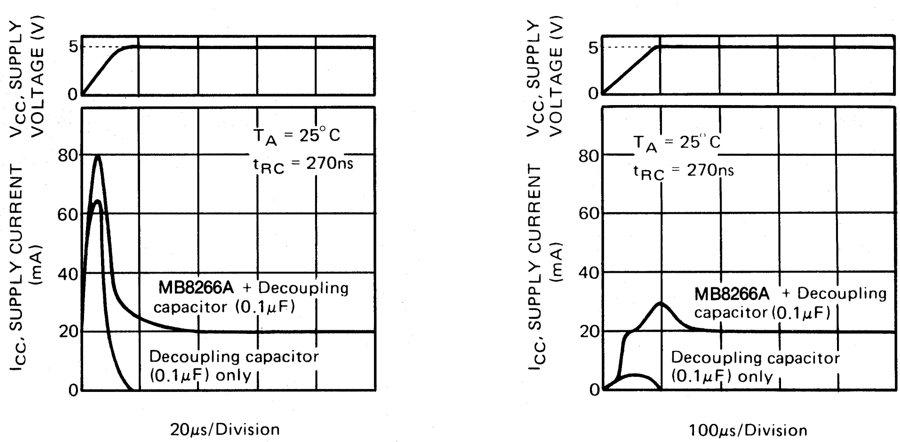


TYPICAL CHARACTERISTICS CURVES (Continued)

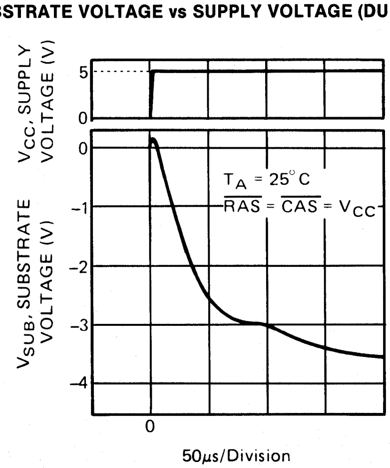
CURRENT WAVEFORM DURING POWER UP



CURRENT WAVEFORM DURING POWER UP (ON MEMORY BOARD)



SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE (DURING POWER UP)



Preliminary

FUJITSU

MB8281-12, MB8281-15
MOS 65,536 Bit Static Column Dynamic Random Access Memory

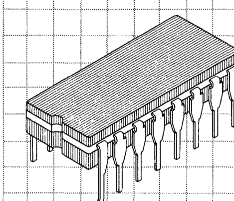
Description

The MB8281 is a 64K x 1 static column dynamic RAM. It features a static mode of operation in which very fast random access within the same a row is performed by simply changing the column address. In this mode the MB8281 operates like a static RAM.

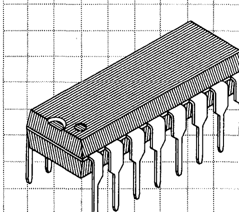
The MB8281 design has been optimized for high performance applications such as word processing, fast buffer memory, graphics terminals, and peripheral storage devices where high speed access, low power dissipation, compact layout, and low cost are required.

The MB8281 has fully TTL compatible inputs and output. It operates on a single +5 V ± 10% power supply. An on-chip substrate bias generator provides high performance operation. The MB8281 contains on chip address input and data input latches.

The MB8281 is fabricated with Fujitsu's advanced silicon gate NMOS double layer polysilicon process. This process along with the use of single transistor storage cells permits maximum circuit density and minimum chip size. Multiplexed row and column addressing allows the MB8281 to be packaged in a standard 16-pin DIP.



Ceramic Package
DIP-16C-C04

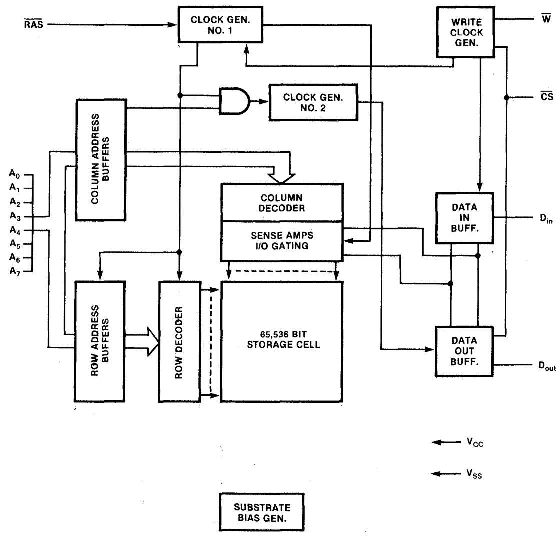


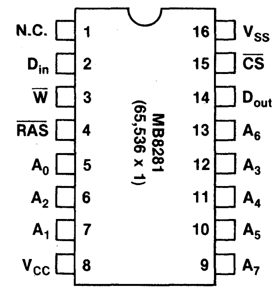
Plastic Package
DIP-16P-M03

Features

- **Row Access Time**
  120 ns (MB8281-12)
  150 ns (MB8281-15)
- **Static Access Time**
  55 ns (MB8281-12)
  70 ns (MB8281-15)
- **Random Cycle Time**
  230 ns (MB8281-12)
  260 ns (MB8281-15)
- **Static Cycle Time**
  60 ns (MB8281-12)
  75 ns (MB8281-15)
- **Single +5 V Supply, ±10% tolerance**
- **Low Power**
  Active 523 mW (max) at TSC = 60 ns
  Standby 33 mW (max)
- **Static mode read/write**
- **Short read/write**
- **Edge triggered write**
- **Internal write period control**
- **Fast chip select output control**
- **2 ms/128 cycle refresh**
- **$\overline{\text{RAS}}$-only refresh**

MB8281 Block Diagram and Pin Assignment





Preliminary

MOS Memories

FUJITSU

MB81256-10, MB81256-12, MB81256-15
NMOS 262,144-Bit Dynamic
Random Access Memory

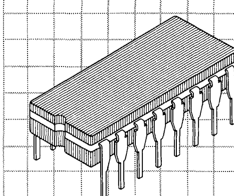
Description

The Fujitsu MB81256 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

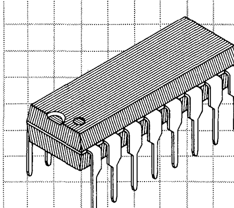
The MB81256 features "page mode" which allows high speed random access of up to 512-bits within the same row. Additionally, the MB81256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. Multiplexed row and column address inputs permit the MB81256 to be housed in a Jedec standard 16-pin dual in-line package and 18-pad LCC.

The MB81256 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

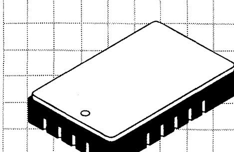
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Cerdip Package
DIP-16C-C04



Plastic Package
DIP-16P-M03

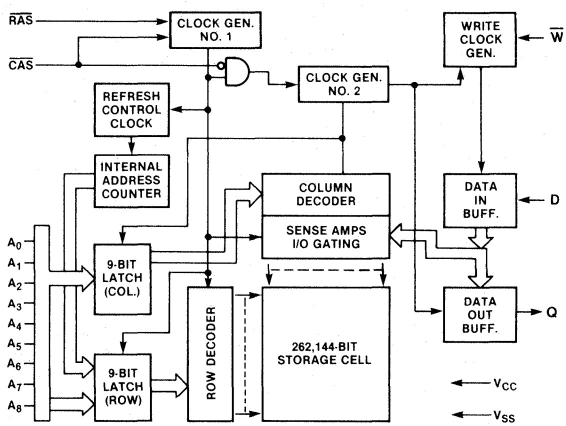


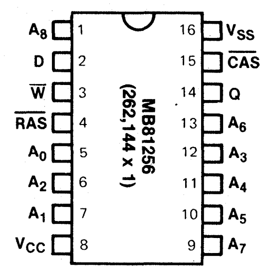
Ceramic LCC
LCC-18C-F04

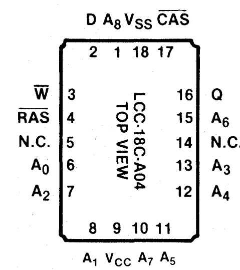
Features

- **262,144 x 1-bit organization**
- **Row Access Time/Cycle Time:**
  MB81256-10
  100 ns Max/210 ns Min.
  MB81256-12
  120 ns Max/230 ns Min.
  MB81256-15
  150 ns Max/260 ns Min.
- **Low Power Dissipation:**
  314 mW max. (t_{RC} = 260 ns)
  25 mW (Standby)
- **+5V supply voltage, ±10% tolerance**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Common I/O capability using "Early Write" operation**
- **On-chip substrate bias generator**
- **Page Mode Capability**
- **Fast Read-Write Cycle, TRWC = TRC**
- **t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} eliminated**
- **$\overline{CAS}$-before-$\overline{RAS}$ on chip refresh**
- **Hidden $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh**
- **$\overline{RAS}$-only refresh**
- **4 ms/256 cycle refresh**
- **Output unlatched at cycle end allows two dimensional chip select**
- **On-chip Address and Data-in latches**
- **Industry standard 16-pin package**

MB81256 Block Diagram and Pin Assignments







NOTE: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage on Any Pin relative to V_{SS}		V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Operating Temperature (ambient)		T_{OP}	0 to 70	°C
Storage Temperature	Gerdip	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C (ambient)
	V_{SS}	0	0	0	V	
Input High Voltage All Inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage All Inputs	V_{IL}	−1.0	—	0.8	V	

Capacitance
($T_A = 25\,°C$)

Parameter	Symbol	Value Min	Typ	Max	Unit
Input Capacitance A_0 to A_8, D	C_{IN1}	—	—	7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}	—	—	10	pF
Output Capacitance Q	C_{OUT}	—	—	7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81256-10 Min	Max	MB81256-12 Min	Max	MB81256-15 Min	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}	—	70	—	65	—	57	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}/\overline{CAS} = V_{IH}$)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} = Min.)	I_{CC3}	—	60	—	55	—	50	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = Min.)	I_{CC4}	—	35	—	30	—	25	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = Min.)	I_{CC5}	—	65	—	60	—	55	mA
INPUT LEAKAGE CURRENT Any Input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB81256-10 Min	MB81256-10 Max	MB81256-12 Min	MB81256-12 Max	MB81256-15 Min	MB81256-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV	—	4	—	4	—	4	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	210	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	210	—	230	—	260	—	ns
Access Time from $\overline{\text{RAS}}$	(4), (6)	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{\text{CAS}}$	(5), (6)	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	25	0	25	0	30	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{\text{RAS}}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{\text{RAS}}$ Pulse Width		t_{RAS}	TRELREH	110	100000	120	100000	150	100000	ns
$\overline{\text{RAS}}$ Hold Time		t_{RSH}	TCELREH	60	—	60	—	75	—	ns
$\overline{\text{CAS}}$ Pulse Width		t_{CAS}	TCELCEH	60	100000	60	100000	75	100000	ns
$\overline{\text{CAS}}$ Hold Time		t_{CSH}	TRELCEH	110	—	120	—	150	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	(4), (7)	t_{RCD}	TRELCEL	20	50	22	60	25	75	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Set Up Time		t_{CRS}	TCEXREL	15	—	20	—	20	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	12	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	20	—	25	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	(10)	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	(10)	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Write Command Set Up Time	(8)	t_{WCS}	TWLCEL	0	—	0	—	0	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	15	—	20	—	25	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	15	—	20	—	25	—	ns
Write Command to $\overline{\text{RAS}}$ Lead Time		t_{RWL}	TWLREH	40	—	50	—	60	—	ns
Write Command to $\overline{\text{CAS}}$ Lead Time		t_{CWL}	TWLCEH	40	—	50	—	60	—	ns
Data In Set Up Time		t_{DS}	TDVCEL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	15	—	20	—	25	—	ns
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ Delay	(8)	t_{CWD}	TCELWL	15	—	20	—	25	—	ns
Refresh Set Up Time for $\overline{\text{CAS}}$ Referenced to $\overline{\text{RAS}}$		t_{FCS}	TCELREL	20	—	25	—	30	—	ns
Refresh Hold Time for $\overline{\text{CAS}}$ Referenced to $\overline{\text{RAS}}$		t_{FCH}	TRELCEX	20	—	25	—	30	—	ns
Page Mode Read/Write Cycle Time		t_{PC}	TCELCEL	100	—	120	—	150	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	100	—	120	—	150	—	ns
Page Mode $\overline{\text{CAS}}$ Precharge Time		t_{CP}	TCEHCEL	40	—	50	—	65	—	ns
Refresh Counter Test $\overline{\text{RAS}}$ Pulse Width	(9)	t_{TRAS}	TRELREH	230	10000	265	10000	320	10000	ns
Refresh Counter Test Cycle Time	(9)	t_{RTC}	TRELREL	330	—	375	—	430	—	ns
RAS Precharge to $\overline{\text{CAS}}$ Active Time		t_{RPC}	TREHCEL	20	—	20	—	20	—	ns
Refresh Counter Test $\overline{\text{CAS}}$ Precharge Time	(9)	t_{CPT}	TCEHCEL	50	—	60	—	70	—	ns
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle		t_{CPR}	TCEHCEL	20	—	25	—	30	—	ns

See Notes on following page.

Notes: *These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

AC Characteristics, continued

Notes:

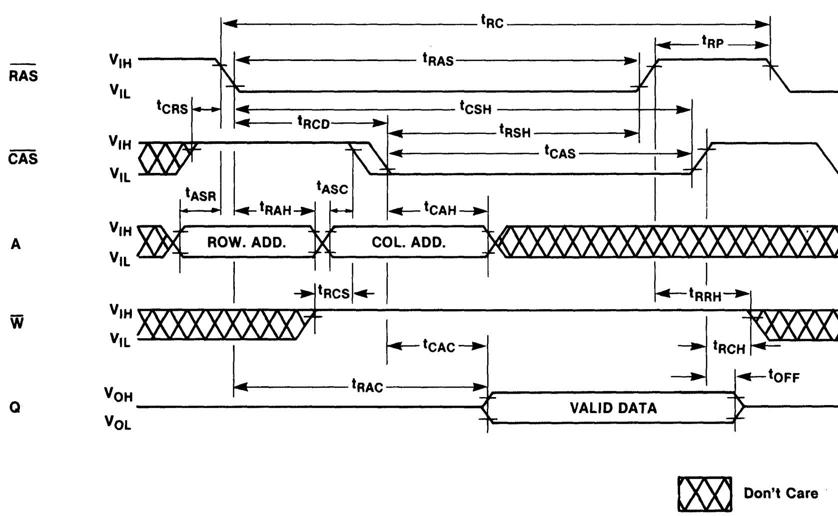
1. An initial pause of $200\mu s$ is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved.

   If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.
2. AC characteristics assume $t_T = 5ns$.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (Max.) the specified maximum value of t_{RAC} (Max.) can be met. If $t_{RCD} > t_{RCD}$ (Max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (Max.).
5. Assumes that $t_{RCD} > t_{RCD}$ (Max.).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
8. t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle.

   If $t_{CWD} > t_{CWD}$ (Min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Test mode write cycle only.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

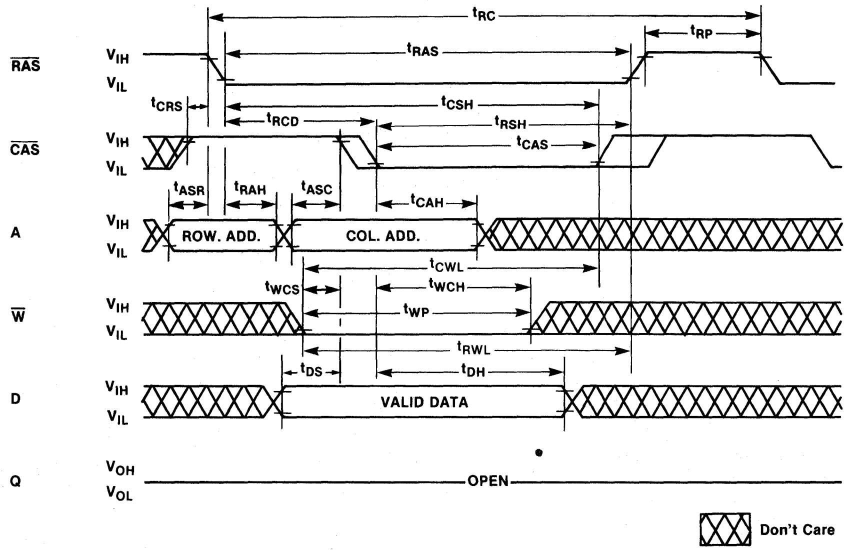
Timing Diagrams

Read Cycle

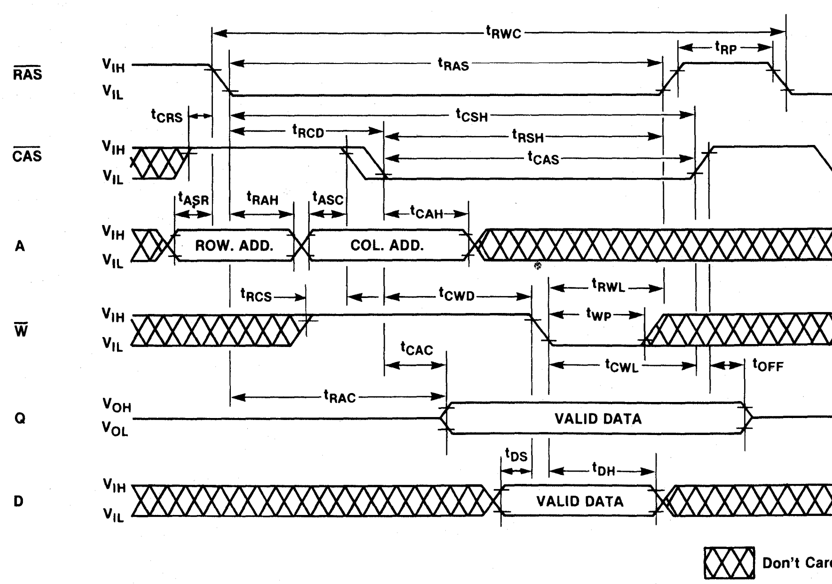


Timing Diagrams, continued

Write Cycle (Early Write)

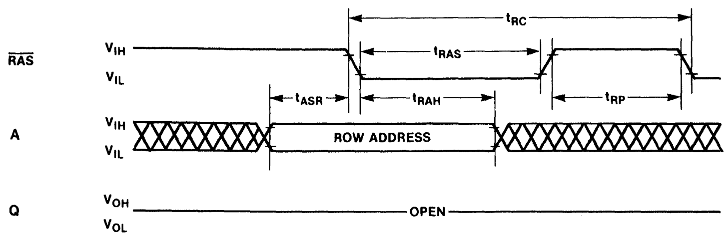


Read-Write/Read-Modify-Write Cycle

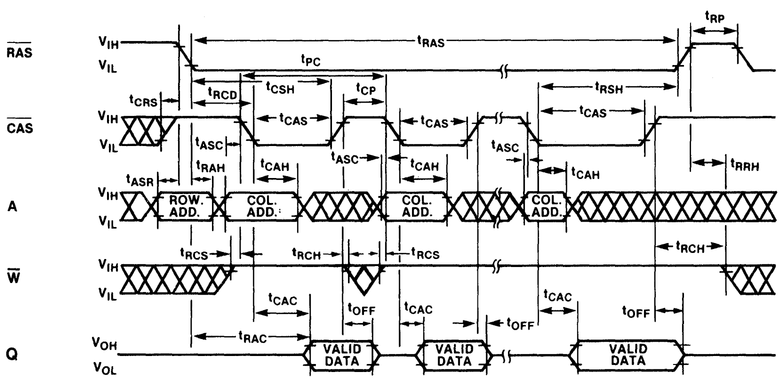


Timing Diagrams, continued

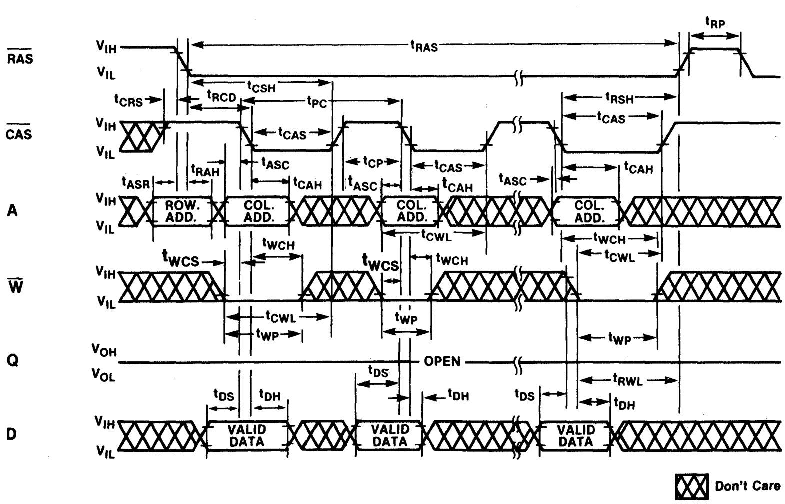
"$\overline{RAS}$-Only" Refresh Cycle
NOTE: $\overline{CAS} = V_{IH}$, W, D = Don't Care



Page Mode Read Cycle

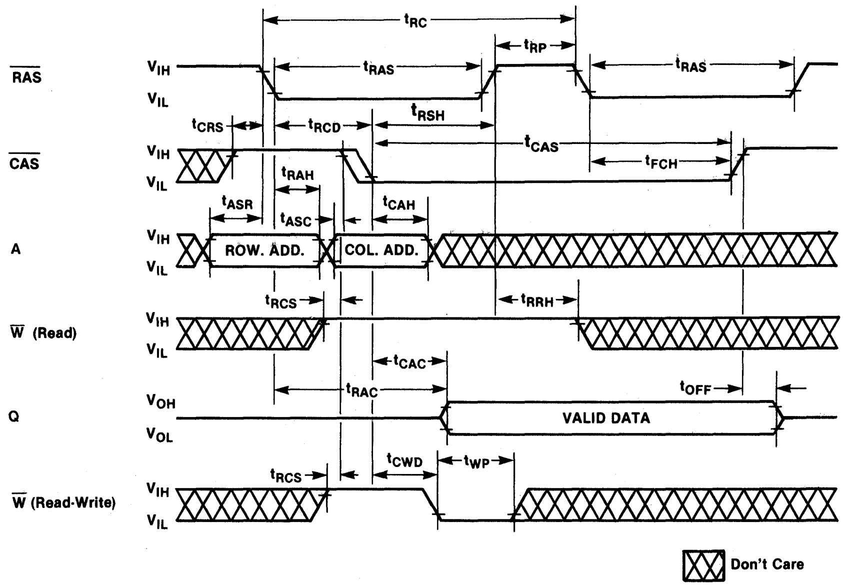


Page Mode Write Cycle

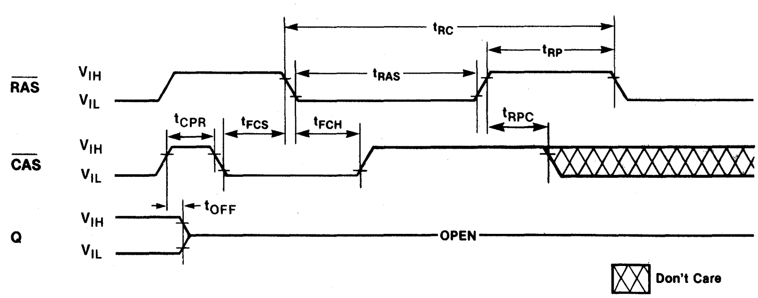


Timing Diagrams, continued

Hidden Refresh Cycle

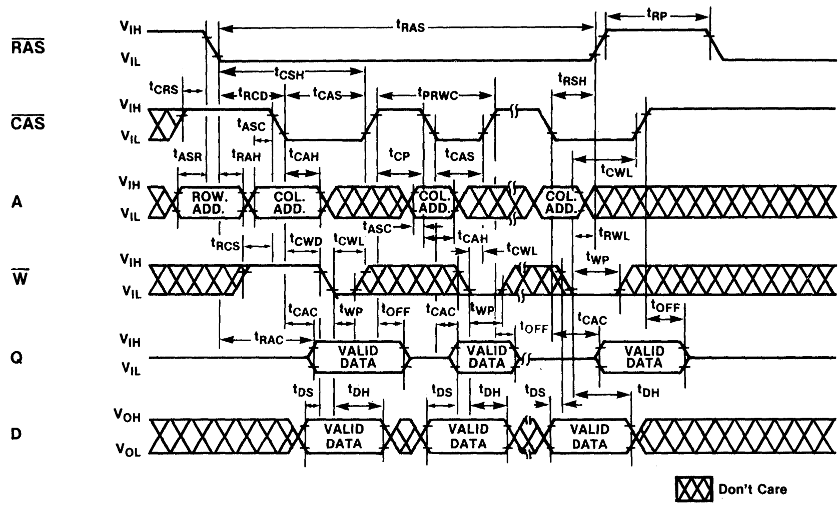


"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle
NOTE: A, $\overline{W}$, D = Don't Care

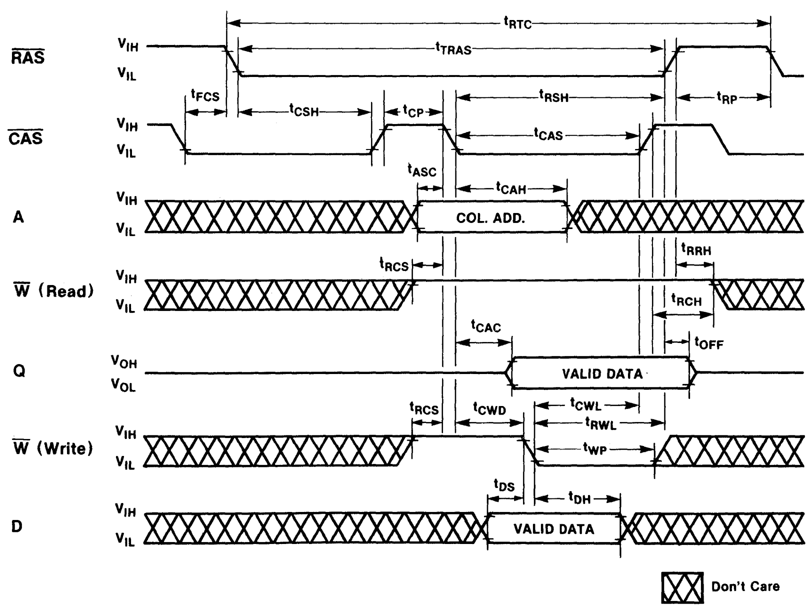


Timing Diagrams, continued

Page Mode Read-Write Cycle



"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Counter Test Cycle



Description

Simplified Timing Requirement
The MB81256 has improved circuitry that eases timing requirements for high speed access operations. The MB81256 can operate under the condition of t_{RCD} (max) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB81256 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB81256 provides higher throughput in inter-leaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle
The MB81256 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low' during a $\overline{CAS}$ transition to "low", the MB81256 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", after t_{CWD} following a $\overline{CAS}$ transition to "low", the MB81256 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle (t_{RWC} = t_{RC}) is possible with the MB81256.

Address Inputs
A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB81256. Nine row-address bits are established on the input pins (A_0 through A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable
The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

Data Input
Data is written into the MB81256 during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD(max)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD(max)}$. Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode
Page mode operation permits strobing the row address into the MB81256 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row address doesn't change. Thus, the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

$\overline{RAS}$-Only Refresh
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-adresses ($A_0 \sim A_7$) at least every 4 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 256 row-addresses ($A_0 \sim A_7$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81256 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh
A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB81256, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle
A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and then goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A ROW ADDRESS
Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A COLUMN ADDRESS
All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

(1). Initialize the internal refresh counter. For this operation, 8 cycles are required.

(2). Write a test pattern of "low"s into memory cells at a single column address and 256 row address.

(3). Using a read-modify-write cycle, read the "low" written at the last operation (Step 2) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.

(4). Read the "high"s written at the last operation (Step 3).

(5). Complement the test pattern and repeat steps (2), (3) and (4).

Preliminary

MOS Memories

FUJITSU

MB81257-10, MB81257-12, MB81257-15
NMOS 262,144-Bit Dynamic Random Access Memory With Nibble Mode

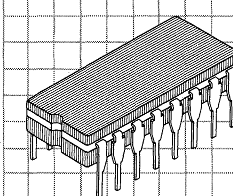
Description

The Fujitsu MB81257 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

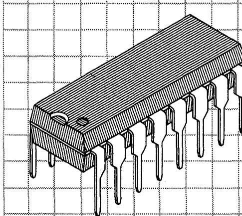
The MB81257 features "nibble mode" which allows high speed serial access of up to four bits of data. Additionally, the MB81257 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability that is an upward compatible version of the MB8266A. Multiplexed row and column address inputs permit the MB81257 to be housed in a Jedec standard 16-pin dual in-line package and 18-pad LCC.

The MB81257 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

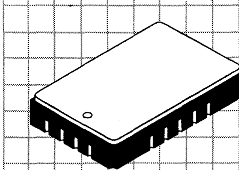
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Cerdip Package
DIP-16C-C04



Plastic Package
DIP-16P-M03

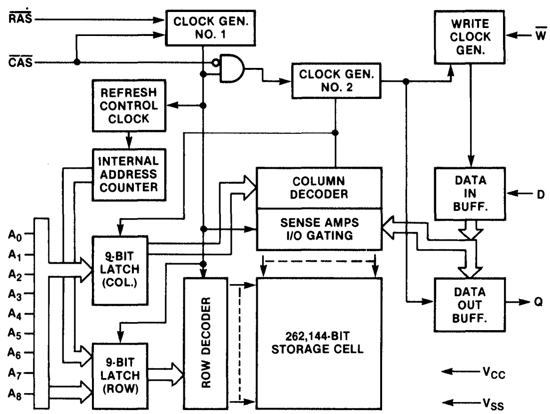


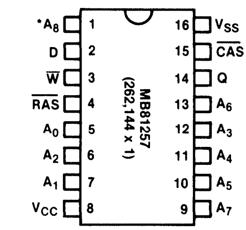
Ceramic LCC
LCC-18C-F04

Features

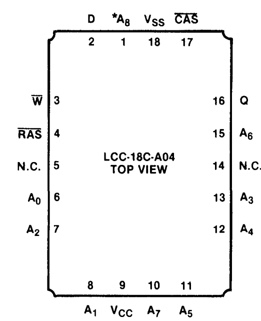
- **262,144 x 1-bit organization**
- **Row Access Time/Cycle Time:**
  - **MB81257-10 100 ns Max/ 210 ns Min.**
  - **MB81257-12 120 ns Max/ 230 ns Min.**
  - **MB81257-15 150 ns Max/ 260 ns Min.**
- **Low Power Dissipation:**
  - **314 mW max. (t_{RC} = 260 ns)**
  - **25 mW (Standby)**
- **+5V supply voltage, ±10% tolerance**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Common I/O capability using "Early Write" operation**
- **On-chip substrate bias generator**
- **Nibble mode capability for faster access**
- **Fast Read-Write Cycle, TRWC = TRC**
- **t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} eliminated**
- **$\overline{CAS}$-before-$\overline{RAS}$ on chip refresh**
- **Hidden $\overline{CAS}$ before-$\overline{RAS}$ on-chip refresh**
- **$\overline{RAS}$-only refresh**
- **Refresh 4 ms/256 cycles**
- **Output unlatched at cycle end allows two dimensional chip select**
- **On-chip Address and Data-in latches**
- **Industry standard 16-pin package**

MB81257 Block Diagram and Pin Assignments





*: A_8 (Pin 1) is Assigned for Nibble (4-bit) Address.



NOTE: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage on Any Pin relative to V_{SS}		V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Operating Temperature (ambient)		T_{OP}	0 to 70	°C
Storage Temperature	Cerdip	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C ambient
	V_{SS}	0	0	0	V	
Input High Voltage All Inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage All Inputs	V_{IL}	−1.0	—	0.8	V	

Capacitance
($T_A = 25°C$)

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit
Input Capacitance A_0 to A_8, D	C_{IN1}	—	—	7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}	—	—	10	pF
Output Capacitance Q	C_{OUT}	—	—	7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81257-10 Min	MB81257-10 Max	MB81257-12 Min	MB81257-12 Max	MB81257-15 Min	MB81257-15 Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}	—	70	—	65	—	57	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}/\overline{CAS} = V_{IH}$)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} = Min.)	I_{CC3}	—	60	—	55	—	50	mA
NIBBLE MODE CURRENT* Average Power Supply Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{NC} = Min.)	I_{CC4}	—	22	—	20	—	18	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = Min.)	I_{CC5}	—	65	—	60	—	55	mA
INPUT LEAKAGE CURRENT Any Input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB81257-10 Min	MB81257-10 Max	MB81257-12 Min	MB81257-12 Max	MB81257-15 Min	MB81257-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV	—	4	—	4	—	4	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	210	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	210	—	230	—	260	—	ns
Access Time from $\overline{RAS}$	(4), (6)	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$	(5), (6)	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	25	0	25	0	30	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	110	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	60	—	60	—	75	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	60	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	110	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	(4), (7)	t_{RCD}	TRELCEL	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEHREL	15	—	20	—	20	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	12	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	20	—	25	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{CAS}$	(10)	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	(10)	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Write Command Set Up Time	(8)	t_{WCS}	TWLCEL	0	—	0	—	0	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	15	—	20	—	25	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	15	—	20	—	25	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	40	—	50	—	60	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	20	—	30	—	40	—	ns
Data In Set Up Time		t_{DS}	TDVCEL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	15	—	20	—	25	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay	(8)	t_{CWD}	TCELWL	15	—	20	—	25	—	ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCS}	TCELREL	20	—	25	—	30	—	ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCH}	TRELCEX	20	—	25	—	30	—	ns
Nibble Mode Read-Write Cycle Time		t_{NRWC}	TCEHCEH	50	—	65	—	80	—	ns
Nibble Mode Read/Write Cycle Time		t_{NC}	TCEHCEH	50	—	65	—	80	—	ns
Nibble Mode Access Time		t_{NCAC}	TCELQV	—	20	—	30	—	40	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	TCELCEH	20	—	30	—	40	—	ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	TCEHCEL	20	—	25	—	30	—	ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	TCELREH	20	—	30	—	40	—	ns
Nibble Mode $\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$		t_{RNH}	TREHCEL	20	—	20	—	20	—	ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	TCELREH	40	—	50	—	60	—	ns
Refresh Counter Test Cycle Time	(9)	t_{RTC}	TRELREL	330	—	375	—	430	—	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	(9)	t_{CPT}	TCEHCEL	50	—	60	—	70	—	ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	(9)	t_{TRAS}	TRELREH	230	10000	265	10000	320	10000	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20	—	20	—	20	—	ns
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle		t_{CPR}	TCEHCEL	20	—	25	—	30	—	ns

See Notes on following page.

*These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

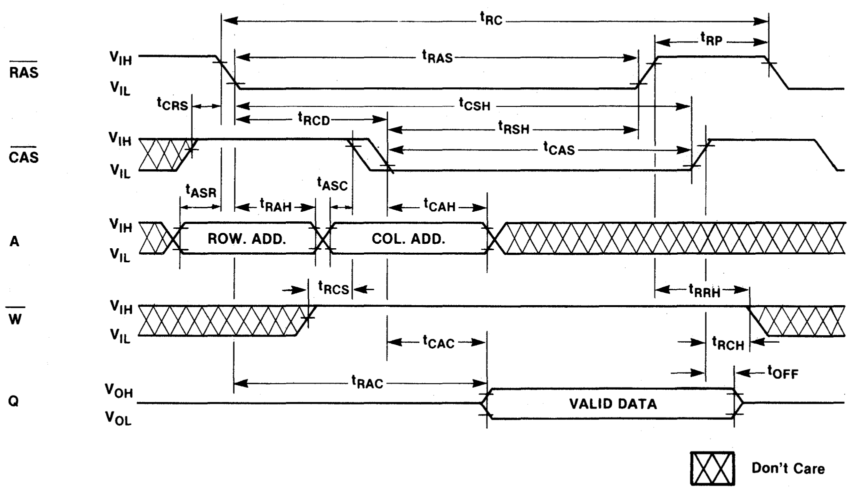
AC Characteristics

Notes:

1. An initial pause of 200μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved.
   If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.
2. AC characteristics assume t_T = 5ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (Max.) the specified maximum value of t_{RAC} (Max.) can be met. If $t_{RCD} > t_{RCD}$ (Max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (Max.).
5. Assumes that $t_{RCD} > t_{RCD}$ (Max.).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
8. t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle.
   If $t_{CWD} > t_{CWD}$ (Min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Test mode cycle only.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

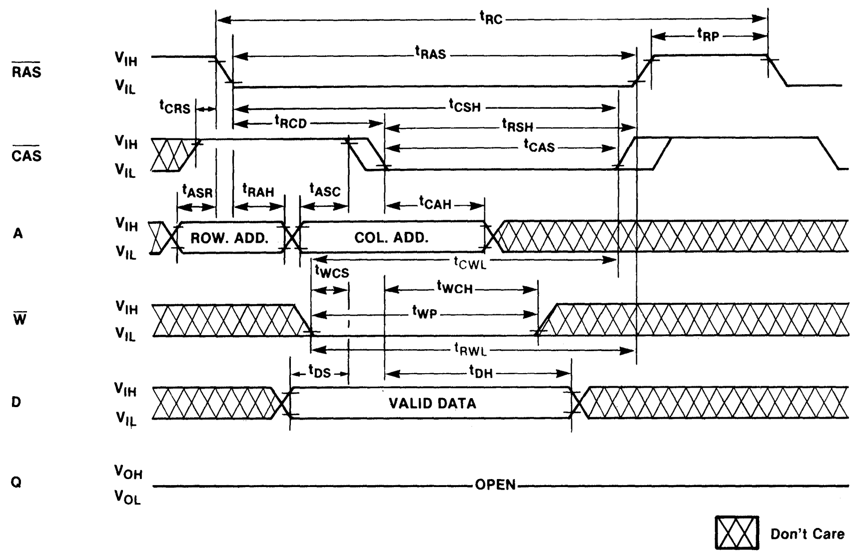
Timing Diagrams

Read Cycle

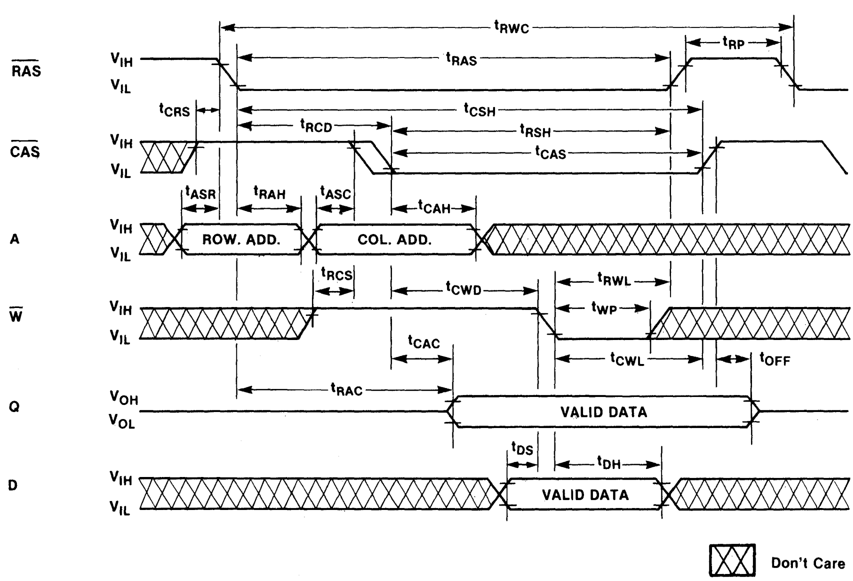


Timing Diagrams, continued

Write Cycle (Early Write)

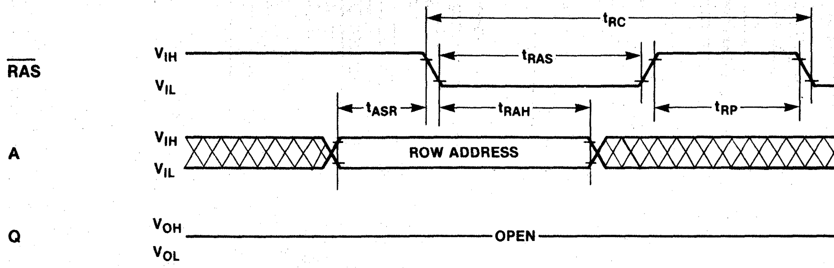


Read-Write/Read-Modify-Write Cycle

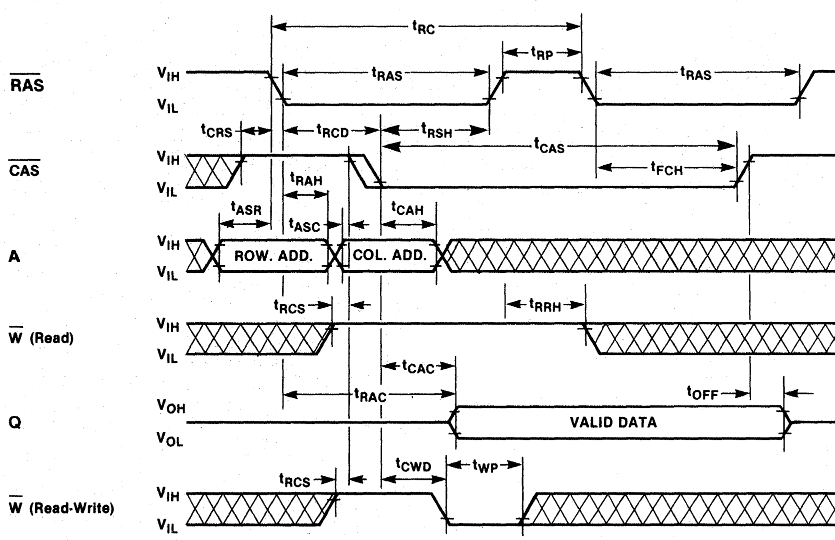


Timing Diagrams, continued

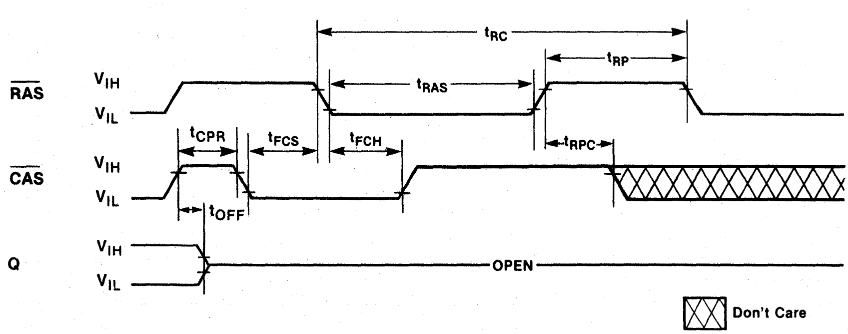
"$\overline{RAS}$-Only" Refresh Cycle
NOTE: $\overline{CAS} = V_{IH}$, W, D = Don't Care



Hidden Refresh Cycle

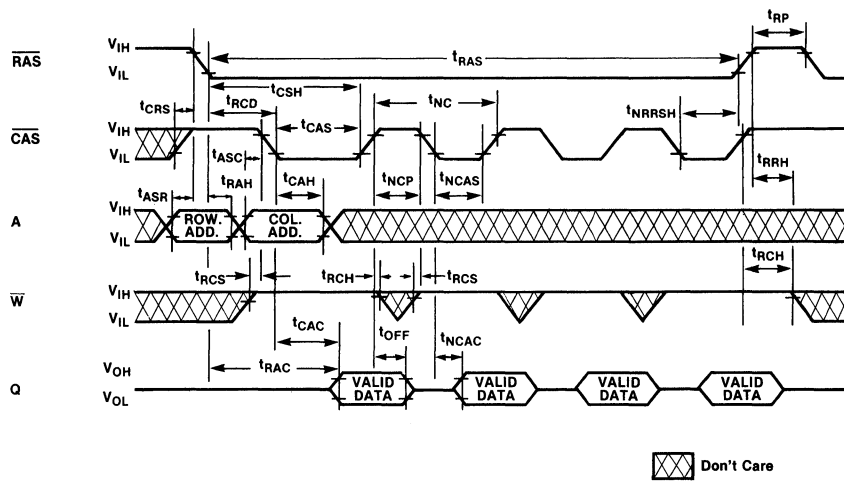


"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle
NOTE: Address, $\overline{W}$, D = Don't Care

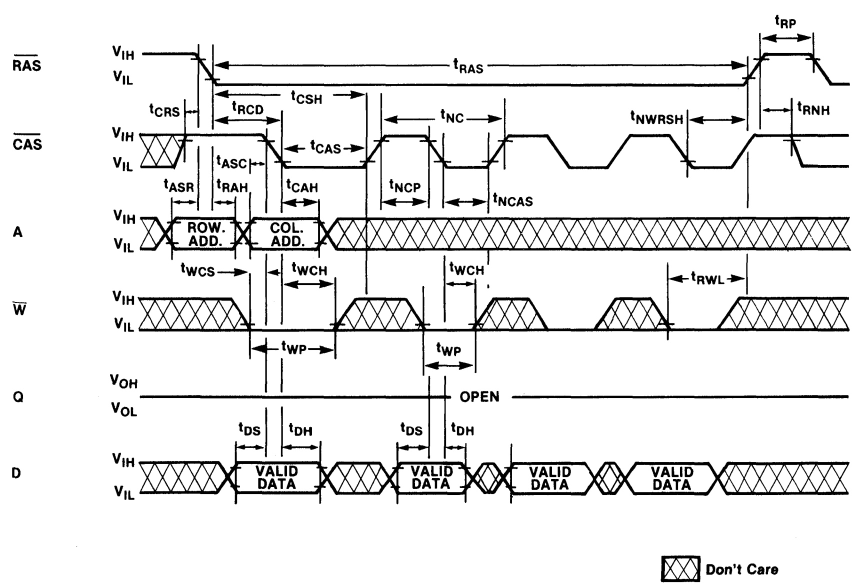


Timing Diagrams, continued

Nibble Mode Read Cycle

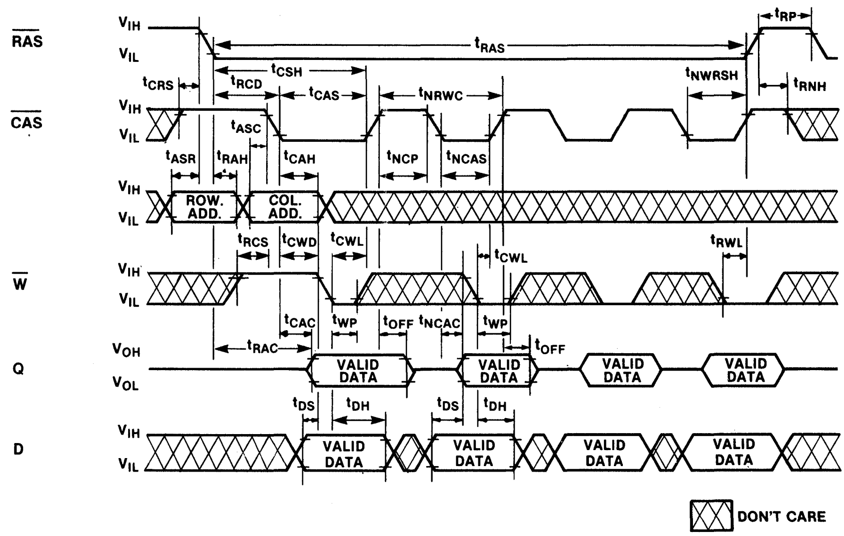


Nibble Mode Write Cycle

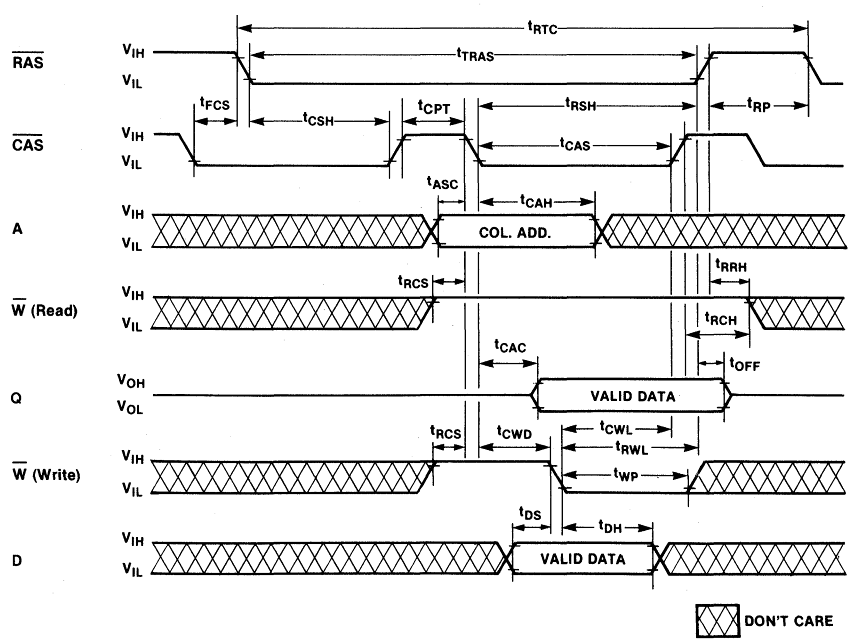


Timing Diagrams, continued

Nibble Mode Read-Write Cycle



"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Counter Test Cycle



Description

Simplified Timing Requirement

The MB81257 has improved circuitry that eases timing requirements for high speed access operations. The MB81257 can operate under the condition of t_{RCD} (max) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB81257 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB81257 provides higher throughput in interleaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle

The MB81257 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low" during a $\overline{CAS}$ transition to "low", the MB81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", after t_{CWD} following a $\overline{CAS}$ transition to "low", the MB81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle ($t_{RWC} = t_{RC}$) is possible with the MB81257.

Address Inputs

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB81257. Nine row address bits are established on the input pins (A_0 through A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

Data Input

Data is written into the MB81257 during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD(max)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD(max)}$. Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See table I below).

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of the D_{OUT} pin is determined by the first normal access cycle.

The data output is controlled

Table 1
Nibble Mode Address Sequence Example

Sequence	Nibble Bit	RA_8	Row Address	CA_8	Column Address	Comments
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Description, continued

only by the $\overline{\mathrm{W}}$ state referenced at the $\overline{\mathrm{CAS}}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} > t_{WCS}$(min.) is met, the data output will remain open circuit throughout the succeeding nibble cycle regardless of the $\overline{\mathrm{W}}$ state. When $t_{CWD} > t_{CWD}$(min.) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{\mathrm{W}}$ state. The write operation is done during the period in which the $\overline{\mathrm{W}}$ and $\overline{\mathrm{CAS}}$ clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of the timing conditions of $\overline{\mathrm{W}}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit). (See table II and Figure 2 below).

$\overline{\mathrm{RAS}}$-Only Refresh
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-adresses ($A_0 \sim A_7$) at least every 4 ms. $\overline{\mathrm{RAS}}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{\mathrm{CAS}}$ is brought "low". Strobing each of the 256 row-addresses ($A_0 \sim A_7$) with $\overline{\mathrm{RAS}}$ will cause all bits in each row to be refreshed. $\overline{\mathrm{RAS}}$-only refresh results in a substantial reduction in power dissipation.

$\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ Refresh
$\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ refreshing available on the MB81257 offers an alternate refresh method. If $\overline{\mathrm{CAS}}$ is held "low" for the specified period (t_{FCS}) before $\overline{\mathrm{RAS}}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ refresh operation.

Hidden Refresh
A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{\mathrm{CAS}}$ active time. For the MB81257, a hidden refresh cycle is a $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ refresh cycle.

$\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ Refresh Counter Test Cycle
A special timing sequence using the $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ refresh activated circuitry.

After the $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ refresh operation, if $\overline{\mathrm{CAS}}$ goes to "high" and then goes to "low" again while $\overline{\mathrm{RAS}}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A ROW ADDRESS
Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A COLUMN ADDRESS
All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{\mathrm{CAS}}$.

Suggested $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ Counter Test Procedure
The timing, as shown in the $\overline{\mathrm{CAS}}$-before-$\overline{\mathrm{RAS}}$ Counter Test Cycle, is used for all the following operations:

(1). Initialize the internal refresh counter. For this operation, 8 cycles are required.

(2). Write a test pattern of "low"s into memory cells at a single column address and 256 row address.

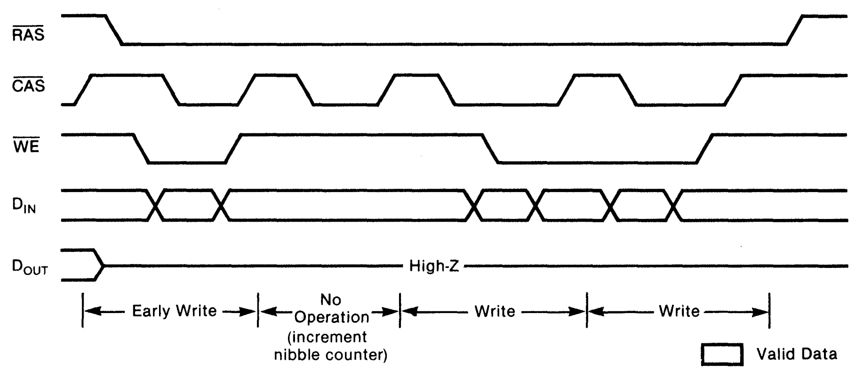
(3). Using a read-modify-write cycle, read the "low" written at the last operation (Step (2)) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.

(4). Read the "high"s written at the last operation (Step 3).

(5). Complement the test pattern and repeat steps (2), (3) and (4).

Figure 2
Nibble Mode

1) In this case the first nibble cycle is an Early Write cycle.



2) In this case the first nibble cycle is a delayed write (Read-Write) cycle.

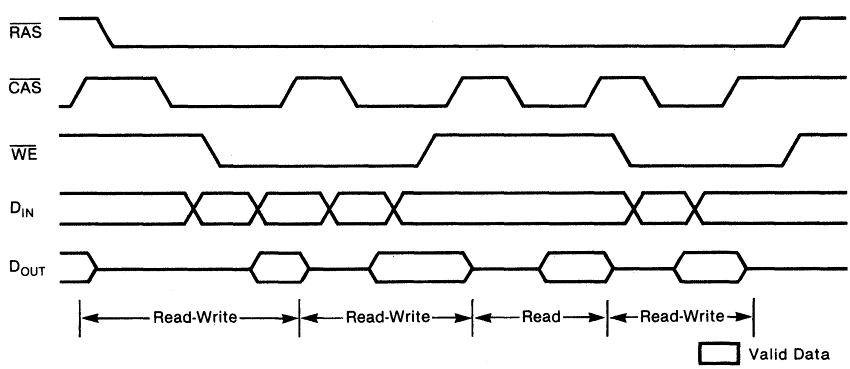


Table 2
Functional Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby.
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read.
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geq t_{WCS}$ (min).
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geq t_{CWD}$ (min).
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$ Only Refresh.
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh. Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.

FUJITSU
MICROELECTRONICS, INC.

MB81416-10
MB81416-12
MB81416-15

16,384 WORD BY 4-BIT NMOS DYNAMIC RANDOM ACCESS MEMORY

PRELIMINARY

Note: This is not a final specification. Some parametric limits are subject to change.

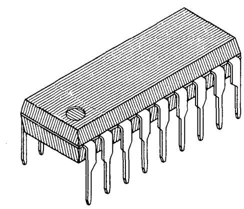
DESCRIPTION

The Fujitsu MB81416 is a fully decoded, dynamic NMOS random access memory organized as 16384 words by 4-bits. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

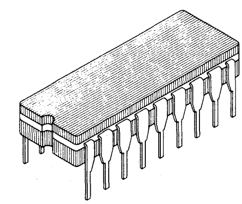
Multiplexed row and column address inputs permit the MB81416 to be housed in a standard 18-pin DIP that is compatible with the JEDEC approved pinout. Greater refresh versatility is provided by a new $\overline{CAS}$ before $\overline{RAS}$ on-chip refresh capability. The MB81416 also features "page mode" which allows high speed random access of up to 64 nibble wide words within the same row address.

The MB81416 is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and the power supply tolerance is very wide. All inputs and outputs are TTL compatible.



PLASTIC PACKAGE DIP-18P-M01

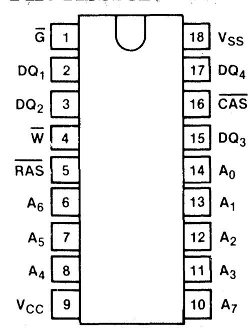


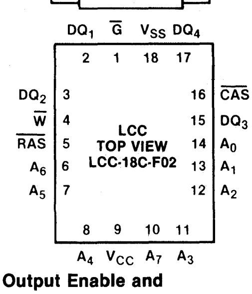
CERDIP PACKAGE DIP-18C-C01

FEATURES

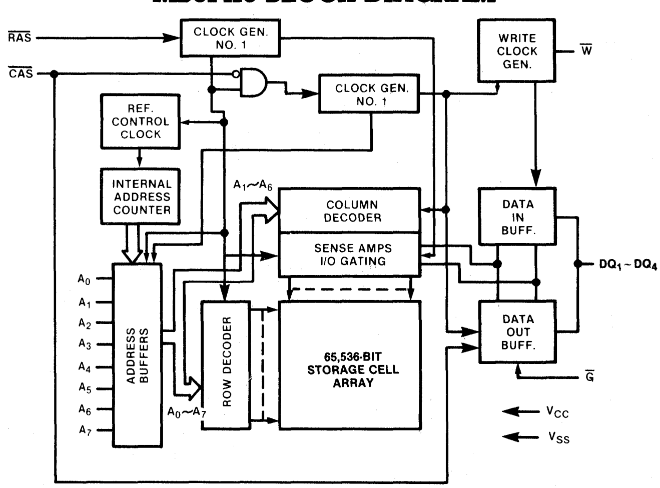
- **Organized as 16384 words by 4-bits**
- **Row Access Time/Cycle Time:**
  MB81416-10 100nsec max/200 min.
  MB81416-12 120nsec max/230 min.
  MB81416-15 150nsec max/260 min.
- **Low Active Power (t_{RC} = min)**
  MB81416-10 303mW (max.)
  MB81416-12 275mW (max.)
  MB81416-15 248mW (max.)
  All devices 25mW standby
- **Single +5V ±10% Power Supply**
- **$\overline{CAS}$ before $\overline{RAS}$ Refresh**
- **$\overline{RAS}$ Only Refresh**
- **Hidden $\overline{CAS}$ before $\overline{RAS}$ Refresh**
- **2ms/128 cycle Refresh ($A_0 \sim A_6$)**
- **Read-Modify-Write Capability**
- **Page Mode Capability for faster access**
- **Output unlatched at cycle end**
- **Early Write or Output Enable controls output buffer impedance**
- **On Chip Address and Data-In latches**
- **Standard 18-pin DIP**
- **All Inputs TTL Compatible, low capacitive load**
- **Three-State TTL Compatible Outputs**
- **On-chip Substrate Bias Generator**

PIN ASSIGNMENTS





MB81416 BLOCK DIAGRAM



NOTE: The following IEEE Std. 662-1980 Symbols are used in this data sheet: DQ = Data I/O, $\overline{G}$ = Output Enable and $\overline{W}$ = Write Enable.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_7$,	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{G}$	C_{IN2}	—	8	pF
Output Capacitance $DQ_1 \sim DQ_4$	C_D	—	7	pF

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs except DQ	V_{IL}	−2.0	—	0.8	V	
Input Low Voltage, DQ	V_{ILD}*	−1.0	—	0.8	V	

*The device will withstand undershoots to the −2.0V level with a maximum pulse width of 20ns at the −1.5V level.

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB81416-10	I_{CC1}		55	mA
	MB81416-12			50	
	MB81416-15			45	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		4.5	mA
REFRESH CURRENT1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB81416-10	I_{CC3}		38	mA
	MB81416-12			35	
	MB81416-15			32	
PAGE MODE CURRENT Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min)	MB81416-10	I_{CC4}		38	mA
	MB81416-12			35	
	MB81416-15			32	
REFRESH CURRENT 2* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$)	MB81416-10	I_{CC5}		42	mA
	MB81416-12			38	
	MB81416-15			35	
INPUT LEAKAGE CURRENT Input leakage current, any input ($0 \leqq V_{IN} \leqq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		I_{OL}	−10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = −5mA)		V_{OH}	2.4		V
Output low voltage (I_{OL} = 4.2mA)		V_{OL}		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
I_{CC} is dependent on input low voltage level V_{ILD}, $V_{ILD} > -0.5V$.

PRELIMINARY

Note: This is not a final specification. Some parametric limits are subject to change.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol		MB81416-10		MB81416-12		MB81416-15		Unit
		Alternate	*Standard	Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}	TRVRV	—	2	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	290	—	330	—	375	—	ns
Access Time from $\overline{RAS}$	(4), (6)	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$	(5), (6)	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn Off Delay		t_{OFF}	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	50	—	60	—	75	—	ns
$\overline{CAS}$ Precharge Time (Page Mode only)		t_{CP}	TCEHCEL	45	—	50	—	60	—	ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	TCEHCEL	40	—	45	—	55	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	100	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	(4), (7)	t_{RCD}	TRELCEL	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEHREL	20	—	25	—	30	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	(9)	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Read Command Hold Time Referenced to $\overline{CAS}$	(9)	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Write Command Set Up Time		t_{WCS}	TWLCEL	–5	—	–5	—	–5	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	20	—	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	20	—	25	—	30	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	45	—	50	—	60	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	45	—	50	—	60	—	ns
Data In Set Up Time		t_{DS}	TDVCEL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	20	—	25	—	30	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay	(8)	t_{CWD}	TCELWL	85	—	100	—	120	—	ns
$\overline{RAS}$ to $\overline{W}$ Delay	(8)	t_{RWD}	TRELWL	135	—	160	—	195	—	ns
Access Time from $\overline{G}$		t_{OEA}	TGLQV	—	25	—	30	—	40	ns
$\overline{G}$ to Data in Delay Time		t_{OED}	TGHDV	30	—	35	—	40	—	ns
$\overline{G}$ Hold Time Referenced to $\overline{W}$		t_{OEH}	TWLGL	0	—	0	—	0	—	ns
Output Buffer Turn Off Delay from $\overline{G}$		t_{OEZ}	TGHQZ	0	30	0	35	0	40	ns
Page Mode Cycle Time		t_{PC}	TCELCEL	105	—	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	180	—	205	—	240	—	ns
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{FCS}	TCELREL	20	—	25	—	30	—	ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{FCH}	TRELCEH	20	—	25	—	30	—	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20	—	20	—	20	—	ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	(10)	t_{TRAS}	TRELREH	280	—	325	—	390	—	ns
Refresh Counter Test Cycle Time	(10)	t_{RTC}	TRELREL	380	—	435	—	500	—	ns
$\overline{G}$ to $\overline{RAS}$ Inactive Setup Time		t_{OES}	TGLREH	0	—	0	—	0	—	ns
Data in to $\overline{CAS}$ Delay Time	(11)	t_{DZC}	TDXCEL	0	—	0	—	0	—	ns
Data in to $\overline{G}$ Delay Time	(11)	t_{DZO}	TDXGL	0	—	0	—	0	—	ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ cycle)		t_{CPR}	TCEHCEL	25	—	30	—	30	—	ns

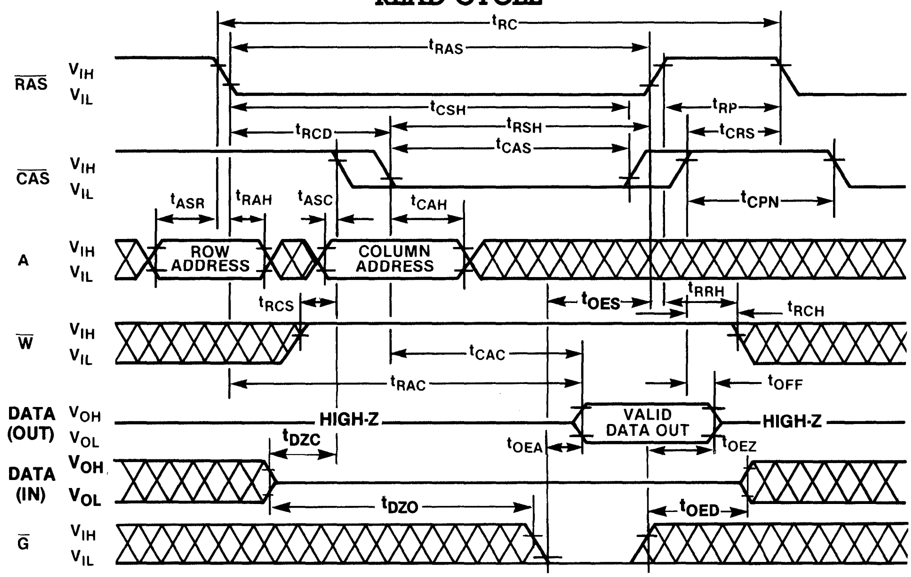
Notes: See notes on next page

*These symbols are described in IEEE Std. 662-1980: IEEE Standard Terminology for Semiconductor Memory.

Notes:

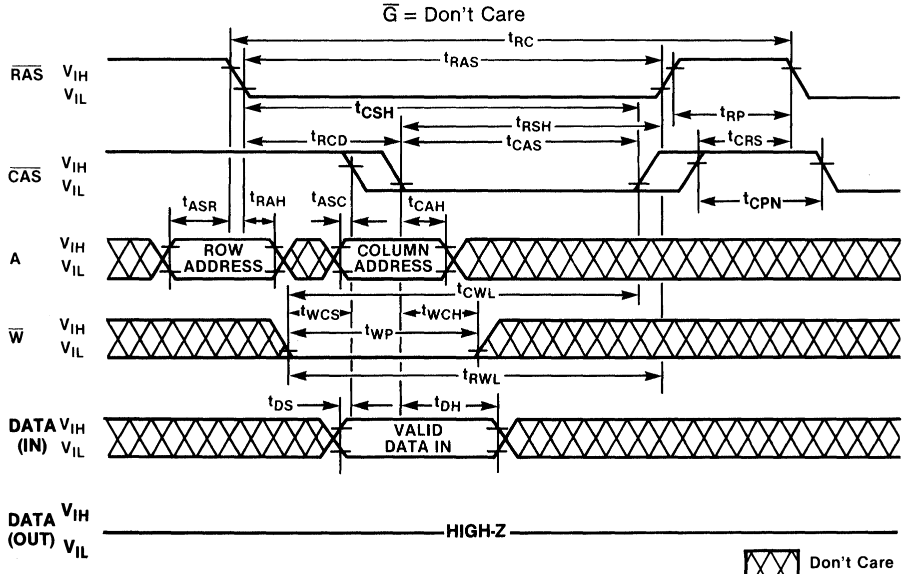
1. An initial pause of 200μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T = 5ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.): t_T = 5ns.
8. t_{WCS}, t_{CWD} and t_{RWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Refresh counter test cycle only.
11. Either t_{DZC} or t_{DZO} must be satisfied for all cycles.

READ CYCLE



WRITE CYCLE (Early Write)

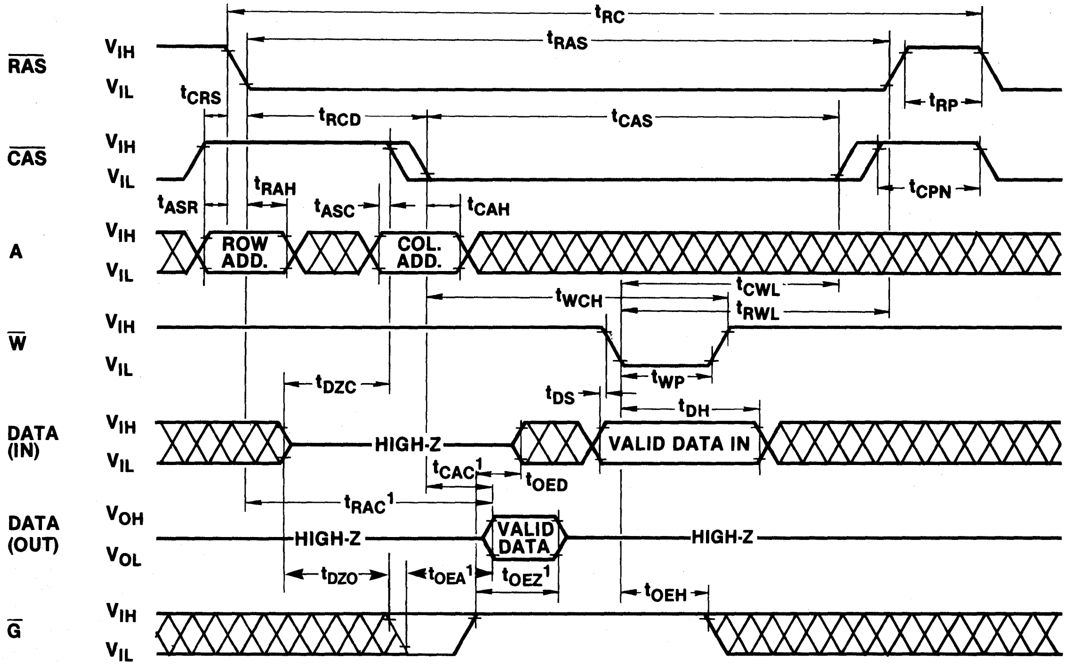
$\overline{G}$ = Don't Care



Note: This is not a final specification.
Some parametric limits are subject to change.

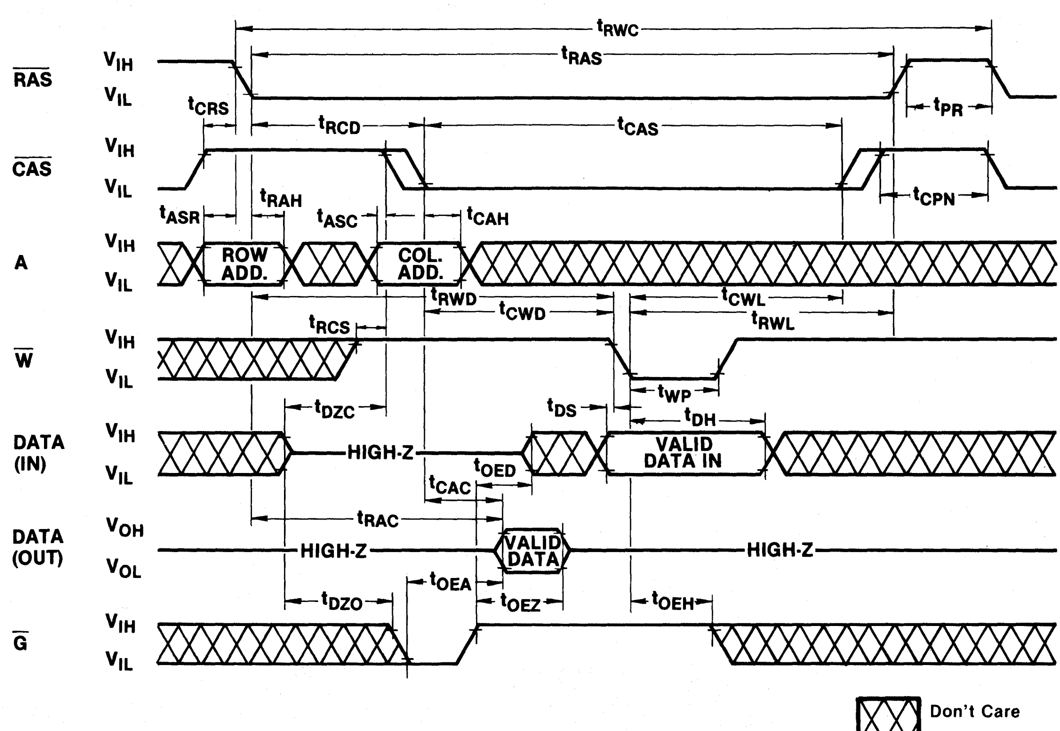
WRITE CYCLE

(Output Enable Controlled)

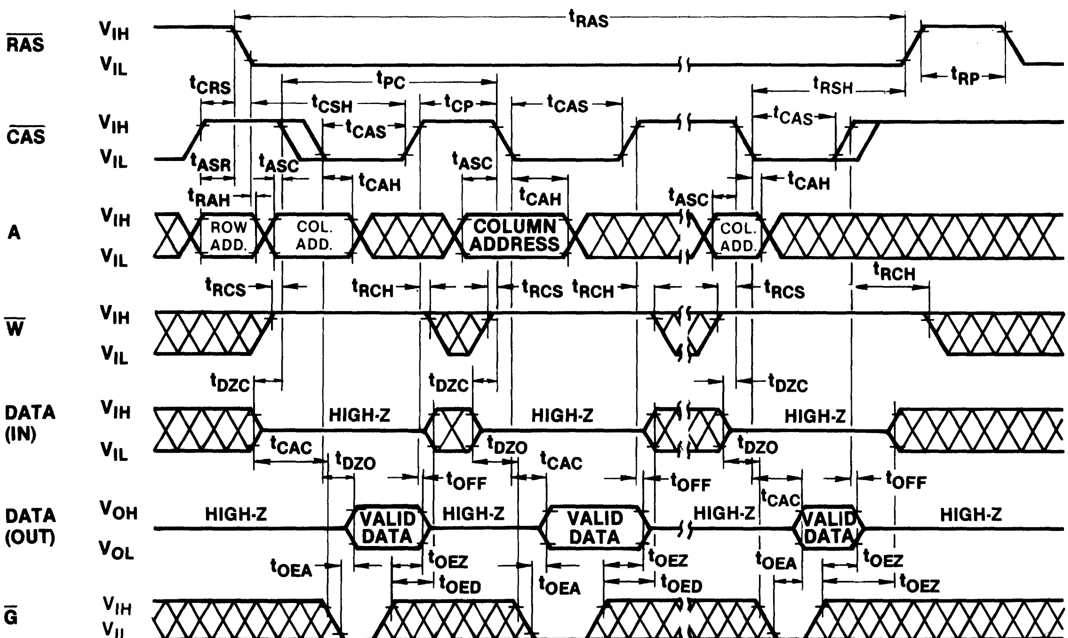


Note 1: When t_{CWD} is satisfied and $\overline{G}$ is low (Delayed-Write Cycle), the data out will be "VALID". But when t_{CWD} is not satisfied, the data out will be "INVALID".

READ-MODIFY-WRITE CYCLE

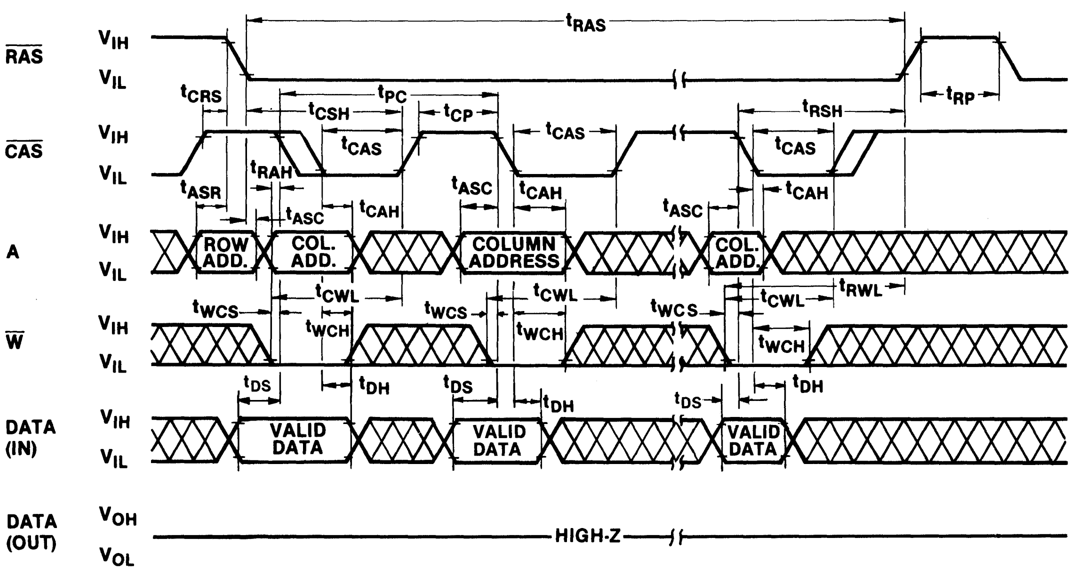


PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

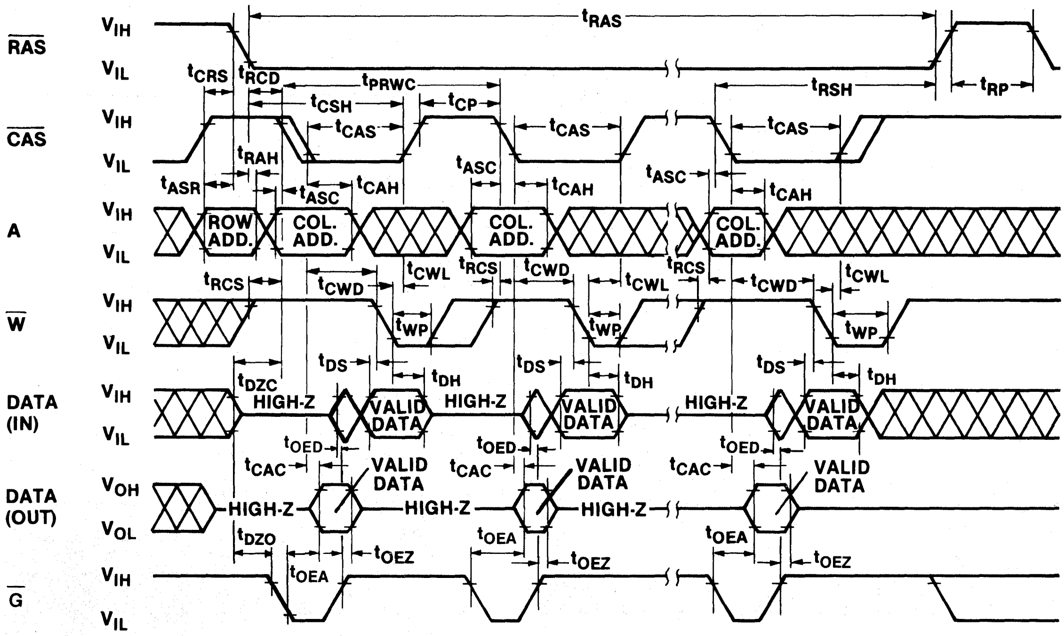
(G = Don't Care)



Don't Care

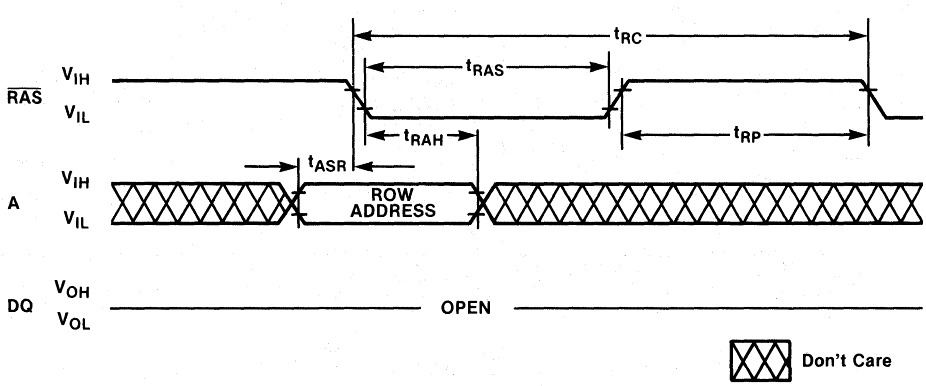
PRELIMINARY
Note: This is not a final specification.
Some parametric limits are subject to change.

PAGE MODE READ-WRITE CYCLE



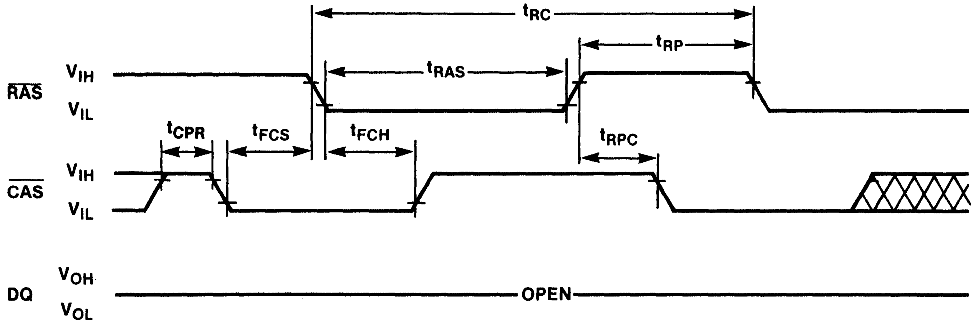
RAS ONLY REFRESH CYCLE

NOTE: $\overline{CAS} = V_{IH}$; A_7, $\overline{W}$, $\overline{G}$, = Don't Care

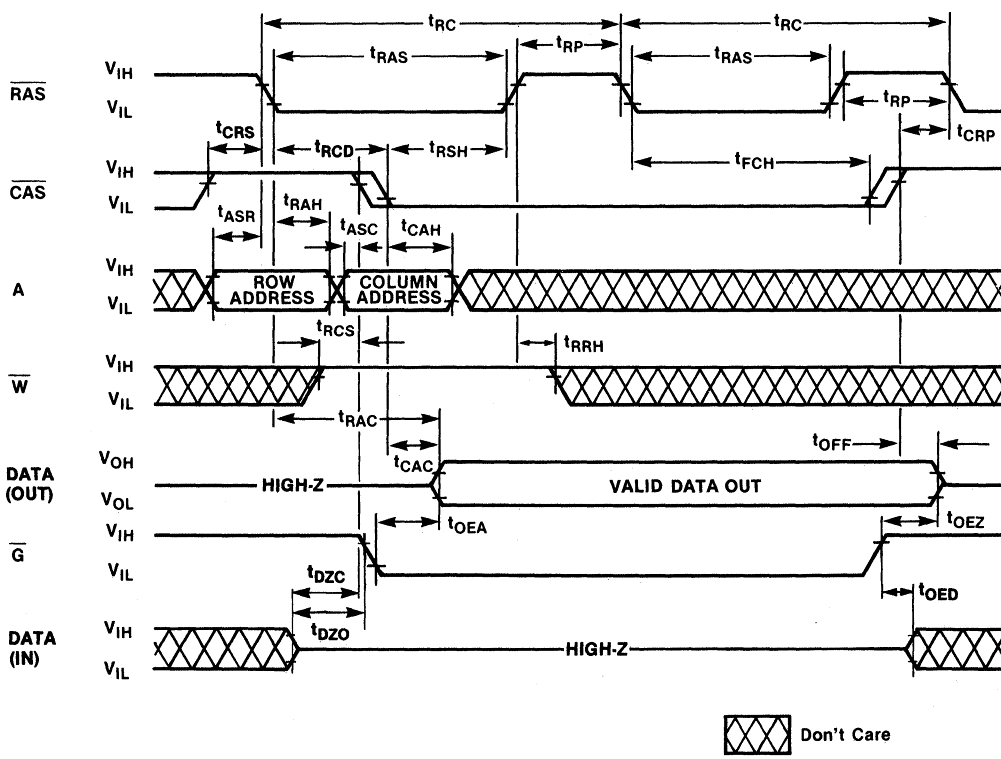


CAS-BEFORE-RAS REFRESH CYCLE

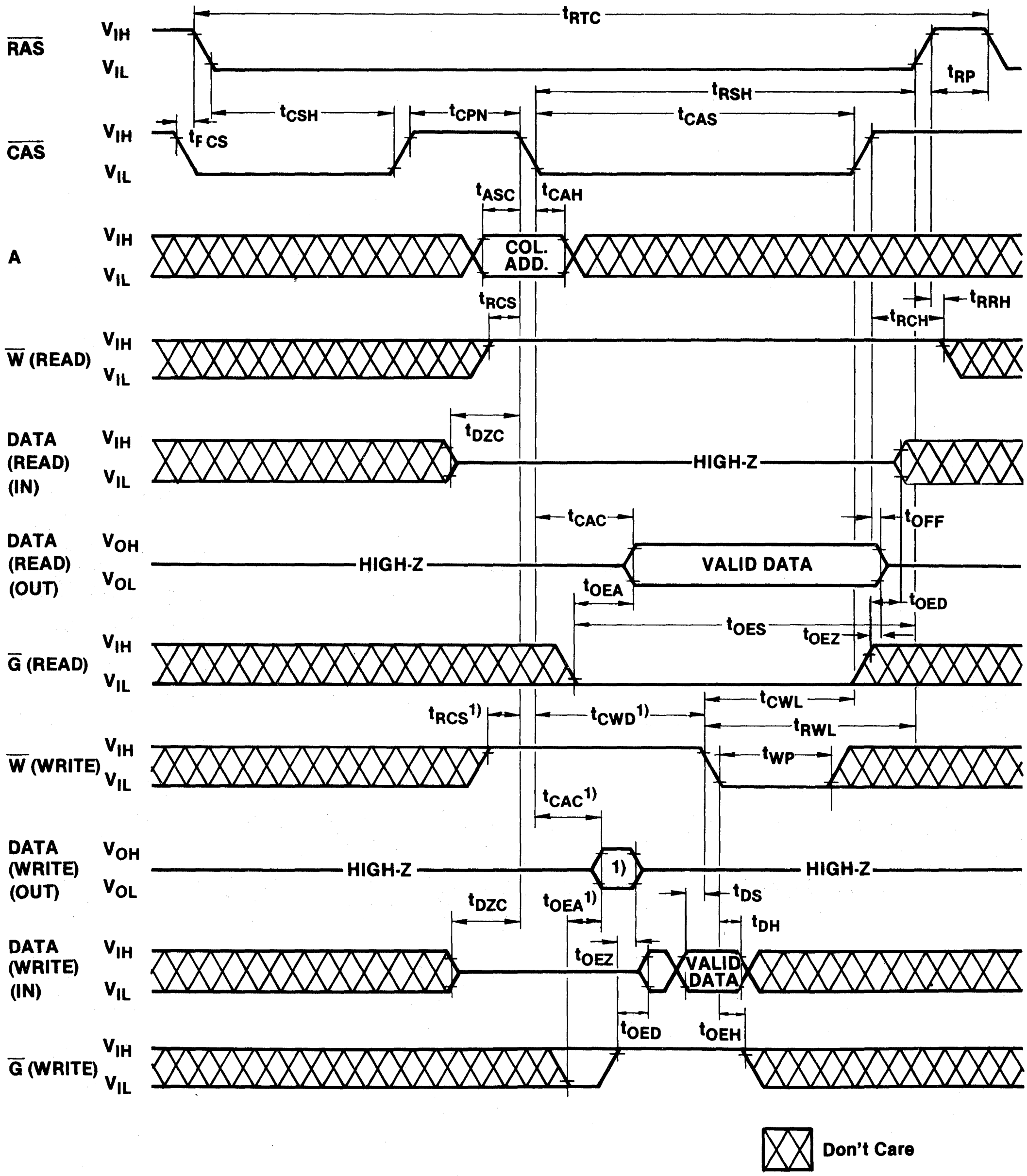
NOTE: A, W, G = Don't Care



HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



Note 1: When t_{CWD} is satisfied and $\overline{G}$ is low (Delayed-Write Cycle), the data out will be "VALID". But when t_{CWD} is not satisfied, the data out will be "INVALID".

PRELIMINARY

Note: This is not a final specification. Some parametric limits are subject to change.

DESCRIPTION

Address Inputs

A total of 14 binary input address bits are needed to decode any one of 16,384 nibble wide words from the MB81416's 65,536 memory cells. Addressing a Random 4-bit word is initiated by establishing 8 row address bits on the address input pins, (A_0 through A_7), and after they are stable, latching these address bits with the falling edge of the Row Address Strobe ($\overline{RAS}$). Then 6 column address bits are established on the address input pins A_1 through A_6. After the addresses are stable, they are latched with the falling edge of the Column Address Strobe ($\overline{CAS}$). Address timing is made non-critical by the MB81416's "gated $\overline{CAS}$" circuitry which automatically inhibits $\overline{CAS}$ until the Row Adress Hold time (t_{RAH}) has been satisfied and the address inputs have changed from row to column addresses.

Data Input/Output

The MB81416 has 4 common I/O pins (DQ_1, DQ_2, DQ_3, and DQ_4). Read or write modes are selected with the write enable pin ($\overline{W}$). An output enable pin ($\overline{G}$) controls the state of the output buffers making delayed write and read-modify-write cycles possible. The DQ pins provide TTL compatible inputs and three-state TTL compatible outputs with a fan-out of two standard TTL loads. Data-out has the same polarity as data-in.

Write Enable

The read mode or write modes are determined by the state of the write enable pin ($\overline{W}$). A logic high on $\overline{W}$ selects the read mode and a logic low on $\overline{W}$ selects the write mode. When $\overline{W}$ is high (read mode), the data inputs are disabled. If $\overline{W}$ goes low and satisfies the write command set-up time (t_{WCS}) before $\overline{CAS}$ goes low, the data outputs will remain in the high-impedance state for the duration of the cycle. This allows a write cycle to occur regardless of the state of the output enable ($\overline{G}$).

Output Enable

The output buffers are controlled by both $\overline{CAS}$ and output enable ($\overline{G}$). If either $\overline{CAS}$ or $\overline{G}$ are high the output buffers are in the high impedance state. During a read or read-modify-write cycle if both $\overline{CAS}$ and $\overline{G}$ are low, the output buffers are enabled. During an early write cycle $\overline{G}$ has no effect on the output buffers.

Data Inputs

Data may be written into the MB81416 during a write or read-modify-write cycle. The last falling edge of $\overline{CAS}$ or $\overline{W}$, strobes the data into the 4 on-chip data latches. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with both the set-up time (t_{DS}) and hold time (t_{DH}) referenced to the falling edge of $\overline{CAS}$. The outputs are in the high impedance state regardless of $\overline{G}$'s state. In a delayed write or a read-modify-write cycle, $\overline{W}$ is brought low after $\overline{CAS}$, data is strobed-in by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$. To avoid buss contention on I/O pins, it is necessary during a delayed write or a read-modify-write cycle for $\overline{G}$ to be high prior to data input so that the output buffers are in the high impedance state when data is being written.

Data Outputs

Data can be read from the MB81416 with either a read or a read-modify-write cycle. These cycles begin with the outputs in the high impedance state. The outputs contain active, valid data only after both $\overline{CAS}$ and $\overline{G}$ have been brought low and have satisfied the minimum access time from $\overline{RAS}$ (t_{RAC}) and the minimum access time from the output enable t_{OED}. Outputs contain valid data as long as both $\overline{CAS}$ and $\overline{G}$ are held low. They return to the high impedance state when either $\overline{CAS}$ or $\overline{G}$ go high.

$\overline{RAS}$-Only Refresh

The MB81416's dynamic memory cells may be refreshed by performing any memory cycle at each of the 128 row addresses (A_0 through A_6) at least every 2 milliseconds. When a row is accessed all bits in the row are refreshed. During refresh, A_7 (Pin 10) is not used and either V_{IH} or V_{IL} may be applied to this pin.

$\overline{RAS}$-only Refresh is a simplified cycle that consists of strobing a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. During a $\overline{RAS}$-only Refresh cycle, $\overline{CAS}$ is high and the output buffers are in the high impedance state. Strobing each of the 128 row addresses (A_0 through A_6) with $\overline{RAS}$ will refresh all 65,536 memory cells in the MB81416. $\overline{RAS}$-only Refresh results in a substantial reduction in power dissipation compared to a full $\overline{RAS}/\overline{CAS}$ memory cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set-up time (t_{FCS}) before $\overline{RAS}$ goes low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden $\overline{CAS}$ Before $\overline{RAS}$ Refresh

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$ before $\overline{RAS}$ refresh capability.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle provides a convenient way to verify the functionality of the $\overline{CAS}$ before $\overline{RAS}$ refresh circuitry. The cycle

***Note:** $\overline{CAS}$ Before $\overline{RAS}$ Refresh available on request.

begins with a $\overline{CAS}$ before $\overline{RAS}$ operation. Then $\overline{CAS}$ is cycled "high" and then "low". This enables a read, write, or read-modify-write operation to occur. Four memory cells are accessed with the location defined as follows:

Row Address — Bits A_0 through A_6 are supplied by the on-chip refresh counter. Bit A_7 is set low internally.

Column Address — Bits A_1 through A_6 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Procedure

The $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle timing is used in each of the following steps:

1. Initialized the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into each set of 4 memory cells at a single column address and 128 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 128 times so that "highs" are written into the 128 sets of 4 memory cells.
4. Read the highs written during step 3.
5. Compliment the test pattern and repeat steps 2, 3, and 4.

Page Mode

Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to read, write, or read-modify-write. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to setup and strobe sequential row addresses for the same page. Up to 64 nibble wide words may be accessed with the same row address.

Preliminary

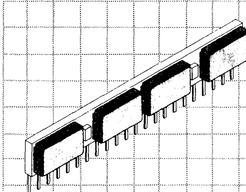
FUJITSU

MB85101A-10, MB85101A-12, MB85101A-15
MOS 65,536 x 4-Bit Dynamic RAM Module

Description

The Fujitsu MB85101A is a 64K x 4 dynamic RAM high density memory module. It consists of four MB8264A DRAMs in 18-pad LCC packages mounted on a 22-pin multilayer ceramic substrate.

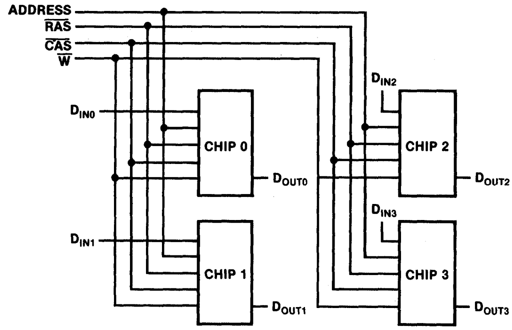
The MB85101A is intended for use in memory applications in which large amounts of memory are required in a compact space or in which board space is limited. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desktop computers and peripheral storage.

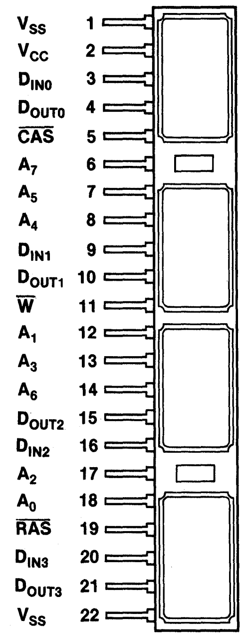


Features

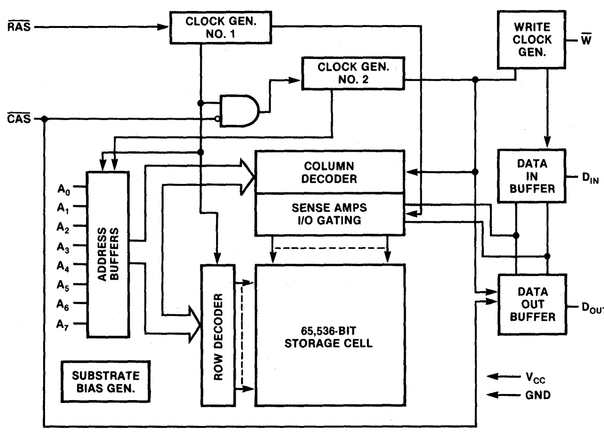
- 65,536 x 4-bit DRAM module
- Row Access Time
  100 ns max. (MB85101A-10)
  120 ns max. (MB85101A-12)
  150 ns max. (MB85101A-15)
- Cycle Time
  200 ns min. (MB85101A-10)
  230 ns min. (MB85101A-12)
  260 ns min. (MB85101A-15)
- Single +5 V supply, ±10% tolerance
- Low power (active)
  1100 mW max. (MB85101A-10)
  990 mW max. (MB85101A-12)
  880 mW max. (MB85101A-15)
  88 mW max. (standby)
- 2 ms/128 cycle refresh
- $\overline{RAS}$-only and Hidden refresh capability
- Read-Modify-Write and Page Mode capability
- Common I/O capability using Early Write operation
- Output unlatched at cycle end allows extended page boundary and two dimentional chip selects.
- On-chip latches for Addresses and Data-in

MB85101 Block Diagram and Pin Assignment



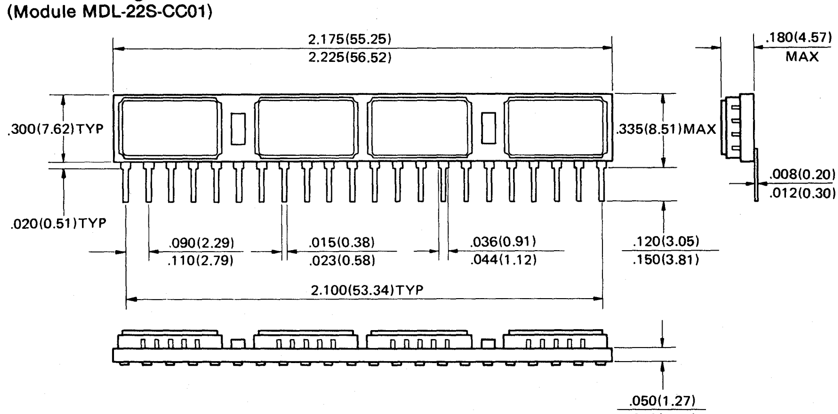


Block Diagram for Each Chip



Package Dimensions
Dimensions in inches (millimeters)

22-Lead Single In-Line Package
(Module MDL-22S-CC01)



Preliminary

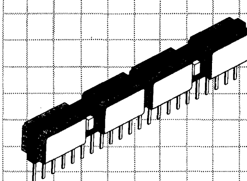
FUJITSU

MB85103A-12, MB85103A-15
MOS 65,536 x 8-Bit Dynamic RAM Module

Description

The Fujitsu MB85103A is a 64K x 8 dynamic RAM high density memory module. It consists of eight MB8264A DRAMs in 18-pad LCC packages mounted on a 22-pin multilayer ceramic substrate.

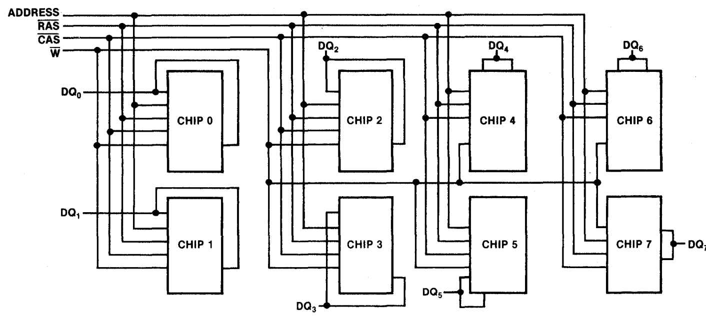
The MB85103A is intended for use in memory applications in which large amounts of memory are required in a compact space or in which board space is limited. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desktop computers and peripheral storage.

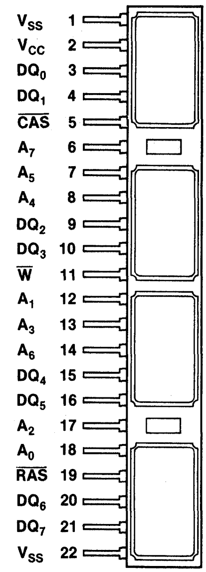


Features

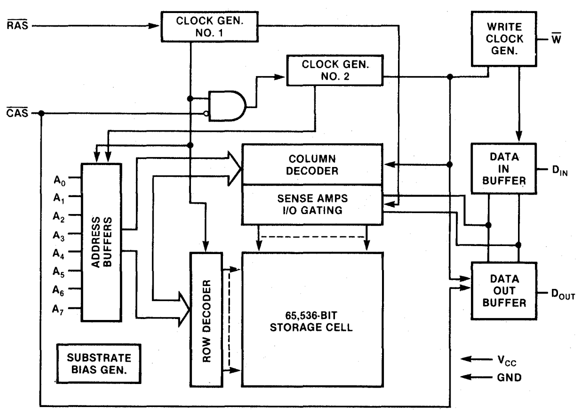
- **65,536 x 8-bit DRAM module**
- **Row Access Time**
  120 ns max. (MB85103A-12)
  150 ns max. (MB85103A-15)
- **Cycle Time**
  230 ns min. (MB85103A-12)
  260 ns min. (MB85103A-15)
- **Single +5 V supply, ±10% tolerance**
- **Low power (active)**
  1980 mW max. (MB85103A-12)
  1760 mW max. (MB85103A-15)
  176 mW max. (standby)
- **2 ms/128 cycle refresh**
- **$\overline{\text{RAS}}$-only and Hidden refresh capability**
- **Page Mode capability**
- **Common I/O**
- **Output unlatched at cycle end allows extended page boundary and two dimentional chip selects.**
- **On-chip latches for Addresses and Data-in**

MB85103 Block Diagram and Pin Assignment



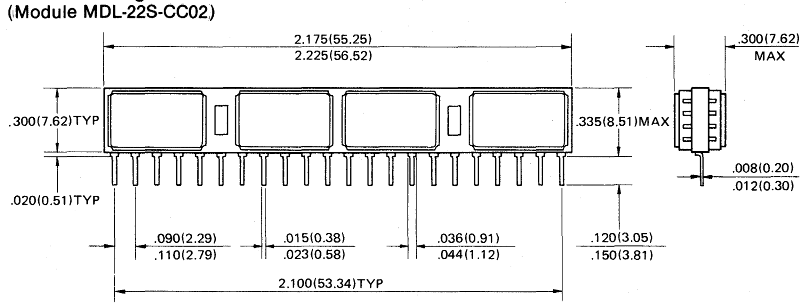


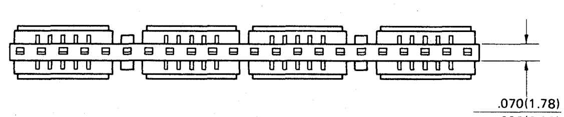
Block Diagram for Each Chip



Package Dimensions
Dimensions in inches (millimeters)

22-Lead Single In-Line Package
(Module MDL-22S-CC02)





Preliminary

FUJITSU

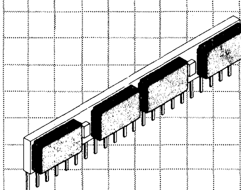
■ MB85108A-12, MB85108A-15
MOS 262,144 x 1-Bit Dynamic RAM Module

Description

The Fujitsu MB85108A is a 256K x 1 dynamic RAM high density memory module. It consists of four MB8266A DRAMs in 18-pad LCC packages mounted on a 22-pin multilayer ceramic substrate.

The MB85108A is intended for use in memory applications in which large amounts of memory are required in a compact space or in which board space is limited. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desktop computers, and peripheral storage.

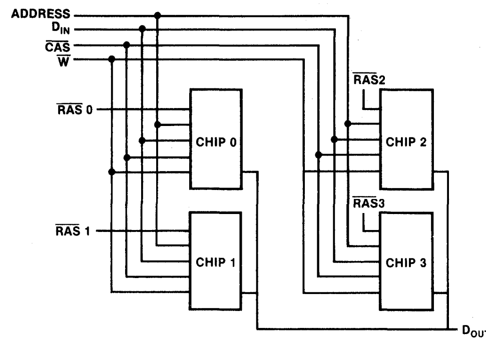
The MB85108A features two new functional enhancements that make it more versatile than previous dynamic RAM's. The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh mode provides an on-chip refresh capability. The nibble mode function allows high speed serial access to up to 4 bits of data.

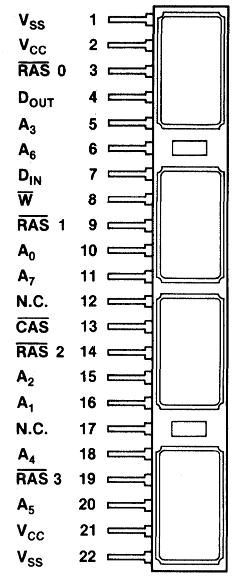


Features

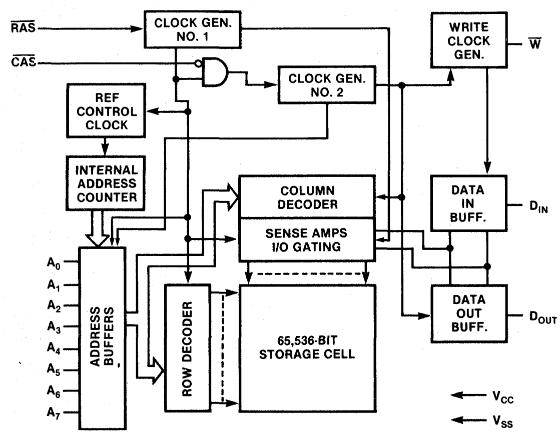
- **262,144 x 1-bit DRAM module**
- **Row Access Time**
  120 ns max. (MB85108A-12)
  150 ns max. (MB85108A-15)
- **Cycle Time**
  230 ns min. (MB85108A-12)
  260 ns min. (MB85108A-15)
- **Nibble Cycle Time**
  70 ns min. (MB85108A-12)
  90 ns min. (MB85108A-15)
- **Single +5 V supply, ±10% tolerance**
- **Low power (active)**
  341 mW max. (MB85108A-12)
  303 mW max. (MB85108A-15)
  99 mW max. (standby)
- **2 ms/128 cycle refresh**
- **$\overline{\text{RAS}}$-only, Hidden and $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability**
- **Read-Modify-Write capability**
- **Nibble Mode capability**
- **Common I/O capability using Early Write**
- **On-chip Address and Data-in latches**
- **Output unlatched at cycle end allows extended page boundary and two dimentional chip selects.**

MB85108 Block Diagram and Pin Assignment



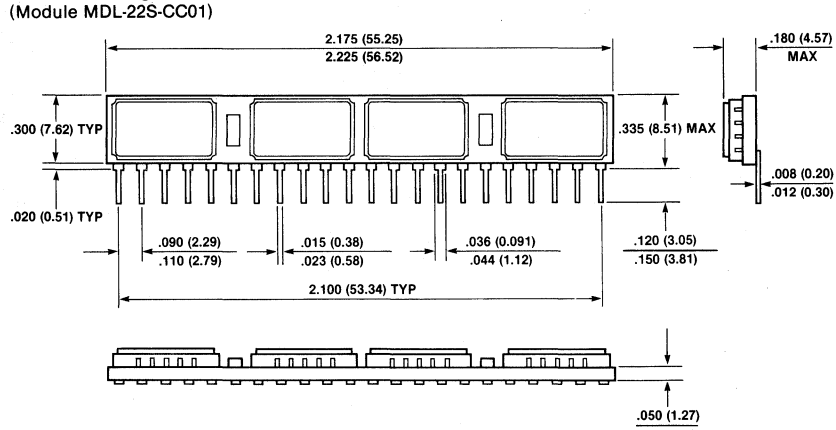


Block Diagram for Each Chip



Package Dimensions
Dimensions in inches
(millimeters)

22-Lead Single In-Line Package
(Module MDL-22S-CC01)



NMOS Static RAMs

Quick Guide To Products in This Section

Device	Organization	Access Time (max)	Power Supply Volts	Power Dissipation	Package	Page
MB8128-10	2K x 8	100 nS	+5	550/110 mW	24-pin	2-2
MB8128-15	2K x 8	150 nS	+5	385/83 mW	24-pin	2-2
MB8167A-55	16K x 1	55 nS	+5	660/140 mW	20-pin	2-7
MB8167A-70	16K x 1	70 nS	+5	660/140 mW	20-pin	2-7
MB8168-55	4K x 4	55 nS	+5	825/220 mW	20-pin	2-12
MB8168-70	4K x 4	70 nS	+5	825/220 mW	20-pin	2-12

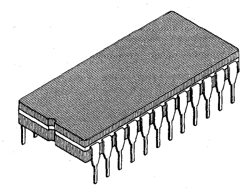
MB8128-10
MB8128-15

NMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

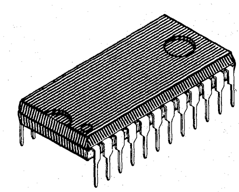
DESCRIPTION

The MB8128 is fabricated using N-channel silicon gate MOS technology. It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.

MB8128 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required. The MB8128 is compatible with TTL logic families in all respects; inputs, outputs and a single +5V supply.



CERDIP PACKAGE
DIP-24C-C03

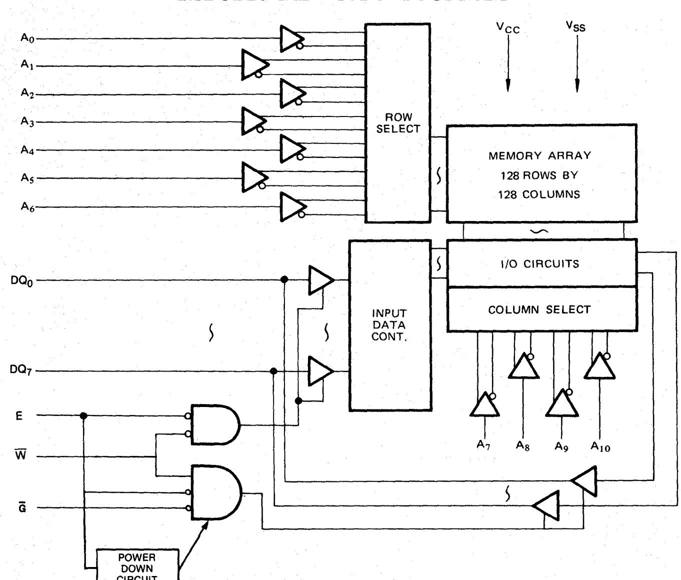


PLASTIC PACKAGE
DIP-24P-M01

FEATURES

- **2048 words x 8-bit organization**
- **Static operation: no clocks or refresh required**
- **Fast access time:**
  MB8128-10 100 ns Max.
  MB8128-15 150 ns Max.
- **Single +5V supply voltage**
- **Common data inputs and outputs**
- **TTL compatible inputs and outputs**
- **Three-state output with OR-tie capability**
- **Chip Enable for simplified memory expansion**
- **Automatic power down**
- **Industry standard 24-pin DIP package**
- **Pin compatible with MB8416 (CMOS Static RAM) and MBM2716 (EPROM)**

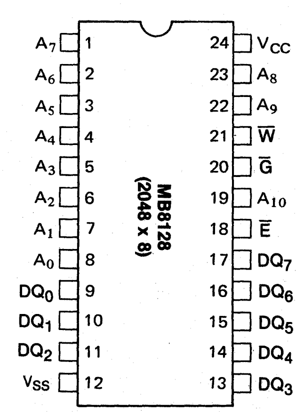
MB8128 BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	NOT SELECTED	I_{SB}	HIGH Z
L	H	H	D_{OUT} DISABLE	I_{CC}	HIGH Z
L	L	H	READ	I_{CC}	D_{OUT}
L	X	L	WRITE	I_{CC}	D_{IN}

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on Any Pin With Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	– 3.5 to +7	V
Temperature Under Bias	T_A	– 10 to +85	°C
Storage Temperature	T_{STG}	– 65 to +150	°C
Power Dissipation	P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient (1) Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.2	—	6.0	V	

NOTE: 1) The operating ambient temperature range is guaranteed with traverse airflow exceeding 2 linear meters/second.

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter			Symbol	Min	Typ	Max	Unit
Input Leakage Current ($V_{IN} = V_{SS}$ to V_{CC}, V_{CC} = Max)			I_{LI}	−10	—	10	μA
Input/Output Leakage Current ($\overline{E}$ or $\overline{G} = V_{IH}$, $V_{I/O} = V_{SS}$ to V_{CC}, V_{CC} = Max)			I_{LO}	−10	—	10	μA
Power Supply Current (V_{CC} = Max, $\overline{E} = V_{IL}$, DQ = Open)	T_A = 25°C	MB8128-10	I_{CC}	—	70	—	mA
		MB8128-15		—	50	—	
	T_A = 0°C	MB8128-10		—	—	100	
		MB8128-15		—	—	70	
Output Low Voltage (I_{OL} = 2.1 mA)			V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 1.0 mA)			V_{OH}	2.4	—	—	V
Standby Current (V_{CC} = Min to Max, $\overline{E} = V_{IH}$)		MB8128-10	I_{SB}	—	8	20	mA
		MB8128-15		—	6	15	
Peak Power-On Current ($V_{CC} = V_{SS}$ to V_{CC} Min, $\overline{E}$ = Lower of V_{CC} or V_{IH} Min)		MB8128-10	I_{PO}	—	—	20	mA
		MB8128-15		—	—	15	

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

READ CYCLE

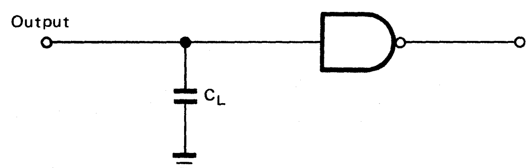
Parameter	Symbol	MB8128-10			MB8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Read Cycle Time	TAVAV	100	—	—	150	—	—	ns
Address Access Time	TAVQV	—	—	100	—	—	150	ns
Chip Enable Access Time	TELQV	—	—	100	—	—	150	ns
Output Hold from Address Change	TAXQX	15	—	—	20	—	—	ns
Chip Enable to Output Active	TELQX	0	—	—	0	—	—	ns
Chip Enable to Output in High Z	TEHQX	—	—	40	—	—	60	ns
Output Enable to Output Valid	TGLQV	—	—	50	—	—	60	ns
Output Enable to Output Active	TGLQX	10	—	—	10	—	—	ns
Output Enable to Output in High Z	TGLQZ	—	—	40	—	—	60	ns
Chip Select to Power Up Time	TELIH	0	—	—	0	—	—	ns
Chip Select to Power Down Time	TEHIL	—	—	40	—	—	60	ns

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Input/Output Capacitance (V_{OUT} = 0V)	$C_{I/O}$	—	7	pF

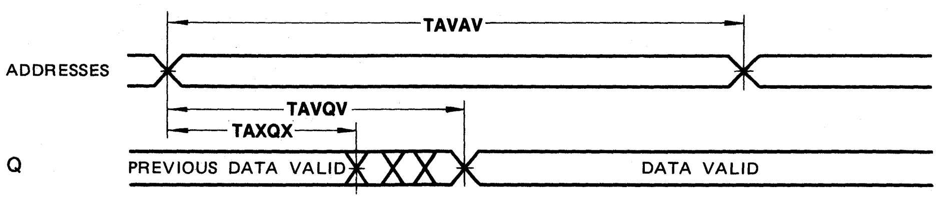
AC TEST CONDITIONS

Input Pulse Levels:	0.8V to 2.4V
Input Pulse Rise and Fall Time:	10 ns
Timing Measurement Reference Levels:	Input: 1.5V
	Output: 1.5V
Output Load:	1 TTL Gate and C_L = 100 pF

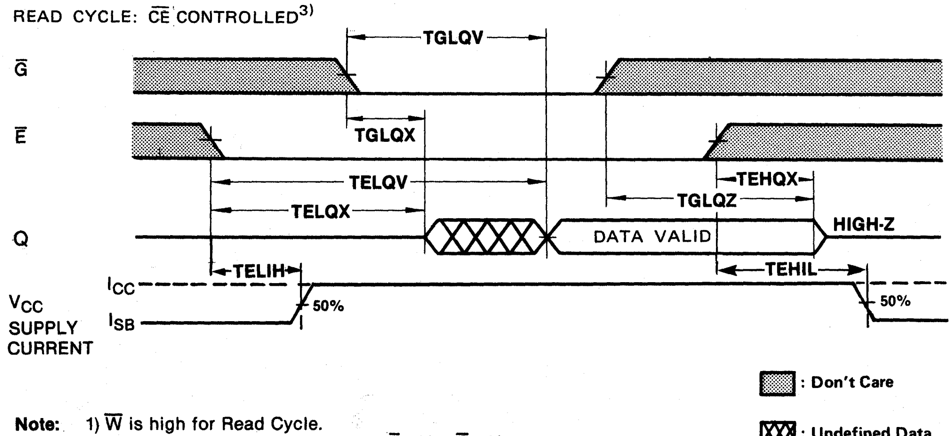


READ CYCLE

READ CYCLE: ADDRESS CONTROLLED[2)]



READ CYCLE: $\overline{CE}$ CONTROLLED[3)]

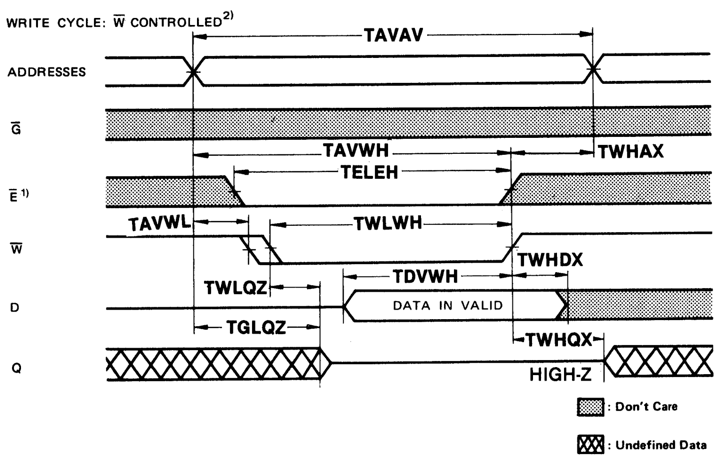


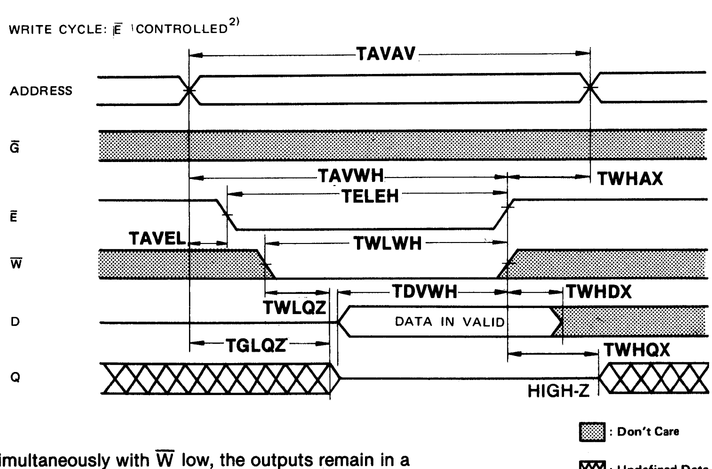
Note: 1) $\overline{W}$ is high for Read Cycle.
2) Device is continuously selected, $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$.
3) Addresses valid prior to or coincident with $\overline{E}$ transition low.

WRITE CYCLE

Parameter	Symbol	MB8128-10			MB8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Cycle Time	TAVAV	100	—	—	150	—	—	ns
Address Valid to End of Write	TAVWH	95	—	—	140	—	—	ns
Chip Select to End of Write	TELEH	95	—	—	140	—	—	ns
Data Valid to End of Write	TDVWH	40	—	—	60	—	—	ns
Data Hold Time	TWHDX	5	—	—	5	—	—	ns
Write Pulse Width	TWLWH	85	—	—	130	—	—	ns
Write Recovery Time	TWHAX	5	—	—	10	—	—	ns
Address Setup Time	TAVWL	0	—	—	0	—	—	ns
	TAVEL	0	—	—	0	—	—	ns
Output Active From End of Write	TWHQX	10	—	—	10	—	—	ns
Write Enable to Output in High Z	TWLQZ	—	—	40	—	—	60	ns

WRITE CYCLE





Note: 1) If $\overline{E}$ goes low simultaneously with $\overline{W}$ low, the outputs remain in a high impedance state.
2) $\overline{E}$ or $\overline{W}$ must be high during address transitions.

OVERVIEW

The MB8128 from Fujitsu is a high performance part, designed for high speed and low system power requirements.

The high speed is obtained by advanced NMOS processing. The low system power requirements are achieved by the use of the MB8128 chip enable (active low). The MB8128 automatically enters standby operation drawing only I_{SB} whenever the chip enable is high. Upon activation of chip enable ($\overline{E}$ = LOW) the MB8128 automatically powers up. This automatic power up/down is an extremely useful feature. Care must be used as proper decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

FUJITSU

■ MB8167A-55, MB8167A-70
NMOS 16,384-Bit Static Random Access Memory

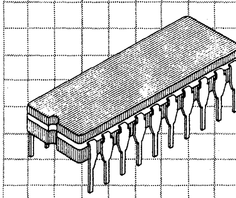
Description

The Fujitsu MB8167A is a 16,384 words by 1-bit static random access memory fabricated using N-channel silicon gate MOS technology. Separate input/output pins are provided. All devices are fully compatible with TTL logic families in all respects: inputs, output and the use of a single +5 V DC supply.

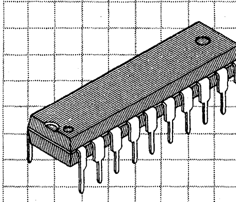
For ease of use, chip enable ($\bar{E}$) permits the selection of an individual package when outputs are OR-tied, and automatically powers down the MB8167A. This device offers the advantages of low power dissipation, low cost, and high performance.

Features

- **Organized as 16,384 words x 1-bit**
- **Static operation: no clocks or refresh required**
- **Fast Access Time:**
  - **MB8167A-55 55 ns Max.**
  - **MB8167A-70 70 ns Max.**
- **Single +5 V DC supply voltage**
- **Separate data input and output**
- **TTL compatible inputs and output**
- **Three-state output with OR-tie capability**
- **Chip enable for simplified memory expansion and automatic power down**
- **All inputs and output have protection against static charge**
- **Standard 20-pin DIP package**

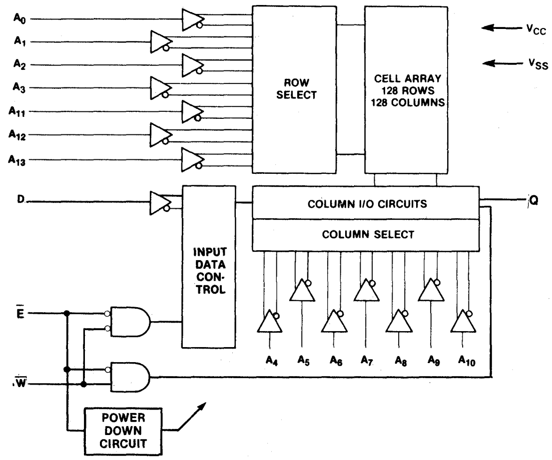


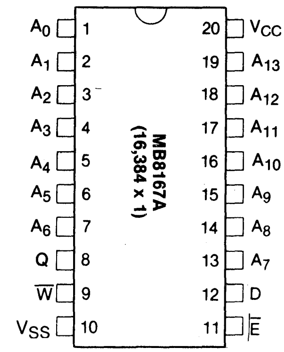
Cerdip Package
DIP-20C-C03



Plastic Package
DIP-20P-M01

MB8167A Block Diagram and Pin Assignment





Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}		VIN, VOUT, VCC	−3.5 to +7	V
Temperature Under Bias		TA	−10 to +85	°C
Storage Temperature	Ceramic	TSTG	−65 to +150	°C
	Plastic	TSTG	−55 to +125	
Power Dissipation		PD	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance
(T_A = 25°C; f = 1 MHz, this parameter is sampled, not 100% tested.)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0V)	CIN	—	5	pF
Output Capacitance (VOUT = 0V)	COUT	—	6	pF

Recommended Operating Conditions
(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	VCC	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	VIL	−3.0	—	0.8	V	
Input High Voltage	VIH	2.0	—	6.0	V	

Note: (1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 2 linear meters/second.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

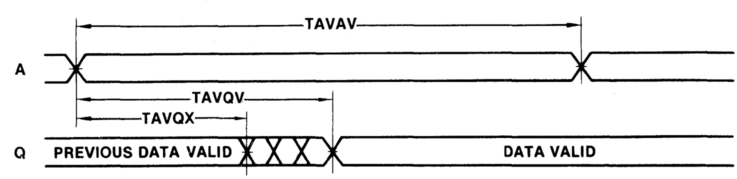
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (VIN = VSS to VCC, VCC = Max)	ILI	—	0.01	10	µA
Output Leakage Current $\overline{E}$ = VIH, VOUT = VSS to VCC Min, VCC = Max)	I_{LO}	—	0.1	50	µA
Power Supply Current (VCC = Max, $\overline{E}$ = VIL, IOUT = 0mA)	ICC	—	90	120	mA
Output Low Voltage (IOL = 16mA)	VOL	—	—	0.45	V
Output High Voltage (IOH = −4mA)	VOH	2.4	—	—	V
Standby Current (VCC = Min to Max, $\overline{E}$ = VIH	ISB	—	15	25	mA
Peak Power-On Current (VCC = VSS to VCC Min, $\overline{E}$ = Lower of VCC or VIH Min)	IPO	—	—	25	mA

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

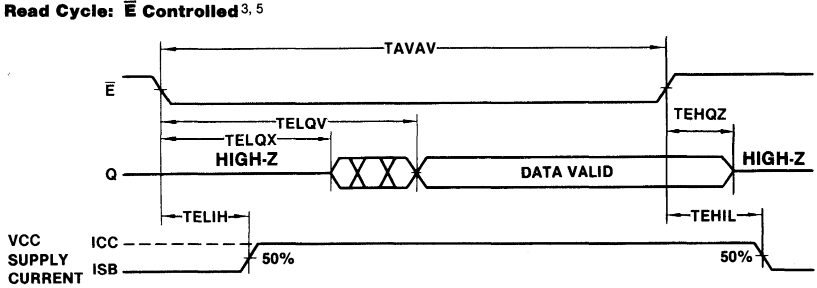
Read Cycle

Parameter	Notes	Symbol	MB8167A-55 Min	MB8167A-55 Max	MB8167A-70 Min	MB8167A-70 Max	Unit
Read Cycle Time		TAVAV	55	—	70	—	ns
Address Access Time		TAVQV	55	—	70	ns	
Chip Enable Access Time		TELQV	—	55	—	70	ns
Output Hold from Address Change		TAVQX	5	—	5	—	ns
Chip Enable to Output Active	1 2	TELQX	10	—	10	—	ns
Chip Enable to Output in High Z	1 2	TEHQZ	0	30	0	40	ns
Chip Enable to Power Up Time		TELIH	0	—	0	—	ns
Chip Enable to Power Down Time		TEHIL	—	30	—	35	ns

Read Cycle: Address Controlled[3,4]



Read Cycle: $\overline{E}$ Controlled[3,5]



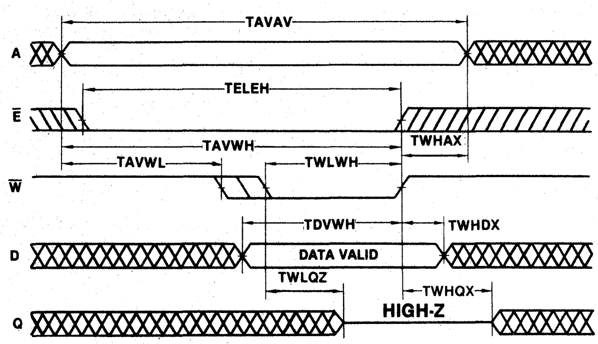
Notes:
1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig.2.
3. $\overline{W}$ is high for Read Cycle.
4. Device is continuously selected, $\overline{E}$ = VIL.
5. Addresses valid prior to or coincident with $\overline{E}$ transition low.

AC Characteristics
(Recommended operating conditions unless otherwise noted.) (continued)

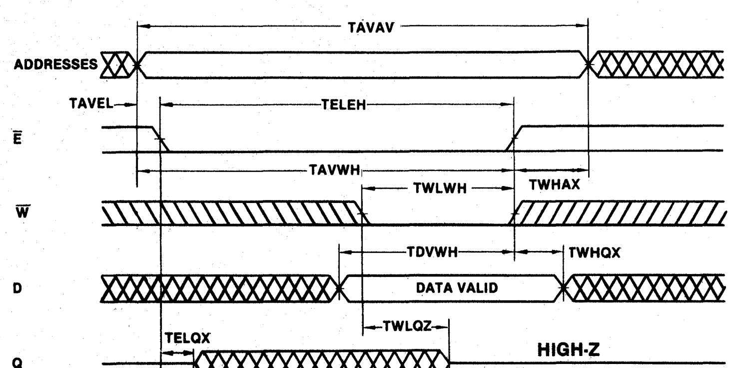
Write Cycle

Parameter	Notes	Symbol	MB8167A-55 Min	MB8167A-55 Max	MB8167A-70 Min	MB8167A-70 Max	Unit
Write Cycle Time		TAVAV	55	—	70	—	ns
Address Valid to End of Write		TAVWH	45	—	50	—	ns
Chip Enable to End of Write		TELEH	50	—	60	—	ns
Data Valid to End of Write		TDVWH	35	—	45	—	ns
Data Hold Time		TWHDX	0	—	0	—	ns
Write Pulse Width		TWLWH	35	—	45	—	ns
Write Recovery Time		TWHAX	5	—	10	—	ns
Address Setup Time		TAVWL	5	—	5	—	ns
		TAVEL	0	—	0	—	ns
Output Active From End of Write	7 8	TWHQX	0	—	0	—	ns
Write Enable to Output in High Z	7 8	TWLQZ	—	30	—	35	ns

Write Cycle: $\overline{W}$ Controlled 9



Write Cycle: $\overline{E}$ Controlled 9

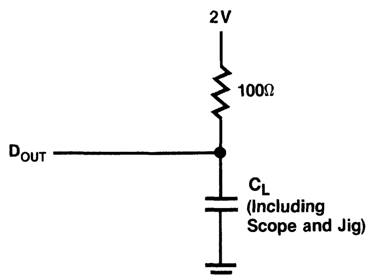


Notes:
6. If $\overline{E}$ goes high simultaneously with $\overline{W}$-high, the output remains in a high impedance state.
7. Transition is measured at the point of ±500mV from steady state voltage.
8. This parameter is measured with specified loading in Fig. 2.
9. $\overline{E}$ or $\overline{W}$ must be high during address transitions.

AC Test Conditions

Input Pulse Levels:	0.8 V to 2.2 V
Input Pulse Rise and Fall Times:	5 ns
Timing Measurement Reference Levels:	Inputs: 1.5 V Output: 1.5 V
Load Capacitance:	5 pF for TEHQZ, TWLQZ, TELQX and TWHQX 30 pF for all others

Fig. 2: Output Load



FUJITSU
MICROELECTRONICS, INC.

MB8168-55
MB8168-70

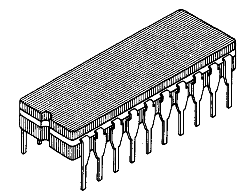
NMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

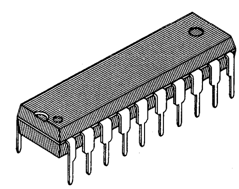
The Fujitsu MB8168 is a 4096 word by 4-bit static random access memory fabricated using N-channel silicon gate MOS technology. The memory is fully static and requires no clock or timing strobe. All pins are TTL compatible and a single 5V power supply is required.

A separate chip select $\overline{E}$ pin simplifies multipackage system design. It permits the selection of an individual package when outputs are OR-tied. Furthermore, when selecting a single package by $\overline{E}$, the other deselected packages automatically power down.

All Fujitsu devices offer the advantages of low power dissipation, low cost and high performance.



CERDIP PACKAGE
DIP-20C-C03

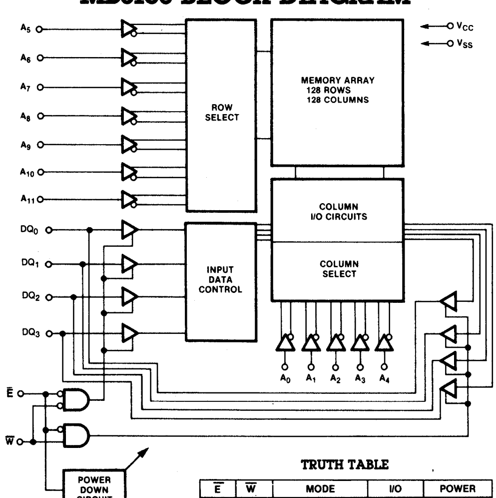


PLASTIC PACKAGE
DIP-20P-M01

FEATURES

- **Organized as 4096 words x 4-bits**
- **Fully Static Operation, no clocks or timing strobe required**
- **Fast Access Time:**
  MB8168-55 55 ns Max.
  MB8168-70 70 ns Max.
- **Low Power Consumption:**
  I_{CC} = 150mA Max. (Active)
  I_{SB} = 40mA Max.(Standby)
- **Single +5V DC Supply Voltage, ±10% tolerance**
- **Common data input and output**
- **Three-state output with OR-tie capability**
- **Chip select for simplified memory expansion, automatic power-down**
- **Standard 20-pin DIP package**
- **Pin compatible with Intel 2168**

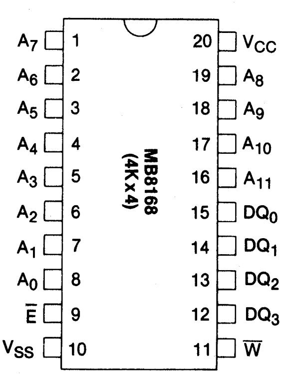
MB8168 BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7.0	V
Short Circuit Output Current	—	20	mA
Temperature Under Bias	T_A	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	6.0	V	

Note: 1. The operating ambient temperature range is guaranteed with transverse airflow exceeding 2 linear meters/second.

CAPACITANCE (T_A = 25 °C, f = 1 MHz, this parameter is sampled, not 100% tested.)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance Address, $\overline{W}$: V_{IN} = 0V	C_{IN}	—	7	pF
Input Capacitance $\overline{E}$: V_{IN} = 0V	$C_{\overline{E}}$	—	8	pF
Output Capacitance Data I/O, V_{OUT} = 0V	C_{OUT}	—	8	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{OUT} = V_{SS} to 4.5V, V_{CC} = Max)	I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{E}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC}	—	150	mA
Output Low Voltage (I_{OL} = 8mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)	V_{OH}	2.4	—	V
Standby Current (V_{CC} = Min to Max, $\overline{E}$ = V_{IH}, I_{OUT} = 0mA)	I_{SB}	—	40	mA
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{E}$ = Lower of V_{CC} or V_{IH} Min)	I_{PO}	—	50	mA
Output Short Circuit Current (V_{OUT} = V_{SS} to V_{CC})	I_{OS}	−200	200	mA

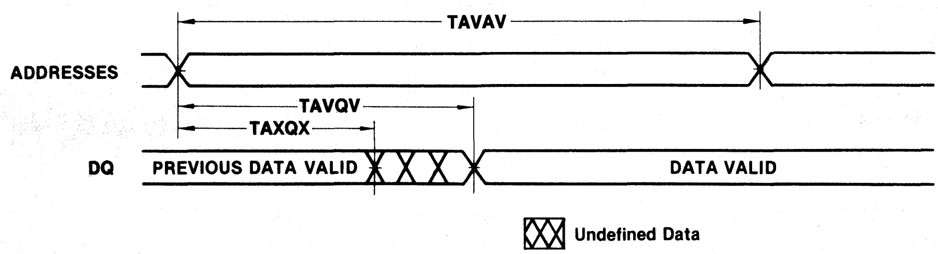
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

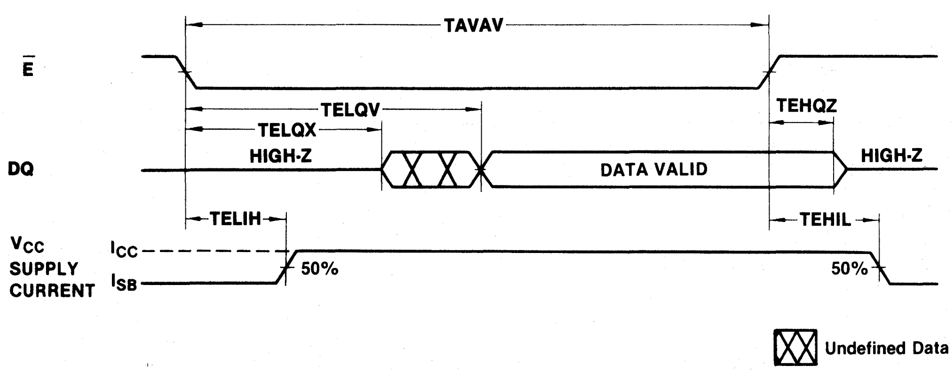
READ CYCLE

Parameter	NOTES	Symbol	MB8168-55			MB8168-70			Unit
			Min	Typ	Max	Min	Typ	Max	
Read Cycle Time		TAVAV	55	—	—	70	—	—	ns
Address Access Time		TAVQV	—	—	55	—	—	70	ns
Chip Enable Access Time		TELQV	—	—	55	—	—	70	ns
Output Hold from Address Change		TAXQX	5	—	—	5	—	—	ns
Chip Enable to Output Active	1 2	TELQX	10	—	—	10	—	—	ns
Chip Enable to Output in High Z	1 2	TEHQZ	0	—	30	0	—	40	ns
Chip Enable to Power Up Time	3	TELIH	0	—	—	0	—	—	ns
Chip Enable to Power Down Time	3	TEHIL	—	—	55	—	—	70	ns

READ CYCLE: ADDRESS CHANGING 4,5



READ CYCLE: $\overline{CS}$ CHANGING 4,6

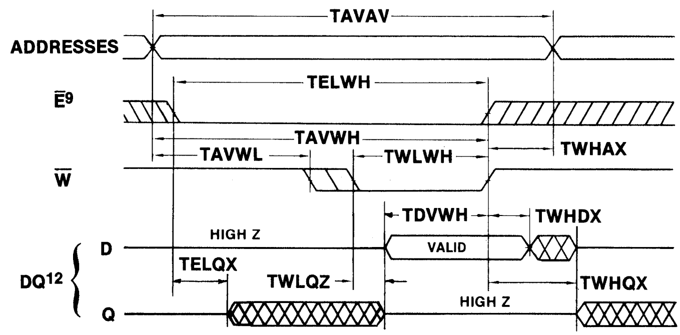


Notes: 1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig. 2. This parameter is sampled and not 100% tested.
3. $I_H = I_{CC\,(Max)}$, $I_L = I_{SB\,(Max)}$
4. $\overline{W}$ is high for Read Cycle.
5. Device is continuously selected. $\overline{E} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{E}$ transition low.

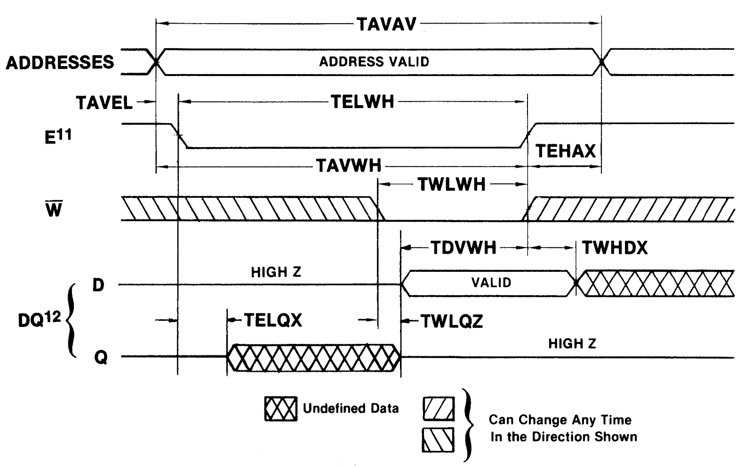
WRITE CYCLE

Parameter	NOTES	Symbol	MB8168-55 Min	MB8168-55 Typ	MB8168-55 Max	MB8168-70 Min	MB8168-70 Typ	MB8168-70 Max	Unit
Write Cycle Time		TAVAV	55	—	—	70	—	—	ns
Address Valid to End of Write		TAVWH	50	—	—	60	—	—	ns
Chip Enable to End of Write		TELWH	50	—	—	60	—	—	ns
Data Valid to End of Write		TDVWH	25	—	—	30	—	—	ns
Data Hold Time		TWHDX	0	—	—	0	—	—	ns
Write Pulse Width		TWLWH	50	—	—	60	—	—	ns
Write Recovery Time		TWHAX, TEHAX	0	—	—	0	—	—	ns
Address Setup Time		TAVWL, TAVEL	0	—	—	0	—	—	ns
Output Active From End of Write	7 8	TWHQX	0	—	—	0	—	—	ns
Write Enable to Output in High Z	7 8	TWLQZ	0	—	30	0	—	40	ns
Chip Enable to Output Active		TELQX	10	—	—	10	—	—	ns

WRITE CYCLE: $\overline{W}$ CONTROLLED[10]



WRITE CYCLE: $\overline{E}$ CONTROLLED[10]



Notes: 7. Transition is measureed at the point of ±500 mV from steady state voltage.
8. This parameter is measured with specified loading in Fig. 2.
9. If $\overline{E}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high impedance state.
10. $\overline{E}$ or $\overline{W}$ must be high during address transitions.
11. If $\overline{W}$ is low for the entire cycle Data Out remains High Z throughout the cycle.
12. Q shows when the DQ pin is driven by the memory chip. D shows when the DQ pin is externally driven.

AC TEST CONDITIONS

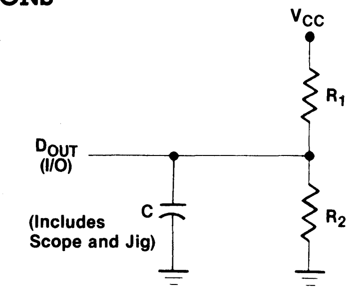
Input Conditions:

Input Pulse Levels:	**0V to 3.0V**
Input Pulse Rise/Fall Times:	**5 ns**
Input Timing Reference Level:	**1.5V**

Output Conditions:

Output Timing Reference Level:	**0.8V to 2.0V**
Output Load:	

	R_1	R_2	C	Parameters Measured
Load I	480Ω	255Ω	30pF	except TELQX, TEHQZ, TWLQZ, and TWHQX
Load II	480Ω	255Ω	5pF	TELQX, TEHQZ, TWLQZ, and TWHQX



OUTPUT LOAD

DEVICE OPERATION

Controls

The MB8168 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When $\overline{E} \geq V_{IH}$, the device is deselected and automatically controlled to the standby mode, reducing the power requirements to less than one-sixth of the selected state. When $\overline{E} \leq V_{IL}$, the device is selected (active) and read or write cycles may be performed. $\overline{E}$ should be controlled to track V_{CC} during the initial system power-on to prevent all of the MB8168's in a system from drawing active I_{CC} during power-up.

When $\overline{W} \geq V_{IH}$ and the chip is selected, a read cycle may be performed. When $\overline{W} \leq V_{IL}$ and the chip is selected a write cycle may be performed.

Read Cycle

A read cycle is selected when $\overline{E} \leq V_{IL}$ and $\overline{W} \geq V_{IH}$. Read access time is measured from either the $\overline{E}$ high to low transition or from valid address as shown in the read cycle timing diagrams.

Write Cycle

A write cycle is seleted when $\overline{E} \leq V_{IL}$ and $\overline{W} \leq V_{IH}$. The actual beginning of the write cycle is initiated by the latter of $\overline{E}$ or $\overline{W}$ going low as shown in the write cycle timing diagrams. The address setup times shown in the timing diagrams must be met and the addresses must remain stable for the entire write cycle. The write cycle is terminated by either $\overline{E}$ or $\overline{W}$ going high. If the timing specifications are not met, data may be altered or lost.

In summary, the write cycle may be initiated by the latter of $\overline{E}$ or $\overline{W}$ going low and may be terminated by $\overline{E}$ or $\overline{W}$ going high, whichever occurs first, and the setup and hold times must be referenced to the controlling signal transitions. Either $\overline{E}$ or $\overline{W}$ must be high (greater than V_{IH}), during an address transition.

CMOS Static RAMs

Quick Guide To Products in This Section

Device	Organization	Access Time (max)	Power Supply Volts	Power Dissipation	Package	Page
MB8416-20	2K x 8	200 nS	+5	330 mW/55 μW	24-pin	3-2
MB8416-20L	2K x 8	200 nS	+5	330 mW/5.5 μW	24-pin	3-2
MB8416A-12	2K x 8	120 nS	+5	330 mW/5.5 mW	24-pin	3-8
MB8416A-15	2K x 8	150 nS	+5	330 mW/5.5 mW	24-pin	3-8
MB8416A-12L	2K x 8	120 nS	+5	330 mW/275 μW	24-pin	3-8
MB8416A-15L	2K x 8	150 nS	+5	330 mW/275 μW	24-pin	3-8
MB8417-20	2K x 8	200 nS	+5	330 mW/55 μW	24-pin	3-15
MB8417-20L	2K x 8	200 nS	+5	330 mW/5.5 μW	24-pin	3-15
MB8417A-12	2K x 8	120 nS	+5	330 mW/5.5 mW	24-pin	3-22
MB8417A-15	2K x 8	150 nS	+5	330 mW/5.5 mW	24-pin	3-22
MB8417-12L	2K x 8	120 nS	+5	330 mW/275 μW	24-pin	3-22
MB8417A-15L	2K x 8	150 nS	+5	330 mW/275 μW	24-pin	3-22
MB8418-20	2K x 8	200 nS	+5	330 mW/55 μW	24-pin	3-29
MB8418-20L	2K x 8	200 nS	+5	330 mW/5.5 μW	24-pin	3-29
MB8418A-12	2K x 8	120 nS	+5	330 mW/5.5 mW	24-pin	3-35
MB8418A-15	2K x 8	150 nS	+5	330 mW/5.5 mW	24-pin	3-35
MB8418A-12L	2K x 8	120 nS	+5	330 mW/275 μW	24-pin	3-35
MB8418A-15L	2K x 8	150 nS	+5	330 mW/275 μW	24-pin	3-35
MB8464-10	8K x 8	100 nS	+5	500 mW/11 mW	28-pin	3-42
MB8464-15	8K x 8	150 nS	+5	500 mW/11 mW	28-pin	3-42
MB8464-10L	8K x 8	100 nS	+5	330 mW/1.1 mW	28-pin	3-42
MB8464-15L	8K x 8	150 nS	+5	330 mW/1.1 mW	28-pin	3-42

FUJITSU
MICROELECTRONICS, INC.

MB8416-20
MB8416-20L

CMOS 16384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

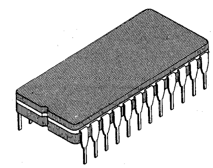
The Fujitsu MB8416 is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

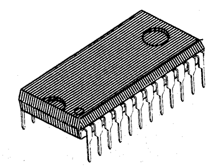
The MB8416 can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Output Enable ($\overline{G}$) input permits the disable of all outputs when outputs are OR-tied. The MB8416 is packaged in an industry standard 24-pin dual in-line package, or 32-pin leadless chip carrier.

FEATURES

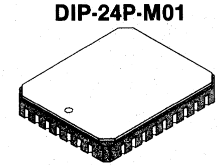
- **Extended temperature range:**
  MB8416-20: −40° to +85°C
  MB8416-20-L: −40° to +70°C
- **Organized as 2048 words by 8-bits**
- **Fast Access Time: 200 ns Max.**
- **Low Standby Power:**
  MB8416-20: 55 μW
  MB8416-20L: 5.5 μW
- **Completely Static Operation, no clocks required**
- **Single +5 Volt Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Low Data Retention Voltage: 2.0V Min.**
- **Pin compatible with HM6116, TC5517 and μPD446**



CERDIP PACKAGE
DIP-24C-C03

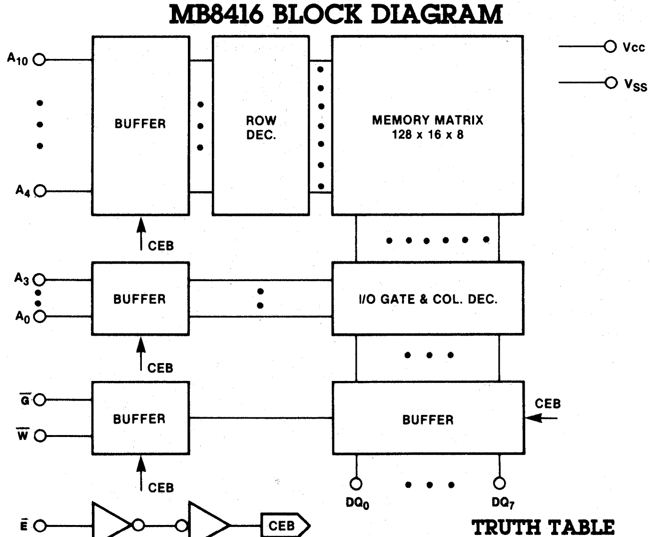


PLASTIC PACKAGE
DIP-24P-M01



LEADLESS CHIP CARRIER
LCC-32C-A02

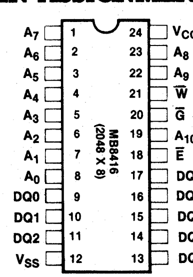
MB8416 BLOCK DIAGRAM

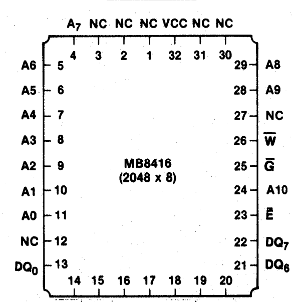


TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
L	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENTS





ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Cerdip	T_{stg}	−65	150	°C
	Plastic		−40	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0V)

Parameter	Symbol		MB8416			Unit
			Min	Typ	Max	
Ambient Temperature	T_A	MB8416-20L	−40	—	+70	°C
		MB8416-20	−40	—	+85	
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		−0.3	—	0.8	V

CAPACITANCE

(T_A = 25°F, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

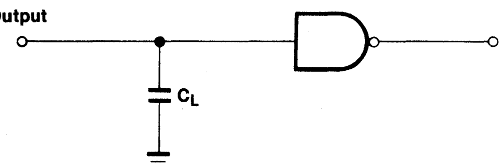
STATIC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Condition	Symbol		Min	Max	Units
Standby Supply Current	$\bar{E} = V_{CC} - 0.2$ to $V_{CC} + 0.2$V $V_{IN} = -0.2$V to V_{CC} +0.2V	I_{SB1}	MB8416-20L	—	1	μA
			MB8416-20	—	10	
Standby Supply Current	$\bar{E} = V_{IH}$ $V_{IN} = -0.2$V to V_{CC} +0.2V	I_{SB2}		—	2	mA
Active Supply Current	$\bar{E} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}		—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}		—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}		−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\bar{E} = V_{IH}$	I_{LO}		−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}		2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}		—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels: 0.6V to 2.4V
Input Pulse Rise and Fall Times: 10 ns
Input Timing Reference Level: 0.8V to 2.2V
Output Timing Reference Level: 0.8V to 2.2V
Output Load: 1 TTL Gate and
C_L = 5 pF for TEHQZ, TGHQZ and TWLQZ
C_L = 100 pF for all others.



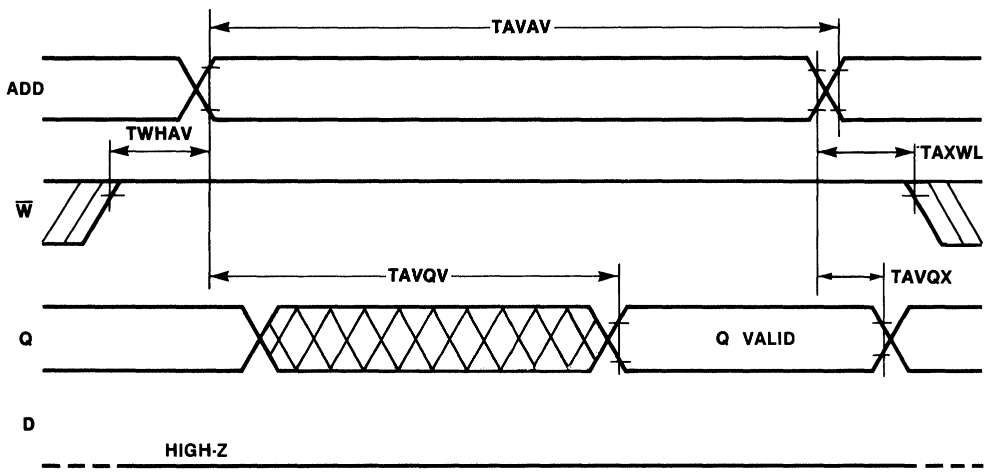
DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAV	200	—	ns
Write Cycle Time	TAVAV	200	—	ns
Address Access Time	TAVQV	—	200	ns
Chip Enable Access Time	TELQV	—	200	ns
Output Hold from Address Change	TAVQX	15	—	ns
Output Low Z from $\overline{E}$	TELQX	15	—	ns
Output High Z from $\overline{E}$	TEHQZ	—	60	ns
Output Low Z from $\overline{G}$	TGLQX	15	—	ns
Output High Z from $\overline{G}$	TGHQZ	—	60	ns
Output Low Z from $\overline{W}$	TWHQX	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	60	ns
Output Enable to Output Valid	TGLQV	—	100	ns
Address Set Up Time	TAVEL, TAVWL	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	ns
Write Set Up Time	TWLEL	0	—	ns
Write Hold Time	TEHWH	0	—	ns
Address Valid to End of Write	TAVWH	160	—	ns
Chip Enable to End of Write	TELEH	160	—	ns
Write Pulse Width	TWLWH	140	—	ns
Write Recovery Time	TWHAX, TEHAX	10	—	ns
Data Set Up Time	TDVEH, TDVWH	60	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	ns

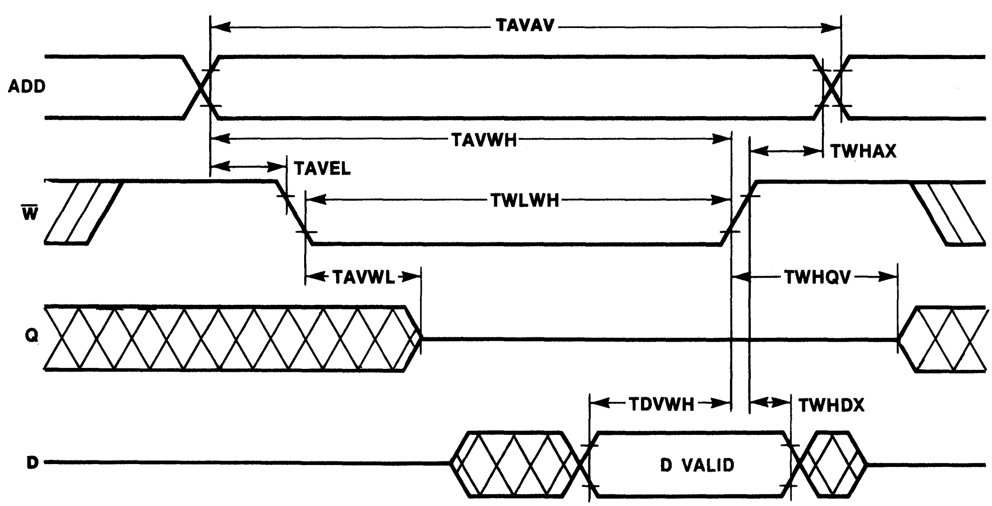
WAVEFORMS

MODE 1: $\overline{W}$ Controlled: ($\overline{E}$ = Low, $\overline{G}$ = Low)

Read Cycle



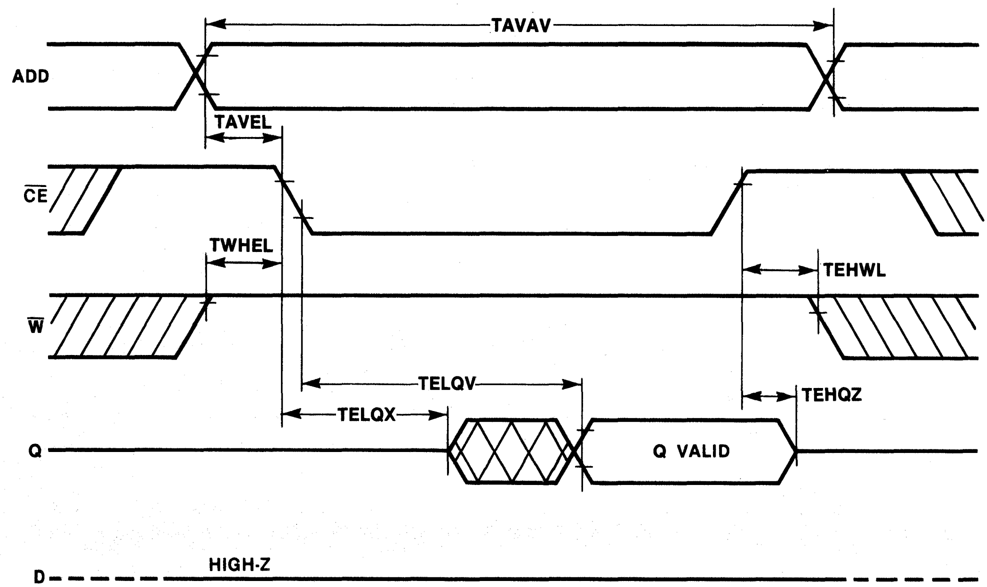
Write Cycle



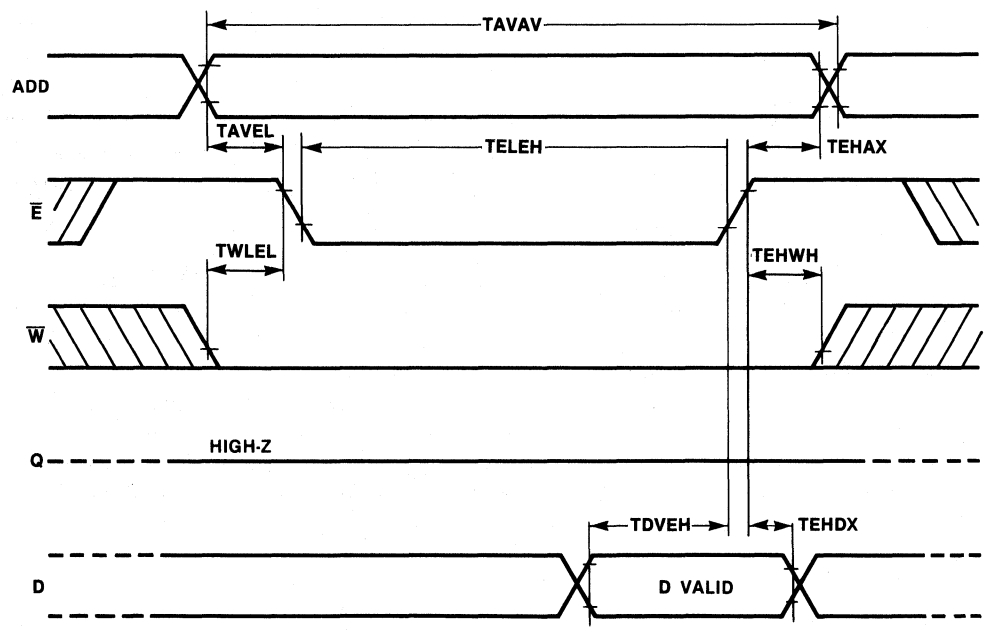
WAVEFORMS (Continued)

MODE 2: $\overline{E}$ Controlled, ($\overline{G}$ = Low)

Read Cycle

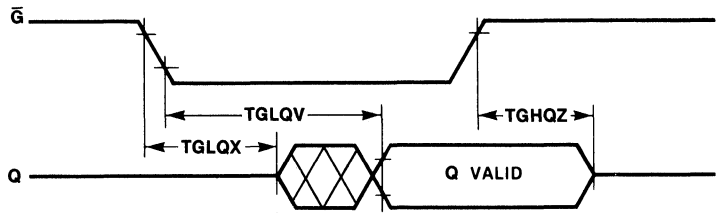


Write Cycle



WAVEFORMS (Continued)

Enable/Disable $\overline{G}$ Controlled; ($\overline{E}$ = Low, $\overline{W}$ = High)
Read Cycle



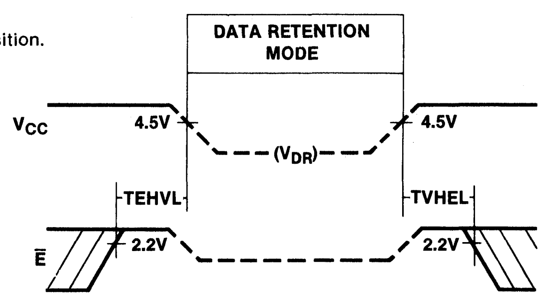
DYNAMIC CHARACTERISTICS

Data Retention Characteristics, NOTES [1, 2, 3] (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol		Min	Max	Unit
Data Retention Supply Voltage	1	VDR		2.0	5.5	V
Data Retention Supply Current	2	IDR	MB8416-20	—	10	μA
			MB8416-20L	—	1	μA
Data Retention Set Up Time	3	TEHVCL		60	—	ns
Recovery Time	3	TVHEL		60	—	ns

NOTES:

1. $\overline{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V
   $\overline{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
2. V_{CC} = VDR = 2.0V, $\overline{E}$ = VDR ± 0.2V V_{IN} = − 0.2V to VDR + 0.2V.
3. V_L = 4.5V on the falling transition, V_H = 4.5V on the rising transition.



FUJITSU

MB8416A-12, MB8416A-12L, MB8416A-15, MB8416A-15L

CMOS 16,384-Bit Static Random Access Memory

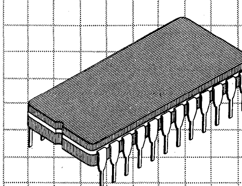
Description

The Fujitsu MB8416A is a 2048-word by 8-bit static random access memory fabricated with CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volt power supply is required.

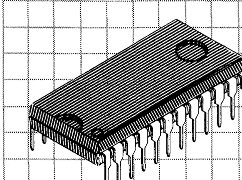
The MB8416A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

Features

- Organization: 2048 words x 8-bits
- Fast Access Time:
  120 ns max. (MB8416A-12/12L)
  150 ns max. (MB8416A-15/15L)
- Completely static operation: No clocks required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply
- Low power standby:
  5.5 mW max. (MB8416A-12/15)
  275μW max. (MB8416A-12L/15L)
- Data retention: 2.0V min.
- Jedec Standard 24-pin DIP (Ceramic Cerdip/Plastic Mold)
- Also Jedec Standard 32 pad LCC package.
- Pin compatible with HM6116, TC5517 and μPD446
- Output Enable ($\overline{G}$) pin for precise data bus control

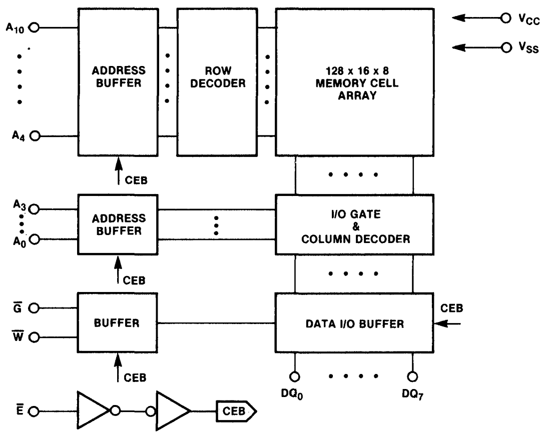


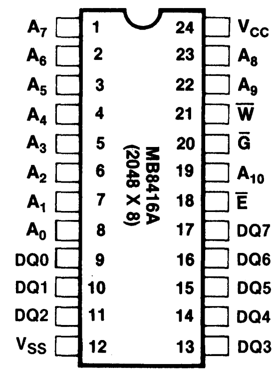
Ceramic Package (Cerdip)
DIP-24C-C03



Plastic Package
DIP-24P-M01

MB8416A Block Diagram and Pin Assignment





Truth Table

$\overline{E}_2$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High-Z
L	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Storage Temperature	Cerdip	T_{stg}	−65 to +150	°C
	Plastic		−40 to +125	
Temperature Under Bias		T_{bias}	−10 to +85	°C
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC}+0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5 to V_{CC}+0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	—	—	10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	—	7	pF

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Ambient Temperature	T_A	0	—	70	°C

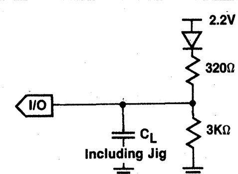
DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	MB8416A-12/15 Min	MB8416A-12/15 Max	MB8416A-12L/15L Min	MB8416A-12L/15L Max	Unit
Standby Supply Current 1	$\overline{E} = V_{CC} - 0.2$ to $V_{CC} + 0.2V$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	—	1	—	0.05	mA
Standby Supply Current 2	$\overline{E} = V_{IH}$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}	—	2	—	1	mA
Active Supply Current	$\overline{E} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}	—	60	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}	—	60	—	60	mA
Input Leakage Current	$V_{IN} = 0V$ to V_{CC}	I_{LI}	−1.0	1.0	−1.0	1.0	μA
Output Leakage Current	$V_{I/O} = 0V$ to V_{CC} $\overline{E} = V_{IH}$ or $\overline{G} = V_{IH}$	I_{LO}	−1.0	1.0	−1.0	1.0	μA
Output High Voltage	$I_{OUT} = -1.0$ mA	V_{OH}	2.4	—	2.4	—	V
Output Low Voltage	$I_{OUT} = 4.0$ mA	V_{OL}	—	0.4	—	0.4	V

Note: All voltages are referenced to GND.

AC Test Conditions

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Times:	5ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$ Output: $V_{OL} = 0.8V$, $V_{OH} = 2.2V$
Output Load:	$C_L = 5_{PF}$ for TEHQZ, TGHQZ and TWLQZ $C_L = 100$ pF for all others.

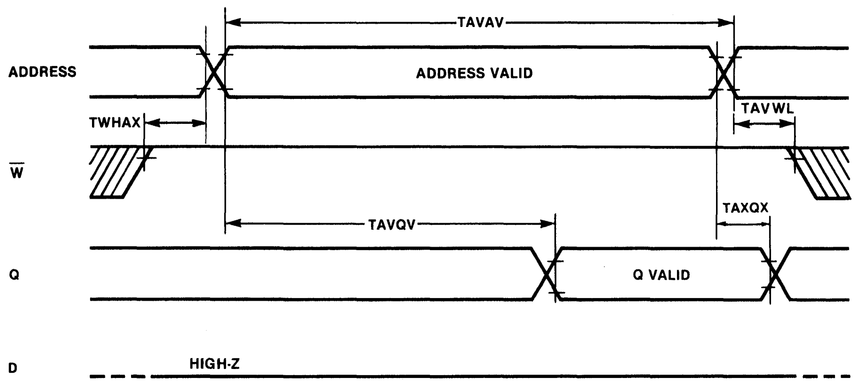


AC Characteristics
(Recommended operating conditions unless otherwise noted.)

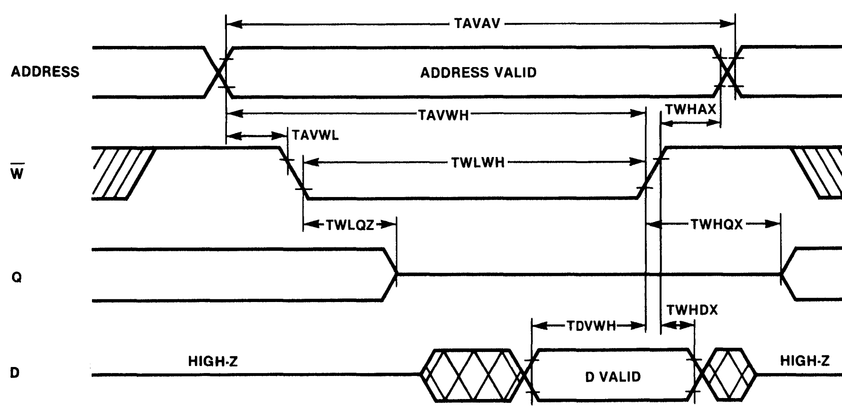
Parameter	Symbol	MB8416A-12/12L Min	MB8416A-12/12L Max	MB8416A-15/15L Min	MB8416A-15/15L Max	Unit
Read Cycle Time	TAVAV	120	—	150	—	ns
Write Cycle Time	TAVAV	120	—	150	—	ns
Address Access Time	TAVQV	—	120	—	150	ns
Chip Enable Access Time	TELQV	—	120	—	150	ns
Output Hold from Address Change	TAXQX	15	—	15	—	ns
Output Low Z from $\overline{E}$	TELQX	15	—	15	—	ns
Output High Z from $\overline{E}$	TEHQZ	—	40	—	50	ns
Output Low Z from $\overline{G}$	TGLQX	10	—	10	—	ns
Output High Z from $\overline{G}$	TGHQZ	—	40	—	50	ns
Output Low Z from $\overline{W}$	TWHQX	15	—	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	40	—	50	ns
Output Enable to Output Valid	TGLQV	—	50	—	60	ns
Address Set Up Time	TAVEL, TAVWL	0	—	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	0	—	ns
Write Set Up Time	TWLEL	0	—	0	—	ns
Write Hold Time	TEHWH	0	—	0	—	ns
Address Valid to End of Write	TAVWH	100	—	120	—	ns
Chip Enabled to End of Write	TELEH	100	—	120	—	ns
Write Pulse Width	TWLWH	70	—	90	—	ns
Write Recovery Time	TWHAX, TEHAX	5	—	5	—	ns
Data Set Up Time	TDVEH, TDVWH	35	—	40	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	0	—	ns

Mode 1 — $\overline{W}$ Controlled
($\overline{E}$ = Low, $\overline{G}$ = Low)

Read Cycle Timing Diagram

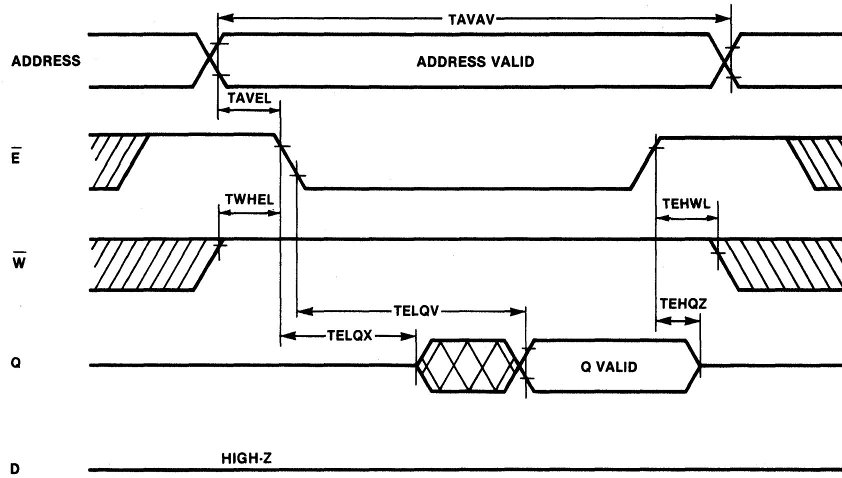


Write Cycle Timing Diagram

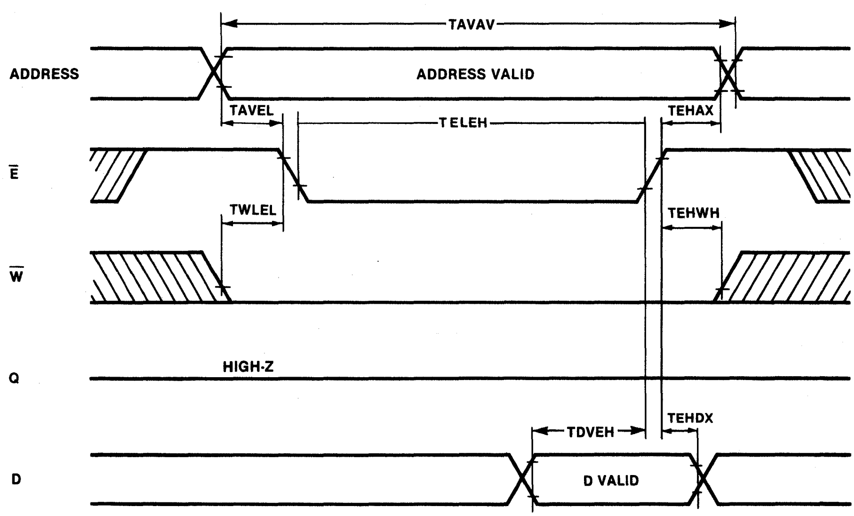


Mode 2 — $\overline{E}$ Controlled
($\overline{G}$ = Low)

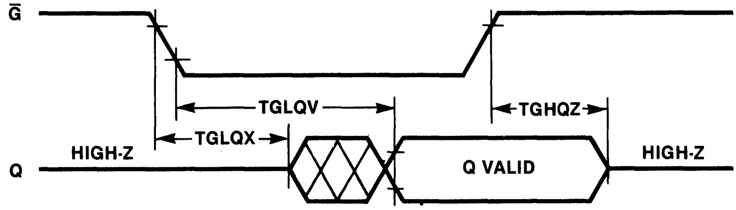
Read Cycle Timing Diagram



Write Cycle Timing Diagram



Mode 3 — $\overline{G}$ Controlled
($\overline{E}$ = Low, $\overline{W}$ = High, Address Valid)

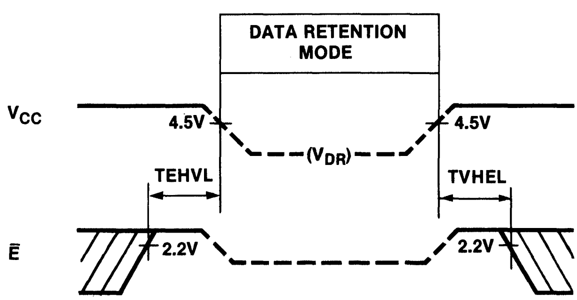


Data Retention Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8416A-12/15 Min	MB8416A-12/15 Max	MB8416A-12L/15L Min	MB8416A-12L/15L Max	Unit	Test Condition
Data Retention Supply Voltage	V_{DR}	2.0	5.5	2.0	5.5	V	Note 1
Data Retention Supply Current	I_{DR}	—	0.5	—	0.03	mA	Note 2
Data Retention Set Up Time	TEHVL	40	—	40	—	ns	Note 3
Recovery Time	TVHEL	40	—	40	—	ns	Note 3

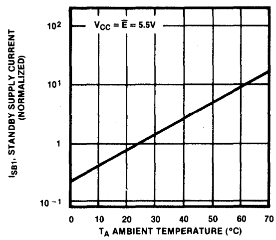
Note 1. $\overline{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V, $\overline{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
Note 2. $V_{CC} = V_{DR}$ = 3.0V, $\overline{E} = V_{DR}$ −0.2V to V_{DR} +0.2V, V_{IN} = −0.2V to V_{DR} +0.2V.
Note 3. V_L = 4.5V on the falling transition, V_H = 4.5V on the rising transition.

Data Retention Timing Diagram

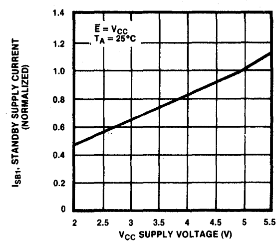


Typical Characteristics Curves

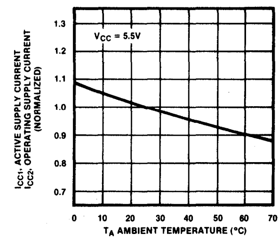
Standby Supply Current vs. Ambient Temp



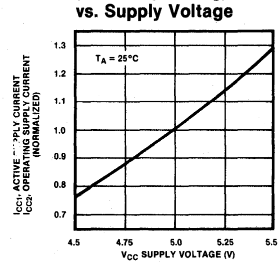
Standby Supply Current vs. Supply Voltage



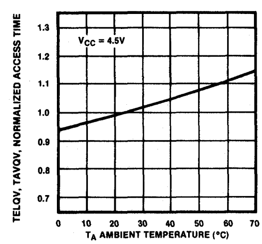
Supply Current (Active/Operating) vs. Ambient Temp



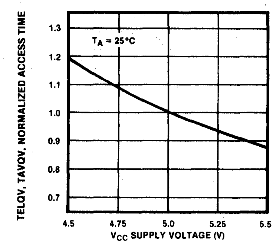
Supply Current (Active/Operating) vs. Supply Voltage



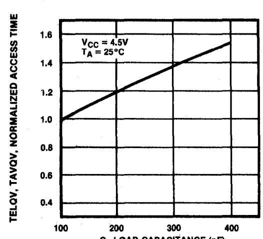
Access Times vs. Ambient Temp



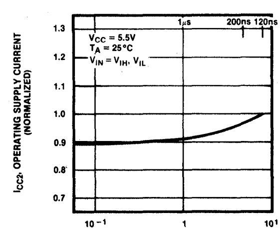
Access Times vs. Supply Voltage



Access Times vs. Load Capacitance



Supply Current vs. Frequency



MB8417-20
MB8417-20L

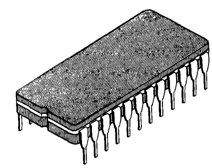
CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

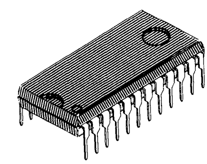
The Fujitsu MB8417 is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

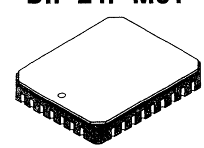
The MB8417 can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Chip Select $\overline{S}$ permits the fast access time. The MB8417 is packaged in an industry standard 24-pin dual in-line package or 32-pin leadless chip carrier.



CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24P-M01

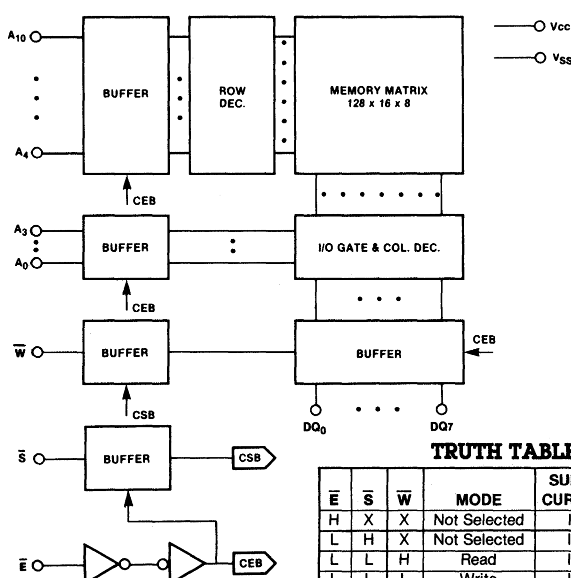


LEADLESS CHIP CARRIER
LCC-32C-A02

FEATURES

- Extended temperature range:
  MB8417-20: −40°C to +85°C
  MB8417-20L: −40°C to +70°C
- Organized as 2048 words by 8-bits
- Fast Access Time:
  200 ns Max. ($\overline{E}$ Controlled)
  100 ns Max. ($\overline{S}$ Controlled)
- Low Standby Power:
  MB8417-20: 55 μW
  MB8417-20L: 5.5 μW
- Completely Static Operation, no clocks required
- Single +5 Volt Power Supply
- TTL Compatible Inputs/Outputs
- Low Data Retention Voltage: 2.0V Min.
- Pin compatible with TC5516 and μPD447

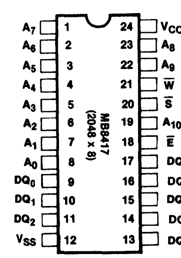
MB8417 BLOCK DIAGRAM

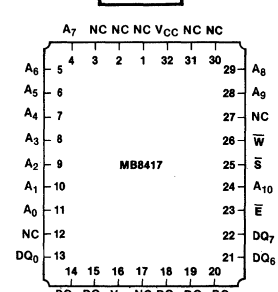


TRUTH TABLE

$\overline{E}$	$\overline{S}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
L	H	X	Not Selected	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Cerdip	T_{stg}	−65	150	°C
	Plastic		−40	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS, V_{SS} = GND

Parameter	Symbol		MB8417 Min	Typ	Max	Unit
Ambient Temperature	T_A	MB8417-20L	−40	—	+70	°C
		MB8417-20	−40	—	+85	
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		−0.3	—	0.8	V

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input / Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

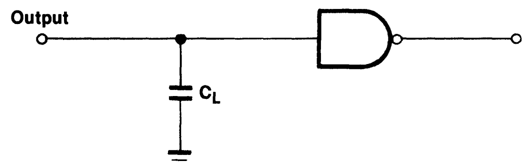
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol		Min	Max	Units
Standby Supply Current	$\overline{E} = V_{CC} - 0.2$ to $V_{CC} + 0.2V$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	MB8417-20L	—	1	μA
			MB8417-20	—	10	
Standby Supply Current	$\overline{E} = V_{IH}$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}		—	2	mA
Active Supply Current	$\overline{E} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}		—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}		—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}		−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{E} = V_{IH}$ or $\overline{S} = V_{IH}$	I_{LO}		−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}		2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}		—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and**
	C_L = 5 pF for TEHQZ, TGHQZ and TWLQZ
	C_L = 100 pF for all others.



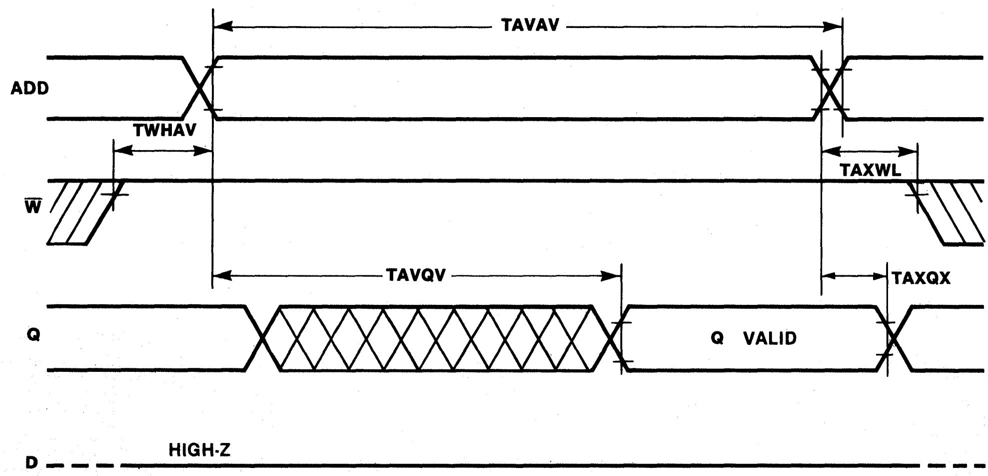
DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAV	200	—	ns
Write Cycle Time	TAVAV	200	—	ns
Address Access Time	TAVQV	—	200	ns
Chip Enable Access Time	TELQV	—	200	ns
Chip Select Access Time	TSLQV	—	100	ns
Output Hold from Address Change	TAXQX	15	—	ns
Output Low Z from $\overline{E}$ or $\overline{S}$	TELQX, TSLQX	15	—	ns
Output High Z from $\overline{E}$ or $\overline{S}$	TEHQZ, TSHQZ	—	60	ns
Output Low Z from $\overline{W}$	TWHQX	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	60	ns
Address Set Up Time	TAVWL, TAVSL, TAVEL	0	—	ns
Read Set Up Time	TWHAV, TWHEL, TWHSL	0	—	ns
Read Hold Time	TEHWL, TAXWL, TSHWL	0	—	ns
Write Set Up Time	TWLSL, TWLEL	0	—	ns
Write Hold Time	TSHWH, TEHWH	0	—	ns
Address Valid to End of Write	TAVSH, TAVWH	160	—	ns
Chip Enable to End of Write	TELEH	160	—	ns
Chip Selection to End of Write	TSLSH	100	—	ns
Write Pulse Width	TWLWH	140	—	ns
Write Recovery Time	TEHAX, TWHAX, TSHAX	10	—	ns
Data Set Up Time	TDVWH, TDVEH, TDVSH	60	—	ns
Data Hold Time	TEHDX, TWHDX, TSHDX	0	—	ns

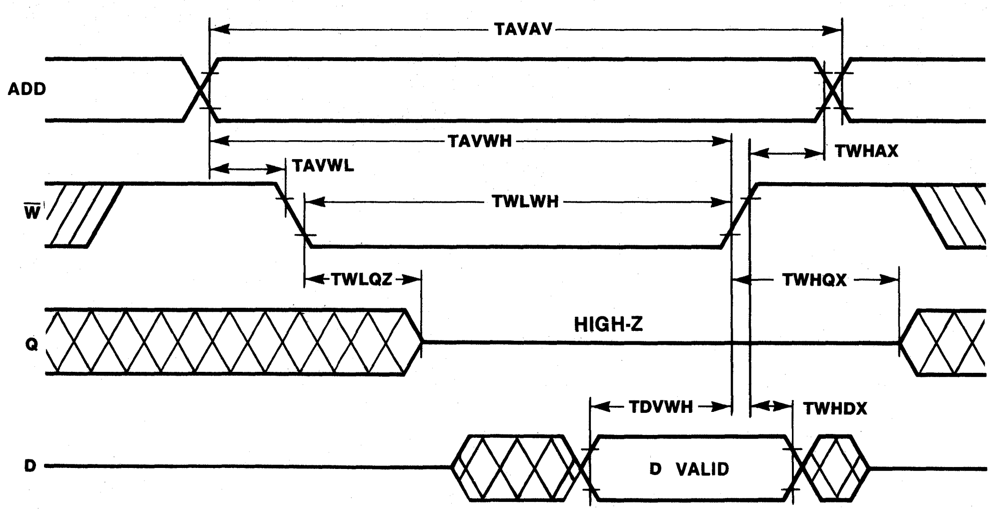
WAVEFORMS

MODE 1: $\overline{W}$ Controlled: ($\overline{E}$ = Low, $\overline{S}$ = Low)

Read Cycle



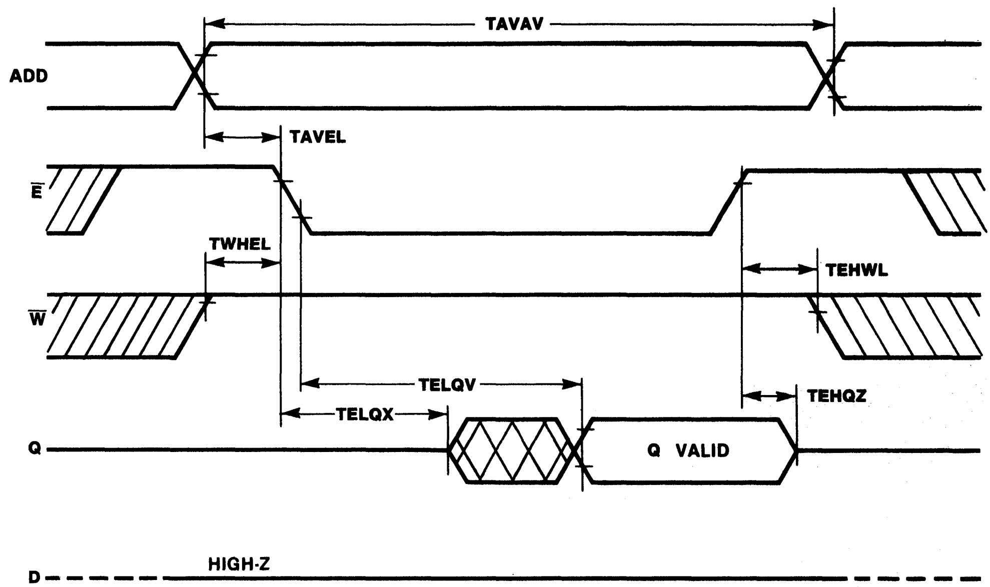
Write Cycle



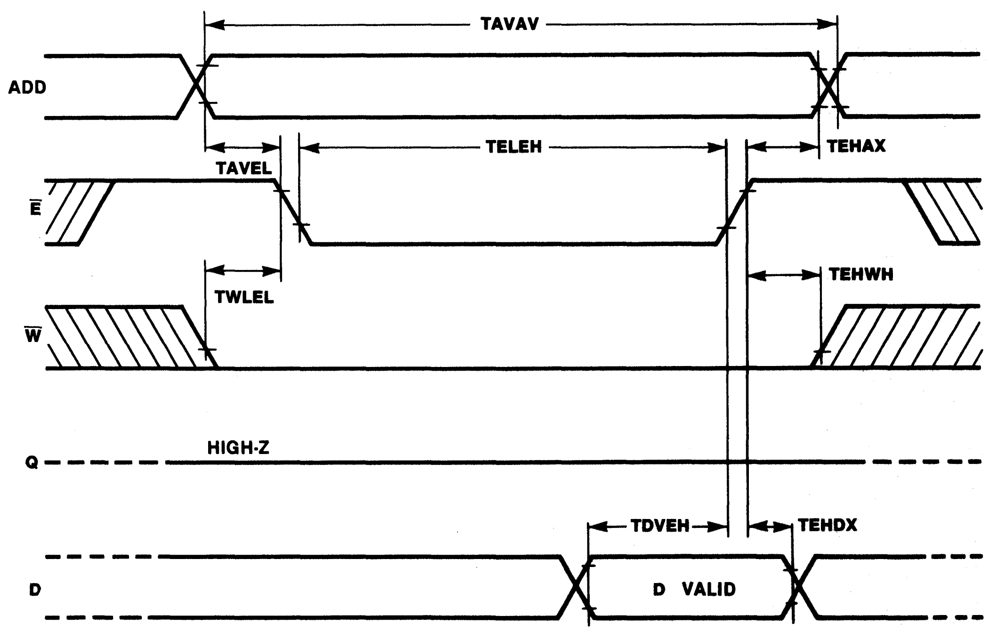
WAVEFORMS (Continued)

MODE 2: $\bar{E}$ Controlled, ($\bar{S}$ = Low)

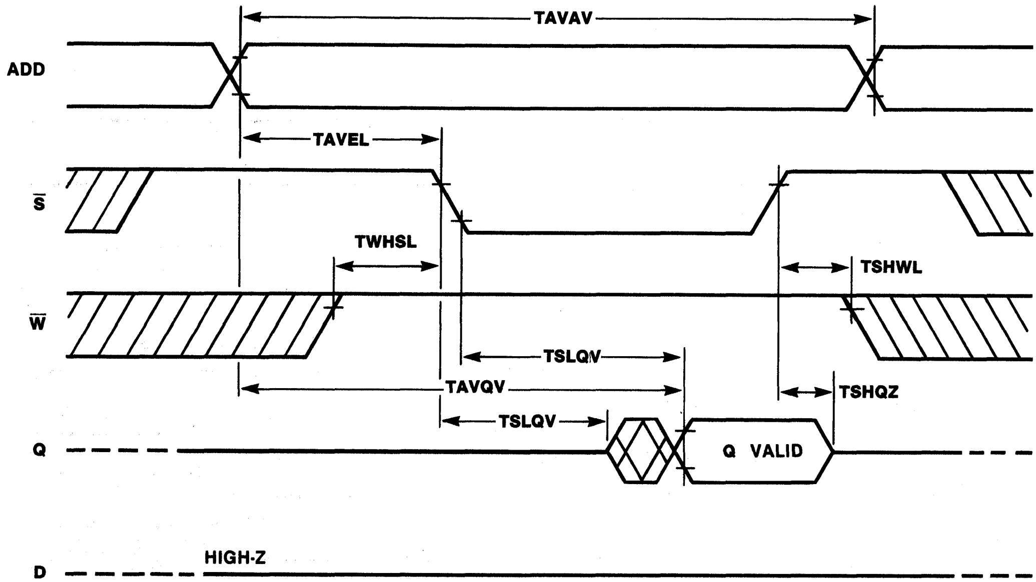
Read Cycle



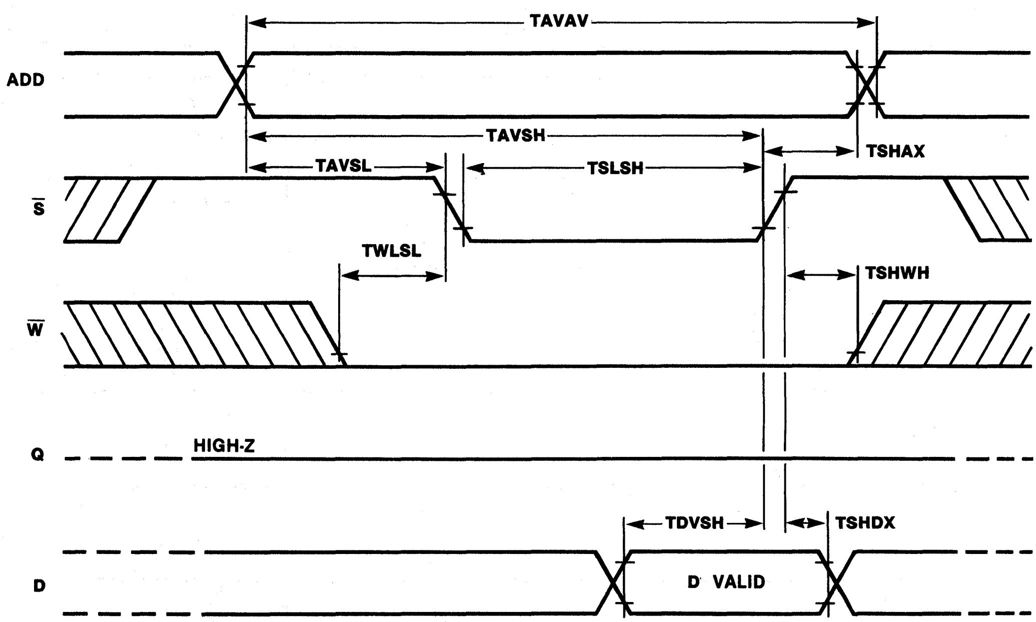
Write Cycle



WAVEFORMS (Continued)
MODE 3: $\bar{S}$ Controlled, ($\bar{E}$ = Low)
Read Cycle



Write Cycle



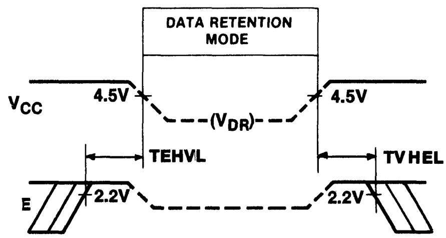
DYNAMIC CHARACTERISTICS

Data Retention Characteristics, NOTES [1],[2],[3] (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol		Min	Max	Unit
Data Retention Supply Voltage	[1]	VDR		2.0	5.5	V
Data Retention Supply Current	[2]	IDR	MB8417-20	—	10	μA
			MB8417-20L	—	1	μA
Data Retention Set Up Time	[3]	TEHVL		60	—	ns
Recovery Time	[3]	TVHEL		60	—	ns

NOTES:

1. $\bar{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V, $\bar{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
2. V_{CC} = VDR = 2.0V, $\bar{E}$ = VDR ± 0.2V V_{IN} = − 0.2V to VDR + 0.2V.
3. V_L = 4.5V on the falling transition, V_H = 4.5V on the rising transition.



MOS Memories

FUJITSU

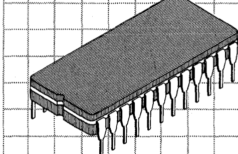
MB8417A-12, MB8417A-12L, MB8417A-15, MB8417A-15L

CMOS 16,384-Bit Static Random Access Memory

Description

The Fujitsu MB8417A is a 2048-word by 8-bit static random access memory fabricated with CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volt power supply is required.

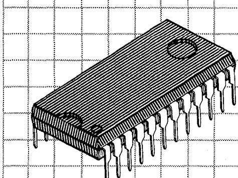
The MB8417A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.



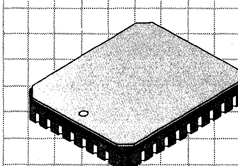
24-Lead Ceramic (Cerdip) DIP-24C-C03

Features

- **Organization: 2048 words x 8-bits**
- **Fast Access Time:**
  - **$\overline{E}$ Controlled:**
    - **120 ns max. (MB8417A-12/12L)**
    - **150 ns max. (MB8417A-15/15L)**
  - **$\overline{S}$ Controlled:**
    - **50 ns max. (MB8417A-12/12L)**
    - **60 ns max. (MB8417A-15/15L)**
- **Completely static operation: No clocks required**
- **TTL compatible inputs/outputs**
- **Three-state output**
- **Common data input/output**
- **Single +5V power supply**
- **Low power standby:**
  - **5.5 mW max. (MB8417A-12/15)**
  - **275μW max. (MB8417A-12L/15L)**
- **Data retention: 2.0V min.**
- **Jedec Standard 24-pin DIP (Ceramic Cerdip/Plastic Mold)**
- **Jedec Standard 32-pin leadless chip carrier**
- **Pin compatible with TC5516**

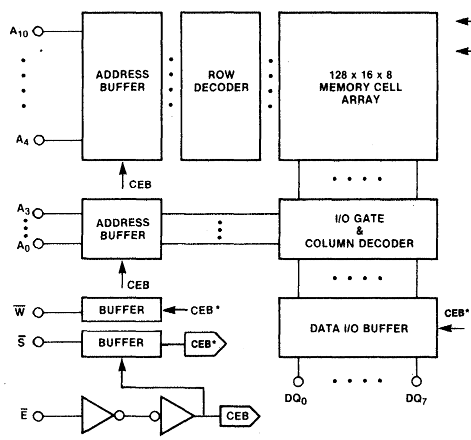


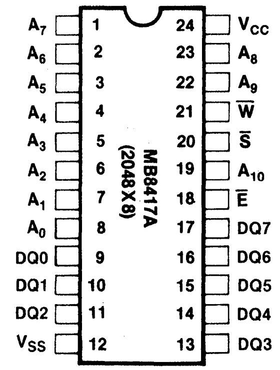
24-Lead Plastic DIP DIP-24P-M01



Leadless Chip Carrier LCC-32C-A02

MB8417A Block Diagram and Pin Assignment





Truth Table

$\overline{E}$	$\overline{S}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High-Z
L	H	X	Not Selected	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Storage Temperature	Cerdip	T_{stg}	−65 to +150	°C
	Plastic		−40 to +125	
Temperature Under Bias		T_{bias}	−10 to +85	°C
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC}+0.5	V
Output Voltage		$V_{I/O}$	−0.5 to V_{CC}+0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	—	—	10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	—	7	pF

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Ambient Temperature	T_A	0	—	70	°C

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	MB8417A-12/15 Min	MB8417A-12/15 Max	MB8417A-12L/15L Min	MB8417A-12L/15L Max	Unit
Standby Supply Current 1	$\overline{E} = V_{CC} - 0.2$ to $V_{CC} + 0.2V$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	—	1	—	0.05	mA
Standby Supply Current 2	$\overline{E} = V_{IH}$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}	—	2	—	1	mA
Active Supply Current	$\overline{E} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}	—	60	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}	—	60	—	60	mA
Input Leakage Current	$V_{IN} = 0V$ to V_{CC}	I_{LI}	−1.0	1.0	−1.0	1.0	μA
Output Leakage Current	$V_{I/O} = 0V$ to V_{CC} $\overline{E} = V_{IH}$ or $\overline{S} = V_{IH}$	I_{LO}	−1.0	1.0	−1.0	1.0	μA
Output High Voltage	$I_{OUT} = -1.0$ mA	V_{OH}	2.4	—	2.4	—	V
Output Low Voltage	$I_{OUT} = 4.0$ mA	V_{OL}	—	0.4	—	0.4	V

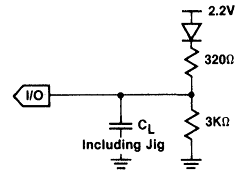
Note: All voltages are referenced to GND.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8417A-12/12L Min	MB8417A-12/12L Max	MB8417A-15/15L Min	MB8417A-15/15L Max	Unit
Read Cycle Time	TAVAV	120	—	150	—	ns
Write Cycle Time	TAVAV	120	—	150	—	ns
Address Access Time	TAVQV	—	120	—	150	ns
Chip Enable Access Time	TELQV	—	120	—	150	ns
Output Hold from Address Change	TAXQX	15	—	15	—	ns
Output Low Z from $\overline{E}$	TELQX	15	—	15	—	ns
Output High Z from $\overline{E}$	TEHQZ	—	40	—	50	ns
Output Low Z from $\overline{S}$	TSLQX	10	—	10	—	ns
Output High Z from $\overline{S}$	TSHQZ	—	40	—	50	ns
Output Low Z from $\overline{W}$	TNHQX	15	—	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	40	—	50	ns
Chip Select to Output Valid	TSLQV	—	50	—	60	ns
Address Set Up Time	TAVEL, TAVWL	0	—	0	—	ns
Address Set Up Time	TAVSL	20	—	20	—	ns
Read Set Up Time	TWHEL, TWHAV, TWHSL	0	—	0	—	ns
Read Hold Time	TAXWL, TEHWL, TSHWL	0	—	0	—	ns
Write Set Up Time	TWLEL, TWLSL	0	—	0	—	ns
Write Hold Time	TEHWH, TSHWH	0	—	0	—	ns
Address Valid to End of Write	TAVWH, TAVSH	100	—	120	—	ns
Chip Enabled to End of Write	TELEH	100	—	120	—	ns
Chip Selection to End of Write	TSLSH	50	—	60	—	ns
Write Pulse Width	TWLWH, TWLSH	70	—	90	—	ns
Write Recovery Time	TSHAX, TWHAX, TEHAX	5	—	5	—	ns
Data Set Up Time	TDVSH, TDVEH, TDVWH	35	—	40	—	ns
Data Hold Time	TSHDX, TWHDX, TEHDX	0	—	0	—	ns

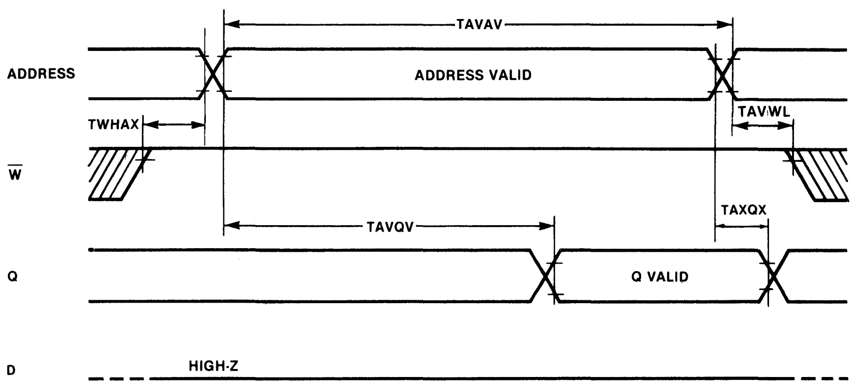
AC Test Conditions

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Times:	5ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$ Output: $V_{OL} = 0.8V$, $V_{OH} = 2.2V$
Output Load:	$C_L = 5_{PF}$ for TEHQZ, TSHQZ and TWLQZ $C_L = 100$ pF for all others.

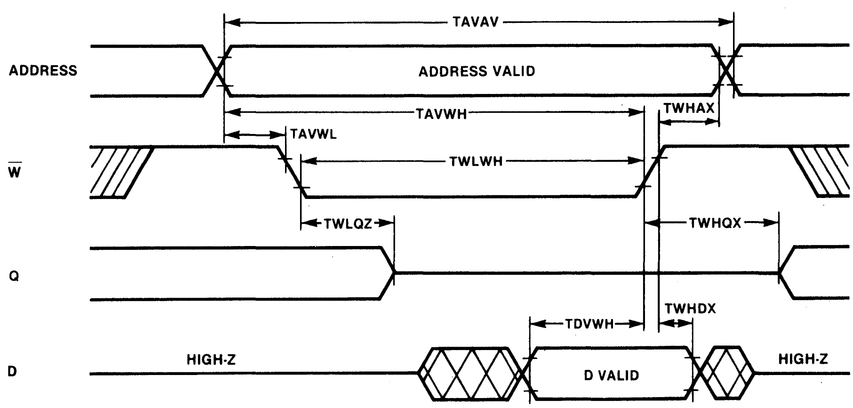


Mode 1 — $\overline{W}$ Controlled
($\overline{E}$ = Low, $\overline{S}$ = Low)

Read Cycle Timing Diagram

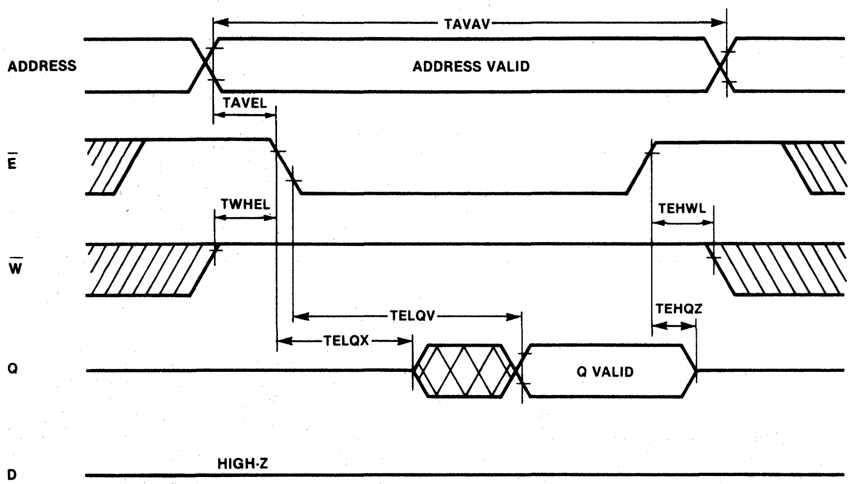


Write Cycle Timing Diagram

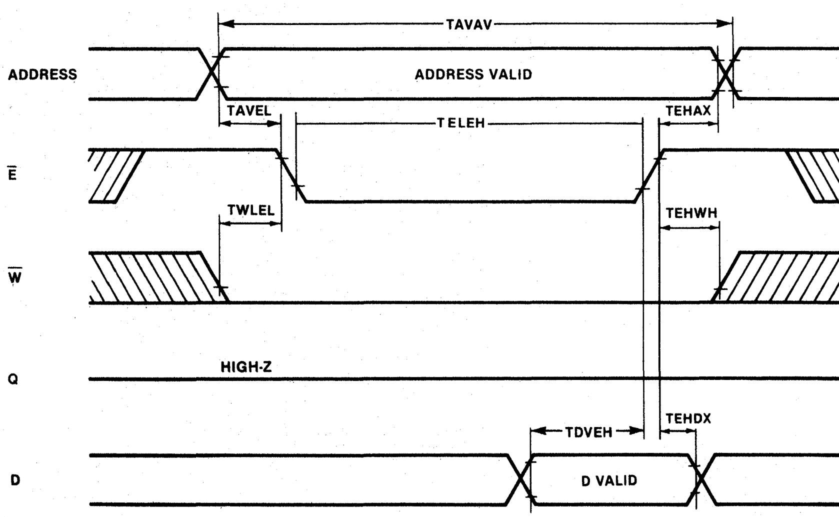


Mode 2 — $\overline{E}$ Controlled
($\overline{S}$ = Low)

Read Cycle Timing Diagram

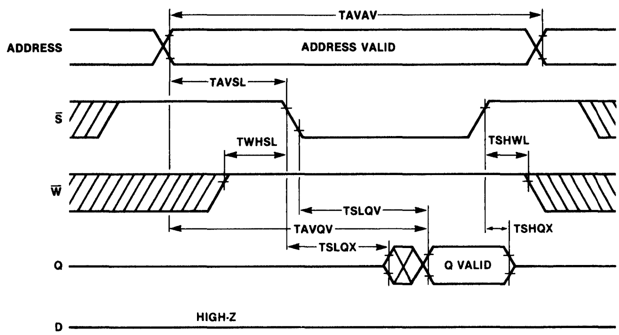


Write Cycle Timing Diagram

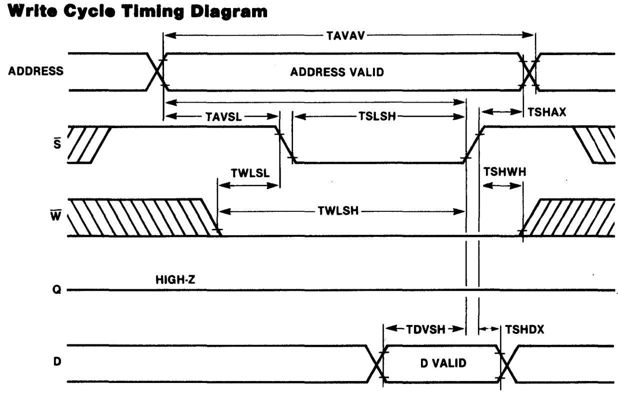


Mode 3 — $\overline{S}$ Controlled
($\overline{E}$ = Low, $\overline{W}$ = High, Address Valid)

Read Cycle Timing Diagram



Write Cycle Timing Diagram

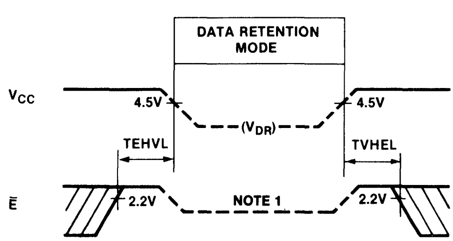


Data Retention Characteristics
(Recommended operating conditions unless otherwise noted.)

		MB8417A-12/15		MB8417A-12L/15L			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Condition**
Data Retention Supply Voltage	V_{DR}	2.0	5.5	2.0	5.5	V	Note 1
Data Retention Supply Current	I_{DR}	—	0.5	—	0.03	mA	Note 2
Data Retention Set Up Time	TEHVL	40	—	40	—	ns	Note 3
Recovery Time	TVHEL	40	—	40	—	ns	Note 3

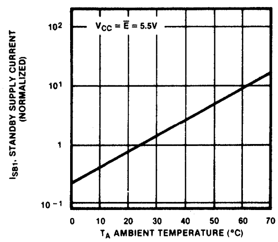
Note 1. $\overline{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V, $\overline{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
Note 2. $V_{CC} = V_{DR}$ = 3.0V, $\overline{E} = V_{DR}$ −0.2V to V_{DR} +0.2V, V_{IN} = −0.2V to V_{DR} +0.2V.
Note 3. V_L = 4.5V on the falling transition, V_H = 4.5V on the rising transition.

Data Retention Timing Diagram

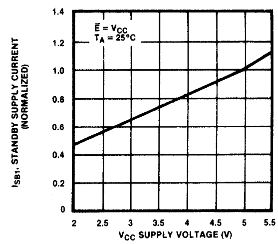


Typical Characteristics Curves

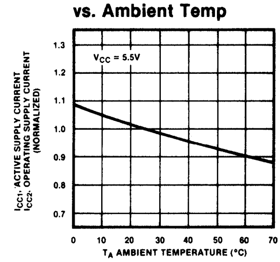
Standby Supply Current vs. Ambient Temp



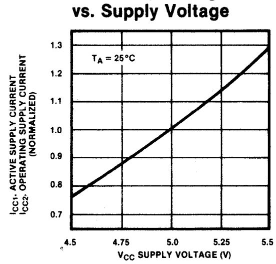
Standby Supply Current vs. Supply Voltage



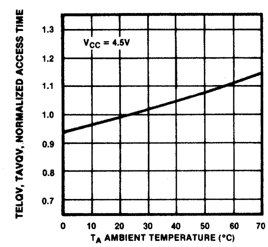
Supply Current (Active/Operating) vs. Ambient Temp



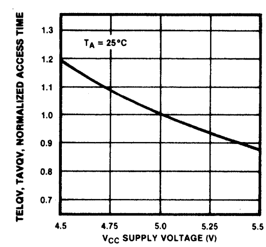
Supply Current (Active/Operating) vs. Supply Voltage



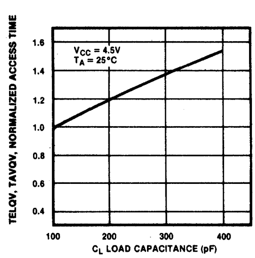
Access Time vs. Ambient Temp



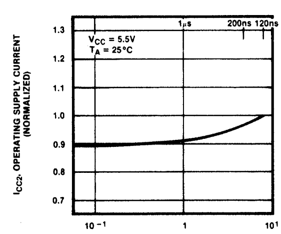
Access Time vs. Supply Voltage



Access Times vs. Load Capacitance



Supply Current vs. Frequency



MB8418-20
MB8418-20L

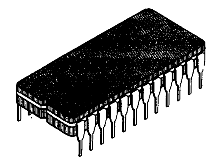
CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

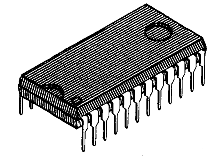
The Fujitsu MB8418 is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

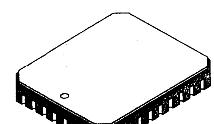
The MB8418 can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Two Chip Enables ($\overline{E}_2$ and $\overline{E}_1$) permit the selection of an individual device when the outputs are OR-tied. $\overline{E}_2$ controls minimum power consumption. The MB8418 is packaged in an industry standard 24-pin dual in-line package, or 32-pin leadless chip carrier.



CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
DIP-24P-M01

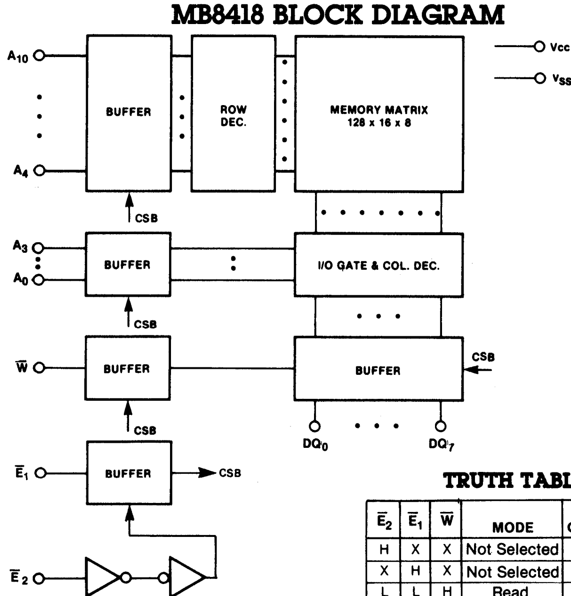


LEADLESS CHIP CARRIER
LCC-32-A02

FEATURES

- **Extended temperature range:**
  MB8418-20: −40°C to +85°C
  MB8418-20L: −40°C to +70°C
- **Organized as 2048 words by 8-bits**
- **Fast Access Time: 200 ns Max.**
- **Low Standby Power:**
  MB8418-20: 55μW
  MB8418-20L: 5.5μW
- **Completely Static Operation, no clocks required**
- **Single +5 Volt Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Low Data Retention Voltage: 2.0V Min.**
- **Pin compatible with HM6116, TC5517 and μPD446**

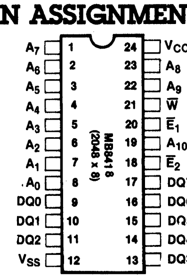
MB8418 BLOCK DIAGRAM

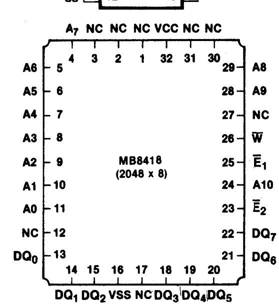


TRUTH TABLE

$\overline{E}_2$	$\overline{E}_1$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
X	H	X	Not Selected	I_{SB}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENTS





ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Cerdip	T_{stg}	−65	150	°C
	Plastic		−40	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS, (Referenced to V_{SS} = GND)

Parameter	Symbol		MB8418			Unit
			Min	Typ	Max	
Ambient Temperature	T_A	MB8418-20L	−40	—	+70	°C
		MB8418-20	−40	—	+85	
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		−0.3	—	0.8	V

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input / Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

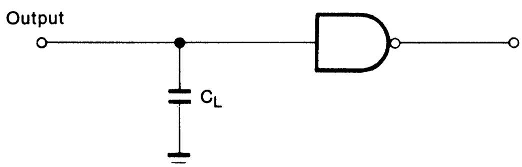
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol		Min	Max	Units
Standby Supply Current	$\overline{E}_2 = V_{CC} \pm 0.2$ OR $\overline{E}_1 = V_{CC} + 0.2V$ and $\overline{E}_2 = V_{SS} \pm 0.2V$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	MB8418-20L	—	1	μA
			MB8418-20	—	10	
Standby Supply Current	$\overline{E}_2$ or $\overline{E}_1 = V_{IH}$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}		—	2	mA
Active Supply Current	$\overline{E}_2 = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}		—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}		—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}		−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{E}_2 = V_{IH}$ or $\overline{E}_1 = V_{IH}$	I_{LO}		−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}		2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}		—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns (0.8V to 2.2 V)**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and**
	C_L = 5 pF for TEHQZ and TWHQZ
	C_L = 100 pF for all others.



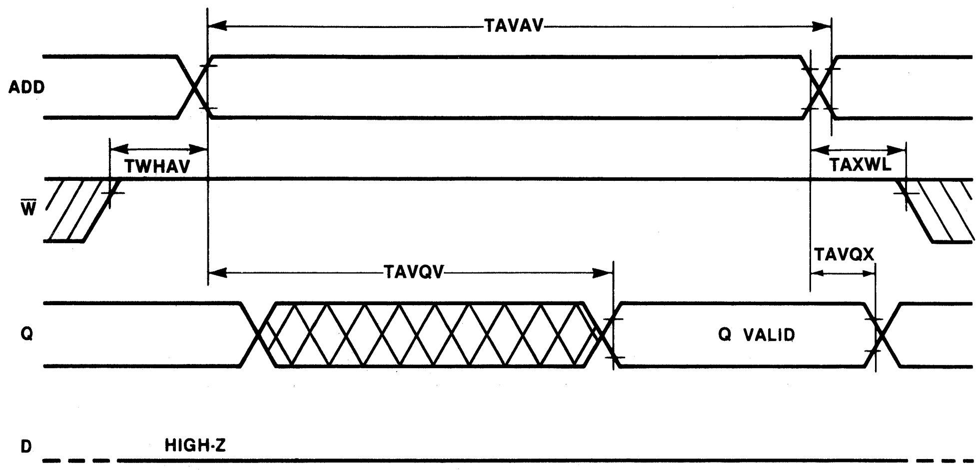
DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAV	200	—	ns
Write Cycle Time	TAVAV	200	—	ns
Address Access Time	TAVQV	—	200	ns
Chip Enable Access Time	TELQV	—	200	ns
Output Hold from Address Change	TAVQX	15	—	ns
Output Low Z from $\overline{E}_2$ or $\overline{E}_1$	TELQX	15	—	ns
Output High Z from $\overline{E}_2$ or $\overline{E}_1$	TEHQZ	—	60	ns
Output Low Z from $\overline{W}$	TWHQV	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	60	ns
Address Set Up Time	TAVEL, TAVWL	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	ns
Write Set Up Time	TWLEL	0	—	ns
Write Hold Time	TEHWH	0	—	ns
Address Valid to End of Write	TAVWH	160	—	ns
Chip Enable to End of Write	TELEH	160	—	ns
Write Pulse Width	TWLWH	140	—	ns
Write Recovery Time	TWHAX, TEHAX	10	—	ns
Data Set Up Time	TDVEH, TDVWH	60	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	ns

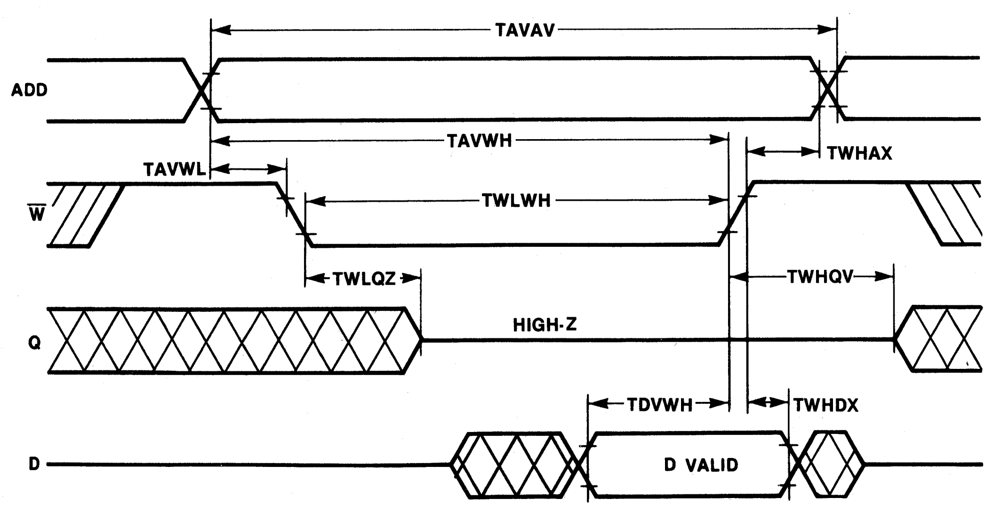
WAVEFORMS

MODE 1: W Controlled: ($\overline{E}_2 = \overline{E}_1 = LOW$)

Read Cycle



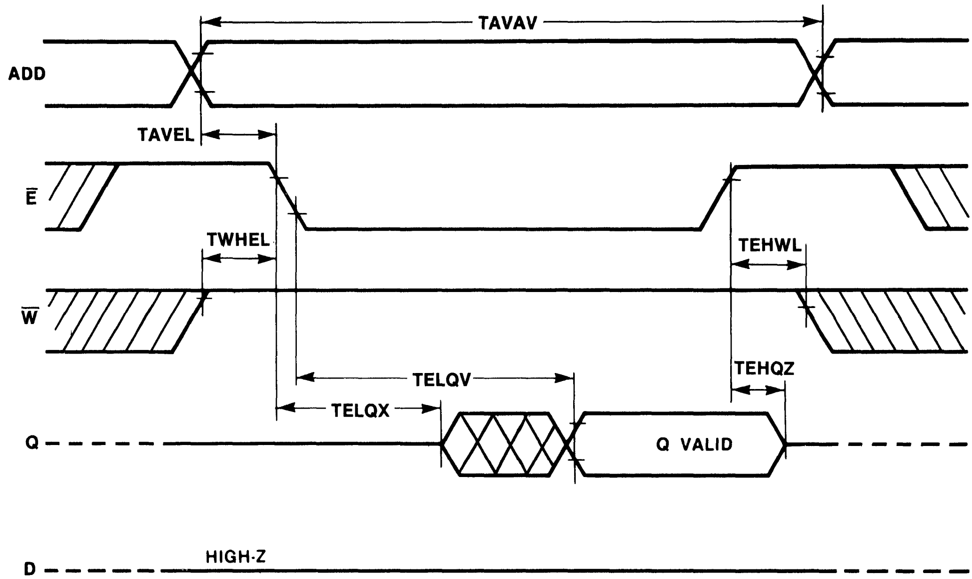
Write Cycle



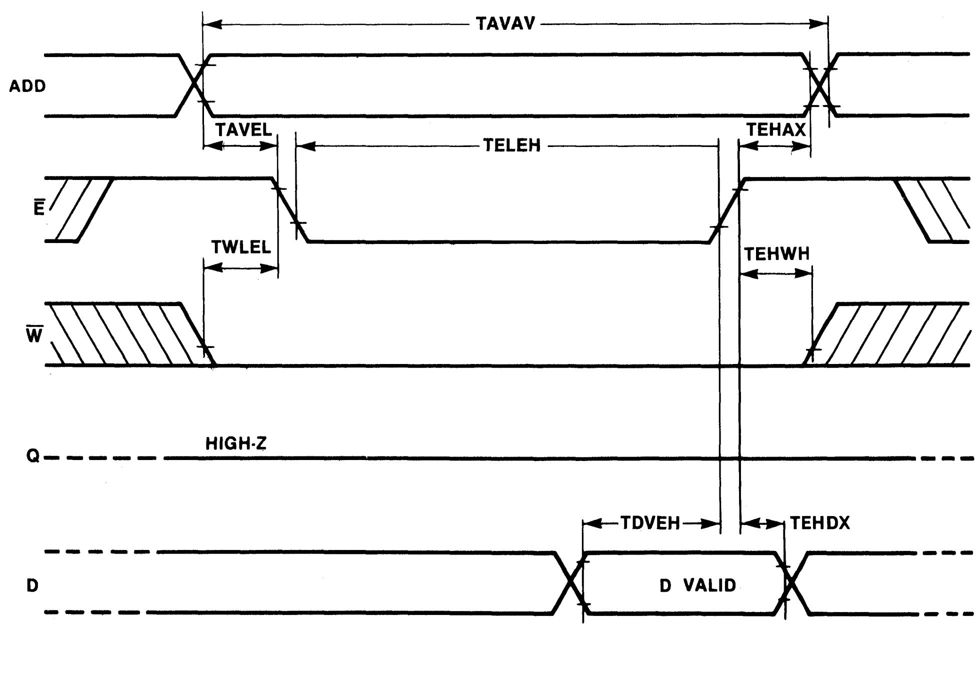
WAVEFORMS (Continued)

MODE 2: $\overline{E}_2$ or $\overline{E}_1$ Controlled ($\overline{E}_2$ = Low or $\overline{E}_1$ = Low)

Read Cycle



Write Cycle



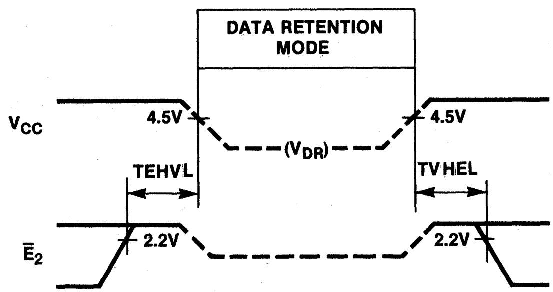
DYNAMIC CHARACTERISTICS

Data Retention Characteristics, NOTES 1, 2, 3 (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol		Min	Max	Unit
Data Retention Supply Voltage	1	VDR		2.0	5.5	V
Data Retention Supply Current	2	IDR	MB8418-20	—	10	μA
			MB8418-20L	—	1	μA
Data Retention Set Up Time	3	TEHVCL		60	—	ns
Recovery Time	3	TVHEL		60	—	ns

Notes:

1. $\overline{E}_2 = 2.2V$ to $V_{CC} \pm 0.3V$ for $VDR = 2.5V$ to $5.5V$
   $\overline{E}_2 = V_{CC} \pm 0.3V$ for $VDR = 2.0$ to $2.5V$.
2. $V_{CC} = V_{DR}$, $\overline{E}_2 = V_{DR} - 0.2V$ to $V_{DR} + 0.2V$, $V_{IN} = -0.2V$ to $V_{DR} + 0.2V$.
3. $V_L = 4.5V$ on the falling transition, $V_H = 4.5V$ on the rising transition.



MOS Memories

FUJITSU

■ MB8418A-12, MB8418A-12L, MB8418A-15, MB8418A-15L

CMOS 16,384-Bit Static Random Access Memory

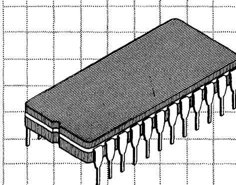
Description

The Fujitsu MB8418A is a 2048-word by 8-bit static random access memory fabricated with CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volt power supply is required.

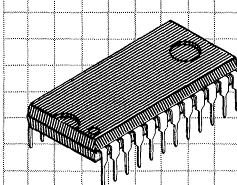
The MB8418A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

Features

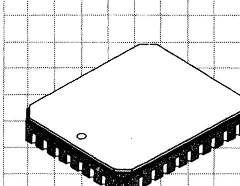
- **Organization: 2048 words x 8-bits**
- **Fast Access Time:**
  120 ns max. (MB8418A-12/12L)
  150 ns max. (MB8418A-15/15L)
- **Completely static operation: No clocks required**
- **TTL compatible inputs/outputs**
- **Three-state output**
- **Common data input/output**
- **Single +5V power supply**
- **Low power standby:**
  5.5 mW max. (MB8418A-12/15)
  275mW max. (MB8418A-12L/15L)
- **Data retention: 2.0V min.**
- **Standard 24-pin DIP (Ceramic Cerdip/Plastic Mold)**
- **Standard 32-pin leadless chip carrier.**
- **Dual chip enable inputs for battery back-up use.**



Ceramic Package (Cerdip)
DIP-24C-C03

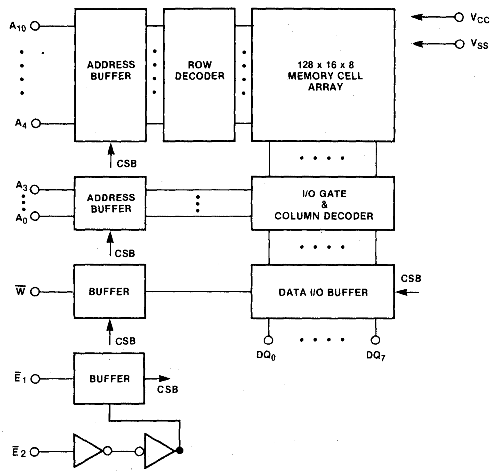


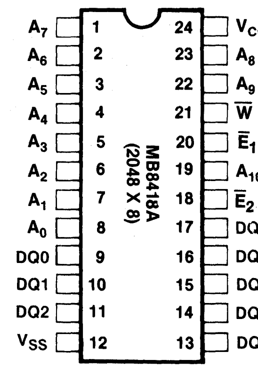
Plastic Package
DIP-24P-M01



Leadless Chip Carrier
LCC-32C-A02

MB8418A Block Diagram and Pin Assignment





Truth Table

$\overline{E}_2$	$\overline{E}_1$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High-Z
X	H	X	Not Selected	I_{SB}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

Absolute Maximum Ratings
(See Note)

Parameter		Symbol	Value	Unit
Storage Temperature	Cerdip Plastic	T_{stg}	−65 to +150 −40 to +125	°C
Temperature Under Bias		T_{bias}	−10 to +85	°C
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC}+0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5 to V_{CC}+0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance
($f = 1$ MHz, $T_A = 25\,°C$)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	—	—	10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	—	7	pF

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Ambient Temperature	T_A	0	—	70	°C

DC Characteristics

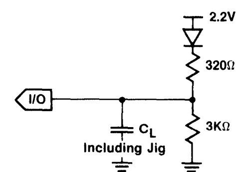
(Recommended operating conditions unless otherwise noted.)

			MB8418A-12/15		MB8418A-12L/15L		
Parameter	**Condition**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Standby Supply Current 1	$\overline{E}_2 = V_{CC} \pm 0.2$ OR $\overline{E}_1 = V_{CC} + 0.2V$ and $\overline{E}_2 = V_{SS} \pm 0.2V$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	—	1	—	0.05	mA
Standby Supply Current 2	$\overline{E}_2$ or $\overline{E}_1 = V_{IH}$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}	—	2	—	1	mA
Active Supply Current	$\overline{E}_1 = \overline{E}_2 = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}	—	60	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}	—	60	—	60	mA
Input Leakage Current	$V_{IN} = 0V$ to V_{CC}	I_{LI}	−1.0	1.0	−1.0	1.0	μA
Output Leakage Current	$V_{I/O} = 0V$ to V_{CC} $\overline{E}_2 = V_{IH}$ or $\overline{E}_1 = V_{IH}$	I_{LO}	−1.0	1.0	−1.0	1.0	μA
Output High Voltage	$I_{OUT} = -1.0$ mA	V_{OH}	2.4	—	2.4	—	V
Output Low Voltage	$I_{OUT} = 4.0$ mA	V_{OL}	—	0.4	—	0.4	V

Note: All voltages are referenced to GND.

AC Test Conditions

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Times:	5ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$ Output: $V_{OL} = 0.8V$, $V_{OH} = 2.2V$
Output Load:	$C_L = 5_{PF}$ for TEHQZ and TWHQZ $C_L = 100$ pF for all others.



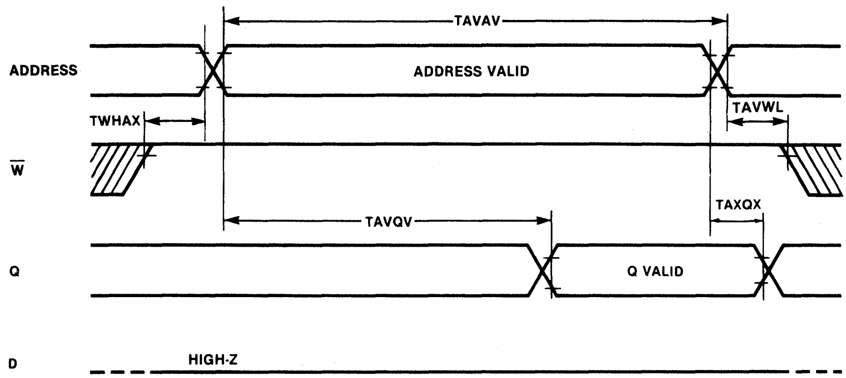
AC Characteristics

(Recommended operating conditions unless otherwise noted.)

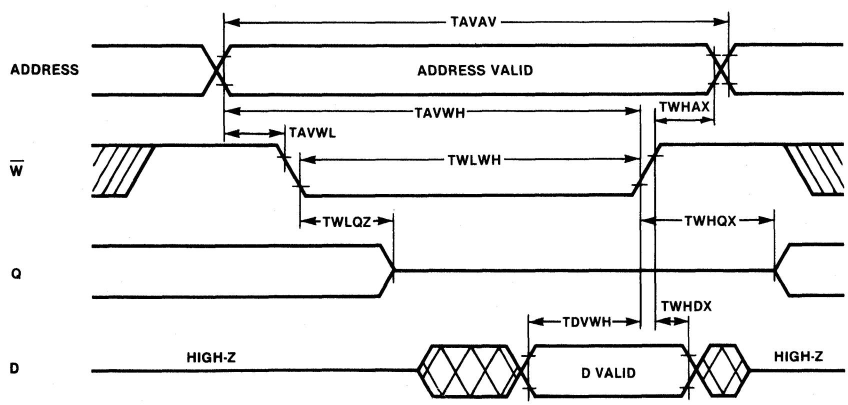
		MB8418A-12/12L		MB8418A-15/15L		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read Cycle Time	TAVAV	120	—	150	—	ns
Write Cycle Time	TAVAV	120	—	150	—	ns
Address Access Time	TAVQV	—	120	—	150	ns
Chip Enable Access Time	TELQV	—	120	—	150	ns
Output Hold from Address Change	TAXQX	15	—	15	—	ns
Output Low Z from $\overline{E}_2$ or $\overline{E}_1$	TELQX	15	—	15	—	ns
Output High Z from $\overline{E}_2$ or $\overline{E}_1$	TEHQZ	—	40	—	50	ns
Output Low Z from $\overline{W}$	TWHQX	15	—	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	40	—	50	ns
Address Set Up Time	TAVEL, TAVWL	0	—	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	0	—	ns
Write Set Up Time	TWLEL	0	—	0	—	ns
Write Hold Time	TEHWH	0	—	0	—	ns
Address Valid to End of Write	TAVWH	100	—	120	—	ns
Chip Enabled to End of Write	TELEH	100	—	120	—	ns
Write Pulse Width	TWLWH	70	—	90	—	ns
Write Recovery Time	TWHAX, TEHAX	5	—	5	—	ns
Data Set Up Time	TDVEH, TDVWH	35	—	40	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	0	—	ns

Mode 1 — $\overline{W}$ Controlled
($\overline{E}$ = Low)

Read Cycle Timing Diagram

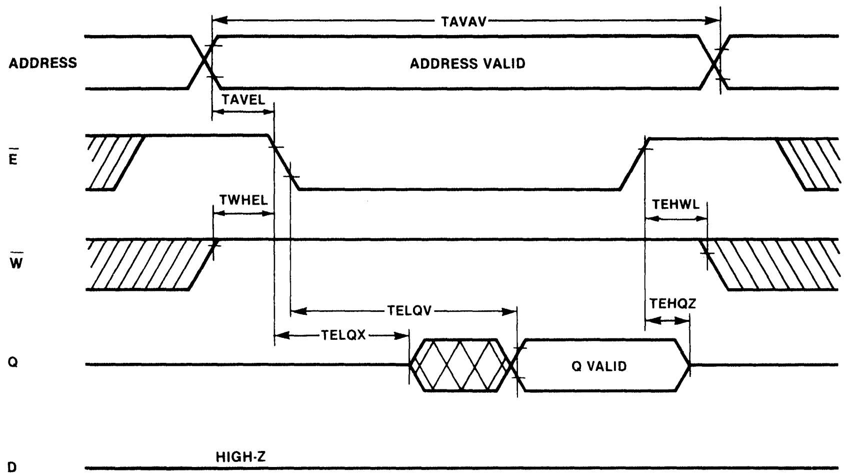


Write Cycle Timing Diagram

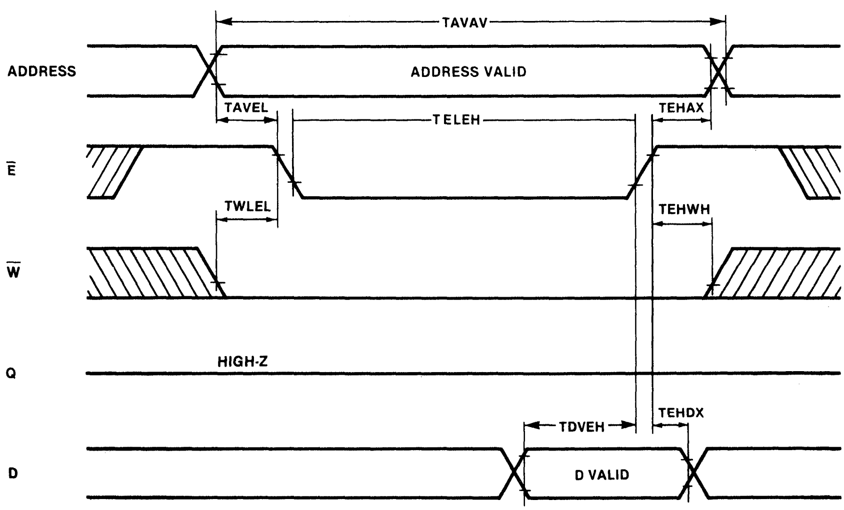


Mode 2 — $\overline{E}_2$ or $\overline{E}_1$ Controlled
($\overline{E}$ = Low)

Read Cycle Timing Diagram



Write Cycle Timing Diagram

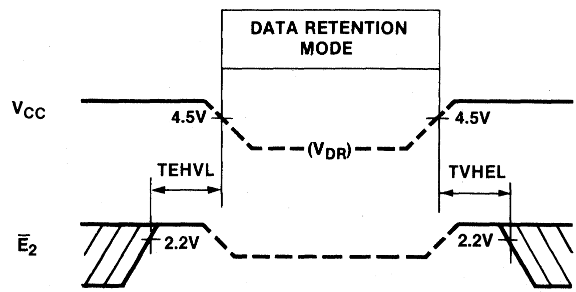


Data Retention Characteristics
(Recommended operating conditions unless otherwise noted.)

		MB8418A-12/15		MB8418A-12L/15L			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Condition**
Data Retention Supply Voltage	V_{DR}	2.0	5.5	2.0	5.5	V	Note 1
Data Retention Supply Current	I_{DR}	—	0.5	—	0.03	mA	Note 2
Data Retention Set Up Time	TEHVL	40	—	40	—	ns	Note 3
Recovery Time	TVHEL	40	—	40	—	ns	Note 3

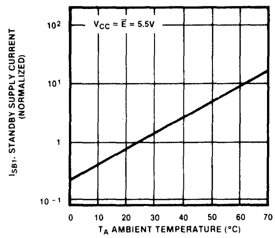
Note 1. $\bar{E}_2 = 2.2V$ to $V_{CC} + 0.3V$ for VDR = 2.5V to 5.5V
$\bar{E}_2 = V_{CC} \pm 0.3V$ for VDR = 2.0 to 2.5V.
Note 2. $V_{CC} = V_{DR} = 3.0V$, $\bar{E}_2 = V_{DR} - 0.2V$ to $V_{DR} + 0.2V$, $V_{IN} = -0.2V$ to $V_{DR} + 0.2V$.
Note 3. $V_L = 4.5V$ on the falling transition, $V_H = 4.5V$ on the rising transition.

Data Retention Timing Diagram

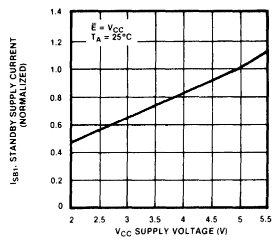


Typical Characteristics Curves

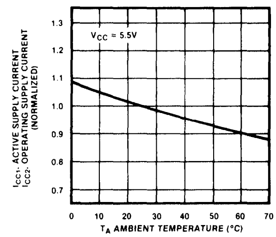
Standby Supply Current vs. Ambient Temp



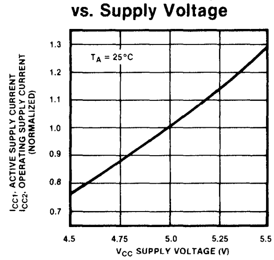
Standby Supply Current vs. Supply Voltage



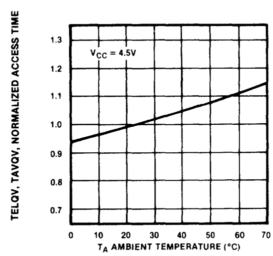
Supply Current (Active/Operating) vs. Ambient Temp



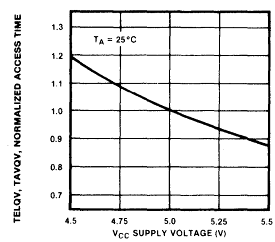
Supply Current (Active/Operating) vs. Supply Voltage



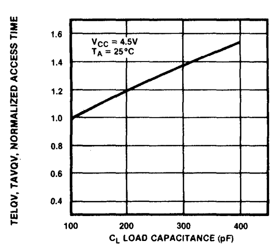
Access Time vs. Ambient Temp



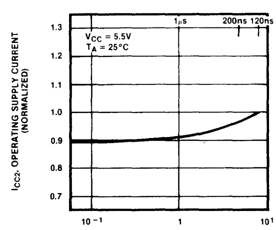
Access Time vs. Supply Voltage



Access Time vs. Load Capacitance



Supply Current vs. Frequency



FUJITSU
MICROELECTRONICS, INC.

MB8464
MB8464-L

PRELIMINARY

Note: This is not a final specification.
Some parametric limits are subject to change.

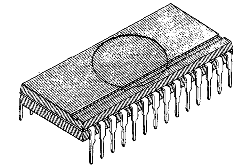
CMOS 65,536-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

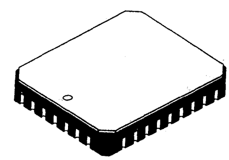
The Fujitsu MB8464 is a 8192 word by 8-bit static random access memory. This device is fabricated using a combination of Fujitsu's high-speed N-Channel MOS silicon-gate technology and the low power consumptive complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All inputs and output pins are TTL compatible, and a single +5V power supply is used. It is possible to retain data at low power supply voltage.

The MB8464 can be used for high performance applications such as microcomputer systems where fast access times and ease of use are required. Output Enable $\overline{G}$ input permits the disable of all outputs when outputs are OR-tied. The MB8464 is packaged in an industry standard 28-pin dual in-line package and is also available in a 32-pin leadless chip carrier.



PLASTIC PACKAGE
DIP-28P-M02

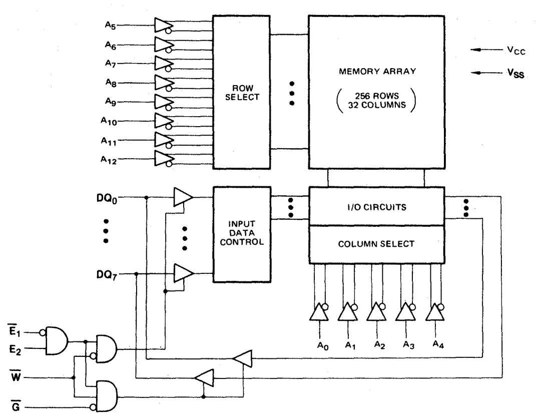


LEADLESS CHIP CARRIER
LCC-32C-A02

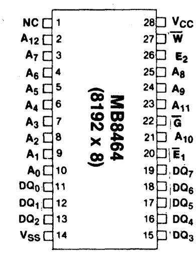
FEATURES

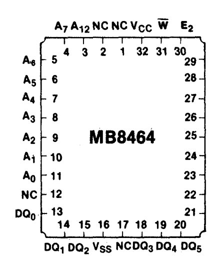
- **Organized as 8192 words by 8-bits**
- **Fast access times:**
  MB8464-12/-12L: 120 ns Max.
  MB8464-15/-15L: 150 ns Max.
- **Low Power Consumption:**
  MB8464-12/-15: 500 mW Max. (Active)
  MB8464-12L/-15L: 330 mW Max. (Active)
  MB8464-12/-15: 11 mW Max. (Standby)
  MB8464-12L/-15L: 0.55 mW Max. (Standby)
- **Completely static operation: no clock or refresh needed**
- **Single +5V supply voltage, ±10% tolerance**
- **Common data inputs and outputs**
- **TTL compatible inputs and outputs**
- **Low data retention voltage: 2.0V min.**
- **Standard 28-pin DIP and 32-pin leadless chip carrier**

MB8464 BLOCK DIAGRAM



PIN ASSIGNMENTS





TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	Not Selected	I_{SB}	High-Z
X	L	X	X	Not Selected	I_{SB}	High-Z
L	H	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	H	L	H	Read	I_{CC}	D_{OUT}
L	H	X	L	Write	I_{CC}	D_{IN}

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Storage Temperature	Cerdip	T_{stg}	−65 to +150	°C
	Plastic		−40 to +125	°C
Temperature Under Bias		T_{bias}	−10 to +85	°C
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC} + 0.5	V
Output Voltage		$V_{I/O}$	−0.5 to V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to 70°C
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}**	−0.3	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC})		I_{LI}	—	±10	μA
Output Leakage Current ($\overline{E}_1 = V_{IH}$ OR $E_2 = V_{IL}$ OR $\overline{G} = V_{IH}$ OR $\overline{W} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC})		I_{LO}	—	±10	μA
Standby Power Supply Current ($-0.2V \leq E_2 \leq 0.2V$ OR $V_{CC} - 0.2V \leq \overline{E}_1 \leq V_{CC} + 0.2V$ $V_{CC} - 0.2V \leq E_2 \leq V_{CC} + 0.2V$)	Standard	I_{SB1}	—	2	mA
	L-Version		—	0.1	mA
Standby Power Supply Current ($\overline{E}_1 = V_{IH}$ OR $E_2 = V_{IL}$)	Standard	I_{SB2}	—	5	mA
	L-Version		—	3	mA
Active Power Supply Current ($\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = 0$)	Standard	I_{CC1}	—	30	mA
	L-Version		—	25	mA
Active Power Supply Current (Cycle = Min., Duty = 100% $I_{OUT} = 0$)	Standard	I_{CC2}	—	90	mA
	L-Version		—	60	mA
Output High Voltage (I_{OH} = −1.0mA)		V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 2.1mA)		V_{OL}	—	0.4	V

**V_{IL}(min) = −0.3V for DC level, V_{IL}(min) = −3.0V, for ≤50 nsec pulse.

PRELIMINARY

Note: This is not a final specification. Some parametric limits are subject to change.

AC TEST CONDITIONS

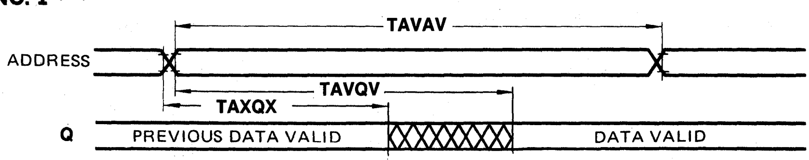
Input Pulse Levels:	**0.6V to 2.4 V**
Input Pulse Rise and Fall Times:	**5 ns**
Timing Reference Level:	**Input = 0.8 V, 2.2 V** **Output = 0.8V, 2.0 V**
Output Load:	**1 TTL gate + 5pF (including scope & jig) for TGHQZ, TWLQZ, TEHQZ, TWHQX, TGLQX and TEHQX** **1 TTL gate + 100pF for all others.**

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

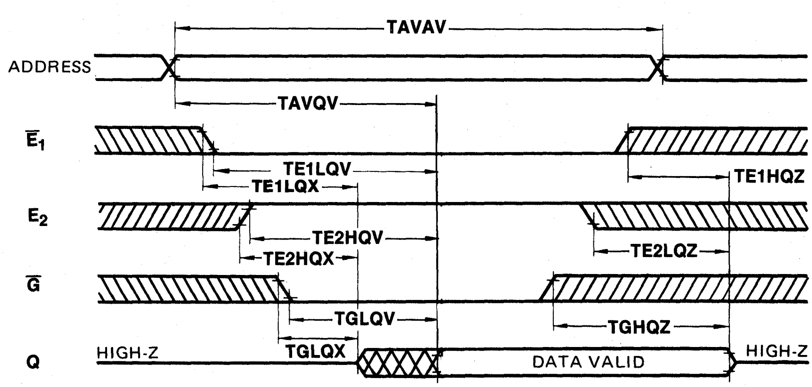
READ CYCLE

Parameter	Symbol	MB8464-12/12L Min	MB8464-12/12L Max	MB8464-15/15L Min	MB8464-15/15L Max	Unit
Read Cycle Time	TAVAV	120		150		ns
Address Access Time	TAVQV		120		150	ns
$\overline{E}_1$ Access Time	TE1LQV		120		150	ns
E_2 Access Time	TE2HQV		120		150	ns
Output Enable to Output Valid	TGLQV		50		60	ns
Output Hold from Address Change	TAXQX	10		10		ns
Chip Enable to Output Low-Z	TE1LQX, TE2HQX	10		10		ns
Output Enable to Output Low-Z	TGLQX	5		5		ns
Chip Enable to Output High-Z	TE1HQZ, TE2HQZ		40		50	ns
Output Enable to Output High-Z	TGHQZ		40		50	ns

READ CYCLE No. 1[1) 2)]



READ CYCLE No. 2[1)]



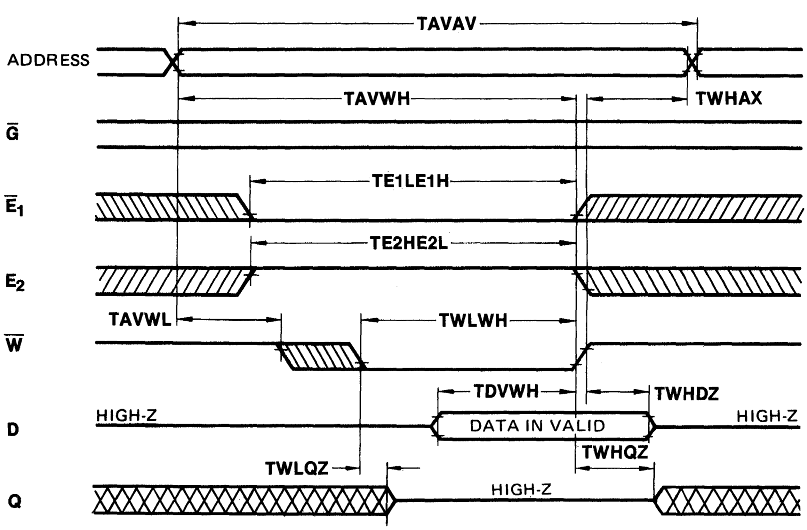
Note: 1) $\overline{W}$ is high for Read Cycle.
2) Device is continuosly selected, $\overline{E}_1 = \overline{G} = V_{IL}$, $E_2 = V_{IH}$.

WRITE CYCLE

Parameter	Symbol	MB8464-12/12L		MB8464-15/15L		Unit
		Min	Max	Min	Max	
Write Cycle Time	TAVAV	120		150		ns
Address Valid to End of Write	TAVWH, TAVE1H, TAVE2L	85	—	100	—	ns
Chip Enable to End of Write	TE1LE1H, TE2HE2L	85	—	100	—	ns
Data Valid to End of Write	TDVWH, TDVE1H, TDVE2L	40	—	50	—	ns
Data Hold Time	TWHDZ, TE1HDZ, TE2LDZ	0	—	0	—	ns
Write Pulse Width	TWLWH	70	—	90	—	ns
Address Setup Time	TAVWL, TAVE1L, TAVE2H	0	—	0	—	ns
Write Recovery Time	TWHAX, TE1HAX, TE2LAX	5	—	5	—	ns
Chip Enable to Output Low-Z	TE1LQX, TE2HQX	5	—	5	—	ns
Write Enable to Output Low-Z	TWHQX	5	—	5	—	ns
Write Enable to Output High-Z	TWLQZ	—	40	—	50	ns

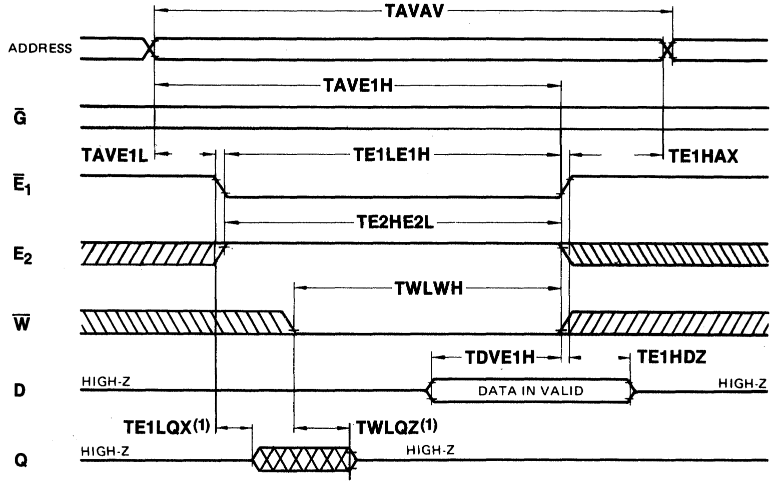
WRITE CYCLE TIMING DIAGRAMS

WRITE CYCLE NO. 1 ($\overline{W}$ Controlled)

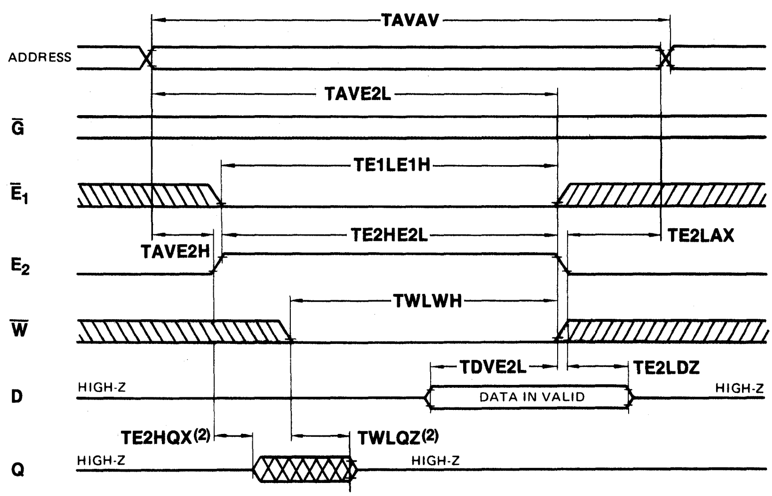


Note: 1) IF $\overline{G}$, $\overline{E}_1$, and E_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE NO. 2 ($\overline{E}_1$ Controlled)



WRITE CYCLE NO. 3 (E_2 Controlled)



Note: 1) If $\overline{G}$, E_2 and $\overline{W}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

2) If $\overline{G}$, $\overline{E}_1$ and $\overline{W}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

PRELIMINARY

Note: This is not a final specification.
Some parametric limits are subject to change.

DATA RETENTION CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Notes		Symbol	Min	Max	Unit
Data Retention Supply Voltage	1		VDR	2.0	5.5	V
Data Retention Supply Current	2	L-Version	IDR	—	0.1	mA
		Standard			50	μA
Data Retention Set Up Time	3		TE2LVL, TE1HVL	0		ns
Recovery Time	3		TVHE1L, TVHE2H	TAVAV		ns

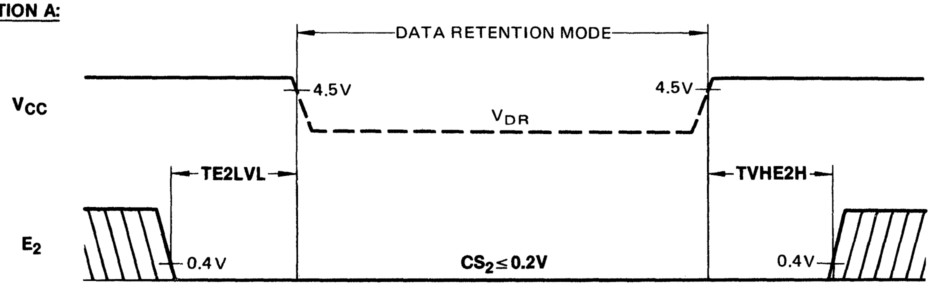
Note 1: E_2 controlled: $E_2 \leq 0.2V$
$\overline{E}_1$ controlled: $\overline{E}_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)

Note 2: E_2 controlled: $V_{DR} = 3.0V$, $E_2 \leq 0.2V$
$\overline{E}_1$ controlled: $V_{DR} = 3.0V$, $\overline{E}_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)

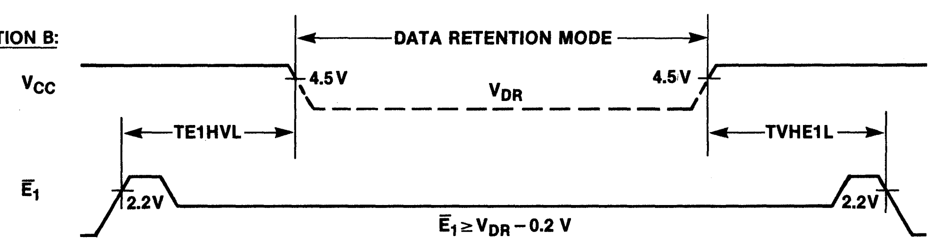
Note 3: $V_L = 4.5V$ on falling transition, $V_H = 4.5V$ on rising transition.

DATA RETENTION TIMING

CONDITION A:



OR
CONDITION B:

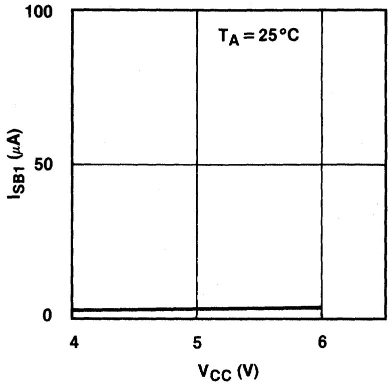


PRELIMINARY

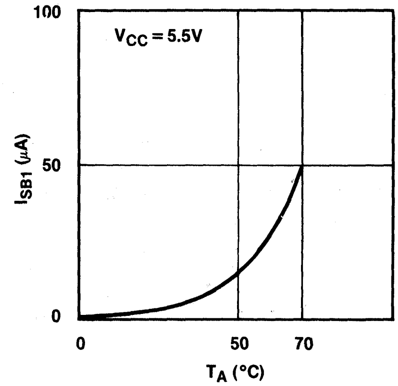
Note: This is not a final specification.
Some parametric limits are subject to change.

TYPICAL CHARACTERISTICS CURVES

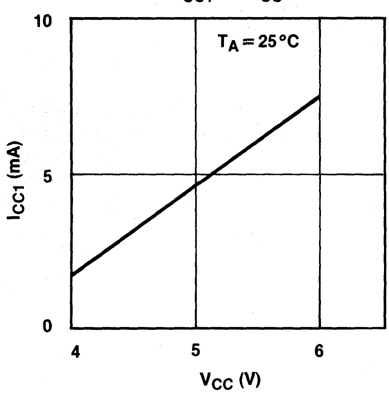
I_{SB1} vs. V_{CC}



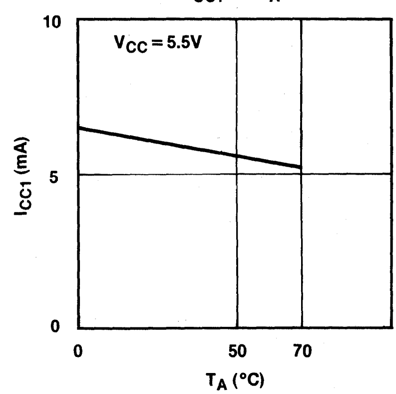
I_{SB1} vs. T_A



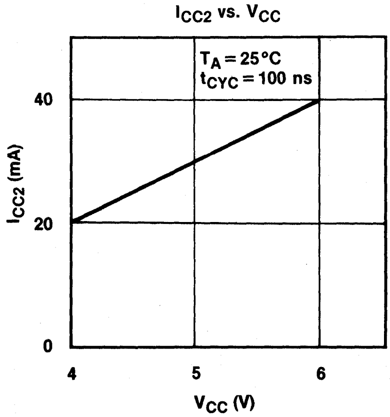
I_{CC1} vs. V_{CC}



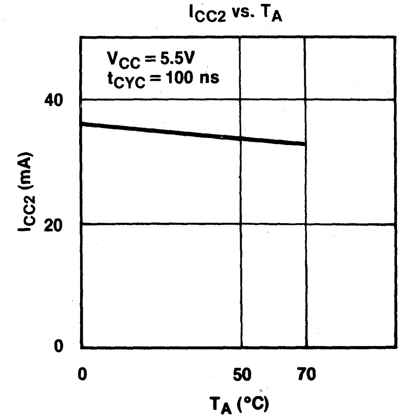
I_{CC1} vs. T_A



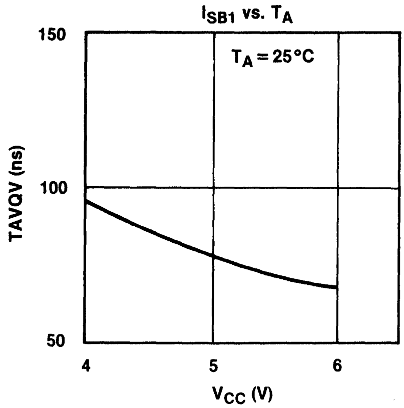
I_{CC2} vs. V_{CC}

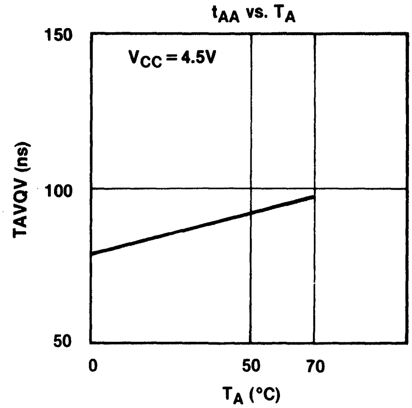


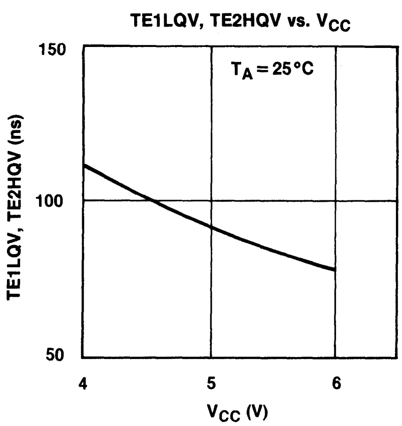
I_{CC2} vs. T_A

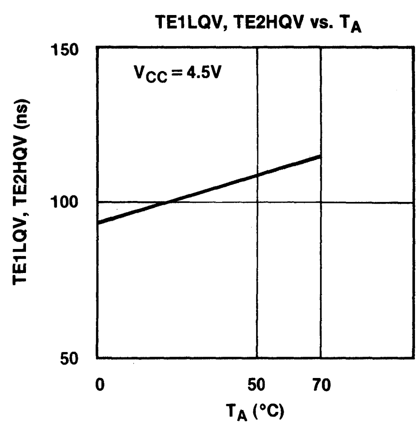


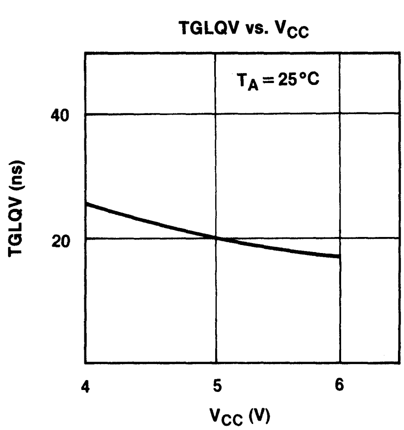
TYPICAL CHARACTERISTICS CURVES (Continued)

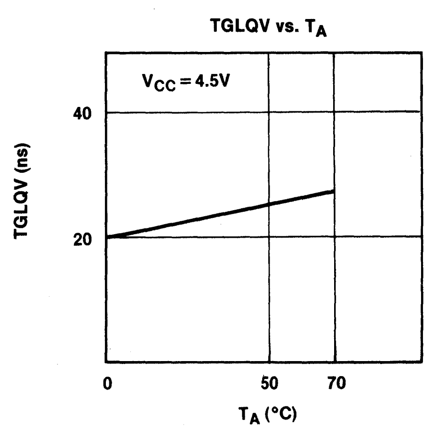












NMOS & CMOS EPROMs

Quick Guide To Products in This Section

Device	Technology	Organization	Access Time (max)	Power Supply Volts	Power Active	Dissipation Standby	Package	Page
MBM2764-20	NMOS	8K x 8	200 nS	+5	550 mW	143 mW	28-pin	4-2
MBM2764-25	NMOS	8K x 8	250 nS	+5	550 mW	193 mW	28-pin	4-2
MBM2764-30	NMOS	8K x 8	300 nS	+5	550 mW	193 mW	28-pin	4-2
MBM2764-30X	NMOS	8K x 8	300 nS	+5	550 mW	193 mW	28-pin	4-2
MBM27C64-25	CMOS	8K x 8	250 nS	+5	40 mW/MHz	550 μW	28-pin	4-9
MBM27C64-30	CMOS	8K x 8	300 nS	+5	40 mW/MHz	550 μW	28-pin	4-9
MBM27128-25	NMOS	16K x 8	250 nS	+5	550 mW	193 mW	28-pin	4-16
MBM27128-30	NMOS	16K x 8	300 nS	+5	550 mW	193 mW	28-pin	4-16
MBM27256-20	NMOS	32K x 8	200 nS	+5V	525 mW	210 mW	28-pin	4-22
MBM27256-25	NMOS	32K x 8	250 nS	+5V	525 mW	210 mW	28-pin	4-22
MBM27256-30	NMOS	32K x 8	300 nS	+5V	525 mW	210 mW	28-pin	4-22
MBM27C256-25	CMOS	32K x 8	250 nS	+5	40 mW/MHz	550 μW	28-pin	4-29
MBM27C256-35	CMOS	32K x 8	300 nS	+5	40 mW/MHz	550 μW	28-pin	4-29
MBM27C256-45	CMOS	32K x 8	450 nS	+5	40 mW/MHz	550 μW	28-pin	4-29

FUJITSU
MICROELECTRONICS, INC.

NMOS 65,536-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

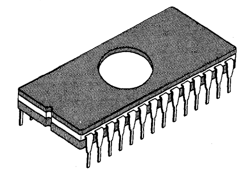
MBM2764-20
MBM2764-25
MBM2764-30
MBM2764-30-X

DESCRIPTION

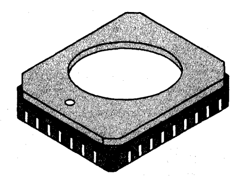
The Fujitsu MBM2764 is a high-speed 65,536-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin dual in-line package with a transparent lid is used to package the MBM2764. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM2764 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8,192 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



CERDIP PACKAGE
DIP-28C-C01

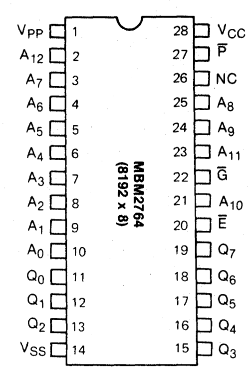


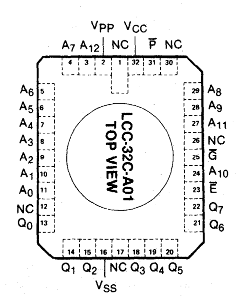
LCC Package
LCC-32C-A01

FEATURES

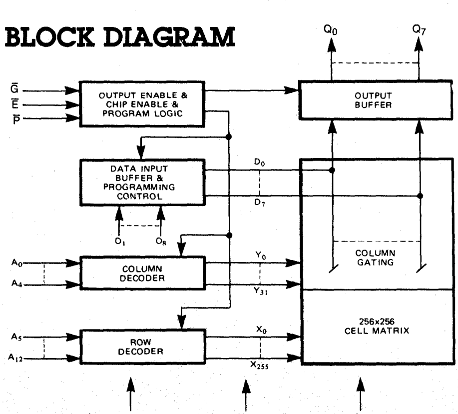
- **Organized as 8192 words by 8-bits, fully decoded**
- **Fast Access Time:**
  - **MBM2764-20 200 ns**
  - **MBM2764-25 250 ns**
  - **MBM2764-30 300 ns**
  - **MBM2764-30-X 300 ns**
- **Simple programming requirements**
- **Single location programming**
- **Programs with Quick Pro™ (see page 4-7)**
- **Low power requirement:**
  - **550mW active**
  - **193mW standby**
- **Extended temperature range: MBM2764-30-X: −40°C to +85°C**
- **No clocks required, Fully static operation**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable $\overline{G}$ pin for simplified memory expansion**
- **Single +5V Operation**
- **Standard 28-pin DIP package**
- **Pin compatible with Intel 2764**

PIN ASSIGNMENT





MBM2764 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Temperature Under Bias	MBM2764-20/-25/30	T_A	−25 to +85	°C
	MBM2764-30-X		−50 to +95	
Storage Temperature		T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to V_{SS}		V_{IN}, V_{OUT}	−0.6 to +7	V
V_{CC} with Respect to V_{SS}		V_{CC}	−0.6 to +7	V
V_{PP} with Respect to V_{SS}		V_{PP}	−0.6 to +22	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

FUNCTIONS AND PIN CONNECTIONS V_{CC} (28) = +5, V_{SS} (14) = GND

Function (DIP Pin No.) / Mode	Address Input (2 ~ 10,21,23 ~ 25)	Data Q (11 ~ 13,15 ~ 19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	I_{CC} Supply (28)	V_{PP} (1)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC2}	V_{CC}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	Don't Care	I_{CC2}	V_{CC}
				Don't Care	V_{IL}		
Stand By	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{CC1}	V_{CC}
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	I_{CC2}	V_{PP}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC2}	V_{PP}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{CC1}	V_{PP}

Note: 1. $\overline{P}$ works as if G (output enable) during reading operation.

CAPACITANCE

(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	4	6	pF
Ouput Capacitance (V_{OUT} = 0V)	C_{OUT}	8	12	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature	
						MBM2764-20/-25/-30	MBM2764-30-X
Supply Voltage	V_{CC}	4.50	5.0	5.50	V	0 °C to +70 °C	−40 °C to +85 °C
Supply Voltage	V_{PP}	V_{CC} − 0.6	—	V_{CC} + 0.6	V		
Supply Voltage	V_{SS}	—	GND	—	V		
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 1	V		
Input Low Voltage	V_{IL}	−0.1	—	0.8	V		

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Symbol	Min	Max	Unit
Input Load Current	$V_{IN} = 5.5V$	I_{LI}	—	10	μA
Output Leakage Current	$V_{OUT} = 5.5V$	I_{LO}	—	10	μA
V_{PP} Supply Current	$V_{PP} = V_{CC} \pm 0.6V$	I_{PP}	—	15	mA
V_{CC} Standby Current	$\overline{E} = V_{IH}$	I_{CC1}	—	35	mA
V_{CC} Supply Current (Active)	$\overline{E} = V_{IL}$	I_{CC2}	—	100	mA
Input Low Voltage	—	V_{IL}	−0.1	+0.8	V
Input High Voltage	—	V_{IH}	2.0	$V_{CC}+1$	V
Output Low Voltage	$I_{OL} = 2.1mA$	V_{OL}	—	0.45	V
Output High Voltage	$I_{OH} = -400\mu A$	V_{OH}	2.4	—	V

AC CHARACTERISTICS

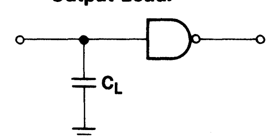
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM2764-20		MBM2764-25		MBM2764-30 MBM2764-30-X		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	TAVQV	—	200	—	250	—	300	ns	$\overline{E} = \overline{G} = V_{IL}$
$\overline{E}$ to Output Delay	TELQV	—	200	—	250	—	300	ns	$\overline{E} = V_{IL}$
$\overline{G}$ to Output Delay	TGLQV	10	70	10	100	10	120	ns	$\overline{E} = V_{IL}$
Output Enable High to Output Float	TGHQZ, TEHQZ	0	60	0	60	0	105	ns	$\overline{E} = V_{IL}$
Address to Output Hold	TAXQX	0	—	0	—	0	—	ns	$\overline{E} = \overline{G} = V_{IL}$

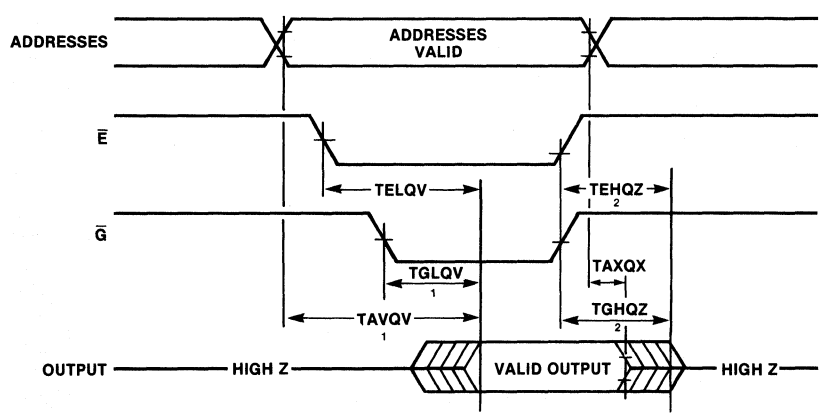
AC TEST CONDITIONS

Input Pulse levels: **0.8V to 2.2V**
Input Rise and Fall Time: **≤20nsec**
Timing Measurement Reference Levels: **1.0V and 2.0V for inputs**
0.8V and 2.0V for outputs
1 TTL gate and C_L = 100 pF

Output Load:

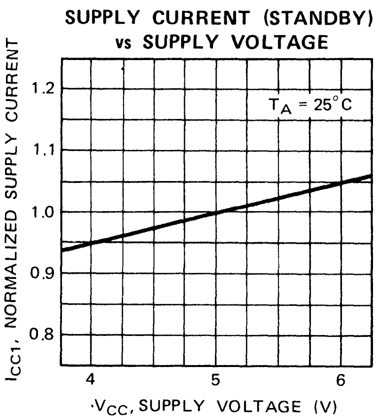


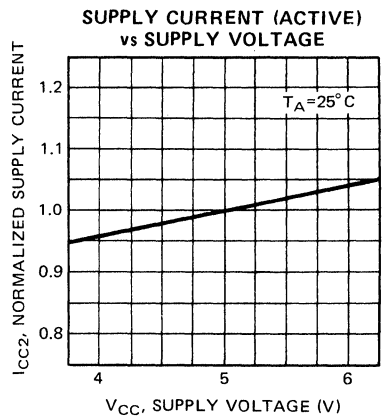
OPERATION TIMING DIAGRAM

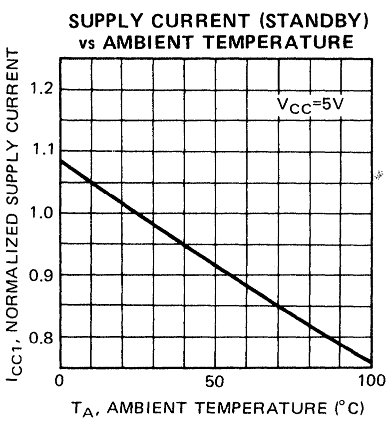


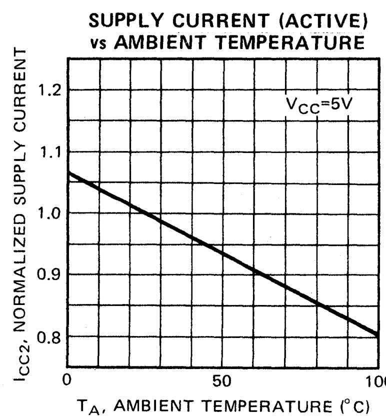
Notes: (1) $\overline{G}$ may be delay up to TAVQV—TGLQV after the falling edge of $\overline{E}$ without impact on TAVQV.
(2) TGHQZ or TEHQZ are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

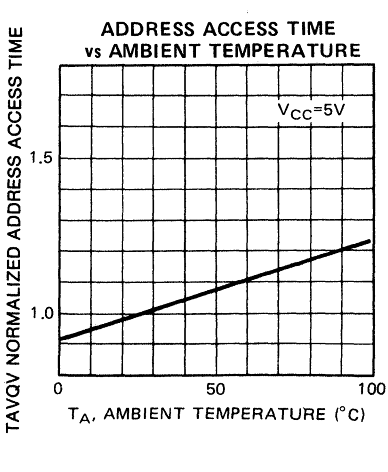
TYPICAL CHARACTERISTICS CURVES

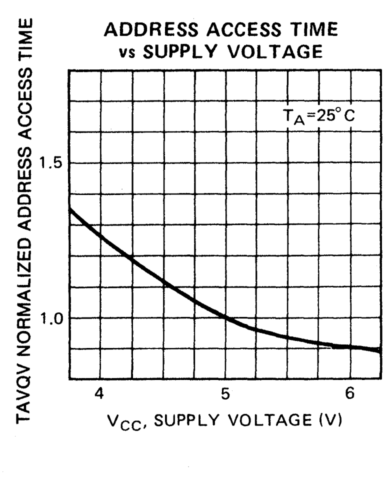




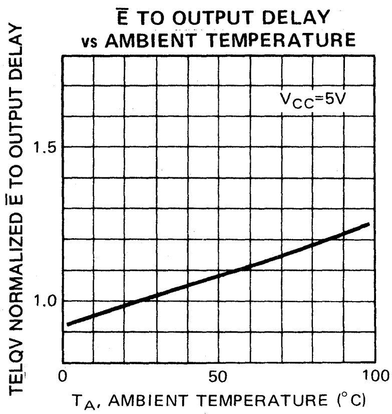


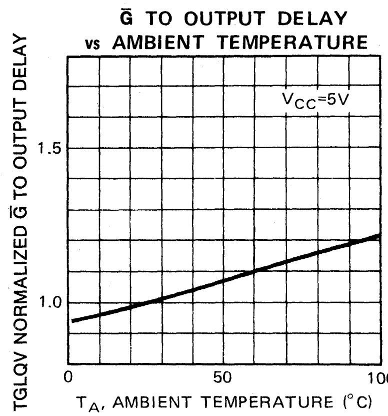


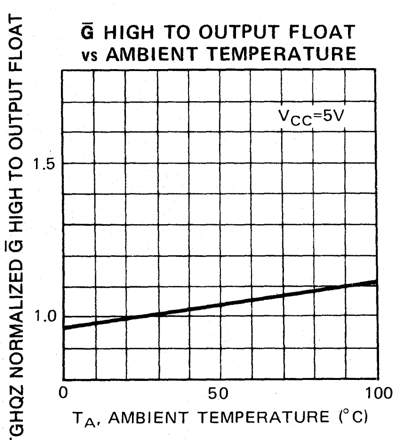


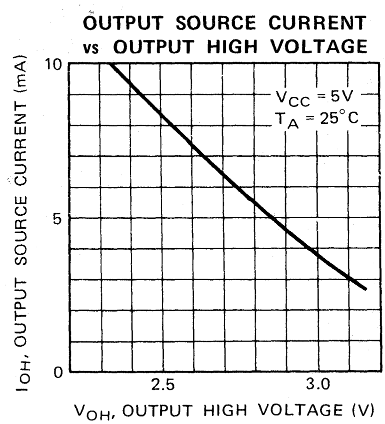


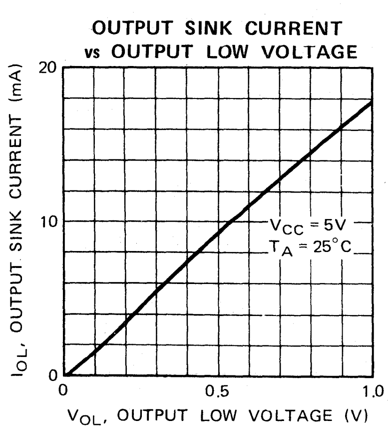
TYPICAL CHARACTERISTICS CURVES (Continued)

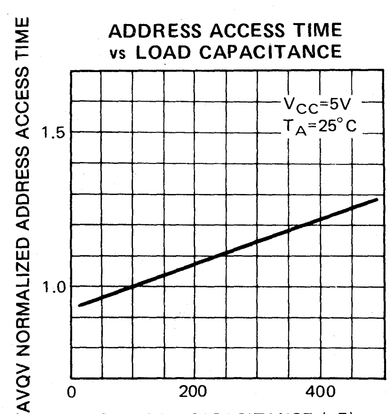












PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM2764 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Fig. 1 — MEMORY CELL

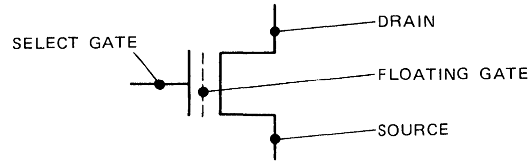
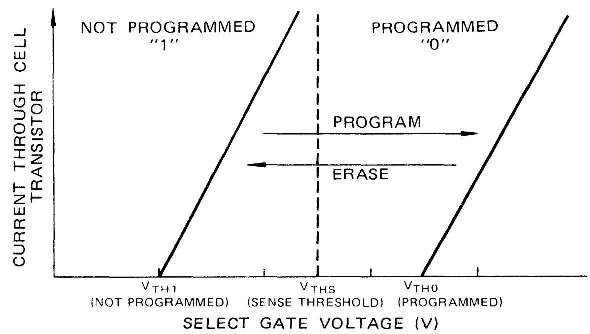


Fig. 2 — MEMORY CELL THRESHOLD SHIFT



CONVENTIONAL PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM2764 has all 65,536-bits in the "1" or high state. "0's" are loaded into the MBM2764 through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ and $\overline{P}$ are both at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1 μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the $\overline{P}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{P}$ input is prohibited when programming.

QUICK PRO™

In addition to the standard 50 millisecond pulse width programming procedure, the MBM2764 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulse to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the E input. Conversely, a TTL high input must be applied to the G input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the P pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach proper stored charge levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM2764 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM2764. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2 for 15 to 20 minutes.

The MBM2764 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM2764 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM2764 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING/ERASING INFORMATION (Continued)

DC CHARACTERISTICS

($T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	$V_{IN} = 0.45V–5.25V$
Output Low Voltage	V_{OL}	—	0.45	V	$I_{OL} = 2.1$ mA
Output High Voltage	V_{OH}	2.4	—	V	$I_{OH} = -400\mu A$
V_{CC} Supply Current	I_{CC}	—	100	mA	—
Input Low Voltage	V_{IL}	−0.1	0.8	V	—
Input High Voltage	V_{IH}	2.0	$V_{CC}+1$	V	—
V_{PP} Supply Current	I_{PP}	—	30	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

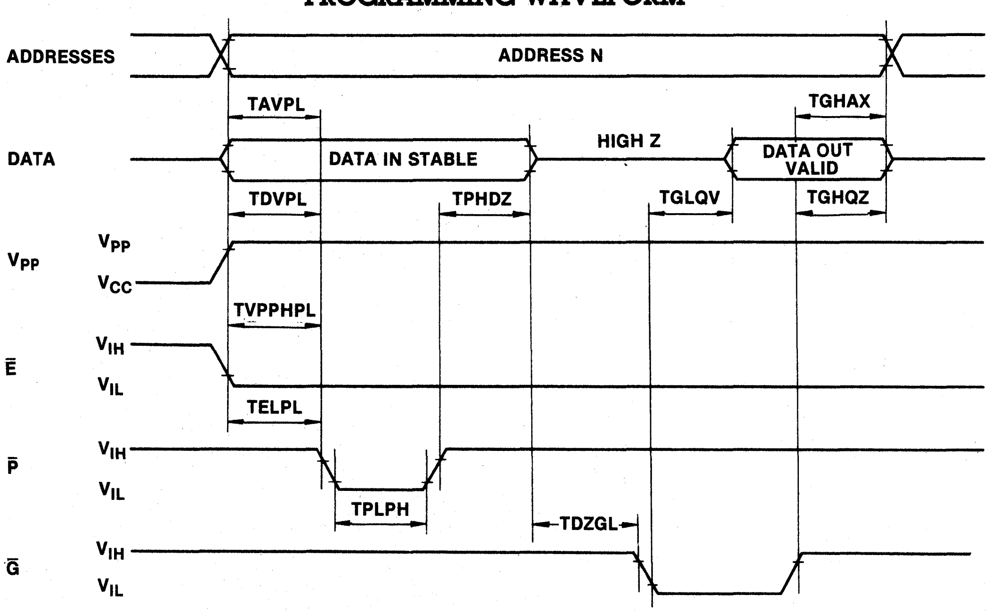
AC CHARACTERISTICS

($T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	TAVPL	2	—	—	μs
$\overline{E}$ Setup Time	TELPL	2	—	—	μs
Data Setup Time	TDVPL	2	—	—	μs
Address Hold Time	TGHAX	0	—	—	μs
Data Hold Time [1]	TPHDZ	2	—	—	μs
Chip Enable to Output Float Delay	TGHQZ	—	—	130	ns
V_{PP} Setup Time	TVPPHL	2	—	—	μs
$\overline{P}$ Pulse Width-Conventional	TPLPH	45	50	55	ms
$\overline{P}$ Pulse Width-Quick-Pro™	TPLPH	0.45	1.00	1.05	ms
$\overline{G}$ Setup Time [1]	TDZGL	2	—	—	μs
Data Valid from $\overline{G}$	TGLQV	—	—	150	ns

Notes:
[1] TPHDZ + TDZQL ≥ 50μs.

PROGRAMMING WAVEFORM



FUJITSU

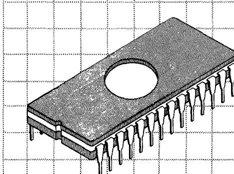
MBM27C64-25, MBM27C64-30
CMOS 65,536-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

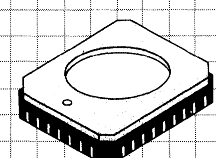
The Fujitsu MBM27C64 is a high speed 65,536-bit static Complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where the extremely low power consumption of CMOS is essential. The device dissipates only 40 mW/MHz when active, typically 5μW when in standby, yet it provides the same high speed performance as the NMOS MBM2764-type devices.

This package is available in either a Jedec Standard 28-pin dual-in-line package or a Jedec Standard 32-pin LCC package both of which have a transparent lid. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can be programmed into the memory.

The MBM27C64 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8192 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package
DIP-28C-C01

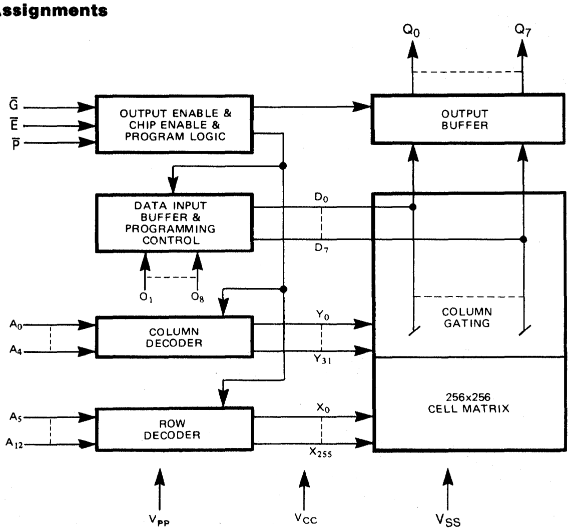


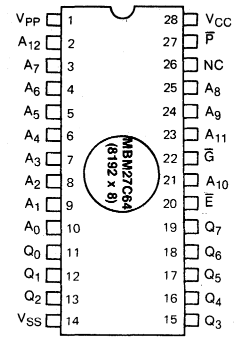
Leadless Chip Carrier
LCC-32C-A01

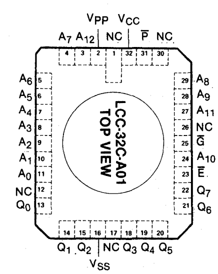
Features

- **CMOS Power Consumption:**
  550μW max. (Standby)
  5.5μW typ. (Standby)
  40mW/MHz (Active)
- **Fast Access Time:**
  MBM27C64-25 250 ns max.
  MBM27C64-30 300 ns max.
- **Utilizes the same simple programming requirements as MBM2764**
- **May be programmed 8 times faster than conventional methods using Fujitsu's QUICKPRO algorithm (see page 4-14)**
- **Single +5V operation**
- **10% V_{CC} tolerance standard**
- **TTL compatible inputs/outputs**
- **Three-state output provides OR-tie capability**
- **Output Enable $\overline{G}$ pin provides precise data bus control**
- **Pin and function compatible with 2764-type devices**
- **−40°C to +85°C and −55°C to +125°C temp. ranges available**

MBM27C64 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Parameter	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to V_{SS}	V_{IN}, V_{OUT}	−0.6 to +7	V
V_{CC} with Respect to V_{SS}	V_{CC}	−0.6 to +7	V
V_{PP} with Respect to V_{SS}	V_{PP}	−0.6 to +22	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections
(V_{CC}(28) = +5, V_{SS}(14) = GND)

Function (DIP Pin No.)

Mode	Address Input (2-10,21,23-25)	Data I/O (11-13,15-19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	I_{CC} Supply (28)	V_{PP} (1)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC1}	V_{CC}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH} / Don't Care	Don't Care / V_{IL}	I_{CC1}	V_{CC}
Stand By	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{SB1}	V_{CC}
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	I_{CC1}	V_{PP}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC1}	V_{PP}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{SB1}	V_{PP}

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	8	12	pF

Recommended Operating Conditions
(Referenced to V_{SS} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage (Note 1)	V_{CC}	4.50	5.0	5.50	V	
Supply Voltage	V_{PP}	V_{CC} −0.6	—	V_{CC} +0.6	V	0°C to +70°C
Supply Voltage	V_{SS}	—	GND	—	V	Note 2
Input High Voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.1	—	0.8	V	

Note 1. V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.
Note 2. −40°C to +85°C available as MBM27C64-25-X, MBM27C64-30-X −55°C to +125°C available as MBM27C64-30-W.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ (Note 1)	Max	Unit
Input Load Current (V_{IN} = 5.50V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.50V)	I_{LO}	—	—	10	μA
V_{PP} Supply Current	I_{PP}	—	1	100	μA
V_{CC} Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	—	—	1	mA
V_{CC} Standby Current ($\overline{E}$ = V_{CC} −0.3V to V_{CC} + 0.3V, I_{OUT} = 0mA)	I_{SB2}	—	1	100	μA
V_{CC} Active Current ($\overline{E}$ = V_{IL})	I_{CC1}	—	—	30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0mA)	I_{CC2}	—	—	30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

Note 1. V_{CC} = 5.0V and TA = 25°C.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

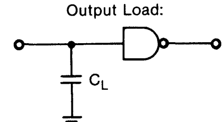
Parameter	Symbol	MBM27C64-25 Min	MBM27C64-25 Max	MBM27C64-30 Min	MBM27C64-30 Max	Unit
Address to Output Delay ($\overline{E}$ = $\overline{G}$ = V_{IL}, $\overline{P}$ = V_{IH})	TAVQV	—	250	—	300	ns
$\overline{E}$ to Output Delay ($\overline{G}$ = V_{IL}, $\overline{P}$ = V_{IH})	TELQV	—	250	—	300	ns
$\overline{G}$ to Output Delay ($\overline{E}$ = V_{IL}, $\overline{P}$ = V_{IH})	TGLQV	10	100	10	150	ns
$\overline{P}$ to Output Delay ($\overline{E}$ = $\overline{G}$ = V_{IL})	TPHQV	10	100	10	150	ns
Output Enable High to Output Float (See Note 2)	TGHQZ	0	60	0	105	ns
Address to Output Hold	TAXQX	0	—	0	—	ns

Note 2. TGHQZ is specified from $\overline{E}$, $\overline{G}$, or $\overline{P}$, whichever occurs first.

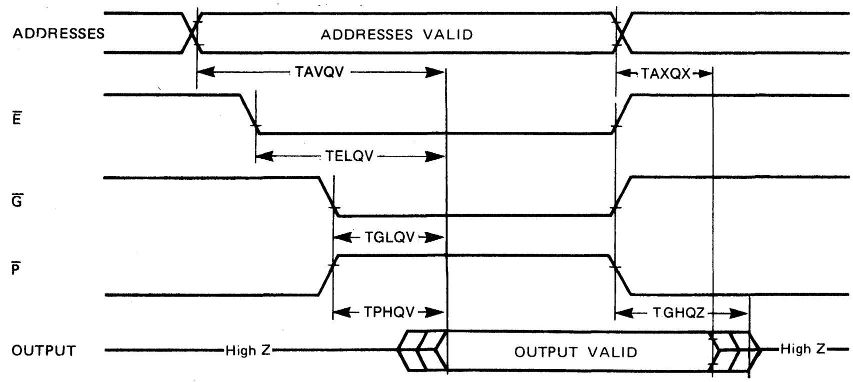
AC Test Conditions

Input Pulse Levels: 0.8 V to 2.2 V
Input Rise and Fall Time: ≤20nsec
Timing Measurement Reference Levels: 1.0 and 2.0V for inputs
0.8 and 2.0V for outputs
1 TTL gate and C_L = 100 pF

Output Load:



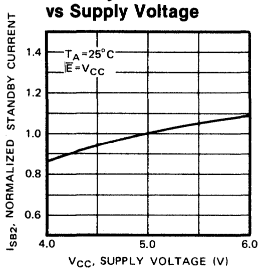
Operation Timing Diagram



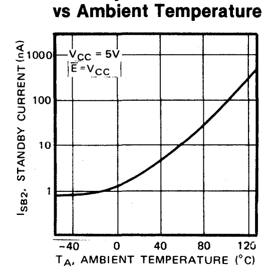
Note 3. Ḡ may be delayed up to TAVQV—TGLQV after the falling edge of Ē without impact on TAVQV.

Typical Characteristics Curves

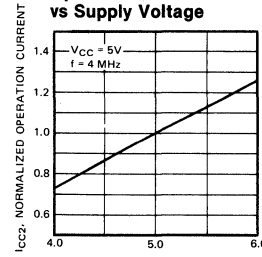
Standby Current vs Supply Voltage



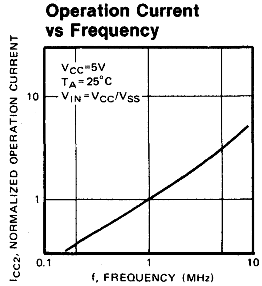
Standby Current vs Ambient Temperature



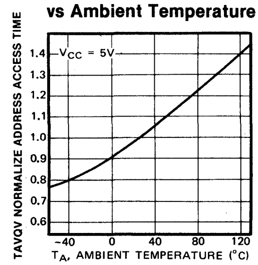
Operation Current vs Supply Voltage



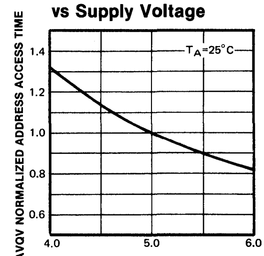
Operation Current vs Frequency



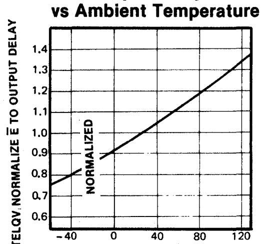
Address Access Time vs Ambient Temperature



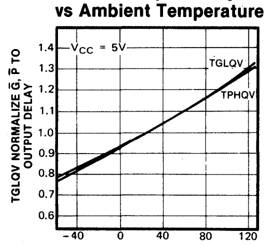
Address Access Time vs Supply Voltage



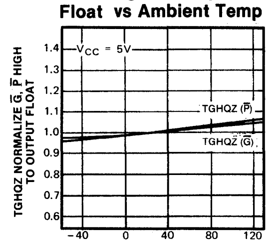
Ē to Output Delay vs Ambient Temperature



Ḡ, P̄ to Output Delay vs Ambient Temperature

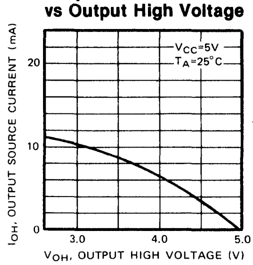


Ḡ, P̄ High to Output Float vs Ambient Temp

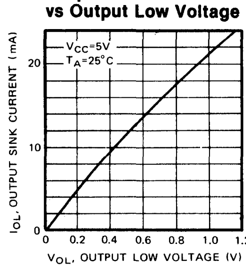


Typical Characteristics Curves, continued

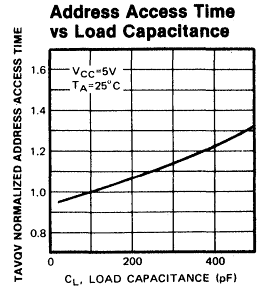
Output Source Current vs Output High Voltage



Output Sink Current vs Output Low Voltage



Address Access Time vs Load Capacitance



Programming/Erasing Information

Memory Cell Description

The MBM27C64 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C64 has all 65,536 bits in the "1" or high state. "0's" are loaded into the MBM27C64 through the procedure of programming.

Conventional Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ and $\overline{P}$ are both at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. A pattern of eight bits are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the P input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{P}$ input is prohibited when programming.

Fig. 1 — Memory Cell

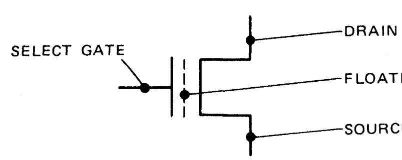
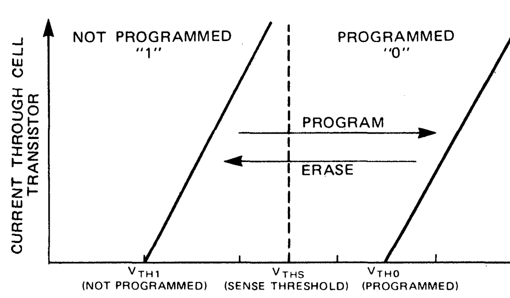


Fig. 2 — Memory Cell Threshold Shift



Programming/Erasing Information, continued

Quick Pro™ Programming
In addition to the standard 50 millisecond pulse width programming procedure, the MBM27C64 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulses to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the $\overline{E}$ input and a TTL high input must be applied to the $\overline{G}$ input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the $\overline{P}$ pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach proper stored charge levels.

Erasure
In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C64 to an ultraviolet light source. A dosage of 15W-seconds/cm2 is required to completely erase an MBM27C64. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm2) for 15 to 20 minutes. The MBM27C64 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C64 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C64 and such exposure should be prevented to realize maximum data retention. If used in such an environment, the package windows should be covered by an opaque label or substance.

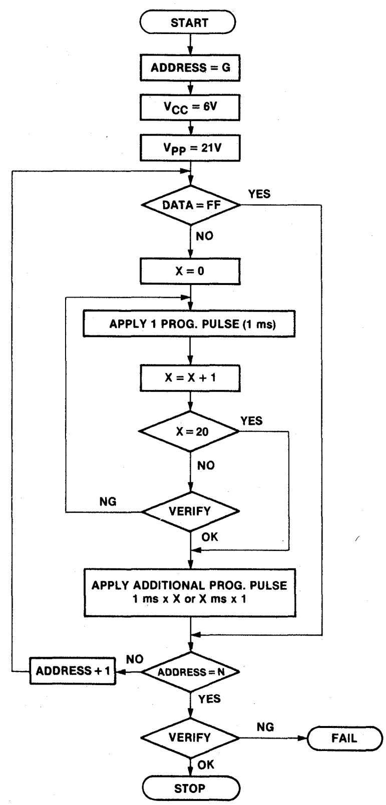
Fig. 3 — Quick Pro™ Program Flow Chart

V_{CC} = 6V ± 0.25V
V_{PP} = 21V ± 0.5V

T_{pw} = 1 ms ± 50μs
(* = X ms ± 5%)

G: START ADDRESS
N: STOP ADDRESS

MAXIMUM 40 ms + α/BYTE
MINIMUM 2 ms + α/BYTE
(FOR EXAMPLE
64K BIT EPROM
MAXIMUM 320sec + β
MINIMUM 16sec + β



QUICK PRO™ IS A TRADEMARK OF FUJITSU LIMITED

DC Characteristics
(T_A = 25 ±5°C,
V_{CC} = 5V ±10% (Conventional),
V_{CC} = 6V ± 0.25V (Quick Pro™)
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	V_{IN} = 0.45V-5.25V
Output Low Voltage During Verify	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
Output High Voltage During Verify	V_{OH}	2.4	—	V	I_{OH} = −400mA
V_{CC} Supply Current	I_{CC1}	—	30	mA	—
Input Low Voltage	V_{IL}	−0.1	0.8	V	—
Input High Voltage	V_{IH}	2.0	V_{CC} +0.3	V	—
V_{PP} Supply Current During Programming Pulse	I_{PP2}	—	30	mA	E = P = V_{IL}

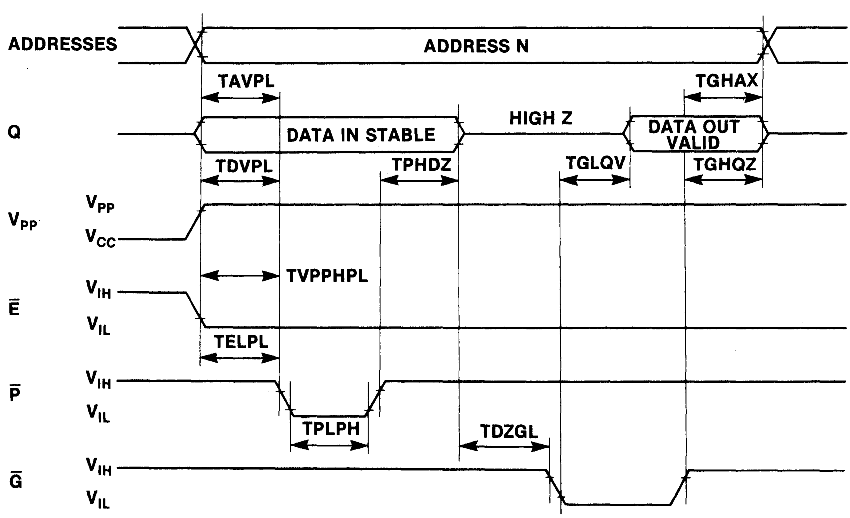
Note 1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
Note 2. V_{PP} must not be greater than 21.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{E} = \overline{P} = V_{IL}$, V_{PP} must not be switched from 5 volts to 21 volts or vise-versa.

AC Characteristics
(T_A = 25 ±5°C,
V_{CC} = 5V ±10% (Conventional),
V_{CC} = 6V ± 0.25V (Quick Pro™)
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	TAVPL	2	—	—	μs
$\overline{E}$ Setup Time	TELPL	2	—	—	μs
Data Setup Time	TDVPL	2	—	—	μs
Address Hold Time	TGHAX	0	—	—	μs
Data Hold Time [1]	TPHDZ	2	—	—	μs
Chip Enable to Output Float Delay	TGHQZ	0	—	130	ns
V_{PP} Setup Time	TVPPHPL	2	—	—	μs
$\overline{P}$ Pulse Width-Conventional	TPLPH	25	50	55	ms
$\overline{P}$ Pulse Width-Quick-Pro™	TPLPH	0.95	1.00	1.05	ms
$\overline{G}$ Setup Time [1]	TDZGL	2	—	—	μs
Data Valid from $\overline{G}$	TGLQV	—	—	150	ns

Note [1] TPHDZ + TDZGL ≥ 50μs.

Programming Waveform



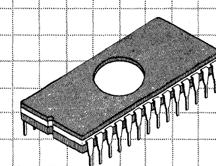
MBM27128-25, MBM27128-30
UV Erasable 131,072-Bit Read Only Memory

Description

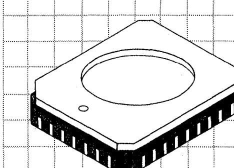
The Fujitsu MBM27128 is a high speed 131,072-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin dual in-line package or leadless chip carrier (32-pin) with a transparent lid is used to package the MBM27128. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27128 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 16,384 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in single supply systems.



Cerdip Package
DIP-28C-C01



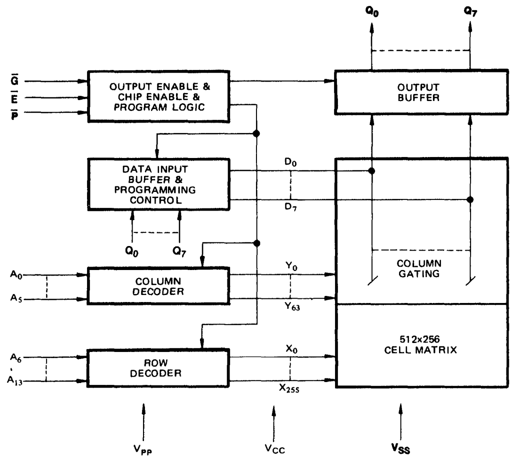
Leadless Chip Carrier
LCC-32C-A01

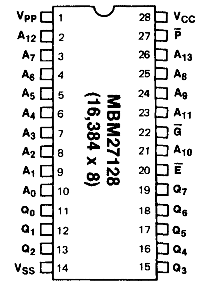
Features

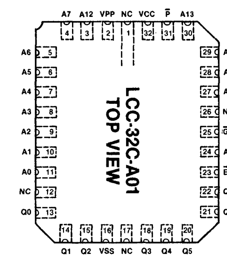
- **Organized as 16,384 x 8 fully decoded**
- **Low power requirement: [550 mW (act), 193 mW (standby)]**
- **No clocks required (fully static operation)**
- **Programmable utilizing the Quick Pro™ Algorithm**
- **Program compatible with the Intel int$_e$ligent Programming™ Algorithm**
- **Fast access Time:**
  MBM27128-25 250 ns Max.
  MBM27128-30 300 ns Max.
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable $\overline{G}$ pin provides precise control of the data bus**
- **Single +5V operation**
- **Standard 28-pin DIP package**
- **Pin compatible with Intel 27128**

Quick Pro™ is a trademark of Fujitsu Microelectronics Inc.
int$_e$ligent Programming™ is a trademark of Intel Corporation.

MBM27128 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Parameter	Symbol		Unit
Temperature Under Bias	T_A	-25 to $+85$	°C
Storage Temperature	T_{stg}	-65 to $+125$	°C
Inputs/Outputs with Respect to V_{SS}	V_{IN}, V_{OUT}	-0.6 to $+7$	V
V_{PP} with Respect to V_{SS}	V_{PP}	-0.6 to $+22$	V
V_{CC} with Respect to V_{SS}	V_{CC}	-0.6 to $+7$	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections

Mode	Function (DIP Pin No.) Address Input A_0-A_{13} (2-10, 23-26, 21)	Data Q_0-Q_7 (11-13, 15-19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	V_{CC} (28)	V_{PP} (1)	V_{SS} (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	V_{SS}
Output Disable	Don't Care	High Z	V_{IL}	V_{IH} / Don't Care	Don't Care / V_{IL}	V_{CC}	V_{CC}	V_{SS}
Stand by	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	V_{SS}
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	V_{SS}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	V_{SS}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	V_{SS}

Capacitance
($T_A = 25°C$, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance ($V_{IN} = 0V$)	C_{IN}	—	4	6	pF
Ouput Capacitance ($V_{OUT} = 0V$)	C_{OUT}	—	8	12	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
V_{PP} Supply Voltage	V_{PP}	$V_{CC}-0.6$	—	$V_{CC}+0.6$	V	
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+1$	V	
Input Low Voltage	V_{IL}	−0.1	—	0.8	V	

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

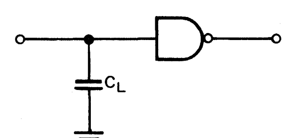
Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current ($V_{IN} = 5.5V$)	I_{LI}	—	—	10	μA
Output Leakage Current ($V_{OUT} = 5.5V$)	I_{LO}	—	—	10	μA
V_{CC} Standby Current ($\overline{E} = V_{IH}$)	I_{CC1}	—	—	35	mA
V_{CC} Supply Current ($\overline{E} = V_{IL}$)	I_{CC2}	—	—	100	mA
V_{PP} Supply Current ($V_{PP} = V_{CC} \pm 0.6V$)	I_{PP}	—	—	5	mA
Output Low Voltage ($V_{OL} = 2.1mA$)	V_{OL}	—	—	0.45	V
Output High Voltage ($I_{OH} = -400\mu A$)	V_{OH}	2.4	—	—	V

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

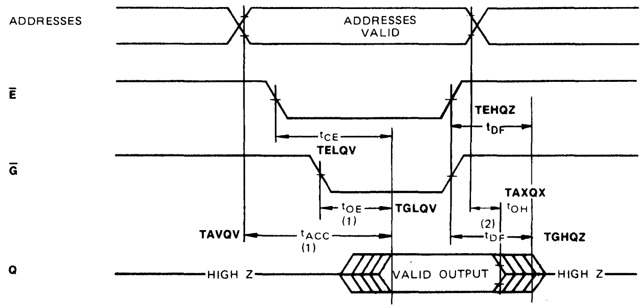
		MBM27128-25		MBM27128-30		
Parameter	Symbol	Min	Max	Min	Max	
Address Access Time	TAVQV	—	250	—	300	ns
$\overline{E}$ to Output Delay	TELQV	—	250	—	300	ns
$\overline{G}$ to Output Delay	TGLQV	—	100	—	120	ns
Address to Hold Time	TAXQX	0	—	0	—	ns
$\overline{E}$ or $\overline{G}$ High to Output Float	TGHQZ, TEHQZ	0	60	0	105	ns

AC Test Conditions
(Including programming)

Input Pulse levels:	**0.8V to 2.2V**
Input Rise and Fall Time:	**≤20nsec**
Timing Measurement Reference Levels:	**1.0V and 2.0V for inputs**
	0.8V and 2.0V for outputs
Output Load:	**1 TTL gate and C_L = 100 pF**



Operation Timing Diagram



Note 1. $\overline{G}$ may be delayed up to TAVQV-TGLQV after falling edge of $\overline{E}$ without impact on TAVQV.
Notes 2. TGHDZ or TEHQZ is specified from $\overline{G}$ or $\overline{E}$ respectively, which ever occurs first.

Programming/Erasing Information

Memory Cell Description

The MBM27128 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Conventional Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27128 has all 131,072-bits in the "1" or high state. "0's" are loaded into the MBM27128 through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ and $\overline{P}$ are both at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the $\overline{P}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{P}$ input is prohibited when programming.

Fig. 1 — Memory Cell

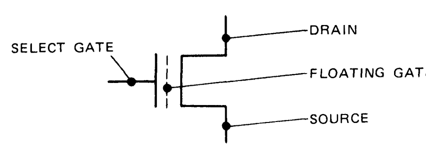
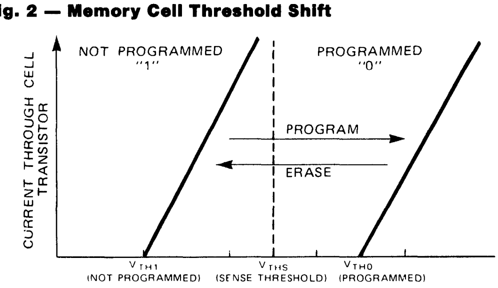


Fig. 2 — Memory Cell Threshold Shift



Programming/Erasure Information, continued

"Quick Pro™" Programming

In addition to the standard 50 millisecond pulse width programming procedure, the MBM27128 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulse to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

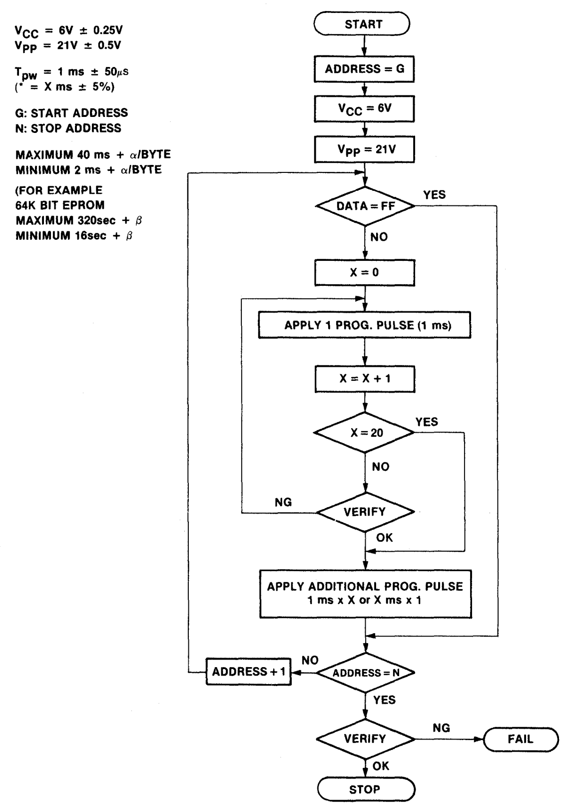
The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the $\overline{E}$ input and a TTL high input must be applied to the $\overline{G}$ input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the $\overline{P}$ pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach sufficient stored charge levels.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27128 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27128. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2 for 15 to 20 minutes. The MBM27128 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27128 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27128 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Figure 3. — Quick Pro™ Flow Chart



QUICK PRO™ IS A TRADEMARK OF FUJITSU LIMITED

Programming Characteristics

DC Characteristics

(T_A = 25 ±5°C,
V_{CC} = 5V ±5% (Conventional),
V_{CC} = 6V ± 0.25V (Quick Pro™)
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	V_{IN} = 5.25V/0.45V
V_{PP} Supply Current During Programming Pulse	I_{PP2}	—	30	mA	$\overline{E} = \overline{P} = V_{IL}$
V_{PP} Supply Current During Verify	I_{PP3}	—	5	mA	$\overline{E} = V_{IL}$ $\overline{P} = V_{IH}$
V_{PP} Supply Current Program Inhibit (Active)	I_{PP4}	—	5	mA	$\overline{E} = V_{IH}$
V_{CC} Supply Current Program Inhibit	I_{CC1}	—	35	mA	$\overline{E} = V_{IH}$
V_{CC} Supply Current Program & Verify	I_{CC2}	—	100	mA	—
Input Low Voltage	V_{IL}	−0.1	+0.8	V	—
Input High Voltage	V_{IH}	2.0	V_{CC}+1	V	—
Output Low Voltage During Verify	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
Output High Voltage During Verify	V_{OH}	2.4	—	V	I_{OH} = −400μA

Note 1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

Note 2. V_{PP} must not be greater than 21.5 volts including overshot. Permanent device change may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{E} = \overline{P} = V_{IL}$, V_{PP} must not be switched from V_{CC} to 21 volts or vise-versa.

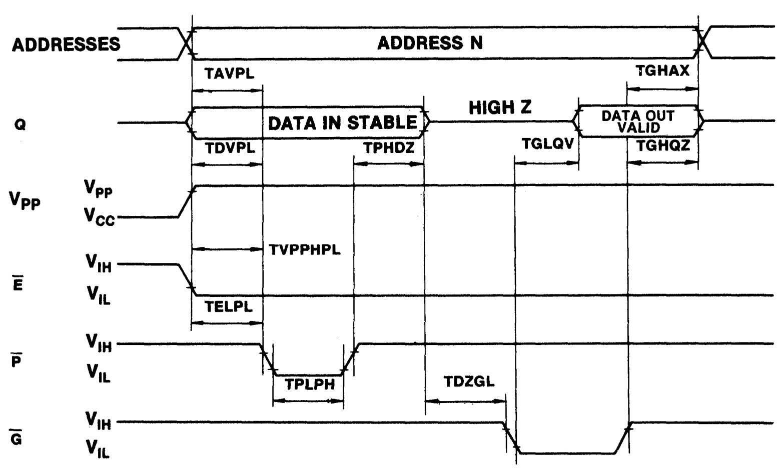
AC Characteristics

(T_A = 25 ±5°C,
V_{CC} = 5V ±5% (Conventional),
V_{CC} = 6V ± 0.25V (Quick Pro™)
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	TAVPL	2	—	—	μs
Chip Enable Setup Time	TELPL	2	—	—	μs
Output Enable Time [1]	TDZGL	2	—	—	μs
Data Setup Time	TDVPL	2	—	—	μs
Address Hold Time	TGHAX	0	—	—	μs
Data Hold Time [1]	TPHDZ	2	—	—	μs
Output Enable to Output Float Delay	TGHQZ	—	—	130	ns
Data Valid from Output Enable	TGLQV	—	—	150	ns
V_{PP} Setup Time	TVPPHPL	2	—	—	μs
$\overline{P}$ Pulse Width-Conventional	TPLPH	25	50	55	ms
$\overline{P}$ Pulse Width-Quick-Pro™	TPLPH	0.95	1.00	1.05	ms

Note [1] TPHDZ + TDZGL ≥ 50μs.

Programming Waveform



Preliminary

MOS Memories

FUJITSU

■ MBM27256-20, MBM27256-25, MBM27256-30

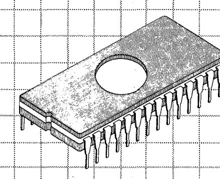
CMOS 32,768 X 8-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

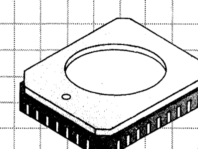
The Fujitsu MBM27256 is a high speed 262,144-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual in-line package with a transparent lid and 32-pad leadless chip carrier (LCC) are used to package the MBM27256. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27256 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package DIP-28C-C01

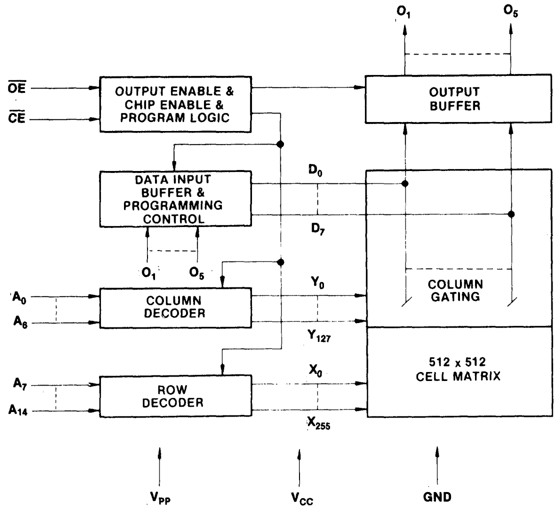


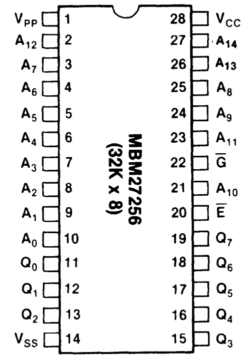
Ceramic Package LCC-32C-A01

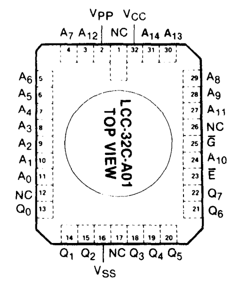
Features

- **32,768 words by 8-bits organization, fully decoded**
- **Programming utilizing the Quick Pro™ Algorithm**
- **Programs with two 1 ms pulses**
- **Low Power requirement [525 mW (act.), 210 mW (standby)]**
- **No clocks required (fully static operation)**
- **TTL compatible inputs and outputs**
- **Three state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Fast Access Time:**
  MBM27256-20 200 ns max.
  MBM27256-25 250 ns max.
  MBM27256-35 300 ns max.
- **Single +5V operation**
- **Standard 28-pin DIP package/32-pad LCC**

MBM27256 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Parameter	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
V_{PP} with Respect to GND	V_{PP}	−0.6 to +22	V
V_{CC} with Respect to GND	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections

Function (DIP Pin No.) / Mode	Address Input (2~10, 21, 23~27)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{CC}	V_{CC}	GND
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Stand By	Don't Care	High Z	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	V_{CC}	V_{PP}	GND

Capacitance
($T_A = 25°C$, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance ($V_{IN} = 0V$)	C_{IN}	—	4	6	pF
Output Capacitance ($V_{OUT} = 0V$)	C_{OUT}	—	8	12	pF

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} Supply Voltage(1)	V_{CC}	4.75	5.0	5.25	V	0°C to +70°C
V_{PP} Supply Voltage	V_{PP}	V_{CC} −0.6	—	V_{CC} +0.6	V	
Input High Voltage	V_{IH}	2.0	—	V_{CC} +1	V	
Input Low Voltage	V_{IL}	−0.1	—	0.8	V	

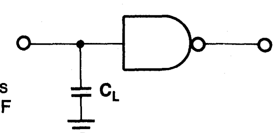
Note 1. V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current ($V_{IN} = 5.25V$)	I_{LI}	—	—	10	μA
Output Leakage Current ($V_{OUT} = 5.25V$)	I_{LO}	—	—	10	μA
V_{CC} Standby Current ($\overline{CE} = V_{IH}$)	I_{CC1}	—	—	40	mA
V_{CC} Supply Current ($\overline{CE} = V_{IL}$)	I_{CC2}	—	—	100	mA
V_{PP} Standby Current ($V_{PP} = V_{CC} \pm 0.6V$)	I_{PP}	—	—	5	mA
Output Low Voltage ($I_{OL} = 2.1$ mA)	V_{OL}	—	—	0.45	V
Output High Voltage ($I_{OH} = -400\mu A$)	V_{OH}	2.4	—	—	V

AC Test Conditions

Input Pulse Levels:	0.8 V to 2.2 V
Input Rise and Fall Times:	≤ 20 ns
Timing Measurement Reference Levels:	1.0 V and 2.0 V for inputs 0.8 V and 2.0 V for outputs
Output Load:	1 TTL gate and $C_L = 100$ pF

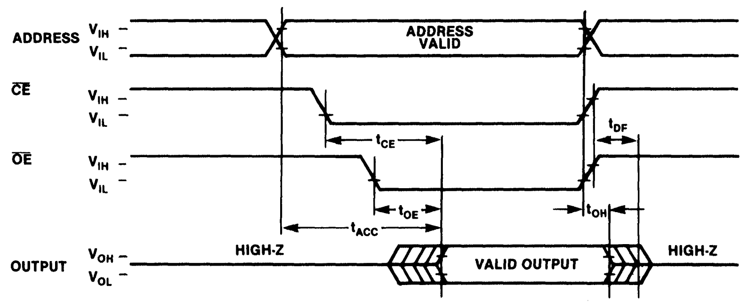


AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27256-20 Min	Typ	Max	MBM27256-25 Min	Typ	Max	MBM27256-30 Min	Typ	Max	Unit
Address to Output Delay*1	t_{ACC}	—	—	200	—	—	250	—	—	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	—	—	200	—	—	250	—	—	300	ns
$\overline{OE}$ to Output Delay*1	t_{OE}	10	—	70	10	—	100	10	—	120	ns
Address to Output Hold	t_{OH}	0	—	—	0	—	—	0	—	—	ns
Output Enable High to Output Float*2	t_{DF}	0	—	60	0	—	60	0	—	105	ns

Notes:
***1.** $\overline{OE}$ may be delayed up to t_{ACC}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
***2.** t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output Float is defined as the point where data is no longer driven.

Operation Timing Diagram



Programming/Erasing Information

Memory Cell Description

The MBM27256 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 3). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 4). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Conventional Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27256 has all 262,144 bits in the "1", or high, state. "0's" are loaded into the MBM27256 through the procedure of programming.

Quick Pro™ Programming

The programming mode is entered when +12.5V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{CE}$ and $\overline{OE}$ are V_{IH}. A 0.1µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit pattern are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 msec, TTL low-level pulse is applied to the $\overline{CE}$ pin and after that additional pulse is applied to the $\overline{CE}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flow chart.)

1) Input the start address (Address = G).
2) Set the V_{CC} = 6V and V_{PP} = 12.5V.
3) Data input.
4) Compare the input data. If data are FF, jump to the 11). If data are not FF, proceed the next step.
5) Set the number of programming pulse to 0. (X = 0).
6) Apply ONE programming pulse to $\overline{CE}$ pin (t_{PW} = 1 ms Typ.)
7) Count the programming pulse (X = X + 1).

Fig. 1 — Memory Cell

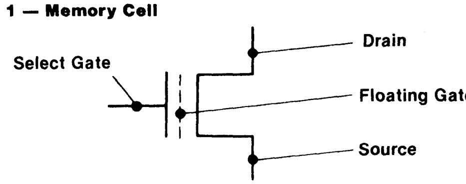
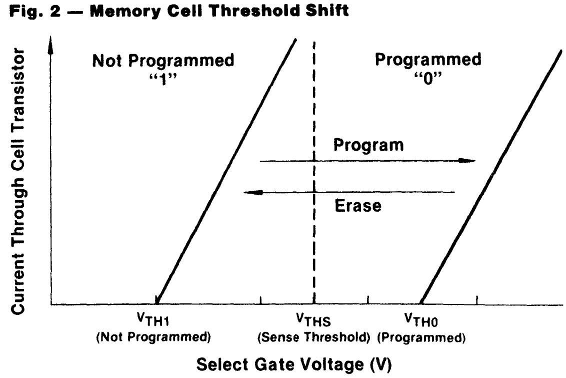


Fig. 2 — Memory Cell Threshold Shift



Programming/Erasing Information, continued

8) Compare the number of programming pulse. If X = 20, jump to the 10). If X < 20, proceed the next step.
9) Verify the data. If programmed data are the same as input data, proceed the next step. If programming data are not the same as input data, repeat the 6) thru 8).
10) Apply the additional programming pulse to the $\overline{CE}$ pin (1 ms x X or X ms x 1).
11) Compare the address. If the programmed address is end address, proceed the next step.
    If the programmed address is not end address, proceed from step 3) for next address (G +).
12) Verify the data. If programmed data are not the same as input data, the part is no good. If programmed data are the same as input data, programming is end.

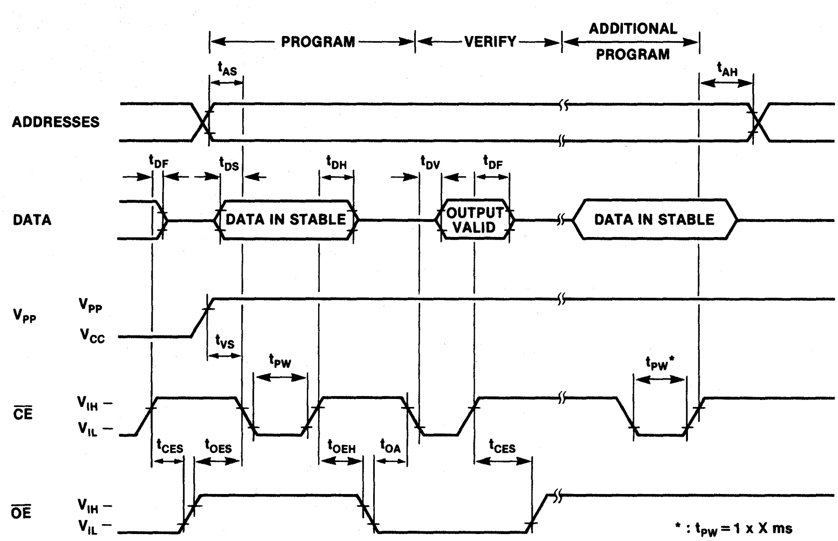
All that is required is that one 1 msec program pulse be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 1.05 msec. Therefore, applying a DC level to the PGM input is prohibited when programming.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27256 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27256. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2) for 15 to 20 minutes. The MBM27256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27256 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27256 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Programming Waveform



Programming/Erasing Information, continued

DC Characteristics
($T_A = 25° \pm 5°C$,
$V_{CC} = 6V \pm .025V$,
$V_{PP} = 12.5V \pm 0.5V$)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current ($V_{IN} = 5.25V/0.45V$)	I_{LI}	—	—	10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE} = V_{IL}$)	I_{PP}	—	—	30	mA
V_{CC} Supply Current	I_{CC}	—	—	30	mA
Input Low Voltage	V_{IL}	−0.1	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Output Low Voltage During Verify ($I_{OL} = 2.1$ mA)	V_{OL}	—	—	0.45	V
Output High Voltage During Verify ($I_{OH} = -400\mu A$)	V_{OH}	2.4	—	—	V

Notes:
(1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
(2) V_{PP} must not be greater than 13 V including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.5 volts or vise-versa.

AC Characteristics
($T_A = 25 \pm 5°C$,
$V_{CC} = 6V \pm 0.25V$,
$V_{PP} = 21V \pm 0.5V$)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2	—	—	μs
$\overline{CE}$ Setup Time	t_{CES}	2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
V_{PP} Setup Time	t_{VS}	2	—	—	μs
Address Hold Time	t_{AH}	2	—	—	μs
$\overline{OE}$ Hold Time*	t_{OEH}	2	—	—	μs
Data Hold Time	t_{DH}	2	—	—	μs
$\overline{OE}$ Recovery Time*	t_{OA}	2	—	—	μs
$\overline{CE}$ to Output Valid	t_{DV}	—	—	1	μs
Output Disable to Output Float Delay	t_{DF}	—	—	130	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms

* $t_{OEH} + t_{OR} \geq 50\ \mu s$

Programming/Erasing Information, continued

Fig. 3 — Quick Pro™ Program Flow Chart

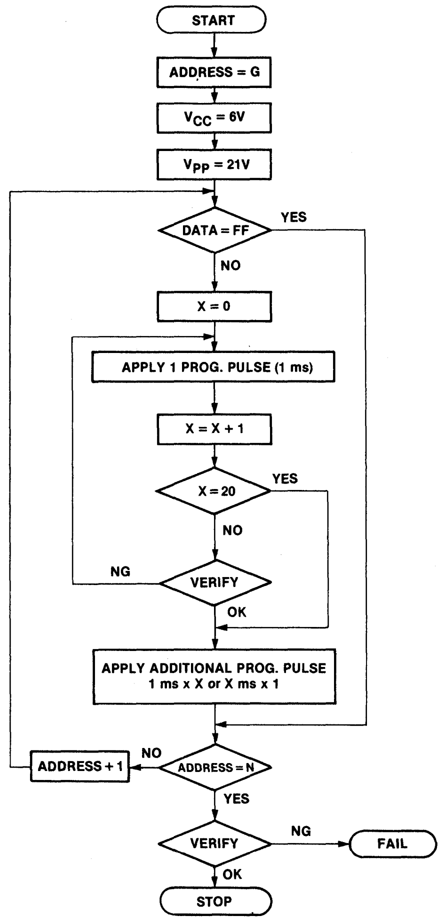
V_{CC} = 6V ± 0.25V
V_{PP} = 21V ± 0.5V

T_{pw} = 1 ms ± 50μs
(* = X ms ± 5%)

G: START ADDRESS
N: STOP ADDRESS

MAXIMUM 40 ms + α/BYTE
MINIMUM 2 ms + α/BYTE

(FOR EXAMPLE
64K BIT EPROM
MAXIMUM 320sec + β
MINIMUM 16sec + β



QUICK PRO™ IS A TRADEMARK OF FUJITSU LIMITED

FUJITSU

MBM27C256-25, MBM27C256-30, MBM27C256-45

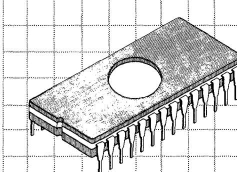
CMOS 32,768 X 8-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

The Fujitsu MBM27C256 is a high speed 262,144-bits complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad leadless chip carrier (LCC) are used to package the MBM27C256. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

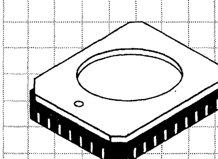
The MBM27C256 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package DIP-28C-C01

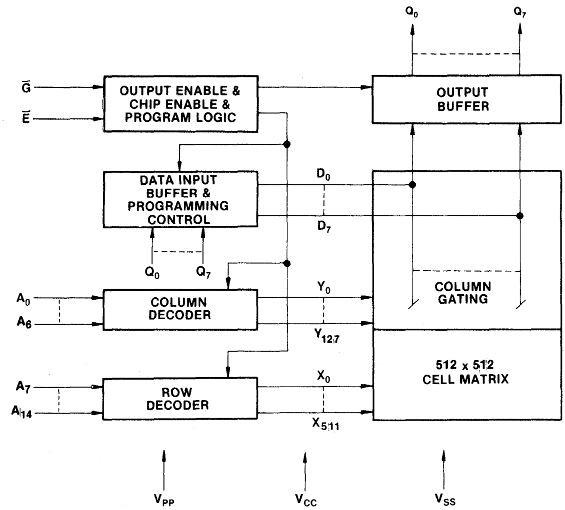
Features

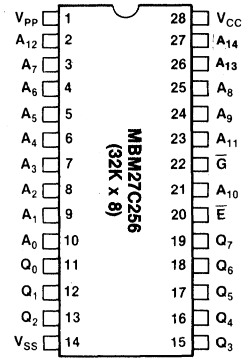
- CMOS Power Consumption:
  550 μW max. (Standby)
  40 mW/MHz (Active)
- 32,768 words by 8-bits organization, fuly decoded
- Simple programming requirements
- Single location programming
- High speed programming algorythm (typically two 1 ms pulses)
- No clock required (fully static operation)
- TTL compatible inputs and outputs
- Three state output with OR-tie capability
- Output Enable $\overline{G}$ pin for simplified memory expansion
- Fast Access Time:
  MBM27C256-25 250 ns max.
  MBM27C256-30 300 ns max.
  MBM27C256-45 450 ns max.
- Single +5V operation
- Jedec Standard 28-pin DIP package/32-pad LCC

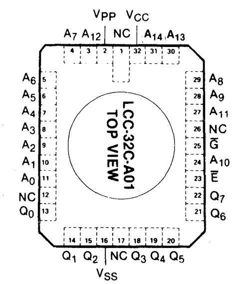


Ceramic Package LCC-32C-A01

MBM27C256 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Parameter	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
V_{PP} with Respect to GND	V_{PP}	−0.6 to +22	V
V_{CC} with Respect to GND	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections

Function (DIP Pin No.) / Mode	Address Input (2~10, 21, 23~27)	Data (11~13, 15~19)	$\overline{E}$ (20)	$\overline{G}$ (22)	V_{CC} (28)	V_{PP} (1)	V_{SS} (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{CC}	V_{CC}	GND
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Stand By	Don't Care	High Z	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	V_{CC}	V_{PP}	GND

Capacitance
($T_A = 25°C$, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	12	pF

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} Supply Voltage[1]	V_{CC}	4.50	5.0	5.50	V	0°C to +70°C
V_{PP} Supply Voltage	V_{PP}	V_{CC} −0.6	—	V_{CC} +0.6	V	
Input High Voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.1	—	0.8	V	

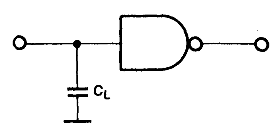
Note 1. V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.25V)	I_{LO}	—	—	10	μA
V_{PP} Supply Current	I_{PP}	—	1	100	μA
V_{CC} Standby Current ($\overline{E} = V_{IH}$)	I_{SB1}	—	—	1	mA
V_{CC} Standby Current ($\overline{E} = V_{CC}$ −0.3V to V_{CC} + 0.3V, I_{OUT} = 0mA)	I_{SB2}	—	1	100	μA
V_{CC} Active Current ($\overline{E} = V_{IL}$)	I_{CC1}	—	—	30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0mA)	I_{CC2}	—	—	30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH1}	2.4	—	—	V
Output High Voltage (I_{OH} = −100μA)	V_{OH2}	V_{CC} −0.7	—	—	V

AC Test Conditions

Input Pulse Levels: 0.8 V to 2.0 V
Input Rise and Fall Time: ≤20 ns
Timing Measurement Reference Levels: 1.0 V and 2.0 V for inputs; 0.8 V and 2.0 V for outputs
Output Load: 1 TTL gate and C_L = 100pF



AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27C256 -25 Min	MBM27C256 -25 Max	MBM27C256 -30 Min	MBM27C256 -30 Max	MBM27C256 -45 Min	MBM27C256 -45 Max	Unit
Address to Output Delay ($\overline{E} = \overline{G} = V_{IL}$)	TAVQV	—	250	—	300	—	450	ns
$\overline{E}$ to Output Delay ($\overline{G} = V_{IL}$)	TELQV	—	250	—	300	—	450	ns
$\overline{G}$ to Output Delay ($\overline{E} = V_{IL}$)	TGLQV	—	100	—	120	—	150	ns
Output Enable High to Output Float (See Note)	TGHQZ	0	60	0	105	—	130	ns
Address to Output Hold	TAXQX	0	—	0	—	0	—	ns

Note: TGHQZ is specified from $\overline{E}$, or $\overline{G}$, whichever occurs first.

Programming/Erasing Information, continued

The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the E input and a TTL high input must be applied to the G input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the P pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach sufficient stored charge levels.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C256 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27C256. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2) for 15 to 20 minutes. The MBM27C256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

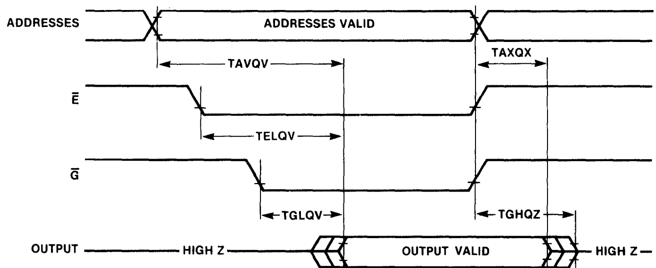
It is important to note that the MBM27C256 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C256 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

DC Characteristics
(T_A = 25 ±5 °C,
V_{CC} = 6V ±0.25V,
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}	—	—	10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{E} = V_{IL}$)	I_{PP}	—	—	30	mA
V_{CC} Supply Current	I_{CC}	—	—	30	mA
Input Low Voltage	V_{IL}	−0.1	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}	—	—	0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

Notes:
(1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
(2) V_{PP} must not be greater than 21.5 V including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{E} = V_{IL}$, V_{PP} must not be switched from 5 volts to 21 volts or vise-versa.

Operation Timing Diagram



Notes: 1. $\overline{G}$ may be delayed up to TAVQV—TGLQV after the falling edge of $\overline{E}$ without impact on TAVQV.
2. TGHQZ is specified from $\overline{E}$ or $\overline{G}$, whichever occurs first.

Programming/Erasing Information

Memory Cell Description

The MBM27C256 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 3). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 4). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 4.

Conventional Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C256 has all 262,144 bits in the "1", or high, state. "0's" are loaded into the MBM27C256 through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ is at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. A pattern of eight bits are placed on the respective output pins. The voltage levels should be standard TTL levels.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55.0 msec.

"Quick Pro" Programming

In addition to the standard 50 millisecond pulse width programming procedure, the MBM27C256 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulse to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

Fig. 1 — Memory Cell

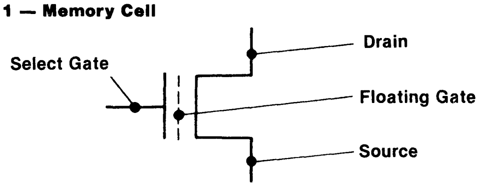
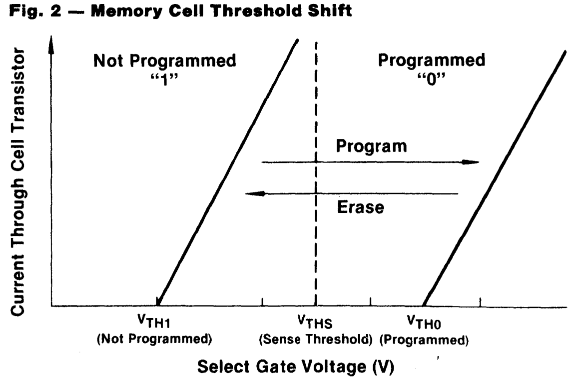


Fig. 2 — Memory Cell Threshold Shift

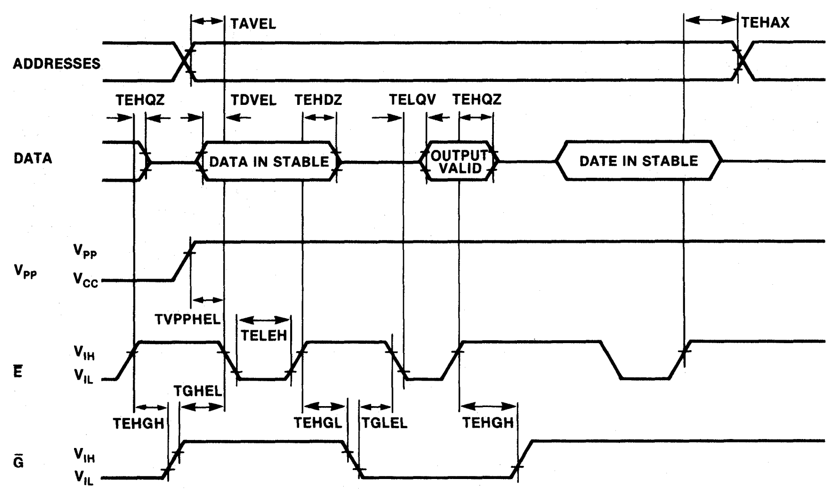


AC Characteristics
(T_A = 25 ±5 °C,
V_{CC} = 5V ±5%
V_{PP} = 21V ±0.5V)

Parameter		Symbol	Min	Typ	Max	Unit
Address Setup Time		TAVEL	2	—	—	µs
$\overline{E}$ Setup Time		TEHGH	2	—	—	µs
$\overline{G}$ Setup Time		TGHEL	2	—	—	µs
Data Setup Time		TDVEL	2	—	—	µs
V_{PP} Setup Time		TVPPHEL	2	—	—	µs
Address Hold Time		TEHAX	2	—	—	µs
$\overline{G}$ Hold Time	1	TEHGL	2	—	—	µs
Data Hold Time		TEHDZ	2	—	—	µs
$\overline{G}$ Recovery Time	1	TGLEL	2	—	—	µs
$\overline{E}$ to Output Valid		TELQV	—	—	1	µs
Output Disable to Output Float Delay		TEHQZ	—	—	130	ns
Programming Pulse Width-Quick-Pro™		TELEH	0.95	1.00	1.05	ms
Programming Pulse Width-Conventional		TELEH	45	50	55	

1 TEHGL + TGLEL ≥ 50 µs

Programming Waveform



Bipolar RAMs

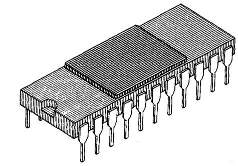
Quick Guide To Products in This Section

Device	Technology	Organization	Access Time (max)	Power Supply Volts	Maximum Power Dissipation with Typical Power Supply	Package	Page
MB7072E	ECL	256 x 4	125 nS	+5.2	1040 mW	22-pin	5-2
MBM10415AH	ECL	1K x 1	20 nS	−5.2	780 mW	16-pin	5-7
MBM10422	ECL	256 x 4	10 nS	−5.2	1040 mW	24-pin	5-12
MBM10422A-7	ECL	256 x 4	7 nS	−5.2	1040 mW	24-pin	5-17
MBM10470A-10	ECL	4K x 1	20 nS	−5.2	1040 mW	18-pin	5-22
MBM10474-15	ECL	1K x 4	15 nS	−5.2	1040 mW	24-pin	5-26
MBM10480-25	ECL	16K x 1	25 nS	−5.2	936 mW	20-pin	5-30
MBM93419	TTL	64 x 9	45 nS	+5	1000 mW	28-pin	5-34
MBM100422A-7	ECL	256 x 4	7 nS	−4.5	900 mW	24-pin	5-38
MBM100474-15	ECL	1K x 4	15 nS	−4.5	900 mW	24-pin	5-42
MBM100480-25	ECL	16K x 1	15 nS	−4.5	1100 mW	20-pin	5-47

ECL 256 X 4-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MB7072 is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. The MB7072 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production. Operation for the MB7072 is specified over a temperature range of 0 °C to 75 °C (ambient).

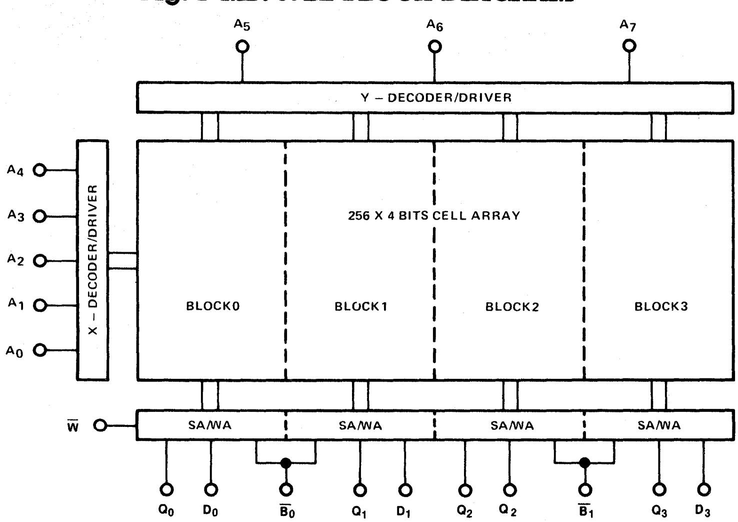


CERAMIC PACKAGE
DIP-22C-F01

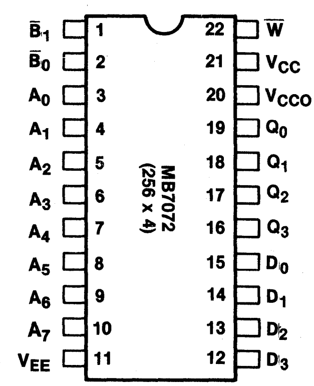
FEATURES

- **Organized as 256 words by 4-bits**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry standard 10K-series ECL families**
- **Address Access Time: MB7072E 12ns Max.**
- **DOPOS and IOP Processing**
- **Two block select pins for flexibility in organization**

Fig. 1-MB7072E BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{B}$	$\overline{W}$	DI		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DO	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−25 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in operational sections of this data sheet.

GUARANTEED OPERATING RANGES

Part Number	Supply Voltage (V_{EE})			Ambient Temperature
	Min	Typ	Max	
MB7072 E	−5.46V	−5.2V	−4.94V	0 °C to 75 °C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
*Input Pin Capacitance	C_{IN}	—	—	8	pF
Output Pin Capacitance	C_{OUT}	—	—	8	pF

*$\bar{B}$ Capacitance = 12pF (max)

DC CHARACTERISTICS

($V_{CC} = V_{CCO} = 0V, V_{EE} = -5.2V$, Output Load = 50Ω to −2.0V, with transverse airflow ≥ 2.5 m/s, unless otherwise noted.)

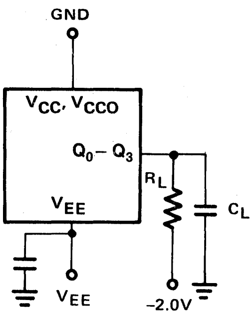
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IHmax}$ or V_{ILmin})	V_{OH}	−1000 −960 −900	— — —	−840 −810 −720	mV	0 °C 25 °C 75 °C
Output Low Voltage ($V_{IN} = V_{INmax}$ or V_{ILmin})	V_{OL}	−1870 −1850 −1830	— — —	−1665 −1650 −1625	mV	0 °C 25 °C 75 °C
Output High Voltage ($V_{IN} = V_{IHmin}$ or V_{ILmax})	V_{OHC}	−1020 −980 −920	— — —	— — —	mV	0 °C 25 °C 75 °C
Output Low Voltage ($V_{IN} = V_{IHmin}$ or V_{ILmax}	V_{OLC}	— — —	— — —	−1645 −1630 −1605	mV	0 °C 25 °C 75 °C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	— — —	−840 −810 −720	mV	0 °C 25 °C 75 °C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	— — —	−1490 −1475 −1450	mV	0 °C 25 °C 75 °C
*Input High Current ($V_{IN} = V_{IHmax}$)	I_{IH}	—	—	220	μA	0° to 75 °C
**Input Low Current ($V_{IN} = V_{ILmin}$)	I_{IL}	0.5	—	170	μA	0° to 75 °C
Power Supply Current (All Inputs and Output Open)	I_{EE}	−200	—	—	mA	0° to 75 °C

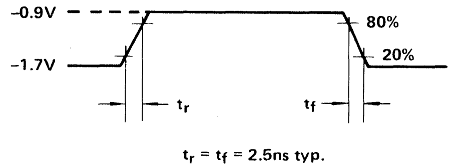
*$\bar{B}$ Input High Current = 300μA (max)
**$\bar{B}$ Input Low Current = 240μA (max)

AC CHARACTERISTICS

($V_{CC} = V_{CCO} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $T_A = 0°$ to $+75°C$ with transverse airflow ≥ 2.5 m/s, Output Load = 50Ω to −2V and 15 pF to GND, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS



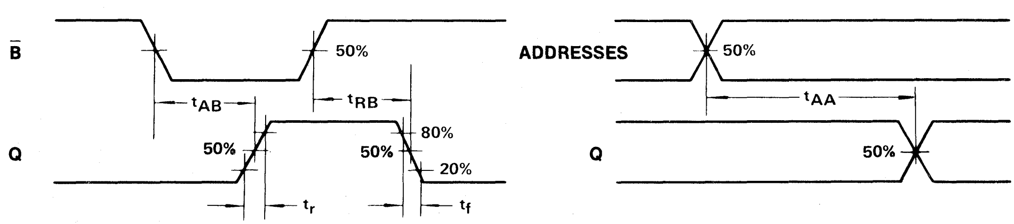


OUTPUT LOAD: $R_L = 50\Omega$
$C_L = 15$ pF
(INCLUDING JIG AND STRAY CAPACITANCE)

READ CYCLE

Parameter	Symbol	MB7072E			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}	—	—	12	ns
Block Select Access Time	t_{AB}	—	3.0	5.0	ns
Block Select Recovery Time	t_{RB}	—	3.0	5.0	ns

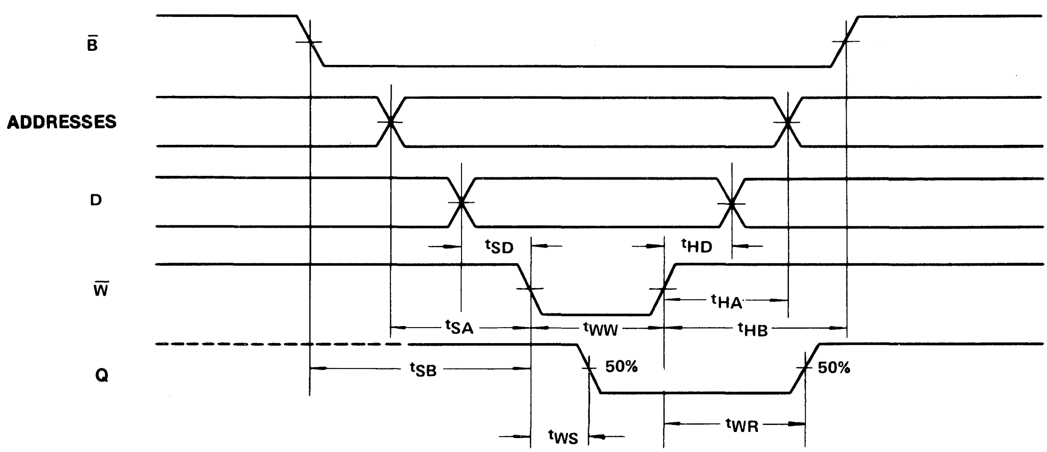
READ CYCLE



WRITE CYCLE

Parameter	Symbol	MB7072E			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	9.0	5.5	—	ns
Write Recovery Time	t_{WR}	—	6.0	9.0	ns
Write Disable Time	t_{WS}	—	3.0	5.0	ns
Address Set Up Time	t_{SA}	3.0	—	—	ns
Block Select Set Up Time	t_{SB}	2.0	—	—	ns
Data Set Up Time	t_{SD}	2.0	—	—	ns
Address Hold Time	t_{HA}	2.0	—	—	ns
Block Select Hold Time	t_{HB}	2.0	—	—	ns
Data Hold Time	t_{HD}	2.0	—	—	ns

WRITE CYCLE



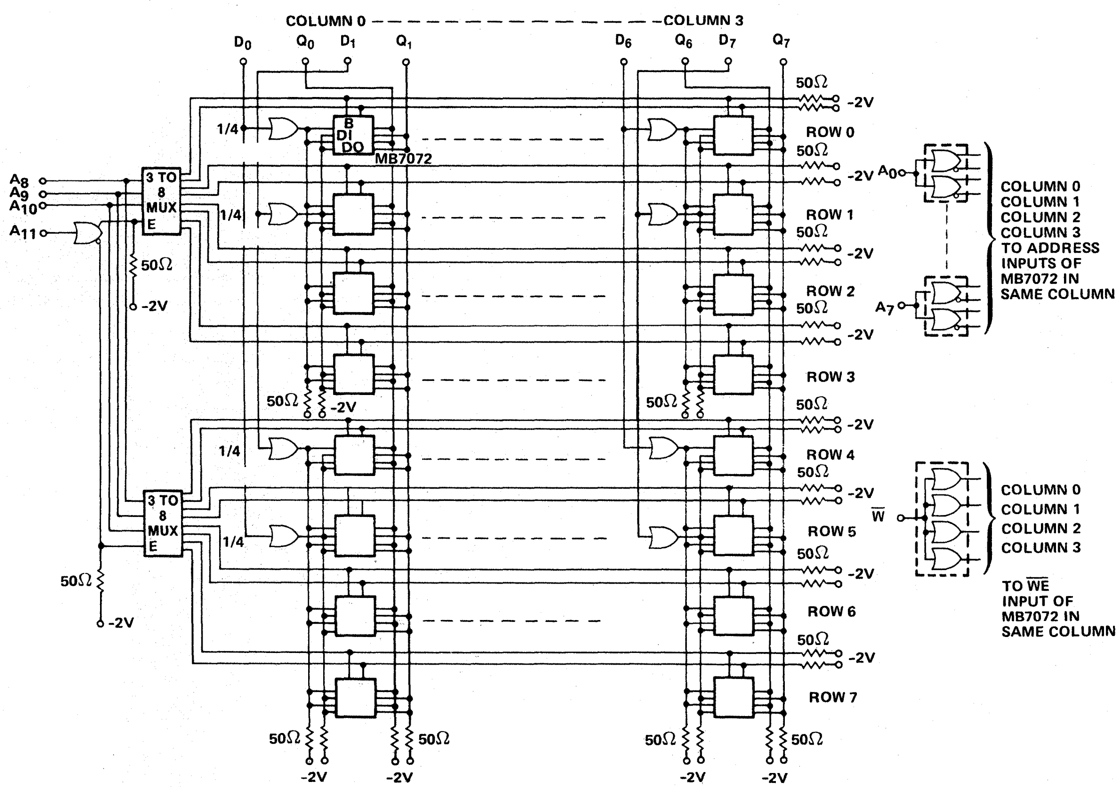
RISE TIME AND FALL TIME

Parameter	Symbol	MB7072E			Unit
		Min	Typ	Max	
Ouput Rise Time	t_r	—	3.0	—	ns
Output Fall Time	t_f	—	3.0	—	ns

APPLICATION INFORMATION

The Fujitsu MB7072E is a fully decoded 256 word by 4-bits ECL memory. High speed makes them ideally suited to mainframe applications, including cache and microprogram control. Figure 3 illustrates one application; a 4K word x 8-bit memory. As with all ECL memory systems, extreme care must be taken in PC board layout and bussing to minimize reflections and crosstalk.

Fig. 3 — 4K WORD X 8-BIT MEMORY SYSTEM



FUJITSU
MICROELECTRONICS, INC.

MBM10415AH

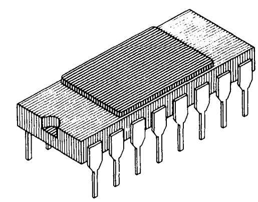
ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM10415AH is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. It is organized as 1024 words by one bit, and features on-chip voltage compensation for improved noise margin.

The MBM10415AH offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10415AH is specified over a temperature range of from 0 °C 75 °C (ambient). It also features frit-sealed 16-pin dual in-line packaging, and is fully compatible with industry-standard 10K-series ECL families.

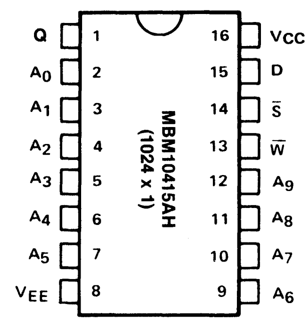


CERAMIC PACKAGE DIP-16C-F01

FEATURES

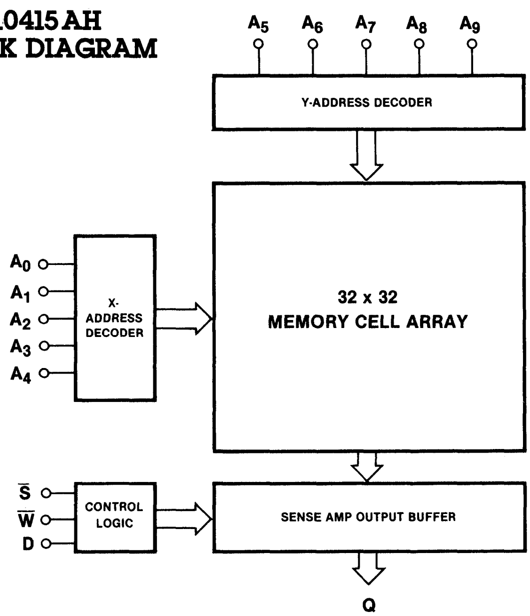
- **1024 words x 1-bit organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time: MBM10415AH: 20 ns Max.**
- **Chip select access time: MBM10415AH: 8 ns Max.**
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.5mW/bit**
- **DOPOS and IOP processing**
- **Pin compatible with F10415 and MCM10146**

PIN ASSIGNMENT



*V_{CC} grounded

MBM10415 AH BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	L	L	WRITE"L"
L	L	H	L	WRITE"H"
L	H	X	D_{OUT}	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0 °C to +75 °C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	5	pF
Output Pin Capacitance	C_{OUT}	—	7	8	pF

DC CHARACTERISTICS

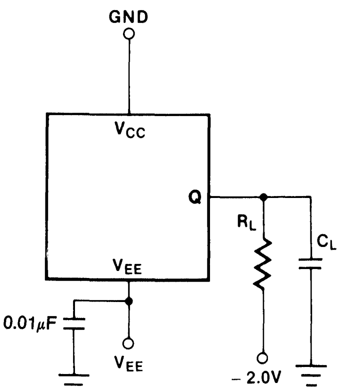
(V_{CC} = 0V, V_{EE} = −5.2V, Output load = 50Ω to −2.0V and Airflow ≥ 2.5 m/s unless otherwise noted.)

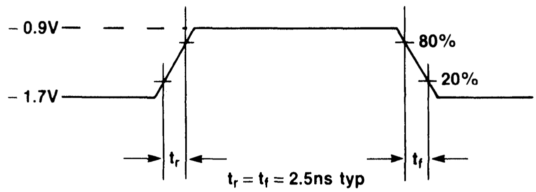
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 − 960 − 900	—	− 840 − 810 − 720	mV	0 °C 25 °C 75 °C
Output Low Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0 °C 25 °C 75 °C
Output High Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 − 980 − 920	—	—	mV	0 °C 25 °C 75 °C
Output Low Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0 °C 25 °C 75 °C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	− 840 − 810 − 720	mV	0 °C 25 °C 75 °C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0 °C 25 °C 75 °C
Input High Current ($V_{IN} = V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75 °C
Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75 °C
$\overline{S}$ Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75 °C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−125 −150	—	—	mA	75 °C 0 °C

AC CHARACTERISTICS

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pf to GND and Airflow ≥ 2.5 m/s unless otherwise noted.)

AC TEST CONDITIONS





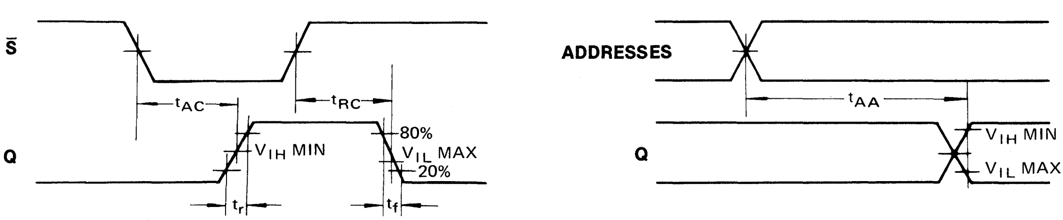
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM10415AH Typ	Max	Unit
Address Access Time	t_{AA}	13	20	ns
Chip Select Access Time	t_{AC}	5	8	ns
Chip Select Recovery Time	t_{RB}	5	8	ns

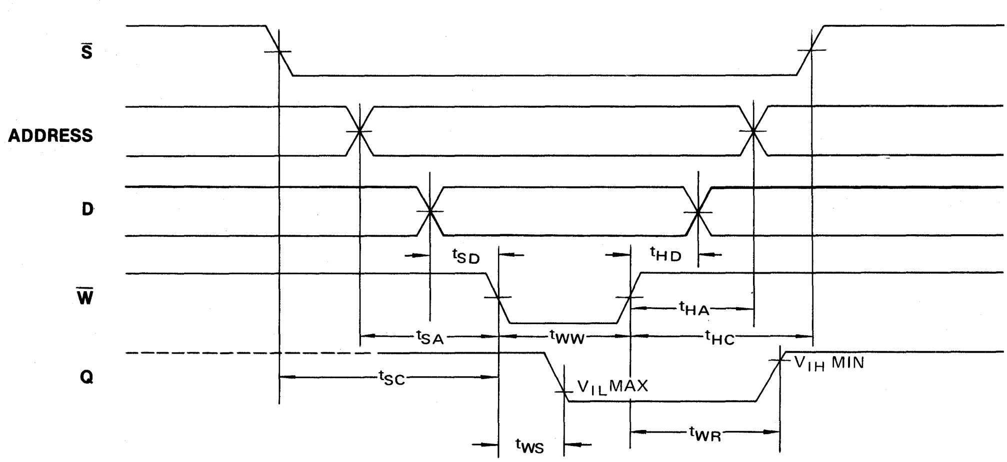
READ CYCLE



WRITE CYCLE

Parameter	Symbol	MBM10415AH			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	14	9	—	ns
Write Disable Time	t_{WS}	—	5	10	ns
Write Recovery Time	t_{WR}	—	5	10	ns
Address Set Up Time	t_{SA}	5	3	—	ns
Chip Select Set Up Time	t_{SC}	4	0	—	ns
Data Set Up Time	t_{SD}	4	0	—	ns
Address Hold Time	t_{HA}	3	0	—	ns
Chip Select Hold Time	t_{HC}	4	0	—	ns
Data Hold Time	t_{HD}	4	0	—	ns

WRITE CYCLE

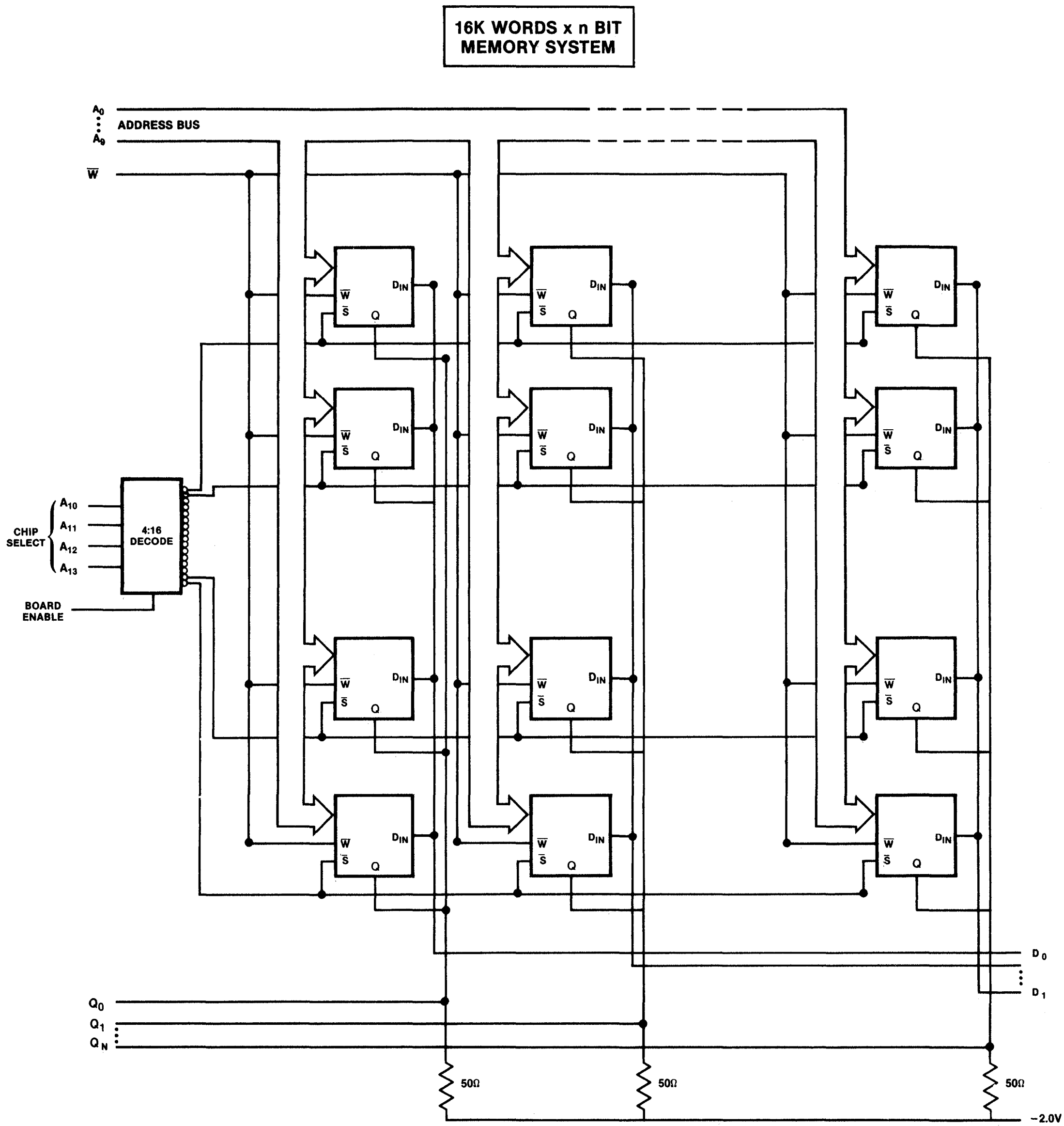


RISE TIME AND FALL TIME

Parameter	Symbol	MBM10415AH			Unit
		Min	Typ	Max	
Output Rise Time	t_r	—	5	—	ns
Output Fall Time	t_f	—	5	—	ns

APPLICATIONS INFORMATION

LARGE SYSTEM APPLICATION



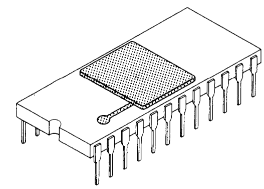
ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM10422 is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4-bits and features on-chip voltage compensation for improved noise margin.

The MBM10422 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for MBM10422 is specified over a temperature range of 0° to 75°C (ambient). It features metal sealed 24-pin dual in-line packaging, and is fully compatible with industry standard 10K-series ECL families.

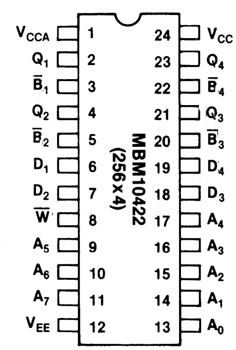


CERAMIC PACKAGE
DIP-24C-A02

FEATURES

- 256 words x 4-bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time: 10ns max.
- Block select access time: 5ns max.
- Open emitter output for easy memory expansion
- Power dissipation of 0.7 mW/bit
- DOPOS and IOP processing
- Pin compatible with F10422

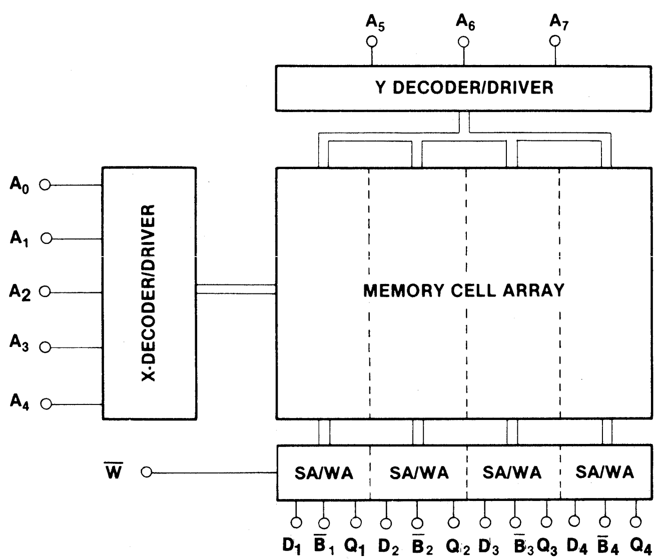
PIN ASSIGNMENT



*V_{CC} Grounded

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid appliction of any voltage higher than maximum rated voltages to this device.

BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\bar{B}$	$\overline{W}$	DI		
H	X	X	L	DISABLED
L	L	H	L	WRITE"H"
L	L	L	L	WRITE"L"
L	H	X	DO	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

DC CHARACTERISTICS

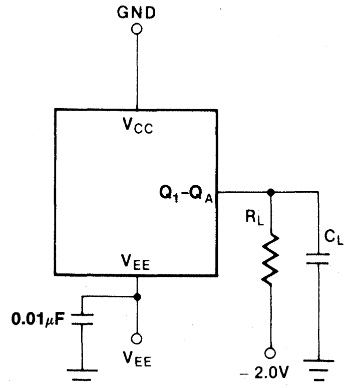
(V_{CC} = 0V, V_{EE} = −5.2V, Output load = 50Ω to −2.0V and Airflow ≥ 2.5 m/s unless otherwise noted.)

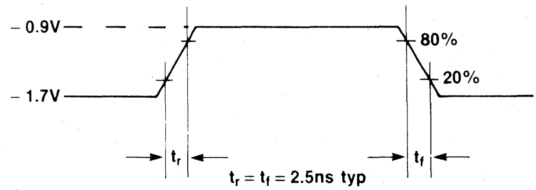
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 −960 −900	—	−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 −980 −920	—	—	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{W}$ Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−180	—	—	mA	0° to 75°C

AC CHARACTERISTICS

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥ 2.5m/s unless otherwise noted.)

AC TEST CONDITIONS





$t_r = t_f = 2.5$ns typ

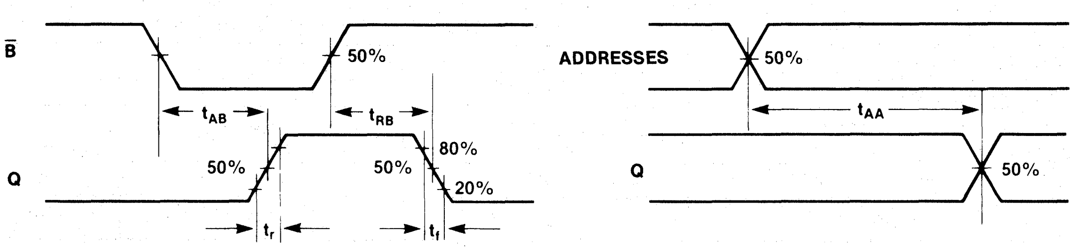
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	—	10	ns
Block Select Access Time	t_{AB}	—	—	5	ns
Block Select Recovery Time	t_{RB}	—	—	5	ns

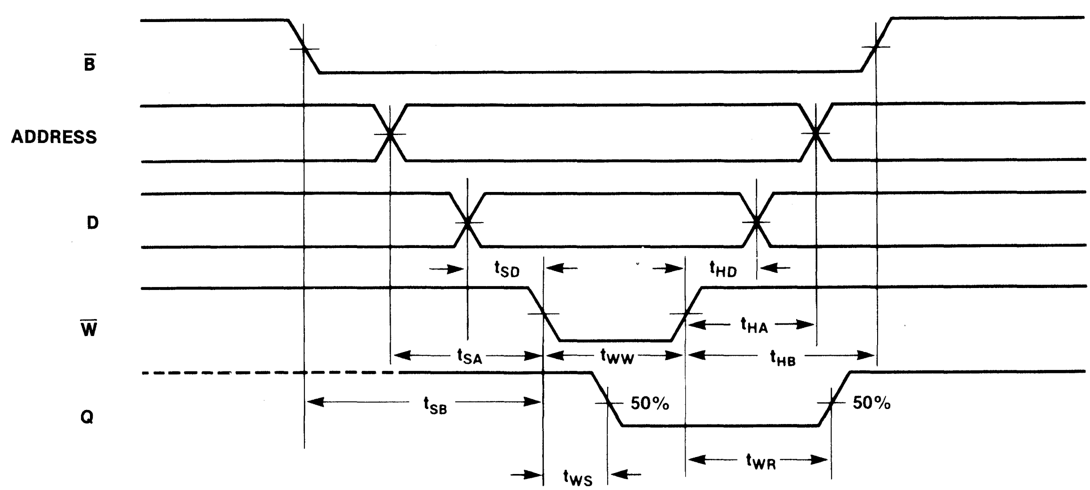
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	7	—	—	ns
Write Disable Time	t_{WS}	—	—	5	ns
Write Recovery Time	t_{WR}	—	—	10	ns
Address Set Up Time	t_{SA}	1	—	—	ns
Block Select Set Up Time	t_{SB}	1	—	—	ns
Data Set Up Time	t_{SD}	1	—	—	ns
Address Hold Time	t_{HA}	2	—	—	ns
Block Select Set Up Time	t_{HB}	2	—	—	ns
Data Hold Time	t_{HD}	2	—	—	ns

WRITE CYCLE TIMING DIAGRAM

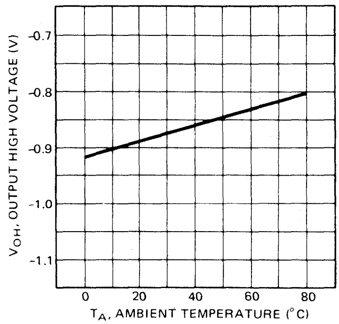


RISE TIME AND FALL TIME

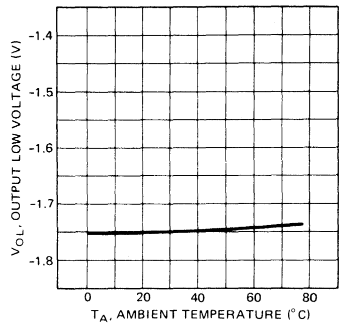
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	2	—	ns
Output Fall Time	t_f	—	2	—	ns

TYPICAL CHARACTERISTICS CURVES

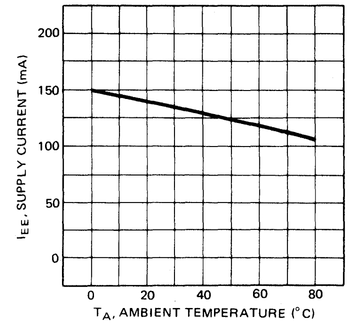
OUTPUT HIGH VOLTAGE
vs AMBIENT TEMPERATURE



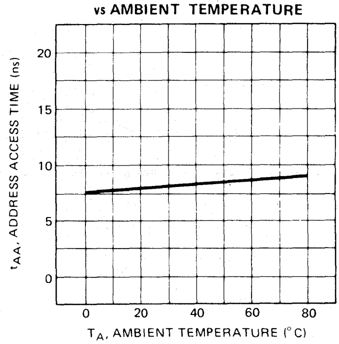
OUTPUT LOW VOLTAGE
vs AMBIENT TEMPERATURE



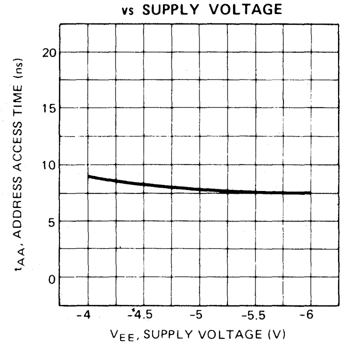
SUPPLY CURRENT
vs AMBIENT TEMPERATURE



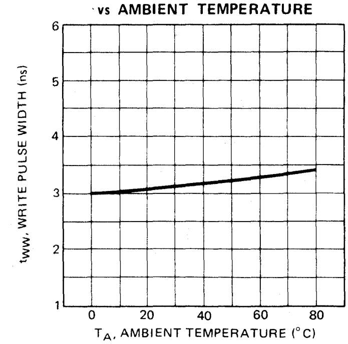
ADDRESS ACCESS TIME
vs AMBIENT TEMPERATURE



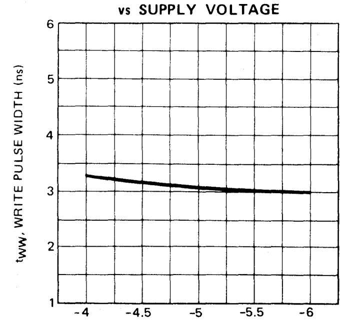
ADDRESS ACCESS TIME
vs SUPPLY VOLTAGE



WRITE PULSE WIDTH
vs AMBIENT TEMPERATURE



WRITE PULSE WIDTH
vs SUPPLY VOLTAGE



FUJITSU
MICROELECTRONICS, INC.

MBM10422A-7

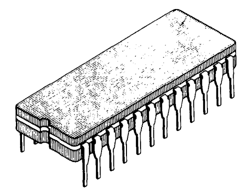
ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

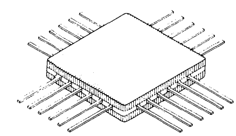
The Fujitsu MBM10422A is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4-bits and features on-chip voltage compensation for improved noise margin.

The MBM10422A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for MBM10422A is specified over a temperature range of 0°C to 75°C (T_A for DIP, T_C for flat package). It features cerdip 24-pin dual in-line and flat packaging, and is fully compatible with industry standard 10K-series ECL families.



CERDIP PACKAGE
DIP-24C-C05

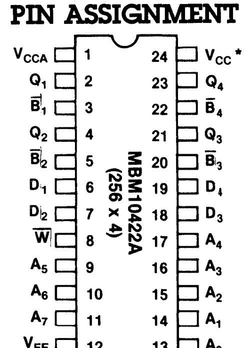


FLAT PACKAGE
FPT-24C-C02

FEATURES

- **256 words x 4-bits organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time: 7ns max.**
- **Block select access time: 5ns max.**
- **Open emitter output for easy memory expansion**
- **Power dissipation of 0.7 mW/bit**
- **DOPOS and IOP-II processing**
- **Pin compatible with F10422**

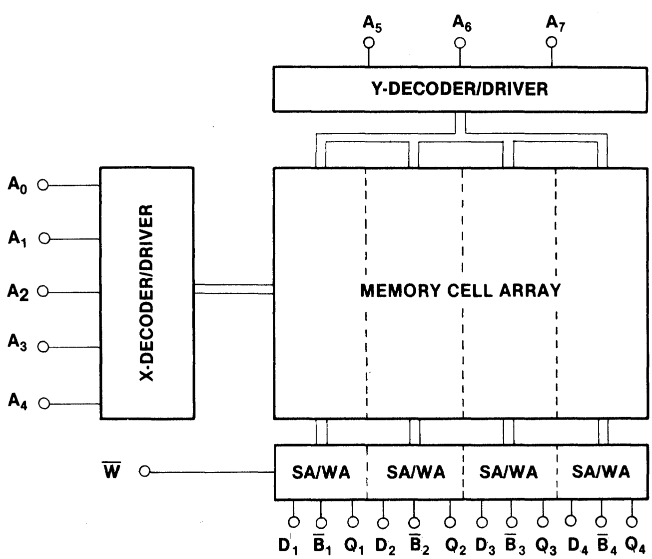
PIN ASSIGNMENT



$^*V_{CC}$ Grounded

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoidappliction of any voltage higher than maximum rated voltages to this device.

MBM10422 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{B}$	$\overline{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE"H"
L	L	L	L	WRITE"L"
L	H	X	DOUT	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Temperature*
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

* Ambient Temperature for DIP, case temperature for flat package

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	5	pF
Output Pin Capacitance	C_{OUT}	—	6	8	pF

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V, Output load = 50Ω to −2.0V, T_A = 0°C to 75°C for DIP, T_C = 0°C to 75°C for flat package, and Airflow = ≥ 25 m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 −960 −900	—	−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 −980 −920	—	—	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{B}$ Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA	0° to 75°C

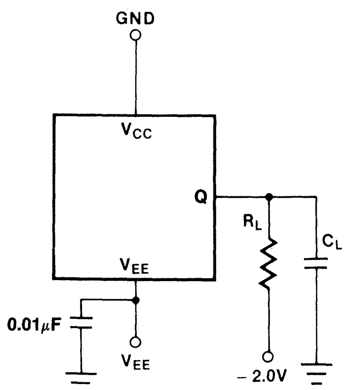
FUNCTIONAL DESCRIPTION

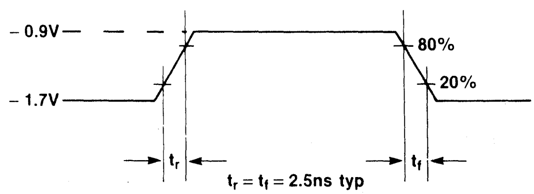
The Fujitsu MBM10422A-7 is fully decoded 1024-bit read/write random access memory organized as 256 words by 4-bits. Memory cell selection is achieved by means of a 8-bit address designated $A_0 \sim A_7$. The active low Block Select $\overline{B}$ input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{W}$ input. With $\overline{W}$ and $\overline{B}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{B}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

AC CHARACTERISTICS

Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, T_C = 0°C to 75°C for flat package, and Airflow = ≥ 25 m/s, unless otherwise noted.

AC TEST CONDITIONS





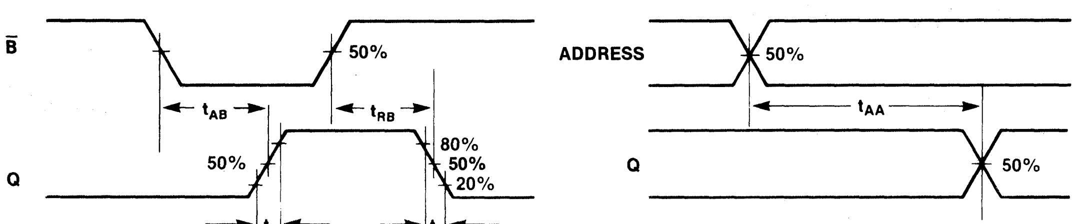
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	5	7	ns
Block Select Access Time	t_{AB}	—	2.5	4	ns
Block Select Recovery Time	t_{RB}	—	2.5	4	ns

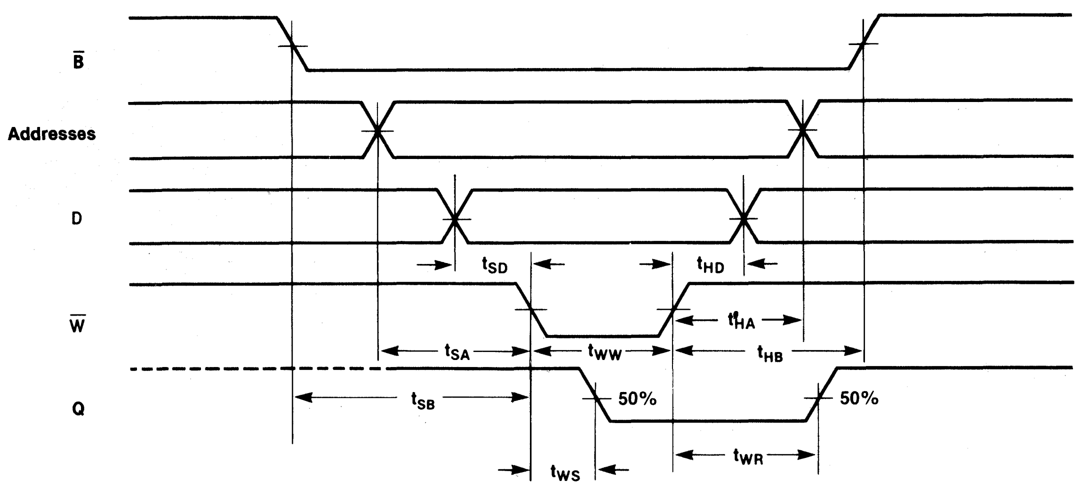
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	5	—	—	ns
Write Disable Time	t_{WS}	—	—	4	ns
Write Recovery Time	t_{WR}	—	—	8	ns
Address Set Up Time	t_{SA}	1	—	—	ns
Block Select Set Up Time	t_{SB}	1	—	—	ns
Data Set Up Time	t_{SD}	1	—	—	ns
Address Hold Time	t_{HA}	1	—	—	ns
Block Select Hold Time	t_{HB}	1	—	—	ns
Data Hold Time	t_{HD}	1	—	—	ns

WRITE CYCLE

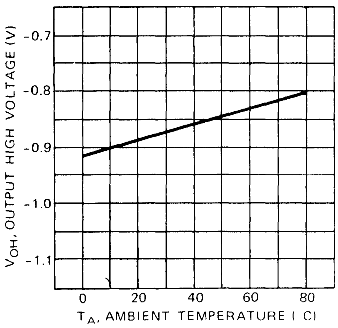


RISE TIME AND FALL TIME

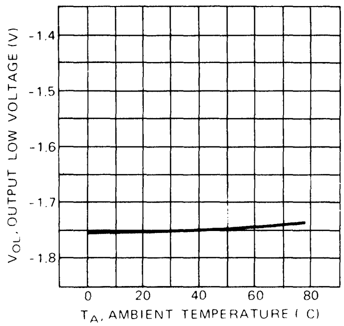
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	1.5	—	ns
Output Fall Time	t_f	—	1.5	—	ns

TYPICAL CHARACTERISTICS CURVES

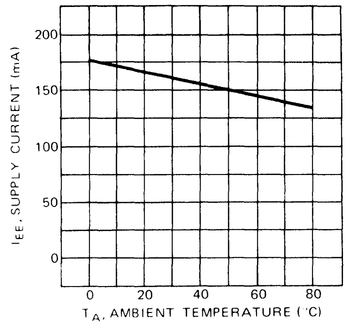
OUTPUT HIGH VOLTAGE
vs AMBIENT TEMPERATURE



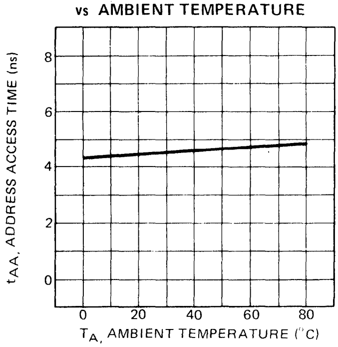
OUTPUT LOW VOLTAGE
vs AMBIENT TEMPERATURE



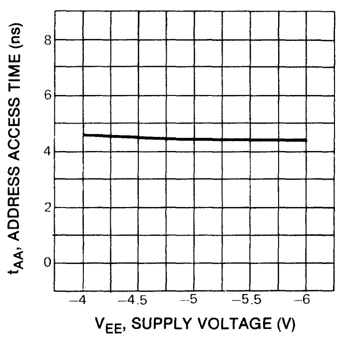
SUPPLY CURRENT
vs AMBIENT TEMPERATURE



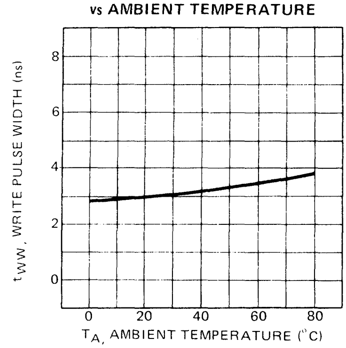
ADDRESS ACCESS TIME
vs AMBIENT TEMPERATURE



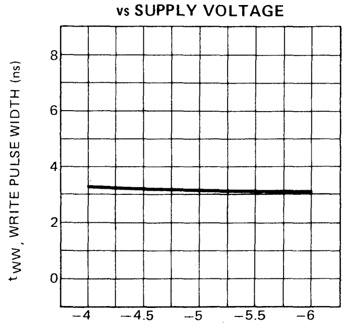
ADDRESS ACCESS TIME
vs SUPPLY VOLTAGE



WRITE PULSE WIDTH
vs AMBIENT TEMPERATURE



WRITE PULSE WIDTH
vs SUPPLY VOLTAGE



Preliminary

Bipolar Memories

FUJITSU

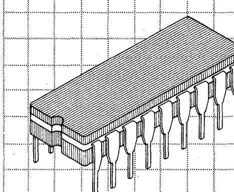
MBM10470A-10
ECL 4096-Bit Bipolar Random Access Memory

Description

The Fujitsu MBM10470A-10 is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage compensation for improved noise margin.

The MBM10470A-10 offers extremely small cell and chip size, achieved through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10470A-10 is specified over a temperature range of from 0° to 75°C (ambient). It also features 18-pin dual-in-line ceramic packaging, and is fully compatible with industry-standard 10K-series ECL families.

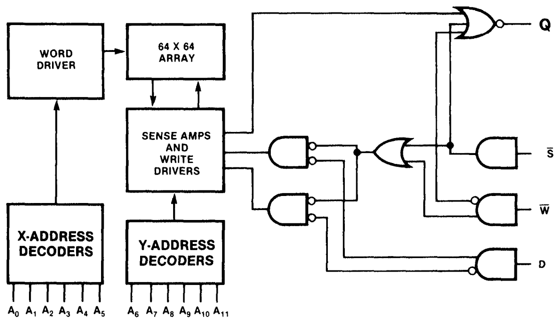


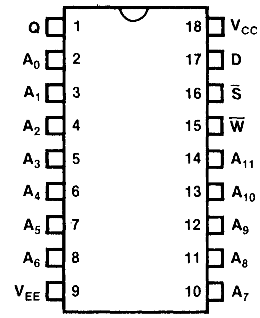
Ceramic Package
DIP-18C-C01

Features

- 4096 words x 1-bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address Access Time: 10 ns max.
- Chip Select Access Time: 6 ns max.
- Open emitter output for ease of memory expansion
- Low Power Dissipation: 0.22mW/bit
- DOPOS and IOP II processing
- Pin compatible with the F10470

MBM10470A Block Diagram and Pin Assignment





*V_{CC} grounded

Truth Table

Input $\overline{S}$	$\overline{W}$	D_{IN}	Q	Mode
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level L = Low Voltage Level X = Don't care

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in operational sections of this data sheet. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therfore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

Functional Description

The Fujitsu MBM10470A-10 is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated $A_0 \sim A_{11}$. The active low Chip Select $\overline{S}$ input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{W}$ input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

DC Characteristics

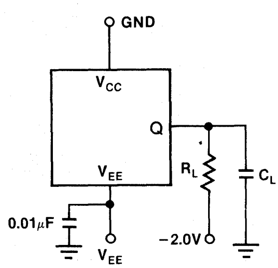
($V_{CC} = 0V$, $V_{EE} = -5.2V$, Output Load = 50Ω and 30 pF to −2.0V, $T_A = 0°C$ to 75°C, Airflow ≥ 2.5 m/s, unless otherwise noted.)

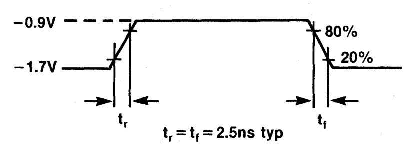
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\bar{S}$ Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	−200			mA	0°C to 75°C

AC Characteristics

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30 pF to GND, $T_A = 0°C$ to 75°C and Airflow ≥ 2.5 m/s unless otherwise noted.)

Figure 2—AC Test Conditions





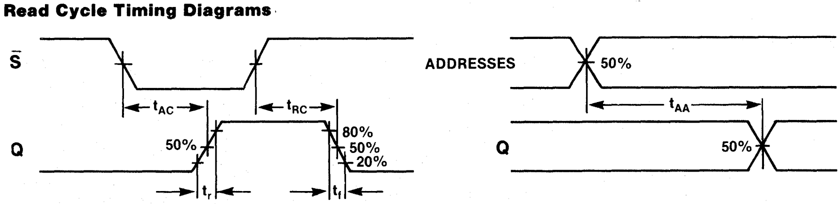
Output Load: $R_L = 50Ω$
$C_L = 30pF$
(including jig and stray capacitance)

Note: All timing measurements referenced to 50% input levels.

Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	—	10	ns
Chip Select Access Time	t_{AC}	—	—	6	ns
Chip Select Recovery Time	t_{RC}	—	—	6	ns

Read Cycle Timing Diagrams

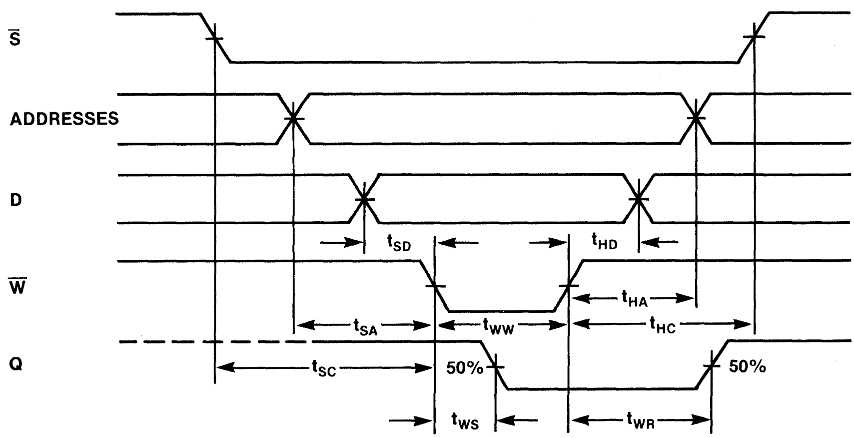


AC Characteristics
(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30 pF to GND, $T_A = 0°C$ to 75°C and Airflow ≥ 2.5 m/s unless otherwise noted.)

Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	12	—	—	ns
Write Disable Time	t_{WS}	—	—	6	ns
Write Recovery Time	t_{WR}	—	—	10	ns
Address Set Up Time	t_{SA}	1	0	—	ns
Chip Select Set Up Time	t_{SC}	1	0	—	ns
Data Set Up Time	t_{SD}	1	0	—	ns
Address Hold Time	t_{HA}	2	0	—	ns
Chip Select Hold Time	t_{HC}	2	0	—	ns
Data Hold Time	t_{HD}	2	0	—	ns

Write Cycle Timing Diagram



Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	1.5	—	ns
Output Fall Time	t_f	—	1.5	—	ns

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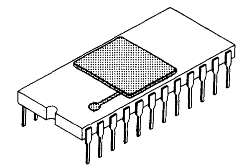
ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM10474 is a fully decoded 4096-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications.

The MBM10474 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10474 is specified over a temperature range of 0°C to 75°C (ambient). It features 24-pin dual in-line ceramic packaging and is fully compatible with industry-standard 10K-series ECL families.

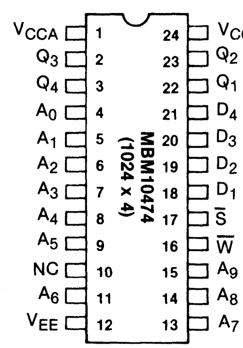


CERAMIC PACKAGE
DIP-24C-A02

FEATURES

- 1024 words x 4-bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time:
  15ns Max.
  11ns Typ.
- Chip select time:
  8ns Max.
  4ns Typ.
- Open emitter output for easy memory expansion
- Low power dissipation:
  0.2mW/bit
- DOPOS and IOP processing
- Pin compatible with F10474

PIN ASSIGNMENT

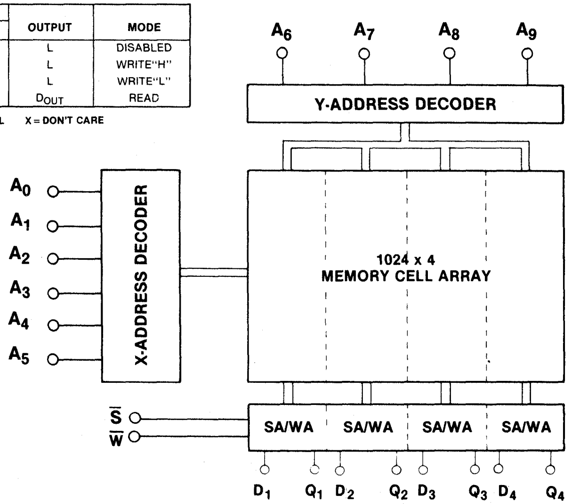


MBM10474 BLOCK DIAGRAM

TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE"H"
L	L	L	L	WRITE"L"
L	H	X	D_{OUT}	READ

H = HIGH VOLTAGE LEVEL X = DON'T CARE
L = LOW VOLTAGE LEVEL



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	6	pF
Output Pin Capacitance	C_{OUT}	—	6	8	pF

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V , Output load = 50Ω to −2.0V and Airflow ≥ 2.5m/s unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 −960 −900	—	−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 −980 −920	—	—	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{S}$ Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA	0° to 75°C

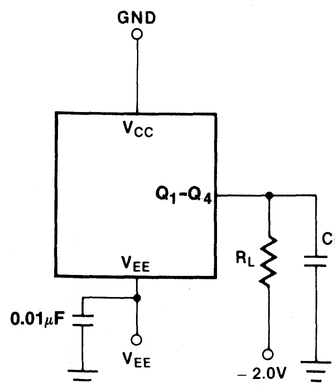
FUNCTIONAL DESCRIPTION

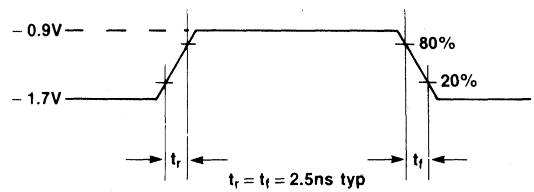
The Fujitsu MBM10474 is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4-bits. Memory cell selection is achieved by means of a 10-bit address designated $A_0 \sim A_9$. The active low Chip Select $\overline{S}$ input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{W}$ input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

AC CHARACTERISTICS

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥ 2.5m/s unless otherwise noted.)

AC TEST CONDITIONS





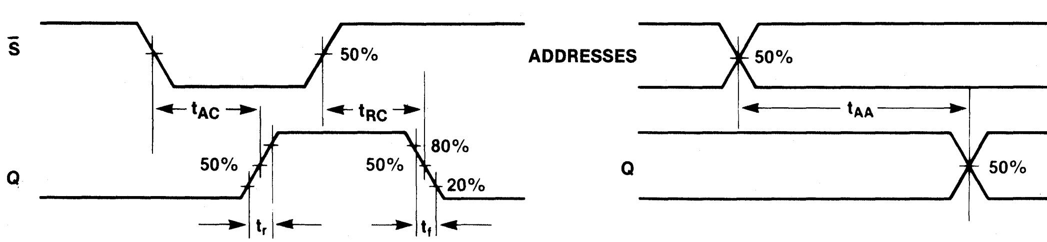
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	11	15	ns
Chip Select Access Time	t_{AC}	—	4	8	ns
Chip Select Recovery Time	t_{RC}	—	4	8	ns

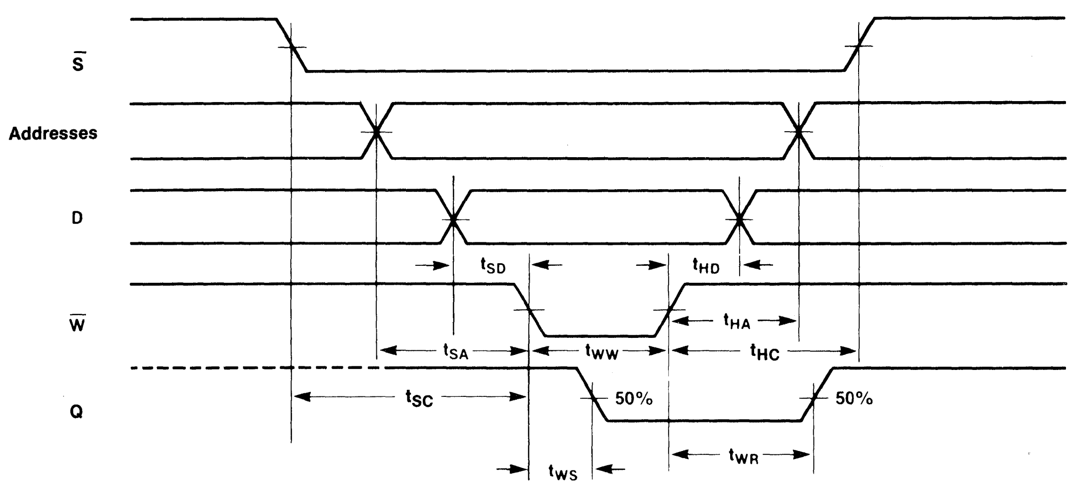
READ CYCLE



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	15	—	—	ns
Write Disable Time	t_{WS}	—	—	8	ns
Write Recovery Time	t_{WR}	—	—	8	ns
Address Set Up Time	t_{SA}	2	—	—	ns
Chip Select Set Up Time	t_{SC}	2	—	—	ns
Data Set Up Time	t_{SD}	2	—	—	ns
Address Hold Time	t_{HA}	3	—	—	ns
Chip Select Hold Time	t_{HC}	2	—	—	ns
Data Hold Time	t_{HD}	2	—	—	ns

WRITE CYCLE



RISE TIME AND FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	1.5	2	5	ns
Output Fall Time	t_f	1.0	2	5	ns

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MBM10480-25

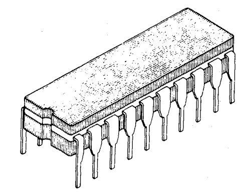
ECL 16,384-BIT BIPOLAR RANDOM ACCESS MEMORY

PRELIMINARY
Note: This is not a final specification. Some parametric limits are subject to change.

DESCRIPTION

The Fujitsu MBM10480 is a fully decoded 16,384-bit ECL read/write random access memory designed for main frame memory, control and buffer storage applications. This device is organized as 16,384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

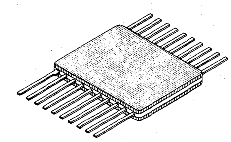
Operation for the MBM10480 is specified over a temperature range of 0 °C to 75 °C (T_A for DIP, T_C for flat package). It features cerdip 20-pin dual in-line and flat packaging, and is fully compatible with industry-standard 10K-series ECL families.



CERDIP PACKAGE
DIP-20C-C03

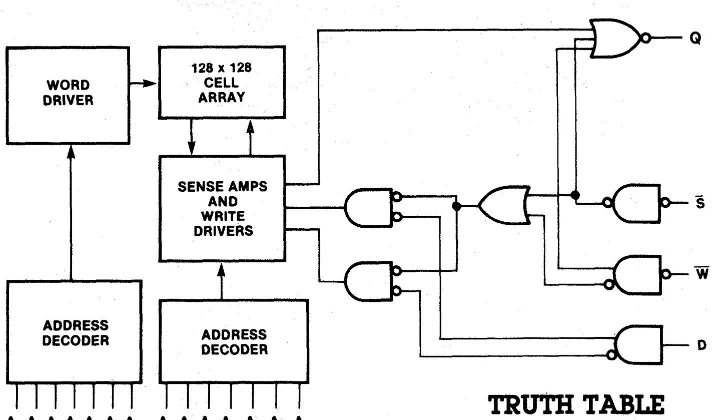
FEATURES

- **Organized as 16,384 x 1**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address Access Time: 25 ns max.**
- **Chip select access time: 15 ns max.**
- **Open emitter output for easy memory expansion**
- **Low power dissipation of 0.05 mW/bit**
- **DOPOS processing (Doped Polysilicon)**
- **Pin compatible with the F10480**

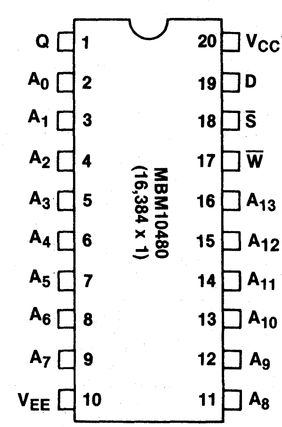


FLATPACK
FPT-20C-C01

MBM10480 BLOCK DIAGRAM



PIN ASSIGNMENT



*V_{CC} grounded

TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't care

Note: This is not a final specification.
Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS (See Note)

Parameter		Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})		V_{EE}	+0.5 to −7.0	V
Input Voltage		V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)		I_{OUT}	−30	mA
Temperature Under Bias	DIP	T_A	−55 to +125	°C
	Flat	T_C		
Storage Temperature		T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

GUARANTEED OPERATING CONDITIONS (Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Temperature*
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

* Ambient Temperature for DIP, case temperature for flat package

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	5	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω and 30 pF to −2.0V, T_A = 0°C to 75°C for DIP, T_C=0°C to 75°C for Flat package and Airflow ≥ 2.5 m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OH}	−1000 − 960 − 900	—	− 840 − 810 − 720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OHC}	−1020 − 980 − 920	—	—	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	− 840 − 810 − 720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\,max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current (V_{IN} = $V_{IL\,min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{S}$ Input Low Current (V_{IN} = $V_{IL\,min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA	0° to 75°C

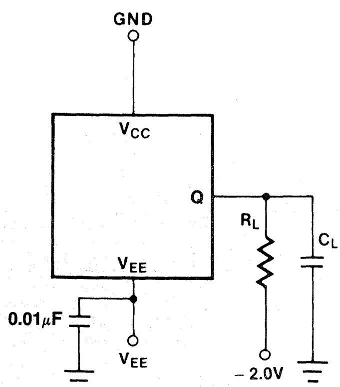
FUNCTIONAL DESCRIPTION

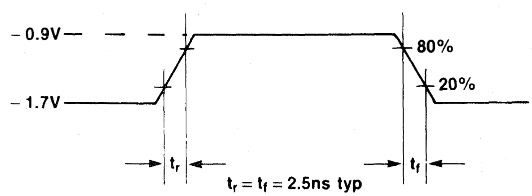
The Fujitsu MBM10480 is a fully decoded 16,384-bit read/write random access memory organized as 16,384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated $A_0 \sim A_{13}$. The active low Chip Select $\overline{S}$ input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{W}$ input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

AC CHARACTERISTICS

($V_{CC} = 0V$, Output Load = 50Ω to −2.0V and 30pF to GND, $T_A = 0°C$ to 75°C for DIP, $T_C = 0°C$ to 75°C for flat package, and Airflow = ≥ 25 m/s, unless otherwise noted.)

AC TEST CONDITIONS





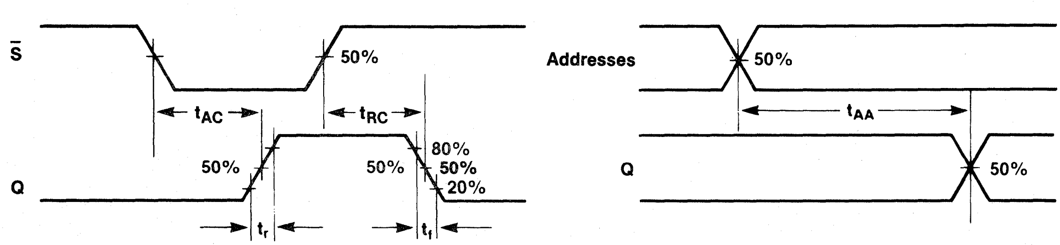
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	—	25	ns
Chip Select Access Time	t_{AC}	—	—	15	ns
Chip Select Recovery Time	t_{RC}	—	—	15	ns

READ CYCLE TIMING DIAGRAMS



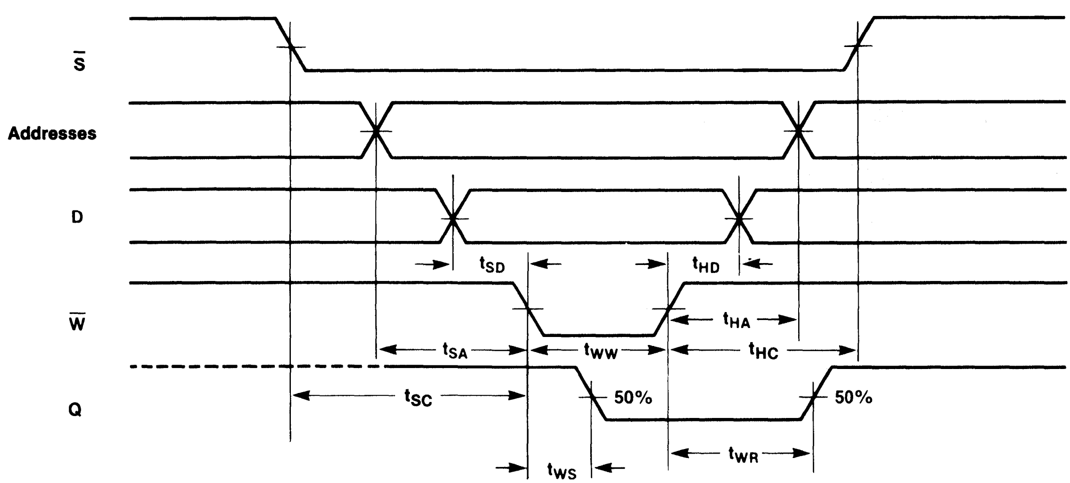
PRELIMINARY

Note: This is not a final specification.
Some parametric limits are subject to change.

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	25	—	—	ns
Write Disable Time	t_{WS}	—	—	15	ns
Write Recovery Time	t_{WR}	—	—	20	ns
Address Set Up Time	t_{SA}	5	—	—	ns
Chip Select Set Up Time	t_{SC}	5	—	—	ns
Data Set Up Time	t_{SD}	5	—	—	ns
Address Hold Time	t_{HA}	5	—	—	ns
Chip Select Hold Time	t_{HC}	5	—	—	ns
Data Hold Time	t_{HD}	5	—	—	ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME AND FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	3	—	ns
Output Fall Time	t_f	—	3	—	ns

TTL 576-BIT BIPOLAR RANDOM ACCESS MEMORY

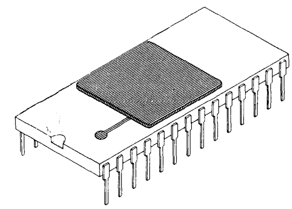
DESCRIPTION

The Fujitsu MBM93419 is a high speed TTL read/write random-access memory, organized as 64 words by 9 bits, with open-collector outputs.

MBM93419 is packaged in a 28-pin dual-in-line package, and is plug-in replaceable with F93419. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and the number of required bits per word is relatively large. The ninth bit can provide parity for 8-bit word systems.

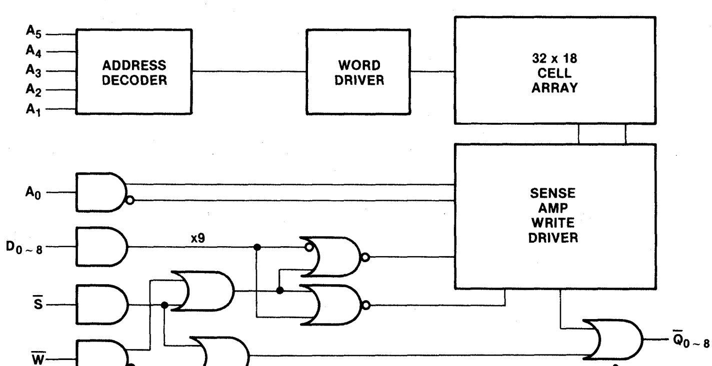
FEATURES

- **Organization:**
  64 words x 9-bits
- **+5V Single Power Supply**
- **TTL Inputs and Outputs**
- **Open Collector Outputs**
- **Address Access Time:**
  45 ns Max.
- **Chip Select Access Time:**
  40 ns Max.
- **Power Dissipation:**
  1.3mW/bit Typ.
- **Compatible with F93419**

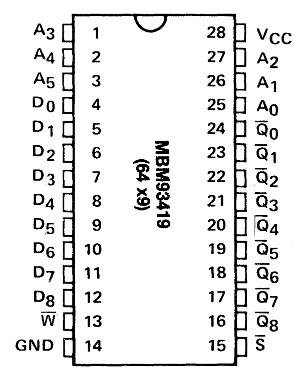


CERAMIC PACKAGE
DIP-28C-A01

MBM93419 BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D		
H	X	X	H	DISABLED
L	L	H	H	WRITE "H"
L	L	L	H	WRITE "L"
L	H	X	$\overline{D_{OUT}}$	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE
*DATA OUTPUT IS THE COMPLEMENT OF DATA INPUT

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this device.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage (DC)	V_{IN}	−0.5 to +5.5	V
Input Current (DC)	I_{IN}	−12.0 to +5.0	mA
Output Voltage (V_{OUT} = "H")	V_{OUT}	−0.5 to +5.5	V
Output Current (DC, V_{OUT} = "L")	I_{OUT}	+20.0	mA
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

GUARANTEED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0° C to +75° C
Input High Voltage	V_{IH}	2.1	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.8	V	

CAPACITANCE

(T_A = 25 °C, V_{CC} = 5.0V, V_{IN} = 2.0V, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	—	5.0	pF
Output Pin Capacitance	C_{OUT}	—	—	8.0	pF

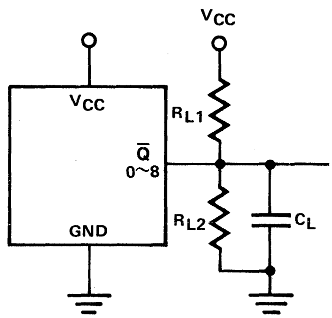
DC CHARACTERISTICS

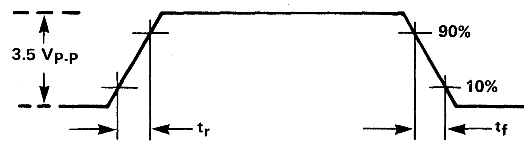
(V_{CC} = 5V ±5%, T_A = 0 °C to 75 °C, Air Flow ≥ 2.5m/sec, After Warm-up ≥ 2 min.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Low Voltage	V_{OL}	V_{CC} = Min, I_{OL} = 12mA	—	0.4	0.5	V
Input High Voltage	V_{IH}	—	—	1.6	—	V
Input Low Voltage	V_{IL}	—	—	1.5	—	V
Input Low Current	I_{IL}	V_{CC} = Max, V_{IN} = 0.4V	—	-250	-400	μA
Input High Current	I_{IH1}	V_{CC} = Max, V_{IN} = 4.5V	—	1.0	40	μA
Input High Current	I_{IH2}	V_{CC} = Max, V_{IN} = 5.25V	—	—	1.0	mA
Output Leakage Current	I_{CEX}	V_{CC} = Max, V_{OUT} = 4.5V	—	1.0	100	μA
Input Clamp Diode Voltage	V_{CD}	V_{CC} = Max, V_{OUT} = 4.5V	—	-1.0	-1.5	V
Power Supply Current	I_{CC}	V_{CC} = Max, T_A = 25° C All Input GND	—	160	200	mA

AC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 75°C, Air Flow ≥ 2.5 m/sec, After Warm-up ≥ 2 min.)



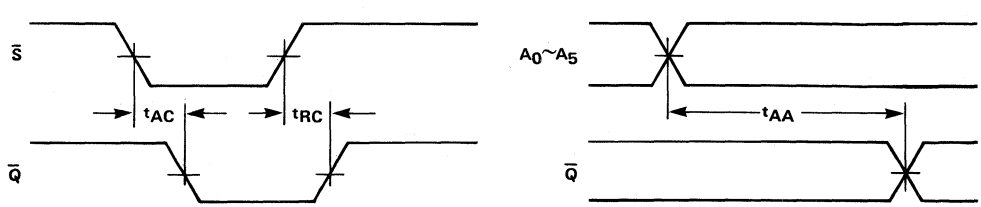


Input Pulse Voltage: 3.5V_{P-P}
Input Pulse Rise and Fall Time: 10ns
Output Load: R_{L1} = 450Ω
R_{L2} = 750Ω
C_L = 30pF (Including Jig)
Timing Measurement Levels: Input = 1.5V
Output = 1.5V

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	26	45	ns
Chip Select Access Time	t_{AC}	—	18	40	ns
Chip Select Recovery Time	t_{RC}	—	18	40	ns

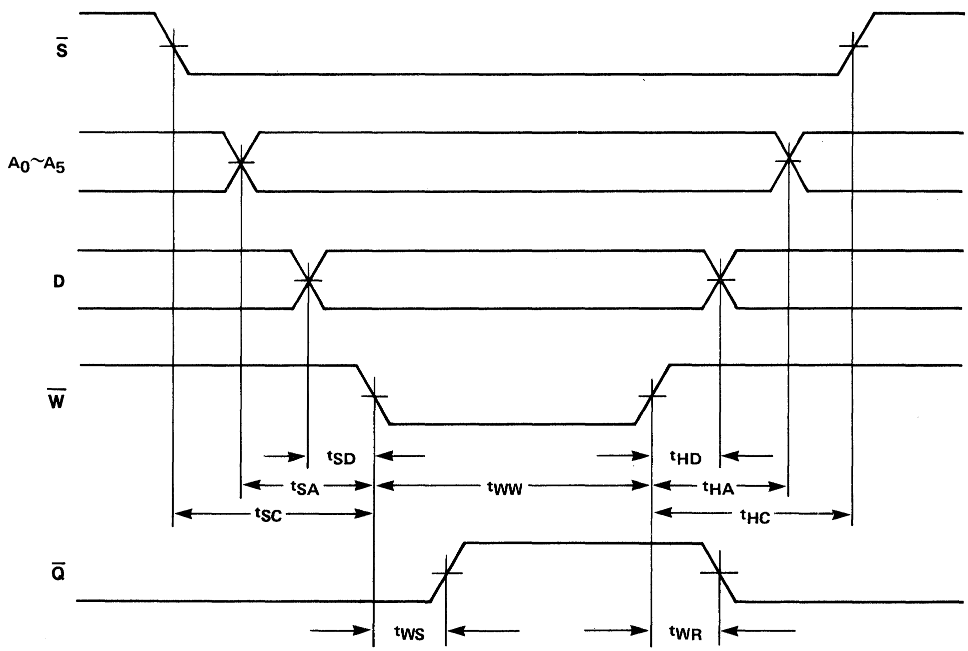
READ CYCLE



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	35	7	—	ns
Write Recovery Time	t_{WR}	—	20	45	ns
Write Delayed Time	t_{WS}	—	20	40	ns
Address Setup Time	t_{SA}	5	0	—	ns
Chip Select Setup Time	t_{SC}	5	0	—	ns
Data Setup Time	t_{SD}	5	0	—	ns
Address Hold Time	t_{HA}	5	0	—	ns
Chip Select Hold Time	t_{HC}	5	0	—	ns
Data Hold Time	t_{HD}	5	0	—	ns

WRITE CYCLE



MBM100422A-7

PRELIMINARY

Note: This is not a final specification. Some parametric limits are subject to change.

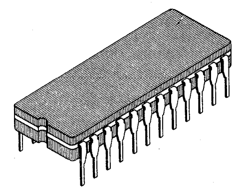
ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

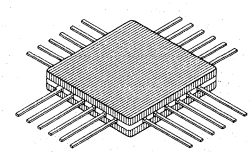
The Fujitsu MBM100422A is a fully decoded 1024-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4-bits, and it features on-chip voltage compensation for improved noise margin.

The MBM100422A offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM100422A-7 is specified over a temperature range of 0 °C to 85 °C (T_A for DIP, T_C for flat). It features cerdip 24-pin dual in-line or flat packaging, and is fully compatible with industry-standard 100K-series ECL families.



CERDIP PACKAGE
DIP-24C-C05



FLAT PACKAGE
FPT-24C-C02

FEATURES

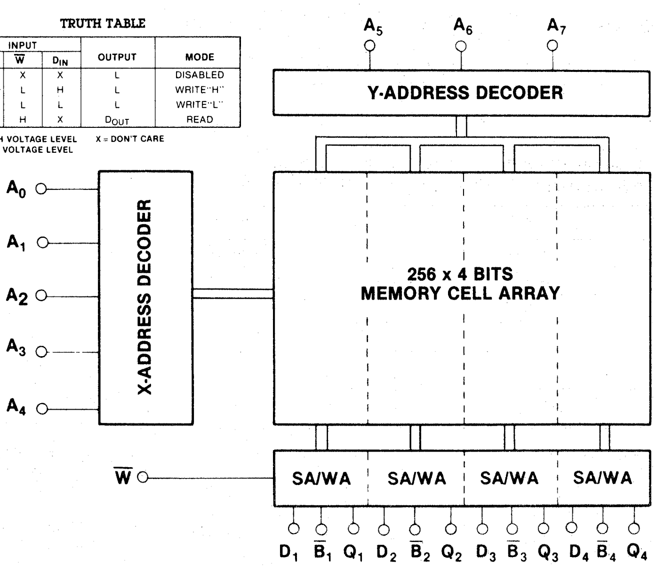
- **256 words x 4-bits organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 100K-series ECL families**
- **Address Access Time: 7 ns max.**
- **Block Select Access Time: 4 ns max.**
- **Open emitter output for easy memory expansion**
- **Low power dissipation of 0.7 mW/bit**
- **DOPOS and IOP-II processing**
- **Pin compatible with the F100422**

MBM100422A BLOCK DIAGRAM

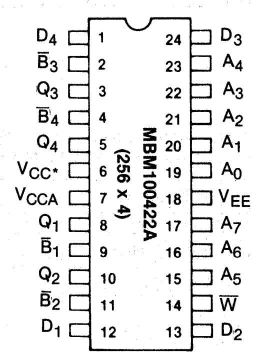
TRUTH TABLE

INPUT $\overline{S}$	INPUT $\overline{W}$	INPUT D_{IN}	OUTPUT	MODE
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = HIGH VOLTAGE LEVEL X = DON'T CARE
L = LOW VOLTAGE LEVEL



PIN ASSIGNMENT



*V_{CC} Grounded

NOTE: DIP and Flat package styles conform to the same pin assignment.

PRELIMINARY

**Note: This is not a final specification.
Some parametric limits are subject to change.**

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100422A is fully decoded 1024-bit read/write random access memory organized as 256 words by 4 bits. Memory cell selection is achieved by means of a 8-bit address designated $A_0 \sim A_7$. The active low Block Select $\overline{B}$ input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{W}$ input. With $\overline{W}$ and $\overline{B}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{B}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	DIP = T_A, Flat = T_C	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Temperature*
Supply Voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to +85°C

* Ambient for DIP, case for Flat package.

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω and 30 pF to −2.0V, T_A = 0°C to 85°C and Airflow ≥ 2.5 m/s, unless otherwise noted.)

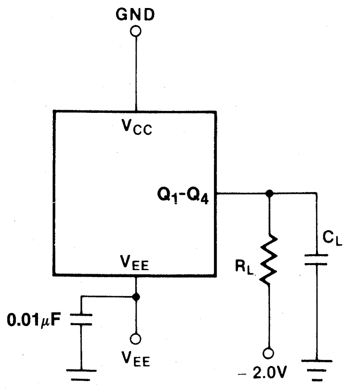
Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage ($V_{IN} = V_{IH max.}$ or $V_{IL min.}$)	V_{OH}	−1025	—	−880	mV
Output Low Voltage ($V_{IN} = V_{IH max.}$ or $V_{IL min.}$)	V_{OL}	−1810	—	−1620	mV
Output High Voltage ($V_{IN} = V_{IH min.}$ or $V_{IL max.}$)	V_{OHC}	−1035	—	—	mV
Output Low Voltage ($V_{IN} = V_{IH min.}$ or $V_{IL max.}$)	V_{OLC}	—	—	−1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1165	—	−880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1810	—	−1475	mV
Input High Current ($V_{IN} = V_{IH max.}$)	I_{IH}	—	—	220	μA
Input Low Current ($V_{IN} = V_{IL min.}$)	I_{IL}	−50	—	—	μA
$\overline{B}$ Input Low Current ($V_{IN} = V_{IL min.}$)	I_{IL}	0.5	—	170	μA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA

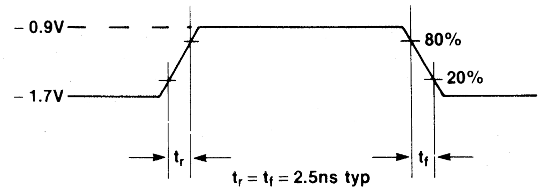
PRELIMINARY
Note: This is not a final specification. Some parametric limits are subject to change.

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ±5%, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat package, Output Load = 50Ω to −2.0V and 30pF to GND, and Airflow ≥ 2.5 m/s, unless otherwise noted.)

AC TEST CONDITIONS





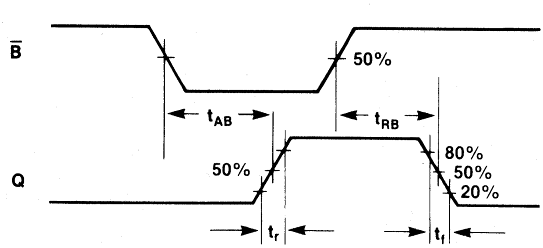
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

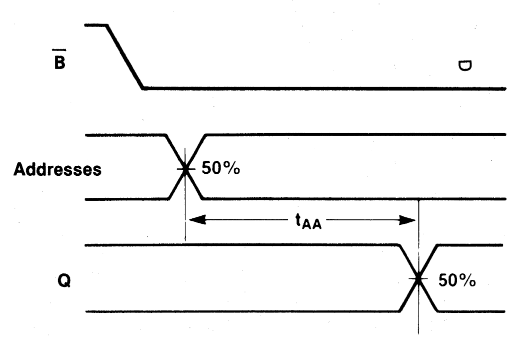
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	5	7	ns
Block Select Access Time	t_{AB}	—	2.5	4	ns
Block Select Recovery Time	t_{RB}	—	2.5	4	ns

READ CYCLE

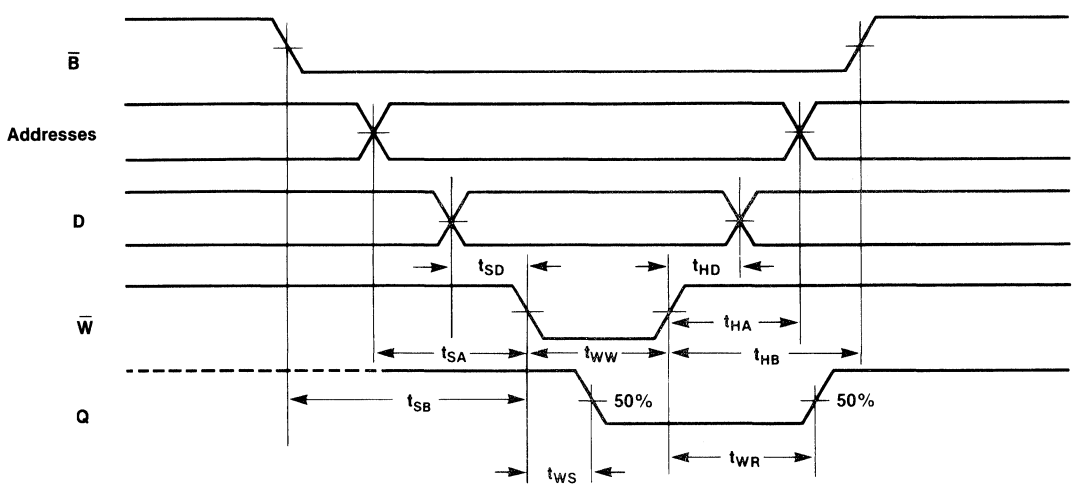




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	5	—	—	ns
Write Disable Time	t_{WS}	—	—	4	ns
Write Recovery Time	t_{WR}	—	—	8	ns
Address Set Up Time	t_{SA}	1	—	—	ns
Block Select Set Up Time	t_{SB}	1	—	—	ns
Data Set Up Time	t_{SD}	1	—	—	ns
Address Hold Time	t_{HA}	1	—	—	ns
Block Select Hold Time	t_{HB}	1	—	—	ns
Data Hold Time	t_{HD}	1	—	—	ns

WRITE CYCLE



RISE TIME AND FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	1.5	—	ns
Output Fall Time	t_f	—	1.5	—	ns

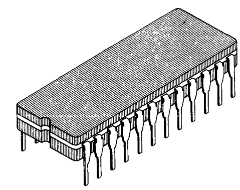
ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

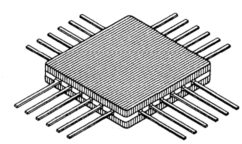
The Fujitsu MBM100474 is a fully decoded 4096-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4-bits, and it features on-chip voltage temperature compensation for improved noise margin.

The MBM100474 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon), processing.

Operation for the MBM100474 is specified over a temperature range of 0 °C to 85 °C (T_A for DIP, T_C for Flat Package). It features 24-pin cerdip dual in-line packaging and flat package, and is fully compatible with industry-standard 100K-series ECL families.



CERDIP PACKAGE
DIP-24C-C05

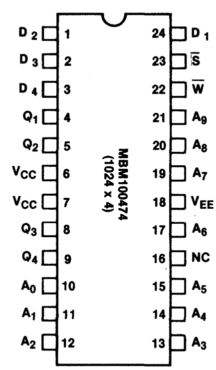


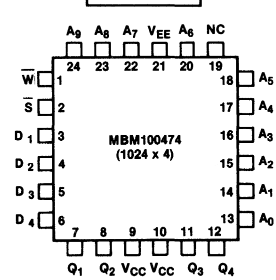
CERDIP PACKAGE
FPT-24C-C02

FEATURES

- **1024 words x 4-bits organization**
- **On-chip voltage/temperature compensation for improved noise margin**
- **Fully compatible with industry-standard 100K-series ECL families**
- **Address Access Time:**
  MBM100474-15: 15 ns max.
- **Chip select access time:**
  MBM100474-15: 8 ns max.
- **Open emitter output for easy memory expansion**
- **Low power dissipation:**
  MBM100474-15:
  0.2mW/bit typ.
- **DOPOS and IOP processing**
- **Pin compatible with the F100474**

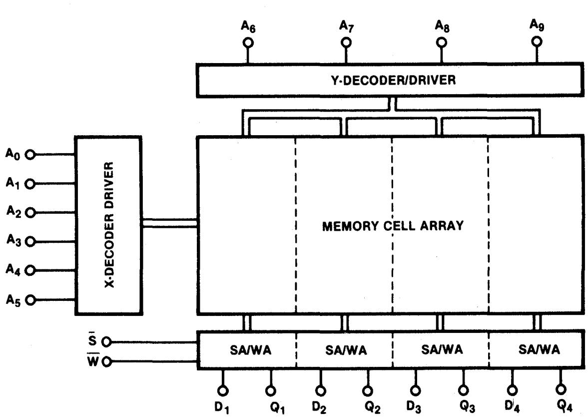
PIN ASSIGNMENTS





*Vcc grounded

MBM100474 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100474 is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated $A_0 \sim A_9$. The active low Chip Select $\overline{S}$ input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{W}$ input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

ABSOLUTE MAXIMUM RATINGS (See Note)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Temperature*
Supply Voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to +85°C

* Ambient for DIP, case for flat package.

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	5	pF
Output Pin Capacitance	C_{OUT}	—	7	8	pF

DC CHARACTERISTICS

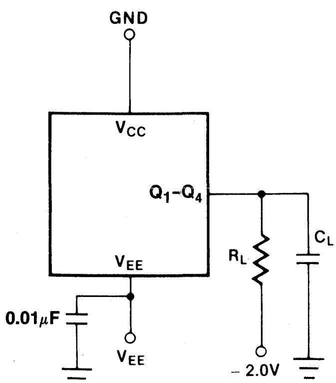
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω to −2.0V, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat package and Airflow ≥ 2.5 m/s, unless otherwise noted.)

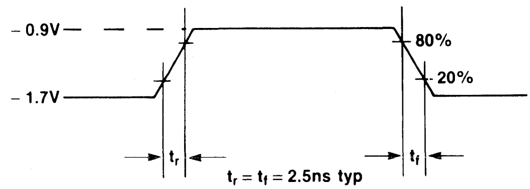
Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage ($V_{IN} = V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OH}	−1025	—	−880	mV
Output Low Voltage ($V_{IN} = V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OL}	−1810	—	−1620	mV
Output High Voltage ($V_{IN} = V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OHC}	−1035	—	—	mV
Output Low Voltage ($V_{IN} = V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OLC}	—	—	−1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1165	—	−880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1810	—	−1475	mV
Input High Current ($V_{IN} = V_{IH\,max.}$)	I_{IH}	—	—	220	μA
Input Low Current ($V_{IN} = V_{IL\,min.}$)	I_{IL}	−50	—	—	μA
$\overline{S}$ Input Low Current ($V_{IN} = V_{IL\,min.}$)	I_{IL}	0.5	—	170	μA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ±5%, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat package, Output Load = 50Ω to −2.0V and 30pF to GND, and Airflow ≥ 2.5 m/s, unless otherwise noted.)

AC TEST CONDITIONS





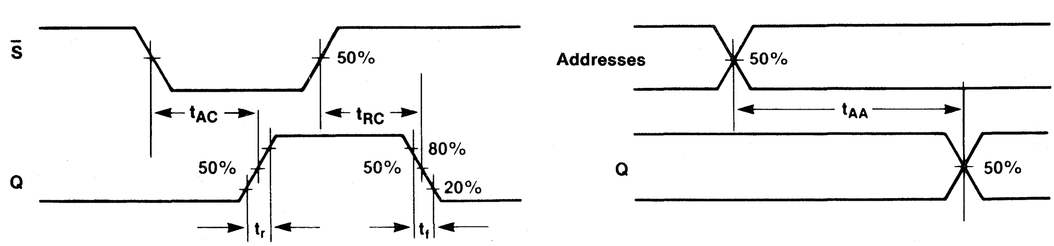
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM100474-15			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}	4		15	ns
Chip Select Access Time	t_{AC}	2		8	ns
Chip Select Recovery Time	t_{RC}	2		8	ns

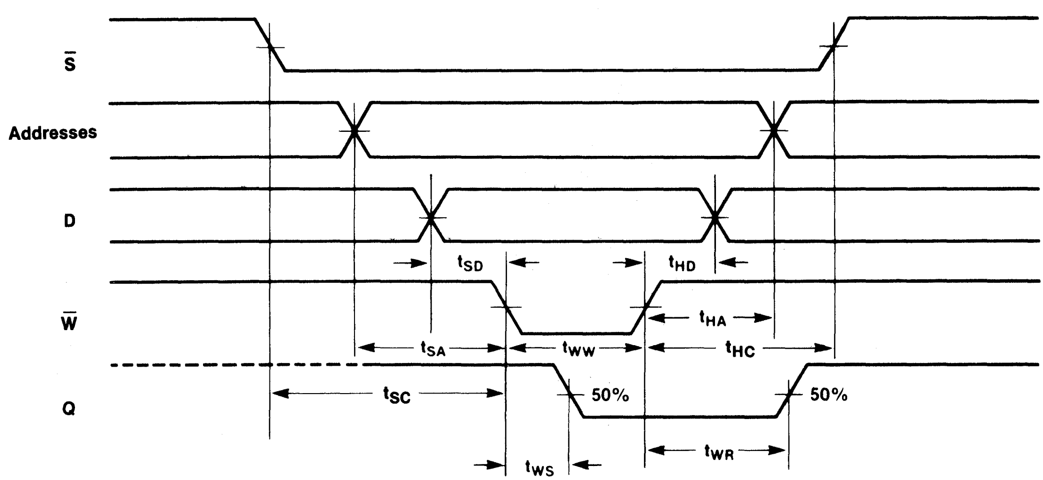
READ CYCLE



WRITE CYCLE

Parameter	Symbol	MBM100474-15			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	15	—	—	ns
Write Disable Time	t_{WS}	—	—	8	ns
Write Recovery Time	t_{WR}	—	—	8	ns
Address Set Up Time	t_{SA}	2	—	—	ns
Chip Select Set Up Time	t_{SC}	2	—	—	ns
Data Set Up Time	t_{SD}	2	—	—	ns
Address Hold Time	t_{HA}	3	—	—	ns
Chip Select Hold Time	t_{HC}	2	—	—	ns
Data Hold Time	t_{HD}	2	—	—	ns

WRITE CYCLE

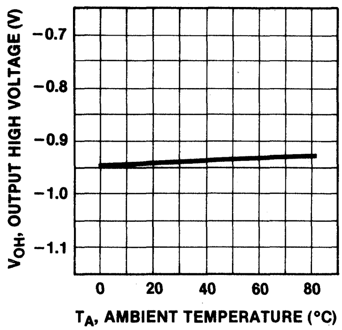


RISE TIME AND FALL TIME

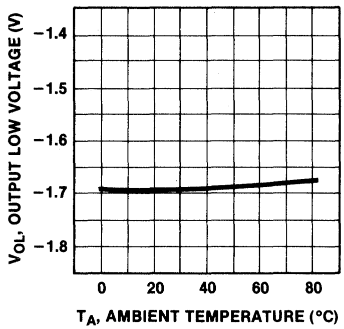
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	1.5	2	5	ns
Output Fall Time	t_f	1.0	2	5	ns

TYPICAL CHARACTERISTICS CURVES

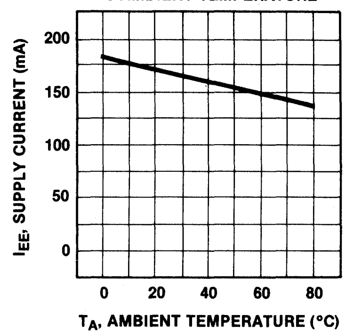
OUTPUT HIGH VOLTAGE
vs AMBIENT TEMPERATURE



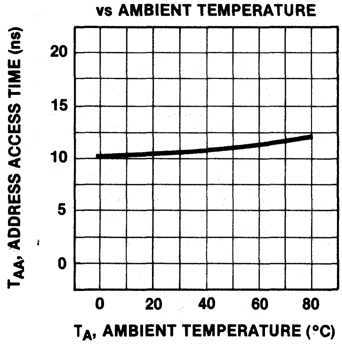
OUTPUT LOW VOLTAGE
vs AMBIENT TEMPERATURE



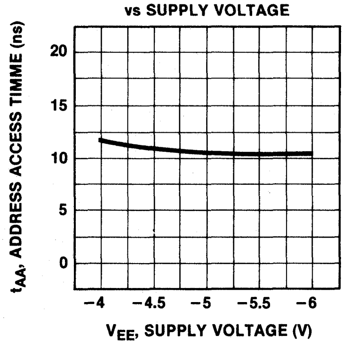
SUPPLY CURRENT
vs AMBIENT TEMPERATURE



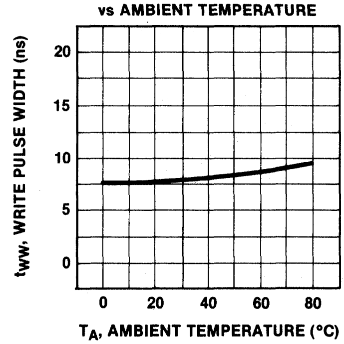
ADDRESS ACCESS TIME
vs AMBIENT TEMPERATURE



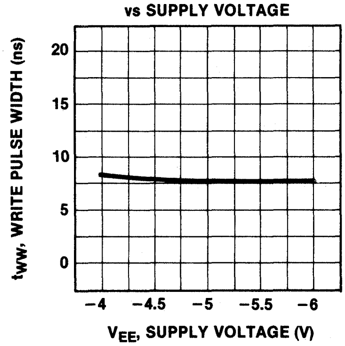
ADDRESS ACCESS TIME
vs SUPPLY VOLTAGE



WRITE PULSE WIDTH
vs AMBIENT TEMPERATURE



WRITE PULSE WIDTH
vs SUPPLY VOLTAGE



FUJITSU
MICROELECTRONICS, INC.

MBM100480-25

PRELIMINARY
Note: This is not a final specification. Some parametric limits are subject to change.

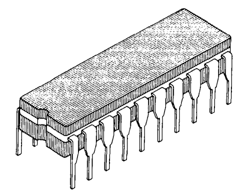
ECL 16,384-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

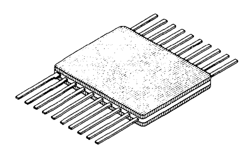
The Fujitsu MBM100480-25 is a fully decoded 16384-bit ECL read/write random access memory designed for main, control and buffer storage applications. This device is organized as 16384 words by 1-bit, and it features on-chip voltage/temperature compensation for improved noise margin.

The MBM100480-25 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM100480-25 is specified over a temperature range of 0 °C to 85 °C (T_A for DIP, T_C for Flat Package). It features 20-pin Cerdip dual in-line or flat packaging. It is fully compatible with industry-standard 100K-series ECL families.



CERDIP PACKAGE
DIP-20C-C03

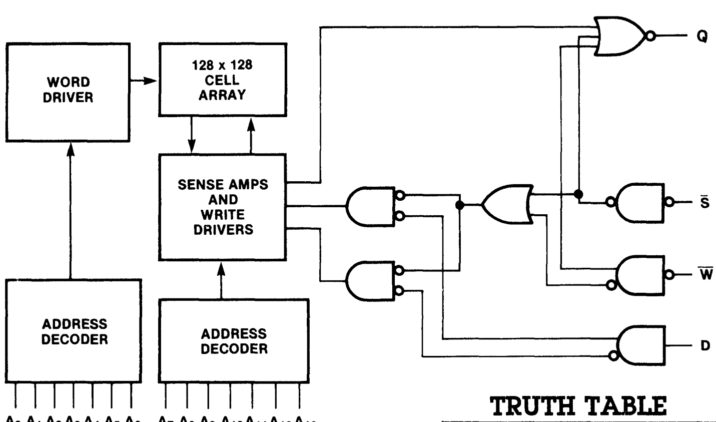


CERDIP PACKAGE
FPT-20C-C01

FEATURES

- **16384 words x 1-bits organization**
- **On-chip voltage/temperature compensation for improved noise margin**
- **Fully compatible with industry-standard 100K-series ECL families**
- **Address Access Time: 25 ns max.**
- **Chip select access time: 15 ns max.**
- **Open emitter output for easy memory expansion**
- **Low power dissipation of 0.04 mW/bit**
- **DOPOS and IOP-II**
- **Pin compatible with the F100480**

MBM100480 BLOCK DIAGRAM

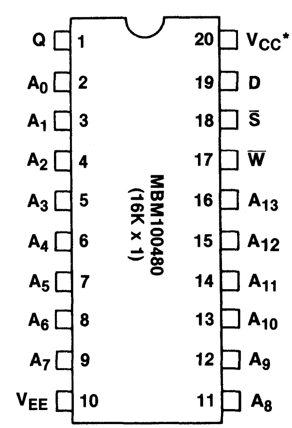


TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't care

PIN ASSIGNMENT



*V_{CC} grounded

Note: DIP and Flat Package styles conform to the same pin assignment.

PRELIMINARY

Note: This is not a final specification.
Some parametric limits are subject to change.

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100480 is fully decoded 16,384-bit read/write random access memory organized as 16,384 words by 1 bit. Memory cell selection is achieved by means of a 8-bit address designated $A_0 \sim A_{13}$. The active low Chip Select $\overline{S}$ input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{W}$ input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

ABSOLUTE MAXIMUM RATINGS (See Note)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A for DIP/T_C for Flat Pack	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

GUARANTEED OPERATING CONDITIONS (Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Temperature*
Supply Voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to +85°C

* Ambient for DIP, case for Flat package.

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	—	—	pF
Output Pin Capacitance	C_{OUT}	—	—	—	pF

DC CHARACTERISTICS

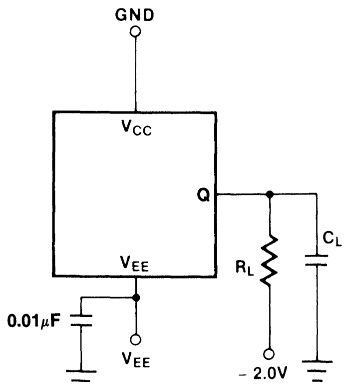
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω, 30pF to −2.0V, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat package and Airflow ≥ 2.5 m/s, unless otherwise noted.)

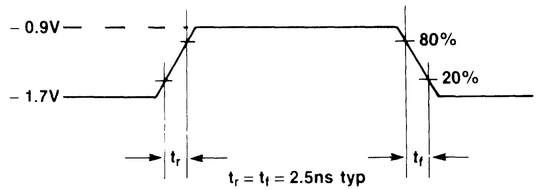
Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage ($V_{IN} = V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OH}	−1025	—	−880	mV
Output Low Voltage ($V_{IN} = V_{IH\,max.}$ or $V_{IL\,min.}$)	V_{OL}	−1810	—	−1620	mV
Output High Voltage ($V_{IN} = V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OHC}	−1035	—	—	mV
Output Low Voltage ($V_{IN} = V_{IH\,min.}$ or $V_{IL\,max.}$)	V_{OLC}	—	—	−1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1165	—	−880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1810	—	−1475	mV
Input High Current ($V_{IN} = V_{IH\,max.}$)	I_{IH}	—	—	220	μA
Input Low Current ($V_{IN} = V_{IL\,min.}$)	I_{IL}	−50	—	—	μA
$\overline{S}$ Input Low Current ($V_{IN} = V_{IL\,min.}$)	I_{IL}	0.5	—	170	μA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ±5%, T_A = 0°C to 85°C for DIP, T_c = 0°C to 85°C for Flat Pack, Output Load = 50Ω to −2.0V and 30pF to GND, and Airflow ≥ 2.5 m/s, unless otherwise noted.)

AC TEST CONDITIONS





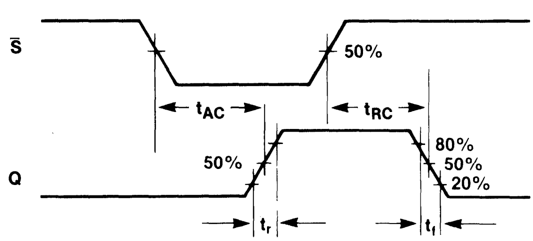
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

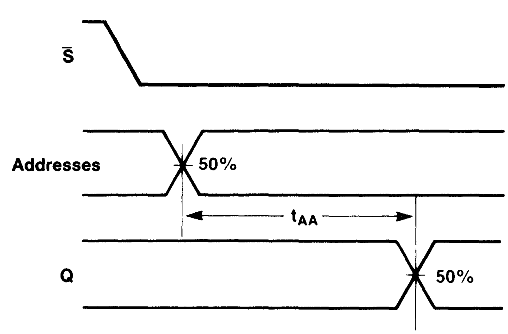
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	—	25	ns
Chip Select Access Time	t_{AC}	—	—	15	ns
Chip Select Recovery Time	t_{RC}	—	—	15	ns

READ CYCLE





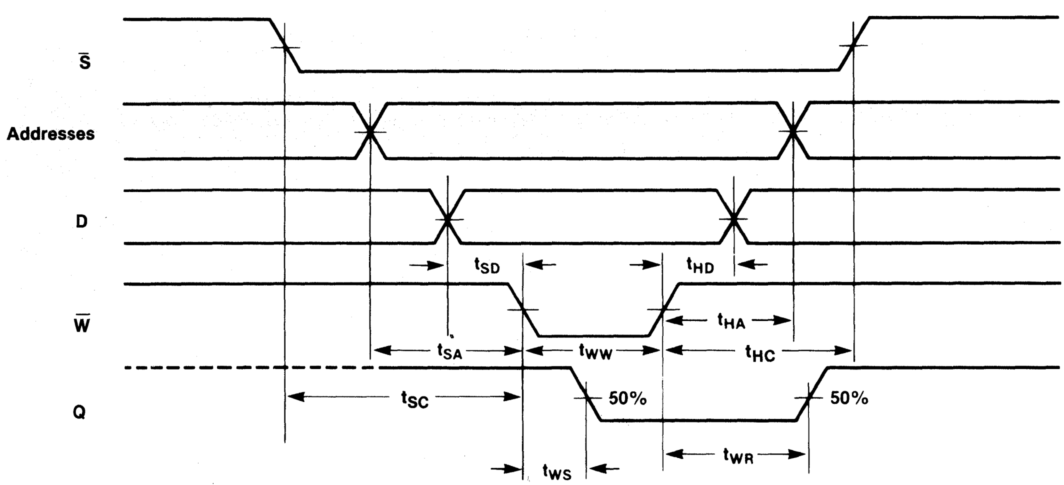
PRELIMINARY

Note: This is not a final specification.
Some parametric limits are subject to change.

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	25	—	—	ns
Write Disable Time	t_{WS}	—	—	15	ns
Write Recovery Time	t_{WR}	—	—	20	ns
Address Set Up Time	t_{SA}	5	—	—	ns
Chip Select Set Up Time	t_{SC}	5	—	—	ns
Data Set Up Time	t_{SD}	5	—	—	ns
Address Hold Time	t_{HA}	5	—	—	ns
Chip Select Hold Time	t_{HC}	5	—	—	ns
Data Hold Time	t_{HD}	5	—	—	ns

WRITE CYCLE



RISE TIME AND FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	3	—	ns
Output Fall Time	t_f	—	3	—	ns

Bipolar PROMs

Fujitsu Microelectronics offers a full line of Schottky TTL bipolar PROMs ranging from 4K to 64K. All FMI PROMs are manufactured using our patented DEAP™ (diffused eutectic aluminum process) technique which produces unmatched reliability and performance. The DEAP technique is responsible for a smaller cell size of 0.56 mil^2 — less than half the size of conventional PROMs. Two passive isolation techniques, SVG (shallow V-groove) and IOP (isolation by oxide and polysilicon) also give a closer cell spacing. These processes increase PROM density, cut die size in half, and ultimately, result in lower chip costs, higher speeds and higher programming yields.

Fujitsu Microelectronics also offers extended temperature range versions of our PROMs which operate between −55°C and 125°C.

For more information on all Fujitsu Microelectronics PROMs, consult our 1983 PROM Data Book.

Fujitsu Part No.	Size	Organization	Output	Package Pins	Other Features	AMD	Fairchild	Harris	Hitachi	Intel	MMI	Motorola	National	NEC	Raytheon	Signetics	TI
MB7117	2048	256 x 8	0C	18							53/6308		54/74S470				TBP18SA22
MB7118	2048	256 x8	3S	20							53/6309		54/74S471				TBP18S22
MB7121	4096	1024 x 4	0C	18		AM27S32	93452	HM7642	HN25044	3605	53/6352	MCM7642	DM54/74S572	μPB406		N/S82S136	TBP24SA41
MB7122	4096	1024 x 4	3S	18		AM27S33	93453	HM7643	HN25045	3625	53/6353	MCM7643	DM54/74S573	μPB426		N/S82S137	TBP24S41
MB7123	4096	512 x 8	0C	20		AM27S28		HM7648			53/6348		DM54/74S473		29620	N/S82S146	TBP28SA42
MB7124	4096	512 x 8	3S	20		AM27S29		HM7649			53/6349		DM54/74S472		29621	N/S82S147	TBP28S42
MB7127	8192	2048 x 4	0C	18		AM27S184		HM7684	HN25084		53/6388	MCM7684	DM77/87S184		29650	N/S82S184	TBP24SA81
MB7128	8192	2048 x 4	3S	18		AM27S185		HM7685	HN25085		53/6389	MCM7685	DM77/87S185		29651	N/S82S185	TBP24S81
MB7131	8192	2048 x 8	0C	24		AM27S180	93450	HM7680	HN25088	3608	53/6380	MCM7680	DM77/87S180		29630	N/S82S180	TBP28SA86
MB7131-SK	8192	1024 x 8	0C	24	.300 mil narrow pkg	AM27S280							DM77/87S280				
MB7132	8192	1024 x 8	3S	24		AM27S181	93451	HM7681	HN25089	3628	53/6381	MCM7681	DM77/87S181	μPB417	29631	N/S82S181	TBP28S86
MB7132-SK	8192	1024 x 8	3S	24	.300 mil narrow pkg	AM27S281							DM77/87S281				
MB7134	16384	4096 x 4	3S	20													
MB7137	16384	2048 x 8	0C	24		AM27S190	93510		HN25168			MCM76160	DM77/87S190	μPB409	29680	N/S82S190	TBP28SA166
MB7137-SK	16384	2048 x 8	0C	24	.300 mil narrow pkg	AM27S290							DM77/87S290				
MB7138	16384	2048 x 8	3S	24		AM27S191	93511	HM76161	HN25169	3636	63S1681	MCM76161	DM77/87S191	μPB429	29681	N/S82S191	TBP28S166
MB7138-SK	16384	2048 x 8	3S	24	.300 mil narrow pkg	AM27S291							DM77/87S291				
MB7141	32768	4096 x 8	0C	24											29670	N/S825320	
MB7142	32768	4096 x 8	3S	24		AM27S43		HM76321		3632	63S3281		DM77/87S321		29671	N/S825321	
MB7143	65536	8192 x 8	0C	24													
MB7144	65536	8192 x 8	3S	24				HM76641									
MB7151	16384	4096 x 4	0C	20		AM27S40											
MB7152	16384	4096 x 4	3S	20		AM27S41		HM76165			53/63S1641					N/S82S195	

Commercial Temperature Range PROMS (0°C to +75°C Operating Temperature)					
Device	**Organization**	**Access Time (max)**	**Power Supply Volts**	**Power Dissipation**	**Package**
MB7117E	256 x 8	45nS	+5	140mA	20-pin
MB7117H	256 x 8	35nS	+5	140mA	20-pin
MB7118E	256 x 8	45nS	+5	140mA	20-pin
MB7118H	256 x 8	45nS	+5	140mA	20-pin
MB7121E	1K x 4	45nS	+5	150mA	18-pin
MB7121H	1K x 4	35nS	+5	150mA	18-pin
MB7122E	1K x 4	45nS	+5	150mA	18-pin
MB7122H	1K x 8	35nS	+5	150mA	18-pin
MB7123E	512 x 8	45nS	+5	170mA	20-pin
MB7123H	512 x 8	35nS	+5	170mA	20-pin
MB7124E	512 x 8	45nS	+5	170mA	20-pin
MB7124H	512 x 8	35nS	+5	170mA	20-pin
MB7127E	2K x 4	55nS	+5	155mA	18-pin
MB7127H	2K x 4	45nS	+5	155mA	18-pin
MB7128E	2K x 4	55nS	+5	155mA	18-pin
MB7128H	2K x 4	45nS	+5	155mA	18-pin
MB7128Y	2K x 4	35nS	+5	155mA	18-pin
MB7131E	1K x 8	55nS	+5	175mA	24-pin
MB7131H	1K x 8	45nS	+5	175mA	24-pin
MB7132E	1K x 8	55nS	+5	175mA	24-pin
MB7132H	1K x 8	45nS	+5	175mA	24-pin
MB7132Y	1K x 8	35nS	+5	175mA	24-pin
MB7133E	4K x 4	55nS	+5	170mA	20-pin
MB7133H	4K x 4	45nS	+5	170mA	20-pin
MB7134E	4K x 4	55nS	+5	170mA	20-pin
MB7134H	4K x 4	45nS	+5	170mA	20-pin
MB7134Y	4K x 4	35nS	+5	170mA	20-pin
MB7137E	2K x 8	55nS	+5	180mA	24-pin
MB7137H	2K x 8	45nS	+5	180mA	24-pin
MB7138E	2K x 8	55nS	+5	180mA	24-pin
MB7138H	2K x 8	45nS	+5	180mA	24-pin
MB7138Y	2K x 8	35nS	+5	180mA	24-pin
MB7141E	4K x 8	65nS	+5	185mA	24-pin
MB7141H	4K x 8	55nS	+5	185mA	24-pin
MB7142E	4K x 8	65nS	+5	185mA	24-pin
MB7142H	4K x 8	55nS	+5	185mA	24-pin
MB7143E	8K x 8	65nS	+5	190mA	24-pin
MB7143H	8K x 8	55nS	+5	190mA	24-pin
MB7144E	8K x 8	65nS	+5	190mA	24-pin
MB7144H	8K x 8	55nS	+5	190mA	24-pin
MB7151E	4K x 4	45nS	+5	170mA	20-pin
MB7151H	4K x 4	55nS	+5	170mA	20-pin
MB7152E	4K x 4	45nS	+5	170mA	20-pin
MB7152H	4K x 4	55nS	+5	170mA	20-pin
MB7152Y	4K x 4	35nS	+5	170mA	20-pin

Extended Temperature Range PROMS (−55°C to +125°C Operating Temperatures)								
Device	**Size**	**Organization**	**Output**	**Package Pins**	**Max Access Time (ns)**	**Max Power Dissipation (mA)**	**Package**	**Alternate Source**
MB7128E-W	8192	2048 x 4	3S	18	55	155	Z, F, V	82S185
MB7132E-W	8192	1024 x 8	3S	24	55	175	Z, F, V	82S181
MB7138E-W	16384	2048 x 8	3S	24	55	180	Z, F, V	82S191
MB7142E-W	32768	4096 x 8	3S	24	65	185	Z, F, V	82S321
MB7144E-W	65536	8000 x 8	3S	24	70	190	Z, F, V	

Fujitsu also offers a family of DEAP PROMs available in extended temperature range (−55°C to +125°C). These PROMs are of the same generic family as the commercial temperature range product and utilize the same programming methods and more elaborate testing procedures. This product is available processed to Mil. Std. 883B or 883C.

General Information

Reliability Testing

Reliability testing includes three types of tests — lot tests (after production starts), periodic tests, and "occasional" tests. This section explains the details of each test in turn.

Lot Tests
The particulars of lot tests are listed in Table 5. There are two types of lot tests, called group A tests and group B tests. Group A tests and Group B tests are performed on items that are tested regularly, usually every week.

Details of individual tests vary with the product under test, but all samples are selected at random from every cycle lot. Tests are not performed in any particular order unless specified. Rather, they are performed for each device type.

Note that the high-temperature storage and continuous-operation tests usually take 500 hours, although they may take only 168 hours in special cases. Good samples are returned to their lots after non-destructive testing. Bad samples and samples that have undergone destruction testing are disposed.

Periodic Tests
Particulars of the periodic tests are also listed in Table 5. There are two types of periodic tests — group C tests and group D tests. Group C tests are performed on items that are tested regularly, usually every 13 weeks. Group D tests include special reliability test and very long life tests. The Group D test is usually done once every 26 weeks.

Details of individual tests vary with the product under test, but all samples are selected at random. Tests are not performed in any particular order unless specified. Rather, they are performed for each device type.

Note that the high-temperature storage and continuous operation tests for group C take 1000 hours and those for group D take 3000 hours.

Occasional Tests
Occasional tests are performed on products whenever necessary. The tests are similar to periodic tests, but their details are specified by the QC/Reliability Engineering Department according to the purpose of the test.

Table 5 Sampling Plan for Reliability Testing.

Group	Subgroup	Device Classification / Test Items		Device Group 1 Sample Size	Device Group 1 Acceptance Number	Device Group 2 Sample Size	Device Group 2 Acceptance Number
A	A1	External Visual Inspection		100% Test of Sampling Devices (All Sampled Devices)			
	A2	Electrical Characteristics	Fuction Test	LTPD 5% $A_c=0$			
	A3		Static Characteristics	LTPD 5% $A_c=0$			
	A4		Dynamic/Switching Characteristics	LTPD 5% $A_c=0$			
B	B1	Physical Dimensions		9	1	6	1
	B2	Environmental Tests	Thermal Environmental Test	9	1	9	1
	B3		Mechanical Environmental Tests	9	1	9	1
	B4-I	Solderability (230°C, 5s)[*1]		9	1	3	1
	B4-II	Solderability (260°C, 5s)[*1]		9	1	3	1
	B5	Lead Integrity[*1]		9	1	3	1
	B6	Pressure-Temperature-Humidity Storage[*2]		9	1[*3]	9	1[*3]
	B7	Endurance Test	High-Temperature Storage[*5]	14	1[*4]	7	1[*4]
	B8		Continuous Operation	24	1[*4]	11	1[*4]
	B9		High-Humidity Storage 85°C, 85%RH[*2]	24	1[*4]	11	1[*4]
C	C1		High-Temperature Storage[*5]	14	1[*6]	7	1[*6]
	C2		Continuous Operation	24	1[*6]	11	1[*6]
	C3		High-Humidity Storage 85°C, 85%RH[*6]	24	1[*6]	11	1[*4]
D	D1		High-Temperature Storage[*5][*7]	14	—	7	—
	D2		Continuous Operation[*7]	24	—	11	—
	D3		High-Humidity Storage 85°C, 85%RH[*2][*7]	24	—	11	—

Test Cycle: Groups A and B for every weekly lot, Goup C every 13 weeks, Group D every 26 weeks

Notes

*1: Electrical reject devices can be used in this test.

*2: These tests are performed on resin-sealed devices.

*3: This test takes 96 hours.

*4: These tests normally take 500 hours. But if no defects are found in the first 168 hours, the lot can be passed and the test may be terminated.

*5: These tests are performed if the junction temperature during continuous operation is less than the maximum rated storage temperature specified for such devices.

*6: These tests take 1000 hours.

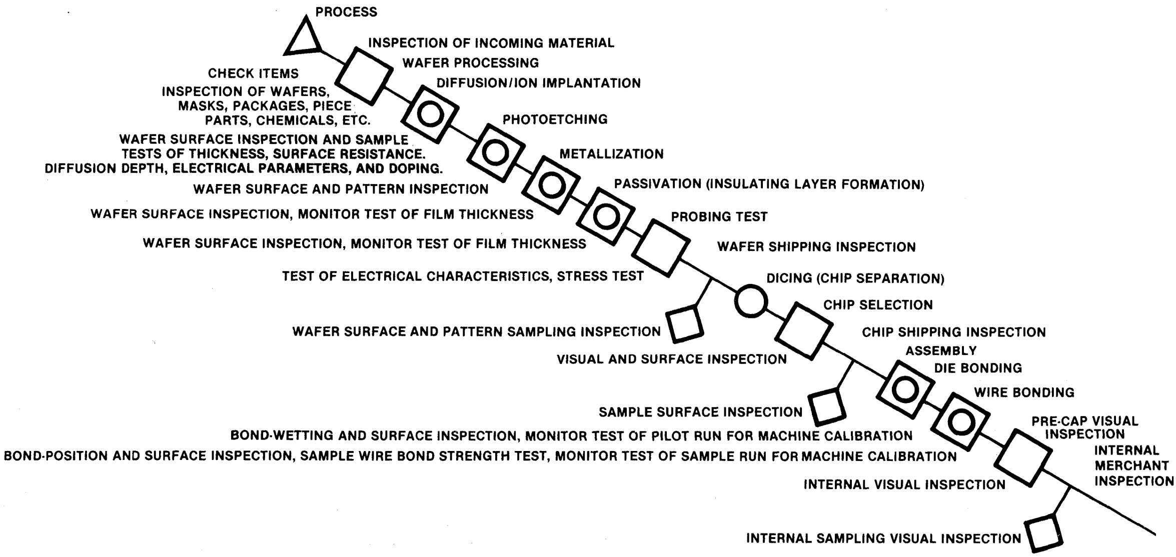
*7: These tests take 3000 hours.

Table 6 — Device Classification

Element Classification	Capacity in bits Bipolar	MOS	Logic/Analog (No. Elements/ Power Consumption)
Group 1 (SS1 and MSI devices)	up to 5000	up to 10,000	up to 1000/500 mW
Group 2 (LSI devices)	over 5000	over 10,000	Other

Quality Control Flow Chart

FIG. 3 THE QUALITY CONTROL FLOW CHART



LEGEND:

○ **PRODUCTION PROCESS**

□ **TEST/INSPECTION**

PRODUCTION PROCESS AND TEST/INSPECTION

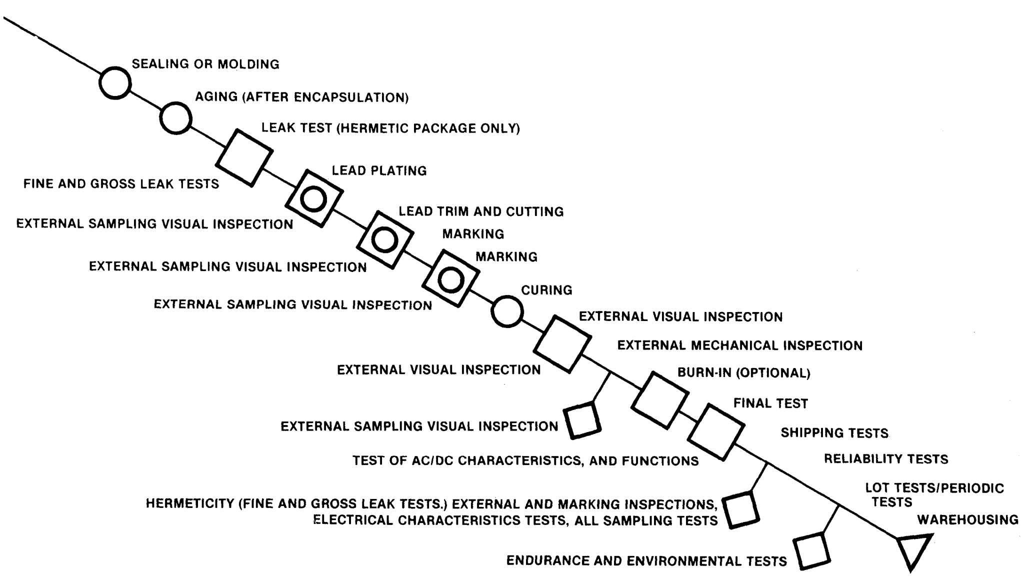
◇ **QC GATE (SAMPLING)**

NOTE: THE FLOW SEQUENCE MAY VARY SLIGHTLY WITH INDIVIDUAL PRODUCT TYPE.

TABLE 2. SAMPLING PLAN FOR THE SHIPPING TESTS.

TEST ITEM	SAMPLING PLAN
Electrical Characteristics	
Appearance	AQL0.25% (Level II)
Marking	
Hermeticity (Fine and Gross Leak Tests)*	AQL2.5% (Level II)
Appearance	

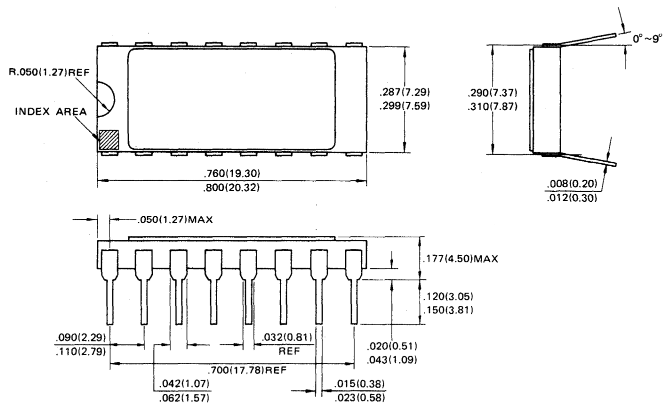
Note: * Applies to hermetic packages only.



Package Dimensions Dimensions in inches (millimeters)

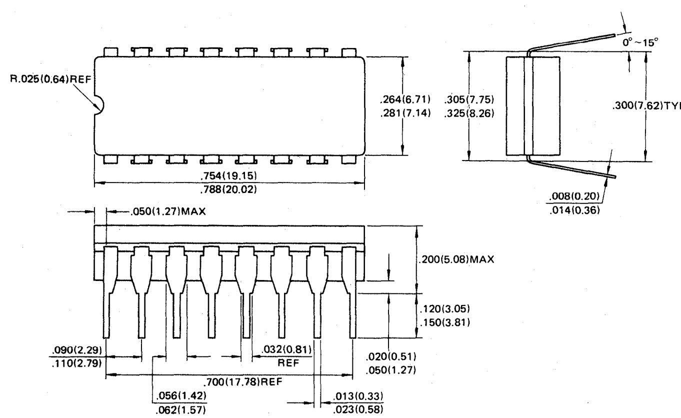
DIP-16C-A02

16-LEAD CERAMIC METAL SEAL DUAL IN-LINE PACKAGE



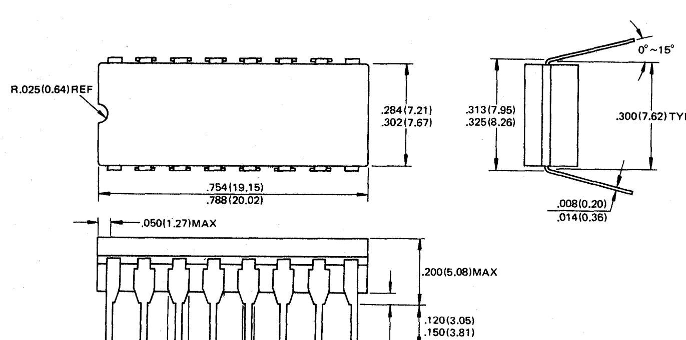
DIP-16C-C03

16-LEAD CERDIP DUAL IN-LINE PACKAGE



DIP-16C-C04

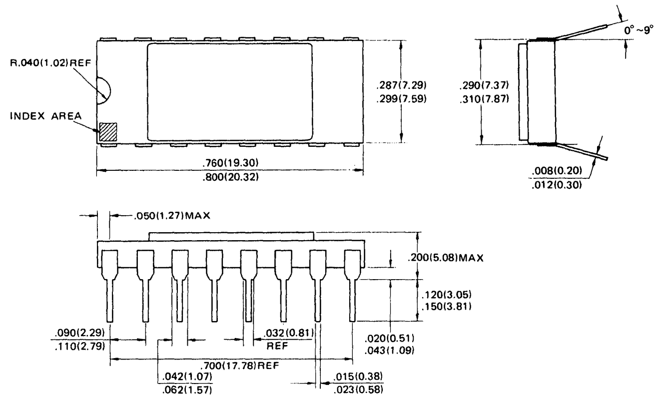
16-LEAD CERDIP DUAL IN-LINE PACKAGE



Package Dimensions Dimensions in inches (millimeters)

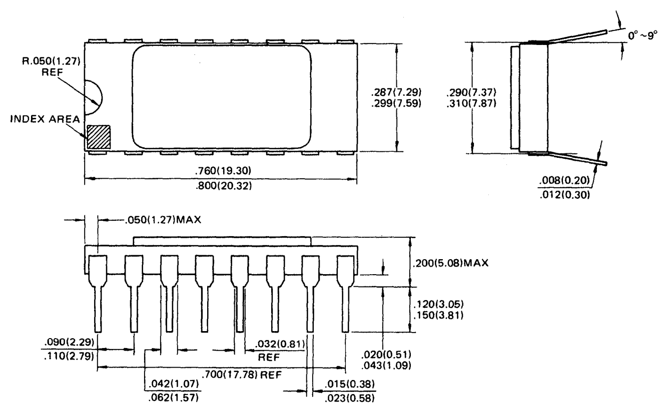
DIP-16C-F01

16-LEAD CERAMIC FRIT SEAL DUAL IN-LINE PACKAGE



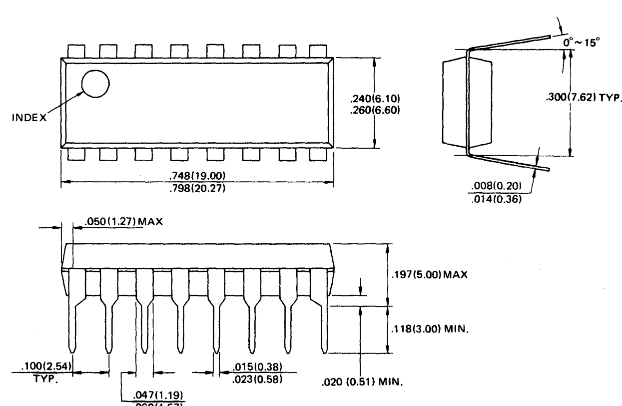
DIP-16C-F02

16-LEAD CERAMIC FRIT SEAL DUAL IN-LINE PACKAGE



DIP-16P-M01

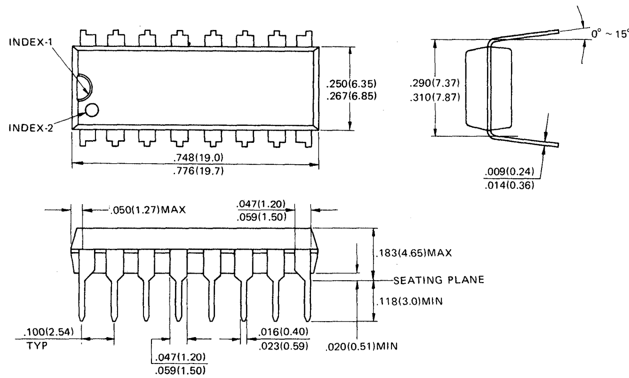
16-LEAD PLASTIC DUAL IN-LINE PACKAGE



Package Dimensions Dimensions in inches (millimeters)

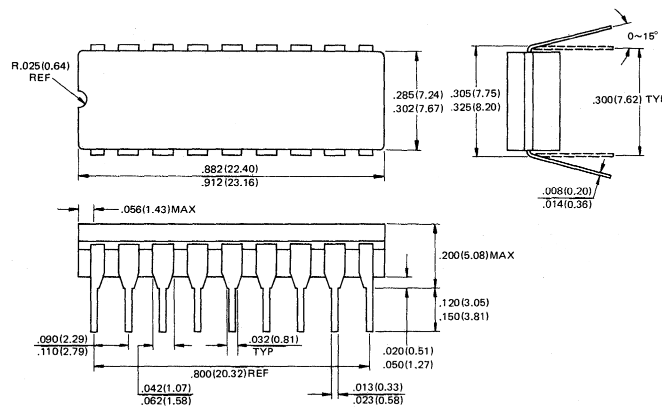
DIP-16P-M03

16-LEAD PLASTIC DUAL IN-LINE PACKAGE



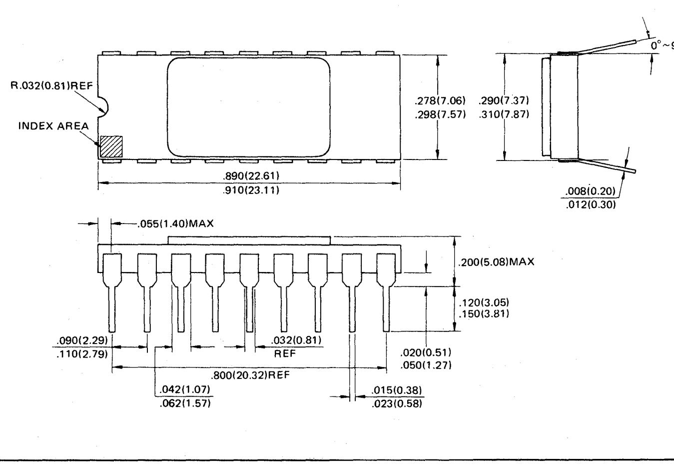
DIP-18C-C01

18-LEAD CERDIP DUAL IN-LINE PACKAGE



DIP-18C-F02

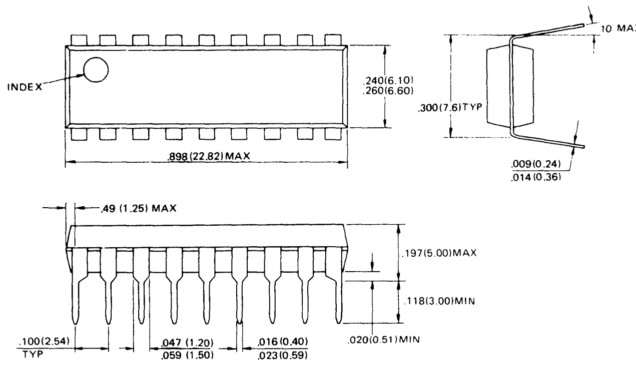
18-LEAD CERAMIC FRIT SEAL DUAL IN-LINE PACKAGE



Package Dimensions Dimensions in inches (millimeters)

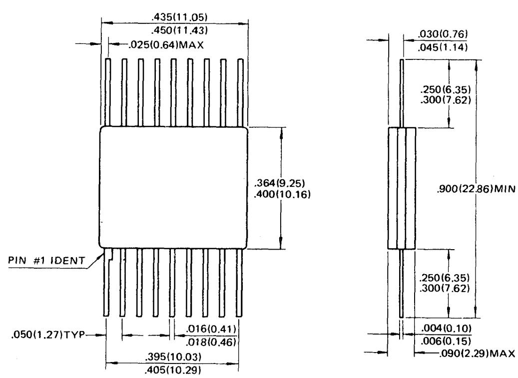
DIP-18P-M01

18-LEAD PLASTIC DUAL IN-LINE PACKAGE



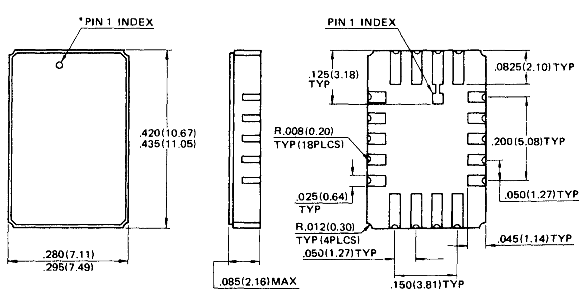
FPT-18C-C01

18-LEAD CERDIP FLAT PACKAGE



LCC-18C-A02

18-PAD CERAMIC METAL SEAL LEADLESS CHIP CARRIER

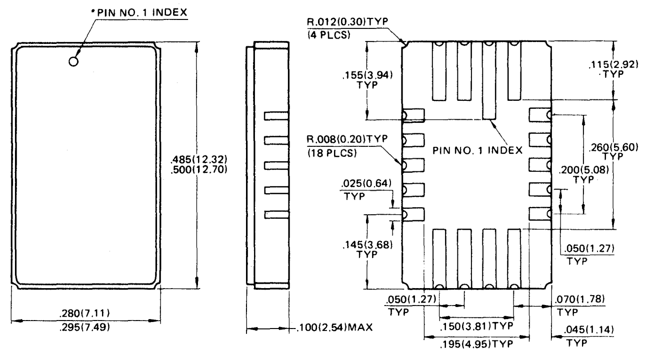


*Shape of Pin 1 index : Subject to change without notice

Package Dimensions Dimensions in inches (millimeters)

LCC-18C-A04

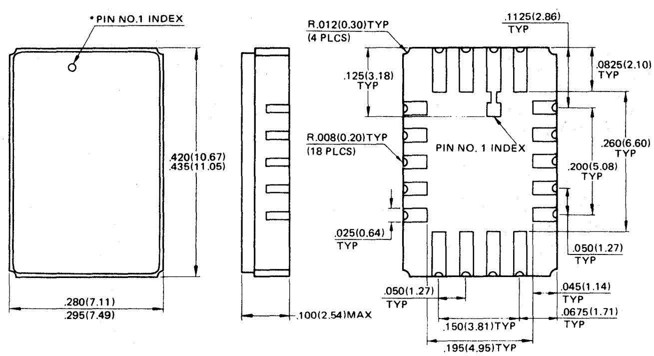
18-PAD CERAMIC LEADLESS CHIP CARRIER



*Shape of Pin 1 index: Subject to change without notice

LCC-18C-F02

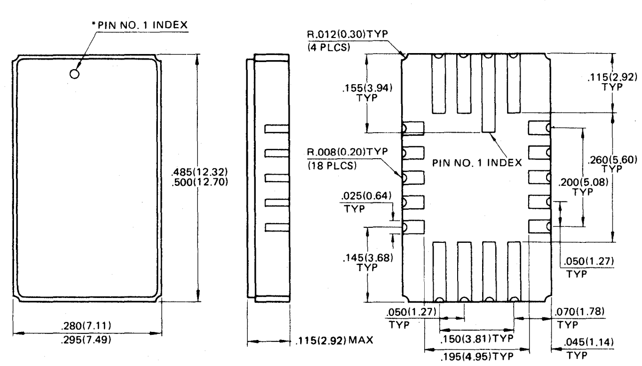
18-PAD CERAMIC FRIT SEAL LEADLESS CHIP CARRIER



*Shape of Pin 1 index: Subject to change without notice

LCC-18C-F04

18-PAD CERAMIC FRIT SEAL LEADLESS CHIP CARRIER

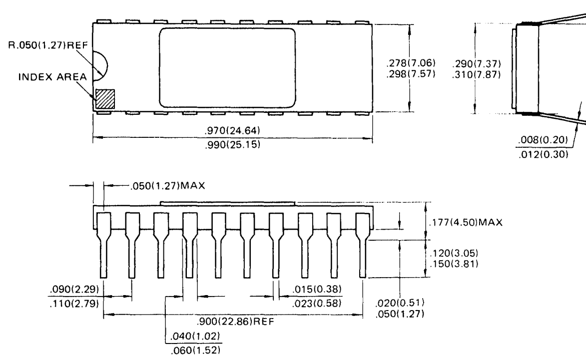


*Shape of Pin 1 index: Subject to change without notice

Package Dimensions Dimensions in inches (millimeters)

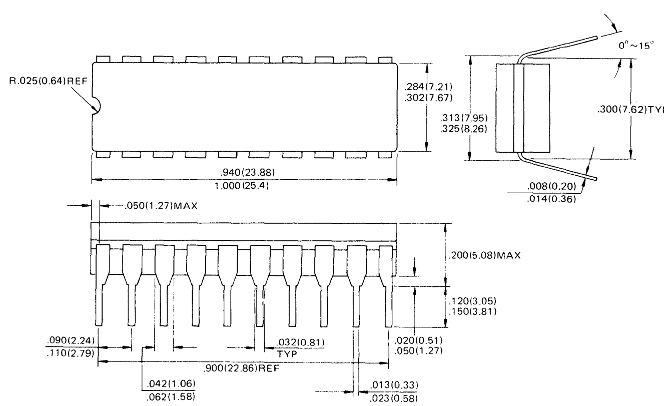
DIP-20C-A01

20-LEAD CERAMIC METAL SEAL DUAL IN-LINE PACKAGE



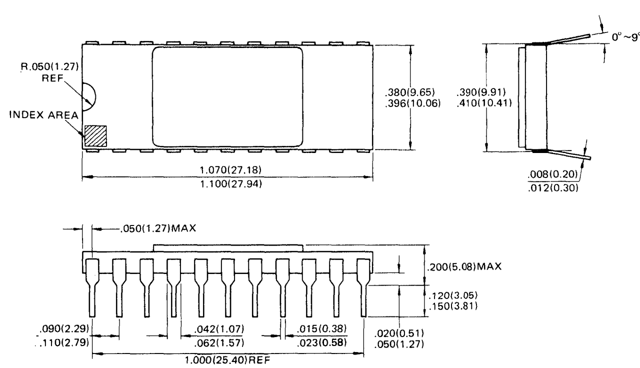
DIP-20C-C03

20-LEAD CERDIP DUAL IN-LINE PACKAGE



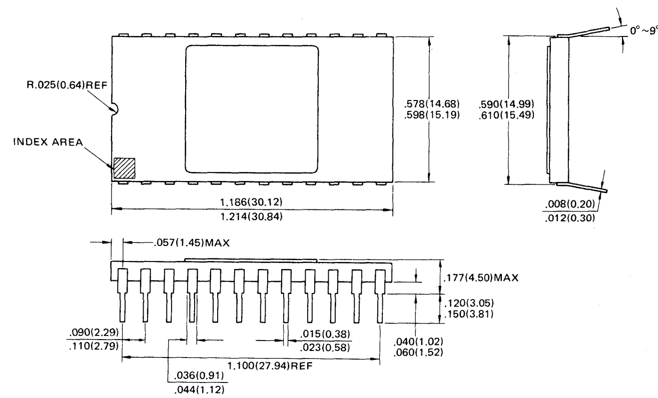
DIP-22C-F01

22-LEAD CERAMIC FRIT SEAL DUAL IN-LINE PACKAGE



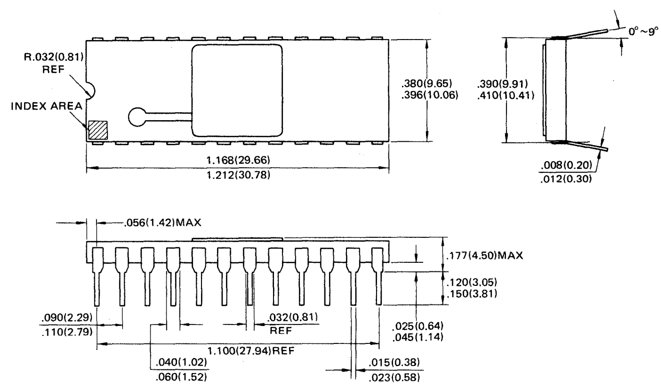
DIP-24C-A01

**24-LEAD CERAMIC
METAL SEAL
DUAL IN-LINE PACKAGE**



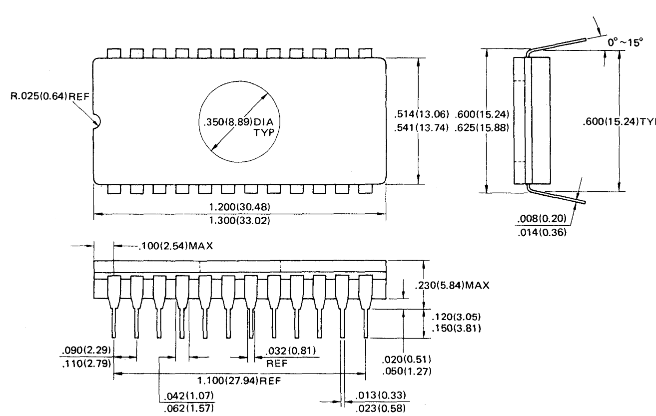
DIP-24C-A02

**24-LEAD CERAMIC
METAL SEAL
DUAL IN-LINE PACKAGE**



DIP-24C-C02

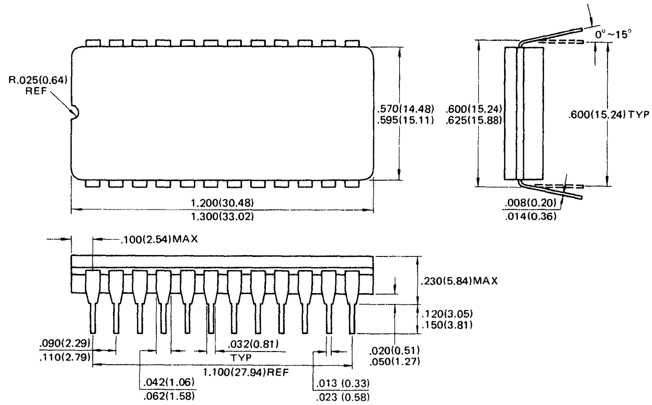
**24-LEAD CERDIP
WITH TRANSPARENT LID
DUAL IN-LINE PACKAGE**



Package Dimensions Dimensions in inches (millimeters)

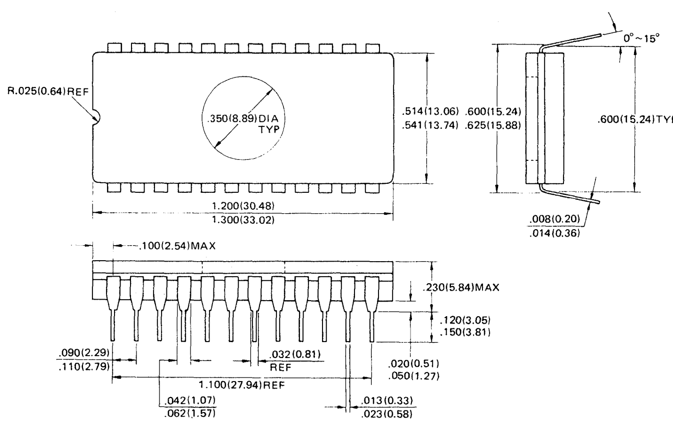
DIP-24C-C03

24-LEAD CERDIP DUAL IN-LINE PACKAGE



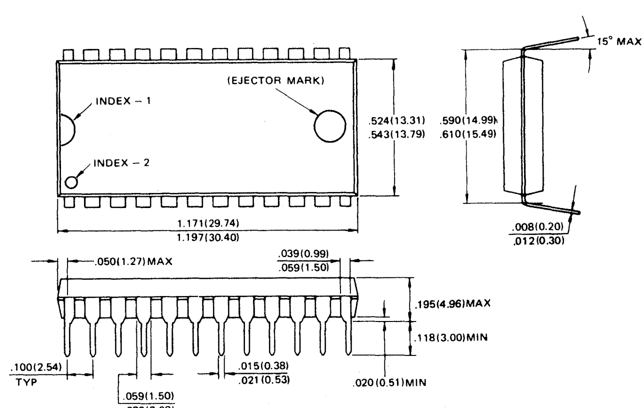
DIP-24P-M01

24-LEAD PLASTIC DUAL IN-LINE PACKAGE



DIP-24P-M02

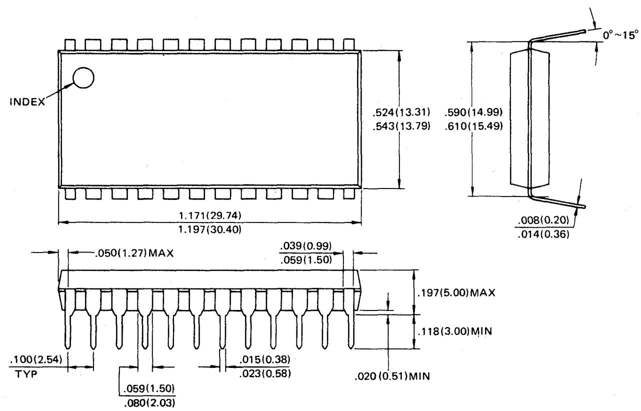
24-LEAD PLASTIC DUAL IN-LINE PACKAGE



Package Dimensions Dimensions in inches (millimeters)

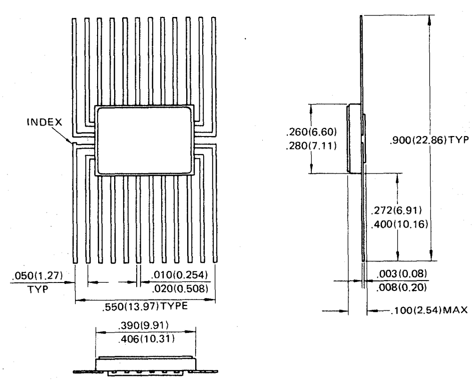
FPT-24-C02

24-LEAD CERDIP FLAT PACKAGE



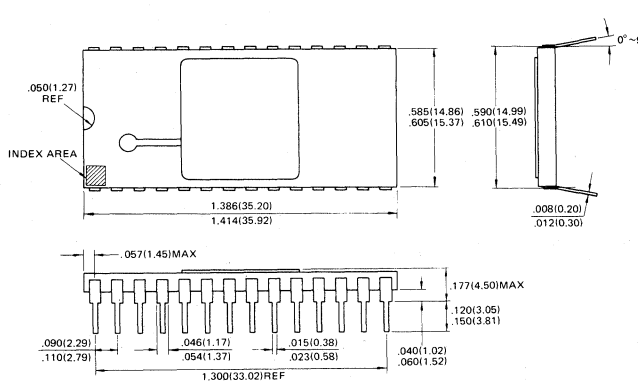
FPT-24C-F01

24-LEAD CERAMIC FRIT SEAL FLAT PACKAGE



DIP-28C-A01

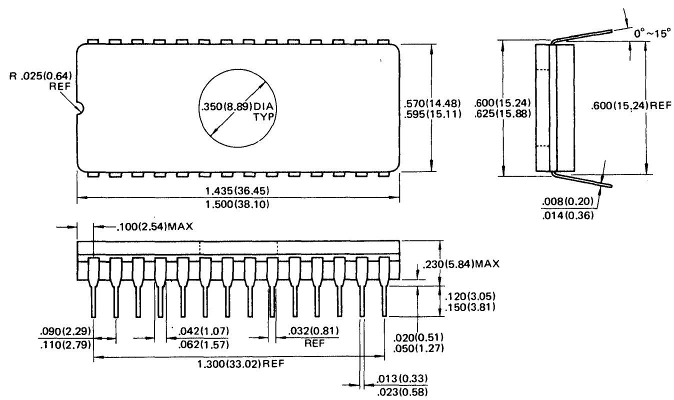
28-LEAD CERAMIC METAL SEAL DUAL IN-LINE PACKAGE



Package Dimensions Dimensions in inches (millimeters)

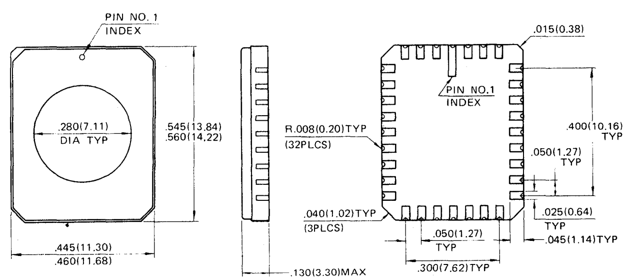
DIP-28C-C01

28-LEAD CERDIP
WITH TRANSPARENT LID
DUAL IN-LINE PACKAGE



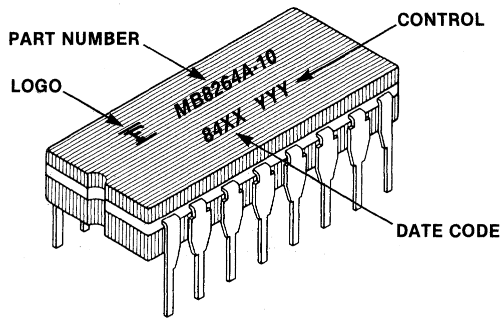
LCC-32C-A01

32-PAD CERAMIC
METAL SEAL
LEADLESS CHIP CARRIER



Ordering Information

Product Marking



Ordering Code

MB 8264-15 Z

- PACKAGE
  - C-CERAMIC
  - P-PLASTIC
  - Z-CERDIP
- PERFORMANCE VARIATIONS (WHEN USED)
  - E, H OR DASH NUMBERS DENOTE ACCESS TIME VARIATIONS
  - L-DENOTES LOW POWER
- DEVICE TYPE
- MANUFACTURER DESIGNATOR
  - MB-DEVICE TYPE IS FUJITSU INTERNAL NUMBER
  - MBM-DEVICE TYPE IS INDUSTRY STANDARD MEMORY NUMBER

Sales Office Listing

Field Sales Offices

HEADQUARTERS
Fujitsu Microelectronics, Inc.
3320 Scott Boulevard
Santa Clara, CA 95051
(408) 727-1700
Telex I/II: 910-338-0190

NORTHERN CALIFORNIA
Fujitsu Microelectronics, Inc.
595 Millich Drive
Suite 210
Campbell, CA 95008
(408) 866-5600

SOUTHERN CALIFORNIA
Fujitsu Microelectronics, Inc.
840 Newport Center Drive
Suite 460
Newport Beach, CA 92660
(714) 720-9688

ATLANTA
Fujitsu Microelectronics, Inc.
3169 Holcomb Bridge
Suite 506
Norcross, GA 30071
(404) 449-8539

AUSTIN
Fujitsu Microelectronics, Inc.
8240 Mopac Expwy. 395 G
Austin, TX 78759
(512) 343-0320

BOSTON
Fujitsu Microelectronics, Inc.
57 Wells Avenue
Newton Centre, MA 02159
(617) 964-7080

CHICAGO
Fujitsu Microelectronics, Inc.
1501 Woodfield Road
Suite 202, South Bldg. IV
Schaumburg, IL 60195
(312) 885-1500
TWX: 910-687-7378

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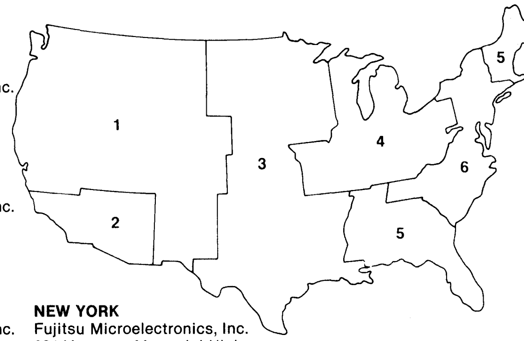
Fujitsu Microelectronics, Inc.
1101 East Arapaho Road
Suite 225
Richardson, TX 75081
(214) 669-1616

HOUSTON
Fujitsu Microelectronics, Inc.
10550 W. Office Drive
Suite 102
Houston, TX 77042
(713) 784-7111

MINNEAPOLIS
Fujitsu Microelectronics, Inc.
3460 Washington Avenue
Eagan, MN 55122
(612) 454-0323

NEW YORK
Fujitsu Microelectronics, Inc.
601 Veterans Memorial Highway
Hauppauge, NY 11788
(516) 361-6565
TWX: 510-227-1049

N. Cal	**1. (408) 866-5600**
S. Cal	**2. (714) 720-9688**
Dallas	**3. (214) 669-1616**
Chicago	**4. (312) 934-6400**
Boston	**5. (617) 964-7080**
New York	**6. (516) 361-6565**



Representatives

Arizona
Thom Luke Sales, Inc.
2940 N. 67th Place
Suite H
Scottsdale, AZ 85251
(602) 941-1901

California
Harvey King Inc.
8124 Miramar Road
San Diego, CA 92126
(619) 566-5252

NorComp Inc.
2975 Scott Blvd.
Santa Clara, CA 95050
(408) 727-7707

Colorado
Straube Associates
7970 Sheridan Ave.
Suite C
Westminster, CO 80003
(303) 426-0890

Connecticut
Comp Rep Associates
605 Washington Ave.
North Haven, CT 06473
(203) 239-9762

Georgia
Dixie Technical Marketing
925 Main Street, Suite 203
Stone Mountain, GA 30086
(409) 962-2530

Idaho
Cascade Components
2419 W. State Street, No. 10
Boise, ID 83702
(208) 343-9886

Illinois
ZMS Electronic Sales
3227 N. Frontage Road, #2702
Arlington Heights, IL 60004
(312) 394-4422

Indiana
Gaertner Associates
6505 E. 82nd Street, #107
Indianapolis, IN 46250
(317) 842-0373

Iowa
Electromec Sales Inc.
1500 2nd Ave., S.E.
Suite 205
Cedar Rapids, IA 52403
(319) 362-6413

Kansas
PMR Corporation
P.O. Box 6264
Overland Park, KS 66206
(913) 381-0004

PMR Corporation
P.O. Box 18089
Wichita, KS 67218
(316) 684-4141

Maryland
Component Sales, Inc.
3701 Old Court Rd., #14
Baltimore, MD 21208
(301) 484-3647

Massachusetts
Comp Rep Associates
100 Everett Street
Westwood, MA 02090
(617) 329-3454

Michigan
AP Associates
9880 E. Grand River
Brighton, MI 48116
(313) 229-6550

Minnesota
Electromec Sales, Inc.
101 W. Burnsville Parkway
Burnsville, MN 55337
(612) 894-8200

Missouri
PMR Corporation
P.O. Box 1539
Maryland Heights, MO 63043
(314) 569-1220

New Jersey
Technical Applications Marketing
389 Passaic Avenue
Fairfield, NJ 07006
(201) 575-4390

New Mexico
Straube Associates, Inc.
11701 Menaul Blvd. N.E.
Suite E
Albuquerque, NM 87112
(505) 292-0428

New York
Tech-Mark/Upstate Associates
P.O. Box 173
Mendon, NY 14506
(716) 624-3840

Technical Applications Marketing
1727 Veterans Highway
Suite 408
S. Hauppauge, NY 11722
(516) 348-0800

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3165 Linwood Road
Cincinnati, OH 45208
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Makin & Associates
5077 Olentangy River Road
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Columbus, OH 43214
(614) 459-2423

Makin & Associates
1640 Frankland Ave.
Suite 5
Kent, OH 44240
(513) 872-2424

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Olson, Ferree and Associates
2215 N.E. Cornell
Hillsboro, OR 97124
(503) 640-9660

Pennsylvania
Omni Sales
1014 Bethlehem Pike
Erdenheim, PA 19118
(215) 233-4600

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3509 S. Main Street
Salt Lake City, UT 84115
(810) 263-2640

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Olson, Ferree & Associates
12727 N.E. 20th
Suite 4
Bellevue, WA 98005
(206) 883-7792

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ZMS Electronic Sales
250 N. Sunnyslope Road, #337
Brookfield, WI 53005
(414) 782-2222

Canada
Pipe-Thompson Ltd.
5468 Dundas Street West
Suite 206
Islington, Ontario M9B 6E3
(416) 236-2355

Woodbery Electronics Sales Ltd.
107A-3700 Gilmore Way
Burnaby, BC V5G 4M1
(604) 430-3302

Puerto Rico
Comp Rep Associates
KQH8 Miradero
P.O. Box 724
Mayaguez, PR 00708
(809) 832-9529

Distributors

Arizona
Cetec Moltronics
3617 N. 35th Ave.
Phoenix, AZ 85017
(602) 272-7951

Marshall Industries
835 West 22nd Street
Tempe, AZ 85281
(602) 968-6181

Time Electronics Arizona
1203 W. Geneva Drive
Tempe, AZ 85252
(602) 967-2000

California
Cetec Electronics
3940 Ruffin Street
Suite E
San Diego, CA 92123
(619) 278-5020

Cetec Electronics
721 Charcot Avenue
San Jose, CA 95131
(408) 263-7373

Cetec Electronics
5610 E. Imperial Hwy
Southgate, CA 90280
(213) 773-6521

Image Electronics
15052 Red Hill Ave.
Unit A
Tustin, CA 92680
(714) 730-0303

Marshall Industries
8015 Deering Ave.
Canoga Park, CA 91304
(213) 999-5001

Marshall Industries
17321 Murphy Avenue
Irvine, CA 92741
(714) 556-6400

Marshall Industries
10105 Carroll Canyon Road
San Diego, CA 92131
(619) 578-9600

Marshall Industries
788 Palomar Ave.
Sunnyvale, CA 94086
(408) 732-1100

Pacesetter Electronics
3137 W. Warner Street
Santa Ana, CA 92704
(714) 557-7131

Time Electronics West
2410 E. Cerritos Ave.
Anaheim, CA 92806
(714) 937-0911

Time Electronics Norcal
1339 Moffett Park Drive
Sunnyvale, CA 94086
(408) 734-9888

Time Electronics West
19210 S. Van Ness
Torrance, CA 95051
(213) 320-0880

Western Microtechnology
10040 Bubb Road
Cupertino, CA 95014
(408) 725-1660

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Bell Industries
8155 West 48th Avenue
Wheatridge, CO 80033
(303) 424-1985

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7000 N. Broadway
Denver, CO 80221
(303) 427-1818

IEC JACO
5750 N. Logan St.
Denver, CO 80216
(303) 292-6121

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Village Lane
Barnes Industrial Park
Wallingford, CT 06492
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Milgray Connecticut
378 Boston Post Road
Orange, CT 06477
(203) 795-0711

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1101 NW 62nd Street
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Ft. Lauderdale, FL 33309
(305) 928-0661

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Orlando, FL 32805
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1850 Lee Road, Suite 104
Winter Park, FL 32789
(305) 647-5747

Time Electronics Florida
6610 N.W. 21st Avenue
Ft. Lauderdale, FL 33309
(305) 974-4800

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Milgray Atlanta
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Atlanta, GA 30338
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3336 Commercial Ave.
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Intercomp Inc.
2200 N. Stonington
Hoffman Estates, IL 60195
(312) 843-2040

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1261 Wiley Dr.
Schaumburg, IL 60195
(312) 490-0155

NEP Electronics
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Chicago, IL 60634
(312) 625-8400

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DEECO
2500 16th Ave., South West
Cedar Rapids, IA 52406
(319) 365-7551

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Milgray Kansas
6901 W. 63rd. Street
Overland Park, KS 66202
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8445 Helgerman
Gaithersburg, MD 20760
(301) 840-9450

Milgray Washington
11820 Parklawn Drive
Room 102
Rockville, MD 20852
(301) 468-6400

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Future Electronics Corp.
133 Flanders Road
Westboro, MA 01581
(617) 366-2400

Marshall Industries
One Wilshire Road
Burlington, MA 01830
(617) 272-8200

Milgray New England
79 Terrace Hall
Burlington, MA 01803
(617) 272-6800

Time Electronics New England
150C New Boston Street
Woodburn, MA 01801
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6731 28th St. S.E.
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Livonia, MI 48150
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Reptron Electronics
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Livonia, MI 48150
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Fairfield, NJ 07004
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Marshall Industries
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Mt. Laurel, NJ 08054
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10 Hooper Road
Endwell, NY 13760
(607) 754-1570

Marshall Industries
275 Oser Ave.
Hauppauge, NY 11787
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1260 Scottsville Road
Rochester, NY 14624
(716) 235-7620

Mast Distributors
215 Marcus Blvd.
Hauppauge, NY 11788
(516) 273-4422

Milgray Electronics
77 Schmitt Blvd.
Farmingdale, NY 11735
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Rome, NY 13440
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Marshall Industries
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Dayton, OH 45424
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Solon, OH 44139
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Reptron Electronics
830 Busch Court
Columbus, OH 43229
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Oregon
Marshall Industries
8230 S.W. Nimbus Ave.
Beaverton, OR 97005
(503) 644-5050

Moore Electronics
15824 S.W. Upper Boones Ferry Rd.
Lake Oswego, OR 97034
(503) 684-3100

Pennsylvania
Time Electronics Mid Atlantic
620 Parkway Ave.
Broomall, PA 19008
(215) 359-1200

Texas
Active Component Technology
4951 Airport Parkway
Suite 590
Dallas, TX 75248
(214) 980-1888

Active Component Technology
6448 Hwy. 290 E.
Bldg. A No. 108
Austin, TX 78723
(512) 452-5254

Marshall Industries
8705 Shoal Creek Blvd.
Suite 202
Austin, TX 78753
(512) 458-5654

Marshall Industries
14205 Proton Road
Dallas, TX 75234
(214) 233-5200

Marshall Industries
3698 Westchase Drive
Houston, TX 77036
(713) 789-6600

Washington
Marshall Industries
14102 NE 21st Street
Bellevue, WA 98007
(206) 747-9100

Wisconsin
Classic Components
2925 S. 160th Street
New Berlin, WI 53151
(414) 786-5300

Marsh Electronics
1563 S. 101st Street
Milwaukee, WI 53214
(414) 475-6000

Canada
Future Electronics Corporation
237 Hymus Blvd.
Pointe Claire, Quebec H9R 5C7
(514) 694-7710

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25 Howden Road Unit 5
Scarborough, Ontario M1R 3E8
(416) 751-2371