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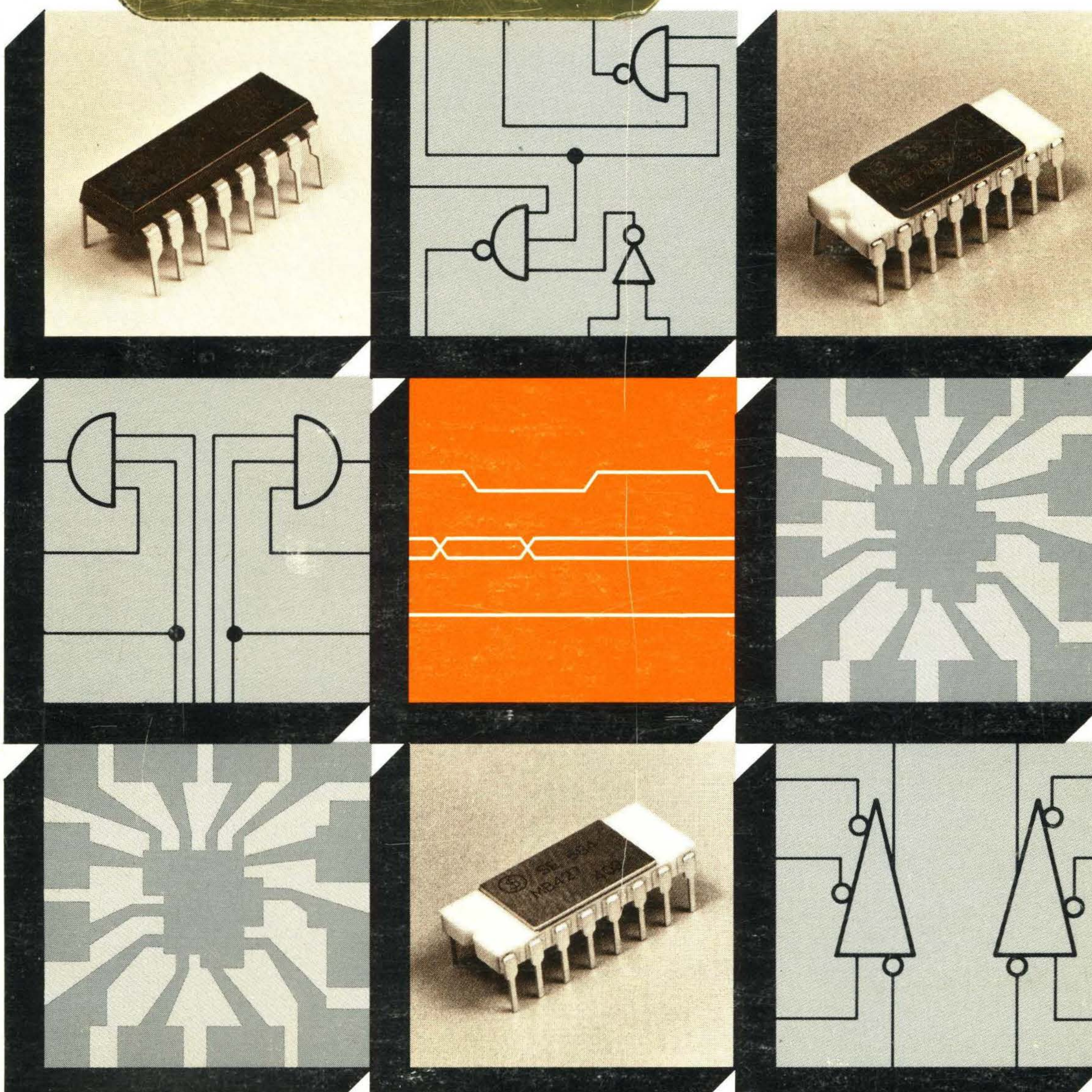
Fujitsu Integrated Circuit Product Catalog

FUJITSU



FUJITSU
Fujitsu Integrated Circuit Product Catalog

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FUJITSU

About Fujitsu America Inc.

Fujitsu-America Incorporated – FAI – is the U.S. marketing arm of Fujitsu Limited of Tokyo, Japan. Fujitsu Limited manufactures and markets data processing and telecommunications systems, and the components these systems use. The Company is the largest manufacturer of computer systems in Japan, with annual sales that exceed $1.2 billion.

Established in 1935 as a communications equipment firm, Fujitsu's expansion into EDP was based on extensive R&D and marketing experience. The company is using its strength in both telecommunications and computing to maximize, worldwide, its opportunities in these rapidly growing markets.

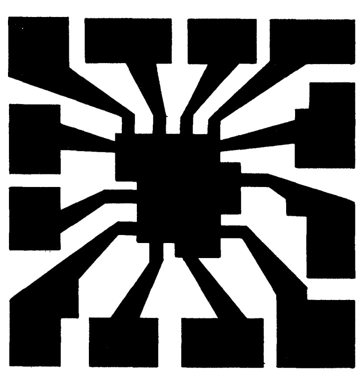
Major basis for its recent, 15%-per-year growth in sales has been the company's innovative technology. This is especially true in integrated circuits – ICs. Shipments of the company's 'M' series – the world's first fourth-generation, all-LSI, ultra-large-scale computer systems – began in 1975 to some of the world's most demanding users.

Until recently, design and development of Fujitsu ICs was dictated by its internal computer and telecommunications needs. The new Fujitsu policy of selling ICs to independent customers means that designs are now dictated primarily by market requirements. A good example is FAI'S new 16-pin, 16K RAM, comparable to the most popular type available and second-sourced by several U.S. manufactuers.

Fujitsu's established systems know-how helps in creating specifications for its ICs that are truly meaningful for IC memory users. It stems from the close relationship with the computer operation, and results in genuinely 'state-of-the-art' designs destined to become future industry standards.

Among Japan's approximately 30 IC manufactuers, Fujitsu ranks among the top five. The company's capabilities in IC development and manufacture are broad – process technologies at Fujitsu include both MOS and bipolar; products include RAMs, ROMSs, PROMs and EROMs, as well as a broad range of memory-peripheral circuits. Fujitsu's special strength has been the ability to handle advanced processes with high-yield, complex designs in which the company is well placed to offer highly competitive products.

Fujitsu's excellent reputation for high-quality, reliable products results from its allocating almost 10% of its annual budget to quality control and reliability assurance. These programs are costly, but make a significant difference in Fujitsu's ability to offer ICs that come as close to 'Zero Defects' as technology permits. The company intends to remain a quality manufacturer.



Product Reliability

To deliver ICs to customers that will operate at the highest reliability levels, comprehensive Reliability and Quality Assurance programs are applied by Fujitsu from the start of product design all the way to manufacture and final test. Reliability statistics are gathered thorughout product life, in customer sockets, to provide detailed life-expectancy data for users world-wide.

Design considerations that affect IC reliability include process technology, circuit-element structure and characteristics, circuit layout, assembly and packaging, and the final applications. Each phase is subject to critical analysis before product designs are accepted within Fujitsu.

Reliable processes are insisted upon at the very start, based on statistics gained over the production of hundreds of millions of ICs. After sample lots of a new product have been made — on 'pilot' lines — trial full-scale production is initiated. Three separate, major runs are undertaken for internal certification and approval. Product integrity is further assured during subsequent routine, full-scale manufacture by 100% in-process testing by Manufacturing, sample in-process testing by QC and between-process testing by QC and test-and-inspection groups.

Process mechanization helps reduce subjective variations implicit in human-supervised processes. Effective QC is further insured by regularly scheduled calibration of all jigs, tools, meters, scales, gauges and test equipment used in manufacture and QC measurement. Clean-room and DI-water purity are similarly scrutinized. Lot assurance testing, failure analysis and similar programs are used extensively, to maintain highest continuing standards. Worker discipline, at all manufacture, QC and final-test stages, also insures consistent quality.

At Fujitsu, reliability is designed and manufactured into the product, not 'burned in' or 'tested in' after the fact. For the user, the end result is remarkable. Statistically, over hundreds of millions of device hours, Fujitsu ICs offer in-use failure rates as much as *an order of magnitude* lower than competitive devices of equivalent characteristics.

How to Use Catalog

This is a comprehensive catalog of Fujitsu-America product data. Information has been arranged by product area, as summarized in the condensed 'Selector Guide' at the front, which contains specific help on how to find the detailed technical data within the catalog itself. Ordering, sales and warranty information is included, along with a brief discussion of FAI product reliability. More details on these aspects of doing business with FAI will be found in the Terms and Conditions of sale, accompanying each order accepted by FAI. A detailed brochure on reliability is available on request, and may be asked for using the business-reply cards at the back of this catalog. Our local representatives appear on a separate list inserted into this catalog.

All information is current as of the date on each individual product data sheet, but FAI reserves the right to change data without notice at any time. If you need a particular type of IC product to replace one or more original FAI products already in your boards, please do not assume that the absence of the original type number from this catalog or the selector guide indicates obsolescence. New, improved devices having different type numbers are continually being introduced that provide superior performance or life, and may be fully compatible with earlier types. Consult your local representative, or FAI, in case of difficulty.

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Ordering Information

ORDERING

All orders and inquiries should be addressed to our representative in your area, or to FAI at its offices in Santa Clara, California. We are not bound by your order until accepted, in writing, by an authorized FAI employee in Santa Clara. On acceptance, orders may not be cancelled in whole or in part, except on default of FAI.

PRICES

Prices are quoted FOB our offices in Santa Clara, and are subject to change without notice. Minimum charge per order is $50.

TAXES

All prices, orders and billings exclude federal, state and local, sales, use and similar taxes, which will be invoiced as separate, additional items unless FAI receives proper tax-exemption certificates before shipment.

PAYMENT

Payment terms are net 30 days from invoice date, but customers will receive a 2% discount on payments received by FAI within 10 days. Interest on overdue accounts is charged at the rate of 10% per annum.

SHIPPING

All shipments are FOB our Santa Clara offices. If the shipping method is not specified by the purchaser, items will be shipped in the most advantageous manner.

RETURNS

Products may be returned for adjustment only with prior FAI approval in writing, and subject to our warranty terms and conditions. All returns to FAI must be prepaid.

WARRANTY

FAI warrants all its IC components against defects in materials and workmanship for one year from delivery date. Our liability covers replacement, repair or credit for the original purchase price provided FAI is notified promptly, in writing, of the defect discovered by the customer. Defective components must be returned within one year of delivery, prepaid, and should satisfy our examination to assure us that defects were not caused by improper use.

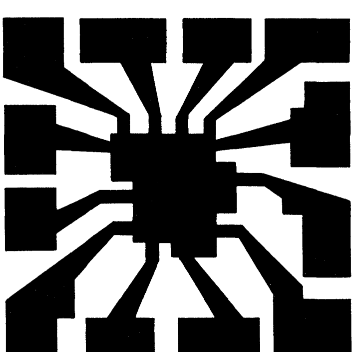
PATENTS

Customers are expected to hold FAI harmless against expenses, damages, costs or losses resulting from suits brought for infringements of patents, designs, trademarks, copyrights or trade names, or for unfair competition arising from FAI's compliance with the customer's designs, specifications or instructions.

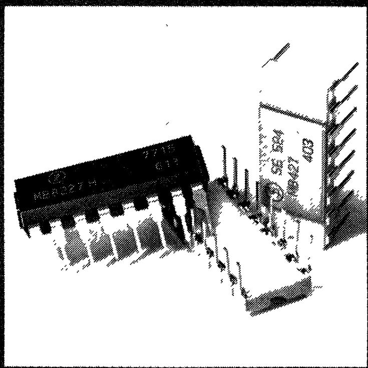
APPLICATIONS ENGINEERING

FAI's staff of applications engineers is available as a service to customers. The staff is fully experienced in applications for FAI products in virtually all computer, computer-peripherals and telecommunications uses.

What is the best FAI memory device for your particular application? How can FAI memory-peripheral circuitry be planned and designed for efficiency and minimum parts types? What are the compromises in FAI part types between speed and cost in your particular application? Is there a better way FAI can suggest that will solve the specific memory or memory-related design problem you're facing? These are the kinds of questions that the FAI Applications Engineering staff faces, and answers, every day. Both in Santa Clara and in Japan, the group is ready to serve you.



Memory Products Selector Guide



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MOS Memories

DYNAMIC RANDOM ACCESS MEMORIES

Silicon Gate NMOS

Device Number	Description	Organization	Access Time Max (ns)	Cycle Time Min (ns)	Power Supplies (V)	Power Dissipation Max (mW)	Clock Level	Output Level	Case	Alternate Source	PG. NO.
MB 8107N E H Y	4096 Bit Dynamic High Speed with Single Phase Clock	4096x1	300 250 200 150	470 430 400 350	+12, ±5	680 680 680 760	MOS	TTL 3-State	DIP22-A	I 2107B TI 4060	1-3
MB 8215E H*	4096 Bit Dynamic High Speed with Single Phase Clock	4096x1	100 70	220 220	+12, −5.2, +7	530 530	MOS	Current Mode	DIP22-A	—	1-11
MB 8224N E H*	4096 Bit Dynamic High Speed	4096x1	280 230 200	450 370 350	+12, ±5	460 460 460	TTL	TTL 3-State	DIP16-A,B,D	MK 4096	1-23
MB 8227N E H	4096 Bit Dynamic High Speed (gated $\overline{CAS}$, $\overline{RAS}$ Only Refresh and Page Mode Capability)	4096x1	250 200 150	375 375 320	+12, ±5	470 470 470	TTL	TTL 3-State	DIP16-A,B,D	MK 4027	1-32
MB 8116E H Y*	16K Bit Dynamic High Speed	16384x1	200 150 120	375 375 320	+12, ±5	460 460 460	TTL	TTL 3-State	DIP16-A,B	MK 4116	1-44

* Note: Coming Soon

STATIC RANDOM ACCESS MEMORIES

Silicon Gate NMOS

Device Number	Description	Organization	Access Time Max (ns)	Cycle Time Min (ns)	Power Supplies (V)	Power Dissipation Max (mW)	Output Level	Case	Alternate Source	PG. NO.
MB 8101N E*	1024 Bit Static RAM	256x4	450 250	450 250	+5	370 370	TTL 3-State	DIP22-A	I 2101	1-56
MB 8111N E*	1024 Bit Static RAM	256x4	450 250	450 250	+5	370 370	TTL 3-State	DIP18-A	I 2111	1-64
MB8102	1024 Bit Static RAM	1024x1	450	450	+5	370	TTL 3-State	DIP 16-A, B	I 2102	1-71
MB 8112N E*	1024 Bit Static RAM	256x4	450 250	450 250	+5	370 370	TTL 3-State	DIP16-A, B	I 2112	1-79
MBM 2115N E H Y	1024 Bit Static Ultra Fast Low Power	1024x1	120 95 70 45	120 95 70 45	+5	340 340 520 680	TTL Open-Drain	DIP16-A, B	I 2115	1-87
MBM 2125N E H Y	1024 Bit Static Ultra Fast Low Power	1024x1	120 95 70 45	120 95 70 45	+5	340 340 520 680	TTL 3-State	DIP16-A, B	I 2125	
MB 8114*	4096 Bit Static Ultra Fast Low Power	1024x4	150	150	+5	480	TTL 3-State	DIP18-A	I 2114	1-94

* Note: Coming Soon

Interface Memory Compatibility Table for Dynamic RAM's					
Driver		Memory		Sense Amp.	
TTL	ECL	Type	Bits	TTL	ECL
MB 8907P*	–	MB 8107	4096	NR	–
NR	–	MB 8224	4096	NR	–
–	MB 8903/8909*	MB 8215	4096	–	MB 8916

NR: Not Required * Note: Clock Driver

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READ ONLY MEMORIES

Device Number	Description	Organization	Access Time Max (ns)	Power Supplies (V)	Power Dissipation Max (mW)	Programming Time (sec)	Output Level	Case	Alternate Source	PG.NO.
Silicon Gate NMOS										
MB 8518E H	8192 Bit Erasable ROM	1024x8	650 450	+12, ±5	800 (Typ)	100	TTL 3-State	DIP24-A	I 2708	1-99
MB 8308N E*	8192 Bit Mask ROM	1024x8	450 250	+12, ±5	775	—	TTL 3-State	DIP24-B	I 2308	1-110

* Note: Coming Soon

Bipolar Memories

RANDOM ACCESS MEMORIES

Device Number	Description	Organization	Access Time Max (Typ) (ns)	Chip Select Access Time Max (ns)	Power Supply (V)	Power Dissipation Max (mW)	Input Level	Output Level	Case	Alternate Source	PG.NO.
Bipolar											
MB 7047	128 Bit ECL Ultra Fast	128x1	14 (9)	8.5	−5.2	520	ECL	ECL	DIP16-A,B	MCM 10147	2-4
MB 7042	256 Bit ECL Ultra Fast	256x1	15 (9)	9	−5.2	750	ECL	ECL	DIP16-A,B	MCM 10152 MCM 10144	2-12
MBM 10410	256 Bit ECL	256x1	35(20)	12	−5.2	680	ECL	ECL	DIP16-A,B	F 10410	2-20
MBM 10415	1024 Bit ECL	1024x1	60(35)	30	−5.2	780	ECL	ECL	DIP16-A,B	F 10415	2-26
MBM 10415A	1024 Bit ECL	1024x1	35(25)	10	−5.2	780	ECL	ECL	DIP16-A,B	F 10415A	
MBM 93415	1024 Bit TTL	1024x1	70(40)	40	+5	815	TTL	TTL Open Coll.	DIP16-A,B	F 93415	2-34
MBM 93415A	1024 Bit TTL	1024x1	45(30)	30	+5	815	TTL	TTL Open Coll.	DIP16-A,B	F 93415A	
MB7071N H	1024-Bit ECL	256x4 256x4	15(12) 10 (7.5)	—	−5.2	1000	ECL	ECL	QIT24	—	2-42
MB7072 N H	1024 Bit ECL	256x4 256x4	15(12) 10 (7.5)	—	−5.2	1000	ECL	ECL	DIP 22-A	—	

PROGRAMMABLE READ ONLY MEMORIES

Device Number	Description	Organization	Access Time Max (Typ) (ns)	Power Supply	Power Dissipation Max (mW)	Bit Programming Time Typ (μs)	Chip Programming Time Max (ms)	Output Level	Case	Alternate Source	PG.NO.
Bipolar											
MB 7051	256 Bit TTL	32x8	75(40)	+5	525	10	256	3-State	DIP16-A,B,C	IM 5610	2-50
MB 7056	256 Bit TTL	32x8	75(40)	+5	525	10	256	Open Coll.	DIP16-A,B,C	IM 5600	
MB 7052	1024 Bit TTL	256x4	70(40)	+5	685	10	1024	3-State	DIP16-A,B,C	IM 5623	2-62
MB 7057	1024 Bit TTL	256x4	70(40)	+5	685	10	1024	Open Coll.	DIP16-A,B,C	IM 5603	
MB 7053	2048 Bit TTL	512x4	70(40)	+5	735	10	2048	3-State	DIP16-A,B,C	IM 5624	2-74
MB 7058	2048 Bit TTL	512x4	70(40)	+5	735	10	2048	Open Coll.	DIP16-A,B,C	IM 5604	
MB 7054	4096 Bit TTL	1024x4	70	+5	685	10	4096	3-State	DIP18-A,C	IM 56S26	2-86
MB 7059	4096 Bit TTL	1024x4	70	+5	685	10	4096	Open Coll.	DIP18-A,C	IM 56S06 μPD 406D	
MB7055	8192 Bit TTL	1024x8	250	+5	500	10	8192	3-State	DIP 24-B	I 2708	2-98
MB7060	8192 Bit TTL	1024x8	250	+5	500	10	8192	Open Coll.	DIP 24-B	—	

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Interface Devices

MEMORY PERIPHERAL CIRCUITS

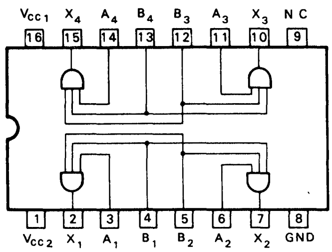
Device Number	Description	Signal Level	Logic	Supply Voltage (V)	Characteristics	Case	PG. NO.
MB8901	Quadruple TTL-MOS Level Shifter/Driver	TTL/MOS	NAND	V_{CC1}=5 V_{CC2}=9~17	t_{PHL}=20nsMAX t_{PLH}=23nsMAX (at C_L=300pF, t_C=600ns)	DIP16-A,C	3-3
MB 8902	Quadruple TTL-MOS Level Shifter/Driver	TTL/MOS	AND	V_{CC1}=5 V_{CC2}=9~17	t_{PHL}=20nsMAX t_{PLH}=23nsMAX (at C_L=300pF, t_C=200ns)	DIP16-A,C	3-9
MB 8907P	Quadruple TTL-MOS Level Shifter/Driver	TTL, DTL /MOS	NAND	V_{CC}=5 V_{DD}=9~17	t_{PHL}=23nsMAX t_{PLH}=27nsMAX (at C_L=300pF)	DIP16-A,C	3-15
MB 8909	Dual 2 Input Positive NOR CML to MOS Level Shifter	CML/MOS	NOR	V_{CC}=5 V_{DD}=7~13 V_{EE}=-5.2	t_{PHL}=17nsMAX t_{PLH}=20nsMAX (at C_L=300pF, t_C=250ns)	DIP16-A,C	3-21
MB 8903	Quadruple 2 Input or ECL to MOS Level Shifter/Driver	ECL/MOS	OR	V_{CC}=5 V_{EE}=-5.2	t_{PHL}=18nsMAX t_{PLH}=13nsMAX (at C_L=300pF)	DIP16-A,C	3-25
MB 8911	Dual Line Receiver (TTL Compatible, Open Collector Output)	TTL	—	V_{CC}=5 V_{EE}=-6.0	t_{PHL}=26nsMAX t_{PLH}=28nsMAX (at C_L=15pF)	DIP14-A	3-32
MB 8912	Dual Digit Driver/Sense Amplifier (TTL Compatible)	TTL	—	V_{CC}=5 V_{EE}=-5.2	trd=22nsMAX (at C_L=30pF)	DIP16-A,C	3-36
MB 8915	Dual Digit Driver/Sense Amplifier (TTL Compatible, Open Collector Output)	TTL	—	V_{CC}=5 V_{EE}=-6.0	trd=27nsMAX (at C_L=15pF)	DIP16-A,C	3-39
MB 8916	Dual Sense Amplifier with Read Strobe (ECL Compatible)	ECL	—	V_{CC}=5 V_R=8 V_{EE}=-5.2	trd=5nsTYP (at C_L=15pF)	DIP16-A,C	3-54

PERIPHERAL INTERFACE CIRCUITS

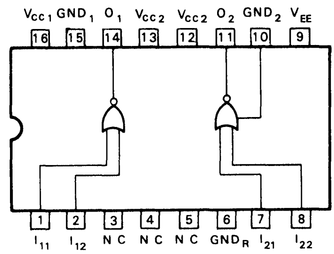
Device Number	Description	Signal Level	Characteristics (T_A=0~70° C)				Case	Alternate Source	
			Supply Voltage (V)	Fan-Out	Power Dissipation (mW/gate)	tpd			
MB 424	4 Bit Bus Driver/Receiver	TTL	5.0	I_{OL}=40mA C_L=300pF	60	15	DIP16-A,B,C,D	8T26	3-59
MB 425	4 Bit Bidirectional Bus Driver (non Inverting)	TTL	5 0	I_{OL}=50mA C_L=300pF	85	17	DIP16-A,B,C,D	I 3216/8216	3-69
MB 426	4 Bit Bidirectional Bus Driver (Inverting)	TTL	5.0	I_{OL}=50mA C_L=300pF	70	15	DIP16-A,B,C,D	I 3226/8226	3-80
MB 471	8 Bit Input/Output Port	TTL	5.0	I_{OL}=16mA	400*	20	DIP24-B	I 8212/3212	3-91
MB 485	Hex Three-State Buffer	TTL	5.0	I_{OL}=48mA	50	8	DIP16-A,B,C,D	8T95	
MB 486	Hex Three-State Inverter	TTL	5.0	I_{OL}=48mA	40	8	DIP16-A,B,C,D	8T96	
MB 487	Hex Three-State Buffer	TTL	5.0	I_{OL}=48mA	60	8	DIP16-A,B,C,D	8T97	
MB 488	Hex Three-State Inverter	TTL	5.0	I_{OL}=48mA	50	8	DIP16-A,B,C,D	8T98	3-108

* Note: Total Power Dissipation per Package

Pin Configurations



MB 8901/8902/8907P



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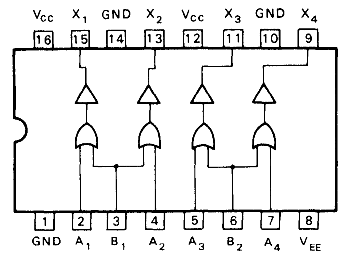
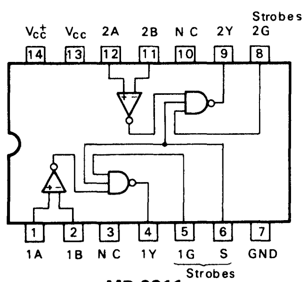
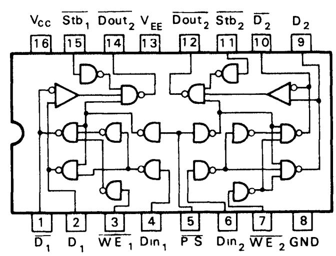


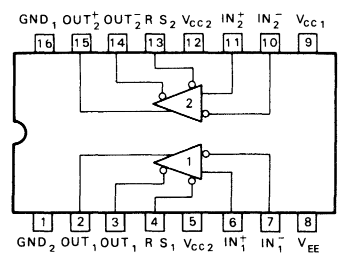
MB 8903



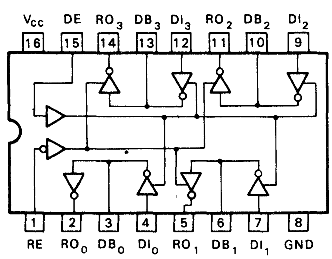
MB 8911



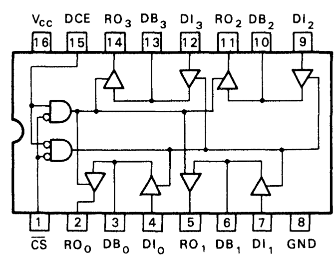
MB 8912/8915



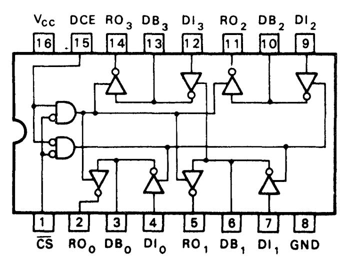
MB 8916



MB 424



MB 425



MB 426

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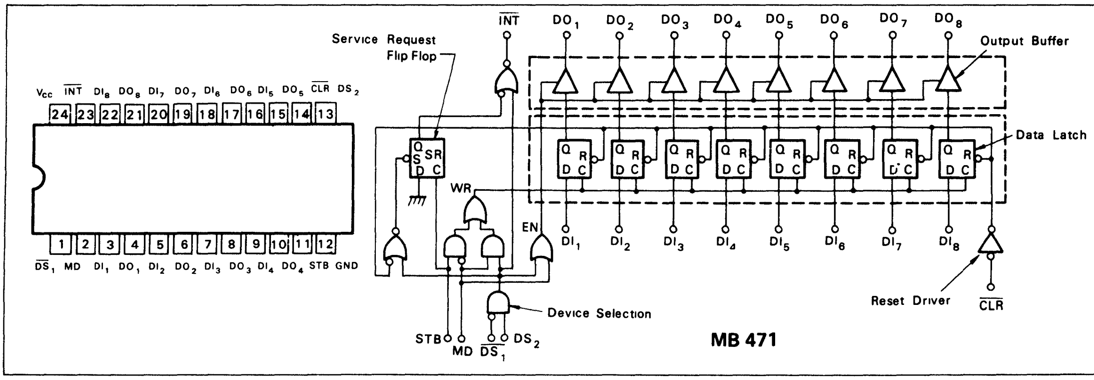
Pin Configurations (con't)



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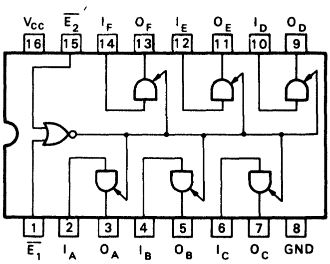
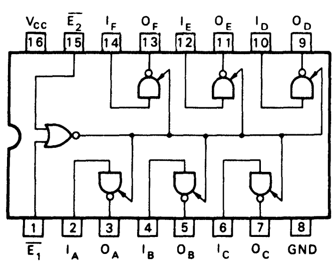


MB 485



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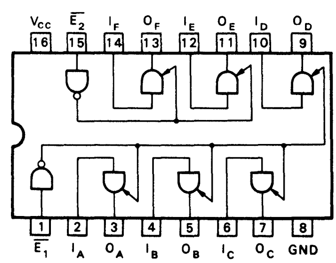

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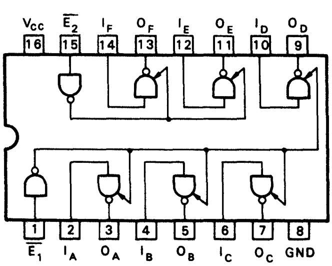
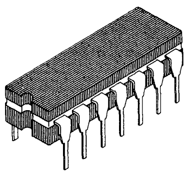
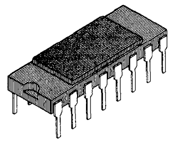


MB 488

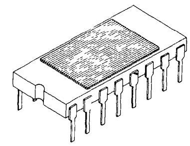
Package Designs



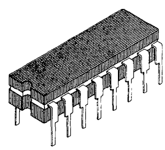
Case DIP14-A
CERDIP



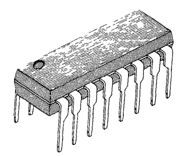
Case DIP 16-A
Ceramic (Frit seal)



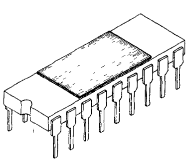
Case DIP16-B
Ceramic (Metal Seal)



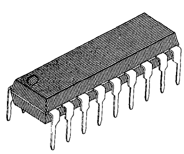
Case DIP16-C
CERDIP



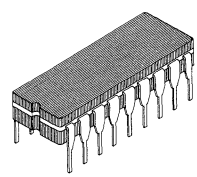
Case DIP16-D
Molded Plastic



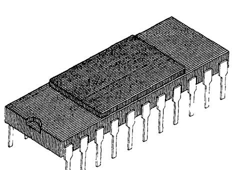
Case DIP18-A
Ceramic (Metal Seal)



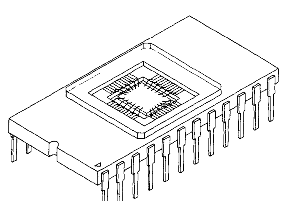
Case DIP18-B
Molded Plastic



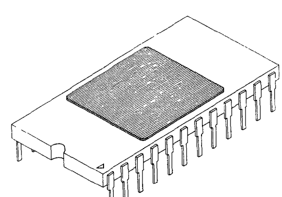
Case DIP18-C
CERDIP



Case DIP22-A
Ceramic (Frit Seal)



Case DIP24-A
Ceramic
(with transparent lid)



Case DIP24-B
Ceramic (Metal Seal)

FUJITSU

MOS Memories

MOS Memories

FUJITSU

MOS 4096-BIT DYNAMIC RANDOM ACCESS MEMORY

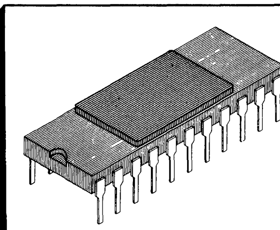
MB 8107N/E/H/Y

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The Fujitsu MB 8107 is a high speed 4096-word by 1-bit dynamic random access memory (RAM) using N-channel silicon gate MOS processing technology with substrate biasing. The MB 8107 is designed for memory applications where low cost and large bit storage are important design objectives.

The device is packaged in a ceramic, hermetically-sealed 22-pin dual-in-line package, and its performance is specified over a temperature range of 0°C to 70°C (ambient). Since the cell operation is dynamic storage, it requires periodic refreshing; in order to assure data retention at 70°C ambient, all combinations of addresses A_0 to A_5 must be exercised within 2 milliseconds.

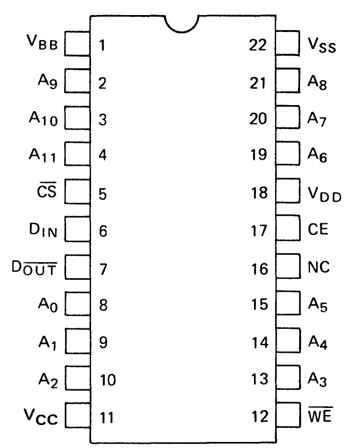
- High-density 4096 x 1 organization
- TTL compatible interface (except $\overline{CE}$)
- $\overline{CS}$ (Chip Select) lead simplifies memory expansion
- Standard 22-pin DIP package
- Fully decoded — on-chip address decode
- Three-state TTL compatible output
- Second source to 4060 and 2107



CASE DIP22-A
CERAMIC PACKAGE

MOS Memories

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Input/Output with Respect to V_{BB}	V_{IN}, V_{OUT}	-0.3 to +22	VDC
V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	–	-0.3 to +22	VDC
Temperature Under Bias	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Power Dissipation	P_D	1.25	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	11.4	12.0	12.6	V
	V_{CC}	4.75	5.0	5.25	V
	V_{BB}	−4.75	−5.0	−5.25	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1.0	—	0.6	V
CE Input High Voltage	V_{IHC}	$V_{DD}-1$	—	$V_{DD}+1$	V
CE Input Low Voltage	V_{ILC}	−1.0	—	1.0	V

DC CHARACTERISTICS

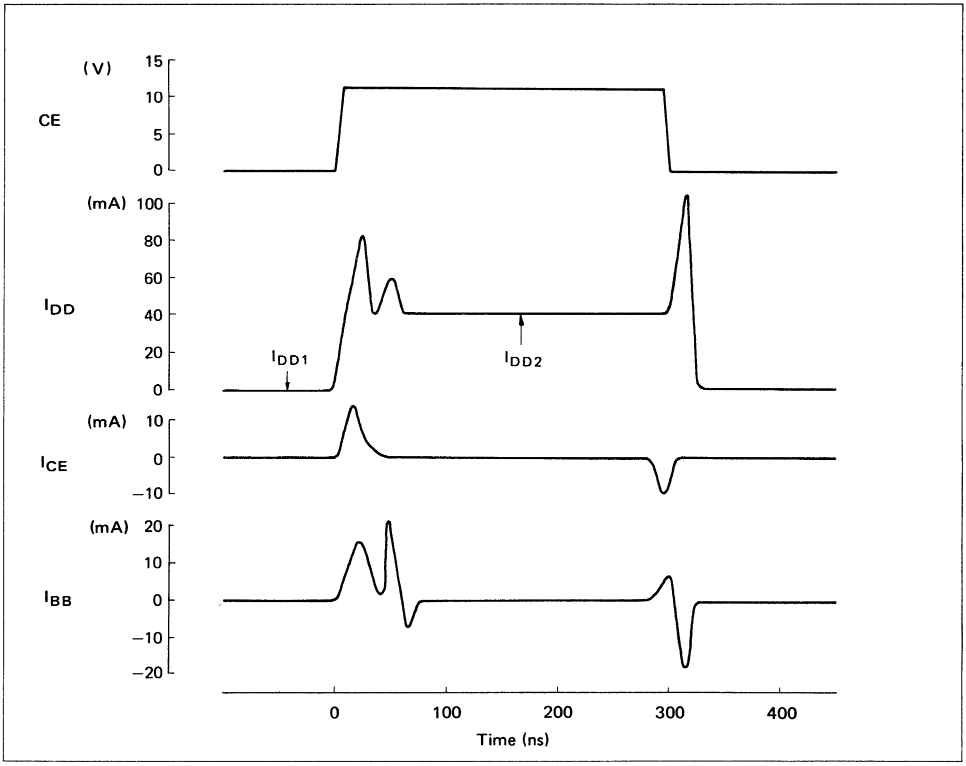
Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (except CE) ($CE = V_{ILC}$ or V_{IHC}, $V_{IN} = 0 \sim V_{IH}$)		I_{IL}	—	.01	10	μA
Input Leakage Current (CE)		I_{ILC}	—	.01	2	μA
Output Leakage Current ($CE = V_{ILC}$ or $\overline{CS} = V_{IH}$, $V_{OUT} = 0 \sim V_{CC}$)		I_{OL}	—	.01	10	μA
Output Low Voltage ($I_{OL} = 2.2$ mA)		V_{OL}	0.0	—	0.45	V
Output High Voltage ($I_{OH} = -2.2$ mA)		V_{OH}	2.4	—	V_{CC}	V
V_{DD} Supply Current ($CE = -1.0 \sim .6$ V, $V_{IN} = 0 \sim V_{IH}$)		I_{DD1}	—	110	200	μA
V_{DD} Supply Current ($CE = V_{IHC}$, $\overline{CS} = V_{IL}$)	MB8107N/E/H	I_{DD2}	—	40	60	mA
	MB8107Y			45	65	
Average V_{DD} Current (Min. Cycle t_T = 20ns, $T_A = 25°C$	MB8107N/E/H	I_{DDAV}	—	36	54	mA
	MB8107Y			38	60	
V_{CC} Supply Current ($CE = V_{ILC}$ or $\overline{CS} = V_{IH}$)		I_{CC}	—	.01	10	μA
V_{BB} Supply Current		I_{BB}	—	—	100	μA

Note: When chip is selected, V_{CC} supply current is dependent on output loading; V_{CC} is connected to the output buffer only.

CAPACITANCE (T_A = 25°C; f = 1MHz; V_{DD} = 12V; V_{CC} = 5V; V_{SS} = OV; V_{BB} = -5V)

Parameter	Symbol	Typ	Max	Unit
Address Capacitance, $\overline{CS}$ ($V_{IN} = V_{SS}$)	C_{AD}	—	6	pF
CE Capacitance ($V_{IN} = V_{SS}$)	C_{CE}	—	25	pF
Data Output Capacitance ($V_{\overline{OUT}}$ = OV)	$C_{\overline{OUT}}$	—	7	pF
D_{IN} and $\overline{WE}$ Capacitance ($V_{IN} = V_{SS}$)	C_{IN}	—	10	pF

CURRENT CHARACTERISTICS



AC CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

READ, WRITE and READ MODIFY WRITE CYCLES

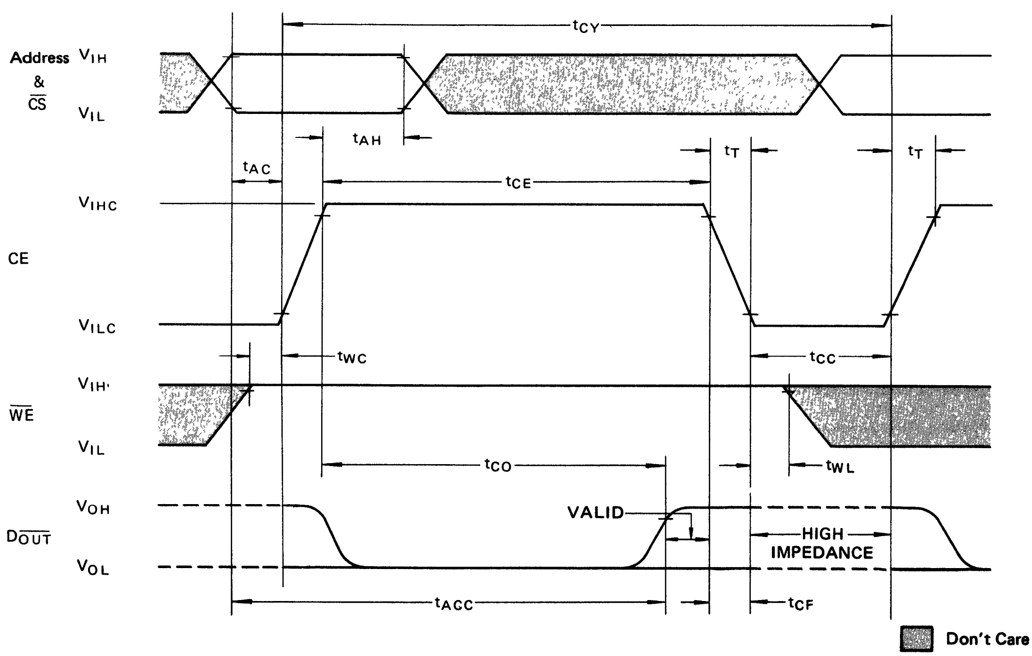
Parameter	Symbol	MB 8107N		MB 8107E		MB 8107H		MB 8107Y		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Time Between Refresh	t_{REF}	—	2	—	2	—	2	—	2	ms
Address to CE Set Up Time	t_{AC}	0	—	0	—	0	—	0	—	ns
Address Hold Time	t_{AH}	50	—	50	—	50	—	50	—	ns
CE Off Time	t_{CC}	130	—	130	—	130	—	130	—	ns
CE Transition Time	t_T	10	40	10	40	10	40	10	40	ns
CE Off to Output High Impedance State	t_{CF}	0	—	0	—	0	—	0	—	ns

Note: t_{AC} is measured from end of address transition.

READ CYCLE (C_L = 50pF; Load = One TTL Gate; Ref = 2.0V; $t_{ACC} = t_{AC} + t_{CO} + 1t_T$; t_T = 20ns)

Parameter	Symbol	MB 8107N		MB 8107E		MB 8107H		MB 8107Y		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	t_{CY}	470	—	430	—	400	—	350	—	ns
CE On Time	t_{CE}	300	4000	260	4000	230	4000	180	4000	ns
CE Output Delay	t_{CO}	—	280	—	230	—	180	—	130	ns
Address to Output Access	t_{ACC}	—	300	—	250	—	200	—	150	ns
CE to $\overline{WE}$	t_{WL}	0	—	0	—	0	—	0	—	ns
$\overline{WE}$ to CE On	t_{WC}	0	—	0	—	0	—	0	—	ns

READ CYCLE TIMING DIAGRAM

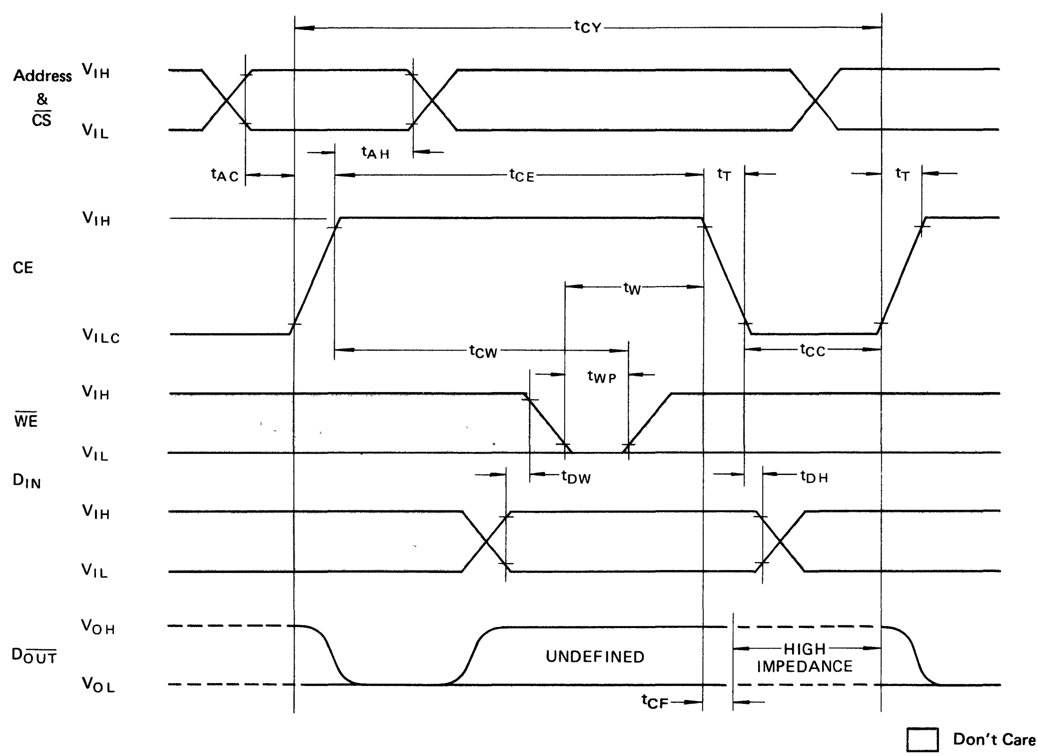


WRITE CYCLE (t_T = 20ns)

Parameter	Symbol	MB 8107N		MB 8107E		MB 8107H		MB 8107Y		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	t_{CY}	470	—	430	—	400	—	350	—	ns
CE On Time	t_{CE}	300	4000	260	4000	230	4000	180	4000	ns
$\overline{WE}$ to CE Off	t_W	180	—	160	—	150	—	130	—	ns
CE to $\overline{WE}$	t_{CW}	150	—	150	—	130	—	100	—	ns
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0	—	0	—	0	—	0	—	ns
D_{IN} Hold Time	t_{DH}	0	—	0	—	0	—	0	—	ns
$\overline{WE}$ Pulse Width	t_{WP}	70	—	60	—	50	—	50	—	ns

Note: If $\overline{WE}$ is low before CE goes high, then D_{IN} must be valid when CE goes high.

WRITE CYCLE TIMING DIAGRAM



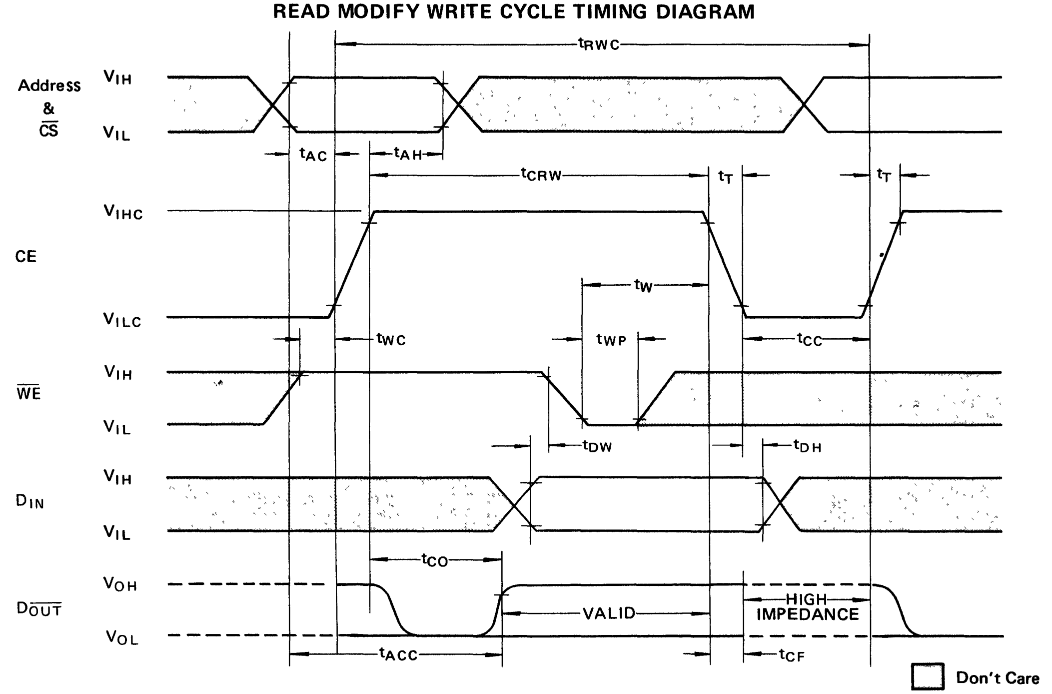
MOS Memories

READ MODIFY WRITE CYCLE (C_L = 50pF; Load = One TTL Gate; Ref = 2.0V; $t_{ACC} = t_{AC} + t_{CO} + 1t_T$: t_T = 20ns)

Parameter	Symbol	MB 8107N		MB 8107E		MB 8107H		MB 8107Y		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
RMW Cycle	t_{RWC}	650	—	580	—	520	—	470	—	ns
CE Width During RMW	t_{CRW}	480	4000	410	4000	350	4000	300	4000	ns
$\overline{WE}$ to CE On	t_{WC}	0	—	0	—	0	—	0	—	ns
$\overline{WE}$ to CE Off	t_W	180	—	160	—	150	—	130	—	ns
$\overline{WE}$ Pulse Width	t_{WP}	70	—	60	—	50	—	50	—	ns
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0	—	0	—	0	—	0	—	ns
D_{IN} Hold Time	t_{DH}	0	—	0	—	0	—	0	—	ns
CE to Output Delay	t_{CO}	—	280	—	230	—	180	—	130	ns
Access Time	t_{ACC}	—	300	—	250	—	200	—	150	ns

Note: $\overline{WE}$ must be at V_{IH} until end of t_{CO}

READ MODIFY WRITE CYCLE TIMING DIAGRAM



Notes:
1) V_{IL}MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
2) V_{IH}MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3) V_{SS}+ 2.0V is the reference level for measuring timing of CE.
4) V_{DD}– 2.0V is the reference level for measuring timing of CE.
5) V_{SS}+ 2.0V is the reference level for measuring the timing of $D_{\overline{OUT}}$.
6) For refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.

TYPICAL CHARACTERISTICS CURVES

Fig. 1 – I_{DD} AVERAGE vs TEMPERATURE

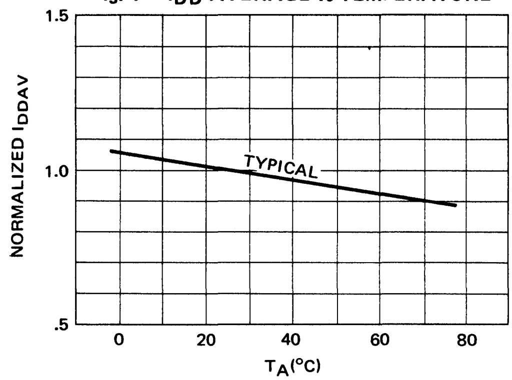


Fig. 2 – I_{DD2} vs TEMPERATURE

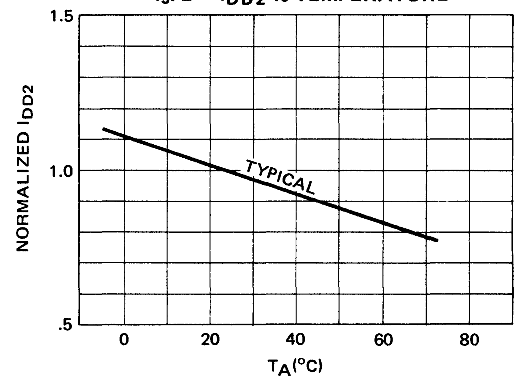


Fig. 3 – TYPICAL REFRESH vs TEMPERATURE

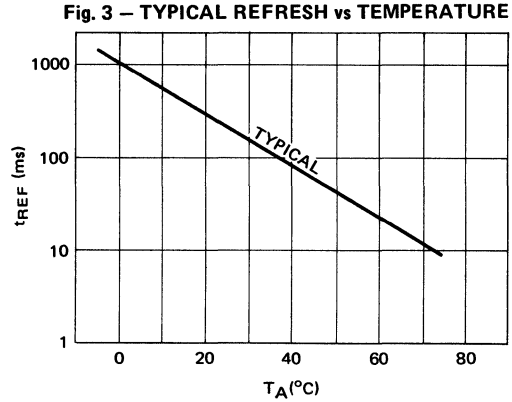


Fig. 4 – TYPICAL ACCESS TIME vs TEMPERATURE

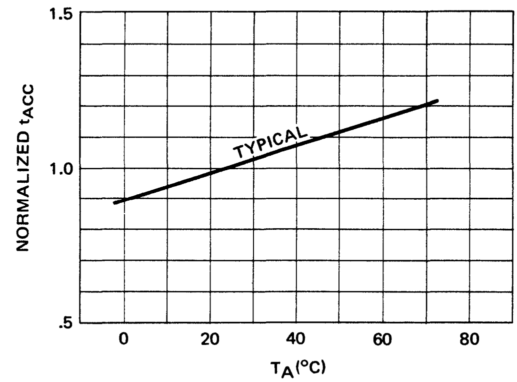


Fig. 5 – TYPICAL I_{OH} vs V_{OH}

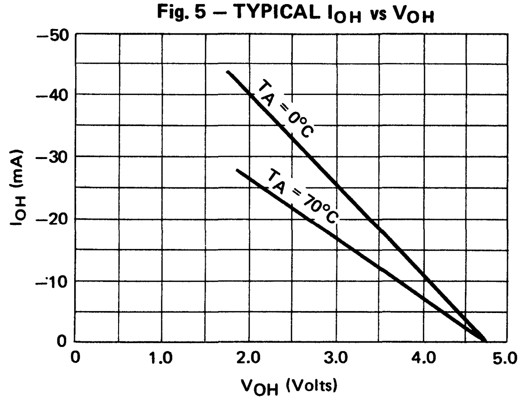


Fig. 6 – TYPICAL I_{OL} vs V_{OL}

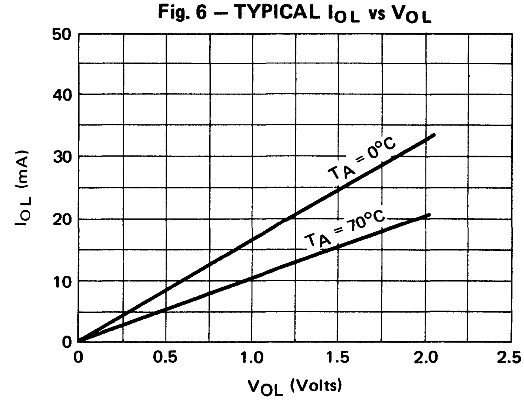
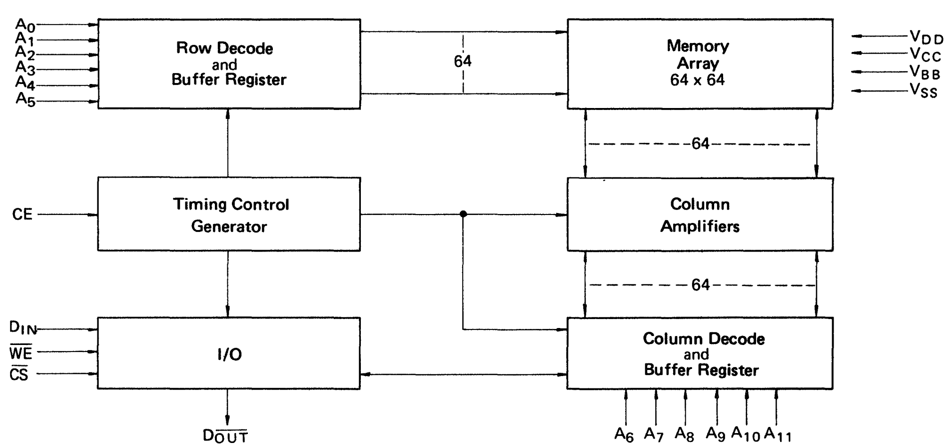
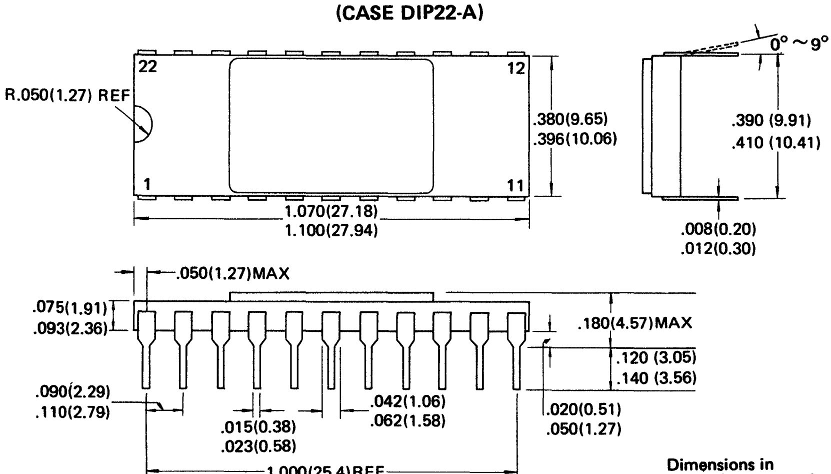


Fig. 7 — MB 8107 BLOCK DIAGRAM



PACKAGE DIMENSIONS

22-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE DIP22-A)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others.

MOS 4096-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 8215E

FUJITSU

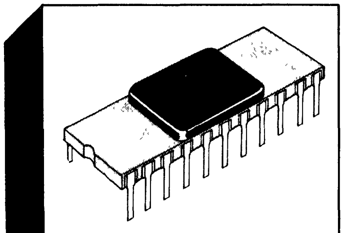
4096-BIT HIGH-SPEED DYNAMIC RANDOM ACCESS MEMORY

The Fujitsu MB 8215 is a high-speed 4096-bit dynamic random access memory designed for main memory or similarly demanding applications. The device is organized as 4096 words by one bit and employs N-channel silicon gate processing technology, with substrate biasing, for maximum device speed and excellent speed power product.

All address and control inputs are fully TTL compatible, with the exception of the single-phase, hi-level clock (CE). Outputs are differential and offer OR-tie capability. Also, a $\overline{CS}$ (Chip Select) lead is provided for simplification of memory expansion.

The MB 8215 is packaged in a ceramic, hermetically-sealed 22-pin dual-in-line package. Performance for the device is specified over the 0°C to 70°C ambient operating temperature range. Since the cell operation is dynamic storage, periodic refreshing is required. In order to assure data at 70°C (ambient), all combinations of addresses A_0 to A_5 must be exercised within 2.0 ms.

- 4096 words x 1 bit organization
- High-speed access time of 70 ns typ. (100 ns max.)
- Minimum read cycle time of 220 ns
- Single-phase, hi-level clock
- TTL-compatible inputs
- Differential outputs with OR-tie capability
- $\overline{CS}$ (Chip Select) lead for simplified memory expansion

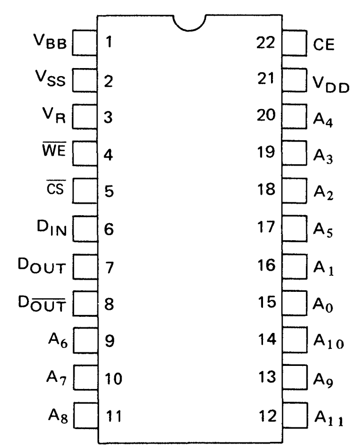


CASE DIP22-A
CERAMIC PACKAGE

- Fully decoded
- Standard 22-pin package

MOS Memories

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Temperature Under Bias	T_A	0 to +70	°C
Storage Temperature	T_{stg}	- 65 to +150	°C
Inputs/Outputs with Respect to V_{BB}	V_{IN}, V_{OUT}	-0.3 to +22	VDC
Supply V_{DD} and V_R with Respect to V_{BB}	–	-0.3 to +22	VDC
Supply V_{SS} with Respect to V_{BB}	–	-0.3 to +8	VDC

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC AND OPERATING CHARACTERISTICS

(T_A = 0°C ~ 70°C, V_{DD} = +12V ± 5%, V_R = +7V ± 5%, V_{BB} = −5.2V ± 5%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	2.4	—	V_R	V
Input Low Voltage	V_{IL}	−1.0	—	0.6	V
CE Input High Voltage	V_{IHC}	V_{DD} −1.0	—	V_{DD} +1.0	V
CE Input Low Voltage	V_{ILC}	−1.0	—	0.8	V
Data Output Differential Current (D_{OUT}, $D_{\overline{OUT}}$ = V_R)	I_{DO}	500	—	—	μA
Input Leakage Current (CE = V_{IHC} or V_{ILC}, V_{IN} = V_{SS} to V_{IH})	I_{IL}	—	—	10	μA
CE Input Leakage Current (CE = V_{ILC} to V_{IHC}, V_{IN} = V_{IL} to V_{IH})	I_{ILC}	—	—	10	μA
Output Leakage Current (CE = V_{ILC}, V_{IN} = V_{IL} to V_{IH}) (CE = V_{ILC} to V_{IHC}, $V_{\overline{CS}}$ = V_{IH}, V_{IN} (except $\overline{CS}$) = V_{IL} to V_{IH})	I_{OL}	—	—	3	μA
V_{DD} Supply Current (CE = V_{ILC}, V_{IN} = V_{SS} to V_{IH})	I_{DDL}	—	—	400	μA
V_R Supply Current (CE = V_{ILC}, V_{IN} = V_{IL} to V_{IH})	I_{RL}	—	—	100	μA
V_{BB} Supply Current (CE = V_{ILC} to V_{IHC}, V_{IN} = V_{IL} to V_{IH})	I_{BB}	—	—	100	μA
V_{DD} Supply Current (CE = V_{IHC}, V_{IN} = V_{IL} to V_{IH})	I_{DDH}	—	15	25	mA
V_R Supply Current (CE = V_{IHC}, V_{IN} = V_{IL} to V_{IH})	I_{RH}	—	25	40	mA
V_{DD} Supply Current (t_{CYC} = 220ns, t_{CE} = 120ns)	I_{DDA}	—	33	42	mA
V_R Supply Current (t_{CYC} = 220ns, t_{CE} = 120ns)	I_{RA}	—	14	20	mA
V_{BB} Supply Current (t_{CYC} = 220ns, t_{CE} = 120ns)	I_{BBA}	—	60	200	μA

AC CHARACTERISTICS

($T_A = 0°C \sim 70°C$, $V_{DD} = +12V \pm 5\%$, $V_R = +7V \pm 5\%$, $V_{BB} = -5.2V \pm 5\%$, $V_{SS} = 0V$)

READ, WRITE and READ MODIFY WRITE CYCLES (t_r, $t_f \leqq 20ns$)

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Refresh	t_{REF}	—	—	2	ms
Address to CE	t_{ACE}	0	—	—	ns
Address Hold Time	t_{AH}	50	—	—	ns
CE Off Time	t_{CC}	100	—	—	ns
$\overline{CS}$ to CE	t_{CSE}	0	—	—	ns
CE to $\overline{CS}$	t_{CES}	0	—	—	ns
CE to $\overline{WE}$	t_{CEW}	0	—	—	ns
Output Data Valid Time	t_{DOV}	0	—	—	ns

READ and REFRESH CYCLES (t_r, $t_f \leqq 20ns$; $R_L = 100\Omega$; $C_L = 50pF$)

Parameter	Symbol	Min	Typ	Max	Unit
CE to Output Delay	t_{ACC}	—	70	100	ns
CE On Time	t_{CE}	120	—	3,000	ns
$\overline{WE}$ to CE	t_{WCE}	0	—	—	ns
Read Refresh Cycle Time	t_{CYC}	220	—	—	ns

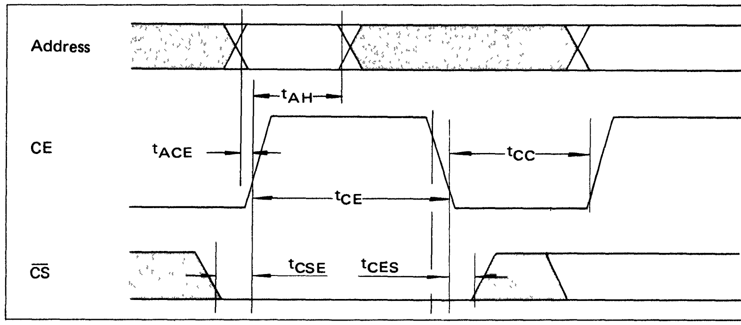
WRITE CYCLE (t_r, $t_f \leqq 20ns$)

Parameter	Symbol	Min	Typ	Max	Unit
CE to $\overline{WE}$	t_{CEW}	0	—	—	ns
Write Width	t_W	80	—	—	ns
Write Data Set Up Time	t_{DW}	0	—	—	ns
Write Data Hold Time	t_{CED}	0	—	—	ns
CE On Time	t_{CE}	100	—	3,000	ns
Write Cycle Time	t_{CYC}	200	—	—	ns

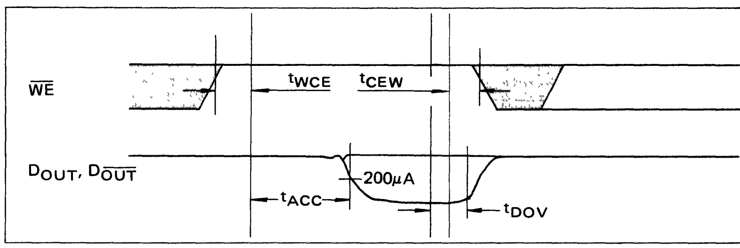
READ MODIFY WRITE CYCLE (t_r, $t_f \leqq 20ns$; $R_L = 100\Omega$; $C_L = 50pF$)

Parameter	Symbol	Min	Typ	Max	Unit
CE to Output Delay	t_{ACC}	—	70	100	ns
Write Width	t_W	80	—	—	ns
CE to $\overline{WE}$	t_{CEW}	0	—	—	ns
Write Data Set Up Time	t_{DW}	0	—	—	ns
Write Data Hold Time	t_{CED}	0	—	—	ns
CE On Time	t_{CE}	200	—	3,000	ns
Read Modify Write Cycle Time	t_{CYCM}	300	—	—	ns
$\overline{WE}$ to CE	t_{WCE}	0	—	—	ns

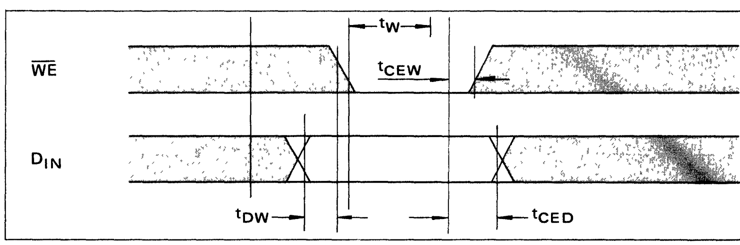
TIMING DIAGRAMS



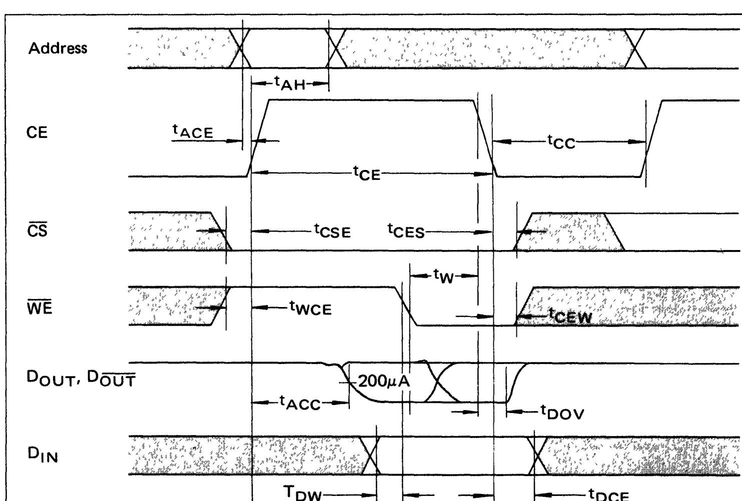
READ CYCLE



WRITE CYCLE



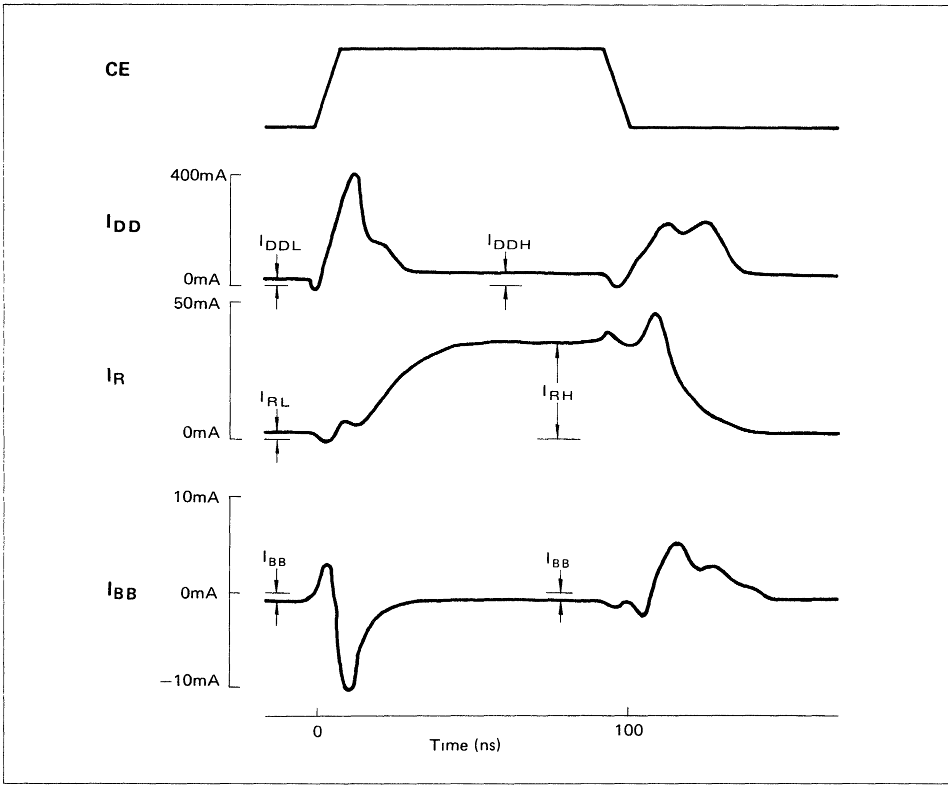
READ MODIFY WRITE CYCLE



NOTE:
$V_{SS} + 1.5V$ and $V_{DD} - 1.5V$ are the reference levels for measuring the timing of CE. 0.6V and 2.4V are the reference levels for measuring the timing of $\overline{CS}$, $\overline{WE}$, D_{IN}, and all Addresses.

Don't Care

CURRENT CHARACTERISTICS



CAPACITANCE (f = 1MHz; $V_{SS} - V_{BB}$ = 4.94V; $V_{DD} - V_{SS}$ = 12.6V; $V_{IN} = V_{SS}$)

Parameter	Symbol	Min	Typ	Max	Unit
Address Inputs	C_A	—	—	3	pF
CE Input	C_{CE}	—	33	40	pF
$\overline{WE}$, $\overline{CS}$ Inputs	$C_{\overline{WE}}$, $C_{\overline{CS}}$	—	—	6	pF
D_{IN} Input	C_{DIN}	—	—	3	pF
D_{OUT}, $D_{\overline{OUT}}$	C_{DO}, $C_{\overline{DO}}$	—	—	3	pF

MOS Memories

TYPICAL CHARACTERISTICS CURVES

Fig. 1—NORMALIZED ACCESS TIME vs V_{DD} SUPPLY VOLTAGE

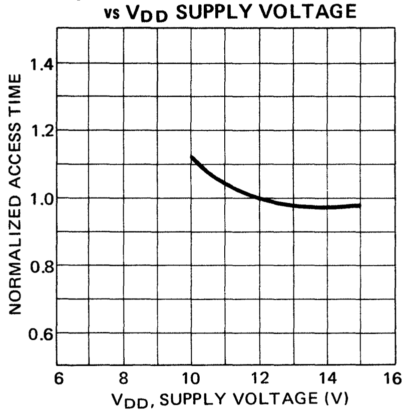


Fig. 2—NORMALIZED ACCESS TIME vs V_R SUPPLY VOLTAGE

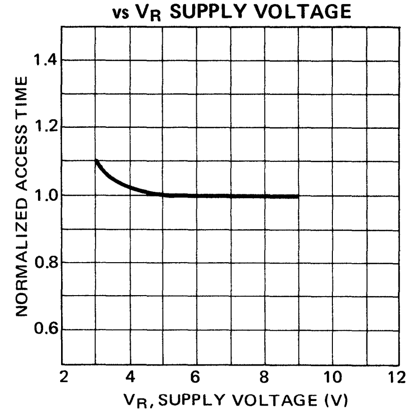


Fig. 3—I_{DD} SUPPLY CURRENT vs CYCLE TIME

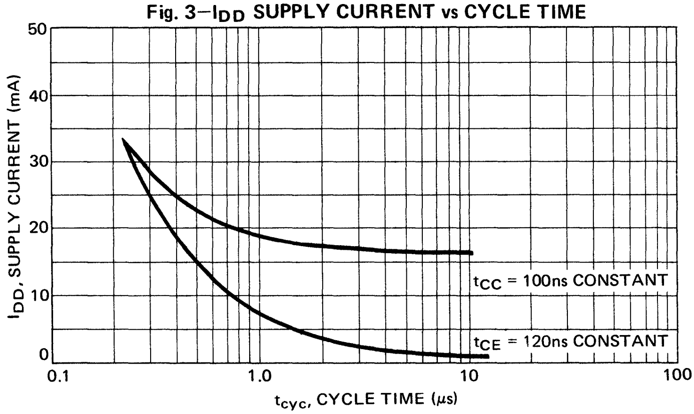


Fig. 4—I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

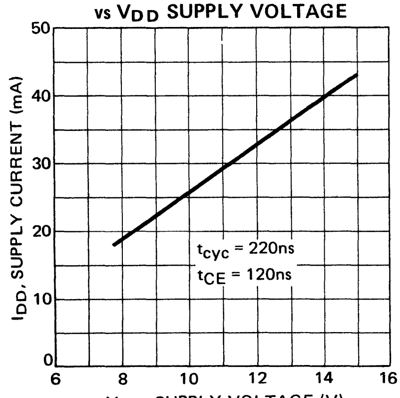


Fig. 5—I_{DD} SUPPLY CURRENT vs AMBIENT TEMPERATURE

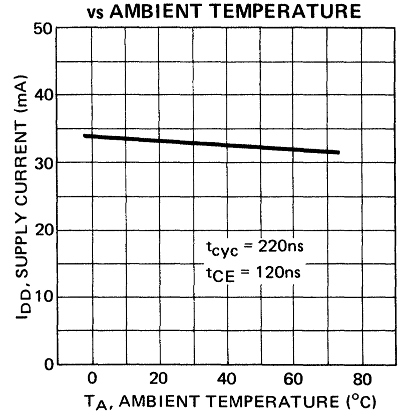


Fig. 6—NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

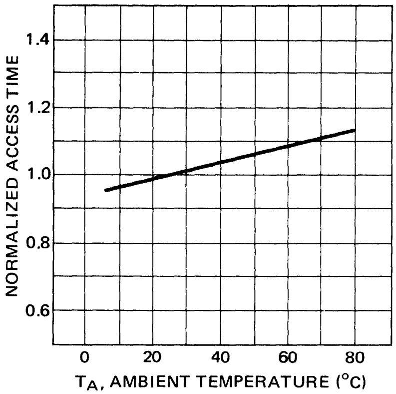


Fig. 7—REFRESH TIME vs AMBIENT TEMPERATURE

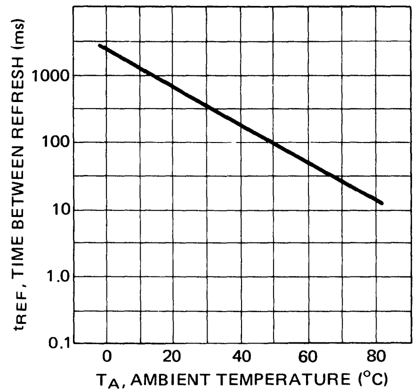


Fig. 8—I_R SUPPLY CURRENT vs CYCLE TIME

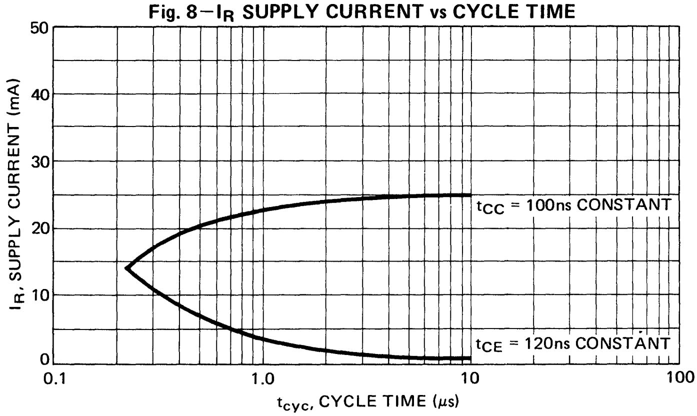


Fig. 9—I_R SUPPLY CURRENT vs V_R SUPPLY VOLTAGE

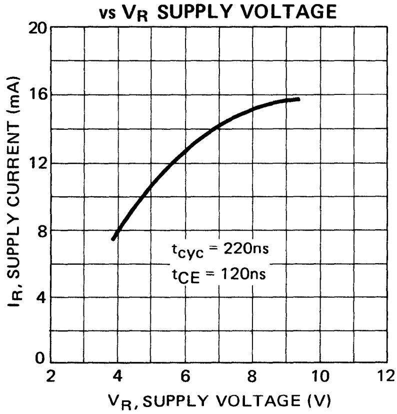
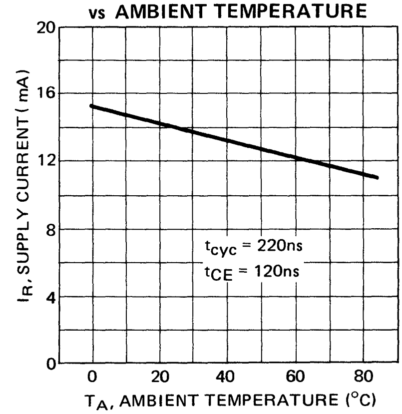


Fig. 10—I_R SUPPLY CURRENT vs AMBIENT TEMPERATURE



MOS Memories

TYPICAL TRANSIENT WAVEFORMS

Fig. 11—CHIP ENABLE VOLTAGE

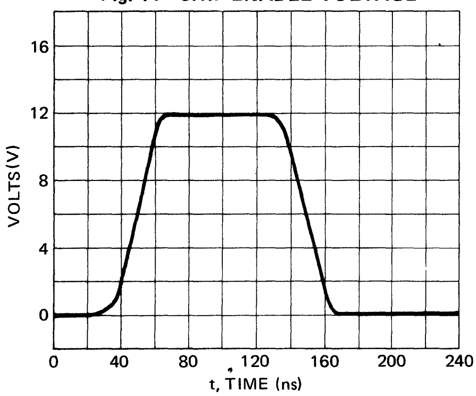


Fig. 12—I_{SS} SUPPLY CURRENT

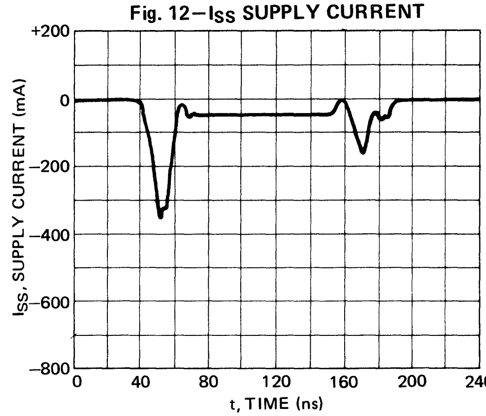


Fig. 13—I_{DD} SUPPLY CURRENT

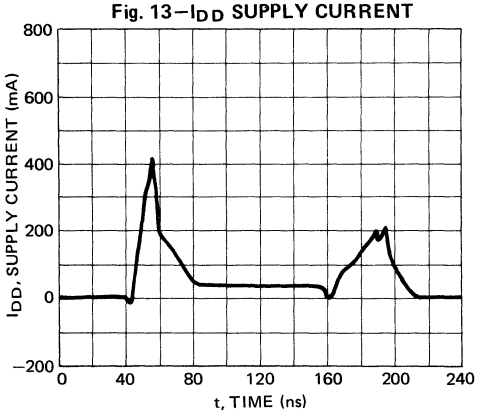


Fig. 14—I_{BB} SUPPLY CURRENT

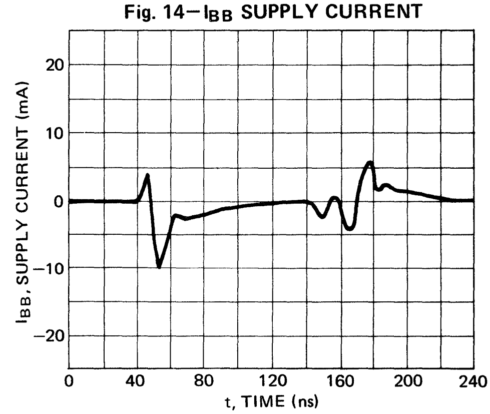


Fig. 15—I_R SUPPLY CURRENT

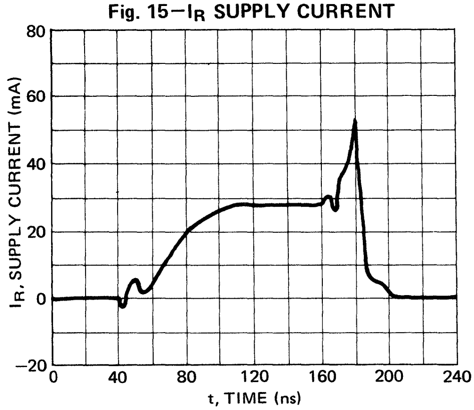
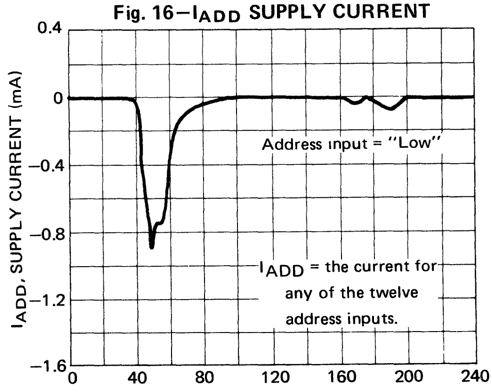
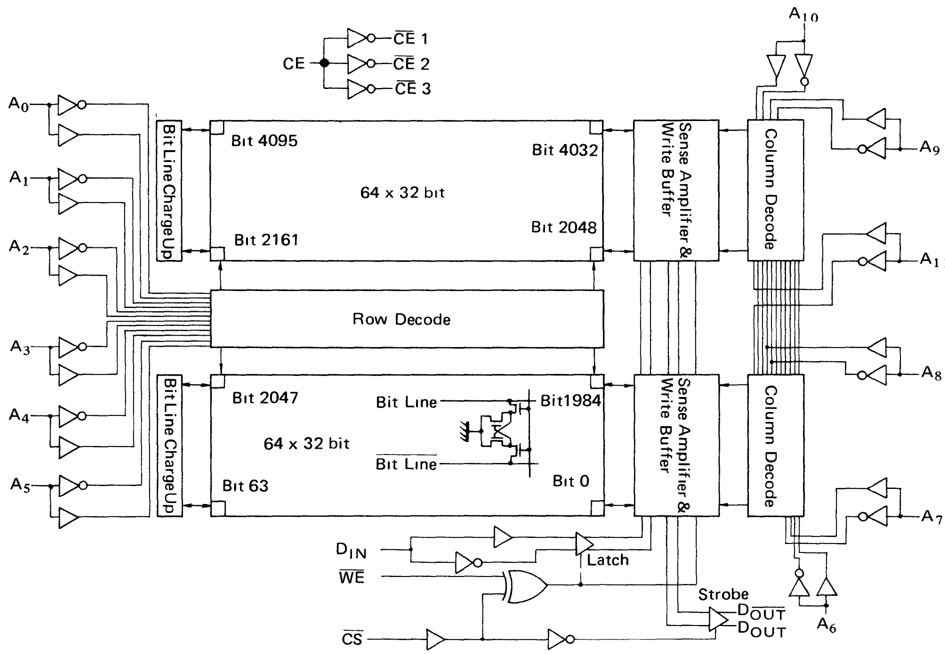


Fig. 16—I_{ADD} SUPPLY CURRENT



FUNCTIONAL DESCRIPTION/APPLICATIONS INFORMATION

Fig. 15—MB 8215 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MB 8215 4096-bit dynamic RAM uses four-transistor storage cells, fabricated with N-channel silicon gate MOS technology. When the single hi-level clock (CE) goes high, three internal clocks are brought from V_{DD} to V_{SS}. When CE is low, these three clocks are brought to V_{DD} in preparation for memory operations.

Read Cycle— Data held in the storage cells can be read through the D_{OUT} and $D_{\overline{OUT}}$ lines when $\overline{CS}$ is low and $\overline{WE}$ (Write Enable) is high. When CE is brought high, the output state of the address buffers is made stable to select one word line out of the 64 lines available, and bring it from low to high. When the word line is high, the storage cells can sink current through either the bit-lines or $\overline{\text{bit-lines}}$ and the data in the cell is transfered to the sense amplifier.

Column decode operation is identical with row decode: the column decoder selects one sense amplifier out of 64 to transfer the data to the output buffer. D_{OUT} or $D_{\overline{OUT}}$ sinks current respectively depending on whether the data in the memory cell is a "1" or "0".

Write Cycle— Data can be written into the storage cell when $\overline{CS}$ and $\overline{WE}$ are low. When CE is high, one cell is selected, as in the read cycle. During this period, the low state of $\overline{WE}$ activates the write-enable buffer to transfer the D_{IN} signal to the cell via one write buffer which is selected out of the 64 lines available by the column decoder.

INPUT/OUTPUT SIGNALS

Chip Enable (CE)— CE is a single-phase, hi-level clock; all memory cycles are initiated when CE goes high. CE Off Time (t_{CC}) must not exceed 2.0ms (Ta=70°C); if it does, cell data will not be retained, and internal circuits will not operate properly. CE must be brought from high to low at least once before a memory cycle.

Chip Select ($\overline{CS}$)— The $\overline{CS}$ signal controls the write-enable and output buffers, and it must be low during the read, write, and read modify write cycles. When $\overline{CS}$ is high, the input is disconnected, and the output is in the high impedance mode. Refresh can be achieved, even when $\overline{CS}$ is high, because the memory will function even though the write-enable buffers and output buffers are not operated.

Write Enable ($\overline{WE}$)— When $\overline{WE}$ is high, the memory is in the read operation, while $\overline{WE}$ low indicates the write operation is taking place. For the read modify write operation, a combination of $\overline{WE}$ high (for reading data) and low (for writing new data) is required.

Data In (D_{IN})– When CE is brought to high with $\overline{WE}$ low, or when $\overline{WE}$ is brought to low with CE high, the D_{IN} signal can be transfered to the cell. Therefore, the D_{IN} signal must remain valid when CE is high and $\overline{WE}$ is low.

Data Out (D_{OUT}), $\overline{\text{Data Out}}$ ($D_{\overline{OUT}}$)– The output is a differential current sink type which requires the use of a differential sense amplifier (Fujitsu MB 8916 or equivalent), with resistors positioned as shown in Figure 17 (Access Time Measuring Circuit diagram). When D_{IN} is high, D_{OUT} sinks greater current than $D_{\overline{OUT}}$; under reversed conditions, the opposite is true. During CE and $\overline{WE}$ high, D_{OUT} and $D_{\overline{OUT}}$ hold the above-mentioned state. Then, as $\overline{WE}$ is brought low, newly stored data is brought out through D_{OUT} and $D_{\overline{OUT}}$. When CE is low (or $\overline{CS}$ high), D_{OUT} and $D_{\overline{OUT}}$ are in the high impedance state, and even if CE goes high with $\overline{CS}$ low, this state will remain until data is transferred to D_{OUT} and $D_{\overline{OUT}}$.

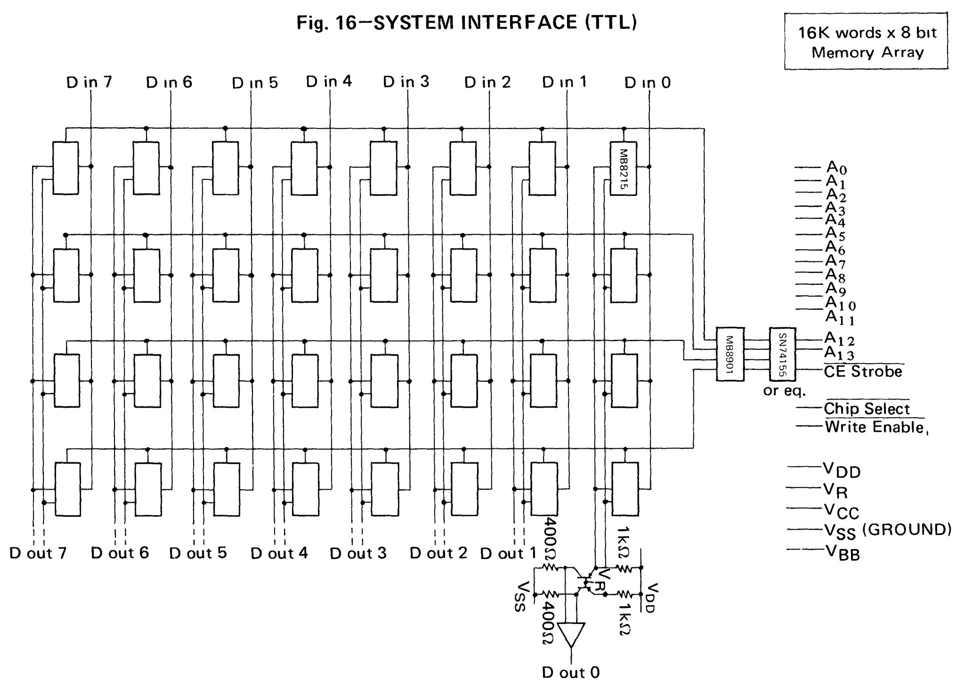
Addresses– The addresses are latched in the address buffers when CE is brought high. For normal operation, the addresses must be stable during the specified time t_{AH} (address hold time).

APPLICATIONS INFORMATION

Refresh– Refresh can be accomplished during any of the read, write, or read modify write cycles. In the case of the refresh cycle, $\overline{CS}$ can be in either state during the read cycle, but it must be high during the write and read modify write cycles. The memory is refreshed by selecting each of the 64 row addresses (A_0 to A_5) every 2.0ms. During minimum read cycle operation (i.e., t_{CYC} = 220ns) the time ratio of refreshing to total operation is about 0.7%.

Power Dissipation– The MB 8215 has a maximum power dissipation of 680 mW (500mW typical). In stand-by mode, this is reduced to approximately 6.4mW.

Fig. 16–SYSTEM INTERFACE (TTL)



NOTES: 1) MB 8901: FUJITSU Quad 2-Input NAND TTL to MOS Level Shifter/Driver, similar to SN-75361/75365 or equivalent.

2) MB 8912: FUJITSU Dual Sense Amp (TTL Output), or equivalent.

ACCESS TIME MEASURING CIRCUIT

The MB 8215 has differential outputs which require a differential sense amplifier and load resistors connected to interface with the external circuit. Measurement of the access time can be accomplished by latching the output data in an external circuit. Access time is then calculated by measuring the time between the rising edge of CE and rising edge of the latch ($\overline{C_C}$), and then substracting the delay time introduced by the sense amplifier circuit.

In order to measure access time with a differential current between D_{OUT} and $D_{\overline{OUT}}$ of 200μA, a 200μA source should be connected as shown in Figure 17, with the off-set current injected between A and B.

Fig. 17—ACCESS TIME MEASURING CIRCUIT

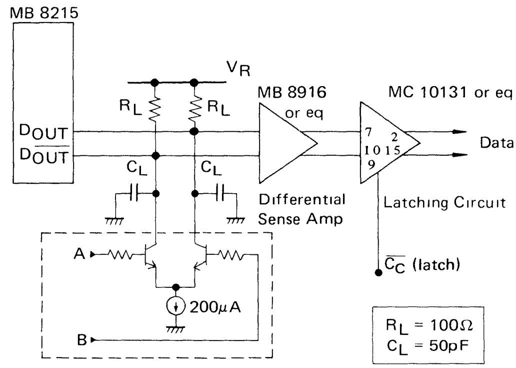
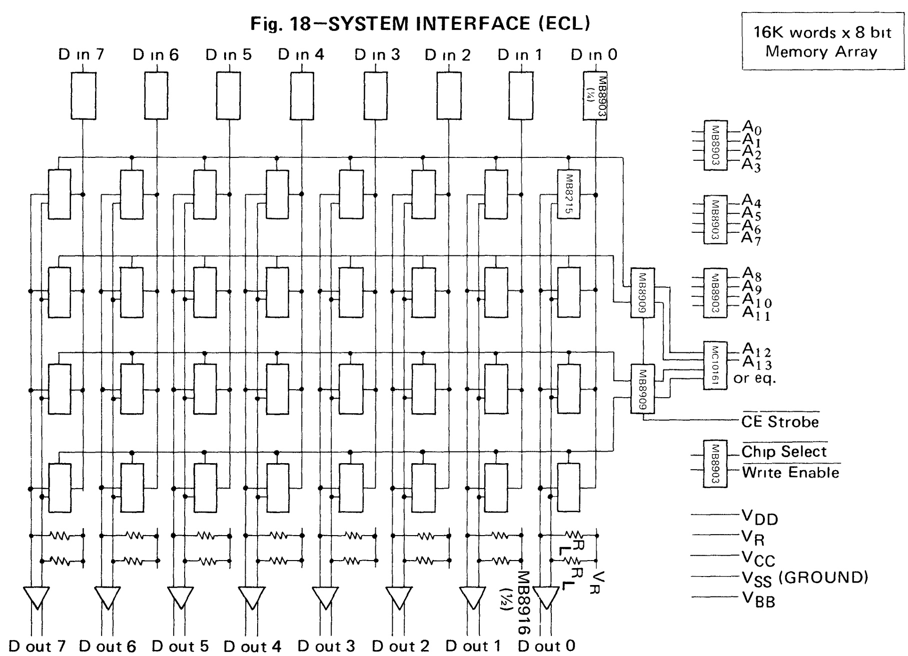
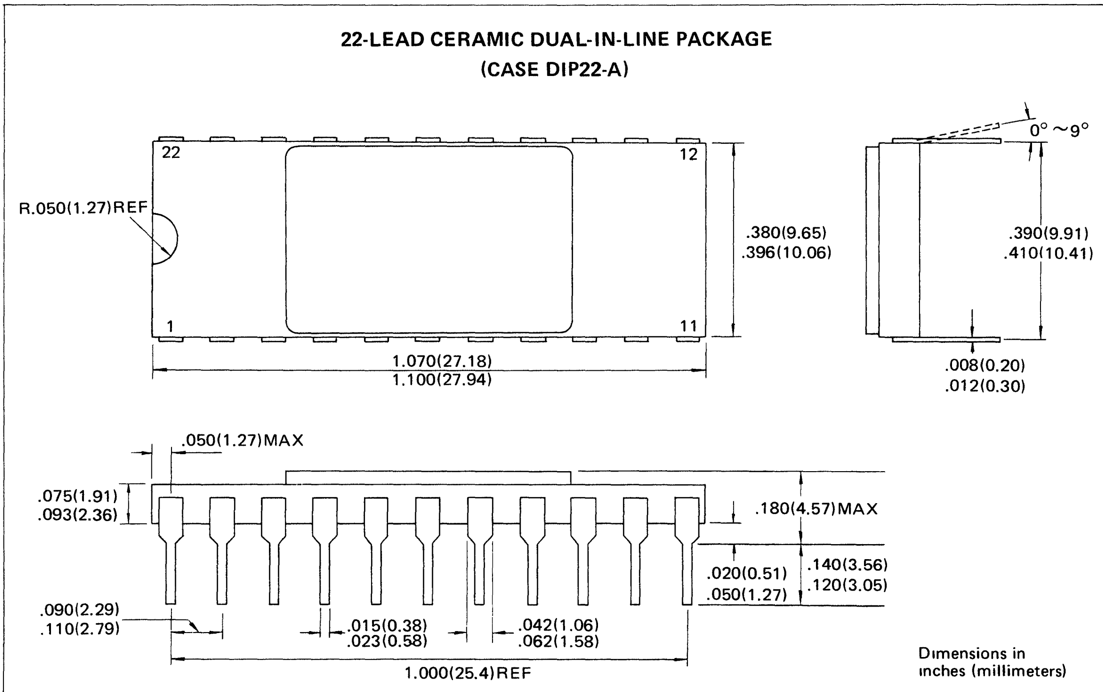


Fig. 18—SYSTEM INTERFACE (ECL)



NOTES: 1) MB 8903: FUJITSU Quad 2-Input OR ECL to MOS Level Shifter/Driver, similar to MC 10177 or equivalent.
2) MB 8909: FUJITSU Dual 2-Input Positive NOR ECL to MOS Level Shifter/Driver, similar to MC 10127 or equivalent.
3) MB 8916: FUJITSU Dual Sense Amp ECL Output, or equivalent.

PACKAGE DIMENSIONS



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications, consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Ltd. or others.

MOS 4096-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 8224N/E/H

FUJITSU

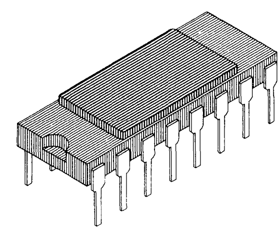
4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The Fujitsu MB 8224 is a 4096-word by 1-bit dynamic N-channel MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

A unique multiplexing and latching technique for the address inputs permits the MB 8224 to be packaged in a standard 16-pin DIP configuration. This package size provides for high system bit densities.

The MB 8224 uses a single-transistor cell to achieve high speed and low cost. However, cell operation is dynamic storage, thus, requiring periodic refreshing. Each of the 64 row addresses must be refreshed every 2 milliseconds.

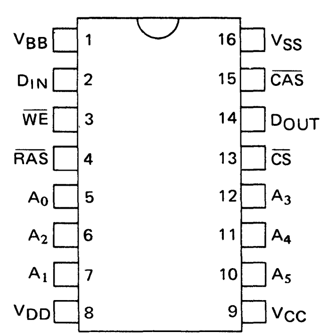
- 4096 words x 1 bit organization
- Silicon gate, N-channel MOS technology
- Access time:
  200 ns max (MB 8224H)
  230 ns max. (MB 8224E)
  280 ns max. (MB 8224N)
- Read cycle time:
  340 ns min. (MB 8224H)
  370 ns min. (MB 8224E)
  450 ns min. (MB 8224N)
- Two low-voltage clocks
- All inputs TTL compatible
- Output three-state TTL compatible
- $\overline{CS}$ (Chip Select) lead simplifies memory expansion
- Full on-chip address decode
- Low power dissipation of 470 mW (max.)



CASE DIP16-B
CERAMIC PACKAGE

- Standard 16-pin DIP package
- Interchangeable with MK4096, MK4027, MCM6604, Intel 2104

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{BB} ($V_{SS} - V_{BB} \geqslant 4.5V$)	V_{IN}, V_{OUT}	-0.3 to +20	VDC
Operating temperature range	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Power Dissipation	P_D	1.0	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS NOTES 1

(Recommended DC operating conditions and full operating temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	NOTES	Symbol	Min	Typ	Max	Unit
Supply Voltage	1	V_{DD}	10.8	12.0	13.2	V
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V
Supply Voltage		V_{SS}	—	0.0	—	V
Supply Voltage	1	V_{BB}	−4.5	−5.0	−5.5	V
Input High Voltage	2	V_{IH}	2.4	—	V_{CC}+1.0	V
Input Low Voltage		V_{IL}	−1.0	—	0.8	V

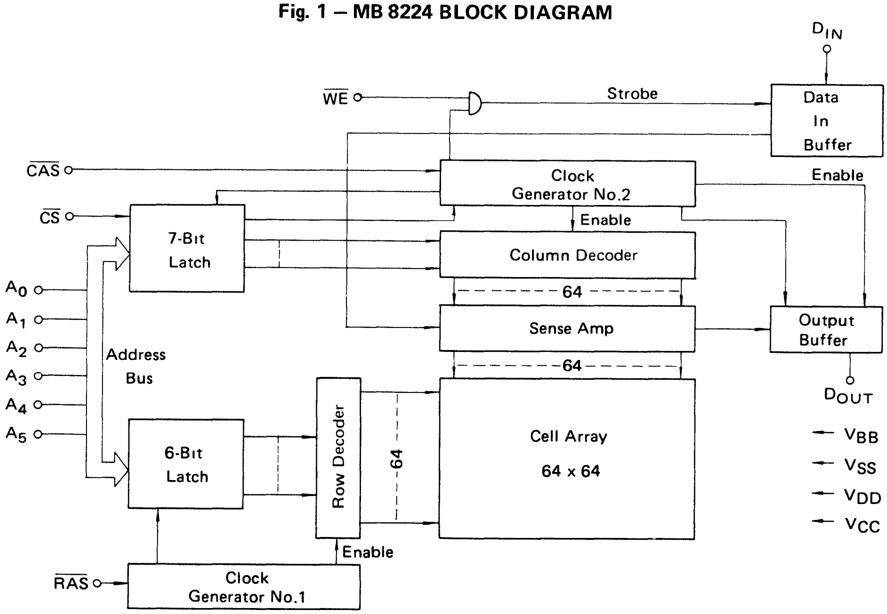
DC CHARACTERISTICS

Parameter		NOTES	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{OH}= -5.0mA)			V_{OH}	2.4	—	V_{CC}	V
Output Low Voltage (I_{OL}= 2.0mA)			V_{OL}	—	—	0.4	V
Input Leakage Current			I_{IL}	—	—	10	μA
Output Leakage Current for high impedance state ($\overline{CS}$=V_{IH})			I_{OL}	—	—	10	μA
V_{DD} Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, chip deselected)	MB 8224N		I_{DD1}	—	—	1.5	mA
	MB 8224E		I_{DD1}	—	—	1.5	mA
	MB 8224H		I_{DD1}	—	—	2.0	mA
Average V_{DD} Current (minimum cycle)			I_{DD2}	—	—	35	mA
Average V_{DD} Current ($\overline{RAS}$ only refresh cycle)			I_{DD3}	—	—	25	mA
Average V_{BB} Current	MB 8224N		I_{BB}	—	—	75	μA
	MB 8224E		I_{BB}	—	—	75	μA
	MB 8224H		I_{BB}	—	—	150	μA
V_{CC} Supply Current ($\overline{CS}$ = V_{IH})		3	I_{CC}	—	—	10	μA

CAPACITANCE (T_A = 25 °C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0 \sim A_5$, $\overline{WE}$, $\overline{CS}$, D_{IN})	C_{I1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I2}	—	10	pF
Output Capacitance	C_O	—	8	pF

Fig. 1 — MB 8224 BLOCK DIAGRAM



AC OPERATING CONDITIONS AND CHARACTERISTICS NOTES 1,4

(Recommended DC operating conditions and full operating temperature range unless otherwise noted.)

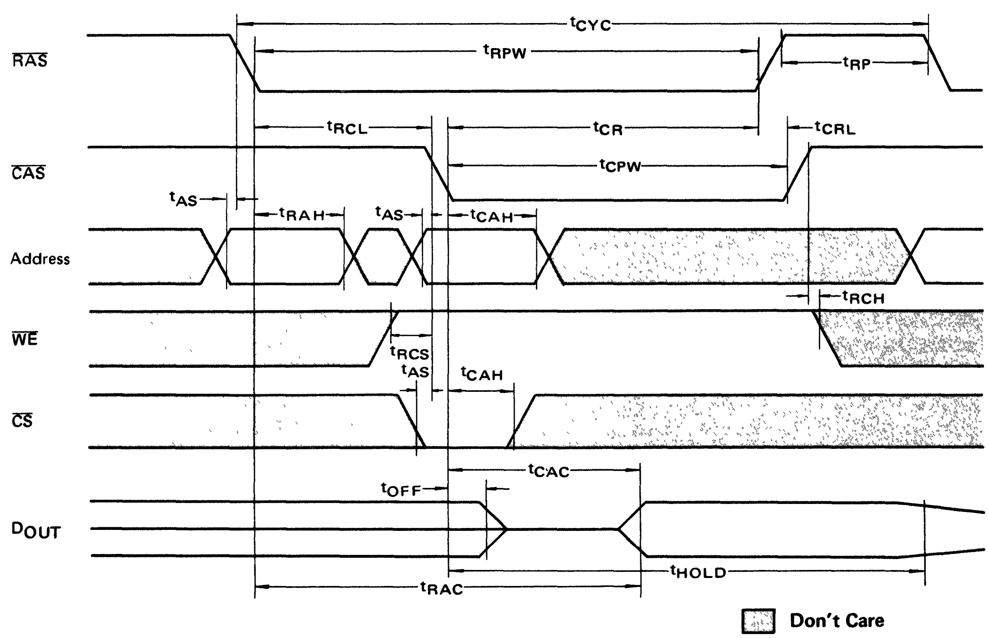
READ, WRITE, READ MODIFY WRITE and $\overline{RAS}$ ONLY REFRESH CYCLES (t_T = 10 ns)

Parameter (NOTES)	Symbol	MB 8224N		MB 8224E		MB 8224H		Unit
		Min	Max	Min	Max	Min	Max	
Time Between Refresh	t_{REF}	—	2	—	2	—	2	ms
$\overline{RAS}$ Precharge Time	t_{RP}	150	—	120	—	120	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Lead Time (5)	t_{RCL}	95	2000	80	2000	70	2000	ns
$\overline{RAS}$ Hold Time	t_{CR}	175	—	140	—	120	—	ns
$\overline{CAS}$ to $\overline{RAS}$ Lead Time (6)	t_{CRL}	—	40	—	40	—	40	ns
Address Set Up Time	t_{AS}	0	—	0	—	0	—	ns
Address Hold Time	t_{AH}	85	—	70	—	60	—	ns
Output Deselect Time	t_{OFF}	0	100	0	85	0	75	ns
Data Out Hold Time	t_{HOLD}	2	—	2	—	2	—	ms
Rise and Fall Time	t_T	5	50	5	50	5	50	ns

READ CYCLE (t_T = 10ns)

Parameter	NOTES	Symbol	MB 8224N Min	MB 8224N Max	MB 8224E Min	MB 8224E Max	MB 8224H Min	MB 8224H Max	Unit
Read Cycle Time		t_{CYC}	450	—	370	—	340	—	ns
$\overline{RAS}$ Pulse Width	7	t_{RPW}	280	32000	230	32000	200	32000	ns
$\overline{CAS}$ Pulse Width		t_{CPW}	175	—	140	—	120	—	ns
Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
Read Command Hold Time		t_{RCH}	30	—	30	—	30	—	ns
Access Time from $\overline{RAS}$ (C_L = 50pF)	8	t_{RAC}	280	—	230	—	200	—	ns
Access Time from $\overline{CAS}$ (C_L = 50pF)		t_{CAC}	175	—	140	—	120	—	ns

Read Cycle Timing Diagram



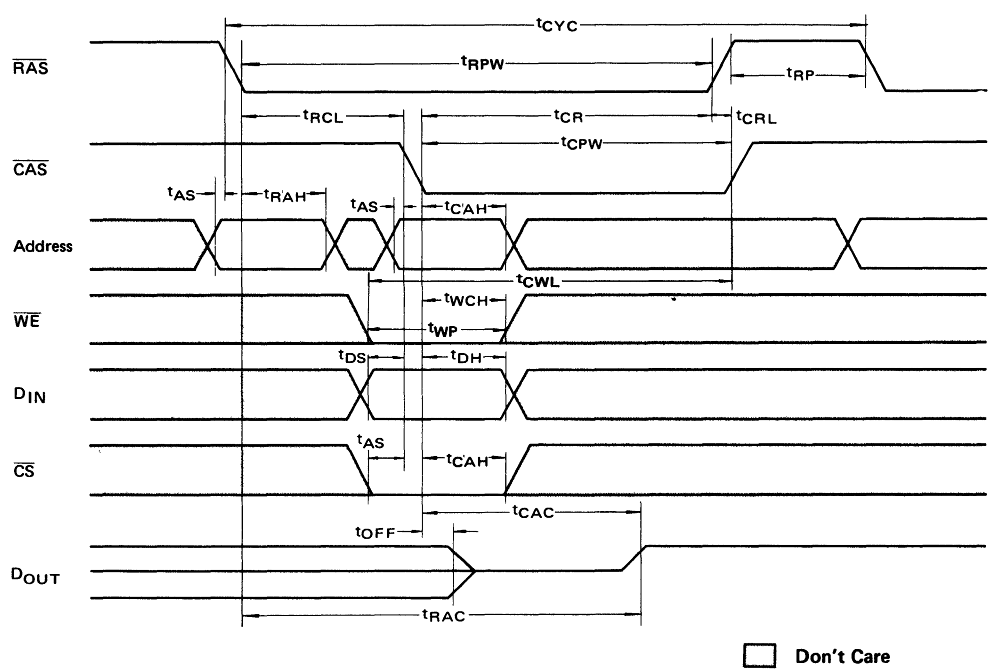
REFRESH CYCLE

Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milli-seconds or less. Any read, write or read modify write cycle will refresh a selected row. $\overline{RAS}$ only refresh cycle is also used to refresh a selected row with reducing power dissipation. However, prior to the first cycle following a period (beyond 2ms) of "$\overline{RAS}$ only refresh", a memory cycle employing both $\overline{RAS}$ and $\overline{CAS}$ must be performed with $\overline{CS}$ high level (chip non-select mode) to insure proper device operation. And if a write or read modify write cycle is used to refresh a row, the chip must be deselected ($\overline{CS}$ high) to prevent writing data into the selected cell.

WRITE CYCLE (t_T = 10ns)

Parameter	NOTES	Symbol	MB 8224N Min	MB 8224N Max	MB 8224E Min	MB 8224E Max	MB 8224H Min	MB 8224H Max	Unit
Write Cycle Time		t_{CYC}	450	—	370	—	340	—	ns
$\overline{RAS}$ Pulse Width		t_{RPW}	280	32000	230	32000	200	32000	ns
$\overline{CAS}$ Pulse Width		t_{CPW}	175	—	140	—	120	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	175	—	140	—	120	—	ns
Write Command Hold Time		t_{WCH}	130	—	110	—	100	—	ns
Write Command Pulse Width		t_{WP}	130	—	110	—	100	—	ns
Data In Set Up Time	9	t_{DS}	0	—	0	—	0	—	ns
Data In Hold Time	9	t_{DH}	150	—	140	—	100	—	ns

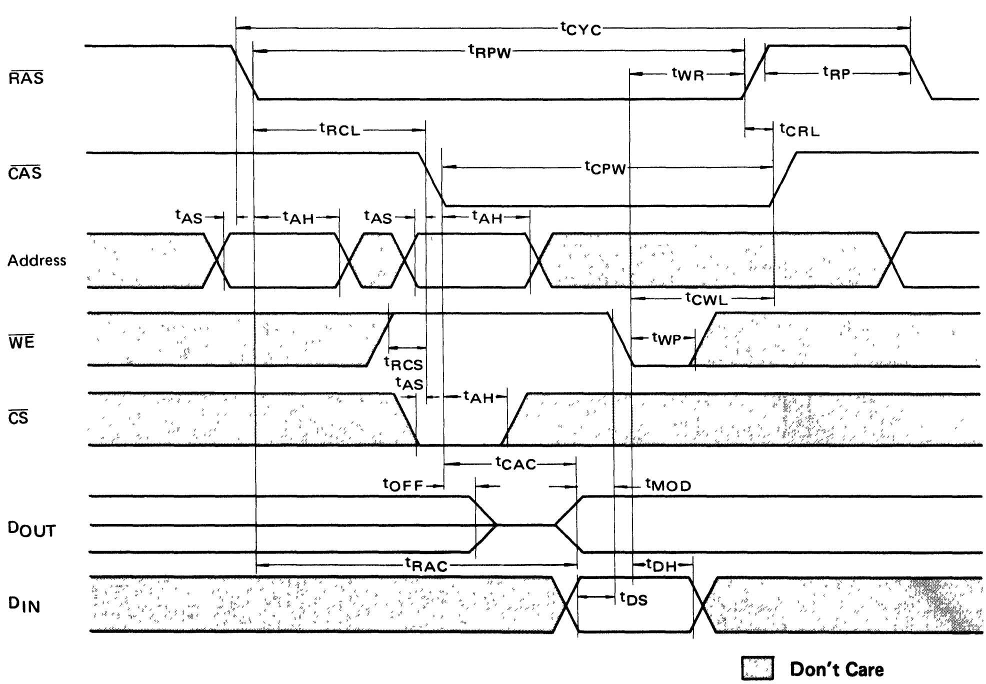
Write Cycle Timing Diagram



READ MODIFY WRITE CYCLE (t_T = 10ns)

Parameter	NOTES	Symbol	MB 8224N Min	MB 8224N Max	MB 8224E Min	MB 8224E Max	MB 8224H Min	MB 8224H Max	Unit
Read/Write Cycle Time		t_{CYC}	635	—	520	—	470	—	ns
$\overline{RAS}$ Pulse Width	10	t_{RPW}	465	32000	380	32000	330	32000	ns
$\overline{CAS}$ Pulse Width		t_{CPW}	360	—	290	—	250	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	175	—	140	—	120	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{WR}	175	—	140	—	120	—	ns
Write Command Pulse Width		t_{WP}	130	—	110	—	100	—	ns
Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
Modify Time		t_{MOD}	0	—	0	—	0	—	ns
Data In Set Up Time		t_{DS}	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	150	—	140	—	100	—	ns
Access Time from $\overline{RAS}$ (C_L = 50pF)		t_{RAC}	280	—	230	—	200	—	ns
Access Time from $\overline{CAS}$ (C_L = 50pF)		t_{CAC}	175	—	140	—	120	—	ns

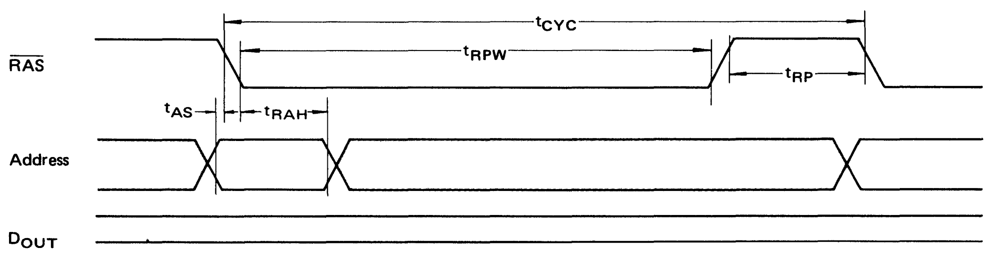
Read Modify Write Cycle Timing Diagram



$\overline{RAS}$ ONLY REFRESH CYCLE (t_T = 10ns)

Parameter	Symbol	MB 8224N		MB 8224E		MB 8224H		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{RAS}$ Only Refresh Cycle Time	t_{CYC}	450	—	370	—	340	—	ns
$\overline{RAS}$ Pulse Width	t_{RPW}	280	32000	230	32000	200	32000	ns

$\overline{RAS}$ Only Refresh Cycle Timing Diagram



Prior to the first cycle following a period (beyond 2 ms) of "$\overline{RAS}$ only refresh", a memory cycle employing both $\overline{RAS}$ and $\overline{CAS}$ must be performed with $\overline{CS}$ high level (chip non-select mode) to insure proper device operation.

☐ Don't Care

NOTES:

1) All voltages referenced to V_{SS}. V_{BB} must be applied before (and removed after) other supply voltages.
2) Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5.5V).
3) When chip is selected, V_{CC} supply current is dependent on output loading; V_{CC} is connected to the output buffer only.
4) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of input signals. Transition times (t_T) are also measured between V_{IH} and V_{IL}.
5) $t_{RCL} = t_{AH} + 1t_T$.
6) When $t_{CR} > t_{CR}$ (min.) and $t_{CPW} > t_{CPW}$ (min.), t_{CRL} (min.) is defined by $t_{CPW} - t_{CR}$. (Read or write cycle)
   And when $t_{WR} > t_{WR}$(min.) and $t_{CWL} > t_{CWL}$(min.), t_{CRL}(min.) is defined by $t_{CWL} - t_{WR}$. (Read Modify Write Cycle)
7) $t_{RPW} \geqq t_{RAC}$.
8) t_{RAC} (min.) = t_{RCL} (min.) + $1t_T$ + t_{CAC} (min.). Then if $t_{RCL} > t_{RCL}$ (min.), t_{RAC} will be greater by the amount t_{RCL} exceeds t_{RCL} (min.).
9) These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10) $t_{RPW} \geqq t_{RAC} + t_{MOD} + 1t_T + t_{WR}$.

TYPICAL CHARACTERISTICS CURVES

Fig. 2 – I_{DD} NORMALIZED VS DUTY CYCLE

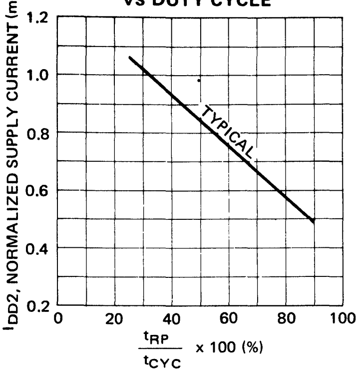


Fig. 3 – I_{DD} NORMALIZED VS V_{DD} SUPPLY VOLTAGE

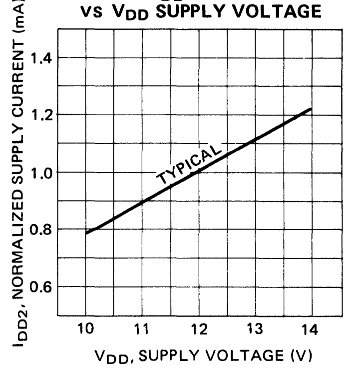


Fig. 4 – I_{DD} NORMALIZED VS AMBIENT TEMERATURE

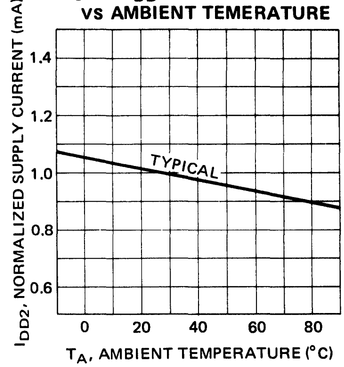


Fig. 5 – t_{CAC} NORMALIZED ACCESS TIME VS V_{DD} SUPPLY VOLTAGE

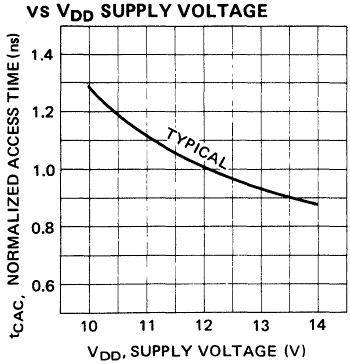


Fig. 6 – t_{CAC} NORMALIZED ACCESS TIME VS AMBIENT TEMPERATURE

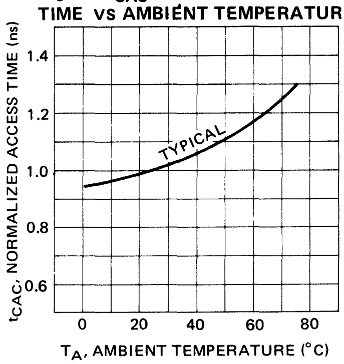


Fig. 7 – t_{REF} REFRESH TIME VS AMBIENT TEMPERATURE

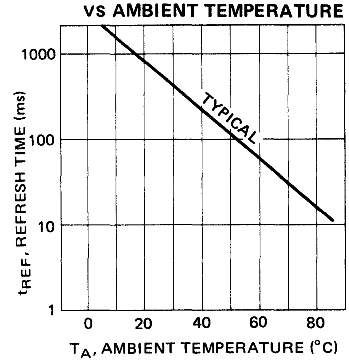


Fig. 8 – I_{OH} OUTPUT HIGH CURRENT VS V_{OH} OUTPUT HIGH VOLTAGE

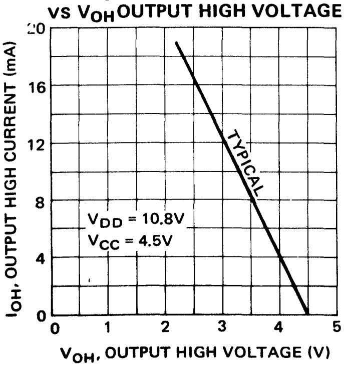


Fig. 9 – I_{OL} OUTPUT LOW CURRENT VS V_{OL} OUTPUT LOW VOLTAGE

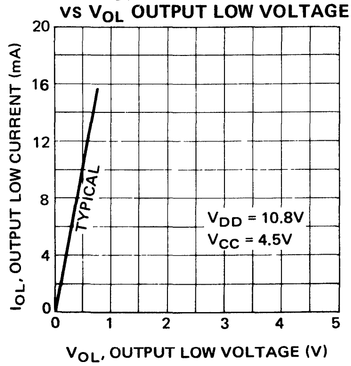
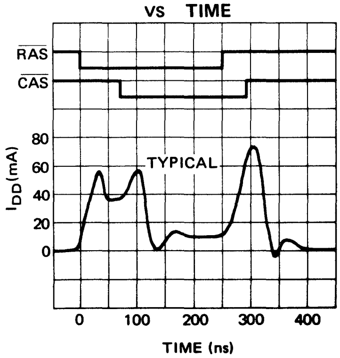
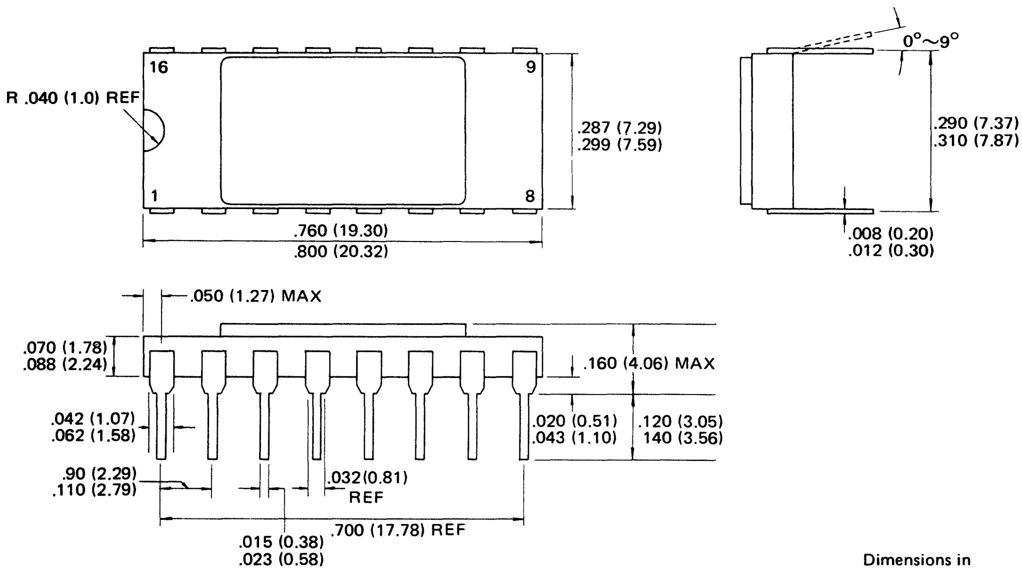


Fig. 10 – CURRENT TRANSIENTS VS TIME



PACKAGE DIMENSIONS

16-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE DIP16-A)



Dimensions in
inches (millimeters)

FUJITSU

MOS 4096-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 8227N/E/H

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

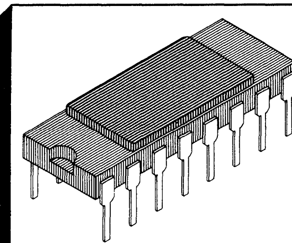
The Fujitsu MB 8227E/H is a fully decoded, dynamic NMOS random access memory organized as 4,096 one-bit words. The design is optimized for high-speed, high-performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 8227 to be housed in a standard 16-pin DIP. Pin-outs conform to the accepted industry standard.

The MB 8227 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerances are 10%. All inputs are TTL compatible; the output is three-state TTL.

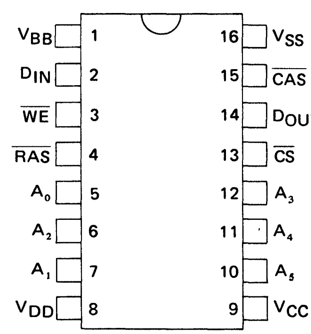
- 4,096 x 1 RAM, 16-pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  150 ns max. (MB 8227H)
  200 ns max. (MB 8227E)
  250 ns max. (MB 8227N)
- Cycle time,
  320 ns min. (MB 8227H)
  375 ns min. (MB 8227E/N)
- Low power: 462 mW active, 27 mW standby (max.)
- 10% tolerance on +12V, ±5V, supplies
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 64 refresh cycles



CASE DIP16-A
CERAMIC PACKAGE

- Output latched and valid into next cycle
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses, Data-out, Data-in, and Chip-Select
- Compatible with MK4027

PIN ASSIGNMENT



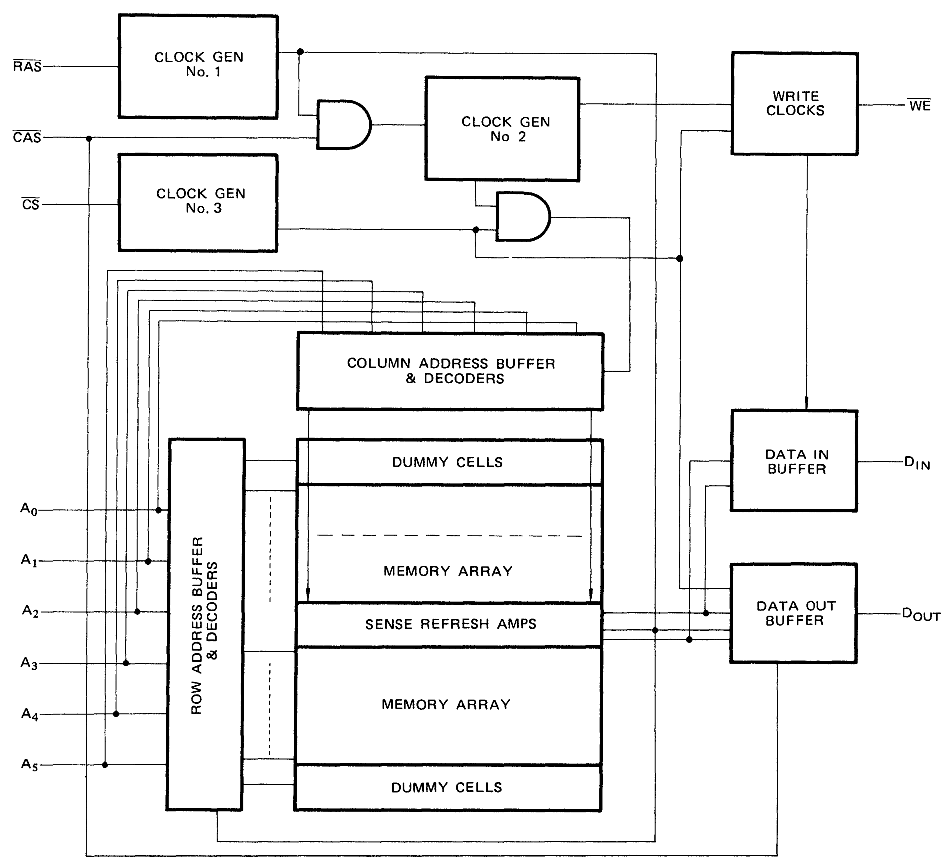
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any type of voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{BB}	V_{IN}, V_{OUT}	-0.5 to +20	V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}	V_{DD}, V_{CC}	-0.5 to +15	V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0V$)	–	0	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.0	W
Short circuit output current	–	50	mA

Note: Permanent damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB 8227 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_5$, D_{IN}, $\overline{CS}$	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	10	pF
Output Capacitance D_{OUT}	C_{OUT}	—	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	NOTES	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	1	V_{DD}	10.8	12.0	13.2	V	0°C to +70°C
	1 2	V_{CC}	4.5	5.0	5.5	V	
	1	V_{SS}	0	0	0	V	
	1	V_{BB}	-4.5	-5.0	-5.5	V	
Input High Voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IHC}	2.4		7.0	V	
Input High Voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IH}	2.2		7.0	V	
Input Low Voltage, all inputs	1	V_{IL}	-1.0		0.8	V	

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	Min	Max	Units
OPERATING CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} min)		I_{DD1} I_{BB1}		35 300	mA μA
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IHC}, output disabled)		I_{DD2}		2.0	mA
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} min)		I_{DD3}		25	mA
V_{CC} POWER SUPPLY CURRENT ($\overline{CS}$ = V_{IH})	3	I_{CC}	-10	10	μA
INPUT LEAKAGE CURRENT Input leakage current, any input (V_{BB} = -5V, 0V ≤ V_{IN} ≤ 7V, all other pins not under test = 0V)		I_{IL}	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is high impedance state, $\overline{CS}$ = V_{IH})		I_{OL}	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = -5mA) Output low voltage (I_{OL} = 3.2mA)		V_{OH} V_{OL}	2.4	 0.4	V V

Notes:

1) All voltages are referenced to V_{SS}.
2) Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in the standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
3) When Data out is enabled, V_{CC} power supply current depends upon output loading; V_{CC} is connected to the output buffer only.

DYNAMIC CHARACTERISTICS NOTES 4, 5, 6

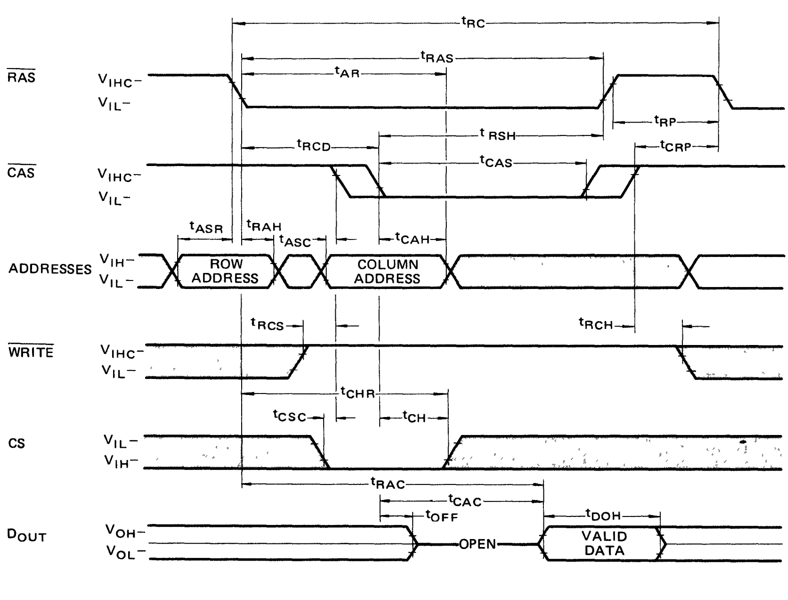
(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 8227E		MB 8227H		Units
			Min	Max	Min	Max	
Time between Refresh		t_{REF}		2		2	ms
Random Read/Write Cycle Time		t_{RC}	375		320		ns
Read-Write Cycle Time		t_{RWC}	420		330		ns
Access Time from $\overline{RAS}$	7 9	t_{RAC}		200		150	ns
Access Time from $\overline{CAS}$	8 9	t_{CAC}		135		100	ns
Output Buffer Turn Off Delay		t_{OFF}		50		40	ns
Transition Time		t_T	3	50	3	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	32000	150	32000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135		100		ns
$\overline{CAS}$ Precharge Time		t_{CP}	80		60		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135		100		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	t_{RCD}	25	65	20	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0		0		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	25		20		ns
Column Address Set Up Time		t_{ASC}	−10		−10		ns
Column Address Hold Time		t_{CAH}	55		45		ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120		95		ns
Chip Select Set Up Time		t_{CSC}	−10		−10		ns
Chip Select Hold Time		t_{CH}	55		45		ns
Chip Select Hold Time Referenced to $\overline{RAS}$		t_{CHR}	120		95		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time		t_{RCH}	0		0		ns
Write Command Set Up Time	11	t_{WCS}	0		0		ns
Write Command Hold Time		t_{WCH}	55		45		ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	120		95		ns
Write Command Pulse Width		t_{WP}	55		45		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	135		100		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	135		100		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	55		45		ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120		95		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	11	t_{CWD}	80		60		ns
$\overline{RAS}$ to $\overline{WE}$ Delay	11	t_{RWD}	145		110		ns
Data Out Hold Time		t_{DOH}	32		32		µs

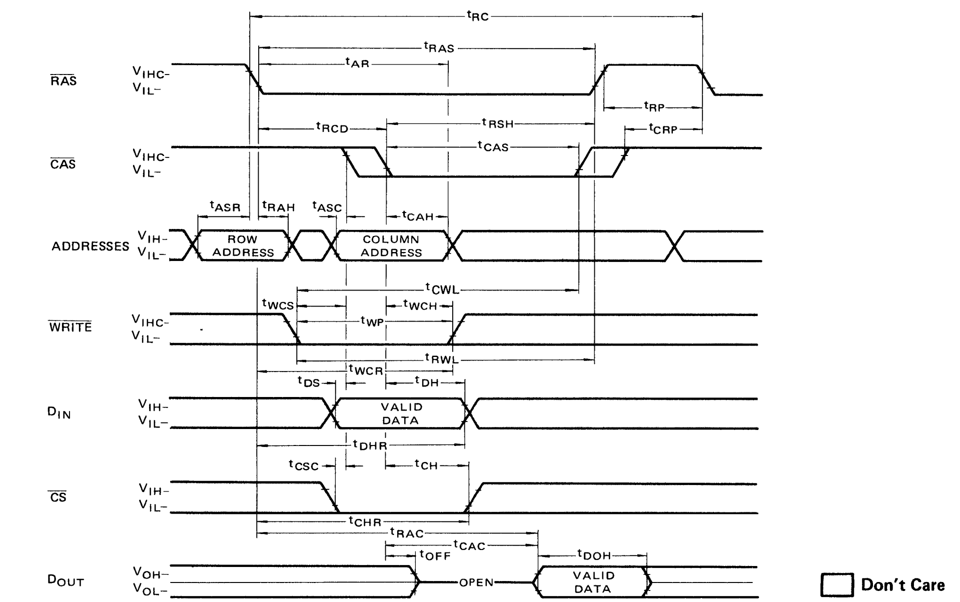
Notes:

4) Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5) Dynamic measurements assume t_T=5ns.
6) V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
7) Assumes that $t_{RCD} \leqslant t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8) Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).
9) Measured with a load equivalent to 2 TTL loads and 100pF.
10) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} will contain the data written into the selected cell.
If $t_{CWD} \geqslant t_{CWD}$ (min) and $t_{RWD} \geqslant t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

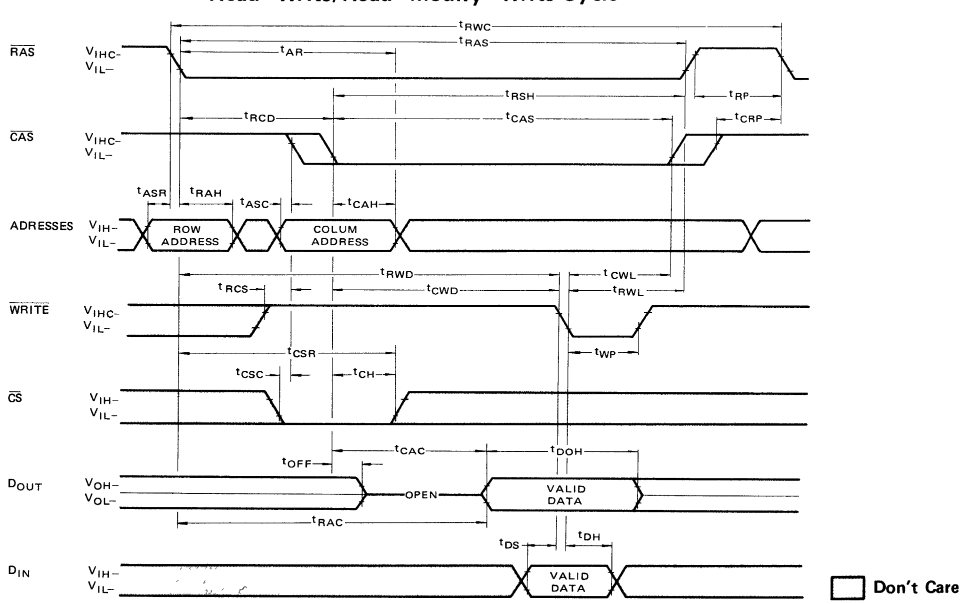
Read Cycle Timing Diagram



Write Cycle (Early Write)



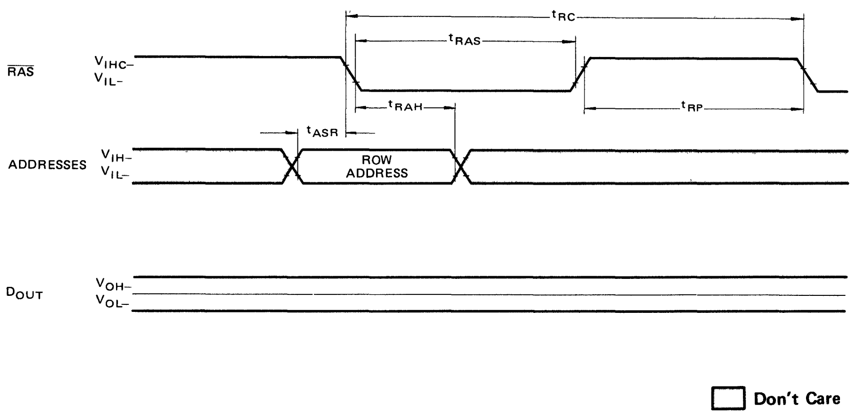
Read–Write/Read–Modify–Write Cycle



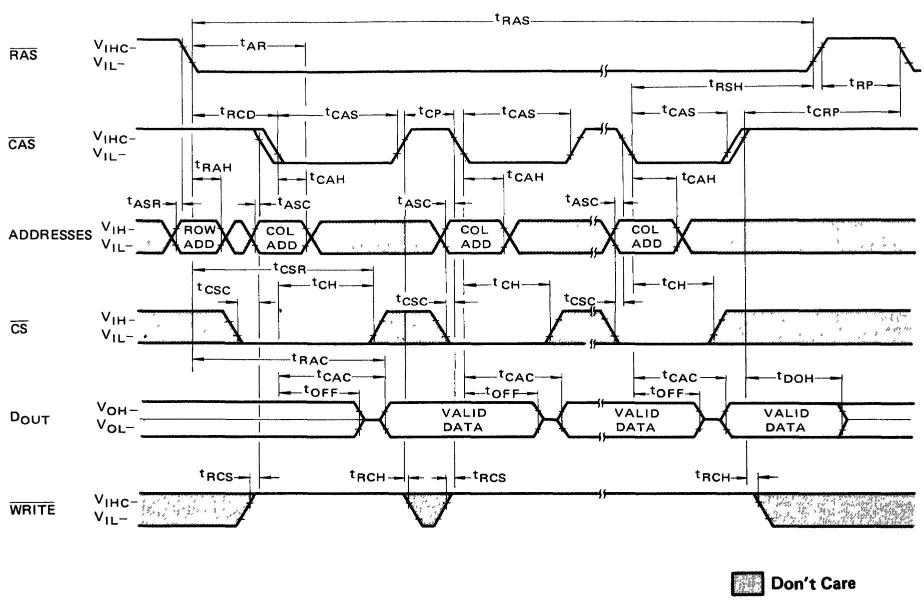
MOS Memories

"$\overline{\text{RAS}}$–ONLY" Refresh Cycle

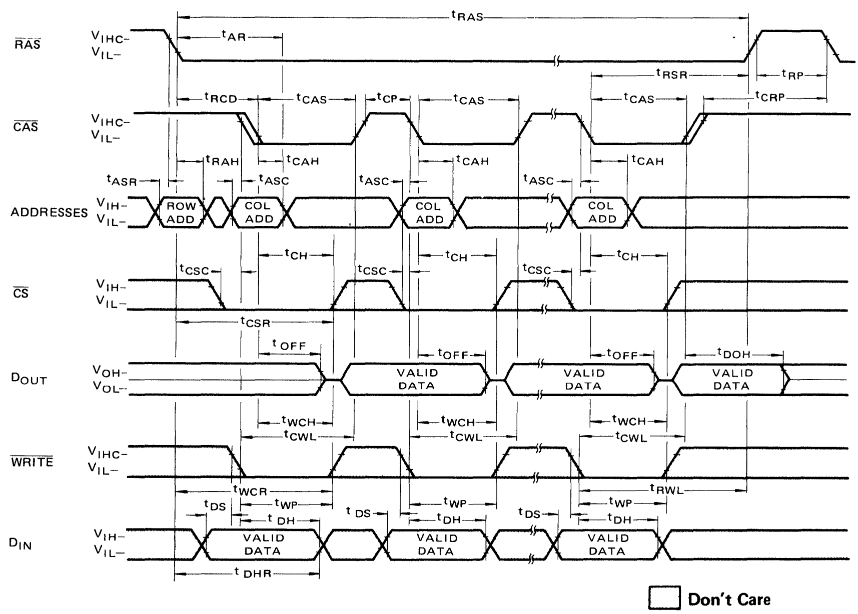
NOTE: D_{OUT} remains unchanged from previous cycle.



Page Mode Read Cycle



Page Mode Write Cycle



DESCRIPTION

Address Inputs:
Twelve binary input address bits are required to decode any one of the 4096 storage locations of the MB 8227. The twelve input address bits are multiplexed, six at a time, into the chip via the address input pins (A_0 through A_5). The Row Address Strobe, $\overline{RAS}$, latches the 6 row address bits when a negative going TTL level clock is applied to $\overline{RAS}$; and the Column Address Strobe, $\overline{CAS}$, latches the 6 column address bits plus Chip Select, $\overline{CS}$, when a subsequent negative going TTL level clock is applied to $\overline{CAS}$. $\overline{CAS}$ is internally "gated" by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and before column address information is actually required. This gated $\overline{CAS}$ feature simplifies timing requirements for multiplexed inputs and minimizes the system access and cycle time.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. The data input pin is disabled when the read mode is selected. $\overline{WE}$ can be driven by a standard TTL circuit without a pull-up resistor.

Data Input:
Data to be written into a selected memory cell is latched into an on-chip register during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, strobes the Data in (D_{IN}) register. Set-up and hold times are referenced to $\overline{WE}$ or $\overline{CAS}$, whichever negative transition occurs later. If the chip is unselected, $\overline{CS}$ high at $\overline{CAS}$ time, $\overline{WE}$ commands are not executed and data in the memory is not affected.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output data is latched until $\overline{CAS}$ is brought low. Then the output, D_{OUT}, will go to an open circuit regardless of the state of any other input pin. In a read, read-modify-write, or delayed write cycle, if the chip is selected, the output latch and buffer will contain the data read from the selected memory cell after access time. In a write cycle ($\overline{WE}$ low before $\overline{CAS}$ low), if the chip is selected, the output latch and buffer will contain the input

(cont'd)

data after access time. The output remains valid until the next negative transition of $\overline{CAS}$. $\overline{RAS}$-only refresh cycles will not affect valid data.

Page-Mode:
Page-mode operation permits strobing the row-address into the MB 8227 while holding $\overline{RAS}$ at a logic low(0) throughout all successive memory operations in which the row address does not change. This permits successive memory operations at multiple column addresses with the same row address with higher speed and lower power. The power dissipated by the negative going edge of $\overline{RAS}$ is saved; and the access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

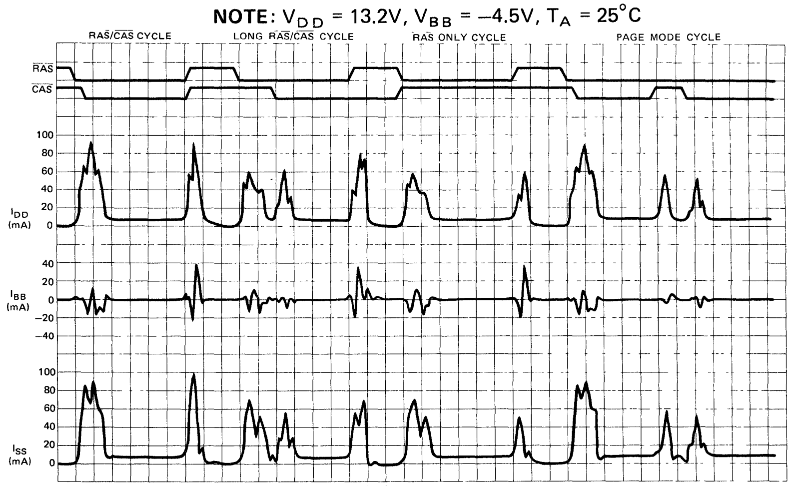
Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 64 row addresses at least every two milliseconds. Any operation in which $\overline{RAS}$ transits accomplishes refresh. Regardless of the state of $\overline{CS}$, a read cycle will refresh the selected row. Refresh will also occur during a write or read-modify-write cycle, but the chip should be unselected to prevent data being written into the selected memory location. If, during a refresh cycle, the MB 8227 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if $\overline{RAS}$-only refresh is continued for long periods, the output buffer may lose data. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Power Considerations:
The output buffer of the MB 8227 can be powered via V_{CC} from the supply voltage (normally 5 volts) to which the memory is interfaced. In standby operation, V_{CC} may be removed without affecting refresh. Thus standby power is conserved because all memory functions may be turned off except for $\overline{RAS}$ timing and refresh addresses.
Most of the MB 8227 circuitry, including sense amplifiers, is dynamic, and most of the power drain comes from an address strobe ($\overline{RAS}$ or $\overline{CAS}$) edge. Thus, dynamic power dissipation depends mostly on operating frequency.
To minimize power dissipation, the Row Address Strobe, $\overline{RAS}$, should only be applied to selected IC's. $\overline{CAS}$ must be supplied to all the IC's in a system in order to turn off unselected outputs. But IC's that didn't receive a $\overline{RAS}$ input will not dissipate power on $\overline{CAS}$ edges except for that needed to turn off outputs. If $\overline{RAS}$ is supplied only to selected chips, $\overline{CS}$ can be at logic zero. Chips that receive $\overline{CAS}$, but not $\overline{RAS}$, will be unselected regardless of $\overline{CS}$. However, for refresh, either the $\overline{CS}$ input or $\overline{CAS}$ must be high to prevent wired-OR outputs from turning on simultaneously.

Power Up:
No particular power supply sequencing is required for the MB 8227. However, absolute maximum ratings must be adhered to. Thus, V_{BB} should be turned on first and turned off last, and V_{BB} should be less than V_{SS} when V_{DD} is turned on. After power is applied, several cycles are required before proper operation is assured. About eight refresh cycles should be sufficient to accomplish this.

Current Waveforms

NOTE: V_{DD} = 13.2V, V_{BB} = –4.5V, T_A = 25°C



TYPICAL CHARACTERISTICS CURVES

Fig. 2 – NORMALIZED ACCESS TIME vs V_{DD} SUPPLY VOLTAGE

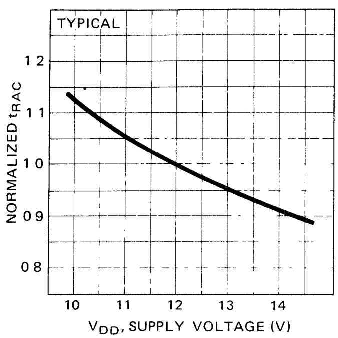


Fig. 3 – NORMALIZED ACCESS TIME vs V_{BB} SUPPLY VOLTAGE

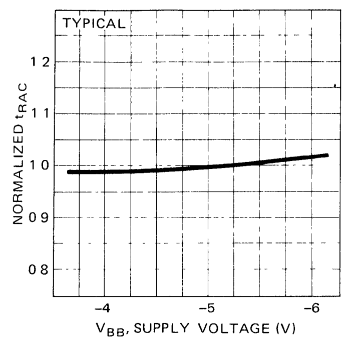


Fig. 4 – NORMALIZED ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

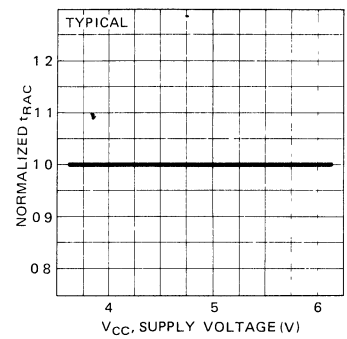


Fig. 5 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

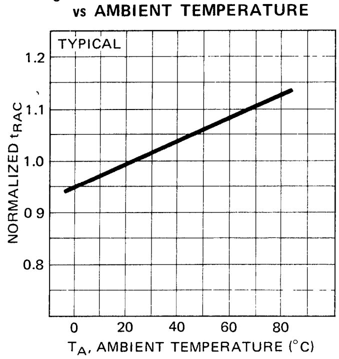


Fig. 6 – I_{DD1} (AVERAGE) vs CYCLE RATE

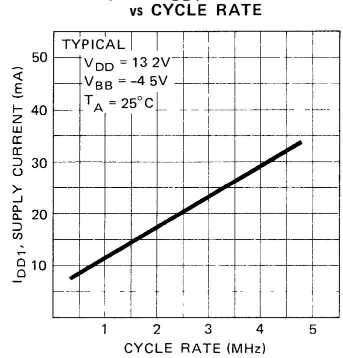


Fig. 7 – I_{DD1} (AVERAGE) vs V_{DD} SUPPLY VOLTAGE

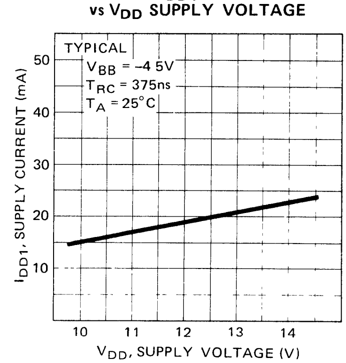


Fig. 8 – I_{DD1} (AVERAGE) vs AMBIENT TEMPERATURE

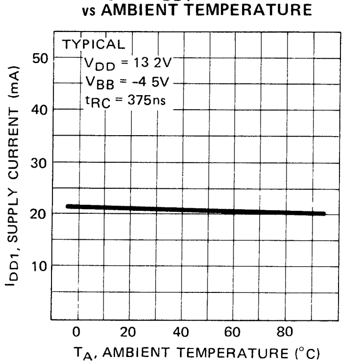


Fig. 9 – I_{DD2} (STANDBY) vs V_{DD} SUPPLY VOLTAGE

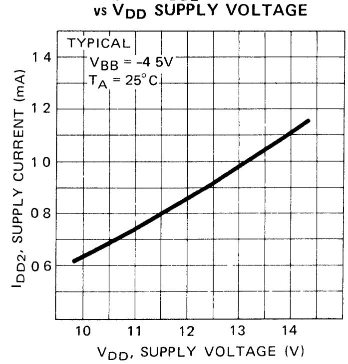
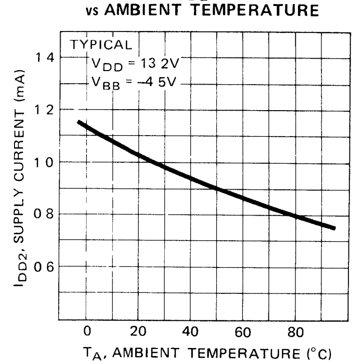
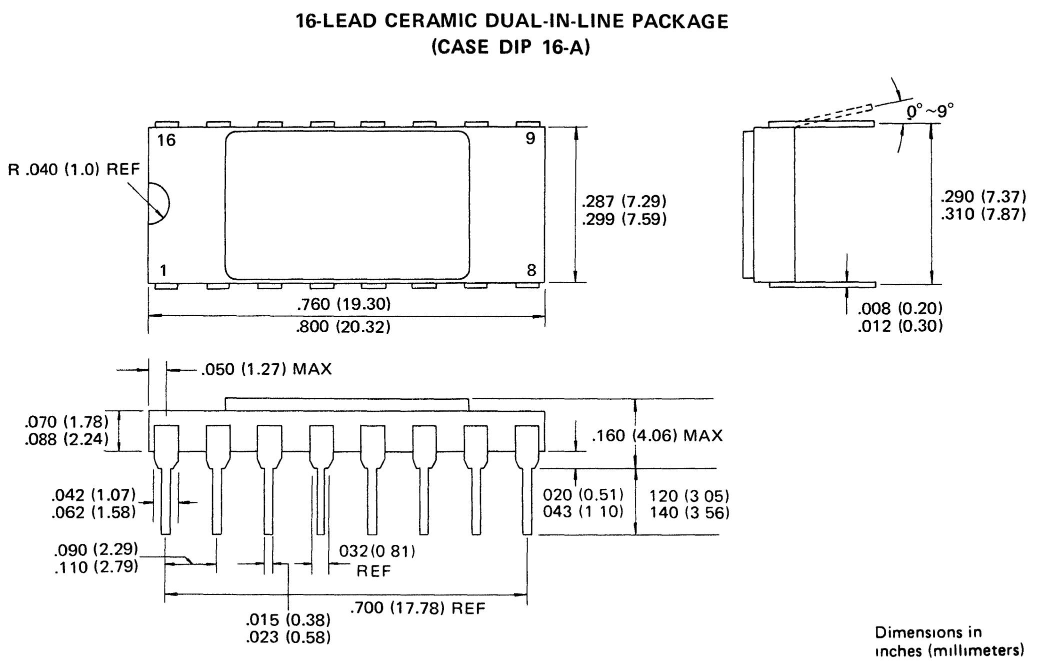


Fig. 10 – I_{DD2} (STANDBY) vs AMBIENT TEMPERATURE



PACKAGE DIMENSIONS



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specification.

Fig. 11 — I_{DD3} ($\overline{RAS}$-ONLY) vs CYCLE RATE

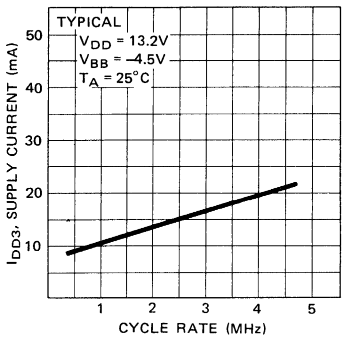


Fig. 12 — I_{DD3} ($\overline{RAS}$-ONLY) vs V_{DD} SUPPLY VOLTAGE

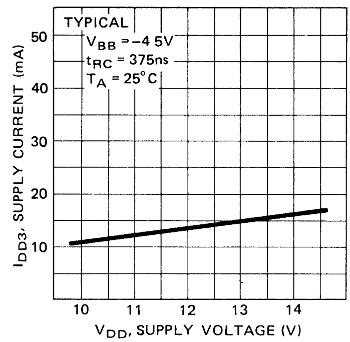


Fig. 13 — I_{DD3} ($\overline{RAS}$-ONLY) vs AMBIENT TEMPERATURE

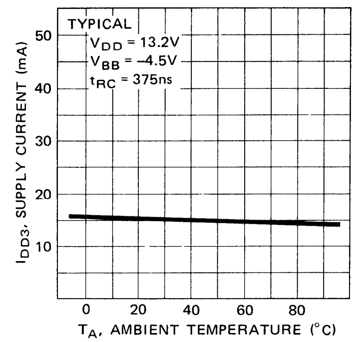


Fig. 14 — V_{IHC}, V_{ILC} INPUT LEVELS vs V_{DD} SUPPLY VOLTAGE

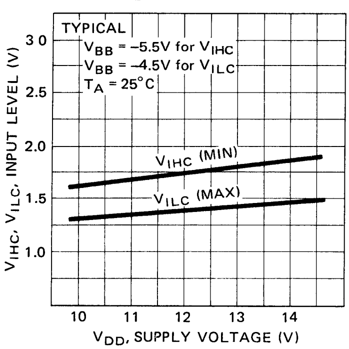


Fig. 15 — V_{IHC}, V_{ILC} INPUT LEVELS vs V_{BB} SUPPLY VOLTAGE

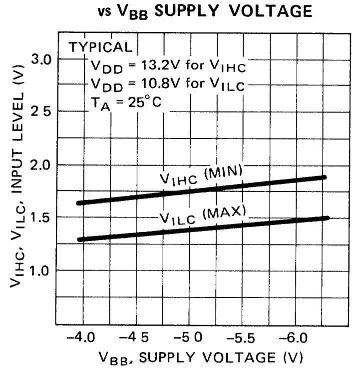


Fig. 16 — V_{IHC}, V_{ILC} INPUT LEVELS vs AMBIENT TEMPERATURE

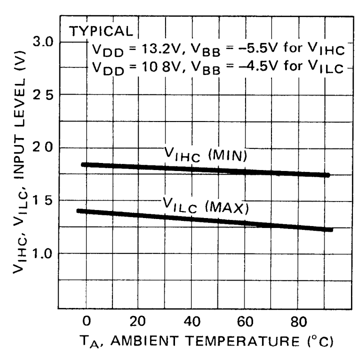


Fig. 17 — V_{IH}, V_{IL} INPUT LEVELS vs V_{DD} SUPPLY VOLTAGE

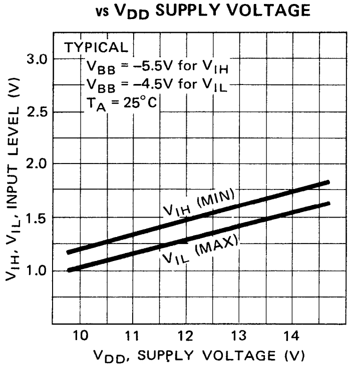


Fig. 18 — V_{IH}, V_{IL} INPUT LEVELS vs V_{BB} SUPPLY VOLTAGE

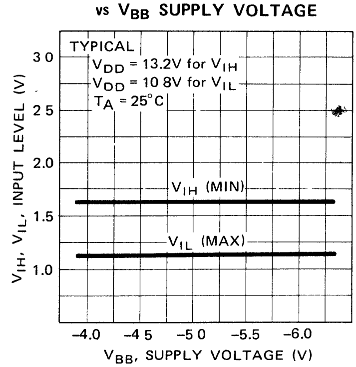
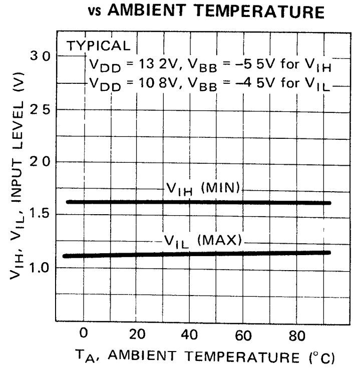


Fig. 19 — V_{IH}, V_{IL} INPUT LEVELS vs AMBIENT TEMPERATURE



FUJITSU

MOS 16384-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 8116N/E/H

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

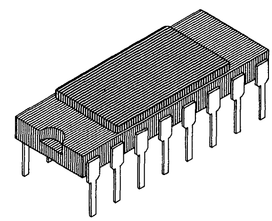
The Fujitsu MB 8116 is a fully decoded, dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Mutliplexed row and column address inputs permit the MB 8116 to be housed in a standard 16-pin DIP. Pinouts conform to the accepted industry standard.

The MB 8116 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerances are 10%. All inputs are TTL compatible; the output is three-state TTL.

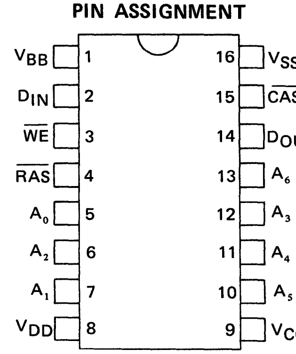
- 16,384 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  150 ns max. (MB 8116H)
  200 ns max. (MB 8116E)
  250 ns max. (MB 8116N)
- Cycle time,
  375 ns min. (MB 8116E/H)
  410 ns min. (MB 8116N)
- Low power: 462 mW active, 20 mW standby (max.)
- 10% tolerance on +12V, ±5V supplies
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refresh cycles



CASE DIP16-A
CERAMIC PACKAGE

- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- Compatible with MK4116 and TMS4070

PIN ASSIGNMENT



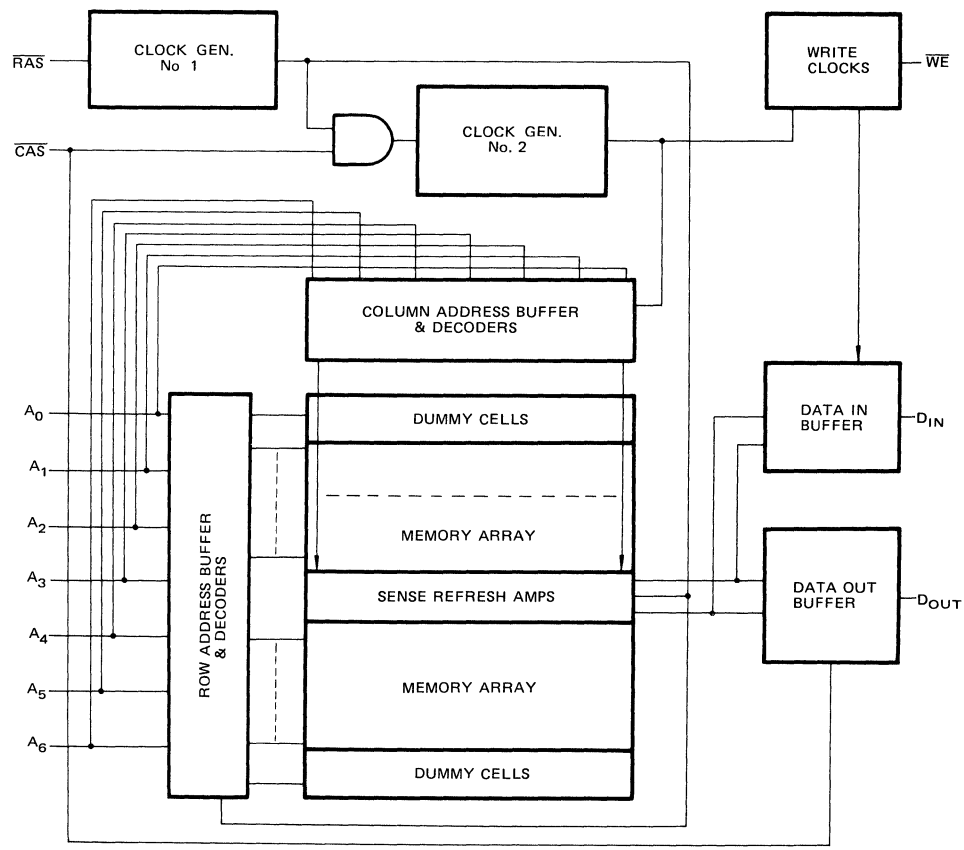
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{BB}	V_{IN}, V_{OUT}	-0.5 to + 20	V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}	V_{DD}, V_{CC}	-0.5 to + 15	V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0V$)	–	0	V
Storage Temperature	T_{stg}	- 55 to +150	°C
Power Dissipation	P_D	1.0	W
Short circuit output current	–	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB 8116 BLOCK DIAGRAM



CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_6$, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	10	pF
Output Capacitance D_{OUT}	C_{OUT}	—	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	NOTES	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	1	V_{DD}	10.8	12.0	13.2	V	0°C to +70°C
	1 2	V_{CC}	4.5	5.0	5.5	V	
	1	V_{SS}	0	0	0	V	
	1	V_{BB}	-4.5	-5.0	-5.5	V	
Input High Voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IHC}	2.7	—	6.5	V	
Input High Voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V_{IL}	-1.0	—	0.8	V	

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	Min	Max	Units
OPERATING CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375ns)		I_{DD1} I_{BB1}		35 200	mA μA
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IHC})		I_{DD2} I_{BB2}		1.5 100	mA μA
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC} ; t_{RC} = 375ns)		I_{DD3} I_{BB3}		25 200	mA μA
PAGE MODE CURRENT Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling ; t_{PC} = 225ns)		I_{DD4} I_{BB4}		27 200	mA μA
V_{CC} POWER SUPPLY CURRENT (Data out is disabled)	3	I_{CC}	-10	10	μA
INPUT LEAKAGE CURRENT Input leakage current, any input (V_{BB}= -5V, 0V$\leq V_{IN} \leq$7V, all other pins not under test = 0V)		I_{IL}	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled)		I_{OL}	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = -5mA) Output low voltage (I_{OL} = 4.2mA)		V_{OH} V_{OL}	2.4 	 0.4	V V

Notes:

1) All voltages are referenced to V_{SS}.
2) Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in the standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH}(min) specification is not guaranteed in this mode.
3) When Data out is enabled, V_{CC} power supply current depends upon output loading; V_{CC} is connected to the output buffer only.

DYNAMIC CHARACTERISTICS NOTES 4, 5, 6

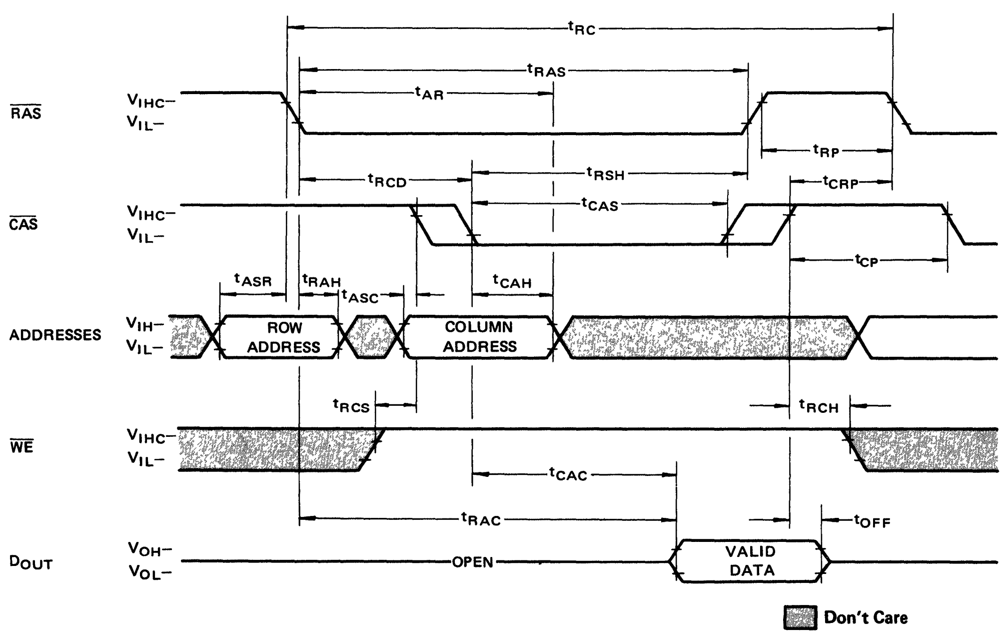
(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 8116E		MB 8116H		Units
			Min	Max	Min	Max	
Time between Refresh		t_{REF}		2		2	ms
Random Read/Write Cycle Time		t_{RC}	375		375		ns
Read-Write Cycle Time		t_{RWC}	375		375		ns
Page Mode Cycle Time		t_{PC}	225		170		ns
Access Time from $\overline{RAS}$	7 9	t_{RAC}		200		150	ns
Access Time from $\overline{CAS}$	8 9	t_{CAC}		135		100	ns
Output Buffer Turn Off Delay		t_{OFF}	0	50	0	50	ns
Transition Time		t_T	3	50	3	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	32000	150	32000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135		100		ns
$\overline{CAS}$ Precharge Time		t_{CP}	80		60		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	10000	100	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	t_{RCD}	30	65	25	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	−20		−20		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	25		20		ns
Column Address Set Up Time		t_{ASC}	-5		-5		ns
Column Address Hold Time		t_{CAH}	55		45		ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120		95		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time		t_{RCH}	10		10		ns
Write Command Set Up Time	11	t_{WCS}	-10		-10		ns
Write Command Hold Time		t_{WCH}	55		45		ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	120		95		ns
Write Command Pulse Width		t_{WP}	55		45		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80		60		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80		60		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	55		45		ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120		95		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	11	t_{CWD}	95		70		ns
$\overline{RAS}$ to $\overline{WE}$ Delay	11	t_{RWD}	160		120		ns

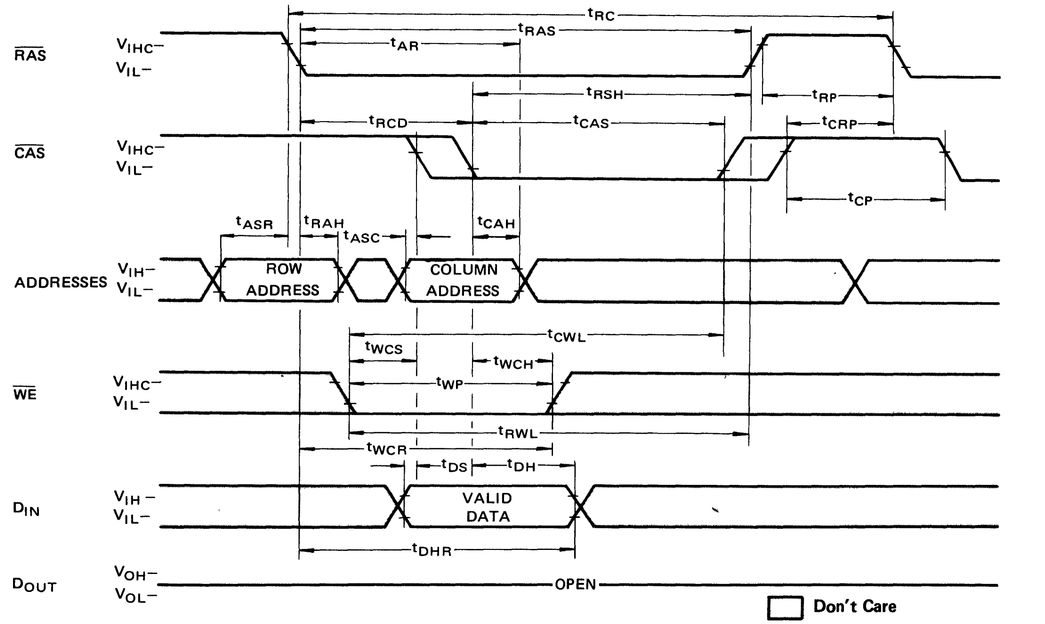
Notes:

4) Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5) Dynamic measurements assume t_T=5ns.
6) V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
7) Assumes that $t_{RCD} \leqslant t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8) Assumes that $t_{RCD} \geqslant t_{RCD}$(max).
9) Measured with a load equivalent to 2 TTL loads and 100pF.
10) Operation within the t_{RCD} (max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
11) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqslant 0$ns or $t_{WCS} \geqslant t_{RCD}-t_{RCD}$(max), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
If $t_{CWD} \geqslant t_{CWD}$(min) and $t_{RWD} \geqslant t_{RWD}$(min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

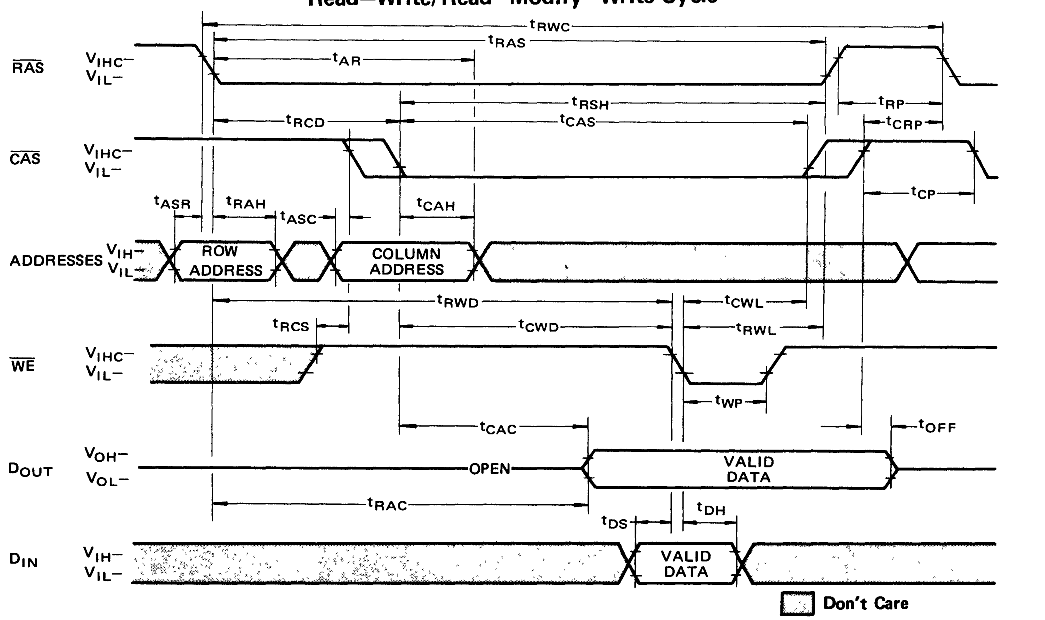
Read Cycle Timing Diagram



Write Cycle (Early Write)



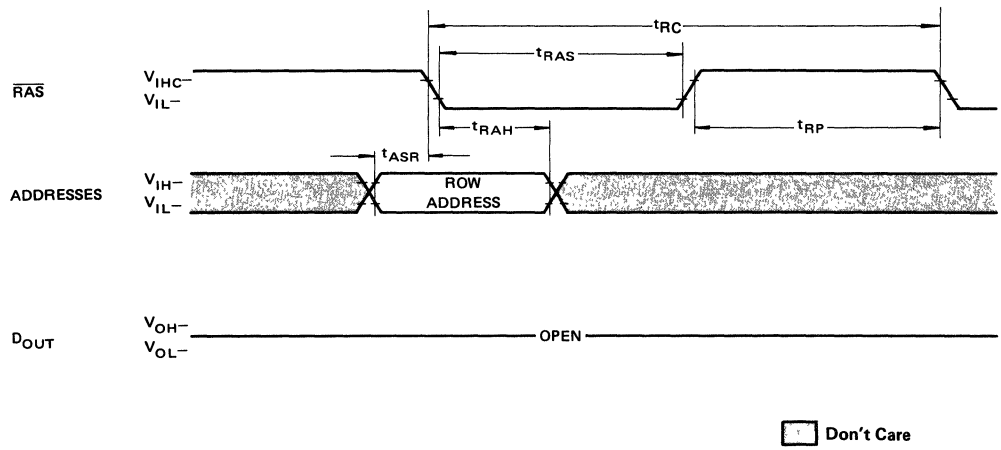
Read–Write/Read–Modify–Write Cycle



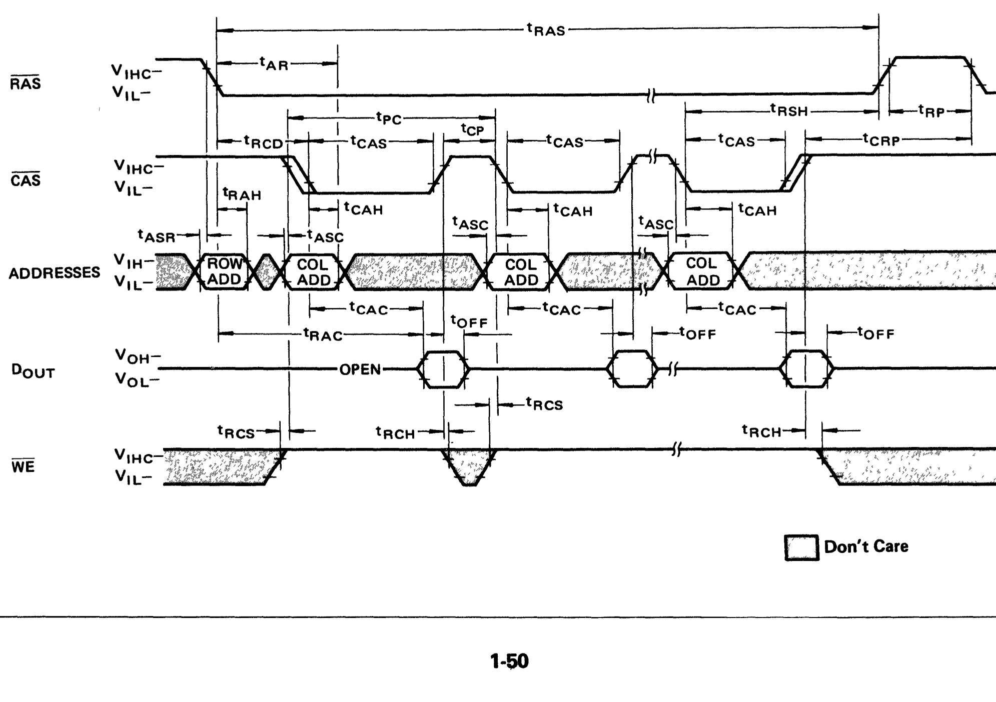
MOS Memories

"$\overline{RAS}$–ONLY" Refresh Cycle

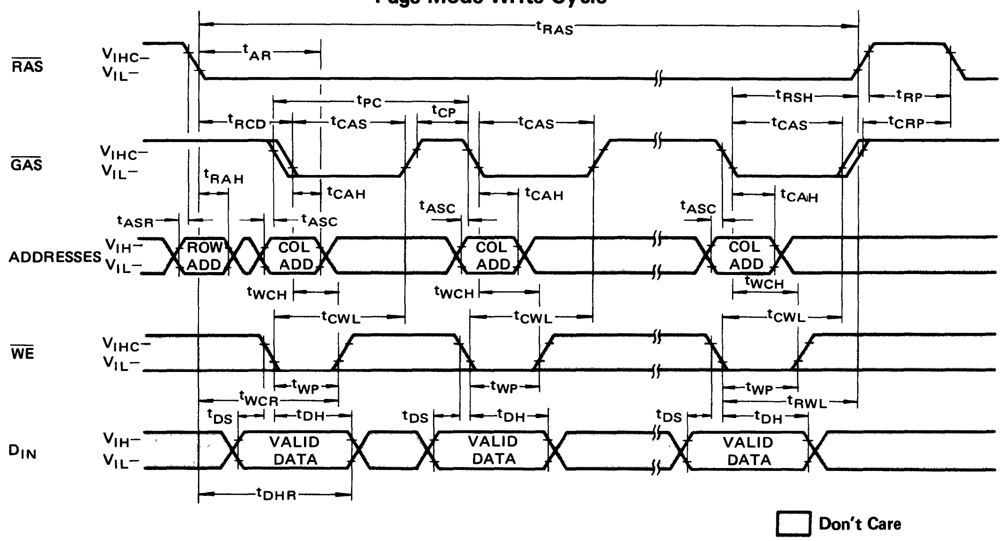
NOTE: $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = Don't care



Page Mode Read Cycle



Page Mode Write Cycle



DESCRIPTION

Address Inputs:
A total of fourteen binary input address bits are required to decode any 1 of 16,384 storage cell locations within the MB 8116. Seven row-address bits are established on the input pins (A_0 through A_6) and latched with the Row Address Strobe ($\overline{RAS}$). Then seven column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected. $\overline{WE}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input:
Data is written into the MB 8116 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

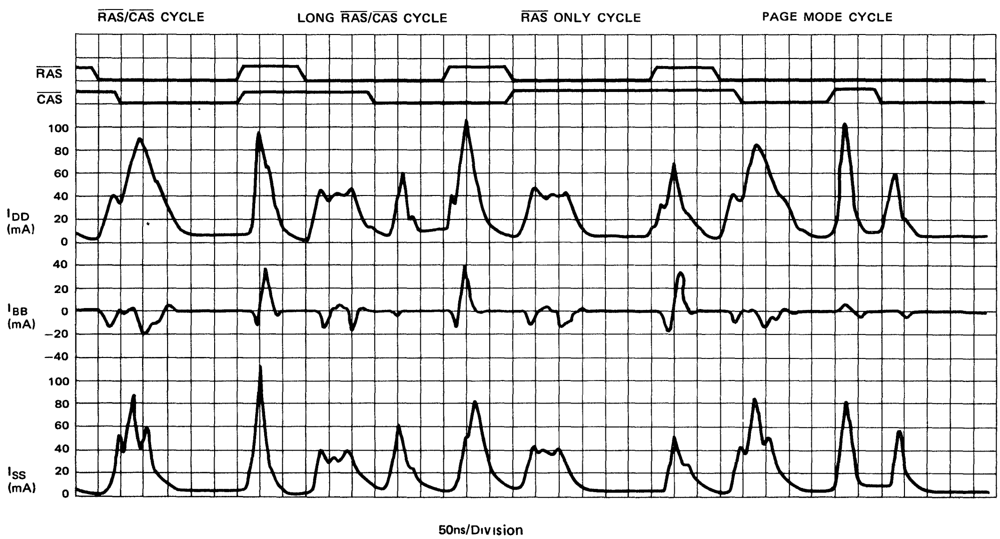
Page-Mode:
Page-mode operation permits strobing the row-address into the MB 8116 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

(cont'd)

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses at least every two milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Current Waveforms

NOTE: V_{DD} = 13.2V, V_{BB} = −4.5V, T_A = 25°C



TYPICAL CHARACTERISTICS CURVES

Fig. 2 — NORMALIZED ACCESS TIME vs V_{DD} SUPPLY VOLTAGE

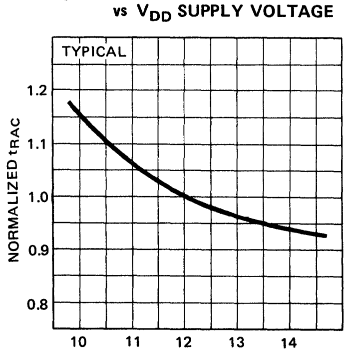


Fig. 3 — NORMALIZED ACCESS TIME vs V_{BB} SUPPLY VOLTAGE

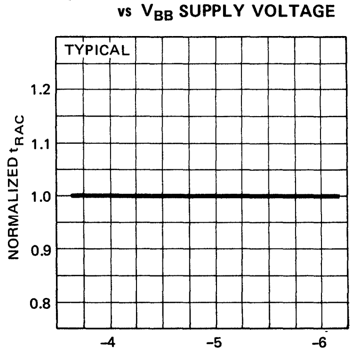


Fig. 4 — NORMALIZED ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

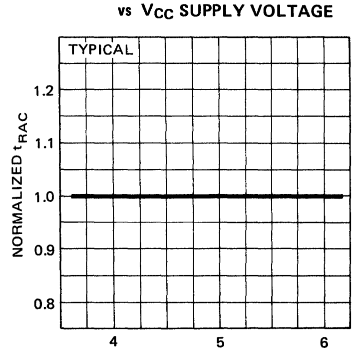


Fig. 5 — NORMALIZED ACCESS TIME vs T_j JUNCTION TEMPERATURE

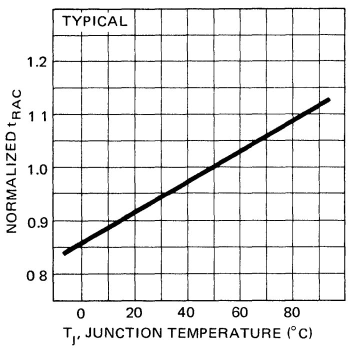


Fig. 6 — I_{DD1} (AVERAGE) vs CYCLE RATE

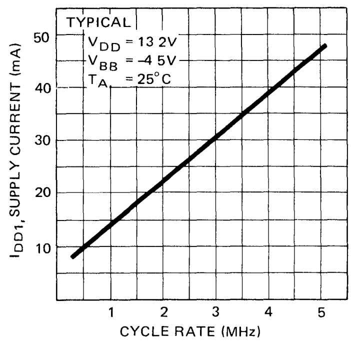


Fig. 7 — I_{DD1} (AVERAGE) vs V_{DD} SUPPLY VOLTAGE

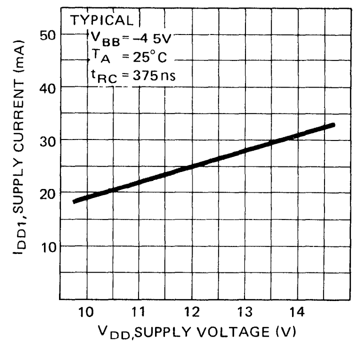


Fig. 8 — I_{DD1} (AVERAGE) vs T_j JUNCTION TEMPERATURE

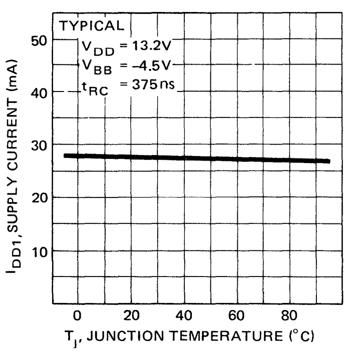


Fig. 9 — I_{DD2} (STANDBY) vs V_{DD} SUPPLY VOLTAGE

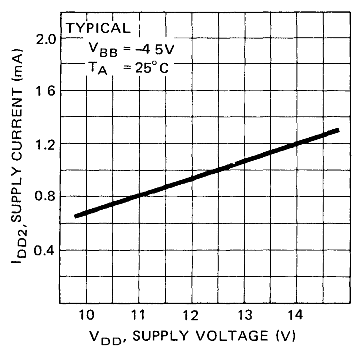


Fig. 10 — I_{DD2} (STANDBY) vs T_j JUNCTION TEMPERATURE

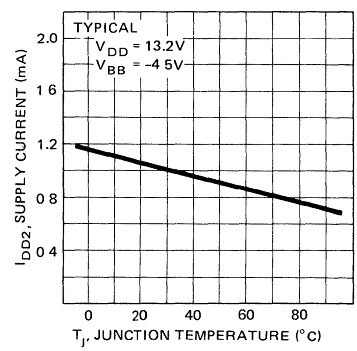


Fig. 11 — I_{DD3} ($\overline{RAS}$–ONLY) vs CYCLE RATE

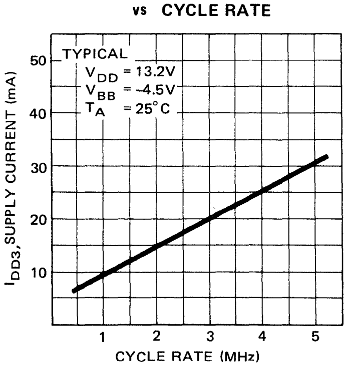


Fig. 12 — I_{DD3} ($\overline{RAS}$–ONLY) vs V_{DD} SUPPLY VOLTAGE

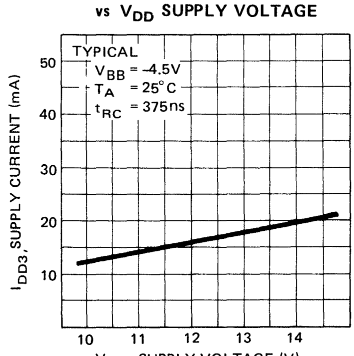


Fig. 13 — I_{DD3} ($\overline{RAS}$–ONLY) vs T_j JUNCTION TEMPERATURE

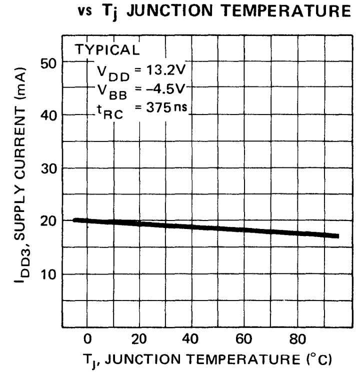


Fig. 14 — I_{DD4} (PAGE—MODE) vs CYCLE RATE

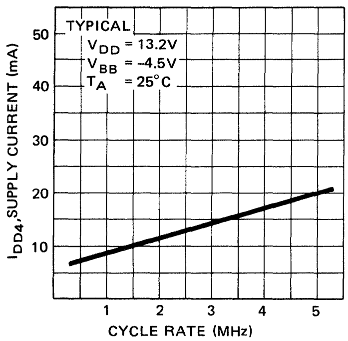


Fig. 15 — I_{DD4} (PAGE—MODE) vs V_{DD} SUPPLY VOLTAGE

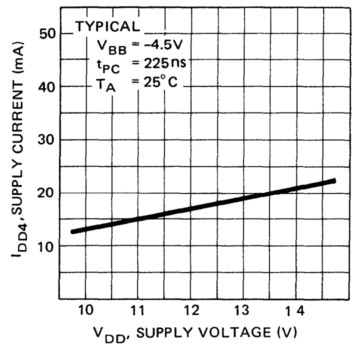


Fig. 16 — I_{DD4} (PAGE—MODE) vs T_j JUNCTION TEMPERATURE

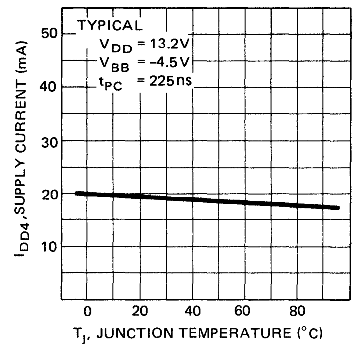


Fig. 17 — V_{IHC}, V_{ILC} INPUT LEVELS vs V_{DD} SUPPLY VOLTAGE

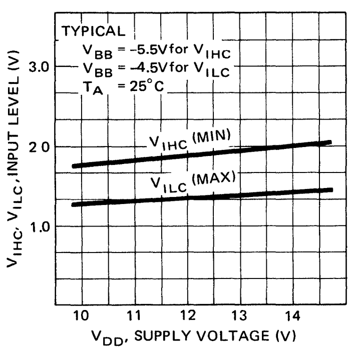


Fig. 18 — V_{IHC}, V_{ILC} INPUT LEVELS vs V_{BB} SUPPLY VOLTAGE

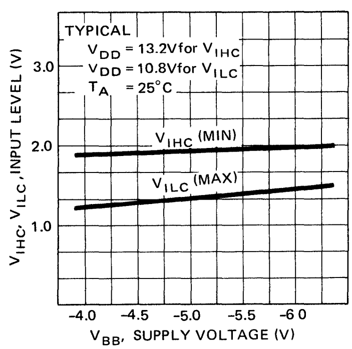


Fig. 19 — V_{IHC}, V_{ILC} INPUT LEVELS vs T_j JUNCTION TEMPERATURE

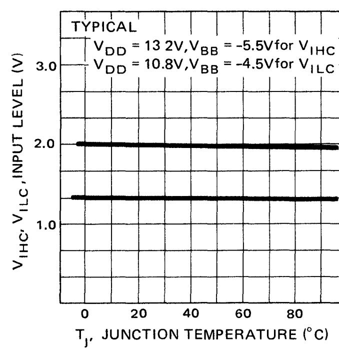


Fig. 20 — V_{IH}, V_{IL} INPUT LEVLES vs V_{DD} SUPPLY VOLTAGE

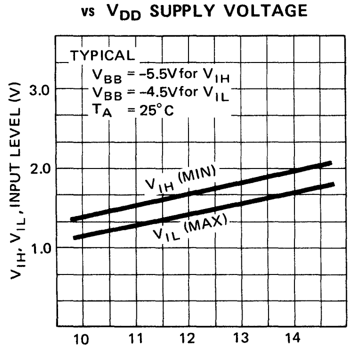


Fig. 21 — V_{IH}, V_{IL} INPUT LEVELS vs V_{BB} SUPPLY VOLTAGE

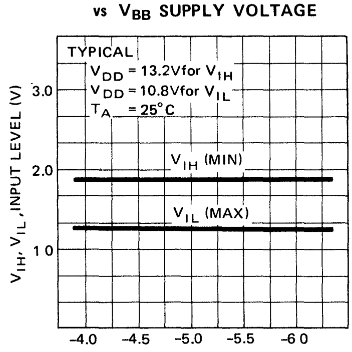
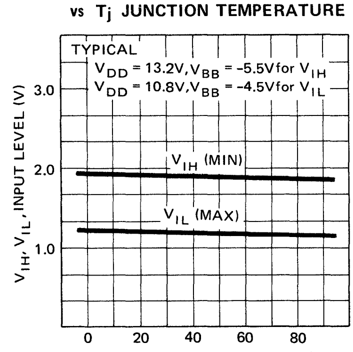
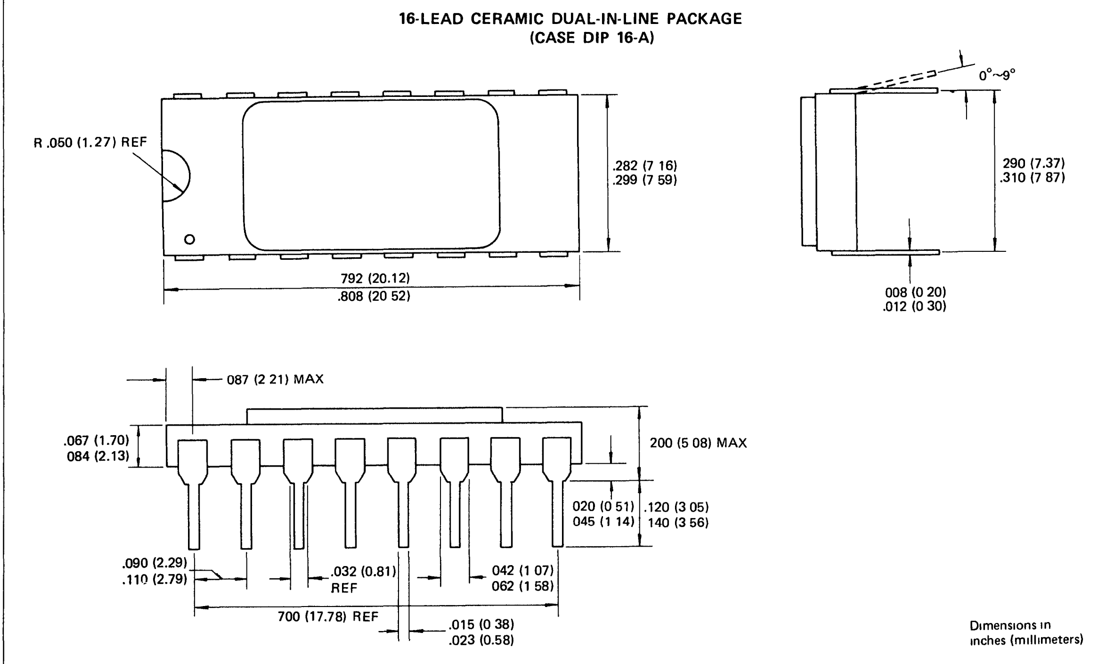


Fig. 22 — V_{IH}, V_{IL} INPUT LEVELS vs T_j JUNCTION TEMPERATURE



PACKAGE DIMENSIONS



FUJITSU

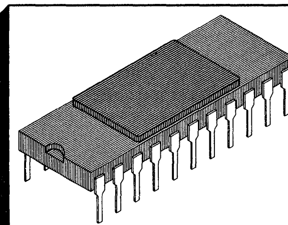
MOS 1024-BIT STATIC RANDOM ACCESS MEMORY

MB 8101N/E

1024-BIT STATIC RANDOM ACCESS MEMORY WITH SEPARATE I/O

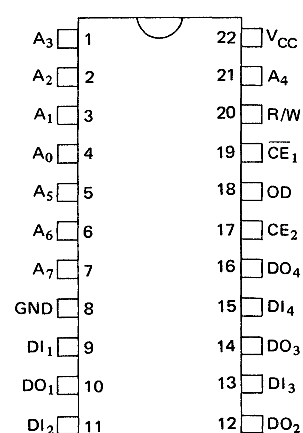
The Fujitsu MB 8101 is a 256 word by 4 bit static random access memory fabricated using N-channel silicon gate MOS technology. All devices are fully compatible with TTL logic families in all respects: inputs, outputs, and the use of a single +5V DC supply. For ease of use, two chip-enables permit selection of an individual package when outputs are OR-tied. All devices offer the advantages of low power dissipation, low cost, and high performance.

- 256 words x 4 bits organization
- Static operation: no clocks or refresh required
- Fast access time:
  250 ns max. (MB 8101E)
  450 ns max. (MB 8101N)
- Single +5V DC supply voltage
- TTL compatible inputs and outputs
- Three-state output with OR-tie capability
- Two chip enable leads for simplified memory expansion
- Output disable provided for use in common data bus systems
- Standard 22-pin DIP package
- Pin compatible with the 2101



CASE DIP22-A
CERAMIC PACKAGE

PIN ASSIGNMENT



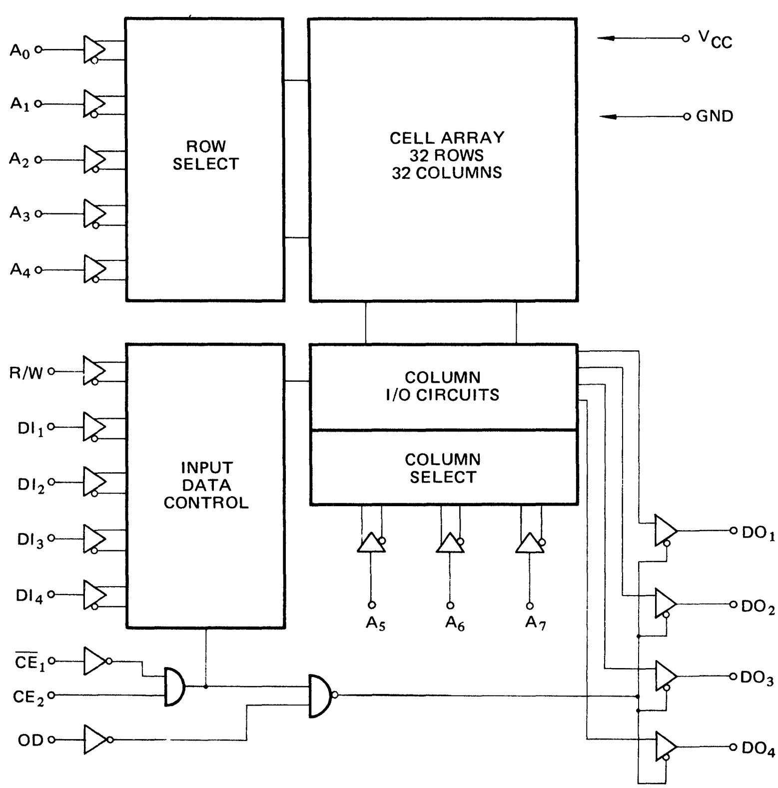
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7	V
Input Voltage	V_{IN}	–0.5 to +7	V
Output Voltage	V_{OUT}	–0.5 to +7	V
Storage Temperature	T_{stg}	–65 to +150	°C
Power Dissipation	P_D	1.0	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB 8101 BLOCK DIAGRAM



CAPACITANCE (T_A=25°C; f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} =0V)	C_{IN}	4	8	pF
Output Capacitance (V_{OUT}=0V)	C_{OUT}	8	12	pF

RECOMMENDED OPERATING CONDITIONS
(Referenced to V_{SS})

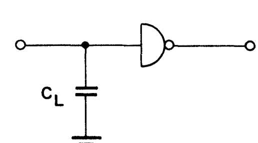
Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C to +70°C
Input Low Voltage	V_{IL}	-0.5		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	

STATIC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN}=0V to 5.25V)	I_{IL}		10	μA
Output Leakage Current ($\overline{CE}_1$=2.2V, V_{OUT}=4.0V)	I_{OL1}		10	μA
Output Leakage Current ($\overline{CE}_1$=2.2V, V_{OUT}=0.45V)	I_{OL2}		-25	μA
Power Supply Current (V_{IN}=5.25V, I_O=0mA, T_A=0°C)	I_{CC}		70	mA
Output Low Voltage (I_{OL}=2mA)	V_{OL}		0.45	V
Output High Voltage (I_{OH}=-150μA)	V_{OH}	2.2		V

Fig. 2 — DYNAMIC TEST CONDITIONS

Input Pulse Levels:	0.65V to 2.2V
Input Pulse Rise and Fall Time:	10ns
Timing Measurement Reference Levels	Input: 1.5V Output: 0.8V and 2.0V
Output Load:	1 TTL Gate and C_L=100pF



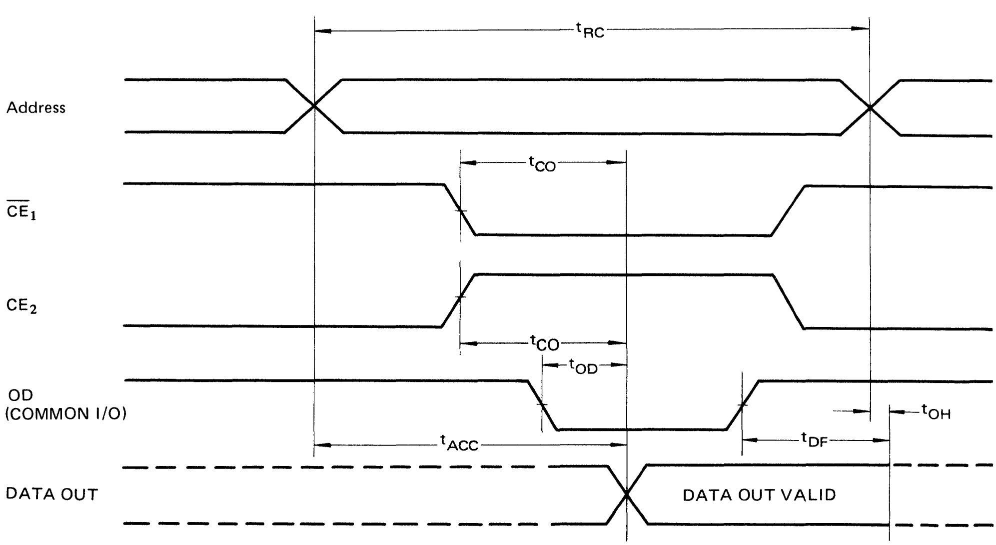
DYNAMIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB 8101N			MB 8101E			Unit
		Min	Typ	Max	Min	Typ	Max	
Read Cycle	t_{RC}	450			250			ns
Address Access Time	t_{ACC}			450			250	ns
Chip Enable to Output	t_{CO}			350			180	ns
Output Disable to Output	t_{OD}			300			130	ns
Data Output to High Impedance	t_{DF}	0		150	0		150	ns
Previous Read Data Valid after Change of Address	t_{OH}	40			40			ns

READ CYCLE TIMING DIAGRAM



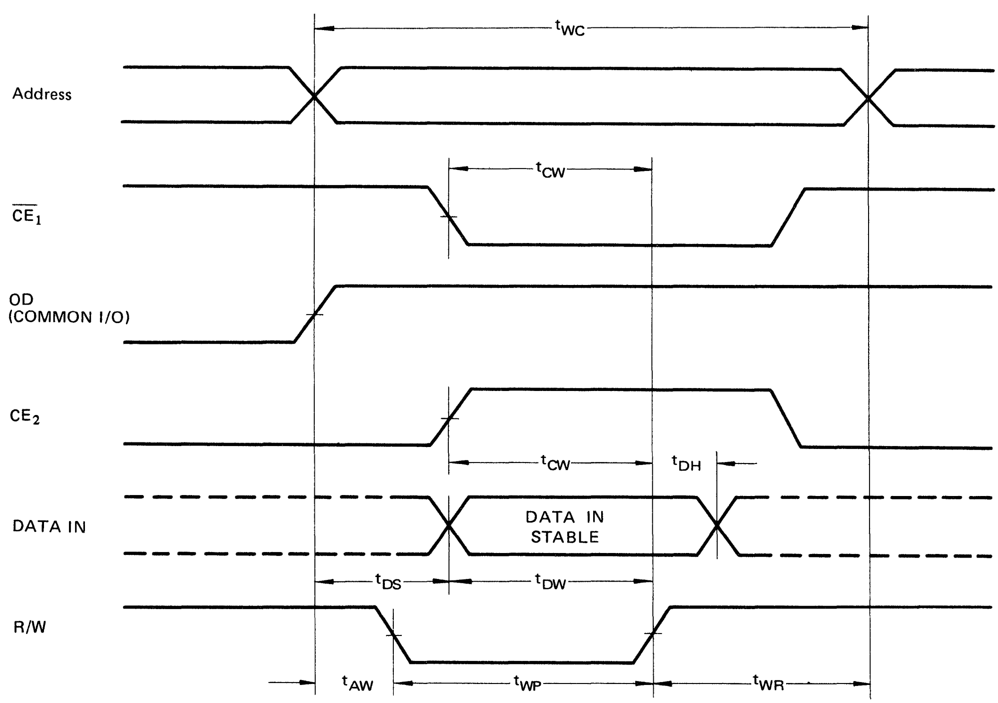
Notes: 1) t_{DF} is measured with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.

2) OD should be tied low for separate I/O operation.

WRITE CYCLE

Parameter	Symbol	MB 8101N			MB 8101E			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Cycle	t_{WC}	450			170			ns
Address to Write Setup	t_{AW}	100			20			ns
Chip Enable to Write	t_{CW}	350			100			ns
Data Setup Time	t_{DW}	200			100			ns
Data Hold Time	t_{DH}	100			0			ns
Write Pulse Width	t_{WP}	250			150			ns
Write Recovery Time	t_{WR}	50			0			ns
Output Disable Setup	t_{DS}	150			70			ns

WRITE CYCLE TIMING DIAGRAM



Notes: 1) t_{DF} is measured with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.

2) OD should be tied low for separate I/O operation.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – I_{CC} SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

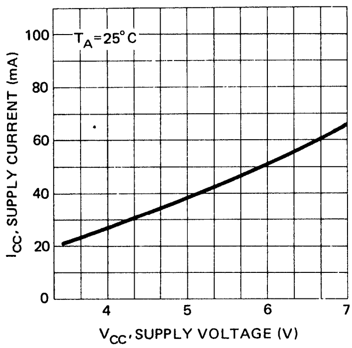


Fig. 4 – I_{CC} SUPPLY CURRENT vs AMBIENT TEMPERATURE

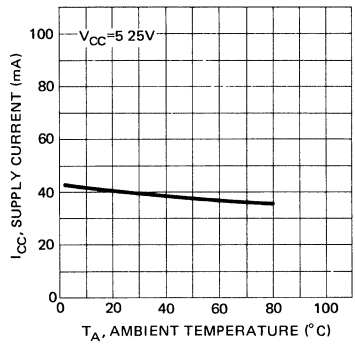


Fig. 5 – I_{OL} OUTPUT SINK CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

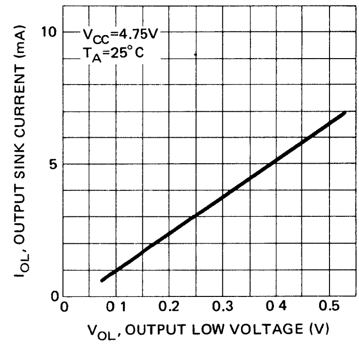


Fig. 6 – I_{OH} OUTPUT SOURCE CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

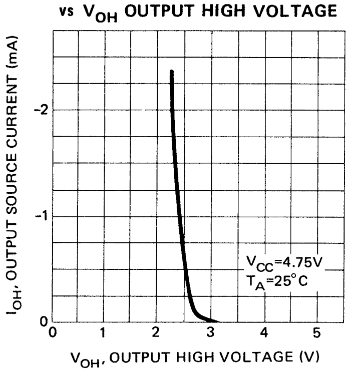


Fig. 7 – V_{OUT} OUTPUT VOLTAGE vs V_{IN} INPUT VOLTAGE

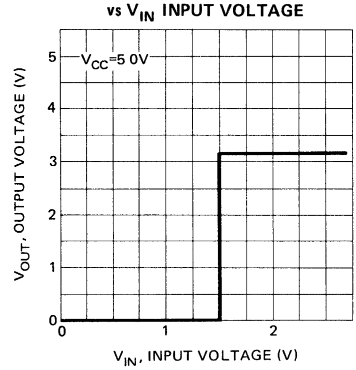


Fig. 8 – V_{ITH} INPUT THRESHOLD VOLTAGE vs AMBIENT TEMPERATURE

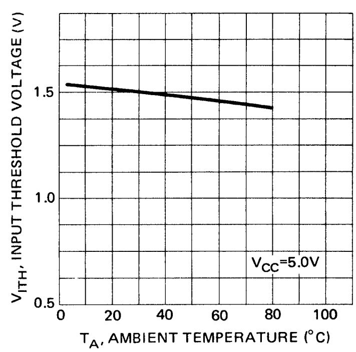


Fig. 9 – NORMALIZED ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

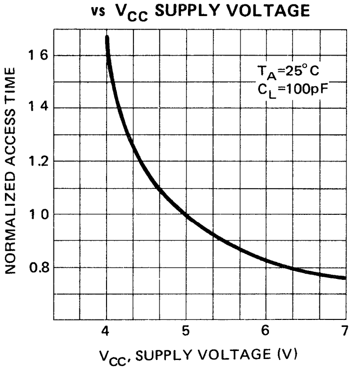


Fig. 10 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

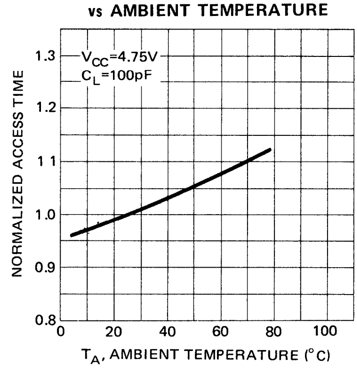
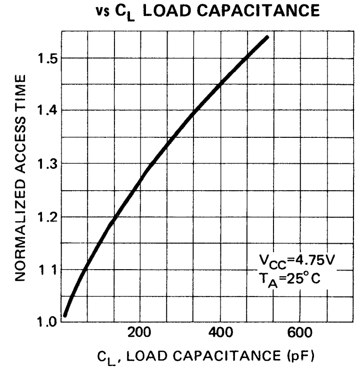


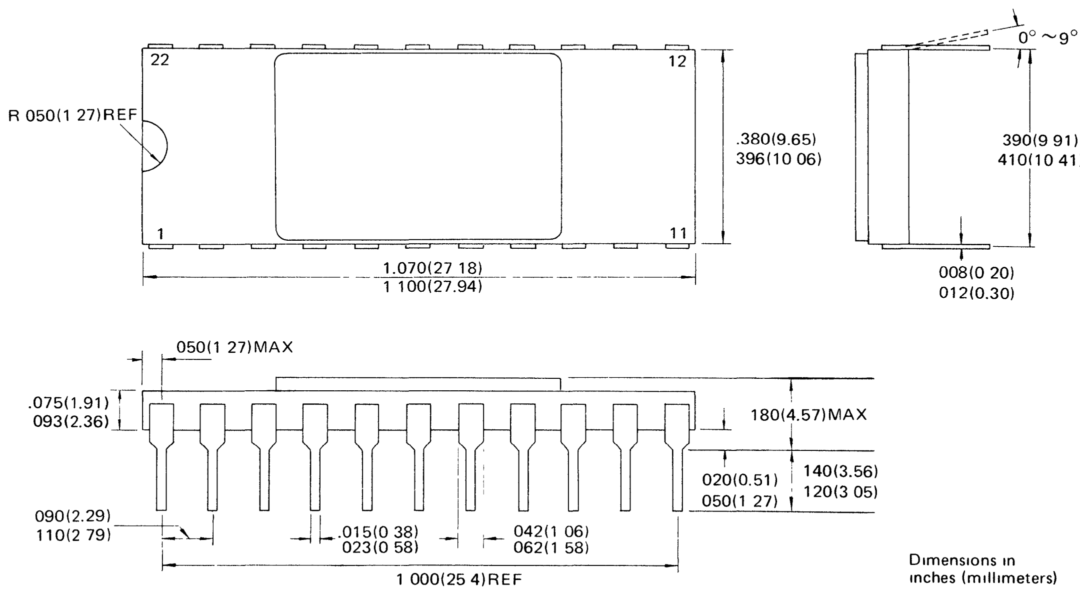
Fig. 11 – NORMALIZED ACCESS TIME vs C_L LOAD CAPACITANCE



MOS Memories

PACKAGE DIMENSIONS

22-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE DIP22-A)



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specification.

FUJITSU

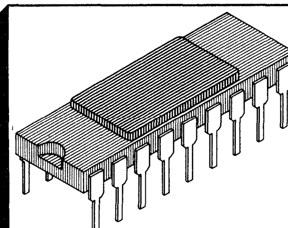
MOS 1024-BIT STATIC RANDOM ACCESS MEMORY

MB 8111N/E

1024-BIT STATIC RANDOM ACCESS MEMORY WITH COMMON I/O AND OUTPUT DISABLE

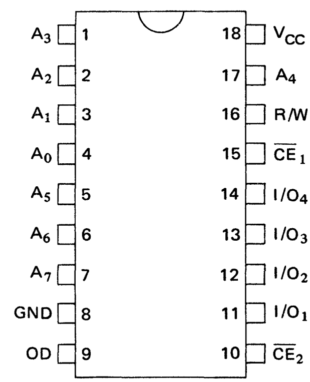
The Fujitsu MB 8111 is a 256 word by 4 bit static random access memory fabricated using N-channel silicon gate MOS technology. Common input/output pins are provided. All devices are fully compatible with TTL logic families in all respects: inputs, outputs, and the use of a single +5V DC supply. For ease of use, separate chip enables ($\overline{CE}$) permit the selection of an individual package when outputs are OR-tied. All devices offer the advantages of low power dissipation, low cost, and high performance.

- Fast access time:
  250 ns max. (MB 8111E)
  450 ns max. (MB 8111N)
- Single +5V DC supply voltage
- Common data input and output
- TTL compatible inputs and outputs
- Three-state output with OR-tie capability
- Two chip enable leads for simpified memory expansion
- Standard 18-pin DIP package
- Pin compatible with the 2111
- 256 words x 4 bits organization
- Static operation: no clocks or refresh required



CASE DIP18-D
CERAMIC PACKAGE

PIN ASSIGNMENT



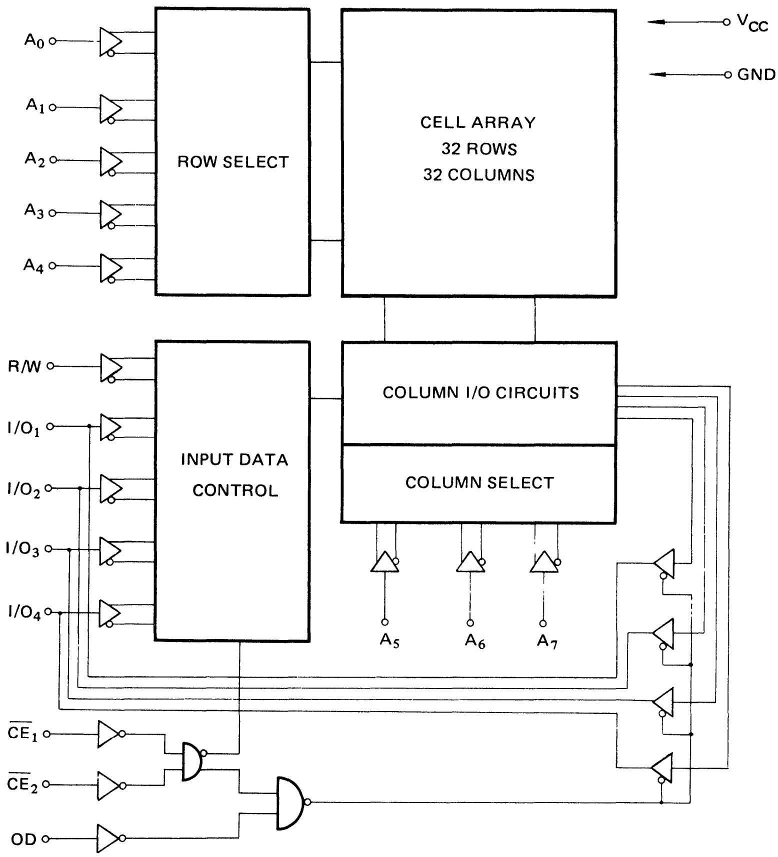
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
Input Voltage	V_{IN}	-0.5 to +7	V
Output Voltage	V_{OUT}	-0.5 to +7	V
Storage Temperature	T_{stg}	-65 to +150	°C
Power Dissipation	P_D	1.0	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB 8111 BLOCK DIAGRAM



CAPACITANCE (T_A=25°C; f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	4	8	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	10	15	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C to +70°C
Input Low Voltage	V_{IL}	-0.5		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	

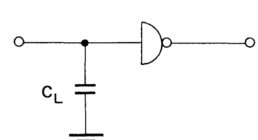
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN}=0V to 5.25V)	I_{IL}		10	μA
I/O Leakage Current ($\overline{CE}_1$=$\overline{CE}_2$=2.2V, $V_{I/O}$=4.0V)	I_{OL1}		10	μA
I/O Leakage Current ($\overline{CE}_1$=$\overline{CE}_2$=2.2V, $V_{I/O}$=0.45V)	I_{OL2}		-25	μA
Power Supply Current (V_{IN}=5.25V, $I_{I/O}$=0mA, T_A=0°C)	I_{CC}		70	mA
Output Low Voltage (I_{OL}=2mA)	V_{OL}		0.45	V
Output High Voltage (I_{OH}=-150μA)	V_{OH}	2.2		V

Fig. 2 – DYNAMIC TEST CONDITIONS

Input Pulse Levels: 0.65V to 2.2V
Input Pulse Rise and Fall Time: 10ns
Timing Measurement Reference Levels: Input: 1.5V; Output: 0.8V to 2.0V
Output Load: 1 TTL Gate and C_L=100pF



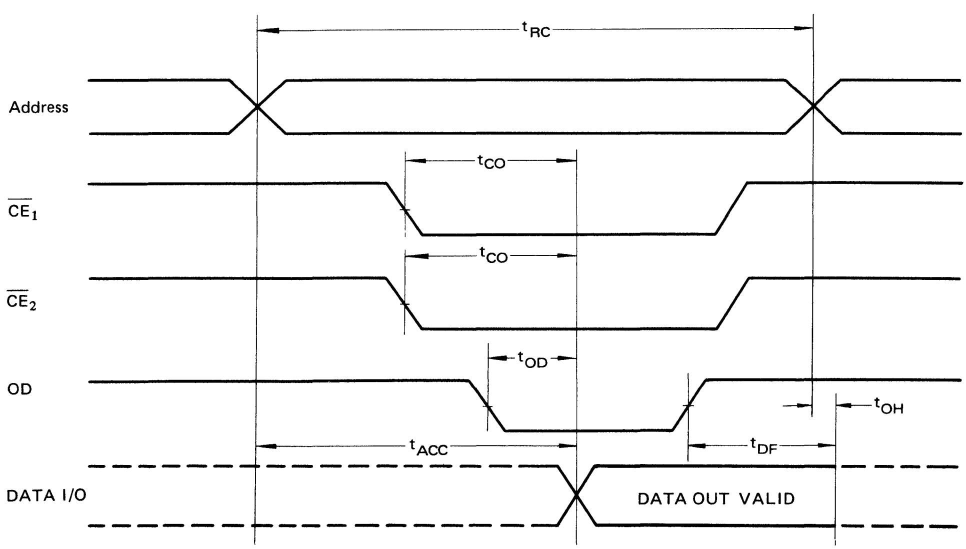
DYNAMIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB 8111N			MB 8111E			Unit
		Min	Typ	Max	Min	Typ	Max	
Read Cycle	t_{RC}	450			250			ns
Address Access time	t_{ACC}			450			250	ns
Chip Enable to Output	t_{CO}			350			180	ns
Output Disable to Output	t_{OD}			300			130	ns
Data Output to High Impedance	t_{DF}	0		150	0		150	ns
Previous Read Data Valid after Change of Address	t_{OH}	40			40			ns

READ CYCLE TIMING DIAGRAM

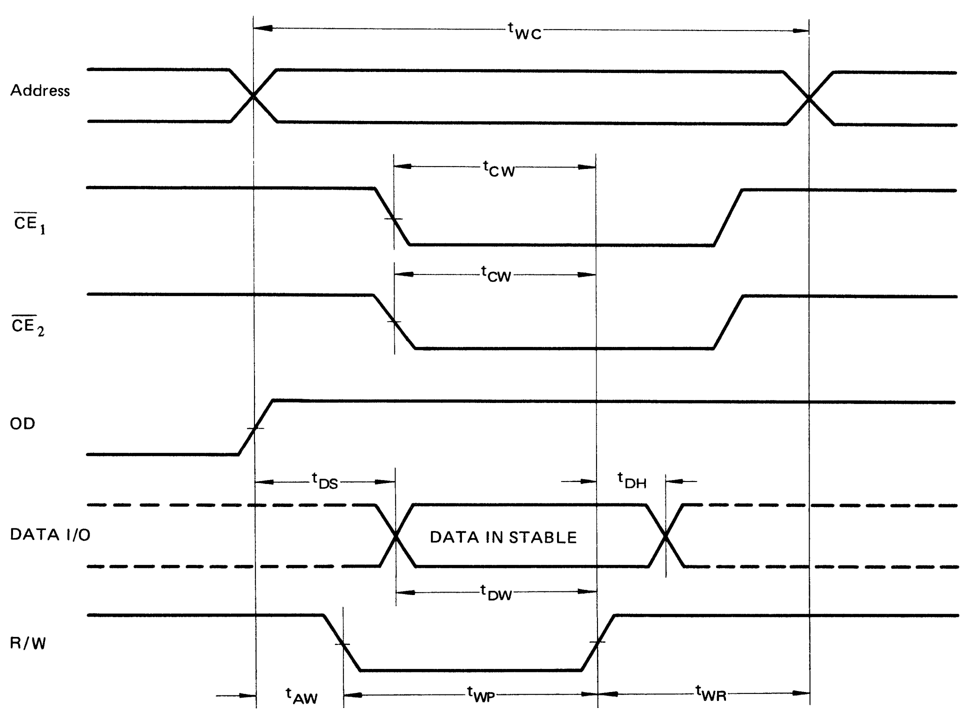


Note: 1) t_{DF} is measured with respect to the trailing edge of $\overline{CE}_1$, $\overline{CE}_2$, or OD, whichever occurs first.

WRITE CYCLE

Parameter	Symbol	MB 8111N			MB 8111E			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Cycle	t_{WC}	450			170			ns
Address to Write Setup	t_{AW}	100			20			ns
Chip Enable to Write	t_{CW}	350			100			ns
Data Setup Time	t_{DW}	200			100			ns
Data Hold Time	t_{DH}	100			0			ns
Write Pulse Width	t_{WP}	250			150			ns
Write Recovery Time	t_{WR}	50			0			ns
Output Disable Setup	t_{DS}	150			70			ns

WRITE CYCLE TIMING DIAGRAM



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – I_{CC} SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

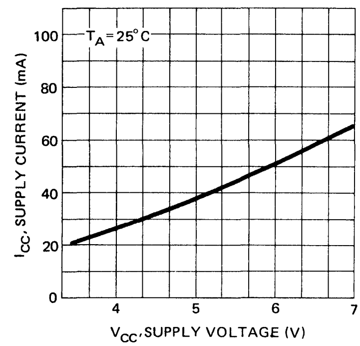


Fig. 4 – I_{CC} SUPPLY CURRENT vs AMBIENT TEMPERATURE

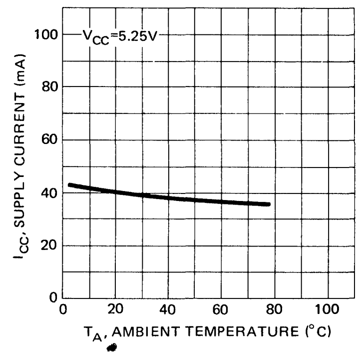


Fig. 5 – I_{OL} OUTPUT SINK CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

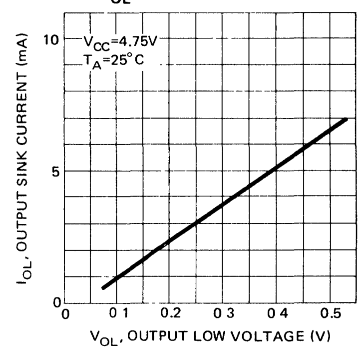


Fig. 6 – I_{OH} OUTPUT SOURCE CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

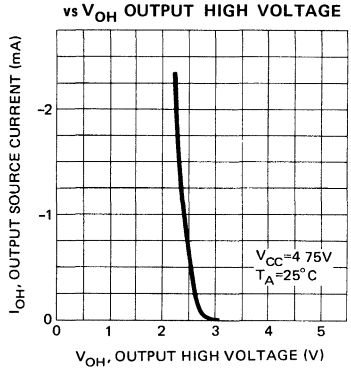


Fig. 7 – V_{OUT} OUTPUT VOLTAGE vs V_{IN} INPUT VOLTAGE

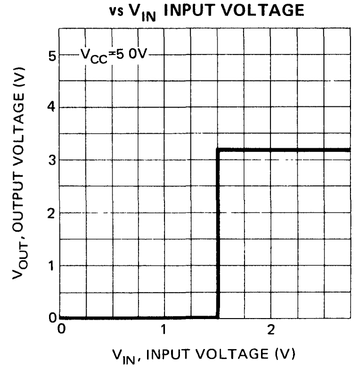


Fig. 8 – V_{ITH} INPUT THRESHOLD VOLTAGE vs AMBIENT TEMPERATURE

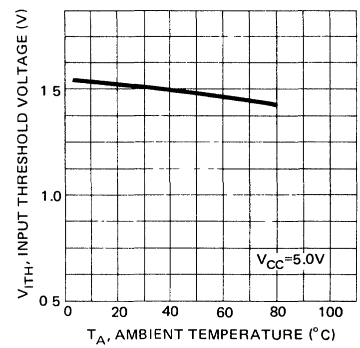


Fig. 9 – NORMALIZED ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

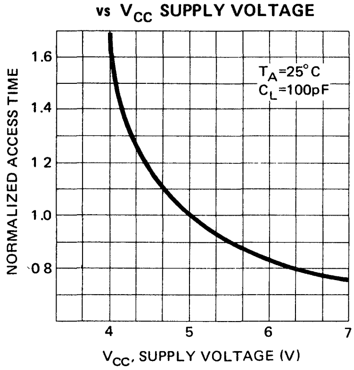


Fig. 10 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

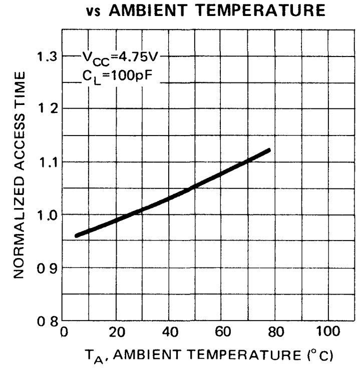
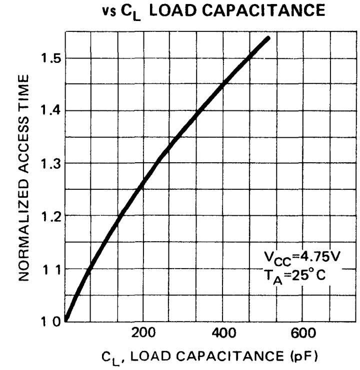
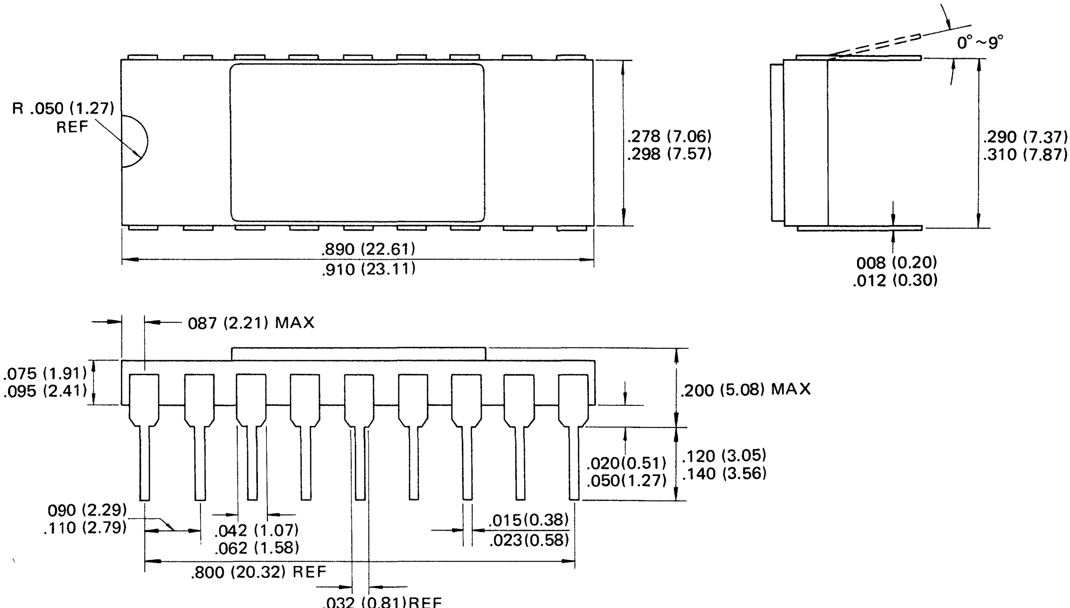


Fig. 11 – NORMALIZED ACCESS TIME vs C_L LOAD CAPACITANCE



PACKAGE DIMENSIONS

18-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE DIP 18-D)



Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specification.

MOS 1024-BIT STATIC RANDOM ACCESS MEMORY

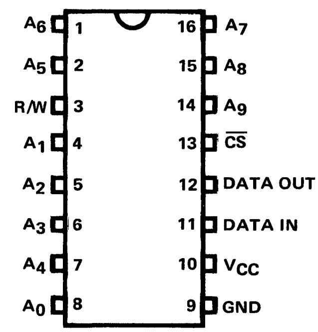
MB 8102

FUJITSU

1024 BIT STATIC MOS RANDOM ACCESS MEMORY

- 1024 words by 1 bit static MOS RAM
- No clocks or refreshing required
- Fast access time – 450 ns
- Single +5V supply voltage
- TTL compatible input and output
- Three-state output – OR-tie capability
- Simple memory expansion – chip select input
- Low power dissipation – typically 150 mW
- Full on-chip address decode
- All inputs have protection against static charge
- N-channel silicon gate MOS technology

PIN ASSIGNMENT

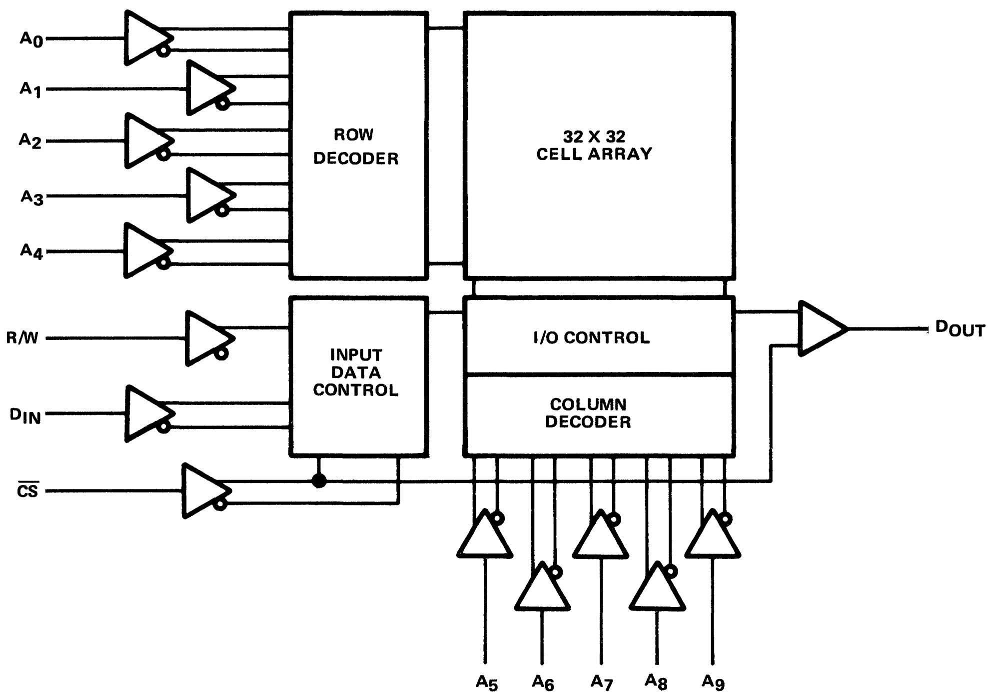


ABSOLUTE MAXIMUM RATINGS (See Note)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to + 7	V
Input Voltage	V_{IN}	-0.5 to +7	V
Output Voltage	V_{OUT}	-0.5 to +7	V
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C

Note: Stress above those listed in ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIG. 1—BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

(1) D.C.
$T_A = 0°C$ to $+70°C$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	-0.5		0.65	V
Input High Voltage	V_{IH}	2.2		V_{CC}	V

(2) A.C.
$T_A = 0°C$ to $+70°C$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Read Cycle	t_{RC}	450			ns
Write Cycle	t_{WC}	450			ns
Address to Write Setup	t_{AW}	150			ns
Write Pulse Width	t_{WP}	200			ns
Write Recovery Time	t_{WR}	50			ns
Data Setup Time	t_{DW}	200			ns
Data Hold Time	t_{DH}	50			ns
Chip Select to Write Setup	t_{CW}	200			ns
Chip Select Hold Time	t_{CH}	0			ns

ELECTRICAL CHARACTERISTICS

(1) D.C.
$T_A = 0°C$ to $+70°C$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Load Current	I_{LI}	$V_{IN} = 0$ to 5.25V			10	μA
Output Leakage Current	I_{LOH}	$\overline{CS} = 2.2V$ $V_{OUT} = 2.4V$ to V_{CC}			10	μA
Output Leakage Current	I_{LOL}	$\overline{CS} = 2.2V$ $V_{OUT} = 0.4V$			-25	μA
Power Supply Current	I_{CC1}	All Input = V_{CC} $T_A = 25°C$ D_{OUT} Open		30	60	mA
Power Supply Current	I_{CC2}	All Input = V_{CC} $T_A = 0°C$ D_{OUT} Open			70	mA
Output Low Voltage	V_{OL}	$I_{OL} = 3.2$ mA			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -100$ μA	2.2			V

(2) A.C.*
$T_A = 0^\circ C$ to $+70^\circ C$

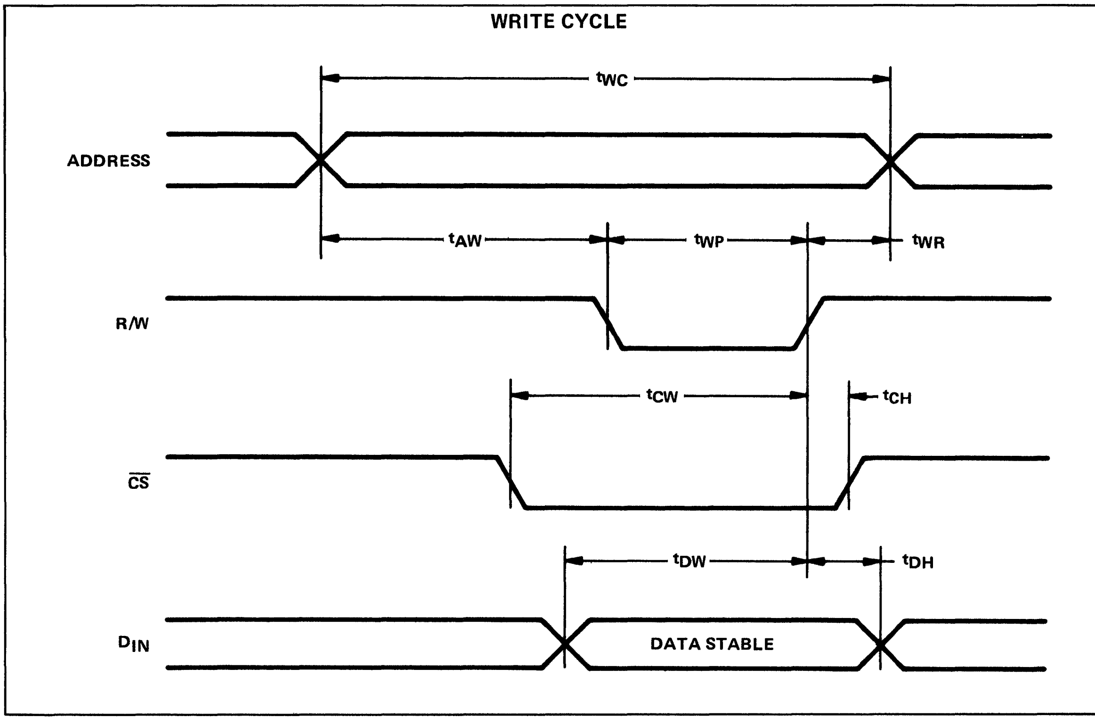
Parameter	Symbol	Min.	Typ.	Max.	Unit
Address Access Time	t_{ACC}			450	ns
Chip Select Access Time	t_{CO}			200	ns
Previous Read Data Valid with Respect to Address Change	t_{OH1}	50			ns
Previous Read Data Valid with Respect to Chip Select	t_{OH2}	0			ns

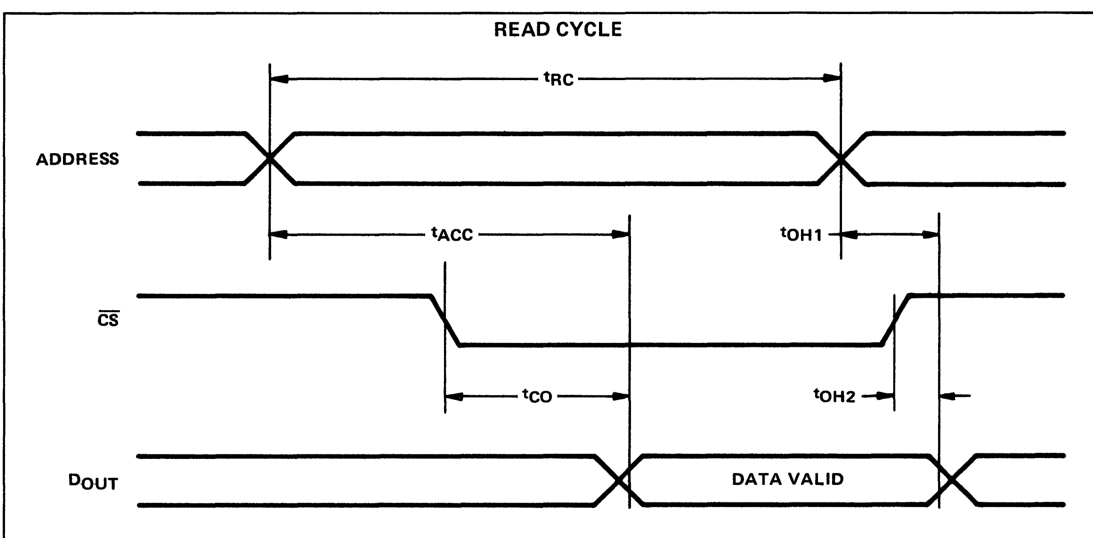
*Input Pulse Levels: 0.8V to 2.0V
Input Rise and Fall Times: 10 ns
Timing Measurement Input: 1.5V
Reference Levels Output: 0.8V and 2.0V
Output Load: 1 TTL Gate and C_L = 100 pF

(3) CAPACITANCE
(Periodically Sampled), $T_A = 25^\circ C$, f = 1 MHz

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance (Address, $\overline{CS}$, D_{IN})	C_{IN1}	V_{IN} = 0V			5	pF
Input Capacitance (R/W)	C_{IN2}	V_{IN} = 0V			7	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V			10	pF

TIMING DIAGRAM





TYPICAL CHARACTERISTICS CURVES

FIG. 2 — SUPPLY CURRENT VS. AMBIENT TEMPERATURE

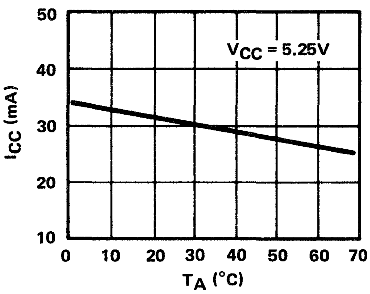


FIG. 3 — SUPPLY CURRENT VS. SUPPLY VOLTAGE

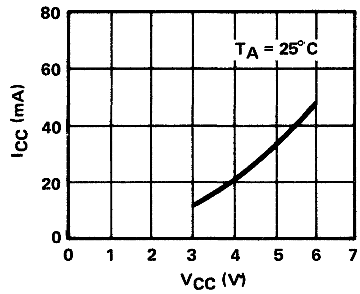


FIG. 4 — OUTPUT CURRENT VS. OUTPUT VOLTAGE (NON SELECT)

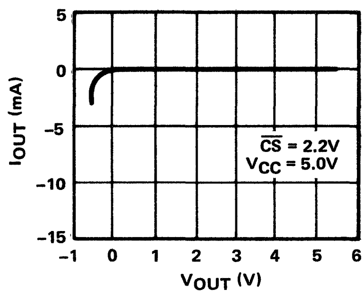


FIG. 5 — INPUT VOLTAGE VS. OUTPUT VOLTAGE

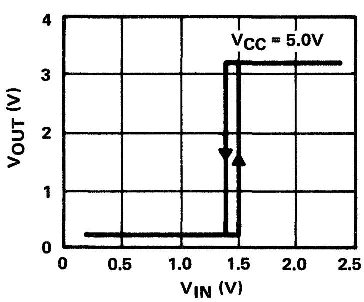


FIG. 6 — OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

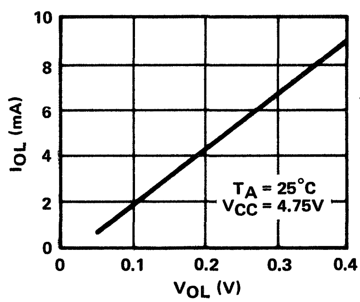


FIG. 7 — ACCESS TIME VS. LOAD CAPACITANCE

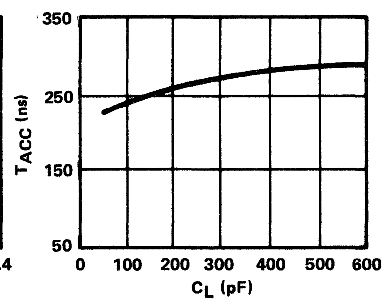


FIG. 8 — OUTPUT VOLTAGE VS. OUTPUT SOURCE CURRENT

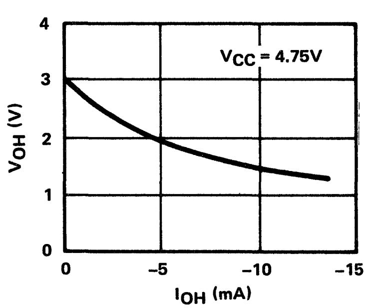


FIG. 9 — INPUT CURRENT VS. INPUT VOLTAGE

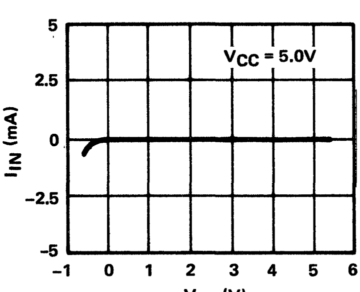
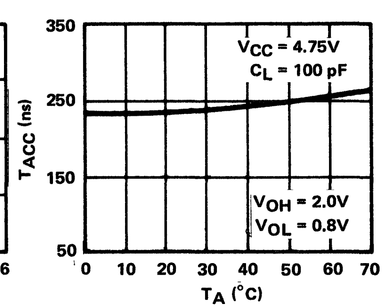
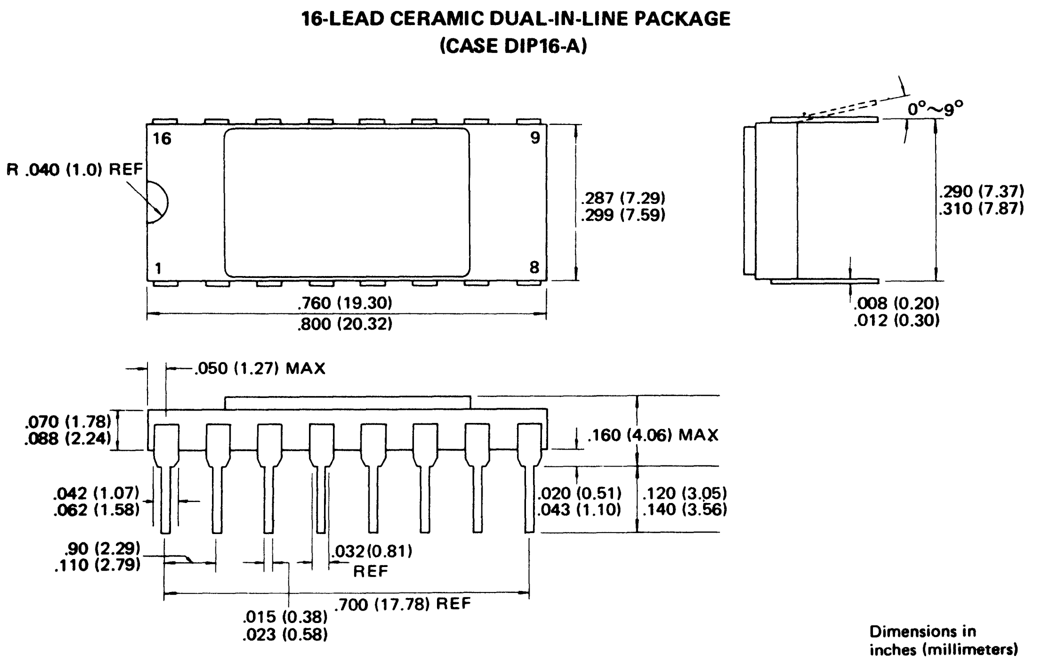


FIG. 10 — ACCESS TIME VS. AMBIENT TEMPERATURE



PACKAGE DIMENSIONS



MOS 1024-BIT STATIC RANDOM ACCESS MEMORY

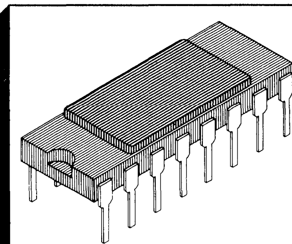
FUJITSU

MB 8112N/E

1024-BIT STATIC RANDOM ACCESS MEMORY WITH COMMON DATA I/O

The Fujitsu MB 8112 is a 256 word by 4-bit static random access memory fabricated using N-channel silicon gate MOS technology. Common input/output pins are provided. All devices are fully compatible with TTL logic families in all respects: inputs, outputs, and the use of a single +5V DC supply. For ease of use, chip enable ($\overline{CE}$) permits the selection of an individual package when outputs are OR-tied. All devices offer the advantages of low power dissipation, low cost, and high performance.

- Fast access time:
  250 ns max. (MB 8112E)
  450 ns max. (MB 8112N)
- Single +5V DC supply voltage
- Common data input and output
- TTL compatible inputs and outputs
- Three-state output with OR-tie capability
- Chip enable ($\overline{CE}$) lead for simplified memory expansion
- Standard 16-pin DIP package
- Pin compatible with the 2112
- 256 words x 4-bits organization
- Static operation: no clocks or refresh required



CASE DIP16-A
CERAMIC PACKAGE

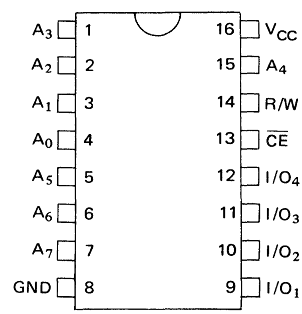
MOS Memories

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
Input Voltage	V_{IN}	-0.5 to +7	V
Output Voltage	V_{OUT}	-0.5 to +7	V
Storage Temperature	T_{stg}	-65 to +150	°C
Power Dissipation	P_D	1.0	W

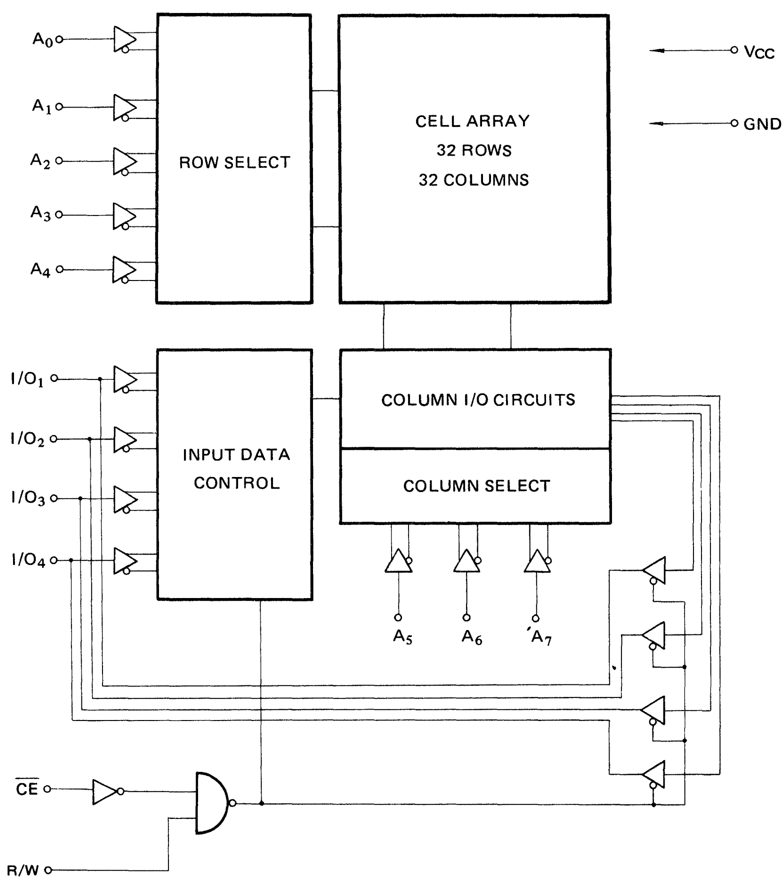
Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 8112 BLOCK DIAGRAM



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN}=0V)	C_{IN}	4	8	pF
I/O Capacitance ($V_{I/O}$=0V)	$C_{I/O}$	10	15	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Input Low Voltage	V_{IL}	-0.5		0.65	V	0°C to +70°C
Input High Voltage	V_{IH}	2.2		V_{CC}	V	

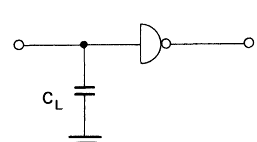
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = 0V to 5.25V)	I_{IL}		10	µA
I/O Leakage Current ($\overline{CE}$=2.2V, $V_{I/O}$ =4.0V)	I_{OL1}		10	µA
I/O Leakage Current ($\overline{CE}$=2.2V, $V_{I/O}$ =0.45V)	I_{OL2}		-25	µA
Power Supply Current (V_{IN} = 5.25V, $I_{I/O}$=0mA, T_A = 0°C)	I_{CC}		70	mA
Output Low Voltage (I_{OL} = 2mA)	V_{OL}		0.45	V
Output High Voltage (I_{OH}=-150µA)	V_{OH}	2.2		V

Fig. 2 — DYNAMIC TEST CONDITIONS

Input Pulse Lavels:	0.65V to 2.2V
Input Pulse Rise and Fall Time:	10ns
Timing Measurement Reference Levels	Input: 1.5V Output: 0.8V and 2.0V
Output Load:	1 TTL Gate and C_L =100pF



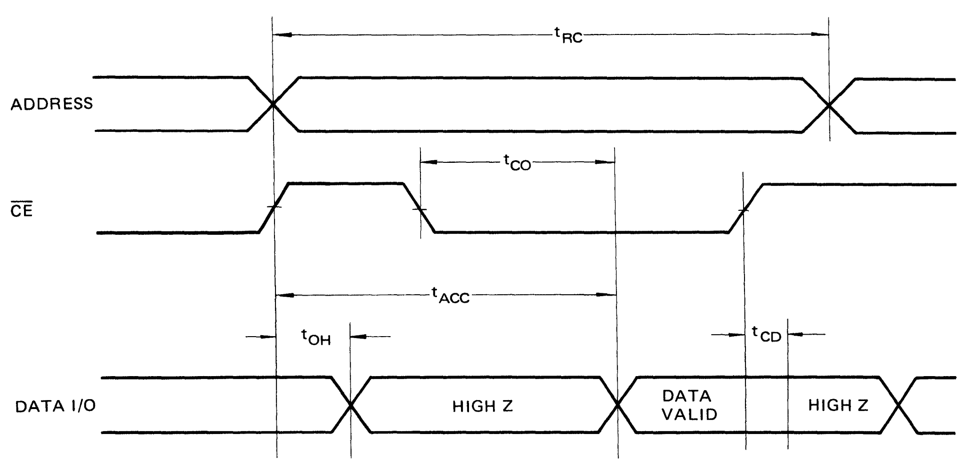
DYNAMIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB 8112N			MB 8112E			Unit
		Min	Typ	Max	Min	Typ	Max	
Read Cycle	t_{RC}	450			250			ns
Address Access Time	t_{ACC}			450			250	ns
Chip Enable to Output	t_{CO}			350			180	ns
Chip Enable to Output Disable Time	t_{CD}	0		150	0		120	ns
Previous Read Data Valid after Change of Address	t_{OH}	40			40			ns

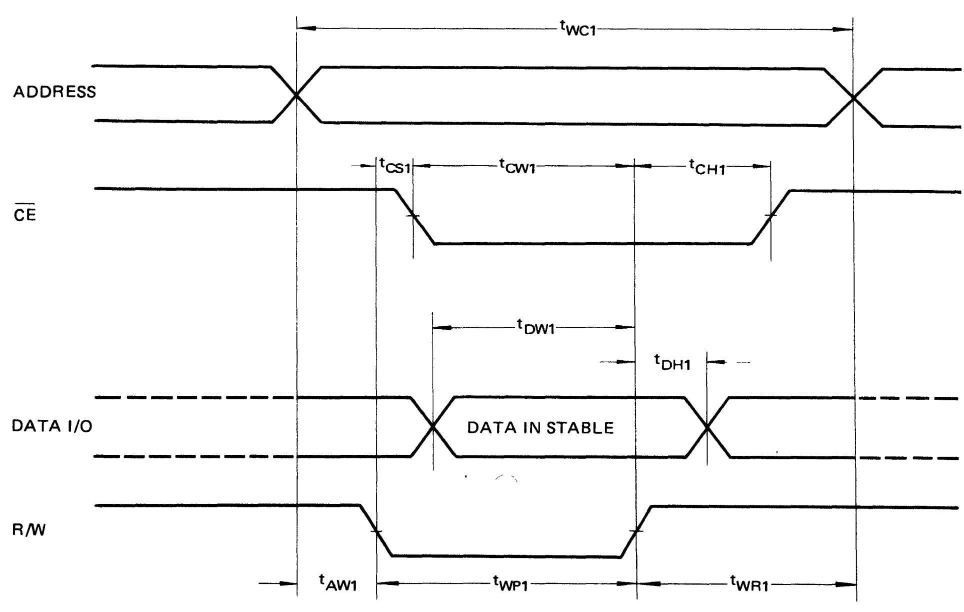
READ CYCLE TIMING DIAGRAM



WRITE CYCLE #1

Parameter	Symbol	MB 8112N			MB 8112E			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Cycle	t_{WC1}	450			200			ns
Address to Write Setup	t_{AW1}	100			20			ns
Data Setup Time	t_{DW1}	200			180			ns
Write Pulse Width	t_{WP1}	250			180			ns
Chip Enable Setup Time	t_{CS1}	0			0			ns
Chip Enable Hold Time	t_{CH1}	0			0			ns
Write Recovery Time	t_{WR1}	50			0			ns
Data Hold Time	t_{DH1}	50			0			ns
Chip Enable to Write Setup Time	t_{CW1}	250			180			ns

WRITE CYCLE #1 TIMING DIAGRAM

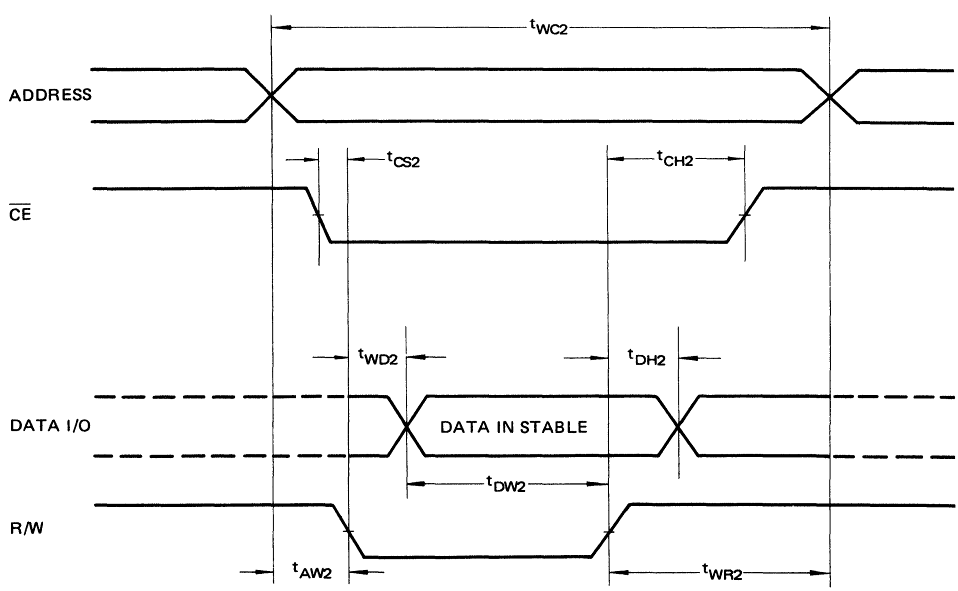


MOS Memories

WRITE CYCLE #2

Parameter	Symbol	MB 8112N			MB 8112E			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Cycle	t_{WC2}	500			250			ns
Address to Write Setup	t_{AW2}	100			20			ns
Data Setup Time	t_{DW2}	200			110			ns
Write to Output Disable Time	t_{WD2}	150			120			ns
Data Hold Time	t_{DH2}	50			0			ns
Write Recovery Time	t_{WR2}	50			0			ns
Chip Enable Setup Time	t_{CS2}	0			0			ns
Chip Enable Hold Time	t_{CH2}	0			0			ns

WRITE CYCLE #2 TIMING DIAGRAM



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – I_{CC} SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

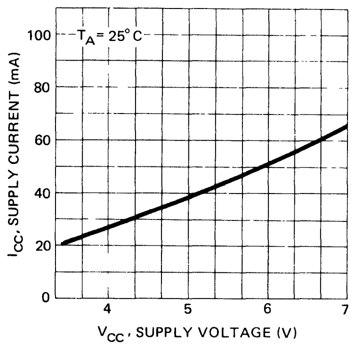


Fig. 4 – I_{CC} SUPPLY CURRENT vs AMBIENT TEMPERATURE

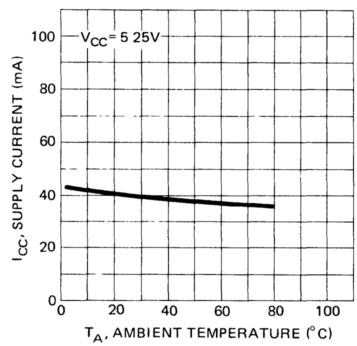


Fig. 5 – I_{OL} OUTPUT SINK CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

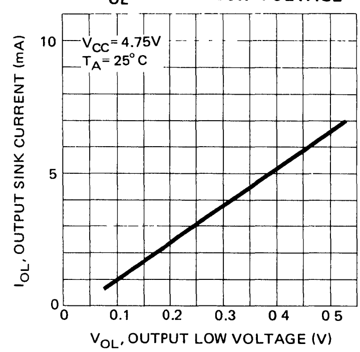


Fig. 6 – I_{OH} OUTPUT SOURCE CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

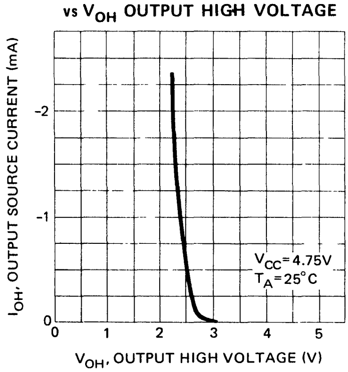


Fig. 7 – V_{OUT} OUTPUT VOLTAGE vs V_{IN} INPUT VOLTAGE

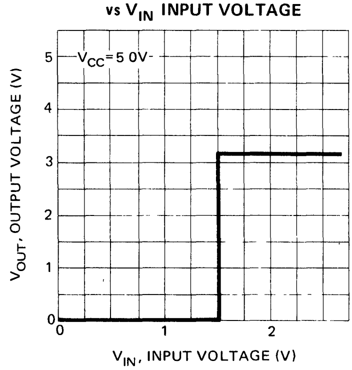


Fig. 8 – V_{ITH} INPUT THRESHOLD VOLTAGE vs AMBIENT TEMPERATURE

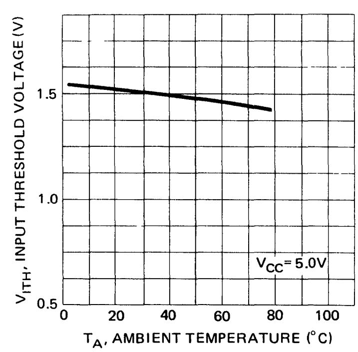


Fig. 9 – NORMALIZED ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

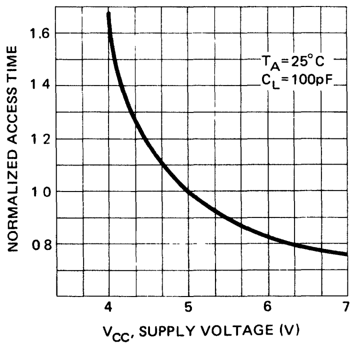


Fig. 10 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

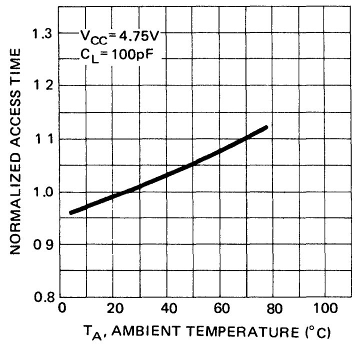
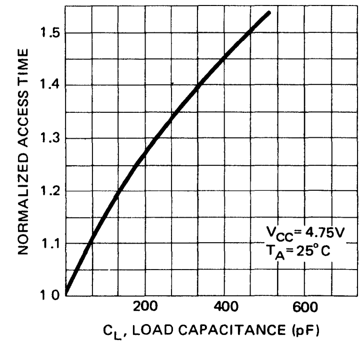
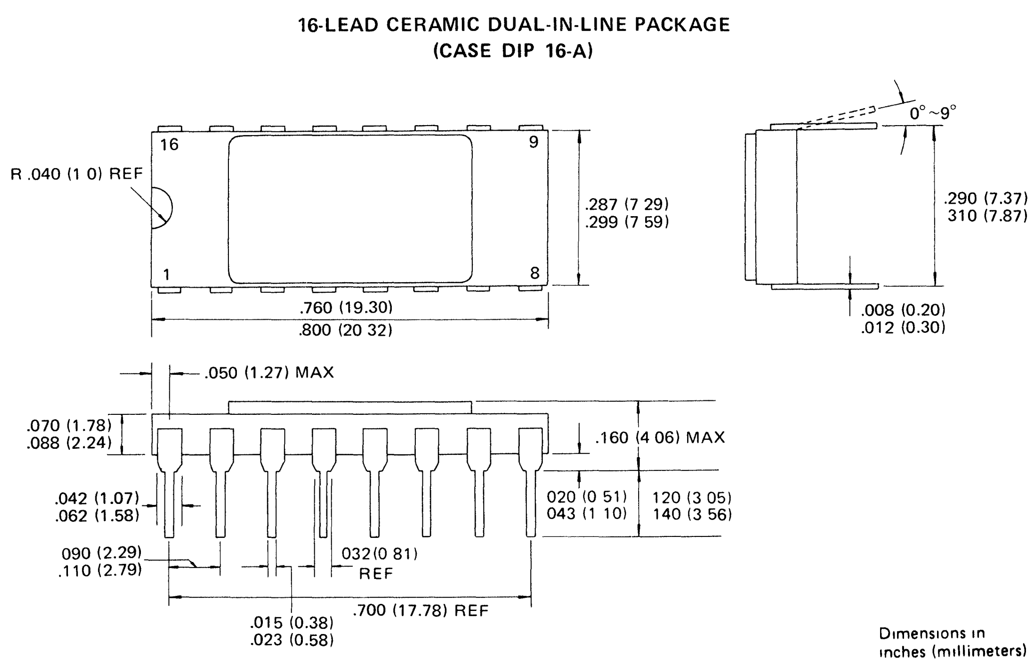


Fig. 11 – NORMALIZED ACCESS TIME vs C_L LOAD CAPACITANCE



PACKAGE DIMENSIONS



FUJITSU

MOS 1024-BIT STATIC RANDOM ACCESS MEMORY

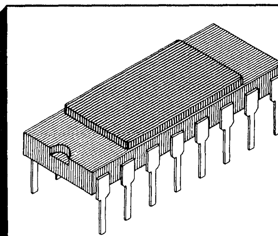
MBM 2115N/E/H/Y
MBM 2125N/E/H/Y

MOS Memories

1024-BIT HIGH-SPEED STATIC RANDOM ACCESS MEMORY

The Fujitsu MBM 2115/25 is a series of fully decoded 1024-bit static random access memories, each with 1024-word by 1-bit organization. All devices are fully compatible with TTL logic families, featuring suitable output, inputs, and the use of a single +5 VDC power supply. MBM 2115/25 devices are fabricated with N-channel silicon gate MOS technology. With this process, design and production of high-speed MOS RAMs with performance comparable with bipolar RAMs is ensured. And all devices offer the advantages of low power dissipation and reduced cost. All devices are capable of driving bus-organized systems.

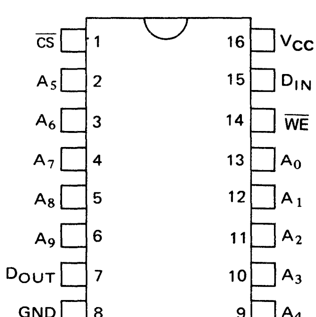
- 1024 words x 1 bit organization
- Fast access time:
  70 ns max.(MBM 2115H/25H)
  90 ns max.(MBM 2115E/25E)
  120 ns max.(MBM 2115N/25N)
- 35 ns (max.) chip select time
- TTL outputs and inputs:
  Open drain output (MBM 2115)
  Three-state output
  (MBM 2125)
- Single +5 VDC supply voltage
- Low power dissipation
- All inputs protected against static charge
- $\overline{CS}$ ($\overline{\text{Chip Select}}$) lead for simplified memory expansion



CASE DIP16-A
CERAMIC PACKAGE

- Fully decoded
- Standard 16-pin DIP package
- Pin compatible with the 93415/25 and interchangeable with the 2115/25

PIN ASSIGNMENT



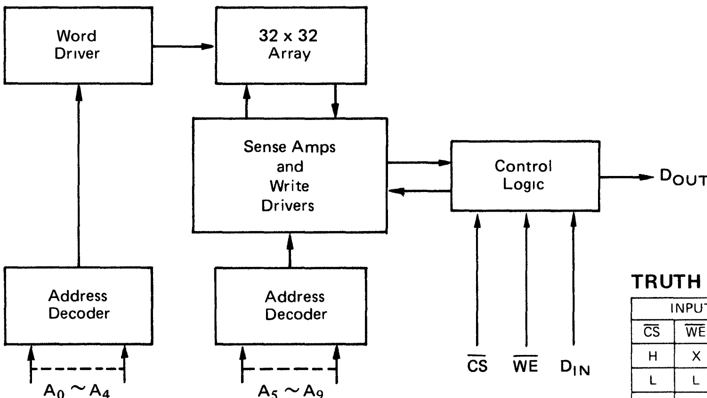
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	VDC
Input Voltage	V_{IN}	-0.5 to +5.5	VDC
Output Voltage	V_{OUT}	-0.5 to +7	VDC
DC Output Current	I_{OUT}	20	mA
Temperature Under Bias	T_A	-10 to +85	°C
Storage Temperature	T_{stg}	-65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MBM 2115/25 BLOCK DIAGRAM



TRUTH TABLE

INPUTS			MBM 2115 Output	MBM 2125 Output	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}			
H	X	X	H	HIGH Z	NOT SELECTED
L	L	L	H	HIGH Z	WRITE "0"
L	L	H	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

DC AND OPERATING CHARACTERISTICS

($T_A = 0°C \sim 75°C$, V_{CC} = +5V ±5%, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
MBM 2115 Output Low Voltage (I_{OL} = 12mA)		V_{OL1}	—	0.3	0.45	V
MBM 2125 Output Low Voltage (I_{OL} = 7mA)		V_{OL2}	—	0.3	0.45	V
MBM 2125 Output High Voltage (I_{OH} = −3.2mA)		V_{OH}	2.4	—	—	V
Input Low Voltage		V_{IL}	—	—	0.8	V
Input High Voltage		V_{IH}	2.1	—	—	V
MBM 2115 Output Leakage Current (V_{OUT} = 4.5V)		I_{OL1}	—	—	50	μA
MBM 2125 Output Current (High Z) (V_{OUT} = 0.5/2.4V)		I_{OL2}	—	—	50	μA
Input Leakage Current (V_{IN} = 0.4/4.5V)		I_{IL}	—	—	10	μA
Power Supply Current (V_{CC} = max.; all inputs = 0V)	MBM 2115N/25N	I_{CC}	—	—	65	mA
	MBM 2115E/25E	I_{CC}	—	—	65	mA
	MBM 2115H/25H	I_{CC}	—	—	100	mA

CAPACITANCE

(f = 1 MHz; V_{CC} = +5V; T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Lead Capacitance	C_I	—	4	5	pF
Output Lead Capacitance	C_O	—	7	8	pF

AC CHARACTERISTICS

(T_A = 0°C ~ 75°C, V_{CC} = +5V ± 5%, unless otherwise noted.)

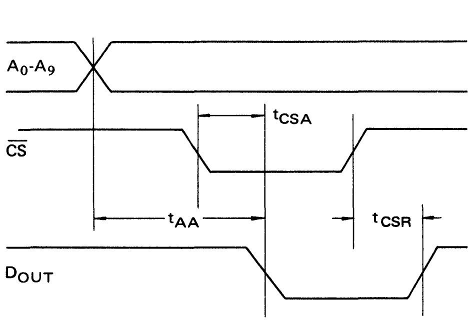
READ CYCLE (MBM 2115N/E/H)

Parameter	Symbol	MBM 2115N			MBM 2115E			MBM 2115H			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	—	90	120	—	65	95	—	55	70	ns
Chip Select Time	t_{CSA}	5	—	35	5	—	35	5	—	35	ns
Chip Select Recovery Time	t_{CSR}	—	—	40	—	—	40	—	—	40	ns

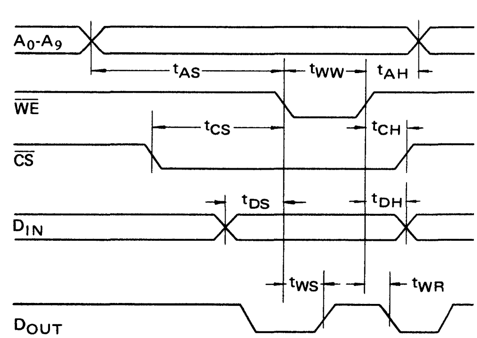
WRITE CYCLE (MBM 2115N/E/H)

Parameter	Symbol	MBM 2115N			MBM 2115E			MBM 2115H			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Write Disable Time	t_{WS}	—	—	40	—	—	40	—	—	40	ns
Write Recovery Time	t_{WR}	5	—	50	5	—	50	5	—	45	ns
Write Pulse Width	t_{WW}	60	—	—	60	—	—	50	—	—	ns
Data Set Up Time Prior to Write	t_{DS}	15	—	—	15	—	—	5	—	—	ns
Data Hold Time After Write	t_{DH}	15	—	—	15	—	—	5	—	—	ns
Address Set Up Time	t_{AS}	20	—	—	20	—	—	15	—	—	ns
Address Hold Time	t_{AH}	15	—	—	15	—	—	5	—	—	ns
Chip Select Set Up Time	t_{CS}	15	—	—	15	—	—	5	—	—	ns
Chip Select Hold Time	t_{CH}	15	—	—	15	—	—	5	—	—	ns

READ CYCLE TIMING DIAGRAM



WRITE CYCLE TIMING DIAGRAM



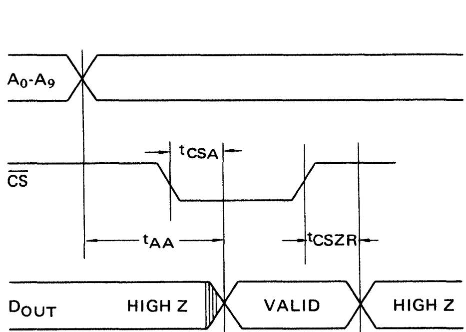
READ CYCLE (MBM 2125N/E/H)

Parameter	Symbol	MBM 2125N			MBM 2125E			MBM 2125H			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	—	90	120	—	65	95	—	55	70	ns
Chip Select Time	t_{CSA}	5	—	35	5	—	35	5	—	35	ns
Chip Select to High Z	t_{CSZR}	—	—	40	—	—	40	—	—	40	ns

WRITE CYCLE (MBM 2125N/E/H)

Parameter	Symbol	MBM 2125N			MBM 2125E			MBM 2125H			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Write Disable to High Z	t_{WSZ}	—	—	40	—	—	40	—	—	40	ns
Write Recovery Time	t_{WR}	5	—	50	5	—	50	5	—	45	ns
Write Pulse Width	t_{WW}	60	—	—	60	—	—	50	—	—	ns
Data Set Up Time Prior to Write	t_{DS}	15	—	—	15	—	—	5	—	—	ns
Data Hold Time After Write	t_{DH}	15	—	—	15	—	—	5	—	—	ns
Address Set Up Time	t_{AS}	20	—	—	20	—	—	15	—	—	ns
Address Hold Time	t_{AH}	15	—	—	15	—	—	5	—	—	ns
Chip Select Set Up Time	t_{CS}	15	—	—	15	—	—	5	—	—	ns
Chip Select Hold Time	t_{CH}	15	—	—	15	—	—	5	—	—	ns

READ CYCLE TIMING DIAGRAM



WRITE CYCLE TIMING DIAGRAM

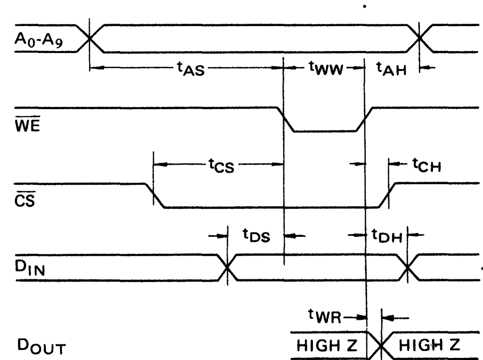


Fig. 2 — AC TEST CONDITIONS

Input Pulse Levels:	0V to 3.5V
Input Rise and Fall Time:	10 ns
Timing Measurement Reference Level:	1.5V
Output Load (MBM 2115):	$R_1 = 330\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
Output Load (MBM 2125):	$R_1 = 510\Omega$, $R_2 = 300\Omega$, $C_L = 30pF$
	(including scope and jig)

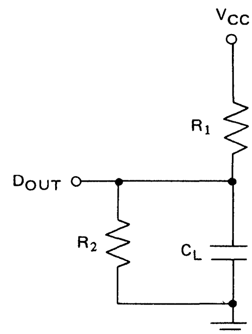
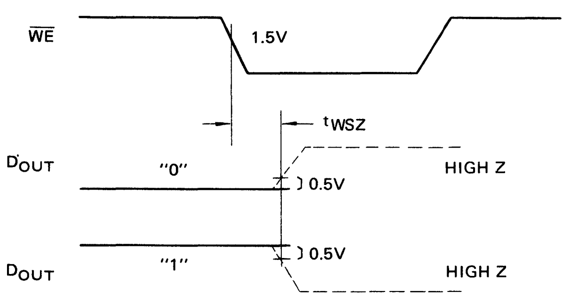
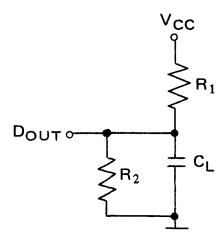


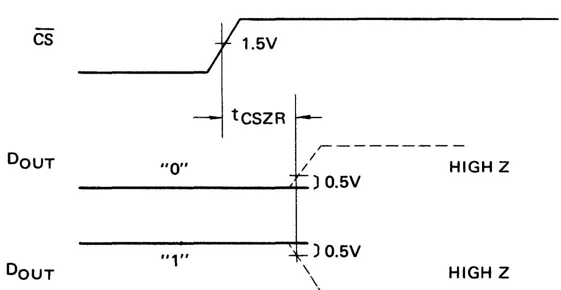
Fig. 3 — MBM 2125 WRITE ENABLE TO HIGH Z DELAY

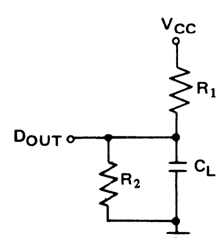




Output Load: $R_1 = 750\Omega$
$R_2 = 500\Omega$
$C_L = 5pF$

Fig. 4 — MBM 2125 PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z





Output Load: $R_1 = 750\Omega$
$R_2 = 500\Omega$
$C_L = 5pF$

TYPICAL CHARACTERISTICS CURVES

Fig. 5 – I_{CC} VS TEMPERATURE

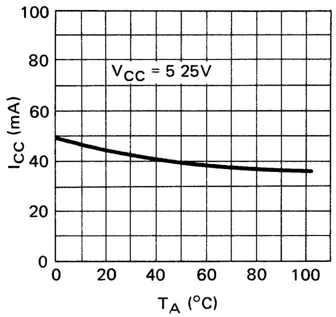


Fig. 6 – I_{CC} VS V_{CC}

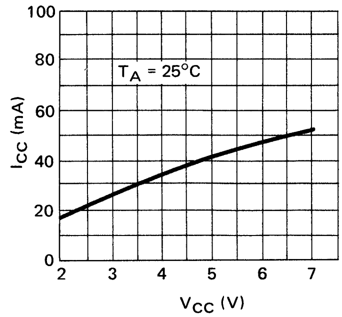


Fig. 7 – I_{OL} VS V_{OL}

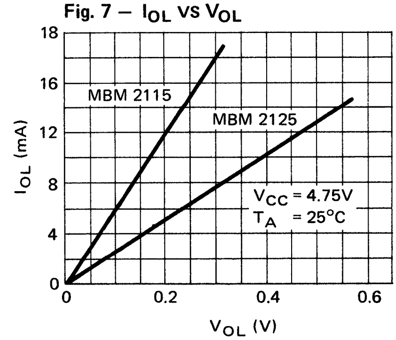


Fig. 8 – V_{ITH} VS TEMPERATURE

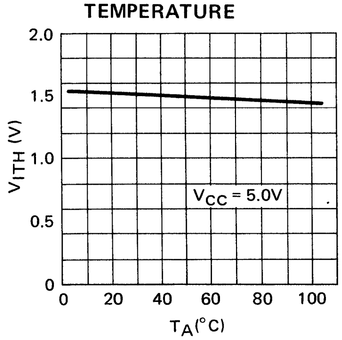


Fig. 9 – ADDRESS ACCESS TIME VS TEMPERATURE

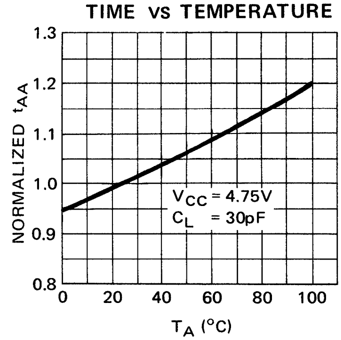


Fig. 10 – ADDRESS ACCESS TIME VS V_{CC}

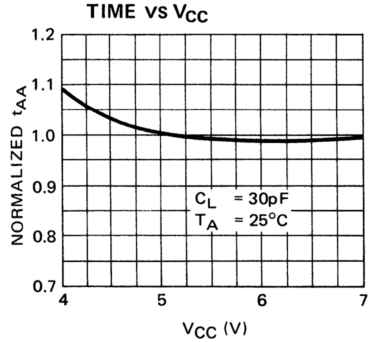


Fig. 11 – V_{OUT} VS V_{IN}

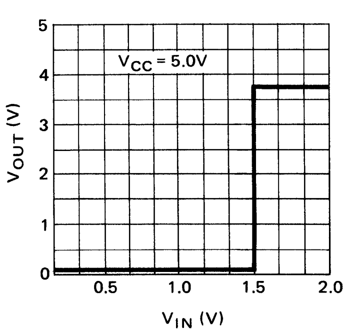


Fig. 12 – I_{OH} VS V_{OH}

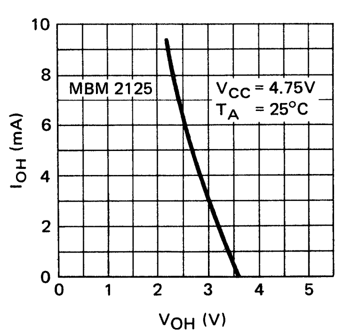
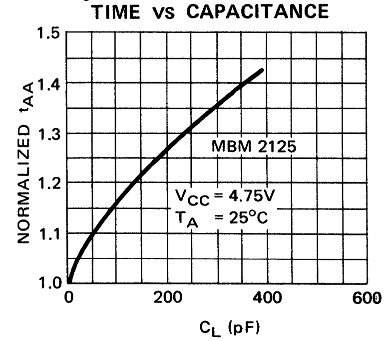
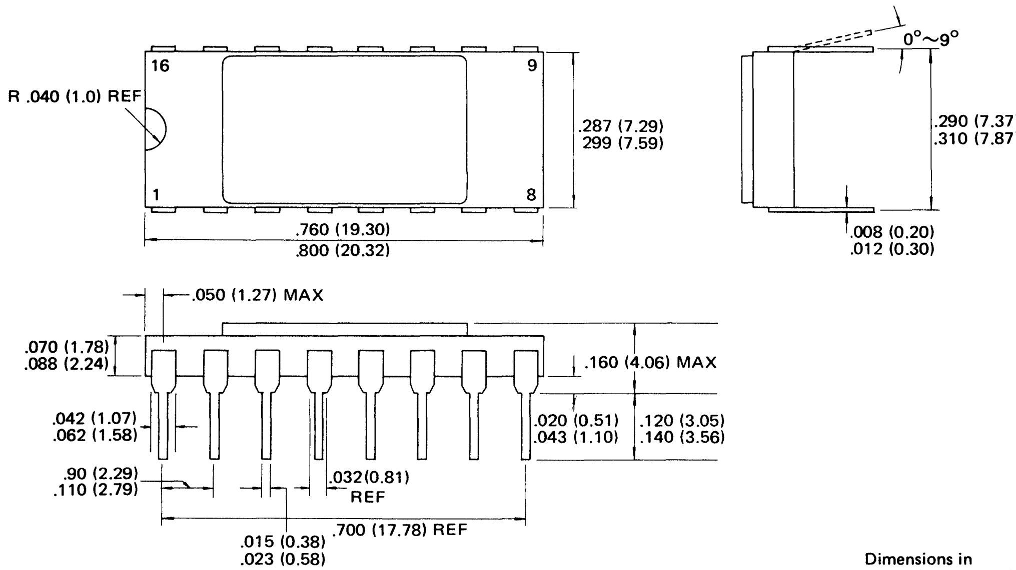


Fig. 13 – ADDRESS ACCESS TIME VS CAPACITANCE



PACKAGE DIMENSIONS

16-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE DIP16-B)



Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

HIGH SPEED 4096-BIT (1024X4) STATIC RANDOM ACCESS MEMORY

MB 8114

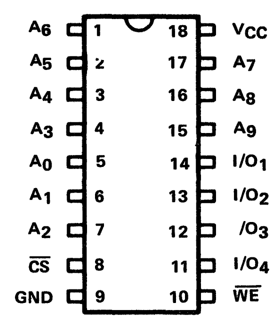
HIGH SPEED 4096-BIT (1024 X 4) STATIC RANDOM ACCESS MEMORY

The MB 8114 is a 4096-bit static random access memory organized as 1024-words by 4 bits using N-channel silicon gate MOS technology. It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.

The MB 8114 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required. The MB 8114 is compatible with TTL logic families in all respects: inputs, outputs and a single +5V supply.

- Pin-out compatible to 2114 MOS RAM
- Fast access time:
  - 150 ns max. (MB 8114H)
  - 200 ns max. (MB 8114E)
  - 250 ns max. (MB 8114N)
- Single +5V power supply
- Low power dissipation
- Common data input and output using three-state outputs
- Standard 18-pin dual-in-line package
- All inputs and outputs have protection against static charge
- Completely static memory

PIN ASSIGNMENT



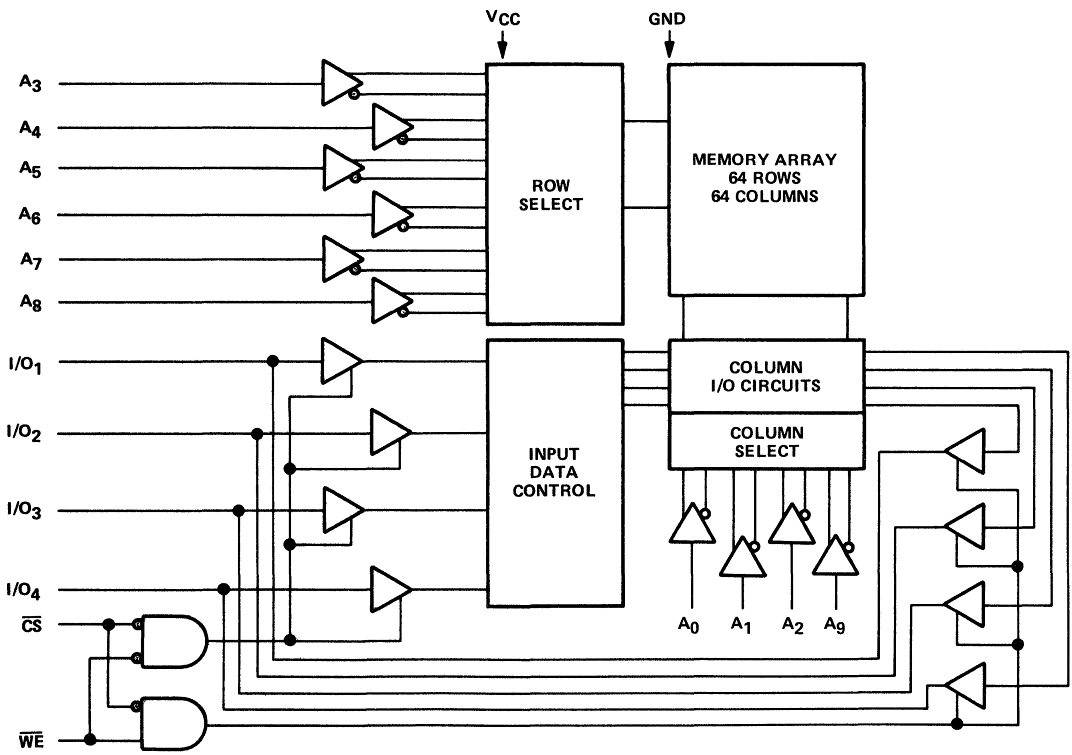
PIN NAMES	
A0 TO A9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CS}$	CHIP SELECT
I/01 – I/04	DATA INPUT/OUTPUT

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Temperature Under Bias	T_{op}	–10 to + 85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Supply Voltage	V_{CC}	–0.5 to +7	V
Input Voltage	V_{IN}	–0.5 to +7	V
Output Voltage	V_{OUT}	–0.5 to +7	V
Power Dissipation	P_W	1.0	W

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 BLOCK DIAGRAM



DC CHARACTERISTICS

V_{CC} = 5V ± 5%, T_A = 0°C to +70°C

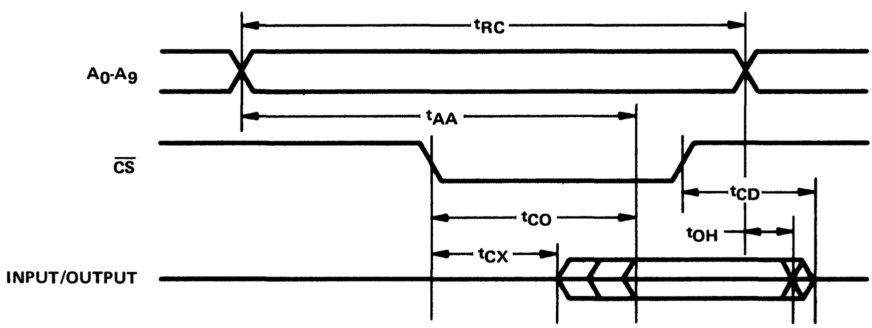
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0 mA	2.4			V
Input Low Voltage	V_{IL}		−0.5		0.8	V
Input High Voltage	V_{IH}		2.2			V
Input Load Current	I_{LI}	V_{IN} = 0 to +5.25V			10	μA
I/O Leakage Current	I_{LOL}	$\overline{CS}$ = 2.2V $V_{I/O}$ = 0.4V			−10	μA
I/O Leakage Current	I_{LOH}	$\overline{CS}$ = 2.2V $V_{I/O}$ = 5.25V			10	μA
Power Supply Current	I_{CC}	V_{IN} = 5.25V I/O = 0 mA T_A = 0°C			90	mA

AC CHARACTERISTICS

READ CYCLE
V_{CC} = 5V ± 5%, T_A = 0°C to +70°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	150			ns
Address Access Time	t_{AA}			150	ns
Chip Select Time	t_{CO}			70	ns
Chip Selection to Output Active	t_{CX}	0			ns
Chip Select to Output Disable Time	t_{CD}			50	ns
Previous Read Data Valid After Change of Address	t_{OH}	20			ns

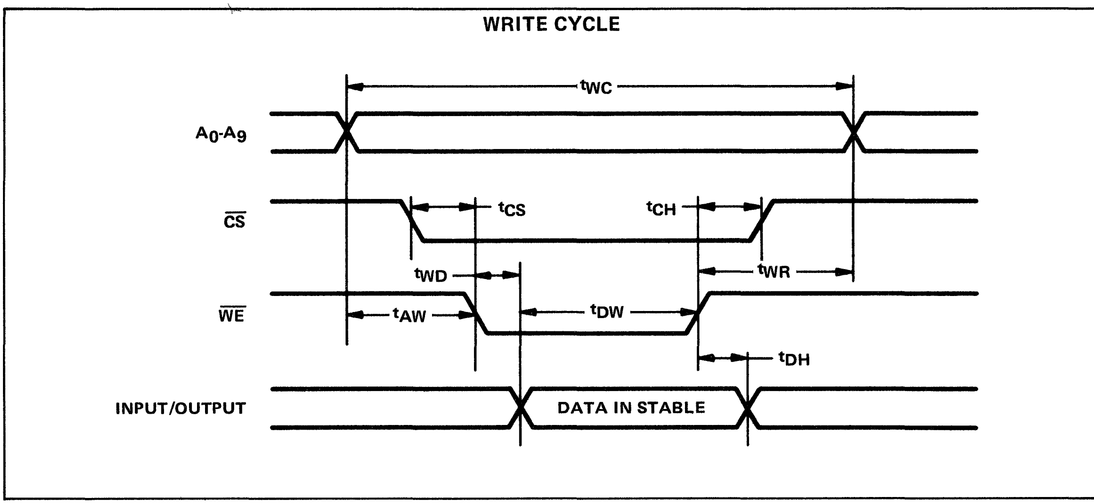
WAVEFORM



WRITE CYCLE
V_{CC} = 5V ± 5%, T_A = 0°C to +70°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	150			ns
Address to Write Setup Time	t_{AW}	30			ns
Data Setup Time	t_{DW}	50			ns
Write to Output Disable Time	t_{WD}	50			ns
Chip Select Setup Time	t_{CS}	0			ns
Chip Select Hold Time	t_{CH}	0			ns
Write Recovery Time	t_{WR}	20			ns
Data Hold Time	t_{DH}	0			ns

WAVEFORM



DYNAMIC CONDITIONS OF TEST

Input Pulse Levels: 0.8V to +2.2V
Input Rise and Fall Time: 10 ns
Timing Measurement Input: 1.5V
Reference Levels: 1.5V
Output Load: 1 TTL Gate and C_L = 50 pF

CAPACITANCE

$T_A = 25°C$, f = 1 MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			5	pF
Input Capacitance	C_{IN}			5	pF

UV ERASABLE 8192-BIT READ ONLY MEMORY

FUJITSU

MB 8518E/H

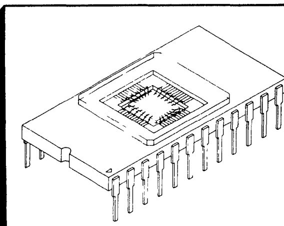
MOS 8192-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MB 8518 is a high speed 8192-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 24-pin dual-in-line package with a transparent lid is used to package the MB 8518. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MB 8518 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. A pin-for-pin equivalent mask programmed ROM, the Fujitsu MB 8308, is available for large volume requirements.

- 1024 words by 8 bits organization, fully decoded
- Fast programming (typ. 100 sec. for all 8192 bits)
- Low power requirement (only one high-level pulse required)
- No clocks required (fully static operation)
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip Select ($\overline{CS}$) lead for simplified memory expansion



CASE DIP24-A
CERAMIC PACKAGE

- Choice of access times (450 ns or 650 ns max.)
- Standard (+12V and ±5V) power supplies
- Standard 24-pin DIP package
- Interchangeable with Intel 2708

MOS Memories

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to + 85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs (Except PRG and $\overline{CS}$/WE) with Respect to V_{BB}	V_{IN1}, V_{OUT}	−0.3 to +15	V
Program Input with Respect to V_{BB}	V_P	−0.3 to +35	V
$\overline{CS}$/WE with Respect to V_{BB}	V_{IN2}	−0.3 to +20	V
V_{CC} and V_{SS} with Respect to V_{BB}	V_{CC}, V_{SS}	−0.3 to +15	V
V_{DD} with Respect to V_{BB}	V_{DD}	−0.3 to +20	V
Power Dissipation	P_D	1.5	W

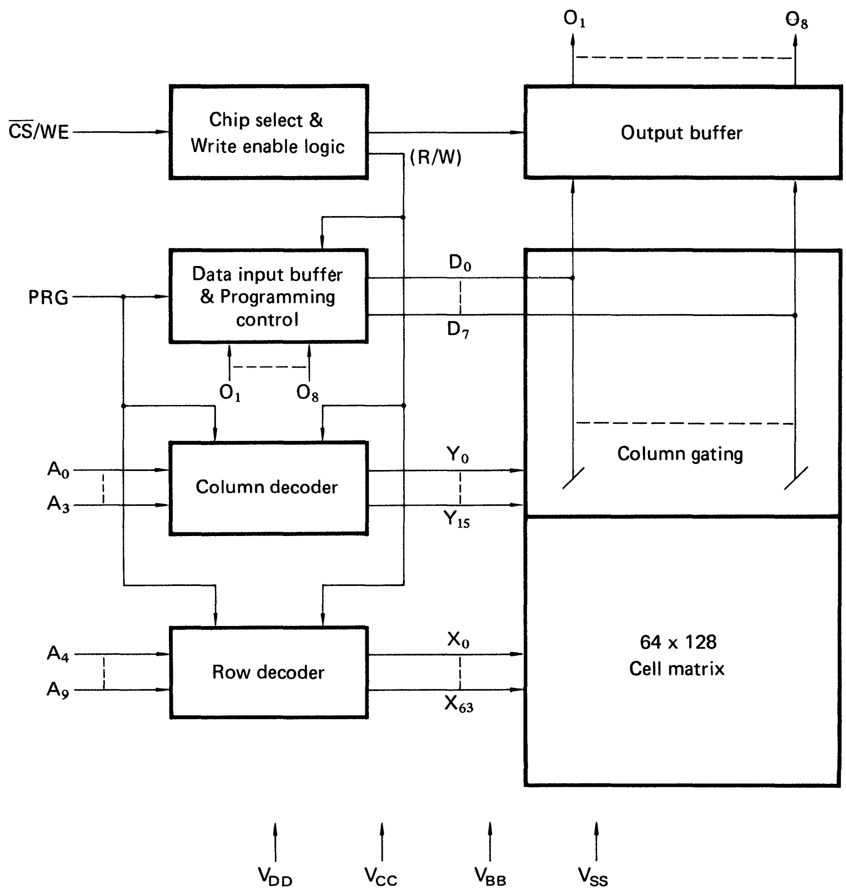
Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

A_7	1	24	V_{CC}
A_6	2	23	A_8
A_5	3	22	A_9
A_4	4	21	V_{BB}
A_3	5	20	$\overline{CS}$/WE
A_2	6	19	V_{DD}
A_1	7	18	PRG
A_0	8	17	O_8
O_1	9	16	O_7
O_2	10	15	O_6
O_3	11	14	O_5
V_{SS}	12	13	O_4

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Fig. 1 — MB 8518 BLOCK DIAGRAM



FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (1~8, 22, 23)	Data I/O (9~11,13~17)	V_{SS} (GND) (12)	PRG (Program) (18)	V_{DD} Supply (19)	$\overline{CS}$/WE (20)	V_{BB} Supply (21)	V_{CC} Supply (24)
Read	A_{IN}	D_{OUT}	GND	GND	+12V	V_{IL}	–5V	+5V
Deselect	DON'T CARE	HIGH Z	GND	GND	+12V	V_{IH}	–5V	+5V
Program	A_{IN}	D_{IN}	GND	PULSED +26V	+12V	V_{IHW}	–5V	+5V

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Recommended DC operating conditions and 0 ~ 70°C temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	11.4	12	12.6	V
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Supply Voltage	V_{SS}	—	0.0	—	V
Supply Voltage	V_{BB}	−4.75	−5.0	−5.25	V
Input High Voltage	V_{IH}	3.0	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.65	V

DC CHARACTERISTICS (Pin 18 PRG must be tied to V_{SS} during read operation.)

Parameter	Symbol	Min	Typ	Max	Unit
Address and Chip Select Input Load Current (V_{IN}=5.25V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT}=5.25V, $\overline{CS}$/WE=5V)	I_{LO}	—	—	10	μA
V_{DD} Supply Current (All Inputs=V_{IH}, $\overline{CS}$/WE=5V)	I_{DD}*	—	50	65	mA
V_{CC} Supply Current (All Inputs=V_{IH}, $\overline{CS}$/WE=5V)	I_{CC}*	—	7	10	mA
V_{BB} Supply Current (All Inputs=V_{IH}, $\overline{CS}$/WE=5V)	I_{BB}*	—	30	45	mA
Output Low Voltage (I_{OL}=1.6mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH}=−100μA)	V_{OH1}	3.7	—	—	V
Output High Voltage (I_{OH}=−1mA)	V_{OH2}	2.4	—	—	V
Power Dissipation (T_A=70°C)	P_D	—	—	800	mW

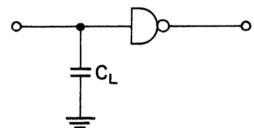
***Note:** Typical values are measured at nominal voltage and T_A=25°C; max. values at T_A=0°C.

CAPACITANCE (T_A=25°C; f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN}=0V)	C_{IN}	—	4	6	pF
Output Capacitance (V_{OUT}=0V)	C_{OUT}	—	8	12	pF

Fig. 2 — DYNAMIC TEST CONDITIONS

Input Pulse Levels:	0.65V to 3.0V
Input Rise and Fall Time:	≦20ns
Timing Measurement Reference Levels:	0.8V and 2.8V for inputs
	0.8V and 2.4V for outputs
Output Load:	1 TTL gate and C_L=100pF



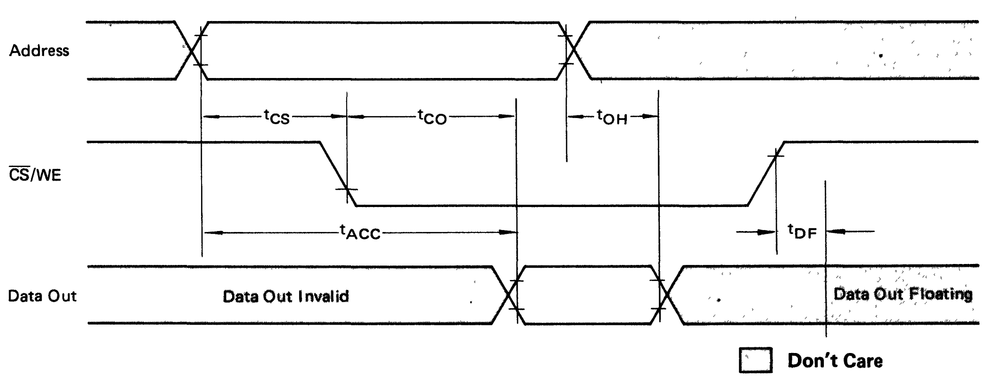
DYNAMIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB 8518E			MB 8518H			Unit
		Min	Typ	Max	Min	Typ	Max	
Address to Output Delay	t_{ACC}	—	—	650	—	—	450	ns
Chip Select to Output Delay	t_{CO}	—	—	120	—	—	120	ns
Chip Deselect to Output Float	t_{DF}	0	—	120	0	—	120	ns
Address to Output Hold	t_{OH}	0	—	—	0	—	—	ns
Chip Select Delay	t_{CS}*	—	—	530	—	—	330	ns

***Note:** $t_{ACC}=t_{CS}+t_{CO}$ at t_{CS} > 330ns, and t_{ACC}=450ns (max.) at t_{CS} ≦ 330ns.

OPERATION TIMING DIAGRAM



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs V_{DD} SUPPLY VOLTAGE

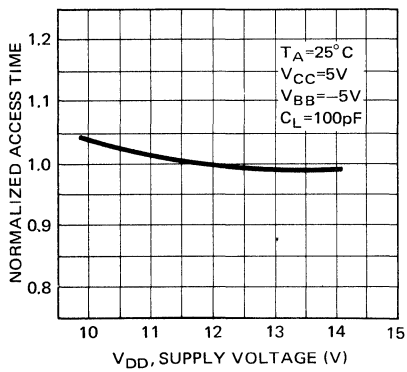


Fig. 4 – NORMALIZED ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

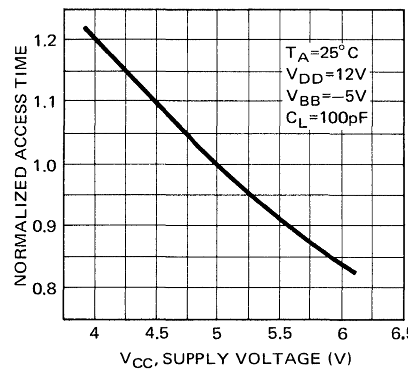


Fig. 5 – NORMALIZED ACCESS TIME vs V_{BB} SUPPLY VOLTAGE

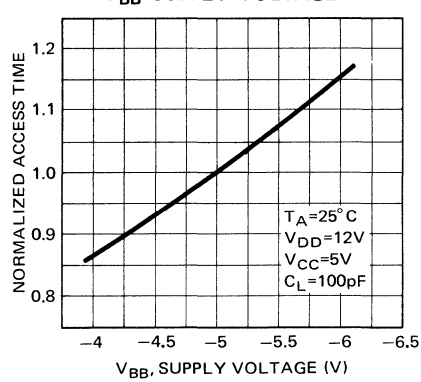


Fig. 6 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

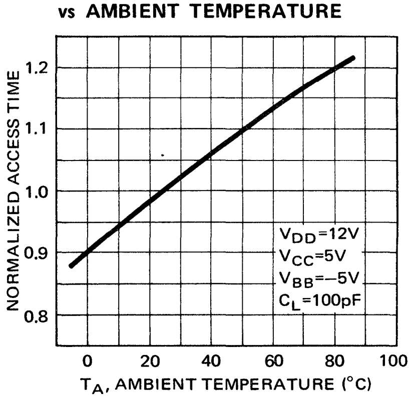
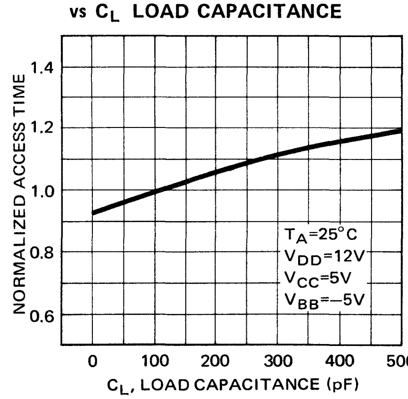


Fig. 7 – NORMALIZED ACCESS TIME vs C_L LOAD CAPACITANCE



MOS Memories

Fig. 8 — I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

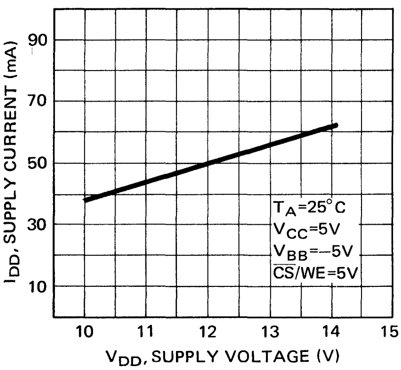


Fig. 9 — I_{CC} SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

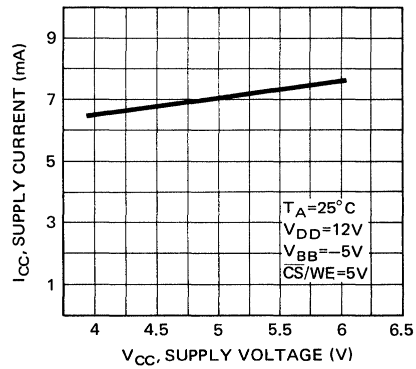


Fig. 10 — I_{BB} SUPPLY CURRENT vs V_{BB} SUPPLY VOLTAGE

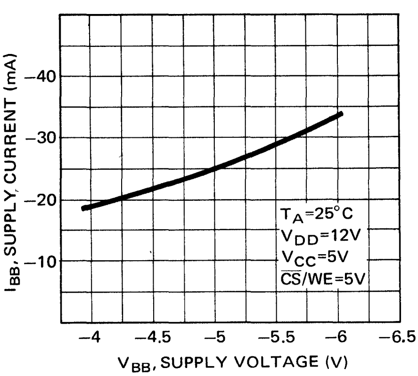


Fig. 11 — I_{OH} OUTPUT SOURCE CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

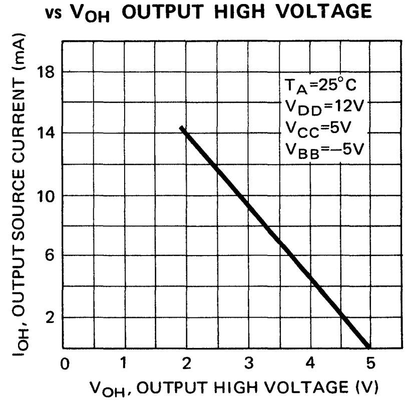


Fig. 12 — I_{OL} OUTPUT SINK CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

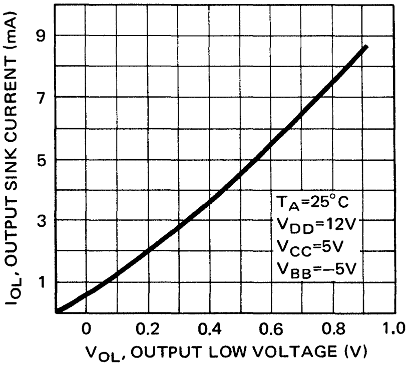
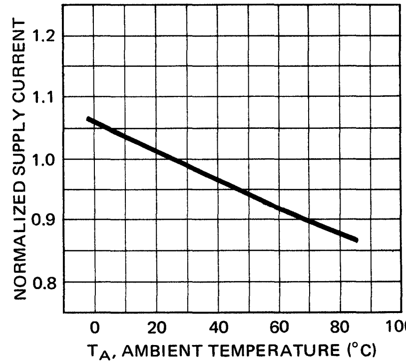


Fig. 13 — NORMALIZED SUPPLY CURRENT vs AMBIENT TEMPERATURE



PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MB 8518 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 14). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 15). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{THO}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 15.

Fig. 14 — MEMORY CELL

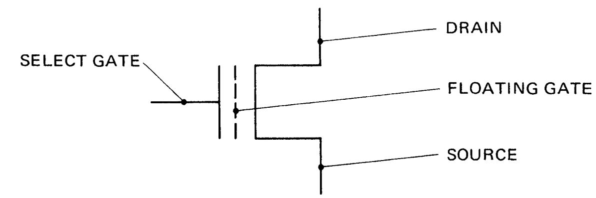
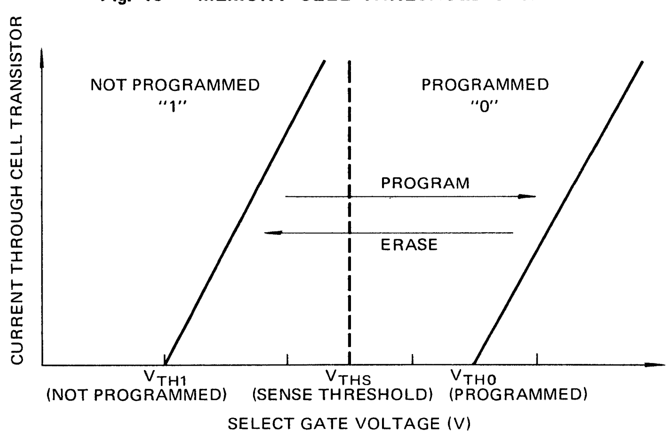


Fig. 15 — MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Initially, and after each erasure, all bits are in the "1" (output high) state. Information is stored by programming a "0" into each desired bit location. Address and supply voltage (V_{DD}, V_{CC}, V_{BB} and V_{SS}) input levels used in the read mode of operation are also applicable in the programming mode. For programming operation, the circuit is set up by applying +12V to the $\overline{CS}$/WE lead (pin 20). The word address is then selected in the same manner as in the read mode, with data to be programmed applied 8 bits in parallel to the data lines ($O_1 \sim O_8$). After address and data set up, one program pulse (V_P) per address is applied to the Program input (pin 18). One pass through all addresses to be programmed is defined as a program loop. The number of loops required (N) is a function of the program pulse width (t_{PW}) according to the formula $N \times t_{PW} \geqq 100$ msec. For programming verification, program loops and read loops may be alternated as shown in "Read/Program/Read Transitions Diagram" on page 10.

During programming, the selected row and column lines are pulsed to approximately 22 volts, and the floating gate is charged (as described previously). It is the presence of these 22V pulses on the interconnected gates that leads to the requirement that *all addresses must be programmed sequentially; programming of single words or small blocks of words is not allowed,* as transients may be generated that could partially alter the charge state of cells not being programmed.

ERASING

The MB 8518 can be erased by exposure to high-intensity, shortwave ultraviolet light at a wavelength of 2537Å. The recommended integrated dosage (UV intensity x exposure time) is 10Wsec./cm^2. Normally, commercial ultraviolet lamps should be used without shortwave filters, with the device to be erased placed one inch (2 to 3cm) away from the lamp tube. It is suggested that a guard band of 3~4 times the

(cont.)

PROGRAMMING/ERASING INFORMATION (continued)

minimum required period for erasure be used, the minimum period being the time which appears to erase all bits. The guard band will ensure erasure at temperature and voltage extremes. Typical guard band erase times for various UV source power ratings are: typically 10 minutes for 12,000μW/cm^2; typically 30 minutes for 6,000μW/cm^2.

SUPPLEMENTARY INFORMATION

Programming can be performed in accordance with the procedure described in "Programming" on page 7. A recommended circuit for programming pulse generation is shown in Fig. 16. The program pulse high voltage (V_{PH}) source must sink more than 20mA, and the program pulse low voltage (V_{PL}) source should drive more than 8mA.

The width of the program pulse can vary anywhere from 0.1 to 1.0 msec. The number of loops (N) can vary from a minimum of 100 (t_{PW}=1.0 msec.) to a maximum of more than 1,000 (t_{PW}=0.1 msec.), depending on the value selected for t_{PW}. Remember, however, *there must be "N" successive loops through all 1024 addresses. It is incorrect to apply "N" program pulses to one address, change to the next address, and again apply "N" program pulses.*

With reference to the timing diagram, optimum or more efficient programming is achieved when:

$t_{CSS} = t_{AS} = t_{DS} = 10\ \mu$sec.
$t_{PW} = 1.0$ msec.
$t_{AH} = t_{DH} = 1.0\ \mu$sec.
$t_{PR} = t_{PF} = 0.5\ \mu$sec.

Thus the time for one address is:

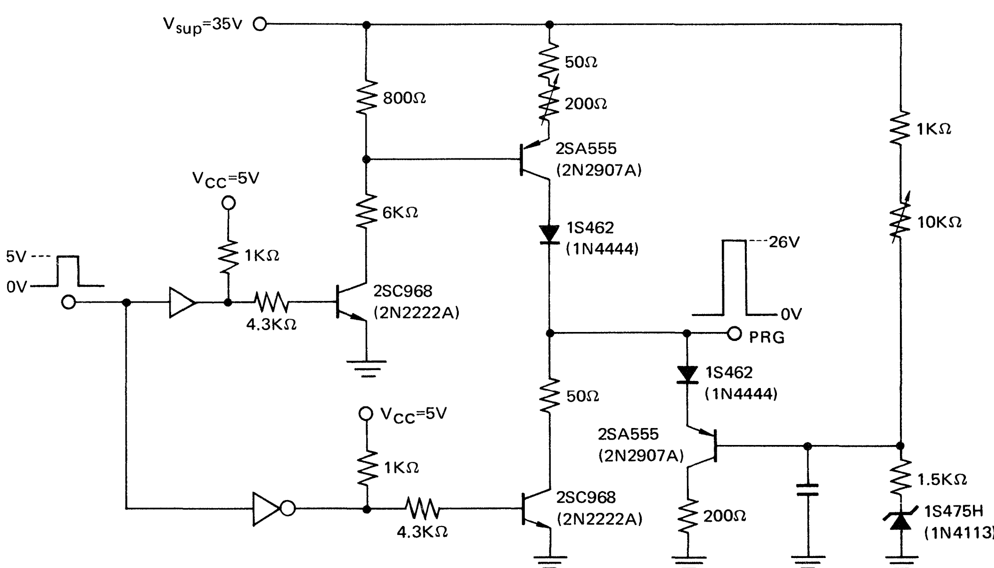
$t_{AS} + t_{PR} + t_{PW} + t_{PF} + t_{AH} =$ 1.012 msec.

For 100 loops and 1024 addresses, the total time to program an entire device will be:

1.012 msec./address x 100 loops x 1024 addresses = 103.6 sec.

Note that the program pulse duty cycle is approximately 99%. Regardless of the length of the program pulse, the requirement for making successive passes through all addresses cannot be eliminated.

Fig. 16 – SAMPLE PROGRAM PULSE DRIVER CIRCUIT



STATIC SPECIFICATIONS (T_A=25°C, V_{DD}=12V±5%, V_{CC}=5V±5%, V_{SS}=0V, V_{BB}=−5V±5%)

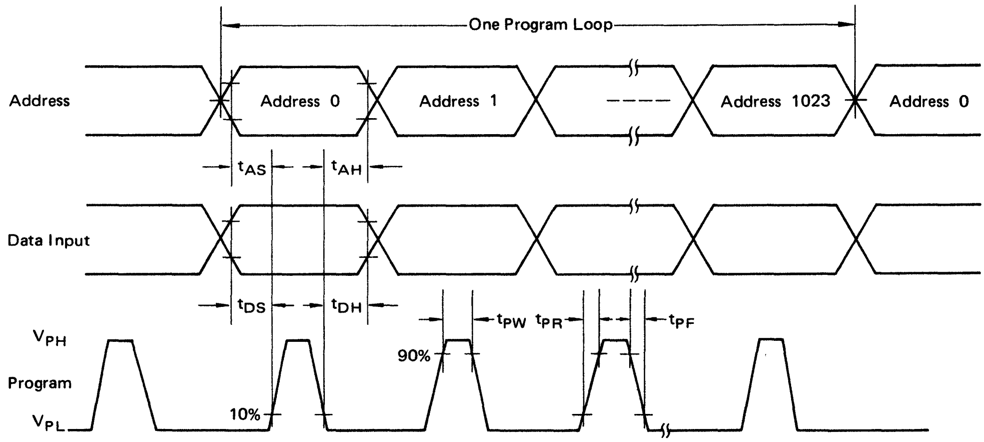
Parameter	Symbol	Min	Typ	Max	Unit
Input High Voltage for Address and Data	V_{IH}	3.0	—	V_{CC}+1	V
Input Low Voltage for Address and Data	V_{IL}	V_{SS}	—	0.65	V
Address and Data Input Load Current (V_{IN}=5.25V, $\overline{CS}$/WE=11.4V)	I_{LIA}, I_{LID}	—	—	10	μA
$\overline{CS}$/WE Input Load Current ($\overline{CS}$/WE=12.6V)	I_{LIW}	—	—	10	μA
$\overline{CS}$/WE Input High Voltage	V_{IHW}	11.4	—	12.6	V
V_{DD} Supply Current (All Inputs=V_{IH}, PRG=V_{PL}, $\overline{CS}$/WE=11.4V)	I_{DDW}	—	—	78	mA
V_{CC} Supply Current (All Inputs=V_{IH}, $\overline{CS}$/WE=11.4V)	I_{CCW}	—	—	12	mA
V_{BB} Supply Current (All Inputs=V_{IH}, $\overline{CS}$/WE=11.4V)	I_{BBW}	—	—	50	mA
Program Pulse Source Current	I_{PL}	—	—	8	mA
Program Pulse Sink Current	I_{PH}	—	—	20	mA
Program Pulse Low Voltage	V_{PL}	V_{SS}	—	1	V
Program Pulse High Voltage	V_{PH}	—	—	27	V
Program Pulse Height	—	25	—	27	V

DYNAMIC SPECIFICATIONS (T_A=25°C)

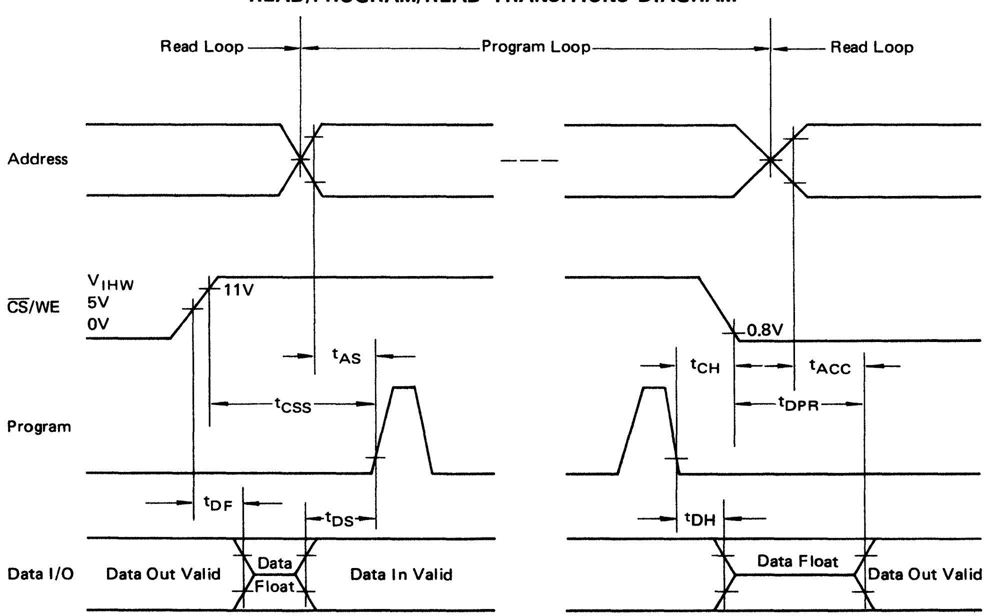
Parameter	Symbol	Min	Typ	Max	Unit
Address Set Up Time	t_{AS}	10	—	—	μs
$\overline{CS}$/WE Set Up Time	t_{CSS}	10	—	—	μs
Data Set Up Time	t_{DS}	10	—	—	μs
Address Hold Time	t_{AH}	1	—	—	μs
$\overline{CS}$/WE Hold Time	t_{CH}	0.5	—	—	μs
Data Hold Time	t_{DH}	1	—	—	μs
Chip Deselect to Output Float Delay	t_{DF}	0	—	120	ns
Program to Read Delay	t_{DPR}	—	—	10	μs
Program Pulse Width	t_{PW}	0.1	—	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	—	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	—	2.0	μs

PROGRAMMING/ERASING INFORMATION (continued)

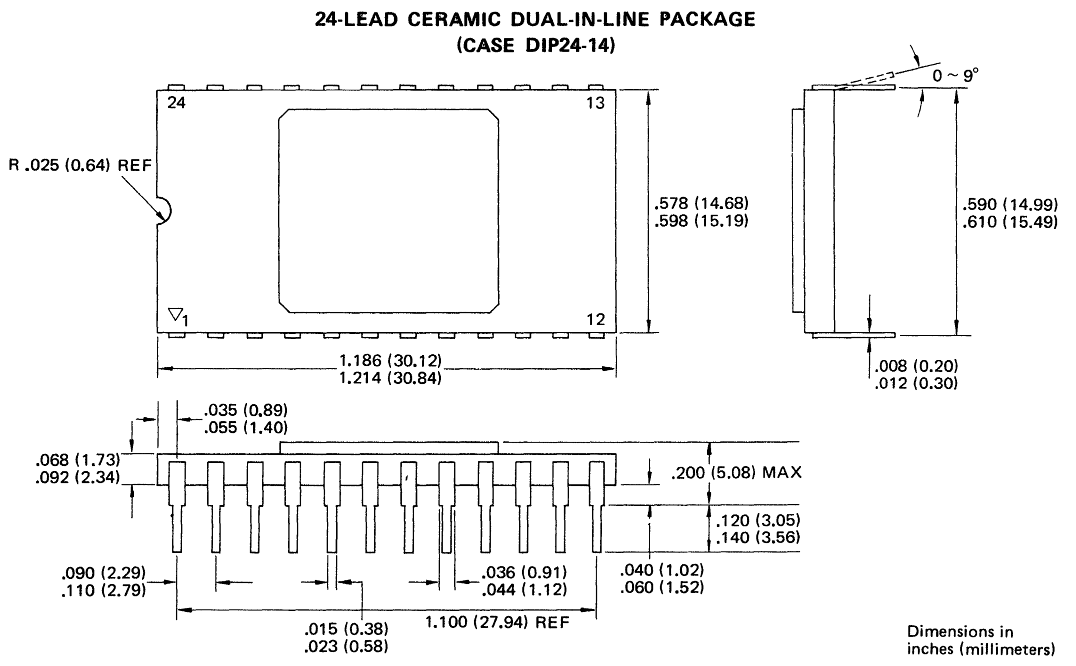
PROGRAM MODE TIMING DIAGRAM



READ/PROGRAM/READ TRANSITIONS DIAGRAM



PACKAGE DIMENSIONS



MOS 8192-BIT STATIC READ ONLY MEMORY

MB 8308N/E

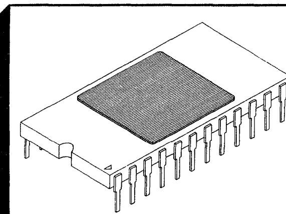
FUJITSU

MOS 8192-BIT MASK PROGRAMMED READ ONLY MEMORY

The Fujitsu MB 8308 is a high performance 8192-bit static N-channel MOS mask-programmed read only memory (ROM). The memory is organized as 1024 words by 8 bits — a feature which simplifies the design of small memory systems, permitting incremental memory sizes as small as 1024 words.

The fast access time allows the ROM to service high performance microcomputer applications without stalling the processor. Two chip select input signals are logically ANDed together to provide control of the output buffers. As chip select polarity can be customer specified, addressing of 4 memory chips without external gating is possible. The outputs of unselected chips are turned off and assume a high-impedance state, enabling them to be OR-wired with additional MB 8308 devices and other 3-state components.

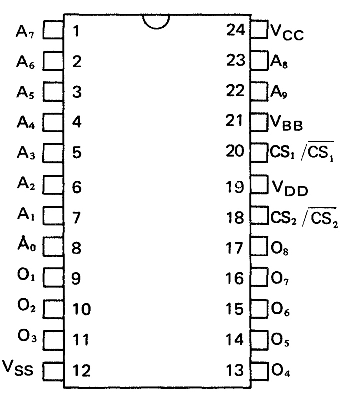
- 1024 words by 8 bits organization
- Choice of high speed access times (250 ns or 450 ns max.)
- Two fully programmable chip select inputs
- Low capacitance inputs for simplified driving
- Logic voltage levels compatible to TTL
- 3-state output buffers for simplified expansion
- Standard (+12V and ±5V) power supplies
- N-channel silicon gate MOS technology
- Mask-programmed version of Fujitsu MB 8518 EROM



CASE DIP24-B
CERAMIC PACKAGE

- Direct plug-in replacement for Intel 8308/2308

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Temperature Under Bias	T_A	-25 to +85	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Voltage on Any Pin with Respect to V_{BB}	V_{IN}, V_{OUT}	-0.3 to +20	V
Power Dissipation	P_D	1.0	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{DD}	11.4	12.0	12.6	V	0°C to +70°C
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Supply Voltage	V_{SS}	0.0	0.0	0.0	V	
Supply Voltage	V_{BB}	−4.75	−5.0	−5.25	V	
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V	
Input Low Voltage	V_{IL}	−1	—	0.8	V	

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V)	I_{LI}	—	—	10	μA
Output Leakage Current (Chip deselected)	I_{LO}	—	—	10	μA
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH1}	2.4	—	—	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH2}	3.7	—	—	V
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	—	—	0.45	V
V_{CC} Supply Current	I_{CC}	—	—	2.0	mA
V_{DD} Supply Current	I_{DD}	—	—	60	mA
V_{BB} Supply Current	I_{BB}	—	10	1000	μA
Power Dissipation	P_D	—	—	775	mW

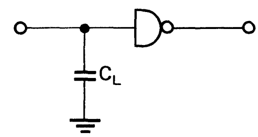
CAPACITANCE (T_A = 25°C; f = 1 MHz; V_{BB} = −5V; V_{DD}, V_{CC} and all other pins tied to V_{SS}.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	—	—	6	pF
Output Capacitance	C_{OUT}	—	—	12	pF

MOS Memories

Fig. 1 — DYNAMIC TEST CONDITIONS

Input Pulse Levels:	0.8V to 2.4V
Input Rise and Fall Time:	20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.4V for outputs
Output Load:	1 TTL gate and C_L = 100pF



DYNAMIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB 8308N			MB 8308E			Unit
		Min	Typ	Max	Min	Typ	Max	
Address to Output Delay	t_{ACC}	—	200	450	—	160	250	ns
Chip Select to Output Delay	t_{CO}	—	85	160	—	85	160	ns
Chip Select to Output Data Float	t_{DF}	—	85	160	—	85	160	ns
Output Data Hold	t_{OH}	0	—	—	0	—	—	ns

OPERATION TIMING DIAGRAM

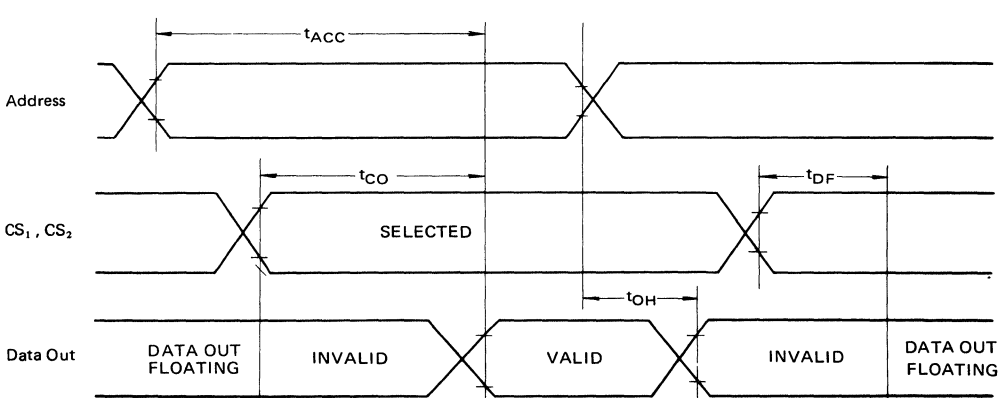
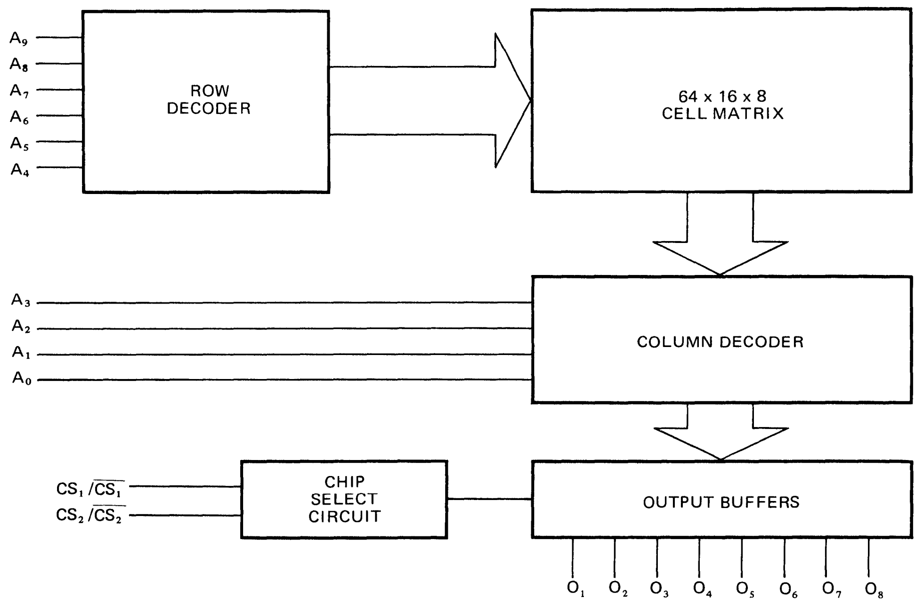


Fig. 2 — MB 8308 BLOCK DIAGRAM



TYPICAL CHARACTERISTICS CURVES

Fig. 3 — I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

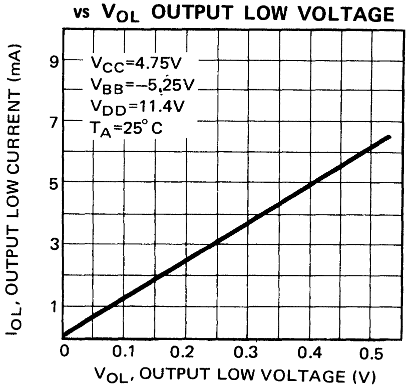


Fig. 4 — I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

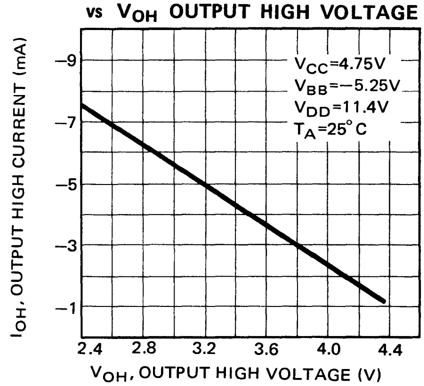


Fig. 5 — I_{OL} OUTPUT LOW CURRENT vs AMBIENT TEMPERATURE

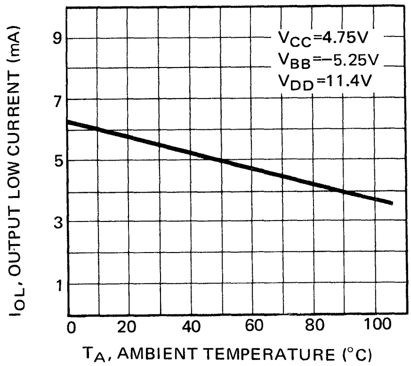


Fig. 6 — I_{OH} OUTPUT HIGH CURRENT vs AMBIENT TEMPERATURE

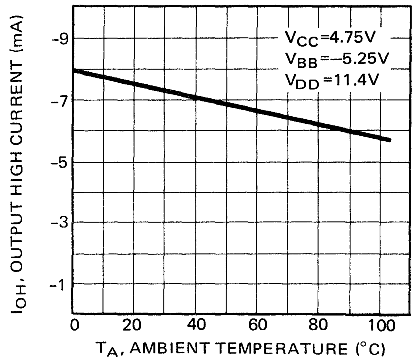


Fig. 7 — I_{CC}, I_{DD} NORMALIZED vs AMBIENT TEMPERATURE

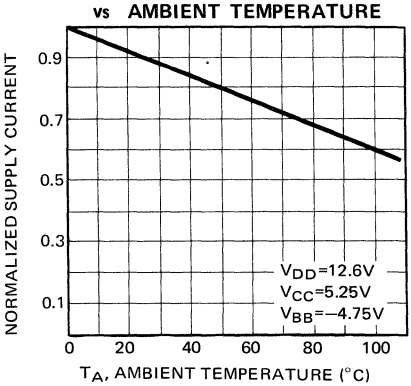


Fig. 8 — Δ OUTPUT DELAY TIME vs Δ CAPACITANCE

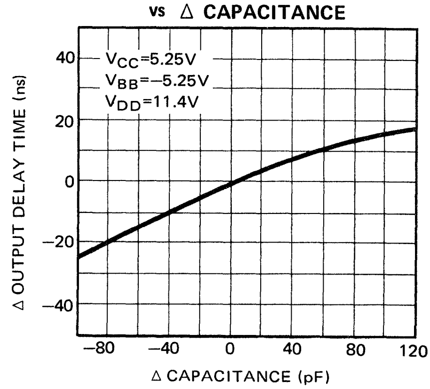


Fig. 9 — t_{ACC} NORMALIZED vs AMBIENT TEMPERATURE

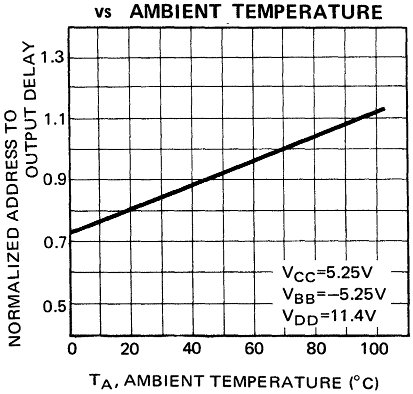
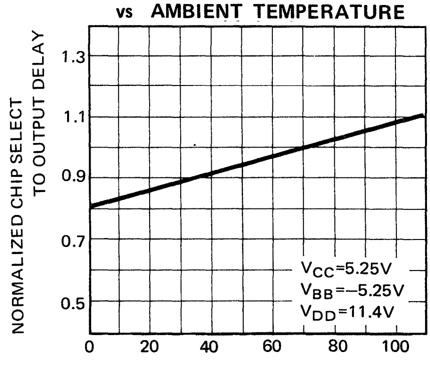


Fig. 10 — t_{CO} NORMALIZED vs AMBIENT TEMPERATURE



PROGRAMMING INFORMATION

The Fujitsu MB 8308 is factory-programmed utilizing a metal mask designed to the customer's specifications. Data for MB 8308 programming is normally submitted on punch cards or paper tape, following the procedures outlined below (note that in the examples given, positive logic convention is used). A printout of the truth table should be supplied with the order.

CHIP SELECT OPTION

There are two chip select pins ($CS_1/\overline{CS_1}$ and $CS_2/\overline{CS_2}$) on the MB 8308. The input code for these pins is a customer option to be specified according to the chip select truth table on this page.

ADDRESS/DATA FORMAT

The MB 8308 has 1024 address locations, each address containing 8 data bits (either logic "1" or logic "0"). The data to be programmed in each address location is provided by the customer in the form of two hexadecimal digits per address followed by a separation notation consisting of either a blank for punch cards or a decimal point (".") for paper tape. The first hexadecimal digit corresponds to bits 5 to 8 for the address, while the second hexadecimal digit corresponds to bits 1 to 4. The address of the 8 bits to be programmed is assigned using three hexadecimal digits for punch cards and four hexadecimal digits for paper tape. If an address is not selected, the 8 bits in that address are considered to be positive logic "0's".

PUNCH CARD FORMAT

80-column Hollerith cards should be used, punched with an IBM 026/029 keypunch or equivalent. The first card is a title card, the second is for defining the chip select option desired, and the remaining 64 cards are for defining the bit pattern to be programmed for all 1024 addresses.

The format used requires only 64 cards for defining the data to be programmed. Each of the data cards contains the 8 bits of data for each of 16 address locations. The 16 address locations include the address punched in columns 21~23 of the card and the next fifteen sequential locations. The address is defined by a 3-digit hexadecimal number and must be 000 (the first address in memory) or one of any multiple of 16 up to 3F0 (the last address in memory minus 15, or decimal number 1,008). In other words, all data is handled in blocks of 16 addresses, with the first address for each block being one of 64 possibilities; i.e., 0, 16, 32, 48, 64, 80, . . . 1008. If any block of 16 addresses is left out of the punch card deck, all the data in those addresses will be automatically masked as zeroes.

Data is punched in columns 30~76, starting with the 8 bits of data associated with the address in columns 21~23 of the card; this is continued for the next fifteen address locations. Each 8 bits of data for the address are punched in two adjacent columns as any two-digit hexadecimal number from 00 (binary 00000000) to FF (binary 11111111). Be sure to leave a blank space between each two-digit data input hexadecimal number entered (i.e., columns 32, 35, etc.).

CHIP SELECT TRUTH TABLE

CHIP SELECT NUMBER	SELECTED $CS_2/\overline{CS_2}$	SELECTED $CS_1/\overline{CS_1}$	DESELECTED
0 0	0	0	0 1, 1 0, 1 1
0 1	0	1	0 0, 1 0, 1 1
1 0	1	0	0 0, 0 1, 1 1
1 1	1	1	0 0, 0 1, 1 0

PUNCH CARD DEFINITION TABLE

Title Card		
Columns	1 ~ 9	Blank
Columns	10 ~ 29	Customer's name, ROM pattern number, etc. Any alpha-numeric characters
Columns	30 ~ 31	Blank
Columns	32 ~ 37	Punch a right-justified decimal number to indicate the total number of bit "1's" in the data field of the ROM. The maximum number is 8192. The chip select code bits are not included in this number. Note that this is an optional check, and the card field may be left blank.
Columns	38 ~ 80	Blank
Chip Select Card		
Columns	1 ~ 30	Blank
Columns	31, 33	Chip select numbers (00, 01, 10, or 11)
Columns	32, 34 ~ 80	Blank
Data Cards		
Columns	1 ~ 20	Blank
Columns	21 ~ 23	Address. A hexadecimal number between 000 and 3F0 is entered. Note that column 23 is always zero.
Columns	24 ~ 29	Blank
Columns	30 ~ 76	Data. Two columns per address starting with the 8 bits of data for the address punched in columns 21~23 are entered. Each 8 bits of data is coded as a hexadecimal number, 00 through FF. Leave a blank between each two-digit hexadecimal number.
Columns	77 ~ 80	Blank

PAPER TAPE FORMAT

Punched paper tape may be utilized to provide memory data information. Either an 8-bit ASCII code or ISO code with even parity can be used, with the tape format identical to that used for punch cards. Thus, the tape will have a title section, a chip select section and a data section. However, the chip select section should be coded last on the paper tape. Also, there is no data check total, as provided on the title punch card (columns 32~37).

Title Section— Up to 20 alpha-numeric characters are permitted. The first entry is "$" and the last is "LF" (line feed).

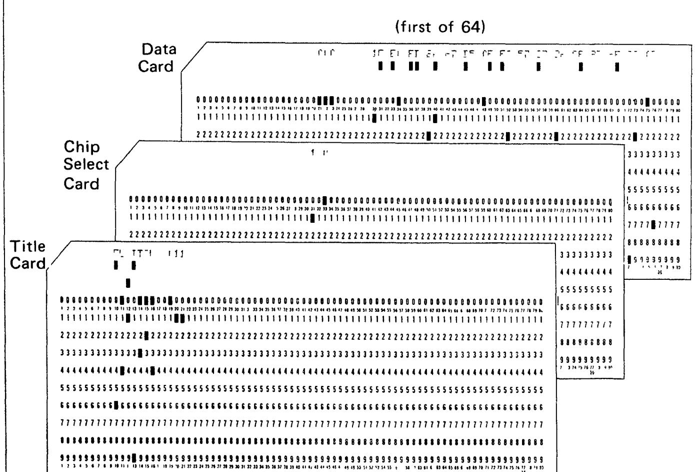
Data Section— Type "#" before an address and "," after an address. As with the punch cards, up to 64 addresses may be used. The address is defined by a four-digit hexadecimal number which must be 0000 or any multiple of 16 up to 03F0. Data numbers follow the address, and are assumed to be the data for addresses incremented in ascending order starting with the last address defined by "#". A data number used is any two-digit hexadecimal number from 00 to FF, and must be followed by a decimal point (".").

Unlike punch cards, the tape option does not require that an address be denoted prior to every block of 16 addresses of data. In other words, a successive string of data for more than 16 address locations is permitted. However, any punched address must follow the rule that it be 0000 or a multiple of 16 up to 03F0. In order to facilitate checking, we suggest that an address label be used between every block of 16 locations programmed.

Any block of memory locations not punched will be treated as zeroes. At the end of the data section, punch ")"; thus, the last punches in this section will be a hexadecimal data number followed by a decimal point and ")".

Chip Select Section— Type "*" before and after the chip select number. This entry will be made directly after the data section end mark ")". As before, entries can be 00, 01, 10 or 11. Chip select entry example is *10*.

Fig. 11 – EXAMPLE PUNCH CARD DECK



PAPER TAPE CODE TABLE

Character	Use
$	Title start
LF (line feed)	Title end
#	Address start
, (comma)	Address end
. (period)	Data separation
)	Data section end
*	Chip select start/end

MARKING

Up to three alpha-numeric digits are permitted for proprietary identification of a customer's ROM. These numbers will be marked on each package. For convenience, we suggest that these numbers be included as the last three digits of the title card or the title section of the tape, whichever is used, in the allocated space. Also, customers are requested to indicate marking instructions on their purchase order.

HEXADECIMAL NUMBERING SYSTEM

The hexadecimal (HEX) numbering system has a base of 16 and consists of 16 symbols. The table shown lists the binary (base 2) and decimal (base 10) equivalents to the hexadecimal numbers.

In a typical memory system, a "word" is defined as a block of data bits, usually 8 or 16 bits in length. The MB 8308 is organized to provide 8 bits of parallel data at its output at one time. Thus, 1024 address locations are required to locate all 8,192 bits (1024 x 8). For programming purposes, the addresses are numbered from 0_{10} to 1023_{10} or HEX 000 to HEX 3FF.

The programming rules .require that data inputs be handled in blocks of 16 sequential memory locations starting with address 0_{10}. Thus, the addresses for the first memory location of each block are, respectively, 0, 16, 32, 48, 64, and so forth up to 1008 (decimal). In hexadecimal, these numbers are, respectively, 000, 010, 030, 040, 050, and so forth, up to 3F0. Note that the last digit for any of these addresses is always 0.

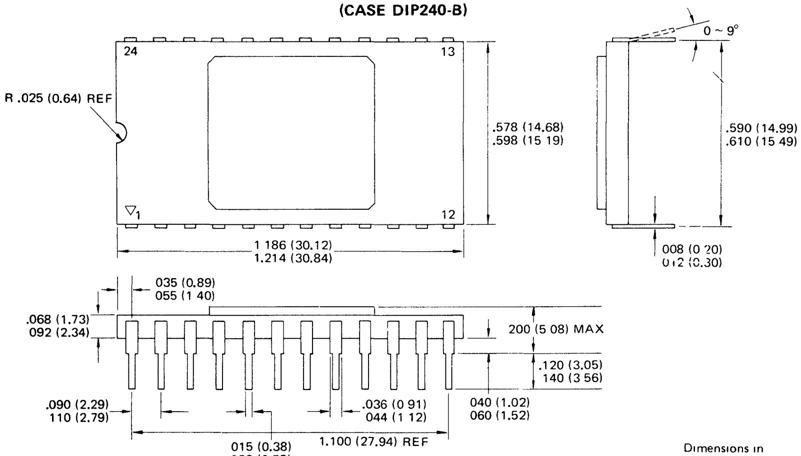
HEX CONVERSION TABLE

HEX Number	Decimal Number	Binary Number
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
A	10	1010
B	11	1011
C	12	1100
D	13	1101
E	14	1110
F	15	1111

MOS Memories

PACKAGE DIMENSIONS

24-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE DIP240-B)

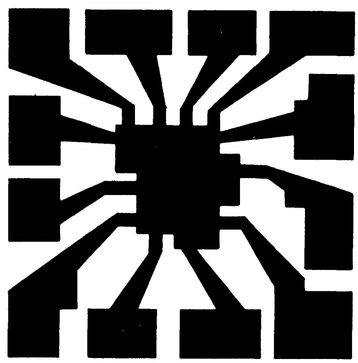


Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information herein has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

Bipolar Memories



Bipolar Memories

FUJITSU

ECL 128-BIT BIPOLAR RANDOM ACCESS MEMORY

MB 7047

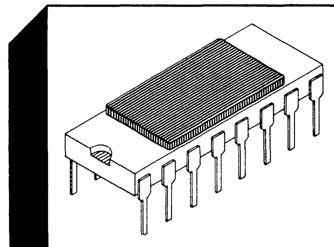
128-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MB 7047 is a fully decoded 128-bit read/write ECL random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 128 words by one bit, and it features on-chip voltage compensation for improved noise margin, two active low chip select lines for ease of memory expansion, and has a separate data in and non-inverting data out line.

The MB 7047 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon) processing. With cell size reduced to approximately half that of normal, ultra-fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MB 7047 is specified over a temperature range of from 0°C to 75°C (ambient). The device comes in a hermetically-sealed glass/ceramic dual-in-line package, and is compatible with industry-standard 10K-series ECL families.

- 128 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Patented DOPOS processing
- Outstanding read access time of 9 ns (typ.)
- Ultra-fast chip select time of 4.5 ns (typ.)
- Low power requirement (3 mW/bit dissipation)
- Multiple chip select leads for simplified memory expansion
- Pin compatible with the MCM10147



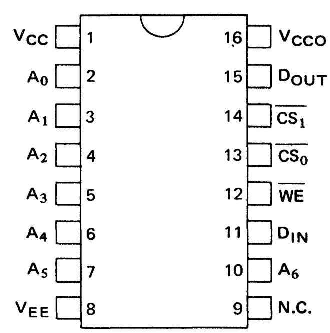
CASE DIP16-A
CERAMIC PACKAGE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC Output High)	I_{OUT}	30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

PIN ASSIGNMENT



Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING RANGES

Part Number	Supply Voltage (V_{EE})			Ambient Temperature
	Min	Typ	Max	
MB 7047	−5.46V	−5.2V	−4.94V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω to −2.0V, Air Flow ≧2.5m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IHmax}$ or V_{ILmin})	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IHmax}$ or V_{ILmin})	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IHmin}$ or V_{ILmax})	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IHmin}$ or V_{ILmax})	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IHmax}$)	I_{IH}			35	μA	0° to 75°C
$\overline{WE}$ Input High Current ($V_{IN} = V_{IHmax}$)	I_{IH}			75	μA	0° to 75°C
Input Low Current ($V_{IN} = V_{ILmin}$)	I_{IL}	−6		6	μA	0° to 75°C
Power Supply Current (All Inputs High and Output Open)	I_{EE}	50	75	100 105	mA	25°C 0° to 75°C

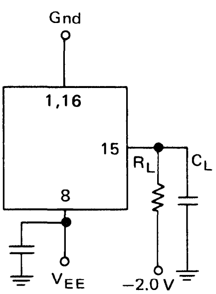
CAPACITANCE

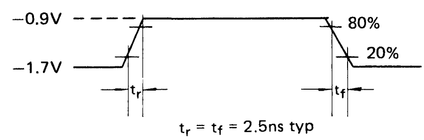
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Input Pin Capacitance	C_{IN}	—	4	5	pF	25°C
Output Pin Capacitance	C_{OUT}	—	7	8	pF	25°C

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V±5%, Output Load = 50Ω to −2V and 15pF to V_{CC}, Air Flow ≧2.5m/s, unless otherwise noted.)

Fig. 1 — AC TEST CONDITIONS





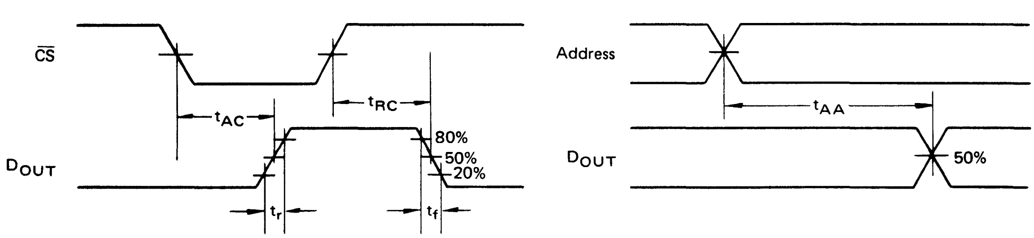
$t_r = t_f$ = 2.5ns typ

Output Load: R_L = 50Ω
C_L = 15pF
(Including Jig and Stray Capacitance)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit	T_A
X-Address Access Time	t_{AAX}		9.0	12.0 14.0	ns	25°C 0° to 75°C
Y-Address Access Time	t_{AAY}		7.0	10.0 12.0	ns	25°C 0° to 75°C
Chip Select Access Time and Recovery Time	t_{AC},t_{RC}		4.5	8.0 8.5	ns	25°C 0° to 75°C

READ CYCLE TIMING DIAGRAMS



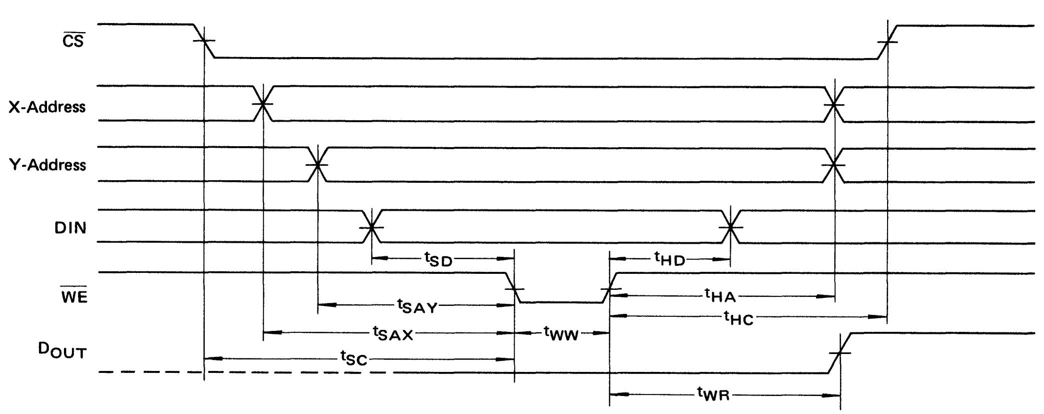
Bipolar Memories

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Write Pulse Width	t_{WW}*	8.0	—	—	ns	0°to 75°C
Write Recovery Time	t_{WR}**	—	—	8.0	ns	25°C
X-Address Set Up Time	t_{SAX}**	4.0	—	—	ns	25°C
Y-Address Set Up Time	t_{SAY}**	3.0	—	—	ns	25°C
Chip Select Set Up Time	t_{SC}**	1.0	—	—	ns	25°C
Data Set Up Time	t_{SD}**	1.0	—	—	ns	25°C
Address Hold Time	t_{HA}**	3.0	—	—	ns	25°C
Chip Select Hold Time	t_{HC}**	1.0	—	—	ns	25°C
Data Hold Time	t_{HD}**	1.0	—	—	ns	25°C

*Note: t_{WW} measured at t_{SA} = 4.0ns
**Note: Values indicated measured at t_{WW} = 8.0ns.

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output Rise Time	t_r	—	1.2	—	ns	25°C
Output Fall Time	t_f	—	1.2	—	ns	25°C

TYPICAL CHARACTERISTICS CURVES

Fig. 2 – V_{OH} OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

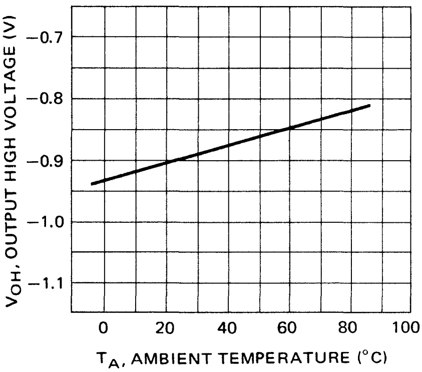


Fig. 3 – V_{OL} OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

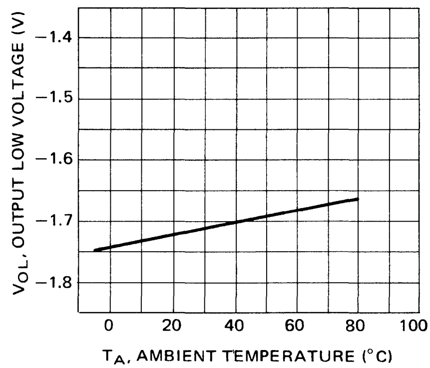


Fig. 4 – I_{EE} SUPPLY CURRENT vs V_{EE} SUPPLY VOLTAGE

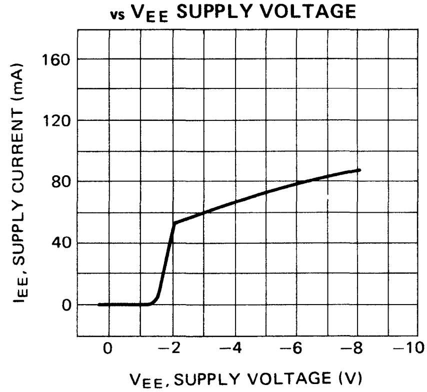


Fig. 5 – I_{IH} INPUT HIGH CURRENT vs AMBIENT TEMPERATURE

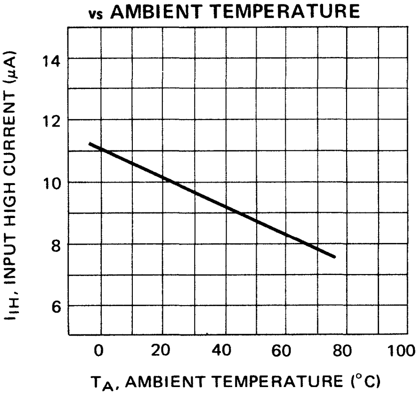
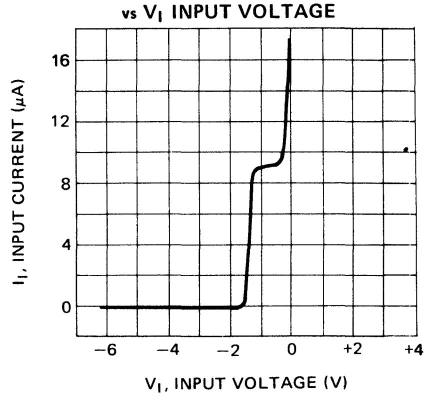


Fig. 6 – I_I INPUT CURRENT vs V_I INPUT VOLTAGE



Bipolar Memories

Fig. 7 — t_{AA} ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

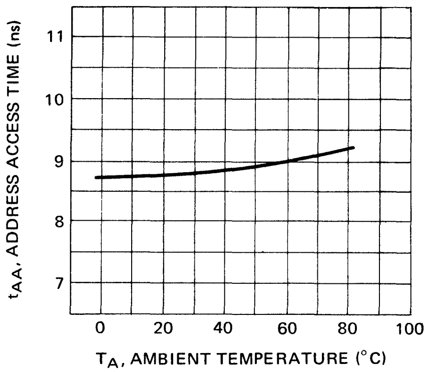


Fig. 8 — t_{AA} ADDRESS ACCESS TIME vs V_{EE} SUPPLY VOLTAGE

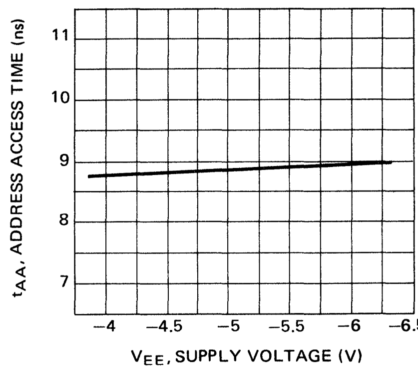


Fig. 9 — t_{WW} WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

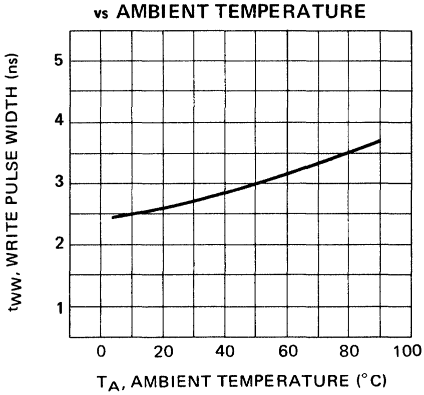
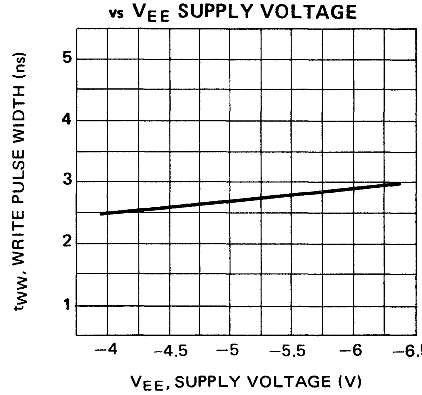
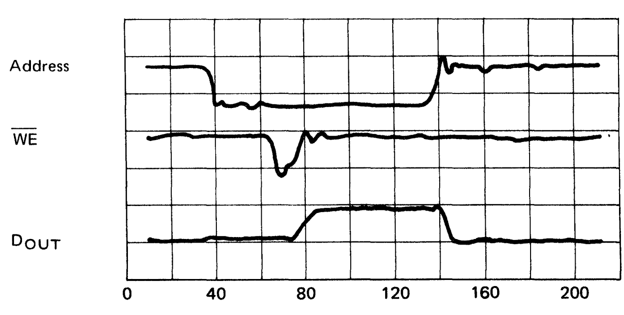


Fig. 10 — t_{WW} WRITE PULSE WIDTH vs V_{EE} SUPPLY VOLTAGE



TYPICAL TRANSIENT WAVEFORMS



Note: Vertical grid 1V per division.

FUNCTIONAL DESCRIPTION/APPLICATIONS INFORMATION

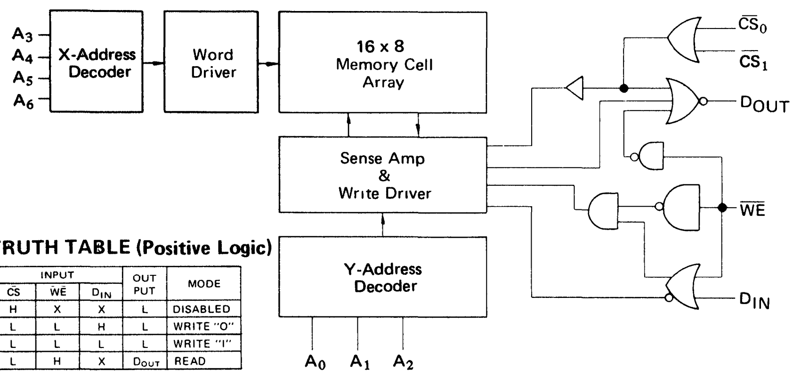
Functional Description

The Fujitsu MB 7047 is a fully decoded 128-bit read/write random access memory organized as 128 words by 1 bit. Memory cell selection is achieved by means of an 7-bit address designated $A_0 \sim A_6$. Two active low chip select ($\overline{CS}$) inputs are provided for increased logic flexibility, permitting memory array expansion up to 512 words without additional decoding. For larger memories, the fast chip select access time permits the decoding of $\overline{CS}$ from the address without affecting system performance.

Read and write operating modes (all $\overline{CS}$ inputs low) are controlled by the state of the active low write enable ($\overline{WE}$) input. With $\overline{WE}$ held low, the chip is in the write mode; in this condition, D_{OUT} is low and the data at D_{IN} is written into the addressed location. With $\overline{WE}$ held high, the chip is in the read mode; data in the addressed location is then transferred to D_{OUT} and read out non-inverted.

D_{OUT} is low except when reading out a stored high. Open emitter outputs are provided on the MB 7047 to allow maximum flexibility in output wired-OR connection for memory expansion.

Fig. 12 — MB 7047 BLOCK DIAGRAM
LOGIC DIAGRAM

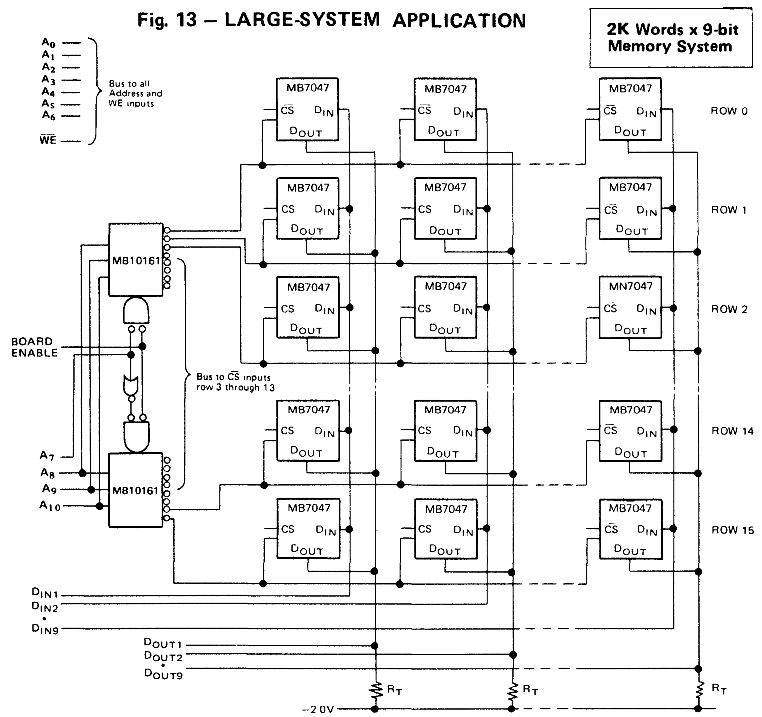


TRUTH TABLE (Positive Logic)

INPUT			OUT PUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "O"
L	L	L	L	WRITE "I"
L	H	X	D_{OUT}	READ

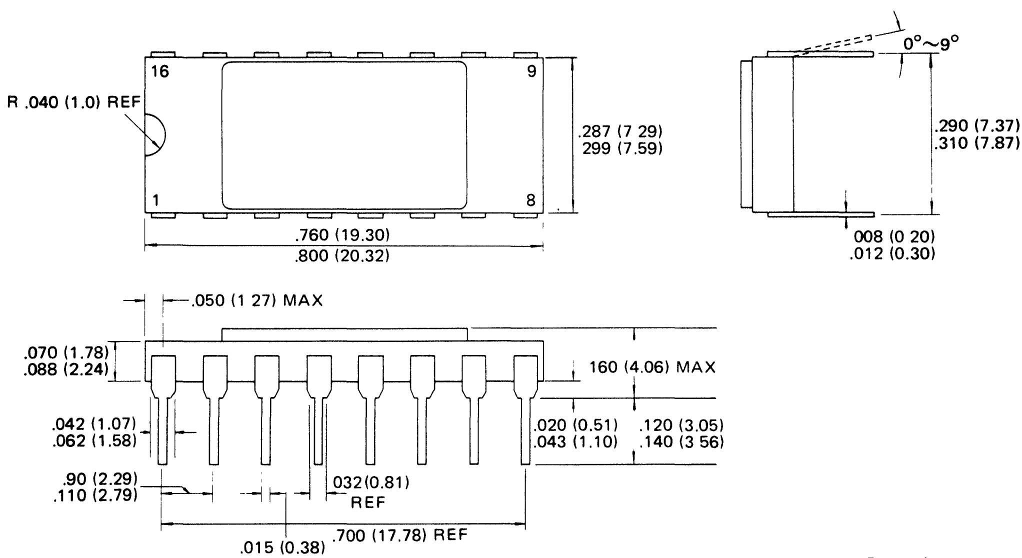
X = Don't Care

Fig. 13 — LARGE-SYSTEM APPLICATION



PACKAGE DIMENSIONS

16-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE DIP16-A)



Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information herein has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

ECL 256-BIT BIPOLAR RAM

FUJITSU

MB 7042

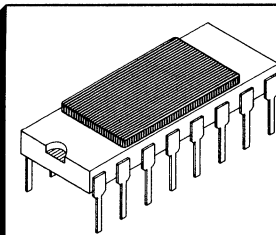
256-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MB 7042 is a fully decoded 256-bit read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 256 words by one bit, and it features on-chip voltage compensation for improved noise margin, three active low chip select lines for ease of memory expansion, and has a separate data in and non-inverting data out line.

The MB 7042 offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon) processing. With cell size reduced to approximately half that of normal, ultra-fast access time with high yields and outstanding device reliability are achieved in volume production.

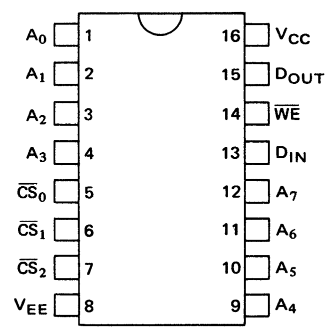
Operation for the MB 7042 is specified over a temperature range of from 0°C to 75°C (ambient). The device comes in a hermetically-sealed glass/ceramic dual-in-line package, and is compatible with industry-standard 10K-series ECL families.

- 256 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Patented DOPOS processing
- Outstanding read access time of 9 ns (typ.)
- Ultra-fast chip select time of 3.5 ns (typ.)
- Low power requirement (2 mW/bit dissipation)
- Multiple chip select leads for simplified memory expansion
- Pin compatible with the F10410, MCM10144/10152, and HM2106



CASE DIP16-A
CERAMIC PACKAGE

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	0.5 to V_{EE}	V
Output Current (DC Output High)	I_{OUT}	30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid appplication of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING RANGES

Part Number	Supply Voltage (V_{EE})			Ambient Temperature
	Min	Typ	Max	
MB 7042	−5.46V	−5.2V	−4.94V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V Output Load = 50Ω to −2.0V, Air Flow ≧2.5m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = V_{IHmax} or V_{ILmin})	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IHmax} or V_{ILmin})	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = V_{IHmin} or V_{ILmax})	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IHmin} or V_{ILmax})	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = V_{IHmax})	I_{IH}		10	50	μA	0° to 75°C
$\overline{CS}$ Input High Current (V_{IN} = V_{IHmax})	I_{IH}			220	μA	0° to 75°C
$\overline{WE}$ Input High Current (V_{IN} = V_{IHmax})	I_{IH}		30	150	μA	0° to 75°C
Input Low Current (V_{IN} = V_{ILmin})	I_{IL}	−50			μA	0° to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{ILmin})	I_{IL}	0.5		170	μA	0° to 75°C
Power Supply Current (All Inputs High and Output Open)	I_{EE}	60	100	145 140 130	mA	0°C 25°C 75°C

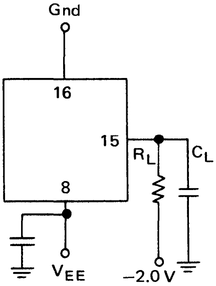
CAPACITANCE

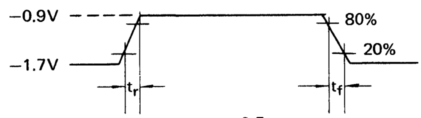
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Input Pin Capacitance	C_{IN}	—	4	5	pF	25°C
Output Pin Capacitance	C_{OUT}	—	7	8	pF	25°C

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V±5%, Output Load = 50Ω to −2V and 15pF to V_{CC}, Air Flow ≧2.5m/s, unless otherwise noted.)

Fig. 1 — AC TEST CONDITIONS



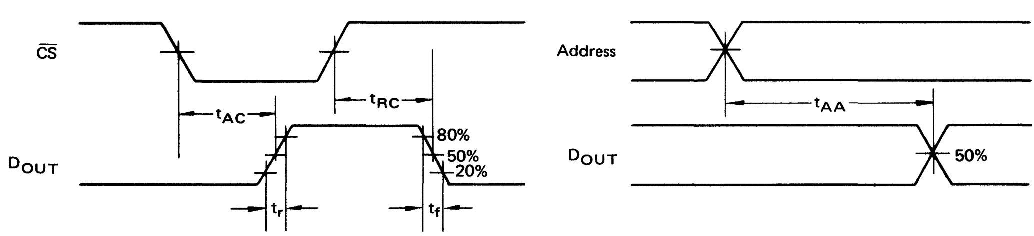


Output Load: R_L = 50Ω
C_L = 15pF
(Including Jig and Stray Capacitance)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Address Access Time	t_{AA}		9.0	13.0 15.0	ns	25°C 0 to 75°C
Chip Select Access Time and Recovery Time	t_{AC}, t_{RC}		3.5	8.0 9.0	ns	25°C 0 to 75°C

READ CYCLE TIMING DIAGRAMS



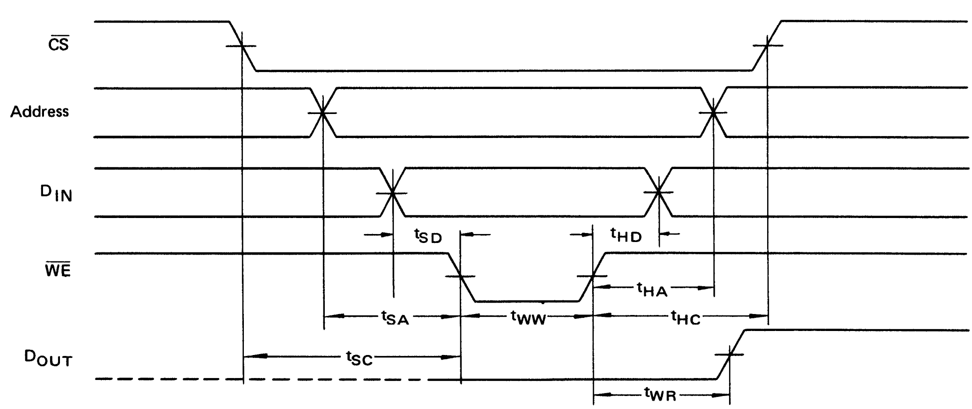
Bipolar Memories

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Write Pulse Width	t_{WW}*	8.0 9.0	4.5		ns	25°C 0° to 75°C
Write Recovery Time	t_{WR}**		5.5	9.0 10.0	ns	25°C 0° to 75°C
Address Set Up Time	t_{SA}**	4.0 4.0			ns	25°C 0° to 75°C
Chip Select Set Up Time	t_{SC}**	1.0 2.0			ns	25°C 0° to 75°C
Data Set Up Time	t_{SD}**	1.0 2.0			ns	25°C 0° to 75°C
Address Hold Time	t_{HA}**	3.0 3.0			ns	25°C 0° to 75°C
Chip Select Hold Time	t_{HC}**	1.0 1.0			ns	25°C 0° to 75°C
Data Hold Time	t_{HD}**	1.0 2.0			ns	25°C 0° to 75°C

*Note: t_{WW} measured at t_{SA} = 4.0ns
**Note: Values indicated measured at respective min values of t_{WW}.

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output Rise Time	t_r	—	1.2	—	ns	25°C
Output Fall Time	t_f	—	1.2	—	ns	25°C

TYPICAL CHARACTERISTICS CURVES

Fig. 2 – V_{OH} OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

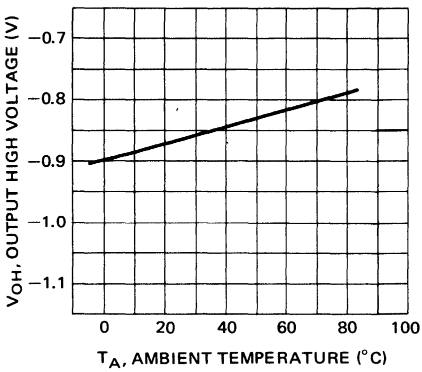


Fig. 3 – V_{OL} OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

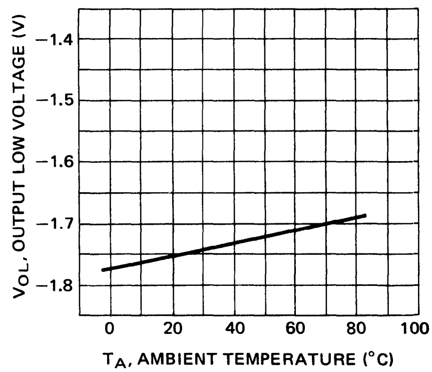


Fig. 4 – I_{EE} SUPPLY CURRENT vs AMBIENT TEMPERATURE

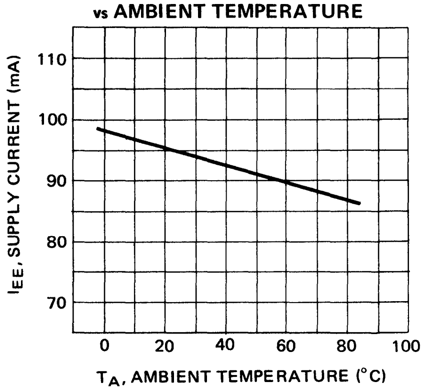


Fig. 5 – I_{EE} SUPPLY CURRENT vs V_{EE} SUPPLY VOLTAGE

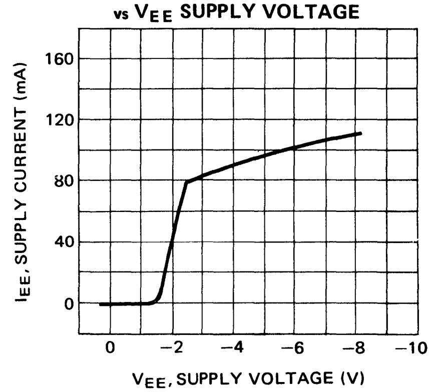


Fig. 6 – I_{IH} INPUT HIGH CURRENT vs AMBIENT TEMPERATURE

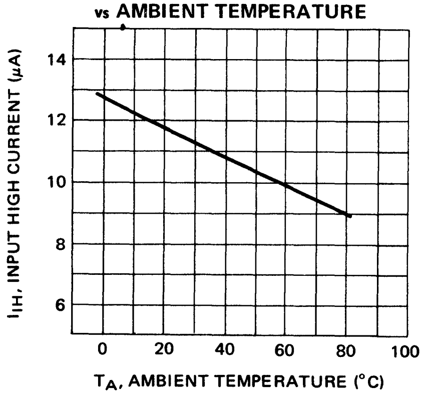
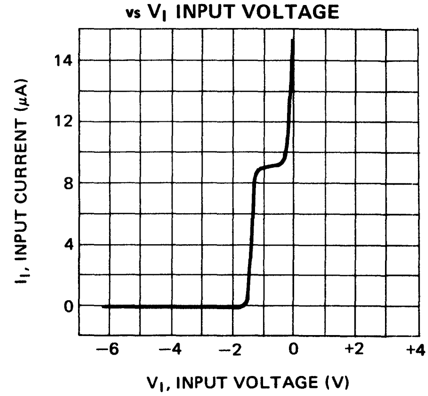


Fig. 7 – I_I INPUT CURRENT vs V_I INPUT VOLTAGE



Bipolar Memories

Fig. 8 — t_{AA} ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

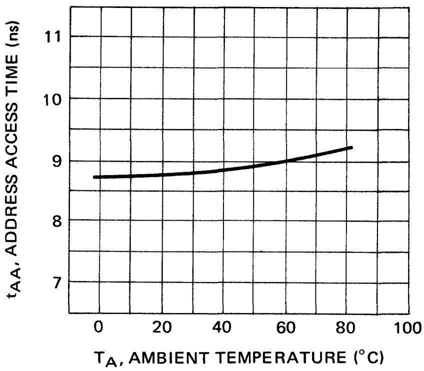


Fig. 9 — t_{AA} ADDRESS ACCESS TIME vs V_{EE} SUPPLY VOLTAGE

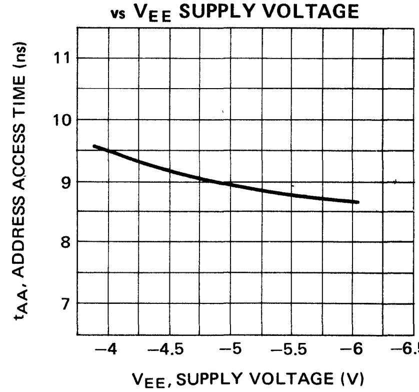


Fig. 10 — t_{WW} WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

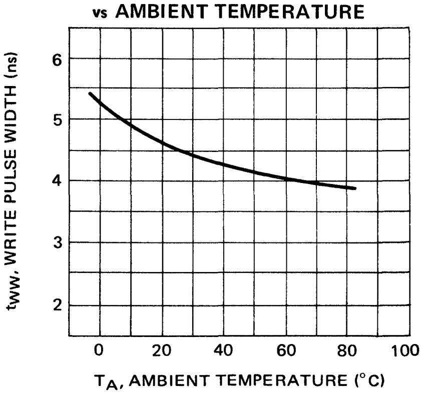
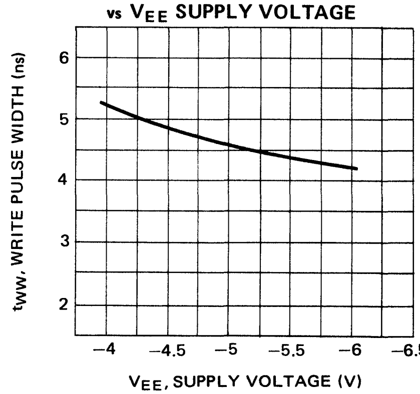
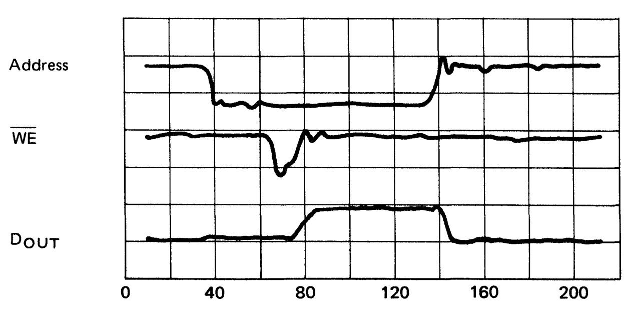


Fig. 11 — t_{WW} WRITE PULSE WIDTH, vs V_{EE} SUPPLY VOLTAGE



TYPICAL TRANSIENT WAVEFORMS



Note: Vertical grid 1V per division.

FUNCTIONAL DESCRIPTION/APPLICATIONS INFORMATION

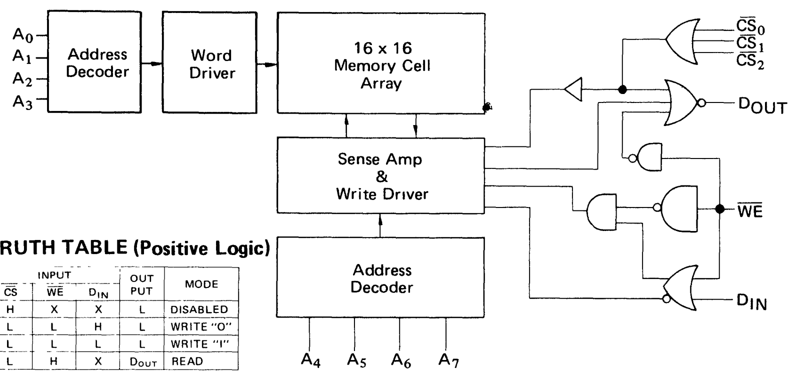
Functional Description

The Fujitsu MB 7042 is a fully decoded 256-bit read/write random access memory organized as 256 words by 1 bit. Memory cell selection is achieved by means of an 8-bit address designated $A_0 \sim A_7$. Three active low chip select ($\overline{CS}$) inputs are provided for increased logic flexibility, permitting memory array expansion up to 2048 words without additional decoding. For larger memories, the fast chip select access time permits the decoding of $\overline{CS}$ from the address without affecting system performance.

Read and write operating modes (all $\overline{CS}$ inputs low) are controlled by the state of the active low write enable ($\overline{WE}$) input. With $\overline{WE}$ held low, the chip is in the write mode; in this condition, D_{OUT} is low and the data at D_{IN} is written into the addressed location. With $\overline{WE}$ held high, the chip is in the read mode; data in the addressed location is then transferred to D_{OUT} and read out non-inverted.

D_{OUT} is low except when reading out a stored high. Open emitter outputs are provided on the MB 7042 to allow maximum flexibility in output wired-OR connection for memory expansion.

Fig. 12 — MB 7042 BLOCK DIAGRAM
LOGIC DIAGRAM



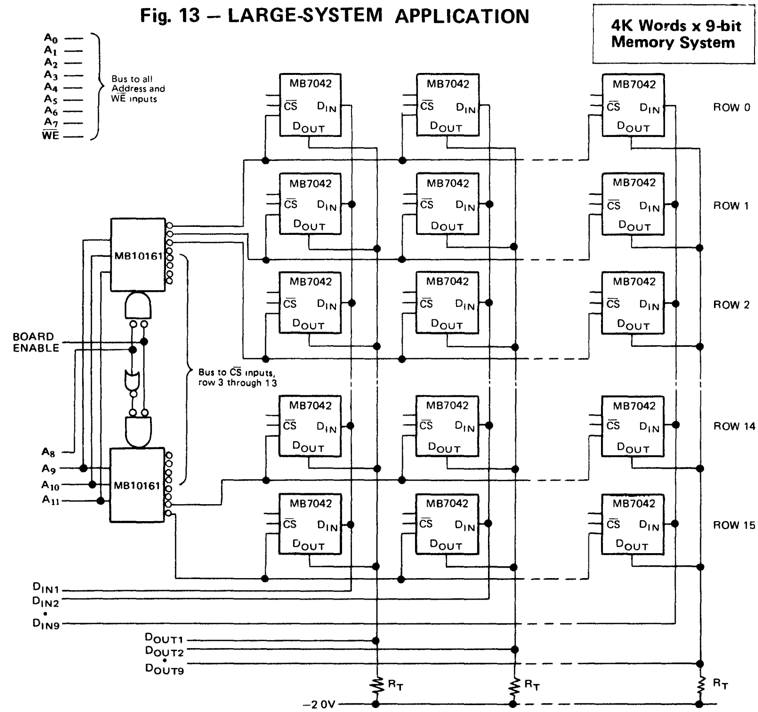
TRUTH TABLE (Positive Logic)

INPUT $\overline{CS}$	$\overline{WE}$	D_{IN}	OUT PUT	MODE
H	X	X	L	DISABLED
L	L	H	L	WRITE "O"
L	L	L	L	WRITE "I"
L	H	X	D_{OUT}	READ

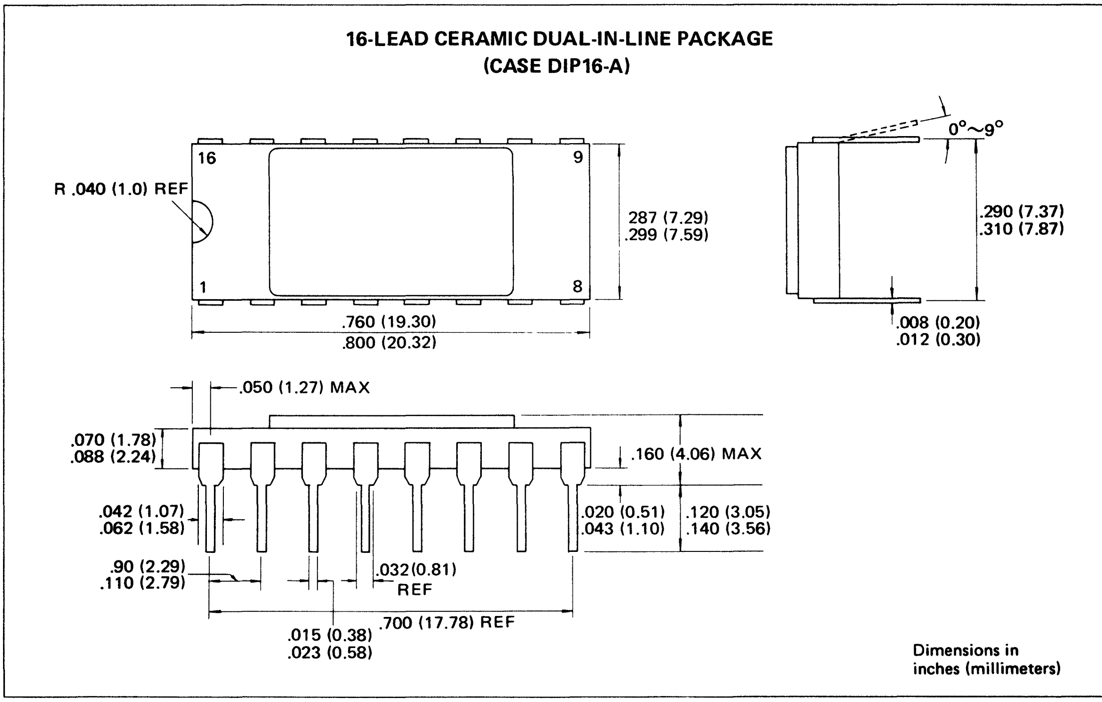
X = Don't Care

Fig. 13 — LARGE-SYSTEM APPLICATION

4K Words x 9-bit Memory System



PACKAGE DIMENSIONS



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FUJITSU

ECL 256-BIT READ/WRITE RANDOM ACCESS MEMORY

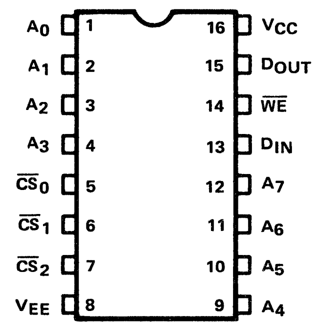
MBM 10410

256-BIT RANDOM ACCESS MEMORY

The MBM 10410 is an ECL 256-Bit Read/Write Random Access Memory (RAM), organized 256 words x 1 bit. It has a typical access time of 20 ns and is compatible with the MB10K Logic family. It is designed for high-speed scratch pad and buffer storage applications.

- Read access time, 20 ns typ.
- Chip select access time, 7 ns typ.
- Power dissipation, 1.8 mW/bit
- Simple memory expansion (3 chip selects)
- Output can be wired-OR for easy memory expansion
- Standard 16-lead DIP

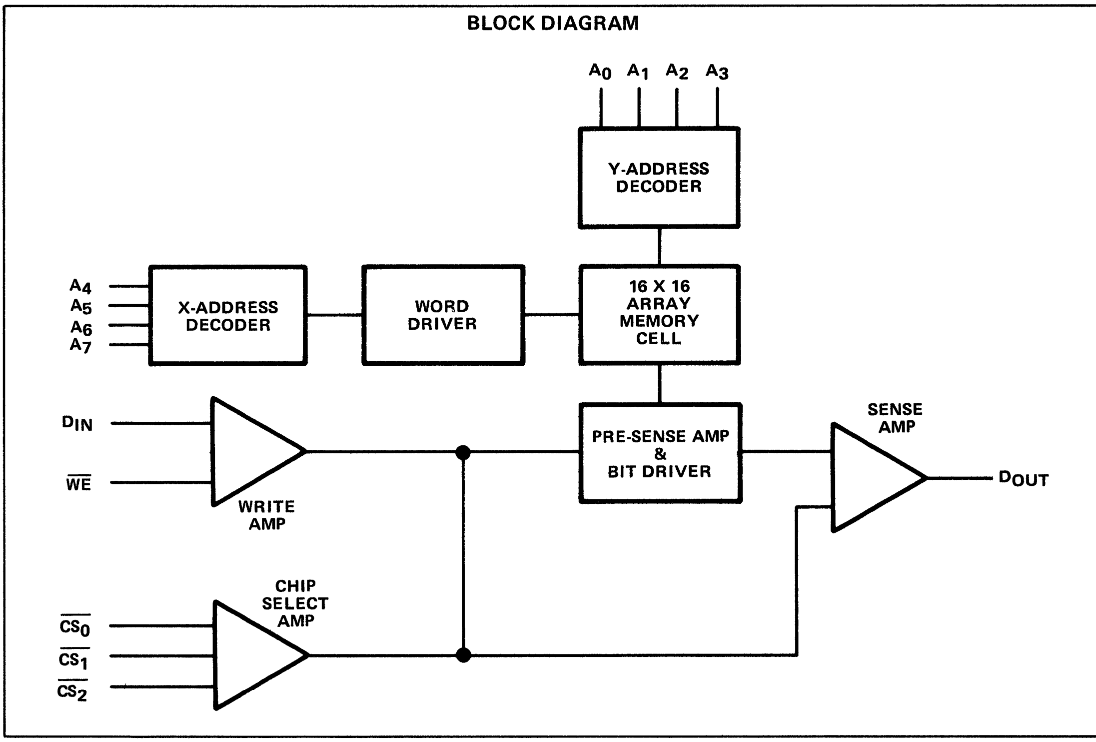
PIN CONFIGURATION



DIP
(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Storage Temperature	T_{stg}	–55 to +150	°C
V_{EE} Pin Potential to Ground Pin	V_{EE}	0 to –7	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC Output High)	I_{OUT}	30	mA



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	*	*	L	Inhibit
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	*	D_{OUT}	Read

Notes:
H = High Voltage Level
L = Low Voltage Level
* = Don't Care (H or L)

GUARANTEED OPERATING RANGES

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{EE}	–5.2 ± 5%	V
Ambient Temperature	T_A	0 to +75	°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V, R_L = 50Ω to −2.0V, AIRFLOW ≥ 2.5 m/s)

Characteristics	Symbol	Pin Under Test	Limits T_A = 0°C Min.	T_A = 0°C Max.	T_A = 25°C Min.	T_A = 25°C Typ.	T_A = 25°C Max.	T_A = 75°C Min.	T_A = 75°C Max.	Unit	Notes
Power Supply Current	I_{EE}	8		130		80			120	mA	
Input High Current	I_{IH}	1-4, 9-12, 13, 14		100		50	100		100	μA	
		5-7		150		100	150		150		
Input Low Current	I_{IL}	5-7	0.5	150	0.5	100	150	0.5	150		
Output High Voltage	V_{OH}	15	−1.00	−0.84	−0.96		−0.81	−0.90	−0.72	V	
Output Low Voltage	V_{OL}	15	−1.87	−1.665	−1.85		−1.65	−1.83	−1.625	V	
Output Threshold High Voltage	V_{OHA}	15	−1.02		−0.98			−0.92		V	$\overline{CS} = V_{ILA}$
Output Threshold Low Voltage	V_{OLA}	15		−1.645			−1.63		−1.605	V	$\overline{CS} = V_{IHA}$ or $\overline{WE} = V_{ILA}$
Input Voltage	V_{IH}			−0.84			−0.81		−0.72	V	
	V_{IL}		−1.87		−1.85			−1.83		V	
	V_{IHA}		−1.145		−1.105			−1.045		V	
	V_{ILA}			−1.49			−1.475		−1.45	V	

Bipolar Memories

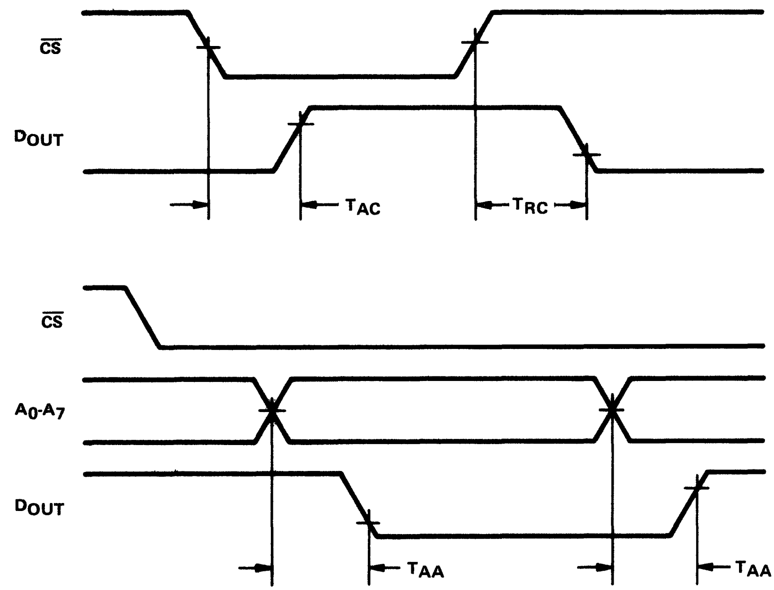
SWITCHING CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V ± 5%, R_L = 50Ω to −2.0V, AIRFLOW ⩾ 2.5 m/s)

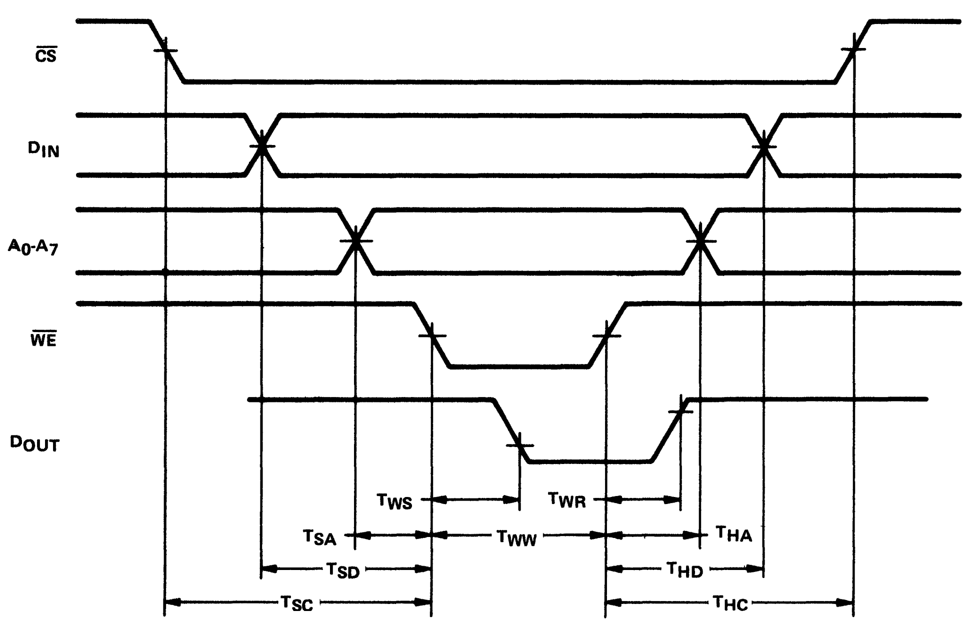
Characteristics	Symbol	T_A = 25°C			T_A = 0-75°C		Unit	Notes
		Min.	Typ.	Max.	Min.	Max.		
READ MODE								
Chip Select Access Time	T_{AC}		7	10		12	ns	
Chip Select Recovery Time	T_{RC}		7	10		12	ns	
Address Access Time	T_{AA}		20	25		35	ns	
WRITE MODE								
Minimum Write Pulse Width	T_{WW}	20			25		ns	
Write Disable Time	T_{WS}			10		12	ns	
Write Recovery Time	T_{WR}			20		20	ns	
WRITE MODE CONDITION								T_{WW} = 20 ns (25°C) = 25 ns (0-75°C)
Chip Select Set-Up Time	T_{SC}	5			5		ns	
Address Set-Up Time	T_{SA}	8			8		ns	
Data Set-Up Time	T_{SD}	5			5		ns	
Chip Select Hold Time	T_{HC}	5			5		ns	
Address Hold Time	T_{HA}	2			2		ns	
Data Hold Time	T_{HD}	5			5		ns	
Output Rise/Fall Time	t_r/t_f		2.5			3.0	ns	20-80%
Pin-Capacitance Input	C_I						pF	
Pin-Capacitance Output	C_O						pF	

TIMING CHART

READ MODE

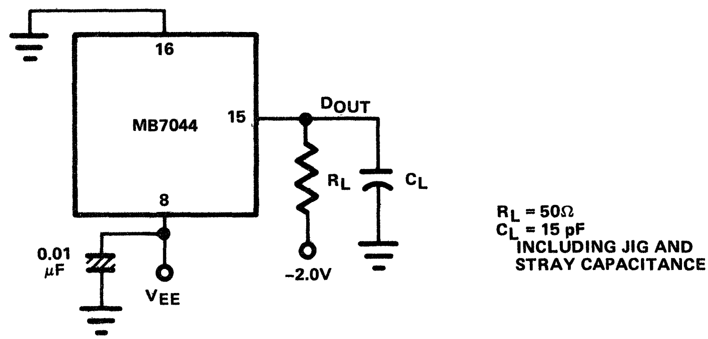


WRITE MODE

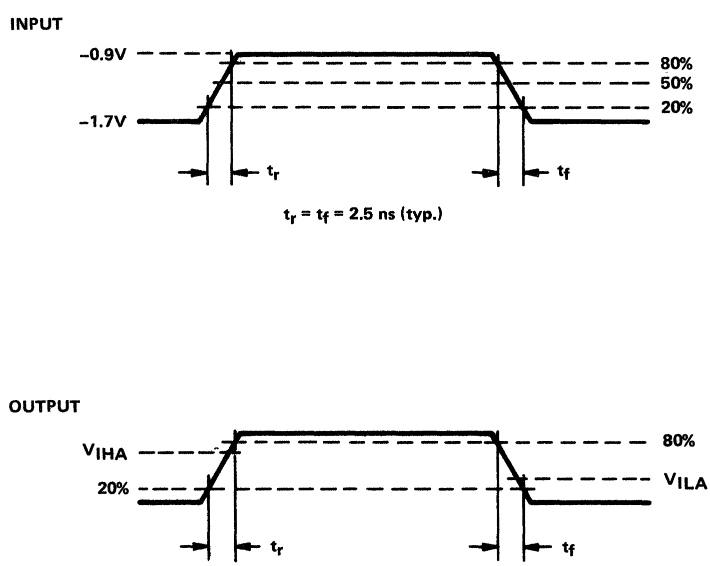


SWITCHING TIME CONDITIONS

LOADING



INPUT AND OUTPUT



FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10415
MBM 10415A

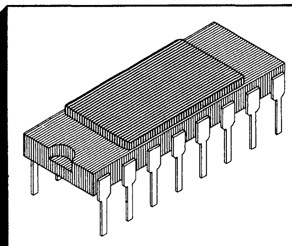
1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10415 and MBM 10415A are fully decoded 1024-bit ECL read/write random access memories designed for high-speed scratch pad, control and buffer storage applications. Both devices are organized as 1024 words by one bit, and they feature on-chip voltage compensation for improved noise margin.

The MBM 10415/MBM 10415A offer extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon), processing. ~~As a~~ result ~~very~~ fast
As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

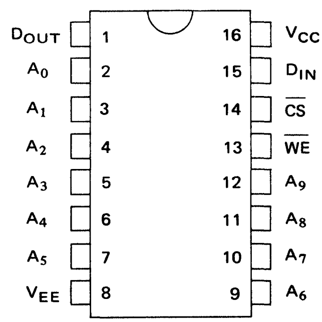
Operation for the MBM 10145/MBM 10145A is specified over a temperature range of from 0° to 75°C (ambient). They also feature frit-sealed 16-pin dual-in-line packaging, and are fully compatible with industry-standard 10K-series ECL families.

- 1024 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time:
  35 ns typ. (MBM 10415)
  25 ns typ. (MBM 10415A)
- Chip select access time:
  15 ns typ. (MBM 10415)
  7 ns typ. (MBM 10415A)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.5 mW/bit
- DOPOS and IOP processing
- Pin compatible with the F10415/A and HM2110



CASE DIP16-A
CERAMIC PACKAGE

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC Output High)	I_{OUT}	30	mA
Temperature Under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{stg}	-65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING RANGES

Part Number	Supply Voltage (V_{EE})			Ambient Temperature
	Min	Typ	Max	
MBM 10415, MBM 10415A	−5.46V	−5.2V	−4.94V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω to −2.0V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IHmax}$ or V_{ILmin})	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IHmax}$ or V_{ILmin})	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IHmin}$ or V_{ILmax})	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IHmin}$ or V_{ILmax})	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IHmax}$)	I_{IH}			220	μA	0°to 75°C
Input Low Current ($V_{IN} = V_{ILmin}$)	I_{IL}	−50			μA	0°to 75°C
$\overline{CS}$ Input Low Current ($V_{IN} = V_{ILmin}$)	I_{IL}	0.5		170	μA	0°to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}		90 105	 150	mA	75°C 0°C

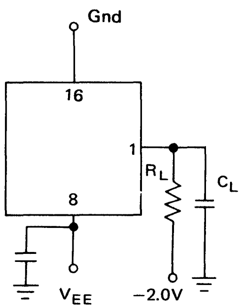
CAPACITANCE

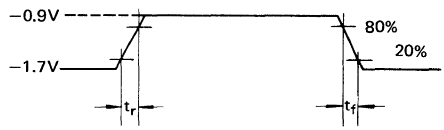
Parameter	Symbol	MBM 10415			MBM 10415A			Unit
		Min	Typ	Max	Min	Typ.	Max	
Input Pin Capacitance	C_{IN}	—	4	5	—	4	5	pF
Output Pin Capacitance	C_{OUT}	—	7	8	—	7	8	pF

AC CHARACTERISTICS

(V_{CC}=0V, V_{EE}=−5.2V±5%, T_A=0° to 75°C, Output Load =50Ω to −2V and 30pF to V_{CC}, unless otherwise noted.)

Fig. 1 — AC TEST CONDITIONS





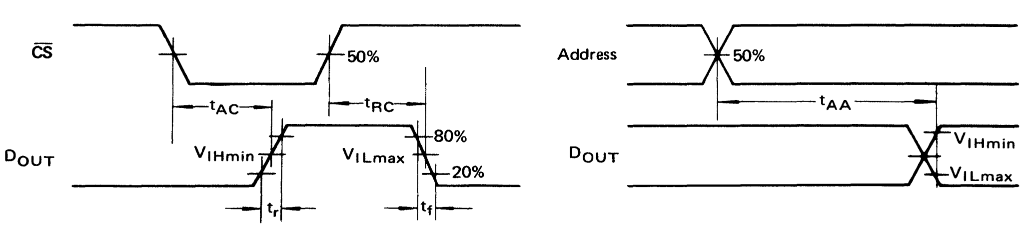
t_r=t_f=2.5ns typ

Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

READ CYCLE

Parameter	Symbol	MBM 10415			MBM 10415A			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	—	35	60	—	25	35	ns
Chip Select Access Time	t_{AC}	—	15	30	—	7	10	ns
Chip Select Recovery Time	t_{RC}	—	20	35	—	7	10	ns

READ CYCLE TIMING DIAGRAMS

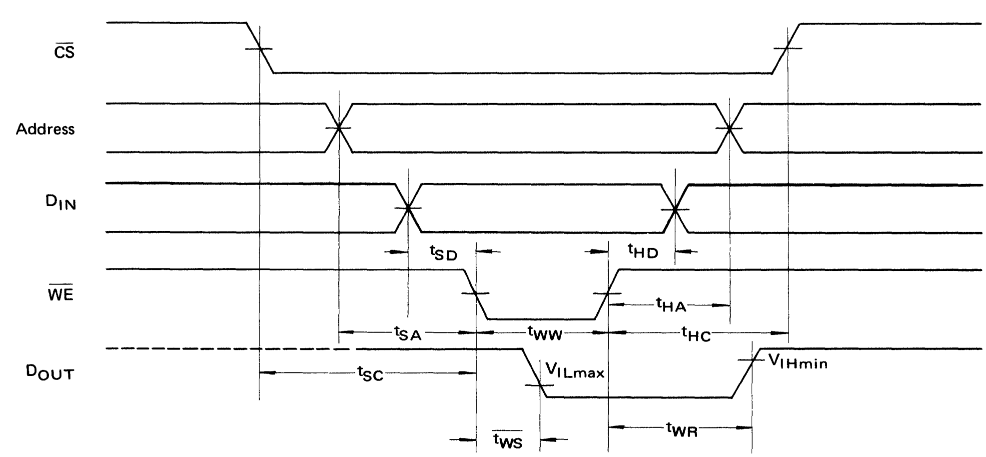


WRITE CYCLE

Parameter	Symbol	MBM 10415			MBM 10415A			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}*	35	25	—	25	20	—	ns
Write Recovery Time	t_{WR}**	30	20	—	10	7	—	ns
Write Disable Time	t_{WS}**	30	20	—	10	7	—	ns
Address Set Up Time	t_{SA}**	20	15	—	8	5	—	ns
Chip Select Set Up Time	t_{SC}**	5	0	—	5	0	—	ns
Data Set Up Time	t_{SD}**	5	0	—	5	0	—	ns
Address Hold Time	t_{HA}**	5	1	—	4	1	—	ns
Chip Select Hold Time	t_{HC}**	5	0	—	5	0	—	ns
Data Hold Time	t_{HD}**	5	0	—	5	0	—	ns

*Note: For MBM 10415, t_{SA} = 20ns; for MBM 10415A, t_{SA} = 8ns.
**Note: For MBM 10415, t_{WW}=35ns; for MBM 10415A, t_{WW}=25ns.

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	MBM 10415			MBM 10415A			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Rise Time	t_r	—	5	—	—	5	—	ns
Output Fall Time	t_f	—	5	—	—	5	—	ns

TYPICAL CHARACTERISTICS CURVES

Fig. 2 — I_{EE} SUPPLY CURRENT vs AMBIENT TEMPERATURE

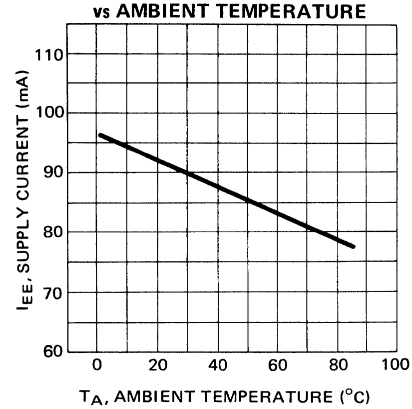


Fig. 3 — V_{OH} OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

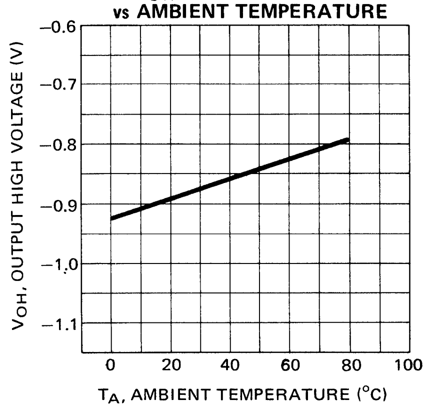


Fig. 4 — V_{OL} OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

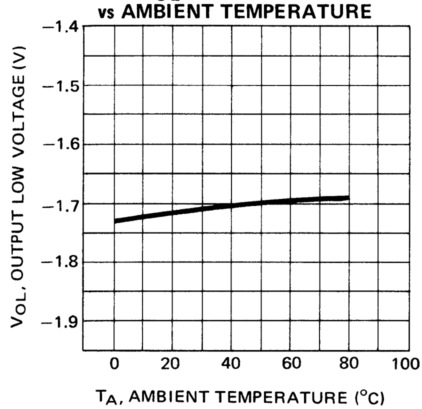


Fig. 5 — I_{EE} SUPPLY CURRENT vs V_{EE} SUPPLY VOLTAGE

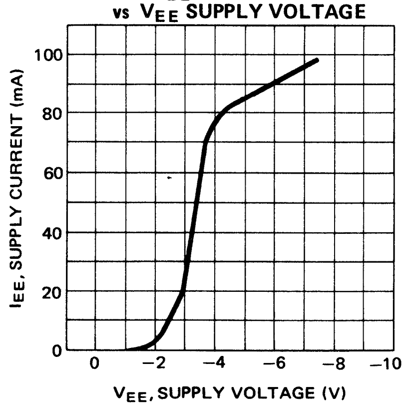
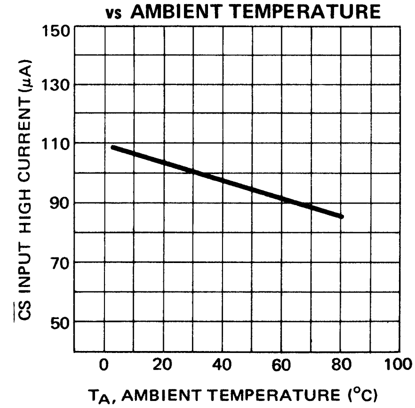


Fig. 6 — $\overline{CS}$ INPUT HIGH CURRENT vs AMBIENT TEMPERATURE



Bipolar Memories

Fig. 7 — t_{AA} ADDRESS ACCESS TIME vs V_{EE} SUPPLY VOLTAGE

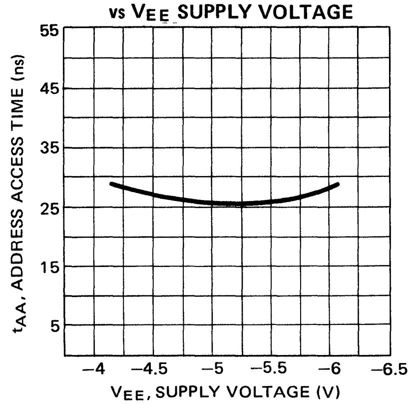


Fig. 8 — t_{WW} WRITE PULSE WIDTH vs V_{EE} SUPPLY VOLTAGE

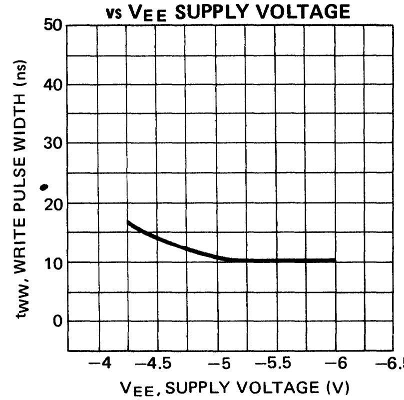


Fig. 9 — t_{AC} CHIP SELECT ACCESS TIME vs AMBIENT TEMPERATURE

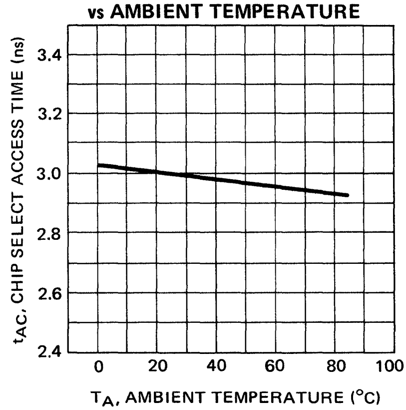


Fig. 10 — t_{AA} ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

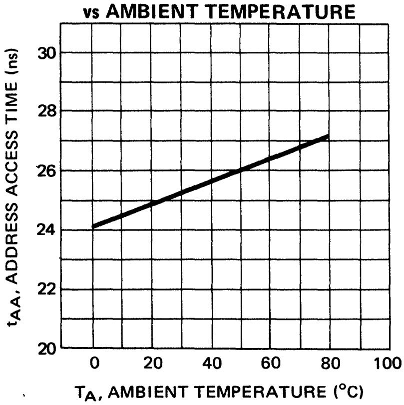
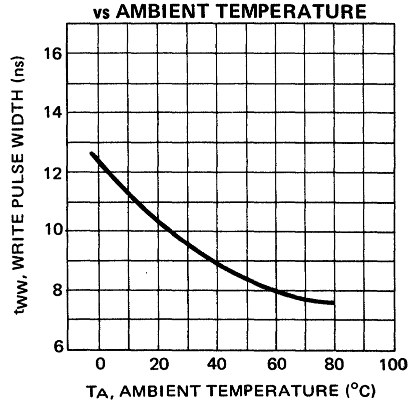


Fig. 11 — t_{WW} WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

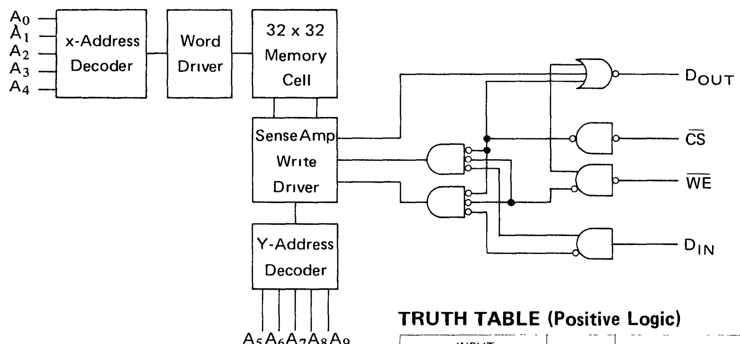


FUNCTIONAL DESCRIPTION/APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10415 and MBM 10415A are fully decoded 1024-bit read/write random access memories organized as 1024 words by one bit. Memory cell selection is achieved by means of a 10-bit address designated $A_0 \sim A_9$. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transfered to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Fig. 12 – MBM 10415/A BLOCK DIAGRAM



TRUTH TABLE (Positive Logic)

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

X = Don't care

Fig. 13 – LARGE-SYSTEM APPLICATION

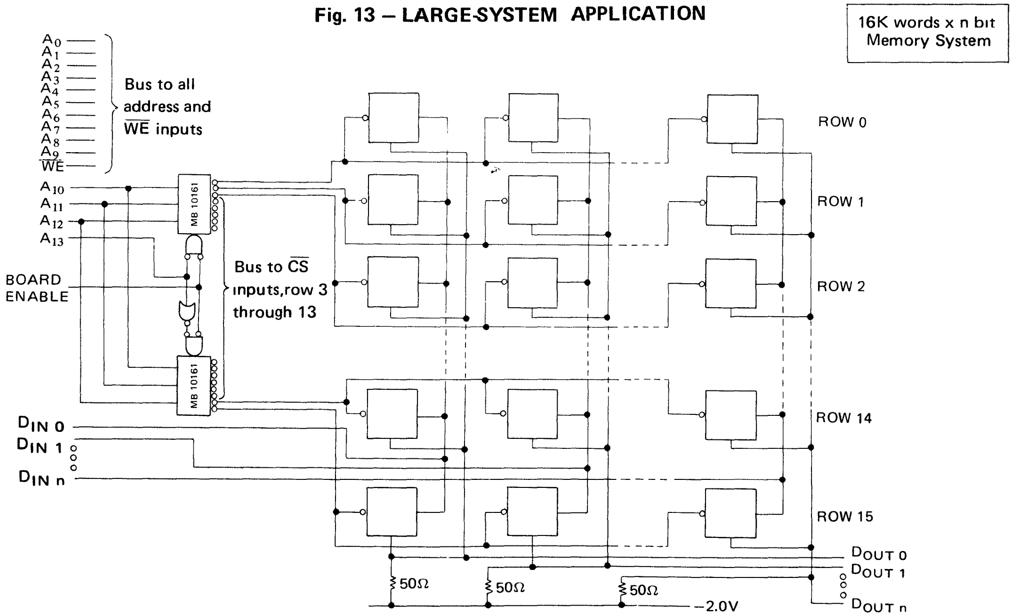
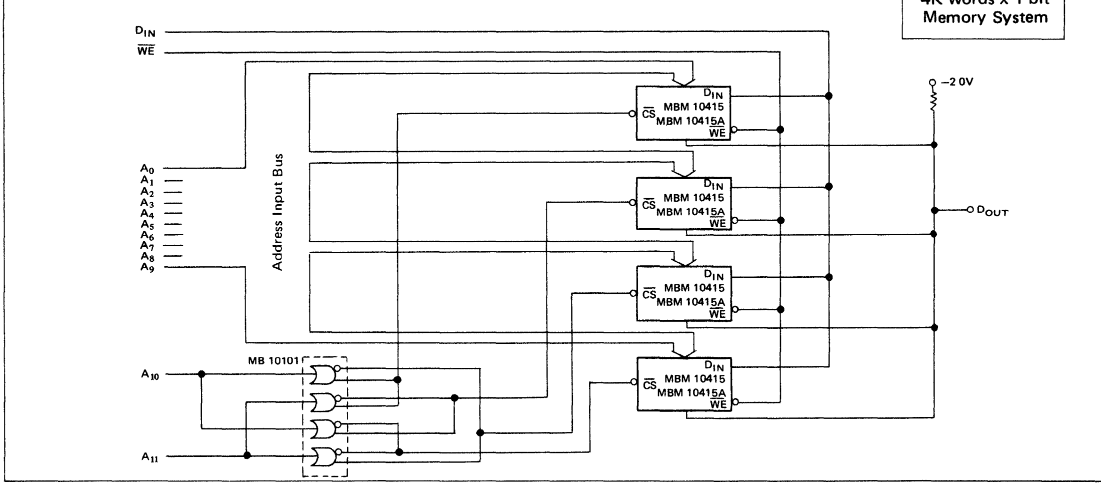
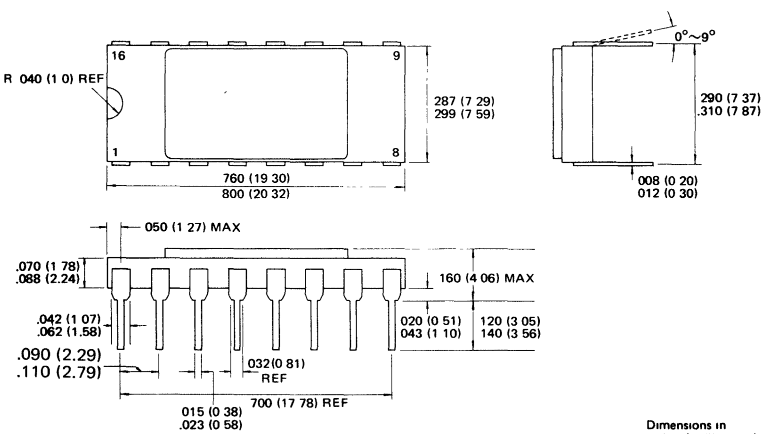


Fig. 14 – SMALL-SYSTEM APPLICATION



PACKAGE DIMENSIONS

16-LEAD CERAMIC DUAL-IN-LINE PACKAGE (CASE DIP16-A)



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information herein has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

TTL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

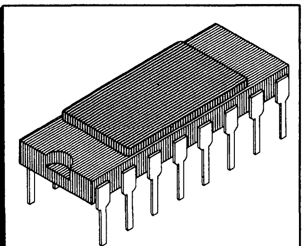
MBM 93415
MBM 93415A

1024-BIT BIPOLAR TTL RANDOM ACCESS MEMORY

The Fujitsu MBM 93415 and MBM 93415A are fully decoded 1024-bit TTL read/write random access memories for buffer control storage and high performance main memory applications. Both devices are organized as 1024-words by one bit, and they feature on-chip voltage compensation for improved noise margin.

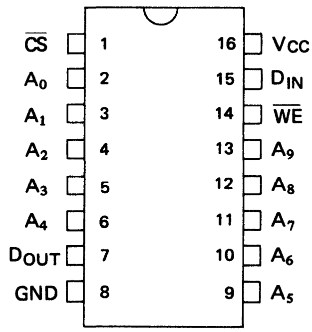
The MBM 93415/MBM 93415A have extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

- 1024 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with standard DTL and TTL families
- Address access time:
  40 ns typ.(MBM 93415)
  30 ns typ (MBM 93415A)
- Chip select access time: 15 ns typ. (both types)
- Open collector output
- Low power dissipation of 0.4mW/bit typ
- DOPOS and IOP processing
- Interchangeable with F93415/93415A



CASE DIP 16-A
CERAMIC PACKAGE

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to Ground Pin	V_{CC}	-0.5 to +7.0	V
Input Voltage (DC)*	V_{IN}	-0.5 to +5.5	V
Input Current (DC)*	I_{IN}	- 12 to +5.0	mA
Voltage Applied to Output (Output High)	V_{OUT}	-0.5 to +5.5	V
Output Current (DC, Output Low)	I_{OUT}	+20	mA
Temperature Under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{stg}	-65 to +150	°C

*Either input voltage or input current limit is sufficient to protect the input.

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING RANGES

Part Number	Supply Voltage (V_{CC})			Ambient Temperature
	Min	Typ	Max	
MBM 93415, MBM 93415A	4.75 V	5.0 V	5.25 V	0°C to 75°C

DC CHARACTERISTICS

(Guaranteed operating range unless otherwise noted, Airflow = 2.5m/s, after two minute warm-up.)

Parameter	Symbol	Min	Typ	Max	Unit
Output Low Voltage (V_{CC} = Min, I_{OL} = 16mA)	V_{OL}	–	0.3	0.45	V
Input High Voltage (guaranteed input high voltage for all inputs)	V_{IH}	2.1	1.6	–	V
Input Low Voltage (guaranteed input low voltage for all inputs)	V_{IL}	–	1.5	0.8	V
Input Low Current (V_{CC} = Max, V_{IN} = 0.4V)	I_{IL}	–	–250	–400	μA
Input High Current (V_{CC} = Max, V_{IN} = 4.5V)	I_{IH1}	–	1.0	40	μA
Input High Current (V_{CC} = Max, V_{IN} = 5.25V)	I_{IH2}	–	–	1.0	mA
Output Leakage Current (V_{CC} = Max, V_{OUT} = 4.5V)	I_{CEX}	–	1.0	100	μA
Input Diode Clamp Voltage (V_{CC} = Max, I_{IN} = –10mA)	V_{CD}	–	–1.0	–1.5	V
Power Supply Current (V_{CC} = Max, all inputs grounded)	I_{CC}	–	95	155*	mA
		–		130**	mA

***Note:** T_A = 0°C to 25°C ****Note:** T_A = 25°C to 75°C

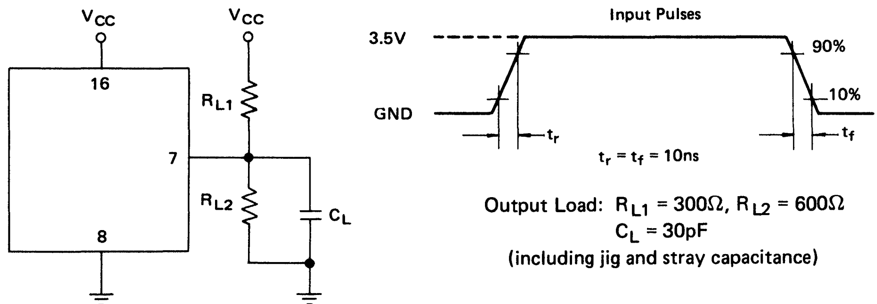
CAPACITANCE

Parameter	Symbol	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	4	5	pF
Output Pin Capacitance	C_{OUT}	7	8	pF

AC CHARACTERISTICS

(Guaranteed operating range unless otherwise noted, Airflow = 2.5m/s, after two minute warm-up.)

Fig. 1 — AC TEST CONDITIONS

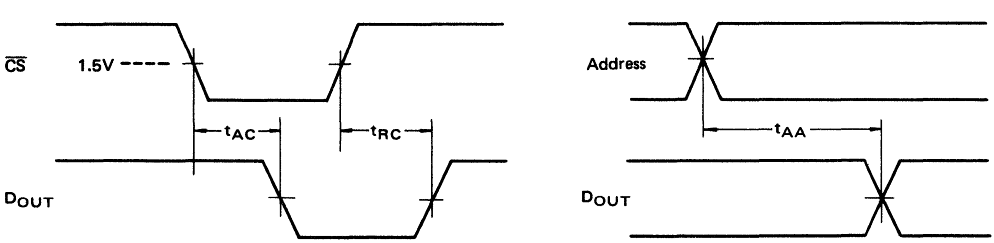


Output Load: $R_{L1} = 300\Omega$, $R_{L2} = 600\Omega$
$C_L = 30pF$
(including jig and stray capacitance)

READ CYCLE

Parameter	Symbol	MBM 93415			MBM 93415A			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	–	40	70	–	30	45	ns
Chip Select Access Time	t_{AC}	–	15	40	–	15	30	ns
Chip Select Recovery Time	t_{RC}	–	20	40	–	15	30	ns

READ CYCLE TIMING DIAGRAMS



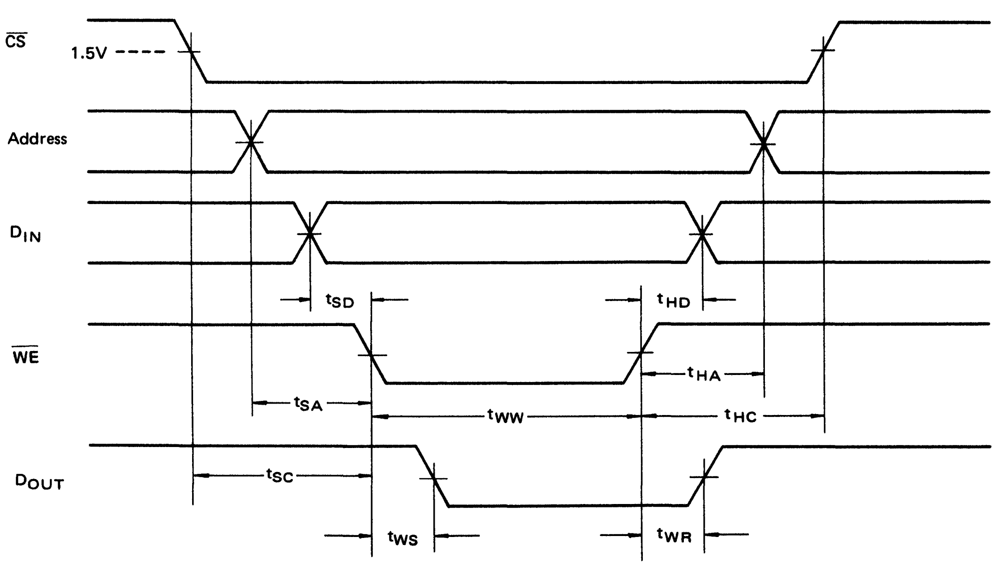
NOTE: All time measurements referenced to 1.5V.

WRITE CYCLE

Parameter	Symbol	MBM 93415			MBM 93415A			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}*	50	25	–	35	25	–	ns
Write Recovery Time	t_{WR}**	–	25	50	–	20	40	ns
Write Disable Time	t_{WS}**	–	20	40	–	20	30	ns
Address Set Up Time	t_{SA}**	15	0	–	5	0	–	ns
Chip Select Set Up Time	t_{SC}**	5	0	–	5	0	–	ns
Data Set Up Time	t_{SD}**	5	0	–	5	0	–	ns
Address Hold Time	t_{HA}**	5	0	–	5	0	–	ns
Chip Select Hold Time	t_{HC}**	5	0	–	5	0	–	ns
Data Hold Time	t_{HD}**	5	0	–	5	0	–	ns

***Note:** For MBM 93415, t_{SA}=15ns; for MBM 93415A, t_{SA}=5ns.
****Note:** For MBM 93415, t_{WW}=50ns; for MBM 93415A, t_{WW}=35ns.

WRITE CYCLE TIMING DIAGRAM



NOTE: All time measurements referenced to 1.5V.

TYPICAL CHARACTERISTICS CURVES

Fig. 2 — I_{CC} SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

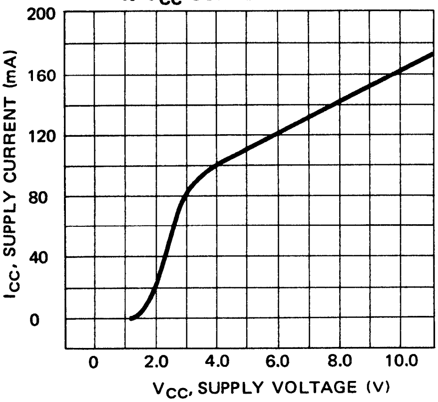


Fig. 3 — I_{CC} SUPPLY CURRENT vs AMBIENT TEMPERATURE

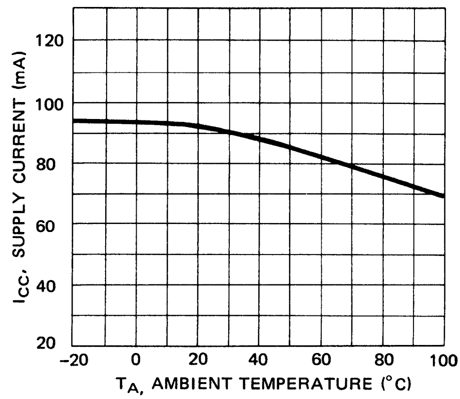


Fig. 4 — I_{OUT} OUTPUT CURRENT vs V_{OUT} OUTPUT VOLTAGE (LOW STATE)

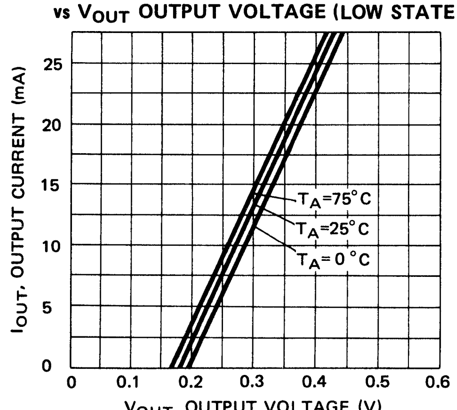


Fig. 5 — I_{OUT} OUTPUT CURRENT vs V_{OUT} OUTPUT VOLTAGE (HIGH STATE)

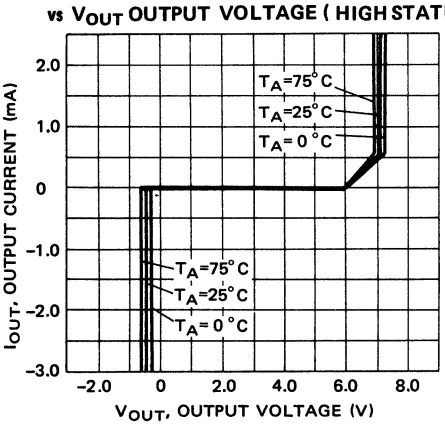
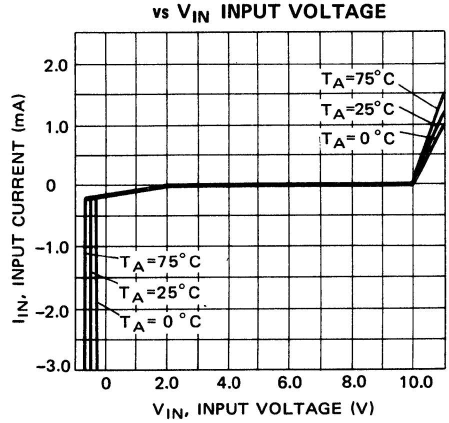


Fig. 6 — I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



Bipolar Memories

Fig. 7 – t_{AA} ADDRESS ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

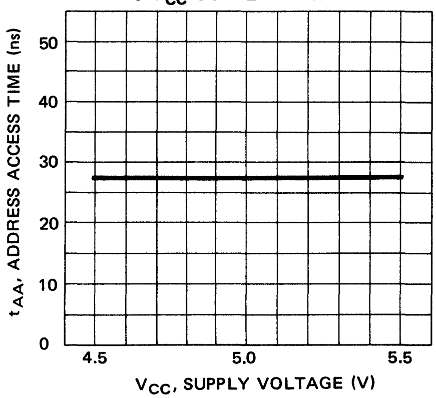


Fig. 8 – t_{AA} ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

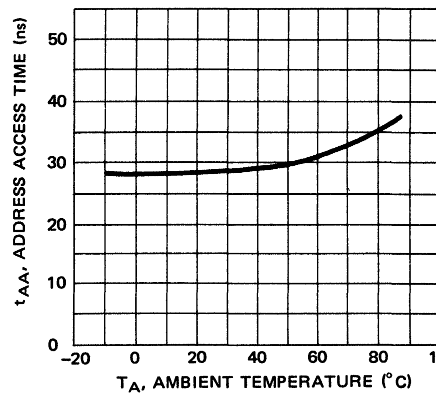


Fig. 9 – t_{WW} WRITE PULSE WIDTH vs V_{CC} SUPPLY VOLTAGE

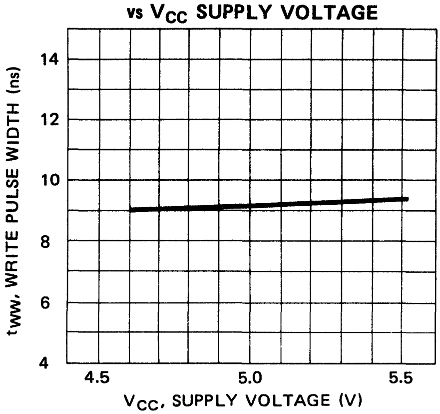
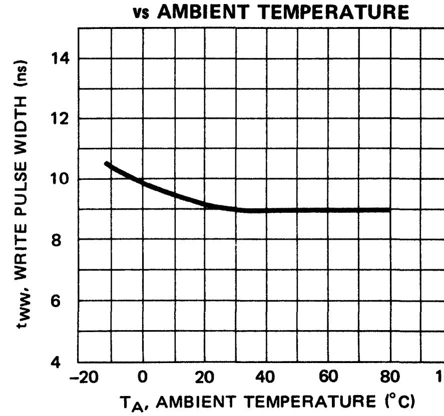
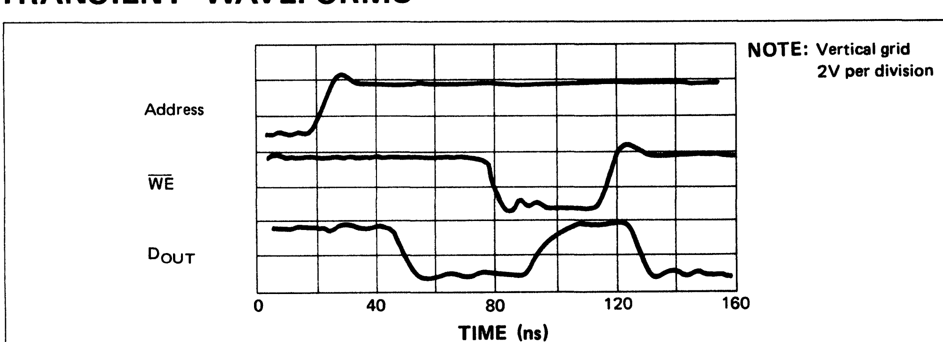


Fig. 10 – t_{WW} WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



TYPICAL TRANSIENT WAVEFORMS

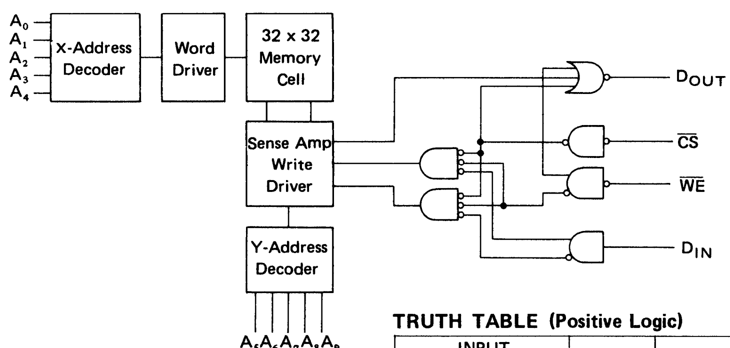


FUNCTIONAL DESCRIPTION/APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 93415 and MBM 93415A are fully decoded 1024-bit read/write random access memories organized as 1024 words by one bit. Memory cell selection is achieved by means of a 10-bit address designated $A_0 \sim A_9$. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transfered to D_{OUT} and read out non-inverted. Open collector outputs are provided to allow for maximum flexibility in output wired-OR connection.

Fig. 11 — MBM 93415/A BLOCK DIAGRAM



TRUTH TABLE (Positive Logic)

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	H	DISABLED
L	L	L	H	WRITE "L"
L	L	H	H	WRITE "H"
L	H	X	D_{OUT}	READ

X = Don't care

Fig. 12 — LARGE-SYSTEM APPLICATION

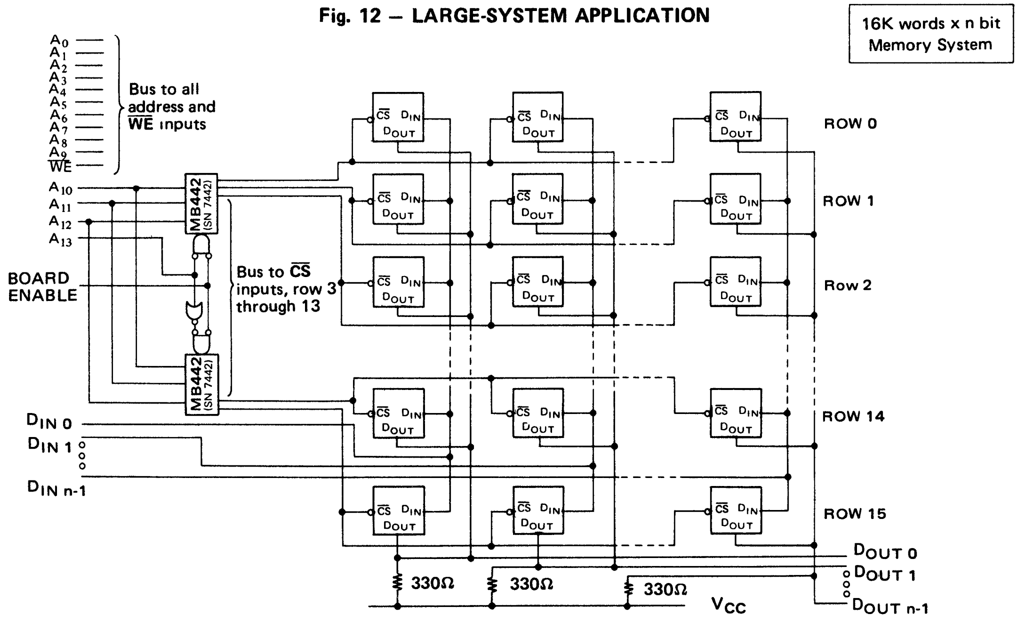
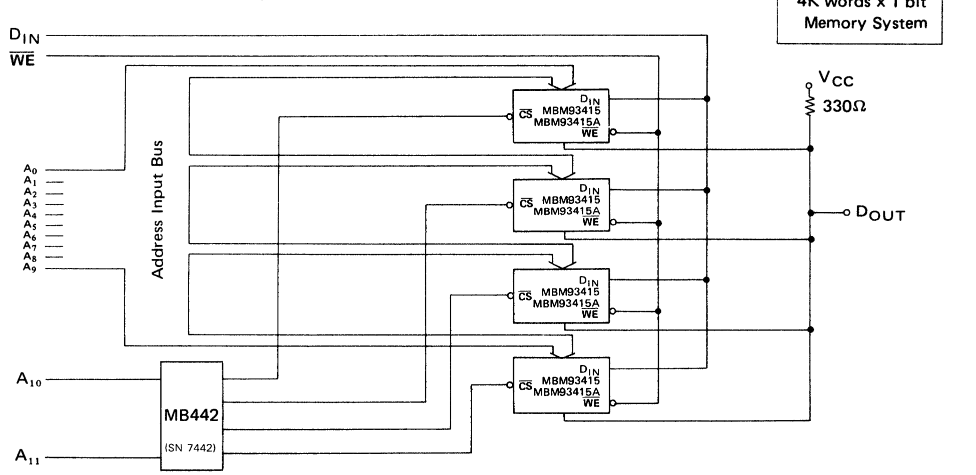
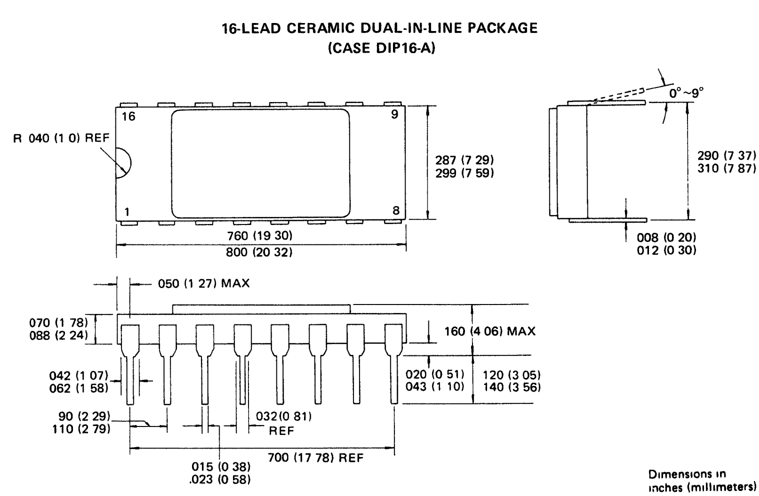


Fig. 13 — SMALL-SYSTEM APPLICATION



PACKAGE DIMENSIONS



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information herein has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

FULLY DECODED 1024-BIT ECL READ/WRITE RAM

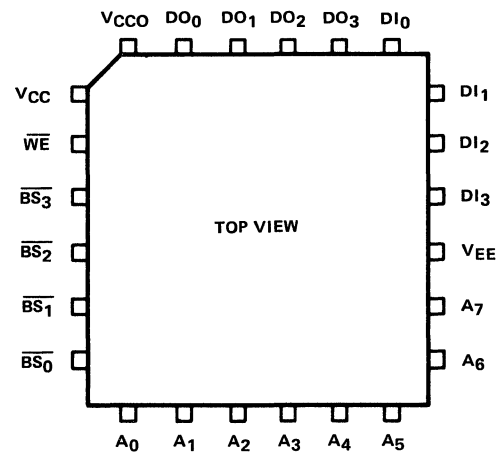
MB 7071N/H
MB 7072 N

1024-BIT ECL READ/WRITE RANDOM ACCESS MEMORY

The MB7071 and MB7072 devices are fully decoded 1024 bits ECL read/write random access memories designed for high speed scratch pad, control, and buffer storage applications. The MB7071 has maximum access times of 10 ns (H version) and 15 ns (N version), while the MB7072 has maximum access time of 15 ns. Normal organization is 256 x 4, but organizations of 512 x 2 and 1024 x 1 are made possible by utilizing the block select feature. The MB7071 is available in our 24-pin QIT package, while the MB7072 is available in our standard 22-pin DIP.

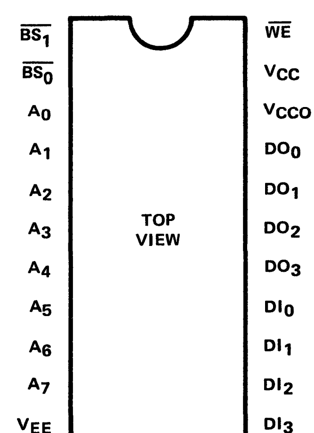
- 256 words x 4 bits organization
- Fully compatible with 10K-series ECL families
- Address access time: 10 ns (max.)
- Low power dissipation of 0.8 mW/bit
- Operating temperature: 0°C to +75°C (ambient)

MB 7071 PIN ASSIGNMENT



*TERMINAL SPACING = 75 mil

MB 7072 PIN ASSIGNMENT

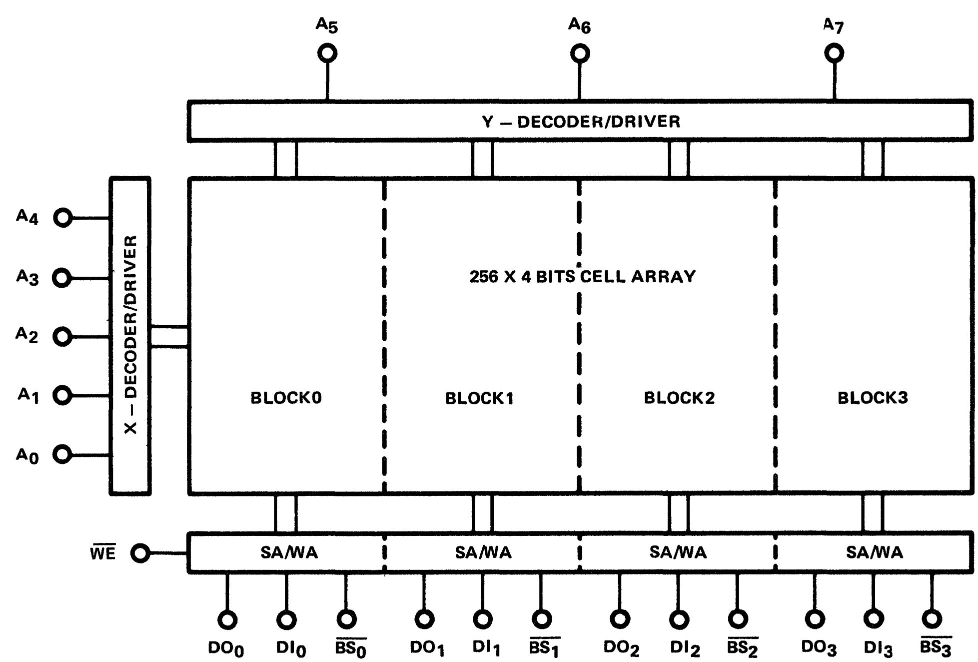


STANDARD 22 PIN DIP

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+05. to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC Output High)	I_{OUT}	30	mA
Temperature Under Bias	T_A	−25 to +125	°C
Storage Temperature	T_{stg}	−55 to +150	°C

MB 7071 BLOCK DIAGRAM



TRUTH TABLE (POSITIVE LOGIC)

INPUT BS	INPUT WE	INPUT DI	OUTPUT	MODE
H	X	X	L	DISABLE
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	DO	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

DC CHARACTERISTICS

V_{EE} = −5.2V, Output Load = 50 Ohm to −2V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Output High Voltage	V_{OH}	−1000 − 960 − 900		− 840 − 810 − 720	mV	0°C 25°C 75°C $V_{IN} = V_{IHmax}$ or V_{ILmin}
Output Low Voltage	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C $V_{IN} = V_{IHmax}$ or V_{ILmin}
Output High Voltage	V_{OHC}	−1020 − 980 − 920			mV	0°C 25°C 75°C $V_{IN} = V_{IHmin}$ or V_{ILmax}
Output Low Voltage	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C $V_{IN} = V_{IHmin}$ or V_{ILmax}
Input High Voltage	V_{IH}	−1145 −1105 −1045		− 840 − 810 − 720	mV	0°C 25°C 75°C
Input Low Voltage	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current	I_{IH}			220	μA	0°C to 75°C
Input Low Current	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current	I_{EE}		N: −120 H: −160		mA mA	0°C to 75°C 0°C to 75°C

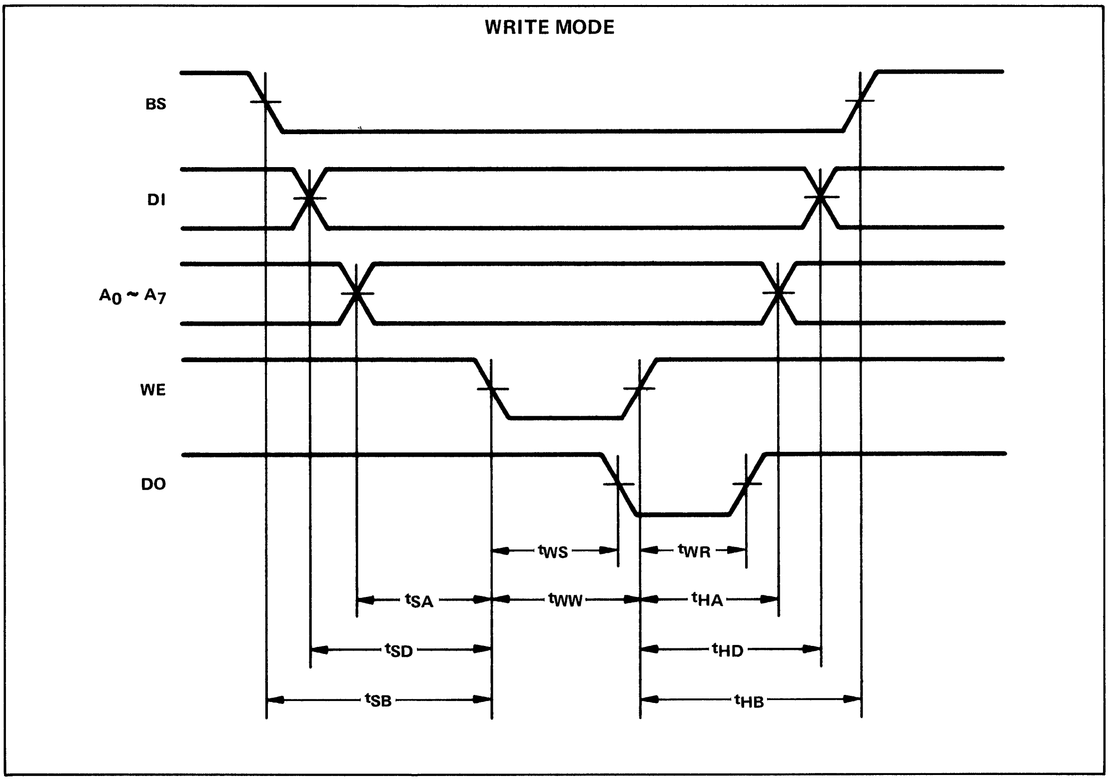
Bipolar Memories

AC CHARACTERISTICS

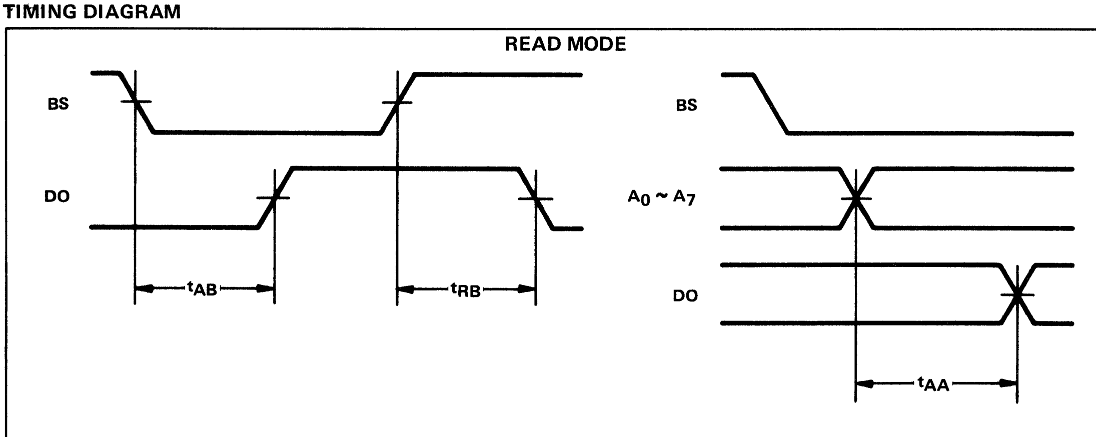
V_{EE} = –5.2V ± 5%, T_A = 0°C to +75°C, Output Load = 50 Ohm to –2V and 15 pF to V_{CC}

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Block Select Access Time	t_{AB}		3.0	4.5	ns	
Block Select Recovery Time	t_{RB}		3.0	4.5	ns	
Address Access Time	t_{AA}		N: 9.0 H: 7.5	N: 15.0 H: 10.0	ns ns	
Write Pulse Width	t_{WW}	8.0	5.5		ns	
Address Set Up Time	t_{SA}	N: 3.0 H: 2.0			ns ns	t_{WW} = 8.0 ns
Block Select Set Up Time	t_{SB}	N: 3.0 H: 2.0			ns ns	
Data Set Up Time	t_{SD}	N: 3.0 H: 2.0			ns ns	
Address Hold Time	t_{HA}	N: 4.0 H: 2.0			ns ns	
Block Select Hold Time	t_{HB}	N: 4.0 H: 2.0			ns ns	
Data Hold Time	t_{HD}	N: 4.0 H: 2.0			ns ns	
Write Disable Time	t_{WS}	5.0	3.0		ns	
Write Recovery Time	t_{WR}	9.0	6.0		ns	
Output Rise Time	t_r		3.0		ns	Measured between 20% and 80% points
Output Fall Time	t_f		3.0		ns	
Input Pin Capacitance	C_{IN}			8.0	pF	
Output Pin Capacitance	C_{OUT}			8.0	pF	

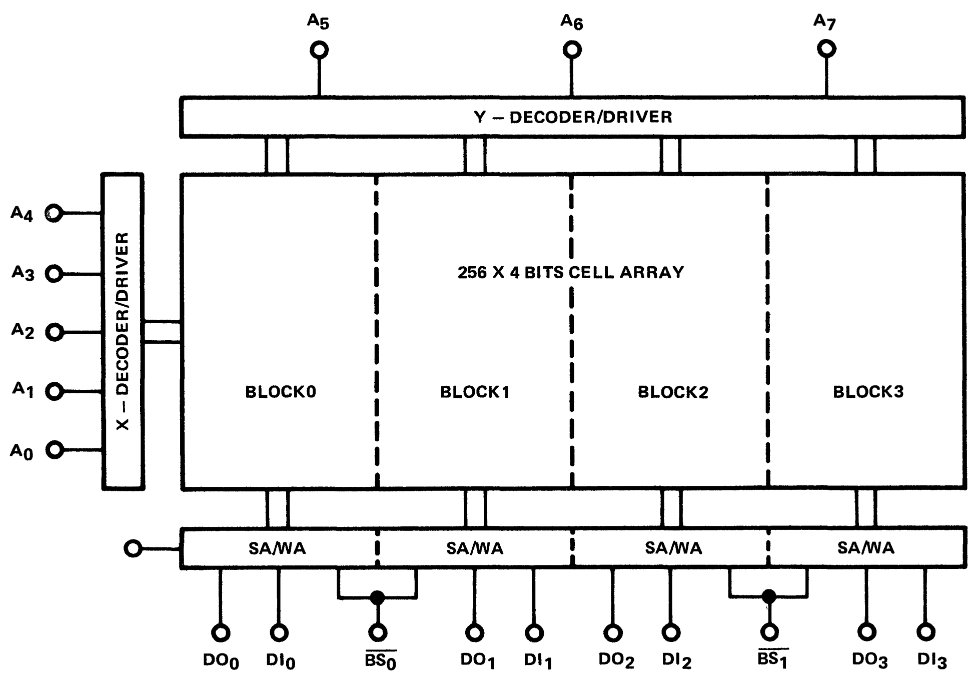
TIMING DIAGRAM



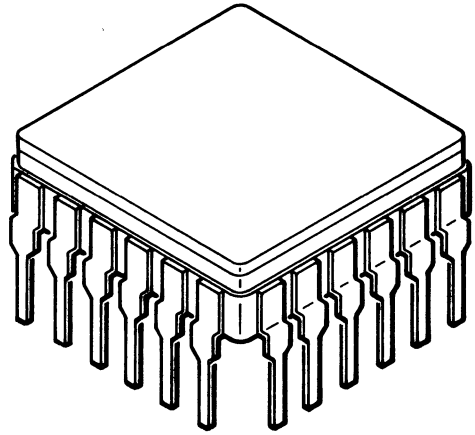
TIMING DIAGRAM



MB 7072 BLOCK DIAGRAM

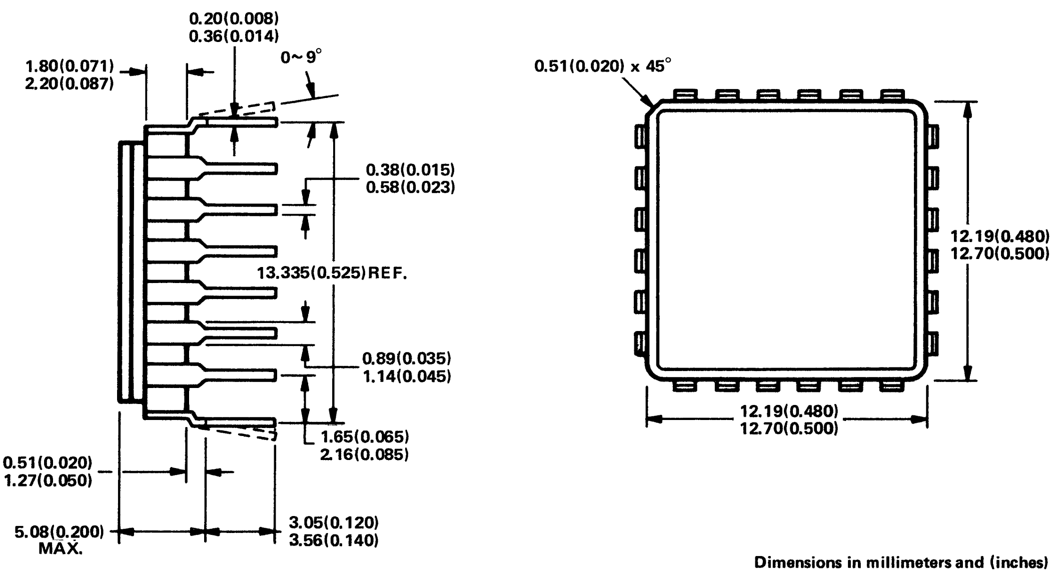


MB 7071 – CASE QIT24 CERAMIC PACKAGE



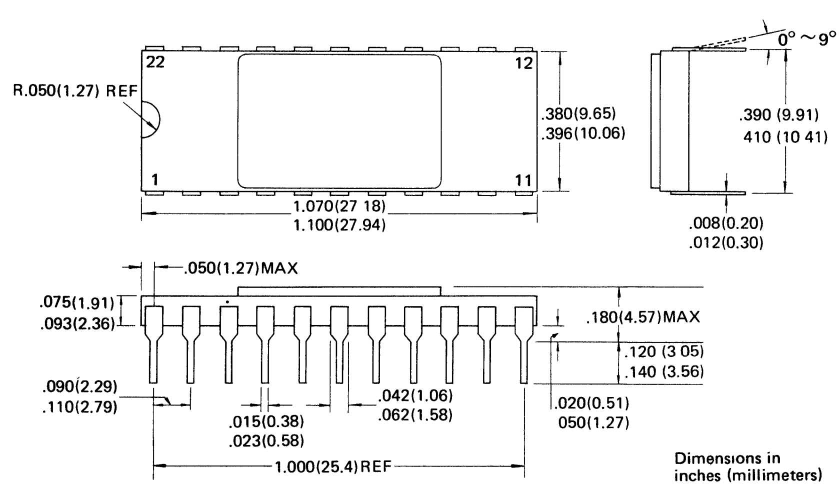
PACKAGE DIMENSIONS

MB 7071



Dimensions in millimeters and (inches)

MB 7072



Dimensions in inches (millimeters)

FUJITSU

PROGRAMMABLE 256-BIT READ ONLY MEMORY

MB 7051 MB 7056

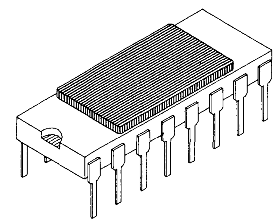
TTL 256-BIT PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MB 7051 and MB 7056 are electrically field programmable high-speed bipolar TTL 256-bit read only memories organized as 32 words by 8 bits. With three-state outputs provided on the MB 7051 and uncommitted collector outputs on the MB 7056, memory expansion is simple. Both devices have on-chip address decoding and chip enable, and they are fully compatible with both DTL and TTL circuits.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be electrically programmed in the selected bit locations at the rate of 10 μs/bit (typical).

Additional circuitry is built into the Fujitsu PROM chip to allow factory testing after packaging for AC, DC and programming parameters. The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform tests of key parameters prior to shipment. This results in extremely high programmability.

- 32 words by 8 bits organization, fully decoded
- High programmability of 99% typical (98% minimum)
- Programming by diffused aluminum eutectic process
- Ultra-fast programming time of 10 μs/bit (typical)
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques
- Fast access time of 40 ns typical (50 ns maximum) at 25°C



CASE DIP16-A
CERAMIC PACKAGE

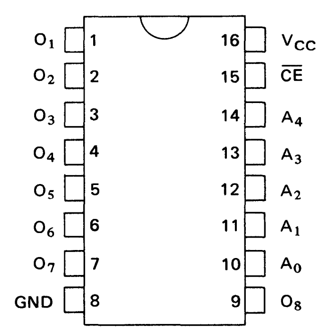
- DTL/TTL compatible inputs and outputs
- Active pull-up (3-state) on MB 7051 or resistor pull-up (open-collector) on MB 7056
- Chip enable ($\overline{CE}$) lead for simplified memory expansion
- Standard 16-pin DIP package
- Interchangeable with IM5600/5610

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to Ground Pin	V_{CC}	-0.5 to + 7.0	V
Input Voltage	V_{IN}	-1.5 to + 5.5	V
Output Voltage	V_{OUT}	-0.5 to + 5.5	V
Output Voltage (during programming)	V_{PRG}	-0.5 to 32.5	V
Input Current	I_{IN}	− 20	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{PRG}	+220	mA
Temperature under Bias	T_A	-25 to +125	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

PIN ASSIGNMENT



GUARANTEED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	—	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	—	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

(Full guaranteed operating ranges unless otherwise noted.)

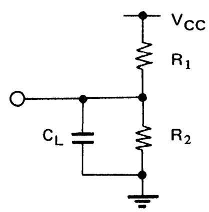
Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}	—	—	60	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.4V)		I_F	—	—	−1.0	mA
Output Low Voltage (I_{OL} = 16mA)		V_{OL}	—	—	0.45	V
Output Leakage Current (V_O = 5.5V, chip disabled)		I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.4V, chip disabled)		I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −10mA)		V_{IC}	—	—	−1.5	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}	—	—	100	mA
Output Leakage Current (V_O = 5.5V, chip enabled)		I_{OLK}*	—	—	100	μA
Output High Voltage (I_O = −2.4mA)	MB 7051	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	MB 7051	I_{OS}*	−15	—	−60	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{I\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

CAPACITANCE (f=1MHz; V_{CC} = +5V; V_{IN} = +2V; T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	12	pF

Fig. 1—AC TEST CONDITIONS



INPUT CONDITIONS

Amplitude .... 0V to 3V

Rise and Fall Time.......... 5ns from 1V to 2V

Frequency .... 1 MHz

	MB 7051/7056		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}"1"	∞	600Ω	30pF
t_{DIS}"0"	300Ω	600Ω	30pF
t_{EN}"1"	∞	600Ω	30pF
t_{EN}"0"	300Ω	600Ω	30pF

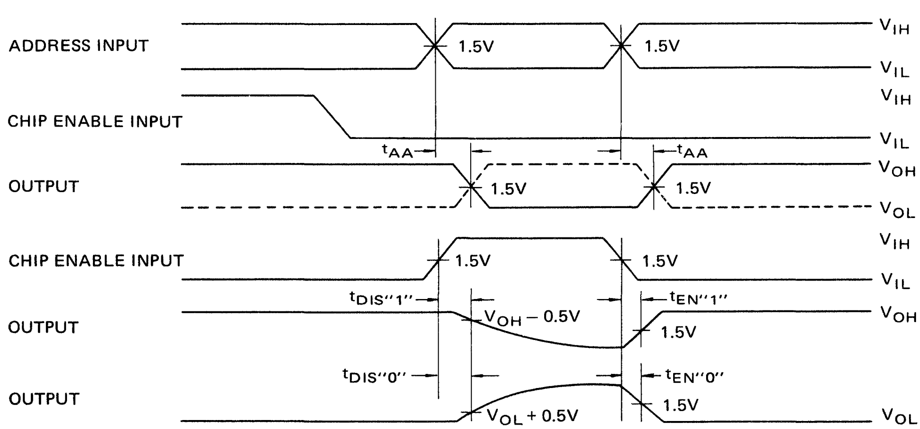
AC CHARACTERISTICS

(Full guaranteed operating ranges unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Access Time (via address input)	t_{AA}*	—	(40)	75 (50)	ns
Output Disable Time	t_{DIS}*	—	(35)	75 (50)	ns
Output Enable Time	t_{EN}*	—	(35)	75 (50)	ns

***Note:** Values in parenthesis denote conditions at $T_A = 25°C$ and $V_{CC} = 5.0V$.

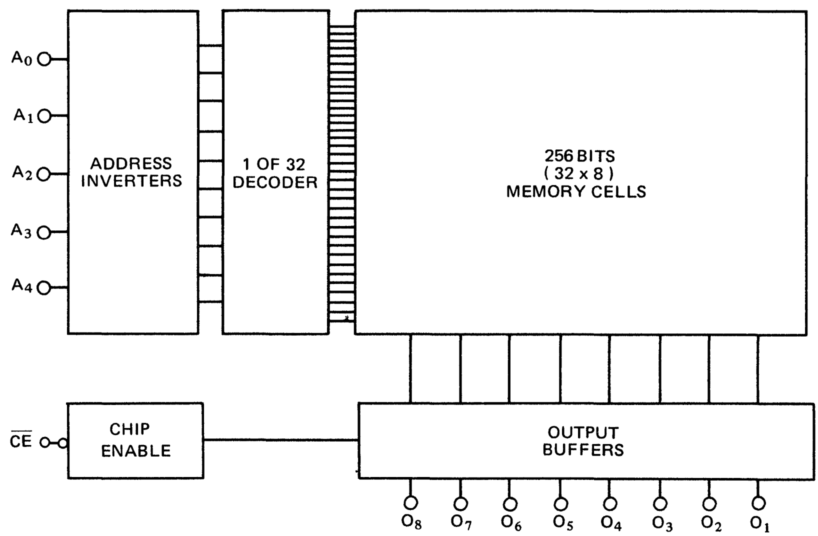
OPERATION TIMING DIAGRAM



Notes: 1) Output disable time is the time taken for the output to reach a high resistance state when the chip enable is taken high. Output enable time is the time taken for the output to become active when the chip enable is taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

2) t_{AA}, t_{DIS}"1" and t_{EN}"1" cannot be tested prior to programming, but are guaranteed by factory testing.

Fig. 2—MB 7051/7056 BLOCK DIAGRAM



TYPICAL INPUT CHARACTERISTICS CURVES

Fig. 3—I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

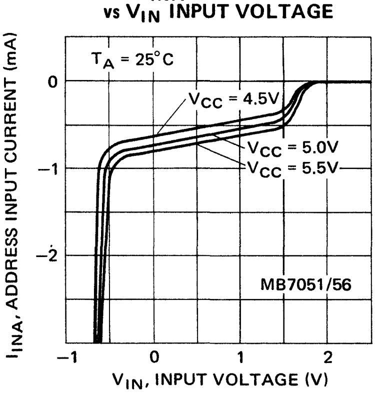
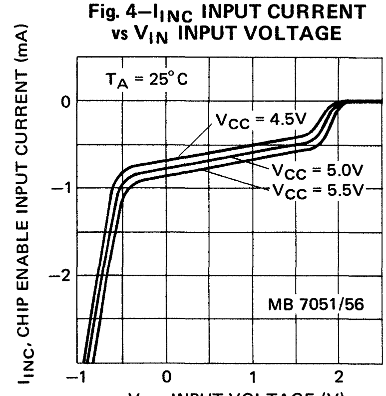


Fig. 4—I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE



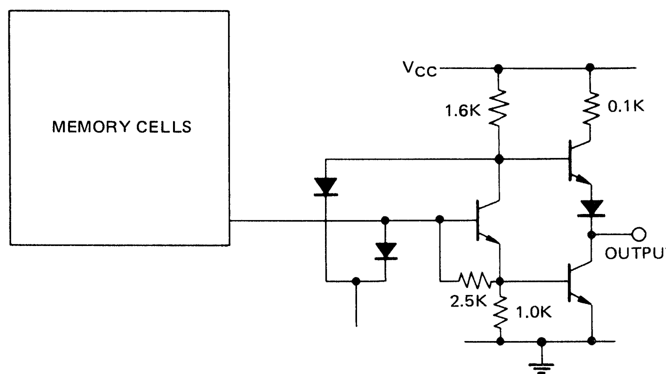
OUTPUT CIRCUIT INFORMATION

THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

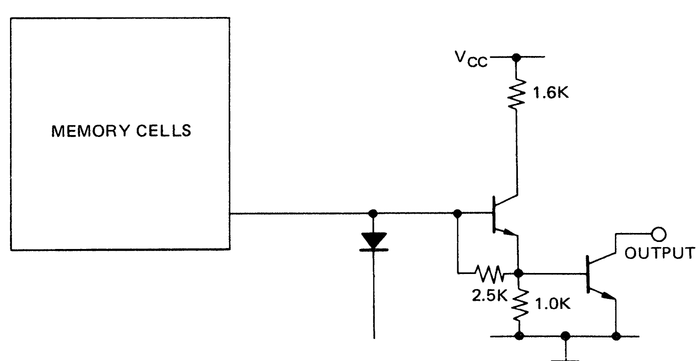
Fig. 5—MB 7051 OUTPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7051 (3-state) compared to 0 mA for the MB 7056 (open-collector).

Fig. 6—MB 7056 OUTPUT



Bipolar Memories

TYPICAL OUTPUT/SWITCHING CHARACTERISTICS CURVES

Fig. 7—I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT VOLTAGE

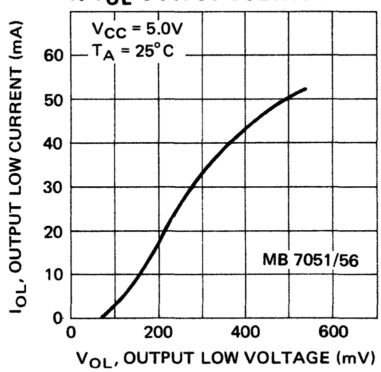


Fig. 8—I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

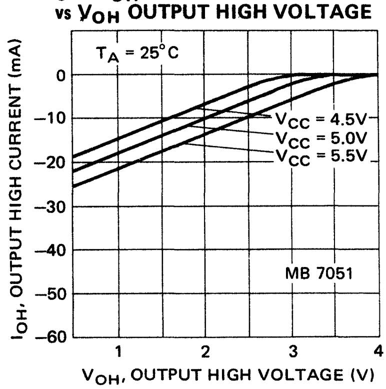


Fig. 9—t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

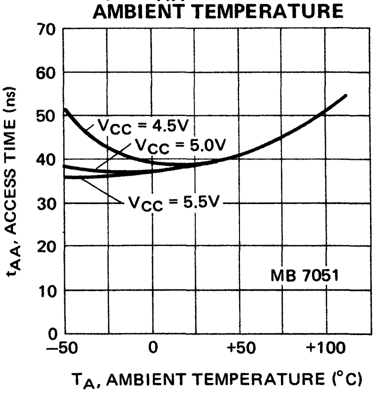


Fig. 10—t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

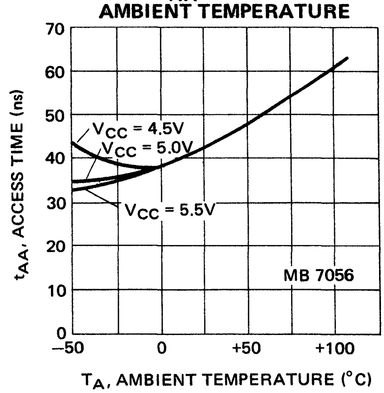


Fig. 11—t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

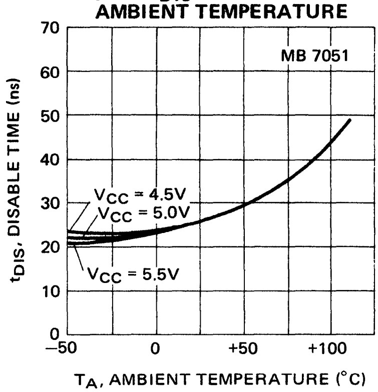


Fig. 12—t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

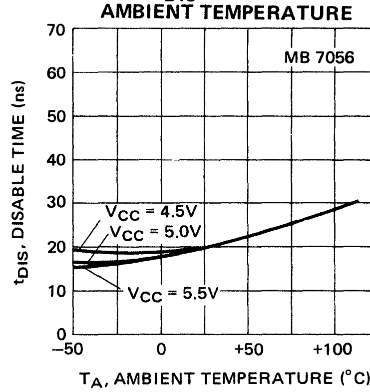


Fig. 13—t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

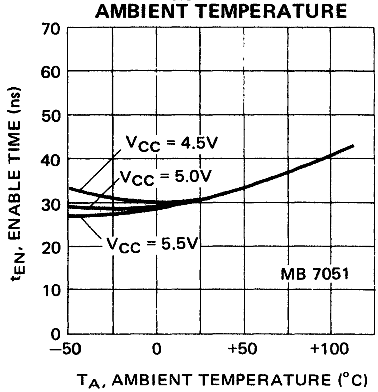


Fig. 14—t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

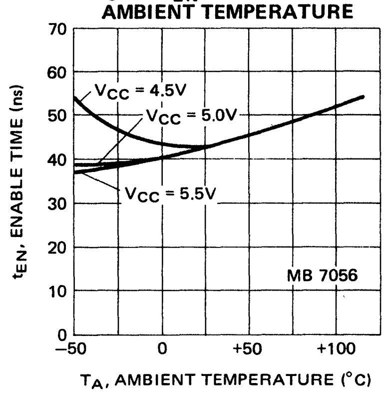


Fig. 15—DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

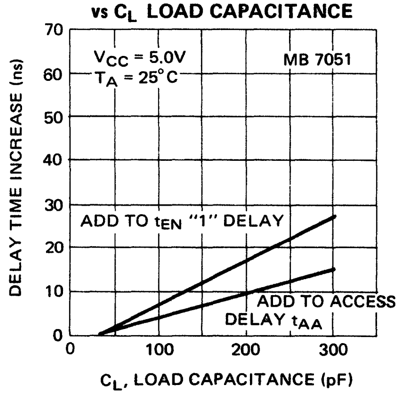
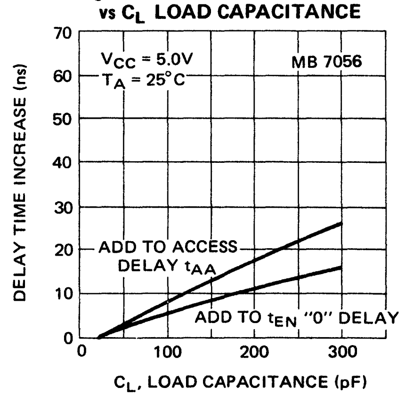


Fig. 16—DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

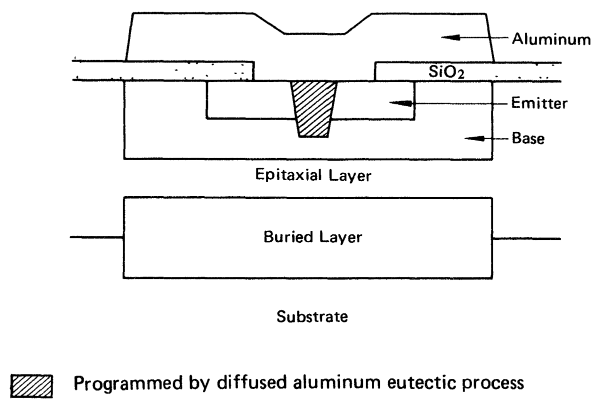
FUJITSU PROM TECHNOLOGY

Fujitsu's sophisticated Fine Emitter technology and programming pulse method enables higher programmability and faster programming time than ordinary PROMs, for the highest reliability.

Fast programming time of typically 10μs/bit is achieved with a fine emitter cell which requires less programming energy; thus, negligible thermal stress. Further, Fujitsu advanced technology allows very high programmability of typically 99%.

To assure that the element is programmed properly, an additional four programming pulses are applied immediately after a sense pulse indicates conduction in the programmed bit. This high reliability feature virtually eliminates aluminium migration in the programmed cell. The basic manufacturing process is a highly reliable gold doped TTL process.

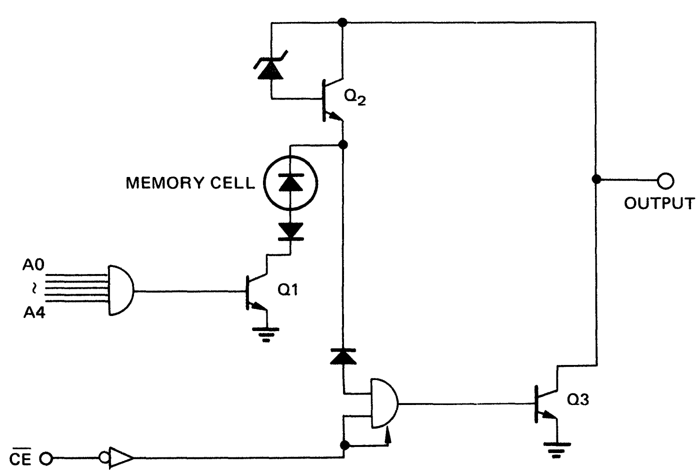
Fig. 17 – PROGRAMMED CELL (CROSS SECTION)



SPECIAL FACTORY TESTING

One extra row and one extra column of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

Fig. 18—INTERNAL PROGRAMMING CIRCUIT



PROGRAMMING

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using five address inputs to turn on transistor Q1. By taking the chip enable input high, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the sensed voltage indicates that the selected bit is in the logic one state.

An additional 4 programming pulses are required to ensure that the bit is fully programmed, and to achieve high reliability.

One output must be programmed at a time, since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking the chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA/MB7051 at V_{OH} = 2.1V and V_{CC}=4.35V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

Note:
These PROMs can be programmed via either of two methods. First, the MB 7051/56, which are directly compatible with the IM 5600/10, can be programmed using the IM 5600/10 programmer. Additionally, the MB 7051/56 can be programmed using the same specification (with the exception of clamp and reference voltages) as used for the MB 7052/IM 5623, MB 7057/IM 5603, IM 5604 and IM 5624; thus, the programming specifications contained herein are provided for your convenience when using these latter methods.

DC SPECIFICATIONS (T_A = 25°C)

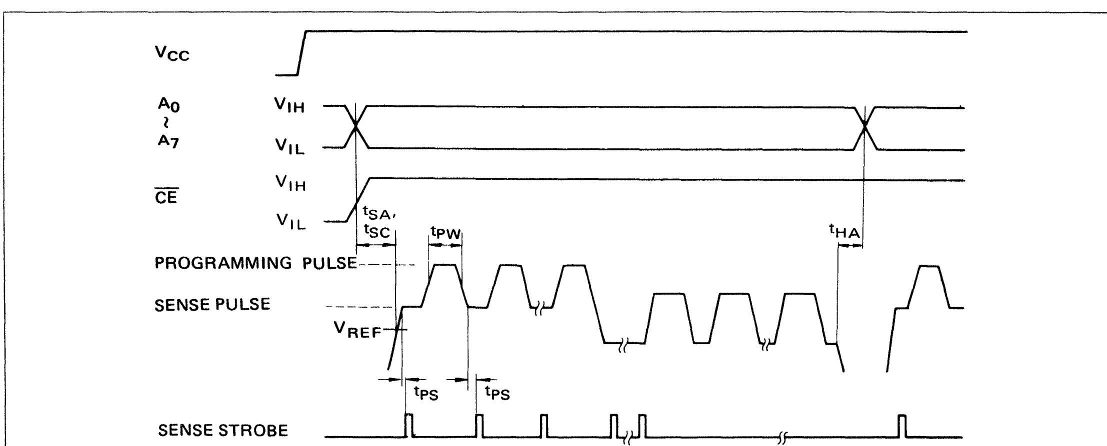
Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.25	V
Power Supply Voltage	V_{CC}	5.0	5.0	5.25	V
Programming Pulse Current	I_{PRG}	190	200	210	mA
Sense Pulse Current	I_{SNS}	19	20	21	mA
Programming Pulse Clamp Voltage	V_{PRG}	31.5	32.0	32.0	V
Sense Pulse Clamp Voltage	V_{SNS}	31.5	32.0	32.0	V
Sensed Voltage for a Programmed "1"	V_{REF}	13.4	13.5	13.6	V

AC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Duty Cycle	—	70	—	—	%
Programming Pulse Width	t_{PW}*	7.2	7.5	7.8	μs
Programming Pulse Ramp Rate (Rise)	—	50	—	70	V/μs
Programming Pulse Ramp Rate (Fall)	—	—	—	150	V/μs
Address Input Set-up Time	t_{SA}	500	—	—	ns
Chip Enable Input Set-up Time	t_{SC}	500	—	—	ns
Address Input Hold Time	t_{HA}	500	—	—	ns
Chip Enable Input Hold Time	t_{HC}	500	—	—	ns
Programming Pulse Trailing Edge to Sense Strobe Time	t_{PS}	700	—	—	ns
Programming Pulse Number	—	—	—	100	Time
Programming Time/Device	—	—	—	256	ms
Additional Programming Pulse Number	—	4	4	4	Time

***Note:** Stipulated at 150Ω load and 15V.

TYPICAL WAVEFORMS



PROGRAMMING INFORMATION (continued)

PROGRAMMING PROCEDURE

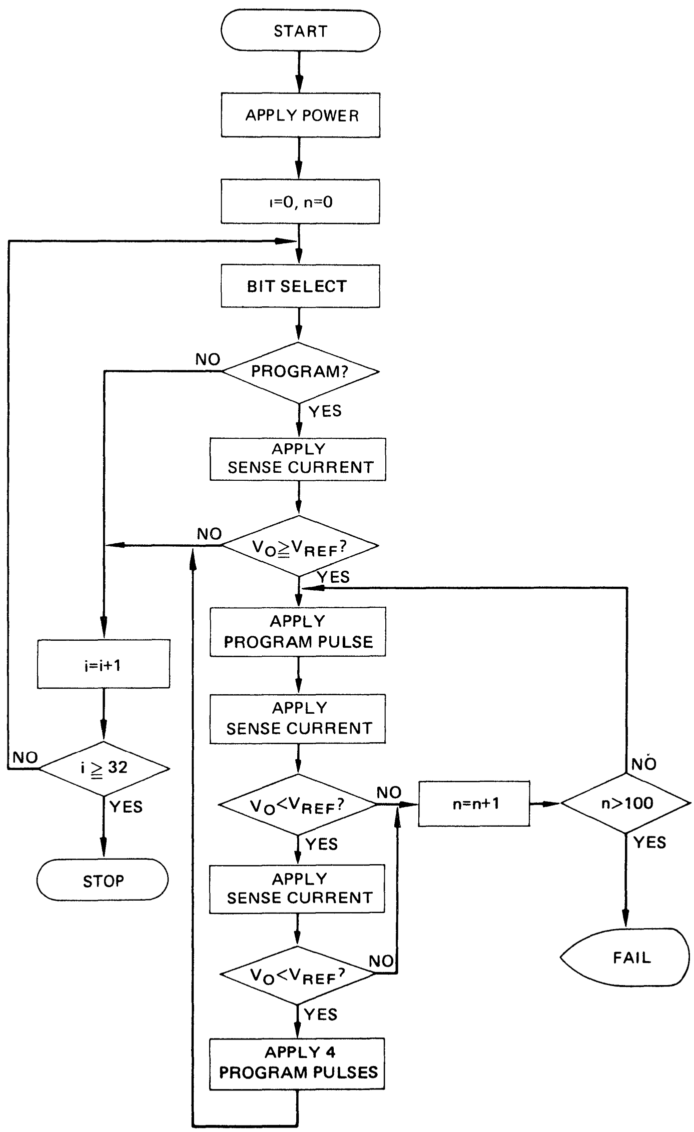
1. Apply the proper power ; V_{CC} = 5.0V, GND = 0V
2. Select the desired word using five address inputs.
3. Take the chip enable input high.
4. Apply 20mA sense current to the desired output after a delay of t_{SC}, and confirm that the output voltage "V_O" is higher than, or equal to, the sensed voltage "V_{REF}". (In the case of $V_O < V_{REF}$, select the next desired address after a delay of t_{HA}.)
5. Apply a programming pulse with amplitude of 200mA and duration of t_{PW}.
6. Apply the 20mA sense current and compare V_O with V_{REF} after a delay of t_{PS}.
   a) In the case of $V_O \geq V_{REF}$, the selected bit is still in the logic ZERO state. Repeat steps "5" and "6".
   b) In the case of $V_O < V_{REF}$, the selected bit is then in the logic ONE state. Apply the sense current again, and confirm $V_O < V_{REF}$ after a delay of equal to (or greater than) t_{PW} without intervening with programming pulse. In the case of $V_O \geq V_{REF}$, repeat steps "5" and "6" again.
7. After confirmation of $V_O < V_{REF}$, apply four additional programming pulses. In the case of $V_O \geq V_{REF}$, then, repeat steps "5" and "6", again. Select the next desired word after a delay of t_{HA}.

Notes: 1) Sense current must be interrupted (= zero) during each address change.

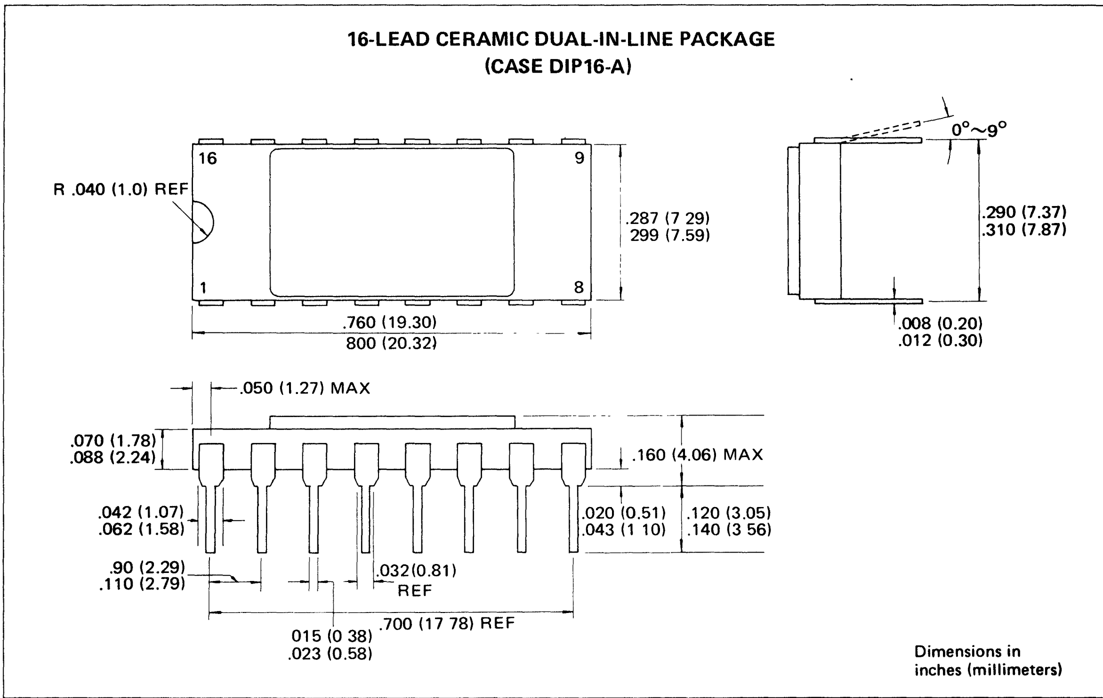
2) Programming must be done bit by bit.

3) Ambient temperature during programming must be room temperature (25° ±2°C).

Fig. 19—PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information herein has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

PROGRAMMABLE 1024-BIT READ ONLY MEMORY

MB 7052
MB 7057

FUJITSU

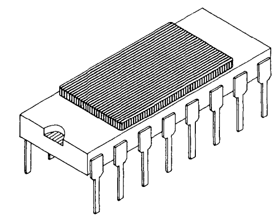
TTL 1024-BIT PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MB 7052 and MB 7057 are electrically field programmable, high speed bipolar TTL 1024-bit read only memories organized as 256 words by 4 bits. With three-state outputs provided on the MB 7052 and uncommitted collector outputs on the MB 7057, memory expansion is simple. Both devices have on-chip address decoding and chip enable, and they are fully compatible with both DTL and TTL circuits.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be electrically programmed in the selected bit locations at the rate of 10 μs/bit (typical).

Additional circuitry is built into the Fujitsu PROM chip to allow factory testing after packaging for AC, DC and programming parameters. The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform tests of key parameters prior to shipment. This results in extremely high programmability.

- 256 words x 4 bits organization, fully decoded
- High programmability of 99% typical (98% minimum)
- Programming by diffused aluminum eutectic process
- Ultra-fast programming time of 10 μs/bit (typical)
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques



CASE DIP16-A
CERAMIC PACKAGE

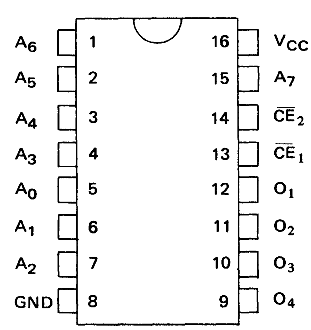
- Fast access time of 40 ns typical (60 ns maximum) at T_A = 25°C
- DTL/TTL compatible inputs and outputs
- Active pull-up (3-state) on MB 7052 or resistor pull-up (open-collector) on MB 7057
- Two chip enable ($\overline{CE}$) leads for simplified memory expansion
- Standard 16-pin DIP package
- Interchangeable with IM5603/5623

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to Ground Pin	V_{CC}	−0.5 to + 7.0	V
Input Voltage	V_{IN}	−1.5 to + 5.5	V
Output Voltage	V_{OUT}	−0.5 to + 5.5	V
Output Voltage (during programming)	V_{PRG}	−0.5 to +28.5	V
Input Current	I_{IN}	− 20	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{PRG}	+220	mA
Temperature Under Bias	T_A	−25 to +125	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

PIN ASSIGNMENT



GUARANTEED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	—	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	—	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

(Full guaranteed operating ranges unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}	—	—	60	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.4V)		I_F	—	—	−1.0	mA
Output Low Voltage (I_{OL} = 16mA)		V_{OL}	—	—	0.45	V
Output Leakage Current (V_O = 5.5V, chip disabled)		I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.4V, chip disabled)		I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −10mA)		V_{IC}	—	—	−1.5	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}	—	—	130	mA
Output Leakage Current (V_O = 5.5V, chip enabled)		I_{OLK}*	—	—	100	μA
Output High Voltage (I_O = −2.4mA)	MB 7052	V_{OH}*	2.4	—	—	V
Output High Voltage (I_O = −0.4mA)	MB 7057	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	MB 7052	I_{OS}*	−15	—	−60	mA
Output Short Circuit Current (V_O = GND)	MB 7057	I_{OS}*	−1.0	—	−6.0	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{I\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

CAPACITANCE (f = 1MHz; V_{CC} = +5V; V_{IN} = +2V; T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	12	pF

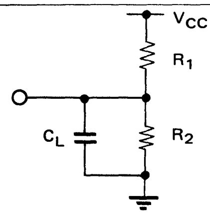


Fig. 1— AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude .... 0V to 3V
Rise and Fall Time .... 5ns from 1V to 2V
Frequency.................. 1 MHz

	MB7052			MB7057		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF	300Ω	600Ω	30pF
t_{DIS} "1"	∞	600Ω	10pF	∞	3.3KΩ	10pF
t_{DIS} "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t_{EN} "1"	∞	600Ω	30pF	∞	3.3KΩ	30pF
t_{EN} "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

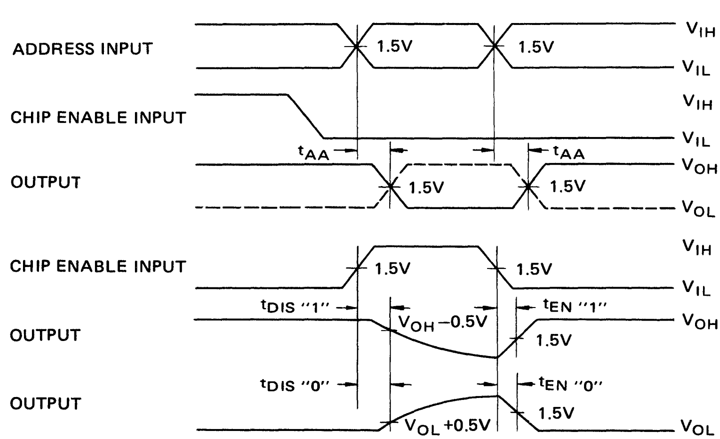
AC CHARACTERISTICS

(Full guaranteed operating ranges unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Access Time (via address input)	t_{AA}*	—	(40)	70 (60)	ns
Output Disable Time	t_{DIS}*	—	(16)	40 (30)	ns
Output Enable Time	t_{EN}*	—	(22)	40 (30)	ns

***Note:** Values in parenthesis denote conditions at $T_A = 25°C$.

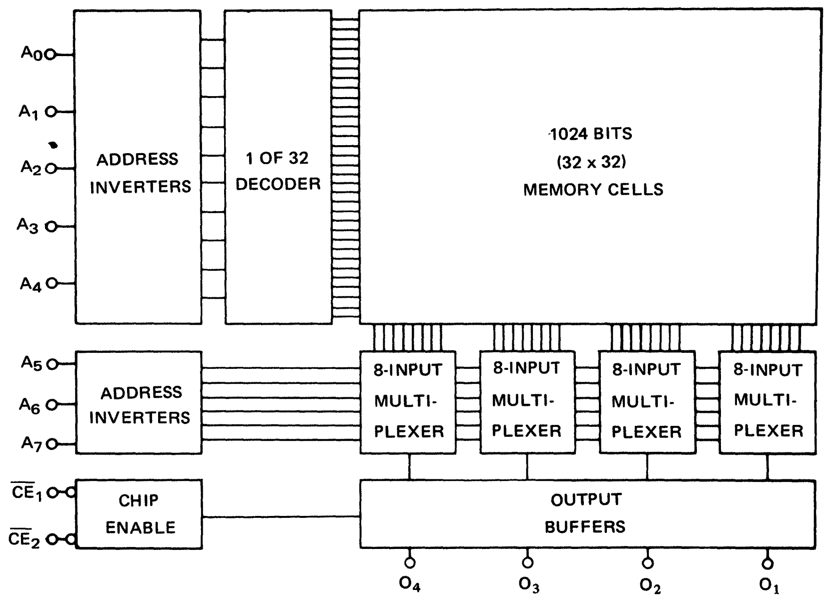
OPERATION TIMING DIAGRAM



Notes: 1) Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

2) t_{AA}, t_{DIS}"1" and t_{EN}"1" cannot be tested prior to programming, but are guaranteed by factory testing.

Fig. 2 — MB 7052/7057 BLOCK DIAGRAM



TYPICAL INPUT CHARACTERISTICS CURVES

Fig. 3 — I_{INA} INPUT CURRENT VS V_{IN} INPUT VOLTAGE

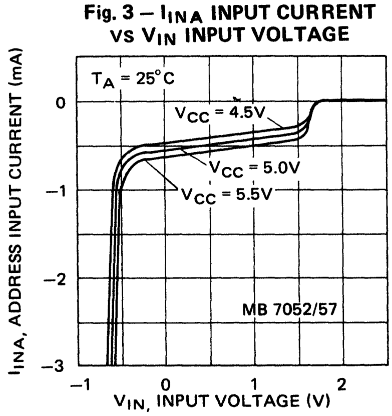
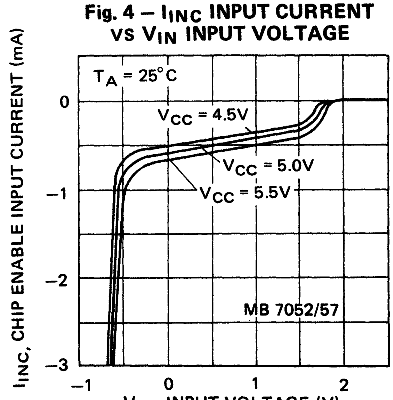


Fig. 4 — I_{INC} INPUT CURRENT VS V_{IN} INPUT VOLTAGE



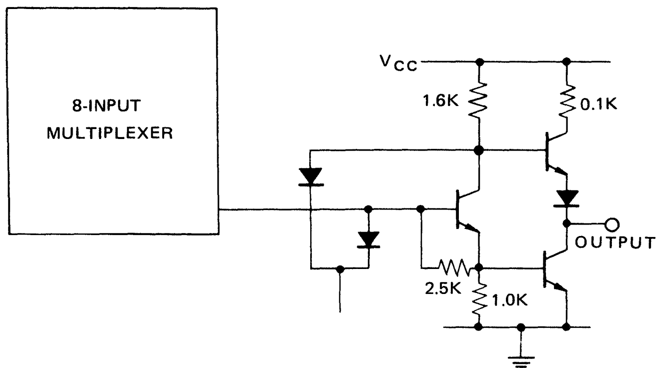
OUTPUT CIRCUIT INFORMATION

THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impendance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

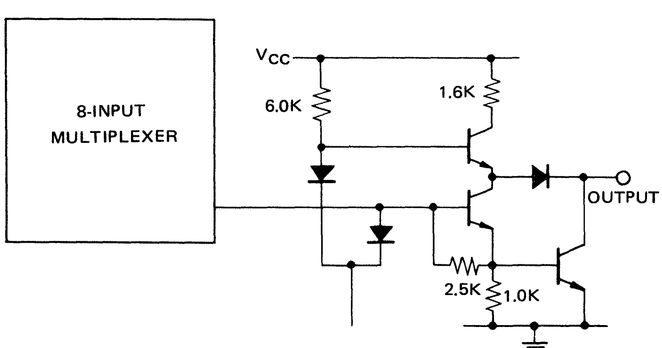
Fig. 5 – MB 7052 OUTPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7052 (3-state) compared to typically 3.0mA for the MB 7057 (open-collector).

Fig. 6 – MB 7057 OUTPUT



Bipolar Memories

TYPICAL OUTPUT/SWITCHING CHARACTERISTICS CURVES

Fig. 7 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

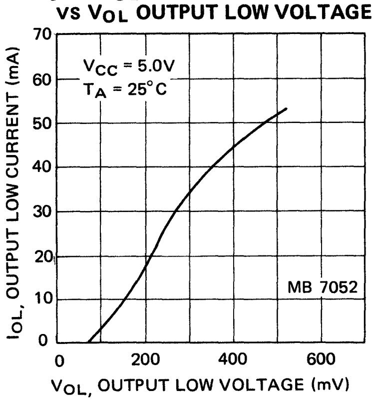


Fig. 8 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

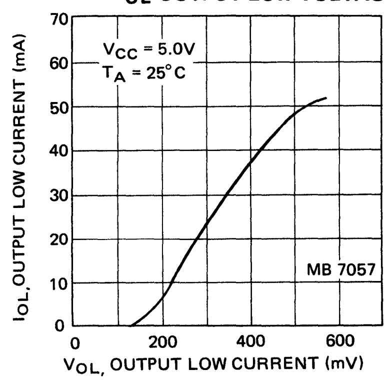


Fig. 9 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

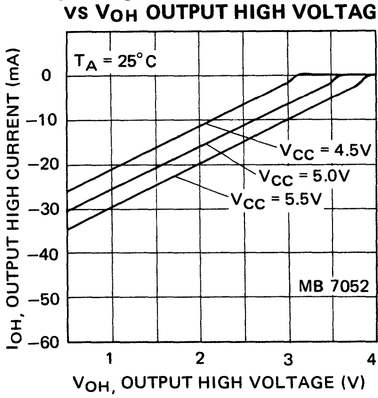


Fig. 10 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

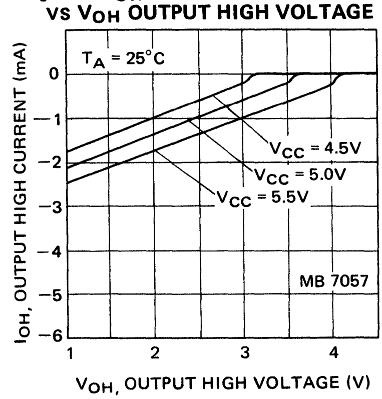


Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

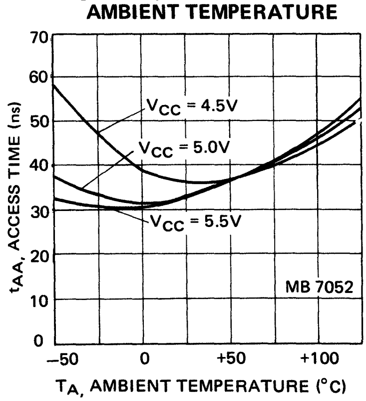


Fig. 12 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

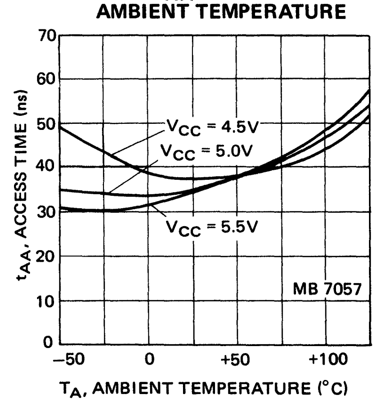


Fig. 13 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

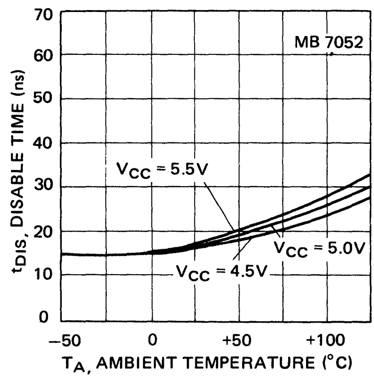


Fig. 14 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

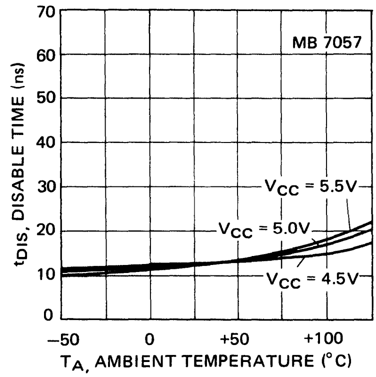


Fig. 15 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

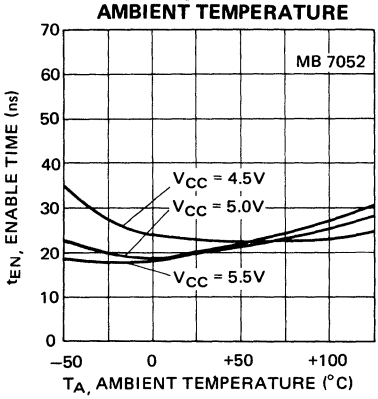


Fig. 16 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

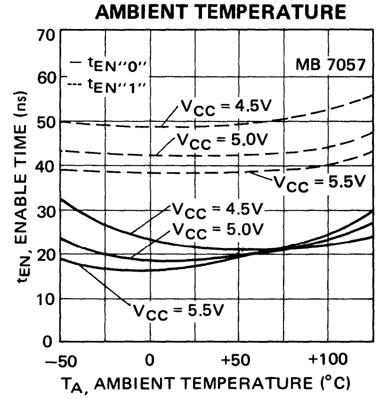


Fig. 17 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

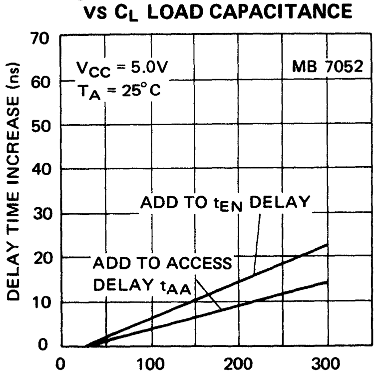
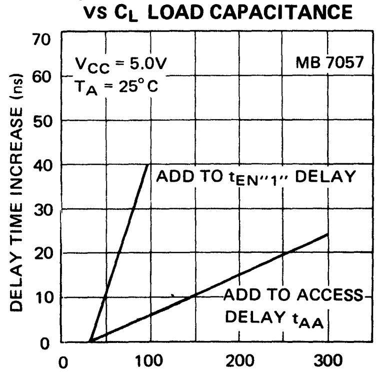


Fig. 18 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

Fujitsu's sophisticated Fine Emitter technology and programming pulse method enables higher programmability and faster programming time than ordinary PROMs, for the highest reliability.

Fast programming time of typically 10μs/bit is achieved with a fine emitter cell which requires less programming energy; thus, negligible thermal stress. Further, Fujitsu advanced technology allows very high programmability of typically 99%.

To assure that the element is programmed properly, an additional four programming pulses are applied immediately after a sense pulse indicates conduction in the programmed bit. This high reliability feature virtually eliminates aluminum migration in the programmed cell. The basic manufacturing process is a highly reliable gold doped TTL process.

SPECIAL FACTORY TESTING

One extra row and one extra column of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

Fig. 19 — PROGRAMMED CELL (CROSS SECTION)

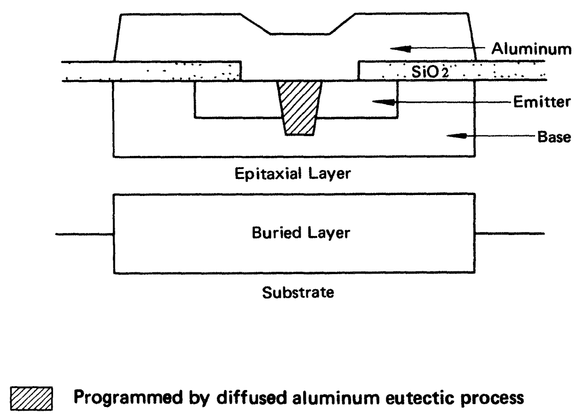
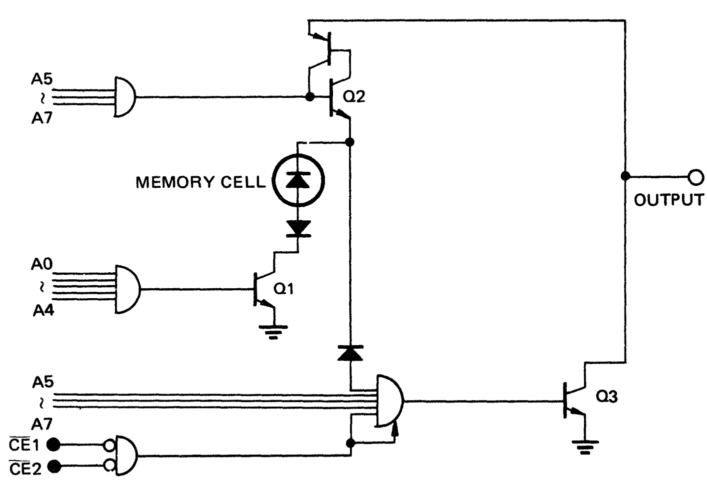


Fig. 20 — INTERNAL PROGRAMMING CIRCUIT



A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using eight address inputs to turn on transistors Q1 and Q2. By taking either (or both) chip enable inputs high, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the sensed voltage indicates that the selected bit is in the logic one state.

An additional 4 programming pulses are required to ensure that the bit is fully programmed, and to achieve high reliability.

One output must be programmed at a time, since the internal decording circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking both chip enable inputs low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA/MB7052 (400μA /MB7057) at V_{OH}=2.1V and V_{CC}= 4.35V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.25	V
Power Supply Voltage	V_{CC}	5.0	5.0	5.25	V
Programming Pulse Current	I_{PRG}	190	200	210	mA
Sense Pulse Current	I_{SNS}	19	20	21	mA
Programming Pulse Clamp Voltage	V_{PRG}	27.5	28.0	28.0	V
Sense Pulse Clamp Voltage	V_{SNS}	27.5	28.0	28.0	V
Sensed Voltage for a Programmed "1"	V_{REF}	6.9	7.0	7.1	V

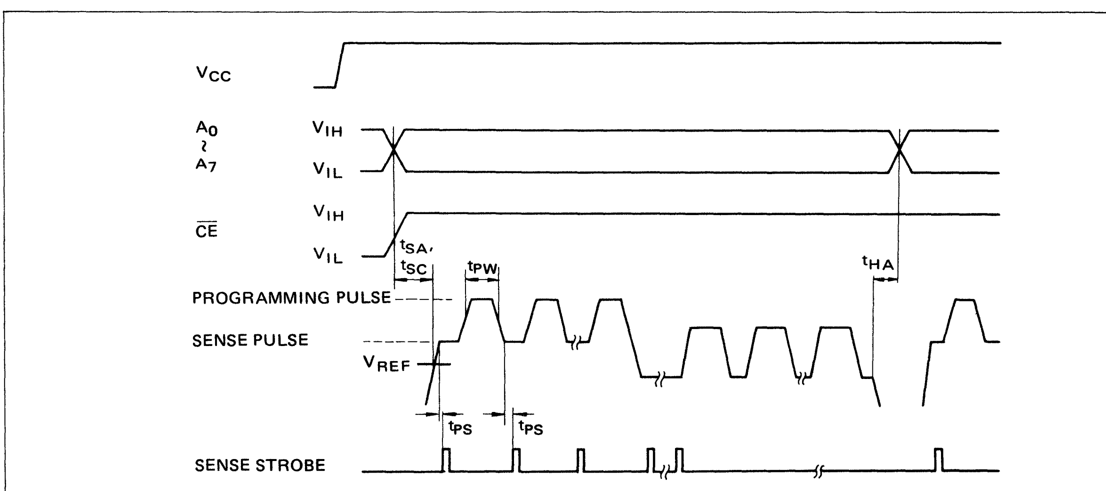
PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Duty Cycle	—	70	—	—	%
Programming Pulse Width	t_{PW}*	7.2	7.5	7.8	μs
Programming Pulse Ramp Rate (Rise)	—	50	—	70	V/μs
Programming Pulse Ramp Rate (Fall)	—	—	—	150	V/μs
Address Input Set-up Time	t_{SA}	500	—	—	ns
Chip Enable Input Set-up Time	t_{SC}	500	—	—	ns
Address Input Hold Time	t_{HA}	500	—	—	ns
Chip Enable Input Hold Time	t_{HC}	500	—	—	ns
Programming Pulse Trailing Edge to Sense Strobe Time	t_{PS}	700	—	—	ns
Programming Pulse Number	—	—	—	100	Time
Programming Time/Device	—	—	—	1024	ms
Additional Programming Pulse Number	—	4	4	4	Time

* Note: Stipulated at 150Ω load and 15V.

TYPICAL WAVEFORMS

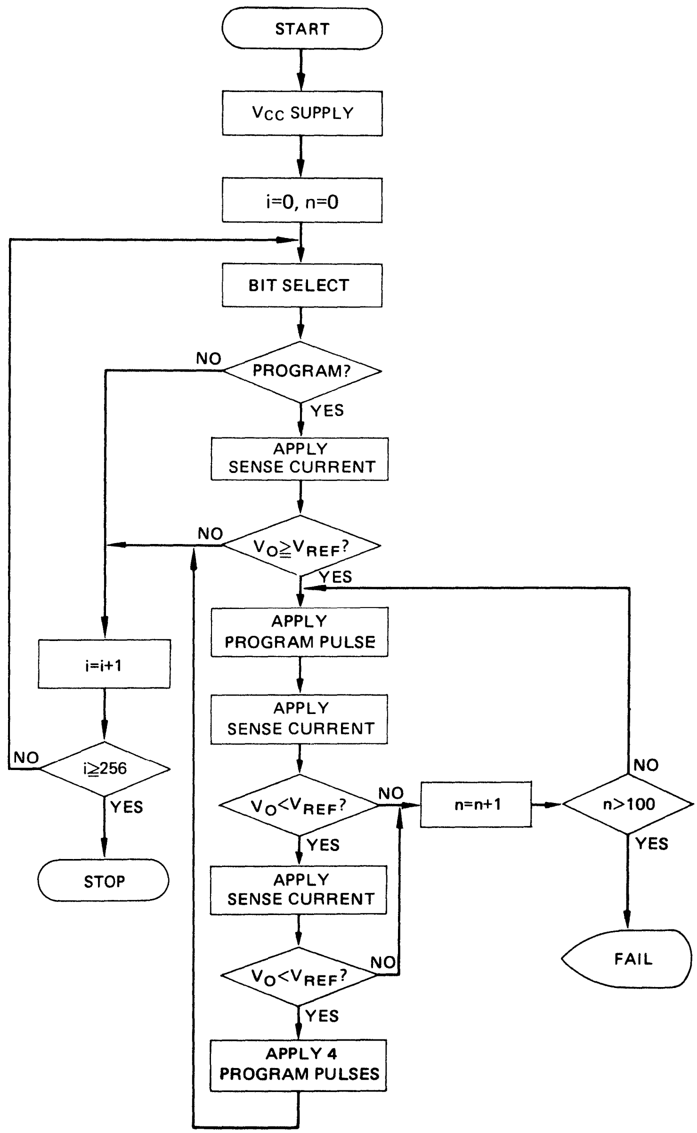


PROGRAMMING PROCEDURE

1. Apply the proper power; V_{CC} = 5.0V, GND = 0V
2. Select the desired word using eight address inputs.
3. Take either (or both) chip enable inputs high.
4. Apply 20mA sense current to the desired output after a delay of t_{SC}, and confirm that the output voltage "V_O" is higher than, or equal to, the sensed voltage "V_{REF}". (In the case of $V_O < V_{REF}$, select the next desired address after a delay of t_{HA}.)
5. Apply a programming pulse with amplitude of 200mA and duration of t_{PW}.
6. Apply the 20mA sense current and compare V_O with V_{REF} after a delay of t_{PS}.
   a) In the case of $V_O \geq V_{REF}$, the selected bit is still in the logic ZERO state. Repeat steps "5" and "6".
   b) In the case of $V_O < V_{REF}$, the selected bit is then in the logic ONE state. Apply the sense current again, and confirm $V_O < V_{REF}$ after a delay of equal to (or greater than) t_{PW} without intervening with programming pulse. In the case of $V_O \geq V_{REF}$, repeat step "5" and "6" again.
7. After confirmation of $V_O < V_{REF}$, apply four additional programming pulses. In the case of $V_O \geq V_{REF}$, then, repeat steps "5" and "6", again. Select the next desired word after a delay of t_{HA}.

Note: 1) Sense current must be interrupted (= zero) during each address change.
2) Programming must be done bit by bit.
3) Ambient temperature during programming must be room temperature (25° ± 2°C).

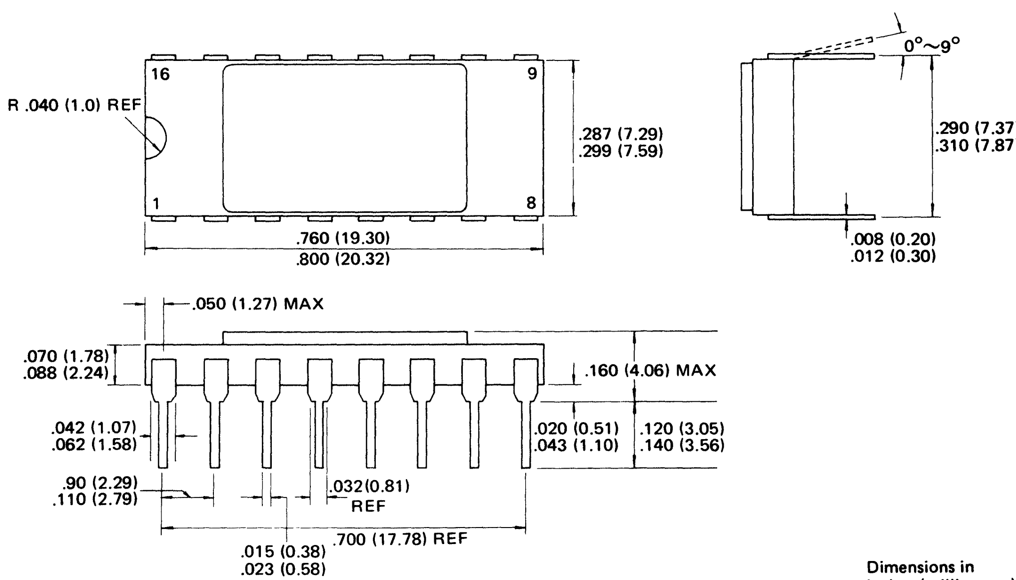
Fig. 21 – PROGRAMMING FLOW CHART



Bipolar Memories

PACKAGE DIMENSIONS

16-LEAD CERAMIC DUAL-IN-LINE PACKAGE
(CASE DIP16-A)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information herein has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

FUJITSU

PROGRAMMABLE 2048-BIT READ ONLY MEMORY

MB 7053 MB 7058

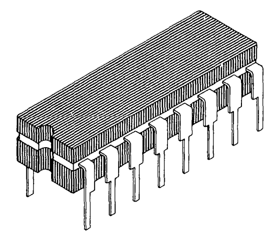
TTL 2048-BIT PROGRAMMABLE READ-ONLY MEMORY

The Fujitsu MB 7053 and MB 7058 are electrically field programmable, high speed bipolar TTL 2048-bit read only memories organized as 512 words by 4 bits. With three-state outputs provided on the MB 7053 and uncommitted collector outputs on the MB 7058, memory expansion is simple. Both devices have on-chip address decoding and chip enable, and they are fully compatible with both DTL and TTL circuits.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be electrically programmed in the selected bit locations at the rate of 10 μs/bit (typical).

Additionial circuitry is built into the Futjitsu PROM chip to allow factory testing after packaging for AC, DC and programming parameters. The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform tests of key parameters prior to shipment. This results in extremely high programmability.

- 512 words x 4 bits organization, fully decoded
- High programmability of 99% typical (98% minimum)
- Programming by diffused aluminum eutectic process
- Ultra-fast programming time of 10 μs/bit (typical)
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques



CASE DIP16-C
CERAMIC PACKAGE

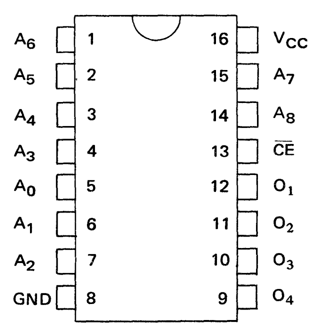
- Fast access time of 40 ns typical (60 ns maximum) at T_A = 25°C
- DTL/TTL compatible inputs and outputs
- Active pull-up (3-state) on MB 7053 or resistor pull-up (open-collector) on MB 7058
- Chip enable ($\overline{CE}$) lead for simplified memory expansion
- Standard 16-pin DIP package
- Interchangeable with IM5604/5624

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to Ground Pin	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	−1.5 to +5.5	V
Output Voltage	V_{OUT}	-0.5 to +5.5	V
Output Voltage (during programming)	V_{PRG}	-0.5 to +28.5	V
Input Current	I_{IN}	-20	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{PRG}	+220	mA
Temperature Under Bias	T_A	-25 to +125	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

PIN ASSIGNMENT



Bipolar Memories

GUARANTEED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	—	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	—	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS
(Full guaranteed operating ranges unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}	—	—	60	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.4V)		I_F	—	—	−1.0	mA
Output Low Voltage (I_{OL} = 16mA)		V_{OL}	—	—	0.45	V
Output Leakage Current (V_O = 5.5V, chip disabled)		I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.4V, chip disabled)		I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −10mA)		V_{IC}	—	—	−1.5	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}	—	—	140	mA
Output Leakage Current (V_O = 5.5V, chip enabled)		I_{OLK}*	—	—	100	μA
Output High Voltage (I_O = −2.4mA)	MB 7053	V_{OH}*	2.4	—	—	V
Output High Voltage (I_O = −0.4mA)	MB 7058	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	MB 7053	I_{OS}*	−15	—	−60	mA
Output Short Circuit Current (V_O = GND)	MB 7058	I_{OS}*	−1.0	—	−6.0	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{I\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

CAPACITANCE (f = 1MHz; V_{CC} = +5V; V_{IN} = +2V; T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	12	pF

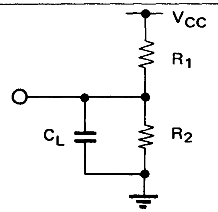


Fig. 1— AC TEST CONDITIONS

	MB7053			MB7058		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF	300Ω	600Ω	30pF
t_{DIS} "1"	∞	600Ω	10pF	∞	3.3KΩ	10pF
t_{DIS} "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t_{EN} "1"	∞	600Ω	30pF	∞	3.3KΩ	30pF
t_{EN} "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

INPUT CONDITIONS

Amplitude .... 0V to 3V
Rise and Fall Time .... 5ns from 1V to 2V
Frequency.................. 1 MHz

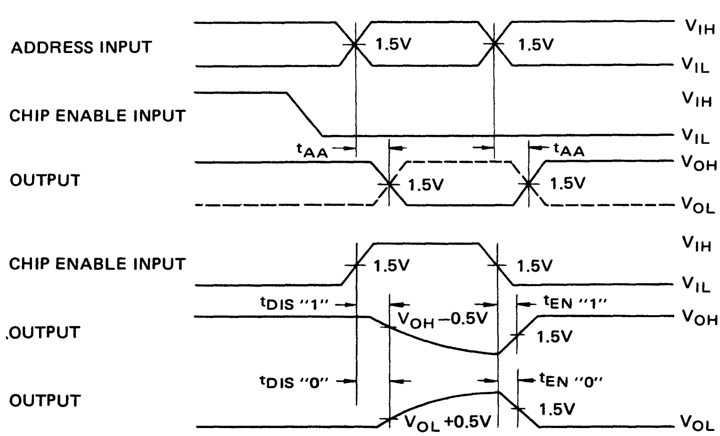
AC CHARACTERISTICS

(Full guaranteed operating ranges unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Access Time (via address input)	t_{AA}*	—	(40)	70 (60)	ns
Output Disable Time	t_{DIS}*	—	(16)	40 (30)	ns
Output Enable Time	t_{EN}*	—	(22)	40 (30)	ns

***Note:** Values in parenthesis denote conditions at $T_A = 25°C$.

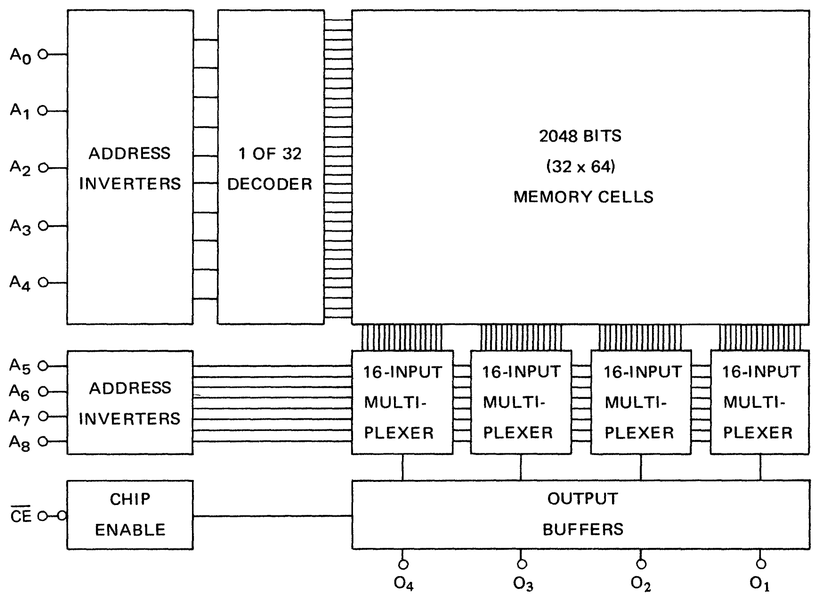
OPERATION TIMING DIAGRAM



Notes: 1) Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

2) t_{AA}, t_{DIS}"1" and t_{EN}"1" cannot be tested prior to programming, but are guaranteed by factory testing.

Fig. 2 — MB 7053/7058 BLOCK DIAGRAM



TYPICAL INPUT CHARACTERISTICS CURVES

Fig. 3 — I_{INA} INPUT CURRENT VS V_{IN} INPUT VOLTAGE

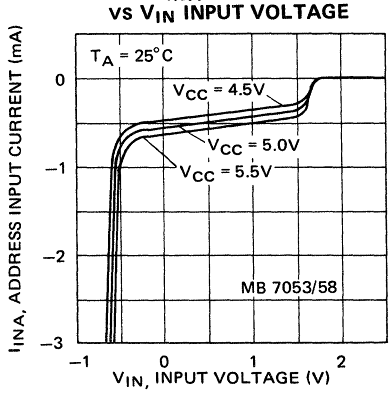
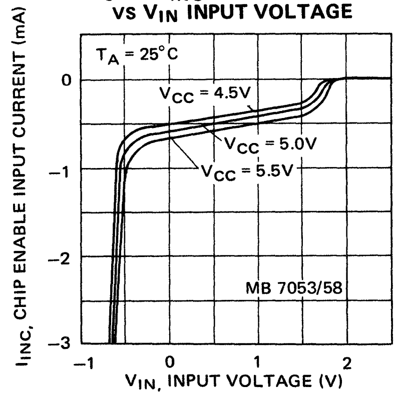


Fig. 4 — I_{INC} INPUT CURRENT VS V_{IN} INPUT VOLTAGE



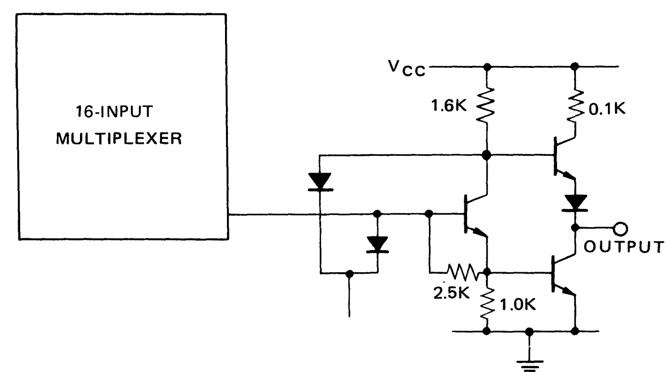
OUTPUT CIRCUIT INFORMATION

THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impendance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

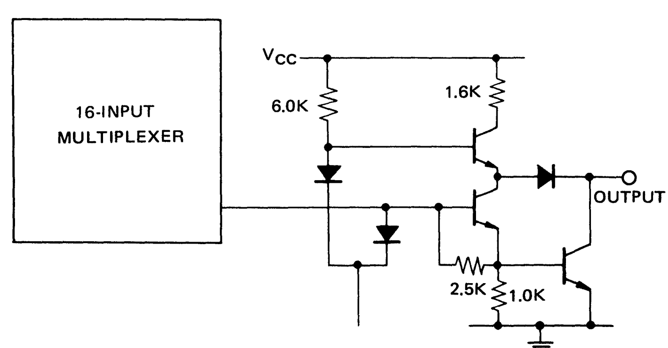
Fig. 5 — MB 7053 OUTPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7053 (3-state) compared to typically 3.0mA for the MB 7058 (open-collector).

Fig. 6 — MB 7058 OUTPUT



Bipolar Memories

TYPICAL OUTPUT/SWITCHING CHARACTERISTICS CURVES

Fig. 7 – I_{OL} OUTPUT LOW CURRENT VS V_{OL} OUTPUT LOW VOLTAGE

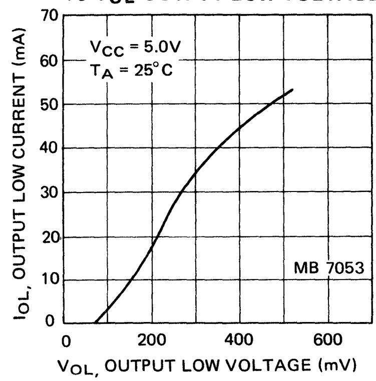


Fig. 8 – I_{OL} OUTPUT LOW CURRENT VS V_{OL} OUTPUT LOW VOLTAGE

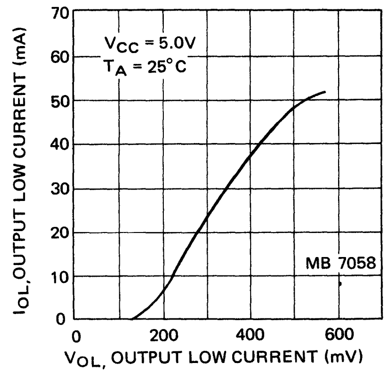


Fig. 9 – I_{OH} OUTPUT HIGH CURRENT VS V_{OH} OUTPUT HIGH VOLTAGE

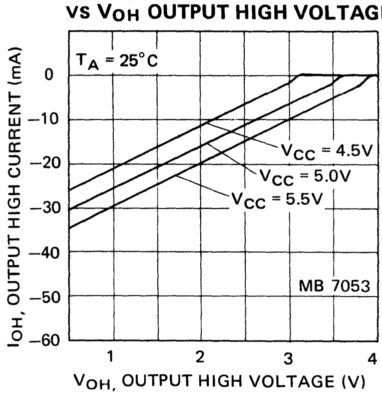


Fig. 10 – I_{OH} OUTPUT HIGH CURRENT VS V_{OH} OUTPUT HIGH VOLTAGE

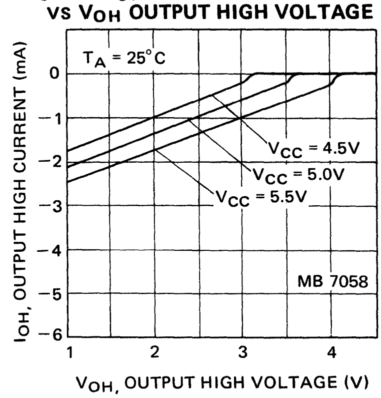


Fig. 11 – t_{AA} ACCESS TIME VS AMBIENT TEMPERATURE

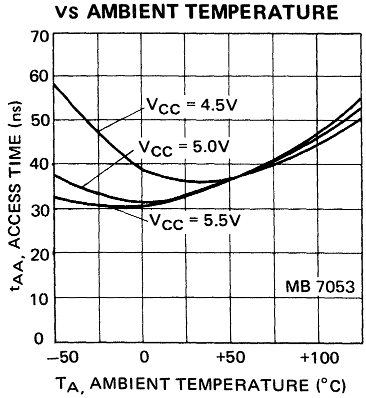


Fig. 12 – t_{AA} ACCESS TIME VS AMBIENT TEMPERATURE

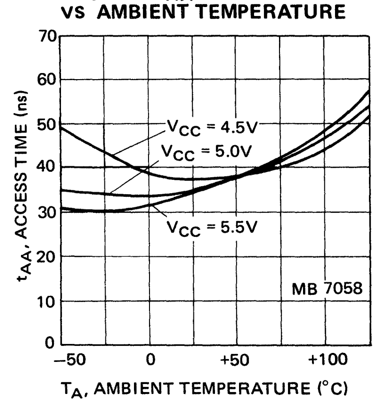


Fig. 13 — t_{DIS} DISABLE TIME VS AMBIENT TEMPERATURE

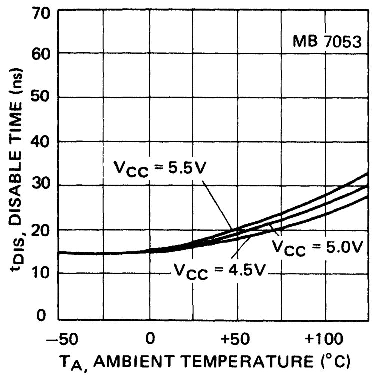


Fig. 14 — t_{DIS} DISABLE TIME VS AMBIENT TEMPERATURE

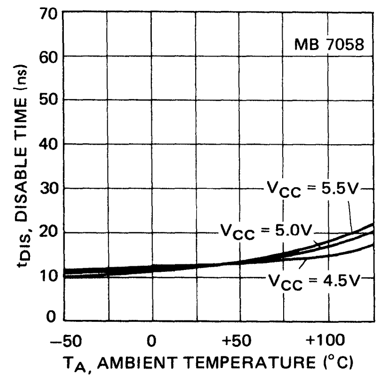


Fig. 15 — t_{EN} ENABLE TIME VS AMBIENT TEMPERATURE

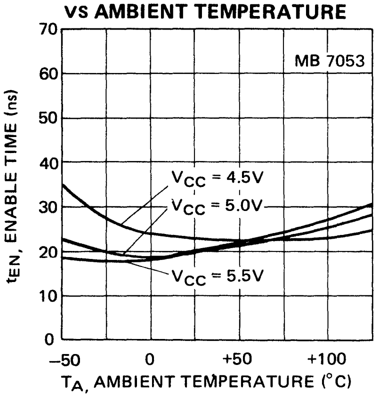


Fig. 16 — t_{EN} ENABLE TIME VS AMBIENT TEMPERATURE

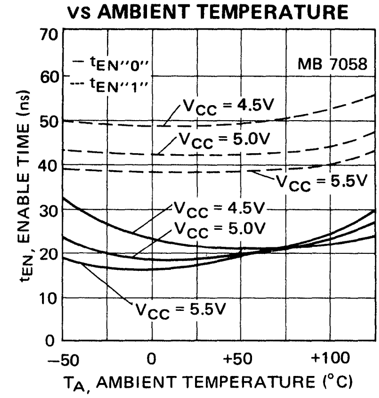


Fig. 17 — DELAY TIME INCREASE VS C_L LOAD CAPACITANCE

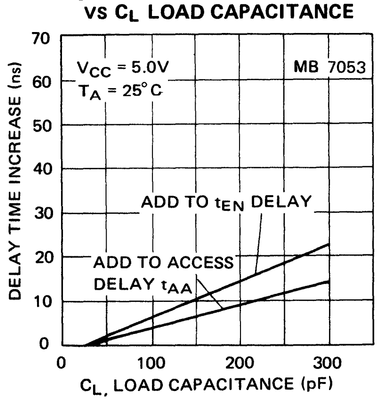
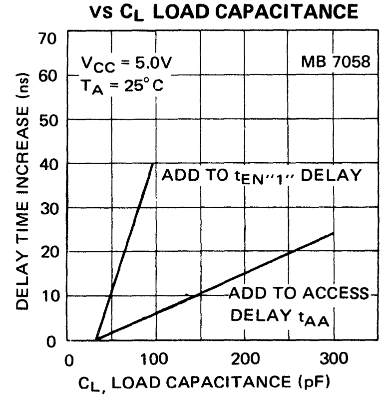


Fig. 18 — DELAY TIME INCREASE VS C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

Fujitsu's sophisticated Fine Emitter technology and programming pulse method enables higher programmability and faster programming time than ordinary PROMs, for the highest reliability.

Fast programming time of typically 10μs/bit is achieved with a fine emitter cell which requires less programming energy; thus, negligible thermal stress. Further, Fujitsu advanced technology allows very high programmability of typically 99%.

To assure that the element is programmed properly, an additional four programming pulses are applied immediately after a sense pulse indicates conduction in the programmed bit. This high reliability feature virtually eliminates aluminum migration in the programmed cell. The basic manufacturing process is a highly reliable gold doped TTL process.

SPECIAL FACTORY TESTING

One extra row and one extra column of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

Fig. 19 — PROGRAMMED CELL (CROSS SECTION)

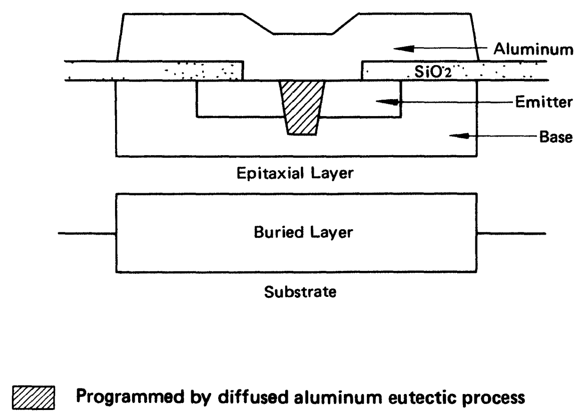
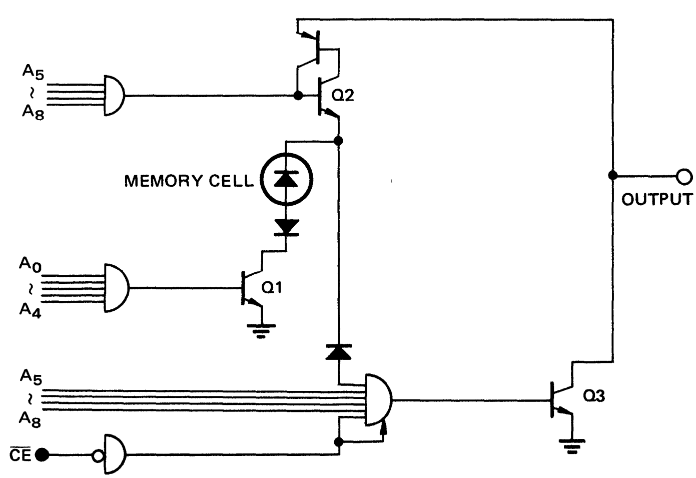


Fig. 20 — INTERNAL PROGRAMMING CIRCUIT



A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using eight address inputs to turn on transistors Q1 and Q2. By taking either (or both) chip enable inputs high, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the sensed voltage indicates that the selected bit is in the logic one state.

An additional 4 programming pulses are required to ensure that the bit is fully programmed, and to achieve high reliability.

One output must be programmed at a time, since the internal decording circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking both chip enable inputs low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA/MB7053 (400μA /MB7058) at V_{OH}=2.1V and V_{CC}= 4.35V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.25	V
Power Supply Voltage	V_{CC}	5.0	5.0	5.25	V
Programming Pulse Current	I_{PRG}	190	200	210	mA
Sense Pulse Current	I_{SNS}	19	20	21	mA
Programming Pulse Clamp Voltage	V_{PRG}	27.5	28.0	28.0	V
Sense Pulse Clamp Voltage	V_{SNS}	27.5	28.0	28.0	V
Sensed Voltage for a Programmed "1"	V_{REF}	6.9	7.0	7.1	V

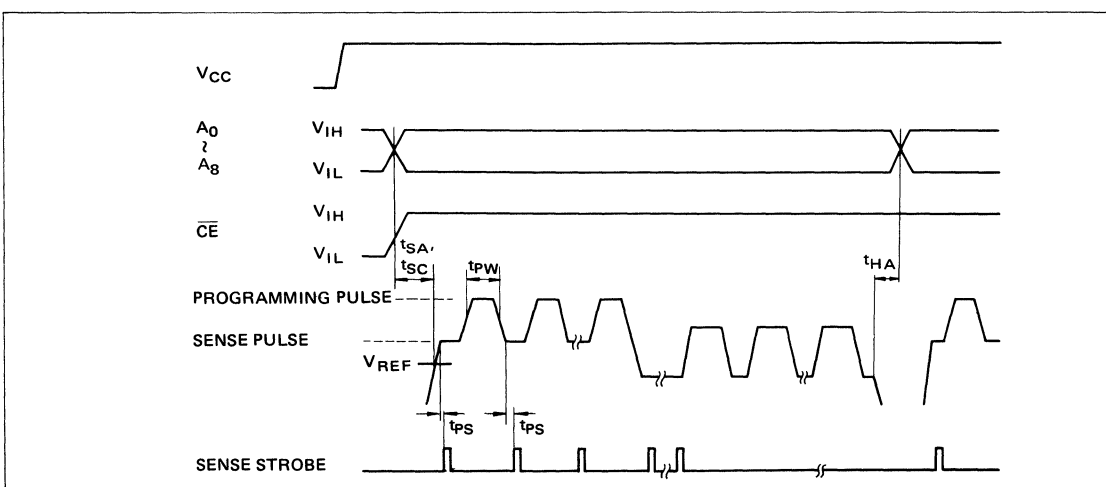
PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Duty Cycle	—	70	—	—	%
Programming Pulse Width	t_{PW}*	7.2	7.5	7.8	μs
Programming Pulse Ramp Rate (Rise)	—	50	—	70	V/μs
Programming Pulse Ramp Rate (Fall)	—	—	—	150	V/μs
Address Input Set-up Time	t_{SA}	500	—	—	ns
Chip Enable Input Set-up Time	t_{SC}	500	—	—	ns
Address Input Hold Time	t_{HA}	500	—	—	ns
Chip Enable Input Hold Time	t_{HC}	500	—	—	ns
Programming Pulse Trailing Edge to Sense Strobe Time	t_{PS}	700	—	—	ns
Programming Pulse Number	—	—	—	100	Time
Programming Time/Device	—	—	—	2048	ms
Additional Programming Pulse Number	—	4	4	4	Time

* Note: Stipulated at 150Ω load and 15V.

TYPICAL WAVEFORMS

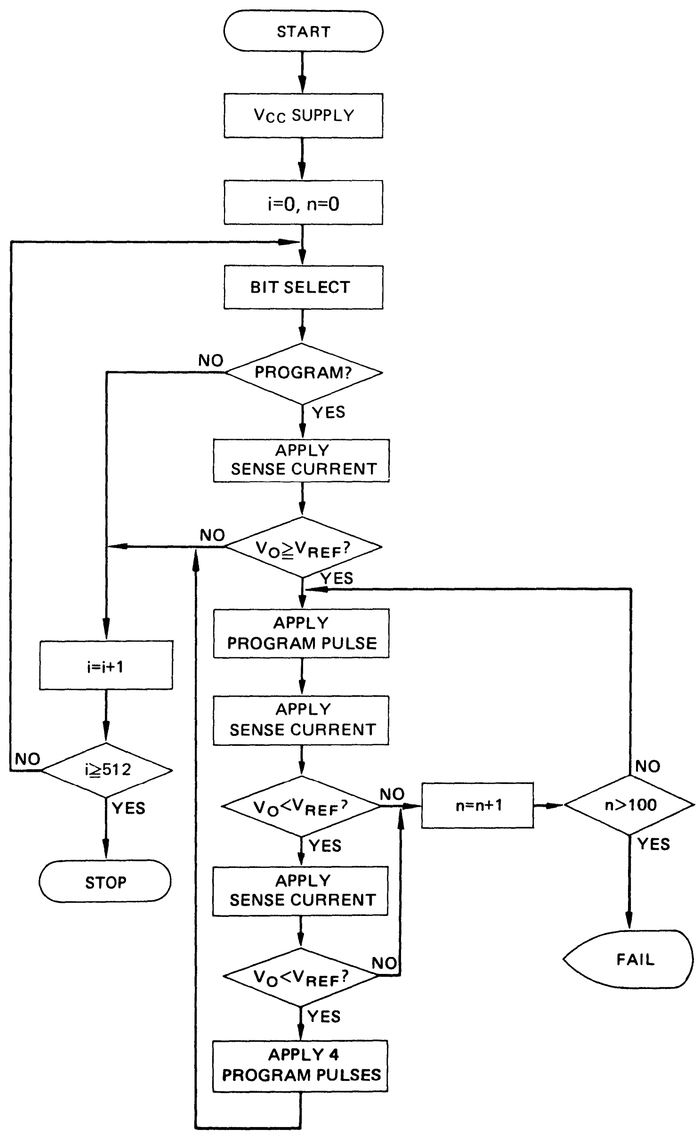


PROGRAMMING PROCEDURE

1. Apply the proper power; V_{CC} = 5.0V, GND = 0V
2. Select the desired word using nine address inputs.
3. Take either (or both) chip enable inputs high.
4. Apply 20mA sense current to the desired output after a delay of t_{SC}, and confirm that the output voltage "V_O" is higher than, or equal to, the sensed voltage "V_{REF}". (In the case of $V_O < V_{REF}$, select the next desired address after a delay of t_{HA}.)
5. Apply a programming pulse with amplitude of 200mA and duration of t_{PW}.
6. Apply the 20mA sense current and compare V_O with V_{REF} after a delay of t_{PS}.
   a) In the case of $V_O \geqq V_{REF}$, the selected bit is still in the logic ZERO state. Repeat steps "5" and "6".
   b) In the case of $V_O < V_{REF}$, the selected bit is then in the logic ONE state. Apply the sense current again, and confirm $V_O < V_{REF}$ after a delay of equal to (or greater than) t_{PW} without intervening with programming pulse. In the case of $V_O \geqq V_{REF}$, repeat step "5" and "6" again.
7. After confirmation of $V_O < V_{REF}$, apply four additional programming pulses. In the case of $V_O \geqq V_{REF}$, then, repeat steps "5" and "6", again. Select the next desired word after a delay of t_{HA}.

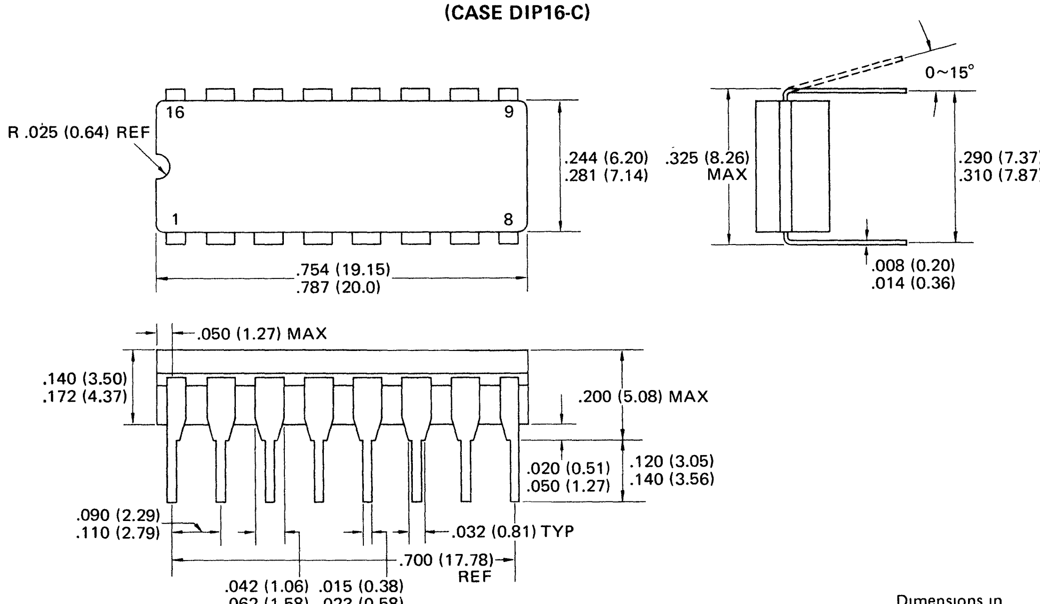
Note: 1) Sense current must be interrupted (= zero) during each address change.
2) Programming must be done bit by bit.
3) Ambient temperature during programming must be room temperature (25° ± 2°C).

Fig. 21 — PROGRAMMING FLOW CHART



Bipolar Memories

PACKAGE DIMENSIONS



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FUJITSU

PROGRAMMABLE 4096-BIT READ ONLY MEMORY

MB 7054 MB 7059

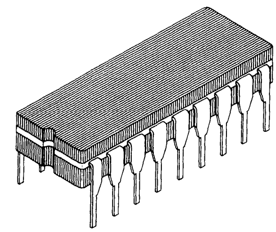
TTL 4096-BIT PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MB 7054 and MB 7059 are electrically field programmable, high-speed bipolar TTL 4096-bit read only memories organized as 1024 words by 4 bits. With three-state outputs provided on the MB 7054 and uncommitted collector outputs on the MB 7059, memory expansion is simple. Both devices have on-chip address decoding and chip enable, and they are fully compatible with both DTL and TTL circuits.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be electrically programmed in the selected bit locations at the rate of 10 μs/bit (typical).

Additional circuitry is built into the Fujitsu PROM chip to allow factory testing after packaging for AC, DC and programming parameters. The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform tests of key parameters prior to shipment. This results in extremely high programmability.

- 1024 words x 4 bits organization, fully decoded.
- High programmability of 99% typical (98% minimum)
- Programming by diffused aluminum eutectic process
- Ultra-fast programming time of 10 μs/bit (typical)
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques



CASE DIP18-C
CERAMIC PACKAGE

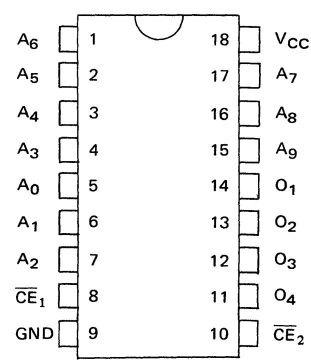
- Fast access time of 45 ns
- DTL/TTL compatible inputs and outputs
- Active pull-up (3-state) on MB 7054 or resistor pull-up (open-collector) on MB 7059
- Two chip enable ($\overline{CE}$) leads for simplified memory expansion
- Standard 18-pin DIP package
- Second-source available

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to Ground Pin	V_{CC}	-0.5 to + 7.0	V
Input Voltage	V_{IN}	-1.5 to + 5.5	V
Output Voltage	V_{OUT}	-0.5 to + 5.5	V
Output Voltage (during programming)	V_{PRG}	-0.5 to +28.5	V
Input Current	I_{IN}	- 20	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{PRG}	+220	mA
Temperature Under Bias	T_A	-25 to +125	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

PIN ASSIGNMENT



GUARANTEED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	—	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	—	V
Ambient Temperature	T_A	0	—	75	°C

DC CHARACTERISTICS

(Full guaranteed operating ranges unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}	—	—	60	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}	—	—	1.0	mA
Input Load Current (V_{IL} = 0.4V)		I_F	—	—	−0.5	mA
Output Low Voltage (I_{OL} = 16mA)		V_{OL}	—	—	0.45	V
Output Leakage Current (V_O = 5.5V, chip disabled)		I_{OIH}	—	—	40	μA
Output Leakage Current (V_O = 0.4V, chip disabled)		I_{OIL}	—	—	−40	μA
Input Clamp Voltage (I_{IN} = −10mA)		V_{IC}	—	—	−1.5	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}	—	—	130	mA
Output Leakage Current (V_O = 5.5V, chip enabled)		I_{OLK}*	—	—	100	μA
Output High Voltage (I_O = −2.4mA)	MB 7054	V_{OH}*	2.4	—	—	V
Output High Voltage (I_O = −0.4mA)	MB 7059	V_{OH}*	2.4	—	—	V
Output Short Circuit Current (V_O = GND)	MB 7054	I_{OS}*	−15	—	−60	mA
Output Short Circuit Current (V_O = GND)	MB 7059	I_{OS}*	−1.0	—	−6.0	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{I\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

CAPACITANCE (f = 1MHz; V_{CC} = +5V; V_{IN} = +2V; T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	—	—	10	pF
Output Capacitance	C_O	—	—	12	pF

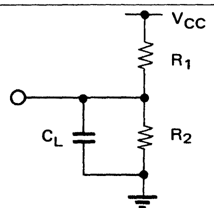


Fig. 1— AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude .... 0V to 3V
Rise and Fall Time .... 5ns from 1V to 2V
Frequency.................. 1 MHz

	MB7054			MB7059		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF	300Ω	600Ω	30pF
t_{DIS} "1"	∞	600Ω	10pF	∞	3.3KΩ	10pF
t_{DIS} "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t_{EN} "1"	∞	600Ω	30pF	∞	3.3KΩ	30pF
t_{EN} "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

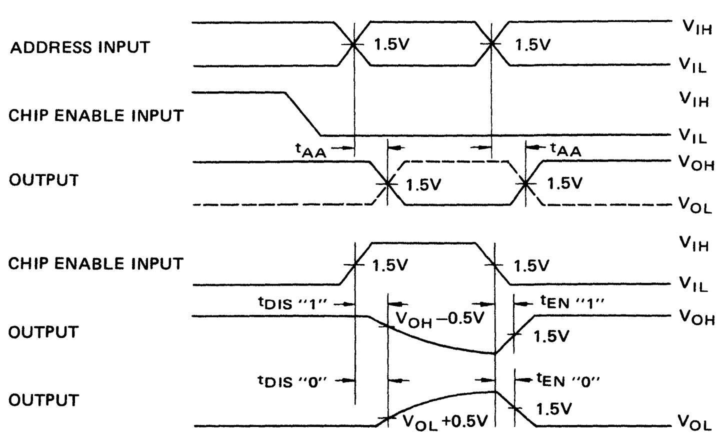
AC CHARACTERISTICS

(Full guaranteed operating ranges unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Access Time (via address input)	t_{AA}*	—	(45)	70	ns
Output Disable Time	t_{DIS}*	—	(16)	40	ns
Output Enable Time	t_{EN}*	—	(22)	40	ns

***Note:** Values in parenthesis denote conditions at $T_A = 25°C$.

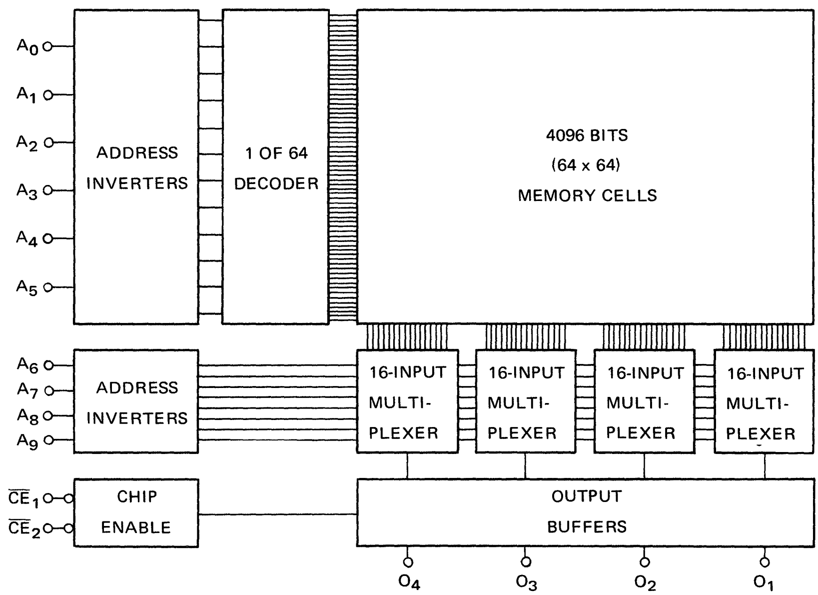
OPERATION TIMING DIAGRAM



Notes: 1) Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

2) t_{AA}, t_{DIS}"1" and t_{EN}"1" cannot be tested prior to programming, but are guaranteed by factory testing.

Fig. 2 – MB 7054/7059 BLOCK DIAGRAM



TYPICAL INPUT CHARACTERISTICS CURVES

Fig. 3 – I_{INA} INPUT CURRENT VS V_{IN} INPUT VOLTAGE

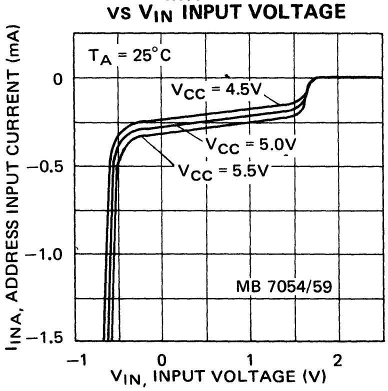
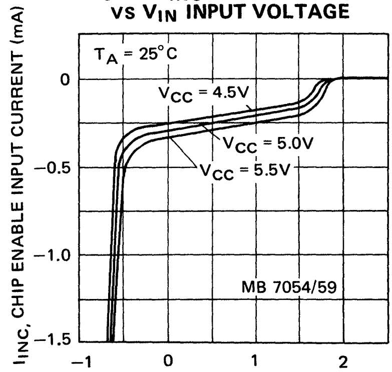


Fig. 4 – I_{INC} INPUT CURRENT VS V_{IN} INPUT VOLTAGE



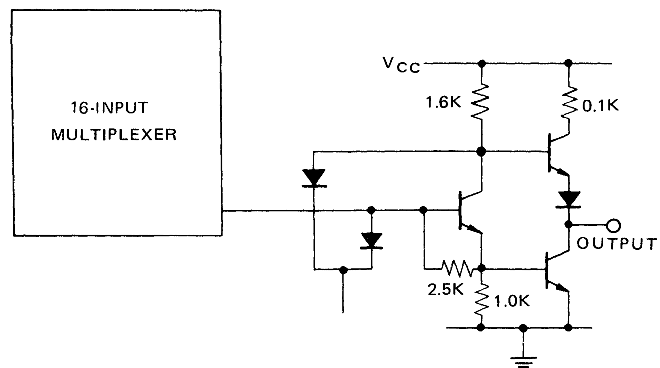
OUTPUT CIRCUIT INFORMATION

THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impendance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

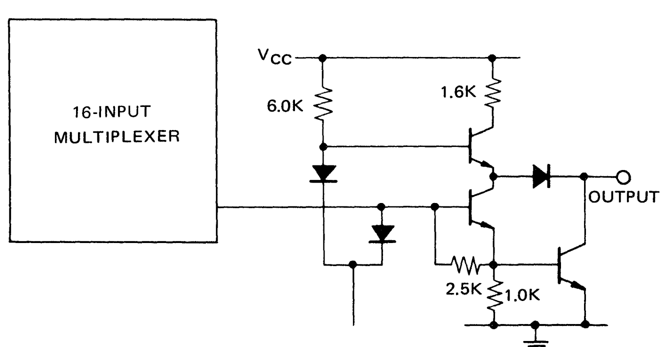
Fig. 5 – MB 7054 OUTPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7054 (3-state) compared to typically 3.0mA for the MB 7059 (open-collector).

Fig. 6 – MB 7059 OUTPUT



Bipolar Memories

TYPICAL OUTPUT/SWITCHING CHARACTERISTICS CURVES

Fig. 7 — I_{OL} OUTPUT LOW CURRENT VS V_{OL} OUTPUT LOW VOLTAGE

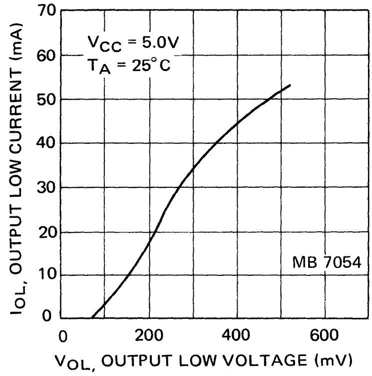


Fig. 8 — I_{OL} OUTPUT LOW CURRENT VS V_{OL} OUTPUT LOW VOLTAGE

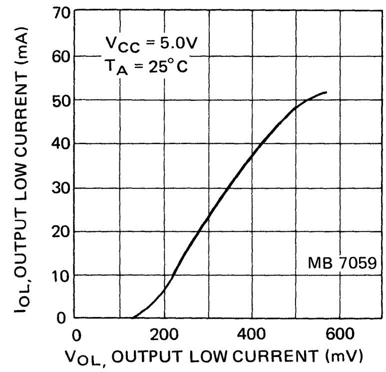


Fig. 9 — I_{OH} OUTPUT HIGH CURRENT VS V_{OH} OUTPUT HIGH VOLTAGE

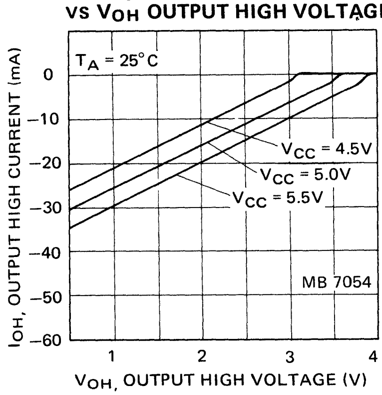


Fig. 10 — I_{OH} OUTPUT HIGH CURRENT VS V_{OH} OUTPUT HIGH VOLTAGE

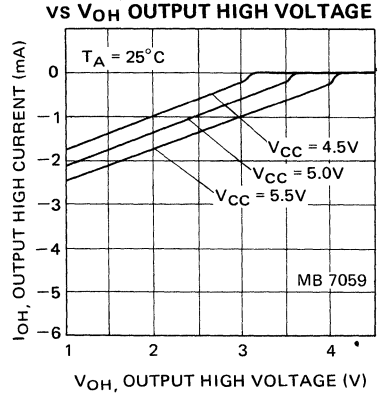


Fig. 11 — t_{AA} ACCESS TIME VS AMBIENT TEMPERATURE

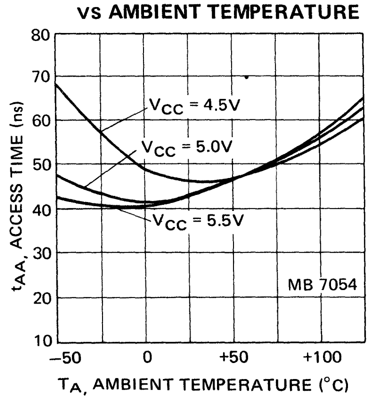


Fig. 12 — t_{AA} ACCESS TIME VS AMBIENT TEMPERATURE

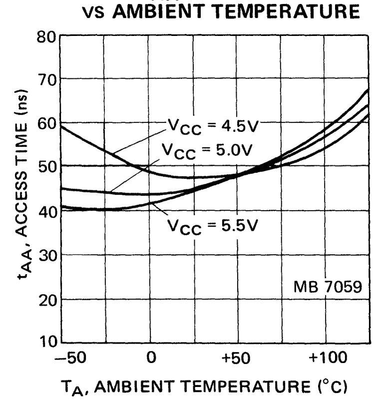


Fig. 13 — t_{DIS} DISABLE TIME VS AMBIENT TEMPERATURE

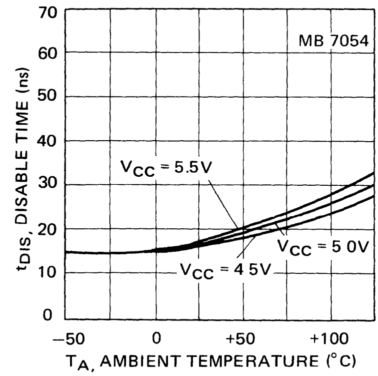


Fig. 14 — t_{DIS} DISABLE TIME VS AMBIENT TEMPERATURE

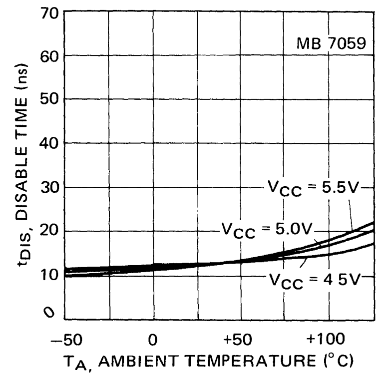


Fig. 15 — t_{EN} ENABLE TIME VS AMBIENT TEMPERATURE

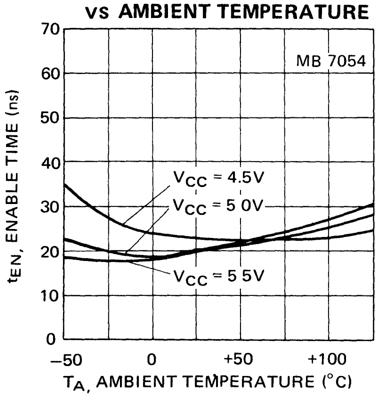


Fig. 16 — t_{EN} ENABLE TIME VS AMBIENT TEMPERATURE

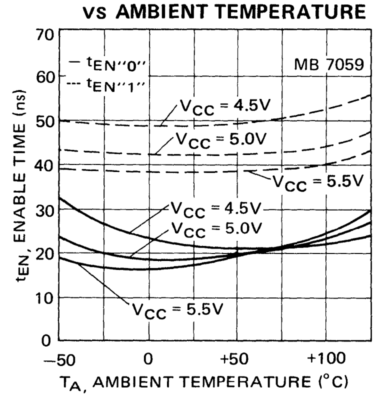


Fig. 17 — DELAY TIME INCREASE VS C_L LOAD CAPACITANCE

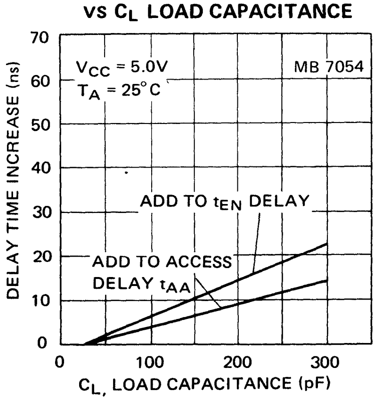
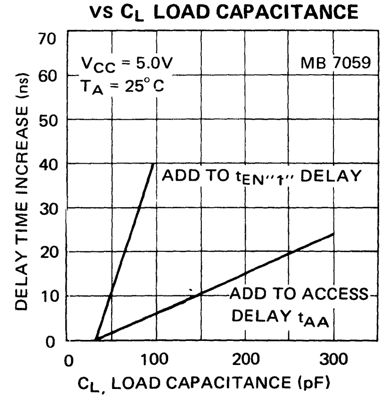


Fig. 18 — DELAY TIME INCREASE VS C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

Fujitsu's sophisticated Fine Emitter technology and programming pulse method enables higher programmability and faster programming time than ordinary PROMs, for the highest reliability.

Fast programming time of typically 10μs/bit is achieved with a fine emitter cell which requires less programming energy; thus, negligible thermal stress. Further, Fujitsu advanced technology allows very high programmability of typically 99%.

To assure that the element is programmed properly, an additional four programming pulses are applied immediately after a sense pulse indicates conduction in the programmed bit. This high reliability feature virtually eliminates aluminum migration in the programmed cell. The basic manufacturing process is a highly reliable gold doped TTL process.

SPECIAL FACTORY TESTING

One extra row and one extra column of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

Fig. 19 — PROGRAMMED CELL (CROSS SECTION)

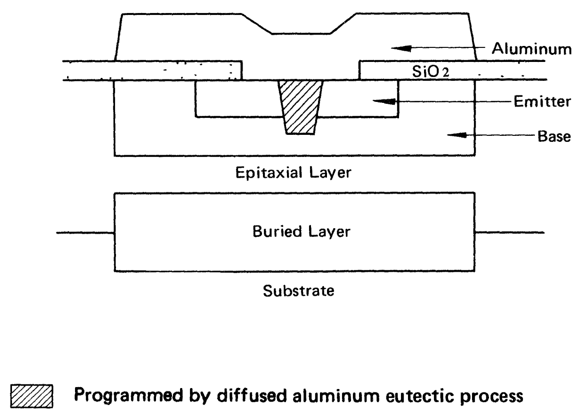
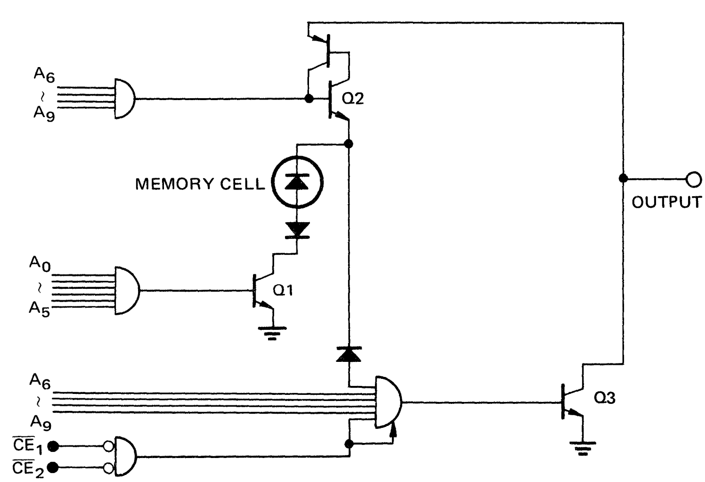


Fig. 20 — INTERNAL PROGRAMMING CIRCUIT



A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using eight address inputs to turn on transistors Q1 and Q2. By taking either (or both) chip enable inputs high, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the sensed voltage indicates that the selected bit is in the logic one state.

An additional 4 programming pulses are required to ensure that the bit is fully programmed, and to achieve high reliability.

One output must be programmed at a time, since the internal decording circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking both chip enable inputs low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA/MB7054 (400μA /MB7059) at V_{OH}=2.1V and V_{CC}= 4.35V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.25	V
Power Supply Voltage	V_{CC}	5.0	5.0	5.25	V
Programming Pulse Current	I_{PRG}	190	200	210	mA
Sense Pulse Current	I_{SNS}	19	20	21	mA
Programming Pulse Clamp Voltage	V_{PRG}	27.5	28.0	28.0	V
Sense Pulse Clamp Voltage	V_{SNS}	27.5	28.0	28.0	V
Sensed Voltage for a Programmed "1"	V_{REF}	6.9	7.0	7.1	V

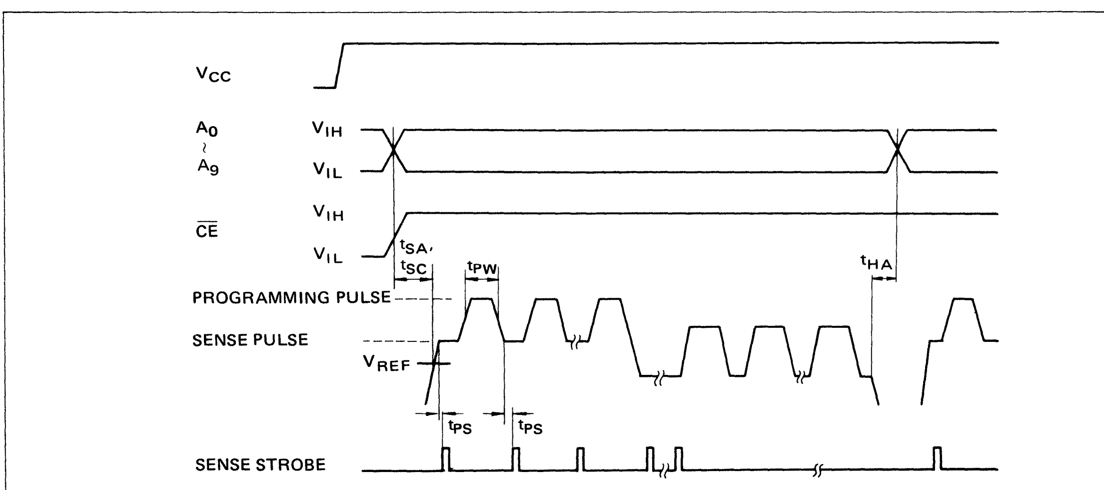
PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS ($T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Duty Cycle	—	70	—	—	%
Programming Pulse Width	t_{PW}*	7.2	7.5	7.8	µs
Programming Pulse Ramp Rate (Rise)	—	50	—	70	V/µs
Programming Pulse Ramp Rate (Fall)	—	—	—	150	V/µs
Address Input Set-up Time	t_{SA}	500	—	—	ns
Chip Enable Input Set-up Time	t_{SC}	500	—	—	ns
Address Input Hold Time	t_{HA}	500	—	—	ns
Chip Enable Input Hold Time	t_{HC}	500	—	—	ns
Programming Pulse Trailing Edge to Sense Strobe Time	t_{PS}	700	—	—	ns
Programming Pulse Number	—	—	—	100	Time
Programming Time/Device	—	—	—	4096	ms
Additional Programming Pulse Number	—	4	4	4	Time

* Note: Stipulated at 150Ω load and 15V.

TYPICAL WAVEFORMS

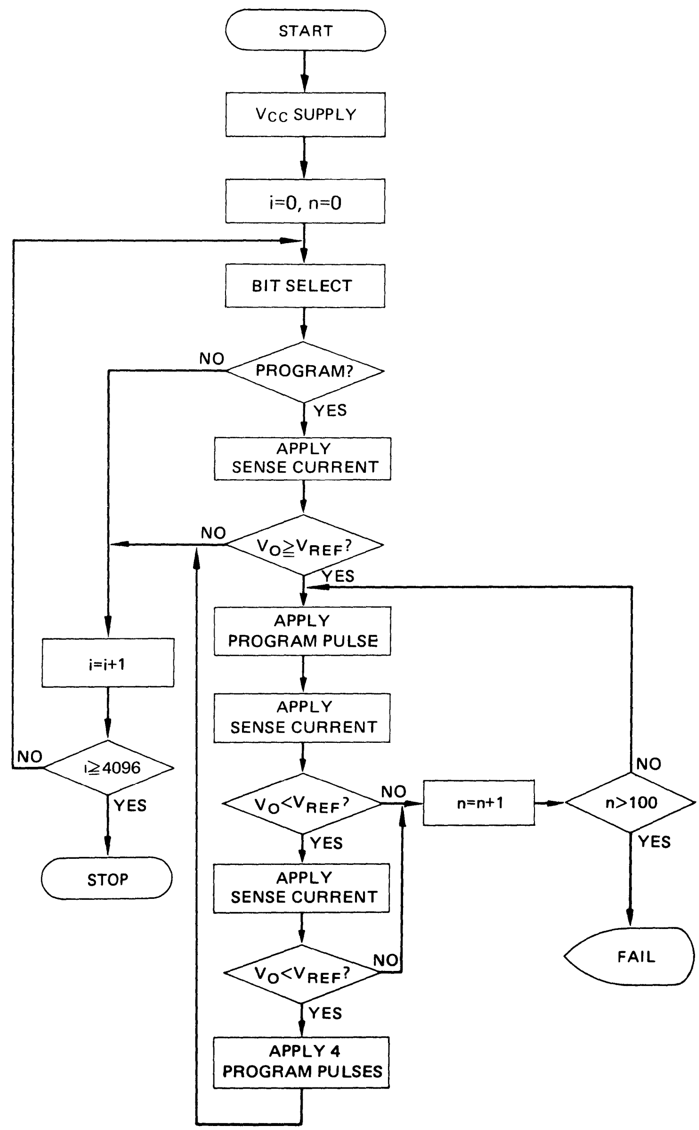


PROGRAMMING PROCEDURE

1. Apply the proper power; V_{CC} = 5.0V, GND = 0V
2. Select the desired word using ten address inputs.
3. Take either (or both) chip enable inputs high.
4. Apply 20mA sense current to the desired output after a delay of t_{SC}, and confirm that the output voltage "V_O" is higher than, or equal to, the sensed voltage "V_{REF}". (In the case of $V_O < V_{REF}$, select the next desired address after a delay of t_{HA}.)
5. Apply a programming pulse with amplitude of 200mA and duration of t_{PW}.
6. Apply the 20mA sense current and compare V_O with V_{REF} after a delay of t_{PS}.
   a) In the case of $V_O \geq V_{REF}$, the selected bit is still in the logic ZERO state. Repeat steps "5" and "6".
   b) In the case of $V_O < V_{REF}$, the selected bit is then in the logic ONE state. Apply the sense current again, and confirm $V_O < V_{REF}$ after a delay of equal to (or greater than) t_{PW} without intervening with programming pulse. In the case of $V_O \geq V_{REF}$, repeat step "5" and "6" again.
7. After confirmation of $V_O < V_{REF}$, apply four additional programming pulses. In the case of $V_O \geq V_{REF}$, then, repeat steps "5" and "6", again. Select the next desired word after a delay of t_{HA}.

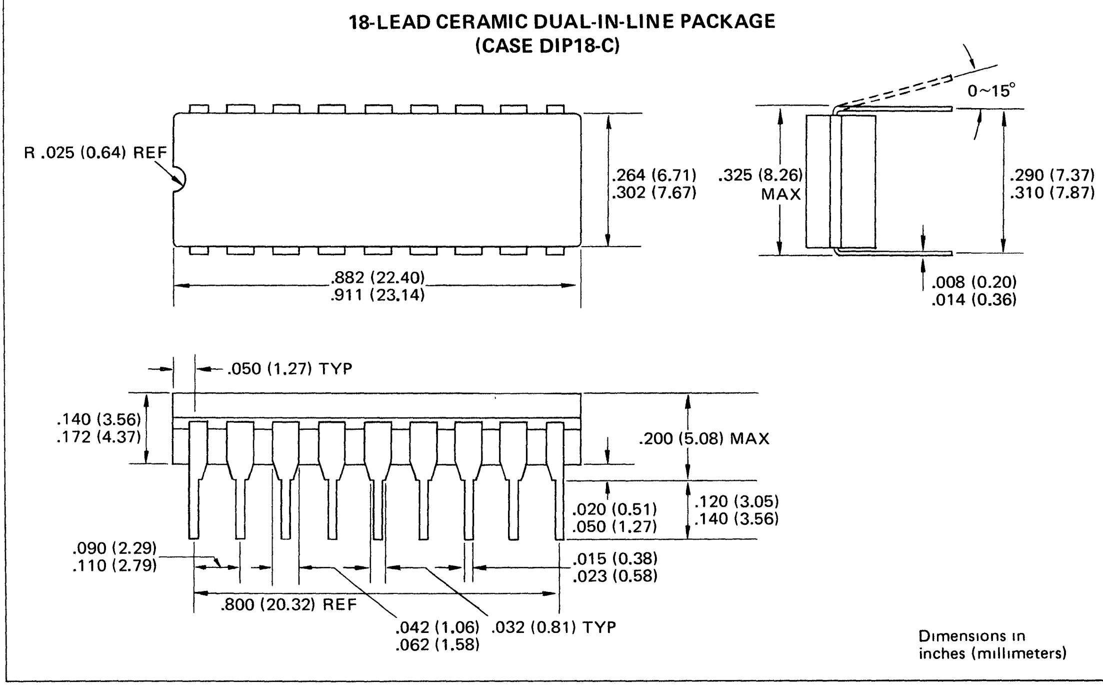
Note: 1) Sense current must be interrupted (= zero) during each address change.
2) Programming must be done bit by bit.
3) Ambient temperature during programming must be room temperature (25° ± 2°C).

Fig. 21 — PROGRAMMING FLOW CHART



Bipolar Memories

PACKAGE DIMENSIONS



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FUJITSU

PROGRAMMABLE 8192-BIT READ ONLY MEMORY

MB 7055
MB 7060

8192-BIT READ ONLY MEMORY

The Fujitsu MB7055 is an electrically field programmable, high-speed/low-power bipolar TTL 8192-bit read only memory housed in a 24-pin dual-in-line package. It is a direct plug-in replacement for MOS 8K bit EPROMs. With two chip enable inputs and 3-state outputs, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be electrically programmed in the selected bit locations at the rate of 10 μs/bit (typical).

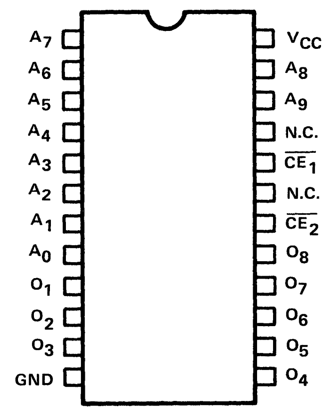
Additional circuitry is built into the Fujitsu PROM chip to allow factory testing after packaging for AC, DC and programming parameters. The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform tests of key parameters prior to shipment. This results in extremely high programmability.

- +5V single power supply
- 1024 x 8 bits organization, fully decoded
- High programmability of 96% typical
- Programming by diffused aluminum eutectic process
- Ultra-fast programming time of 10 μs/bit (typical)
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques
- Fast access time of 150 ns typical
- Small power dissipation of 0.04 mW/bit typical
- DTL/TTL compatible inputs and output
- Standard 24-pin DIP package
- Pin-to-pin compatible with MB8518 and Intel 2708

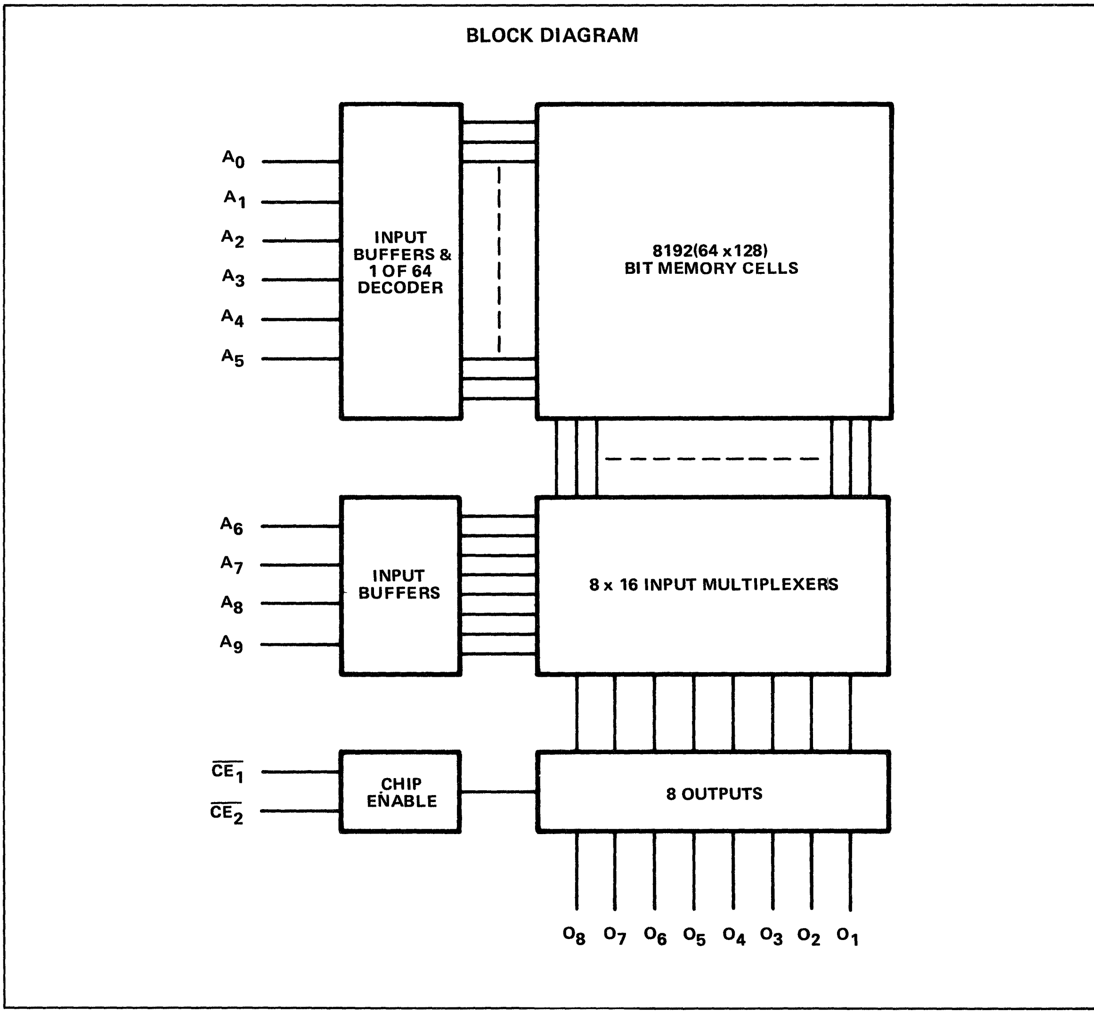
PROGRAMMING

The MB7055 can be programmed using same specification as used for the MB7052/IM5623, MB7057/IM5603, MB7053/IM5624, MB7058/IM5604, MB7054 and MB7059.

PIN ASSIGNMENT



TOP VIEW



ELECTRICAL CHARACTERISTICS

COMMERCIAL GRADE
$T_A = 0°C$ to $+75°C$, $V_{CC} = 5V \pm 5\%$

$I_{IL} = -0.18$ mA max.: $V_I = 0.4V$
$I_{IH} = 60\ \mu A$ max.: $V_I = 4.5V$
$V_{IH} = 2V$ min.: $V_{IL} = 0.8V$ max.
$V_{IC} = -1.5V$ max.: $I_I = -10$ mA
$I_{CC} = 70$ mA typ.: 100 mA max.

$V_{OL} = 0.45V$ max.: $I_O = 3.6$ mA
$V_{OH} = 2.4V$ min.: $I_O = -1.0$ mA
$I_{OIH} = 40\ \mu A$ max.: $V_O = 5.5V$
$I_{OIL} = -40\ \mu A$ max.: $V_O = 0.4V$
$I_{OLK} = 100\ \mu A$ max.: $V_O = 5.5V$

$I_{OS} = -3$ mA min.: -15 mA max.
$C_{IN} = 10$ pF max.: $C_{OUT} = 12$ pF max.
$t_{AA} = 150$ ns typ.: 250 ns max.
$t_{AC} = 60$ ns typ.: 150 ns max.

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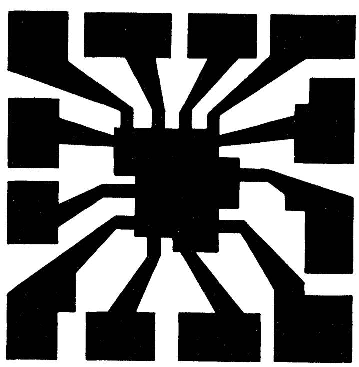
Interface Devices



FUJITSU

QUADRUPLE TTL TO MOS LEVEL SHIFTER/DRIVER

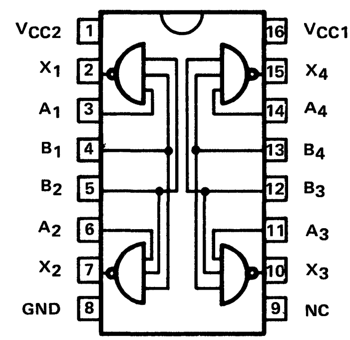
MB 8901

QUADRUPLE TTL TO MOS LEVEL SHIFTER/DRIVER

The MB 8901 is a level shifter from TTL/DTL level input to MOS level output, and also a high-speed clock driver. Using Schottky barrier diodes and PNP transistors in the circuit, the power dissipation is remarkably reduced without degradation of switching speed.

- High speed: 23 ns (t_{PLH} @ 300 pF)
- Wide operating range of V_{CC2}: variable output voltage (+9V to +17V)
- Low power dissipation
  50 mW for output low state
  70 mW for output high state
  (stand by power per circuit)
- TTL or DTL compatible inputs
- Standard 16-leads dual-in-line ceramic package

PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage*	V_{CC1}	+ 7	V
Supply Voltage*	V_{CC2}	+23	V
Input Voltage*	V_{IN}	-0.5 to 5.5	V
Operating Free-Air Temperature	T_{op}	-25 to +100	°C
Storage Temperature	T_{stg}	-65 to +150	°C

*These voltage values are with respect to GND lead.

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

RECOMMENDED OPERATING CONDITION

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC1}	5.0 ± 5%	V
Supply Voltage	V_{CC2}	9.0 to 17	V
Operating Free-Air Temperature	T_{op}	0 to +70	°C

DC CHARACTERISTICS

(T_A = 0°C ~ 70°C unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	V_{IL} = 0.8V I_{OUT} = −0.1 mA	V_{CC2} −0.5	V_{CC2} −0.3		V
Output Low Voltage	V_{OL}	V_{IH} = 2.0V V_{CC1} = 4.75V V_{CC2} = 16.8V I_{OUT} = 0.1 mA		0.35	0.6	V
Input Low Current (Input A)	I_{IL}(A)	V_{IL} = 0.4V V_{CC1} = 5.25V V_{CC2} = 16.8V		−1.0	−1.6	mA
Input Low Current (Input B)	I_{IL}(B)	same as above		−2.0	−3.2	mA
Input High Current (Input A)	I_{IH}(A)	V_{IH} = 2.4V			40	μA
Input High Current (Input B)	I_{IH}(B)	V_{IH} = 2.4V			80	μA
Operating Supply Voltage of V_{CC2}	V_{CC2}		9.0		17	V
Supply Current (Output Low) (*1)	I_{CC1L}	V_{CC1} = 5.25V V_{CC2} = 16.8V I_{IH} = 5.25V T_A = 25°C		40	60	mA
	I_{CC2L}	same as above		0.2	0.5	mA
Supply Current (Output High) (*2)	I_{CC1H}	V_{CC1} = 5.25V V_{CC2} = 16.8V V_{IL} = 0V T_A = 25°C		26	40	mA
	I_{CC2H}	same as above		10	16	mA

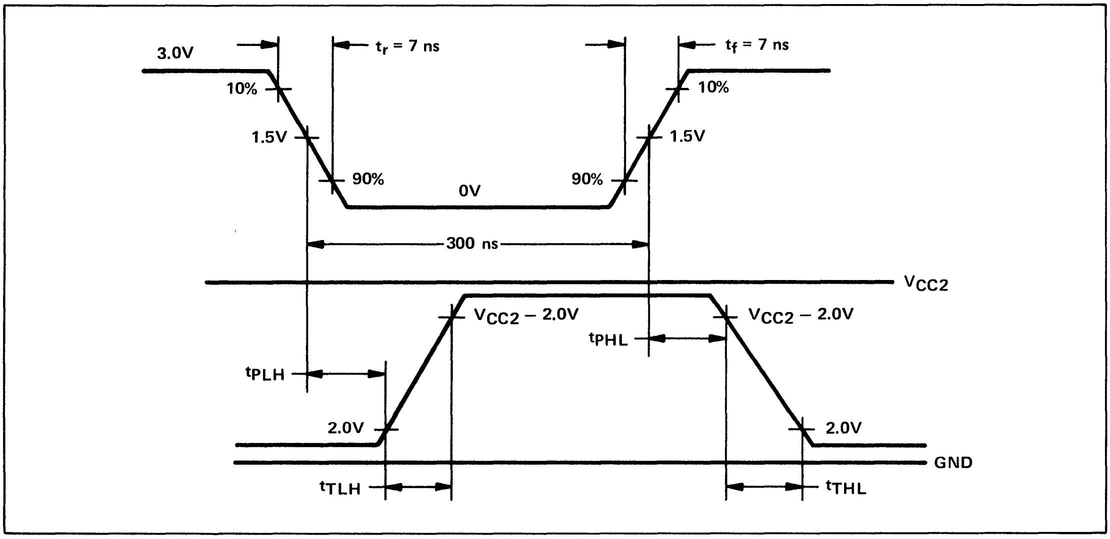
(*1) The typical values are applicable for V_{CC1} = 5.0V, V_{CC2} = 16.0V, T_A = 25°C.
(*2) These values are total current for a package.

AC CHARACTERISTICS

(T_A = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input to Output Delay	t_{PLH}	V_{CC1} = 5.0V V_{CC2} = 16.0V C_L = 300 pF	10	18	23	ns
Input to Output Delay	t_{PHL}	same as above	7	14	20	ns
Output Rise Time	t_{TLH}	V_{CC1} = 5.0V V_{CC2}= 16.0V C_L = 300 pF	12	21	30	ns
Output Fall Time	t_{THL}	same as above	12	22	30	ns
$t_{PHL} + t_{THL}$	t_{DHL}	same as above	20	36	45	ns
$t_{PLH} + t_{TLH}$	t_{DLH}	same as above	25	40	50	ns

WAVEFORMS



POWER CONSIDERATION

The total power dissipation of the MB 8901 is given as

$$P_T = n(P_{CC1} + P_{CC2}) + C_L V_{CC2}^2 f + (4 - n)P_{ST} \quad (1)$$

Interface Devices

where,

n = The number of circuits operating at frequency f,
P_{ST} = DC power dissipation per circuit,
$C_L V_{CC2}^2 f$ = The power required for charging and discharging load capacitance,
f = The frequency of switching,
C_L = The total load capacitance.

P_{CC1} and P_{CC2} are expressed as below,

$$P_{CC1} = \theta P_{STH1} + (1-\theta)P_{STL1} + K_1(f) \tag{2}$$

$$P_{CC2} = \theta P_{STH2} + (1-\theta)P_{STL2} + K_2(f) \tag{3}$$

where,

P_{CC1} = The power supplied from V_{CC1} when the circuit is operating with no load capacitance,
P_{CC2} = The power supplied from V_{CC2} when the circuit is operating with no load capacitance,
P_{STH1} = The DC component of P_{CC1} when output is High,
P_{STL1} = The DC component of P_{CC1} when output is Low,
P_{STH2} = The DC component of P_{CC2} when output is High,
P_{STL2} = The DC component of P_{CC2} when output is Low,
θ = Duty ratio,
$K_1(f)$ = The AC component of P_{CC1},
$K_2(f)$ = The AC component of P_{CC2}.

Assuming that

$$P_{STH} = P_{STH1} + P_{STH2} \tag{4}$$

$$P_{STL} = P_{STL1} + P_{STL2} \tag{5}$$

where,

P_{STH} = The DC power dissipation when output is High,
P_{STL} = The DC power dissipation when output is Low.

Then, substitution of Eqs. (2), (3), (4), (5) into Eq. (1) yields,

$$P_T = n[\theta\, P_{STH} + (1-\theta)P_{STL} + K_1(f) + K_2(f)] + C_L V_{CC2}^2\, f + (4-n)P_{ST} \tag{6}$$

On the other hand, each component of DC power per circuit can be obtained as follows.

$$P_{STL1} = (I_{CC1L}/4)\ V_{CC1} \tag{7}$$

$$P_{STL2} = (I_{CC2L}/4)\ V_{CC2} \tag{8}$$

$$P_{STH1} = (I_{CC1H}/4)\ V_{CC1} \tag{9}$$

$$P_{STH2} = (I_{CC2H}/4)\ V_{CC2} \tag{10}$$

The typical and maximum values of I_{CC1L}, I_{CC2L}, I_{CC1H} and I_{CC2H} are shown in the specification table.

For example, we calculate each value of Eqs. (1) to (10) in the case of duty ratio θ = 50%.

Items	Typ.	Max.	Items	Typ.	Max.
V_{CC1}	5.0V	5.25V	V_{CC2}	16.0V	16.8V
I_{CC1L}/PKG	40 mA	60 mA	I_{CC2L}/PKG	0.2 mA	0.5 mA
I_{CC1H}/PKG	26 mA	40 mA	I_{CC2H}/PKG	10 mA	16 mA
P_{STL1}/CCT	50 mW	78.8 mW	P_{STL2}/CCT	0.8 mW	2.1 mW
P_{STH1}/CCT	32.5 mW	52.5 mW	P_{STH2}/CCT	40 mW	67.2 mW
P_{STL}/CCT	50.8 mW	80.9 mW	P_{STH}/CCT	72.5 mW	119.7 mW
P_{CC1}/CCT	41.2 + K_1(f) mW	65.6 + K_1(f) mW	P_{CC2}/CCT	20.4 + K_2(f) mW	34.6 + K_2(f) mW

	Total Power Dissipation
Typ.	$P_T = n[41.2 + K_1(f) + 20.4 + K_2(f)] + C_L V_{CC2}^2 f + (4 - n)P_{ST}$
Max.	$P_T = n[65.6 + K_1(f) + 34.6 + K_2(f)] + C_L V_{CC2}^2 f + (4 - n)P_{ST}$

We should estimate P_T in the case of $P_{ST} = P_{STL}$ and in the case of $P_{ST} = P_{STH}$.

The Eq. of P_T can be reduced as shown in the table below, assuming $K_1(f) = 0$ because P_{CC1} hardly depends on the frequency.

Items	P_{ST}	Total Power Dissipation
Typ.	P_{STL}	$P_T = n[61.6 + K_2(f)] + C_L(16)^2 f + 50.8(4 - n)$
Max.		$P_T = n[100.2 + K_2(f)] + C_L(16.8)^2 f + 80.9(4 - n)$
Typ.	I_{STH}	$P_T = n[61.6 + K_2(f)] + C_L(16)^2 f + 72.5(4 - n)$
Max.		$P_T = n[100.2 + K_2(f)] + C_L(16.8)^2 f + 119.7(4 - n)$

The values of the $K_2(f)$ can be calculated by substracting $P_{ST2}[= 1/2(P_{STH2} + P_{STL2})]$ from P_{CC2} in Fig. 1.

The total power dissipation should be restricted by the upper limit of the junction temperature and the thermal resistance of the package. The maximum load capacitance of one package or of one circuit is determined from the current capability of lead wire. Thus, the load capacitance must be limited by two factors that are power dissipation and current density of lead wire. For the MB 8901 these limits are shown as below.

Total Power Dissipation/PKG . . . . Max. 600 mW

Total Load Capacitance/PKG . . . . Max. 1000 pF

Load Capacitance/CCT . . . . Max. 600 pF

The maximum total load capacitance of MB 8901 (which contains four circuits in a package) can be derived by substituting these limits to the Eqs. of P_T (corresponding to each frequency of switching). The result of the calculation in the case of n = 4 is shown in Fig. 2.

Besides, we can obtain the maximum total load capacitance of any duty ratio by applying $[\theta P_{STH} + (1 - \theta)P_{STL}]$ for P_{ST}.

Fig. 1—P_{CC1} AND P_{CC2} VS. FREQUENCY OF SWITCHING

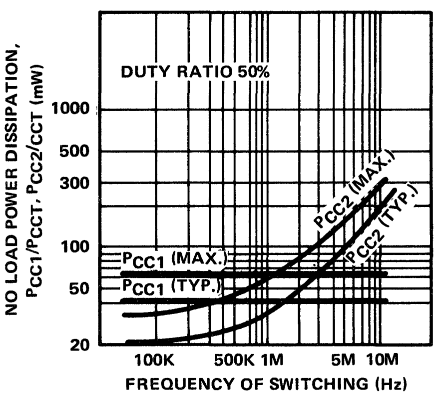
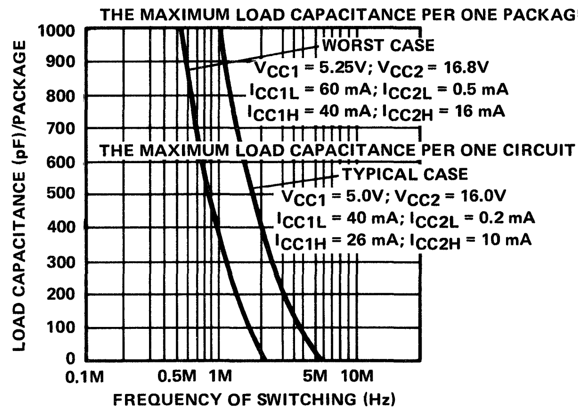


Fig. 2—THE MAXIMUM LOAD CAPACITANCE VS. FREQUENCY



FUJITSU

(QUADRUPLE TTL TO MOS LEVEL SHIFTER/DRIVER) ((AND.function))

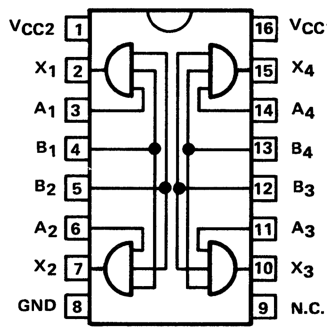
MB 8902

QUADRUPLE TTL TO MOS LEVEL SHIFTER/DRIVER (AND FUNCTION)

The MB8902 is a level shifter from TTL/DTL level input to MOS level output, and also a high speed clock driver. Using Schottky barrier diodes and PNP transistors in the circuit, the power dissipation is remarkably reduced without degradation of switching speed.

- High speed: 23 ns max. (t_{PLH} @ 300 pF)
- Wide operating range of V_{CC2}: Variable output voltage (9V to 17V)
- Low power dissipation:
  40 mW for output low state
  40 mW for output high state
  (Stand by power/circuit, @ V_{CC2} = 12V)
- TTL or DTL compatible inputs
- Standard ceramic 16-leads dual-in-line package

PIN ASSIGNMENT



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (*1)	V_{CC1}	7	V
Supply Voltage (*1)	V_{CC2}	23	V
Input Voltage (*1)	V_I	-0.5 to +5.5	V
Operating Free-Air Temperature Range	T_{op}	-25 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(*1) These voltage values are with respect to GND lead.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC1}	5.0 ± 5%	V
Supply Voltage	V_{CC2}	9.0 to 17	V
Operating Free-Air Temperature Range	T_{op}	0 to +70	°C

DC CHARACTERISTICS

($T_A = 0°C \sim 70°C$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	$V_{IH} = 2.0V$ $I_{OUT} = -0.1$ mA	V_{CC2} −0.5	V_{CC2} −0.3		V
Output Low Voltage	V_{OL}	$V_{IL} = 0.8V$ $V_{CC1} = 4.75V$ $V_{CC2} = 12.6V$ $I_{OUT} = 0.1$ mA		0.35	0.6	V
Input Low Current (Input A)	I_{IL} (A)	$V_{IL} = 0.4V$ $V_{CC1} = 5.25V$ $V_{CC2} = 12.6V$		−1.0	−1.6	mA
Input Low Current (Input B)	I_{IL} (B)	Same as above		−2.0	−3.2	mA
Input High Current (Input A)	I_{IH} (A)	$V_{IH} = 2.4V$			40	μA
Input High Current (Input B)	I_{IH} (B)	$V_{IH} = 2.4V$			80	μA
Operating Supply Voltage of V_{CC2}	V_{CC2}		9.0		17	V
Supply Current (Output Low)(*1)	I_{CC1L}	$V_{CC1} = 5.25V$ $V_{CC2} = 12.6V$ $V_{IL} = 0V$ $T_A = 25°C$		30	50	mA
	I_{CC2L}	Same as above		0.2	0.5	mA
Supply Current (Output High)(*1)	I_{CC1H}	$V_{CC1} = 5.25V$ $V_{CC2} = 12.6V$ $V_{IH} = 5.25V$ $T_A = 25°C$		16	30	mA
	I_{CC2H}	Same as above		10	16	mA

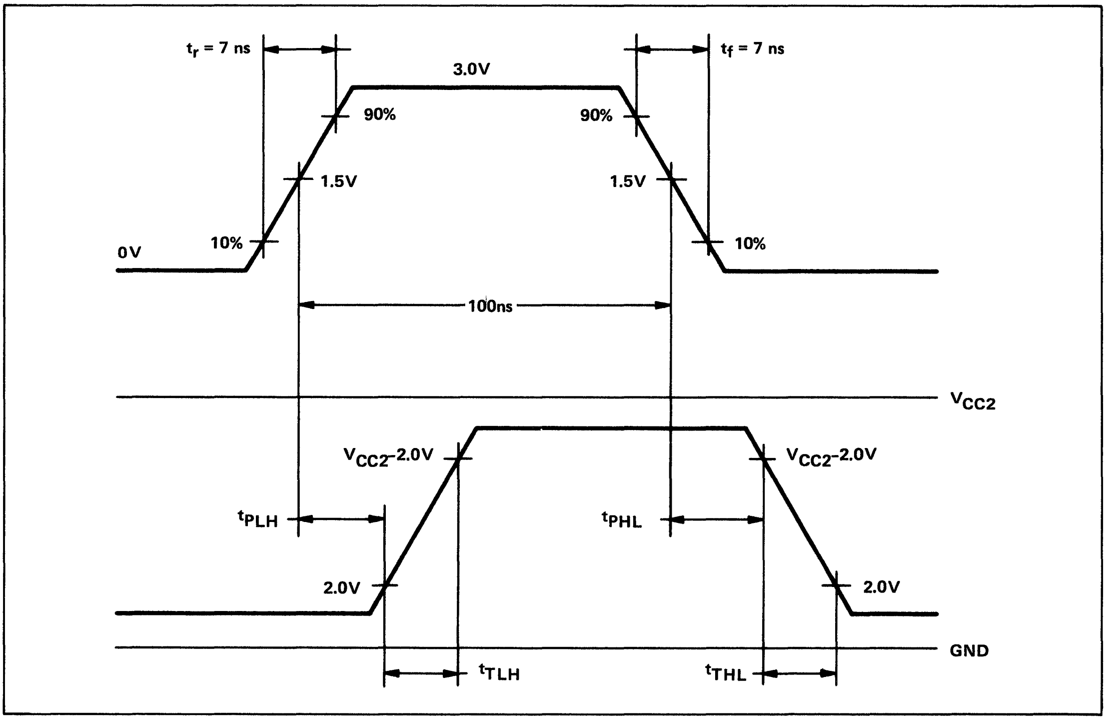
(*1) The typical values are applicable for $V_{CC1} = 5.0V$, $V_{CC2} = 12.0V$, $T_A = 25°C$.
(*2) These values are total current for a package.

AC CHARACTERISTICS

(T_A = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input to Output Delay	t_{PLH}	V_{CC1} = 5.0V V_{CC2} = 12.0V C_L = 300 pF	7	16	23	ns
Input to Output Delay	t_{PHL}	Same as above	7	15	20	ns
Output Rise Time	t_{TLH}	V_{CC1} = 5.0V V_{CC2} = 12.0V C_L = 300 pF	7	15	25	ns
Output Fall Time	t_{THL}	Same as above	7	16	25	ns
$t_{PLH} + t_{TLH}$	t_{DLH}	Same as above	20	31	45	ns
$t_{PHL} + t_{THL}$	t_{DHL}	Same as above	15	31	40	ns

WAVEFORMS



POWER CONSIDERATION

The total power dissipation of the MB 8902 is given as

$$P_T = n(P_{CC1} + P_{CC2}) + C_L V_{CC2}^2 f + (4 - n)P_{ST} \quad (1)$$

where,

n: The number of circuits operating at frequency f.
P_{ST}; DC power dissipation per circuit.
$C_L V_{CC2}^2 f$: The power required for charging and discharging load capacitance.
f: The frequency of switching.
C_L: The total load capacitance.

P_{CC1} and P_{CC2} are expressed as below,

$$P_{CC1} = \theta P_{STH1} + (1 - \theta)P_{STL1} + K_1(f) \quad (2)$$

$$P_{CC2} = \theta P_{STH2} + (1 - \theta)P_{STL2} + K_2(f) \quad (3)$$

where,

P_{CC1}: The power supplied from V_{CC1} when the circuit is operating with no load capacitance.
P_{CC2}: The power supplied from V_{CC2} when the circuit is operating with no load capacitance.
P_{STH1}: The DC component of P_{CC1} when output is High.
P_{STL1}: The DC component of P_{CC1} when output is Low.
P_{STH2}: The DC component of P_{CC2} when output is High.
P_{STL2}: The DC component of P_{CC2} when output is Low.
θ: Duty ratio.
$K_1(f)$: The AC component of P_{CC1}.
$K_2(f)$: The AC component of P_{CC2}.

Assuming that

$$P_{STH} = P_{STH1} + P_{STH2} \quad (4)$$

$$P_{STL} = P_{STL1} + P_{STL2} \quad (5)$$

where,

P_{STH}: The DC power dissipation when output is High.
P_{STL}: The DC power dissipation when output is Low.

Then, substitution of Eqs. (2), (3), (4), (5) into Eq. (1) yields,

$$P_T = n[\theta P_{STH} + (1 - \theta)P_{STL} + K_1(f) + K_2(f)] + C_L V_{CC2}^2 f + (4 - n)P_{ST} \quad (6)$$

On the other hand, each component of DC power per circuit can be obtained as follows,

$$P_{STL1} = (I_{CC1L}/4)V_{CC1} \quad (7)$$

$$P_{STL2} = (I_{CC2L}/4)V_{CC2} \quad (8)$$

$$P_{STH1} = (I_{CC1H}/4)V_{CC1} \quad (9)$$

$$P_{STH2} = (I_{CC2H}/4)V_{CC2} \quad (10)$$

The typical and maximum value of I_{CC1L}, I_{CC2L}, I_{CC1H} and I_{CC2H} are shown in the specification table.

For example, we calculate each value of Eqs. (1) to (10) in the case of duty ratio θ = 50%.

Items	Typ.	Max.
V_{CC1}	5.0V	5.25V
I_{CC1L}/PKG	30 mA	50 mA
I_{CC1H}/PKG	16 mA	30 mA
P_{STL1}/CCT	37.5 mW	65.6 mW
P_{STH1}/CCT	20 mW	39.4 mW
P_{STL}/CCT	38.1 mW	67.2 mW
P_{CC1}/CCT	28.8 + K_1(f) mW	52.5 +K_1(f) mW
V_{CC2}	12.0 V	12.6 V
I_{CC2L}/PKG	0.2 mA	0.5 mA
I_{CC2H}/PKG	10 mA	16 mA
P_{STL2}/CCT	0.6 mW	1.6 mW
P_{STH2}/CCT	30 mW	50.4 mW
P_{STH}/CCT	50 mW	89.8 mW
P_{CC2}/CCT	15.3 + K_2(f) mW	26.0 + K_2(f) mW

	Total Power Dissipation
Typ.	$P_T = n[28.8 + K_1(f) + 15.3 + K_2(f)] + C_L V_{CC2}^2 f + (4 - n)P_{ST}$
Max.	$P_T = n[52.5 + K_1(f) + 26.0 + K_2(f)] + C_L V_{CC2}^2 f + (4 - n)P_{ST}$

We should estimate P_T in the case of $P_{ST} = P_{STL}$ and in the case of $P_{ST} = P_{STH}$.

The Eq. of P_T can be reduced as shown in the table below, assuming $K_1(f) = 0$ because P_{CC1} hardly depends on the frequency.

Interface Devices

Items	P_{ST}	Total Power Dissipation
Typ.	P_{STL}	$P_T = n[44.1 + K_2(f)] + C_L(12)^2f + 38.1(4 - n)$
Max.		$P_T = n[78.5 + K_2(f)] + C_L(12.6)^2f + 67.2(4 - n)$
Typ.	I_{STH}	$P_T = n[44.1 + K_2(f)] + C_L(12)^2f + 50(4 - n)$
Max.		$P_T = n[78.5 + K_2(f)] + C_L(12.6)^2f + 89.8(4 - n)$

The values of the $K_2(f)$ can be calculated by subtracting $P_{ST2}[= 1/2(P_{STH2} + P_{STL2})]$ from P_{CC2} in Fig. 1.

The total power dissipation should be restricted by the upper limit of the junction temperature and the thermal resistance of the package. The maximum load capacitance of one package or of one circuit is determined from the current capability of lead wire. Thus, the load capacitance must be limited by two factors that are power dissipation and current density of lead wire. For the MB 8902 these limits are shown in the table below.

Total Power Dissipation/PKG	Max. 600 mW
Total Load Capacitance/PKG	Max. 1000 pF
Load Capacitance/CCT	Max. 600 pF

The maximum total load capacitance of MB 8902 (which contains four circuits in a package) can be derived by substituting these limits to the Eqs. of P_T (corresponding to each frequency of switching). The result of the calculation in the case of n = 4 is shown in Fig. 2.

Besides, we can obtain the maximum total load capacitance of any duty ratio by applying $(\theta P_{STH} + (1 - \theta)P_{STL})$ for P_{ST}.

FIG. 1 — P_{CC1} AND P_{CC2} VS. FREQUENCY SWITCHING

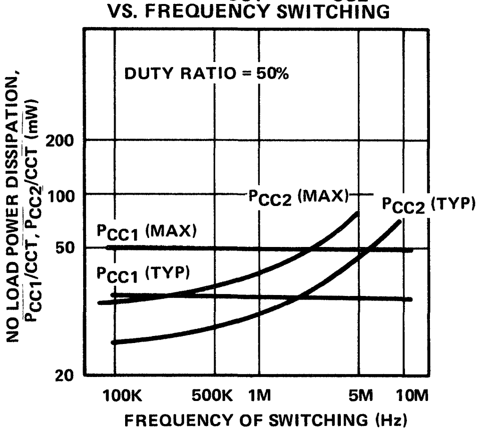
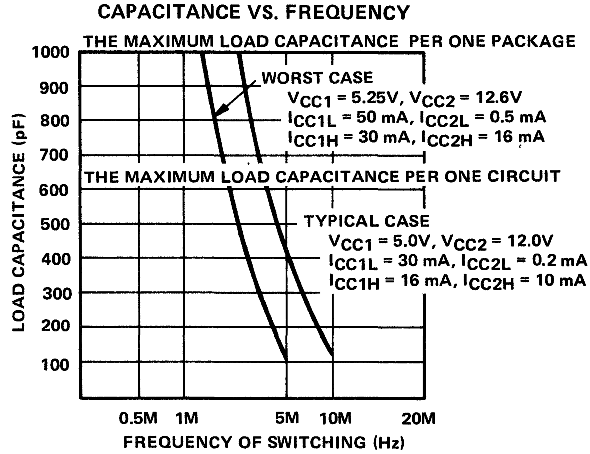


FIG. 2 — THE MAXIMUM LOAD CAPACITANCE VS. FREQUENCY



(QUADRUPLE TTL TO MOS LEVEL SHIFTER/DRIVER) ((NAND.function))

FUJITSU

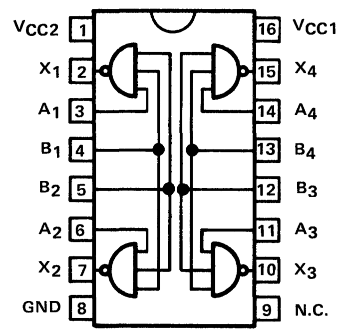
MB 8907

QUADRUPLE TTL TO MOS LEVEL SHIFTER/DRIVER (NAND FUNCTION)

The MB8907 is a level shifter from TTL/DTL level input to MOS level output, and also a high speed clock driver. Using Schottky barrier diodes and PNP transistors in the circuit, the power dissipation is remarkably reduced without degradation of switching speed.

- High speed: 23 ns max. (t_{PLH} @ 300 pF)
- Wide operating range of V_{CC2}: Variable output voltage (9V to 17V)
- Low power dissipation:
  40 mW for output low state
  40 mW for output high state
  (Stand by power/circuit, @ V_{CC2} = 12V)
- TTL or DTL compatible inputs
- Standard ceramic 16-leads dual-in-line package

PIN ASSIGNMENT



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (*1)	V_{CC1}	7	V
Supply Voltage (*1)	V_{CC2}	23	V
Input Voltage (*1)	V_I	−0.5 to +5.5	V
Operating Free-Air Temperature Range	T_{op}	−25 to +100	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

(*1) These voltage values are with respect to GND lead.

Interface Devices

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC1}	5.0 ± 5%	V
Supply Voltage	V_{CC2}	9.0 to 17	V
Operating Free-Air Temperature Range	T_{op}	0 to +70	°C

DC CHARACTERISTICS

(T_A = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	V_{IH} = 2.0V I_{OUT} = –0.1 mA	V_{CC2} –0.7	V_{CC2} –0.35		V
Output Low Voltage	V_{OL}	V_{IL} = 0.8V V_{CC1} = 4.75V V_{CC2} = 12.6V I_{OUT} = 0.1 mA		0.3	0.45	V
Input Low Current (Input A)	I_{IL} (A)	V_{IL} = 0.4V V_{CC1} = 5.25V V_{CC2} = 12.6V		–1.0	–2.0	mA
Input Low Current (Input B)	I_{IL} (B)	Same as above		–2.0	–4.0	mA
Input High Current (Input A)	I_{IH} (A)	V_{IH} = 2.4V			40	μA
Input High Current (Input B)	I_{IH} (B)	V_{IH} = 2.4V			80	μA
Operating Supply Voltage of V_{CC2}	V_{CC2}		9.0		17	V
Supply Current (Output Low)(*1)	I_{CC1L}	V_{CC1} = 5.25V V_{CC2} = 12.6V V_{IL} = 0V T_A = 25°C		40	60	mA
	I_{CC2L}	Same as above		0.2	2	mA
Supply Current (Output High)(*2)	I_{CC1H}	V_{CC1} = 5.25V V_{CC2} = 12.6V V_{IH} = 5.25V T_A = 25°C		25	40	mA
	I_{CC2H}	Same as above		10	20	mA

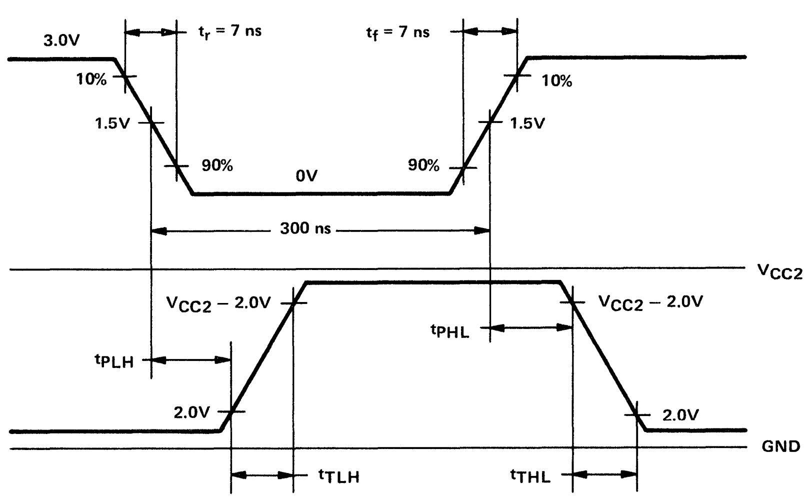
(*1) The typical values are applicable for V_{CC1} = 5.0V, V_{CC2} = 12.0V, T_A = 25°C.
(*2) These values are total current for a package.

AC CHARACTERISTICS

(T_A = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input to Output Delay	t_{PLH}	V_{CC1} = 5.0V, V_{CC2} = 12.0V, C_L = 300 pF	7	16	23	ns
Input to Output Delay	t_{PHL}	Same as above	7	15	20	ns
Output Rise Time	t_{TLH}	V_{CC1} = 5.0V, V_{CC2} = 12.0V, C_L = 300 pF	7	15	25	ns
Output Fall Time	t_{THL}	Same as above	7	16	25	ns
$t_{PLH} + t_{TLH}$	t_{DLH}	Same as above	20	31	45	ns
$t_{PHL} + t_{THL}$	t_{DHL}	Same as above	15	31	40	ns

WAVEFORMS



Interface Devices

POWER CONSIDERATION

The total power dissipation of the MB 8907 is given as

$$P_T = n(P_{CC1} + P_{CC2}) + C_L V_{CC2}^2 f + (4 - n)P_{ST} \quad (1)$$

where,

n: The number of circuits operating at frequency f.
P_{ST}; DC power dissipation per circuit.
$C_L V_{CC2}^2 f$: The power required for charging and discharging load capacitance.
f: The frequency of switching.
C_L: The total load capacitance.

P_{CC1} and P_{CC2} are expressed as below,

$$P_{CC1} = \theta P_{STH1} + (1 - \theta)P_{STL1} + K_1(f) \quad (2)$$

$$P_{CC2} = \theta P_{STH2} + (1 - \theta)P_{STL2} + K_2(f) \quad (3)$$

where,

P_{CC1}: The power supplied from V_{CC1} when the circuit is operating with no load capacitance.
P_{CC2}: The power supplied from V_{CC2} when the circuit is operating with no load capacitance.
P_{STH1}: The DC component of P_{CC1} when output is High.
P_{STL1}: The DC component of P_{CC1} when output is Low.
P_{STH2}: The DC component of P_{CC2} when output is High.
P_{STL2}: The DC component of P_{CC2} when output is Low.
θ: Duty ratio.
$K_1(f)$: The AC component of P_{CC1}.
$K_2(f)$: The AC component of P_{CC2}.

Assuming that

$$P_{STH} = P_{STH1} + P_{STH2} \quad (4)$$

$$P_{STL} = P_{STL1} + P_{STL2} \quad (5)$$

where,

P_{STH}: The DC power dissipation when output is High.
P_{STL}: The DC power dissipation when output is Low.

Then, substitution of Eqs. (2), (3), (4), (5) into Eq. (1) yields,

$$P_T = n[\theta P_{STH} + (1 - \theta)P_{STL} + K_1(f) + K_2(f)] + C_L V_{CC2}^2 f + (4 - n)P_{ST} \quad (6)$$

On the other hand, each component of DC power per circuit can be obtained as follows,

$$P_{STL1} = (I_{CC1L}/4)V_{CC1} \quad (7)$$

$$P_{STL2} = (I_{CC2L}/4)V_{CC2} \quad (8)$$

$$P_{STH1} = (I_{CC1H}/4)V_{CC1} \quad (9)$$

$$P_{STH2} = (I_{CC2H}/4)V_{CC2} \quad (10)$$

The typical and maximum value of I_{CC1L}, I_{CC2L}, I_{CC1H} and I_{CC2H} are shown in the specification table.

For example, we calculate each value of Eqs. (1) to (10) in the case of duty ratio θ = 50%.

Items	Typ.	Max.
V_{CC1}	5.0 V	5.25V
I_{CC1L}/PKG	40 mA	60 mA
I_{CC1H}/PKG	25 mA	40 mA
P_{STL1}/CCT	40 mW	78.8 mW
P_{STH1}/CCT	31.3 mW	52.5 mW
P_{STL}/CCT	40.6 mW	85.1 mW
P_{CC1}/CCT	$35.6 + K_1(f)$ mW	$65.7 + K_1(f)$ mW
V_{CC2}	12.0 V	12.6 V
I_{CC2L}/PKG	0.2 mA	2.0 mA
I_{CC2H}/PKG	10 mA	20 mA
P_{STL2}/CCT	0.6 mW	6.3 mW
P_{STH2}/CCT	30 mW	63 mW
P_{STH}/CCT	61.3 mW	115.5 mW
P_{CC2}/CCT	$15.3 + K_2(f)$ mW	$34.7 + K_2(f)$ mW

	Total Power Dissipation
Typ.	$P_T = n[35.6 + K_1(f) + 15.3 + K_2(f)] + C_L V_{CC2}^2 f + (4 - n)P_{ST}$
Max.	$P_T = n[65.7 + K_1(f) + 34.7 + K_2(f)] + C_L V_{CC2}^2 f + (4 - n)P_{ST}$

We should estimate P_T in the case of $P_{ST} = P_{STL}$ and in the case of $P_{ST} = P_{STH}$.

The Eq. of P_T can be reduced as shown in the table below, assuming $K_1(f) = 0$ because P_{CC1} hardly depends on the frequency.

Items	P_{ST}	Total Power Dissipation
Typ.	P_{STL}	$P_T = n[50.9 + K_2(f)] + C_L(12)^2f + 40.6(4 - n)$
Max.		$P_T = n[100.4 + K_2(f)] + C_L(12.6)^2f + 85.1(4 - n)$
Typ.	P_{STH}	$P_T = n[50.9 + K_2(f)] + C_L(12)^2f + 61.3(4 - n)$
Max.		$P_T = n[100.4 + K_2(f)] + C_L(12.6)^2f + 115.5(4 - n)$

The values of the $K_2(f)$ can be calculated by subtracting $P_{ST2}[= 1/2(P_{STH2} + P_{STL2})]$ from P_{CC2} in Fig. 1.

The total power dissipation should be restricted by the upper limit of the junction temperature and the thermal resistance of the package. The maximum load capacitance of one package or of one circuit is determined from the current capability of lead wire. Thus, the load capacitance must be limited by two factors that are power dissipation and current density of lead wire. For the MB 8907 these limits are shown in the table below.

Total Power Dissipation/PKG	Max. 600 mW
Total Load Capacitance/PKG	Max. 1000 pF
Load Capacitance/CCT	Max. 600 pF

The maximum total load capacitance of MB 8907 (which contains four circuits in a package) can be derived by substituting these limits to the Eqs. of P_T (corresponding to each frequency of switching). The result of the calculation in the case of n = 4 is shown in Fig. 2.

Besides, we can obtain the maximum total load capacitance of any duty ratio by appling $[\theta P_{STH} + (1 - \theta)P_{STL}]$ for P_{ST}.

FIG. 1 — P_{CC1} AND P_{CC2} VS. FREQUENCY OF SWITCHING

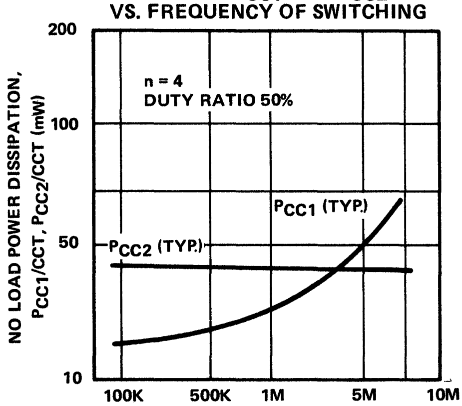
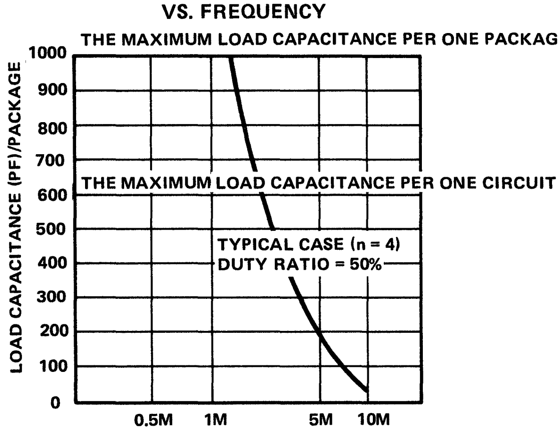


FIG. 2 — LOAD CAPACITANCE VS. FREQUENCY



FUJITSU

DUAL CML TO MOS LEVEL SHIFTER

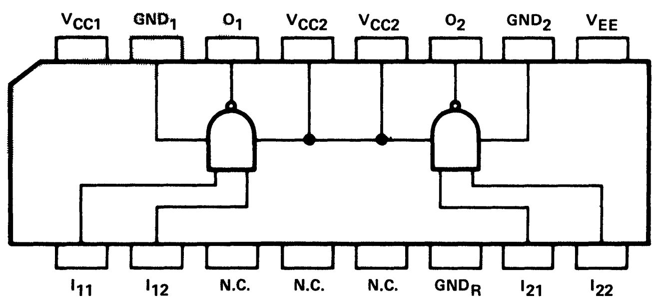
MB 8909

DUAL CML TO MOS LEVEL SHIFTER

The MB8909 is a level shifter from CML level input to MOS level output, and also a high speed clock driver, using Schottky barrier diodes and PNP transistors in the circuit.

- High speed:
  - 12 ns typ. (t_{PLH} @ 300 pF)
  - 16 ns typ. (t_{TLH} @ 300 pF)
- Wide operating range of V_{CC2}
  - Variable output voltage
  - (7V to 16V)

PIN ASSIGNMENT



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (*1)	V_{CC1}	-0.3 to + 7	V
Supply Voltage (*1)	V_{CC2}	-0.3 to +20	V
Supply Voltage (*1)	V_{EE}	-7 to +0.3	V
Supply Voltage (*1)	V_I	V_{EE} to +0.3	V
Output Load Capacitance	C_L	1200 pF/PKG 600 pF/CCT	
Operating Free-Air Temperature Range	T_{op}	-25 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

(*1) These voltage values are with respect to GND lead.

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Value	Unit
Supply Voltage (*1)	V_{CC1}	5.0 ± 5%	V
Supply Voltage (*1)	V_{CC2}	7.0 to 16.0	V
Supply Voltage (*1)	V_{EE}	-5.2 ± 4%	V
Output Load Capacitance	C_L	0 ~ 300 pF/CCT	
Operating Temperature	T_{op}	0 to +70	°C

(*1) These voltage values are with respect to GND lead.

DC CHARACTERISTICS

(T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}					V
Input Low Voltage	V_{IL}					V
Input Low Current	I_{IL}	V_{IL} = -1.75V		150	500	μA
Input High Current	I_{IH}	V_{IH} = -0.85V		0.35	1.0	mA
Output Low Voltage	V_{OL}	$V_{IN} = V_{IH}$ I_{OL} = 0.1 mA		0.35	0.6	V
Output High Voltage	V_{OH}	$V_{IN} = V_{IL}$ I_{OH} = -0.1 mA	V_{CC2} -0.5	V_{CC2} -0.3		V
Output Clamp Voltage	V_{OC}	$V_{IN} = V_{IL}$ I_{OH} = 20 mA			V_{CC2} +1.0	V
Output Current	I_{OL}	$V_{IN} = V_{IH}$ V_{OL} = 1.5V	20			mA
Supply Current ("ON")/PKG	I_{CC1L}	V_{IH} = -0.85V		15.9	23	mA
	I_{CC2L}	Same as above			150	μA
	I_{EEL}	Same as above	-32	-22		mA
Supply Current ("OFF")/PKG	I_{CC1H}	V_{IL} = -1.75V		12.4	18.5	mA
	I_{CC2H}	Same as above		7.0	10	mA
	I_{EEH}	Same as above	-29.5	-21.9		mA

Note: The typical values are applicable for V_{CC1} = 5.0V, V_{CC2} = 12.0V, V_{EE} = -5.2V, V_{IH} = -0.85V, V_{IL} = -1.75V, T_A = 25°C.

TESTING VOLTAGE VALUES

T_A	0°C	25°C	70°C
V_{IH}min.	−1.17	−1.14	−1.05
V_{IL}max.	−1.46	−1.44	−1.42

AC CHARACTERISTICS

T_A = 25°C, V_{CC1} = 5.0V, V_{CC2} = 12.0V, V_{EE} = −5.2V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current	I_{CC1}	T_C = 250 ns C_L = 0 pF Duty Cycle = 50% V_{IH} = −0.85V V_{IL} = −1.75V		14.5		mA
	I_{CC2}			8.5		
	I_{EE}			23.5		

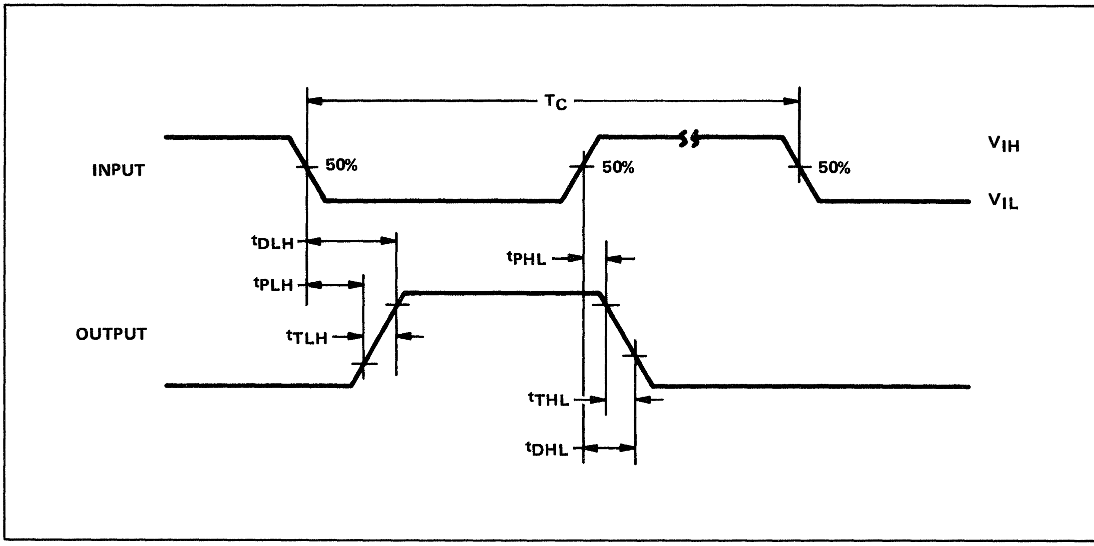
SWITCHING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC1} = 5.0V ± 5%, V_{CC2} = 12.0V ± 5%, V_{EE} = −5.2V ± 4%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propogation Time, Input to Output	t_{PLH}	C_L = 300 pF T_C = 250 ns V_{IH} = −0.85V ± 0.03V V_{IL} = −1.75V ± 0.03V	7	12	19	ns
Propogation Time, Input to Output	t_{PHL}		5	11	17	
Output Rise Time	t_{TLH}			16	23	
Output Fall Time	t_{THL}			13	20	
Delay Time, Low-to-High Level	t_{DLH}		18	28	39	
Delay Time, High-to-Low Level	t_{DHL}		15	24	32	

Note: The typical values are applicable for V_{CC1} = 5.0V, V_{CC2} = 12V, V_{EE} = −5.2V, T_A = 25°C.

SWITCHING CHARACTERISTICS (con't)



FUJITSU

QUADRUPLE 2-INPUT OR ECL TO MOS LEVEL SHIFTER/DRIVER

MB 8903

QUADRUPLE 2-INPUT OR ECL TO MOS LEVEL/SHIFTER

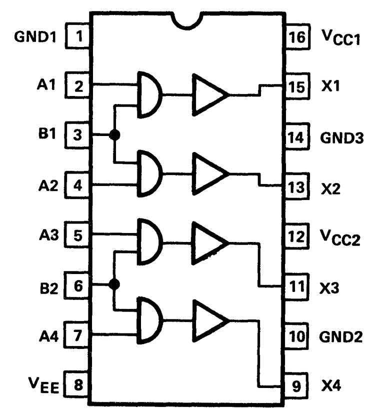
The MB 8903 is a quad 2-input OR gate and consists of four ECL to MOS translators which convert MB 10K logic levels to NMOS levels.

It is designed for use in N-channel memory systems as a Read/Write, Data/Address Driver.

It may also be used as a high fanout ECL to TTL translator, or in other applications requiring the capability to drive high capacitive loads.

- Fast propagation delay: 10 ns typ. @ 300 pF/ckt
- Low power dissipation: 420 mW typ./pkg @ 5.0 MHz (all 4 drivers have 300 pF)
- Input: ECL10K
- Output: +0.4V, V_{OL} max.
  +3.0V, V_{OH} min.

PIN ASSIGNMENT



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	0 to +7.0	V
Supply Voltage	V_{EE}	-8.0 to 0	V
Input Voltage	V_{IN}	V_{EE} to 0	V
Output Voltage	V_O	0 to V_{CC} + 0.5	V
Capacitive Load	C_L	0 pF to 600 pF/ckt 0 pF to 1800 pF/pkg	
Operating Frequency	f_C	0 to +10	MHz
Operating Temperature Range	T_{op}	-25 to +100	°C
Storage Temperature	T_{stg}	-55 to +150	°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.0 ± 5%	V
Supply Voltage	V_{EE}	−5.2 ± 5%	V
Capacitive Load	C_L	0 pF to 300 pF/ckt	
Operating Frequency	f_C	0 to 5	MHz
Operating Temperature Range	T_{op}	0 to +70	°C

AC CHARACTERISTICS

(T_A = 25°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Propagation Delay	t_{PLH}	V_{CC} = 5.00V V_{EE} = −5.20V C_L = 300 pF		13	ns
Propagation Delay	t_{PHL}			18	ns
Rise Time	t_{TLH}			15	ns
Fall Time	t_{THL}			13	ns

Input voltage values are below.

T_A (°C)	$V_{IHmax.}$	$V_{ILmin.}$	$V_{IHmin.}$	$V_{ILmax.}$
0	−0.845	−1.870	−1.150	−1.490
25	−0.810	−1.850	−1.105	−1.475
70	−0.730	−1.830	−1.055	−1.450

(Units V)

DC CHARACTERISTICS

(Air flow is greater than 2.5 m/sec)

Parameter	Symbol	Conditions	T_A (°C)	Min.	Max.	Unit
Output High Voltage	V_{OH}	V_{CC} = 4.75V V_{EE} = –5.20V $V_I = V_{IHmax.}$ I_O = –0.1 mA (*1)	0 25 70	3.0 3.0 3.0		V V V
Output High Threshold Voltage	V_{OTH}	V_{CC} = 4.75V V_{EE} = –5.20V $V_I = V_{IHmin.}$ I_O = –0.1 mA (*1)	0 25 70	3.0 3.0 3.0		V V V
Output Low Threshold Voltage	V_{OTL}	V_{CC} = 5.25V V_{EE} = –5.20V $V_I = V_{ILmax.}$ I_O = 0.1 mA (*1)	0 25 70		0.4 0.4 0.4	V V V
Output Low Voltage	V_{OL1}	V_{CC} = 4.75V V_{EE} = –5.20V $V_I = V_{ILmin.}$ I_O = 0.1 mA (*1)	0 25 70		0.4 0.4 0.4	V V V
Output Low Voltage	V_{OL2}	V_{CC} = 4.75V V_{EE} = –5.20V $V_I = V_{ILmin.}$ I_O = 20 mA (*1)	0 25 70		0.6 0.6 0.6	V V V
Input High Current	I_{IHA}	V_{CC} = 5.00V V_{EE} = –5.20V $V_I = V_{IHmax.}$ (*1)	25		265	μA
	I_{IHB}	V_{CC} = 5.00V V_{EE} = –5.20V $V_I = V_{IHmax.}$ (*1)	25		370	μA
Input Low Current	I_{IL}	V_{CC} = 5.00V V_{EE} = –5.20V $V_I = V_{ILmin.}$ (*1)	25	0.5		μA

(*1) Other inputs are open.

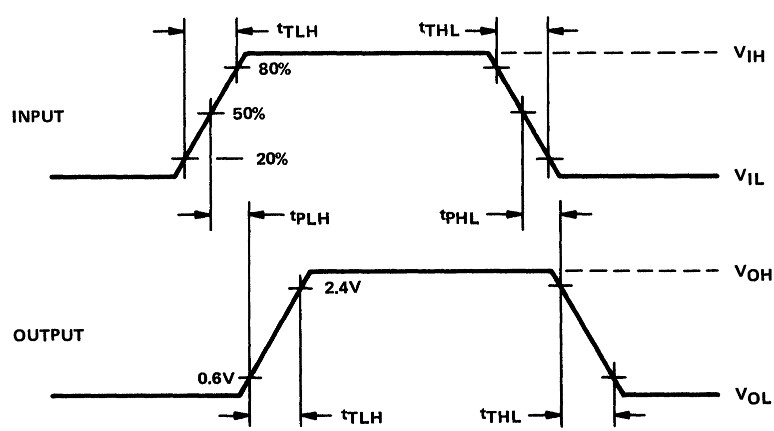
Interface Devices

DC CHARACTERISTICS (continued)

Parameter	Symbol	Conditions	T_A (°C)	Min.	Max.	Unit
Positive Power Supply Current	I_{CCH}	V_{CC} = 5.00V V_{EE} = −5.20V $V_I = V_{IHmax.}$	25		32	mA
Positive Power Supply Current	I_{CCL}	V_{CC} = 5.00V V_{EE} = −5.20V Inputs open	25		57	mA
Negative Power Supply Current	I_{EE}	V_{CC} = 5.00V V_{EE} = −5.2V Inputs open	25	−40		mA

(*1) Other inputs are open.

WAVEFORMS



INPUT PULSE
V_{IH} = −0.89V, V_{IL} = −1.69V
$t_{TLH} = t_{THL}$ = 2.0 ns ± 0.2 ns
PRR = 5 MHz

FIG. 1 — POWER DISSIPATION
VS. FREQUENCY

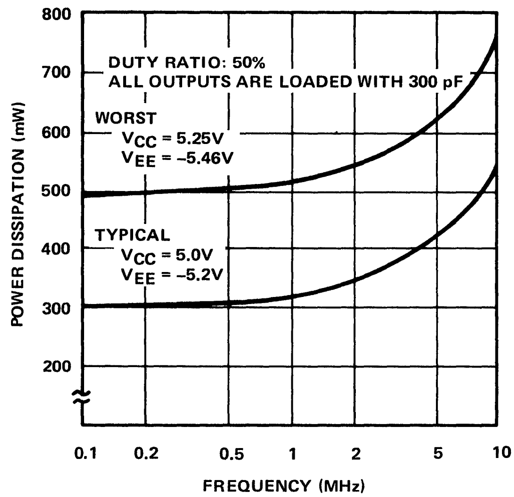


FIG. 2 — OUTPUT VOLTAGE
(HIGH) VS. OUTPUT CURRENT

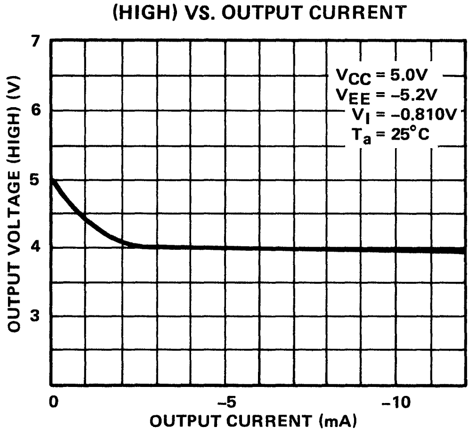


FIG. 3 — OUTPUT VOLTAGE
(LOW) VS. OUTPUT CURRENT

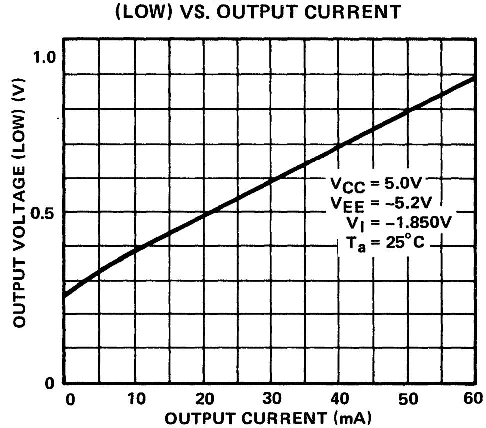


FIG. 4 — OUTPUT VOLTAGE (HIGH) VS. TEMPERATURE

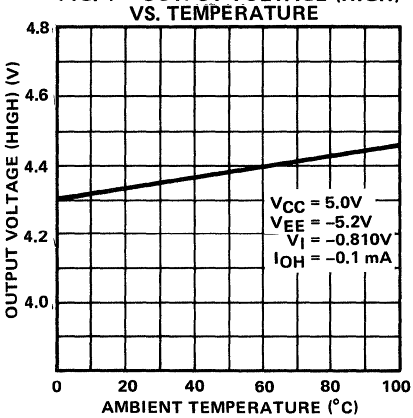


FIG. 5 — OUTPUT VOLTAGE (LOW) VS. TEMPERATURE

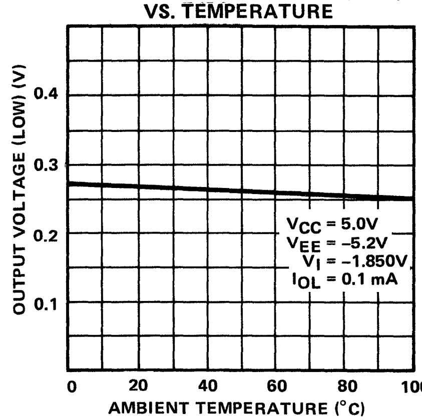


FIG. 6 — POSITIVE SUPPLY CURRENT VS. TEMPERATURE

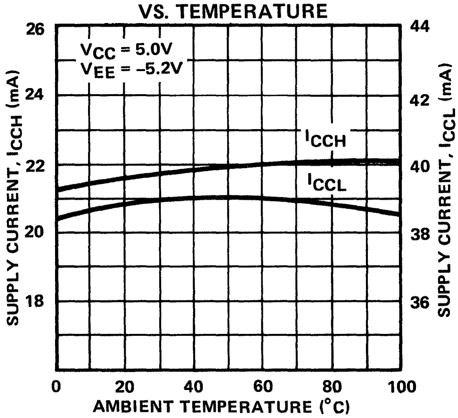


FIG. 7 — NEGATIVE SUPPLY CURRENT VS. TEMPERATURE

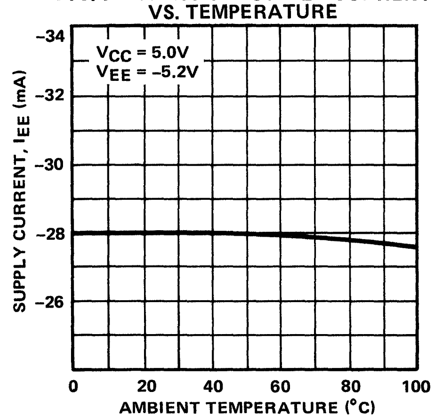


FIG. 8 – SWITCHING TIMES VS. LOAD CAPACITANCE

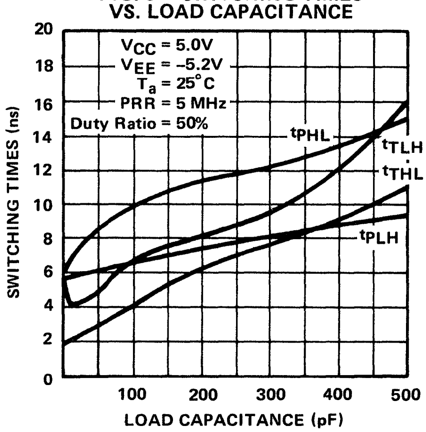


FIG. 9 – SWITCHING TIMES VS. TEMPERATURE

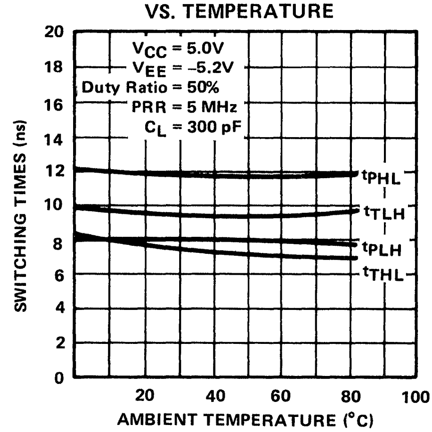


FIG. 10 – SWITCHING TIMES VS. POSITIVE SUPPLY VOLTAGE

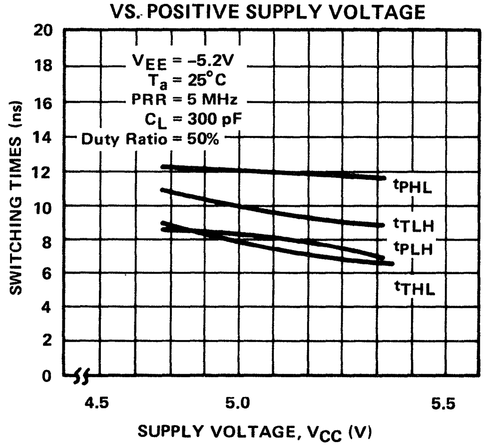
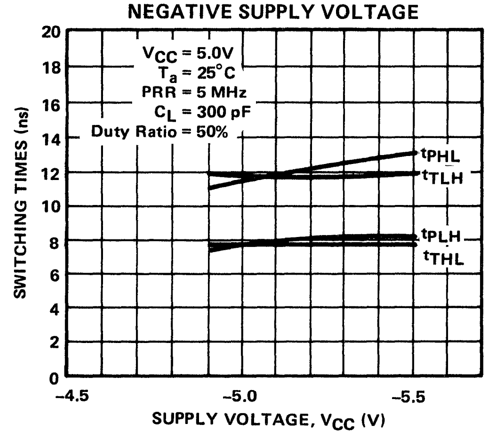


FIG. 11 – SWITCHING TIMES VS. NEGATIVE SUPPLY VOLTAGE



Interface Devices

FUJITSU

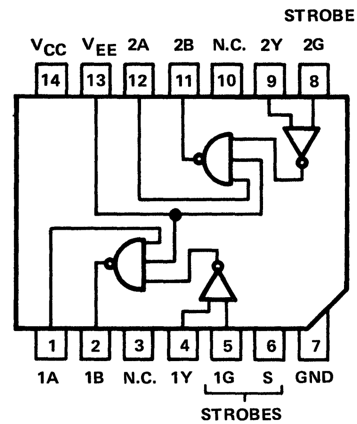
DUAL LINE RECEIVER

MB 8911

DUAL LINE RECEIVER

- High common-mode rejection ratio
- High input impedance
- High input sensitivity
- Differential input common-mode voltage range of ±3V
- Strobe inputs for receiver selection
- Gate inputs for logic versatility
- TTL or DTL drive capability
- High dc noise margins
- Standard ceramic 14-lead dual-in-line package

PIN ASSIGNMENT



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (*1)	V_{CC}	7	V
Supply Voltage (*1)	V_{EE}	-8.5	V
Differential Input Voltage (*2)		±6	V
Common mode input voltage (*1)		±5	V
Strobe Input Voltage (*1)		5.5	V
Operating Free-Air Temperature Range	T_{op}	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(*1) These voltage values are with respect to network ground terminal.
(*2) These voltage values are at the noninverting (+) terminal with respect to the inverting (–) terminal.

FUNCTION TABLE

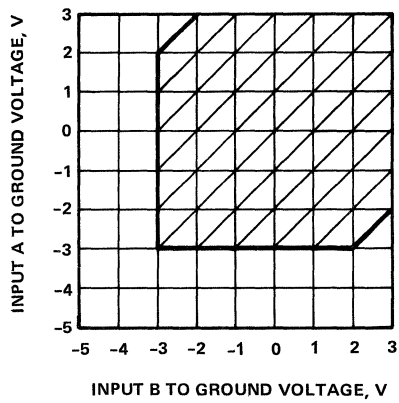
DIFFERENTIAL INPUTS A–B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geqslant 25$ mV	L or H	L or H	H
-25 mV $\leqslant V_{ID} \leqslant +25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leqslant -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

RECOMMENDED OPERATING CONDITIONS (*3)

Parameter	Symbol	Value	Unit
Supply Voltage (*1)	V_{CC}	5 ± 5%	V
Supply Voltage (*1)	V_{EE}	–5 ± 5% (or –6 ± 5%)	V
Output Sink Current		-16	mA
Differential Input Voltage		±5	V
Common Mode Input Voltage (*1)		±3	V
Input Voltage Range, Any Input to Ground (*4)		–5 to +3	V
Operating Free-Air Temperature Range	T_{op}	0 to +70	°C

(*3) When using only one channel of the line receiver, the inputs of the other channel should be grounded.
(*4) The recommended combinations of input voltages fall within the shaded area of the figure that follows.

RECOMMENDED COMBINATIONS
OF INPUT VOLTAGES FOR
LINE RECEIVERS



AC CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = –5V, T_A = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation Delay Time, Low to High Level, from Differential Inputs A and B to Output	$t_{PLH(D)}$	R_L = 390Ω C_L = 15 pF	10	21	28 [(27) *4]	ns
Propagation Delay Time, High to Low Level, from Differential Inputs A and B to Output	$t_{PHL(D)}$	R_L = 390Ω C_L = 15 pF	10	21	26 [(27) *4]	ns
Propagation Delay Time, Low to High Level, from Strobe Input G or S to Output	$t_{PLH(S)}$	R_L = 390Ω C_L = 15 pF	5	13	20	ns
Propagation Delay Time, High to Low Level, from Strobe Input G or S to Output	$t_{PHL(S)}$	R_L = 390Ω C_L = 15 pF	5	13	20	ns

(*4) These maximum values are applicable for V_{EE} = –6V.

DC CHARACTERISTICS

(T_A = 0°C to +70°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-Level Input Current into 1A or 2A	I_{IH}	V_{CC} = max., V_{EE} = max. V_{ID} = 0.5V V_{IC} = 2.5V			75	μA
Low-Level Input Current into 1A or 2A	I_{IL}	V_{CC} = max., V_{EE} = max. V_{ID} = −2V V_{IC} = −1V			−10	μA
High-Level Input Current into 1G or 2G	I_{IHG1}	V_{CC} = max., V_{EE} = max., $V_{IH(S)}$ = 2.4V			40	μA
	I_{IHG2}	V_{CC} = max., V_{EE} = max. $V_{IH(S)}$ = 5.5V			1	mA
Low-Level Input Current into 1G or 2G	I_{ILG}	V_{CC} = max., V_{EE} = max. $V_{IL(S)}$ = 0.4V			− 1.6	mA
High-Level Input Current into S	I_{IHS1}	V_{CC} = max., V_{EE} = max. $V_{IH(S)}$ = 2.4V			80	μA
	I_{IHS2}	V_{CC} = max., V_{EE} = max. $V_{IH(S)}$ = 5.5V			2	mA
Low-Level Input Current into S	I_{ILS}	V_{CC} = max., V_{EE} = max. $V_{IL(S)}$ = 0.4V			− 3.2	mA
Low-Level Output Voltage	V_{OL}	V_{CC} = min., V_{EE} = min. I_{SINK} = 16 mA V_{IC} = 0V			0.4	V
High-Level Output Current	I_{OH}	V_{CC} = min., V_{EE} = min. V_{OH} = 5.25V			250	μA
High Logic-Level Supply Current from V_{CC}	I_{CCH}	V_{CC} = max., V_{EE} = max. V_{ID} = 25 mV		14	30	mA
High Logic-Level Supply Current from V_{EE}	I_{EEH}	V_{CC} = max., V_{EE} = max. V_{ID} = 25 mV		−11	−15	mA

FUJITSU

DUAL DIGIT DRIVER/SENSE AMPLIFIER

MB 8912

DUAL DIGIT DRIVER/SENSE AMPLIFIER

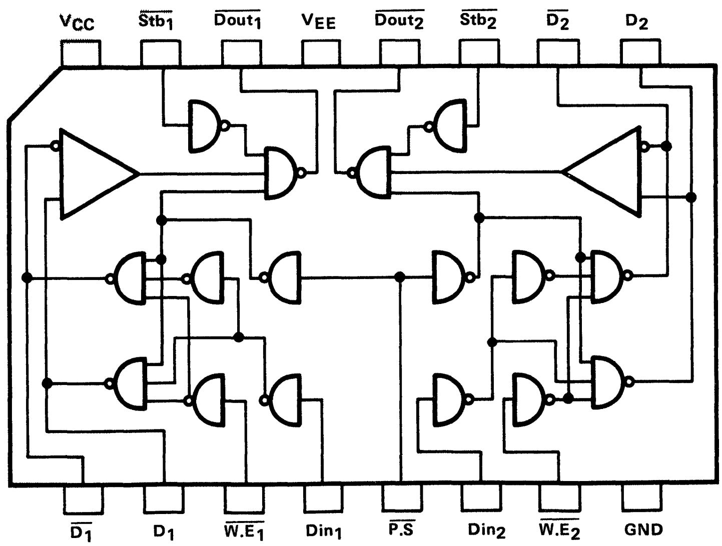
The MB 8912 is a TTL/DTL compatible high-speed digit driver (write amplifier) and sense amplifier.

This digit driver turns a MOS memory device such as MB 8201 into WRITE mode and writes a signal with TTL/DTL input signals. The sense amplifier senses output signal of the MOS memory device and converts the signal to TTL/DTL level.

High speed operation of the circuits is achieved by use of Schottky barrier diodes.

- High speed operation
  Write delay time, 22 ns max.
  Write recovery time, 18 ns max.
  Read delay time, 22 ns max.
  Strobe delay time, 18 ns max.
- High input sensitivity
- High common-mode rejection ratio
- TTL or DTL compatible input/output
- Standard ceramic 16-leads dual-in-line package

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	0 to +7	V
Supply Voltage	V_{EE}	−7 to 0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Operating Free-Air Temperature Range	T_{op}	−25 to +100	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.0 ± 5%	V
Supply Voltage	V_{EE}	-5.2 ± 5%	V
D or $\overline{D}$ Input Voltage (*1)	V_{ID}	V_{CC} +0.25, −1.00	V
D or $\overline{D}$ Input Voltage (*1)	$V_{I(D-\overline{D})}$	12 to 1000	mV
Operating Free-Air Temperature Range	T_{op}	0 to +70	°C
Output Sink Current	F/O	0 to +22	mA

(*1) READ mode.

DC CHARACTERISTICS

(T_A = 0°C ~ +70°C)

Parameter	Symbol	Conditions	V_{CC}	V_{EE}	Min.	Max.	Unit
Input High Voltage	V_{IH}				2.0		V
Input Low Voltage	V_{IL}					0.8	V
D/D Output Low Voltage	$V_{OL(D)}$	$\overline{Stb}$ = 0.8V R_L = 300Ω (A)	4.75V	-5.46V		0.5	V
D/D Output High Voltage	$V_{OH(D)}$	$\overline{Stb}$ = 0.8V R_L = 300Ω (A)	5.25V	-5.46V	5.05		V
S/A Input Sense Voltage	$V_{I(S)}$	$\overline{P.S}$, $\overline{Stb}$ = 0V	4.75V	-4.94V	12	1000	mV
S/A Output Low Voltage	$V_{OL(S)}$	Din, $\overline{P.S}$, $\overline{Stb}$ = 0.8V I_{OL} = 22 mA	4.75V	-5.46V		0.5	V
S/A Output High Voltage	$V_{OH(S)}$	Din = 0.8V (B) I_{OH} = −0.8 mA	4.75V	-4.94V	2.4		V
Input Low Current	I_{IL1}	V_{IL} = 0.4V	5.25V	-5.46V		1.6	mA
Input Low Current	I_{IL2}	V_{IL} = 0.4V	5.25V	-5.46V		3.2	mA
Input High Current	I_{IH}	V_{IH} = 2.4V	5.25V	-5.46V		200	μA
Output Short Current	I_{OS}	$\overline{W.E}$, $\overline{Stb}$ = 2.0V D = 5.0V, (C)	5.25V	-5.46V	100	380	mA
Supply Current D WRITE Mode	I_{CC}	$\overline{W.E}$, $\overline{P.S}$, Din = 0V $\overline{Stb}$ = 2.0V	5.25V	-5.46V		92	mA
	I_{EE}					30	

Interface Devices

(A) TRUTH TABLE

CONDITIONS			OUTPUT	
$\overline{P.S}$	Din	$\overline{W.E}$	$\overline{D}$	D
0.8V	0.8V	0.8V	V_{OH}	V_{OL}
0.8V	0.8V	2.0V	V_{OH}	V_{OH}
0.8V	2.0V	0.8V	V_{OL}	V_{OH}
2.0V	0.8V	0.8V	V_{OH}	V_{OH}

(B) TRUTH TABLE

CONDITIONS				$\overline{Dout}$
$\overline{D}$	D	$\overline{P.S}$	$\overline{Stb}$	
5.0 V	4.75V	0.8V	0.8V	V_{OH}
4.75V	5.0 V	2.0V	0.8V	V_{OH}
4.75V	5.0 V	0.8V	2.0V	V_{OH}
4.75V	5.0 V	2.0V	2.0V	V_{OH}

(C) Measurement Time: 0.3 sec., max.

AC CHARACTERISTICS

($T_A = 0°C \sim +70°C$, $V_{CC} = 5V$, $V_{EE} = -5.2V$)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Write Delay	t_{WD}	$\overline{D}$,D output, $R_L = 300\Omega$, $C_L = 50$ pF		22	ns
Write Recovery	t_{WR}	Same as above		18	ns
Data Hold	t_{DH}	Same as above	3		ns
Data Set-Up	t_{DS}	Same as above	10		ns
Enable Write Delay	t_{EW}	Same as above		22	ns
Minimum Write Width	t_{WW}	Same as above	24		ns
Read Delay	t_{SD}	$\overline{Dout}$ output, $R_L = 280\Omega$, $C_L = 30$ pF		22	ns
Strobe Delay	t_{SD}	Same as above		18	ns
Strobe Recovery	t_{SR}	Same as above		18	ns
Enable Read Delay	t_{ER}	Same as above		18	ns
Minimum Strobe Width	t_{WS}	Same as above	18		ns

FUJITSU

DUAL DIGIT DRIVER/SENSE AMPLIFIER

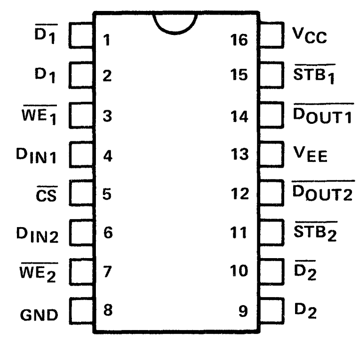
MB 8915

DUAL DIGIT DRIVER/SENSE AMPLIFIER

The Fujitsu MB8915 is a dual digit driver/sense amplifier with TTL level open-collector outputs which enable to make Wired-OR connection. This device is designed to provide with high speed operation and high sensitivity, and is suitable for the peripheral of the Fujitsu MB8201 High Speed MOS Random Access Memory and similar device which have common terminals for both data inputs and data outputs. This device is also designed to provide high noise-filtering ratio by adopting differential amplifier input circuitries.

- High speed operation with Schottky clamped TTL:
  t_{WD} = 14 ns typ. at C_L = 50 pF
  t_{RD} = 14 ns typ. at C_L = 15 pF
- High sensitivity with differential amplifier inputs: V_{IS} = 3 mA
- Connectable of Wired-OR with open-collector outputs
- MOS/TTL interface peripheral
- Dual power supplies: V_{CC} = 5.0V, V_{EE} = -6.0V
- Power consumption: 420 mW
- High noise-filtering ratio with differential amplifier inputs
- Fujitsu original device
- Standard 16-pin dual-in-line package

PIN ASSIGNMENT



TOP VIEW

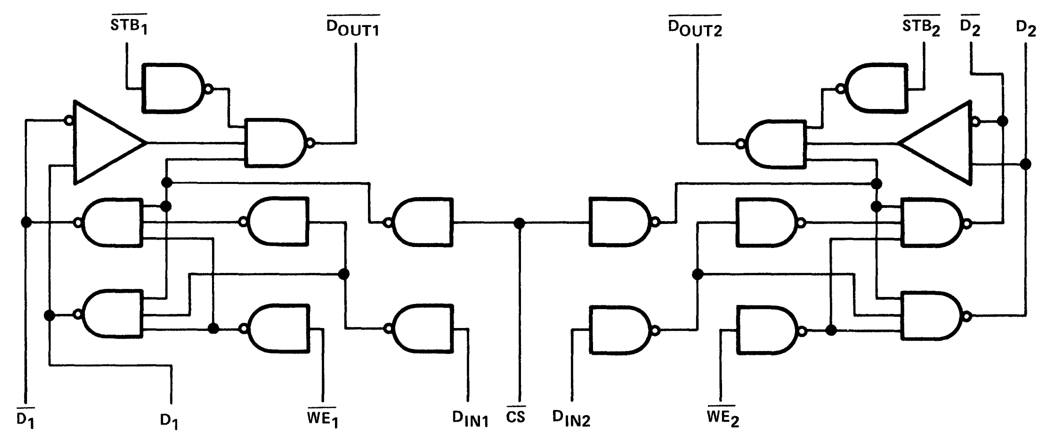
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to GND Pin	V_{CC}	-0.3 to +7.0	V
V_{EE} Pin Potential to GND Pin	V_{EE}	-8.0 to +0.3	V
Input Voltage except D and $\overline{D}$	V_I	-0.5 to +5.5	V
Input Voltage for D and $\overline{D}$	V_{ID}	-0.5 to +5.5	V
Output Voltage	V_O	-0.5 to +5.5	V
Operating Temperature	T_{op}	-25 to +100	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

FUNCTIONAL DESCRIPTION/APPLICATION INFORMATION

LOGIC DIAGRAM



FUNCTION TABLE
(TRUTH TABLE)

DIGIT DRIVER

D_{IN}	$\overline{WE}$	$\overline{CS}$	D	$\overline{D}$
0	0	0	0	1
1	0	0	1	0
0	1	0	1	1
0	0	1	1	1
1	1	0	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

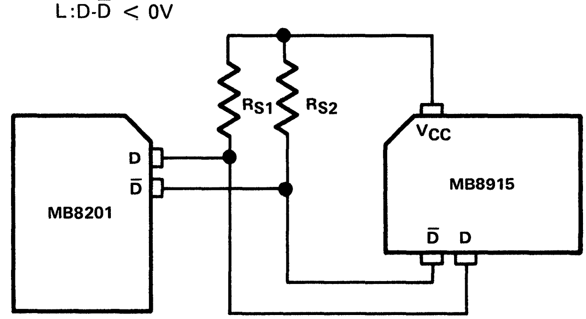
SENSE AMP

D-$\overline{D}$	$\overline{STB}$	$\overline{CS}$	$\overline{D_{OUT}}$
L	0	0	1
H	0	0	0
L	1	0	1
L	0	1	1
H	1	0	1
H	0	1	1
L	1	1	1
H	1	1	1

H:D-$\overline{D}$ $>$ 0V
L:D-$\overline{D}$ $<$ 0V

APPLICATION NOTE

When the MB8915 is connected to the MB8201 MOS RAM, sense resistors shall be connected externally between V_{CC} and D($\overline{D}$) terminals as in the figure to the right:



$R_{S1} = R_{S2} \approx 300\Omega \sim 1K\ \Omega$

GUARANTEED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	4.75 to 5.25	V
Supply Voltage	V_{EE}	-6.3 to -5.7	V
Output Sink Current	F/O	0 to 20	mA
$D(\overline{D})$ Input Voltage (Read Mode)	V_{ID}	V_{CC} -1.0 to V_{CC} +0.25	V
D-$\overline{D}$ Voltage Difference (Read Mode)	$V_{I(D-\overline{D})}$	12 to 1000	mV
Ambient Temperature	T_a	0 to +70	°C

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = -6.0V and T_A = 0°C to +70°C unless otherwise noted)

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Unit	Test Circuit
Propagation Delay Time $\overline{WE2}$ to $\overline{D2}$ for Write Mode (R_L = 300 ohm, C_L = 50 pF)	T_{WD1}	–	–	21	ns	Fig. 17
	T_{WD2}	–	–	22	ns	
	T_{WR}	–	–	18	ns	
	T_{WW}	–	–	24	ns	
Propagation Delay Time $\overline{CS}$ to $\overline{D2}$ for Write Mode (R_L = 300 ohm, C_L = 50 pF)	T_{EW}	–	–	22	ns	Fig. 18
Propagation Delay Time D2 to $\overline{D}_{out2}$ for Read Mode (R_L = 390 ohm, C_L = 15 pF)	$T_{RD(HL)}$	–	–	22	ns	Fig. 19
	$T_{RD(LH)}$	–	–	27	ns	
Propagation Delay Time Stb2 to $\overline{D}_{out2}$ (R_L = 390 ohm, C_L = 15 pF)	T_{SD}	–	–	18	ns	Fig. 20
	T_{SR}	–	–	24	ns	
	T_{WS}	–	–	18	ns	
Propagation Delay Time $\overline{CS}$ to $\overline{D}_{out2}$ for Read Mode (R_L = 390 ohm, C_L = 15 pF)	$T_{ER(HL)}$	–	–	18	ns	Fig. 21
	$T_{ER(LH)}$	–	–	24	ns	

Note: C_L includes jig and probe capacitance.

Interface Devices

DC CHARACTERISTICS

(V_{IH} = 2.0V, V_{IL} = 0.8V and T_A = 0°C to +70°C unless otherwise noted)

Parameter	Symbol	Value			Unit	Test Circuit
		Min.	Typ.	Max.		
Output High Voltage for Sense Amplifier Mode (V_{CC} = 4.75V, V_{EE} = –5.7V, R_L = 390 ohm)	$V_{OH(DO)}$	4.5	–	–	V	Fig. 1
Output High Voltage for Digit Driver Mode (V_{CC} = 5.25V, V_{EE} = –6.3V, R_L = 300 ohm)	$V_{OH(D)1}$	5.05	–	–	V	Fig. 2
Output High Voltage for Digit Driver Mode (V_{CC} = 4.75V, V_{EE} = –6.3V, I_{OH} = –0.8 mA)	$V_{OH(D)2}$	2.4	–	–	V	Fig. 3
Output Low Voltage for Sense Amplifier Mode (V_{CC} = 4.75V, V_{EE} = –6.3V, I_{OL} = 20 mA)	$V_{OL(DO)}$	–	–	0.5	V	Fig. 4
Output Low Voltage for Digit Driver Mode (V_{CC} = 4.75V, V_{EE} = –6.3V, R_L = 300 ohm)	$V_{OL(D)}$	–	–	0.5	V	Fig. 5
Input High Current for inputs except $\overline{CS}$ V_{CC} = 5.25V, V_{EE} = –6.3V, V_{IH} = 2.4V)	I_{IH1}	–	–	100	μA	Fig. 6
Input High Current for $\overline{CS}$ (V_{CC} = 5.25V, V_{EE} = –6.3V, V_{IH} = 2.4V)	I_{IH2}	–	–	200	μA	Fig. 7
Input Low Current for inputs except $\overline{CS}$ (V_{CC} = 5.25V, V_{EE} = –6.3V, V_{IL} = 0.4V)	I_{IL1}	–	–	-1.6	mA	Fig. 8
Input Low Current for $\overline{CS}$ (V_{CC} = 5.25V, V_{EE} = –6.3V, V_{IL} = 0.4V)	I_{IL2}	–	–	-3.2	mA	Fig. 9
Output Leakage Current for Sense Amplifier Mode (V_{CC} = 4.75V, V_{EE} = –5.7V, $V_{O(DO)}$ = 5.5V)	$I_{OH(DO)}$	–	–	100	μA	Fig. 10
Output Leakage Current for Digit Driver Mode (V_{CC} = 5.25V, V_{EE} = –6.3V, V_{OH1} = 5.25V, V_{OH2} = 5.7V)	$I_{OH(D)}$	–	–	5	μA	Fig. 11
Power Supply Current from V_{CC} for Stand-by Mode (V_{CC} = 5.25V, V_{EE} = –6.3V)	I_{CC1}	–	–	85	mA	Fig. 12
Power Supply Current from V_{EE} for Stand-by Mode (V_{CC} = 5.25V, V_{EE} = –6.3V)	I_{EE1}	–	–	-30	mA	Fig. 12
Power Supply Current from V_{CC} for Read Mode (V_{CC} = 5.25V, V_{EE} = –6.3V)	I_{CC2}	–	–	92	mA	Fig. 13
Power Supply Current from V_{EE} for Read Mode (V_{CC} = 5.25V, V_{EE} = –6.3V)	I_{EE2}	–	–	-30	mA	Fig. 13
Power Supply Current from V_{CC} for Write Mode V_{CC} = 5.25V, V_{EE} = –6.3V)	I_{CC3}	–	–	92	mA	Fig. 14

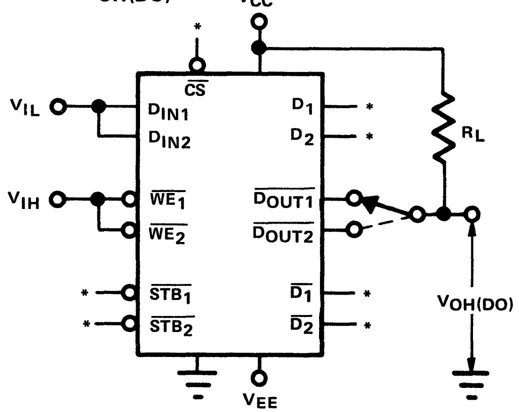
DC CHARACTERISTICS (continued)

Parameter	Symbol	Value			Unit	Test Circuit
		Min.	Typ.	Max.		
Power Supply Current from V_{EE} for Write Mode (V_{CC} = 5.25V, V_{EE} = -6.3V)	I_{EE3}	–	–	-30	mA	Fig. 14
Input Clamp Voltage (I_{IL} = -1 mA)	V_{IC}	-1.16	–	-0.23	V	Fig. 15
Input Current Sensitivity (V_{CC} = 5.25V/4.75V, V_{EE} = -6.3V/-5.7V)	$I_{I(D)}$	0.04	–	3.5	mA	Fig. 16

Note: Terminals not specified in this table and figures are in the open condition.

DC/AC TEST CIRCUIT

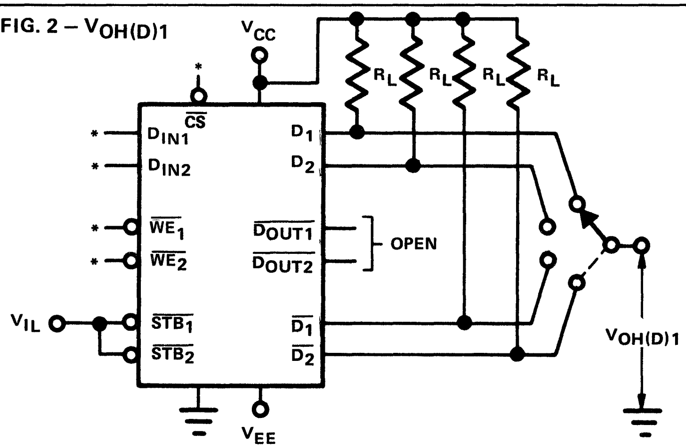
FIG. 1 – $V_{OH(DO)}$



*INPUT CONDITIONS

$\overline{CS}$	$\overline{STB}$	D	$\overline{D}$
V_{IL}	V_{IL}	4.75V	5.00V
V_{IH}	V_{IL}	5.00V	4.75V
V_{IL}	V_{IH}	5.00V	4.75V
V_{IH}	V_{IH}	5.00V	4.75V

FIG. 2 – $V_{OH(D)1}$



*INPUT CONDITIONS

$\overline{CS}$	D_{IN}	$\overline{WE}$	Measuring Terminals
V_{IL}	V_{IH}	V_{IL}	D
V_{IL}	V_{IL}	V_{IH}	D/$\overline{D}$
V_{IL}	V_{IL}	V_{IL}	$\overline{D}$
V_{IH}	V_{IL}	V_{IL}	D/$\overline{D}$

FIG. 3 – $V_{OH(D)2}$

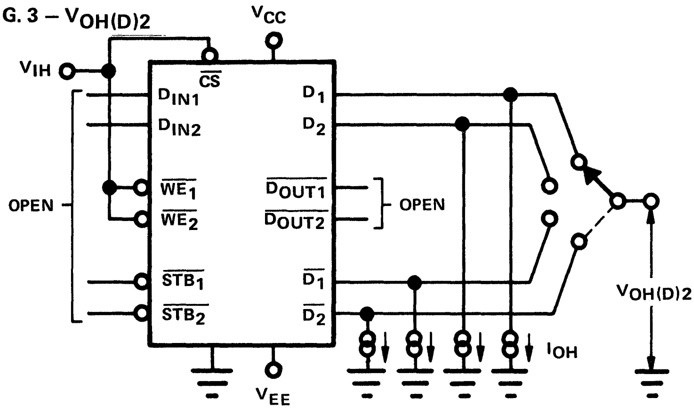


FIG. 4 – $V_{OL(DO)}$

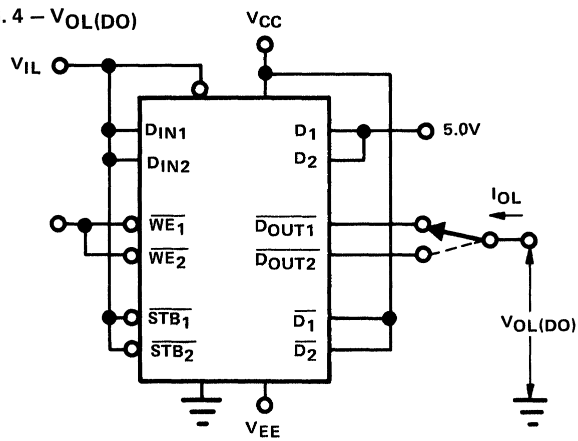
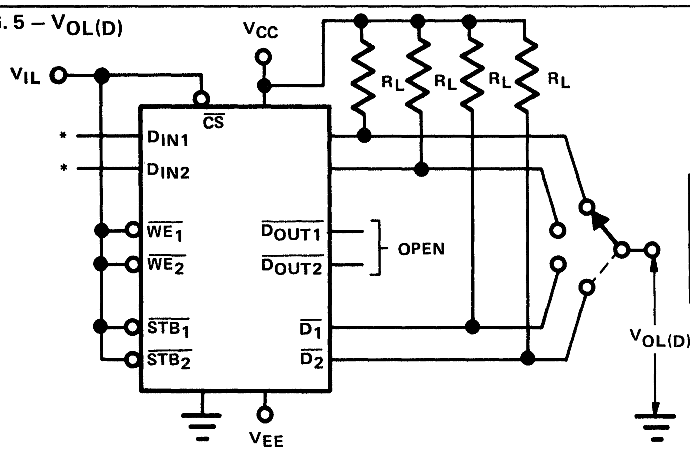


FIG. 5 – $V_{OL(D)}$



*INPUT CONDITIONS

D_{IN}	Measuring Terminals
V_{IL}	D
V_{IH}	$\overline{D}$

FIG. 6 – I_{IH1}

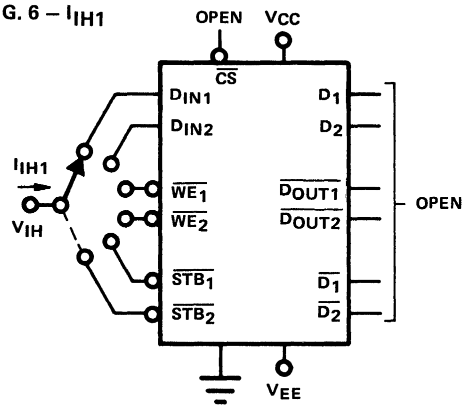


FIG. 7 – I_{IH2}

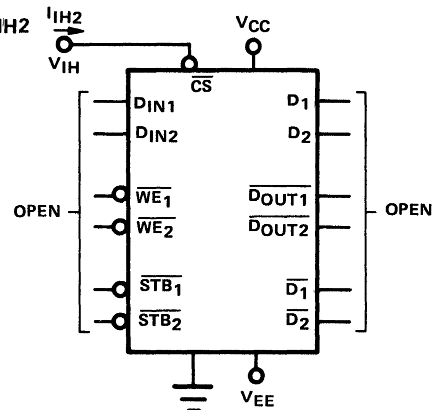


FIG. 8 – I_{IL1}

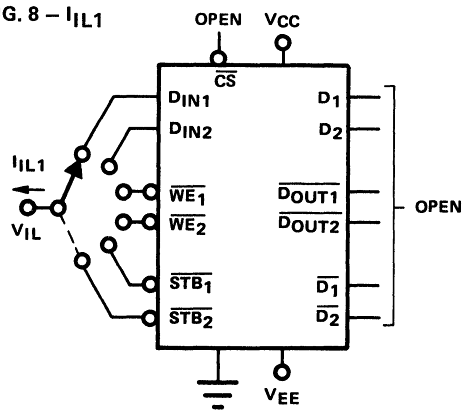


FIG. 9 – I_{IL2}

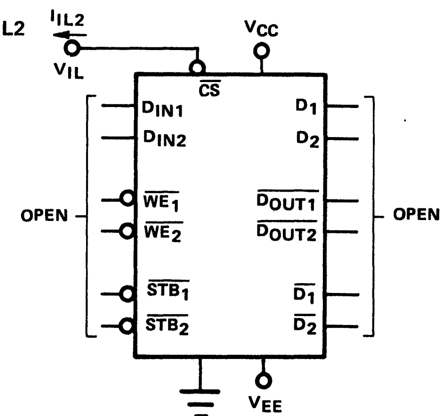
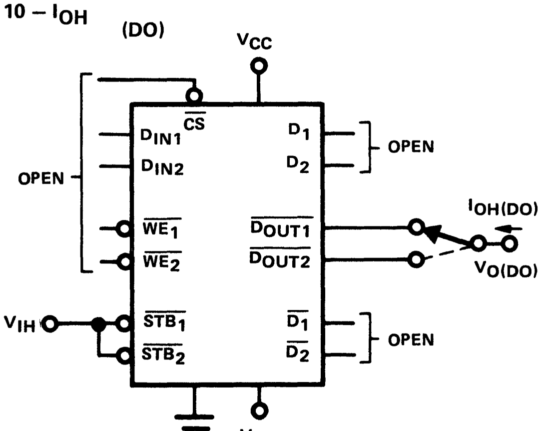


FIG. 10 – I_{OH} (DO)



Interface Devices

FIG. 11 – $I_{OH(D)}$

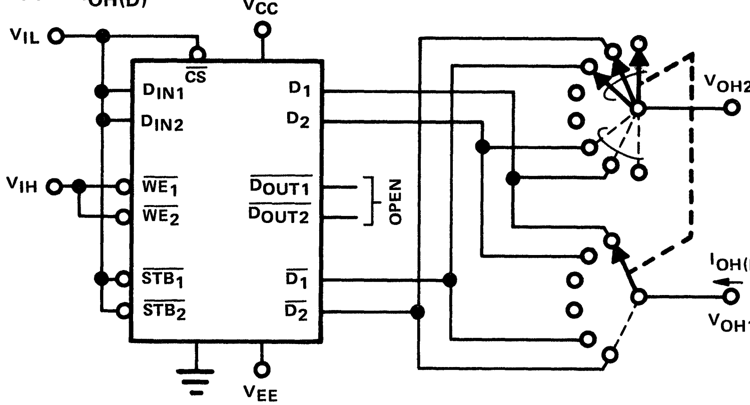


FIG. 12 – I_{CC1}/I_{EE1}

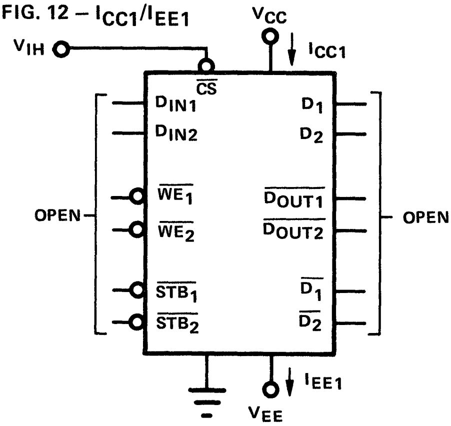


FIG. 13 – I_{CC2}/I_{EE2}

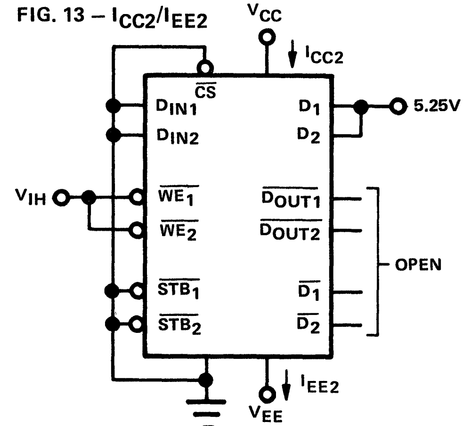


FIG. 14 – I_{CC3}/I_{EE3}

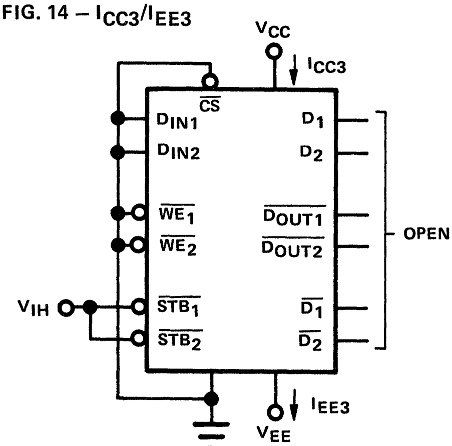


FIG. 15 – V_{IC}

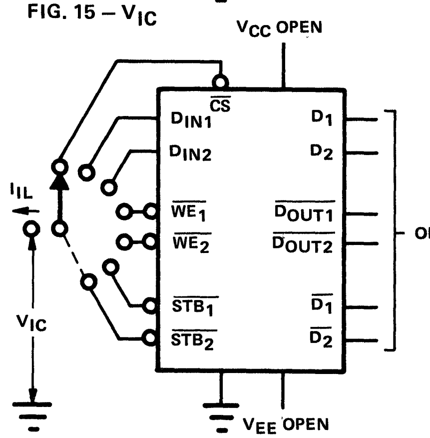
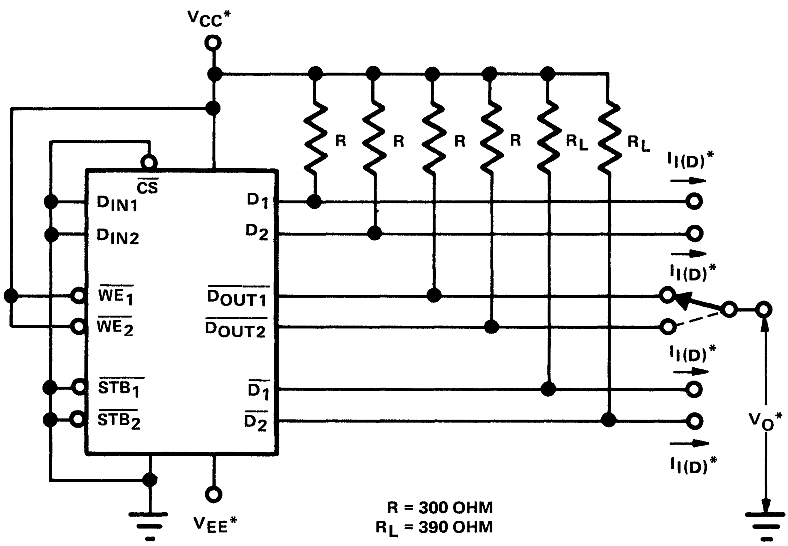


FIG. 16 – $I_{I(D)}$



*INPUT CONDITIONS

V_{CC}	V_{EE}	$I_{I(D)}$ D_1/D_2	$I_{I(D)}$ $\overline{D_1}/\overline{D_2}$	V_O LIMIT
5.25V	-6.3V	-40 μA	open	5.0V Min.
		open	-40 μA	0.5V Max.
4.75V	-5.7V	-40 μA	open	4.5V Min.
		open	-40 μA	0.5V Max.

FIG. 17 – PROPAGATION DELAY TIME, $\overline{WE_2}$ TO $\overline{D_2}$

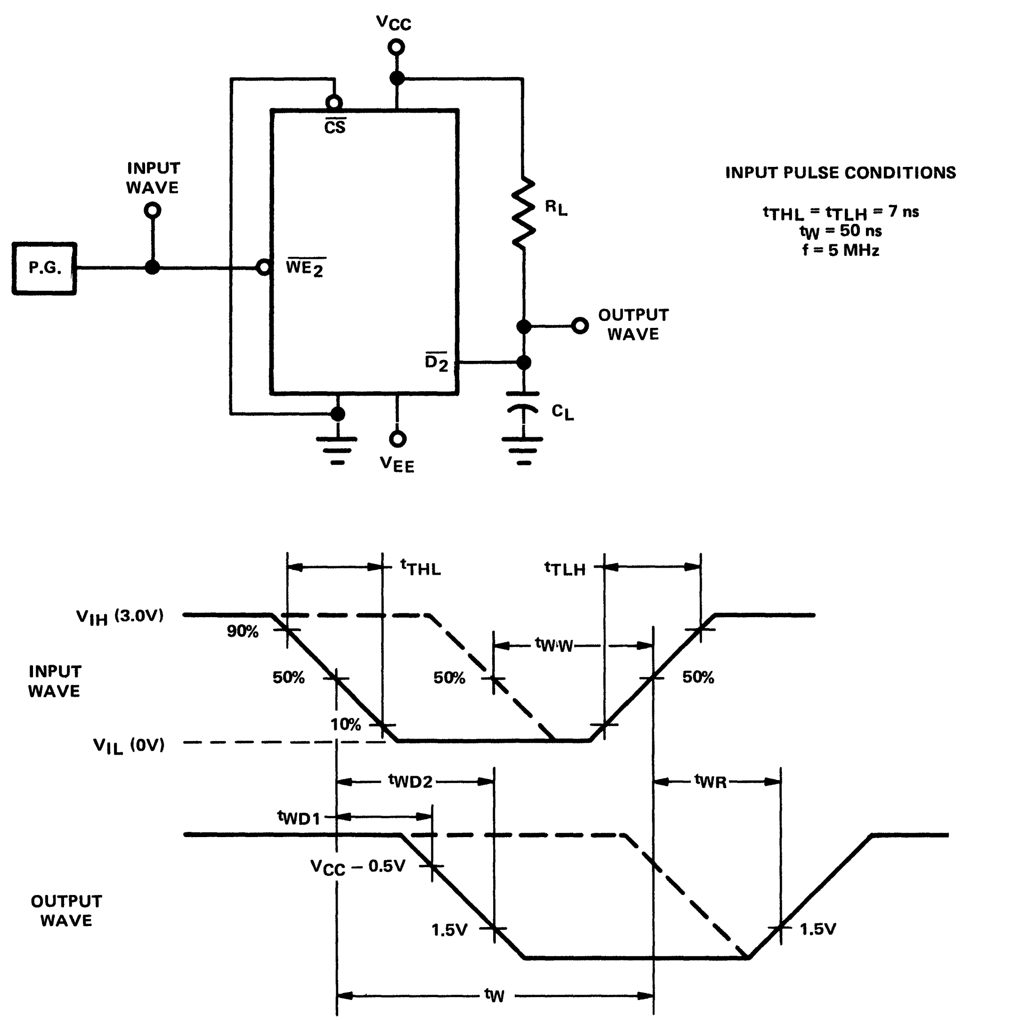
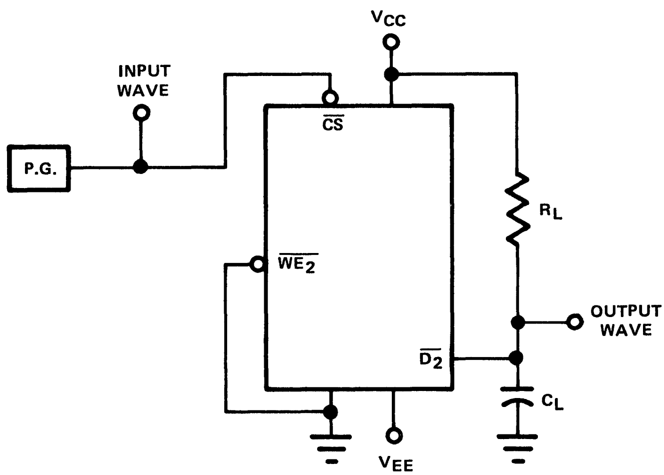


FIG. 18 – PROPAGATION DELAY TIME, $\overline{CS}$ TO $\overline{D_2}$



INPUT PULSE CONDITIONS

$t_{THL} = t_{TLH} = 7$ ns
$t_W = 50$ ns
f = 5 MHz

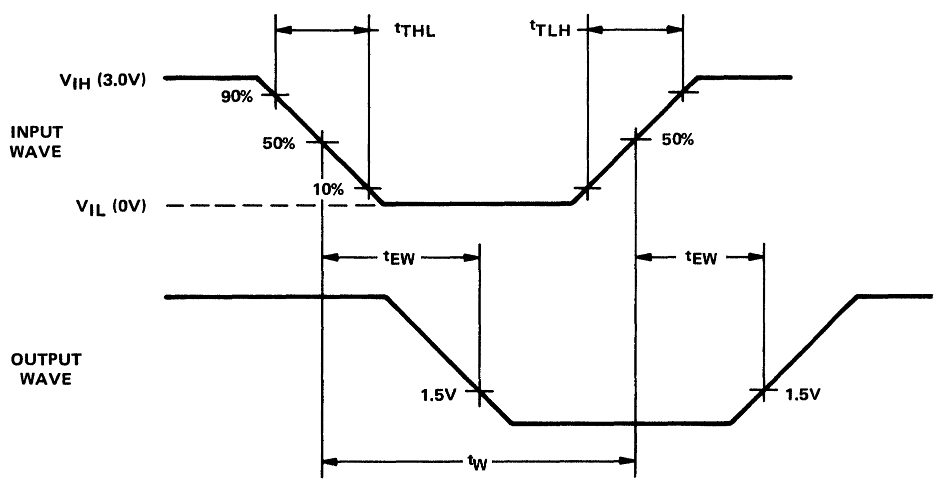
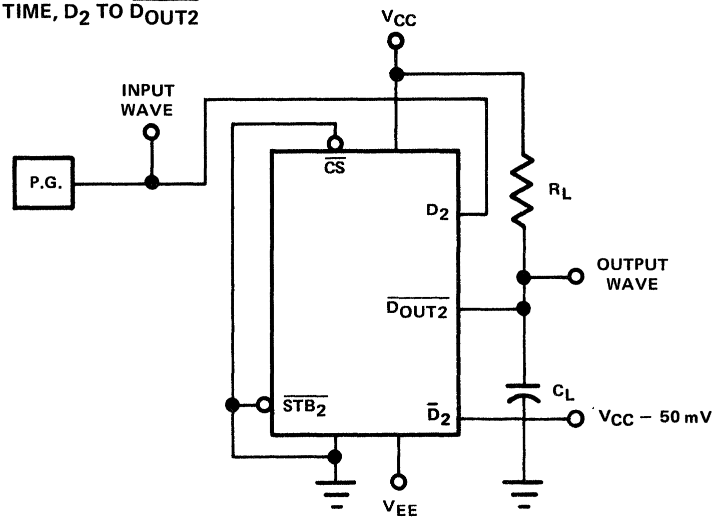


FIG. 19 – PROPAGATION DELAY TIME, D_2 TO $\overline{D_{OUT2}}$



INPUT PULSE CONDITIONS

$t_{THL} = t_{TLH} = 3$ ns
$t_W = 50$ ns
f = 5 MHz
INPUT AMPLITUDE
$V_P = 100$ mV

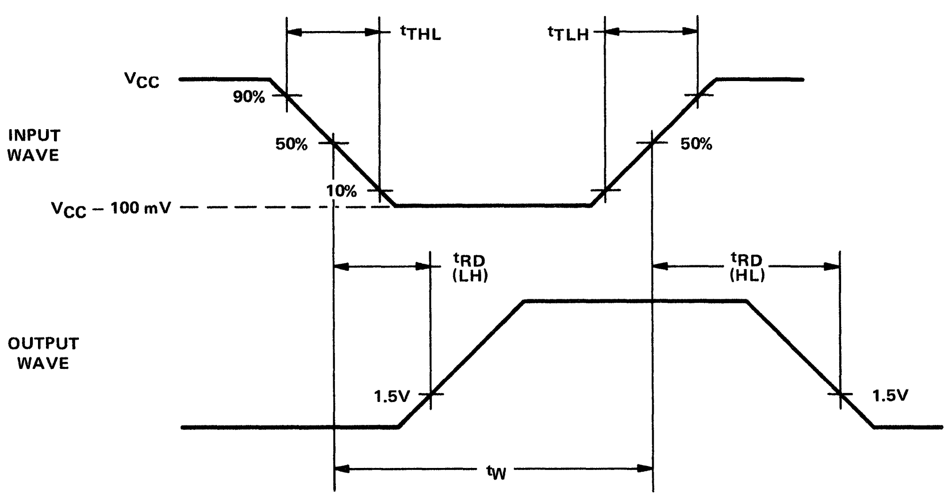


FIG. 20 – PROPAGATION DELAY TIME, $\overline{STB_2}$

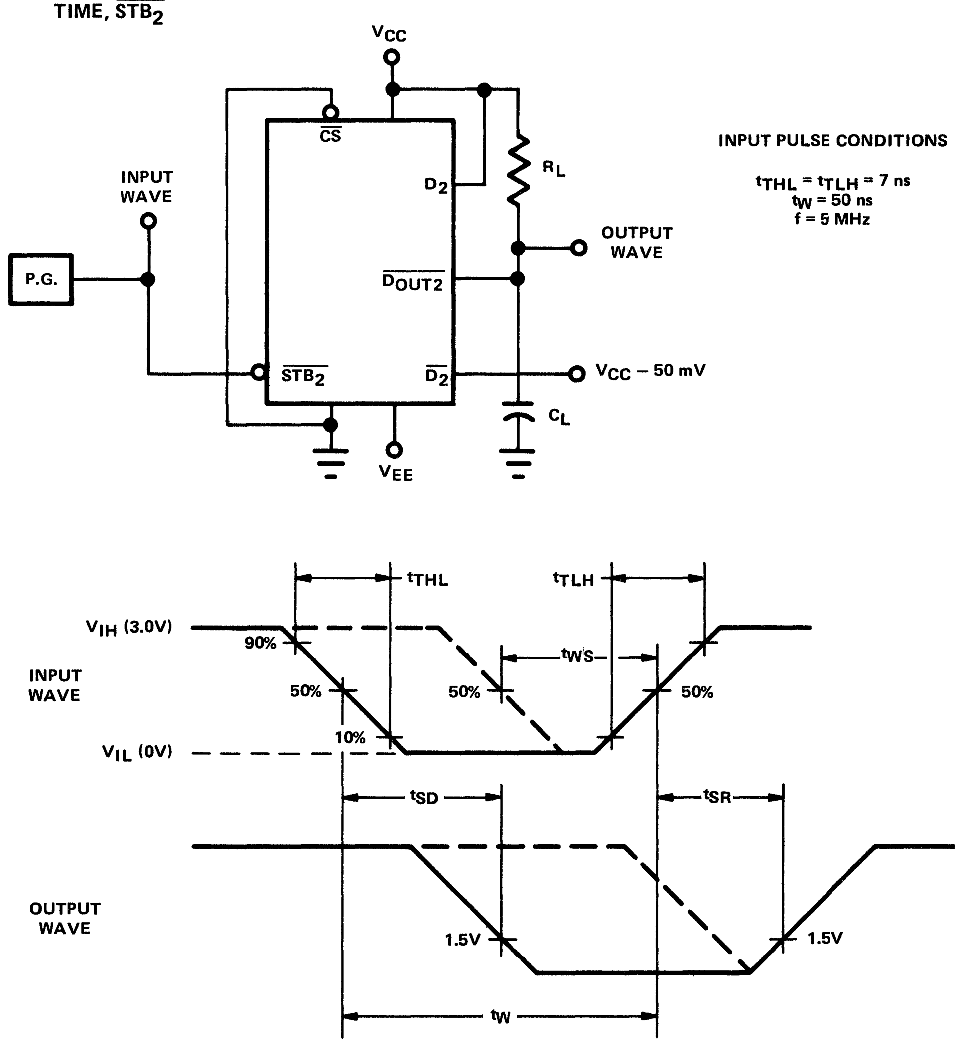
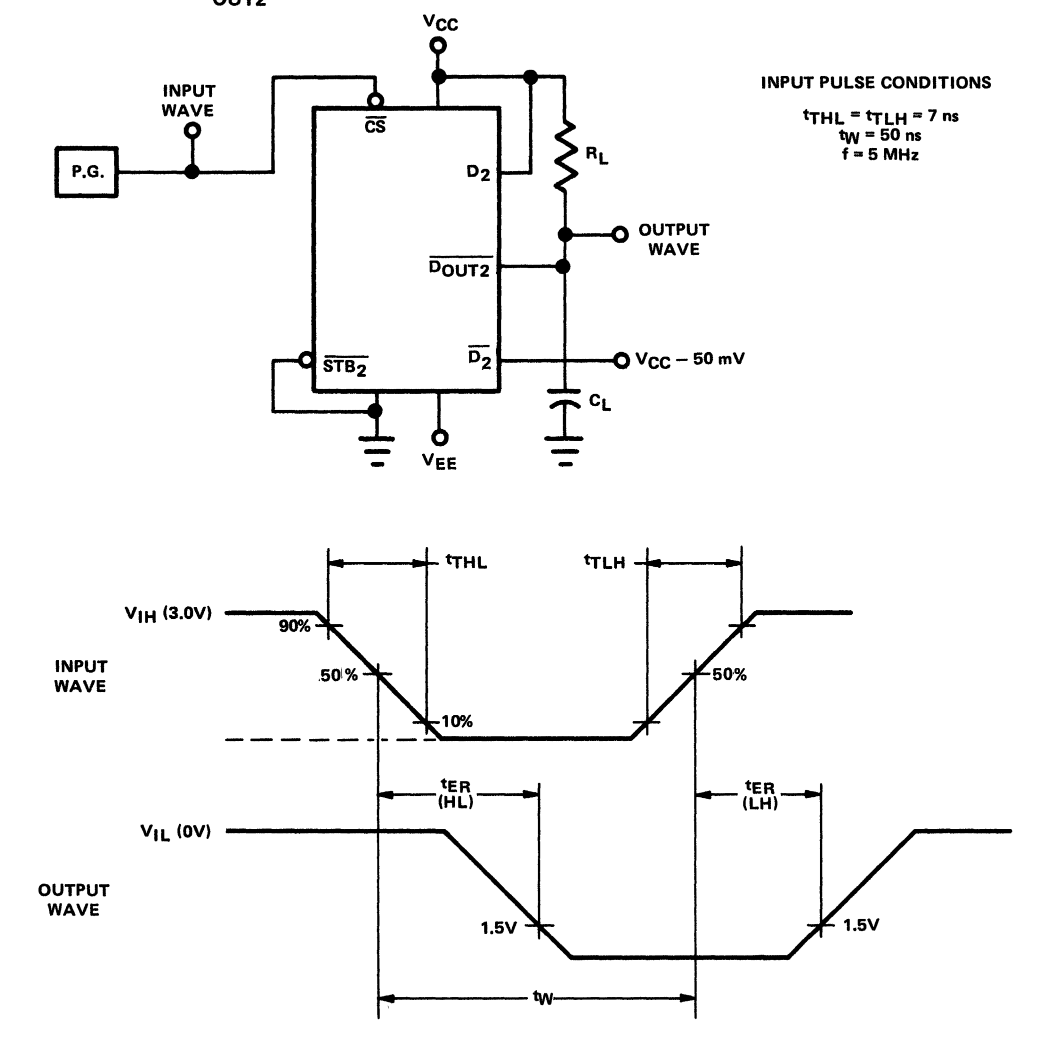
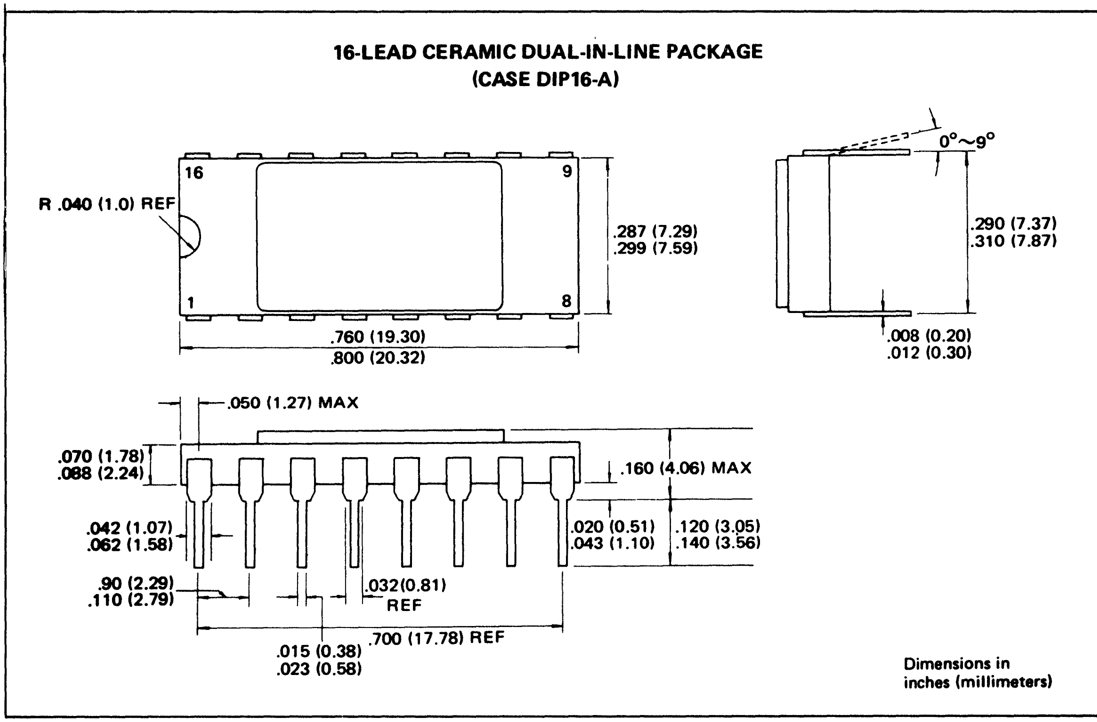


FIG. 21 — PROPAGATION DELAY TIME $\overline{CS}$ TO $\overline{D_{OUT2}}$



PACKAGE DIMENSIONS



DUAL SENSE AMPLIFIER

MB 8916

FUJITSU

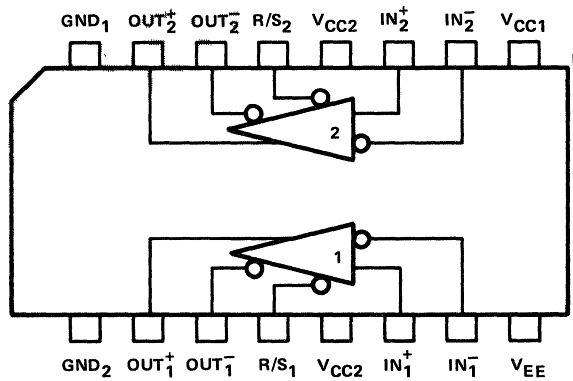
DUAL SENSE AMPLIFIER

The MB8916 is an ECL (CML) compatible high speed sense amplifier.

This sense amplifier senses output signal of the MOS memory devices (such as MB8215, MB8207) and converts the signal to ECL (CML) level.

- High speed operation:
  Read delay time, 4.5 ns max.
  Strobe delay time, 3.2 ns max.
- High input sensitivity
- ECL (CML) compatible input/output
- Standard ceramic 16-leads dual-in-line package

PIN ASSIGNMENT



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC2} V_{CC1} V_{EE}	−0.3 to +10.5 −0.3 to + 6.5 −8.0 to +0.3	V V V
Input Voltage	V_I $V_{R/S}$	−0.3 to V_{CC2} + 0.5 −5.0 to +0.3	V V
Input Difference Voltage (between In^+ and In^-)		±5.0	V
Output Current	I_O	0 to +50	mA
Operating Free-Air Temperature Range	T_{op}	−25 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

TRUTH TABLE

IN	R/S	OUT^+	OUT^-
$IN^+ > IN^-$	L	H	L
$IN^+ < IN^-$	L	L	H
Not Stable	H	L	H

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC2} V_{CC1} V_{EE}	6.5 to 8.5 5.0 ± 5% –5.2 ± 5%	V V V
Input Voltage	V_I	3.2 to V_{CC2} +0.25	V
Input Difference Voltage	V_{ID}	±4.5	V
Operating Free-Air Temperature Range	T_{op}	0 to +70	°C

Note: When one of S/A circuit is left unused, inputs of the circuit should be biased in the range of the recommended input voltage (ex. V_{CC2}) to ensure operation of the other circuit.

DC CHARACTERISTICS

Characteristics	Symbol	$T_A = 0°C$			$T_A = 25°C$			$T_A = 70°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Offset Voltage	V_{IO}				-3	±1	+ 3				mV	
Input Offset Current	I_{IO}				−1	±0.1	+ 1				μA	
Input Current	I_{IN}					7	20				μA	
Voltage Gain	G_V					57					dB	
Output Voltage High Level *1	V_{OH}	−1.005		−0.845	−0.960	−0.900	−0.810	−0.905		−0.730	V	$V_{IN}^+ = 7.0V$ (7.1V) $V_{IN}^- = 7.1V$ (7.0V)
Output Voltage Low Level *1	V_{OL}	−1.870		−1.660	−1.850	−1.750	−1.650	−1.830		−1.625	V	$V_{IN}^+ = 7.0V$ (7.1V) $V_{IN}^- = 7.1V$ (7.0V)
Output Voltage High Level *2	V_{OHA}	−1.020			−0.980			−0.925			V	Same as above
Output Voltage Low Level *2	V_{OLA}			−1.640			−1.630			−1.605	V	Same as above
Input Current (R/S) High Level	I_{IH}						265				μA	
Input Current (R/S) Low Level	I_{IL}				0.5						μA	
Supply Current V_{CC1}	I_{CC1}				10.0	14.8	19.0				mA	
V_{CC2}	I_{CC2}				9.0	14.4	18.5				mA	
V_{EE}	I_{EE}				25.0	35.3	45.0				mA	

*1. R/S: V_{IH}max. & open.
*2. R/S: V_{IH}min. & V_{IL}max.

Power Supply Voltage: $V_{CC1} = 5.0V$, $V_{CC2} = 7.0V$, $V_{EE} = -5.2V$

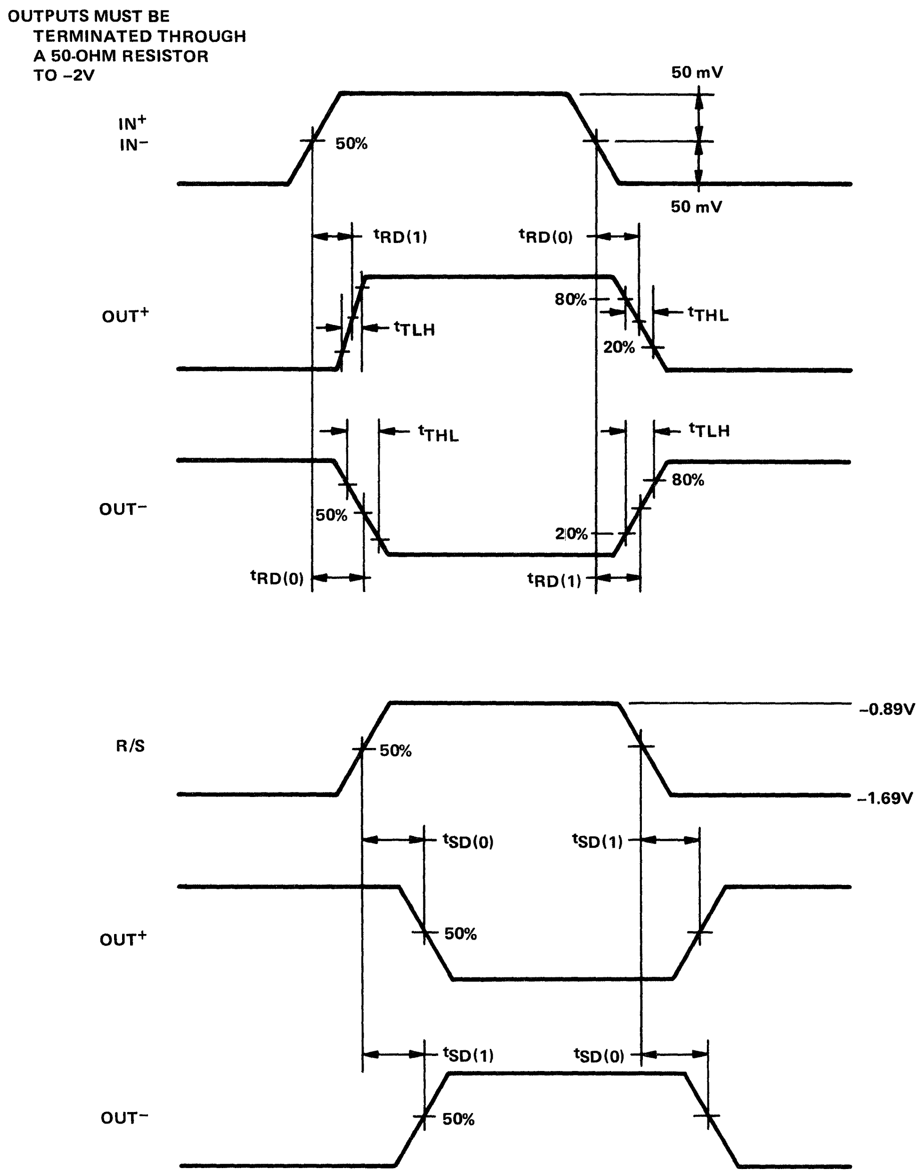
Bias Voltage:	V_{IH} max.	V_{IL} min.	V_{IHA} min.	V_{ILA} max.
T_A: 0°C	−0.845	−1.870	−1.150	−1.490
25°C	−0.810	−1.850	−1.105	−1.475
70°C	−0.730	−1.830	−1.055	−1.450

Outputs must be connected to a 50-ohm resistor to −2V.

AC CHARACTERISTICS

Characteristics	Symbol	$T_A = 0°C$			$T_A = 25°C$			$T_A = 70°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read Delay Time	$t_{RD(1)}$											
	$t_{RD(0)}$			3.8	2.0	2.9	3.8			4.5	ns	
Strobe Delay Time	$t_{SD(1)}$											
	$t_{SD(0)}$			2.6	1.0	1.9	2.6			3.2	ns	
Output Rise Time	t_{TLH}			1.5		0.9	1.5			2.1	ns	
Output Fall Time	t_{THL}			1.5		0.8	1.5			2.1	ns	

WAVEFORMS



*This specification is applicable under the condition of 2.5m/sec air flow.

FUJITSU

4-BIT BUS DRIVER/RECEIVER

MB 424

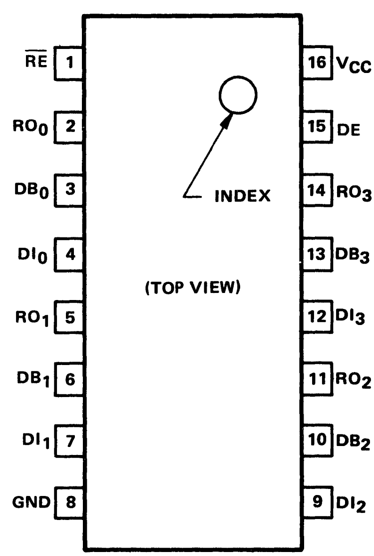
4-BIT DRIVER/RECEIVER

The Fujitsu MB 424 is a 4-bit bus driver/receiver which has two control lines to enable drivers or receivers. This device is suitable to expand the bi-directional data bus and the address lines for the microcomputer system using the Fujitsu MBL 6800 microprocessor unit or similar devices.

- Schottky clamped TTL
- 3-state outputs
- "L" level output sink current:
  40 mA (Driver)
  16 mA (Receiver)
- "H" level output current:
  10 mA (Driver)
  2 mA (Receiver)
- Low input load current by using PNP transistor: 200 μA max.
- Schottky input-clamping diode
- High speed operation with high capacitance load
  Driver: t_{pd} = 12 ns typ.,
  20 ns max. at 300 pF
  Receiver: t_{pd} = 7 ns typ.,
  14 ns max at 30 pF
- Especially high speed operation on 3-state
- Pin compatible with Signetics 8T26 and Motorola MC6880
- Standard 16-pin dual-in-line package

SYMBOL	PIN NAME
$\overline{RE}$	RECEIVER ENABLE
DE	DRIVER ENABLE
DI	DATA INPUT
DB	DATA BUS
RO	RECEIVER OUTPUT

PIN ASSIGNMENT



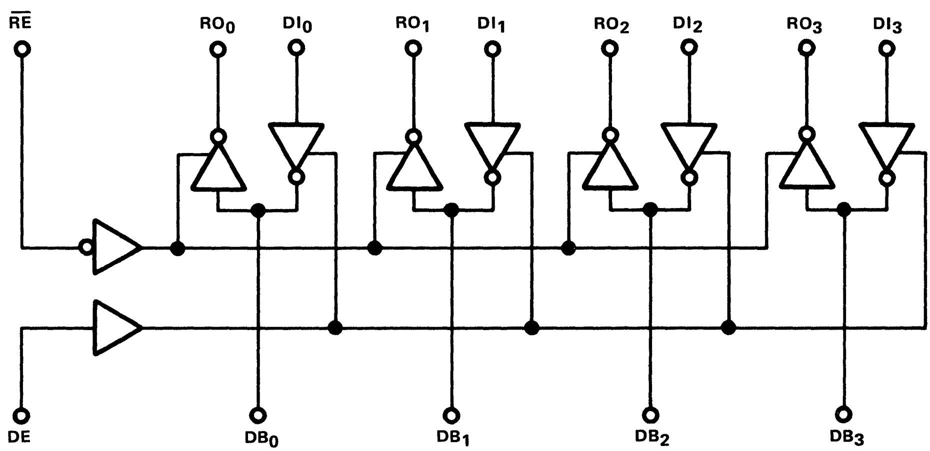
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to GND Pin	V_{CC}	− 0.5 to +7.0	V
Input Voltage	V_I	− 1.0 to +5.5	V
Output Voltage	V_O	− 0.5 to +7.0	V
Operating Temperature	T_{op}	−15.0 to +75.0	°C
Storage Temperature	T_{stg}	−40.0 to +125.0	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

FUNCTIONAL DESCRIPTION/APPLICATION INFORMATION

LOGIC DIAGRAM



FUNCTION TABLE

Mode Control		Driver State	Receiver State	Reference Figure
$\overline{RE}$	DE			
0	0	HZ	RO = $\overline{DB}$	Fig. 1
0	1	DB = $\overline{DI}$	RO = DI	Fig. 2
1	0	HZ	HZ	Fig. 3
1	1	DB = $\overline{DI}$	HZ	Fig. 4

HZ: high impedance state.

REFERENCE FIGURE

FIG. 1

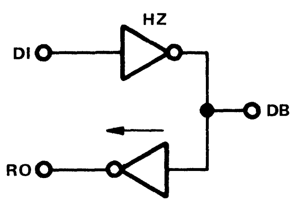


FIG.2

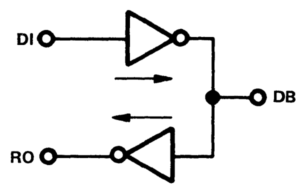


FIG. 3

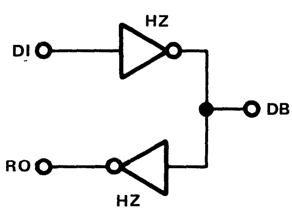
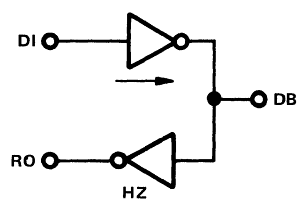


FIG. 4



APPLICATIONS

- Half-duplex data transmission
- Memory interface buffer
- Data routing in bus-oriented system
- MOS/CMOS to TTL interface
- High current driver

GUARANTEED OPERATING RANGES

Item	Symbol	Range	Unit
Supply Voltage	V_{CC}	+4.75 to + 5.25	V
Driver Output Current "H" state "L" state	 I_{OHD} I_{OLD}	 10 Max. 40 Max.	 mA mA
Receiver Output Current "H" state "L" state	 I_{OHR} I_{OLR}	 2 Max. 16 Max.	 mA mA
Ambient Temperature	T_A	0 to +75	°C

DC CHARACTERISTICS

(T_A = 0°C to +75°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Test Circuit
Output High Voltage for DB (V_{CC} = 4.75V, I_{OH} = −10 mA, V_{IL} = 0.85V)	V_{OH1}	2.6	3.3	—	V	Fig. 1
Output High Voltage for RO (V_{CC} = 4.75V, I_{OH} = −2 mA, V_{IL} = 0.85V)	V_{OH2}	2.6	3.2	—	V	Fig. 2
Output Low Voltage for DB (V_{CC} = 4.75V, I_{OL} = 40 mA, V_{IH} = 2.0V)	V_{OL1}	—	—	0.5	V	Fig. 3
Output Low Voltage for RO (V_{CC} = 4.75V, I_{OL} = 16 mA, V_{IH} = 2.0V)	V_{OL2}	—	—	0.5	V	Fig. 4
Input High Current for RE, DE and DI (V_{CC} = 5.25V, V_{IH} = 5.5V)	I_{IH}	—	—	25	μA	Fig. 5 Fig. 6
Input Low Current for All Inputs (V_{CC} = 5.25V, V_{IL} = 0.4V)	I_{IL}	—	-40	-200	μA	Fig. 7 Fig. 8 Fig. 9
Output Short Circuit Current for DB (V_{CC} = 5.25V)	I_{OS1}	-50	—	-150	mA	Fig. 10
Output Short Circuit Current for RO (V_{CC} = 5.25V)	I_{OS2}	-30	—	- 75	mA	Fig. 11
Output Leakage Current for DB/RO (High Impedance State, V_{CC} = 5.25V, V_O = 5.25V/0.4V)	I_{OZ}	—	—	±100	μA	Fig. 12
Power Supply Current (All Outputs are High, V_{CC} = 5.25V)	I_{CCH}	—	39	71	mA	Fig. 13
Power Supply Current (All Outputs are Low, V_{CC} = 5.25V)	I_{CCL}	—	51	87	mA	Fig. 14
Input Clamp Voltage for All Inputs (V_{CC} = 4.75V, I_{IL} = −5 mA	V_{IC}	—	—	−1.0	V	Fig. 15 Fig. 16

*All typical values are at V_{CC} = 5.0V and T_A = 25°C.

AC CHARACTERISTICS (see NOTE)

(V_{CC} = 5.0V, T_A = 25°C ± 2°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Circuit
Propagation Delay Time DI to DB (R_1 = 30 ohm, R_2 = 260 ohm, C_L = 300 pF)	t_{PLH} t_{PHL}	—	11 13	20 20	ns ns	Fig. 17
Propagation Delay Time DB to RO (R_1 = 92 ohm, R_2 = 1.3K ohm, C_L = 30 pF)	t_{PLH} t_{PHL}	—	7 7	14 14	ns ns	Fig. 18
Driver Enable Time (R_3 = 70 ohm, R_4 = 2.4K ohm, R_5 = 5K ohm, C_L = 300 pF)	t_{PZL}	—	20	35	ns	Fig. 19
Driver Disable Time (R_3 = 70 ohm, R_4 = 2.4K ohm, R_5 = 5K ohm, C_L = 300 pF)	t_{PLZ}	—	12	25	ns	Fig. 19
Receiver Enable Time (R_3 = 240 ohm, R_4 = 2.4K ohm, R_5 = 5K ohm, C_L = 30 pF)	t_{PZL}	—	17	30	ns	Fig. 20
Receiver Disable Time (R_3 = 240 ohm, R_4 = 2.4K ohm, R_5 = 5K ohm, C_L = 30 pF)	t_{PLZ}	—	8	15	ns	Fig. 20

Note: C_L includes jig and probe capacitance.

DC/AC TEST CIRCUIT

FIG. 1 V_{OH1}

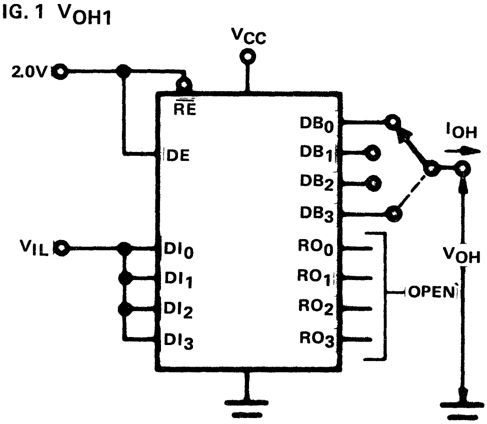
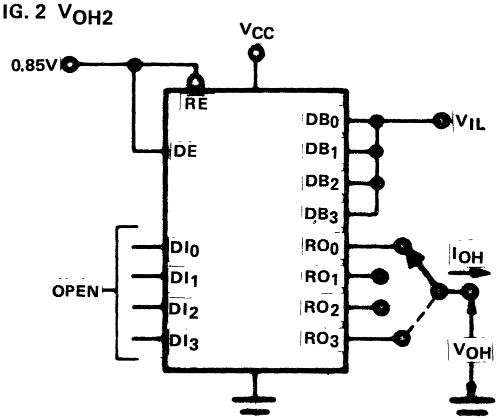


FIG. 2 V_{OH2}



Interface Devices

FIG. 3 V_{OL1}

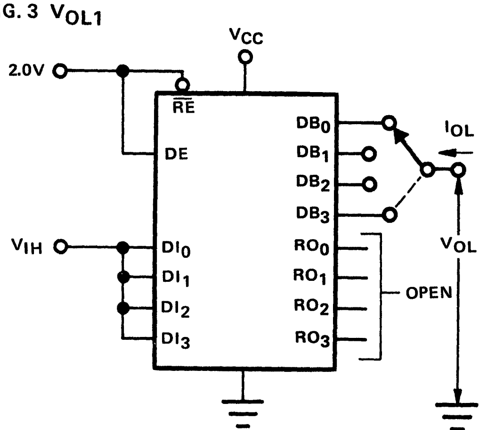


FIG. 4 V_{OL2}

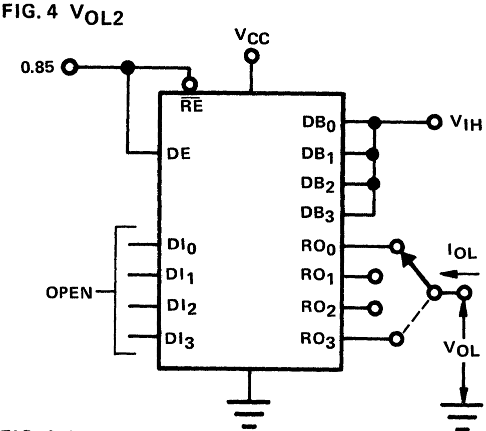


FIG. 5 I_{IH}

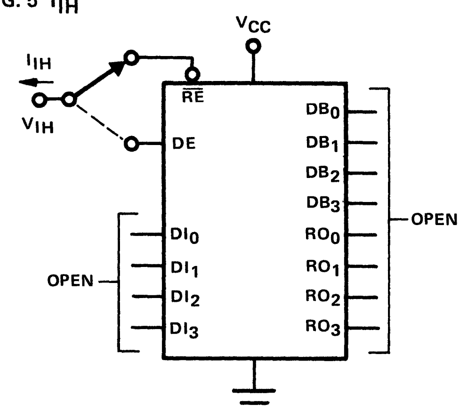


FIG. 6 I_{IH}

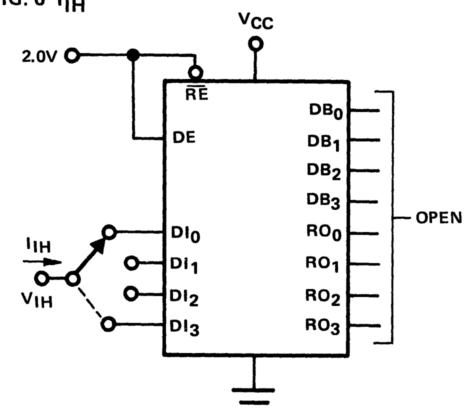


FIG. 7 I_{IL}

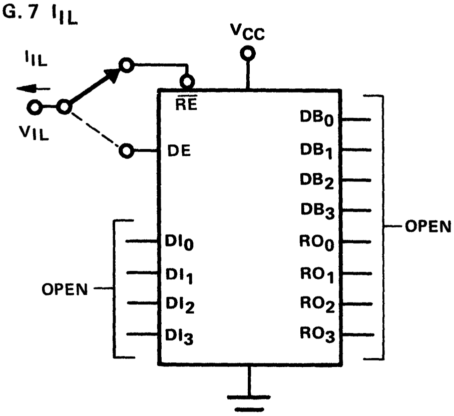


FIG. 8 I_{IL}

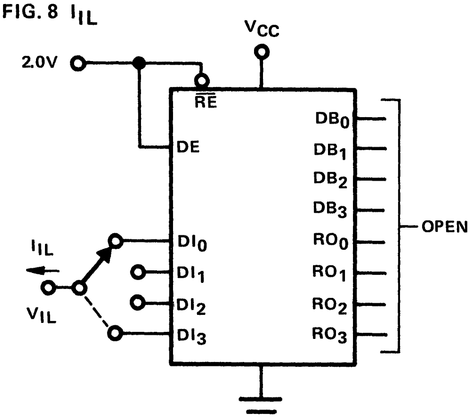


FIG. 9 I_{IL}

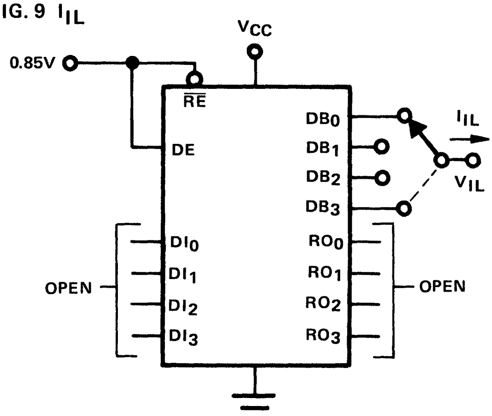


FIG. 10 I_{OS1}

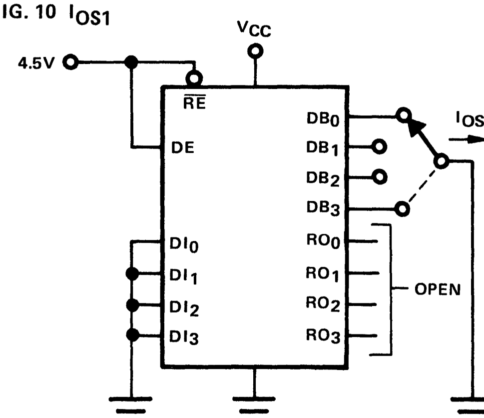


FIG. 11 I_{OS2}

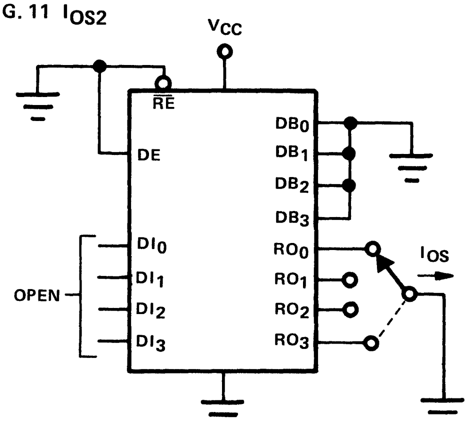


FIG. 12 I_{OZ}

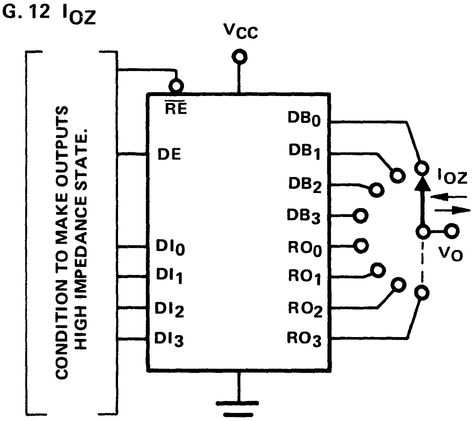


FIG. 13 I_{CCH}

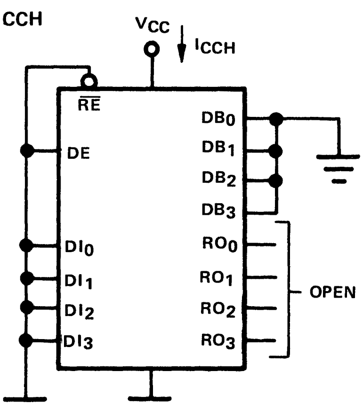
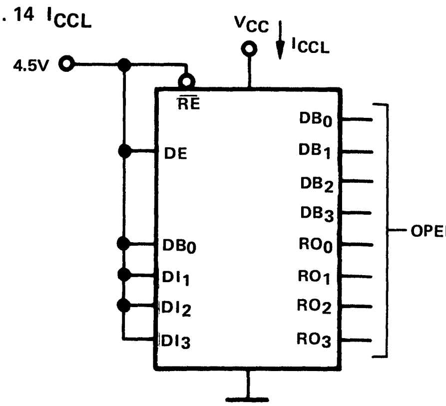


FIG. 14 I_{CCL}



Interface Devices

FIG. 15 V_{IC}

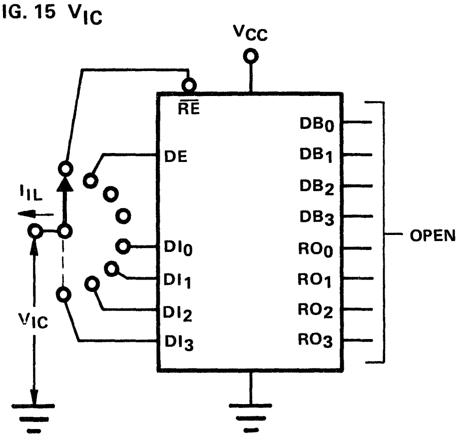


FIG. 16 V_{IC}

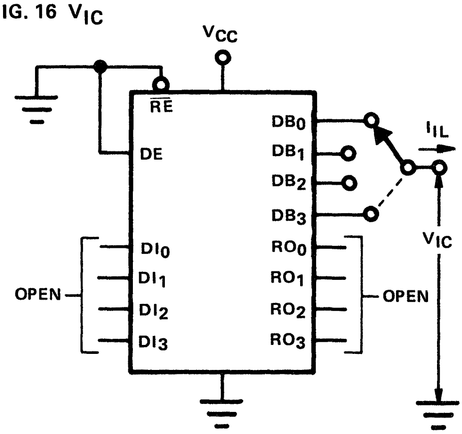


Fig. 17–t_{PLH}/t_{PHL} (DI TO DB)

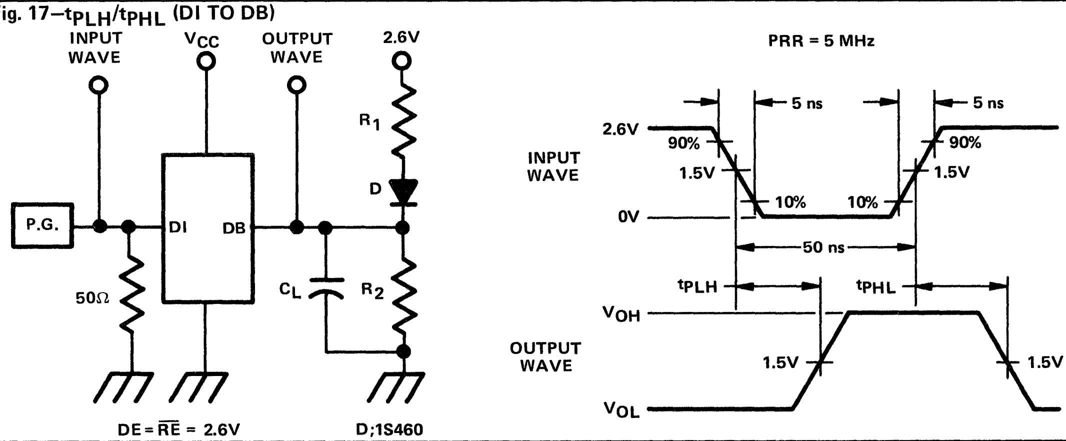


Fig. 18—t_{PLH}/t_{PHL} (DB TO RO)

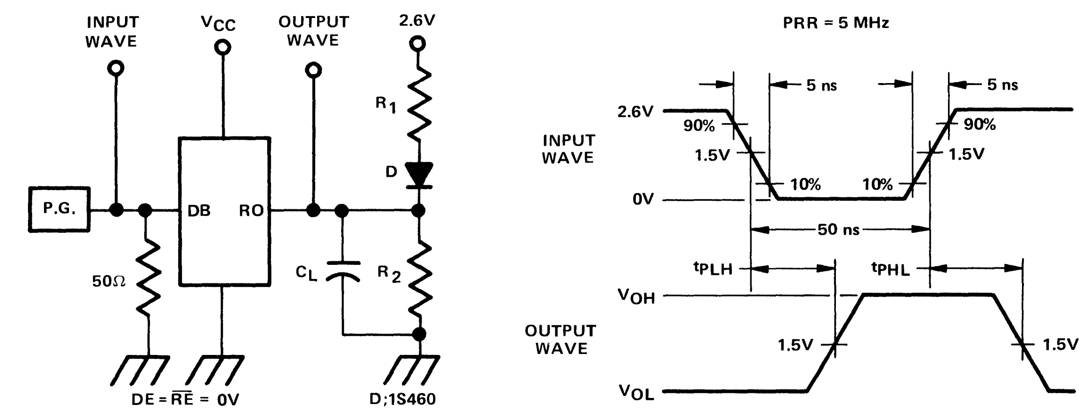


Fig. 19—t_{PZL}/t_{PLZ} (DRIVER)

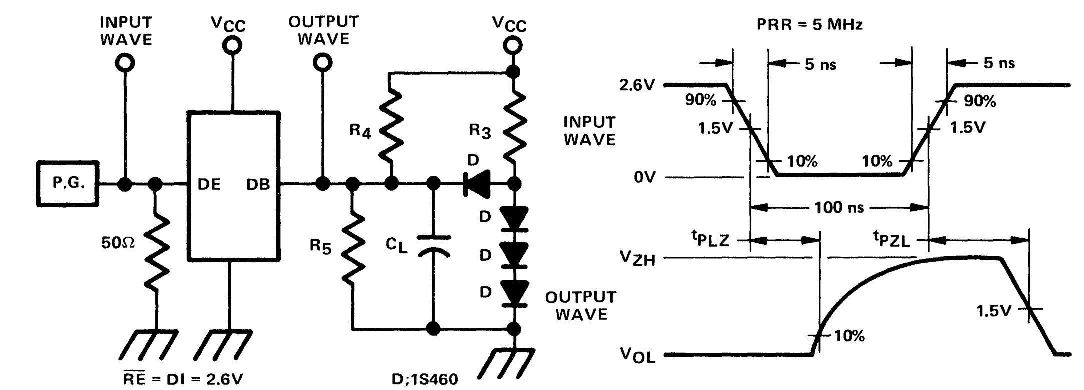
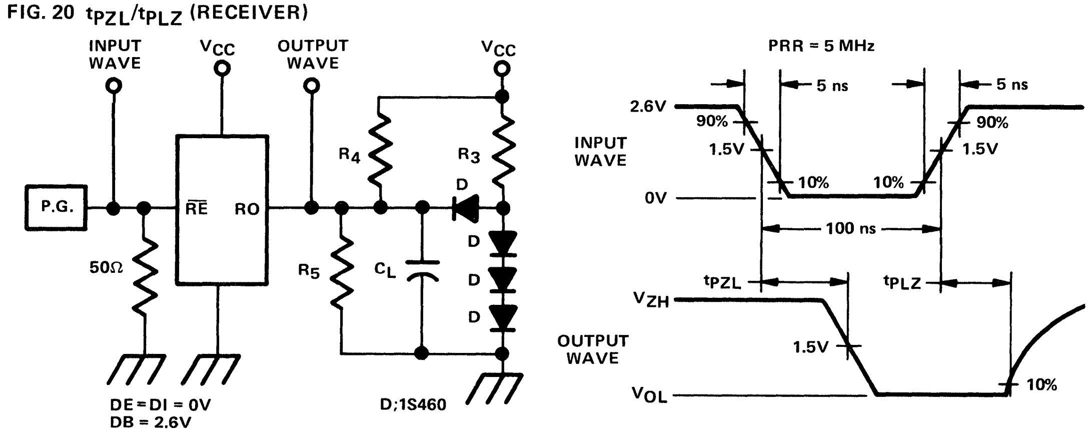
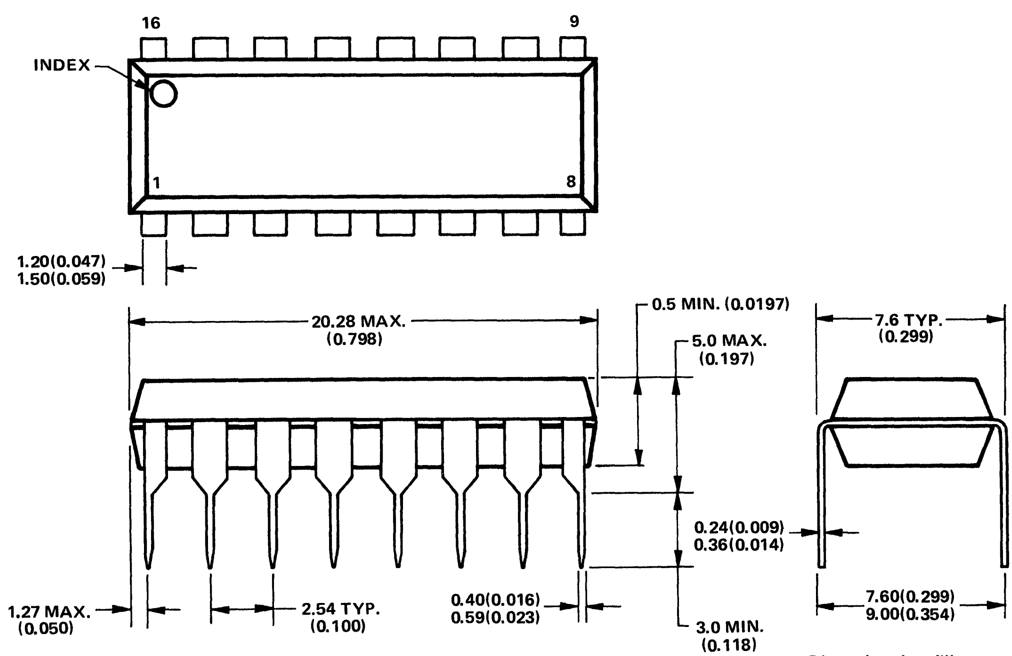


FIG. 20 t_{PZL}/t_{PLZ} (RECEIVER)



PACKAGE DIMENSIONS



FUJITSU

4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER (NON-INVERTING) MB 425

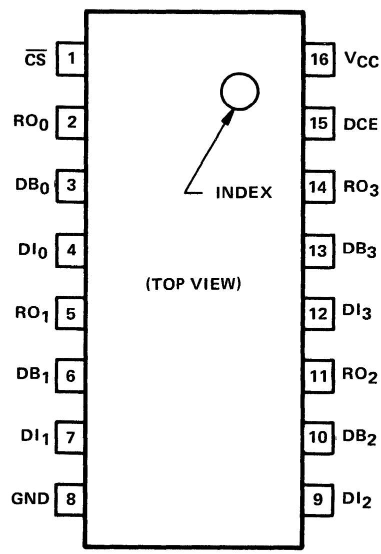
4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER (NON-INVERTING)

The Fujitsu MB 425 is a 4-bit non-inverting bi-directional bus driver/receiver. The function of driver or receiver is selected by Direction Control input. This device is designed for non-inverting data bus buffer/driver of the Fujitsu MBL 6800 microprocessor unit or similar devices.

- Schottky clamped TTL
- 3-state outputs
- "L" level output sink current:
  55 mA (Driver)
  16 mA (Receiver)
- "H" level output current:
  10 mA (Driver)
  1 mA (Receiver)
- "H" level output voltage (I_{OH} = −1 mA): 3.65V min.
- Low input load current by using PNP transistor: 250 μA max.
- High-speed operation with high capacitance load
  Driver: t_{pd} = 17 ns typ., 30 ns max. at 300 pF
  Receiver: t_{pd} = 10 ns typ., 25 ns max. at 30 pF
- Especially high speed operation on 3-state
- Pin compatible with Intel 8216
- Standard 16-pin dual-in-line package

SYMBOL	PIN NAME
$\overline{CS}$	CHIP SELECT
DCE	DIRECTION CONTROL ENABLE
DI	DATA INPUT
DB	DATA BUS
RO	RECEIVER OUTPUT

PIN ASSIGNMENT



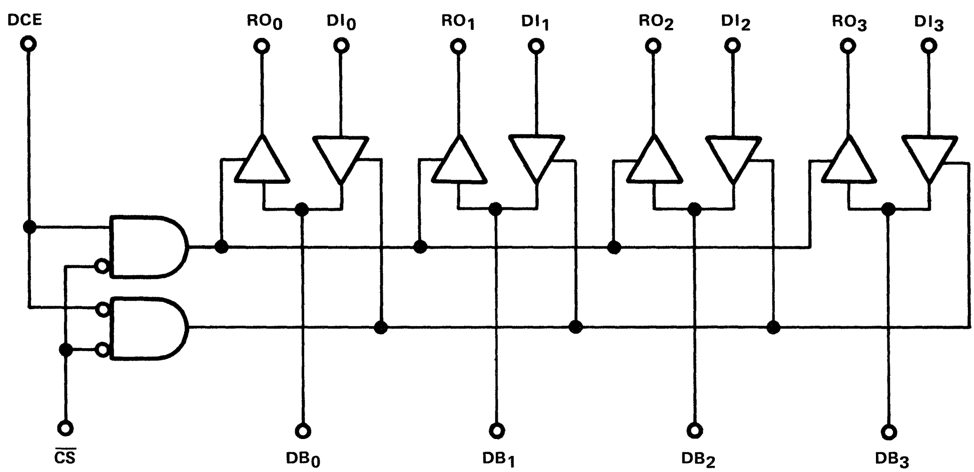
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to GND Pin	V_{CC}	− 0.5 to +7.0	V
Input Voltage	V_I	− 1.0 to +5.5	V
Output Voltage	V_O	− 0.5 to +7.0	V
Operating Temperature	T_{op}	−15.0 to +75.0	°C
Storage Temperature	T_{stg}	−40.0 to +125.0	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

FUNCTIONAL DESCRIPTION/APPLICATION INFORMATION

LOGIC DIAGRAM



FUNCTION TABLE

Mode Control		Driver State	Receiver State	Reference Figure
$\overline{CS}$	DCE			
0	0	DB = DI	HZ	Fig. 1
0	1	HZ	RO = DB	Fig. 2
1	0	HZ	HZ	Fig. 3
1	1	HZ	HZ	Fig. 4

HZ : high impedance state

REFERENCE FIGURE

FIG. 1

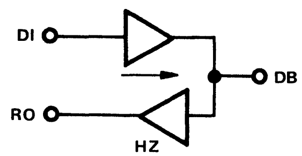


FIG. 2

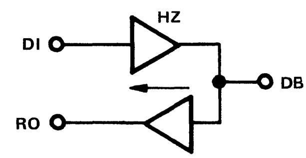


FIG. 3

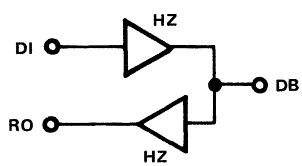
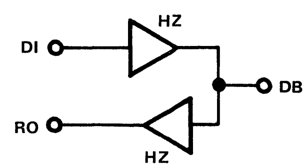


FIG. 4



APPLICATIONS

- Data Bus Buffer for the Fujitsu MBL 6800 microprocessor unit or similar devices.
- Interface Buffer of memory and I/O device to a bi-directional bus of microcomputer system.

GUARANTEED OPERATING RANGES

Item	Symbol	Range	Unit
Supply Voltage	V_{CC}	+4.75 to +5.25	V
Driver Output Current			
"H" state	I_{OHD}	10 Max.	mA
"L" state	I_{OLD}	55 Max.	mA
Receiver Output Current			
"H" state	I_{OHR}	1 Max.	mA
"L" state	I_{OLR}	16 Max.	mA
Ambient Temperature	T_A	0 to +75	°C

DC CHARACTERISTICS (see NOTE)

(T_A = 0°C to 75°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Circuit
Output High Voltage for RO (V_{CC} = 4.75V, I_{OH} = −1 mA, V_{IH} = 2.0V)	V_{OH1}	3.65	4.2	–	V	Fig. 1
Output High Voltage for DB (V_{CC} = 4.75V, I_{OH} = −10 mA, V_{IH} = 2.0V)	V_{OH2}	2.4	3.2	–	V	Fig.2
Ouput Low Voltage for RO/DB (V_{CC} = 4.75V, I_{OL} = 16 mA/25 mA, V_{IL} = 0.95V)	V_{OL1}	–	–	0.45	V	Fig. 3 Fig. 4
Output Low Voltage for DB (V_{CC} = 4.75V, I_{OL} = 55 mA, V_{IL} = 0.95V)	V_{OL2}	–	–	0.6	V	Fig. 3
Input High Current for $\overline{CS}$ and DCE (V_{CC} = 5.25V, V_{IH} = 5.5V)	I_{IH1}	–	–	20	μA	Fig. 5
Input High Current for DI (V_{CC} = 5.25V, V_{IH} = 5.5V)	I_{IH2}	–	–	10	μA	Fig. 6
Input Low Current for $\overline{CS}$ and DCE (V_{CC} = 5.25V, V_{IL} = 0.4V)	I_{IL1}	–	-80	-500	μA	Fig. 7
Input Low Current for DI and DB (V_{CC} = 5.25V, V_{IL} = 0.4V)	I_{IL2}	–	-40	-250	μA	Fig. 8 Fig. 9
Output Short Circuit Current for RO (V_{CC} = 5.25V)	I_{OS1}	-15	–	- 65	mA	Fig. 10
Output Short Circuit Current for DB (V_{CC} = 5.25V)	I_{OS2}	-30	–	-120	mA	Fig. 11
Output Leakage Current for RO (high impedance state, V_{CC} = 5.25V, V_O = 0.45V/5.25V)	I_{OZ1}	–	–	± 20	μA	Fig. 12
Output Leakage Current for DB (high impedance state, V_{CC} = 5.25V, V_O = 0.45V/5.25V)	I_{OZ2}	–	–	±100	μA	Fig. 12
Power Supply Current (All Inputs are High, V_{CC} = 5.25V)	I_{CCH}	–	67	130	mA	Fig. 13
Power Supply Current (All Inputs are Low, V_{CC} = 5.25V)	I_{CCL}	–	69	130	mA	Fig. 14
Input Clamp Voltage for All Inputs (V_{CC} = 4.75V, I_{IL} = −5 mA)	V_{IC}	–	–	- 1.0	V	Fig. 15 Fig. 16

Note: All typical values are at V_{CC} = 5.0V and T_A = 25°C.

AC CHARACTERISTICS (see NOTE)

(V_{CC} = 5.0V, T_A = 25°C ± 2°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Circuit
Propagation Delay Time DB to RO (R_1 = 300 ohm, R_2 = 600 ohm, C_L = 30 pF)	t_{PLH} t_{PHL}	– –	10 10	25 25	ns ns	Fig. 17
Propagation Delay Time DI to DB (R_1 = 90 ohm, R_2 = 180 ohm, C_L = 300 pF)	t_{PLH} t_{PHL}	– –	15 20	30 30	ns ns	Fig. 18
Receiver Enable Time (R_1 = 300 ohm, R_2 = 600 0hm, C_L = 30 pF)	t_{PZL}	–	16	35	ns	Fig. 19
Receiver Disable Time (R_1 = 300 ohm, R_2 = 600 ohm, C_L = 5 pF)	t_{PLZ}	–	15	35	ns	
Receiver Enable Time (R_1 = 10K ohm, R_2 = 1K ohm, C_L = 30 pF)	t_{PZH}	–	30	55	ns	Fig. 20
Receiver Disable Time (R_1 = 10K ohm, R_2 = 1K ohm, C_L = 5 pF)	t_{PHZ}	–	10	25	ns	
Driver Enable Time (R_1 = 90 ohm, R_2 = 180 ohm, C_L = 300 pF)	t_{PZL}	–	23	45	ns	Fig. 21
Driver Disable Time (R_1 = 90 ohm, R_2 = 180 ohm, C_L = 5 pF)	t_{PLZ}	–	6	20	ns	
Driver Enable Time (R_1 = 10K ohm, R_2 = 1K ohm, C_L = 300 pF)	t_{PZH}	–	30	55	ns	Fig. 22
Driver Disable Time (R_1 = 10K ohm, R_2 = 1K ohm, C_L = 5 pF)	t_{PHZ}	–	6	20	ns	

Note: C_L includes jig and probe capacitance.

DC/AC TEST CIRCUIT

FIG. 1 V_{OH1}

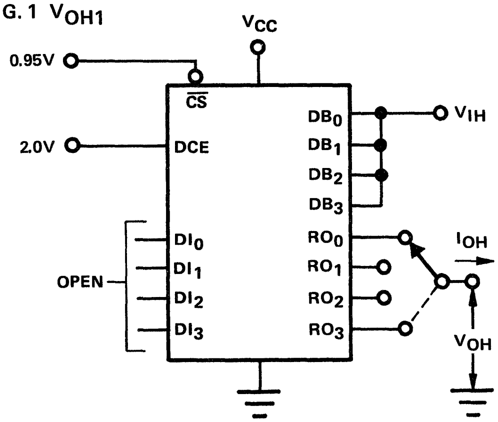


FIG. 2 V_{OH2}

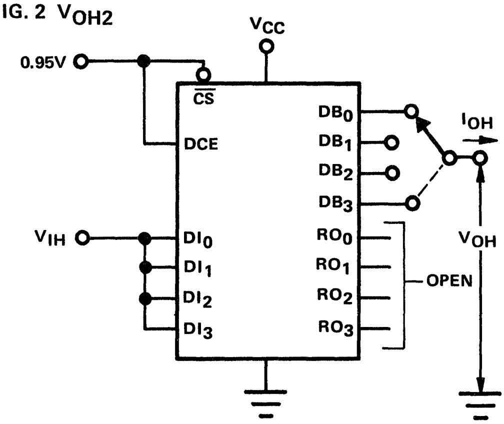


FIG. 3 V_{OL1}/V_{OL2}

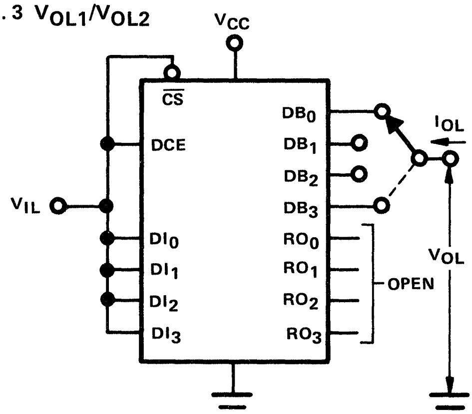


FIG. 4 V_{OL1}

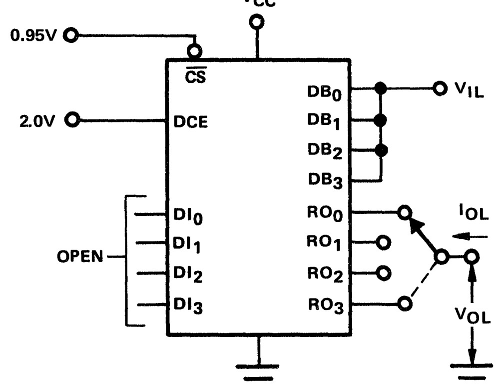


FIG. 5 I_{IH1}

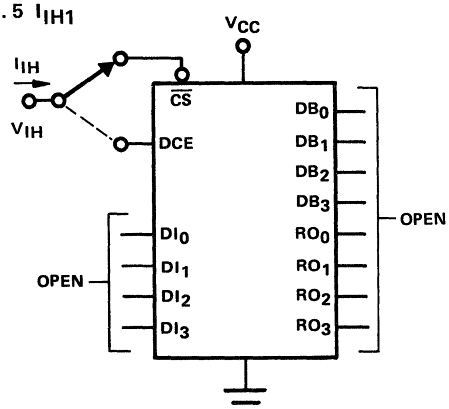


FIG. 6 I_{IH2}

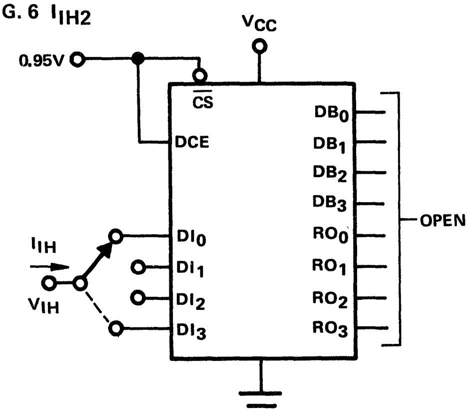


FIG. 7 I_{IL1}

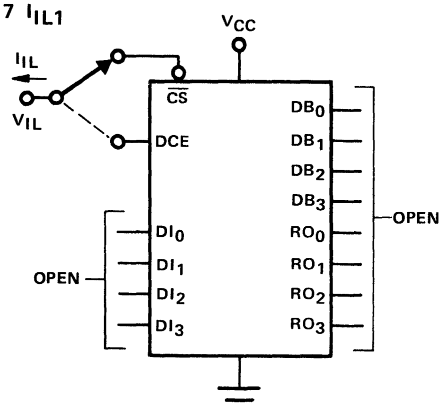


FIG. 8 I_{IL2}

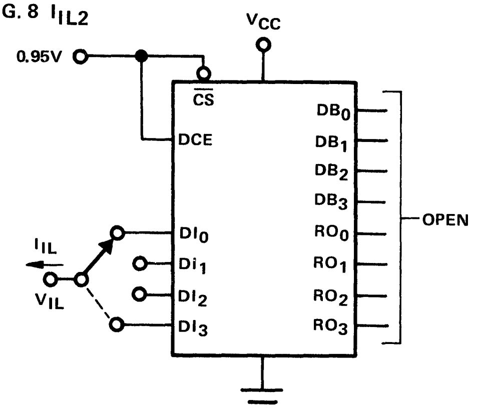


FIG. 9 I_{IL2}

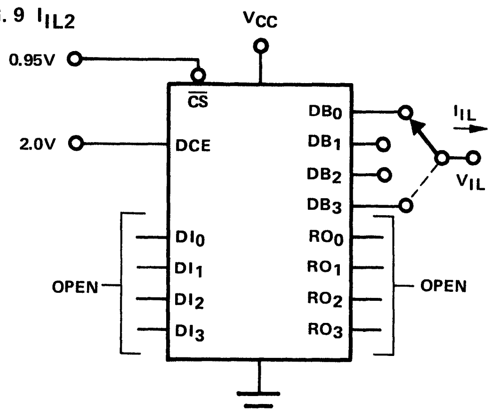


FIG. 10 I_{OS1}

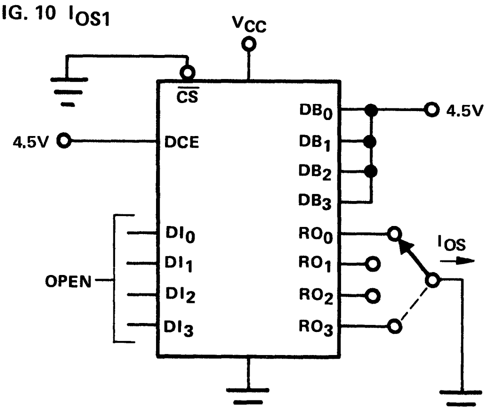


FIG. 11 I_{OS2}

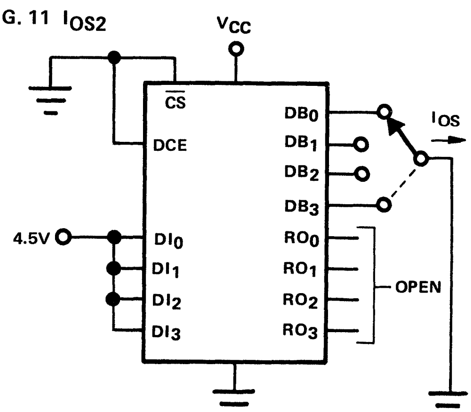


FIG. 12 I_{OZ}

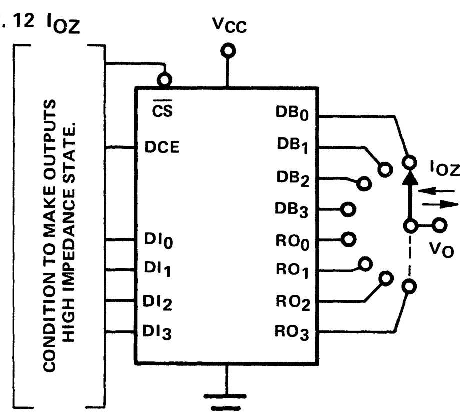


FIG. 13 I_{CCH}

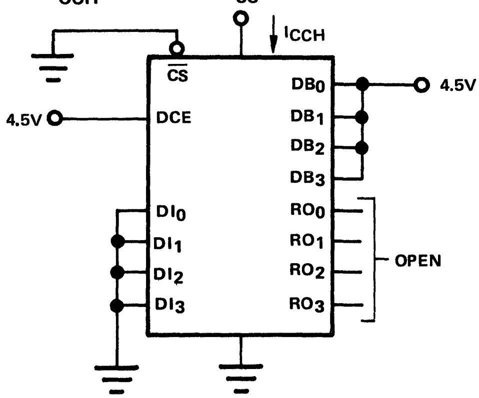


FIG. 14 I_{CCL}

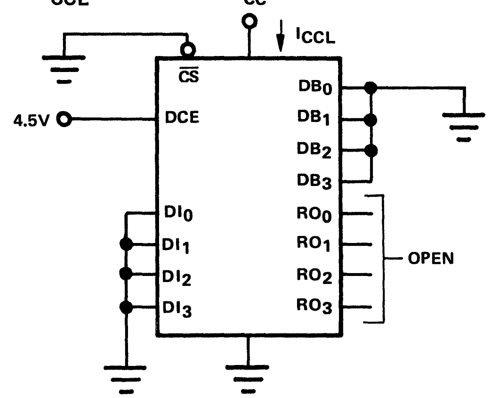


FIG. 15 V_{IC}

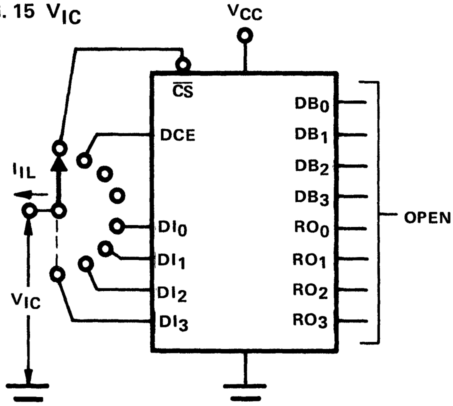


FIG. 16 V_{IC}

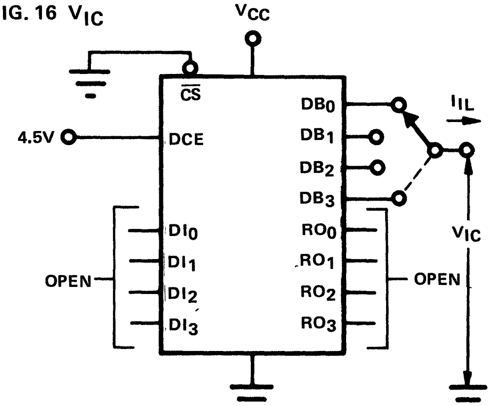


FIG. 17 t_{PLH}/t_{PHL} (DB TO RO)

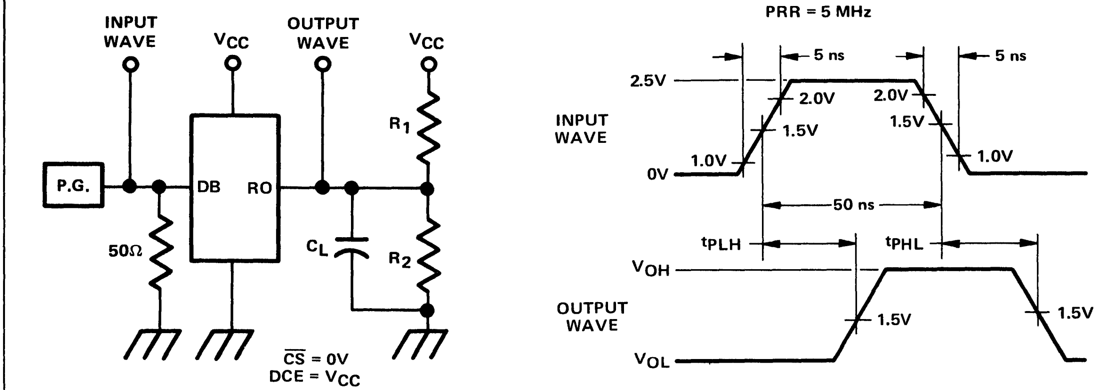


FIG. 18 t_{PLH}/t_{PHL} (BI TO DB)

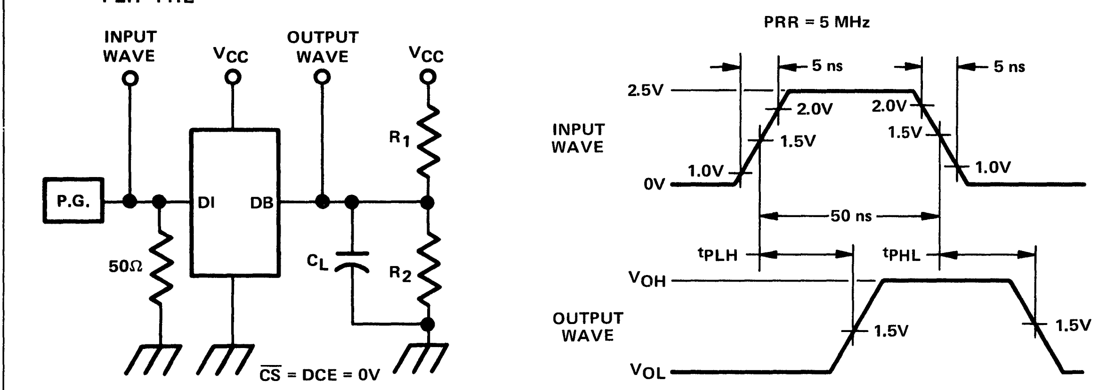
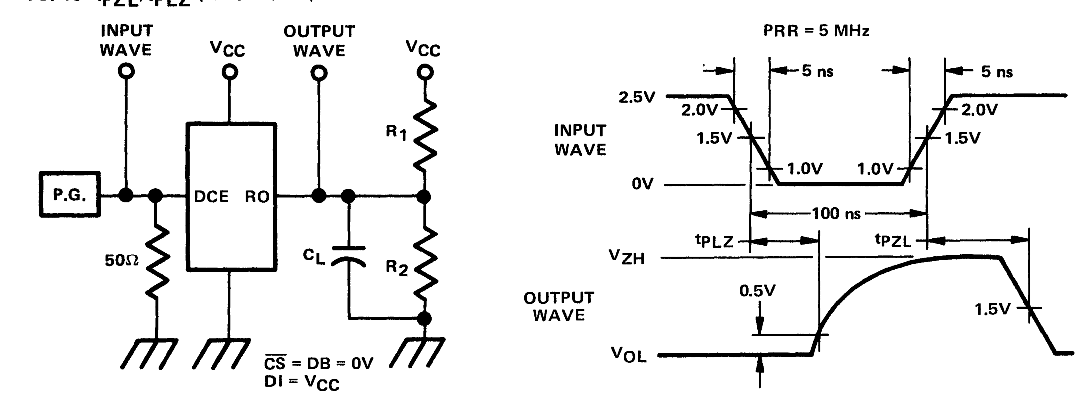


FIG. 19 t_{PZL}/t_{PLZ} (RECEIVER)



Interface Devices

FIG. 20 t_{PZH}/t_{PHZ} (RECEIVER)

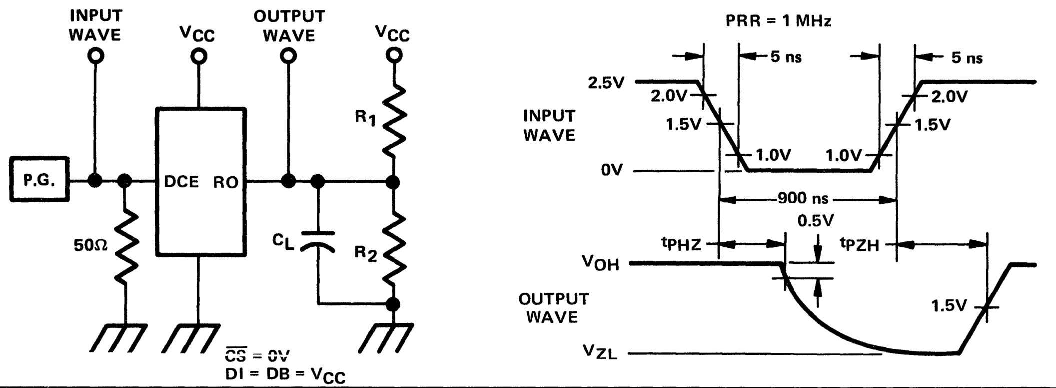


FIG. 21 t_{PZL}/t_{PLZ} (DRIVER)

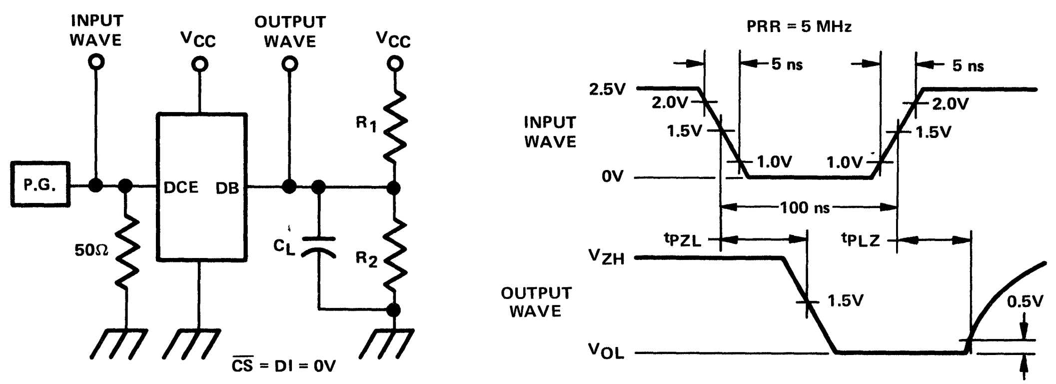
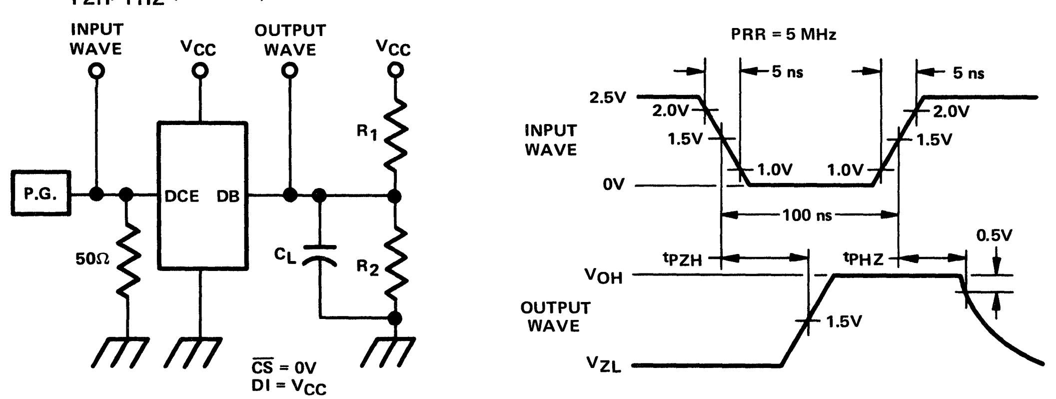
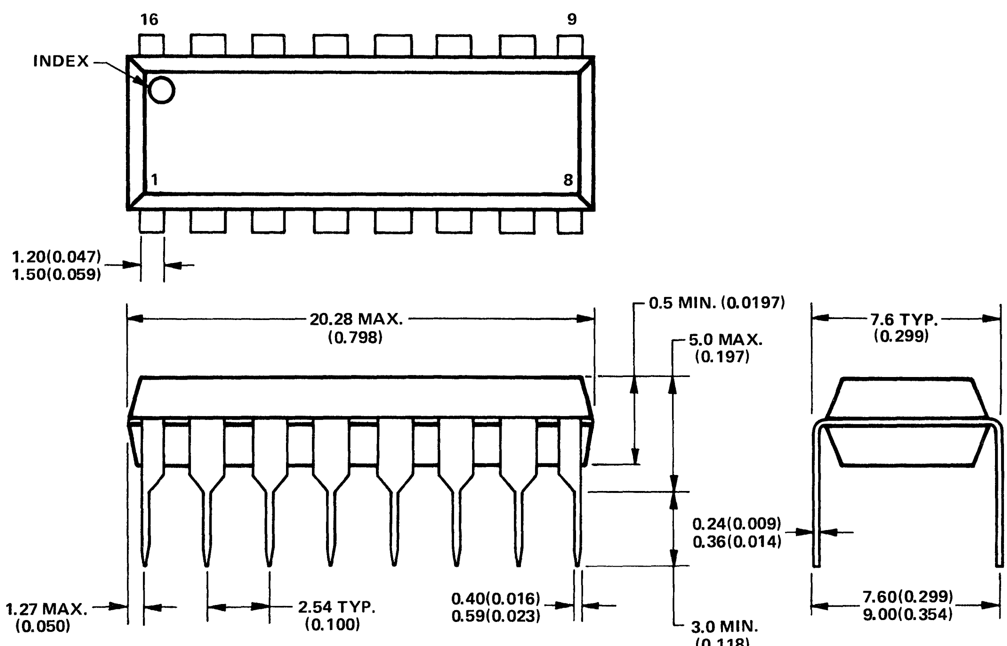


FIG. 22 t_{PZH}/t_{PHZ} (DRIVER)



PACKAGE DIMENSIONS



Dimensions in millimeters

4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER (INVERTING)

MB 426

FUJITSU

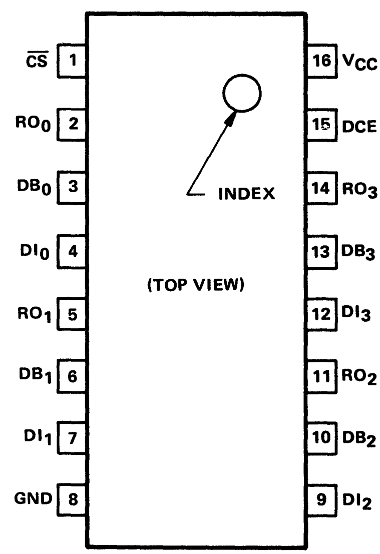
4 - BIT PARALLEL BI-DIRECTIONAL BUS DRIVER (INVERTING)

The Fujitsu MB 426 is a 4-bit inverting bi-directional bus driver/receiver. The function of driver or receiver is selected by Direction Control input. This device is designed for inverting data bus buffer/driver of the Fujitsu MBL 6800 micro-processor unit or similar devices.

- Schottky clamped TTL
- 3-state outputs
- "L" level output sink current:
  50 mA (Driver)
  16 mA (Receiver)
- "H" level output current:
  10 mA (Driver)
  1 mA (Receiver
- "H" level output voltage (I_{OH} = −1 mA): 3.65V min.
- Low input load current by using PNP transistor: 250 μA max.
- High-speed operation with high capacitance load
  Driver: t_{pd} = 14 ns typ., 25 ns max. at 300 pF
  Receiver: t_{pd} = 11 ns typ., 25 ns max. at 30 pF
- Especially high speed operation on 3-state
- Pin compatible with Intel 8226
- Standard 16-pin dual-in-line package

SYMBOL	PIN NAME
$\overline{CS}$	CHIP SELECT
DCE	DIRECTION CONTROL ENABLE
DI	DATA INPUT
DB	DATA BUS
RO	RECEIVER OUTPUT

PIN ASSIGNMENT



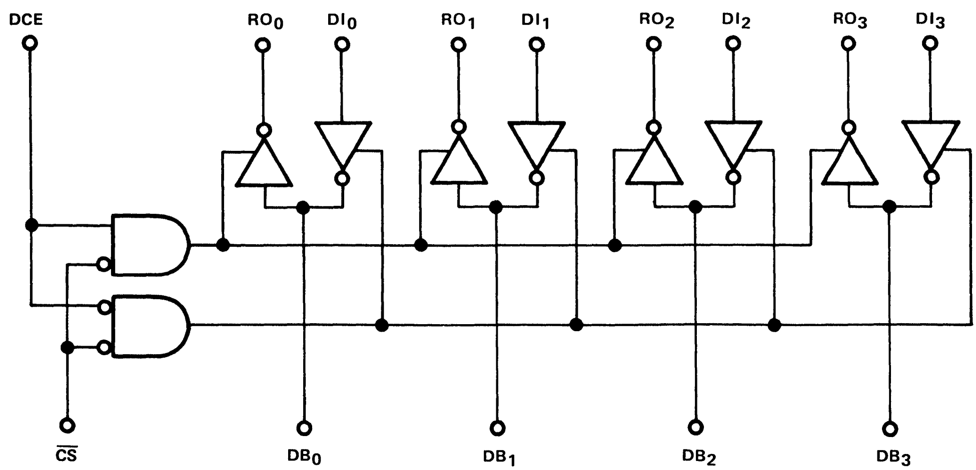
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to GND Pin	V_{CC}	− 0.5 to +7.0	V
Input Voltage	V_I	− 1.0 to +5.5	V
Output Voltage	V_O	− 0.5 to +7.0	V
Operating Temperature	T_{op}	−15.0 to +75.0	°C
Storage Temperature	T_{stg}	−40.0 to +125.0	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

FUNCTIONAL DESCRIPTION/APPLICATION INFORMATION

LOGIC DIAGRAM



FUNCTION TABLE

Mode Control		Driver State	Receiver State	Reference Figure
$\overline{CS}$	DCE			
0	0	DB = $\overline{DI}$	HZ	Fig. 1
0	1	HZ	RO = $\overline{DB}$	Fig. 2
1	0	HZ	HZ	Fig. 3
1	1	HZ	HZ	Fig. 4

HZ: high impedance state.

REFERENCE FIGURE

FIG. 1

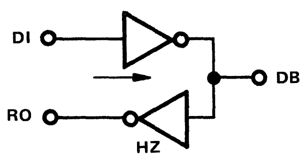


FIG. 2

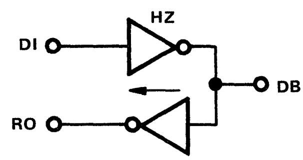


FIG. 3

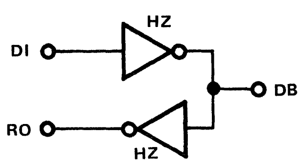
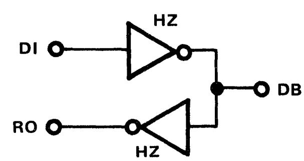


FIG. 4



APPLICATIONS

- Data Bus Buffer for the Fujitsu MBL 6800 micro-processor unit or similar devices
- Interface Buffer of memory and I/O device to a bi-directional bus of micro-computer system

GUARANTEED OPERATING RANGES

Item	Symbol	Range	Unit
Supply Voltage	V_{CC}	+4.75 to +5.25	V
Driver Output Current			
"H" state	I_{OHD}	10 Max.	mA
"L" state	I_{OLD}	50 Max.	mA
Receiver Output Current			
"H" state	I_{OHR}	1 Max.	mA
"L" state	I_{OLR}	16 Max.	mA
Ambient Temperature	T_A	0 to +75	°C

DC CHARACTERISTICS (see NOTE)

(T_A = 0°C to 75°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Circuit
Output High Voltage for RO (V_{CC} = 4.75V, I_{OH} = −1 mA, V_{IL} = 0.95V)	V_{OH1}	3.65	4.2	–	V	Fig. 1
Output High Voltage for DB (V_{CC} = 4.75V, I_{OH} = −10 mA, V_{IL} = 0.95V)	V_{OH2}	2.4	3.2	–	V	Fig.2
Ouput Low Voltage for RO/DB (V_{CC} = 4.75V, I_{OL} = 16 mA/25 mA, V_{IH} = 2.0V)	V_{OL1}	–	–	0.45	V	Fig. 3 Fig. 4
Output Low Voltage for DB (V_{CC} = 4.75V, I_{OL} = 50 mA, V_{IH} = 2.0V)	V_{OL2}	–	–	0.6	V	Fig. 3
Input High Current for $\overline{CS}$ and DCE (V_{CC} = 5.25V, V_{IH} = 5.5V)	I_{IH1}	–	–	20	μA	Fig. 5
Input High Current for DI (V_{CC} = 5.25V, V_{IH} = 5.5V)	I_{IH2}	–	–	10	μA	Fig. 6
Input Low Current for $\overline{CS}$ and DCE (V_{CC} = 5.25V, V_{IL} = 0.4V)	I_{IL1}	–	-80	-500	μA	Fig. 7
Input Low Current for DI and DB (V_{CC} = 5.25V, V_{IL} = 0.4V)	I_{IL2}	–	-40	-250	μA	Fig. 8 Fig. 9
Output Short Circuit Current for RO (V_{CC} = 5.25V)	I_{OS1}	-15	–	- 65	mA	Fig. 10
Output Short Circuit Current for DB (V_{CC} = 5.25V)	I_{OS2}	-30	–	-120	mA	Fig. 11
Output Leakage Current for RO (high impedance state, V_{CC} = 5.25V, V_O = 0.45V/5.25V)	I_{OZ1}	–	–	± 20	μA	Fig. 12
Output Leakage Current for DB (high impedance state, V_{CC} = 5.25V, V_O = 0.45V/5.25V)	I_{OZ2}	–	–	±100	μA	Fig. 12
Power Supply Current (All Inputs are High, V_{CC} = 5.25V)	I_{CCH}	–	42	80	mA	Fig. 13
Power Supply Current (All Inputs are Low, V_{CC} = 5.25V)	I_{CCL}	–	65	120	mA	Fig. 14
Input Clamp Voltage for All Inputs (V_{CC} = 4.75V, I_{IL} = -5 mA)	V_{IC}	–	–	- 1.0	V	Fig. 15 Fig. 16

Note: All typical values are at V_{CC} = 5.0V and T_A = 25°C.

AC CHARACTERISTICS (see NOTE)

(V_{CC} = 5.0V, T_A = 25°C ± 2°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Circuit
Propagation Delay Time DB to RO (R_1 = 300 ohm, R_2 = 600 ohm, C_L = 30 pF)	t_{PLH} t_{PHL}	– –	11 12	25 25	ns ns	Fig. 17
Propagation Delay Time DI to DB (R_1 = 90 ohm, R_2 = 180 ohm, C_L = 300 pF)	t_{PLH} t_{PHL}	– –	12 16	25 25	ns ns	Fig. 18
Receiver Enable Time (R_1 = 300 ohm, R_2 = 600 0hm, C_L = 30 pF)	t_{PZL}	–	26	45	ns	Fig. 19
Receiver Disable Time (R_1 = 300 ohm, R_2 = 600 ohm, C_L = 5 pF)	t_{PLZ}	–	12	25	ns	
Receiver Enable Time (R_1 = 10K ohm, R_2 = 1K ohm, C_L = 30 pF)	t_{PZH}	–	15	35	ns	Fig. 20
Receiver Disable Time (R_1 = 10K ohm, R_2 = 1K ohm, C_L = 5 pF)	t_{PHZ}	–	10	25	ns	
Driver Enable Time (R_1 = 90 ohm, R_2 = 180 ohm, C_L = 300 pF)	t_{PZL}	–	25	45	ns	Fig. 21
Driver Disable Time (R_1 = 90 ohm, R_2 = 180 ohm, C_L = 5 pF)	t_{PLZ}	–	7	20	ns	
Driver Enable Time (R_1 = 10K ohm, R_2 = 1K ohm, C_L = 300 pF)	t_{PZH}	–	19	45	ns	Fig. 22
Driver Disable Time (R_1 = 10K ohm, R_2 = 1K ohm, C_L = 5 pF)	t_{PHZ}	–	7	20	ns	

Note: C_L includes jig and probe capacitance.

DC/AC TEST CIRCUIT

FIG. 1 V_{OH1}

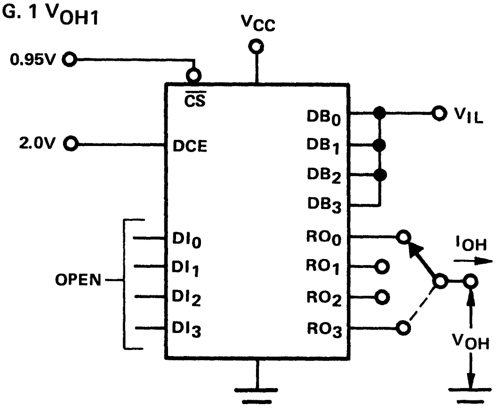


FIG. 2 V_{OH2}

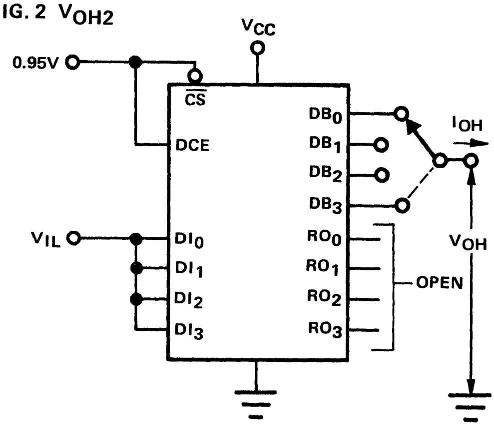


FIG. 3 V_{OL1}/V_{OL2}

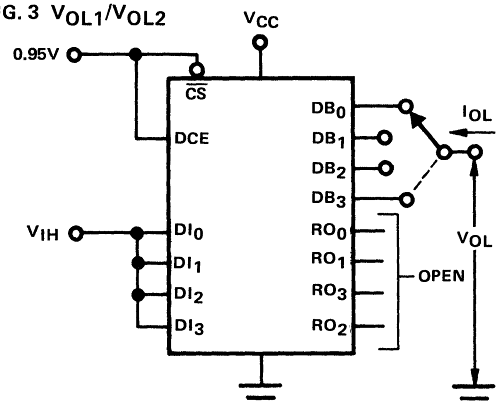


FIG. 4 V_{OL1}

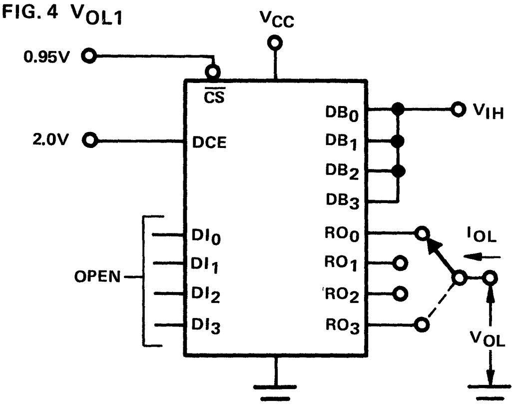


FIG. 5 I_{IH1}

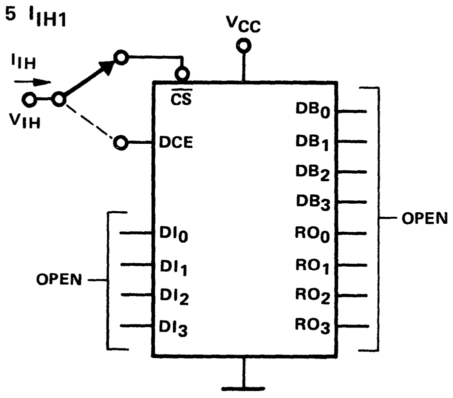
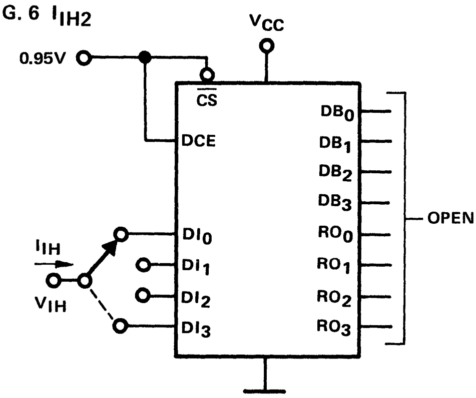


FIG. 6 I_{IH2}



Interface Devices

Fig. 7—I_{IL1}

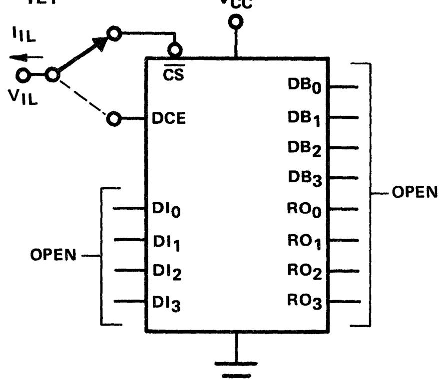


Fig. 8.—I_{IL2}

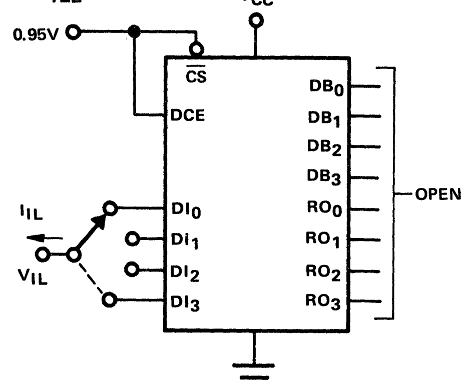


Fig. 9—I_{IL2}

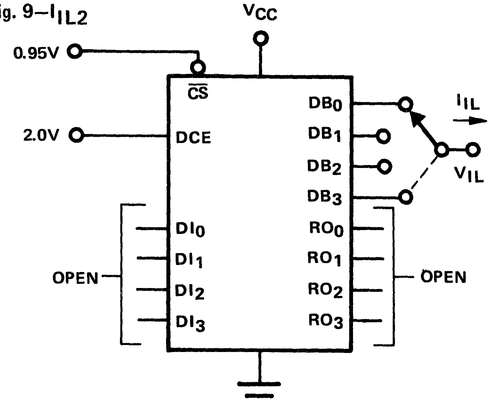


FIG. 10—I_{OS1}

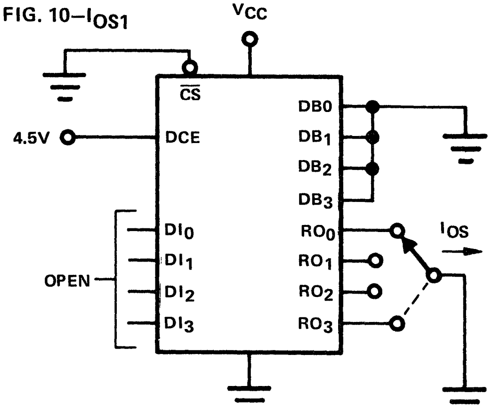


Fig. 11—I_{OS2}

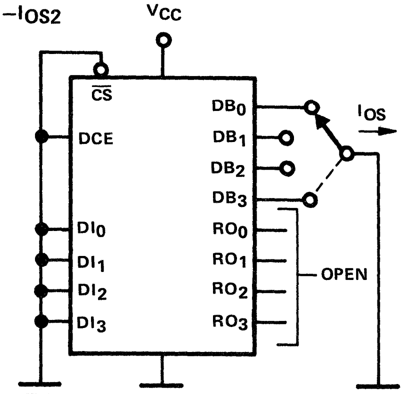


Fig. 12—I_{OZ}

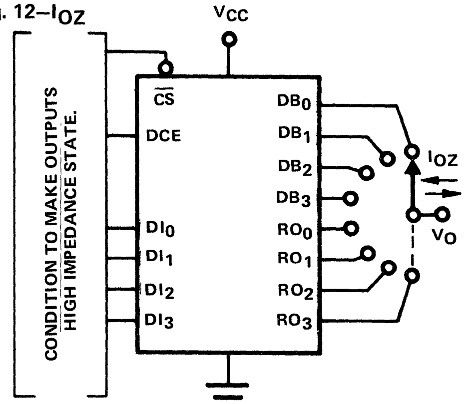


Fig. 13.—I_{CCH}

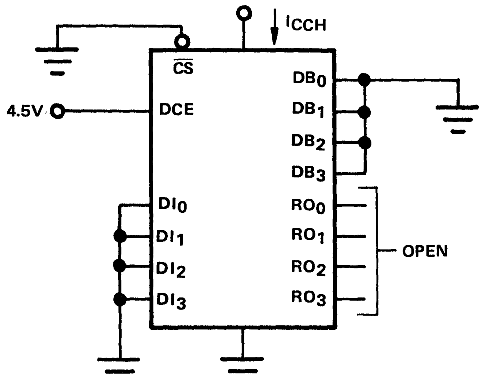


Fig. 14—I_{CCL}

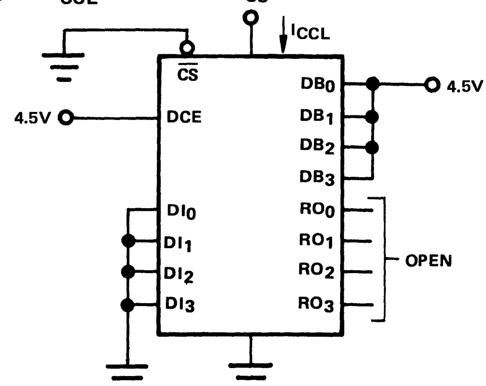


Fig. 15—V_{IC}

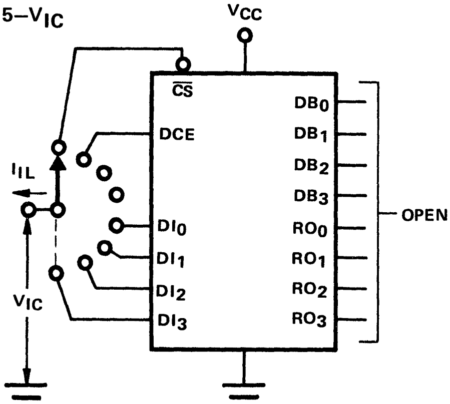


Fig. 16—V_{IC}

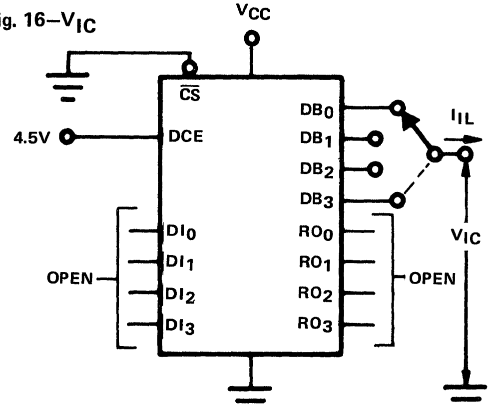


Fig. 17—t_{PLH}/t_{PHL} (DB TO RO)

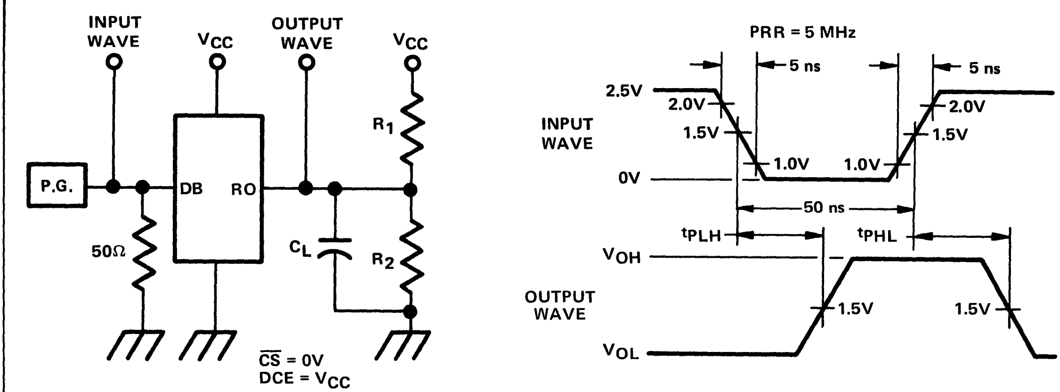


Fig. 18—t_{PLH}/t_{PHL} (DI TO DB)

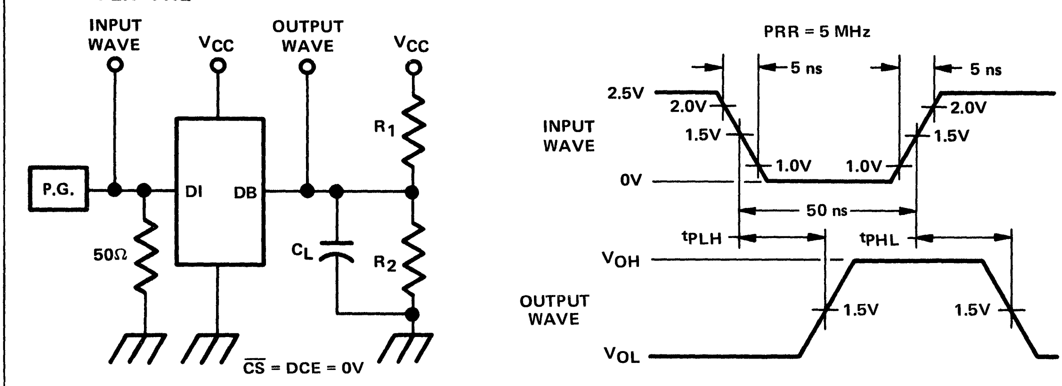


Fig. 19—t_{PZL}/t_{PLZ} (RECEIVER)

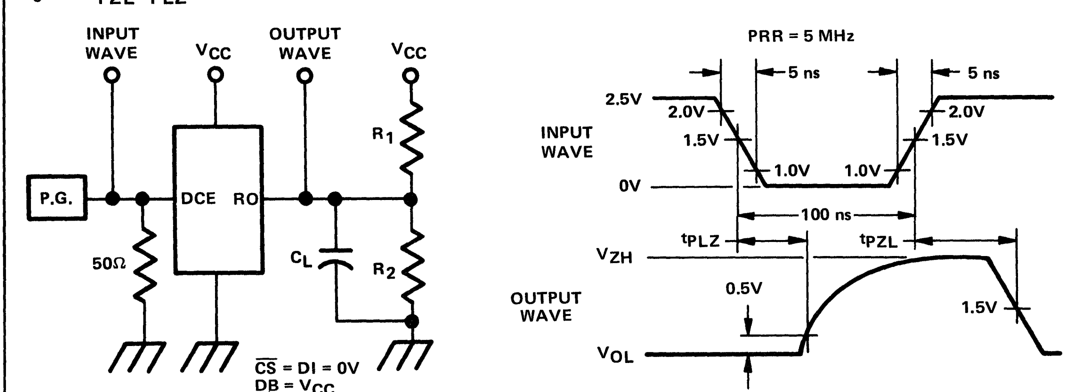


Fig. 20—t_{PZH}/t_{PHZ} (RECEIVER)

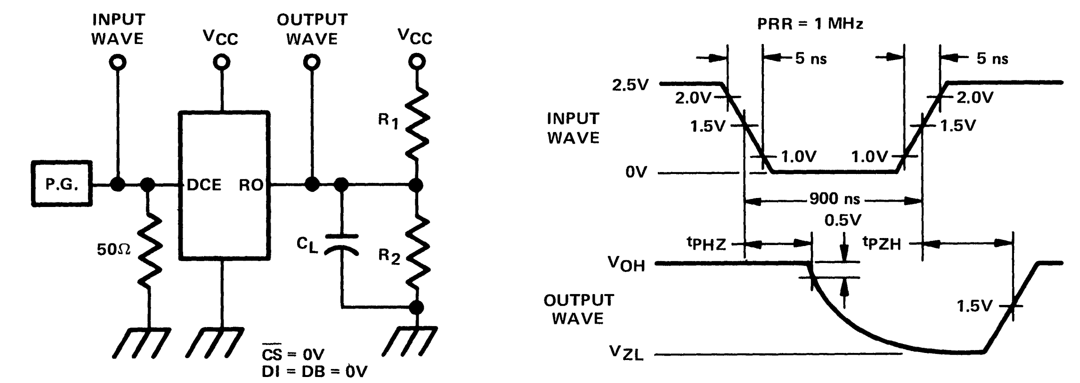


Fig. 21—t_{PZL}/t_{PLZ} (DRIVER)

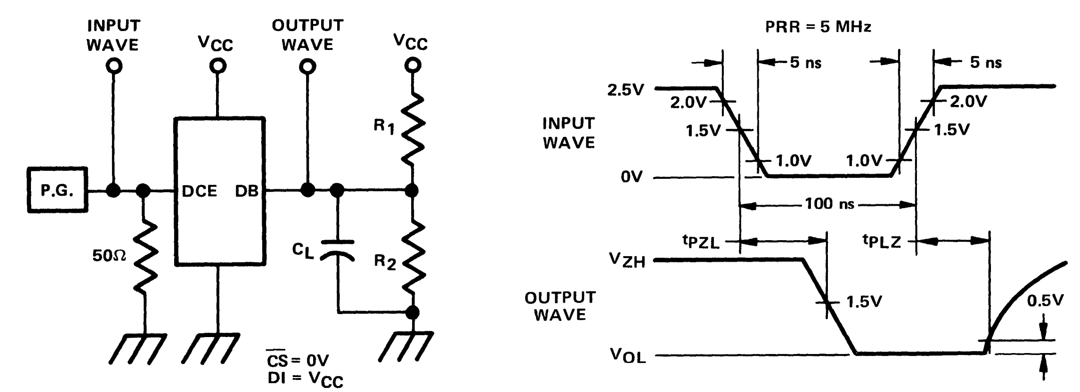
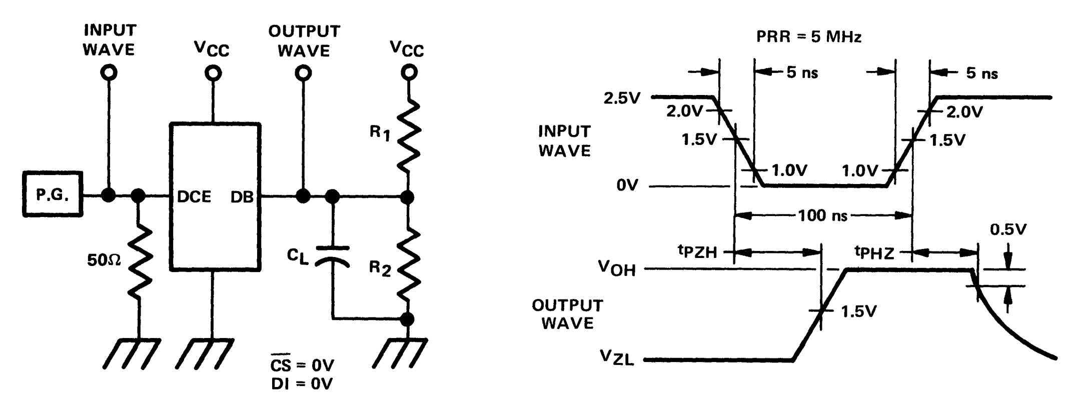
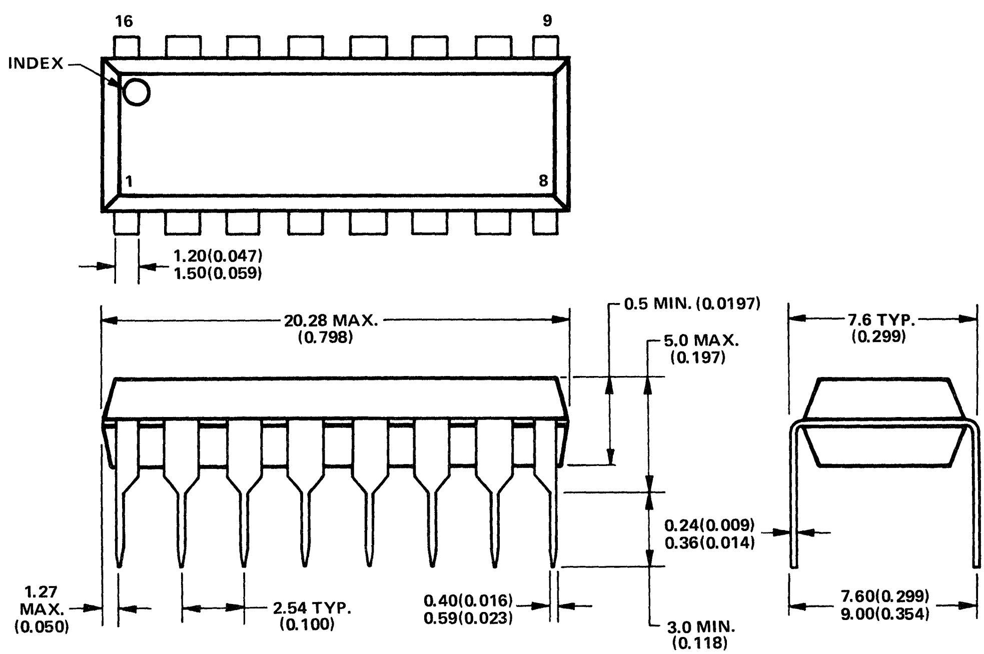


Fig. 22—t_{PZH}/t_{PHZ} (DRIVER)



Interface Devices

PACKAGE DIMENSIONS



Dimensions in millimeters

8-BIT TTL INPUT/OUTPUT PORT

MB 471

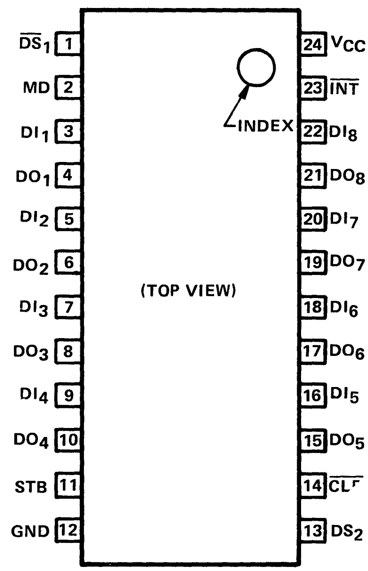
FUJITSU

8-BIT TTL INPUT/OUTPUT PORT

The Fujitsu MB 471 is an 8-bit input/output port which consists of 8-bit latch, 3-state output buffers, device selection/control logic and service request flip-flop for micro-processor. Through these built-in circuits, the MB 471 can be used for various functions such as latches, gated buffers or multiplexers and especially for main peripheral and input/output functions of microcomputer system using the Fujitsu MBL6800 micro-processor unit or similar devices.

- Schottky clamped TTL
- 3-state outputs
- "L" level output sink current: 15 mA
- "H" level output current: 1 mA
- "H" level output voltage: 3.65V min.
- Low input load current by using PNP transistor: 250 μA max.
- Parallel 8-bit register and buffer
- Asynchronous clear
- High speed operation: t_{pd} = 18 ns typ.
- Schottky input-clamping diode
- Pin compatible with Intel 8212
- Standard 24-pin dual-in-line package

PIN CONFIGURATION



SYMBOL	PIN NAME
$DI_1 \sim DI_8$	DATA INPUT
$DO_1 \sim DO_8$	DATA OUTPUT
$\overline{DS}_1$, DS_2	DEVICE SELECT INPUT
MD	MODE INPUT
STB	STROBE INPUT
$\overline{INT}$	INTERRUPT OUTPUT
$\overline{CLR}$	CLEAR INPUT

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to GND Pin	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_I	-1.0 to +5.5	V
Output Voltage	V_O	-0.5 to +7.0	V
Operating Temperature	T_{op}	-15 to + 75	°C
Storage Temperature	T_{stg}	-40 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Interface Devices

FUNCTIONAL DESCRIPTION/APPLICATION INFORMATION

FUNCTION TABLE

(1) Data Output (DO)

MD	$DS_1 \cdot DS_2$	STB	DI	$\overline{CLR}$	WR	EN	DO	REMARKS	
L	H	L ↑ H ↓ L	L	H	L ↑ H ↓ L	H	L	DATA LATCH	INPUT MODE
			H				H		
		H	L	X	H		L	DATA INPUT	
			H				H		
		L	X	H	L		Q_0	HOLD	
				L			L	RESET	
	L	X	X	X	X	L	HZ	HIGH IMPEDANCE	
H	H	X	L	X	H	H	L	DATA INPUT	OUTPUT MODE
			H				H		
	L	X	X	H	L		Q_0	HOLD	
				L			L	RESET	

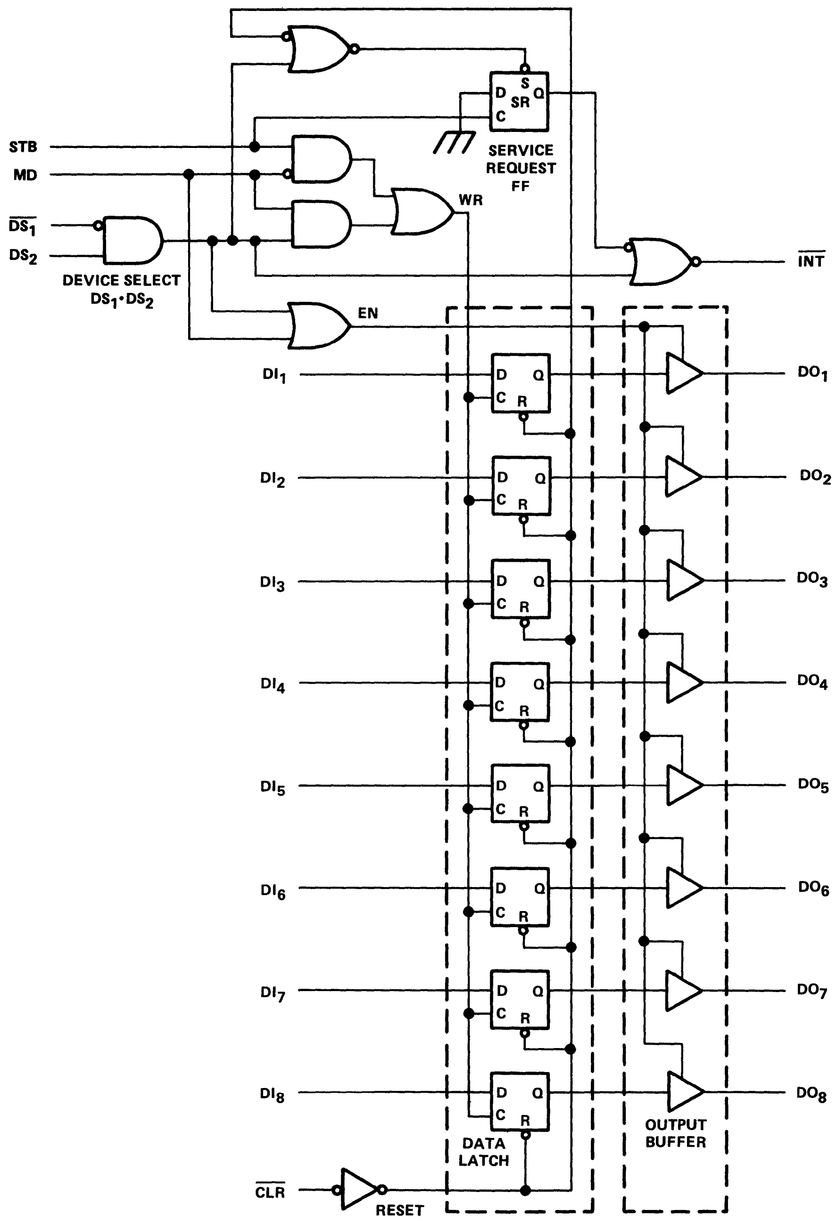
(2) Interrupt Output (INT)

MD	$DS_1 \cdot DS_2$	$\overline{CLR}$	STB	DI	S (SR)	C (SR)	Q (SR)	$\overline{INT}$	REMARKS
X	H	X	X	X	L	X	H	L	INTERRUPT
	L	L	X		L	X	H	H	RESET
		H	H ↓ L		H	H ↓ L	L	L	INTERRUPT
	H ↓ L	H	L		L ↑ H	L	H	H	RESET

Note:

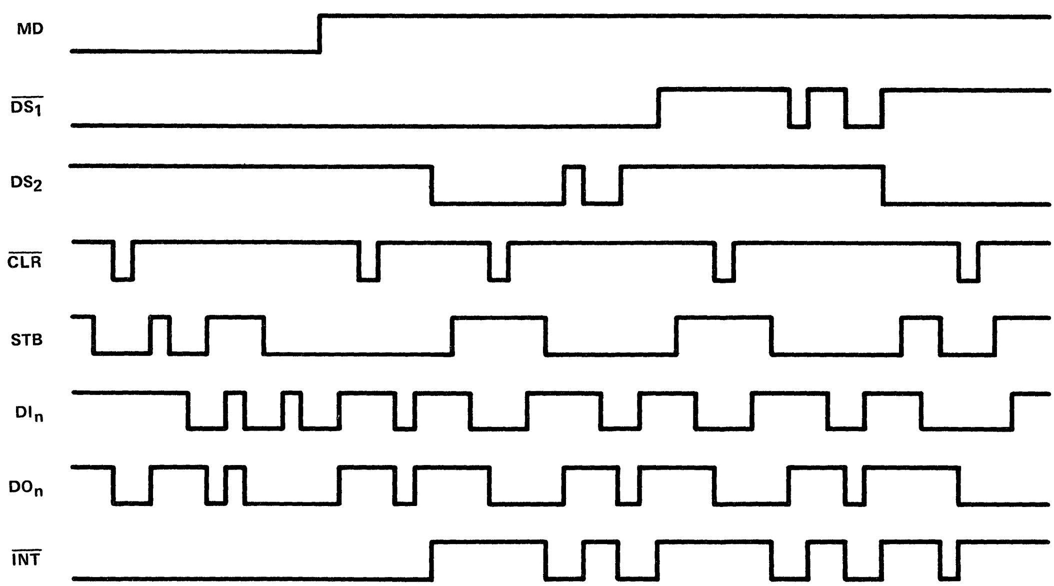
x: Irrevelant
Q_0: The state before Data Latch output (Q)
HZ: High impedance state
$DS_1 \cdot DS_2$ = H: When $\overline{DS_1}$ = L and DS_2 = H
$DS_1 \cdot DS_2$ = L: When $\overline{DS_1}$ = H or DS_2 = L

LOGIC DIAGRAM



Interface Devices

FUNCTIONAL TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

(1) Data Latch

The data latch consists of eight flip-flops as shown in the Logic Diagram. All of the flip-flops are D-type. The output Q of the flip-flop follows the data input D of the flip-flop while the clock input C of the flip-flop is "H" level. When the clock input C returns "L" level, the data is latched in the flip-flop. The data latch is cleared simultaneously upon the eight flip-flops through the reset input R of each flip-flop by an asynchronous reset input $\overline{CLR}$. The clock input C is not disturbed by the reset input $\overline{CLR}$.

(2) Output Buffer

Each of the data latch outputs Q is connected to an output buffer as shown in the Logic Diagram. All of the output buffers are 3-state and non-inverting type and have a common enable line EN. This common enable line EN either enables all of the buffers to transmit the data from the data latch outputs Q or disable all of the buffers to set its output state into a high-impedance. This high impedance state allows the MB 471 to be connected directly onto a bi-directional data bus of the Fujitsu MBL6800 microprocessor or similar devices.

(3) Control Logic

The MB 471 has the control inputs $\overline{DS_1}$, DS_2, MD and STB as shown in the Logic Diagram. These inputs control the functions of device selection, data latching, output buffer state selection and service request flip-flop as follows:

(a) $\overline{DS_1}$, DS_2 (Device Selection)

The device selection inputs $\overline{DS_1}$ and DS_2 are used for device selection and setting the service request flip-flop. When the input $\overline{DS_1}$ is "L" level and the input DS_2 is "H" level, the output of the device selection logic is "H" level and this device is selected. Then, the output buffers are enabled and simultaneously the service request flip-flop SR is asynchronously set.

(b) MD (Mode)

The mode selection input MD is used for controlling the output buffer state together with the output of the device selection logic $DS_1 \cdot DS_2$ and selecting the source of clock signal to the clock inputs C of the data latch. When the input MD is "H" level, i.e., output mode, the output buffers are enabled and the source of clock signal to the data latch is from the device selection logic $DS_1 \cdot DS_2$. When the input MD is "L" level, i.e., input mode, the output buffer state is determined by the device selection logic $DS_1 \cdot DS_2$ and the source of clock signal to the data latch is from the strobe input STB.

(c) STB (Strobe)

The strobe input STB is used to transmit a clock signal to the clock input C_s of the data latch and the service request flip-flop SR. When the input MD is "L" level, the data latch enables to receive a clock signal from the input STB. The clock input of the service request flip-flop SR receives unconditionally a clock signal from the input STB and the service request flip-flop SR is synchronously reset by the signal.

(d) SR (Service Request Flip-Flop)

The service request flip-flop SR is used to generate and control interrupt signal for a microcomputer system. When the input $\overline{CLR}$ is "L" level, the SR is set in the non-interrupt state. The output Q of SR is connected to an inverting input of a "NOR" gate and the other input of the "NOR" gate is non-inverting and connected to the output of the device selection logic $DS_1 \cdot DS_2$. When the interrupt output $\overline{INT}$ of the "NOR" gate is "LOW" level, it is in the interrupt state so as to connect to active low input priority generating circuits.

APPLICATIONS

- Gated Buffer
- Bi-directional Bus Driver
- Interrupting Input Port
- Interrupting Instruction Port
- Output Port
- Peripheral Circuit for the Fujitsu MBL6800 microprocessor unit or similar devices.

GUARANTEED OPERATING RANGE

Item	Symbol	Range	Unit
Supply Voltage	V_{CC}	+4.75 to +5.25	V
Output High Current	I_{OH}	1.0 Max.	mA
Output Low Current	I_{OL}	15 Max.	mA
Pulse Width	t_W	25 Min.	ns
Data Set-Up Time	t_S	15 Min.	ns
Data Hold Time	t_H	20 Min.	ns
Ambient Temperature	T_A	0 to +75	°C

DC CHARACTERISTICS (see NOTE)

T_A = 0°C to +75°C (unless otherwise noted)

Parameter	Symbol	Value			Unit	Test Circuit
		Min.	Typ.	Max.		
Output High Voltage (V_{CC} = 4.75V, I_{OH} = −1 mA, V_{IL} = 0.85V, V_{IH} = 2.0V)	V_{OH}	3.65	4.2	–	V	Fig. 1
Output Low Voltage (V_{CC} = 4.75V, I_{OL} = 15 mA, V_{IL} = 0.85V, V_{IH} = 2.0V)	V_{OL}	–	–	0.45	V	Fig. 2
Input High Current for DI, DS_2, STB, $\overline{CLR}$ (V_{CC} = 5.25V, V_{IH} = 5.5V)	I_{IH}	–	–	10	µA	Fig. 3
Input High Current for MD (V_{CC} = 5.25V, V_{IH} = 5.5V)	I_{IH}	–	–	30	µA	Fig. 3
Input High Current for $\overline{DS_1}$ (V_{CC} = 5.25V, V_{IH} = 5.5V)	I_{IH}	–	–	40	µA	Fig. 3
Input Low Current for DI, DS_2, STB, $\overline{CLR}$ (V_{CC} = 5.25V, V_{IL} = 0.4V)	I_{IL}	–	–	-0.25	mA	Fig. 4
Input Low Current for MD (V_{CC} = 5.25V, V_{IL} = 0.4V)	I_{IL}	–	–	-0.75	mA	Fig. 4
Input Low Current for $\overline{DS_1}$ (V_{CC} = 5.25V, V_{IL} = 0.4V)	I_{IL}	–	–	-1.0	mA	Fig. 4
Output Short Circuit Current (V_{CC} = 5.25V)	I_{OS}	-15	–	-75	mA	Fig. 5 Fig. 6
Output Leakage Current (High Impedance State, V_{CC} = 5.25V, V_O = 0.45V/5.5V)	I_{OZ}	–	–	±100	µA	Fig. 7
Power Supply Current (All Outputs are High, V_{CC} = 5.25V)	I_{CCH}	–	48	80	mA	Fig. 8
Power Supply Current (All Outputs are Low, V_{CC} = 5.25V)	I_{CCL}	–	90	130	mA	Fig. 8
Input Clamp Voltage (V_{CC} = 4.75V, I_{IL} = -5 mA)	V_{IC}	–	–	-1.0	V	Fig. 9

Note: All typical values are at V_{CC} = 5.0V and T_A = 25°C.

AC CHARACTERISTICS (see NOTE)

$T_A = 25^\circ C \pm 2^\circ C$, $V_{CC} = 5.0V$, $R_{L1} = 300$ Ohm, $R_{L2} = 600$ Ohm, $C_L = 30$ pF (unless otherwise noted)

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Unit	Test Circuit
Propagation Delay Time DI to DO	t_{PLH}	–	20	30	ns	Fig. 10
	t_{PHL}	–	16	25	ns	
Propagation Delay Time STB to DO	t_{PLH}	–	25	40	ns	Fig. 11
	t_{PHL}	–	22	40	ns	
Propagation Delay Time $\overline{DS_1}/DS_2$ to DO	t_{PLH}	–	22	40	ns	Fig. 12
	t_{PHL}	–	24	40	ns	
Propagation Delay Time $\overline{CLR}$ to DO	t_{PHL}	–	28	45	ns	Fig. 13
Propagation Delay Time $\overline{DS_1}/DS_2$ to $\overline{INT}$	t_{PLH}	–	18	30	ns	Fig. 14
	t_{PHL}	–	20	30	ns	
Propagation Delay Time $\overline{CLR}$/STB to INT	t_{PLH}	–	32	45	ns	Fig. 15
	t_{PHL}	–	22	40	ns	
Output Enable Time $\overline{DS_1}/DS_2$ to DO ($R_{L1} = 10K$ Ohm, $R_{L2} = 1K$ Ohm, $C_L = 5$ pF)	t_{PZH}	–	25	40	ns	Fig. 16
Output Disable Time $\overline{DS_1}/DS_2$ to DO ($R_{L1} = 10K$ Ohm, $R_{L2} = 1K$ Ohm, $C_L = 5$ pF)	t_{PHZ}	–	14	30	ns	Fig. 16
Output Enable Time $\overline{DS_1}/DS_2$ to DO	t_{PZL}	–	26	40	ns	Fig. 16
Output Disable Time $\overline{DS_1}/DS_2$ to DO	t_{PLZ}	–	20	30	ns	Fig. 16
Pulse Width	t_W	–	–	25	ns	Fig. 11, 12, 13, 14, 15
Data Set-Up Time	t_S	–	–	15	ns	Fig. 10
Data Hold Time	t_H	–	–	20	ns	Fig. 11, 12

Note: C_L includes jig and probe capacitance.

DC/AC TEST CIRCUIT

FIG. 1 V_{OH}

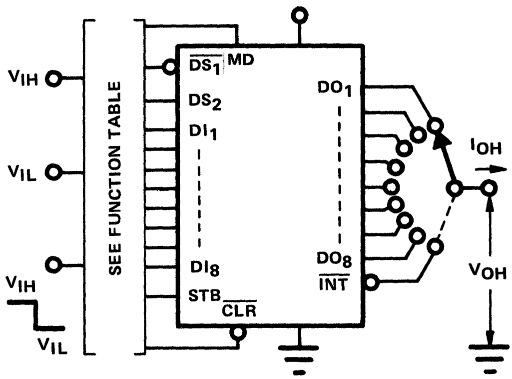


FIG. 2 V_{OL}

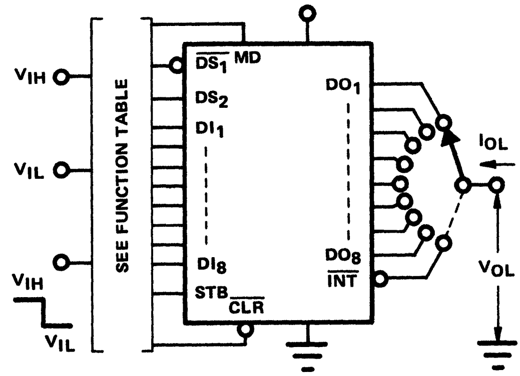
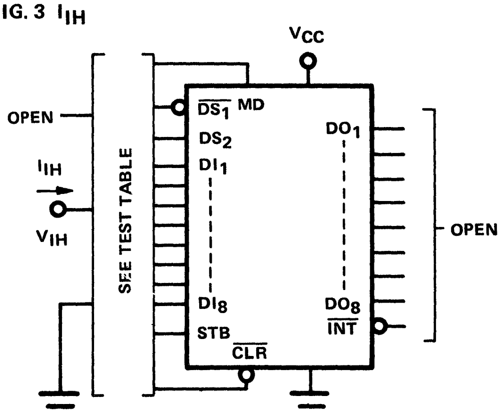


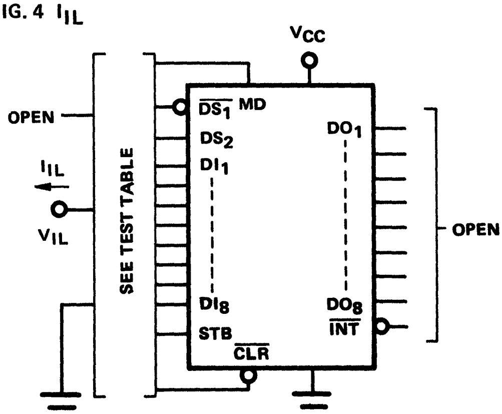
FIG. 3 I_{IH}



TEST TABLE

Input Under Testing	GND	Apply V_{CC}	Open
MD	$\overline{DS_1}$	DS_2	$DI_1 - DI_8$ STB, $\overline{CLR}$
$\overline{DS_1}$	MD	STB	$DI_1 - DI_8$ DS_2, $\overline{CLR}$
DS_2, $DI_1 - DI_8$, STB, $\overline{CLR}$	–	–	All Inputs Except Under Testing

FIG. 4 I_{IL}



TEST TABLE

Input Under Testing	GND	Apply V_{CC}	Open
MD	$\overline{DS_1}$	DS_2	$DI_1 - DI_8$ STB, $\overline{CLR}$
$\overline{DS_1}$	MD	STB	$DI_1 - DI_8$ DS_2, $\overline{CLR}$
DS_2, $DI_1 - DI_8$, STB, $\overline{CLR}$	–	–	All Inputs Except Under Testing

FIG. 5 I_{OS}

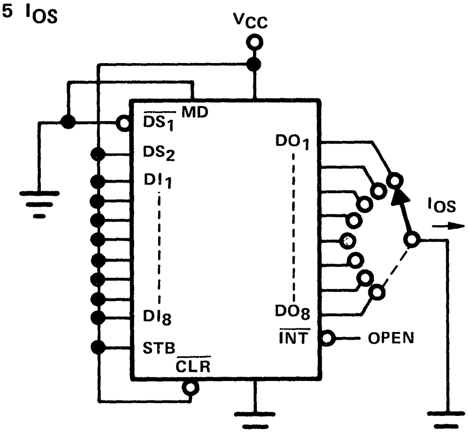


FIG. 6 I_{OS}

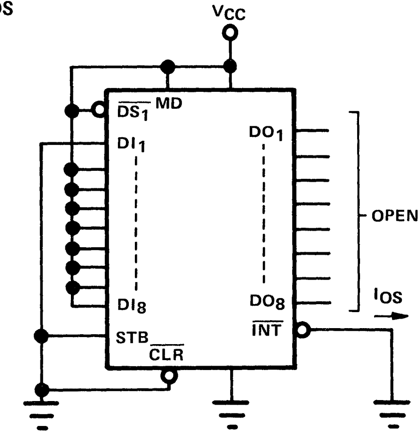


FIG. 7 I_{OZ}

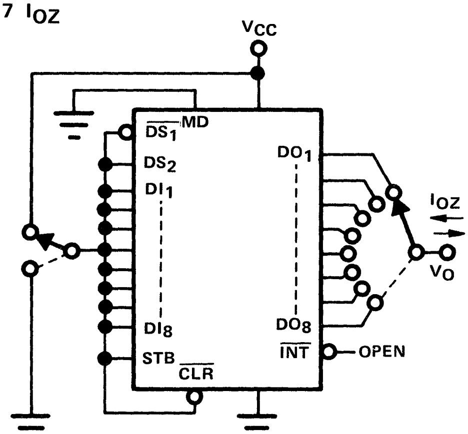


FIG. 8 I_{CC}

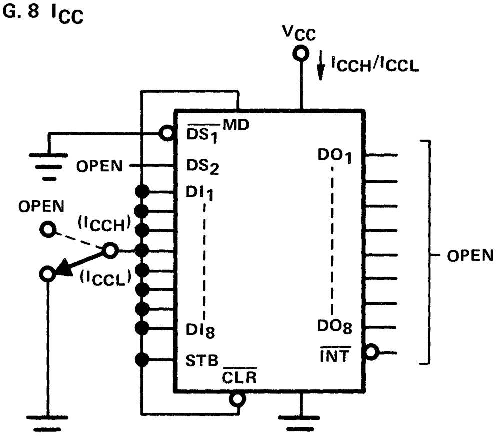


FIG. 9 V_{IC}

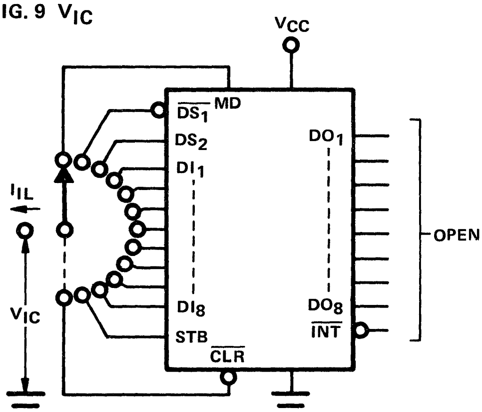
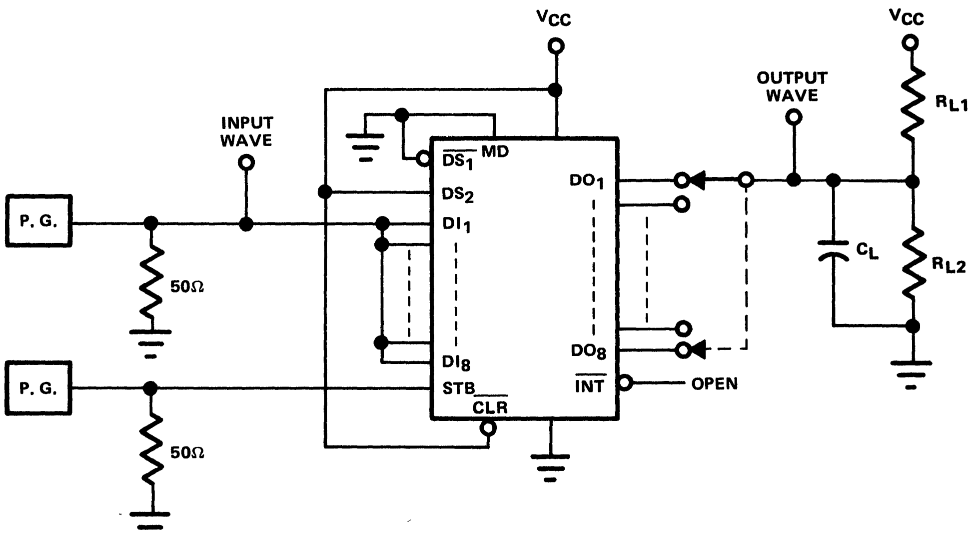


FIG. 10 t_{PLH}/t_{PHL} (DI TO DO)



INPUT PULSE CONDITION

V_{IL} = 0V, V_{IH} = 2.5V, $f(DI_n)$ = 1 MHz, $t_w(DI_n)$ = 500 ns, $t_{TLH} = t_{THL}$ = 5 ns, t_s > 15 ns

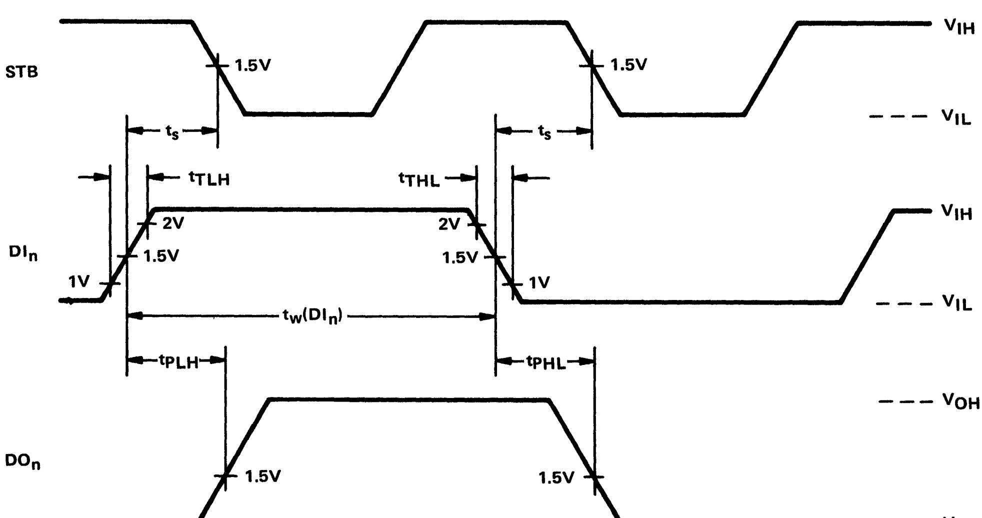
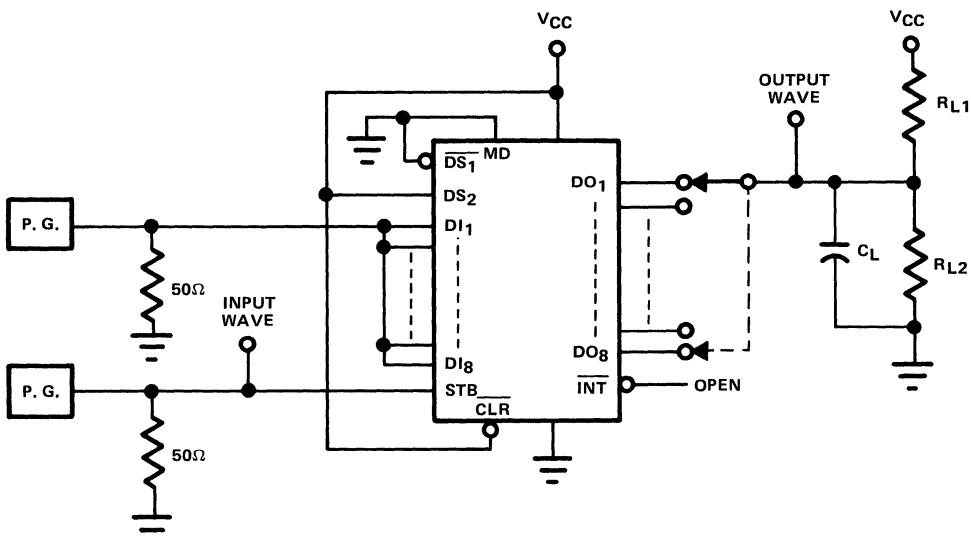


FIG. 11 t_{PLH}/t_{PHL} (STB TO DO)



INPUT PULSE CONDITION

V_{IL} = 0V, V_{IH} = 2.5V, f(STB) = 1 MHz, t_{TLH} = t_{THL} = 5 ns, t_w(STB) ≥ 25 ns, t_H ≥ 20 ns

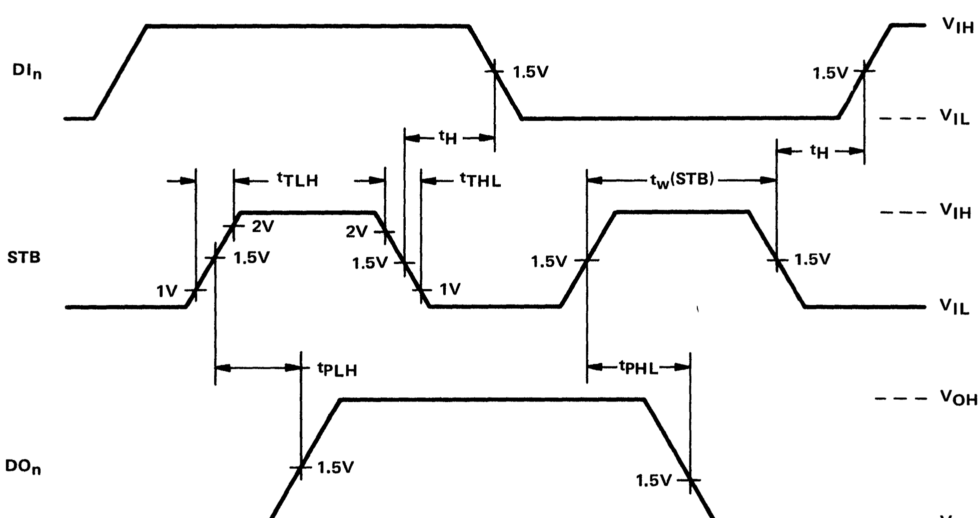
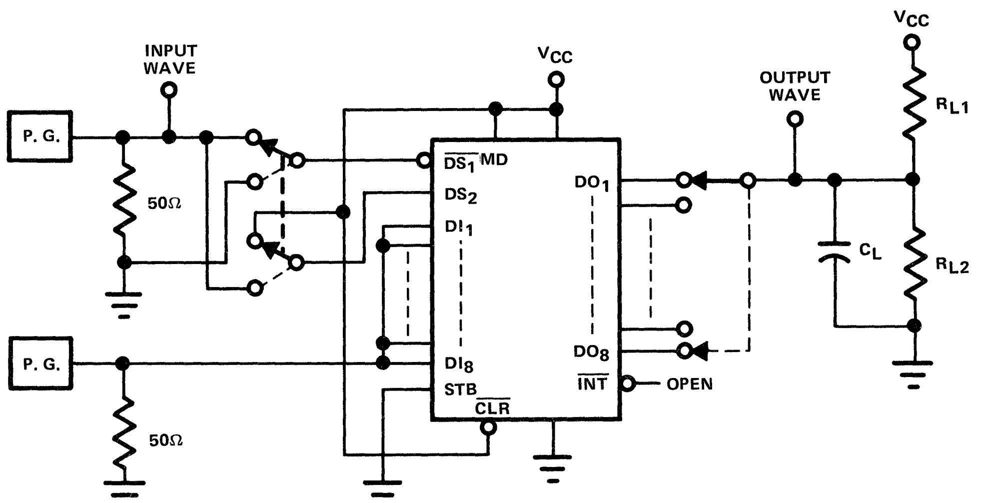


FIG. 12 t_{PLH}/t_{PHL} ($\overline{DS_1}/DS_2$ TO DO)



INPUT PULSE CONDITION

V_{IL} = 0V, V_{IH} = 2.5V, $f(\overline{DS_1}, DS_2)$ = 1 MHz, $t_{TLH} = t_{THL}$ = 5 ns, $t_w(\overline{DS_1}, DS_2) \geqslant 25$ ns, $t_H \geqslant 20$ ns

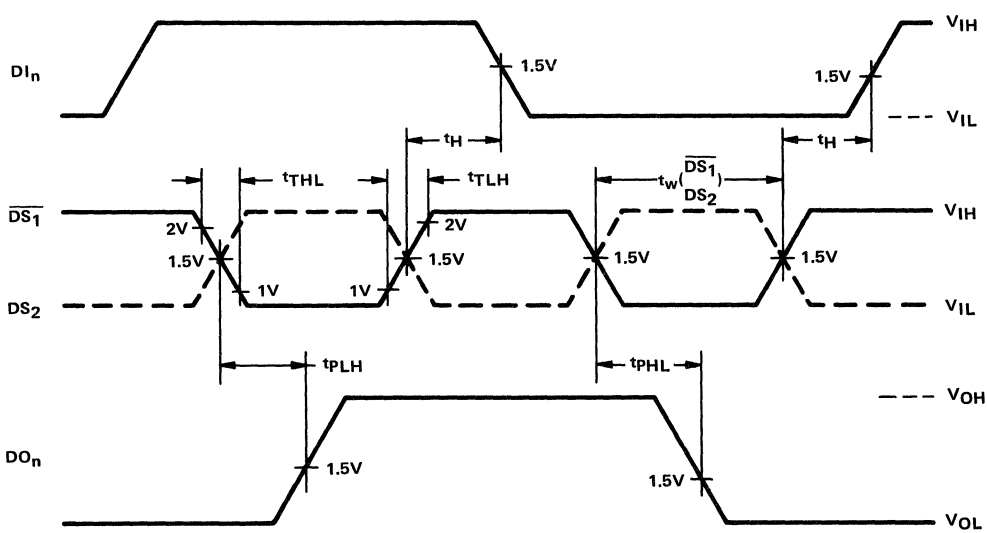
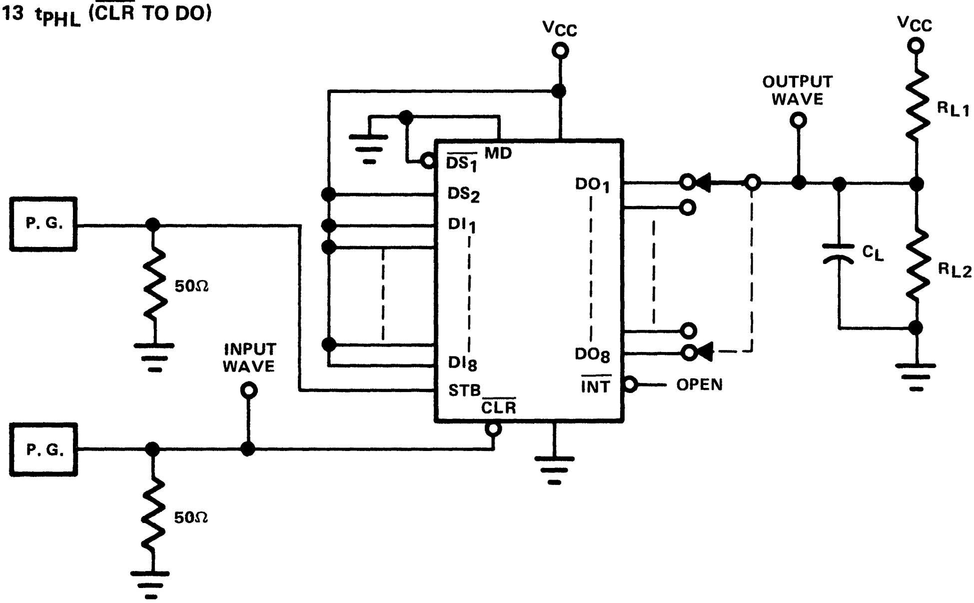
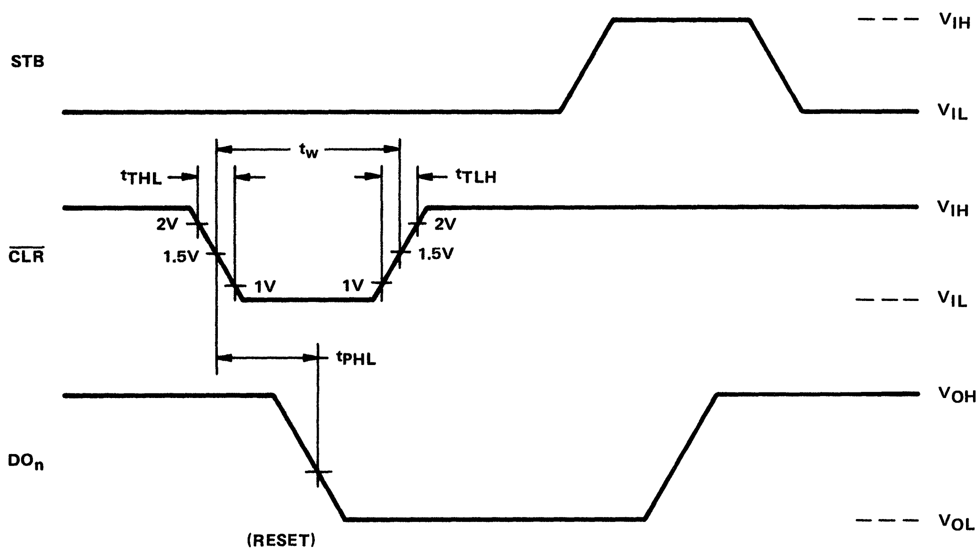


FIG. 13 t_{PHL} ($\overline{CLR}$ TO DO)



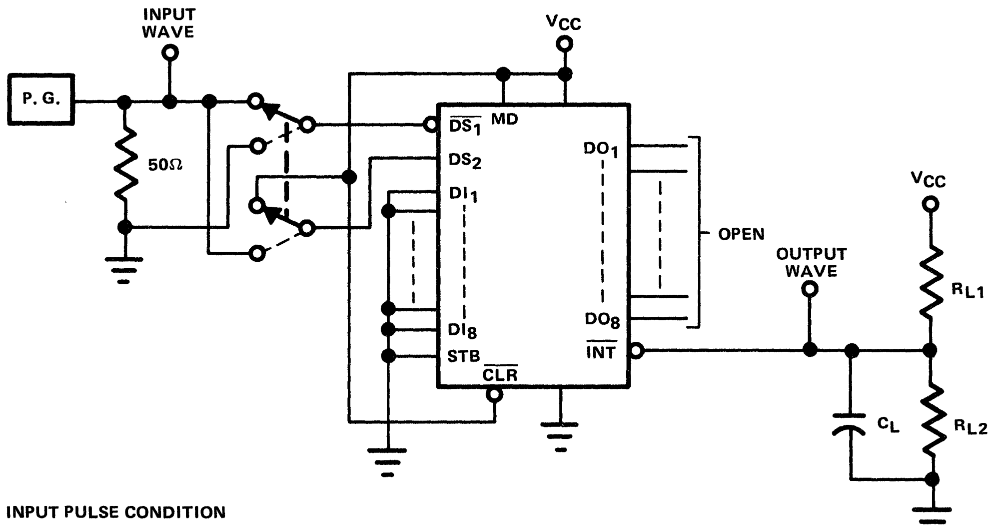
INPUT PULSE CONDITION

$V_{IL} = 0V$, $V_{IH} = 2.5V$, $f = 1$ MHz, $t_{TLH} = t_{THL} = 5$ ns, $t_w \geqslant 25$ ns



Interface Devices

FIG. 14 t_{PLH}/t_{PHL} ($\overline{DS}$ /DS_2 TO $\overline{INT}$)



INPUT PULSE CONDITION

V_{IL} = 0V, V_{IH} = 2.5V, f = 1 MHz, t_{TLH} = t_{THL} = 5 ns, $t_w \geq$ 25 ns

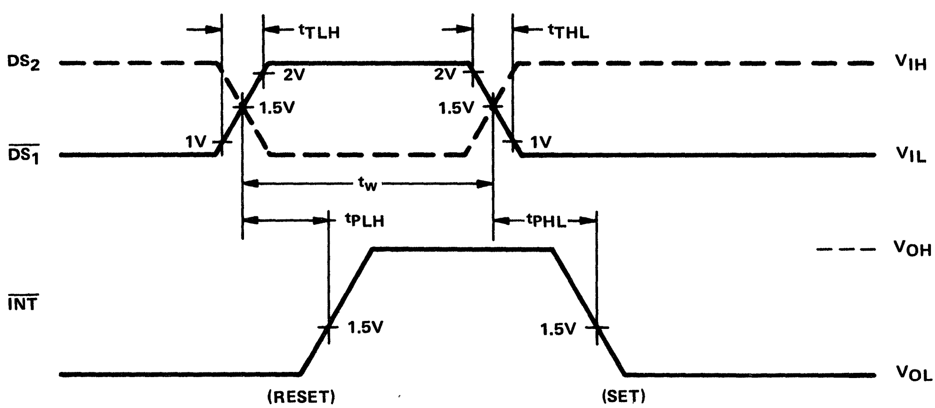
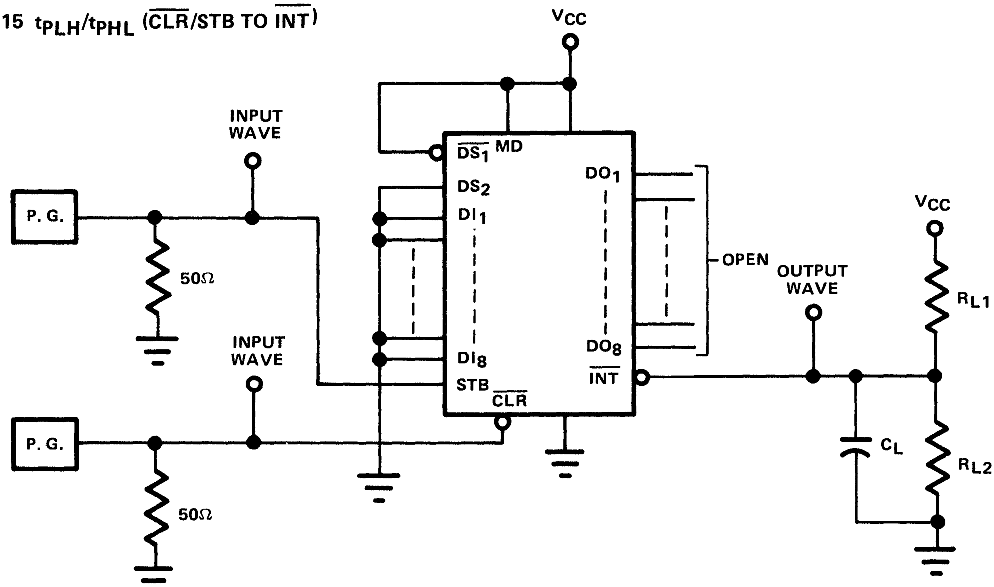


FIG. 15 t_{PLH}/t_{PHL} ($\overline{CLR}$/STB TO $\overline{INT}$)



INPUT PULSE CONDITION

V_{IL} = 0V, V_{IH} = 2.5V, f = 1 MHz, t_{TLH} = t_{THL} = 5 ns, $t_w \geqslant$ 25 ns

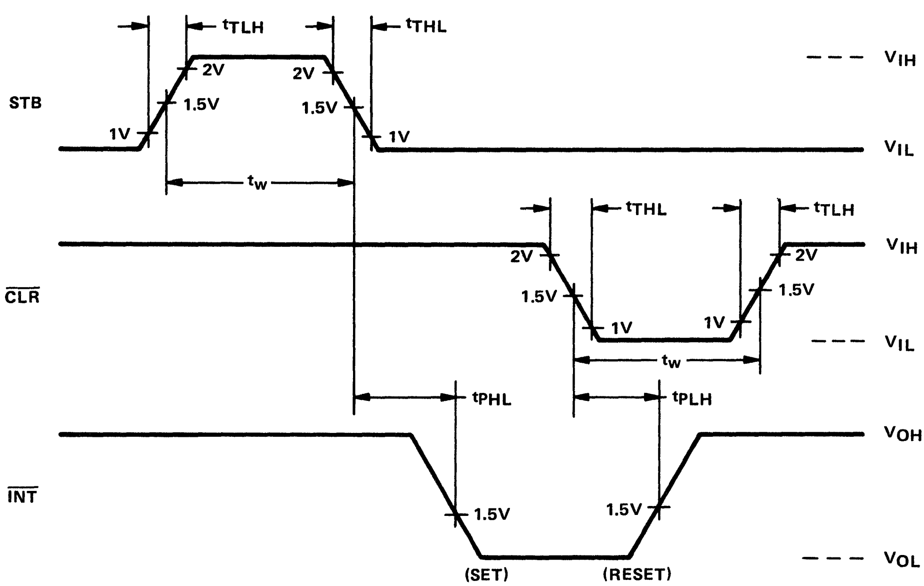
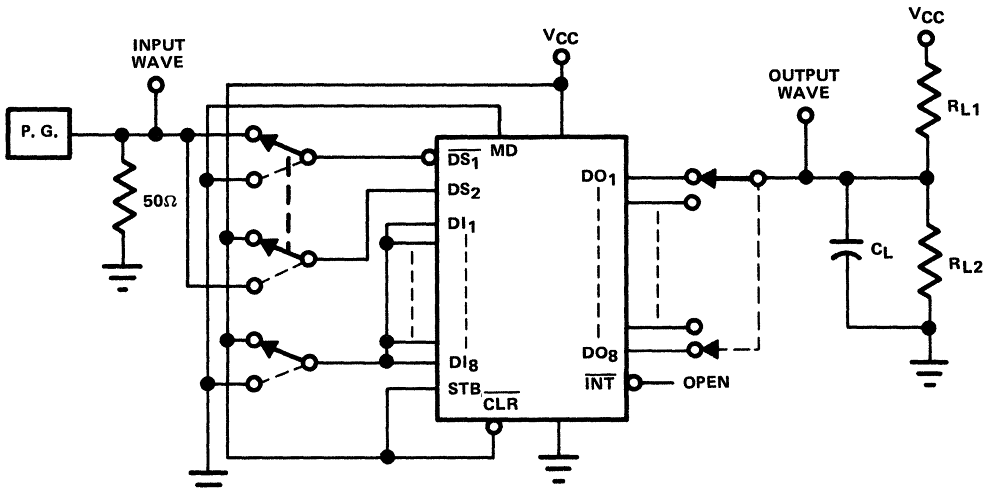
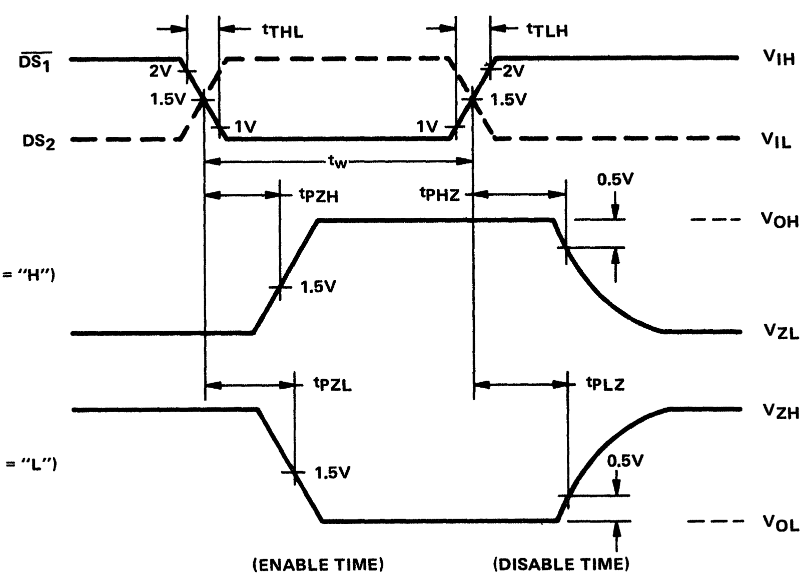


FIG. 16 $t_{PHZ}/t_{PZH}/t_{PLZ}/t_{PZL}$



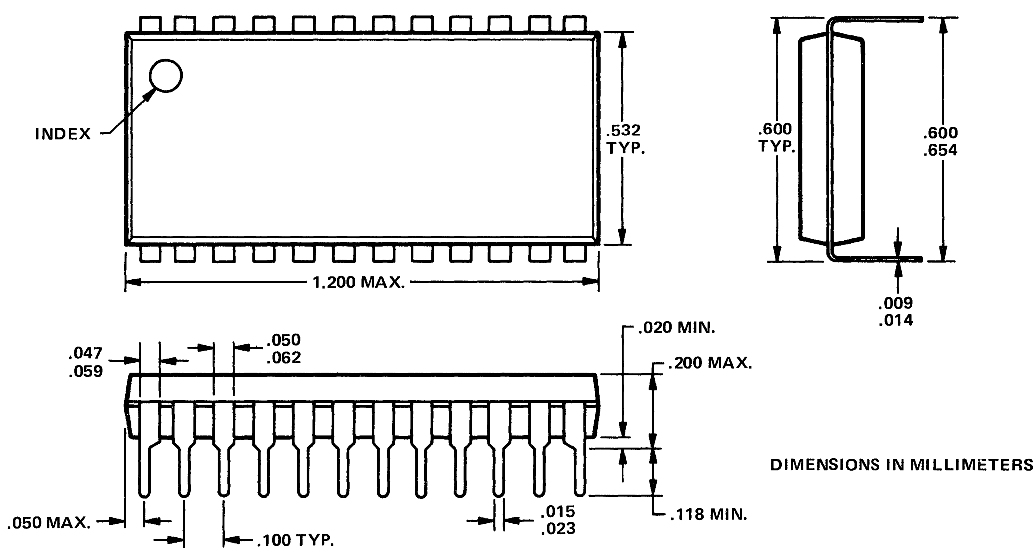
INPUT PULSE CONDITION

V_{IL} = 0V, V_{IH} = 2.5V, f = 1 MHz, $t_{TLH} = t_{THL}$ = 5 ns, t_w = 500 ns



PACKAGE DIMENSIONS

24-LEAD PLASTIC DUAL IN-LINE PACKAGE



HEX THREE-STATE BUFFER/INVERTER

MB 485
MB 486
MB 487
MB 488

FUJITSU

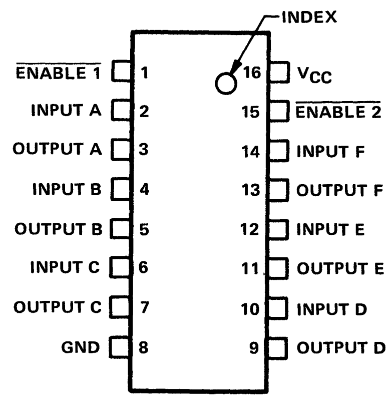
HEX THREE-STATE BUFFER/INVERTER

The Fujitsu MB 485/MB 486/MB 487/MB 488 are 3-state buffers/inverters each of which consists of six buffer gates and control logic. These devices are the most suitable for address buffer of the Fujitsu MBL6800 microprocessor unit or similar devices.

The MB 485/MB 486 include a 2-input enable logic which controls the six buffers, and MB 487/MB 488 include two enable logics, one of which controls the four buffers and the other controls two buffers. While the MB 485/MB 487 are non-inverting type, the MB 486/MB 488 are inverting type.

- Shottky clamped TTL
- 3- state outputs
- High speed operation: 8.0 ns typ.
- Single +5V power supply
- Connectable to the Fujitsu MB 74LS (Logic Series)/MBL 6800 MPU or similar devices
- Pin compatible with Motorola XC6885/XC6886/XC6887/XC6888 and Signetics 8T95/8T96/8T97/8T98, respectively
- Low input load current by using PNP transitor: 0.4 mA max.
- Standard 16-pin dual-in-line package

PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS (See Note)

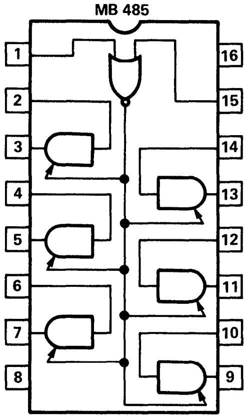
Rating	Symbol	Value	Unit
V_{CC} Pin Potential to GND Pin	V_{CC}	+7.0 Max.	V
Input Voltage	V_I	+5.5 Max.	V
Operating Temperature	T_{op}	−15 to + 75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

Note: Permenent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

FUNCTIONAL DESCRIPTION/APPLICATION INFORMATION

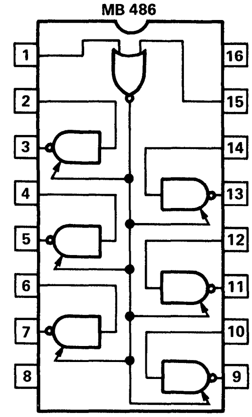
BLOCK DIAGRAM/FUNCTION TABLE

MB 485



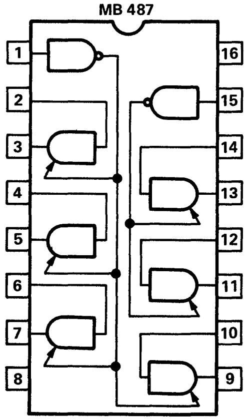
$\overline{\text{ENABLE 2}}$	$\overline{\text{ENABLE 1}}$	INPUT	OUTPUT
L	L	L	L
L	L	H	H
L	H	X	O
H	L	X	O
H	H	X	O

MB 486



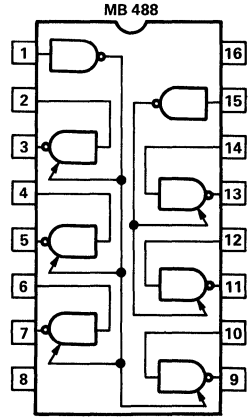
$\overline{\text{ENABLE 2}}$	$\overline{\text{ENABLE 1}}$	INPUT	OUTPUT
L	L	L	H
L	L	H	L
L	H	X	O
H	L	X	O
H	H	X	O

MB 487



$\overline{\text{ENABLE}}$	INPUT	OUTPUT
L	L	L
L	H	H
H	X	O

MB 488



$\overline{\text{ENABLE}}$	INPUT	OUTPUT
L	L	H
L	H	L
H	X	O

L: LOW LEVEL
H: HIGH LEVEL
O: HIGH IMPEDANCE STATE (OPEN)
X: IRRELEVANT

APPLICATIONS

- Address Buffer on the Fujitsu MBL 6800 microprocessor unit or similar devices.
- Level Converter of TTL/DTL or MOS/CMOS to 3-state TTL bus level

GUARANTEED OPERATING RANGE

Part Number	Supply Voltage (V_{CC})			Ambient Temperature
	Min.	Typ.	Max.	
MB 485, MB 486, MB 487, MB 488	+4.75V	+5.0V	+5.25V	0°C to + 75°C

AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = 25°C unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Circuit
Propagation Delay Input to Output (R_L = 200 ohm, C_L = 50 pF)	MB 485/MB 487	t_{PLH}	3	7	12	ns	Fig. 14
	MB 486/MB 488		4	7	11		
	MB 485/MB 487	t_{PHL}	3	9	13	ns	Fig. 14
	MB 486/MB 488		3	6	10		
Propagation Delay $\overline{\text{Enable}}$ to Output (R_L = 200 ohm, C_L = 5 pF)	MB 485/MB 487	$t_{PLO(\overline{E})}$	3	6	12	ns	Fig. 15 Fig. 16
	MB 486/MB 488		5	10	16		
	MB 485/MB 487	$t_{PHO(\overline{E})}$	3	5	10	ns	
	MB 486/MB 488		3	6	10		
Propagation Delay $\overline{\text{Enable}}$ to Output (R_L = 200 ohm, C_L = 50 pF)	MB 485/MB 487	$t_{POL(\overline{E})}$	12	14	25	ns	Fig. 15 Fig. 16
	MB 486/MB 488		11	18	24		
	MB 485/MB 487	$t_{POH(\overline{E})}$	8	19	25	ns	
	MB 486/MB 488		7	15	22		

Note: C_L includes jig and probe capacitance.

DC CHARACTERISTICS

(T_A = 0°C to +75°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Min.	Unit	Test Circuit
Output High Voltage (V_{CC} = 4.75V, I_{OH} = –5.2 mA)	V_{OH}	2.4	3.0	—	V	Fig. 1
Output Low Voltage (V_{CC} = 4.75V, I_{OL} = 43 mA)	V_{OL}	—	—	0.5	V	Fig. 2
Input High Current for Inputs (V_{CC} = 5.25V, $V_{IH(I)}$ = 2.4V)	$I_{IH(I)}$	—	—	40	μA	Fig. 3
Input High Current for $\overline{E}$ (V_{CC} = 5.25V, $V_{IH(\overline{E})}$ = 2.4V)	$I_{IH(\overline{E})}$	—	—	- 40	μA	Fig. 4
Input Low Current for Inputs (V_{CC} = 5.25V, $V_{IL(I)}$ = 0.5V)	$I_{IL(I)}$	—	—	-400	μA	Fig. 5
Input Low Current for $\overline{E}$ (V_{CC} = 5.25V, $V_{IL(\overline{E})}$ = 0.5V)	$I_{IL(\overline{E})}$	—	—	-400	μA	Fig. 6
Output 3-State Current (V_{CC} = 5.25V, V_{OH} = 2.4V)	I_{OZ1}	—	—	40	μA	Fig. 7
Output 3-State Current (V_{CC} = 5.25V, V_{OL} = 0.5V)	I_{OZ2}	—	—	- 40	μA	Fig. 8
Output Short Circuit Current (V_{CC} = 5.25V)	I_{OS}	-40	-80	–115	mA	Fig. 9
Power Supply Current for MB 485/MB 487 (V_{CC} = 5.25V)	I_{CC}	—	65	98	mA	Fig. 10
Power Supply Current for MB 486/MB 488 (V_{CC} = 5.25V)	I_{CC}	—	59	89	mA	Fig. 10
Input Clamp Voltage (V_{CC} = 4.75V, I_{IC} = –12 mA)	V_{IC}	—	—	–1.5	V	Fig. 11
Output Clamp Voltage (V_{CC} = 0V, I_{OC} = –12 mA)	V_{OC}	—	—	–1.5	V	Fig. 12
Input Voltage Rating (I_I = 1.0 mA)	V_I	5.5	—	—	V	Fig. 13
Input High Voltage (V_{CC} = 4.75V, T_A = 25°C)	V_{IH}	2.0	—	—	V	—
Input Low Voltage (V_{CC} = 4.75V, T_A = 25°C)	V_{IL}	—	—	0.8	V	—

FIG. 1 V_{OH}

TEST TABLE

PART NO.	$DI_{A\text{-}F}$
MB485, MB487	0.8V
MB486, MB488	2.0V

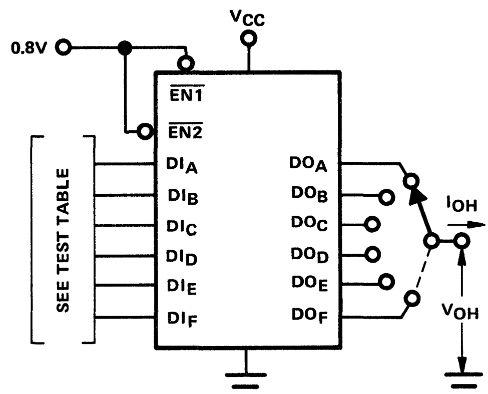


FIG. 2 V_{OL}

TEST TABLE

PART NO.	$DI_{A\text{-}F}$
MB485, MB487	0.8V
MB486, MB488	2.0V

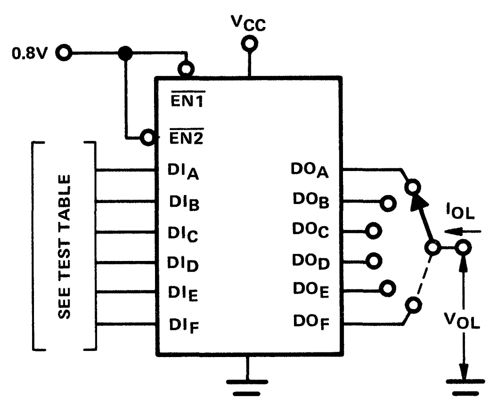


FIG 3. $I_{IH(I)}$

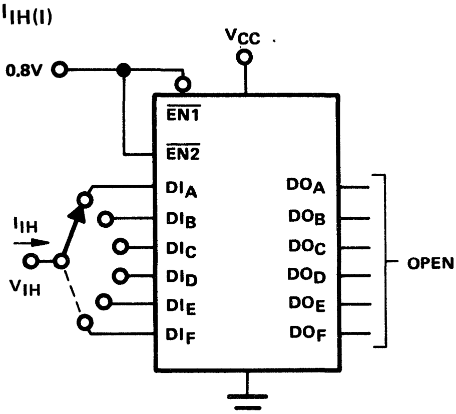


FIG. 4 $I_{IH(\overline{E})}$

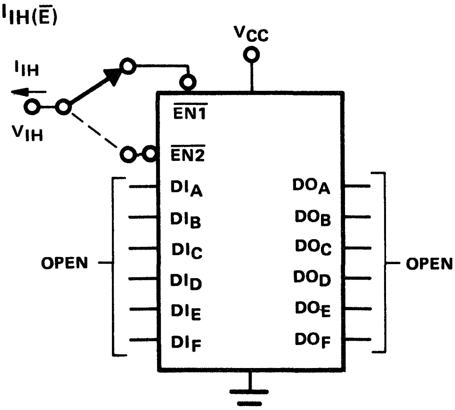


FIG. 5 $I_{IL(I)}$

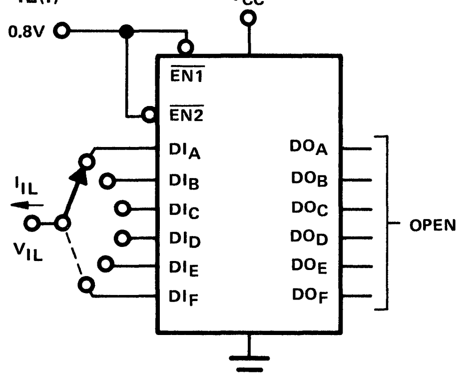


FIG. 6 $I_{IL(\overline{E})}$

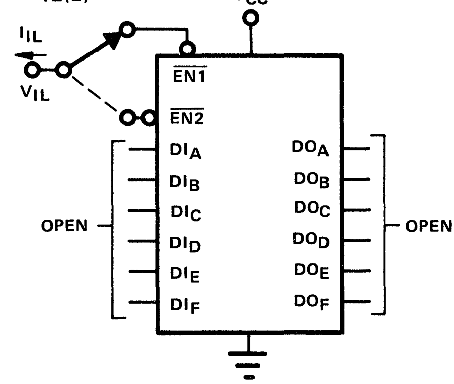


FIG. 7 I_{OZ1}

TEST TABLE

PART NO.	$DI_{A\text{-}F}$	$\overline{EN1}$	$\overline{EN2}$
MB485, MB486	0.8V	2.0V	0.8V
		0.8V	2.0V
	2.0V	2.0V	0.8V
		0.8V	2.0V
MB487, MB488	0.8V	2.0V	2.0V
	2.0V		

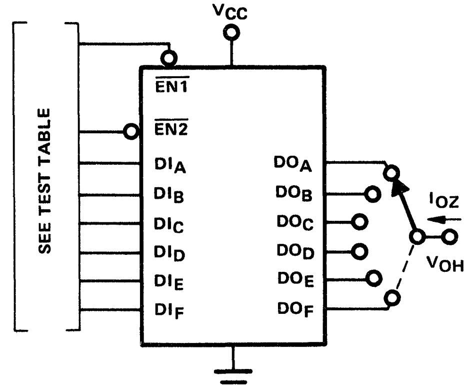


FIG. 8. I_{OZ2}

TEST TABLE

PART NO.	$DI_{A\text{-}F}$	$\overline{EN1}$	$\overline{EN2}$
MB485, MB486	0.8V	2.0V	0.8V
		0.8V	2.0V
	2.0V	2.0V	0.8V
		0.8V	2.0V
MB487, MB488	0.8V	2.0V	2.0V
	2.0V		

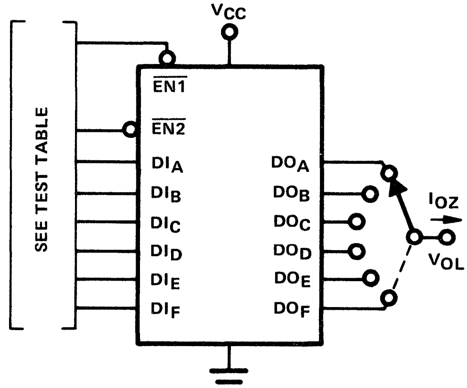


FIG 9. I_{OS}

TEST TABLE

PART NO.	DI_{A-F}
MB485, MB487	4.5V
MB486, MB488	0V

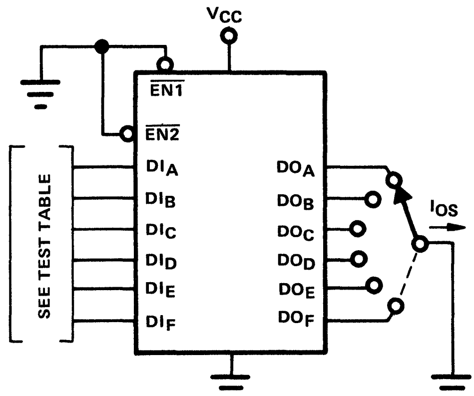


FIG.10. I_{CC}

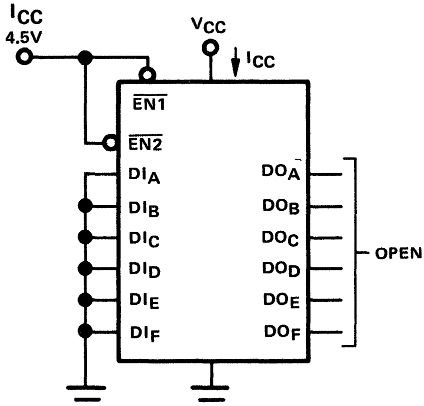


FIG. 11 V_{IC}

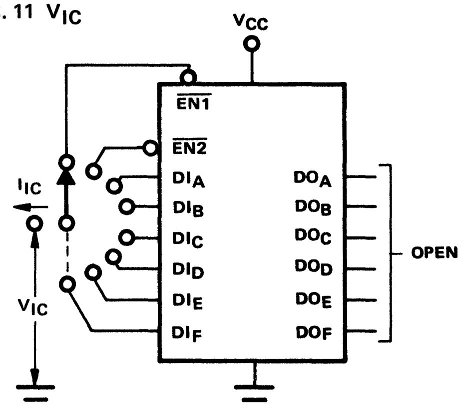


FIG. 12 V_{OC}

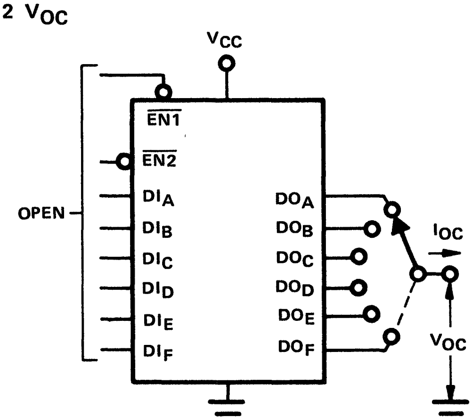


FIG. 13 V_I

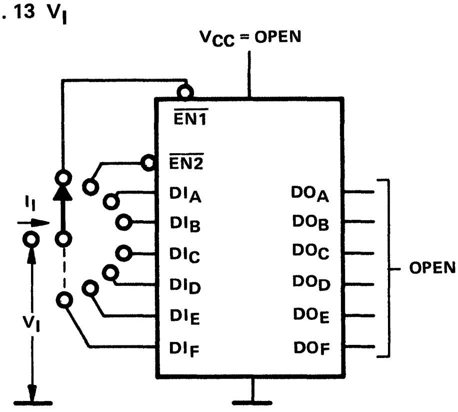
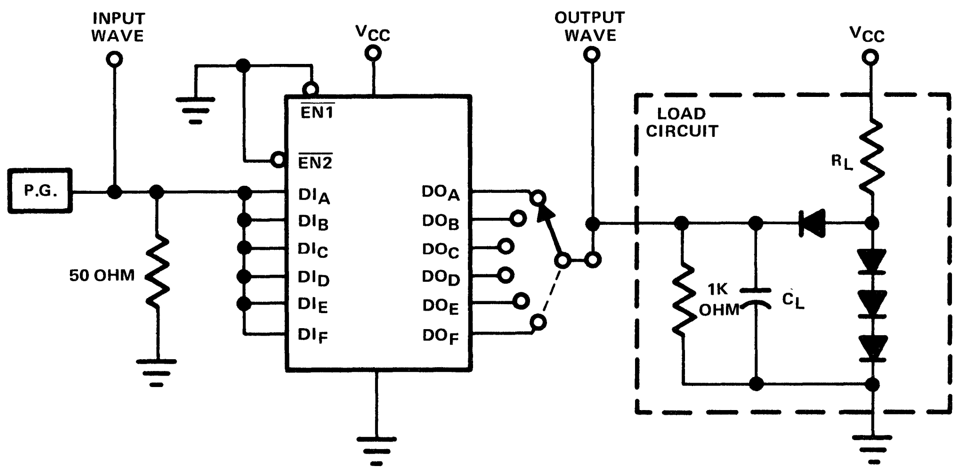
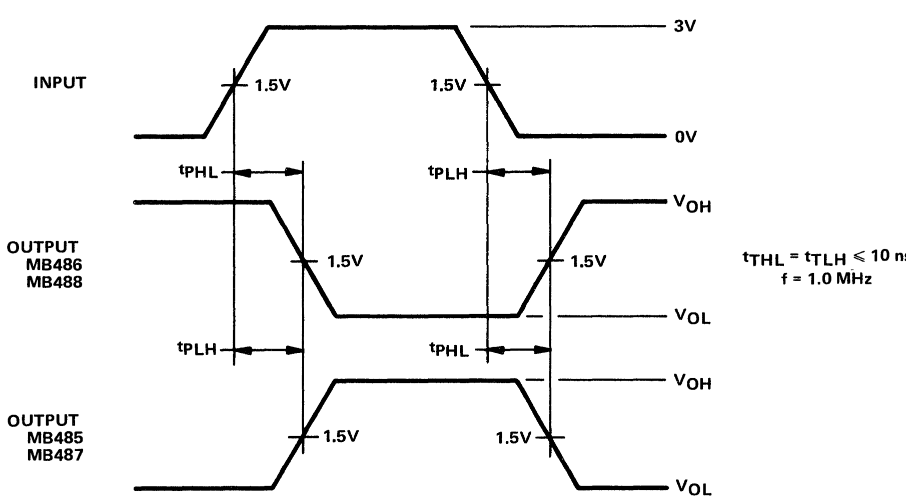


FIG. 14 t_{PLH}/t_{PHL}





Interface Devices

FIG. 15 $t_{PLO(\overline{E})}/t_{PHO(\overline{E})}/t_{POL(\overline{E})}/t_{POH(\overline{E})}$ FOR MB 485 AND MB 487

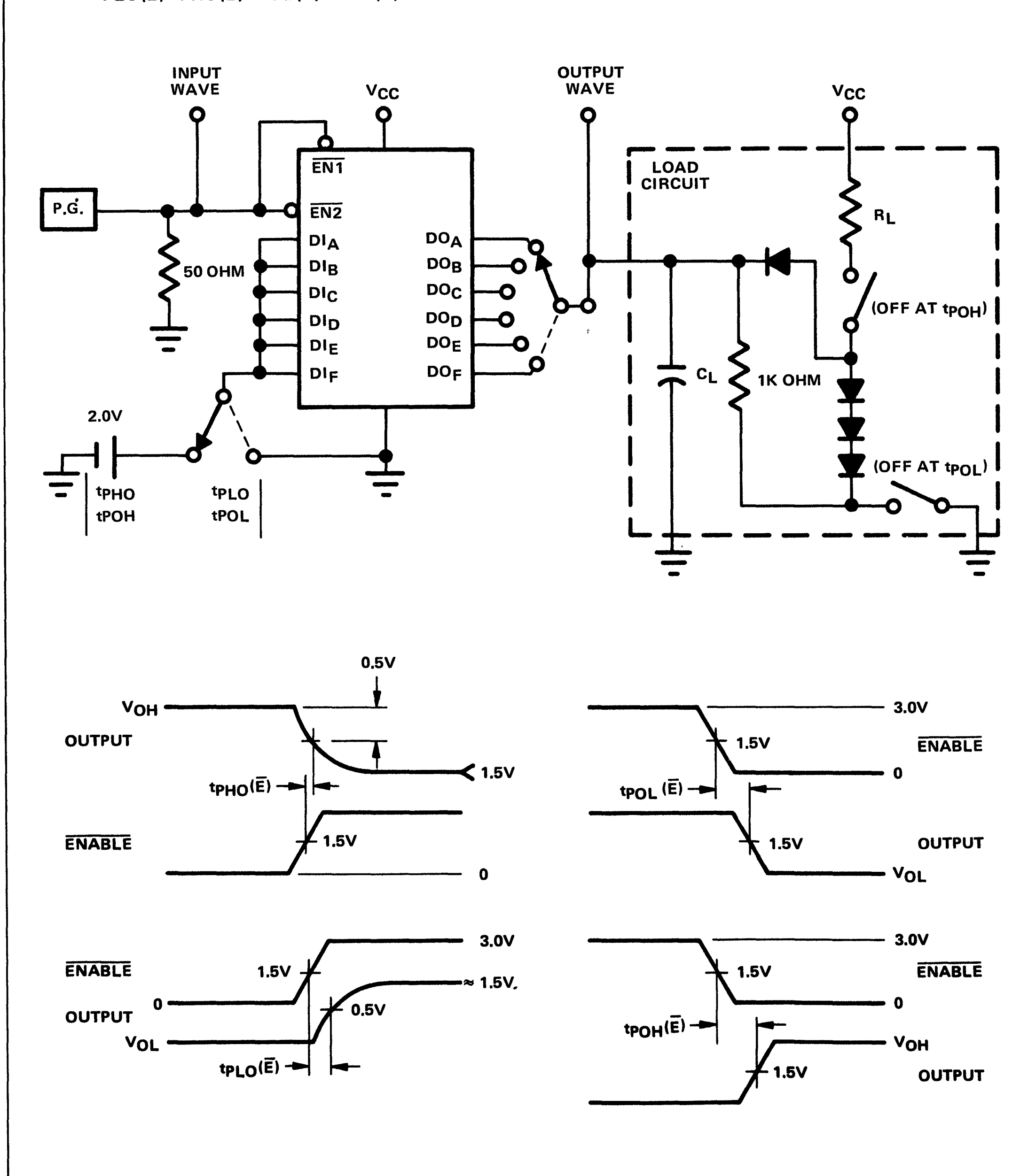
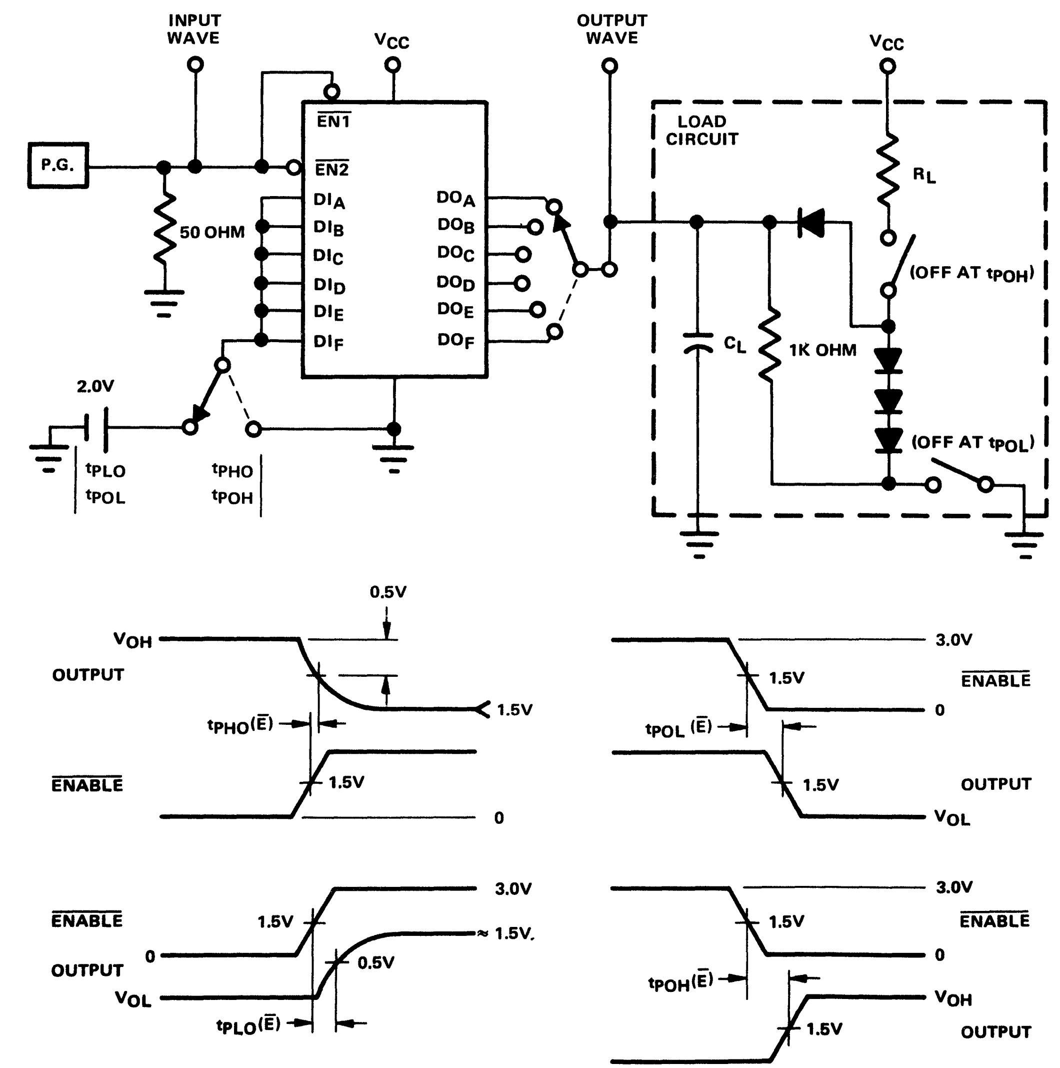
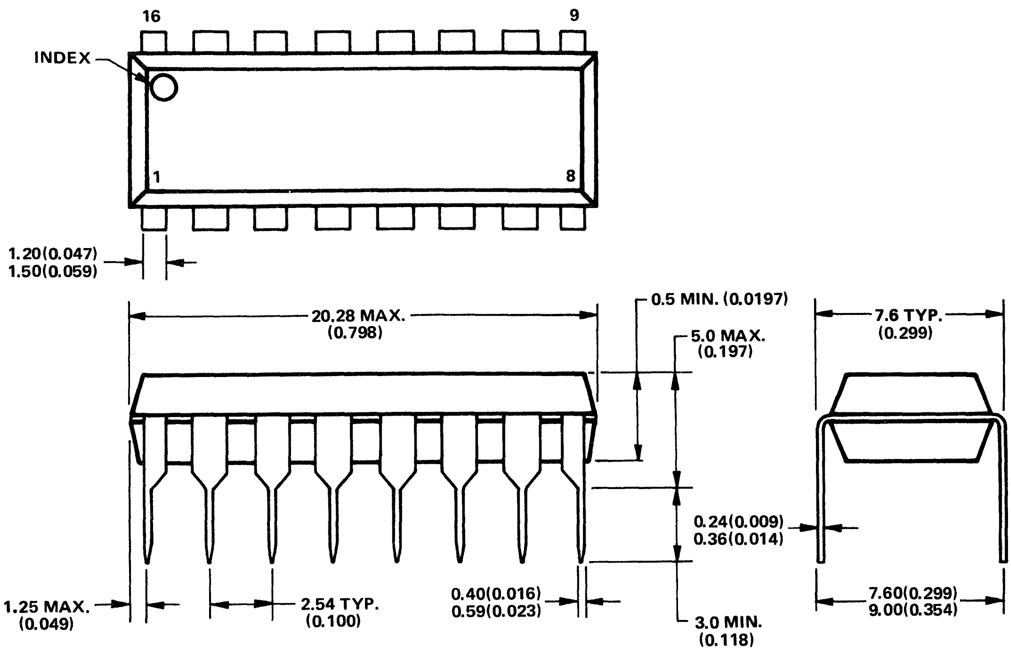


FIG. 16 $t_{PLO(\overline{E})}/t_{PHO(\overline{E})}/t_{POL(\overline{E})}/t_{POH(\overline{E})}$ FOR MB 486 AND MB 488



Interface Devices

PACKAGE DIMENSIONS



Dimensions in millimeters

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