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μA LINEAR

1982 LINEAR DIVISION PRODUCTS

FAIRCHILD

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Introduction

Product specifications in this data book cover the current standard linear product line. The data sheets included are organized in sections by type of product—Operational Amplifier, Comparator, Voltage Regulator, Interface, Data Acquisition, Telecommunication, and Special Function. In addition, a separate section covers hybrid voltage regulators.

Basic product specifications are listed on each data sheet, including maximum ratings, electrical characteristics, performance curves, and packaging information. For many products, typical applications and test circuits are also included. A separate section on packaging includes detailed information about the various packages available. The codes included on each data sheet indicate the specific package(s) offered for the product.

An industry cross reference keys Fairchild linear products to direct replacements and functional equivalents offered by other major linear product manufacturers. In addition, there is an alpha-numeric product listing including all basic part numbers. Electrical, temperature, and package variations as indicated by suffixes are not included in the alpha-numeric listing. These variations are indicated on the data sheet referenced under Order Information. An explanation of the part numbering method appears at the beginning of the packaging section.

Information about high reliability linear products and any other product information may be obtained from a local sales office or by contacting:

Fairchild Linear Products
Marketing Department MS 4-370
313 Fairchild Drive
Mountain View, California 94042

Any inquiries involving the hybrid voltage regulators included in this data book should be directed to:

Fairchild Hybrid Products
Marketing Department MS 19-1425
369 Whisman Road
Mountain View, California 94042

The specifications included in this data book are as current and correct as could reasonably be determined at time of printing. Any errors noted by users, whether involving content or omission, can be directed to Linear Marketing at the above address; such information would be appreciated.

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Alpha Numeric Index

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Industry Cross Reference Guide

Part Number	Fairchild Equivalent
AMD	
715DC	μA715DC
715HC	μA715HC
715DM	μA715DM
715HM	μA715HM
723DC	μA723DC
723DM	μA723DM
723HC	μA723HC
723HM	μA723HM
723PC	μA723PC
725HC	μA725HC
725HM	μA725HM
733DC	μA733DC
733DM	μA733DM
733HC	μA733HC
733HM	μA733HM
741FM	μA741FM
741HC	μA741HC
741HM	μA741HM
741AFM	μA741AFM
741AHM	μA741AHM
741EHC	μA741EHC
747DC	μA747DC
747DM	μA747DM
747HC	μA747HC
747HM	μA747HM
747PC	μA747PC
747ADM	μA747ADM
747AHM	μA747AHM
747EDC	μA747EDC
747EHC	μA747EHC
748HC	μA748HC
748HM	μA748HM
AM1408L6	μA0802CDC
AM1408L7	μA0802BDC
AM1408L8	μA0802ADC
AM1458H	μA1458HC
AM1508L8	μA0802DM
AM1558H	μA1558HM
DAC-08CQ	μA0801CDC
DAC-08EQ	μA0801EDC
DAC-08Q	μA0801DM
LM101H	μA101HM
LM101AH	μA101AHM
LM105H	μA105HM
LM108H	μA108HM
LM108AH	μA108AHM
LM111H	μA111HM
LM124D	μA124DM

Part Number	Fairchild Equivalent
AMD (Cont.)	
LM139D	μA139DM
LM139AD	μA139ADM
LM201H	μA201HC
LM201AH	μA201AHM
LM208H	μA208HM
LM208AH	μA208AHM
LM224D	μA224DV
LM239D	μA239DC
LM239AD	μA239ADC
LM301AH	μA301AHC
LM305H	μA305HC
LM305AH	μA305AHC
LM308H	μA308HC
LM308AH	μA308AHC
LM311H	μA311HC
LM324D	μA324DC
LM324N	μA324PC
LM339D	μA339DC
LM339N	μA339PC
LM339AD	μA339ADC
LM339AN	μA339APC
INTERSIL	
ICL108LNTY	μA108HM
ICL741CHSPA	μA741TC
ICL741MHSTY	μA741HM
LM101AH	μA101AHM
LM105H	μA105HM
LM108H	μA108HM
LM108AH	μA108AHM
LM111H	μA111HM
LM124J	μA124DM
LM301AH	μA301AHC
LM301AN	μA301ATC
LM305H	μA305HC
LM308H	μA308HC
LM308N	μA308TC
LM308AH	μA308AHC
LM308AN	μA308ATC
LM311H	μA311HC
LM311N	μA311TC
LM324J	μA324DC
LM324N-14	μA324PC
NE555N	μA555TC
NE556N	μA556PC
μA723DC	μA723DC
μA723DM	μA723DM
μA723HC	μA723HC

Part Number	Fairchild Equivalent
INTERSIL (Cont.)	
μA723HM	μA723HM
μA723PC	μA723PC
μA733HC	μA733HC
μA733HM	μA733HM
μA741FM	μA741FM
μA741HC	μA741HC
μA741HM	μA741HM
μA741TC	μA741TC
μA748HC	μA748HC
μA748HM	μA748HM
μA748TC	μA748TC
MOTOROLA	
LM101AH	μA101AHM
LM105HM	μA105HM
LM108H	μA108HM
LM108AH	μA108AHM
LM109K	μA109KM
LM111H	μA111HM
LM111J-8	μA111RM
LM117K	μA117KM
LM124J	μA124DM
LM139J	μA139DM
LM139AJ	μA139ADM
LM201AH	μA201AHM
LM208H	μA208HM
LM208AH	μA208AHM
LM209K	μA209KM
LM217K	μA217UV
LM224J	μA224DV
LM239AJ	μA239ADC
LM239J	μA239DC
LM293H	*μA293RC
LM293AH	*μA293ARC
LM301AH	μA301AHC
LM301AN	μA301ATC
LM305H	μA305HC
LM308AH	μA308AHC
LM308AN	μA308ATC
LM308H	μA308HC
LM308N	μA308TC
LM309K	μA309KC
LM311H	μA311HC
LM311J-8	μA311RC
LM311N	μA311TC
LM317K	μA317KC
LM317T	μA317UC
LM324J	μA324DC

*Note
Not exact package replacement

Part Number	Fairchild Equivalent
MOTOROLA (Cont.)	
LM339AJ	μA339ADC
LM339J	μA339DC
LM393AN	μA393ATC
LM393N	μA393TC
LM710CH	μA710HC
LM711CH	μA711HC
LM723CH	μA723HC
LM723CJ	μA723DC
LM741CH	μA741HC
LM741CN	μA741TC
LM2901N	μA2901PC
LM2902N	μA2902PV
LM2903N	μA2903TC
MC1408L6	μA0802CDC
MC1408L7	μA0802BDC
MC1408L8	μA0802ADC
MC1408P6	μA0802CPC
MC1408P7	μA0802BPC
MC1408P8	μA0802APC
MC1411P	μA9665PC
MC1412P	μA9666PC
MC1413P	μA9667PC
MC1416P	μA9668PC
MC1455P1	μA555TC
MC1458CG	μA1458CHC
MC1458CP1	μA1458CTC
MC1458CU	μA1458CRC
MC1458G	μA1458HC
MC1458P1	μA1458TC
MC1458U	μA1458RC
MC1488L	μA1488DC
MC1488P	μA1488PC
MC1489L	μA1489DC
MC1489P	μA1489PC
MC1489AL	μA1489ADC
MC1489AP	μA1489APC
MC1508L8	μA0802DM
MC1558G	μA1558HM
MC1558U	μA1558RM
MC1709CP1	μA709TC
MC1709CP2	μA709PC
MC1709G	μA709HM
MC1710CG	μA710HC
MC1710CL	μA710DC
MC1710CP	μA710PC
MC1710G	μA710HM
MC1710L	μA710DM
MC1711CG	μA711HC
MC1711CL	μA711DC
MC1711CP	μA711PC
MC1711G	μA711HM
MC1711L	μA711DM
MC1723CG	μA723HC
MC1723CL	μA723DC
MC1723CP	μA723PC
MC1723G	μA723HM
MC1723L	μA723DM
MC1733G	μA733HM
MC1733L	μA733DM
MOTOROLA (Cont.)	
MC1733CG	μA733HC
MC1733CL	μA733DC
MC1741CG	μA741HC
MC1741CP1	μA741TC
MC1741CU	μA741RC
MC1741G	μA741HM
MC1747CG	μA747HC
MC1747CL	μA747DC
MC1747CP2	μA747PC
MC1747G	μA747HM
MC1747L	μA747DM
MC1748CG	μA748HC
MC1748CP1	μA748TC
MC1748G	μA748HM
MC1776CG	μA776HC
MC1776CP1	μA776TC
MC1776G	μA776HM
MC3302L	μA3302DC
MC3302P	μA3302PC
MC3303P	μA3303PC
MC3386P	μA3086PC
MC3403L	μA3403DC
MC3403P	μA3403PC
MC3440AP	μA9640PC
MC3443P	μA9640PC
MC3448AL	μA3448ADC
MC3448AP	μA3448APC
MC3456P	μA556PC
MC3458P1	μA798TC
MC3488AP	μA9636AT
MC3558U	*μA798TC
MC55107L	μA55107ADM
MC75107L	μA75107ADC
MC75107P	μA75107APC
MC75450P	μA75450BPC
MC75451U	μA75451ARC
MC75452U	μA75452ARC
MC75453U	μA75453ARC
MC75461P	μA75461TC
MC75462P	μA75462TC
MC75491P	μA75491PC
MC75492P	μA75492PC
MC7805K	μA7805KM
MC7805CK	μA7805KC
MC7805CT	μA7805UC
MC7806CK	μA7806KC
MC7806CT	μA7806UC
MC7812K	μA7812KM
MC7812CK	μA7812KC
MC7812CT	μA7812UC
MC7815K	μA7815KM
MC7815CK	μA7815KC
MC7815CT	μA7815UC
MC7818K	μA7818KM
MC7818CK	μA7818KC
MC7818CT	μA7818UC
MC7824K	μA7824KM
MC7824CK	μA7824KC
MC7824CT	μA7824UC
MOTOROLA (Cont.)	
MC78L05ACP	μA78L05AWC
MC78L12ACP	μA78L12AWC
MC78L15ACP	μA78L15AWC
MC78M05CG	μA78M05HC
MC78M05CT	μA78M05UC
MC78M06CG	μA78M06HC
MC78M06CT	μA78M06UC
MC78M08CG	μA78M08HC
MC78M08CT	μA78M08UC
MC78M12CG	μA78M12HC
MC78M12CT	μA78M12UC
MC78M15CT	μA78M15UC
MC78M24CT	μA78M24UC
MC7905CK	μA7905KC
MC7905CT	μA7905UC
MC7908CK	μA7908KC
MC7908CT	μA7908UC
MC7912CK	μA7912KC
MC7912CT	μA7912UC
MC7915CK	μA7915KC
MC7915CT	μA7915UC
MC8T26AP	μA8T26APC
MC8T26AL	μA8T26ADC
MC8T28AP	μA8T28PC
MC8T28AL	μA8T28DC
SN75451BP	*μA75451BTC
SN75452BP	μA75452BTC
SN75453BP	μA75453BTC
μA710HC	μA710HC
μA711HC	μA711HC
μA723DC	μA723DC
μA723HC	μA723HC
μA723PC	μA723PC
μA741HC	μA741HC
μA741TC	μA741TC
NATIONAL	
DS75107J	μA75107ADC
DS75107N	μA75107APC
DS75108N	μA75108BPC
DS75450N	μA75450BPC
DS75451J-8	μA75451ARC
DS75451N	μA75451ATC
DS75452J-8	μA75452ARC
DS75452N	μA75452ATC
DS75453J-8	μA75453ARC
DS75453N	μA75453ATC
DS75461N	μA75461TC
DS75462N	μA75462TC
DS75491N	μA75491PC
DS75492N	μA75492PC
DS8T26AJ	μA8T26ADM
DS8T28J	μA8T28DM
LF351N	μA771TC
LF353N	μA772TC
LF398H	μA398HC
LM101AH	μA101AHM
LM105H	μA105HM
LM108H	μA108HM

*Note

Not exact package replacement

Part Number	Fairchild Equivalent
NATIONAL (Cont.)	
LM108H	μA108AHM
LM109K	μA109KM
LM111H	μA111HM
LM124J	μA124DM
LM139J	μA139DM
LM139AJ	μA139ADM
LM140K-5.0	μA7805KM
LM140K-8.0	μA7808KM
LM140K-12	μA7812KM
LM140K-15	μA7815KM
LM140K-18	μA7818KM
LM140K-24	μA7824KM
LM201AH	μA201AHM
LM208H	μA208HM
LM208AH	μA208AHM
LM209K	μA209KM
LM224J	μA224DV
LM239J	μA239DC
LM239AJ	μA239ADC
LM301AH	μA301AHC
LM301AN	μA301ATC
LM305H	μA305HC
LM305AH	μA305AHC
LM308H	μA308HC
LM308N	μA308TC
LM308AH	μA308AHC
LM308AN	μA308ATC
LM309K	μA309KC
LM311H	μA311HC
LM311J-8	μA311RC
LM311N	μA311TC
LM317K	μA317KC
LM317T	μA317UC
LM324J	μA324DC
LM324N	μA324PC
LM339J	μA339DC
LM339N	μA339PC
LM339AJ	μA339ADC
LM339AN	μA339APC
LM340K-5.0	μA7805KC
LM340T-5.0	μA7805UC
LM340K-6.0	μA7806KC
LM340K-8.0	μA7808KC
LM340K-12	μA7812KC
LM340T-12	μA7812UC
LM340K-15	μA7815KC
LM340T-15	μA7815UC
LM340K-18	μA7818KC
LM340K-24	μA7824KC
LM348J	μA348DC
LM348N	μA348PC
LM376N	μA376TC
LM393N	μA393TC
LM555CN	μA555TC
LM556CN	μA556PC
LM709H	μA709HM
LM709CH	μA709HC
LM709CN	μA709PC
LM709CN-8	μA709TC
NATIONAL (Cont.)	
LM709AH	μA709AHM
LM710H	μA710HM
LM710CH	μA710HC
LM710CN	μA710PC
LM711H	μA711HM
LM711CH	μA711HC
LM711CN	μA711PC
LM723H	μA723HM
LM723J	μA723DM
LM723CH	μA723HC
LM723CJ	μA723DC
LM723CN	μA723PC
LM725H	μA725HM
LM725CH	μA725HC
LM725CN	μA725TC
LM733H	μA733HM
LM733CH	μA733HC
LM733CN	μA733PC
LM741H	μA741HM
LM741AH	μA741AHM
LM741CH	μA741HC
LM741CJ	μA741RC
LM741CN	μA741TC
LM741EH	μA741EHC
LM741EN	μA741ETC
LM747H	μA747HM
LM747J	μA747DM
LM747AH	μA747AHM
LM747AJ	μA747ADM
LM747CH	μA747HC
LM747CJ	μA747DC
LM747CN	μA747PC
LM747EH	μA747EHC
LM747EJ	μA747EDC
LM748H	μA748HM
LM748CH	μA748HC
LM748CN	μA748TC
LM760CH	μA760HC
LM1458H	μA1458HC
LM1458J	μA1458RC
LM1458N	μA1458TC
LM1558H	μA1558HM
LM1558J	μA1558RM
LM2901N	μA2901PC
LM2901J	μA2901DC
LM2903N	μA2903TC
LM3086N	μA3086PC
LM3302J	μA3302DC
LM3302N	μA3302PC
LM7805CK	μA7805KC
LM7805CT	μA7805UC
LM7812CK	μA7812KC
LM7812CT	μA7812UC
LM7815CK	μA7815KC
LM7815CT	μA7815UC
LM78L05ACZ	μA78L05AWC
LM78L12ACZ	μA78L12AWC
LM78L15ACZ	μA78L15AWC
LM78M05CP	*μA78M05UC
NATIONAL (Cont.)	
LM78M12CP	*μA78M12UC
LM78M15CP	*μA78M15UC
LM7905CK	μA7905KC
LM7905CT	μA7905UC
LM7912CK	μA7912KC
LM7912CT	μA7912UC
LM7915CK	μA7915KC
LM7915CT	μA7915UC
LM7905CH	μA79M05AHC
LM7912CH	μA79M12AHC
LM7915CH	μA79M15AHC
PMI	
CMP-03AJ	μA111HM
CMP-03AZ	μA111RM
CMP-04BY	μA139DM
CMP-04FY	μA239DC
DAC-08Q	μA0801DM
DAC-08Q	μA0802DM
DAC-08CP	μA0801CPC
DAC-08CP	μA0802BPC
DAC-08CQ	μA0801CDC
DAC-08CQ	μA0802BDC
DAC-08EP	μA0801EPC
DAC-08EP	μA0802APC
DAC-08EQ	μA0801EDC
DAC-08EQ	μA0802ADC
DAC1408A-6P	μA0802CPC
DAC1408A-6Q	μA0802CDC
DAC1408A-7P	μA0802BPC
DAC1408A-7Q	μA0802BDC
DAC1408A-8P	μA0802APC
DAC1408A-8Q	μA0802ADC
DAC1508A-8Q	μA0802DM
OP-07J	μA714HM
OP-07CJ	μA714HC
OP-07EJ	μA714EHC
PM108J	μA108HM
PM108AJ	μA108AHM
PM111J	μA111HM
PM111Z	μA111RM
PM139Y	μA139DM
PM208J	μA208HM
PM208AJ	μA208AHM
PM308J	μA308HC
PM308P	μA308TC
PM308AJ	μA308AHC
PM308AP	μA308ATC
PM311J	μA311HC
PM311Z	μA311RC
PM339Y	μA339DC
PM339AY	μA339ADC
PM725J	μA725HM
PM725CJ	μA725HC
PM725CP	μA725TC
PM741J	μA741HM
PM741CJ	μA741HC
PM741CZ	μA741RC
PM1458J	μA1458HC

Note

Not exact package replacement

Part Number	Fairchild Equivalent
PMI (Cont.)	
PM1458Z	μA1458RC
PM1558J	μA1558HM
PM1558Z	μA1558RM
SIGNETICS	
LM101AH	μA101AHM
LM111H	μA111HM
LM124F	μA124DM
LM139F	μA139DM
LM193FE	μA193RM
LM201AN	*μA201AHM
LM224N	μA224PV
LM224F	μA224DV
LM301AN	μA301ATC
LM324N	μA324PC
LM324F	μA324DC
LM339N	μA339PC
LM339F	μA339DC
LM2901F	μA2901DC
LM2901N	μA2901PC
LM2903FE	μA2903RC
LM2903N	μA2903TC
MC1458FE	μA1458RC
MC1458H	μA1458HC
MC1458N	μA1458TC
MC1488N	μA1488PC
MC1488F	μA1488DC
MC1489N	μA1489PC
MC1489F	μA1489DC
MC1489AN	μA1489APC
MC1489AF	μA1489ADC
MC1558H	μA1558HM
MC1558FE	μA1558RM
MC3302N	μA3302PC
MC3302F	μA3302DC
NE5501	μA9665PC
ULN2001N	μA9665PC
ULN2003F	μA9667DC
ULN2003N	μA9667PC
ULN2004F	μA9668DC
ULN2004N	μA9668PC
μA723F	μA723DM
μA723H	μA723HM
μA723CF	μA723DC
μA723CH	μA723HC
μA723CN	μA723PC
μA733F	μA733DM
μA733H	μA733HM
μA733CF	μA733DC
μA733CH	μA733HC
μA733CN	μA733PC
μA741FE	μA741RM
μA741CFE	μA741RC
μA741CN	μA741TC
μA747F	μA747DM
μA747H	μA747HM
μA747CF	μA747DC
μA747CH	μA747HC
μA747CN	μA747PC
μA748CN	μA748TC

Part Number	Fairchild Equivalent
SILICON GENERAL	
SG101T	μA101HM
SG101AT	μA101AHM
SG105T	μA105HM
SG108T	μA108HM
SG108AT	μA108AHM
SG109K	μA109KM
SG111T	μA111HM
SG117K	μA117KM
SG124J	μA124DM
SG139J	μA139DM
SG139AJ	μA139ADM
SG201T	μA201HC
SG201AT	μA201AHM
SG208T	μA208HM
SG208AT	μA208AHM
SG209K	μA209KM
SG217P	μA217UV
SG224J	μA224DV
SG224N	μA224PV
SG239J	μA239DC
SG239N	μA239PC
SG239AJ	μA239ADC
SG239AN	μA239APC
SG301AM	μA301ATC
SG301AT	μA301AHC
SG305T	μA305HC
SG305AT	μA305AHC
SG308M	μA308TC
SG308T	μA308HC
SG308AM	μA308ATC
SG308AT	μA308AHC
SG309K	μA309KC
SG311M	μA311TC
SG311T	μA311HC
SG317K	μA317KC
SG317P	μA317UC
SG324J	μA324DC
SG324N	μA324PC
SG339J	μA339DC
SG339N	μA339PC
SG339AJ	μA339ADC
SG339AN	μA339APC
SG555M	μA555TC
SG556N	μA556PC
SG710J	μA710DM
SG710T	μA710HM
SG710CN	μA710PC
SG710CT	μA710HC
SG711J	μA711DM
SG711T	μA711HM
SG711CJ	μA711DC
SG711CN	μA711PC
SG711CT	μA711HC
SG723CJ	μA723DC
SG723CT	μA723HC
SG723J	μA723DM
SG723T	μA723HM
SG723CN	μA723PC

Part Number	Fairchild Equivalent
SILICON GENERAL (Cont.)	
SG733J	μA733DM
SG733T	μA733HM
SG733CJ	μA733DC
SG733CN	μA733PC
SG733CT	μA733HC
SG741F	μA741FM
SG741T	μA741HM
SG741CM	μA741TC
SG747J	μA747DM
SG747T	μA747HM
SG747CJ	μA747DC
SG747CN	μA747PC
SG747CT	μA747HC
SG748T	μA748HM
SG748CM	μA748TC
SG748CT	μA748HC
SG1458M	μA1458TC
SG1458T	μA1458HC
SG1458CM	μA1458CTC
SG1458CT	μA1458CHC
SG1488J	μA1488DC
SG1489J	μA1489DC
SG1489AJ	μA1489ADC
SG1558T	μA1558HM
SG2001J	*μA9665PC
SG2002J	μA9666DC
SG2003J	μA9667DC
SG3086J	μA3086DC
SG3086N	μA3086PC
SG3302J	μA3302DC
SG3302N	μA3302PC
SG7805K	μA7805KM
SG7805CK	μA7805KC
SG7805CP	μA7805UC
SG7808K	μA7808KM
SG7808CK	μA7808KC
SG7808CP	μA7808UC
SG7812K	μA7812KM
SG7812CK	μA7812KC
SG7812CP	μA7812UC
SG7815K	μA7815KM
SG7815CK	μA7815KC
SG7815CP	μA7815UC
SG7818K	μA7818KM
SG7818CK	μA7818KC
SG7818CP	μA7818UC
SG7824K	μA7824KM
SG7824CK	μA7824KC
SG7824CP	μA7824UC
SG7905K	μA7905KM
SG7905CK	μA7905KC
SG7905CP	μA7905UC
SG7908K	μA7908KM
SG7908CK	μA7908KC
SG7908CP	μA7908UC
SG7912K	μA7912KM
SG7912CK	μA7912KC
SG7912CP	μA7912UC

*Note

Not exact package replacement

Part Number	Fairchild Equivalent
SILICON GENERAL (Cont.)	
SG7915K	μA7915KM
SG7915CK	μA7915KC
SG7915CP	μA7915UC
SG75450BCN	μA75450BPC
SG75451BCM	μA75451BTC
SG75451BCY	μA75451BRC
SG75452BCM	μA75452BTC
SG75452BCY	μA75452BRC
SG75453BCM	μA75453BTC
SG75453BCY	μA75453BRC
SG75461CM	μA75461TC
SG75462CM	μA75462TC
TEXAS INSTRUMENTS	
AM26S10CJ	μA9640DC
AM26S10CN	μA9640PC
LM101AJ	*μA101AHM
LM105L	μA105HM
LM111JG	μA111RM
LM124J	μA124DM
LM139J	μA139DM
LM139AJ	μA139ADM
LM148J	μA148DM
LM193JG	μA193RM
LM201AJG	*μA201AHM
LM209LA	*μA209KM
LM217KC	μA217UV
LM224J	μA224DV
LM224N	μA224PV
LM239J	μA239DC
LM239N	μA239PC
LM248J	μA248DC
LM293JG	μA293RC
LM293P	μA293TC
LM301AP	μA301ATC
LM305L	μA305HC
LM305AL	μA305AHC
LM309LA	*μA309KC
LM311JG	μA311RC
LM311P	μA311TC
LM317KC	μA317UC
LM318JG	*μA318HC
LM324J	μA324DC
LM324N	μA324PC
LM339AJ	μA339ADC
LM339AN	μA339APC
LM339J	μA339DC
LM339N	μA339PC
LM348J	μA348DC
LM348N	μA348PC
LM376P	μA376TC
LM393JG	μA393RC
LM393P	μA393TC
LM2901J	μA2901DC
LM2901N	μA2091PC
LM2902N	μA2902PV
LM2903JG	μA2903RC

Part Number	Fairchild Equivalent
TEXAS INSTRUMENTS (Cont.)	
LM2903P	μA2903TC
MC1458JG	μA1458RC
MC1458P	μA1458TC
MC1558JG	μA1558RM
NE555P	μA555TC
NE556N	μA556PC
RC4136J	μA4136DC
RC4136N	μA4136PC
SA555P	μA555TC
SN55107AJ	μA55107ADM
SN55110AJ	μA55110ADM
SN75107AJ	μA75107ADC
SN75107AN	μA75107APC
SN75107BJ	μA75107BDC
SN75107BN	μA75107BPC
SN75108BN	μA75108BPC
SN75110AJ	μA75110ADC
SN75110AN	μA75110APC
SN75114J	μA9614DC
SN75114N	μA9614PC
SN75115J	μA9615DC
SN75115N	μA9615PC
SN75150N	μA75150PC
SN75150P	μA75150TC
SN75154J	μA75154DC
SN75154N	μA75154PC
SN75188J	μA1488DC
SN75188N	μA1488PC
SN75189J	μA1489DC
SN75189N	μA1489PC
SN75189AJ	μA1489ADC
SN75189AN	μA1489APC
SN75450BN	μA75450BPC
SN75451BJG	μA75451BRC
SN75451BP	μA75451BTC
SN75452BJG	μA75452BRC
SN75452BP	μA75452BTC
SN75453BJG	μA75453BRC
SN75453BP	μA75453BTC
SN75461P	μA75461TC
SN75462P	μA75462TC
SN75471P	μA75471TC
SN75472P	μA75472TC
SN75491N	μA75491PC
SN75492N	μA75492PC
TL081ACJG	μA771ARC
TL081ACP	μA771ATC
TL081BCJG	μA771BRC
TL081BCP	μA771BTC
TL081CJG	μA771RC
TL081CP	μA771TC
TL431CLP	μA431AWC
TL494CN	μA494PC
TL494CJ	μA494DC
TL494MJ	μA494DM
ULN2001AN	μA9665PC
ULN2002AJ	μA9666DC
ULN2002AN	μA9666PC

Part Number	Fairchild Equivalent
TEXAS INSTRUMENTS (Cont.)	
ULN2003AJ	μA9667DC
ULN2003AN	μA9667PC
ULN2004AJ	μA9668DC
ULN2004AN	μA9668PC
μA709MU	μA709FM
μA709AMU	μA709AFM
μA709CP	μA709TC
μA710CJ	μA710DC
μA710CN	μA710PC
μA710MJ	μA710DM
μA711CN	μA711PC
μA711MJ	μA711DM
μA723CJ	μA723DC
μA723CN	μA723PC
μA723MJ	μA723DM
μA733CJ	μA733DC
μA733CN	μA733PC
μA733MJ	μA733DM
μA741CJG	μA741RC
μA741CP	μA741TC
μA741MJG	μA741RM
μA747C	μA747DC
μA747CN	μA747PC
μA747MJ	μA747DM
μA748CP	μA748TC
μA2240CJ	μA2240DC
μA2240CN	μA2240PC
μA7805CKC	μA7805UC
μA7808CKC	μA7808UC
μA7812CKC	μA7812UC
μA7815CKC	μA7815UC
μA7818CKC	μA7818UC
μA7824CKC	μA7824UC
μA7885CKC	μA7885UC
μA78L05CLP	μA78L05AWC
μA78L12CLP	μA78L12AWC
μA78L15CLP	μA78L15AWC
μA78M05CKC	μA78M05UC
μA78M06CKC	μA78M06UC
μA78M08CKC	μA78M08UC
μA78M12CKC	μA78M12UC
μA78M15CKC	μA78M15UC
μA78M24CKC	μA78M24UC
μA7905CKC	μA7905UC
μA7908CKC	μA7908UC
μA7912CKC	μA7912UC
μA7915CKC	μA7915UC
μA79M05CKC	μA79M05AUC
μA79M08CKC	μA79M08AUC
μA79M12CKC	μA79M12AUC
μA79M15CKC	μA79M15AUC
9614CJ	μA9614DC
9614CN	μA9614PC
9615CJ	μA9615DC
9615CN	μA9615PC

***Note**

Not exact package replacement

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Ordering Information

Three basic units of information are contained in the ordering code.

μA741	T	C
Device Type	Package Type	Temperature Range

Device Type

This group of alpha numeric characters defines the device including functional and electrical characteristics, alpha suffixes are added to further delineate electrical options.

Package Type

One alpha suffix represents the basic package style.

- D = Dual In-line (Hermetic, Ceramic)
- F = Flatpak (Hermetic)
- H = Metal Package
- J = Dual In-Line (Side Brazed)
- K = Metal Power Package (TO-3)
- P = Dual In-Line (Molded)
- R = 8-lead DIP (Hermetic, Ceramic)
- S = Metal Package (Hybrid only)
- T = 8-lead DIP (Molded)
- U = Power Package (Molded, TO-220)
- U1 = Power Package (Molded)
- W = Molded Package (TO-92 Outline)

Different outlines exist within each package style to accommodate various die sizes and number of leads. Specific dimensions for each package can be found in the Package Outline section of this catalog, listed by online code. These specific codes are referenced on each data sheet.

Temperature Range

One alpha suffix represents one of the following three basic temperature grades in common use. Exact values and conditions are specified on the device data sheets.

C = Commercial	M = Military	V = Industrial
0°C to +70/75°C	−55°C to +125°C	−20°C to 85°C
	−55°C to + 85°C	−40°C to +85°C

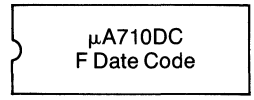
Examples

μA741FM This number code indicates a μA741 Operational Amplifier in a flatpak with military temperature rating capability.

μA725EHC This number code indicates a μA725 Instrumentation Operational Amplifier, electrical option E, in a metal package with a commercial temperature rating capability.

Device Identification

All Fairchild standard catalog linear circuits will be marked as shown in the following example.



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Voltage Regulator Testing

Linear Products

Testing Voltage Regulators
All Fairchild voltage regulators are factory-tested with automated equipment to ascertain that they meet or exceed guaranteed specifications. The testing equipment operates at relatively high speeds and automatically measures output voltage tolerances, line and load regulation, quiescent current, short-circuit current, and a long list of other voltage regulator parameters. To adequately interpret published voltage regulator specifications, it is advisable to have some understanding of the testing as performed at Fairchild. This is also important for customer incoming inspection, as some correlation is necessary between factory testing and customer acceptance testing.

Individual parameter tests performed on Fairchild voltage regulators require only a few milliseconds, so a complete regulator test can be accomplished in a fraction of a second. Such short testing times mean that the device junction temperature is very close to ambient. If the devices were tested under steady-state conditions, costs would unfortunately increase, and the increased expense would be passed on to the customer. Consequently, published parameters are based on fast testing and usually specified with a constant junction temperature of 25°C. Exceptions are noted in the individual data sheet tables.

When a regulator is operated with high dissipation, however, the effect of temperature drift must be evaluated or at least considered. For example, a μA7805 1 ampere positive voltage regulator with a junction temperature of 25°C, a 10 V input, and a load current variation of 1.5 A has a guaranteed load regulation of less than 50 mV for military-grade units and less than 100 mV for commercial-grade units. Under steady-state testing conditions, as opposed to pulsed testing conditions, junction temperature would increase by 30°C to 55°C (based on a 4°C/W junction-to-case thermal resistance and an infinite heat sink.) The μA7805 regulator has a temperature coefficient of −1.1 mV/°C, so a 30°C junction-temperature increase means an output voltage drift of −33 mV. This drift must be considered if load regulation is being measured under steady-state conditions.

Incoming inspection tests should accommodate these conditions. One approach would be to duplicate the testing procedure used by manufacturing; i.e., maintain a constant junction temperature of 25°C. If steady-state testing is performed during acceptance evaluation, a correlation between the method used in incoming inspection and the method used by Fairchild must be established. In this case, the temperature coefficients of each regulator type must be considered.

3-Terminal Regulators
Testing of 3-terminal regulators is performed at input voltages that reflect actual use conditions. The input-output voltage differential considers all of the variations associated with nominal, unregulated power supplies. For example, a 12 V regulator (μA7812) test uses a 7 V I/O voltage differential and considers the following parameters.

Device Input/Output Voltage Differential—2 V Nom.
Line Voltage Reference—10%
Filtered Supply Ripple—10%
Line Regulation—10%
Diode Drop and Source Impedance Variations—1 V

This is expressed in the following equation.

$$V_{IN} = V_{OUT(max)} + (V_{IN} - V_{OUT}) + \text{Ripple} + \text{Line Reg} + V_D$$
$$= 12.6\text{ V} + 2\text{ V} + 1.46\text{ V} + 1.6\text{ V} + 1\text{ V}$$
$$= 18.66\text{ V}$$

A 12 V regulator, then, is not only tested with a guard band, but the input voltage range used allows for greater variation than is present in actual operating conditions. All Fairchild 3-terminal regulator tests are based on similar practical considerations.

Figure 2-1 shows a self-contained load-pulsing circuit that can be used for measuring load regulation of either a positive or negative regulator. The μA555 timer operates in the astable mode as a free-running multivibrator. Transistors Q2 and Q4, along with the load resistors R_L, provide the required loading across the regulator outputs. The on and off times of Q2 and Q4 are set by potentiometers R2 and R4. Transistors Q2 and Q4 must be capable of handling the load current levels to be measured. Line regulation of positive or negative regulators can be measured using the circuits in *Figure 2-2*. Here a pulse generator switches the input voltages between $V_{IN\ (min)}$ and $V_{IN\ (max)}$ but a similar arrangement could be used by substituting a μA555 timer for the pulse generator.

Fig. 2-1 Self-Contained Load Regulation Test Circuit for Positive or Negative Regulators

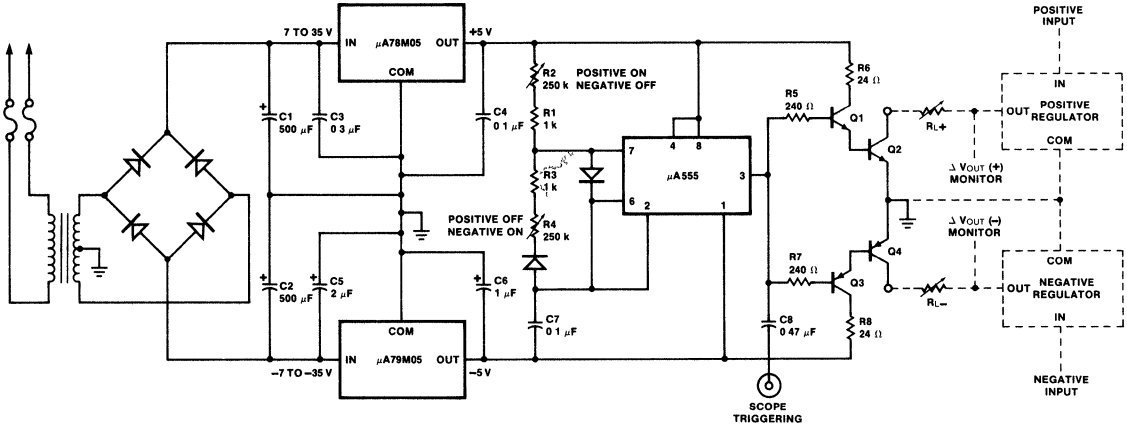
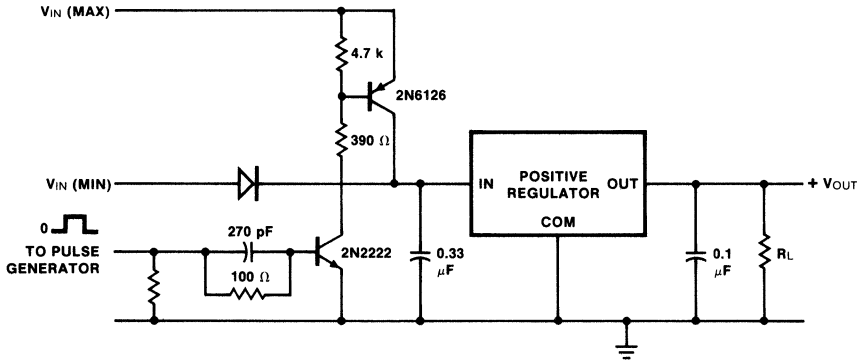
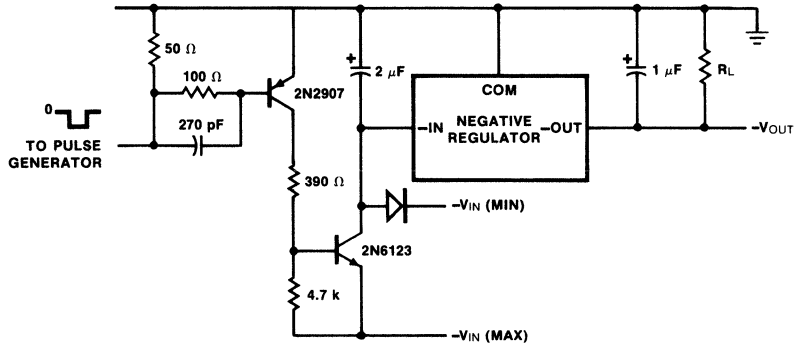


Fig. 2-2 Line Regulation Test Circuits

a. For Positive Regulators



b. For Negative Regulators



Ripple Rejection
Ripple rejection is the ratio (in dB) of the regulator input ac component (or the output of the sine wave generator) to the output ac component of the device under test. Its measurement is quite straightforward.

Ripple rejection of Fairchild regulators is normally specified at a load current of 30 to 50% of the rated output of the device. This is more realistic than the 20 mA or so specified by some other manufacturers. A regulator with good ripple rejection at low output currents may.not necessarily maintain this feature at moderate-to-high current levels unless special effort is made during the layout of the integrated circuit to keep the reference circuit on isotherms (equal temperature lines) and away from the heat source (series-pass element).

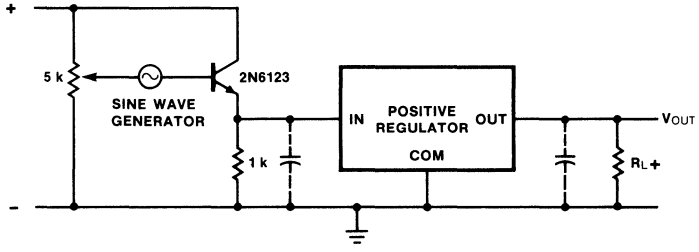
Figure 2-3 shows two simple circuits for measuring ripple rejection of positive and negative regulators.

The 5 k potentiometers in both circuits provide the bias necessary to produce the dc level of the input voltage to the regulator. The sine-wave generators are used to produce the ac component of the regulator input voltage.

Life Test and Burn-In (See *Figure 2-4*)
Burn-in information is provided here as a guide to perform regulator life testing. The burn-in performed by Fairchild is based on the thermal resistance of the regulator package. The power dissipation level is selected so that the junction temperature is near the maximum specified level (150°C for most products). The power level is then determined based on the chosen ambient. In general, burn-in is performed at 25°C ambient without a heat sink but it can also be done with a heat sink or a different ambient.

Fig. 2-3 Ripple Rejection Measurement Circuits

a. For Positive Regulators



b. For Negative Regulators

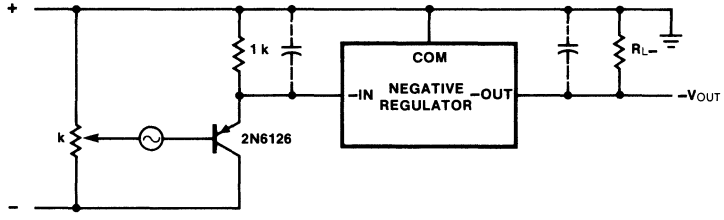
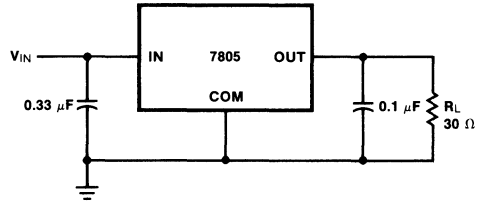


Fig. 2-4 Burn-In Circuit for μA7805 Regulator in TO-220 Package



Example: Determine a burn-in circuit, operating at a 25°C ambient, for a μA7805 in the TO-220 package. From the data sheet:

$$\theta_{JA} = 65°C/W \text{ max}$$

$$P_D = \frac{T_J(\text{max}) - T_A}{\theta_{JA}} = \frac{150 - 25}{65} = 1.92 \text{ W}$$

If $R_L = 30\ \Omega$ and the effects of I_Q are neglected,

$$P_D = (V_{IN} - V_{OUT}) \frac{V_{OUT}}{R_L}$$

or

$$V_{IN} = P_D \frac{R_L}{V_{OUT}} + V_{OUT} = 16.5 \text{ V}$$

If the same circuit is used at an ambient of 125°C,

$$V_{IN} = P_D \frac{R_L}{V_{OUT}} + V_{OUT}$$

$$= \frac{150-125}{65} \times \frac{30}{5} + 5$$

$$= 7.3 \text{ V}$$

Note that the value of the load resistor chosen here (30 Ω) is arbitrary. Any other value giving output currents within the rating of the device could be used. If the burn-in is to be performed at more than one temperature, selecting a common load resistor for all temperatures and changing the input voltage to give the required power dissipations simplifies the design and construction of the burn-in fixtures.

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Thermal Considerations

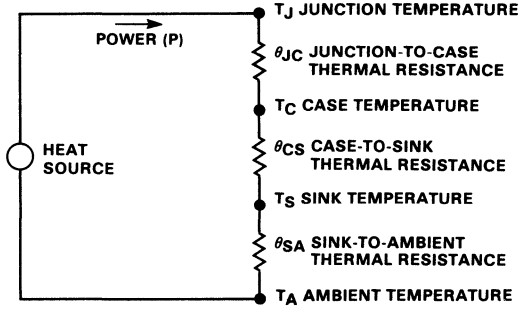
To fully utilize the various available regulator packages, sufficient attention must be paid to proper heat removal. For efficient thermal management, the user must rely on important parameters supplied by the manufacturer, such as junction-to-case and junction-to-ambient thermal resistance and maximum operating junction temperature. The device temperature depends on the power dissipation level, the means for removing the heat generated by this power dissipation and the temperature of the body (heat sink) to which this heat is removed.

Figure 6-1 shows a simplified equivalent circuit for a typical semiconductor device in equilibrium. The power dissipation, which is analogous to current flow in electrical terms, is caused by a heat source similar to a voltage source. Temperature is analogous to voltage potential and thermal resistance to ohmic resistance. Extending the analogy of Ohm's law to

$$\theta_{JA(tot)} = \theta_{JC} + \theta_{CS} + \theta_{SA} = \frac{T_J - T_A}{P_D}$$

Thermal resistance, then, is the rise in the temperature of a package above some reference level per unit of power dissipation in that package, usually expressed in degrees centigrade per watt. The reference temperature may be ambient or it may be the temperature of a heat sink to which the package is connected. There are several factors that affect thermal resistance including die size, the size of the heat source on the die (series-pass transistor in an IC regulator), die-attach material and thickness, leadframe material, construction and thickness.

Fig. 6-1. Simplified Thermal Circuit



Thermal Evaluation Of Regulators

To measure thermal resistance, the difference between the junction temperature and the chosen reference temperature, case, sink or ambient, must be determined. Ambient or sink temperature measurement is straightforward. For case-temperature measurement, the device should have a sufficiently large heat sink and the power level should be close to the specified rating of the package-die combination. The case or tab temperature can be measured by an infrared microradiometer or by using a thermocouple soldered to a point in the center of the case or tab at the tab-heat-sink interface as close to the die as practical.

Measurement of the junction temperature, unfortunately, is not as simple and involves some calibrations. There are several methods available for junction-temperature measurement; the two most commonly used are described here.

Thermal Shutdown Method

With this method, the thermal shutdown temperature of each device is used as the thermometer in determining the thermal resistance. The device is first heated externally, with as little internal power dissipation as practical, until it reaches thermal shutdown. Then, with the device mounted on a heat sink, the regulator is powered externally until it reaches thermal shutdown again. With some packages, the ambient of the device and its heat sink may have to be elevated sufficiently to force the regulator into shutdown. The thermal resistance of the device can then be calculated by using

$$\theta_{JC} = \frac{T_J - T_C}{P_D}$$

where θ_{JC} is the junction-to-case thermal resistance
T_J is the measured thermal shutdown temperature
T_C is the measured case temperature
P_D is the power dissipated to force the device into shutdown and is equal to

$$(V_{IN} - V_{OUT})\, I_{OUT} + V_{IN}\, I_Q$$

I_Q is the quiescent current of the device and can be neglected for low thermal resistance packages such as the TO-3 and TO-220.

Substrate or Isolation Diode Method
The second method of thermal-resistance measurement utilizes the isolation diodes within the integrated circuits as temperature sensing element*. Under normal operating conditions, the substrate diodes are reverse biased and separate or "isolate" active as well as passive components within an integrated circuit. (See *Figure 6-2*). When the regulator is reverse biased and a constant current is forced through the device between the input terminal and ground, the substrate diodes become forward biased; naturally, when the forward drop is measured, the diode with the highest temperature (lowest forward drop) is detected. Measurement of the thermal resistance of the regulator then involves two steps:

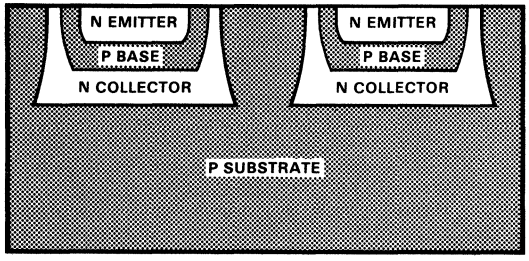
Calibrating the substrate diode at a fixed I_{SUBS} level in an oven or bath at two temperatures, preferably near the device operating junction temperature. It is assumed that this voltage drop changes linearly with temperature.

*For more detailed explanation of this method, see Fairchild Application Note 205, "Thermal Evaluation of Integrated Circuits". For μA723 thermal considerations, see page 3-29.

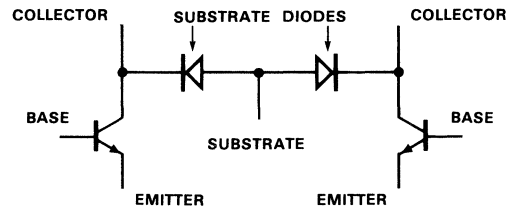
Measuring the junction temperature. The device is powered through a switching circuit S1 at a duty cycle greater than 99% (*Figure 6-3*); thus the device is electrically heated until it reaches equilibrium. During short measuring intervals (< 1% duty cycle), the switching circuit de-energizes the device and the forward drop of the substrate diode is measured at the previously calibrated I_{SUBS} current level. This voltage drop must be measured as soon as possible (several microseconds) after the removal of the power pulse to avoid inaccurate readings due to cooling of the chip. Diode D1 prevents reverse current from flowing through the load resistor R_L during the substrate-diode measuring interval. Since the change in the isolation diode drop is assumed to be linear with temperature, the measured voltage drop can be converted to its corresponding junction temperature by interpolation or extrapolation. Thermal resistance can then be calculated by the same formula used in the thermal-shutdown method.

Heat Sink Requirements
When is a heat sink necessary, and what type of a heat sink should one use? The answers to these questions depend on reliability and cost requirements. Heat sinking is necessary to keep the operating junction temperature T_J of the regulator below the

Fig. 6-2 Monolithic Transistor Isolation

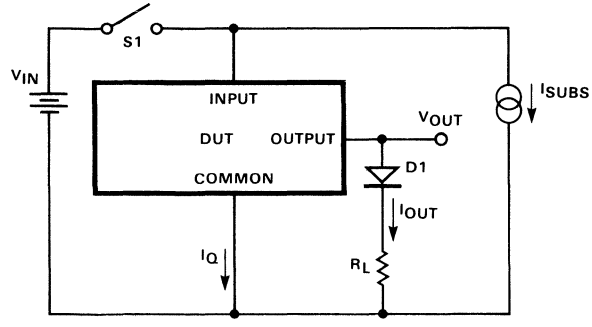


Cross-sectional Diagram Showing Two Monolithic Transistors Isolated by Substrate Diodes



Equivalent Circuit

Fig. 6-3 Thermal Resistance Measurement Circuit Using Substrate Diode Technique



specified maximum value. Since semiconductor reliability improves as operating junction temperature is lowered, a reliability/cost compromise is usually made in the device design.

Table 6-1 is a tabulation by package of the various regulators available from Fairchild. It also lists the average and maximum values of thermal resistance for the regulator chip-package combinations and can be used as a guide in selecting a suitable package when designing a regulator circuit.

Thermal characteristics of voltage-regulator chips and packages determine that some form of heat sinking is mandatory whenever the power dissipation exceeds the following.

0.67 W for the TO-39 package
0.69 W for the TO-92 package
1.56 W for the Mini Batwing and Power Watt (similar to TO-202) packages
1.8 W for the TO-220 package
2.8 W for the TO-3 package

at 25°C ambient or lower power levels at ambients above 25°C.

To choose or design a heat sink, the designer must determine the following regulator parameters.

$P_{D(max)}$—Maximum power dissipation: $(V_{IN} - V_{OUT})$ $I_{OUT} + V_{IN} I_Q$
$T_{A(max)}$—Maximum ambient temperature the regulator will encounter during operation.
$T_{J(max)}$—Maximum operating junction temperature, specified by the manufacturer.
θ_{JC}, θ_{JA}—Junction-to-case and junction-to-ambient thermal resistance values, also specified by the regulator manufacturer.
θ_{CS}—Case-to-heat-sink thermal resistance which, for large packages, can range from about 0.2°C/W to about 1°C/W depending on the quality of the contact between the package and the heat sink.
θ_{SA}—Heat-sink-to-ambient thermal resistance, specified by heat-sink manufacturer.

Maximum permissible dissipation without a heat sink is determined by

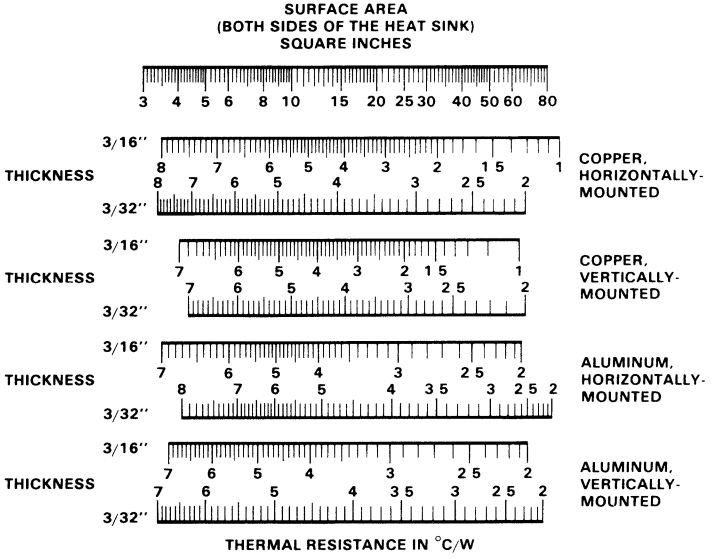
$$P_{D(max)} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}}$$

If the device dissipation P_D exceeds this figure, a heat sink is necessary. The total required thermal resistance may then be calculated.

$$\theta_{JA(tot)} = \theta_{JC} + \theta_{CS} + \theta_{SA} = \frac{T_{J(max)} - T_{A(max)}}{P_D}$$

Case-to-sink and sink-to-ambient thermal resistance information on commercially available heat sinks is normally provided by the heat sink manufacturer. A summary of some commercially available heat sinks is shown in *Table 6-2*. However, if a chassis or other conventional surface is used as a heat sink, *Figure 6-4* can be used as a guide to estimate the required surface area.

Fig. 6-4 Heat Sink Material Selection Guide



To determine either area required or thermal resistance of a given area, draw a vertical line between the top (or area) line down to the material of interest.

Table 6-1 Thermal Resistance (θ_{JC}, θ_{JA}) By Device and Package*

Resistances Listed as Follows:
θ_{JC} (TYP) θ_{JC} (MAX) in °C/W
θ_{JA} (TYP) θ_{JA} (MAX)

Reg. Type	Device No./Series	I_{OUT} (A)	TO-3 K	4-Lead TO-3 K	TO-220 U	Power Watt U1*	TO-39 H
Pos. 3-Term	μA78LXX	0.1					20 40 140 190
	μA78MXX	0.5			3.0 5.0 62 70		18 25 120 185
	μA109, μA209 μA309, 5 V	1	3.5 5.5 40 45				
	μA78XX	1	3.5 5.5 40 45		3.0 5.0 60 65		
	78H05, 5 V	5	1.5 2.0 37 40				
	μA78HXX	5	2.0 2.5 32 38				
Neg. 3-Term	μA79MXX	0.5			3.0 5.0 62 70		18 25 120 185
	μA79XX	1	3.5 5.5 40 45		3.0 5.0 60 65		
Pos. Adj.	μA105/ 305/376	0.012 to 0.045					
	μA723	0.125					
	μA78MG 4-TERM	0.5				6 8 75 80	
	μA78G 4-TERM	1		4.0 6.0 44 47		6 8 75 80	
	μA78HG	5	2.0 2.5 32 38				
Neg. Adj.	μA79MG 4-TERM.	0.5				6 8 75 80	
	μA79G 4-TERM.	1		4.0 6.0 44 47		6 8 75 80	

Note
*Similar to TO-202

4-Lead TO-39 H	TO-92 W	TO-99 8-Lead TO-5 H	TO-100 10-Lead TO-5 H	TO-116 14-Pin Plastic D	TO-116 14-Pin Ceramic D	8 Pin Minidip T
	- - 160 180					
		25 40 150 190				- - 160 190
			25 50 150 190	- - 150 190	- - 125 160	
18 25 125 185						
18 25 125 185						

How to Choose a Heat Sink—Example
Determine the heat sink required for a regulator which has the following system requirements:

Operating ambient temperature range: 0°C–60°C
Maximum junction temperature: 125°C
Maximum output current: 800 mA
Maximum input to output differential: 10 V

From *Table 6-1,* the choice is narrowed down to the μA7800 family, available in TO-3 and TO-220 packages. The TO-220 package is sufficent (lower cost, better thermal resistance).

θ_{JC} = 5°C/W maximum (from data sheet or *Table 6-1*)

$$\theta_{JA(tot)} = \theta_{JC} + \theta_{CS} + \theta_{SA} = \frac{T_J - T_A}{PD}$$

$$\theta_{CS} + \theta_{SA} = \frac{125 - 60}{0.8 \times 10} - 5 = 3.13°C/W$$

Assuming θ_{CS} = 0.13°C/W then θ_{SA} = 3°C/W

This thermal resistance value can be achieved by using either 22 square inches of 3/16 inch thick vertically mounted aluminum (*Figure 6-4*) or a commercial heat sink (*Table 6-2*).

Tips for Better Regulator Heat Sinking
Avoid placing heat-dissipating components such as power resistors next to regulators.

When using low dissipation packages such as TO-5, TO-39, and TO-92, keep lead lengths to a minimum and use the largest possible area of the printed board traces or mounting hardware to provide a heat dissipation path for the regulator.

When using larger packages, be sure the heat sink surface is flat and free from ridges or high spots. Check the regulator package for burrs or peened-over corners. Regardless of the smoothness and flatness of the package and heat-sink contact, air pockets between them are unavoidable unless a lubricant is used. Therefore, for good thermal conduction, use a thin layer of thermal lubricant such as Dow Corning DC-340, General Electric 662 or Thermacote by Thermalloy.

In some applications, especially with negative regulators, it is desirable to electrically insulate the regulator case from the heat sink. Hardware kits for this purpose are commercially available for such packages as the TO-3 and TO-220. They generally consist of a 0.003 to 0.005 inch thick piece of mica or bonded fiberglass to electrically isolate the two surfaces, yet provide a thermal path between them. As expected, the thermal resistance will increase but, as in the direct metal-to-metal joint, some improvement can be realized by using thermal lubricant on each side of the mica.

If the regulator is mounted on a heat sink with fins, the most efficient heat transfer takes place when the fin is in a vertical plane, as this type of mounting forces the heat transfer from fin to air in a combination of radiation and convection.

If it is necessary to bend any of the regulator leads, handle them carefully to avoid straining the package. Furthermore, lead bending should be restricted since repeated bending will fatigue and eventually break the leads.

Table 6-2. Heat Sink Selection Guide

This list is only representative. No attempt has been made to provide a complete list of all heat sink manufacturers. All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

θ_{SA} Approx. (°C/W)	Manufacturer and Type
TO-3 Packages	
0.4 (9" length)	Thermalloy (Extruded) 6590 Series
0.4–0.5 (6" length)	Thermalloy (Extruded) 6660, 6560 Series
0.56–3.0	Wakefield 400 Series
0.6 (7.5" length)	Thermalloy (Extruded) 6470 Series
0.7–1.2 (5–5.5" length)	Thermalloy (Extruded) 6423, 6443, 6441, 6450 Series
1.0–5.4 (3" length)	Thermalloy (Extruded) 6427, 6500, 6123, 6401, 6403, 6421, 6463, 6176, 6129, 6141, 6169, 6135, 6442 Series
1.9	IERC E2 Series (Extruded)
2.1	IERC E1, E3 Series (Extruded)
2.3–4.7	Wakefield 600 Series
4.2	IERC HP3 Series
4.5	Staver V3-5-2
4.8–7.5	Thermalloy 6001 Series
5–6	IERC HP3 Series
5–10	Thermalloy 6013 Series
5.6	Staver V3-3-2
5.9–10	Wakefield 680 Series
6	Wakefield 390 Series
6.4	Staver V3-7-224
6.5–7.5	IERC UP Series
8	Staver V1-5

Table 6-2. (Cont.)

θ_{SA} Approx. (°C/W)	Manufacturer and Type
8.1	Staver V3-5
8.8	Staver V3-7-96
9.5	Staver V3-3
9.5-10.5	IERC LA Series
9.8-13.9	Wakefield 630 Series
10	Staver V1-3
11	Thermalloy 6103, 6117 Series
TO-220 Packages (See Note 1)	
4.2	IERC HP3 Series
5-6	IERC HP1 Series
6.4	Staver V3-7-225
6.5-7.5	IERC VP Series
7.1	Thermalloy 6070 Series
8.1	Staver V3-5
8.8	Staver V3-7-96
9.5	Staver V3-3
10	Thermalloy 6032, 6034 Series
12.5-14.2	Staver V4-3-192
13	Staver V5-1
15	Thermalloy 6030 Series
15.1-17.2	Staver V4-3-128
16	Thermalloy 6072, 6106 Series
18	Thermalloy 6038, 6107 Series
19	IERC PB Series
20	Staver V6-2
20	Thermalloy 6025 Series
25	IERC PA Series
TO-92 Packages	
30	Staver F2-7
46	Staver F5-7A, F5-8-1
50	IERC RUR Series
57	Staver F5-7D
65-5	IERC RU Series
72	Staver F1-7
85	Thermalloy 2224 Series
Mini Batwing	
10	Thermalloy 6069 Series
10.6	Thermalloy 6068 Series
11.7	Thermalloy 6067 Series
13	Thermalloy 6066 Series
20	Thermalloy 6062 Series
26	Thermalloy 6064 Series

θ_{SA} Approx. (°C/W)	Manufacturer and Type
TO-5 and TO-39 Packages	
12	Thermalloy 1101, 1103 Series
12-16	Wakefield 260-5 Series
15	Staver V3A-5
22	Thermalloy 1116, 1121, 1123 Series
22	Thermalloy 1130, 1131, 1132 Series
24	Staver F5-5C
25	Thermalloy 2227 Series
26-30	IERC Thermal Links
27-83	Wakefield 200 Series
28	Staver F5-5B
34	Thermalloy 2228 Series
35	IERC Clip Mount Thermal Link
39	Thermalloy 2215 Series
41	Thermalloy 2205 Series
42	Staver F5-5A
42-65	Wakefield 296 Series
46	Staver F6-5, F6-5L
50	Thermalloy 2225 Series
50-55	IERC Fan Tops
53	Thermalloy 2211 Series
55	Thermalloy 2210 Series
56	Thermalloy 1129 Series
58	Thermalloy 2230, 2235 Series
60	Thermalloy 2226 Series
68	Staver F1-5
72	Thermalloy 1115 Series
Power Watt (similar to TO-202) **Packages** (See Note 2)	
12.5-14.2	Staver V4-3-192
13	Thermalloy 6063 Series
13	Staver V5-1
15.1-17.2	Staver V4-3-128
19	Thermalloy 6106 Series
20	Staver V6-2
24	Thermalloy 6047 Series
25	Thermalloy 6107 Series
37	IERC PA1-7CB with PVC-1B Clip
40-42	Staver F7-3
40-43	Staver F7-2
42	IERC PA2-7CB with PVC-1B Clip
42-44	Staver F7-1

Notes

1. Most TO-3 heat sinks can also be used with TO-220 packages with appropriate hole patterns.
2. Most TO-220 heat sinks can be used with the Power Watt package.

IERC: 135 W. Magnolia Blvd., Burbank, CA 91502
Staver Co., Inc.: 41-51 N. Saxon Ave., Bay Shore, N.Y. 11706

Thermalloy Inc.: 2021 W. Valley View Lane, Dallas, TX 75234
Wakefield Engineering, Inc.: Audubon Rd., Wakefield, MA 01880

FAIRCHILD
A Schlumberger Company

μA7800 Series 3-Terminal Positive Voltage Regulators

Linear Products

Description

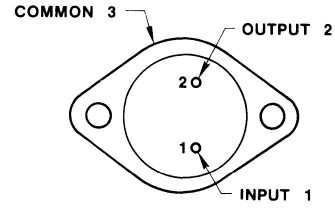
The μA7800 series of monolithic 3-Terminal Positive Voltage Regulators is constructed using the Fairchild Planar epitaxial process. These regulators employ internal current-limiting, thermal-shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1 A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- **OUTPUT CURRENT IN EXCESS OF 1 A**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**
- **AVAILABLE IN THE TO-220 AND THE TO-3 PACKAGE**
- **OUTPUT VOLTAGES OF 5, 6, 8, 8.5, 12, 15, 18, AND 24 V**

Absolute Maximum Ratings

Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	
μA7800	−55°C to +150°C
μA7800C	0°C to +125°C
Pin Temperature	
Soldering, 60s time limit	
TO-3 Package	300°C
Soldering, 10s time limit	
TO-220 Package	230°C

Connection Diagram
TO-3 Package

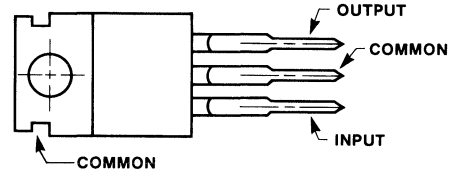


(Top View)

Order Information

Type	Package	Code	Part No.
μA7805	Metal	HJ	μA7805KM
μA7806	Metal	HJ	μA7806KM
μA7808	Metal	HJ	μA7808KM
μA7812	Metal	HJ	μA7812KM
μA7815	Metal	HJ	μA7815KM
μA7818	Metal	HJ	μA7818KM
μA7824	Metal	HJ	μA7824KM
μA7805C	Metal	HJ	μA7805KC
μA7806C	Metal	HJ	μA7806KC
μA7808C	Metal	HJ	μA7808KC
μA7812C	Metal	HJ	μA7812KC
μA7815C	Metal	HJ	μA7815KC
μA7818C	Metal	HJ	μA7818KC
μA7824C	Metal	HJ	μA7824KC

Connection Diagram
To-220 Package

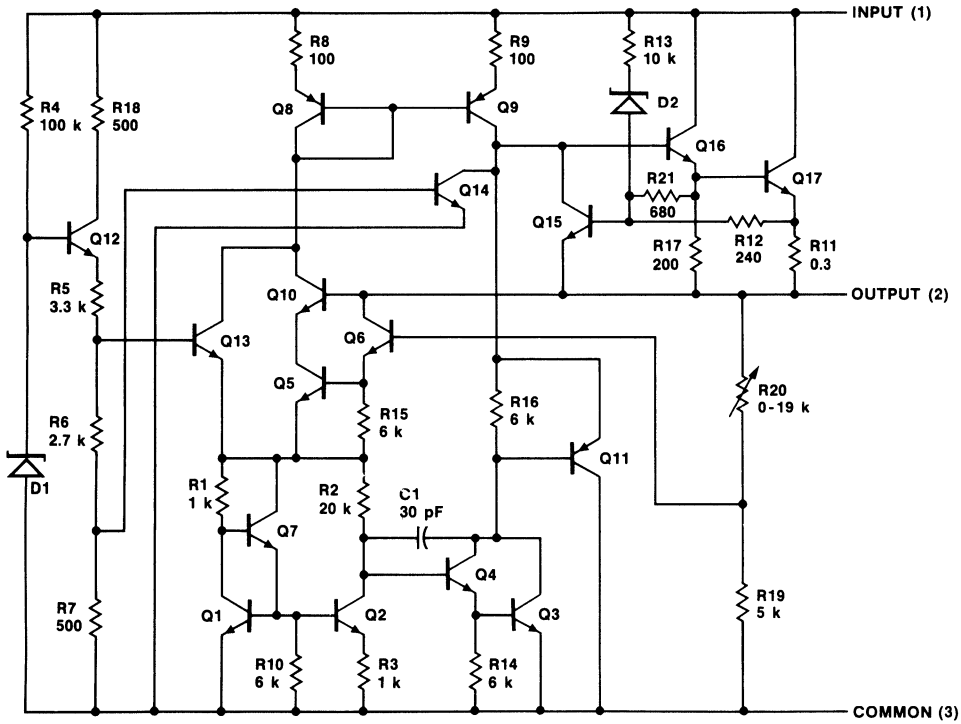


(Side View)

Order Information

Type	Package	Code	Part No.
μA7805C	Molded Power Pack	GH	μA7805UC
μA7806C	Molded Power Pack	GH	μA7806UC
μA7808C	Molded Power Pack	GH	μA7808UC
μA7885C	Molded Power Pack	GH	μA7885UC
μA7812C	Molded Power Pack	GH	μA7812UC
μA7815C	Molded Power Pack	GH	μA7815UC
μA7818C	Molded Power Pack	GH	μA7818UC
μA7824C	Molded Power Pack	GH	μA7824UC

Equivalent Circuit



μA7805

Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V		3	50	mV
			8 V ≤ V_{IN} ≤ 12 V		1	25	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5	25	mV
Output Voltage		8.0 V ≤ V_{IN} ≤ 20 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		4.65		5.35	V
Quiescent Current		T_J = 25°C			4.2	6.0	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 25 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V		68	78		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0	2.5	V
Output Resistance		f = 1 kHz			17		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			0.75	1.2	A
Peak Output Current		T_J = 25°C		1.3	2.2	3.3	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55° C ≤ T_J ≤ +25°C			0.4	mV/°C/ V_{OUT}
			+25°C ≤ T_J ≤ +150°C			0.3	

μA7805C

Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V		3	100	mV
			8 V ≤V_{IN} ≤ 12 V		1	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
Output Voltage		7 V ≤ V_{IN} ≤ 20 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		4.75		5.25	V
Quiescent Current		T_J = 25°C			4.2	8.0	mA
Quiescent Current Change	with line	7 V ≤ V_{IN} ≤ 25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V		62	78		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			17		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			750		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			1.1		mV/°C

μA7806C
Electrical Characteristics V_{IN} = 11 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		5.75	6.0	6.25	V
Line Regulation		T_J = 25°C	8 V ≤ V_{IN} ≤ 25 V		5	120	mV
			9 V ≤ V_{IN} ≤ 13 V		1.5	60	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		14	120	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	60	mV
Output Voltage		8 V ≤ V_{IN} ≤ 21 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		5.7		6.3	V
Quiescent Current		T_J = 25°C			4.3	8.0	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 25 V				1.3	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			45		μV
Ripple Rejection		f = 120 Hz, 9 V ≤ V_{IN} ≤ 19 V		59	75		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			19		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			550		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			0.8		mV/°C

Note
1. For all tables, all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA7808

Electrical Characteristics V_{IN} = 14 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	80	mV
			11 V ≤ V_{IN} ≤ 17 V		2.0	40	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	100	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	40	mV
Output Voltage		11.5 V ≤ V_{IN} ≤ 23 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		7.6		8.4	V
Quiescent Current		T_J = 25°C			4.3	6.0	mA
Quiescent Current Change	with line	11.5 V ≤ V_{IN} ≤ 25 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		62	72		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0	2.5	V
Output Resistance		f = 1 kHz			16		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			0.75	1.2	A
Peak Output Current		T_J = 25°C		1.3	2.2	3.3	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55°C ≤ T_J ≤ +25°C			0.4	mV/°C/V_{OUT}
			+25°C ≤ T_J ≤ 150°C			0.3	

μA7808C

Electrical Characteristics V_{IN} = 14 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	160	mV
			11 V ≤ V_{IN} ≤ 17 V		2.0	80	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	160	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	80	mV
Output Voltage		10.5 V ≤ V_{IN} ≤ 23 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		7.6		8.4	V
Quiescent Current		T_J = 25°C			4.3	8.0	mA
Quiescent Current Change	with line	10.5 V ≤ V_{IN} ≤ 25 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			52		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		56	72		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			16		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			450		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			0.8		mV/°C

μA7885C
Electrical Characteristics V_{IN} = 15 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		8.15	8.5	8.85	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	170	mV
			11 V ≤ V_{IN} ≤ 17 V		2.0	85	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	170	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	85	mV
Output Voltage		11 V ≤ V_{IN} ≤ 23.5 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		8.1		8.9	V
Quiescent Current		T_J = 25°C			4.3	8.0	mA
Quiescent Current Change	with line	10.5 V ≤ V_{IN} ≤ 25 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			55		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		56	70		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			16		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			450		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			0.8		mV/°C

Note
1 For all tables, all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately

μA7812

Electrical Characteristics V_{IN} = 19 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		11.5	12.0	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V		10	120	mV
			16 V ≤ V_{IN} ≤ 22 V		3.0	60	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	120	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	60	mV
Output Voltage		15.5 V ≤ V_{IN} ≤ 27 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.3	6.0	mA
Quiescent Current Change	with line	15 V ≤ V_{IN} ≤ 30 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V		61	71		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0	2.5	V
Output Resistance		f = 1 kHz			18		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			0.75	1.2	A
Peak Output Current		T_J = 25°C		1.3	2.2	3.3	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55°C ≤ T_J ≤ +25°C			0.4	mV/°C/V_{OUT}
			+25°C ≤ T_J ≤ 150°C			0.3	

μA7812C

Electrical Characteristics V_{IN} = 19 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		11.5	12.0	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V		10	240	mV
			16 V ≤ V_{IN} ≤ 22 V		3.0	120	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	240	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	120	mV
Output Voltage		14.5 V ≤ V_{IN} ≤ 27 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.3	8.0	mA
Quiescent Current Change	with line	14.5 V ≤ V_{IN} ≤ 30 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			75		μV
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V		55	71		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			18		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			350		mA
Peak Output Current		T_J = 25°C			2.2		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C			1.0		mV/°C

μA7815
Electrical Characteristics V_{IN} = 23 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		14.4	15.0	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V		11	150	mV
			20 V ≤ V_{IN} ≤ 26 V		3	75	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	150	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	75	mV
Output Voltage		18.5 V ≤ V_{IN} ≤ 30 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		14.25		15.75	V
Quiescent Current		T_J = 25°C			4.4	6.0	mA
Quiescent Current Change	with line	18.5 V ≤ V_{IN} ≤ 30 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V		60	70		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0	2.5	V
Output Resistance		f = 1 kHz			19		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			0.75		A
Peak Output Current		T_J = 25°C		1.3	2.2	3.3	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55° C ≤ T_J ≤ +25°C			0.4	mV/°C/ V_{OUT}
			+25°C ≤ T_J ≤ +150°C			0.3	

μA7815C
Electrical Characteristics V_{IN} = 23 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		14.4	15.0	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V		11	300	mV
			20 V ≤ V_{IN} ≤ 26 V		3	150	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	300	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	150	mV
Output Voltage		17.5 V ≤ V_{IN} ≤ 30 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		14.25		15.75	V
Quiescent Current		T_J = 25°C			4.4	8.0	mA
Quiescent Current Change	with line	17.5 V ≤ V_{IN} ≤ 30 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			90		μV
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V		54	70		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			19		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			230		A
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤125°C			1.0		mV/°C

μA7818

Electrical Characteristics V_{IN} = 27 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		17.3	18.0	18.7	V
Line Regulation		T_J = 25°C	21 V ≤ V_{IN} ≤ 33 V		15	180	mV
			24 V ≤ V_{IN} ≤ 30 V		5.0	90	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	180	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	90	mV
Output Voltage		22 V ≤ V_{IN} ≤ 33 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		17.1		18.9	V
Quiescent Current		T_J = 25°C			4.5	6.0	mA
Quiescent Current Change	with line	22 V ≤ V_{IN} ≤ 33 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 22 V ≤ V_{IN} ≤ 32 V		59	69		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			22	2.5	mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			0.75	1.2	A
Peak Output Current		T_J = 25°C		1.3	2.2	3.3	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	+25° C ≤ T_J ≤ +150°C			0.4	mV/°C/ V_{OUT}
			−55°C ≤ T_J ≤ +25°C			0.3	

μA7818C

Electrical Characteristics V_{IN} = 27 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		17.3	18.0	18.7	V
Line Regulation		T_J = 25°C	21 V ≤ V_{IN} ≤ 33 V		15	360	mV
			24 V ≤ V_{IN} ≤ 30 V		5.0	180	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	360	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	180	mV
Output Voltage		21 V ≤ V_{IN} ≤ 33 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		17.1		18.9	V
Quiescent Current		T_J = 25°C			4.5	8.0	mA
Quiescent Current Change	with line	21 V ≤ V_{IN} ≤ 33 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			110		μV
Ripple Rejection		f = 120 Hz, 22 V ≤ V_{IN} ≤ 32 V		53	69		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			22		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			200		mA
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤125°C			1.0		mV/°C

μA7824
Electrical Characteristics V_{IN} = 33 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

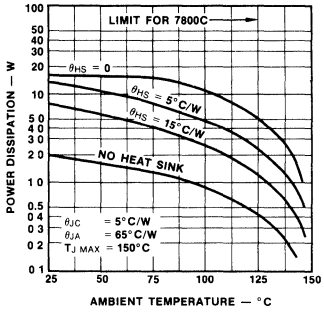
Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		23.0	24.0	25.0	V
Line Regulation		T_J = 25°C	27 V ≤ V_{IN} ≤ 38 V		18	240	mV
			30 V ≤ V_{IN} ≤ 36 V		6	120	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	240	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	120	mV
Output Voltage		28 V ≤ V_{IN} ≤ 38 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		22.8		25.2	V
Quiescent Current		T_J = 25°C			4.6	6.0	mA
Quiescent Current Change	with line	28 V ≤ V_{IN} ≤ 38 V				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V		56	66		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0	2.5	V
Output Resistance		f = 1 kHz			28		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			0.75	1.2	A
Peak Output Current		T_J = 25°C		1.3	2.2	3.3	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55° C ≤ T_J ≤ +25°C			0.4	mV/°C/V_{OUT}
			+25°C ≤ T_J ≤ +150°C			0.3	

μA7824C
Electrical Characteristics V_{IN} = 33 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

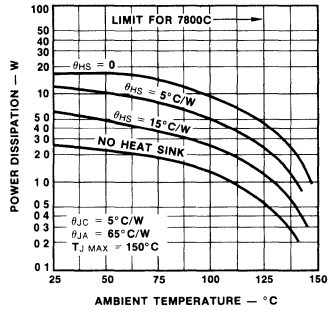
Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		23.0	24.0	25.0	V
Line Regulation		T_J = 25°C	27 V ≤ V_{IN} ≤ 38 V		18	480	mV
			30 V ≤ V_{IN} ≤ 36 V		6	240	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 1.5 A		12	480	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4	240	mV
Output Voltage		27 V ≤ V_{IN} ≤ 38 V 5 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		22.8		25.2	V
Quiescent Current		T_J = 25°C			4.6	8.0	mA
Quiescent Current Change	with line	27 V ≤ V_{IN} ≤ 38 V				1.0	mA
	with load	5 mA ≤ I_{OUT} ≤ 1.0 A				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			170		μV
Ripple Rejection		f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V		50	66		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0		V
Output Resistance		f = 1 kHz			28		mΩ
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			150		mA
Peak Output Current		T_J = 25°C			2.1		A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA, 0°C ≤ T_J ≤125°C			1.5		mV/°C

Typical Performance Curves

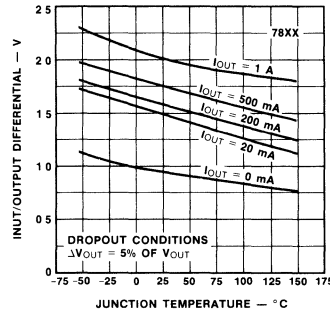
Worst Case Power Dissipation Versus Ambient Temperature (TO-3)



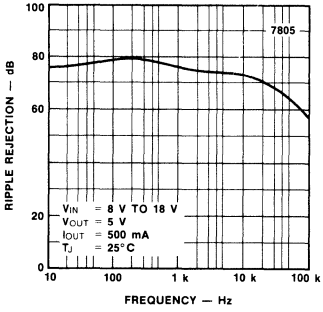
Worst Case Power Dissipation Versus Ambient Temperature (TO-220)



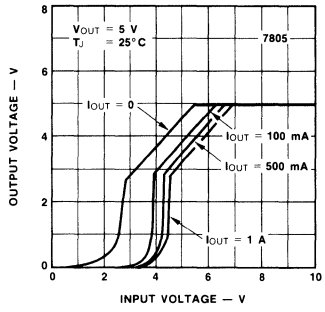
Dropout Voltage as a Function of Junction Temperature



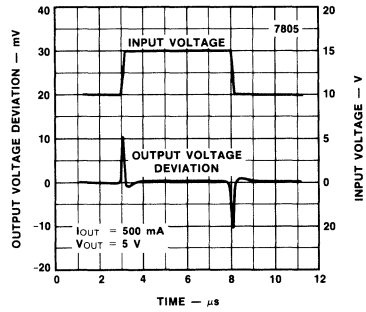
Ripple Rejection as a Function of Frequency



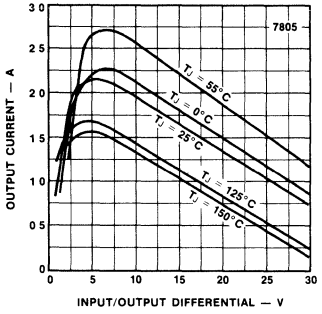
Dropout Characteristics



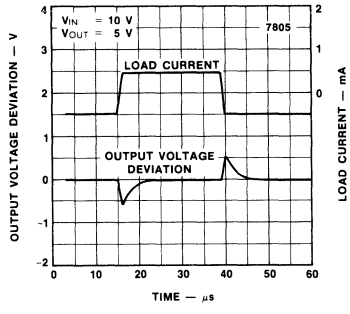
Line Transient Response



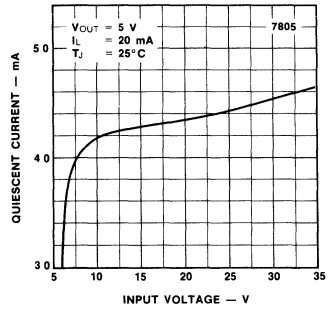
Peak Output Current as a Function of Input/Output Differential Voltage



Load Transient Response

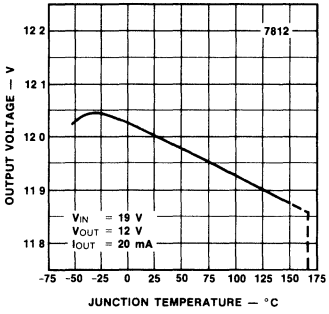


Quiescent Current as a Function of Input Voltage

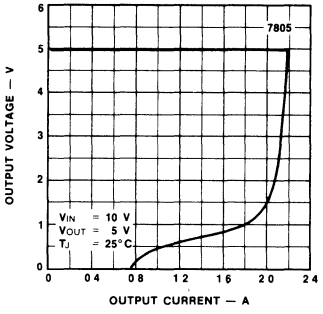


Typical Performance Curves (Cont.)

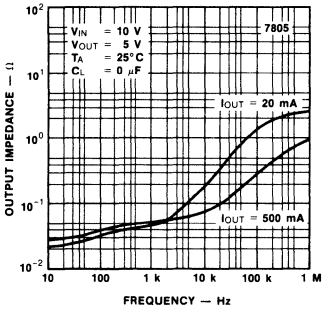
Output Voltage as a Function of Junction Temperature



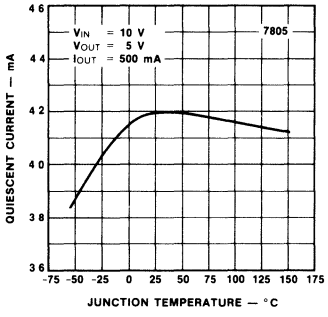
Current Limiting Characteristics



Output Impedance as a Function of Frequency

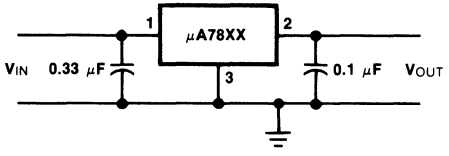


Quiescent Current as a Function of Temperature



Note
The other μA7800 series devices have similar curves.

DC Parameter Test Circuit



Design Considerations

The μA7800 fixed voltage regulator series has thermal-overload protection from excessive power dissipation, internal short circuit protection which limits the regulator's maximum current, and output transistor safe area-compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 7800, 125°C for 7800C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC} °C/W	Max θ_{JC} °C/W	Typ θ_{JA} °C/W	Max θ_{JA} °C/W
TO-3	3.5	5.5	40	45
TO-220	3.0	5.0	60	65

$$P_{D(MAX)} = \frac{T_{J(Max)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J(Max)} - T_A}{\theta_{JA}}$$
(Without heat sink)

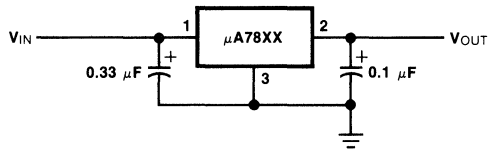
$\theta_{CA} = \theta_{CS} + \theta_{SA}$

solving for T_J: $T_J = T_A + P_D (\theta_{JC} + \theta_{CA})$
or $T_A + P_D\theta_{JA}$ (Without heat sink)

where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-case-thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink to thermal resistance
θ_{SA} = Heat sink-to-ambient thermal resistance
θ_{JA} = Junction-to-ambient thermal resistance

Typical Applications

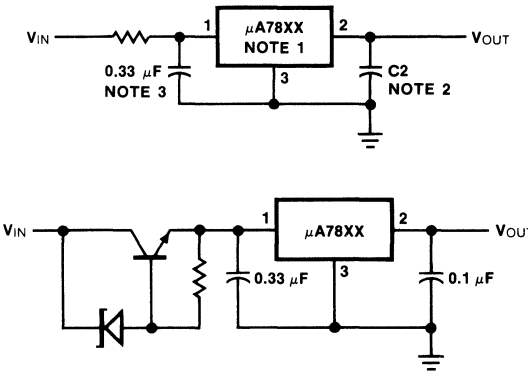
Fixed Output Regulator



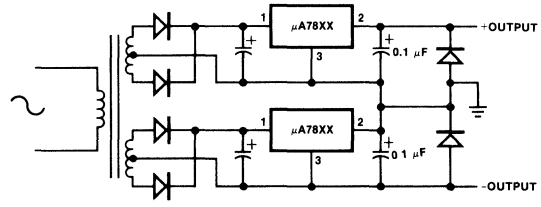
Notes

1. To specify an output voltage, substitute voltage value for "XX."
2. Bypass capacitors are recommended for optimum stability and transient response, and should be located as close as possible to the regulator.

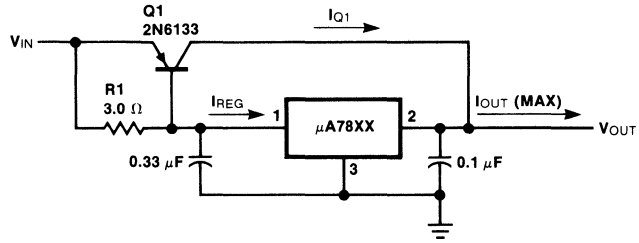
High Input Voltage Circuits



Positive and Negative Regulator



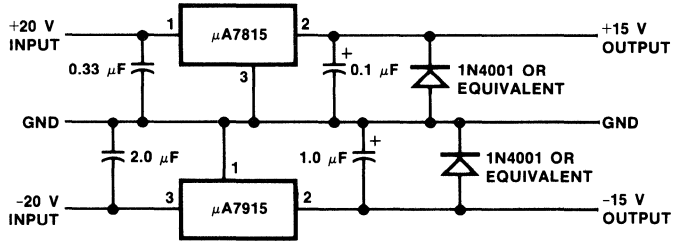
High Current Voltage Regulator



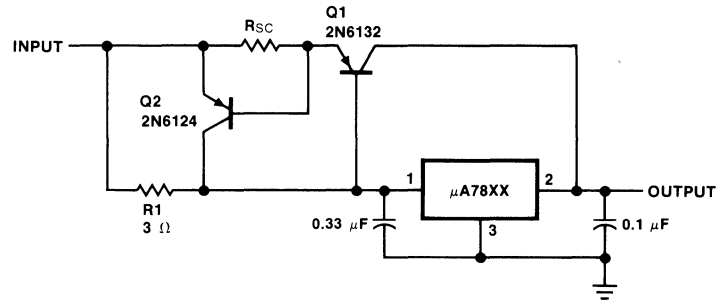
$$\beta(Q1) \geq \frac{I_{OUT(Max)}}{I_{REG(Max)}}$$

$$R1 = \frac{0.9}{I_{REG}} = \frac{\beta(Q1)\, V_{BE(Q1)}}{I_{REG(Max)}\,(\beta + 1) - I_{OUT(Max)}}$$

Dual Supply
Operational Amplifier Supply (± 15 V @ 1.0 A)



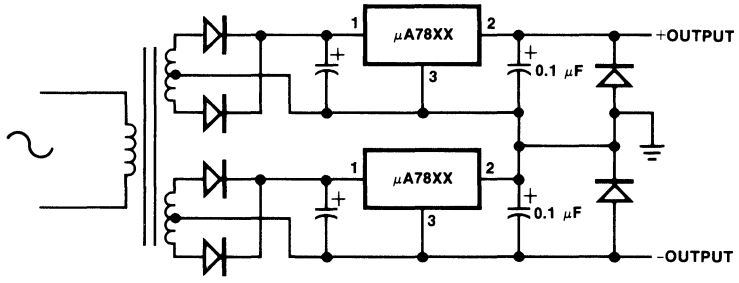
**High Output Current,
Short Circuit Protected**



$$R_{SC} = \frac{0.8}{I_{SC}}$$

$$R1 = \frac{\beta V_{BE(Q1)}}{I_{REG(Max)}\,(\beta + 1) - I_{OUT(Max)}}$$

Positive and Negative Regulator



FAIRCHILD

A Schlumberger Company

μA78M00 Series 3-Terminal Positive Voltage Regulators

Linear Products

Description

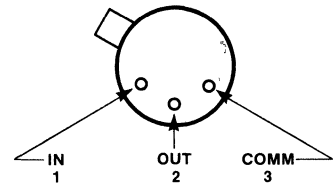
The μA78M00 series of 3-Terminal Medium Current Positive Voltage Regulators is constructed using the Fairchild Planar epitaxial process. These regulators employ internal current-limiting, thermal-shutdown and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver in excess of 500 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- **OUTPUT CURRENT IN EXCESS OF 0.5 A**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL-OVERLOAD PROTECTION**
- **INTERNAL SHORT-CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**
- **AVAILABLE IN JEDEC TO-220 AND TO-39 PACKAGES**
- **OUTPUT VOLTAGES OF 5 V, 6 V, 8 V, 12 V, 15 V, AND 24 V**
- **MILITARY AND COMMERCIAL TEMPERATURE RANGE**

Absolute Maximum Ratings

Input Voltage	
(5 V through 15 V)	35 V
(20 V, 24 V)	40 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
TO-39	−65°C to + 150°C
TO-220	−55°C to + 150°C
Operating Junction Temperature Range	
μA78M00	−55°C to + 150°C
μA78M00C	0°C to + 125°C
Pin Temperatures (Soldering, 60 s time limit)	
TO-39	300°C
(Soldering, 10 s time limit)	
TO-220	230°C

Connection Diagram TO-39 Package

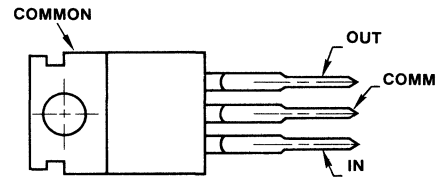


(Top View)

Order Information

Type	Package	Code	Part No.
μA78M05	Metal	FC	μA78M05HM
μA78M06	Metal	FC	μA78M06HM
μA78M08	Metal	FC	μA78M08HM
μA78M12	Metal	FC	μA78M12HM
μA78M15	Metal	FC	μA78M15HM
μA78M24	Metal	FC	μA78M24HM
μA78M05C	Metal	FC	μA78M05HC
μA78M06C	Metal	FC	μA78M06HC
μA78M08C	Metal	FC	μA78M08HC
μA78M12C	Metal	FC	μA78M12HC
μA78M15C	Metal	FC	μA78M15HC

Connection Diagram TO-220 Package

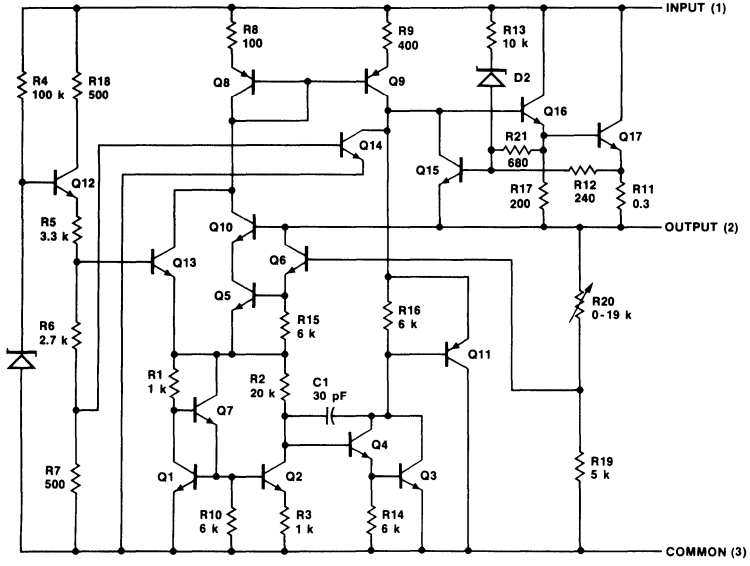


(Side View)

Order Information

Type	Package	Code	Part No.
μA78M05C	Molded Power Pack	GH	μA78M05UC
μA78M06C	Molded Power Pack	GH	μA78M06UC
μA78M08C	Molded Power Pack	GH	μA78M08UC
μA78M12C	Molded Power Pack	GH	μA78M12UC
μA78M15C	Molded Power Pack	GH	μA78M15UC
μA78M24C	Molded Power Pack	GH	μA78M24UC

Equivalent Circuit



μA78M05

Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		3.0	50	mV
			8 V ≤ V_{IN} ≤ 20 V, I_{OUT} = 200 mA		1.0	25	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		20	50	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	25	mV
Output Voltage		8 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 350 mA		4.7		5.3	V
Quiescent Current		T_J = 25°C			4.5	7.0	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V	I_{OUT} = 100 mA	62			dB
			I_{OUT} = 300 mA, T_J = 25°C	62	80		dB
Dropout Voltage		T_A = 25°C, I_{OUT} = 350 mA			2.0	2.5	V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			300	600	mA
Peak Output Current		T_J = 25°C		0.5	0.7	1.4	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55°C ≤ T_J ≤ +25°C			0.4	mV/°C/V_{OUT}
			+25°C ≤ T_J ≤ +150°C			0.3	

Note

All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M05C
Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		3.0	100	mV
			8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		1.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		20	100	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	50	mV
Output Voltage		7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 350 mA		4.75		5.25	V
Quiescent Current		T_J = 25°C			4.5	8.0	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V	I_{OUT} = 100 mA	62			dB
			I_{OUT} = 300 mA, T_J = 25°C	62	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			300		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			1.0		mV/°C

Note
All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M06

Electrical Characteristics V_{IN} = 11 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		5.75	6.0	6.25	V
Line Regulation		T_J = 25°C	8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		5.0	60	mV
			9 V ≤ V_{IN} ≤ 20 V, I_{OUT} = 200 mA		1.5	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		20	60	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	30	mV
Output Voltage		9 V ≤ V_{IN} ≤ 21 V, 5 mA ≤ I_{OUT} ≤ 350 mA		5.7		6.3	V
Quiescent Current		T_J = 25°C			4.5	7.0	mA
Quiescent Current Change	with line	9 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 9 V ≤ V_{IN} ≤ 19 V	I_{OUT} = 100 mA	59			dB
			I_{OUT} = 300 mA, T_J = 25°C	59	80		dB
Dropout Voltage		T_A = 25°C, I_{OUT} = 350 mA			2.0	2.5	V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			300	600	mA
Peak Output Current		T_J = 25°C		0.5	0.7	1.4	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55°C ≤ T_J ≤ +25°C			.4	mV/°C/ V_{OUT}
			+25°C ≤ T_J ≤ +150°C			.3	

Note

All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M06C

Electrical Characteristics V_{IN} = 11 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		5.75	6.0	6.25	V
Line Regulation		T_J = 25°C	8 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		5.0	100	mV
			9 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		1.5	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		20	120	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	60	mV
Output Voltage		8 V ≤ V_{IN} ≤ 21 V, 5 mA ≤ I_{OUT} ≤ 350 mA		5.7		6.3	V
Quiescent Current		T_J = 25°C			4.5	8.0	mA
Quiescent Current Change	with line	9 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			45		μV
Ripple Rejection		f = 120 Hz, 9 V ≤ V_{IN} ≤ 19 V	I_{OUT} = 100 mA	59			dB
			I_{OUT} = 300 mA, T_J = 25°C	59	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			270		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			0.5		mV/°C

Note

All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M08

Electrical Characteristics V_{IN} = 14 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		6.0	60	mV
			11 V ≤ V_{IN} ≤ 20 V, I_{OUT} = 200 mA		2.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	80	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	40	mV
Output Voltage		11.5 V ≤ V_{IN} ≤ 23 V, 5 mA ≤ I_{OUT} ≤ 350 mA		7.6		8.4	V
Quiescent Current		T_J = 25°C			4.6	7.0	mA
Quiescent Current Change	with line	11.5 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V	I_{OUT} = 100 mA	56			dB
			I_{OUT} = 300 mA, T_J = 25°C	56	80		dB
Dropout Voltage		T_A = 25°C, I_{OUT} = 350 mA			2.0	2.5	V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			300	600	mA
Peak Output Current		T_J = 25°C		0.5	0.7	1.4	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55°C ≤ T_J ≤ +25°C			0.4	mV/°C
			+25°C ≤ T_J ≤ +150°C			0.3	

Note

All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M08C

Electrical Characteristics V_{IN} = 14 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		6.0	100	mV
			11 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		2.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	160	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	80	mV
Output Voltage		10.5 V ≤ V_{IN} ≤ 23 V, 5 mA ≤ I_{OUT} ≤ 350 mA		7.6		8.4	V
Quiescent Current		T_J = 25°C			4.6	8.0	mA
Quiescent Current Change	with line	10.5 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			52		μV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V	I_{OUT} = 100 mA	56			dB
			I_{OUT} = 300 mA, T_J = 25°C	56	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			250		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			0.5		mV/°C

Note

All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M12

Electrical Characteristics V_{IN} = 19 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		11.5	12	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		8.0	60	mV
			16 V ≤ V_{IN} ≤ 25 V, I_{OUT} = 200 mA		2.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	120	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	60	mV
Output Voltage		15.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_{OUT} ≤ 350 mA		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.8	7.0	mA
Quiescent Current Change	with line	15 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V	I_{OUT} = 100 mA	55			dB
			I_{OUT} = 300 mA, T_J = 25°C	55	80		dB
Dropout Voltage		T_A = 25°C, I_{OUT} = 350 mA			2.0	2.5	V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			300	600	mA
Peak Output Current		T_J = 25°C		0.5	0.7	1.4	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55°C ≤ T_J ≤ +25°C			0.4	mV/°C/V_{OUT}
			+25°C ≤ T_J ≤ +150°C			0.3	

Note

All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M12C

Electrical Characteristics V_{IN} = 19 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		11.5	12	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		8.0	100	mV
			16 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		2.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	240	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	120	mV
Output Voltage		14.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_{OUT} ≤ 350 mA		11.4		12.6	V
Quiescent Current		T_J = 25°C			4.8	8.0	mA
Quiescent Current Change	with line	14.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			75		μV
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V	I_{OUT} = 100 mA	55			dB
			I_{OUT} = 300 mA, T_J = 25°C	55	80		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			1.0		mV/°C

Note

All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M15
Electrical Characteristics V_{IN} = 23 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		14.4	15	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		10	60	mV
			20 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		3.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	150	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	75	mV
Output Voltage		18.5 V ≤ V_{IN} ≤ 30 V, 5 mA ≤ I_{OUT} ≤ 350 mA		14.25		15.75	V
Quiescent Current		T_J = 25°C			4.8	7.0	mA
Quiescent Current Change	with line	18.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V	I_{OUT} = 100 mA	54			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	70		dB
Dropout Voltage		T_A = 25°C			2.0	2.5	V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			300	600	mA
Peak Output Current		T_J = 25°C		0.5	0.7	1.4	A
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55°C ≤ T_J ≤ +25°C			0.4	mV/°C
			+25°C ≤ T_J ≤ +150°C			0.3	V_{OUT}

Note
All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M15C
Electrical Characteristics V_{IN} = 23 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		14.4	15	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		10	100	mV
			20 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA		3.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		25	300	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	150	mV
Output Voltage		17.5 V ≤ V_{IN} ≤ 30 V, 5 mA ≤ I_{OUT} ≤ 350 mA		14.25		15.75	V
Quiescent Current		T_J = 25°C			4.8	8.0	mA
Quiescent Current Change	with line	17.5 V ≤ V_{IN} ≤ 30 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			90		μV
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V	I_{OUT} = 100 mA	54			dB
			I_{OUT} = 300 mA, T_J = 25°C	54	70		dB
Dropout Voltage		T_A = 25°C			2.0		V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			1.0		mV/°C

Note
All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA78M24
Electrical Characteristics V_{IN} = 33 V, I_{OUT} = 350 mA, −55°C ≤ T_J ≤ 150°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		23	24	25	V
Line Regulation		T_J = 25°C	27 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA		10	60	mV
			30 V ≤ V_{IN} ≤ 36 V, I_{OUT} = 200 mA		5.0	30	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		30	240	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	120	mV
Output Voltage		28 V ≤ V_{IN} ≤ 38 V, 5 mA ≤ I_{OUT} ≤ 350 mA		22.8		25.2	V
Quiescent Current		T_J = 25°C			5.0	7.0	mA
Quiescent Current Change	with line	28 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8	40	μV/V_{OUT}
Ripple Rejection		f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	50	70		dB
Dropout Voltage		T_A = 25°C, I_{OUT} = 350 mA			2.0	2.5	V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			300	600	mA
Peak Output Current		T_J = 25°C		0.5	0.7	1.4	mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA	−55°C ≤ T_J ≤ +25°C			0.4	mV/°C V_{OUT}
			+25°C ≤ T_J ≤ +150°C			0.3	

Note
All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

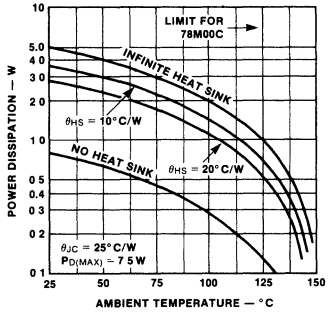
μA78M24C
Electrical Characteristics V_{IN} = 33 V, I_{OUT} = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		23	24	25	V
Line Regulation		T_J = 25°C	27 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA		10	100	mV
			28 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA		5.0	50	mV
Load Regulation		T_J = 25°C	5 mA ≤ I_{OUT} ≤ 500 mA		30	480	mV
			5 mA ≤ I_{OUT} ≤ 200 mA		10	240	mV
Output Voltage		27 V ≤ V_{IN} ≤ 38 V, 5 mA ≤ I_{OUT} ≤ 350 mA		22.8		25.2	V
Quiescent Current		T_J = 25°C			5.0	8.0	mA
Quiescent Current Change	with line	27 V ≤ V_{IN} ≤ 38 V, I_{OUT} = 200 mA				0.8	mA
	with load	5 mA ≤ I_{OUT} ≤ 350 mA				0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			170		μV
Ripple Rejection		f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V	I_{OUT} = 100 mA	50			dB
			I_{OUT} = 300 mA, T_J = 25°C	50	70		dB
Dropout Voltage		T_A = 25°C, I_{OUT} = 350 mA			2.0		V
Short-Circuit Current		T_J = 25°C, V_{IN} = 35 V			240		mA
Peak Output Current		T_J = 25°C			700		mA
Average Temperature Coefficient of Output Voltage		I_{OUT} = 5 mA			1.2		mV/°C

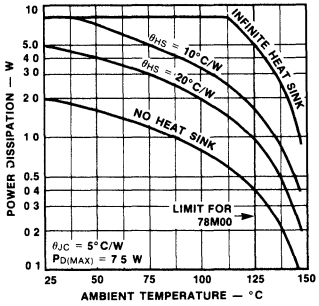
Note
All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Curves

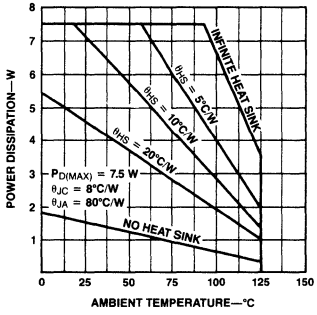
Worst Case Power Dissipation Versus Ambient Temperature TO-39



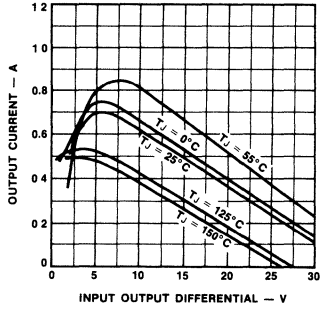
Worst Case Power Dissipation Versus Ambient Temperature TO-220



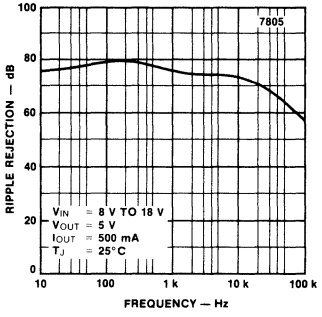
Power Watt (UIC) Worst Case Power Dissipation Versus Ambient Temperature



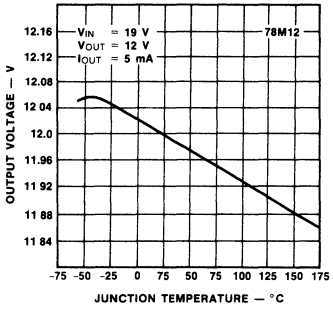
Peak Output Current as a Function of Input-Output Differential Voltage



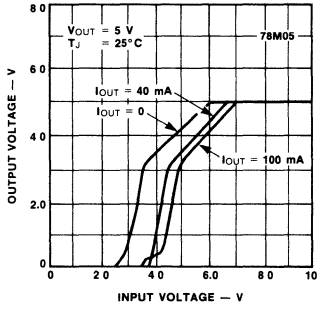
Ripple Rejection as a Function of Frequency



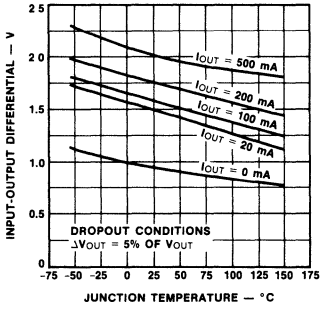
Output Voltage as a Function of Junction Temperature



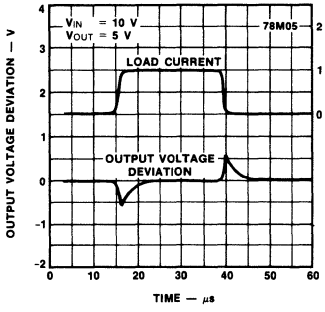
Dropout Characteristics



Dropout Voltage as a Function of Junction Temperature



Load Transient Response

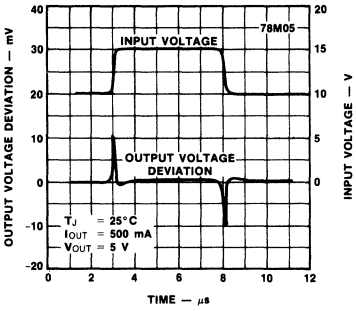


Note

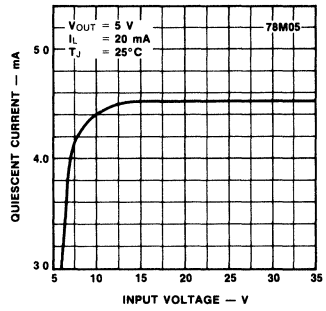
Other μA78M00 Series devices have similar curves.

Typical Performance Curves (Cont.)

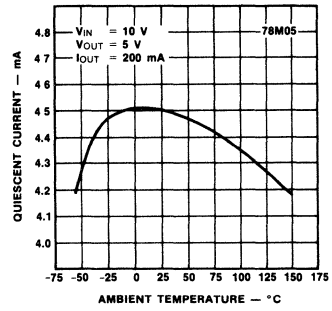
Line Transient Response



Quiescant Current as a Function of Input Voltage



Quiescent Current as a Function of Temperature



Design Considerations

The μA78M00 fixed voltage regulator series has thermal-overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output short circuit current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 78M00, 125°C for 78M00C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θJC	Max θJC	Typ θJA	Max θJA
TO-39	18	25	120	160
TO-220	3	5	60	65
Power Watt	6	8	70	75

$$P_{D\,(MAX)} = \frac{T_{J\,(Max)} - T_A}{\theta_{JC} + \theta_{CA}} \quad \text{or}$$

$$\frac{T_{J\,(Max)} - T_A}{\theta J_A} \quad \text{(Without a heat sink)}$$

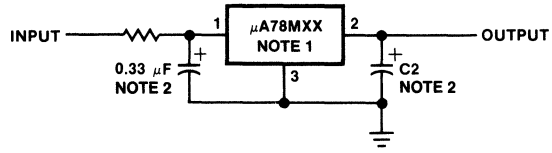
$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J: $T_J = T_A + P_D\,(\theta_{JC}+\theta_{CA})$ or $T_A + P_D\,\theta_{JA}$ (Without a heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink to resistance
θ_{SA} = Heat sink-to-ambient thermal resistance
θ_{JA} = Junction-to-ambient thermal resistance

Typical Applications

Fixed Output Regulator



Notes

1. To specify an output voltage, substitute voltage value for "XX".
2. Bypass Capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

FAIRCHILD

A Schlumberger Company

μA78L00 Series 3-Terminal Positive Voltage Regulators

Linear Products

Description

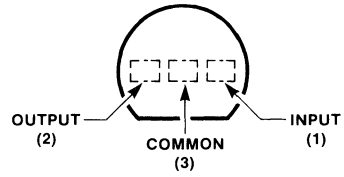
The μA78L00 series of 3-Terminal Positive Voltage Regulators is constructed using the Fairchild Planar epitaxial process. These regulators employ internal current-limiting and thermal-shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The μA78L00 used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

- **OUTPUT CURRENT UP TO 100 mA**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **AVAILABLE IN JEDEC TO-92**
- **OUTPUT VOLTAGES OF 5 V, 6.2 V, 8.2 V, 9 V, 12 V, 15 V**
- **OUTPUT VOLTAGE TOLERANCES OF ±5% OVER THE TEMPERATURE RANGE**

Absolute Maximum Ratings

Input Voltage	
5.0 V to 15 V	35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	−55°C to + 150°C
Operating Junction Temperature Ranges	
μA78L00C (Commercial)	0°C to + 125°C
Pin Temperatures	
(Soldering, 10 s)	260°C

Connection Diagram
TO-92 Package

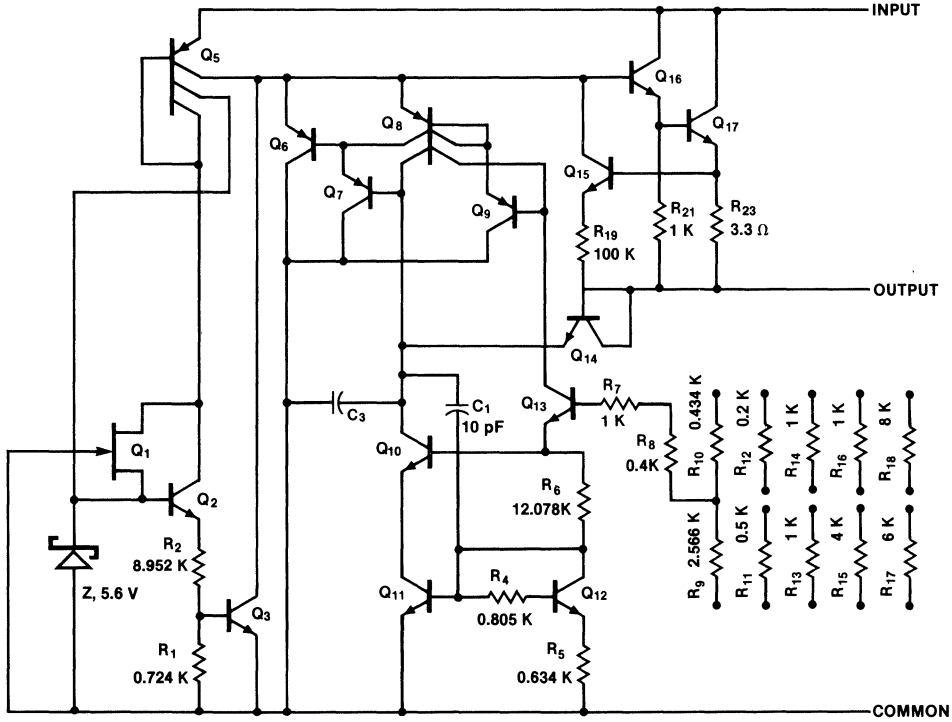


(Top View)

Order Information

Type	Package	Code	Part No.
μA78L05AC	Molded	EI	μA78L05AWC
μA78L62AC	Molded	EI	μA78L62AWC
μA78L82AC	Molded	EI	μA78L82AWC
μA78L09AC	Molded	EI	μA78L09AWC
μA78L12AC	Molded	EI	μA78L12AWC
μA78L15AC	Molded	EI	μA78L15AWC

Equivalent Circuit



μA78L05AC and μA78L05AV (Note 2)
Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified. (Note 1)

Characteristic		Condition		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7 V ≤ V_{IN} ≤ 20 V		55	150	mV
			8 V ≤ V_{IN} ≤ 20 V		45	100	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		11	60	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		5.0	30	mV
Output Voltage		7 V ≤ V_{IN} ≤ 20 V	1 mA ≤ I_{OUT} ≤ 40 mA	4.75		5.25	V
		7 V ≤ V_{IN} ≤ V_{Max} (Note 3)	1 mA ≤ I_{OUT} ≤ 70 mA	4.75		5.25	V
Quiescent Current					2.0	5.5	mA
Quiescent Current Change	with line	8 V ≤ V_{IN} ≤ 20 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
Temperature Coefficient of V_{OUT}		I_{OUT} = 5 mA			−0.65		mV/°C
Ripple Rejection		f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V, T_J = 25°C		41	49		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short-Circuit Current		T_J = 25°C			140		mA

Notes on μA78L15 page.

μA78L62AC
Electrical Characteristics V_{IN} = 12 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified. (Note 1)

Characteristic		Condition		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		5.95	6.2	6.45	V
Line Regulation		T_J = 25°C	8.5 V ≤ V_{IN} ≤ 20 V		65	175	mV
			9 V ≤ V_{IN} ≤ 20 V		55	125	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		13	80	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		6.0	40	mV
Output Voltage		8.5 V ≤ V_{IN} ≤ 20 V	1 mA ≤ I_{OUT} ≤ 40 mA	5.90		6.5	V
		8.5 V ≤ V_{IN} ≤ V_{Max} (Note 3)	1 mA ≤ I_{OUT} ≤ 70 mA	5.90		6.5	V
Quiescent Current					2.0	5.5	mA
Quiescent Current Change	with line	8.0 V ≤ V_{IN} ≤ 20 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			50		μV
Temperature Coefficient of V_{OUT}		I_{OUT} = 5 mA			−0.75		mV/°C
Ripple Rejection		f = 120 Hz, 10 V ≤ V_{IN} ≤ 20 V, T_J = 25°C		40	46		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short-Circuit Current		T_J = 25°C			140		mA

μA78L82AC
Electrical Characteristics V_{IN} = 14 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified. (Note 1)

Characteristic		Condition		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		7.87	8.2	8.53	V
Line Regulation		T_J = 25°C	11 V ≤ V_{IN} ≤ 23 V		80	175	mV
			12 V ≤ V_{IN} ≤ 23 V		70	125	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		15	80	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		8.0	40	mV
Output Voltage		11 V ≤ V_{IN} ≤ 23 V	1 mA ≤ I_{OUT} ≤ 40 mA	7.8		8.5	V
		11 V ≤ V_{IN} ≤ V_{Max} (Note 3)	1 mA ≤ I_{OUT} ≤ 70 mA	7.8		8.6	V
Quiescent Current					2.1	5.5	mA
Quiescent Current Change	with line	12 V ≤ V_{IN} ≤ 23 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			60		μV
Temperature Coefficient of V_{OUT}		I_{OUT} = 5 mA			−0.8		mV/°C
Ripple Rejection		f = 120 Hz, 12 V ≤ V_{IN} ≤ 22 V, T_J = 25°C		39	45		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short-Circuit Current		T_J = 25°C			140		mA

Notes on μA78L15 page.

μA78L09AC

Electrical Characteristics V_{IN} = 15 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified. (Note 1)

Characteristic		Condition		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		8.64	9.0	9.36	V
Line Regulation		T_J = 25°C	11.5 V ≤ V_{IN} ≤ 24 V		90	200	mV
			13 V ≤ V_{IN} ≤ 24 V		100	150	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		20	90	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		10	45	mV
Output Voltage		11.5 V ≤ V_{IN} ≤ 24 V	1 mA ≤ I_{OUT} ≤ 40 mA	8.55		9.45	V
		11.5 V ≤ V_{IN} ≤ V_{Max} (Note 3)	1 mA ≤ I_{OUT} ≤ 70 mA	8.55		9.45	V
Quiescent Current					2.1	5.5	mA
Quiescent Current Change	with line	11.5 V ≤ V_{IN} ≤ 24 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			70		μV
Temperature Coefficient of V_{OUT}		I_{OUT} = 5 mA			−0.9		mV/°C
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V, T_J = 25°C		38	44		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short-Circuit Current		T_J = 25°C			140		mA

μA78L12AC

Electrical Characteristics V_{IN} = 19 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified. (Note 1)

Characteristic		Condition		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		11.5	12	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 27 V		120	250	mV
			16 V ≤ V_{IN} ≤ 27 V		100	200	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		20	100	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		10	50	mV
Output Voltage		14.5 V ≤ V_{IN} ≤ 27 V	1 mA ≤ I_{OUT} ≤ 40 mA	11.4		12.6	V
		14.5 V ≤ V_{IN} ≤ V_{Max} (Note 3)	1 mA ≤ I_{OUT} ≤ 70 mA	11.4		12.6	V
Quiescent Current					2.1	5.5	mA
Quiescent Current Change	with line	16 V ≤ V_{IN} ≤ 27 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			80		μV
Temperature Coefficient of V_{OUT}		I_{OUT} = 5 mA			−1.0		mV/°C
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V, T_J = 25°C		37	42		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short-Circuit Current		T_J = 25°C			140		mA

Notes on μA78L15 page.

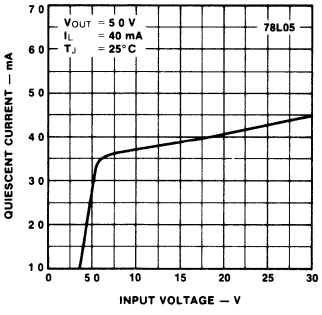
μA78L15AC
Electrical Characteristics V_{IN} = 23 V, I_{OUT} = 40 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified. (Note 1)

Characteristic		Condition		Min	Typ	Max	Unit
Output Voltage		T_J = 25°C		14.4	15	15.6	V
Line Regulation		T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V		130	300	mV
			20 V ≤ V_{IN} ≤ 30 V		110	250	mV
Load Regulation		T_J = 25°C	1 mA ≤ I_{OUT} ≤ 100 mA		25	150	mV
			1 mA ≤ I_{OUT} ≤ 40 mA		12	75	mV
Output Voltage		17.5 V ≤ V_{IN} ≤ 30 V	1 mA ≤ I_{OUT} ≤ 40 mA	14.25		15.75	V
		17.5 V ≤ V_{IN} ≤ V_{Max} (Note 2)	1 mA ≤ I_{OUT} ≤ 70 mA	14.25		15.75	V
Quiescent Current					2.2	5.5	mA
Quiescent Current Change	with line	20 V ≤ V_{IN} ≤ 30 V				1.5	mA
	with load	1 mA ≤ I_{OUT} ≤ 40 mA				0.1	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			90		μV
Temperature Coefficient of V_{OUT}		I_{OUT} = 5 mA			−1.3		mV/°C
Ripple Rejection		f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V, T_J = 25°C		34	39		dB
Dropout Voltage		T_J = 25°C			1.7		V
Peak Output/Short-Circuit Current		T_J = 25°C			140		mA

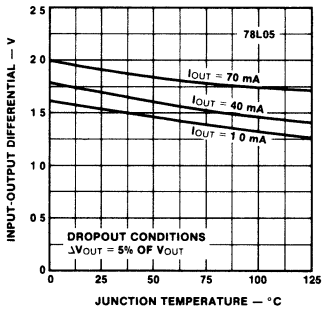
Notes
1. The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.
2. Power Dissipation ≤ .75 W.

Typical Performance Curves

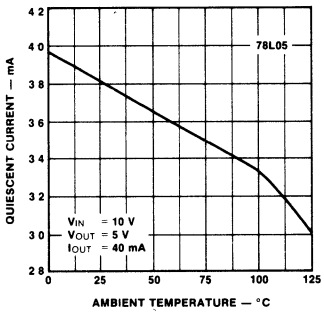
Quiescent Current as a Function of Input Voltage



Dropout Voltage as a Function of Junction Temperature



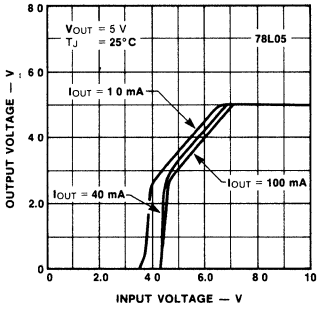
Quiescent Current as a Function of Temperature



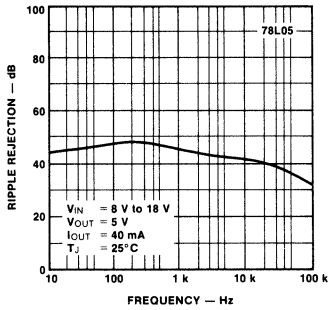
Note
Other μA78L00 Series devices have similar curves.

Typical Performance Curves (Cont.)

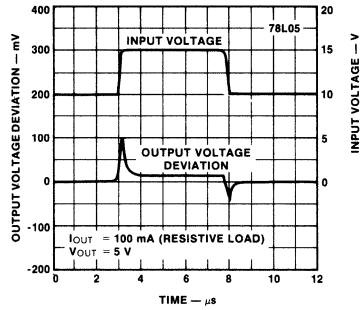
Dropout Characteristics



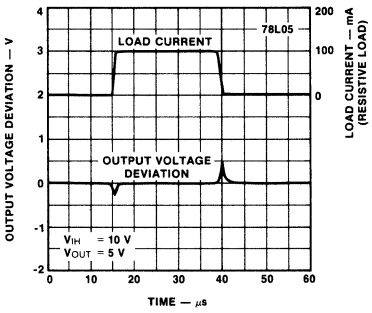
Ripple Rejection as a Function of Frequency



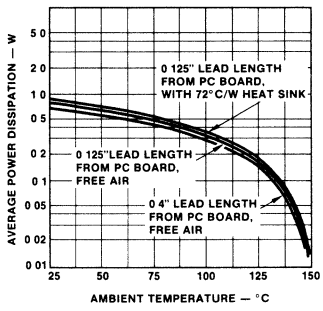
Line Transient Response



Load-Transient Response



TO-92 Worst Case Power Dissipation Versus Ambient Temperature



Design Considerations

The μA78L series regulators have thermal overload protection from excessive power, internal short-circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}	Typ θ_{JA}	Max θ_{JA}
TO-92			160	175

Thermal Considerations

The TO-92 molded package manufactured by Fairchild is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1 cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.

An explanation of the thermal paths of the TO-92 will allow the designer to determine the thermal stress he is applying in any given application.

The TO-92 Package

The TO-92 package thermal paths are complex. In addition to the path through the molding compound to ambient temperature, there is another path through the pins, in parallel with the case path, to ambient temperature, as shown in *Figure 1*.

The total thermal resistance in this model is then:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})(\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL} + \theta_{LA}}$$

Where: θ_{JC} = thermal resistance of the case between the regulator die and a point on the case directly above the die location.

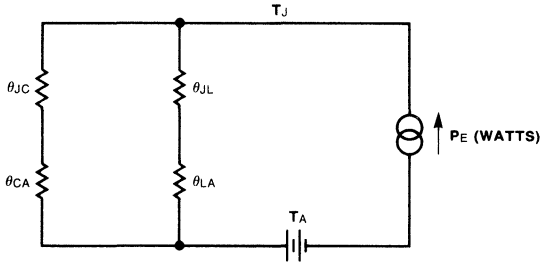
θ_{CA} = thermal resistance between the case and air at ambient temperature.

θ_{JL} = thermal resistance from transistor die through the collector lead to a point 1/16 inch below the regulator case.

θ_{LA} = total thermal resistance of the collector-base-emitter pins to ambient temperature.

θ_{JA} = junction to ambient thermal resistance.

TO-92 Thermal Equivalent Circuit
Fig. 1



Methods of Heat Sinking

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small 72°C/W flag type heat sink, such as the Staver F1-7D-2, on the 78LXX molded case. The heat sink effectively replaces the θ_{CA} (*Figure 2*) and the new thermal resistance, θ'_{JA}, is

θ'_{JA} = 145°C/W (assuming .125 inch lead length)

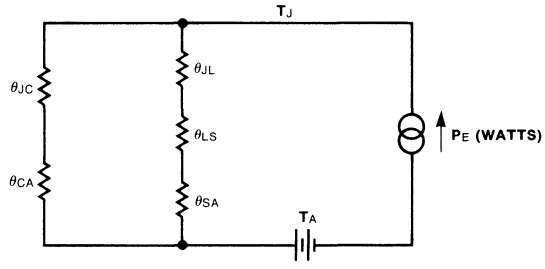
The net change of 15°C/W increases the allowable power dissipation to 0.86 W with an inserted cost of 1-2 cents. A still further decrease in θ_{JA} could be achieved by using a heat sink rated at 46°C/W, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total θ_{JA}, the other external thermal resistance, θ_{LA}, may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, θ_{SA}, from the pins at the mounting point to ambient, that is, the mounting medium. θ_{LA} is then equal to $\theta_{LS} + \theta_{SA}$. The new model is shown in *Figure 2*.

In the case of a socket, θ_{SA} could be as high as 270°C/W, thus causing a net increase in θ_{JA} and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net θ_{JA} to the original value, but pin sinking would not be accomplished.

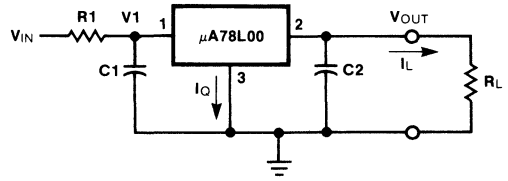
In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the pins. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

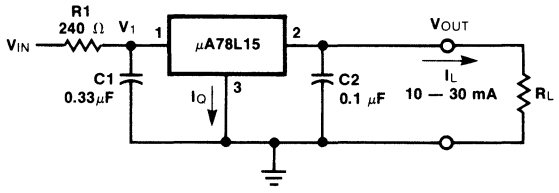
The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additional resistors are not significantly effective; beyond some point, additional copper area is not effective.

TO-92 Thermal Equivalent Circuit
(Pin at Other Than Ambient Temperature)
Fig. 2



High Dissipation Applications





When it is necessary to operate a μA78L00 regulator with a large input-output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total power dissipation between R1 and the regulator.

$$R1 = \frac{V_{IN(Min)} - V_{OUT} - 2.0\ V}{I_{L(Max)} + I_Q}$$

where I_Q is the regulator quiescent current.

Regulator power dissipation at maximum input voltage and maximum load current is now

$$P_{D(Max)} = (V_1 - V_{OUT})\, I_{L(Max)} + V_1\, I_Q$$

where

$$V_1 = V_{IN(Max)} - (I_{L(Max)} + I_Q)\, R1$$

The presence of R1 will affect load regulation according to the equation:

load regulation (at constant VIN)
= load regulation (at constant V1)
+ (line regulation, mV per V)
× (RI) × (ΔIL).

As an example, consider a 15 V regulator with a supply voltage of 30 ±5 V, required to supply a maximum load current of 30 mA. I_Q is 4.3 mA, and minimum load current is to be 10 mA.

$$R1 = \frac{25 - 15 - 2}{30 + 4.3} = \frac{34.3}{8} \simeq 240\ \Omega$$

$$V_1 = 35 - (30 + 4.3).24 = 35 - 8.2 = 26.8\ V$$

$$P_{D(Max)} = (26.8 - 15)\ 30 + 26.8\ (4.3)$$

$$= 354 + 115$$

= 470 mW, which permit operation up to 70°C in most applications.

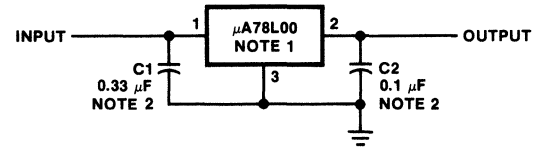
Line regulation of this circuit is typically 110 mV for an input range of 25-35 V at a constant load current; i.e. 11 mV/V.

Load regulation = constant V_1 load regulation (typically 10 mV, 10-30 mA I_L)

+ (11 mV/V) × 0.24 × 20 mA (typically 53 mV)

= 63 mV for a load current change of 20 mA at a constant V_{IN} of 30 V.

Typical Applications



Notes

1. To specify an output voltage, substitute voltage value for "00".
2. Bypass Capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

FAIRCHILD
A Schlumberger Company

μA109 • μA209 • μA309
5 Volt Regulator

Linear Products

Description

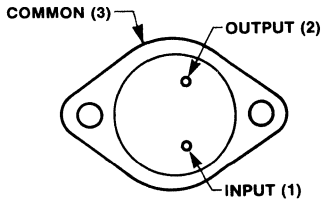
The μA109, μA209, and μA309 are complete 5 Volt Regulators constructed using the Fairchild Planar epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially indestructible. They are intended for use as local regulators, eliminating noise and distribution problems associated with single point regulation. If adequate heat sinking is provided, they can provide over 1 A output current. The μA109, μA209, and μA309 are intended primarily for use with TTL and DTL logic and are completely specified under worst case conditions to match the power supply requirements of these logic families. In addition to use as a fixed 5 V regulator, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

- **OUTPUT CURRENT IN EXCESS OF 1 A**
- **SPECIFIED TO MATCH WORST CASE TTL AND DTL REQUIREMENTS**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL-OVERLOAD PROTECTION**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**

Absolute Maximum Ratings

Input Voltage	35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	
Military Grade (μA109)	−55°C to +150°C
Industrial Grade (μA209)	−25°C to +150°C
Commercial Grade (μA309)	0°C to 125°C
Temperature (Soldering, 60 s)	300°C

Connection Diagram
TO-3 Package



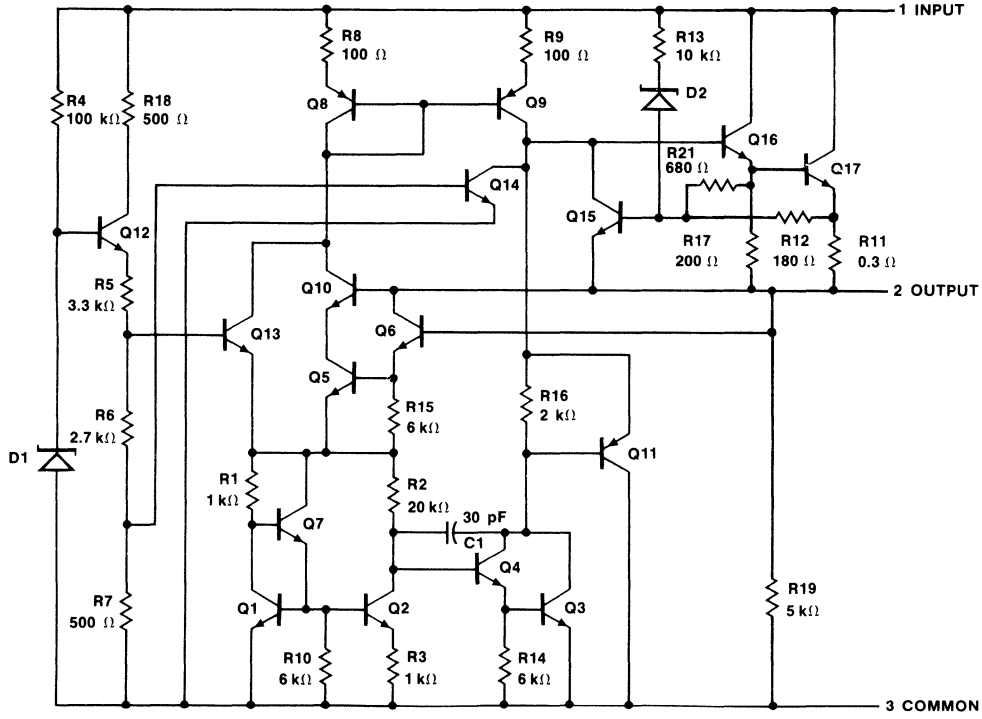
(Top View)

Case is connected to ground.

Order Information

Type	Package	Code	Part No.
μA109	Metal	HJ	μA109KM
μA209	Metal	HJ	μA209KM
μA309	Metal	HJ	μA309KC

Equivalent Circuit



μA109 • μA209
Electrical Characteristics $T_J = -55°C$ to $+150°C$ for 109, $-25°C$ to $+150°C$ for 209, $V_{IN} = 10$ V, $I_{OUT} = 0.5$ A, unless otherwise specified

Characteristic		Condition		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		4.7	5.05	5.3	V
Line Regulation		$T_J = 25°C$, $7\ V \le V_{IN} \le 25$ V			4	50	mV
Load Regulation		$T_J = 25°C$, $5\ mA \le I_{OUT} \le 1.5$ A			15	100	mV
Output Voltage		$8\ V \le V_{IN} \le 20$ V, $5\ mA \le I_{OUT} \le 1$ A, $P \le 15$ W		4.6		5.4	V
Quiescent Current		$7\ V \le V_{IN} \le 25$ V				10	mA
			$T_J = 25°C$		4.2		mA
Quiescent Current Change	with line	$8\ V \le V_{IN} \le 25$ V				0.8	mA
	with load	$5\ mA \le I_{OUT} \le 1.0$ A				0.5	mA
Output Noise Voltage		$T_A = 25°C$, $10Hz \le f \le 100$ kHz			40		μV
Long Term Stability						10	mV
Thermal Resistance Junction to Case (Note)					3.0		°C/W

Note
Without a heat sink, the thermal resistance is θ_{JA} (max) 45°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

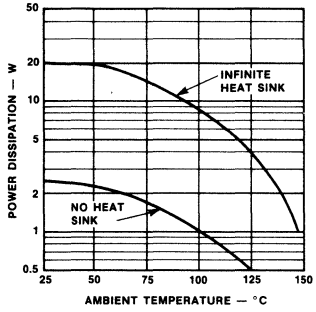
μA309
Electrical Characteristics (Note)

Characteristic		Condition	Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$	4.8	5.05	5.2	V
Line Regulation		$T_J = 25°C$ $7.0\ V \le V_{IN} \le 25$ V		4.0	50	mV
Load Regulation		$T_J = 25°C$ $5.0\ mA \le I_{OUT} \le 1.5$ A		50	100	mV
Output Voltage		$7.0\ V \le V_{IN} \le 25$ V $5.0\ mA \le I_{OUT} \le 1.0$ A $P \le 20$ W	4.75		5.25	V
Quiescent Current		$7.0\ V \le V_{IN} \le 25$ V		5.2	10	mA
Quiescent Current Change	with line	$7.0\ V \le V_{IN} \le 25$ V			0.8	mA
	with load	$5.0\ mA \le I_{OUT} \le 1.0$ A			0.5	mA
Output Noise Voltage		$T_A = 25°C$ $10\ Hz \le f \le 100$ kHz		40		μV
Long Term Stability					20	mV

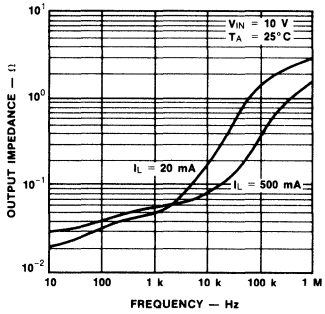
Note
Unless otherwise specified, these specifications apply for $0°C \le T_J \le 125°C$, $V_{IN} = 10$ V and $I_{OUT} = 0.5$ A.

Typical Performance Curves For μA109 and μA209

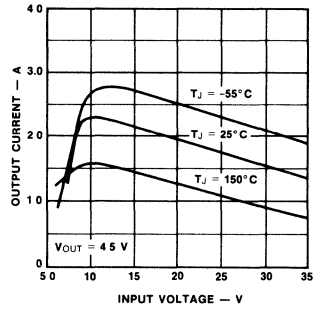
Maximum Average Power Dissipation as a Function of Ambient Temperature



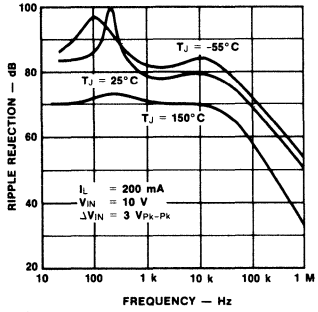
Output Impedance as a Function of Frequency



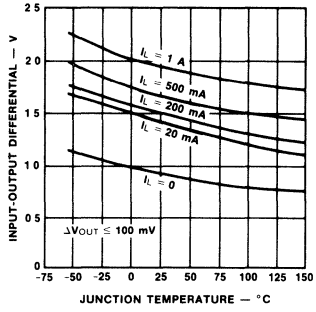
Peak Output Current as a Function of Input Voltage



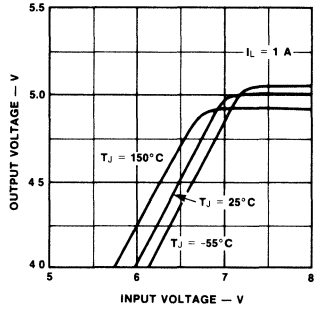
Ripple Rejection as a Function of Frequency



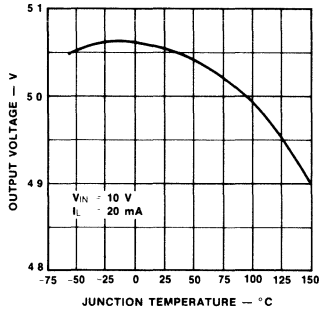
Dropout Voltage



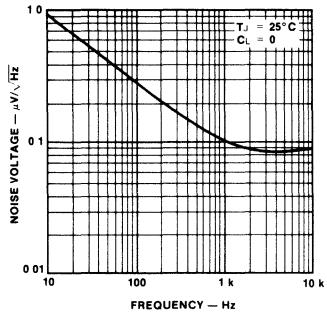
Dropout Characteristic



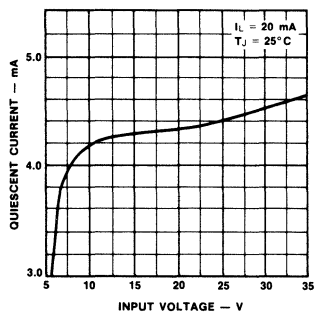
Output Voltage as a Function of Junction Temperature



Output Noise Voltage as a Function of Frequency

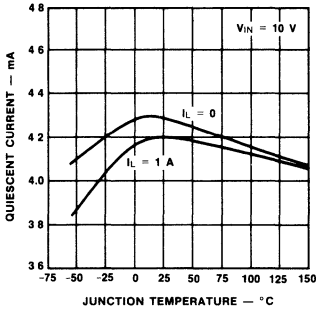


Quiescent Current as a Function of Input Voltage



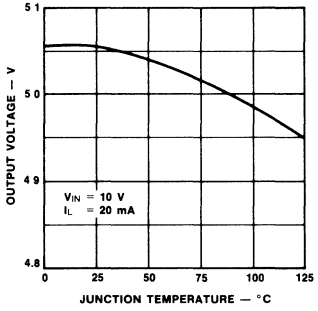
Typical Performance Curves for μA109 and μA209 (Cont.)

Quiescent Current as a Function of Temperature

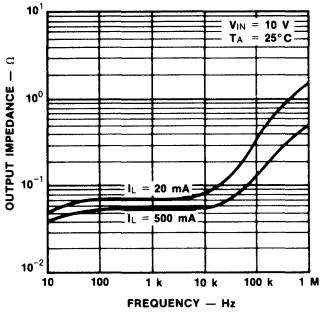


Typical Performance Curves for μA309

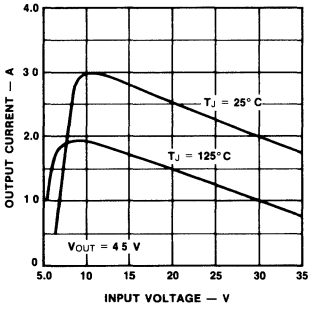
Output Voltage as a Function of Junction Temperature



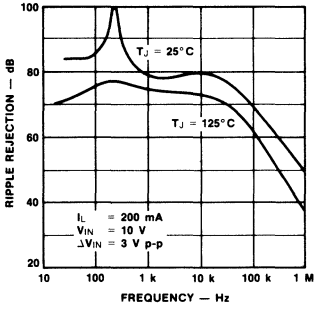
Output Impedance as a Function of Frequency



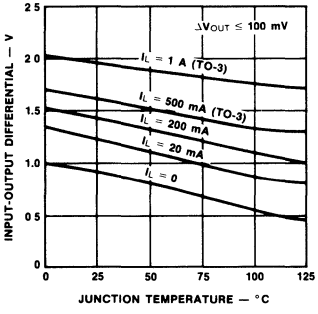
Peak Output Current as a Function of Output Voltage



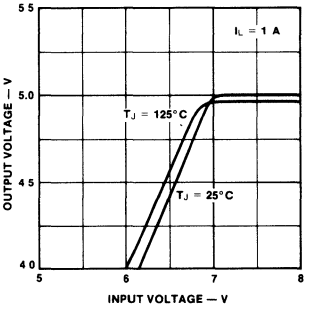
Ripple Rejection as a Function of Frequency



Dropout Voltage

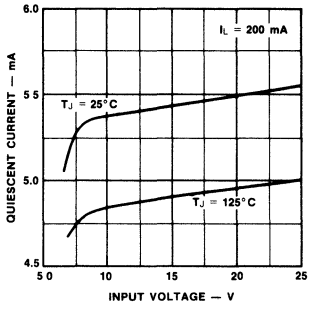


Dropout Characteristic

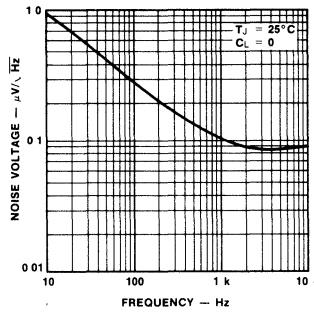


Typical Performance Curves for μA309 (Cont.)

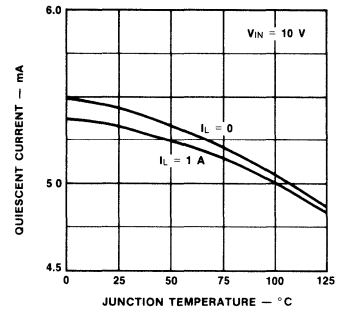
Quiescent Current as a Function of Input Voltage



Output Noise Voltage as a Function of Frequency

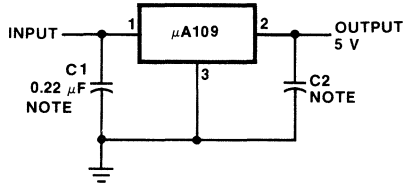


Quiescent Current as a Function of Junction Temperature



Typical Applications

Fixed 5 V Regulator



Note

Bypass capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

FAIRCHILD
A Schlumberger Company

μA7900 Series 3-Terminal Negative Voltage Regulators

Linear Products

Description

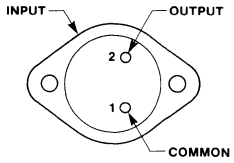
The μA7900 series of Monolithic 3-Terminal Negative Regulators is manufactured using the Fairchild Planar epitaxial process. These negative regulators are intended as complements to the popular μA7800 series of positive voltage regulators, and they are available in the same voltage options from −5 to −15 V. The 7900s employ internal current-limiting, safe-area protection, and thermal shutdown, making them virtually indestructible.

- **OUTPUT CURRENT IN EXCESS OF 1 A**
- **INTERNAL THERMAL-OVERLOAD PROTECTION**
- **INTERNAL SHORT-CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**
- **AVAILABLE IN THE TO-220 AND THE TO-3 PACKAGE**
- **OUTPUT VOLTAGES ARE 5, 8, 12 and 15 V**

Absolute Maximum Ratings

Input Voltage	
(5 V through 18 V)	−35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
TO-3 (Aluminum or Steel)	−65°C to +150°C
TO-220	−55°C to +150°C
Operating Junction Temperature Range	
Military (μA7900)	−55°C to +150°C
Commercial (μA7900C)	0°C to +125°C
Pin Temperature	
TO-3 (Soldering, 60 s)	300°C
TO-220 (Soldering, 10 s)	230°C

Connection Diagram
TO-3 Package

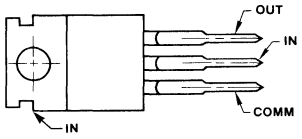


(Top View)

Order Information

Type	Package	Code	Part No.
μA7905	Metal	HJ	μA7905KM
μA7908	Metal	HJ	μA7908KM
μA7912	Metal	HJ	μA7912KM
μA7915	Metal	HJ	μA7915KM
μA7905C	Metal	HJ	μA7905KC
μA7908C	Metal	HJ	μA7908KC
μA7912C	Metal	HJ	μA7912KC
μA7915C	Metal	HJ	μA7915KC

Connection Diagram
TO-220 Package



(Top View)

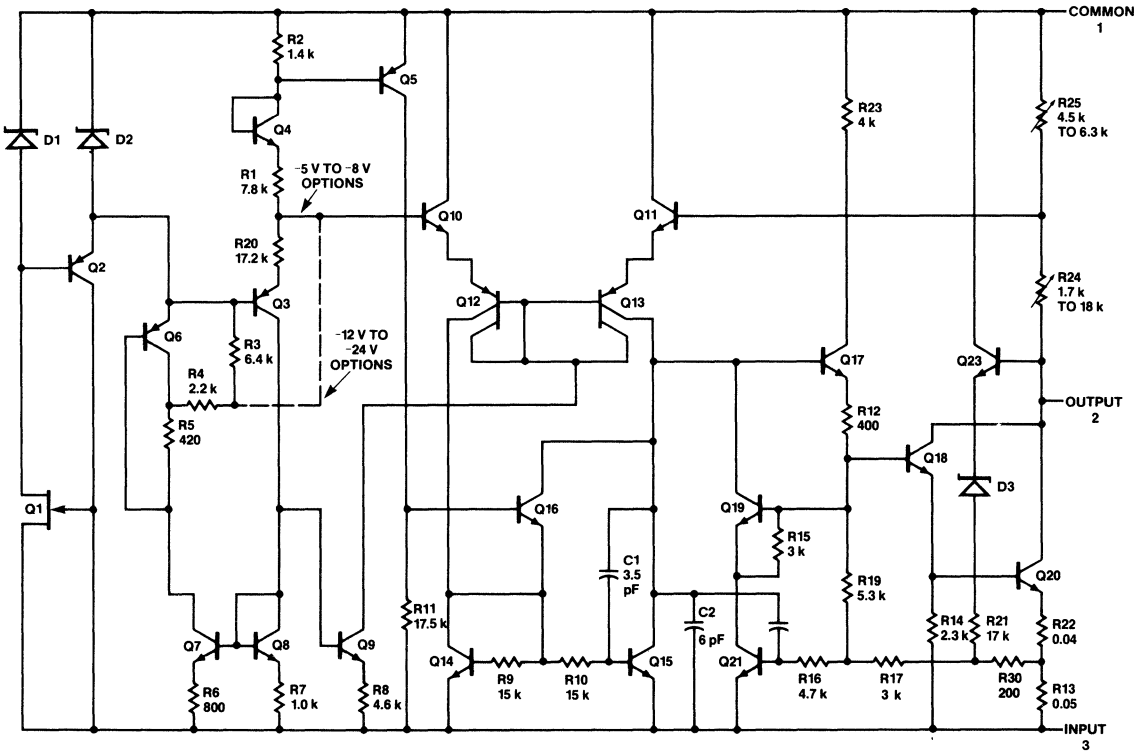
Order Information

Type	Package	Code	Part No.
μA7905C	Molded Power Pack	GH	μA7905UC
μA7908C	Molded Power Pack	GH	μA7908UC
μA7912C	Molded Power Pack	GH	μA7912UC
μA7915C	Molded Power Pack	GH	μA7915UC

Note

The convention for Negative Regulators is the Algebraic value, thus −15 is less than −10 V.

Equivalent Circuit



μA7905
Electrical Characteristics $V_{IN} = -10$ V, $I_{OUT} = 500$ mA, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, $-55°C \leq T_J \leq 150°C$, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−4.8	−5.0	−5.2	V
Line Regulation		$T_J = 25°C$	$-7\ V \leq V_{IN} \leq -25\ V$		3	50	mV
			$-8\ V \leq V_{IN} \leq -12\ V$		1	25	mV
Load Regulation		$T_J = 25°C$	$5\ mA \leq I_{OUT} \leq 1.5\ A$		15	100	mV
			$250\ mA \leq I_{OUT} \leq 750\ mA$		5	25	mV
Output Voltage		$-8.0\ V \leq V_{IN} \leq -20\ V$ $5\ mA \leq I_{OUT} \leq 1.0\ A$ $p \leq 15\ W$		−4.70		−5.30	V
Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
Quiescent Current Change	with line	$-8\ V \leq V_{IN} \leq -25\ V$				1.3	mA
	with load	$5\ mA \leq I_{OUT} \leq 1.0\ A$				0.5	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	$\mu V/V_{OUT}$
Ripple Rejection		$f = 120\ Hz$, $-8\ V \leq V_{IN} \leq -18\ V$		54	60		dB
Dropout Voltage		$I_{OUT} = 1.0\ A$, $T_J = 25°C$			1.1	2.3	V
Peak Output Current		$T_J = 25°C$		1.3	2.1	3.3	A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$, $-55°C \leq T_J \leq 150°C$				0.3	mV/°C/V_{OUT}
Short-Circuit Current		$V_{IN} = -35\ V$, $T_J = 25°C$				1.2	A

μA7905C
Electrical Characteristics $V_{IN} = -10$ V, $I_{OUT} = 500$ mA, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, $0°C \leq T_J \leq 125°C$, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−4.8	−5.0	−5.2	V
Line Regulation		$T_J = 25°C$	$-7\ V \leq V_{IN} \leq -25\ V$		3.0	100	mV
			$-8\ V \leq V_{IN} \leq -12\ V$		1.0	50	mV
Load Regulation		$T_J = 25°C$	$5\ mA \leq I_{OUT} \leq 1.5\ A$		15	100	mV
			$250\ mA \leq I_{OUT} \leq 750\ mA$		5.0	50	mV
Output Voltage		$-7\ V \leq V_{IN} \leq -20\ V$ $5\ mA \leq I_{OUT} \leq 1.0\ A$ $p \leq 15\ W$		−4.75		−5.25	V
Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
Quiescent Current Change	with line	$-7\ V \leq V_{IN} \leq -25\ V$				1.3	mA
	with load	$5\ mA \leq I_{OUT} \leq 1.0\ A$				0.5	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			125		μV
Ripple Rejection		$f = 120\ Hz$, $-8\ V \leq V_{IN} \leq -18\ V$		54	60		dB
Dropout Voltage		$I_{OUT} = 1.0\ A$, $T_J = 25°C$			1.1		V
Peak Output Current		$T_J = 25°C$			2.1		A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$, $0°C \leq T_J \leq 125°C$			0.4		mV/°C

Note
1. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA7908

Electrical Characteristics $V_{IN} = -14$ V, $I_{OUT} = 500$ mA, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, $-55°C \leq T_J \leq 150°C$, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−7.7	−8.0	−8.3	V
Line Regulation		$T_J = 25°C$	$-10.5\ V \leq V_{IN} \leq -25\ V$		6.0	80	mV
			$-11\ V \leq V_{IN} \leq -17\ V$		2.0	40	mV
Load Regulation		$T_J = 25°C$	$5\ mA \leq I_{OUT} \leq 1.5\ A$		12	100	mV
			$250\ mA \leq I_{OUT} \leq 750\ mA$		4.0	40	mV
Output Voltage		$-11.5\ V \leq V_{IN} \leq -23\ V$ $5\ mA \leq I_{OUT} \leq 1.0\ A$ $p \leq 15\ W$		−7.6		−8.4	V
Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
Quiescent Current Change	with line	$-11.5\ V \leq V_{IN} \leq -25\ V$				1.0	mA
	with load	$5\ mA \leq I_{OUT} \leq 1.0\ A$				0.5	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	$\mu V/V_{OUT}$
Ripple Rejection		$f = 120\ Hz$, $-11.5\ V \leq V_{IN} \leq -21.5\ V$		54	60		dB
Dropout Voltage		$I_{OUT} = 1.0\ A$, $T_J = 25°C$			1.1	2.3	V
Peak Output Current		$T_J = 25°C$		1.3	2.1	3.3	A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$, $-55°C \leq T_J \leq 150°C$				0.3	$mV/°C/V_{OUT}$
Short-Circuit Current		$V_{IN} = -35\ V$, $T_J = 25°C$				1.2	A

μA7908C

Electrical Characteristics $V_{IN} = -14$ V, $I_{OUT} = 500$ mA, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, $0°C \leq T_J \leq 125°C$, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−7.7	−8.0	−8.3	V
Line Regulation		$T_J = 25°C$	$-10.5\ V \leq V_{IN} \leq -25\ V$		6.0	160	mV
			$-11\ V \leq V_{IN} \leq -17\ V$		2.0	80	mV
Load Regulation		$T_J = 25°C$	$5\ mA \leq I_{OUT} \leq 1.5\ A$		12	160	mV
			$250\ mA \leq I_{OUT} \leq 750\ mA$		4.0	80	mV
Output Voltage		$-10.5\ V \leq V_{IN} \leq -23\ V$ $5\ mA \leq I_{OUT} \leq 1.0\ A$ $p \leq 15\ W$		−7.6		−8.4	V
Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
Quiescent Current Change	with line	$-10.5\ V \leq V_{IN} \leq -25\ V$				1.0	mA
	with load	$5\ mA \leq I_{OUT} \leq 1.0\ A$				0.5	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			200		μV
Ripple Rejection		$f = 120\ Hz$, $-11.5\ V \leq V_{IN} \leq -21.5\ V$		54	60		dB
Dropout Voltage		$I_{OUT} = 1.0\ A$, $T_J = 25°C$			1.1		V
Peak Output Current		$T_J = 25°C$			2.1		A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$, $0°C \leq T_J \leq 125°C$			0.6		mV/°C

Note

1. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately

μA7912
Electrical Characteristics $V_{IN} = -19$ V, $I_{OUT} = 500$ mA, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, $-55°C \leq T_J \leq 150°C$, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−11.5	−12.0	−12.5	V
Line Regulation		$T_J = 25°C$	$-14.5\ V \leq V_{IN} \leq -30\ V$		10	120	mV
			$-16\ V \leq V_{IN} \leq -22\ V$		3.0	60	mV
Load Regulation		$T_J = 25°C$	$5\ mA \leq I_{OUT} \leq 1.5\ A$		12	120	mV
			$250\ mA \leq I_{OUT} \leq 750\ mA$		4.0	60	mV
Output Voltage		$-15.5\ V \leq V_{IN} \leq -27\ V$ $5\ mA \leq I_{OUT} \leq 1.0\ A$ $p \leq 15\ W$		−11.4		−12.6	V
Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
Quiescent Current Change	with line	$-15\ V \leq V_{IN} \leq -30\ V$				1.0	mA
	with load	$5\ mA \leq I_{OUT} \leq 1.0\ A$				0.5	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	$\mu V/V_{OUT}$
Ripple Rejection		$f = 120\ Hz$, $-15\ V \leq V_{IN} \leq -25\ V$		54	60		dB
Dropout Voltage		$I_{OUT} = 1.0\ A$, $T_J = 25°C$			1.1	2.3	V
Peak Output Current		$T_J = 25°C$		1.3	2.1	3.3	A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$, $-55°C \leq T_J \leq 150°C$				0.3	$mV/°C/V_{OUT}$
Short-Circuit Current		$V_{IN} = -35\ V$, $T_J = 25°C$				1.2	A

μA7912C
Electrical Characteristics $V_{IN} = -19$ V, $I_{OUT} = 500$ mA, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, $0°C \leq T_J \leq 125°C$, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−11.5	−12.0	−12.5	V
Line Regulation		$T_J = 25°C$	$-14.5\ V \leq V_{IN} \leq -30\ V$		10	240	mV
			$-16\ V \leq V_{IN} \leq -22\ V$		3.0	120	mV
Load Regulation		$T_J = 25°C$	$5\ mA \leq I_{OUT} \leq 1.5\ A$		12	240	mV
			$250\ mA \leq I_{OUT} \leq 750\ mA$		4.0	120	mV
Output Voltage		$-14.5\ V \leq V_{IN} \leq -27\ V$ $5\ mA \leq I_{OUT} \leq 1.0\ A$ $p \leq 15\ W$		−11.4		−12.6	V
Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
Quiescent Current Change	with line	$-14.5\ V \leq V_{IN} \leq -30\ V$				1.0	mA
	with load	$5\ mA \leq I_{OUT} \leq 1.0\ A$				0.5	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			300		μV
Ripple Rejection		$f = 120\ Hz$, $-15\ V \leq V_{IN} \leq -25\ V$		54	60		dB
Dropout Voltage		$I_{OUT} = 1.0\ A$, $T_J = 25°C$			1.1		V
Peak Output Current		$T_J = 25°C$			2.1		A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$, $0°C \leq T_J \leq 125°C$			0.8		mV/°C

Note
1. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA7915

Electrical Characteristics $V_{IN} = -23$ V, $I_{OUT} = 500$ mA, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, $-55°C \leq T_J \leq 150°C$, unless otherwise specified.

Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−14.4	−15.0	−15.6	V
Line Regulation		$T_J = 25°C$	$-17.5\ V \leq V_{IN} \leq -30\ V$		11	150	mV
			$-20\ V \leq V_{IN} \leq -26\ V$		3.0	75	mV
Load Regulation		$T_J = 25°C$	$5\ mA \leq I_{OUT} \leq 1.5\ A$		12	150	mV
			$250\ mA \leq I_{OUT} \leq 750\ mA$		4.0	75	mV
Output Voltage		$-18.5\ V \leq V_{IN} \leq -30\ V$ $5\ mA \leq I_{OUT} \leq 1.0\ A$ $p \leq 15\ W$		−14.25		−15.75	V
Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
Quiescent Current Change	with line	$-18.5\ V \leq V_{IN} \leq -30\ V$				1.0	mA
	with load	$5\ mA \leq I_{OUT} \leq 1.0\ A$				0.5	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	$\mu V/V_{OUT}$
Ripple Rejection		$f = 120\ Hz$, $-18.5\ V \leq V_{IN} \leq -28.5\ V$		54	60		dB
Dropout Voltage		$I_{OUT} = 1.0\ A$, $T_J = 25°C$			1.1	2.3	V
Peak Output Current		$T_J = 25°C$		1.3	2.1	3.3	A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$, $-55°C \leq T_J \leq 150°C$			−1.0	1.3	$mV/°C/V_{OUT}$
Short-Circuit Current		$V_{IN} = -35\ V$, $T_J = 25°C$				1.2	A

μA7915C

Electrical Characteristics $V_{IN} = -23$ V, $I_{OUT} = 500$ mA, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, $0°C \leq T_J \leq 125°C$, unless otherwise specified.

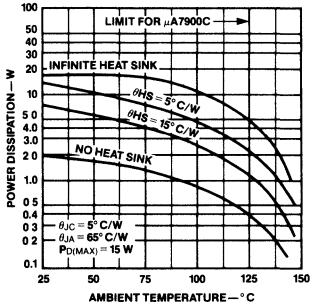
Characteristic		Condition (Note)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−14.4	−15.0	−15.6	V
Line Regulation		$T_J = 25°C$	$-17.5\ V \leq V_{IN} \leq -30\ V$		11	300	mV
			$-20\ V \leq V_{IN} \leq -26\ V$		3.0	150	mV
Load Regulation		$T_J = 25°C$	$5\ mA \leq I_{OUT} \leq 1.5\ A$		12	300	mV
			$250\ mA \leq I_{OUT} \leq 750\ mA$		4.0	150	mV
Output Voltage		$-17.5\ V \leq V_{IN} \leq -30\ V$ $5\ mA \leq I_{OUT} \leq 1.0\ A$ $p \leq 15\ W$		−14.25		−15.75	V
Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
Quiescent Current Change	with line	$-17.5\ V \leq V_{IN} \leq -30\ V$				1.0	mA
	with load	$5\ mA \leq I_{OUT} \leq 1.0\ A$				0.5	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			375		μV
Ripple Rejection		$f = 120\ Hz$, $-18.5\ V \leq V_{IN} \leq -28.5\ V$		54	60		dB
Dropout Voltage		$I_{OUT} = 1.0\ A$, $T_J = 25°C$			1.1		V
Peak Output Current		$T_J = 25°C$			2.1		A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$, $0°C \leq T_J \leq 125°C$			1.0		mV/°C

Note

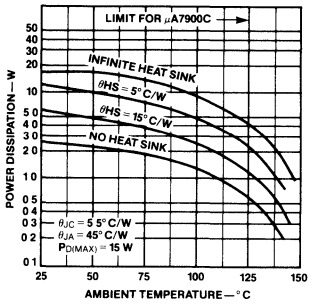
1. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Curves

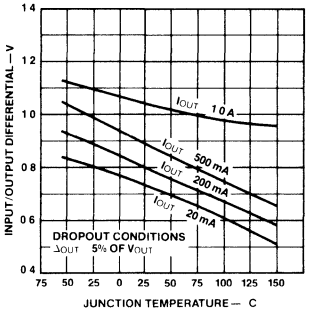
Worst Case Power Dissipation as a Function of Ambient Temperature (TO-220)



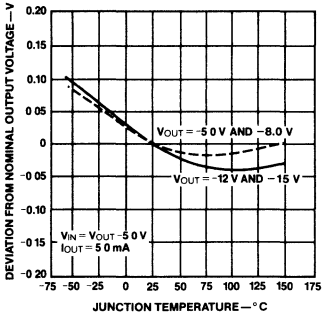
Worst Case Power Dissipation as a Function of Ambient Temperature (TO-3)



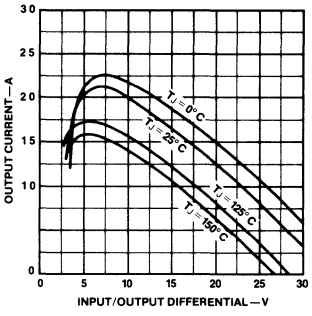
Dropout Voltage as a Function of Junction Temperature



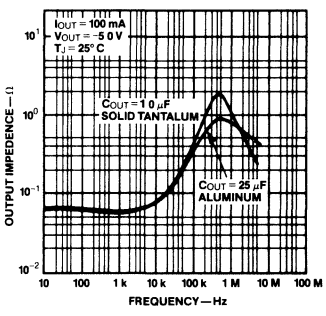
Output Voltage as a Function of Junction Temperature



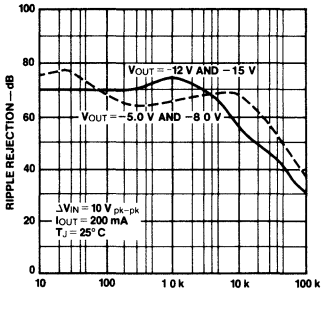
Peak Output Current as a Function of Input-Output Differential Voltage



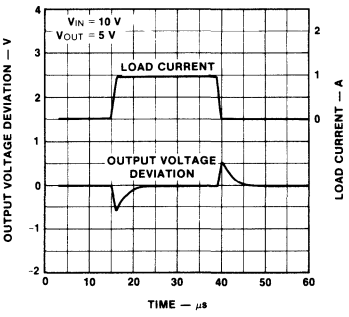
Output Impedance as a Function of Frequency



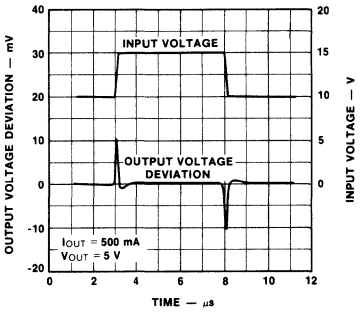
Ripple Rejection as a Function of Frequency



Load Transient Response



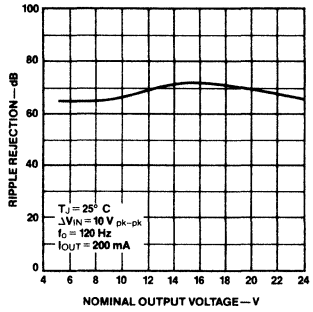
Line Transient Response



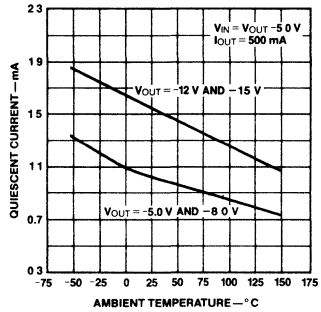
2

Typical Performance Curves (Cont.)

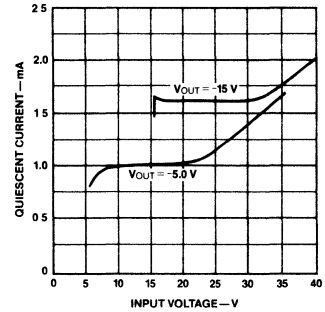
Ripple Rejection as a Function of Output Voltages



Quiescent Current as a Function of Input Voltage



Quiescent Current as a Function of Temperature



Design Considerations

The μA7900 fixed voltage regulator series has thermal-overload protection from excessive power dissipation, internal short-circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 7900, 125°C for 7900C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC} °C/W	Max θ_{JC} °C/W	Typ θ_{JA} °C/W	Max θ_{JA} °C/W
TO-3	3.5	5.5	40	45
TO-220	3.0	5.0	60	65

$$P_{D(MAX)} = \frac{T_{J\,(Max)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,(Max)}\ T_A}{\theta_{JA}}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA} \text{ (Without heat sink)}$$

Solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$

or $T_A + P_D\theta_{JA}$ (Without heat sink)

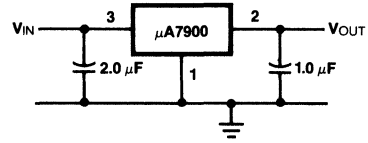
Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction-to-Ambient Thermal Resistance
θ_{JC} = Junction-to-Case Thermal Resistance
θ_{CA} = Case-to-Ambient Thermal Resistance
θ_{CS} = Case-to-Heat Sink Thermal Resistance
θ_{SA} = Heat Sink-to-Ambient Thermal Resistance

Typical Applications

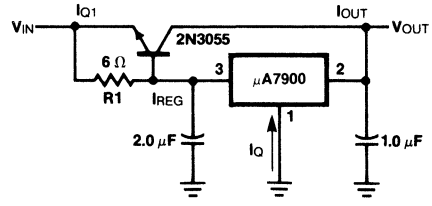
Bypass capacitors are recommended for stable operation of the μA7900 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2 μF on the input, 1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fixed Output Regulator

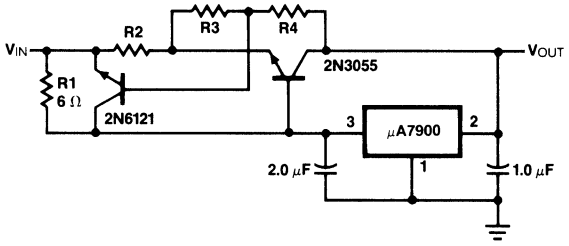


High Current Voltage Regulator

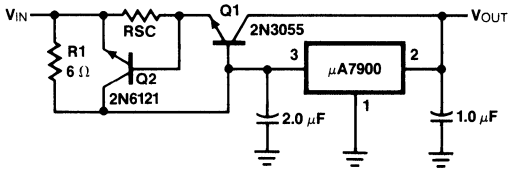


$$R1 = \frac{V_{BE(QI)}}{I_{REG}} \quad I_{QI} = \beta(Q1)I_{REG}$$

High Output Current, Foldback Current Limited

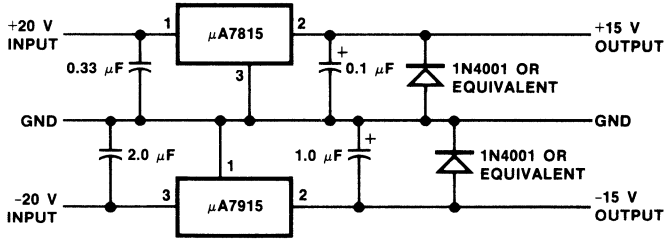


High Output Current, Short-Circuit Protected



$$RSC = \frac{V_{BE(Q2)}}{I_{SC}}$$

Operational Amplifier Supply (± 15 V @ 1.0 A)



FAIRCHILD

A Schlumberger Company

μA79M00 Series 3-Terminal Negative Voltage Regulators

Linear Products

Description

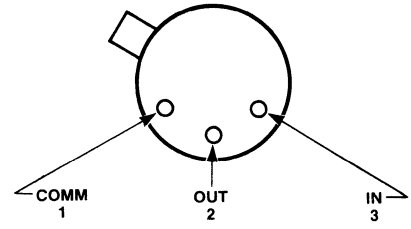
The μA79MOO series of 3-Terminal Medium Current Negative Voltage Regulators are constructed using the Fairchild Planar epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 500 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- **OUTPUT CURRENT IN EXCESS OF 0.5 A**
- **INTERNAL THERMAL-OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**
- **AVAILABLE IN JEDEC TO-220 AND TO-39 PACKAGES**
- **OUTPUT VOLTAGES OF −5 V, −8 V, −12 V, and −15 V**

Absolute Maximum Ratings

Input Voltage	
−5 V through −15 V	−35 V
−24 V	−40 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
TO-39	−65°C to +150°C
TO-220	−55°C to +125°C
Operating Junction Temperature Range	
TO-39	
Military (μA79M00)	−55°C to +150°C
Commercial (μA79M00C)	0°C to +125°C
TO-220	
Commercial (μA79M00C)	0°C to +125°C
Pin Temperature	
(Soldering, 60 s) TO-39	300°C
(Soldering, 10 s) TO-220	230°C

Connection Diagram TO-39 Package

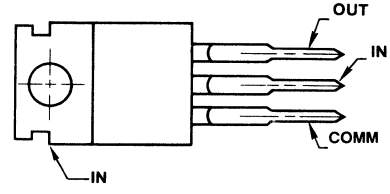


(Top View)

Order Information

Type	Package	Code	Part No.
μA79M05	Metal	FC	μA79M05HM
μA79M05C	Metal	FC	μA79M05AHC
μA79M08	Metal	FC	μA79M08HM
μA79M08C	Metal	FC	μA79M08AHC
μA79M12	Metal	FC	μA79M12HM
μA79M12C	Metal	FC	μA79M12AHC
μA79M15	Metal	FC	μA79M15HM
μA79M15C	Metal	FC	μA79M15AHC

Connection Diagram TO-220 Package

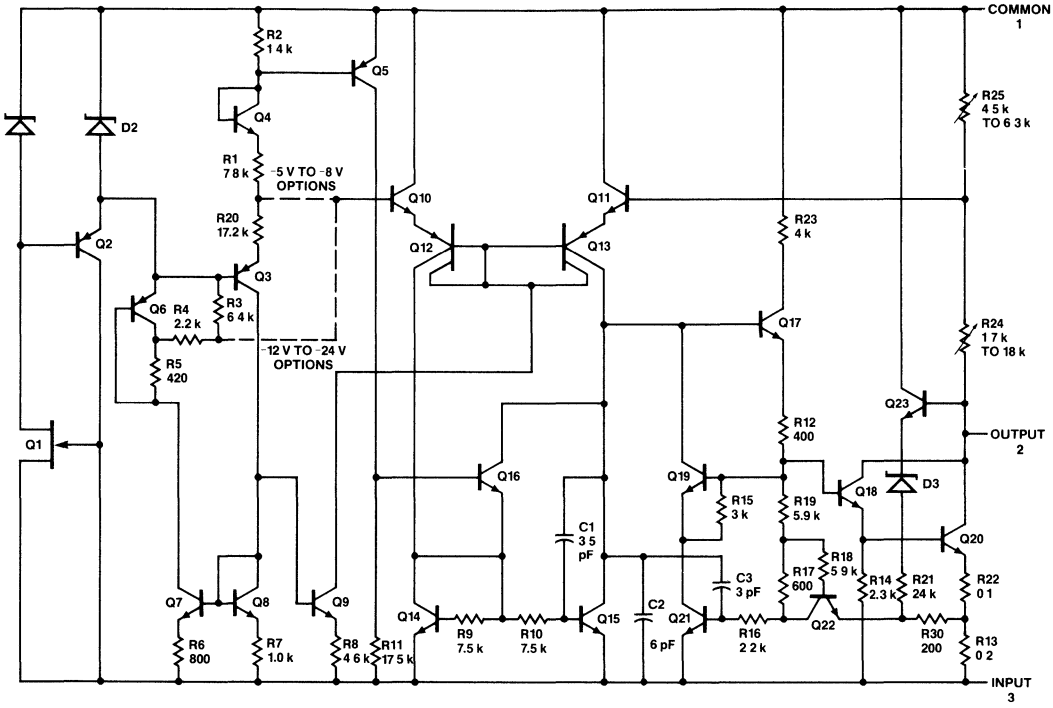


(Side View)

Order Information

Type	Package	Code	Part No.
μA79M05C	Molded Power Pack	GH	μA79M05AUC
μA79M08C	Molded Power Pack	GH	μA79M08AUC
μA79M12C	Molded Power Pack	GH	μA79M12AUC
μA79M15C	Molded Power Pack	GH	μA79M15AUC

Equivalent Circuit



μA79M05HM

Electrical Characteristics $V_{IN} = -10$ V, $I_{OUT} = 350$ mA, $-55°C \leq T_J \leq 150°C$, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, unless otherwise specified. Notes 1 and 2

Characteristic		Condition (Note 3)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−5.2	−5.0	−4.8	V
Line Regulation		$T_J = 25°C$	$-25\ V \leq V_{IN} \leq -7\ V$		7.0	50	mV
			$-18\ V \leq V_{IN} \leq -8\ V$		3.0	30	mV
Load Regulation		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 500\ mA$			75	100	mV
		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 350\ mA$			50		mV
Output Voltage		$-25\ V \leq V_{IN} \leq -7\ V$ $5\ mA \leq I_{OUT} \leq 350\ mA$, $P_D \leq 4\ W$		−5.25		−4.75	V
Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
Quiescent Current Change	with line	$-25\ V \leq V_{IN} \leq -8\ V$				0.4	mA
	with load	$5\ mA \leq I_{OUT} \leq 350\ mA$				0.4	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	μV/V_{OUT}
Ripple Rejection		$-18\ V \leq V_{IN} \leq -8\ V$,	$I_{OUT} = 100\ mA$	50			dB
		$f = 120\ Hz$	$I_{OUT} = 300\ mA$, $T_J = 25°C$	54	60		dB
Dropout Voltage		$T_J = 25°C$			1.1	2.3	V
Short-Circuit Current		$T_J = 25°C$, $V_{IN} = -35\ V$				0.6	A
Peak Output Current				0.5	0.65	1.4	A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$ $-55°C \leq T_J \leq +150°C$				0.3	mV/ °C/ V_{OUT}

Notes on 79M05A page.

μA79M05AHC AND μA79M05AUC
Electrical Characteristics $V_{IN} = -10$ V, $I_{OUT} = 350$ mA, $-0°C \leq T_J \leq 125°C$, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, unless otherwise specified.

Characteristic		Condition (Note 3)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−5.2	−5.0	−4.8	V
Line Regulation		$T_J = 25°C$	$-25\ V \leq V_{IN} \leq -7\ V$		7.0	50	mV
			$-18\ V \leq V_{IN} \leq -8\ V$		3.0	30	mV
Load Regulation		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 500\ mA$			75	100	mV
		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 350\ mA$			50		mV
Output Voltage		$-25\ V \leq V_{IN} \leq -7\ V$ $5\ mA \leq I_{OUT} \leq 350\ mA$, $P_D \leq 4\ W$		−5.25		−4.75	V
Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
Quiescent Current Change	with line	$-25\ V \leq V_{IN} \leq -8\ V$				0.4	mA
	with load	$5\ mA \leq I_{OUT} \leq 350\ mA$				0.4	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			125		μV
Ripple Rejection		$-18\ V \leq V_{IN} \leq -8\ V$,	$I_{OUT} = 100\ mA$	50			dB
		$f = 120\ Hz$	$I_{OUT} = 300\ mA$, $T_J = 25°C$	54	60		dB
Dropout Voltage		$T_J = 25°C$			1.1		V
Short-Circuit Current		$T_J = 25°C$, $V_{IN} = -30\ V$			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$			0.4		mV/ °C

Notes
1. See Test Circuit.
2. The convention for negative regulators is the algebraic values, thus −15 V is less than −10 V
3. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA79M08HM
Electrical Characteristics $V_{IN} = -14$ V, $I_{OUT} = 350$ mA, $-55°C \leq T_J \leq 150°C$, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, unless otherwise specified.

Characteristic		Condition (Note 3)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−8.3	−8.0	−7.7	V
Line Regulation		$T_J = 25°C$	$-25\ V \leq V_{IN} \leq -10.5\ V$		8.0	80	mV
			$-21\ V \leq V_{IN} \leq -11\ V$		4.0	50	mV
Load Regulation		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 500\ mA$			90	160	mV
		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 350\ mA$			60		mV
Output Voltage		$-25\ V \leq V_{IN} \leq -10.5\ V$ $5\ mA \leq I_{OUT} \leq 350\ mA$, $P_D \leq 4\ W$		−8.4		−7.6	V
Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
Quiescent Current Change	with line	$-25\ V \leq V_{IN} \leq -10.5\ V$				0.4	mA
	with load	$5\ mA \leq I_{OUT} \leq 350\ mA$				0.4	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	$\mu V/V_{OUT}$
Ripple Rejection		$-21.5\ V \leq V_{IN} \leq -11.5\ V$,	$I_{OUT} = 100\ mA$	50			dB
		$f = 120\ Hz$	$I_{OUT} = 300\ mA$, $T_J = 25°C$	54	59		dB
Dropout Voltage		$T_J = 25°C$			1.1	2.3	V
Short-Circuit Current		$T_J = 25°C$, $V_{IN} = -35\ V$				0.6	A
Peak Output Current				0.5	0.65	1.4	A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$ $-55°C \leq T_J \leq +150°C$				0.3	mV/ °C/ V_{OUT}

μA79M08AHC AND μA79M08AUC
Electrical Characteristics $V_{IN} = -14$ V, $I_{OUT} = 350$ mA, $0°C \leq T_J \leq 125°C$, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, unless otherwise specified.

Characteristic		Condition (Note 3)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−8.3	−8.0	−7.7	V
Line Regulation		$T_J = 25°C$	$-25\ V \leq V_{IN} \leq -10.5\ V$		8.0	80	mV
			$-21\ V \leq V_{IN} \leq -11\ V$		4.0	50	mV
Load Regulation		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 500\ mA$			90	160	mV
		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 350\ mA$			60		mV
Output Voltage		$-25\ V \leq V_{IN} \leq -10.5\ V$ $5\ mA \leq I_{OUT} \leq 350\ mA$, $P_D \leq 4\ W$		−8.4		−7.6	V
Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
Quiescent Current Change	with line	$-25\ V \leq V_{IN} \leq -10.5\ V$				0.4	mA
	with load	$5\ mA \leq I_{OUT} \leq 350\ mA$				0.4	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			200		μV
Ripple Rejection		$-21.5\ V \leq V_{IN} \leq -11.5\ V$,	$I_{OUT} = 100\ mA$	50			dB
		$f = 120\ Hz$	$I_{OUT} = 300\ mA$, $T_J = 25°C$	54	59		dB
Dropout Voltage		$T_J = 25°C$			1.1		V
Short-Circuit Current		$T_J = 25°C$, $V_{IN} = -30\ V$			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5\ mA$			0.6		mV/ °C

Notes on 79M05A page.

μA79M12HM
Electrical Characteristics $V_{IN} = -11$ V, $I_{OUT} = 350$ mA, $-55°C \leq T_J \leq 150°C$, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, unless otherwise specified.

Characteristic		Condition (Note 3)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−12.5	−12	−11.5	V
Line Regulation		$T_J = 25°C$	$-30\ V \leq V_{IN} \leq -14.5$ V		9.0	80	mV
			$-25\ V \leq V_{IN} \leq -15$ V		5.0	50	mV
Load Regulation		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 500$ mA			65	240	mV
		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 350$ mA			45		mV
Output Voltage		$-30\ V \leq V_{IN} \leq -14.5$ V $5\ mA \leq I_{OUT} \leq 350$ mA, $P_D \leq 4$ W		−12.6		−11.4	V
Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
Quiescent Current Change	with line	$-30\ V \leq V_{IN} \leq -14.5$ V				0.4	mA
	with load	$5\ mA \leq I_{OUT} \leq 350$ mA				0.4	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			25	80	$\mu V/V_{OUT}$
Ripple Rejection		$-25\ V \leq V_{IN} \leq -15$ V,	$I_{OUT} = 100$ mA	50			dB
		f = 120 Hz	$I_{OUT} = 300$ mA, $T_J = 25°C$	54	60		dB
Dropout Voltage		$T_J = 25°C$			1.1	2.3	V
Short-Circuit Current		$T_J = 25°C$, $V_{IN} = -35$ V				0.6	A
Peak Output Current				0.5	0.65	1.4	A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5$ mA $-55°C \leq T_J \leq +150°C$				0.3	mV/ °C/ V_{OUT}

μA79M12AHC AND μA79M12AUC
Electrical Characteristics $V_{IN} = -19$ V, $I_{OUT} = 350$ mA, $0°C \leq T_J \leq 125°C$, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, unless otherwise specified.

Characteristic		Condition (Note 3)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−12.5	−12	−11.5	V
Line Regulation		$T_J = 25°C$	$-30\ V \leq V_{IN} \leq -14.5$ V		9.0	80	mV
			$-25\ V \leq V_{IN} \leq -15$ V		5.0	50	mV
Load Regulation		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 500$ mA			65	240	mV
		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 350$ mA			45		mV
Output Voltage		$-30\ V \leq V_{IN} \leq -14.5$ V $5\ mA \leq I_{OUT} \leq 350$ mA, $P_D \leq 4$ W		−12.6		−11.4	V
Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
Quiescent Current Change	with line	$-30\ V \leq V_{IN} \leq -14.5$ V				0.4	mA
	with load	$5\ mA \leq I_{OUT} \leq 350$ mA				0.4	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			300		μV
Ripple Rejection		$-25\ V \leq V_{IN} \leq -15$ V	$I_{OUT} = 100$ mA	50			dB
		f = 120 Hz	$I_{OUT} = 300$ mA, $T_J = 25°C$	54	60		dB
Dropout Voltage		$T_J = 25°C$			1.1		V
Short-Circuit Current		$T_J = 25°C$, $V_{IN} = -30$ V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5$ mA			0.8		mV/ °C

Notes on 79M05A page.

μA79M15HM
Electrical Characteristics $V_{IN} = -23$ V, $I_{OUT} = 350$ mA, $-55°C \leq T_J \leq 150°C$, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, unless otherwise specified.

Characteristic		Condition (Note 3)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−15.6	−15	−14.4	V
Line Regulation		$T_J = 25°C$	$-30\ V \leq V_{IN} \leq -17.5$ V		9.0	80	mV
			$-28\ V \leq V_{IN} \leq -18$ V		7.0	50	mV
Load Regulation		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 500$ mA			65	240	mV
		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 350$ mA			45		mV
Output Voltage		$-30\ V \leq V_{IN} \leq -17.5$ V $5\ mA \leq I_{OUT} \leq 350$ mA, $P_D \leq 4$ W		−15.75		−14.25	V
Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
Quiescent Current Change	with line	$-30\ V \leq V_{IN} \leq -17.5$ V				0.4	mA
	with load	$5\ mA \leq I_{OUT} \leq 350$ mA				0.4	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			25	80	$\mu V/V_{OUT}$
Ripple Rejection		$-28.5\ V \leq V_{IN} \leq -18.5$ V,	$I_{OUT} = 100$ mA	50			dB
		f = 120 Hz	$I_{OUT} = 300$ mA, $T_J = 25°C$	54	59		dB
Dropout Voltage		$T_J = 25°C$			1.1	2.3	V
Short-Circuit Current		$T_J = 25°C$, $V_{IN} = -35$ V				0.6	A
Peak Output Current				0.5	0.65	1.4	A
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5$ mA $-55°C \leq T_J \leq +150°C$				0.3	mV/ °C/ V_{OUT}

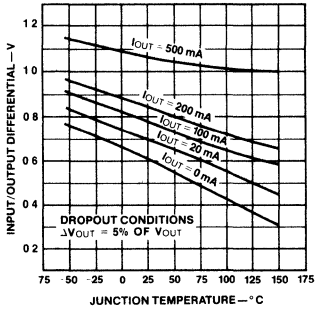
μA79M15AHC AND μA79M15AUC
Electrical Characteristics $V_{IN} = -23$ V, $I_{OUT} = 350$ mA, $0°C \leq T_J \leq 125°C$, $C_{IN} = 2\ \mu F$, $C_{OUT} = 1\ \mu F$, unless otherwise specified.

Characteristic		Condition (Note 3)		Min	Typ	Max	Unit
Output Voltage		$T_J = 25°C$		−15.6	−15	−14.4	V
Line Regulation		$T_J = 25°C$	$-30\ V \leq V_{IN} \leq -17.5$ V		9.0	80	mV
			$-28\ V \leq V_{IN} \leq -18$ V		7.0	50	mV
Load Regulation		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 500$ mA			65	240	mV
		$T_J = 25°C$, $5\ mA \leq I_{OUT} \leq 350$ mA			45		mV
Output Voltage		$-30\ V \leq V_{IN} \leq -17.5$ V $5\ mA \leq I_{OUT} \leq 350$ mA, $P_D \leq 4$ W		−15.75		−14.25	V
Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
Quiescent Current Change	with line	$-30\ V \leq V_{IN} \leq -17.5$ V				0.4	mA
	with load	$5\ mA \leq I_{OUT} \leq 350$ mA				0.4	mA
Output Noise Voltage		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			375		μV
Ripple Rejection		$-28.5\ V \leq V_{IN} \leq -18.5$ V,	$I_{OUT} = 100$ mA	50			dB
		f = 120 Hz	$I_{OUT} = 300$ mA, $T_J = 25°C$	54	59		dB
Dropout Voltage		$T_J = 25°C$			1.1		V
Short-Circuit Current		$T_J = 25°C$, $V_{IN} = -30$ V			140		mA
Peak Output Current					650		mA
Average Temperature Coefficient of Output Voltage		$I_{OUT} = 5$ mA			1.0		mV/ °C

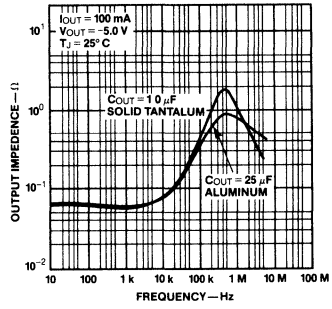
Note
All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Curves

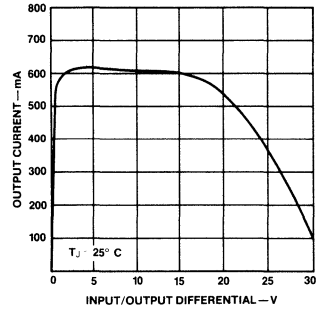
Dropout Voltage as a Function of Junction Temerature



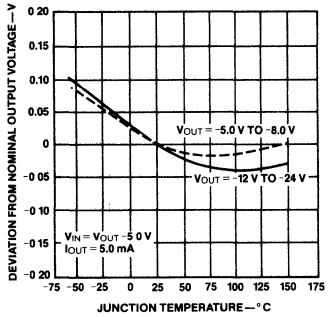
Output Voltage as a Function of Junction Temperature



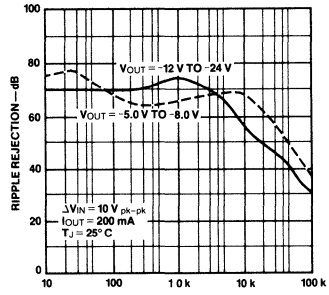
Peak Output Current as a Function of Input-Output Differential Voltage



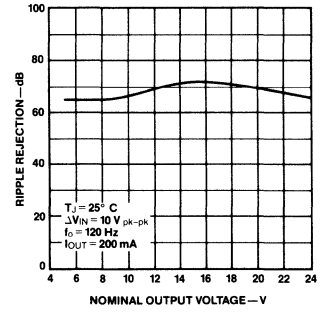
Output Impedance as a Function of Frequency



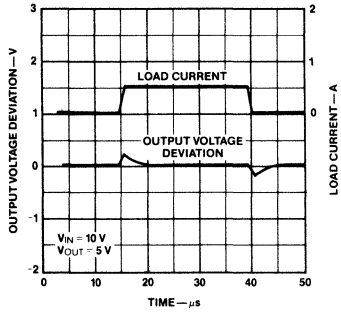
Ripple Rejection as a Function of Frequency



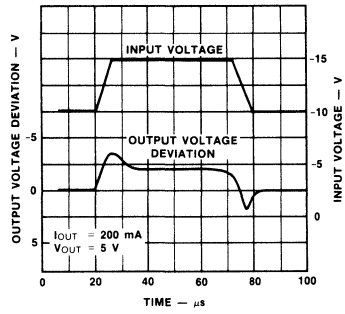
Ripple Rejection as a Function of Output Voltages



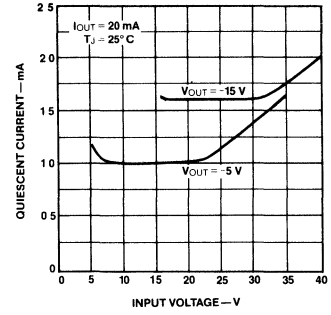
Load Transient Response



Line Transient Response

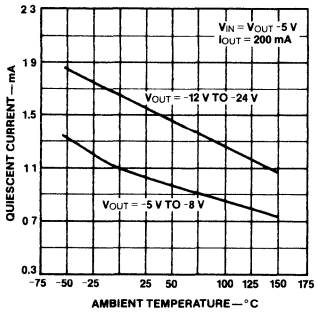


Quiescent Current as a Function of Input Voltage

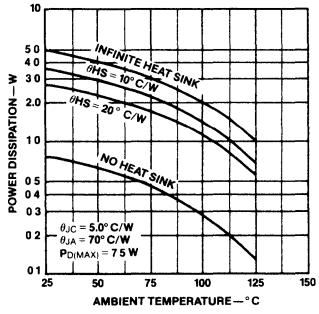


Typical Performance Curves (Cont.)

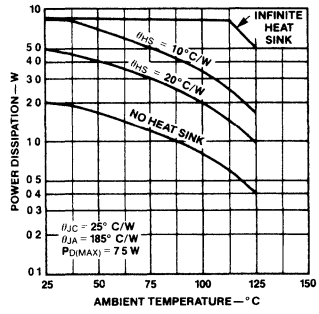
Quiescent Current as a Function of Temperature



Worst Case Power Dissipation Versus Ambient Temperature TO-39



Worst Case Power Dissipation Versus Ambient Temperature TO-220



2

Design Considerations

The μ79M00 fixed voltage regulator series has thermal-overload protection from excessive power, internal short-circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output current as the voltage across the pass transistor is increased.

The safe-area protection network may cause the device to latch-up if the output is shorted and the regulator is operating with high input voltages. This mode of operation will not damage the device. However, power (input voltage or the load) must be interrupted momentarily for the device to recover from the latched condition.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for 79M00, 125°C for 79M00AC and 79M00C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}	Typ θ_{JA}	Max θ_{JA}
TO-39	18.0	25	120	160
TO-220	3.0	5.0	60	65

$$P_{D\,(MAX)} = \frac{T_{J\,(Max)} - T_A}{\theta_{JC} + \theta_{CA}} \quad \text{or} \quad \frac{T_{J\,(Max)} - T_A}{\theta_{JA}}$$

(Without a heat sink)

$\theta_{CA} = \theta_{CS} + \theta_{SA}$

Solving for T_J: $T_J = T_A + P_D\,(\theta_{JC}+\theta_{CA})$ or $T_A + P_D\,\theta_{JA}$

(Without a heat sink)

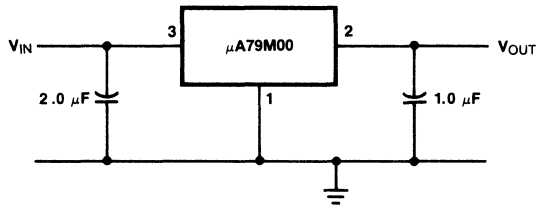
Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-case thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink thermal resistance
θ_{SA} = Heat sink-to-ambient thermal resistance
θ_{JA} = Junction-to-ambient thermal resistance

Typical Applications

Bypass capacitors are recommended for stable operation of the 79M00 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2 μF on the input, 1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capactiors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fixed Output Regulator



FAIRCHILD

A Schlumberger Company

μA78G • μA79G 4-Terminal Adjustable Voltage Regulators

Linear Products

Description

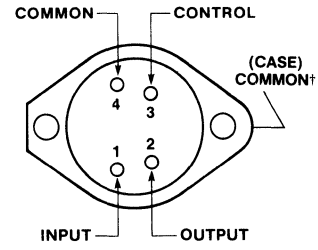
The μA78G and μA79G are 4-Terminal Adjustable Voltage Regulators. They are designed to deliver continuous load currents of up to 1.0 A with a maximum input voltage of 40 V for the positive regulator 78G and −40 V for the negative regulator 79G. Output current capability can be increased to greater than 1.0 A through use of one or more external transistors. The output voltage range of the 78G positive voltage regulator is 5 V to 30 V and the output voltage range of the negative 79G is −30 V to −2.2 V. For systems requiring both a positive and negative, the 78G and 79G are excellent for use as a dual tracking regulator with appropriate external circuitry. These 4-terminal voltage regulators are constructed using the Fairchild Planar process.

- **OUTPUT CURRENT IN EXCESS OF 1 A**
- **μA78G POSITIVE OUTPUT 5 TO 30 V**
- **μA79G NEGATIVE OUTPUT −30 TO −2.2 V**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT PROTECTION**
- **OUTPUT TRANSISTOR SAFE-AREA PROTECTION**
- **MILITARY AND COMMERCIAL VERSIONS**
- **4-PIN TO-202 TYPE AND 4-PIN TO-3**

Absolute Maximum Ratings

Input Voltage	
μA78G, μA78GC	40 V
μA79G, μA79GC	−40 V
Control Pin Voltage	
μA78G, μA78GC	$0 \leq V \leq V_{OUT}$
μA79G, μA79GC	$-V_{OUT} \leq -V \leq 0$
Power Dissipation	
Operating Junction Temperature Range	Internally Limited
Military (μA78G, μA79G)	−55°C to 150°C
Commercial (μA78GC, μA79GC)	0°C to 150°C
Storage Temperature Range	
4-Pin Power Watt (U1)	−55°C to +150°C
4-Pin TO-3 (K)	−65°C to +150°C
Pin Temperature (Soldering)	
4-Pin Power Watt (U1) (10 s)	230°C
4-Pin TO-3 (K) (60 s)	300°C

μA78G Connection Diagram TO-3 Package



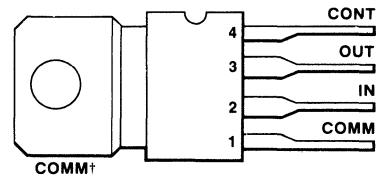
(Top View)

Heat sink tabs connected to common through device substrate.

Order Information

Type	Package	Code	Part No.
μA78G	TO-3	GK	μA78GKM
μA78GC	TO-3	GK	μA78GKC

μA78G Connection Diagram Power Watt Package



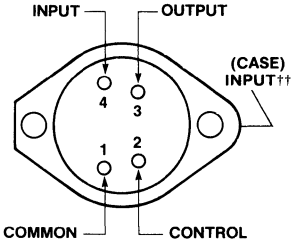
(Side View)

Heat sink tabs connected to common through device substrate.

Order Information

Type	Package	Code	Part No.
μA78GC	Power Watt	8Z	μA78GU1C

μA79G Connection Diagram
TO-3 Package



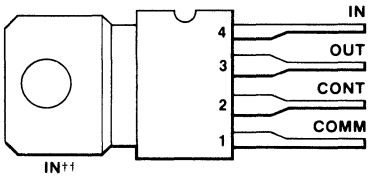
(Top View)

Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

Order Information

Type	Package	Code	Part No.
μA79G	TO-3	GK	μA79GKM
μA79GC	TO-3	GK	μA79GKC

μA79G Connection Diagram
Power Watt Package



(Side View)

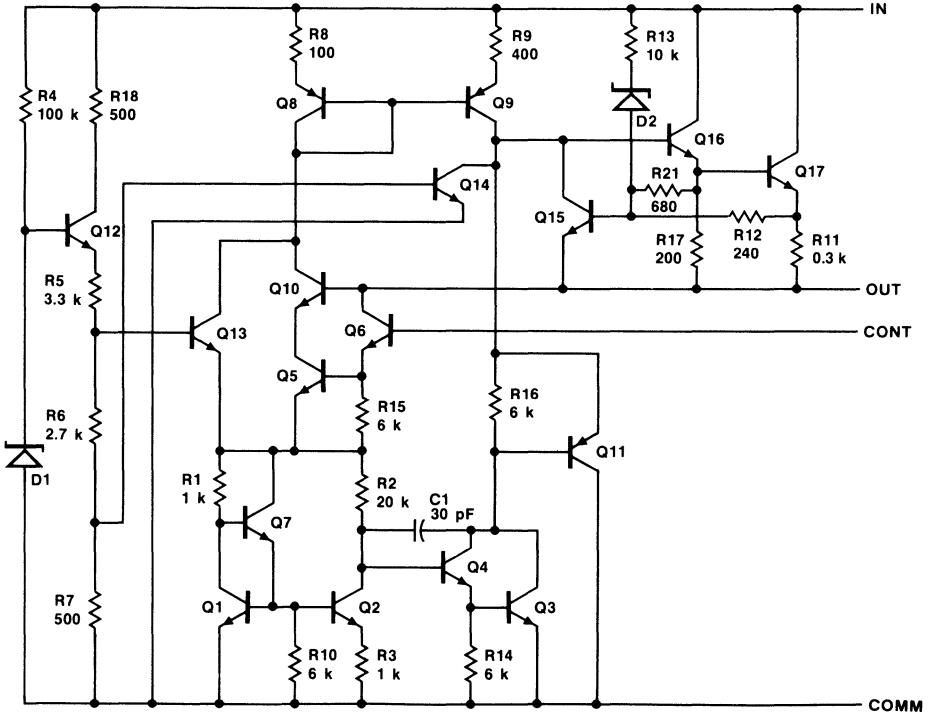
Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

Order Information

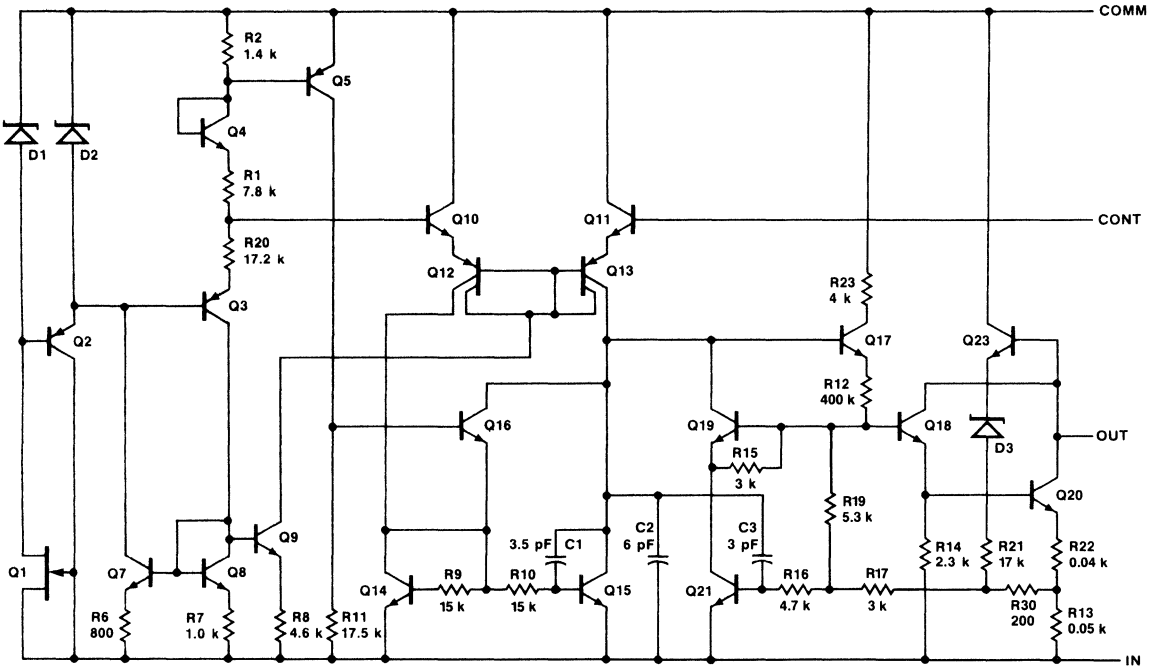
Type	Package	Code	Part No.
μA79GC	Power Watt	8Z	μA79GU1C

2

μA78G Equivalent Circuit



79G Equivalent Circuit



μA78G, μA78GC
Electrical Characteristics $0°C \leq T_J \leq 125°C$ for 78GC, $C_{IN} = 0.33\ \mu F$, $C_{OUT} = 0.1\ \mu F$ and $-55°C \leq T_J \leq 150°C$ for 78G, $V_{IN} = 10\ V$, $I_{OUT} = 500\ mA$, Test Circuit 1, unless otherwise specified.

Characteristic	Condition (Note 1, 3)		Min	Typ	Max	Unit
Input Voltage Range	$T_J = 25°C$		7.5		40	V
Output Voltage Range	$V_{IN} = V_{OUT} + 5\ V$		5.0		30	V
Output Voltage Tolerance	$V_{OUT} + 3\ V \leq V_{IN} \leq V_{OUT} + 15\ V$, $5\ mA \leq I_{OUT} \leq 1.0\ A$, $P_D \leq 15\ W$, $V_{IN\ (max)} = 38\ V$	$T_J = 25°C$			4.0	%(V_{OUT})
					5.0	%(V_{OUT})
Line Regulation	$T_J = 25°C$, $V_{OUT} \leq 10\ V$, $(V_{OUT} + 2.5\ V) \leq V_{IN} \leq (V_{OUT} + 20\ V)$				1.0	%(V_{OUT})
	$T_J = 25°C$, $V_{OUT} \geq 10\ V$, $(V_{OUT} + 3\ V) \leq V_{IN} \leq (V_{OUT} + 15\ V)$, $(V_{OUT} + 3\ V) \leq V_{IN} \leq (V_{OUT} + 7\ V)$				0.75 0.67	%(V_{OUT})
Load Regulation	$T_J = 25°C$, $V_{IN} = V_{OUT} + 5\ V$	$250\ mA \leq I_{OUT} \leq 750\ mA$ $5\ mA \leq I_{OUT} \leq 1.5\ A$			1.0 2.0	%(V_{OUT})
Control Pin Current	$T_J = 25°C$			1.0	5.0	μA
					8.0	μA
Quiescent Current	$T_J = 25°C$			3.2	5.0	mA
					6.0	mA
Ripple Rejection	$8\ V \leq V_{IN} \leq 18\ V$, $f = 120\ Hz$	μA78G	68	78		dB
	$V_{OUT} = 5\ V$	μA78GC	62	78		dB
Output Noise Voltage	$T_J = 25°C$, $10\ Hz < f < 100\ kHz$, $V_{OUT} = 5\ V$, $I_{OUT} = 5\ mA$			8	40	$\mu V / V_{OUT}$
Dropout Voltage	(Note 2)	μA78G		2	2.5	V
		μA78GC			2.5	V
Short Circuit Current	$T_J = 25°C$, $V_{IN} = 30\ V$			.750	1.2	A
Peak Output Current	$T_J = 25°C$		1.3	2.2	3.3	A
Average Temperature Coefficient of Output Voltage	$V_{OUT} = 5\ V$, $I_{OUT} = 5\ mA$	$T_J = -55°C$ to $+25°C$			.4	mV/°C/V_{OUT}
		$T_J = +25°C$ to $+150°C$			.3	
Control Pin Voltage (Reference)	$T_J = 25°C$		4.8	5.0	5.2	V
			4.75		5.25	V

Notes

1. V_{OUT} is defined for the 78GC as $V_{OUT} = \frac{R1 + R2}{R2}(5.0)$; The 79GC as $V_{OUT} = \frac{R1 + R2}{R2}(-2.23)$
2. Dropout Voltage is defined as that input-output voltage differential which causes the output voltage to decrease by 5% of its initial value.
3. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

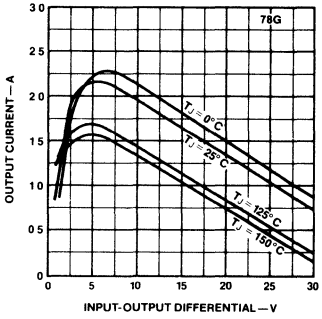
μA79G, μA79GC
Electrical Characteristics $0°C \le T_J \le 125°C$ for 79GC and $-55°C \le T_J \le 150°C$ for 79G, $V_{IN} = -10$ V, $I_{OUT} = 500$ mA, $C_{IN} = 2$ μF, $C_{OUT} = 1$ μF, Test Circuit 2 and Note 3 unless otherwise specified.

Characteristic	Condition (Note 1)		Min	Typ	Max	Unit
Input Voltage Range	$T_J = 25°C$		−40		−7.0	V
Nominal Output Voltage Range	$V_{IN} = V_{OUT} - 5$ V		−30		−2.23	V
Output Voltage Tolerance	$V_{OUT} -15$ V $\le V_{IN} \le V_{OUT} - 3$ V, 5 mA $\le I_{OUT} \le$ 1.0 A, $P_D \le 15$ W, $V_{IN\ (max)} = -38$ V	$T_J = 25°C$			4.0	%(V_{OUT})
					5.0	%(V_{OUT})
Line Regulation	$T_J = 25°C$, $V_{OUT} \ge -10$ V, $(V_{OUT} - 20\ V) \le V_{IN} \le (V_{OUT} - 2.5\ V)$				1.0	%(V_{OUT})
	$T_J = 25°C$, $V_{OUT} \le -10$ V, $(V_{OUT} - 15\ V) \le V_{IN} \le (V_{OUT} - 3\ V)$, $(V_{OUT} - 7\ V) \le V_{IN} \le (V_{OUT} - 3\ V)$				0.75 0.67	%(V_{OUT})
Load Regulation	$T_J = 25°C$, $V_{IN} = V_{OUT} - 5$ V	250 mA $\le I_{OUT} \le$ 750 mA 5 mA $\le I_{OUT} \le$ 1.5 A			1.0 2.0	%(V_{OUT})
Control Pin Current	$T_J = 25°C$			0.4	2.0	μA
					3.0	μA
Quiescent Current	$T_J = 25°C$			0.5	1.5	mA
					2.0	mA
Ripple Rejection	$-18\ V \le V_{IN} \le -8$ V,	μA79G	50	60		dB
	$V_{OUT} = -5$ V, f = 120 Hz	μA79GC	50	60		dB
Output Noise Voltage	$T_J = 25°C$, 10 Hz $\le$ f $\le$ 100 kHz, $V_{OUT} = -5$ V, $I_{OUT} = 5$ mA			25	80	μV/V_{OUT}
Dropout Voltage	(Note 2)	μA79G		1.1	2.3	V
		μA79GC			2.3	V
Short Circuit Current	$T_J = 25°C$, $V_{IN} = -30$ V			0.25	1.2	A
Peak Output Current	$T_J = 25°C$		1.3	2.1	3.3	A
Average Temperature Coefficient of Output Voltage	$V_{OUT} = -5$ V, $I_{OUT} = 5$ mA	$T_J = -55°C$ to $+25°C$			0.3	mV/°C/V_{OUT}
		$T_J = +25°C$ to $+150°C$			0.3	
Control Pin Voltage (Reference)	$T_J = 25°C$		−2.32	−2.23	−2.14	V
			−2.35		−2.11	V

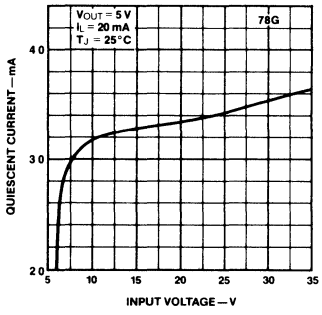
Notes
1. V_{OUT} is defined for the 78GC as $V_{OUT} = \frac{R1 + R2}{R2}(5.0)$; The 79GC as $V_{OUT} = \frac{R1 + R2}{R2}(-2.23)$.
2. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by 5% of its initial value.
3. The convention for negative regulators is the algebraic value, thus −15 is less than −10 V.
4. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \le 10$ ms, duty cycle $\le 5\%$).
   Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Curves for μA78G

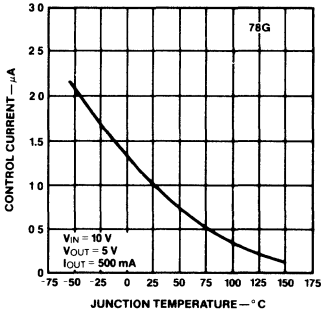
Peak Output Current vs Input-Output Differential Voltage



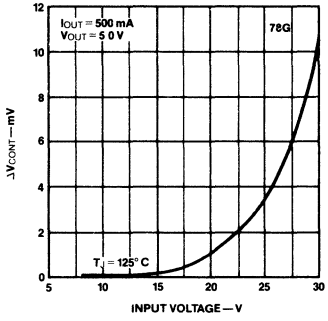
Quiescent Current vs Input Voltage



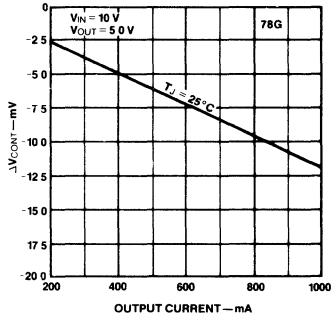
Control Current vs Temperature



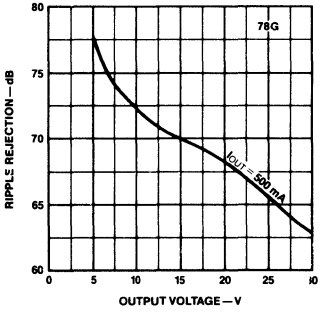
Differential Control Voltage vs Input Voltage



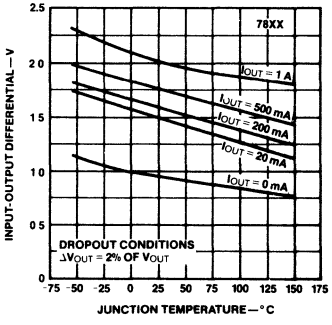
Differential Control Voltage vs Output Current



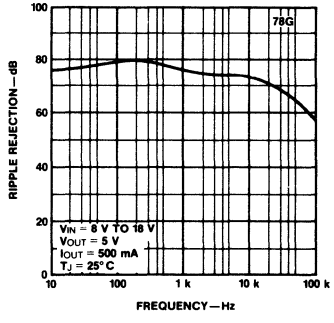
Ripple Rejection vs Output Voltage



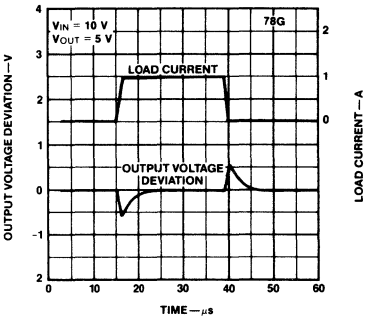
Dropout Voltage vs Junction Temperature



Ripple Rejection vs Frequency

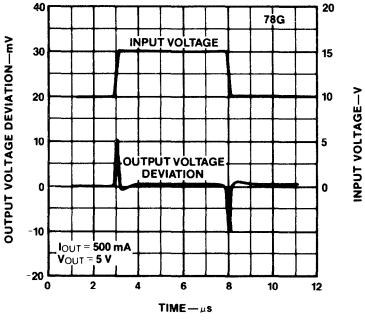


Load Transient Response



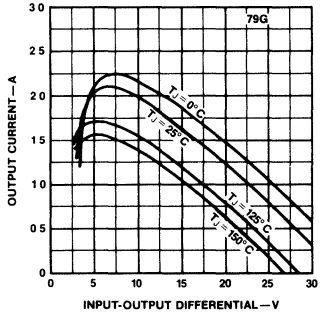
Typical Performance Curves for μA78G (Cont.)

Line Transient Response

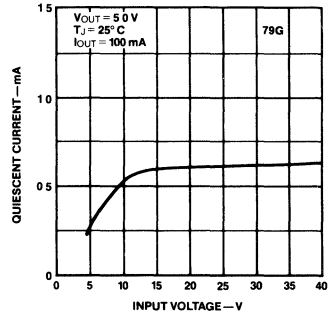


Typical Performance Curves for μA79G

Peak Output Current vs Input-Output Differential Voltage

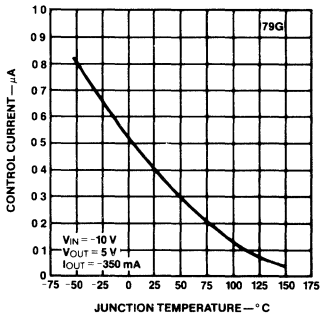


Quiescent Current vs Input Voltage

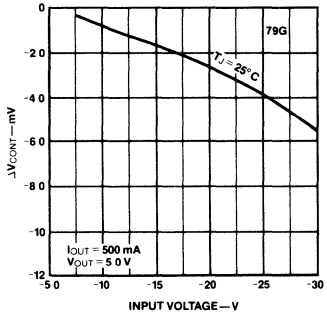


Typical Performance Curves for μA79G (Cont.)

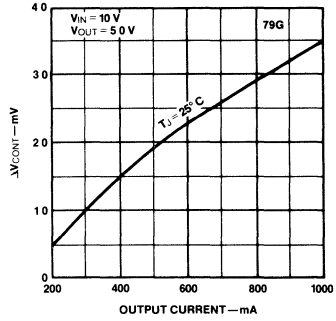
Control Current vs Temperature



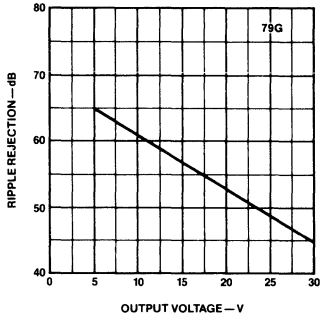
Differential Control Voltage vs Input Voltage



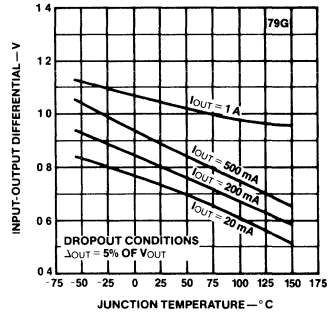
Differential Control Voltage vs Output Current



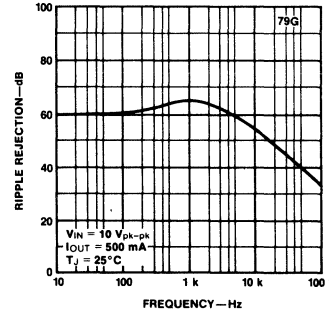
Ripple Rejection vs Output Voltage



Dropout Voltage vs Junction Temperature

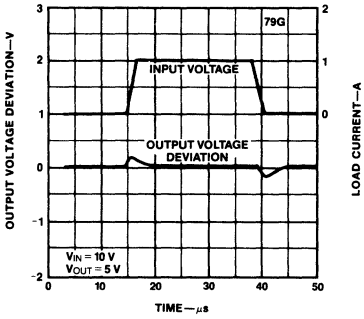


Ripple Rejection vs Frequency

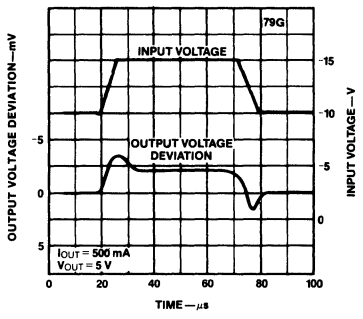


Typical Performance Curves for μA79G (Cont.)

Load Transient Response



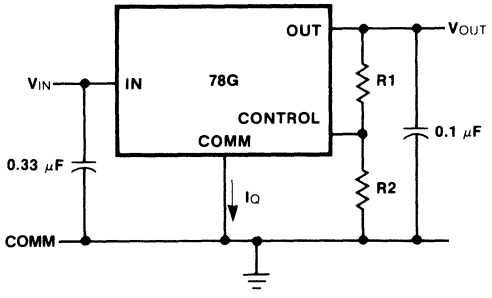
Line Transient Response



2

Test Circuits

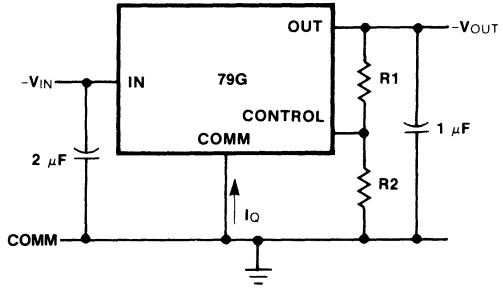
μA78G Test Circuit 1



$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

$V_{CONTROL}$ Nominal = 5 V

μA79G Test Circuit 2



$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

$V_{CONTROL}$ Nominal = −2.23 V

Recommended R2 current ≈ 1 mA

∴ R2 = 5 kΩ (78/G)

R2 = 2.2 kΩ (79/G)

Design Considerations

The 78G and 79G adjustable voltage regulators have an output voltage which varies from $V_{CONTROL}$ to typically

$$V_{IN} - 2\ V \text{ by } V_{OUT} = V_{CONTROL}\ \frac{(R1 + R2)}{R2}.$$

The nominal reference in the 78G is 5.0 V and 79G is −2.23 V. If we allow 1.0 mA to flow in the control string to eliminate bias current effects, we can make R2 = 5 kΩ in the 78G. The output voltage is then: V_{OUT} = (R1 + R2) V, where R1 and R2 are in kΩs.

Example: If R2 = 5 kΩ and R1 = 10 kΩ then
V_{OUT} = 15 V nominal, for the 78G
R2 = 2.2 kΩ and R1 = 12.8 kΩ then
V_{OUT} = −15.2 nominal, for the 79G

By proper wiring of the feedback resistors, load regulation of the device can be improved significantly.

Both 78G and 79G regulators have thermal-overload protection from excessive power, internal short-circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Design Considerations (Cont.)

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

	Typ °C/W	Max °C/W	Typ °C/W	Max °C/W
Package	θ_{JC}	θ_{JC}	θ_{JA}	θ_{JA}
Power Watt	7.5	11	75	80
TO-3	4.0	6	44	47

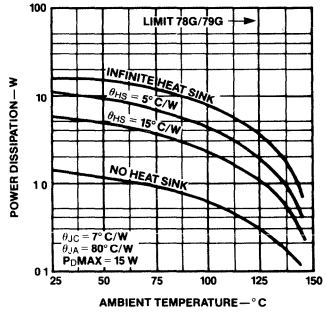
$$P_{D\,(max)} = \frac{T_{J\,(max)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,(max)} - T_A}{\theta_{JA}}$$
(Without a heat sink)

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

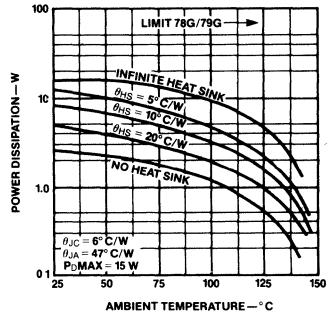
Solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink resistance
θ_{SA} = Heat sink to ambient thermal resistance

μA78G and μA79G
Power Tab (U1) Package
Worst Case Power Dissipation
vs Ambient Temperature

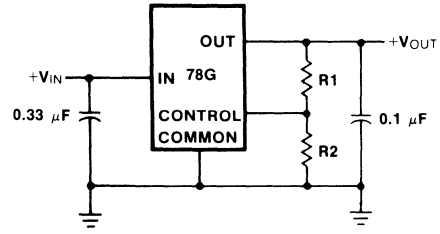


μA78G and μA79G
TO-3 Package
Worst Case Power Dissipation vs
Ambient Temperature
Test Circuit



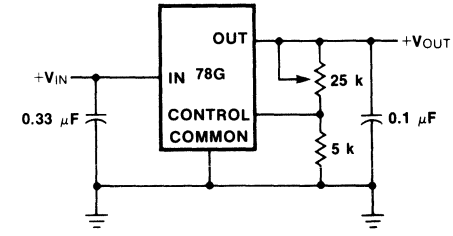
Typical Applications For μA78G
Bypassing of the input and output (0.33 μF and 0.1 μF, respectively) is necessary.

Basic Positive Regulator



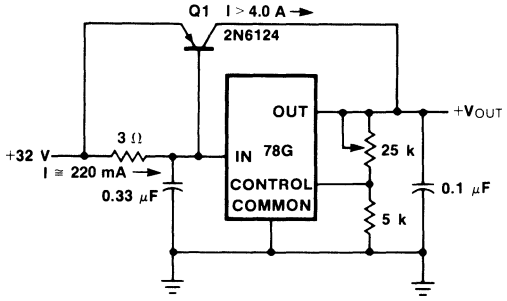
$$V_{OUT} = V_{COUNT}\left(\frac{R_1 + R_2}{R_2}\right)$$

Positive 5 to 30 V Adjustable Regulator



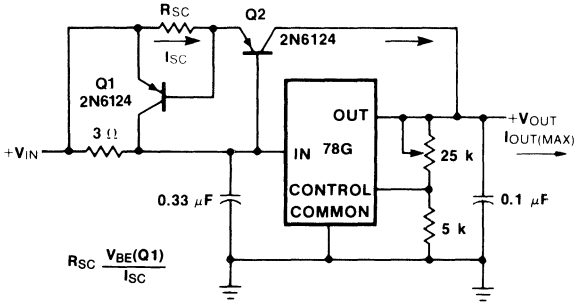
Typical Applications for μA78G (Cont.)

Positive 5 V to 30 V Adjustable Regulator $I_{OUT} > 5.0$ A

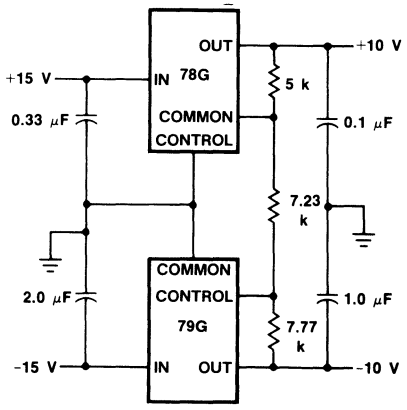


External series pass device is not short circuit protected.

Positive High-Current Short-Circuit Protected Regulator

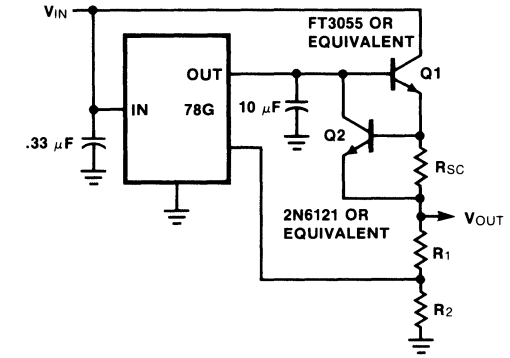


± 10 V, 1.0 A Dual Tracking Regulator



If load is not ground referenced, connect reverse biased diodes from outputs to ground.

Positive High-Current Short-Circuit Protected Regulator



2

FAIRCHILD

A Schlumberger Company

μA78MG • μA79MG 4-Terminal Adjustable Voltage Regulators

Linear Products

Description

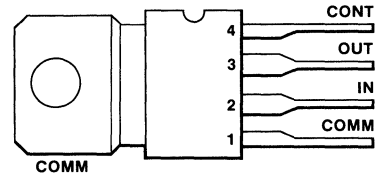
The μA78MG and μA79MG are 4-Terminal Adjustable Voltage Regulators. They are designed to deliver continuous load currents of up to 500 mA with a maximum input voltage of 40 V for the positive regulator 78MG and −40 V for the negative regulator 79MG. Output current capability can be increased to greater than 10 A through use of one or more external transistors. The output voltage range of the 78MG positive voltage regulator is 5 V to 30 V and the output voltage range of the negative 79MG is −30 to −2.2 V. For systems requiring both a positive and negative, the 78MG and 79MG are excellent for use as a dual tracking regulator. These 4-terminal voltage regulators are constructed using the Fairchild Planar process.

- **OUTPUT CURRENT IN EXCESS OF 0.5 A**
- **μA78MG POSITIVE OUTPUT VOLTAGE 5 to 30 V**
- **μA79MG NEGATIVE OUTPUT VOLTAGE −30 V TO −2.2 V**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT PROTECTION**
- **OUTPUT TRANSISTOR SAFE-AREA PROTECTION**

Absolute Maximum Ratings

Input Voltage	
μA78MGC	40 V
μA79MGC	−40 V
Control Pin Voltage	
μA78MGC	$0 \leq V \leq V_{OUT}$
μA79MGC	$-V_{OUT} \leq -V \leq 0$
Power Dissipation	Internally Limited
Operating Junction Temperature Range	0°C to 125°C
Storage Temperature Range	−55°C to +150°C
Pin Temperature (Soldering, 10 s)	230°C

Connection Diagram
μA78MG Power Watt



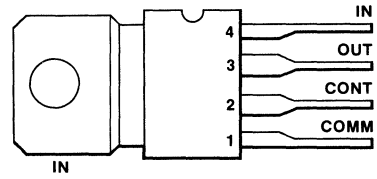
(Side View)

Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

Order Information

Type	Package	Code	Part No.
μA78MGC	Molded Power Pack	8Z	μA78MGU1C

Connection Diagram
μA79MG Power Watt



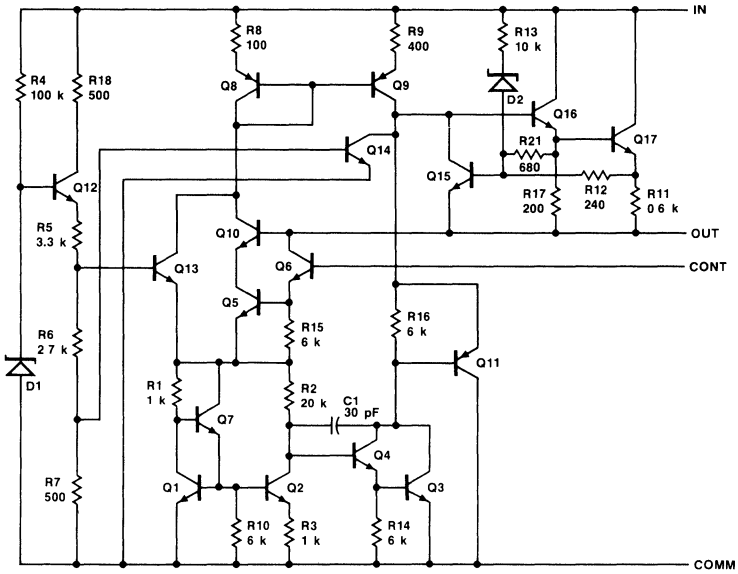
(Side View)

Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

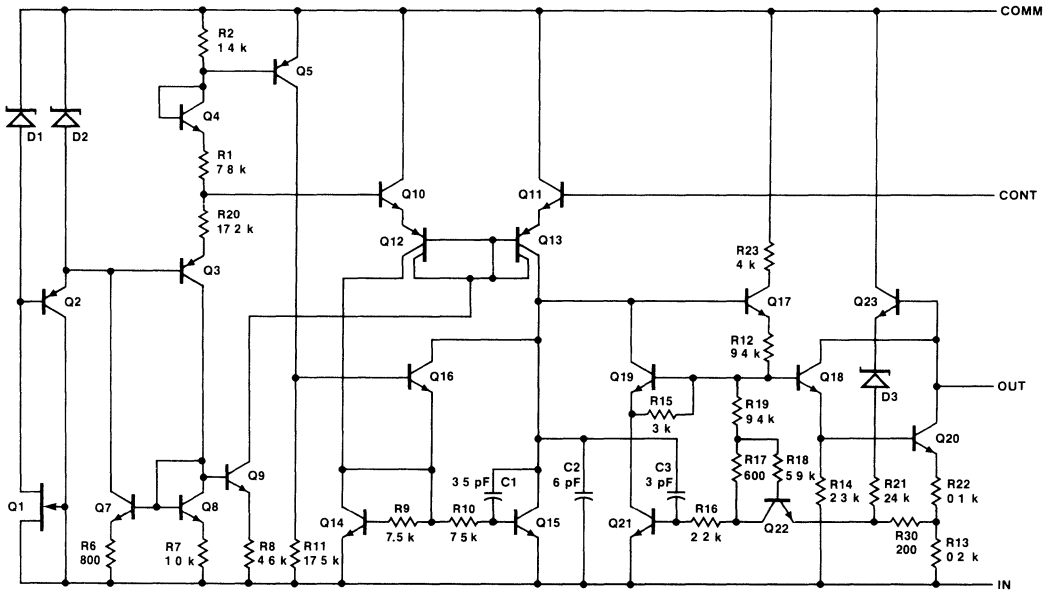
Order Information

Type	Package	Code	Part No.
μA79MG	Molded Power Pack	8Z	μA79MGU1C

78MG Equivalent Circuit



79MG Equivalent Circuit



Resistor values in Ω unless otherwise noted.

μA78MGC
Electrical Characteristics $0°C \leq T_J \leq 125°C$ for μA78MGC, V_{IN} = 10 V, I_{OUT} = 350 mA, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, Test Circuit 1, unless otherwise specified.

Characteristic	Condition (1 and 3)		Min	Typ	Max	Unit
Input Voltage Range	T_J = 25°C		7.5		40	V
Output Voltage Range	$V_{IN} = V_{OUT}$ + 5 V		5.0		30	V
Output Voltage Tolerance	V_{OUT} + 3 V ≤ V_{IN} ≤ V_{OUT} + 15 V, 5 mA ≤ I_{OUT} ≤ 350 mA, $P_D \leq$ 5 W, V_{INMax} = 38 V	T_J = 25°C			4.0	%(V_{OUT})
					5.0	%(V_{OUT})
Line Regulation	T_J = 25°C, I_{OUT} = 200 mA, $V_{OUT} \leq$ 10 V (V_{OUT} + 2.5 V) ≤ V_{IN} ≤ (V_{OUT} + 20 V) T_J = 25°C, I_{OUT} = 200 mA, $V_{OUT} \geq$ 10 V (V_{OUT} + 3 V) ≤ V_{IN} ≤ (V_{OUT} + 15 V) (V_{OUT} + 3 V) ≤ V_{IN} ≤ (V_{OUT} + 7 V)				1.0 0.75 0.67	%(V_{OUT}) %(V_{OUT}) %(V_{OUT})
Load Regulation	T_J = 25°C 5 mA ≤ I_{OUT} ≤ 500 mA, $V_{IN} = V_{OUT}$ + 7 V				1.0	%(V_{OUT})
Control Pin Current	T_J = 25°C			1.0	5.0	μA
					8.0	μA
Quiescent Current	T_J = 25°C			2.8	5.0	mA
					6.0	mA
Ripple Rejection	8 V ≤ V_{IN} ≤ 18 V, V_{OUT} = 5 V, f = 120 Hz	I_{OUT} = 300 mA, T_J = 25°C	62	80		dB
		I_{OUT} = 100 mA	62			dB
Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, V_{OUT} = 5 V			8	40	μV/V_{OUT}
Dropout Voltage	(Note 2)	μA78MGHM		2	2.5	V
		μA78MG (HC and C)			2.5	
Short-Circuit Current	V_{IN} = 35 V, T_J = 25°C				600	mA
Peak Output Current	T_J = 25°C		0.4	0.8	1.4	A
Average Temperature Coefficient of Output Voltage	V_{OUT} = 5 V, I_{OUT} = 5 mA	T_J = −55°C to +25°C			0.4	mV/°C/V_{OUT}
		T_J = +25°C to +150°C			0.3	
Control Pin Voltage (Reference)	T_J = 25°C		4.8	5.0	5.2	V
			4.75		5.25	V

Notes

1. V_{OUT} is defined for the 78MGC as $V_{OUT} = \frac{R1 + R2}{R2}$ (5 0).
   The 79MGC as $V_{OUT} = \frac{R1 + R2}{R2}$ (−2.23).
2. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by 5% of its initial value.
3. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

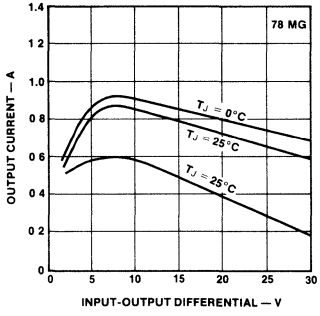
μA79MGC
Electrical Characteristics $0°C \leq T_J \leq 125°C$ for μA79MGC, $V_{IN} = -10$ V, $I_{OUT} = 350$ mA, $C_{IN} = 2.0$ μF, $C_{OUT} = 1.0$ μF, Test Circuit 2, unless otherwise specified.

Characteristic	Condition (1, 2, and 3)		Min	Typ	Max	Unit
Input Voltage Range	$T_J = 25°C$		−40		−7.0	V
Output Voltage Range	$V_{IN} = V_{OUT} - 5$ V		−30		−2.23	V
Output Voltage Tolerance	$V_{OUT} - 15$ V $\leq V_{IN} \leq V_{OUT} - 3$ V, 5 mA $\leq I_{OUT} \leq$ 350 mA, $P_D \leq 5$ W, $V_{INMax} = -38$ V	$T_J = 25°C$			4.0	%(V_{OUT})
					5.0	%(V_{OUT})
Line Regulation	$T_J = 25°C$, $I_{OUT} = 200$ mA, $V_{OUT} \geq -10$ V, $(V_{OUT} - 20\text{ V}) \leq V_{IN} \leq (V_{OUT} - 2.5\text{ V})$				1.0	%(V_{OUT})
	$T_J = 25°C$, $I_{OUT} = 200$ mA, $V_{OUT} \leq -10$ V, $(V_{OUT} - 15\text{ V}) \leq V_{IN} \leq (V_{OUT} - 3\text{ V})$				0.75	%(V_{OUT})
	$(V_{OUT} - 7\text{ V}) \leq V_{IN} \leq (V_{OUT} - 3\text{ V})$				0.67	%(V_{OUT})
Load Regulation	$V_{IN} = V_{OUT} - 7$ V, 5 mA $\leq I_{OUT} \leq$ 500 mA, $T_J = 25°C$				1.0	%(V_{OUT})
Control Pin Current	$T_J = 25°C$				3.0	μA
					2.0	μA
Quiescent Current	$T_J = 25°C$			0.5	1.5	mA
					2.5	mA
Ripple Rejection	$-18\text{ V} \leq V_{IN} \leq -8$ V, $V_{OUT} = -5$ V, f = 120 Hz	$T_J = 25°C$, $I_{OUT} = 300$ mA	54	65		dB
		$I_{OUT} = 100$ mA	50			dB
Output Noise Voltage	10 Hz $\leq$ f $\leq$ 100 kHz, $V_{OUT} = -5$ V			25	80	μV/V_{OUT}
Dropout Voltage	(Note 2)	μA79MGHM		1.1	2.3	V
		μA79MG (HC and C)			2.3	
Short-Circuit Current	$V_{IN} = -35$ V				600	mA
Peak Output Current			0.4	.65	1.4	mA
Average Temperature Coefficient of Output Voltage	$V_{OUT} = -5$ V, $I_{OUT} = -5$ mA	$T_J = -55°C$ to $+25°C$			0.3	mV/°C/V_{OUT}
		$T_J = +25°C$ to $+150°C$			0.3	
Control Pin Voltage (Reference)	$T_J = 25°C$		−2.32	−2.23	−2.14	V
			−2.35		−2.11	V

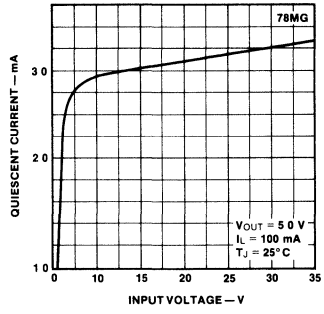
Notes
1. The convention for negative regulators is the Algebraic value, thus −15 is less than −10 V.
2. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.
3. V_{OUT} is defined for the 79MGC as $V_{OUT} = \frac{R1 + R2}{R2}(-2.23)$.

Typical Performance Curves For μA78MG

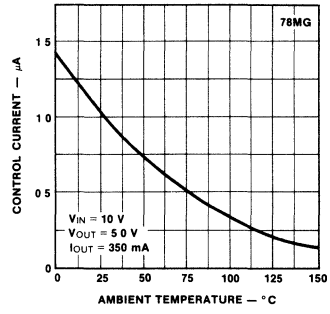
Peak Output Current as a Function of Input-Output Differential Voltage



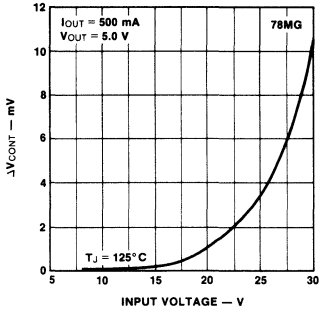
Quiescent Current as a Function of Input Voltage



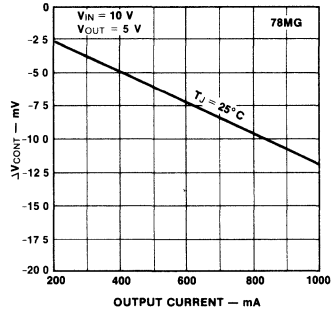
Control Current as a Function of Temperature



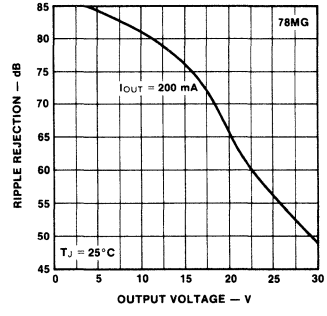
Differential Control Voltage as a Function of Input Voltage



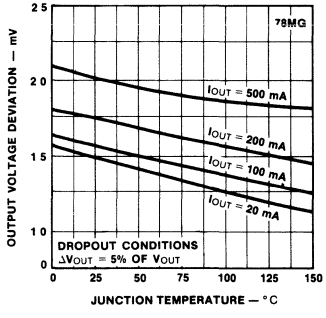
Differential Control Voltage as a Function of Output Current



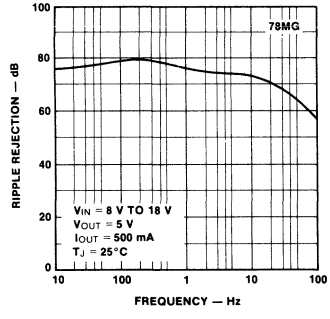
Ripple Rejection as a Function of Output Voltage



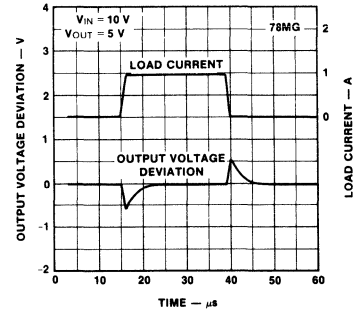
Dropout Voltage as a Function of Junction Temperature



Ripple Rejection as a Function of Frequency

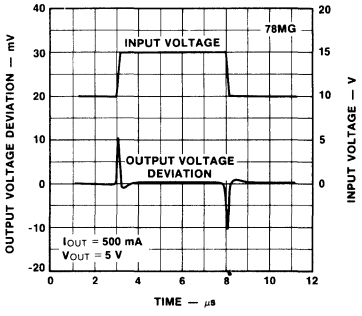


Load Transient Response



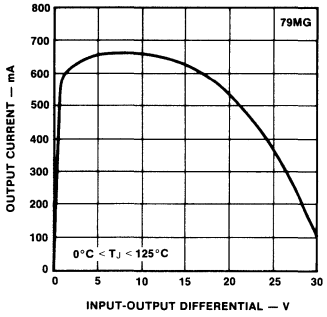
Performance Curves For μA78MG (Cont.)

Line Transient Response

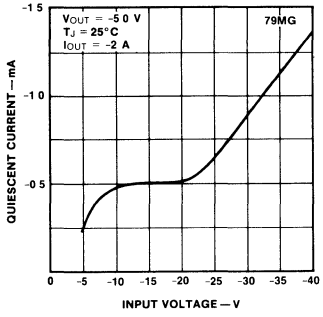


Typical Performance Curves for μA79MG

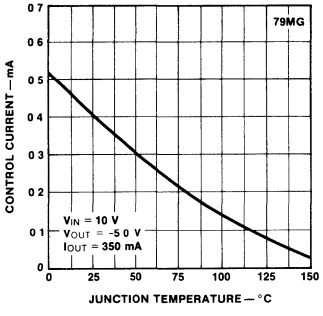
Peak Output Current as a Function of Input-Output Differential Voltage



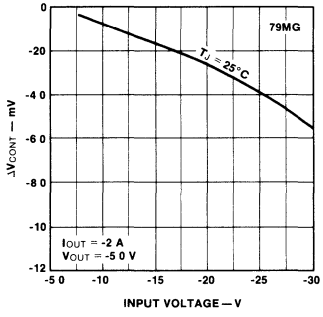
Quiescent Current as a Function of Input Voltage



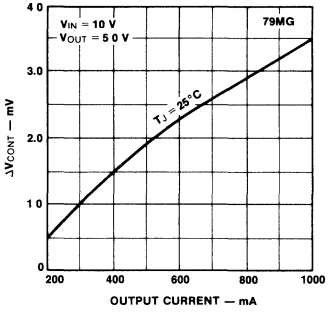
Control Current as a Function of Temperature



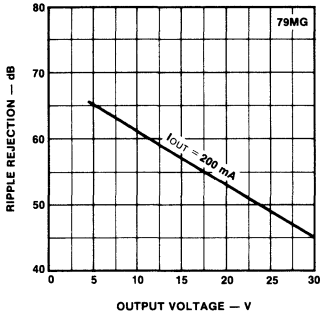
Differential Control Voltage as a Function of Input Voltage



Differential Control Voltage as a Function of Output Current

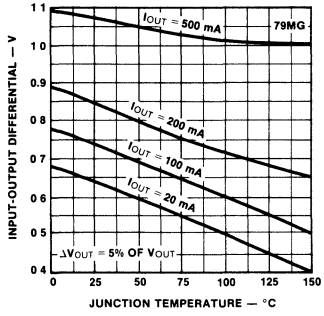


Ripple Rejection as a Function of Output Voltage

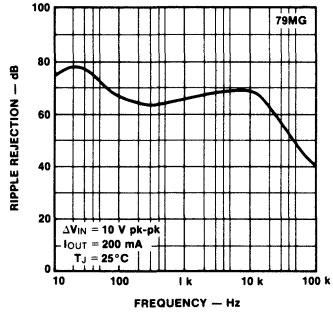


Performance Curves For μA79MG (Cont.)

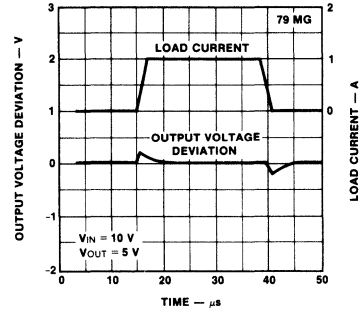
Dropout Voltage as a Function of Junction Temperature



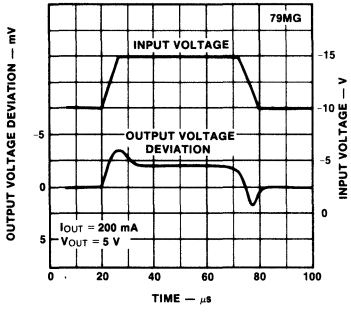
Ripple Rejection as a Function of Frequency



Load Transient Response

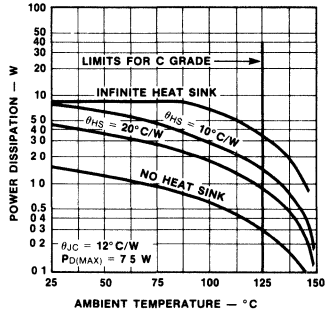


Line Transient Response



μA78MG and μA79MG Power Watt (U1)

Worst Case Power Dissipation Versus Ambient Temperature



Design Considerations

The 78MG and 79MG variable voltage regulators have an output voltage which varies from $V_{CONTROL}$ to typically $V_{IN} - 2$ V by $V_{OUT} = V_{CONTROL} \frac{(R1 + R2)}{R2}$.

The nominal reference in the 78MG is 5.0 V and 79MG is −2.23 V. If we allow 1.0 mA to flow in the control string to eliminate bias current effects, we can make R2 = 5 kΩ in the 78MG. The output voltage is then: V_{OUT} = (R1 + R2) Volts, where R1 and R2 are in kΩs.

Example: If R2 = 5 kΩ and R1 = 10 kΩ then V_{OUT} = 15 V nominal, for the 78MG;
R2 = 2.2 kΩ and R1 = 12.8 kΩ then V_{OUT} = −15.2 V nominal, for the 79MG.

By proper wiring of the feedback resistors, load regulation of the devices can be improved significantly.

Both 78MG and 79MG regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typical θ_{JC}	Max θ_{JC}	Typical θ_{JA}	Max θ_{JA}
Power Watt	8.0	12.0	70	75

$$P_{D(Max)} = \frac{T_{J(Max)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J(Max)} - T_A}{\theta_{JA}}$$

(Without a heat sink) $\theta_{CA} = \theta_{CS} + \theta_{SA}$

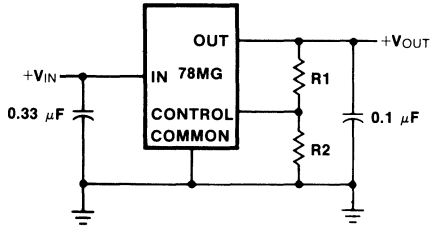
Solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$
or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-case thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink thermal resistance
θ_{SA} = Heat sink-to-ambient thermal resistance
θ_{JA} = Junction-to-ambient thermal resistance

Typical Applications for μA78MG
Bypass capacitors are recommended for stable operation of the μA78MG over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

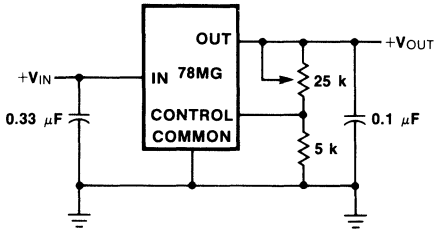
The bypass capacitors, (0.33 μF on the input, 0.1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Basic Positive Regulator

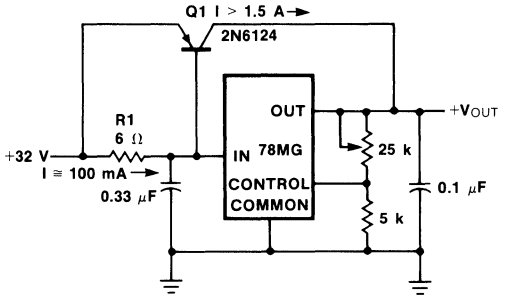


$$V_{OUT} = V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

Positive 5 to 30 V Adjustable Regulator

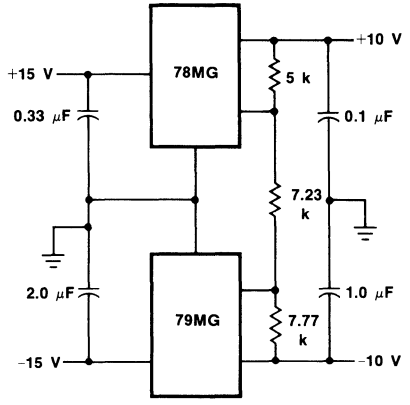


Positive 5 to 30 V Adjustable Regulator
$I_{OUT} > 1.5A$



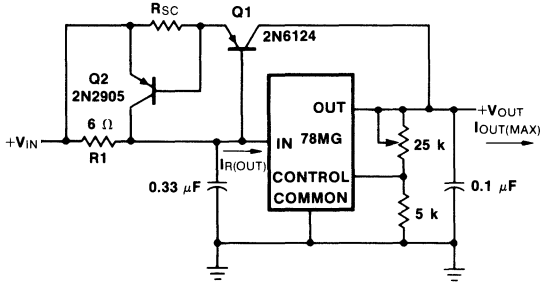
$$R1 = \frac{\beta V_{BE(Q1)}}{I_{R(Max)}(\beta) - I_{(OUT)}}$$

± 10 V, 500 mA Dual Tracking Regulator



Note
External series pass device is not short circuit protected.

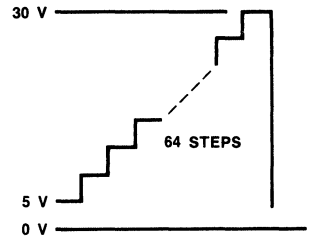
Positive High-Current Short-Circuit Protected Regulator



$$R1 = \frac{\beta V_{BE(Q1)}}{V_{R(Max)}(\beta + 1) - I_{OUT(Max)}}$$

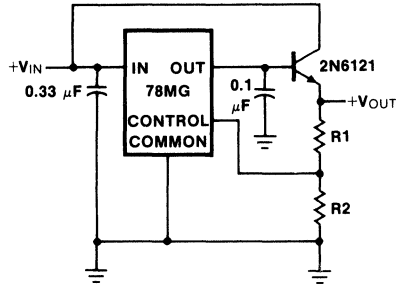
If load is not ground referenced, connect reverse biased diodes from outputs to ground.

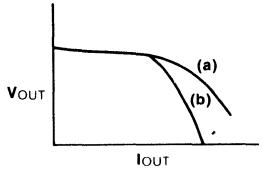
Output Waveform



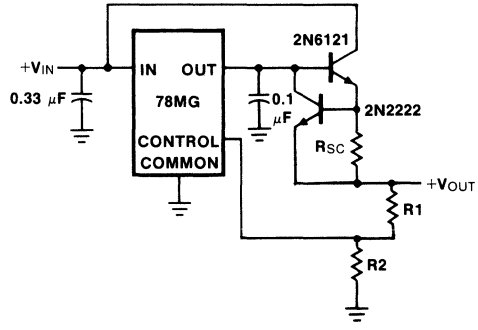
Positive High-Current Voltage Regulator

External Series Pass (a)





Short-Circuit Limit (b)

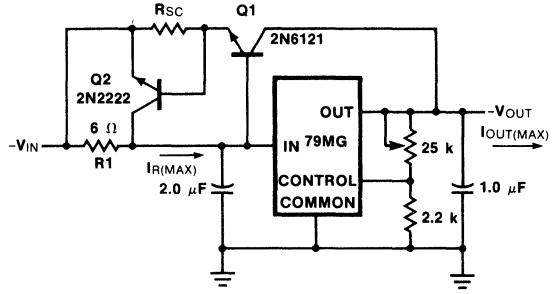


Typical Applications for 79MG

Bypass capacitors are recommended for stable operation of the μA79MG over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

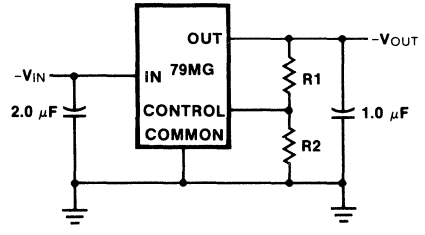
The bypass capacitors, (2 μF on the input, 1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Negative High-Current Short-Circuit Protected Regulator



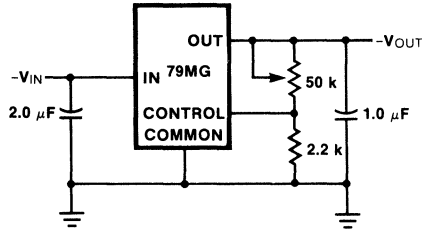
$$R1 = \frac{\beta V_{BE(Q1)}}{I_{R(Max)}\,(\beta) - I_{OUT(Max)}}$$

Basic Negative Regulator

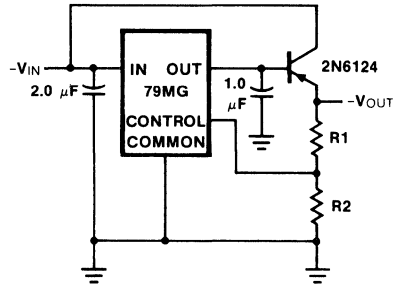


$$V_{OUT} = -V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

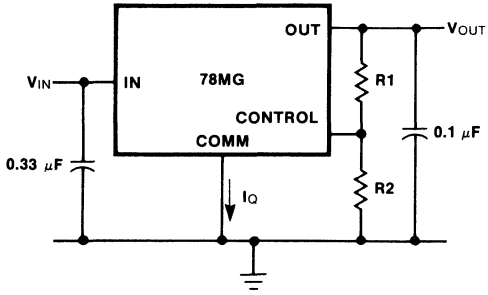
−30 V to −2.2 V Adjustable Regulator



Negative High-Current Voltage Regulator External Series Pass



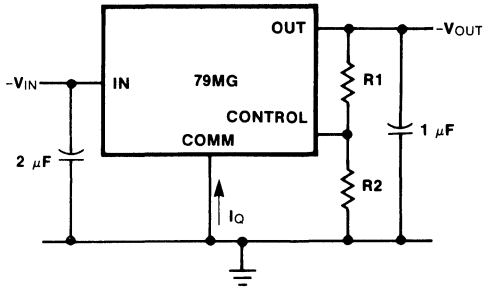
78MG Test Circuit 1



$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right)V_{CONTROL}$$

$V_{CONTROL}$ Nominally = 5 V

79MG Test Circuit 2



$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right)V_{CONTROL}$$

$V_{CONTROL}$ Nominally = −2.23 V

Recommended R2 current ≈ 1 mA
∴R2 = 5 kΩ (78MG)
R2 = 2.2 kΩ (79MG)

2

FAIRCHILD
A Schlumberger Company

μA723 Precision Voltage Regulator

Linear Products

Description

The μA723 is a Monolithic Voltage Regulator constructed using the Fairchild Planar epitaxial process. The device consists of a temperature-compensated reference amplifier, error amplifier, power-series pass transistor and current-limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

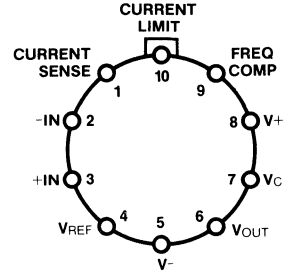
- **POSITIVE OR NEGATIVE SUPPLY OPERATION**
- **SERIES, SHUNT, SWITCHING OR FLOATING OPERATION**
- **0.01% LINE AND LOAD REGULATION**
- **OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 V**
- **OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR**

Absolute Maximum Ratings

Pulse Voltage from V+ to V−, (50 ms) (μA723)	50 V
Continuous Voltage from V+ to V−	40 V
Input/Output Voltage Differential	40 V
Differential Input Voltage	±5 V
Voltage Between Non-Inverting Input and V−	+8 V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note)	
Metal	800 mW
DIP	1000 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA723)	−55°C to +125°C
Commercial (μA723C)	0°C to +70°C
Pin Temperature (Soldering)	
Metal, Ceramic DIP (60 s)	300°C
Molded DIP (10 s)	260°C

Notes on following pages.

Connection Diagram 10-Pin Metal



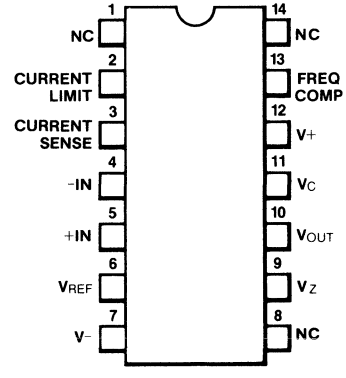
(Top View)

Pin 5 connected to case.

Order Information

Type	Package	Code	Part No.
μA723	Metal	5X	μA723HM
μA723C	Metal	5X	μA723HC

Connection Diagram 14-Pin DIP

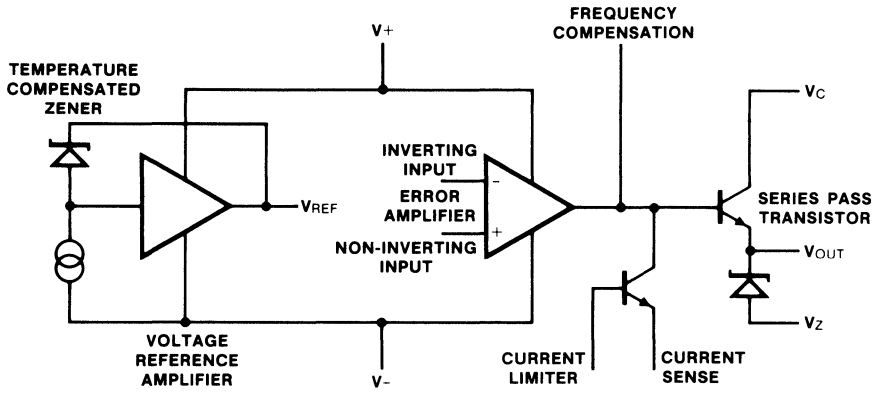


(Top View)

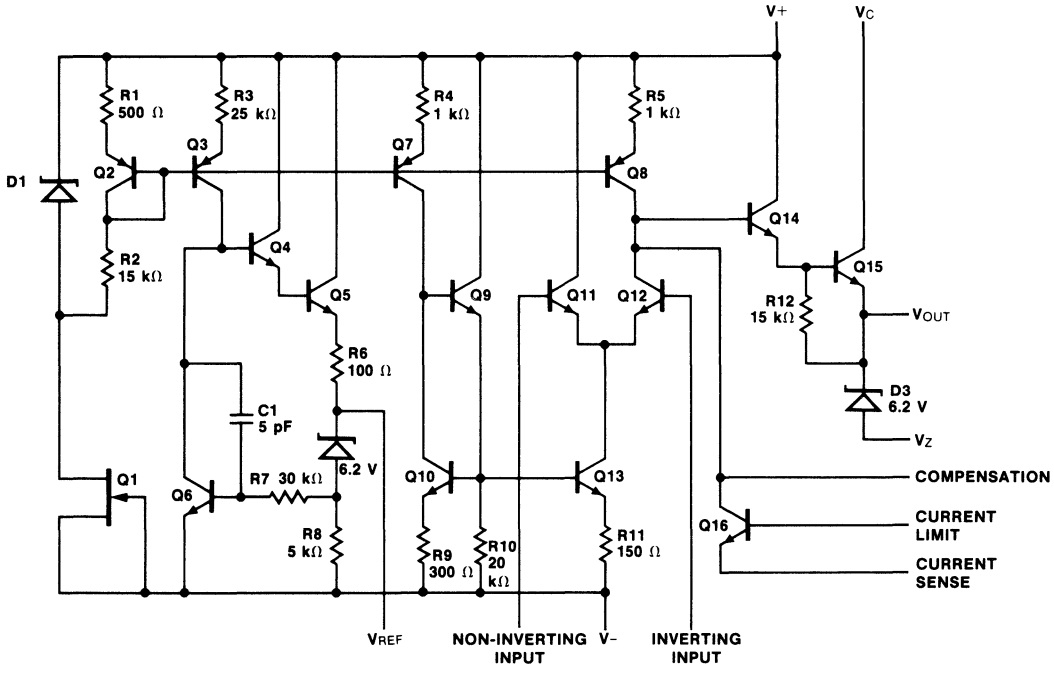
Order Information

Type	Package	Code	Part No.
μA723	Ceramic DIP	6B	μA723DM
μA723C	Ceramic DIP	6B	μA723DC
μA723C	Molded DIP	9B	μA723PC

Block Diagram



Equivalent Circuit



Note

1. Rating applies to ambient temperatures up to 25°C. Above 25°C ambient derate based on the following thermal resistance values:

	θJA	
	*Typ	Max
TO-5	150	190
Molded DIP	80	90
Ceramic DIP	95	105

μA723
Electrical Characteristic $T_A = 25°C$, $V_{IN} = V+ = V_C = 12$ V, $V- = 0$, $V_{OUT} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, C1 = 100 pF, $C_{REF} = 0$, unless otherwise specified. Divider impedance as seen by error amplifier ≤ 10 kΩ connected shown in *Figure 1*. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

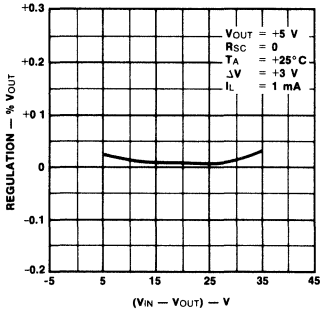
Characteristic	Condition	Min	Typ	Max	Unit
Line Regulation	V_{IN} = 12 V to V_{IN} = 15 V		0.01	0.1	$\%V_O$
	V_{IN} = 12 V to V_{IN} = 40 V		0.02	0.2	$\%V_O$
	$-55°C \leq T_A \leq +125°C$, V_{IN} = 12 V to V_{IN} = 15 V			0.3	$\%V_O$
Load Regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.15	$\%V_O$
	$-55°C \leq T_A \leq +125°C$, I_L = 1 mA to I_L = 50 mA			0.6	$\%V_O$
Ripple Rejection	f = 50 Hz to 10 kHz		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86		dB
Average Temperature Coefficient of Output Voltage	$-55°C \leq T_A \leq +125°C$		0.002	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10 Ω, $V_O = 0$		65		mA
Reference Voltage	I_{REF} = 0.1 mA	6.95	7.15	7.35	V
Reference Voltage Change With Load	I_{REF} = 0.1 mA to 5 mA			20	mV
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, V_{IN} = 30 V		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input/Output Voltage Differential		3.0		38	V

μA723C
Electrical Characteristic $T_A = 25°C$, $V_{IN} = V+ = V_C = 12$ V, $V- = 0$, $V_{OUT} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, C1 = 100 pF, $C_{REF} = 0$, unless otherwise specified. Divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in *Figure 1*. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

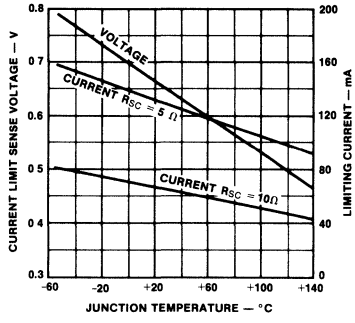
Characteristic	Condition	Min	Typ	Max	Unit
Line Regulation	$V_{IN} = 12$ V to $V_{IN} = 15$ V		0.01	0.1	$\%V_O$
	$V_{IN} = 12$ V to $V_{IN} = 40$ V		0.1	0.5	$\%V_O$
	$0°C \leq T_A \leq 70°C$, $V_{IN} = 12$ V to $V_{IN} = 15$ V			0.3	$\%V_O$
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		0.03	0.2	$\%V_O$
	$0°C \leq T_A \leq 70°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	$\%V_O$
Ripple Rejection	f = 50 Hz to 10 kHz		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$0°C \leq T_A \leq 70°C$		0.003	0.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10$ Ω, $V_O = 0$		65		mA
Reference Voltage	$I_{REF} = 0.1$ mA	6.80	7.15	7.50	V
Reference Voltage Change With Load	$I_{REF} = 0.1$ mA to 5 mA			20	mV
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30$ V		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input/Output Voltage Differential		3.0		38	V

Typical Performance Curves for μA723 and μA723C

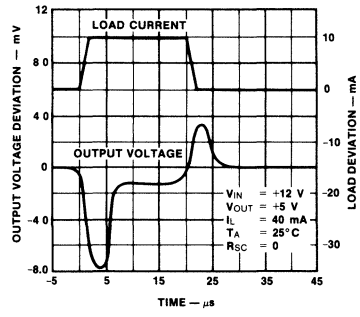
Line Regulation as a Function of Input/Output Voltage Differential



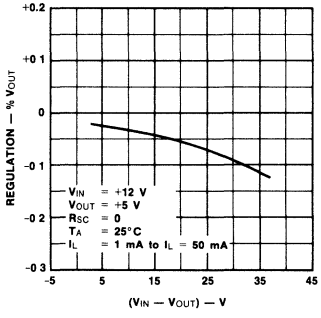
Current Limiting Characteristics as a Function of Junction Temperature



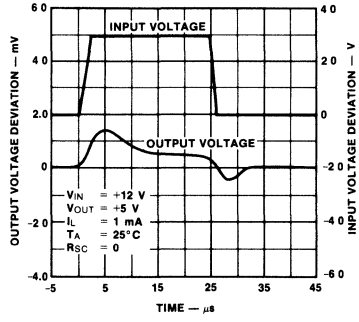
Load Transient Response



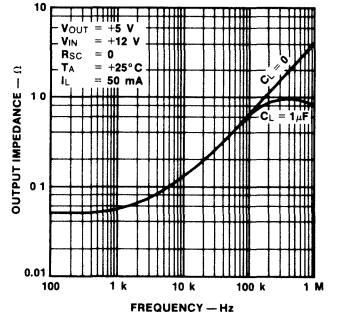
Load Regulation as a Function of Input/Output Voltage Differential



Line Transient Response

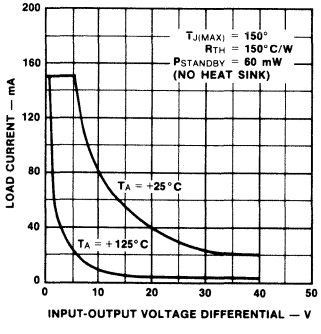


Output Impedance as a Function of Frequency

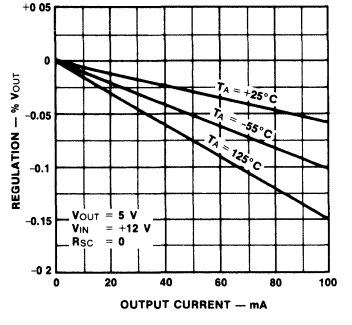


Typical Performance Curves for μA723

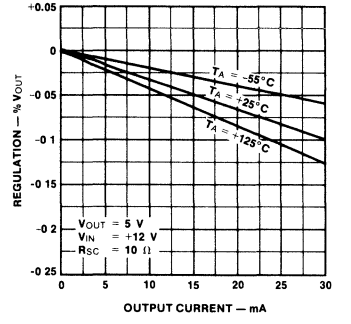
Maximum Load Current as a Function of Input-Output Voltage Differential



Load Regulation Characteristics Without Current Limiting

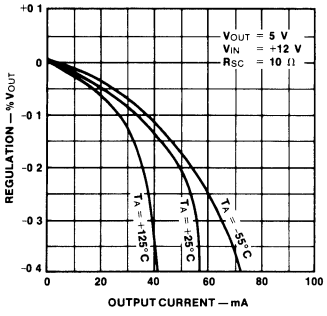


Load Regulation Characteristics With Current Limiting

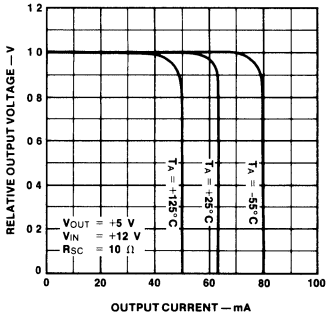


Typical Performance Curves (Cont.)

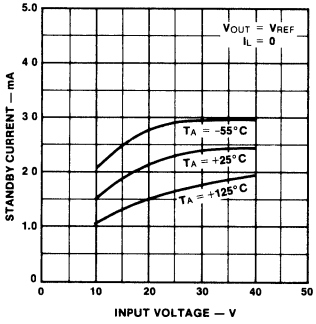
Load Regulation Characteristics With Current Limiting



Current Limiting Characteristics

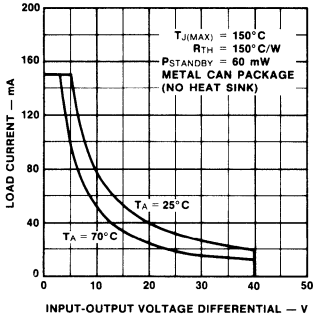


Standby Current Drain as a Function of Input Voltage

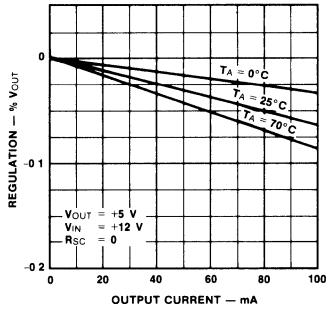


Typical Performance Curves for μA723C

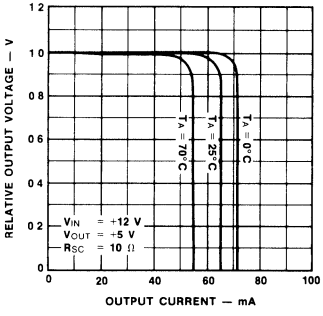
Maximum Load Current as a Function of Input/Output Voltage Differential



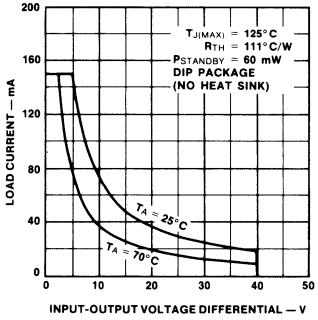
Load Regulation Characteristics Without Current Limiting



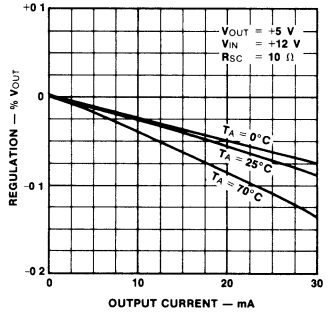
Current Limiting Characteristics



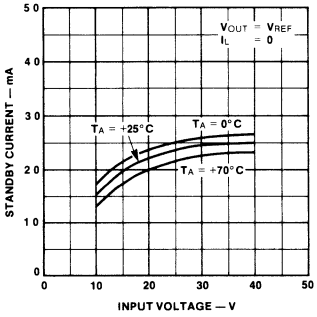
Maximum Load Current as a Function of Input/Output Voltage Differential



Load Regulation Characteristics With Current Limiting

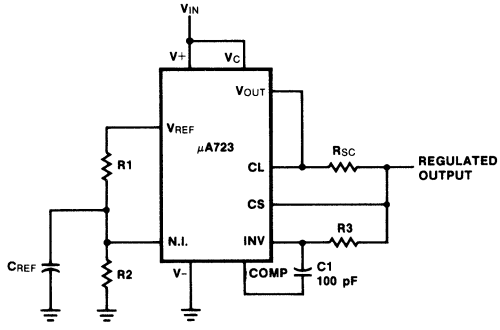


Standby Current Drain as a Function of Input Voltage



Typical Applications

Fig. 1 Basic Low Voltage Regulator (V_{OUT} = 2 to 7 V)



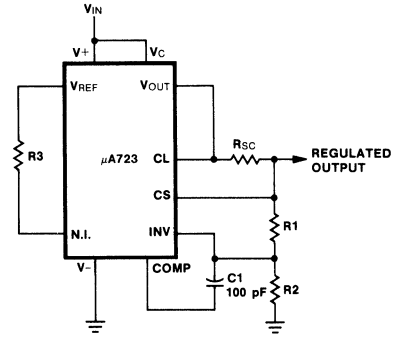
Typical Performance

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

Note

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

Fig. 2 Basic High Voltage Regulator (V_{OUT} = 7 to 37 V)



Typical Performance

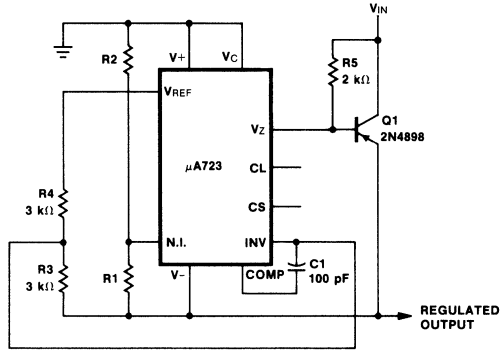
Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L = 50 mA)	4.5 mV

Note

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Fig. 3 Negative Voltage Regulator

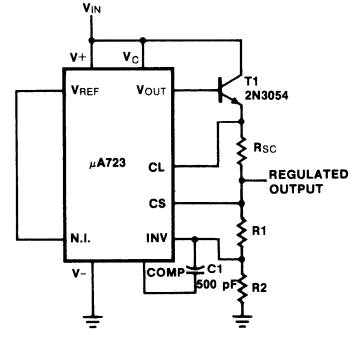


Typical Performance

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 3 V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

Note 4

Fig. 4 Positive Voltage Regulator (External npn Pass Transistor)



Typical Performance

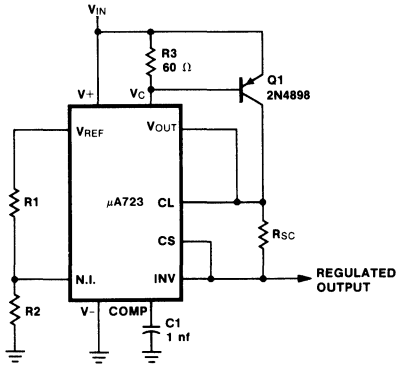
Regulated Output Voltage	+15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L = 1 A)	15 mV

Notes

1. Figures in parentheses may be used if R1/R2 divider is placed on opposite side of error amp.
2. Replace R1/R2 in figures with divider shown in *Figure 8.*
3. V+ must be connected to a +3 V or greater supply.
4. For metal can applications where V_Z is required, an external 6.2 V zener diode should be connected in series with V_{OUT}

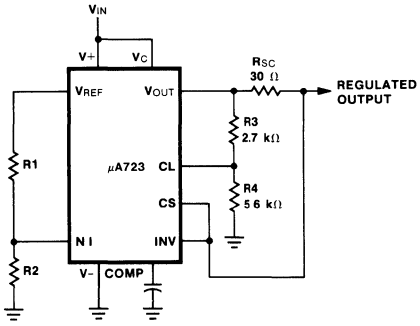
Typical Applications (Cont.)

Fig. 5 Positive Voltage Regulator (External pnp Pass Transistor)



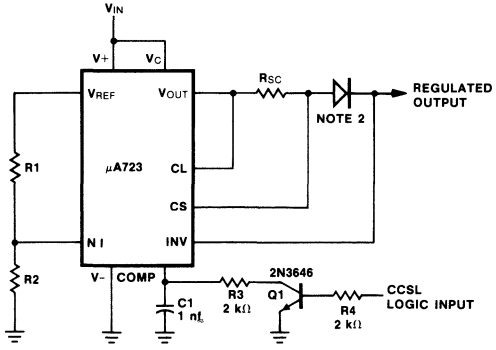
Typical Performance	
Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 1 A)	5 mV

Fig. 6 Foldback Current Limiting



Typical Performance	
Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Short-Circuit Current	20 mA

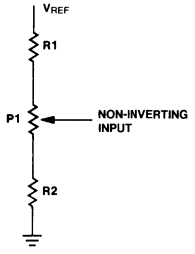
Fig. 7 Remote Shutdown Regulator with Current Limiting



Notes
Current limit transistor may be used for shutdown if current limiting is not required. Add if $V_{OUT} > 10$ V

Typical Performance	
Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

Fig. 8 Output Voltage Adjust



FAIRCHILD

A Schlumberger Company

μA105 • μA305 μA305A • μA376 Voltage Regulators

Linear Products

Description

The 105/305/305A/376 are Monolithic Positive Voltage Regulators constructed using the Fairchild Planar epitaxial process. Applications for these devices include both linear and switching regulator circuits with output voltages greater than 4.5 V. These devices will not oscillate when confronted with varying resistive and reactive loads and will start reliably regardless of the load within the ratings of the circuit. They also feature fast response to both load and line transients. Used independently, the 105/305 will supply 12 mA, the 305A, 45 mA and 376, 25 mA. The 105 is specified for the military temperature range (−55°C to +125°C) and the 305/376/305A are specified for 0°C to +70°C operation. The 105/305/305A are in an 8-pin TO-5 package and the 376 is available in the space and cost saving DIP.

- **LOW STANDBY CURRENT DRAIN**
- **ADJUSTABLE OUTPUT VOLTAGE FROM 4.5 TO 40 V**
- **HIGH OUTPUT CURRENTS EXCEEDING 10 A WITH EXTERNAL COMPONENTS**
- **LOAD REGULATION BETTER THAN 0.1%, FULL LOAD WITH CURRENT LIMITING**
- **DC LINE REGULATION GUARANTEED AT 0.03%/V**
- **RIPPLE REJECTION OF 0.01%/V**

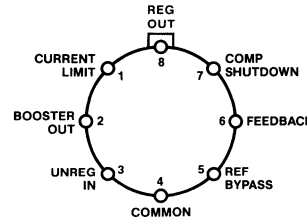
Absolute Maximum Ratings

Input Voltage	
μA105, μA305A	50 V
μA305, μA376	40 V
Input/Output Voltage Differential	40 V
Internal Power Dissipation (Note 1)	
μA105, μA305,	500 mW
μA305A, μA376	450 mW
Operating Temperature Range	
Military (μA105)	−55°C to +125°C
Commercial (μA305, μA305A, μA376)	0°C to 70°C
Storage Temperature Range	
Metal	−65°C to +150°C
DIP	−55°C to +125°C
Pin Temperature	
Metal soldering (60 s)	300°C
DIP Soldering (10 s)	260°C

Notes

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.25 mW/°C for the metal can and 5.6 mW/°C for the mini Dip.

Connection Diagram 8-Pin Metal Package

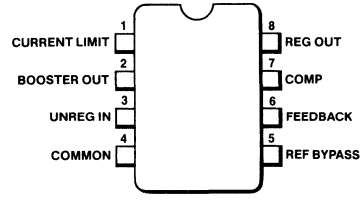


(Top View)

Order Information

Type	Package	Code	Part No.
μA105	Metal	5W	μA105HM
μA305	Metal	5W	μA305HC
μA305A	Metal	5W	μA305AHC

Connection Diagram 8-Pin DIP

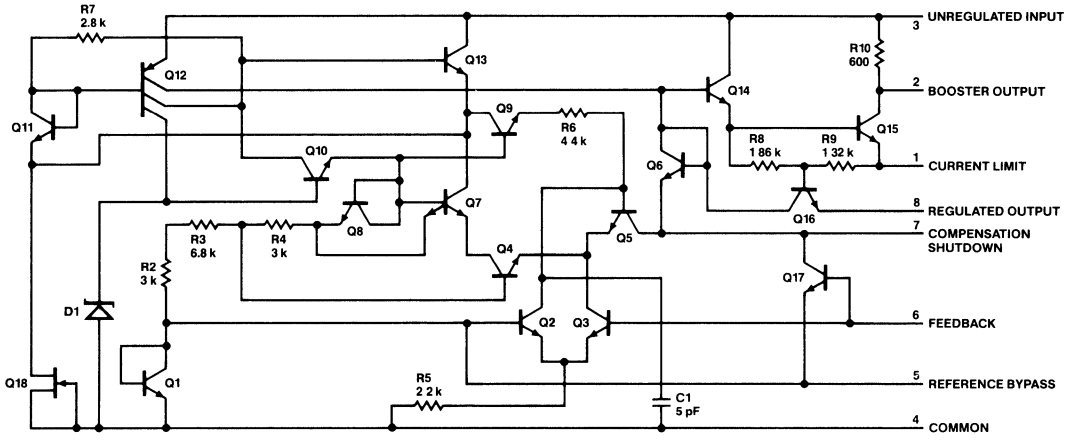


(Top View)

Order Information

Type	Package	Code	Part No.
μA376	Molded DIP	9T	μA376TC

Equivalent Circuit



Pin Connections Shown are for Metal Package

μA105
Electrical Characteristics $T_A = 25°C$ unless otherwise specified (Note 2)

Characteristic	Condition		Min	Typ	Max	Unit
Input Voltage Range			8.5		50	V
Output Voltage Range			4.5		40	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_L \leq 12$ mA	$R_{SC} = 10\ \Omega$, $T_A = 25°C$		0.02	0.05	%
		$R_{SC} = 10\ \Omega$, $T_A = 125°C$		0.03	0.1	%
		$R_{SC} = 10\ \Omega$, $T_A = -55°C$		0.03	0.1	%
Line Regulation	$V_{IN} - V_O \leq 5$ V			0.025	0.06	%/V
	$V_{IN} - V_O > 5$ V			0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz			0.003	0.01	%/V
Temperature Stability (Note 5)	$-55°C \leq T_A \leq 125°C$			0.3	1.0	%
Feedback Sense Voltage			1.63	1.7	1.81	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz	$C_{REF} = 0$		0.005		%
		$C_{REF} > 0.1\ \mu F$		0.002		%
Current Limit Sense Voltage (Note 4)	$R_{SC} = 10\Omega$, $T_A = 25°C$, $V_O = 0$ V		225	300	375	mV
Standby Current Drain	$V_{IN} = 50$ V			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

Notes

2. These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
4. With no external pass transistor.
5. Temperature Stability is defined as the percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

μA305
Electrical Characteristics $T_A = 25°C$ unless otherwise specified (Note 2)

Characteristic	Condition		Min	Typ	Max	Unit
Input Voltage Range			8.5		40	V
Output Voltage Range			4.5		30	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_L \leq 12$ mA	$R_{SC} = 10\ \Omega$, $T_A = 25°C$		0.02	0.05	%
		$R_{SC} = 15\ \Omega$, $T_A = 70°C$		0.03	0.1	%
		$R_{SC} = 10\ \Omega$, $T_A = 0°C$		0.03	0.1	%
Line Regulation	$V_{IN} - V_O \leq 5$ V			0.025	0.06	%/V
	$V_{IN} - V_O > 5$ V			0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz			0.003	0.01	%/V
Temperature Stability (Note 5)	$0°C \leq T_A \leq 70°C$			0.3	1.0	%
Feedback Sense Voltage			1.63	1.7	1.81	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz	$C_{REF} = 0$		0.005		%
		$C_{REF} > 0.1\ \mu F$		0.002		%
Current Limit Sense Voltage (Note 4)	$R_{SC} = 10\ \Omega$, $T_A = 25°C$, $V_O = 0$ V		225	300	375	mV
Standby Current Drain	$V_{IN} = 40$ V			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

μA305A
Electrical Characteristics $T_A = 25°C$ unless otherwise specified (Note 2)

Characteristic	Condition		Min	Typ	Max	Unit
Input Voltage Range			8.5		50	V
Output Voltage Range			4.5		40	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation	$0 \leq I_L \leq 45$ mA	$R_{SC} = 0\ \Omega$, $T_A = 25°C$		0.02	0.2	%
		$R_{SC} = 0\ \Omega$, $T_A = 70°C$		0.03	0.4	%
		$R_{SC} = 0\ \Omega$, $T_A = 0°C$		0.03	0.4	%
Line Regulation	$V_{IN} - V_O \leq 5$ V			0.025	0.06	%/V
	$V_{IN} - V_O > 5$ V			0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz			0.003		%/V
Temperature Stability (Note 5)	$0°C \leq T_A \leq 70°C$			0.3	1.0	%
Feedback Sense Voltage			1.55	1.7	1.85	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz	$C_{REF} = 0$		0.005		%
		$C_{REF} > 0.1\ \mu F$		0.002		%
Current Limit Sense Voltage (Note 4)	$R_{SC} = 10\ \Omega$, $T_A = 25°C$, $V_O = 0$ V		225	300	375	mV
Standby Current Drain	$V_{IN} = 50$ V			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

Notes on following page.

μA376
Electrical Characteristics $0°C \leq T_A \leq 70°C$

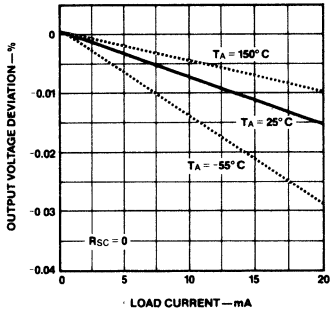
Characteristic	Condition		Min	Typ	Max	Unit
Input Voltage Range			9.0		40	V
Output Voltage Range			5.0		37	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation	$0 \leq I_L \leq 25$ mA	$R_{SC} = 0\ \Omega$, $T_A = 25°C$			0.2	%
		$R_{SC} = 0\ \Omega$, $T_A = 70°C$			0.5	%
		$R_{SC} = 0\ \Omega$, $T_A = 0°C$			0.5	%
Line Regulation	$T_A = 25°C$				0.03	%/V
	$0°C \leq T_A \leq 70°C$				0.1	%/V
Ripple Rejection	f = 120 Hz, $T_A = 25°C$				0.1	%/V
Standby Current Drain	$V_{IN} = 30$ V, $T_A = 25°C$				2.5	mA
Reference Voltage			1.60	1.72	1.80	V
Current Limit Sense Voltage				360		mV

Notes

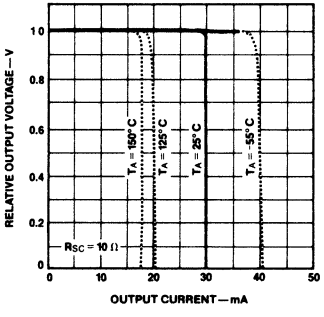
2. These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
4. With no external pass transistor.
5. Temperature Stability is defined as the percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Typical Performance Curves for μA105/μA305/μA305A

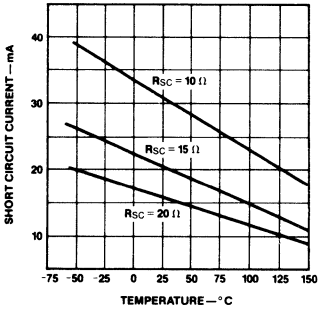
Load Regulation



Current Limiting Characteristics

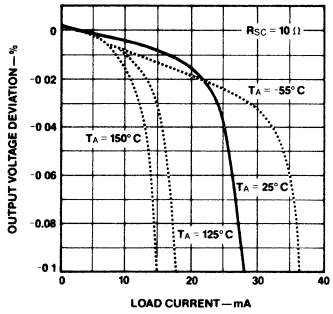


Short Circuit Current as a Function of Temperature

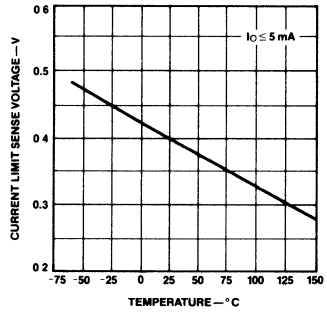


Performance Curves for μA105/μA305/μA305A (Cont.)

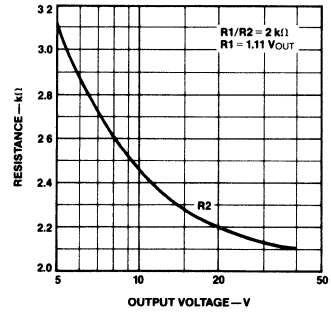
Current Limiting Characteristics



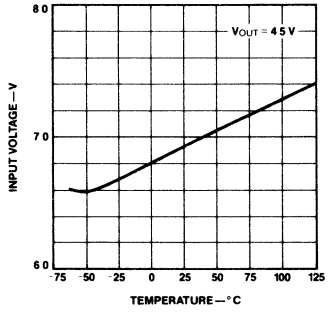
Current Limit Sense Voltage as a Function of Temperature



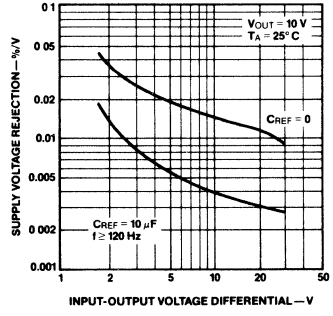
Optimum Divider Resistance Values



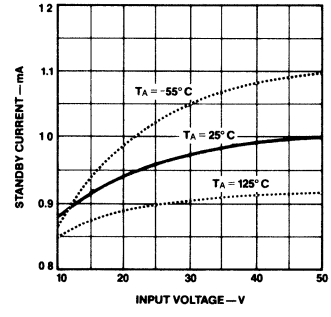
Minimum Input Voltage as a Function of Temperature



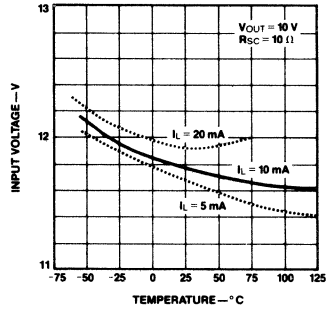
Supply Voltage Rejection as a Function of Input/Output Voltage Differential



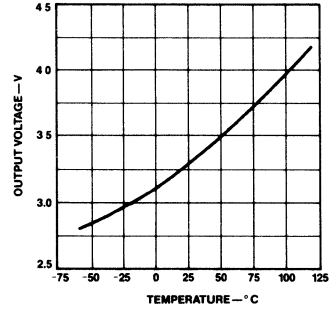
Standby Current Drain as a Function of Input Voltage



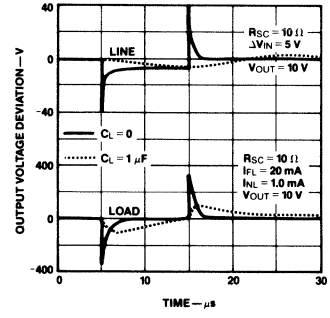
Regulator Dropout Voltage



Minimum Output Voltage as a Function of Temperature

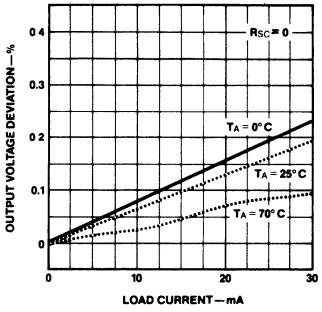


Transient Response

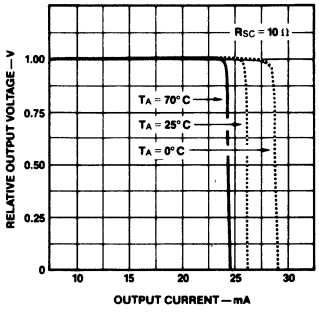


Typical Performance Curves for μA376

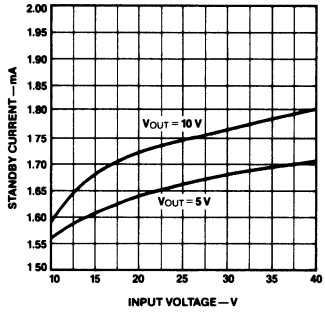
Load Regulation



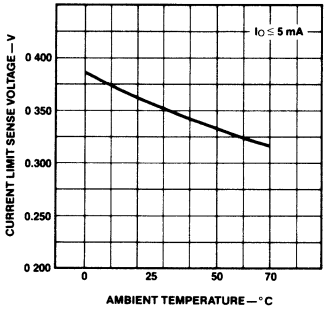
Current Limiting Characteristics



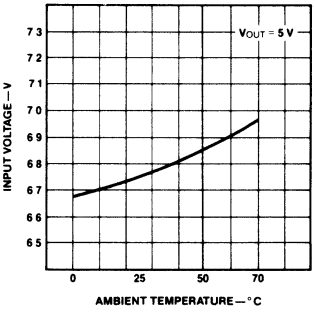
Standby Current Drain as a Function of Input Voltage T_A = 25°C



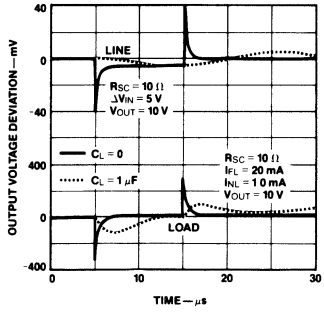
Current Limit Sense Voltage as a Function of Temperature



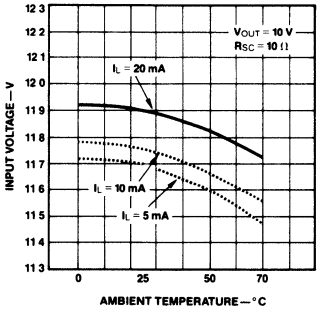
Minimum Input Voltage as a Function of Temperature



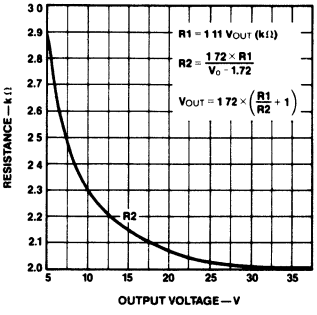
Transient Response



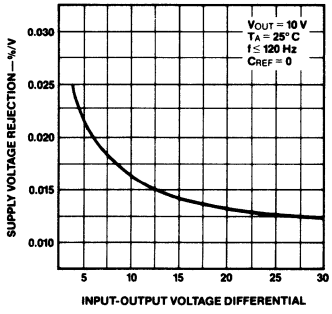
Regulator Dropout Voltage



Optimum Divider Resistance

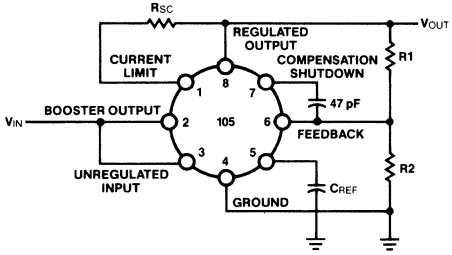


Supply Voltages Rejection as a Function of Input/Output Voltage Differential



Typical Applications

Basic Positive Regulator With Current Limiting



$$V_{OUT} \approx 1.72 \frac{R1 + R2}{R2} V$$

$$I_{SC} \approx \frac{V_{SENSE}}{R_{SC}} mA$$

FAIRCHILD
A Schlumberger Company

μA117 • μA217 • μA317 3-Terminal Positive Adjustable Regulators

Linear Products

Description

The μA117 is a 3-Terminal Adjustable Positive Voltage Regulator capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current-limiting, thermal-shutdown and safe-area compensation, making it essentially blow-out proof.

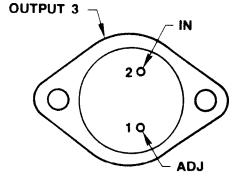
The μA117 series serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, and a programmable output regulator; or by connecting a fixed resistor between the adjustment and output, the μA117 series can be used as a precision current regulator.

- **OUTPUT CURRENT IN EXCESS OF 1.5 A IN TO-3 AND TO-220 PACKAGES**
- **OUTPUT ADJUSTABLE BETWEEN 1.2 V AND 37 V**
- **INTERNAL THERMAL-OVERLOAD PROTECTION**
- **INTERNAL SHORT-CIRCUIT CURRENT-LIMITING CONSTANT TEMPERATURE**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**
- **FLOATING OPERATION FOR HIGH-VOLTAGE APPLICATIONS**
- **STANDARD 3-PIN TRANSISTOR PACKAGES**
- **AVAILABLE IN MILITARY TEMPERATURE RANGE**

Absolute Maximum Ratings

Input-Output Voltage Differential	40 V_{dc}
Power Dissipation	Internally Limited
Operating Junction Temperature	
Military (μA117)	−55°C to +150°C
Automotive (μA217)	−40°C to +125°C
Commercial (μA317C)	0°C to +125°C
Storage Temperature	
TO-3 Steel	−65°C to +150°C
TO-220	−55°C to +150°C
Pin Temperature	
TO-3 Package	
(Soldering, 60 s Time Limit)	300°C
TO-220 Package	
(Soldering, 10 s Time Limit)	230°C

Connection Diagram
TO-3 Package

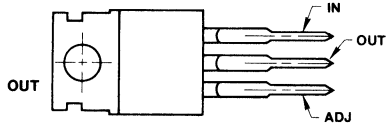


(Top View)

Order Information

Type	Package	Code	Part No.
μA317	Metal	HJ	μA317KC
μA117	Metal	HJ	μA117KM

Connection Diagram
TO-220 Package

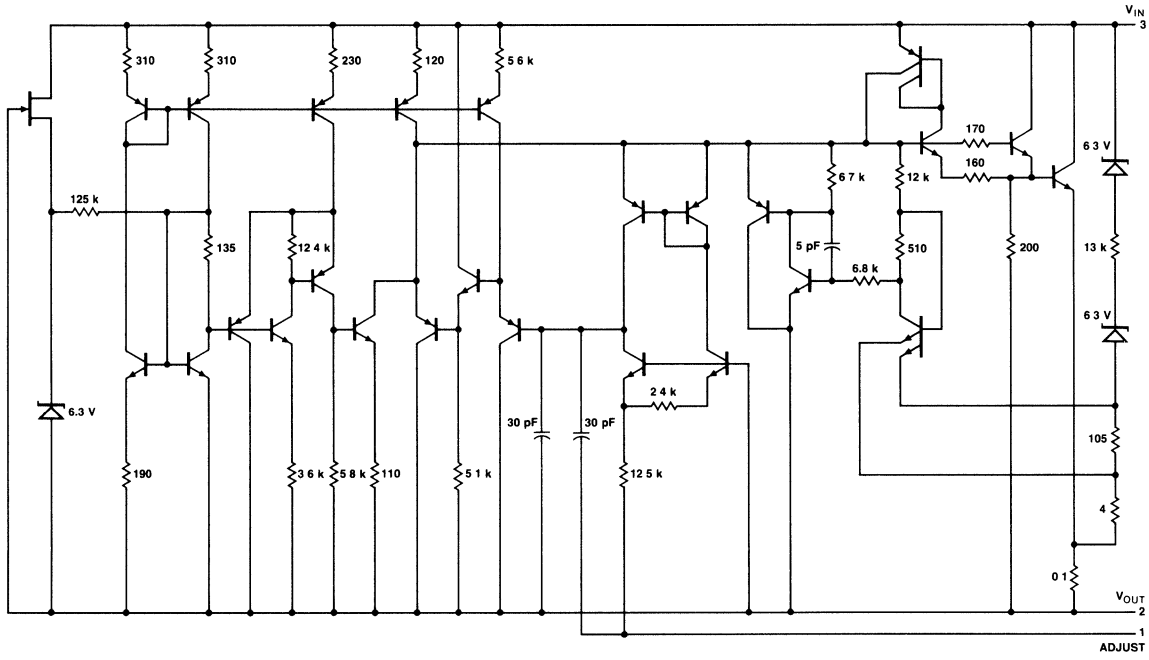


(Top View)

Order Information

Type	Package	Code	Part No.
μA317	Molded Power Pack	GH	μA317UC
μA217	Molded Power Pack	GH	μA217UV

Schematic Diagram



Electrical Characteristics $V_I - V_O = 5$ V; $I_O = 0.5$ A for K and U Packages
T_J = Operating Temperature (see Note 1); I_{Max} and P_{Max} per Note 2; unless otherwise specified.

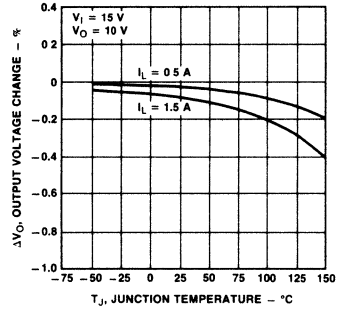
Symbol	Characteristic	Condition		μA117/217			μA317			Unit
				Min	Typ	Max	Min	Typ	Max	
Reg_{Line}	Line Regulation (Note 3, 7)	$T_A = 25°C$, $3\ V \le V_I - V_O \le 40\ V$			0.01	0.02		0.01	0.04	%/V
		$3\ V \le V_I - V_O \le 40\ V$			0.02	0.05		0.02	0.07	%/V
Reg_{Load}	Load Regulation (Note 3)	$T_A = 25°C$, $10\ mA \le I_O \le I_{Max}$	$V_O \le 5\ V$		5	15		5	25	mV
			$V_O \ge 5\ V$		0.1	0.3		0.1	0.5	$\%V_O$
		$10\ mA \le I_O \le I_{Max}$	$V_O \le 5\ V$		20	50		20	70	mV
			$V_O \ge 5\ V$		0.3	1		0.3	1.5	$\%V_O$
I_{Adj}	Adjustment Pin Current				50	100		50	100	μA
ΔI_{Adj}	Adjustment Pin Current Change	$2.5\ V \le V_I - V_O \le 40\ V$ $10\ mA \le I_L \le I_{Max}$, $P_D \le P_{Max}$			0.2	5		0.2	5	μA
V_{Ref}	Reference Voltage (Note 4)	$3\ V \le V_I - V_O \le 40\ V$ $10\ mA \le I_O \le I_{Max}$, $P_D \le P_{Max}$		1.20	1.25	1.30	1.20	1.25	1.30	V
T_S	Temperature Stability				0.7			0.7		$\%V_O$
$I_{L(Min)}$	Minimum Load Current to Maintain Regulation	$V_I - V_O = 40\ V$			3.5	5		3.5	10	mA
I_{Max}	Maximum Output Current	$V_I - V_O \le 15\ V$, $P_D \le P_{Max}$ K and U Packages		1.5	2.2		1.5	2.2		A
		$V_I - V_O = 40\ V$, $P_D \le P_{Max}$, $T_A = 25°C$ K and U Packages		0.25	0.4		0.15	0.4		
N	RMS Noise, % of V_O	$T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$			0.003			0.003		$\%V_O$
RR	Ripple Rejection (Note 5)	$V_O = 10\ V$, $f = 120\ Hz$	Without C_{Adj}		65			65		dB
			$C_{Adj} = 10\ \mu F$	66	80		66	80		
S	Long-Term Stability, $T_J = T_{high}$ (Note 6)	$T_A = 25°C$ for Endpoint Measurements			0.3	1		0.3	1	%1.0 k Hrs
$R_{\theta JC}$	Thermal Resistance Junction to Case	K Package (TO-3)			2.3	3		2.3	3	°C/W
		U Package (TO-220)						5		

Notes

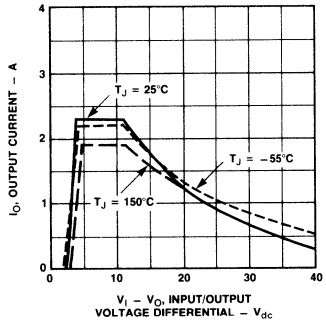
1. μA117 Operating Junction Temperature Range = −55°C to +150°C
   μA217 Operating Junction Temperature Range = −25°C to +120°C
2. I_{Max} = 1.5 A for K (TO-3) and U (TO-220) Packages
   P_{Max} = 20 W for K (TO-3) and U (TO-220) Packages
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. Selected devices with tightened tolerance reference voltage available.
5. C_{Adj}, when used, is connected between the adjustment pin and ground.
6. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
7. $I_{OUT} = 0.5$ A for $V_I - V_O \le 25$ V and I_{Max} for $V_I - V_O \ge 25$ V.

Typical Performance Curves

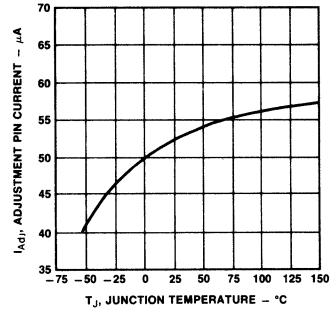
Load Regulation



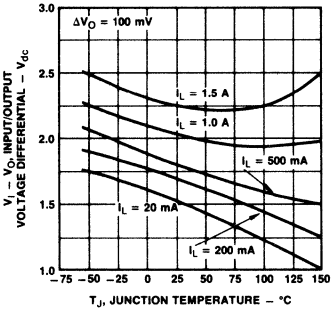
Current Limit



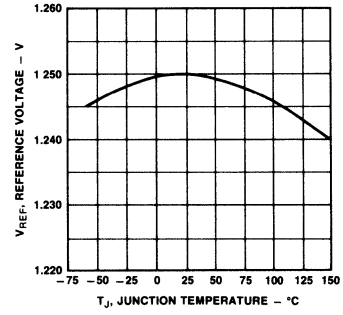
Adjustment Pin Current



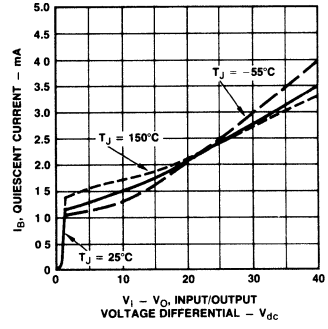
Dropout Voltage



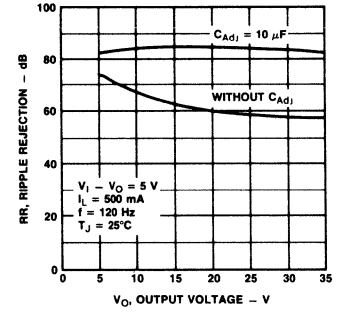
Temperature Stability



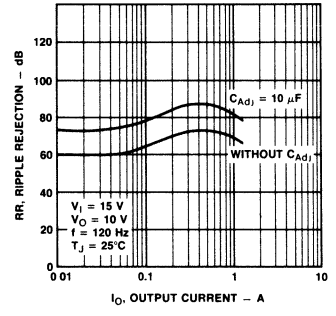
Minimum Operating Current



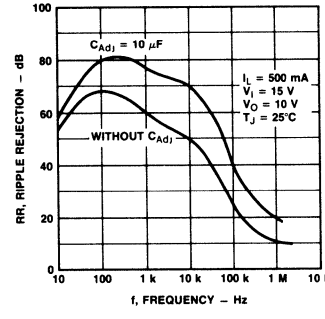
Ripple Rejection as a Function of Output Voltage



Ripple Rejection as a Function of Output Current

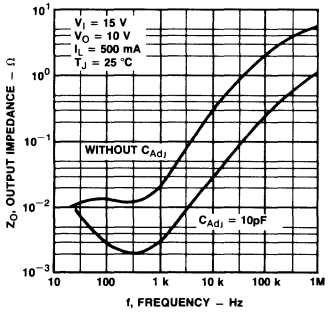


Ripple Rejection as a Function of Frequency

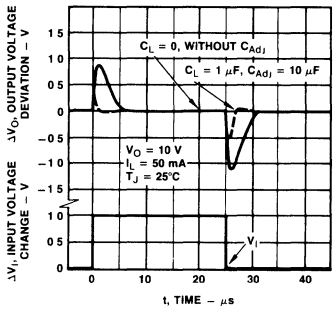


Typical Performance Curves (Cont.)

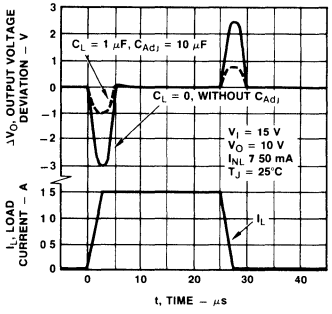
Output Impedance



Line Transient Response



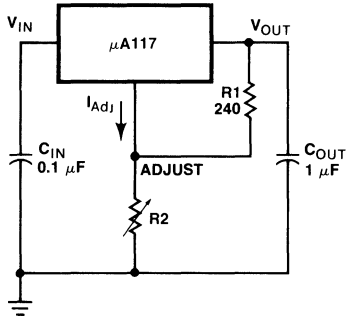
Load Transient Response



2

Typical Applications

Standard Application



C_{IN} is required if regulator is located an appreciable distance from power supply filter.

$$V_{OUT} = 1.25\ V\ \left(1 + \frac{R2}{R1}\right) + I_{Adj}\ R2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

Basic Circuit Operation

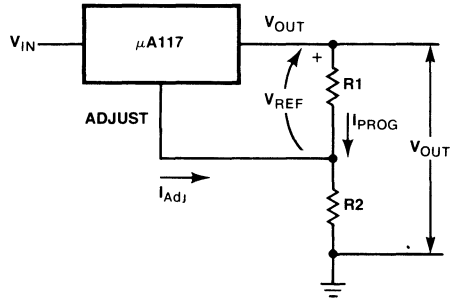
The μA117 is a 3-terminal floating regulator. In operation, the μA117 develops and maintains a nominal 1.25 V reference (V_{REF}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{Prog}) by R1 (see *Figure 1*), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{OUT} = V_{REF}\ \left(1 + \frac{R2}{R1}\right)\ + I_{Adj}\ R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the μA117 was designed to control I_{Adj} to less than 0 and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the μA117 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Fig. 1. Basic Circuit Configuration



V_{Ref} = 1.25 V TYPICAL

Load Regulation
The μA117 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors
A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{IN}) is recommended to reduce the sensitivity to input line impedance.

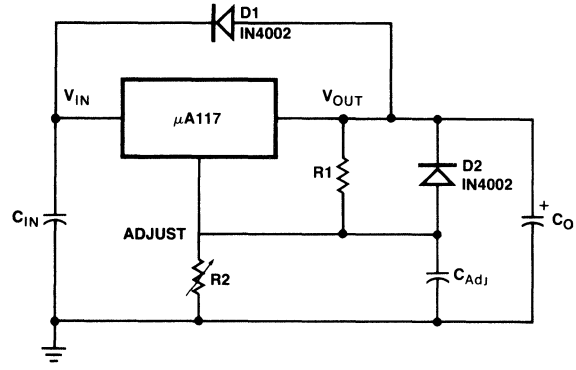
The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the μA117 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes
When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 2 shows the μA117 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25$ μF, $C_{Adj} > 10$ μF). Diode D1 prevents C_O from discharging through the IC during an input short circuit. Diode D2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Fig. 2. Voltage Regulator with Protection Diodes



FAIRCHILD

A Schlumberger Company

μA431
Adjustable Precision Shunt Regulator

Linear Products

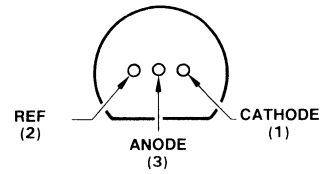
Description

The μA431 is a 3-terminal Adjustable Shunt Regulator with guaranteed temperature stability over the entire temperature range of operation. The output voltage may be set at any level greater than 2.5 V (V_{REF}) up to 36 V merely by selecting two external resistors that act as a voltage divided network. Due to the sharp turn-on characteristics this device is an excellent replacement for many zener diode applications.

This product will operate over the entire temperature range of −55°C to +125°C. This includes the unique automotive range of −40°C to +85°C.

- **AVERAGE TEMPERATURE COEFFICIENT 50 ppm/°C**
- **TEMPERATURE COMPENSATED FOR OPERATION OVER THE FULL TEMPERATURE RANGE**
- **PROGRAMMABLE OUTPUT VOLTAGE**
- **FAST TURN-ON RESPONSE**
- **LOW OUTPUT NOISE**

Connection Diagram
TO-92 Package



(Top View)

Order Information

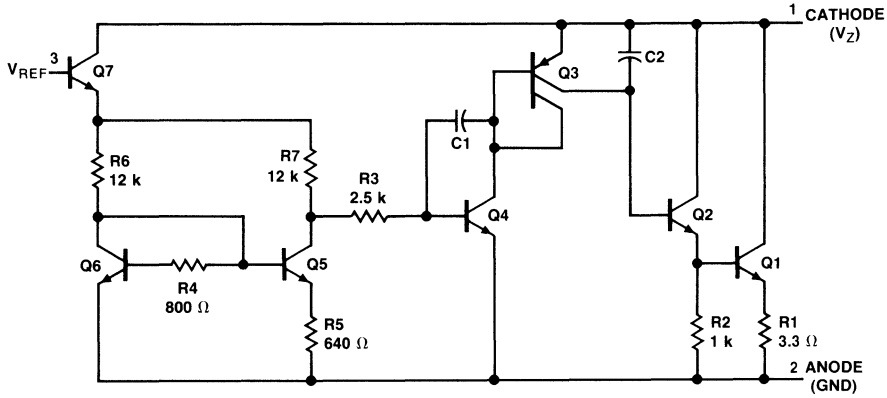
Type	Package	Code	Part No.
μA431C	Molded	EI	μA431AWC

Absolute Maximum Ratings

Cathode Voltage	37 V
Continuous Cathode Current	−10 mA to +150 mA
Reference Voltage	−.5 V
Reference Input Current	10 mA
Operating Temperature Range	
μA431C	0°C to +70°C
Storage Temperature Range	
TO-92 Molded	−55°C to +150°C
Power Dissipation	
TO-92 Molded	775 mW
Pin Temperature (Soldering)	
TO-92 Molded (10s)	260°C

Operating Conditions	Min	Max
Cathode Voltage, V_Z	V_{REF}	37 V
Cathode Current, I_Z	1 mA	100 mA

Equivalent Circuit

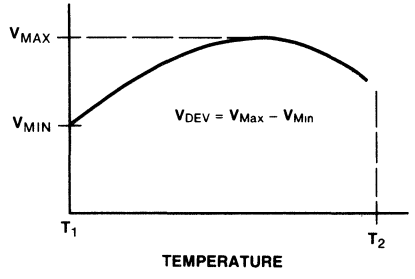


Electrical Characteristics At 25°C ambient temperature unless otherwise noted

Symbol	Characteristic	Condition		μA431C Min	μA431C Typ	μA431C Max	Unit
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, I_{IN} = 10 mA (*Figure 1*)		2.440	2.495	2.550	V
V_{DEV}	Deviation of Reference Input Voltage Over Temperature	$V_Z = V_{REF}$, I_{IN} = 10 mA, T_A = full range, See Note 1 (*Figure 1*)			8	17	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I_Z = 10 mA (*Figure 2*)	V_Z from V_{REF} to 10 V		−1.4	−2.7	mV/V
			V_Z from 10 V to 36 V		−1	−2	mV/V
I_{REF}	Reference Input Current	R_1 = 10 kΩ, R_2 = ∞, I_{IN} = 10 mA (*Figure 2*)			2	4	μA
αI_{REF}	Deviation of Reference Input Current over Temperature	R_1 = 10 kΩ, R_2 = ∞, I_{IN} = 10 mA, T_A = Full Range (*Figure 2*)			0.4	1.2	μA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$ (*Figure 1*)			0.4	1	mA
$I_{Z(OFF)}$	Off-State Current	V_Z = 36 V, V_{REF} = 0 V (*Figure 3*)			0.3	1	μA
r_Z	Dynamic Output Impedance	$V_Z = V_{REF}$, Frequency = 0 Hz, See Note 2 (*Figure 1*)				.75	Ω

Notes

1. Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range.



The average temperature coefficient of the reference input voltage, αVREF, is defined as:

$$\alpha V_{REF} \frac{ppm}{°C} = \pm \left[\frac{V_{Max} - V_{Min}}{V_{REF\ (at\ 25°C)}}\right]^{10^6} \frac{}{T_2 - T_1} = \pm \left[\frac{V_{DEV}}{V_{REF\ (at\ 25°C)}}\right]^{10^6} \frac{}{T_2 - T_1}$$

where $T_2 - T_1$ = full temperature change.

αV_{REF} can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV} = 8 mV, V_{REF} = 2495 mV, $T_2 - T_1$ = 70°C, slope is positive

$$\alpha V_{REF} = \frac{\left[\frac{8\ mV}{2495\ mV}\right]^{10^6}}{70°C} = +46\ ppm/°C$$

2. The dynamic output impedance, r_Z, is defined as:

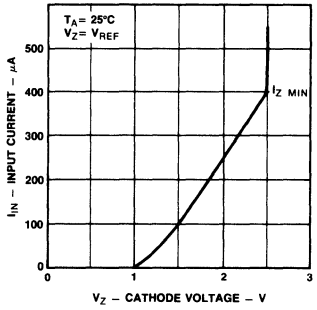
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see Figure 2), the dynamic output impedance of the overall circuit, r_Z', is defined as:

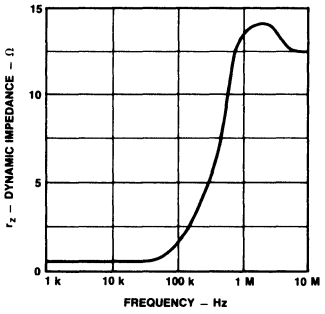
$$r_Z' = \frac{\Delta V_Z'}{\Delta I_Z'} \simeq \left[r_Z\ 1 + \frac{R1}{R2}\right]$$

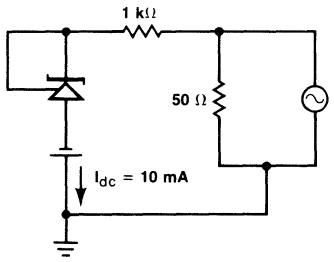
Typical Performance Curves

Input Current as a Function of V_Z

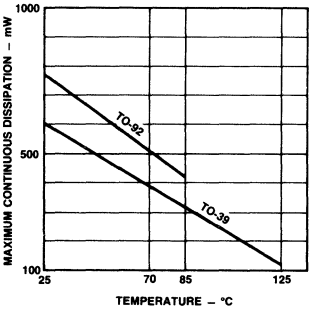


Dynamic Impedance as a Function of Frequency

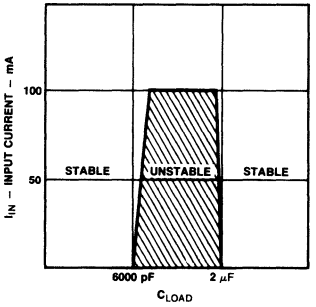




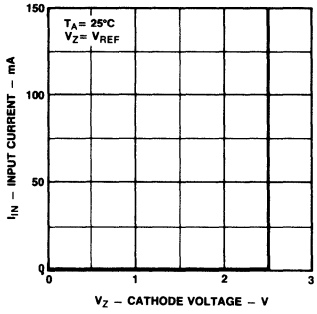
Thermal Information

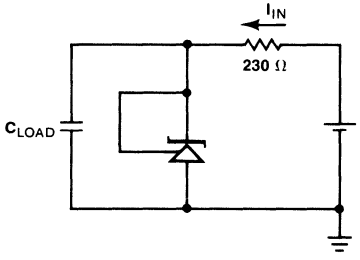


Range of Instability



Input Current as a Function of V_Z





DC Test Circuits

Fig. 1 Test Circuit For $V_Z = V_{REF}$

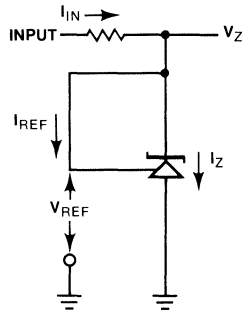
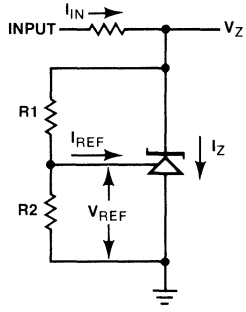
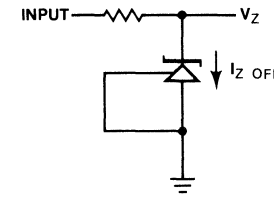


Fig. 2 Test Circuit For $V_Z > V_{REF}$



$V_Z = V_{REF} (1 + R1/R2) + I_{REF} \bullet R1$

Fig. 3 Test Circuit for Off-State Current



FAIRCHILD
A Schlumberger Company

μA78S40 Universal Switching Regulator Subsystem

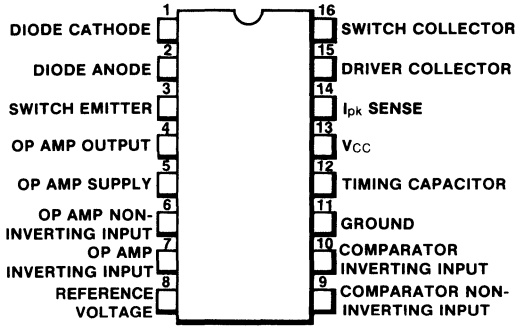
Linear Products

Description

The μA78S40 is a Monolithic Regulator Subsystem consisting of all the active building blocks necessary for switching regulator systems. The device consists of a temperature-compensated voltage reference, a duty-cycle controllable oscillator with an active current limit circuit, an error amplifier, high-current, high-voltage output switch, a power diode and an uncommitted operational amplifier. The device can drive external npn or pnp transistors when currents in excess of 1.5 A or voltages in excess of 40 V are required. The device can be used for step-down, step-up or inverting switching regulators as well as for series pass regulators. It features wide supply voltage range, low standby power dissipation, high efficiency and low drift. It is useful for any stand-alone, low part count switching system and works extremely well in battery operated systems.

- **STEP-UP, STEP DOWN OR INVERTING SWITCHING REGULATORS**
- **OUTPUT ADJUSTABLE FROM 1.3 to 40 V**
- **PEAK CURRENTS TO 1.5 A WITHOUT EXTERNAL TRANSISTORS**
- **OPERATION FROM 2.5 to 40 V INPUT**
- **LOW STANDBY CURRENT DRAIN**
- **80 dB LINE AND LOAD REGULATION**
- **HIGH GAIN, HIGH CURRENT, INDEPENDENT OP AMP**
- **PULSE WIDTH MODULATION WITH NO DOUBLE PULSING**

Connection Diagram
16-Pin DIP

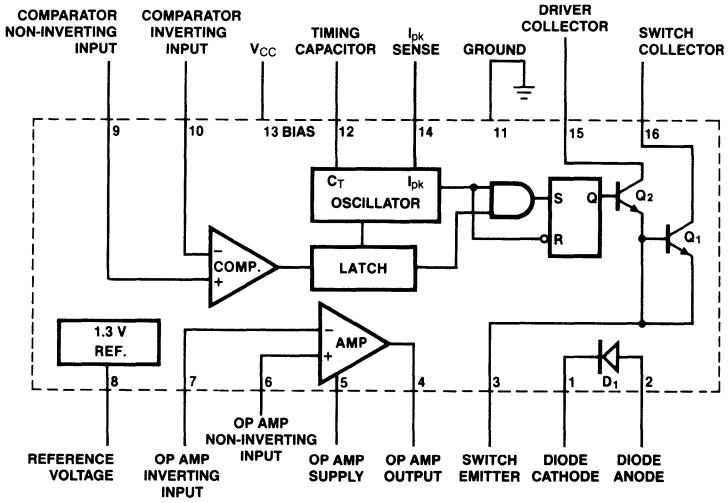


(Top View)

Order Information

Type	Package	Code	Part No.
μA78S40	Ceramic DIP	6B	μA78S40DM
μA78S40	Ceramic DIP	6B	μA78S40DC
μA78S40	Molded DIP	9B	μA78S40PC

Block Diagram



Absolute Maximum Ratings

Input Voltage from V+ to V−	40 V
Input Voltage from V+ Op Amp to V−	40 V
Common Mode Input Range (Error Amplifier and Op Amp)	−0.3 to V+
Differential Input Voltage (Note 1)	±30 V
Output-Short Circuit Duration (Op Amp)	continuous
Current from V_{REF}	10 mA
Voltage from Switch Collectors to GND	40 V
Voltage from Switch Emitters to GND	40 V
Voltage from Switch Collectors to Emitter	40 V
Voltage from Power Diode to GND	40 V
Reverse Power Diode Voltage	40 V
Current through Power Switch	1.5 A
Current through Power Diode	1.5 A
Internal Power Dissipation (Note 2)	
Molded DIP	1500 mW
Ceramic DIP	1000 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA78S40M)	−55°C to 125°C
Commercial (μA78S40C)	0°C to 70°C
Pin Temperature	
Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Notes

1. For supply voltages less than 30 V, the absolute maximum voltage is equal to the supply voltage.
2. Ratings apply to 25°C ambient, derate ceramic DIP at 8 mW/°C and plastic DIP at 14 mW/°C.

Functional Description

The μA78S40 is a variable frequency, variable duty cycle device. The initial switching frequency is set by the timing capacitor. The initial duty cycle is 6:1. This switching frequency and duty cycle can be modified by two mechanisms—the current limit circuitry (I_{pk} sense) and the comparator.

The comparator modifies the OFF time. When the output voltage is correct, the comparator output is in the HIGH state and has no effect on the circuit operation. If the output voltage is too high then the comparator output goes LOW. In the LOW state the comparator inhibits the turn on of the output stage switching transistors. As long as the comparator is LOW the system is in OFF time. As the output current rises the OFF time decreases. As the output current nears its maximum the OFF time approaches its minimum value. The comparator can inhibit several ON cycles, one ON cycle or any portion of an ON cycle. Once the ON cycle has begun the comparator cannot inhibit until the beginning of the next ON cycle.

The current limit modifies the ON time. The current limit is activated when a 300 mV potential appears between pin 13 (V_{CC}) and pin 14 (I pk). This potential is intended to result when designed for peak current flows through R_{SC}. When the peak current is reached the current limit is turned on. The current limit circuitry provides for a quick end to ON time and the immediate start of OFF time. Generally the oscillator is free running but the current limit action tends to reset the timing cycle.

Increasing load results in more current limited ON time and less OFF time. The switching frequency increases with load current.

V_D is the forward voltage drop across the internal power diode. It is listed on the data sheet as 1.25 V typical, 1.5 V maximum. If an external diode is used, then its own forward voltage drop must be used for V_D.

V_S is the voltage across the switch element (output transistors Q1 and Q2) when the switch is closed or on. This is listed on the data sheet as output saturation voltage.

Output saturation voltage 1 — defined as the switching element voltage for Q2 and Q1 in the Darlington configuration with collectors tied together. On the data sheet this applies to *Figure 1,* the step down mode.

Output saturation voltage 2 — switching element voltage for just Q1 used as a transistor switch. This applies to *Figure 2* of the data sheet, the step-up mode.

For the inverting mode, *Figure 3,* the saturation voltage of the external transistor should be used for V_S.

Electrical Characteristics V_{IN} = 5.0 V, $V_{Op\ Amp}$ = 5.0 V, T_A = Operating temperature range, unless otherwise specified.

Characteristic	Condition	Min	Typ	Max	Unit
General Characteristics					
Supply Voltage		2.5		40	V
Supply Current (Op Amp Disconnected)	V_{IN} = 5.0 V V_{IN} = 40 V		1.8 2.3	3.5 5.0	mA mA
Supply Current Op Amp Connected	V_{IN} = 5.0 V_{IN} = 40 V			4.0 5.5	mA mA
Reference Section					
Reference Voltage	I_{REF} = 1.0 mA, $0 < T_A < 70°C$ μA78S40C I_{REF} = 1.0 mA, $-55°C < T_A < 125°C$ μA78S40M	1.180	1.245	1.310	V
Reference Voltage Line Regulation	V_{IN} = 3.0 V to V_{IN} = 40 V, I_{REF} = 1.0 mA, T_A = 25°C		0.04	0.2	mV/V
Reference Voltage Load Regulation	I_{REF} = 1.0 mA to I_{REF} = 10 mA, T_A = 25°C		0.2	0.5	mV/mA
Oscillator Section					
Charging Current	V_{IN} = 5.0 V, T_A = 25°C	20		50	μA
Charging Current	V_{IN} = 40 V, T_A = 25°C	20		70	μA
Discharge Current	V_{IN} = 5.0 V, T_A = 25°C	150		250	μA
Discharge Current	V_{IN} = 40 V, T_A = 25°C	150		350	μA
Oscillator Voltage Swing	V_{IN} = 5 V, T_A = 25°C		0.5		V
t_{on}/t_{off}			6.0		μs/μs
Current Limit Section					
Current Limit Sense Voltage	T_A = 25°C	250		350	mV
Output Switch Section					
Output Saturation Voltage 1	I_{SW} = 1.0 A, *Figure 1*		1.1	1.3	V
Output Saturation Voltage 2	I_{SW} = 1.0 A, *Figure 2*		0.45	0.7	V
Output Transistor h_{FE}	I_C = 1.0 A, V_{CE} = 5.0 V, T_A = 25°C		70		
Output Leakage Current	V_{OUT} = 40 V, T_A = 25°C		10		nA
Power Diode					
Forward Voltage Drop	I_D = 1.0 A		1.25	1.5	V
Diode Leakage Current	V_D = 40 V, T_A = 25°C		10		nA
Comparator					
Input Offset Voltage	$V_{CM} = V_{REF}$		1.5	15	mV
Input Bias Current	$V_{CM} = V_{REF}$		35	200	nA
Input Offset Current	$V_{CM} = V_{REF}$		5.0	75	nA
Common Mode Voltage Range	T_A = 25°C	0		V+ −2	V
Power Supply Rejection Ratio	V_{IN} = 3.0 V to 40 V, T_A = 25°C	70	96		dB

Electrical Characteristics V_{IN} = 5.0 V, $V_{Op\ Amp}$ = 5.0 V, T_A = Operating temperature range, unless otherwise specified.

Characteristic	Condition	Min	Typ	Max	Unit
Output Operational Amplifier					
Input Offset Voltage	V_{CM} = 2.5 V		4.0	15	mV
Input Bias Current	V_{CM} = 2.5 V		30	200	nA
Input Offset Current	V_{CM} = 2.5 V		5.0	75	nA
Voltage Gain +	R_L = 2.0 k to GND; V_O = 1.0 to 2.5 V, T_A = 25°C	25 k	250 k		V/V
Voltage Gain −	R_L = 2.0 k to V+ Op Amp; V_O = 1.0 to 2.5 V, T_A = 25°C	25 k	250 k		V/V
Common Mode Voltage Range	T_A = 25°C	0		V+ −2	V
Common Mode Rejection Ratio	V_{CM} = 0 to 3.0 V, T_A = 25°C	76	100		dB
Power Supply Rejection Ratio	V+ Op Amp = 3.0 to 40 V, T_A = 25°C	76	100		dB
Output Source Current	T_A = 25°C	75	150		mA
Output Sink Current	T_A = 25°C	10	35		mA
Slew Rate	T_A = 25°C		0.6		V/μs
Output LOW Voltage	I_L = −5.0 mA, T_A = 25°C			1.0	V
Output HIGH Voltage	I_L = 50 mA, T_A = 25°C	V+OP Amp −3.0 V			V

Design Formulas

Characteristic	Step Down	Step Up	Inverting	Unit
I_{pk}	$2\ I_{OUT(Max)}$	$2\ I_{OUT(Max)} \bullet \frac{V_{OUT} + V_D - V_S}{V_{IN} - V_S}$	$2\ I_{OUT(Max)} \bullet \frac{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_S}{V_{IN} - V_S}$	A
R_{SC}	$0.33/I_{pk}$	$0\ 33\ I_{pk}$	$0.33\ I_{pk}$	Ω
$\frac{t_{on}}{t_{off}}$	$\frac{V_{OUT} + V_D}{V_{IN} - V_S - V_{OUT}}$	$\frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_S}$	$\frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} - V_S}$	
L	$\frac{V_{OUT} + V_D}{I_{pk}} \bullet t_{off}$	$\frac{V_{OUT} + V_D - V_{IN}}{I_{pk}} \bullet t_{off}$	$\frac{\lvert V_{OUT}\rvert + V_D}{I_{pk}} \bullet t_{off}$	μH
t_{off}	$\frac{I_{pk} \bullet L}{V_{OUT} + V_D}$	$\frac{I_{pk} \bullet L}{V_{OUT} + V_D - V_{IN}}$	$\frac{I_{pk} \bullet L}{\lvert V_{OUT}\rvert + V_D}$	μs
C_T (μF)	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$	$45 \times 10^{-5}\ t_{off}(\mu s)$	μF
C_O	$\frac{I_{pk} \bullet (t_{on} + t_{off})}{8\ V_{ripple}}$	$\frac{(I_{pk} - I_{OUT})^2 \bullet t_{off}}{2\ I_{pk} \bullet V_{ripple}}$	$\frac{(I_{pk} - I_{OUT})^2 \bullet t_{off}}{2\ I_{pk} \bullet V_{ripple}}$	μF
Efficiency	$\frac{V_{IN} - V_S + V_D}{V_{IN}} \bullet \frac{V_{OUT}}{V_{OUT} + V_D}$	$\frac{V_{IN} - V_S}{V_{IN}} \bullet \frac{V_{OUT}}{V_{OUT} + V_D - V_S}$	$\frac{V_{IN} - V_S}{V_{IN}} \bullet \frac{\lvert V_{OUT}\rvert}{V_{OUT} + V_D}$	
$I_{IN(Avg)}$ (Max load Condition)	$\frac{I_{pk}}{2} \bullet \frac{V_{OUT} + V_D}{V_{IN} - V_S + V_D}$	$\frac{I_{pk}}{2}$	$\frac{I_{pk}}{2} \bullet \frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} + \lvert V_{OUT}\rvert + V_D - V_S}$	A

H

Fig. 1. Typical Step-Down Performance
T_A = 25°C

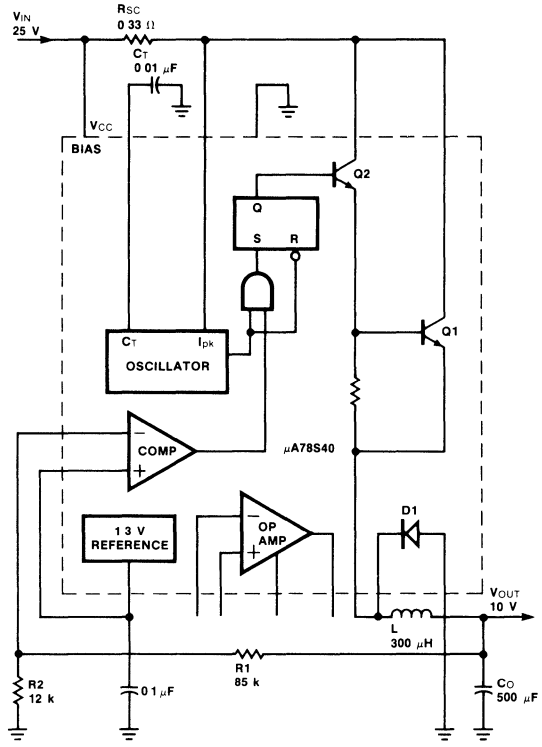
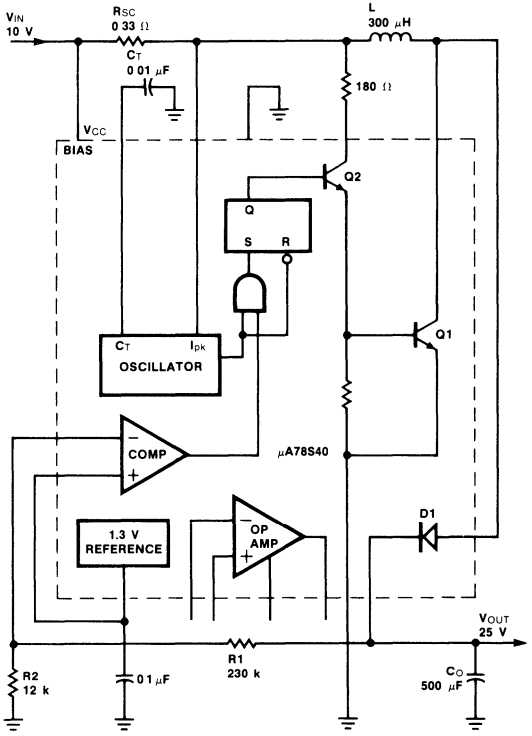


Fig. 2. Typical Step-Up Operational Performance
T_A = 25°C



Characteristic	Condition	Typical Value
Output Voltage	I_{OUT} = 200 mA	10 V
Line Regulation	20 ≤ V_{IN} ≤ 30 V	1.5 mV
Load Regulation	5 mA ≤ I_{OUT}	
	I_{OUT} ≤ 300 mA	3.0 mV
Max Output Current	V_{OUT} = 9.5 V	500 mA
Output Ripple	I_{OUT} = 200 mA	50 mV
Efficiency	I_{OUT} = 200 mA	74%
Standby Current	I_{OUT} = 200 mA	2.8 mA

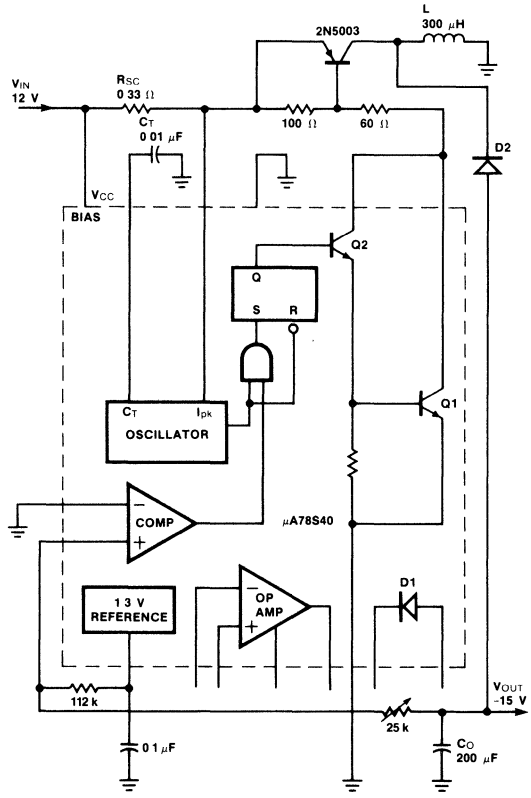
Characteristic	Condition	Typical Value
Output Voltage	I_{OUT} = 50 mA	25 V
Line Regulation	5 V ≤ V_{IN} ≤ 15 V	4.0 mV
Load Regulation	5 mA ≤ I_{OUT}	
	I_{OUT} ≤ 100 mA	2.0 mV
Max Output Current	V_{OUT} = 23.75 V	160 mA
Output Ripple	I_{OUT} = 50 mA	30 mV
Efficiency	I_{OUT} = 50 mA	79%
Standby Current	I_{OUT} = 50 mA	2.6 mA

Notes

1 For I_{OUT} ≥ 200 mA use external diode to limit on chip power dissipation

2 It is recommended that the internal reference (pin 8) be bypassed by a 0.1 μF capacitor directly to (pin 11) the ground point of the μA78S40.

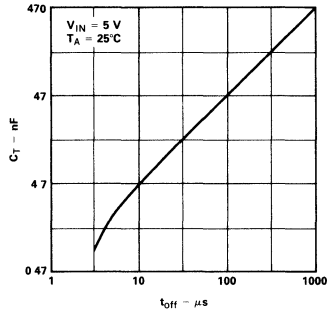
Fig. 3. Typical Inversion Operational Performance T_A = 25°C



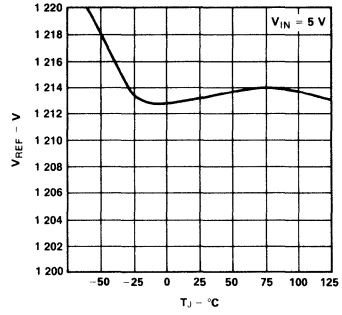
Characteristic	Condition	Typical Value
Output Voltage	I_{OUT} = 100 mA	−15 V
Line Regulation	8 V ≤ V_{IN} ≤ 18 V	5.0 mV
Load Regulation	5 mA ≤ I_{OUT}	
	I_{OUT} ≤ 150 mA	3.0 mV
Max Output Current	V_{OUT} = 14.25 V	160 mA
Output Ripple	I_{OUT} = 100 mA	20 mV
Efficiency	I_{OUT} = 100 mA	70%
Standby Current	I_{OUT} = 100 mA	2.3 mA

Typical Performance Curves

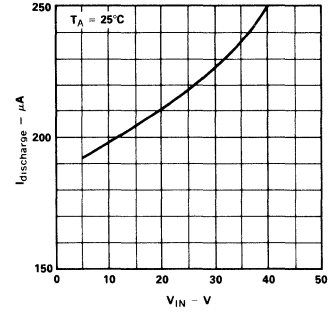
C_T as a Function of t_{off}



V_{REF} as a Function of T_J

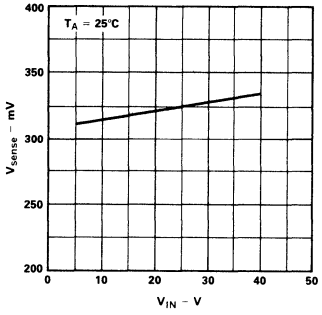


$I_{discharge}$ as a Function of V_{IN}

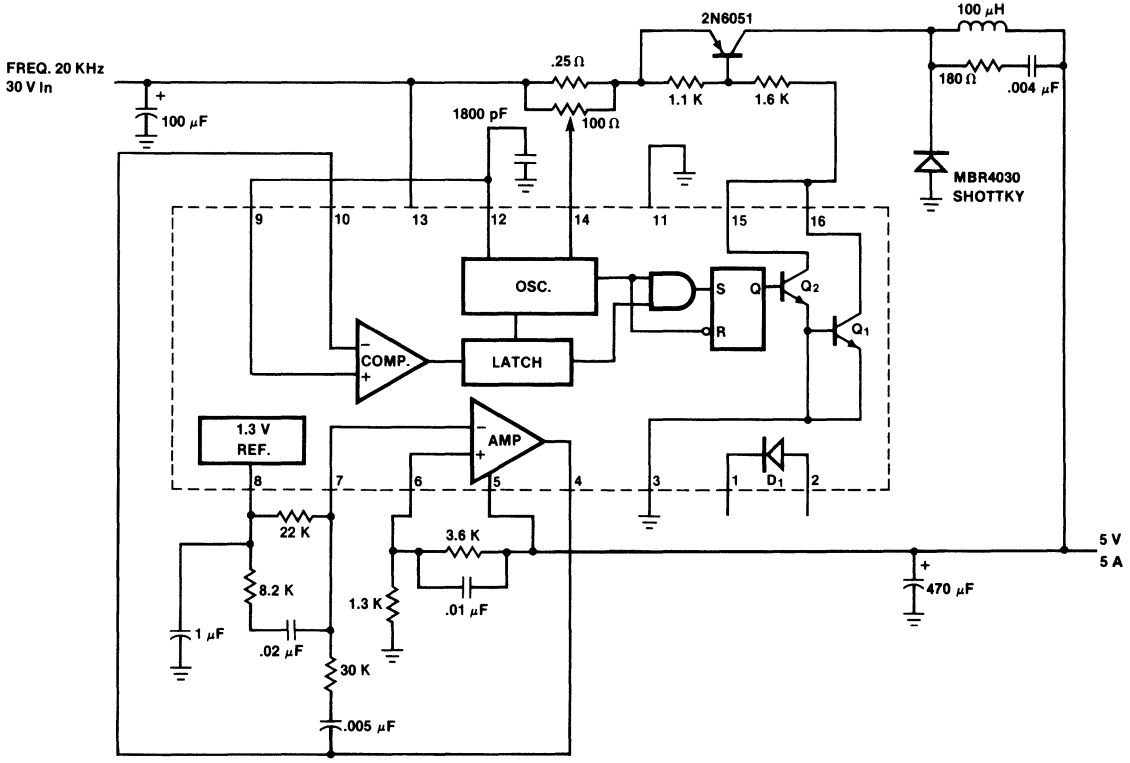


Typical Performance Curves (Cont.)

V_{Sense} as a Function of V_{IN}



Typical Pulse Width Modulator Application



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μA494
Pulse Width Modulated Control Circuit

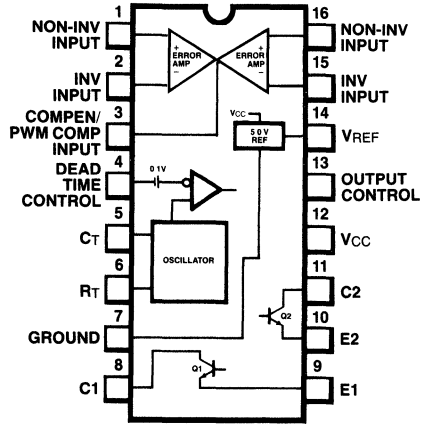
Linear Products

Description

The μA494 is a monolithic integrated circuit which includes all the necessary building blocks for the design of pulse width modulated (PWM) switching power supplies, including push-pull, bridge and series configurations. The device can operate at switching frequencies between 1.0 kHz and 300 kHz and output voltages up to 40 V. The μA494C is specified over an operating temperature range of 0°C to 70°C and the μA494M is specified over an operating temperature range of −55°C to 125°C.

- **UNCOMMITTED OUTPUT TRANSISTORS CAPABLE OF 200 mA SOURCE OR SINK**
- **ON-CHIP ERROR AMPLIFIERS**
- **ON-CHIP 5 V REFERENCE**
- **INTERNAL PROTECTION FROM DOUBLE PULSING OF OUTPUTS WITH NARROW PULSE WIDTHS OR WITH SUPPLY VOLTAGES BELOW SPECIFIED LIMITS**
- **DEAD TIME CONTROL COMPARATOR**
- **OUTPUT CONTROL SELECTS SINGLE-ENDED OR PUSH-PULL OPERATION**
- **EASILY SYNCHRONIZED (SLAVED) TO OTHER CIRCUITS**

Connection Diagram
16-Pin DIP

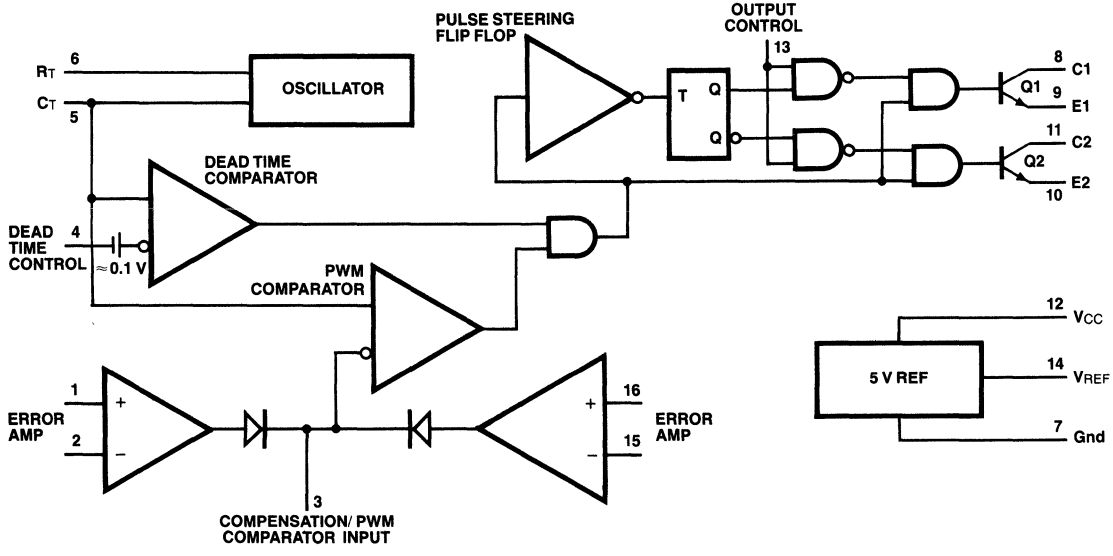


(Top View)

Order Information

Type	Package	Code	Part No.
μA494C	Ceramic DIP	6A	μA494DC
μA494C	Molded DIP	9A	μA494PC
μA494M	Ceramic DIP	6A	μA494DM

Equivalent Circuit



Absolute Maximum Ratings	μA494C
Power Supply Voltage (V_{CC})	42 V
Voltage From Any Pin to Ground (except pin 8 and pin 11)	V_{CC} + 0.3 V
Output Collector Voltage (V_{C1}, V_{C2})	42 V
Peak Collector Current (I_{C1} and I_{C2})	250 mA
Internal Power Dissipation (Note)	
Molded DIP	1500 mW
Ceramic DIP	1000 mW
Storage Temperature Range	−65°C to + 150°C
Operating Temperature Range	0°C to 70°C
Pin Temperature	
Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Functional Description

The basic oscillator (switching) frequency is controlled by an external resistor (R_T) and capacitor (C_T). The relationship between the values of R_T C_T and frequency is shown in *Figure 10*.

The level of the sawtooth wave form is compared with an error voltage by the pulse width modulated comparator. The output of the PWM Comparator directs the pulse steering flip flop and the output control logic.

The error voltage is generated by the error amplifier. The error amplifier boosts the voltage difference between the output and the 5 V internal reference. See *Figure 7* for error amp sensing techniques. The second error amp is typically used to implement current limiting.

The output control logic (pin 13) selects either push-pull or single-ended operation of the output transistors (see *Figure 6*).

The dead time control prevents on-state overlap of the output transistors as can be seen in *Figure 5*. The dead time is approximately 3 to 5% of the total period if the dead time control (pin 4) is grounded. This dead time can be increased by connecting the dead time control to a voltage up to 5 V.

The frequency response of the error amps (*Figure 11*) can be modified by using external resistors and capacitors. These components are typically connected between the compensation terminal (pin 3) and the inverting input of the error amps (pin 2 or pin 15).

The switching frequency of two or more μA494 circuits can be synchronized. The timing Capacitor, C_T is connected as shown in *Figure 8*. Charging current is provided by the master circuit. Discharging is through all the circuits slaved to the master. R_T is required only for the master circuit.

Recommended Operating Conditions

Symbol	Characteristic	μA494C Min	μA494C Max	Unit
V_{CC}	Power Supply Voltage	7.0	40	V
V_{IN}	Voltage on Any Pin Except Pins 8 and 11 (Referenced to Ground)	−0.3	V_{CC} +0.3	V
V_{C1}, V_{C2}	Output Voltage	−0.3	40	V
I_{C1}, I_{C2}	Output Collector Current		200	mA
C_T	Timing Capacitor	470		pF
			10	μF
R_T	Timing Resistor	1.8	500	kΩ
f_{osc}	Oscillator Frequency	1.0	300	kHz
T_A	Operating Ambient Temperature Range	0	+70	°C

Note

Ratings apply at 25°C, above 25°C ambient derate Hermetic DIP at 8 mW/°C and Plastic DIP at 14 mW/°C

μA494C

Electrical Characteristics Recommended Operating Conditions per above except V_{CC} = 15 V, f_{osc} = 10 kHz, T_A = 0 to 70°C unless otherwise specified.

Symbol	Characteristic	Condition	μA494C Min	μA494C Typ	μA494C Max	Unit
Reference Section						
V_{REF}	Reference Voltage	I_{REF} = 1.0 mA	4.75	5.0	5.25	V
Reg_{line}	Line Regulation of Reference Voltage	7.0 V < V_{CC} < 40 V		2.0	25	mV
TCV_{REF}	Temperature Coefficient of Reference Voltage	0°C < T_A < 70°C		0.01	0.03	%/°C
Reg_{load}	Load Regulation of Reference Voltage	1 < I_{REF} < 10 mA		1.0	15	mV
Oscillator Section						
f_{osc}	Oscillator Frequency *(Figure 10)*	C_T = 0.01 μF, R_T = 12 kΩ		10		kHz
Δf_{osc}	Oscillator Frequency Change Over Operating Temperature Range 0°C < T_A < + 70°C	C_T = 0.01 μF, R_T = 12 kΩ			2	%
Dead-Time Control Section						
$I_{IB(DT)}$	Input Bias Current (Pin 4)	V_{CC} = 15 V, 0 V < V4 < 5.25 V		−2.0	−10	μA
$DC_{(max)}$	Maximum Duty Cycle, Each Output	V_{CC} = 15 V, Pin 4 = 0 V, Output Control Pin = V_{REF}	45			%
$V_{TH(in)}$	Input Threshold Voltage Zero Duty Cycle Maximum Duty Cycle		0	3.0	3.3	V
Error Amplifier Sections						
$V_{IO(EA)}$	Input Offset Voltage	V_3 = 2.5V		2.0	10	mV
I_{IO}	Input Offset Current	V_3 = 2.5 V		25	250	nA
I_{IB}	Input Bias Current	V_3 = 2.5 V		0.2	1.0	μA
V_{ICR}	Input Common Mode Voltage Range	7 V < V_{CC} < 40 V	−0.3		Vcc	V
A_{VOL}	Large Signal Open Loop Voltage Gain	0.5 V < V_3 < 3.5 V	60	74		dB
f_c	Unity Gain Bandwidth			650		kHz
PWM Comparator Section (Pin 3) *Figure 9*						
V_{THI}	Inhibit Threshold Voltage	Zero Duty Cycle		4.0	4.5	V
I_{O-}	Output Sink Current (Note)	0.5 V < V_3 < 3.5 V	−0.2	−0.6		mA
I_{O+}	Output Source Current (Note)	0.5 V < V_3 < 3.5 V	2.0			mA

Note
These limits apply when the voltage measured at Pin 3 is within the range specified.

μA494C
Electrical Characteristics Recommended Operating Conditions per above except V_{CC} = 15 V, f_{osc} = 10 kHz, T_A = 0 to 70°C unless otherwise specified. (Cont.)

Symbol	Characteristic	Condition	μA494C Min	μA494C Typ	μA494C Max	Unit
Output Section						
$V_{CE(sat)}$	Output Saturation Voltage Common-Emitter Configuration, *Figure 3* Emitter-Follower Configuration, *Figure 4*	V_E = 0 V, I_C = 200 mA V_C = 15 V, I_E = 200 mA		1.1 1.5	1.3 2.5	V
$I_{C(off)}$	Collector Off-State Current	V_{CC} = 40 V, V_{CE} = 40 V		2.0	100	μA
$I_{E(off)}$	Emitter Off-State Current	V_{CC} = V_C = 40 V, V_E = 0			−100	μA
Output Control (Pin 13) *Figure 6*						
V_{OCL}	Output Control (pin 13) Voltage Required for Single-Ended or Parallel Output Operation				0.4	V
V_{OCH}	Output Control (pin 13) Voltage Required for Push-Pull Operation		2.4			V
Total Device						
I_{CC}	Standby Power Supply Current			6.0	10	mA
Output ac Characteristics Use Recommended Operating Conditions with T_A = 25°C						
t_r	Rise Time of Output Voltage Common-Emitter Configuration, *Figure 3* Emitter-Follower Configuration, *Figure 4*			100 100	200 200	ns ns
t_f	Fall Time of Output Voltage Common-Emitter Configuration, *Figure 3* Emitter-Follower Configuration, *Figure 4*			25 40	100 100	ns ns

Test Circuits

Fig. 1 Error Amplifier Test Circuit

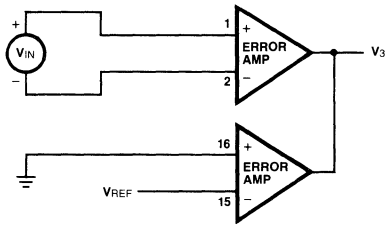
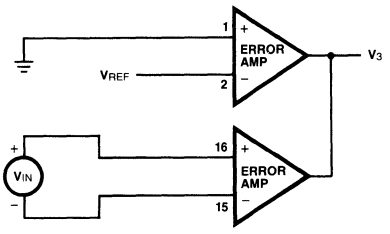


Fig. 2 Current Limit Sense Amplifier Test Circuit



Test Circuits (Cont.)

Fig. 3 Common-Emitter Configuration Test Circuit and Waveform

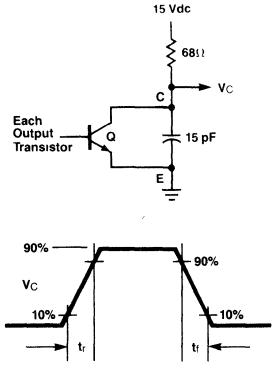


Fig. 4 Emitter-Follower Configuration Test Circuit and Waveform

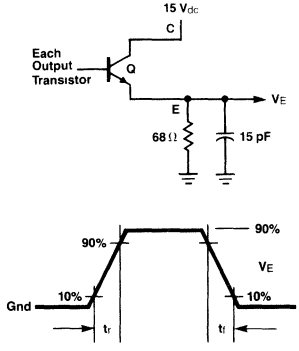
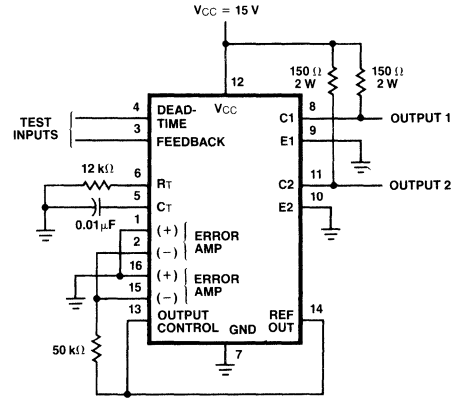
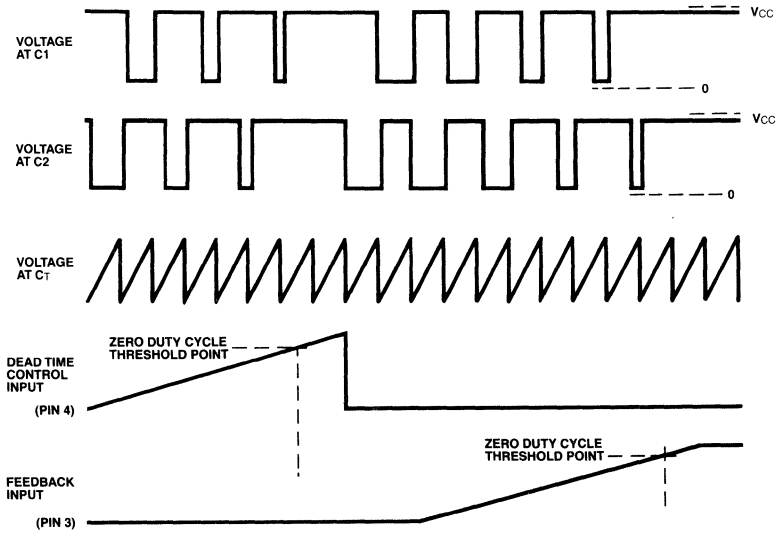


Fig. 5 Dead-Time and Feedback Control Test Circuit



Voltage Waveforms



Typical Applications

Fig. 6 Output Connections for Single-Ended and Push-Pull Configurations

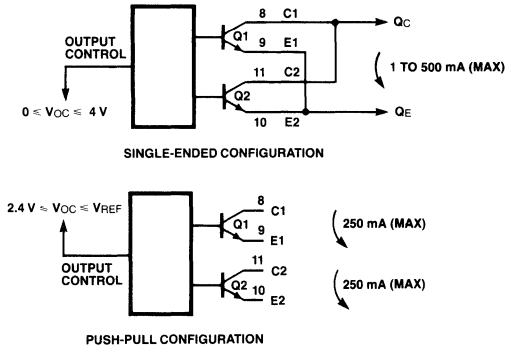


Fig. 7 Error Amplifier Sensing Techniques

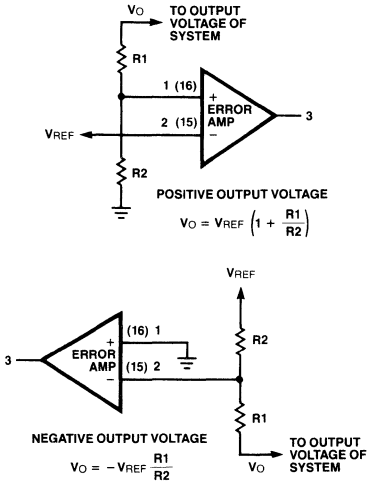


Fig. 8 Slaving Two or More Control Circuits

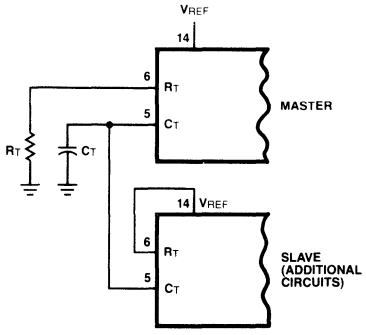


Fig. 9 Error Amplifier and Current Limit Sense Amplifier Output Circuits

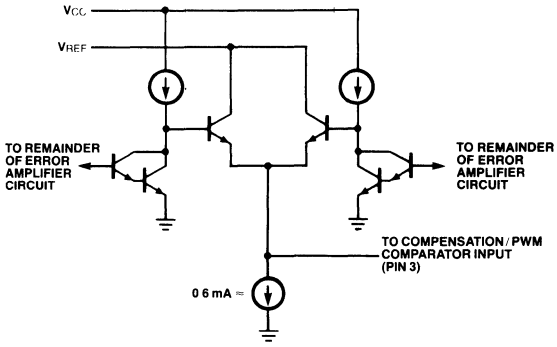


Fig. 10 Oscillator Frequency vs Timing Resistance

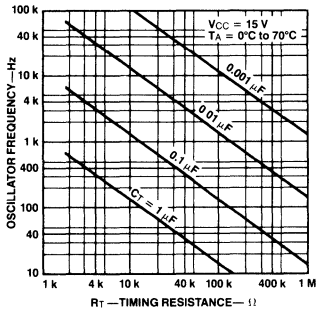
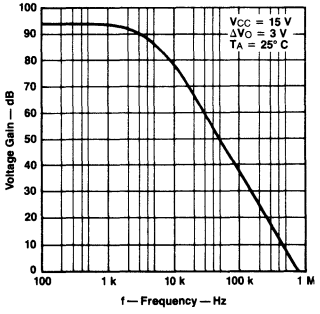


Fig. 11 Amplifier Voltage Gain vs Frequency



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μA78H05 • μA78H05A 5-Volt 5-Amp Voltage Regulators

Hybrid Products

Description

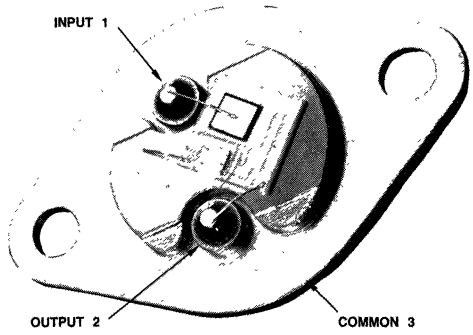
The μA78H05 and μA78H05A are hybrid regulators with 5.0 V fixed outputs and 5.0 A output capabilities. They have the inherent characteristics of the monolithic 3-terminal regulators, i.e., full thermal overload, short-circuit and safe-area protection. All devices are packaged in hermetically sealed TO-3s providing 50 W power dissipation. If the safe operating area is exceeded, the device shuts down rather than failing or damaging other system components (Note 1). This feature eliminates costly output circuitry and overly conservative heat sinks typical of high-current regulators built from discrete components.

- **5.0 A OUTPUT CURRENT**
- **INTERNAL CURRENT AND THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT PROTECTION**
- **LOW DROPOUT VOLTAGE (TYPICALLY 2.3 V @ 5.0 A)**
- **50 W POWER DISSIPATION**
- **STEEL TO-3 PACKAGE**
- **ALL PIN-FOR-PIN COMPATIBLE WITH THE SH323**

Note

1. These voltage regulators offer output transistor safe-area protection. However, to maintain full protection, the devices must be operated within the maximum input-to-output voltage differential ratings, as listed on this data sheet under "Absolute Maximum Ratings." For applications violating these limits, devices will not be fully protected

Connection Diagram
TO-3 Metal Package

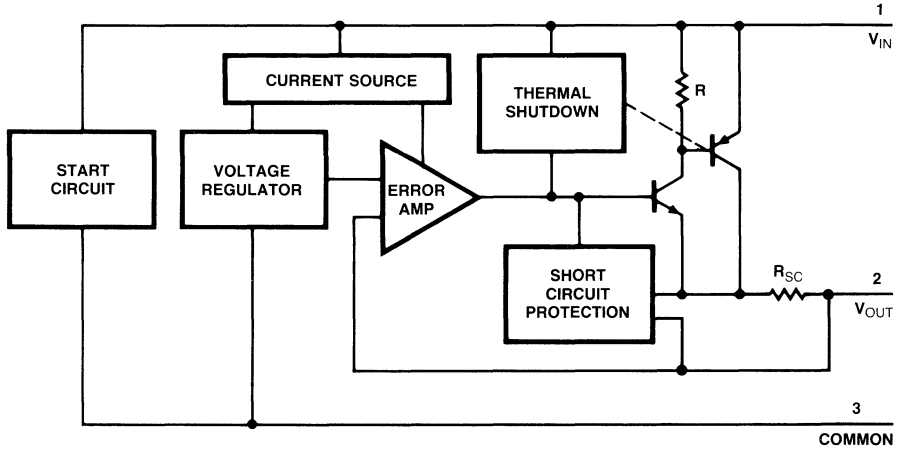


(Top View)

Order Information

Type	Package	Code	Part No.
μA7805	Metal	GN	μA78H05SC
μA7805A	Metal	GN	μA78H05ASC
μA7805	Metal	GN	μA78H05SM
μA7805A	Metal	GN	μA78H05ASM

Block Diagram



Absolute Maximum Ratings

Input Voltage	40 V
Input-to-Output Voltage Differential, Output Short Circuited	35 V
Internal Power Dissipation	50 W @ 25°C Case
Operating Junction Temperature	150°C
Military Temperature Range	
μA78H05SM	−55°C to +150°C
μA78H05ASM	−55°C to +150°C
Commercial Temperature Range	
μA78H05SC	0°C to +150°C
μA78H05ASC	0°C to +150°C
Storage Temperature Range	−55°C to +150°C
Pin Temperature (Soldering, 60 s)	300°C

μA78H05 • μA78H05A
Electrical Characteristics T_J = 25°C, V_{IN} = 10 V, I_{OUT} = 2.0 A unless otherwise specified.

Symbol	Characteristic	Condition		Limits Min	Typ	Max	Unit
V_{OUT}	Output Voltage	I_{OUT} = 2.0 A		4.85	5.0	5.25	V
ΔV_{OUT}	Line Regulation (Note 2)	V_{IN} = 8.5 to 25 V (μA78H05)			10	50	mV
		V_{IN} = 7.5 to 25 V (μA78H05A)			10	50	mV
ΔV_{OUT}	Load Regulation (Note 2)	10 mA ≤ I_{OUT} ≤ 5.0 A			10	50	mV
I_Q	Quiescent Current	I_{OUT} = 0			3.0	10	mA
RR	Ripple Rejection	I_{OUT} = 1.0 A, f = 120 Hz, 5.0 V_{pk-pk}		60			dB
V_n	Output Noise	10 Hz ≤ f ≤ 100 kHz			40		μV_{RMS}
V_{DD}	Dropout Voltage (Note 3)	μA78H05	I_{OUT} = 5.0 A		2.3		V
			I_{OUT} = 3.0 A		2.0		V
		μA78H05A	I_{OUT} = 5.0 A		2.3	2.5	V
			I_{OUT} = 3.0 A		2.0	2.3	V
I_{OS}	Short-Circuit Current Limit				7.0	12.0	A_{pk}

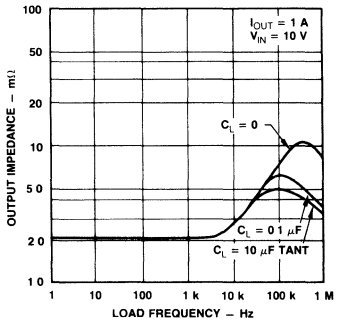
Notes

2 Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1 ms and a duty cycle of ≤ 5% Full Kelvin connection methods must be used to measure these parameters.

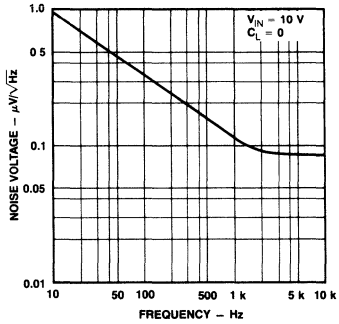
3 Dropout Voltage is the input-output voltage differential that causes the output voltage to decrease by 5% of its initial value.

Typical Performance Curves

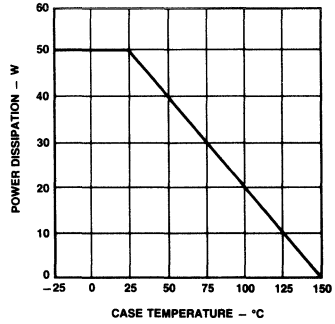
Output Impedance



Output Noise Voltage

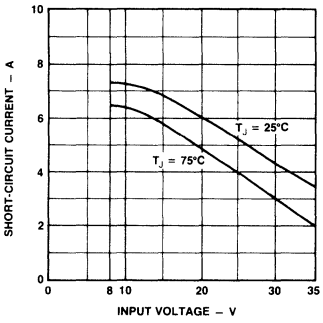


Maximum Power Dissipation

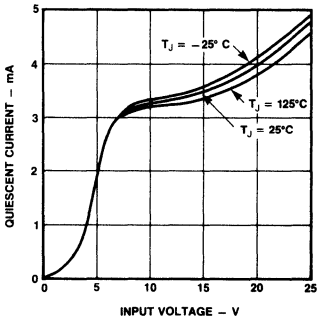


Typical Performance Curves (Cont.)

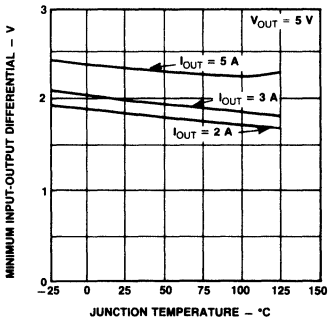
Short Circuit Current



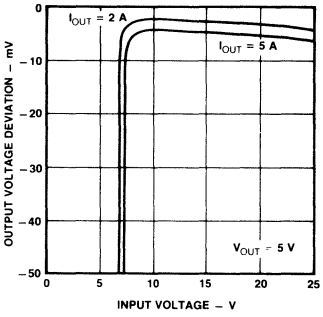
Quiescent Current



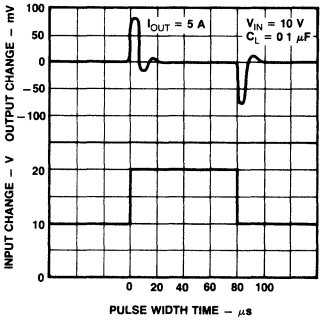
Dropout Voltage



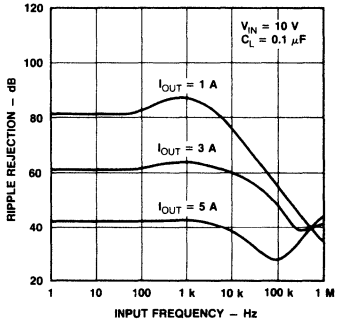
Line Regulation



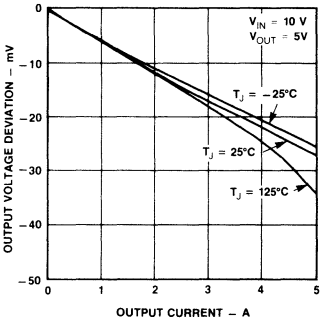
Line Transient Response



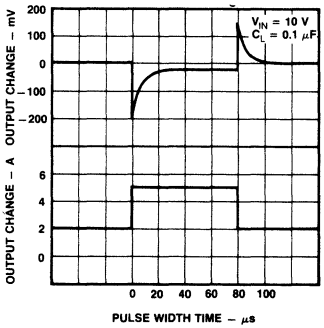
Ripple Rejection



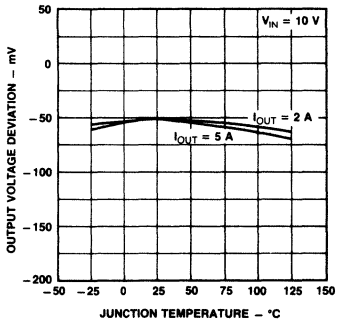
Load Regulation



Load Transient Response

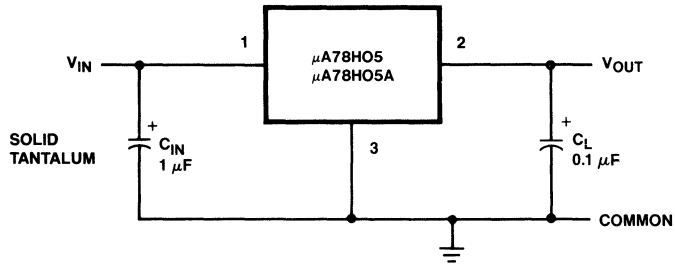


Output Voltage Deviation vs Junction Temperature



Test Circuit

Fixed Output Voltage



Design Considerations

These devices have thermal-overload protection from excessive power and internal short-circuit protection which limits the circuit's maximum current. Thus, the devices are protected from overload abnormalities. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C). It is recommended by the manufacturer that the maximum junction temperature be kept as low as possible for increased reliability. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}
TO-3	1.8	2.5

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JC} + \theta_{CA}}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA})$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-case thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink thermal resistance
θ_{SA} = Heat sink-to-ambient thermal resistance

The devices are designed to operate without external compensation components. However, the amount of external filtering of these voltage regulators depends upon the circuit layout. If in a specific application the regulator is more than four inches from the filter capacitor, a 1 μF solid tantalum capacitor should be used at the input. A 0.1 μF capacitor should be used at the output to reduce transients created by fast switching loads, as seen in the basic test circuit. These filter capacitors must be located as close to the regulator as possible.

Caution: Permanent damage can result from forcing the output voltage higher than the input voltage. A protection diode from output to input should be used if this condition exists.

FAIRCHILD
A Schlumberger Company

μA78P05
5-Volt 10-Amp Voltage Regulator

Hybrid Products

Description

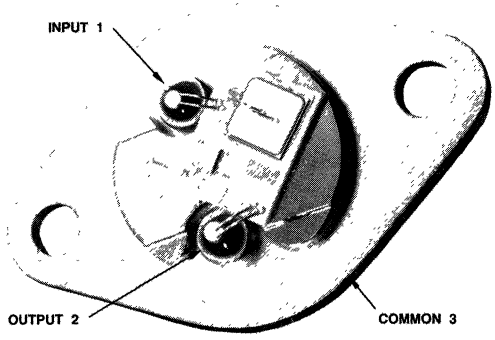
The μA78P05 3-terminal positive 5 V regulator, consisting of a monolithic control chip driving a series-pass transistor, is capable of delivering 10 A. This hybrid device is virtually blow-out proof and contains all the protection features inherent in monolithic regulators such as internal short-circuit current limiting, thermal overload and safe-area protection. If the safe-operating area is exceeded, the device shuts down rather than failing or damaging other system components (Note 1). This feature eliminates costly output circuitry and overly conservative heat sinks typical of high-current regulators built with discrete components. The μA78P05 is packaged in a hermetically sealed TO-3 providing 70 W power dissipation.

- **10 A OUTPUT CURRENT**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMIT**
- **LOW DROPOUT VOLTAGE (TYPICALLY 2.3 V @ 10 A)**
- **70 W POWER DISSIPATION**
- **PIN-FOR-PIN COMPATIBLE WITH THE μA78H05, μA78H05A AND SH323**
- **STEEL TO-3 PACKAGE**

Note

1 This voltage regulator offers output transistor safe-area protection However, to maintain full protection, the device must be operated within the maximum input-to-output voltage differential ratings as listed on this data sheet under "Absolute Maximum Ratings." For applications violating these limits, device will not be fully protected.

Connection Diagram
TO-3 Metal Package

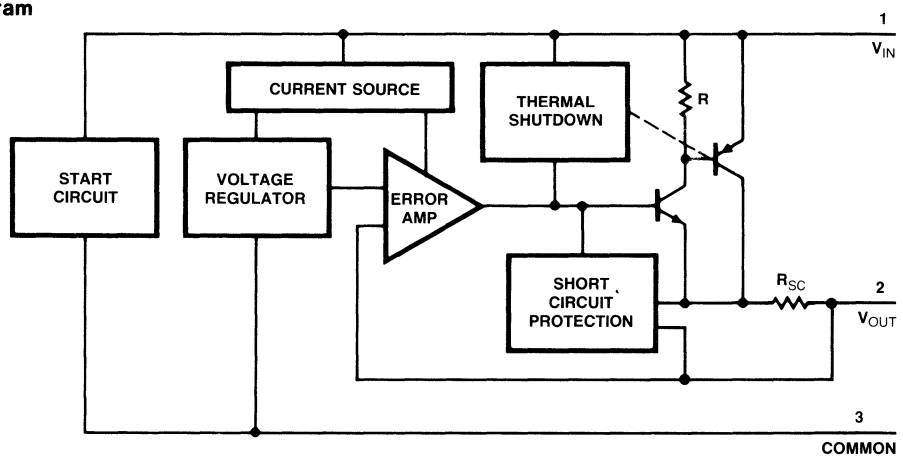


(Top View)

Order Information

Type	Package	Code	Part No.
μA78P05	Metal	6N	μA78P05SC
μA78P05	Metal	6N	μA78P05SM

Block Diagram



Absolute Maximum Ratings

Input Voltage	40 V	Military Temperature Range μA78P05SM	−55°C to +150°C
Input-to-Output Voltage Differential, Output Short-Circuited	35 V	Commercial Temperature Range μA78P05SC	0°C to +150°C
Internal Power Dissipation	70 W @ 25°C Case	Storage Temperature Range	−55°C to +150°C
Operating Junction Temperature	150°C	Pin Temperature (Soldering, 60 s)	300°C

μA78P05
Electrical Characteristics T_J = 25°C, V_{IN} = 10 V, I_{OUT} = 2.0 A unless otherwise specified

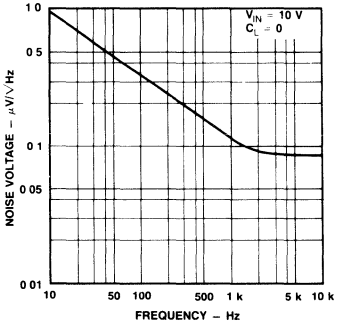
Symbol	Characteristic	Condition	Limits Min	Typ	Max	Unit
V_{OUT}	Output Voltage	I_{OUT} = 2.0 A	4.85	5.0	5.25	V
ΔV_{OUT}	Line Regulation (Note 2)	V_{IN} = 8 to 25 V		10	50	mV
ΔV_{OUT}	Load Regulation (Note 2)	10 mA ≤ I_{OUT} ≤ 5 A		25	40	mV
ΔV_{OUT}	Load Regulation (Note 2)	10 mA ≤ I_{OUT} ≤ 10 A		50	75	mV
I_Q	Quiescent Current	I_{OUT} = 0		3.4	10	mA
RR	Ripple Rejection	I_{OUT} = 1.0 A, f = 120 Hz, 5.0 V_{pk-pk}	60			dB
V_n	Output Noise	10 Hz ≤ f ≤ 100 kHz		40		μV_{RMS}
V_{DD}	Dropout Voltage (Note 3)	I_{OUT} = 5.0 A		2.0	2.3	V
		I_{OUT} = 10 A		2.5	3.0	V
I_{OS}	Short-Circuit Current Limit			14		A_{pk}

Notes

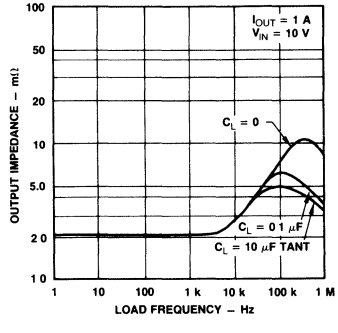
2. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1 ms and a duty cycle ≤ 5%. Full Kelvin connection methods must be used to measure these parameters.
3. Dropout Voltage is the input-output voltage differential that causes the output voltage to decrease by 5% of its initial value.

Typical Performance Curves

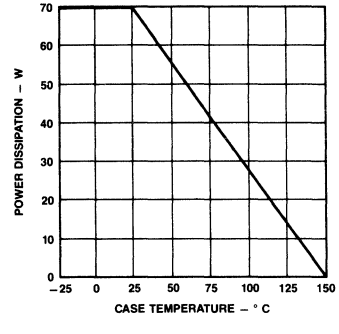
Output Noise Voltage



Output Impedance

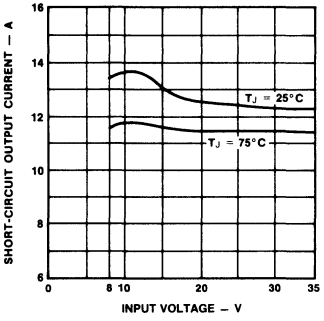


Maximum Power Dissipation

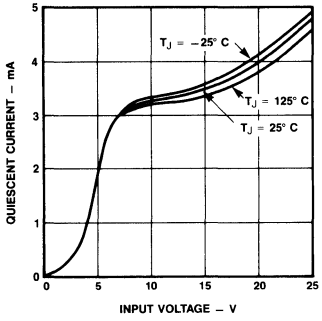


Typical Performance Curves (Cont.)

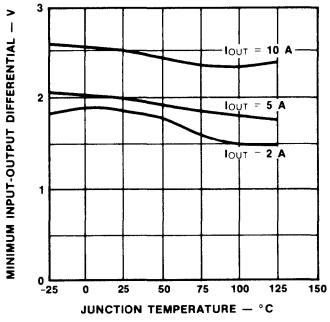
Short Circuit Current



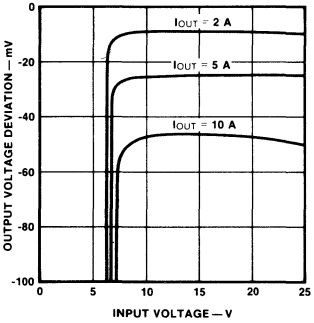
Quiescent Current



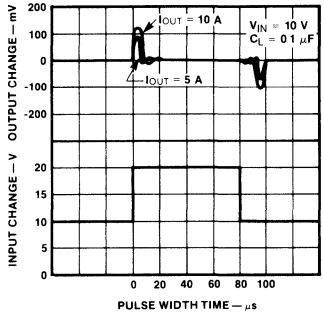
Dropout Voltage



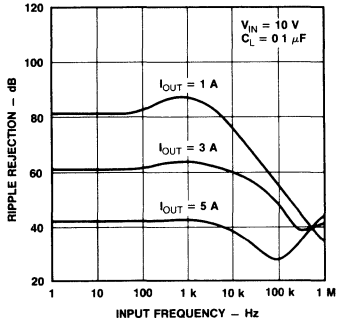
Line Regulation



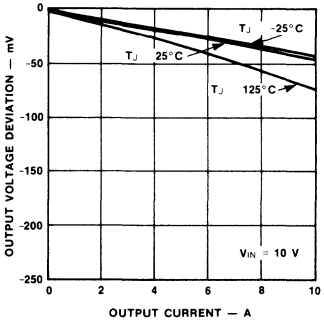
Line Transient Response



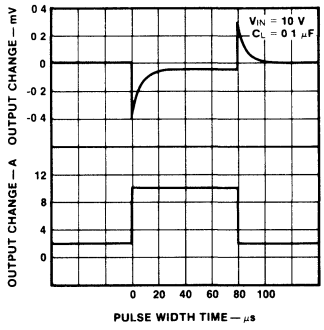
Ripple Rejection



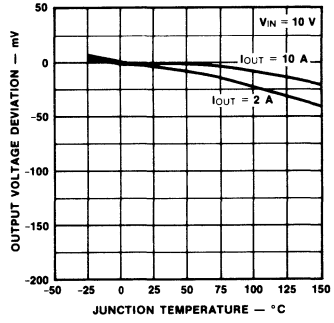
Load Regulation



Load Transient Response

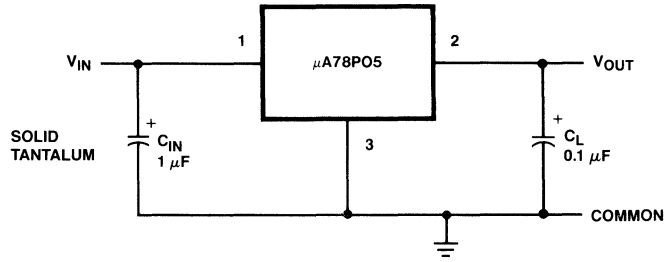


Output Voltage Deviation vs Junction Temperature



3

Basic Test Circuit



Design Considerations

This device has thermal-overload protection from excessive power and internal short-circuit protection which limits the circuit's maximum current. Thus, the devices are protected from overload abnormalities. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C). It is recommended by the manufacturer that the maximum junction temperature be kept as low as possible for increased reliability. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}
TO-3	1.5	1.8

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JC} + \theta_{CA}}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA})$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-case thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink thermal resistance
θ_{SA} = Heat sink-to-ambient thermal resistance

The μA78P05 is designed to operate without external compensation components. However, the amount of external filtering of this voltage regulator depends upon the circuit layout. If in a specific application the regulator is more than four inches from the filter capacitor, a 1 μF solid tantalum capacitor should be used at the input. A 0.1 μF capacitor should be used at the output to reduce transients created by fast switching loads, as seen in the basic test circuit. These filter capacitors must be located as close to the regulator as possible.

Caution: Permanent damage can result from forcing the output voltage higher than the input voltage. A protection diode from output to input should be used if this condition exists.

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μA78H12A 5-Amp Voltage Regulator

Hybrid Products

Description

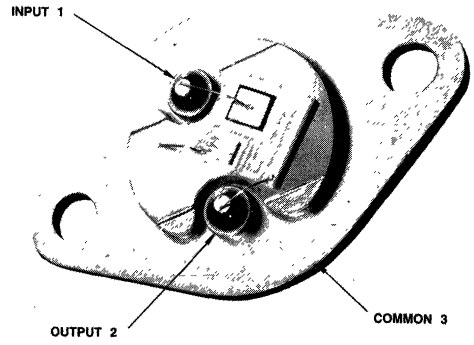
The μA78H12A is a hybrid regulator with 12.0 V fixed output and 5.0 A output capability. It has the inherent characteristics of the monolithic 3-terminal regulators; i.e., full thermal overload, short-circuit and safe-area protection. All devices are packaged in hermetically sealed TO-3s providing 50 W power dissipation. If the safe operating area is exceeded, the device shuts down, rather than failing or damaging other system components (Note 1). This feature eliminates costly output circuitry and overly conservative heat sinks typical of high-current regulators built from discrete components.

- **5.0 A OUTPUT CURRENT**
- **INTERNAL CURRENT AND THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT PROTECTION**
- **LOW DROPOUT VOLTAGE (TYPICALLY 2.3 V @ 5.0 A)**
- **50 W POWER DISSIPATION**
- **STEEL TO-3 PACKAGE**

Note

1. This voltage regulator offers output transistor safe-area protection However, to maintain full protection, the device must be operated within the maximum input-to-output voltage differential ratings, as listed on this data sheet under "Absolute Maximum Ratings." For applications violating these limits, device will not be fully protected.

Connection Diagram
TO-3 Metal Package

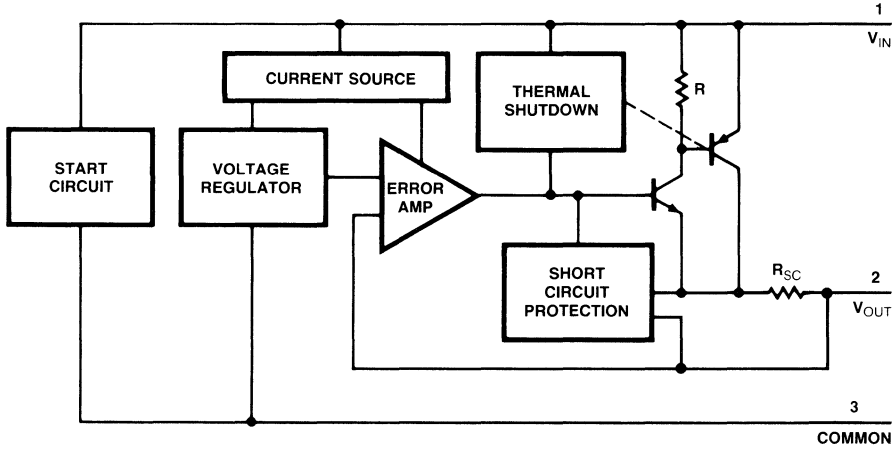


(Top View)

Order Information

Type	Package	Code	Part No.
μA78H12A	Metal	GN	μA78H12ASC
μA78H12A	Metal	GN	μA78H12ASM

Block Diagram



Absolute Maximum Ratings

Input Voltage	40 V	Commercial Temperature Range	
Input-to-Output Voltage Differential, Output Short-Circuited	35 V	μA78H12ASC	0°C to +150°C
Internal Power Dissipation	50 W @ 25°C Case	Storage Temperature Range	−55°C to +150°C
Operating Junction Temperature	150°C	Pin Temperature (Soldering, 60 s)	300°C
Military Temperature Range μA78H12ASM	−55°C to +150°C		

μA7812A
Electrical Characteristics T_J = 25°C, V_{IN} = 19 V, I_{OUT} = 2.0 A unless otherwise specified

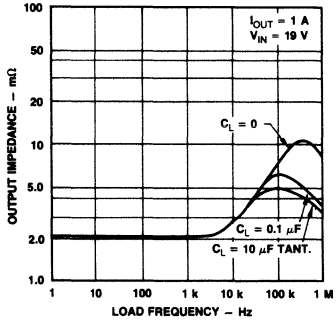
Symbol	Characteristic	Condition	Limits			Unit
			Min	Typ	Max	
V_{OUT}	Output Voltage	I_{OUT} = 2.0 A	11.5	12	12.5	V
ΔV_{OUT}	Line Regulation (Note 2)	V_{IN} = 16 to 25 V		20	120	mV
ΔV_{OUT}	Load Regulation (Note 2)	10 mA ≤ I_{OUT} ≤ 5.0 A		20	120	mV
I_Q	Quiescent Current	I_{OUT} = 0, V_{IN} = 17 V		3.7	10	mA
RR	Ripple Rejection	I_{OUT} = 1.0 A, f = 120 Hz, 5.0 $V_{pk\text{-}pk}$	60			dB
V_n	Output Noise	10 Hz ≤ f ≤ 100 kHz, V_{IN} = 17 V		75		V_{RMS}
V_{DD}	Dropout Voltage (Note 3)	I_{OUT} = 5.0 A		2.3	2.5	V
		I_{OUT} = 3.0 A		2.0	2.3	V
I_{OS}	Short-Circuit Current Limit			7.0	12.0	A_{pk}

Notes

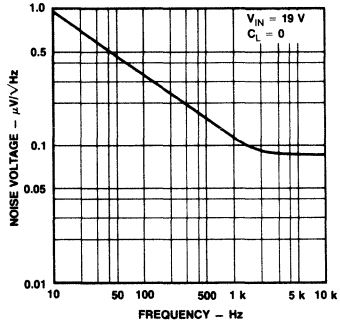
2. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1 ms and a duty cycle ≤ 5%. Full Kelvin connection methods must be used to measure these parameters.
3. Dropout Voltage is the input-to-output voltage differential that causes the output voltage to decrease by 5% of its initial value.

Typical Performance Curves

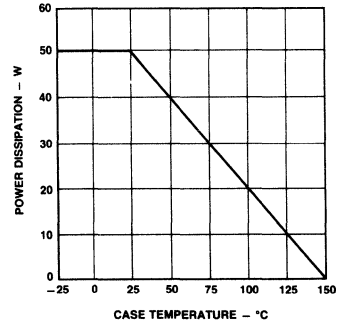
Output Impedance



Output Noise Voltage

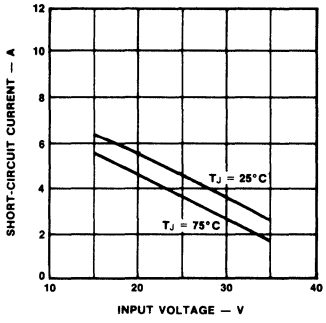


Maximum Power Dissipation

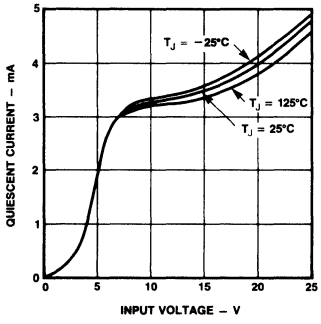


Typical Performance Curves (Cont.)

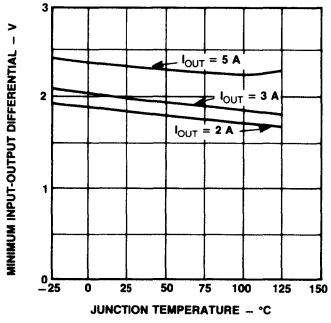
Short Circuit Current



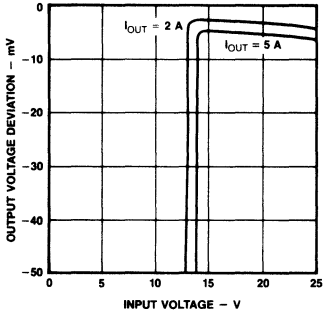
Quiescent Current



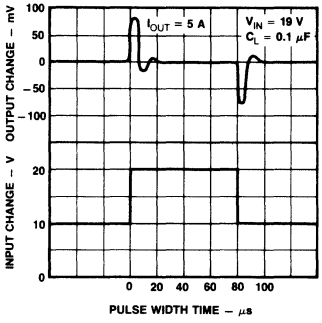
Dropout Voltage



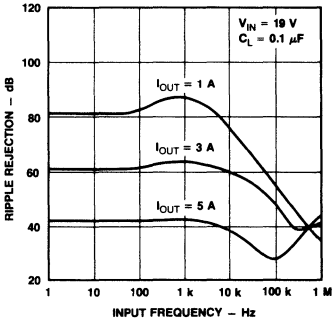
Line Regulation



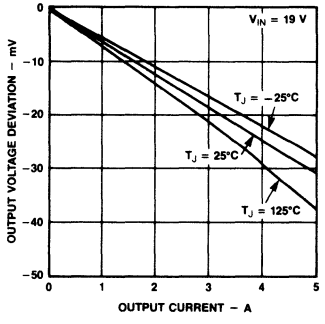
Line Transient Response



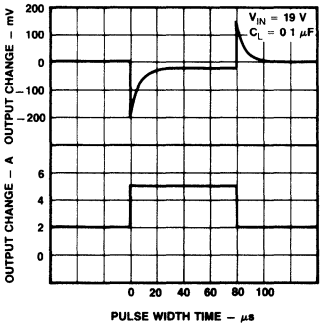
Ripple Rejection



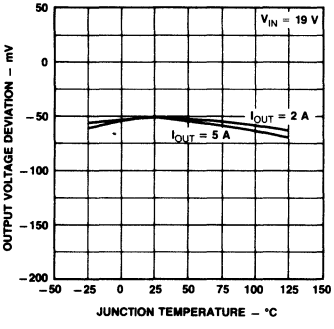
Load Regulation



Load Transient Response

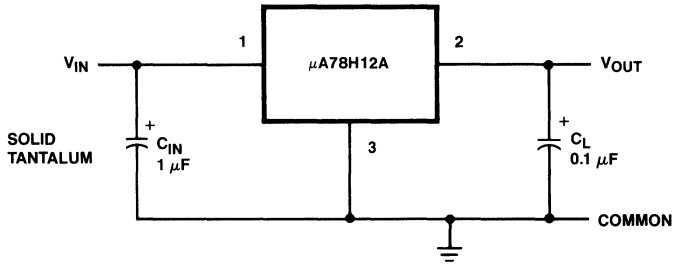


Output Voltage Deviation vs Junction Temperature



3

Basic Test Circuit



Design Considerations

This device has thermal-overload protection from excessive power and internal short-circuit protection which limits the circuit's maximum current. Thus, the device is protected from overload abnormalities. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C). It is recommended by the manufacturer that the maximum junction temperature be kept as low as possible for increased reliability. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}
TO-3	1.8	2.5

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JC} + \theta_{CA}}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{JA})$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-case thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink thermal resistance
θ_{SA} = Heat sink-to-ambient thermal resistance

The devices are designed to operate without external compensation components. However, the amount of external filtering of these voltage regulators depends upon the circuit layout. If in a specific application the regulator is more than four inches from the filter capacitor, a 1 μF solid tantalum capacitor should be used at the input. A 0.1 μF capacitor should be used at the output to reduce transients created by fast switching loads, as seen in the basic test circuit. These filter capacitors must be located as close to the regulator as possible.

Caution: Permanent damage can result from forcing the output voltage higher than the input voltage. A protection diode from output to input should be used if this condition exists.

FAIRCHILD
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μA78HGA
Positive Adjustable 5-Amp Voltage Regulator

Hybrid Products

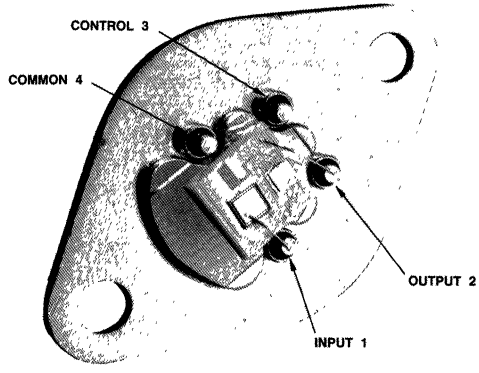
Description

The μA78HGA is an adjustable 4-terminal positive voltage regulator capable of supplying in excess of 5.0 A over a 5.0 V to 24 V output range. Only two external resistors are required to set the output voltage.

The μA78HGA is packaged in a hermetically sealed TO-3, providing 50 W power dissipation. The regulator consists of a monolithic chip driving a discrete series-pass element. A beryllium-oxide substrate is used in conjunction with an isothermal layout to optimize the thermal characteristics of each device and still maintain electrical isolation between the various chips. This unique circuit design limits the maximum junction temperature of the power output transistor to provide full automatic thermal overload protection. If the safe operating area is ever exceeded (Note 1), the device simply shuts down rather than failing or damaging other system components. This feature eliminates the need to design costly regulators built from discrete components.

- **5.0 A OUTPUT CURRENT**
- **INTERNAL CURRENT AND THERMAL LIMITING**
- **INTERNAL SHORT CIRCUIT CURRENT LIMIT**
- **LOW DROPOUT VOLTAGE (TYPICALLY 2.3 V @ 5.0 A)**
- **50 W POWER DISSIPATION**
- **ELECTRICALLY NEUTRAL CASE**
- **STEEL TO-3 PACKAGE**
- **ALL PIN-FOR-PIN COMPATIBLE WITH μA78HG**

Connection Diagram
TO-3 Metal Package

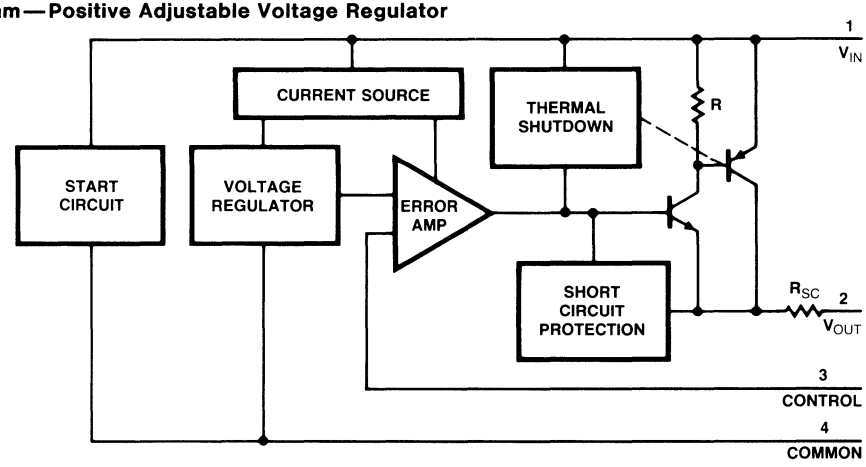


(Top View)

Order Information

Type	Package	Code	Part No.
μA78HGA	Metal	JA	μA78HGASC
μA78HGA	Metal	JA	μA78HGASM

Block Diagram—Positive Adjustable Voltage Regulator



Notes on following pages

Absolute Maximum Ratings

Input Voltage	40 V
Internal Power Dissipation	50 W @ 25°C Case
Maximum Input-to-Output Voltage	
Differential Output Short Circuit	35 V
Operating Junction Temperature	150°C
Military Temperature Range μA78HGASM	−55°C to +150°C
Commercial Temperature Range μA78HGASC	0°C to +150°C
Storage Temperature Range	−55°C to +150°C
Pin Temperature (Soldering, 60 s)	300°C

Electrical Characteristics T_J = 25°C, V_{IN} = 10 V, I_{OUT} = 2.0 A unless otherwise specified

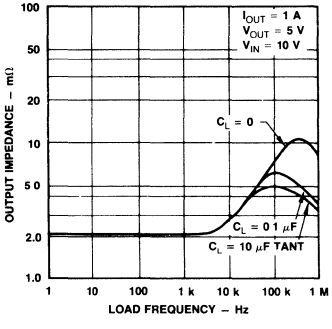
Symbol	Characteristic	Condition (Note 3)	Limits Min	Typ	Max	Unit
V_{OUT}	Output Voltage (Note 4)	I_{OUT} = 2.0 A, V_{IN} = V_{OUT} + 3.5 V	5.0		24	V
ΔV_{OUT}	Line Regulation (Note 2)	V_{IN} = 7.5 to 25 V		0.2%	1%	V
ΔV_{OUT}	Load Regulation (Note 2)	10 mA ≤ I_{OUT} ≤ 5.0 A		0.2%	1%	V
I_Q	Quiescent Current	I_{OUT} = 0		3.4	10	mA
RR	Ripple Rejection	I_{OUT} = 1.0 A, f = 210 Hz, 5.0 V_{pk-pk}	60			dB
V_n	Output Noise	10 Hz ≤ f ≤ 100 kHz, V_{IN} = V_{OUT} + 5.0 V		50		μV_{RMS}
V_{DD}	Dropout Voltage (Note 5)	I_{OUT} = 5.0 A		2.3	2.5	V
		I_{OUT} = 3.0 A		2.0	2.3	V
I_{OS}	Short-Circuit Current Limit	V_{IN} = 15 V		7.0	12.0	A_{pk}
V_C	Control Pin Voltage		4.85	5.0	5.25	V

Notes

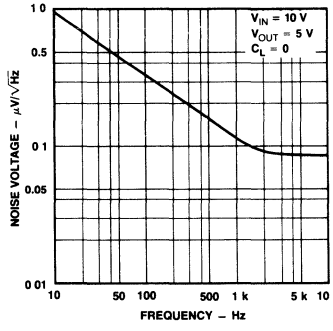
1. This voltage regulator offers output transistor safe-area protection. However, to maintain full protection, the device must be operated within the maximum input-to-output voltage differential rating listed on the data sheet under "Absolute Maximum Ratings." For applications violating these limits, device will not be fully protected.
2. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1 ms and a duty cycle ≤ 5%. Full Kelvin connection methods must be used to measure these parameters.
3. The performance characteristics of the adjustable series (μA78HGA) is specified for V_{OUT} = 5.0 V, unless otherwise noted.
4. V_{OUT} is defined as $V_{OUT} = \frac{R1 + R2}{R2}$ (V_{CONT}) where R1 and R2 are defined in the Basic Test Circuit diagram.
5. Dropout Voltage is the input-output voltage differential that causes the output voltage to decrease by 5% of its initial value.

Typical Performance Curves

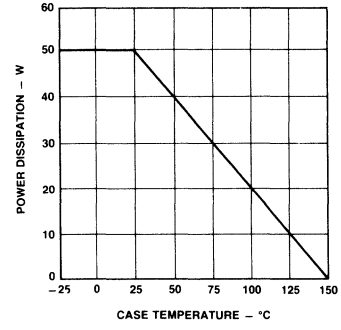
Output Impedance



Output Noise Voltage

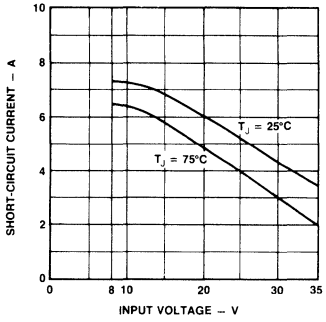


Maximum Power Dissipation

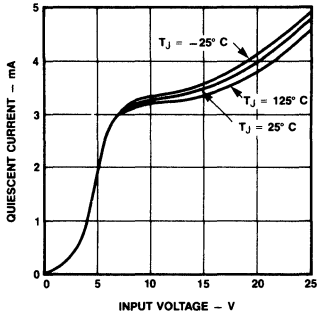


Typical Performance Curves (Cont.)

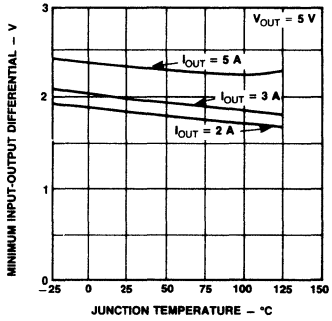
Short Circuit Current



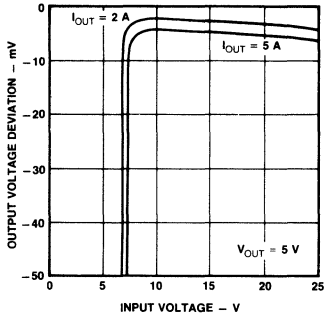
Quiescent Current



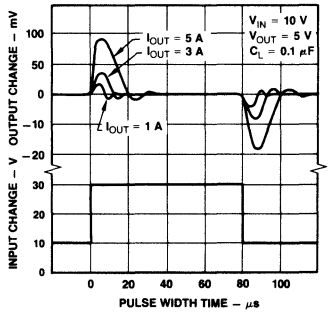
Dropout Voltage



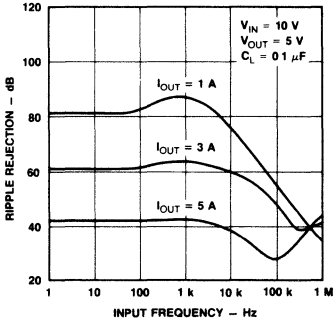
Line Regulation



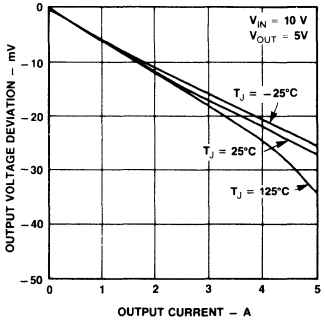
Line Transient Response



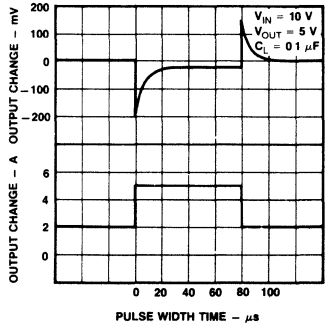
Ripple Rejection



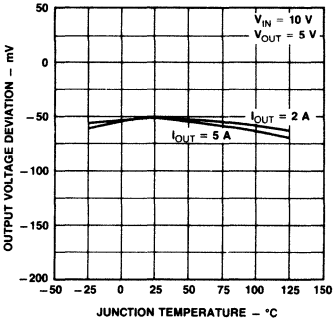
Load Regulation



Load Transient Response



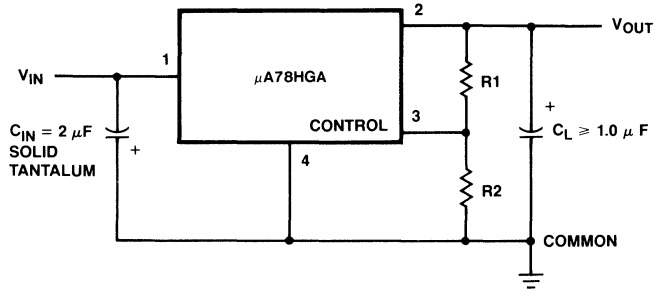
Output Voltage Deviation vs Junction Temperature



3

Test Circuit

Adjustable Output Voltage



Design Considerations

This device has thermal-overload protection from excessive power and internal short-circuit protection which limits the circuit's maximum current. Thus, the device is protected from overload abnormalities. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C). It is recommended by the manufacturer that the maximum junction temperature be kept as low as possible for increased reliability. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}
TO-3	1.8	2.5

$$P_{D(MAX)} = \frac{T_{J(max)} - T_A}{\theta_{JC} + \theta_{CA}}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA})$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-case thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{SA} = Heat sink-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink thermal resistance

This device is designed to operate without external compensation components. However, the amount of external filtering of this voltage regulator depends upon the circuit layout. If in a specific application the regulator is more than four inches from the filter capacitor, a 1 μF solid tantalum capacitor should be used at the input. A 0.1 μF capacitor should be used at the output to reduce transients created by fast switching loads, as seen in the basic test circuit. These filter capacitors must be located as close to the regulator as possible.

Caution: Permanent damage can result from forcing the output voltage higher than the input voltage. A protection diode from output to input should be used if this condition exists.

Voltage Output

The device has an adjustable output voltage from 5.0 V to 24 V which can be programmed by the external resistor network (potentiometer or two fixed resistors) using the relationship

$$V_{OUT} = V_{CONTROL} \left(\frac{R1 + R2}{R2} \right)$$

Example: If R1 = 0 Ω and R2 = 5 kΩ, then
V_{OUT} = 5 V nominal.
Or, if R1 = 10 kΩ and R2 = 5 kΩ, then
V_{OUT} = 15 V.

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μA79HG
5 A Negative Adjustable Voltage Regulator

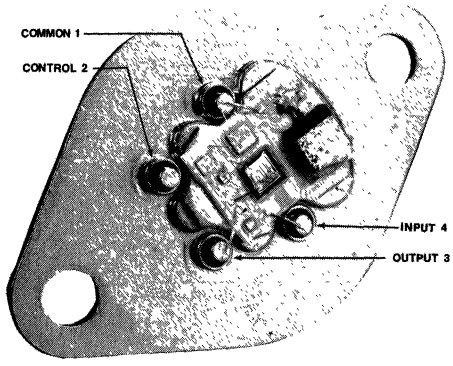
Hybrid Products

Description

The μA79HG is an adjustable 4-terminal negative voltage regulator capable of supplying in excess of −5 A over a −24 V to −2.11 V output range. The μA79HG hybrid voltage regulator has been designed with all the inherent characteristics of the monolithic 4-terminal regulator; i.e., full thermal overload and short circuit protection. The μA79HG is packaged in a hermetically-sealed 4-pin TO-3 package providing 50 W power dissipation. The regulator consists of a monolithic chip driving a discrete-series pass element and short circuit detection transistors.

- **−5.0 A OUTPUT CURRENT**
- **INTERNAL CURRENT AND THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMIT**
- **LOW DROP-OUT VOLTAGE (TYPICALLY 2.2 V @ 5.0 A)**
- **50 W POWER DISSIPATION**
- **ELECTRICALLY NEUTRAL CASE**
- **STEEL TO-3 CASE**

Connection Diagram
4-Pin Metal Package

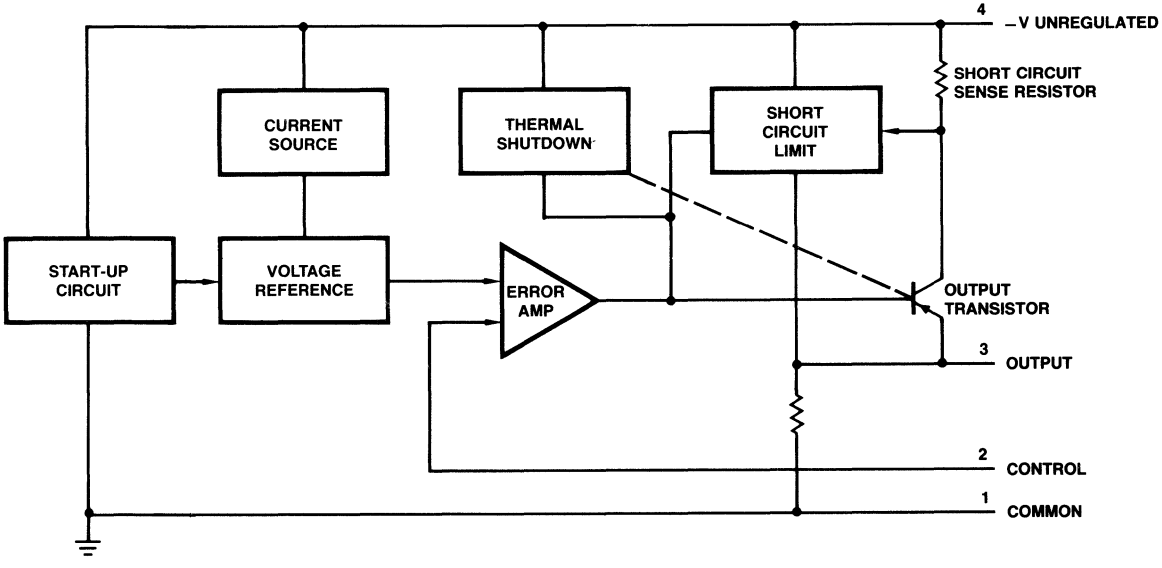


(Top View)

Order Information

Type	Package	Code	Part No.
μA79HG	Metal	JA	μA79HGSC
μA79HG	Metal	JA	μA79HGSM

Block Diagram



Absolute Maximum Ratings

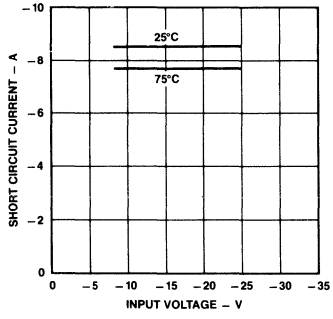
Input Voltage	−40 V	Storage Temperature Range	−55°C to +150°C
Internal Power Dissipation	50 W @ 25°C Case	Pin Temperature (Soldering, 60 s)	300°C
Maximum Input-to-Output Voltage Differential	−35 V		
Operating Junction Temperature Range	0°C to +150°C		

μA79HG
Electrical Characteristics T_J = 25°C, V_{IN} = −10 V and I_{OUT} = −2.0 A unless otherwise specified.

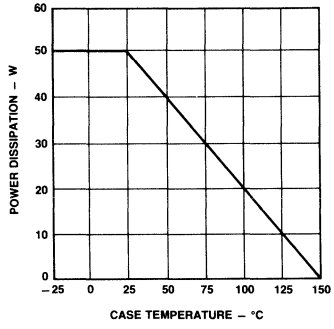
Characteristic	Limits Min	Typ	Max	Unit	Condition
Input Voltage Range	−40		−7.0	V	
Nominal Output Voltage Range	−24		−2.11	V	$V_{IN} = V_{OUT} - 5$ V
Output Voltage Tolerance			4	%(V_{OUT})	−40 V ≤ V_{IN} ≤ −7 V
Line Regulation		0.4	1.0	%(V_{OUT})	−40 V ≤ V_{IN} ≤ −7 V
Load Regulation		0.7	1.0	%(V_{OUT})	$V_{IN} = V_{OUT} - 10$ V, −10 mA ≤ I_{OUT} ≤ −5.0 A
Control Pin Current			3.0	μA	
Quiescent Current			−5.0	mA	V_{IN} = −10 V
Ripple Rejection		50		dB	−18 V ≤ V_{IN} ≤ −8.5 V, V_{OUT} = −5 V, f = 120 Hz
Output Noise Voltage		200		μV	10 Hz ≤ f ≤ 100 kHz, V_{OUT} = −5.0 V
Dropout Voltage		2.2		V	I_{OUT} = −5 A
Short Circuit Current Limit		−8	−12	A	V_{IN} = −15 V
Control Pin Voltage (Reference)	−2.35		−2.11	V	V_{IN} = −10 V

Typical Performance Curves

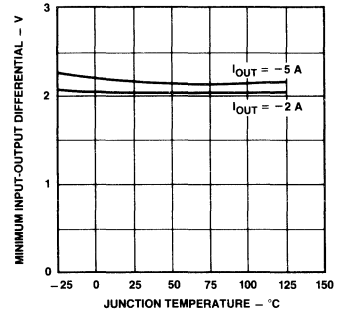
Short Circuit Current



Quiescent Current

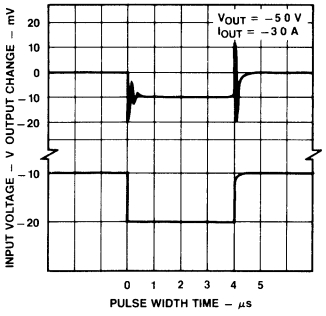


Dropout Voltage

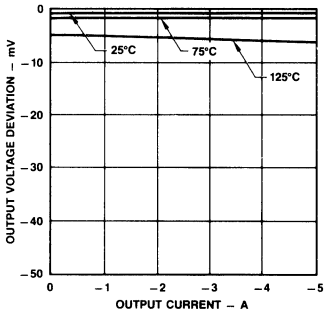


Typical Performance Curves (Cont.)

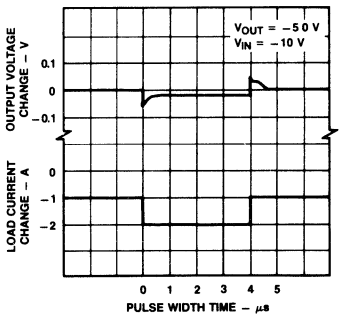
Line Transient Response



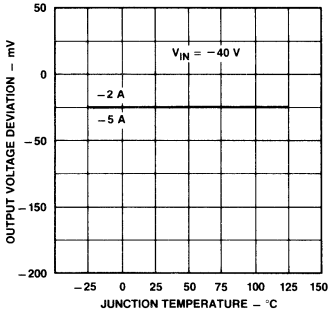
Load Regulation



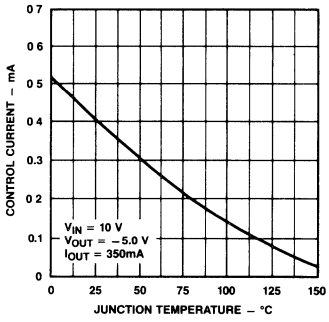
Load Transient Response



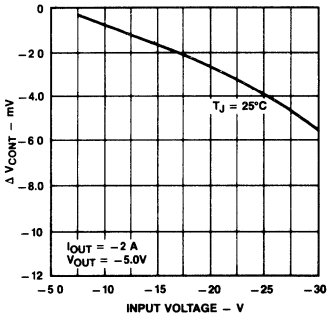
Output Voltage Deviation vs Junction Temperature



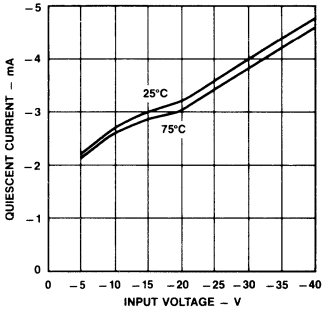
Control Current vs Temperature



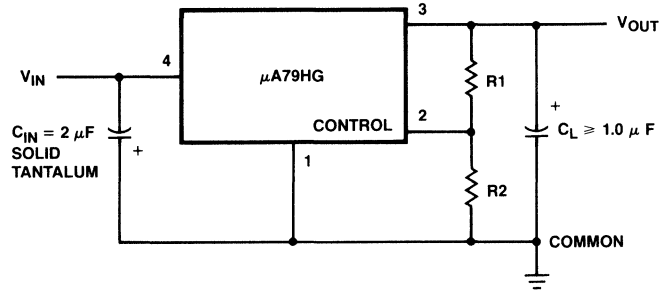
Differential Control Voltage vs Input Voltage



Maximum Power Dissipation



Basic Test Circuit, Adjustable Output Voltage



$$VOUT \simeq V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

Design Considerations

This device has thermal overload protection from excessive power and internal short circuit protection which limits the circuit's maximum current. Thus, the device is protected from overload abnormalities. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C). It is recommended by the manufacturer that the maximum junction temperature be kept as low as possible for increased reliability. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used.

Package	Typ	Max
	θ_{JC}	θ_{JC}
TO-3	1.8	2.5

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$$T_J = T_A + P_D\,(\theta_{JC} + \theta_{CA})$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-case thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink thermal resistance
θ_{SA} = Heat sink-to-ambient thermal resistance

The device is designed to operate without external compensation components. However, the amount of external filtering of these voltage regulators depends upon the circuit layout. If in a specific application the regulator is more than four inches from the filter capacitor, a 2 μF solid tantalum capacitor should be used at the input. A 1 μF capacitor should be used at the output to reduce transients created by fast switching loads, as seen in the basic test circuit. These filter capacitors must be located as close to the regulator as possible.

Caution: Permanent damage can result from forcing the output voltage higher than the input voltage. A protection diode from output to input should be used if this condition exists.

Voltage Output

The device has an adjustable output voltage from −2.11 to −24 V which can be programmed by the external resistor network (potentiometer or two fixed resistors) using the relationship:

$$V_{OUT} = V_{CONTROL}\left(\frac{R1 + R2}{R2}\right)$$

Example: If R1 = 0 Ω and R2 = 5 kΩ, then V_{OUT} = −2.11 V nominal.
Or, if R1 = 12.8 kΩ and R2 = 2.1 kΩ then V_{OUT} = −15 V.

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SH323 • SH223 • SH123
5 A, 3 V
Voltage Regulator

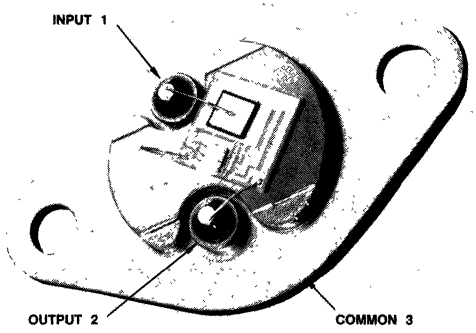
Hybrid Products

Description

The SH232 is a hybrid regulator with 5.0 V fixed output and 3.0 A output capability. It has the inherent characteristics of the monolithic 3-terminal regulators, i.e., full thermal overload, short circuit and safe area protection. All devices are packaged in hermetically sealed TO-3s providing 50 W power dissipation. If the safe operating area is exceeded, the device shuts down rather than failing or damaging other system components (Note 1). This feature eliminates costly output circuitry and overly conservative heat sinks typical of high-current regulators built from discrete components.

- **3.0 A OUTPUT CURRENT**
- **INTERNAL CURRENT AND THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT PROTECTION**
- **LOW DROPOUT VOLTAGE (TYPICALLY 2.0 V @ 3.0 A)**
- **50 W POWER DISSIPATION**
- **STEEL TO-3 PACKAGE**
- **ALL PIN-FOR-PIN COMPATIBLE WITH THE LM323, SG323**

Connection Diagram
2-Pin Metal Package

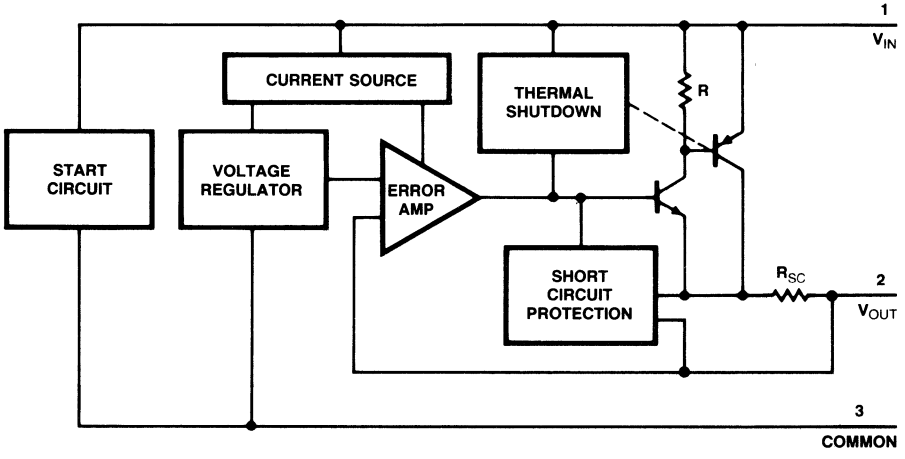


(Top View)

Order Information

Type	Package	Code	Part No.
SH323	Metal	GN	SH323SC
SH223	Metal	GN	SH223SV
SH123	Metal	GN	SH123SM

Block Diagram



Absolute Maximum Ratings

Input Voltage	40 V	Military Temperature Range SH123SM	−55°C to +150°C
Input-to-Output Voltage Differential		Commercial Temperature Range SH323SC	0°C to +150°C
Output Short Circuited	35 V	Storage Temperature Range	−55°C to +150°C
Internal Power Dissipation	50 W @ 25°C Case	Pin Temperature (Soldering, 60 s)	300°C
Operating Junction Temperature	150°C		
Industrial Temperature Range SH223SV	−25°C to +150°C		

Electrical Characteristics T_J = 25°C, V_{IN} = 10 V, I_{OUT} = 2.0 A unless otherwise specified.

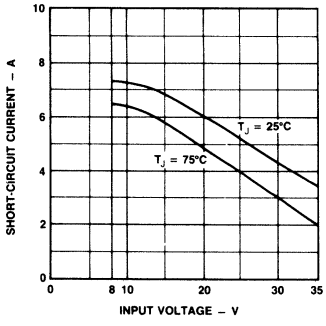
		Limits				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
V_{OUT}	Output Voltage	4.85	5.0	5.25	V	I_{OUT} = 2.0 A
ΔV_{OUT}	Line Regulation (Note 2)		10	25	mV	V_{IN} = 7.5 to 25 V
ΔV_{OUT}	Load Regulation (Note 2)		10	50	mV	10 mA ≤ I_{OUT} ≤ 3.0 A
I_Q	Quiescent Current		3.0	10	mA	I_{OUT} = 0
RR	Ripple Rejection	60			dB	I_{OUT} = 1.0 A, f = 120 Hz, 5.0 V_{pk-pk}
V_n	Output Noise		40		μV_{RMS}	10 Hz ≤ f ≤ 100 kHz, V_{IN} = 10 V
V_{DD}	Dropout Voltage (Note 3)		2.0	2.3	V	I_{OUT} = 3 A
I_{OS}	Short Circuit Current Limit		7.0	12.0	A_{pk}	V_{IN} = 10 V

Notes

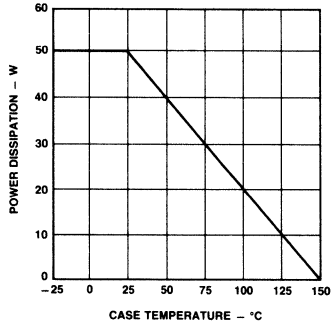
1. This voltage regulator offers output transistor safe area protection. However, to maintain full protection, the device must be operated within the maximum input-to-output voltage differential ratings, as listed on this data sheet under "Absolute Maximum Ratings." For applications violating these limits, device will not be fully protected
2. Load and line regulation are specified at constant junction temperature Pulse testing is required with a pulse width ≤ 1 ms and a duty cycle ≤ 5% Full Kelvin connection methods must be used to measure these parameters
3. Dropout Voltage is the input-output voltage differential that causes the output voltage to decrease by 5% of its initial value

Typical Performance Curves

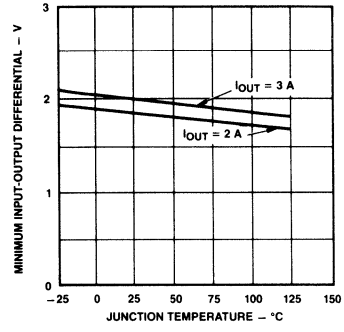
Short Circuit Current



Maximum Power Dissipation

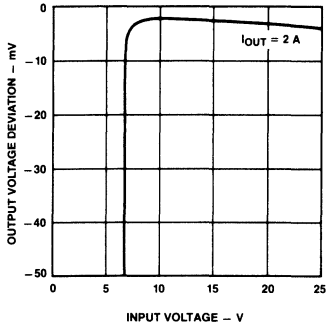


Dropout Voltage

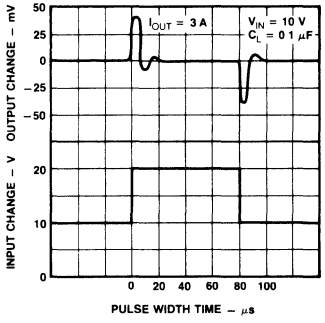


Typical Performance Curves (Cont.)

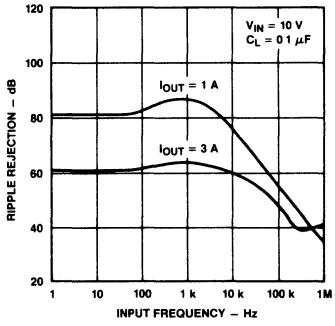
Line Regulation



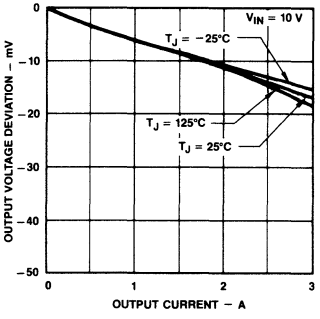
Line Transient Response



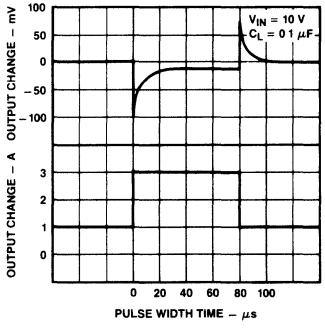
Ripple Rejection



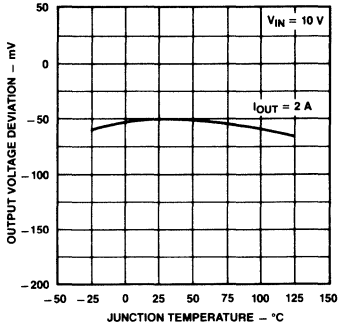
Load Regulation



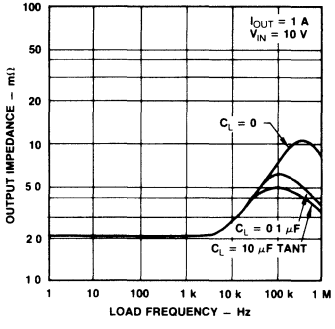
Load Transient Response



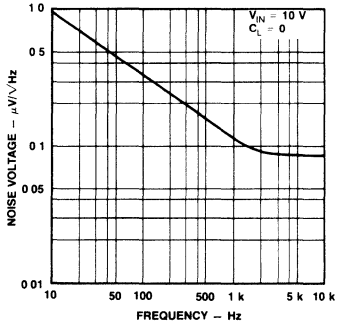
V_{OUT} vs Junction Temperature



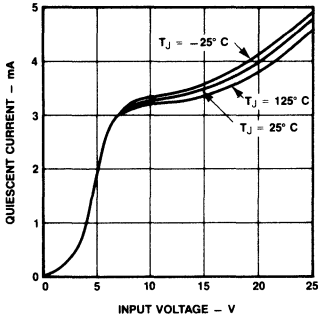
Output Impedance



Output Noise Voltage



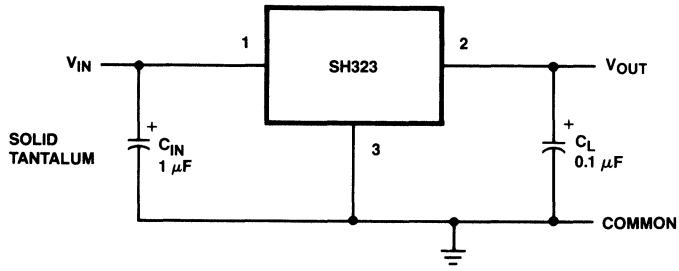
Quiescent Current



3

Test Circuit

Fixed Output Voltage



Design Considerations

This device has thermal overload protection from excessive power and internal short circuit protection which limits the circuit's maximum current. Thus, the device is protected from overload abnormalities. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C). It is recommended by the manufacturer that the maximum junction temperature be kept as low as possible for increased reliability. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used.

Package	Typ θ_{JC}	Max θ_{JC}
TO-3	1.8	2.5

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA})$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-case thermal resistance
θ_{CA} = Case-to-ambient thermal resistance
θ_{CS} = Case-to-heat sink thermal resistance
θ_{SA} = Heat sink-to-ambient thermal resistance

The device is designed to operated without external compensation components. However, the amount of external filtering of this voltage regulator depends upon the circuit layout. If in a specific application the regulator is more than four inches from the filter capacitor, a 1 μF solid tantalum capacitor should be used at the input. A 0.1 μF capacitor should be used at the output to reduce transients created by fast switching loads, as seen in the basic test circuit. These filter capacitors must be located as close to the regulator as possible.

Caution: Permanent damage can result from forcing the output voltage higher than the input voltage. A protection diode from output to input should be used if this condition exists.

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SH1605
5 A Efficient Switching Regulator

Hybrid Products

Description

The SH1605 is a hybrid switching regulator with high output current capabilities. It incorporates a temperature-compensated voltage reference, a duty-cycle controllable oscillator, error amplifier, high current-high voltage output switch, and a power diode. The SH1605 can supply 5 A of regulated output current over a wide range of output voltage.

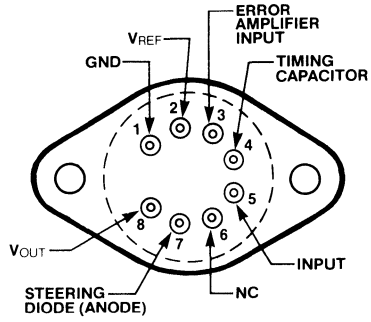
- **STEP DOWN SWITCHING REGULATOR**
- **OUTPUT ADJUSTABLE FROM 3.0 TO 30 V**
- **5 A OUTPUT CURRENT**
- **HIGH EFFICIENCY**
- **UP TO 150 W OUTPUT POWER**

Absolute Maximum Ratings

T_A = 25°C unless otherwise specified

V_{IN} - $V_{OUT(min)}$	5 V
Input Voltage	35 V Max
Output Current	6 A
Operating Temperature T_J	150°C
Internal Power Dissipation	20 W
Storage Temperature Range	−65°C to +150°C
Duty Cycle	20 ≤ D ≤ 80%
V_{7-8}	60 V
I_{7-8}	6 A

Connection Diagram
8-Pin TO-3 Type

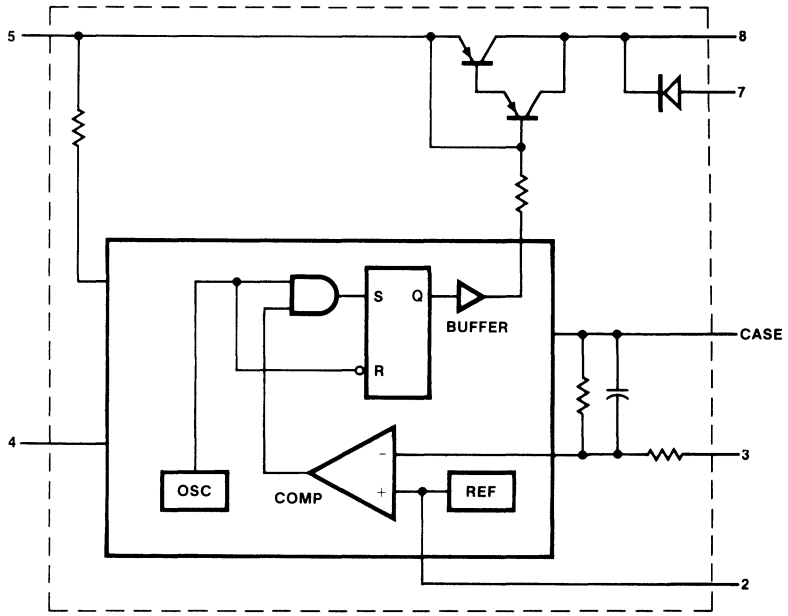


Case = Ground

Order Information

Type	Package	Code	Part No.
SH1605	Metal	8G	SH1605S

Block Diagram



Electrical Characteristics $T_C = 25°C$, $V_{IN} = 15$ V unless otherwise specified.

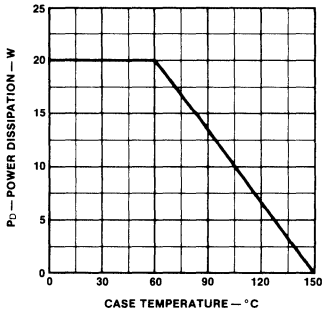
Symbol	Characteristics	Conditions	SH1605 Min	SH1605 Typ	SH1605 Max	Units
V_{OUT}	Output Voltage	$V_{IN} \geq V_O + 5$ V, $I_O = 2$ A	3.0		30.0	V
V_S	Switch Saturation	$I_{OUT} = 5.0$ A, $I_{OUT} = 2.0$ A		1.5 1.0	2.0 1.2	V V
V_F	Diode On Voltage	$I_{OUT} = 5.0$ A, $I_{OUT} = 2.0$ A		2.2 1.6	2.8 2.0	V V
V_{CC}	Supply Voltage		10		35	V
I_{RD}	Diode Reverse Current	$V_{RD} = 25$ V		2.0		μA
I_Q	Quiescent Current	$I_{OUT} = 0.2$ A		30		mA
Reference and Oscillator Section						
V_3	Voltage on Pin 3			2.5		V
$\Delta V_3/T$	V_3 Temperature Coefficient			150		ppm/°C
I_4	Charging Current—Pin 4			25		μA
V_4	Voltage Swing—Pin 4			0.5		V
I_{14}	Discharging Current—Pin 4			225		μA
Switching Characteristics						
Symbol	**Characteristics**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
t_r	Voltage Rise Time	$I_{OUT} = 2.0$ A $I_{OUT} = 5.0$ A		700 1.8		ns μs
t_f	Voltage Fall Time	$I_{OUT} = 2.0$ A $I_{OUT} = 5.0$ A		700 900		ns ns
t_s	Storage Time	$I_{OUT} = 5.0$ A		2.6		μs
t_d	Delay Time	$I_{OUT} = 5.0$ A		2.5		μs
Thermal Characteristics						
P_D	Power Dissipation	$I_{OUT} = 5.0$ A $V_{OUT} = 10$ V		16		W
η	Efficiency	$V_{OUT} = 10$V, $I_{OUT} = 5$ A		75		%
θ_{J-C}	Thermal Resistance			4.5		°C/W

Notes

1 θ_{C-A}. Typical is 30°C/W for natural convection cooling.

2. For heatsinking requirements see power derating curve.

Power Derating Curve



Design Equations

$$\text{Efficiency } (\eta) = \frac{P_{OUT} \times 100}{P_{IN}}$$

$$\text{Transistor DC Losses } (P_T) = I_{OUT} \times V_S \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

$$\text{Diode DC Losses } (P_D) = I_{OUT} \times V_F \frac{t_{OFF}}{t_{ON} + t_{OFF}}$$

$$\text{Drive Circuit Losses } (D_L) = \frac{V_{IN}2}{300} \times \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

Switching Losses Transistor:

$$(P_S) = V_{IN} \times I_{OUT} \frac{t_r + t_f}{2(t_{ON} + t_{OFF})}$$

$$\text{Transistor Duty Cycle} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Diode Duty Cycle} = \frac{t_{OFF}}{t_{ON} + t_{OFF}} = 1 - \frac{V_{OUT}}{V_{IN}}$$

$$\text{Power Inductor } (P_L) = I_{OUT}^2 \times R_L \text{ (Winding Resistance)}$$

Efficiency:

$$(\eta) = \frac{V_{OUT}\, I_{OUT}}{V_{OUT}\, I_{OUT} + P_T + P_D + D_L + P_S + P_L} \times 100$$

3

Design Considerations

Figure 1 is a typical design of a step-down switching regulator using the SH1605.

Nominal Design Objectives

V_{OUT} = +5 V	Line Regulation = 2%
$I_{OUT(max)}$ = 5.0 A	Load Regulation = 2%
$I_{OUT(min)}$ = 1.0 A	Ripple (max) = 0.1 $V_{pk\text{-}pk}$
V_{IN} = 12 to 18 V	Efficiency = 70%

First, R3 is calculated from *Equation 5*:

$$R3 = \frac{(2 \times 10^3)(V_{OUT} - 2.5)}{2.5} = 2\ k\Omega$$

Since the required $I_{OUT(min)}$ is 1 A to maintain continouous operation, the peak-to-peak current excursion must be equal to 2 A or less, i.e.,

$$\Delta I_1 = 2\ I_{OUT(min)}$$

To calculate the value of the inductor, assume the nominal on time of the system as 60 μs. This value is chosen keeping the efficiency / component-size trade-off in mind. From *Equation 1*.

$$L1 = \left(\frac{V_{IN} - V_{OUT}}{\Delta I_1}\right) t_{on} = \frac{10}{2}(6 \times 10^{-5}) = 300\ \mu H$$

where $V_{IN(nom)}$ = 15 V, t_{on} = 60 μs

$$\Delta I_1 = 2\ A$$

One very important element in achieving the optimum performance in a switching regulator is to insure the inductor is kept below the specified saturation limits.

Since the timing capacitor controls the 60 μs on time, C_T can be determined using *Equation 7*:

$$C_T = \frac{(t_{on})(I_C)}{\Delta V} = \frac{(6 \times 10^{-5})(2.5 \times 10^{-5})}{5 \times 10^{-1}} = 3000\ pF$$

where I_C = 25 μA nominal per data sheet.

The final step is to determine the requirements for the output capacitor C_O to obtain the desired value of ripple voltage. Consideration must be given to the absolute value of C_O as well as the internal effective series resistance (ESR). Since the capacitor size is inversely proportional to the operating frequency, the lowest frequency of operation must be calculated. Minimum operating frequency can be determined by using $\Delta I_{1(max)}$ vs $\Delta I_{1(nom)}$ in *Equation 9*.

$$\text{Minimum Frequency} = \frac{1}{1.3 \times 10^{-4}} = 7.7\ kHz$$

The output capacitor can now be determined as follows:

$$C_{O(min)} = \frac{\Delta 1_1}{(8\ f_{(min)}\ V_{ripple(max)})}$$

$$= \frac{2}{(8 \times 7.7 \times 10^3) \times (1 \times 10^{-1})}$$

$$= 325\ \mu F$$

The maximum acceptable ESR is therefore

$$ESR(max) = \frac{V_{ripple(max)}}{\Delta I_{1(max)}} = 0.025\Omega$$

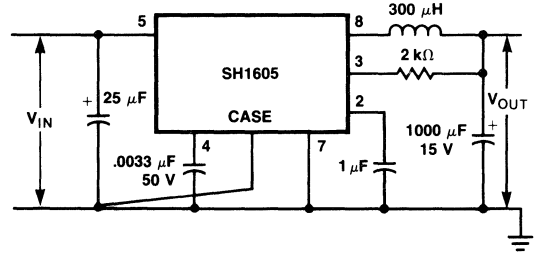
Normally, the minimum capacitance value should be increased considerably if a low ESR capacitor is not used.

As a final step for minimizing switching transients at the device input, a low ESR capacitor must be used for decoupling purposes between the input terminal and ground.

The SH1605 is a highly versatile building block for high current, step-down switching regulator systems. However, to attain optimum performance and reliability the following guidelines should be followed:

- Keep operating period long, relative to the device switching times, for optimum efficiency.
- Insure that the inductor stays out of saturation and minimize the series resistance.
- Use high quality capacitors for input and output to minimize ripple and noise.

Fig. 1 Design Example



Note

Circuit Performance

V_{IN} = 12-18 V

V_{OUT} = 5 06 V

Load Reg = 50 mV (1 A $\leq I_{OUT} \leq$ 5 A)

Line Reg = 50 mV (12 V $\leq V_{IN}$ 18 V)

SH1605 must be mounted on a heat sink with a maximum thermal resistance of $\phi_{CA} \leq 4°$ C/W

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Testing Operational Amplifiers

Linear Products

What is an OP AMP?

An operational amplifier is a direct-coupled high-gain amplifier, often powered by both a positive and a negative supply so that the output can swing both above and below ground. When used by itself, the op amp is limited, because the high gain (80 dB or much higher) causes saturation, since the output swings as far as possible toward one of the supplies. However, with feedback applied in a closed-loop configuration, the op amp becomes a useful device. Since the properties of the closed-loop circuit depend primarily on characteristics of the feedback components rather than the op amp, and since typical feedback components, i.e., resistors and capacitors, have high precision and low drift, closed-loop op amp circuits can be very accurate and stable.

The name operational amplifier is derived from one of the original uses of closed-loop op amp circuits, performing mathematical operations in analog computers. Early op amps used a single, ground-referenced inverting input, where a positive voltage change at the input caused a negative change at the output. The more versatile, modern op amps have two floating inputs—one inverting and one non-inverting. Since an op amp responds equally to the two inputs, the output depends on the difference between the inputs, known as differential inputs. A common-mode signal, applied equally to both inputs, is ignored since there is no difference between inputs. By grounding one of the inputs, the differential amplifier becomes a ground-referenced amplifier.

With negative feedback applied to an inverting input, the op amp continually adjusts the output to minimize (or null) the differential input voltage. Because the gain of the op amp is so high, the nulled input voltage is always small, regardless of the output voltage. For example, if the gain is 100,000 and output is at 10 V, the differential input is only 100 μV, a negligible voltage. Thus, it can be said that the op amp with negative feedback is continually adjusting the outputs to keep the inputs at the same voltage.

Major dc Parameters

There are seven important parameters that are tested and guaranteed on all modern IC op amps. In the following discussions, input voltage refers to the differential voltage at zero common-mode voltage.

Input Offset Voltage V_{OS}
Ideally, the output voltage should be zero when the input voltage is zero, but practically, there will always be small mismatches in the amplifier components. Input offset voltage is the input voltage required to zero the output, typically a millivolt or two. V_{OS}, usually caused by mismatches in the base-emitter voltages of the amplifier input transistors, is undesirable in a direct-coupled circuit because the circuit will usually amplify it, causing a large dc error, which is temperature-dependent.

To avoid the effects of input currents, V_{OS} should ideally be measured at zero source impedance (resistance from each input to ground). For testing purposes, some low impedance, usually 50 ohms, is used.

Input Bias Current I_B
Although op amp inputs ideally draw no current, practically, some bias current must flow into each input. For op amps with bipolar transistors at the input, I_B is the base current of the input transistor, typically 100 nA. Where source impedance is low, I_B has no effect; but in high-impedance circuits, a voltage (I_B x source resistance) will appear at the amplifier input. This error is similar to V_{OS} and is also temperature-dependent.

Because of the design of differential stages, the two I_Bs of an op amp vary with the input voltage, but their sum remains constant. The parameter usually tested is the total input bias current $I_{B(Total)} = (I_{B(inverting)} + I_{B(noninverting)})$.
The average input bias current specified on data sheets is just $I_{B(Total)}/2$.

Occasionally, it is necessary to measure the two input currents separately. To make $I_{B(Total)}$ divide evenly between the two inputs and not in a random way, dependent on V_{OS}, the standard convention is to null the op amp in a feedback loop.

Input Offset Current I_{OS}
Because an op amp has differential inputs, many of the effects of the two input currents can be eliminated if both currents are equal, since equal effects at both inputs would cancel. Practically, the two input currents cannot be made exactly equal, so the difference between them is specified. The input offset current is the difference between the two input currents when the op amp is nulled. In applications where the inputs are operated from equal source impedance, I_{OS} is the parameter of interest.

In op amps with a simple input stage, like the μA709 or μA749, I_{OS} is dependent on the beta match of the input transistors. In more complicated devices, like

4

the μA741, I_{OS} also depends on matching the current sources that supply the input transistors.

High-Impedance Composite Input Offset Voltage V_{OS} 10 k
The input offsets of an op amp are fully specified by either:

V_{OS}, $I_{B(inv)}$, $I_{B(ninv)}$ or V_{OS}, I_{OS}, $I_{B(Total)}$

In either case, common-mode and differential input voltages can be calculated for any source resistances, equal or unequal. In applications with equal source resistors, V_{OS} dominates at low impedances and I_{OS} dominates at high impedances. At some intermediate resistance, V_{OS} and I_{OS} effects are about equal and may add or cancel, depending on their signs which are statistically uncorrelated. If they add, the composite offset will be greater than V_{OS} and may even be greater than the data sheet limit for V_{OS}. To guard against this possibility, a high-impedance composite input offset voltage at a specified source resistance, usually 10 k, is tested and guaranteed. V_{OS} 10 k is not an independent parameter of an op amp; it is a calculated number, determined by the interaction of the independent parameters V_{OS} and I_{OS} with external source resistors.

Voltage Gain
The gain of an op amp, as with any other amplifier, is the ratio of a change in the output voltage to a change in the input voltage. Gain can be specified in V/V or in dB. The symbol A_{VOL} in used to indicate open-loop voltage gain, the gain of the amplifier without feedback.

Common Mode Rejection Ratio CMRR
Ideally, an op amp ignores common-mode signals. Practically, there will always be some small response. The standard convention for measuring this response is to null the amplifier, then measure the change in V_{OS} when large common-mode voltages are applied. The common mode rejection ratio CMRR is the ratio of change in V_{OS} to the change in common-mode voltage, specified in dB. To avoid a minus sign (−100 dB, −70 dB), CMRR is often specified "upside-down" as the change in common-mode voltage over the change in V_{OS}. Typical op amps have 80 to 100 dB CMRR.

Power Supply Rejection Ratio PSRR
Power supply rejection ratio is a measure of the ability of the op amp to ignore changes in the power supply voltages. The change in V_{OS} is measured as the supplies are varied. Power supply rejection ratio PSRR is the ratio of the change in V_{OS} to the total change in power supply voltage. For example, if the supplies vary from ±5 V to ±20 V, the total change is 40 − 10 = 30 V. PSRR is usually specified in μV/V or sometimes in dB, in which case the "upside-down" form is used. Typical op amps have 30 μV/V (90 dB) PSRR.

Minor dc Parameters Usually Specified

Output Swing
Ideally, the output voltage of an op amp should be able to swing all the way to either supply. However, real op amps saturate within a volt or two of the supplies, depending on how many base-emitter junctions and/or saturated transistors are involved. Op amp output stages are usually complementary-symmetry emitter followers, so output impedance is low, whether the op amp is sinking or sourcing output current. To ensure that both the npn and pnp are operating, both positive and negative swing are tested, with an external resistor connected to load the output.

Output Short-Circuit Current I_{SC}
Most recent op amps have a protective current limit built into the output. If the output is short circuited or otherwise overloaded, the output current limits at some safe value, typically 25 mA. The current limit circuits for each direction of current (sourcing and sinking) are independent and must be tested separately, although they are designed to limit at the same value.

I_{SC} is generally tested under worst-case conditions. For example, an input voltage is applied to cause the output to swing to positive saturation, but the output is then shorted to the negative supply and held there while I_{SC} is read. This causes maximum power dissipation in the output transistor.

Supply Current I_S or I_{SUP}
The standby current of the amplifier is measured when the output is at zero. In modern op amps that have no ground terminal, the standby current into the V+ lead is equal to the standby current out of the V− lead and could be measured at either terminal. In older op amps, such as the μA702, that do have a ground terminal, the currents must be measured separately.

Power Consumption
Power consumption is determined by multiplying the supply current times the total supply voltage. This parameter is guaranteed by the I_S test.

Offset Adjust $V_{OS(adj)}$
Some op amps have a pair of offset adjust terminals. Zero offset voltage can be obtained by adjusting a potentiometer connected between these terminals. Test each $V_{OS(adj)}$ terminal by measuring V_{OS} while the terminal is shorted to V−. This indicates the maximum effect of the terminal on V_{OS}.

DC Stress Tests

Data Sheets always include "absolute maximum" limits on common-mode input voltage, differential input voltage, and supply voltage. To guarantee these ranges, any of several tests can be performed. Sometimes a measurement is taken during the test if

there is some measurable indication of a failure. Other times, certain voltages are simply applied and removed before the main test sequence.

Common-Mode Stress
This is not usually tested. The inputs are moved over a large common-mode voltage range during CMRR; since the absolute maximum range is only slightly larger, a separate test is usually unnecessary.

Differential Stress (Input Leakage—IL)
In this test, the inputs are subjected to absolute maximum differential input voltage. All of $I_{B(Total)}$ will flow in the more positive input and the more negative input should see nothing but leakage. Breakdown occurs if the input stage is defective. Input leakage is often measured during the test.

Supply Stress
Supply current is measured under absolute maximum supply voltages.

Internal MOS Capacitor Test—Cap Stress
Many modern op amps include a small MOS capacitor on the chip to set the amplifier frequency response. The silicon dioxide dielectric of the cap is made only thick enough to withstand the absolute maximum total supply voltage. To test the dielectric, maximum supplies are applied and the circuit is swung to whichever state puts the full voltage across the cap. The output is often measured. Typically, if the dielectric ruptures, the amplifier will latch up in an improper state; the output will go negative when it should be positive.

AC Parameters

Since ac parameters are not usually tested in production, only typical values are shown on the data sheet. However, three common ac parameters should be recognized.

Risetime and Overshoot
The small-signal step response is a simple test that indicates both the bandwidth and stability of an amplifier under specified conditions. The risetime is related to the bandwidth, and the overshoot is a measure of stability.

Slew Rate
Slew rate is a large-signal phenomenon resulting from the capacitor connected to adjust the small-signal frequency response. So that the capacitors can be small, they are usually connected to high-impedance nodes in the circuit, that receive dc bias from current sources. If the amplifier is to reproduce a large signal, such as a 10 V step, the circuit no longer behaves according to its small-signal model. The current source at the compensation node cannot pump enough current into the cap to move the output far enough, fast enough. If current (I) is provided to the cap (C), the output will *slew* toward the final value at a slew rate $dV/dt = I/C$. Slew rate limiting (or rate limiting) occurs with all large, fast signals when current to the capacitor is insufficient.

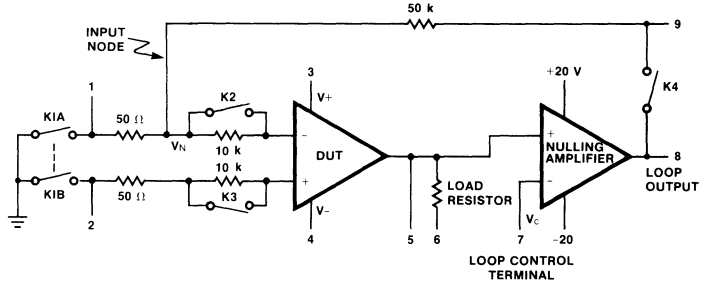
The Basic OP AMP Test Loop

All op amps are basically alike, high-gain differential amplifiers. The reason there are so many different op amps is that no one circuit design can possibly optimize all the dc and ac parameters. Op amps are designed to optimize a parameter (high gain, low power consumption, etc.) for particular applications. Fortunately for test engineers, however, the similarities of all op amps are so great that a single test circuit can be used to perform all standard dc tests. This circuit, shown in *Figure 8-1*, is the basic op amp test loop.

Performing all tests requires five power supplies: the V+ and V− supplies for the device under test (DUT), a control voltage V_C applied at the loop control terminal, and supplies to run the nulling amplifier, usually ± 15 V or ± 20 V.

Operation of the test loop, with all relays closed, is as follows:
- The inverting input of the nulling amplifier is the control terminal of the loop. The DUT output is connected to the non-inverting input of the null amplifier.
- The null amplifier output controls the DUT input through the feedback divider.
- There is one inversion in the loop, provided by the DUT. Therefore, the null amplifier operates with negative feedback.

Fig. 8-1 Basic Op Amp Test Loop



- With negative feedback, the null amplifier continually adjusts its output to keep its input voltages equal.
- Therefore, the null amplifier adjusts the loop output so that the DUT output follows the control terminal.

The input node voltage, V_N in *Figure 8-1*, is always 1/1000th of the loop output voltage (actually it is 1/1001th, but it is common to neglect the 0.1% error). Thinking in reverse, the circuit has a closed-loop gain of 1000 and any voltage V_N appears 1000 times larger at the loop output. Since the input voltages to the nulled op amp are always very small, the gain simplifies measurements.

Equations for V_N

Figure 8-2 shows the DUT portion of the test loop, leaving out the 50 Ω resistors since their effect is negligible in this analysis. V_{OS} is represented as a small voltage source moved outside the op amp. Current flows into both inputs of the op amp. With V_N adjusted by feedback to produce a DUT output of zero, and with V_{OS} accounted for externally, no voltage exists between the op amp inputs; *zero in* means *zero out*. V_N equations can now be written for the various settings of K2 and K3

K2 closed, K3 closed: $V_{N1} = V_{OS}$

The input bias currents have no effect because there is no source resistance.

K2 closed, K3 open: $V_{N2} = V_{OS} - I_{B(ninv)} \times 10\ k$

With only K3 open, V_N is a composite voltage involving V_{OS} and $I_{B(ninv)}$. To test $I_{B(ninv)}$, measure V_{N2}, then subtract it from V_{N1} (equal to V_{OS}).

K2 open, K3 closed: $V_{N3} = V_{OS} + I_{B(inv)} \times 10\ k$

To measure $I_{B(inv)}$, subtract V_{OS} from V_{N3}.

K2 open, K3 open:

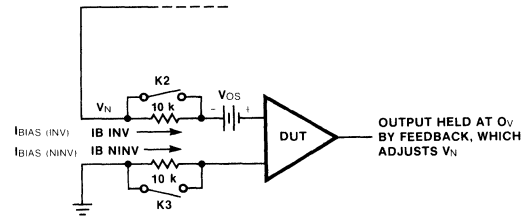
$$V_{N4} = -I_{B(ninv)}\ (10\ k) + V_{OS} + I_{B(inv)}\ (10\ k)$$
$$= V_{OS} + \left(I_{B(inv)} - I_{B(ninv)}\right)\ (10\ k)$$
$$= V_{OS} + I_{OS}\ (10\ k)$$
$$= V_{OS}\ 10\ k$$

V_{N4} is the high-impedance composite input offset voltage. To measure I_{OS}, subtract V_{OS} from V_{N4}.

Each relay setting combination provides an easy way to measure some important parameter of the op amp. For a measurement of $I_{B(total)}$, measure V_{N3} and subtract it from V_{N2}.

$$\Delta V_N = V_{OS} + I_{B(inv)}\ (10\ k) + I_{B(ninv)}\ (10\ k) - V_{OS}$$
$$= \left(I_{B(inv)} + I_{B(ninv)}\right)\ (10\ k)$$
$$= I_{B(total)}\ (10\ k)$$

Fig. 8-2 Simplified Input Circuit For Calculating V_N



Testing Using the Op Amp Test Loop

For the following tests of op amp parameters, refer to the test loop schematic, *Figure 8-1*, whenever necessary. All relays are normally closed.

Input Offset Voltage V_{OS}

Set the loop control voltage V_C to zero. The nulling amplifier immediately adjusts the loop output to zero the DUT output. By definition, the input node voltage V_N equals V_{OS}; therefore, the loop output is 1000 V_{OS}. For example, if the loop output reads 1.0 V, V_{OS} is 1.0 mV.

Input Currents (Separately)

Measure V_{OS}. Then open K2 and K3 alternately and compute the changes in V_N as previously described. Because 1000 V_N is always read at the loop output, a voltage change $\Delta V_N = 1000 \times I_B \times 10\ k$ will be measured. Thus, if I_B is 100 nA, the measured change will be 1.0 V.

Total Input Bias Current $I_{B(total)}$

This was explained in the previous section. Measure V_{N2}; then measure V_{N3} and subtract. The measured change at the loop output is 1000 x $I_{B(total)}$ x 10 k. An alternate method to test $I_{B(total)}$ is to open K1 and K4, tie pins 1 and 2 together, and use a current meter to read $I_{B(total)}$. The industry trend is for dynamic testing, however, since there is some small inaccuracy associated with the latter method.

High-Impedance Composite Input Offset Voltage V_{OS} 10 k

Measure V_{N4} as previously described.

Input Offset Current I_{OS}

Measure V_{OS}. Then measure V_{OS} 10 k and subtract. $\Delta V = (1000)\ (I_{OS})\ (10\ k)$.

Gain

In testing low-gain ac amplifiers, such as audio amplifiers, the normal procedure is to apply a small, known input and measure the large ac output. When testing high-gain dc amplifiers, such as op amps, the reverse procedure is used. The test loop is used to vary the output over a large, known range, and the dc change at the input is measured.

A normal test for a DUT using ± 15 V supplies is to measure the average dc gain over the output range −10 V to +10 V. Since gain is always specified

with a load resistor, pin 6 should be grounded. Set $V_C = -10$ V; the null amplifier brings the DUT output to −10 V. Measure V_N. Then set V_C to +10 V; the null amplifier brings the DUT output to +10 V. Measure the change in V_N. For example, if the gain is 100,000 and the total output change is 20 V (−10 V to +10 V), the loop output change should be (1000) (20/100,000) = 200 mV.

Note that the DUT is tested at the inverting input; therefore, if the output goes from −10 V to +10 V (a positive change), a small negative change should be seen at the input.

As mentioned previously, gain is always tested with an external load resistor, often 2 kΩ. Since the op amp output stage must provide current to this resistor, the output stage must dissipate power. If the op amp is an IC, a thermal signal will then travel across the chip to the input stage, where it mixes with the true, circuit-related input signal. Depending on the relative sizes of the circuit and thermal components, this may cause peculiar readings to occur during a gain test. If the thermal component partially cancels the circuit component, the change in V_N will be smaller than normal, indicating a larger gain. If the two components cancel, no change in V_N will be read, indicating an effective gain of infinity. If the thermal component is larger than the circuit component, a wrong-polarity change in V_N will occur, indicating a "negative gain."

There is no general agreement in industry about the significance or seriousness of "negative gain." Devices that show negative gain in a test circuit usually behave normally in customer applications. Nevertheless, a device exhibiting a large negative gain may be questionable. Fairchild's policy is to allow a wrong-polarity reading of 20-100% of the right-polarity limit.[1]

[1]For a more complete discussion of thermal effects, see Solomon, J E "The Monolithic Op Amp A Tutorial Study," IEEE Journal of Solid State Circuits, Vol SC-9, No 6 (Dec, 1974)

To check the linearity of the op amp transfer function, gain is sometimes tested over two different parts of the output range. That is, instead of performing a single test as the output swings from −10 V to +10 V, gain is tested as the output swings from 0 V to +10 V, and then from 0 V to −10 V. Such testing will identify units that have very high gain over part of the output range and very low gain over the other part of the range.

Common Mode Rejection Ratio CMRR
The definition of CMRR might imply that testing involves holding V_C at zero and opening K1, tying pins 1 and 2 together to a voltage V_{CM}, then varying V_{CM} and reading the change in V_N at the loop output. However, this method does not provide accurate results. Because of the 50 Ω/50 kΩ feedback divider, only 99.9% of V_{CM} appears at the inverting input of the DUT. Since there is no divider at the non-inverting input, 100% of V_{CM} appears there, causing a 0.1% differential signal injected by the unbalanced test circuit. This error, only 60 dB below V_{CM}, is disastrous, for devices typically have 80 to 100 dB CMRR.

The obvious solution is to add another 50 kΩ resistor from the non-inverting input to ground, which should attenuate V_{CM} equally at both inputs to eliminate the differential error signal. The problem now becomes one of accurately matching the dividers. Advanced analysis of the four resistors as a bridge circuit indicates that, with careful matching, quite high CMRRs can be measured.

An easier solution eliminates the need for precisely matched pairs of precision resistors. Instead of holding V+, V− and V_C constant and moving pins 1 and 2, perform the inverse procedure. For example, to apply a V_{CM} of +10 V, leave K1 closed and change V+ from +15 V to +5 V. Then change V− from −15 V to −25 V and change V_C from 0 V to −10 V. From the point of view of the DUT, this is equivalent to the original method. The total supply voltage is still 30 V, the DUT output is still held at the midpoint between the supplies, and both inputs are 10 V above that midpoint, which makes $V_{CM} = +10$ V. However, from the point of view of the bridge, no V_{CM} has been applied, pins 1 and 2 are at ground as always, and V_N is the routine differential input voltage of the DUT.

This method permits accurate measurement of any CMRR without matched resistors. There is no need for a 50 kΩ resistor at the non-inverting input, since it would only shunt the 50 Ω resistor on all tests.

In summary, to measure CMRR, raise V+, V− and V_C to V_{CM} volts above nominal, and measure V_N. Then lower V+, V− and V_C to V_{CM} volts below nominal and measure the change in V_N.

Sometimes CMRR is tested with 10 kΩ source impedances (K2 and K3 open). In this case, any changes in I_{OS} contribute to the total change in V_N. A test with 10 k sources is not necessarily a more rigid test than with 50 Ω; the change in V_N may be larger or smaller, depending on how the V_{OS} and I_{OS} components interact.

Power Supply Rejection Ratio PSRR
The PSRR test is very direct and simple, with none of the problems that occur with CMRR testing. Hold V_C at zero, set both supplies to minimum values, and measure V_N. Then set both supplies to maximum values and measure the change in V_N. PSRR may also be tested with 10 kΩ source impedance.

Output Voltage Swings
Measure at pin 5, saturating the DUT output by applying a large differential input voltage.

There are three possible ways to saturate the DUT. The most direct way is to open K1 and K4 and apply the voltage directly across pins 1 and 2. Another way

is to open K4 only and apply a voltage at pin 9. This voltage is divided 1000:1, so 20 V at pin 9 will apply 20 mV to the DUT input, sufficient drive for almost any op amp. The third way is similar to the second except that all relays are closed and the null amplifier applies the 20 V to pin 9. Set V_C to 15 V; the null amplifier will immediately try to bring the DUT output to 15 V, but the DUT cannot swing all the way to V+. The null amplifier output eventually saturates around 18 V and the DUT output also saturates as desired.

Since output swings are always specified with a load resistor, pin 6 should be grounded.

Output Short-Circuit Current I_{SC}
This test involves the same procedure as in measuring voltage swing, except that instead of using load resistor on pin 6, connect a current meter from pin 5 to ground or to the worst-case opposite supply. When the DUT attempts to swing in response to the input, the current meter shorts the output and measures I_{SC}.

Supply Current I_S
Specifications usually indicate the DUT output should be zero, so set V_C to 0 and measure the current into pin 3. The state of the output has little effect on the I_S reading of recent op amps, biased internally by current sources. However, in earlier devices like the μA709, I_S is heavily dependent on the output state, even with nothing connected to the output.

Offset Adjust $V_{OS(adj)}$
The DUT of *Figure 8-1* has no offset adjust pins. Devices with offset adjust pins have relays to connect them alternately, usually to V−. V_C should be set to zero and a measurement taken at the loop output. At the least, the measurement should guarantee that the adjust range is sufficient to eliminate the V_{OS} of the particular device being tested. A more rigid test might require enough range to eliminate the worst possible V_{OS}, even though the DUT has a lower V_{OS}.

Common-Mode Stress
Open K1 and K4. Apply V_{CM} directly to pins 1 and 2.

Differential Stress (IL)
Open K1 and K4. Apply voltage directly across pins 1 and 2. Measure leakage at more-negative input.

Supply Stress
Perform supply current test at specified supplies.

Cap Stress
Test like output voltage swings, using specified supplies and swinging output to specified state.

Common Variations of the Basic Test Loop
The test loop is never used in the exact simplified form shown in *Figure 8-1*. Each op amp has quirks that require some variations on the basic theme. The following are some common variations.

AC Compensation Capacitors
While ac stabilization of the test loop is a complex topic, in general, each type of op amp has its own frequency response which may or may not be externally adjustable. When preparing a test loop for a particular device, it is necessary to use the frequency-response curves of the DUT and the null amplifier to determine which stabilization scheme to use and to predict which capacitors will be required.

Loop Output Noise Filter
A small RC noise filter with time constant around 1 ms is usually attached to the loop output and all measurements taken through this filter. The waveforms at the filtered output often prove to be much cleaner than the unfiltered version.

Source Resistors
Most general-purpose op amps are tested with 10 kΩ source resistors. However, op amps with very low input currents may use 50 k, 100 k, 1 M, or even 10 M resistors for improved resolution.

Test Loop Gain
The most common form of the test loop, with 50 kΩ/50 Ω resistor combination, gives a gain of 1000. For certain tests, usually $V_{OS(adj)}$, the 50 kΩ is split into a 45 kΩ and a 5 kΩ resistor, and the 45 kΩ resistor can be shorted with a relay to reduce the gain to 100. For devices with very low V_{OS}, a feedback resistor of 500 kΩ can be used to give a gain of 10,000.

MOSFETs in Place of K2 and K3
Some premium devices, such as the μA108, μA156, and μA725, have extremely low I_{BIAS} and/or V_{OS}. When testing these units, if reed relays are used for K2 and K3, difficulty may arise with the low-level properties of the reeds. Typical problems include thermally-generated EMFs, leakage current, and flexing of the reeds after closing. MOSFETs are usually a good substitute when reeds prove unsatisfactory. The high contact resistance of FETs (100 Ω) is not detrimental if the current passing through them is small, i.e., 1 nA. Benefits include clean switching, no thermal offsets, no leakage, no bounce, no microphonics, and no mechanical wear.

Conclusion

Because it works so well on the bench or in conjunction with high-speed automatic testers, the basic op amp test loop circuit is used universally by manufacturers and others who must test operational amplifiers. The test loop is so accurate and easy to use that it benefits even those who test only a few units on the bench.

FAIRCHILD

A Schlumberger Company

μA709
High Performance Operational Amplifier

Linear Products

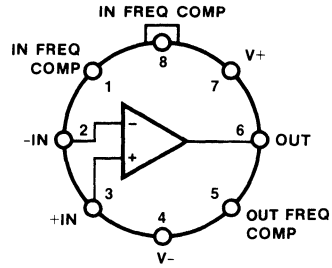
Description

The μA709 is a Monolithic High-Gain Operational Amplifier constructed using the Fairchild Planar epitaxial process. It features low-offset, high-input impedance, large input common mode range, high output-swing under load and low-power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little performance degradation. The amplifier is intended for use in dc servo systems, high impedance analog computers, low level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

Absolute Maximum Ratings

Supply Voltage	±18 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
Mini DIP	310 mW
DIP	670 mW
Flatpak	570 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Storage Temperature Range	
Metal and Flatpak	−65°C to +150°C
Molded DIPs	−55°C to +125°C
Operating Temperature Range	
Military (μA709A and μA709)	−55°C to +125°C
Commercial (μA709C)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Package, Flatpak (60 s)	300°C
Molded DIPs (10 s)	260°C
Output Short Circuit Duration	5 s

Connection Diagram
8-Pin Metal Package



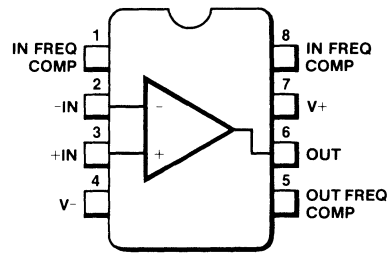
(Top View)

Pin 4 connected to case

Order Information

Type	Package	Code	Part No.
μA709A	Metal	5W	μA709AHM
μA709	Metal	5W	μA709HM
μA709C	Metal	5W	μA709HC

Connection Diagram
8-Pin DIP



(Top View)

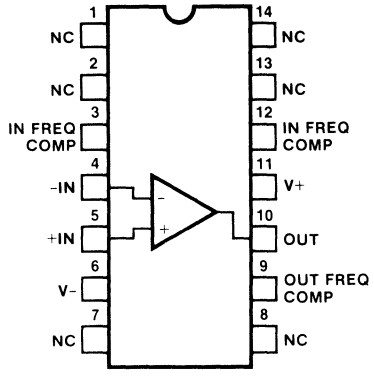
Order Information

Type	Package	Code	Part No.
μA709C	Molded DIP	9T	μA709TC

Note

Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal package, 8 3 mW/°C for DIP, 7.1 mW/°C for the flatpak and 5.6 mW/°C for the 8-pin DIP.

Connection Diagram
14-Pin DIP

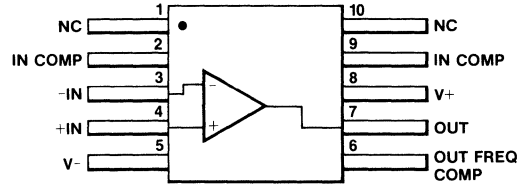


(Top View)

Order Information

Type	Package	Code	Part No.
μA709C	Molded DIP	9A	μA709PC

Connection Diagram
10-Pin Flatpak

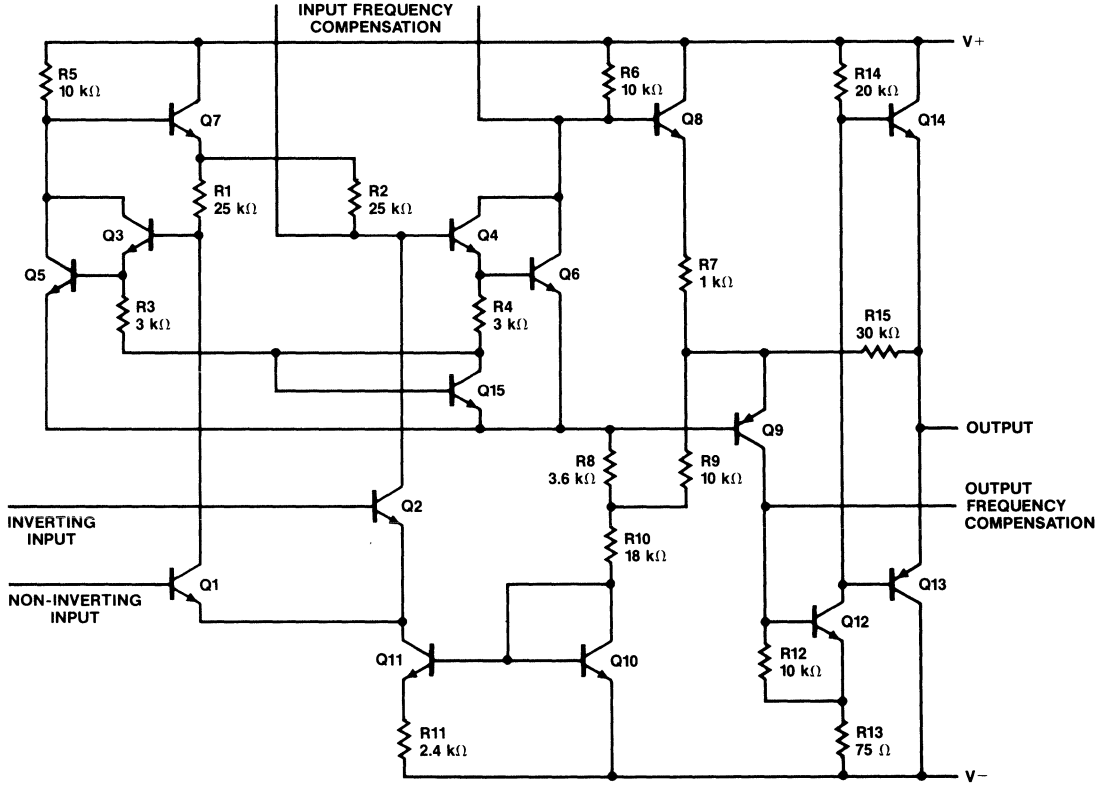


(Top View)

Order Information

Type	Package	Code	Part No.
μA709A	Flatpak	3F	μA709AFM
μA709	Flatpak	3F	μA709FM

Equivalent Circuit



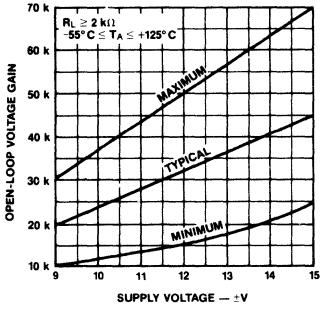
μA709A, μA709 and μA709C
Electrical Characteristics $T_A = +25°C$, $\pm 9\ V \leq V_S \leq \pm 15\ V$

Characteristic (see definitions)		Condition	709A			709			709C (V_S ± 15 V)			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage		$R_S \leq 10\ k\Omega$		0.6	2.0		1.0	5.0		2.0	7.5	mV
Input Offset Current				10	50		50	200		100	500	nA
Input Bias Current				100	200		200	500		300	1500	nA
Input Resistance			350	700		150	400		50	250		kΩ
Output Resistance				150			150			150		Ω
Supply Current		$V_S = \pm 15\ V$		2.5	3.6							mA
Power Consumption		$V_S = \pm 15\ V$		75	108		80	165		80	200	mW
Transient Response	Risetime	$V_S = \pm 15\ V$ $V_{IN} = 20\ mV$ $R_L = 2\ k\Omega$ $C1 = 5\ nF$			1.5		0.3	1.0		0.3		μS
	Overshoot	$R2 = 50\Omega$ $C_L \leq 100\ pF$ $R1 = 1.5\ k\Omega$ $C2 = 200\ pF$			30		10	30		10		%
The following specifications apply for the operating temperature range												
Input Offset Voltage		$R_S \leq 10\ k\Omega$			3.0			6.0			10.0	mV
Average Temperature Coefficient of Input Offset Voltage		$R_S = 50\Omega$		1.8	10		3.0					μV/°C
		$R_S \leq 10\ k\Omega$		4.8	25		6.0					
Input Offset Current		T_A = HIGH		3.5	50		20	200				nA
		T_A = LOW		40	250		100	500			750	
Average Temperature Coefficient of Input Offset Current		$T_A = +25°C$ to $+125°C$		0.08	0.5							nA/°C
		$T_A = +25°C$ to $-55°C$		0.45	2.8							
Input Bias Current		$T_A = -55°C$		300	600		500	1500			2000	μA
Input Resistance		$T_A = -55°C$	85	170		40	100		35	80		kΩ
Input Voltage Range		$V_S = \pm 15\ V$	±8.0	±10		±8.0	±10		±8	±10		V
Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	80	110		70	90					dB
Supply Voltage Rejection Ratio		$R_S \leq 10\ k\Omega$		40	100		25	150				μV/V
Large Signal Voltage Gain		$V_S = \pm 15\ V$ $R_L \geq 2\ k\Omega$ $V_{OUT} = \pm 10\ V$	25		70	25	45	70	15	45		V/mV
Output Voltage Swing		$V_S = \pm 15\ V$ $R_L \geq 10\ k\Omega$	±12	±14		±12	±14					V
		$V_S = \pm 15\ V$ $R_L \geq 2\ k\Omega$	±10	±13		±10	±13					
Supply Current		T_A = HIGH		2.1	3.0							mA
		T_A = LOW		2.7	4.5							

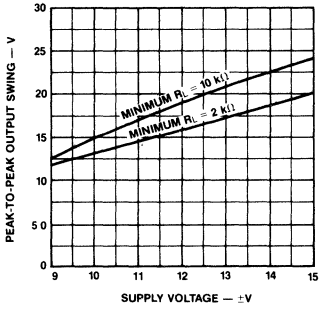
4

Typical Performance Curves for μA709A

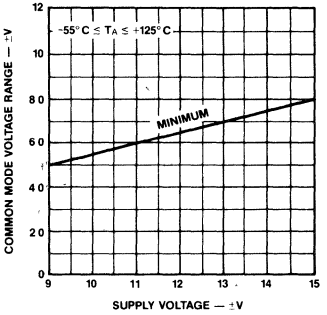
Voltage Gain as a Function of Supply Voltage



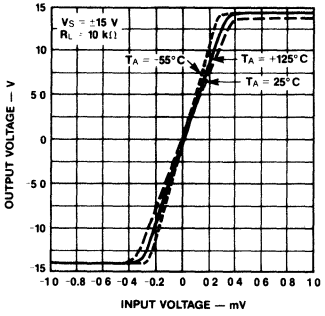
Output Voltage Swing as a Function of Supply Voltage



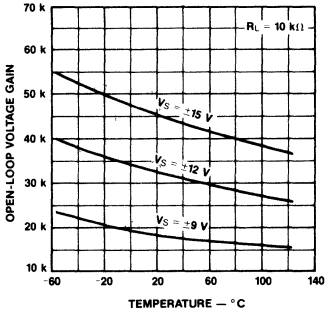
Input Common Mode Voltage Range as a Function of Supply Voltage



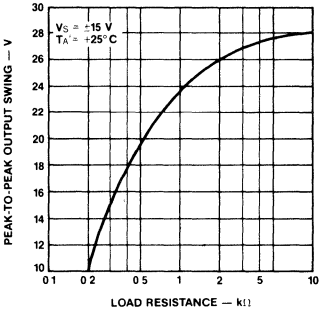
Voltage Transfer Characteristic



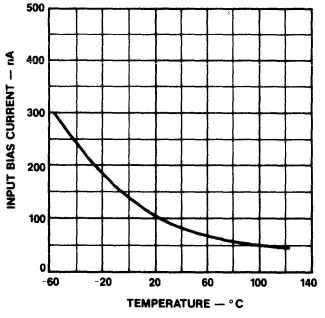
Voltage Gain as a Function of Ambient Temperature



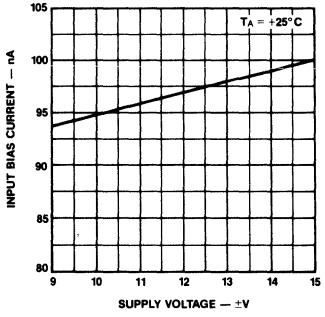
Output Voltage Swing as a Function of Load Resistance



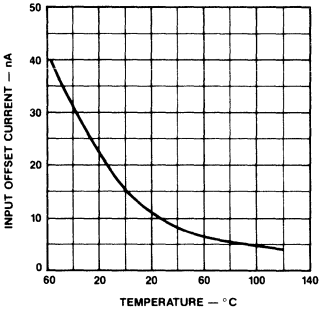
Input Bias Current as a Function of Ambient Temperature



Input Bias Current as a Function of Supply Voltage

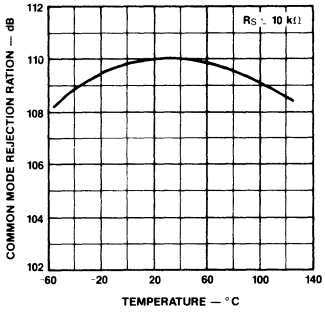


Input Offset Current as a Function of Ambient Temperature

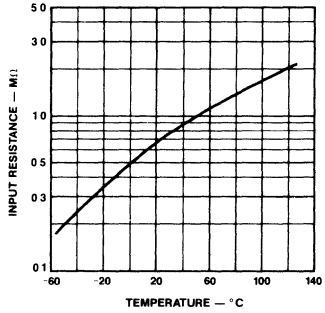


Typical Performance Curves for μA709A (Cont.)

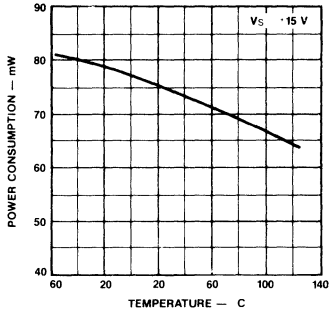
Common Mode Rejection Ratio as a Function of Ambient Temperature



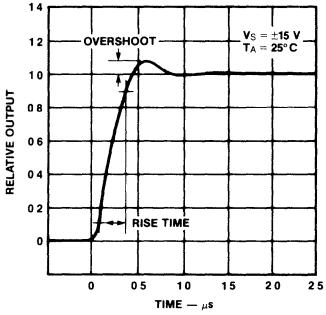
Input Resistance as a Function of Ambient Temperature



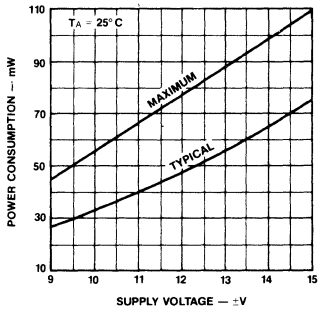
Power Consumption as a Function of Ambient Temperature



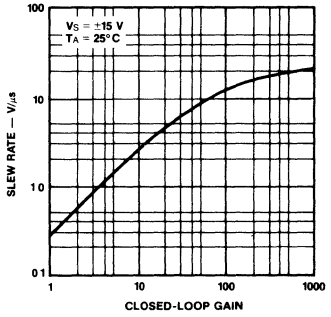
Transient Response



Power Consumption as a Function of Supply Voltage

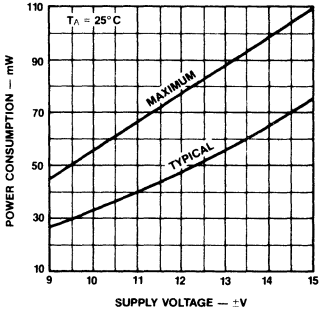


Slew Rate as a Function of Closed-Loop Gain Using Recommended Compensation Networks

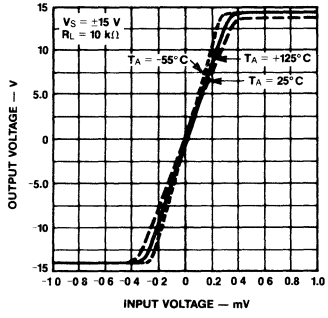


Typical Performance Curves for μA709 and μA709C

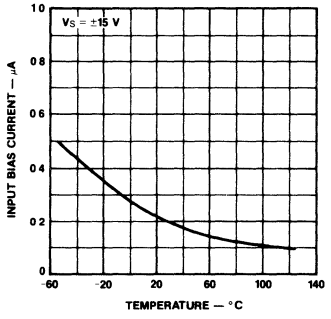
Power Consumption as a Function of Supply Voltage



Voltage Transfer Characteristic

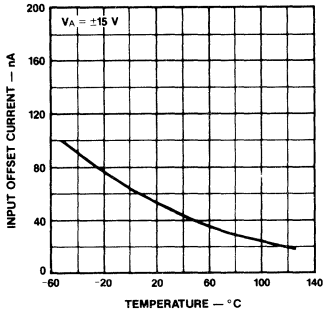


Input Bias Current as a Function of Ambient Temperature

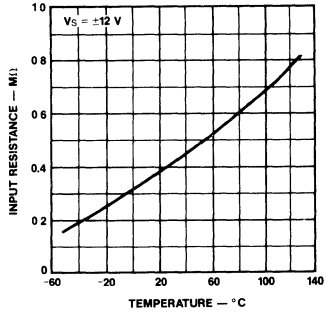


Typical Performance Curves for μA709 and μA709C (Cont.)

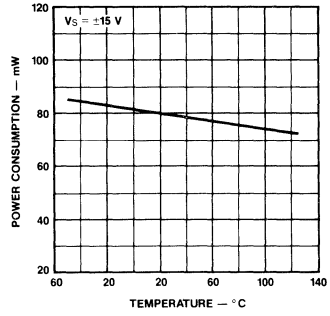
Input Offset Current as a Function of Ambient Temperature



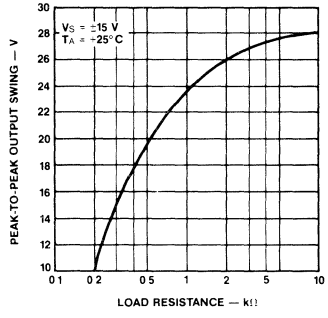
Input Resistance as a Function of Ambient Temperature



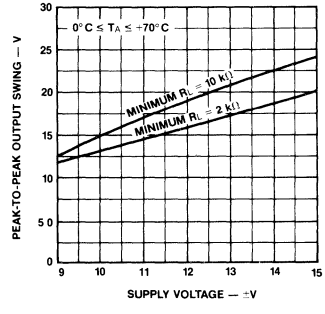
Power Consumption as a Function of Ambient Temperature



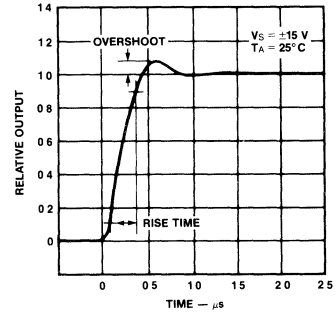
Output Voltage Swing as a Function of Load Resistance



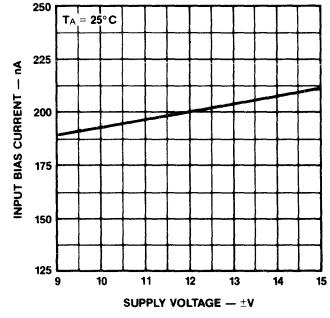
Output Voltage Swing as a Function of Supply Voltage



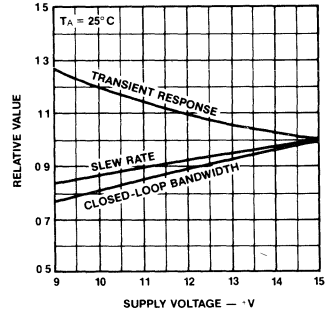
Transient Response



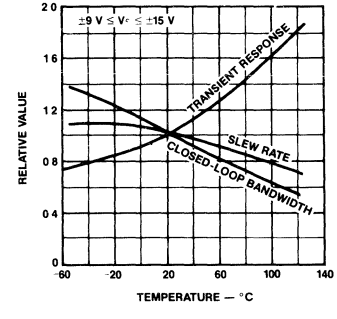
Input Bias Current as a Function of Supply Voltage



Frequency Characteristics as a Function of Supply Voltage

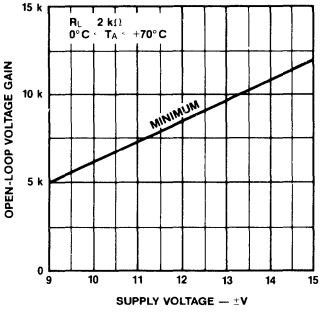


Frequency Characteristics as a Function of Ambient Temperature

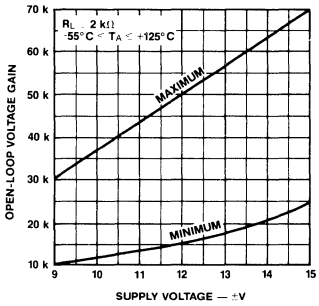


Typical Performance Curves for μA709 and μA709C (Cont.)

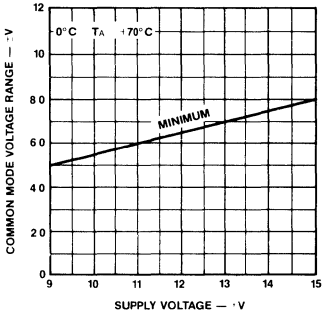
Voltage Gain as a Function of Supply Voltage (709C only)



Voltage Gain as a Function of Supply Voltage (709 only)

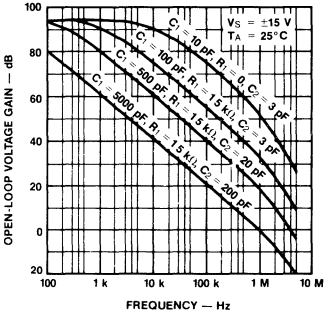


Input Common Mode Voltage Range as a Function of Supply Voltage

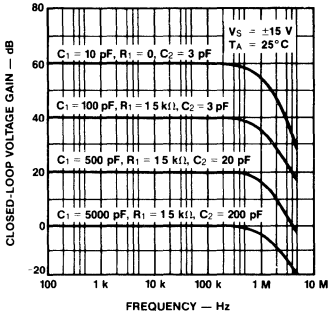


Frequency Compensation Curves For All Types

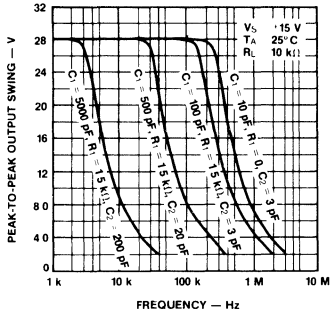
Open-Loop Frequency Response for Various Values of Compensation



Frequency Response for Various Closed Loop Gains

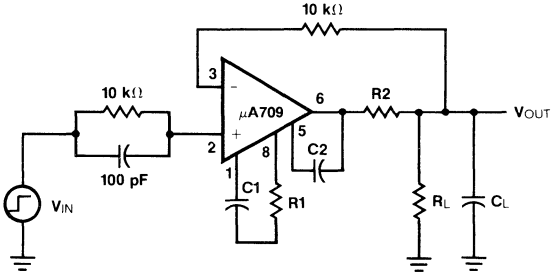


Output Voltage Swing as a Function of Frequency for Various Compensation Networks



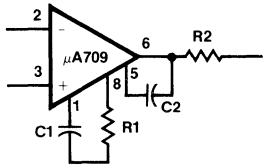
Test Circuits

Transient Response Circuit



Note
Pin numbers on this and all succeeding circuits apply to metal can or mini DIP package.

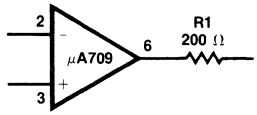
Frequency Compensation Circuit



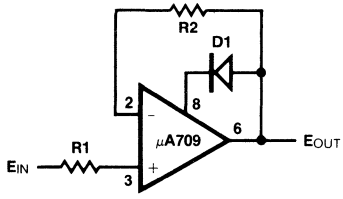
Note
Use R2 = 50 Ω when the amplifier is operated with capacitive loading

Protection Circuits

Output Short-Circuit Protection

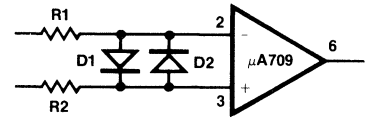


Latch-Up Protection

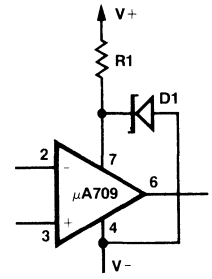


Pin numbers apply to metal can or mini DIP package only.

Input Breakdown-Protection



Supply Overvoltage-Protection



FAIRCHILD

A Schlumberger Company

μA714
Precision Operational Amplifier

Linear Products

Description

The μA714 is a Monolithic Instrumentation Operational Amplifier constructed using the Fairchild Planar epitaxial process. It is intended for precise, low-level signal amplification applications where low noise, low drift and accurate closed-loop gain are required. The offset null capability, low-power consumption, very high-voltage gain as well as wide power-supply voltage range provide superior performance for a wide range of instrumentation applications.

- **LOW OFFSET VOLTAGE 75 μV**
- **LOW OFFSET VOLTAGE DRIFT 1.3 μV/°C**
- **LOW BIAS CURRENT ±3.0 nA**
- **LOW INPUT NOISE CURRENT 0.17 pA/√Hz @ 1.0 kHz MAX**
- **HIGH OPEN LOOP GAIN 500,000 TYPICALLY**
- **LOW INPUT OFFSET CURRENT 2.8 nA MAX**
- **HIGH COMMON MODE REJECTION 110 dB MIN**
- **WIDE POWER SUPPLY RANGE ±3.0 TO ±22 V**

Absolute Maximum Ratings

μA714, μA714E, μA714C

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±22 V
Storage Temperature Range	
Metal Package	−65°C to +150°C
Operating Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Pin Temperature	
Metal Package (Soldering, 60 s)	300°C

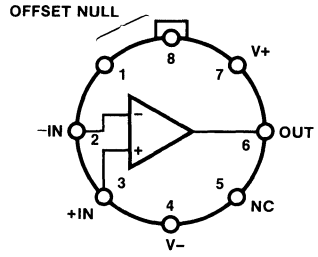
μA714L

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±18 V
Storage Temperature Range	
Metal Package	−65°C to +150°C
Operating Temperature Range	
Military	
Commercial	0°C to +70°C
Pin Temperature	
Metal Package (Soldering, 60 s)	300°C

Notes

1. Ratings applies to ambient temperature to 70°C. Above T_A = 70°C derate linearly 6.3 mW/°C.
2. For supply voltage less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Connection Diagram
8-Pin Metal Package



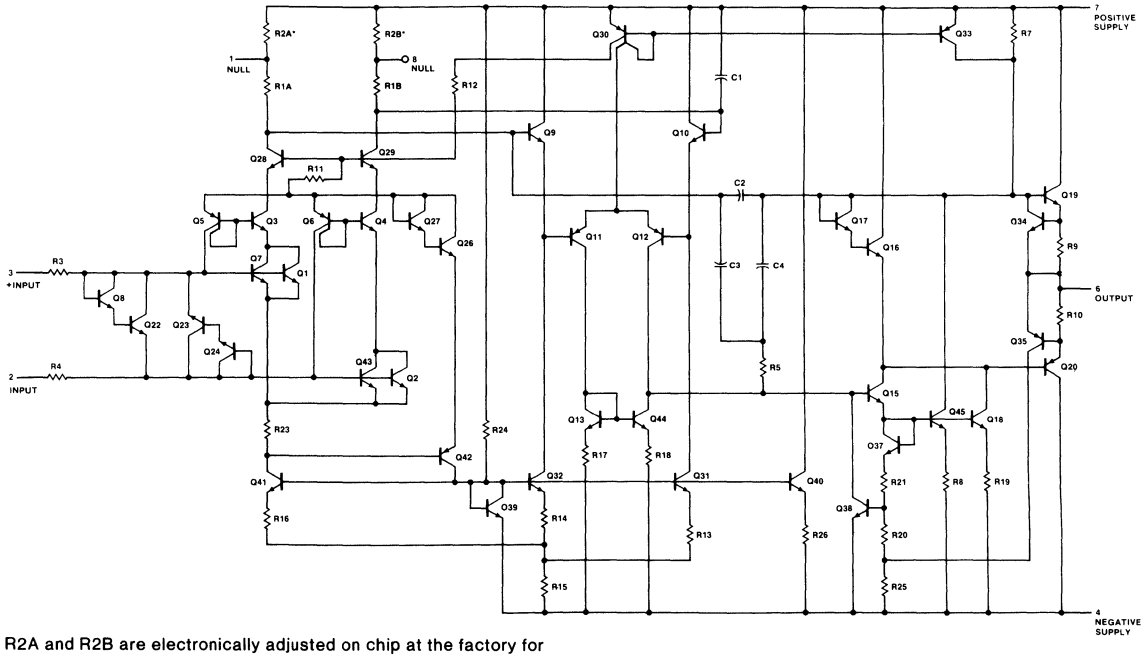
(Top View)

Order Information

Type	Package	Code	Part No.
714	Metal	5W	μA714HM
714E	Metal	5W	μA714EHC
714C	Metal	5W	μA714HC
714L	Metal	5W	μA714LHC

4

Equivalent Circuit



R2A and R2B are electronically adjusted on chip at the factory for minimum offset voltage

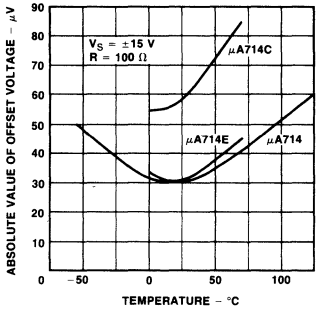
μA714
Electrical Characteristics

These specifications apply for $V_S = \pm 15$ V, $T_A = 25°C$.		714		
Characteristic	**Condition**	**Min**	**Typ**	**Max**
Input Offset Voltage	(Note 3), $R_S = 50\ \Omega$, $V_{CM} = 0.0$ V		30	75
Long Term Input Offset Voltage Stability	(Note 4), $R_S = 50\ \Omega$, $V_{CM} = 0.0$ V		0.2	1.0
Input Offset Current	$V_{CM} = 0.0$ V		0.4	2.8
Input Bias Current	$V_{CM} = 0.0$ V		± 1.0	± 3.0
Input Noise Voltage	0.1 Hz to 10 Hz (Note 5)		0.35	0.6
Input Noise Voltage Density	$f_O = 10$ Hz (Note 5) $f_O = 100$ Hz (Note 5) $f_O = 1000$ Hz (Note 5)		10.3 10.0 9.6	18.0 13.0 11.0
Input Noise Current	0.1 Hz to 10 Hz (Note 5)		14	30
Input Noise Current Density	$f_O = 10$ Hz (Note 5) $f_O = 100$ Hz (Note 5) $f_O = 1000$ Hz (Note 5)		0.32 0.14 0.12	0.80 0.23 0.17
Input Resistance—Differential Mode		20	60	
Input Resistance—Common Mode			200	
Input Voltage Range		± 13.0	± 14.0	
Common Mode Rejection Ratio	$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	110	126	
Power Supply Rejection Ratio	$V_S = \pm 3.0$ V to ± 18 V, $R_S = 50\ \Omega$	100	110	
Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, $V_O = -10$ V to $+10$ V	200	500	
	$R_L \geq 500\ \Omega$, $V_O = -0.5$ V to $+0.5$ V $V_S = \pm 3.0$ V	150	500	
Maximum Output Voltage Swing	$R_L \geq 10$ kΩ	± 12.5	± 13.0	
	$R_L \geq 2.0$ kΩ	± 12.0	± 12.8	
	$R_L \geq 1.0$ kΩ	± 10.5	± 12.0	
Slewing Rate	$R_L \geq 2.0$ kΩ		0.17	
Closed Loop Bandwidth	$A_{VCL} = +1.0$		0.6	
Open Loop Output Resistance	$V_O = 0$ V, $I_O = 0$ A		60	
Power Consumption	$V_O = 0$ V		75	120
	$V_S = \pm 3.0$ V, $V_O = 0$ V		4.0	6.0
Offset Adjustment Range	$R_P = 20$ kΩ		± 4.0	
The following specifications apply for $V_S = \pm 15$ V, $-55°C \leq T_A \leq +125°C$				
Input Offset Voltage	(Note 3), $R_S = \Omega$, $V_{CM} = 0.0$ V		60	200
Average Input Offset Voltage Drift Without External Trim	$R_S = 50\ \Omega$, $V_{CM} = 0.0$ V		0.3	1.3
With External Trim	(Note 5), $R_P = 20$ kΩ, $R_S = 50\ \Omega$		0.3	1.3
Input Offset Current	$V_{CM} = 0.0$ V		1.2	5.6
Average Input Offset Current Drift	$V_{CM} = 0.0$ V		8.0	50
Input Bias Current	$V_{CM} = 0.0$ V		± 2.0	± 6.0
Average Input Bias Current Drift	$V_{CM} = 0.0$ V		13	50
Input Voltage Range		± 13.0	± 13.5	
Common Mode Rejection Ratio	$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	106	123	
Power Supply Rejection Ratio	$V_S = \pm 3.0$ V to ± 18 V, $R_S = 50\ \Omega$	94	106	
Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, $V_O = -10$ V to $+10$ V	150	400	
Maximum Output Voltage Swing	$R_L \geq 2.0$ kΩ	± 12.0	± 12.6	

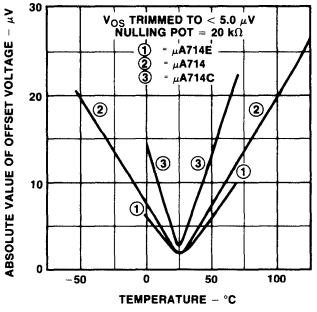
714E			714C			714L			
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
	30	75		60	150		100	250	μV
	0.3	1.5		0.4	2.0		0.5	3.0	μV/mo.
	0.5	3.8		0.8	6.0		5.0	20	nA
	±1.2	±4.0		±1.8	±7.0		6.0	±30	nA
	0.35	0.6		0.38	0.65				μVp-p
	10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5		10.5 10.2 9.8		nV/$\sqrt{Hz}$
	14	30		15	35		15		pA p-p
	0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18		0.35 0.15 0.13		pA/$\sqrt{Hz}$
15	50		8.0	33		8.0	33		MΩ
	160			120			120		GΩ
±13.0	±14.0		±13.0	±14.0		±13.0	±14.0		V
106	123		100	120		100	120		dB
94	107		90	104		90	104		dB
200	500		120	400		100	300		V/mV
150	500		100	400		50	150		
±12.5	±13.0		±12.0	±13.0		±12.0	±13.0		V
±12.0	±12.8		±11.5	±12.8		±11.0	±12.8		
±10.5	±12.0			±12.0			±12.0		
	0.17			0.17			0.17		V/μs
	0.6			0.6			0.6		MHz
	60			60			60		Ω
	75	120		80	150		100	180	mW
	4.0	6.0		4.0	8.0		5.0	12	
	±4.0			±4.0			±4.0		mV
The following specifications apply for V_S = ±15 V, 0°C ≤ T_A ≤ 70°C									
	45	130		85	250			400	μV
	0.3	1.3		0.5	1.8		1.0	3.0	μV/°C
	0.3	1.3		0.4	1.6				μV/°C
	0.9	5.3		1.6	8.0		8.0	40	nA
	8.0	35		12	50		20	100	pA/°C
	±1.5	±5.5		±2.2	±9.0		±15	±60	nA
	13	35		18	50		35	150	pA/°C
±13.0	±13.5		±13.0	±13.5		±13.0	±13.5		V
103	123		97	120		94	120		dB
90	104		86	100		83	100		dB
180	450		100	400		80	400		V/mV
±12.0	±12.6		±11.0	±12.6		±10.0	±12.6		V

Typical Performance Curves

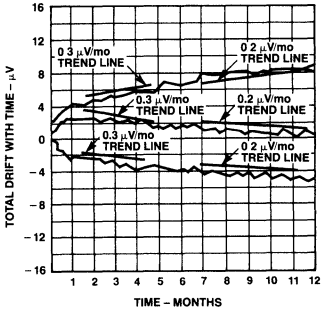
Untrimmed Offset Voltage Versus Temperature



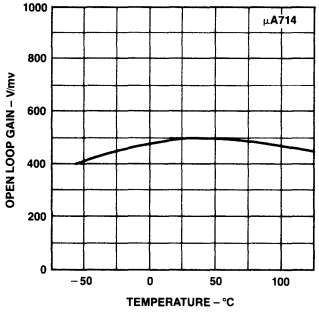
Trimmed Offset Voltage Versus Temperature



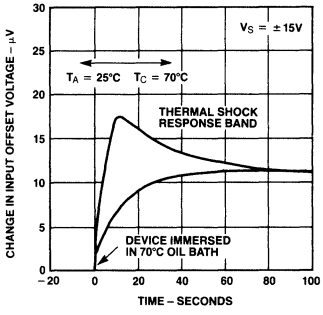
Offset Voltage Stability Versus Time



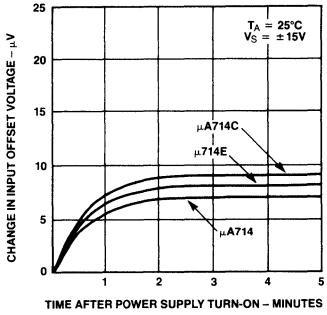
Open Loop Gain Versus Temperature



Offset Voltage Change Due to Thermal Shock



Warm-Up Drift

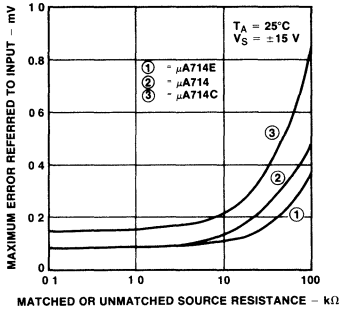


Notes

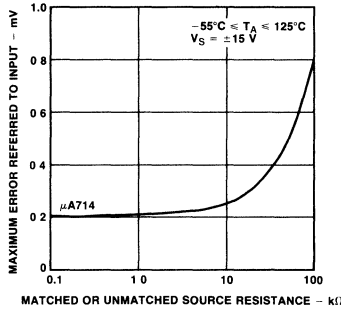
3. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. Long term input offset voltage stability refers to the averaged trend of V_{OS} versus time over extended periods after the first 30 days of operation. Parameter is not 100% tested. 90% of the units meet this specification.
5. Parameter is not 100% tested; 90% of the units meet this specification.

Typical Performance Curves (Cont.)

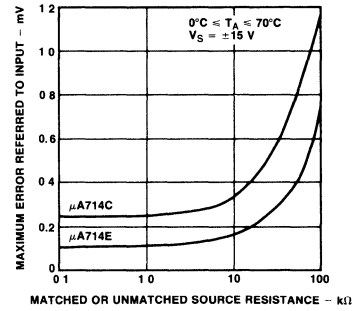
Maximum Error Versus Source Resistance



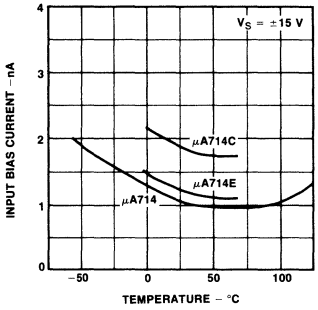
Maximum Error Versus Source Resistance



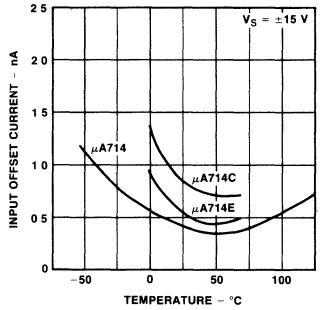
Maximum Error Versus Source Resistance



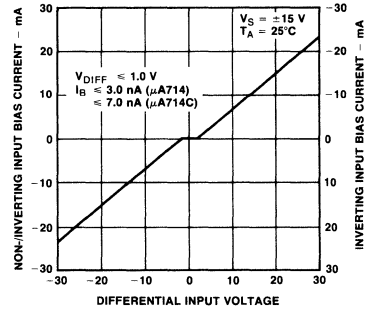
Input Bias Current Versus Temperature



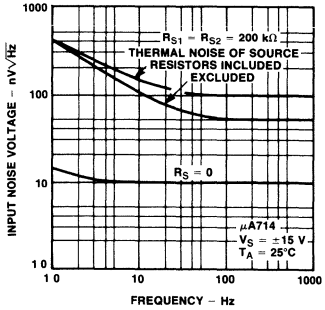
Input Offset Current Versus Temperature



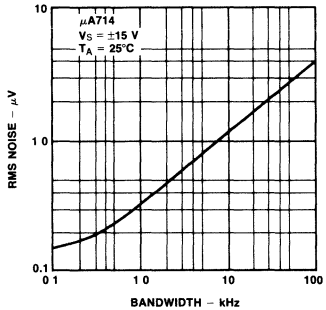
Input Bias Current Versus Differential Input Voltage



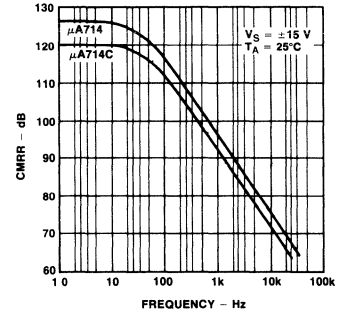
Input Spot Noise Voltage Versus Frequency



Input Wideband Noise Versus Bandwidth (0.1 Hz to Frequency Indicated)

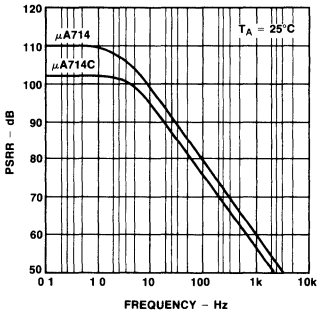


CMRR Versus Frequency

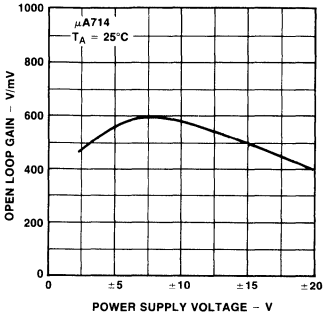


Typical Performance Curves (Cont.)

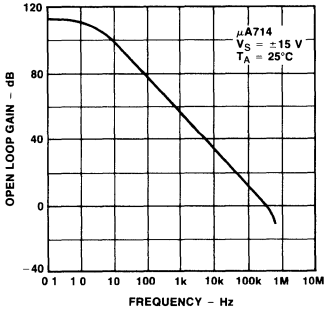
PSRR Versus Frequency



Open Loop Gain Versus Power Supply Voltage



Open Loop Frequency Response



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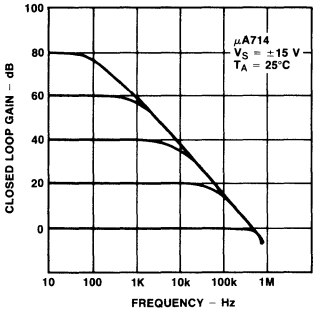
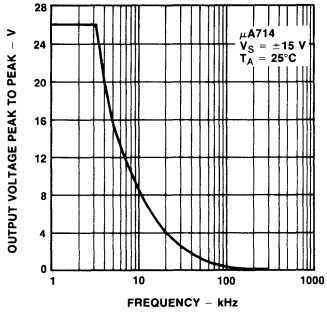
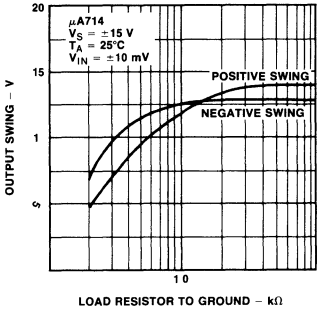
Closed Loop Response For Various Gain Configurations



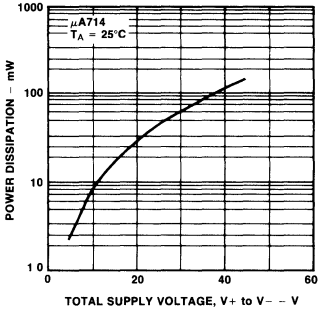
Maximum Undistorted Output Versus Frequency



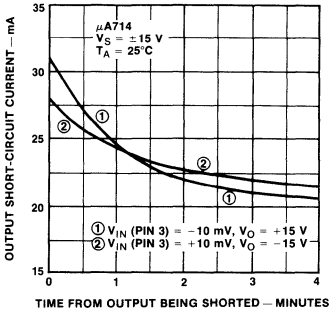
Output Voltage Versus Load Resistance



Power Consumption Versus Power Supply

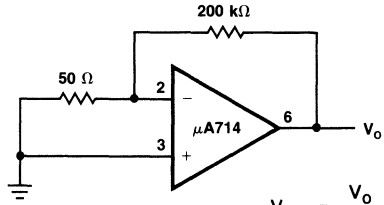


Output Short-Circuit Current Versus Time



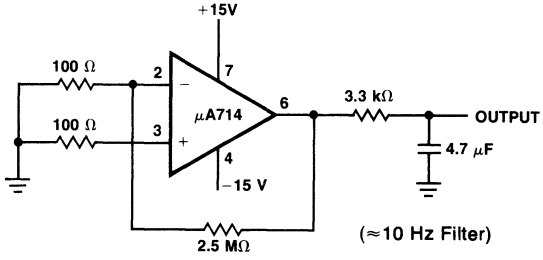
Test Circuits

Offset Voltage Test Circuit



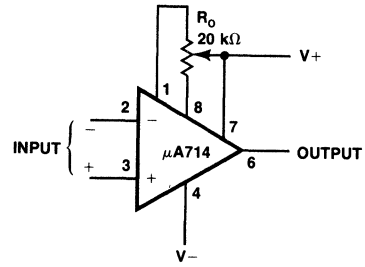
$$V_{OS} = \frac{V_o}{4000}$$

Low Frequency Noise Test Circuit



$$\text{Input Referred Noise} = \frac{V_o}{25{,}000} = \frac{5\ \text{mV/cm}}{25{,}000} = 200\ \text{nV/cm}$$

Optional Offset Nulling Circuit



FAIRCHILD
A Schlumberger Company

μA715 High-Speed Operational Amplifier

Linear Products

Description

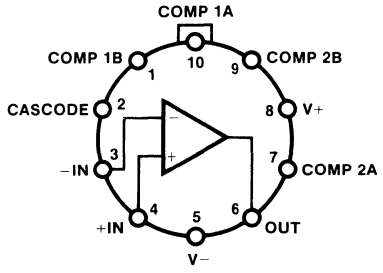
The μA715 is a High-Speed, High-Gain, Monolithic Operational Amplifier constructed using the Fairchild Planar epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The μA715 features fast settling time, high slew rate, low offsets and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The μA715 is ideally suited for use in A/D and D/A converters, active filters, deflection amplifiers, video amplifiers, phase-locked loops, multiplexed analog gates, precision comparators, sample and holds and general feedback applications requiring dc wide bandwidth operation.

- **HIGH SLEW RATE—100 V/μs**
- **FAST SETTLING TIME—800 ns**
- **WIDE BANDWIDTH—65 MHz**
- **WIDE OPERATING SUPPLY RANGE**
- **WIDE INPUT VOLTAGE RANGES**

Absolute Maximum Ratings

Supply Voltage	± 18 V
Internal Power Dissipation (Note 1)	
Metal	500 mW
DIP	670 mW
Differential Input Voltage	± 15 V
Input Voltage (Note 2)	± 15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA715)	−55°C to +125°C
Commercial (μA715C)	0°C to +70°C
Pin Temperature (Soldering, 60 s)	300°C

Connection Diagram 10-Pin Metal Package

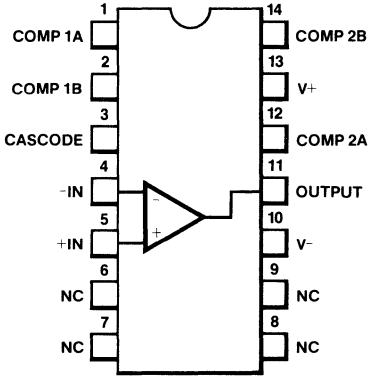


(Top View)

Order Information

Type	Package	Code	Part No.
μA715	Metal	5X	μA715HM
μA715C	Metal	5X	μA715HC

Connection Diagram 14-Pin DIP



(Top View)

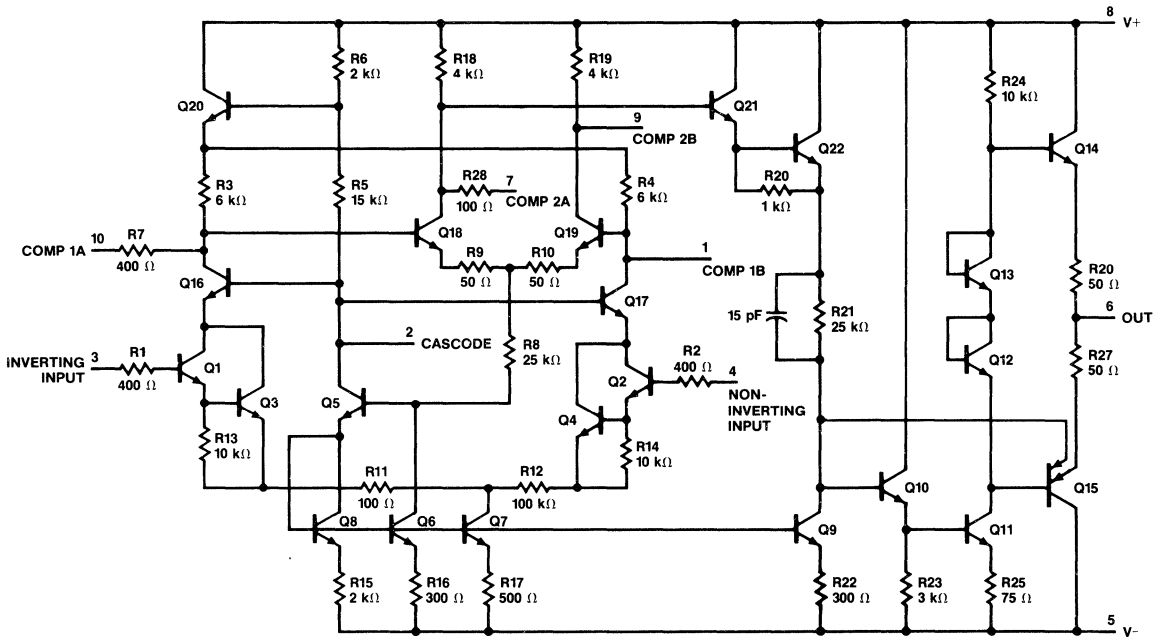
Order Information

Type	Package	Code	Part No.
μA715	Ceramic DIP	6A	μA715DM
μA715C	Ceramic DIP	6A	μA715DC

Notes

1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal package and 8.3 mW/°C for the DIP.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Equivalent Circuit



All pin numbers shown refer to 10-pin metal package

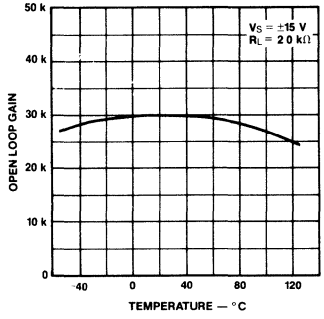
μA715 and μA715C
Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

Characteristic		Condition	μA715 Min	μA715 Typ	μA715 Max	μA715C Min	μA715C Typ	μA715C Max	Unit
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	5.0		2.0	7.5	mV
Input Offset Current				70	250		70	250	nA
Input Bias Current				400	750		0.4	1.5	μA
Input Resistance				1.0			1.0		MΩ
Input Voltage Range			±10	±12		±10	±12		V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	15,000	30,000		10,000	30,000		
Output Resistance				75			75		Ω
Supply Current				5.5	7.0		5.5	10	mA
Power Consumption				165	210		165	300	mW
Settling Time (Unity Gain)		$V_{OUT} = \pm 5$ V		800			800		ns
Transient Response (Unity Gain)	Rise Time	V_{IN} = 400 mV		30	60		30	75	ns
	Overshoot			25	40		25	50	%
Slew Rate		Av = 100		70			70		V/μs
		Av = 10		38			38		V/μs
		Av = 1 (non-inverting)	15	18		10	18		V/μs
		Av = 1 (inverting)		100			100		V/μs
The following apply for TA High to Low (Note 4)									
Input Offset Voltage		$R_S \leq 10$ kΩ			7.5			10	mV
Input Offset Current		T_A = High			250			250	nA
		T_A = Low			800			750	nA
Input Bias Current		T_A = High			750			1500	nA
		T_A = Low			4.0			7.5	μA
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	74	92		74(3)	92(3)		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		45	300		45(3)	400(1)	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	10,000			8,000			
Output Voltage Swing		$R_L \geq 2$ kΩ	±10	±13		±10	±13		V

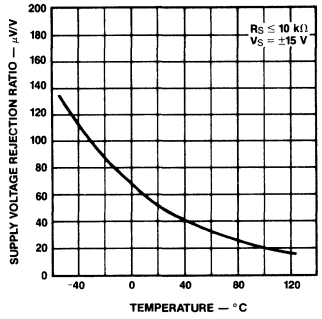
Note
3. Specification applies to TA = 25°C only.
4. For μA715 $-55°C \leq T_A \leq 125°C$
   For μA715C $0°C \leq T_A \leq 70°C$

Typical Performance Curves for μA715

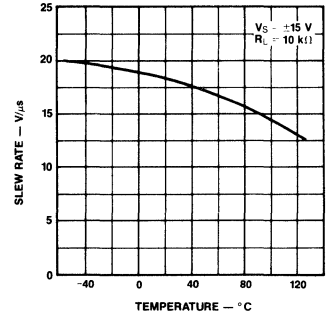
Open Loop Gain as a Function of Ambient Temperature



Supply Voltage Rejection Ratio as a Function of Ambient Temperature

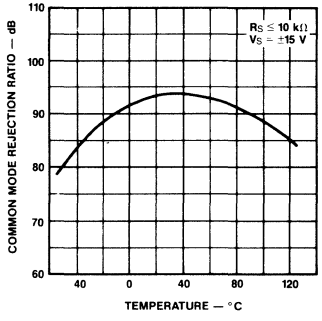


Slew Rate as a Function of Temperature

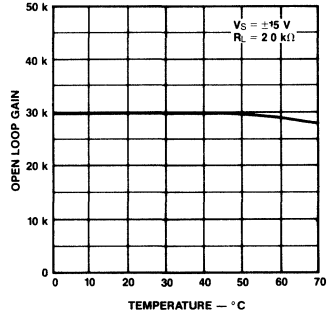


Typical Performance Curves for μA715C

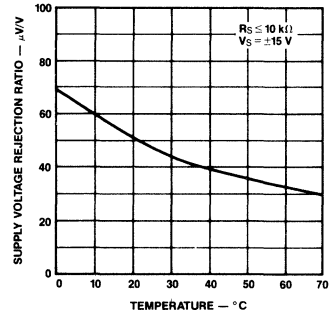
Common Mode Rejection Ratio as a Function of Ambient Temperature



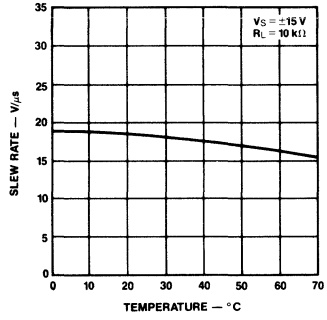
Open Loop Gain as a Function of Ambient Temperature



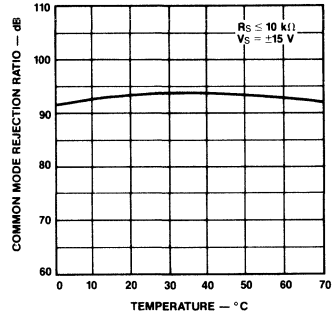
Supply Voltage Rejection Ratio as a Function of Ambient Temperature



Slew Rate as a Function of Temperature

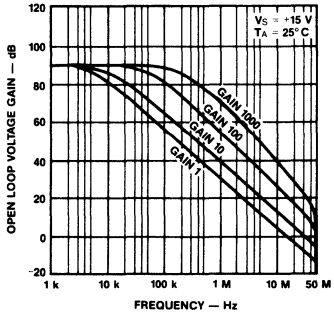


Common Mode Rejection Ratio as a Function of Ambient Temperature

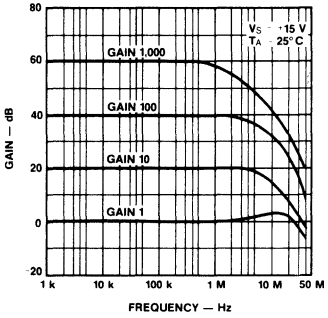


Typical Performance Curves for μA715 and μA715C

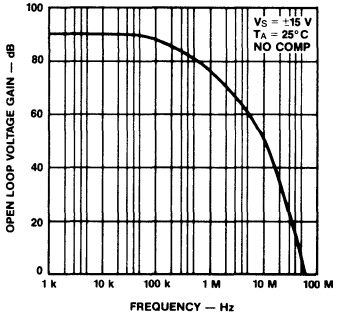
Open Loop Gain as a Function of Frequency



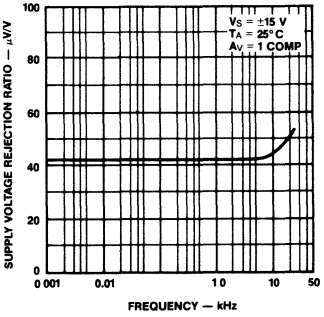
Closed Loop Frequency Response for Various Gain Configurations



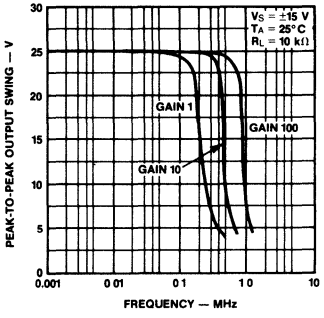
Open Loop Response With Compensation Necessary for Various Closed Loop Gain Configurations



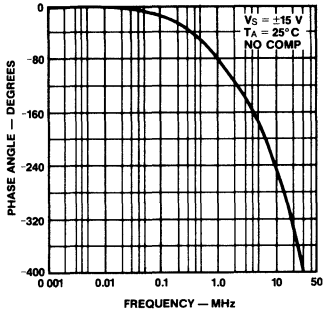
Supply Voltage Rejection Ratio as a Function of Frequency



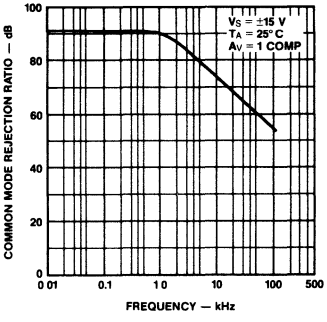
Output Swing as a Function of Frequency for Various Closed Loop Gain Configurations



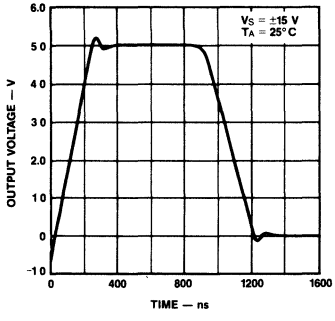
Open Loop Phase as a Function of Frequency



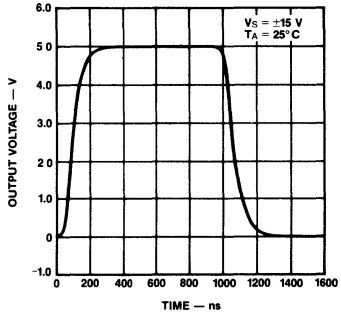
Common Mode Rejection Ratio as a Function of Frequency



Unity Gain Large Signal Pulse Response



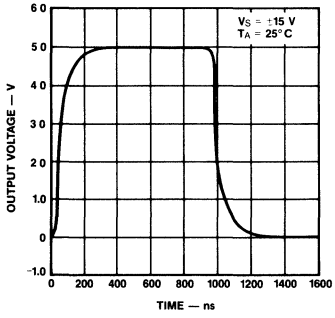
Large Signal Pulse Response for Gain 10



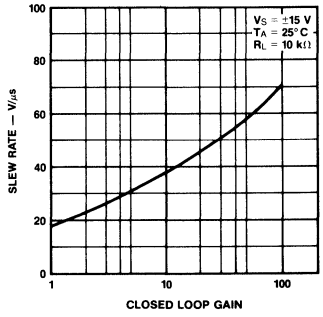
4

Typical Performance Curves for μA715 and μA715C (Cont.)

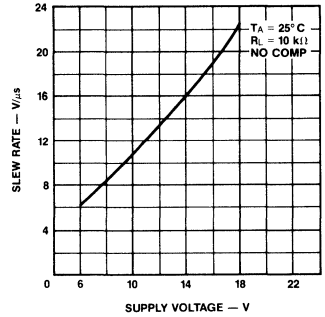
Large Signal Pulse Response for Gain 100



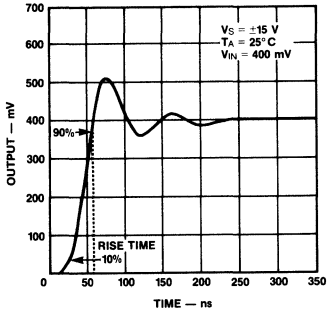
Slew Rate as a Function of the Closed Loop Gain



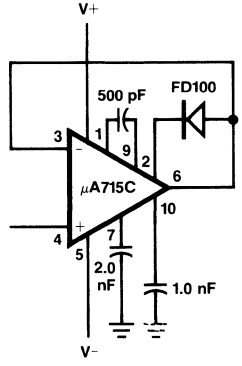
Slew Rate as a Function of Supply Voltage



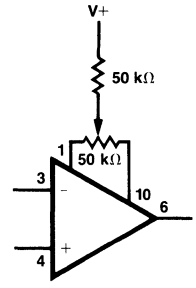
Voltage Follower Transient Response



Voltage Follower

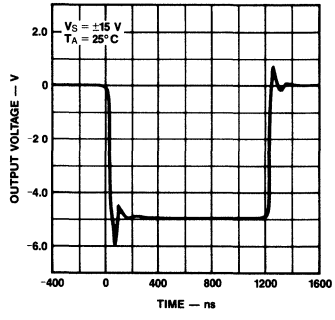


Voltage Offset Null Circuit

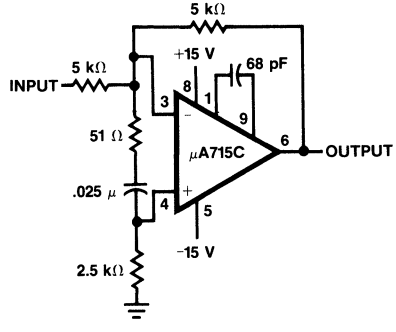


Note
Pin numbers apply to metal package.

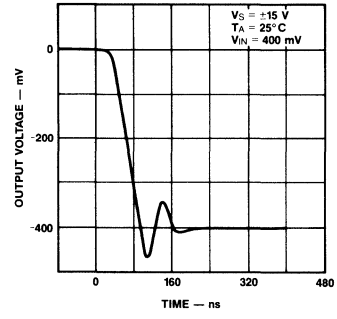
Inverting Unity Gain Large Signal Pulse Response



High Slew Rate Circuit



Small Signal Pulse Response Inverting Unity Gain

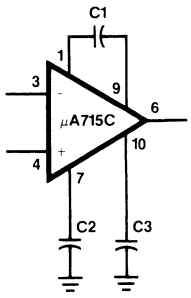


Non-Inverting Compensation Components Values

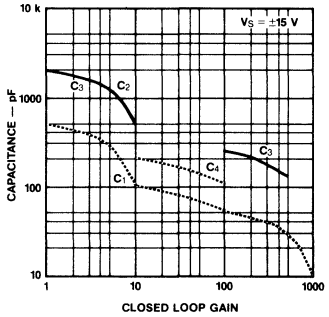
Closed Loop Gain	C1	C2	C3
1000	10 pF		
100	50pF		250 pF
10 (Note)	100 pF	500pF	1000 pF
1	500 pF	2000pF	1000 pF

Note
For gain 10, compensation may be simplified by removing C2, C3 and adding a 200 pF capacitor (C4) between Pin 7 and 10

Frequency Compensation Circuit



Suggested Values of Compensation Capacitors as a Function of the Closed Loop Gain

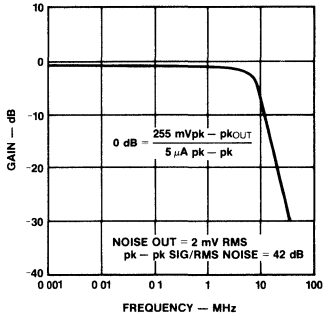


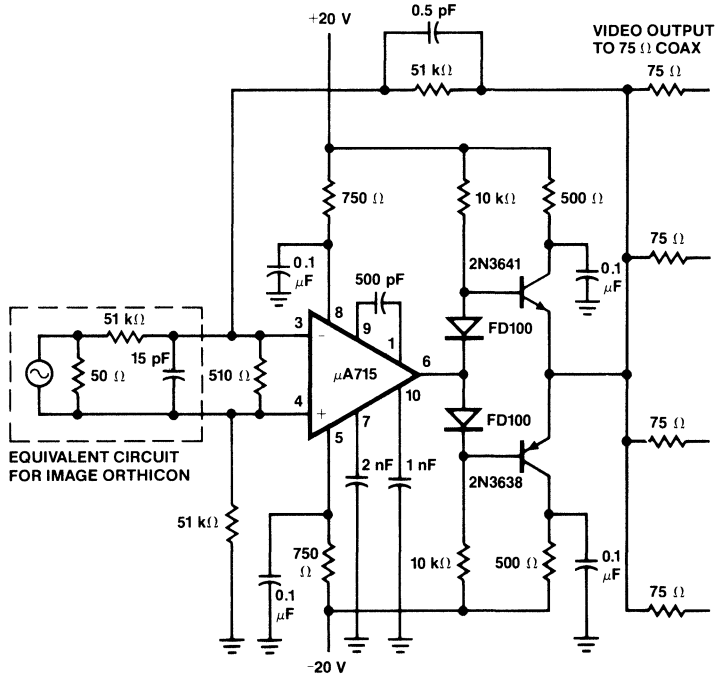
Layout Instructions

Layout—The layout should be such that stray capacitance is minimal.
Supplies—The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.
Ringing—Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100 Ω. Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3.0 pF for gain 10 should be adequate.
Latch-Up—This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between pins 6 and 2 with the cathode toward pin 2 is the recommended preventive measure.

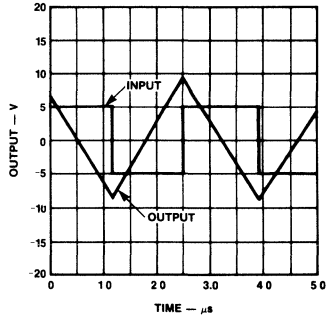
Typical Applications

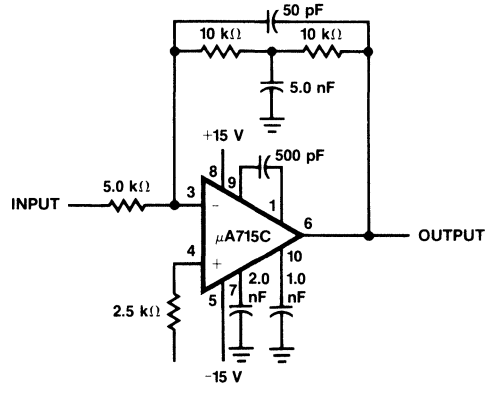
Wide Band Video Amplifier With 75 Ω Coax Cable Drive Capability





High Speed Integrator





FAIRCHILD

A Schlumberger Company

μA725 Instrumentation Operation Amplifier

Linear Products

Description

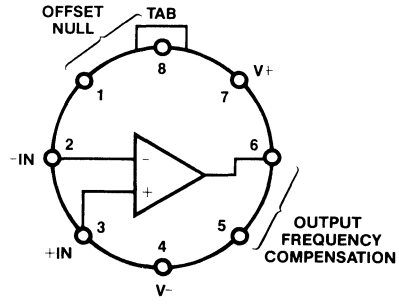
The μA725 is a Monolithic Instrumentation Operational Amplifier constructed using the Fairchild Planar epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed-loop gain are required. The offset-null capability, low-power consumption, very high-voltage gain as well as wide power-supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725 is pin compatible with the popular μA741 operational amplifier.

- **LOW INPUT NOISE CURRENT 0.15 pA/$\sqrt{Hz}$**
- **HIGH OPEN-LOOP GAIN 3,000,000**
- **LOW INPUT OFFSET CURRENT 2 nA**
- **LOW INPUT VOLTAGE DRIFT 0.6 μV/°C**
- **HIGH COMMON MODE REJECTION 120 dB**
- **HIGH INPUT VOLTAGE RANGE ±14 V**
- **WIDE POWER SUPPLY RANGE ±3 V TO ±22 V**
- **OFFSET NULL CAPABILITY**

Absolute Maximum Ratings

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
DIP	310 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±22 V
Votage Between Offset Null and V+	±0.5 V
Storage Temperature Range	
Metal Package	−65°C to +150°C
DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA725A, μA725)	−55°C to +125°C
Commercial (μA725E, μA725C)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Package (60 s)	300°C
DIP (10 s)	260°C

Connection Diagram 8-Pin Metal Package

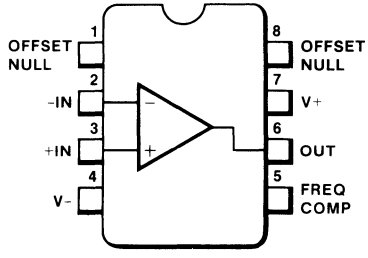


(Top View)

Order Information

Type	Package	Code	Part No.
μA725	Metal	5W	μA725HM
μA725A	Metal	5W	μA725AHM
μA725C	Metal	5W	μA725HC
μA725E	Metal	5W	μA725EHC

Connection Diagram 8-Pin DIP



(Top View)

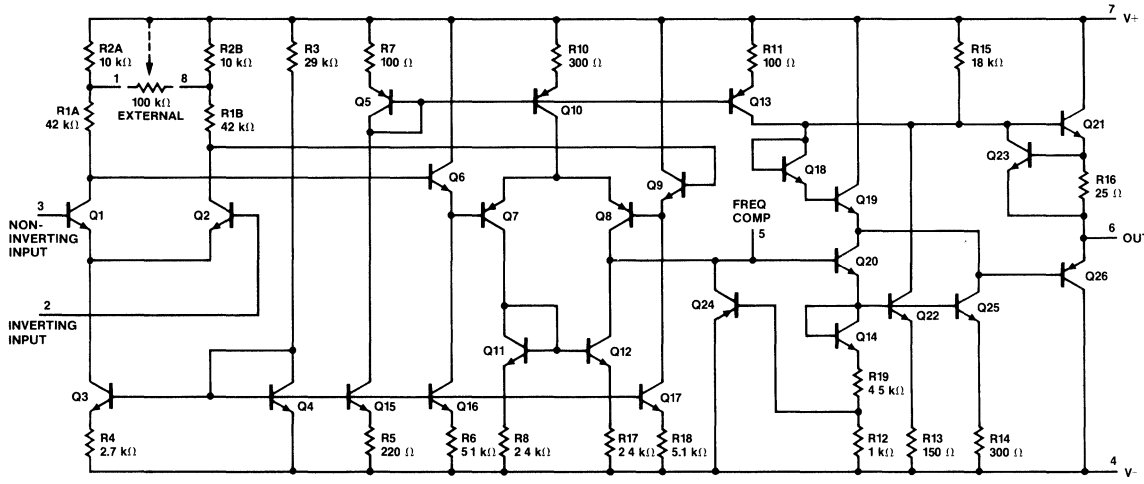
Order Information

Type	Package	Code	Part No.
μA725C	Molded DIP	9T	μA725TC

Notes

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6 3 mW/°C.
2. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Equivalent Circuit



Pin numbers for metal package only.

μA725A/E and μA725
Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified

Characteristic	Condition	μA725A/E			μA725			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			0.5		0.5	1.0	mV
Input Offset Current				5.0		2.0	20	nA
Input Bias Current				75		42	100	nA
Input Noise Voltage	$f_o = 10$ Hz			15		15		nV/$\sqrt{\text{Hz}}$
	$f_o = 100$ Hz			12		9.0		nV/$\sqrt{\text{Hz}}$
	$f_o = 1$ kHz			12		8.0		nV/$\sqrt{\text{Hz}}$
Input Noise Current	$f_o = 10$ Hz			1.2		1.0		pA/$\sqrt{\text{Hz}}$
	$f_o = 100$ Hz			0.6		0.3		pA/$\sqrt{\text{Hz}}$
	$f_o = 1$ kHz			0.25		0.15		pA/$\sqrt{\text{Hz}}$
Input Resistance			1.5			1.5		MΩ
Input Voltage Range		± 13.5	± 14		± 13.5	± 14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	1,000 k	3,000 k		1,000 k	3,000 k		V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	120	130		110	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	5.0		2.0	10	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	± 12.5			± 12	± 13.5		V
	$R_L \geq 2$ kΩ	± 10			± 10	± 13.5		V
Output Resistance			150			150		Ω
Power Consumption			80	120 (3)		80	105	mW
	$V_S \pm 3$ V			6				
The following specifications apply for $T_A = T_{HIGH}$ and T_{LOW}								
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			0.75			1.5	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50$ Ω			2.0		2.0	5.0	μV/°C
Average Input Offset Voltage Drift (With external trim)	$R_S = 50$ Ω		0.6	1.0		0.6		μV/°C
Input Offset Current	T_A = High			4.0		1.2	20	nA
	T_A = Low		5.0	18		7.5	40	nA
Average Input Offset Current Drift				90		35	150	pA/°C
Input Bias Current	T_A = High			70		20	100	nA
	T_A = Low			180		80	200	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, T_A = High	1,000 k			1,000 k			V/V
	$R_L \geq 2$ kΩ, T_A = Low	500 k			250 k			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	110			100			dB
Power Suppy Rejection Ratio	$R_S \leq 10$ kΩ			8.0			20	μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	± 10			± 10			V

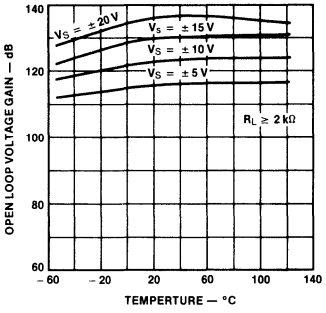
Note
3. For 725E limit is 150 mW.

μA725C
Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified

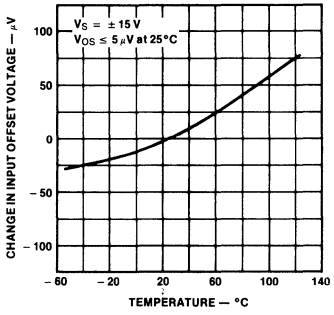
Characteristic	Condition	μA725C Min	μA725C Typ	μA725C Max	Unit
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	2.5	mV
Input Offset Current			2.0	35	nA
Input Bias Current			42	125	nA
Input Noise Voltage	$f_o = 10$ Hz		15		nV/$\sqrt{Hz}$
	$f_o = 100$ Hz		9.0		nV/$\sqrt{Hz}$
	$f_o = 1$ kHz		8.0		nV/$\sqrt{Hz}$
Input Noise Current	$f_o = 10$ Hz		1.0		pA/$\sqrt{Hz}$
	$f_o = 100$ Hz		.3		pA/$\sqrt{Hz}$
	$f_o = 1$ kHz		.15		pA/$\sqrt{Hz}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	250 k	3,000 k		V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	94	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	35	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±13.5		V
	$R_L \geq 2$ kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	150	mW
The following specifications apply for T_A = High and Low					
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			3.5	mV
Average Input Offset Voltage Drift (Without external trim)	$R_S = 50$ Ω		2.0		μV/°C
Average Input Offset Voltage Drift (With external trim)	$R_S = 50$ Ω		0.6		μV/°C
Input Offset Current	T_A = High		1.2	35	nA
	T_A = Low		4.0	50	nA
Average Input Offset Current Drift			10		pA/°C
Input Bias Current	T_A = High			125	nA
	T_A = Low			250	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, T_A = High	125 k			V/V
	$R_L \geq 2$ kΩ, T_A = Low	125 k			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ		115		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		20		μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

Typical Performance Curves for μA725A and μA725

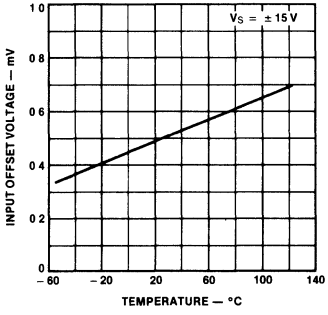
Open Loop Voltage Gain as a Function of Temperature for Various Supply Voltages



Nulled Input Offset Voltage as a Function of Temperature

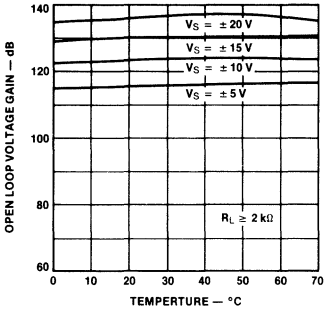


Unnulled Input Offset Voltage as a Function of Temperature

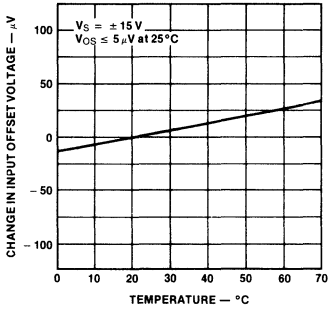


Typical Performance Curves for μA725E and μA725C

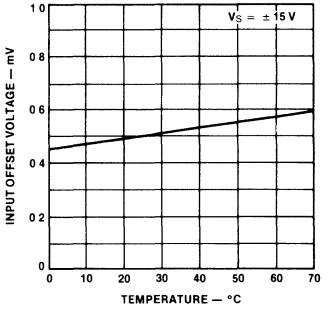
Open Loop Voltage Gain as a Function of Temperature for Various Supply Voltages



Nulled Input Offset Voltage as a Function of Temperature

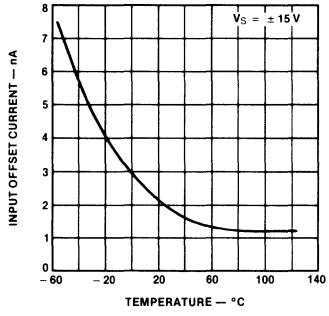


Unnulled Input Offset Voltage as a Function of Temperature

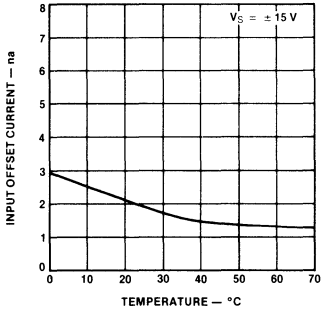


Typical Performance Curves for all Types (Unless Otherwise Specified)

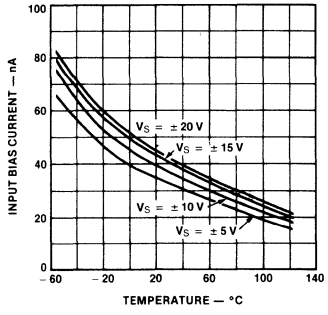
Input Offset Current as a Function of Temperature μA725A and μA725



Input Offset Current as a Function of Temperature μA725C and μA725E



Input Bias Current as a Function of Temperature μA725A and μA725



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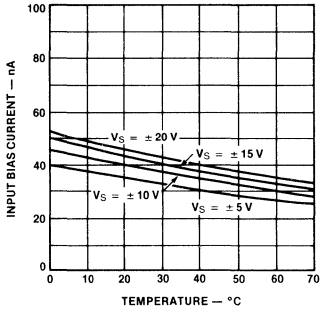
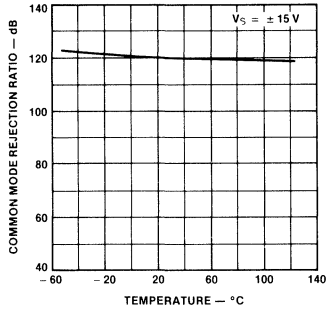
Typical Performance Curves for all Types (Cont.)

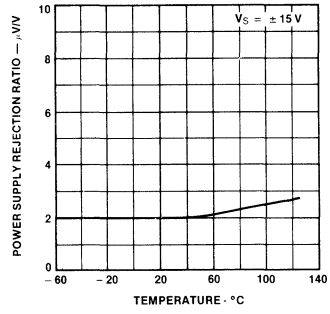
Input Bias Current as a Function of Temperature μA725C and μA725E



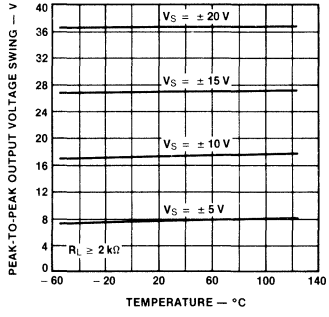
Common Mode Rejection Ratio as a Function of Temperature



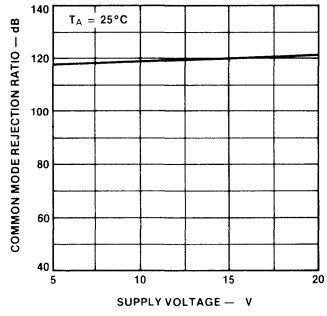
Supply Voltage Rejection Ratio as a Function of Temperature



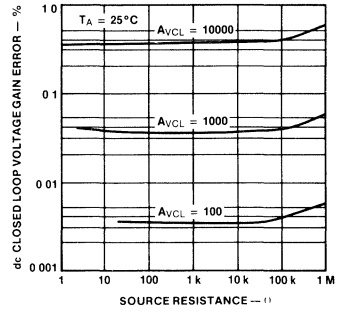
Output Voltage Swing as a Function of Temperature



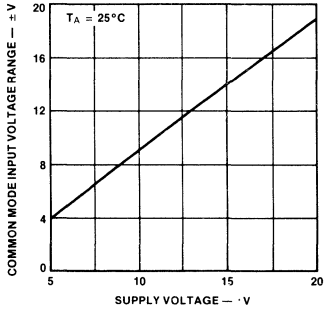
Common Mode Rejection Ratio as a Function of Supply Voltage



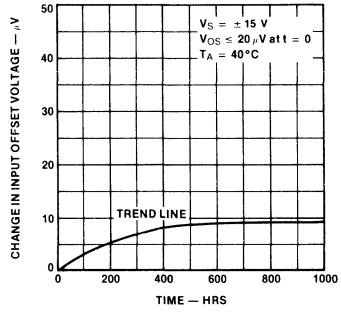
DC Closed Loop Voltage Gain Error as a Function of Source Resistance



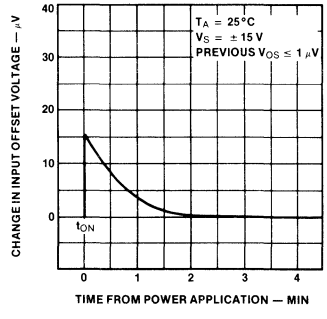
Common Mode Input Voltage Range as a Function of Supply Voltage



Input Offset Voltage Drift as a Function of Time

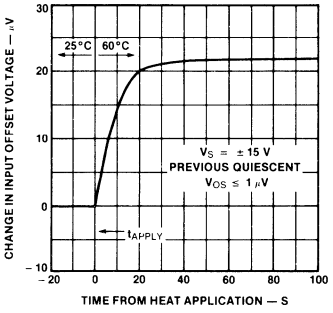


Stabilization Time of Input Offset Voltage From Power Turn On

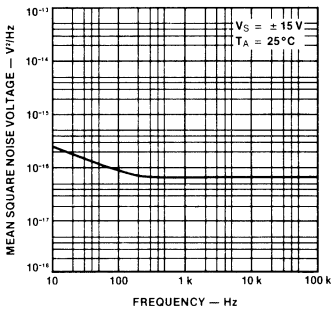


Typical Performance Curves for all Types (Cont.)

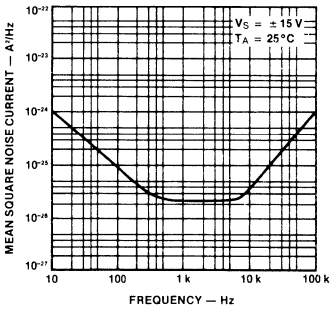
Change In Input Offset Voltage Due to Thermal Shock as a Function of Time



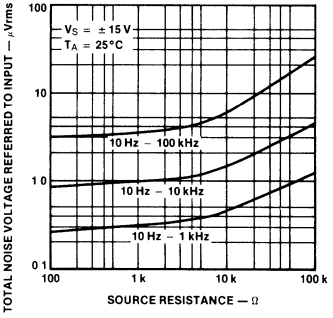
Input Noise Voltage as a Function of Frequency



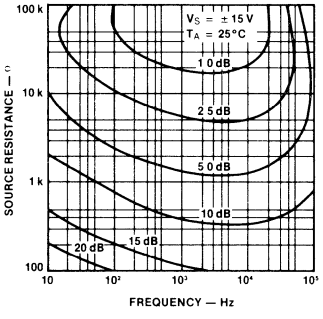
Input Noise Current as a Function of Frequency



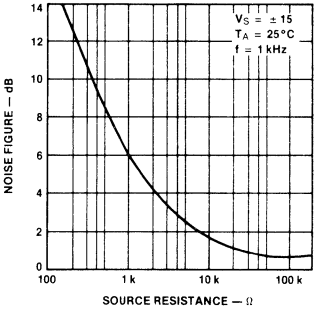
Broad Band Noise for Various Bandwidths



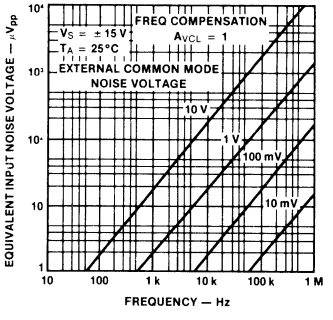
Narrow Band Spot Noise Figure Contours



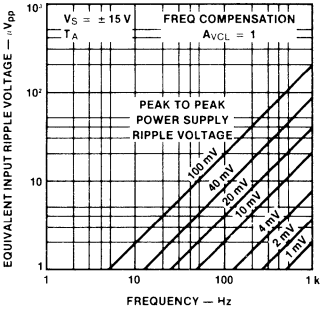
Noise Figure as a Function of Source Resistance



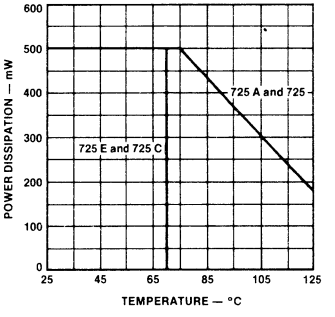
Equivalent Input Noise Voltage Due to External Common Mode Noise as a Function of Frequency



Equivalent Input Ripple Voltage Due to Power Supply Ripple as a Function of Frequency



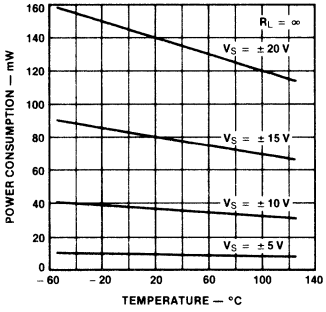
Absolute Maximum Power Dissipation as a Function of Ambient Temperature



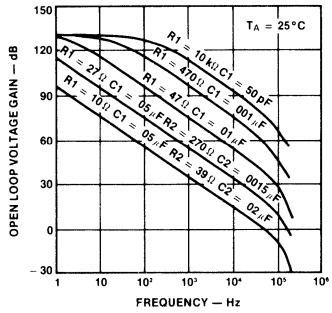
4

Typical Performance Curves for all Types (Cont.)

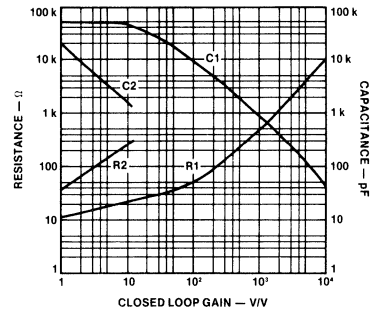
Power Consumption as a Function of Temperature



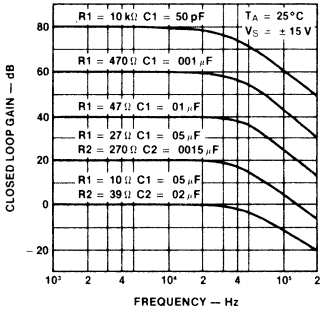
Open Loop Voltage Gain as a Function of Frequency Using Recommended Compensation Networks



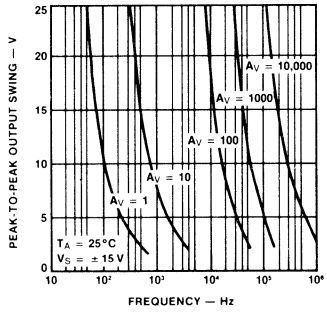
Values for Suggested Compensation Networks for Various Closed Loop Voltage Gains



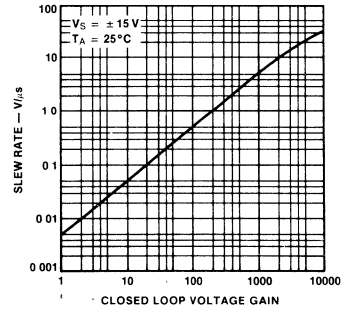
Frequency Response for Various Closed Loop Gains Using Recommended Compensation Networks



Output Voltage Swing as a Function of Frequency for Recommended Compensation Networks



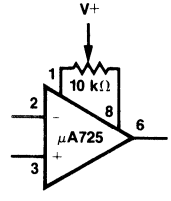
Slew Rate as a Function of Closed Loop Gain Using Recommended Compensation Networks



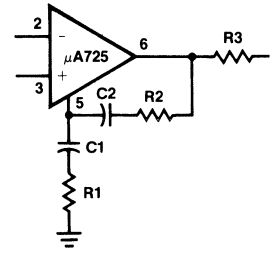
Compensation Component Values

A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	—	—
1,000	470	.001	—	—
100	47	.01	—	—
10	27	.05	270	.0015
1	10	.05	39	.02

Voltage Offset Null Circuit

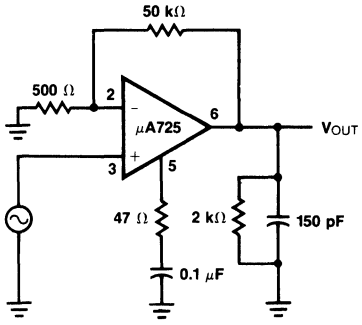


Frequency Compensation Circuit



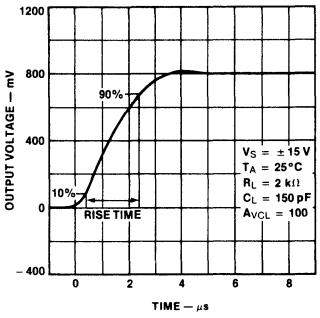
Use $R_3 = 51\,\Omega$ when the amplifier is operated with capacitive load.

Transient Response Test Circuit



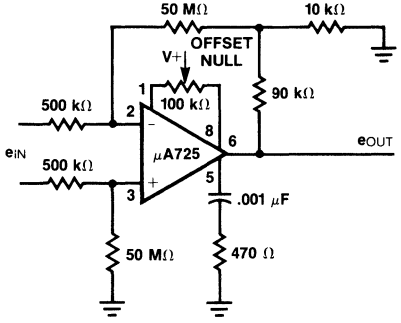
Pin numbers are shown for metal package only.

Transient Response



Typical Applications

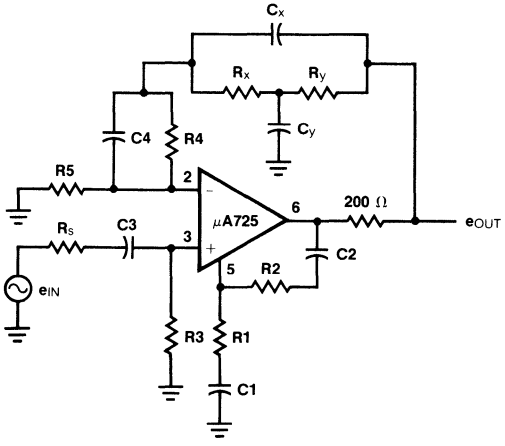
Precision Amplifier A_{VCL} = 1000



Pin numbers are shown for metal package only.

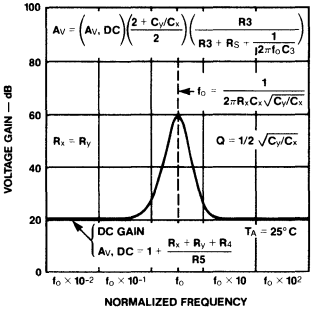
Characteristics
A_V = 1000 = 60 dB
DC Gain Error = 0.05%
Bandwidth = 1 kHz for −0.05% error
Diff. Input Res. = 1 MΩ
Typical amplifying capability
e_{IN} = 10 μV on V_{CMI} = 1.0 V
Caution: Minimize Stray Capacitance

Active Filter—Band Pass With 60 dB Gain

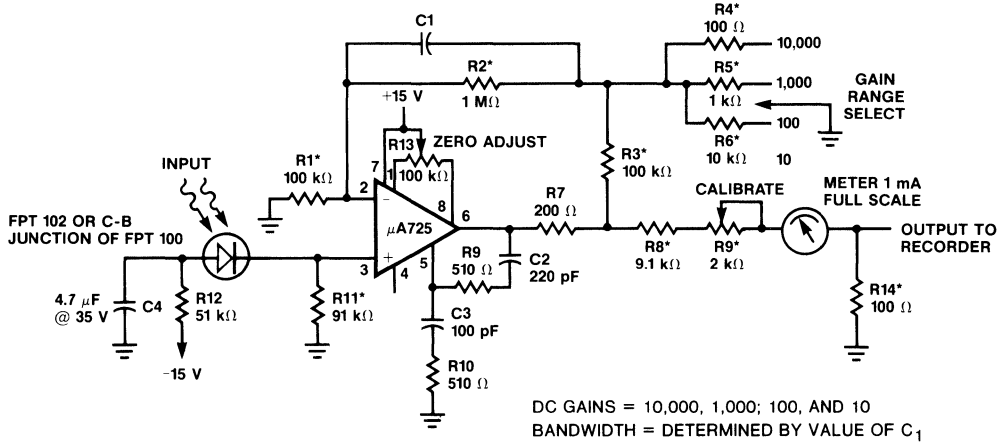


Pin numbers are shown for metal package only.

Active Filter Frequency Response



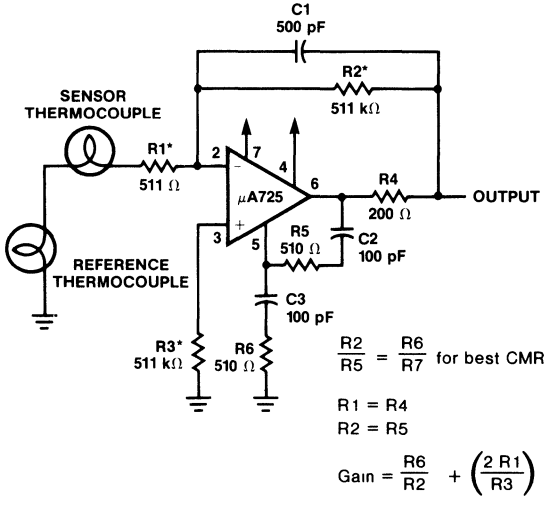
Photodiode Amplifier



Notes

*Indicates ± 1% metal film resistors recommended for temperature stability.
Pin numbers are shown for metal package only.

Thermocouple Amplifier

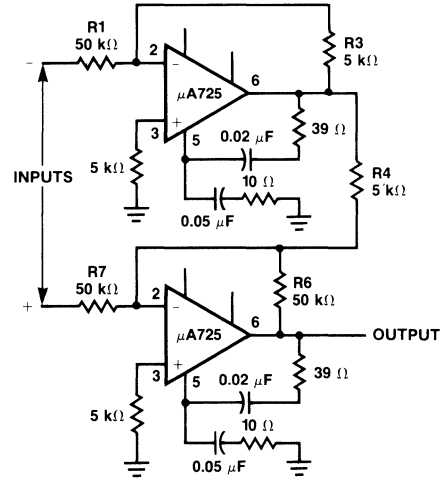


DC GAINS = 1000
BANDWIDTH = DC TO 540 Hz
EQUIVALENT INPUT NOISE = 0.24 μVrms

Notes

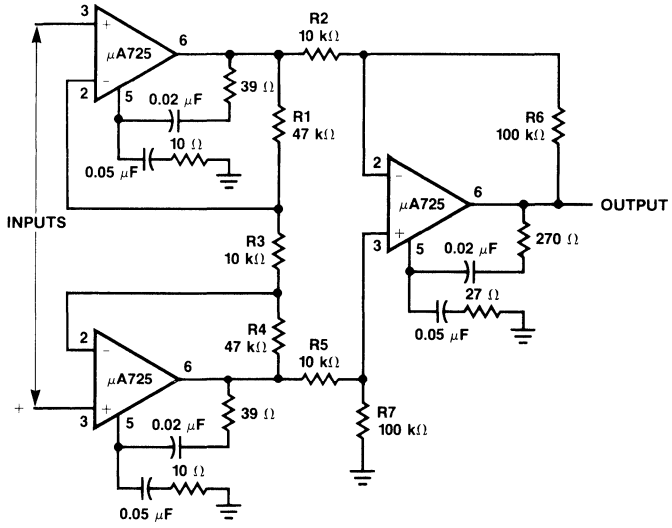
*Indicates ± 1% metal film resistors recommended for temperature stability.
Pin numbers are shown for metal package only.

± 100 V Common Mode Range Differential Amplifier



Pin numbers are shown for metal package only.

Instrumentation Amplifier With High Common Mode Rejection



$\frac{R1}{R6} = \frac{R3}{R4}$ for best CMRR

R3 = R4

R1 = R6 = 10 R3

Gain = $\frac{R6}{R7}$

Pin numbers are shown for metal package only.

FAIRCHILD

A Schlumberger Company

μA739 • μA749 Dual Audio Operational Amplifier/Preamplifier

Linear Products

Description

The μA739 and μA749 consist of two identical High-Gain Operational Amplifiers constructed on a single silcon chip using the Fairchild Planar epitaxial process. These 3-stage amplifiers use Class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from dc to 10 MHz, where two high performance operational amplifiers are required. In addition, the outputs may be wired-OR for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers, peak detectors, etc.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW POWER CONSUMPTION**
- **HIGH GAIN, 25,000 V/V**
- **LARGE COMMON MODE RANGE, +11 V, −13 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

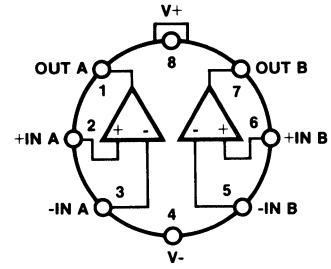
Absolute Maximum Ratings

Supply Voltage	
(μA749, μA749C, μA739)	± 18 V
(μ749D)	± 12 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
DIP	650 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	
(μA749, μA749C, μA739)	± 15 V
(μA749D)	± 12 V
Storage Temperature Range	
Metal Package and Ceramic DIP	−65°C to +150°C
Molded DIP	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Pin Temperature	
Metal Package, Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Output Short Circuit Duration, T_A = 25°C (Note 3)	30 seconds

Notes

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C for the Ceramic DIP.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply

Connection Diagram 8-Pin Metal Package



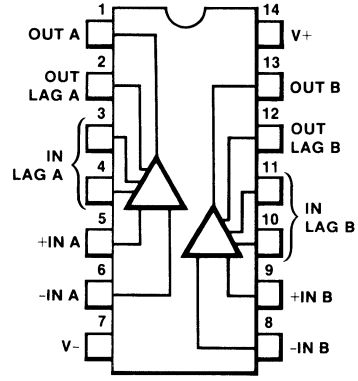
(Top View)

Pin 4 is connected to case.

Order Information

Type	Package	Code	Part No.
μA749D	Metal	5W	μA749DHC

Connection Diagram 14-Pin DIP

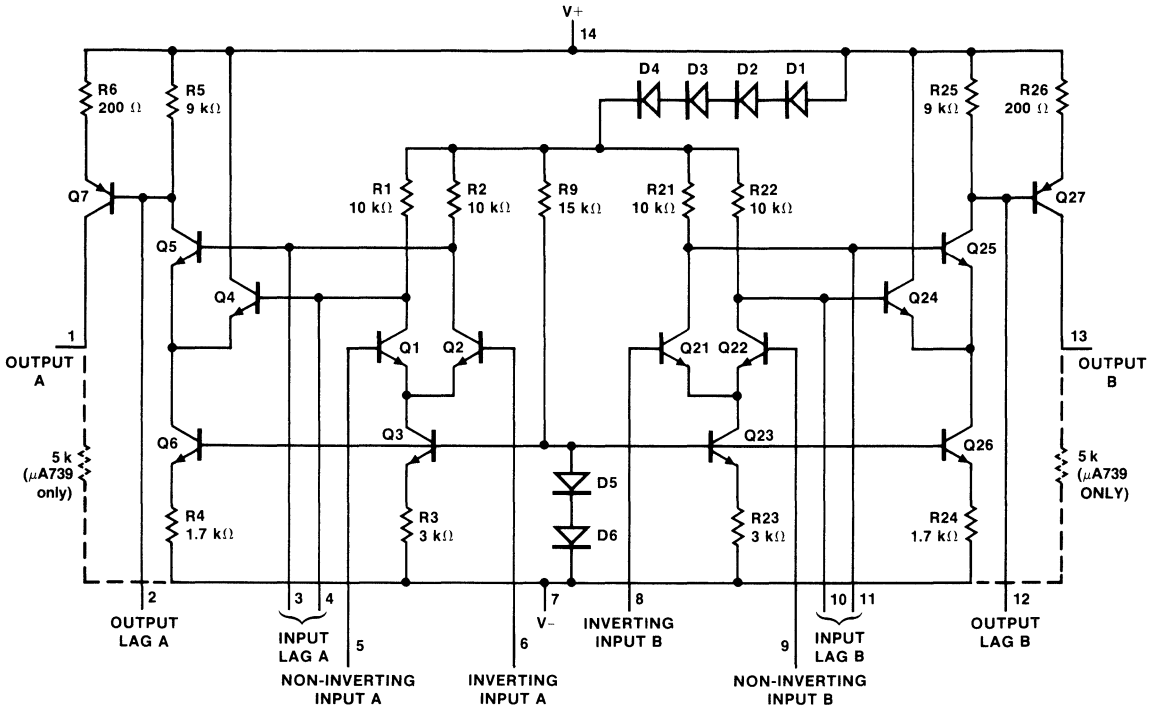


(Top View)

Order Information

Type	Package	Code	Part No.
μA739C	Ceramic DIP	6A	μA739DC
μA739C	Molded DIP	9A	μA739PC
μA749C	Ceramic DIP	6A	μA749DC
μA749C	Molded DIP	9A	μA749PC

Equivalent Circuit



Pin numbers for DIP only.

μA749C, μA749D and μA739E
Electrical Characteristics V+ = ±15 V, R_L = 5 kΩ to Pin 7, T_A = 25°C unless otherwise specified

Characteristic	Condition
Input Offset Voltage	R_S = 200 Ω
Input Offset Current	
Input Bias Current	
Input Resistance	
Large Signal Voltage Gain	V_{OUT} = ±10 V
Positive Output Voltage Swing	
Negative Output Voltage Swing	
Output Resistance	f = 1.0 kHz
Common Mode Rejection Ratio	R_S = 200 Ω, V_{IN} = +11.5 V to −13.5 V
Supply Voltage Rejection Ratio	R_S = 200 Ω
Input Voltage Range	
Internal Power Dissipation	V_{OUT} = 0
Supply Current	V_{OUT} = 0
Broadband Noise Figure	R_S = 10 kΩ, BW = 10 Hz to 10 kHz
Turn On Delay (See *Figure 3*)	Open Loop, V_{IN} = ±20 mV
Turn Off Delay (See *Figure 3*)	Open Loop, V_{IN} = ±20 mV
Slew Rate (unity gain) (See *Figure 2*)	C_1 = 0.02 μF, R_1 = 33 Ω, C_2 = 10 pF
Channel Separation (See *Figure 4*)	R_S = 1 kΩ, f = 10 kHz
The following specifications apply for V+ = ±4.0 V, R_L = 10 kΩ to Pin 7, T_A = 25°C	
Input Offset Voltage	R_S = 200 Ω
Input Offset Current	
Input Bias Current	
Supply Current	V_{OUT} = 0
Internal Power Dissipation	V_{OUT} = 0
Large Signal Voltage Gain	V_{OUT} = ±2.0 V
Positive Output Voltage Swing	
Negative Output Voltage Swing	
The following specifications apply for T_A = T_{HIGH} to T_{LOW}, V_S = ±15 V, R_L = 5 kΩ to Pin 7.	
Large Signal Voltage Gain	V_{OUT} = ±10 V, T_A = HIGH
	V_{OUT} = ±10 V, T_A = LOW
Positive Output Voltage Swing	
Negative Output Voltage Swing	
Input Offset Voltage	R_S = 200 Ω
Input Offset Current	T_A = HIGH
	T_A = LOW
Input Bias Current	T_A = HIGH
	T_A = LOW
Input Offset Voltage Drift	R_S = 200 Ω, +25°C ≤ T_A ≤ HIGH
	R_S = 200 Ω, LOW ≤ T_A ≤ +25°C

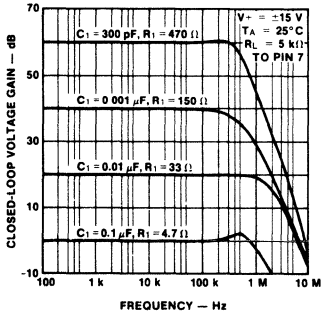
μA749C			μA749D V_{CC} = ±6 V, R_L = 10 K			μA739C			
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	1.0	6.0		1.0	10		1.0	6.0	mV
	50	750		50	600		50	1000	nA
	0.3	1.5		0.3	1.5		0.3	2.0	μA
50	150		50	150		37	150		kΩ
15,000	50,000		10,000	20,000		6,500	20,000		V/V
+12	+13		+4.5	+5.0		+12	+13		V
−14	−15		−5.5	−6.0		−14	−15		V
	5.0			10			5.0		kΩ
70	90		70	90		70	90		dB
	50	350		50	100		50		μV/V
−13		+11	−4		+2.5	−10		+11	V
	180	330							mW
	9.0	14	2.0	3.0	4.5		9.0	14	mA
	2.5			2.5			2.0		dB
	.2			.2			.2		μs
	.3			.3			.3		μs
	1.0			1.0			1.0		V/μs
	140			140			140		dB
		6.0					1.0	6.0	mV
	50	600					50	1000	nA
	.3	1.5					300		μA
	2.5						2.5		mA
	20						20		mW
15,000	60,000					2,500	15,000		V/V
+2.5	+2.8					+2.5	+2.8		V
−3.6	−4.0					−3.6	−4.0		V
8,000	40,000								V/V
15,000	50,000								V/V
+12	+13								V
−14	−15								V
	1.0	9.0							mV
	.05	1.5							μA
	.05	1.5							μA
	.3	3.0							μA
	.3	3.0							μA
	3.0								μV/°C
	3.0								μV/°C

μA749C, μA749D and μA739C
Electrical Characteristics (Cont.) $V+ = \pm 15$ V, $R_L = 5$ kΩ to Pin 7, $T_A = 25°C$ unless otherwise specified

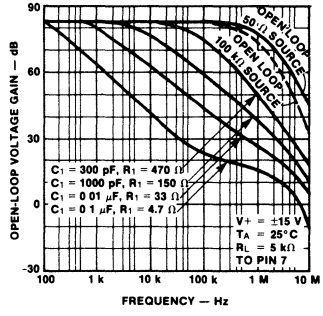
Characteristics	Condition
Input Offset Current Drift	$+25°C \leq T_A$
	LOW $\leq T_A \leq +25°C$
Input Bias Current Drift	LOW $\leq T_A \leq$ HIGH
Supply Current	$V_{OUT} = 0$, T_A =HIGH
	$V_{OUT} = 0$, T_A = LOW
Internal Power Dissipation	$V_{OUT} = 0$, T_A = HIGH
	$V_{OUT} = 0$, T_A = LOW
The following specifications apply for T_{HIGH} to T_{LOW}, $V_S = \pm 4.5$ V, $R_L = 10$ kΩ to Pin 7.	
Input Offset Voltage	$R_S = 200\ \Omega$
Input Offset Current	
Large Signal Voltage Gain	$V_{OUT} = \pm 2.0$ V, T_A =
	$V_{OUT} = \pm 2.0$ V, T_A =
Positive Output Voltage Swing	
Negative Output Voltage Swing	

Typical Performance Curves for μA749C and μA739C

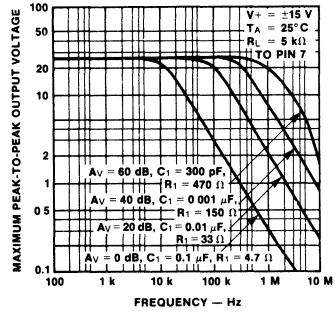
Closed Loop Gain as a Function of Frequency



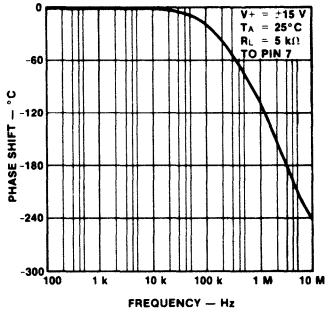
Open Loop Frequency Response Using Recommended Compensation Networks



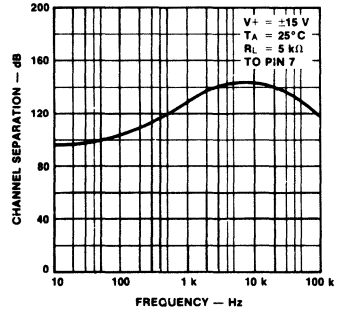
Output Capability as a Function of Frequency and Compensation



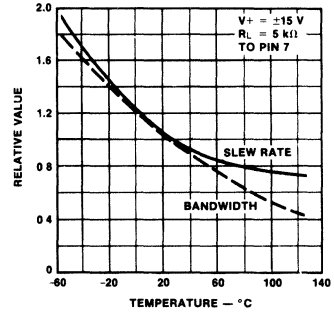
Open Loop Phase Shift Without Compensation



Channel Separation as Function of Frequency



Change of AC Characteristics With Temperature

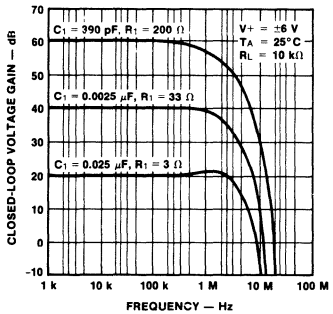


μA749C			μA749D V_{CC} = ±6 V, R_L = 10 K			μA739C			
Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
	.5								nA/°C
	2.0								nA/°C
	4.0								nA/°C
	10								mA
	10								mA
	100								mW
	200								mW
	1.5	7.0							mV
	50	1,000							nA
8,000									V/V
15,000									V/V
+2.5	+2.8								V
−3.6	−4.0								V

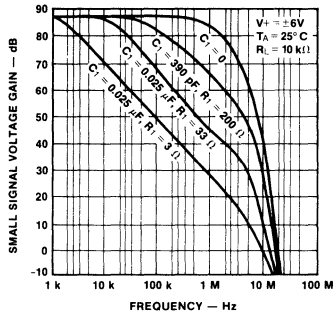
4

Typical Performance Curves for μA749D

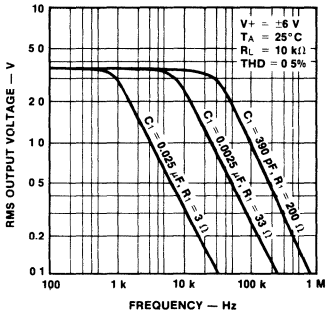
Closed Loop Gain as a Function of Frequency



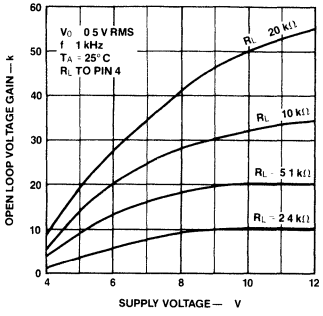
Open Loop Frequency Response Using Recommended Compensation Networks



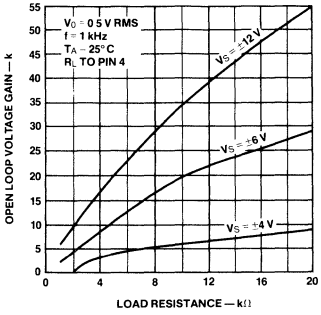
Output Voltage Swing as a Function of Frequency for Various Compensation Networks



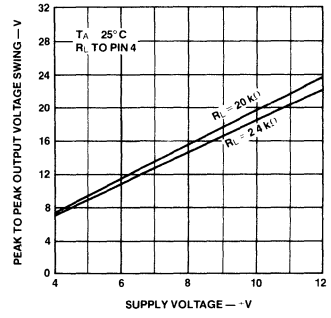
Open Loop Voltage Gain As a Function of Supply Voltage



Open Loop Voltage Gain As a Function of Load Resistance

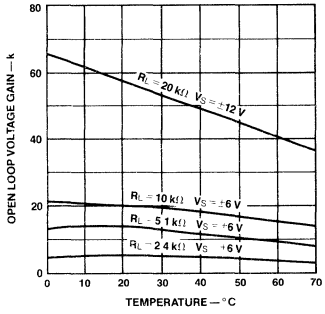


Typical Output Voltage As a Function of Supply Voltage

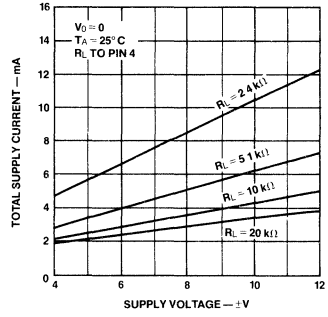


Typical Performance Curves for μA749D (Cont.)

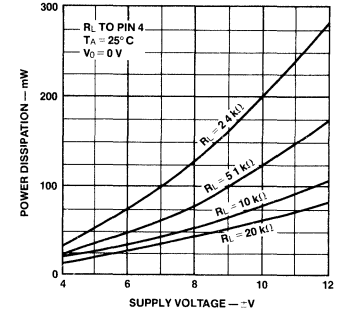
Open Loop Gain As a Function of Temperature



Total Supply Current As a Function of Supply Voltage

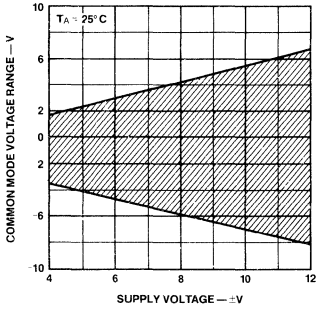


Total Power Dissipation As a Function of Supply Voltage and Load

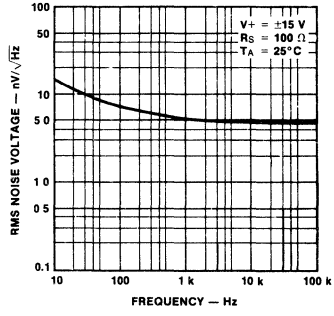


Typical Performance Curves for μA749 and μA749C

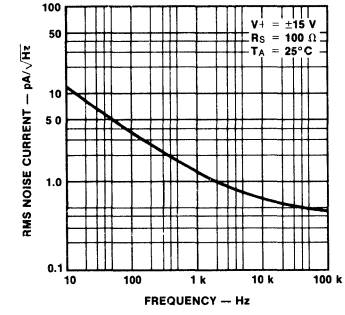
Common Mode Range As a Function of Supply Voltage



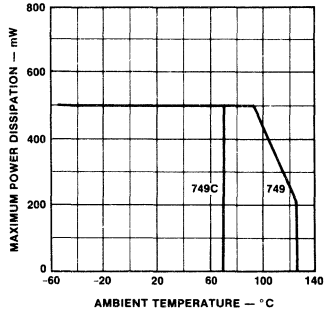
Input Noise Voltage as a Function of Frequency



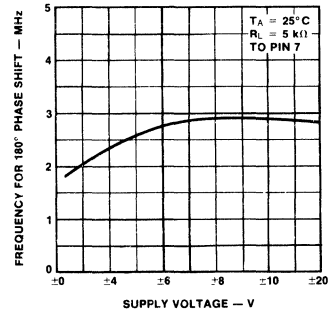
Input Noise Current as a Function of Frequency



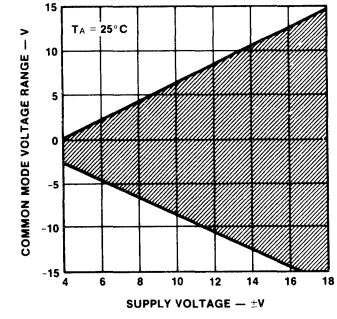
Absolute Maximum Power Dissipation as a Function of Temperature



Open Loop 180° Phase Shift Frequency as a Function of Supply Voltage

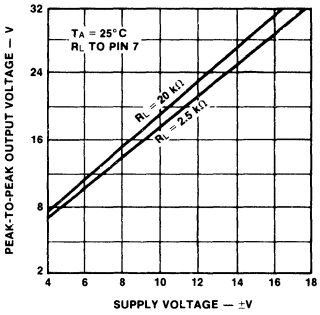


Common Mode Range as a Function of Supply Voltage

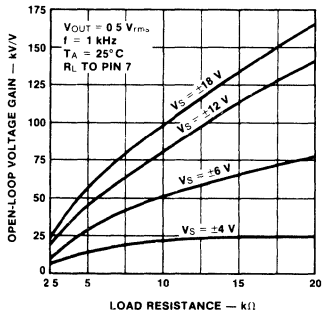


Typical Performance Curves for μA749 and μA749C (Cont.)

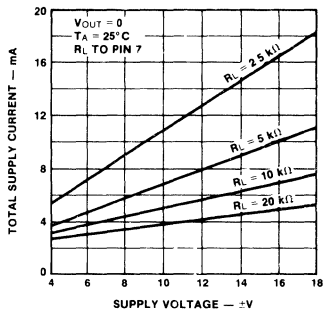
Typical Output Voltage as a Function of Supply Voltage



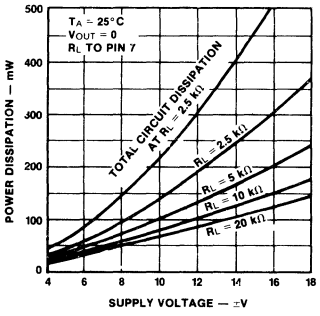
Open Loop Voltage Gain as a Function of Load Resistance



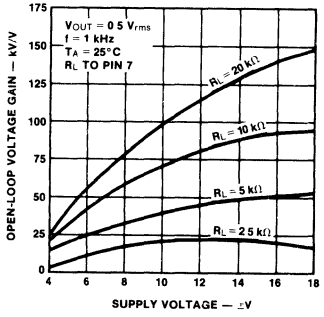
Total Supply Current as a Function of Supply Voltage



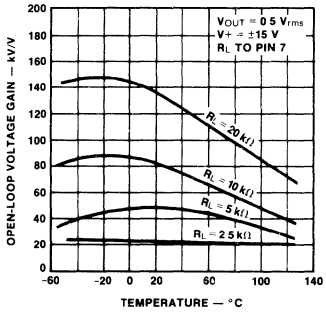
Total Power Dissipation as a Function of Supply Voltage and Load



Open Loop Voltage Gain as a Function of Supply Voltage

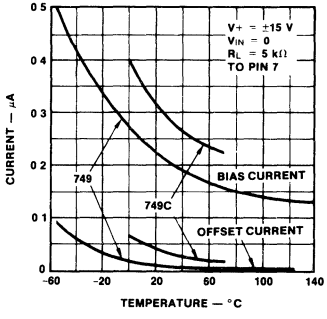


Open Loop Gain as a Function of Temperature

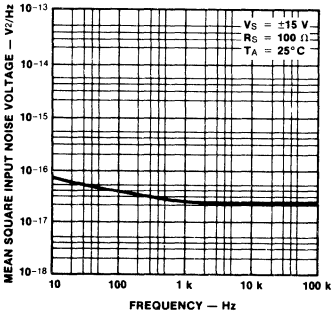


Typical Performance Curves for μA739C

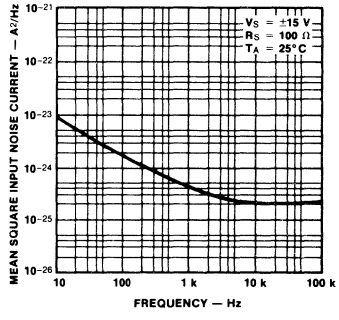
Input Offset Current and Bias Current as Functions of Temperature



Input Noise Voltage as a Function of Frequency

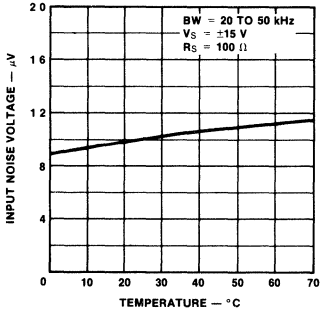


Input Noise Current as a Function of Frequency

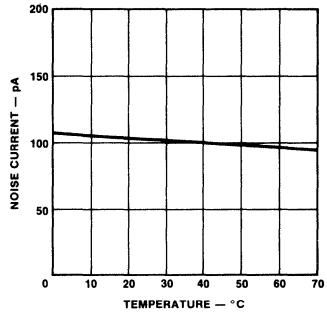


Typical Performance Curves for μA739C (Cont.)

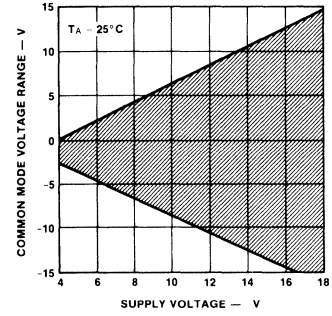
Wide Band Input Noise Voltage as a Function of Temperature



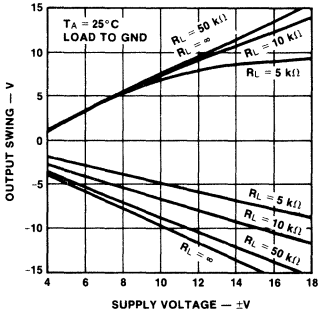
Wide Band Input Noise Current as a Function of Temperature



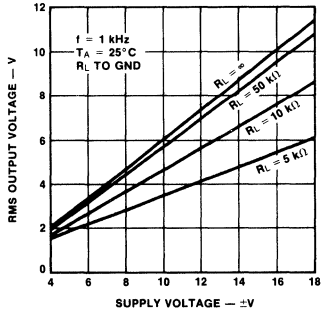
Common Mode Range as a Function of Supply Voltage



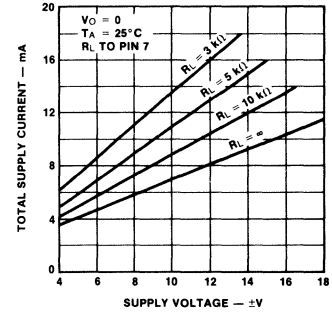
Typical Output Voltage as a Function of Supply Voltage



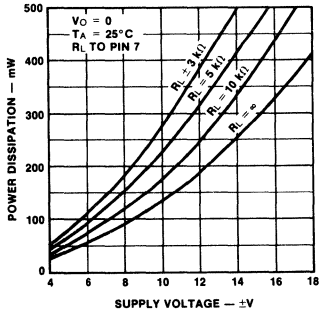
Output Capability as a Function of Supply Voltage



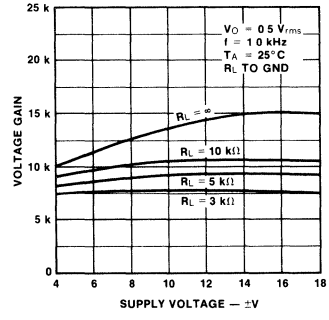
Total Supply Current as a Function of Supply Voltage



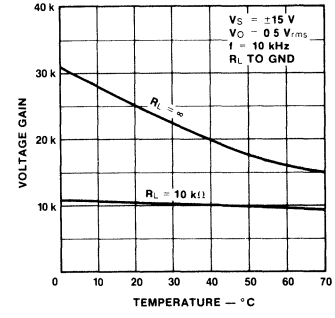
Total Power Dissipation as a Function of Supply Voltage and Load



Open Loop Voltage Gain as a Function of Supply Voltage

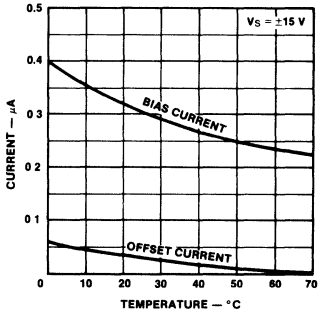


Open Loop Gain as a Function of Temperature



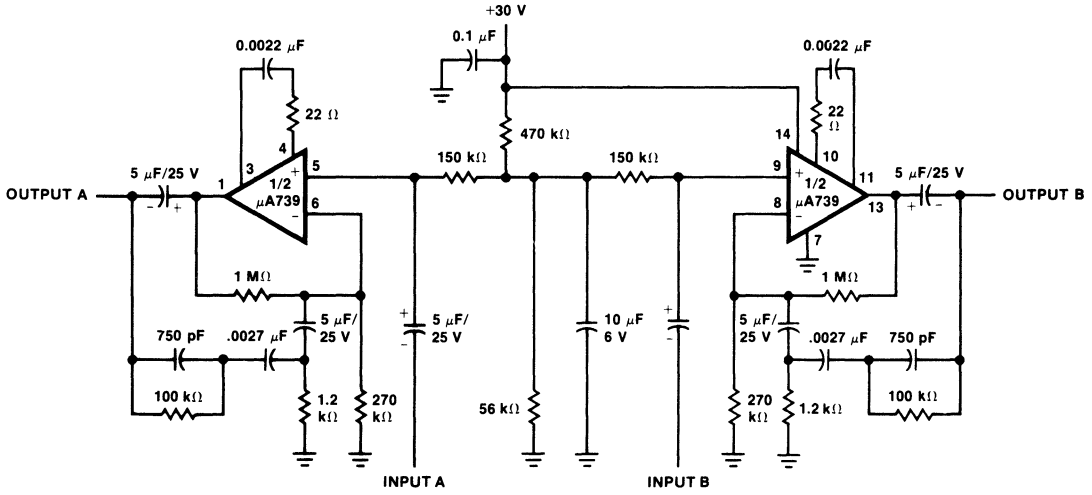
Typical Performance Curves for μA739C (Cont.)

Input Offset Current and Bias Current as a Function of Temperature



Typical Applications

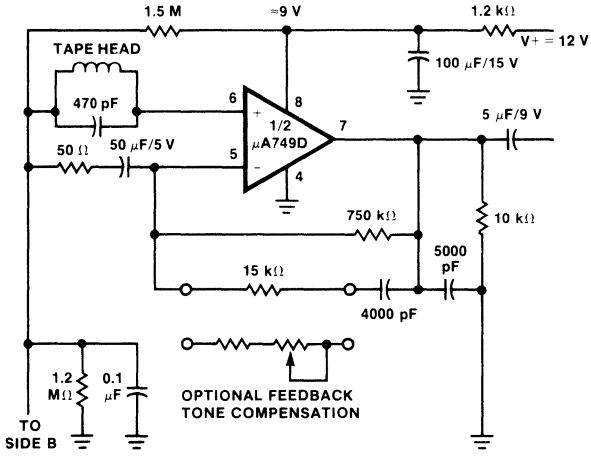
Stereo Phono Preamplifier—RIAA Equalized

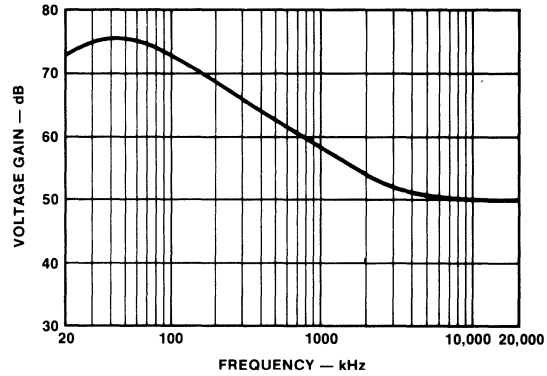


Typical Performance
Gain 40 dB at 1 kHz, RIAA equalized
Input overload point, 80 mV rms
Noise Level, 2 μV referred to input
Signal to noise ratio, 74 dB below 10 mW
Channel separation @ 1 kHz, 80 dB

Typical Applications (Cont.)

Stereo Tape Preamplifier





Typical Performance

Gain at 1 kHz	60 dB
Output Voltage Swing	2.8 V rms
Power Consumption	30 mW

FAIRCHILD
A Schlumberger Company

μA741 Operational Amplifier

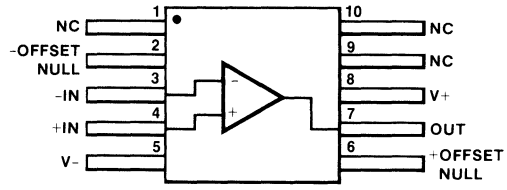
Linear Products

Description

The μA741 is a high performance Monolithic Operational Amplifier constructed using the Fairchild Planar epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

Connection Diagram 10-Pin Flatpak

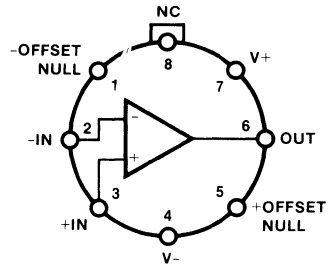


(Top View)

Order Information

Type	Package	Code	Part No.
μA741	Flatpak	3F	μA741FM
μA741A	Flatpak	3F	μA741AFM

Connection Diagram 8-Pin Metal Package



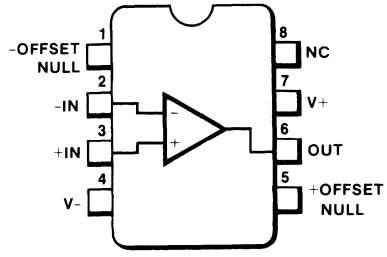
(Top View)

Pin 4 connected to case

Order Information

Type	Package	Code	Part No.
μA741	Metal	5W	μA741HM
μA741A	Metal	5W	μA741AHM
μA741C	Metal	5W	μA741HC
μA741E	Metal	5W	μA741EHC

Connection Diagram 8-Pin DIP



(Top View)

Order Information

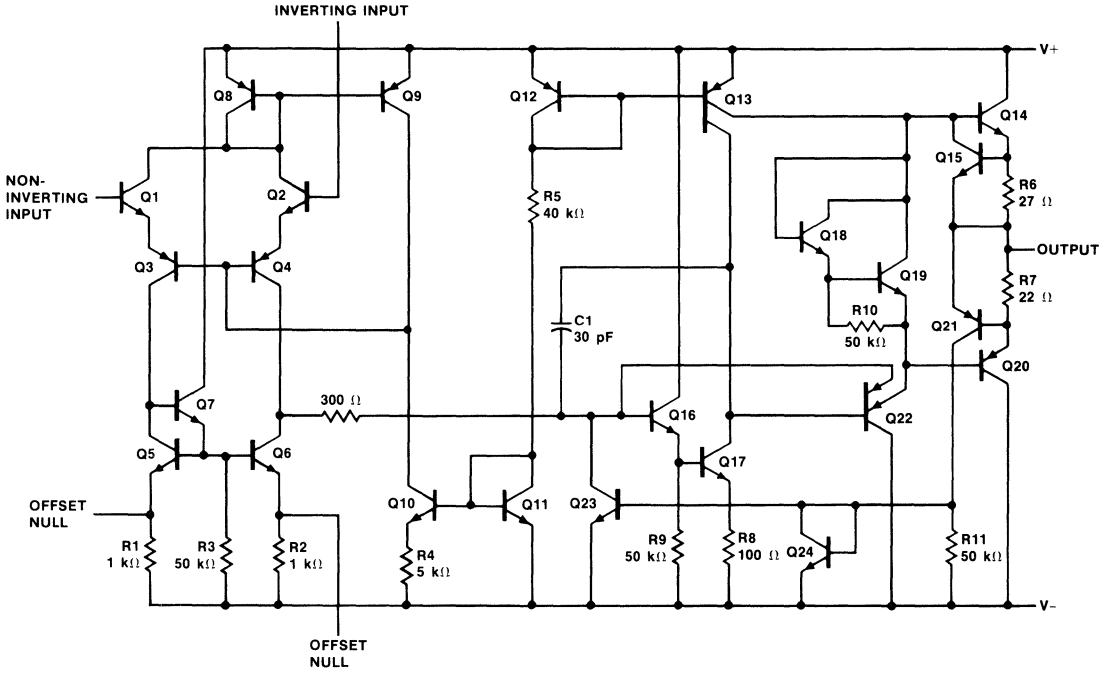
Type	Package	Code	Part No.
μA741C	Molded DIP	9T	μA741TC
μA741C	Ceramic DIP	6T	μA741RC

4

Absolute Maximum Ratings

Supply Voltage	
μA741A, μA741, μA741E	±22 V
μA741C	±18 V
Internal Power Dissipation (Note 1)	
Metal Package	500 MW
DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Package and Flatpak	−65°C to +150°C
DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA741A, μA741)	−55°C to +125°C
Commercial (μA741E, μA741C)	0°C to +70°C
Pin Temperature (Soldering 60 s)	
Metal Package, Flatpak, and Ceramic DIP	300°C
Molded DIP (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

Equivalent Circuit



Notes

1 Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6 3 mW/°C for the metal package, 7.1 mW/°C for the flatpak, and 5.6 mW/°C for the DIP

2 For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

3 Short circuit may be to ground or either supply Rating applies to +125°C case temperature or 75°C ambient temperature.

μA741 and μA741C
Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified

Characteristic		Condition	μA741 Min	μA741 Typ	μA741 Max	μA741C Min	μA741C Typ	μA741C Max	Unit
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0		2.0	6.0	mV
Input Offset Current				20	200		20	200	nA
Input Bias Current				80	500		80	500	nA
Power Supply Rejection Ratio		$V_S = +10, -20$ $V_S = +20, -10$ V, $R_S = 50\ \Omega$		30	150		30	150	μV/V
Input Resistance			.3	2.0		.3	2.0		MΩ
Input Capacitance				1.4			1.4		pF
Offset Voltage Adjustment Range				±15			±15		mV
Input Voltage Range						±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ				70	90		dB
Output Short Circuit Current				25			25		mA
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	50k	200k		20k	200k		
Output Resistance				75			75		Ω
Output Voltage Swing		$R_L \geq 10$ kΩ				±12	±14		V
		$R_L \geq 2$ kΩ				±10	±13		V
Supply Current				1.7	2.8		1.7	2.8	mA
Power Consumption				50	85		50	85	mW
Transient Response (Unity Gain)	Rise Time	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		.3			.3		μs
	Overshoot			5.0			5.0		%
Bandwidth (Note 4)				1.0			1.0		MHz
Slew Rate		$R_L \geq 2$ kΩ		.5			.5		V/μs

Notes
4 Calculated value from BW(MHz) = $\frac{0\ 35}{\text{Rise Time } (\mu s)}$

5 All $V_{CC} = 15$ V for μA741 and μA741C

6. Maximum supply current for all devices
   25°C = 2 8 mA
   125°C = 2.5 mA
   −55°C = 3 3 mA

μA741 and μA741C
Electrical Characteristics (Cont.) The following specifications apply over the range of $-55°C \leq T_A \leq 125°C$ for μA741, $0°C \leq T_A \leq 70°C$ for μA741C

Characteristic	Condition	μA741			μA741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage							7.5	mV
	$R_S \leq 10\ k\Omega$		1.0	6.0				mV
Input Offset Current							300	nA
	$T_A = +125°C$		7.0	200				nA
	$T_A = -55°C$		85	500				nA
Input Bias Current							800	nA
	$T_A = +125°C$		.03	.5				μA
	$T_A = -55°C$		.3	1.5				μA
Input Voltage Range		±12	±13					V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90					dB
Adjustment for Input Offset Voltage			±15			±15		mV
Supply Voltage Rejection Ratio	$V_S = +10, -20$; $V_S = +20, -10\ V$, $R_S = 50\ \Omega$		30	150				μV/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14					V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10\ V$	25k			15k			
Supply Current	$T_A = +125°C$		1.5	2.5				mA
	$T_A = -55°C$		2.0	3.3				mA
Power Consumption	$T_A = +125°C$		45	75				mW
	$T_A = -55°C$		60	100				mW

Notes
4 Calculated value from BW(MHz) = $\frac{0.35}{\text{Rise Time } (\mu s)}$

5. All $V_{CC} = 15\ V$ for μA741 and μA741C.
6. Maximum supply current for all devices
   25°C = 2 8 mA
   125°C = 2.5 mA
   −55°C = 3 3 mA

μA741A and μA741E
Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

Characteristic	Condition	μA741A/E Min	Typ	Max	Unit
Input Offset Voltage	$R_S \leq 50\ \Omega$		0.8	3.0	mV
Average Input Offset Voltage Drift				15	μV/°C
Input Offset Current			3.0	30	nA
Average Input Offset Current Drift				0.5	nA/°C
Input Bias Current			30	80	nA
Power Supply Rejection Ratio	$V_S = +10, -20$; $V_S = +20$ V, -10 V, $R_S = 50\ \Omega$		15	50	μV/V
Output Short Circuit Current		10	25	40	mA
Power Consumption	$V_S = \pm 20$ V		80	150	mW
Input Impedance	$V_S = \pm 20$ V	1.0	6.0		MΩ
Large Signal Voltage Gain	$V_S = \pm 20$ V, $R_L = 2$ kΩ, $V_{OUT} = \pm 15$ V	50	200		V/mV
Transient Response (Unity Gain) — Rise Time			0.25	0.8	μs
Transient Response (Unity Gain) — Overshoot			6.0	20	%
Bandwidth (Note 4)		.437	1.5		MHz
Slew Rate (Unity Gain)	$V_{IN} = \pm 10$ V	0.3	0.7		V/μs

The following specifications apply over the range of $-55°C \leq T_A \leq 125°C$ for the 741A, and $0°C \leq T_A \leq 70°C$ for the 741E.

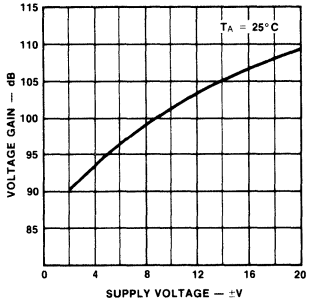
Input Offset Voltage					4.0	mV
Input Offset Current					70	nA
Input Bias Current					210	nA
Common Mode Rejection Ratio	$V_S = \pm 20$ V, $V_{IN} = \pm 15$ V, $R_S = 50\ \Omega$		80	95		dB
Adjustment For Input Offset Voltage	$V_S = \pm 20$ V		10			mV
Output Short Circuit Current			10		40	mA
Power Consumption	$V_S = \pm 20$ V, μA741A, −55°C				165	mW
Power Consumption	$V_S = \pm 20$ V, μA741A, +125°C				135	mW
Power Consumption	$V_S = \pm 20$ V, μA741E				150	mW
Input Impedance	$V_S = \pm 20$ V		0.5			MΩ
Output Voltage Swing	$V_S = \pm 20$ V, $R_L = 10$ kΩ		±16			V
Output Voltage Swing	$V_S = \pm 20$ V, $R_L = 2$ kΩ		±15			V
Large Signal Voltage Gain	$V_S = \pm 20$ V, $R_L = 2$ kΩ, $V_{OUT} = \pm 15$ V		32			V/mV V/mV
Large Signal Voltage Gain	$V_S = \pm 5$ V, $R_L = 2$ kΩ, $V_{OUT} = \pm 2$ V		10			V/mV

Notes

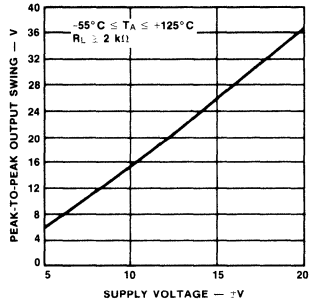
4. Calculated value from: $BW(MHz) = \frac{0.35}{\text{Rise Time } (\mu s)}$
5. All $V_{CC} = 15$ V for μA741 and μA741C
6. Maximum supply current for all devices
   25°C = 2 8 mA
   125°C = 2 5 mA
   −55°C = 3 3 mA

Typical Performance Curves for μA741A and μA741

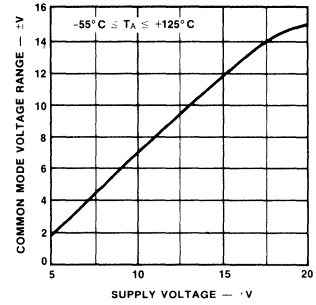
Open Loop Voltage Gain as a Function of Supply Voltage



Output Voltage Swing as a Function of Supply Voltage

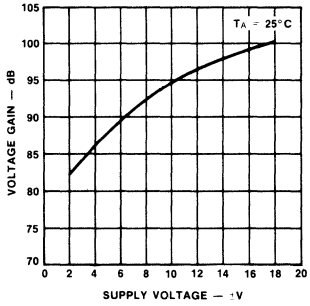


Input Common Mode Voltage as a Function of Supply Voltage

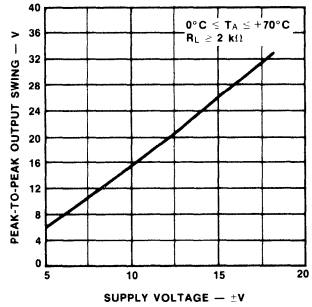


Typical Performance Curves for μA741E and μA741C

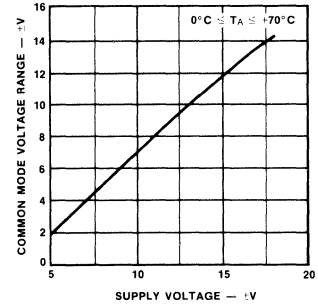
Open Loop Voltage Gain as a Function of Supply Voltage



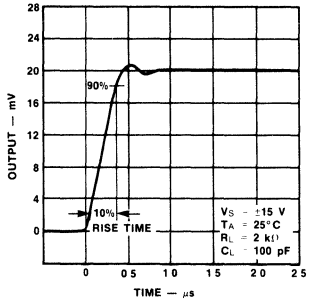
Output Voltage Swing as a Function of Supply Voltage



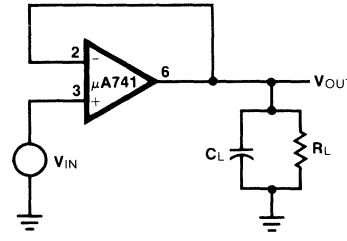
Input Common Mode Voltage Range as a Function of Supply Voltage



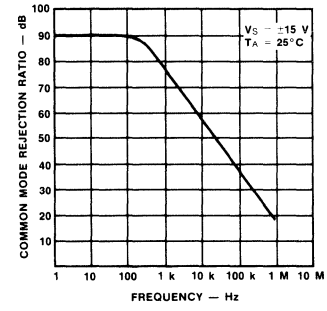
Transient Response



Transient Response Test Circuit

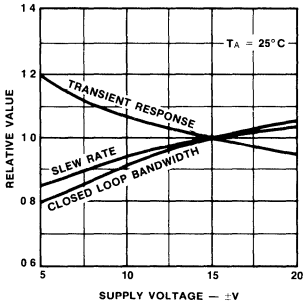


Common Mode Rejection Ratio as a Function of Frequency

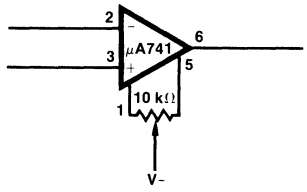


Typical Performance Curves for μA741E and μA741C (Cont.)

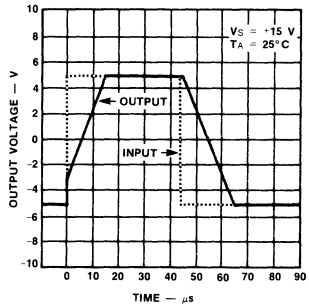
Frequency Characteristics as a Function of Supply Voltage



Voltage Offset Null Circuit

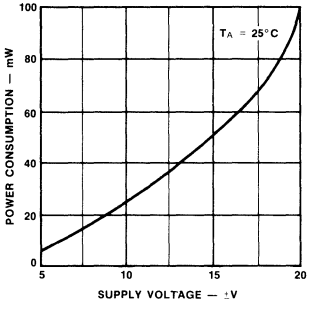


Voltage Follower Large Signal Pulse Response

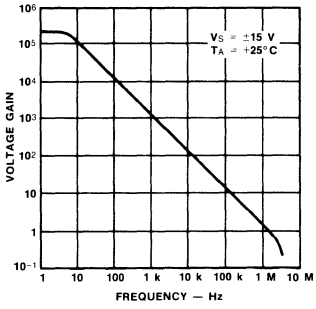


Typical Performance Curves for μA741A, μA741, μA741E and μA741C

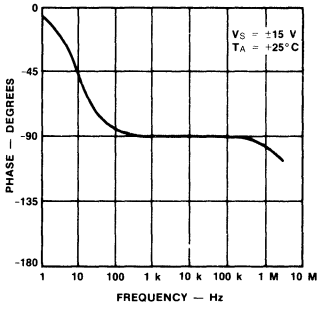
Power Consumption as a Function of Supply Voltage



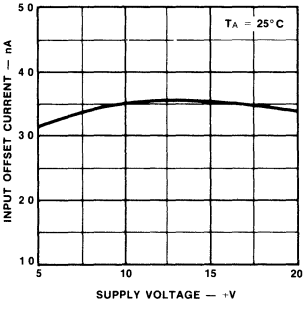
Open Loop Voltage Gain as a Function of Frequency



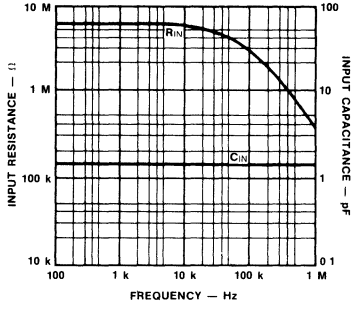
Open Loop Phase Response as a Function of Frequency



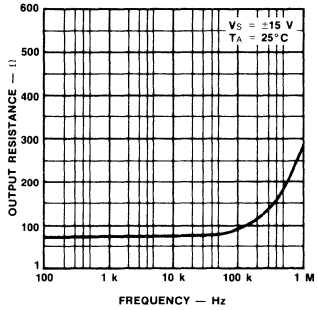
Input Offset Current as a Function of Supply Voltage



Input Resistance and Input Capacitance as a Function of Frequency

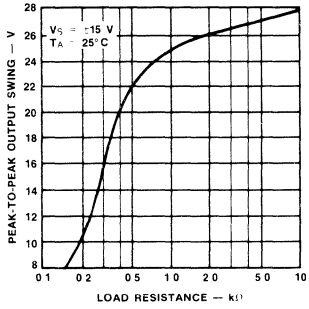


Output Resistance as a Function of Frequency

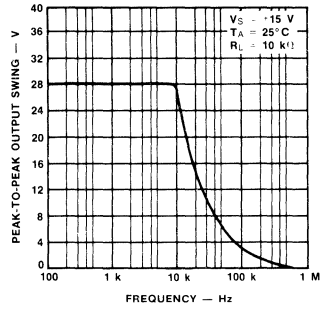


Typical Performance Curves for μA741A, μA741, μA741E and μA741C (Cont.)

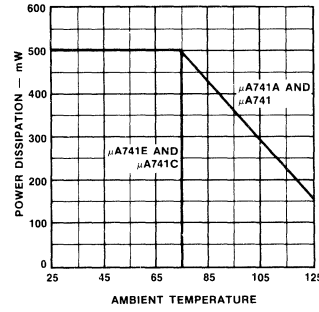
Output Voltage Swing as a Function of Load Resistance



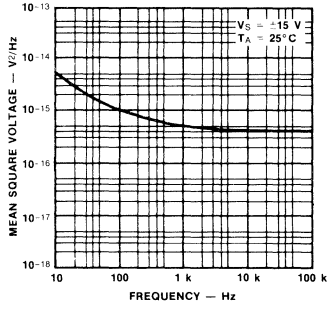
Output Voltage Swing as a Function of Frequency



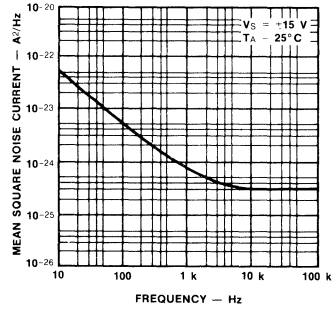
Absolute Maximum Power Dissipation as a Function of Ambient Temperature



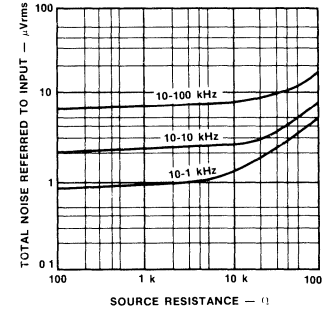
Input Noise Voltage as a Function of Frequency



Input Noise Current as a Function of Frequency

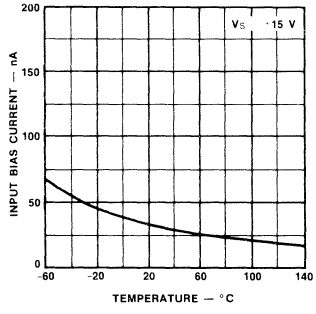


Broadband Noise for Various Bandwidths

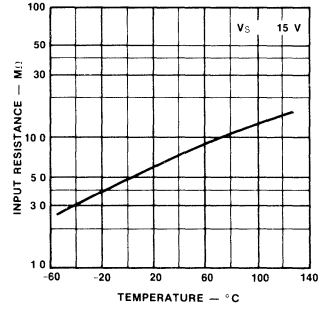


Typical Performance Curves for μA741A and μA741

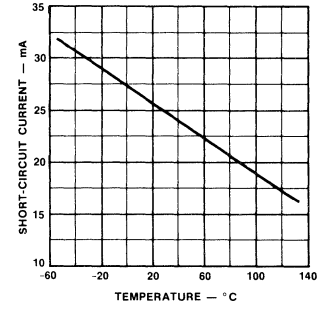
Input Bias Current as a Function of Ambient Temperature



Input Resistance as a Function of Ambient Temperature

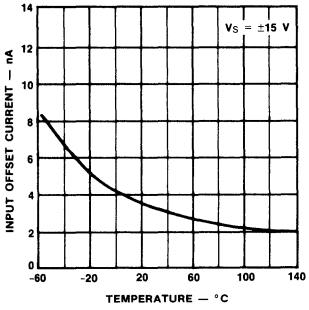


Output Short-Circuit Current as a Function of Ambient Temperature

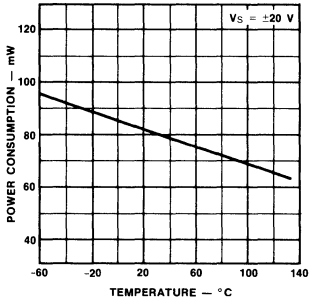


Typical Performance Curves for μA741A and μA741 (Cont.)

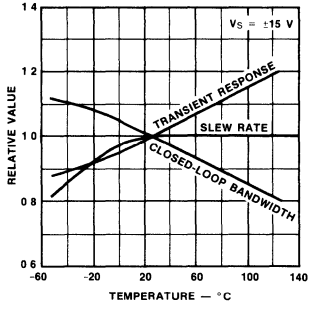
Input Offset Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature

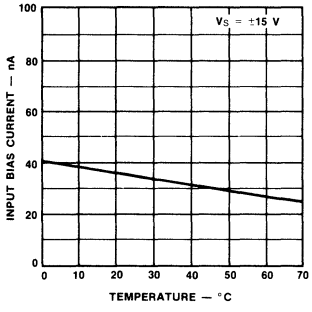


Frequency Characteristics as a Function of Ambient Temperature

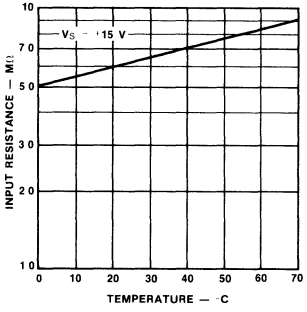


Typical Performance Curves for μA741E and μA741C

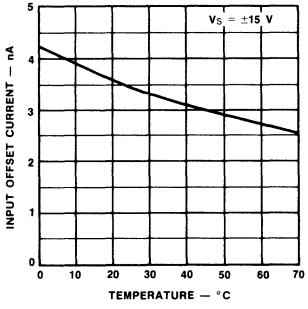
Input Bias Current as a Function of Ambient Temperature



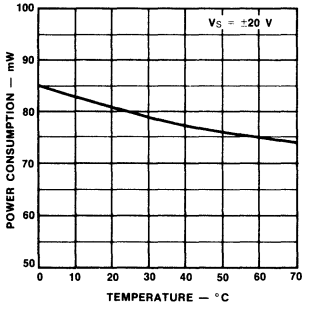
Input Resistance as a Function of Ambient Temperature



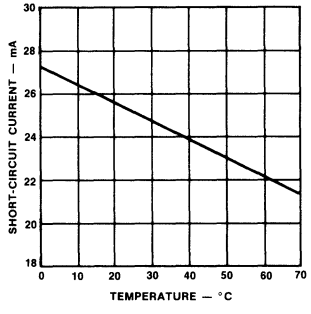
Input Offset Current as a Function of Ambient Temperature



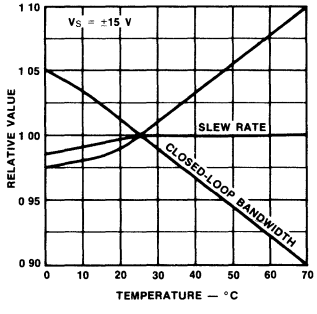
Power Consumption as a Function of Ambient Temperature



Output Short Circuit Current as a Function of Ambient Temperature



Frequency Characteristics as a Function of Ambient Temperature



4

FAIRCHILD

A Schlumberger Company

μA747 Dual Operational Amplifier

Linear Products

Description

The μA747 is a pair of high performance Monolithic Operational Amplifiers constructed using the Fairchild Planar epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of latch-up make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

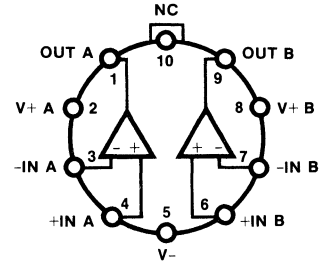
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

Absolute Maximum Ratings

Supply Voltage	
Military (μA747A, μA747, μA747E)	±22 V
Commercial (μA747C)	±18 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
DIP	670 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage Between Offset Null and V−	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA747A, μA747)	−55°C to +125°C
Commercial (μA747E, μA747C)	0°C to 70°C
Pin Temperature (Soldering)	
Metal and Ceramic DIP (60 s)	300°C
Molded DIP (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

Notes on following pages.

Connection Diagram
10-Pin Metal Package



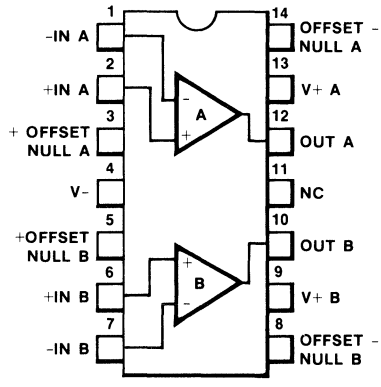
(Top View)

V + A is internally connected to V + B for μA747A, μA747, μA747E, and μA747C.

Order Information

Type	Package	Code	Part No.
μA747	Metal	5X	μA747HM
μA747A	Metal	5X	μA747AHM
μA747C	Metal	5X	μA747HC
μA747E	Metal	5X	μA747EHC

Connection Diagram
14-Pin DIP

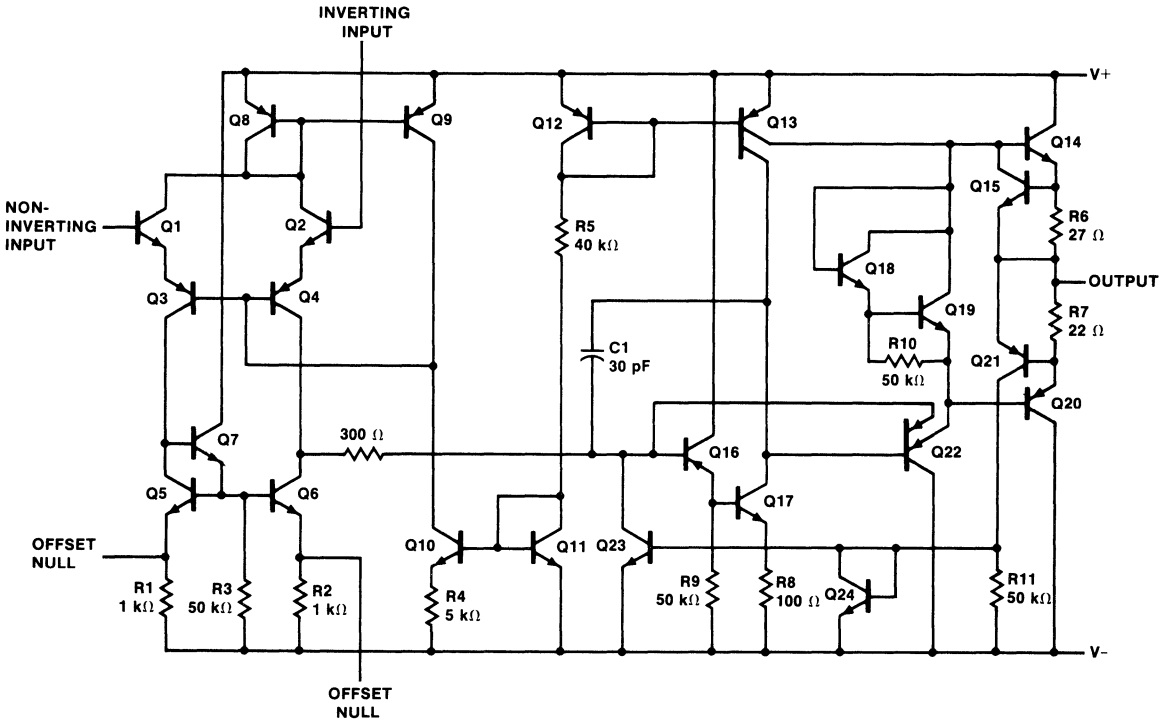


(Top View)

Order Information

Type	Package	Code	Part No.
μA747	Ceramic DIP	6A	μA747DM
μA747A	Ceramic DIP	6A	μA747ADM
μA747C	Ceramic DIP	6A	μA747DC
μA747C	Molded DIP	9A	μA747PC
μA747E	Ceramic DIP	6A	μA747EDC

Equivalent Circuit (1/2 of circuit shown)



Notes

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Package and 7 1 mW/°C for the DIP
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.

μA747 and μA747C
Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified

Characteristic		Condition	μA747 Min	μA747 Typ	μA747 Max	μA747C Min	μA747C Typ	μA747C Max	Unit
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0		1.0	6.0	mV
Input Offset Current				20	200		20	200	nA
Input Bias Current				80	500		80	500	nA
Power Supply Rejection Ratio		$V_S = +10, -20$; $V_S = +20, -10$ V, $R_S = 50\ \Omega$		30	150		30	150	μV/V
Input Resistance			.3	2.0		.3	2.0		MΩ
Input Capacitance				1.4			1.4		pF
Offset Voltage Adjustment Range				±15			±15		mV
Output Short Circuit Current				25			25		mA
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	50k	200k		25k	200k		
Output Resistance				75			75		Ω
Supply Current (Total)				3.4	5.6		3.9	5.6	mA
Power Consumption (Total)				100	170		100	170	mW
Transient Response (Unity Gain)	Rise Time	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		.3			.3		μs
	Overshoot			5.0			5.0		%
Bandwidth (Note 4)				1.0			1.0		MHz
Slew Rate		$R_L \geq 2$ kΩ		.5			.5		V/μs
Channel Separation				120			120		dB

The following specifications apply over the range of $-55°C \leq T_A \leq 125°C$ for μA747, $0°C \leq T_A \leq 70°C$ for μA747C

Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0		1.0	7.5	mV
Input Offset Current						7.0	300	nA
	$T_A = +125°C$		7.0	200				nA
	$T_A = -55°C$		85	500				nA
Input Bias Current						30	800	nA
	$T_A = +125°C$		.03	.5				μA
	$T_A = -55°C$		.3	1.5				μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$V_S = +10, -20$; $V_S = +20, -10$ V, $R_S = 50\ \Omega$		30	150		30	150	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	25k			15k			
Supply Current (Total)						4.0	6.6	mA
	$T_A = +125°C$		3.0	5.0				mA
	$T_A = -55°C$		4.0	6.6				mA
Power Consumption (Total)						120	200	mW
	$T_A = +125°C$		90	150				mW
	$T_A = -55°C$		120	200				mW

Note
4 Calculated value from $BW(MHz) = \frac{0.35}{\text{Rise Time } (\mu s)}$

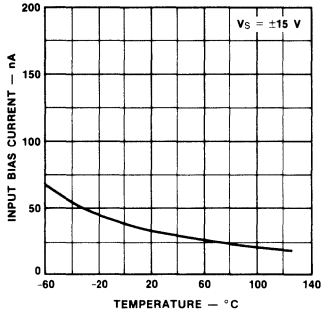
μA747A and μA747E
Electrical Characteristics $\pm 5\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$ unless otherwise specified.

Characteristic	Condition			μA747A/E Min	Typ	Max	Unit
Input Offset Voltage	$R_S \leq 50\ \Omega$				0.8	3.0	mV
Average Input Offset Voltage Drift						15	μV/°C
Input Offset Current					3	30	nA
Average Input Offset Current Drift	μA747E	$T_A = 25°C$ to 70°C				0.2	nA/°C
		$T_A = 0°C$ to 25°C				0.5	nA/°C
	μA747A	$T_A = 25°C$ to 125°C				0.2	nA/°C
		$T_A = -55°C$ to 0°C				0.5	nA/°C
Input Bias Current					30	80	nA
Power Supply Rejection Ratio	$V_S = +10, -20$; $V_S = +20\ V, -10\ V$, $R_S = 50\ \Omega$				15	50	μV/V
Common Mode Rejection Ratio	$V_S = \pm 20\ V$, $V_{IN} = \pm 15\ V$, $R_S = 50\ \Omega$			80	95		dB
Adjustment For Input Offset Voltage	$V_S = \pm 20\ V$			10			mV
Output Short Circuit Current	μA747A			10	25	40	mA
	μA747E			10	25	35	mA
Power Consumption	$V_S = \pm 20\ V$				160	300	mW
Input Impedance	$V_S = \pm 20\ V$			1.0	6		MΩ
Large Signal Voltage Gain	$V_S = \pm 20\ V$, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 15\ V$			50			V/mV
Transient Response (Unity Gain) Rise Time	$V_{IN} = 20\ mV$, $R_L = 2\ k\Omega$, $C_L \leq 100\ V_S$				0.25	0.8	μs
Transient Response (Unity Gain) Overshoot					6	20	%
Bandwidth (Note 4)				0.437	1.5		MHz
Slew Rate (Unity Gain)	$V_{IN} = \pm 10\ V$			0.3	0.7		V/μs
The following specifications apply over the range of $-55°C \leq T_A \leq 125°C$ for μA747A, $0°C \leq T_A \leq 70°C$ for μA747E							
Input Offset Voltage						4.0	mV
Input Offset Current						70	nA
Input Bias Current						210	nA
Output Short Circuit Current				10		40	mA
Power Consumption	$V_S = \pm 20\ V$	μA747A	−55°C			330	mW
			+125°C			270	mW
		μA747E				330	mW
Input Impedance	$V_S = \pm 20\ V$			0.5			MΩ
Output Voltage Swing	$V_S = \pm 20\ V$	$R_L = 10\ k\Omega$		±16			V
		$R_L = 2\ k\Omega$		±15			V
Large Signal Voltage Gain	$V_S = \pm 20\ V$, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 15\ V$			32			V/mV
	$V_S = \pm 5\ V$, $R_L = 2\ k\Omega$, $V_{OUT} = \pm 2\ V$			10			V/mV
Channel Separation	$V_S = \pm 20\ V$			100			dB

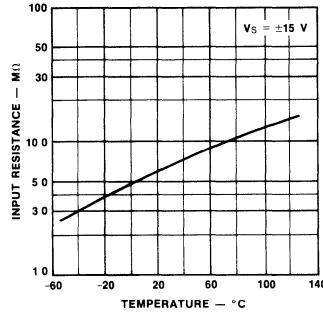
Note
4 Calculated value from: $BW(MHz) = \frac{0.35}{\text{Rise Time } (\mu s)}$

Typical Performance Curves for μA747A and μA747

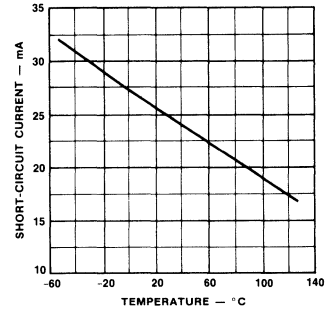
Input Bias Current as a Function of Ambient Temperature



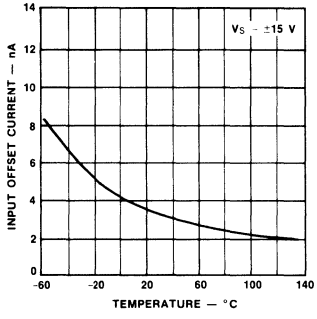
Input Resistance as a Function of Ambient Temperature



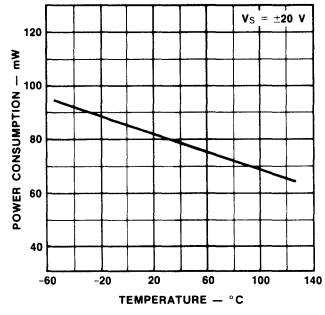
Output Short Circuit Current as a Function of Ambient Temperature



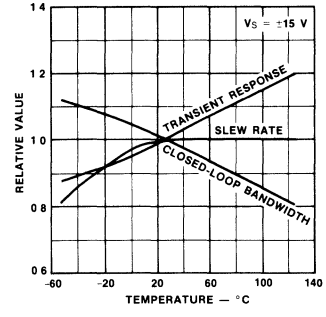
Input Offset Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature

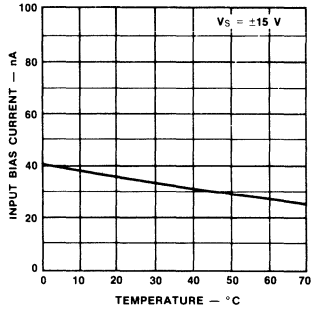


Frequency Characteristics as a Function of Ambient Temperature

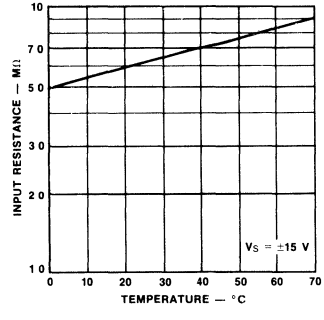


Typical Performance Curves for μA747E and μA747C

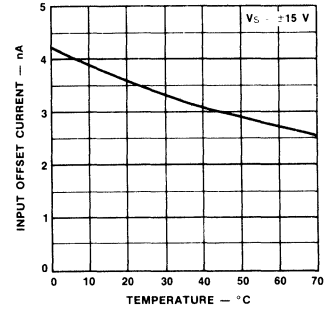
Input Bias Current as a Function of Ambient Temperature



Input Resistance as a Function of Ambient Temperature

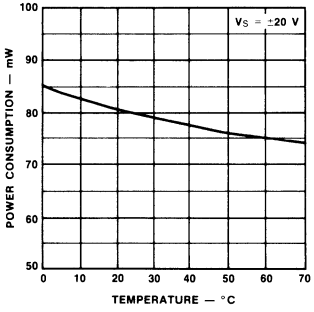


Input Offset Current as a Function of Ambient Temperature

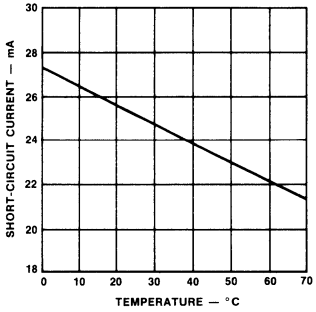


Typical Performance Curves for μA747E and μA747C (Cont.)

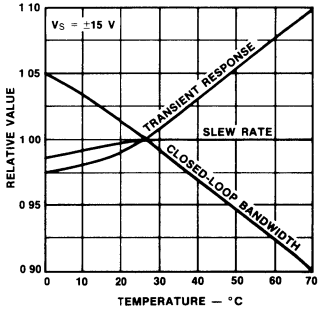
Power Consumption as a Function of Ambient Temperature



Output Short-Circuit Current as a Function of Ambient Temperature

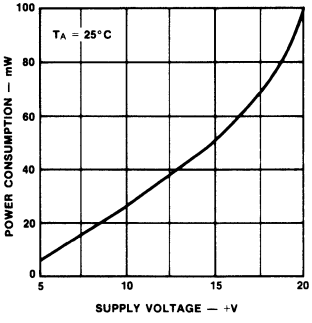


Frequency Characteristics as a Function of Ambient Temperature

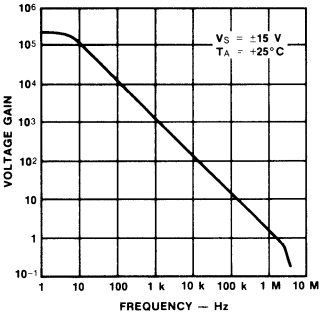


Typical Performance Curves for μA747A, μA747C, μA747 and μA747E

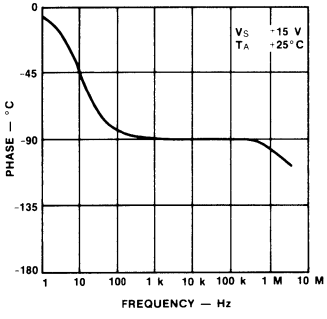
Power Consumption as a Function of Supply Voltage



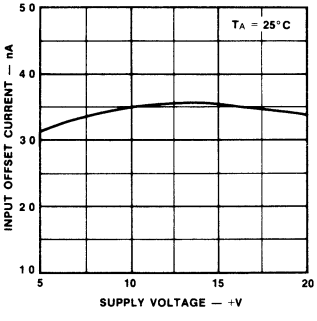
Open Loop Voltage Gain as a Function of Frequency



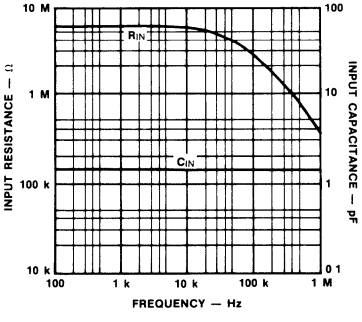
Open Loop Phase Response as a Function of Frequency



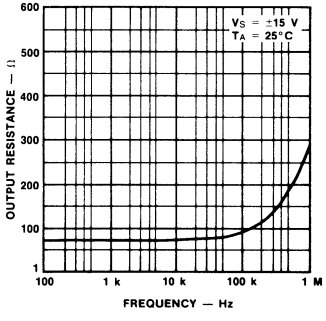
Input Offset Current as a Function of Supply Voltage



Input Resistance and Input Capacitance as a Function of Frequency



Output Resistance as a Function of Frequency



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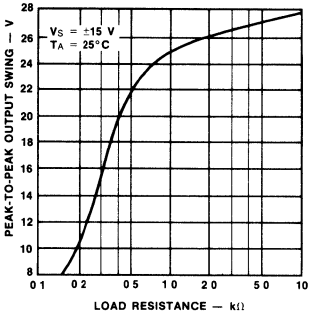
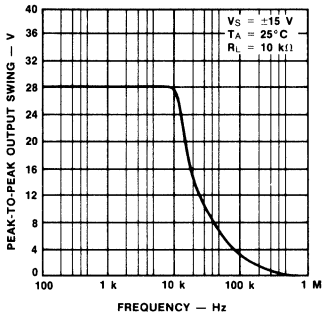
Typical Performance Curves for μA747A, μA747C, μA747 and μA747E (Cont.)

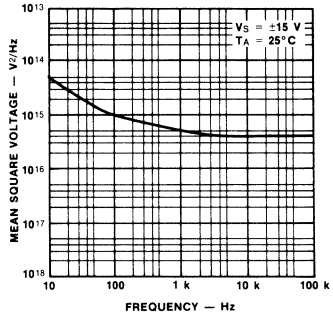
Output Voltage Swing as a Function of Load Resistance



Output Voltage Swing as a Function of Frequency

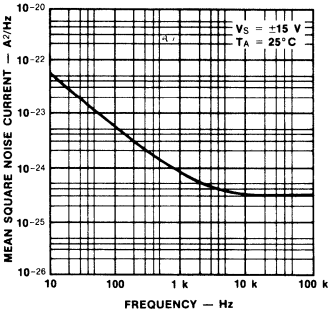


Input Noise Voltage Density as a Function of Frequency

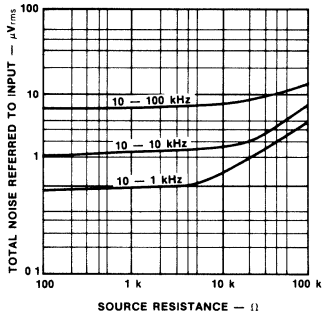


Typical Performance Curves for μA747 and μA747C

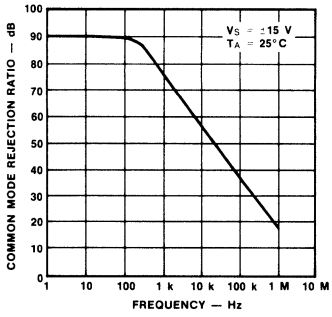
Input Noise Current Density as a Function of Frequency



Broadband Noise for Various Bandwidths

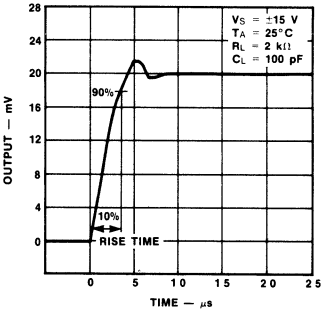


Common Mode Rejection Ratio as a Function of Frequency

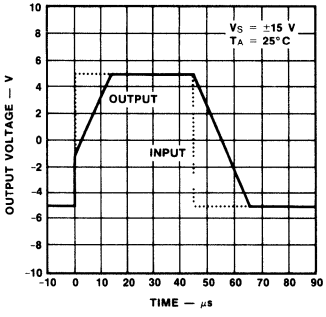


Typical Performance Curves for μA747 and μA747C (Cont.)

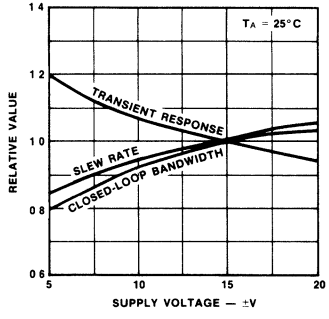
Transient Response



Voltage Follower Large Signal Pulse Response

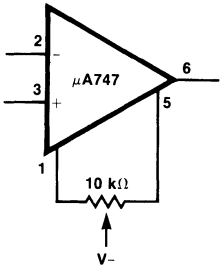


Frequency Characteristics as a Function of Supply Voltage

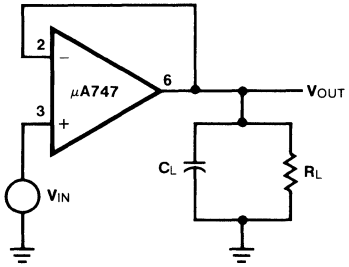


Test Circuits

Voltage Offset Null Circuit

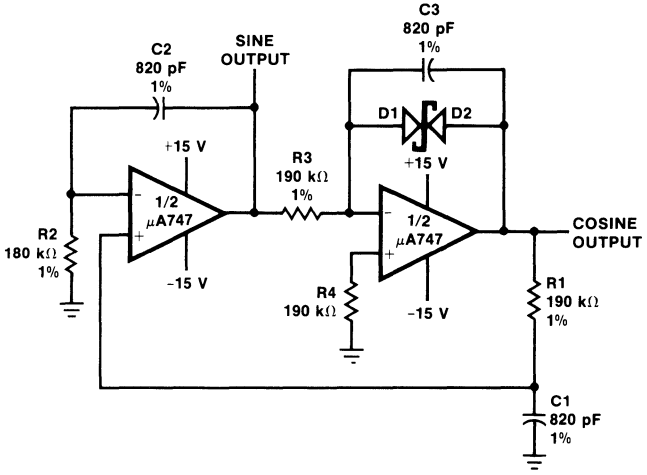


Transient Response Test Circuit



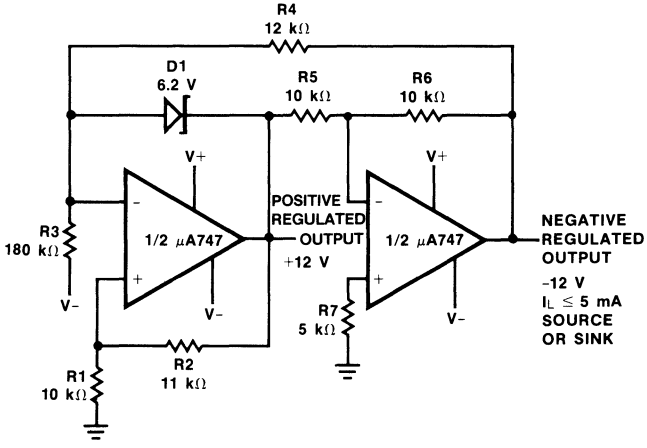
Typical Applications

Quadrature Oscillator



$$f = \frac{1}{2\pi\sqrt{C2R2C3R3}} \quad (R1C1 = R2C2)$$

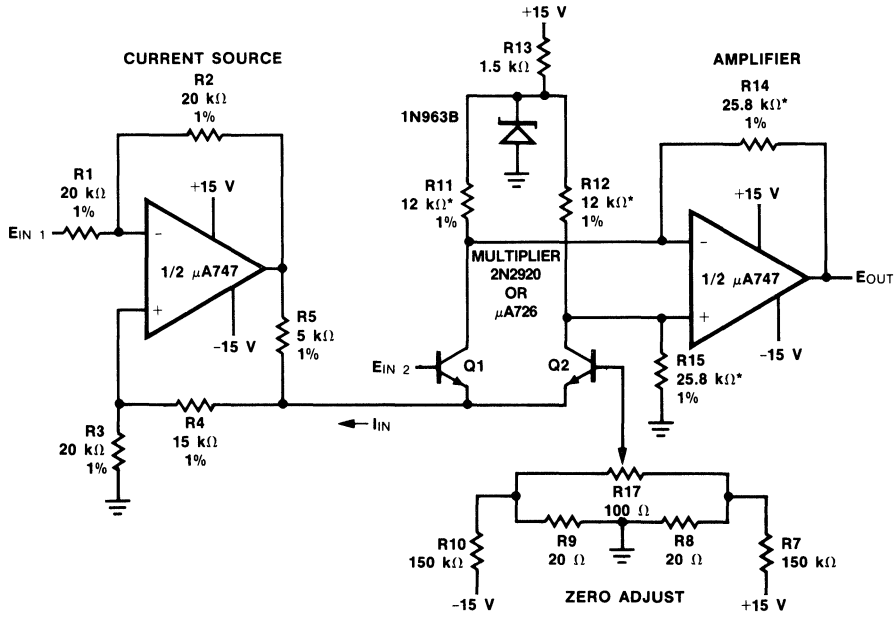
Tracking Positive and Negative Voltage References



$$\text{Positive Output} = V_{D1} \times \frac{R1 + R2}{R2}$$

$$\text{Negative Output} = -\text{Positive Output} \times \frac{R6}{R5}$$

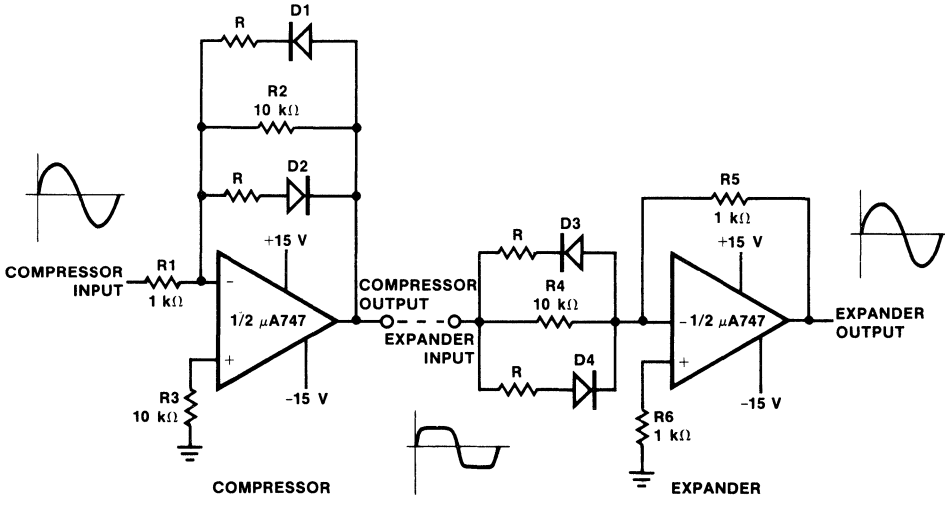
Analog Multiplier



*Matched to 0 1%

$E_{OUT} = 100E_{IN_1} \times E_{IN_2}$

Compressor/Expander Amplifiers



Notes

1. Maximum Compression Expansion Ratio = R/R (10 kΩ > R ≥ 0)
2. Diodes D1 through D4 are matched FD666 or Equivalent

FAIRCHILD
A Schlumberger Company

μA748 Operational Amplifier

Linear Products

Description

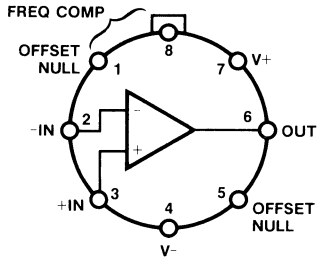
The μA748 is a High Performance Monolithic Operational Amplifier constructed using the Fairchild Planar epitaxial process. It is intended for a high wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of latch-up make the μA748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA748 is short circuit protected and has the same pin configuration as the popular μA741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor.

- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

Absolute Maximum Ratings

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Package	−65°C to +150°C
DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA748)	−55°C to +125°C
Commercial (μA748C)	0°C to +70°C
Pin Temperature (Soldering 60 s)	
Metal Package	300°C
Molded DIP (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

Connection Diagram 8-Pin Metal Package



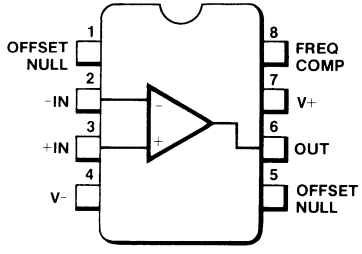
(Top View)

Pin 4 connected to case

Order Information

Type	Package	Code	Part No.
μA748	Metal	5W	μA748HM
μA748C	Metal	5W	μA748HC

Connection Diagram 8-Pin DIP



(Top View)

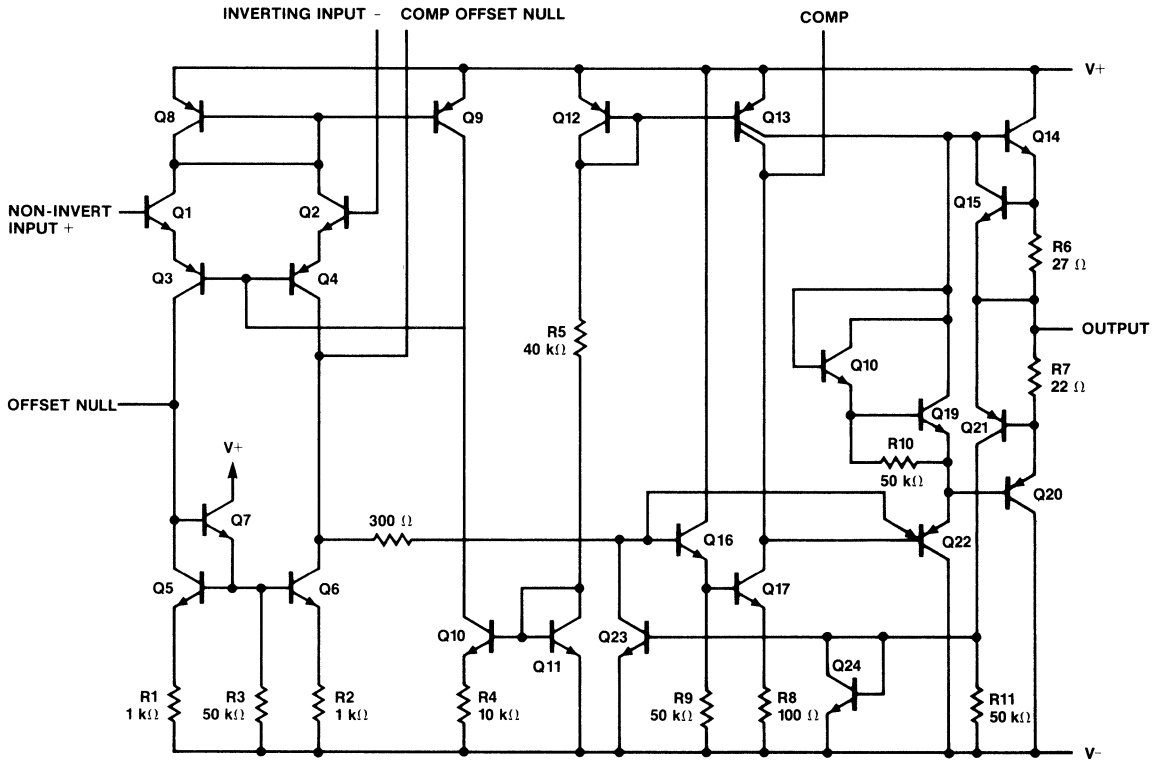
Order Information

Type	Package	Code	Part No.
μA748C	Molded DIP	9T	μA748TC

Notes

1. Rating applies to ambient temperatures up to 70°C Above 70°C ambient derate linearly at 6 3 mW/°C for metal package, 5 6 mW/°C for the DIP
2. For supply voltages less than ± 15 V, the absolute maximum input voltage in equal to the supply voltage
3. Short circuit may be to ground or either supply Rating applies to +125°C case temperature or +75°C ambient temperature

Equivalent Circuit



μA748 and μA78A
Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified.

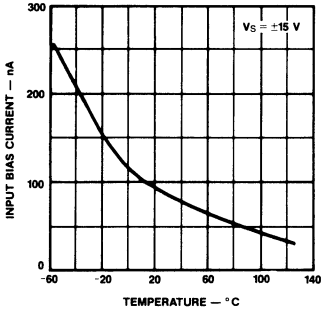
Characteristic		Condition	μA748A			μA748			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage		$R_S \leq 10$ kΩ		0.5	2.0		1.0	5.0	mV
Input Offset Current				2.0	10		20	200	nA
Input Bias Current				20	75		80	500	nA
Input Resistance			2.0	10.0		0.3	2.0		MΩ
Input Capacitance				3.0			2.0		pF
Offset Voltage Adjustment Range				±25			±15		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	50 k	250 k		50 k	150 k		V/V
Output Resistance				100			75		Ω
Output Short-Circuit Current				±25			25		mA
Supply Current				1.9	2.8		1.9	2.8	mA
Power Consumption				60	85		60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.3			0.3		μs
	Overshoot			5.0			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2$ kΩ		0.5			0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.2			0.2		μs
	Overshoot			5.0			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \geq 2$ kΩ, $C_C = 3.5$ pF					5.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq 125°C$									
Input Offset Voltage		$R_S \leq 10$ kΩ		0.5	3.0		1.0	6.0	mV
Input Offset Current		T_A = HIGH			25		10	200	nA
		T_A = LOW			25		50	500	nA
Input Bias Current		T_A = HIGH			0.1		0.03	0.5	μA
		T_A = LOW			0.1		0.3	1.5	μA
Input Voltage Range			±12	±13		±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	80	95		70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		13	100		30	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	25 k			25 k			V/V
Output Voltage Swing		$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
		$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Supply Current		T_A = HIGH		1.5	2.5		1.5	2.5	mA
		T_A = LOW		2.0	3.3		2.0	3.3	mA
Power Consumption		T_A = HIGH		40	75		45	75	mW
		T_A = LOW		60	100		60	100	mW

μA748C
Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified.

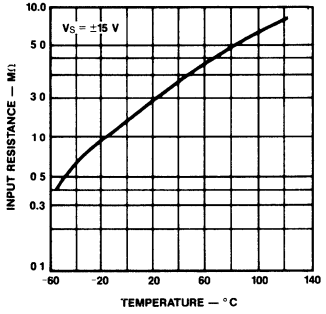
Characteristic		Condition	μA748C Min	Typ	Max	Unit
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				2.0		pF
Offset Voltage Adjustment Range				± 15		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	20 k	150 k		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \geq 2$ kΩ, $C_C = 3.5$ pF		5.5		V/μs
The following specification apply for $0°C \leq T_A \leq 70°C$						
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	7.5	mV
Input Offset Current		T_A = HIGH			300	nA
		T_A = LOW			800	μA
Input Voltage Range			± 12	± 13		V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	15,000			V/V
Output Voltage Swing		$R_L \geq 10$ kΩ	± 12	± 14		V
		$R_L \geq 2$ kΩ	± 10	± 13		V
Supply Current		T_A = HIGH		1.5	2.5	mA
		T_A = LO		2.0	3.3	mA
Power Consumption		T_A = HIGH		45	75	mW
		T_A = LO		60	100	mW

Typical Performance Curves for μA748

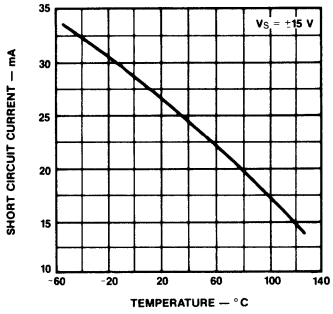
Input Bias Current as a Function of Ambient Temperature



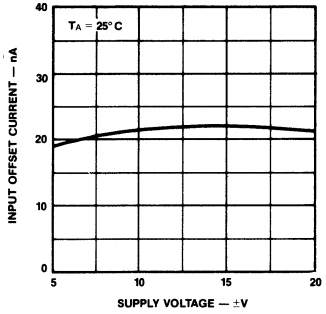
Input Resistance as a Function of Ambient Temperature



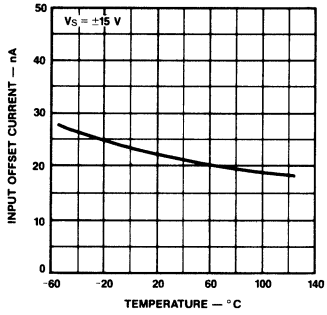
Output Short Circuit Current as a Function of Ambient Temperature



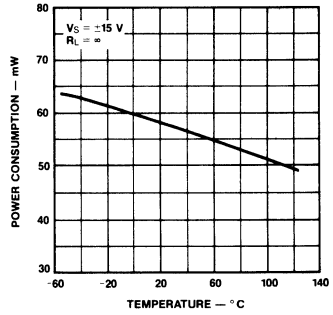
Input Offset Current as a Function of Supply Voltage



Input Offset Current as a Function of Ambient Temperature

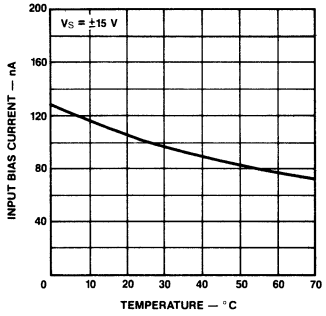


Power Consumption as a Function of Ambient Temperature

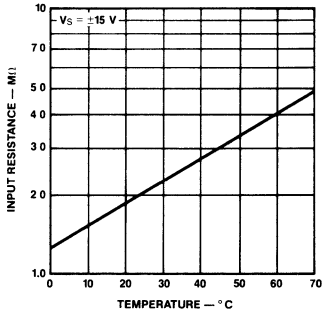


Typical Perfomance Curves for μA748C

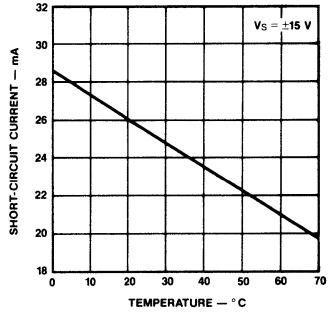
Input Bias Current as a Function of Ambient Temperature



Input Resistance as a Function of Ambient Temperature

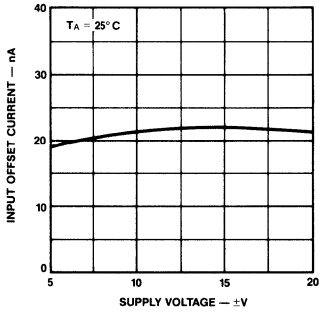


Output Short Circuit Current as a Function of Ambient Temperature

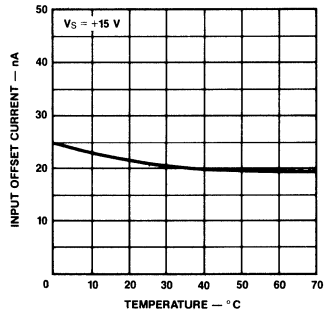


Typical Perfomance Curves for μA748C (Cont.)

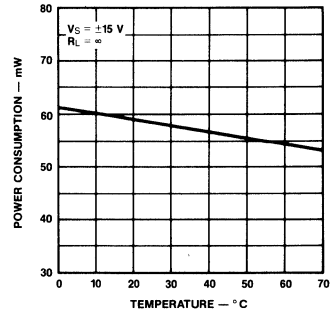
Input Offset Current as a Function of Supply Voltage



Input Offset Current as a Function of Ambient Temperature

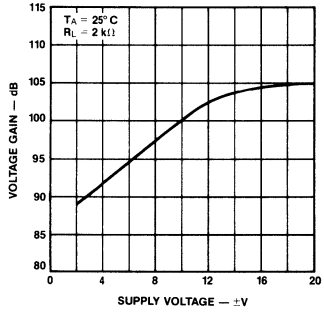


Power Consumption as a Function of Ambient Temperature

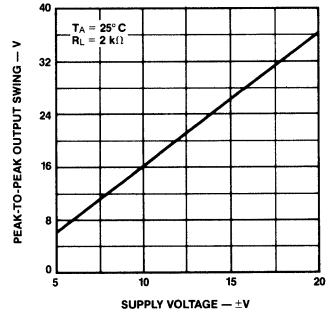


Typical Perfomance Curves for μA748 and μA748C

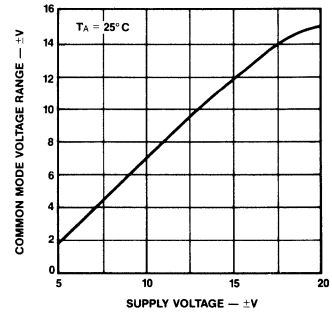
Open Loop Voltage Gain as a Function of Supply Voltage



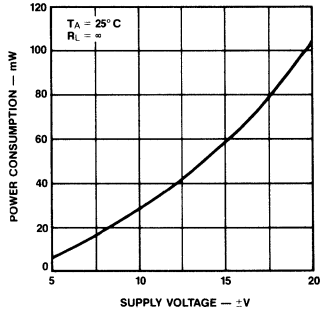
Output Voltage Swing as a Function of Supply Voltage



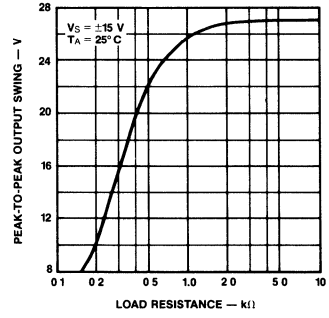
Input Common Mode Voltage Range as a Function of Supply Voltage



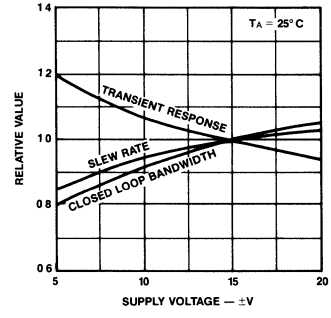
Power Consumption as a Function of Supply Voltage



Output Voltage Swing as a Function of Load Resistance

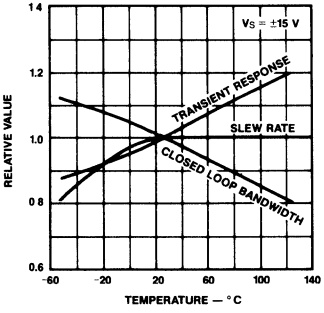


Frequency Characteristics as a Function of Supply Voltage

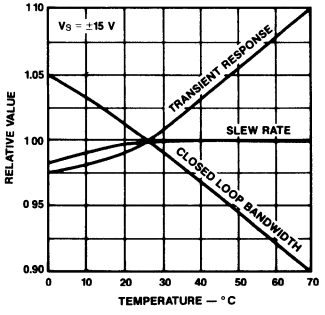


Typical Perfomance Curves for μA748 and μA748C (Cont.)

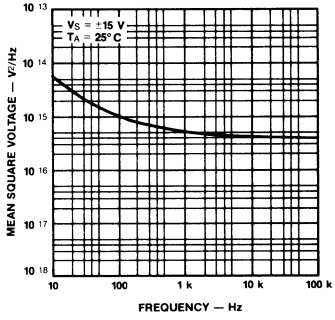
μA748 Frequency Characteristics as a Function of Ambient Temperature



μ748C Frequency Characteristics as a Function of Ambient Temperature

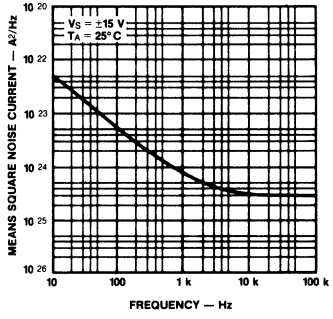


Input Noise Voltage as a Function of Frequency

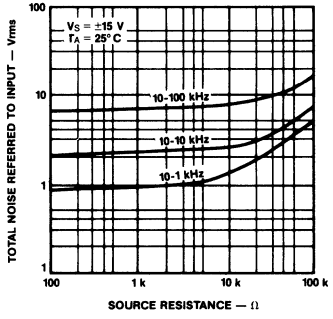


4

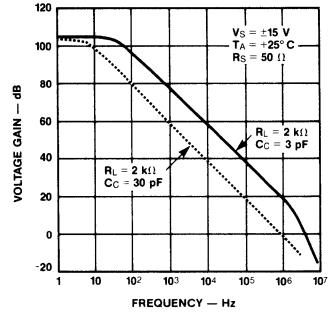
Input Noise Current as a Function of Frequency



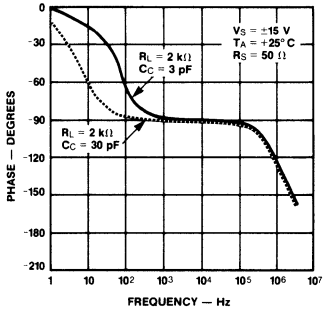
Broad Band Noise for Various Bandwidths



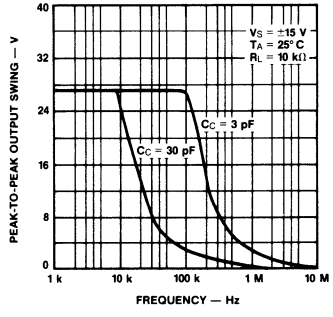
Open Loop Voltage Gain as a Function of Frequency



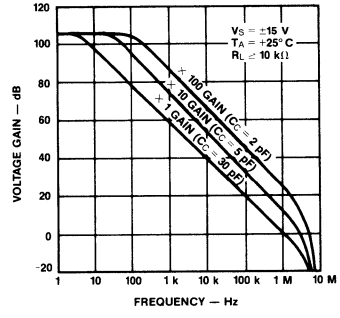
Open Loop Phase Response as a Function of Frequency



Output Voltage Swing as a Function of Frequency

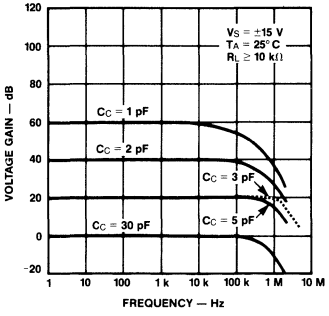


Open Loop Voltage Gain as a Function of Frequency for Various Gain/Compensation Options

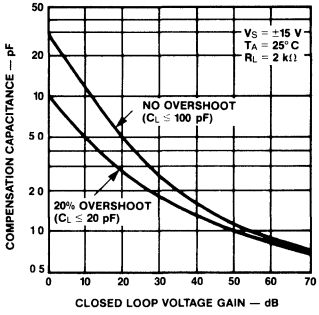


Typical Perfomance Curves for μA748 and μA748C (Cont.)

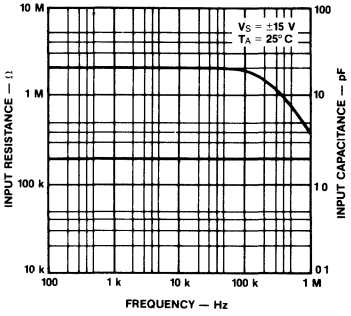
Frequency Response for Various Closed Loop Gains



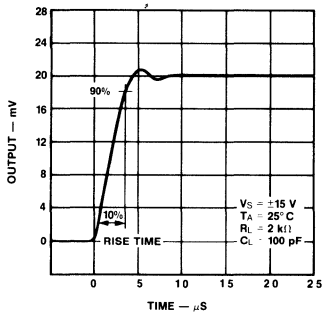
Compensation Capacitance as a Function of Closed Loop Voltage Gain



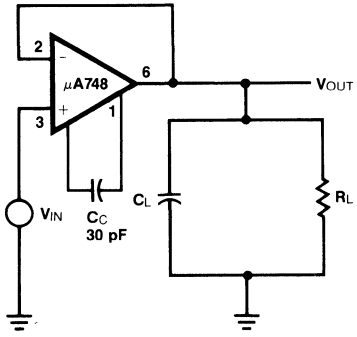
Input Resistance and Input Capacitance as a Function of Frequency



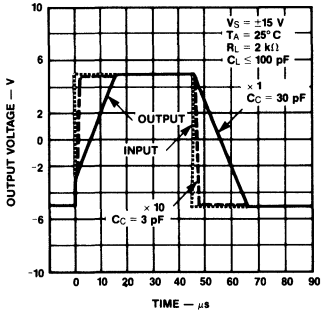
Voltage Follower Transient Response (Gain of 1)



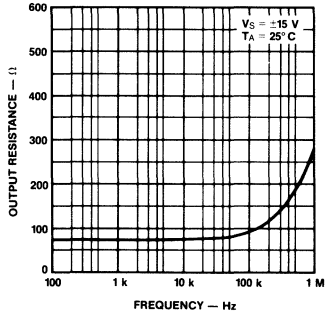
Transient Response Test Circuit



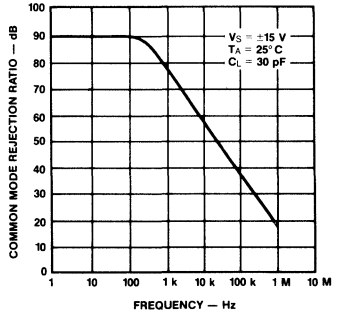
Voltage Follower Large-Signal Pulse Response



Output Resistance as a Function of Frequency

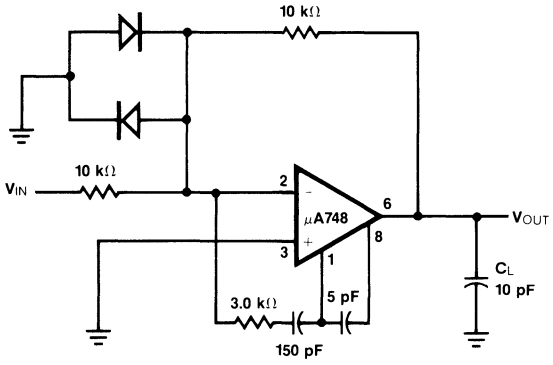


Common Mode Rejection Ratio as a Function of Frequency

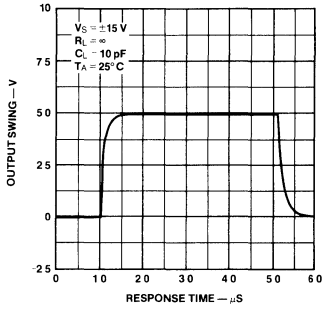


Typical Performance Curves for μA748 and μA748C (Cont.)

Feed Forward Compensation

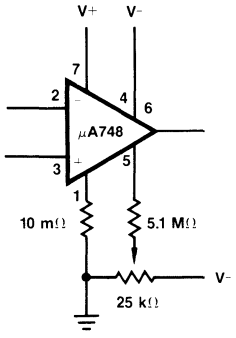


Large Signal Feed Forward Transient Response

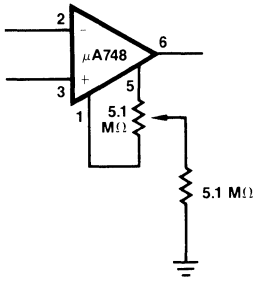


4

Voltage Offset Null Circuit



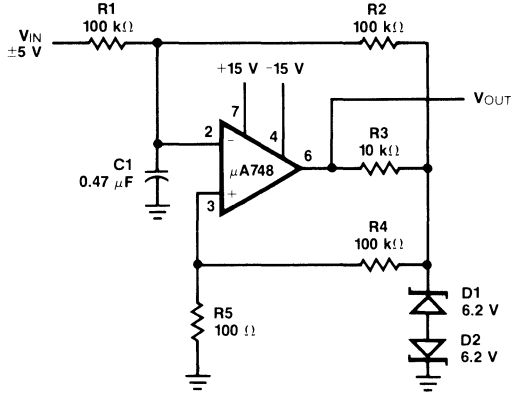
Suggested



Alternate

Typical Applications

Pulse Width Modulator



$$f_c = \frac{1}{2\pi R2\ C1}$$

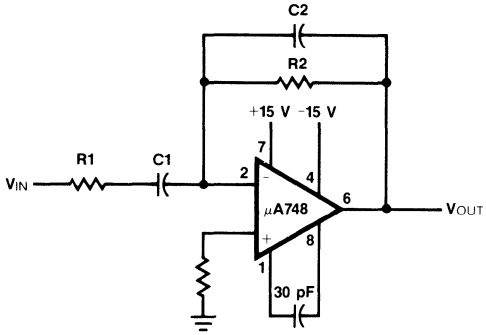
$$f_n = \frac{1}{2\pi R1\ C1}$$

$$= \frac{1}{2\pi R2\ C2}$$

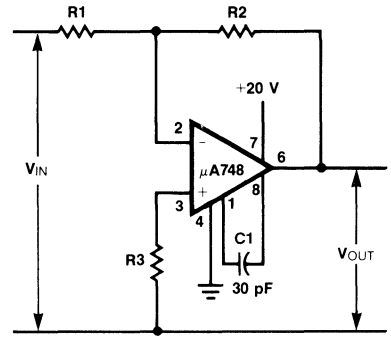
$$f_c < f_n < f_{unity\ gain}$$

Typical Applications (Cont.)

Practical Differentiator



Circuit for Operating the μA748 Without a Negative Supply



FAIRCHILD
A Schlumberger Company

μA759 Power Operational Amplifier

Linear Products

Description

The μA759 is a High Performance Monolithic Operational Amplifier constructed using the Fairchild Planar Epitaxial process. The amplifier provides 325 mA output current and features small signal characteristics better than the μA741. The amplifier is designed to operate from a single or dual power supply and the input common mode range includes the negative supply. The high gain and high output power provide superior performance whenever an operational amplifier is needed. The μA759 employs internal current limiting, thermal shutdown and safe-area compensation making it essentially indestructible. It is intended for a wide range of applications including voltage regulators, audio amplifiers, servo amplifiers and power drivers.

- **OUTPUT CURRENT—325 mA MINIMUM**
- **INTERNAL SHORT-CIRCUIT CURRENT LIMITING**
- **INTERNAL THERMAL-OVERLOAD PROTECTION**
- **INTERNAL OUTPUT TRANSISTORS SAFE-AREA PROTECTION**
- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**

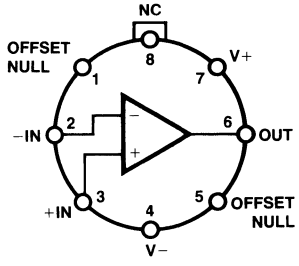
Absolute Maximum Ratings

Supply Voltage	
Between V+ and V−	36V
Differential Input Voltage (Note 1)	30 V
Input Voltage (Note 1)	(V− −0.3 V) to V+
Internal Power Dissipation (Note 2)	Internally Limited
Operating Junction Temperature Range	
Military (μA749)	−55°C to +150°C
Commercial (μA759C)	0°C to +125°C
Storage Temperature Range	
4-Pin Power Watt (U1)	−55°C to +150°C
8-Pin TO-99 (H)	−65°C to +150 °C
Pin Temperature	
4-Pin Power Watt (U1) (Soldering, 10 s)	260°C
8-Pin TO-99 (H) (Soldering, 60 s)	300°C

Notes

1. For a supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, use the thermal resistance values on page 3

Connection Diagram 8-Pin Metal Package



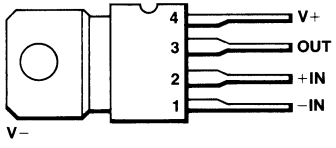
(Top View)

Pin 4 connected to case

Order Information

Type	Package	Code	Part No.
μA759	Metal	5W	μA759HM
μA759C	Metal	5W	μA759HC

Connection Diagram Power Watt Package



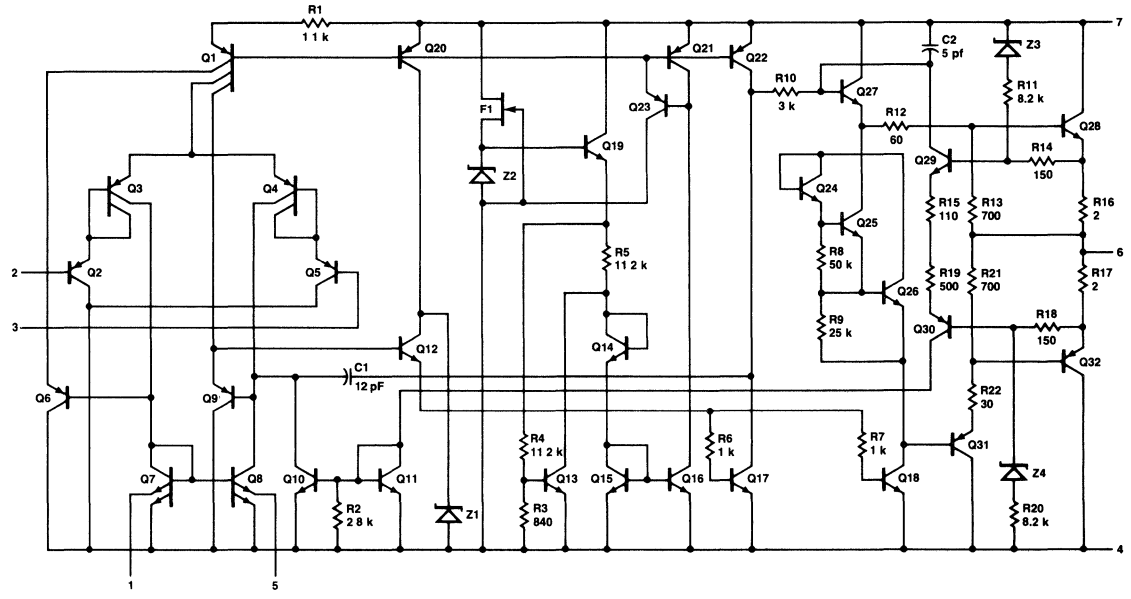
(Top View)

Order Information

Type	Package	Code	Part No.
μA759C	Power Watt	8Z	μA759U1C

4

Equivalent Circuit



Electrical Characteristics $V_S = \pm 15$ V, $T_J = 25°C$ unless otherwise specified

Characteristic		Condition	μA759 Min	μA759 Typ	μA759 Max	μA759C Min	μA759C Typ	μA759C Max	Unit
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	3.0		1.0	6.0	mV
Input Offset Current				5.0	30		5.0	50	nA
Input Bias Current				50	150		50	250	nA
Input Resistance			0.25	1.5		0.25	1.5		MΩ
Input Voltage Range			+13 to $-V_S$	+13 to $-V_S$		+13 to $-V_S$	+13 to $-V_S$		V
Large Signal Voltage Gain		$R_L \geq 50\ \Omega$, $V_{OUT} = \pm 10$ V	50 k	200 k		25 k	200 k		V/V
Supply Current				12	18		12	18	mA
Peak Output Current		$3\text{ V} \leq \lvert V_S - V_{OUT}\rvert < 10$ V	±325	±500		±325	±500		mA
Short Circuit Current		$\lvert V_S - V_{OUT}\rvert = 30$ V		±200			±200		mA
Transient Response (Unity Gain)	Risetime	$R_L \geq 50\ \Omega$		300			300		ns
	Overshoot	$R_L \geq 50\ \Omega$		5.0			10		%
Slew Rate		$R_L \geq 50\ \Omega$		0.6			0.5		V/μs
Unity Gain Bandwidth				1.0			1.0		MHz
The following specifications apply for $-55°C \leq T_J \leq 150°C$ (μA759), or $0° \leq T_J \leq 125°C$ (μA759C)									
Input Offset Voltage		$R_S \leq 10$ kΩ			4.5			7.5	mV
Input Offset Current					60			100	nA
Input Bias Current					300			400	nA
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	80	100		70	100		dB
Power Supply Rejection Ratio		$R_S \leq 10$ kΩ	80	100		80	100		dB
Large Signal Voltage Gain		$R_L \geq 50\ \Omega$, $V_{OUT} = \pm 10$ V	25 k	200 k		25 k	200 k		V/V
Output Voltage Swing		$R_L \geq 50\ \Omega$	±10	±12.5		±10	±12.5		V

Package	Type	Max	Typ	Max
	θ_{JC} °C/W	θ_{JC} °C/W	θ_{JA} °C/W	θ_{JA} °C/W
Power Watt (U1)	8.0	12	75	80
Metal Can (H)	30	40	120	185

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

(Without a heat sink)

$\theta_{CA} = \theta_{CS} + \theta_{SA}$

Solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where:
- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JA} = Junction to ambient thermal resistance
- θ_{JC} = Junction to case thermal resistance
- θ_{CA} = Case to ambient thermal resistance
- θ_{CS} = Case to heat sink thermal resistance
- θ_{SA} = Heat sink to ambient thermal resistance

Mounting Hints

Metal Can Package (μA759HC/μA759HM)

The μA759 in the 8-Pin TO-99 metal can package must be used with a heat sink. With ± 15 V power supplies, the μA759 can dissipate up to 540 mW in its quiescent (no load) state. This would result in a 100°C rise in chip temperature to 125°C (assuming a 25°C ambient temperature). In order to avoid this problem, it is advisable to use either a slip on or stud mount heat sink with this package. If a stud mount heat sink is used, it may be necessary to use insulating washers between the stud and the chassis because the case of the μA759 is internally connected to the negative power supply terminal.

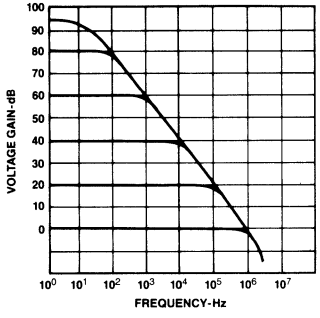
Power Watt Package (μA759U1C)

The μA759U1C is designed to be attached by the tab to a heat sink. This heat sink can be either one of the many heat sinks which are commercially available, a piece of metal such as the equipment chassis, or a suitable amount of copper foil as on a double sided PC board. The important thing to remember is that the negative power supply connection to the op amp must be made through the tab. Furthermore, adequate heat sinking must be provided to keep the chip temperature below 125°C under worst case load and ambient temperature conditions.

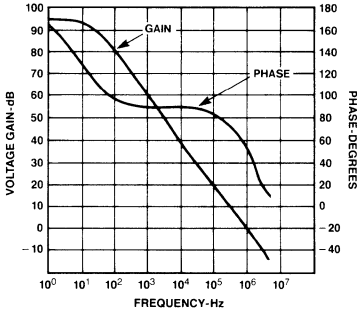
4

Typical Performance Curves

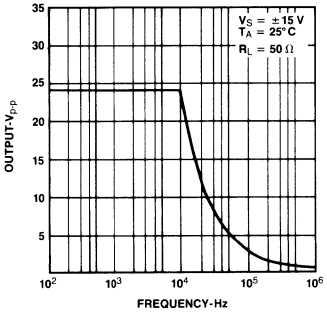
Frequency Response at Various Closed Loop Gain Settings



Open Loop Gain and Phase Response as a Function of Frequency

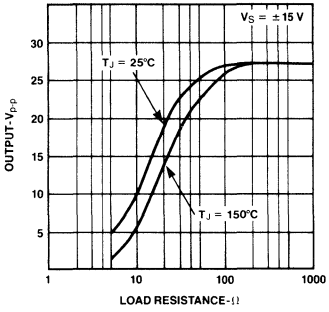


Output Voltage as a Function of Frequency

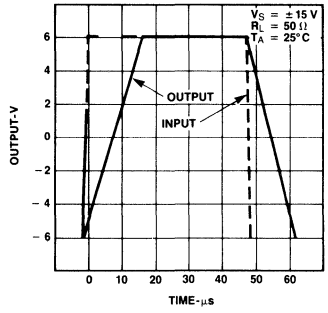


Typical Performance Curves (Cont.)

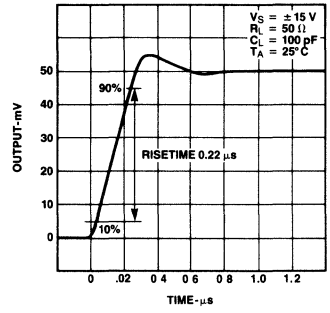
P-P Output Voltage as a Function of Load Resistance



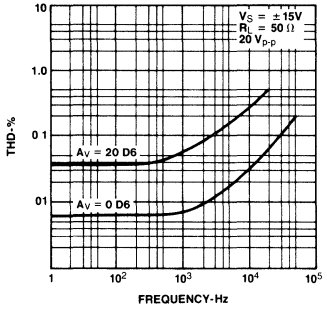
Voltage Follower Large Signal Pulse Response



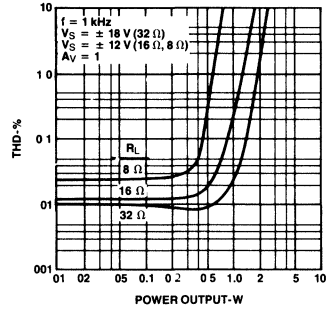
Voltage Follower Transient Response



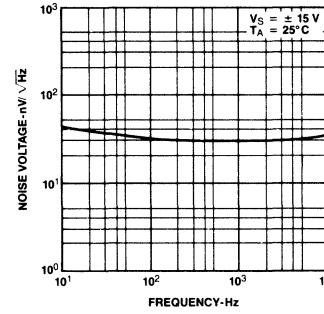
Total Harmonic Distortion as a Function of Frequency



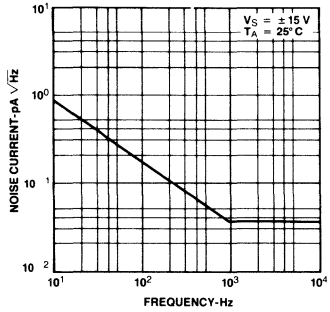
Total Harmonic Distortion as a Function of Power Output



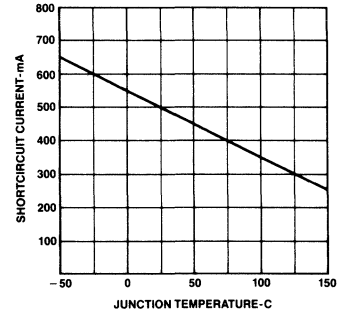
Input Noise Voltage as a Function of Frequency



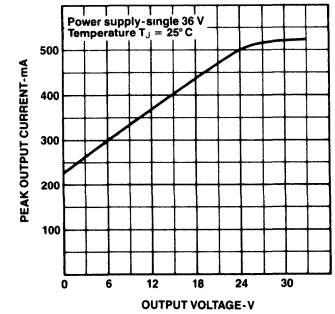
Noise Current as a Function of Frequency



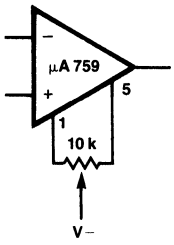
Output Short Circuit Current as a Function of Junction Temperature



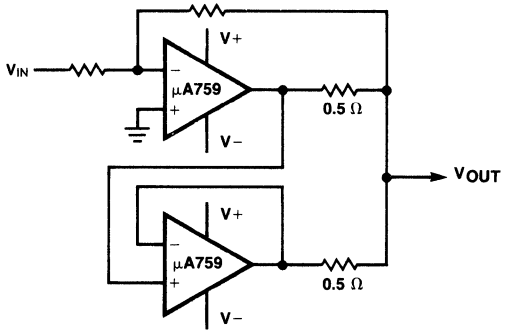
Peak Output Current as a Function of Output Voltage



Offset Null Circuit

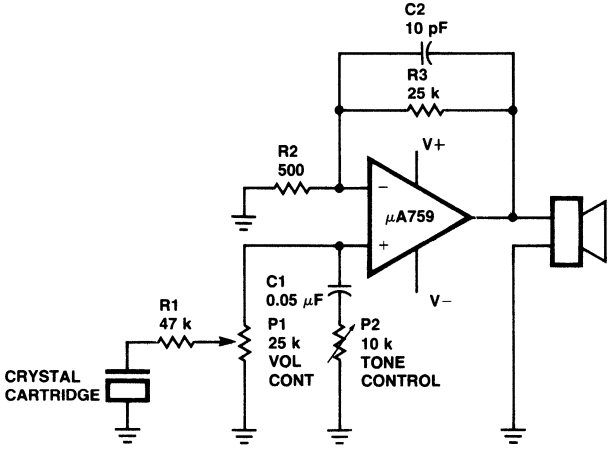


Paralleling μA759 Power OP Amps



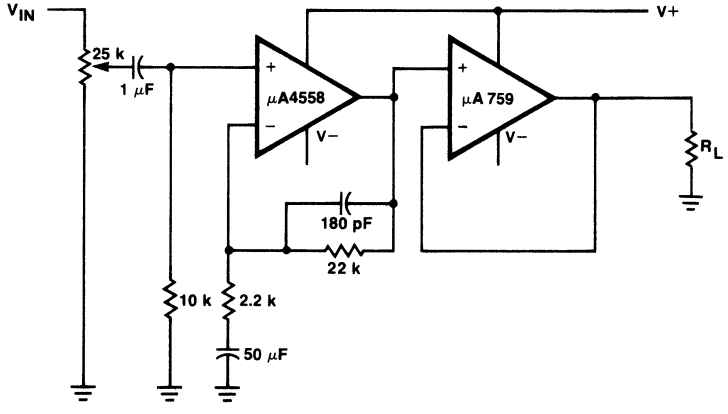
Audio Applications

Low Cost Phono Amplifier

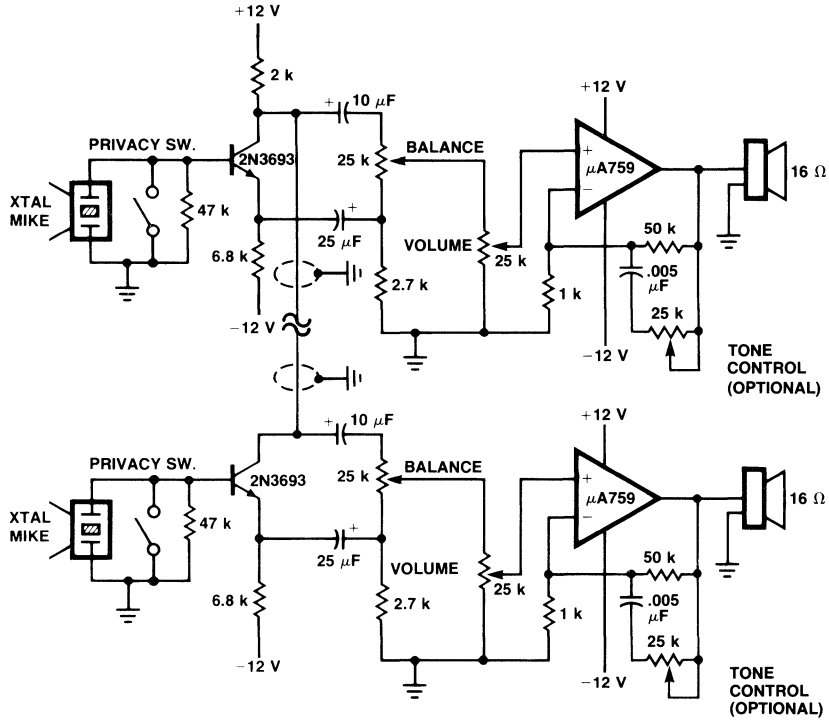


Speaker Impedance (ohms)	Output Power (watts)	Min Supply (volts)	V_{out}p-p (volts)
4	.18	9	2.4
8	.36	12	4.8
16	.72	15	9.6
32	1.44	25	19.2

Headphone Amplifier



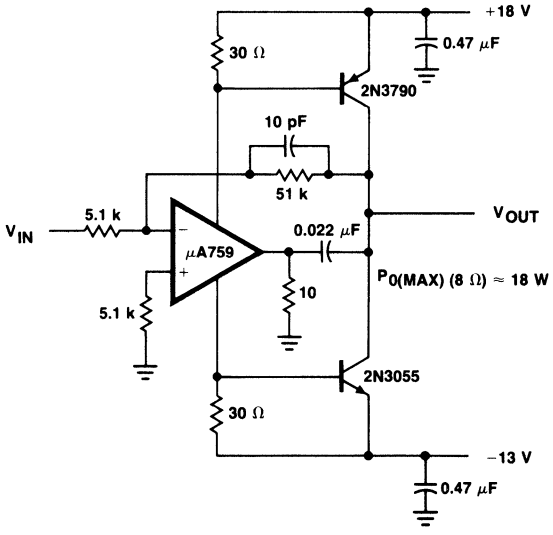
Bidirectional Intercom System Using the μA759 Power OP Amp



Features

- Circuit Simplicity
- 1 Watt of Audio Output
- Duplex operation with only one two-wire cable as interconnect.

High Slew Rate Power OP Amp/Audio Amp

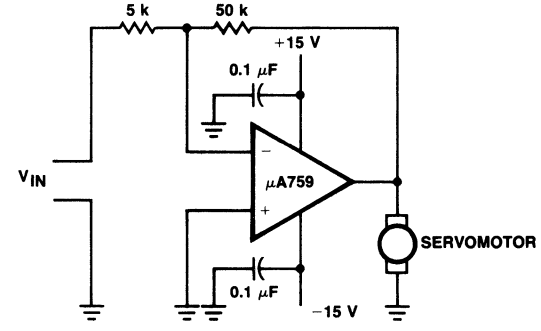


Features
- High Slew Rate 9 V/μs
- High 3 dB Power Bandwidth 85 kHz
- 18 Watts Output Power Into an 8 Ω Load.
- Low Distortion — .2%, 10 VRMS, 1 kHz Into 8 Ω

Design Consideration
- $A_V \geq 10$

Servo Applications

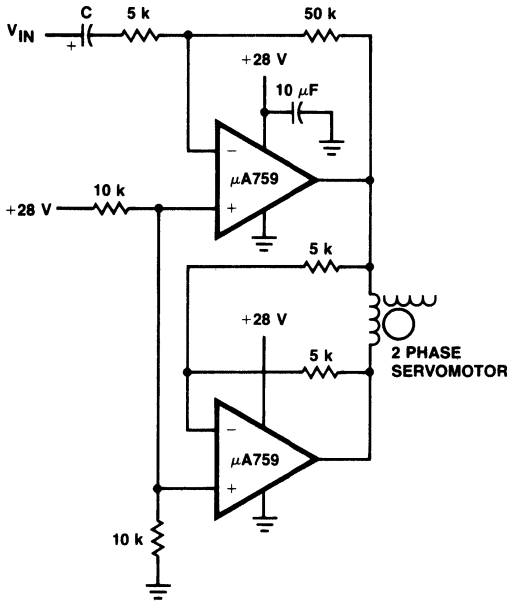
DC Servo Amplifiers



Features
- Circuit Simplicity
- One Chip Means Excellent Reliability

Design Considerations
- $I_{OUT} \leq 325$ mA

AC Servo Amplifier – Bridge Type



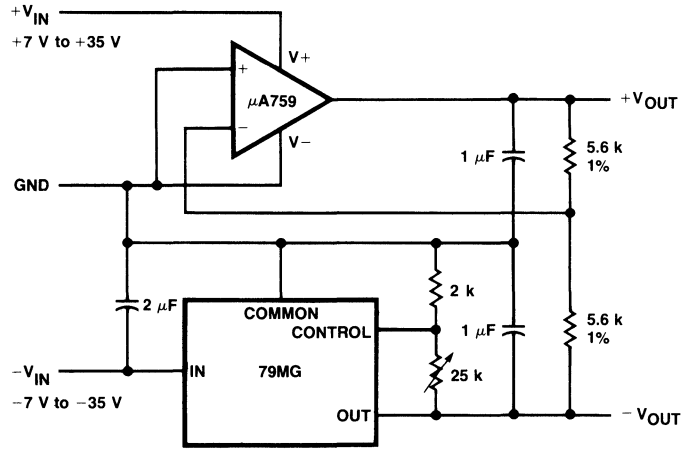
Features
- Gain of 10
- Use of μA759 Means Simple Inexpensive Circuit

Design Considerations
- 325 mA Max Output Current

4

Regulator Applications

Adjustable Dual Tracking Regulator

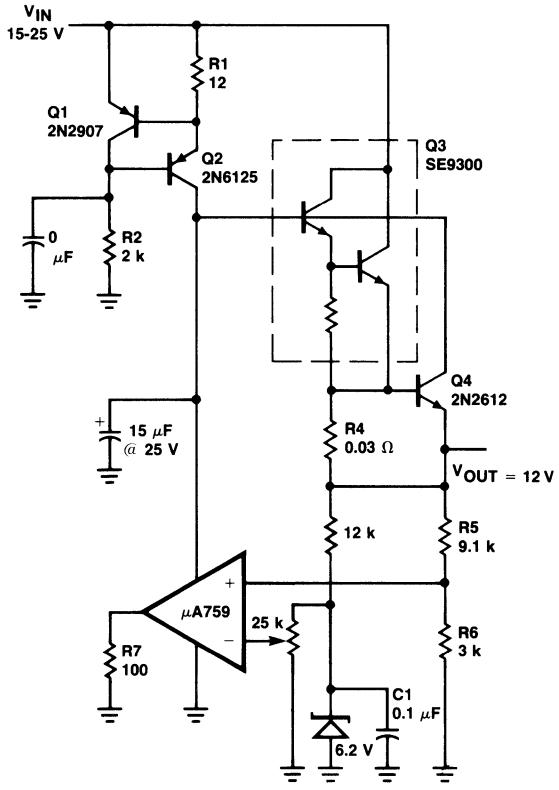


Features

- Wide Output Voltage Range (±2.2 to ±30 V)
- Excellent Load Regulation $\Delta V_{OUT} < \pm 5$ mV for $\Delta I_{OUT} = \pm 0.2$ A
- Excellent Line Regulation $\Delta_{OUT} < \pm 2$ mV for $\Delta V_{IN} = 10$ V

Regulator Applications (Con't)

10 Amp – 12 Volt Regulator



Features

- Excellent Load and Line Regulation
- Excellent Temperature Coefficient-Depends Largely on Tempco of the Reference Zener

FAIRCHILD

A Schlumberger Company

μA771 • μA772 • μA774 Operational Amplifier Family

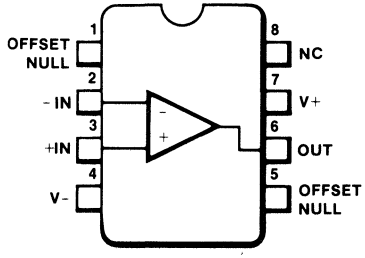
Linear Products

Description

These monolithic JFET Input Operational Amplifiers incorporate well-matched ion-implanted JFETS on the same chip with standard bipolar transistors. The key features of these op amps are low input bias currents in the sub nanoamp range plus high slew rate (13 V/μs typically) and wide bandwidth (3.0 MHz typically).

- **LOW INPUT BIAS CURRENT—200 pA**
- **LOW INPUT OFFSET CURRENT—100 pA**
- **HIGH SLEW RATE—13 V/μs TYPICALLY**
- **WIDE BANDWIDTH—3.0 MHz TYPICALLY**

μA771 Connection Diagram
8-Pin DIP

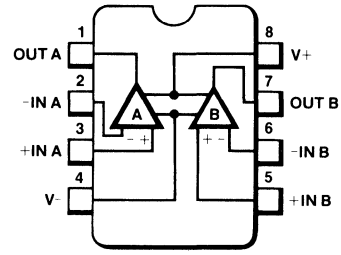


(Top View)

Order Information

Type	Package	Code	Part No.
μA771AM	Ceramic	6T	μA771ARM
μA771BM	Ceramic	6T	μA771BRM
μA771A	Ceramic	6T	μA771ARC
μA771B	Ceramic	6T	μA771BRC
μA771	Ceramic	6T	μA771RC
μA771A	Molded	9T	μA771ATC
μA771B	Molded	9T	μA771BTC
μA771	Molded	9T	μA771TC
μA771L	Ceramic	6T	μA771LRC
μA771L	Molded	9T	μA771LTC

μA772 Connection Diagram
8-Pin DIP

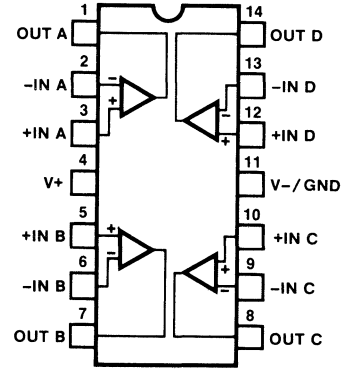


(Top View)

Order Information

Type	Package	Code	Part No.
μA772AM	Ceramic	6T	μA772ARM
μA772BM	Ceramic	6T	μA772BRM
μA772A	Ceramic	6T	μA772ARC
μA772B	Ceramic	6T	μA772BRC
μA772	Ceramic	6T	μA772RC
μA772A	Molded	9T	μA772ATC
μA772B	Molded	9T	μA772BTC
μA772	Molded	9T	μA772TC

μA774 Connection Diagram
14-Pin DIP



(Top View)

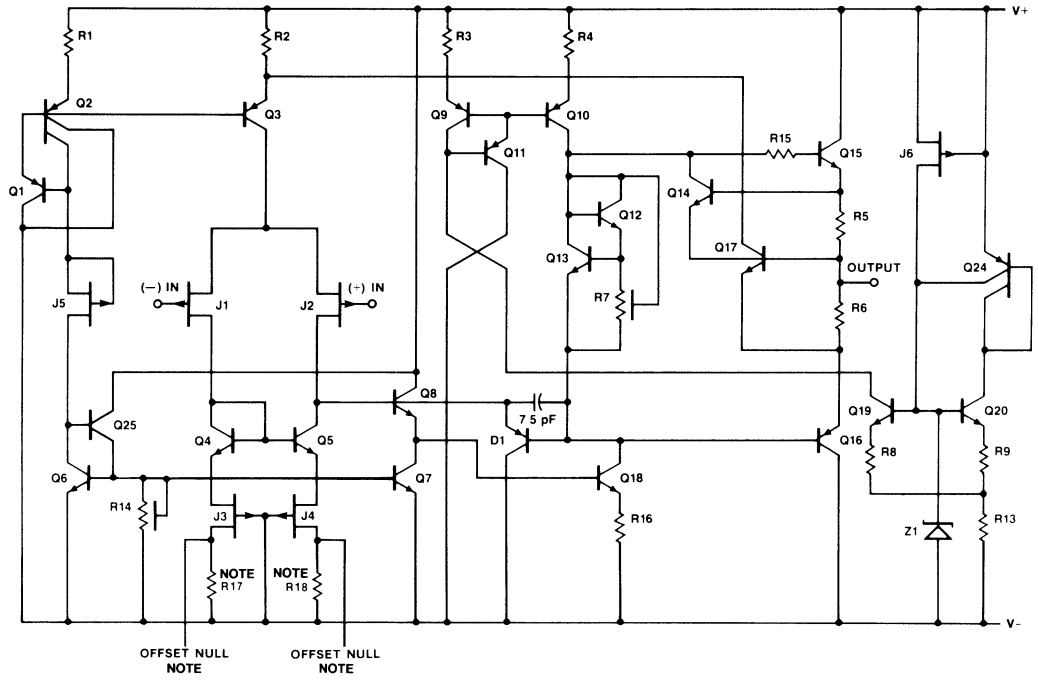
Order Information

Type	Package	Code	Part No.
μA774L	Ceramic	6A	μA774LDC
μA774L	Molded	9A	μA774LPC

Absolute Maximum Ratings

Supply Voltage	± 18 V	Operating Temperature Range	
Internal Power Dissipation		Commercial	
(Note 1)		μAF77XA, μAF77XB,	
Ceramic DIP	670 mW	μAF77X, μAF77XL	0°C to +70°C
Molded DIP Package	310 mW	Military	
Differential Input Voltage	± 30 V	μAF77XAM, μAF77XBM	−55°C to +125°C
Input Voltage Range (Note 2)	± 16 V	Pin Temperature	
Output Short-Circuit Duration	continuous	Molded DIP (Soldering, 10 s)	260°C
Storage Temperature Range		Ceramic DIP (Soldering, 60 s)	300°C
Ceramic	−65°C to +150°C		
Molded	−55°C to +125°C		

Equivalent Circuit



Note

μA771 only

Notes

1. Rating applies to ambient temperatures up to 70°C above T_A = 70°C 5.6 mW/°C for the mini DIP and 8.3 mW/°C for the DIP
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

DC Electrical Characteristics—Commercial Grade Devices

Symbol	Characteristic	Condition	μA77X			μA77XL			Unit
			Min	Typ	Max	Min	Typ	Max	
The Following Specifications Apply for $V_S = \pm 15$ V, $T_A = 25°C$									
V_{OS}	Input Offset Voltage	(Note 3) $R_S = 10\ k\Omega$			10.0			15.0	mV
I_{OS}	Input Offset Current	(Notes 3, 4) $T_j = 25°C$			100			100	pA
I_B	Input Bias Current	(Notes 3, 4) $T_j = 25°C$		50	200		50	200	pA
R_{IN}	Input Resistance			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V $R_L = 2\ k\Omega$	50	100		50	100		V/mV
I_{SC}	Short Circuit Current			25			25		mA
I_S	Supply Current	Per Amplifier			2.8			2.8	mA
The Following Specifications Apply for $V_S = \pm 15$ V, $0°C \leq T_A$ 70°C									
V_{OS}	Input Offset Voltage	(Note 3) $R_S = 10\ k\Omega$			13			20	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10			10		μV/°C
I_{OS}	Input Offset Current	(Notes 3, 4)			4.0			4.0	nA
I_B	Input Bias Current	(Notes 3, 4)			8.0			8.0	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	25			25			V/mV
V_O	Output Voltage Swing	$R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10			±12 ±10			V V
V_{CM}	Input Common Mode Voltage Range		±11	+15 −12		±11	+15 −12		V
CMRR	Common Mode Rejection Ratio	$R_S = 10\ k\Omega$	70			70			dB
PSRR	Supply Voltage Rejection Ratio	$R_S = 10\ k\Omega$	70			70			dB
I_S	Supply Current	Per Amplifier			3.0			3.0	mA

Notes

3 V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

4. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D $T_j = T_A = \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

5 Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

DC Electrical Characteristics—Commercial Grade Devices

Symbol	Characteristic	Condition	μA77XA			μA77XB			Unit
			Min	Typ	Max	Min	Typ	Max	
The Following Specifications Apply for $V_S = \pm 15$ V, $T_A = 25°C$									
V_{OS}	Input Offset Voltage	(Note 3) $R_S = 10\ k\Omega$			2.0			5.0	mV
I_{OS}	Input Offset Current	(Notes 3, 4) $T_j = 25°C$			50			50	pA
I_B	Input Bias Current	(Notes 3, 4) $T_j = 25°C$		50	100		50	100	pA
R_{IN}	Input Resistance			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V $R_L = 2\ k\Omega$	50	100		50	100		V/mV
I_{SC}	Short Circuit Current			25			25		mA
I_S	Supply Current	Per Amplifier			2.8			2.8	mA
The Following Specifications Apply for $V_S = \pm 15$ V, $0°C \leq T_A$ 70°C									
V_{OS}	Input Offset Voltage	(Note 3) $R_S = 10\ k\Omega$			4.0			7.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10			10		μV/°C
I_{OS}	Input Offset Current	(Notes 3, 4)			2.0			2.0	nA
I_B	Input Bias Current	(Notes 3, 4)			4.0			4.0	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L = 2\ k\Omega$	25			25			V/mV
V_O	Output Voltage Swing	$R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10			±12 ±10			V V
V_{CM}	Input Common Mode Voltage Range		±11	+15 −12		±11	+15 −12		V
CMRR	Common Mode Rejection Ratio	$R_S = 10\ k\Omega$	80			80			dB
PSRR	Supply Voltage Rejection Ratio	$R_S = 10\ k\Omega$	80			80			dB
I_S	Supply Current	Per Amplifier			3.0			3.0	mA

Notes

3 V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$

4 The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j Due to limited production test time, the input bias currents measured are correlated to junction temperature In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D $T_j = T_A = \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient Use of a heat sink is recommended if input bias current is to be kept to a minimum

5 Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice

DC Electrical Characteristics—Military Grade Devices

Symbol	Characteristic	Condition	μA77XAM			μA77XBM			Unit
			Min	Typ	Max	Min	Typ	Max	
The Following Specifications Apply for $V_S = \pm 15$ V, $T_A = 25°C$									
V_{OS}	Input Offset Voltage	$R_S = 10$ kΩ (Note 3)			2.0			5.0	mV
I_{OS}	Input Offset Current	(Notes 3, 4) $T_j = 25°C$			50			50	pA
I_B	Input Bias Current	(Notes 3, 4) $T_j = 25°C$		50	100		50	100	pA
R_{IN}	Input Resistance			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L = 2$ kΩ	50			50			V/mV
V_O	Output Voltage Swing	$R_L = 10$ kΩ $R_L = 2$ kΩ	±12 ±10			±12 ±10			V V
V_{CM}	Input Common Mode Voltage Range		±11	+15 −12		±11	+15 −12		V
CMRR	Common Mode Rejection Ratio	$R_S = 10$ kΩ	80			80			dB
PSRR	Supply Voltage Rejection Ratio	$R_S = 10$ kΩ	80			80			dB
I_S	Supply Current	Per Amplifier			2.8			2.8	mA
The Following Specifications Apply for $V_S = \pm 15$ V, $-55°C \leq T_A$ 125°C									
V_{OS}	Input Offset Voltage	$R_S = 10$ kΩ (Note 3)			5.0			8.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10$ kΩ		10			10		μV°/C
I_{OS}	Input Offset Current	(Notes 3, 4)			20			20	nA
I_B	Input Bias Current	(Notes 3, 4)			50			50	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V $R_L = 2$ kΩ	25			25			V/mV
V_O	Output Voltage Swing	$R_L = 10$ kΩ $R_L = 2$ kΩ	±12 ±10			±12 ±10			V V
CMRR	Common Mode Rejection Ratio	$R_S = 10$ kΩ	80			80			dB
PSRR	Supply Voltage Rejection Ratio	$R_S = 10$ kΩ	80			80			dB
I_S	Supply Current	Per Amplifier			3.4			3.4	mA

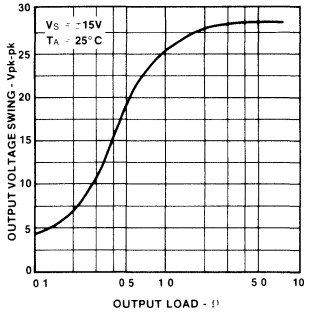
Commercial and Military
AC Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$

Symbol	Characteristic	Condition	All Grades			Unit
			Min	Typ	Max	
SR	Slew Rate	*(Figure 1)*		13		V/μs
GBW	Gain Bandwidth Product	*(Figure 2)*		3.0		MHz
e_n	Equivalent Input Noise Voltage	$R_S = 100$ Ω, f = 1000 Hz		16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

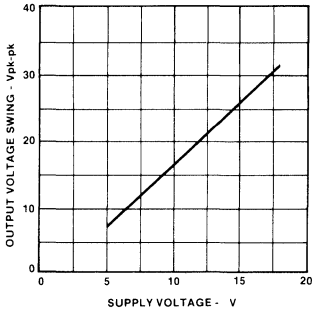
Notes on preceding page

Typical Performance Curves

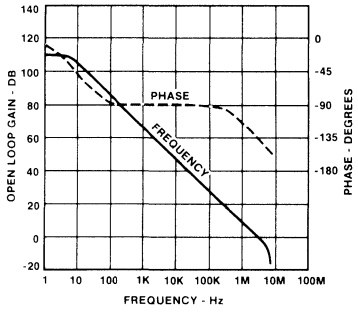
Output Voltage Swing vs. Load Resistance



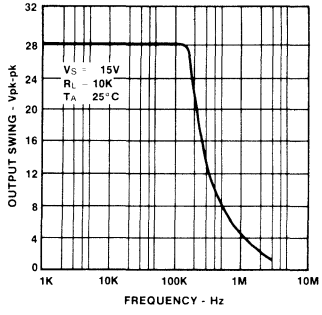
Output Voltage Swing vs. Supply Voltage



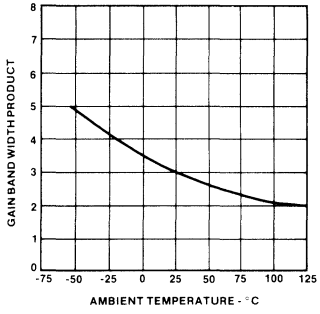
Open Loop Frequency Response



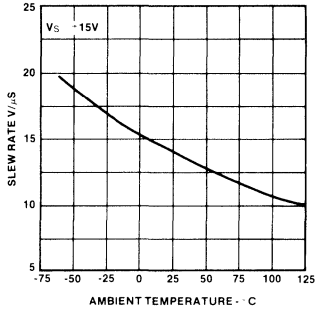
Maximum Undistorted Output vs. Frequency



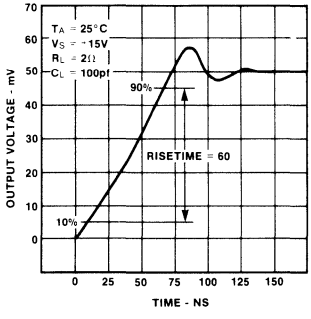
Gain Bandwidth Product vs. Temperature



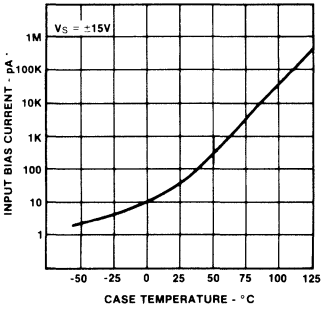
Slew Rate vs. Temperature



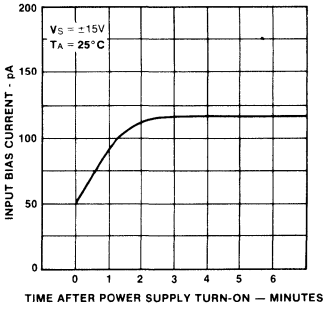
Small Signal Pulse Response



Input Bias Current vs. Temperature



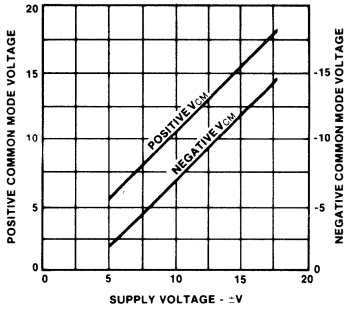
Bias Current Warm-up Change



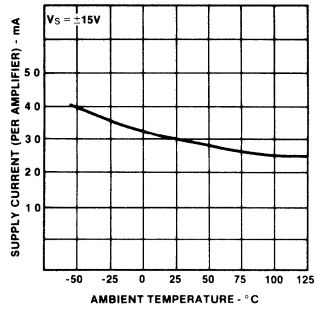
4

Typical Performance Curves (Cont.)

Maximum Common Mode Input Voltage vs. Supply Voltage

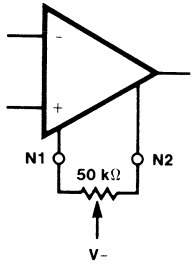


Supply Current vs. Temperature



Test Circuit

Input Offset Voltage Null Circuit (μA771 only)



Typical Applications

Fig. 1. Unity Gain Amplifier

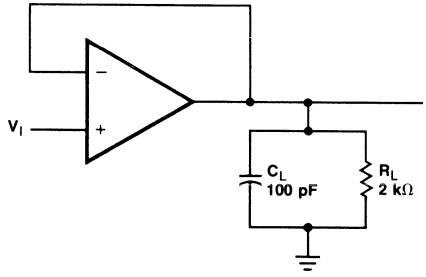
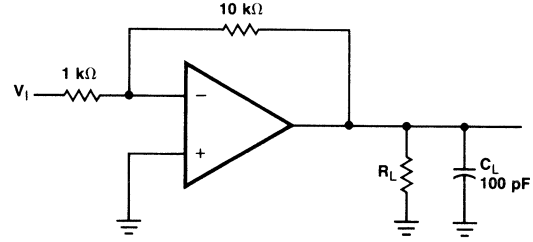


Fig. 2. Gain-of-10 Inverting Amplifier



FAIRCHILD

A Schlumberger Company

μA776 Multi-Purpose Programmable Op Amp

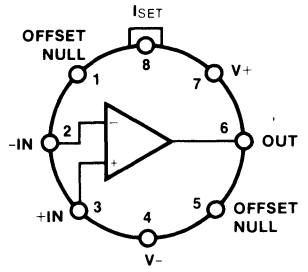
Linear Products

Description

The μA776 Programmable Operational Amplifier is constructed using the Fairchild Planar epitaxial process. High input impedance, low supply currents, and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics result in an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input noise voltage and current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano watt power consumption or for characteristics similar to the μA741. Internal frequency compensation, absence of latch-up, high slew rate and short circuit current protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

- **MICROPOWER CONSUMPTION**
- **± 1.2 V to ± 18 V OPERATION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **LOW INPUT BIAS CURRENTS**
- **WIDE PROGRAMMING RANGE**
- **HIGH SLEW RATE**
- **LOW NOISE**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET NULL CAPABILITY**
- **NO LATCH-UP**

Connection Diagram
8-Pin Metal Package

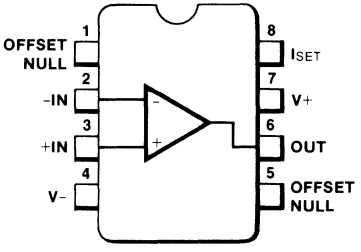


(Top View)

Order Information

Type	Package	Code	Part No.
μA776	Metal	5 W	μA776HM
μA776C	Metal	5 W	μA776HC

Connection Diagram
8-Pin DIP



(Top View)

Order Information

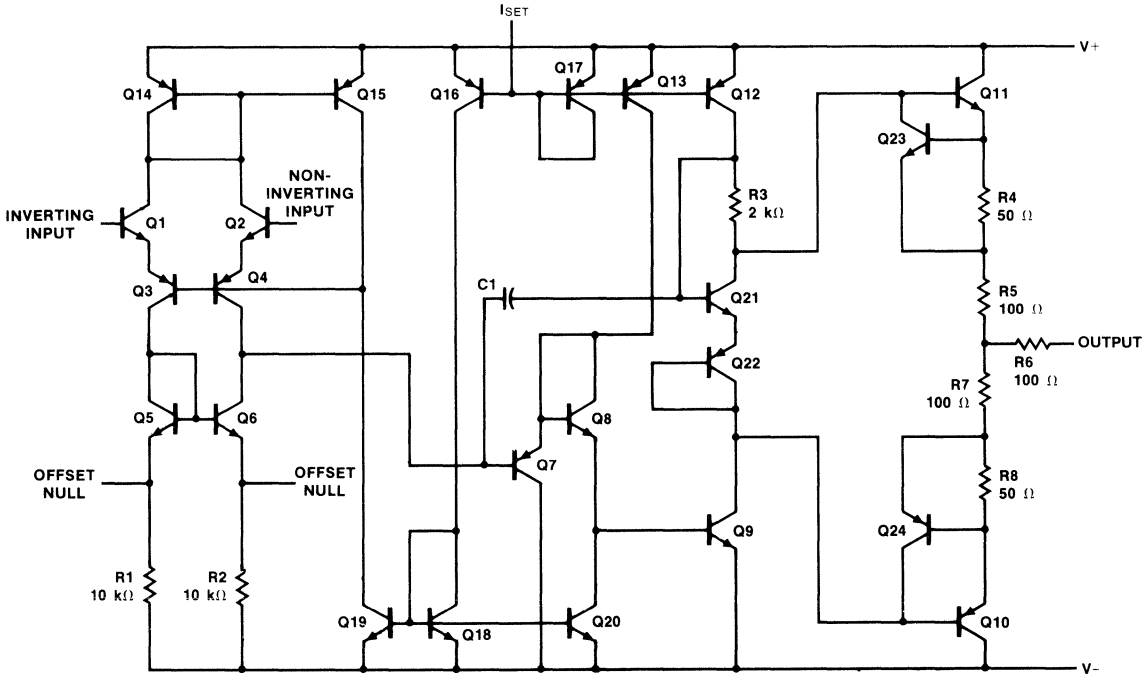
Type	Package	Code	Part No.
μA776C	Molded DIP	9T	μA776TC

4

Absolute Maximum Ratings

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage Between Offset Null and V−	±0.5 V
I_{SET} (Maximum Current at I_{SET})	500 μA
V_{SET} (Maximum Voltage to Ground at I_{SET})	$(V+ - 2.0\ V) \leq V_{SET} \leq V+$
Storage Temperature	
Metal Package	−65°C to +150°C
DIP	−55°C to +125°C
Operating Temperature	
Military (μA776)	−55°C to +125°C
Commercial (μA776C)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Package (60 s)	300°C
DIP (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

Equivalent Circuit



Notes

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for the DIP, and 5.6 mW/°C for the Mini DIP
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short Circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for $I_{SET} \leq 30$ μA.

± 15 V Operation for μA776
Electrical Characteristics T_A = 25°C, unless otherwise specified.

Characteristic		Condition	I_{SET} = 1.5 μA			I_{SET} = 15 μA			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	5.0		2.0	5.0	mV
Input Offset Current		$R_S \leq 10$ kΩ		0.7	3.0		2.0	15	nA
Input Bias Current				2.0	7.5		15	50	nA
Input Resistance				50			5.0		mΩ
Input Capacitance				2.0			2.0		pF
Offset Voltage Adjustment Range				9.0			18		mV
Large Signal Voltage Gain		$R_L \geq 75$ kΩ, V_{OUT} = ± 10 V	200 k	400 k					V/V
		$R_L \geq 5$ kΩ, V_{OUT} = ± 10 V				100 k	400 k		V/V
Output Resistance				5.0 k			1.0 k		Ω
Output Short-Circuit Current				3.0			12		mA
Supply Current				20	25		160	180	μA
Power Consumption					0.75			5.4	mW
Transient Response (unity gain)	Rise Time	V_{IN} = 20 mV, $R_L \geq 5$ kΩ, C_L = 100 pF		1.6			0.35		μs
	Overshoot			0			10		%
Slew Rate		$R_L \geq 5$ kΩ		0.1			0.8		V/μs
Output Voltage Swing		$R_L \geq 75$ kΩ	± 12	± 14					V
		$R_L \geq 5$ kΩ				± 10	± 13		V
The following specifications apply −55°C ≤ T_A ≤ +125°C									
Input Offset Voltage		$R_S \leq 10$ kΩ			6.0			6.0	mV
Input Offset Current		T_A = +125°C			5.0			15	nA
		T_A = −55°C			10			40	nA
Input Bias Current		T_A = +125°C			7.5			50	nA
		T_A = −55°C			20			120	nA
Input Voltage Range			± 10			± 10			V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		25	150		25	150	μV/V
Large Signal Voltage Gain		$R_L \geq 75$ kΩ, V_{OUT} = ± 10 V	100 k			75 k			V/V
Output Voltage Swing		$R_L \geq 75$ kΩ	± 10			± 10			V
Supply Current					30			200	μA
Power Consumption					0.9			6.0	mW

±3 V Operation For μA776
Electrical Characteristics T_A = 25°C, unless otherwise specified.

Characteristic		Condition	I_{SET} = 1.5 μA			I_{SET} = 15 μA			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	5.0		2.0	5.0	mV
Input Offset Current				0.7	3.0		2.0	15	nA
Input Bias Current				2.0	7.5		15	50	nA
Input Resistance				50			5.0		MΩ
Input Capacitance				2.0			2.0		pF
Offset Voltage Adjustment Range				9.0			18		mV
Large Signal Voltage Gain		$R_L \geq 75$ kΩ, $V_{OUT} = \pm 1$ V	50 k	200 k					V/V
		$R_L \geq 5$ kΩ, $V_{OUT} = \pm 1$ V				50 k	200 k		V/V
Output Resistance				5.0 k			1.0 k		Ω
Output Short-Circuit Current				3.0			5.0		mA
Supply Current				13	20		130	160	μA
Power Consumption				78	120		780	960	μW
Transient Response (unity gain)	Rise Time	V_{IN} = 20 mV, $R_L \geq 5$ kΩ, C_L = 100 pF		3.0			0.6		μs
	Overshoot			0			5		%
Slew Rate		$R_L \geq 5$ kΩ		0.03			0.35		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$									
Input Offset Voltage		$R_S \leq 10$ kΩ			6.0			6.0	mV
Input Offset Current		$T_A = +125°C$			5.0			15	nA
		$T_A = -55°C$			10			40	nA
Input Bias Current		$T_A = +125°C$			7.5			50	nA
		$T_A = -55°C$			20			120	nA
Input Voltage Range			±1.0			±1.0			V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	86		70	86		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		25	150		25	150	μV/V
Large Signal Voltage Gain		$R_L \geq 75$ kΩ, $V_{OUT} = \pm 1$ V	25 k						V/V
		$R_L \geq 5$ kΩ, $V_{OUT} = \pm 1$ V				25 k			V/V
Output Voltage Swing		$R_L \geq 75$ kΩ	±2.0	±2.4					V
		$R_L \geq 5$ kΩ				±1.9	±2.1		V
Supply Current					25			180	μA
Power Consumption					150			1080	μW

± 15 V Operation for μA776C
Electrical Characteristics T_A = 25°C, unless otherwise specified.

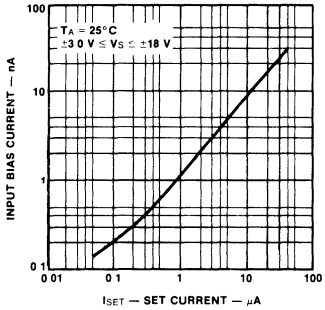
Characteristic		Conditions	I_{SET} = 1.5 μA			I_{SET} = 15 μA			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	6.0		2.0	6.0	mV
Input Offset Current				0.7	6.0		2.0	25	nA
Input Bias Current				2.0	10		15	50	nA
Input Resistance				50			5.0		MΩ
Input Capacitance				2.0			2.0		pF
Offset Voltage Adjustment Range				9.0			18		mV
Large Signal Voltage Gain		$R_L \geq 75$ kΩ, V_{OUT} = ± 10 V	50 k	400 k					V/V
		$R_L \geq 5$ kΩ, V_{OUT} = ± 10 V				50 k	400 k		V/V
Output Resistance				5.0			1.0		kΩ
Output Short-Circuit Current				3.0			12		mA
Supply Current				20	30		160	190	μA
Power Consumption					0.9			5.7	mW
Transient Response (unity gain)	Rise Time	V_{IN} = 20 mV, $R_L \geq 5$ kΩ, $C_L \leq 100$ pF		1.6			0.35		μs
	Overshoot			0			10		%
Slew Rate		$R_L \leq 5$ kΩ		0.1			0.8		V/μs
Output Voltage Swing		$R_L \geq 75$ kΩ	± 12	± 14					V
		$R_L \geq 5$ kΩ				± 10	± 13		V
The following specifications apply 0°C ≤ T_A ≤ +70°C									
Input Offset Voltage		$R_S \leq 10$ kΩ			7.5			7.5	mV
Input Offset Current		T_A = +70°C			6.0			25	nA
		T_A = 0°C			10			40	nA
Input Bias Current		T_A = +70°C			10			50	nA
		T_A = 0°C			20			100	nA
Input Voltage Range			± 10			± 10			V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		25	200		25	200	μV/V
Large Signal Voltage Gain		$R_L \geq 75$ kΩ, V_{OUT} = ± 10 V	50 k			50 k			V/V
Output Voltage Swing		$R_L \geq 75$ kΩ	± 10			± 10			V
Supply Current					35			200	μA
Power Consumption					1.05			6.0	mW

±3 V Operation For μA776C
Electrical Characteristics T_A = 25°C, unless otherwise specified.

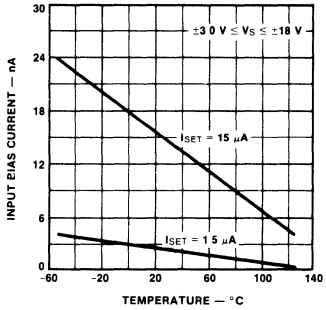
Characteristic		Condition	I_{SET} = 1.5 μA			I_{SET} = 15 μA			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	6.0		2.0	6.0	mV
Input Offset Current				0.7	6.0		2.0	25	nA
Input Bias Current				2.0	10		15	50	nA
Input Resistance				50			5.0		mΩ
Input Capacitance				2.0			2.0		pF
Offset Voltage Adjustment Range				9.0			18		mV
Large Signal Voltage Gain		$R_L \geq 75$ kΩ, $V_{OUT} = \pm 1$ V	25 k	200 k					V/V
		$R_L \geq 5$ kΩ, $V_{OUT} = \pm 1$ V				25 k	200 k		V/V
Output Resistance				5.0			1.0		kΩ
Output Short-Circuit Current				3.0			5.0		mA
Supply Current				13	20		130	170	μA
Power Consumption				78	120		780	1020	μW
Transient Response (unity gain)	Rise Time	V_{IN} = 20 mV, $R_L \geq 5$ kΩ, $C_L \leq 100$ pF		3.0			0.6		μs
	Overshoot			0			5		%
Slew Rate		$R_L \leq 5$ kΩ		0.03			0.35		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C									
Input Offset Voltage		$R_S \leq 10$ kΩ			7.5			7.5	mV
Input Offset Current		T_A = +70°C			6.0			25	nA
		T_A = 0°C			10			40	nA
Input Bias Current		T_A = +70°C			10			50	nA
		T_A = 0°C			20			100	nA
Input Voltage Range			±1.0			±1.0			V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	86		70	86		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		25	200		25	200	μV/V
Large Signal Voltage Gain		$R_L \geq 75$ kΩ, $V_{OUT} = \pm 1$ V	25 k						V/V
		$R_L \geq 5$ kΩ, $V_{OUT} = \pm 1$ V				25 k			V/V
Output Voltage Swing		$R_L \geq 75$ kΩ	±2.0	±2.4					V
		$R_L \geq 5$ kΩ				±2.0	±2.1		V
Supply Current					25			180	μA
Power Consumption					150			1080	μW

Typical Performance Curves for μA776 and μA776C

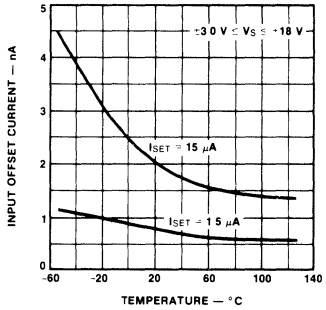
Input Bias Current as a Function of Set Current



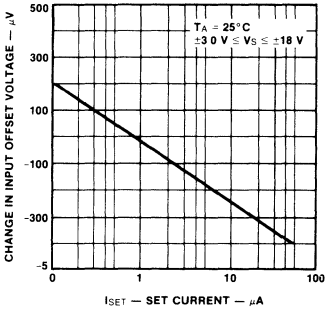
Input Bias Current as a Function of Ambient Temperature



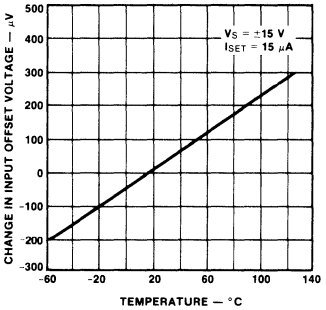
Input Offset Current as a Function of Ambient Temperature



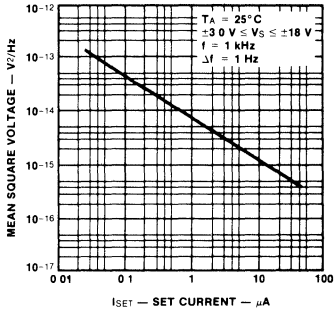
Change in Input Offset Voltage as a Function of Set Current



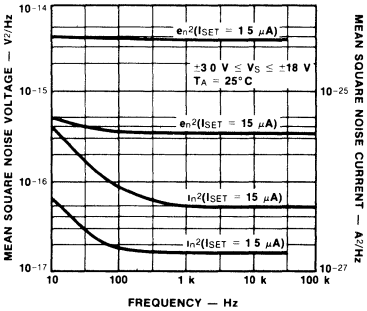
Change in Input Offset Voltage as a Function of Ambient Temperature (Unnulled)



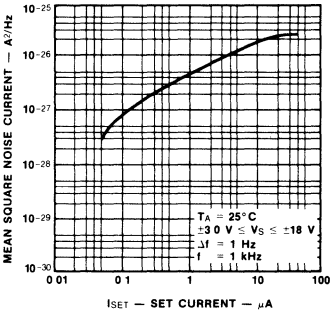
Input Noise Voltage as a Function of Set Current



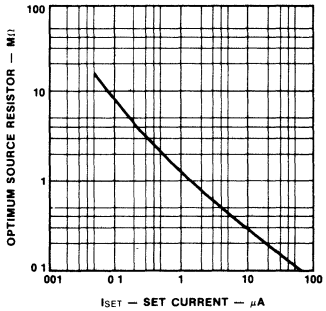
Input Noise Voltage and Current as a Function of Frequency



Input Noise Current as a Function of Set Current



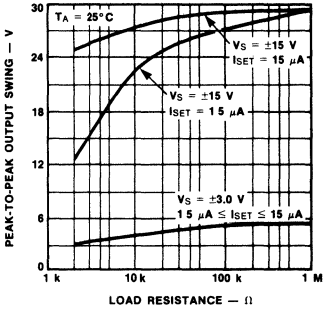
Optimum Source Resistor for Minimum Noise as a Function of Set Current



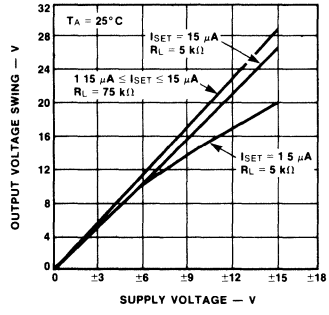
4

Typical Performance Curves for μA776 and μA776C (Cont.)

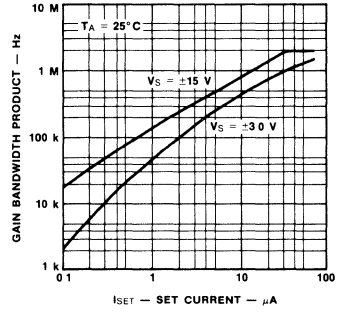
Output Voltage Swing as a Function of Load Resistance



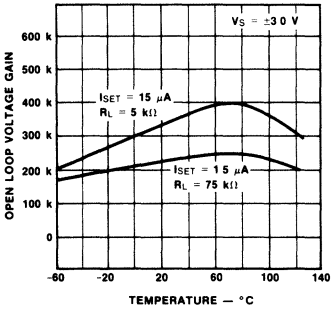
Output Voltage Swing as a Function of Supply Voltage



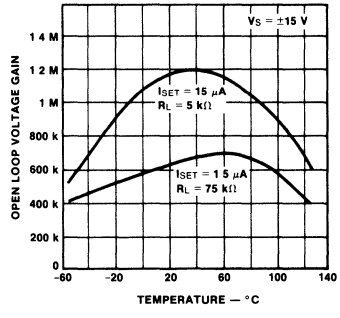
Gain-Bandwidth Product as a Function of Set Current



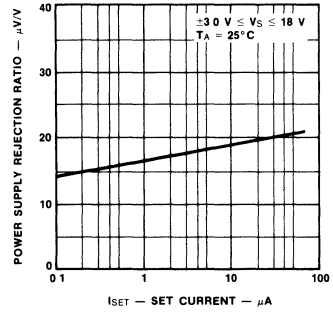
Open Loop Voltage Gain as a Function of Ambient Temperature



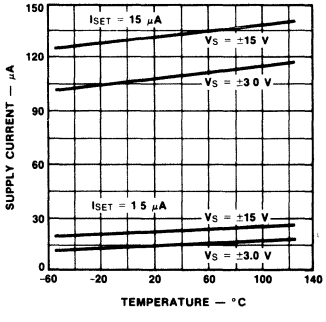
Open Loop Voltage Gain as a Function of Ambient Temperature



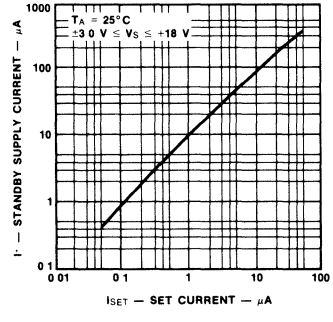
Power Supply Rejection Ratio as a Function of Set Current



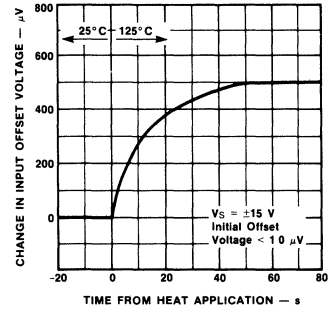
Supply Current as a Function of Ambient Temperature



Standby Supply Current as a Function of Set Current

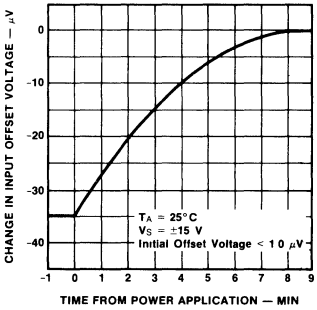


Thermal Response of Input Offset Voltage to Step Change of Case Temperature

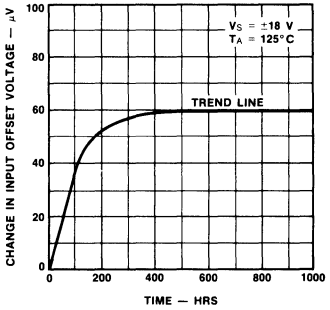


Typical Performance Curves for μA776 and μA776C (Cont.)

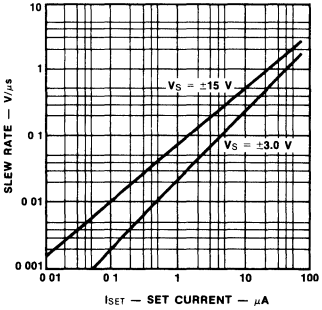
Stabilization Time of Input Offset Voltage From Power On



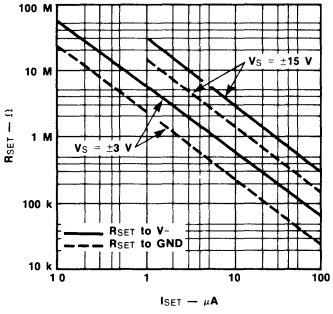
Input Offset Voltage Drift as a Function of Time



Slew Rate as a Function of Set Current



Set Current as a Function of Set Resistor



Quiescent Current Setting Resistor (I_{SET} to V^-)

V_S	I_{SET}	
	1.5 μA	15 μA
±1.5 V	1.7 MΩ	170 kΩ
±3.0 V	3.6 MΩ	360 kΩ
±6.0 V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

Note
The μA776 may be operated with R_{SET} connected to ground or V−

I_{SET} Equations

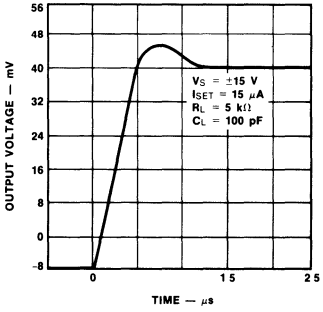
$$I_{SET} = \frac{V+ - 0.7 - V-}{R_{SET}}$$

where R_{SET} is connected to V−

$$I_{SET} = \frac{V+ - 0.7}{R_{SET}}$$

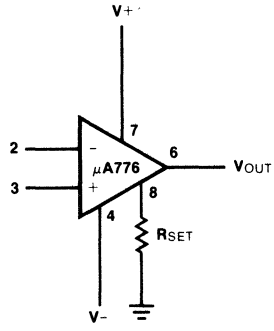
where R_{SET} is connected to ground.

Voltage Follower Transient Response (Unity Gain)

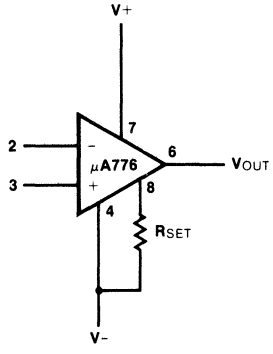


Biasing Circuits

Resistor Biasing

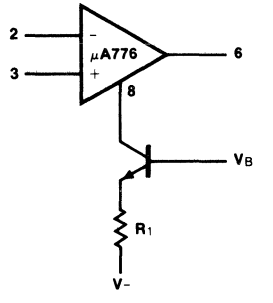


R_{SET} Connected to Ground

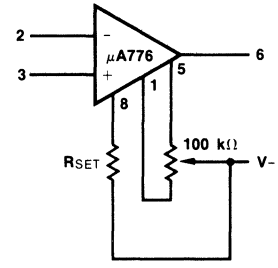


R_{SET} Connected to V^-
*Recommended for supply voltages less than ±6 V.

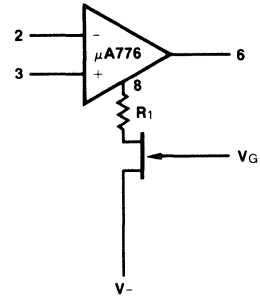
Transistor Current Source Biasing



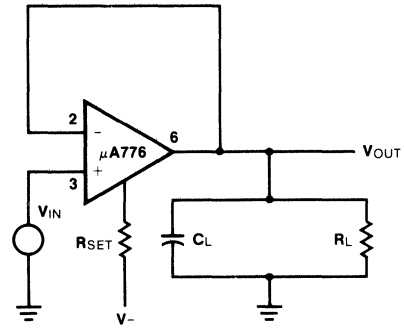
Voltage Offset Null Circuit



FET Current Source Biasing



Transient Response Test Circuit



FAIRCHILD
A Schlumberger Company

μA791 Power Operational Amplifier

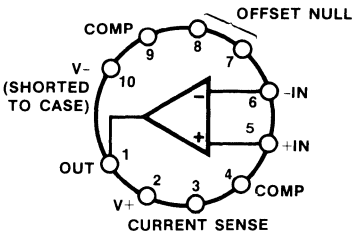
Linear Products

Description

The μA791 is a High Performance Monolithic Operational Amplifier constructed using the Fairchild Planar Epitaxial process with input characteristics similar to the μA741 operational amplifier and 1A available output current. It is intended for use in a wide variety of applications including audio amplifiers, servo amplifiers, and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required. The μA791 is thermal-overload and short-circuit protected.

- **CURRENT OUTPUT TO 1 A**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **NO LATCH UP**
- **LARGE COMMON MODE AND DIFFERENTIAL MODE RANGES**
- **THERMAL-OVERLOAD PROTECTION**

Connection Diagram
10-Pin Metal Package

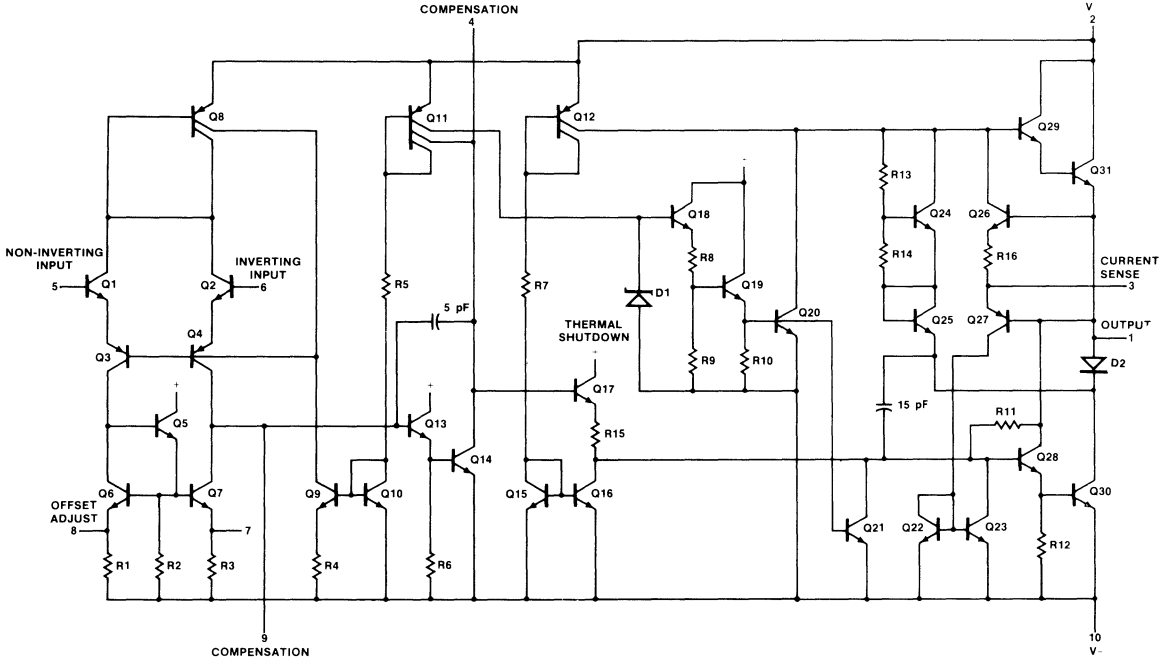


(Top View)

Order Information

Type	Package	Code	Part No.
μA791C	Metal	5H	μA791KC
μA791	Metal	5H	μA791KM

Equivalent Circuit



Note

Pin connections shown are for metal can.

Absolute Maximum Ratings

Supply Voltage	
Military (μA791)	±22 V
Commercial (μA791C)	±18 V
Peak Output Current	1.25 A
Continuous Internal Power Dissipation (Total Package) (Note 1)	Internally Limited
Peak Internal Power Dissipation (Per Output Transistor for $t \leq 5$ s, Note 2)	15 W
Differential Input Voltage	±30 V
Input Voltage (Note 3)	±15 V
Voltages between offset Null and V−	±0.5 V
Operating Junction Temperature	
Military (μA791)	−55°C to +150°C
Commercial (μA791C)	0°C to +125°C
Storage Temperature	
Metal Package	−65°C to +150°C
Pin Temperature	
Metal Package (Soldering, 60 s max.)	280°C

Notes

1 Thermal resistance of the packages (without a heat sink)

Package	Junction to Case		Junction to Ambient		Unit
	Typ	Max	Typ	Max	
TO-3	4	6	35	40	°C/W

2. Under short circuit conditions, the safe operating area and dc power dissipation limitations must be observed.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

μA791 and μA791C
Electrical Characteristics $V_S = \pm 15$ V, $T_J = 25°C$ unless otherwise specified

		μA791			μA791C			
Characteristic	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0		2.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	1.0		MΩ
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio		70			70			dB
Power Supply Rejection Ratio				150			150	μV/V
Large Signal Voltage Gain	$R_L = 1$ kΩ, $V_{OUT} = \pm 10$ V	50 k			20 k			V/V
	$R_L = 10$ Ω, $V_{OUT} = \pm 10$ V	50 k			20 k			V/V
Output Voltage Swing	$R_{SC} = 0$, $R_L = 1$ kΩ	±12	±14		±11.5	±14		V
	$R_{SC} = 0$, $R_L = 10$ Ω	±10	±12.2		±10	±12.2		V
Output Short Circuit Current	$R_{SC} = 0.7$ Ω		1000			1000		mA
	$R_{SC} = 1.5$ Ω		500			500		mA
Supply Current (Zero Signal)				25			30	mA

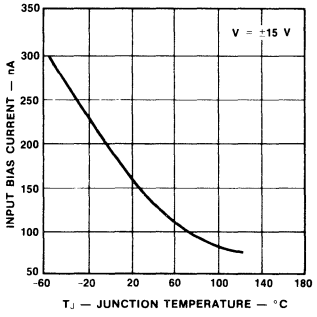
μA791 and μA791C
Electrical Characteristics (Cont.)
The following specifications apply for $-55°C \leq T_J \leq 150°C$

Characteristic	Condition	μA791			μA791C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			800	nA
Common Mode Rejection Ratio		70			70			dB
Power Supply Rejection Ratio				150			150	μV/V
Large Signal Voltage Gain	$R_L = 1\ k\Omega$, $V_{OUT} = \pm 10\ V$	25 k			15 k			V/V
	$R_L = 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	25 k			15 k			V/V
Output Voltage Swing	$R_{SC} = 0$, $R_L = 1\ k\Omega$	±10			±10			V
	$R_{SC} = 0$, $R_L = 10\ k\Omega$	±10			±10			V
Supply Current (Zero Signal)				30			30	mA

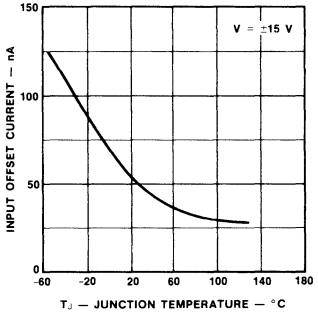
4

Typical Performance Curves for μA791 and μA791C

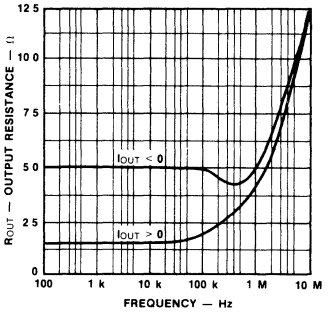
Input Bias Current as a Function of Junction Temperature



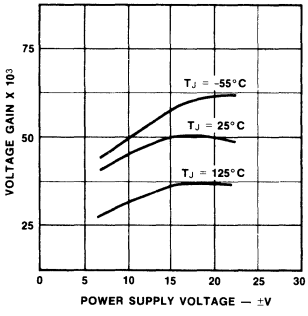
Input Offset Current as a Function of Junction Temperature



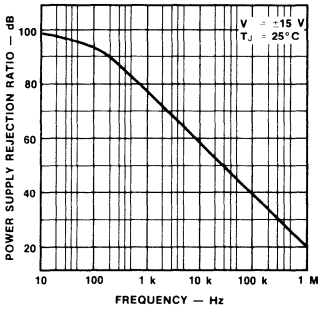
Output Resistance as a Function of Frequency (Open Loop)



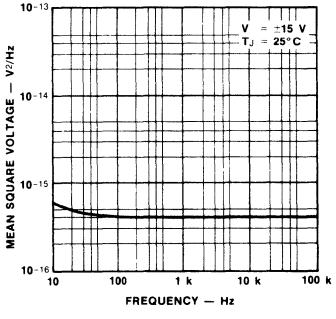
Voltage Gain as a Function of Power Supply Voltage



Power Supply Rejection Ratio as a Function of Frequency

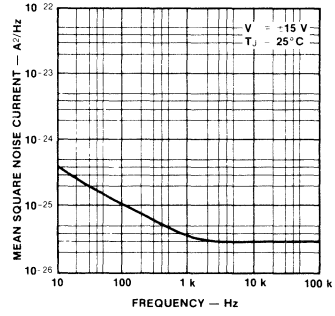


Input Noise Voltage as a Function of Frequency

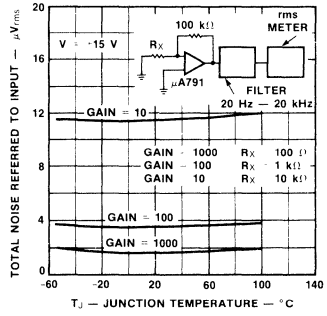


Typical Performance Curves for μA791 and μA791C (Cont.)

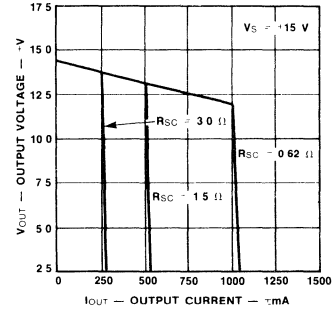
Input Noise Current as a Function of Frequency



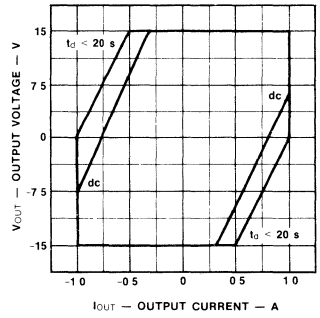
Total Noise (20 Hz–20 kHz) as a Function of Junction Temperature



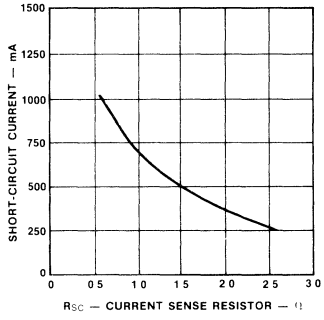
Output Voltage Swing as a Function of Output Current



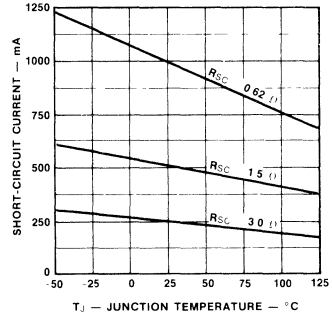
Output Safe Operating Area per Output Transistor



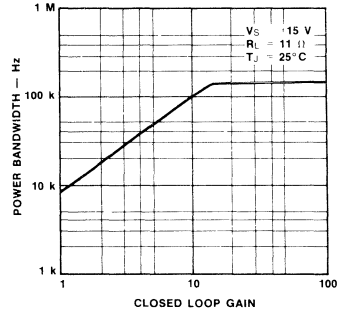
Short Circuit Current as a Function of Current Sense Resistor, R_{SC}



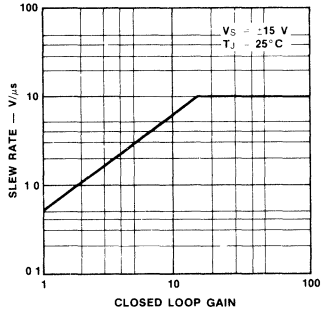
Short Circuit Current as a Function of Case Temperature



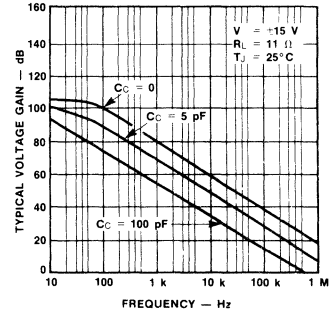
Power Bandwidth as a Function of Closed Loop Gain



Slew Rate as a Function of Closed Loop Gain

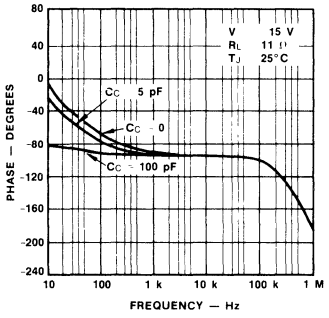


Voltage Gain as a Function of Open Loop Frequency Response

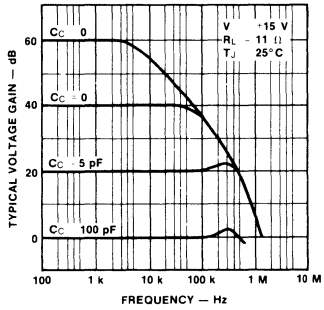


Typical Performance Curves for μA791 and μA791C (Cont.)

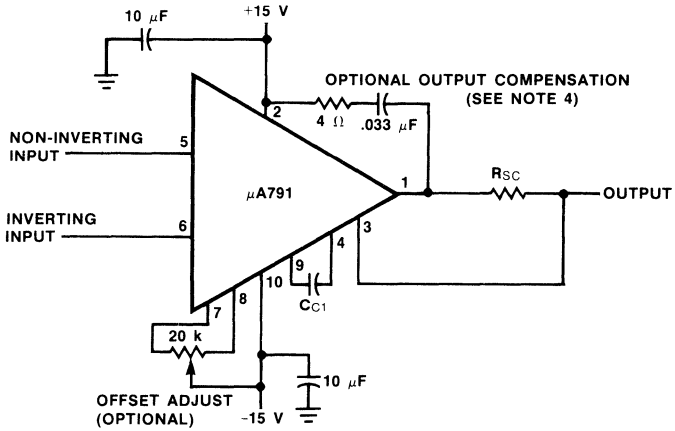
Open Loop Phase Response as a Function of Frequency



Frequency Response for Closed Loop Gains



Frequency Compensation



Gain	C_C
1	100 pF
10	5pF
100	Not Reg.

R_{SC}	I_{SC}
0.6 Ω	1.0 A
1.5 Ω	500 mA
3.0 Ω	250 mA

Notes

1 Power supply decoupling capacitors and compensation network components must have short leads and they must be located at the amplifier pins.

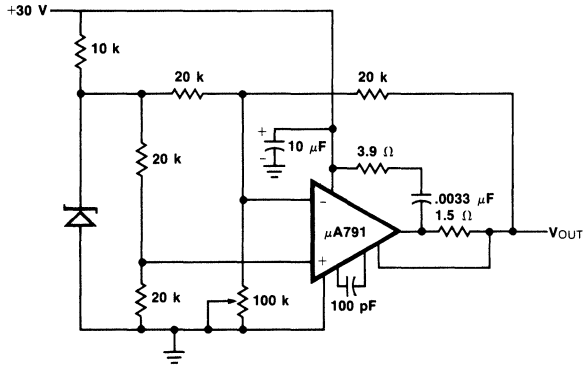
2. When short-circuit limiting is not required, connect terminals one and three together.

3. Pin connections in parentheses are for plastic packages.

4. Output compensation may be required for some loads.

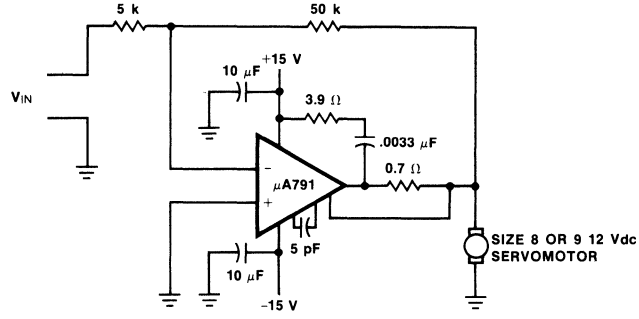
Typical Applications

Positive Voltage Regulator

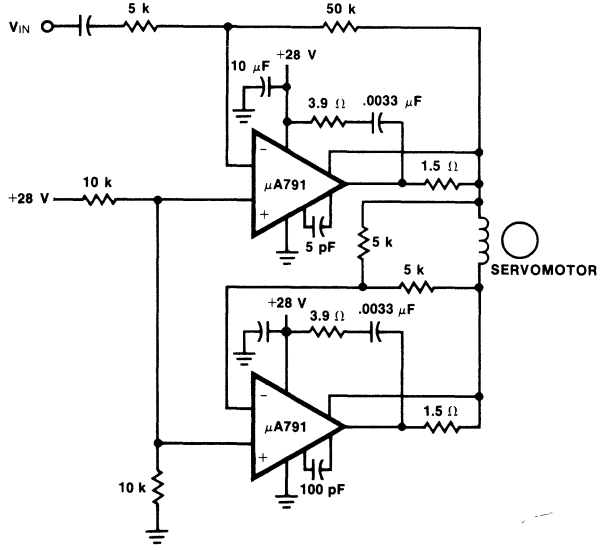


Notes
3.0 V to 27 V regulator
500 mA output current

DC Servo Amplifier



AC Servo Amplifier Bridge Type



FAIRCHILD
A Schlumberger Company

μA798
Dual Operational Amplifier

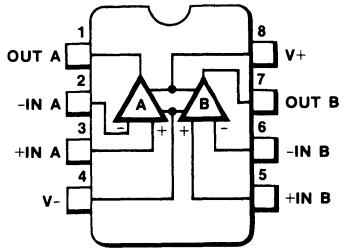
Linear Products

Description

The μA798 is a monolithic pair of independent, high gain, internally frequency compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage. They are constructed using the Fairchild Planar epitaxial process.

- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **OUTPUT VOLTAGE CAN SWING NEAR GROUND OR NEGATIVE SUPPLY**
- **INTERNALLY COMPENSATED**
- **WIDE POWER SUPPLY RANGE SINGLE SUPPLY OF 3.0 TO 36 V DUAL SUPPLY OF ± 1.5 V TO ± 18 V**
- **CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION**
- **SHORT CIRCUIT PROTECTED OUTPUT**
- **HIGH OPEN LOOP GAIN 200 k**
- **EXCEEDS 1458 TYPE PERFORMANCE**
- **OPERATION SPECIFIED AT ± 15 V AND +5 V POWER SUPPLIES**
- **HIGH OUTPUT CURRENT SINK CAPABILITY 0.8 mA AT V_{OUT} = 400 mV**

Connection Diagram
8-Pin Mini DIP



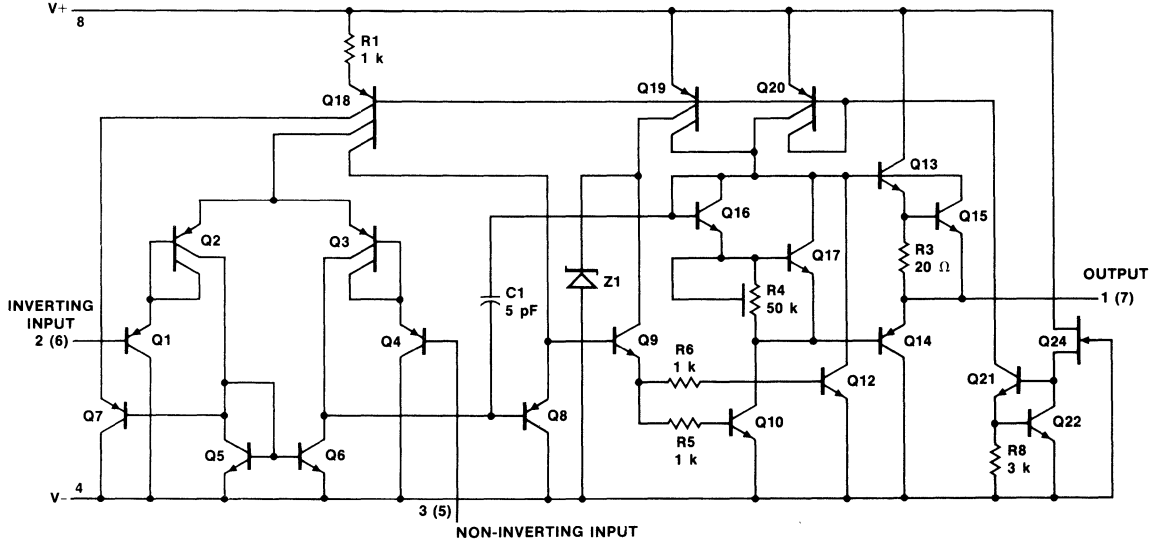
(Top View)

Order Information

Type	Package	Code	Part No.
μA798C	Molded DIP	9T	μA798TC

4

Equivalent Circuit (1/2 of circuit shown)



Absolute Maximum Ratings

Supply Voltage Between V+ and V−	36 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (V−) (Note 1)	−0.3 V (V−) to V+
Internal Power Dissipation (Note 2)	310 mW
Operating Temperature Range	
Commercial (C)	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C (Note 5)
Output Short Circuit Duration	

Notes

1. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C. Above TA = 70°C, derate linearly 5.6 mW/°C for the Molded DIP.
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.
5. Indefinite on shorts to ground or V− supply. Shorts to V+ supply may result in power dissipation exceeding the absolute maximum rating.

μA798C
Electrical Characteristics $V_S = \pm 15$, V, $T_A = 25°C$ unless otherwise noted.

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage			2.0	6.0	mV
Input Offset Current			10	50	nA
Input Bias Current			−50	−250	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L = 2$ kΩ	20	200		V/mV
Power Bandwidth	$A_V = 1$, $R_L = 2$ kΩ, $V_{OUT} = 20$ V pk-pk		9.0		kHz
Small Signal Bandwidth	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		1.0		MHz
Slew Rate	$A_V = 1$, $V_{IN} = -10$ V to +10 V		0.6		V/μs
Rise Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		μs
Fall Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		μs
Overshoot	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		20		%
Phase Margin	$A_V = 1$, $R_L = 2$ kΩ, $C_L = 200$ pF		60		Degree
Crossover Distortion	$V_{IN} = 30$ mV pk-pk, $V_{OUT} = 2$ V pk-pk f = 10 kHz		0.1		%
Output Voltage Range	$R_L = 10$ kΩ $R_L = 2$ kΩ	±13 ±12	±14 ±13.5		V V
Individual Output Short Circuit Current	(Notes 3, 4)	±10	±30		mA
Output Impedance	f = 20 Hz		800		Ω
Power Supply Rejection Ratio	Positive Negative		30 30	150 150	μV/V μV/V
Power Supply Current	$V_{OUT} = 0$, $R_L = \infty$		2.0	4.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB
The following specifications apply for $0°C \leq T_A \leq 70°C$					
Input Offset Voltage				7.5	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				−400	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ, $V_{OUT} = \pm 10$ V	15			V/mV
Output Voltage Range	$R_L = 2$ kΩ	±10			V

Notes
3. Not to exceed maximum package power dissipation.
4. Indefinite on shorts to ground or V− supply. Shorts to V+ supply may result in power dissipation exceeding the absolute maximum rating.

Electrical Characteristics $V_S = \pm 5.0$ V and Ground, $T_A = 25°C$ unless otherwise noted.

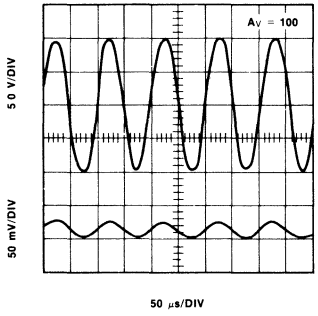
Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage			2.0	7.5	mV
Input Offset Current			10	50	nA
Input Bias Current			−80	−250	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range (Note 5)	$R_L = 10$ kΩ $R_L = 10$ kΩ, 5.0 V ≤ V_S ≤ 30 V	4.0 (V+) −1.5			V pk-pk V pk-pk
Output Sink Current	$V_{IN} = 1.0$ V, $V_{OUT} = 200$ mV	0.35			mA
Power Supply Current			2.0	4.0	mA

Note

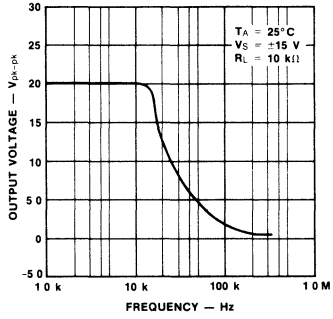
5. Output will swing to ground.

Typical Performance Curves

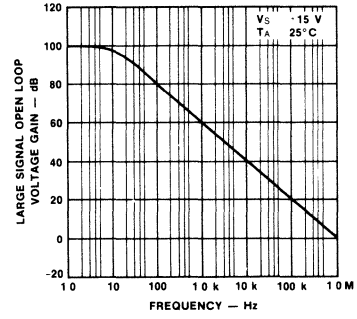
Sinewave Response



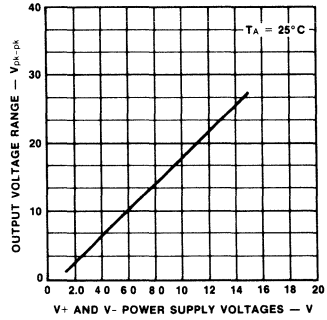
Output Voltage as a Function of Frequency



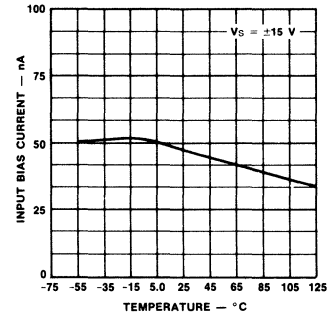
Large Signal Open Loop Voltage Gain as a Function of Frequency



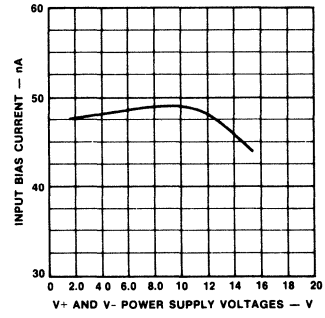
Output Swing as a Function of Supply Voltage



Input Bias Current as a Function of Temperature

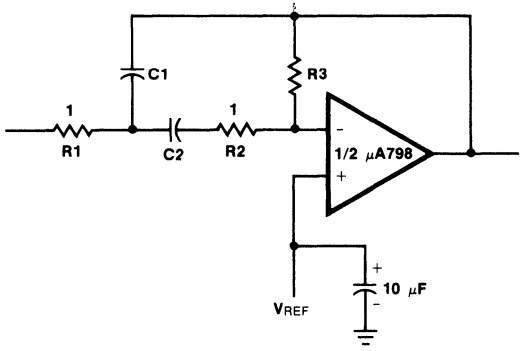


Input Bias Current as a Function of Supply Voltage



Typical Applications

Multiple Feedback Bandpass Filter



$f_o \triangleq$ center frequency

BW $\triangleq$ Bandwidth
R in kΩ
C in μF

$$Q = \frac{f_o}{BW} < 10$$

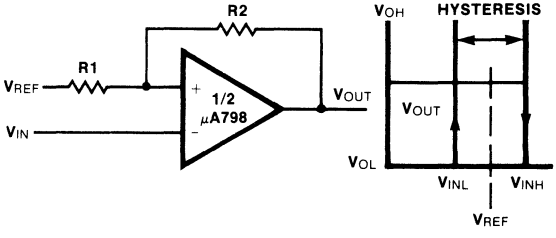
$$C1 = C2 = \frac{Q}{3}$$

$$\left.\begin{array}{l} R1 = R2 = 1 \\ R3 = 9Q^2 - 1 \end{array}\right\}$$ Use scaling factors in these expressions.

If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters

Design example:
given: Q = 5, f_o = 1 kHz
Let R1 = R2 = 10 kΩ
then R3 = $9(5)^2 - 10$
R3 = 215 kΩ
$C = \frac{5}{3} = 1.6$ nF

Comparator With Hysteresis



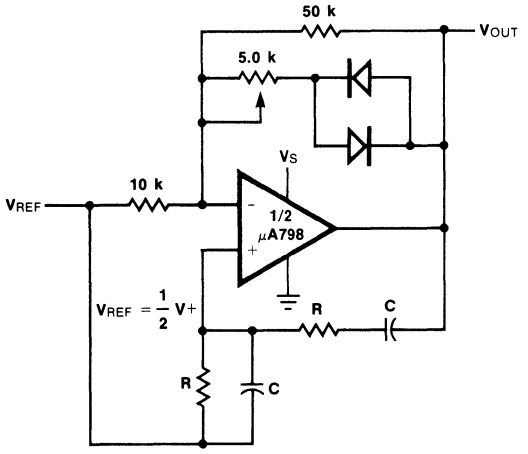
$$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH}\, V_{OL})$$

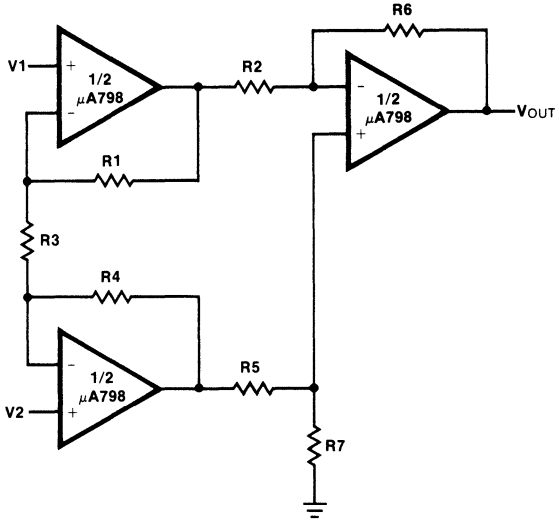
$$f = \frac{R1 + R2}{4CR_fR1} \text{ if } R3 = \frac{R2R1}{R2 + R1}$$

Wein Bridge Oscillator



$$f_o = \frac{1}{2\pi RC} \quad \text{for } f_o = 1 \text{ kHz}$$
R = 16 kΩ
C = 0.01 μF

High Impedance Differential Amplifier



$$V_{OUT} = C(1 + a + b)(V2 - V1)$$

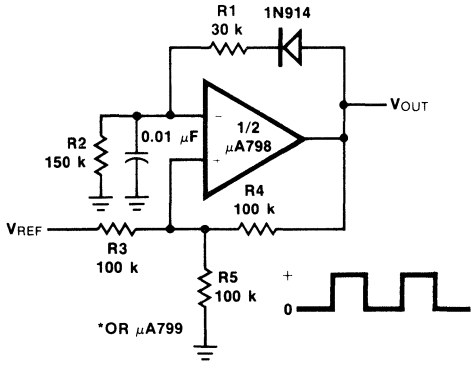
$$\frac{R2}{R5} \equiv \frac{R6}{R7} \text{ for best CMRR}$$

R1 = R4
R2 = R5

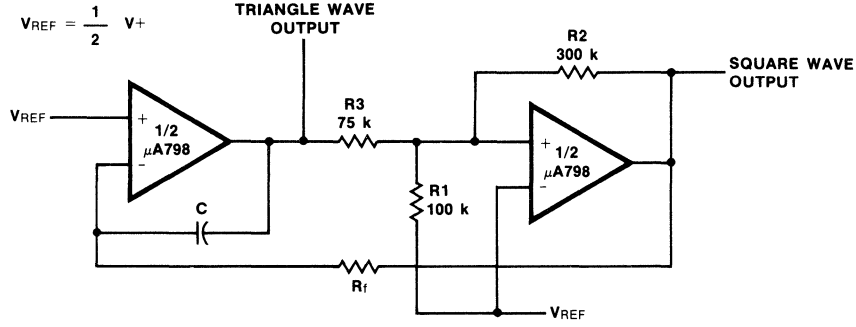
$$\text{Gain} = \frac{R6}{R2}\left(1 + \frac{2R1}{R3}\right) = C(1 + a + b)$$

Typical Applications (Cont.)

Pulse Generator



Function Generator



FAIRCHILD

A Schlumberger Company

μA101 • μA201 General Purpose Operational Amplifiers

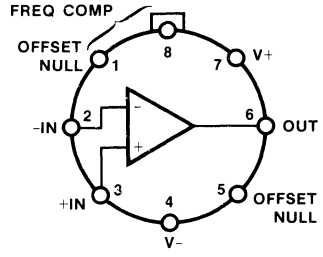
Linear Products

Description

The μA101 and μA201 are General Purpose Monolithic Operational Amplifiers constructed using the Fairchild Planar epitaxial process. They are intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. The μA101 and μA201 compensate easily with a single external component. High common mode voltage range and absence of "latch-up" make the μA101 and μA201 ideal for use as voltage followers. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA101 and μA201 are short-circuit protected and have the same pin configuration as the popular μA741, μA748 and μA709.

- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

Connection Diagram
8-Pin Metal Package



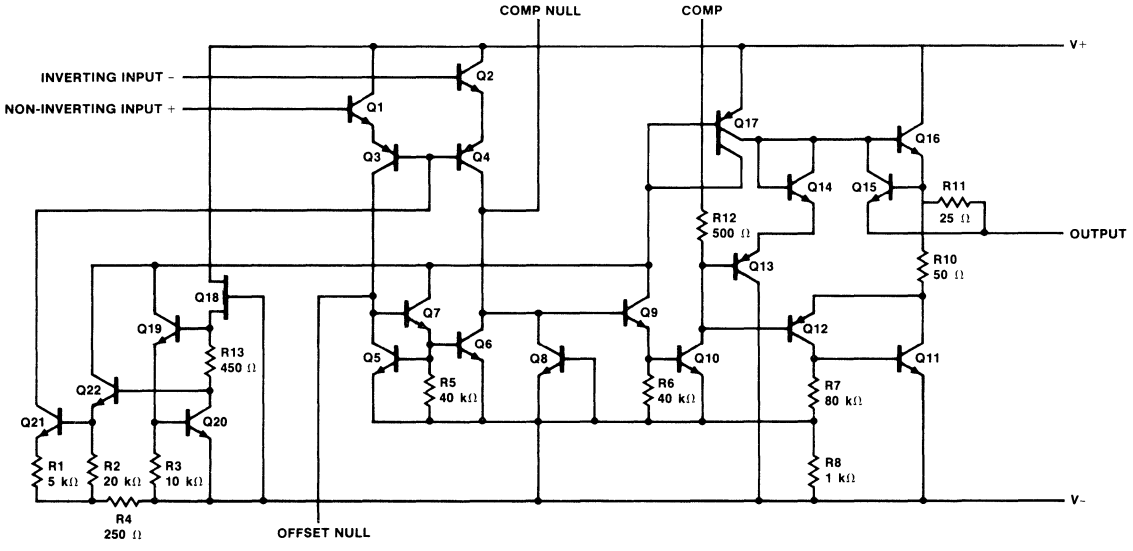
(Top View)

Pin 4 connected to case

Order Information

Type	Package	Code	Part No.
μA101	Metal	5W	μA101HM
μA201	Metal	5W	μA201HC

Equivalent Circuit



Absolute Maximum Ratings

Supply Voltage	±22 V	Operating Temperature Range (Note 3)	
Internal Power Dissipation (Note 1)		Military (μA101)	−55°C to +125°C
Metal Package	500 mW	Commercial (μA201)	0°C to +70°C
Differential Input Voltage	±30 V	Pin Temperature (Soldering, 60 s)	300°C
Input Voltage (Note 2)	±15 V		
Storage Temperature Range			
Metal Package	−65°C to +150°C		

μA101
Electrical Characteristics $\pm 5.0\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$, unless otherwise specified.

μA201
Electrical Characteristics $\pm 5.0\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$

Characteristic	Condition	μA101 Min	μA101 Typ	μA101 Max	μA201 Min	μA201 Typ	μA201 Max	Unit
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	5.0		2.0	7.5	mV
Input Offset Current			40	200		100	500	nA
Input Bias Current			120	500		0.25	1.5	μA
Input Resistance		300	800		100	400		kΩ
Supply Current	$V_S = \pm 20\ V$		1.8	3.0				mA
	$V_S = \pm 15\ V$					1.8	3.0	
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$	50	160		20	150		V/mV
The following specifications apply over $-55°C \leq T_J \leq 125°C$ for μA101, $0°C \leq T_J \leq 70°C$ for μA201.								
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0			10	mV
Average Temperature Coefficient of Input	$R_S \leq 50\ \Omega$		3.0			6.0		μV/°C
Offset Voltage	$R_S \leq 10\ k\Omega$		6.0			10.0		μV/°C
Input Offset Current	$T_A =$		10	200		50	400	nA
	$T_A =$		100	500		150	750	nA
Average Temperature Coefficient of Input Offset Current	$+25 \leq T_A \leq$ max min $\leq T_A \leq +25°C$		0.01 0.02	0.1 0.2		0.01 0.02	0.3 0.6	nA/°C nA/°C
Input Bias Current	$T_A = -55°C$		0.28	1.5		0.32	2.0	μA
Supply Current	$T_A = +125°C$, $V_S = \pm 20\ V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$V_S = \pm 15\ V$, $R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 15\ V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB

Notes

1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. The 101 ratings apply to +125°C case temperature or +75°C ambient temperature. The 201 ratings apply to case temperatures up to +70°C.

FAIRCHILD

A Schlumberger Company

μA101A • μA201A • μA301A General-Purpose Operational Amplifiers

Linear Products

Description

The μA101A, μA201A and μA301A are General-Purpose Monolithic Operational Amplifiers constructed using the Fairchild Planar epitaxial process. These integrated cirucuits are intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers and sample and hold circuits is improved due to the low drift and low bias currents of the μA101A, μA201A, or μA301A. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of "latch-up" coupled with internal short-circuit protection make the μA101A, μA201A and μA301A virtually foolproof.

- **LOW OFFSET CURRENT AND VOLTAGE**
- **LOW OFFSET CURRENT DRIFT**
- **LOW BIAS CURRENT**
- **SHORT CIRCUIT PROTECTED**
- **LOW POWER CONSUMPTION**

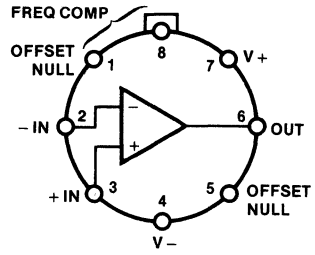
Absolute Maximum Ratings

Supply Voltage	
Military and Instrument (μA101A and μA201A)	±22 V
Commercial (μA301A)	±18 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Package	−64°C to +150°C
DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA101A)	−55°C to +125°C
Instrument (μA201A)	−25°C to +85°C
Commercial (μA301A)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Package (60 s)	300°C
DIP (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

Notes

1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the metal package, 5.6 mW/°C for the DIP.
2. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. 101A and 201A ratings apply to +125°C case temperature or +75°C ambient temperature. 301A ratings apply for case temperatures to 70°C.

Connection Diagram 8-Pin Metal Package



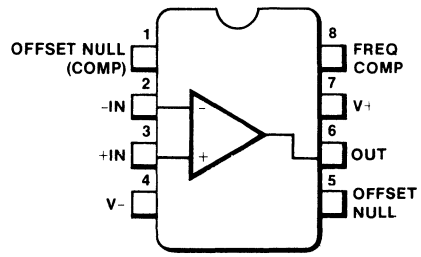
(Top View)

Pin 4 connected to case

Order Information

Type	Package	Code	Part No.
μA101A	Metal	5 W	μA101AHM
μA201A	Metal	5 W	μA201AHM
μA301A	Metal	5 W	μA301HC

Connection Diagram 8-Pin DIP



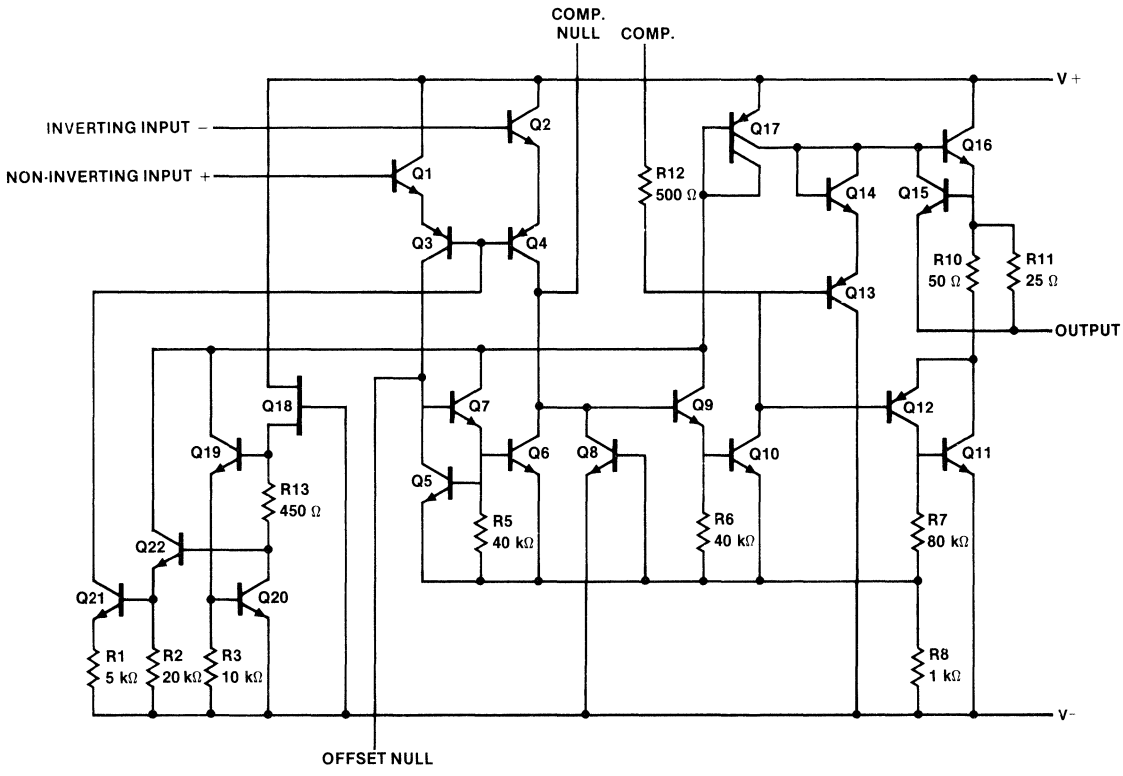
(Top View)

Order Information

Type	Package	Code	Part No.
μA301A	Molded DIP	9T	μA301ATC

4

Equivalent Circuit



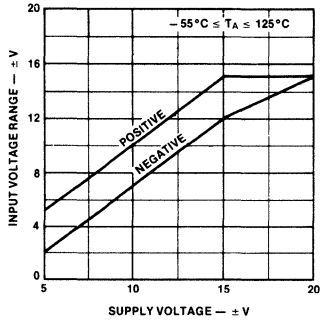
Electrical Characteristics $T_A = +25°C$ unless otherwise noted. Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the μA101A and μA201A, and from ±5.0 V to ±15 V for the 301A.

			μA101A, μA201A			μA301A			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{IO}	Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.7	2.0		2.0	7.5	mV
I_{IO}	Input Offset Current			1.5	10		3.0	50	nA
I_{IB}	Input Bias Current			30	75		70	250	nA
r_i	Input Resistance		1.5	4.0		0.5	2.0		MΩ
I_{CC}, I_{EE}	Supply Current	$V_{CC}/V_{EE} = \pm 20$ V $V_{CC}/V_{EE} = \pm 15$ V		1.8	3.0		1.8	3.0	mA
A_V	Large Signal Voltage Gain	V_{CC}/V_{EE} ±15 V, V_O = ±10 V, $R_L > 2.0\ k\Omega$	50	160		25	160		V/mV
The following specifications apply over the operating temperature range.									
V_{IO}	Input Offset Voltage	$R_S \leq 10\ k\Omega$			3.0			10	mV
I_{IO}	Input Offset Current				20			70	nA
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	T_A (min) $\leq T_A \leq T_A$(max)		3.0	15		6.0	30	μV/°C
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	$+25°C \leq T_A \leq T_A$ (max) T_A (min) $\leq T_A \leq 25°C$		0.01 0.02	0.1 0.2		0.01 0.02	0.3 0.6	nA/°C
I_B	Input Bias Current				100			300	nA
A_V	Large Signal Voltage Gain	$V_{CC}/V_{EE} = \pm 15$ V, V_O = ±10 V, $R_L \geq 2.0\ k\Omega$	25			15			V/mV
V_I	Input Voltage Range	$V_{CC}/V_{EE} = \pm 20$ V $V_{CC}/V_{EE} = \pm 15$ V	±15			±12			V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	80	96		70	90		dB
PSSR	Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	80	96		70	96		dB
V_O	Output Voltage Swing	$V_{CC}/V_{EE} = \pm 15$ V, $R_L = 10\ k\Omega$ $R_L = 2.0\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V
I_{CC}, I_{EE}	Supply Currents	$T_A = T_A$ (max) $V_{CC}/V_{EE} = \pm 20$ V		1.2	2.5				mA

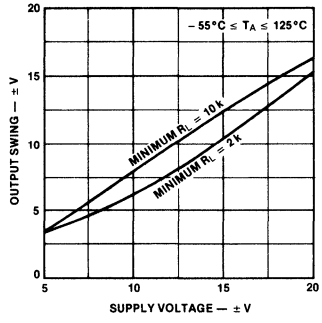
4

Typical Performance Curves for μA101A and μA201A

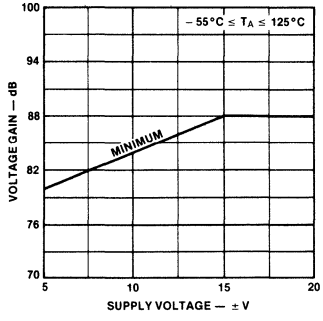
Input Voltage Range as a Function of Supply Voltage



Output Swing as a Function of Supply Voltage

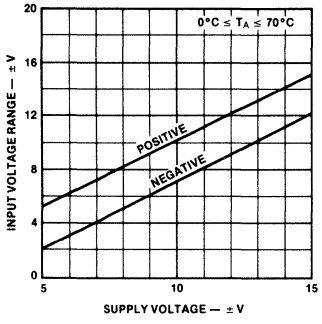


Voltage Gain as a Function of Supply Voltage

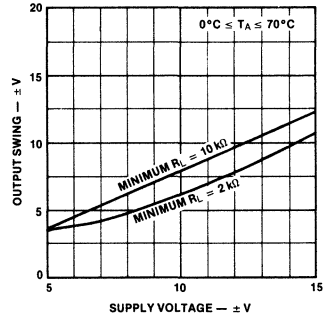


Typical Performance Curves for μA301A

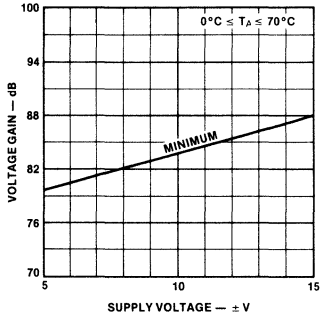
Input Voltage Range as a Function of Supply Voltage



Output Swing as a Function of Supply Voltage

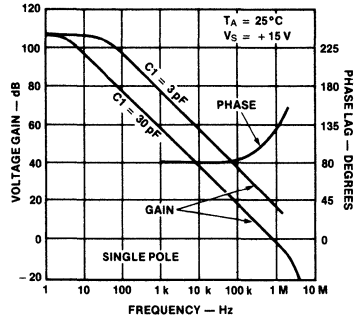


Voltage Gain as a Function of Supply Voltage

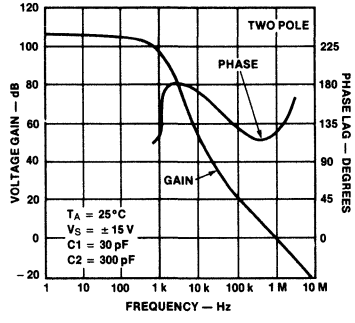


Typical Performance Curves for μA101A, μA201A and μA301A

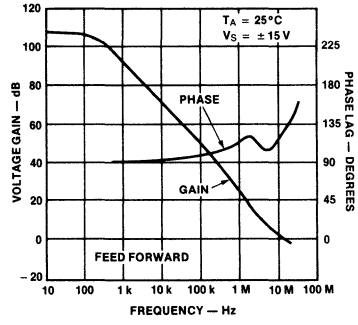
Open Loop Frequency Response



Open Loop Frequency Response

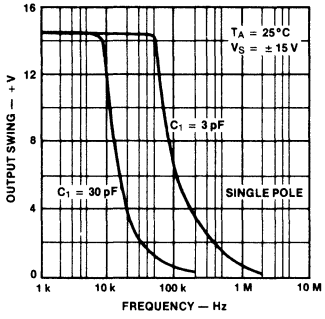


Open Loop Frequency Response

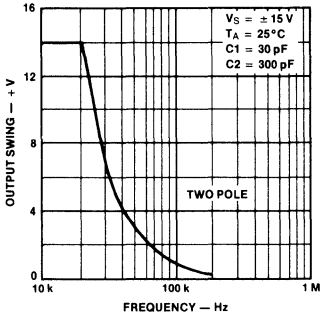


Typical Performance Curves for μA101A, μA201A and μA301A (Cont.)

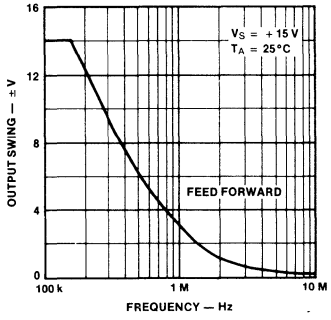
Large Signal Frequency Response



Large Signal Frequency Response

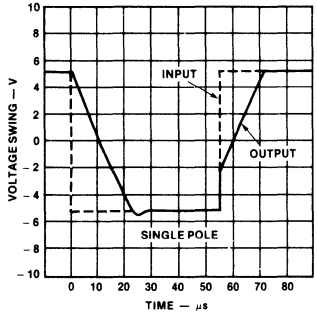


Large Signal Frequency Response

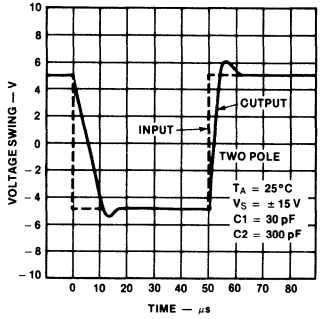


4

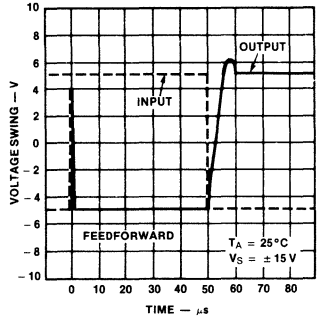
Voltage Follower Pulse Response



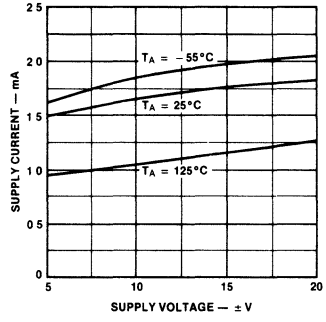
Voltage Follower Pulse Response



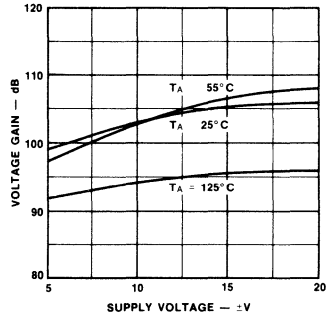
Inverter Pulse Response



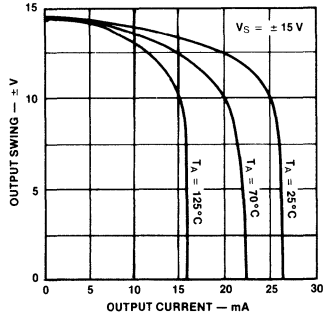
Supply Voltage Current as Function of Supply Voltage



Voltage Gain as a Function of Supply Voltage

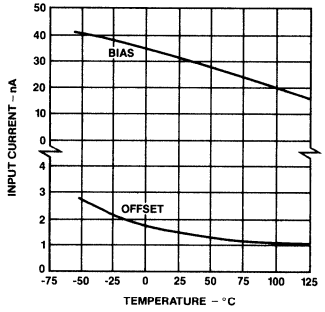


Current Limiting

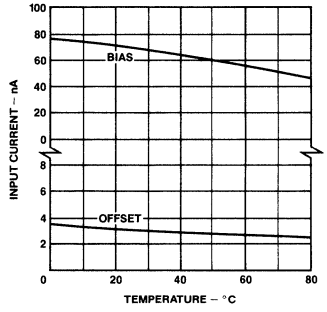


Typical Performance Curves for μA101, μA201 and μA301 (Cont.)

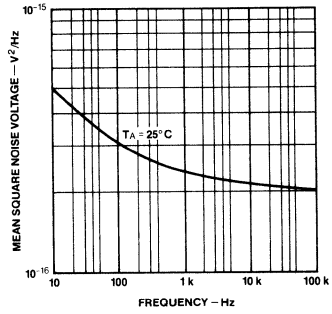
Input Current vs Temperature (μA101A and μA201A only)



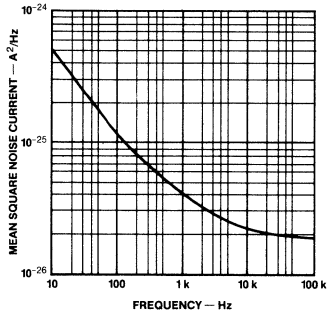
Input Current vs Temperature (μA301A only)



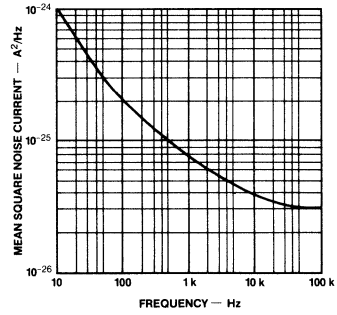
Input Noise Voltage vs Frequency



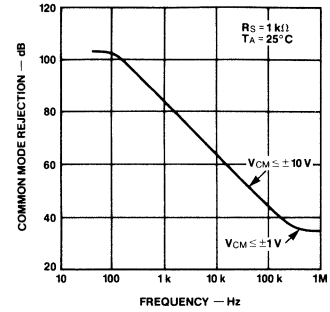
Input Noise Current vs Frequency (μA101A and μA201A only)



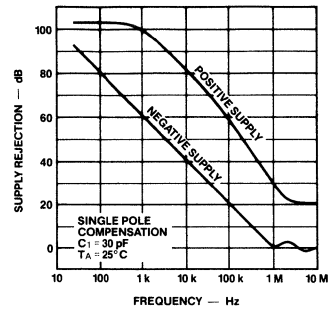
Input Noise Current vs Frequency (μA301A only)



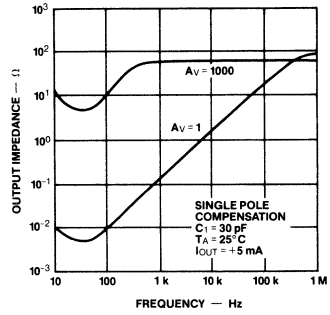
Common Mode Rejection vs Frequency



Power Supply Rejection vs Frequency

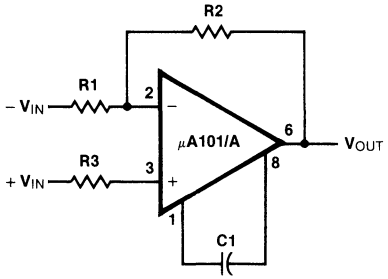


Closed Loop Output Impedance vs Frequency



Compensation Circuits
(All pin numbers shown refer to 8-Pin metal package)

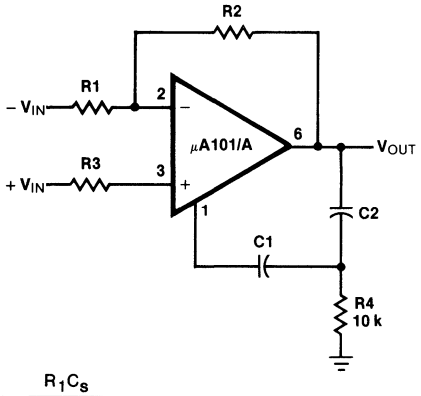
Single Pole Compensation



$$C_1 \geq \frac{R_1 C_s}{R_1 + R_2}$$

C_s = 30 pF

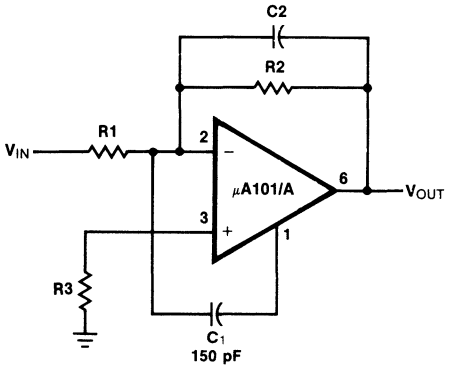
Two Pole Compensation



$$C_1 \geq \frac{R_1 C_s}{R_1 + R_2}$$

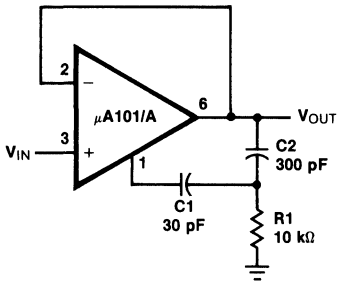
C_s = 30 pF
$C_2 = 10\ C_1$

Feedforward Compensation



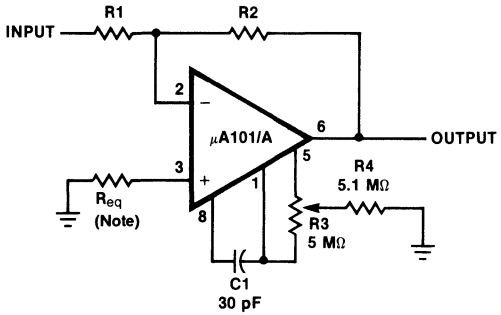
Typical Applications
(All pin numbers shown refer to 8-Pin metal package)

Fast Voltage Follower



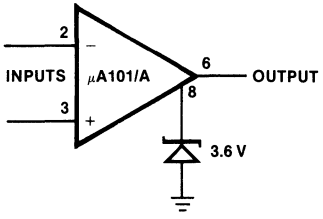
Power Bandwidth: 15 kHz
Slew Rate: 1 V/μs

Inverting Amplifier With Balancing Circuit



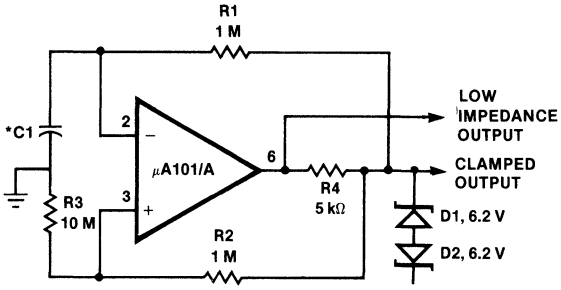
Note
May be zero or equal to parallel combination of R1 and R2 for minimum offset.

Voltage Comparator for Driving or DTL Integrated Circuits



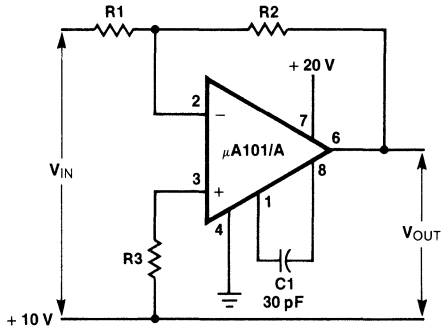
Typical Applications (Cont.)
(All pin numbers shown refer to 8-Pin metal package)

Low Frequency Square Wave Generator

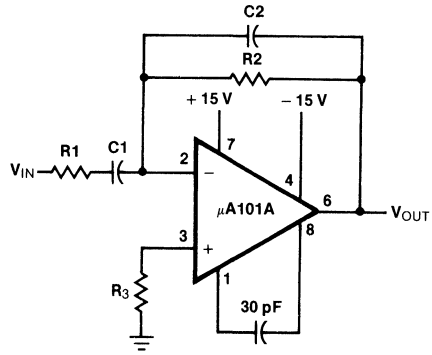


*Adjust C_1 for frequency

Circuit for Operating Without a Negative Supply



Practical Differentiator



$$f_c = \frac{1}{2\pi R_2 C_1}$$

$$f_h = \frac{1}{2\pi R_1 C_1}$$

$$= \frac{1}{2\pi R_2 C_2}$$

$f_c < f_h < f_{unity\ gain}$

FAIRCHILD

A Schlumberger Company

μA107 • μA207 • μA307 General Purpose Operational Amplifiers

Linear Products

Description

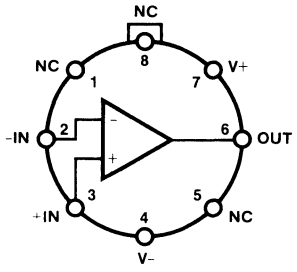
The μA107 General Purpose Operational Amplifier series is constructed using the Fairchild Planar epitaxial process. Advanced processing techniques have reduced the 107 input current an order of magnitude below industry standards such as the μA709 while still replacing, pin-for-pin, μA709, μA101, μA101A, and μA741. The μA107, μA207, and μA307 offer better accuracy, internal compensation, and lower noise for high impedance circuit applications while providing features similar to the μA101A. The low input currents allow the device to be used in slow-charge applications such as long period integrators, slow ramps, and sample-and-hold circuits. The μA207 is identical to the μA107 except that the μA207 performance is guaranteed from −25°C to +85°C while the μA107 performance is guaranteed over a −55°C to +125°C temperature range. The μA307 is guaranteed over a 0°C to +70°C temperature range.

- **LOW OFFSET VOLTAGE**
- **LOW INPUT CURRENT**
- **LOW OFFSET CURRENT**
- **GUARANTEED DRIFT CHARACTERISTICS**
- **GUARANTEED OFFSETS OVER COMMON MODE RANGE**

Absolute Maximum Ratings

Supply Voltage	
Military and Instrument (μA107 and μA207)	±22 V
Commercial (μA307)	±18 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
Molded DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Package	−65°C to +150°C
Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA107)	−55°C to +125°C
Instrument (μA207)	−25°C to +85°C
Commercial (μA307)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Package (60 s)	300°C
Molded DIP (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

Connection Diagram
8-Pin Metal Package



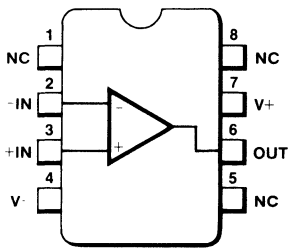
(Top View)

Pin 4 connected to case

Order Information

Type	Package	Code	Part No.
μA107	Metal	5W	μA107HM
μA207	Metal	5W	μA207HM
μA307	Metal	5W	μA307HC

8-Pin Molded DIP



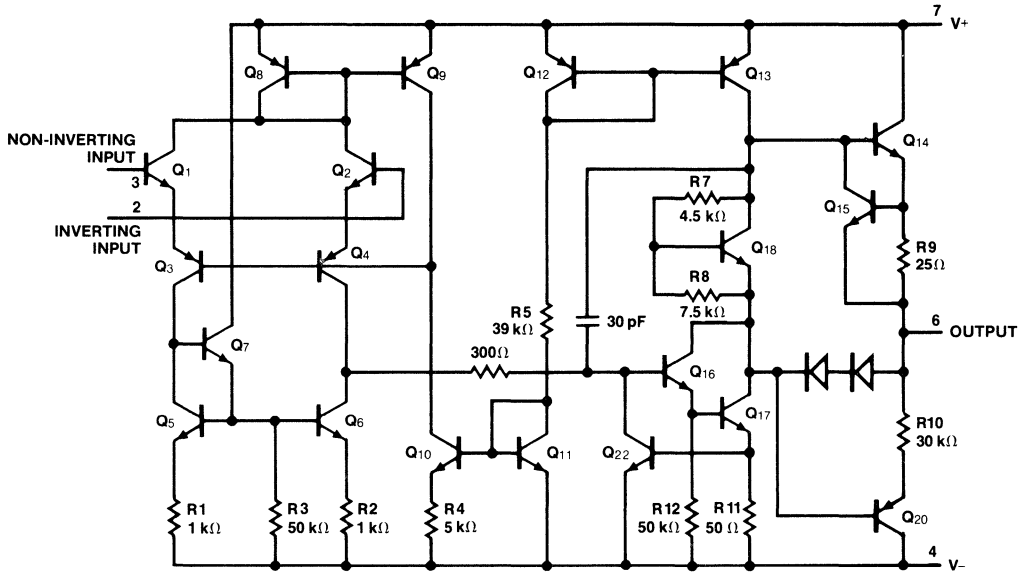
(Top View)

Order Information

Type	Package	Code	Part No.
μA307	Molded DIP	9T	μA307TC

Notes on following page

Equivalent Circuit



Notes

1 Rating applies to ambient temperatures up to 70°C Above 70°C ambient derate linearly at 6 3 mW/°C for metal package and 5 6 mW/°C for the molded DIP

2 For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage

3 Continuous short circuit is allowed with μA307 for case temperatures to 70°C and ambient temperatures to 55°C

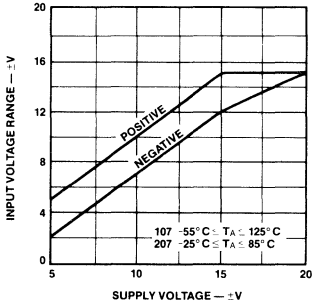
μA107/μA207
Electrical Characteristics $\pm 5.0\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$ unless otherwise specified.

Characteristics	Conditions		Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 50\ k\Omega$			0.7	2.0	mV
Input Offset Current				1.5	10	nA
Input Bias Current				30	75	nA
Input Resistance			1.5	4.0		MΩ
Supply Current	$V_S = \pm 20\ V$			1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$ $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$		50	160		V/mV
The following applies for $55°C \leq T_A \leq 125°C$ unless otherwise specified						
Input Offset Voltage	$R_S \leq 50\ k\Omega$				3.0	mV
Average Temperature Coefficient of Input Offset Voltage				3.0	15	μV/°C
Input Offset Current					20	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$			0.01	0.1	nA/°C
	$-55°C \leq T_A \leq 25°C$			0.02	0.2	nA/°C
Input Bias Current					100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20\ V$			1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$ $R_L \geq 2\ k\Omega$		25			V/mV
Output Voltage Swing	$V_S = \pm 15\ V$	$R_L = 10\ k\Omega$	±12	±14		V
		$R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 20\ V$		±15			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		dB

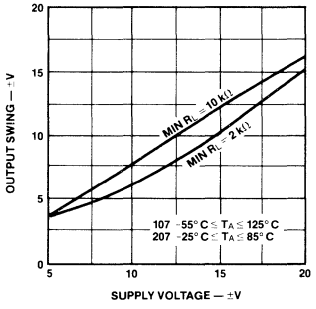
4

Guaranteed Performance Curves for μA107 and μA207

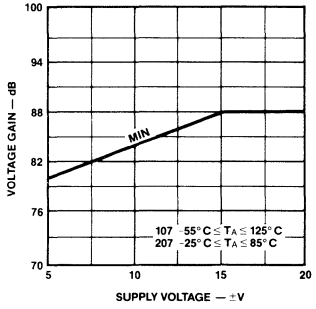
Input Voltage Range vs Supply Voltage



Output Swing vs Supply Voltage



Voltage Gain vs Supply Voltage

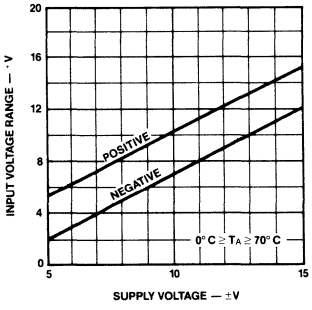


μA307
Electrical Characteristics $\pm 5.0\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$ unless otherwise specified.

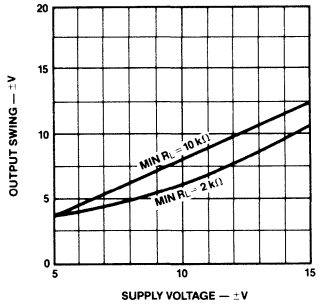
Characteristics	Conditions		Min	Typ	Max	Units
Input Offset Voltage	$R_S \leq 50\ k\Omega$			2.0	7.5	mV
Input Offset Current				3.0	50	nA
Input Bias Current				70	250	nA
Input Resistance			0.5	2.0		MΩ
Supply Current	$V_S = \pm 15\ V$			1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$ $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$		25	160		V/mV
The following specifications apply for $0°C \leq T_A \leq 70°C$						
Input Offset Voltage	$R_S \leq 50\ k\Omega$				10	mV
Average Temperature Coefficient of Input Offset Voltage				6.0	30	μV/°C
Input Offset Current					70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$			0.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$			0.02	0.6	nA/°C
Input Bias Current					300	nA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$ $R_L \geq 2\ k\Omega$		15			V/mV
Output Voltage Swing	$V_S = \pm 15\ V$	$R_L = 10\ k\Omega$	±12	±14		V
		$R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15\ V$		±12			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		70	96		dB

Guaranteed Performance Curves for μA307

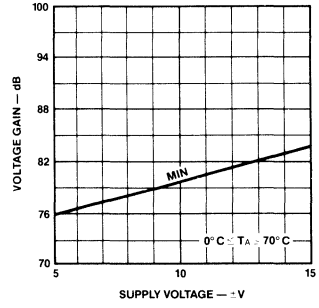
Input Voltage Range vs Supply Voltage



Output Swing vs Supply Voltage

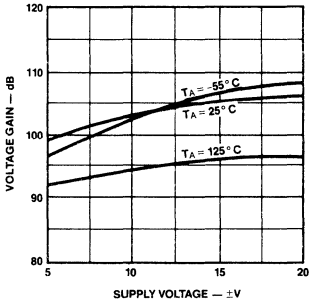


Voltage Gain vs Supply Voltage

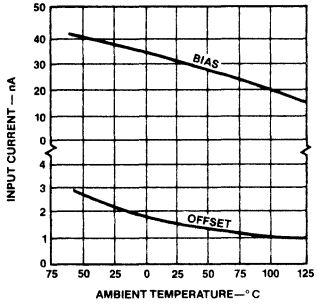


Typical Performance Curves for μA107 and μA207

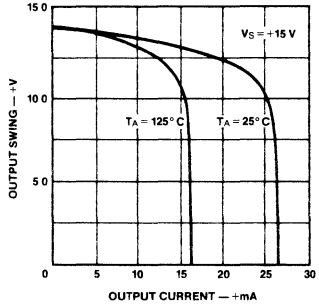
Voltage Gain vs Supply Voltage



Input Current vs Supply Voltage

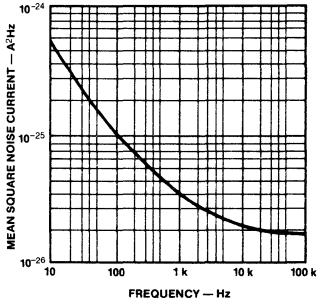


Current Limiting

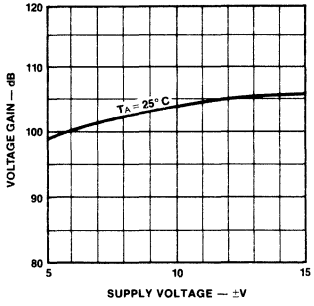


Typical Performance Curves for μA307

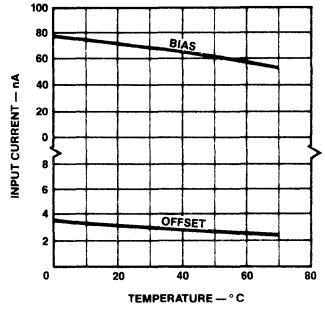
Input Noise Current vs Frequency



Voltage Gain vs Supply Voltage

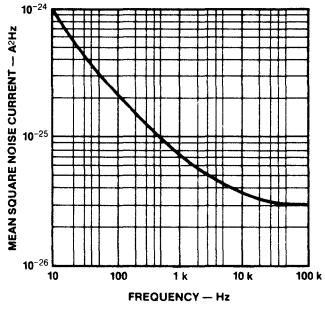


Input Current vs Ambient Temperature

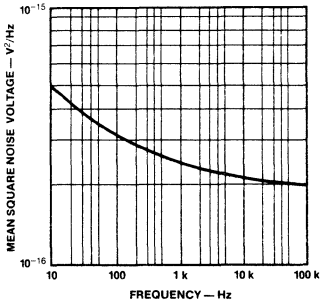


Typical Performance Curves for μA307 (Cont.)

Current Limiting

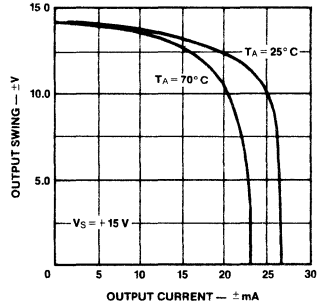


Input Noise Current vs Frequency



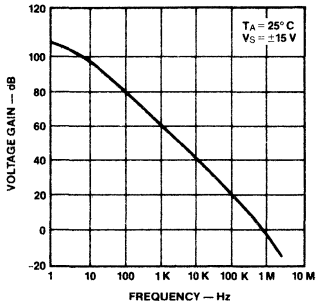
Typical Performance Curves for μA107, μA207, μA307 (Cont.)

Input Noise Voltage vs Frequency

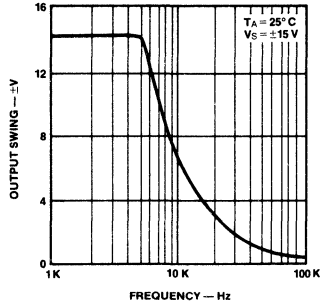


Typical Performance Curves for μA107, μA207 and μA307 (Cont.)

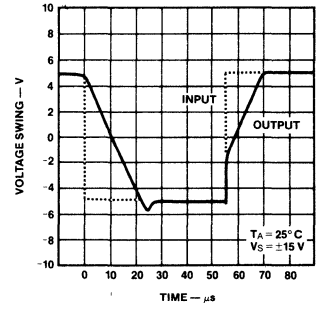
Open Loop Frequency Response



Large Signal Frequency Response

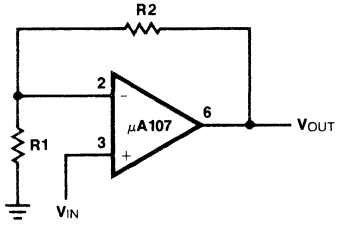


Voltage Follower Pulse Response



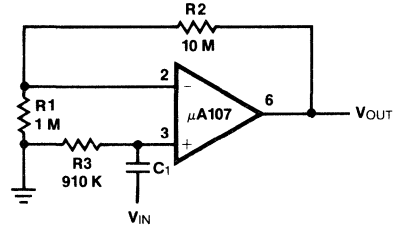
Typical Applications

Non-Inverting Amplifier



$$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$$

Non-Inverting AC Amplifier

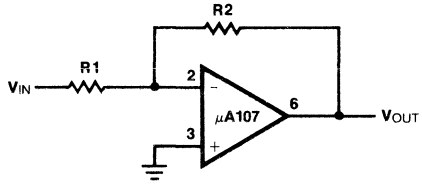


$$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$$

$$R_{IN} = R_3$$

$$R_3 = R_1 R_2$$

Inverting Amplifier



$$V_{OUT} = \frac{R_2}{R_1} V_{IN}$$

$$R_{IN} = R_1$$

FAIRCHILD

A Schlumberger Company

μA108/A • μA208/A • μA308/A Super Beta Operational Amplifiers

Linear Products

Description

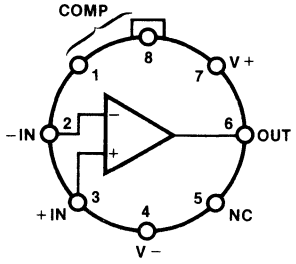
The μA108 Super Beta Operational Amplifier series is constructed using the Fairchild Planar epitaxial process. High input impedance, low noise, low-input offsets, and temperature drift are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low-drift performance. The μA108A series is specially selected for extremely low offset voltage and drift, and high common-mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high-speed sample-and-hold circuits and precision high-speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

- **GUARANTEED LOW INPUT OFFSET CHARACTERISTICS**
- **HIGH INPUT IMPEDANCE**
- **LOW OFFSET CURRENT**
- **LOW BIAS CURRENT**
- **OPERATION OVER WIDE SUPPLY RANGE**

Absolute Maximum Ratings

Supply Voltage	
μA108A, μA108, μA208A, μA208	±20 V
μA308A, μA308	±18 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
DIP	310 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA108A, μA108)	−55°C to +125°C
Industrial (μA208A, μA208)	−25°C to +85°C
Commercial (μA308A, μA308)	0°C to +70°C
Pin Temperature (Soldering)	
Metal (60 s)	300°C
DIP (10 s)	260°C
Output Short Circuit Duration (Note 4)	Indefinite

Connection Diagram
8-Pin Metal Package

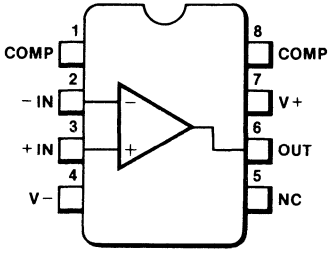


(Top View)

Order Information

Type	Package	Code	Part No.
μA108A	Metal	5W	μA108AHM
μA108	Metal	5W	μA108HM
μA208A	Metal	5W	μA208AHM
μA208	Metal	5W	μA208HM
μA308A	Metal	5W	μA308AHM
μA308	Metal	5W	μA308HM

Connection Diagram
8-Pin DIP



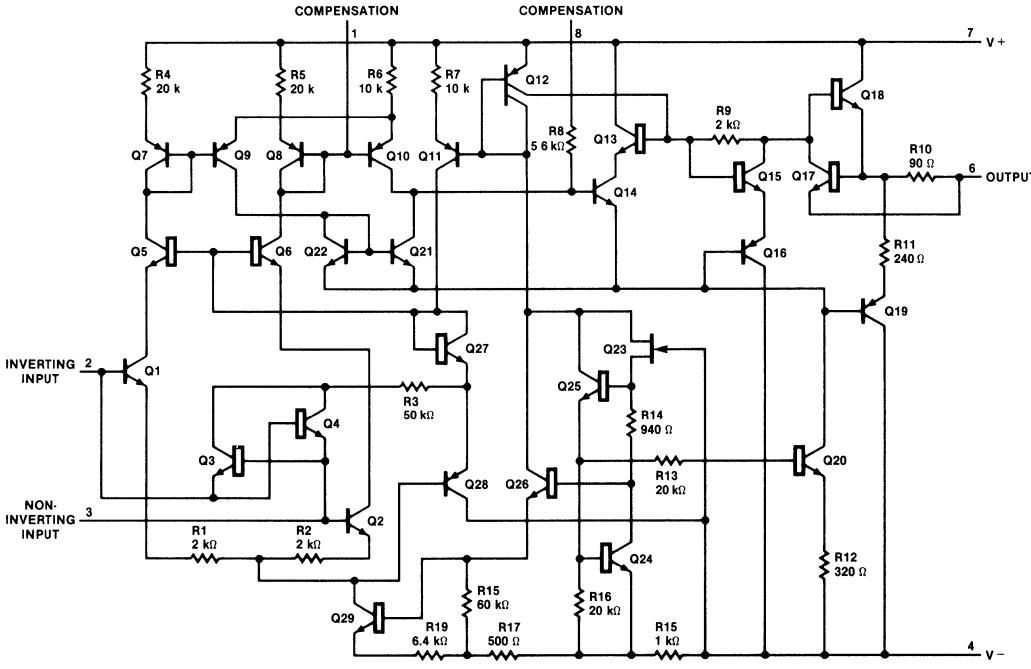
(Top View)

Order Information

Type	Package	Code	Part No.
μA308A	Molded	9T	μA308ATC
μA308	Molded	9T	μA308TC

See notes on following pages

Equivalent Circuit



Notes

1. Rating applies to ambient temperatures up to 70°C ambient derate linearly at 6.3 mW/°C for metal package, 8.3 mW/°C for the DIP.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless adequate limiting resistance is used.
3. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short circuit may be to either supply or ground. Rating applies to operation up to the maximum operating temperature range.

μA108/A and μA208/A
Electrical Characteristics Unless otherwise noted these specifications apply for supply voltages of $\pm 5.0V \leq V_S \leq \pm 20$ V, $T_A = +25°C$.

		μA108A μA208A			μA108 μA208			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{IO}	Input Offset Voltage		0.3	0.5		0.7	2.0	mV
I_{IO}	Input Offset Current		0.05	0.2		0.05	0.2	nA
I_{IB}	Input Bias Current		0.8	2.0		0.8	2.0	nA
r_i	Input Resistance	30	70		30	70		MΩ
I_{CC}, I_{EE}	Power Supply Currents $V_{CC} = +20$ V, $V_{EE} = -20$ V		±0.3	±0.6		±0.3	±0.6	mA
A_{VOL}	Large Signal Voltage Gain $V_{CC} = \lvert V_{EE} \rvert = +15$ V, $V_O = \pm 10$ V, $R_L \geq 10$ kΩ	80	300		50	300		V/mV
The following specifications apply over the operating temperature range. (Note 5)								
V_{IO}	Input Offset Voltage			1.0			3.0	mV
I_{IO}	Input Offset Current			0.4			0.4	nA
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leq T_A \leq T_A(max)$		1.0	5.0		3.0	15	μV/°C
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current		0.5	2.5		0.5	2.5	pA/°C
I_{IB}	Input Bias Current		0.8	3.0			3.0	nA
A_{VOL}	Large Signal Voltage Gain $V_{CC} = \lvert V_{EE} \rvert = +15$ V, $V_O = \pm 10$ V, $R_L = 10$ kΩ	40			25			V/mV
V_{IR}	Input Voltage Range $V_{CC} = \lvert V_{EE} \rvert = +15$ V	±13.5			±13.5			V
CMRR	Common-Mode Rejection Ratio	96	110		85	100		dB
PSSR	Power Supply Voltage Rejection Ratio	96	110		80	96		dB
V_{OR}	Output Voltage Range $V_{CC} = \lvert V_{EE} \rvert = +15$ V, $R_L = 10$ kΩ	±13	±14		±13	±14		V
I_{CC}, I_{EE}	Supply Current ($T_A = T_A$[max])		±0.15	±0.4		±0.15	±0.4	mA

Note

5 For the μA108/A specifications apply over $-55°C \leq T_A \leq 125°C$ For the μA208/A specifications apply over $-25°C \leq T_A \leq 85°C$.

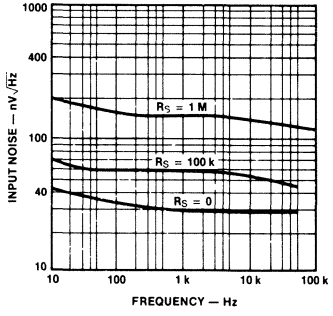
μA308/A

Electrical Characteristics Unless otherwise noted these specifications apply for supply voltages of $+5.0\ V \leq V_{CC} \leq +15\ V$ and $-5.0\ V \geq V_{EE} \geq -15\ V$, $T_A = +25°C$.

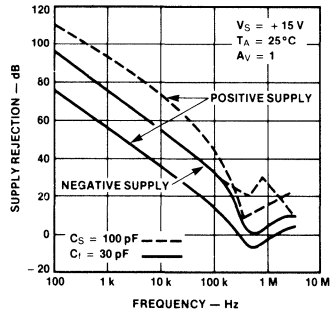
Symbol	Characteristic	μA308A			μA308			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage		0.3	0.5		2.0	7.5	mV
I_{IO}	Input Offset Current		0.2	1.0		0.2	1.0	nA
I_{IB}	Input Bias Current		1.5	7.0		1.5	7.0	nA
r_i	Input Resistance	10	40		10	40		MΩ
I_{CC}, I_{EE}	Power Supply Currents $V_{CC} = +15\ V$, $V_{EE} = -15\ V$		±0.3	±0.8		±0.3	±0.8	mA
A_{VOL}	Large Signal Voltage Gain $V_{CC} = +15\ V$, $V_{EE} = -15\ V$, $V_O = \pm 10\ V$, $R_L \geq 10\ k\Omega$	80	300		25	300		V/mV
The following specifications apply over $0°C \leq T_A \leq 70°C$								
V_{IO}	Input Offset Voltage			0.73			10	mV
I_{IO}	Input Offset Current			1.5			1.5	nA
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leq T_A \leq T_A(max)$		1.0	5.0		6.0	30	μV/°C
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current		2.0	10		2.0	10	pA/°C
I_{IB}	Input Bias Current			10			10	nA
A_{VOL}	Large Signal Voltage Gain $V_{CC} = +15\ V$, $V_{EE} = -15\ V$, $V_O = \pm 10\ V$, $R_L \geq 10\ k\Omega$	60			15			V/mV
V_{IR}	Input Voltage Range $V_{CC} = +15\ V$, $V_{EE} = -15\ V$	±13.5			±13.5			V
CMRR	Common-Mode Rejection Ratio $R_S \leq 50\ k\Omega$	96	110		80	100		dB
PSSR	Supply Voltage Rejection Ratio $R_S \leq 50\ k\Omega$	96	110		80	96		dB
V_{OR}	Output Voltage Range $V_{CC} = +15\ V$, $V_{EE} = -15\ V$, $R_L = 10\ k\Omega$	±13	±14		±13	±14		V

Typical Performance Curves for μA108 Series

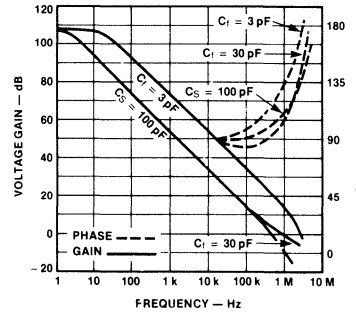
Input Noise Voltage as a Function of Frequency



Power Supply Rejection as a Function of Frequency

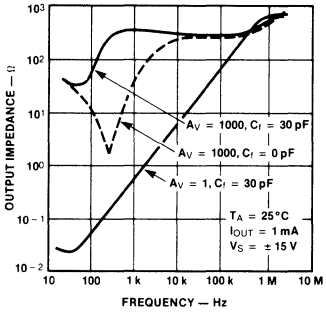


Open Loop Frequency Response

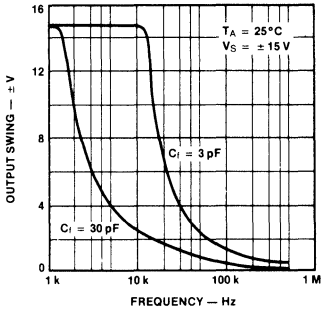


Typical Performance Curves for μA108 Series (Cont.)

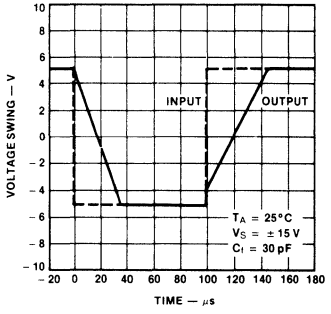
Closed Loop Output Impedance



Large Signal Frequency Response



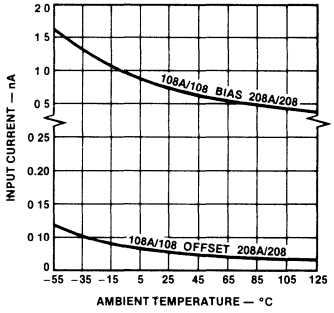
Voltage Follower Pulse Response



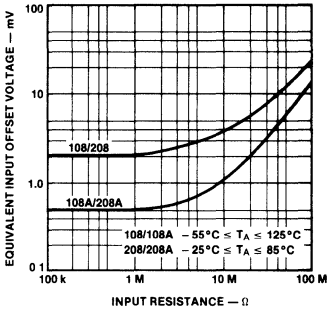
Typical Performance Curves for μA108A, μA108, μA208A and μA208 (Unless Otherwise Specified)

4

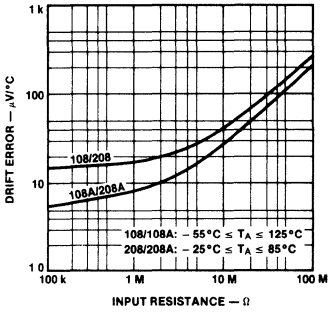
Input Currents as a Function of Ambient Temperature



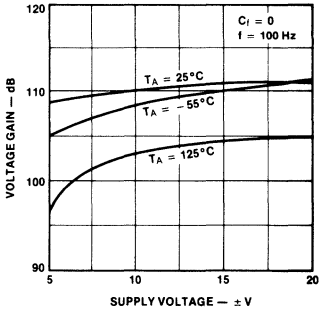
Maximum Offset Error



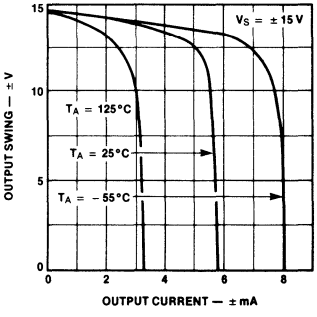
Maximum Drift Error



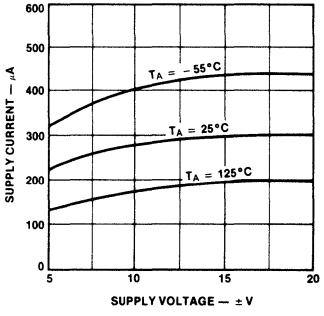
Voltage Gain as a Function of Supply Voltage μA108



Output Swing as a Function of Output Current μA108

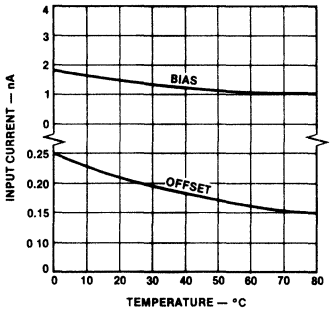


Supply Current as a Function of Supply Voltage μA108

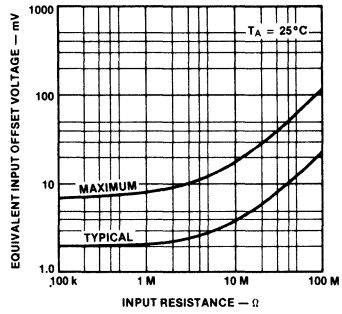


Typical Performance Curves for μA308A and μA308 (Unless Otherwise Specified)

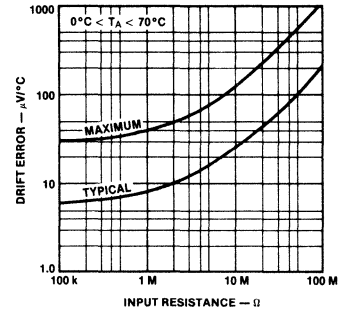
Input Current as a Function of Ambient Temperature



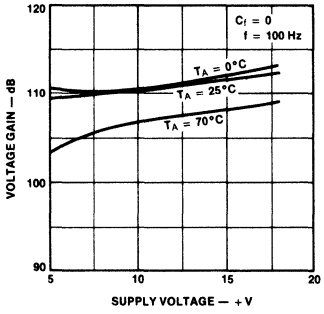
Maximum Offset Error μA308



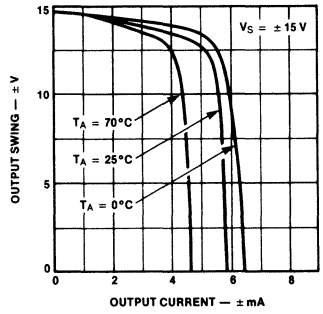
Maximum Drift Error μA308



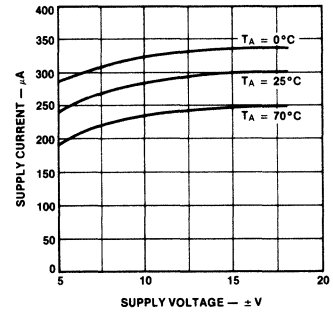
Voltage Gain as a Function of Supply Voltage



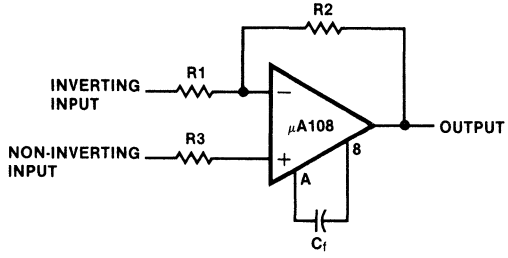
Output Swing as a Function of Output Current

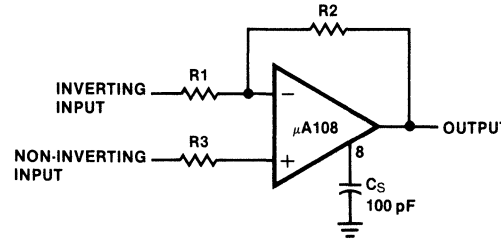


Supply Current as a Function of Supply Voltage



Standard Compensation Circuits

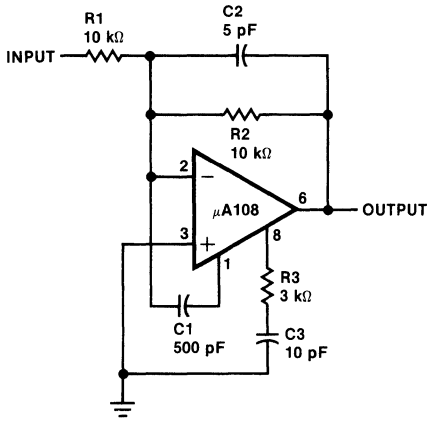




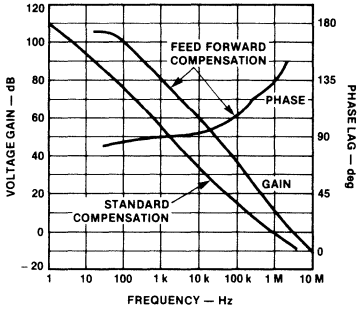
$$C_f \geq 30 \left(\frac{1}{1 + \frac{R_2}{R_1}} \right)$$

Feedforward Compensation Higher Slew Rate and Wider Bandwidth

Standard Feedforward



Open Loop Voltage Gain



Guarding

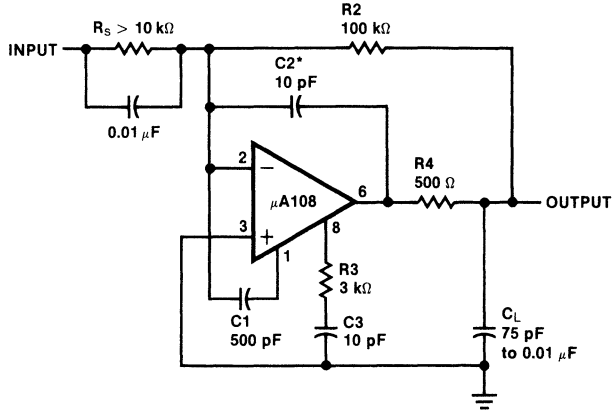
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the μA108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-pin TO-99 package is accomplished by using a 10-pin circle, with the pins of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard μA741 and μA101A pin configuration).

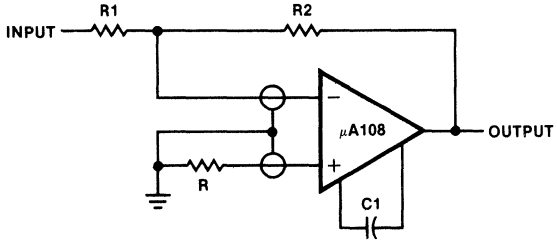
4

Feedforward Compensation for Decoupling Load Capacitance

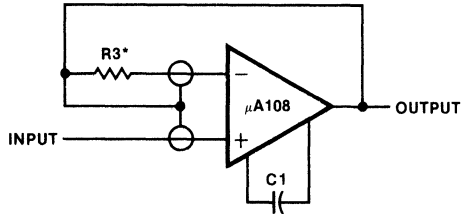


$$*C_2 > \frac{5 \times 10^5}{R_2}\ \text{pF}$$

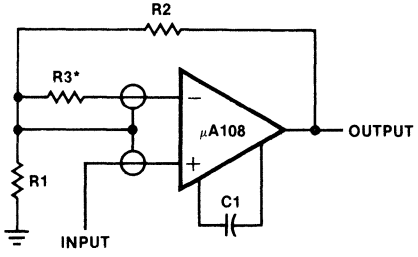
Inverting Amplifier



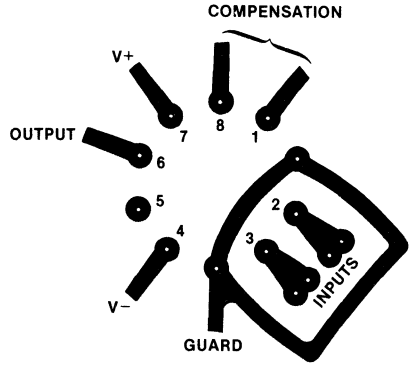
Follower



Non-Inverting Amplifier



Board Layout for Input Guarding With TO-99 Package



(Bottom View)

FAIRCHILD

A Schlumberger Company

μA318 High-Speed Operational Amplifier

Linear Products

Description

The μA318 is a Precision High-Speed Operational Amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing dc performance.

The μA318 has internal unity gain frequency compensation. This simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150 V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

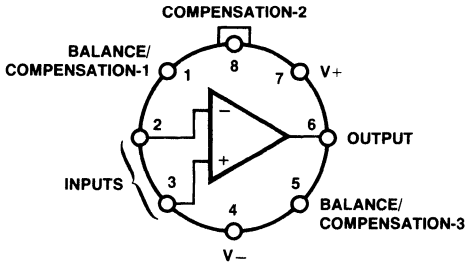
The high speed and fast settling time of this op amp makes it useful in a/d converters, oscillators, active filters, sample-and-hold circuits or general-purpose amplifiers. This device is easy to apply and offers a better ac performance than industry standards such as the μA709.

- **15 MHz SMALL SIGNAL BANDWIDTH**
- **GUARANTEED 50 V/μs SLEW RATE**
- **MAXIMUM BIAS CURRENT OF 500 nA**
- **OPERATES FROM SUPPLIES OF ±5 V TO ±20 V**
- **INTERNAL FREQUENCY COMPENSATION**
- **INPUT AND OUTPUT OVERLOAD PROTECTED**
- **PIN COMPATIBLE WITH GENERAL PURPOSE OP AMPS**

Absolute Maximum Ratings

Supply Voltage	±20 V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering, 60 s)	300°C

Connection Diagram
8-Pin Metal Package



(Top View)

Order Information

Type	Package	Code	Part No.
μA318	Metal	5W	μA318HC

4

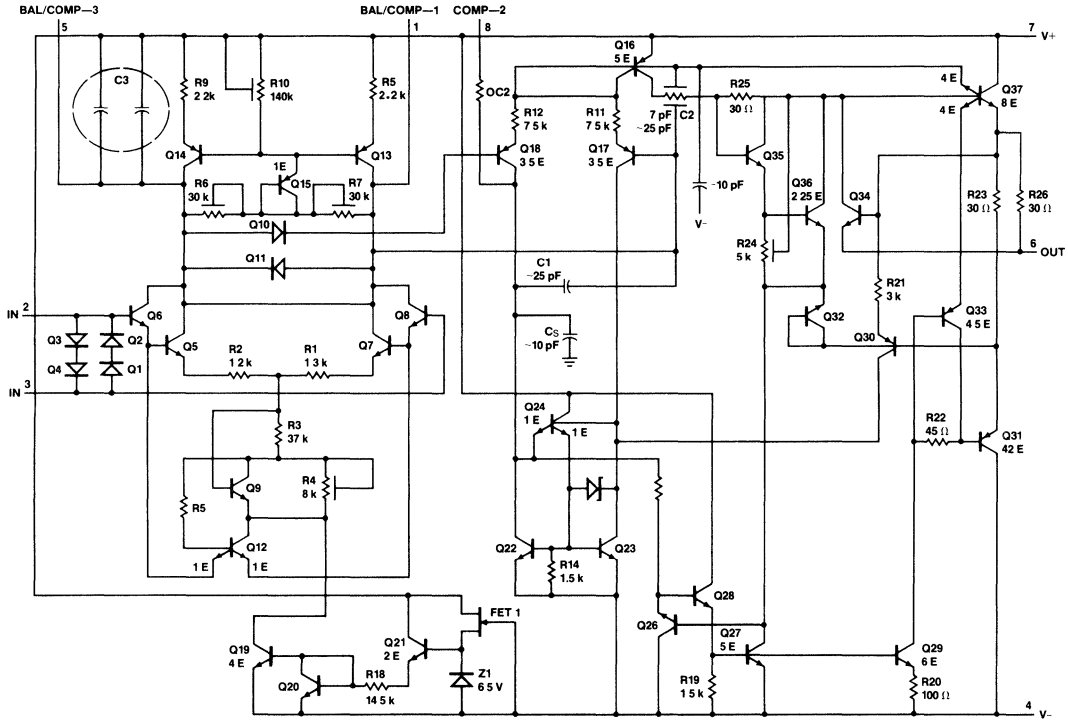
Notes

1 The maximum junction temperature of the μA318 is 150°C for operating at elevated temperatures. The package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case.

2 The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.

3 For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Equivalent Circuit



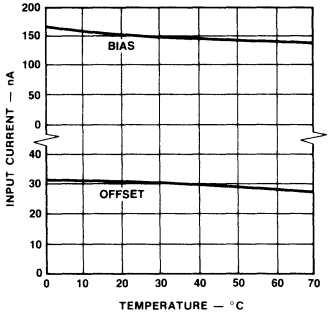
μA318
Electrical Characteristics $\pm 5\ V \leq VS \leq \pm 20\ V$, $T_A = +25°C$

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage			4	10	mV
Input Offset Current			30	200	nA
Input Bias Current			150	500	nA
Input Resistance		0.5	3		MΩ
Supply Current			5	10	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$	25	200		V/mV
Slew Rate	$V_S = \pm 15\ V$, $A_V = 1$	50	70		V/μs
Small Signal Bandwidth	$V_S = \pm 15\ V$		15		MHz
The following specifications apply for $0°C < T_A < +70°C$					
Input Offset Voltage				15	mV
Input Offset Current				300	nA
Input Bias Current				750	nA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L \geq 2\ k\Omega$	20			V/mV
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L = 2\ k\Omega$	±12	±13		V
Input Voltage Range	$V_S = \pm 15\ V$	±11.5			V
Common-Mode Rejection Ratio		70	100		dB
Supply Voltage Rejection Ratio		65	80		dB

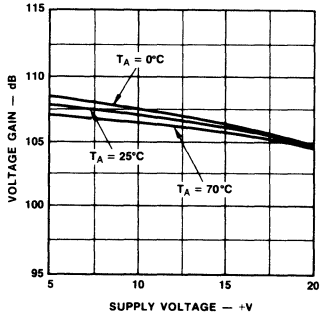
4

Typical Performance Curves

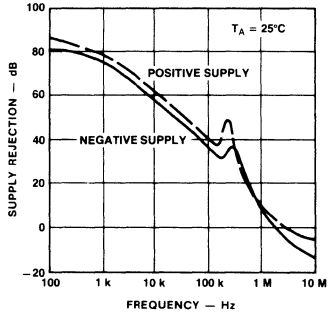
Input Current



Voltage Gain

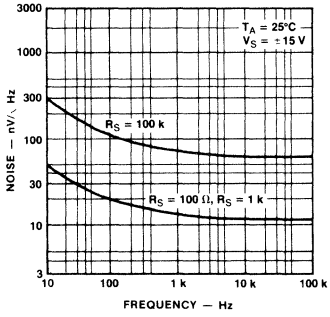


Power Supply Rejection

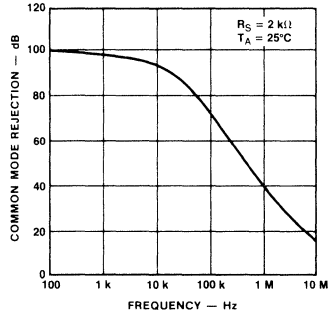


Typical Performance Curves (Cont.)

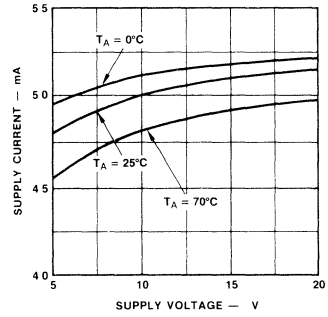
Input Noise Voltage



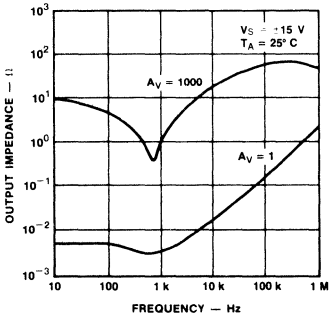
Common Mode Rejection



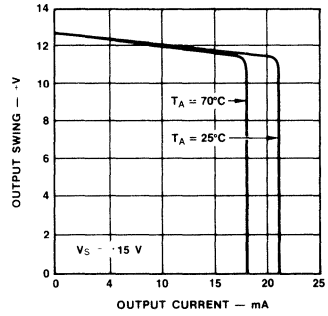
Supply Current



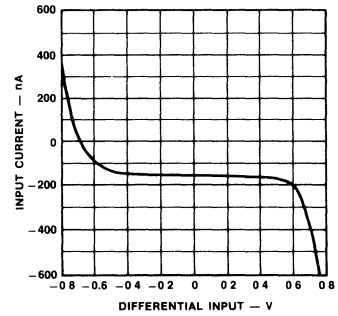
Closed Loop Output Impedance



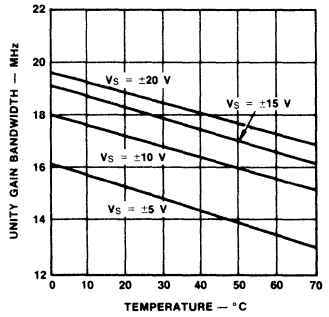
Current Limiting



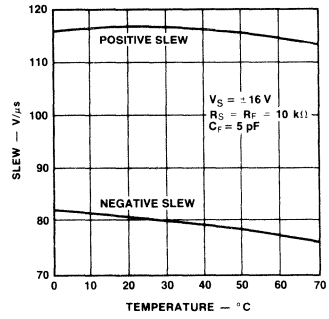
Input Current



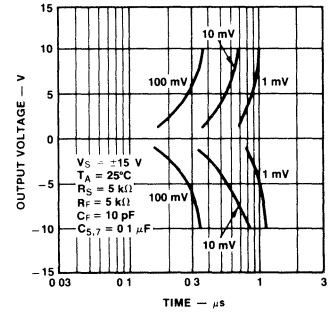
Unity Gain Bandwidth



Voltage Follower Slew Rate

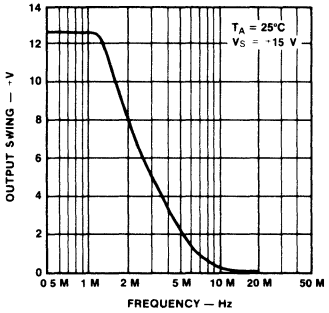


Inverter Settling Time

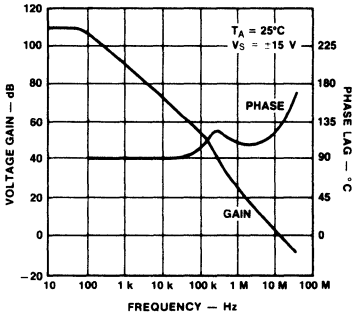


Typical Performance Curves (Cont.)

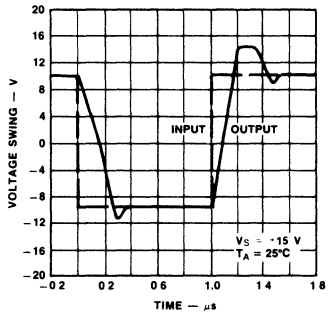
Large Signal Frequency Response



Open Loop Frequency Response

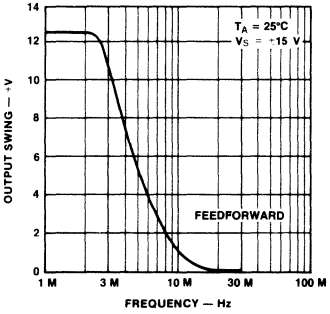


Voltage Follower Pulse Response

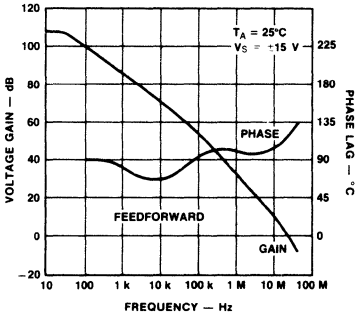


4

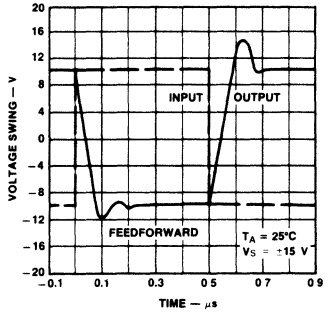
Large Signal Frequency Response



Open Loop Frequency Response

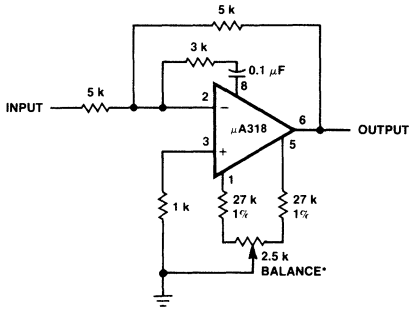


Inverter Pulse Response



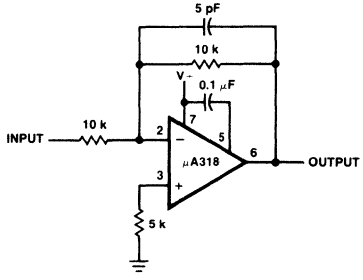
Auxiliary Circuits

Feedforward Compensation For Greater Inverting Slew Rate



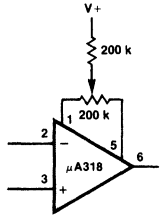
Slew rate typically 150 V/μs.
Balance circuit necessary for increased slew.

Compensation for Minimum Settling Time

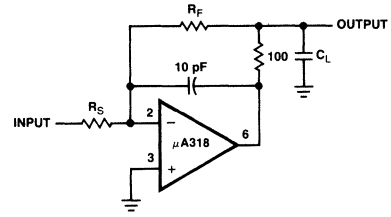


Slew and settling time to 0.1% for a 10 V step change is 800 ns.

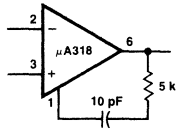
Offset Balancing



Isolating Large Capacitive Loads

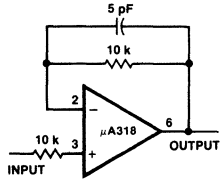


Overcompensation

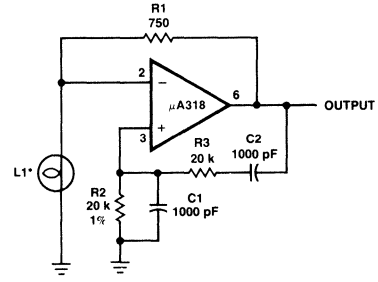


Typical Applications

Fast Voltage Follower



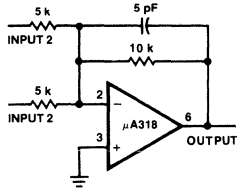
Wein Bridge Sine Wave Oscillator



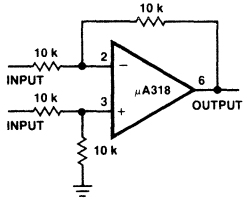
L1 = 10 V - 14 mA bulb ELDEMA 1869
R2 = R3
C1 = C2

$$f = \frac{1}{2\pi R2\ C1}$$

Fast Summing Amplifier



Differential Amplifier



FAIRCHILD

A Schlumberger Company

μA124 • μA224 • μA324 μA2902 Quad Operational Amplifiers

Linear Products

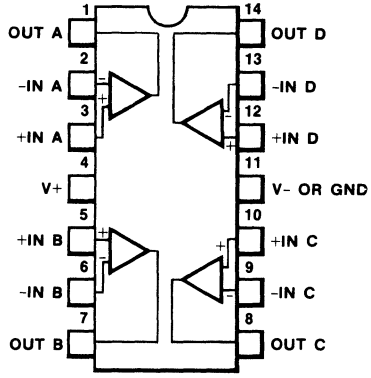
Description

The μA124 series of Quad Operational Amplifiers consists of four independent high-gain, internally frequency-compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage. They are constructed using the Fairchild Planar epitaxial process.

- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **OUTPUT VOLTAGE CAN SWING TO GROUND OR NEGATIVE SUPPLY**
- **FOUR INTERNALLY COMPENSATED OPERATIONAL AMPLIFIERS IN A SINGLE PACKAGE**
- **WIDE POWER SUPPLY RANGE SINGLE OF 3.0 V to 30 V DUAL SUPPLY OF ± 1.5 V to ± 16 V**
- **POWER DRAIN SUITABLE FOR BATTERY OPERATION**

Connection Diagram

14-Pin DIP

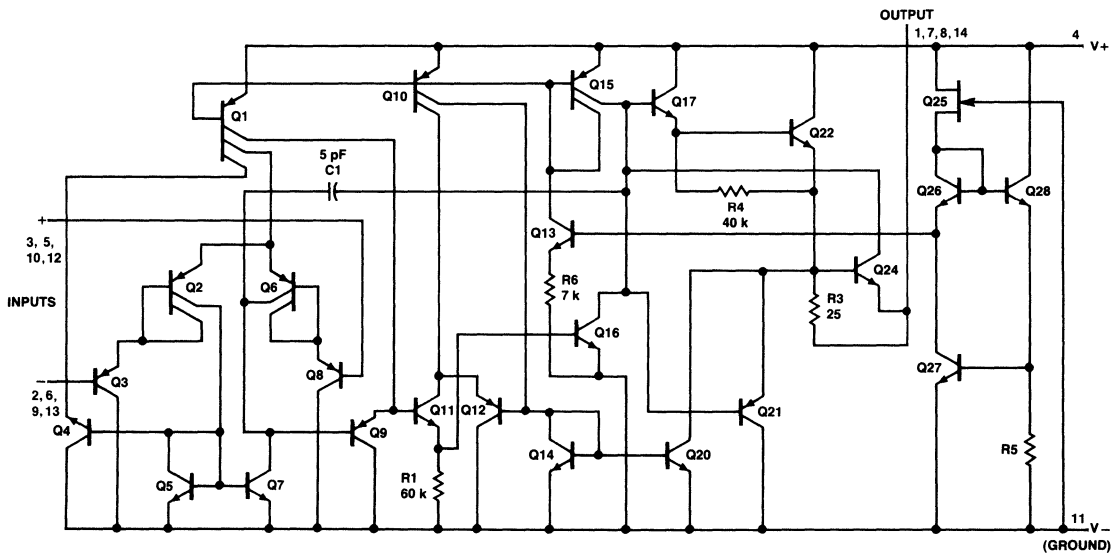


(Top View)

Order Information

Type	Package	Code	Part No.
μA124	Ceramic DIP	6A	μA124DM
μA224	Molded DIP	6A	μA224PV
μA224	Ceramic DIP	9A	μA224DV
μA324	Molded DIP	6A	μA324PC
μA324	Ceramic DIP	9A	μA324DC
μA2902	Molded DIP	9A	μA2902PV

Equivalent Circuit (1/4 of circuit shown)



Absolute Maximum Ratings

Supply Voltage Between V+ and V−	32
Differential Input Voltage (Note 1)	32
Input Voltage (V−) (Note 1)	−0.3 V (V−) to V+
Internal Power Dissipation (Note 2)	670 mW
Operating Temperature Range	
μA124	−55°C to +125°C
μA224	−25°C to +85°C
μA324	0°C to +70°C
μA2902	−40°C to +85°C
Storage Temperature Range	
Molded DIP	−55°C to +125°C
Ceramic DIP	−65°C to +150°C
Pin Temperature (Soldering)	
Molded DIP (10 s)	260°C
Ceramic DIP (60 s)	300°C

Notes

1. T_{low} = −55°C for μA124 = −40°C for μA2902 = −25°C for μA224 = 0°C for μA324; T_{high} = +125°C for μA124 = +85°C for μA2902 and μA224 = +70°C for μA324
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} − 1.5 V, but either or both inputs can go to +32 V without damage (+26 V for μA2902).
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

μA124, μA224 and μA324
Electrical Characteristics V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C unless otherwise noted.

Symbol	Characteristic	Condition	μA124/μA224			μA324			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	V_{CC} = 5.0 V to 30 V V_{IC} = 0 V to V_{CC} −1.5 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω $T_A = T_{high}$ to T_{low} (Note 1)		2.0	5.0 7.0		2.0	7.0 9.0	mV
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$T_A = T_{high}$ to T_{low} (Note 1)		7.0			7.0		μV/°C
I_{IO}	Input Offset Current	$T_A = T_{high}$ to T_{low} (Note 1)		3.0	30 ±100		5.0	50 150	nA
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	$T_A = T_{high}$ to T_{low} (Note 1)		10			10		pA/°C
I_{IB}	Input Bias Current	$T_A = T_{high}$ to T_{low} (Note 1)		−45 −40	−150 −300		−45 −50	−250 −500	nA
V_{ICR}	Input Common-Mode Voltage Range (Note 2)	V_{CC} = 30 V V_{CC} = 30 V $T_A = T_{high}$ to T_{low} (Note 1)	0 0		28.5 28	0 0		28.5 28	V
V_{IDR}	Differential Input Voltage Range				V_{CC}			V_{CC}	V
A_{VOL}	Large Signal Open-Loop Voltage Gain	R_L = 2.0 kΩ, V_{CC} = 15 V, $T_A = T_{high}$ to T_{low} (Note 1)	50 25	100		25 15	100		V/mV
	Channel Separation	1.0 kHz ≤ f ≤ 20 kHz, Input Referenced		−120			−120		dB
CMMR	Common-Mode Rejection Ratio	R_S ≤ 10 kΩ	70	85		65	70		dB
PSSR	Power Supply Rejection Ratio		65	100		65	100		dB
V_{OH}	Output Voltage—High	($T_A = T_{high}$ to T_{low}) (Note 1) V_{CC} = 30 V, R_L = 2 kΩ V_{CC} = 30 V, R_L = 10 kΩ	 26 27	 28		 26 27	 28		V
V_{OL}	Output Voltage—Low	V_{CC} = 5.0 V, R_L = 10 kΩ, $T_A = T_{high}$ to T_{low} (Note 1)		5.0	20		5.0	20	mV
I_{O+}	Output Source Current	(V_{ID} = +1.0 V, V_{CC} = 15 V) $T_A = T_{high}$ to T_{low} (Note 1)	20 10	40 20		20 10	40 20		mA
I_{O-}	Output Sink Current	V_{ID} = −1.0 V, V_{CC} = 15 V $T_A = T_{high}$ to T_{low} (Note 1) V_{ID} = −1.0 V, V_O = 200 mV	10 5 12	20 8 50		10 5 12	20 8 50		mA mA μA
I_{OS}	Output Short Circuit to Ground (Note 3)			40	60		40	60	mA
I_{CC}	Power Supply Current	($T_A = T_{high}$ to T_{low}) (Note 1) V_{CC} = 30 V, V_O = 0 V, R_L = ∞ V_{CC} = 5 V, V_O = 0 V, R_L = ∞		 1.5 0.7	 3.0 1.2		 1.5 0.7	 3.0 1.2	mA

Notes

1. T_{low} = −55°C for μA124 = −40°C for μA2902 = −25°C for μA224 = 0°C for μA324; T_{high} = +125°C for μA124 = +85°C for μA2902 and μA224 = +70°C for μA324
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} − 1.5 V, but either or both inputs can go to +32 V without damage (+26 V for μA2902).
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

μA2902
Electrical Characteristics (Cont.) V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C unless otherwise noted.

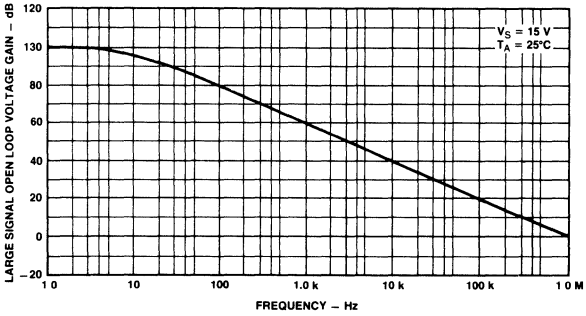
Symbol	Characteristic	Condition	μA2902 Min	μA2902 Typ	μA2902 Max	Unit
V_{IO}	Input Offset Voltage	V_{CC} = 5.0 V to 26 V, V_{IC} = 0 V to V_{CC} −1.5 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω T_A = 25°C T_A = T_{high} to T_{low} (Note 1)		2.0	7.0 10	mV
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	T_A = T_{high} to T_{low} (Note 1)		7.0		μV/°C
I_{IO}	Input Offset Current	T_A = T_{high} to T_{low} (Note 1)		5.0 45	50 200	nA
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	T_A = T_{high} to T_{low} (Note 1)		10		pA/°C
I_{IB}	Input Bias Current	T_A = T_{high} to T_{low} (Note 1)		−45 −50	−250 −500	nA
V_{ICR}	Input Common-Mode Voltage Range (Note 2)	V_{CC} = 26 V V_{CC} = 26 V, T_A = T_{high} to T_{low}	0 0		24.5 24	V
V_{IDR}	Differential Input Voltage Range				V_{CC}	V
A_{VOL}	Large Signal Open-Loop Voltage Gain	R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing, T_A = T_{high} to T_{low} (Note 1)	15	100		V/mV
	Channel Separation	1.0 kHz ≤ f ≤ 20 kHz, Input Referenced		−120		dB
CMMR	Common-Mode Rejection Ratio	R_S ≤ 10 kΩ	50	70		dB
PSSR	Power Supply Rejection Ratio		50	100		dB
V_{OH}	Output Voltage—High	(T_A = T_{high} to T_{low}) (Note 1) V_{CC} = 26 V, R_L = 2 kΩ V_{CC} = 26 V, R_L = 10 kΩ	 22 23	 24		V
V_{OL}	Output Voltage—Low	V_{CC} = 5.0 V, R_L ≤ 10 kΩ, T_A = T_{high} to T_{low} (Note 1)		5.0	100	mV
I_{O+}	Output Source Current	(V_{ID} = +1.0 V, V_{CC} = 15 V) T_A = T_{high} to T_{low} (Note 1)	20 10	40 20		mA
I_{O-}	Output Sink Current	V_{ID} = −1.0 V, V_{CC} = 15 V T_A = T_{high} to T_{low} (Note 1)	10 5	20 8		mA
I_{OS}	Output Short Circuit to Ground (Note 3)			40	60	mA
I_{CC}	Power Supply Current	(T_A = T_{high} to T_{low}) (Note 1) V_{CC} = 26 V, V_O = 0 V, R_L = ∞ V_{CC} = 5 V, V_O = 0 V, R_L = ∞		1.5 0.7	3.0 1.2	mA

Notes

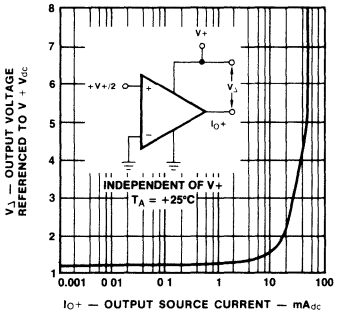
1. T_{low} = −55°C for μA124 = −40°C for μA2902 = −25°C for μA224 = 0°C for μA324; T_{high} = +125°C for μA124 = +85°C for μA2902 and μA224 = +70°C for μA324
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} − 1 5 V, but either or both inputs can go to +32 V without damage (+26 V for μA2902).
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Typical Performance Curves

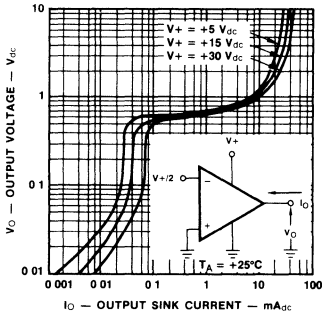
Large Signal Open Loop Voltage Gain as a Function of Frequency



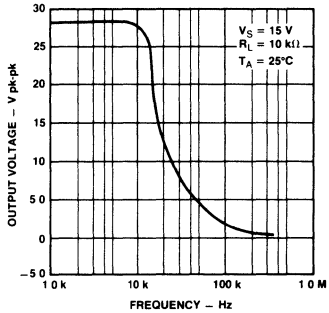
Output Characteristics Current Sourcing



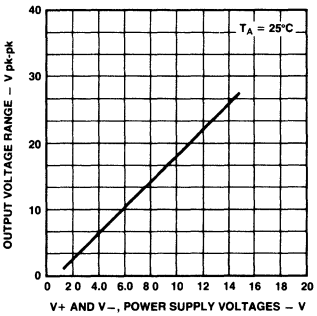
Output Characteristics Current Sinking



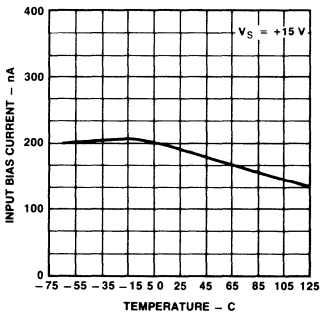
Output Voltage as a Function of Frequency



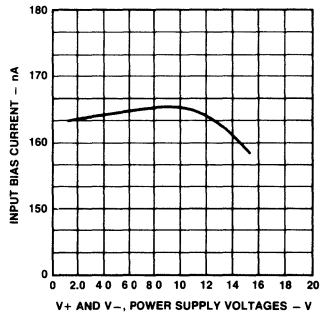
Output Swing as a Function of Supply Voltage



Input Bias Current as a Function of Temperature



Input Bias Current as a Function of Supply Voltage



FAIRCHILD

A Schlumberger Company

μA148 • μA248 • μA348 Quad Operational Amplifiers

Linear Products

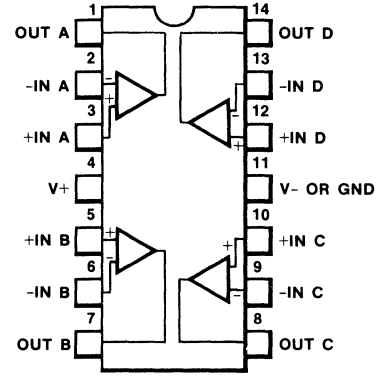
Description

The μA148 series is a true quad μA741. It consists of four independent, high-gain, internally-compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar μA741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single μA741 type op amp.

Other features include input offset currents and input bias current which are much less than those of a standard μA741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

- **μA741 OP AMP OPERATING CHARACTERISTICS**
- **LOW SUPPLY CURRENT DRAIN**
- **CLASS AB OUTPUT STAGE—NO CROSSOVER DISTORTION**
- **PIN COMPATIBLE WITH THE μA324 & μA3403**
- **LOW INPUT OFFSET VOLTAGE—1 mV TYP**
- **LOW INPUT OFFSET CURRENT—4 nA TYP**
- **LOW INPUT BIAS CURRENT—30 nA TYP**
- **GAIN BANDWIDTH PRODUCT FOR μA148 (UNITY GAIN)—1.0 MHz TYP**
- **HIGH DEGREE OF ISOLATION BETWEEN AMPLIFIERS—120 dB**
- **OVERLOAD PROTECTION FOR INPUTS AND OUTPUTS**

Connection Diagram
14 Pin DIP



(Top View)

Order Information

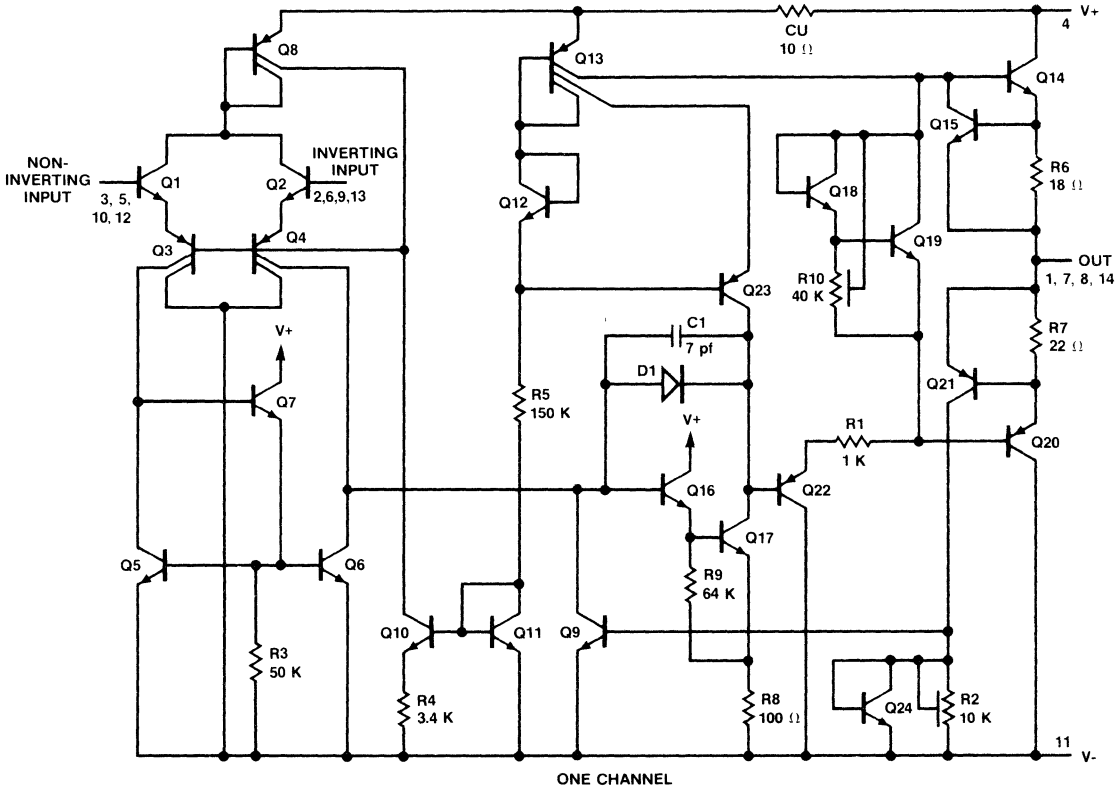
Type	Package	Code	Part No.
μA148	Ceramic DIP	6A	μA148DM
μA248	Ceramic DIP	6A	μA248DC
μA348	Ceramic DIP	6A	μA348DC
μA348	Molded DIP	9A	μA348PC

Absolute Maximum Ratings

	μA148	μA248	μA348
Supply Voltage	±22 V	±18 V	±18 V
Differential Input Voltage	±44V	±36 V	±36 V
Input Voltage	±22 V	±18 V	±18 V
Output Short-Circuit Duration (Note 1)	continuous	continuous	continuous
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{JA}), (Note 2)			
Molded DIP P_D	—	700 mW	700 mW
θ_{JA}	—	150°C	150°C/W
Ceramic DIP P_D	670 mW	670 mW	670 mW
θ_{JA}	100°C/W	100°C/W	100°C/W
Operating Temperature	$-55°C < T_A < +125°C$	$-25°C < T_A < +85°C$	$0°C < T_A < +70°C$
Storage Temperature	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Pin Temperature (Soldering)			
Molded DIP (10 s)	—	260°C	260°C
Ceramic DIP (60 s)	300°C	300°C	300°C

Notes on following pages

Equivalent Circuit (1/4 of Circuit Shown)



ONE CHANNEL

Notes

1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
2. The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{J\,(MAX)} - T_A)/\theta_{JA}$ or the 25°C $P_{D\,(MAX)}$, whichever is less.

μA148 and μA248

DC Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise noted

Characteristic	Condition	μA148 Min	μA148 Typ	μA148 Max	μA248 Min	μA248 Typ	μA248 Max	Unit
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0		1.0	6.0	mV
Input Offset Current			4	25		4	50	nA
Input Bias Current			30	100		30	200	nA
Input Resistance		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers			2.4	3.6		2.4	4.5	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L \geq 2$ kΩ	50	160		25	160		V/mV
Amplifier to Amplifier Coupling	f = 1 Hz to 20 kHz (Input Referred)		−120			−120		dB
Output Short-Circuit Current			25			25		mA
The following specifications apply over the operating Temperature Range								
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0			7.5	mV
Input Offset Current				75			125	nA
Input Bias Current				325			500	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	25			15			V/mV
Output Voltage Swing	$R_L = 10$ kΩ	±12	±13		±12	±13		V
	$R_L = 2$ kΩ	±10	±12		±10	±12		V
Input Voltage Range		±12			±12			V
Common-Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection	$R_S \leq 10$ kΩ	77	96		77	96		dB

AC Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise noted

Small Signal Bandwidth			1.0			1.0		MHz
Phase Margin	Av = 1		60			60		degrees
Slew Rate	Av = 1		0.5			0.5		V/μs

μA348

DC Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise noted

Characteristic	Condition	μA348 Min	μA348 Typ	μA348 Max	Unit
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current			4	50	nA
Input Bias Current			30	200	nA
Input Resistance		0.8	2.5		MΩ
Supply Current All Amplifiers			2.4	4.5	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L \geq 2$ kΩ	25	160		V/mV
Amplifier to Amplifier Coupling	f = 1 Hz to 20 kHz (Input Referred)		−120		dB
Output Short-Circuit Current			25		mA
The following specifications apply over the operating temperature Range					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				100	nA
Input Bias Current				400	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	15			V/mV
Output Voltage Swing	$R_L = 10$ kΩ	±12	±13		V
	$R_L = 2$ kΩ	±10	±12		V
Input Voltage Range		±12			V
Common-Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection	$R_S \leq 10$ kΩ	77	96		dB

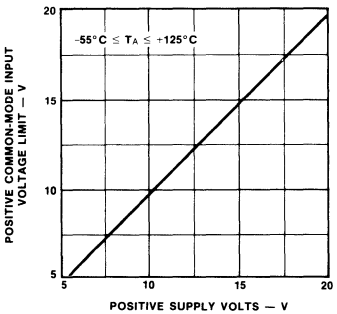
μA348
AC Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise noted

Small Signal Bandwidth			1.0		MHz
Phase Margin	Av = 1		60		degrees
Slew Rate	Av = 1		0.5		V/μs

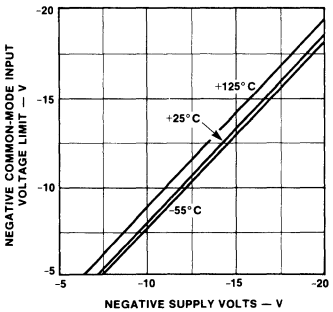
Note
μA148, 248, 348 are capable of driving 100 pF capacitive load.

Typical Performance Curves

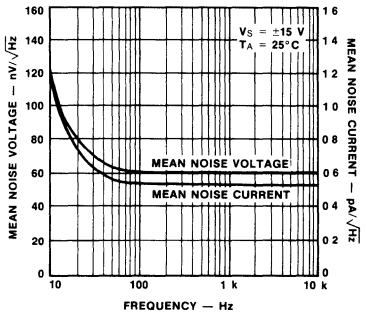
Positive Common Mode Input Voltage Limit as a Function of Supply Voltage



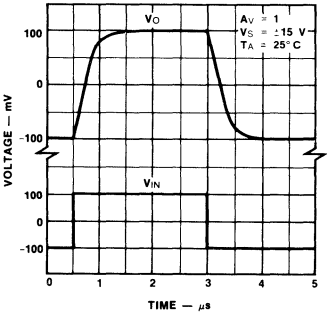
Negative Common Mode Input Voltage Limit as a Function of Supply Voltage



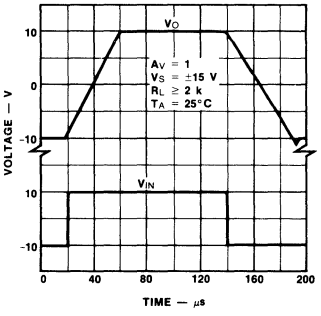
Input Noise Voltage and Noise Current as a Function of Frequency



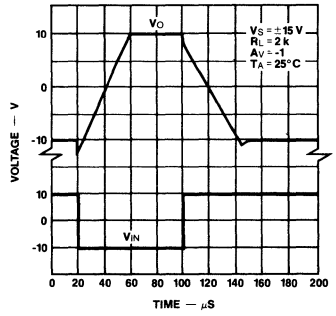
Small Signal Pulse Response



Large Signal Pulse Response

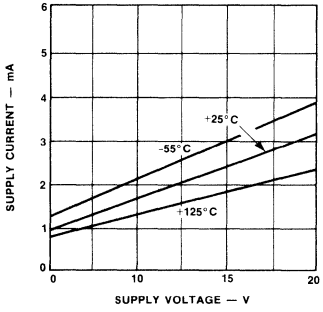


Inverting Large Signal Pulse Response

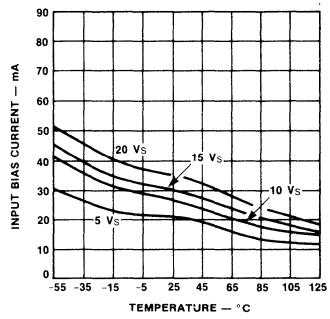


Typical Performance Curves (Cont.)

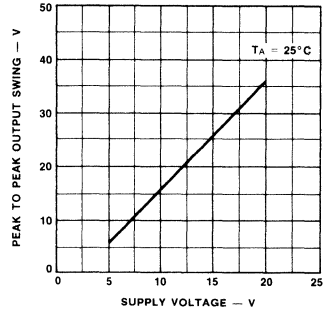
Supply Current as a Function of Power Supply Voltage



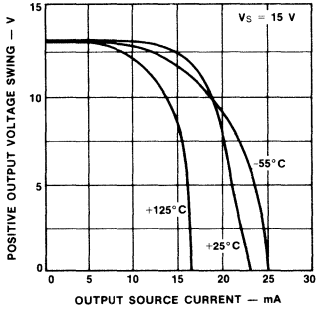
Input Bias Current as a Function of Ambient Temperature



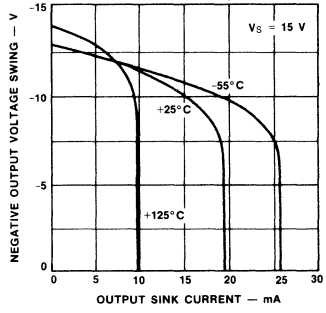
Output Voltage Swing as a Function of Supply Voltage



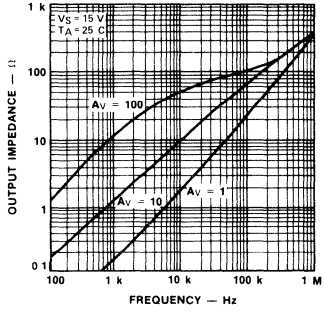
Output Voltage as a Function of Source Current



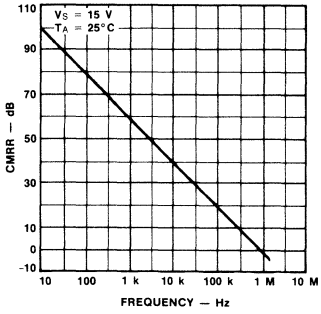
Output Voltage as a Function of Sink Current



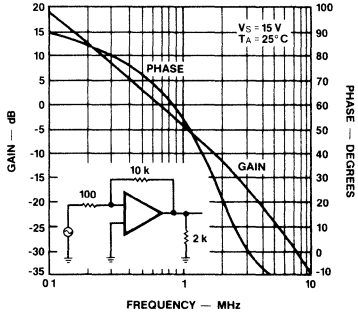
Output Impedance as a Function of Frequency



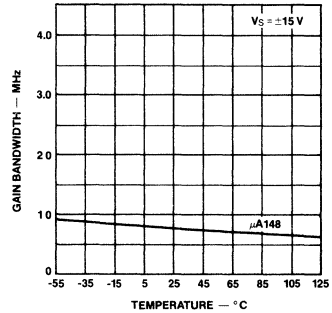
CMRR and Open Loop Frequency Response as a Function of Frequency



Gain as a Function of Frequency



Gain Band Width as a Function of Temperature



FAIRCHILD

A Schlumberger Company

μA1458 • μA1558 Dual Internally Compensated Operational Amplifiers

Linear Products

Description

The μA1458/μA1558 are a monolithic pair of Internally Compensated High Performance Amplifiers constructed using the Fairchild Planar epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA1458/μA1558 ideal for use as voltage followers. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

The μA1458/μA1558 are short-circuit protected and require no external components for frequency compensation. The internal 6 db/octave roll-off insures stability in closed loop applications. For single amplifier performance, see the μA741 data sheet.

The Fairchild μA1458/μA1558 slew rate has been improved to 0.8/μs typical.

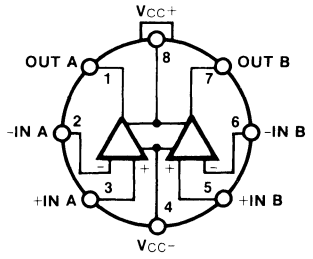
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**
- **MINI DIP PACKAGE**

Absolute Maximum Ratings

Supply Voltage	
Military (μA1558)	±22 V
Commercial (μA1458 and μA1458C)	±18 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
DIP	310 mW
Differential Input Voltage (Note 2)	±30 V
Common-Mode Input Swing (Note 2)	±15 V
Output Short Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA1558)	−55°C to +125°C
Commercial (μA1458 and μA1458C)	0°C to 70°C
Pin Temperature (Soldering, 60 s)	
Metal Package	300°C
Mini DIP (Soldering, 10 s)	260°C

Notes on following pages.

Connection Diagram
8-Pin Metal Package

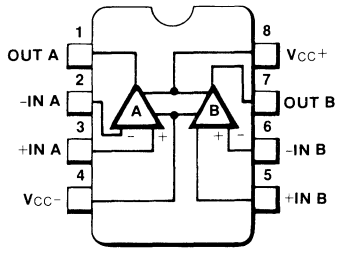


(Top View)

Order Information

Type	Package	Code	Part No.
μA1458	Metal	5W	μA1458HC
μA1458C	Metal	5W	μA1458CHC
μA1558	Metal	5W	μA1558HM

Connection Diagram
8-Pin DIP

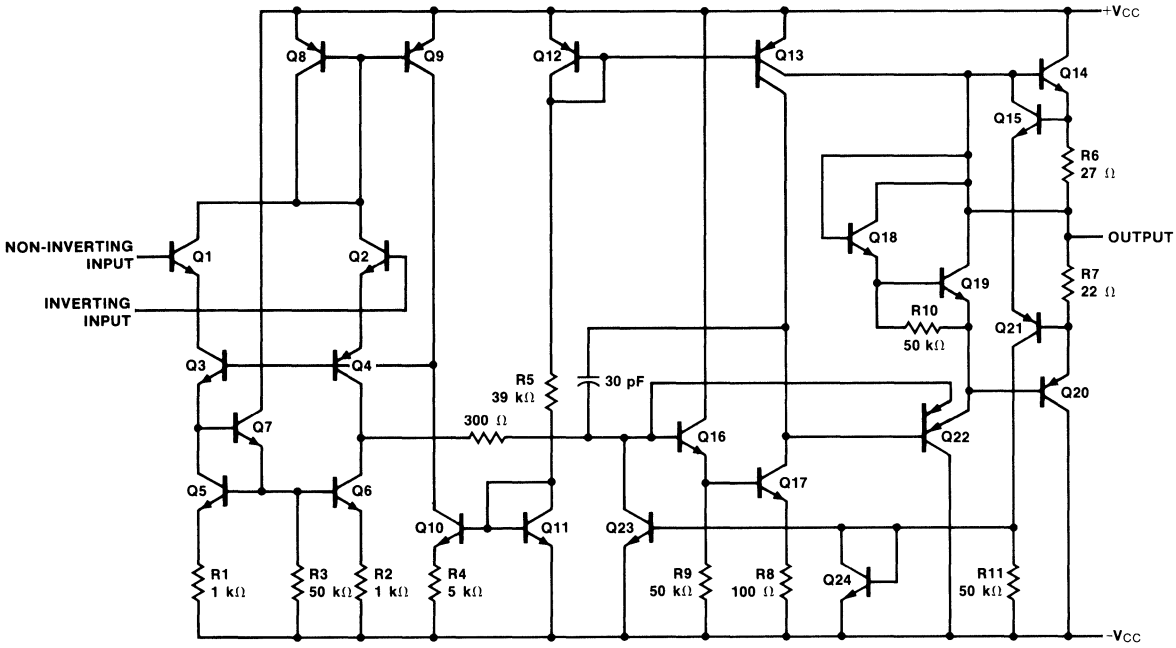


(Top View)

Order Information

Type	Package	Code	Part No.
μA1458	Ceramic DIP	6T	μA1458RC
μA1458	Molded DIP	9T	μA1458TC
μA1458C	Ceramic DIP	6T	μA1458CRC
μA1458C	Molded DIP	9T	μA1458CTC
μA1558	Ceramic DIP	6T	μA1558RM

Equivalent Circuit (Each Amplifier)



Notes

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6 3 mW/°C for the Metal Package and 5.6 mW/°C for the mini DIP.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 70°C ambient temperature.

Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

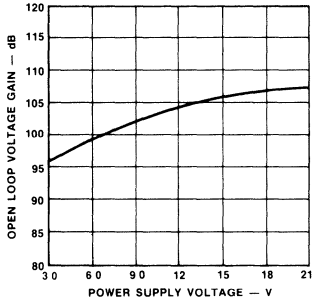
Characteristic	Condition	μA1458			μA1458C			μA1558			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		2.0	10		1.0	5.0	mV
Input Offset Current			.03	0.2		.03	0.3		0.03	0.2	μA
Input Bias Current			0.2	0.5		0.2	0.7		0.2	0.5	μA
Differential Input Impedance Parallel Input Resistance	f = 20 Hz, Open Loop	0.3	1.0			1.0		0.3	1.0		MΩ
Parallel Input Capacitance			6.0			6.0			6.0		pF
Common-Mode Input Impedance	f = 20 Hz		200			200			200		MΩ
Common-Mode Input Voltage Swing		± 12	± 13		± 11	± 13		± 12	± 13		V
Equivalent Input Noise Voltage	$A_V = 100$ $R_S = 10$ kΩ f = 1.0 kHz BW = 1.0 Hz		45			45			45		nV/√Hz
Common-Mode Rejection Ratio	f = 100 Hz	70	90		60	90		70	90		dB
Open-Loop Voltage Gain	$V_{OUT} = \pm 10$ V $R_L = 2.0$ kΩ	20 k	100 k		20 k	100 k		50 k	200 k		V/V
Power Bandwidth	$A_V = 1$ $R_S = 2.0$ kΩ THD ≤ 5% $V_{OUT} = 20\ V_{pk\text{-}pk}$		14			14			14		kHz
Unity Gain Crossover Frequency (Open Loop)			1.1			1.1			1.1		MHz
Phase Margin (Open Loop)			65			65			65		Degrees
Gain Margin			11			11			11		dB
Slew Rate	$A_V = 1$		0.8			0.8			0.8		V/μs
Output Impedance	f = 20 Hz		75			75			75		Ω
Short-Circuit Output Current			20			20			20		mA
Output Voltage Swing	$R_L = 10$ kΩ	± 12	± 14		± 11	± 14		± 12	± 14		V
Power Supply Sensitivity V_{CC-} = Constant V_{CC+} = Constant	$R_S \leq 10$ kΩ		30	150		30			30	150	μV/V
Power Supply Current	I+		2.3	5.6		2.3	8.0		2.3	5.0	mA
	I−		2.3	5.6		2.3	8.0		2.3	5.0	mA
Power Dissipation	$V_{OUT} = 0$		70	170		70	240		70	150	mW
The following specifications apply for $0°C < T_A < 70°C$ (μA1458 and μA1458C) $-55°C \leq T_A \leq 125°C$ (μA1558)											
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			12			6.0	mV
Input Offset Current				0.3			0.4			0.5	μA
Input Bias Current				0.8			1.0			1.5	μA
Open-Loop Voltage Gain	$V_{OUT} = \pm 10$ V $R_L = 2.0$ kΩ	15 k			15 k			25 k			V/V
Output Voltage Swing	$R_L = 2$ kΩ	± 10	± 13		±9.0	± 13		± 10	± 13		V
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω		15			15			15		μV/°C

4

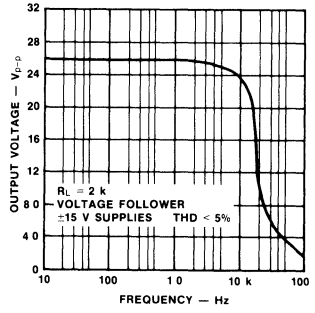
Typical Performance Curves for μA1458, μA1458C and μA1558

$V_{CC}+ = +15$ V, $V_{CC}- = -15$ V, $T_A = 25°C$ unless otherwise noted

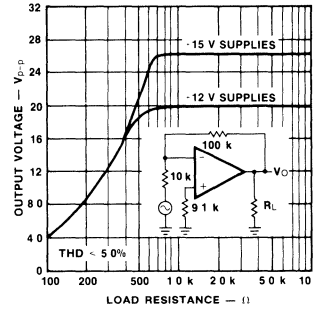
Open-Loop Voltage Gain as a Function of Power Supply Voltages



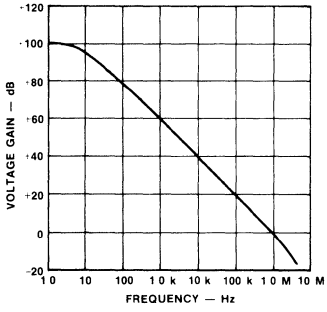
Power Bandwidth (Large Signal Swing as a Function of Frequency)



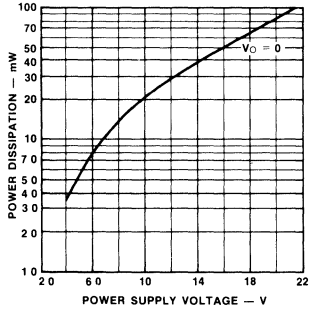
Output Voltage Swing as a Function of Load Resistance



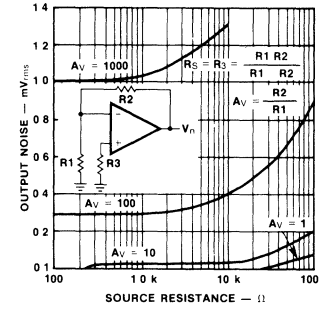
Open-Loop Frequency Response



Power Dissipation as a Function of Power Supply Voltage

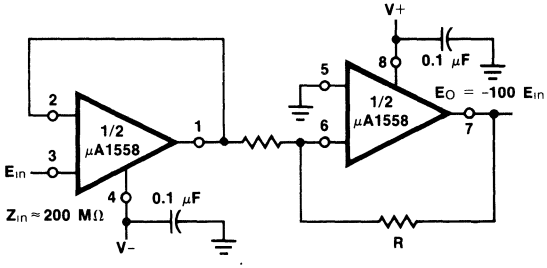


Output Noise as a Function of Source Resistance

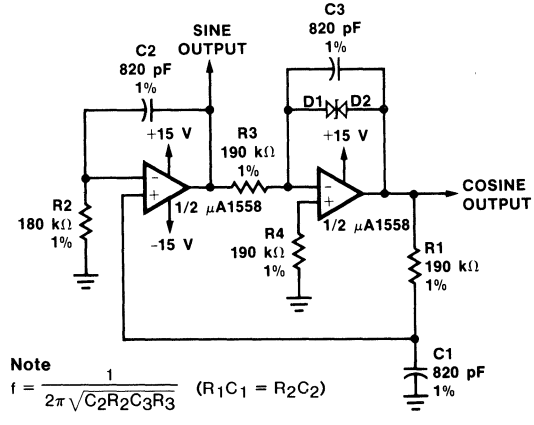


Typical Applications

High-Impedance, High-Gain Inverting Amplifier

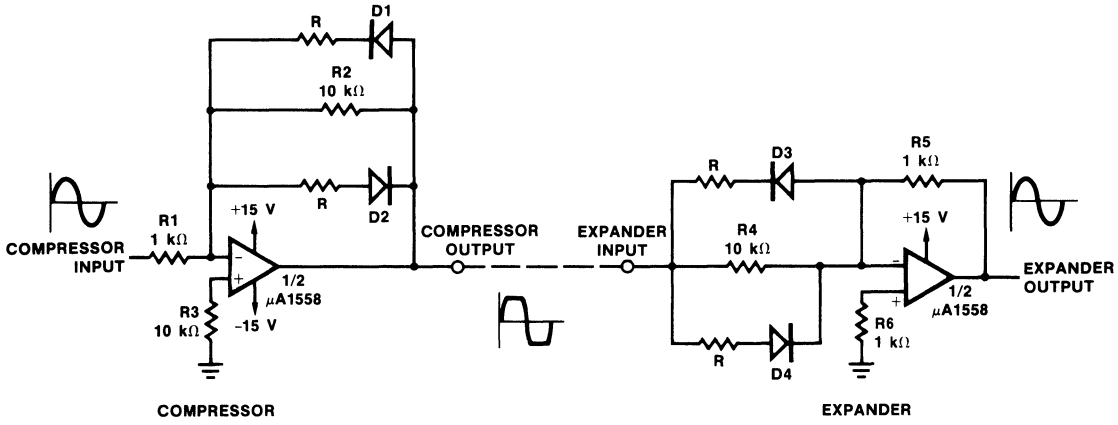


Quadrature Oscillator



Typical Applications (Cont.)

Compressor/Expander Amplifiers

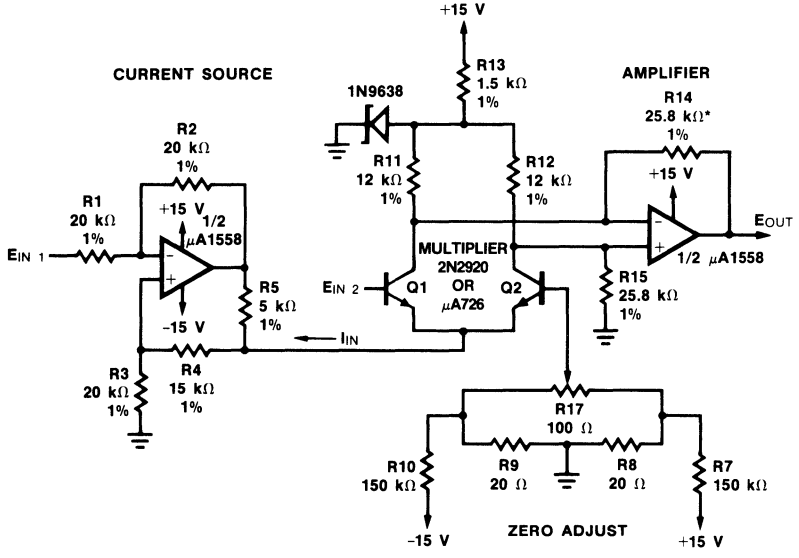


Notes

Maximum compression expansion ratio = R_1/R ($10\ k\Omega > R \geq 0$)

Diodes D1 through D4 are matched FD6666 or equivalent

Analog Multiplier



*Matched to 0.1%

$E_{OUT} = 100\ E_{IN1} \times E_{IN2}$

FAIRCHILD
A Schlumberger Company

μA3303 • μA3403 Quad Operational Amplifiers

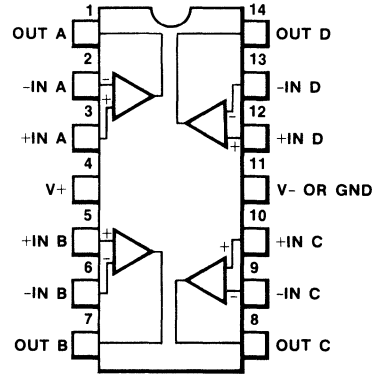
Linear Products

Description

The μA3303 and μA3403 are Monolithic Quad Operational Amplifiers consisting of four independent high-gain, internally frequency-compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. They are constructed using the Fairchild Planar epitaxial process.

- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND OR NEGATIVE SUPPLY**
- **OUTPUT VOLTAGE CAN SWING TO GROUND OR NEGATIVE SUPPLY**
- **FOUR INTERNALLY COMPENSATED OPERATIONAL AMPLIFIERS IN A SINGLE PACKAGE**
- **WIDE POWER SUPPLY RANGE SINGLE SUPPLY OF 3.0 TO 36 V**
  DUAL SUPPLY of ± 1.5 TO ± 18 V
- **CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION**
- **SHORT CIRCUIT PROTECTED OUTPUTS**
- **HIGH OPEN LOOP GAIN 200 k**
- **μA741 OPERATIONAL AMPLIFIER TYPE PERFORMANCE**

Connection Diagram
14-Pin DIP

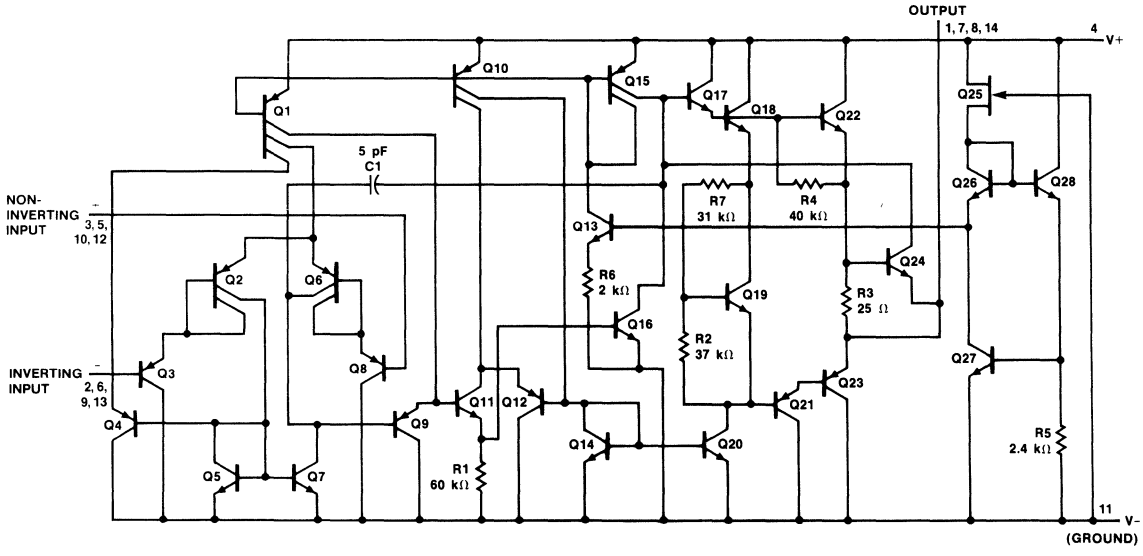


(Top View)

Order Information

Type	Package	Code	Part No.
μA3303	Molded DIP	9A	μA3303PC
μA3403	Ceramic DIP	6A	μA3403DC
μA3403	Molded DIP	9A	μA3403PC

Equivalent Circuit (1/4 of circuit shown)



Absolute Maximum Ratings

Supply Voltage Between V+ and V−	36 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (V−) (Note 1)	−0.3 V(V−) to V+
Internal Power Dissipation (Note 2)	670 mW
Operating Temperature Range	
μA3303	−40°C to +85°C
μA3403	0°C to +70°C
Storage Temperature Range	
Molded Package	−55°C to +125°C
Ceramic Package	−65°C to +150°C
Pin Temperature (Soldering)	
Molded Package (10 s)	260°C
Ceramic Package (60 s)	300°C

Notes

1. For supply Voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies to ambient temperature up to 70°C, derate linearly at 8.3 mW/°C.

Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise noted.

Characteristic	Condition	μ3303 Min	μ3303 Typ	μ3303 Max	Unit
Input Offset Voltage			2.0	8.0	mV
Input Offset Current			30	75	nA
Input Bias Current			200	−500	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+12 to $-V_S$	+12.5 to $-V_S$		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	$V_{OUT} = \pm 10$ V, $R_L = 2$ kΩ	20	200		V/mV
Power Bandwidth	$A_V = 1$, $R_L = 2$ kΩ, $V_{OUT} = 20$ V pk-pk		18		kHz
Small Signal Bandwidth	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		1.0		MHz
Slew Rate	$A_V = 1$, $V_{IN} = -10$ V to + 10 V		0.6		V/μs
Rise Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		μs
Fall Time	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		0.3		μs
Overshoot	$A_V = 1$, $R_L = 10$ kΩ, $V_{OUT} = 50$ mV		5.0		%
Phase Margin	$A_V = 1$, $R_L = 2$ kΩ, $C_L = 200$ pF		60		Degree
Crossover Distortion at f = 10 kHz	$V_{IN} = 30$ mV pk-pk, $V_{OUT} = 2$ V pk-pk		1.0		%
Output Voltage Range	$R_L = 10$ kΩ $R_L = 2$ kΩ	± 12 ± 10	12.5 12		V V
Individual Output Short Circuit Current	(Note 3)	± 10	± 30	± 45	mA
Output Impedance	f = 20 Hz		80		Ω
Power Supply Rejection Ratio	Positive Negative		30 30	150 150	μV/V μV/V
Power Supply Current	$V_{OUT} = 0$, $R_L = \infty$		2.8	7.0	mA
The following specification apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage				10	mA
Storage Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				250	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				−1000	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ, $V_{OUT} = \pm 10$ V	15			V/mV
Output Voltage Range	$R_L = 2$ kΩ	± 10			V

Electrical Characteristic V_S = +5.0 V, V_S- = Gnd, T_A = 25°C unless otherwise noted.

Characteristic	Condition	μA3303 Min	μA3303 Typ	μA3303 Max	Unit
Input Offset Voltage				10	mV
Input Offset Current				75	nA
Input Bias Current				−500	nA
Large Signal Open Loop Voltage Gain	R_L = 2 kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range (Note 4)	R_L = 10 kΩ R_L = 10 kΩ, 5.0 V ≤ V_S ≤ 30 V	3.5 (V+) −1.7			V pk-pk V pk-pk
Power Supply Current			2.5	7.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB

Electrical Characteristics V_S = ± 15 V, T_A = 25°C unless otherwise noted

Characteristic	Condition	μA3403 Min	μA3403 Typ	μA3403 Max	Unit
Input Offset Voltage			2.0	8.0	mV
Input Offset Current			30	50	nA
Input Bias Current			−200	−500	nA
Input Impedance	f = 20 Hz	0.3	1.0		MΩ
Input Common Mode Voltage Range		+13 to $-V_S$	+13.5 to $-V_S$		V
Common Mode Rejection Ratio	R_S ≤ 10 kΩ	70	90		dB
Large Signal Open Loop Voltage Gain	V_{OUT} = ± 10 V, R_L = 2 kΩ	20	200		V/mV
Power Bandwidth	A_V = 1, R_L = 2 kΩ, V_{OUT} = 20 V pk-pk		9.0		kHz
Small Signal Bandwidth	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		1.0		MHz
Slew Rate	A_V = 1, V_{IN} = −10 V to + 10 V		0.6		V/μs
Rise Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Fall Time	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		0.3		μs
Overshoot	A_V = 1, R_L = 10 kΩ, V_{OUT} = 50 mV		5.0		%
Phase Margin	A_V = 1, R_L = 2 kΩ, C_L = 200 pF		60		Degree
Crossover Distortion at f = 10 kHz	V_{IN} = 30 mV pk-pk, V_{OUT} = 2 V pk-pk			1.0	%
Output Voltage Range	R_L = 10 kΩ R_L = 2 kΩ	± 12 ± 10	± 13.5 ± 13		V V
Individual Output Short Circuit Current	(Note 3)	± 10	± 30	± 45	mA
Output Impedance	f = 20 Hz		80		Ω
Power Supply Rejection Ratio	Positive Negative		30 30	150 150	μV/V μV/V
Power Supply Current	V_{OUT} = 0, R_L = ∞		2.8	7.0	mA

Electrical Characteristics $V_S = \pm 15$ V, $-55°C \leq T_A \leq +125°C$

Characteristic	Condition	μA3403 Min	μA3403 Typ	μA3403 Max	Unit
Input Offset Voltage				10	mV
Average Temperature Coefficient of Input Offset Voltage			10		μV/°C
Input Offset Current				200	nA
Average Temperature Coefficient of Input Offset Current			50		pA/°C
Input Bias Current				−800	nA
Large Signal Open Loop Voltage Range	$R_L = 2$ kΩ, $V_{OUT} = \pm$ 10 V	15			V/mV
Output Voltage Range	$R_L = 2$ kΩ	± 10			V

Electrical Characteristics $V_S = +5.0$ V, $V_S- = G$, $T_A = 25°C$ unless otherwise noted.

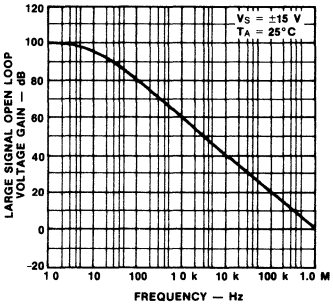
Characteristic	Condition	μA3403 Min	μA3403 Typ	μA3403 Max	Unit
Input Offset Voltage			2.0	10	mV
Input Offset Current			30	50	nA
Input Bias Current			−200	−500	nA
Large Signal Open Loop Voltage Gain	$R_L = 2$ kΩ	20	200		V/mV
Power Supply Rejection Ratio				150	μV/V
Output Voltage Range (Note 4)	$R_L = 10$ kΩ $R_L =$ kΩ, 5.0 V $\leq V_S \leq$ 30 V	3.5 (V+) −1.7			V pk-pk V pk-pk
Power Supply Current			2.5	7.0	mA
Channel Separation	f = 1 kHz to 20 kHz (Input Referenced)		−120		dB

Notes

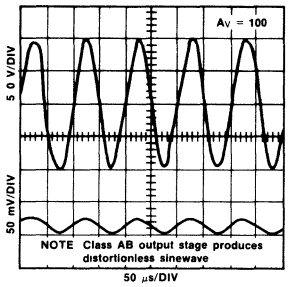
3. Not to exceed maximum package power dissipation.
4. Output will swing to ground.

Typical Performance Curves

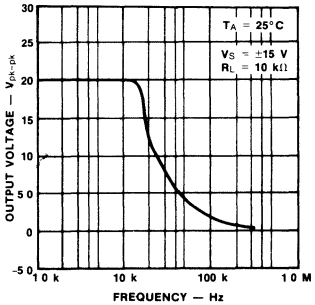
Large Signal Open Loop Voltage Gain as a Function of Frequency



Sine Wave Response

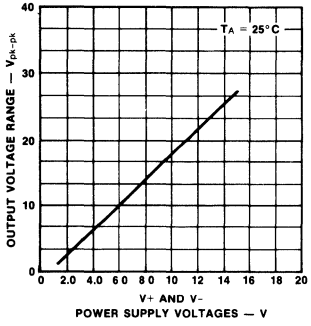


Output Voltage as a Function of Frequency

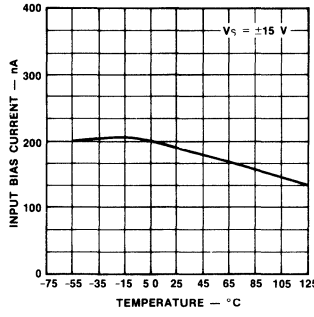


Typical Performance Curves (Cont.)

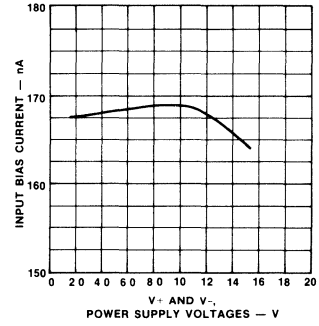
Output Swing as a Function of Supply Voltage



Input Bias Current as a Function of Temperature

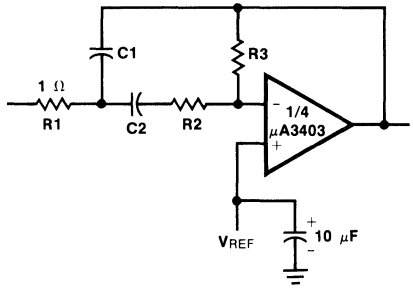


Input Bias Current as a Function of Supply Voltage



Typical Applications

Multiple Feedback Bandpass Filter



f_o = center frequency

BW = Bandwidth
R in kΩ
C in μF

$$Q = \frac{f_o}{BW} < 10$$

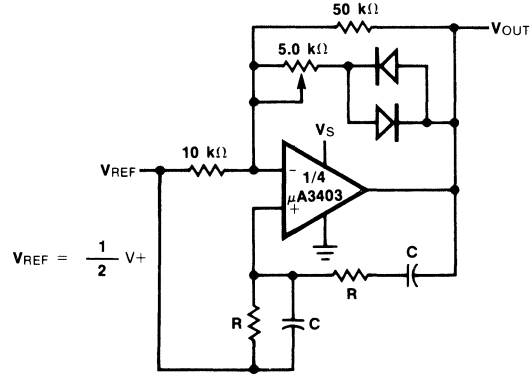
$$C1 = C2 = \frac{Q}{3}$$

$$\left.\begin{array}{l} R1 = R2 = 1 \\ R8 = 9Q^2 - 1 \end{array}\right\}$$ Use scaling factors in these expressions.

If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

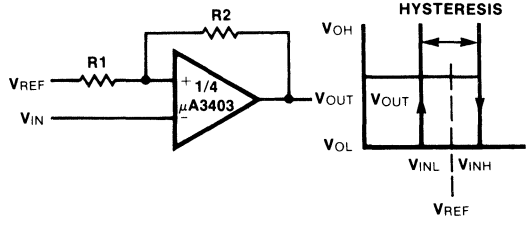
Design example:
given: Q = 5, f_o = 1 kHz
Let R1 = R2 = 10 kΩ
then R3 = $9(5)^2 - 10$
R3 = 215 kΩ
$C = \frac{5}{3}$ = 1.6 nF

Wein Bridge Oscillator



$$f_o = \frac{1}{2\pi RC}$$ for f_o = 1 kHz
R = 16 kΩ
C = 0.01 μF

Comparator With Hysteresis



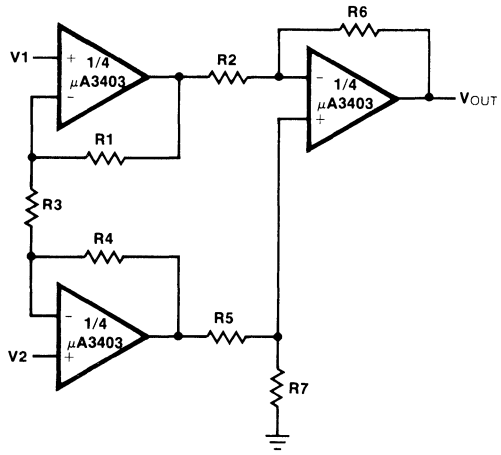
$$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Typical Applications (Cont.)

High Impedance Differential Amplifier



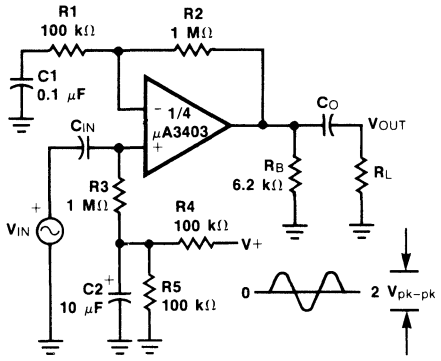
$V_{OUT} = C(1 + a + b)(V2 - V1)$

$\frac{R2}{R5} \equiv \frac{R6}{R7}$ for best CMRR

R1 = R4
R2 = R5

$\text{Gain} = \frac{R6}{R5}\left(1 + \frac{2R1}{R3}\right) = C\,(1 + a + b)$

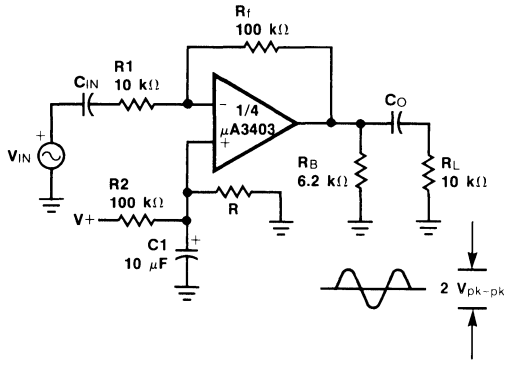
AC Coupled Non-Inverting Amplifier



$A_V = 1 + \frac{R2}{R1}$

A_V = 11 (as shown)

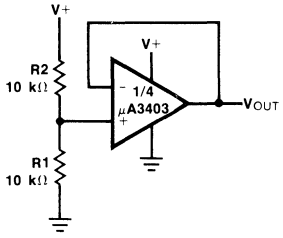
AC Coupled Inverting Amplifer



$A_V = \frac{Rf}{R1}$

A_V = 10 (as shown)

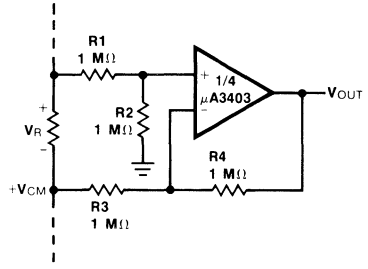
Voltage Reference



$V_{OUT} = \frac{R1}{R1 + R2}\left(= \frac{V+}{2} \text{ as shown}\right)$

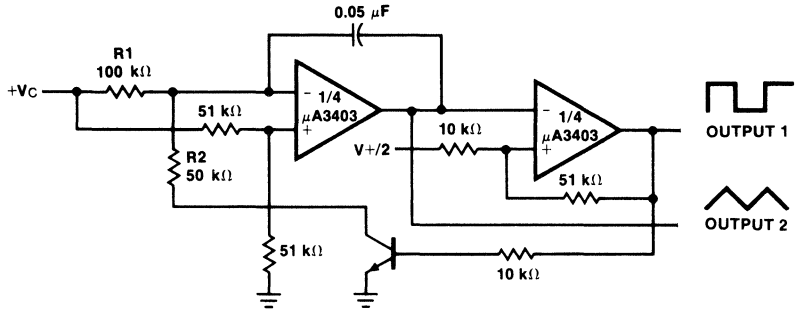
$V_{OUT} = \frac{1}{2} V_{CC}$

Ground Referencing a Differential Input Signal

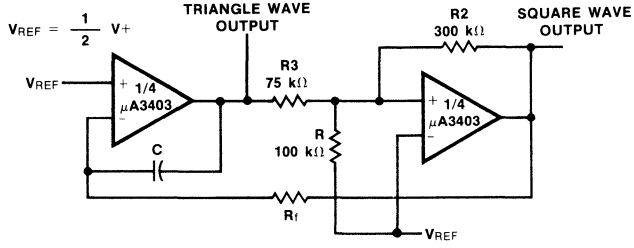


Typical Applications (Cont.)

Voltage Controlled Oscillator

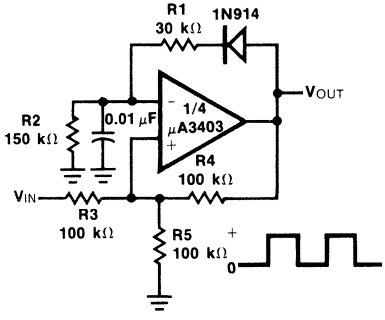


Function Generator



$$f = \frac{R1 + R2}{4CR_fR1} \quad \text{if} \quad R3 = \frac{R2R1}{R2 + R1}$$

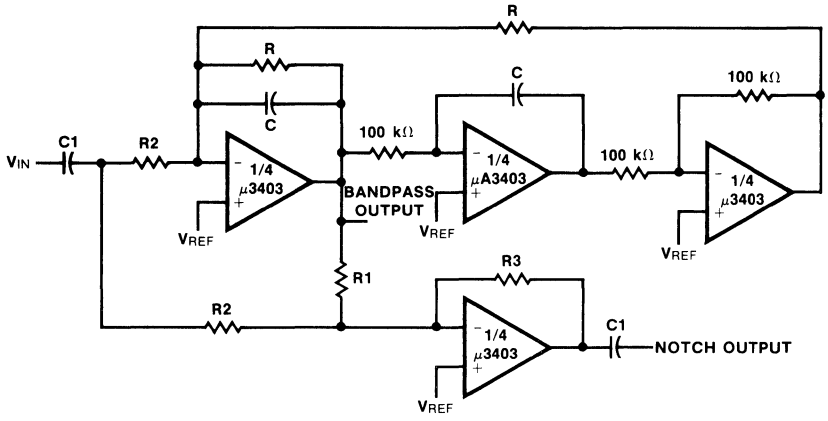
Pulse Generator



*Wide Control Voltage Range.
$0V_{DC} \leq V_C \leq 2\ (V+ - 1.5\ V_{DC})$

Typical Applications (Cont.)

Bi-Quad Filter



$$Q = \frac{BW}{f_o}$$

where

T_{BP} = Center Frequency Gain

T_N = Bandpass Notch Gain

$$f_o = \frac{1}{2\pi RC}$$

$R1 = QR$

$$R2 = \frac{R1}{T_{BP}}$$

$R3 = T_N R2$

$C1 = 10\ C$

Example:

f_o = 1000 Hz

BW = 100 Hz

T_{BP} = 1

T_N = 1

R = 160 kΩ

R1 = 1.6 MΩ

R2 = 1.6 MΩ

R3 = 1.6 MΩ

C = 0.001 μF

4

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μA4136 Quad Operational Amplifiers

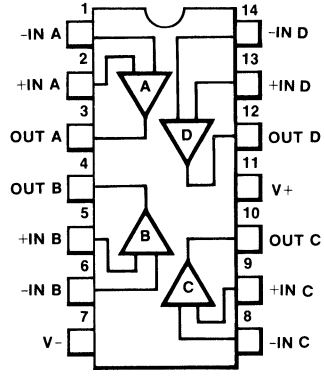
Linear Products

Description

The μA4136 Monolithic Quad Operational Amplifiers consists of four independent high gain, internal frequency compensated operational amplifiers. The specifically designed low noise input transistors allow the μA4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. They are constructed using the Fairchild Planar Epitaxial process. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.

- **UNITY GAIN BANDWIDTH 3 MHz**
- **CONTINUOUS SHORT CIRCUIT PROTECTION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **NO LATCH-UP**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **μA741 OPERATIONAL AMPLIFIER TYPE PERFORMANCE**
- **PARAMETER TRACKING OVER TEMPERATURE RANGE**
- **GAIN AND PHASE MATCH BETWEEN AMPLIFIERS**

Connection Diagram
14-Pin DIP

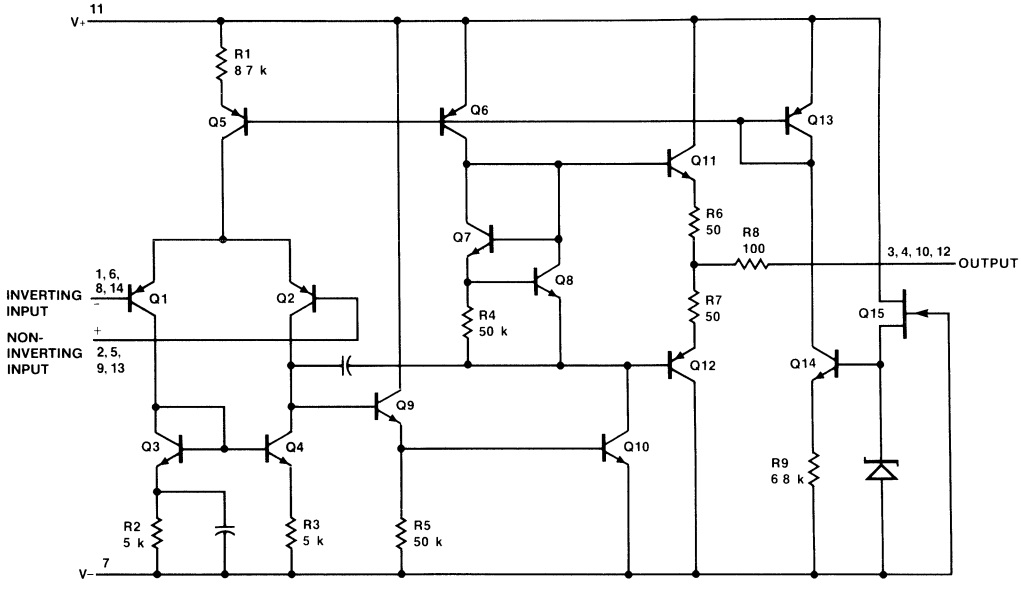


(Top View)

Order Information

Type	Package	Code	Part No.
μA4136	Ceramic DIP	6A	μA4136DM
μA4136C	Ceramic DIP	6A	μA4136DC
μA4136C	Molded DIP	9A	μA4136PC

Equivalent Circuit (1/4 of circuit shown)



Absolute Maximum Ratings

Supply Voltage	
μA4136	±22 V
μA4136C	±18 V
Differential Input Voltage (Note 1)	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	670 mW
Output Short Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
μA4136	−55°C to +125°C
μA4136C	0°C to +70°C
Storage Temperature range	
Molded Package	−55°C to +125°C
Ceramic Package	−65°C to +150°C
Pin Temperature	
Molded Package (10 s)	260°C
Ceramic Package (60 s)	300°C

Notes

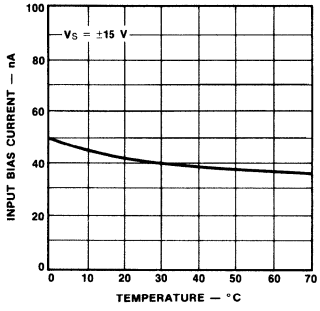
1. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage
2. Rating applies to ambient temperature up to 70°C Above T_A = 70°C, derate linearly at 8 3 mW/°C
3. Short circuit may be to ground, one amplifier only I_{SC} = 45 mA (Typical)

Electrical Characteristics T_A = 25°C, V_S = ±15 V unless otherwise specified

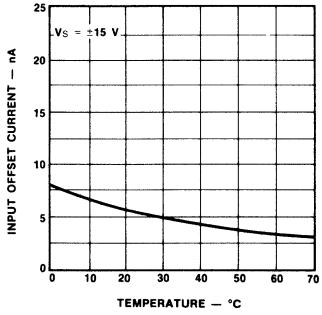
Characteristic	Condition	μA4136 Min	μA4136 Typ	μA4136 Max	μA4136C Min	μA4136C Typ	μA4136C Max	Unit
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	50 k	300 k		20 k	300 k		
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Power Consumption			210	340		210	340	mW
Transient Response (Unity Gain) Risetime	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		0.13			0.13		μs
Transient Response (Unity Gain) Overshoot	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate (Unity Gain)	$R_L \geq 2\ k\Omega$		1.5			1.0		V/μs
Channel Separation (Open Loop) (Gain = 100)	F = 10 kHz, R_S = 1 kΩ		105			105		dB
	f = 10 kHz, R_S = 1 kΩ		105			105		dB
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for μA4136; $0°C \leq T_A \leq +70°C$ for μA4136C.								
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	25 k			15 k			
Output Voltage Swing	$R_L \geq 2\ k\Omega$, V_S = ±15 V	±12			±10			V
Power Consumption	T_A = High		180	300		180	300	mW
	T_A = Low		240	400		240	400	mW

Typical Performance Curves

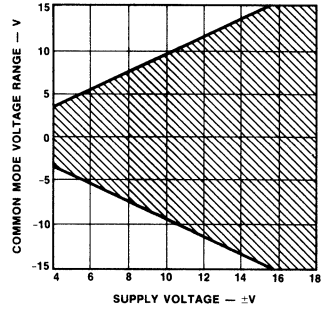
Input Bias Current as a Function of Ambient Temperature



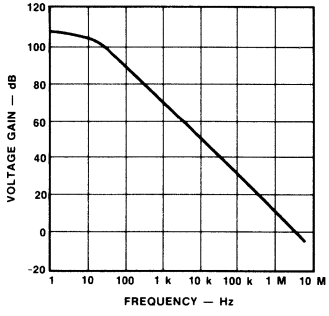
Input Offset Current as a Function of Ambient Temperature



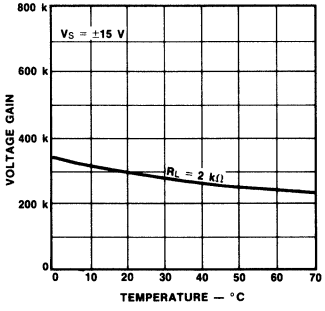
Common Mode Range as a Function of Supply Voltage



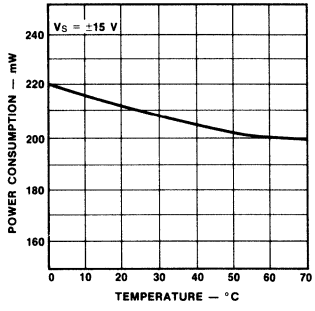
Open Loop Voltage Gain as a Function of Frequency



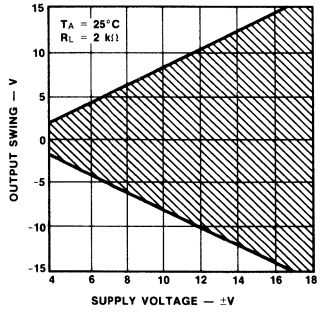
Open Loop Gain as a Function of Temperature



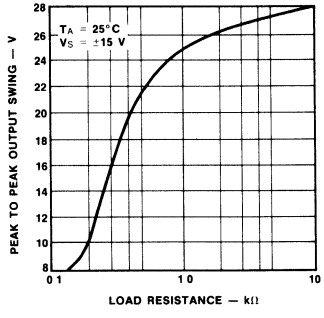
Power Consumption as a Function of Ambient Temperature



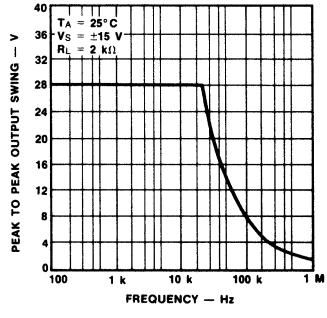
Typical Output Voltage as a Function of Supply Voltage



Output Voltage Swing as a Function of Load Resistance

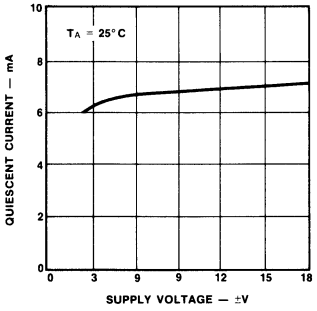


Output Voltage Swing as a Function of Frequency

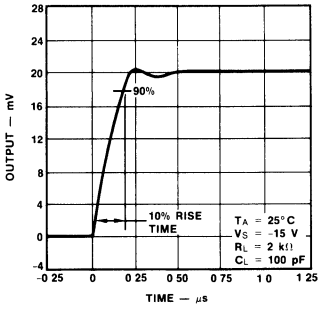


Typical Performance Curves (Cont.)

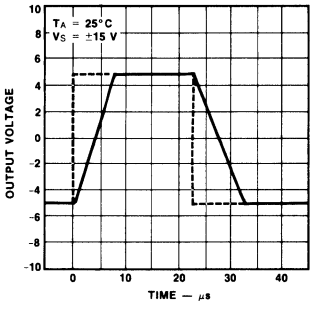
Quiesent Current as a Function of Supply Voltage



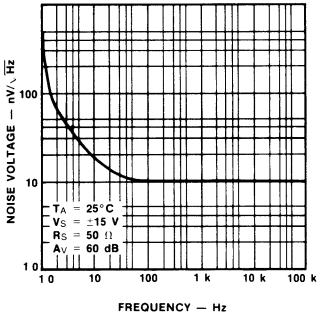
Transient Response



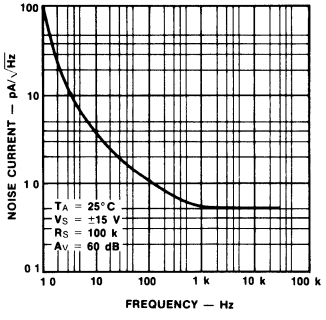
Voltage Follower Large Signal Pulse Response



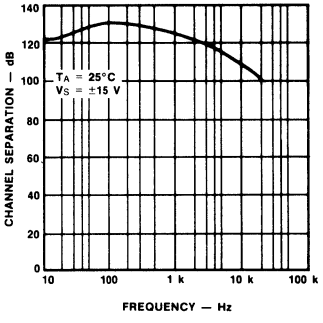
Input Noise Voltage as a Function of Frequency



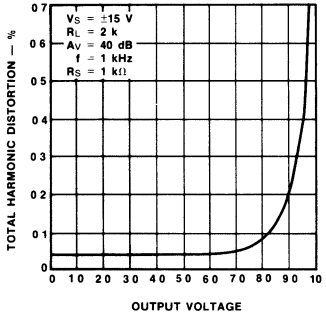
Input Noise Current as a Function of Frequency



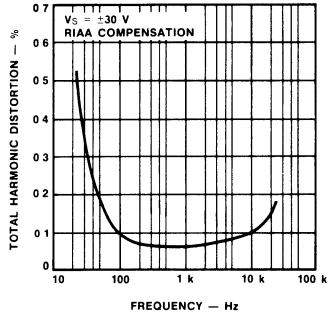
Channel Separation



Total Harmonic Distortion as a Function of Output Voltage f = 1 kHz



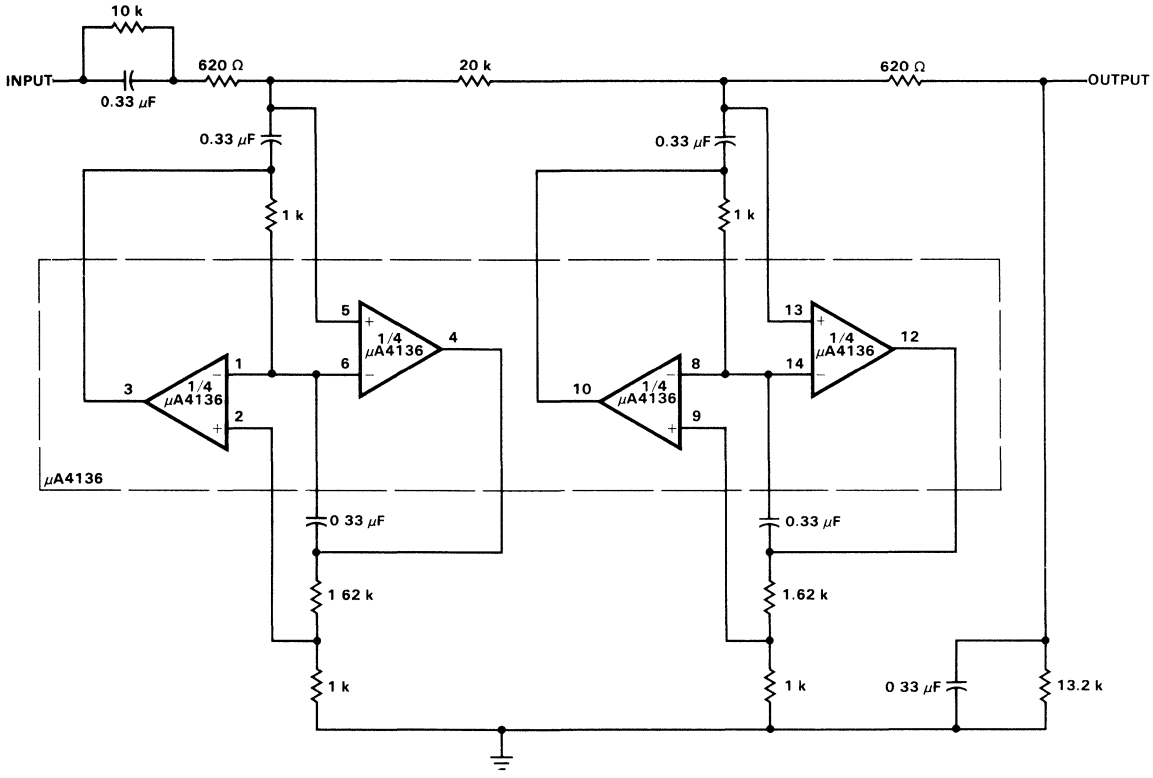
Distortion as a Function of Frequency V_{OUT} = 1 Vrms



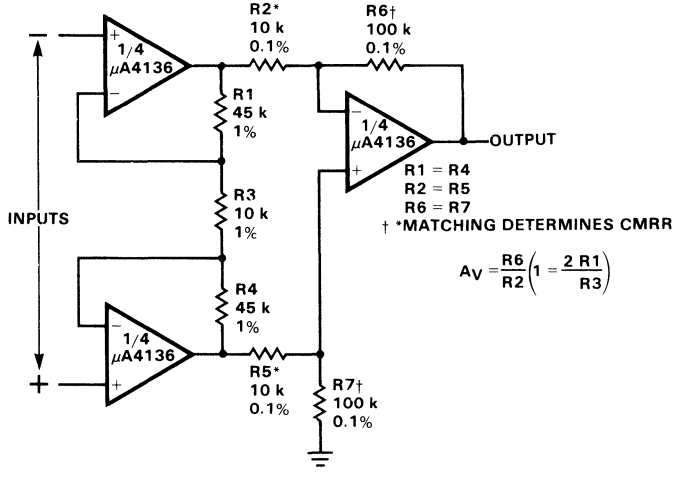
4

Typical Applications

400 Hz Lowpass Butterworth Active Filter

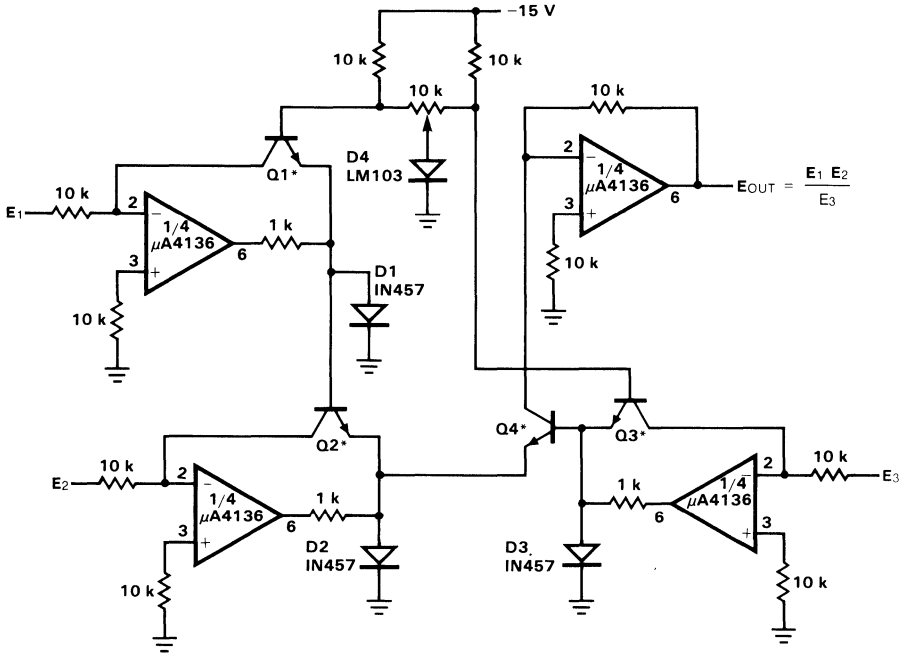


Differential Input Instrumentation Amplifier with High Common Mode Rejection

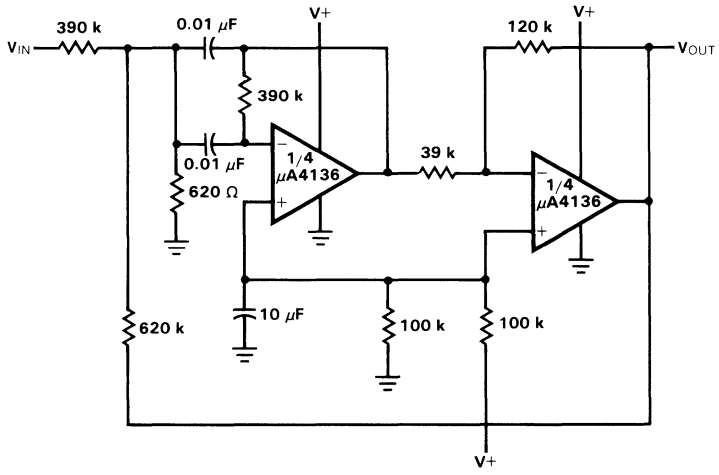


Typical Applications (Cont.)

Analog Multiplier/Divider

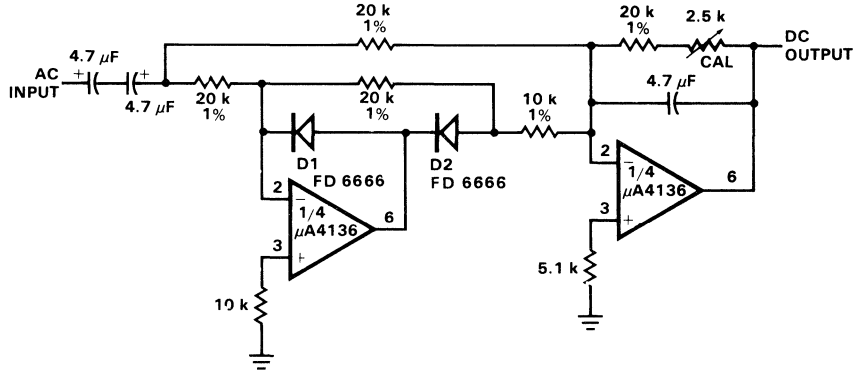


1 kHz Bandpass Active Filter

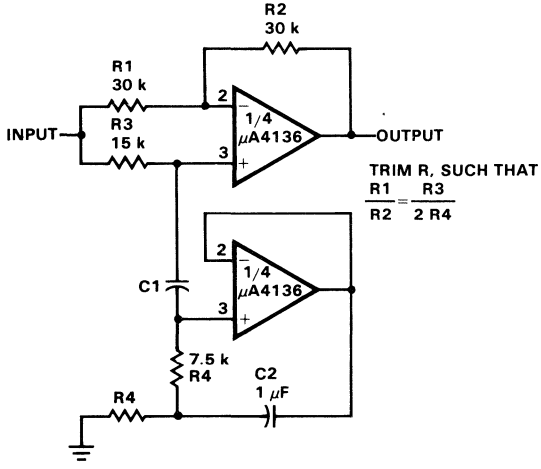


Typical Applications (Cont.)

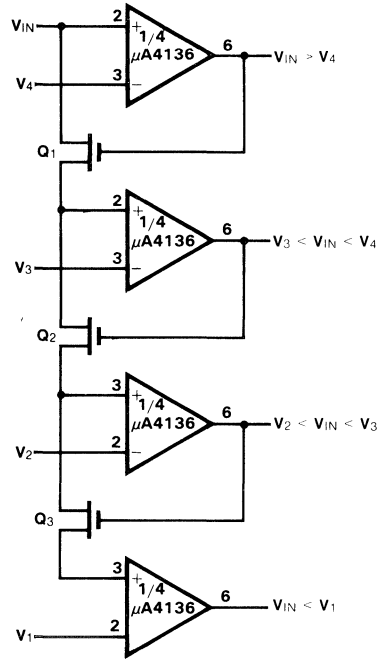
Full-Wave Rectifier and Averaging Filter



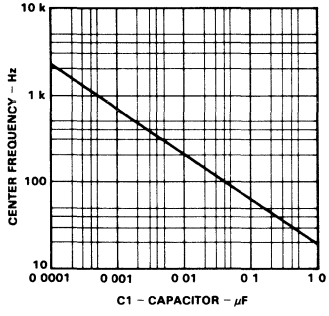
Notch Filter Using the μA4136 as a Gyrator



Multiple Aperture Window Discriminator



Notch Frequency as a Function of C1



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μA710 High-Speed Differential Comparator

Linear Products

Description

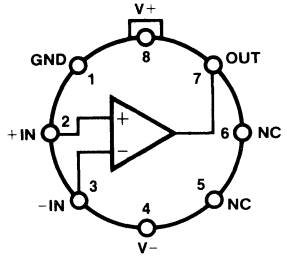
The μA710 is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse-height discriminator, a voltage comparator in high-speed a/d converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **5 μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

Absolute Maximum Ratings

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
Molded DIP	670 mW
Storage Temperature Range	
Metal Package, Ceramic DIP	−65°C to +150°C
Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA710)	−55°C to +125°C
Commercial (μA710C)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Package, Ceramic DIP (60 s)	300°C
Molded DIP (10 s)	260°C

Connection Diagram 8-Pin Metal Package



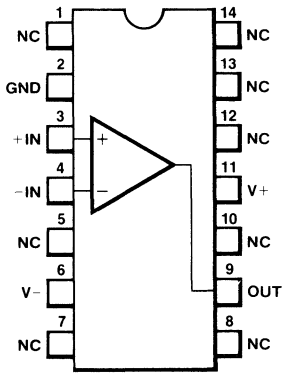
(Top View)

Pin 4 connected to case

Order Information

Type	Package	Code	Part No.
μA710	Metal	5W	μA710HM
μA710C	Metal	5W	μA710HC

Connection Diagram 14-Pin DIP



(Top View)

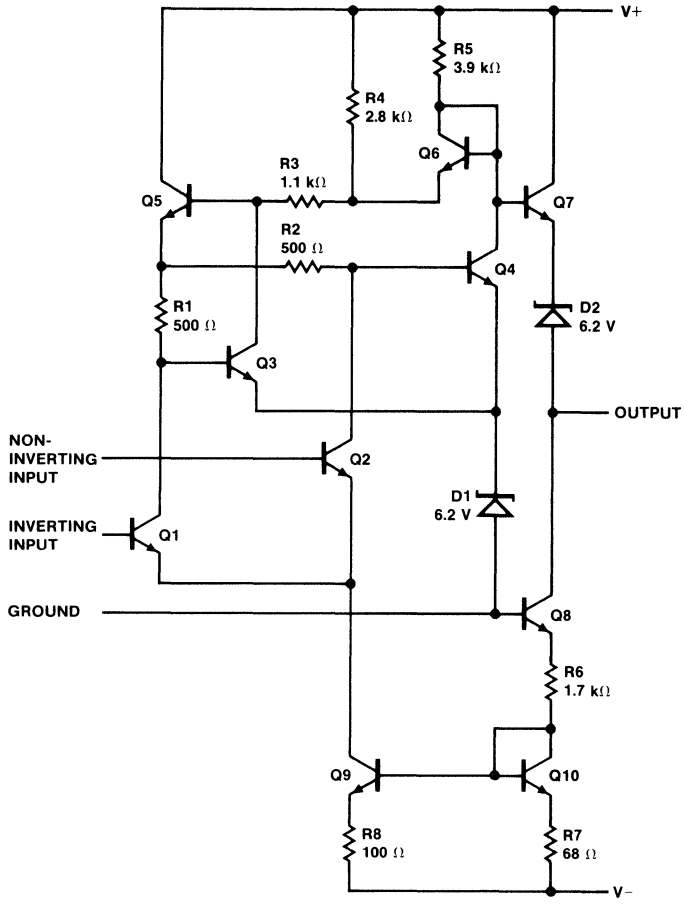
Order Information

Type	Package	Code	Part No.
μA710	Ceramic DIP	6A	μA710DM
μA710C	Ceramic DIP	6A	μA710DC
μA710C	Molded DIP	9A	μA710PC

Notes

1 Rating applies to ambient temperatures up to 70°C Above 70°C ambient derate linearly at 6.3 mW/°C for metal package, 8 3 mW/°C for DIPs

Equivalent Circuit



μA710
Electrical Characteristics $T_A = 25°C$, $V+ = 12.0$ V, $V- = -6.0$ V unless otherwise specified.

Characteristic	Condition (Note 2)	Min	Typ	Max	Unit
Input Offset Voltage	$R_S \leq 200\ \Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	2.0	2.5		mA
Response Time (Note 3)			40		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage	$R_S \leq 200\ \Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = +125°C$ $R_A = 50\ \Omega$. $T_A = 25°C$ to $T_A = -55°C$		3.5 2.7	10 10	μV/°C μV/°C
Input Offset Current	$T_A = +125°C$ $T_A = -55°C$		0.25 1.8	3.0 7.0	μA μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$ $T_A = 25°C$ to $T_A -55°C$		5.0 15	25 75	nA/°C nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	$V- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_s \leq 200\ \Omega$	80	100		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		1000			
Output HIGH Voltage	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$ $T_A = -55°C$, $\Delta V_{IN} \geq 5$mV, $V_{OUT} = 0$	0.5 1.0	1.7 2.3		mA mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	V_{OUT} = GND, Inverting Input = +5 mV		4.6	7.0	mA
Power Consumption	V_{OUT} = GND, Inverting Input = +10 mV		90	150	mW

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Notes

2 The input offset voltage and input offset current are specified for a logic threshold voltage as follows For 710, 1.8 V at −55°C, 1.4 V at +25°C, 1 0 V at +125°C. For 710C, 1.5 V at 0°C, 1 4 V at +25°C, and 1.2 V at +70°C.

3. The response time specified is for a 100 mV input step with 5 mV overdrive.

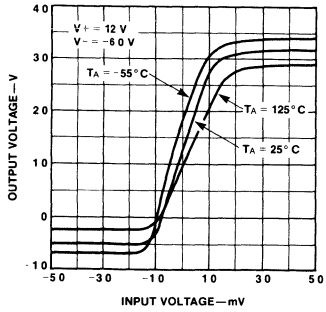
μA710C
Electrical Characteristics $T_A = 25°C$, V+ = 12.0 V, V− = −6.0 V unless otherwise specified

Characteristic	Condition (Note 2)	Min	Typ	Max	Unit
Input Offset Voltage	$R_A \leq 200\ \Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 200\ \Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$ $T_A = 25°C$ to $T_A = 0°C$		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	V = −7.0 V	±5.0			V
Common Mode Rejection Ratio	$R_A \leq 200\ \Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Output HIGH Voltage	$\Delta V_{IN} \geq 5$ mV, $O \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5$ mV	−1.0	-0.5	0	V
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5			mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	V_{OUT} = GND, Inverting Input = +5 mV		4.6	7.0	mA
Power Comsumption	V_{OUT} = GND, Inverting Input = +10 mV		90	150	mW

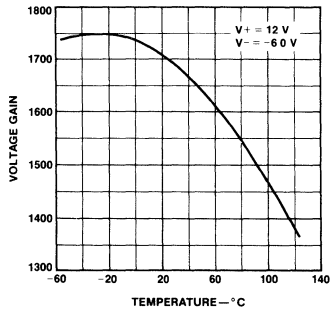
Notes on preceding page

Typical Performance Curves for μA710

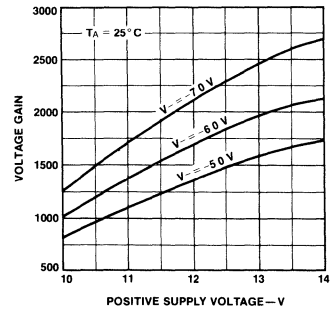
Voltage Transfer Characteristic



Voltage Gain as a Function of Ambient Temperature

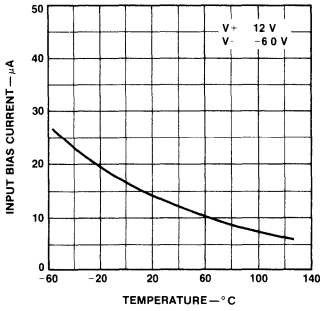


Voltage Gain as a Function of Supply Voltages

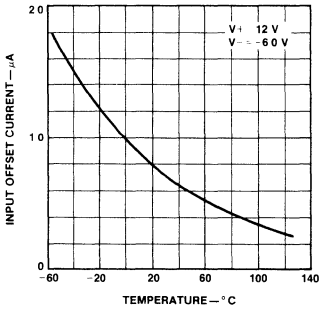


Typical Performance Curves for μA710 (Cont.)

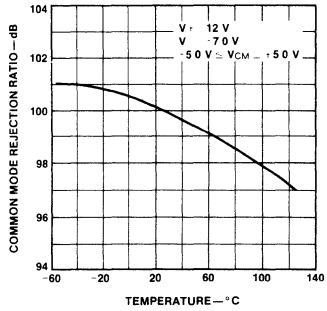
Input Bias Current as a Function of Ambient Temperature



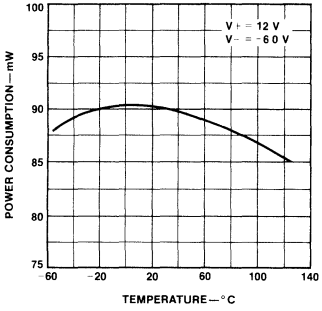
Input Offset Current as a Function of Ambient Temperature



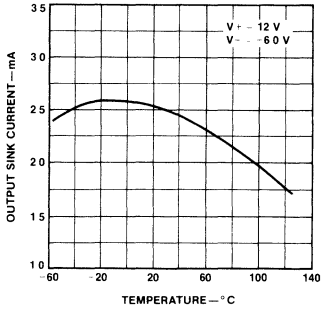
Common Mode Rejection Ratio as a Function of Ambient Temperature



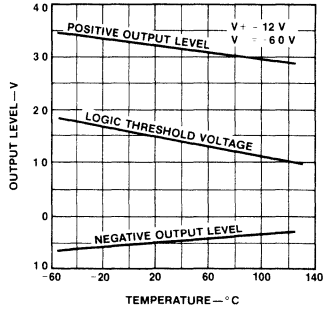
Power Consumption as a Function of Ambient Temperature



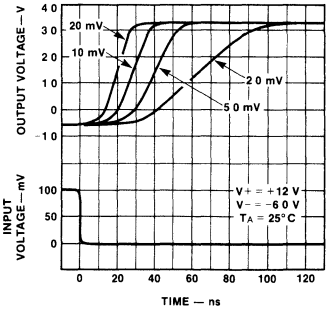
Output Sink Current as a Function of Ambient Temperature



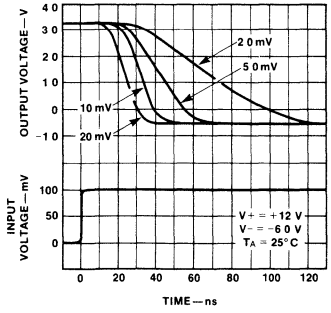
Output Voltage Levels as a Function of Ambient Temperature



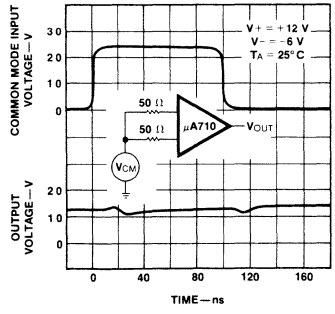
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives



Common Mode Pulse Response



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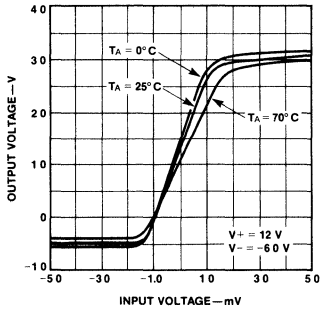
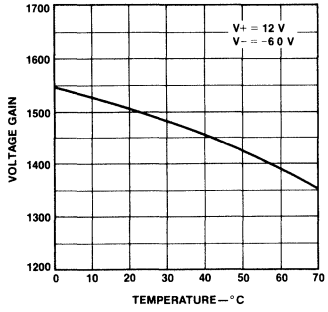
Typical Performance Curves for μA710C

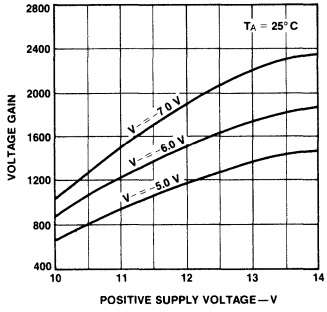
Voltage Transfer Characteristic



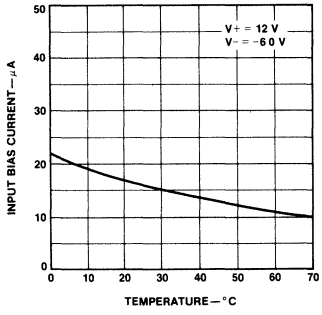
Voltage Gain as a Function of Ambient Temperature



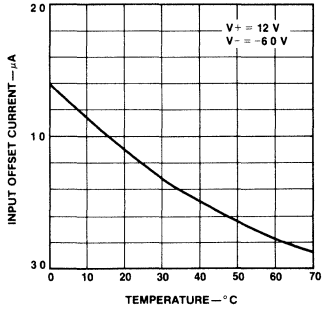
Voltage Gain as a Function of Supply Voltages



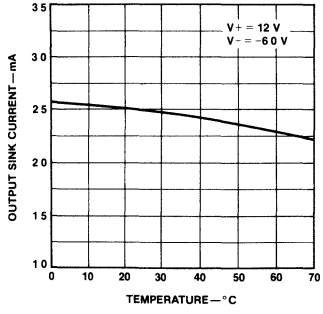
Input Bias Current as a Function of Ambient Temperature



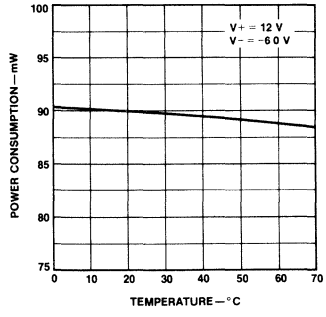
Input Offset Current as a Function of Ambient Temperature



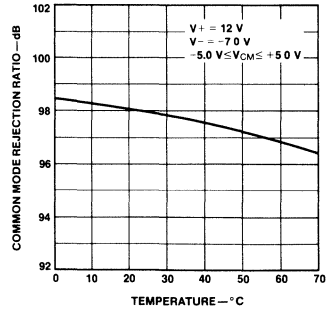
Common Mode Rejection Ratio as a Function of Ambient Temperature



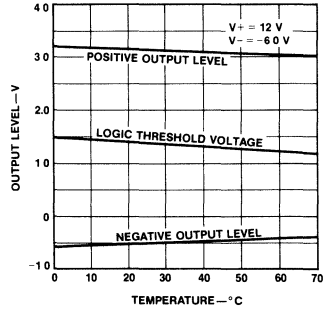
Power Consumption as a Function of Ambient Temperature



Output Sink Current as a Function of Ambient Temperature

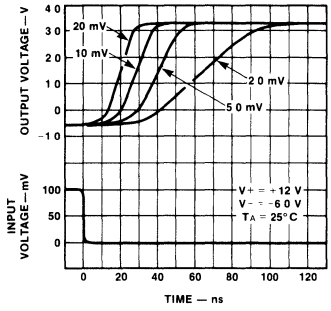


Output Voltage Levels as a Function of Ambient Temperature

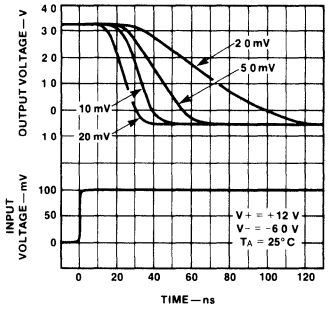


Typical Performance Curves for μA710C (Cont.)

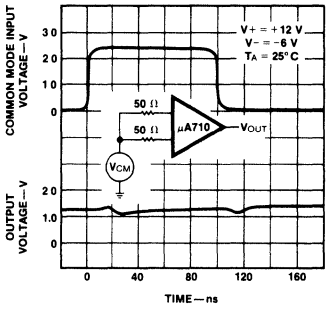
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives



Common Mode Pulse Response



5

FAIRCHILD

A Schlumberger Company

μA711
Dual High-Speed Differential Comparator

Linear Products

Description

The μA711 is a Dual, Differential Voltage Comparator featuring high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-Go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed using the Fairchild Planar epitaxial process.

- **FAST RESPONSE TIME—40 ns TYPICAL**
- **5 mV MAXIMUM OFFSET VOLTAGE**
- **10 μA MAXIMUM OFFSET CURRENT**
- **INDEPENDENT COMPARATOR STROBING**

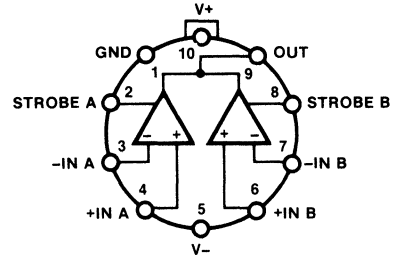
Absolute Maximum Ratings

Positive Supply Voltage	+14 V
Negative Supply Voltage	−7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	
Metal	500 mW
DIP	670 mW
Operating Temperature Range	
Military (μA711)	−55°C to +125°C
Commercial (μA711C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Metal Package, Ceramic DIP	
Molded DIP (Soldering, 10 s)	260°C

Notes

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the metal package, 8.3 mW/°C for the DIP.

Connection Diagram
10-Pin Metal Package



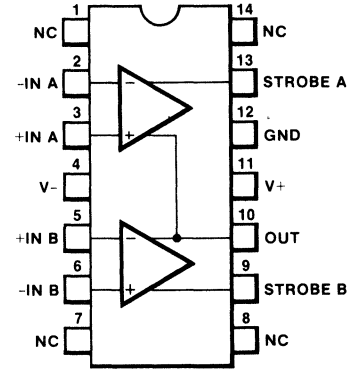
(Top View)

Pin 5 connected to case

Order Information

Type	Package	Code	Part No.
μA711	Metal	5X	μA711HM
μA711C	Metal	5X	μA711HC

Connection Diagram
14-Pin DIP

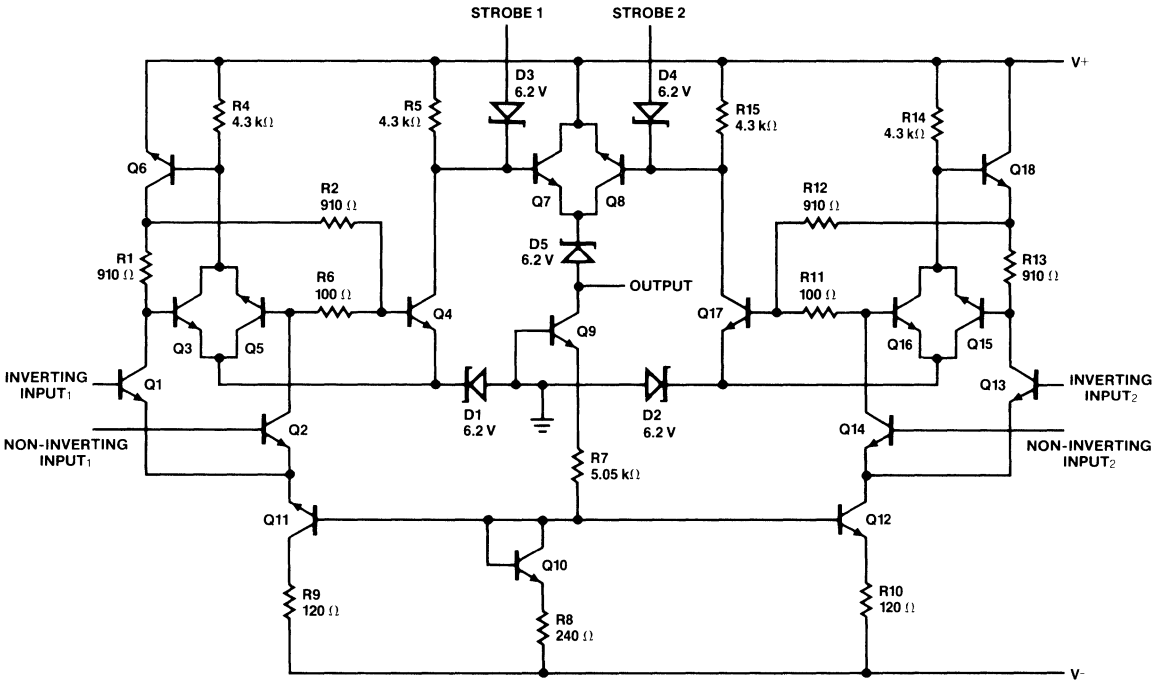


(Top View)

Order Information

Type	Package	Code	Part No.
μA711	Ceramic DIP	6A	μA711DM
μA711C	Ceramic DIP	6A	μA711DC
μA711C	Molded DIP	9A	μA711PC

Equivalent Circuit



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μA711
Electrical Characteristics $T_A = 25°C$, $V+ = 12$ V, $V- = -6.0$ V unless otherwise specified

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage	$V_{OUT} = +1.4$ V, $R_S \leq 200\ \Omega$, $V_{CM} = 0$		1.0	3.5	mV
	$V_{OUT} = +1.4$ V, $R_S \leq 200\ \Omega$		1.0	5.0	mV
Input Offset Current	$V_{OUT} = +1.4$ V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V- = -7.0$ V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Output HIGH Voltage	$V_{IN} \geq 10$ mV, $I_O = 5$ mA	2.5	3.5		V
Output LOW Voltage	$V_{IN} \geq 10$ mV	−1.0	−0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3$ V	−1.0		0	V
Output Sink Current	$V_{IN} \geq 10$ mV, $V_{OUT} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{STROBE} = 100$ mV		1.2	2.5	mA
Positive Supply Current	V_{OUT} = Ground, Inverting Input = +5 mV		8.6		mA
Negative Supply Current	V_{OUT} = Ground, Inverting Input = +5 mV		3.9		mA
Power Consumption			130	200	mW

The following specifications apply for $-55°C \leq T_A \leq +125°C$

Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\ \Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

Notes
2 The response time specified (see definitions) is for a 100 mV step input with 5 mV overdrive.
3. The input offset voltage is specified for a logic threshold as follows:
711. 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C—
711C: 1 5 V at 0°C, 1.4 V at +25°C, 1.2 V at +70°C

μA711C

Electrical Characteristics $T_A = 25°C$, $V+ = 12$ V, $V- = -6.0$ V unless otherwise specified

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage	$V_{OUT} = +1.4$ V, $R_S \leq 200\ \Omega$, $V_{CM} = 0$		1.0	5.0	mV
	$V_{OUT} = +1.4$ V, $R_S \leq 200\ \Omega$		1.0	7.5	mV
Input Offset Current	$V_{OUT} = +1.4$ V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V- = -7.0$ V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Output HIGH Voltage	$V_{IN} \geq 10$ mV, $I_O = 5$ mA	2.5	3.5		V
Output LOW Voltage	$V_{IN} \geq 10$ mV	−1.0	−0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3$ V	−1.0		0	V
Output Sink Current	$V_{IN} \geq 10$ mV, $V_{OUT} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{STROBE} = 100$ mV		1.2	2.5	mA
Positive Supply Current	V_{OUT} Ground, Inverting Input = +10 mV		8.6		mA
Negative Supply Current	V_{OUT} Ground, Inverting Input = +10 mV		3.9		mA
Power Consumption			130	230	mW

The following specifications apply for $0°C \leq T_A \leq +70°C$

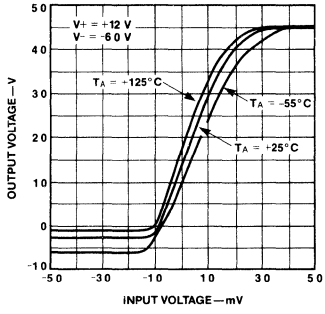
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, $V_{CM} = 0$			6.0	mV
	$R_S \leq 200\ \Omega$			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

Notes

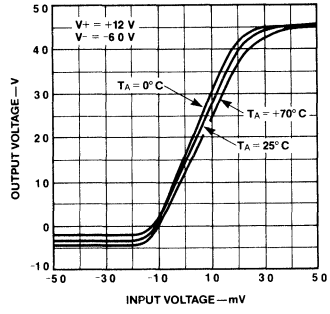
2. The response time specified (see definitions) is for a 100 mV step input with 5 mV overdrive.
3. The input offset voltage is specified for a logic threshold as follows:
   711: 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C—
   711C: 1.5 V at 0°C, 1.4 V at +25°C, 1.2 V at +70°C

Typical Performance Curves

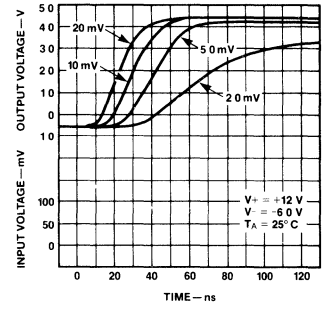
Voltage Transfer Characteristic μA711



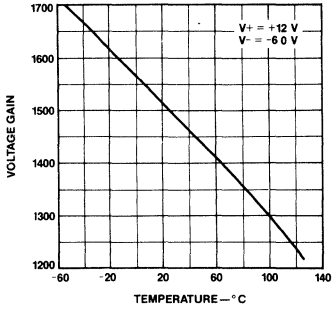
Voltage Transfer Characteristic μA711C



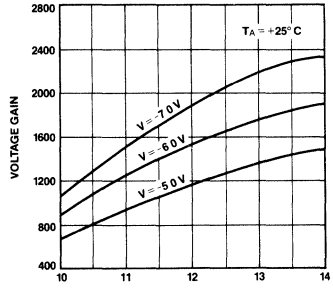
Response Time for Various Input Overdrives



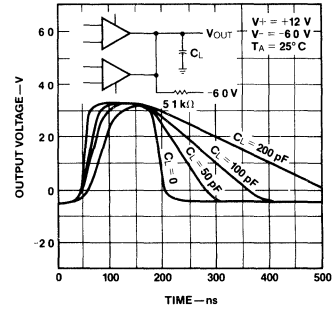
Voltage Gain as a Function of Ambient Temperature



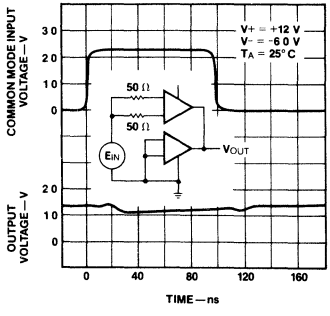
Voltage Gain as a Function of Supply Voltages



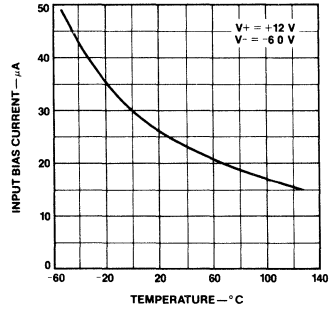
Output Pulse Stretching With Capacitive Loading



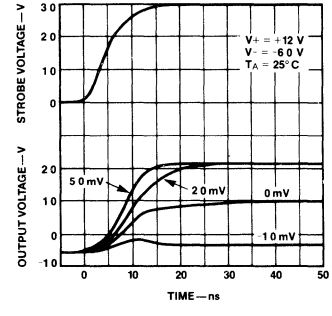
Common Mode Pulse Response



Input Bias Current as a Function of Ambient Temperature

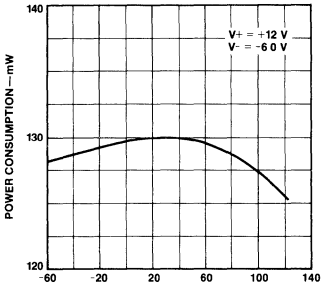


Strobe Release Time for Various Input Overdrives



Typical Performance Curves (Cont.)

Power Consumption as a Function of Ambient Temperature



5

FAIRCHILD

A Schlumberger Company

μA734 Precision Voltage Comparator

Linear Products

Description

The μA734 is a Precision Voltage Comparator constructed on a single silicon chip using the Fairchild Planar epitaxial process. It is specifically designed for high accuracy level sensing and measuring applications. The μA734 is extremely useful for analog-to-digital converters with 12-bit accuracies and one mega-bit conversion rates. Maximum resolution is obtained by high gain, low input offset current, and low input offset voltage. Its superior temperature stability can be improved by offset nulling which further reduces offset voltage drift. Balanced or unbalanced supply operation and standard TTL logic compatibility enhance the μA734 versatility.

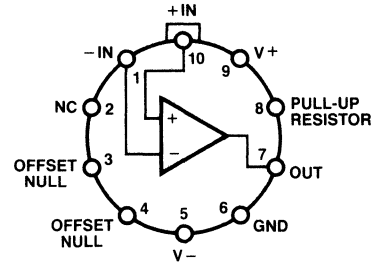
- **CONSTANT INPUT IMPEDANCE OVER DIFFERENTIAL INPUT RANGE**
- **HIGH INPUT IMPEDANCE—55 MΩ**
- **LOW DRIFT—3.5 μV/°C**
- **HIGH GAIN—60 k**
- **BALANCED OFFSET NULL CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE— ±5 V to ±18 V**
- **TTL COMPATIBLE**

Absolute Maximum Ratings	T_A = 25°C unless specified otherwise
Supply Voltage	±18 V
Peak Output Current	10 mA
Differential Input Voltage	±10 V
Input Voltage Range (Note 1)	±13 V
Voltage Between Offset Null and V−	±0.5 V
Internal Power Dissipation (Note 2)	
Metal Package	500 mW
Ceramic DIP	670 mW
Operating Temperature Range	
Military (μA734)	−55°C to +125°C
Commercial (μA734C)	0°C to +70°C
Storage Temperature Range	
Metal Can, DIP	−65°C to +150°C
Pin Temperature (Soldering, 60 s Max)	300°C

Notes

1. Rating applies for ±15 V supplies. For other supply voltages the rating is within 2 V of either supply.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6 3 mW/°C for metal package, 8 3 mW/°C for DIP.

Connection Diagram
10-Pin Metal Package

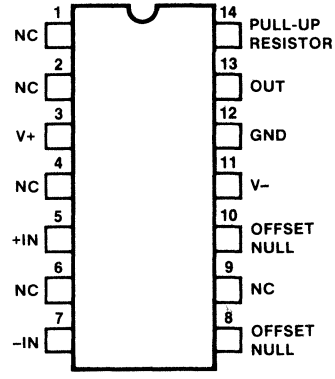


(Top View)

Order Information

Type	Package	Code	Part No.
μA734	Metal	5N	μA734HM
μA734C	Metal	5N	μA734HC

Connection Diagram
14-Pin DIP

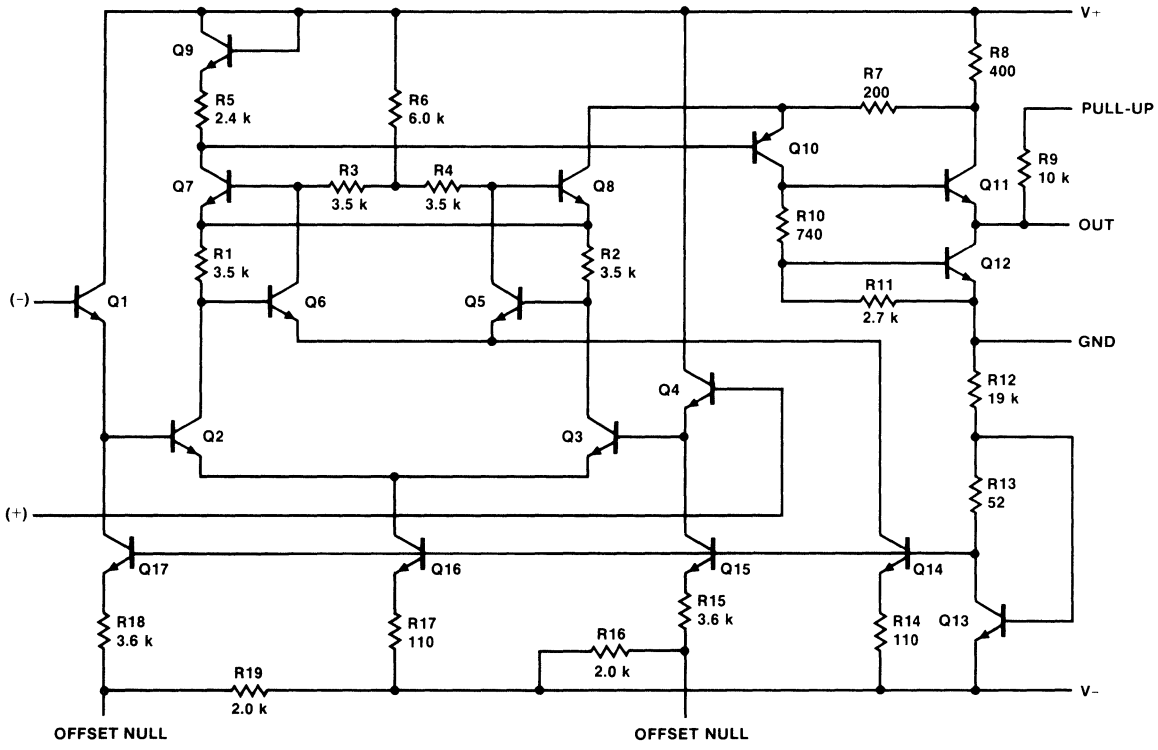


(Top View)

Order Information

Type	Package	Code	Part No.
μA734	Ceramic DIP	6A	μA734DM
μA734C	Ceramic DIP	6A	μA734DC

Equivalent Circuit



5

μA734C Electrical Characteristics $T_A = 25°C$, Pin 8 tied to +15 V, unless otherwise specified, $V\pm = \pm 15V$. (Note 3)

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.1	5.0	mV
Input Offset Current			3.5	25	nA
Input Bias Current			30	100	nA
Input Resistance		7.0	55		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	35 k	60 k		V/V
Positive Supply Current Output LOW			4.0	5.0	mA
Negative Supply Current Output LOW			1.5	2.0	mA
Power Consumption—Output LOW			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.2	7.5	mV
Input Offset Current			4.0	45	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leq 50\ \Omega$		3.5	20	μV/°C
Average Input Offset Current Drift	T_A = +25°C to +70°C		0.02	0.3	nA/°C
	T_A = +25°C to 0°C		0.05	0.75	nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio V_S = ±5 V to ±18 V	$R_S \leq 50\ k\Omega$		6.0	100	μV/V
Output HIGH Voltage	I_{OUT} = 0.080 mA	7.0			V
	I_{OUT} = 0.080 mA, V_8 = +5.0 V	2.4		5.0	V
Output LOW Voltage	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current Output LOW				7.0	mA
Negative Supply Current Output LOW				2.5	mA
Power Dissipation—Output LOW				145	mW

Note

3. Pin numbers refer to metal package.

μA734 Electrical Characteristics $T_A = 25°C$, Pin 8 tied to +15 V, unless otherwise specified, $V\pm = \pm 15$ V. (Note 3)

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage	$R_S \leq 50$ kΩ		0.9	3.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			28	50	nA
Input Resistance		20	60		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	35 k	70 k		V/V
Positive Supply Current Output LOW			4.0	5.0	mA
Negative Supply Current Output LOW			1.5	2.0	mA
Power Consumption—Output LOW			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage	$R_S \leq 50$ kΩ		1.1	4.0	mV
Input Offset Current			3.0	20	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leq 50$ kΩ		2.5	15	μV/°C
Average Input Offset Current Drift	T_A = +25°C to +125°C T_A = +25°C to −55°C		0.01 0.05	0.1 0.4	nA/°C nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		± 10			V
Differential Input Voltage Range		± 10			V
Common Mode Rejection Ratio	$R_S \leq 50$ kΩ	70	100		dB
Supply Voltage Rejection Ratio V_S = ±5 V to ±18 V	$R_S \leq 50$ kΩ		5.0	100	μV/V
Output HIGH Voltage	I_{OUT} = 0.080 mA I_{OUT} = 0.080 mA, V_8 = +5.0 V	7.0 2.4		5.0	V V
Output LOW Voltage	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current Output LOW				7.0	mA
Negative Supply Current Output LOW				2.5	mA
Power Dissipation—Output LOW				145	mW

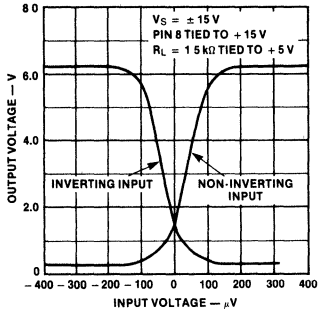
5

Note

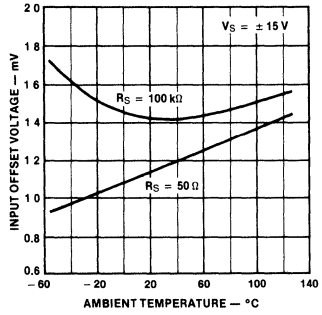
3. Pin numbers refer to metal package.

Typical Performance Curves For μA734 and μA734C

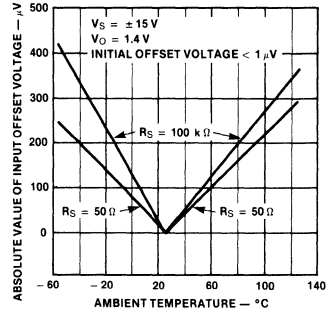
Transfer Characteristics



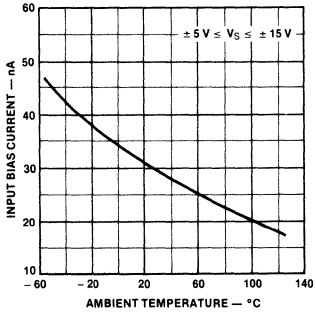
Un-Nulled Input Offset Voltage vs. Ambient Temperature



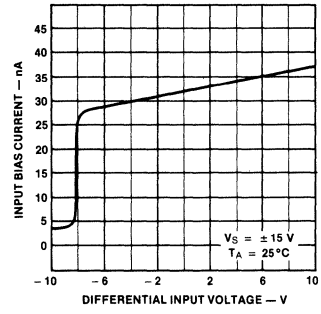
Input Offset Voltage Change vs. Ambient Temperature Nulled to Zero at 25°C



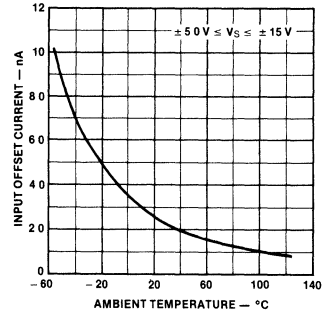
Input Bias Current vs. Ambient Temperature



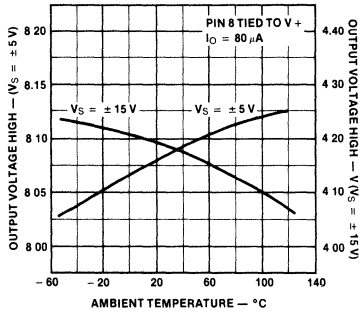
Input Bias Current vs. Differential Input Voltage



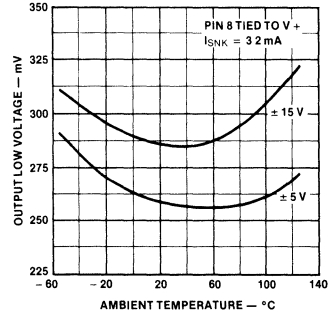
Input Offset Current vs. Ambient Temperature



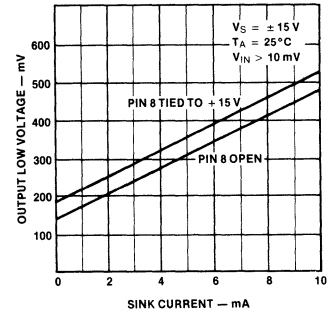
Output High Voltage vs. Supply Voltage and Ambient Temperature



Output Low Voltage vs. Supply Voltage and Ambient Temperature

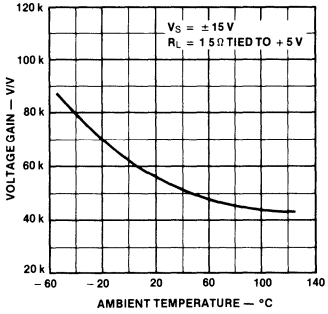


Output Voltage Low vs. Sink Current

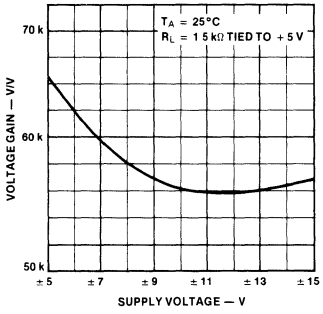


Typical Performance Curves for μA734 and μA734C (Cont.)

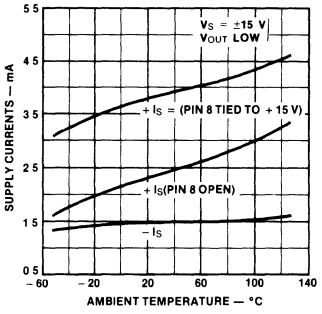
Voltage Gain vs. Ambient Temperature



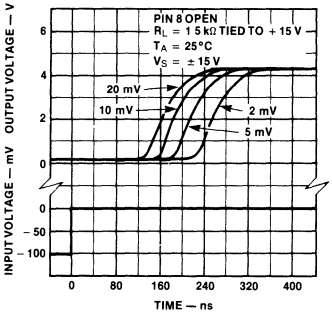
Voltage Gain vs. Supply Voltage



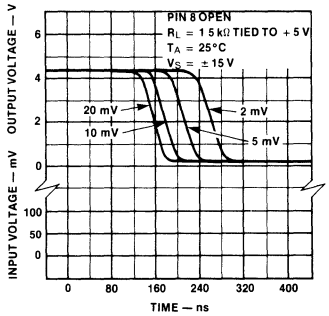
Positive and Negative Supply Currents vs. Ambient Temperature



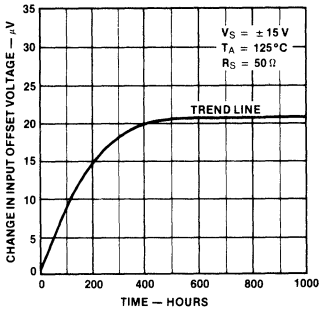
Response Time For Various Input Overdrives



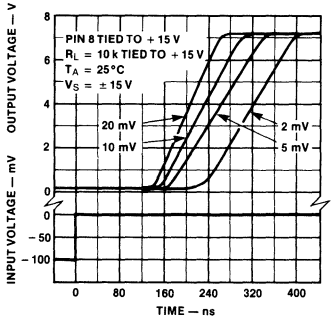
Response Time For Various Input Overdrives



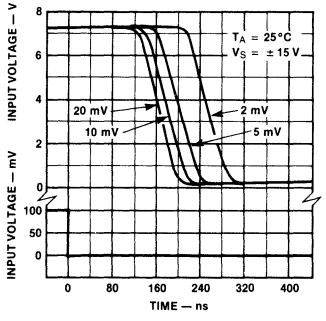
Input Offset Voltage Drift vs. Time



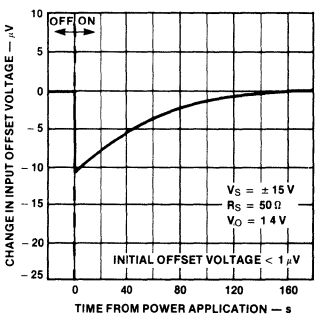
Response Time For Various Input Overdrives



Response Time For Various Input Overdrives

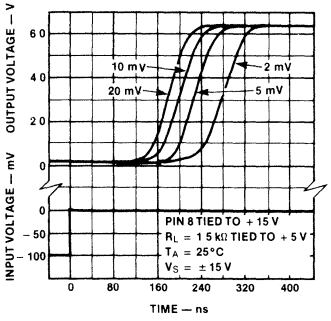


Stabilization Time of Input Offset Voltage From Power Turn-On

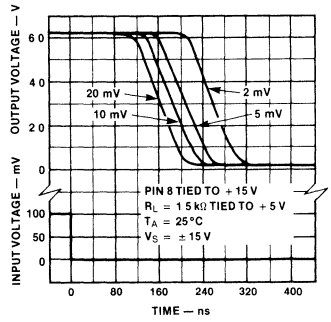


Typical Performance Curves for μA734 and μA734C (Cont.)

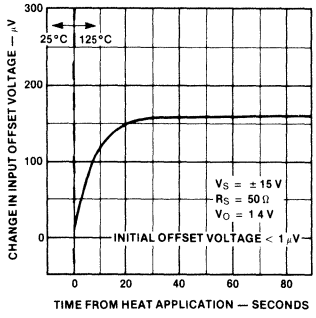
Response Time For Various Input Overdrives



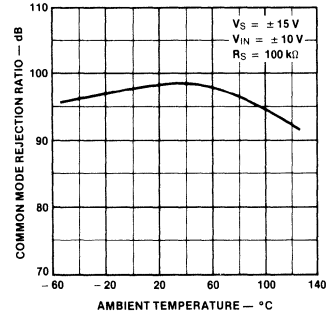
Response Time For Various Input Overdrives



Thermal Response of Input Offset Voltage To Step Change of Case Temperature

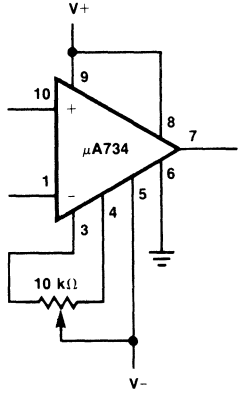


Common Mode Rejection Ratio vs. Ambient Temperature

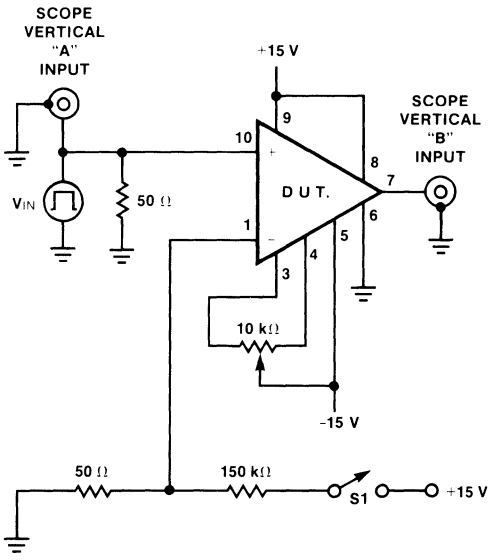


Test Circuits

Offset Null Circuit

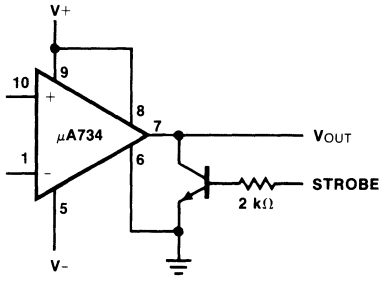


AC Test Circuit

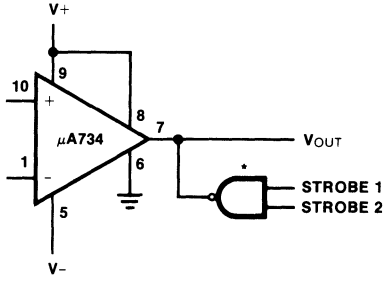


Typical Applications

Strobe Circuitry



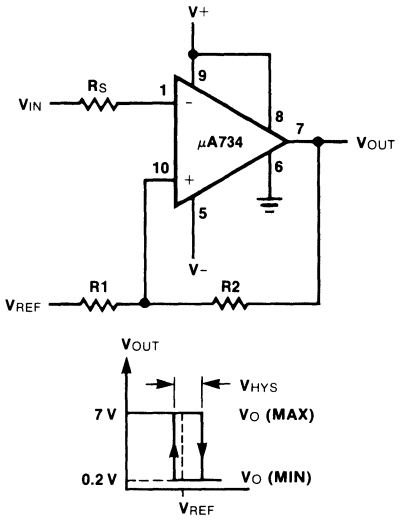
Alternate Strobe Circuitry



* ½ 9944

Typical Applications (Cont.)

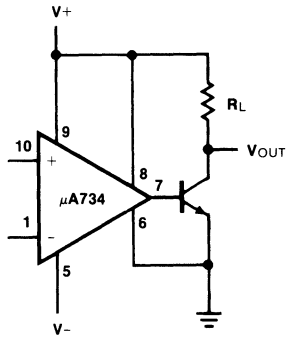
Level Detector With Hysteresis



$$R_S = \frac{R_1 R_2}{R_1 + R_2} \text{ FOR MINIMUM OFFSET}$$

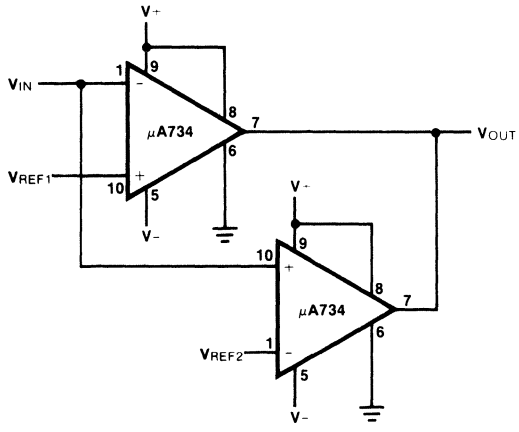
$$V_{HYS} = \frac{R_1 [V_{O\,MAX} - V_{O\,MIN}]}{R_1 + R_2}$$

High Power Output Circuits

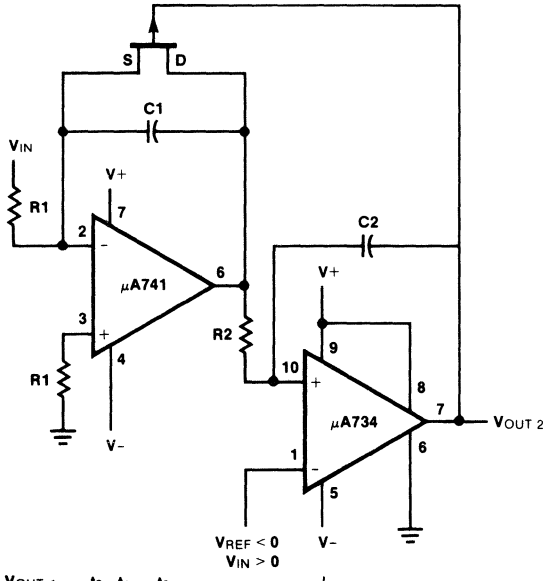


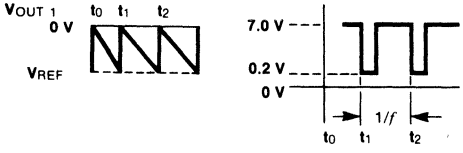
Typical Applications (Cont.)

Precision Dual Limit Go No Go Tester



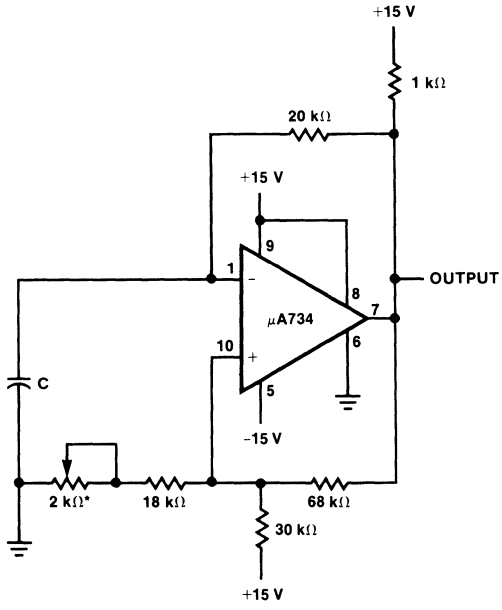
Voltage Controlled Oscillator

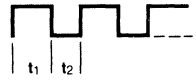




$$\frac{V_{IN}}{|V_{REF}|R_1 C_1} \qquad R_2 C_2 > \frac{|V_{REF}|C_1}{I_{DSS}}$$

Free Running Oscillator



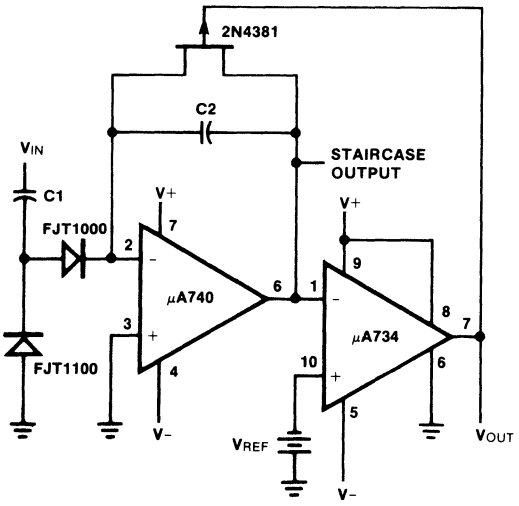


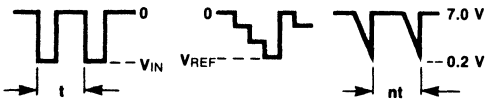
$C \cong 80 \times 10^{-6}\, t$

*Adjusts $\frac{T_1}{T_2}$

Typical Applications (Cont.)

Frequency Divider and Staircase Generator

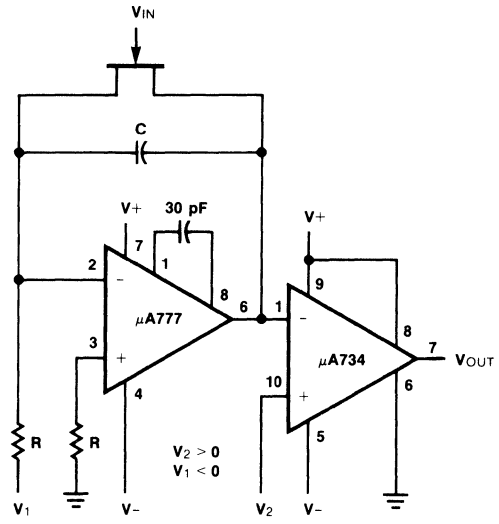




$$|V_{REF}| = 2V_D + N\left[3.5T + 2V_D - \frac{C_1 V_{IN}}{C_2}\right]$$

T in Seconds
V_D for FJT 1000 ≈ 0 31 V

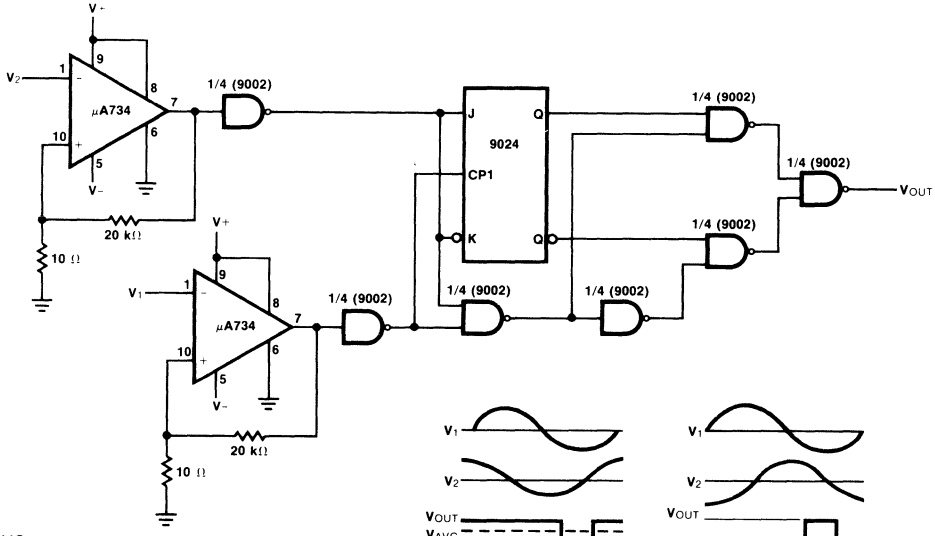
Pulse Width Discriminator



V_{OUT} Pulse Appears

Whenever $T > \frac{R\,C\,V_2}{V_1}$

Phase Meter



$$\phi = \frac{2\pi\, V_{AVG}}{V_{OUT,\,PEAK}} - \pi$$

FAIRCHILD
A Schlumberger Company

μA760 High-Speed Differential Comparator

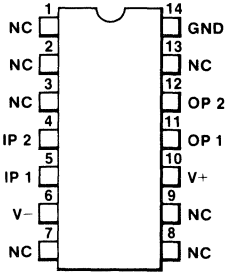
Linear Products

Description

The μA760 is a Differential Voltage Comparator offering considerable speed improvement over the μA710 family and operation from symmetric supplies of from ±4.5 V to ±6.5 V. The μA760 can be used in high-speed analog-to-digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The μA760 output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.

- **GUARANTEED HIGH SPEED—25 ns MAX**
- **GUARANTEED DELAY MATCHING ON BOTH OUTPUTS**
- **COMPLEMENTARY TTL COMPATIBLE OUTPUTS**
- **HIGH SENSITIVITY**
- **STANDARD SUPPLY VOLTAGES**

Connection Diagram
14-Pin DIP

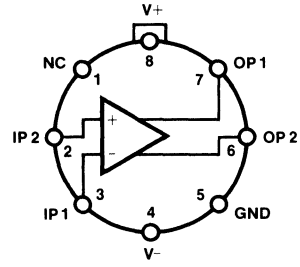


(Top View)

Order Information

Type	Package	Code	Part No.
μA760	Ceramic DIP	6A	μA760DM
μA760C	Ceramic DIP	6A	μA760DC

Connection Diagram
8-Pin Metal Package



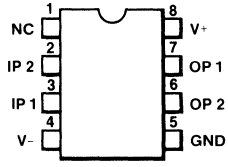
(Top View)

Pin 4 connected to case

Order Information

Type	Package	Code	Part No.
μA760	Metal	5W	μA760HM
μA760C	Metal	5W	μA760HC

Connection Diagram
8-Pin DIP



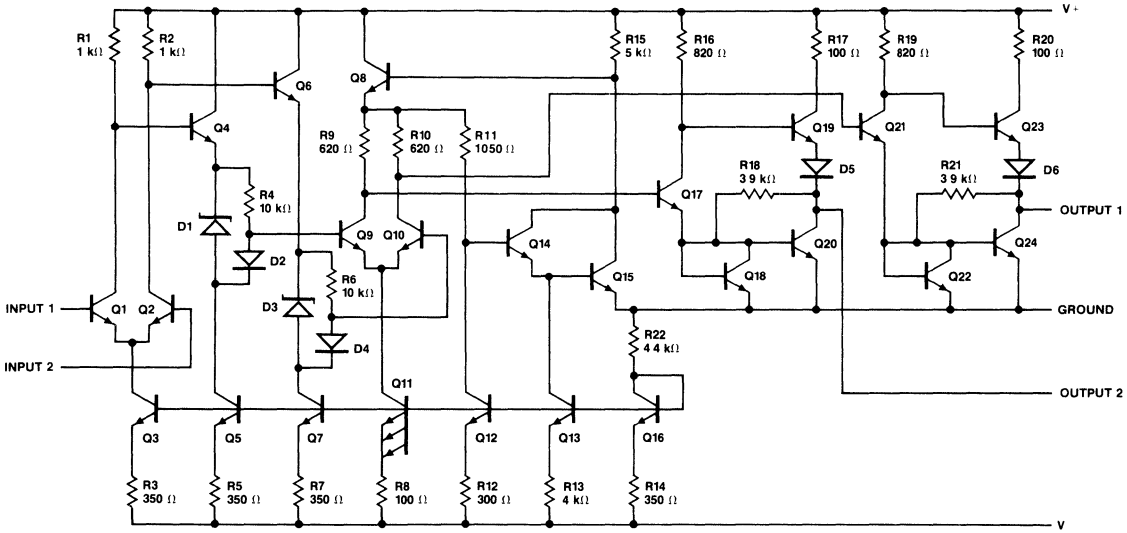
(Top View)

Order Information

Type	Package	Code	Part No.
μA760	Ceramic DIP	6T	μA760RM
μA760C	Ceramic DIP	6T	μA760RC

Absolute Maximum Ratings			
Positive Supply Voltage	+8 V	Operating Temperature Range	
Negative Supply Voltage	−8 V	Military (μA760)	−55°C to 125°C
Peak Output Current	10 mA	Commercial (μA760C)	0°C to 70°C
Differential Input Voltage	±5 V	Storage Temperature Range	
Input Voltage	$V+ \geq V_{IN} \geq V-$	Metal and Ceramic DIP	−65°C to 150°C
Internal Power Dissipation		Molded DIP	−55°C to 125°C
(Note 1)		Pin Temperature (Soldering)	
Metal Package	500 mW	Metal and Ceramic DIP	
DIP	670 mW	(60 s)	300°C
		Molded DIP	260°C

Equivalent Circuit



5

Note

1. Ratings applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal package and 8.3 mW/°C for the ceramic DIP. For molded DIP, derate at 6.7 mW/°C above 30°C ambient temperature.

μA760
Electrical Characteristics $V_S = \pm 4.5$ V to ± 6.5 V, $T_A = -55°C$ to $+125°C$, $T_A = 25°C$ for typical figures unless otherwise specified.

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	(Note 2), $T_A = 25°C$		18	30	ns
	(Note 3), $T_A = 25°C$			25	ns
	(Note 4)		16		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	(Note 2), $T_A = 25°C$			5.0	ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	(Note 2), $T_A = 25°C$			5.0	ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	(Note 2), $T_A = 25°C$			7.5	ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	(Note 2), $T_A = 25°C$			7.5	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = -55°C$ to $T_A = +125°C$		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$		2.0		nA/°C
	$T_A = 25°C$ to $T_A = -55°C$		7.0		nA/°C
Input Voltage Range	$V_S = \pm 6.5$ V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		V
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0$ mA	2.4	3.2		V
	$V_S = \pm 5.0$ V	2.4	3.0		V
	$I_{OUT} = 80\ \mu A$, $V_S = \pm 4.5$ V				
Output LOW Voltage (either output)	$I_{SINK} = 3.2$ mA		0.25	0.4	V
Positive Supply Current	$V_S = \pm 6.5$ V		18	32	mA
Negative Supply Current	$V_S = \pm 6.5$ V		9.0	16	mA

Notes

2. Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output
3. Response time measured from the 50% point of a 2 $V_{pk\text{-}pk}$ 10 MHz sinusoidal input to the 50% point of the output
4. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

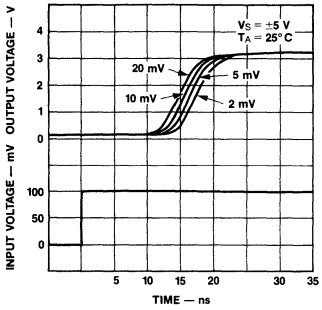
μA760C
Electrical Characteristics $V_S = \pm 4.5$ V to 6.5 V, $T_A = 0°C$ to $70°C$, $T_A = 25°C$ for typical figures unless otherwise specified.

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	(Note 2), $T_A = 25°C$ (Note 3), $T_A = 25°C$ (Note 4)		18 16	30 25	ns ns ns
Response Time Difference between Outputs (t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$) (t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$) (t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$) (t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	 (Note 2), $T_A = 25°C$ (Note 2), $T_A = 25°C$ (Note 2), $T_A = 25°C$ (Note 2), $T_A = 25°C$			 5.0 5.0 10 10	 ns ns ns ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0°C$ to $T_A = +70°C$		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$ $T_A = 25°C$ to $T_A = 0°C$		5.0 10		nA/°C nA/°C
Input Voltage Range	$V_S = \pm 6.5$ V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0$ mA $V_S = \pm 5.0$ V $I_{OUT} = 80\ \mu A$, $V_S = \pm 4.5$ V	 2.4 2.5	 3.2 3.0		 V V
Output LOW Voltage (either output)	$I_{SINK} = 3.2$ mA		0.25	0.4	V
Positive Supply Current	$V_S = \pm 6.5$ V		18	34	mA
Negative Supply Current	$V_S = \pm 6.5$ V		9.0	16	mA

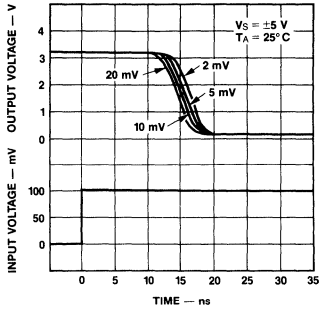
Notes
2. Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
3. Response time measured from the 50% point of a 2 $V_{pk\text{-}pk}$ 10 MHz sinusoidal input to the 50% point of the output.
4. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Typical Performance Curves

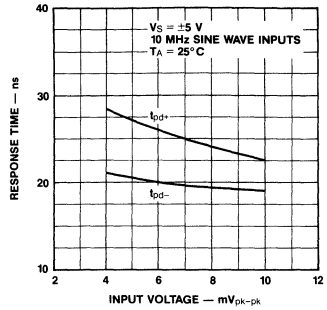
Response Time for Various Input Overdrives



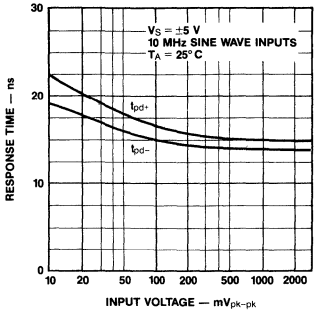
Response Time for Various Input Overdrives



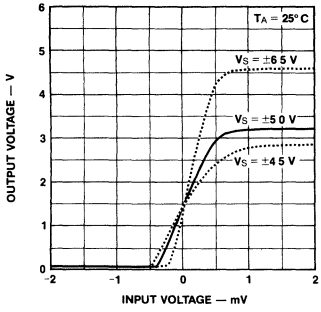
Response Time as a Function of Input Voltage



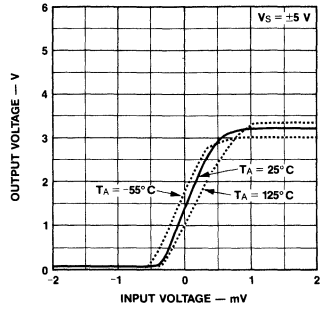
Response Time as a Function of Input Voltage



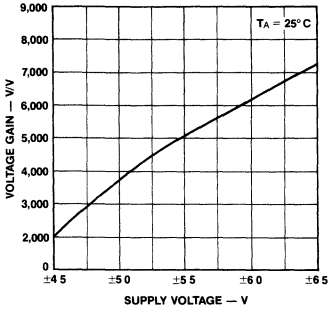
Voltage Transfer Characteristic



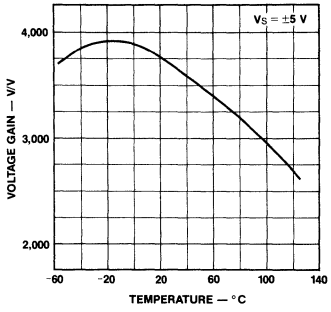
Voltage Transfer Characteristic



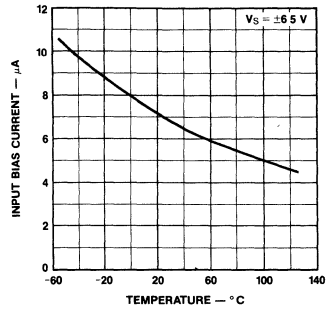
Voltage Gain as a Function of Supply Voltage



Voltage Gain as a Function of Ambient Temperature

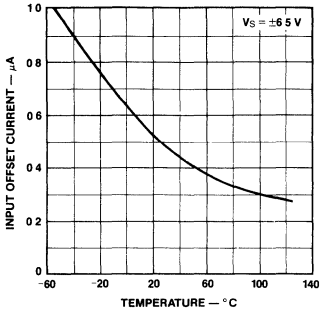


Input Bias Current as a Function of Ambient Temperature

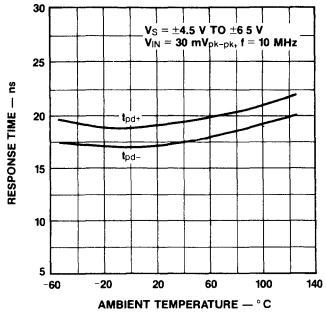


Typical Performance Curves (Cont.)

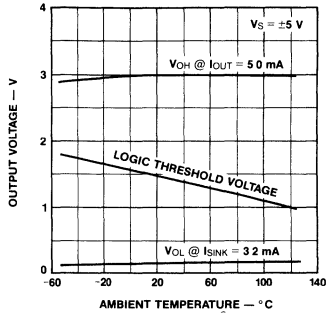
Input Offset Current as a Function of Ambient Temperature



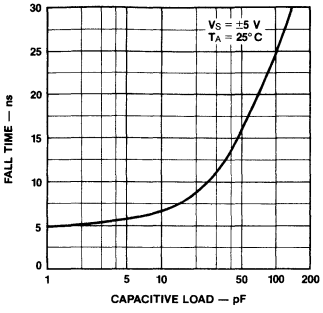
Response Time as a Function of Ambient Temperature



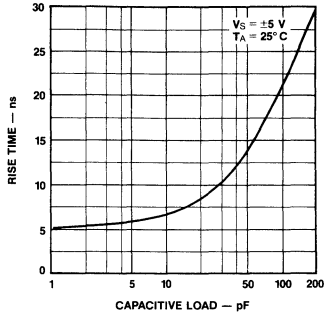
Output Voltage Levels as a Function of Ambient Temperature



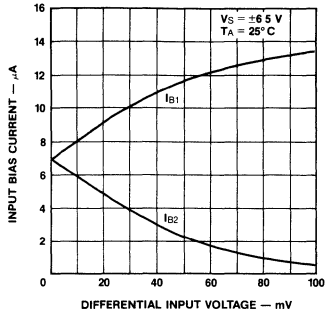
Rise Time as a Function of Capacitive Load



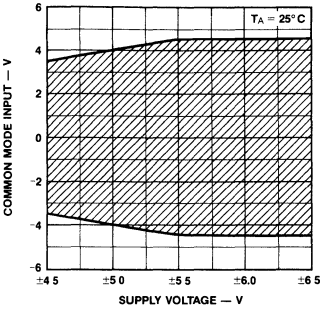
Fall Time as a Function of Capacitive Load



Input Bias Current as a Function of Differential Input Voltage



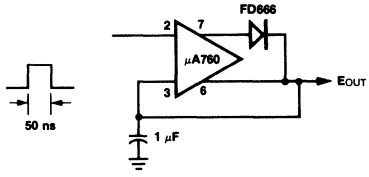
Common Mode Range as a Function of Supply Voltage



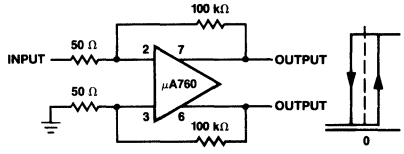
5

Typical Applications

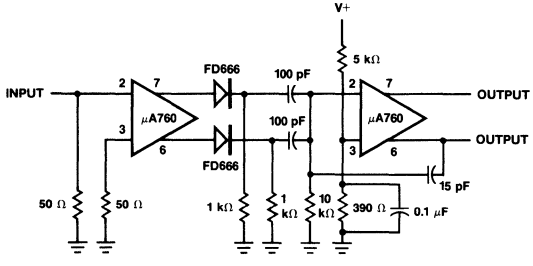
Fast Positive Peak Detector



Level Detector with Hysteresis

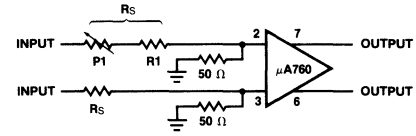


Zero Crossing Detector



Total Delay = 30 ns
Input frequency = 300 Hz to 3 MHz
Minimum input voltage = 20 mVpk-pk

Line Receiver With High Common Mode Range



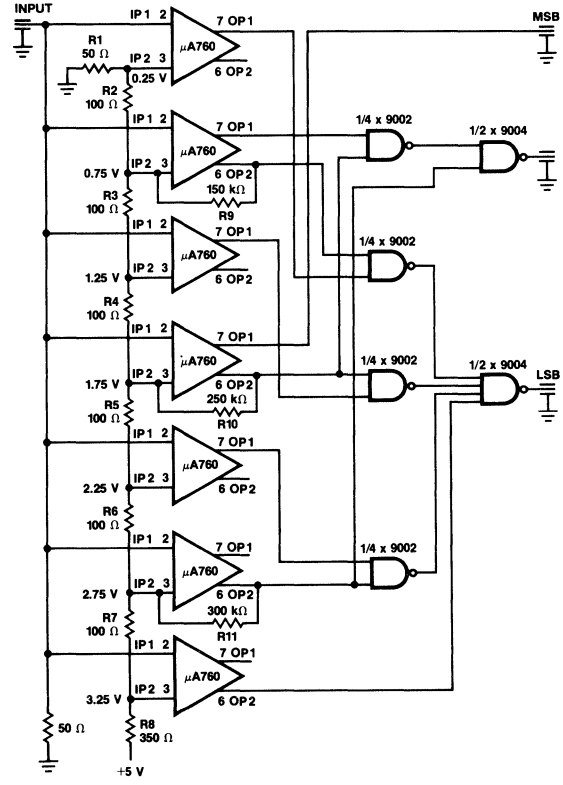
Common mode range = $\pm 4 \times \frac{RS}{50}$ V

Differential input sensitivity = $5 \times \frac{RS}{50}$ mV

P_1 must be adjusted for optimum common mode rejection.

For R_S = 200 Ω
Common mode range = ± 16 V
Sensitivity = 20 mV

High-Speed 3-Bit A/D Converter



Input voltage range: 3.5 V
Typical conversion speed: 30 ns

Pin numbers shown are for Metal Package only.

FAIRCHILD
A Schlumberger Company

μA111 • μA311
Voltage Comparators

Linear Products

DESCRIPTION

The μA111 and μA311 are monolithic, low input current Voltage Comparators, each constructed using the Fairchild Planar epitaxial process. The μA111 series operates from the single 5 V integrated circuit logic supply to the standard ±15 V operational amplifier supplies. The μA111 series is intended for a wide range of applications including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.

- **LOW INPUT BIAS CURRENT 150 nA MAX (111), 250 nA MAX (311)**
- **LOW INPUT OFFSET CURRENT 20 nA MAX (111), 50 nA MAX (311)**
- **DIFFERENTIAL INPUT VOLTAGE ±30 V**
- **POWER SUPPLY VOLTAGE SINGLE 5.0 V SUPPLY TO ±15 V**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **STROBE CAPABILITY**

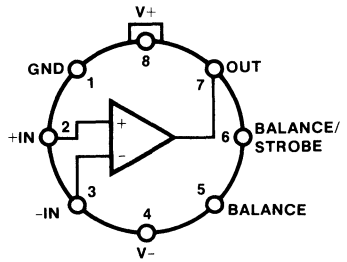
Absolute Maximum Ratings

Voltage Between V+ and V− Terminals	36 V
Output to V− (μA111)	50 V
(μA311)	40 V
Ground to V−	30 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	500 mW
Output Short-Circuit Duration	10 s
Storage Temperature Range	
Metal and Ceramic DIP	−65°C to +150°C
Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA111)	−55°C to +125°C
Commercial (μA311)	0°C to +70°C
Pin Temperature (Soldering)	
Metal and Ceramic (60 s)	300°C
Molded (10 s)	260°C

Notes

1. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C to Metal Package, 8.3 mW/°C for mini DIP.

Connection Diagram
8-Pin Metal Package

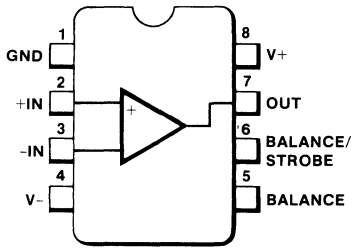


(Top View)

Order Information

Type	Package	Code	Part No.
μA111	Metal	5W	μA111HM
μA311	Metal	5W	μA311HC

Connection Diagram
8-Pin Mini DIP

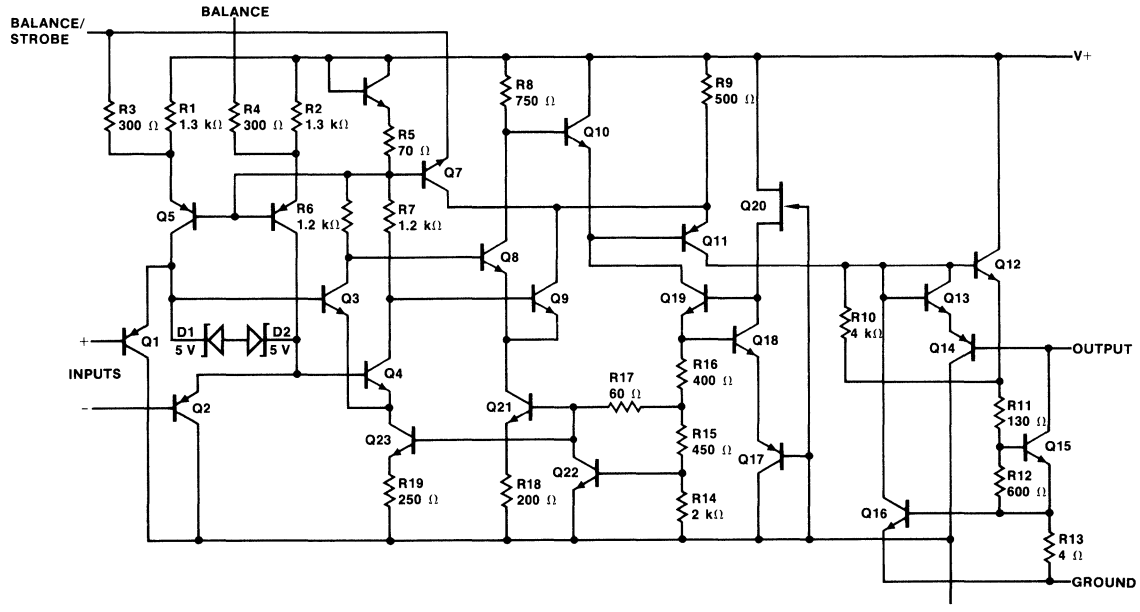


(Top View)

Order Information

Type	Package	Code	Part No.
μA111	Ceramic DIP	6T	μA111RM
μA311	Ceramic DIP	6T	μA311RC
μA311	Molded DIP	9T	μA311TC

Equivalent Circuit



μA111

Electrical Characteristics $V_S = \pm 15$ V, $T_A = -55°C$ to $+125°C$ unless otherwise specified. (Note 3)

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50\ k\Omega$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35$ V $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50\ k\Omega$			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq 4.5$ V, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35$ V		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Notes on following pages.

μA311

Electrical Characteristics $V_S = \pm 15$ V, $T_A = 0°C$ to $+ 70°C$ unless otherwise specified. (Note 3)

Characteric	Condition	Min	Typ	Max	Unit
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50\ k\Omega$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35$ V $T_A = 25°C$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50\ k\Omega$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			± 14		V
Saturation Voltage	$V^+ \geq 4.5$ V, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

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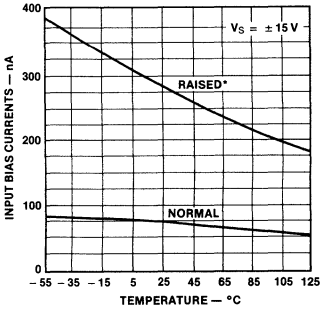
Notes

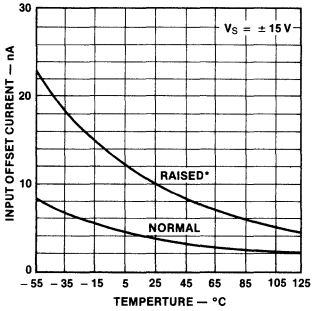
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5 V supply up to ± 15 V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Typical Performance Curves for μA111

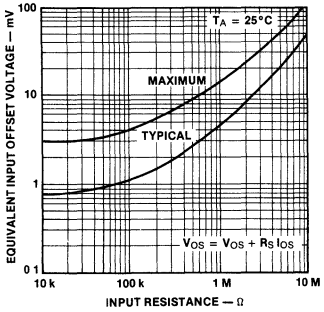
Input Bias Current as a Function of Temperature



Input Offset Current as a Function of Temperature



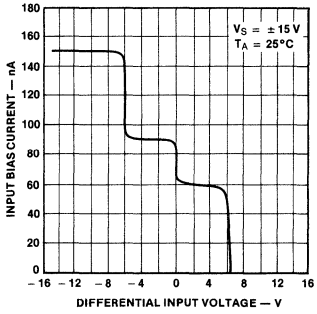
Offset Voltage as a Function of Input Resistance



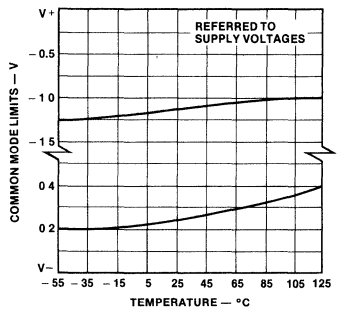
*Pins 5, 6 and 8 are shorted.

Typical Performance Curves for μA111

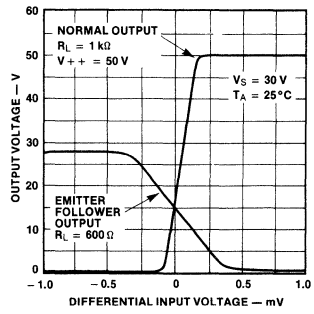
Input Bias Current as a Function of Differential Input Voltage



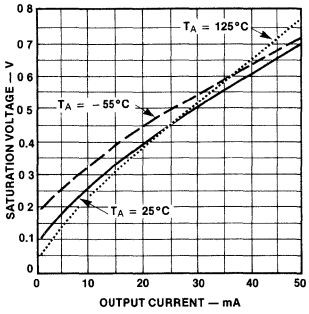
Common Mode Limits as a Function of Temperature



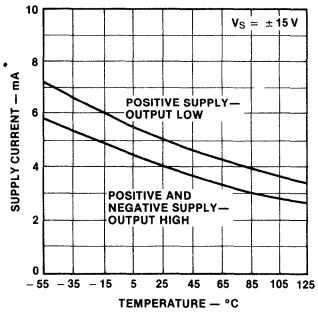
Output Voltage as a Function of Differential Input Voltage



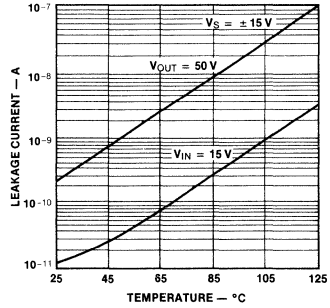
Output Saturation Voltage as a Function of Output Current



Supply Current as a Function of Temperature

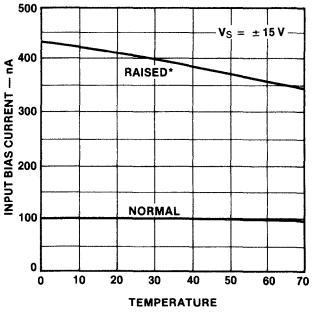


Leakage Current as a Function of Temperature

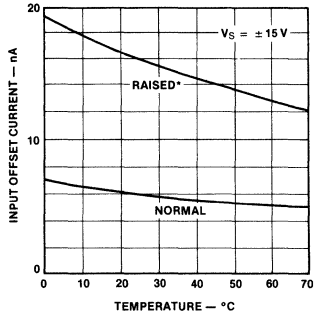


Typical Performance Curves for μA311

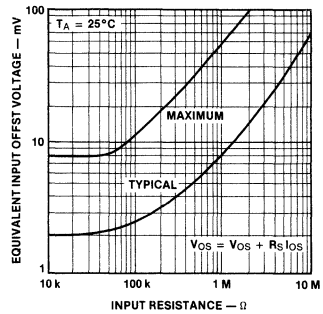
Input Bias Current as a Function of Temperature



Input Offset Current as a Function of Temperature



Offset Voltage as a Function of Input Resistance

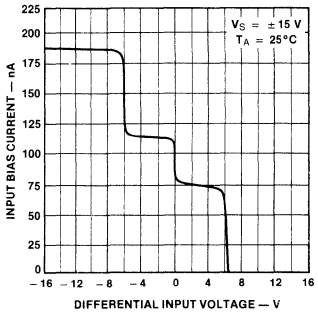


*Pins 5, 6 and 8 are shorted.

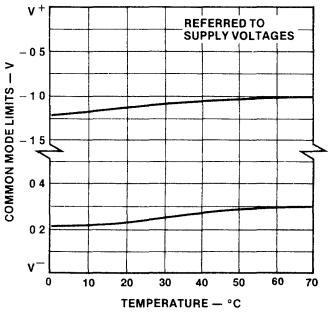
*Pins 5, 6 and 8 are shorted.

Typical Performance Curves for μA311 (Cont.)

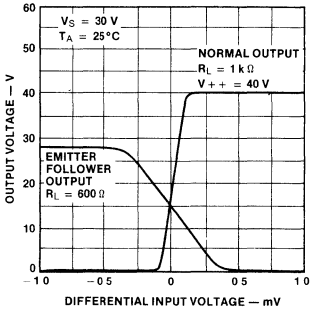
Input Bias Current as a Function of Differential Input Voltage



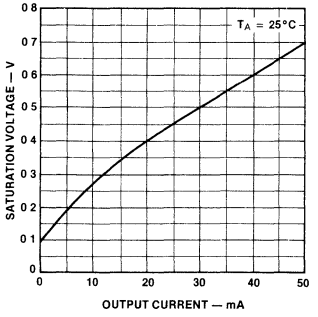
Common Mode Limits as a Function of Temperature



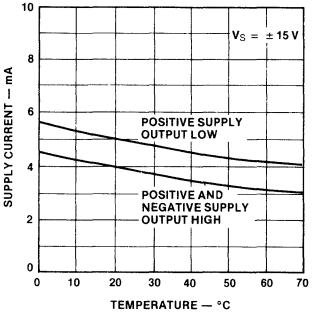
Output Voltage as a Function of Differential Input Voltage



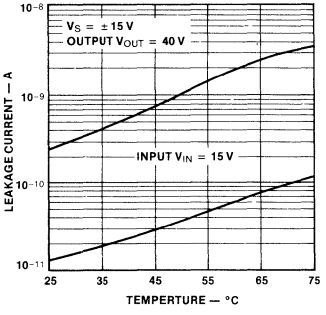
Saturation Voltage as a Function of Current



Supply Current as a Function of Temperature

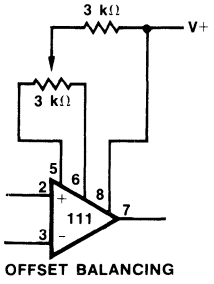


Leakage Currents as a Function of Temperature

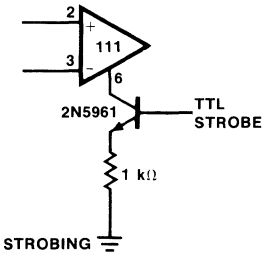


Typical Applications

Offset Null Circuit

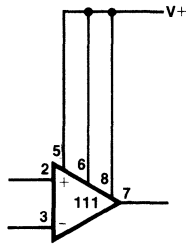


Strobe Circuit



Typical Applications (Cont.)

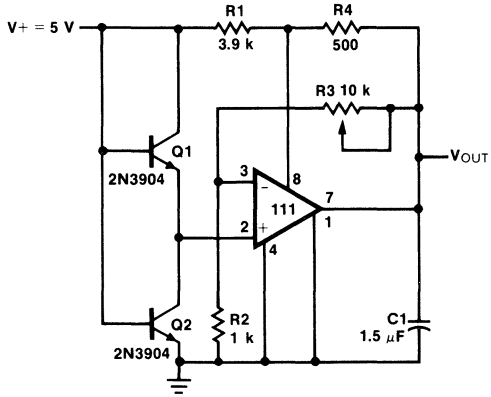
Increasing Input Stage Current*



Note

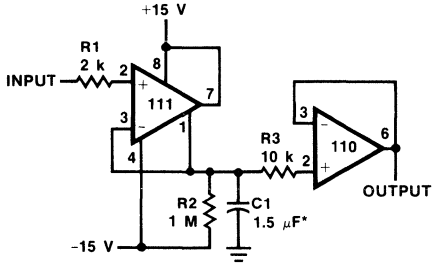
*Increases typical common mode slew rate from 7.0 V/μs to 18 V/μs.

Adjustable Low Voltage Reference Supply



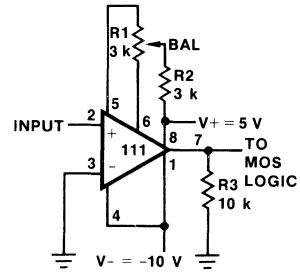
*Solid tantalum

Positive Peak Detector



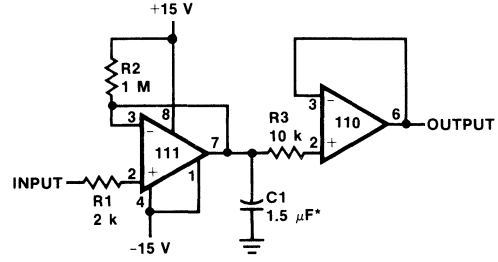
*Solid tantalum

Zero Crossing Detector Driving MOS Logic



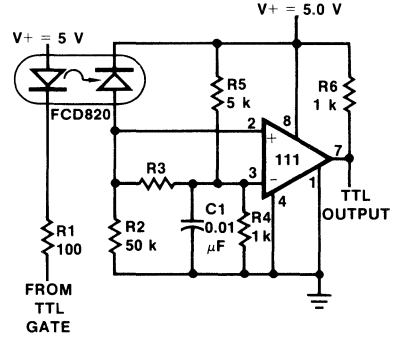
*Solid tantalum

Negative Peak Detector



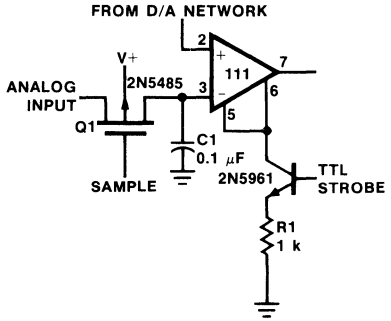
*Solid tantalum

Digital Transmission Isolator



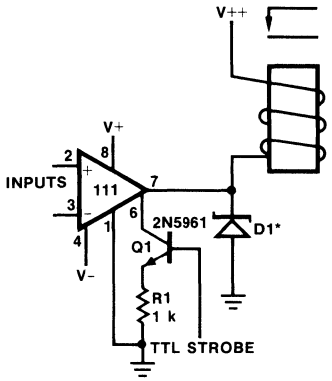
Typical Applications (Cont.)

Strobing of Both Input And Output Stages



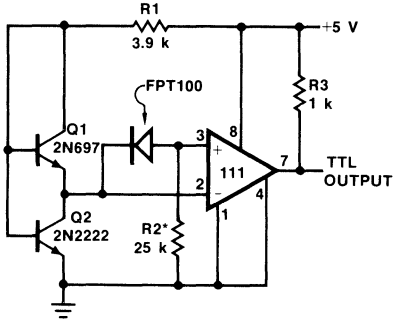
*Typical input current is 50 pA with inputs strobed off.

Relay Driver with Strobe



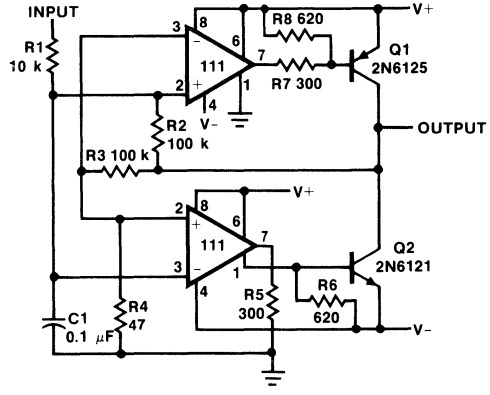
*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

Precision Photodiode Comparator

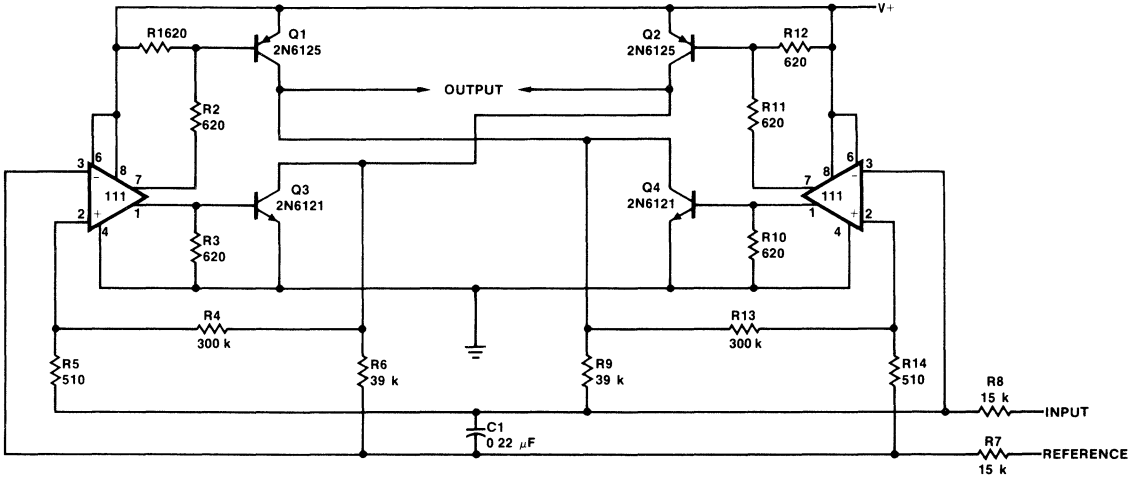


*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude

Switching Power Amplifier



Switching Power Amplifier



FAIRCHILD
A Schlumberger Company

μA139 • μA239 • μA339 μA2901 • μA3302 Quad Comparators

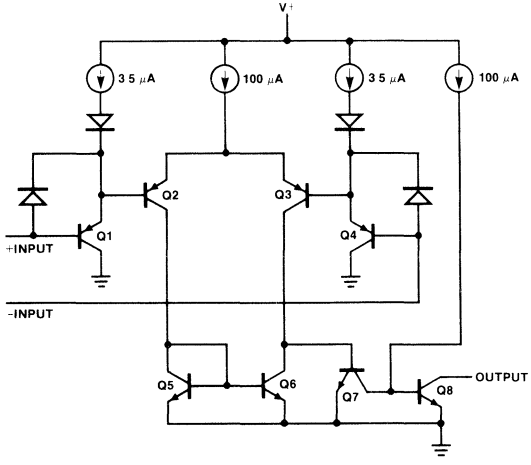
Linear Products

Description

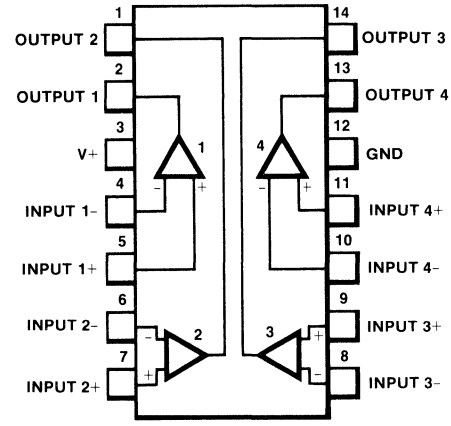
The μA139 series consists of four independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected pnp input stages allow the input common-mode voltage to include ground.

- **SINGLE SUPPLY OPERATION +2.0 V TO +36 V**
- **DUAL SUPPLY OPERATION ±1.0 V TO ±18 V**
- **ALLOW COMPARISON OF VOLTAGES NEAR GROUND POTENTIAL**
- **LOW CURRENT DRAIN 800 μA TYP**
- **COMPATIBLE WITH ALL FORMS OF LOGIC**
- **LOW INPUT BIAS CURRENT 25 nA TYP**
- **LOW INPUT OFFSET CURRENT ±5 nA TYP**
- **LOW OFFSET VOLTAGE ±2 mV**

Schematic Diagram



Connection Diagram 14-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA139A	Ceramic DIP	6A	μA139ADM
μA139	Ceramic DIP	6A	μA139DM
μA239A	Ceramic DIP	6A	μA239ADC
μA239A	Molded DIP	9A	μA239APC
μA239	Ceramic DIP	6A	μA239DC
μA239	Molded DIP	9A	μA239PC
μA339A	Ceramic DIP	6A	μA339ADC
μA339A	Molded DIP	9A	μA339APC
μA339	Ceramic DIP	6A	μA339DC
μA339	Molded DIP	9A	μA339PC
μA2901	Ceramic DIP	6A	μA2901DC
μA2901	Molded DIP	9A	μA2901PC
μA3302	Ceramic DIP	6A	μA3302DC
μA3302	Molded DIP	9A	μA3302PC

Absolute Maximum Ratings

	μA139/μA239/μA339 μA139A/μA239A/μA339A μA2901	μA3302
Supply Voltage, V+	36 V or ± 18 V	28 V or ± 14 V
Differential Input Voltage	36 V	28 V
Input Voltage Range	−0.3 V to +36 V	−0.3 V to +28 V
Power Dissipation (Note 1) 9A, 6A	1 W	1 W
Output Short Circuit to GND, (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3$ V), (Note 3)	50 mA	50 mA
Operating Temperature Range		
μA339, μA339A	0°C to +70°C	
μA239, μA239A	−25°C to +85°C	
μA139, μA139A	−55°C to +125°C	
μA2901, μA3302	−40°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Pin Temperature (Soldering)		
Ceramic DIP (60 s)	300°C	300°C
Molded DIP (10 s)	260°C	260°C

5

Factors Important to Maximum Ratings and Electrical Characteristics

Notes

1. For operating at high temperatures, the μA339/μA339A, μA2901, μA3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 125°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient The μA139 and μA139A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V+
3. This input current will exist only when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input pnp transistors becoming forward biased and thereby acting as input diode clamps. In addition to diode action, there is also lateral npn parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level or to ground for a large over-drive, for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which is negative, again returns to a value greater than −0.3 V.
4. These specifications apply for V+ = 5.0 V and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the μA239/μA239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the μA339/μA339A temperature specifications are limited to $0°C \leq T_A \leq -70°C$, and the μA2901, μA3302 temperature range is $-40°C \leq T_A \leq +85°C$.
5. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go to +30 V without damage.
7. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained; see typical performance characteristics section
8. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V or 0.3 V below the magnitude of the negative power supply, if used.
9. At output switch point, $V_O \cong 1.4$ V, $R_S = 0\ \Omega$ with V+ from 5 V; and over the full input common-mode range 0 V to V+ −1.5 V.
10. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5 V supply, V_{IN} should be limited to 25 V maximum and a limiting resistor should be used on all inputs that might exceed the positive supply

Electrical Characteristics V+ = 5 V (Note 4)

Characteristic	Condition	μA139A			μA239A, μA339A			μA139			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C (Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = 25°C (Note 5)		25	100		25	250		25	100	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		±5.0	±25		±5.0	±50		±5.0	±25	nA
Input Common-Mode Voltage Range	T_A = 25°C (Note 6)	0		V+ −1.5	0		V+ −1.5	0		V+ −1.5	V
Supply Current	R_L = ∞ on all Comparators, T_A = 25°C		0.8	2.0		0.8	2.0		0.8	2.0	mA
	R_L = ∞, V+ = 30 V, T_A = 25°C										
Voltage Gain	$R_L \geq 15\ k\Omega$, V+ = 15 V, (To Support Large V_O Swing) T_A = 25°C	50	200		50	200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{ref} = 1.4 V, V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C		300			300			300		ns
Response Time	V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C (Note 7)		1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, $V_O \leq 1.5$ V, T_A = 25°C	6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4.0$ mA, T_A = 25°C		250	400		250	400		250	400	mV
Output Leakage Current	$V_{IN(+)} \geq 1.0$ V, $V_{IN(-)}$ = 0, V_O = 30 V, T_A = 25°C			200			200			200	nA
Input Offset Voltage	(Note 9)			4.0			4.0			9.0	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150			±100	nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300	nA
Input Common-Mode Voltage Range		0		V+ −2.0	0		V+ −2.0	0		V+ −2.0	V
Saturation Voltage	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4$ mA			700			700			700	mV
Output Leakage Current	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, V_O = 30 V			1.0			1.0			1.0	μA
Differential Input Voltage	Keep all $V_{INs} \geq 0$ V (or V−, if used) (Note 8)			V+			V+			36	V

Notes on following page

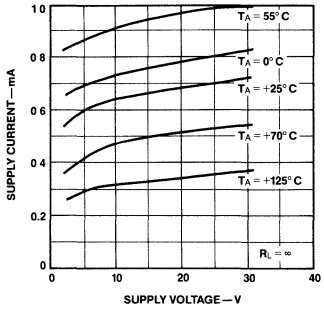
Electrical Characteristics V+ = 5 V (Note 4)

Characteristic	Condition	μA239, μA339			μA2901			μA3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C (Note 9)		±2.0	±5.0		±2.0	±7.0		±3.0	±20	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = 25°C (Note 5)		25	250		25	250		25	500	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		±5.0	±50		±5.0	±50		±5.0	±100	nA
Input Common-Mode Voltage Range	T_A = 25°C (Note 6)	0		V+ −1.5	0		V+ −1.5	0		V+ −1.5	V
Supply Current	$R_L = \infty$ on all Comparators, T_A = 25°C		0.8	2.0		0.8	2.0		0.8	2.0	mA
	$R_L = \infty$, V+ = 30 V, T_A = 25°C					1.0	2.5				
Voltage Gain	$R_L \geq 15$ kΩ, V+ = 15 V, To Support Large V_O Swing, T_A = 25°C		200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{ref} = 1.4 V, V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C		300			300			300		ns
Response Time	V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C (Note 7)		1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, $V_O \leq 1.5$ V, T_A = 25°C	6.0	16		6.0	16		2.0	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4.0$ mA, T_A = 25°C		250	400			400		250	500	mV
Output Leakage Current	$V_{IN(+)} \geq 1.0$ V, $V_{IN(-)}$ = 0, V_O = 30 V, T_A = 25°C			200			200			200	nA
Input Offset Voltage	(Note 9)			9.0		9.0	15			40	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150		50	200			300	nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			400		200	500			1000	nA
Input Common-Mode Voltage Range		0		V+ −2.0	0		V+ −2.0	0		V+ −2.0	V
Saturation Voltage	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4$ mA			700		400	700			700	mV
Output Leakage Current	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, V_O = 30			1.0			1.0			1.0	μA
Differential Input Voltage	Keep all $V_{INs} \geq 0$ V (or V−, if used) (Note 8)			36			V+			V+	V

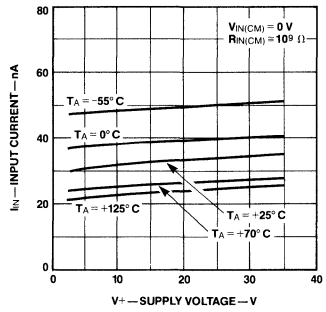
Notes on following page

Typical Performance Curves for μA139/μA239/μA339/μA139A, μA239A/μA339A/μA3302

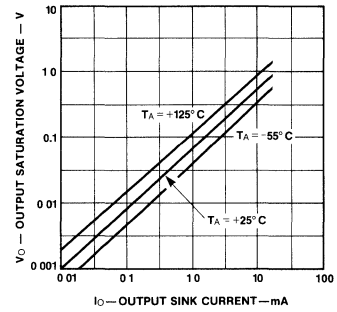
Supply Current



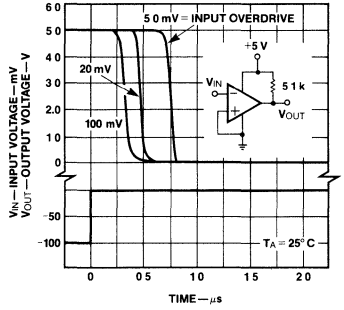
Input Current



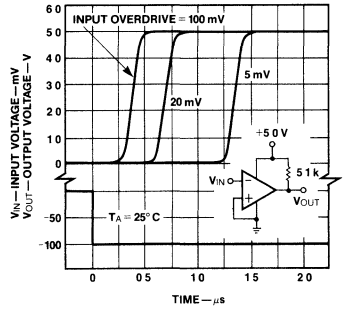
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition

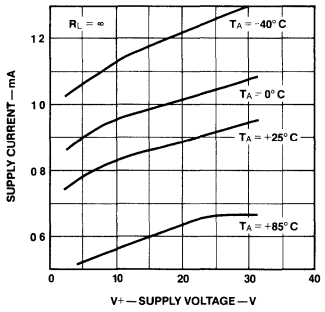


Response Time for Various Input Overdrives—Positive Transition

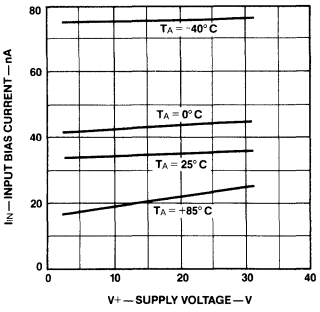


Typical Performance Curves for μA2901

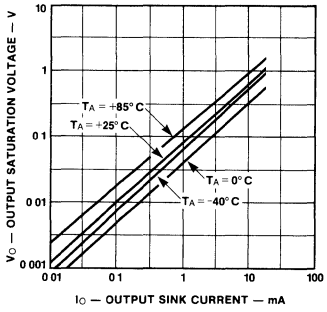
Supply Current



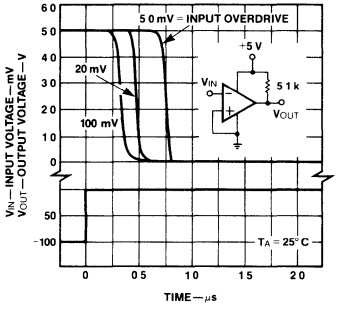
Input Current



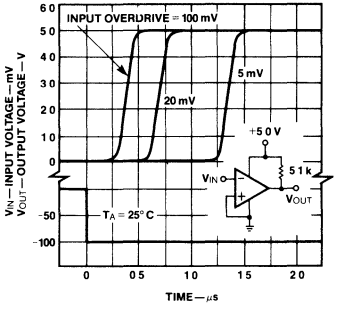
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



5

Application Information

The μA139 series are high-gain, wide-bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard pc board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input/output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the μA139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 2 V to 30 V.

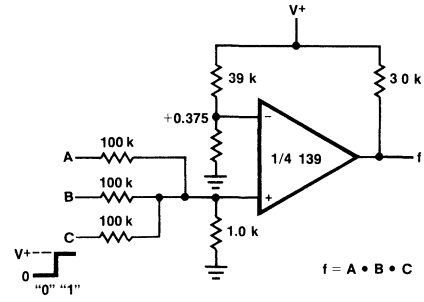
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going more negative than −0.3 V (at 25°C). An input clamp diode can be used as shown in the applications section.

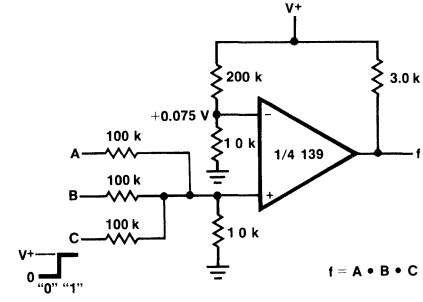
The output of the μA139 series is the uncommitted collector of a grounded-emitter npn output transistor. Many collectors can be tied together to provide wired-OR output function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the μA139 package. The output can also be used as a simple SP/ST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60 Ω saturation resistance of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications (V+ = 15 V)

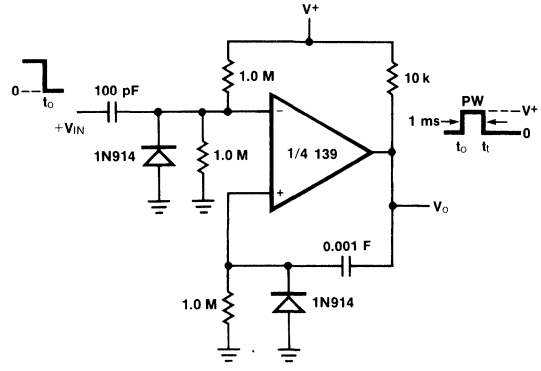
AND Gate



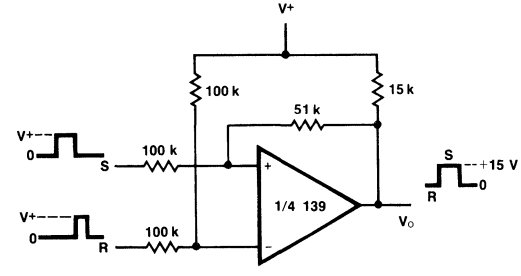
OR Gate



Monostable Multivibrator

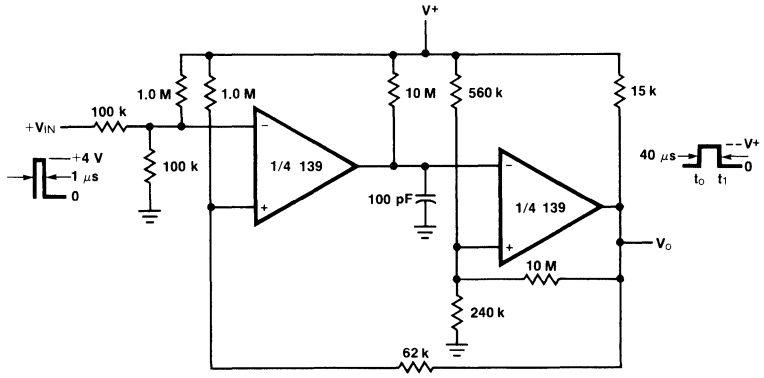


Bistable Multivibrator

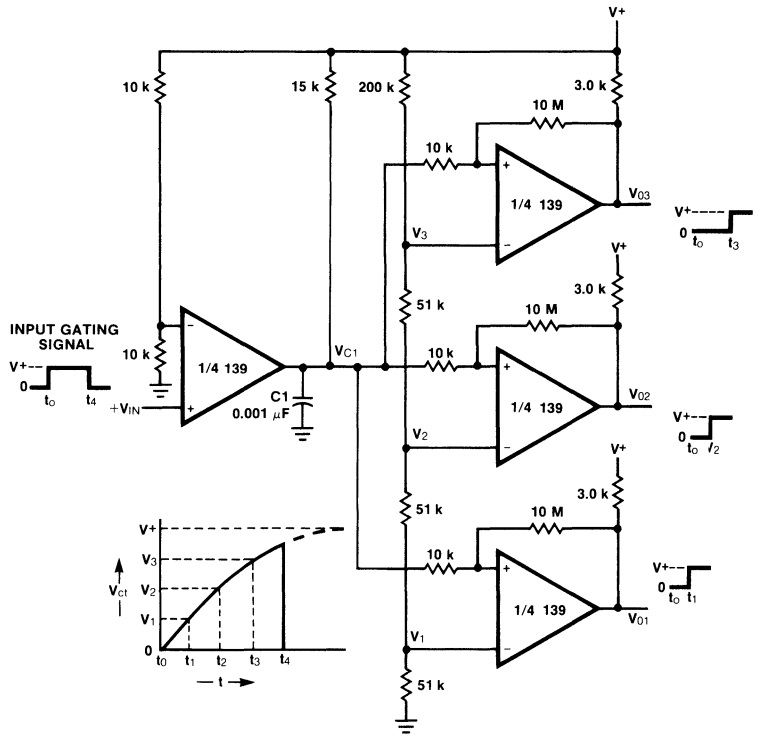


Typical Applications (V+ = 15 V) (Cont.)

Monostable Multivibrator with Input Lock-Out

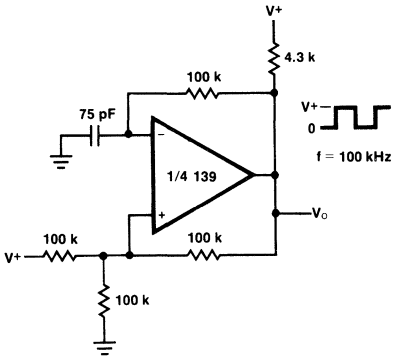


Time Delay Generator

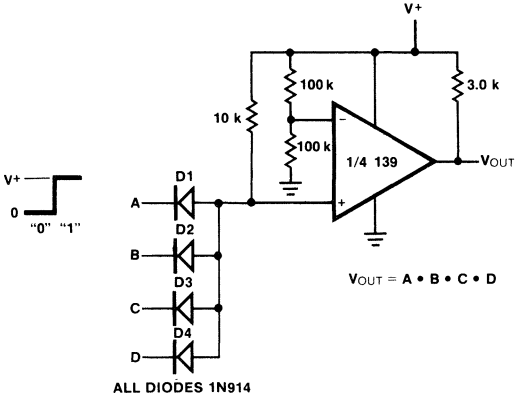


Typical Applications (V+ = 15 V) (Cont.)

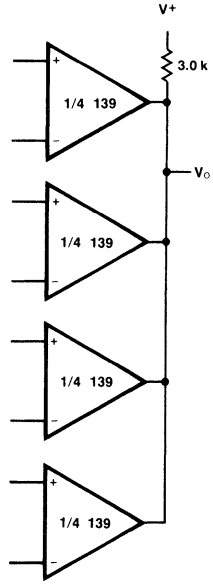
Squarewave Oscillator



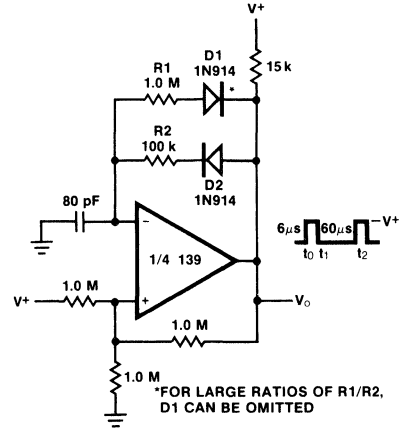
Large Fan-In AND Gate



Wired-OR Outputs



Pulse Generator



FAIRCHILD

A Schlumberger Company

μA193/293/393/2903 Low-Power, Low-Offset Dual Comparators

Linear Products

Description

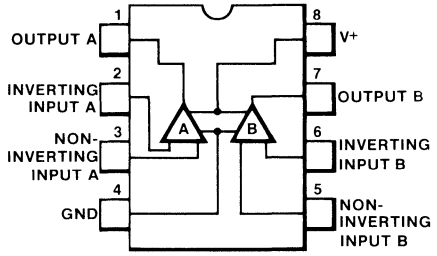
The μA193 series consists of two independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected pnp input stage allows the input common-mode voltage to include ground.

- **SINGLE SUPPLY OPERATION +2.0 V TO +36 V**
- **DUAL SUPPLY OPERATION ±1.0 V TO ±18 V**
- **ALLOW COMPARISON OF VOLTAGES NEAR GROUND POTENTIAL**
- **LOW CURRENT DRAIN 400 μA TYP**
- **COMPATIBLE WITH ALL FORMS OF LOGIC**
- **LOW INPUT BIAS CURRENT 25 nA TYP**
- **LOW INPUT OFFSET CURRENT ±5 nA TYP**
- **LOW OFFSET VOLTAGE ±2 mV**

Absolute Maximum Ratings

Supply Voltage, V+	36 V or ±18 V
Differential Input Voltage	36 V
Input Voltage Range	−0.3 V to +36 V
Power Dissipation (Note 1)	
9T, 6T	800 mW
Output Short-Circuit to GND, (Note 2)	Continuous
Input Current ($V_{IN} < -0.3$ V), (Note 3)	50 mA
Operating Temperature Range	
μA393, μA393A	0°C to +70°C
μA293, μA293A	−25°C to +85°C
μA193, μA193A	−55°C to +125°C
μA2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Hermetic DIP, Metal Package (Soldering 60 s)	300°C
Molded DIP (Soldering, 10 s)	

Connection Diagram 8-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA193A	Ceramic DIP	6T	μA193ARM
μA193	Ceramic DIP	6T	μA193RM
μA293A	Ceramic DIP	6T	μA293ARC
μA293A	Molded DIP	9T	μA293ATC
μA293	Ceramic DIP	6T	μA293RC
μA293	Molded DIP	9T	μA293TC
μA393A	Ceramic DIP	6T	μA393ARC
μA393A	Molded DIP	9T	μA393ATC
μA393	Ceramic DIP	6T	μA393RC
μA393	Molded DIP	9T	μA393TC
μA2903	Ceramic DIP	6T	μA2903RC
μA2903	Molded DIP	9T	μA2903TC

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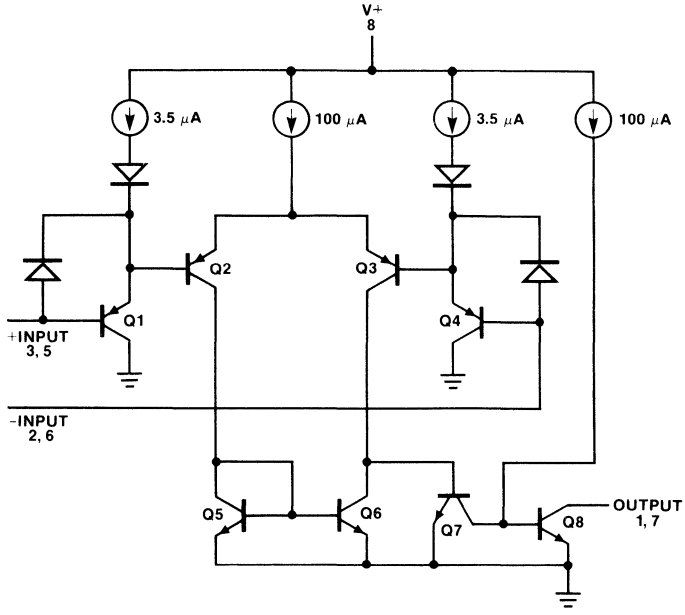
Notes

1 For operating at high temperatures, the μA393/μA393A, μA2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient The μA193 and μA193A must be derated based on a 150°C maximum junction temperature The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate

2 Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent fo the magnitude of V+.

3 This input current will exist only when the voltage at any of the input leads is driven negative It is due to the collector-base junction of the input pnp transistors becoming forward biased and thereby acting as input diode clamps. In addition to the diode action, there is also lateral npn parasitic transistor action on the IC chip This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0 3 V

Circuit Schematic (1/2 of Circuit Shown)



μA193/A, μA293A, and μA393A
Electrical Characteristics V+ = 5 V (Note 4)

Characteristic	Condition	μA193A			μA293A, μA393A			μA193			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, (Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = 25°C, (Note 5)		25	100		25	250		25	100	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		±5.0	±25		±5.0	±50		±5.0	±25	nA
Input Common-Mode Voltage Range	T_A = 25°C, (Note 6)	0		V+ −1.5	0		V+ −1.5	0		V+ −1.5	V
Supply Current	R_L = ∞ on all Comparators, T_A = 25°C R_L = ∞, V+ = 30 V, T_A = 25°C		0.4 1.0	1.0 2.5		0.4 1.0	1.0 2.5		0.4	1.0 2.5	mA
Voltage Gain	$R_L \geq 15\ k\Omega$, V+ = 15 V (To Support Large V_O Swing), T_A = 25°C	50	200		50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V, V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C		300			300			300		ns
Response Time	V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C, (Note 7)		1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, $V_O \leq 1.5$ V, T_A = 25°C	6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, $I_{sink} \leq 4.0$ mA, T_A = 25°C		250	400		250	400		250	400	mV
Output Leakage Current	$V_{IN(+)} \geq 1.0$ V, $V_{IN(-)}$ = 0, V_O = 30 V, T_A = 25°C			200			200			200	nA
Input Offset Voltage	(Note 9)			4.0			4.0			9.0	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150			±100	nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300	nA
Input Common-Mode Voltage Range		0		V+ −2.0	0		V+ −2.0	0		V+ −2.0	V
Saturation Voltage	$V_{IN(-)} \geq 1.0$ V, $V_{IN(+)}$ = 0, $I_{sink} \leq 4$ mA			700			700			700	mV
Output Leakage Current	$V_{IN(+)} \geq 1.0$ V, $V_{IN(-)}$ = 0, V_O = 30 V			1.0			1.0			1.0	μA
Differential Input Voltage	Keep all $V_{INs} \geq 0$ V (or V−, if used), (Note 8)			V+			V+			V+	V

Notes

4. These specifications apply for V+ = 5.0 V and −55°C ≤ T_A ≤ +125°C, unless otherwise stated With the μA293/μA293A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the μA393/μA393A temperature specifications are limited to 0°C ≤ T_A ≤ 70°C, and the μA2903 temperature range is −40°C ≤ T_A ≤ +85°C.
5. The direction of the input current is out of the IC due to the pnp input stage This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V The upper end of the common-mode voltage range is V+ −1 5 V, but either or both inputs can go to +30 V without damage
7. The response time specified is for a 100 mV input step with 5 mV overdrive For larger overdrive signals 300 ns can be obtained, see typical performance curves

μA293, μA393 and μA2903
Electrical Characteristics V+ = 5 V (Note 4)

Characteristic	Condition	μA293, μA393			μA2903			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, (Note 9)		±2.0	±5.0		±2.0	±7.0	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = 25°C, (Note 5)		25	250		25	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		±5.0	±50		±5.0	±50	nA
Input Common-Mode Voltage Range	T_A = 25°C, (Note 6)	0		V+ −1.5	0		V+ −1.5	V
Supply Current	$R_L = \infty$ on all Comparators, T_A = 25°C $R_L = \infty$, V+ = 30 V, T_A = 25°C		0.4 1.0	1.0 2.5		0.4 1.0	1.0 2.5	mA
Voltage Gain	$R_L \geq$ 15 kΩ, V+ = 15 V (To Support Large V_O Swing), T_A = 25°C	50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V, V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C		300			300		ns
Response Time	V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C, (Note 7)		1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq$ 1.0 V, $V_{IN(+)}$ = 0, $V_O \leq$ 1.5 V, T_A = 25°C	6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN(-)} \geq$ 1.0 V, $V_{IN(+)}$ = 0, $I_{sink} \leq$ 4.0 mA, T_A = 25°C		250	400		250	400	mV
Output Leakage Current	$V_{IN(+)} \geq$ 1.0 V, $V_{IN(-)}$ = 0, V_O = 30 V, T_A = 25°C			200			200	nA
Input Offset Voltage	(Note 9)			9.0		9.0	15	mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150		50	200	nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			400		200	500	nA
Input Common-Mode Voltage Range		0		V+ −2.0	0		V+ −2.0	V
Saturation Voltage	$V_{IN(-)} \geq$ 1.0 V, $V_{IN(+)}$ = 0, $I_{sink} \leq$ 4 mA			700		400	700	mV
Output Leakage Current	$V_{IN(+)} \geq$ 1.0 V, $V_{IN(-)}$ = 0, V_O = 30 V			1.0			1.0	μA
Differential Input Voltage	Keep all $V_{INs} \geq$ 0 V (or V−, if used), (Note 8)			V+			V+	V

Notes

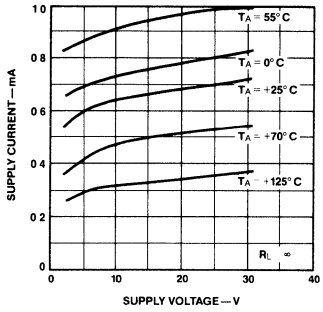
8 Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, comparator will provide a proper output state The low input voltage state must not be less than −0 3 V or 0 3 V below the magnitude of the negative power supply, if used

9. At output switch point, $V_O \cong$ 1.4 V, R_S = 0 Ω with V+ from 5 V, and over the full input common-mode range (0 V to V+ −1 5 V)

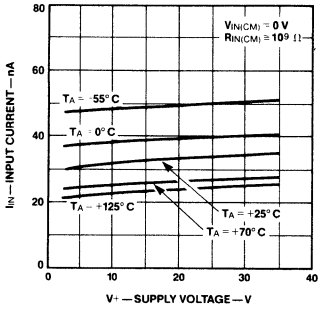
10 For input signals that exceed V_{CC}, only the overdriven comparator is affected With a 5 V supply, V_{IN} should be limited to 25 V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Typical Performance Curves for μA193/293/393

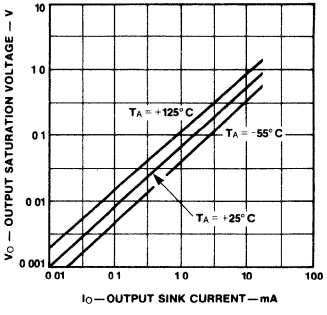
Supply Current



Input Current

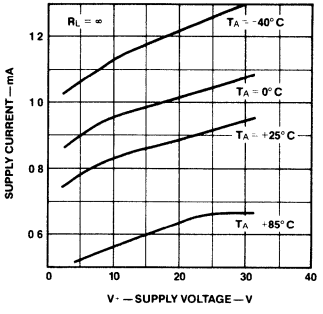


Output Saturation Voltage

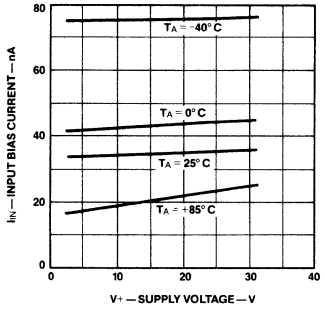


Typical Performance Curves for μA2903

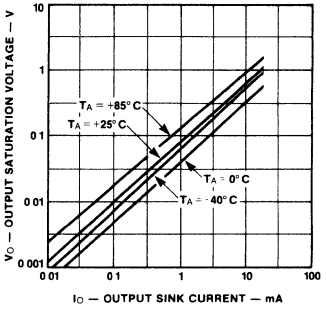
Supply Current



Input Current

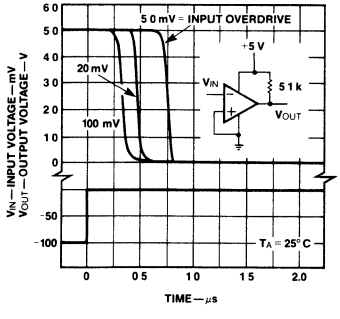


Output Saturation Voltage

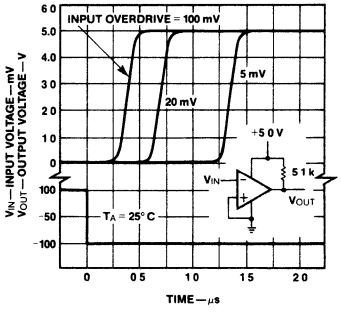


Typical Performance Curves For All Devices

Response Time for Various Input Overdrives Negative Transition



Response Time for Various Input Overdrives Positive Transition



5

Application Information

The μA193 series are high-gain, wide-bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard pc board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to less than 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required. All pins of any unused omparators should be grounded.

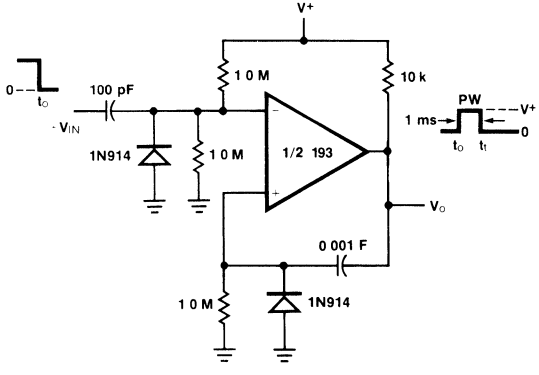
The bias network of the μA193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V to 30 V. It is unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V (at 25°C). An input clamp diode can be used as shown in the applications section.

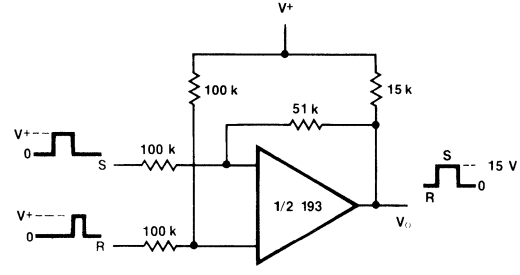
The output of the μA193 series is the uncommitted collector of a grounded-emitter npn output transistor. Many collectors can be tied together to provide an output ORing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the μA193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60 Ω saturation resistance of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications (V+ = 15 V)

One-Shot Multivibrator



Bi-Stable Multivibrator



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μA9614 Dual Differential Line Driver

Interface Products

Description

The μA9614 is a TTL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTL, with the active pull-up and the pull-down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other (See Applications). The active pull-up is short-circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary, providing NAND and AND functions of the inputs and adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both input and output to handle line transients.

- **SINGLE 5 V SUPPLY**
- **TTL COMPATIBLE INPUTS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS**
- **COMPLEMENTARY OUTPUTS FOR NAND AND OPERATION**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR APPLICATION**
- **MILITARY TEMPERATURE RANGE**

Absolute Maximum Ratings

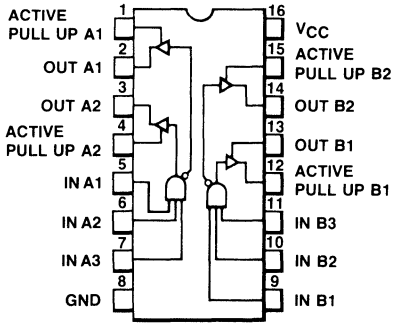
(above which the useful life may be impaired)

Storage Temperature Range	−65° C to +150° C
V_{CC} Pin Potential to Ground Pin	−0.7 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collector)	−0.5 V to +12 V
Pin Temperature	
Ceramic DIP, Flatpak (Soldering, 60 s)	300° C
Molded DIP (Soldering, 10 s)	260° C
Internal Power Dissipation (Note)	670 mW
Operating Temperature Range	
Military (μA9614)	−55° C to +125° C
Commercial (μA9614C)	0° C to +70° C

Note

For Ceramic DIP, rating applies to ambient temperatures up to 70° C, above 70° C derate linearly at 8.3 mW/° C. For the Flatpak, derate linearly at 7 1 mW/° C above 60° C.

Connection Diagram 16-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA9614	Ceramic DIP	6B	μA9614DM
μA9614C	Ceramic DIP	6B	μA9614DC
μA9614C	Molded DIP	9B	μA9614PC

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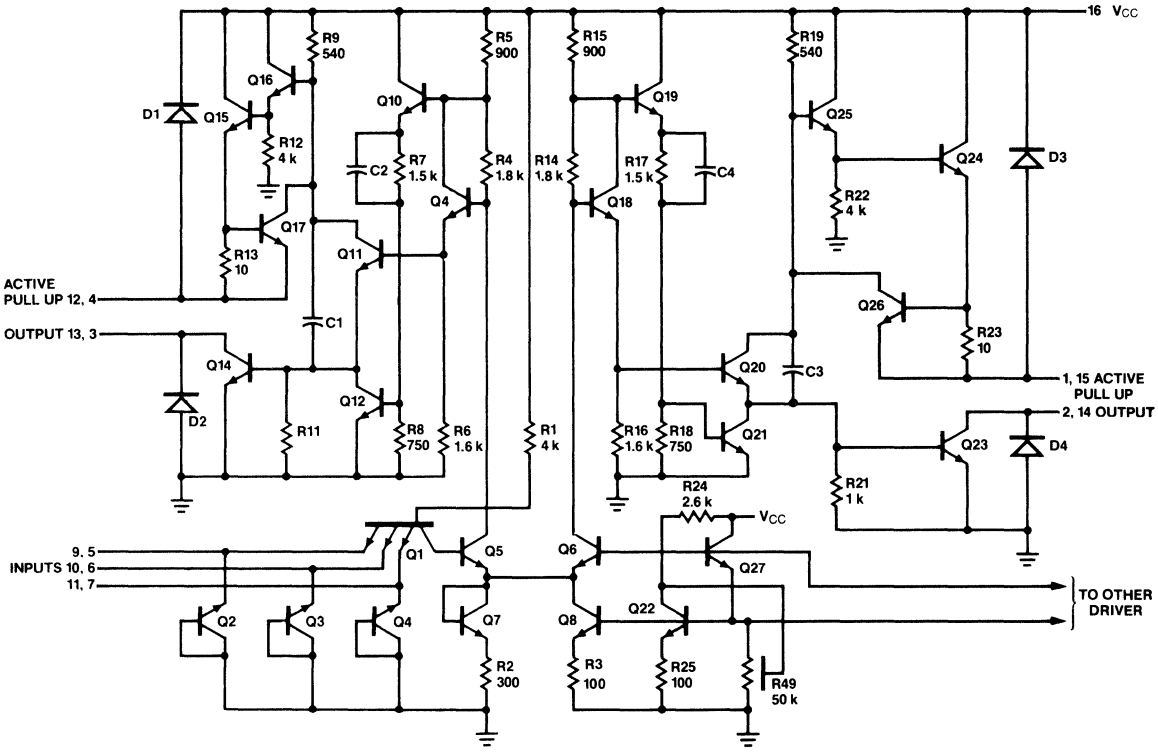
Equivalent Circuit (1/2 of circuit)



μA9614
Electrical Characteristics V_{CC} = 5.0 V ± 10%.

Symbol	Characteristic	−55°C		+25°C			+125°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
V_{OL}	Output LOW Voltage		400		200	400		400	mV	I_{OL} = 40 mA V_{CC} = 4.5 V
V_{OH1}	Output HIGH Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA, V_{CC} = 4.5 V
V_{OH2}		2.0		2.0	2.6		2.0		V	I_{OH} = −20 mA, V_{CC} = 4.5 V
I_{SC}	Output Short Circuit Current			−40	−90	−120			mA	V_{OUT} = 0.0 V V_{CC} = 5.5 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 12.0 V V_{CC} = 5.5 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.4 V V_{CC} = 5.5 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V V_{CC} = 5.5 V
V_{IL}	Input LOW Voltage		0.8		1.3	0.8		0.8	V	V_{CC} = 5.5 V
V_{IH}	Input HIGH Voltage	2.0		2.0	1.5		2.0		V	V_{CC} = 4.5 V
V_{OLC}	Clamped Output LOW Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA V_{CC} = 5.5 V
I_{CC}	Supply Current				34	50			mA	Inputs = 0 V V_{CC} = 5.5 V
I_{max}	Supply Current				46	65			mA	Inputs = 0 V V_{max} = 7.0 V
t_{PLH}	Turn-Off Time				14	20			ns	C_L = 30 pF V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	20			ns	See AC Circuit V_M = 1.5 V
V_{CD}	Input Clamp Diode Voltage				−1.0	−1.5			V	V_{CC} = 4.5 V I_{IC} = −12 mA

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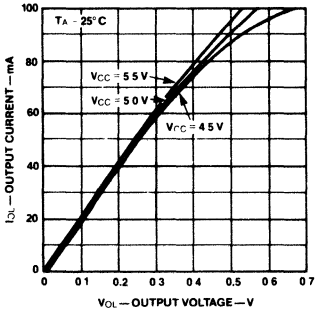
μA9614C
Electrical Characteristics V_{CC} = 5.0 V ± 5%.

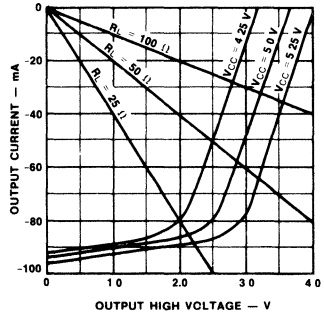
		0°C		+25°C			+75°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Condition**
V_{OL}	Output LOW Voltage		450		200	450		450	mV	I_{OL} = 40 mA V_{CC} = 4.75 V
V_{OH1}	Output HIGH Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA, V_{CC} = 4.75 V
V_{OH2}		2.0		2.0	2.6		2.0		V	I_{OH} = −40 mA, V_{CC} = 4.75 V
I_{SC}	Output Short Circuit Current			−40	−90	−120			mA	V_{OUT} = 0.0 V V_{CC} = 5.25 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 5.25 V V_{CC} = 5.25 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.45 V V_{CC} = 5.25 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V V_{CC} = 5.25 V
V_{IL}	Input LOW Voltage		0.8		1.3	0.8		0.8	V	V_{CC} = 5.25 V
V_{IH}	Input HIGH Voltage	2.0		2.0	1.5		2.0		V	V_{CC} = 4.75 V
V_{OLC}	Clamped Output LOW Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA V_{CC} = 5.25 V
I_{CC}	Supply Current				33	50			mA	Inputs = 0 V V_{CC} = 5.25
I_{max}	Supply Current				46	70			mA	Inputs = 0 V V_{max} = 7.0 V
t_{PLH}	Turn-Off Time				14	30			ns	C_L = 30 pF V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	30			ns	See AC Circuit V_M = 1.5 V
V_{CD}	Input Clamp Diode Voltage				−1.0	−1.5			V	V_{CC} = 4.75 V I_{IC} = −12 mA

Typical Performance Curves

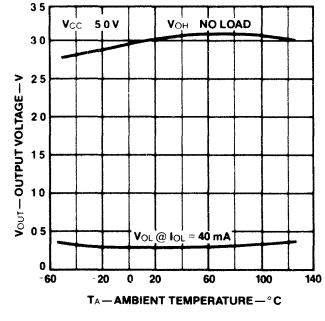
Active Pull Down Output LOW Current vs Output LOW Voltage



Active Pull-Up Output HIGH Current vs Output HIGH Voltage

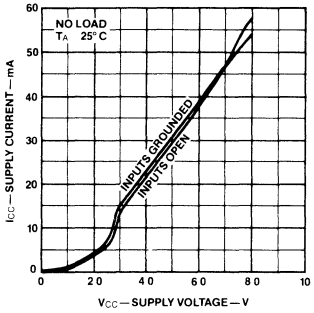


Logic Levels vs Ambient Temperature

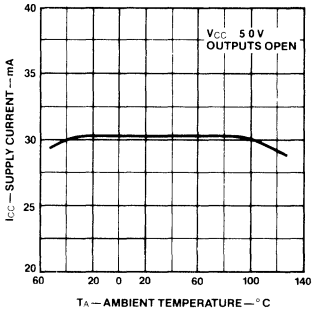


Typical Performance Curves (Cont.)

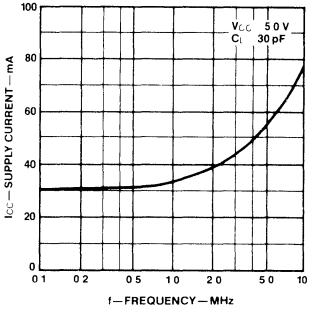
Supply Current vs Supply Voltage



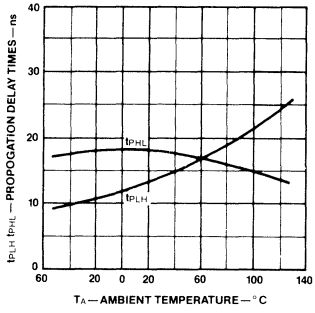
Supply Current vs Temperature



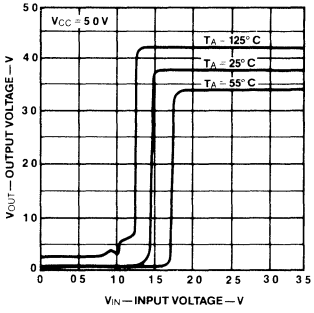
Supply Current vs Operating Frequency



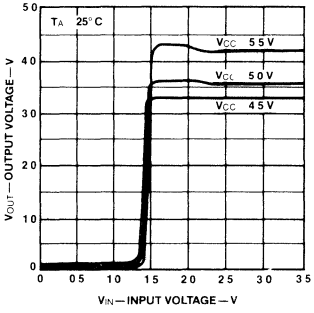
Propagation Delay Time vs Temperature



Transfer Characteristics vs Temperature



Transfer Characteristics vs Supply Voltage



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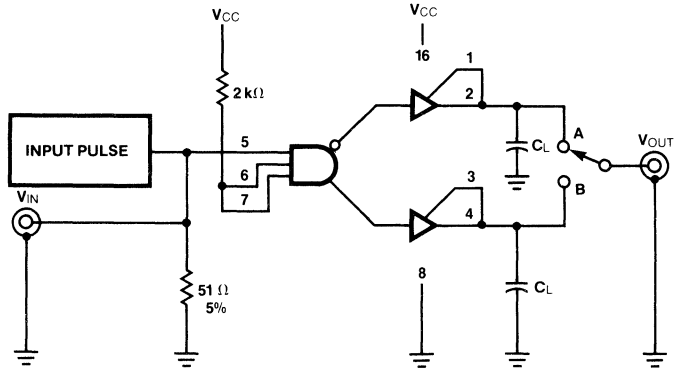
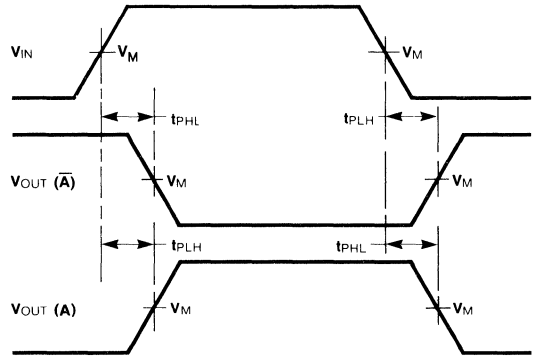
AC Test Circuit and Waveforms

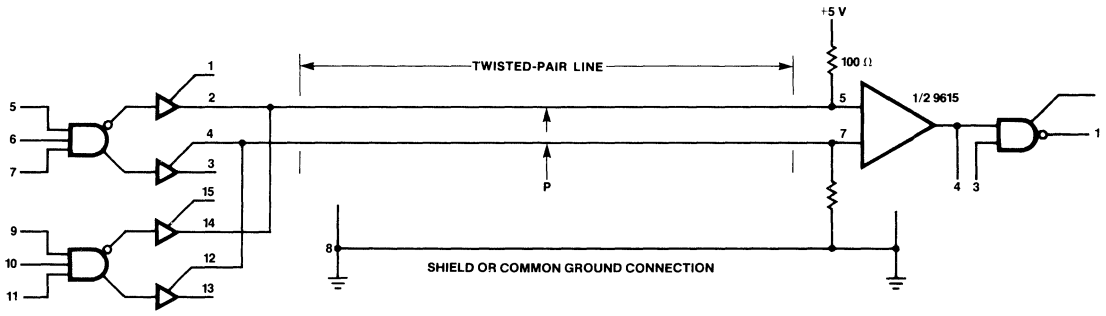




Input Pulse
Frequency = 500 kHz
Amplitude = 3.0 ±0 1 V
Pulse Width = 110 ± 10 ns
$t_r = t_f \leq 5.0$ ns

Typical Applications

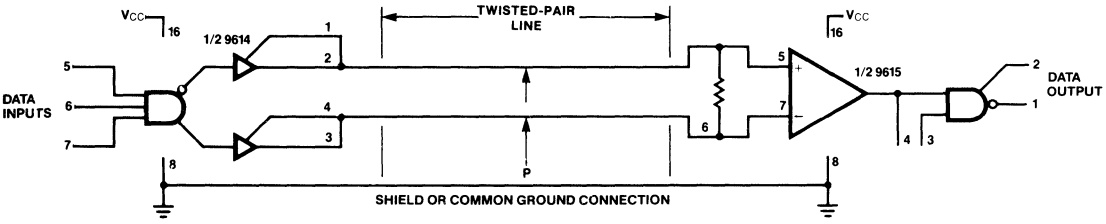
Differential Mode Expansion Multiplex Operation



Only one driver is enabled at one time

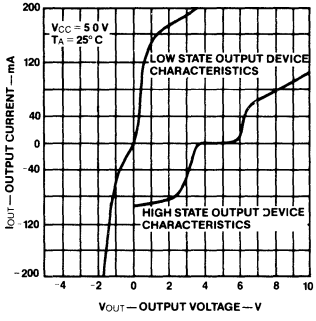
Expand by tying NAND active pull-down outputs together and by tying AND active pull-up outputs together. The drivers can be inhibited by taking one input to ground

Simplex — Differential Operation



See μA9615 data sheet for operation of μA9615

Typical Reflection Diagram



See μ9621 data sheet for usage of reflection diagram

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μA9615
Dual Differential Line Receiver

Interface Products

Description

The 9615 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 V supply. It can receive differential data in the presence of high level (± 15 V) common mode voltages and deliver undisturbed TTL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe and a 130 Ω terminating resistor are provided at the inputs. The output has an uncommitted collector with an active pull-up available on an adjacent pin to allow either wire-OR or active pull-up TTL output configuration.

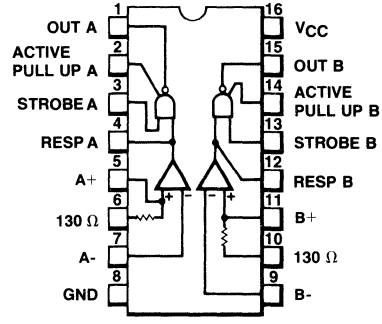
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **CHOICE OF AN UNCOMMITTED COLLECTOR OR ACTIVE PULL-UP**
- **STROBE**
- **FULL MILITARY TEMPERATURE RANGE**
- **SINGLE 5 V SUPPLY VOLTAGES**
- **FREQUENCY RESPONSE CONTROL**
- **130 Ω TERMINATING RESISTOR**

Absolute Maximum Ratings above which the useful life may be impaired	
Storage Temperature	−65°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Pins 5, 6, 7, 9, 10,11)	±20 V
Voltage Applied to Outputs for HIGH output State without Active Pull-Up	−0.5 V to +13.2 V
Voltage Applied to Strobe	−0.5 V to +5.5 V
Pin Temperature Range	
Ceramic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note)	670 mW
Operating Temperature Range	
Military (9615)	−55°C to +125°C
Commercial (9615C)	0°C to +70°C

Note

For Ceramic DIP, rating applies to ambient temperatures up to 70°C; above 70°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 60°C.

Connection Diagram
16-Pin DIP

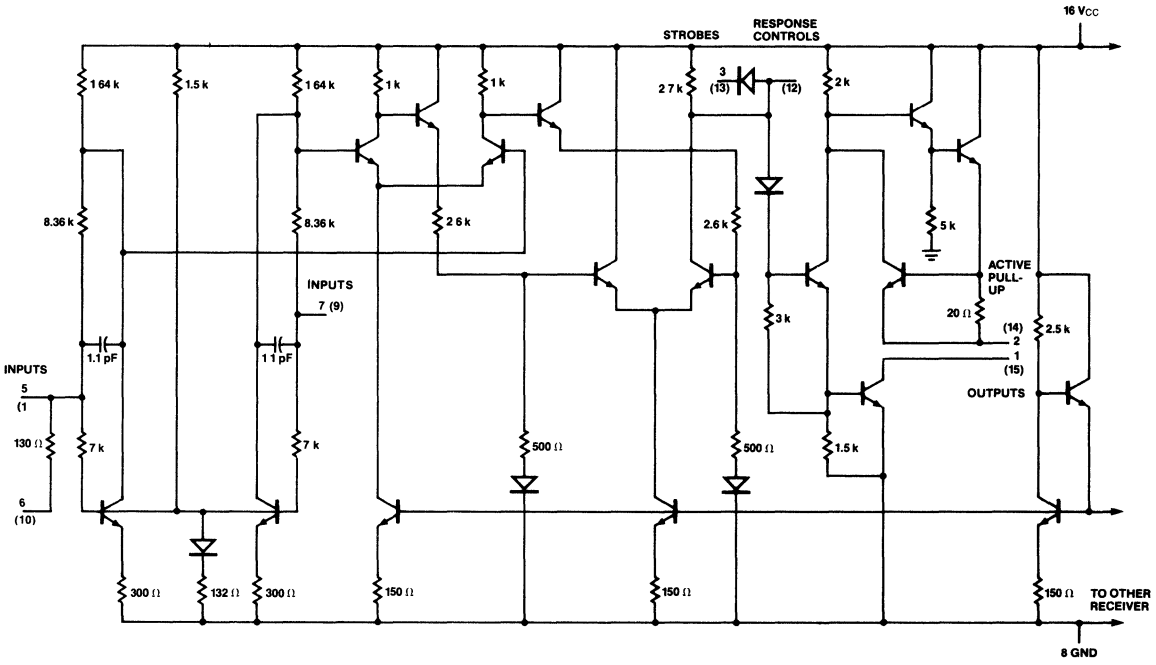


(Top View)

Order Information

Type	Package	Code	Part No.
μA9615	Ceramic DIP	6B	μA9615DM
μA9615C	Ceramic DIP	6B	μA9615DC
μA9615C	Molded DIP	9B	μA9615PC

Equivalent Circuit (½ μA9615)



μA9615
Electrical Characteristics V_{CC} = 5.0 V ± 10%.

Symbol	Characteristic	T = −55°C		T = 25°C			T = +125°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
V_{OL}	Output LOW Voltage		0.40		0.18	0.40		0.40	V	V_{CC} = 4.5 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output HIGH Voltage	2.2		2.4	3.2		2.4		V	V_{CC} = 4.5 V, V_{OUT} = ** I_{OH} = −5.0 mA, *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 12 V, *V_{DIFF} = V_{CC} V_{CC} = 4.5 V
I_{SC}	Output Shorted Current			−15	−39	−80			mA	V_{CC} = 5.5 V, **V_{SC} = 0 V, *V_{DIFF} = −0.5 V
I_{IN}	Input Current		−0.9		−0.49	−0.7		−0.7	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V Other Input = 5.5 V
$I_{IN(ST)}$	Strobe Input Current				−1.15	−2.4			mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			−1.2	−3.4				mA	V_{CC} = 5.5 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	−15	+15	−15	±17.5	+15	−15	+15	V	V_{CC} = 5.0 V, *V_{DIFF} = 1.0 V
$I_{R(ST)}$	Strobe Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V, *V_{DIFF} = −0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			77	130	167			Ω	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = GND
V_{TH}***	Differential Input Threshold Voltage	−500	500	−500	80	500	−500	500	mV	V_{CM} = 0 V V_{CC} = 5.0 V ±10%
		−1.0	1.0	−1.0		+1.0	−1.0	1.0	V	−15 ≤ V_{CM} V_{CM} ≤ +15 V V_{CC} = 5.0 V ±10%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.5 V, −Inputs = 0 V, +Inputs = 0.5 V
t_{PLH}	Turn-Off Time				30	50			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, *Figure 1*
t_{PHL}	Turn-On Time				30	50			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, *Figure 1*

Notes

*V_{DIFF} is a differential input voltage referred from "+IN A" to "−IN A" and from "+IN B" to "−IN B".

**Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up "B".

***See input-output transfer characteristic graphs on following pages.

μA9615C
Electrical Characteristics V_{CC} = 5.0 V ± 5%.

Symbol	Characteristic	T = 0°C		T = 25°C			T = 70°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
V_{OL}	Output LOW Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75 V, V_{OUT} = **, I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4		V	V_{CC} = 4.75 V, V_{OUT} = **, I_{OH} = −5.0 mA, *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 5.25 V, *V_{DIFF} = V_{CC}, V_{CC} = 4.75 V
I_{SC}	Output Shorted Current			−14		−100			mA	V_{CC} = 5.25 V, **V_{SC} = 0 V, *V_{DIFF} = −0.5 V
I_{IN}	Input Current		−0.9		−0.49	−0.7		−0.7	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V; Other Input = 5.25 V
$I_{IN(ST)}$	Strobe Input Current				−1.15	−2.4			mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V, *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			−1.2	−3.4				mA	V_{CC} = 5.25 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	−15	+15	−15	± 17.5	+15	−15	+15	V	V_{CC} = 5.0 V, *V_{DIFF} = 1.0 V
$I_{R(ST)}$	Strobe Input Leakage Current					5.0		10	μA	V_{CC} = 4.75 V, *V_{DIFF} = −0.5 V, V_R = 4.5 V
R_{IN}	Input Resistor			74	130	179			Ω	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = GND
V_{TH}***	Differential Input Threshold Voltage	−500	500	−500	80	500	−500	500	mV	V_{CM} = 0 V, V_{CC} = 5.0 V ±5%
		−1.0	1.0	−1.0		1.0	−1.0	1.0	V	−15 ≤ V_{CM} ≤ +15 V, V_{CC} = 5.0 V ±5%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.25 V, +Inputs = 0.5 V, −Inputs = 0 V
t_{PLH}	Turn-Off Time				30	75			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, *Figure 1*
t_{PHL}	Turn-On Time				30	75			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, *Figure 1*

Notes

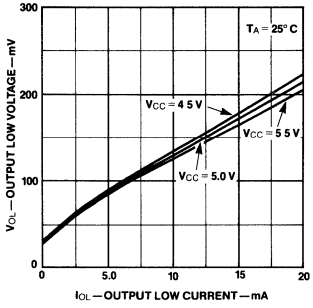
*V_{DIFF} is a differential input voltage referred from "+IN A" to "−IN A" and from "+IN B" to "−IN B".

**Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up "B".

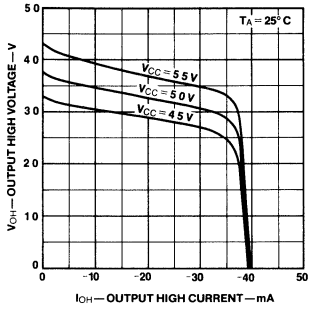
***See input-output transfer characteristic graphs on following pages.

Typical Performance Curves for μA9615 and μA9615C

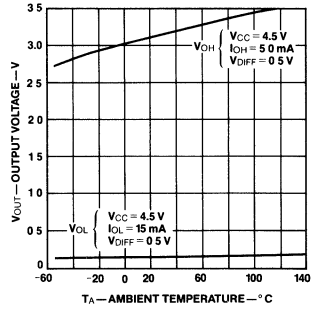
Output LOW Voltage as a Function of Output LOW Current



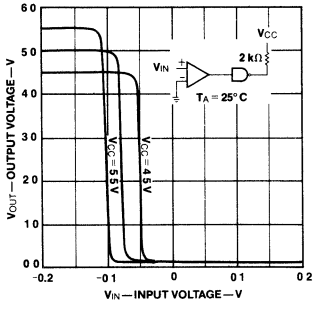
Output HIGH Voltage as a Function of Output HIGH Current



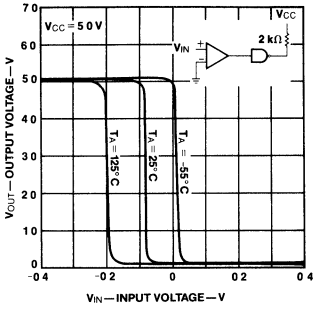
Output HIGH Voltage as a Function of Ambient Temperature



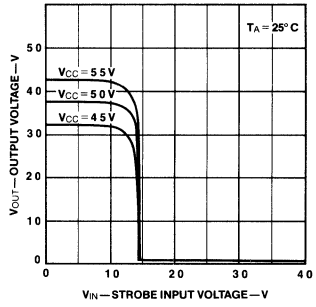
Input/Output Transfer Characteristics as a Function of V_{CC}



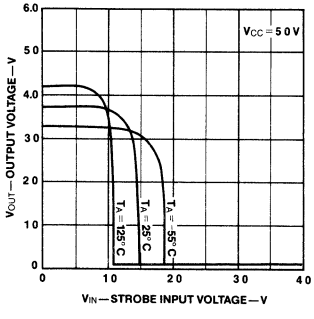
Input/Output Transfer Characteristics as a Function of Temperature



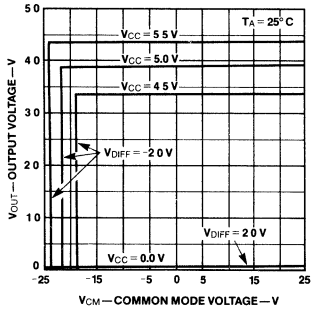
Strobe Input/Output Transfer Characteristic as a Function of V_{CC}



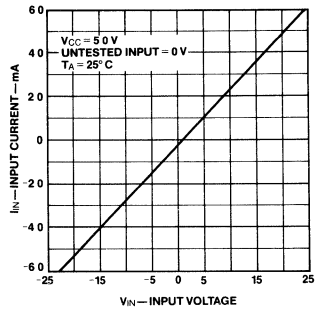
Strobe Input/Output Transfer Characteristic as a Function Of Ambient Temperature



Output Voltage as a Function of Common Mode Voltage

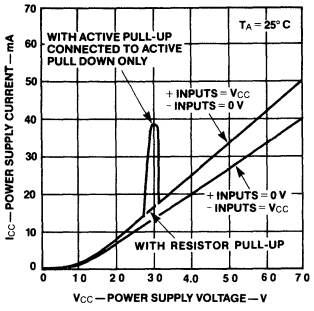


Input Current as a Function of Input Voltage

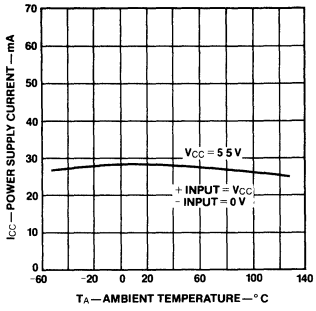


Typical Performance Curves for μA9615 and μA9615C (Cont.)

Power Supply Current as a Function of Power Supply Voltage



Power Supply Current as a Function of Ambient Temperature



Switching Time as a Function of Ambient Temperature

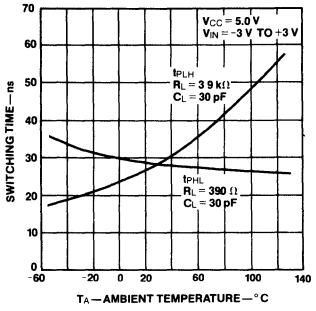
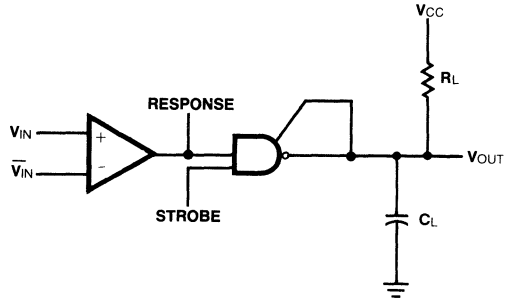
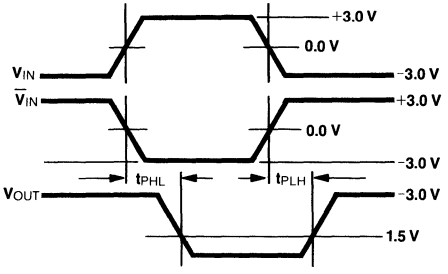


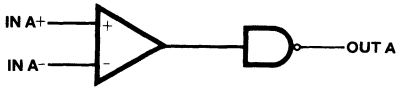
Fig. 1 Switching Time Test Circuit and Waveforms

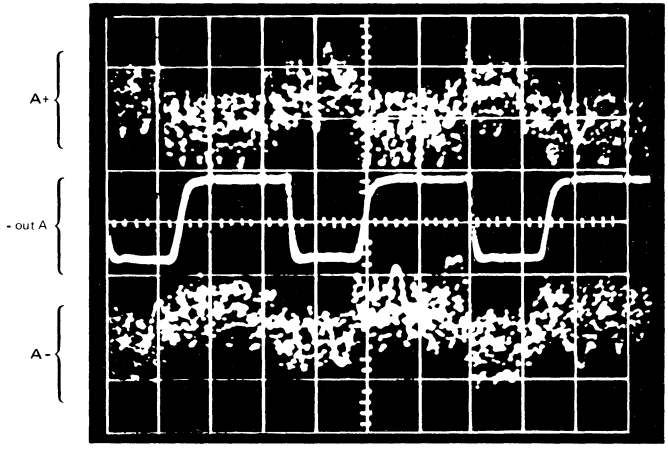




(*USE V_{IN} OR $\overline{V_{IN}}$ GROUND OTHER INPUT)
STROBE AND RESPONSE ARE LEFT OPEN

Fig. 2





VERTICAL = 2.0 V/DIV. HORIZONTAL = 50 ns/DIV.

Photograph of a 9615 switching differential data in the presence of high common mode noise.

Typical Applications

Fig. 3 Standard Usage

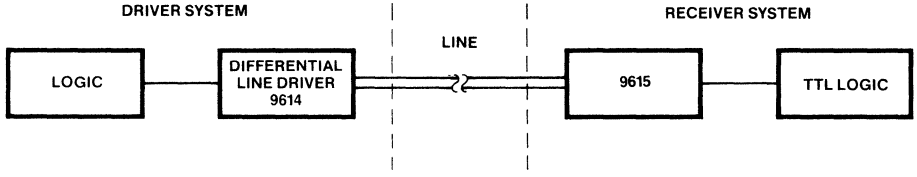
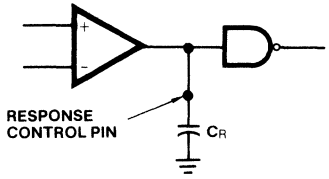


Fig. 4 Frequency Response Control

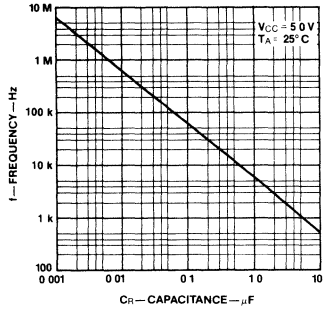


Notes

$C_R > .01\ \mu F$ may cause slowing of rise and fall times of the output

Due to the mechanism of induction of differential noise, the use of the response control is not normally needed

Frequency Response as a Function of Capacitance



FAIRCHILD
A Schlumberger Company

μA9616
Triple EIA RS-232-C/ MIL-STD-188C Line Driver

Interface Products

Description

The 9616 is a Triple Line Driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24 and/or MIL-STD-188C (by the appropriate device selection). Each driver converts TTL/DTL logic levels to EIA/CCITT and/or MIL-STD-188C logic levels for transmission between data terminal equipment and data communications equipment. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short-circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH on the inhibit terminal interrupts signal transfer and forces the output to a V_{OL} (EIA/CCITT MARK) state.

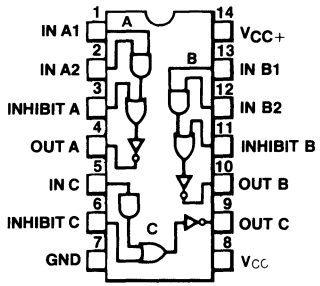
For the complementary function, see the 9617 Triple EIA RS-232-C Line Receiver and the 9627 Dual EIA RS-232-C and MIL-STD-188C Line Receiver.

- **INTERNAL SLEW RATE LIMITING**
- **MEETS EIA RS-232-C AND CCITT V.24 AND/OR MIL-STD-188C**
- **LOGIC TRUE INHIBIT FUNCTION**
- **OUTPUT SHORT-CIRCUIT CURRENT LIMITING**
- **OUTPUT VOLTAGE LEVELS INDEPENDENT OF SUPPLY VOLTAGES**

Absolute Maximum Ratings

Supply Voltage	± 15 V
Input or Inhibit Voltage	−1.5 V to +6.0 V
Output Signal Voltage	± 15 V
Internal Power Dissipation (Note 1)	670 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
RS-232 MIL-STD-188 (9616)	−55°C to +125°C
RS-232 (9616C)	0°C to 70°C
RS-232 MIL-STD-188 (9616E)	0°C to 70°C
Pin Temperatures	
Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Connection Diagram
14-Pin



(Top View)

Order Information

Type	Package	Code	Part No.
μA9616	Ceramic DIP	6A	μA9616DM
μA9616C	Ceramic DIP	6A	μA9616DC
μA9616E	Ceramic DIP	6A	μA9616EDC
μA9616C	Molded DIP	9A	μA9616PC
μA9616E	Molded DIP	9A	μA9616EPC

Truth Table Sections A and B

Input		Inhibit	Output
1	2		
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	L
X	X	H	L

Truth Table Section C

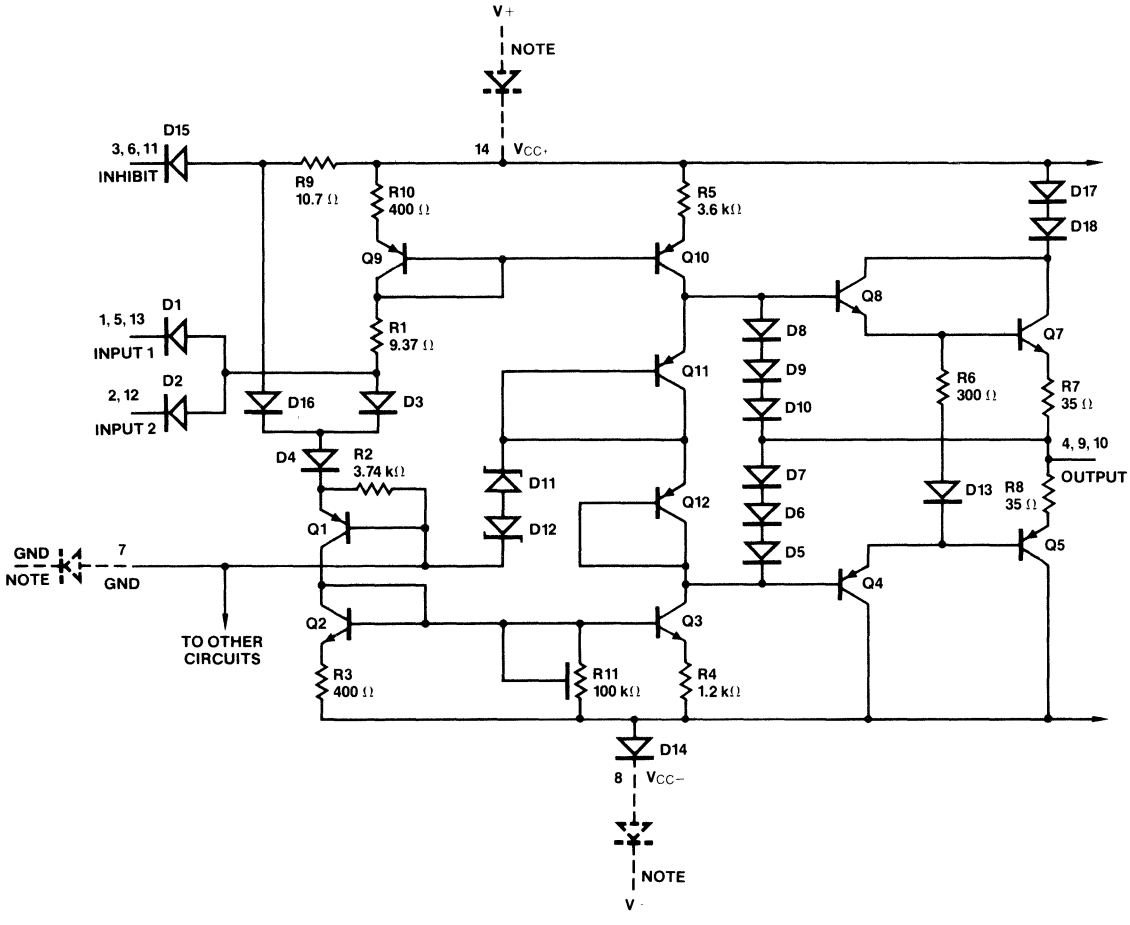
Input	Inhibit	Output
L	L	H
H	L	L
L	H	L
H	H	L

X = Output not dependent on input

Note

1. For Ceramic and Molded DIP above 60°C derate linearly at 8.3 mW/°C.

Equivalent Circuit (One of three channels)



Note

Three external diodes in series with V_{CC+}, V_{CC-} and GND are required to meet the ±2.0 V requirement

μA9616 AND μA9616E, RS-232-C and MIL-STD-188C
DC Characteristics $V_{CC} = \pm 12\ V \pm 10\%$; $R_L \geq 3\ k\Omega$. See Test Circuit, unless otherwise specified. (Note 2)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8\ V$	5.0	6.0	7.0	V
V_{OL}	Output LOW Voltage	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\ V$	−7.0	−6.0	−5.0	V
	Ripple Rejection	Power Supply Ripple = 2.4 Vp-p, f = 400 Hz		0.25		% of V_{OUT}
V_{OH} to V_{OL}	Output HIGH Voltage to Output LOW Voltage Magnitude Matching Error				±10	%
I_{SC+}	Positive Output Short Circuit Current	$R_L = 0\ \Omega$, V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8\ V$	−45	−25	−12	mA
I_{SC-}	Negative Output Short Circuit Current	$R_L = 0\ \Omega$, $V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\ V$	+12	+25	+45	mA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	$V_{IN1} = V_{IN2} = 2.4\ V$			40	μA
		$V_{IN1} = V_{IN2} = 5.5\ V$			1.0	mA
I_{IL}	Input LOW Current	$V_{IN1} = V_{IN2} = 0.4\ V$	−1.6	−1.2		mA
I_+	Positive Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8\ V$		15	25	mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\ V$		7.5	15	
I_-	Negative Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8\ V$	−1.0	0		mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\ V$	−25	−15		
R_{OUT}	Output Resistance, Power On	$R_L = 6\ k\Omega$, $\Delta I_L = 10\ mA$		75		Ω
R_{OUT}	Output Resistance, Power Off	$-2.0\ V \leq V_{OUT} \leq +2.0\ V$ (Notes 4 and 5)	300			Ω

μA9616 AND μA9616E, RS-232-C and MIL-STD-188C
AC Characteristics $0 \leq T_A \leq 70°C$, (Notes 2 and 3)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
	Positive Slew Rate	$0\ pF \leq C_L \leq 2500\ pF$, $R_L \geq 3\ k\Omega$	4.0	15	30	V/μs
	Negative Slew Rate	$0\ pF \leq C_L \leq 2500\ pF$, $R_L \geq 3\ k\Omega$	−30	−15	−4.0	V/μs
t_{PLH}	Propagation Delay Time	No Load		740		ns
t_{PHL}	Propagation Delay Time	No Load		740		ns

Notes
2. The operating temperature range for the 9616 is −55°C to +125°C and 9616E is 0°C to +70°C.
3. An external capacitor may be needed to meet signal wave shaping requirements of MIL-STD-188C at the applicable modulation rate. No external capacitor is needed to meet RS-232-C over the operating temperature range of 0°C to +70°C.
4. All input and supply pins grounded.
5. Three external diodes in series with V_{CC+}, V_{CC-} and GND are required to meet the ±2.0 V requirement

9616C, EIA RS-232-C
DC Characteristics $V_{CC} = \pm 12\ V \pm 10\%$, over operating temperature range. See Test Circuit, $R_L = 3\ k\Omega$, unless otherwise specified.

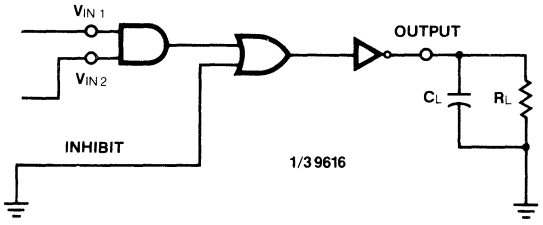
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8\ V$	5.0	6.0	7.5	V
V_{OL}	Output LOW Voltage	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\ V$	−7.5	−6.0	−5.0	V
I_{SC+}	Positive Output Short-Circuit Current	$R_L = 0\ \Omega$, V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8\ V$		−25		mA
I_{SC-}	Negative Output Short-Circuit Current	$R_L = 0\ \Omega$, $V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\ V$		25		mA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	$V_{IN1} = V_{IN2} = 2.4\ V$			40	μA
		$V_{IN1} = V_{IN2} = 5.5\ V$			1.0	mA
I_{IL}	Input LOW Current	$V_{IN1} = V_{IN2} = 0.4\ V$	−1.6	−1.2		mA
I_+	Positive Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8\ V$		15	22	mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\ V$		7.5	13	
I_-	Negative Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8\ V$	−1.0	0		mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0\ V$	−22	−15		
R_{OUT}	Output Resistance, Power Off	$-2.0\ V \leq V_{OUT} \leq +2.0\ V$ (Notes 4 and 5)	300			Ω

9616C, EIA RS-232-C
AC Characteristics $0 \leq T_A \leq 70°C$, (Note 6)

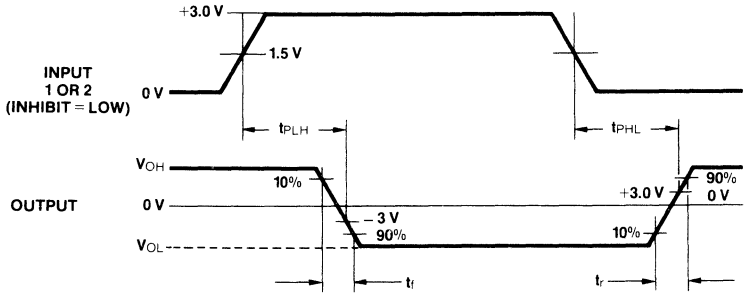
Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
	Positive Slew Rate	$0\ pF \leq C_L \leq 2500\ pF$, $R_L \geq 3\ k\Omega$	4.0	15	30	V/μs
	Negative Slew Rate	$0\ pF \leq C_L \leq 2500\ pF$, $R_L \geq 3\ k\Omega$	−30	−15	−4.0	V/μs
t_{PLH}	Propagation Delay Time	No Load		740		ns
t_{PHL}	Propagation Delay Time	No Load		740		ns

Notes
4 All input and supply pins grounded.
5 Three external diodes in series with V_{CC+}, V_{CC-} and GND are required to meet the ±2.0 V requirement
6 The operating temperature range for the 9616 is −55°C to +125°C and 9616E is 0°C to +70°C.

AC Test Circuit



Voltage Waveforms



Note

Omit V_{IN2} for channel "C".

Input: Frequency = 50 kHz
Pulse Width = 20 μs
t_r and t_f = 10 ± 5 ns

6

FAIRCHILD

A Schlumberger Company

μA9627 • μA9627C RS-232C/MIL-STD-188C Dual Line Receivers

Interface Products

Description

The 9627 is a Dual Line Receiver which meets the electrical interface specifications of EIA RS-232C and MIL-STD-188C. The input circuitry accommodates ±25 V input signals and the differential inputs allow user selection of either inverting or non-inverting logic for the receiver operation. The 9627 provides both a selectable hysteresis range and selectable receiver input resistance. When pin 1 is tied to V_{CC}, the typical switching points are at +2.6 V and −2.6 V, thus meeting RS-232-C requirements. When pin 1 is open, the typical switching points are at +50 μA and −50 μA, thus satisfying the requirements to MIL-STD-188C LOW level interface. Connecting the R_{IN} pin to the (−) input yields an input impedance in the range of 3 kΩ to 7 kΩ and satisfies RS-232-C requirements; leaving R_{IN} unconnected, the input resistance will be greater than 6 kΩ to satisfy MIL-STD-188C.

The output circuitry is TTL/DTL compatible and will allow "collector-dotting" to generate the wire-OR function. A TTL/DTL strobe is also provided for each receiver. The EIA failsafe mode of operation is shown in the application section of this data sheet.

- **EIA RS-232-C INPUT STANDARDS**
- **MIL-STD-188C INPUT STANDARDS**
- **VARIABLE HYSTERESIS CONTROL**
- **HIGH COMMON-MODE REJECTION**
- **R_{IN} CONTROL (5 kΩ OR 10 kΩ)**
- **WIRED-OR CAPABILITY**
- **CHOICE OF INVERTING AND NON-INVERTING INPUTS**
- **OUTPUTS AND STROBE TTL COMPATIBLE**

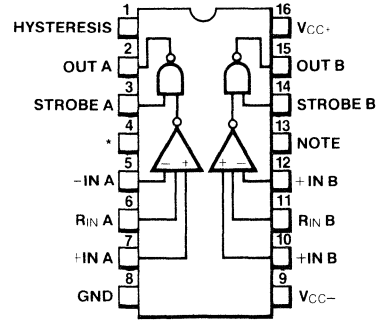
Absolute Maximum Ratings

V_{CC+} to Ground	0 V to +15 V
V_{CC-} to Ground	0 V to −15 V
Input Voltage Referred to Ground Pin	±25 V
Strobe to Ground Voltage	−0.5 V to +5.5 V
Maximum Applied Output Voltage	−0.5 V to +15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (9627)	−55°C to +125°C
Commercial (9627C)	0°C to +70°C
Internal Power Dissipation (Note 1)	730 mW
Pin Temperature	
Ceramic DIP, (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Notes

1. Above 65°C ambient temperature, derate linearly at 8.3 mW/°C

Connection Diagram
16-Pin DIP



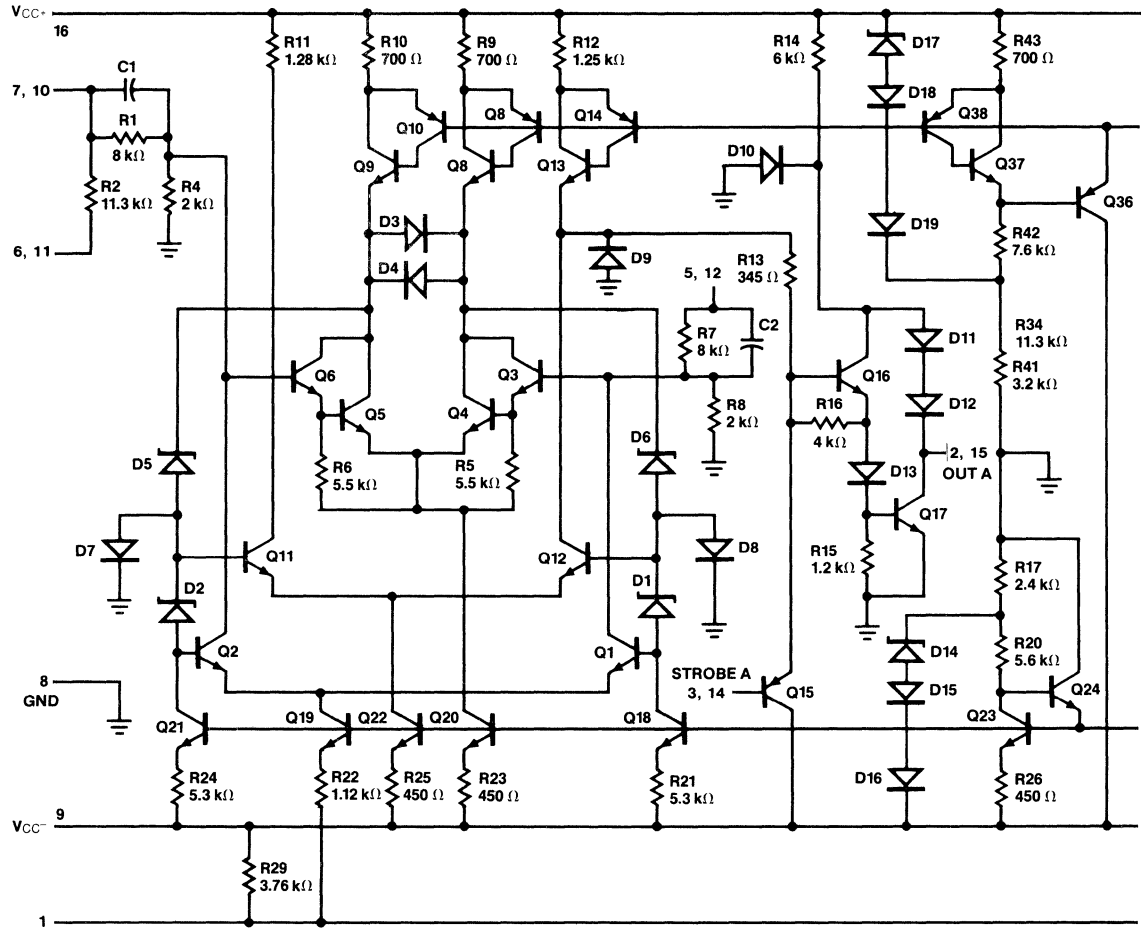
(Top View)

*Internal Connection—
make no connection to this pin.

Order Information

Type	Package	Code	Part No.
μA9627	Ceramic DIP	6B	μA9627DM
μA9627C	Ceramic DIP	6B	μA9627DC
μA9627C	Molded DIP	9B	μA9627PC

Equivalent Circuit (1/2 of circuit shown)



$C_1 = C_2 = C_3 = C_4 = 1\ 1$ pF
Pin 4 and 13 = Internal connection

μA9627
DC Characteristics V_{CC+} = 12 V ± 10%, V_{CC-} = −12 V ± 10% over Operating Temperature Range, unless otherwise specified.

MIL • STD • 188C

Symbol	Characteristic	Condition (Pins 6 and 11 Open, Inverting Inputs Open, Pin 1 Open)		Min	Typ	Max	Unit
V_{OL}	Output LOW Voltage	V_{CC+} = +10.8 V, V_{CC-} = −13.2 V Non-Inverting Input = −0.6 V, I_{OL} = 6.4 mA				0.4	V
V_{OH}	Output HIGH Voltage	V_{CC+} = +10.8 V, V_{CC-} = −13.2 V Non-Inverting Input = +0.6 V, I_{OH} = −0.5 mA		2.4			V
I_{SC}	Output Shorted Current	V_{CC+} = +13.2 V, V_{CC-} = −10.8 V Non-Inverting Input = +0.6 V Outputs Grounded				3.0	mA
I_{IH} (Strobe)	Input HIGH Current (Strobe)	V_{CC+} = +10.8 V, V_{CC-} = −13.2 V Non-Inverting Input = +0.6 V	V_S = 2.4 V			40	μA
			V_S = 5.5 V			1.0	mA
R_{IN}	Input Resistance	V_{CC+} = +13.2 V, V_{CC-} = −13.2 V Non-Inverting Input = +3.0 V or −3.0 V		6.0			kΩ
I_{TH+}	Positive Threshold Current	V_{OUT} = 2.4 V				100	μA
I_{TH-}	Negative Threshold Current	V_{OUT} = 0.4 V		−100			μA
V_{IL} (Strobe)	Input LOW Voltage (Strobe)	$V_{Non\text{-}Inverting\ Input}$ = −0.6 V				0.8	V
V_{IH} (Strobe)	Input HIGH Voltage (Strobe)	$V_{Non\text{-}Inverting\ Input}$ = +0.6 V V_{CC+} = +13.2 V, V_{CC-} = −10.8 V		2.0			V
I_+	Positive Supply Current	$V_{Non\text{-}Inverting\ Input}$ = −0.6 V				18	mA
			T_A = +125°C (9627)			12.4	
I_-	Negative Supply Current	$V_{Non\text{-}Inverting\ Input}$ = +0.6 V		−16			mA
			T_A = +125°C (9627)	−11.4			

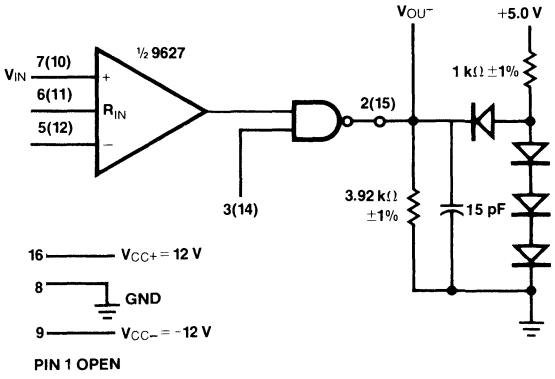
RS-232C

Symbol	Characteristic	Condition (Non-Inverting Inputs Connected to Ground, R_{IN} Inputs Connected to Inverting Inputs, Pin 1 Connected to V_{CC-})	Min	Typ	Max	Unit
R_{IN}	Input Resistance	V_{IN} = +3.0 V to +25 V	3.0		7.0	kΩ
		V_{IN} = −3.0 V to −25 V	3.0		7.0	kΩ
V_{IN}	Input Voltage	Open Circuit	−2.0		2.0	V
V_{TH+}	Positive Threshold Voltage				+3.0	V
V_{TH-}	Negative Threshold Voltage		−3.0			V

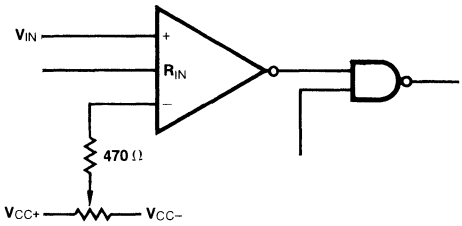
AC Characteristics T_A = +25°C, V_{CC+} = +12 V, V_{CC-} = −12 V, MIL-STD-188C • RS-232C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time	See AC Test Circuit		60	250	ns
t_{PHL}	Propagation Delay Time	See AC Test Circuit		84	250	ns

AC Test Circuit and Waveforms

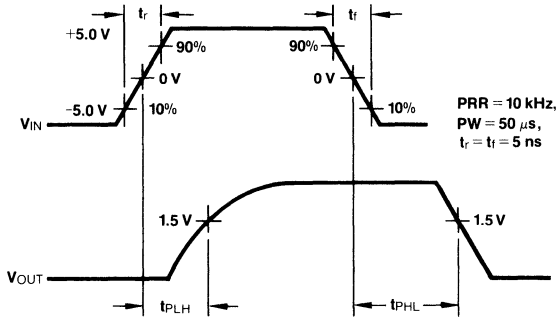


Threshold Current Matching Circuit

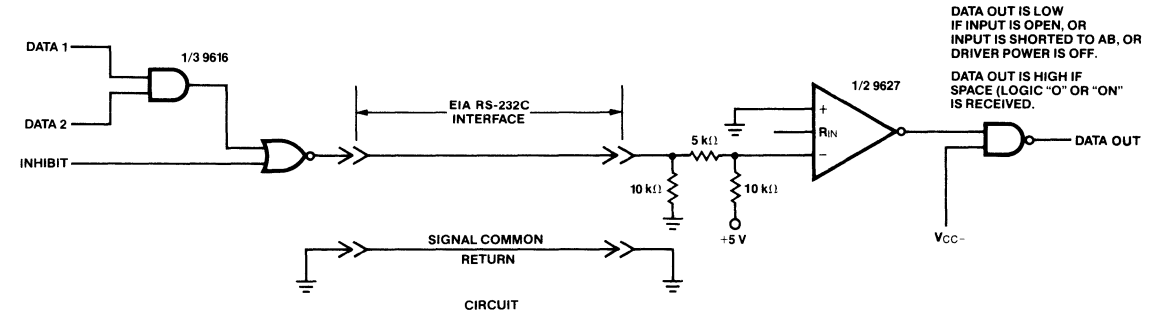


ADJUST POT TO ACHIEVE POSITIVE THRESHOLD CURRENT AND NEGATIVE THRESHOLD CURRENT MATCHING

Notes
15 pF includes jig capacitance
All diodes are FD777 or equivalent

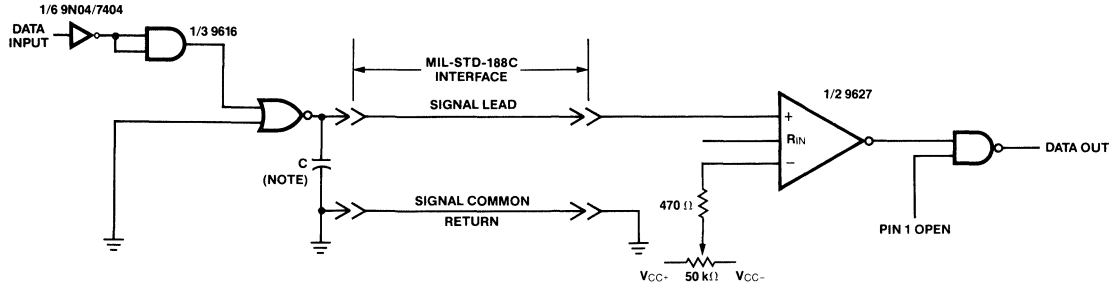


EIA RS-232C Interface with Failsafe Receiver (Pin 1 Connected to V_{CC-})



6

MIL-STD-188C Interface
(Pin 1 Open)



Capacitor for transmitter waveshaping at applicable modulation rate

FAIRCHILD
A Schlumberger Company

μA9636A Dual Programmable Slew Rate Line Driver EIA RS-423 Driver

Interface Products

Description

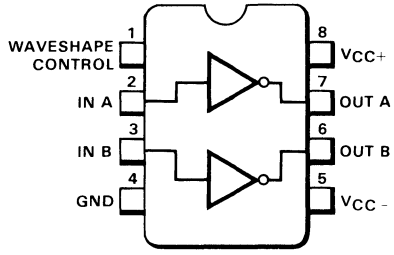
The μA9636A is a TTL/CMOS compatible, dual, single-ended, line driver which has been specifically designed to satisfy the requirements of EIA Standard RS-423.

The μA9636A is suitable for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between the wave shaping control (WS) pin and ground. This eliminates any need for external filtering of the output signals. Output voltage levels and slew rates are independent of power supply variations. Current limiting is provided in both output states. The μA9636A is designed for nominal power supplies of ± 12 V.

Inputs are TTL compatible with input current loading low enough (1/10 UL) to be also compatible with CMOS logic. Clamp diodes are provided on the inputs to limit transients below ground.

- **PROGRAMMABLE SLEW RATE LIMITING**
- **MEETS EIA RS-423 REQUIREMENTS**
- **COMMERCIAL OR MILITARY TEMPERATURE RANGE**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **TTL AND CMOS COMPATIBLE INPUTS**

Connection Diagram
8-Pin DIP



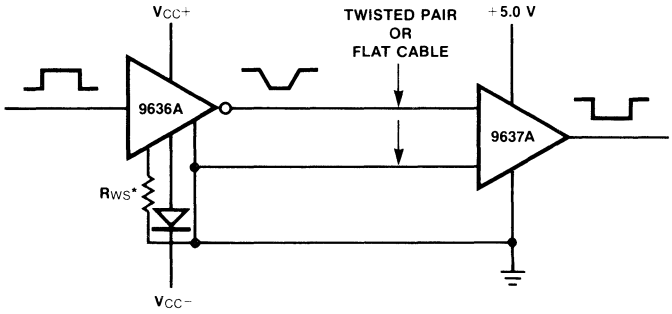
(Top View)

Order Information

Type	Package	Code	Part No.
μA9636A	Ceramic DIP	6T	μA9636ARM
μA9636A	Ceramic DIP	6T	μA9636ARC
μA9636A	Molded DIP	9T	μA9636ATC

6

RS-423 System Application



Note

Newer versions will not require the external diode and normal operation is not impaired if the diode is absent

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

V_{CC}+ Pin Potential to Ground Pin	V_{CC}− to +15 V
V_{CC}− Pin Potential to Ground Pin	+0.5 to −15 V
V_{CC}+ Pin Potential to V_{CC}− Pin	0 to +30 V
Output Potential to Ground Pin	± 15 V
Output Source Current	−150 mA
Output Sink Current	150 mA
Internal Power Dissipation (Note 1)	
9T Molded DIP	1.3 W
6T Ceramic DIP	1.15 W
Operating Temperature	
Military (9636ARM)	−55°C to 125° C
Commercial (9636ARC/ATC)	0°C to 70° C
Storage Temperature	−65° C to 150° C
Pin Temperature	
Molded DIP (Soldering, 10 s)	260° C
Ceramic DIP (Soldering, 60 s)	300°C

Notes

1. Derate at 7.7 mW/°C for ambient temperature above 25°C for 6T package and derate 11.1 mW/°C for 9T package.

μA9636A
Recommended Operating Conditions

Characteristic	μA9636ARM			μA9636ARC, μA9636ATC			Unit
	Min	Typ	Max	Min	Typ	Max	
Positive Supply Voltage (V_{CC}+)	10.8	12	13.2	10.8	12	13.2	V
Negative Supply Voltage (V_{CC}−)	−13.2	−12	−10.8	−13.2	−12	−10.8	V
Operating Ambient Temperature (T_A)	−55	25	125	0	25	70	°C
Wave Shaping Resistance (R_{WS})	10		500	10		1000	kΩ

μA9636A
Electrical Characteristics Over recommended temperature supply voltage and wave shaping resistance ranges unless noted.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH1}	Output HIGH Voltage	R_L to GND (R_L = ∞)	5.0	5.6	6.0	V
V_{OH2}		R_L to GND (R_L = 3 kΩ)	5.0	5.6	6.0	V
V_{OH3}		R_L to GND (R_L = 450 Ω)	4.0	5.5	6.0	V
V_{OL1}	Output LOW Voltage	R_L to GND (R_L = ∞)	−6.0	−5.7	−5.0	V
V_{OL2}		R_L to GND (R_L = 3 kΩ)	−6.0	−5.6	−5.0	V
V_{OL3}		R_L to GND (R_L = 450 Ω)	−6.0	−5.4	−4.0	V
R_O	Output Resistance	450 Ω ≤ R_L		25	50	Ω
I_{SC}+	Output Short Circuit Current	V_{OUT} = 0 V, V_{IN} = 0 V (Note 2)	−150	−60	−15	mA
I_{SC}−	Output Short Circuit Current	V_{OUT} = 0 V, V_{IN} = 2.0 V (Note 2)	15	60	150	mA
I_{OX}	Output Leakage Current	V_{OUT} = ±6 V, Power-Off	−100		100	μA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_{CD}	Input Clamp Diode	I_{IN} = 15 mA	−1.5	−1.1		V
I_{IL}	Input LOW Current	V_{IN} = 0.4 V	−80	−16		μA
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V		1.0	10	μA
		V_{IN} = 5.5 V		10	100	μA
I_{CC}+	Positive Supply Current	V_{CC}+ = +12 V, V_{CC}− = −12 V, R_L = ∞, R_{WS} = 100 kΩ, V_{IN} = 0 V		13	18	mA
I_{CC}−	Negative Supply Current	V_{CC}+ = +12 V, V_{CC}− = −12 V, R_L = ∞, R_{WS} = 100 kΩ, V_{IN} = 0 V	−18	−13		mA

Notes

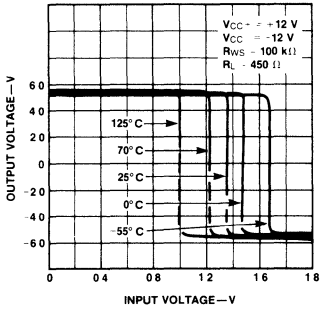
2. Only one output should be shorted at a time.

μA9636A
AC Characteristics $T_A = 25°C$, $V_{CC} = \pm 12\ V$ ± 10%, see AC Test Circuit

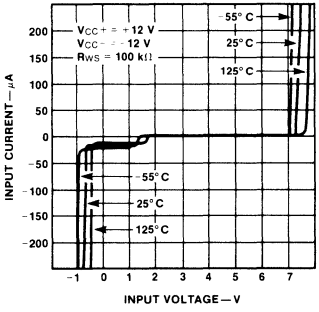
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_r	Output Rise Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	μs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	μs
		$R_{WS} = 500\ k\Omega$	40	55	70	μs
		$R_{WS} = 1000\ k\Omega$	80	110	140	μs
t_f	Output Fall Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	μs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	μs
		$R_{WS} = 500\ k\Omega$	40	55	70	μs
		$R_{WS} = 1000\ k\Omega$	80	110	140	μs

Typical Performance Curves

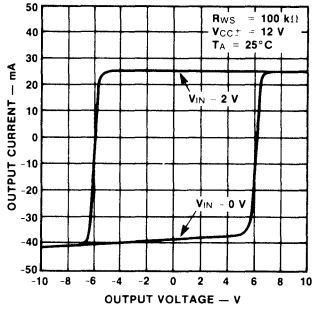
Input/Output Transfer Characteristic vs Temperature



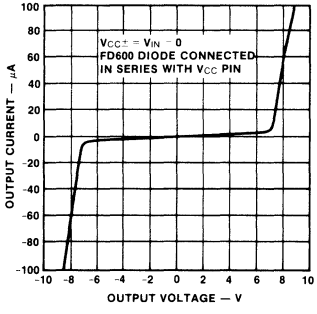
Input Current vs Input Voltage



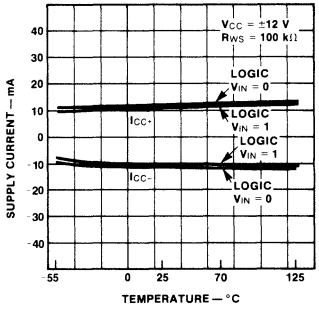
Output Current vs Output Voltage (Power On)



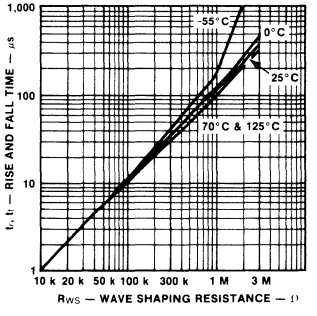
Output Current vs Output Voltage (Power Off)



Supply Current vs Temperature



Transition Time vs R_{WS}



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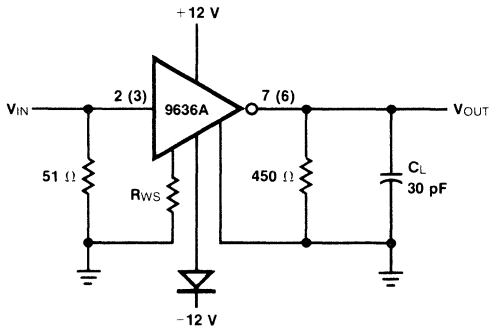
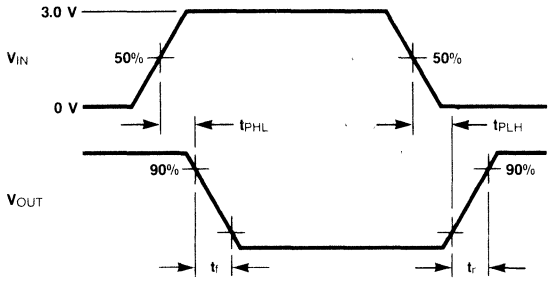
AC Test Circuit and Waveforms



C_L — Includes jig and probe capacitance



V_{IN}
Amplitude 3 0 V
Offset 0 V
Pulse Width 500 μs
PRR 1 kHz
t_r, t_f 10 ns

FAIRCHILD

A Schlumberger Company

μA9637A Dual Differential Line Receiver

Interface Products

Description

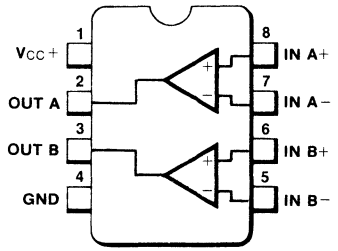
The μA9637A is a Schottky Dual Differential Line Receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422 and RS-423. In addition, the μA9637A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The μA9637A is suitable for use as a line receiver in digital data systems, using either single-ended or differential, unipolar or bipolar transmission. It requires a single 5 V power supply and has Schottky TTL compatible outputs. The μA9637A has an operational input common mode range ±7 V either differentially or to ground.

- **DUAL CHANNELS**
- **SINGLE 5 V SUPPLY**
- **SATISFIES EIA STANDARDS RS-422 AND RS-423**
- **BUILT IN ±35 mV HYSTERESIS**
- **HIGH COMMON MODE RANGE**
- **HIGH INPUT IMPEDANCE**
- **TTL COMPATIBLE OUTPUT**
- **SCHOTTKY TECHNOLOGY**

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Supply Voltage (V_{CC} Potential to Ground)	−0.5 V to 7.0 V
Input Potential to Ground Pin	±15 V
Differential Input Voltage	±15 V
Output Potential to Ground Pin	−0.5 V to 5.5 V
Output Sink Current	50 mA
Internal Power Dissipation (Note 1)	
6T Ceramic DIP	1.15 W
9T Molded DIP	1.3 W
Operating Temperature	
μA9637ARM	−55°C to 125°C
μA9637ARC, μA9637ATC	0°C to 70°C
Storage Temperature	−65°C to 150°C
Pin Temperature	
Ceramic DIP (Soldering, 30 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Connection Diagram 8-Pin DIP



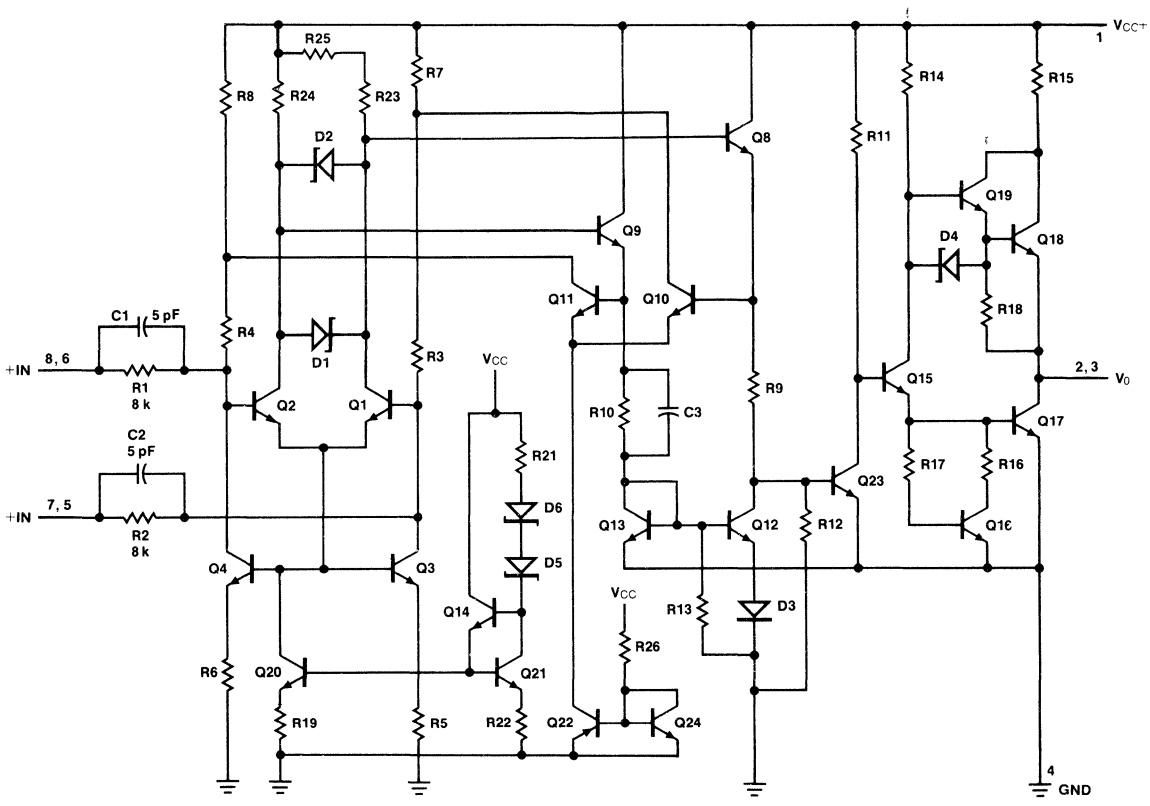
Top View

Order Information

Type	Package	Code	Part No.
μA9637A	Ceramic DIP	6T	μA9637ARM
μA9637A	Ceramic DIP	6T	μA9637ARC
μA9637A	Molded DIP	9T	μA9637ATC

6

Equivalent Circuit



μA9637A
Recommended Operating Conditions

Characteristic	μA9637ARM			μA9637ARC, μA9637ATC			Unit
	Min	Typ	Max	Min	Typ	Max	
Supply Voltage (V_{CC})	4.5	5.0	5.5	4.75	5.0	5.25	V
Operating Ambient Temperature (T_A)	−55	25	125	0	25	70	°C

μA9637A
Electrical Characteristics Over recommended temperature and supply voltage ranges, unless otherwise noted.

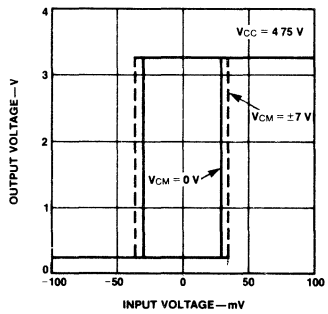
Symbol	Characteristic	Condition (1)	Min	Typ	Max	Unit
V_{TH}	Differential Input Threshold Voltage	$-7.0\ V \leq V_{CM} \leq 7.0\ V$ (3)	−0.2		0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage	$-7.0\ V \leq V_{CM} \leq 7.0\ V$ (4)	−0.4		0.4	V
I_{IN}	Input Current	V_{IN} = 10 V, $0 \leq V_{CC} \leq 5.5\ V$ (5) $V_{IN} = -10\ V$, $0 \leq V_{CC} \leq 5.5\ V$ (5)	 −3.25	1.1 −1.6	3.25	mA mA
V_{OL}	Output LOW Voltage	I_{OL} = 20 mA, V_{CC} = Min		0.35	0.5	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0$ mA, V_{CC} = Min	2.5	3.5		V
I_{SC}	Output Short Circuit Current	V_{OUT} = 0 V, V_{CC} = Max (6)	−40	−75	−100	mA
I_{CC}	Supply Current	V_{CC} = Max, $V_{IN(+)}$ = 0.5 V, $V_{IN(-)}$ = GND, (Both outputs low)		35	50	mA
V_{HYST}	Input Hysteresis	$V_{CM} = \pm 7$ V (See curves)		70		mV

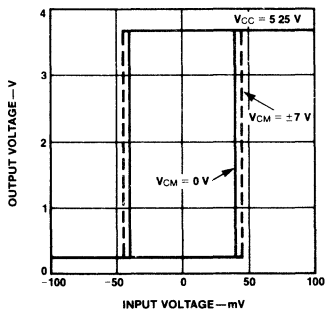
μA9637A
AC Characteristics V_{CC} = 5 V, T_A = 25°C

Symbol	Characteristic	Condition (1)	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time LOW to HIGH	See AC Test Circuit		15	25	ns
t_{PHL}	Propagation Delay Time HIGH to LOW	See AC Test Circuit		13	25	ns

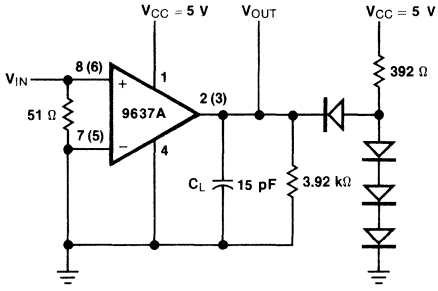
Notes
2 Use Min/Max values specified in recommended operating conditions
3. Typical limits are at V_{CC} = 5.0 V and 25°C
4. V_{DIFF} (Differential Input Voltage) = $(V_{IN+}) - (V_{IN-})$
V_{CM} (Common Mode Input Voltage) = (V_{IN+}) or (V_{IN-})
5 500 Ω ± 1% in series with inputs
6 The input not under test is tied to ground
7 Only one output should be shorted at a time.

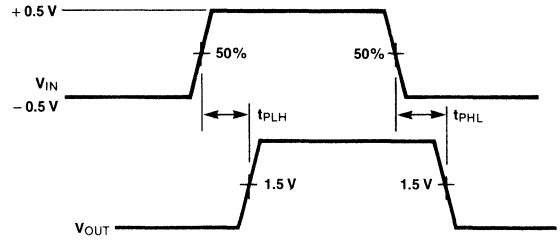
Typical Input/Output Transfer Characteristics





AC Test Circuit and Waveforms



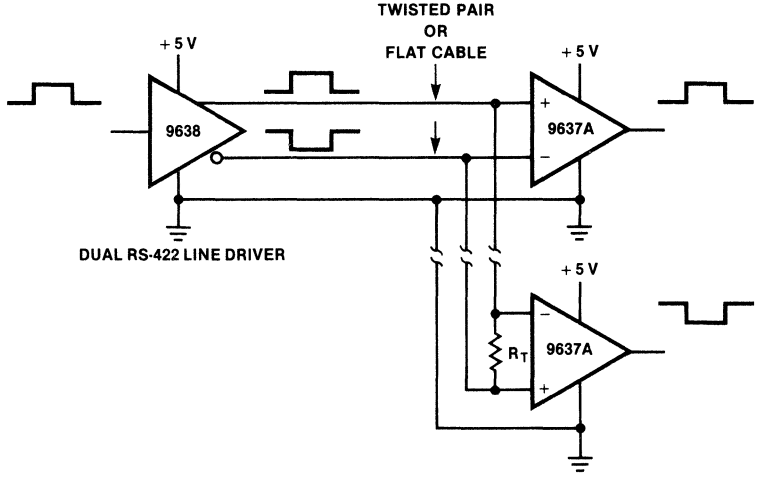


C_L includes jig and probe capacitance. All diodes are FD700 or equivalent.

V_{IN}
Amplitude: 1 0 V
Offset: 0.5 V
Pulse Width: 100 ns
PRR. 5 MHz
t_r t_f = ≤ 5 ns

Typical Application

RS-422 System Application (FIPS 1020) Differential Simplex Bus Transmission



Note
R_t ≥ 50 Ω for RS-422 operation
R_t combined with input impedance of receivers must be greater than 90 Ω.

FAIRCHILD
A Schlumberger Company

μA9638 Dual High-Speed Differential Line Driver (EIA-RS-422)

Interface Products

Description

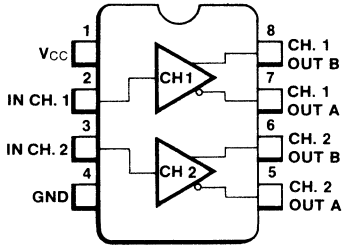
The 9638 is a Schottky, TTL-compatible Dual Channel Differential Line Driver, designed specifically to meet the EIA-RS-422 specifications. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem-pole TTL outputs, with active pull-up and pull-down. The device features a short-circuit protected active pull-up with low output impedance and is specified to drive 50 Ω transmission lines at high speed. The mini DIP provides high package density.

- **SINGLE 5 V SUPPLY**
- **SCHOTTKY TECHNOLOGY**
- **TTL AND CMOS-COMPATIBLE INPUTS**
- **OUTPUT SHORT-CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **COMPLEMENTARY OUTPUTS**
- **MINIMUM OUTPUT SKEW (< 1 ns TYPICAL)**
- **50 mA OUTPUT DRIVE CAPABILITY FOR 50 Ω TRANSMISSION LINES**
- **MEETS EIA-RS-422 SPECIFICATIONS**
- **PROPAGATION DELAY OF LESS THAN 10 ns**
- **"GLITCHLESS" DIFFERENTIAL OUTPUT**
- **DELAY TIME STABLE WITH V_{CC} AND TEMPERATURE VARIATIONS (< 2 ns TYPICAL) (FIGURE 3)**

Absolute Maximum Ratings

V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +7.0 V
Internal Power Dissipation	800 mW
Operating Temperature	
9638RM	−55° C to +125° C
9638RC,9638TC	0° C to 70° C
Storage Temperature	−65° C to +150° C
Pin Temprature	
Molded DIP (Soldering, 10 s)	260° C
Ceramic DIP (Soldering, 30 s)	300° C

Connection Diagram
8-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA9638	Ceramic DIP	6T	μA9638RM
μA9638	Ceramic DIP	6T	μA9638RC
μA9638	Molded DIP	9T	μA9638TC

6

Recommended Operating Conditions

Symbol	Characteristic	9638RM			9638RC, 9638TC			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
I_{OH}	Output HIGH Current			−50			−50	mA
I_{OL}	Output LOW Current			50			50	mA
T_A	Ambient Temperature	−55		125	0		70	°C

Electrical Characteristics Over recommended ambient temperature, unless otherwise noted

Symbol	Characteristic	Condition (Notes 1 and 2)		Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage	9638RC, 9638TC				0.8	V
		9638RM				0.7	
V_I	Clamped Input Voltage	V_{CC} = Min, I_{IN} = −18 mA			−1.0	−1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IH} = V_{IH} Min,	I_{OH} = −10 mA	2.5	3.5		V
		V_{IL} = V_{IL} Max	I_{OH} = −40 mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IH} = V_{IH} Min, V_{IL} = V_{IL} Max, I_{OL} = 40 mA				0.5	V
I_{IN}	Input Current at Maximum Input Voltage	V_{CC} = Max, V_{IN} Max = 5.5 V				50	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IH} = 2.7 V				25	μA
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IL} = 0.5 V				−200	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, V_{OUT} = 0 V		−50		−150	mA
V_T, $\overline{V}_T$	Terminated Output Voltage	See *Figure 1*		2.0			V
$V_T - \overline{V}_T$	Output Balance					0.4	V
V_{OS},$\overline{V}_{OS}$	Output Offset Voltage					3.0	V
$V_{OS}-\overline{V}_{OS}$	Output Offset Balance					0.4	V
I_x	Output Leakage Current	−0.25 V < Vx < 6.0 V				100	μA
I_{CC}	Supply Current (both drivers)	All input at 0 V, V_{CC} = 5.5 V, no load			45	65	mA

AC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PHL}	Propagation Delay	T_A = 25°C, C_L = 15 pF (Note 2), R_L = 100 Ω, See *Figure 2*		10	20	ns
t_{PLH}				10	20	ns
t_f	Fall Time, 90% − 10%			10	20	ns
t_r	Rise Time, 10% − 90%			10	20	ns
$t_{PA}-t_{PB}$	Skew Between Outputs A and B			1		ns

Notes

1 Use minimum and maximum values specified in recommended operating conditions.

2. Typical limits are at V_{CC} = 5.0 and T_A = 25°C.

DC Test Circuit

Fig. 1 Terminated Output Voltage and Output Balance

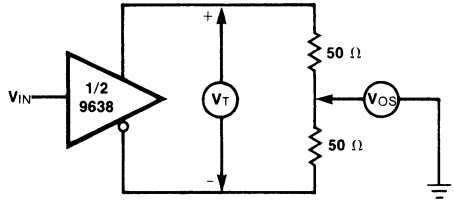
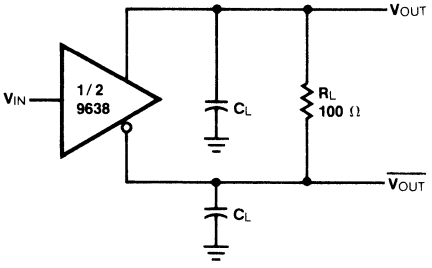
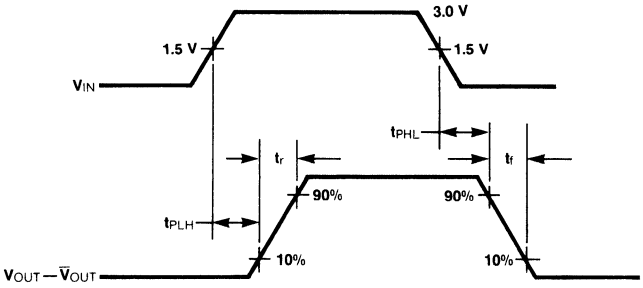


Fig. 2 AC Test Circuit and Voltage Waveform



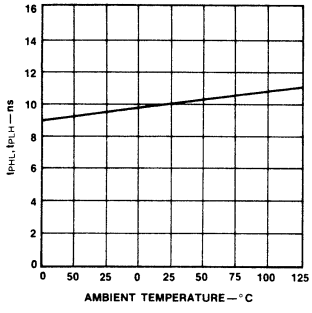


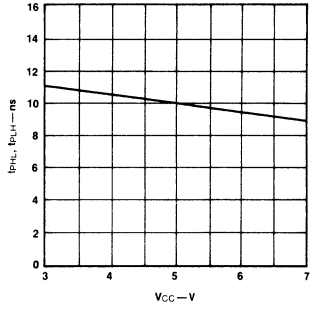
Notes

1 The pulse generator has the following characteristics
Z_{OUT} = 50 Ω, PRR = 500 kHz
t_W = 100 ns, $t_r \leq 5$ ns

2 C_L includes probe and jig capacitance

Fig. 3 Typical Delay Characteristics





6

FAIRCHILD
A Schlumberger Company

μA1488
RS-232C
Quad Line Driver

Interface Products

Description

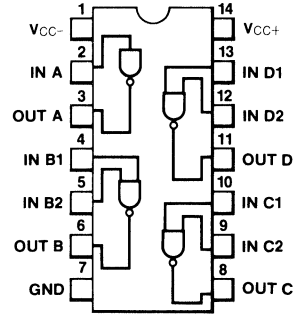
The μA1488 is an EIA RS-232C specified Quad Line Driver. This device is used to interface data terminals with data communications equipment. The μA1488 is a pin-for-pin replacement of the MC1488.

- **CURRENT LIMITED OUTPUT— ± 10 mA TYP**
- **POWER-OFF SOURCE IMPEDANCE 300 Ω MIN**
- **SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR**
- **FLEXIBLE OPERATING SUPPLY RANGE**

Absolute Maximum Ratings (at 25°C unless otherwise noted)

Power Supply Voltages	
VCC+	+15 V
VCC−	−15 V
Input Voltage Range (V_{IR})	−15 Vdc to +7.0 Vdc
Output Signal Voltage	± 15 Vdc
Continuous Total Power Dissipation (Note 1)	800 mW
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Pin Temperatures	
Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Connection Diagram
14-Pin DIP



(Top View)

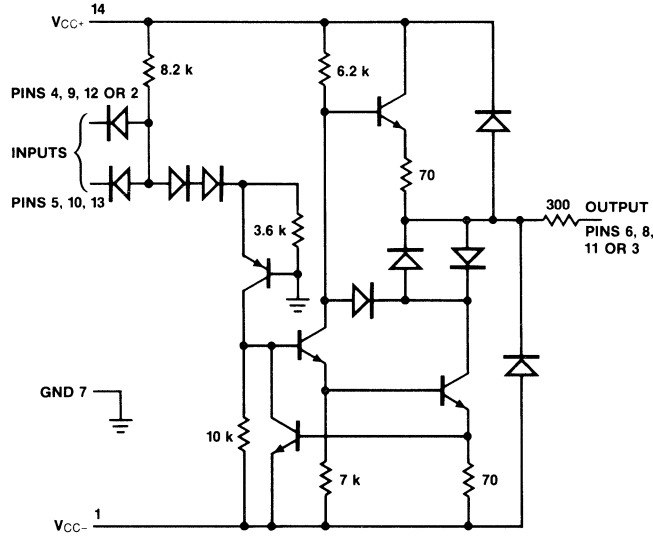
Order Information

Type	Package	Code	Part No.
μA1488	Ceramic DIP	6A	μA1488DC
μA1488	Molded DIP	9A	μA1488PC

Notes

1 Above 60°C ambient temperatures, derate linearly at 8 3 mW/°C

Circuit Schematic (¼ of Circuit Shown)



DC Characteristics V_{CC+} = +9.0 V ± 1%, V_{CC-} = −9.0 V ± 1%, T_A = 0 to +70°C, unless otherwise noted.

Symbol	Characteristic	Condition	Fig	Min	Typ	Max	Unit
I_{IL}	Input LOW Current	V_{IL} = 0	1		1.0	1.6	mA
I_{IH}	Input HIGH Current	V_{IH} = 5.0 V	1			10	μA
V_{OH}	Output HIGH Voltage	V_{IL} = 0.8 V, R_L = 3.0 kΩ V_{CC+} = +9.0 V, V_{CC-} = −9.0 V	2	+6.0	+7.0		V
		V_{IL} = 0.8 V, R_L = 3.0 kΩ V_{CC+} = +13.2 V, V_{CC-} = −13.2 V	2	+9.0	+10.5		
V_{OL}	Output LOW Voltage	V_{IH} = 1.9 V, R_L = 3.0 kΩ V_{CC+} = +9.0 V, V_{CC-} = −9.0 V	2	−6.0	−7.0		V
		V_{IH} = 1.9 V, R_L = 3.0 kΩ V_{CC+} = +13.2 V, V_{CC-} = −13.2 V	2	−9.0	−10.5		
I_{OS+}	Positive Output Short-Circuit Current	V_{IL} = 0.8 V (Note 2)	3	+6.0	+10	+12	mA
I_{OS-}	Negative Output Short-Circuit Current	V_{IH} = 1.9 V (Note 2)	3	−6.0	−10	−12	mA
R_{OUT}	Output Resistance	V_{CC+} = V_{CC-} = 0 V, V_O = ±2.0 V	4	300			Ω
I_{CC+}	Positive Supply Current	R_L = ∞ V_{IH} = 1.9 V, V_{CC+} = +0.9 V V_{IL} = 0.8 V, V_{CC-} = +9.0 V V_{IH} = 1.9 V, V_{CC+} = +12 V V_{IL} = 0.8 V, V_{CC+} = +12 V V_{IH} = 1.9 V, V_{CC+} = +15 V V_{IL} = 0.8 V, V_{CC+} = +15 V	5		+15 +4.5 +19 +5.5	+20 +6.0 +25 +7.0 +34 +12	mA
I_{CC-}	Negative Supply Current	R_L = ∞ V_{IH} = 1.9 V, V_{CC-} = −9.0 V V_{IL} = 0.8 V, V_{CC-} = −9.0 V V_{IH} = 1.9 V, V_{CC-} = −12 V V_{IL} = 0.8 V, V_{CC-} = −12 V V_{IH} = 1.9 V, V_{CC-} = −15 V V_{IL} = 0.8 V, V_{CC-} = −15 V	5		−13 −18	−17 −15 −23 −15 −34 −2.5	mA μA mA μA mA mA
P_C	Power Consumption	V_{CC+} = 9.0 V, V_{CC-} = −9.0 V V_{CC+} = 12 V, V_{CC-} = −12 V				333 576	mW

AC Characteristics V_{CC+} = +9.0 V ± 1%, V_{CC-} = −9.0 V ± 1%, T_A = 25°C

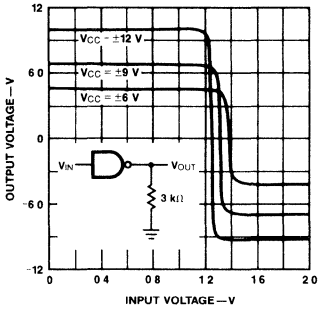
Symbol	Characteristic	Condition	Fig	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Time	R_L = 3.0 kΩ, C_L = 15 pF	6		220 70	350 175	ns
t_f t_r	Fall Time Rise Time	R_L = 3.0 kΩ, C_L = 15 pF	6		70 55	75 100	ns

Notes

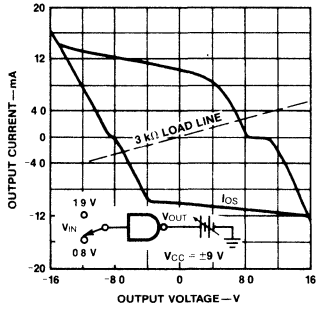
2 Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously

Typical Performance Curves

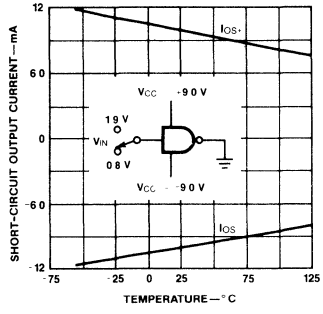
Transfer Characteristics as a Function of Power Supply Voltage



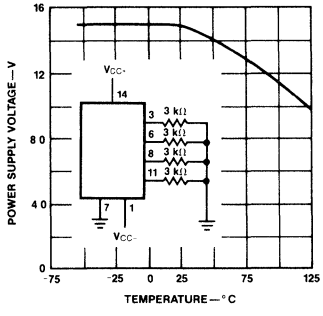
Output Voltage and Current Limiting Characteristics



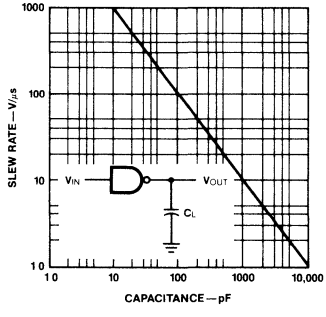
Short-Circuit Output Current as a Function of Temperature



Maximum Operating Temperature as a Function of Power Supply Voltage



Output Slew Rate as a Function of Load Capacitance



DC Test Circuits

Fig. 1 Input Current

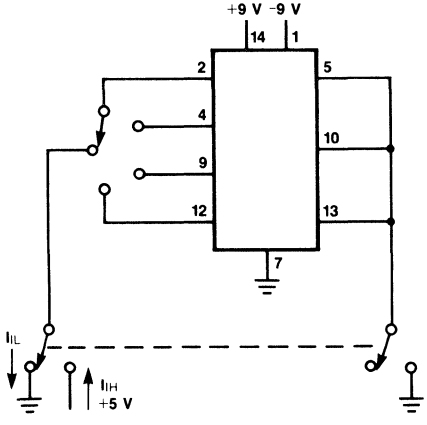


Fig. 2 Output Voltage

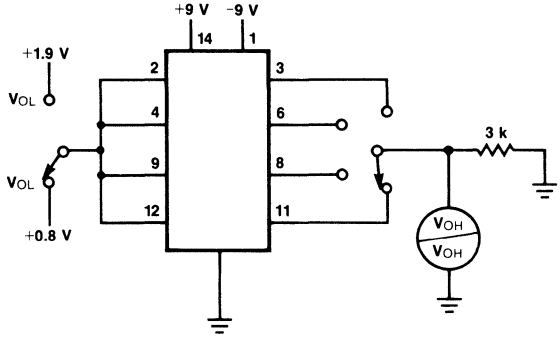


Fig. 3 Output Short-Circuit Current

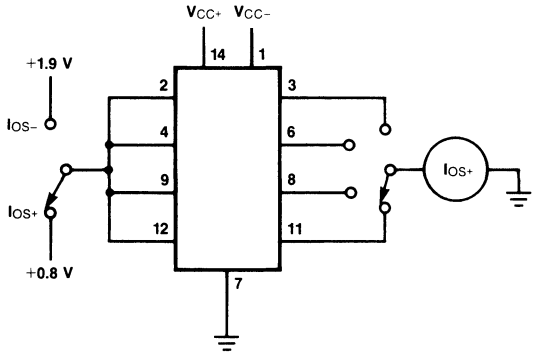


Fig. 4 Output Resistance (Power-off)

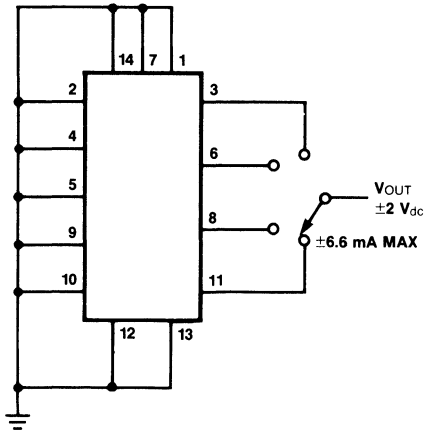


Fig. 5 Power-Supply Currents

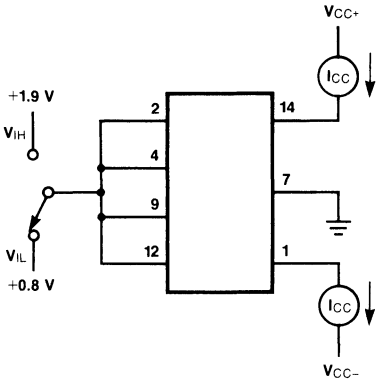
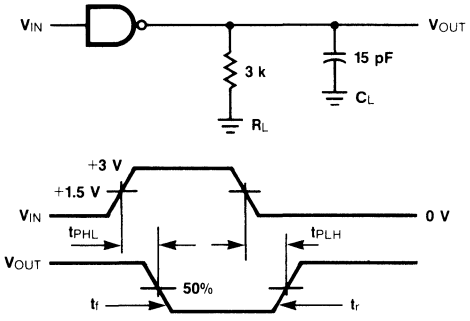


Fig. 6 AC Test Circuit and Voltage Waveform



t_r and t_f are measured 10% to 90%

6

FAIRCHILD
A Schlumberger Company

μA1489 • μA1489A RS-232C Quad Line Receivers

Interface Products

Description

The μA1489 and the μA1489A are EIA RS-232C specified Quad Line Receivers. These devices are used to interface data terminals with data communications equipment. The μA1489 and μA1489A are pin-for-pin replacements of the MC1489 and MC1489A respectively.

- **INPUT RESISTANCE 3.0 kΩ to 7.0 kΩ**
- **INPUT SIGNAL RANGE ±30 V**
- **INPUT THRESHOLD HYSTERESIS BUILT IN**
- **RESPONSE CONTROL**
  - **a) LOGIC THRESHOLD SHIFTING**
  - **b) INPUT NOISE FILTERING**

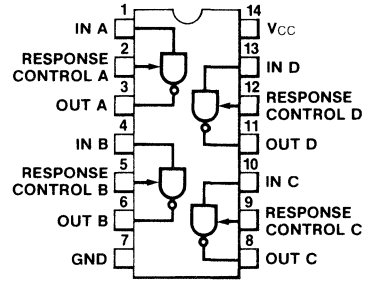
Absolute Maximum Ratings

Power Supply Voltage	+10 Vdc
Input Voltage Range	±30 Vdc
Output Load Current	20 mA
Continuous Total Power Dissipation (Note 1)	800 mW
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to + 175°C
Pin Temperatures	
Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Notes

1 Above 60°C ambient temperature, derate linearly at 8 3 mW/°C

Connection Diagram 14-Pin DIP

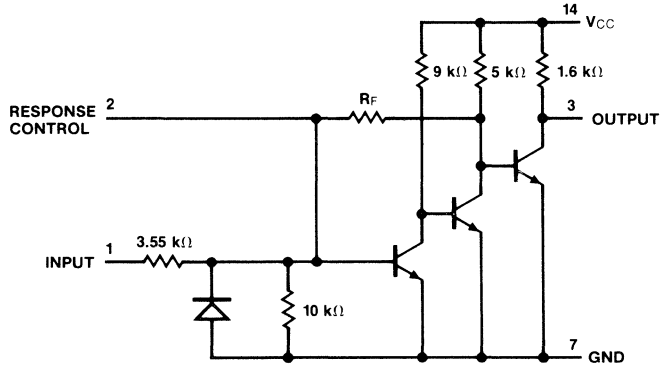


(Top View)

Order Information

Type	Package	Code	Part No.
μA1489	Ceramic DIP	6A	μA1489DC
μA1489	Molded DIP	9A	μA1489PC
μA1489A	Ceramic DIP	6A	μA1489ADC
μA1489A	Molded DIP	9A	μA1489APC

Circuit Schematic (1/4 of circuit shown)



	μA1489	μA1489A
RF	10 kΩ	2 kΩ

DC Characteristics V_{CC} = 5.0 V ± 1%, response control pin is open, T_A = 0°C to 70°C unless otherwise noted.

Symbol	Characteristic	Condition		Fig	Min	Typ	Max	Unit
I_{IH}	Positive Input Current	V_{IH} = 25 V V_{IH} = 3.0 V		1	3.6 0.43		8.3	mA
I_{IL}	Negative Input Current	V_{IL} = −25 V V_{IL} = −3.0 V		1	−3.6 −0.43		−8.3	mA
V_{IHL}	Input Turn-on Threshold Voltage	T_A =25°C, $V_{OL} \leq$ 0.45 V	μA1489 μA1489A	2	1.0 1.75	 1.95	1.5 2.25	V
V_{ILH}	Input Turn-off Threshold Voltage	T_A = 25°C, $V_{OH} \geq$ 2.5 V, I_L = −0.5 mA	μA1489 μA1489A	2	0.75 0.75	 0.8	1.25 1.25	V
V_{OH}	Output HIGH Voltage	V_{IH} = 0.75 V, I_L = −0.5 mA Input open circuit, I_L = −0.5 mA		2	2.6	4.0	5.0	V
V_{OL}	Output LOW Voltage	V_{IL} = 3.0 V, I_L = 10 mA		2		0.2	0.45	V
I_{OS}	Output Short-circuit Current			3		3.0		mA
I_{CC}	Power Supply Current	V_{IH} = 5.0 V		4		20	26	mA
P_C	Power Consumption	V_{IH} = 5.0 V		4		100	130	mW

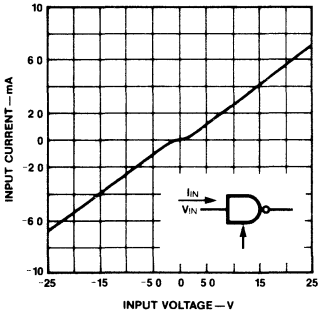
AC Characteristics V_{CC} = 5.0 V ± 1%, T_A = 25°C

Symbol	Characteristic	Condition	Fig	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Time	R_L = 3.9 kΩ R_L = 390 Ω	5		25 25	85 50	ns
t_r t_f	Rise Time Fall Time	R_L = 3.9 kΩ R_L = 390 Ω	5		120 10	175 20	ns

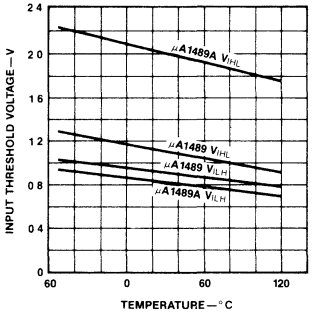
6

Typical Performance Curves

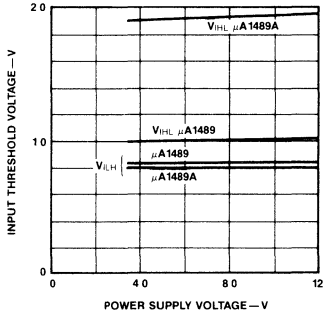
Input Current as a Function of Input Voltage



Input Threshold Voltage as a Function of Temperature

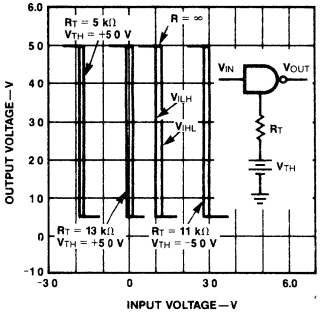


Input Threshold Voltage as a Function of Power Supply Voltage

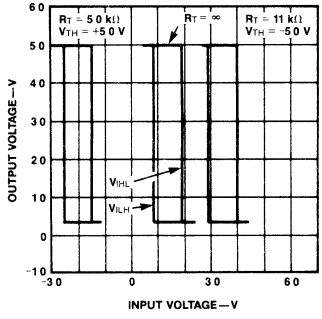


Performance Curves (Cont.)

μA1489 Input Threshold Voltage Adjustment



μA1489A Input Threshold Voltage Adjustment



Test Circuits

Fig. 1 Input Current

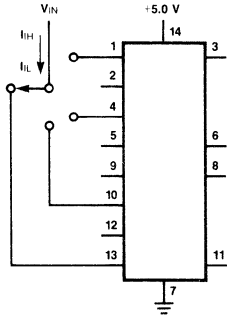


Fig. 3 Output Short-Circuit Current

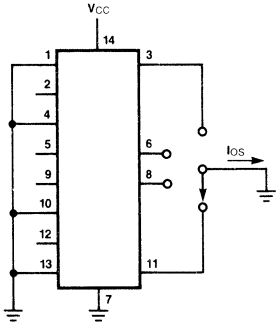


Fig. 2 Output Voltage and Input Threshold Voltage

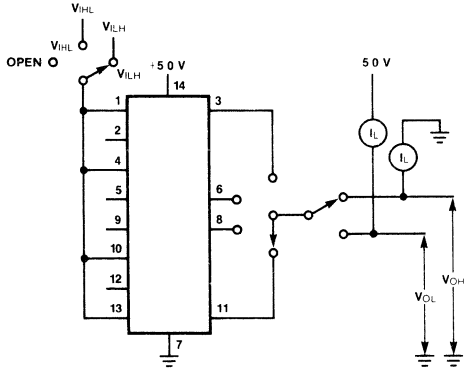


Fig. 4 Power Supply Current

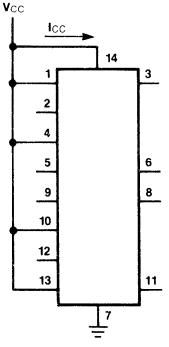
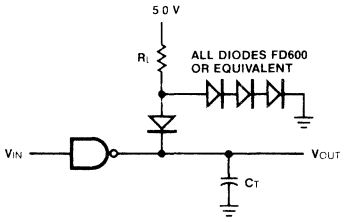


Fig. 5 AC Test Circuit and Voltage Waveforms



Note

C_T = 15 pf = Total parasitic capacitance, which includes probe and jig capacitance.

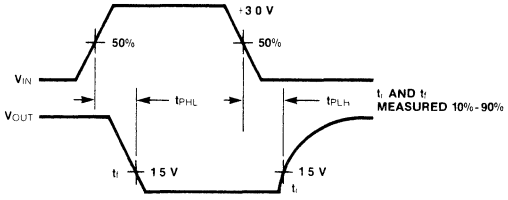
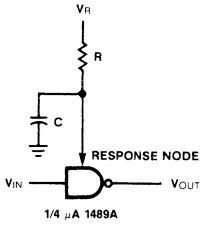


Fig. 6 Response Control Node



Notes

Capacitor is for noise filtering
Resistor is for threshold shifting

6

FAIRCHILD
A Schlumberger Company

μA55/75107A•μA75107B
μA75108B
Dual Line Receivers

Interface Products

Description

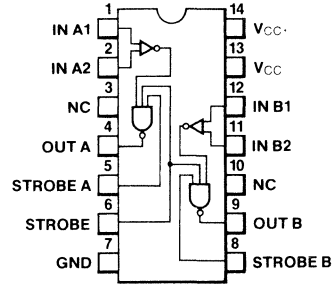
The devices in this series are high-speed, two-channel Line Receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25 mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. They feature high-input impedance and low-input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3 V but can be increased to ±15 V by the use of input attenuators. Separate or common strobes are available. The 55/75107 circuits feature an active pull-up (totem-pole output). The 75108B circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the 55110/75110A line drivers. These line receivers are useful in high-speed balanced, unbalanced and party-line transmission systems and as data comparators.

- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **HIGH COMMON-MODE REJECTION RATIO**
- **HIGH INPUT IMPEDANCE**
- **HIGH INPUT SENSITIVITY**
- **INPUT COMMON-MODE VOLTAGE RANGE OF ±3 V**
- **SEPARATE OR COMMON STROBES**
- **WIRED-OR OUTPUT CAPABILITY**
- **HIGH dc NOISE MARGINS**
- **STROBE INPUT CLAMP DIODES**
- **INPUT IS DIODE PROTECTED AGAINST POWER-OFF LOADING ON B VERSIONS DEVICES**

Absolute Maximum Ratings

Supply Voltage (Note 1)	±7 V
Internal Power Dissipation (Note 3)	670 mW
Differential Input Voltage (Note 2)	±6 V
Common Mode Input Voltage (Note 1)	±5 V
Strobe Input Voltage (Note 1)	5.5 V
Operating Temperature Range	
55107A	−55°C to +125°C
75107A/107B/108B	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Connection Diagram
14-Pin DIP



(Top View)

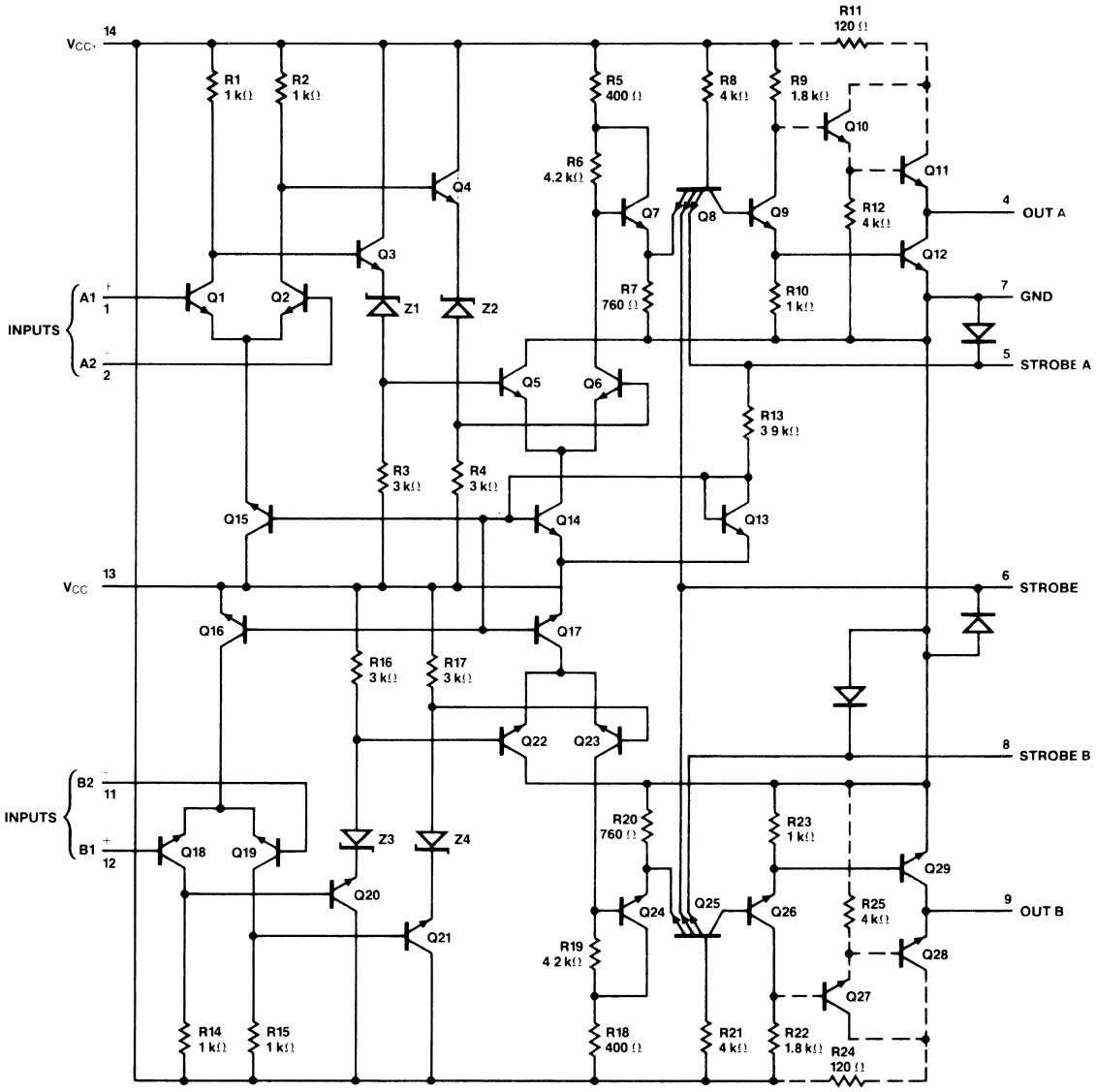
Order Information

Type	Package	Code	Part No.
μA55107A	Ceramic DIP	6A	μA55107ADM
μA75107A	Ceramic DIP	6A	μA75107ADC
μA75107A	Molded DIP	9A	μA75107APC
μA75107B	Ceramic DIP	6A	μA75107BDC
μA75107B	Molded DIP	9A	μA75107BPC
μA75108B	Molded DIP	9A	μA75108BPC

Notes

1. These voltages are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (−) terminal.
3. For Ceramic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C.

Equivalent Circuit



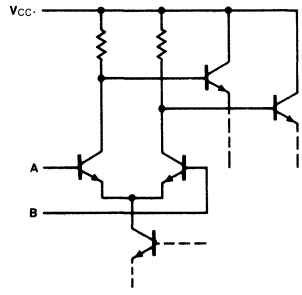
Note

Components shown with dashed lines are applicable to the 55107A and 75107B only. See description for differences between A and B versions

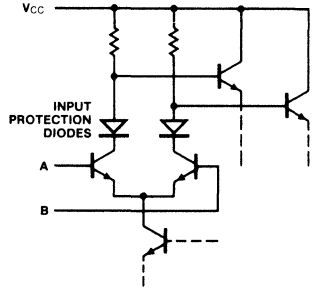
Pin 3 not connected

Circuit Differences Between A and B Versions
The essential difference between the 55/75107A and 75107B versions is shown in the following schematics of the input stage:

"A" Version

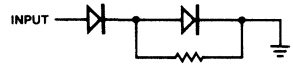


"B" Version

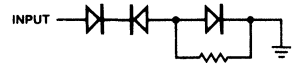


The input protection diodes are useful in certain party-line systems which may have multiple V_{CC+} power supplies and, in which case, may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

"A" Version



"B" Version

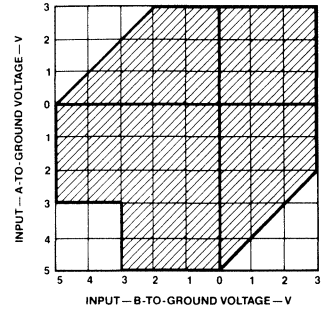


This would be a problem in specific systems which might possibly have the transmission lines biased to some potential greater than 1.4 V. Since this is not a widespread application problem, both the A and B versions will be available. The ratings and characteristic specifications of the B versions are the same as those of the A versions.

Truth Table

Differential Inputs	Strobes		Output
A-B	G	S	
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} <$ 25 mV	L or H	L	H
	L	L or H	H
	H	H	Indeterminate
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

Recommended Combinations of Input Voltage for Line Receivers



55/75107A, 75107B
DC Characteristics Ratings apply over full ambient temperature range with V_{CC+} = Max and V_{CC-} = Max, unless otherwise noted (Notes 4 & 6)

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{DIFF} = 0.5 V, V_{CM} = −3 V to +3 V			30	75	μA
I_{IL}	Input LOW Current	V_{DIFF} = −2 V, V_{CM} = −3 V to +3 V				−10	μA
$I_{IH(G)}$	Gate Input HIGH Current	V_{GATE} = 2.4 V				40	μA
		V_{GATE} = V_{CC+}				1.0	mA
$I_{IL(G)}$	Gate Input LOW Current	V_{GATE} = 0.4 V				−1.6	mA
$I_{IH(S)}$	Strobe Input HIGH Current	V_{STROBE} = 2.4 V				80	μA
		V_{STROBE} = V_{CC+}				2.0	mA
$I_{IL(S)}$	Strobe Input LOW Current	V_{STROBE} = 0.4 V				−3.2	mA
V_{OH}	Output HIGH Voltage	I_L = −400 μA, V_{CM} = −3 V to +3 V	V_{CC+} = MIN, V_{CC-} = MIN	2.4			V
V_{OL}	Output LOW Voltage	I_{SINK} = 16 mA, V_{CM} = −3 V to +3 V	V_{CC+} = MIN, V_{CC-} = MIN			0.4	V
I_{SC}	Short-Circuit Output Current	V_{OUT} = 0 (Note 5)		−18		−70	mA
I_{CC+}	Positive Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			18	30	mA
I_{CC-}	Negative Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			−8.4	−15	mA

55/75107A, 75107B
AC Characteristics V_{CC+} = +5 V, V_{CC-} = −5 V, R_L = 390 Ω, C_L = 50 pF, T_A = 25°C. See Test Circuit

$t_{PLH(D)}$	Propagation Delay Time		17	25	ns
$t_{PHL(D)}$			17	25	ns
$t_{PLH(S)}$			10	15	ns
$t_{PHL(S)}$			10	15	ns

6

Notes
4 For 55107A guaranteed supply voltage range is ±4 5 V to ±5 5 V Operating temperature range is −55°C ≤ T_A ≤ +125°C
For 75107A/B and 75108B guaranteed supply voltage range is ±4 75 V to ±5 25 V. Operating temperature range is 0°C ≤ T_A ≤ 70°C

5 Not more than one (1) output should be shorted at a time
6 V_{CC-} Max implies V_{CC-} = −5.5 V or −5 25 V, depending on device type

75108B
DC Characteristics Ratings apply over full ambient temperature range with V_{CC+} = Max and V_{CC-} = Max, unless otherwise noted (Notes 4 & 6)

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{DIFF} = 0.5 V, V_{CM} = −3 V to +3 V			30	75	μA
I_{IL}	Input LOW Current	V_{DIFF} = −2 V, V_{CM} = −3 V to +3 V				−10	μA
$I_{IH(G)}$	Gate Input HIGH Current	V_{GATE} = 2.4 V				40	μA
		V_{GATE} = V_{CC+}				1.0	mA
$I_{IL(G)}$	Gate Input LOW Current	V_{GATE} = 0.4 V				−1.6	mA
$I_{IH(S)}$	Strobe Input HIGH Current	V_{STROBE} = 2.4 V				80	μA
		V_{STROBE} = V_{CC+}				2.0	mA
$I_{IL(S)}$	Strobe Input LOW Current	V_{STROBE} = 0.4 V				−3.2	mA
V_{OL}	Output LOW Voltage	I_{SINK} = 16 mA, V_{CM} = −3 V to +3 V	V_{CC+} = MIN, V_{CC-} = MIN			0.4	V
I_{OH}	Output HIGH Current	V_{OUT} = V_{CC+}	V_{CC+} = MIN, V_{CC-} = MIN			250	μA
I_{CC+}	Positive Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			18	30	mA
I_{CC-}	Negative Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			−8.4	−15	mA

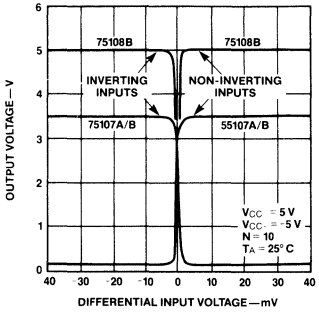
75108B
AC Characteristics V_{CC+} = +5 V, V_{CC-} = −5 V, R_L = 390 Ω, C_L = 15 pF, T_A = 25°C. See Test Circuit

$t_{PLH(D)}$	Propogation Delay Time			19	25	ns
$t_{PHL(D)}$				19	25	ns
$t_{PLH(S)}$				13	20	ns
$t_{PHL(S)}$				13	20	ns

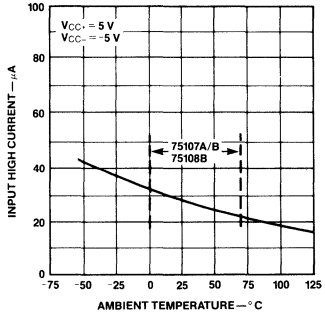
Notes
4. For 55107A guaranteed supply voltage range is ±4.5 V to ±5.5 V. Operating temperature range is −55°C ≤ T_A ≤ +125°C.
   For 75107A/B and 75108B guaranteed supply voltage range is ±4.75 V to ±5.25 V. Operating temperature range is 0°C ≤ T_A ≤ 70°C.
5. Not more than one (1) output should be shorted at a time.
6. V_{CC-} Max implies V_{CC-} = −5.5 V or −5.25 V, depending on device type.

Typical Performance Curves

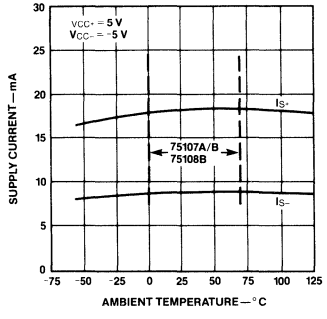
Output Voltage vs Differential Input Voltage



Input HIGH Current Into 1A or 2A vs Ambient Temperature

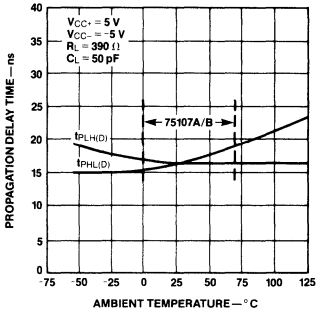


High Logic Level Supply Current vs Ambient Temperature

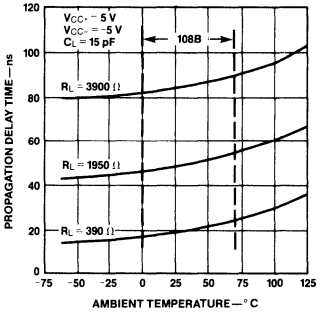


Performance Curves (Cont.)

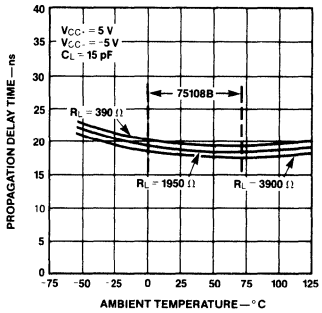
55/75107A, 75107B Propagation Delay Time (Differential Inputs) vs Ambient Temperature



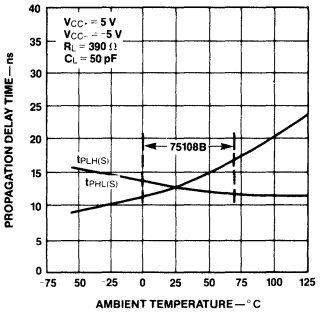
75108B Propagation Delay Time LOW-to-HIGH Level vs Ambient Temperature



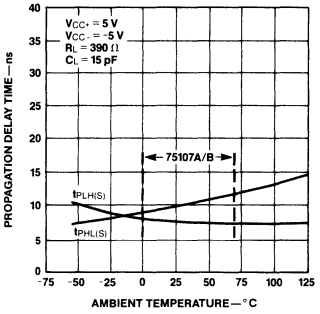
75108B Propagation Delay Time HIGH-to-LOW Level vs Ambient Temperature



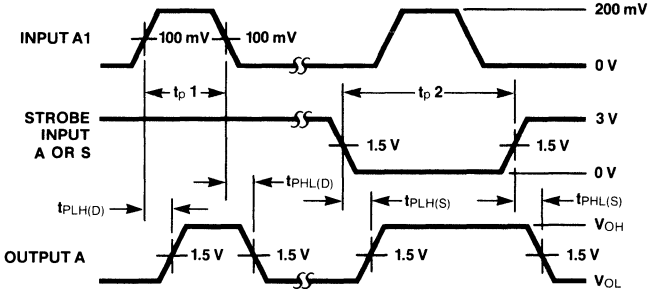
75108B Propagation Delay Time (Strobe Inputs) vs Ambient Temperature



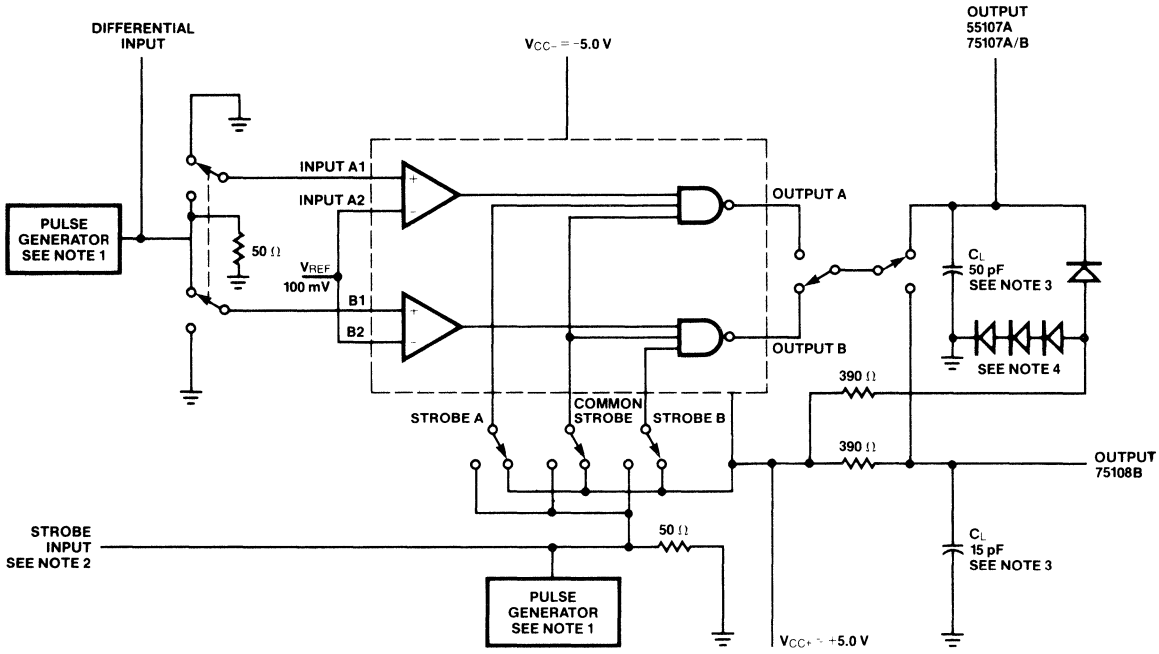
55/75107A, 75107B Propagation Delay Time (Strobe Inputs) vs Ambient Temperature



Voltage Waveforms



AC Test Circuit



Notes

1 The pulse generators have the following characteristics Z_{OUT} = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 μs, PRR = 500 kHz

2 Strobe input pulse is applied to Strobe A when inputs A1-A2 are being tested to common Strobe when inputs A1-A2 or B1-B2 are being tested, and to Strobe B when inputs B1-B2 are being tested.

3 C_L includes probe and jig capacitance

4 All diodes are 1N916

Application

The 55/75107A dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

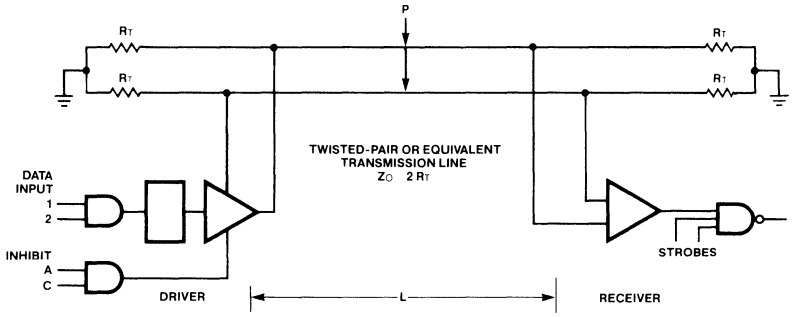
$$V_{DIFF} \simeq 1/2\ I_{OUT(on)} \cdot R_T$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

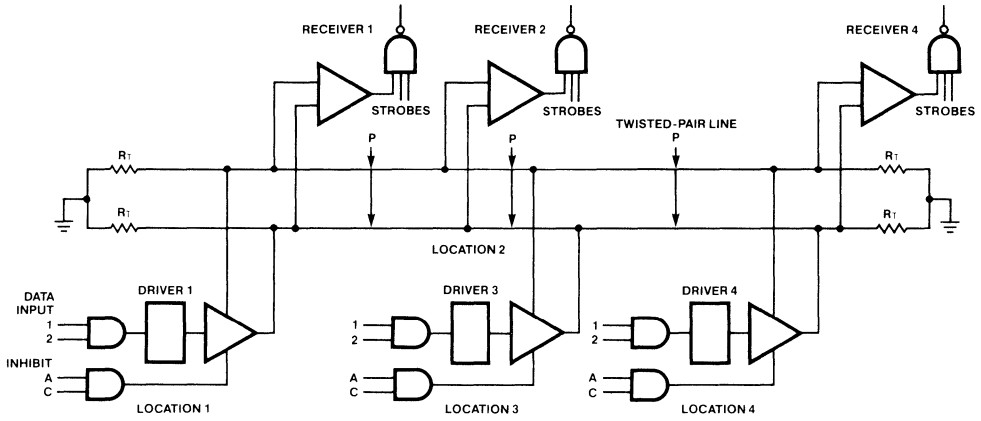
Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \simeq I_{OUT(on)} \cdot R_T$$

Basic Balanced-Line Transmission System



Data-Bus or Party-Line System

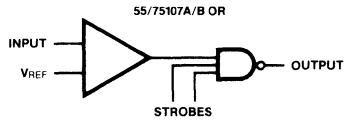


The strobe feature of the receivers and the inhibit feature of the drivers allow the 55/75107A dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. The 55/75107A device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

The 55/75107A dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.

The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3.0 V to +3.0 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

Unbalanced or Single-Line Systems



Precautions in the Use of 55/75107A and 75108B Dual Line Receivers

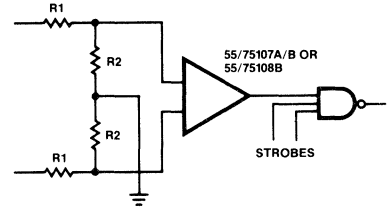
The following precaution should be observed when using or testing 55/75107A line circuits.

When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0 V and +3.0 V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

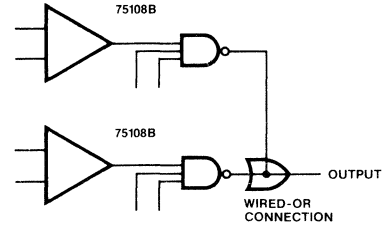
The 55/75107A and 75108B line receivers feature a common-mode input voltage range of ±3.0 V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common-mode range can be extended by the use of external input attenuators. Common-mode input voltages can in this way be reduced to ±3.0 V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

The 75108B line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other 75108B outputs. This allows a level of logic to be implemented without additional logic delay.

Increasing Common-Mode Input Voltage Range of Receiver



75108B Wired-OR Output Connections



FAIRCHILD
A Schlumberger Company

μA55/75110A
Dual Line Drivers

Interface Products

Description

The μA55110A and μA75110A have improved output current regulation with supply voltage and temperature variations. The higher current outputs allow data to be transmitted over longer lines. These drivers offer optimum performance when used with the μA55107A, μA75107A and μA75108B line receivers.

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the two drivers is in the output current specificaiton. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by LOW logic levels on the inhibit inputs.

The inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high; the output impedance of output transistor is biased to cutoff.

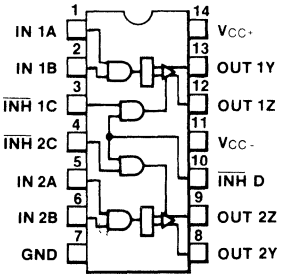
- **NO OUTPUT TRANSIENTS ON POWER-UP OR DOWN**
- **IMPROVED STABILITY OVER SUPPLY VOLTAGE AND TEMPERATURE RANGES**
- **CONSTANT-CURRENT, HIGH-IMPEDANCE OUTPUTS**
- **HIGH SPEED 15 ns**
- **STANDARD SUPPLY VOLTAGES**
- **INHIBITOR AVAILABLE FOR DRIVER SELECTION**
- **HIGH COMMON-MODE OUTPUT VOLTAGE RANGE (−3 V to 10 V)**
- **TTL INPUT COMPATIBILITY**

Function Table

Inputs				Outputs	
Logic		Inhibitor			
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = HIGH, L = LOW, X = Don't Care

Connection Diagram
14-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA55110A	Ceramic DIP	6A	μA55110ADM
μA75110A	Ceramic DIP	6A	μA75110ADC
μA75110A	Molded DIP	9A	μA75110APC

Absolute Maximum Ratings

Over operating temperature range, unless otherwise specified

Supply voltage, V_{CC+} (Note 1)	7 V
Supply voltage, V_{CC-}	−7 V
Input voltage (any input)	5.5 V
Output voltage (any output)	−5 V to 12 V
Continuous total dissipation at T_A = 25°C (Note 2)	
Ceramic DIP	900 mW
Molded DIP	1700 mW
Operating temperature range	
μA55110A	−55°C to 125°C
μA75110A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Pin temperature	
Ceramic DIP Soldering (60 s)	300°C
Molded DIP Soldering (10 s)	260°C

Notes

1 Voltage values are with respect to network ground terminal.

2 For operation above 25°C ambient temperature, derate ceramic DIP at 8 mW/°C and molded DIP at 14 mW/°C

6

Recommended Operating Conditions (Note 3)

Characteristic	55110A			75110A			Unit
	Min	Typ	Max	Min	Typ	Max	
Supply Voltage V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply Voltage V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Positive Common Mode Output Voltage	0		10	0		10	V
Negative Common Mode Output Voltage	0		−3	0		−3	V
Operating Ambient Temperature Range	−55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Ambient Temperature Range (unless otherwise noted)

Symbol	Characteristic		Condition (Note 4)	55110A/75110A			Unit
				Min	Typ (5)	Max	
V_{IH}	Input HIGH voltage			2			V
V_{IL}	Input LOW voltage					0.8	V
V_{IC}	Input clamp voltage		$V_{CC\pm}$ = MIN, I_{IN} = −12 mA		−0.9	−1.5	V
$I_{O(on)}$	On-state output current		$V_{CC\pm}$ = MAX, V_{OUT} = 10 V $V_{CC\pm}$ = MIN, V_{OUT} = −3 V	6.5	12 12	15	mA
$I_{O(off)}$	Off-state output current		$V_{CC\pm}$ = MIN, V_{OUT} = 10 V			100	μA
I_I	Input current at maximum input voltage	A, B or C Inputs	$V_{CC\pm}$ = MAX, V_{IN} = 5.5 V			1	mA
		D input				2	
I_{IH}	Input HIGH Current	A, B or C Inputs	$V_{CC\pm}$ = MAX, V_{IN} = 2.4 V			40	μA
		D Input				80	
I_{IL}	Input LOW Current	A, B or C Inputs	$V_{CC\pm}$ = MAX, V_{IN} = 0.4 V			−3	mA
		D Input				−6	
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled		$V_{CC\pm}$ = MAX, A & B inputs at 0.4 V, C & D inputs at 2 V		23	35	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled				−34	−50	
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited		$V_{CC\pm}$ = MAX, A, B, C, & D inputs at 0.4 V		21		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited				−17		

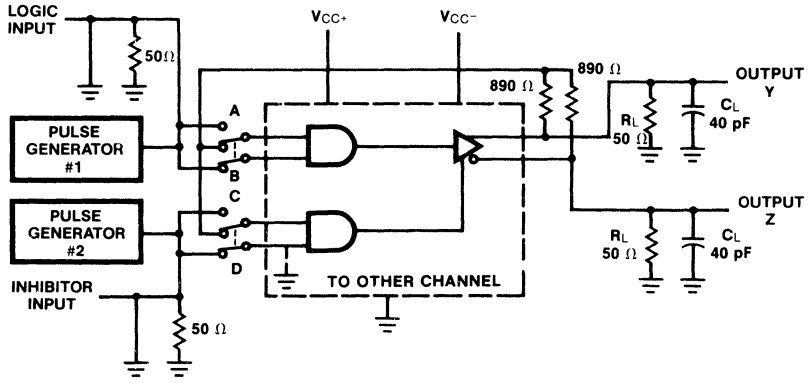
AC Characteristics V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

Symbol	Characteristic	From (Input)	To (Output)	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, LOW to HIGH	A or B	Y or Z	C_L = 40 pF, R_L = 50 Ω See *Figures*		9	15	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					9	15	ns
t_{PLH}	Propagation Delay Time, LOW to HIGH	C or D	Y or Z			16	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					13	25	ns

Notes

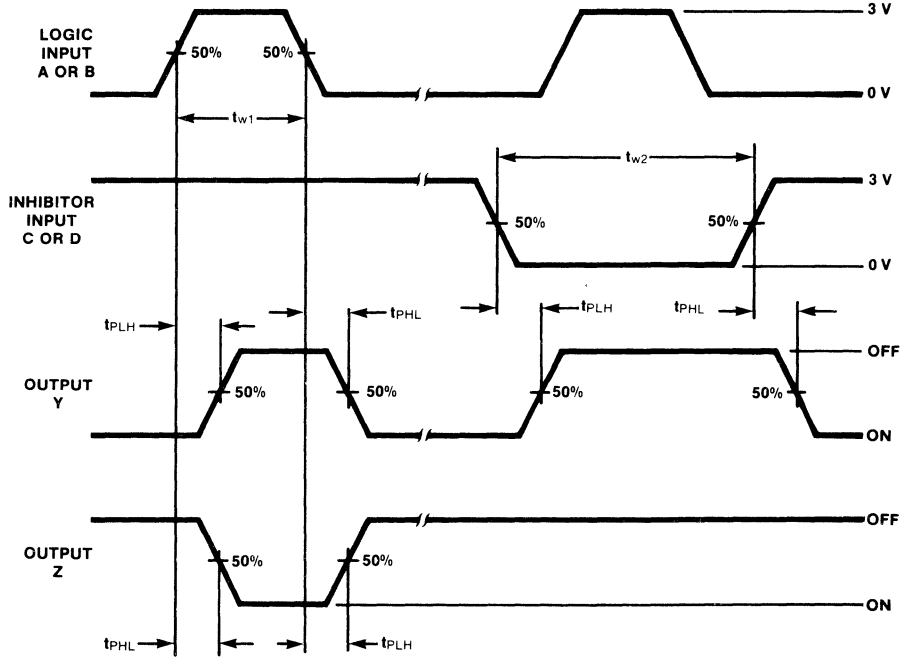
3. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.
4. For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
5. All typical values are V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

Characteristic Measurement Information



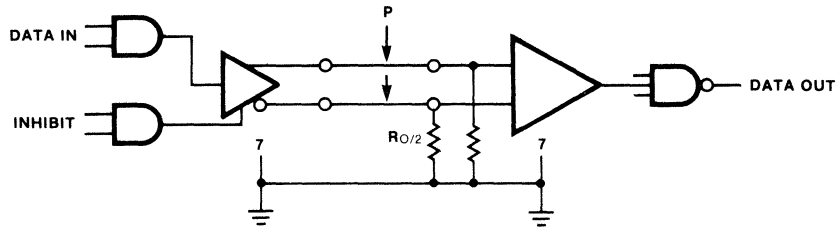
The pulse generators have the following characteristics
Z_{OUT} = 50 Ω, $t_r = t_f$ = 10 ±5 ns, t_{w1} = 500 ns, PRR = 1 MHz,
t_{w2} = 1 ms, PRR = 500 kHz
C_L includes probe and jig capacitance
For simplicity, only one channel and the inhibitor connections are shown

AC Test Circuit and Waveforms

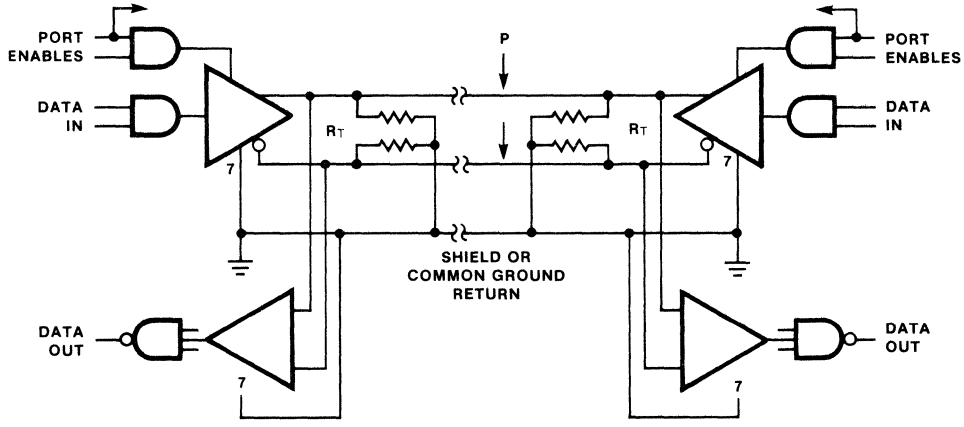


Typical Applications

Simplex Operation



Half-Duplex Operation



Notes

1 All drivers are μA75110A or μA55110A. Receivers are μA75107A or μA75108B. Twisted-pair or coaxial transmission line should be used for minimum noise and cross talk.

2 When only one driver in a package is being used, the outputs of the other driver should either be grounded or inhibited to reduce power dissipation.

FAIRCHILD
A Schlumberger Company

μA75150
Dual Line Driver

Interface Products

Description

The 75150 is a monolithic Dual Line Driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12 V and −12 V power supplies.

- **WITHSTANDS SUSTAINED OUTPUT SHORT-CIRCUIT TO ANY LOW-IMPEDANCE VOLTAGE BETWEEN −25 V AND +25 V**
- **2.0 μs MAX TRANSITION TIME THROUGH THE +3.0 V TO −3.0 V TRANSITION REGION UNDER FULL 2500 pF LOAD**
- **INPUTS COMPATIBLE WITH MOST TTL AND DTL FAMILIES**
- **COMMON STROBE INPUT**
- **INVERTING OUTPUT**
- **SLEW RATE CAN BE CONTROLLED WITH AN EXTERNAL CAPACITOR AT THE OUTPUT**
- **STANDARD SUPPLY VOLTAGES ± 12 V**

Absolute Maximum Ratings over operating ambient temperature range, unless otherwise noted.

Supply Voltage V_{CC+} (See Note 1)	15 V
Supply Voltage V_{CC-} (See Note 1)	−15 V
Input Voltage (See Note)	15 V
Applied Output Voltage (See Note)	±25 V
Operating Temperature	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Pin Temperature Molded, (Soldering, 10 s)	260°C

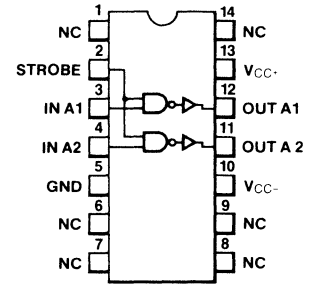
Notes

1 Voltage values are with respect to network ground terminal.

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply Voltage V_{CC+}	10.8	12	13.2	V
Supply Voltage V_{CC-}	−10.8	−12	−13.2	V
Input Voltage, V_I	0		5.5	V
Applied Output Voltage, V_O			±15	V
Operating Ambient Temperature, T_A	0		70	°C

Connection Diagram
14-Pin DIP

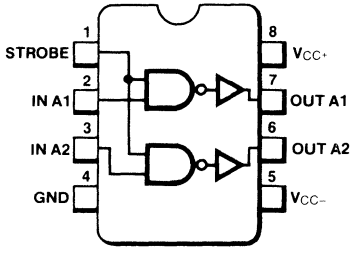


(Top View)

Order Information

Type	Package	Code	Part No.
μA75150	Molded DIP	9A	μA75150PC

Connection Diagram
8-Pin DIP



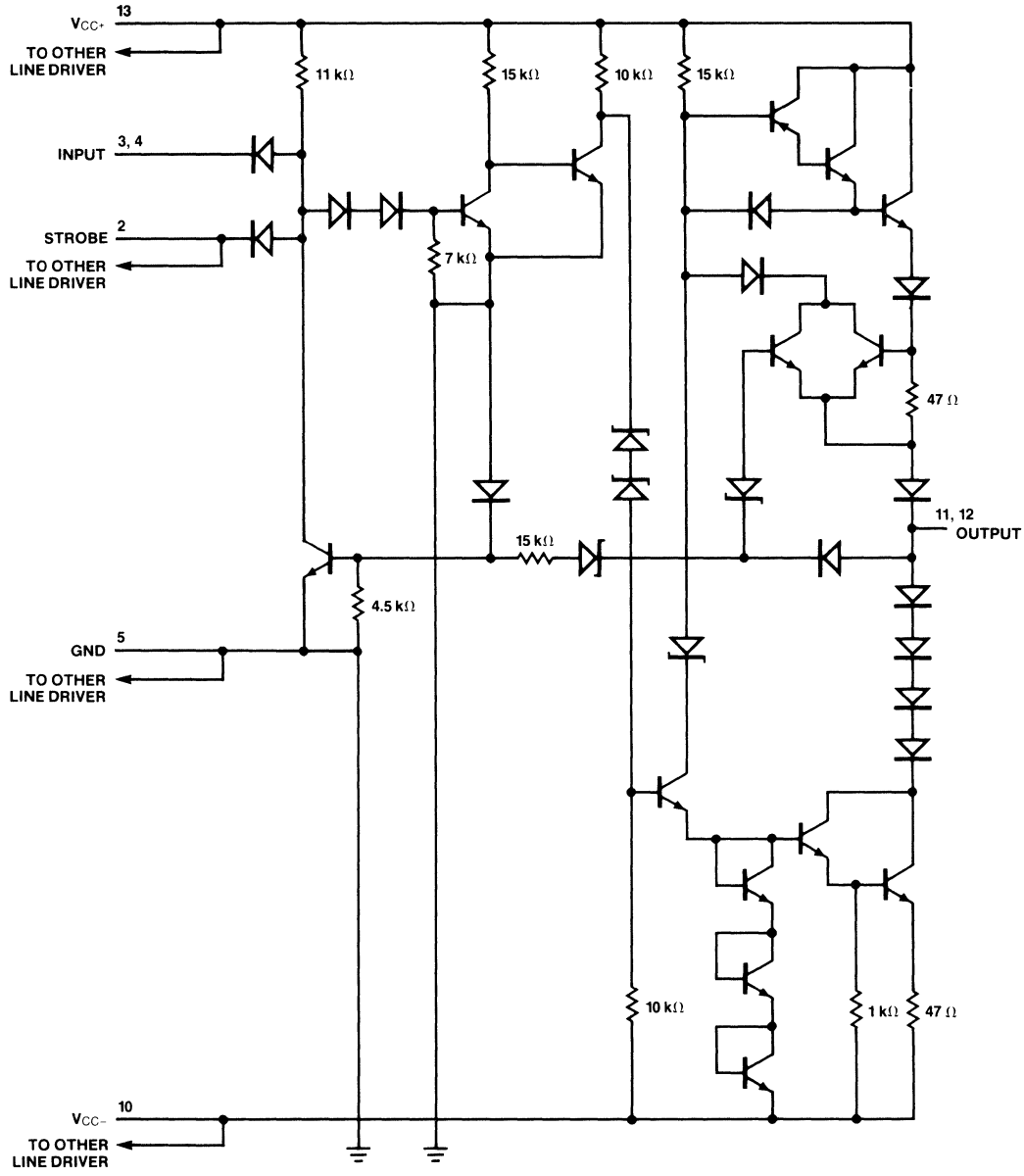
(Top View)

Order Information

Type	Package	Code	Part No.
μA75150	Molded DIP	9T	μA75150TC

6

Schematic (each line driver)



Component values shown are nominal
Pins 1, 6, 7, 8, 9, and 14 = not connected
Pin connections are for 14-lead DIP

DC Characteristics T_A = 0 to 70°C, unless otherwise specified (Note 2)

Symbol	Characteristic	Test Figure	Condition		Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage	1			2.0			V
V_{IL}	Input LOW Voltage	2					0.8	V
V_{OH}	Output HIGH Voltage	2	V_{CC+} = 10.8 V, V_{CC-} = −13.2 V, V_{IL} = 0.8 V, R_L = 3 kΩ to 7 kΩ		5.0	8.0		V
V_{OL}	Output LOW Voltage	1	V_{CC+} = 10.8 V, V_{CC-} = −10.8 V, V_{IH} = 2 V, R_L = 3 kΩ to 7 kΩ			−8.0	−5.0	V
I_{IH}	Input HIGH Current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 2.4 V	Data Input		1.0	10	μA
				Strobe Input		2.0	20	
I_{IL}	Input LOW Current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0.4	Data Input		−1.0	−1.6	mA
				Strobe Input		−2.0	−3.2	
I_{OS}	Short-Circuit Output Current	4	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	V_O = 25 V		2.0		mA
				V_O = −25 V		−3.0		
				V_O = 0 V, V_I = 3 V		15		
				V_O = 0 V, V_I = 0 V		−15		
I_{CCH+}	Supply Current from V_{CC+}, Output High	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 3 V, R_L = 3 kΩ,			10	22	mA
I_{CCH-}	Supply Current from V_{CC-}, Output HIGH		T_A = 25°C			−1.0	−10	mA
I_{CCL+}	Supply Current from V_{CC+}, Output LOW	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 3 V, R_L = 3 kΩ,			8.0	17	mA
I_{CCL-}	Supply Current from V_{CC-}, Output LOW		T_A = 25°C			−9.0	−20	mA

AC Characteristics V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

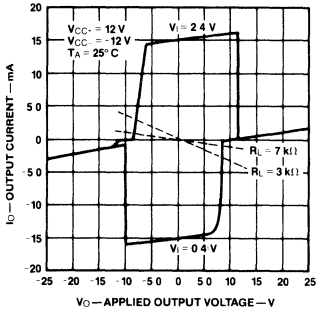
Symbol	Characteristic	Test Figure	Condition	Min	Typ	Max	Unit
t_{TLH}	Transition Time, Output LOW to HIGH	6	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ	0.2	1.4	2.0	μs
t_{THL}	Transition Time, Output HIGH to LOW			0.2	1.5	2.0	μs
t_{TLH}	Transition Time, Output LOW to HIGH	6	C_L = 15 pF, R_L = 7 kΩ		40		ns
t_{THL}	Transition Time, Output HIGH to LOW				20		ns
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	6	C_L = 15 pF, R_L = 7 kΩ		60		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				45		ns

Notes

2 The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more negative voltage. All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

Typical Performance Curve

Typical Output Current vs Applied Output Voltage



Test Circuits

Fig. 1 V_{IH}, V_{OL}

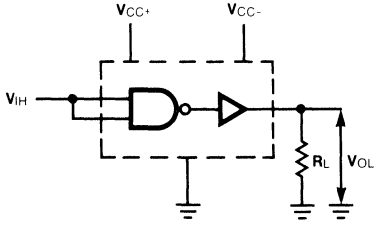
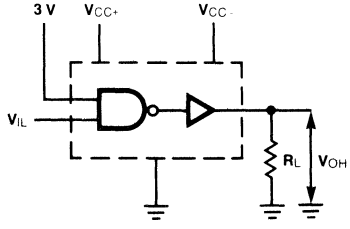
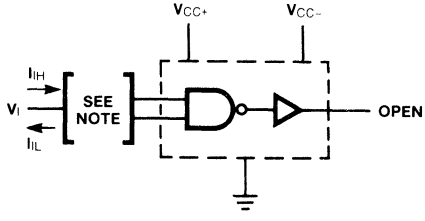


Fig. 2 V_{IL}, V_{OH}



Each input is tested separately

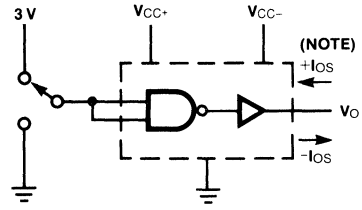
Fig. 3 I_{IH}, I_{IL}



Note

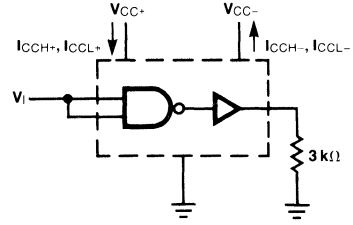
When testing I_{IH}, the other input is at 3 V, when testing I_{IL}, the other input is open

Fig. 4 I_{OS}



I_{OS} is tested for both input conditions at each of the specified output conditions.

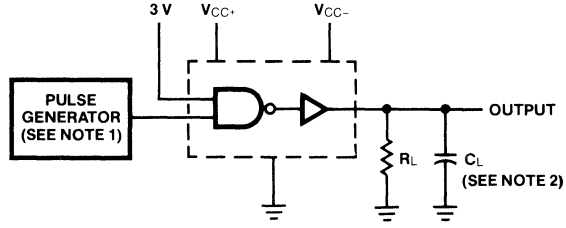
Fig. 5 I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}



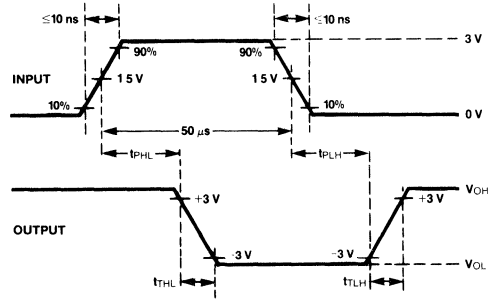
*Arrows indicate actual direction of current flow. Current into a terminal is a positive value

Fig. 6 Switching Characteristics

Test Circuit



Voltage Waveforms



Notes

1. The pulse generator has the following characteristics duty cycle ≤ 50%, $Z_{OUT} \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance

FAIRCHILD
A Schlumberger Company

μA75154
RS-232C
Quad Line Receiver

Interface Products

Description

The 75154 is a monolithic Quad Line Receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5 V supply; however, a built-in option allows operation from a 12 V supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

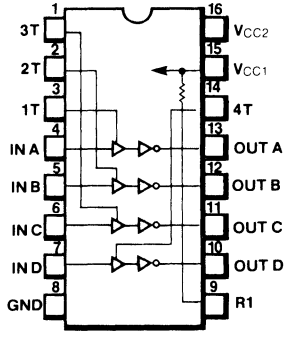
In normal operation, the threshold control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode of operation, if the input voltage goes to zero, the output voltage will remain LOW or HIGH as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go HIGH regardless of the previous input condition.

The 75154 is characterized for operation from 0° C to 70° C.

- **INPUT RESISTANCE—3 kΩ TO 7 kΩ OVER FULL RS-232C VOLTAGE RANGE**
- **INPUT THRESHOLD ADJUSTABLE TO MEET FAIL-SAFE REQUIREMENTS WITHOUT USING EXTERNAL COMPONENTS**
- **BUILT-IN HYSTERESIS FOR INCREASED NOISE IMMUNITY**
- **INVERTING OUTPUT COMPATIBLE WITH DTL OR TTL**
- **OUTPUT WITH ACTIVE PULL-UP FOR SYMMETRICAL SWITCHING SPEEDS**
- **STANDARD SUPPLY VOLTAGES—5 V OR 12 V**

Connection Diagram
16-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA75154	Ceramic DIP	6B	μA75154DC
μA75154	Molded DIP	9B	μA75154PC

Absolute Maximum Ratings

Normal Supply Voltage (Pin 15), V_{CC1} (Note 1)	7 V
Alternate Supply Voltage (Pin 16), V_{CC2} (Note 1)	14 V
Input Voltage (Note 1)	±25 V
Continuous Total Power Dissipation (Note 2)	800 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Pin Temperatures	
Molded DIP (Soldering, 10 s)	260°C
Ceramic DIP (Soldering, 60 s)	300°C

Recommended Operating Conditions

	Min	Typ	Max	Unit
Normal Supply Voltage (Pin 15), V_{CC1}	4.5	5	5.5	V
Alternate Supply Voltage (Pin 16), V_{CC2}	10.8	12	13.2	V
Input Voltage			±15	V
Normalized Fan Out from Each Output, N			10	
Operating Ambient Temperature Range	0		70	°C

Notes

1. Voltage values are with respect to the network ground terminal.
2. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C.

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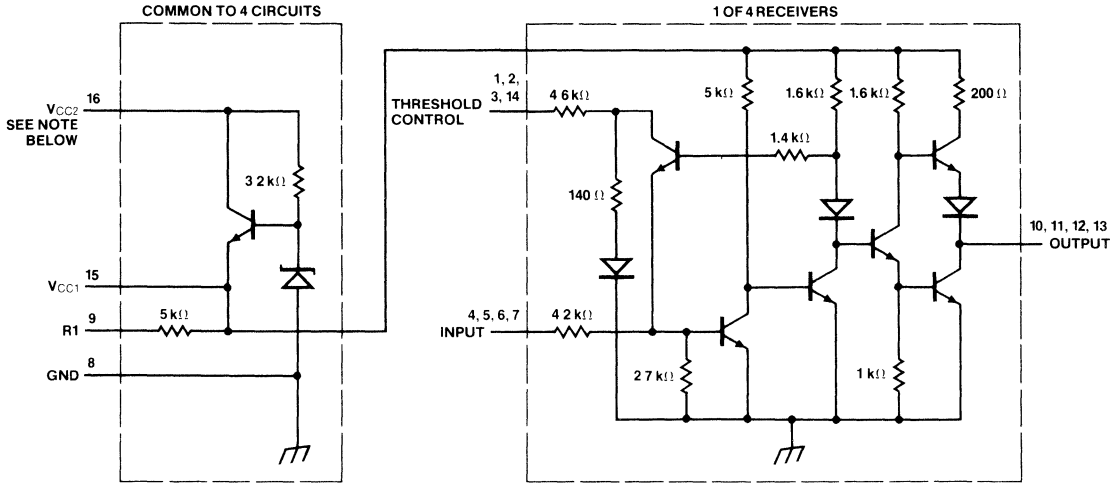
Equivalent Circuit



Notes

Component values shown are normal.

When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

DC Characteristics T_A = 0 to 70°C unless otherwise specified (Note 5)

Symbol	Characteristic		Test Figure	Condition	Min	Typ(4)	Max	Unit
V_{IH}	Input HIGH Voltage		1		3.0			V
V_{IL}	Input LOW Voltage		1				−3.0	V
V_{T+}	Positive-Going Threshold Voltage	Normal Operation	1		0.8	2.2	3.0	V
		Fail-Safe Operation			0.8	2.2	3.0	
V_{T-}	Negative-Going Threshold Voltage	Normal Operation	1		−3.0	−1.1	0	V
		Fail-Safe Operation			0.8	1.4	3.0	
$V_{T+} - V_{T-}$	Hysteresis	Normal Operation	1		0.8	3.3	6.0	V
		Fail-Safe Operation			0	0.8	2.2	
V_{OH}	Output HIGH Voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Output LOW Voltage		1	I_{OL} = 16 mA		0.23	0.4	V
R_I	Input Resistance		2	ΔV_I = −25 V to −14 V	3.0	5.0	7.0	k Ω
				ΔV_I = −14 V to −3 V	3.0	5.0	7.0	
				ΔV_I = −3 V to 3 V	3.0	6.0		
				ΔV_I = 3 V to 14 V	3.0	5.0	7.0	
				ΔV_I = 14 V to 25 V	3.0	5.0	7.0	
$V_{I\ (open)}$	Open-Circuit Input Voltage		3	I_I = 0	0	0.2	2.0	V
I_{OS}	Short-Circuit Output Current (Note 3)		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply Current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply Current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

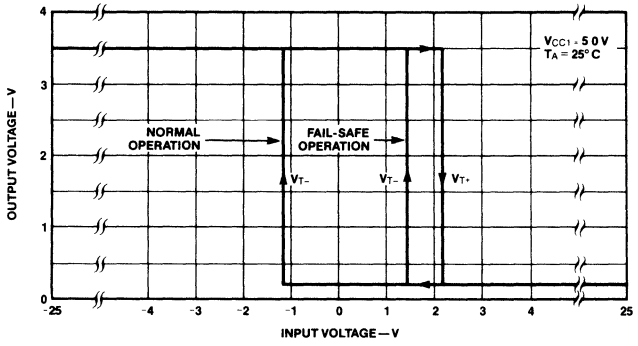
Notes on following pages.

AC Characteristics V_{CC1} = 5.0 V, T_A = 25°C, n = 10

Symbol	Characteristic	Test Figure	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, LOW-to-HIGH	6	C_L = 50 pF, R_L = 390 Ω		22		ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW				20		ns
t_{TLH}	Transition Time, LOW-to-HIGH				9.0		ns
t_{THL}	Transition Time, HIGH-to-LOW				6.0		ns

Typical Characteristics

Output Voltage Versus Input Voltage



Note
For normal operation, the threshold controls are connected to V_{CC1}, pin 15. For fail-safe operation, the threshold controls are open

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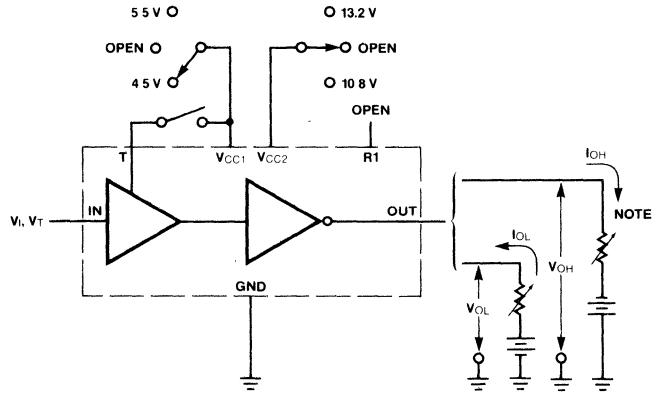
Notes
3. Not more than one output should be shorted at a time.
4. All typical values are at V_{CC1} = 5 V, T_A = 25°C.
5. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3 V is the maximum, the minimum limit is a more-negative voltage.

DC Test Circuits

Fig. 1 V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}



Note
Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

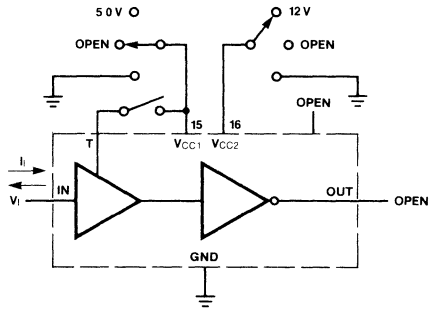
Test Table

Test	Measure	In	T	Out	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open-circuit input	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
(fail safe)	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min,	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note 6	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	Note 6	Pin 15	I_{OH}	T	13.2 V
V_{IL} max,	V_{OH}	−3 V	Pin 15	I_{OH}	5.5 V and T	Open
V_{T-} min (normal)	V_{OH}	−3 V	Pin 15	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max,	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max	V_{OL}	3 V	Pin 15	I_{OL}	4.5 V and T	Open
(normal)	V_{OL}	3 V	Pin 15	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note 7	Pin 15	I_{OL}	5.5 V and T	Open
	V_{OL}	Note 7	Pin 15	I_{OL}	T	13.2 V

Notes
6. Momentarily apply −5 V, then 0.8 V.
7. Momentarily apply 5 V, then ground.

DC Test Circuits (Cont.)

Fig. 2 R_I

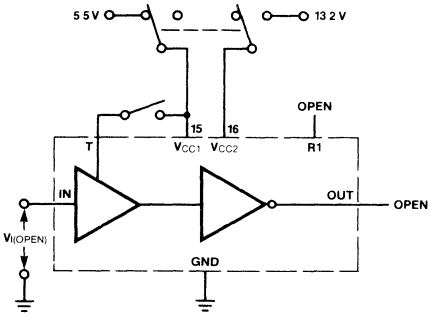


$$R_I = \frac{\Delta V_I}{\Delta I_I}$$

Test Table

T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5 V	Open
Open	GND	Open
Open	Open	Open
Pin 15	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Pin 15	T	12 V
Pin 15	T	GND
Pin 15	T	Open

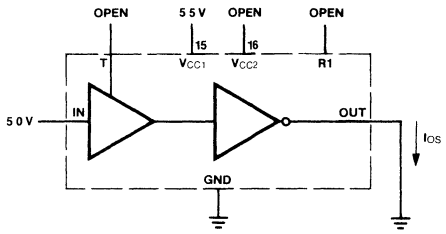
Fig. 3 $V_{I(open)}$



Test Table

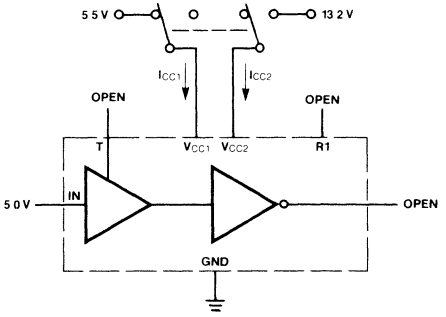
T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5.5 V	Open
Pin 15	5.5 V	Open
Open	Open	13.2 V
Pin 15	T	13.2 V

Fig. 4 I_{OS}



Note
Each output is tested separately

Fig. 5 I_{CC}

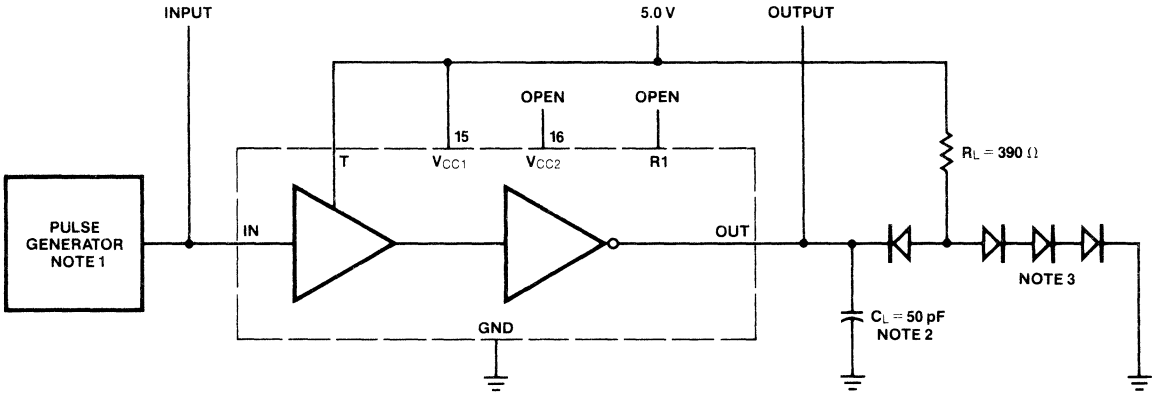


Notes
All four line receivers are tested simultaneously.
Arrows indicate actual direction of current flow. Current into a terminal is a positive value

6

AC Characteristics

Test Circuit



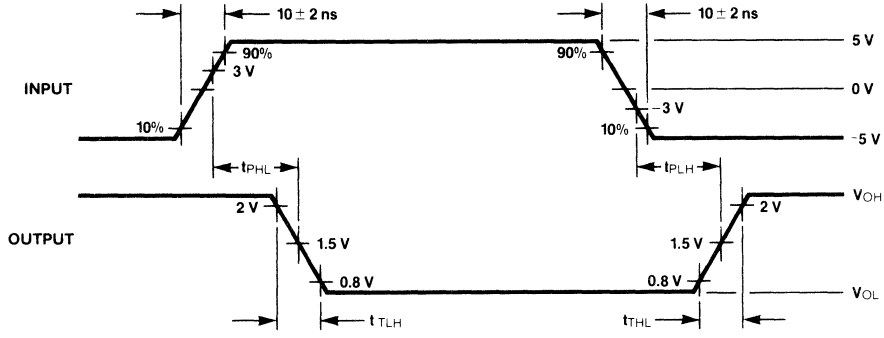
Notes

1 The pulse generator has the following characteristics:
Z_{OUT} = 50 Ω, t_W = 200 ns, duty cycle ≤ 20%

2 C_L includes probe and jig capacitance.

3 All diodes are 1N3064.

Voltage Waveforms



FAIRCHILD

A Schlumberger Company

μA9640/26S10 Quad General-Purpose Bus Transceiver

Interface Products

Description

The μA9640 is a High-Speed Quad Bus Transceiver. Each driver output, which is capable of sinking 100 mA at 0.8 V, is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads. The bus output is capable of driving lines having 100 Ω impedance.

The line can be terminated at both ends and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 V.

The μA9640 features advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

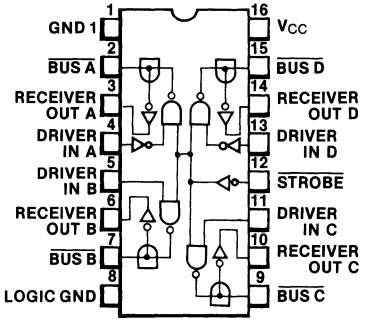
The μA9640 is a pin for pin replacement for the AM26S10.

- **INPUT TO BUS IS INVERTING**
- **QUAD HIGH-SPEED OPEN COLLECTOR BUS TRANSCEIVERS**
- **DRIVER OUTPUTS CAN SINK 100 mA AT 0.8 V MAXIMUM**
- **ADVANCED SCHOTTKY PROCESSING**
- **PNP INPUTS TO REDUCE INPUT LOADING**

Absolute Maximum Ratings

Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ Max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, into Bus	200 mA
Output Current, into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5.0 mA
Operating Temperature	
μA9640DM	−55°C to +125°C
μA9640DC/PC	0°C to +70°C
Storage Temperature	−65°C to +150°C
Pin Temperatures	
Molded DIP (Soldering 10 s)	260°C
Ceramic DIP (Soldering 60 s)	300°C

Connection Diagram 16-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA9640	Ceramic DIP	6B	μA9640DM
μA9640	Ceramic DIP	6B	μA9640DC
μA9640	Molded DIP	9B	μA9640PC

Truth Table

Inputs		Outputs	
$\overline{\text{Strobe}}$	Driver IN_{A-D}	$\overline{Bus}_{A-D}$	Receiver Out_{A-D}
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes control by another bus transceiver)

6

Recommended Operating Conditions

Characteristic	Military (4)			Commercial (5)			Unit
	Min	Typ	Max	Min	Typ	Max	
Positive Supply Voltage	4.50	5.0	5.5	4.75	5.0	5.25	V
Operating Ambient Temperature – T_A	−55	+25	+125	0	+25	+70	°C

DC Characteristics Over operating temperature & voltage range, unless otherwise specified.

Symbol	Characteristic	Condition (Note 1)		Min	Typ (2)	Max	Unit
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN, I_{OH} = −1.0 mA, V_{IN} = V_{IL} or V_{IH}	Mil (4)	2.5	3.4		V
			Comm (5)	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN, I_{OL} = 20 mA, V_{IN} = V_{IL} or V_{IH}				0.5	V
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed Input Logic HIGH for all inputs		2.0			V
V_{IL}	Input LOW Level (Except Bus)	Guaranteed Input Logic LOW for all inputs				0.8	V
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4 V	ENABLE			−0.36	mA
			DATA			−0.54	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7 V	ENABLE			20	μA
			DATA			30	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5 V				100	μA
I_{SC}	Output Short-Circuit Current (Except Bus)	V_{CC} = MAX (Note 3)	Mil (4)	−20		−55	mA
			Comm (5)	−18		−60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX, Enable = GND			45	70	mA

AC Characteristics T_A = +25°C, V_{CC} = 5.0 V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{pLH}, t_{pHL}	Data Input to Bus	R_B = 50 Ω, C_B = 50 pF (Note 6)		10	15	ns
t_{pLH}, t_{pHL}	Enable Input to Bus			14	18	ns
t_{pHL}, t_{pHL}	Bus to Receiver Out	R_B = 50 Ω, R_L = 280 Ω, C_B = 50 pF, C_L = 15 pF (Note 6)		10	15	ns
t_r	Bus	R_B = 50 Ω, C_B = 50 pF (Note 6)	4.0	10		ns
t_f	Bus		2.0	4.0		ns

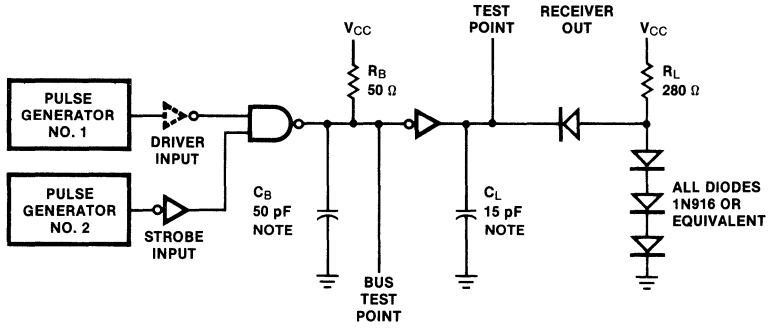
Notes

1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
4. Military temperature range, ceramic DIP
5. Commercial temperature range, ceramic or molded DIP
6. Includes probe and jig capacitance.

Bus Input/Output Characteristics

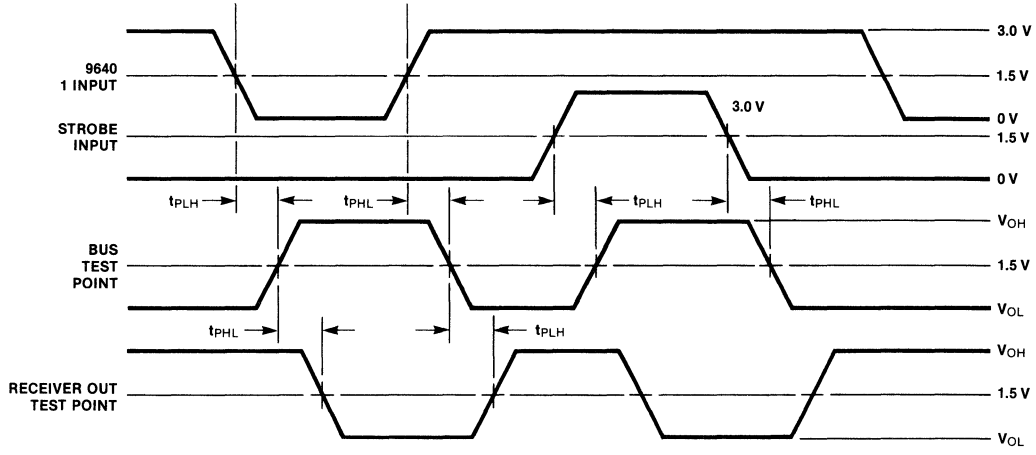
Symbol	Characteristic	Condition (Note 1)			Min	Typ (2)	Max	Unit
V_{OL}	Output LOW Voltage	V_{CC} = Min	Mil (Note 4)	I_{OL} = 40 mA		0.33	0.5	V
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
			Comm (Note 5)	I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
I_O	Bus Leakage Current (Power On)	V_{CC} = Max		V_O = 0.8 V			−50	μA
			Mil (Note 4)	V_O = 4.5 V			200	
			Comm (Note 5)	V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5 V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4 V, V_{CC} = Max		DM		2.0	2.4	V
				DC, PC		2.0	2.25	
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4 V, V_{CC} = Min		DM	1.6	2.0		V
				DC, PC	1.75	2.0		

Fig. 1 AC Test Circuit



Note
Includes probe and jig capacitance.

Fig. 2 Waveforms



FAIRCHILD

A Schlumberger Company

μA3448A Quad Instrumentation Bus (GPIB) Transceiver

Interface Products

Description

μA3448A is a 3-state bidirectional Quad Bus Transceiver operating from a single +5 V supply. It interfaces between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1975), often referred to as GPIB. The required bus termination is internally provided.

The receivers have built-in input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- **3-STATE OUTPUTS**
- **SCHOTTKY TECHNOLOGY**
- **HIGH IMPEDANCE INPUTS**
- **RECEIVER HYSTERESIS—600 mV**
- **SINGLE +5 V SUPPLY**
- **POWER UP/POWER DOWN PROTECTION**
- **NO BUS LOADING WHEN POWER IS REMOVED**

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

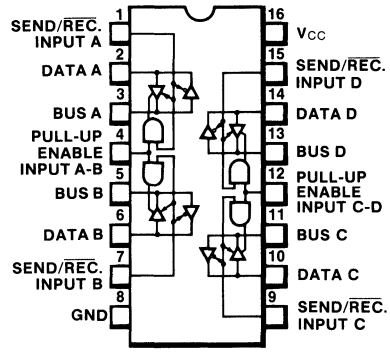
Power Supply Voltage	7.0 V
Input Voltage	5.5 V
Driver Output Current	150 mA
Junction Temperature	150°C
Operating Ambient Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Pin Temperatures	
Molded DIP (Soldering, 10 s)	260°C
Ceramic DIP (Soldering, 60 s)	300°C

Truth Table

Send/$\overline{\text{Rec.}}$	Enable	Info. Flow	Comments
0	X	Bus→Data	—
1	1	Data→Bus	Active Pull-Up
1	0	Data→Bus	Open Collector

X = Don't Care

Connection Diagram
16-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA3448A	Molded DIP	9B	μA3448APC
μA3448A	Ceramic DIP	7B	μA3448ADC

DC Characteristics Unless otherwise noted, 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{BUS} $V_{IC(BUS)}$	Bus Voltage	Bus Pin Open, $V_{IN(S/R)}$ = 0.8 V I_{BUS} = −12 mA	2.75		3.7 −1.5	V V
I_{BUS}	Bus Current	5.0 V ≤ V_{BUS} ≤ 5.5 V V_{BUS} = 0.5 V V_{CC} = 0 V, 0 V ≤ V_{BUS} ≤ 2.75 V	0.7 −1.3		2.5 −3.2 +0.04	mA mA mA
	Receiver Input Hysteresis	$V_{IN(S/R)}$ = 0.8 V	400	600		mV
$V_{ILH(R)}$ $V_{IHL(R)}$	Receiver Input Threshold	$V_{IN(S/R)}$ = 0.8 V, LOW to HIGH $V_{IN(S/R)}$ = 0.8 V, HIGH to LOW	 0.8	1.6 1.0	1.8	V V
$V_{OH(R)}$	Receiver Output HIGH Voltage	$V_{IN(S/R)}$ = 0.8 V, $I_{OH(R)}$ = −800 μA V_{BUS} = 2.0 V	2.7			V
$V_{OL(R)}$	Receiver Output LOW Voltage	$V_{IN(S/R)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA V_{BUS} = 0.8 V			0.5	V
$I_{OS(R)}$	Receiver Output Short-Circuit Current	$V_{IN(S/R)}$ = 0.8 V, V_{BUS} = 2.0 V	−15		−75	mA
$V_{IH(D)}$	Driver Input HIGH Voltage	$V_{IN(S/R)}$ = 2.0 V	2.0			V
$V_{IL(D)}$	Driver Input LOW Voltage	$V_{IN(S/R)}$ = 2.0 V			0.8	V
$I_{IN(D)}$ $I_{IB(D)}$	Driver Input Current Data Pins	$V_{IN(S/R)}$ = $V_{IN(E)}$ = 2.0 V 0.5 V ≤ $V_{IN(D)}$ ≤ 2.7 V $V_{IN(D)}$ = 5.5 V	200		40 200	μA A
$I_{IN(S/R)}$ $I_{IB(S/R)}$	Input Current Send/Receive	0.5 V ≤ $V_{IN(S/R)}$ ≤ 2.7 V $V_{IN(S/R)}$ = 5.5 V	−100		20 100	μA μA
$I_{IN(E)}$ $I_{IB(E)}$	Input Current Enable	0.5 V ≤ $V_{IN(E)}$ ≤ 2.7 V $V_{IN(E)}$ = 5.5 V	−200		20 100	μA μA
$V_{IC(D)}$	Driver Input Clamp Voltage	$V_{IN(S/R)}$ = 2.0 V, $I_{IC(D)}$ = −18 mA			−1.5	V
$V_{OH(D)}$	Driver Output HIGH Voltage	$V_{IN(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V $V_{IH(E)}$ = 2.0 V, I_{OH} = −5.2 mA	2.5			V
$V_{OL(D)}$	Driver Output LOW Voltage (Note)	$V_{IN(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA			0.5	V
$I_{OS(D)}$	Output Short-Circuit Current	$V_{IN(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V	−30		−120	V
I_{CCL} I_{CCH}	Power Supply Current	Listening Mode, All Receivers On Talking Mode, All Drivers On		63 106	85 125	mA

Note
A modification of the IEEE 488-1975 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

AC Characteristics V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$t_{PLH(D)}$ $t_{PHL(D)}$	Propagation Delay of Driver	Output LOW to HIGH Output HIGH to LOW		10 11	15 17	ns ns
$t_{PLH(R)}$ $t_{PHL(R)}$	Propagation Delay of Receiver	Output LOW to HIGH Output HIGH to LOW		20 16	25 23	ns ns

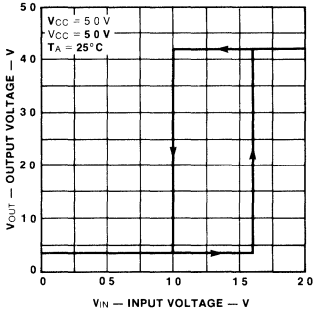
6

AC Characteristics (Cont.) V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted

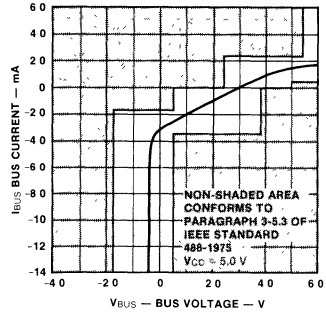
Symbol	Characteristic	Min	Typ	Max	Unit
	Propagation Delay Time—Send/Receiver to Data				
$t_{PHZ(R)}$	Logic HIGH to Third State			30	ns
$t_{PZH(R)}$	Third State to Logic HIGH			30	ns
$t_{PLZ(R)}$	Logic LOW to Third State			30	ns
$t_{PZL(R)}$	Third State to Logic LOW			30	ns
	Propagation Delay Time—Send/Receiver to Bus				
$t_{PHZ(D)}$	Logic HIGH to Third State			30	ns
$t_{PZH(D)}$	Third State to Logic HIGH			30	ns
$t_{PLZ(D)}$	Logic LOW to Third State			30	ns
$t_{PZL(D)}$	Third State to Logic LOW			30	ns
	Turn-On Time—Enable to Bus				
$t_{POFF(E)}$	Pull-Up Enable to Open Collector			30	ns
$t_{PON(E)}$	Open Collector to Pull-Up Enable			20	ns

Typical Performance Curves

Typical Receiver Hysteresis Characteristics

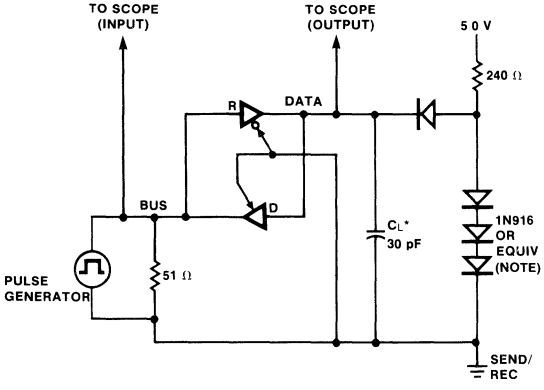


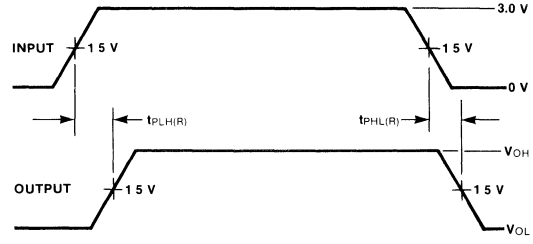
Typical Bus Load Line



AC Test Circuits and Waveforms

Bus Input to Data Output (Receiver)

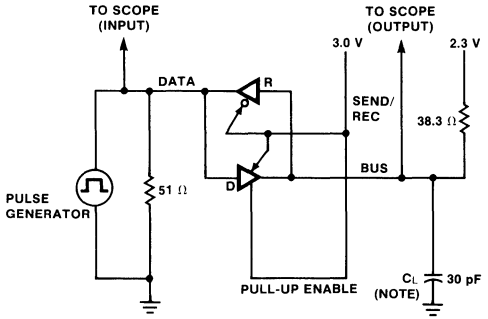




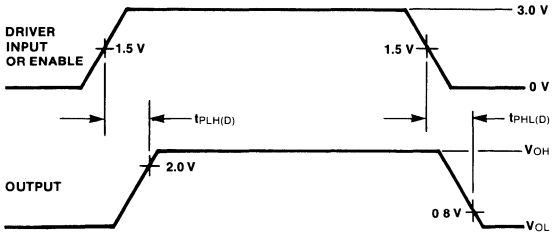
f = 1.0 MHz
$t_{TLH} = t_{THL} \leq 5.0$ ns (10%-90%)
Duty Cycle = 50%
*Includes jig and probe capacitance

AC Test Circuits and Waveforms (Cont.)

Data Input to Bus Output (Driver)

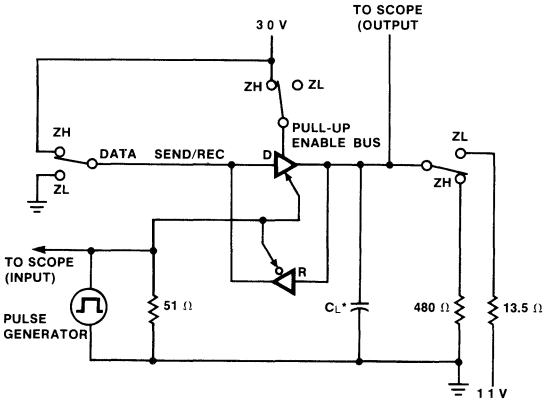


*Includes jig and probe capacitance

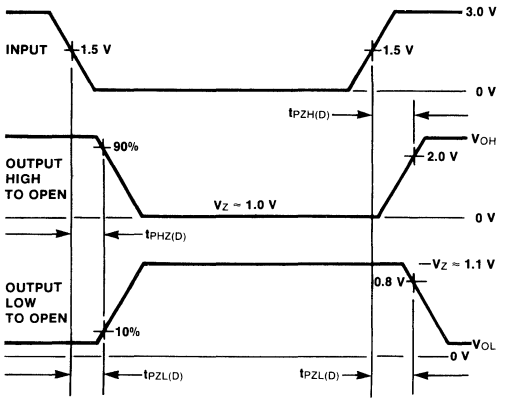


f = 1.0 MHz
$t_{TLH} = t_{THL} \leq 5.0$ ns (10%-90%)
Duty Cycle = 50%

Send/Receive Input to Bus Output (Driver)



C_L = 1 5 pF (Includes jig and probe capacitance)



f = 1.0 MHz
$t_{TLH} = t_{THL} \leq 5.0$ ns (10%-90%)
Duty Cycle = 50%

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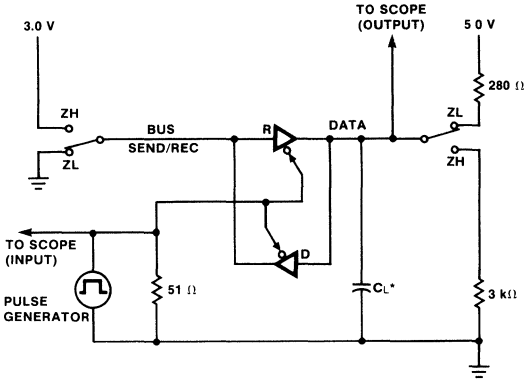
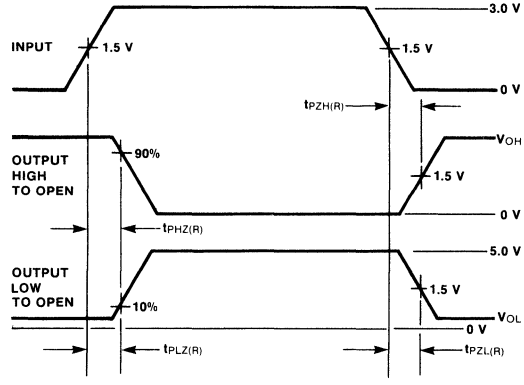
AC Test Circuits and Waveforms (Cont.)

Send/Receive Input to Data Output (Receiver)

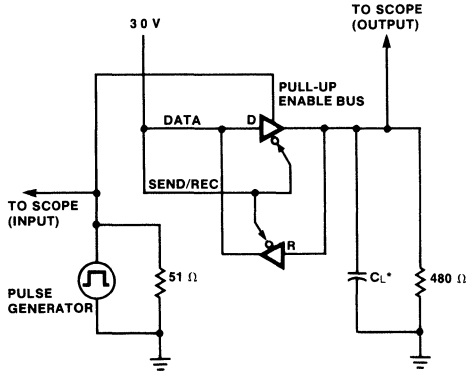


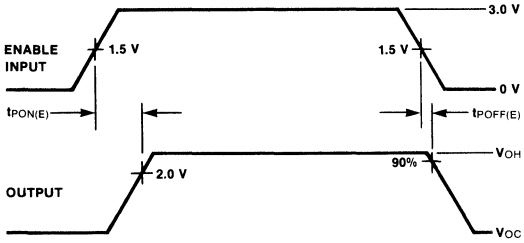


C_L = 1 5 pF (Includes jig and probe capacitance)

f = 1.0 MHz
$t_{TLH} = t_{THL} \leq 5.0$ ns (10%-90%)
Duty Cycle = 50%

Enable Input to Bus Output (Driver)

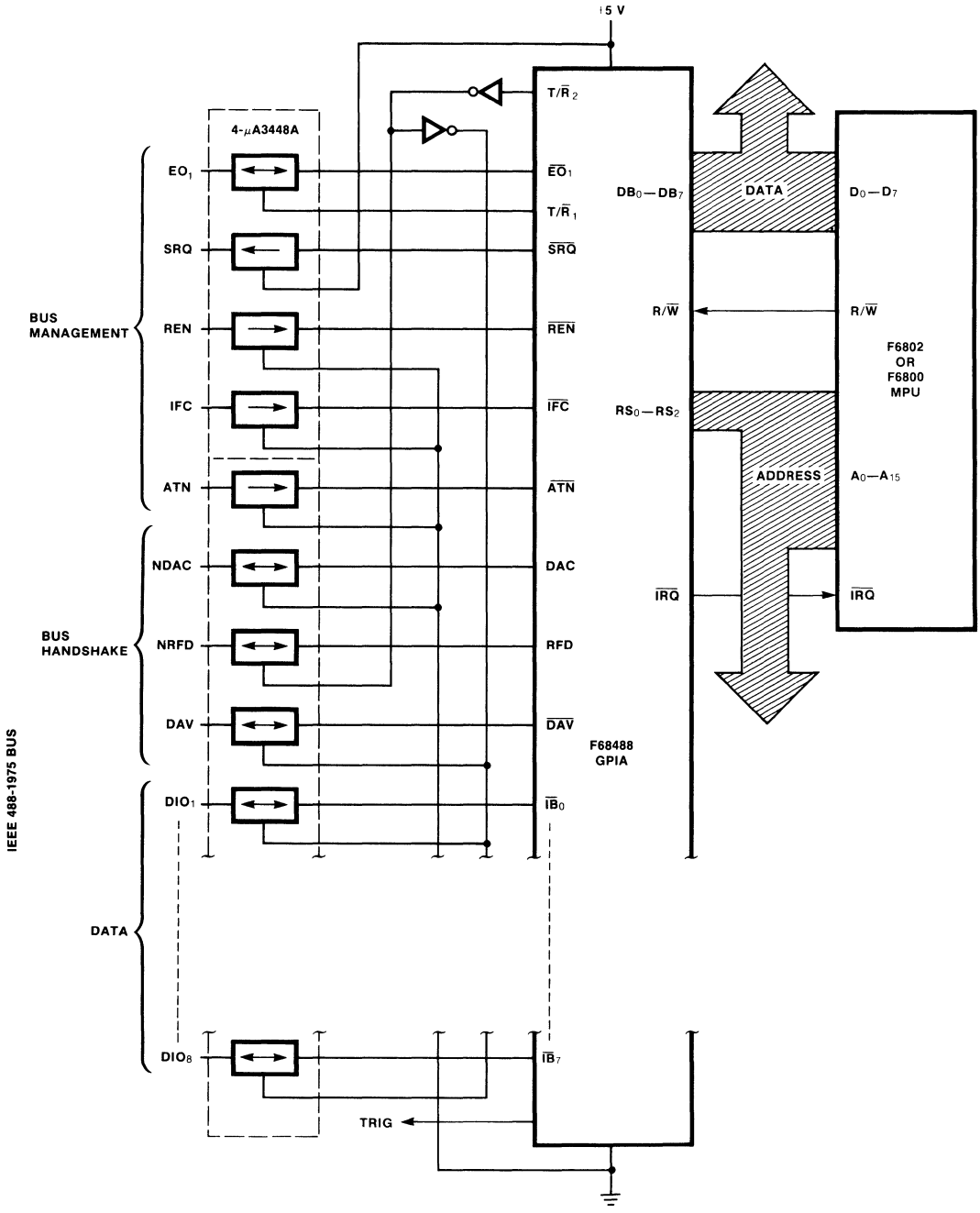




C_L = 1 5 pF (Includes jig and probe capacitance)

f = 1.0 MHz
$t_{TLH} = t_{THL} \leq 5.0$ ns (10%-90%)
Duty Cycle = 50%

Simple System Configuration



Notes

1. Although the μA3448A transceivers are non-inverting, the 488-1975 bus callouts appear inverted with respect to the F68488 pin designations. This is because the 488-1975 Standard is defined for negative logic, while all F6800 MPU components make use of positive logic format.
2. Unless proper considerations are provided, it is recommended that the pull-up enable pins on the μA3448As be grounded, selecting the open-collector mode.

FAIRCHILD
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μA8T26A • μA8T28 Quad 3-State Bus Transceivers

Interface Products

Description

μA8T26A and μA8T28 are Quad 3-State Bus Transceivers featuring MPU or MOS compatibility. Both parts feature high-impedance pnp inputs and high-speed operation made possible by the use of Schottky transistor technology.

These devices are useful as bus extenders in systems employing the F6800, F3870 or other comparable MPU families. Maximum input current of 200 μA at the device input pins assures proper operation despite limited drive capability of the MPU chip.

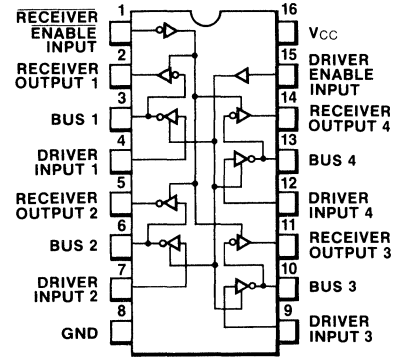
The μA8T26A/28 are identical to the NE8T26A/28 or the MC8T26A/28.

- **μA8T26A—INVERTING BUS**
- **μA8T28—NON-INVERTING**
- **MPU COMPATIBLE**
- **HIGH-IMPEDANCE pnp INPUTS**
- **HIGH-SPEED SCHOTTKY TECHNOLOGY**
- **+5 V SINGLE SUPPLY OPERATION**
- **3-STATE DRIVERS AND RECEIVERS**

Absolute Maximum Ratings	T_A = 25°C unless otherwise noted
Power Supply Voltage (V_{CC})	8.0 V
Input Voltage (V_I)	5.5 V
Junction Temperature (T_J)	
Ceramic DIP	175°C
Molded DIP	150°C
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Pin Temperature	
Molded DIP (Soldering, 10 s)	260°C
Ceramic DIP (Soldering, 60 s)	300°C

Connection Diagrams
16-Pin DIP

μA8T26A

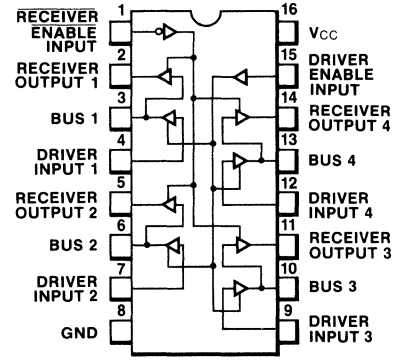


(Top View)

Order Information

Type	Package	Code	Part No.
μA8T26A	Ceramic DIP	6B	μA8T26ADM
μA8T26A	Ceramic DIP	6B	μA8T26ADC
μA8T26A	Molded DIP	9B	μA8T26APC

Connection Diagram
μA8T28

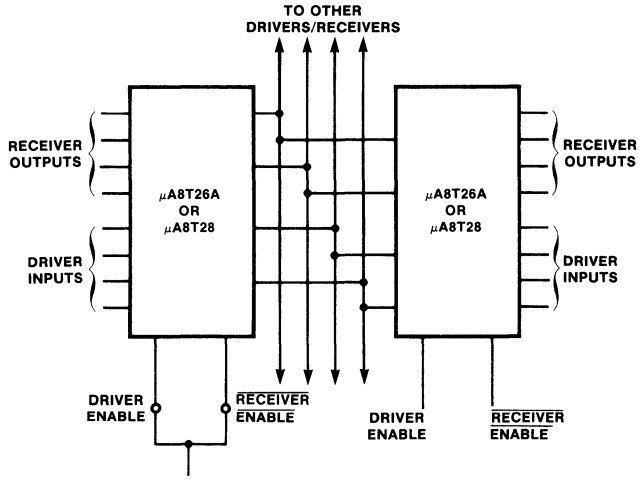


(Top View)

Order Information

Type	Package	Code	Part No.
μA8T28	Ceramic DIP	6B	μA8T28DM
μA8T28	Ceramic DIP	6B	μA8T28DC
μA8T28	Molded DIP	9B	μA8T28PC

Bidirectional Bus Application



DC Characteristics 4.75 V ≤ V_{CC} ≤ 5.25 V for 0°C ≤ T_A ≤ 70°C, and 4.5 V ≤ V_{CC} ≤ 5.5 V for −55°C ≤ T_A ≤ +125°C, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit
	Input Current, LOW Logic State				
$I_{IL(\overline{RE})}$	Receiver Enable Input, $V_{IL(RE)}$ = 0.4 V			−200	μA
$I_{IL(DE)}$	Driver Enable Input, $V_{IL(DE)}$ = 0.4 V			−200	
$I_{IL(D)}$	Driver Input, $V_{IL(D)}$ = 0.4 V			−200	
$I_{IL(B)}$	Bus Receiver Input, $V_{IL(B)}$ = 0.4 V			−200	
	Input Disabled Current, LOW Logic State				
$I_{IL(D)DIS}$	Driver Input, $V_{IL(D)}$ = 0.4 V			−25	μA
	Input Current, HIGH Logic State				
$I_{IH(\overline{RE})}$	Receiver Enable Input, $V_{IH(RE)}$ = 5.25 V			25	μA
$I_{IH(DE)}$	Driver Enable Input, $V_{IH(DE)}$ = 5.25 V			25	
$I_{IH(D)}$	Driver Input, $V_{IH(D)}$ = 5.25 V			25	
$I_{IH(B)}$	Receiver Input, $V_{IH(B)}$ = 5.25 V (μA8T26 only)			100	
	Input Voltage, LOW Logic State				
$V_{IL(\overline{RE})}$	Receiver Enable Input			0.85	V
$V_{IL(DE)}$	Driver Enable Input			0.85	
$V_{IL(D)}$	Driver Input			0.85	
$V_{IL(B)}$	Receiver Input			0.85	
	Input Voltage, HIGH Logic State				
$V_{IH(RE)}$	Receiver Enable Input	2.0			V
$V_{IH(DE)}$	Driver Enable Input	2.0			
$V_{IH(D)}$	Driver Input	2.0			
$V_{IH(B)}$	Receiver Input	2.0			
	Output Voltage, LOW Logic State				
$V_{OL(B)}$	Bus Driver Output, $I_{OL(B)}$ = 48 mA			0.5	V
$V_{OL(R)}$	Receiver Output, $I_{OL(R)}$ = 20 mA			0.5	
	Output Voltage, HIGH Logic State				
$V_{OH(B)}$	Bus Driver Output, $I_{OH(B)}$ = −10 mA	2.4	3.1		V
$V_{OH(R)}$	Receiver Output, $I_{OH(R)}$ = −2.0 mA	2.4	3.1		
	Receiver Output, $I_{OH(R)}$ = −100 μA, VCC = 5.0 V	3.5			
	Output Disabled Leakage Current HIGH Logic State				
$I_{OHL(B)}$	Bus Driver Output, $V_{OH(B)}$ = 2.4 V			100	μA
$I_{OHL(R)}$	Receiver Output, $V_{OH(R)}$ = 2.4 V			100	

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DC Characteristics (Cont.) $4.75\ V \leq V_{CC} \leq 5.25\ V$ for $0°C \leq T_A \leq 70°C$, and $4.5\ V \leq V_{CC} \leq 5.5\ V$ for $-55°C \leq T_A \leq +125°C$, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{OLL(B)}$ $I_{OLL(R)}$	Output Disabled Leakage Current LOW Logic State Bus Output, $V_{OL(B)} = 0.5\ V$ Receiver Output, $V_{OL(R)} = 0.5\ V$			 −100 −100	μA
$V_{IC(DE)}$ $V_{IC(RE)}$ $V_{IC(D)}$	Input Clamp Voltage Driver Enable Input $I_{IC(DE)} = -12\ mA$ Receiver Enable Input $I_{IC(RE)} = -12\ mA$ Driver Input $I_{IC(D)} = -12\ mA$			 −1.0 −1.0 −1.0	V
$I_{OS(B)}$ $I_{OS(R)}$	Output Short-Circuit Current, $V_{CC} = 5.25\ V$, Note Bus Driver Output Receiver Output	 −50 −30	 80 50	 −150 −75	mA
I_{CC}	Power Supply Current $V_{CC} = 5.25\ V$		50	87	mA

Note
Only one output may be short-circuited at a time

μA8T26A AC Characteristics Unless otherwise noted, specifications apply at $T_A = 25°C$ and $V_{CC} = 5.0\ V$.

Symbol	Characteristic	Figure	Typ	Max	Unit
$t_{PLH(R)}$	Propagation Delay Time from Receiver (Bus) Input to HIGH Logic State Receiver Output	1	9	14	ns
$t_{PHL(R)}$	Propagation Delay Time from Receiver (Bus) Input to LOW Logic State Receiver Output	1	6	14	ns
$t_{PLH(D)}$	Propagation Delay Time from Driver Input to HIGH Logic State Driver (Bus) Output	2	10	14	ns
$t_{PHL(D)}$	Propagation Delay Time from Driver Input to LOW Logic State Driver (Bus) Output	2	10	14	ns
$t_{PLZ(RE)}$	Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to HIGH Impedance (Open) Logic State Receiver Output	3	10	15	ns
$t_{PZL(RE)}$	Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to LOW Logic Level Receiver Output	3	15	20	ns
$t_{PLZ(DE)}$	Propagation Delay Time from Driver Enable Input to HIGH Impedance Logic State Driver (Bus) Output	4	15	20	ns
$t_{PZL(DE)}$	Propagation Delay Time from Driver Enable Input to LOW Logic State Driver (Bus) Output	4	19	25	ns

μA8T28 AC Characteristics $T_A = 25°C$, $V_{CC} = 5.0\ V$ unless otherwise specified.

Symbol	Characteristic	Figure	Typ	Max	Unit
$t_{PLH(R)}$ $t_{PHL(R)}$	Propagation Delay Time—Receiver ($C_L = 30\ pF$)	5	−12 −9	17 17	ns
$t_{PLH(D)}$ $t_{PHL(D)}$	Propagation Delay Time—Driver ($C_L = 300\ pF$)	6	−13 −13	17 17	ns
$t_{PZL(RE)}$ $t_{PLZ(RE)}$	Propagation Delay Time—Receiver Enable ($C_L = 30\ pF$)	7	−18 −13	23 18	ns
$t_{PZL(DE)}$ $t_{PLZ(DE)}$	Propagation Delay Time—Driver Enable ($C_L = 300\ pF$)	8	−21 −18	28 23	ns

Fig. 1 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Bus (Receiver) Input to Receiver Output, $t_{PLH(R)}$ and $t_{PHL(R)}$

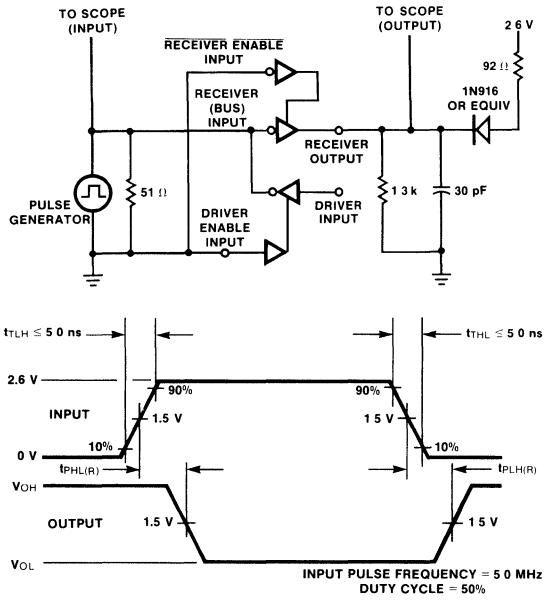

Fig. 2 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Driver Input to Bus (Driver) Output, $t_{PLH(D)}$ and $t_{PHL(D)}$

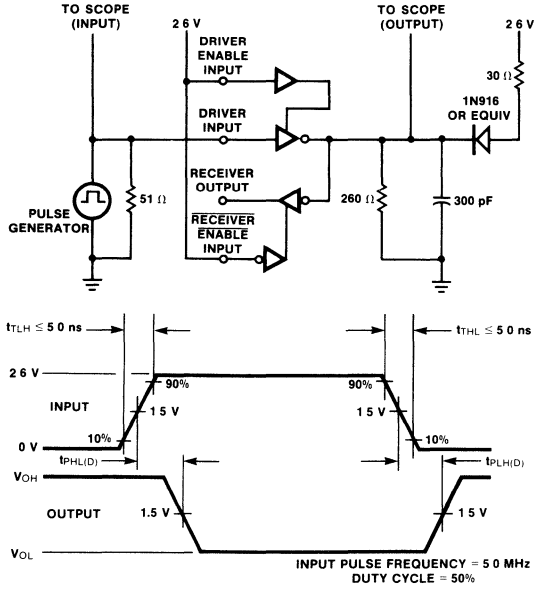

Fig. 3 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Receiver Enable Input to Receiver Output, $t_{PLZ(RE)}$ and $t_{PZL(RE)}$

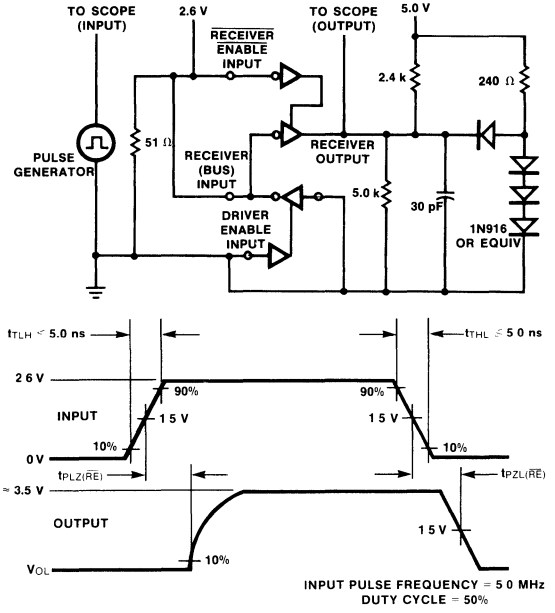

Fig. 4 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Driver Enable Input to Driver (Bus) Output, $t_{PLZ(DE)}$ and $t_{PZL(DE)}$

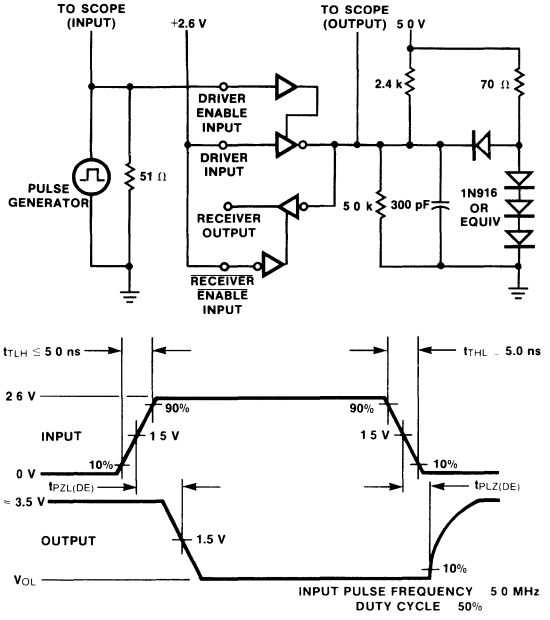

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Fig. 5 **μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Bus (Receiver) Input to Receiver Output, $t_{PLH(R)}$ and $t_{PHL(R)}$**

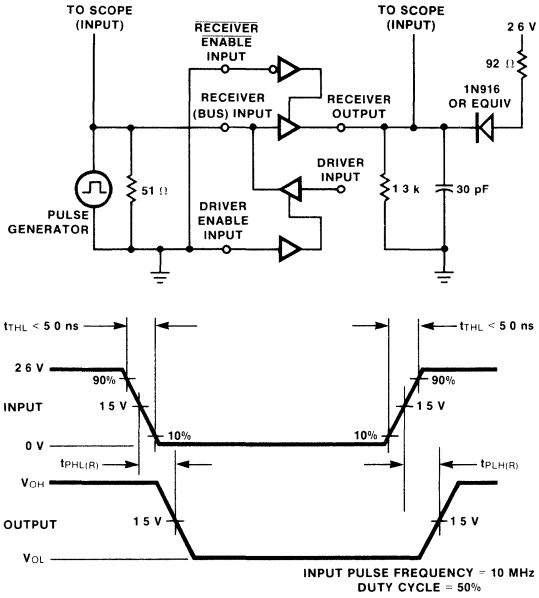


Fig. 6 **μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Driver Input to Bus (Driver) Output, $t_{PLH(D)}$ and $t_{PHL(D)}$**

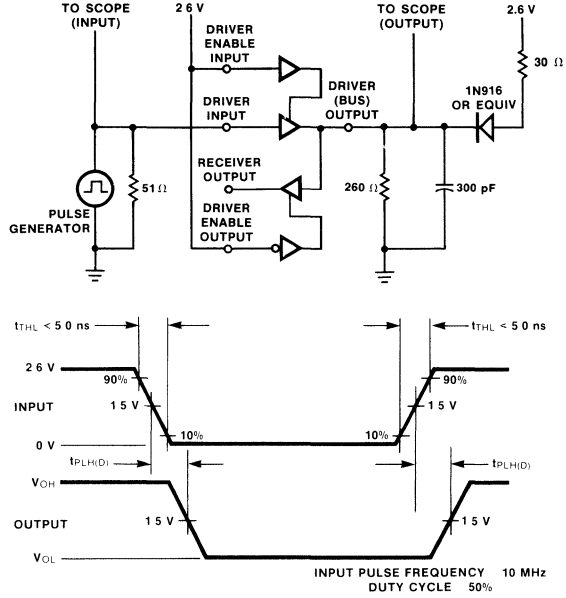


Fig. 7 **μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Receiver Enable Input to Receiver Output, $t_{PLZ(RE)}$ and $t_{PZL(RE)}$**

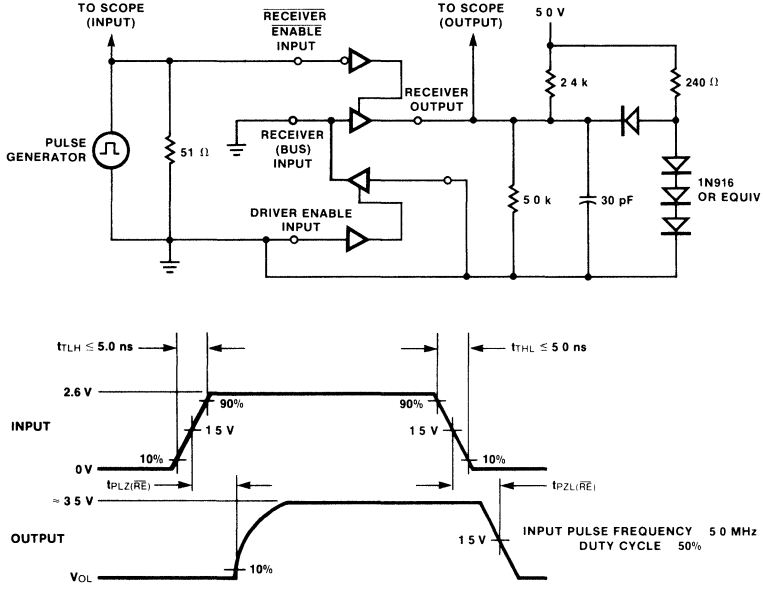
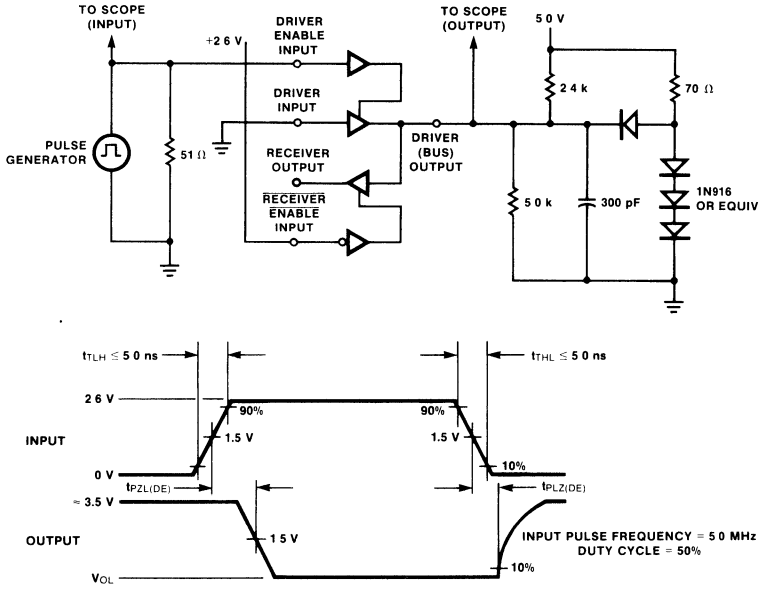


Fig. 8 μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Driver Enable Input to Driver (Bus) Output, $t_{PLZ(DE)}$ and $t_{PZL(DE)}$



6

FAIRCHILD
A Schlumberger Company

μA9643 Dual TTL To MOS/CCD Driver

Interface Products

Description

The μA9643 is a Dual Positive-Logic "AND" TTL-to-MOS Driver. The μA9643 is a functional replacement of the SN75322 with one important exception: the two external pnp transistors are no longer needed for operation. The μA9643 is also a functional replacement for the 75363 with the important exception that the V_{CC3} supply is not needed. The pin connections normally used for the external pnp transistors are purposely not internally connected to the μA9643.

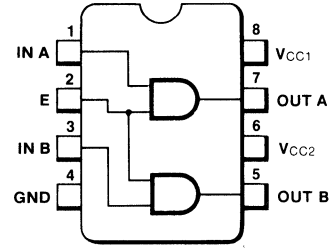
- **SATISFIES CCD MEMORY AND DELAY LINE REQUIREMENTS**
- **DUAL POSITIVE-LOGIC TTL-TO-MOS DRIVER**
- **OPERATES FROM STANDARD BIPOLAR AND MOS SUPPLY VOLTAGES**
- **HIGH-SPEED SWITCHING**
- **TTL AND DTL COMPATIBLE INPUTS**
- **SEPARATE DRIVER ADDRESS INPUTS WITH COMMON STROBE**
- **V_{OH} AND V_{OL} COMPATIBLE WITH POPULAR MOS RAMs**
- **DOES NOT REQUIRE EXTERNAL pnp TRANSISTORS OR V_{CC3}**
- **V_{OH} MINIMUM IS V_{CC2} − 0.5 V**

Absolute Maximum Ratings

Over operating ambient temperature range unless otherwise noted

Supply Voltage Range of V_{CC1} (Note 1)	−0.5 V to 7 V
Supply Voltage Range of V_{CC2}	−0.5 V to 15 V
Input Voltage	5.5 V
Inter-Input Voltage (Note 2)	5.5 V
Continuous Total Dissipation at T_A = 25°C	1000 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Pin Temperature Molded DIP (Soldering, 10 s)	260°C

Connection Diagram
8-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA9643	Molded DIP	9T	μA9643TC

Notes

1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the gates.

Recommended Operating Conditions

Characteristic	Min	Typ	Max	Unit
Supply Voltage, V_{CC1}	4.75	5.0	5.25	V
Supply Voltage, V_{CC2}	4.75	12	15	V
Operating Temperature, T_A	0		70	°C

Electrical Characteristics Over recommended ranges of V_{CC1}, V_{CC2} and operating ambient temperature unless otherwise noted.

Symbol	Characteristic	Condition		Min	Typ(3)	Max	Unit
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA		V_{CC2} − 0.5	V_{CC2} − 0.2		V
V_{OL}	Output LOW Voltage	I_{OL} = 10 mA			0.4	0.5	V
		I_{OL} = 1.0 mA			0.2	0.3	V
I_{IN}	Input Current at Maximum Input Voltage	V_{CC1} = 5.25 V, V_{CC2} = 11.4 V V_{IN} = 5.25 V				0.1	mA
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V	A Inputs			40	μA
			E Inputs			80	
I_{IL}	Input LOW Current	V_{IN} = 0.4 V	A Inputs			0.5	mA
			E Inputs			− 1.0	
$I_{CC1(L)}$	Supply Current from V_{CC1} All Outputs LOW	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	No Load		15	19	mA
$I_{CC2(L)}$	Supply Current from V_{CC2} All Outputs LOW	V_{CC2} = 12.6 V	V_{CC1} = 5.25 V		5.5	9.5	mA
$I_{CC1(H)}$	Supply Current from V_{CC1} All Outputs HIGH	V_{CC1} = 5.5 V V_{CC2} = 13.2 V	No Load		9.0	13	mA
$I_{CC2(H)}$	Supply Current from V_{CC2} All Outputs HIGH	V_{CC2} = 12.6 V	V_{CC1} = 5.25 V		5.5	9.5	mA

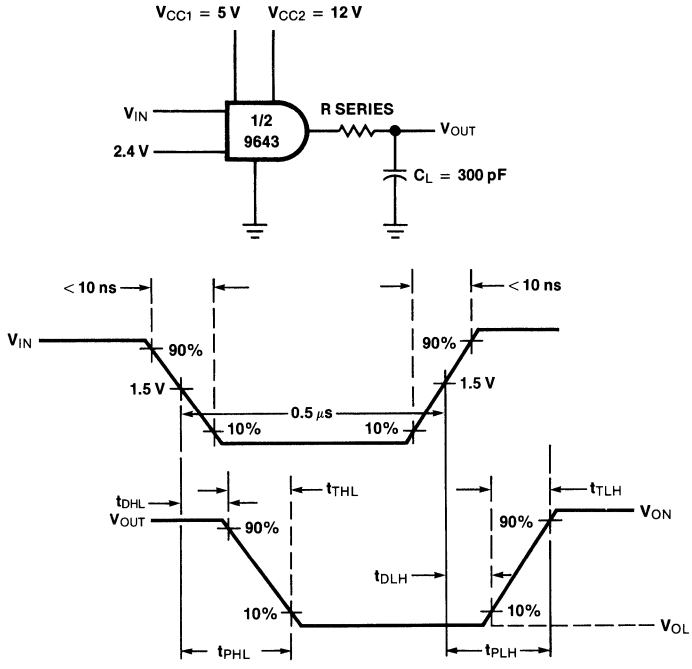
AC Characteristics V_{CC1} = 5.0 V, V_{CC2} = 12 V, T_A = 25°C

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
t_{DLH}	Delay Time	C_L = 300 pF		5.0	9.0	17	ns
t_{DHL}	Delay Time			5.0	9.0	17	ns
t_{TLH}	Rise Time	R_{SERIES} = 0	C_L = 300 pF	6.0	11	17	ns
t_{THL}	Fall Time			6.0	11	17	ns
t_{TLH}	Rise Time	R_{SERIES} = 10 Ω		8.0	14	20	ns
t_{THL}	Fall Time			8.0	14	20	ns
t_{PLH_A} − t_{PLH_B} t_{PHL_A} − t_{PHL_B}	Skew between outputs A and B				0.5		ns

Note

3. All typical values are at V_{CC1} = 5.0 V, V_{CC2} = 12 V, and T_A = 25°C unless otherwise noted.

AC Test Circuit and Waveforms



The pulse generator has the following characteristics:
PRR = 1 MHz, Z_{OUT} – 50 Ω

C_L includes probe and jig capacitance.

FAIRCHILD
A Schlumberger Company

μA9645/3245 Quad TTL-to-MOS/CCD Driver

Interface Products

Description

The μA9645/3245 is a High-Speed Driver intended to be used as a clock (high-level) driver for 18 or 22-pin dynamic NMOS RAMs. It also satisfies the non-overlapping 2-phase clock drive requirements for CCD memories like the F464 (64K) RAM.

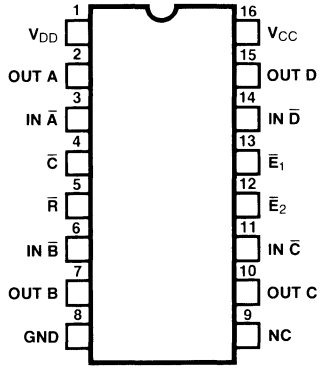
The circuit is designed to operate on nominal +5 V and +12 V power supplies and contains input and output clamp diodes to minimize line reflections.

The device features two common enable inputs, a refresh select input and a clock control input. Internal gating structure is organized so that all four drivers may be deactivated for standby operation, or single driver may be activated for read/write operation or all four drivers may be activated for refresh operation.

The μA9645/3245 is a pin-for-pin replacement of the Intel 3245 Quad TTL-to-MOS Driver, with substantially reduced dc power dissipation.

- **INTERCHANGEABLE WITH INTEL 3245**
- **FOUR HIGH-SPEED, HIGH-CURRENT DRIVERS**
- **CONTROL LOGIC OPTIMIZED FOR MOS RAMs**
- **SATISFIES CCD MEMORY AND DELAY LINE DRIVE REQUIREMENTS**
- **TTL AND DTL COMPATIBLE INPUTS**
- **HIGH-VOLTAGE SCHOTTKY TECHNOLOGY**

Connection Diagram
16-Pin DIP

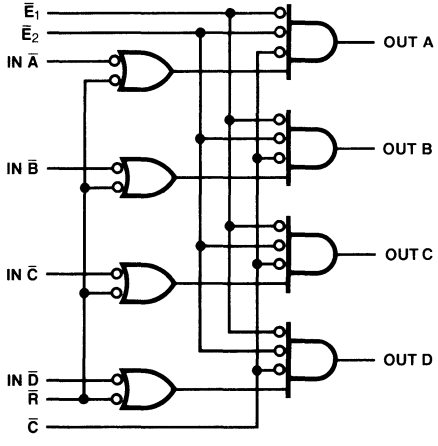


(Top View)

Order Information

Type	Package	Code	Part No.
μA9645	Ceramic DIP	7B	μA9645PC/3245
μA9645	Molded DIP	9B	μA9645DC/3245

Logic Diagram



Truth Table

Inputs					Output
Control			Address		
$\overline{C}$	$\overline{E}_2$	$\overline{E}_1$	$\overline{INPUT}$	$\overline{REFRESH}$	
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	H	L
L	L	L	L	X	H
L	L	L	X	L	H

H = HIGH
L = LOW
X = Don't Care

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +70°C	Outputs For Clock Driver	−1.0 V to V_{DD} +1 V
Storage Temperature	−65°C to +150°C	Operating Temperature Range	0°C to +70°C
Supply Voltage, V_{CC}	−0.5 V to +7.0 V	Junction Temperature (T_J)	
Supply Voltage, V_{DD}	−0.5 V to +14.0 V	Ceramic Package	175°C
All Input Voltages	−1.0 V to V_{DD}	Molded Package	150°C

DC Characteristics T_A = 0°C to 70°C, V_{CC} = 5.0 V ±5%, V_{DD} = 12 V ±5%, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{FD}	Input Load Current, IN ($\overline{A}$,$\overline{B}$,$\overline{C}$,$\overline{D}$)	V_F = 0.45 V			−0.25	mA
I_{FE}	Input Load Current, $\overline{R}$, $\overline{C}$, $\overline{E}_1$, $\overline{E}_2$	V_F = 0.45 V			−1.0	mA
I_{RD}	Data Input Leakage Current	V_R = 5.0 V			10	μA
I_{RE}	Enable Input Leakage Current	V_R = 5.0 V			40	μA
V_{OL}	Output LOW Voltage	I_{OL} = 5 mA, V_{IH} = 2 V			0.45	V
		I_{OL} = −5 mA	−1.0			V
V_{OH}	Output HIGH Voltage	I_{OH} = −1 mA, V_{IL} = 0.8 V	V_{DD} − 0.50			V
		I_{OH} = 5 mA			V_{DD} + 1.0	V
V_{IL}	Input LOW Voltage, All Inputs				0.8	V
V_{IH}	Input HIGH Voltage, All Inputs		2.0			V
$I_{CC(H)}$	Current From V_{CC}	V_{CC} = 5.25 V V_{DD} = 12.6 V All Outputs HIGH		13	20	mA
$I_{DD(H)}$	Current From V_{DD}			14	20	mA
$P_{DI(H)}$	Power Dissipation			248	357	mW
	Power Per Channel			62	90	mW
$I_{CC(L)}$	Current From V_{CC}	V_{CC} = 5.25 V V_{DD} = 12.6 V All Outputs LOW		27	35	mA
$I_{DD(L)}$	Current From V_{DD}			12	15	mA
$P_{D2(L)}$	Power Dissipation			296	373	mW
	Power Per Channel			74	94	mW

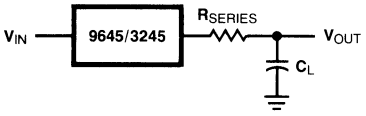
AC Characteristics T_A = 0°C to 70°C, V_{CC} = 5.0 V ±5%, V_{DD} = 12 V ±5% unless otherwise specified.

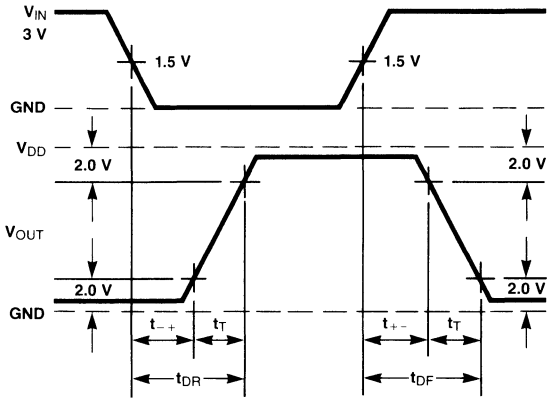
Symbol	Characteristic	Condition	Min (1)	Typ (2,4)	Max (3)	Unit
t_{-+}	Input to Output Delay	R_{SERIES} = 0	5	11		ns
t_{DR}	Delay Plus Rise Time	R_{SERIES} = 0		18	32	ns
t_{+-}	Input to Output Delay	R_{SERIES} = 0	3	7		ns
t_{DF1}	Delay Plus Fall Time	R_{SERIES} = 0		18	32	ns
t_T	Output Transition Time	R_{SERIES} = 20 Ω	10	13	20	ns
t_{DR}	Delay Plus Rise Time	R_{SERIES} = 20 Ω		27	38	ns
t_{DF2}	Delay Plus Fall Time	R_{SERIES} = 20 Ω		24	38	ns

Notes

1. C_L = 150 pF
2. C_L = 200 pF
3. C_L = 250 pF
4. Typical values are measured at 25°C

AC Test Circuit and Waveforms





AC Test Conditions:
Input Pulse Amplitude = 3.0 V
Input Pulse Rise and Fall Times = 5 ns Between 1 V and 2 V

6

FAIRCHILD

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μA9665/6/7/8 High-Current Voltage, Darlington Drivers

Interface Products

Description

The μA9665, μA9666, μA9667 and μA9668 are comprised of seven high-voltage, high-current npn Darlington transistor pairs. All units feature common emitter, open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads and appropriate emitter-base resistors for leakage.

The μA9665 is a general-purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. Input current limiting is done by connecting an appropriate discrete resistor to each input.

The μA9666 version does away with the need for any external discrete resistors, since each unit has a resistor and a Zener diode in series with the input. The μA9666 was specifically designed for direct interface from PMOS logic (operating at supply voltages from 14 to 25 V) to solenoids or relays.

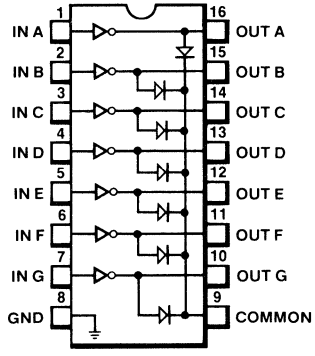
The μA9667 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V.

The μA9668 has an appropriate input resistor to allow direct operation from CMOS or PMOS outputs operating from supply voltages of 6 to 15 V.

μA9665, μA9666, μA9667 and μA9668 offer solutions to a great many interface needs, including solenoids, relays, lamps, small motors and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

- **SEVEN HIGH-GAIN DARLINGTON PAIRS**
- **HIGH OUTPUT VOLTAGE (V_{CE} = 50 V)**
- **HIGH OUTPUT CURRENT (I_C = 350 mA)**
- **DTL, TTL, PMOS, CMOS COMPATIBLE**
- **SUPPRESSION DIODES FOR INDUCTIVE LOADS**
- **2 WATT MOLDED DIP ON COPPER PIN FRAME**

Connection Diagram
16-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA9665	Molded DIP	9B	μA9665PC
μA9666	Ceramic DIP	6B	μA9666DC
μA9666	Molded DIP	9B	μA9666PC
μA9667	Ceramic DIP	6B	μA9667DC
μA9667	Molded DIP	9B	μA9667PC
μA9668	Ceramic DIP	6B	μA9668DC
μA9668	Molded DIP	9B	μA9668PC

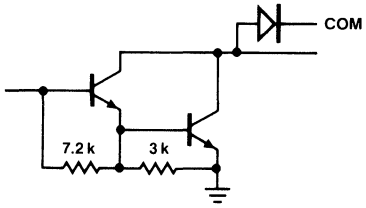
Absolute Maximum Ratings	T_A = 25°C
Output Voltage, V_{CE}	55 V
Input Voltage, V_{IN}	30 V
Emitter-Base Voltage, V_{EBO}	6 V
Continuous Collector Current, I_C	500 mA
Continuous Base Current, I_B	25 mA
Power Dissipation (6B, Kovar lead frame)	1.0 W
Power Dissipation (9B, Copper lead frame) (Note 1)	2.0 W
Pin Temperature	
Molded DIP, Soldering (10 s)	260°C
Ceramic DIP, Soldering (60 s)	300°C
Temperature Range	
Operating, T_A—DC, PC	0°C to +70°C
Storage Temperature Range, T_S	−65°C to +150°C

Notes

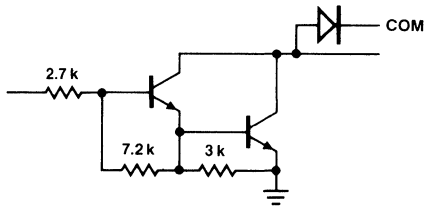
1 Under normal operating conditions, these units will sustain 350 mA per output with $V_{CE(sat)}$ = 1 6 V at 70°C with a pulse width of 20 ms and a duty cycle of 30%

Equivalent Circuits
(Each Device)

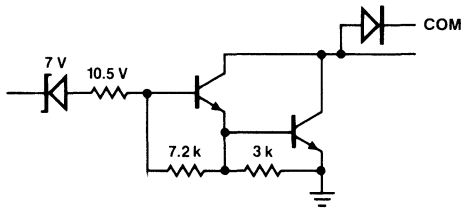
μA9665



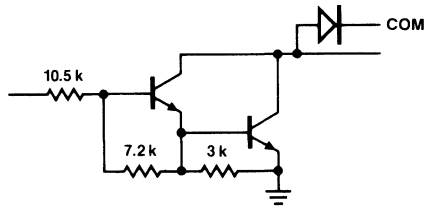
μA9667



μA9666



μA9668



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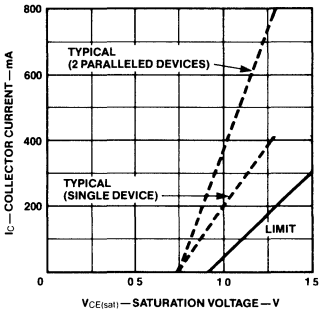
μA9665/6/7/8
Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Characteristic	Test Figure	Conditions (Note 2)	Min	Typ	Max	Unit
I_{CEX}	Output Leakage Current	1a	V_{CE} = 50 V			100	μA
	T_A = +70°C for DC, PC	1b	V_{CE} = 50 V, V_{IN} = 6 V (9666)			500	μA
		1b	V_{CE} = 50 V, V_{IN} = 1 V (9668)			500	μA
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	2	I_C = 350 mA, I_B = 500 μA		1.25	1.6	V
		2	I_C = 200 mA, I_B = 350 μA		1.1	1.3	V
		2	I_C = 100 mA, I_B = 250 μA		0.9	1.1	V
$I_{IN(ON)}$	Input Current	3	V_{IN} = 17 V (9666)		0.85	1.3	mA
		3	V_{IN} = 3.85 V (9667)		0.93	1.35	mA
		3	V_{IN} = 5 V (9668)		0.35	0.5	mA
		3	V_{IN} = 12 V (9668)		1.0	1.45	mA
$I_{IN(OFF)}$	Input Current (Note 3) T_A = +70°C for PC, DC	4	I_C = 500 μA	50	65		μA
$V_{IN(ON)}$	Input Voltage (Note 4)	5	V_{CE} = 2 V, I_C = 300 mA (9666)			13	V
		5	V_{CE} = 2 V, I_C = 200 mA (9667)			2.4	V
		5	V_{CE} = 2 V, I_C = 250 mA (9667)			2.7	V
		5	V_{CE} = 2 V, I_C = 300 mA (9667)			3.0	V
		5	V_{CE} = 2 V, I_C = 125 mA (9668)			5.0	V
		5	V_{CE} = 2 V, I_C = 200 mA (9668)			6.0	V
		5	V_{CE} = 2 V, I_C = 275 mA (9668)			7.0	V
		5	V_{CE} = 2 V, I_C = 350 mA (9668)			8.0	V
h_{FE}	DC Forward Current Transfer Ratio	2	V_{CE} = 2 V, I_C = 350 mA (9665)	1000			
C_{IN}	Input Capacitance				15	30	pF
t_{PLH}	Turn-On Delay		0.5 V_{IN} to 0.5 V_{OUT}		1	5	μs
t_{PHL}	Turn-Off Delay		0.5 V_{IN} to 0.5 V_{OUT}		1	5	μs
I_R	Clamp Diode Leakage Current	6	V_R = 50 V			50	μA
V_F	Clamp Diode Forward Voltage	7	I_F = 350 mA		1.7	2.0	V

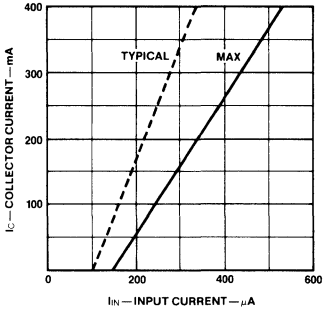
Notes
2. All limits stated apply to the complete Darlington series except as specified for a single device type.
3. The $I_{IN(OFF)}$ current limit guaranteed against partial turn-on of the output.
4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions

Typical Performance Curves

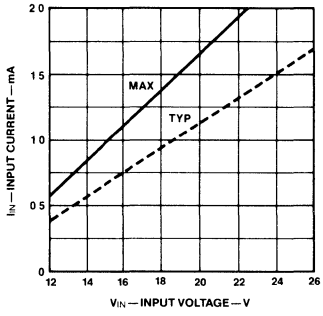
Collector Current vs Saturation Voltage



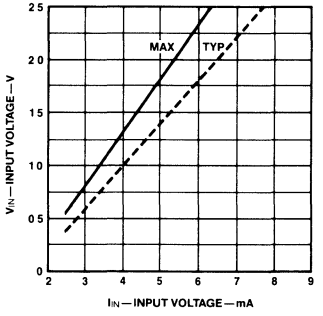
Collector Current vs Input Current



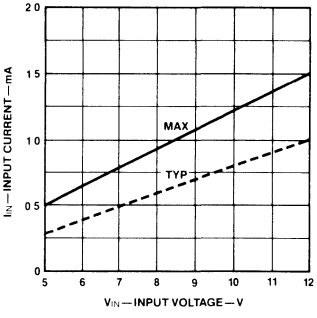
μA9666 Input Current vs Input Voltage



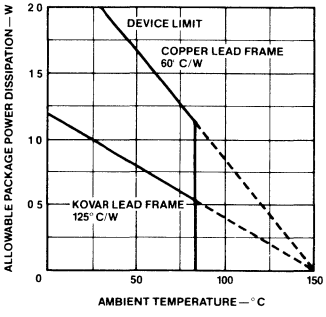
μA9667 Input Current vs Input Voltage



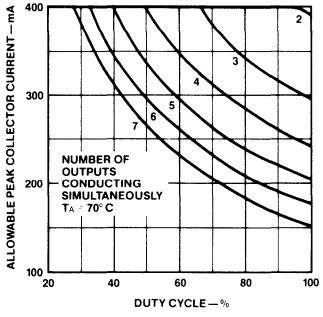
μA9668 Input Current vs Input Voltage



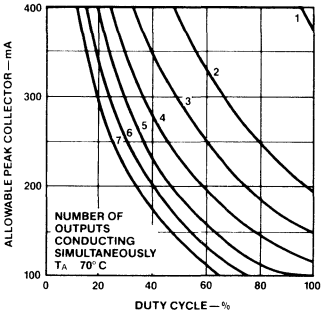
Allowable Average Package Power Dissipation vs Ambient Temperature



Peak Collector Current vs Duty Cycle and Number of Outputs (Molded Package)



Peak Collector Current vs Duty Cycle and Number of Outputs (Ceramic Package)



6

Test Circuits

Figure 1a

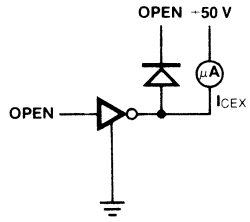


Figure 1b

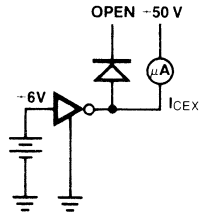


Figure 2

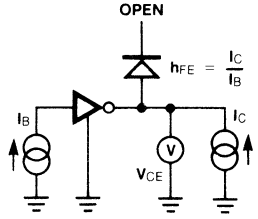


Figure 3

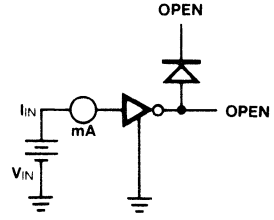


Figure 4

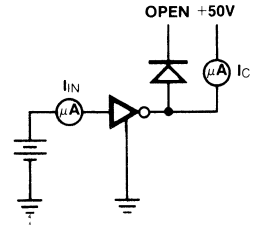


Figure 5

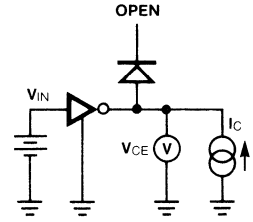


Figure 6

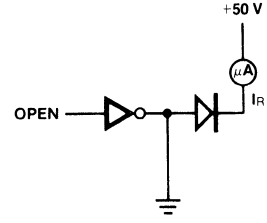
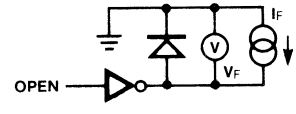
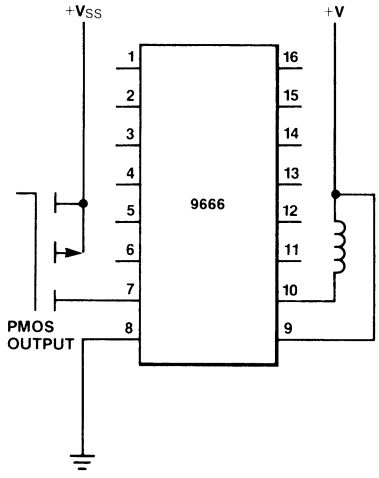


Figure 7

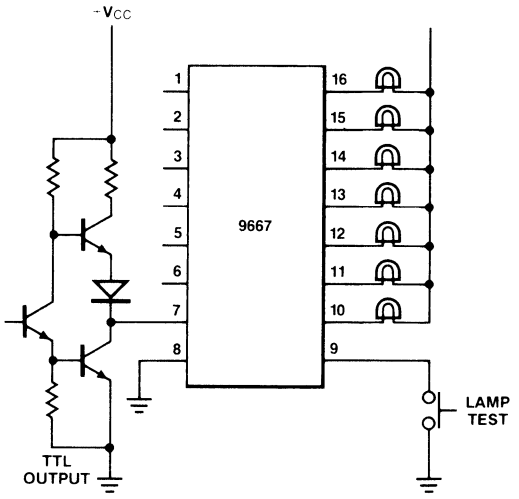


Typical Applications

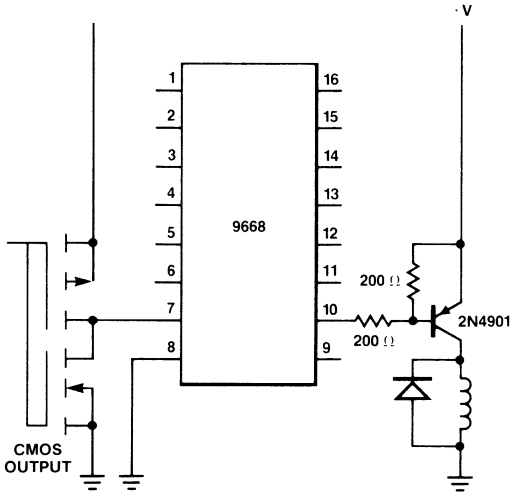
PMOS to Load



Buffer for Higher Current Loads



TTL to Load



FAIRCHILD
A Schlumberger Company

μA75450/60/70 Series Dual Peripheral Drivers

Interface Products

Description

The μA75400 series of devices are Dual High-Speed General-Purpose Interface Drivers that convert TTL and DTL logic levels to high-current drive capability. The μA75450B features two TTL NAND gates and two uncommitted transistors. The μA75451A, μA75452A, and μA75453A feature two standard series 74 TTL gates in AND, NAND, OR and NOR configurations respectively, driving the base of two high voltage, high current, uncommitted collector output transistors.

The μA75400 series offers flexibility in designing high-speed logic buffers, power drivers, lamp drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- **NO LATCH-UP UP TO 55 V**
- **HIGH OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

Absolute Maximum Ratings

	μA75450B	**μA75451A/B μA75461 μA75452A/B μA75462 μA75453A/B μA75471 μA75472**
Supply Voltage, V_{CC}, Note 1	7 V	7 V
Input Voltage, Note 1	5.5 V	5.5 V
Inter-emitter Voltage, Note 2	5.5 V	5.5 V
V_{CC} to Substrate Voltage, Note 6	35 V	
Collector to Substrate Voltage, Note 6	35 V	
Collector to Base Voltage	35 V	
Collector to Emitter Voltage, Note 3	30 V	
Emitter to Base Voltage	5 V	
Output Voltage Notes 1 and 4		Table 2
Continuous Collector Current, Note 5	300 mA	
Continuous Output Current, Note 5		300 mA
Continuous Total Power Dissipation, Note 7	800 mW	800 mW
Operating Ambient Temperature Range	0°C to 70°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Pin Temperature Molded DIP (Soldering, 10 s) Ceramic DIP (Soldering, 60 s)	 260°C 300°C	 260°C 300°C

Notes on following page

Test Table 1 Operating Temperature Range and Supply Voltage Range

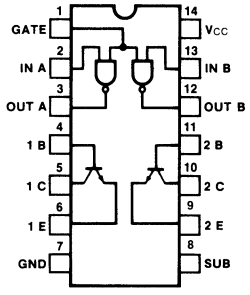
	μA75000 Series
Temperature, T_A	0°C to 70°C
Supply Voltage, V_{CC}	+4.75 V to +5.25 V

Test Table 2

	μA7545XA μA7545XB	μA75461 μA75462	μA75471 μA75472
Maximum Output, V_{OH}	30 V	35 V	80 V
Maximum, Latch-up, V_S	20 V	30 V	55 V

μA75450B
Dual Positive AND Peripheral Drivers

Connection Diagram
14-Pin DIP



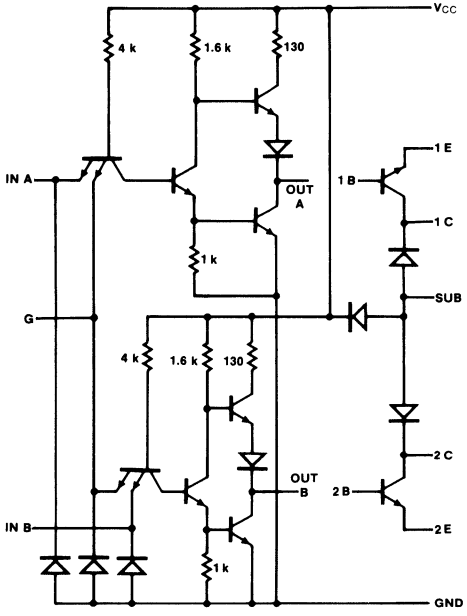
(Top View)

Logic Function
Positive Logic $Z = \overline{XY}$ (gate only)
$Z = XY$ (gate and transistor)

Order Information

Type	Package	Code	Part No.
μA75450B	Molded DIP	9A	μA75450BPC

Equivalent Circuit



All resistor values in ohms

Notes
1 Voltage values are with respect to network ground terminal unless otherwise specified
2 This is the voltage between two emitters of a multiple-emitter input transistor
3 This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω
4 This is the maximum voltage which should be applied to any output when it is in the off state
5 Both halves of these dual circuits may conduct rated current simultaneously
6 For the μA75450 only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation
7 Above 60°C ambient temperature, derate linearly at 8 3 mW/°C for Ceramic DIP and Molded DIP For the Molded Mini DIP and Ceramic Mini DIP, derate at 6 7 mW/°C above 30°C

μA75450B
Electrical Characteristics Guaranteed over operating temperature range and supply voltage range, use test table 1, unless otherwise indicated

TTL Gates

Symbol	Characteristic		Test Figure	Condition	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage		1		2			V
V_{IL}	Input LOW Voltage		2				0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = Min, V_{IL} = 0.8 V I_{OH} = −400 μA	2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = Min, V_{IN} = 2 V I_{OL} = 16 mA		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	Input A	4	V_{CC} = Max, V_{IN} = 5.5 V			1	mA
		Input G					2	
I_{IH}	Input HIGH Current	Input A	4	V_{CC} = Max, V_{IN} = 2.4 V			40	μA
		Input G					80	
I_{IL}	Input LOW Current	Input A	3	V_{CC} = Max, V_{IN} = 0.4 V			−1.6	mA
		Input G					−3.2	
I_{OS}	Short-Circuit Output Current, Note 2		5	V_{CC} = Max	−18		−55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = Max, V_{IN} = 0 V		2	4	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = Max, V_{IN} = 5 V		6	11	

μA75450B
Electrical Characteristics Guaranteed over operating temperature range and supply voltage range, use test table 1, unless otherwise indicated

Output Transistors

Symbol	Characteristic	Condition	Min	Typ (1)	Max	Unit
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0	35			V
$V_{(BR)CER}$	Collector to Base Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω	30			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0	5			V
h_{FE}	Static Forward Current Transfer Ratio, Note 3	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C	25 30			
		V_{CE} = 3 V, I_C = 100 mA	20			
		V_{CE} = 3 V, I_C = 300 mA	25			
$V_{BE(sat)}$	Base to Emitter Voltage, Note 3	I_B = 10 mA, I_C = 100 mA		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA		1.05	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage, Note 3	I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA		0.5	0.7	V

Notes
1 All typical values are at V_{CC} = 5 V, T_A = 25°C
2 Not more than one output should be shorted at a time
3 These parameters must be measured using the pulse techniques t_w = 300 μs, duty cycle ≤ 2%
4 Voltage and current values shown are nominal, exact values vary slightly with transistor parameter

μA75450B
AC Characteristics V_{CC} = 5 V, T_A = 25°C

TTL Gates

Symbol	Characteristic	Test Figure	Condition	μA75450B Min	Typ	Max	Unit
T_{PLH}	Propagation Delay Time, LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		12	22	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				8	15	ns

Output Transistors

Symbol	Characteristic	Test Figure	Condition (Note 3)	Min	Typ	Max	Unit
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = −1 V $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA C_L = 15 pF, R_L = 50 Ω		8	15	ns
t_r	Rise Time				12	20	ns
t_s	Storage Time				7	15	ns
t_f	Fall Time				6	15	ns

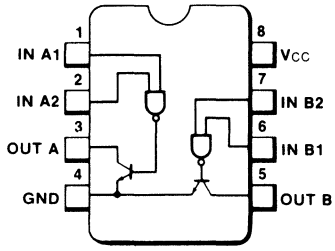
Gates and Transistors Combined

Symbol	Characteristic	Test Figure	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		20	30	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				20	30	ns
t_{TLH}	Transition Time, LOW to HIGH				7	12	ns
t_{THL}	Transition Time, HIGH to LOW				9	15	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_C \approx$ 300 mA R_{BE} = 500 Ω	V_S − 6.5			mV

Notes
1. All typical values are at V_{CC} = 5 V, T_A = 25°C
2. Not more than one output should be shorted at a time
3. These parameters must be measured using the pulse techniques t_w = 300 μs, duty cycle ≤ 2%
4. Voltage and current values shown are nominal, exact values vary slightly with transistor parameter

μA75451A/B • μA75461 • μA75471
Dual Positive AND Peripheral Drivers

Connection Diagram
8-Pin DIP



(Top View)

Truth Table

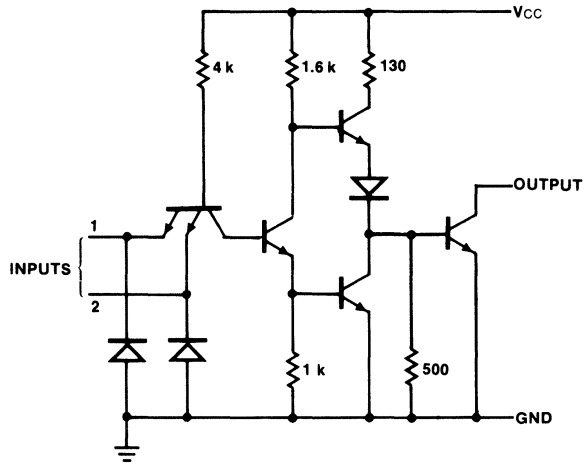
Inputs		Output	
X	Y	Z	
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

Order Information

Type	Package	Code	Part No.
μA75451A	Molded DIP	9T	μA75451ATC
μA75451A	Ceramic DIP	6T	μA75451ARC
μA75451B	Molded DIP	9T	μA75451BTC
μA75451B	Ceramic DIP	6T	μA75451BRC
μA75461	Molded DIP	9T	μA75461TC
μA75471	Molded DIP	9T	μA75471TC

Equivalent Circuit (Each Driver)



Component values shown are nominal All resistor values in ohms

μA75451A/B
Electrical Characteristics Guaranteed over operating temperature range and supply voltage range, use test table 1.

Symbol	Characteristic	Test Figure	Condition (Note 1)	μA75451A			μA75451B			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	7		2.0			2.0			V
V_{IL}	Input LOW Voltage	7				0.8			0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = Min, I_{IN} = −12 mA			−1.5			−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = Min, V_{IH} = 2 V, Note 2			100			100	μA
V_{OL}	Output LOW Voltage	7	V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4		0.25	0.4	V
			V_{CC} = Min V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = Max, V_{IN} = 5.5 V			1.0			1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = Max, V_{IN} = 2.4 V			40			40	μA
I_{IL}	Input LOW Current	8	V_{CC} = Max, V_{IN} = 0.4 V		−1.0	−1.6		−1.0	−1.6	mA
I_{CCH}	Supply Current, Output High	10	V_{CC} = Max, V_{IN} = 5 V		7.0	11		7.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = Max, V_{IN} = 0 V		52	65		52	65	mA

μA75451A/B
AC Characteristics V_{CC} = 5 V, T_A = 25°C

Symbol	Characteristic	Test Figure	Condition	μA75451A			μA75451B			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		20	55		18	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				20	40		18	25	ns
t_{TLH}	Transition Time, LOW to HIGH				8	20		5	8	ns
t_{THL}	Transition Time, HIGH to LOW				12	20		7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	$I_O \approx$ 300 mA, Note 3	V_S − 6.5			V_S − 6.5			mV

Notes
1. All typical values are at V_{CC} = 5 V, T_A = 25°C
2. V_{OH} = 30 V for μA75451A and B, 35 V for μA75461, 80 V for μA75471
3. V_S = 20 V for μA75451A and B, 30 V for μA75461, 55 V for μA75471

μA75461/μA75471
Electrical Characteristics Guaranteed over operating temperature range and supply voltage range, use test table 1, page 1.

Symbol	Characteristic	Test Figure	Condition (Note 1)	μA75461			μA75471			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	7		2.0			2.0			V
V_{IL}	Input LOW Voltage	7				0.8			0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = Min, I_{IN} = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = Min, V_{IH} = 2 V, Note 2			100			100	μA
V_{OL}	Output LOW Voltage	7	V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 100 mA		.16	0.4		0.16	0.4	V
			V_{CC} = Min, V_{IL} = 0.8 V I_{OL} = 300 mA		.35	0.7		0.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = Max, V_I = 5.5 V			1.0			1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = Max, V_I = 2.4 V			40			40	μA
I_{IL}	Input LOW Current	8	V_{CC} = Max, V_I = 0.4 V		−1.0	−1.6		−1.0	−1.6	mA
I_{CCH}	Supply Current, Output High	10	V_{CC} = Max, V_I = 5 V		8.0	11		8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = Max, V_{IH} = 0 V		61	76		61	76	mA

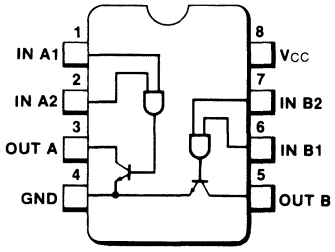
μA75461/μA75471
AC Characteristics V_{CC} = 5 V, T_A = 25°C

Symbol	Characteristic	Test Figure	Condition	μA75461			μA75471			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		35	55		35	55	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				25	40		25	40	ns
t_{TLH}	Transition Time, LOW to HIGH				8	20		8.0	20	ns
t_{THL}	Transition Time, HIGH to LOW				10	20		10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	$I_O \approx$ 300 mA, Note 3	V_S − 10			V_S − 18			mV

Notes
1 All typical values are at V_{CC} = 5 V, T_A = 25°C
2 V_{OH} = 30 V for μA75451A and B, 35 V for μA75461, 80 V for μA75471
3 V_S = 20 V for μA75451A and B, 30 V for μA75461, 55 V for μA75471

μA75452A/B • μA75462 • μA75472
Dual Positive NAND Peripheral Driver

Connection Diagram
8-Pin DIP



(Top View)

Truth Table

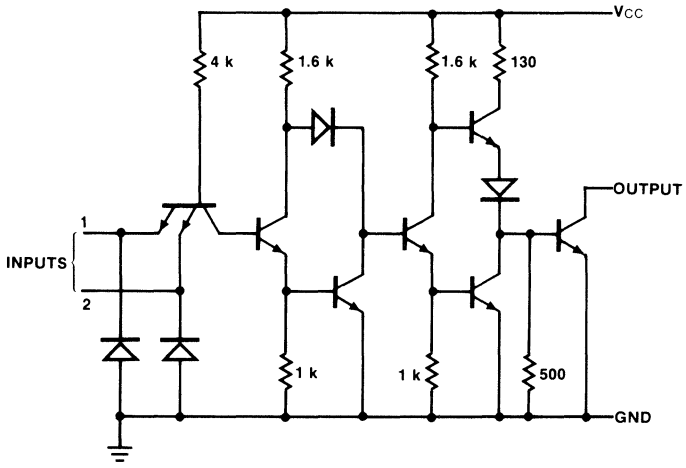
Inputs		Output	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

Order Information

Type	Package	Code	Part No.
μA75452A	Molded DIP	9T	μA75452ATC
μA75452A	Ceramic DIP	6T	μA75452ARC
μA75452B	Molded DIP	9T	μA75452BTC
μA75452B	Ceramic DIP	6T	μA75452BRC
μA75461	Ceramic DIP	6T	μA75461TC
μA75471	Ceramic DIP	6T	μA75471TC

Equivalent Circuit (Each Driver)



Component values shown are nominal All resistor values in ohms

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μA75452A/B
Electrical Characteristics Guaranteed over operating temperature range and supply voltage range, use test table 1, page 1, unless otherwise indicated.

Symbol	Characteristic	Test Figure	Condition (Note 1)	μA75452A			μA75452B			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	7		2			2			V
V_{IL}	Input LOW Voltage	7				0.8			0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = Min, I_{IN} = −12 mA			−1.5			−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = Min V_{IL} = 0.8 V, Note 2			100			100	μA
V_{OL}	Output LOW Voltage	7	V_{CC} = Min, V_{IH} = 2 V I_{OL} = 100 mA		0.25	0.4		0.25	0.4	V
			V_{CC} = Min, V_{IH} = 2 V I_{OL} = 300 mA		0.5	0.7		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = Max, V_{IN} = 5.5 V			1.0			1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = Max, V_{IN} = 2.4 V			40			40	μA
I_{IL}	Input LOW Current	8	V_{CC} = Max, V_{IN} = 0.4 V		−1.0	−1.6		−1.0	−1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = Max, V_{IN} = 0 V		11	14		11	14	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = Max, V_{IN} = 5 V		56	71		56	71	mA

μA75452A/μA75452B
AC Characteristics V_{CC} = 5 V, T_A = 25°C

Symbol	Characteristic	Test Figure	Condition	μA75452A			μA55/75452B			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		25	65		25	35	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				25	50		22	35	ns
t_{TLH}	Transition Time, LOW to HIGH				8	25		5	8	ns
t_{THL}	Transition Time, HIGH to LOW				12	20		7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	$I_O \approx$ 300 mA, Note 3	V_S − 6.5			V_S − 6.5			mV

Notes
1 All typical values are at V_{CC} = 5 V, T_A = 25°C
2 V_{OH} = 30 V for μA75452A and B, 35 V for μA75462, 80 V for μA75472
3 V_S = 20 V for μA75452A and B, 30 V for μA75462, 55 V for μA75472.

μA75462/μA75472
Electrical Characteristics Guaranteed over operating temperature range and supply voltage range, use test table 1, page 1, unless otherwise indicated.

Symbol	Characteristic	Test Figure	Condition (Note 1)	μA75462			μA75472			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	7		2			2.0			V
V_{IL}	Input LOW Voltage	7				0.8			0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = Min, I_{IN} = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = Min V_{IL} = 0.8 V, Note 2			100			100	μA
V_{OL}	Output LOW Voltage	7	V_{CC} = Min V_{IH} = 2 V I_{OL} = 100 mA		0.16	0.4		0.16	0.4	V
			V_{CC} = Min, V_{IH} = 2 V I_{OL} = 300 mA		0.35	0.7		0.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = Max, V_{IN} = 5.5 V			1.0			1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = Max, V_{IN} = 2.4 V			40			40	μA
I_{IL}	Input LOW Current	8	V_{CC} = Max, V_{IN} = 0.4 V		−1.0	−1.6		−1.0	−1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = Max, V_{IN} = 0 V		13	17		13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = Max, V_{IN} = 5 V		65	76		65	76	mA

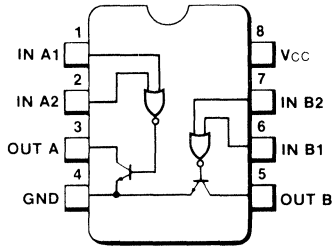
μA75462/μA75472
AC Characteristics V_{CC} = 5 V, T_A = 25°C

Symbol	Characteristic	Test Figure	Condition	μA75462			μA75472			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65		45	65	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				40	50		30	50	ns
t_{TLH}	Transition Time, LOW to HIGH				12	25		13	25	ns
t_{THL}	Transition Time, HIGH to LOW				15	20		10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	$I_O \approx$ 300 mA, Note 3	V_S − 10			V_S − 18			mV

Notes
1 All typical values are at V_{CC} = 5 V, T_A = 25°C.
2 V_{OH} = 30 V for μA75452A and B, 35 V for μA75462, 80 V for μA75472.
3 V_S = 30 V for μA75462 and 55 V for μA75472

μA75453A/B
Dual Positive OR Peripheral Drivers

Connection Diagram
8-Pin DIP



(Top View)

Truth Table

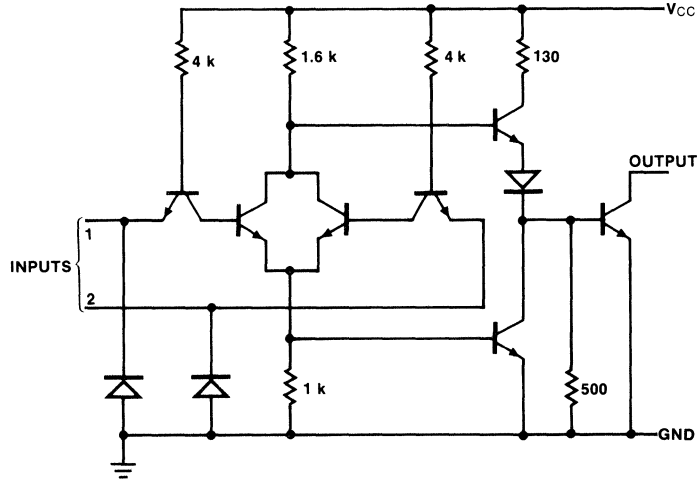
Inputs		Output	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

Order Information

Type	Package	Code	Part No.
μA75453A	Ceramic DIP	6T	μA75453ARC
μA75453A	Molded DIP	9T	μA75453ATC
μA75453B	Ceramic DIP	6T	μA75453BRC
μA75453B	Molded DIP	9T	μA75453BTC

Equivalent Circuit (Each Driver)



Component values shown are nominal All resistor values in ohms

μA75453A/B
Electrical Characteristics Guaranteed over operating temperature range and supply voltage range, use test table 1, page 1, unless otherwise indicated.

Symbol	Characteristic	Test Figure	Condition	Min	Typ (Note)	Max	Unit
V_{IH}	Input HIGH Voltage	7		2			V
V_{IL}	Input LOW Voltage	7				0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = Min, I_{IN} = −12 mA			−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = Min, V_{OH} = 30 V, V_{IH} = 2 V			100	μA
V_{OL}	Output LOW Voltage	7	V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
			V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = Max, V_{IN} = 5.5 V			1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = Max, V_{IN} = 2.4 V			40	μA
I_{IL}	Input LOW Current	8	V_{CC} = Max, V_{IN} = 0.4 V		−1.0	−1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = Max, V_{IN} = 5 V		8.0	11	mA
I_{CCL}	Supply Current, Output LOW		V_{CC} = Max, V_{IN} = 5 V		54	68	mA

μA75453A/B
AC Characteristics V_{CC} = 5 V, T_A = 25°C

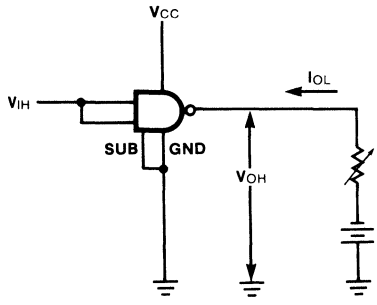
Symbol	Characteristic	Test Figure	Condition	μA75453A			μA75453B			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		20	55		18	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				20	40		16	25	ns
t_{TLH}	Transition Time, LOW to HIGH				8	25		5	8	ns
t_{THL}	Transition Time, HIGH to LOW				12	25		7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S − 6.5			V_S − 6.5			mV

Notes
1 All typical values are at V_{CC} = 5 V, T_A = 25°C
2 V_{OH} = 30 V for μA75453A and B
3 V_S = 20 V for μA75452A and B

Characteristics Measurement Information

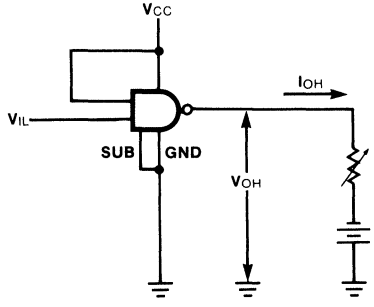
DC Test Circuit (Note)

Fig. 1 V_{IH}, V_{OL}



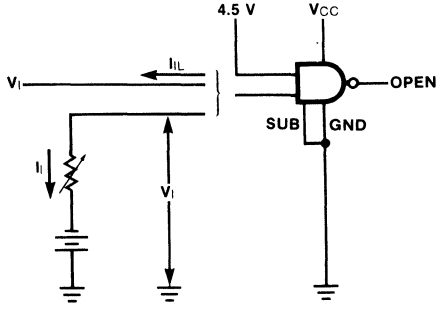
Both inputs are tested simultaneously

Fig. 2 V_{IL}, V_{OH}



Each input is tested separately

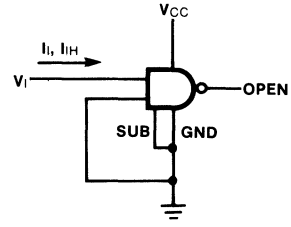
Fig. 3 V_{CD}, I_{IL}



Notes
1 Each input is tested separately.
2 When testing V_{CD}, input not under test is open

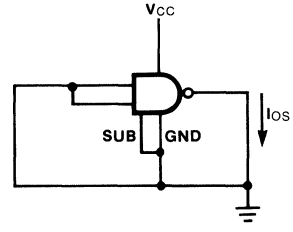
Note
Arrows indicate actual direction of current flow Current into a terminal is a positive value

Fig. 4 I_I, I_{IH}



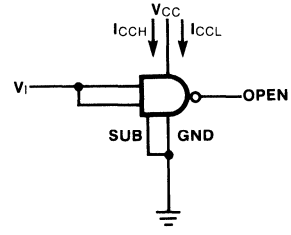
Each input is tested separately

Fig. 5 I_{OS}



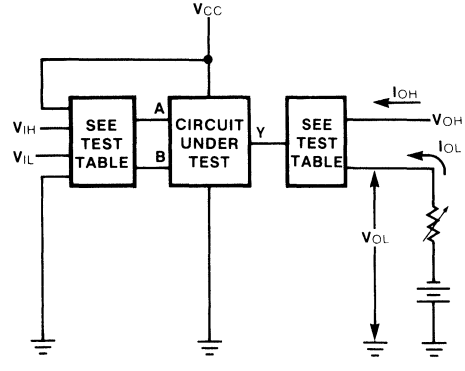
Each gate is tested separately

Fig. 6 I_{CCH}, I_{CCL}



Both gates are tested simultaneously

Fig. 7 V_{IH}, V_{IL}, I_{OH}, V_{OL}



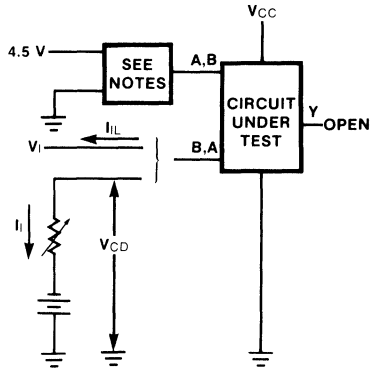
Note
Each input is tested separately.

Characteristics Measurement Information (Cont.)

Test Table 2

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
μA754X1	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
μA754X2	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
μA754X3	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}

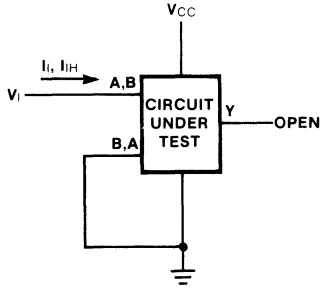
Fig. 8 V_{CD}, I_{IL}



Notes

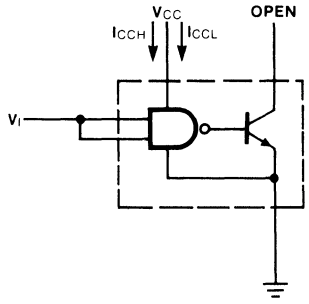
1 Each input is tested separately
2 When testing I_{IL} μA75400, the input not under test is grounded For all other circuits it is at 4 5 V
3 When testing V_{CD}, input not under test is open

Fig. 9 I_I, I_{IH}



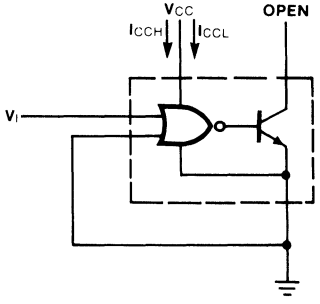
Each input is tested separately.

Fig. 10 I_{CCH}, I_{CCL} for AND, NAND Circuits



Both gates are tested simultaneously

Fig. 11 I_{CCH}, I_{CCL} for OR, NOR Circuits



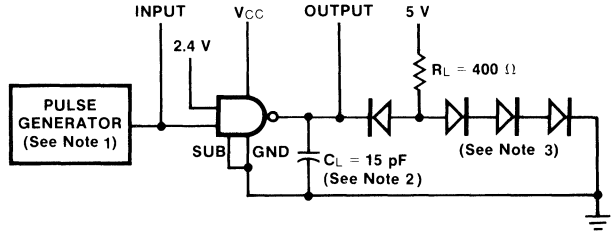
Both gates are tested simultaneously

6

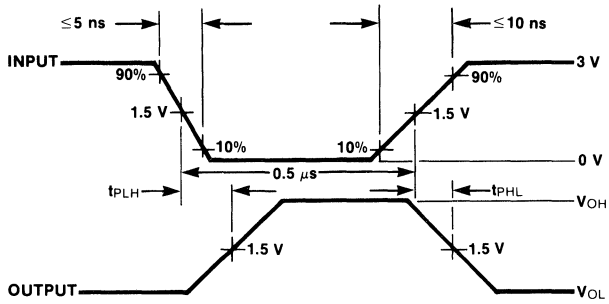
Characteristics Measurement Information
Switching Characteristics

Fig. 12 Propagation Delay Times, Each Gate (μA55450, μA75450 Only)

Test Circuit



Voltage Waveforms



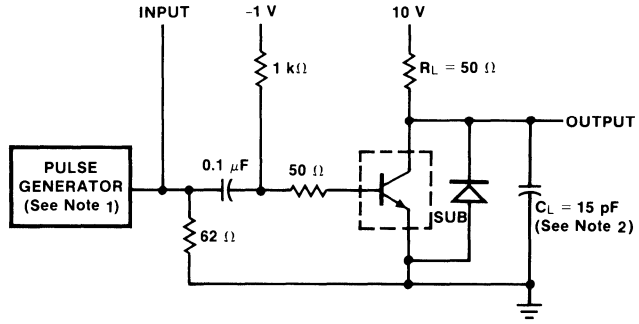
Notes

1 The pulse generator has the following characteristics
PRR = 1 MHz, $Z_{OUT} \approx 50\ \Omega$
2 C_L includes probe and jig capacitance
3 All diodes are FD777

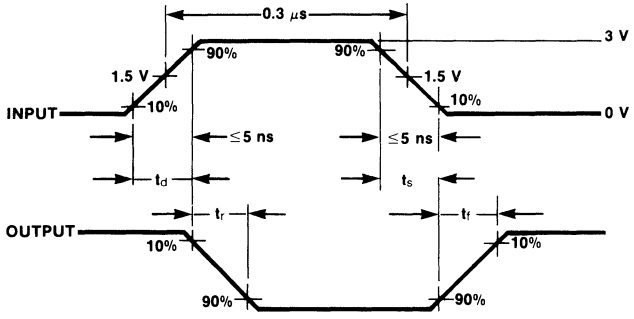
Characteristics Measurement Information
Switching Characteristics (Cont.)

Fig. 13 Switching Times, Each Transistor (μA75450 Only)

Test Circuit



Voltage Waveforms



Notes

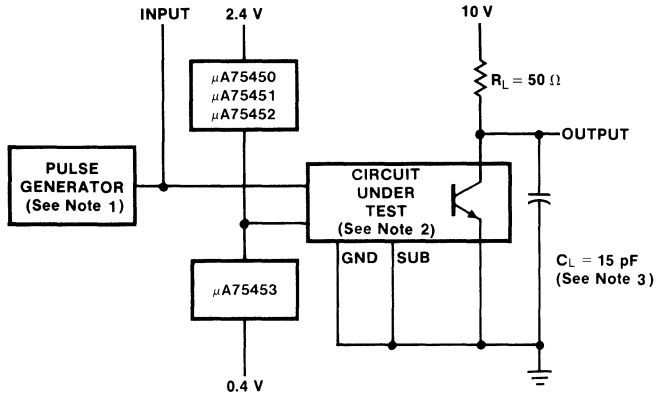
1 The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\ \Omega$

2 C_L includes probe and jig capacitance

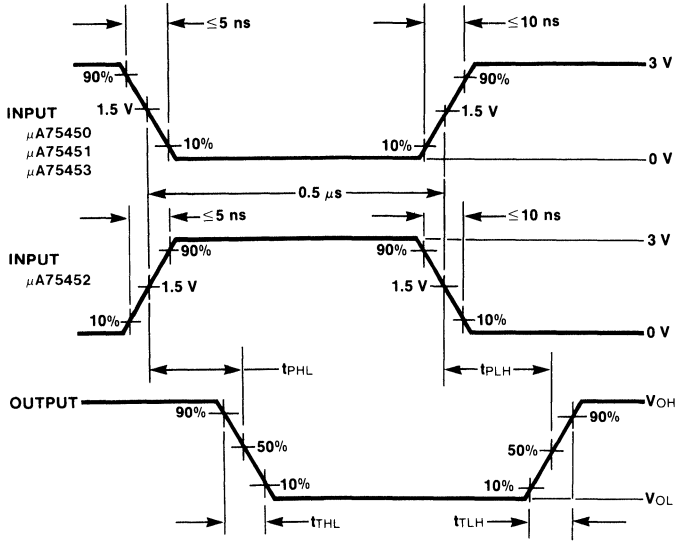
Characteristics Measurement Information
Switching Characteristics (Cont.)

Fig. 14 Switching Times of Complete Drivers

Test Circuit



Voltage Waveforms



Notes

1 The pulse generator has the following characteristics
PRR = 1 MHz, $Z_{OUT} \approx 50\ \Omega$

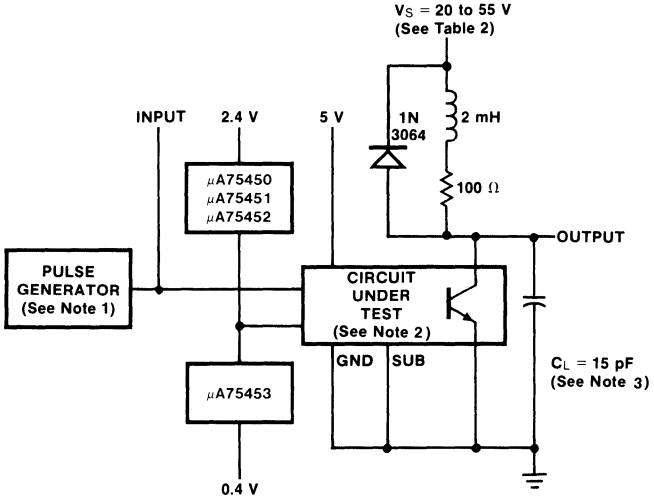
2 When testing μA75450, connect output Y to transistor base with a 500Ω resistor to ground

3 C_L includes probe and jig capacitance

Characteristics Measurement Information
Switching Characteristics (Cont.)

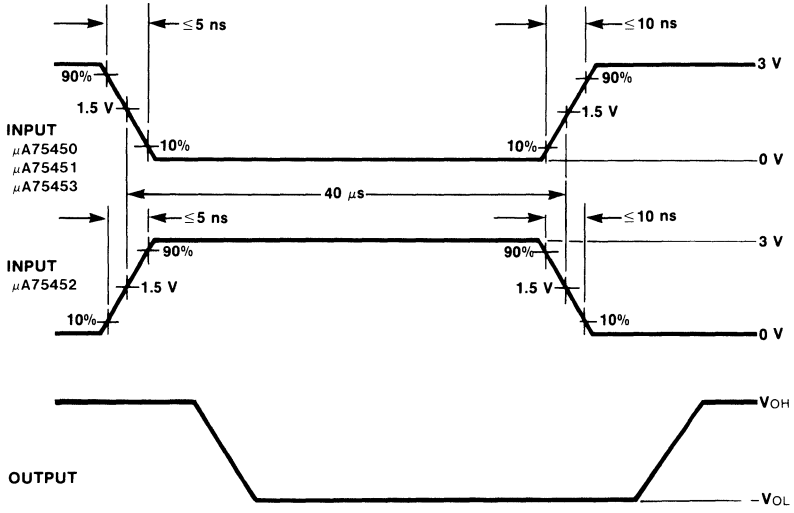
Fig. 15 Latch-up Test of Complete Drivers

Test Circuit



V_S = 20 to 55 V
(see Table 2)

Voltage Waveforms



Notes

1 The pulse generator has the following characteristics
PRR = 12 5 kHz, $Z_{OUT} \approx 50\ \Omega$

2 When testing μA75450, connect output Y to transistor base with a 500 Ω resistor from there to ground, and ground the substrate terminal.

3 C_L includes probe and jig capacitance

FAIRCHILD

A Schlumberger Company

μA75491 • μA75492 MOS to LED Segment and Digit Drivers

Interface Products

Description

The 75491 LED Quad Segment Digit Driver interfaces MOS signals to common cathode LED displays. High output current capability makes the devices ideal in time multiplex systems using segment address or digit scan method of driving LEDs to minimize the number of drivers required.

The 75492 Hex LED/Lamp Driver converts MOS signals to high output currents for LED display digit select or lamp select. The high output current capability makes this device ideal in time multiplex systems using segment address or digit scan method of driving LEDs to minimize the number of drivers required.

μA75491

- **50 mA SOURCE OR SINK CAPABILITY**
- **LOW INPUT CURRENTS FOR MOS COMPATIBILITY**
- **LOW STANDBY POWER**
- **FOUR HIGH GAIN DARLINGTON CIRCUITS**

μA75492

- **250 mA SINK CAPABILITY**
- **MOS COMPATIBLE INPUTS**
- **LOW STANDBY POWER**
- **SIX HIGH GAIN DARLINGTON CIRCUITS**

Truth Tables

μA75491

INPUTS 1A-4A	OUTPUTS 1E-4E	OUTPUTS 1C-4C
L	L	H
H	H	L

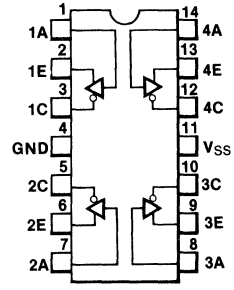
μA75492

INPUTS 1A-6A	OUTPUTS 1Y-6Y
L	H
H	L

H = HIGH Level, L = LOW Level

Connection Diagrams 14-Pin DIP

μA75491

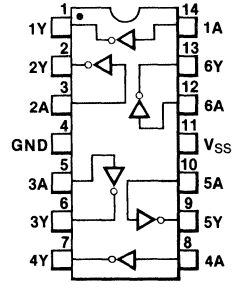


(Top View)

Order Information

Type	Package	Code	Part No.
μA75491	Molded DIP	9A	μA75491PC

μA75492



(Top View)

Order Information

Type	Package	Code	Part No.
μA75492	Molded DIP	9A	μA75492PC

Absolute Maximum Ratings

Supply Voltage	10 V
Input Voltage (Note 1)	−5.0 to V_{SS}
Collector (Output) Voltage (Note 2)	10 V
Collector (Output) to Input Voltage	10 V
Emitter to Ground Voltage ($V_{IN} \geq 5.0$ V) 75491	10 V
Emitter to Input Voltage 75491	5.0 V
Continuous Collector Current 75491,	50 mA
75492	250 mA
Collector Output Current (75492) all collectors	600 mA
Continuous Total Power Dissipation (Note 3)	800 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature Molded DIP (Soldering, 10 s)	260°C

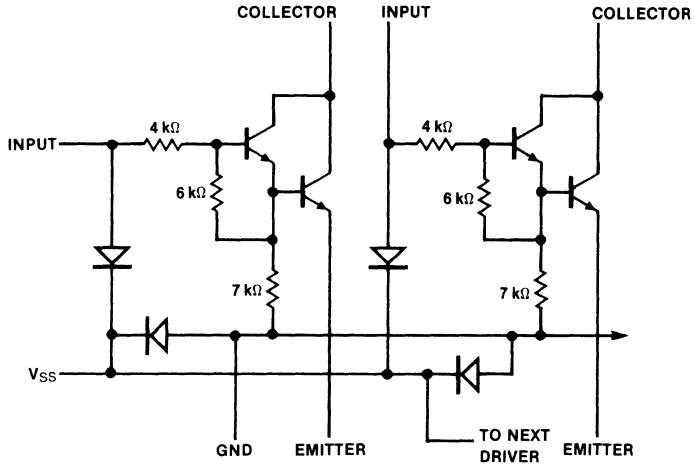
Notes

1 The input is the only device terminal which may be negative with respect to ground

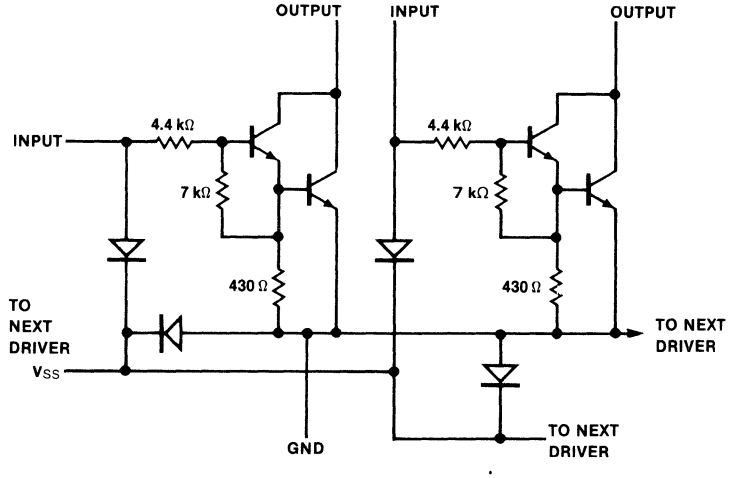
2 Voltage values are with respect to network ground terminal unless otherwise noted

3 Above 60°C ambient temperature, derate linearly at 8 3 mW/°C

Equivalent Circuit (1/2 of μA75491)



Equivalent Circuit (1/3 of μA75492)



μA75491 DC Characteristics V_{SS} = 10 V, T_A = 0°C to 70°C unless otherwise specified

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_{CEL}	LOW Level Collector to Emitter Voltage	V_{IN} = 8.5 V through 1.0 kΩ I_{OL} = 50 mA, V_E = 5.0 V, T_A = 25°C			0.9	1.2	V
		V_{IN} = 8.5 V through 1.0 kΩ I_{OL} = 50 mA, V_E = 5.0 V			0.9	1.5	V
I_{CH}	Collector HIGH Current	V_{CH} = 10 V	V_E = 0, V_{IN} = 0.7 V			100	μA
		V_{CH} = 10 V	V_E = 0, I_{IN} = 40 μA			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10 V	I_{OL} = 20 mA		2.0	3.3	mA
I_{ER}	Reverse Biased Emitter Current	I_C = 0, V_{IN} = 0, V_E = 5.0 V				100	μA
I_{SS}	Supply Current					1.0	mA

μA75491 AC Characteristics V_{SS} = 7.5 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PHL}	Propagation Delay Time	R_L = 200 Ω, V_{INH} = 4.5 V		20		ns
t_{PLH}		C_L = 15 pF, V_E = 0		100		ns

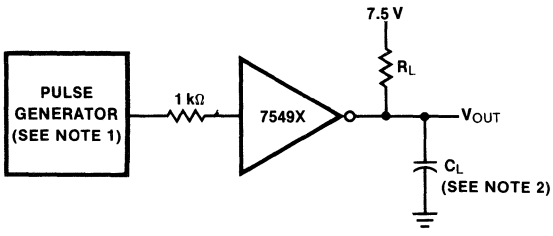
μA75492 DC Characteristics V_{SS} = 10 V, T_A = 0°C to 70°C unless otherwise specified

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_{OL}	Output LOW Voltage	V_{IN} = 6.5 V through 1.0 kΩ I_{OL} = 250 mA, T_A = 25°C			0.9	1.2	V
		V_{IN} = 6.5 V through 1.0 kΩ I_{OL} = 250 mA			0.9	1.5	V
I_{OH}	Output HIGH Current	V_{OH} = 10 V	I_{IN} = 40 μA			200	μA
		V_{OH} = 10 V	V_{IN} = 0.5 V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10 V	I_{OL} = 20 mA		2.0	3.3	mA
I_{SS}	Supply Current					1.0	mA

μA75492 AC Characteristics V_{SS} = 7.5 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PHL}	Propagation Delay Time	R_L = 39 Ω, V_{IN} = 7.5 V		30		ns
t_{PLH}		C_L = 15 pF		300		ns

Test Circuit

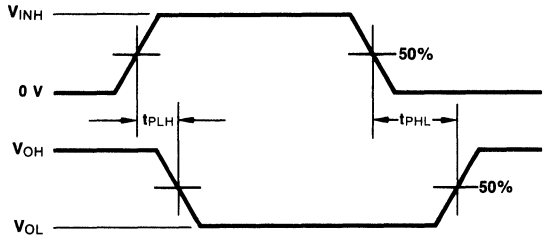


Notes

1 The pulse generator has the following characteristics. Z_{OUT} = 50 Ω, PRR = 100 kHz, t_w = 1 μs

2 C_L includes probe and jig capacitance.

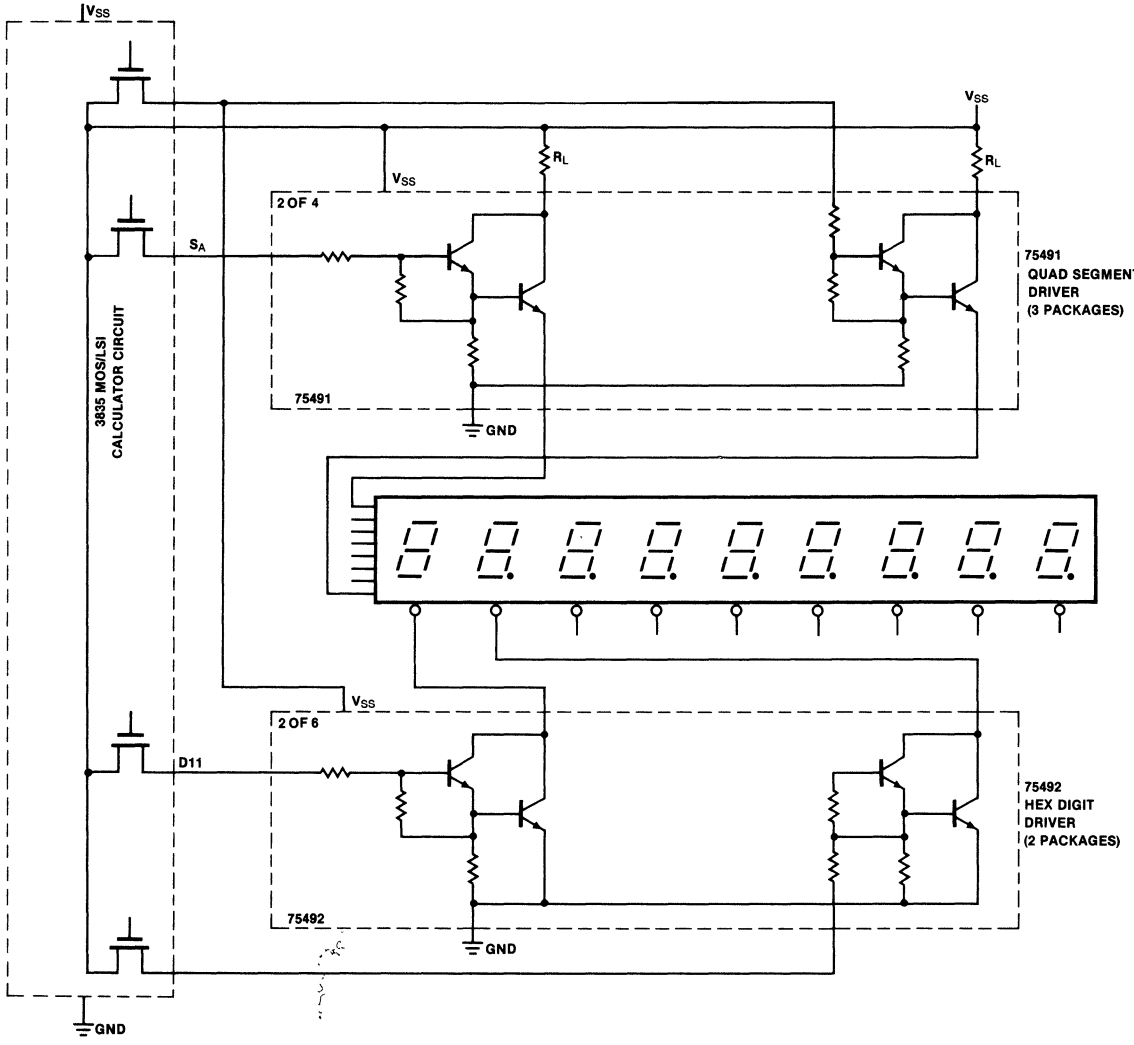
Waveform



Typical Application

Interfacing Between MOS Calculator Circuit and LED Multi-Digit Display

This example of time multiplexing the individual digits in a visible display minimizes display circuitry. Up to twelve digits of a 7-segment display plus decimal point may be displayed using only three 75491 and two 75492 drivers.



FAIRCHILD
A Schlumberger Company

μA438
Serial Input LCD Driver

Interface Products

Description

The μA438 is a CMOS/LSI circuit that drives an LCD display, usually under microprocessor control. The part acts as a "smart" peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms. The μA438 can drive any standard or custom parallel drive LCD display whether it be field effect or dynamic scattering, 7, 9, 13 or 16 segment characters, decimals, leading + or −, or special symbols. Several μA438s can be cascaded. The ac frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the LCD ϕ input, which controls the frequency of an internal oscillator.

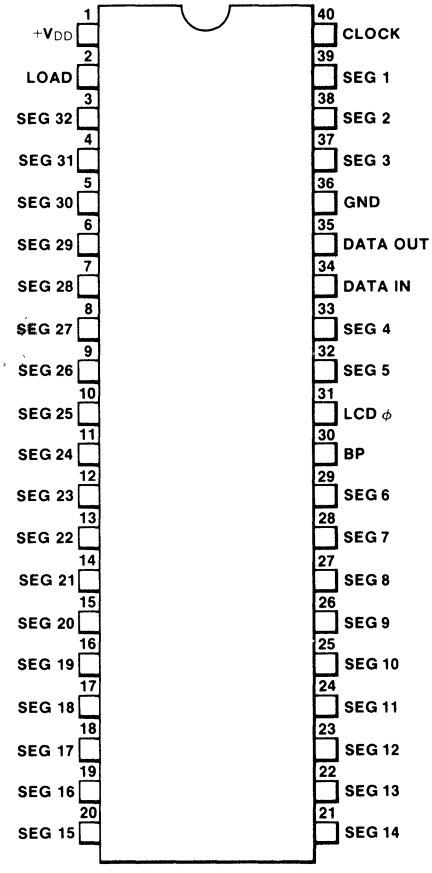
The μA438 can also be used as a column driver in a multiplexed LCD display. In this application it acts as a "dumb" peripheral since timing and refresh must be supplied externally.

- **DRIVES UP TO 32 LCD SEGMENTS OF ARBITRARY CONFIGURATION**
- **CMOS CONSTRUCTION FOR WIDE SUPPLY VOLTAGE RANGE LOW-POWER OPERATION HIGH-NOISE IMMUNITY WIDE TEMPERATURE RANGE**
- **CMOS, NMOS, AND TTL COMPATIBLE INPUTS**
- **CASCADABLE**
- **CHOICE OF ON-CHIP OR EXTERNAL OSCILLATOR**
- **REQUIRES ONLY 3-CONTROL LINES**

Absolute Maximum Ratings

Supply Voltage, V_{DD}	−0.3 V to 15 V
Input Voltage, (CLK, Data In, Load Inputs)	$+V_{DD}$ −15 V to $+V_{DD}$ + 0.3 V
Input Voltage (LCD ϕ Input)	−0.3 V to $+V_{DD}$ +0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +70°C
Pin Temperature (Soldering, 60 s)	300°C

Connection Diagram
40-Pin DIP

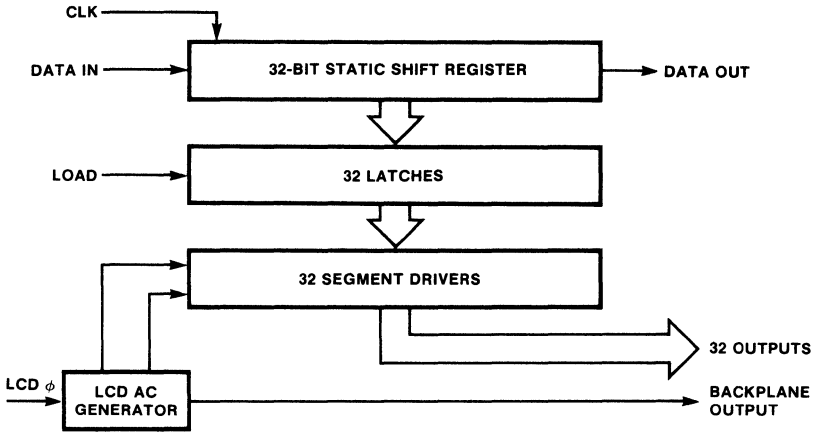


(Top View)

Order Information

Type	Package	Code	Part No.
μA438	Ceramic DIP	6I	μA438JC

Block Diagram



Electrical Characteristics V_{DD} = +5 V unless otherwise specified

Symbol	Characteristics		Condition	Min	Max	Unit
V_{DD}	Supply Voltage			3	13	V
I_{DD1} I_{DD2}	Supply Current		LCDϕ Osc at <15 kHz LCDϕ Driven		60 10	μA μA
V_{IH}	Input HIGH Level	Clock Data Load		0.5 V_{DD}	V_{DD}	V
V_{IL}	Input LOW Level			$V_{DD}-15$	0.2 V_{DD}	V
I_L	Input Current				5	μA
C_I	Input Capacitance				5	pF
R_{ON}	Segment Output Impedance		I_L = 10 μA		40	kΩ
R_{ON}	Backplane Output Impedance				3	kΩ
R_{ON}	Data Out Output Impedance				3	kΩ
f	Clock Rate		50% Duty Cycle	dc	1.5	MHz
t_{DS}	Data Set-up Time		Data change to Clock falling edge	150		ns
t_{DH}	Data Hold Time			100		ns
t_{pw}	Load Pulse Width			200		ns
t_{pd}	Data Out Propagation Delay		C_L = 15 pF		500	ns
V_{IH}	LCDϕ Input HIGH Level			0.9 V_{DD}		V
V_{IL}	LCDϕ Input LOW Level				0.1 V_{DD}	V
I_L	LCDϕ Input Current		Driven		5	μA

Applications

1. The shift register loads, shifts, and outputs on the falling edge of Clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A logic 1 on Load causes a parallel load of the data in the shift register into the latches that control the segment drivers.
4. If LCD ϕ is driven it is in phase with the Backplane Output.
5. To cascade units, (a) connect the Data Out of one chip to Data In of next chip, and (b) either connect Backplane of one chip to LCD ϕ of all other chips (thus one capacitor provides frequency control for all chips) or connect LCD ϕ of all chips to a common driving signal. If the former is chosen, don't tie all backplanes together (just use one of them) and drive LCD ϕ with a Backplane output that doesn't go to the actual backplane. (This reduces the dc component of driving signals).
6. The supply voltage of the μA438 is equal to half the peak-to-peak driving voltage of the LCD. If the μA438 supply voltage is less than the swing of the controlling logic signals, the positive supply leads of the logic circuitry and the μA438 should be tied in common, not the ground (or negative) supply leads. Be careful that input level specifications are met.
7. The LCD ϕ pin can be used in two modes, driven or oscillating. If LCD ϕ is driven, the circuit will sense this condition and pass the LCD ϕ input to the backplane output. If the LCD ϕ pin is allowed to oscillate, its frequency is inversely proportional to capacitance and the LCD driving waveforms have a frequency 2^8 slower than the oscillator itself. The approximate relationship is $f_{out}(Hz) = 2500/c(pF)$.
8. Avoid changing Data In when clock is falling. Avoid changing Load when clock is falling.
9. The number of a segment corresponds to how many clock pulses have occurred since its data was present at the input. For example, the data on SEG 19 was the Data In 19 clock pulses earlier.

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μA9650
4-Bit Current Source

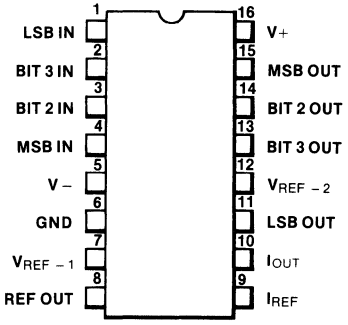
Data Aquisition Products

Description

The μA9650 is a high speed, 4-Bit Precision Current Source, intended for use in d/a and a/d converters with up to 12-bit accuracy. It is constructed on a single silicon chip, using the Fairchild Planar epitaxial process and consists of a reference transistor and four logic operated precision current sources connected to a single output summing line. Logic inputs are fully TTL compatible under all temperature and supply conditions. A clamp circuit is provided to prevent turn on latchup on the reference input.

- **200 ns SETTLING TIME (12 ± 1/2 LSB)**
- **VARIABLE BIT CURRENTS**
- **REFERENCE COMPENSATION**
- **TTL COMPATIBLE**

Connection Diagram
16-Pin DIP



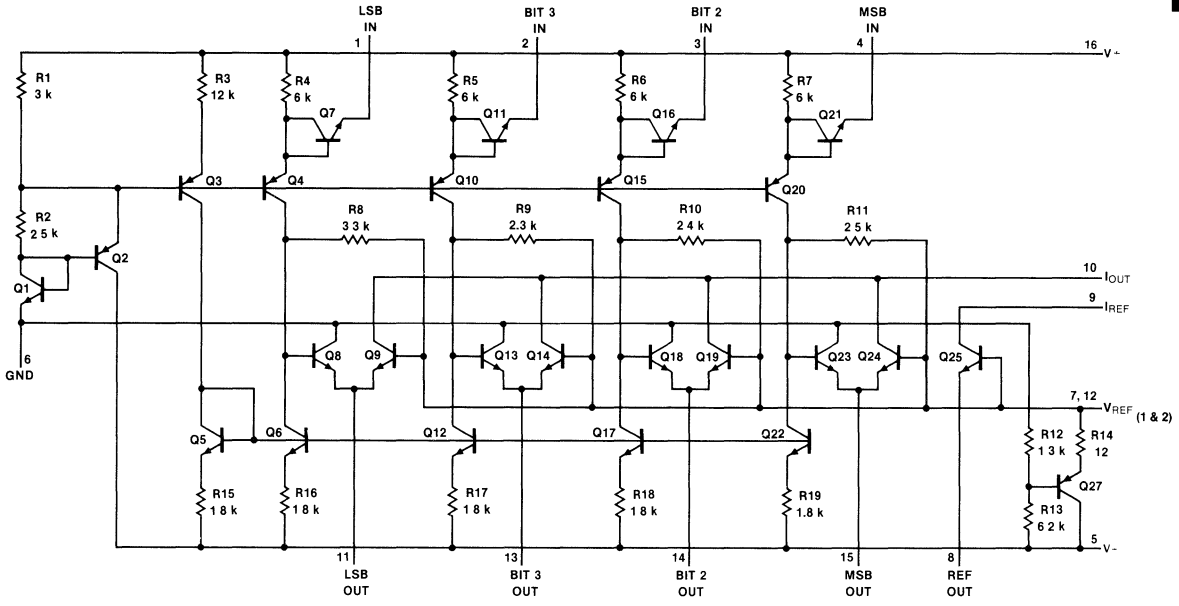
(Top View)

Order Information

Type	Package	Code	Part No.
μA9650-1C	Ceramic DIP	6B	μA9650-1DC
μA9650-2C	Ceramic DIP	6B	μA9650-2DC
μA9650-3D	Ceramic DIP	6B	μA9650-3DC

7

Equivalent Circuit



Absolute Maximum Ratings

$V_{CC}+$	+7 V
$V_{CC}-$	−18 V
MSB Current	2.0 mA
Logic Input Voltage	+5.5 V
Power Dissipation (Note 1)	730 mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to 70°C
Pin Temperature (Soldering, 60 s)	+300°C
V_{REF} Inputs	+7 V to V−
Output (V_{REF} voltage ≥ −7.0 V)	+18 V to V_{REF}

Truth Table

Logic Input	Nominal Output Current (mA)	Logic Input	Nominal Output Current (mA)
0000	1.875	1000	0.875
0001	1.750	1001	0.750
0010	1.625	1010	0.625
0011	1.500	1011	0.500
0100	1.375	1100	0.375
0101	1.250	1101	0.250
0110	1.125	1110	0.125
0111	1.000	1111	0.000

μA9650 Kits Required to Build d/a-a/d Converters

Temperature Range	Type and No. of Units		
0° C to +70° C	9650-1C	9650-2C	9650-3C
Accuracy to:			
8 Bits	0	0	2
10 Bits	0	1	2
12 Bits	1	1	1

Notes

1. Rating applies for ambient temperature to 70°C. Derate linearly at 9.1 mW/°C for ambient temperatures above 70°C.

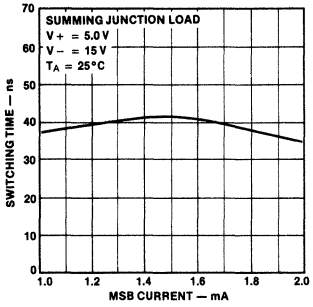
μA9650-1C • μA9650-2C • μA9650-3C
Electrical Characteristics T_A = 20°C, Power Supply Range, 4.5 V, −4.5 V, −14 V to 5.5 V, −16 V, unless otherwise specified.

Characteristic (see definitions)	Condition (Type)	Min	Typ	Max	Unit
Linearity	(μA9650-1C) (μA9650-2C) (μA9650-3C)			±0.01 ±0.05 ±0.2	% of FSI % of FSI % of FSI
Full Scale Output Current Error	(μA9650-1C) (μA9650-2C) (μA9650-3C)			±0.1 ±0.2 ±0.4	% % %
Power Supply Coefficient of Full Scale Output Current	(μA9650-1C) (μA9650-2C, μA9650-3C)			±0.003 ±0.012	%/V %/V
V_{BE} Range			620		mV
h_{FE} of Reference Transistor			1000		
Output Impedance	All Bits On		5.0		MΩ
The following specifications apply for 0°C ≤ T_A ≤ 70°C					
Accuracy	(μA9650-1C) (μA9650-2C) (μA9650-3C)			±0.025 ±0.1 ±0.3	% of FSI % of FSI % of FSI
Full Scale Output Current Error	(μA9650-1C) (μA9650-2C) (μA9650-3C)			0.2 0.3 0.6	% % %
Power Supply Coefficient of Full Scale Output Current	(μA9650-1C) (μA9650-2C, μA9650-3C)			±0.006 ±0.024	%/V %/V
Input LOW Voltage	Each Bit On			0.8	V
Input HIGH Voltage	Each Bit Off	2.0			V
Input LOW Current	V_{IL} = 0.4 V			−1.6	mA
Input HIGH Current	V_{IH} = 2.4 V			40	μA
Output Current	Bit 1 (MSB) Bit 2 Bit 3 Bit 4 (LSB)		1.0 0.5 0.25 0.125	2.0 1.0 0.5 0.25	mA mA mA mA
Output Current	All Bits Off (μA9650-1C) (μA9650-2C, μA9650-3C)		 5.0 5.0	 250 500	 nA nA
Output Voltage	Feeding Op Amp Summing Junction Resistive Load	 −4.0	0	 V+	V V
Reference Current	Using Compensation Transistor		1.0		mA
V_{REF} Current			±1.0	±2.2	mA
Reference Limit Current	V_{REF} = 0 V	20		75	mA
Positive Supply Current	(μA9650-1C, μA9650-2C) (μA9650-3C)			8.0 10	mA mA
Negative Supply Current	(μA9650-1C, μA9650-2C) (μA9650-3C)			−11 −15	mA mA

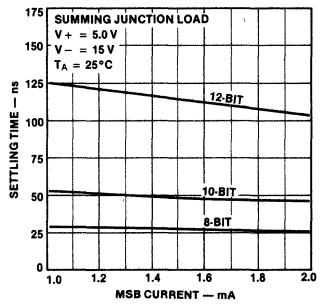
7

Typical Performance Curves

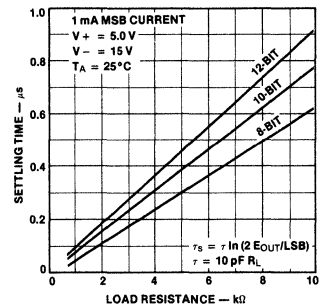
Switching Time as a Function of MSB Current (50% In to 10% Out)



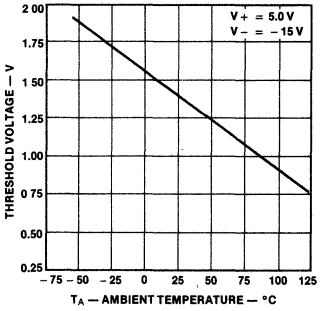
Output Current Settling Time as a Function of MSB Current (0 to FSI Output ± 1/2 LSB)



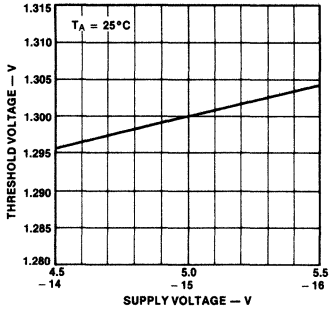
Settling Time as a Function of Load Resistance (0 to FSI Output ± 1/2 LSB)



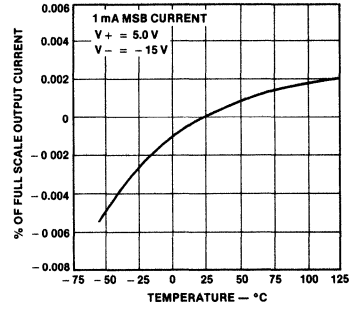
Input Logic Threshold Voltage as a Function of Ambient Temperature



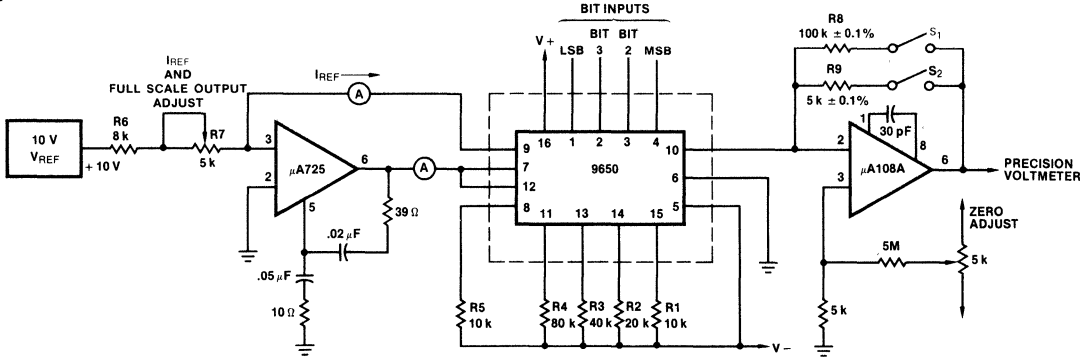
Input Logic Threshold Voltage as a Function of Supply Voltage



Full Scale Output Current Drift as a Function of Ambient Temperature



Typical DC Test Circuit

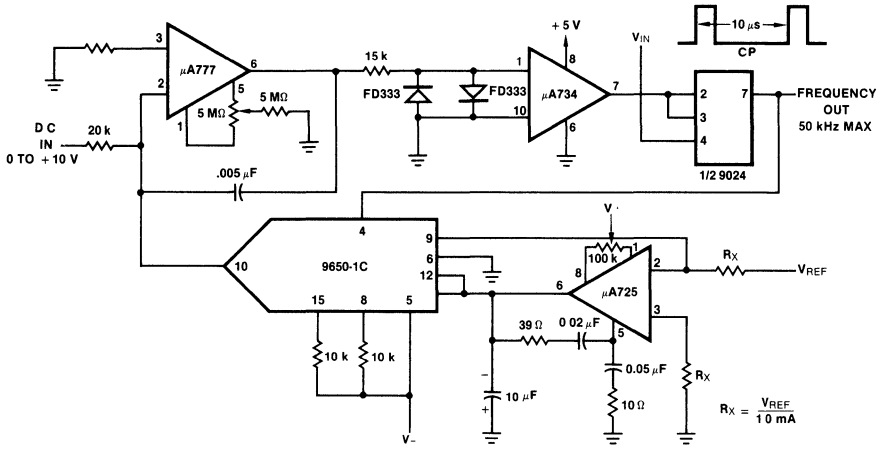


Notes

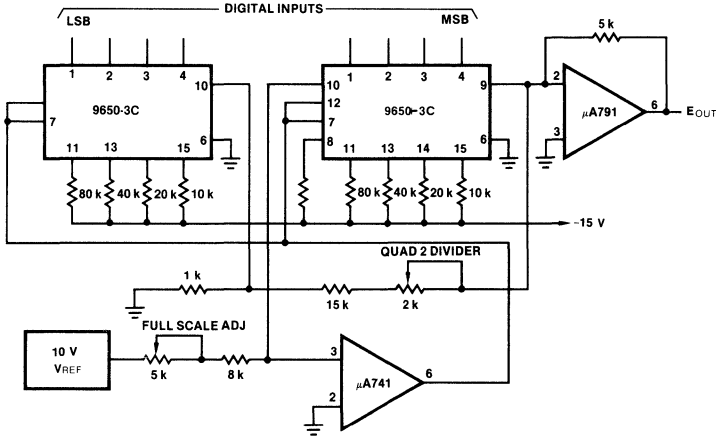
1. Required resistor ratio tolerances of R_1-R_5 to test the various grades are as follows:
   9650-1C, R_5 to R_2 to R_1 — ±0.005%, R_3 to R_1 — ±0.01%, R_4 to R_1 — ±0.02%.
   9650-2C, R_5 to R_2 to R_1 — ±0.025%, R_3 to R_1 — ±0.05%, R_4 to R_1 — ±0.1%.
   9650-3C, R_5 to R_2 to R_1 — ±0.1%, R_3 to R_1 — ±0.2%, R_4 to R_1 — ±0.4%.
2. S_1 closed and S_2 open for output current (all Bits off) tests only.

Typical Applications

Voltage to Frequency Converter

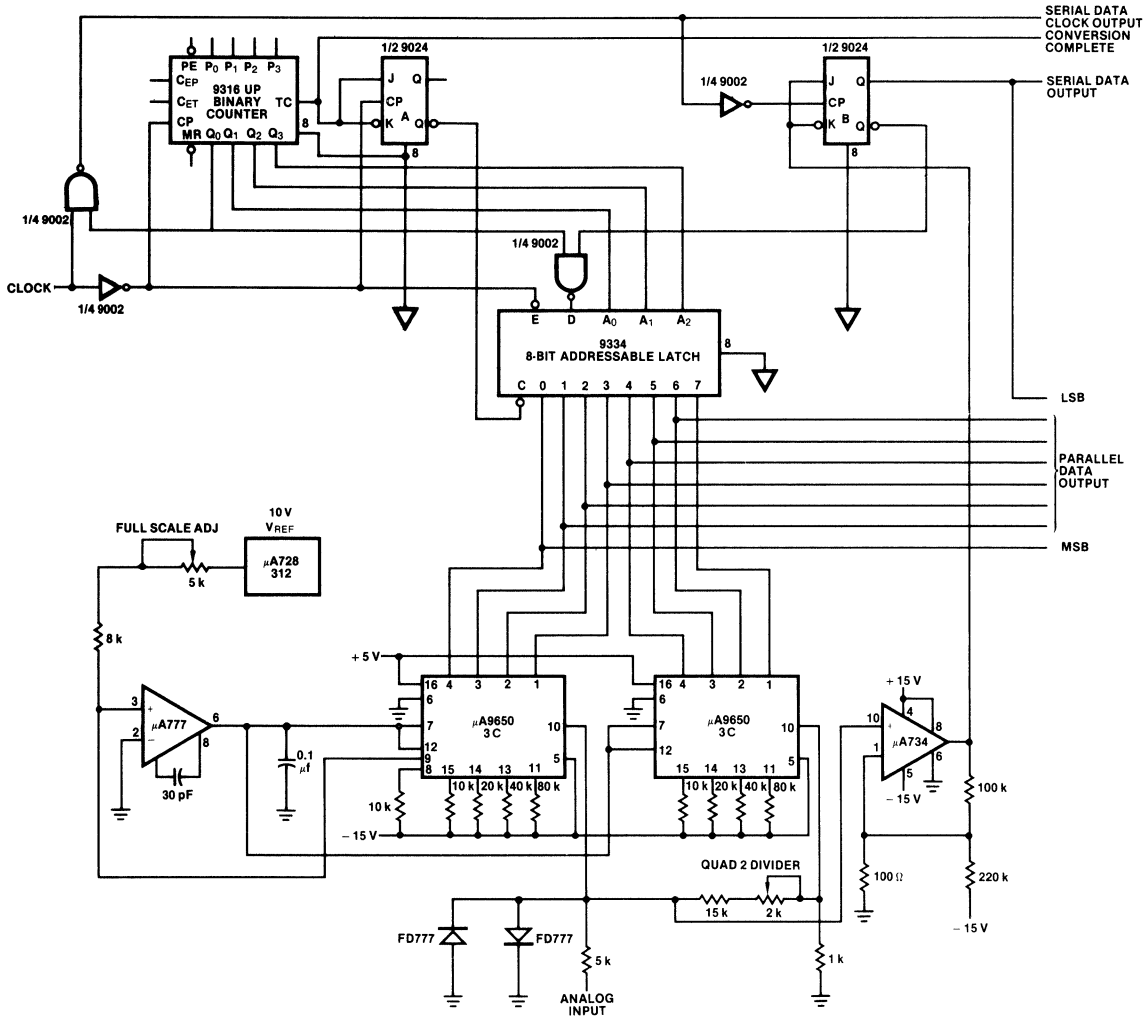


8-Bit d/a Converter



Typical Applications (Cont.)

8-Bit a/d Converter



Note

Digital GND indicated by ▽

Analog GND indicated by ⏚

FAIRCHILD
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μA9706 8-Channel, 12-Bit D/A Converters

Data Aquisition Products

Description

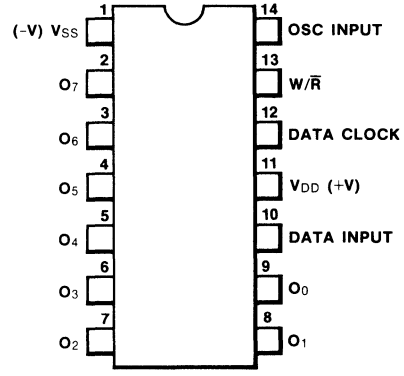
The μA9706 is a d/a converter which allows a microprocessor system to interface and control analog systems. The μA9706 is programmed by 9-bit words, accepted in a serial format, providing conversions on all channels simultaneously and continuously as long as the oscillator signal is present. Digital-to-analog conversion is accomplished using a pulse-width ratio technique for directly controlling the duty cycle of the output pulse streams. Each channel, when appropriately filtered, supplies 6-bit resolution, or 64 discrete analog levels. By properly summing two outputs, the resolution may be controlled up to 12 bits, or 4096 discrete levels. Each channel output maintains 12-bit, or ±.01% full-scale, accuracy.

- **MICROPROCESSOR COMPATIBLE**
- **CMOS TECHNOLOGY**
- **LOW COST**
- **INDEPENDENT CHANNEL OPERATION**
- **LINEARITY ±0.01%**
- **EXPANDABLE TO 12-BIT RESOLUTION**
- **INTERNAL MEMORY**
- **SINGLE SUPPLY +5 V**
- **EXCELLENT STABILITY NO ADJUSTMENTS**

Absolute Maximum Ratings

V_{DD} Relative to V_{SS}	−0.3 V to 5.5 V
Digital Input Range	−0.3 V to V_{DD} +0.3 V
Output Sink or Source Current	25 mA
Operating Temperature	0°C to 85°C
Storage Temperature	−65°C to +150°C
Pin Temperature (Soldering)	
Ceramic DIP (60 s)	300°C
Molded DIP (10 s)	260°C

Connection Diagram
14-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA9706	Molded DIP	9A	μA9706PC
μA9706	Ceramic DIP	7A	μA9706DC

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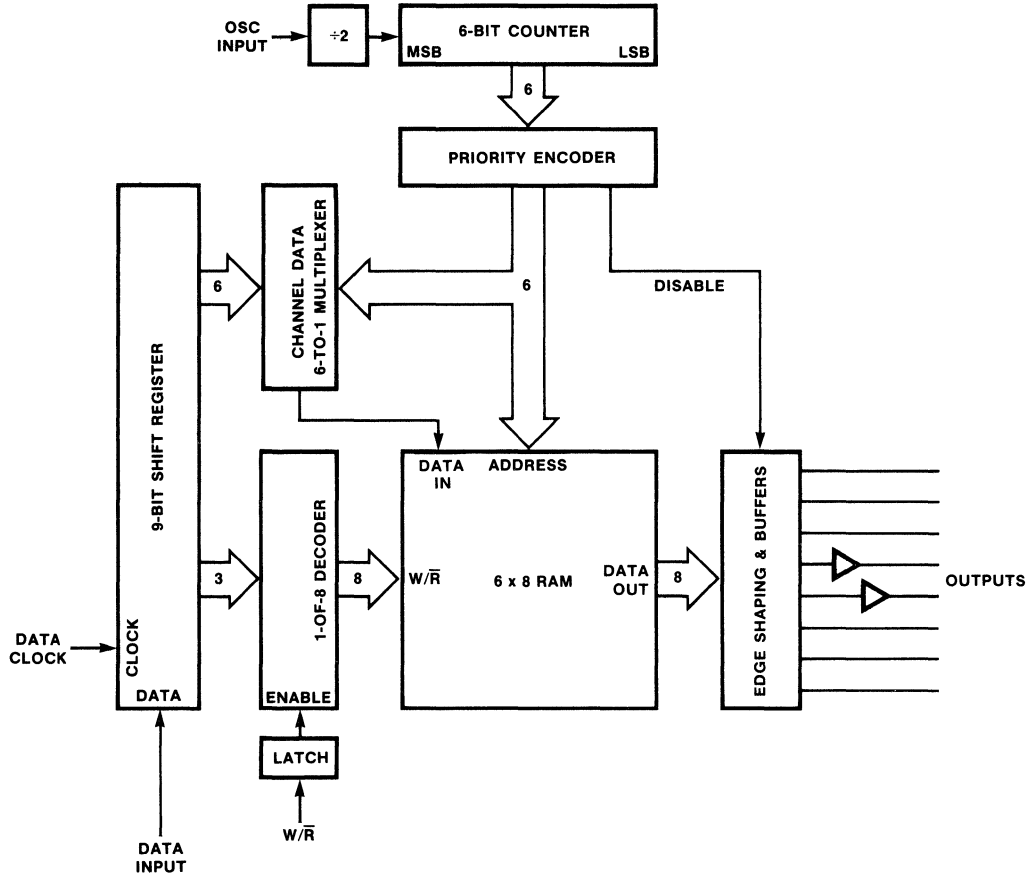
Functional Diagram



Functional Description

The μA9706 consists of seven functional blocks: a 6-bit binary counter, a pulse distributor called a priority encoder, 6 x 8 RAM, 1-of-8 channel address decoder, 6-to-1 channel-data multiplexer, 9-bit input shift register, and a set of eight output buffers.

The pulse-width-ratio conversion scheme divides the conversion cycle into binary-weighted time intervals and associates each time interval with a bit position in the 6-bit control word. The control word residing in RAM is then addressed, bit by bit, each bit addressed for the associated time interval. The value of each bit, "1" or "0," controls the output, HIGH or LOW, during this time interval (see *Figure 1*). In this manner, an output pulse stream is generated with a duty cycle defined by the control word. When the pulse stream is filtered, a dc value is extracted that is proportional to the duty cycle of the pulse stream and, hence, proportional to the control word.

The 6-bit counter generates the fundamental time intervals for the system and may be driven by any open-collector TTL or CMOS logic that produces a square-wave signal with a frequency in the range of 50 kHz to 2 MHz. The time intervals (binary-weighted pulse widths) generated by the counter are decoded by the priority encoder which serves two functions. First, it ensures that each of the six time intervals (control pulses) is used once during the conversion cycle. Second, it distributes the control pulses to both the channel-data multiplexer and to the column-address inputs of the 6 x 8 RAM.

The channel-data multiplexer is enabled during the write mode so that the 6-bit control word may be written. The 6 x 8 RAM provides the storage capability required for the converter to operate independently of the microprocessor, once the control information has been transferred. Since the control information is stored in RAM, simultaneous conversions continue on all eight channels, unaided by the microprocessor unless changes are required. This is accomplished by addressing a single bit in each of the control words and reading the results out in parallel during each time

interval in the conversion cycle. The total cycle time, which is the sum of the six binary-weighted time intervals plus a unit interval (64 clock periods), requires 128 oscillator periods, since the basic oscillator frequency is divided by a factor of two before driving the counter. Conversions may be completed in as little as 64 μs when operating at a 2 MHz clock rate. The control words read from the RAM are directed to the output buffers, six of which have 1 kΩ and two have 50 Ω output impedances. In general, these buffers should drive load impedances larger than the output impedance to reduce the errors caused by the finite output impedance.

Each output is capable of providing 64 discrete output levels representing 6-bit resolution. Since each output pulse stream is accurate to 12 bits, it is possible to sum two outputs and expand the resolution to 12 bits, providing 4096 discrete output levels. This may be easily accomplished by weighing one of the outputs by a factor of 1/64 before summing.

Loading data is a simple procedure that does not affect the conversion cycle. For the μA9706, the 6-bit control word (channel data) and the 3-bit channel address are serially transferred to the 9-bit shift register on the HIGH-to-LOW transitions of the data clock *(Figure 2)*. The data clock has a maximum frequency of 125 kHz with a minimum HIGH and LOW time of 4 μs. Once the nine bits of data have been transferred into the shift register, the data clock must remain static until the write operation is completed to prevent the data from being shifted out of the register. The write mode may be selected after a minimum setup time of 1 μs and is enabled by a HIGH-going $W/\overline{R}$ control pulse. This sets an internal latch that enables the channel-address decoder, which decodes the 3-bit binary channel address, therefore effecting the transfer of the 6-bit control word from the input register to RAM via the channel-data multiplexer at the beginning of the next conversion cycle. The $W/\overline{R}$ pulse has two restrictions: first, it must be equal to or greater than 4 μs in duration; second, it must be less than $128/f_{OSC}$. This latter restriction is necessary to eliminate the possibility of multiple loads occurring from a single $W/\overline{R}$ pulse that could lead to incorrect control-word transfers under certain conditions.

Fig. 1 Output Cycle Example

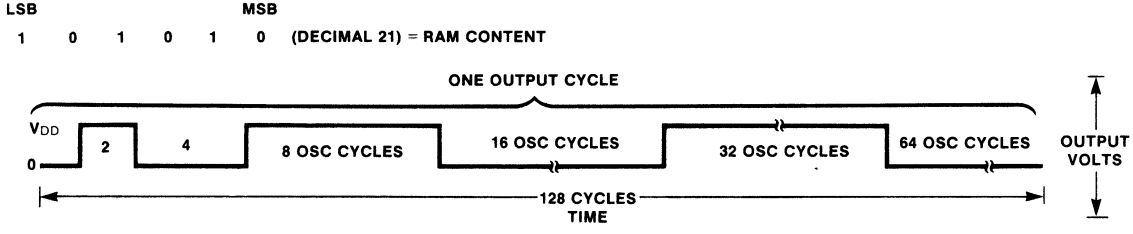
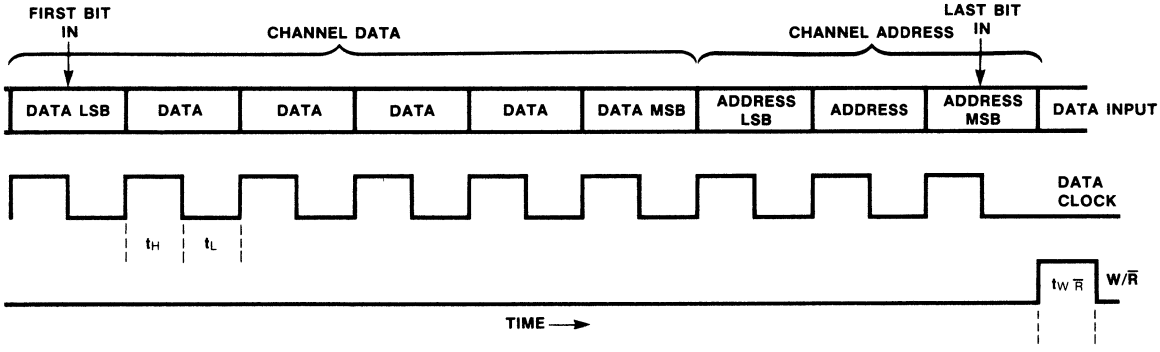


Fig. 2 μA9706 Input Timing and Format



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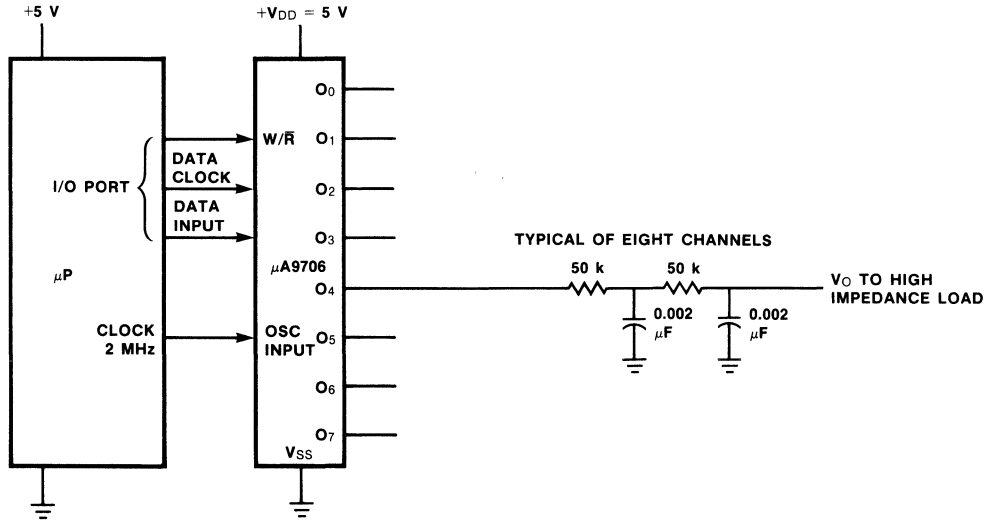
μA9706
Electrical Characteristics V_{DD} = +5 V, V_{SS} = 0 V, T_A = 0°C to +70°C, f_{osc} = 100 kHz

Symbol	Characteristic	Min	Typ	Max	Unit
R_O	Output Resistance (Channels 4 & 5)		30	50	Ω
R_O	Output Resistance (Channels 0, 1, 2, 3, 6, 7)		300	1000	Ω
f_{osc}	Oscillator Frequency	50		2000	kHz
t_H	Data Clock HIGH Time	4			μs
t_L	Data Clock LOW Time	4			μs
$t_{W/R}$	W/$\overline{R}$ Pulse Width	4		$128/f_{osc}$	μs
Error	Linearity			0.01	%
V_{IH}	Voltage Input HIGH			2.7	V
V_{IL}	Voltage Input LOW	0.8			V
I_{DD}	Power Supply Current		40	200	μA
I_{IN}	Input Current			50	μA
C_{IN}	Input Capacitance		8		pF
t_r	Input Rise Time			1.0	μs
t_f	Input Fall Time			1.0	μs
t_s	Input Set-up Time			1.0	μs

Typical Applications



Typical Applications (Cont.)

F8 Object Code Subroutine

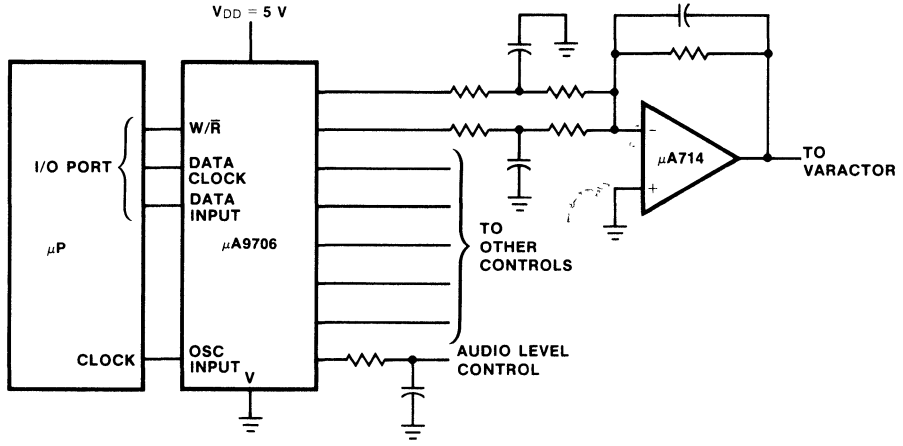
Enter with R_0 = data to be output to 9706
R_1 = address to be output to 9706
entry = H'100'

F8 Object Code

```
M100 – 130
M0100 = 20   20  52  20  04  53  20  07
M0108 = B0   20  0F  B0  40  22  FE  18   Port 0 bit 0 = Data Input
M0110 = 24   0C  B0  24  02  B0  40  12   Port 0 bit 1 = Data Clock
M0118 = 50   42  12  52  94  EF  41  50   Port 0 bit 2 = W/R̄
M0120 = 43   52  70  51  53  40  18  18   Port 0 bit 3 = Scope Trigger
M0128 = 94   E3  20  0B  B0  20  0F  B0
M0130 = 1C
```

Exit = return, destroyed R_0, R_1, R_2, R_3, Acc

Varactor Tuned 12-Bit Receiver System



FAIRCHILD

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μA9708 6-Channel 8-Bit μP Compatible A/D Converter

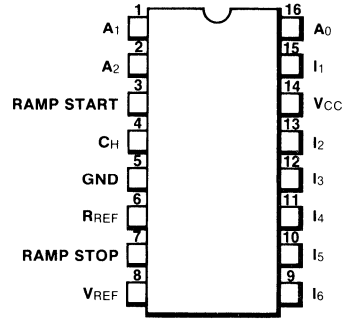
Data Aquisition Products

Description

The μA9708 is a single slope 8-bit, 6-channel ADC subsystem that provides all of the necessary analog functions for a microprocessor-based data control system. The device uses a microprocessor system like the F3870 or F6800 to provide the necessary addressing, timing and counting functions and includes a 1-of-8 decoder, 8-channel analog multiplexer, sample and hold, ramp integrator, precision ramp reference, and a comparator on a single monolithic chip.

- **MPU COMPATIBLE**
- **EXCELLENT LINEARITY OVER FULL TEMPERATURE RANGE ±0.2% MAXIMUM**
- **TYPICAL 300 μs CONVERSION TIME PER CHANNEL**
- **WIDE DYNAMIC RANGE INCLUDES GROUND**
- **AUTO-ZERO AND FULL-SCALE CORRECTION CAPABILITY**
- **RATIOMETRIC CONVERSION—NO PRECISION REFERENCE REQUIRED**
- **SINGLE-SUPPLY OPERATION**
- **TTL COMPATIBLE**
- **DOES NOT REQUIRE ACCESS TO DATA BUS OR ADDRESS BUS**

Connection Diagram
16-Pin DIP

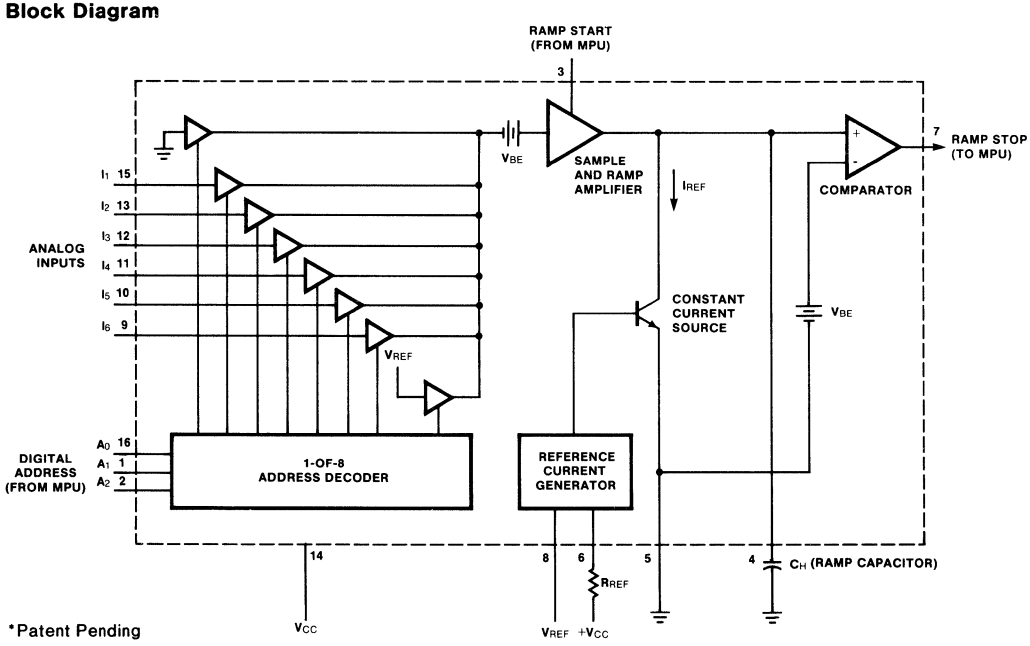


(Top View)

Order Information

Type	Package	Code	Part No.
μA9708	Ceramic DIP	7B	μA9708DM
μA9708	Ceramic DIP	7B	μA9708DC
μA9708	Molded DIP	9B	μA9708PC

Block Diagram



*Patent Pending

Absolute Maximum Ratings

Supply Voltage (V_{CC})	18 V
Comparator Output (Ramp Stop)	−0.3 V to +18 V
Analog Input Range	−0.3 V to 30 V
Digital Input Range	−0.3 V to 30 V
Output Sink Current	10 mA
Operating Temperature Range	
μA9708PC, μA9708DC	0°C to 70°C
μA9708DM	−55°C to 125°C
Storage Temperature Range	−65°C to +150°C
Continuous Total Dissipation	
Ceramic DIP Package	900 mW
Molded DIP Package	1000 mW
Pin Temperature,	
Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Recommended Operating Conditions

Characteristic	Min	Typ	Max	Unit
Supply Voltage (V_{CC})	4.75	5.0	15	V
Reference Voltage (V_{REF})*	2.8		5.25	V
Ramp Capacitor (C_H)	300			pF
Reference Current (I_R)	12		50	μA
Analog Input Range	0		V_{REF}	V
Ramp Stop				
Output Current			1.6	mA

Note

*$2\ V \leq V_{REF} \leq (V_{CC} - 2\ V)$

Channel Selection

Input Address Line			Selected Analog Input
A_2	A_1	A_0	
0	0	0	Ground
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	V_{REF}

Functional Description

This Analog to Digital Converter is a single-slope 8-bit, 6-channel a/d converter that provides all of the necessary analog functions for a microprocessor-based data/control system. The device uses the processor system to provide the necessary addressing, timing and counting functions and includes a 1-of-8 decoder, 8-channel analog multiplexer, sample and hold, precision current reference, ramp integrator and comparator on a single monolithic chip.

For applications that require auto-zero or auto-calibration, (See *Figures 2-5*) line select address 0, 0, 0 and 1, 1, 1 may be used in conjunction with the arithmetic capability of the microprocessor to provide ground and scaling factors. Address 0, 0, 0 internally connects the input of the ramp generator to ground and may be used for zero offset correction in subsequent conversions. Address 1, 1, 1 internally connects the input of the ramp generator to the voltage reference, V_{REF}, and may be used for scale factor correction in subsequent conversions. For the following, refer to the Functional Block Diagram.

Six separate external analog voltage inputs may come into terminals I_1-I_6 and the specific analog input to be converted is selected via address terminals A_0-A_2. The analog input voltage level is transferred to the external ramp capacitor connected to pin 4 when the input to the ramp start terminal (pin 3) is at a logic 0 (See *Figure 1*). The time to charge the capacitor is the acquisition time which is a function of the output impedance of an amplifier internal to the a/d converter and the value of the capacitor. After charging the external capacitor the ramp start terminal is switched to a logic 1 which introduces a high impedance between the analog input voltage and the external capacitor.

The capacitor begins to discharge at a controlled rate. The controlled rate of discharge (ramp) is established by the external reference voltage, the external reference resistor, the value of the external capacitor and the internal leakage of the a/d converter. Connected to the capacitor terminal is a comparator internal to the a/d converter with its output going to the ramp stop terminal (pin 7). The comparator output is a logic one when the capacitor is charged and switches to a logic 0 when the capacitor is in a discharged state. The ramp time is from the time when ramp start goes HIGH (logic "1") to when ramp stop goes LOW (logic "0"). The microprocessor must be programmed to determine this conversion time. The ideal (no undesirable internal source impedances, leakage paths, errors on levels where comparator switches or delay time) conversion time is calculated as follows:

$$\text{Ramp Time} = V_1 \frac{C_H}{I_R}$$

Where V_1 = Analog Input Voltage being measured

C_H = External Ramp Capacitor

$$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$$

Where V_{CC} = Power Supply Voltage

V_{REF} = Reference Voltage

R_{REF} = Reference Resistor

In actual use the errors due to a nonideal a/d converter can be minimized by using a microprocessor to make the calculations. (See *Figures 1* through *4*)

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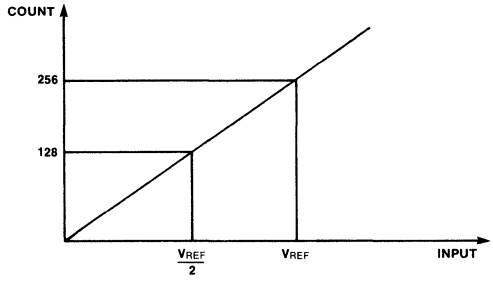
Auto-Zero and Full-Scale Features

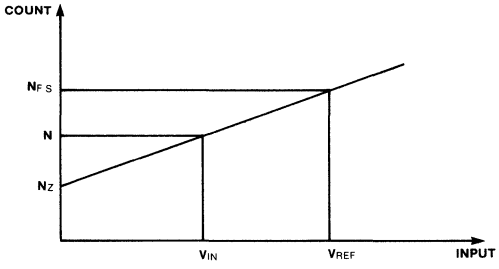
Fig. 1 Ideal Transfer Function



No Zero Offset
No Full-Scale Error

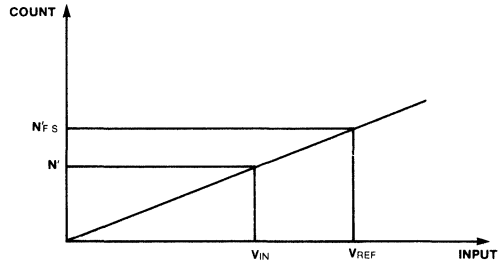
$$\text{Count (n)} = \frac{V_{IN}}{V_{REF}} \times 256$$

Fig. 2 Transfer Function with Zero and Full-Scale Error



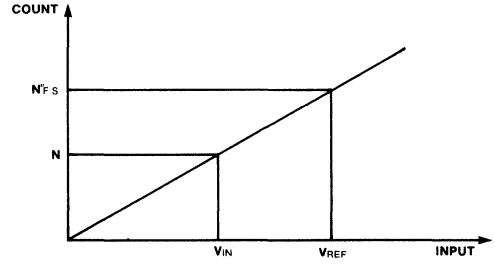
$n_{F.S.} \neq 256$
$n_Z \neq 0$
(n) Has Both Full-Scale and Zero Errors

Fig. 3 Transfer Functions with Zero-Correction Added



$n' = n - n_Z$
n′ Has Full-Scale Error

Fig. 4 Transfer Function with both Zero and Full-Scale Correction Added



$$n'' = (n - n_Z) \times \frac{256}{(n_{F.S.} - n_Z)}$$

Electrical Characteristic Over recommended operating conditions, $-55°C \leq T_A \leq +125°C$, for μA9708DM and $0°C \leq T_A \leq +70°C$ for μA9708DC or μA9708PC; unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
E_A	Conversion Accuracy	Over entire temperature range (Note 1)		±0.2	±0.3	%
E_R	Linearity	Applies to any one channel (Note 2)		±0.08	±0.2	%
V_{OSM}	Multiplexer Input Offset Voltage	Channel ON		2.0	4.0	mV
t_C	Conversion Time Per Channel	Analog Input = 0 V to V_{REF} C_H = 300 pF, I_{REF} = 50 μA		296	350	μs
t_A	Acquisition Time	C_H = 1000 pF		20	40	μs
I_A	Acquisition Current		150			μA
t_O	Ramp Start Delay Time			100		ns
t_M	Multiplexer Address Time			1.0		μs
V_{IH}	Digital Input HIGH Voltage	A_0, A_1, A_2, ramp start	2.0			V
V_{IL}	Digital Input LOW Voltage	A_0, A_1, A_2, ramp start			0.8	V
I_B	Analog Input Current	Channel ON or OFF	−3.0	−1.0		μA
I_{IL}	Input LOW Current	A_0, A_1, A_2, ramp start = 0.4 V	−15	−5		μA
I_{IH}	Input HIGH Current	A_0, A_1, A_2, ramp start = 5.5 V			1.0	μA
I_{OS}	Input Offset Current			1.0	3.0	μA
I_{OH}	Comparator Logic "1" Output Leakage Current	V_{OH} = 15 V			10	μA
V_{OL}	Comparator Logic "0" Output Voltage	I_{OL} = 1.6 mA			0.4	V
PSRR	Power Supply Rejection Ratio	(Note 3)	40			dB
	Cross Talk Between Any Two Channels	(Note 4)	60			dB
I_{CC}	Power Supply Current	V_{CC} = 5 V to 15 V, I_O = 0		7.5	15	mA
C_{IN}	Input Capacitance			3.0		pF
C_{OUT}	Comparator Output Capacitance			5.0		pF

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Notes

1. Conversion accuracy is defined as the deviations from a straight line drawn between the points defined by channel address 000 (0 scale) and channel address 111 (full scale) for all channels.
2. Linearity is defined as the deviation from a straight line drawn between the 0 and full scale points for each channel.
3. Power supply rejection ratio is defined as the conversion error contributed by power supply voltage variations while resolving mid scale on any channel.
4. Cross Talk between channels = $20 \log \frac{\Delta V_{CH}}{\Delta V_I}$

Test Circuits

Fig. 1 Equivalent Timing Waveform for Test Circuits and Applications

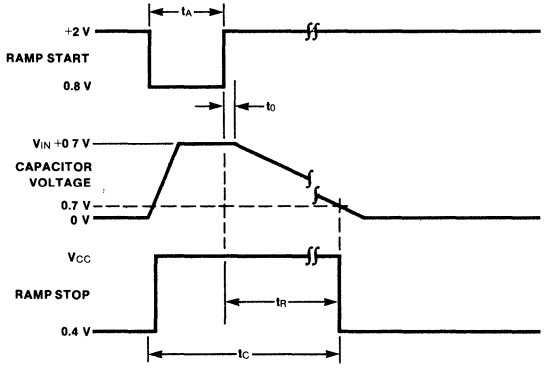
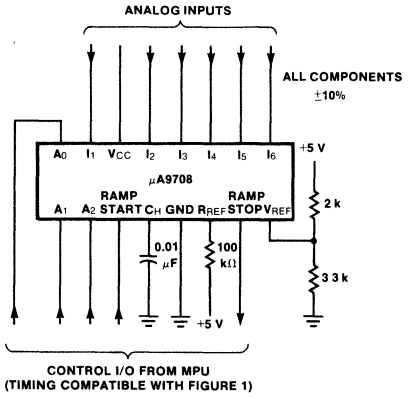


Fig. 2 Slow Speed Evaluation Circuit for Ratiometric Operation



Input Timing:

$t_A > 400\ \mu s$

$$V_{REF} = \left(\frac{3.3\ k\Omega}{2\ k\Omega + 3.3\ k\Omega}\right) 5\ V = 3.1$$

$$I_R = \frac{5\text{-}3.1}{100\ k\Omega} = 19\ \mu A$$

$$t_R|_{max} = \text{full scale ramp time}$$

$$= \frac{0.01 \times 10^{-6}}{19 \times 10^{-6}} \times 3.1 = 1.6\ ms$$

Note

For evaluation purposes, the ramp start timing generation can be implemented with a μA555 timer (astable operation) or MPU evaluation kit, and a time interval meter for ramp time measurement. The TIM meter will measure the time between the 0 to 1 transition of the ramp start and the 1 to 0 transition of the ramp stop. The ramp stop is open collector, and must have an external pull-up resistor to V_{CC}.

Fig. 3 Linearity/Acquisition Time/Conversion Time Test Circuit

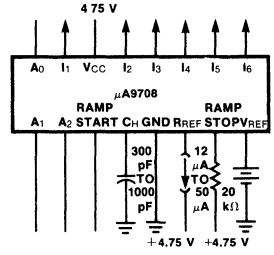
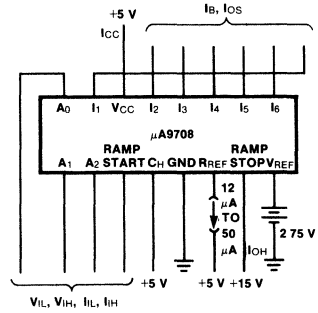


Fig. 4 Static Measurements



Typical Applications

Application Suggestions and Formulas

1. The capacitor node impedance is approximately 30 μΩ and should have no parallel resistance for proper operation.
2. t_R when $V_{IN} = 0$ V will be finite (i.e., the comparator will always toggle for $V_{IN} \geq 0$ V).
3. The ramp stop output is open collector, and an external pull-up resistor is required.
4. All digital inputs and outputs are TTL compatible.
5. For proper operation, timing commences on the 0 to 1 transition of ramp start and terminates on the 1 to 0 transition of ramp stop.
6. $t_A \geq \dfrac{C_H}{150\ \mu A - I_R} \times V_{REF}$
7. t_R (ramp time) $= \dfrac{C_H}{I_R} \times V_{IN}$, $t_R|_{max} = \dfrac{C_H}{I_R} \times V_{REF}$
8. $I_R = \dfrac{V_{CC} - V_{REF}}{R_{REF}}$
9. $2\ V \leq V_{REF} \leq (V_{CC} - 2\ V)$
10. Address lines A_0, A_1, A_2 must be stable throughout the sampling interval, t_A.
11. Pin 6 (R_{REF}) should be bypassed to ground via a 0.02 μF capacitor

Typical Applications (Cont.)

Microprocessor Considerations

Several alternatives exist from a hardware/software standpoint in microprocessor based systems using the μA9708.

1. The ramp time measurement may be implemented in software using a register increment, followed by a branch back depending on the status of the ramp stop.

2. Alternately, the ramp stop may be tied into the interrupt structure in systems containing a programmable binary timer. This scheme has the following advantages:

   a. The CPU is not committed during the ramp time interval.
   b. It requires only 4 bits of an I/O port for control signals.

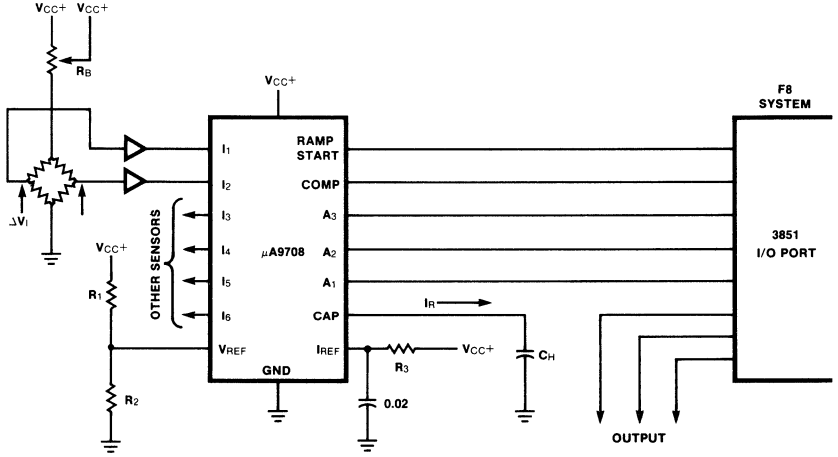
3. The auto-zero/auto-full-scale (see *Figures 2-5*) should use double precision, rounded (as opposed to truncated) arithmatics. Several points are worth noting:

   a. The subtractions are single op code instructions.
   b. The full scale correction uses a multiply by 256 and can be accomplished by a shift left 8 bits (usually one instruction) or placing ($n - n_Z$) in the MSB register and setting the LSB register to zero, for the double precision divide.
   c. The divisor ($n_{F.S.} - n_Z$) of the MSB register will always be zero.

These schemes have the following advantages:

   a. No access to the data bus or address bus is required, by the a/d system.
   b. 4 I/O bits completely support the a/d system.
   c. Since auto full scale/auto zero are implemented in software and long term drift (aging) effects are eliminated.
   d. Software overhead is minimal (typically 30 bytes).
   e. Where ratiometric operation is permissible, the 4 external components may be ±5% tolerance, including the power supply.

Fig. 1 Ratiometric Strain Gage Sensor/Controller

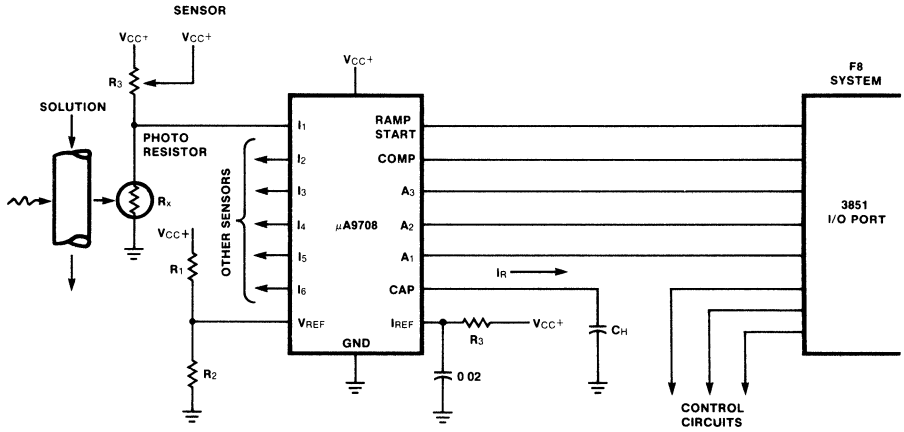


Note

ΔV_I = (Applied Force) and can be Linearized (if necessary) in F8 Software.

Typical Applications (Cont.)

Fig. 2 Opaque Solution Controller



Applications

Beverage Brewers/Dispensers
Chemical Solution Control
Automatic Liquid Mixing Control

$$\text{Ramp Current} = I_R = V_{CC}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{1}{R_3}\right)$$

$$V_I = \left(\frac{R_X}{R_X + R_B}\right) V_{CC+}$$

$$\text{Ramp Time} = V_I\left(\frac{C_H}{I_R}\right) = \left(\frac{R_X}{R_X + R_B}\right)\left(1 + \frac{R_2}{R_1}\right)\left(C_H R_3\right)$$

FAIRCHILD

A Schlumberger Company

μA198/298/398 Monolithic Sample and Hold Amplifiers

Data Acquisition Products

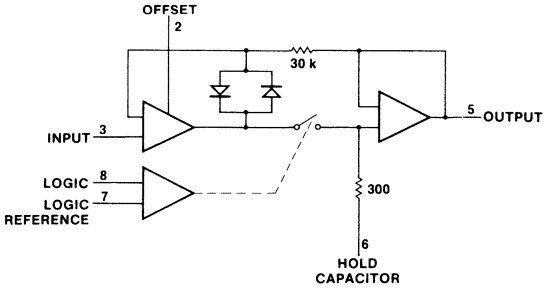
General Description

The μA198/298/398 are Monolithic Sample and Hold Amplifiers which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is typically 4 μs to 0.1%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the μA198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\ \Omega$ allows high source impedances to be used without degrading accuracy.

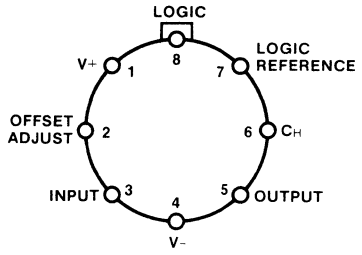
P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 μF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees excellent feedthrough rejection from input to output in the hold mode even for input signals equal to the supply voltages.

- **OPERATES FROM ±5 V TO ±18 V SUPPLIES**
- **ACQUISITION TIME TO .1% TYPICALLY 4 μs**
- **TTL, PMOS, CMOS COMPATIBLE LOGIC INPUT 1.4 V DIFFERENTIAL THRESHOLD**
- **0.5 mV TYPICAL HOLD STEP AT C_H = 0.01 μF**
- **LOW INPUT OFFSET**
- **0.002% GAIN ACCURACY**
- **LOW OUTPUT NOISE IN HOLD MODE**
- **HIGH SUPPLY REJECTION RATIO IN SAMPLE OR HOLD**
- **WIDE BANDWIDTH**

Functional Diagram



Connection Diagram
8-Pin Metal Package

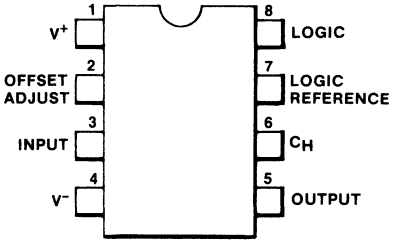


(Top View)

Order Information

Type	Package	Code	Part No.
μA198	Metal	5W	μA198HM
μA298	Metal	5W	μA298HC
μA398	Metal	5W	μA398HC

Connection Diagram
8-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA198	Molded	6T	μA198RM
μA298	Molded	6T	μA298RC
μA398	Molded	6T	μA398RC

7

Absolute Maximum Ratings

Supply Voltage	± 18 V
Power Dissipation (Package Limitation) (Note 1)	500 mW
Operating Ambient Temperature Range	
μA198	−55°C to +125°C
μA298	−25°C to +85°C
μA398	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic-to-Logic Reference Differential Voltage (Note 2)	+7 V, −30 V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 s
Pin Temperature (Soldering, 10 s)	300°C

μA198/μA298/μA398
Electrical Characteristics

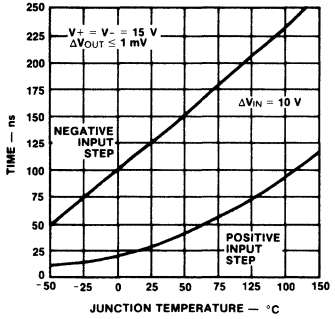
Characteristic	Conditions (Note 3)	μA198/μA298 Min	μA198/μA298 Typ	μA198/μA298 Max	μA398 Min	μA398 Typ	μA398 Max	Unit
Input Offset Voltage (Note 6)	T_J = 25°C Full Temperature Range		1	3 5		2	7 10	mV mV
Input Bias Current (Note 6)	T_J = 25°C Full Temperature Range		5	25 75		10	50 100	nA nA
Input Impedance	T_J = 25°C		10^{10}			10^{10}		Ω
Gain Error	T_J = 25°C, R_L = 10 k Full Temperature Range		0.002	0.005 0.02		0.004	0.01 0.02	% %
Feedthrough Attenuation Ratio at 1 kHz	T_J = 25°C, C_H = 0.01 μF V7 = V8 = 0 V	86	96		80	90		dB
Output Impedance	T_J = 25°C, "HOLD" mode Full Temperature Range		0.5	2 4		0.5	4 6	Ω Ω
"HOLD" Step (Note 4)	T_J = 25°C, C_H = 0.01 μF, V_{OUT} = 0		0.5	2.0		1.0	2.5	mV
Supply Current (Note 6)	$T_J \geq$ 25°C		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	T_J = 25°C		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	T_J = 25°C (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	ΔV_{OUT} = 10 V, C_H = 1000 pF		4			4		μs
	C_H = 0.01 μF		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT}$ = 2 V		5			5		mA
Supply Voltage Rejection Ratio	V_{OUT} = 0	80	110		80	110		dB
Differential Logic Threshold	T_J = 25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

Notes

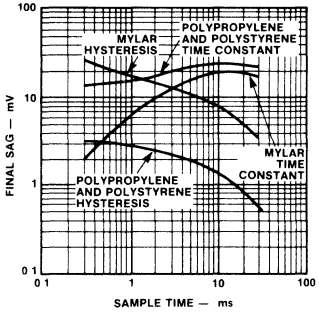
1. The maximum junction temperature of the μA198 is 150°C, for the μA298 is 115°C, and for the μA398 is 100°C. When operating at elevated ambient temperature, the TO-5 package must be derated based on a thermal resistance (Θ_{ja}) of 150° C/W and the R package at (Θ_{ja}) of 130° C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2 V below the positive supply and 3 V above the negative supply.
3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, V_S = ± 15 V, T_J = 25°C, −11.5 V ≤ V_{IN} ≤ +11.5 V, C_H = 0.01 μF, and R_L = 10 kΩ. Logic reference voltage = 0 V and logic voltage = 2.5 V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0 5 mV step with a 5 V logic swing and a 0.01 μF hold capacitor. Magnitude of the hold step is inversely proportional to capacitor value
5. Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
6. These parameters guaranteed over a supply voltage range of ±5 to ± 18 V.

Typical Performance Curves

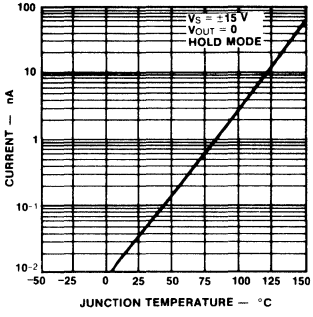
Aperture Time



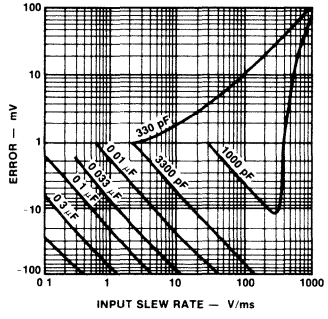
Capacitor Hysteresis



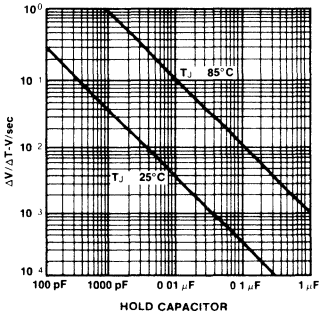
Leakage Current Into Hold Capacitor



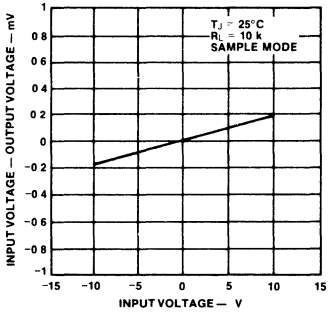
Dynamic Sampling Error



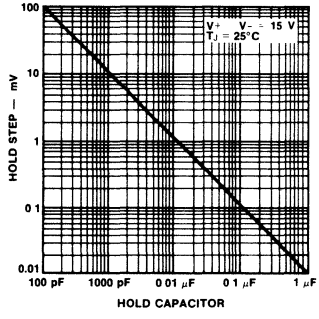
Output Droop Rate



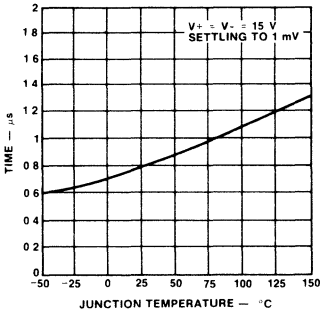
Gain Error



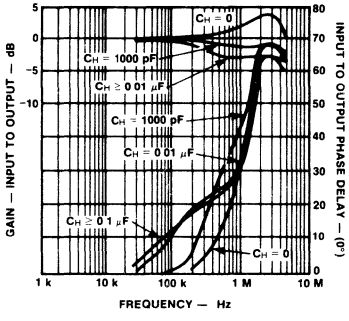
Hold Step



"Hold" Settling Time



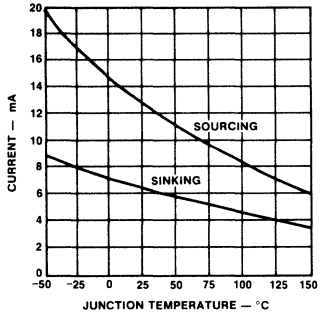
Phase and Gain (Input to Output, Small Signal)



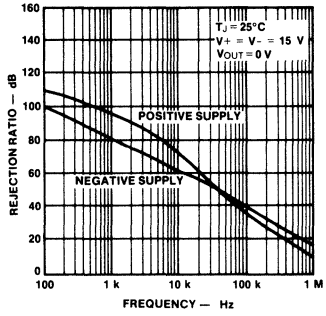
7

Typical Performance Curves (Cont.)

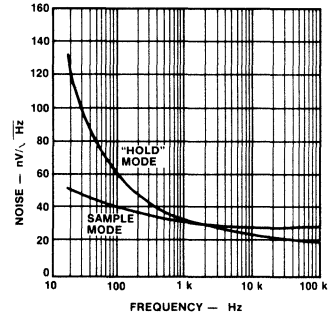
Output Short-Circuit Current



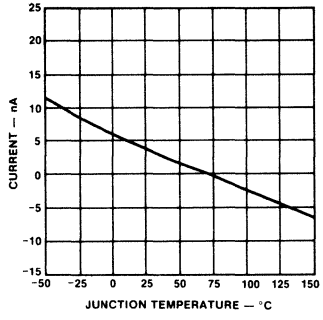
Power Supply Rejection



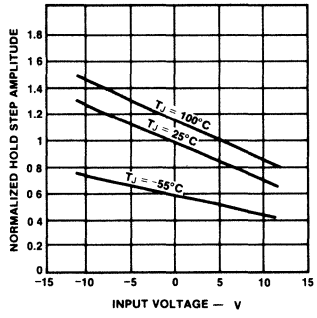
Output Noise



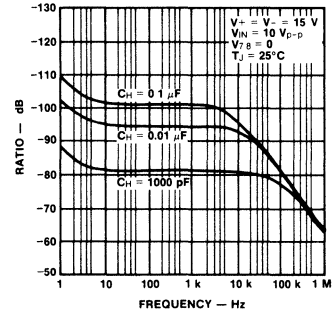
Input Bias Current



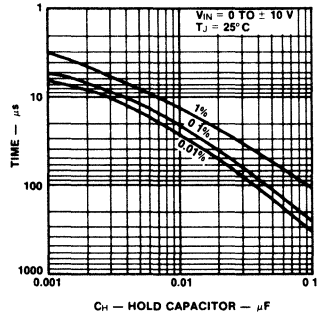
Hold Step vs Input Voltage



Feedthrough Rejection Ratio (Hold Mode)

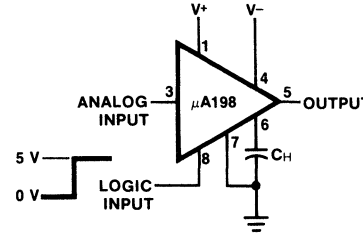


Acquisition Time



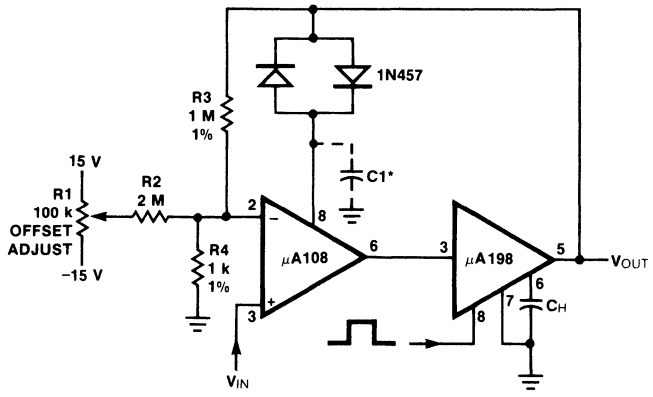
Typical Applications

X1 Sample and Hold



Typical Applications (Cont.)

X1000 Sample and Hold

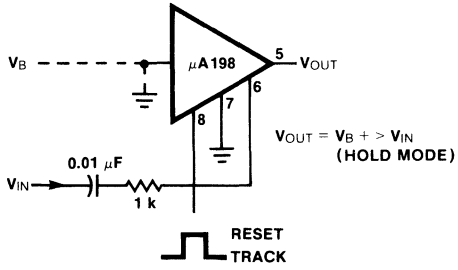


Notes

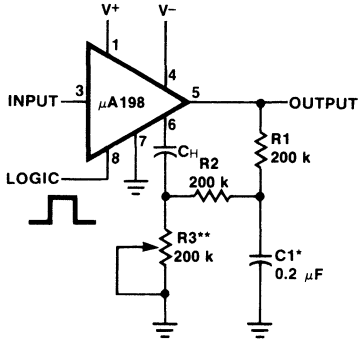
For lower gains, the μA108 must be frequency compensated

Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit (Output Follows Input in Hold Mode)



Capacitor Hysteresis Compensation

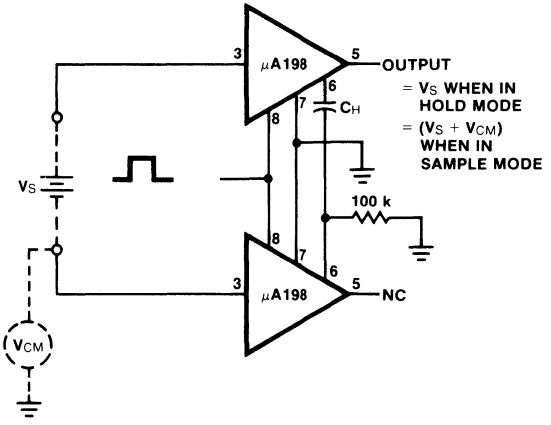


Notes

*Select for time constant C1 = $\frac{\tau}{100\text{ k}}$

**Adjust for amplitude

Differential Hold



7

FAIRCHILD

A Schlumberger Company

μA565 Digital to Analog Converter

Data Acquisition Products

Description

The μA565 is a fast 12-bit digital-to-analog converter combined with a high stability voltage reference on a single monolithic chip. The μA565 chip uses 12 precision, high speed bipolar current steering switches, control amplifier, laser-trimmed thin film resistor network, and buried zener voltage reference to produce a high accuracy analog output current.

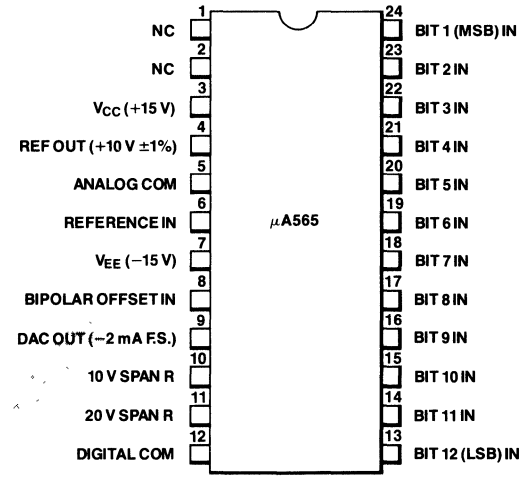
The internal buried zener reference is laser-trimmed to 10.00 V with a ± 1% maximum error. The reference voltage is available externally and can supply up to 1.5 mA beyond that required for the reference and bipolar offset resistors.

The chip also contains additional SiCr thin film resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.

The μA565 is available in four performance grades. The μA565J and K are specified for use over the 0 to 70°C temperature range and the μA565S and T grades are specified for the −55 to +125°C range.

- **SINGLE CHIP CONSTRUCTION**
- **VERY HIGH SPEED, SETTLES TO 1/2 LSB in 200 ns**
- **FULL SCALE SWITCHING TIME—30 ns**
- **HIGH STABILITY BURIED ZENER REFERENCE ON CHIP**
- **MONOTONICITY GUARANTEED OVER TEMPERATURE**
- **LINEARITY GUARANTEED OVER TEMPERATURE—1/2 LSB MAX (μA565K, T)**
- **LOW POWER, 225 mW INCLUDING REFERENCE**

Connection Diagram
24-Pin DIP



(Top View)

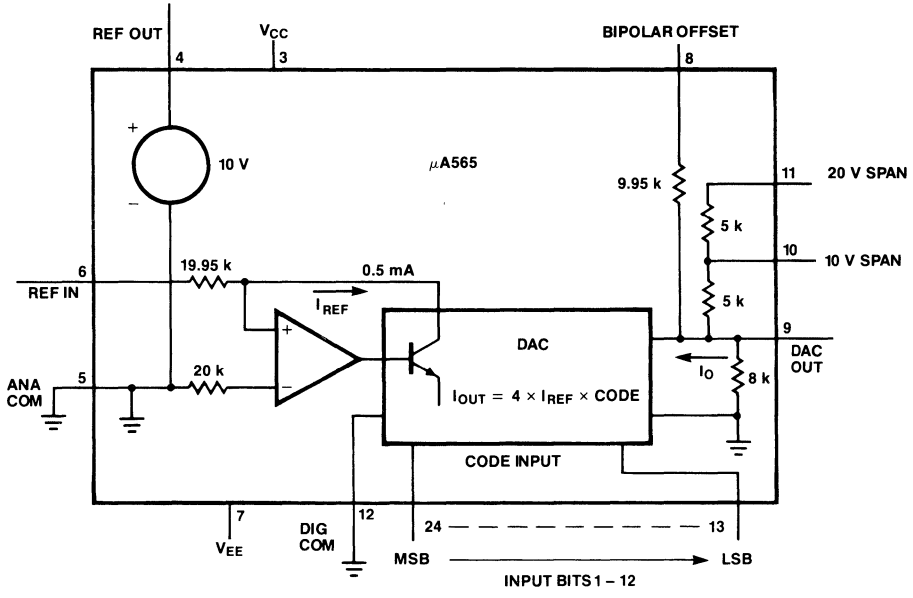
Order Information

Type	Package	Code	Part No.
μA565J	Ceramic (Side Brazed)	7R	μA565JJC
μA565K	Ceramic (Side Brazed)	7R	μA565KJC
μA565S	Ceramic (Side Brazed)	7R	μA565SJM
μA565T	Ceramic (Side Brazed)	7R	μA565TJM

Absolute Maximum Ratings

V_{CC} to Digital Common	0 to +18 V
V_{EE} to Digital Common	0 to −18 V
Analog Common to Digital Common	±1 V
Voltage on DAC Output (Pin 9)	−3 to +12 V
Digital Inputs (Pins 13 to 24) to Digital Com	−1.0 to +7.0 V
Ref In to Analog Common	±12 V
Bipolar Offset to Analog Common	±12 V
10 V Span R to Analog Common	±12 V
20 V Span R to Analog Common	±12 V
Ref Out	Indefinite short to either Common Momentary Short to V_{CC}
Power Dissipation	1000 mW
Operating Temperature: J, K	0°C to +70°C
S, T	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Pin Temperature (Soldering) Ceramic DIP (60 s)	300°C

Block Diagram



Internal Simplified Schematic

μA565
Electrical Characteristics V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C, unless otherwise specified

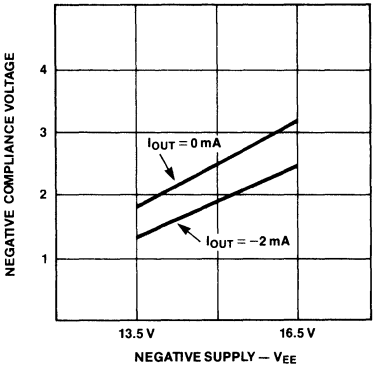
Characteristic		Condition	μA565J, S (Note 1)			μA565K, T (Note 1)			Units
			Min	Typ	Max	Min	Typ	Max	
Data Input Voltage	Bit ON Logic "1"		+2.0		+5.5	+2.0		+5.5	V
	Bit OFF Logic "0"				+0.8			+0.8	V
Data Input Current	Bit ON Logic "1"			+120	+260		+120	+260	μA
	Bit OFF Logic "0"			+35	+75		+35	+75	μA
Resolution					12			12	Bits
Output Current	Unipolar	All bits on	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
	Bipolar	All bits on or off	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Output Resistance (exclusive of span resistors)			6	8	10	6	8	10	kΩ
Output Offset	Unipolar			0.01	0.05		0.01	0.02	% of F.S.
	Bipolar	R_2 = 50 Ω fixed (Note 1)		0.05	0.15		0.05	0.1	% of F.S.
Output Capacitance				25			25		pF
Output Compliance Voltage		I_{min} to I_{max}	−1.5		+10	−1.5		+10	V
Accuracy (error relative to full scale)				± ¼	± ½		± ⅛	± ¼	LSB
				(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
		T_{min} to T_{max}		± ½	± ¾		± ¼	± ½	LSB
				(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
Differential Nonlinearity				± ½	± ¾		± ¼	± ½	LSB
		T_{min} to T_{max}	Monotonicity Guaranteed			Monotonicity Guaranteed			
Temperature Coefficient of Unipolar Zero		T_{min} to T_{max}		1	2		1	2	ppm/°C
Temperature Coefficient of Bipolar Zero		T_{min} to T_{max}		5	10		5	10	ppm/°C
Temperature Coefficient of Gain (Full Scale)		T_{min} to T_{max}		15	30		10	20	ppm/°C
Temperature Coefficient of Differential Nonlinearity		T_{min} to T_{max}		2			2		ppm/°C
Settling Time to ½ LSB		All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns

Note

1. t_{min} and t_{max} are −55°C and 125°C for μA565S and μA565T.
   t_{min} and t_{max} are 0°C and 70°C for μA565J and μA565K.

Typical Performance Curve

Typical Negative Compliance Range vs. Negative Supply



Typical Applications

Buffered Voltage

The standard current-to-voltage conversion connections using an operational amplifier are shown in Fig. 1 with the preferred trimming techniques. If a low offset operational amplifier (μA714L, μA725A) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV max offset voltage should be used to keep offset errors below ½ LSB). If a 50 Ω fixed resistor is substituted for the 100 Ω trimmer, unipolar zero will typically be within ± ½ LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50 Ω resistor for the 100 Ω bipolar offset trimmer will give a bipolar zero error typically within ±2 LSB (0.05%).

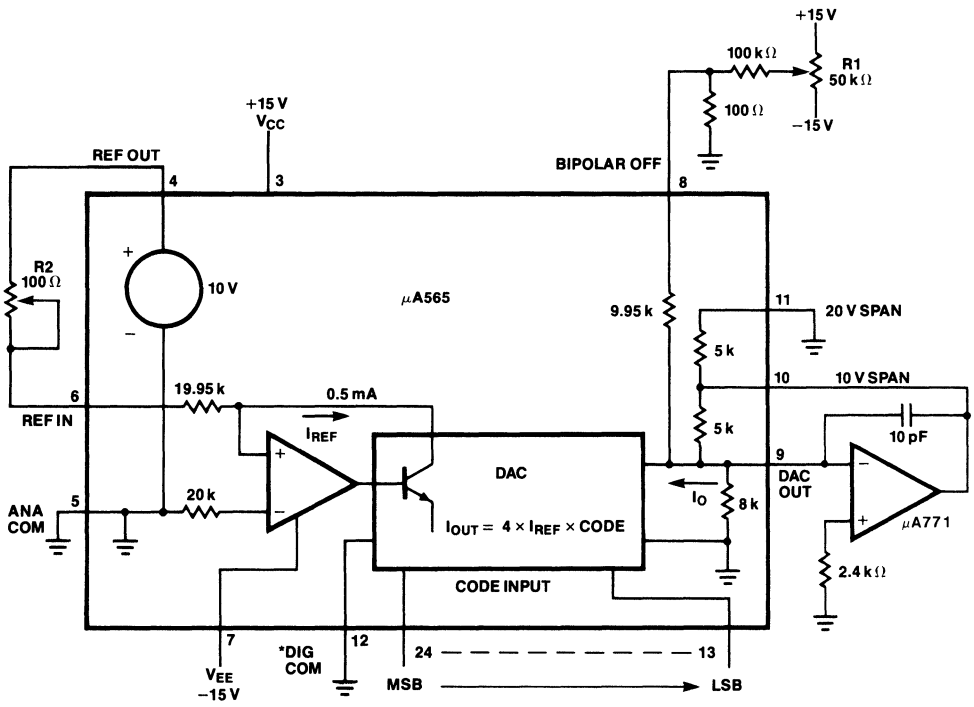
The μA771 is recommended for buffered voltage output applications which require a settling time to ± ½ LSB of two microseconds. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 pF DAC output capacitance.

This unipolar configuration (*Figure 1*) will provide a unipolar 0 to +10 V output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

Step I, Zero Adjust

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1 LSB = 2.44 mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 5.

Fig. 1 0 to +10 V Unipolar Voltage Output



*Digital and analog common must have a common current return path.

See typical applications continued for proper connections.

Typical Applications (Cont.)

Step II, Gain Adjust
Turn all bits ON and adjust 100 Ω gain trimmer, R2, until the output is 9.9976 V. (Full scale is adjusted to 1 LSB less than nominal full scale of 10.000 V.) If a 10.2375 V full scale is desired (exactly 2.5 mV/bit), insert a 120 Ω resistor in series with the gain resistor at pin 10 to the op amp output.

Figure 2, bipolar configuration, will provide a bipolar output voltage from −5.000 to +4.9976 V, with positive full scale occurring with all bits ON (all "1"s).

Step I, Offset Adjust
Turn OFF all bits. Adjust 100 Ω trimmer R1, to give −5.000 V output.

Step II, Gain Adjust
Turn ON all bits, adjust 100 Ω gain trimmer to give a reading of +4.9976 V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

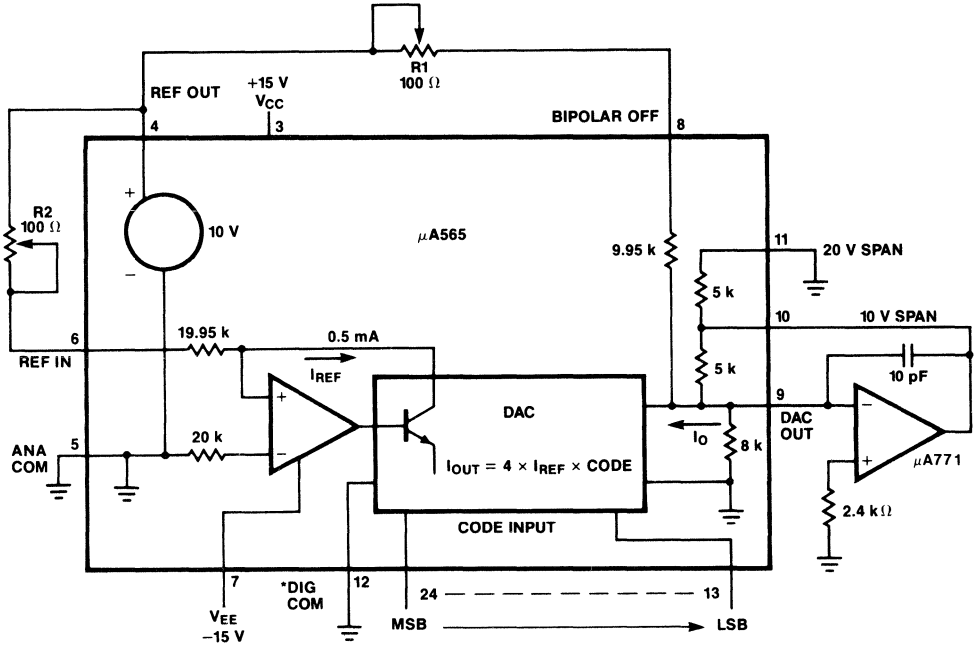
The μA565 can also be easily configured for a unipolar 0 to +5 V range or ±2.5 V and ±10 V bipolar ranges by using the additional 5 k application resistor provided at the 20 V span R terminal, pin 11. For a 5 V span (0 to +5 or ±2.5), the two 5 k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 V range (20 V span) use the 5 k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 V option is shown in *Figure 3*.

Internal/External Reference Use
The μA565 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the μA565 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale and bipolar) are done in this configuration.

The μA565 can be used with an external reference, but may not have sufficient trim range to accommodate a reference which does not match the internal reference.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5 mA to REF IN and 1.0 mA to BIPOLAR OFFSET IN, if used). A minimum of

Fig. 2 ±5 V Bipolar Voltage Output



*Digital and analog common must have a common current return path

See typical applications continued for proper connections

Typical Applications (Cont.)

1.5 mA is available for driving external circuits. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ± 1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

Digital Input Considerations
The μA565 uses a standard positive true straight binary code for unipolar outputs (all "1"s give full scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all "0"s on the inputs, the output will go to negative full scale; with 100...00 (only the MSB on), the output will be 0.00 V; with all "1"s, the output will go to positive full scale.

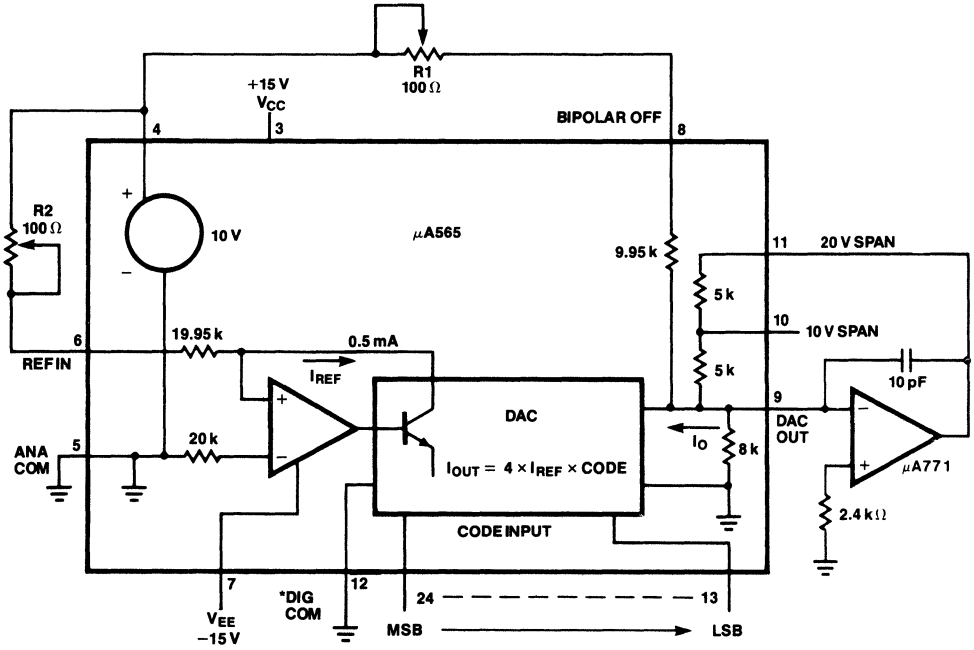
The threshold of the digital input circuitry is set at 1.4 V and does not vary with supply voltage. The input lines can interface with any type of 5 V logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in *Figure 4*. The input line can be modelled as a 30 kΩ resistance connected to −0.7 V rail.

Application of Analog and Digital Commons
The μA565 brings out separate analog and digital grounds to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 mV without any loss in performance. There may be some loss in linearity beyond that level. Up to ± 1 V can be tolerated between the ground lines without damage to the device. If the μA565 is to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog common at pin 5 is the ground reference point for the internal reference and is thus the "high quality" ground for the μA565: it should be connected directly to the analog reference point of the system. The digital common at pin 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If digital common contains high frequency noise beyond 200 mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

Output Voltage Compliance
The μA565 has a typical output compliance range from −2 to +10 V. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8 k in parallel with 25 pF at the output terminal which produces an

Fig. 3 ± 10 V Bipolar Voltage Output

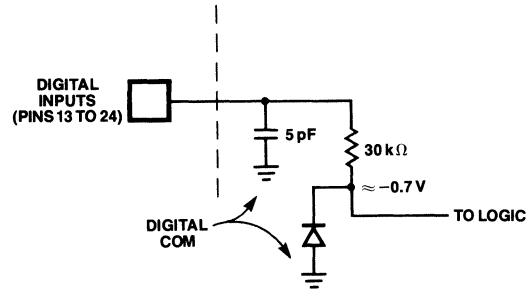


*Digital and analog common must have a common current return path.
See typical applications continued for proper connections.

Typical Applications (Cont.)

equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in the Typical Performance Curve.

Fig. 4 Equivalent Digital Input Circuit



FAIRCHILD

A Schlumberger Company

μA571
Analog to Digital Converter

Data Acquisition Products

Description

The μA571 is a 10-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers—all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 25 μs.

The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.

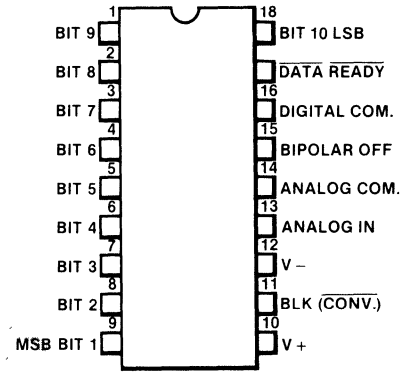
Operation is guaranteed with −15 V and +5 V to +15 V supplies. The device will also operate with a −12 V supply.

Operating on supplies of +5 V to ± 15 V, the μA571 will accept analog inputs of 0 to +10 V, unipolar or ± 5 V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven LOW, the 3-state outputs will be open and a conversion starts. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go LOW and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input HIGH blanks the outputs and readies the device for the next conversion. The μA571 executes a true 10-bit conversion with no missing codes in approximately 25 μs.

The μA571 is available in two versions for the 0 to +70°C temperature range, the μA571J and K. The μA571S guarantees 10-bit accuracy and no missing codes from −55°C to +125°C. All three grades are packaged in an 18-pin ceramic DIP.

- **COMPLETE A/D CONVERTER WITH REFERENCE AND CLOCK**
- **FAST SUCCESSIVE APPROXIMATION CONVERSION—25 μs**
- **NO MISSING CODES OVER TEMPERATURE**
- **DIGITAL MULTIPLEXING—3-STATE OUTPUTS**
- **18-PIN CERAMIC DIP**
- **LOW COST MONOLITHIC CONSTRUCTION**

Connection Diagram
18-Pin DIP



(Top View)

Order Information

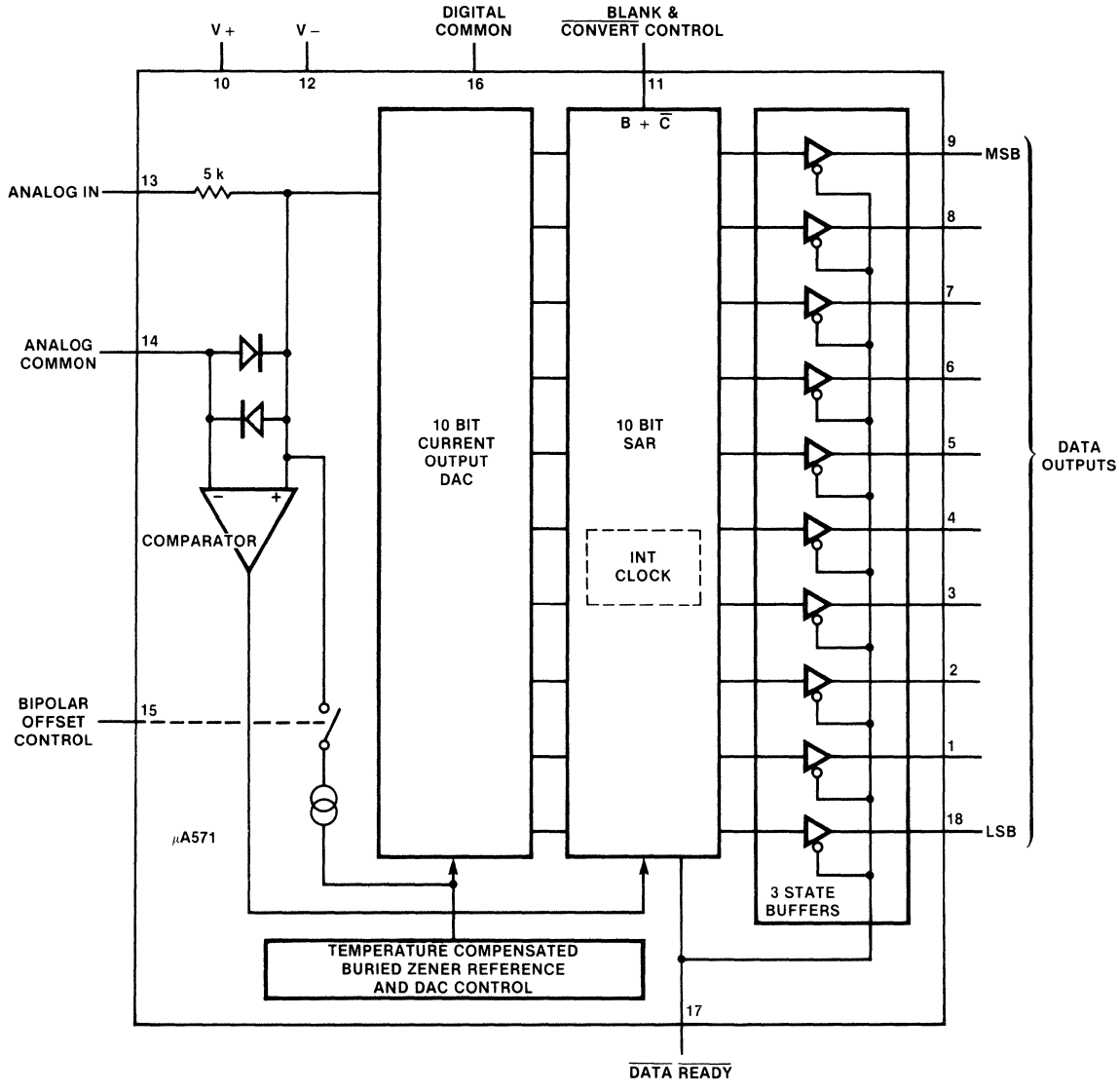
Type	Package	Code	Part No.
μA571J	Ceramic DIP	FD	μA571JJC
μA571K	Ceramic DIP	FD	μA571KJC
μA571S	Ceramic DIP	FD	μA571SJD

7

Absolute Maximum Ratings

V+ to Digital Common	0 to + 7 V	Power Dissipation	800 mW
V− to Digital Common	0 to −16.5 V	Operating Temperature	0°C to +70°C
Analog Common to Digital Common	± 1 V	Storage Temperature	−55°C to +125°C
Analog Input to Analog Common	± 15 V	Pin Temperature (Soldering)	
Control Inputs	0 to V+	Ceramic DIP (60 s)	300°C
Digital Outputs (Blank Mode)	0 to V+		

Block Diagram



μA571
Electrical Characteristics V+ = +5 V, V− = −15 V, T_A = +25°C, all voltages measured with respect to digital common, unless otherwise specified

Characteristic		Condition	μA571JJC Min	μA571JJC Typ	μA571JJC Max	μA571KJC Min	μA571KJC Typ	μA571KJC Max	Units
Resolution				10			10		Bits
Relative Accuracy (Note 1)					±1			±½	LSB
		T_{min} to T_{max}			±1			±½	LSB
Full Scale Calibration (Note 2)		With 15 Ω Resistor in Series with Analog Input		±2			±2		LSB
Unipolar Offset					±1		±½		LSB
Bipolar Offset					±1		±½		LSB
Differential Nonlinearity (Note 3)				10			10		Bits
		T_{min} to T_{max}		9			10		Bits
Temperature Coefficient of Unipolar Offset		T_{min} to T_{max}			±2			±1	LSB
					44			22	ppm/°C
Temperature Coefficient of Bipolar Offset		T_{min} to T_{max}			±2			±1	LSB
					44			22	ppm/°C
Temperature Coefficient of Full Scale Calibration		T_{min} to T_{max} with 15 Ω Resistor or 50 Ω Trimmer			±4			±2	LSB
					88			44	ppm/°C
Power Supply Rejection	CMOS Pos. Supply	±13.5 V ≤ V+ ≤ +16.5 V						±1	LSB
	TTL Pos. Supply	+4.5 V ≤ V+ ≤ 5.5 V			±2			±1	LSB
	Negative Supply	−16.5 V ≤ V+ ≤ −13.5 V			±2			±1	LSB
Analog Input Resistance			3	5	7	3	5	7	kΩ
Analog Input Ranges	Unipolar		0		10	0		10	V
	Bipolar		−5		+5	−5		+5	V
Output Coding	Unipolar		Positive True Binary			Positive True Binary			
	Bipolar		Positive True Offset Binary			Positive True Offset Binary			
Output Sink Current		V_{OUT} = 0.4 V max, T_{min} to T_{max}	3.2			3.2			mA
Output Source Current (Bit Outputs) (Note 4)		V_{OUT} = 2.4 V min, T_{min} to T_{max}	0.5			0.5			mA
Output Leakage When Blanked					±40			±40	μA
Blank & Convert Input		0 ≤ V_{IN} ≤ V+			40			40	μA
Blank-Logic "1"			2.0			2.0			V
Convert-Logic "0"					0.8			0.8	V
Conversion Time			15	25	30	15	25	30	μs
Operating Range	V+		+4.5		+5.5	+4.5		+16.5	V
	V−		−12		−16.5	−12		−16.5	V

Notes
1. Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from zero to the full scale of the device.
2. Full scale calibration is guaranteed trimmable to zero with an external 50 Ω potentiometer in place of the 15 Ω fixed resistor. Full scale is defined as 10 V minus 1 LSB, or 9.990 V.
3. Info coming.
4. The data output lines have active pull-ups to source 0.5 mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6 kΩ internal pull-up resistor.

μA571
Electrical Characteristics (Cont.) V+ = +5 V, V− = −15 V, T_A = +25°C, all voltages measured with respect to digital common, unless otherwise specified

Characteristic	Condition	μA571JDC			μA571KDC			Units
		Min	Typ	Max	Min	Typ	Max	
Operating Current-Blank Mode	V+ = +5 V		2	10		2	10	mA
	V+ = +15 V		5	10		5	10	mA
	V− = −15 V		9	15		9	15	mA
Operating Current-Convert Mode	V+ = +5 V		5			5		mA
	V+ = +15 V		10			10		mA
	V− = −15 V		10			10		mA

μA571
Electrical Characteristics V+ = +5 V, V− = −15 V, T_A = +25°C, all voltages measured with respect to digital common, unless otherwise specified

Characteristic		Condition	μA571SDM			Units
			Min	Typ	Max	
Resolution				10		Bits
Relative Accuracy (Note 1)					±1	LSB
		T_{min} to T_{max}			±1	LSB
Full Scale Calibration (Note 2)		With 15 Ω Resistor in Series with Analog Input		±2		LSB
Unipolar Offset					±1	LSB
Bipolar Offset					±1	LSB
Differential Nonlinearity (Note 3)				10		Bits
		T_{min} to T_{max}		10		Bits
Temperature Coefficient of Unipolar Offset		T_{min} to T_{max}			±2	LSB
					20	ppm/°C
Temperature Coefficient of Bipolar Offset		T_{min} to T_{max}			±2	LSB
					20	ppm/°C
Temperature Coefficient of Full Scale Calibration		T_{min} to T_{max}, with 15 Ω Fixed Resistor or 50 Ω Trimmer			±5	LSB
					50	ppm/°C
Power Supply Rejection	TTL Pos. Supply	+4.5 V ≤ V+ ≤ 5.5 V			±2	LSB
	Neg. Supply	−16.5 V ≤ V+ ≤ −13.5 V			±2	LSB
Analog Input Resistance			3	5	7	kΩ
Analog Input Ranges	Unipolar		0		10	V
	Bipolar		−5		±5	V
Output Coding	Unipolar		Positive True Binary			
	Bipolar		Positive True Offset Binary			
Output Sink Current		V_{OUT} = 0.4 V max, T_{min} to T_{max}	3.2			mA
Output Source Current (Bit Outputs) (Note 4)		V_{OUT} = 2.4 V min, T_{min} to T_{max}	0.5			mA

Notes
1. Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from zero to the full scale of the device.
2. Full scale calibration is guaranteed trimmable to zero with an external 50 Ω potentiometer in place of the 15 Ω fixed resistor. Full scale is defined as 10 V minus 1 LSB, or 9.990 V.
3. Info coming.
4. The data output lines have active pull-ups to source 0.5 mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6 kΩ internal pull-up resistor.

μA571
Electrical Characteristics (Cont.) V+ = +5 V, V− = −15 V, T_A = +25°C, all voltages measured with respect to digital common, unless otherwise specified

Characteristic		Condition	μA571SDM Min	Typ	Max	Unit
Output Leakage When Blanked					±40	μA
Blank & Convert Input					±40	μA
Blank-Logic "1"			2.0			V
Convert-Logic "0"					0.8	V
Conversion Time			15	25	30	μs
Operating Range	V+		+4.5		+5.5	V
	V−		−12		−16.5	V
Operating Current-Blank Mode		V+ = +5 V		2	10	mA
		V+ = +15 V		5	10	mA
		V− = −15 V		9	15	mA
Operating Current-Convert Mode		V+ = +5 V		5		mA
		V+ = +15 V		10		mA
		V− = −15 V		10		mA

Typical Applications

Standard μA571 Operation

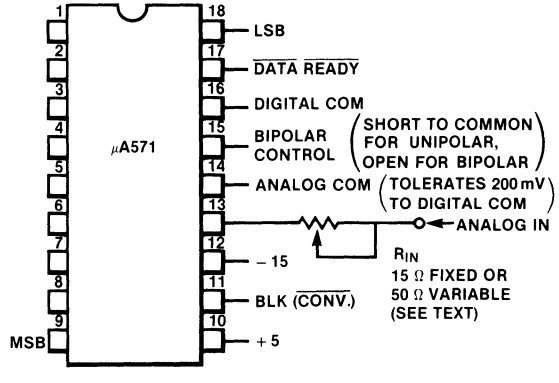
The μA571 contains all the active components required to perform a complete A/D conversion. For most situations, all that is necessary is connection of the power supply (+5 and −15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in the connection diagram.

Full Scale Calibration

The 5 kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.990 V (10 V—1 LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 V full scale can be achieved to sufficient accuracy by simply inserting a 15 Ω resistor in series with the analog input to pin 13. Typical full scale calibration error will then be about ±2 LSB or ±0.2%. If the more precise calibration is desired, a 50 Ω trimmer should be used instead. Set the analog input at 9.990 V, and set ther trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of 9.766 mV. If a nominal full scale of 10.24 V is desired (which makes the LSB exactly 10.00 mV), a 100 Ω resistor in series with a 100 Ω trimmer (or a 200 Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full

7

Fig. 1 Standard μA571 Connections



(Top View)

Typical Applications (Cont.)

scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5 kΩ.

Bipolar Operation
The standard unipolar 0 to +10 V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a −5 V to +5 V range with an offset binary output code. (−5.00 V in will give a 10-bit code of 0000000000; an input of 0.00 V results in an output code of 1000000000 and 4.99 V at the input yields the 1111111111 code). The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in *Figure 2.*

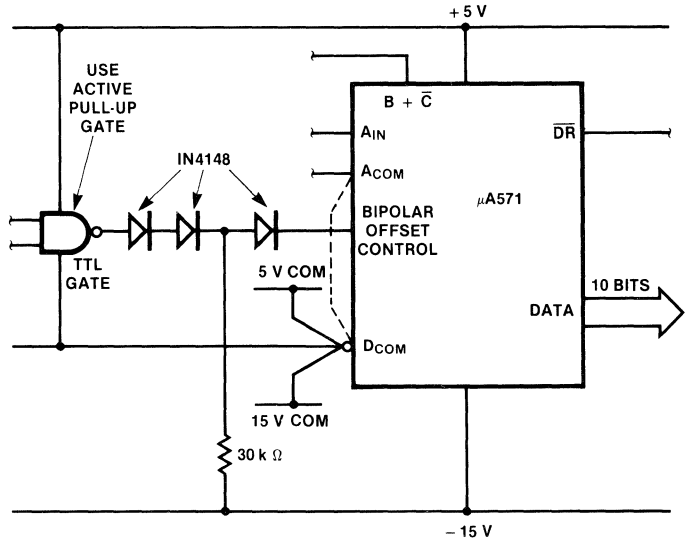
Common Mode Range
The μA571 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200 mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2 mA during a conversion. In addition, a static current of about 2 mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1 mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 V. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

Zero Offset
The apparent zero point of the μA571 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. *Figure 3* illustrates two methods of providing this offset. *Figure 3A* shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

Fig. 2 Bipolar Offset Controlled by Logic Gate



Gate Output = 1 Unipolar 0-10 V Input
Range Gate Ouput = 0 Bipolar ±5 V Input Range

Typical Applications (Cont.)

Fig. 3a Zero Offset ADJ ±3-Bit Range

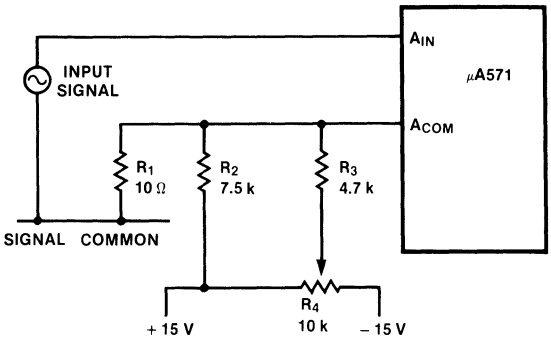
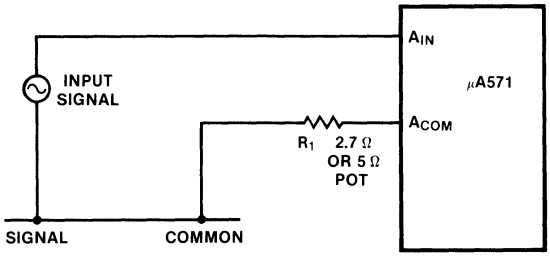


Fig. 3b ½-Bit Zero Offset

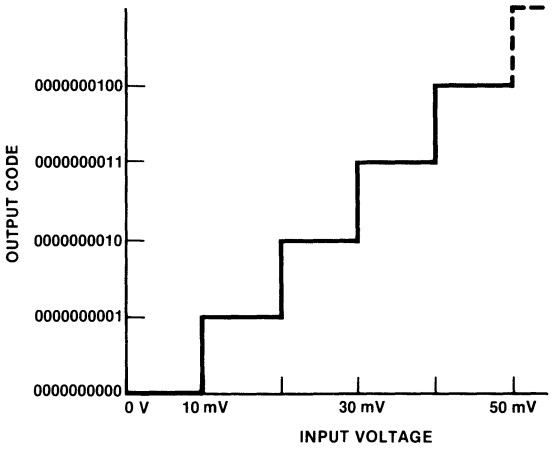


Note

During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common should go to the signal input side of the resistive offset network.

Fig. 4 μA571 Transfer Curve—Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766 mV)

Nominal Characteristics referred to Analog Common



Offset Characteristics with 2.7 in series with Analog Common

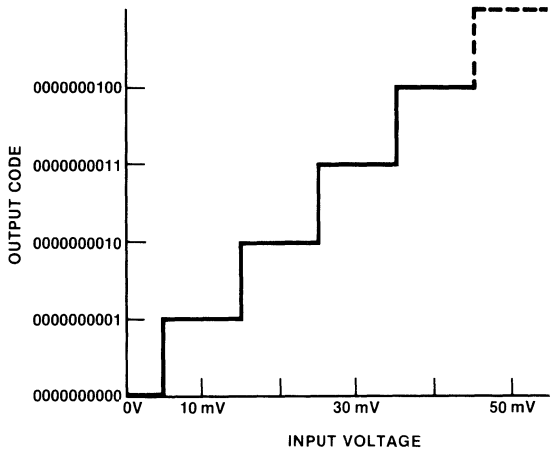


Figure 4 shows the nominal transfer curve near zero for a μA571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in *Figure 3B*. At balance (after a conversion) approximately 2 mA flows into the Analog Common terminal. A 2.7 Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2 mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5 Ω potentiometer (connected as a rheostat) can be used as R2. Additional negative offset range may be obtained by using larger values of R2. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.985 V.

Typical Applications (Cont.)

Control and Timing of the μA571
There are several important timing and control features on the μA571 which must be understood precisely to allow optimum interface to microprocessor or other types of control systems. All of these features are shown in the timing diagram in *Figure 5.*

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held HIGH, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be HIGH. This mode is the lowest power state of the device (typically 150 mW). When the B & $\overline{\text{C}}$ line is brought LOW, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and data lines do not change state. When the conversion cycle is complete (typically 25 μs), the $\overline{\text{DR}}$ line goes LOW, and within 500 ns, the data lines become active with the new data.

About 1.5 μs after the B & $\overline{\text{C}}$ line is again brought HIGH, the $\overline{\text{DR}}$ line will go HIGH and the data lines will go open. When the B & $\overline{\text{C}}$ line is again brought LOW, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2 μs. If the B & $\overline{\text{C}}$ line is brought HIGH during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and data lines will not change. If a 2 μs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

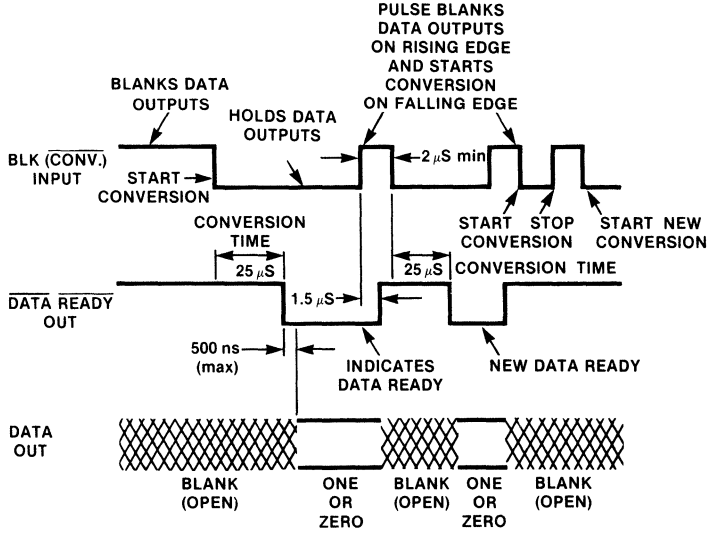
Control Modes with BLANK and $\overline{\text{CONVERT}}$
The timing sequence of the μA571 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode
In this mode, data is present at the output of the converter at all times except when conversion is taking place. *Figure 6* illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally LOW and conversions are triggered by a positive pulse.

Multiplex Mode
In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing shown in *Figure 7.*

This operating mode allows multiple μA571 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held HIGH to keep the outputs blanked. A single μA571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven LOW and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going LOW, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several μA571's are multiplexed in sequence, a new conversion may be started in one μA571 while data is being read from another. As long as the data is read and the first μA571 is cleared within 15 μs after the start of conversion of the second μA571, no data overlap will occur.

Fig. 5 μA571 Timing and Control Sequence



Typical Applications (Cont.)

Fig. 6 Convert Pulse Mode

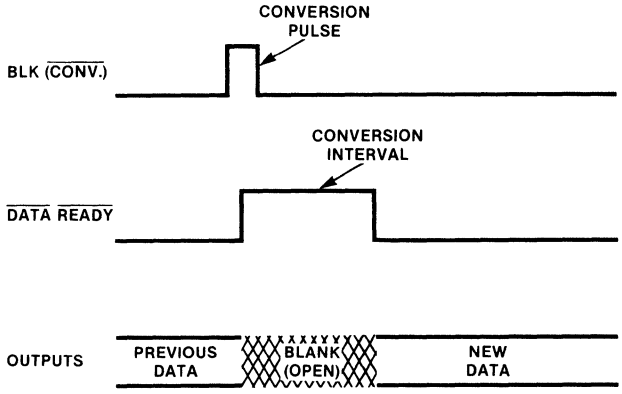
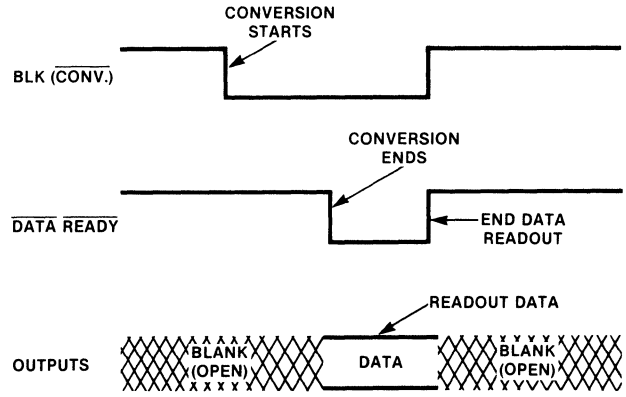


Fig. 7 Multiplex Mode



7

FAIRCHILD

A Schlumberger Company

μA0801 (DAC-08) Series 8-Bit Multiplying D/A Converters

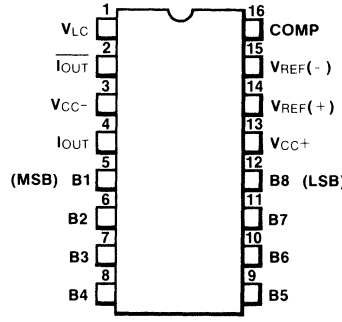
Data Aquisition Products

Description

The μA0801, μA0801E and μA0801C are 8-bit multiplying Digital-to-Analog Converters constructed using the Fairchild Planar epitaxial process. Advanced circuit design achieves very high speed performance with outstanding applications capability and low cost. The μA0801 is specified for the military temperature range (−55°C to +125°C) and the μA0801E and μA0801C are specified for 0°C to +70°C operation. The μA0801 series are pin-for-pin replacements of the DAC-08 and DAC0800 series.

- **FAST SETTLING TIME TO 1/2 LSB 85 ns**
- **FULL SCALE CURRENT PREMATCHED TO ±1 LSB**
- **DIRECT INTERFACE TO TTL, CMOS, ECL, HTL, PMOS, DTL**
- **LINEARITY TO ±0.19% MAX OVER TEMPERATURE RANGE**
- **HIGH OUTPUT COMPLIANCE −10 V TO +18 V**
- **TRUE AND COMPLEMENTED OUTPUTS**
- **WIDE RANGE MULTIPLYING CAPABILITY**
- **LOW FULL SCALE CURRENT DRIFT +10 ppm/°C TYP**
- **WIDE POWER SUPPLY RANGE ±4.5 V TO ±18 V**
- **LOW POWER CONSUMPTION 33 mW @ ±5 V**
- **EXTERNAL COMPENSATION FOR MAX BANDWIDTH**
- **LOW COST**

Connection Diagram
16-Pin DIP

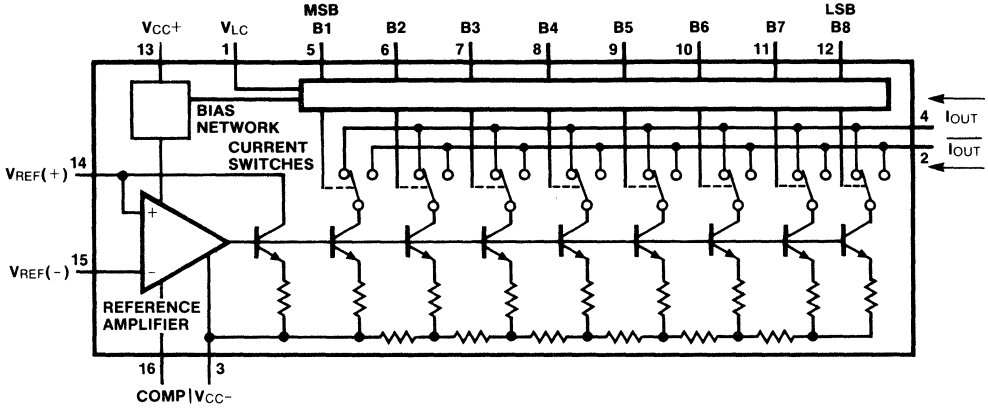


(Top View)

Order Information

Type	Package	Code	Part No.
μA0801	Ceramic DIP	6B	μA0801DM
μA0801E	Ceramic DIP	6B	μA0801EDC
μA0801E	Molded DIP	9B	μA0801EPC
μA0801C	Ceramic DIP	6B	μA0801CDC
μA0801C	Molded DIP	9B	μA0801CPC

Equivalent Circuit and Pin Connection Diagram



Absolute Maximum Ratings

V_{CC+} to V_{CC-}	36 V
Logic Inputs	V_{CC-} to V_{CC-} plus 36 V
V_{LC}	V_{CC-} to V_{CC+}
Reference Inputs (V_{14}, V_{15})	V_{CC-} to V_{CC+}
Reference Input Differential Voltage (V_{14} to V_{15})	± 18 V
Reference Input Current I_{REF} (14)	5.0 mA
Power Dissipation	500 mW
Derate above 90°C (Ceramic DIP)	8.3 mW/°C
Operating Temperature Range	
μA0801	−55°C to +125°C
μA0801E, μA0801C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Ceramic DIP, (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Electrical Characteristics

These specifications apply for V_{CC} = ± 15 V, I_{REF} = 2.0 mA, T_A = −55°C to +125°C for μA0801, T_A = 0°C to 70°C for μA0801E, μA0801C. Output characteristics refer to both $\overline{I_{OUT}}$ and I_{OUT}.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
	Resolution			8	8	8	bits
	Monotonicity			8	8	8	bits
	Non-linearity	μA0801, μA0801E μA0801C				±0.19 ±0.39	% FS
t_S	Settling Time	To ± ½ LSB, all bits switched ON or OFF T_A = 25°C	μA0801		85	135	ns
			μA0801E, μA0801C		85	150	
t_{PLH}, t_{PHL}	Propagation Delay	T_A = 25°C	Each bit		35	60	ns
			All bits switched		35	60	ns
TCI_{FS}	Full Scale Temperature Coefficient				± 10	±50	ppm/°C
V_{OC}	Output Voltage Compliance	Full scale current change < ½ LSB, R_{OUT} > 20 mΩ		−10		+18	V
I_{FS4}	Full Scale Current	V_{REF} = 10.000 V, R_{14}, R_{15} = 5.000 kΩ T_A = 25°C	μA0801E μA0801, μA0801C	1.940	1.990	2.040	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$	μA0801, μA0801E		± 1.0	±8.0	μA
			μA0801C		± 2.0	± 16	
I_{ZS}	Zero Scale Current		μA0801, μA0801E		0.2	2.0	μA
			μA0801C		0.2	4.0	

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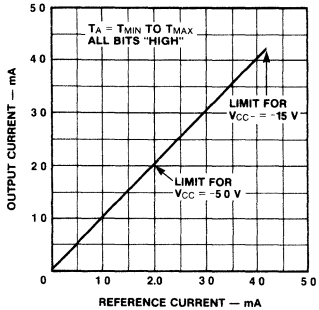
Electrical Characteristics (Cont.)
These specifications apply for V_{CC} = ±15 V, I_{REF} = 2.0 mA, T_A = −55°C to +125°C for μA0801, T_A = 0°C to 70°C for μA0801E, μA0801C. Output characteristics refer to both $\overline{I_{OUT}}$ and I_{OUT}.

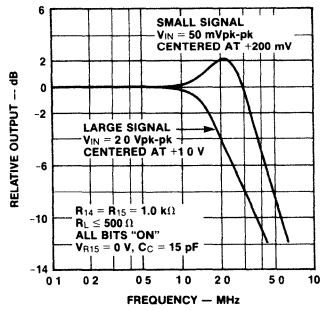
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{FSR}	Output Current Range	$R_{14,\ 15}$ = 5.000 kΩ V_{REF} = +15.00 V, V_{CC-} = −10 V V_{REF} = +25.0 V, V_{CC-} = −12 V			2.1 4.2	mA mA
V_{IL} V_{IH}	Logic Input LOW Voltage Logic Input HIGH Voltage	V_{LC} = 0 V	 2.0		0.8	V V
I_{IL} I_{IH}	Logic Input LOW Current Logic Input HIGH Current	V_{LC} = 0 V, V_{IN} = −10 V to +0.8 V V_{IN} = 2.0 V to 18 V		−2.0 0.002	−10 10	μA μA
V_{IS}	Logic Input Swing	V_{CC-} = −15 V	−10		+18	V
V_{THR}	Logic Threshold Range	V_{CC} = ±15 V	−10		+13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate		4.0	8.0		mA/μs
$PSSI_{FS+}$ $PSSI_{FS-}$	Power Supply Sensitivity	V_{CC+} = 4.5 V to 18 V V_{CC-} = −4.5 V to −18 V I_{REF} = 1.0 mA		0.0003 0.002	0.01 0.01	%/% %/%
I+ I−	Power Supply Current	V_{CC} = ±5.0 V, I_{REF} = 1.0 mA		2.3 −4.3	3.8 −5.8	mA
I+ I−		V_{CC+} = +5.0 V, V_{CC-} = −15 V, I_{REF} = 2.0 mA		2.4 −6.4	3.8 −7.8	
I+ I−		V_{CC} = ±15 V, I_{REF} = 2.0 mA		2.5 −6.5	3.8 −7.8	
P_D	Power Dissipation	V_{CC} = ±5.0 V, I_{REF} = 1.0 mA		33	48	mW
		V_{CC+} = +5.0 V, V_{CC-} = −15 V, I_{REF} = 2.0 mA		108	136	mW
		V_{CC} = ±15 V, I_{REF} = 2.0 mA		135	174	mW

Typical Performance Curves

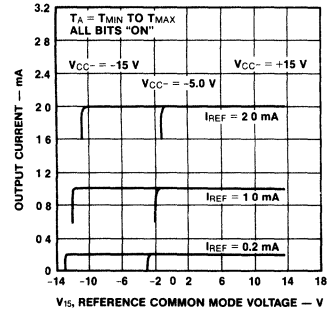
Full Scale Current as a Function of Reference Current



Reference Input Frequency Response



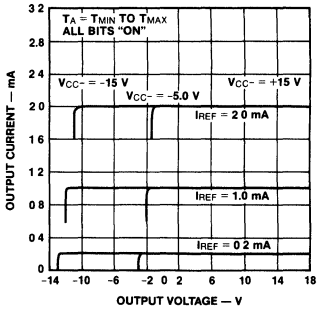
Reference AMP Common Mode Range



Note
Positive common mode range is always (V_{CC-}) +1.5V

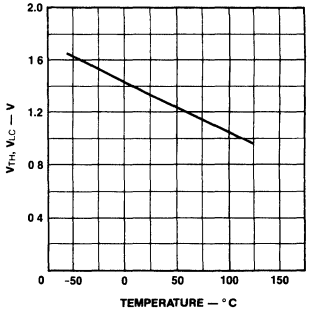
Typical Performance Curves (Cont.)

Output Current as a Function of Output Voltage (Output Voltage Compliance)

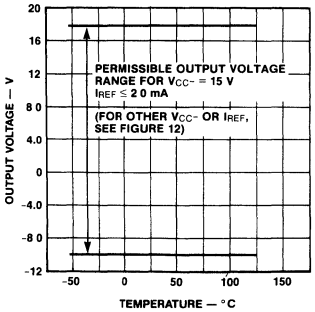


Note
Positive common mode range is always $(V_{CC}+) - 1.5V$

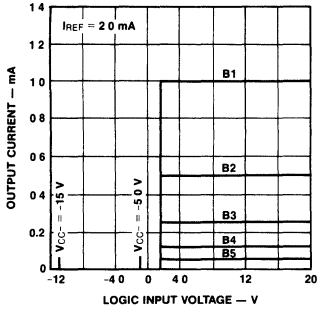
$V_{TH} - V_{LC}$ as a Function of Temperature



Output Voltage Compliance as a Function of Temperature

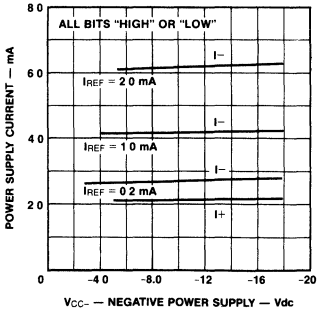


Bit Transfer Characteristics

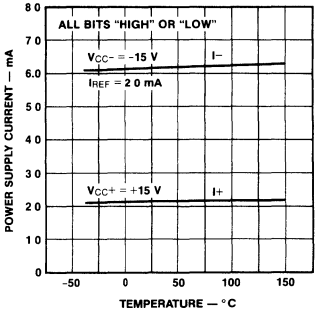


See Note below.

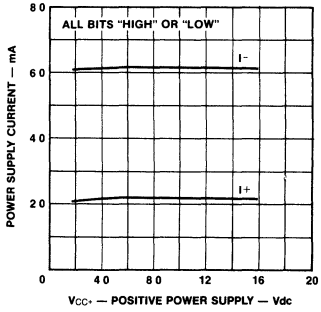
Power Supply Current as a Function of V_{CC-}



Power Supply Current as a Function of Temperature



Power Supply Current as a Function of V_{CC+}

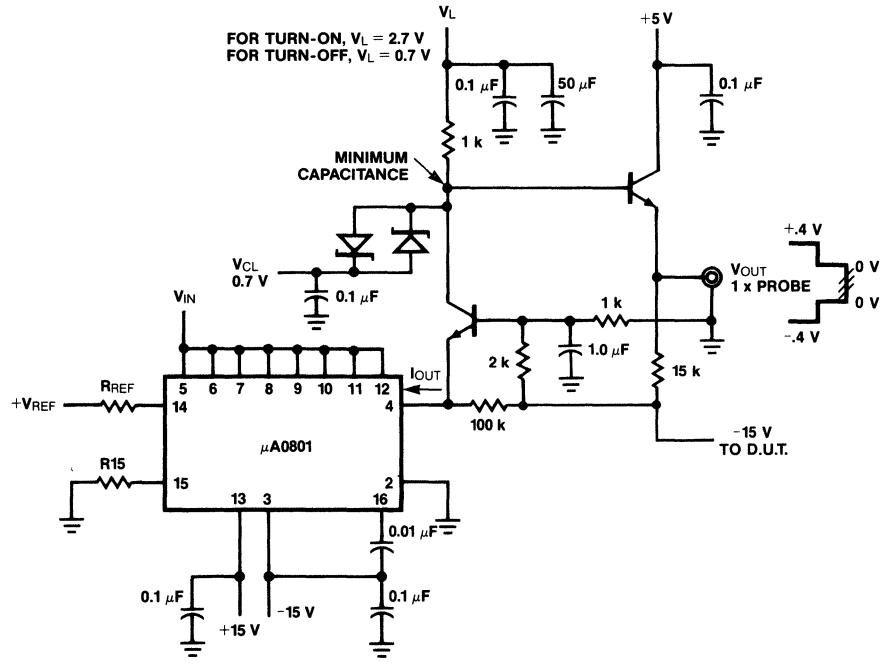


Note
B1 through B8 have identical transfer characteristics. Bits are fully switched, with less than 1/2 LSB error. At less than ± 100 mV from actual threshold, these switching points are guaranteed to lie between 0.8 and 2.0 V over the operating temperature range (V_{LC} = 0.0 V)

7

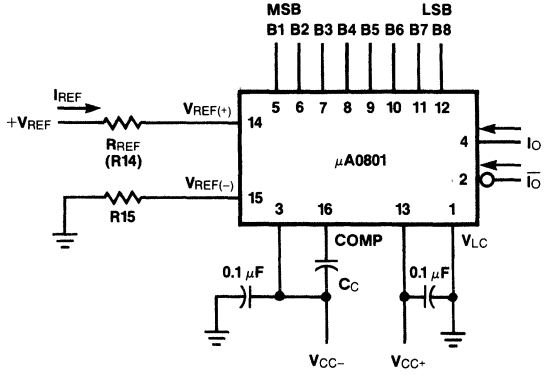
Test Circuits

Fig. 1 Settling Time Measurement



Typical Applications

Fig. 1 Basic Positive Reference Operation



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$
For all logic states

For fixed reference, TTL operation, typical values are:
$V_{REF} = +10.000$ V
$R_{REF} = 5.000$ k
$R_{15} \approx R_{REF}$
$C_C = 0.01$ μF
$V_{LC} = 0$ V (GROUND)

Typical Applications (Cont.)

Fig. 2 Recommended Full Scale Adjustment Circuit

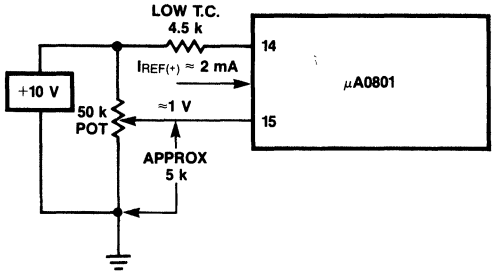
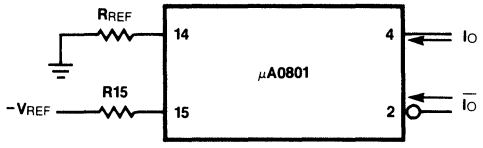


Fig. 3 Basic Negative Reference Operation

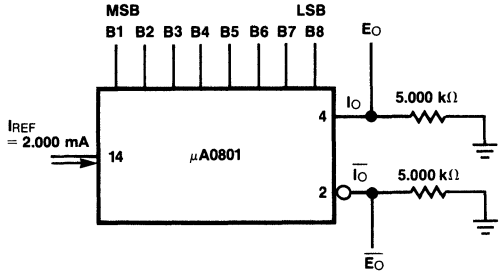


$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note

R_{REF} sets I_{FS}; R15 is for bias current cancellation.

Fig. 4 Basic Unipolar Negative Operation

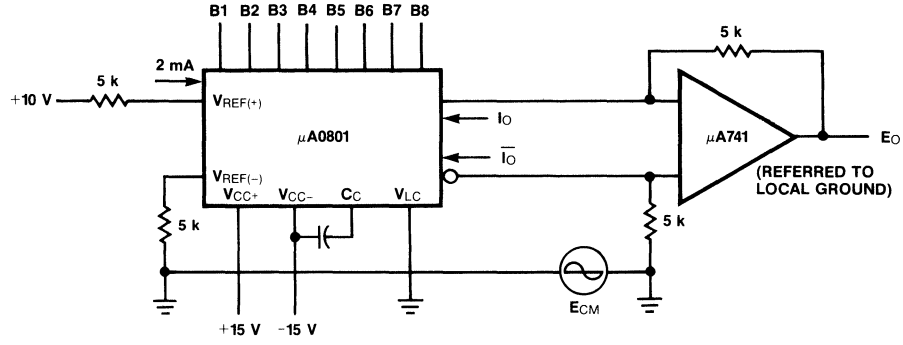


	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	.000	−9.960	.000
Full Scale − LSB	1	1	1	1	1	1	1	0	1.984	.008	−9.920	− .040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	.992	−5.000	−4.960
Half Scale − LSB	0	1	1	1	1	1	1	1	.992	1.000	−4.960	−5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	.008	1.984	− .040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	.000	1.992	.000	−9.960

7

Typical Applications (Cont.)

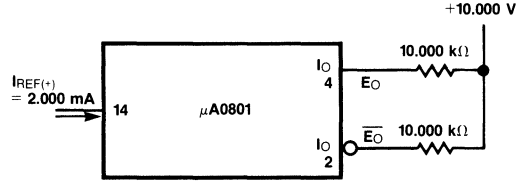
Fig. 5 High Noise Immunity Current To Voltage Conversion



- Provides isolation from ground loops
- Symmetrical ± 10 V output
- Useful within systems between boards
- True complementary/differential current transmission
- High speed analog signal transmission

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos Full Scale − LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	−9.840
Neg Full Scale	0	0	0	0	0	0	0	0	−9.920

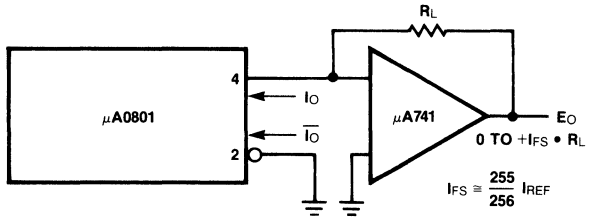
Fig. 6 Basic Bipolar Output Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E}_O$
Pos Full Scale	1	1	1	1	1	1	1	1	− 9.920	+10.000
Pos Full Scale − LSB	1	1	1	1	1	1	1	0	− 9.840	+ 9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	− 0.080	+ 0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+ 0.080
Zero Scale − LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	+ 9.920	− 9.840
Neg Full Scale	0	0	0	0	0	0	0	0	+10.000	− 9.920

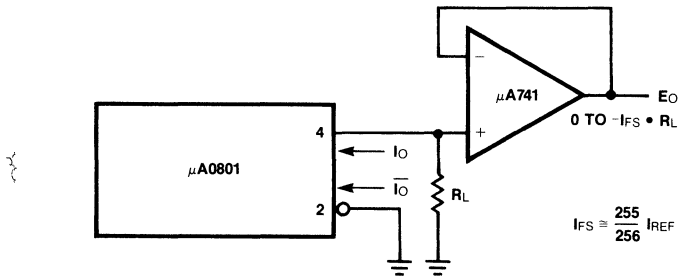
Typical Applications (Cont.)

Fig. 7 Positive Low Impedance Output Operation



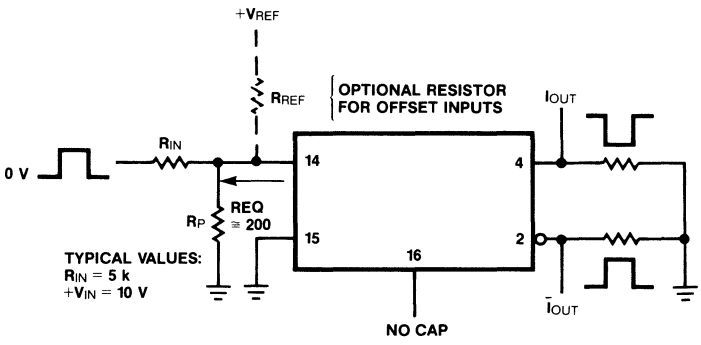
For complementary output (operation as negative logic DAC), connect inverting input of Op-Amp to $\overline{I_O}$ (Pin 2); connect I_O (Pin 4) to ground.

Fig. 8 Negative Low Impedance Output Operation



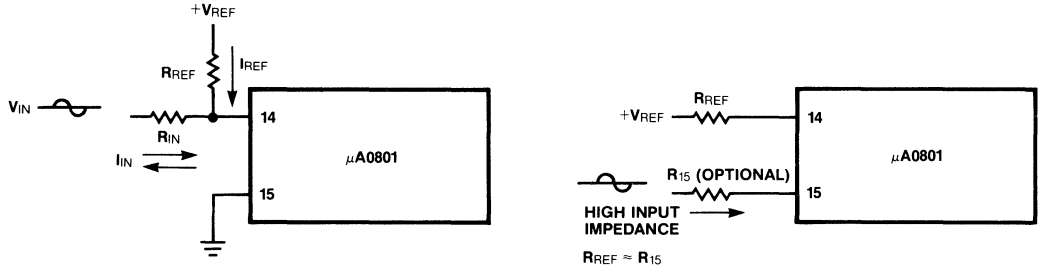
For complementary output (operation as negative logic DAC), connect inverting input of Op-Amp to $\overline{I_O}$ (Pin 2); connect I_O (Pin 4) to ground.

Fig. 9 Pulsed Reference Operation



Typical Applications (Cont.)

Fig. 10 Accommodating Bipolar References

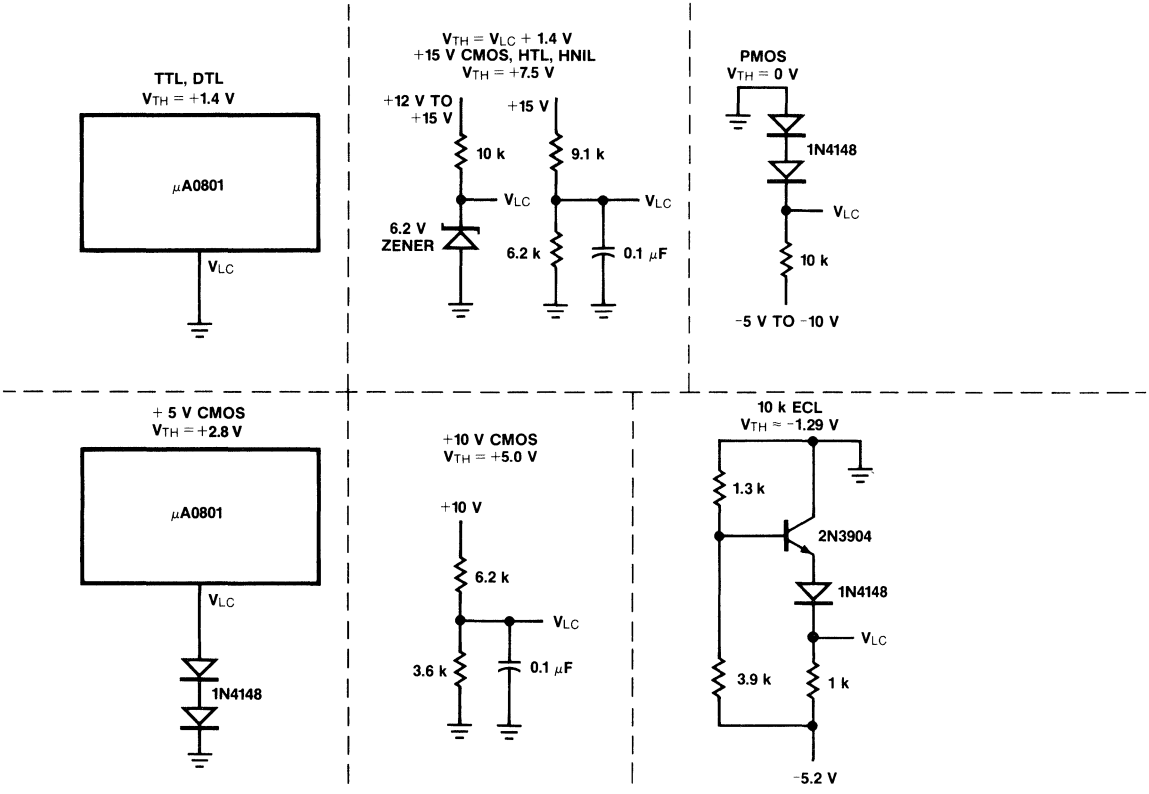


$I_{REF} \geq$ peak negative swing of I_{IN}

$R_{REF} \approx R_{15}$

$+V_{REF}$ must be above peak positive swing of V_{IN}

Fig. 11 Interfacing With Various Logic Families



Note

Do not exceed negative logic input range of DAC

Cross Reference Information

Part No.	Temperature Range	Nonlinearity
μA0801DM (DAC-08Q)	−55°C to +125°C	±0.19%
μA0801EDC (DAC-08EQ)	0°C to +70°C	±0.19%
μA0801EPC (DAC-08EP)	0°C to +70°C	±0.19%
μA0801CDC (DAC-08CQ)	0°C to +70°C	±0.39%
μA0801CPC (DAC-08CP)	0°C to +70°C	±0.39%

FAIRCHILD

A Schlumberger Company

μA0802 (MC1508/1408) Series 8-Bit Multiplying D/A Converter

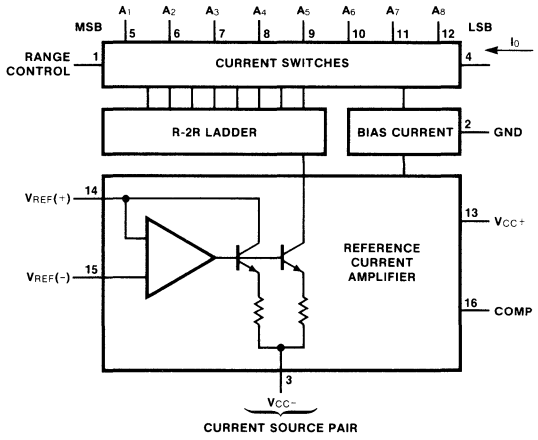
Data Aquisition Products

Description

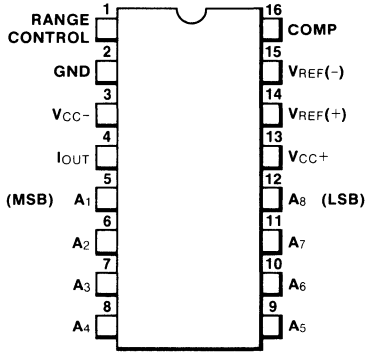
The μA0802, μA0802A, μA0802B, and μA0802C are monolithic 8-bit multiplying Digital-to-Analog Converters constructed using the Fairchild Planar Epitaxial process. It is designed for use where the output current is a linear product of an 8-bit digital word and an analog input voltage. The μA0802 is specified for the military temperature range (−55°C to +125°C) and the μA0802A, μA0802B and μA0802C are specified for 0°C to 70°C operation. The μA0802 series are pin-for-pin replacements for the MC1508/1408 and SSS1408 devices.

- **RELATIVE ACCURACY ±0.1% ERROR MAXIMUM μA0802H**
- **RELATIVE ACCURACY ±0.19% ERROR MAXIMUM μA0802, μA0802A**
- **7 AND 6-BIT ACCURACY AVAILABLE μA0802B, μA0802C**
- **FAST SETTLING TIME TO 1/2 LSB—85 ns**
- **NON-INVERTING DIGITAL INPUTS ARE TTL AND CMOS COMPATIBLE**
- **OUTPUT VOLTAGE SWING +0.5 V to −5.0 V**
- **HIGH-SPEED MULTIPLYING INPUT SLEW RATE 4.0 mA/μs**
- **STANDARD SUPPLY VOLTAGES +5.0 V AND −5.0 V TO −15 V**
- **LOW FULL SCALE CURRENT DRIFT +10 PPM/°C TYPICALLY**
- **LOW POWER CONSUMPTION 33 mW @ ±5 V**
- **LOW COST**

Equivalent Circuit



Connection Diagram 16-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA0802	Ceramic DIP	6B	μA0802DM
μA0802A	Ceramic DIP	6B	μA0802ADC
μA0802A	Molded DIP	9B	μA0802APC
μA0802B	Ceramic DIP	6B	μA0802BDC
μA0802B	Molded DIP	9B	μA0802BPC
μA0802C	Ceramic DIP	6B	μA0802CDC
μA0802C	Molded DIP	9B	μA0802CPC

Additional Order Information

Type	Temperature Range	Relative Accuracy
μA0802 (MC1508L-8)	−55°C to +125°C	±0.19%
μA0802A (MC1408L-8)	0°C to +70°C	±0.19%
μA0802B (MC1408L-7)	0°C to +70°C	±0.39%
μA0802C (MC1408L-6)	0°C to +70°C	±0.78%

7

Absolute Maximum Ratings T_A = +25°C unless otherwise noted

V_{CC+}	5.5 V
V_{CC-}	−16.5 V
Digital Input Voltage (5 V to 12 V)	+5.5 V
Applied Output Voltage	0.5 V to −5.2 V
Reference Current (I14)	5.0 mA
Reference Amplifier Inputs (V_{14}, V_{15})	5.5 V, −16.5 V
Operating Temperature Range	
μA0802	−55°C to +125°C
μA0802A, μA0802B, μA0802C	0°C to +70°C
Storage Temperature Range	
Pin Temperatures	
Ceramic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Electrical Characteristics V_{CC+} = +5.0 V, V_{CC-} = −15 V, $V_{REF}/R14$ = 2.0 mA, μA0802 T_A = −55°C to 125°C. All digital inputs at HIGH logic level.

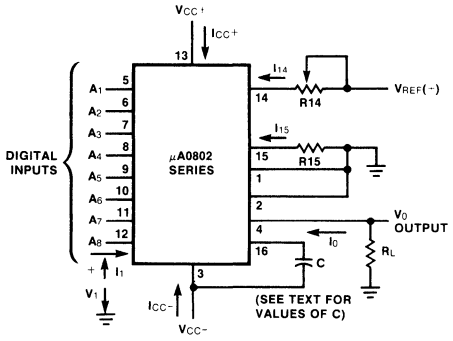
Symbol	Characteristic	Figure	Min	Typ	Max	Unit
E_r	Relative Accuracy (Error Relative to Full Scale I_O) μA0802, μA0802A μA0802B (Note 1) μA0802C (Note 1)	3			 ±0.19 ±0.39 ±0.78	%
t_s	Setting Time to Within ½ LSB (includes t_{PLH}) (T_A = +25°C) (Note 2)	4		85	135	ns
t_{PLH}, t_{PHL}	Propagation Delay Time T_A = +25°C	4		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		PPM/°C
V_{IH} V_{IL}	Digital Input Logic Levels (MSB) HIGH Level, Logic "1" LOW Level, Logic "0"	2	 2.0		 0.8	V
I_{IH} I_{IL}	Digital Input Current (MSB) HIGH Level, V_{IH} − 5.0 V LOW Level, V_{IL} − 0.8 V	2		 0 −0.4	 0.04 −0.8	mA
I_{15}	Reference Input Bias Current (Pin 15)	2		−1.0	−5.0	μA
I_{OR}	Output Current Range V_{CC} = −5.0 V V_{CC} = −6.0 to −15 V	2	 0 0	 2.0 2.0	 2.1 4.2	mA
I_O	Output Current V_{REF} = 2.000 V, R14 = 1000 Ω	2	 1.9	 1.99	 2.1	mA mA
$I_{O(min)}$	Output Current (All bits LOW)	2		0	4.0	μA
V_O	Output Voltage Compliance ($E_r \leq 0.19\%$ at T_A = +25°C) V_{CC-} = −5 V V_{CC-} below −10 V	2			 −0.55, +0.4 −5.0, +0.5	V
SR I_{REF}	Reference Current Slew Rate	5		4.0		mA/μs
PSRR(−)	Output Current Power Supply Sensitivity			0.5	2.7	μA/V
I_{CC+} I_{CC-}	Power Supply Current (All bits LOW)	2		+13.5 −7.5	+22 −13.0	mA
V_{CCR+} V_{CCR-}	Power Supply Voltage Range (T_A = +25°C)	2	+4.5 −4.5	+5.0 −15	+5.5 −16.5	V
P_D	Power Dissipation All bits LOW V_{CC-} = −5.0 V V_{CC-} = −15 V All bits HIGH V_{CC-} = −5.0 V V_{CC-} = −15 V	2		 105 190 90 160	 170 305	mW

Notes

1. All current switches are tested to guarantee at least 50% of rated output current.
2. All bits switched.

Test Circuits

Fig. 1 Notation Definitions



Notes

Typical Values: R14 = R15 = 1 k

V_{REF} = +20 V

C = 15 pF

V_1 and I_1 apply to inputs A_1 thru A_8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

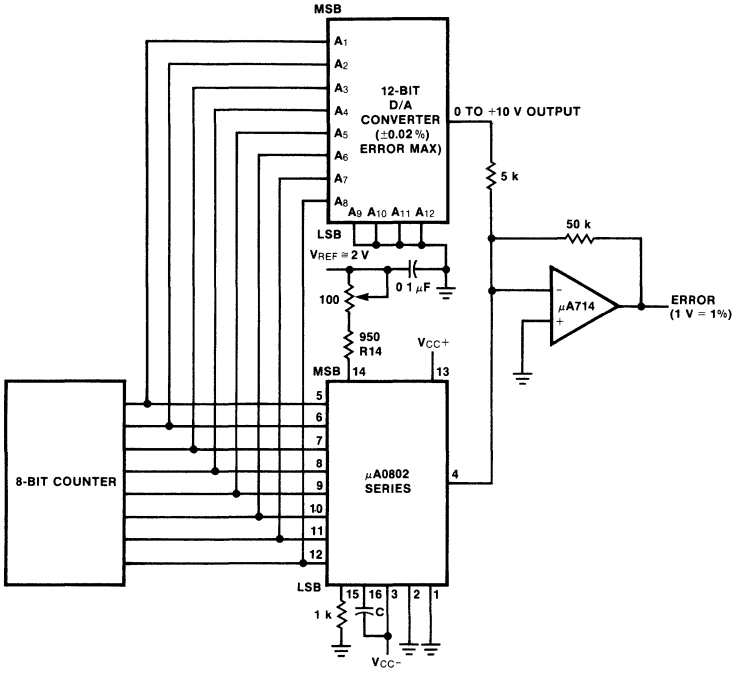
$$I_O = K\left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right]$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at HIGH level

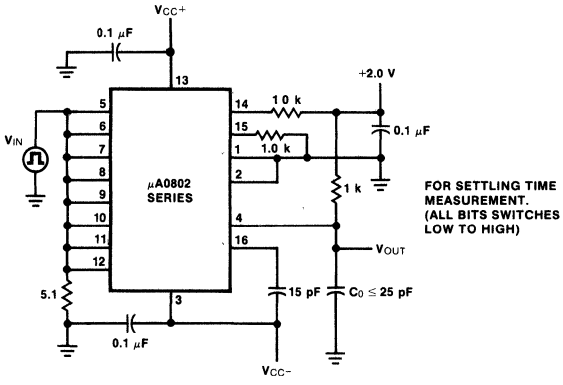
A_N = "0" if A_N is at LOW level

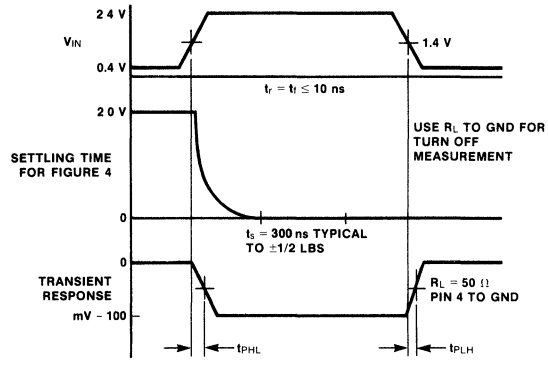
Fig. 2 Relative Accuracy Test Circuit



Test Circuits (Cont.)

Fig. 3 Transient Response and Settling Time





Applications

- Tracking a/d Converters
- Successive Approximation a/d Converters
- 2 1/2 Digit Panel Meters and DVMs
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

Fig. 2 Negative V_{REF}

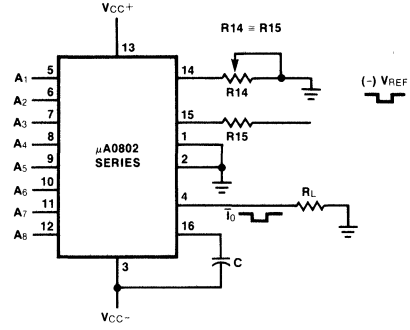
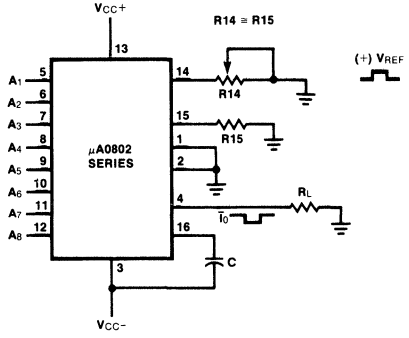
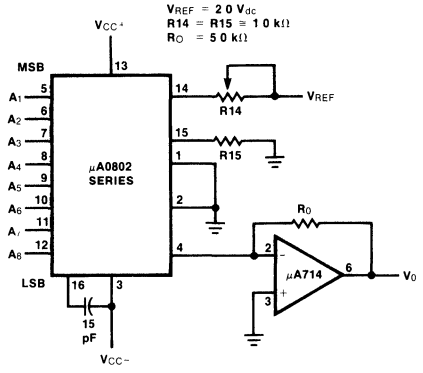


Fig. 1 Positive V_{REF}



Applications (Cont.)

Fig. 3 Use with Current-to-Voltage Converting OP AMP



Notes

Theoretical V_O

$$V_O = \frac{V_{REF}}{R14}(R_O)\left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right]$$

Adjust V_{REF} R14 or R_O so that V_O with all digital inputs at HIGH level is equal to 9.961 Volts.

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\ \frac{255}{256} = 9.961\ V$$

7

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μA3680 Quad Telephone Relay Driver

Telecommunication Products

Description

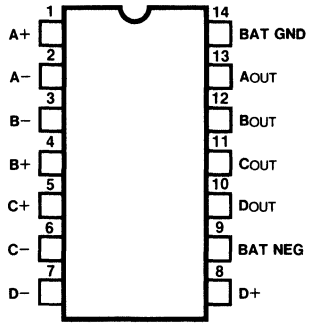
The 3680 relay driver is a monolithic integrated circuit designed to interface −48 V relays to TTL or other logic systems in telephony applications. The device has a 50 mA source capability and operates from −48 V battery power. The quad configuration increases board density in typical line card applications. Since there can be considerable noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a high common-mode range (±20 V referenced to battery ground). Also, each driver has common-mode range separate from the other drivers in the package. Low differential input current (typically 100 μA) draws low power from the driving circuit. Differential inputs permit either inverting or non-inverting operation. A clamp network is incorporated in the driver outputs, eliminating the need for an external network to quench the high voltage inductive backswing caused when the relay is turned off. A fail-safe feature is incorporated to insure that the driver will be off if the V_{IN+} input or both inputs are open. Standby power (driver off) is very low, typically 50 μW per driver.

- **−48 V BATTERY OPERATION**
- **50 mA OUTPUT CAPABILITY**
- **TTL/CMOS-COMPATIBLE COMPARATOR INPUT**
- **HIGH COMMON-MODE INPUT VOLTAGE RANGE**
- **VERY LOW INPUT CURRENT**
- **FAIL-SAFE DISCONNECT FEATURE**
- **BUILT-IN OUTPUT CLAMP DIODE**

Absolute Maximum Ratings (Notes 1 and 2)

	Max	Min
BAT NEG	+0.5 V	−70 V
Input Voltage (BAT NEG ≥ −50 V)	+20 V	BAT NEG −0.5 V
Differential Input Voltage ($V_{IN+} - V_{IN-}$)	±20 V	
Output Current ($L_L \leq 5$ H)	50 mA	
Output Current (R_L)	100 mA	
Power Dissipation (85°C still air with package soldered in PC board)		
Ceramic DIP	650 mW	
Molded DIP	930 mW	
Pin Temperature (soldering)		
Ceramic DIP (60 s)	300°C	
Molded DIP (10 s)	260°C	
Storage Temperature	−65°C to +150°C	

Connection Diagram
14-Pin DIP

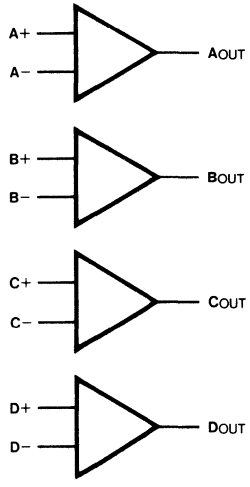


(Top View)

Order Information

Type	Package	Code	Part No.
μA3680	Ceramic DIP	6A	μA3680DC
μA3680	Molded DIP	9A	μA3680PC

Logic Diagram



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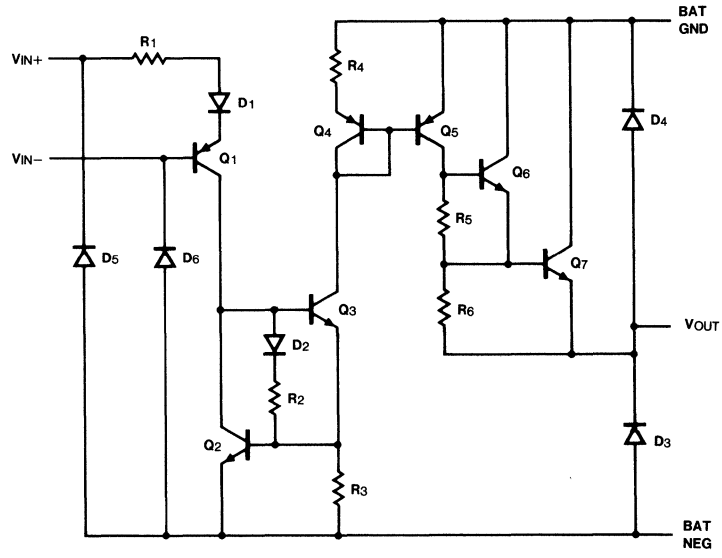
Notes on following pages.

Circuit Schematic (1/4 of circuit shown)



Electrical Characteristics Over Recommended Operating Conditions unless specified otherwise. Typical values for BAT NEG = −52 V, and T_A = 25°C.

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
V_{IH}	Logic "1" Differential Input Voltage			1.3	2.0	V
V_{IL}	Logic "0" Differential Input Voltage		0.8	1.3		V
I_{INH}	Logic "1" Input Current	V_{IN+} = 2 V, V_{IN-} = 0 V_{IN+} = 7 V, V_{IN-} = 0		40 375	100 1000	μA μA
I_{INL}	Logic "0" Input Current	V_{IN+} = 0.4 V, V_{IN-} = 0 V_{IN+} = −7 V, V_{IN-} = 0		+0.01 −1	+5 −100	μA μA
V_{OL}	Output On Voltage	I_{OL} = 50 mA	−2.1	−1.6		V
I_{OFF}	Output Leakage	V_{OUT} = BAT NEG		+2	+100	μA
I_{FS}	Fail-Safe Output Leakage	V_{OUT} = BAT NEG (Inputs open)		+2	+100	μA
I_{LC}	Output Clamp Leakage Current	V_{OUT} = BAT GND		−2	−100	μA
V_C	Output Clamp Voltage	I_{CLAMP} = +50 mA, Referenced to BAT NEG	−1.2	−0.9		V
V_P	Positive Output Clamp Voltage	I_{CLAMP} = −50 mA, Referenced to BAT GND		0.9	1.2	V
$I_{B(ON)}$	Supply Current	All drivers On		−2	−4.4	mA
$I_{B(OFF)}$	Supply Current	All drivers Off		−1	−100	μA
$t_{PD(ON)}$	Propagation Delay to Driver On	L = 1H, R_L = 1k, V_{IN} = 3 V pulse		1	10	μs
$t_{PD(OFF)}$	Propagation Delay to Driver Off	L = 1H, R_L = 1k, V_{IN} = 3 V pulse		1	10	μs

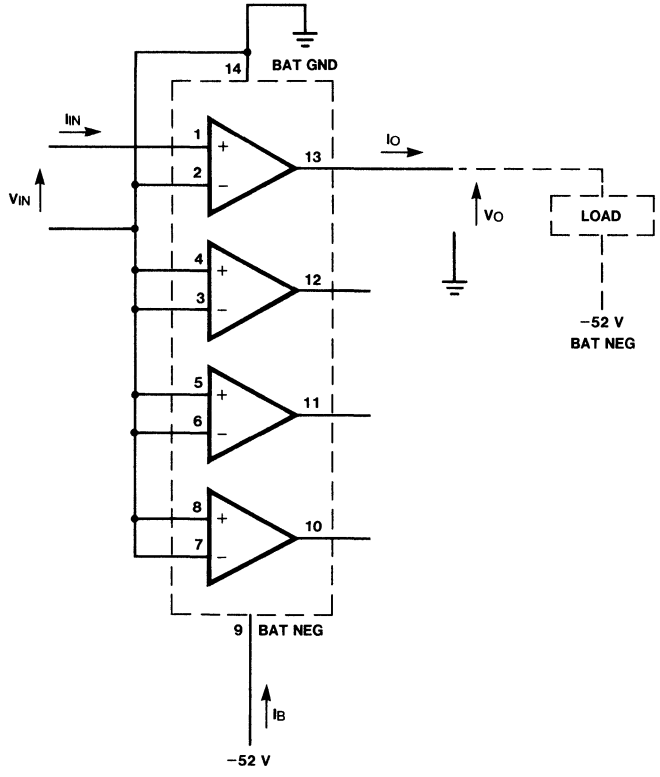
Notes

1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for operating temperature range, they are not meant to imply that the device should be operated at these limits. The electrical characteristic table includes conditions for actual device operation.
2. All voltages are with respect to BAT GND.

Recommended Operating Conditions

Characteristic	Min	Max	Unit
Battery Voltage (BAT NEG)	−60	−10	V
Input Voltage	−10	+10	V
Logic On Voltage ($V_{IN+} - V_{IN-}$)	+2	+10	V
Logic Off Voltage ($V_{IN+} - V_{IN-}$)	−10	+0.8	V
Temperature Range	−25	+85	°C

DC Test Circuit



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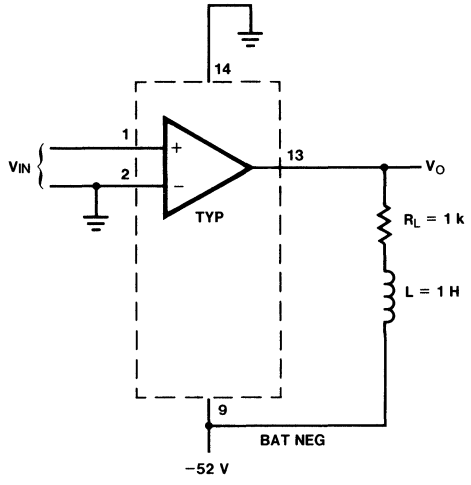
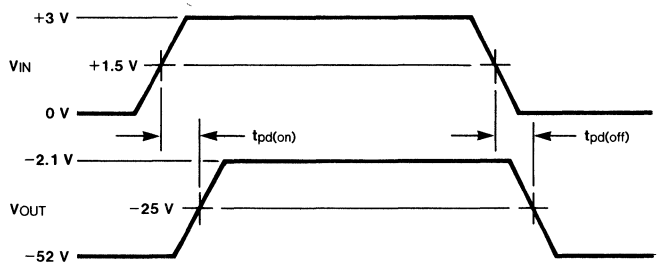
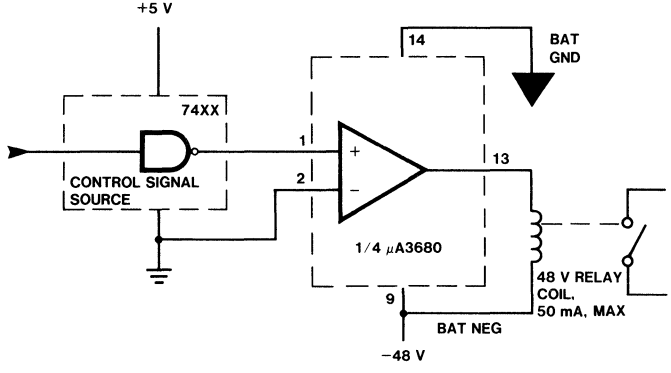
AC Test Circuit and Waveforms





Typical Applications



FAIRCHILD
A Schlumberger Company

μA5116
μ255-Law Companding Codec

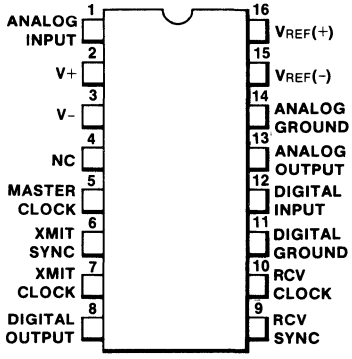
Telecommunication Products

Description

The 5116 is a monolithic CMOS Companding Codec containing both an analog-to-digital converter and a digital-to-analog converter which have transfer characteristics conforming to the μ255-Law companding code. This device performs a coder-decoder function designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in PCM systems. Digital input and output are in serial format using sign-plus-magnitude coding. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64 kb/s to 2.1 Mb/s rate with analog signal sampling occurring at an 8 kHz rate. A SYNC pulse input is provided for synchronizing transmission and reception of multichannel information being multiplexed over a single transmission line.

- **EXCEEDS D3 CHANNEL BANK SPECIFICATIONS**
- **LOW POWER DISSIPATION 30 mW TYPICAL**
- **SYNCHRONOUS/ASYNCHRONOUS OPERATION**
- **ON-CHIP S/H CIRCUIT**
- **ON-CHIP OFFSET NULL CIRCUIT**
- **SEPARATE ANALOG AND DIGITAL GROUNDS**
- **64 kb/s to 2.1 Mb/s SERIAL DATA RATE**
- **±5V POWER SUPPLY OPERATION**

Connection Diagram
16-Pin DIP

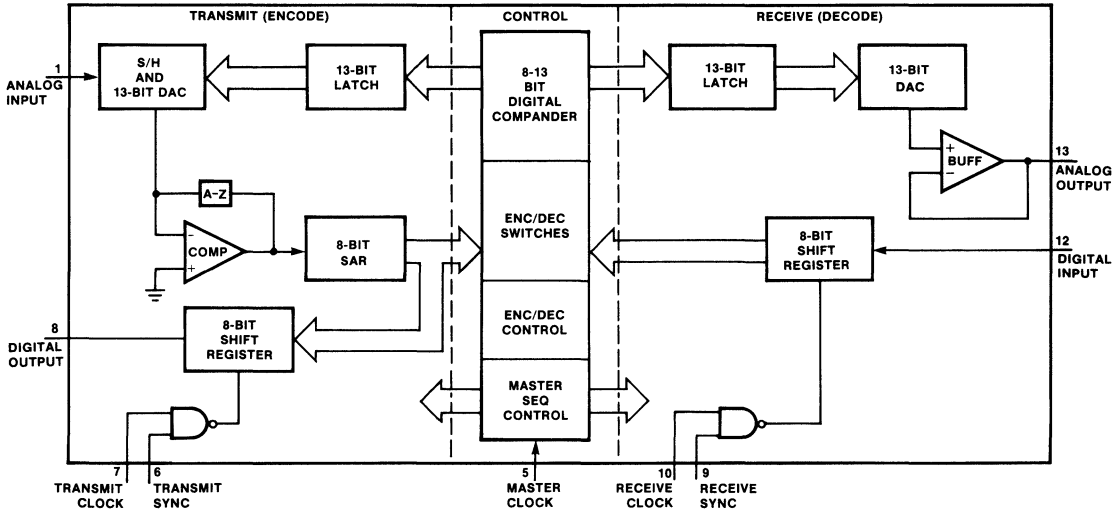


(Top View)

Order Information

Type	Package	Code	Part No.
μA5116	Ceramic DIP	FW	μA5116DC
μA5116	Ceramic DIP (Side Brazed)	FB	μA5116JC

Block Diagram



Pin 4 = not connected

8

Absolute Maximum Ratings (Note)

Supply Voltage (V+)	+6
Supply Voltage (V−)	−6
Analog Input Range	$V- \leq V_{IN} \leq V+$
Digital Input Range	$-0.5\ V \leq V_{IN} \leq V+$
Reference Voltage $V_{REF}(+)$	$-0.5\ V \leq V_{REF}(+) \leq V+$
Reference Voltage $V_{REF}(-)$	$V- \leq V_{REF}(-) \leq 0.5\ V$
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

Note
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

Functional Description (Refer to Block Diagram)

Positive and Negative Reference Voltages, ($V_{REF}(+)$ and $V_{REF}(-)$ Pins 16 and 15)
These inputs provide the conversion references for the digital-to-analog converters in the 5116. $V_{REF}(+)$ and $V_{REF}(-)$ must maintain 100 ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

Analog Input, Pin 1
Voice-frequency analog signals which are bandwidth-limited to 4 kHz are input at this pin. Typically, they are then sampled at an 8 kHz rate (Refer to *Figure 6*). The Analog Input must remain between $V_{REF}(+)$ and $V_{REF}(-)$ for accurate conversion.

Master Clock, Pin 5
This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV Clock, XMIT SYNC or XMIT Clock and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to *Figure 2* for the Timing Diagram)
This input is synchronized with XMIT Clock. When XMIT SYNC goes HIGH, the Digital Output is activated and the A/D conversion begins on the next positive edge of Master Clock. The conversion by Master Clock can be asynchronous with XMIT Clock. The serial output data is clocked out by the positive edges of XMIT Clock. The negative edge of XMIT SYNC causes the Digital Output to become 3-state. XMIT SYNC must go LOW for at least 1 Master Clock prior to the transmission of the next digital word. (Refer to *Figure 10.*)

XMIT Clock, Pin 7 (Refer to *Figure 2* for the Timing Diagram)
The on-chip 8-bit output shift register of the 5116 is unloaded at the clock rate present on this pin. Clock rates of 64 kHz to 2.1 MHz can be used for XMIT Clock. The positive edge of the internal clock transfers the data from the master to the slave of a master-slave flip-flop (refer to *Figure 7*). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT Clock, XMIT SYNC will determine when the first positive edge of the internal clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV SYNC, Pin 9 (Refer to *Figure 3* for the Timing Diagram)
This input is synchronized with RCV Clock, and serial data is clocked in by RCV Clock. Duration of the RCV SYNC pulse is approximately eight RCV Clock periods. The conversion from digital-to-analog starts after the negative edge of RCV SYNC pulse (refer to *Figure 6*). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay LOW for 17 Master Clocks (minimum) before the next digital word is to be received (Refer to *Figure 11*).

RCV Clock, Pin 10 (Refer to *Figure 3* for Timing Diagram)
The on-chip 8-bit shift register for the 5116 is loaded at the clock rate present on this pin. Clock rates of 64 kHz to 2.1 MHz can be used for RCV Clock. Valid data should be applied to the digital input before the positive edge of the internal clock (refer to *Figure 7).* This set-up time, t_{rds}, allows the data to be transferred into the Master of a master-slave flip-flop. The positive edge of the internal clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{rdh}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV Clock, RCV SYNC will determine when the first positive edge of internal clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

Digital Output, Pin 8
The 5116 output register stores the 8-bit encoded sample of the Analog Input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT Clock. When XMIT SYNC is LOW, the Digital Output is an open circuit. When XMIT SYNC is HIGH, the state of the Digital Output is determined by the value of the output bit in the serial shift register. The output is composed of a sign bit, 3 chord bits, and 4 step bits.

The sign bit indicates the polarity of the Analog Input while the chord and step bits indicate the magnitude. In the first chord, the step bit has a value of 0.6 mV. In the second chord, the step bit has a value of 1.2 mV. This doubling of the step value continues for each of the next six successive chords.

Each chord has a specific value and the step bits, 16 in each chord, specify the displacement from that value (refer to *Table 1*. Thus the output, which follows the μ255-Law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit a/d converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the a/d converter (μ255-Law Encoder) is shown in *Figure 8*.

Digital Input, Pin 12
The 5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV Clock. The timing diagram is shown in *Figure 3*. When RCV SYNC goes HIGH, the 5116 uses RCV Clock to clock the serial data into its input register. RCV SYNC goes LOW to indicate the end of serial input data. The eight bits of the input data have the same functions described for the Digital Output. The transfer characteristic of the d/a converter (μ255-Law Decoder) is shown in
Figure 9.

Analog Output, Pin 13
The Analog Output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with (sin x)/x correction to recreate the sampled voice signal.

Operation of Codec With 64 kHz XMIT/RCV Clock Frequencies
XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for one Master Clock period (minimum) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 Master Clock periods (minimum) before the next digital word is received (refer to *Figures 10* and *11*).

Offset Null
The offset null feature of the 5116 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate a/d conversion for inputs near ground. There is no offset adjust of the output amplifier since the output is intended to be ac-coupled to the external filter and the resultant dc error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the Analog Input. Therefore, for an Analog Input of 0 V, the sign bit will be stable.

Table 1 Digital Output Code for 5116

	Chord Code	Chord Value	Step Value
1.	000	0.0 mV	0.613 mV
2.	001	10.11 mV	1.226 mV
3.	010	30.3 mV	2.45 mV
4.	011	70.8 mV	4.90 mV
5.	100	151.7 mV	9.81 mV
6.	101	313 mV	19.61 mV
7.	110	637 mV	39.2 mV
8.	111	1.284 V	78.4 mV

Example:

1	011	0010 = +70.8 mV + (2 x 4.90 mV)
Sign Bit	Chord	Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

8

Electrical Operating Characteristics

Power Supply Requirements

Symbol	Characteristic	Min	Typ	Max	Unit
V+	Positive Supply Voltage	4.75	5.0	5.25	V
V−	Negative Supply Voltage	−5.25	−5.0	−4.75	V
$V_{REF}(+)$	Positive Reference Voltage (Note 1)	2.375	2.5	2.625	V
$V_{REF}(-)$	Negative Reference Voltage (Note 1)	−2.625	−2.5	−2.375	V

DC Characteristics V+ = 5 V, V− = −5 V, $V_{REF}(+)$ = 2.5 V, V_{REF} (−) = −2.5 V.

Symbol	Characteristic	Min	Typ	Max	Unit
R_{INAS}	Analog Input Resistance During Sampling (Note 2)		2		kΩ
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ
C_{INA}	Analog Input Capacitance		150	250	pF
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	±8	mV
R_{OUTA}	Analog Output Resistance		20	50	Ω
I_{OUTA}	Analog Output Current	0.25	0.5		mA
$V_{OFFSET/O}$	Analog Output Offset Voltage		±200	±850	mV
I_{IL}	Logic Input LOW Current (V_{IN} = 0.8 V) Digital Input, Clock Input, SYNC Input (Note 3)		±0.1	±10	μA
I_{IH}	Logic Input HIGH Current (V_{IN} = 2.4 V) Digital Input, Clock Input, SYNC Input (Note 3)		−0.25	−0.8	mA
C_{DO}	Digital Output Capacitance		8	12	pF
I_{DOL}	Digital Output Leakage Current		±0.1	±10	μA
V_{OL}	Digital Output LOW Voltage (Note 4)			0.4	V
V_{OH}	Digital Output HIGH Voltage (Note 4)	3.9			V
I+	Positive Supply Current		4	10	mA
I−	Negative Supply Current		2	6	mA
I_{REF+}	Positive Reference Current		4	20	μA
I_{REF-}	Negative Reference Current		4	20	μA

AC Characteristics Refer to *Figures 2* and *3.*

Symbol	Characteristic	Min	Typ	Max	Unit
f_m	Master Clock Frequency	1.5	1.544	2.1	MHz
f_r, f_x	RCV, XMIT Clock Frequency	0.064	1.544	2.1	MHz
PW_{clk}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns
t_{rc}, t_{fc}	Clock Rise, Fall Time (MASTER, XMIT, RCV			25% of PW_{clk}	ns
t_{rs}, t_{fs}	SYNC Rise, Fall Time (XMIT, RCV)			25% of PW_{clk}	ns
t_{Dlr}, t_{Dlf}	Data Input Rise, Fall Time			25% of PW_{clk}	ns
t_{wsx}, t_{wsr}	SYNC Pulse Width (XMIT, RCV)		$\frac{8}{f_x(f_r)}$		μs
t_{ps}	SYNC Pulse Period (XMIT,RCV)		125		μs
t_{xcs}	XMIT Clock-to-XMIT SYNC Delay (Note 5)	50% of $t_{fc}(t_{rs})$			ns
t_{xcsn}	XMIT Clock-to-XMIT SYNC (Negative Edge) Delay	200			ns
t_{xss}	XMIT SYNC Set-Up Time	200			ns
t_{xdd}	XMIT Data Delay (Note 4)	0		200	ns
t_{xdp}	XMIT DATA Present (Note 4)	0		200	ns
t_{xdt}	XMIT Data Three State (Note 4)			150	ns
t_{dof}	Digital Output Fall Time (Note 4)		50		ns
t_{dor}	Digital Output Rise Time (Note 4)		50		ns
t_{src}	RCV SYNC-to-RCV Clock Delay (Note 5)	50% $t_{rc}(t_{fs})$			ns
t_{rds}	RCV Data Set-Up Time (Note 6)	50			ns
t_{rdh}	RCV Data Hold Time (Note 6)	200			ns
t_{rcs}	RCV Clock-to-RCV SYNC Delay	200			ns
t_{rss}	RCV SYNC Set-Up Time (Note 6)	200			ns
t_{sao}	RCV SYNC-to-Analog Output Delay		7		μs
Slew+	Analog Output Positive Slew Rate		1		V/μs
Slew−	Analog Output Negative Slew Rate		1		V/μs
Droop	Analog Output Droop Rate		25		μV/μs

Notes

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging the internal capacitor to within 1/2 LSB (≤ 300 μV) in 20 μs. Therefore, the external source resistance must be 3 kΩ or less. The equivalent circuit during sampling is shown in *Figure 1.*
3. The 5116 will source current through an internal 6 kΩ resistor to help pull up the TTL output. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30 pF with $I_{OH} = -100$ μA, $I_{OL} = 500$ μA.
5. This delay is necessary to avoid overlapping Clock and SYNC.
6. The first bit of data is loaded when SYNC and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

System Characteristics Refer to *Figures 4* and *5*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
S/D	Signal-to-Distortion	35 29 24	39 34 29		dB dB dB	Analog Input = 0 to −30 dBmO Analog Input = −40 dBmO Analog Input = −45 dBmO
GT	Gain Tracking		±0.1 ±0.1 ±0.2	±0.4 ±0.8 ±2.5	dB dB dB	Analog Input = +3 to −37 dBmO Analog Input = −37 to −50 dBmO Analog Input = −50 to −55 dBmO
N_{IC}	Idle Channel Noise		10	18	dBrnC0	Analog Input = 0 V
TLP	Transmission Level Point		+4		dB	600 Ω

Fig. 1 Equivalent Circuit During Sampling

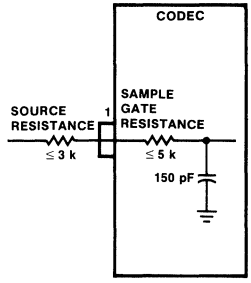
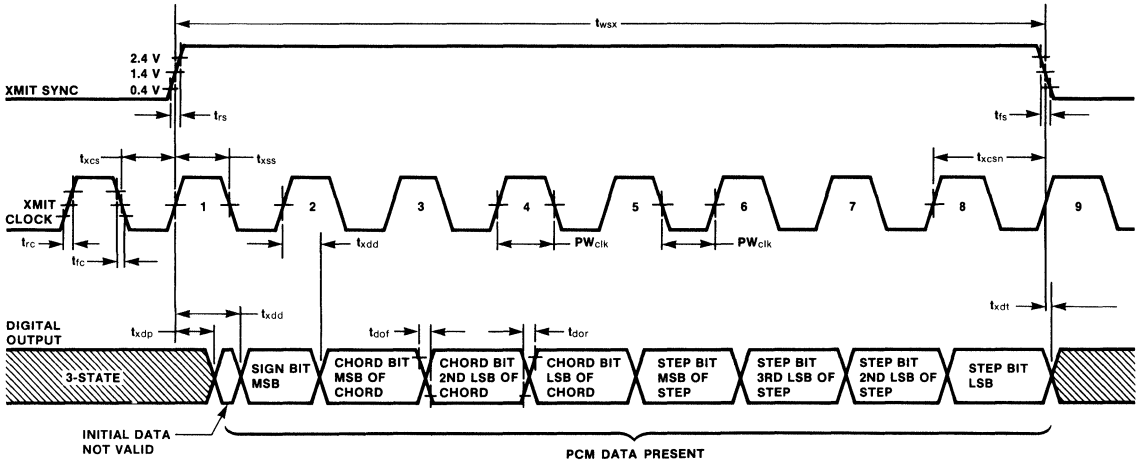
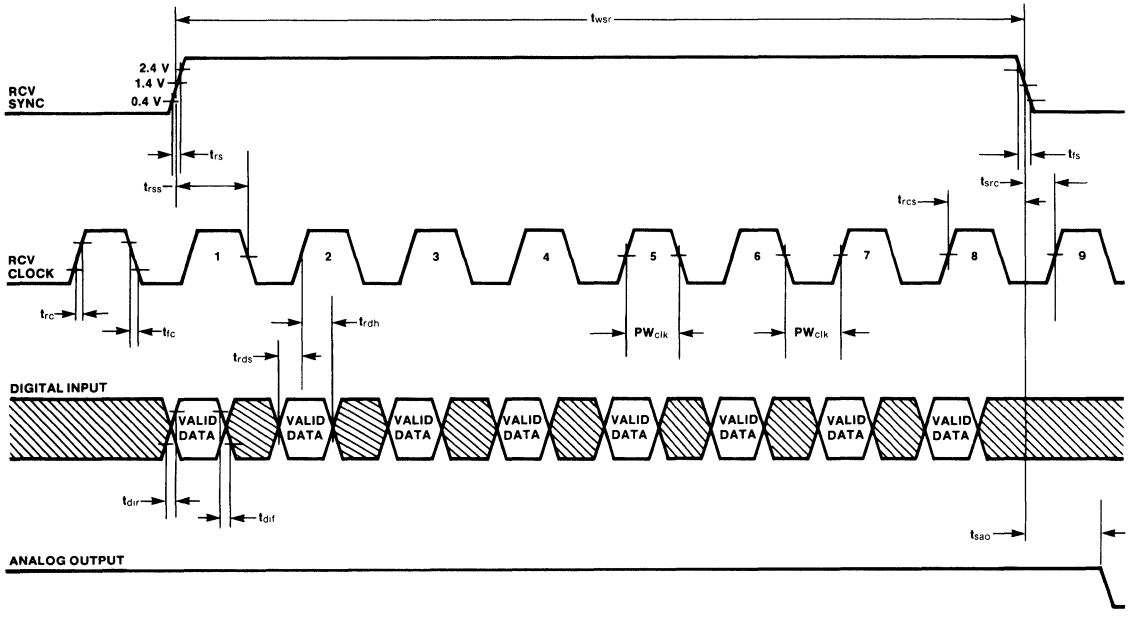


Fig. 2 Transmitter Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

Fig. 3 Receiver Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

Fig. 4 S/D Ratio vs Input Level

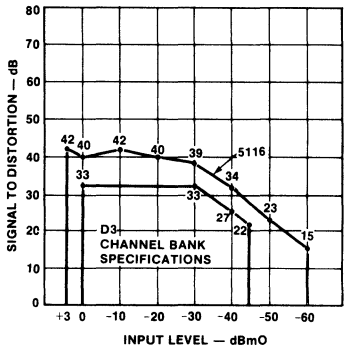


Fig. 5 Gain Tracking Performance

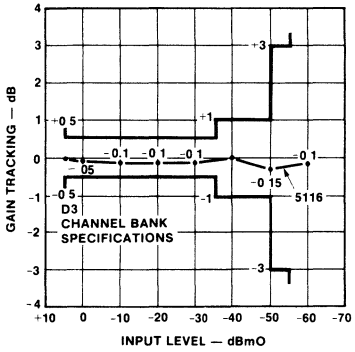


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Fig. 6 A/D, D/A Conversion Timing

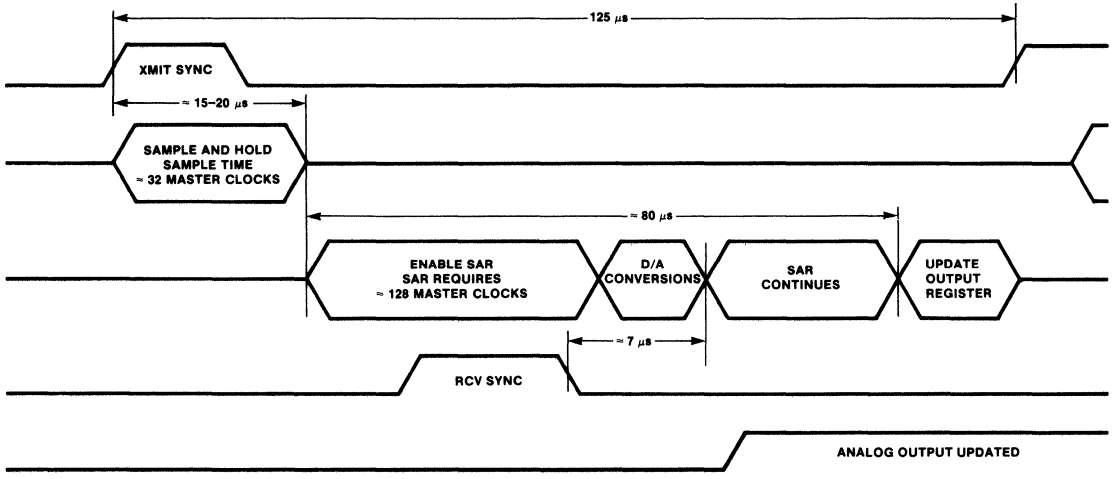
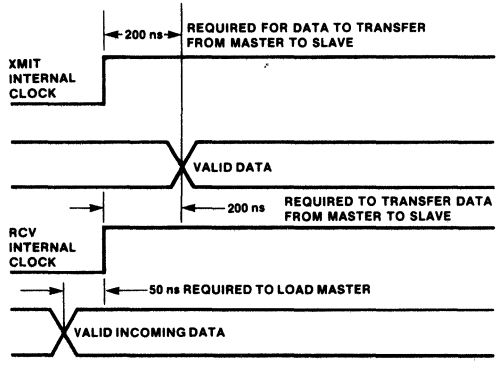


Fig. 7 Data Input/Output Timing



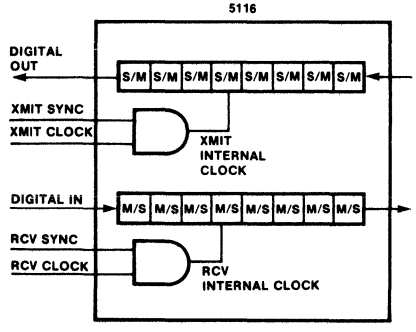


Fig. 8 A/D Converter (μ255-Law Encoder) Transfer Characteristic for 5116

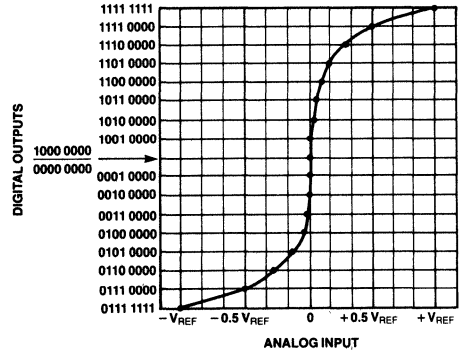


Fig. 9 D/A Converter (μ255-Law Decoder) Transfer Characteristic for 5116

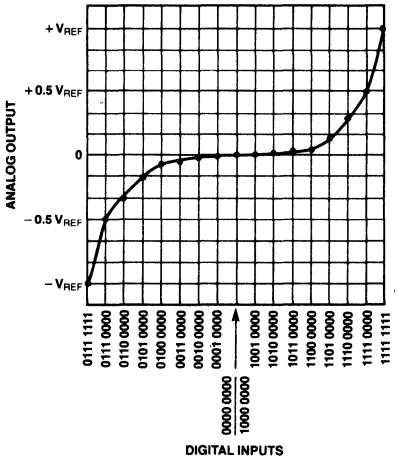
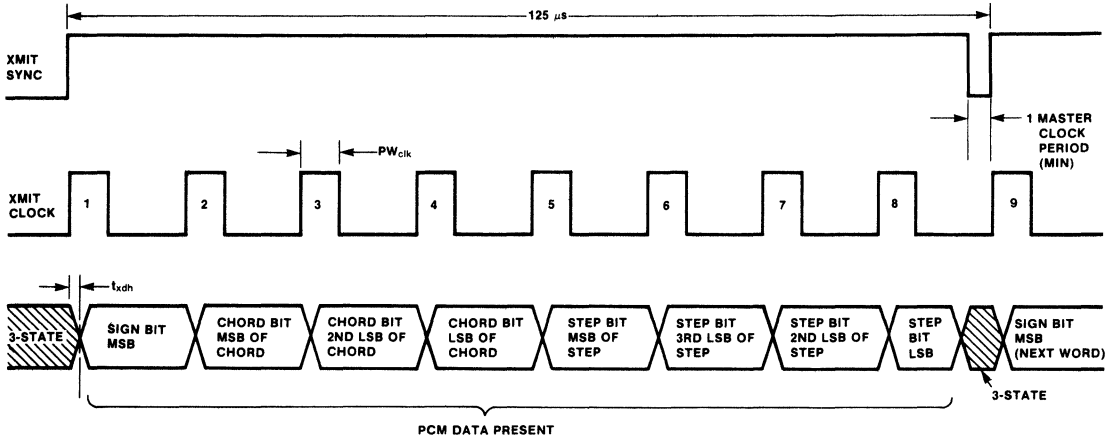


Fig. 10 64 kHz Operation, Transmitter Section Timing



Note

All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

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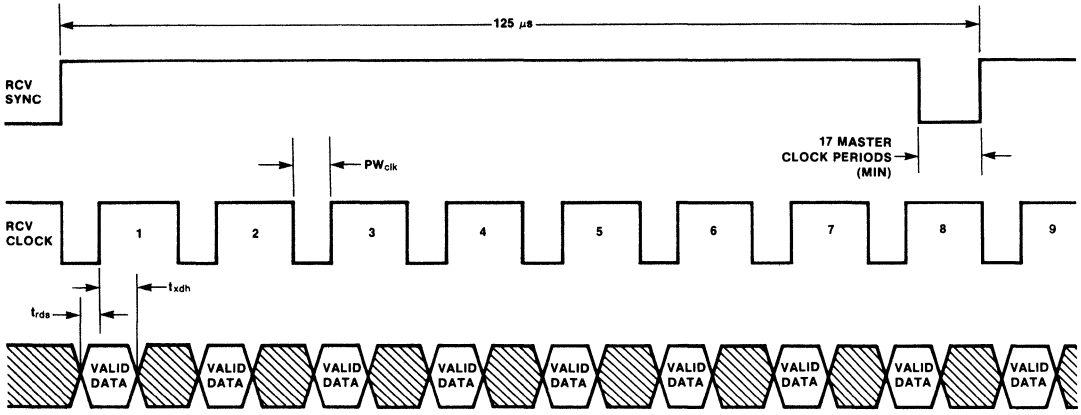
Fig. 11 64 kHz Operation, Receiver Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

Performance Evaluation

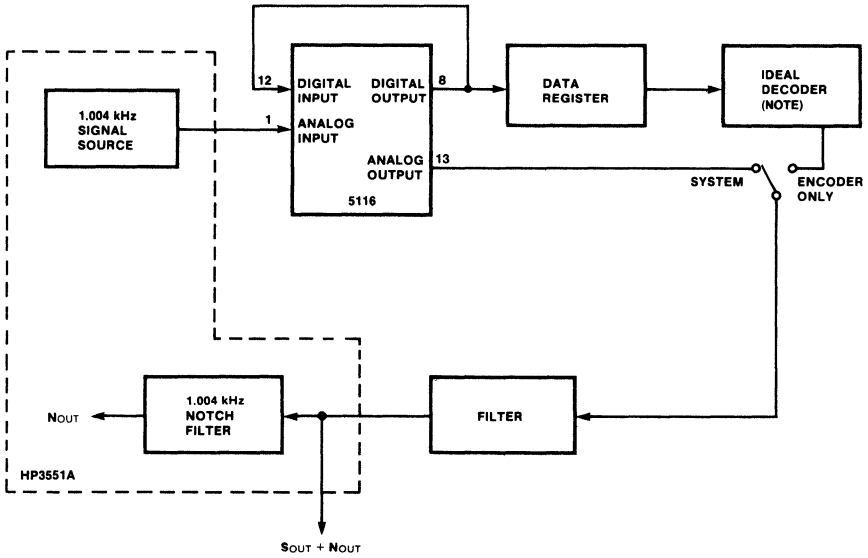
The equipment connections shown in *Figure 12* can be used to evaluate the performance of the 5116. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 1) of the 5116. The Digital Output of the codec is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the 5116 are connected as follows:

1. RCV SYNC is tied to XMIT SYNC.
2. XMIT Clock is tied to Master Clock. The signal is inverted and tied to RCV Clock.

The following timing signals are required:
1. Master Clock = 2.048 MHz
2. XMIT SYNC repetition rate = 8 kHz
3. XMIT SYNC width = 8 XMIT Clock periods

When all the above requirements are met, the set-up of *Figure 12* permits the measurement of synchronous system performance over a wide range of Analog Inputs. The data register and ideal decoder provide a means of checking the encoder portion of the 5116 independently of the decoder section. To test the system in the asynchronous mode, Master Clock should be separated from XMIT Clock, and Master Clock should be separated from RCV Clock. XMIT Clock and RCV Clock are separated also.

Fig. 12 System Characteristics Test Configuration



Note
The ideal decoder consists of a digital decompander and a 13-bit precision DAC

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FAIRCHILD
A Schlumberger Company

μA5151
μ255-Law Companding Codec

Telecommunications Products

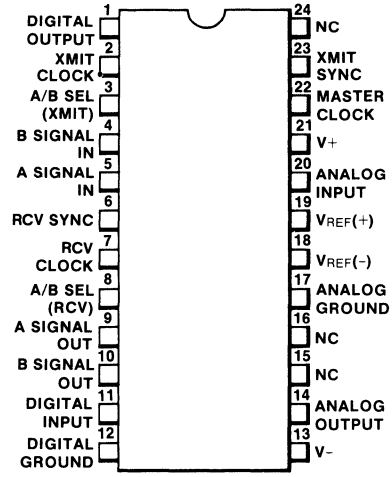
Description

The 5151 is a monolithic CMOS Companding Codec which contains two sections: (1) an analog-to-digital converter which has a transfer characteristic conforming to the standard μ255 companding Law, and (2) a digital-to-analog converter which also conforms to the μ255 companding Law.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in D3 Channel Bank and PBX systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64 kb/s to 2.1 Mb/s rate with analog signal sampling occurring at an 8 kHz rate. A SYNC pulse input is provided for synchronizing transmission and reception of multichannel information being multiplexed over a single transmission line.

- **EXCEEDS D3 CHANNEL BANK SPECIFICATIONS**
- **LOW POWER DISSIPATION 30 mW TYPICAL**
- **SYNCHRONOUS/ASYNCHRONOUS OPERATION**
- **ON-CHIP S/H CIRCUIT**
- **ON-CHIP OFFSET NULL CIRCUIT**
- **SEPARATE ANALOG AND DIGITAL GROUNDS**
- **64 kb/s TO 2.1 Mb/s SERIAL DATA RATE**
- **ZERO CODE SUPPRESSION**
- **±5 V POWER SUPPLY OPERATION**

Connection Diagram
24-Pin DIP

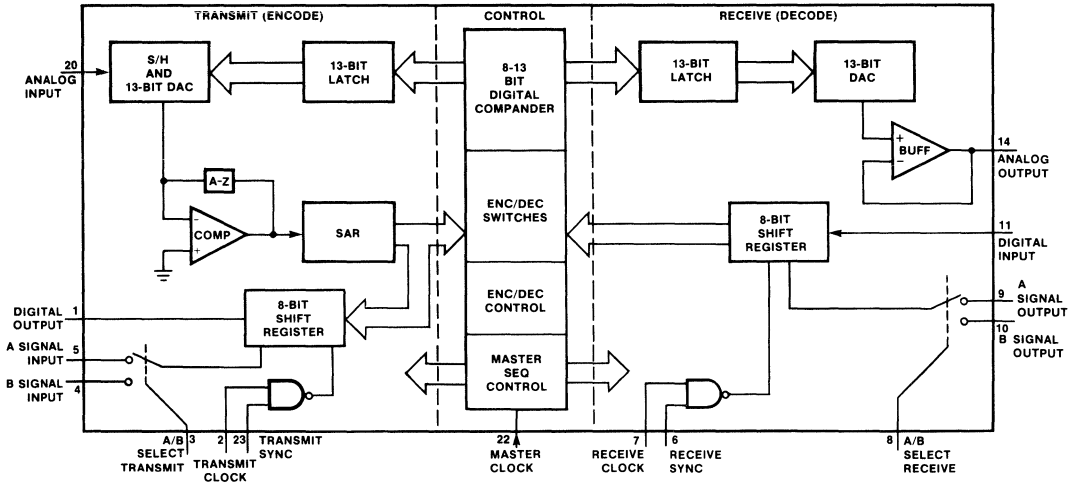


(Top View)

Order Information

Type	Package	Code	Part No.
μA5151	Ceramic DIP	7L	μA5151DC
μA5151	Ceramic DIP (Side Brazed)	7R	μA5151JC

Block Diagram



Pins 15, 16, and 24 = not connected.

Absolute Maximum Ratings (Note)

Supply Voltage (V+)	+6 V
Supply Voltage (V−)	−6 V
Analog Input Range	$V- \leq V_{IN} \leq V+$
Digital Input Range	$-0.5\ V \leq V_{IN} \leq V+$
Reference Voltage $V_{REF}(+)$	$-0.5\ V \leq V_{REF}(+) \leq V+$
Reference Voltage $V_{REF}(-)$	$V- \leq V_{REF}(-) \leq 0.5\ V$
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

Note
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

Functional Description (Refer to Block Diagram)

Positive and Negative Reference Voltages ($V_{REF}(+)$ and $V_{REF}(-)$ Pins 19 and 18)
These inputs provide the conversion references for the digital-to-analog converters in the 5151. $V_{REF}(+)$ and $V_{REF}(-)$ must maintain 100 ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

Analog Input, Pin 20
Voice-frequency analog signals which are bandwidth-limited to 4 kHz are input at this pin. Typically, they are then sampled at an 8 kHz rate (Refer to *Figure 6*). The analog input must remain between $V_{REF}(+)$ and $V_{REF}(-)$ for accurate conversion.

Master Clock, Pin 22
This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV Clock, XMIT SYNC or XMIT Clock and is not internally related to them.

XMIT SYNC, Pin 23 (Refer to *Figure 2* for the Timing Diagram)
This input is synchronized with XMIT Clock. When XMIT SYNC goes HIGH, the digital output is activated and the a/d conversion begins on the next positive edge of Master clock. The conversion by Master Clock can be asynchronous with XMIT Clock. The serial output data is clocked out by the positive edges of XMIT Clock. The negative edge of XMIT SYNC causes the digital output to become 3-state. XMIT SYNC must go LOW for at least 1 master clock prior to the transmission of the next digital word. (Refer to *Figure 10.)*

XMIT Clock, Pin 2 (Refer to *Figure 2* for the Timing Diagram)
The on-chip 8-bit output shift register of the 5151 is unloaded at the clock rate present on this pin. Clock rates of 64 kHz to 2.1 MHz can be used for XMIT Clock. The positive edge of the Internal Clock transfers the data from the master to the slave of a master-slave flip-flop (refer to *Figure 7*). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT Clock, XMIT SYNC will determine when the first positive edge of the Internal Clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV/SYNC, Pin 6 (Refer to *Figure 3* for the Timing Diagram)
This input is synchronized with RCV Clock, and serial data is clocked in by RCV Clock. Duration of the RCV SYNC pulse is approximately eight RCV Clock periods. The conversion from digital-to-analog starts after the negative edge of RCV SYNC pulse (refer to *Figure 6*). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay LOW for 17 Master clocks (minimum) before the next digital word is to be received.(refer to *Figure 11*)

RCV Clock, Pin 7 (Refer to *Figure 3* for Timing Diagram)
The on-chip 8-bit shift register for the 5151 is loaded at the clock rate present on this pin. Clock rates of 64 kHz to 2.1 MHz can be used for RCV Clock. Valid data should be applied to the Digital Input before the positive edge of the internal clock (refer to *Figure 7*). This set-up time, t_{rds}, allows the data to be transferred into the master of a master-slave flip-flop. The positive edge of the Internal Clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{rdh}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV Clock, RCV SYNC will determine when the first positive edge of Internal Clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

Digital Output, Pin 1
The 5151 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT Clock. When XMIT SYNC is LOW, the Digital Output is an open circuit. When XMIT SYNC is HIGH, the state of the Digital Output is determined by the value of the output bit in the serial shift register. The output is composed of a sign bit, 3 chord bits, and 4 step bits. The sign bit indicates the polarity of the Analog

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Input while the chord and step bits indicate the magnitude. In the first chord, the step bit has a value of 0.6 mV. In the second chord, the step bit has a value of 1.2 mV. This doubling of the step value continues for each of the six successive chords.

Each chord has a specific value and the step bits, 16 in each chord, specify the displacement from that value (refer to *Table 1).* Thus the output, which follows the μ255-Law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit a/d converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the a/d converter (μ-Law Encoder) is shown in *Figure 8.*

Digital Input, Pin 11
The 5151 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV Clock. The timing diagram is shown in *Figure 3.* When RCV SYNC goes HIGH, the 5151 uses RCV Clock to clock the serial data into its input register. RCV SYNC goes LOW to indicate the end of serial input data. The eight bits of the input data have the same functions described for the Serial Output. The transfer characteristic of the d/a converter (μ-Law Decoder) is shown in *Figure 9.*

Analog Output, Pin 14
The Analog Output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with (sin x)/x correction to recreate the sampled voice signal. When the 8th bit of the word is a signalling bit, it is assigned a value of 1/2 step. This results in a lower system quantization error rate than would result if the bit were arbitrarily set to 0 (no step) or 1 (full step).

Operation of Codec With 64 kHz XMIT/RCV Clock Frequencies
XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (minimum) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 master clock periods (minimum) before the next digital word is received (refer to *Figures 10 and 11).*

A/B Signal In, Pins 4 and 5
These two pins allow insertion of signalling information into the transmitted data stream. The inserted information occurs as the 8th bit (LSB) in the transmitted word. A positive transition occurring on A/B SEL (XMIT) selects A Signal In while a negative transition selects B Signal In.

A/B Signal Out, Pins 9 and 10
These two pins are provided to output received signalling information. A positive transition on A/B SEL (RCV) routes the signal bit to A Signal Out while a negative transition routes the signal bit (bit 8) to B Signal Out. Refer to *Figure 12.*

A/B SEL (RCV), Pin 8
This input routes the signalling bit, bit 8, either to A Signal Out or to B Signal Out as described in the A/B Signal Out paragraph above, and should be changed only at the start of the 6th and 12th frames as shown in *Figure 13.*

A/B SEL (XMIT), Pin 3
This input selects either A Signal In or B Signal In as described in the A/B Signal In paragraph above, and should be changed only at the start of the 6th and 12th frames as shown *Figure 13.*

Offset Null
The offset null feature of the 5151 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate a/d conversion for inputs near ground. There is no offset adjust of the output amplifier. Since the output is intended to be ac-coupled to the external filter, the resultant dc error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the Analog Input. Therefore, for an Analog Input of 0 V, the sign bit will be stable.

Table 1 Digital Output Code: μ-Law

Chord Code	Chord Value	Step Value
1. 111	0.0 mV	0.613 mV
2. 110	10.11 mV	1.226 mV
3. 101	30.3 mV	2.45 mV
4. 100	70.8 mV	4.90 mV
5. 011	151.7 mV	9.81 mV
6. 010	313 mV	19.61 mV
7. 001	637 mV	39.2 mV
8. 000	1.284 V	78.4 mV

Example:
1 100 1101 = +70.8 mV + (2 x 4.90 mV)
Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

Electrical Operating Characteristics

Power Supply Requirements

Symbol	Characteristic	Min	Typ	Max	Unit
V+	Positive Supply Voltage	4.75	5.0	5.25	V
V−	Negative Supply Voltage	−5.25	−5.0	−4.75	V
$V_{REF}(+)$	Positive Reference Voltage (Note 1)	2.375	2.5	2.625	V
$V_{REF}(-)$	Negative Reference Voltage (Note 1)	−2.625	−2.5	−2.375	V

DC Characteristics V+ = 5.0 V, V− = −5.0 V, $V_{REF}(+)$ = 2.5 V, V_{REF} (−) = −2.5 V.

Symbol	Characteristic	Min	Typ	Max	Unit
R_{INAS}	Analog Input Resistance During Sampling (Note 2)		2		kΩ
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ
C_{INA}	Analog Input Capacitance		150	250	pF
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	±8	mV
R_{OUTA}	Analog Output Resistance		20	50	Ω
I_{OUTA}	Analog Output Current	0.25	0.5		mA
$V_{OFFSET/O}$	Analog Output Offset Voltage		±200	±850	mV
I_{IL}	Logic Input LOW Current (V_{IN} = 0.8 V) Digital Input, Clock Input, SYNC Input (Note 3)		±0.1	±10	μA
I_{IH}	Logic Input HIGH Current (V_{IN} = 2.4 V) Digital Input, Clock Input, SYNC Input (Note 3)		−0.25	−0.8	mA
C_{DO}	Digital Output Capacitance		8	12	pF
I_{DOL}	Digital Output Leakage Current		±0.1	±10	μA
V_{OL}	Digital Output LOW Voltage (Note 4)			0.4	V
V_{OH}	Digital Output HIGH Voltage (Note 4)	3.9			V
I+	Positive Supply Current		4	10	mA
I−	Negative Supply Current		2	6	mA
I_{REF+}	Positive Reference Current		4	20	μA
I_{REF-}	Negative Reference Current		4	20	μA

AC Characteristics Refer to *Figures 2* and *3.*

Symbol	Characteristic	Min	Typ	Max	Unit
f_m	Master Clock Frequency	1.5	1.544	2.1	MHz
f_r, f_x	RCV, XMIT Clock Frequency	0.064	1.544	2.1	MHz
PW_{clk}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns
t_{rc}, t_{fc}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{clk}	ns
t_{rs}, t_{fs}	SYNC Rise, Fall Time (XMIT, RCV)			25% of PW_{clk}	ns
t_{dir}, t_{dif}	Digital Input Rise, Fall Time			25% of PW_{clk}	ns
t_{wsx}, t_{wsr}	SYNC Pulse Width (XMIT RCV)		$\frac{8}{f_x(f_r)}$		μs
t_{ps}	SYNC Pulse Period (XMIT,RCV)		125		μs
t_{xcs}	XMIT Clock-to-XMIT SYNC Delay (Note 5)	50% of $t_{fc}(t_{rs})$			ns
t_{xcsn}	XMIT Clock-to-XMIT SYNC (Negative Edge) Delay	200			ns
t_{xss}	XMIT SYNC Set-Up Time	200			ns
t_{xdd}	XMIT Data Delay (Note 4)	0		200	ns
t_{xdp}	XMIT DATA Present (Note 4)	0		200	ns
t_{xdt}	XMIT Data Three State (Note 4)			150	ns
t_{dof}	Digital Output Fall Time (Note 4)		50		ns
t_{dor}	Digital Output Rise Time (Note 4)		50		ns
t_{src}	RCV SYNC-to-RCV Clock Delay (Note 5)	50% of $t_{rc}(t_{fs})$			ns
t_{rds}	RCV Data Set-Up Time (Note 6)	50			ns
t_{rdh}	RCV Data Hold Time (Note 6)	200			ns
t_{rcs}	RCV Clock-to-RCV SYNC Delay	200			ns
t_{rss}	RCV SYNC Set-Up Time (Note 6)	200			ns
t_{sao}	RCV SYNC-to-Analog Output Delay		7		μs
$t_{A/BI}$	A/B Signalling Input Set-Up Time			200	ns
$t_{A/B\ SH}$	A/B Select Hold Time	200			ns
$t_{A/BSS}$	A/B Select Setup Time	400			ns
$t_{A/BO}$	A/B Signalling Output Delay		200	300	ns
Slew+	Analog Output Positive Slew Rate		1		V/μs
Slew−	Analog Output Negative Slew Rate		1		V/μs
Droop	Analog Output Droop Rate		25		μV/μs

Notes

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging the internal capacitor to within 1/2 LSB (≤ 300 μV) in 20 μs. Therefore, the external source resistance must be 3 kΩ or less. The equivalent circuit during sampling is shown in *Figure 1.*
3. The 5156 will source current through an internal 6 kΩ resistor to help pull up the TTL output. When a transition from "1" to "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30 pF with $I_{OH} = -100$ μA, $I_{OL} = 500$ μA.
5. This delay is necessary to avoid overlapping Clock and SYNC.
6. The first bit of data is loaded when SYNC and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

System Characteristics Refer to *Figures 4* and *5*.

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
S/D	Signal-to-Distortion	35 29 24	39 34 29		dB dB dB	Analog Input = 0 to −30 dBmO Analog Input = −40 dBmO Analog Input = −45 dBmO
GT	Gain Tracking		±0.1 ±0.1 ±0.2	±0.4 ±0.8 ±2.5	dB dB dB	Analog Input = +3 to −37 dBmO Analog Input = −37 to −50 dBmO Analog Input = −50 to −55 dBmO
N_{IC}	Idle Channel Noise		10	18	dBrnC0	Analog Input = 0 V
TLP	Transmission Level Point		+4		dB	600 Ω

Fig. 1 Equivalent Circuit During Sampling

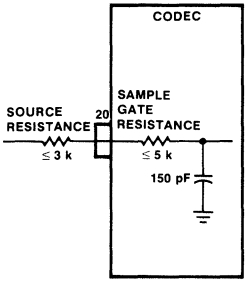
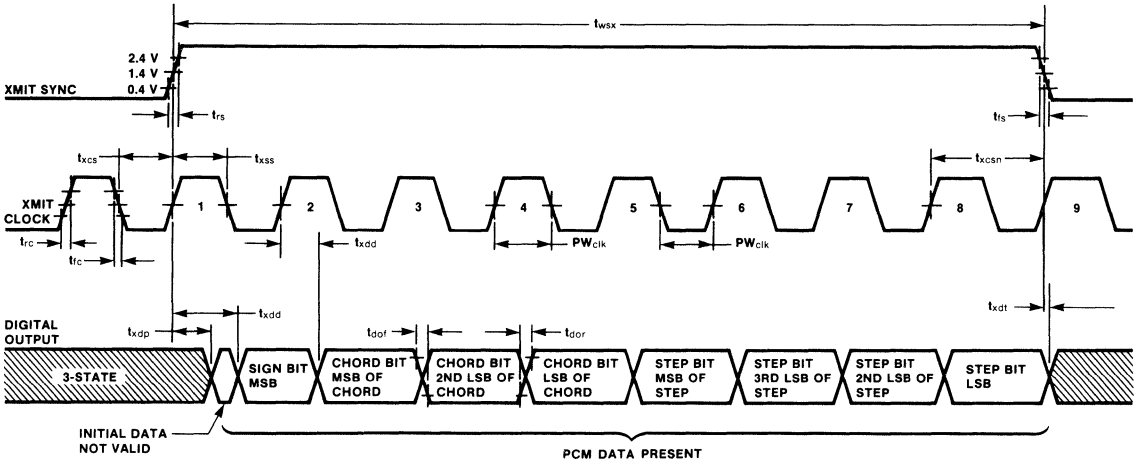


Fig. 2 Transmitter Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

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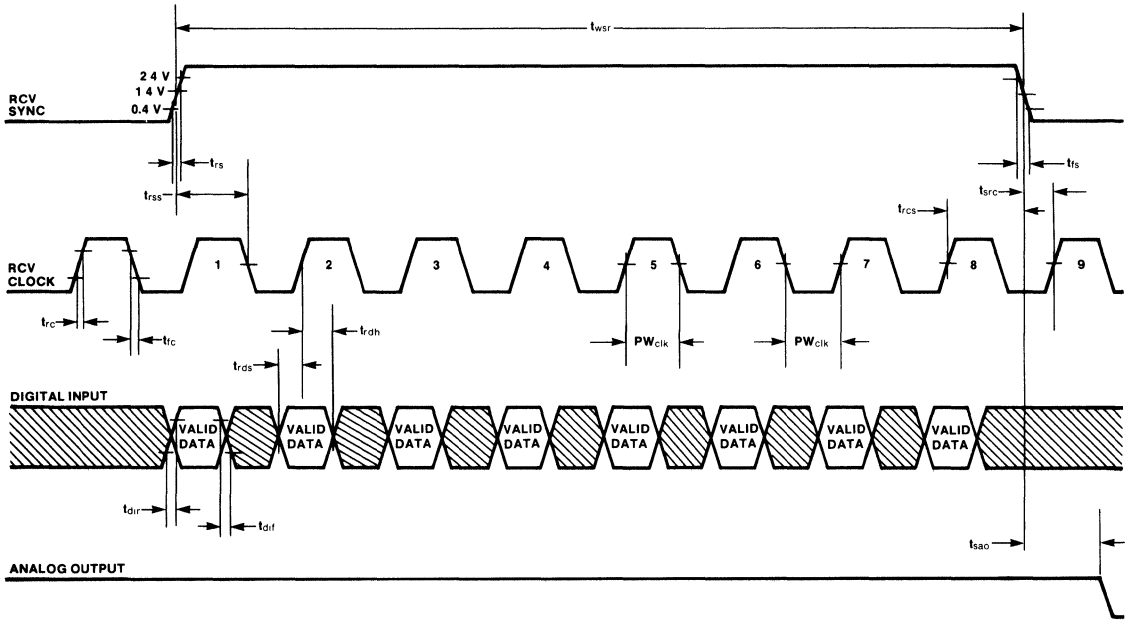
Fig. 3 Receiver Section Timing



Note

All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V

Fig. 4 S/D Ratio vs Input Level

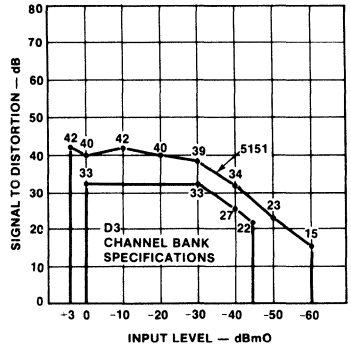


Fig. 5 Gain Tracking Performance

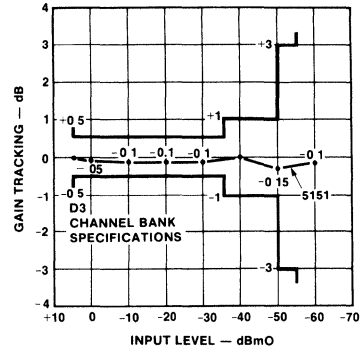


Fig. 6 A/D, D/A Conversion Timing

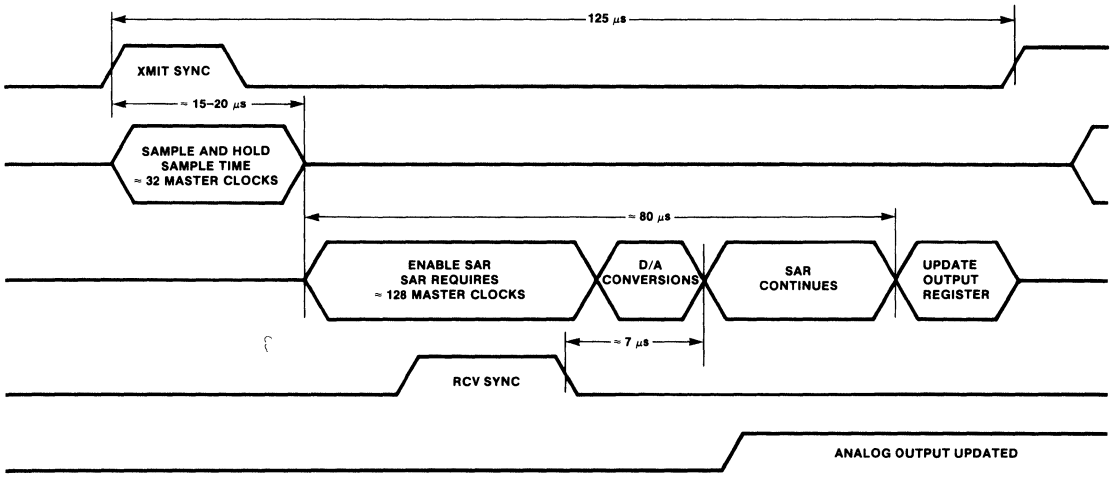
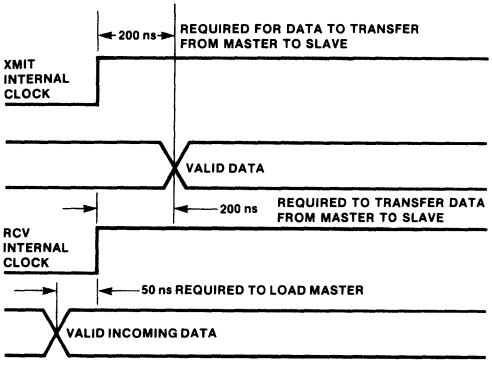


Fig. 7 Data Input/Output Timing



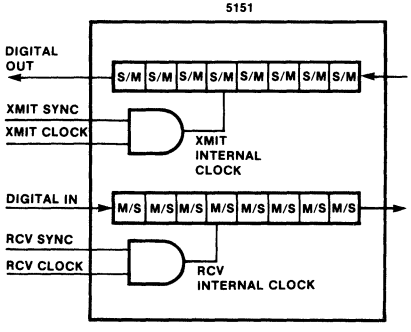
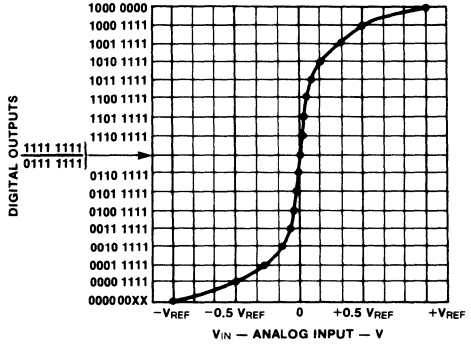


Fig. 8 A/D Converter (μ-Law Encoder) Transfer Characteristic



Signalling = 1.XX = 01
Signalling = 0.XX = 10
No Signalling, XX = 10

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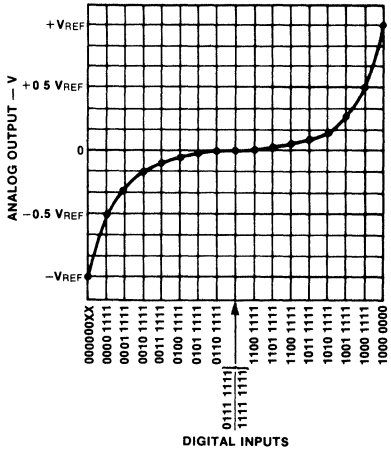
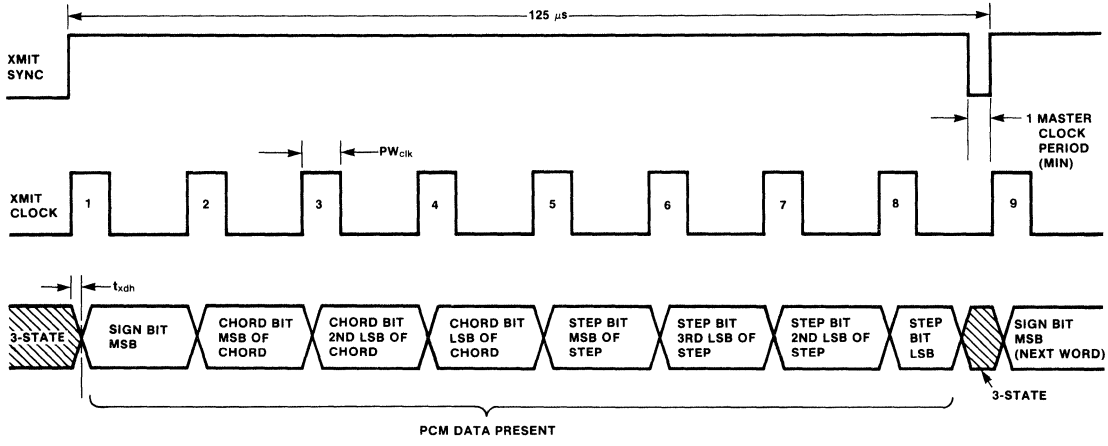
Fig. 9 D/A Converter (μ-Law Decoder) Transfer Characteristic



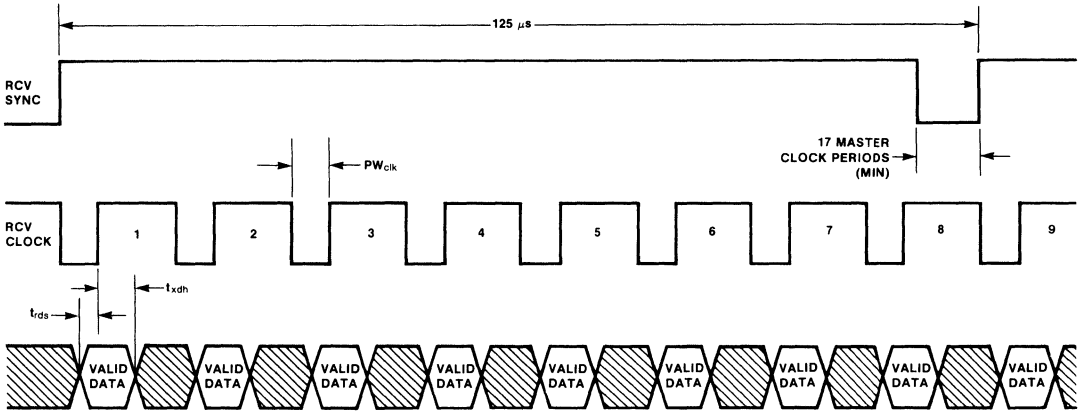
Signalling = 1.XX = 01
Signalling = 0.XX = 10
No Signalling = XX = 10

Fig. 10 64 kHz Operation, Transmitter Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V All delay times are measured from 1.4 V.

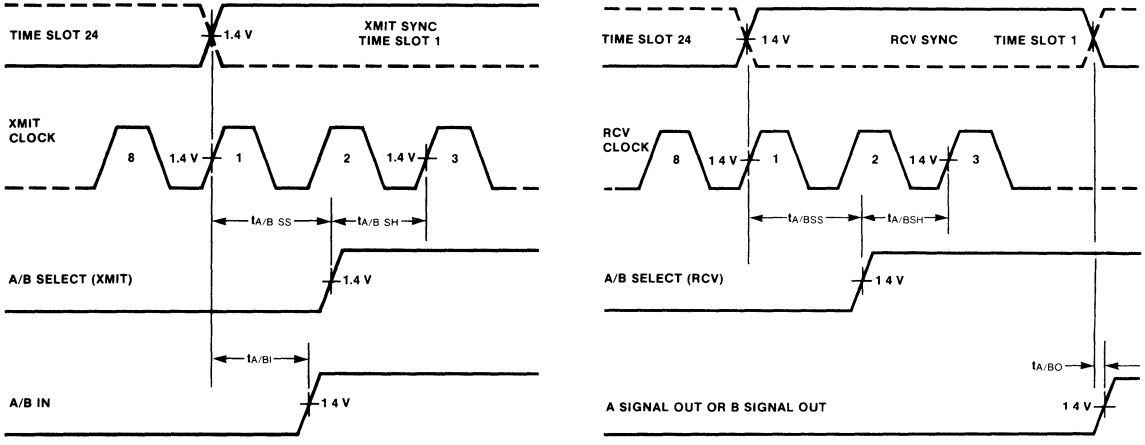
Fig. 11 64 kHz Operation, Receiver Section Timing



Note

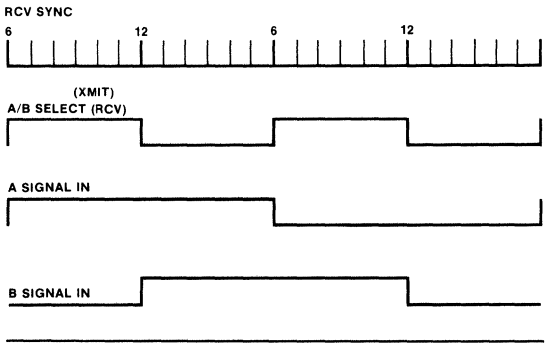
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

Fig. 12 A/B Select Timing



8

Fig. 13 Signalling Timing Requirements for Performance Evaluation



Performance Evaluation

The equipment connections shown in *Figure 14* can be used to evaluate the performance of the 5151. An Analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 20) of the 5151. The Digital Output of the codec is tied back to the Digital Input, and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the 5151 are connected as follows:

1. A/B SEL (RCV) is tied to A/B SEL (XMIT).
2. RCV SYNC is tied to XMIT SYNC.
3. XMIT Clock is tied to Master Clock. The signal is inverted and tied to RCV Clock.

The following timing signals are required:

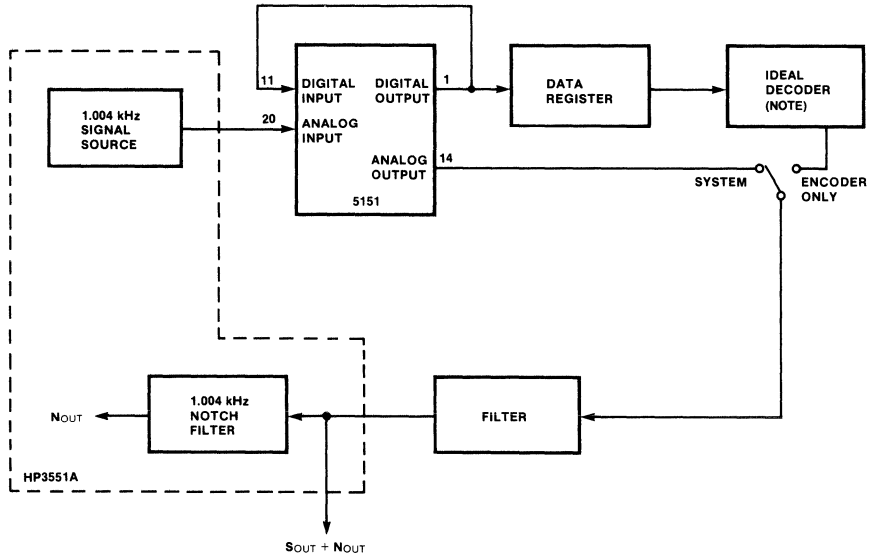
1. Master Clock = 1.544 MHz
2. XMIT SYNC repetition rate = 8 kHz
3. XMIT SYNC width = 8 Master Clock periods

Additional timing signals are shown in *Figure 13.*

When all the above requirements are met, the set-up of *Figure 14* permits the measurement of synchronous system performance over a wide range of Analog Inputs. The data register and ideal decoder provide a means of checking the encoder portion of the 5151 independently of the decoder section. To test the system in the asynchronous mode, Master Clock should be separated from XMIT Clock and from RCV Clock; XMIT Clock and RCV Clock are separated also.

Some experimental results obtained with the 5151 are shown in *Figures 4* and *5.* In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The 5151 exceeds the requirements for Signal-to-Distortion ratio *(Figure 4)* and for Gain Tracking *(Figure 5).*

Fig. 14 System Characteristics Test Configuration



Note

The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

FAIRCHILD
A Schlumberger Company

μA5156
A-Law Companding Codec

Telecommunication Products

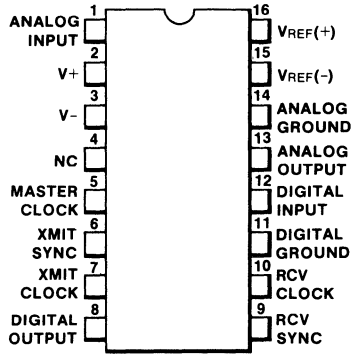
Description

The 5156 is a monolithic CMOS Companding Codec which contains two sections: (1) an analog-to-digital converter which has a transfer characteristic conforming to the standard A-Law companding code, and (2) a digital-to-analog converter which also conforms to the A-Law code.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in PCM systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64 kb/s to 2.1 Mb/s rate with analog signal sampling occurring at an 8 kHz rate. A SYNC pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

- **EXCEEDS CCITT SPECIFICATIONS**
- **EVEN-ORDER BIT INVERSION DATA FORMAT**
- **LOW POWER DISSIPATION 30 mW TYPICAL**
- **SYNCHRONOUS/ASYNCHRONOUS OPERATION**
- **ON-CHIP S/H CIRCUIT**
- **ON-CHIP OFFSET NULL CIRCUIT**
- **SEPARATE ANALOG AND DIGITAL GROUNDS**
- **64 kb/s TO 2.1 Mb/s SERIAL DATA RATE**
- **±5 V POWER SUPPLY OPERATION**

Connection Diagram
16-Pin DIP



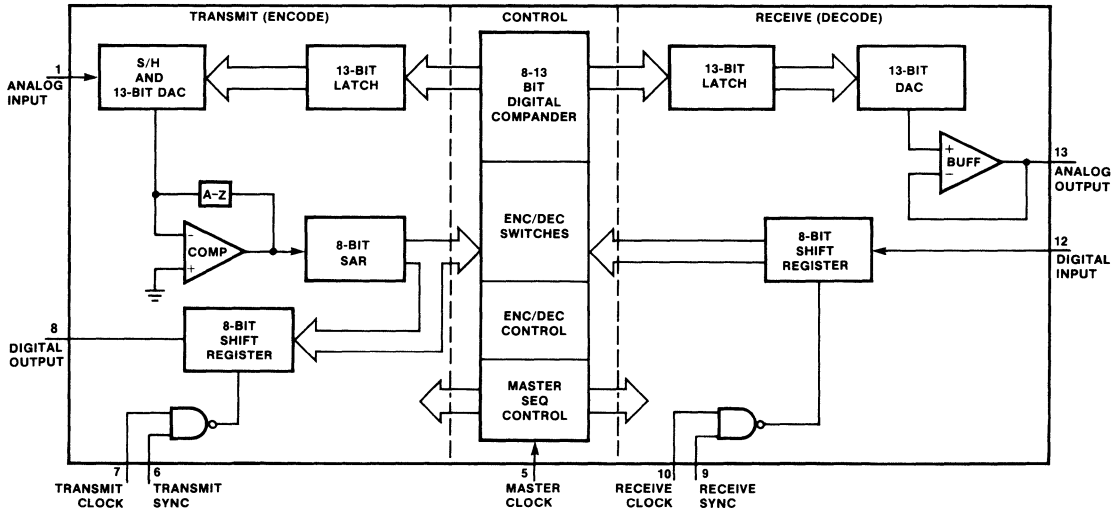
(Top View)

Order Information

Type	Package	Code	Part No.
μA5156	Ceramic DIP	FW	μA5156 DC
μA5156	Ceramic DIP (Side Brazed)	FB	μA5156 JC

8

Block Diagram



Pin 4 = not connected

Absolute Maximum Ratings (Note)

Supply Voltage (V+)	+6 V
Supply Voltage (V−)	−6 V
Analog Input Range	$V- \leq V_{IN} \leq V+$
Digital Input Range	$-0.5\ V \leq V_{IN} \leq V+$
Reference Voltage $V_{REF}(+)$	$-0.5\ V \leq V_{REF}(+) \leq V+$
Reference Voltage $V_{REF}(-)$	$V- \leq V_{REF}(-) \leq 0.5\ V$
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

Note
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

Functional Description (Refer to Block Diagram)

Positive and Negative Reference Voltages
($V_{REF}(+)$ and $V_{REF}(-)$ Pins 16 and 15)
These inputs provide the conversion references for the digital-to-analog converters in the 5156. $V_{REF}(+)$ and $V_{REF}(-)$ must maintain 100 ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

Analog Input, Pin 1
Voice-frequency analog signals which are bandwidth-limited to 4 kHz are input at this pin. Typically, they are then sampled at an 8 kHz rate (Refer to *Figure 6)*. The analog input must remain between $V_{REF}(+)$ and $V_{REF}(-)$ for accurate conversion.

Master Clock, Pin 5
This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV Clock, XMIT SYNC or XMIT Clock and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to *Figure 2* for the Timing Diagram)
This input is synchronized with XMIT Clock. When XMIT SYNC goes HIGH, the digital output is activated and the A/D conversion begins on the next positive edge of Master Clock. The conversion by Master Clock can be asynchronous with XMIT Clock. The serial output data is clocked out by the positive edges of XMIT Clock. The negative edge of XMIT SYNC causes the digital output to become 3-state. XMIT SYNC must go LOW for at least 1 master clock prior to the transmission of the next digital word. (Refer to *Figure 10.*)

XMIT Clock, Pin 7 (Refer to *Figure 2* for the Timing Diagram)
The on-chip 8-bit output shift register of the 5156 is unloaded at the clock rate present on this pin. Clock rates of 64 kHz to 2.1 MHz can be used for XMIT Clock. The positive edge of the Internal Clock transfers the data from the master to the slave of a master-slave flip-flop (refer to *Figure 7*). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT Clock, XMIT SYNC will determine when the first positive edge of the Internal Clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV SYNC, Pin 9 (Refer to *Figure 3* for the Timing Diagram)
This input is synchronized with RCV Clock, and serial data is clocked in by RCV Clock. Duration of the RCV SYNC pulse is approximately eight RCV Clock periods. The conversion from digital-to-analog starts after the negative edge of RCV SYNC pulse (refer to *Figure 6*). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay LOW for 17 Master Clocks (minimum) before the next digital word is to be received. (refer to *Figure 11*).

RCV Clock, Pin 10 (Refer to *Figure 3* for Timing Diagram)
The on-chip 8-bit shift register for the 5156 is loaded at the clock rate present on this pin. Clock rates of 64 kHz to 2.1 MHz can be used for RCV Clock. Valid data should be applied to the digital input before the positive edge of the internal clock (refer to *Figure 7*). This set-up time, t_{rds}, allows the data to be transferred into the master of a master-slave flip-flop. The positive edge of the Internal Clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{rdh}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV Clock, RCV SYNC will determine when the first positive edge of Internal Clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

Digital Output, Pin 8
The 5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT Clock. When XMIT SYNC is LOW, the Digital Output is an open circuit. When XMIT SYNC is HIGH, the state of the Digital Output is determined by the value of the output bit in the serial shift register. The output is composed of a sign bit, 3 chord bits, and 4 step bits. The sign bit indicates the polarity of the Analog Input

while the chord and step bits indicate the magnitude. In the first two chords, the step bit has a value of 1.2 mV. In the third chord, the step bit has a value of 2.4 mV. This doubling of the step value continues for each of the five successive chords.

Each chord has a specific value and the step bits, 16 in each chord, specify the displacement from that value (refer to *Table 1*). Thus the output, which follows the A-Law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit a/d converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the a/d converter (A-Law Encoder) is shown in *Figure 8*.

Digital Input, Pin 12
The 5156 input register accepts the 8-bit encoded analog value and loads it under control of RCV SYNC and RCV Clock. The timing diagram is shown in *Figure 3*. When RCV SYNC goes HIGH, the 5156 uses RCV Clock to clock the serial data into its input register. RCV SYNC goes LOW to indicate the end of serial input data. The eight bits of the input data have the same functions described for the Digital Output. The transfer characteristic of the d/a converter (A-Law Decoder) is shown in *Figure 9*.

Analog Output, Pin 13
The Analog Output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with (sin x)/x correction to recreate the sampled voice signal.

Operation of Codec With 64 kHz XMIT/RCV Clock Frequencies
XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (minimum) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 master clock periods (minimum) before the next digital word is received (refer to *Figures 10* and *11*).

Offset Null
The offset null feature of the 5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate a/d conversion for inputs near ground. There is no offset adjust of the output amplifier. Since the output is intended to be ac-coupled to the external filter, the resultant dc error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the Analog Input. Therefore, for an Analog Input of 0 V, the sign bit will be stable.

Table 1 Digital Output Code: A-Law

	Chord Code	Chord Value	Step Value
1.	101	0.0 mV	1.221 mV
2.	100	20.1 mV	1.221 mV
3.	111	40.3 mV	2.44 mV
4.	110	80.6 mV	4.88 mV
5.	001	161.1 mV	9.77 mV
6.	000	332 mV	19.53 mV
7.	011	645 mV	39.1 mV
8.	010	1.289 V	78.1 mV

Example:
1 110 0111 = +80.6 mV + (2 x 4.88 mV)
Sign Bit Chord Step Bits

If the sign bit were zero, then both plus signs would be changed to minus signs.

8

Electrical Operating Characteristics

Power Supply Requirements

Symbol	Characteristic	Min	Typ	Max	Unit
V+	Positive Supply Voltage	4.75	5.0	5.25	V
V−	Negative Supply Voltage	−5.25	−5.0	−4.75	V
$V_{REF}(+)$	Positive Reference Voltage (Note 1)	2.375	2.5	2.625	V
$V_{REF}(-)$	Negative Reference Voltage (Note 1)	−2.625	−2.5	−2.375	V

DC Characteristics V+ = 5.0 V, V− = −5.0 V, $V_{REF}(+)$ = 2.5 V, $V_{REF}(-)$ = −2.5 V.

Symbol	Characteristic	Min	Typ	Max	Unit
R_{INAS}	Analog Input Resistance During Sampling (Note 2)		2		kΩ
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ
C_{INA}	Analog Input Capacitance		150	250	pF
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	±8	mV
R_{OUTA}	Analog Output Resistance		20	50	Ω
I_{OUTA}	Analog Output Current	0.25	0.5		mA
$V_{OFFSET/O}$	Analog Output Offset Voltage		±200	±850	mV
I_{IL}	Logic Input LOW Current (V_{IN} = 0.8 V) Digital Input, Clock Input, SYNC Input (Note 3)		±0.1	±10	μA
I_{IH}	Logic Input HIGH Current (V_{IN} = 2.4 V) Digital Input, Clock Input, SYNC Input (Note 3)		−0.25	−0.8	mA
C_{DO}	Digital Output Capacitance		8	12	pF
I_{DOL}	Digital Output Leakage Current		±0.1	±10	μA
V_{OL}	Digital Output LOW Voltage (Note 4)			0.4	V
V_{OH}	Digital Output HIGH Voltage (Note 4)	3.9			V
I+	Positive Supply Current		4	10	mA
I−	Negative Supply Current		2	6	mA
I_{REF+}	Positive Reference Current		4	20	μA
I_{REF-}	Negative Reference Current		4	20	μA

AC Characteristics Refer to *Figures 2* and *3.*

Symbol	Characteristic	Min	Typ	Max	Unit
f_m	Master Clock Frequency	1.5	2.048	2.1	MHz
f_r, f_x	RCV, XMIT Clock Frequency	0.064	2.048	2.1	MHz
PW_{clk}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns
t_{rc}, t_{fc}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{clk}	ns
t_{rs}, t_{fs}	SYNC Rise, Fall Time (XMIT, RCV)			25% of PW_{clk}	ns
t_{dlr}, t_{dlf}	Data Input Rise, Fall Time			25% of PW_{clk}	ns
t_{wsx}, t_{wsr}	SYNC Pulse Width (XMIT RCV)		$\frac{8}{f_x(f_r)}$		μs
t_{ps}	SYNC Pulse Period (XMIT RCV)		125		μs
t_{xcs}	XMIT Clock-to-XMIT SYNC Delay (Note 5)	50% of $t_{fc}(t_{rs})$			ns
t_{xcsn}	XMIT Clock-to-XMIT SYNC (Negative Edge) Delay	200			ns
t_{xss}	XMIT SYNC Set-Up Time	200			ns
t_{xdd}	XMIT Data Delay (Note 4)	0		200	ns
t_{xdp}	XMIT Data Present (Note 4)	0		200	ns
t_{xdt}	XMIT Data Three State (Note 4)			150	ns
t_{dof}	Digital Output Fall Time (Note 4)		50		ns
t_{dor}	Digital Output Rise Time (Note 4)		50		ns
t_{src}	RCV SYNC-to-RCV Clock Delay (Note 5)	50% $t_{rc}(t_{fs})$			ns
t_{rds}	RCV Data Set-Up Time (Note 6)	50			ns
t_{rdh}	RCV Data Hold Time (Note 6)	200			ns
t_{rcs}	RCV Clock-to-RCV SYNC Delay	200			ns
t_{rss}	RCV SYNC Set-Up Time (Note 6)	200			ns
t_{sao}	RCV SYNC-to-Analog Output Delay		7		μs
Slew+	Analog Output Positive Slew Rate		1		V/μs
Slew−	Analog Output Negative Slew Rate		1		V/μs
Droop	Analog Output Droop Rate		25		μV/μs

Notes

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging the internal capacitor to within 1/2 LSB (≤ 300 μV) in 20 μs. Therefore, the external source resistance must be 3 kΩ or less. The equivalent circuit during sampling is shown in *Figure 1.*
3. The 5156 will source current through an internal 6 kΩ resistor to help pull up the TTL output. When a transition from "1" to "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30 pF with $I_{OH} = -100$ μA, $I_{OL} = 500$ μA.
5. This delay is necessary to avoid overlapping Clock and SYNC.
6. The first bit of data is loaded when SYNC and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

System Characteristics Refer to *Figures 4* and *5*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
S/D	Signal-to-Distortion	35 29 24	39 34 29		dB dB dB	Analog Input = 0 to −30 dBmO Analog Input = −40 dBmO Analog Input = −45 dBmO
GT	Gain Tracking		±0.1 ±0.1 ±0.2	±0.4 ±0.8 ±2.5	dB dB dB	Analog Input = +3 to −40 dBmO Analog Input = −40 to −50 dBmO Analog Input = −50 to −55 dBmO
N_{IC}	Idle Channel Noise		−80	−72	dBm0	Analog Input = 0 V
TLP	Transmission Level Point		+4		dBm	600 Ω

Fig. 1 Equivalent Circuit During Sampling

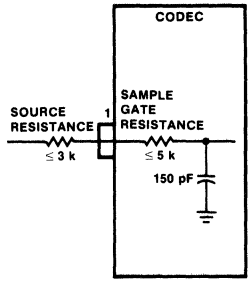
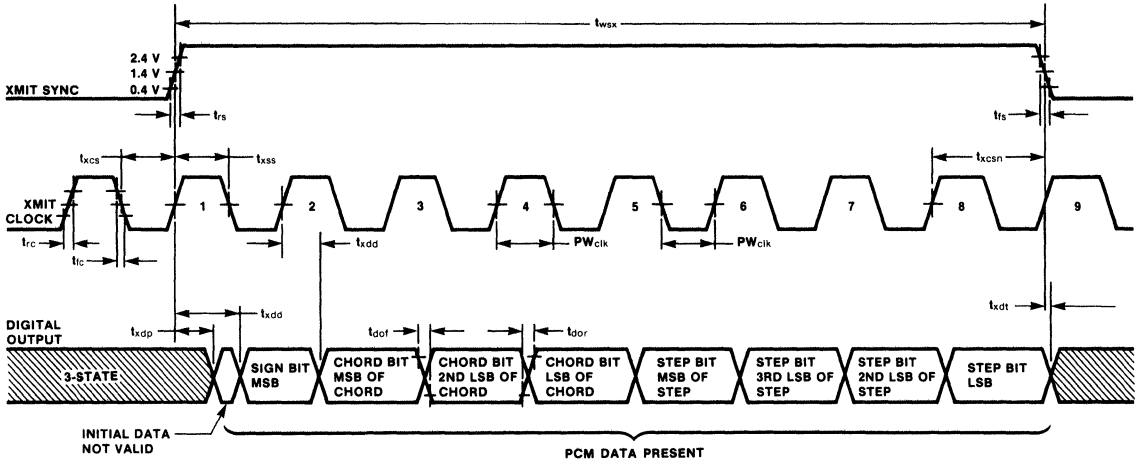
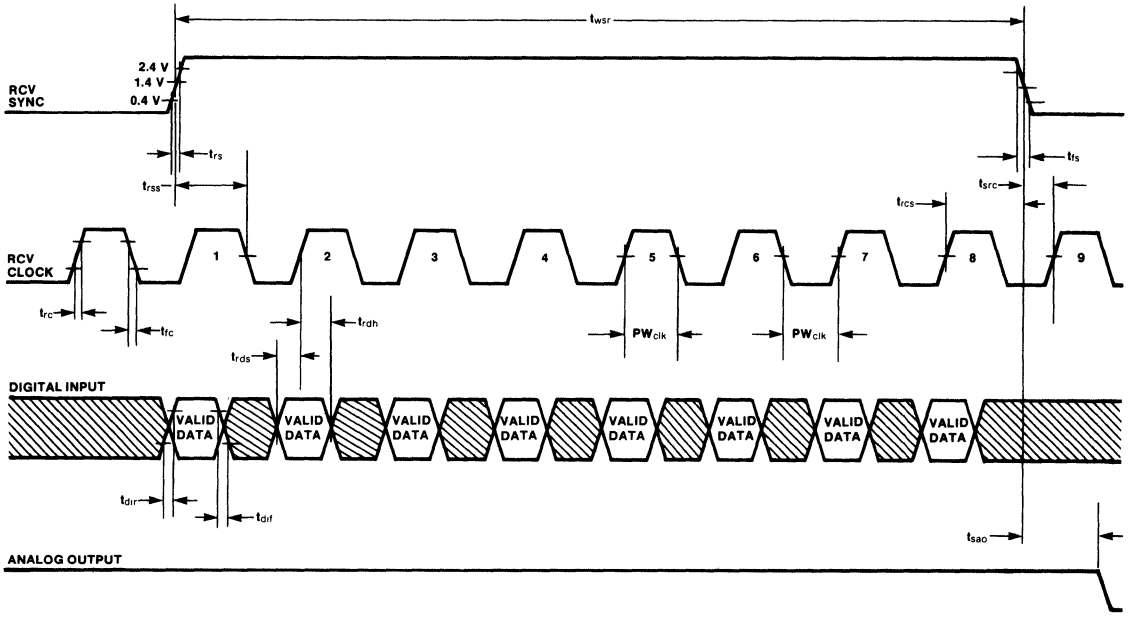


Fig. 2 Transmitter Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

Fig. 3 Receiver Section Timing



Note

All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1.4 V.

Fig. 4 S/D Ratio vs Input Level

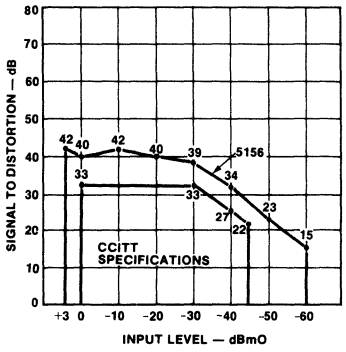


Fig. 5 Gain Tracking Performance

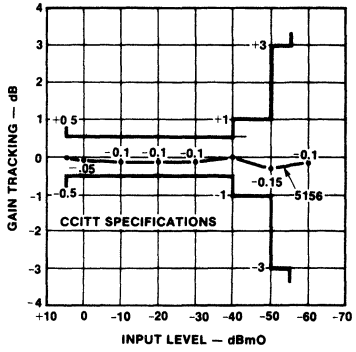


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Fig. 6 A/D, D/A Conversion Timing

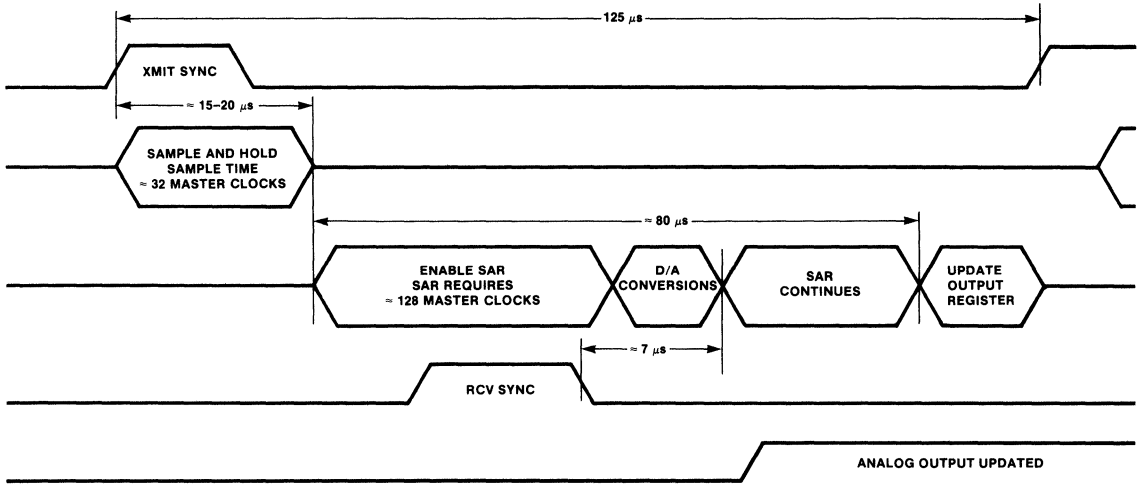
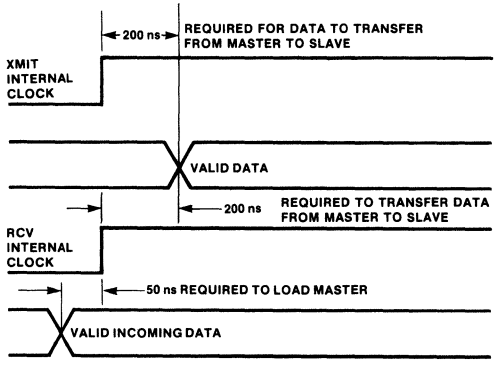


Fig. 7 Data Input/Output Timing



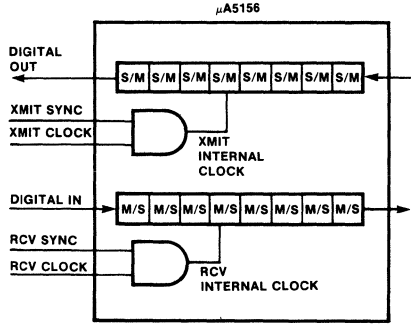


Fig. 8 A/D Converter (A-Law Encoder) Transfer Characteristic

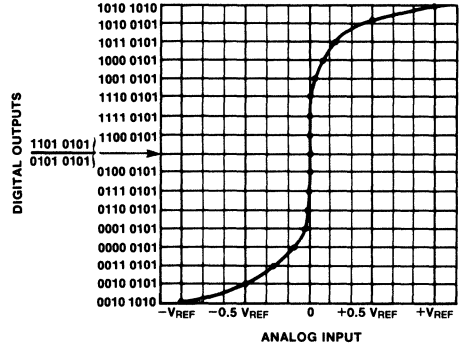


Fig. 9 D/A Converter (A-Law Decoder) Transfer Characteristic

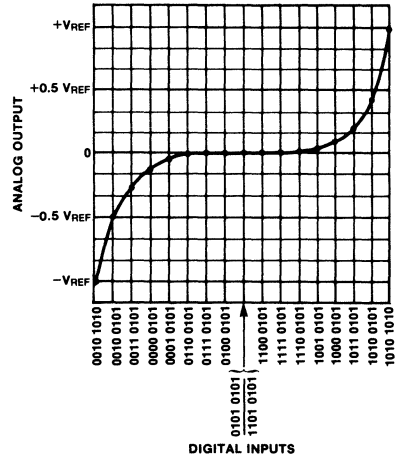
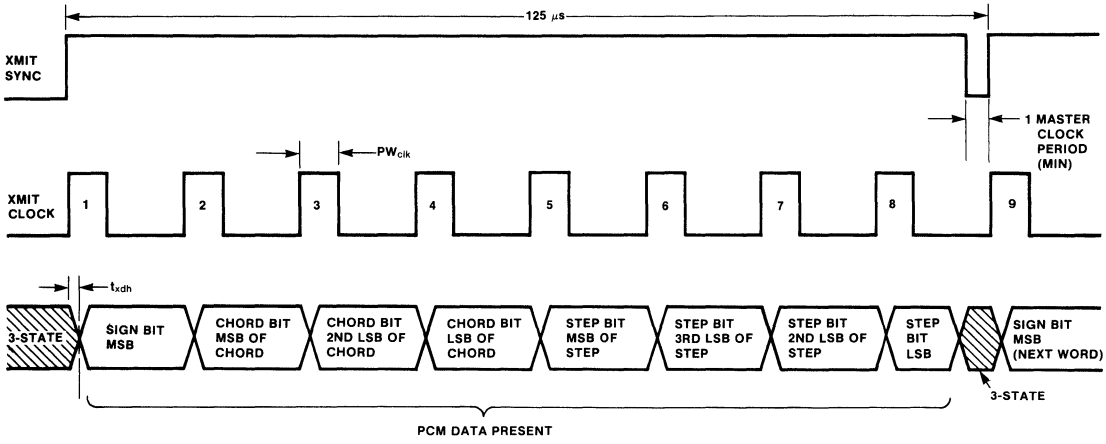
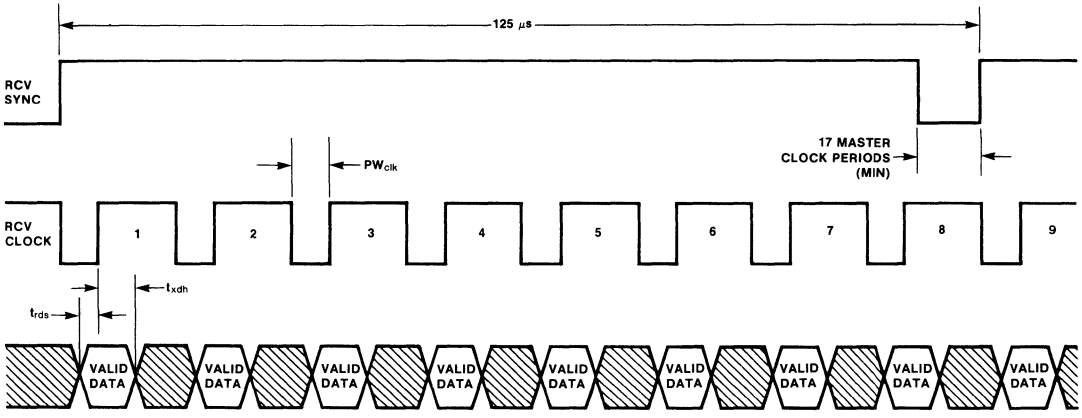


Fig. 10 64 kHz Operation, Transmitter Section Timing



Note
All rise and fall times are measured from 0.4 V and 2 4 V. All delay times are measured from 1.4 V.

Fig. 11 64 kHz Operation, Receiver Section Timing



Note
All rise and fall times are measured from 0.4 V and 2.4 V. All delay times are measured from 1 4 V.

8

Performance Evaluation

The equipment connections shown in *Figure 12* can be used to evaluate the performance of the 5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (Pin 1) of the 5156. The Digital Output of the codec is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3552A. Remaining pins of the 5156 are connected as follows:

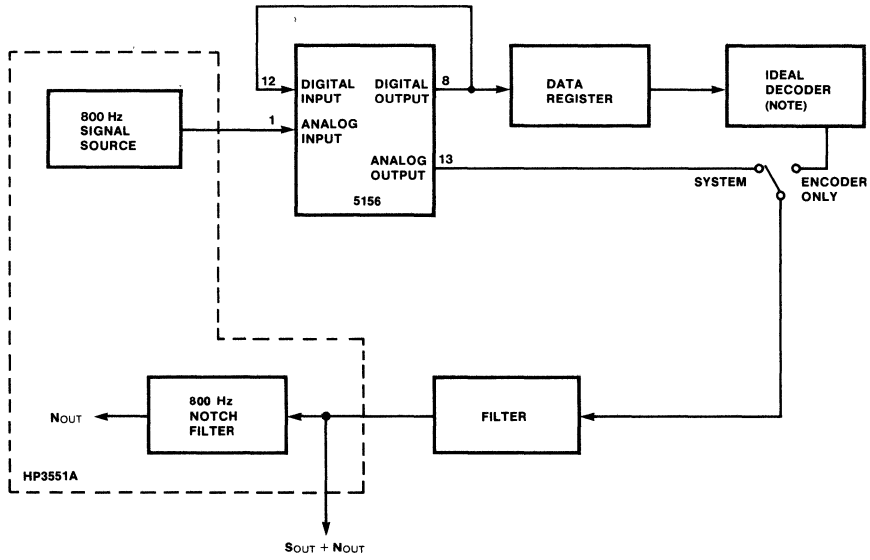
1. RCV SYNC is tied to XMIT SYNC.
2. XMIT Clock is tied to Master Clock. The signal is inverted and tied to RCV Clock.

The following timing signals are required:

1. Master Clock = 2.048 MHz
2. XMIT SYNC repetition rate = 8 kHz
3. XMIT SYNC width = 8 XMIT Clock periods

When all the above requirements are met, the set-up of *Figure 12* permits the measurement of synchronous system performance over a wide range of Analog Inputs. The data register and ideal decoder provide a means of checking the encoder portion of the 5156 independently of the decoder section. To test the system in the asynchronous mode, Master Clock should be separated from XMIT Clock and from RCV Clock; XMIT Clock and RCV Clock are separated also.

Fig. 12 System Characteristics Test Configuration



Note

The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

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μA555
Single Timing Circuit

Special Function Products

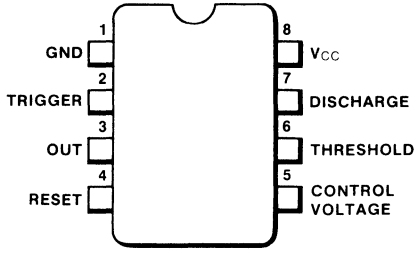
Description

The μA555 Timing Circuit is a very stable controller for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied ending the time-out.

The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

- **TIMING CONTROL, NS TO HOURS**
- **ASTABLE OR MONOSTABLE OPERATING MODES**
- **ADJUSTABLE DUTY CYCLE**
- **200 mA SINK OR SOURCE OUTPUT CURRENT**
- **TTL OUTPUT DRIVE CAPABILITY**
- **TEMPERATURE STABILITY OF 0.005% PER °C**
- **NORMALLY ON OR NORMALLY OFF OUTPUT**
- **DIRECT REPLACEMENT FOR SE555/NE555**

Connection Diagrams
8-Pin DIP

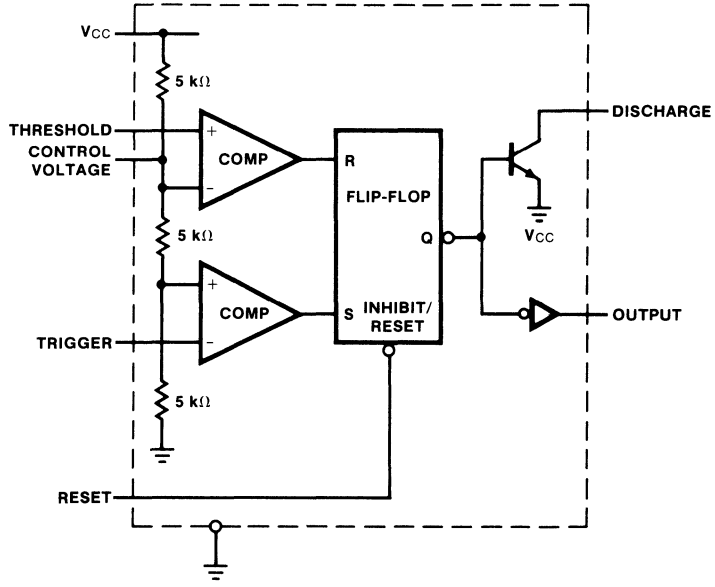


(Top View)

Order Information

Type	Package	Code	Part No.
μA555	Molded DIP	9T	μA555TC

Block Diagram



9

μA555
Electrical Characteristics $T_A = 25°C$, $V_{CC} = +5.0$ V to $+15$ V, unless otherwise specified

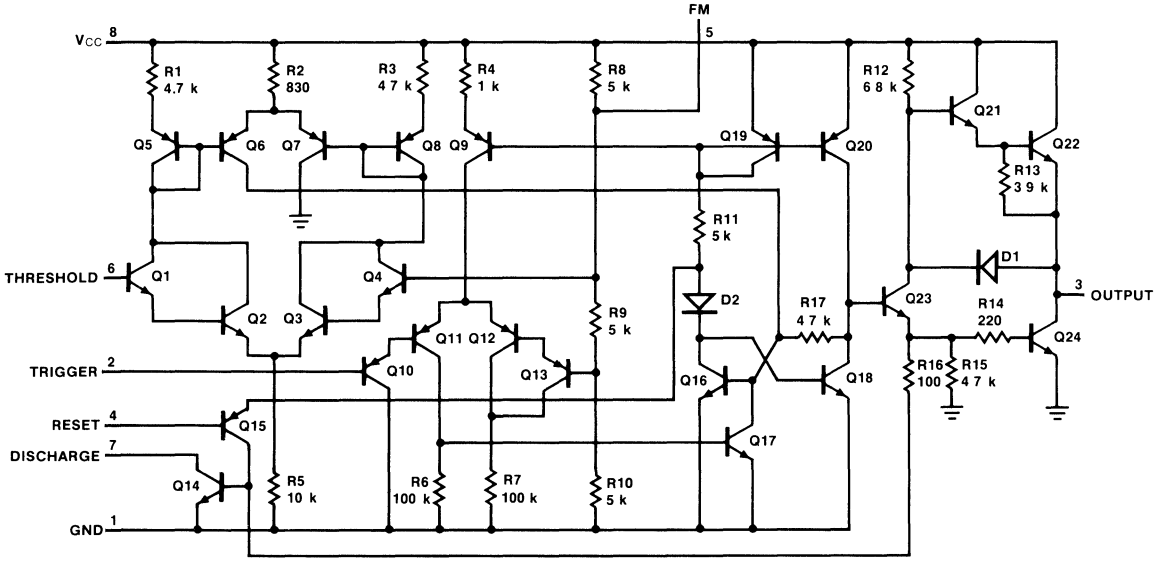
Characteristic	Condition	Min	Typ	Max	Unit
Supply Voltage		4.5		16	V
Supply Current	$V_{CC} = 5.0$ V, $R_L = \infty$		3.0	6.0	mA
	$V_{CC} = 15$ V, $R_L = \infty$ LOW State (Note 1)		10	15	mA
Timing Error					
Initial Accuracy	R_A, $R_B = 1$ kΩ to 100 kΩ		1.0		%
Drift with Temperature	C = 0.1 μF (Note 2)		50		ppm/°C
Drift with Supply Voltage			0.1		% V
Threshold Voltage			2/3		X V_{CC}
Trigger Voltage	$V_{CC} = 15$ V		5.0		V
	$V_{CC} = 5.0$ V		1.67		V
Trigger Current			0.5		μA
Reset Voltage		0.4	0.7	1.0	V
Reset Current			0.1		mA
Threshold Current	Note 3		0.1	0.25	μA
Control Voltage Level	$V_{CC} = 15$ V	9.0	10	11	V
	$V_{CC} = 5.0$ V	2.6	3.33	4.0	V
Output Voltage Drop (LOW)	$V_{CC} = 15$ V, $I_{SINK} = 10$ mA		0.1	0.25	V
	$I_{SINK} = 50$ mA		0.4	0.75	V
	$I_{SINK} = 100$ mA		2.0	2.5	V
	$I_{SINK} = 200$ mA		2.5		V
	$V_{CC} = 5.0$ V, $I_{SINK} = 8.0$ mA				V
	$I_{SINK} = 5.0$ mA		0.25	0.35	V
Output Voltage Drop (HIGH)	$I_{SOURCE} = 200$ mA, $V_{CC} = 15$ V		12.5		V
	$I_{SOURCE} = 100$ mA, $V_{CC} = 15$ V	12.75	13.3		V
	$V_{CC} = 5.0$ V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Notes
1. Supply Current is typically 1.0 mA less when output is HIGH.
2. Tested at $V_{CC} = 5.0$ V and $V_{CC} = 15$ V.
3. This will determine the maximum value of $R_A + R_B$. For 15 V operation, the maximum total R = 20 MΩ.
4. For operating at elevated temperatures, the device must be derated based on a $+125°C$ maximum junction temperature and a thermal resistance of $+150°$ C/W junction to ambient

Absolute Maximum Ratings

Supply Voltage	+18 V
Power Dissipation (Note 1)	600 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering, 10 s)	260°C

Equivalent Circuit

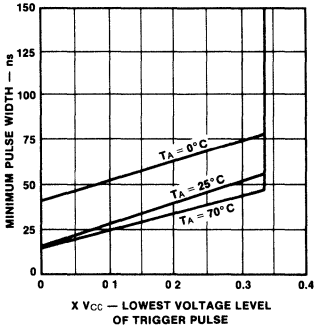


Note

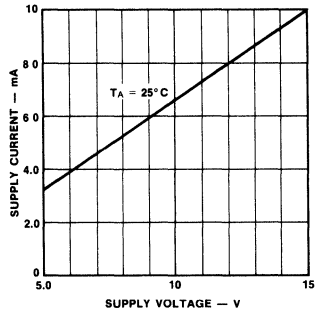
1. Supply Current is typically 1.0 mA less when output is HIGH.

Typical Performance Curves

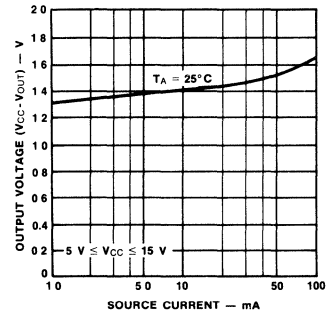
Minimum Pulse Width Required for Triggering



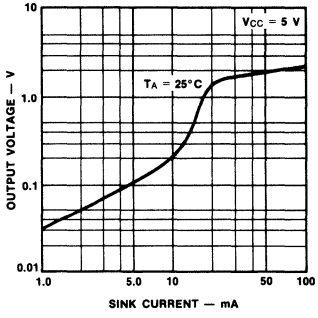
Total Supply Current vs Supply Voltage



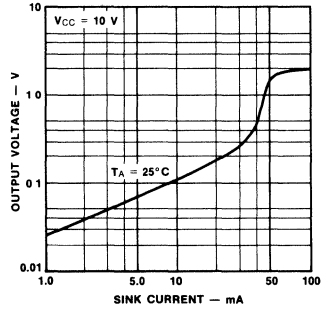
High Output Voltage vs Output Source Current



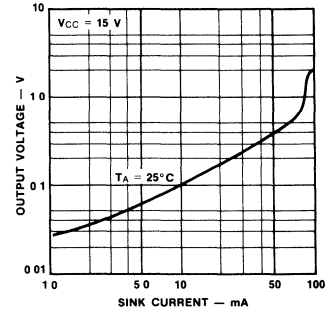
Low Output Voltage vs Output Sink Current



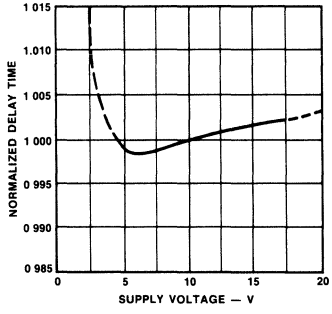
Low Output Voltage vs Output Sink Current



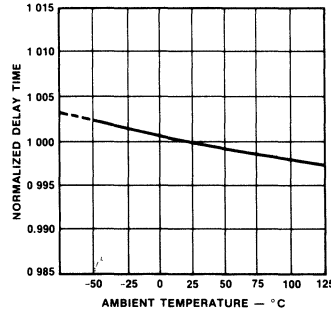
Low Output Voltage vs Output Sink Current



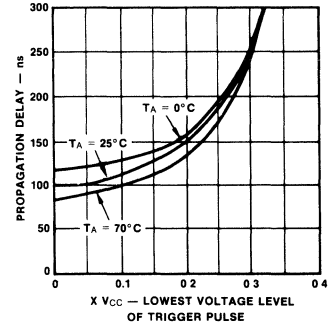
Delay Time vs Supply Voltage



Delay Time vs Ambient Temperature



Propagation Delay vs Voltage Level of Trigger Pulse



Typical Applications

Monostable Operation

In the monostable mode, the timer functions as a one-shot. Referring to *Figure 1* the external capacitor is initially held discharged by a transistor inside the timer.

The circuit triggers on a negative-going input signal when the level reaches ⅓ V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by *Figure 3*. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ = R1C1. When the voltage across the capacitor equals ⅔ V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. *Figure 2* shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possibility of false triggering.

Fig. 1

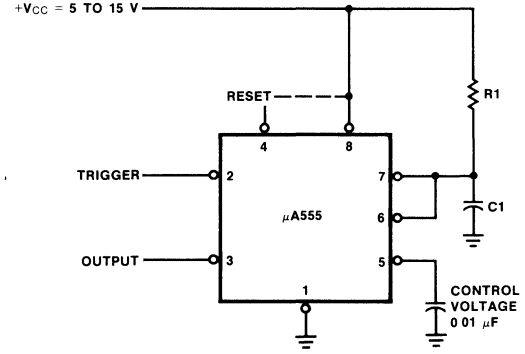


Fig. 2

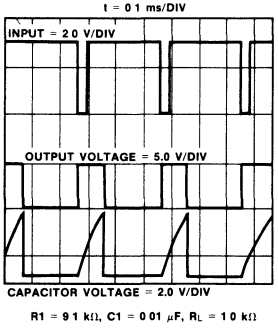
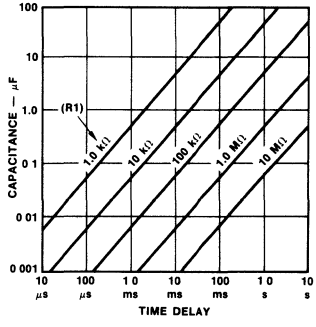


Fig. 3 Time Delay vs R1 and C1



9

Typical Applications (Con't)

Astable Operation
When the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between ⅓ V_{CC} and ⅔ V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by *Figure 6.*

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

Fig. 4

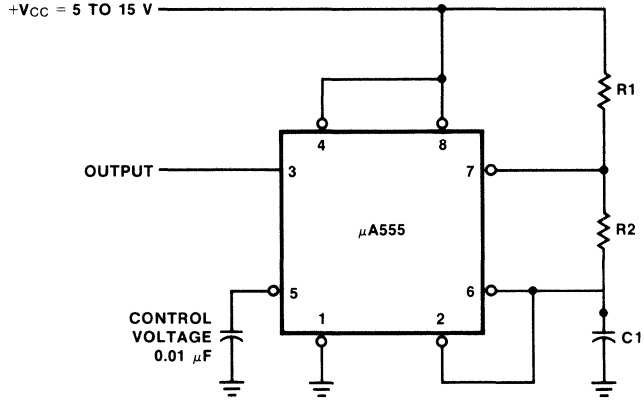


Fig. 5

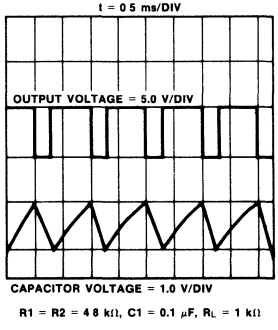
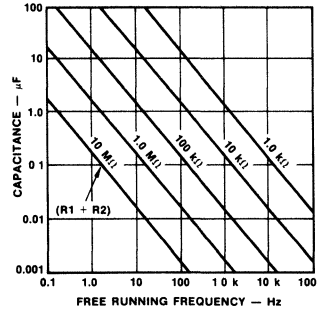


Fig. 6 Free Running Frequency vs R1, R2, and C1



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μA556
Dual Timing Circuit

Special Function Products

Description

The μA556 Timing Circuits are very stable controllers for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied, ending the time-out.

The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

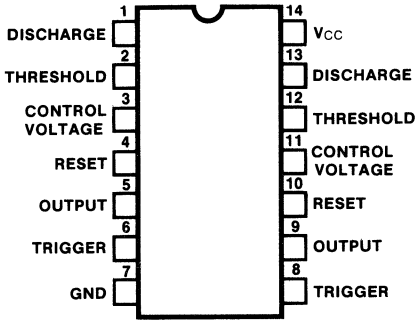
The μA556 Dual Timing Circuit is a pair of 555s for use in sequential timing or applications requiring multiple timers.

- **TIMING CONTROL, μs TO HOURS**
- **ASTABLE OR MONOSTABLE OPERATING MODES**
- **ADJUSTABLE DUTY CYCLE**
- **200 mA SINK OR SOURCE OUTPUT CURRENT**
- **TTL OUTPUT DRIVE CAPABILITY**
- **TEMPERATURE STABILITY OF 0.005% PER °C**
- **NORMALLY ON OR NORMALLY OFF OUTPUT**

Absolute Maximum Ratings

Supply Voltage	+18 V
Power Dissipation	600 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering, 10 s)	260°C

Connection Diagram
14-Pin DIP

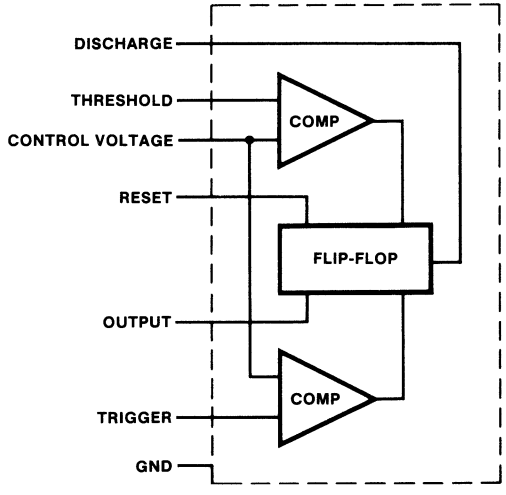


(Top View)

Order Information

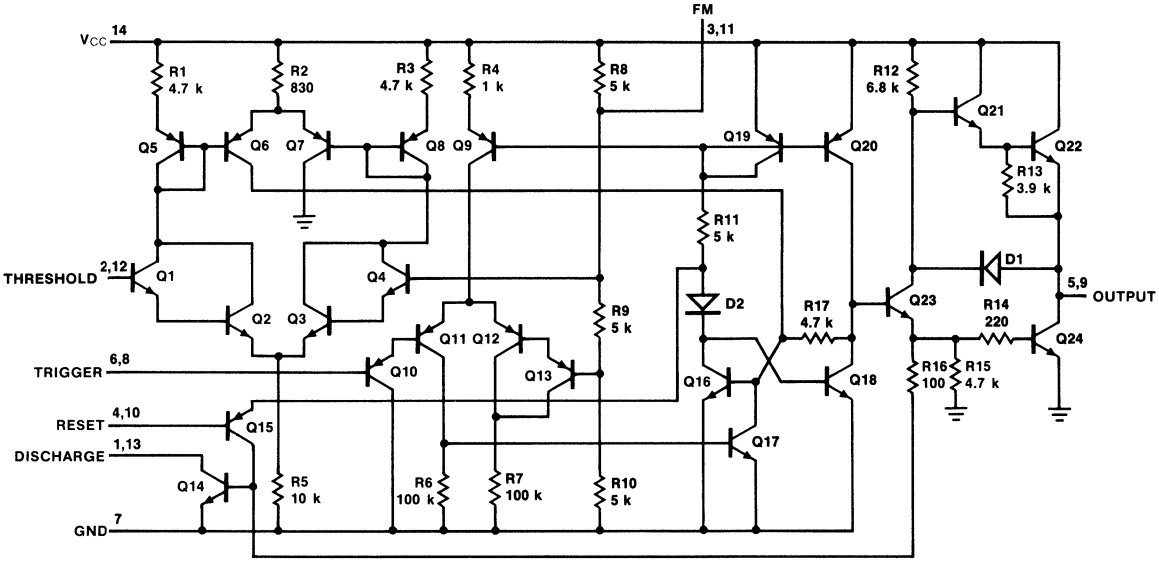
Type	Package	Code	Part No.
μA556	Molded DIP	9A	μA556PC

Block Diagram (1/2 of circuit shown)



9

Equivalent Circuit (1/2 of circuit shown)



Notes

1. Supply current when output is HIGH is typically 1.0 mA less.
2. Tested at V_{CC} = 5 V and V_{CC} = 15 V.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 MΩ.
4. Matching characteristics refer to the difference between performance characteristics of each timer section.

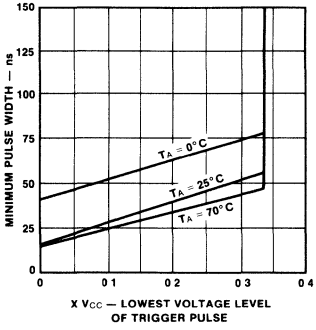
μA556
Electrical Characteristics $T_A = 25°C$, $V_{CC} = +5.0$ V to $+15$ V, unless otherwise specified

Characteristic	Condition	Min	Typ	Max	Unit
Supply Voltage		4.5		16	V
Supply Current (Total)	$V_{CC} = 5.0$ V, $R_L = \infty$		6.0	12	mA
	$V_{CC} = 15$ V, $R_L = \infty$ LOW State (Note 1)		20	28	mA
Timing Error (Monostable)					
Initial Accuracy	$R_A = 2$ kΩ to 100 kΩ		0.75		%
Drift with Temperature	C = 0.1 μF (Note 2)		50		ppm/°C
Drift with Supply Voltage			0.1		% V
Timing Error (Astable)					
Initial Accuracy	R_A, $R_B = 2$ kΩ to 100 kΩ		2.25		%
Drift with Temperature	C = 0.1 μF (Note 2)		150		ppm/°C
Drift with Supply Voltage			0.3		% V
Threshold Voltage			2/3		X V_{CC}
Threshold Current	(Note 3)		30	250	nA
Trigger Voltage	$V_{CC} = 15$ V		5.0		V
	$V_{CC} = 5.0$ V		1.67		V
Trigger Current			0.5		μA
Reset Voltage		0.4	0.7	1.0	V
Reset Current			0.1		mA
Control Voltage Level	$V_{CC} = 15$ V	9.0	10	11	V
	$V_{CC} = 5.0$ V	2.6	3.33	4.0	V
Output Voltage (LOW)	$V_{CC} = 15$ V				
	$I_{SINK} = 10$ mA		0.1	0.25	V
	$I_{SINK} = 50$ mA		0.4	0.75	V
	$I_{SINK} = 100$ mA		2.0	2.75	V
	$I_{SINK} = 200$ mA		2.5		V
	$V_{CC} = 5.0$ V				
	$I_{SINK} = 8.0$ mA				V
	$I_{SINK} = 5.0$ mA		0.25	0.35	V
	$I_{SOURCE} = 200$ mA				
Output Voltage (HIGH)	$V_{CC} = 15$ V		12.5		V
	$I_{SOURCE} = 100$ mA				
	$V_{CC} = 15$ V	12.75	13.3		V
	$V_{CC} = 5.0$ V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns
Discharge Leakage Current			20	100	nA
Matching Characteristics (Note 4)					
Initial Timing Accuracy			0.1	0.2	%
Timing Drift with Temperature			± 10		ppm/°C
Drift with Supply Voltage			0.2	0.5	% V

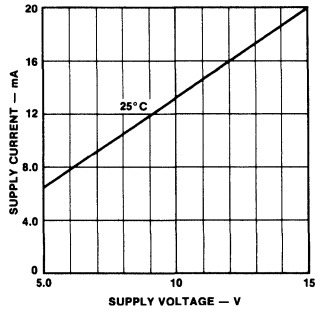
Notes on preceding page

Typical Performance Curves

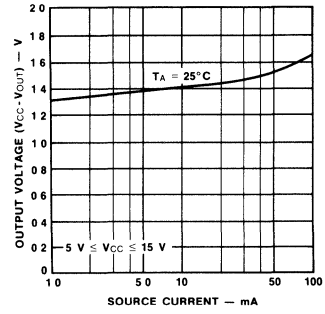
Minimum Pulse Width Required for Triggering



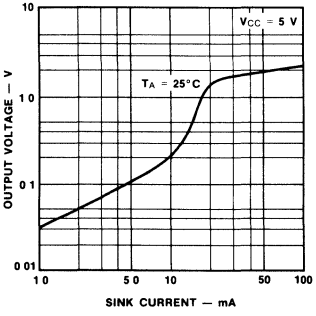
Total Supply Current vs Supply Voltage



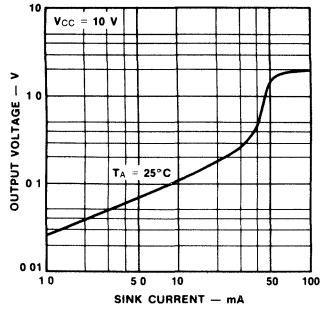
High Output Voltage vs Output Source Current



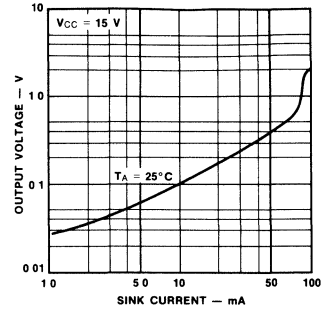
Low Output Voltage vs Output Sink Current



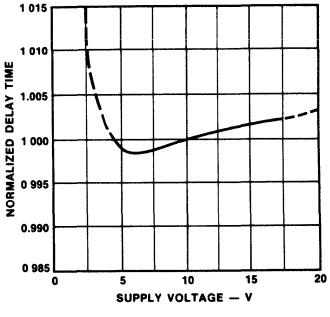
Low Output Voltage vs Output Sink Current



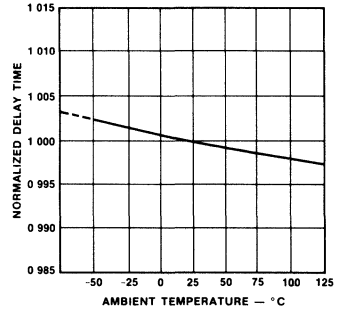
Low Output Voltage vs Output Sink Current



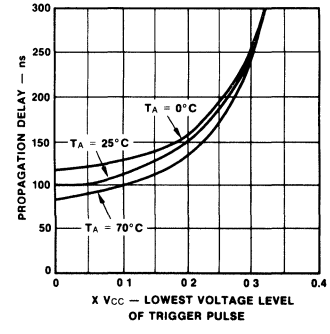
Delay Time vs Supply Voltage



Delay Time vs Ambient Temperature



Propagation Delay vs Voltage Level of Trigger Pulse



Typical Applications

Monostable Operation

In the monostable mode, the timer functions as a one-shot. Referring to *Figure 1* the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to pin 6, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH. The voltage across the capacitor, increases exponentially with the time constant $\tau = R1C1$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. *Figure 2* shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by *Figure 3.* Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 6) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied high to avoid any possibility of false triggering.

Fig. 1

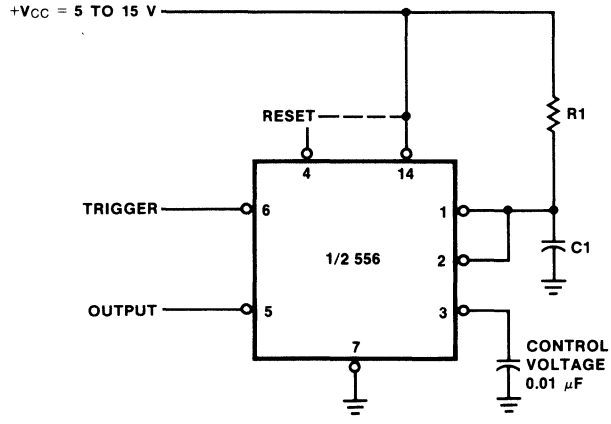


Fig. 2

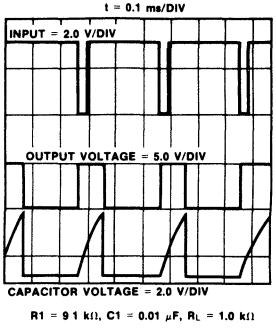
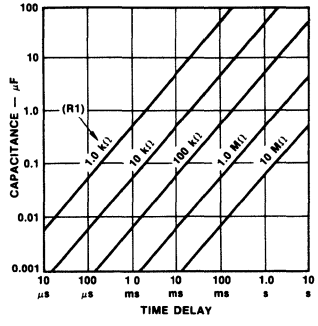


Fig. 3



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Typical Applications (Cont.)

Astable Operation

When the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by *Figure 6*.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

Fig. 4

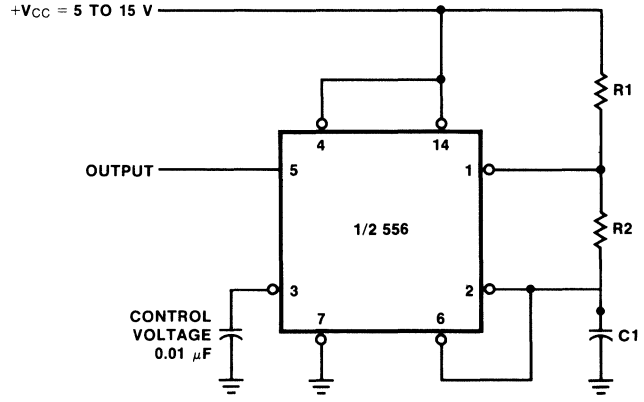


Fig. 5

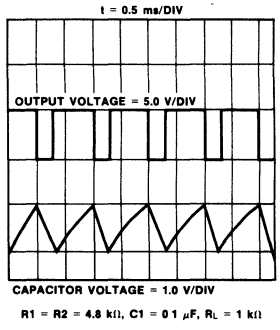
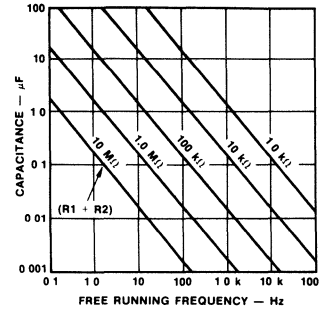


Fig. 6 Free Running Frequency vs R1, R2 and C1



FAIRCHILD
A Schlumberger Company

μA726 Temperature-Controlled Differential Pair

Special Function Products

Description

The μA726 is a Monolithic Transistor Pair in a high thermal-resistant package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers. It is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar process.

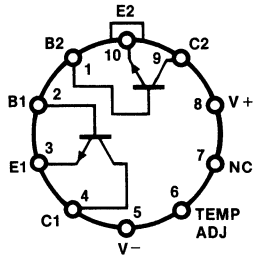
Absolute Maximum Ratings

Operating Temperature Range	
Military (μA726)	−55°C to +125°C
Commercial (μA726C)	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering 60 s)	300°C
Supply Voltage	± 18 V
Internal Power Dissipation	500 mW

Maximum Ratings for Each Transistor

Collector-to-Emitter Voltage, V_{CEO}	30 V
Collector-to-Base Voltage, V_{CBO}	40 V
Collector-to-Substrate Voltage, V_{CIO}	40 V
Emitter-to-Base Voltage, V_{EBO}	5 V
Collector Current, I_C	5 mA

Connection Diagram
10-Pin Metal Package

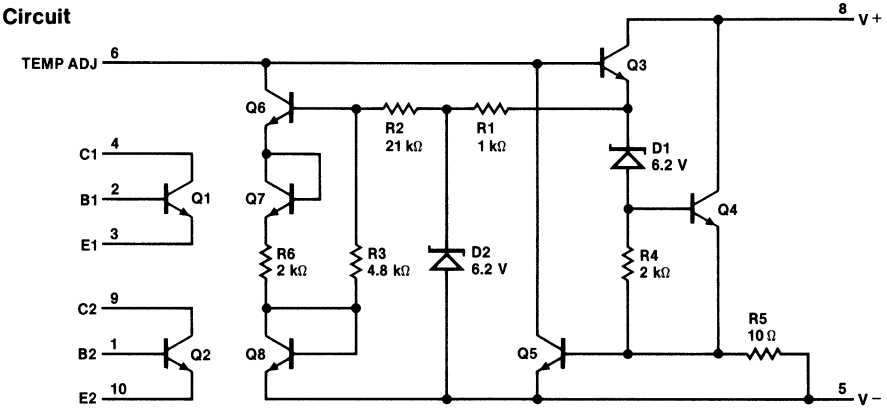


(Top View)

Order Information

Type	Package	Code	Part No.
μA726	Metal	5U	μA726HM
μA726C	Metal	5U	μA726HC

Equivalent Circuit



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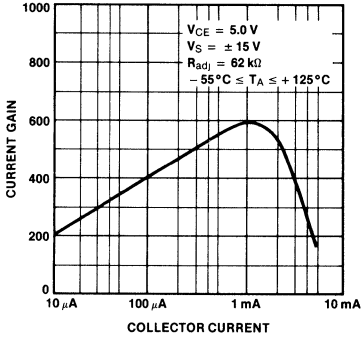
μA726
Electrical Characteristics Min ≤ T_A ≤ Max, V_S = ± 15 V, R_{adj} = 62 kΩ unless otherwise specified.

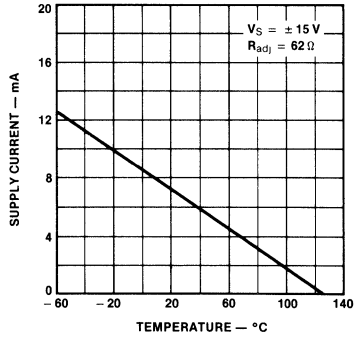
Characteristic	Condition	μA726			μA726C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	10 μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50 Ω		1.0	2.5		1.0	3.0	mV
Input Offset Current	I_C = 10 μA, V_{CE} = 5 V		10	50		10	100	nA
	I_C = 100 μA, V_{CE} = 5 V		50	200		50	400	nA
Average Input Bias Current	I_C = 10 μA, V_{CE} = 5 V		50	150		50	300	nA
	I_C = 100 μA, V_{CE} = 5 V		250	500		250	1000	nA
Offset Voltage Change	I_C = 10 μA, 5 V ≤ V_{CE} ≤ 25 V, R_S ≤ 100 kΩ		0.3	6.0		0.3	6.0	mV
	I_C = 100 μA, 5 V ≤ V_{CE} ≤ 25 V, R_S ≤ 10 kΩ		0.3	6.0		0.3	6.0	mV
Input Offset Voltage Drift	10 μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50 Ω, +25°C ≤ T_A ≤ Max		0.2	1.0		0.2	2.0	μV/°C
Input Offset Voltage Drift	10 μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50 Ω, Min ≤ T_A ≤ +25°C		0.2	1.0		0.2	2.0	μV/°C
Input Offset Current Drift	I_C = 10 μA, V_{CE} = 5 V		10			10		pA/°C
	I_C = 100 μA, V_{CE} = 5 V		30			30		pA/°C
Supply Voltage Rejection Ratio	10 μA ≤ I_C ≤ 100 μA, R_S ≤ 50 Ω		25			25		μV/V
Low Frequency Noise	I_C = 10 μA, V_{CE} = 5V, R_S ≤ 50 Ω BW = .001 Hz to 0.1 Hz		4.0			4.0		μV p-p
Broadband Noise	I_C = 10 μA, V_{CE} = 5 V, R_S ≤ 50 Ω BW = 0.1 Hz to 10 kHz		10			10		μV p-p
Long-term Drift	10 μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50 Ω, T_A = 25°C		5.0			5.0		μV/ week
High Frequency Current Gain	f = 20 MHz, I_C = 100 μA, V_{CE} = 5 V	1.5	3.5		1.5	3.5		
Output Capacitance	I_E = 0, V_{CB} = 5 V		1.0			1.0		pF
Emitter Transition Capacitance	I_E = 100 μA		1.0			1.0		pF
Collector Saturation Voltage	I_B = 100 μA, I_C = 1 mA		0.5	1.0		0.5	1.0	V

Typical Performance Curves for μA726

Current Gain as a Function of Collector Current

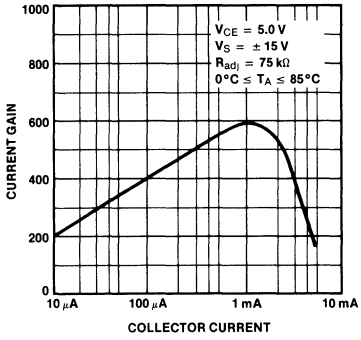


Supply Current as a Function of Ambient Temperature

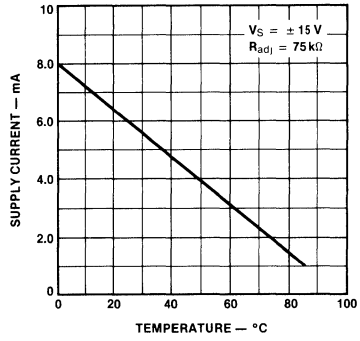


Typical Performance Curves for μA726C (Cont.)

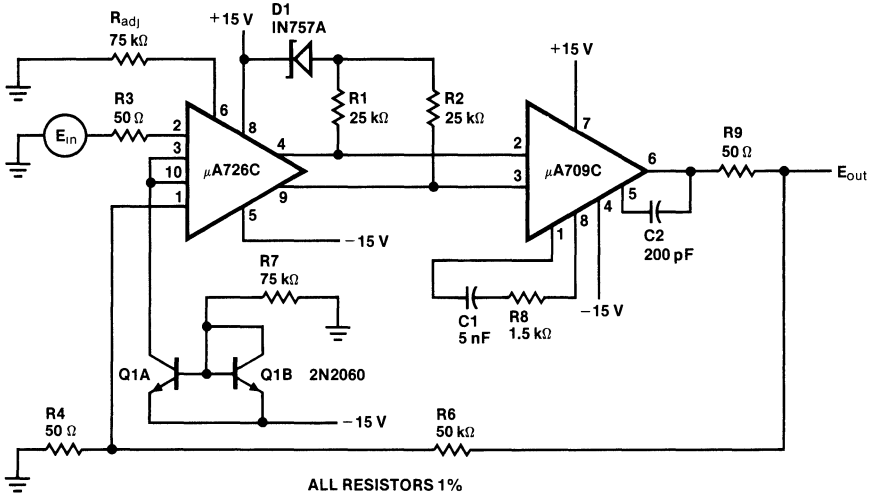
Current Gain as a Function of Collector Current



Supply Current as a Function of Ambient Temperature



Typical x1000 Amplifier Circuit



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FAIRCHILD

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μA727 Temperature-Controlled Differential Preamplifier

Special Function Products

Description

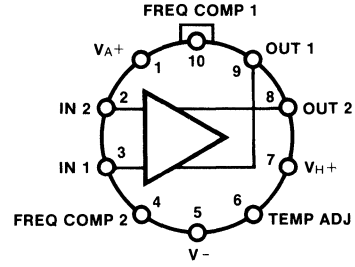
The μA727 is a monolithic, fixed gain, Differential Input/Output Preamplifier, constructed with the Fairchild Planar epitaxial process, mounted in a high thermal resistance package, and held at constant temperature by active regulator circuitry. The high gain and low-standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low drift dc amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain-gauge transducers, and a/d converters.

- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE 300 MΩ**
- **WIDE COMMON MODE RANGE C_{MRR} = 100 dB**

Absolute Maximum Ratings

Operating Temperature Range	
Military (μA727)	−55°C to +125°C
Commercial (μA727C)	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering, 60 s)	300°C
Internal Power Dissipation	500 mW
Supply Voltage (Amplifier and Heater)	± 18 V
Differential Input Voltage	± 10 V
Common Mode Input Voltage	± 15 V

Connection Diagram
10-Pin Metal Package

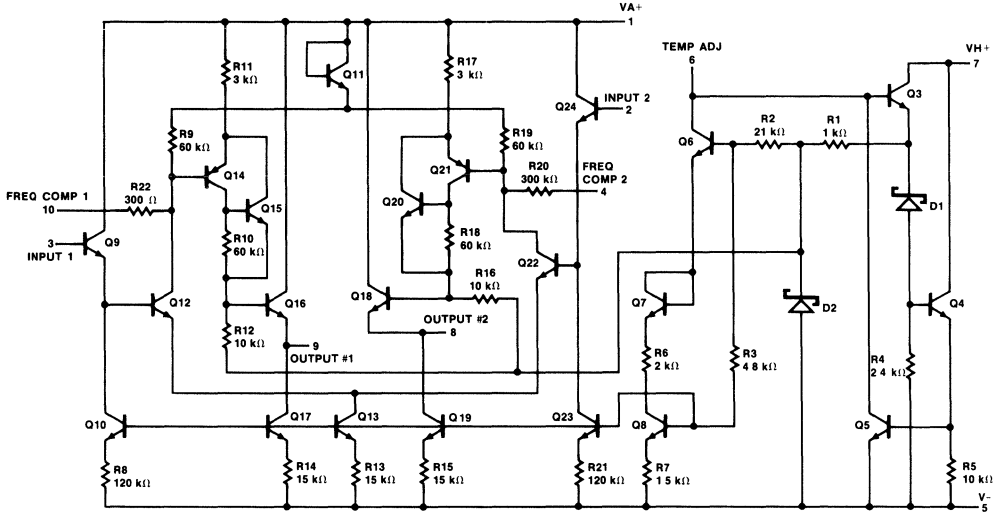


(Top View)

Order Information

Type	Package	Code	Part No.
μA727	Metal	5U	μA727HM
μA727C	Metal	5U	μA727HC

Equivalent Circuit



μA727
Electrical Characteristics $-55°C \leq T_A \leq +125°C$, $V_H+ = +15$ V, $V- = -15$ V, $R_{ADJ} = 330$ kΩ, unless otherwise specified.

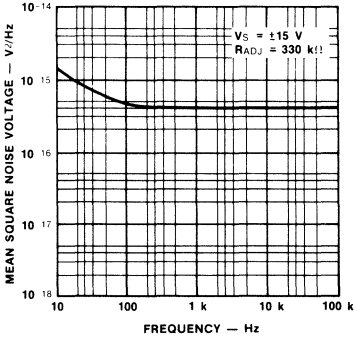
Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0	10	mV
Input Offset Current			2.5	15	nA
Input Bias Current			12	40	nA
Input Offset Voltage Drift	$R_S \leq 50\ \Omega$, $+25°C \leq T_A \leq +125°C$		0.6	1.5	μV/°C
	$R_S \leq 50\ \Omega$, $-55°C \leq T_A \leq +25°C$		0.6	1.5	μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		2.0		pA/°C
	$-55°C \leq T_A \leq +25°C$		2.0		pA/°C
Input Bias Current Drift	$-55°C \leq T_A \leq +125°C$		15		pA/°C
Differential Input Resistance			300		MΩ
Common-Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		80		μV/V
Common-Mode Rejection Ratio	$R_S \leq 100$ kΩ	80	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common-Mode Voltage		−6.0	−5.0	−4.0	V
Differential Output Voltage Swing		±5.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	10	μV/μA
Differential Voltage Gain		60	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\ \Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\ \Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

μA727C
Electrical Characteristics $-20°C \leq T_A \leq +85°C$, $V_H+ = V_A+ = +15$ V, $V- = -15$ V, $R_{ADJ} = 1$ MΩ, unless otherwise specified.

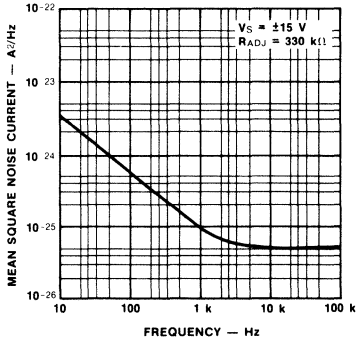
Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0	10	mV
Input Offset Current			2.5	25	nA
Input Bias Current			12	75	nA
Input Offset Voltage Drift	$R_S \leq 50\ \Omega$		0.6	3.0	μV/°C
Input Offset Current Drift			2.0		pA/°C
Input Bias Current Drift			15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ	70	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−7.0	−5.0	−4.0	V
Differential Output Voltage Swing		±3.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	15	μV/μA
Differential Voltage Gain		50	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\ \Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\ \Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

Typical Performance Curves

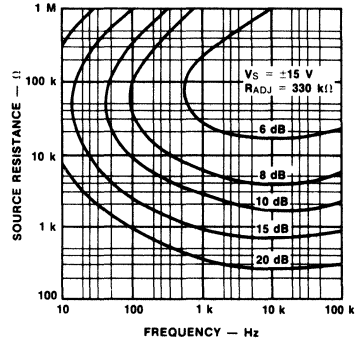
Noise Voltage vs Frequency



Noise Current vs Frequency

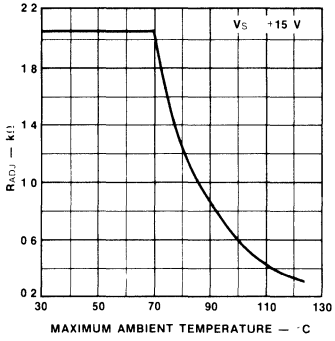


Spot Noise Contours

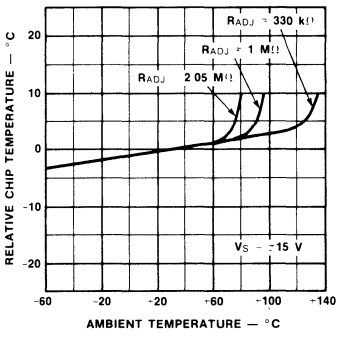


Typical Performance Curves (Cont.)

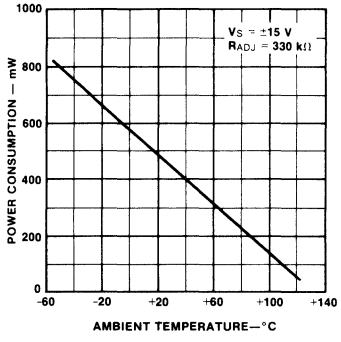
Recommended R_{ADJ} vs Maximum Ambient Temperature



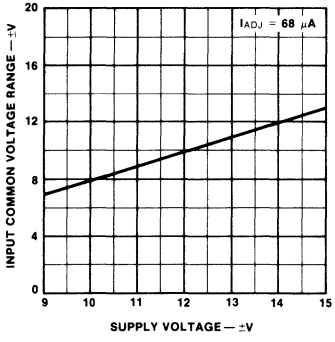
Relative Chip Temperature vs Ambient Temperature



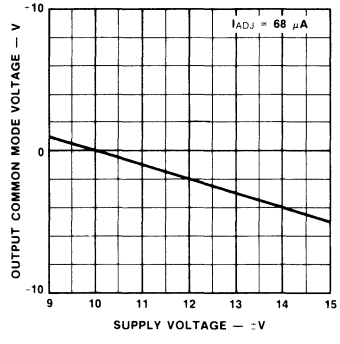
Power Consumption vs Ambient Temperature



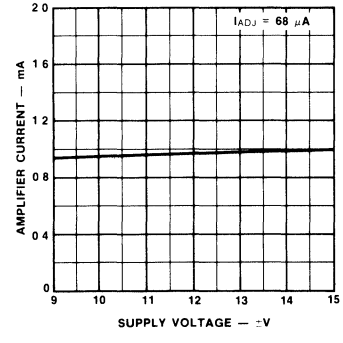
Input Common-Mode Voltage Range vs Supply Voltage



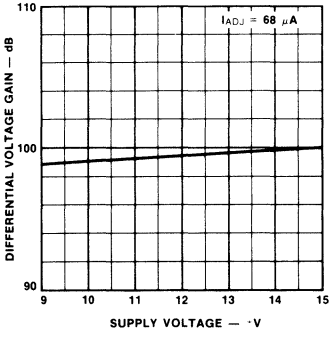
Output Common-Mode Voltage vs Supply Voltage



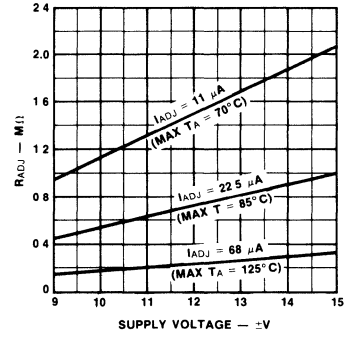
Amplifier Current vs Supply Voltage



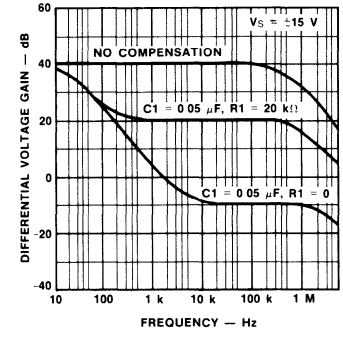
Differential Voltage Gain vs Supply Voltage



Required R_{ADJ} for Constant I_{ADJ} vs Supply Voltage



Open Loop Frequency Response for Various Values of Compensation



9

FAIRCHILD

A Schlumberger Company

μA733 Differential Video Amplifier

Linear Products

Description

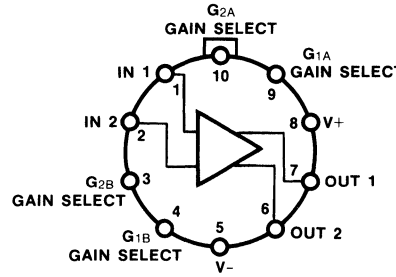
The μA733 is a monolithic two-stage Differential Input, Differential Output Video Amplifier constructed using the Fairchild Planar epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low-phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high-power supply and common-mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

- **120 MHz BANDWIDTH**
- **250 kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100, AND 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

Absolute Maximum Ratings

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	
Metal Package	500 mW
DIP	670 mW
Operating Temperature Range	
Military (μA733)	−55°C to +125°C
Commercial (μA733C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering)	
Metal Package (60 s)	300°C
Ceramic DIP (60 s)	300°C
Molded DIP (10 s)	260°C

Connection Diagram 10-Pin Metal Package



(Top View)

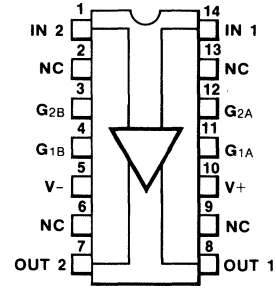
Note

Pin 5 connected to case

Order Information

Type	Package	Code	Part No.
μA733	Metal	5X	μA733HM
μA733C	Metal	5X	μA733HC

Connection Diagram 14-Pin DIP



(Top View)

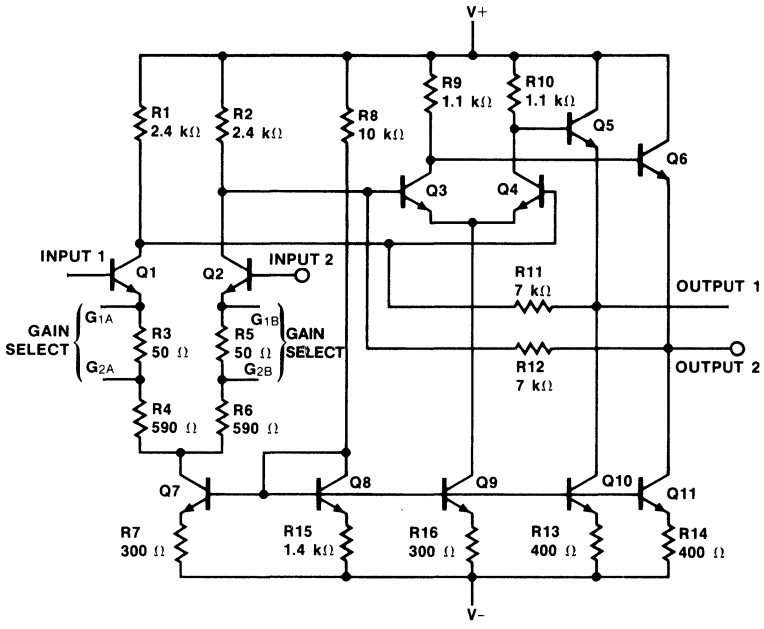
Order Information

Type	Package	Code	Part No.
μA733	Ceramic DIP	6A	μA733DM
μA733C	Ceramic DIP	6A	μA733DC
μA733C	Molded DIP	9A	μA733PC

Note

1 Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal and 8.3 mW/°C for the DIP.

Equivalent Circuit



μA733 and μA733C
Electrical Characteristics $T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified

Characteristic	Condition	μA733			μA733C			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain								
Gain 1, Note 2		300	400	500	250	400	600	
Gain 2, Note 3		90	100	110	80	100	120	
Gain 3, Note 4		9.0	10	11	8.0	10	12	
Bandwidth	$R_S = 50\ \Omega$							
Gain 1			40			40		MHz
Gain 2			90			90		MHz
Gain 3			120			120		MHz
Risetime	$R_S = 50\ \Omega$, $V_{OUT} = 1\ V_{p-p}$							
Gain 1			10.5			10.5		ns
Gain 2			4.5	10		4.5	12	ns
Gain 3			2.5			2.5		ns
Propagation Delay	$R_S = 50\ \Omega$, $V_{OUT} = 1\ V_{p-p}$							
Gain 1			7.5			7.5		ns
Gain 2			6.0	10		6.0	10	ns
Gain 3			3.6			3.6		ns
Input Resistance								
Gain 1			4.0			4.0		kΩ
Gain 2		20	30		10	30		kΩ
Gain 3			250			250		kΩ
Input Capacitance	Gain 2		2.0			2.0		pF
Input Offset Current			0.4	3.0		0.4	5.0	μA
Input Bias Current			9.0	20		9.0	30	μA
Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1 kHz to 10 MHz		12			12		μV_{rms}
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio								
Gain 2	$V_{CM} = \pm 1$ V, f ≤ 100 kHz	60	86		60	86		dB
Gain 2	$V_{CM} = \pm 1$ V, f = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio								
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		50	70		dB
Output Offset Voltage								
Gain 1			0.6	1.5		0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0		0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		3.0	4.0		V_{pk-pk}
Output Sink Current		2.5	3.6		2.5	3.6		mA
Output Resistance			20			20		Ω
Power Supply Current			18	24		18	24	mA

Notes
2. Gain Select pins G_{1A} and G_{1B} connected together.
3. Gain Select pins G_{2A} and G_{2B} connected together.
4. All Gain Select pins open.

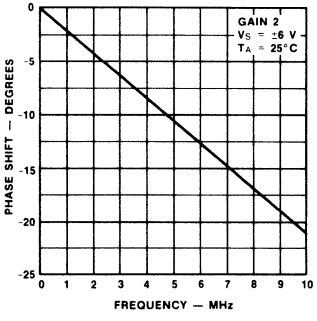
μA733 and μA733C
Electrical Characteristics (Cont.) The following specifications apply for min ≤ T_A ≤ max

Characteristic	Condition	μA733 Min	μA733 Typ	μA733 Max	μA733C Min	μA733C Typ	μA733C Max	Unit
Differential Voltage Gain								
Gain 1, Note 2		200		600	250		600	
Gain 2, Note 3		80		120	80		120	
Gain 3, Note 4		8.0		12	8.0		12	
Input Resistance								
Gain 2		8.0			8.0			kΩ
Input Offset Current				5.0			6.0	μA
Input Bias Current				40			40	μA
Input Voltage Range		± 1.0			± 1.0			V
Common Mode Rejection Ratio		50			50			dB
Supply Voltage Rejection Ratio		50			50			dB
Output Offset Voltage								
Gain 1				1.5				
Gain 2 and Gain 3				1.2			1.5	V
Output Swing		2.5			2.8			V_{pk-pk}
Output Sink Current		2.2			2.5			mA
Positive Supply Current				27			27	mA

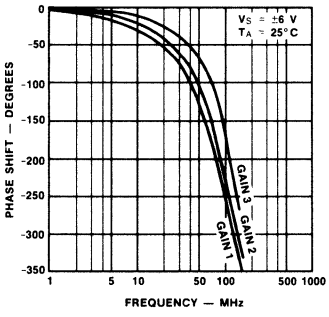
Notes
2 Gain Select pins G_{1A} and G_{1B} connected together
3. Gain Select pins G_{2A} and G_{2B} connected together.
4. All Gain Select pins open.

Typical Performance Curves

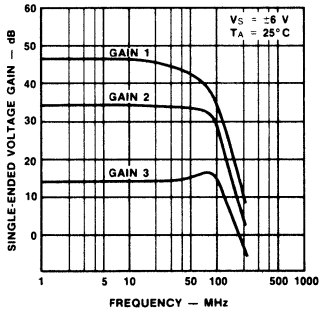
Phase Shift vs Frequency



Phase Shift vs Frequency

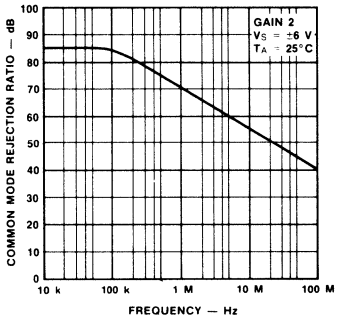


Voltage Gain vs Frequency

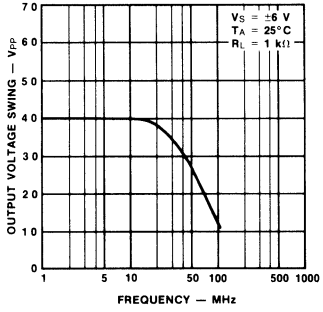


Typical Performance Curves (Cont.)

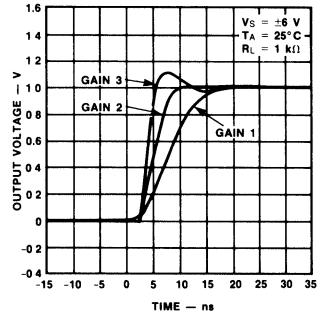
Common Mode Rejection Ratio vs Frequency



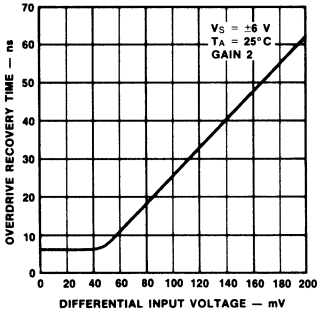
Output Voltage Swing vs Frequency



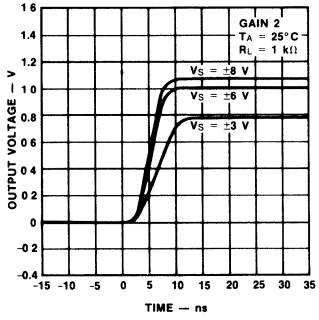
Pulse Response



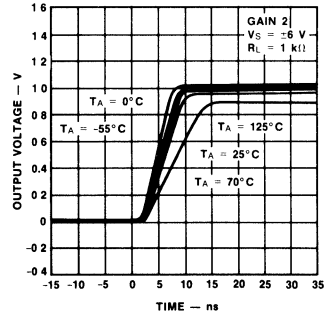
Differential Overdrive Recovery Time



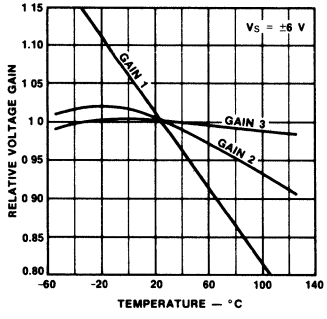
Pulse Response vs Supply Voltage



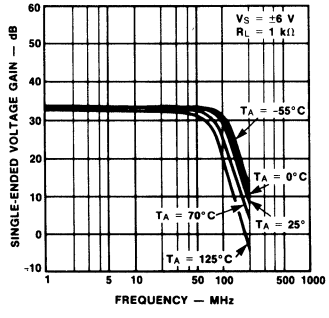
Pulse Response vs Temperature



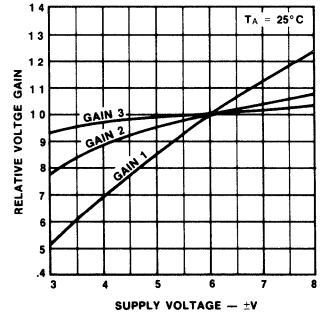
Voltage Gain vs Temperature



Gain Versus Frequency vs Temperature

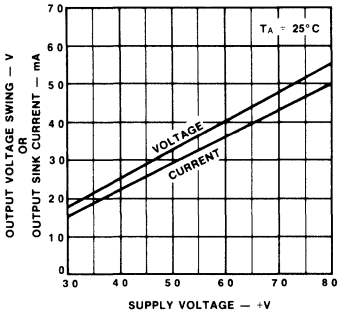


Voltage Gain vs Supply Voltage

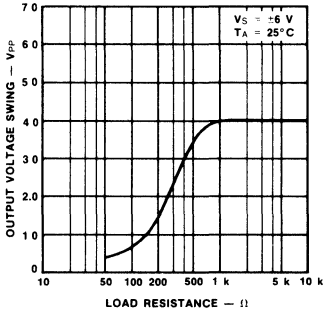


Typical Performance Curves (Cont.)

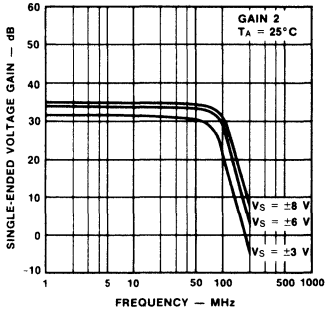
Output Voltage and Current Swing vs Supply Voltage



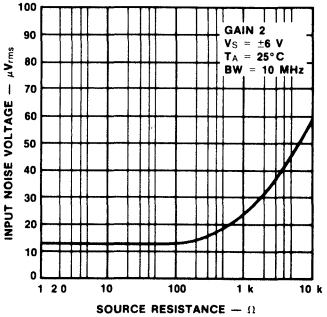
Output Voltage Swing vs Load Resistance



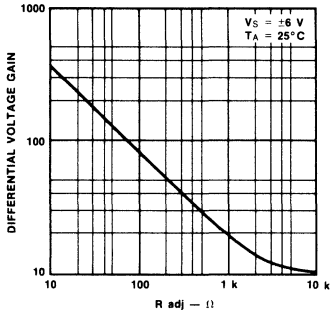
Gain Versus Frequency vs Supply Voltage



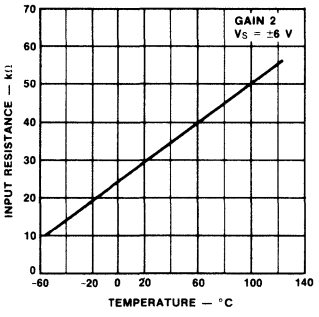
Input Noise Voltage vs Source Resistance



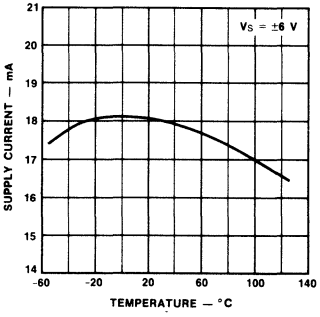
Voltage Gain vs R_{ADJ}



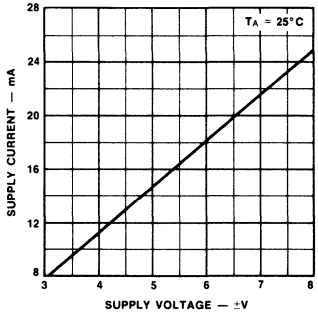
Input Resistance vs Temperature



Supply Current vs Temperature



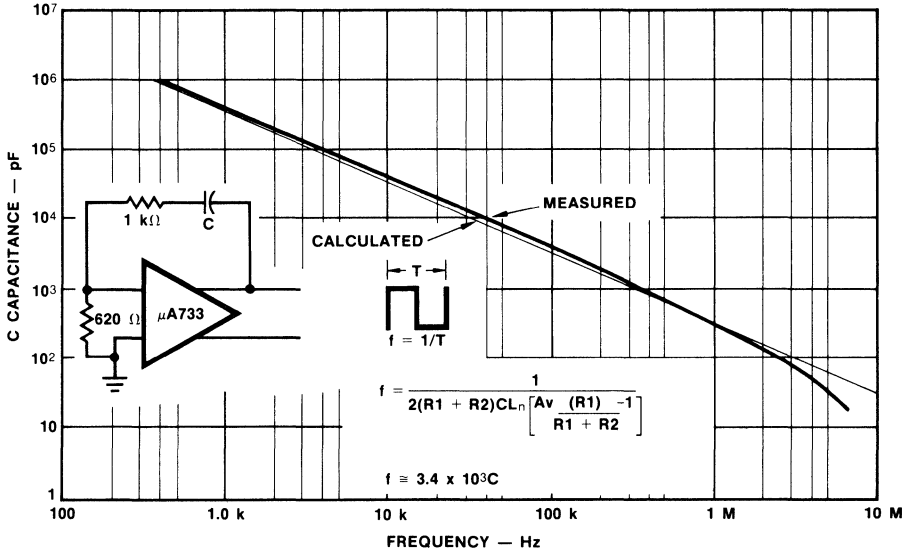
Supply Current vs Supply Voltage



9

Typical Applications

Oscillator Frequency for Various Capacitor Values



FAIRCHILD
A Schlumberger Company

μA757 Gain-Controlled IF Amplifier

Special Function Products

Description

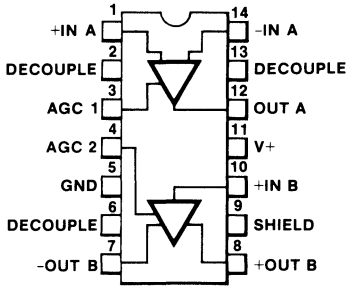
The μA757 is a monolithic high performance, Gain Controlled IF Amplifier constructed using the Fairchild Planar epitaxial process. The amplifier contains two different sections which may be operated independently, or in cascade, from audio frequencies to 25 MHz. The μA757 is intended primarily as a high gain controlled, intermediate frequency amplifier in AM or FM communications receivers. It also has excellent performance when operated in FM receivers as a limiting amplifier.

- **70 dB GAIN AT 10.7 MHz**
- **70 dB AGC RANGE AT 10.7 MHz**
- **300 mV INPUT SIGNAL CAPABILITY**
- **CONSTANT I/O IMPEDANCE WITH AGC**
- **STABLE GAIN WITH SUPPLY VOLTAGE AND TEMPERATURE AT ALL LEVELS OF GAIN REDUCTION**

Absolute Maximum Ratings

Supply Voltage	+15 V
Voltage at any Output Terminal	+24 V
Voltage at either AGC Terminal Note 1	±12 V
Differential Voltage at either Input (Pins 1 and 14, Pins 2 and 10)	±5 V
Internal Power Dissipation Note 2	670 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Pin Temperature (Soldering, 60 s)	300°C

Connection Diagram
14-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA757C	Ceramic DIP	6A	μA757DC

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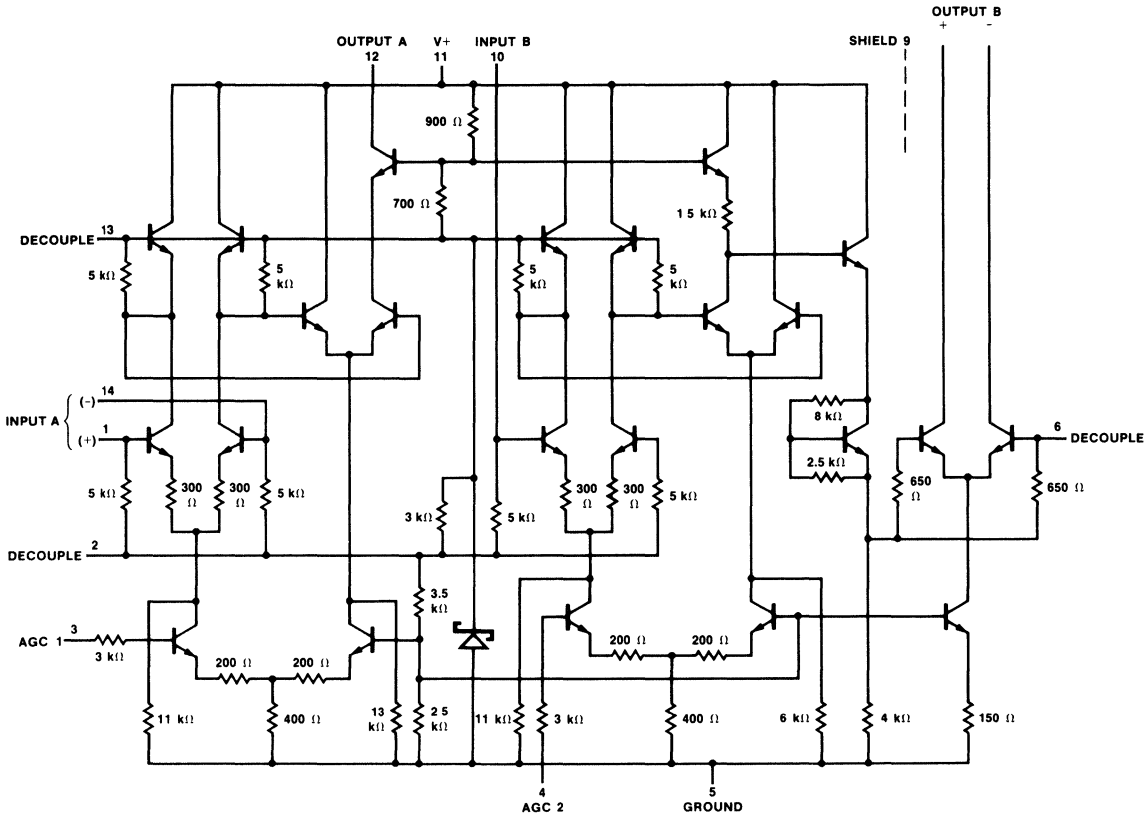
Notes

1. For supply voltages less than +12 V, the absolute maximum voltage at either AGC terminal is equal to the supply voltage.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C.

Equivalent Circuit



μA757
Electrical Characteristics V+ = +12 V, T_A = 25°C, unless otherwise specified

Characteristic	Condition	Test Circuit	Min	Typ	Max	Min	Typ	Max	Unit
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V $V_{AGC\ 1,2}$ = +3.0 V	1		13 17	17 20		14 18	17 22	mA mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8 V $V_{AGC\ 1,2}$ = +3.0 V	1		170 200	210 240		170 220	210 270	mW mW
Voltage Gain at no Reduction	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz $V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2 2	65 60	74 70		65 60	74 70		dB dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz $V_{AGC\ 1,2}$ = +1.7 V, f = 10.7 MHz	2 2	20	39 37	46	20	39 37	46	dB dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz $V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2 2		2.0 1.0	10 8		2.0 1.0	10 8	dB dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		15	50		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		50			50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2		0.5			0.5		mV
Intermodulation Products	Two-tone signal f_1 = 500 kHz, e_1 = 100 mV f_2 = 510 kHz, e_2 = 100 mV I_{OUT} = 1 mA p-p	2		−50			−50		dB
Section 1									
Input Resistance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz $V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz		3.0	5.0 4.5		3.0	5.0 4.5		kΩ kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz $V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.5 2.2			2.5 2.2		pF pF
Output Resistance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz $V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			100 100			100 100		kΩ kΩ
Output Capacitance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz $V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.6 2.2			2.6 2.2		pF pF
Forward Transadmittance	$V_{AGC\ 1}$ = +0.8 V, f = 500 kHz $V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			14 13			14 13		mmho mmho
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.25	0.4		0.25	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.0		8.0	9.0	V
Noise Figure	R_S = 1.0 kΩ, f = 10.7 MHz R_S = 1.0 kΩ, f = 500 kHz			8.0 8.0			8.0 8.0		dB dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, f_c = 500 kHz Interfering signal, f_i = 510 kHz I_{OUT} = 0.5 mAp-p, $V_{AGC\ 1}$ = +0.8 V			15			15		mV

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Section 2
Electrical Characteristics (Cont.) $V+ = +12$ V, $T_A = 25°C$, unless otherwise specified

Characteristic	Condition	Test Circuit	Min	Typ	Max	Min	Typ	Max	Unit
Input Resistance	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz $V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz		3.0	5.0 4.5		3.0	5.0 4.5		kΩ kΩ
Input Capacitance	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz $V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.5 2.2			2.5 2.2		pF pF
Output Resistance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz $V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			26 20			26 20		kΩ kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz $V_{AGC\ 2} = +3.0$ V, f = 10.7 MHz			2.2 2.5			2.2 2.5		pF pF
Forward Transadmittance	$V_{AGC\ 2} = +0.8$ V, f = 500 kHz $V_{AGC\ 2} = +0.8$ V, f = 10.7 MHz			440 280			440 280		mmho mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.7	2.4	3.5	1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		3.8	4.8	7.0	3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC\ 2} = +3.0$ V			5.0	6.0		5.0	6.0	V
Power Supply Sensitivity	$V_S = 12$ V to 15 V 0 dB Gain Reduction 30 dB Gain Reduction 60 dB Gain Reduction			 0.5 0.8 1.0			 0.5 0.8 1.0		 dB/V dB/V dB/V

μA757
Electrical Characteristics (Cont.) $V+ = +12$ V, $T_A = +125°C$, unless otherwise specified

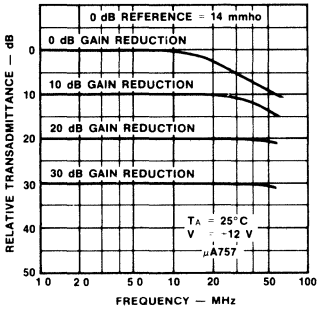
Characteristic	Condition	Test Circuit	Min	Typ	Max	Unit
Supply Current	$V_{AGC\ 1,2} = +0.8$ V $V_{AGC\ 1,2} = +3.0$ V	1		14 17	17 20	mA mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8$ V $V_{AGC\ 1,2} = +3.0$ V	1		170 200	210 240	mW mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8$ V, f = 500 kHz $V_{AGC\ 1,2} = +0.8$ V, f = 10.7 MHz	2 2	55	71 62		dB dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2		35		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, f = 500 kHz $V_{AGC\ 1,2} = +3.0$ V, f = 10.7 MHz	2 2		2.0 −1.0	15	dB dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		15	50	μA
Section 1						
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1$ mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.4	V
Section 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.7	2.8	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		3.8	5.6	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC\ 2} = +3.0$ V			6.0	7.0	V

μA757
Electrical Characteristics V+ = +12 V, T_A = −55°C, unless otherwise specified

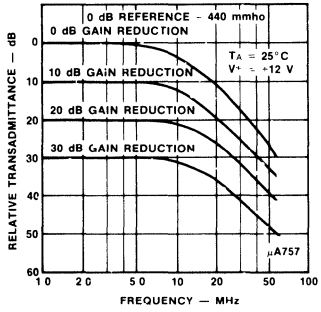
Characteristic	Condition	Test Circuit	Min	Typ	Max	Unit
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V $V_{AGC\ 1,2}$ = +3.0 V	1		10 14	17 20	mA mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8 V $V_{AGC\ 1,2}$ = +3.0 V	1		120 170	210 240	mW mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz $V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2 2	55	68 64		dB dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		28		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz $V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2 2		2.0 −3.0	15	dB dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		30	70	μA
Section 1						
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.0	V
Section 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.0	1.7	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz Output in full limiting		2.3	3.4	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			4.0	6.0	V

Typical Performance Curves

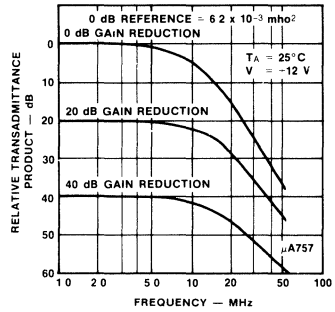
Section 1 Forward Transadmittance vs Frequency



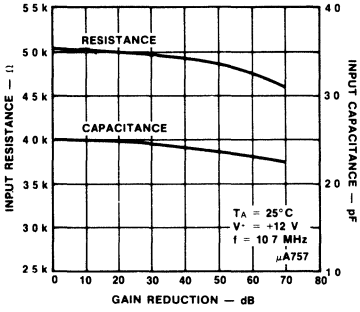
Section 2 Forward Transadmittance vs Frequency



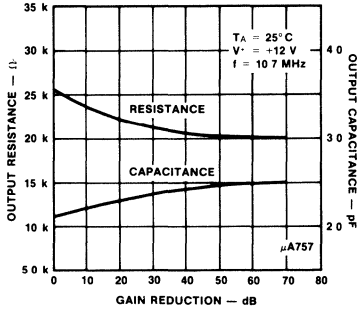
Product of Sections 1 and 2 Forward Transadmittance vs Frequency



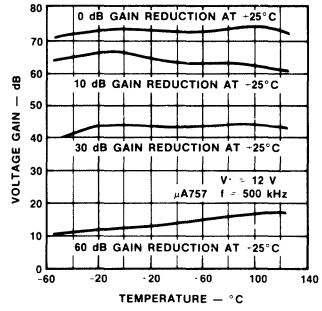
Section 1 and 2 Input Resistance and Capacitance vs Gain Reduction



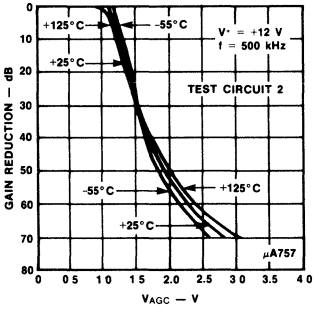
Section 2 Output Resistance and Capacitance vs Gain Reduction



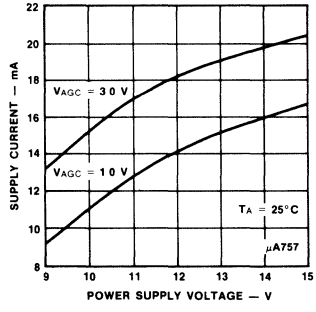
Voltage Gain vs Temperature



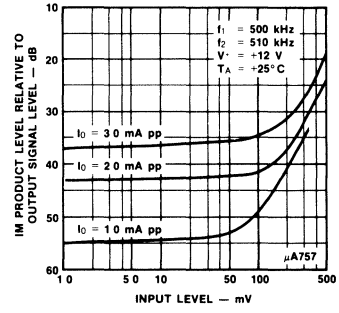
Gain Reduction vs Gain Control Voltage



Power Supply Current vs Supply Voltage

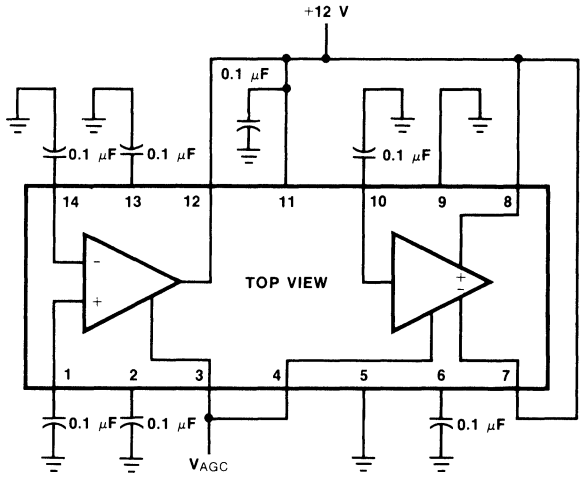


Two Tone IM Distortion Products vs Input Signal Level



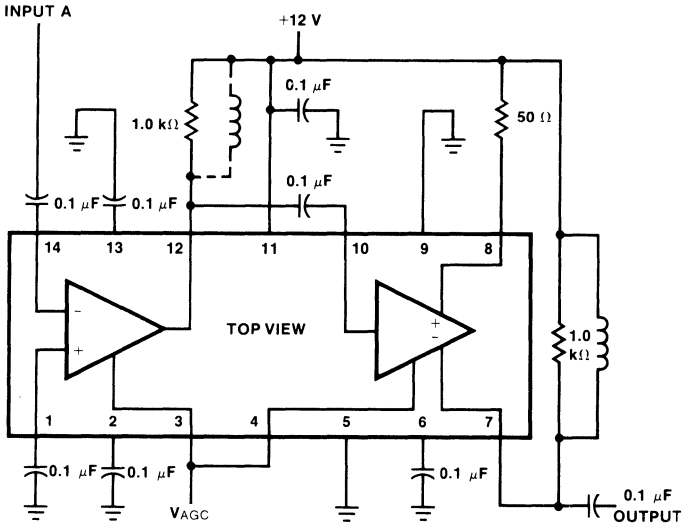
Test Circuit

Test Circuit 1 (Note)



Note
For 10 7 MHz measurements, interstage capacitance and Section 2 output capacitance are tuned out. Pin 9 should be connected to GND.

Test Circuit 2 (Note)



Note
Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C.

FAIRCHILD

A Schlumberger Company

μA2240 Programmable Timer/Counter

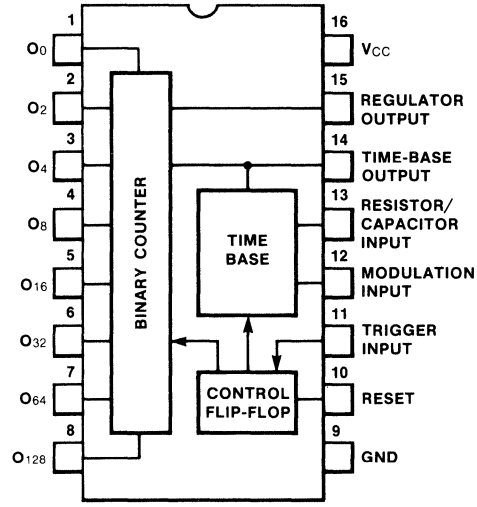
Special Function Products

Description

The μA2240 Programmable Timer/Counter is a monolithic controller capable of producing accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time-base oscillator, programmable 8-bit counter and control flip-flop. An external resistor capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, 255 frequencies or pulse patterns can be generated from a single RC network. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and DTL compatible for easy interface with digital system. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

- **ACCURATE TIMING FROM MICROSECONDS TO DAYS**
- **PROGRAMMABLE DELAYS FROM 1 RC TO 255 RC**
- **TTL, DTL AND CMOS COMPATIBLE OUTPUTS**
- **TIMING DIRECTLY PROPORTIONAL TO RC TIME CONSTANT**
- **HIGH ACCURACY 0.5%**
- **EXTERNAL SYNC AND MODULATION CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE**
- **EXCELLENT SUPPLY VOLTAGE REJECTION**

Connection Diagram
16-Pin DIP

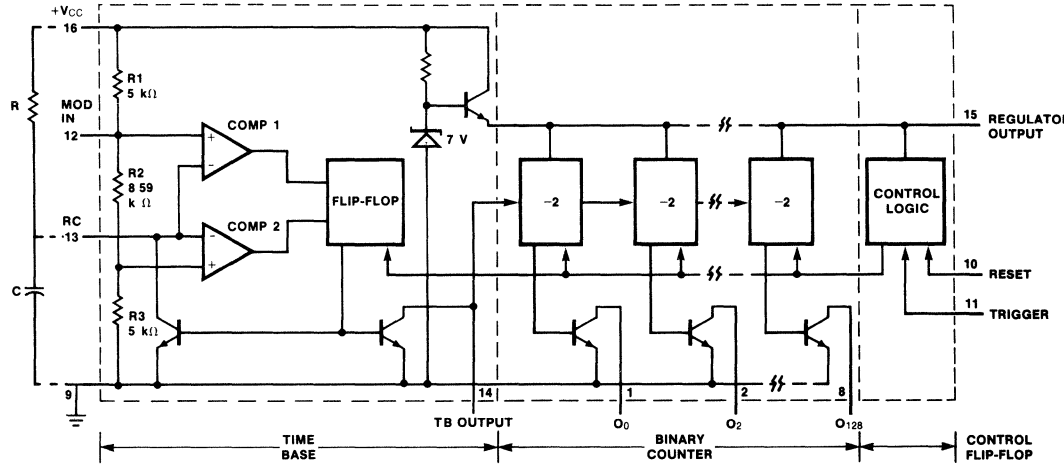


(Top View)

Order Information

Type	Package	Code	Part No.
μA2240	Ceramic DIP	7B	μA2240DM
μA2240C	Ceramic DIP	7B	μA2240DC
μA2240C	Molded DIP	9B	μA2240PC

Block Diagram



Absolute Maximum Ratings

Supply Voltage	18 V
Output Current	10 mA
Output Voltage	18 V
Regulator Output Current	5 mA
Maximum Power Dissipation, Note	
Package Code D (Ceramic)	750 mW
Code P (Molded)	650 mW
Operating Temperature Range	
Military (μA2240)	−55°C to +125°C
Commercial (μA2240C)	0°C to 70°C
Pin Temperature (Soldering)	
Ceramic DIP (60 s)	300°C
Molded DIP (10 s)	260°C

Note

Above 25°C ambient derate linearly at 6 2 mW/°C for Package Code D and at 5 3 mW/°C for Package Code P

Functional Description

(*Figure 1* and Block Diagram, page 1)
When power is applied to the μA2240 with no trigger or reset inputs, the circuit starts with all outputs HIGH. Application of a positive-going trigger pulse to TRIG, Pin 11, initiates the timing cycle. The Trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive-going reset pulse is applied to R, pin 10.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a Reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.

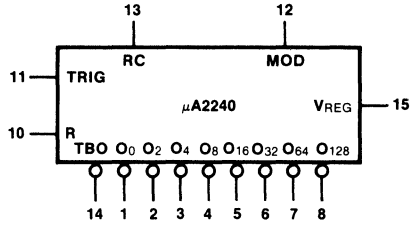
In most timing applications, one or more of the counter outputs are connected to the Reset terminal with S1 closed (*Figure 3*). The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the Reset terminal (switch S1 open), the circuit operates in an astable or free-running mode, following to a trigger input.

Important Operating Information

- Ground connection is pin 9.
- Reset R (pin 10) sets all outputs HIGH.
- Trigger TRIG (pin 11) sets all outputs LOW.
- Time-base TBO (pin 14) can be disabled by bringing the RC input (pin 13) LOW via a 1 k resistor.
- Normal Time-base Output TBO (pin 14) is a negative-going pulse greater than 500 ns.

  Note: Under the conditions of high supply voltages ($V_{CC} > 7$ V) and low values of timing capacitor ($C < 0.1$ μF), the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from TBO (pin 14) to ground (pin 9).
- Reset (pin 10) stops the time-base oscillator.
- Outputs $O_0 \ldots O_{128}$ (pins 1-8) sink 2 mA current with $V_{OL} \leq 0.4$ V.
- For use with external clock, minimum clock pulse amplitude should be 3 V, with greater than 1 μs pulse duration.

Fig. 1 Logic Symbol



V_{CC} = Pin 16
GND = Pin 9

Fig. 2 Timing Diagram of Output Waveforms

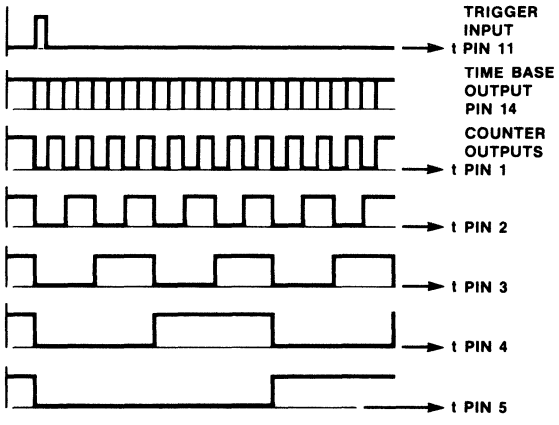


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Fig. 3 Basic Circuit Connection for Timing Applications
Monostable: S1 Closed Astable: S1 Open

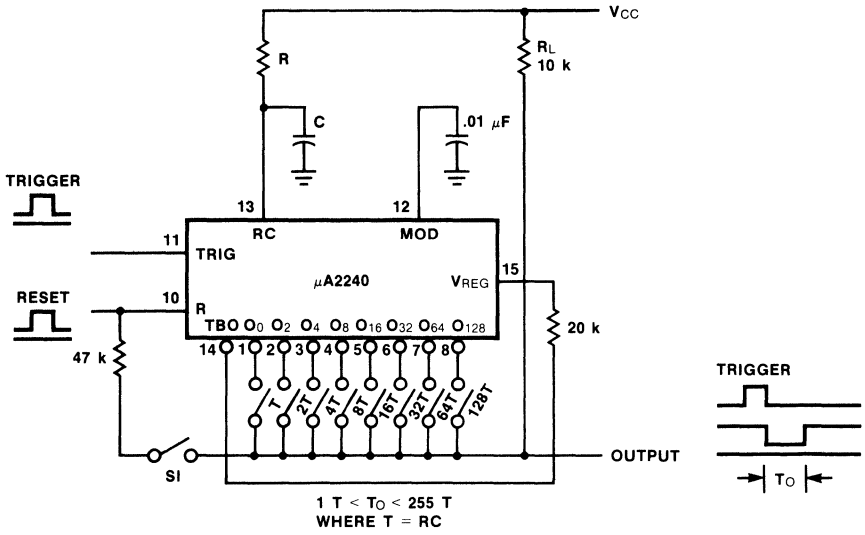


Fig. 4 Operation with External Sync Signal

Circuit Controls

Counter Outputs ($O_0 \ldots O_{128}$, pins 1 thru 8)
The binary counter outputs are buffered open-collector type stages, as shown in the block diagram. Each output is capable of sinking 2 mA at 0.4 V V_{OL}. In the Reset condition, all the counter outputs are HIGH or in the non-conducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2*. The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the programming section.

Reset and Trigger Inputs (R and TRIG, pins 10 and 11)
The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11 respectively. The threshold level for these controls is approximately two diode drops (≈ 1.4 V) above ground. Minimum pulse widths for reset and trigger inputs are shown in the Performance Curves. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, pin 12)
The oscillator time-base period, T, can be modulated by applying a dc voltage to MOD, pin 12 (see Performance Curves). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, pin 12, as shown in *Figure 4*. Recommended sync pulse widths and amplitudes are also given.

The time base can be synchronized by setting the time-base period T to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m)$$

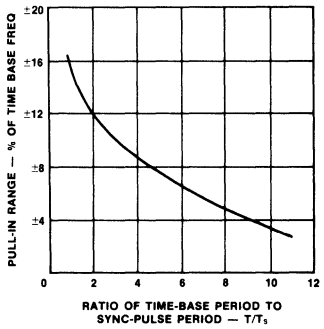
where

$$m \text{ is an integer, } 1 \leq m \leq 10$$

Figure 5 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

RC Terminal (pin 13)
The time-base period T is determined by the external RC network connected to RC, pin 13. When the time base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC.

Fig. 5 Typical Pull-in Range for Harmonic Synchronization

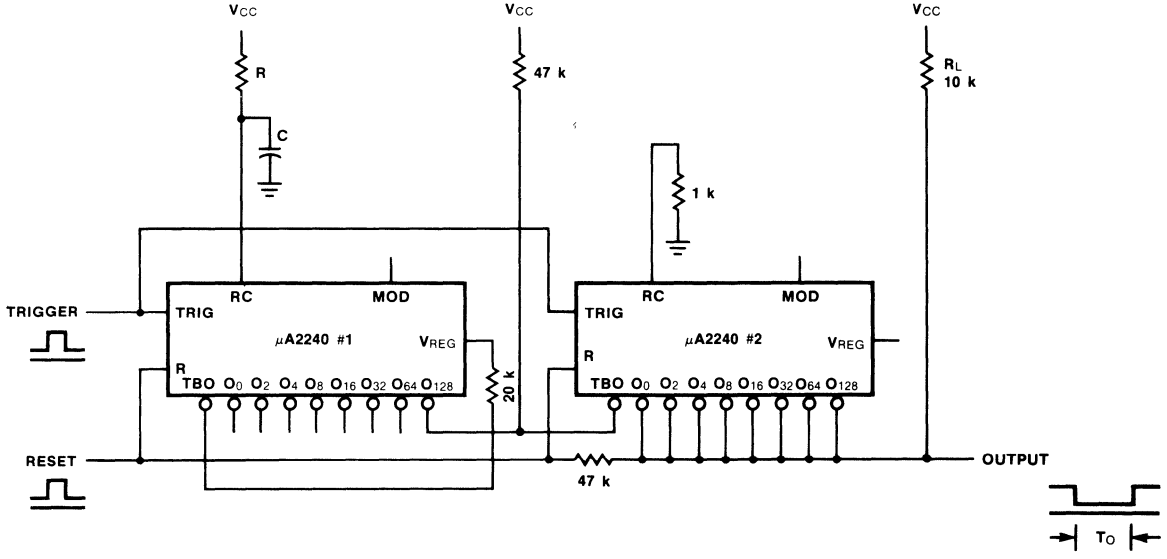


Time-Base Output (TBO, pin 14)
The time-base output is an open-collector type stage as shown in the block diagram, and requires a 20 kΩ pull-up resistor to pin 15 for proper circuit operation. In the Reset state, the time-base output is HIGH. After triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of *Figure 2*. The time-base output is internally connected to the binary-counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative-going edge of the timing or clock pulses generated at TBO, pin 14. The trigger threshold for the counter section is ≈ +1.4 V. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

When using high supply voltages (V_{CC} > 7 V) and a small-value timing capacitor (C < 0.1 μF), the pulse width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from pin 14 to ground.

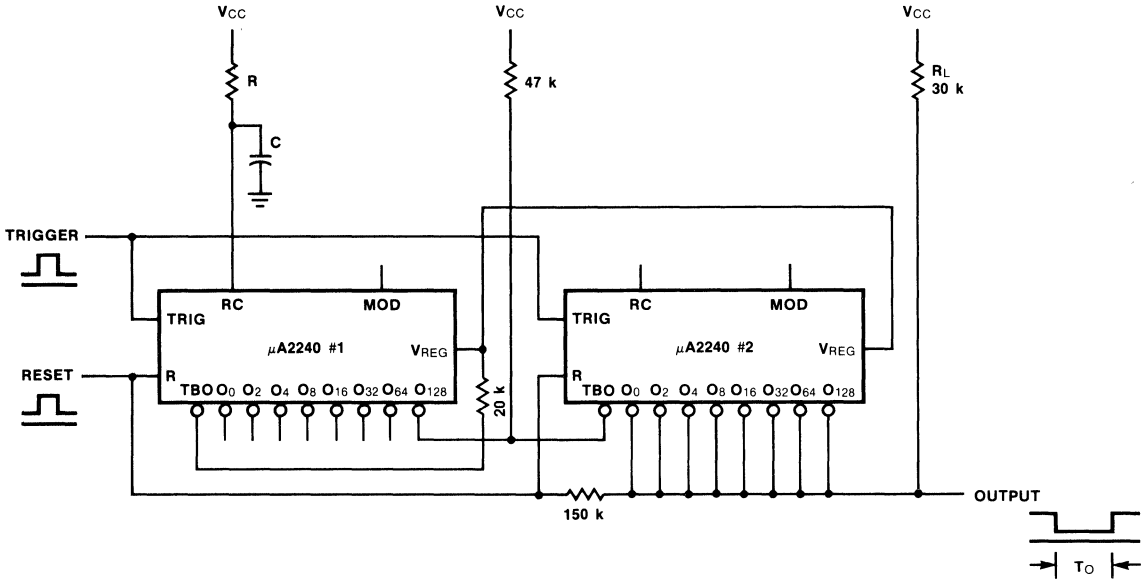
Regular Output (V_{REG}, pin 15)
The regulator output V_{REG} is used internally to drive the binary counter and the control logic. This terminal can also be used as a supply to additional μA2240 circuits when several timer circuits are cascaded (see *Figure 7*) to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time-base, pin 15 should be shorted to pin 16.

Fig. 6 Cascaded Operation for Long Delays



V_{CC} = Pin 16
GND = Pin 9

Fig. 7 Low Power Operation of Cascaded Timers



V_{CC} = Pin 16
GND = Pin 9

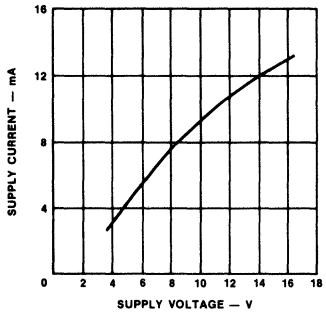
μA2240 and μA2240C
Electrical Characteristics V_{CC} = 5 V, T_A = 25°C, R = 10 kΩ, C = 0.1 μF, unless otherwise noted

Characteristic	Condition	μA2240 Min	μA2240 Typ	μA2240 Max	μA2240C Min	μA2240C Typ	μA2240C Max	Unit
General Characteristics								
Supply Voltage	For $V_{CC} \leq$ 4.5 V, Short Pin 15 to Pin 16	4.0		15	4.0		15	V
Supply Current								
Total Circuit	V_{CC} = 5 V, V_{TR} = 0, V_{RS} = 5 V		3.5	6.0		4.0	7.0	mA
	V_{CC} = 15 V, V_{TR} = 0, V_{RS} = 5 V		12	16		13	18	mA
Counter Only			1			1.5		mA
Regulator Output, V_{Reg}	Measured at Pin 15, V_{CC} = 5 V	4.1	4.4		3.9	4.4		V
	V_{CC} = 15 V	6.0	6.3	6.6	5.8	6.3	6.8	V
Time Base Section								
Timing Accuracy	V_{RS} = 0, V_{TR} = 5 V (Note 1)		0.5	2.0		5.0	5.0	%
Temperature Drift	V_{CC} = 5 V, 0°C $\leq T_J \leq$ 75°C		150	300		200		ppm/°C
	V_{CC} = 15 V, 0°C $\leq T_J \leq$ 75°C		80			80		ppm/°C
Supply Drift	$V_{CC} \geq$ 8 V (See Curves)		0.05	0.2		0.08	0.3	%/V
Max Frequency	R = 1 kΩ, C = 0.007 μF	100	130			130		kHz
Modulation Voltage Level	Measured at Pin 12							
	V_{CC} = 5 V	3.00	3.5	4.0	2.80	3.50	4.20	V
	V_{CC} = 15 V		10.5			10.5		V
Recommended Range of Timing Components	(See Performance Curves)							
Timing Resistor, R		0.001		10	0.001		10	MΩ
Timing Capacitor, C		0.007		1000	0.01		1000	μF
Trigger/Reset Controls								
Trigger	Measured at Pin 11, V_{RS} = 0							
Trigger Threshold			1.4	2.0		1.4	2.0	V
Trigger Current	V_{RS} = 0, V_{TR} = 2 V		8.0			10		μA
Impedance			25			25		kΩ
Response Time	Note 2		1.0			1.0		μs
Reset	Measured at Pin 10, V_{TR} = 0							
Reset Threshold			1.4	2.0		1.4	2.0	V
Reset Current	V_{TR} = 0, V_{RS} = 2 V		8.0			10		μA
Impedance			25			25		kΩ
Response Time	Note 2		0.8			0.8		μs
Counter Section								
Max Toggle Rate	V_{RS} = 0, V_{TR} = 5 V, Measured at Pin 14	0.8	1.5			1.5		MHz
Input Impedance			20			20		kΩ
Input Threshold		1.0	1.4		1.0	1.4		V
Output	Measured at Pins 1 through 8							
Rise Time	R_L = 3 kΩ, C_L = 10 pF		180			180		ns
Fall Time			180			180		ns
Sink Current	$V_{OL} \leq$ 0.4 V	3.0	5.0		2.0	4.0		mA
Leakage Current	V_{OH} = 15 V		0.01	8.0		0.01	15	μA

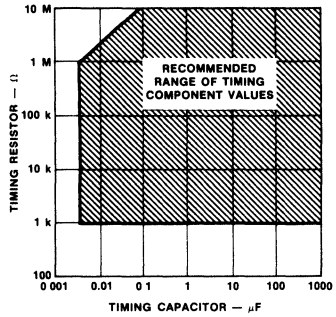
Notes
1. Timing error solely introduced by μA2240, measured as % of ideal time base period of T = 1.00 RC.
2. Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

Typical Performance Curves

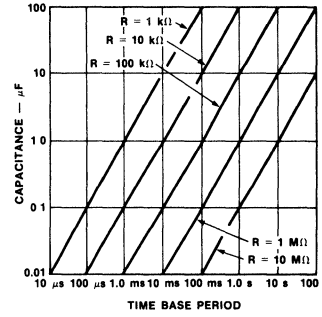
Supply Current vs Supply Voltage in Reset Condition



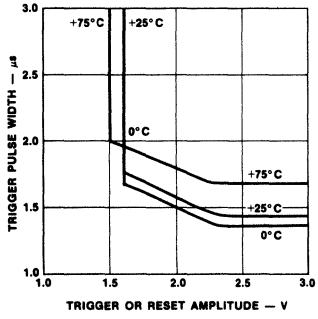
Recommended Range of Timing Component Values



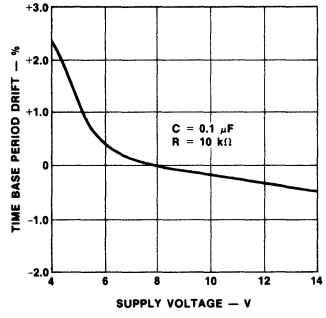
Time Base Period vs External RC



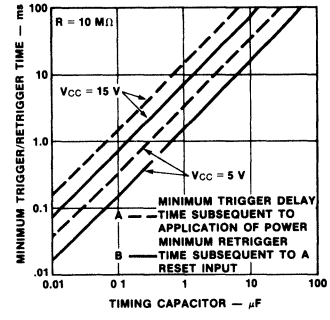
Minimum Trigger Pulse Width vs Trigger and Reset Amplitude



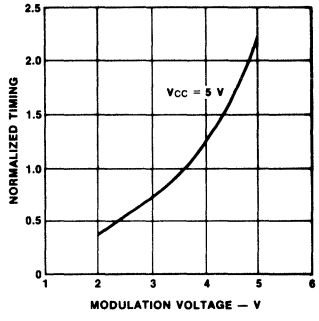
Time Base Period Drift vs Supply Voltage



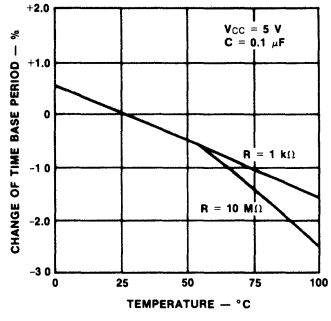
Minimum Trigger/ Retrigger Timing vs Timing Capacitor



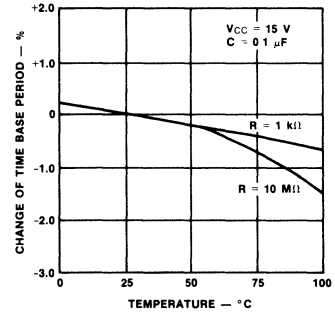
Normalized Change in Time Base Period vs Modulation Voltage



Time Base Period vs Temperature



Time Base Period vs Temperature



Monostable Operation

Precision Timing

In precision timing applications, the μA2240 is used in its monostable or self-resetting mode. The generalized circuit connection for this application is shown in *Figure 3*. The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration, T_O, and then returns to the HIGH state. The duration of the timing cycle T_O is given as:

$$T_O = nT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at RC pin 13 (see Performance Curves) and n is an integer in the range of $1 \leq n \leq 255$ as determined by the combination of counter outputs $O_0 \ldots O_{128}$, pins 1 through 8, connected to the output bus.

Counter-Output Programming

The binary-counter outputs, $O_0 \ldots O_{128}$, pins 1 through 8 are open-collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each counter output can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32 T. Similarly, if pins 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)\ T = 49\ T$. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1\ T \leq T_O \leq 255\ T$.

Ultra Long Time-Delay Application

Two μA2240 units can be cascaded as shown in *Figure 6* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}536$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the Reset and the Trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 7*. In this case, the V_{CC} terminal (pin 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (pin 15) of both units together.

Astable Operation

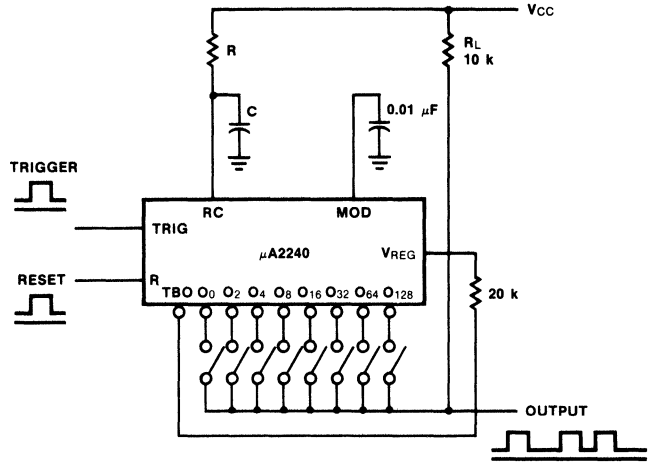
The μA2240 can be operated in its astable or free-running mode by disconnecting the Reset terminal (pin 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free-running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its Reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely. In astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Binary Pattern Generation

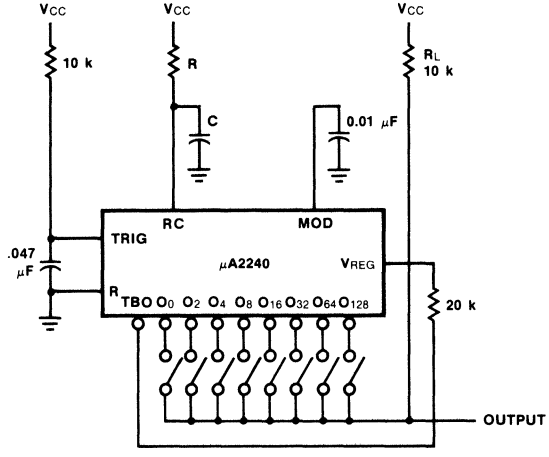
In astable operation, as shown in *Figure 8,* the output of the μA2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2* which shows the phase relations between the counter outputs. *Figures 10* and *11* show some of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

Fig. 8 Operation with Trigger and Reset Inputs



V_{CC} = Pin 16
GND = Pin 9

Fig. 9 Free-Running or Continuous Operation



V_{CC} = Pin 16
GND = Pin 9

Fig. 10 Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

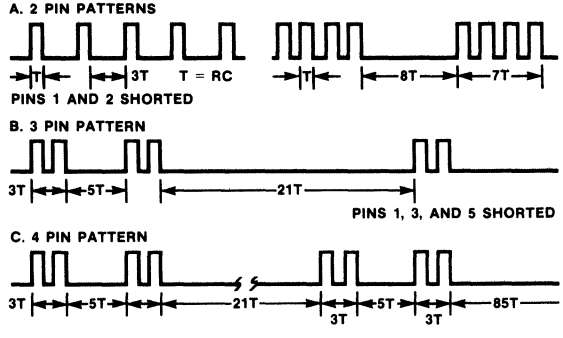
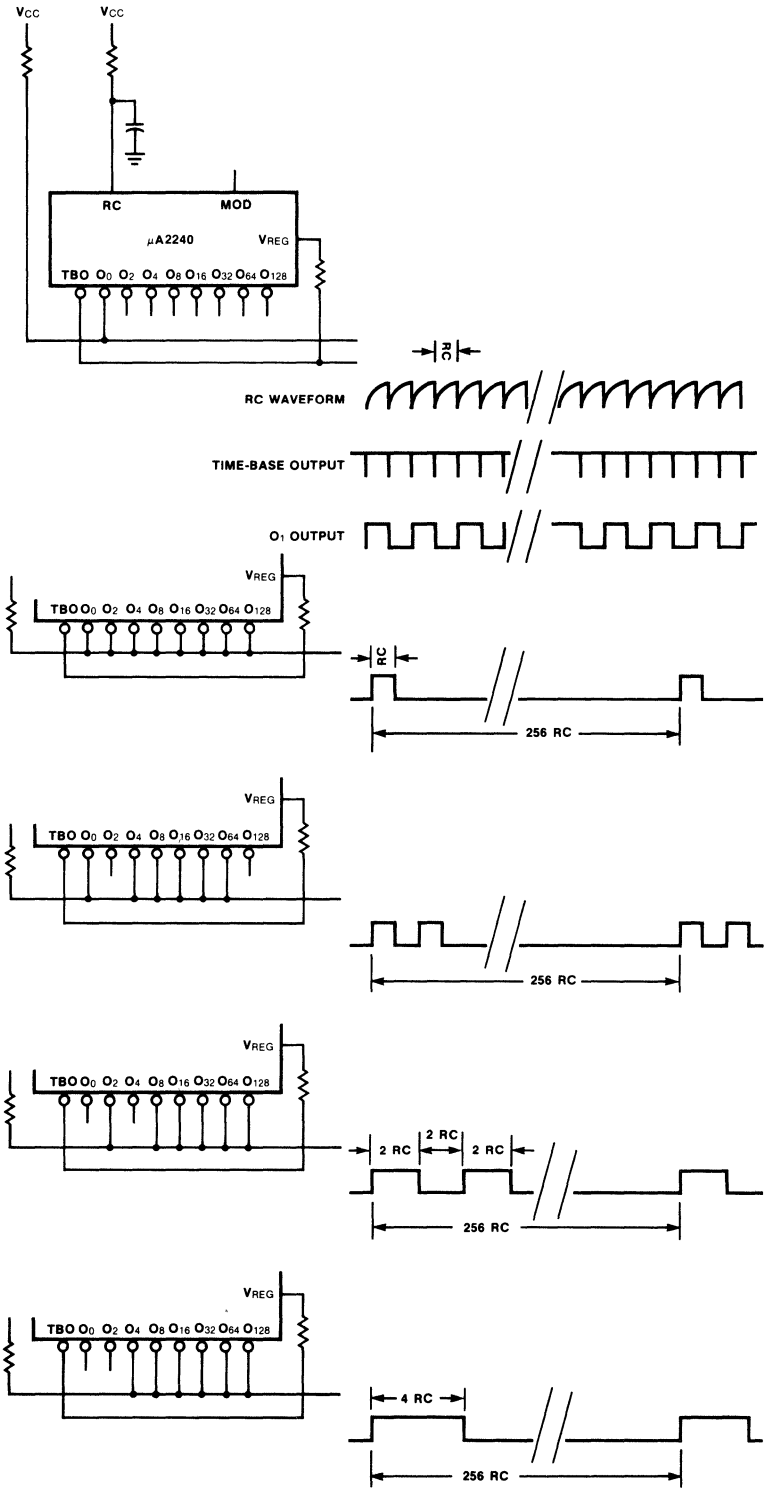


Fig. 11 Continuous Free-run Operation Examples of Output



V_{CC} = Pin 16
GND = Pin 9

9

FAIRCHILD

A Schlumberger Company

μA3086 General-Purpose Transistor Array

Special Function Products

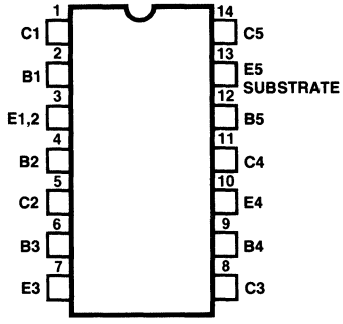
Description

μA3086 contains a differentially connected pair and three individually isolated transistors. The part is designed for general-purpose, low-power applications for consumer and industrial applications.

- **LOW INPUT OFFSET VOLTAGE**
- **WIDEBAND OPERATION**
- **LOW NOISE**
- **MATCHED DIFFERENTIAL AMPLIFIER**

Absolute Maximum Ratings	**Each Transistor**
Power Dissipation (Note 1)	
At T_A = 25°C	300 mW
At T_A = 25°C to 55°C	300 mW
At T_A = 25°C	750 mW (Note 2)
At T_A = 25°C to 55°C	750 mW (Note 2)
Voltages and Currents	
Collector-to-Emitter Voltage, V_{CEO}	15 V
Collector-to-Base Voltage, V_{CBO}	20 V
Collector-to-Substrate Voltage, V_{CIO} (Note 3)	20 V
Emitter-to-Base Voltage, V_{EBO}	5 V
Collector Current, I_C	50 mA
Temperature Range	
Operating Temperature	−40°C to +85°C
Storage Temperature	−55°C to +125°C
Pin Temperature (Soldering)	
Ceramic DIP (60 s)	300°C
Molded DIP (10 s)	260°C

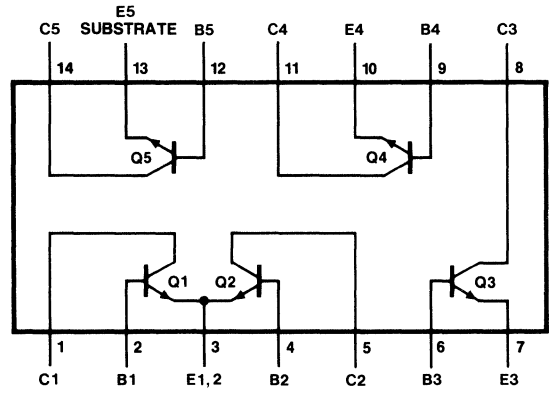
Connection Diagram
14-Pin DIP



Order Information

Type	**Package**	**Code**	**Part No.**
μA3086	Molded DIP	9A	μA3086PC
μA3086	Ceramic DIP	6A	μA3086DC

Logic Diagram



Notes

1. Derate at 5 mW/°C for $T_A > 85°C$.
2. Total package.
3. Substrate must be connected to the most negative voltage to maintain normal operation.

μA3086
Electrical Characteristics $T_A = 25°C$ unless otherwise specified

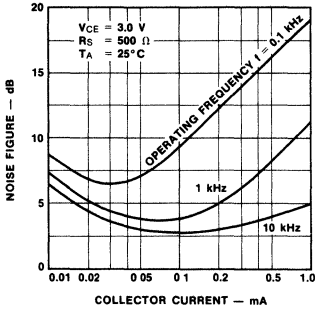
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$	20	60		V
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	15	24		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$I_C = 10\ \mu A$, $I_C = 0$	20	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	$I_E = 10\ \mu A$, $I_C = 0$	5.0	7.0		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 10$ V, $I_E = 0$		0.002	100	nA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 10$ V, $I_B = 0$		See Curve	5.0	μA
h_{FE}	Static Forward Current-Transfer Ratio (Static Beta)	$V_{CE} = 3$ V; $I_C = 10$ mA $I_C = 1$ mA $I_C = 10\ \mu A$	40	100 100 54		
	Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{IO1}\text{-}I_{IO2}\rvert$	$V_{CE} = 3$ V, $I_C = 1$ mA		0.3		μA
V_{BE}	Base-to-Emitter Voltage	$V_{CE} = 3$ V; $I_E = 1$ mA $I_E = 10$ mA		0.715 0.800		V
	Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1}\text{-}V_{BE_2}\rvert$	$V_{CE} = 3$ V, $I_C = 1$ mA		0.45		mV
	Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3}\text{-}V_{BE_4}\rvert$, $\lvert V_{BE_4}\text{-}V_{BE_5}\rvert$, $\lvert V_{BE_5}\text{-}V_{BE_3}\rvert$	$V_{CE} = 3$ V, $I_C = 1$ mA		0.45		mV
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient of Base-to-Emitter Voltage	$V_{CE} = 3$ V, $I_C = 1$ mA		−1.9		mV/°C
$V_{CE(sat)}$	Collector-to-Emitter Saturation Voltage	$I_B = 1$ mA, $I_C = 10$ mA		0.23		V
$\frac{\lvert\Delta V_{10}\rvert}{\Delta T}$	Temperature Coefficient of Magnitude of Input-Offset Voltage	$V_{CE} = 3$ V, $I_C = 1$ mA		1.1		μV/°C
NF	Low Frequency Noise Figure	$f = 1$ kHz, $V_{CE} = 3$ V, $I_C = 100\ \mu A$, $R_S = 1\ k\Omega$		3.25		dB

μA3086
Electrical Characteristics T_A = 25°C unless otherwise specified

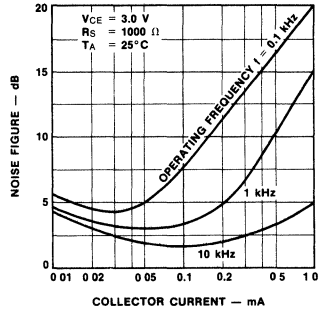
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
	Low Frequency, Small-Signal Equivalent-Circuit Characteristics					
h_{fe}	Forward Current-Transfer Ratio	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA		110		
h_{ie}	Short-Circuit Input Resistance			3.5		kΩ
h_{oe}	Open-Circuit Output Conductance			15.6		μmho
h_{re}	Open-Circuit Reverse Voltage-Transfer Ratio			1.8×10^{-4}		
Y_{fe}	Admittance Characteristics: Forward Transfer Admittance	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA		31 − j1.5		
Y_{ie}	Input Admittance			0.3 + j0.04		
Y_{oe}	Output Admittance			0.001 + j0.03		
Y_{re}	Reverse Transfer Admittance			See Curve		
f_T	Gain-Bandwidth Product	V_{CE} = 3 V, I_C = 3 mA	300	550		MHz
C_{EB}	Emitter-to-Base Capacitance	V_{EB} = 3 V, I_E = 0		0.6		pF
C_{CB}	Collector-to-Base Capacitance	V_{CB} = 3 V, I_C = 0		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	V_{CS} = 3 V, I_C = 0		2.8		pF

Typical Performance Curves

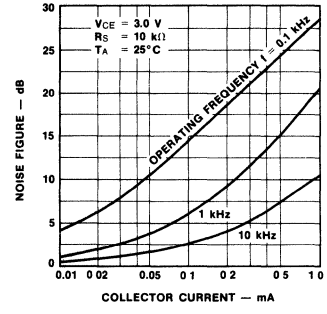
Noise Figure vs Collector Current



Noise Figure vs Collector Current

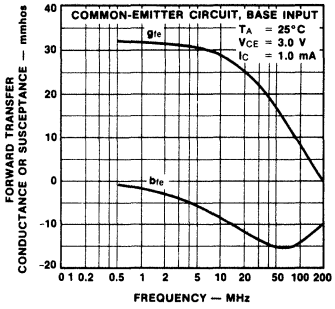


Noise Figure vs Collector Current

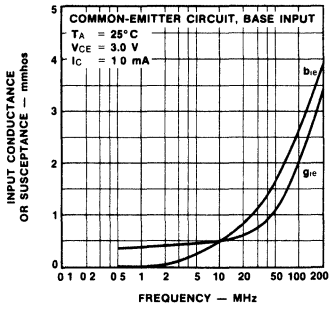


Typical Performance Curves (Cont.)

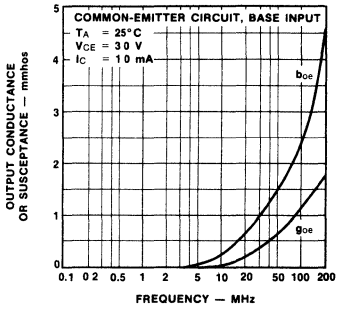
Forward Transfer Admittance vs Frequency



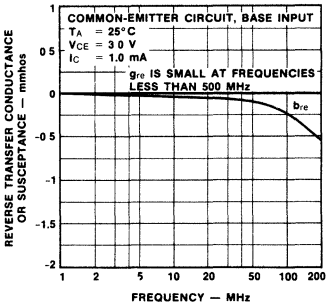
Input Admittance vs Frequency



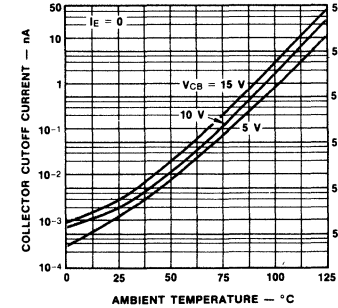
Output Admittance vs Frequency



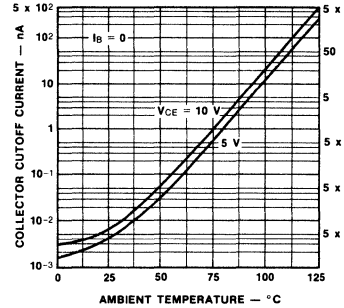
Reverse Transfer Admittance vs Frequency



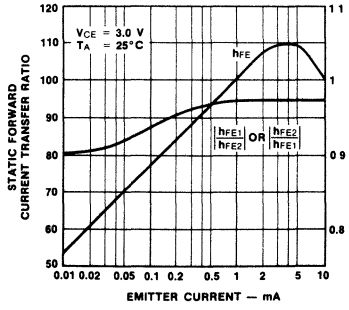
Collector-to-Base Cutoff Current vs Ambient Temperature for Each Transistor



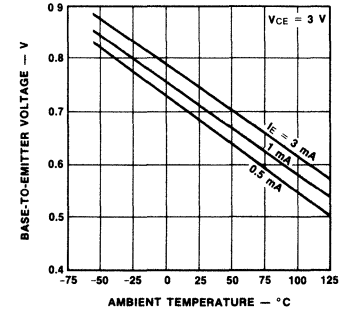
Collector-to-Emitter Cutoff Current vs Ambient Temperature for Each Transistor



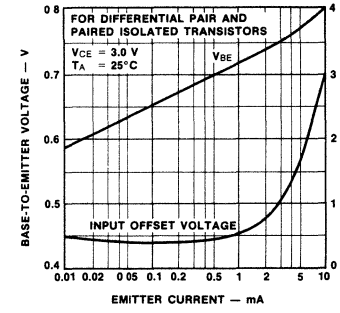
Static Forward Current-Transfer and Beta Ratio for Transistors Q1, Q2 vs Emitter Current



Base-to-Emitter Voltage Characteristic vs Ambient Temperature for Each Transistor



Static Base-to-Emitter Voltage and Input Offset Voltage vs Emitter Current



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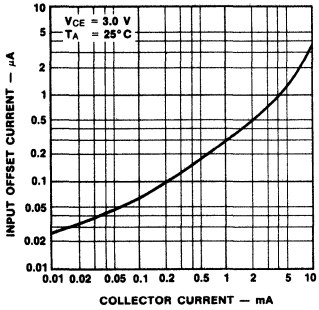
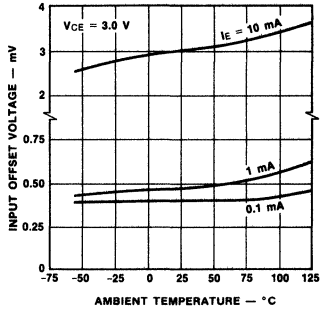
Typical Performance Curves (Cont.)

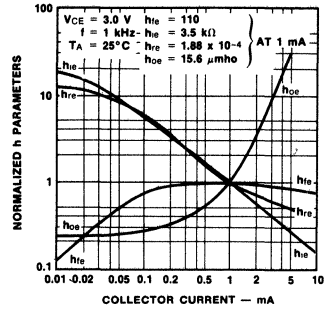
Input Offset Current for Matched Transistor Pair Q1, Q2 vs Collector Current



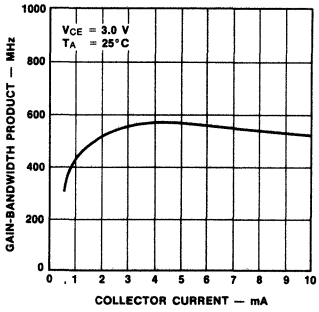
Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Ambient Temperature



Normalized h Parameters vs Collector Current



Gain-Bandwidth Product vs Collector Current



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μA7392
DC Motor Speed Control Circuit

Special Function

Description

The μA7392 is designed for precision, closed-loop, motor speed control systems. It regulates the speed of capstan drive motors in automotive and portable tape players and is useful in a variety of industrial and military control applications, e.g., floppy disc drive systems and data cartridge drive systems. The device is constructed using the Fairchild Planar epitaxial process.

The μA7392 compares actual motor speed to an externally presettable reference voltage. The motor speed is determined by frequency to voltage conversion of the input signal provided by the tachometer generator. The result of the comparison controls the duty cycle of the pulse width modulated switching motor drive output stage to close the system's negative feedback loop.

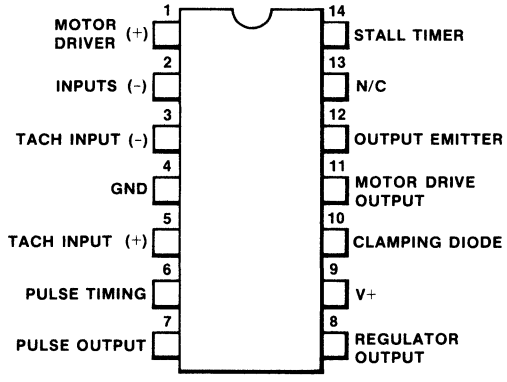
Thermal and over-voltage shutdown are included for self-protection, and a "stall-timer" feature allows the motor to be protected from burn-out during extended mechanical jams.

- **PRECISION PERFORMANCE**
- **HIGH-CURRENT PERFORMANCE**
- **WIDE RANGE TACHOMETER INPUT**
- **THERMAL SHUTDOWN, OVER-VOLTAGE AND STALL PROTECTION**
- **INTERNAL REGULATOR**
- **WIDE SUPPLY VOLTAGE RANGE 6.3 V TO 16 V**

Absolute Maximum Ratings

Supply Voltage (V+), V_9, V_{10}, V_{11}	24 V
Regulator Output Current, I_8	15 mA
Voltage Applied to Pin 6 (Tachometer Pulse Timing)	7 V
Voltage Applied Between Pins 3 and 5 (Tachometer Inputs)	±6 V
Continuous Current through Pins 11 and 12 Motor Drive Output ON	0.3 A
Repetitive Surge Current through Pins 11 and 12 (Motor Drive ON)	1.0 A
Repetitive Surge Current through Pins 10 and 11 (Motor Drive OFF)	0.3 A
Power Dissipation	Internally Limited
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−40°C to +85°C
Pin Temperature (Soldering)	
Ceramic DIP (60 s)	300°C
Molded DIP (10 s)	260°C

Connection Diagram
14-Pin DIP



(Top View)

Order Information

Type	Package	Code	Part No.
μA7392C	Ceramic DIP	6A	μA7392DC
μA7392C	Molded DIP	9A	μA7392PC

Thermal Data
Thermal Resistance, Junction to Ambient
Molded (9A) 70°C/W Typ, 80°C/W Maximum
Ceramic (6A) 100°C/W Typ, 120°C/W Maximum

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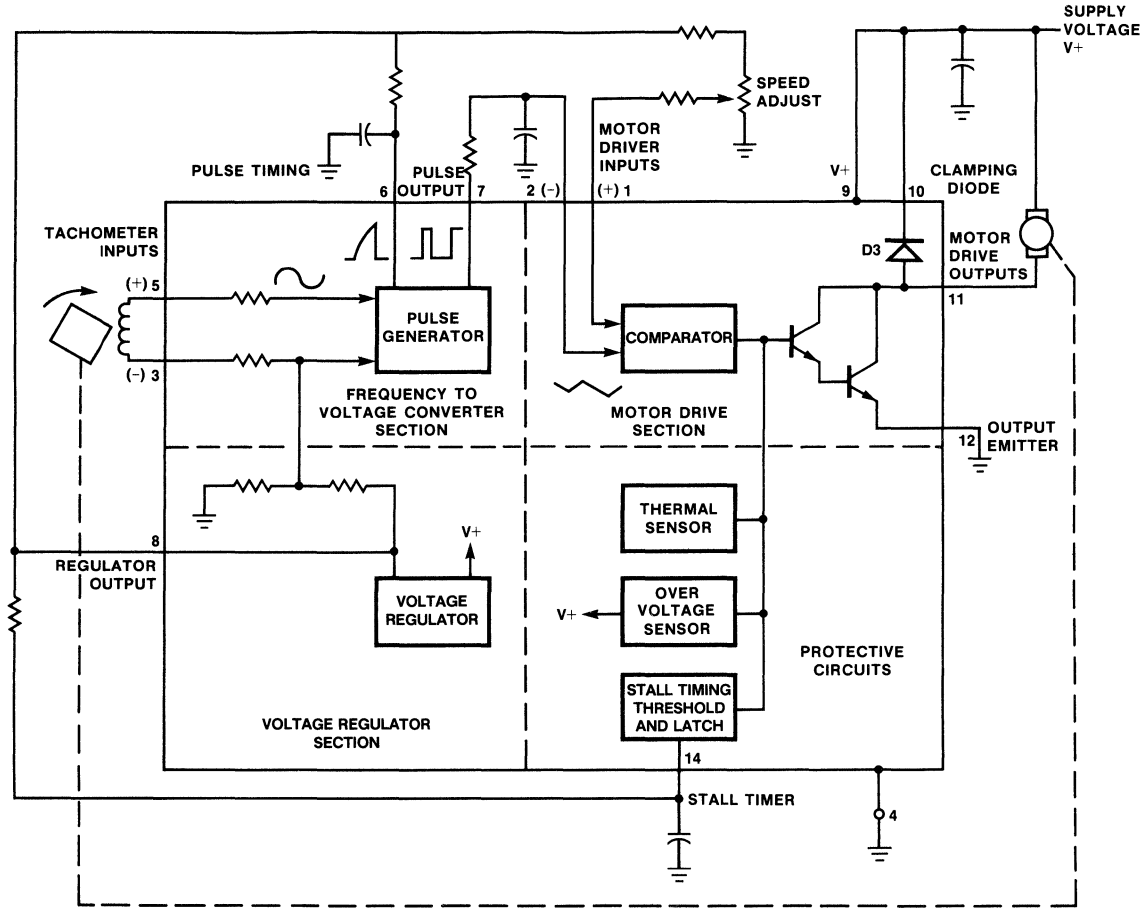
Block Diagram



μA7392
Electrical Characteristics V+ = 14.5 V, T_A = 25°C, unless otherwise noted

Voltage Regulator Section (Test Circuit 1)

Characteristic	Condition	Min	Typ	Max	Unit
Power Supply Current	Excluding Current into Pin 11		7.5	10	mA
Regulator Output Voltage		4.5	5.0	5.5	V
Regulator Output Line Regulation (ΔV_8)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_8)	I_8 from 10 mA to 0		40		mV

Electrical Characteristics V+ = 14.5 V, T_A = 25°C, unless otherwise noted

Frequency to Voltage Converter Section (Test Circuit 2)

Characteristic	Condition	Min	Typ	Max	Unit
Tachometer (−) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_5 = V_3$		1.0	10	μA
Tachometer Input Positive Threshold	$(V_5 - V_3)$	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{pk-pk}
Pulse Timing ON Resistance	V_6 = 1 V		300	500	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_8$
Output Pulse Rise Time			0.3		μs
Output Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_7)			0.13	0.25	V
Pulse Output HIGH Saturation ($V_8 - V_7$)			0.12	0.2	V
Pulse Output HIGH Source Current	V_7 = 1 V	−340	−260	−180	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	$V_{FV} = 0.25\ V_8$ (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	$V_{FV} = 0.25\ V_8$ (Note 2) T_A from −40°C to +85°C		0.3		%

Electrical Characteristics V+ = 14.5 V, T_A = 25°C, unless otherwise noted

Motor Drive Section (Test Circuit 3)

Characteristic	Condition	Min	Typ	Max	Unit
Input Offset Voltage				±20	mV
Input Bias Current			0.1	10	μA
Common-Mode Range		0.8		2.5	V
Motor Drive Output Saturation	I_{11} = 300 mA		1.3	1.6	V
Motor Drive Output Leakage	$V_{11} = V_{10}$ = 16 V			5	μA
Flyback Diode Leakage	V_{10} = 16 V, V_{11} = 0 V			30	μA
Flyback Diode Clamp Voltage	I_{11} = 300 mA Motor Drive Output Off		1.1	1.3	V

Notes

1. Frequency-to-Voltage Conversion, Supply Voltage Stability is defined as.

$$\frac{V_{FV}(16\ V)}{V_8(16\ V)} - \frac{V_{FV}(10\ V)}{V_8(10\ V)} \div \frac{V_{FV}(14.5\ V)}{V_8(14\ 5\ V)} \times 100\%$$

2. V_{FV} is the integrated dc output voltage from the pulse generator (Pin 7)

3. Frequency-to-Voltage Conversion Temperature Stability is defined as·

$$\frac{V_{FV}(85°C)}{V_8(85°C)} - \frac{V_{FV}(-40°C)}{V_8(-40°C)} \div \frac{V_{FV}(25°C)}{V_8(25°C)} \times 100\%$$

μA7392
Electrical Characteristics (Cont.) V+ = 14.5 V, T_A = 25°C, unless otherwise noted

Protective Circuits (Test Circuit 4)

Characteristic	Condition	Min	Typ	Max	Unit
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	2.5	2.9	3.5	V
Stall Timer Threshold Current	Note 5		0.3	3.0	μA

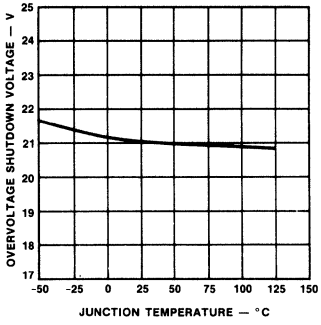
Notes

4 "Motor Drive" circuitry is disabled when these limits are exceeded. If the condition continues for the duration set by the external stall timer components, the circuit is latched off until reset by temporarily opening the power supply input line.

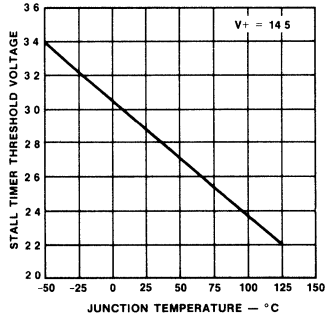
5. If stall timer protection is not required, Pin 14 should be grounded.

Typical Performance Curves

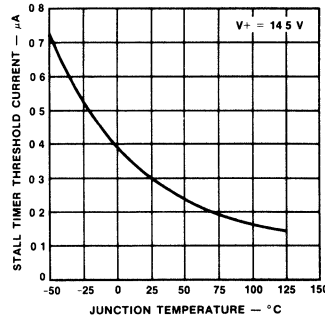
Overvoltage Shutdown Voltage vs Junction Temperature



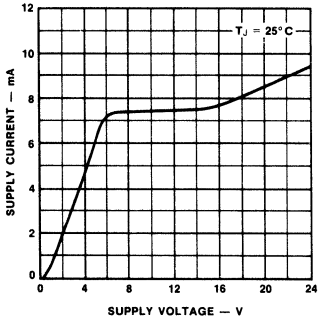
Stall Timer Threshold Voltage vs Junction Temperature



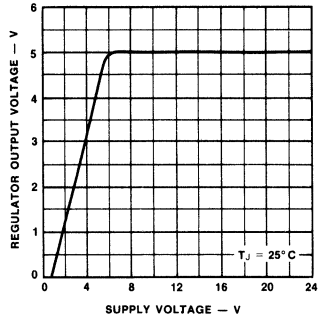
Stall Timer Threshold Current vs Junction Temperature



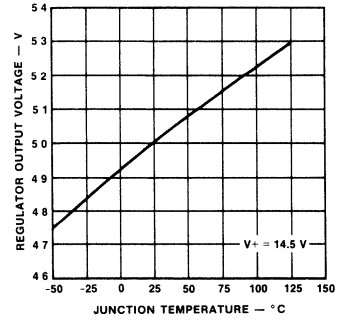
Supply Current vs Supply Voltage



Regulator Output Voltage vs Supply Voltage

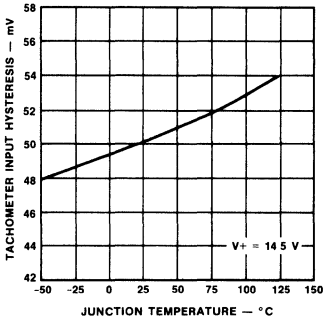


Regulator Output Voltage vs Junction Temperature

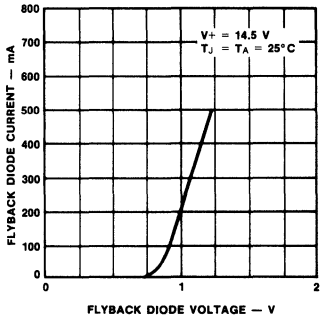


Typical Performance Curves (Cont.)

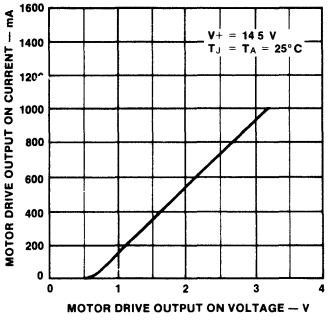
Tachometer Input Hysteresis vs Junction Temperature



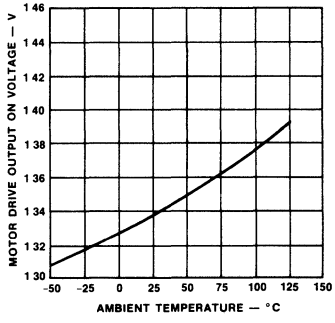
Flyback Diode (D3) Current vs Flyback Diode Voltage



Motor Drive Output on Current vs Motor Drive Output on Voltage

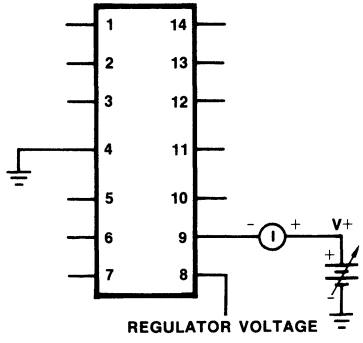


Motor Drive Output on Voltage vs Ambient Temperature



Test Circuits

Test Circuit 1



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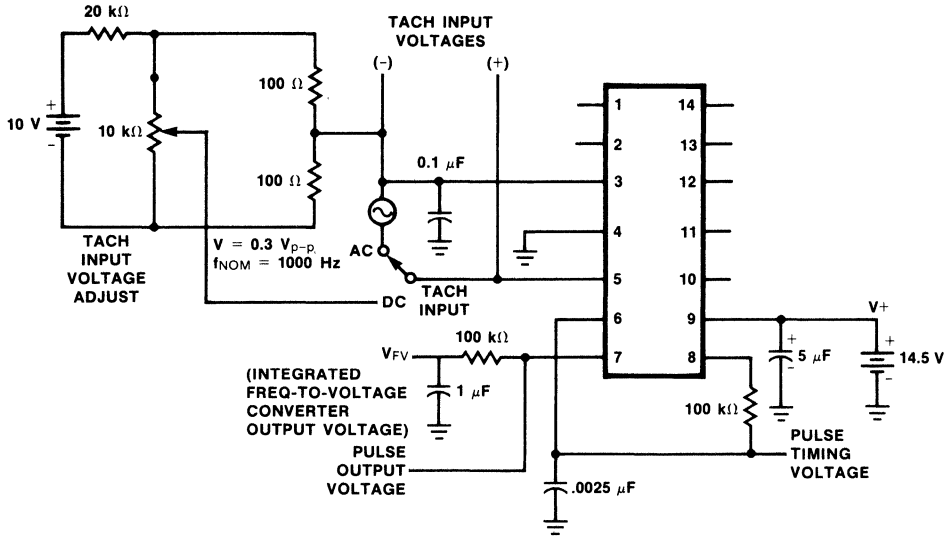
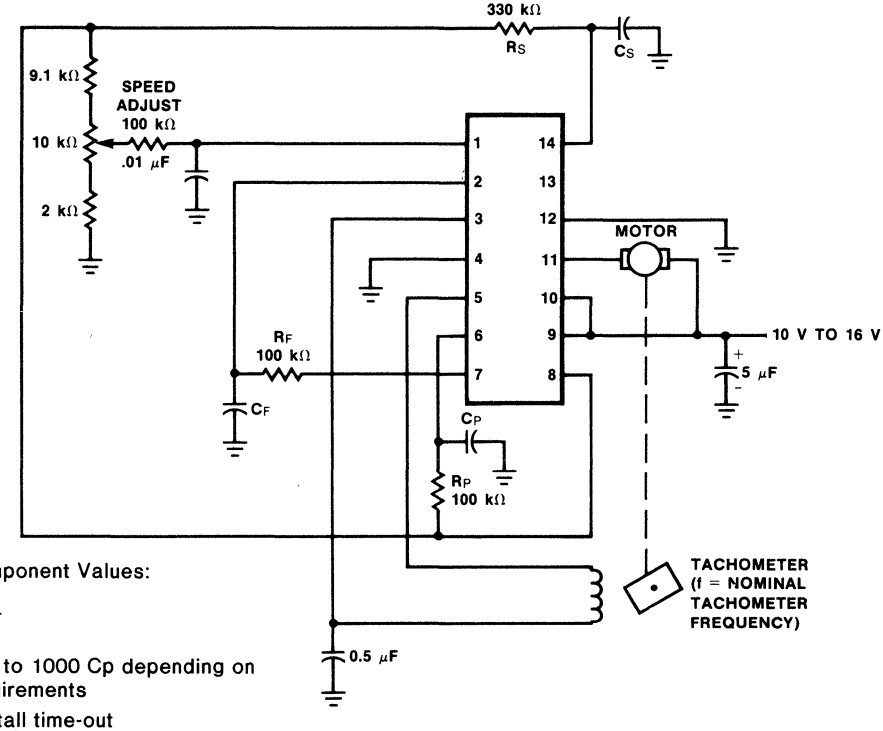
Test Circuits (Cont.)

Test Circuit 2



Typical Application Using Magnetic Tachometer



Typical Component Values:

$$Cp = \frac{1}{4\ R_{PF}}$$

C_F = 10 Cp to 1000 Cp depending on system requirements

$$C_S = \frac{2 \times \text{stall time-out}}{R_S}$$

$R_{Motor} \geq 5\ \Omega$

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Hi Rel Processing

Hi Rel Processing

High Reliability (Hi Rel) processing to MIL-M-38510 & MIL-STD-883 is performed by a totally dedicated Business Unit within the Linear Division of Fairchild to serve the unique Linear components requirements of our various military customers. Fairchild Linear has been committed to the Linear Hi Rel program for many years and intends to continue to maintain a leadership position in that market segment.

The Hi Rel program offers three levels of processing flows as noted below that would normally satisfy a majority of customer requirements.

- JAN-Level "B"—Full compliance to MIL-M-38510 JAN program & QPL listings as published by Defense Electronics Supply Center (DESC), Ohio
- "QB" Flow —Conformance to Level "B" process requirements of MIL-STD-883 to Fairchild MIL temperature range data sheet electricals.
- Class "S" —Compliance to Class "S" process requirements of MIL-M-38510 & MIL-STD-883 including all wafer lot acceptance criteria.

Details of the above flows will be provided in the following pages where each flow will be discussed separately.

- Custom Processing
  —While the intent of the Linear Hi Rel program is to standardize as much as possible for cost effective processing around these three flows, certain customer requirements may dictate special processing. These customer requirements are met by "HL" specifications within the Hi Rel organization. These HL's reflect all the unique requirements of a customer drawing and must be separately negotiated with our marketing department for acceptability of device parameters and process requirements before an order is entered by Fairchild.

JAN Qualified (MIL-M-38510) Level "B" Program

The JAN Program offers the customer a standard of product processing, quality and reliability that is well documented by the manufacturer and monitored by the Defense Electronics Supply Center (DESC) of the U.S. Government. The products are manufactured in the U.S. in a government certified facility to the requirements of MIL-M-38510 and individual product specifications as called out in the MIL-M-38510 "Slash Sheets". The DESC certification is based on standardized documentation for design, processing, test methods, laboratory suitability and personnel training. Facilities and documentation are audited by DESC prior to certification and periodically thereafter.

Fairchild Linear maintains a very active JM 3856 Qualified Products List (QPL) Program and has maintained a leadership position in the total number of Linear QPL's for many years.

An outline of the JAN M38510 Class "B" flow is given in Figure 1.

Linear 'QB' Flow (MIL-STD-883 Level "B")

Fairchild's 'QB' process flow can fill customer needs when a desired product is not available on JAN QPL or when system requirements call for a cost effective but reliable alternative to the full JAN program. The product is processed to MIL-STD-883 methods as specified in Figure 3. Electrical testing is performed to Fairchild data sheet limits for appropriate electrical grade and Burn-In is performed per Fairchild Standard Schematics.

Class "S" Flow

Fairchild Linear offers a complete capability to fulfill all processing requirements of Class "S" at wafer fabrication, assembly and environmental screening and test/finish on selected popular devices. These acceptance criteria meet all requirements called out in MIL-M-38510 and MIL-STD-883 for Class "S" products. It is our intent to standardize the processing of Class "S" products to the 'HS' flow shown in Figures 4A–4C so that customer requirements for Class "S" can be minimized.

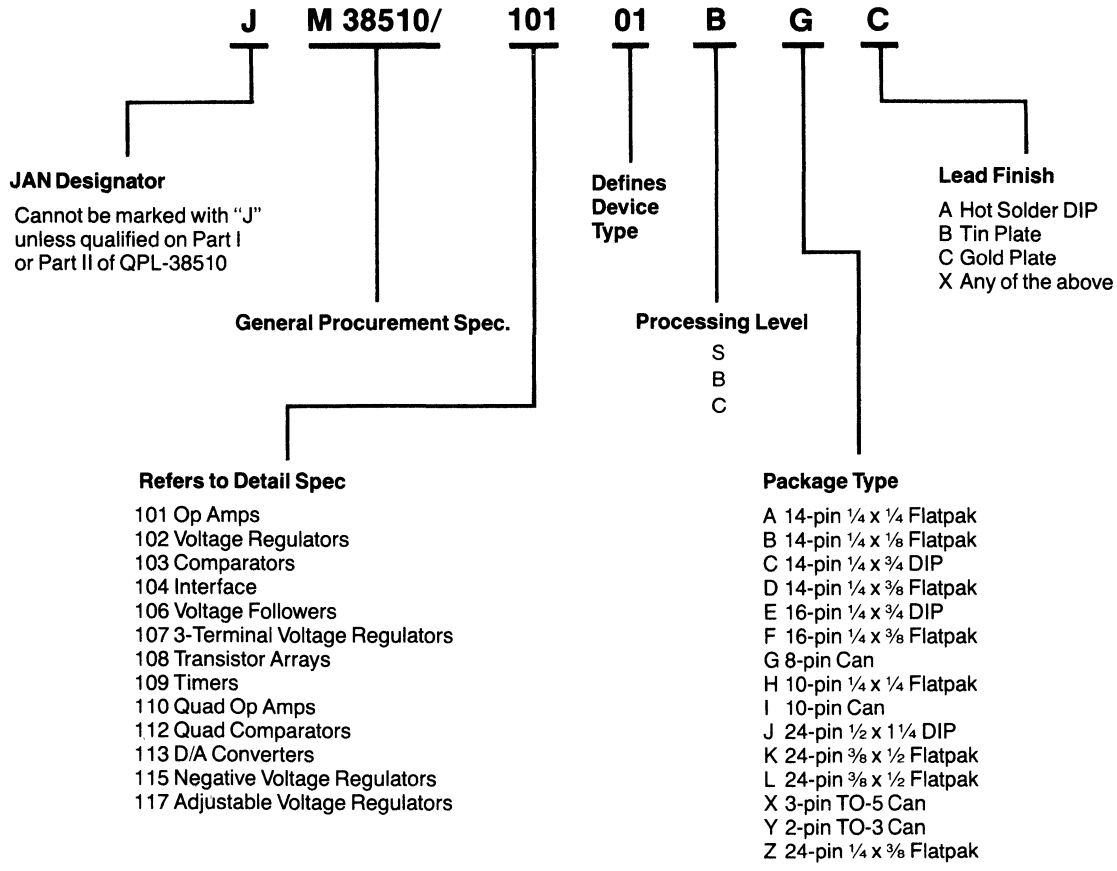
Fig. 1 JAN M38510 Process Flow

MIL-STD-883B Test Methods	Description	Class B
Preseal Visual MTD 2010	Cond. B. Optimum Visual Criteria	Preseal Visual Cond. B
Bond Strength MTD 2011	Bond strength is monitored on a sample basis three times per shift per machine	Bond Strength Cond. D
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	Seal
High Temp Storage MTD 1008	Cond. C Tstg = 150°C	Bake Cond. C Min 24 Hrs.
Temperature Cycle MTD 1010	Cond. C −65°/150°C 10 cycles	Temp Cycle Cond. C
Constant Acceleration MTD 2001 (Note 1)	Cond. E 30000 G's X_1, X_2, Y_1, Y_2	Centrifuge Cond. E Y_1 Only
Hermetic Seal MTD 1014 (Note 1)	Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C Gross-FC43/Hot 10^{-3} cc/sec or Gross-FC78/Vacuum 10^{-5} cc/sec	Hermeticity Cond. A/B Cond. C
Pre Burn-in Electrical	25°C dc electrical testing to remove rejects prior to submission to burn-in screen	Pre B/I Elect 25°C dc
Burn-in Screen MTD 1015 (Note 2)	Cond A, Cond B, Cond C Cond D, Cond E, Cond F	Burn In 160 Hrs 125°C
Post Burn-in Electrical	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include 25°C dc, 125°C dc, 55°C dc, 25°C dc, 25°C ac and 25°C Functional tests	Pst B/I Elect 25°C dc 10% PDA Other DC & AC tests per slash sheet requirement
Quality Conformance Inspection MTD 5005	Group A Electrical Characteristics Group B Package oriented Tests Group C Life Tests—Periodic Conformance Group D: Environmental Tests Periodic Conformance	Quality Conformance Gp A and B
External Visual MTD 2009	3X, 10X magnification Verify dimensions, configuration, lead structure, marking and workmanship	External Visual 100%
	Reliability Figure of Merit	15
	Ordering Part Number	JM38510/ 10101BCB
	Part Marking	JM38510/ 10101BCB

Notes

1. Not Applicable for TO-3 Cans
2. Time Temperature Curve (method 1015) may be used.
3. RELIABILITY Figure of Merit is the Reliability Improvement Factor from RADC Reliability Notebook, Vol. II, RADC-TR-67-108, Table XII-6, page 419.

Fig. 2 JAN Part Numbering System



Linear JAN Generic Part Numbers—Examples

JM38510/	01	02	03	04	05	06	07	08	09	10
101	741	747	101A	108A						
102	723									
103	710	711		111						
104	55107		9614	9615						
106	102									
107	109	78M05	78M12	78M15		7805	7812	7815	7824	
108		3045								
109	555	556								
110	148	149		4136	124					
112	139									
113	DAC08									
115	79M05	79M12	79M15		7905	7912	7915			
117	78MG		117H	117K						

Note
Dated material. Please contact Fairchild for latest revisions.

Fig. 3 QB Flow MIL-STD-883 Level-B

MIL-STD-883B Test Methods	Description	Class B
Preseal Visual MTD 2010	Cond. B. Optimum Visual Criteria	Preseal Visual Cond. B
Bond Strength MTD 2011	Bond strength is monitored on a sample basis three times per shift per machine	Bond Strength Cond. D
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	Seal
High Temp Storage MTD 1008	Cond. C Tstg = 150°C	Bake Cond. C Min 24 Hrs.
Temperature Cycle MTD 1010	Cond. C −65°/150°C 10 cycles	Temp Cycle Cond. C
Constant Acceleration MTD 2001 (Note 1)	Cond. E 30000 G's X_1, X_2, Y_1, Y_2	Centrifuge Cond. E Y_1 Only
Hermetic Seal MTD 1014 (Note 1)	Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C Gross-FC43/Hot 10^{-3} cc/sec or Gross-FC78/Vacuum 10^{-5} cc/sec	Hermeticity Cond. A/B Cond. C
Pre Burn-in Electrical	25°C dc electrical testing to remove rejects prior to submission to burn-in screen	Pre B/I Elect 25°C dc
Burn-in Screen MTD 1015 (Note 2)	Cond A, Cond B, Cond C Cond D, Cond E, Cond F	Burn In 160 Hrs 125°C
Post Burn-in Electrical	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include 25°C dc, 125°C dc, 55°C dc, 25°C dc, 25°C ac and 25°C Functional tests	Post B/I Elect 25°C dc & Funct 125°C dc −55°C dc 25°C ac Sample if apply per Data Sheet
Quality Conformance Inspection MTD 5005	Group A Electrical Characteristics Group B Package oriented Tests Group C Life Tests—Periodic Conformance Group D: Environmental Tests Periodic Conformance	Quality Conformance Gp A and B
External Visual MTD 2009	3X, 10X magnification Verify dimensions, configuration, lead structure, marking and workmanship	Generic Data Available Gp C and D

Notes

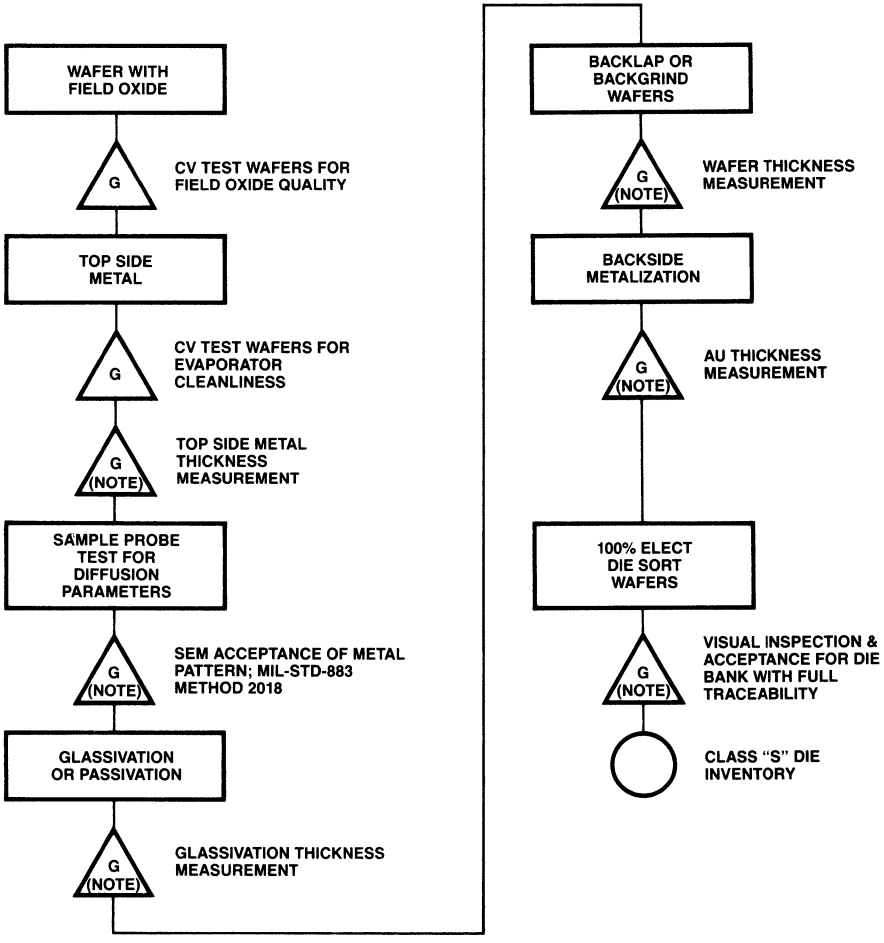
1. Not applicable for TO-3 Cans.
2. Time Temperature Curve (method 1015) may be used.

Class "S" Processing

The Linear Division has designed a Class "S" flow for all processing steps from Wafer Fabrication through Assembly, Test, Burn-In and Finish that will meet the requirements of majority of customers as well as the applicable military specifications and thus reduce the need for custom Level "S" process flows.

The flow charts that follow provide the major steps and acceptance criteria utilized for the processes and should form the basis for any Level "S" business negotiations with Linear Marketing. These flow charts will also provide a prospective customer with Fairchild Linear's capabilities in Level "S" processing.

Fig. 4A Class S: Minimum Wafer Lot Acceptance Steps

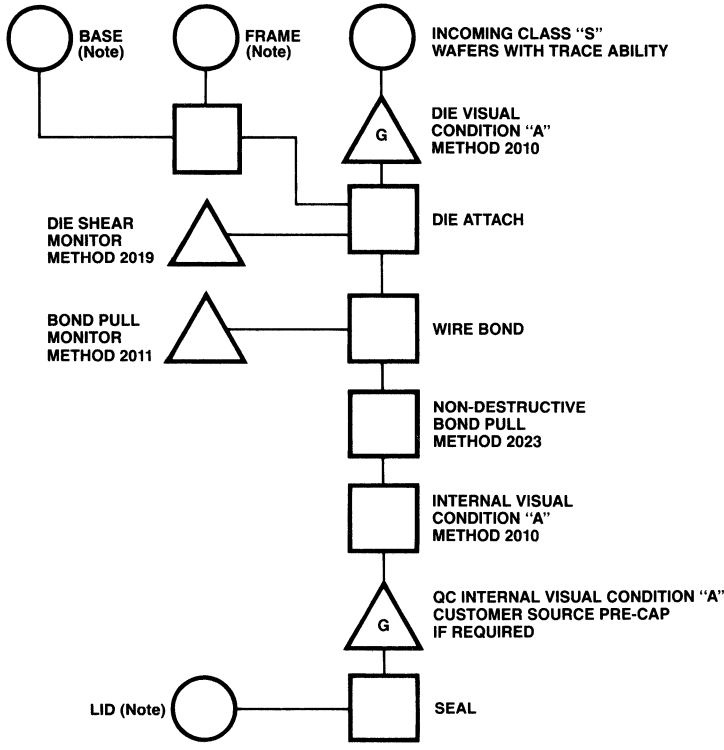


Note

All wafer lot acceptance is done per MIL-STD-883 Method 5007, Table I.

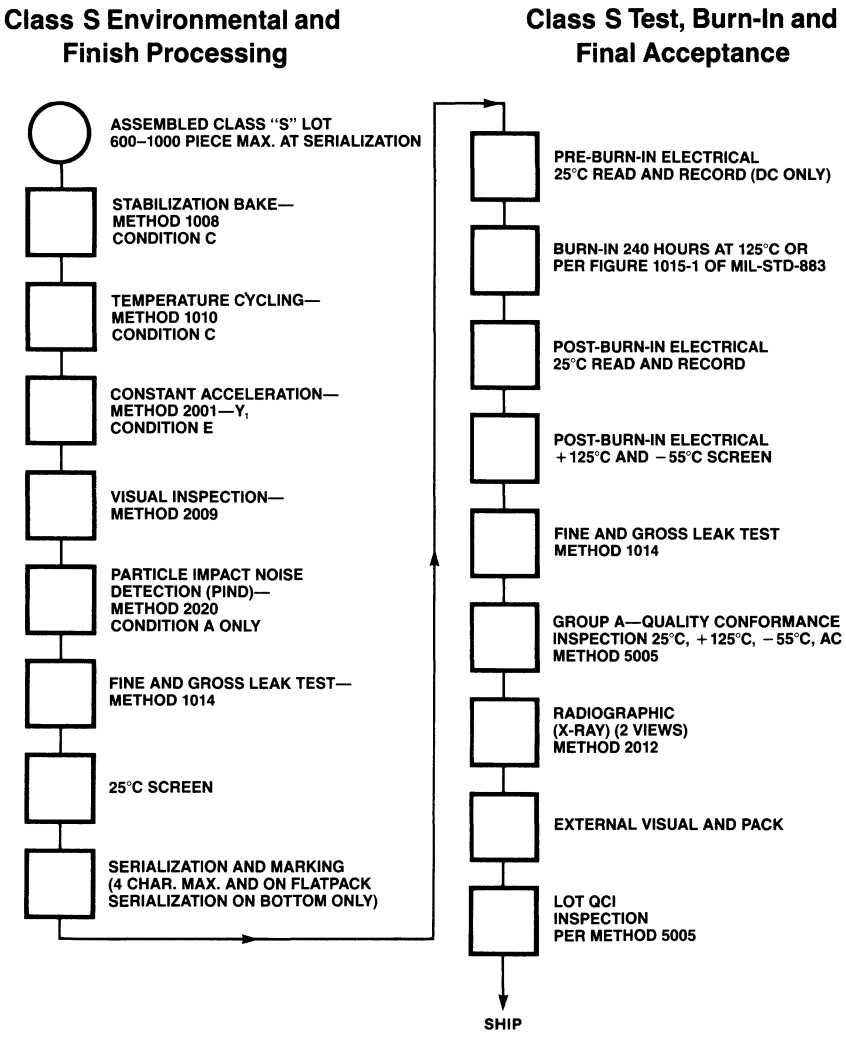
10

Fig. 4B Class S Assembly Flow



Note
Piece part traceability maintained when required.

Fig. 4C



Note
This is a general overview flow and specific packages may have unique requirements other than specified.

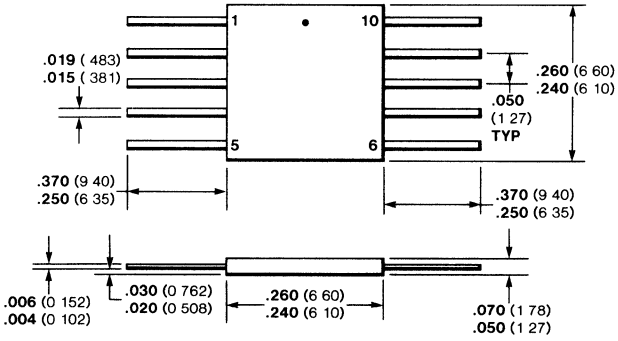
10

FAIRCHILD

A Schlumberger Company

Package Outlines

10-Pin Flatpak
In Accordance with JEDEC TO-91

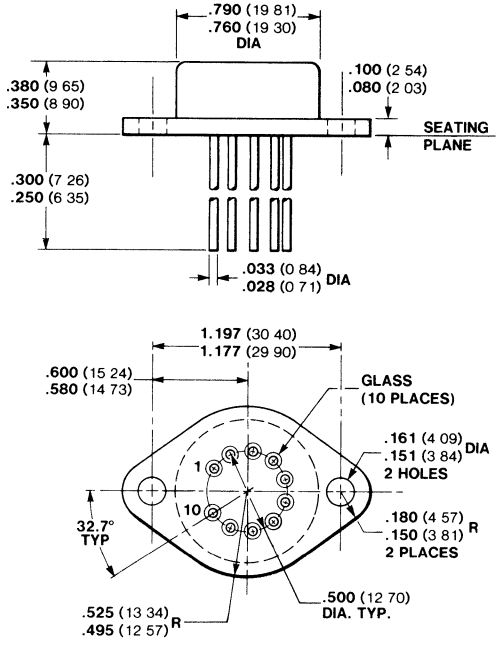


3F

Notes

Pins are tin-plated alloy 42
Hermetically sealed alumina package
Package weight is 0.26 grams

10-Pin Metal Package
Similar to JEDEC TO-3



5H

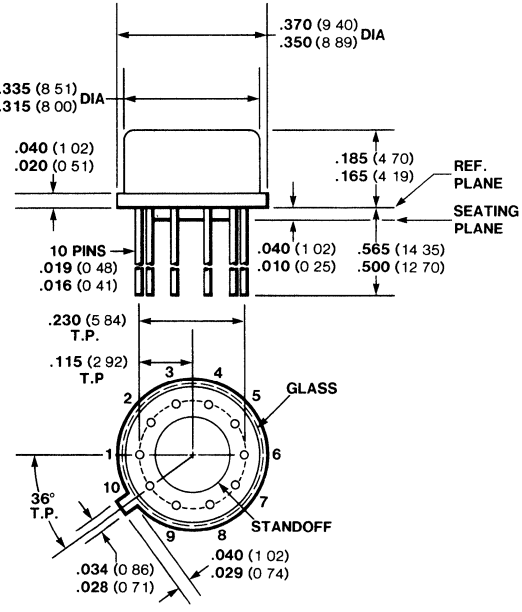
Notes

Base is heavy gold plated over nickel plated steel
Can is nickel plated steel
Pins are heavy gold plated over nickel plated alloy 52
All pins electrically isolated from case with glass
Package weight is 17 grams
*Similar to JEDEC TO-3 except for number of pins, pin length and pin diameter

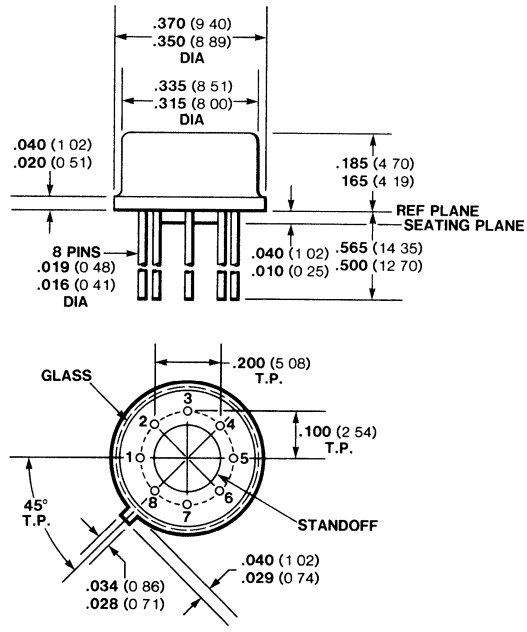
11

All dimensions in inches **bold** and millimeters (parentheses)

10-Pin Metal Package
In Accordance with JEDEC TO-100



8-Pin Metal Package
In Accordance with JEDEC TO-99



5U

Notes

Pins are extra heavy gold-plated kovar
Ten pins
Eyelet is extra heavy gold-plated kovar, glass filled with ceramic standoff
Can is grade A nickel
High RTH package
Package weight is 1.32 grams

5X

Notes

Pins are tin-plated over nickel-plated kovar
Nine pins thru, pin 5 is connected to case
Eyelet is nickel plated kovar, glass filled with ceramic standoff, tin plated outside metal surface
Can is grade A nickel, tin plated outside surface
Package weight is 1.32 grams

5Y

Notes

Pins are tin-plated over nickel plated kovar
Ten pins
Eyelet is nickel plated kovar, glass filled with ceramic standoff, tin plated outside metal surface
Can is grade A nickel, tin plated outside surface
Package weight is 1.32 grams

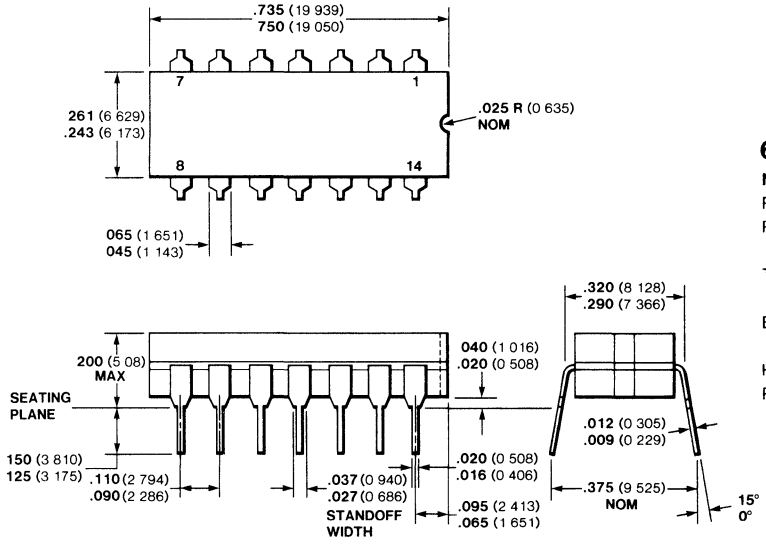
5W

Notes

Pins are tin-plated over nickel plated kovar
Seven pins thru, pin no 4 connected to case
Eyelet is nickel plated kovar, glass filled with ceramic standoff, tin plated outside metal surface
Can is grade A nickel, tin plated outside surface
Package weight is 1 22 grams

All dimensions in inches **bold** and millimeters (parentheses)

14-Pin Ceramic Dual In-Line
In Accordance with JEDEC TO-116



6A, 8A

Notes

Pins are tin-plated alloy 42

Pins are intended for insertion in hole rows on 300 (7 620) centers

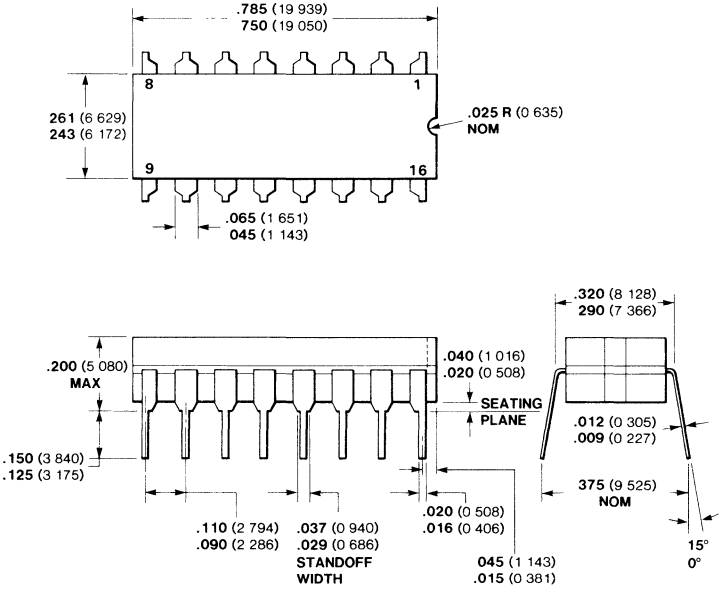
They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for 020 (0 508) diameter pin

Hermetically sealed alumina package

Package weight is 2 0 grams

16-Pin Ceramic Dual In-Line



6B, 8B

Notes

Pins are tin-plated alloy 42

Pins are intended for insertion in hole rows on 300 centers (7 62)

Units are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020 (0 508) diameter pin

Hermetically sealed alumina package

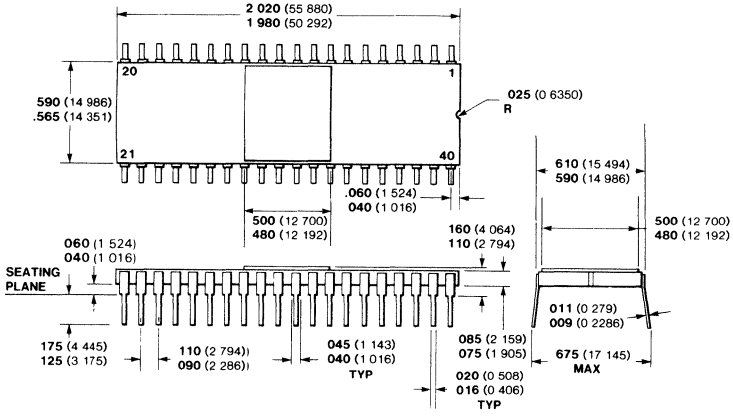
Package weight is 2 0 grams

*The 037- 027 (0 940-0 686) dimension does not apply to the corner pins

11

All dimensions in inches **bold** and millimeters (parentheses)

40-Pin Ceramic Dual In-Line Side Brazed

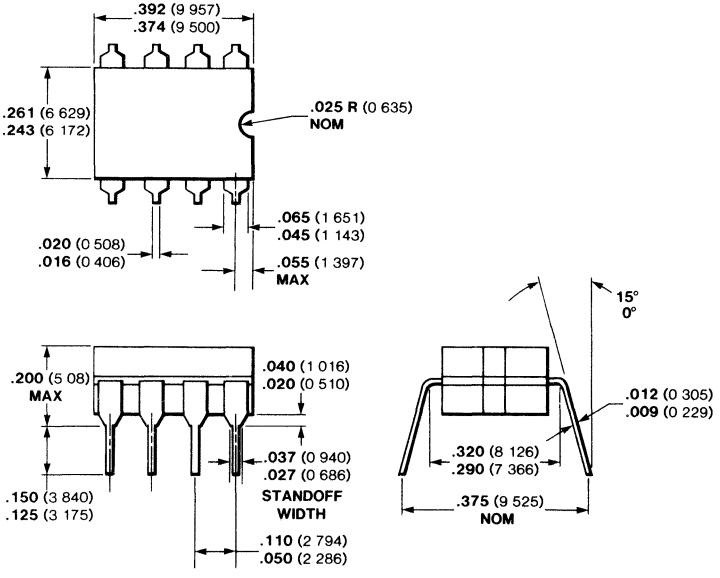


6I

Notes

Pins material nickel gold-plated kovar
Cap is kovar
Base is ceramic
Cavity size is 310 X 310
Package weight is 6 5 gram

8-Pin Ceramic Dual In-Line



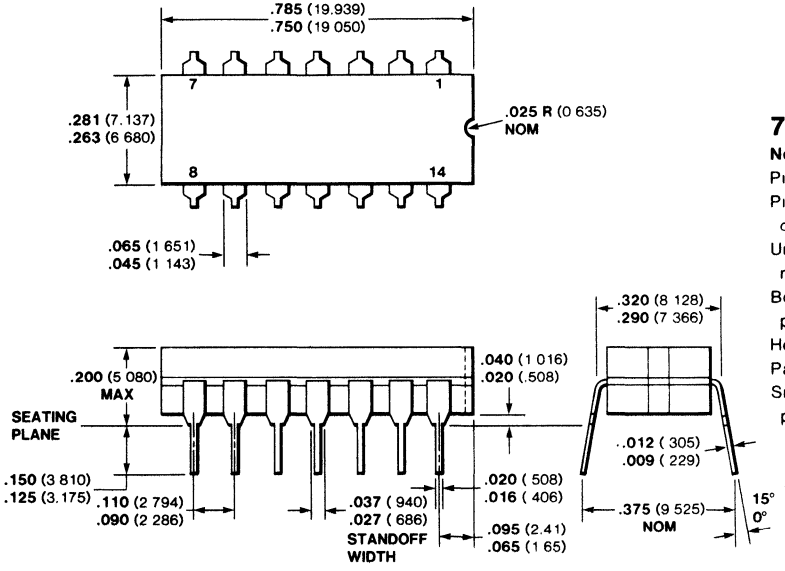
6T, 8P

Notes

Pins are tin-plated alloy 42
Pins are intended for insertion in hole rows on 300 centers
Units are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for 020 (0.508) diameter pin
Hermetically sealed alumina package
Package weight is 1 0 grams

All dimensions in inches **bold** and millimeters (parentheses)

14-Pin Ceramic Dual In-Line
Similar to JEDEC TO-116

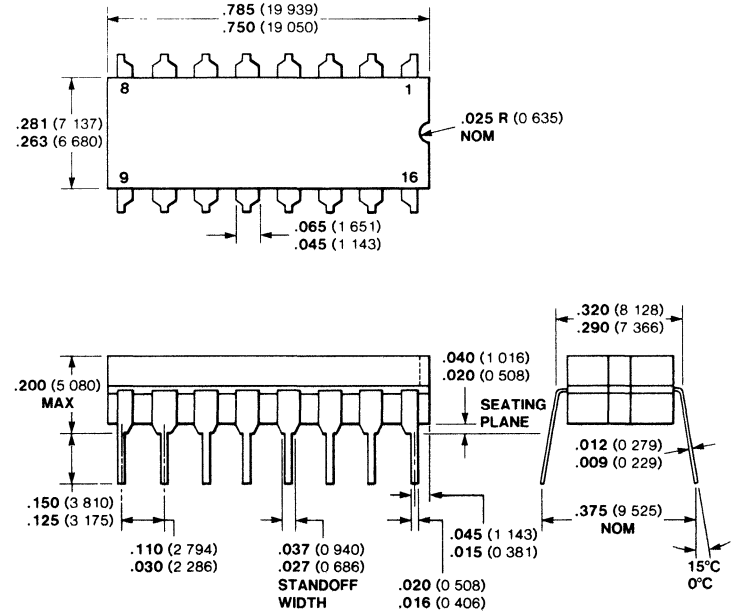


7A

Notes

Pins are tin-plated alloy 42
Pins are intended for insertion in hole rows on 300 (7.62) centers
Units are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for 020 (0 508) diameter pin
Hermetically sealed alumina package
Package weight is 152 2 grams
Similar to JEDEC TO-116 except for package width

16-Pin Ceramic Dual In-Line



7B

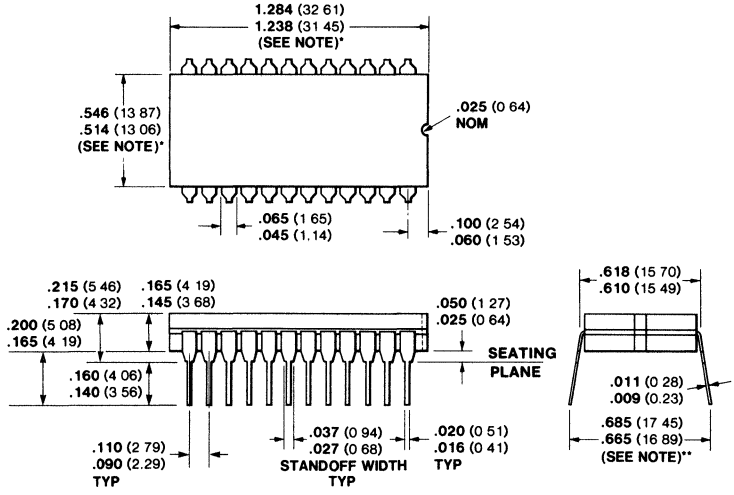
Notes

Pins are tin-plated alloy 42
Pins are intended for insertion in hole rows on 300 (7.62) centers
Units are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for 020 (0 508) diameter pin
Hermetically sealed alumina package
Package weight is 2.2 grams
*The 037- 027 (0.940-0.686) dimension does not apply to the corner pins

11

All dimensions in inches **bold** and millimeters (parentheses)

24-Pin Ceramic Dual In-Line

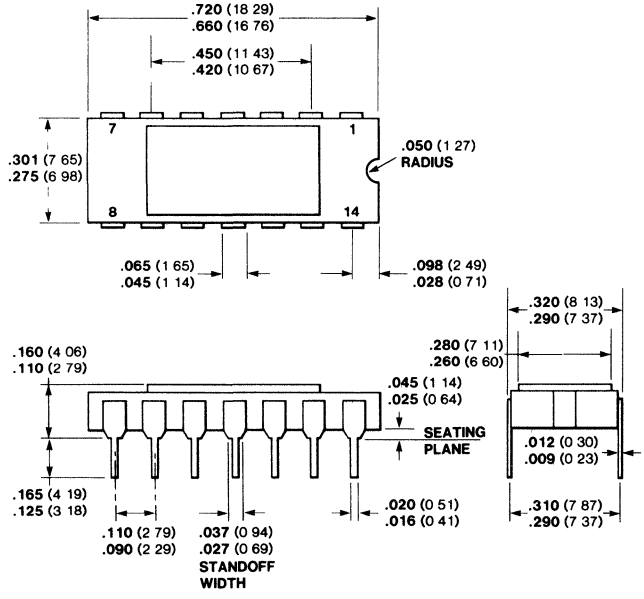


7L

Notes

Pins are tin-plated alloy 42 or equivalent
Package material is alumina
Pins intended for insertion in hole rows on .600 centers (15.24)
They are purposely shipped "positive" misalignment to facilitate insertion
Cavity size is .245 X .245 (6.22 X 6.22)
Package weight is 7.1 grams
These dimensions include misalignment and glass over-run etc.
This dimension is measured from centerline to centerline of pins

14-Pin Ceramic Dual In-Line



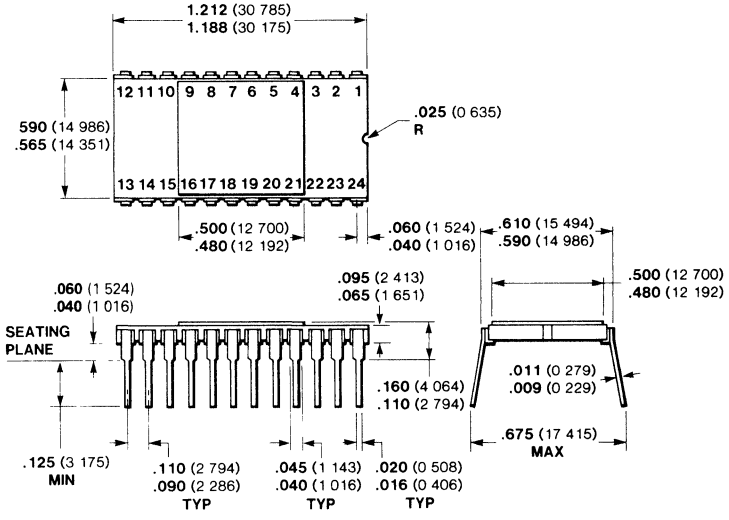
7N

Notes

Pins are gold-plated kovar
Base is alumina
Lid is gold-plated kovar
Pins are intended for insertion in hole rows on .300" centers (7.62)
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Package weight is 1.3 grams

All dimensions in inches **bold** and millimeters (parentheses)

24-Pin Ceramic Dual In-Line Side Brazed

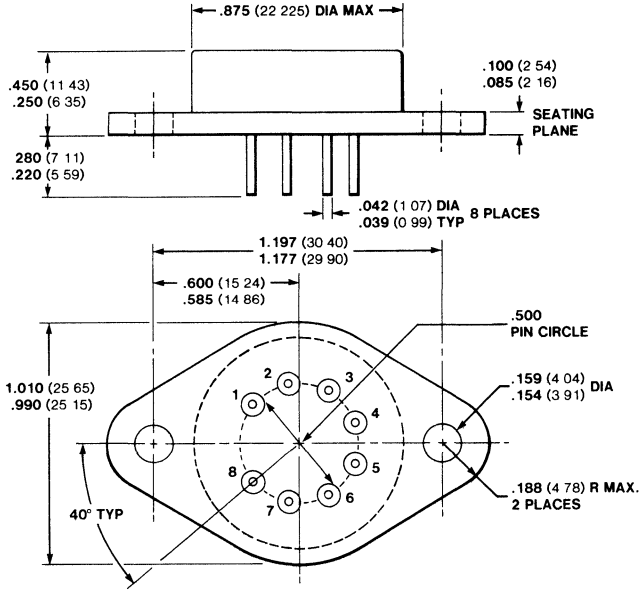


7R

Notes

Pins are nickel gold-plated kovar
Cap is kovar
Base is ceramic
Cavity size is 250 X 250
Package weight is 3 85 gram

8-Pin Metal Package Similar to JEDEC TO-3



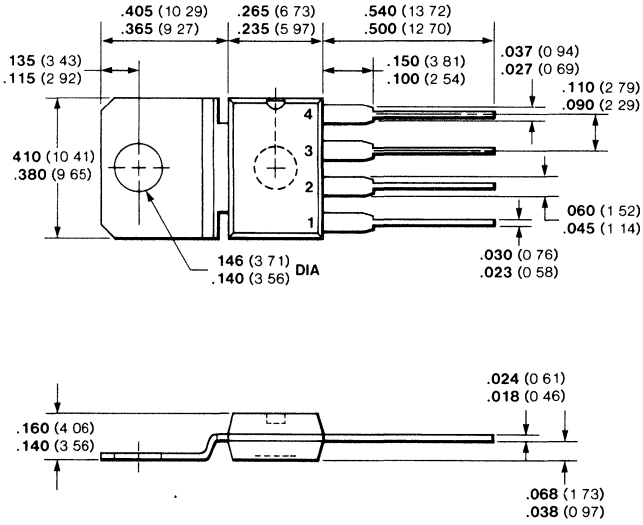
8G

Notes

Pins are gold-plated kovar
7 pins through, pin 4 connected to case
Package weight is 1 22 grams

All dimensions in inches **bold** and millimeters (parentheses)

4-Pin Molded Single Wing

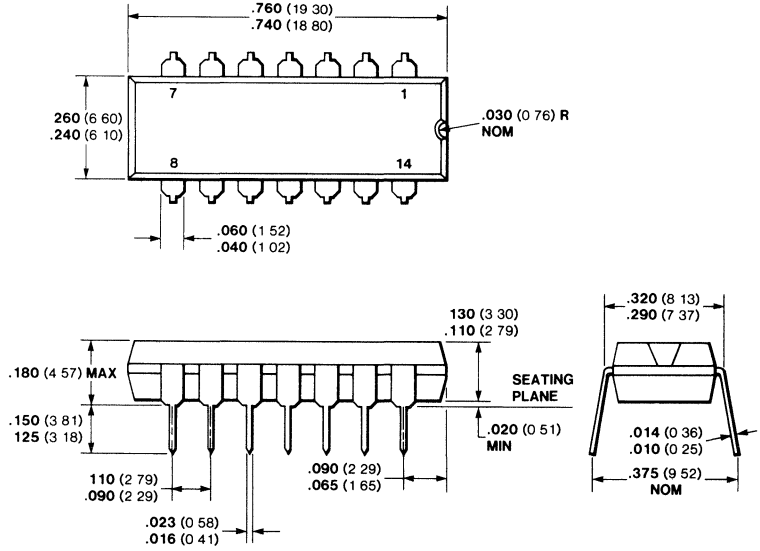


8Z

Notes

Pins are tin plated copper alloy
Mounting tab is electrically insulated from pins
Mounting tab is tin plated copper alloy
Board-drilling dimensions should equal your practice for 033 (0 84) diameter pins
This package is intended to be mounted with the tab flush with the top of the P C board or heat sink A no 4 screw may be used to secure the package Thermal compound is recommended
Package material is plastic
Package weight is 1 2 grams

14-Pin Molded Dual In-Line
In Accordance with JEDEC TO-116



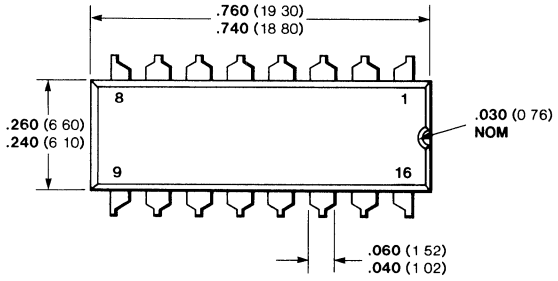
9A

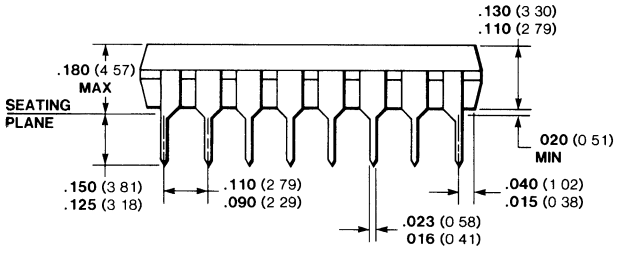
Notes

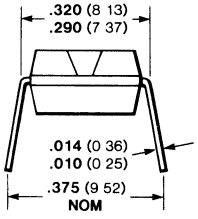
Pins are solder dipped copper alloy
Pins are intended for insertion in hole rows on 300 (7 62) centers
Units are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for 020 (0 51) diameter pin
Package material is plastic
Package weight is 0 9 grams

All dimensions in inches **bold** and millimeters (parentheses)

16-Pin Molded Dual In-Line







9B

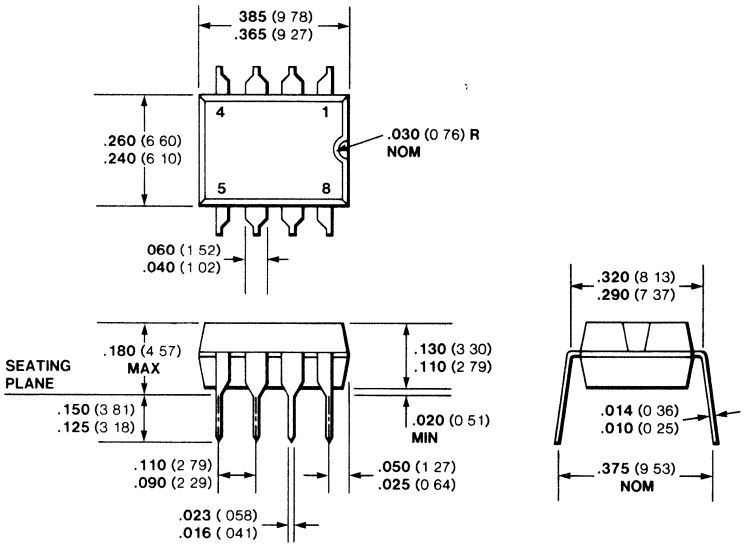
Notes

Pins are solder dipped copper alloy
Pins are intended for insertion in hole rows on 300 (7 62) centers
Units are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for 020 (0 51) diameter pin
Package material is plastic
Package weight is 1 0 grams

11

All dimensions in inches **bold** and millimeters (parentheses)

8-Pin Molded Dual In-Line

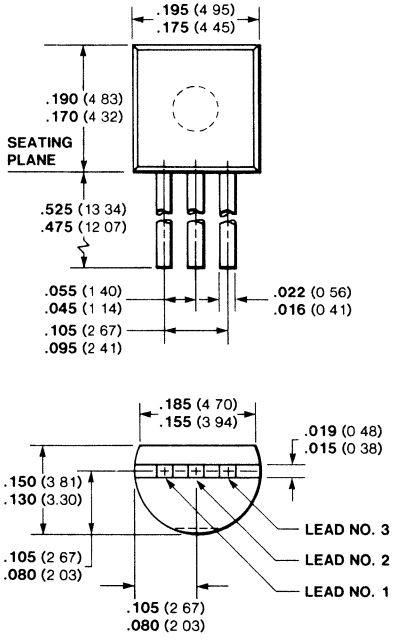


9T

Notes

Pins are solder dipped copper alloy
Pins are intended for insertion in hole rows on 300 (7 62) centers
Units are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for 020 (0 51) diameter pin
Package material is plastic
Package weight is 0.6 gram

3-Pin Molded Package Similar to JEDEC TO-92



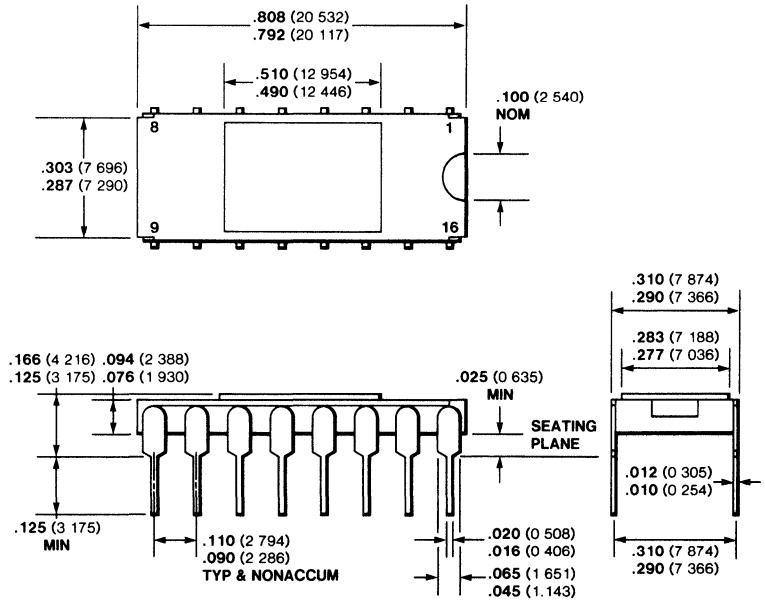
EI

Notes

Pins are solder dipped copper alloy
Pin no 2 connected to die pad
Package material is plastic
Package weight is 0 19 gram
*Similar to JEDEC TO-92 except for pin dimensions

All dimensions in inches **bold** and millimeters (parentheses)

16-Pin Ceramic Dual In-Line

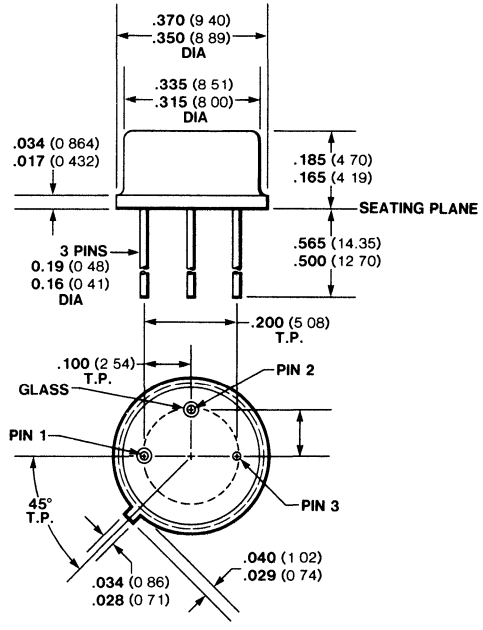


FB

Notes

Pins are nickel alloy 42 or kovar
Base is alumina
Cap is alumina
Pins are intended for insertion in hole rows on .300" centers
Board drilling dimensions should equal your practice for .020" diameter lead
Pin finishes available—tin or gold plate
Cavity size is .220 × 280

2-Pin Metal Package Similar to JEDEC TO-39



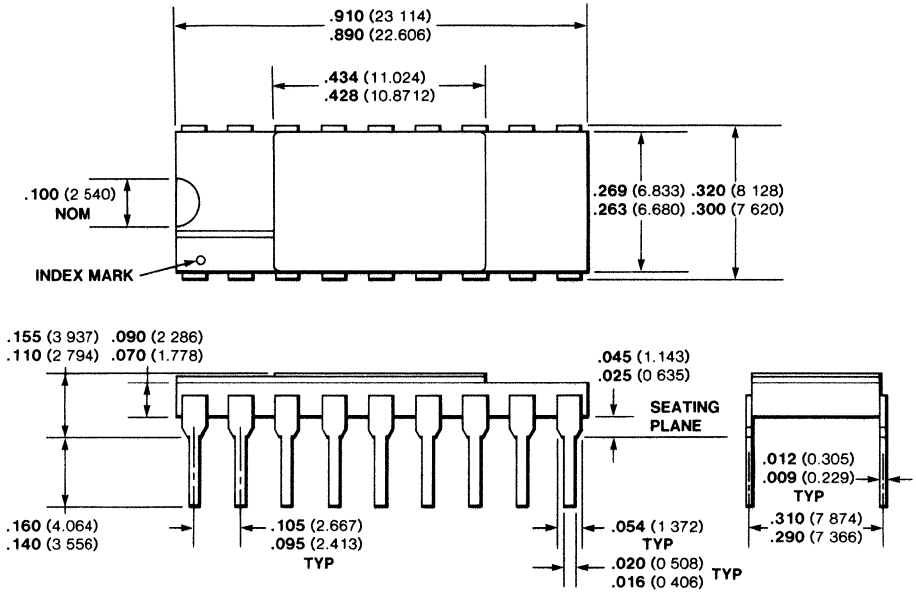
FC

Notes

Pins are gold plated kovar
Pins 1 and 2 are electrically isolated with glass
Pin no 3 connected to case
Eyelet is gold plated kovar
Can is grade A nickel
Package weight is 1.23 grams
*Similar to JEDEC TO-39 except for can height

All dimensions in inches **bold** and millimeters (parentheses)

18-Pin Ceramic DIP
Side-Brazed



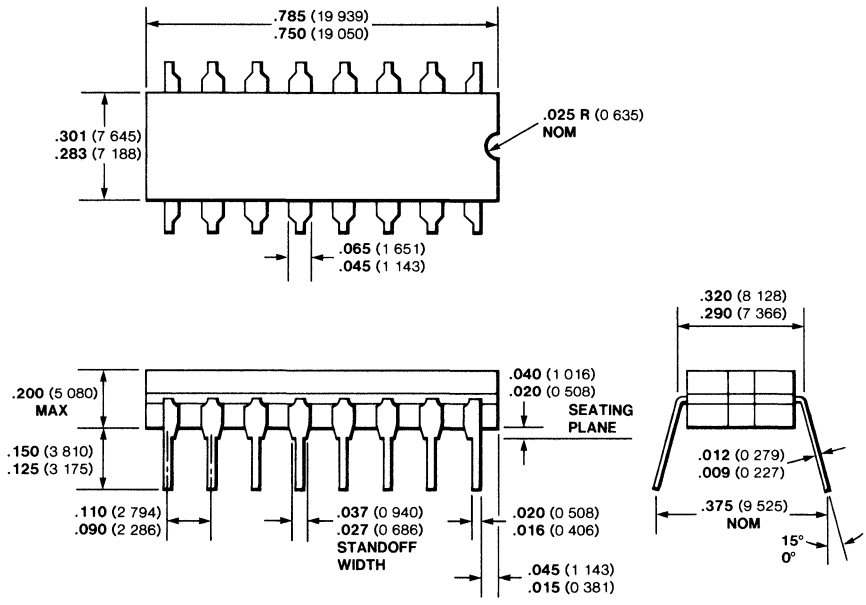
FD

Notes

Pins are nickel alloy 42 or kovar
Base is alumina
Cap is alumina
Pins are intended for insertion in hole rows on .300" centers
Board drilling dimensions should equal your practice for .020" diameter lead
Pin finishes available—tin or gold plate
Cavity size is 220 X 280

All dimensions in inches **bold** and millimeters (parentheses)

16-Pin Ceramic Dual In-Line



FW

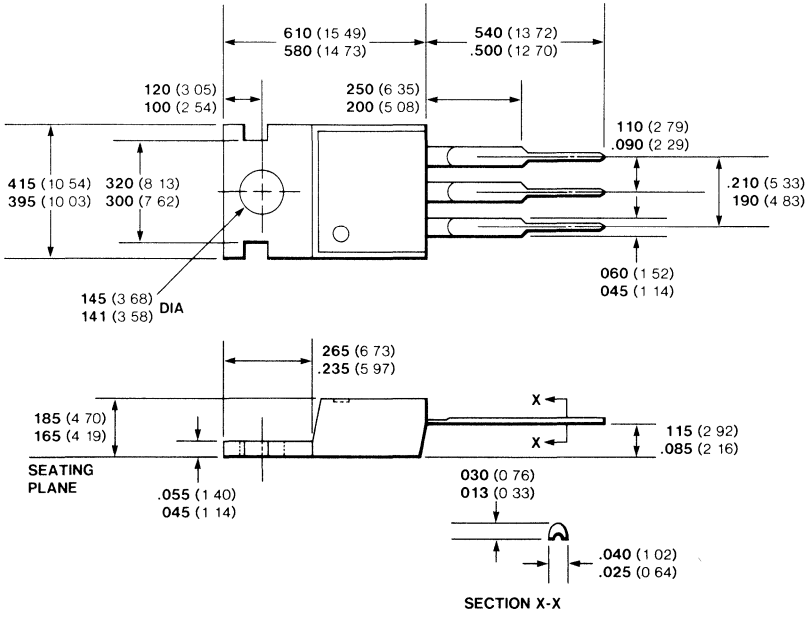
Notes

Pins are tin-plated alloy 42
Pins are intended for insertion in hole rows on 300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Hermetically sealed alumina package
Package weight is 2 2 grams
*The 037-.027 (0 940-0 686) dimension does not apply to the corner pins

11

All dimensions in inches **bold** and millimeters (parentheses)

3-Pin Molded Package
Similar to JEDEC TO-220



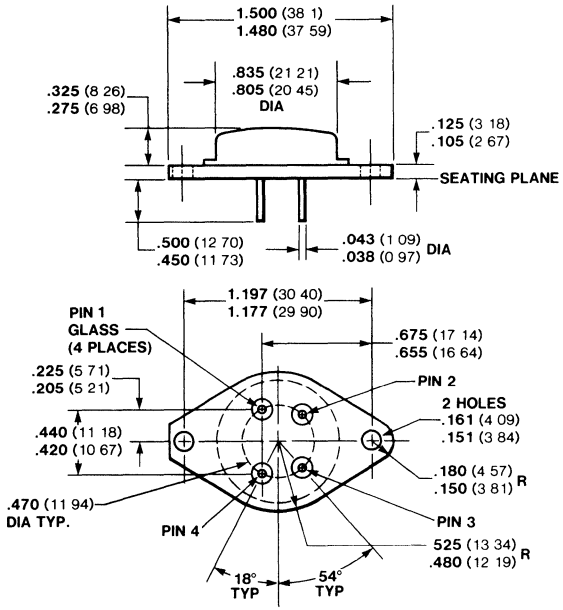
GH

Notes

Pins are solder dipped over nickel plated copper alloy
Pin 2 is electrical contact with the mounting tab
Mounting tab is nickel plated copper alloy
Package material is plastic
Package weight is 2.0 grams

All dimensions in inches **bold** and millimeters (parentheses)

4-Pin Metal Package
Similar to JEDEC TO-3

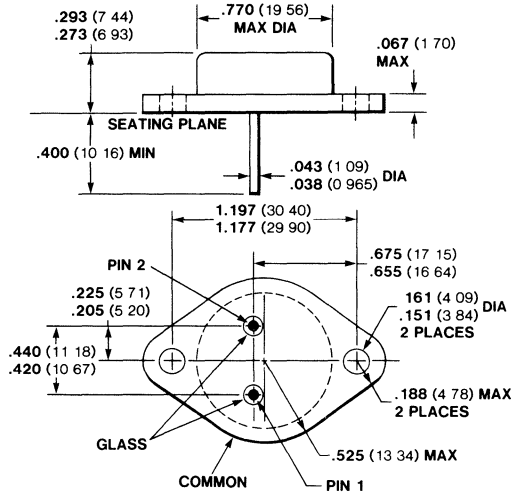


GK

Notes

Base is nickel plated aluminum
Can is aluminum
Pins are gold plated over nickel plated alloy 52
All pins electrically isolated from case with glass
Package weight is 7 4 grams
*Similar to JEDEC TO-3 except for number of pins

2-Pin Metal Package
Similar to JEDEC TO-3



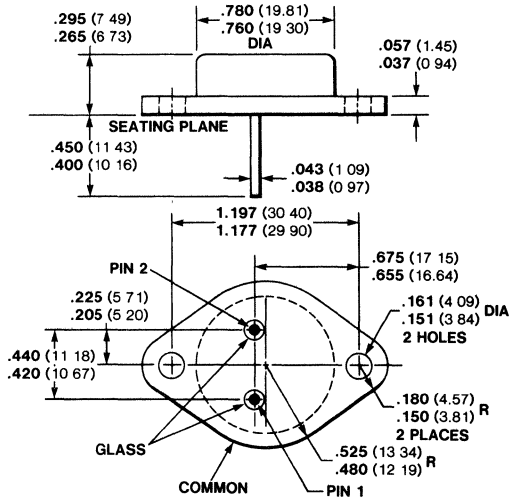
GN

Notes

Pins 1 and 2 electrically isolated from case
Case is third electrical connections

All dimensions in inches **bold** and millimeters (parentheses)

2-Pin Metal Package
In Accordance with JEDEC TO-3

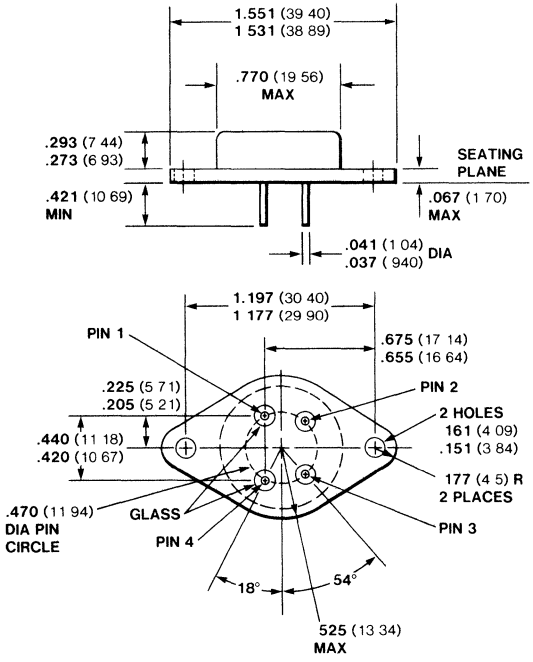


HJ

Notes

Base is nickel plated steel
Can is nickel plated steel
Pins are solder dipped over nickel plated alloy 52
Pins 1 and 2 electrically isolated from case with glass
Case is third electrical connection
Package weight is 9 2 grams

4-Pin Metal Package
Similar to JEDEC TO-3



JA

Notes

Pins are solder dipped alloy 52
All pins electrically isolated from case

All dimensions in inches **bold** and millimeters (parentheses)

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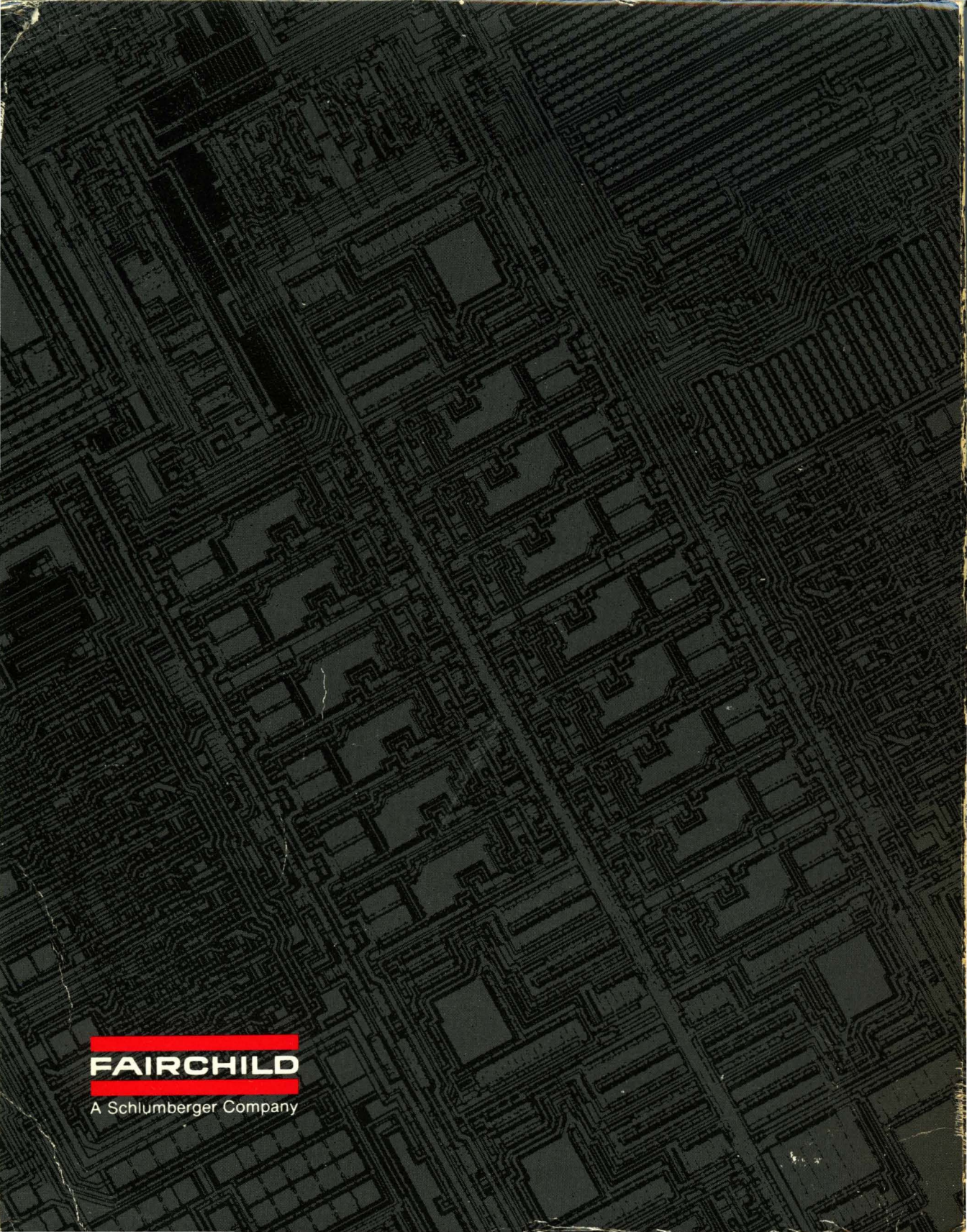
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