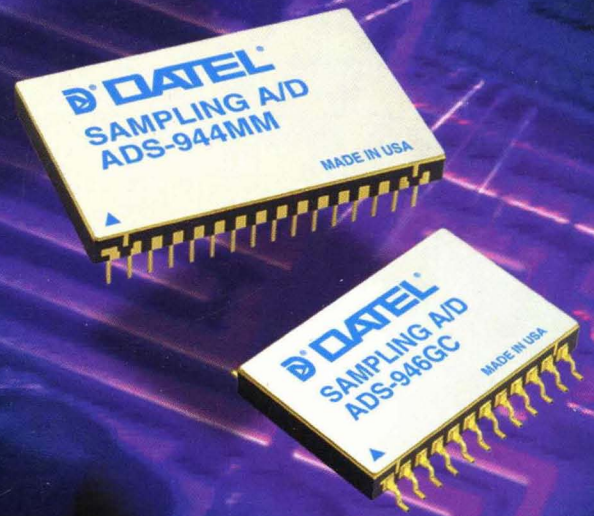
DATEL®

SAMPLING A/D CONVERTERS

ISO 9001 REGISTERED
MIL-STD-1772 CERTIFIED



DATA ACQUISITION COMPONENTS

DATEL®
SAMPLING A/D CONVERTERS
1996

DATEL Sampling A/D Converters and Data Acquisition Components

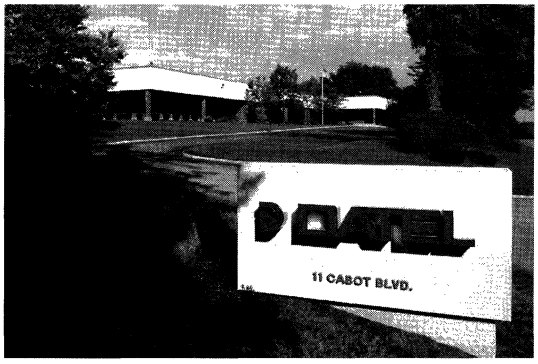
ISO 9001
REGISTERED

MIL-STD-1772
Certified and Qualified

About DATEL

Founded in 1970, today's DATEL is an international electronics manufacturing company that has achieved leadership status in all *four* of its core product lines: sampling A/D converters and data acquisition components; analog I/O boards for PCI, EISA, ISA, VME and Multibus platforms; switching DC/DC power converters; and digital panel voltmeters and instruments.

Our leadership status in high-performance sampling analog-to-digital converters is unchallenged. If you are unfamiliar with our products, you are about to discover 14 and 16-bit ADS's whose outstanding electrical performance, small packaging, low power consumption, ease-of-use and affordable pricing will genuinely impress you.



All our products are proudly designed and manufactured in our modern 180,000 square-foot facility in Mansfield, Massachusetts (U.S.A.). To serve our international customers, we have wholly owned Subsidiary Sales Offices in Japan, Germany, France and the United Kingdom.

Manufacturing and Quality

DATEL's data acquisition components are manufactured and assembled using four basic technologies: monolithic CMOS, monolithic bipolar, thin and thick-film multi-chip module (MCM), and discrete component assemblies.

Our overall Company is ISO-9001 Registered. Our MCM facility is certified to MIL-STD-1772, and we are listed on QML-38534 (the Qualified Manufacturers List). Most of our standard products are MIL-STD-883 qualified, and many are covered by DESC SMD's.

Convenience

DATEL has direct sales offices in the United States (Mansfield, MA), Germany (Munich), France (Montigny Le Bretonneux), England (Tadley) and Japan (Tokyo and Osaka). We employ an extensive network of field sales representatives throughout the USA, Canada, Europe, the Far East and other areas around the world.

In the USA, dial 1-800-233-2765 to immediately receive literature, price and delivery information or applications assistance.

Our E-Mail address is datelcomp@aol.com

There are four ways in which to purchase DATEL Data Acquisition Components:

- VISA or Mastercard
- Bank check or money order
- C.O.D.
- Open an account with established credit

VISA MasterCard

Availability

Most DATEL products are available, in small quantities, from stock and can be shipped from the USA within 24 hours. For price and delivery information, USA customers may contact DATEL directly. Our international customers should contact their local DATEL sales office or representative.

Applications Assistance

DATEL employs a large, knowledgeable, patient staff of degreed Applications and Sales Engineers in both our Headquarters and Subsidiary Offices. These experienced engineers are always available to answer any questions you may have concerning the use or modification of any of our products. Please don't hesitate to call us.

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Product Index

General Disclaimer

In accordance with our policy of continuous product improvement, DATEL, Inc. reserves the right to make changes/improvements to our products and/or their specifications at any time without prior notice to anyone. Prices are also subject to change without notice.

DATEL Inc. makes every effort to ensure information provided in our technical literature is accurate and reliable. We can not, however, assume responsibility for inadvertent errors, inaccuracies, omissions or subsequent changes. We similarly assume no responsibility for the use of this information, and any and all such use of this information shall be entirely at the user's own risk.

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Limitations on the Use of DATEL, Inc. Products

DATEL products are not designed for and should not be used, without the specific prior written consent of DATEL, Inc., in any life-support systems, nuclear-facility applications, aircraft-control applications or any other applications in which failure of the product, in any way, could reasonably result in harm to life, property or the environment.

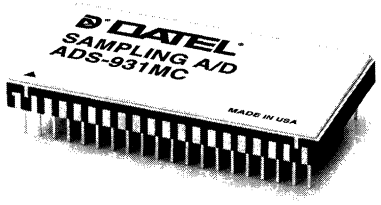
A life-support system is defined as a product or system intended to support or sustain life and whose failure can be reasonably expected to result in significant personal injury or death. Nuclear-facility applications are defined as any application involving a nuclear reactor or the handling and processing of radioactive materials in which the failure of equipment, in any way, could reasonably result in harm to life, property or the environment.

DATEL, Inc., 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For immediate assistance 800-233-2765

New Products

16-Bit Sampling A/D Converters

1 and 2MHz, High Performance

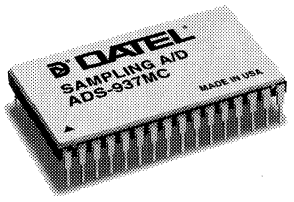


ADS-931, ADS-932

- Functionally complete, requires no external support circuitry
- Small, 40-pin, ceramic TDIP package
- ±5V supplies; 1.85 Watts
- No missing codes over temperature
- Low noise, 50µVrms
- Impressive dynamic performance:
  Peak harmonics as low as –89dB
  THD as low as –89dB
  SNR as high as 87dB
- Ideal for both time and frequency-domain applications
- ±2.75V input range
- Commercial and military temperature ranges
- Edge triggered; On-board FIFO
- TTL compatible

See pages 1-95 and 1-103.

1MHz, Low Power/Cost



ADS-937

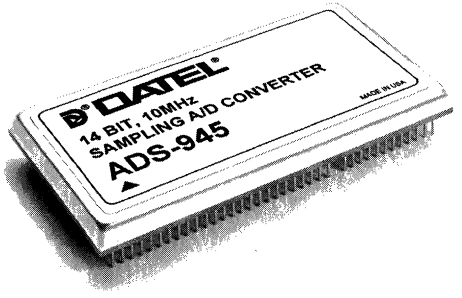
- Low cost!
- Outstanding value!
- Extremely low power, 1.1 Watts
- Small, 32-pin, ceramic, side-brazed TDIP package
- Guaranteed 1MHz sampling rate
- No missing codes over temperature
- Sampling to Nyquist frequencies
- Impressive dynamic performance:
  –84dB peak harmonics (f_{IN} = 500kHz)
  –82dB THD (f_{IN} = 500kHz)
  80dB SNR (f_{IN} = 500kHz)
- TTL compatible; Edge triggered
- Unipolar (0 to –10V) or bipolar (±5V) input
- Commercial and military temperature ranges

See page 1-111.

New Products

14-Bit Sampling A/D Converters

10MHz, Low Noise

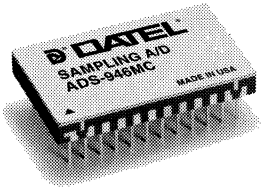


ADS-945

- Functionally complete, requires no external support circuitry
- 10MHz sampling rate guaranteed
- Low noise, 110µVrms
- Ideal for DSP/FFT signal processing
- Superb dynamic performance:
  –86dB peak harmonics (f_{IN} = 2.5MHz)
  –80dB THD (f_{IN} = 2.5MHz)
  78dB SNR (f_{IN} = 2.5MHz)
- No missing codes over temperature
- Commercial and military temperature ranges
- Low power, 4.2 Watts
- 100kΩ input impedance; ±1.25V input range
- Custom, low-profile, 2" x 4" DIP package
- TTL compatible

See page 1-151.

8MHz, 24-Pin DIP



ADS-946

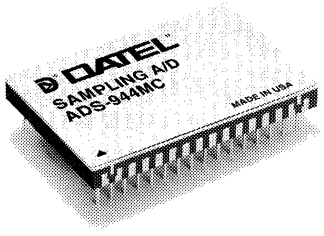
- A bonafide leading-edge product!
- Breaks all of today's performance/package/power barriers
- Functionally complete, requires no external support circuitry
- 8MHz sampling rate guaranteed
- Small, 24-pin, ceramic DDIP package
- ±5V supplies, 1.9 Watts; TTL compatible
- Low noise, 150µVrms
- Impressive dynamic performance:
  –83dB peak harmonics (f_{IN} = 500kHz)
  –81dB THD (f_{IN} = 500kHz)
  75dB SNR (f_{IN} = 500kHz)
- No missing codes over temperature
- Edge triggered; No pipeline delays
- ±2V input range
- Commercial and military temperature ranges
- MIL-STD-883 qualified (Q4 1996)

See page 1-159.

New Products

14-Bit Sampling A/D Converters

5MHz, Low Noise

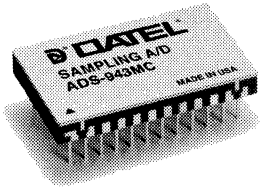


ADS-944

- Functionally complete,requires no external support circuitry
- 5MHz sampling rate guaranteed
- Small, 32-pin, ceramic TDIP package
- Low power, 2.95 Watts
- Low noise, 135µVrms
- No missing codes over temperature
- Edge triggered; No pipeline delays
- Excellent dynamic performance:
  –78dB peak harmonics (f_{IN} = 1MHz)
  –77dB THD (f_{IN} = 1MHz)
  76dB SNR (f_{IN} = 1MHz)
- Commercial and military temperature ranges
- ±1.25V input range; TTL compatible
- SMT packaging optional (J-lead)
- MIL-STD-883 qualified
- DESC SMD available

See page 1-143.

3MHz, Low Harmonics



ADS-943

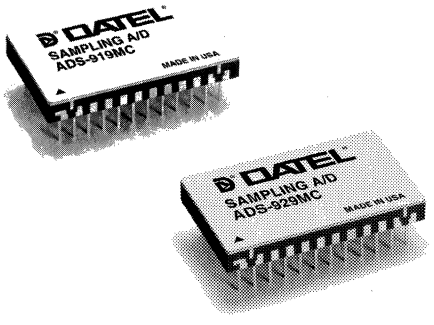
- Functionally complete, requires no external support circuitry
- 3MHz sampling rate guaranteed
- 24-pin DDIP package; ±5V supplies
- Low power, 1.9 Watts
- Low noise, 150µVrms
- Optimized for modern telecomm applications
- Impressive dynamic performance:
  –85dB peak harmonics (f_{IN} = 500kHz)
  –83dB THD (f_{IN} = 500kHz)
  –82dB two-tone IMD
  79dB SNR (f_{IN} = 500kHz)
- Edge triggered; No pipeline delays
- ±2V input range; TTL compatible
- Commercial and military temperature ranges
- No missing codes over temperature
- MIL-STD-883 qualified (Q4 1996)

See page 1-135.

New Products

14-Bit Sampling A/D Converters

2MHz, Great Value

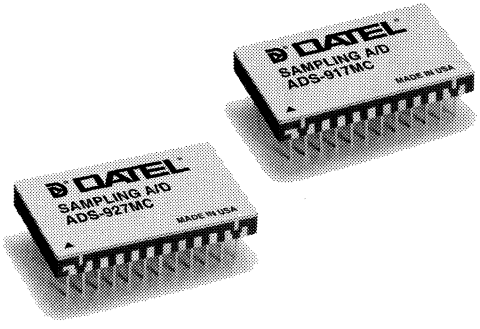


ADS-919, ADS-929

- Outstanding value — the best combination of performance, package, power and price
- Great for imaging applications!
- No missing codes over temperature
- Small, 24-pin, ceramic DDIP package
- Operates from either ±15V or ±12V supplies
- Low power, 1.4W with ±12V supplies
- Edge triggered; No pipeline delays
- Impressive dynamic performance:
  –80dB peak harmonics (f_{IN} = 1MHz)
  –78dB THD (f_{IN} = 1MHz)
  77dB SNR (f_{IN} = 1MHz)
- Unipolar (+10V, ADS-919) or bipolar (±5V, ADS-929) input
- Pin compatible with ADS-926/927 (0.5/1MHz)
- Gull-wing SMT package optional
- MIL-STD-883 qualified

See pages 1-55 and 1-79.

1MHz, Low Cost



ADS-917, ADS-927

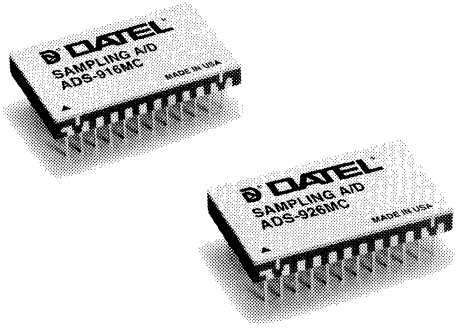
- Functionally complete
- Small, 24-pin, ceramic DDIP package
- Operates from either ±15V or ±12V supplies
- Low power, 1.4W with ±12V supplies
- No missing codes over temperature
- Solid dynamic performance:
  –82dB peak harmonics (f_{IN} = 500kHz)
  –80dB THD (f_{IN} = 500kHz)
  78dB SNR (f_{IN} = 500kHz)
- Edge triggered; No pipeline delays
- Unipolar (+10V, ADS-917) or bipolar (±5V, ADS-927) input
- Pin compatible with ADS-926/929 (0.5/2MHz sampling rates)
- Gull-wing SMT package optional
- MIL-STD-883 qualified

See pages 1-47 and 1-71.

New Products

Sampling A/D Converters

14-Bit, 500kHz

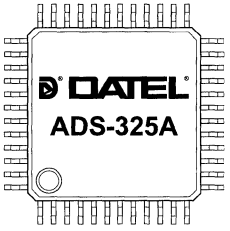


ADS-916, ADS-926

- Low Cost!
- Functionally complete
- Outstanding dynamic performance that surpasses many 16-bit A/D's:
  - –92dB peak harmonics (f_{IN} = 100kHz)
  - –90dB THD (f_{IN} = 100kHz)
  - 80dB SNR (f_{IN} = 100kHz)
- Small, 24-pin, ceramic DDIP package
- Operates from either ±15V or ±12V supplies
- Low power, 1.4 Watts with ±12V supplies
- No missing codes over temperature
- Unipolar (+10V, ADS-916) or bipolar (±5V, ADS-926) input
- Commercial and military temperature ranges
- Gull-wing SMT package optional
- MIL-STD-883 qualified

See pages 1-39 and 1-63.

10-Bit, 20MHz



ADS-325A

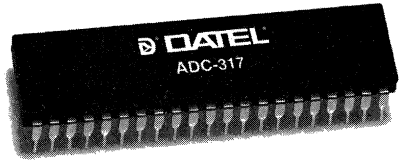
- Complete with input S/H amp and 3-state output latches
- Single-chip, autocalibrating, CMOS design
- Plastic, 48-pin, QFP package
- Single +5V supply; TTL compatible
- Low power consumption, 145mW
- Low input capacitance, 9pF
- Wide input bandwidth, 70MHz
- Excellent performance:
  - ±½LSB DNL
  - –65dB SFDR
  - 54dB SNR
  - –20 to +75°C operation

See page 1-31.

New Products

Flash A/D Converters

8-Bit, 125MHz

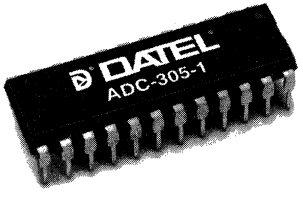


ADC-317

- Low cost!
- ±½LSB INL and DNL
- 46dB signal-to-noise ratio
- 200MHz full power input bandwidth
- No sparkle-code errors
- High input impedance, 190kΩ // 18pF
- ECL compatible
- Single –5.2V supply
- 870mW power consumption
- –20 to +75°C temperature range
- 42-pin plastic DDIP

See page 2-23.

8-Bit, 20MHz



ADC-305

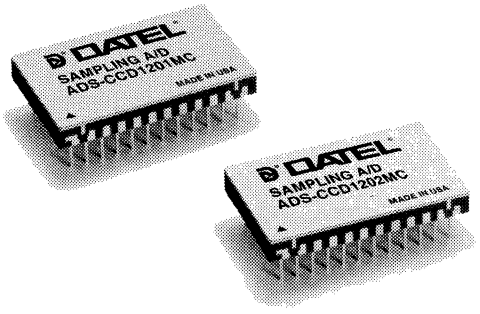
- 90mW max. power dissipation
- ±½LSB INL, ±0.3LSB DNL
- 46dB signal-to-noise ratio
- 60MHz input bandwidth
- Uses two-step parallel conversion technique
- Complete with internal:
  Reference (for 2V input)
  S/H amplifier
  Output data latches
- Single +5V supply; TTL compatible
- –20 to +75°C operation
- 24-pin plastic DIP or SOP

See page 2-18.

New Products

Application Specific for Imaging

1.2 and 2MHz, 12-Bit A/D's

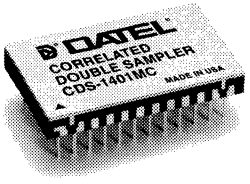


ADS-CCD1201, ADS-CCD1202

- Performance optimized for electronic imaging with CCD's
- Unipolar input range, 0 to +10V
- 4096-to-1 dynamic range
- Outstanding ±1/4LSB DNL
- Low noise: 400µVrms (1/6LSB, CCD1201)
  600µVrms (1/4LSB, CCD1202)
- Full scale step response (empty to full well) with ±1 count maximum error
- Operates from either ±15V or ±12V supplies
- 1.4 Watt power consumption
- Edge triggered; No pipeline delays
- Small, standard, 24-pin DDIP package
- See CDS front-end products
- Low cost!

See pages 1-167 and 1-175.

1-5MHz, CDS Front-Ends



CDS-1401, CDS-1402

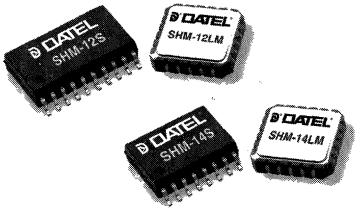
- Complete, single-package, CDS functions
- Subtract "kTC" noise for maximum dynamic range
- Use with most CCD's and high-speed A/D converters
- "Ping-pong" timing for high pixel rates and low noise
- High throughput in 14-bit applications:
  1.25MHz CDS-1401
  5MHz CDS-1402
- Extremely versatile:
  2 independent S/H circuits
  Gain matching
  4 offset adjustments
  4 A/D control lines
- Small, 24-pin DDIP package
- ±15V or ±5V supplies
- See A/D's optimized for imaging
- Low cost!

See pages 4-3 and 4-11.

New Products

Sample-Hold Amplifiers

High Speed, 12/14-Bit Linear



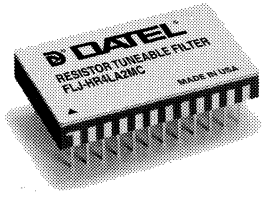
SHM-12, SHM-14

- Low cost!
- Single-chip, complementary bipolar design
- Very linear: ±0.006% SHM-12
  ±0.0012% SHM-14
- Very fast: 20nsec to ±0.012% SHM-12
  25nsec to ±0.012% SHM-14
- Wide bandwidth: 120MHz SHM-12
  250MHz SHM-14
- Low output noise, 65µVrms
- High feedthrough rejection, 80dB
- 1psec aperture jitter
- ±5V supplies, 300mW max. power
- Ceramic LCC or plastic SOIC packages
- Industrial and military temperature ranges
- Evaluation boards available

See pages 3-3 and 3-9.

Active Filters

Resistor Tunable



FLJ-HR Series

- fc (–3dB) variable to 1.6kHz or 100kHz
- fc selectable with only 4 resistors
- Lowpass, highpass and bandpass functions
- 4-pole and 2-pole models
- Cascadable
- Butterworth, Bessel, Cauer and Chebyshev characteristics
- 70dB minimum attenuation at 1MHz
- Small, 24-pin DIP package
- Industrial and military temperature ranges
- High-reliability screening optional

See page 9-3.

DATEL, Inc., 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For immediate assistance 800-233-2765

Selection Guides

Sampling Analog-to-Digital Converters

10-Bit and 12-Bit Resolution ①

Model ②	Sampling Rate (MHz)	Input Range(s) (Volts)	DNL (LSB)	No Missing Codes ③	SNR (dB)	THD (–dB)	Power Supplies (Volts)	Power Dissipation (Watts)	Package	MIL-STD-883 Screening	Page
ADS-325A	20	+2 to +4	±0.5	Yes	54	65	+5	0.15	48-Pin VQFP	No	1-31
ADS-112	1	±5, 0 to +10	±0.5	Yes	72	78	±15, +5	1.3	24-Pin DDIP	Yes	1-3
ADS-CCD1201④	1.2	0 to +10	±0.25	Yes	73	84	±15, +5	1.7	24-Pin DDIP	No	1-167
ADS-117	2	±5, 0 to +10	±0.5	Yes	70	73	±15, +5	1.6	24-Pin DDIP	Yes	1-9
ADS-CCD1202 ④	2	0 to +10	±0.25	Yes	71	78	±15, +5	1.7	24-Pin DDIP	No	1-175
ADS-118	5	±1	±0.5	Yes	69	71	±5	1.3	24-Pin DDIP	No	1-15
ADS-118A	5	±1.25	±0.5	Yes	69	71	±5	1.3	24-Pin DDIP	No	1-15
ADS-119	10	±1.5	±0.5	Yes	69	68	±5	1.8	24-Pin DDIP	Yes	1-23

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① The ADS-325A has 10-bit resolution. All other devices in this table are 12-bit converters.
② DATEL offers MC (0 to +70°C) and MM (–55 to +125°C) versions of each model. ③ Guaranteed over the full military temperature range (–55 to +125°C).
④ The ADS-CCD1201/2 have been optimized for electronic-imaging applications. They are pin-compatible and operate from either ±12V or ±15V supplies.

14-Bit Resolution

Model ①	Sampling Rate (MHz)	Input Range(s) (Volts)	DNL (LSB)	No Missing Codes ②	SNR (dB)	THD (–dB)	Power Supplies (Volts)	Power Dissipation (Watts)	Package	MIL-STD-883 Screening	Page
ADS-916 ③	0.5	0 to +10	±0.5	Yes	80	82	±15, +5	1.6	24-Pin DDIP	No	1-39
ADS-926 ③	0.5	±5	±0.5	Yes	80	87	±15, +5	1.6	24-Pin DDIP	Yes	1-63
ADS-917 ③	1	0 to +10	±0.5	Yes	78	80	±15, +5	1.7	24-Pin DDIP	No	1-47
ADS-927 ③	1	±5	±0.5	Yes	78	80	±15, +5	1.7	24-Pin DDIP	Yes	1-71
ADS-941	1	±5, 0 to +10	±0.5	Yes	78	83	±15, +5	2.8	32-Pin TDIP	No	1-117
ADS-919 ③	2	0 to +10	±0.5	Yes	77	76	±15, +5	1.7	24-Pin DDIP	No	1-55
ADS-929 ③	2	±5	±0.5	Yes	77	79	±15, +5	1.7	24-Pin DDIP	Yes	1-79
ADS-942	2	±5, 0 to +10	±0.5	Yes	75	80	±15, +5	2.9	32-Pin TDIP	No	1-123
ADS-942A	2	±5, 0 to +10	±0.5	Yes	75	80	±15, ±5	2.2	32-Pin TDIP	No	1-129
ADS-943	3	±2	±0.5	Yes	79	78	±5	1.8	24-Pin DDIP	Yes ④	1-135
ADS-944	5	±1.25	±0.5	Yes	76	77	±15, +5, –5.2	2.95	32-Pin TDIP	Yes	1-143
ADS-946	8	±2	±0.5	Yes	76	76	±5	1.9	24-Pin DDIP	Yes ④	1-159
ADS-945	10	±1.25	±0.5	Yes	78	80	±15, +5, –5.2	4.2	Custom DIP	No	1-151

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① DATEL offers MC (0 to +70°C) and MM (–55 to +125°C) versions of each model. ② Guaranteed over the full military temperature range (–55 to +125°C).
③ ADS-916, 917, 919, 926, 927 and 929 are all pin-compatible and operate from either ±12V or ±15V supplies. ④ Available Q4-96.

16-Bit Resolution

Model ①	Sampling Rate (MHz)	Input Range(s) (Volts)	DNL (LSB)	No Missing Codes ②	SNR (dB)	THD (–dB)	Power Supplies (Volts)	Power Dissipation (Watts)	Package	MIL-STD-883 Screening	Page
ADS-930	0.5	±5, 0 to –10	±0.5	Yes	83	89	±15, +5	3.5	40-Pin TDIP	No	1-87
ADS-931	1	±2.75	±0.5	Yes	87	89	±5	1.85	40-Pin TDIP	No	1-95
ADS-937	1	±5, 0 to –10	±0.5	Yes	84	85	±15, ±5	1.1	32-Pin TDIP	No	1-111
ADS-932	2	±2.75	±0.5	Yes	86	88	±5	1.85	40-Pin TDIP	No	1-103

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① DATEL offers MC (0 to +70°C) and MM (–55 to +125°C) versions of each model. ② Guaranteed over the full military temperature range (–55 to +125°C).

Selection Guides

Analog-to-Digital Converters

Model ①	Resolution (Bits)	Guaranteed Conversion Rate/Time	Differential Linearity Error, Max. (LSB)	Integral Linearity Error, Max. (LSB)	Input Range(s) (Volts)	Power Supplies (Volts)	Power Dissipation (mW)	Package ②	Page
ADC-207	7	20MHz	±0.5	±1	+5	+5	250	18-Pin DIP M 24-Pin CLCC M	2-3
ADC-228 ③	8	20MHz	±0.5	±0.5	+5	+5, ±15	1.5 ④	24-Pin DDIP H	2-9
ADC-304	8	20MHz	±0.5	±0.5	–2	+5 or ±5	355	28-Pin DDIP M	2-13
ADC-305	8	20MHz	±0.5	±0.5 ⑤	+2	+5	60	24-Pin DIP M	2-18
ADC-317	8	125MHz	±0.7	±0.8	–2	–5.2	870	42-Pin DDIP M	2-23
ADC-HZ	12	8µs	±0.75	±0.5	+5/10, ±2.5/5/10	+5, ±15	1.1 ④	32-Pin TDIP H	2-28
ADC-HX	12	20µs	±0.75	±0.5	+5/10, ±2.5/5/10	+5, ±15	1.1 ④	32-Pin TDIP H	2-28

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① MIL-STD-883 screening available on all models except ADC-304/305/317.
② M = Monolithic, H = Multi-chip-module hybrid. ③ The ADC-228 is a "complete" flash A/D with reference, input buffer, 3-state output, etc.
④ Watts. ⑤ Listed specification is a typical.

Sample-Hold Amplifiers

Model ①	Acquisition Time to ±0.01% (nsec)	Linearity (%)	Aperture Jitter (psec)	Input Range (Volts)	Gain	Small Signal Bandwidth (MHz)	Hold-Mode Droop Rate (µV/µsec)	Power Supplies (Volts)	Power Dissipation (mW)	Package ②	Page
SHM-12	20	±0.01	1	±1.5	+1	120	±500	±5	250	20-Pin SOIC M 20-Pin CLCC M	3-3
SHM-14	25	±0.002	1	±2.5	+1	250	±2000	±5	250	16-Pin SOIC M 20-Pin CLCC M	3-9
SHM-43	25	±0.01	1	±1	+1	150	±1	±5, +15	545	14-Pin DIP H	3-21
SHM-49	160	±0.01	25	±10	–1	16	±0.5	+5, ±15	365	8-Pin DIP H	3-27
SHM-4860	160	±0.01	50	±10	–1	16	±0.5	+5, ±15	730	24-Pin DDIP H	3-24
SHM-945	275 ③	±0.0004	10	±10	–1	16	±0.5	+5, ±15	305	24-Pin DDIP H	3-30
SHM-30C	650	±0.01	100	±10	+1	4.5	±0.01	±15	735	14-Pin DIP M	3-18
MSH-840 ④	775	±0.01	15	±10	+1/10	13	±1.5	+5, ±15	2.25 ⑤	32-Pin TDIP H	3-33
SHM-20C	1000	±0.01	300	±10	+1	2	±0.08	±15	330	14-Pin DIP M	3-15

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① High-reliability screening available on all models except SHM-20C and SHM-30C. ② M = Monolithic, H = Multi-chip-module hybrid.
③ to ±0.003%. ④ The MSH-840 is a quad simultaneous S/H (SSH) with built-in output multiplexer. ⑤ Watts.

Correlated Double Sampling Circuits

Model	Minimum Guaranteed Pixel Rate (MHz) ①	Full Scale Input Range (Volts)	Broadband Noise (µVrms)	Dynamic Range (dB)	Signal Acquisition Time (nsec)	Hold-Mode Droop Rate (mV/µsec)	Power Supplies (Volts)	Power Dissipation (mW)	Package	Page
CDS-1401	1.25	±10	200	91	250 ②	±0.004	+5, ±15	700	24-Pin DDIP	4-3
CDS-1402	5	±2.5	200	79	65 ③	±5	±5	350	24-Pin DDIP	4-11

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① When used in a 14-bit application. Higher throughputs obtainable at lower resolutions.
② 5V step acquired to ±1mV accuracy. ③ 2V step acquired to ±1mV accuracy.

Selection Guides

Analog Multiplexers

Model	Channels	Settling Time to ±0.01% (µsec)	Access Time (nsec)	Input Range (Volts)	On Resistance (Ohms)	Input Leakage		Power Supplies (Volts)	Maximum Power Dissipation (mW)	Package ①	Page
						Off Channel (pA)	On Channel (pA)				
MX-850	4SE	0.04 ②	20	±10	90	20	400	+5, ±15	270	14-Pin DIP H	5-21
MX-826 ④	8SE	0.150 ③	20	±10	2500	—	—	+5, ±15	575	24-Pin DDIP H	5-18
MX-1616C	16SE/8D	0.8	130	±15	750	10	40	±15	900	28-Pin DDIP M	5-13
MX-818C	8SE/4D	0.8	130	±15	750	10	15	±15	540	18-Pin DIP M	5-13
MV-1606	16SE	2.4	300	±15	270	30	1000	±15	60	28-Pin DDIP M	5-3
MVD-807	8D	2.4	300	±15	270	30	1000	±15	60	28-Pin DDIP M	5-3
MV-808	8SE	2.8	350	±15	250	20	100	+5, ±15	28	16-Pin DIP M	5-3
MVD-409	4D	2.8	350	±15	250	20	50	+5, ±15	28	16-Pin DIP M	5-3
MX-1606	16SE	3.5	500	±15	1500	30	100	±15	45	28-Pin DDIP M	5-8
MX-808	8SE	3.5	500	±15	1500	30	100	±15	45	16-Pin DIP M	5-8
MXD-409	4D	3.5	500	±15	1500	30	100	±15	45	16-Pin DIP M	5-8
MXD-807	8D	3.5	500	±15	1500	30	100	±15	45	28-Pin DDIP M	5-8

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① M = Monolithic, H = Multi-chip-module hybrid. ② 80ns to ±0.001%. ③ 300ns to ±0.003%. ④ MIL-STD-883 models available.

Digital-to-Analog Converters

Model ①	Resolution (Bits)	Settling Time (µsec)	Output	Differential Linearity Error, Max. (LSB)	Integral Linearity Error, Max. (LSB)	Coding	Power Supplies (Volts)	Maximum Power Dissipation (mW)	Package ②	Page
DAC-HF8B	8	0.025	+5, ±2.5mA	±0.5	±0.5	Bin	±15	750	24-Pin DDIP H	6-3
DAC-HF10B	10	0.025	+5, ±2.5mA	±0.5	±0.5	Bin	±15	825	24-Pin DDIP H	6-3
DAC-HF12B	12	0.05	+5, ±2.5mA	±0.5	±0.5	Bin	±15	975	24-Pin DDIP H	6-3
DAC-HK12B	12	3	+5/10, ±2.5/5/10V	±0.75	±0.5	Bin, 2C	+5, ±15	1000 ②	24-Pin DDIP H	6-7
DAC-HZ12B	12	3	+5/10, ±2.5/5/10V	±0.75	±0.5	CBin	±15	500	24-Pin DDIP H	6-15
DAC-HZ12D	3-Digit	3	+2.5/5/10V	±0.25	±0.25	CBCD	±15	500	24-Pin DDIP H	6-15
DAC-HP16B	16	15	+10, ±5/10V	±2	±2	CBin	±15	675 ②	24-Pin DDIP H	6-11

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① MIL-STD-883 models available for all listed products except DAC-HZ Series. ② H = Multi-chip-module hybrid. ③ Typical.

Operational Amplifiers

Model	Open Loop Gain (000)	Gain Bandwidth Product (MHz)	Slew Rate (V/µsec)	Input Offset Voltage (mV)	Offset Voltage Drift (µV/°C)	Input Bias Current (nA)	Output (±V@±mA)	Power Dissipation (±V@±mA)	Package	Page
AM-500	1000	130	±1000	±0.5	±1	±1	10/50	15/22	14-Pin DIP	7-7
AM-1435	100	1000	±300	±2	±5	±20µA	7/14	15/22	14-Pin DIP	7-3

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.

Selection Guides

Instrumentation Amplifiers

Model	Input Impedance ($10^{12}\Omega$)	Slew Rate (V/µsec)	Settling Time, G=1 (µsec)	Gain	Gain Accuracy (%, Max.)	Gain Nonlinearity (%, Max.)	Input Offset Voltage (±mV, Max.)	Output (±V@±mA)	Power Dissipation (±V@±mA)	Package	Page
AM-551 ①	1 ②	±23	3	1-1000	±0.04	±0.01	1 x gain	11/5	15/27	16-Pin DIP	7-10

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① 2-stage design. Front-end gain is resistor programmable. Back-end gain of 1 or 10 is pin selectable.
② CMV = ±11V, CMRR = 100dB.

Single-Package Data Acquisition Systems

Model ①	Resolution (Bits)	Input Channels	Throughput Rate (kHz, Min.)	Differential Linearity Error, Max. (LSB)	Integral Linearity Error, Max. (LSB)	Total Harmonic Distortion (–dB)	No Missing Codes	Power Supplies (Volts)	Maximum Power Dissipation (Watts)	Package	Page
HDAS-16	12	16SE	50	±1	±1	—	–55 to +125°C	+5, ±15	1.25	62-Pin QDIP	8-3
HDAS-8	12	8D	50	±1	±1	—	–55 to +125°C	+5, ±15	1.25	62-Pin QDIP	8-3
HDAS-75	12	8SE	75	±1	±1	73	–55 to +125°C	+5, ±15	0.7	40-Pin DDIP	8-15
HDAS-76	12	4D	75	±1	±1	73	–55 to +125°C	+5, ±15	0.7	40-Pin DDIP	8-15
HDAS-528	12	8SE	400	±0.75	±0.75	73	–55 to +125°C	+5, ±15	3	40-Pin DDIP	8-10
HDAS-524	12	4D	400	±0.75	±0.75	73	–55 to +125°C	+5, ±15	3	40-Pin DDIP	8-10

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① MIL-STD-883 models available for all listed products except HDAS-524.

Tunable Active Filters

Model	Tuning Technique	Poles	Filter Type ①	Low Pass	High Pass	Band Pass	Band Reject	Rolloff (dB/Octave)	Frequency Cutoff Range (f_C)	Package	Page
FLT-U2 ②	Resistors	2	BU, CH, BE, CA	X	X	X		12	0.001Hz-200kHz	16-Pin DDIP	9-11
FLJ-D Series	3-Digit BCD	2	BU, CH, BE	X	X	X	X	12	0.1Hz-160kHz	40-Pin QDIP	9-2
FLJ-UR Series	Resistors	2, 4	BU, CH	X	X	X	X	12, 24, 42	40Hz-20kHz	20-Pin SIP	9-2
FLJ-V Series	Voltage	4	BU	X	X	X		12, 24	20Hz-100kHz	40-Pin QDIP	9-2
FLJ-HR Series ③	Resistors	2, 4	BU, CH, BE, CA	X	X	X		12, 24, 42	10Hz-100kHz	24-Pin DDIP	9-3
FLJ-D5/D6	3-Bit Binary	5, 6	CH	X				60, 80	10Hz-20kHz	40-Pin QDIP	9-2
FLJ-R Series	Resistors	6, 8	CA	X		X		100, 135	10Hz-20kHz	40-Pin QDIP	9-2

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① BU = Butterworth, BE = Bessel, CA = Cauer/elliptical, CH = Chebyshev
② Commercial and military temperature ranges available.
③ High-reliability and military temperature range models available.

Quality Assurance

MIL-STD-1772
Certified and Qualified

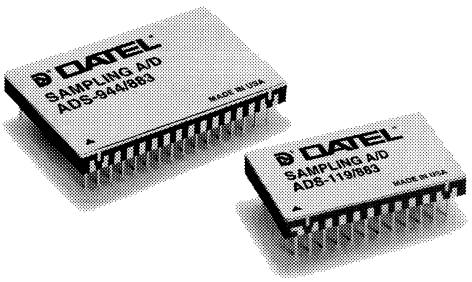
Military and High-Reliability Screening

As other suppliers rapidly exit the military components business, DATEL remains steadfastly committed to supporting our military/aerospace customers. Our commitment is evidenced by the fact we recently completed MIL-STD-883 qualifications for a number of our popular, high-performance sampling A/D converters. Our newest devices are now in the qualification process, and our extremely popular ADS-944 (14-Bit, 5MHz Sampling A/D Converter) is now covered by a DESC SMD.

DATEL remains on QML-38534 (the Qualified Manufacturers List) as we maintain our hybrid facility's MIL-STD-1772 certification. We routinely design, develop, manufacture and screen thick and thin-film chip-and-wire assemblies (nowadays called multi-chip-modules or MCM's) in full compliance with the demanding requirements of MIL-PRF-38534 and MIL-STD-883.

Continuous Improvement

Our overall Company, including our engineering-design functions, our Quality System, and our MCM, SMT and pcb assembly areas, is now ISO-9001 Registered! Not satisfied with this recent achievement, we are actively working to institute an enhanced Reliability Policy/Program that installs design-for-reliability practices earlier in our design cycles. Our standard in-house qualification programs now include HALT (highly accelerated life testing). Our new Qualmark HALT tester combines temperature and voltage extremes with 6-axis vibration to efficiently detect design weaknesses long before products enter the market.



Cost Savings for You!

DATEL recognizes that governments and military contractors are exploring ways to reduce the expense of many military programs, including lowering the cost of purchased components. In response to this need, we now offer a cost-effective alternative to full "883" processing. DATEL's "QL" program removes some of the more expensive aspects of "883" while maintaining its most important elements (burn-in, temperature cycling, hermeticity testing etc.).

The "QL" program is extremely flexible and can be customized to meet your specific cost/reliability objectives. Our Quality Assurance Team stands ready to work with you.

The first table on the following page summarizes MIL-STD-883 screening and the DATEL "QL" Program. Some test conditions are slightly different for "QL" screening. The second table lists the DATEL data acquisition components currently available with MIL-STD-883 screening. Most DATEL products are available with "QL" screening.

Contact us directly if you have any questions.

Quality Assurance *(continued)*

MIL-STD-883 and DATEL "QL" Screening

883 Operation/Test	Method	Conditions	DATEL QL
Incoming Inspection	MIL-PRF-38534		Yes
Element Evaluation	MIL-PRF-38534		No
Wire Bond Pull	2011	Destructive/Nondestructive, In Process (Sample)	Yes
Internal Visual (Precap)	2017	100%	Yes
Temperature Cycling	1010	Test Condition C, –65 to +150°C, 100%	Yes
Constant Acceleration	2001	Test Condition A, Y Axis, 5kg, 100%	Yes
PIND	2020	Test Condition B	As Required
Pre-Burn-in Electrical	—	100%	Yes
Burn-in	1015	Test Condition B, 160hrs. @ +125°C, 100%	Yes
PDA	—	10%	Yes
Final Electrical	Static & Dynamic	Performed @ –55, +25 and +125°C, 100%	Yes
Seal (Fine and Gross Leak)	1014	Test Condition A (Fine), 100%	Yes
		Test Condition C (Gross), 100%	Yes
External Visual	2009	100%	Yes
Group A	MIL-PRF-38534		As Required
Group B	MIL-PRF-38534		As Required
Group C	MIL-PRF-38534		As Required
Group D	MIL-PRF-38534		As Required

MIL-STD-883 Products	Description	DESC Drawing
ADS-111/883	12-Bit, 500kHz Sampling A/D Converter	—
ADS-112/883	12-Bit, 1MHz Sampling A/D Converter	—
ADS-117/883	12-Bit, 2MHz Sampling A/D Converter	—
ADS-119/883	12-Bit, 10MHz Sampling A/D Converter	
ADS-132/883	12-Bit, 2MHz Sampling A/D Converter	—
ADS-926/883	14-Bit, 500kHz Sampling A/D Converter	—
ADS-927/883	14-Bit, 1MHz Sampling A/D Converter	5962-9475701
ADS-929/883	14-Bit, 2MHz Sampling A/D Converter	—
ADS-944/883	14-Bit, 5MHz Sampling A/D Converter	5962-9319801
ADC-HZ12B/883	12-Bit, 8µsec A/D Converter	5962-8850802
ADC-HX12B/883	12-Bit, 20µsec A/D Converter	5962-8850801
ADC-816/883	10-Bit, 800nsec A/D Converter	—
ADC-511/883	12-Bit, 1µsec A/D Converter	—
ADC-228/883	8-Bit, 20MHz, Complete Flash A/D Converter	—
ADC-208/883	8-Bit, 20MHz, Flash A/D Converter	—
ADC-207/883	7-Bit, 20MHz, Flash A/D Converter	—
DAC-HZ12B/883	12-Bit, 3µsec, Voltage-Output D/A Converter	—
DAC-HP16B/883	16-Bit, 15µsec, Voltage-Output D/A Converter	5962-8953101
DAC-HK12B/883	12-Bit D/A Converter with Input Register	5962-8952801
DAC-HF12/883	12-Bit, 50nsec, Current-Output D/A Converter	—
DAC-HF10/883	12-Bit, 25nsec, Current-Output D/A Converter	—
DAC-HF8/883	10-Bit, 25nsec, Current-Output D/A Converter	—
HDAS-76/883	12-Bit, 75kHz, 4-Channel Data Acquisition System	—
HDAS-75/883	12-Bit, 75kHz, 8-Channel Data Acquisition System	—
HDAS-16/883	12-Bit, 50kHz, 16-Channel Data Acquisition System	5962-8851404
HDAS-8/883	12-Bit, 50kHz, 8-Channel Data Acquisition System	5962-8851403
HDAS-528/883	12-Bit, 400kHz, 8-Channel Data Acquisition System	—
MX-826/883	Precision, 8-Channel, High-Speed Multiplexer	5962-9450601
SHM-4860/883	200nsec, ±0.01% Sample-Hold Amplifier	—

Sampling A/D Converters

Incomparable combinations of high performance, small size, low power and affordable pricing define DATEL's unrivaled offering of Sampling A/D Converters. Virtually every new product we announce is a fully functional, easy-to-use device whose overall "value" instantly catapults it to the head of its speed class.

The advantages DATEL products offer are the result of years of engineering experience, an in-depth understanding of customer applications, and a multi-chip, mixed-technology assembly process (referred to as multi-chip-module or MCM technology). Our MCM technology combines integrated circuits fabricated from different semiconductor process technologies (bipolar, CMOS, biCMOS, etc.) with thick and thin-film passive elements into a single-package "seamless" function that exploits the most desirable aspects of each technology (high speed, low power, etc.). It is not limited by the unavoidable compromises inherent to any single technology.

MCM technology gives us the potential for continual performance improvements. Equally important, it allows us to quickly develop application-specific devices or easily modify standard products to meet your unique requirements.

Our new 14 and 16-bit Sampling A/D's feature unmatched performance, package, power and price attributes. All are 100% statically and dynamically tested (using FFT's). Proprietary, error-correcting and auto-calibration circuits enable each device to achieve specified performance over both 0 to +70°C and –55 to +125°C temperature ranges. Exhibiting *both* low noise (excellent DNL, high SNR) and wide bandwidth (low THD), these new A/D's excel in both time-domain (electronic imaging) and frequency-domain (digital communications) applications

These superior products are available *now*! Guarantee the future success of your design by choosing a DATEL Sampling A/D Converter today!

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Selection Guides

Sampling Analog-to-Digital Converters

10-Bit and 12-Bit Resolution ①

Model ②	Sampling Rate (MHz)	Input Range(s) (Volts)	DNL (LSB)	No Missing Codes ③	SNR (dB)	THD (–dB)	Power Supplies (Volts)	Power Dissipation (Watts)	Package	MIL-STD-883 Screening	Page
ADS-325A	20	+2 to +4	±0.5	Yes	54	65	+5	0.15	48-Pin VQFP	No	**1-31**
ADS-112	1	±5, 0 to +10	±0.5	Yes	72	78	±15, +5	1.3	24-Pin DDIP	Yes	**1-3**
ADS-CCD1201④	1.2	0 to +10	±0.25	Yes	73	84	±15, +5	1.7	24-Pin DDIP	No	**1-167**
ADS-117	2	±5, 0 to +10	±0.5	Yes	70	73	±15, +5	1.6	24-Pin DDIP	Yes	**1-9**
ADS-CCD1202④	2	0 to +10	±0.25	Yes	71	78	±15, +5	1.7	24-Pin DDIP	No	**1-175**
ADS-118	5	±1	±0.5	Yes	69	71	±5	1.3	24-Pin DDIP	No	**1-15**
ADS-118A	5	±1.25	±0.5	Yes	69	71	±5	1.3	24-Pin DDIP	No	**1-15**
ADS-119	10	±1.5	±0.5	Yes	69	68	±5	1.8	24-Pin DDIP	Yes	**1-23**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① The ADS-325A has 10-bit resolution. All other devices in this table are 12-bit converters.
② DATEL offers MC (0 to +70°C) and MM (–55 to +125°C) versions of each model. ③ Guaranteed over the full military temperature range (–55 to +125°C).
④ The ADS-CCD1201/2 have been optimized for electronic-imaging applications. They are pin-compatible and operate from either ±12V or ±15V supplies.

14-Bit Resolution

Model ①	Sampling Rate (MHz)	Input Range(s) (Volts)	DNL (LSB)	No Missing Codes ②	SNR (dB)	THD (–dB)	Power Supplies (Volts)	Power Dissipation (Watts)	Package	MIL-STD-883 Screening	Page
ADS-916 ③	0.5	0 to +10	±0.5	Yes	80	82	±15, +5	1.6	24-Pin DDIP	No	**1-39**
ADS-926 ③	0.5	±5	±0.5	Yes	80	87	±15, +5	1.6	24-Pin DDIP	Yes	**1-63**
ADS-917 ③	1	0 to +10	±0.5	Yes	78	80	±15, +5	1.7	24-Pin DDIP	No	**1-47**
ADS-927 ③	1	±5	±0.5	Yes	78	80	±15, +5	1.7	24-Pin DDIP	Yes	**1-71**
ADS-941	1	±5, 0 to +10	±0.5	Yes	78	83	±15, +5	2.8	32-Pin TDIP	No	**1-117**
ADS-919 ③	2	0 to +10	±0.5	Yes	77	76	±15, +5	1.7	24-Pin DDIP	No	**1-55**
ADS-929 ③	2	±5	±0.5	Yes	77	79	±15, +5	1.7	24-Pin DDIP	Yes	**1-79**
ADS-942	2	±5, 0 to +10	±0.5	Yes	75	80	±15, +5	2.9	32-Pin TDIP	No	**1-123**
ADS-942A	2	±5, 0 to +10	±0.5	Yes	75	80	±15, ±5	2.2	32-Pin TDIP	No	**1-129**
ADS-943	3	±2	±0.5	Yes	79	78	±5	1.8	24-Pin DDIP	Yes ④	**1-135**
ADS-944	5	±1.25	±0.5	Yes	76	77	±15, +5, –5.2	2.95	32-Pin TDIP	Yes	**1-143**
ADS-946	8	±2	±0.5	Yes	76	76	±5	1.9	24-Pin DDIP	Yes ④	**1-159**
ADS-945	10	±1.25	±0.5	Yes	78	80	±15, +5, –5.2	4.2	Custom DIP	No	**1-151**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① DATEL offers MC (0 to +70°C) and MM (–55 to +125°C) versions of each model. ② Guaranteed over the full military temperature range (–55 to +125°C).
③ ADS-916, 917, 919, 926, 927 and 929 are all pin-compatible and operate from either ±12V or ±15V supplies. ④ Available Q4-96.

16-Bit Resolution

Model ①	Sampling Rate (MHz)	Input Range(s) (Volts)	DNL (LSB)	No Missing Codes ②	SNR (dB)	THD (–dB)	Power Supplies (Volts)	Power Dissipation (Watts)	Package	MIL-STD-883 Screening	Page
ADS-930	0.5	±5, 0 to –10	±0.5	Yes	83	89	±15, +5	3.5	40-Pin TDIP	No	**1-87**
ADS-931	1	±2.75	±0.5	Yes	87	89	±5	1.85	40-Pin TDIP	No	**1-95**
ADS-937	1	±5, 0 to –10	±0.5	Yes	84	85	±15, ±5	1.1	32-Pin TDIP	No	**1-111**
ADS-932	2	±2.75	±0.5	Yes	86	88	±5	1.85	40-Pin TDIP	No	**1-103**

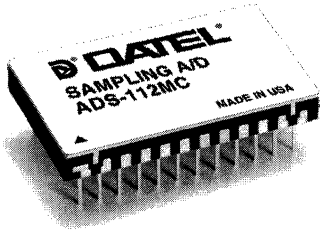
Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① DATEL offers MC (0 to +70°C) and MM (–55 to +125°C) versions of each model. ② Guaranteed over the full military temperature range (–55 to +125°C).

DATEL®
INNOVATION and EXCELLENCE

ADS-112
12-Bit, 1MHz, Low-Power Sampling A/D Converters

FEATURES

- **12-Bit resolution**
- **No missing codes**
- **1MHz minimum sampling rate**
- **Functionally complete**
- **Small 24-pin DDIP**
- **Low-power, 1.3 Watts**
- **Three-state output buffers**
- **Samples to Nyquist frequencies**



GENERAL DESCRIPTION

DATEL's ADS-112 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin DDIP. Requiring ±15V and +5V supplies, a minimum sampling rate of 1MHz is achieved while only dissipating 1.3 Watts. The ADS-112 digitizes signals up to Nyquist frequencies. Models are available for use in either commercial (0 to + 70°C) or military (–55 to +125°C) operating temperature ranges.

Typical applications include spectrum, transient, vibration and waveform analysis. This device is also ideally suited for radar, sonar, video digitization, medical instrumentation and high-speed data acquisition systems.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	24	–15V SUPPLY
2	BIT 11 OUT	23	ANALOG GROUND
3	BIT 10 OUT	22	+15V SUPPLY
4	BIT 9 OUT	21	+10V REFERENCE
5	BIT 8 OUT	20	BIPOLAR
6	BIT 7 OUT	19	ANALOG INPUT
7	BIT 6 OUT	18	$\overline{\text{COMP BIN}}$
8	BIT 5 OUT	17	$\overline{\text{ENABLE}}$ (1–12)
9	BIT 4 OUT	16	START CONVERT
10	BIT 3 OUT	15	$\overline{\text{EOC}}$
11	BIT 2 OUT	14	DIGITAL GROUND
12	BIT 1 OUT (MSB)	13	+5V SUPPLY

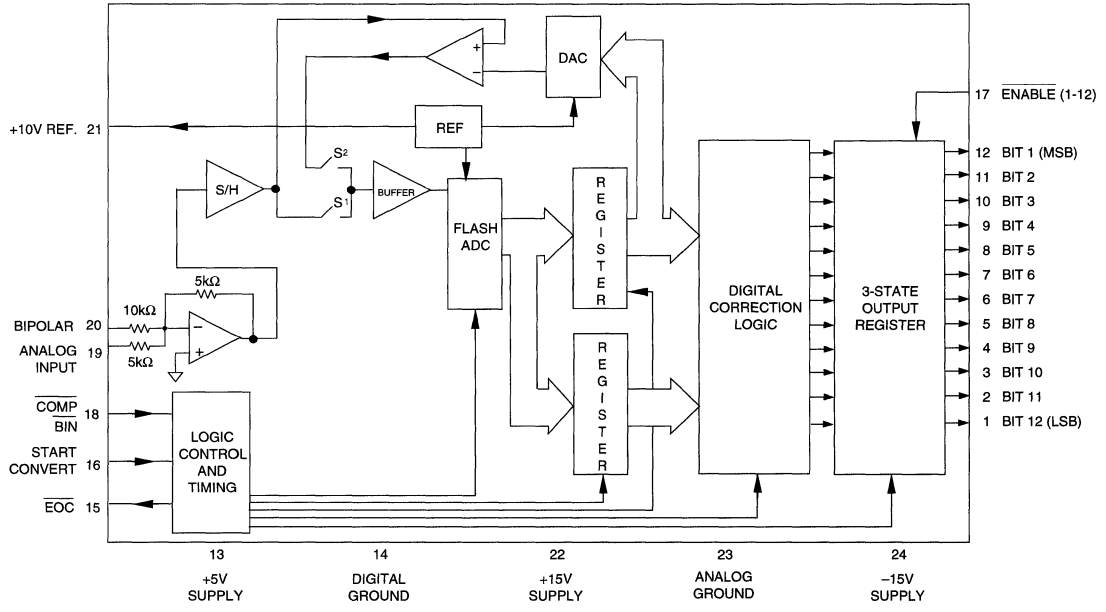


Figure 1. ADS-112 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts
–15V Supply (Pin 24)	0 to –18	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Inputs (Pins 16, 17, 18)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 19)	–9 to +15	Volts
Lead Temp. (10 seconds)	300	°C

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V, 1MHz sampling rate, and a minimum 1 minute warmup unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges ①				
Bipolar	—	±5	—	Volts
Unipolar	—	0 to +10	—	Volts
Input Resistance	4.5	5	—	kΩ
Input Capacitance	—	6	15	pF
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Loading "1"	—	—	+10	µA
Logic Loading "0"	—	—	–600	µA
A/D PERFORMANCE				
Resolution	12 Bits			
No Missing Codes (12 Bits; fin = 500kHz)	Over the operating temperature range.			
Integral Non-Linearity				
+25°C	—	±1/4	±3/4	LSB
0°C to +70°C	—	±1/4	±3/4	LSB
–55°C to +125°C	—	±1/2	±1.5	LSB
Differential Non-Linearity				
+25°C	—	±1/4	±3/4	LSB
0°C to +70°C	—	±1/4	±3/4	LSB
–55°C to +125°C	—	±1/2	±1	LSB
Full Scale Absolute Accuracy				
+25°C	—	±0.13	±0.25	%FSR
0°C to +70°C	—	±0.15	±0.44	%FSR
–55°C to +125°C	—	±0.25	±0.78	%FSR
Unipolar Zero Error †				
0°C to +70°C	—	±0.074	±0.265	%FSR
–55°C to +125°C	—	±0.224	±0.43	%FSR
Bipolar Zero Error †				
0°C to +70°C	—	±0.074	±0.166	%FSR
–55°C to +125°C	—	±0.124	±0.210	%FSR
Bipolar Offset Error †				
0°C to +70°C	—	±0.1	±0.38	%FSR
–55°C to +125°C	—	±0.3	±0.60	%FSR
Gain Error †				
0°C to +70°C	—	±0.1	±0.38	%
–55°C to +125°C	—	±0.3	±0.60	%
Internal Reference Voltage, +25°C	+9.98	+10.0	+10.02	Volts
Drift	—	±5	±30	ppm/°C
External Current	—	—	1.5	mA
DYNAMIC PERFORMANCE				
In-Band Harmonics (–0.5dB)				
dc to 100kHz	—	–81	–75	dB
100kHz to 500kHz	—	–75	–70	dB
Total Harm. Distort. (–0.5dB)				
dc to 100kHz	—	–78	–75	dB
100kHz to 500kHz	—	–73	–68	dB

† See Tech Note 1

DYNAMIC PERF. (Cont.)	MIN.	TYP.	MAX.	UNITS
Signal–to–Noise Ratio (w/o distort., –0.5dB)				
dc to 100kHz	68	72	—	dB
100kHz to 500kHz	67	71	—	dB
Signal–to–Noise Ratio ② (& distort., –0.5dB)				
dc to 100kHz	66	70	—	dB
100kHz to 500kHz	66	70	—	dB
Two–Tone Intermodulation Distort. (fin = 75kHz, 105kHz, fs = 1MHz, –7dB	—	–88	–80	dB
Two–Tone Intermodulation Distort. (fin = 480kHz, 490kHz, fs = 1MHz, –0.5dB)	—	–68	–65	dB
Input Bandwidth (–3dB)				
Small Signal (–20dB input)	8	10	—	MHz
Large Signal (–0.5dB input)	6	8	—	MHz
Slew Rate	—	±150	—	V/µs
Aperture Delay Time	—	—	20	ns
Effect. Aperture Delay Time	—	—	16	ns
Aperture Uncertainty (Jitter)				
RMS	—	—	15	ps
Peak	—	—	±50	ps
Overvoltage Recovery Time	—	—	1000	ns
S/H Acquisition Time	160	250	280	ns
Conversion Rate (Changing Inputs)				
+25°C	1	—	—	MHz
0°C to +70°C	1	—	—	MHz
–55°C to +125°C	1	—	—	MHz
DIGITAL OUTPUTS				
Output Coding				
Pin 18 High	Straight binary/offset binary			
Pin 18 Low	Complementary binary / Complementary offset binary			
Logic Levels				
Logic "1"	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	Volts
Logic Loading "1"	—	—	–160	µA
Logic Loading "0"	—	—	+6.4	mA
POWER REQUIREMENTS				
Power Supply Range ③				
+15V Supply	+14.25	+15.0	+15.75	Volts
–15V Supply	–14.25	–15.0	–15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Power Supply Current				
+15V Supply	—	+24	+35	mA
–15V Supply	—	–40	–48	mA
+5V Supply	—	+80	+95	mA
Power Dissipation	—	1.3	1.7	Watts
Power Supply Rejection	—	—	±0.07	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range, Case				
ADS-112MC	0	—	+70	°C
ADS-112MM, 883	–55	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	24–pin, metal-sealed, ceramic DDIP			
Weight	0.42 ounces (12 grams)			

① See Table 3 also.

② Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

③ For ±12V, +5V operation, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For Immediate Assistance 800-233-2765

TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-112 to zero using the optional external circuitry shown in Figure 4. The external adjustment circuit has no effect on the throughput rate.

2. For best performance, always connect the analog and digital ground pins to a ground plane beneath the converter. The analog and digital grounds are not connected to each other internally.

3. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with 4.7µF, 25V tantalum electrolytic capacitors in parallel with 0.1µF ceramic capacitors. Bypass the +10V reference (pin 21) to analog ground (pin 23).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 18) to +5V or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 18 to ground. The pin 18 signal is compatible with CMOS/TTL logic levels for those users desiring dynamic control of this function.

5. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). To disable, connect pin 17 to a logic "1" (high).

6. Do not change the status of pin 18 when $\overline{\text{EOC}}$ is high.

7. Re-initiating the START CONVERT (pin 16) while $\overline{\text{EOC}}$ is a logic "1" (high) will result in a new conversion sequence.

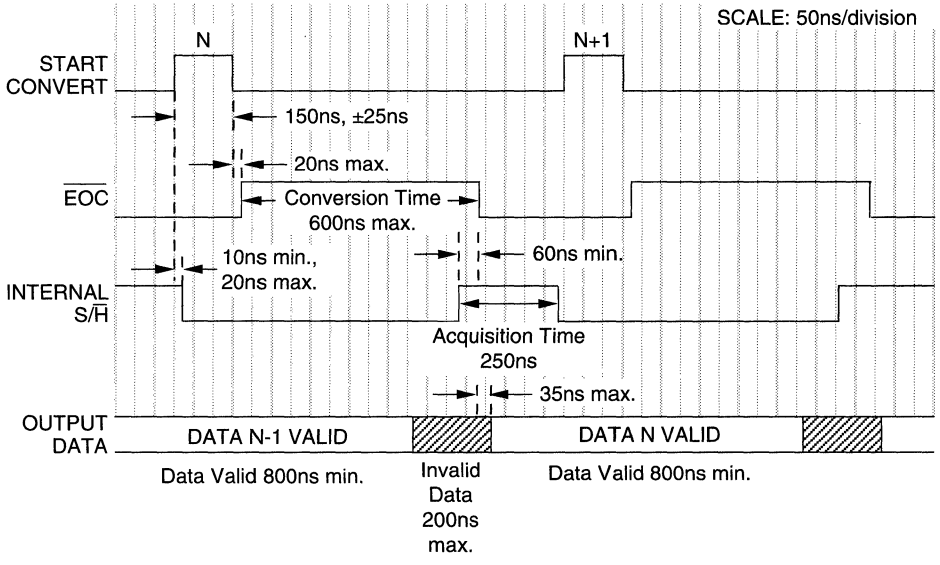


Figure 2. ADS-112 Timing Diagram

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

CALIBRATION PROCEDURE

1. Connect the converter per Figures 3 and 4 and Tables 1 and 3 for the appropriate input range. Apply a pulse of 150 nanoseconds to the START CONVERT input (pin 16) at a rate of 250kHz. This rate is chosen to reduce the flicker if LED's are used on the outputs for calibration purposes.

Table 1. Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
±5V	Pin 19	Pin 20 to Pin 21
0 to+10V	Pin 19	Pin 20 to Ground

2. **Zero Adjustments**
Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 2. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with $\overline{\text{COMP BIN}}$ (pin 18) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with pin 18 tied low (complementary binary).

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 18 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 18 tied low (complementary offset binary).

Table 2. Zero and Gain Adjust

INPUT RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V	+1.22mV	+9.9963V
±5V	+1.22mV	+4.9963V

3. **Full-Scale Adjustment**
Set the output of the voltage reference used in step 2 to the value shown in Table 2. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 18 tied high or between 0000 0000 0001 and 0000 0000 0000 for pin 18 tied low.

To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

Table 3. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	kΩ
0 to +5V, ±2.5V	2	6	kΩ
0 to +2.5V, ±1.25V	2	14	kΩ

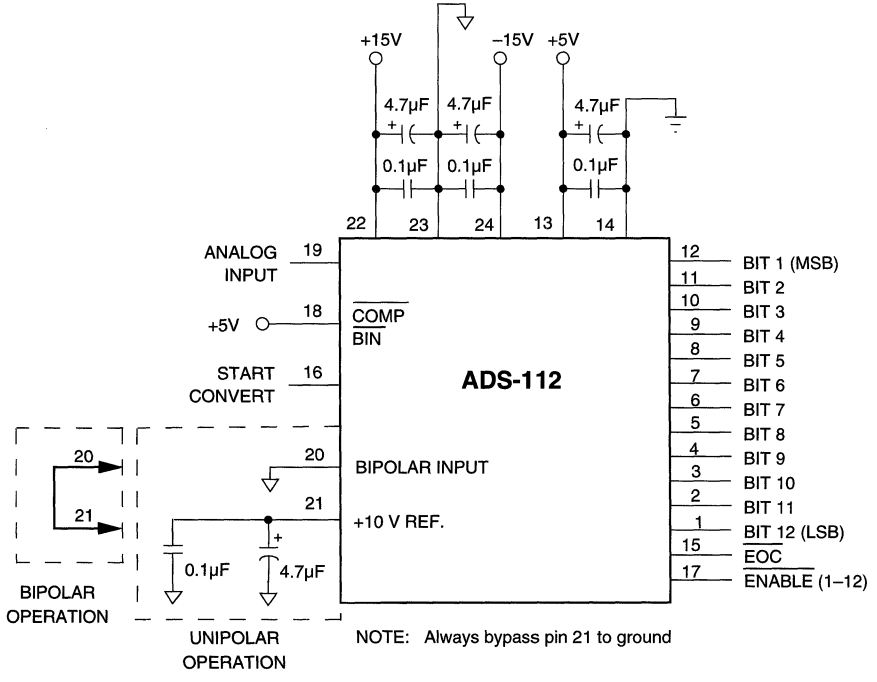


Figure 3. Typical ADS-112 Connection Diagram

Table 4. Output Coding

		STRAIGHT BIN.	COMP. BINARY		
UNIPOLAR	INPUT RANGE	OUTPUT CODING		INPUT RANGE	BIPOLAR
SCALE	0 to +10V	MSB LSB	MSB LSB	±5V	SCALE
+FS –1 LSB	+9.9976	1111 1111 1111	0000 0000 0000	+4.9976	+FS -1 LSB
+7/8 FS	+8.7500	1110 0000 0000	0001 1111 1111	+3.7500	+3/4 FS
+3/4 FS	+7.5000	1100 0000 0000	0011 1111 1111	+2.5000	+1/2 FS
+1/2 FS	+5.0000	1000 0000 0000	0111 1111 1111	0.0000	0
+1/4 FS	+2.5000	0100 0000 0000	1011 1111 1111	-2.5000	-1/2 FS
+1/8 FS	+1.2500	0010 0000 0000	1101 1111 1111	-3.7500	-3/4 FS
+1 LSB	+0.0024	0000 0000 0001	1111 1111 1110	-4.9976	-FS +1 LSB
0	0.0000	0000 0000 0000	1111 1111 1111	-5.0000	-FS
		OFF. BINARY	COMP. OFF. BIN.		

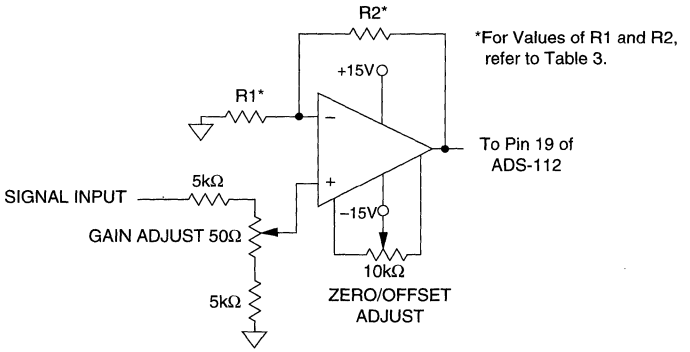


Figure 4. Optional Calibration Circuit

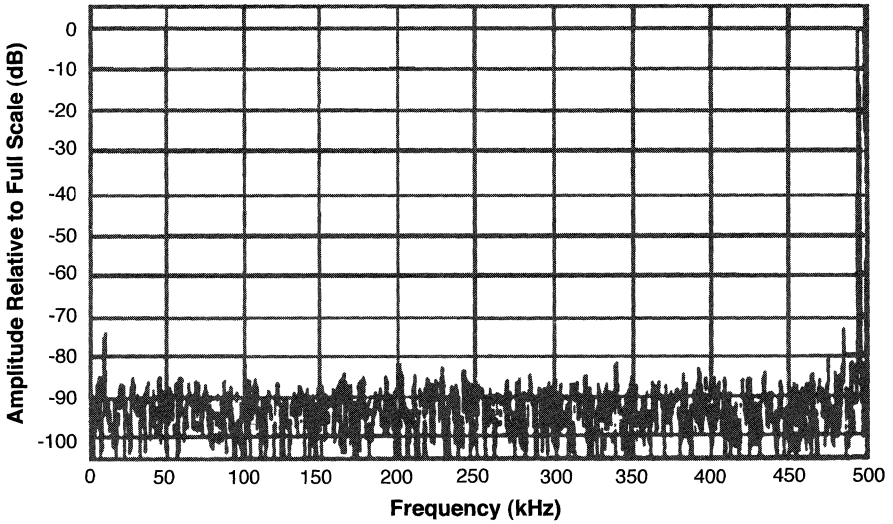
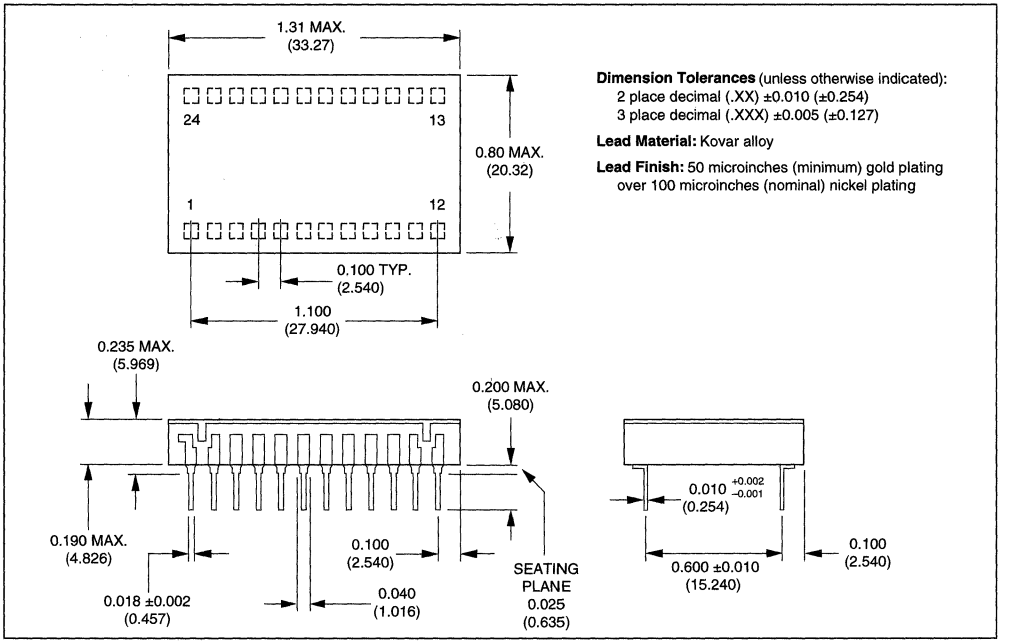


Figure 5. FFT Analysis of ADS-112

MECHANICAL DIMENSIONS
INCHES (mm)



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-112MC	0 to +70°C
ADS-112MM	–55 to +125°C
ADS-112/883	–55 to +125°C

For MIL-STD-883 product specification or availability of surface-mount packaging, contact DATEL.

ACCESSORIES

ADS-EVAL1	Evaluation board (without ADS-112)
HS-24	Heat sink for all ADS-112 models.

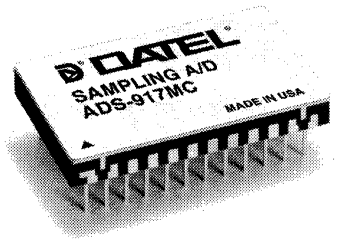
Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For Immediate Assistance 800-233-2765

ADS-117
12-Bit, 2MHz, Low-Power Sampling A/D Converters

FEATURES

- **12-Bit resolution**
- **No missing codes**
- **2MHz minimum throughput**
- **Functionally complete**
- **Small 24-pin DDIP**
- **Low-power, 1.6 Watts**
- **Three-state output buffers**
- **Samples to Nyquist frequencies**



GENERAL DESCRIPTION

DATEL's ADS-117 is a functionally complete, 12-bit, 2MHz, sampling A/D converter. Its standard, 24-pin, double-width DIP contains a fast-settling sample-hold amplifier, a 12-bit subranging (two-step) A/D converter, a precision reference, three-state output register and all the timing and control logic necessary to operate from a single start convert pulse. Digital input and output levels are TTL.

Total harmonic distortion (THD) and signal-to-noise ratio (including distortion) typically run –78dB and 70dB, respectively, with full scale inputs up to 100kHz. The ADS-117 requires ±15V and +5V power supplies and typically consumes 1.6 Watts. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	24	–15V SUPPLY
2	BIT 11 OUT	23	ANALOG GROUND
3	BIT 10 OUT	22	+15V SUPPLY
4	BIT 9 OUT	21	+10V REFERENCE
5	BIT 8 OUT	20	BIPOLAR
6	BIT 7 OUT	19	ANALOG INPUT
7	BIT 6 OUT	18	$\overline{\text{COMP BIN}}$
8	BIT 5 OUT	17	$\overline{\text{ENABLE}}$ (1–12)
9	BIT 4 OUT	16	START CONVERT
10	BIT 3 OUT	15	$\overline{\text{EOC}}$
11	BIT 2 OUT	14	DIGITAL GROUND
12	BIT 1 OUT (MSB)	13	+5V SUPPLY

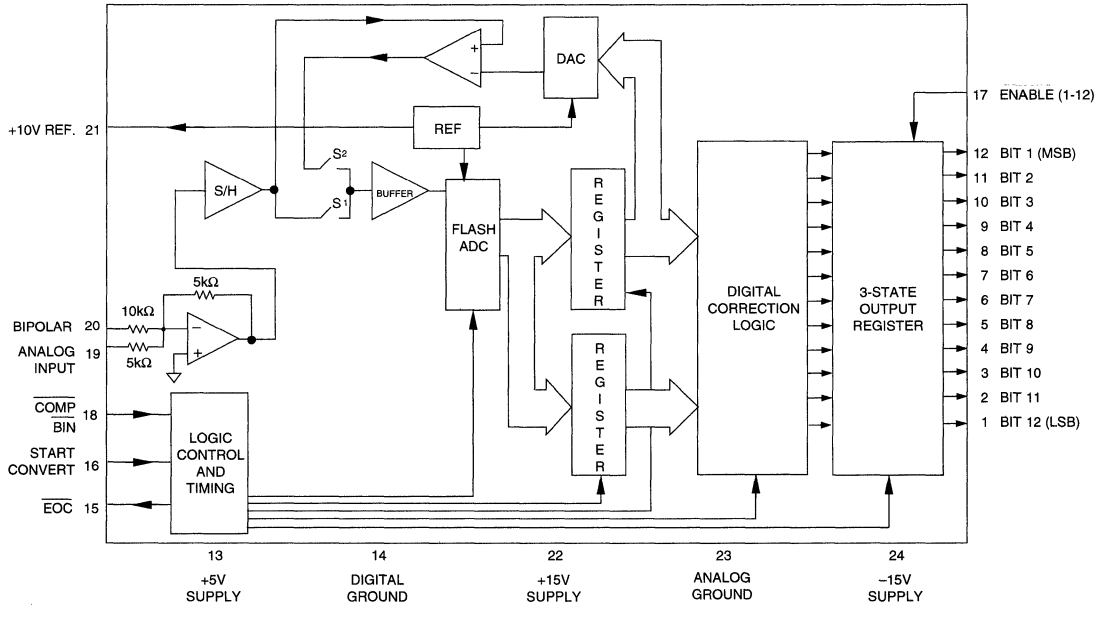


Figure 1. ADS-117 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +16	Volts
–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6.0	Volts
Digital Inputs (Pins 16, 17, 18)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 19)	–9 to +15	Volts
Lead Temp. (10 seconds)	300	°C

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = +15V, +V_{DD} = +5V, 2MHz sampling rate, and a minimum 3 minute warmup unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges ①				
Bipolar	—	±5	—	Volts
Unipolar	—	0 to +10	—	Volts
Input Resistance	4.5	5	—	kΩ
Input Capacitance	—	6	15	pF
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Loading "1"	—	—	+5	µA
Logic Loading "0"	—	—	–600	µA
PERFORMANCE				
Resolution	12 Bits			
No Missing Codes (12 Bits; fin = 1MHz)	0 to +70°C			
Integral Non–Linearity				
0°C to +70°C	—	±1/2	±2	LSB
–55°C to +125°C	—	±1	±3	LSB
Differential Non–Linearity				
0°C to +70°C	—	±1/2	±0.95	LSB
–55°C to +125°C	—	±1	±1.5	LSB
Full Scale Absolute Accuracy (see Tech Note 1)				
0°C to +70°C	—	±0.13	±0.44	%FSR
–55°C to +125°C	—	±0.25	±0.73	%FSR
Unipolar/Bipolar Zero Error				
0°C to +70°C (Tech. Note 1)	—	±0.07	±0.27	%FSR
–55°C to +125°C	—	±0.22	±0.73	%FSR
Bipolar Offset Error				
0°C to +70°C (Tech. Note 1)	—	±0.1	±0.38	%FSR
–55°C to +125°C	—	±0.53	±0.73	%FSR
Gain Error (See Tech. Note 1)				
0°C to +70°C	—	±0.1	±0.38	%
–55°C to +125°C	—	±0.53	±0.73	%
Internal Reference Voltage				
0°C to +70°C	+9.97	+10.0	+10.03	Volts
–55°C to +125°C	+9.95	—	+10.05	Volts
External Current	—	—	1.5	mA
DYNAMIC PERFORMANCE				
Spurious Free Dynamic Range (–0.5dB) ②				
dc to 100kHz	—	–81	—	dB
100kHz to 500kHz	—	–75	–70	dB
500kHz to 1MHz	—	–70	—	dB
Total Harm. Distort. (–0.5dB)				
dc to 100kHz	—	–78	—	dB
100kHz to 500kHz	—	–73	–68	dB
500kHz to 1MHz	—	–71	—	dB
Input Bandwidth (–3dB)				
Small Signal (–20dB input)	8	10	—	MHz
Large Signal (–0.5dB input)	7	9	—	MHz
Feedthrough (1MHz)	–72	–74	—	dB

① See Table 1 also.

DYNAMIC PERF. (Cont.)	MIN.	TYP.	MAX.	UNITS
SNR (w/o distortion, –0.5dB)				
dc to 100kHz				
0°C to +70°C	—	72	—	dB
–55°C to +125°C	—	72	—	dB
100kHz to 500kHz				
0°C to +70°C	65	70	—	dB
–55°C to +125°C	65	70	—	dB
500kHz to 1MHz				
0°C to +70°C	—	70	—	dB
–55°C to +125°C	—	70	—	dB
SNR (and distort., –0.5dB) ③				
dc to 100kHz				
0°C to +70°C	—	70	—	dB
–55°C to +125°C	—	69	—	dB
100kHz to 500kHz				
0°C to +70°C	64	70	—	dB
–55°C to +125°C	62	69	—	dB
500kHz to 1MHz				
0°C to +70°C	—	69	—	dB
–55°C to +125°C	—	69	—	dB
Two–Tone Intermodulation Distortion (fin = 970kHz, 990kHz, fs = 2MHz, –0.5dB)	—	–68	—	dB
Slew Rate	—	±210	—	V/µs
Effect. Aperture Delay Time	—	—	16	ns
Overvoltage Recovery Time; 20%	—	—	500	ns
S/H Acquisition Time to ±0.01%				
0 to +70°C	—	155	165	ns
–55°C to +125°C	—	160	170	ns
Conversion Rate	2	—	—	MHz
OUTPUTS				
Output Coding	Straight binary/offset binary			
Pin 18 High	Complementary binary			
Pin 18 Low	Complementary offset binary			
Logic Levels				
Logic "1"	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	Volts
Logic Loading "1"	—	—	–160	µA
Logic Loading "0"	—	—	+6.4	mA
POWER REQUIREMENTS				
Power Supply Range ④				
+15V Supply	+14.25	+15.0	+15.75	Volts
–15V Supply	–14.25	–15.0	–15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Power Supply Current				
+15V Supply	—	+48	+58	mA
–15V Supply	—	–35	–45	mA
+5V Supply	—	+75	+85	mA
Power Dissipation	—	1.6	1.9	Watts
Power Supply Rejection	—	—	±0.07	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range, Case				
ADS-117MC	0	—	+70	°C
ADS-117MM, 883	–55	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Thermal Impedance				
θjc	—	3	—	°C/W
θca	—	23	—	°C/W
Package Type	24–pin, metal-sealed, ceramic DDIP			
Weight	0.42 ounces (12 grams)			

② Same specifications for in-band harmonics.

③ Effective bits is equal to:

$$\frac{(\text{SNR} + \text{Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

④ For ±12V, +5V operation, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For Immediate Assistance 800-233-2765

TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-117 to zero using the optional external circuitry shown in Figure 4. The external adjustment circuit has no effect on the throughput rate.

2. Always connect the analog and digital grounds to a ground plane beneath the converter for best performance. The analog and digital grounds are not connected to each other internally.

3. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with 4.7µF, 25V tantalum electrolytic capacitors in parallel with 0.1µF ceramic capacitors. Bypass the +10V reference (pin 21) to ANALOG GROUND (pin 23).

4. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 18) to +5V or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 18 to ground. The pin 18 signal is compatible with CMOS/TTL logic levels for those users desiring dynamic control of this function. Do not change $\overline{\text{COMP BIN}}$ status while $\overline{\text{EOC}}$ is high.

5. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). To disable, connect pin 17 to a logic "1" (high).

6. To meet the guaranteed conversion rate, a maximum start convert pulse is specified. A wider start convert pulse will result in slower conversion rates. An initial start convert pulse is required before performing an actual conversion after power-up to assure the sample-hold is in the acquisition mode.

   Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range.

7. Re-initiating the START CONVERT (pin 16) while $\overline{\text{EOC}}$ is a logic "1" (high) will result in a new conversion sequence.

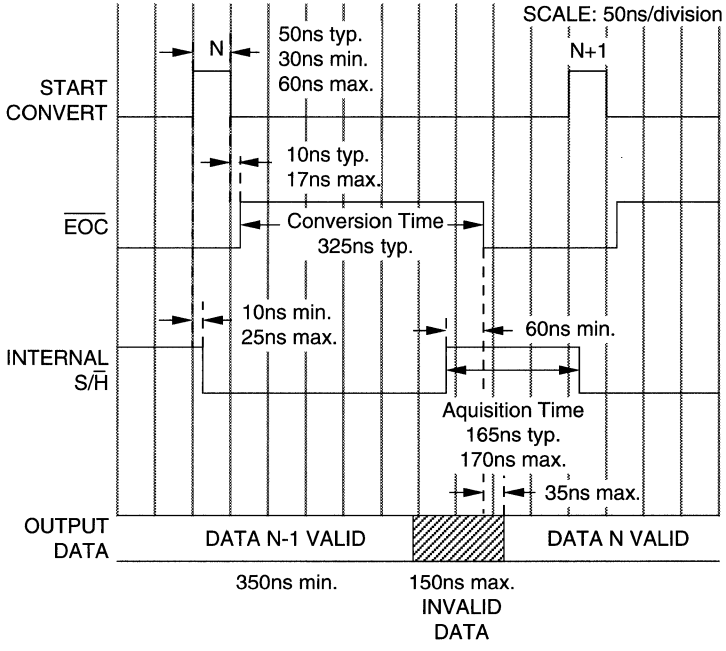


Figure 2. ADS-117 Timing Diagram

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, Figure 4, and Table 1 for the appropriate input range. Apply a pulse of 150 nanoseconds to the START CONVERT input (pin 16) at a rate of 250kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

Table 1. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	kΩ
0 to +5V, ±2.5V	2	6	kΩ
0 to +2.5V, ±1.25V	2	14	kΩ

2. **Zero Adjustments**
Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 2. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the pin 18 tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the pin 18 tied low (complementary binary).

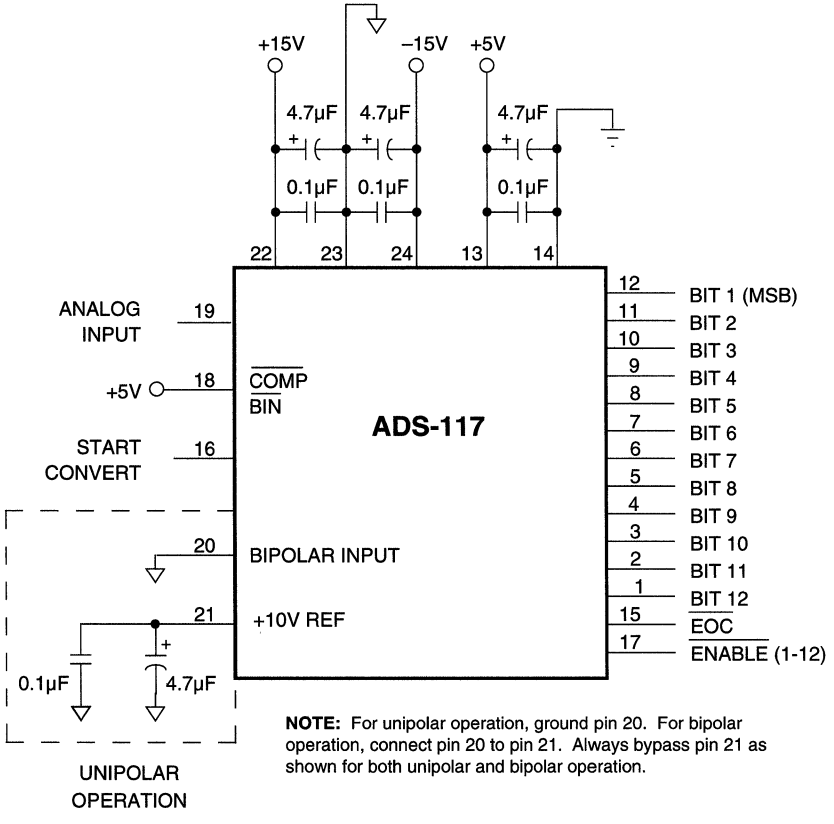
Table 2. Zero and Gain Adjust

INPUT RANGE	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V	+1.22mV	+9.9963V
±5V	+1.22mV	+4.9963V

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 18 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 18 tied low (complementary offset binary).

3. **Full-Scale Adjustment**
Set the output of the voltage reference used in step 2 to the value shown in Table 1. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 18 tied high or between 0000 0000 0001 and 0000 0000 0000 for pin 18 tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.



NOTE: For unipolar operation, ground pin 20. For bipolar operation, connect pin 20 to pin 21. Always bypass pin 21 as shown for both unipolar and bipolar operation.

Figure 3. ADS-117 Connection Diagram

Table 3. Output Coding

UNIPOLAR SCALE	INPUT RANGE 0 to +10V	STRAIGHT BIN. MSB LSB	COMP. BINARY MSB LSB	INPUT RANGE ±5V	BIPOLAR SCALE
+FS -1 LSB	+9.9976	1111 1111 1111	0000 0000 0000	+4.9976	+FS -1 LSB
+7/8 FS	+8.7500	1110 0000 0000	0001 1111 1111	+3.7500	+3/4 FS
+3/4 FS	+7.5000	1100 0000 0000	0011 1111 1111	+2.5000	+1/2 FS
+1/2 FS	+5.0000	1000 0000 0000	0111 1111 1111	0.0000	0
+1/4 FS	+2.5000	0100 0000 0000	1011 1111 1111	-2.5000	-1/2 FS
+1/8 FS	+1.2500	0010 0000 0000	1101 1111 1111	-3.7500	-3/4 FS
+1 LSB	+0.0024	0000 0000 0001	1111 1111 1110	-4.9976	-FS +1 LSB
0	0.0000	0000 0000 0000	1111 1111 1111	-5.0000	-FS
		OFF. BINARY	COMP. OFF. BIN.		

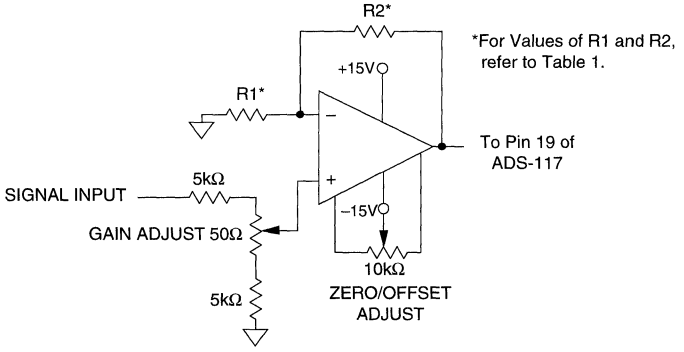


Figure 4. Optional Calibration Circuit

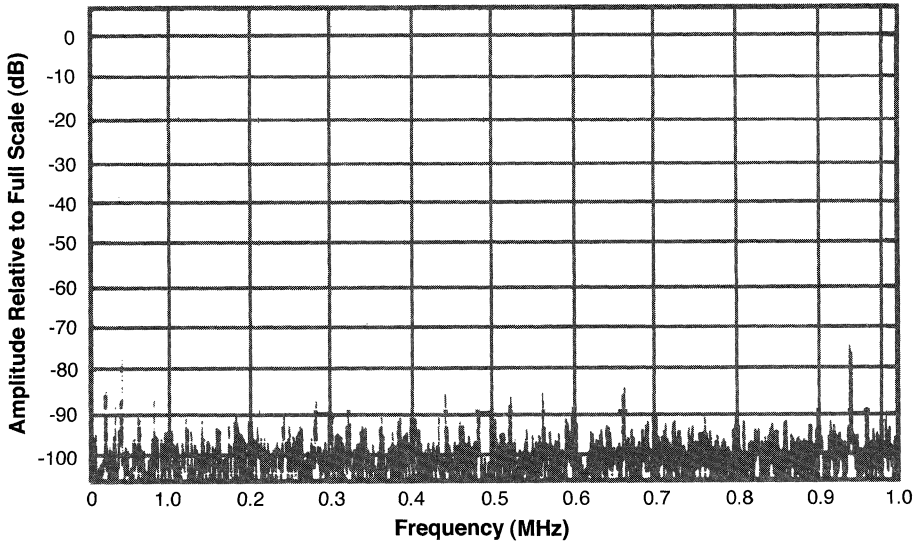
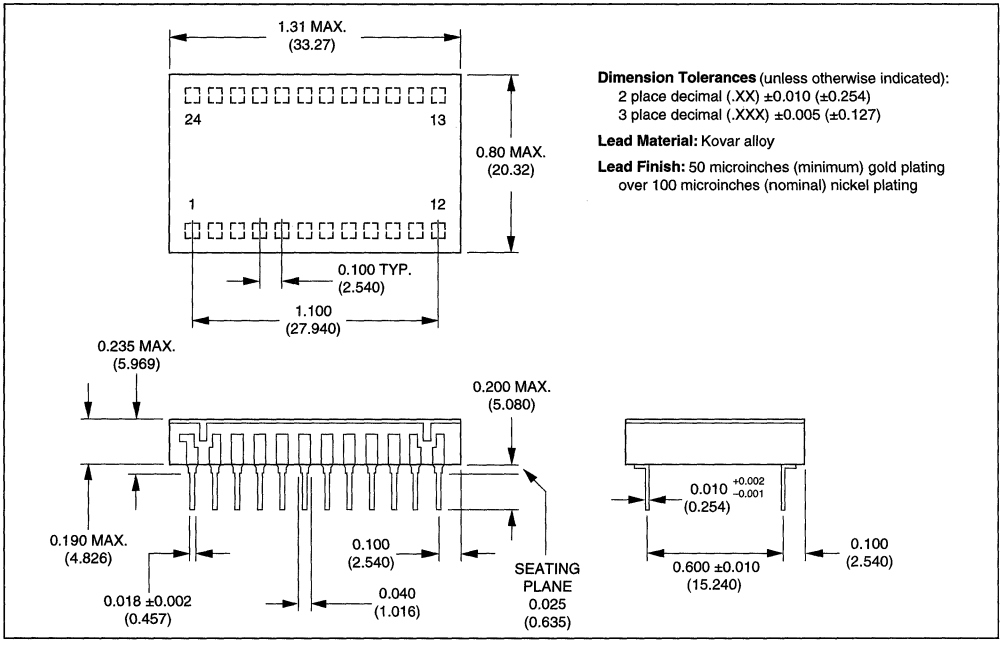


Figure 5. FFT Analysis of ADS-117
(4,096-point FFT, Blackman-Harris window
V_{in} = –0.5dB, f_{in} = 980kHz, f_s = 2MHz)

MECHANICAL DIMENSIONS
INCHES (mm)



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-117MC	0 to +70°C
ADS-117MM	–55 to +125°C
ADS-117/883	–55 to +125°C

For MIL-STD-883 product specification or availability of surface-mount packaging, contact DATEL.

ACCESSORIES

ADS-EVAL1	Evaluation board (without ADS-117)
HS-24	Heat sink for all ADS-117 models.

Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

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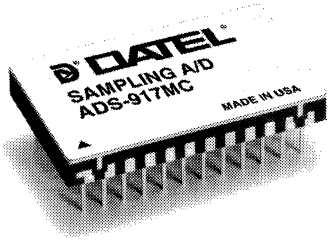
ADS-118, ADS-118A
12-Bit, 5MHz, Low-Power Sampling A/D Converters

FEATURES

- **12-Bit resolution**
- **5MHz minimum sampling rate**
- **Functionally complete**
- **Small 24-pin DDIP**
- **Requires only ±5V supplies**
- **Low-power, 1.3 Watts**
- **Outstanding dynamic performance**
- **No missing codes over full military temperature range**
- **Edge-triggered, no pipeline delay**
- **Ideal for both time and frequency-domain applications**



GENERAL DESCRIPTION

DATEL's ADS-118 and ADS-118A are 12-bit, 5MHz, sampling A/D converters packaged in space-saving 24-pin DDIP's. The ADS-118 offers an input range of ±1V and has three-state outputs. The ADS-118A has an input range of ±1.25V and features direct adjustment of offset error.

These functionally complete low-power devices (1.3 Watts) contain an internal fast-settling sample/hold amplifier, a 12-bit subranging A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. All timing and control logic operates from the rising edge of a single start convert pulse. Digital input and output levels are TTL. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges.

Applications include radar, transient signal analysis, process control, medical/graphic imaging, and FFT spectrum analysis.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	24	NO CONNECT
2	BIT 11	23	ANALOG GROUND
3	BIT 10	22	NO CONNECT
4	BIT 9	21	+5V ANALOG SUPPLY
5	BIT 8	20	–5V SUPPLY
6	BIT 7	19	ANALOG INPUT
7	BIT 6	18	ANALOG GROUND
8	BIT 5	17*	$\overline{\text{ENABLE}}$ /OFFSET ADJ.
9	BIT 4	16	START CONVERT
10	BIT 3	15	$\overline{\text{EOC}}$
11	BIT 2	14	DIGITAL GROUND
12	BIT 1 (MSB)	13	+5V DIGITAL SUPPLY

* ADS-118, Pin 17 is $\overline{\text{ENABLE}}$
ADS-118A, Pin 17 is OFFSET ADJUST

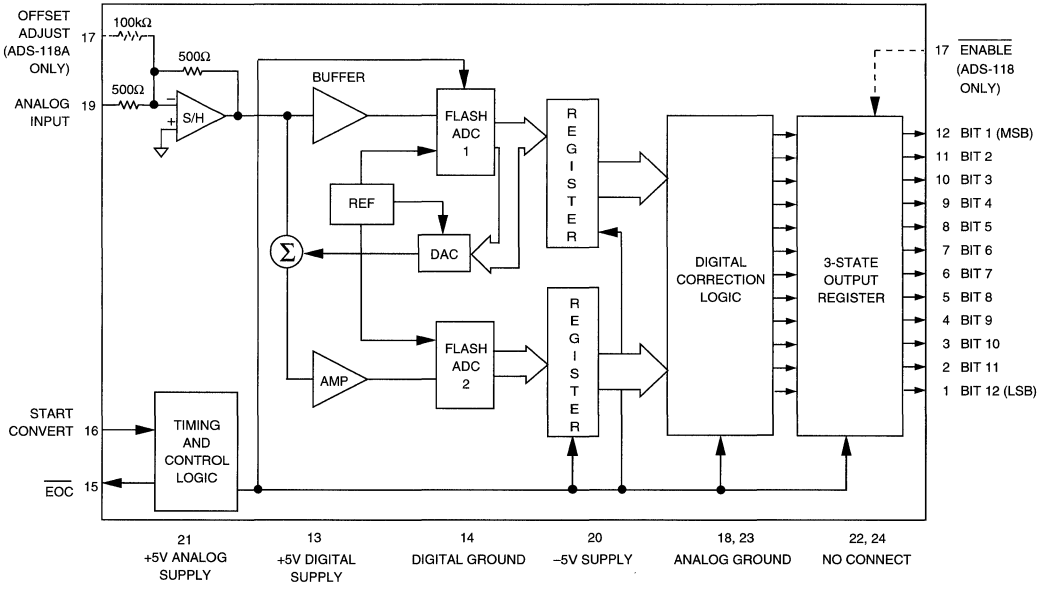


Figure 1. ADS-118/118A Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Supply (Pins 13, 21)	0 to +6	Volts
–5V Supply (Pin 20)	0 to –6	Volts
Digital Inputs (Pins 16, 17)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 19)	±5	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–118MC/AMC	0	—	+70	°C
ADS–118MM/AMM	–55	—	+125	°C
Thermal Impedance				
θjc	—	2	—	°C/Watt
θca	—	23	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{DD} = ±5V, 5MHz sampling rate, and a minimum 3 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Voltage Range, ADS-118 ②	—	±1	—	—	±1	—	—	±1	—	Volt
Input Resistance	475	500	—	475	500	—	475	500	—	Ω
Input Capacitance	—	6	15	—	6	15	—	6	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	50	100	—	50	100	—	50	100	—	ns
STATIC PERFORMANCE										
Resolution	—	12	—	—	12	—	—	12	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.75	—	—	±1.0	—	—	±1.5	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.5	±0.75	—	±0.5	±0.95	—	±0.75	±0.95	LSB
Full Scale Absolute Accuracy	—	±0.1	±0.5	—	±0.5	±0.75	—	±0.75	±1.5	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.1	±0.5	—	±0.5	±0.85	—	±0.85	±2.0	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.1	±0.5	—	±0.5	±1.5	—	±1.5	±2.5	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.5	—	±0.5	±1.0	—	±1.0	±2.5	%
No Missing Codes (f_{in} = 10kHz)	12	—	—	12	—	—	12	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 500kHz	—	–76	–71	—	–74	–70	—	–72	–66	dB
500kHz to 1MHz	—	–75	–71	—	–74	–70	—	–70	–65	dB
1MHz to 2.5MHz	—	–74	–69	—	–73	–67	—	–66	–60	dB
Total Harmonic Distortion (–0.5dB)										
dc to 500kHz	—	–72	–68	—	–71	–67	—	–70	–65	dB
500kHz to 1MHz	—	–71	–67	—	–70	–66	—	–67	–63	dB
1MHz to 2.5MHz	—	–70	–66	—	–69	–65	—	–66	–60	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)										
dc to 500kHz	67	69	—	66	69	—	64	67	—	dB
500kHz to 1MHz	66	69	—	65	68	—	63	66	—	dB
1MHz to 2.5MHz	66	69	—	65	68	—	63	66	—	dB
Signal–to–Noise Ratio ④ (& distortion, –0.5dB)										
dc to 500kHz	65	68	—	64	67	—	62	66	—	dB
500kHz to 1MHz	65	68	—	64	67	—	61	65	—	dB
1MHz to 2.5MHz	64	67	—	63	66	—	60	64	—	dB
Noise	—	195	—	—	195	—	—	195	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 1MHz, 975kHz, f_s = 5MHz, –0.5dB)	—	–74	—	—	–74	—	—	–74	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	20	—	—	20	—	—	20	—	MHz
Large Signal (–0.5dB input)	—	10	—	—	10	—	—	10	—	MHz
Feedthrough Rejection (f_{in} = 2.5MHz)	—	80	—	—	80	—	—	80	—	dB
Slew Rate	—	±400	—	—	±400	—	—	±400	—	V/µs
Aperture Delay Time	—	±10	—	—	±10	—	—	±10	—	ns
Aperture Uncertainty	—	3	—	—	3	—	—	3	—	ps rms
S/H Acquisition Time (to ±0.01%FSR, 2V step)	—	85	90	—	85	90	—	85	90	ns
Overvoltage Recovery Time ⑤	—	200	—	—	200	—	—	200	—	ns
A/D Conversion Rate	5	—	—	5	—	—	5	—	—	MHz

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DIGITAL OUTPUTS	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Delay, Falling Edge of EOC to Output Data Valid	—	—	20	—	—	20	—	—	20	ns
Delay, Falling Edge of ENABLE to Output Data Valid	—	—	10	—	—	10	—	—	10	ns
Output Coding	Offset Binary									
POWER REQUIREMENTS										
Power Supply Ranges ⑥										
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.9	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	–4.9	–5.0	–5.25	Volts
Power Supply Currents										
+5V Supply	—	+205	+220	—	+205	+220	—	+205	+220	mA
–5V Supply	—	–80	–90	—	–80	–90	—	–80	–90	mA
Power Dissipation	—	1.3	1.5	—	1.3	1.5	—	1.3	1.5	Watts
Power Supply Rejection	—	—	±0.1	—	—	±0.1	—	—	±0.1	%FSR/%V

Footnotes:

① All power supplies should be on before applying a start convert pulse. All supplies and the clock (start convert pulses) must be present during warmup periods. The device must be continuously converting during this time.

② Input Voltage Range for ADS-118A is ±1.25V.

③ A 100ns wide start convert pulse is used for all production testing. For applications requiring less than a 5MHz sampling rate, wider start convert pulses can be used. NOTE: The device only requires the rising edge of a start convert pulse to operate.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

⑥ The minimum supply voltages of +4.9V and –4.9V for $\pm V_{DD}$ are required for –55°C operation only. The minimum limits are +4.75V and –4.75V when operating at +125°C.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-118 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 18, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-118 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figures 3a and 3b. When using this circuitry, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). To disable, connect pin 17 to logic "1" (high). The three-state outputs are permanently enabled in the ADS-118A.

4. Applying a start convert pulse while a conversion is in progress ($\overline{\text{EOC}}$ = logic "1") will initiate a new and inaccurate conversion cycle.

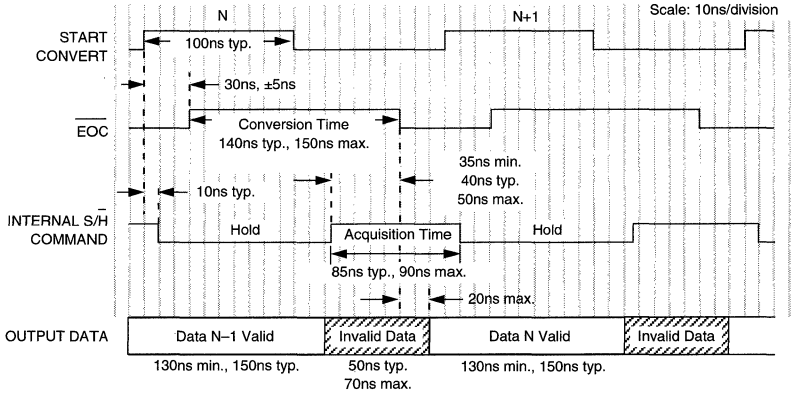


Figure 2. ADS-118/118A Timing Diagram

CALIBRATION PROCEDURE

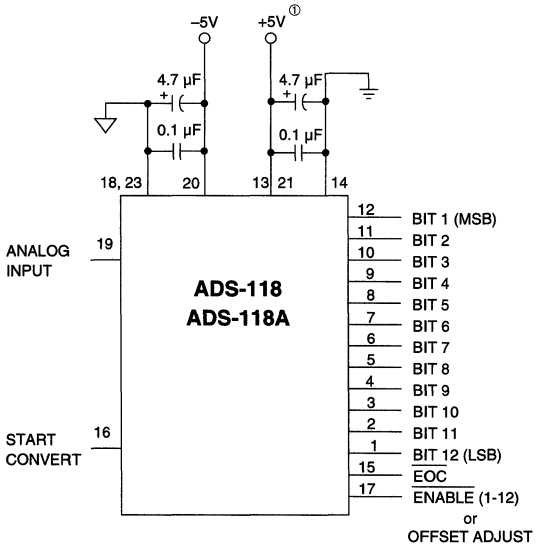
Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuits in Figures 3a and 3b are guaranteed to compensate for the ADS-118's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-118, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+244µV for ADS-118; +305µV for ADS-118A).

Table 1. Output Coding for Bipolar Operation

BIPOLAR SCALE	ADS-118 INPUT VOLTAGE (±1V RANGE)	OUTPUT CODING OFFSET BINARY MSB LSB	ADS-118A INPUT VOLTAGE (±1.25V RANGE)
+FS –1 LSB	+0.99951V	1111 1111 1111	+1.2494V
+3/4 FS	+0.75000V	1110 0000 0000	+0.9375V
+1/2 FS	+0.50000V	1100 0000 0000	+0.6250V
0	0.00000V	1000 0000 0000	0.0000V
–1/2 FS	–0.50000V	0100 0000 0000	–0.6250V
–3/4 FS	–0.75000V	0010 0000 0000	–0.9375V
–FS +1 LSB	–0.99951V	0000 0000 0001	–1.2494V
–FS	–1.00000V	0000 0000 0000	–1.2500V



① A single +5V supply should be used for both +5V analog and +5V digital. If separate supplies are used, the difference between the two cannot exceed 100mV.

Figure 3. Typical Connection Diagram

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+0.99927V for ADS-118; +1.249085V for ADS-118A).

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting.
2. Apply +244µV (ADS-118) or +305µV (ADS-118A) to the ANALOG INPUT (pin 19).
3. Adjust the offset potentiometer until the output bits are 1000 0000 00000 and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +0.99927V (ADS-118) or +1.249085V (ADS-118A) to the ANALOG INPUT (pin 19).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.
3. To confirm proper operation of the device, vary the input signal to obtain the output coding listed in Table 1.

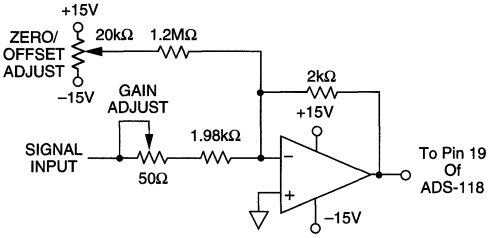
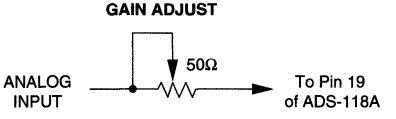


Figure 3a. Optional ADS-118 External Gain and Offset Adjust Circuits



NOTE: Potentiometer is at 25Ω during the device's factory trim procedure.

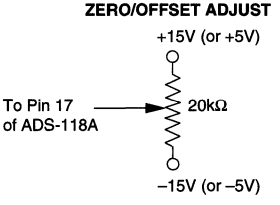


Figure 3b. Optional ADS-118A Gain and Offset Adjust Circuits

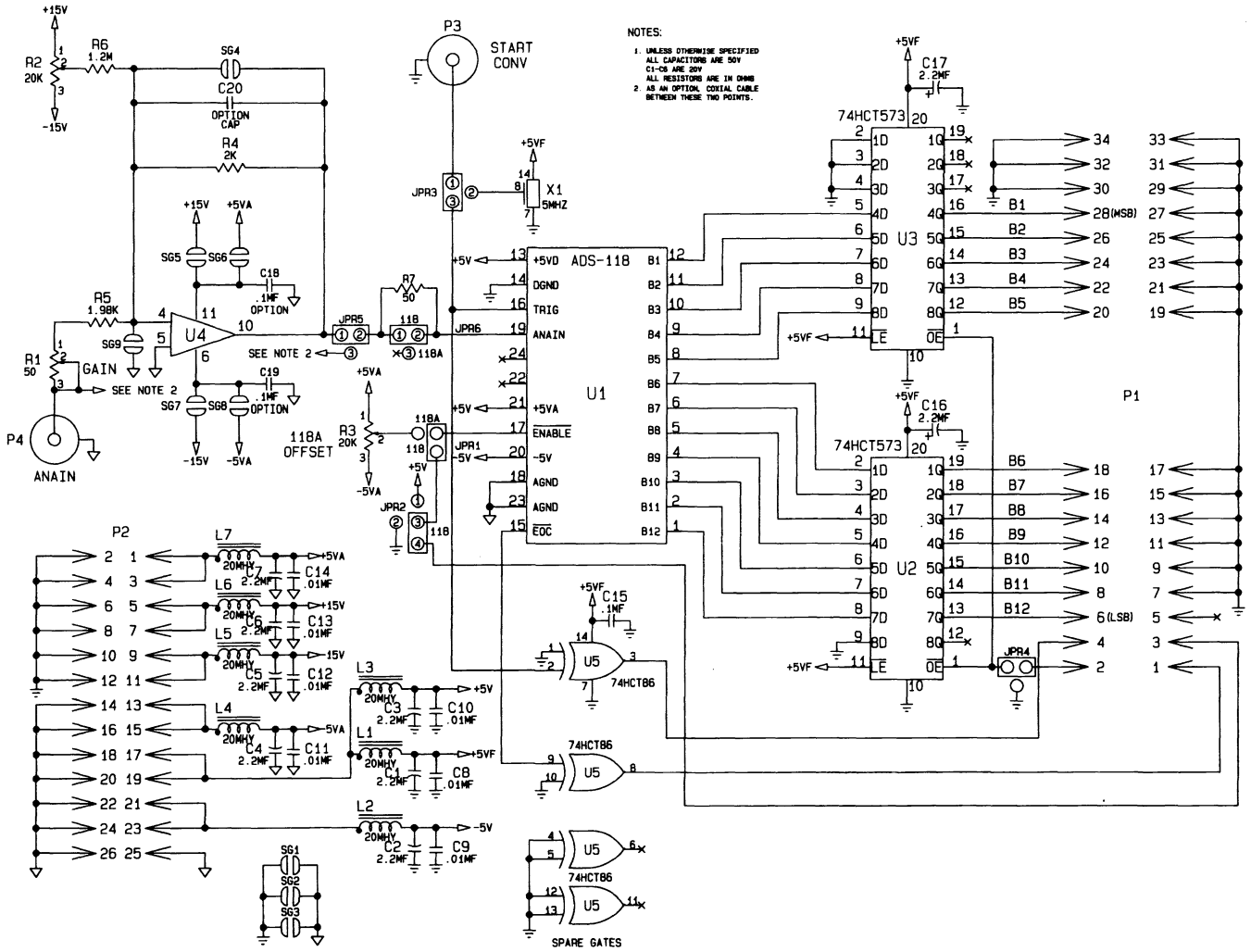


Figure 4. ADS-118/118A Evaluation Board Schematic (ADS-B118)

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

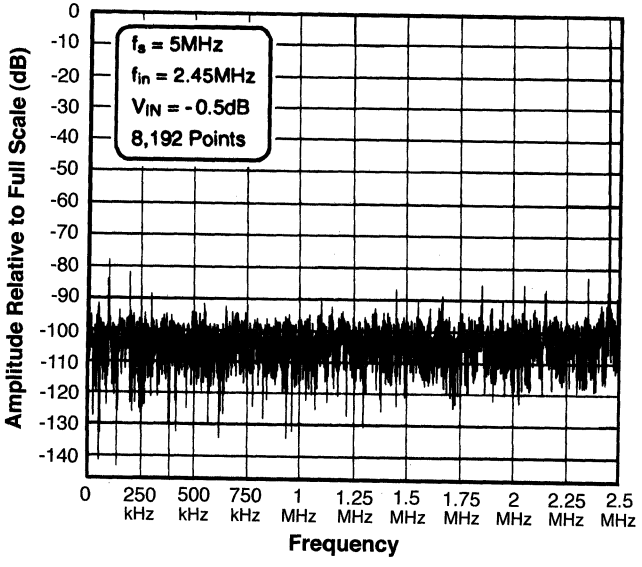


Figure 5. ADS-118 FFT Analysis

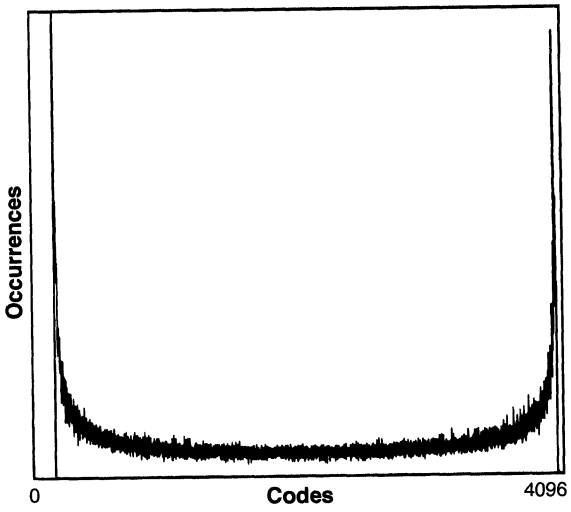


Figure 6. ADS-118 Histogram

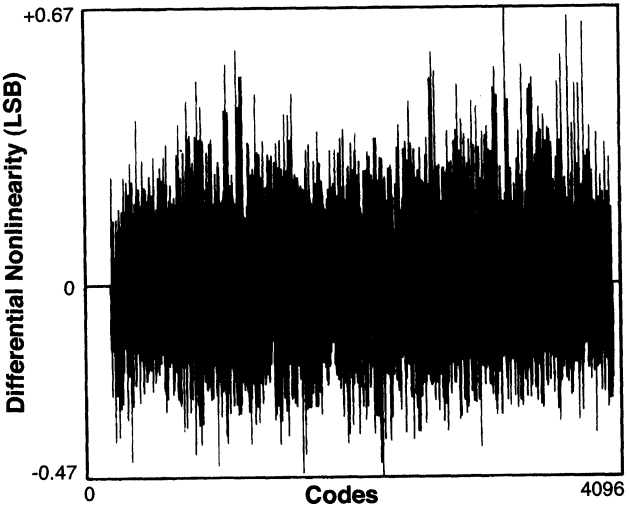
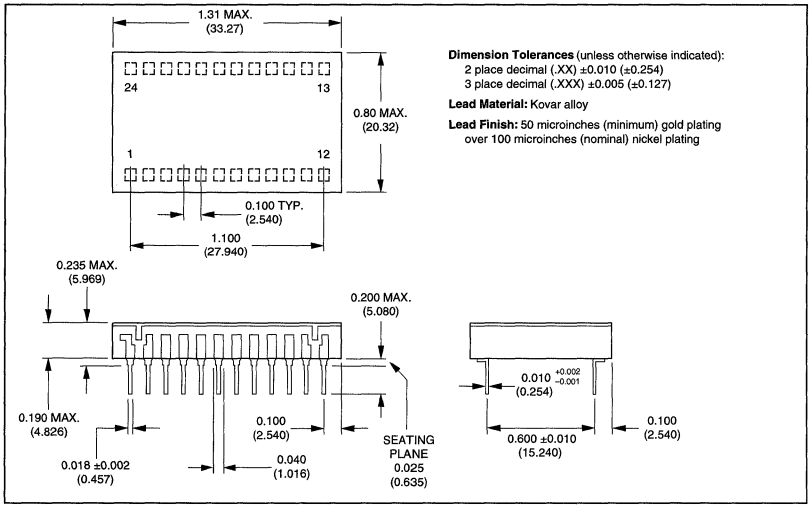


Figure 7. ADS-118 Differential Nonlinearity Derived from Histogram

MECHANICAL DIMENSIONS
INCHES (mm)

24-Pin DDIP Versions

ADS-118MC
ADS-118MM
ADS-118AMC
ADS-118AMM

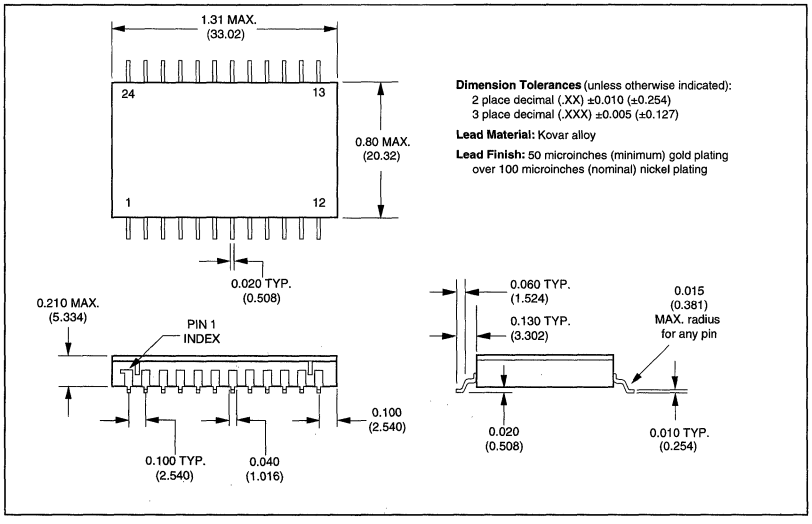


Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

24-Pin Surface Mount Version



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-118MC	0 to +70°C
ADS-118MM	–55 to +125°C
ADS-118AMC	0 to +70°C
ADS-118AMM	–55 to +125°C

For MIL-STD-883 product specification or availability of surface-mount packaging, contact DATEL.

ACCESSORIES

ADS-B118	Evaluation board (without ADS-118)
HS-24	Heat sink for all DDIP ADS-118 models.

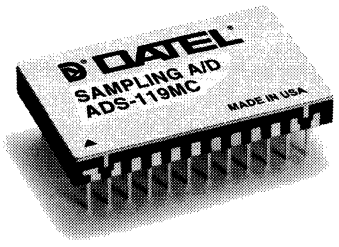
Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

DATEL®
INNOVATION and EXCELLENCE

ADS-119
12-Bit, 10MHz, Low-Power Sampling A/D Converters

FEATURES

- **12-Bit resolution**
- **10MHz minimum sampling rate**
- **Functionally complete**
- **Small 24-pin DDIP or SMT package**
- **Requires only ±5V supplies**
- **Low-power, 1.8 Watts**
- **Outstanding dynamic performance**
- **Edge-triggered**
- **No missing codes over temperature**
- **Ideal for both time and frequency-domain applications**



GENERAL DESCRIPTION

The ADS-119 is a high-performance, 12-bit, 10MHz sampling A/D converter. The device samples input signals up to Nyquist frequencies with no missing codes. The ADS-119 features excellent dynamic performance including a typical SNR of 69dB.

Packaged in a metal-sealed, ceramic, 24-pin DDIP, the functionally complete ADS-119 contains a fast-settling sample/hold amplifier, a subranging (two-pass) A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. All timing and control logic operates from the rising edge of a single start convert pulse. Digital input and output levels are TTL.

Requiring only ±5V supplies, the ADS-119 typically dissipates 1.8 Watts. The unit offers a bipolar input range of ±1.5V. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	24	NO CONNECT
2	BIT 11	23	ANALOG GROUND
3	BIT 10	22	NO CONNECT
4	BIT 9	21	+5V ANALOG SUPPLY
5	BIT 8	20	–5V SUPPLY
6	BIT 7	19	ANALOG INPUT
7	BIT 6	18	ANALOG GROUND
8	BIT 5	17	OFFSET ADJUST
9	BIT 4	16	START CONVERT
10	BIT 3	15	DATA VALID
11	BIT 2	14	DIGITAL GROUND
12	BIT 1 (MSB)	13	+5V DIGITAL SUPPLY

Typical applications include signal analysis, medical/graphic imaging, process control, ATE, radar, and sonar.

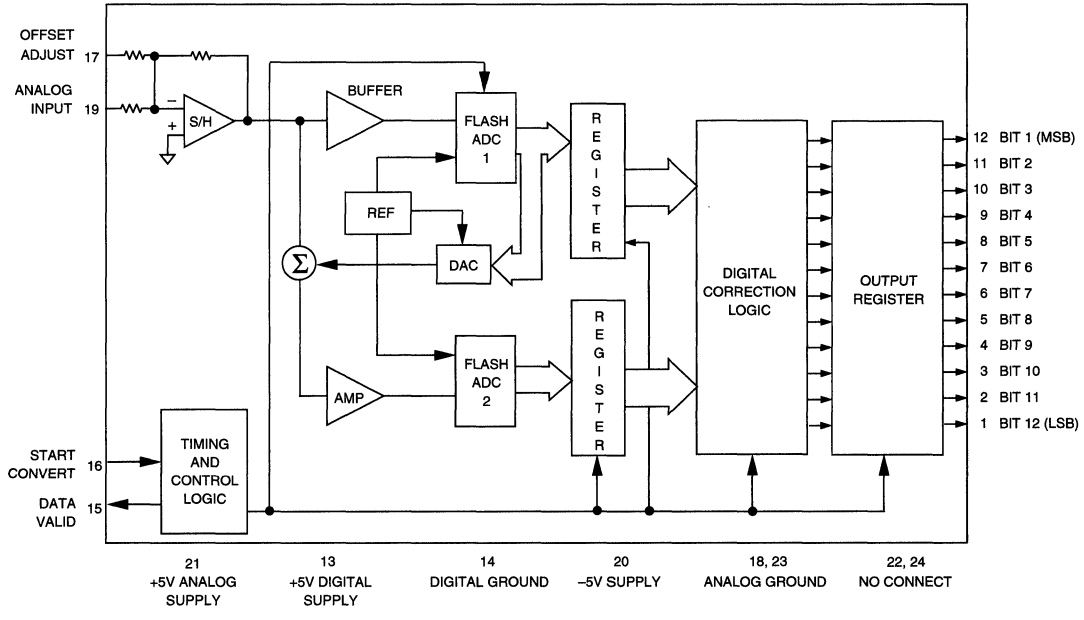


Figure 1. ADS-119 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Supply (Pins 13, 21)	0 to +6	Volts
–5V Supply (Pin 20)	0 to –6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 19)	±5	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–119MC/GC	0	—	+70	°C
ADS–119MM/GM/883	–55	—	+125	°C
Thermal Impedance				
θjc	—	3	—	°C/Watt
θca	—	23	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{DD} = ±5V, 10MHz sampling rate, and a minimum 3 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	±1.5	—	—	±1.5	—	—	±1.5	—	Volts
Input Resistance	300	350	—	300	350	—	300	350	—	Ω
Input Capacitance	—	6	15	—	6	15	—	6	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	50	—	—	50	—	—	50	—	ns
STATIC PERFORMANCE										
Resolution	—	12	—	—	12	—	—	12	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.75	—	—	±1.0	—	—	±1.5	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.5	±0.95	–0.95	±0.5	+1	–0.95	±0.75	+1.25	LSB
Full Scale Absolute Accuracy	—	±0.2	±0.5	—	±0.5	±0.75	—	±0.75	±1.5	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.2	±0.6	—	±0.3	±0.7	—	±0.6	±1.0	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.1	±0.6	—	±0.3	±0.7	—	±0.7	±1.5	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.5	—	±0.5	±1.0	—	±1.0	±2.5	%
No Missing Codes (f_{in} = 10kHz)	12	—	—	12	—	—	12	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 1MHz	—	–70	–63	—	–70	–63	—	–69	–61	dB
1MHz to 2.5MHz	—	–70	–63	—	–70	–63	—	–69	–60	dB
2.5MHz to 5MHz	—	–70	–63	—	–70	–63	—	–67	–60	dB
Total Harmonic Distortion (–0.5dB)										
dc to 1MHz	—	–69	–63	—	–69	–63	—	–68	–60	dB
1MHz to 2.5MHz	—	–68	–63	—	–68	–63	—	–67	–60	dB
2.5MHz to 5MHz	—	–68	–63	—	–67	–63	—	–66	–60	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)										
dc to 1MHz	66	69	—	66	69	—	63	67	—	dB
1MHz to 2.5MHz	66	69	—	66	69	—	63	66	—	dB
2.5MHz to 5MHz	66	69	—	66	69	—	63	66	—	dB
Signal–to–Noise Ratio ④ (& distortion, –0.5dB)										
dc to 1MHz	62	66	—	62	66	—	60	65	—	dB
1MHz to 2.5MHz	62	66	—	62	66	—	60	65	—	dB
2.5MHz to 5MHz	62	66	—	62	66	—	60	64	—	dB
Noise	—	250	—	—	300	—	—	400	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 2.45MHz, 2.2MHz, f_s=10MHz, –0.5dB)	—	–72	—	—	–72	—	—	–72	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	60	—	—	60	—	—	60	—	MHz
Large Signal (–0dB input)	—	10	—	—	10	—	—	10	—	MHz
Feedthrough Rejection (f_{in} = 5MHz)	—	76	—	—	76	—	—	76	—	dB
Slew Rate	—	±400	—	—	±400	—	—	±400	—	V/µs
Aperture Delay Time	—	5	—	—	5	—	—	5	—	ns
Aperture Uncertainty	—	3	—	—	3	—	—	3	—	ps rms
S/H Acquisition Time (to ±0.01%FSR, 3V step)	30	35	37	30	35	37	30	35	37	ns
Overvoltage Recovery Time ⑤	—	100	—	—	100	—	—	100	—	ns
A/D Conversion Rate	10	—	—	10	—	—	10	—	—	MHz

DIGITAL OUTPUTS	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Output Coding	Offset Binary									
POWER REQUIREMENTS										
Power Supply Ranges ⑥										
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.9	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	–4.9	–5.0	–5.25	Volts
Power Supply Currents										
+5V Supply	—	+200	+215	—	+200	+215	—	+200	+215	mA
–5V Supply	—	–180	–205	—	–180	–205	—	–180	–205	mA
Power Dissipation	—	1.8	2.1	—	1.8	2.1	—	1.8	2.1	Watts
Power Supply Rejection	—	—	±0.1	—	—	±0.1	—	—	±0.1	%FSR/%V

Footnotes:

① All power supplies should be on before applying a start convert pulse. All supplies and the clock (start convert pulses) must be present during warmup periods. The device must be continuously converting during this time.

② Contact DATEL for other input voltage ranges.

③ A 50ns wide start convert pulse is used for all production testing. For applications requiring less than a 10MHz sampling rate, wider start convert pulses can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + 20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range. For best overvoltage recovery time, it is recommended that the analog input be clamped to a maximum of ±1.9V.

⑥ The minimum supply voltages of +4.9V and –4.9V for $\pm V_{DD}$ are required for –55°C operation only. The minimum limits are +4.75V and –4.75V when operating at +125°C.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-119 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 18, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-119 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figures 3 and 4. For operation without adjustment, tie pin 17 to analog ground. When using this circuitry, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. Applying a start convert pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") will initiate a new and inaccurate conversion cycle.

4. Data is valid only for the time period (55ns, typical) shown in Figure 2 even if the device is sampling at less than 10MHz.

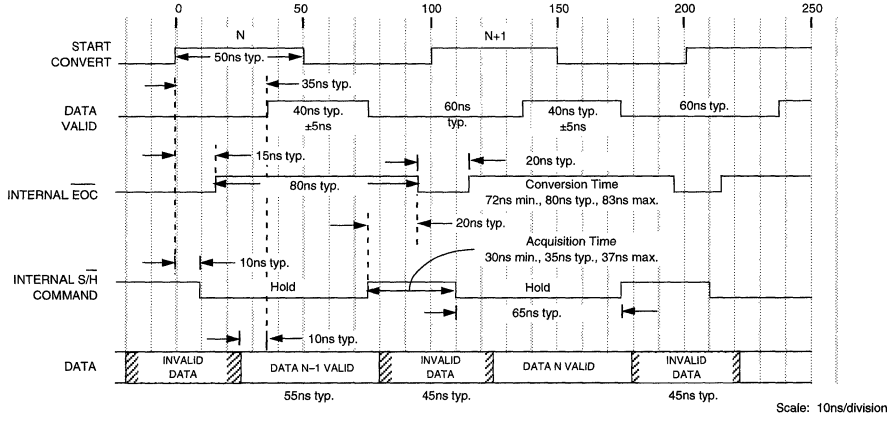


Figure 2. ADS-119 Timing Diagram

CALIBRATION PROCEDURE

(Refer to Figures 3 and 4, Table 1)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuits in Figure 3 and 4 are guaranteed to compensate for the ADS-119's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

Offset adjusting for the ADS-119 is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+366µV).

Table 1. Output Coding for Bipolar Operation

BIPOLAR SCALE	ADS-119 INPUT VOLTAGE (±1.5V RANGE)	OUTPUT CODING OFFSET BINARY MSB LSB
+FS –1 LSB	+1.49927V	1111 1111 1111
+3/4 FS	+1.12500V	1110 0000 0000
+1/2 FS	+0.75000V	1100 0000 0000
0	0.00000V	1000 0000 0000
–1/2 FS	–0.75000V	0100 0000 0000
–3/4 FS	–1.12500V	0010 0000 0000
–FS +1 LSB	–1.49927V	0000 0000 0001
–FS	–1.50000V	0000 0000 0000

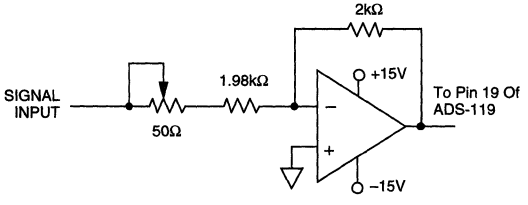


Figure 3.
Optional Calibration Circuit, ADS-119

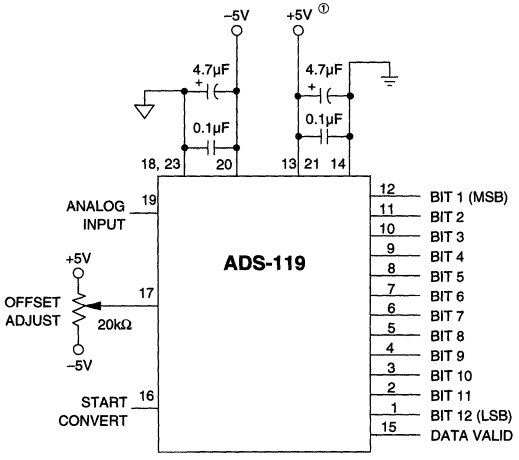
Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+1.4989V).

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting.
2. Apply +366µV to the ANALOG INPUT (pin 19).
3. Adjust the offset potentiometer until the output bits are 1000 0000 0000 and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +1.4989V to the ANALOG INPUT (pin 19).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.
3. To confirm proper operation of the device, vary the input signal to obtain the output coding listed in Table 1.



① A single +5V supply should be used for both the +5V analog and +5V digital. If separate supplies are used, the difference between the two cannot exceed 100mV.

Figure 4. Typical Connection Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to +125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

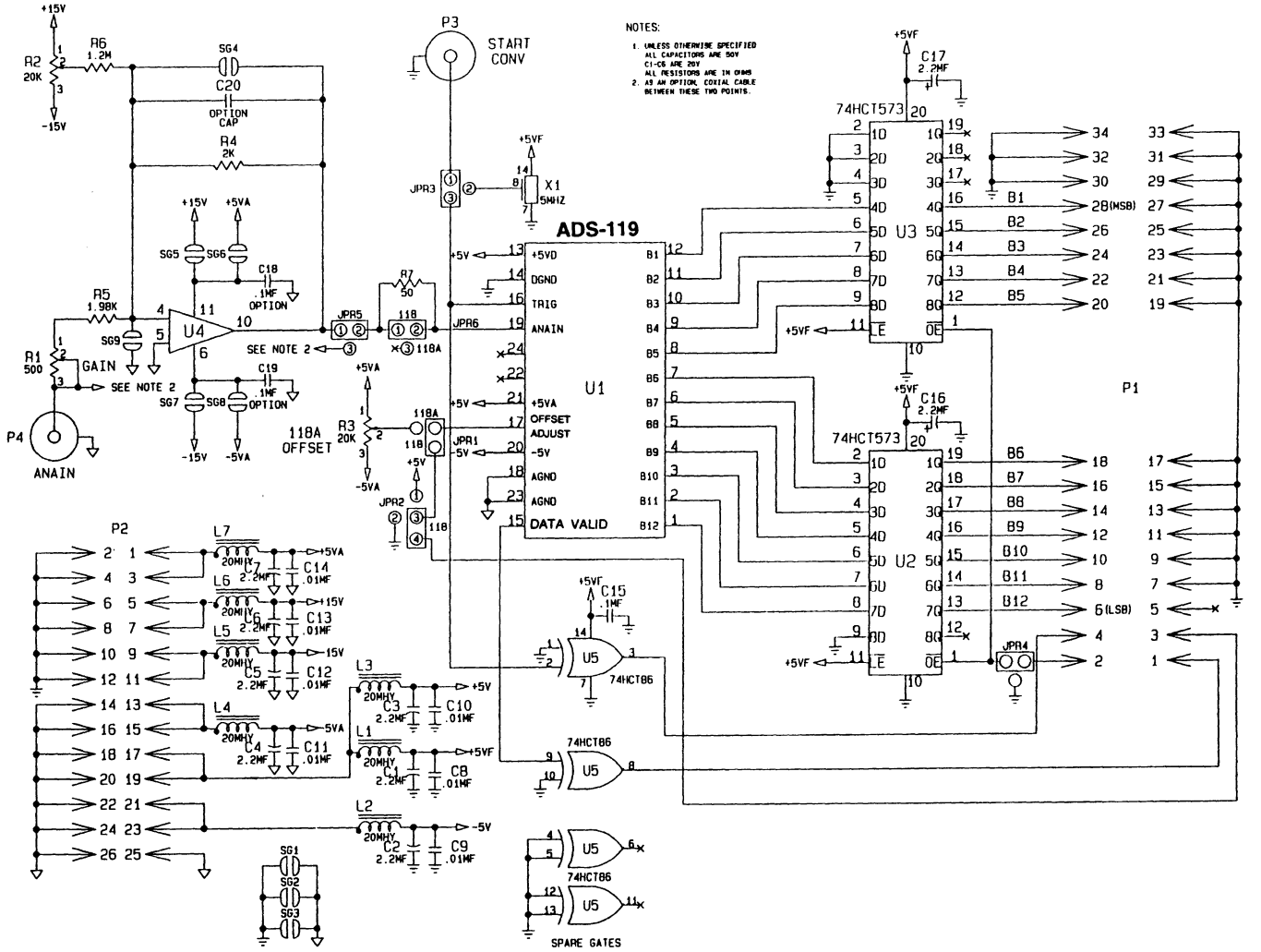


Figure 5. ADS-119 Evaluation Board Schematic (ADS-B119)

PERFORMANCE DATA

This histogram represents the typical peak-to-peak noise (including quantization noise) associated with the ADS-119. 4,096 conversions were processed with the input to the ADS-119 tied to analog ground.

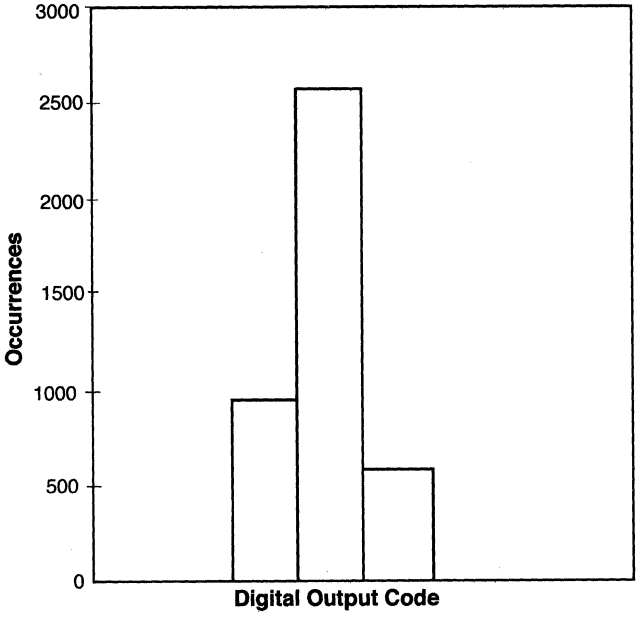


Figure 6. ADS-119 Grounded Input Histogram

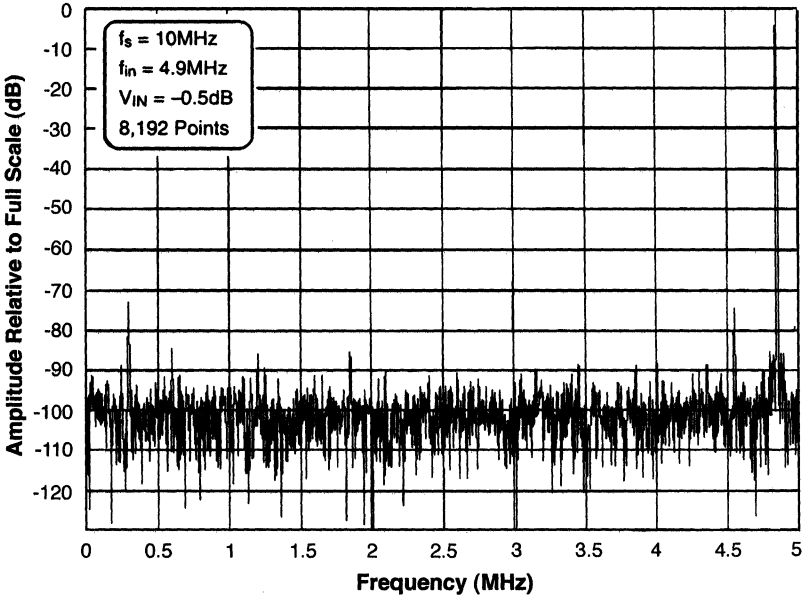


Figure 7. ADS-119 FFT Analysis

PERFORMANCE DATA (Continued)

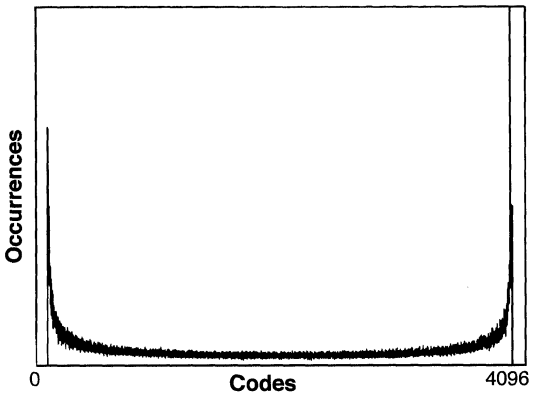


Figure 8. ADS-119 Histogram

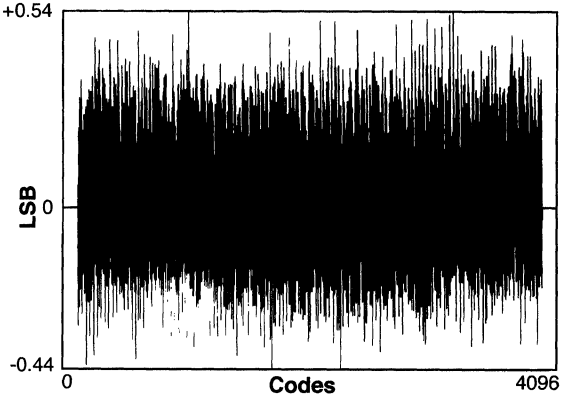


Figure 9. ADS-119 Differential Nonlinearity

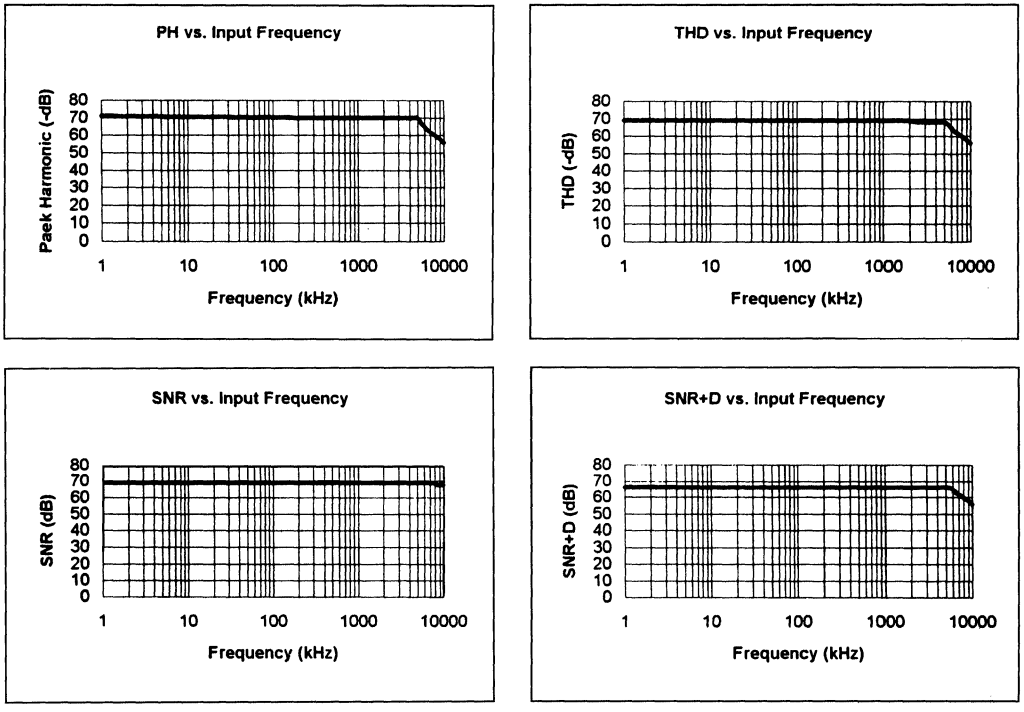
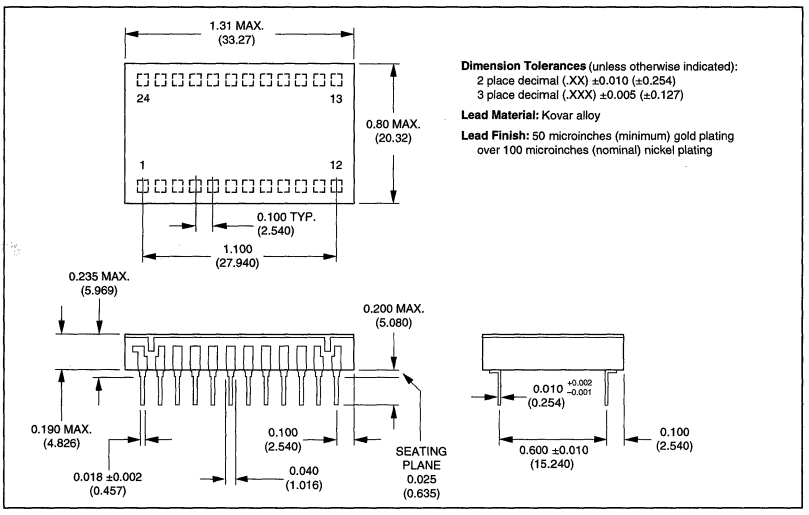


Figure 10. ADS-119 Performance Curves

MECHANICAL DIMENSIONS
INCHES (mm)

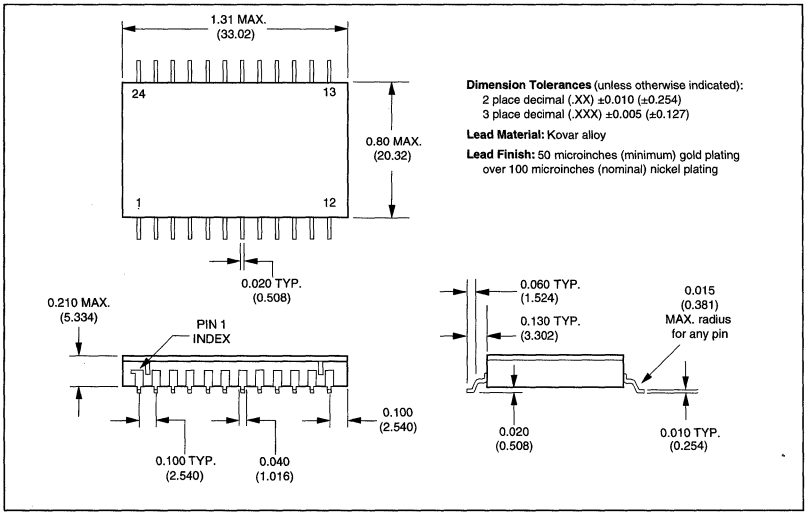
24-Pin DDIP Versions

ADS-119MC
ADS-119MM
ADS-119/883



24-Pin Surface Mount Versions

ADS-119GC
ADS-119GM



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-119MC	0 to +70°C
ADS-119MM	–55 to +125°C
ADS-119/883	–55 to +125°C
ADS-119GC	0 to +70°C
ADS-119GM	–55 to +125°C

ACCESSORIES

ADS-B119	Evaluation Board (without ADS-119)
HS-24	Heat Sink for all ADS-119 DDIP models

Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.
For MIL-STD-883 product specifications contact DATEL.

DATEL®
INNOVATION and EXCELLENCE

ADS-325A
10-Bit, 20MHz Sampling A/D Converter

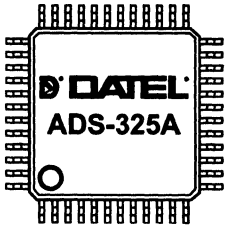
FEATURES

- ±1/2LSB differential nonlinearity error
- Low, 145mW power dissipation
- Internal sample-and-hold circuit
- 50µA input current
- 9pF input capacitance
- 70MHz input bandwidth
- TTL-compatible digital I/O
- Latched three-state output buffer
- Single +5V supply
- Internal calibration circuitry

GENERAL DESCRIPTION

The ADS-325A is a 10-bit, 20MHz, low-power, TTL-compatible sampling A/D converter designed for video applications. Its small, 48-pin, plastic VQFP package contains a sample-and-hold amplifier, a three-state output register, calibration circuitry, and all necessary control logic. Only an external reference voltage is required.

Dynamic performance includes a spurious free dynamic range of 65dB and a signal-to-noise ratio (with distortion) of 54dB with a 3MHz input. The ADS-325A is capable of operating from a single +5V power supply and typically consumes 145mW. The unit operates over the –25 to +75°C temperature range.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 10 (LSB)	48	DIGITAL GROUND (DGND)
2	BIT 9	47	NO CONNECTION
3	BIT 8	46	NO CONNECTION
4	BIT 7	45	+DV_S (Digital)
5	BIT 6	44	ANALOG GROUND (AGND)
6	DIGITAL GROUND (DGND)	43	ANALOG GROUND (AGND)
7	+DV_S (Digital)	42	TEST SIGNAL IN
8	BIT 5	41	CAL. PULSE IN (CAL)
9	BIT 4	40	NO CONNECTION
10	BIT 3	39	ANALOG SIGNAL IN (V_{IN})
11	BIT 2	38	TEST SIGNAL OUT
12	BIT 1 (MSB)	37	TEST SIGNAL IN
13	TEST PIN	36	ANALOG GROUND (AGND)
14	TEST SIGNAL IN	35	REFERENCE BOTTOM (V_B)
15	RESET	34	REFERENCE BOTTOM (V_B)
16	DIGITAL GROUND (DGND)	33	NO CONNECTION
17	SELECT	32	NO CONNECTION
18	+AV_S (Analog)	31	NO CONNECTION
19	TEST MODE	30	REFERENCE TOP (V_T)
20	LINV	29	REFERENCE TOP (V_T)
21	MINV	28	ANALOG GROUND (AGND)
22	CLOCK INPUT	27	ANALOG GROUND (AGND)
23	OUTPUT ENABLE ($\overline{OE}$)	26	+AV_S (Analog)
24	CHIP ENABLE ($\overline{CE}$)	25	+AV_S (Analog)

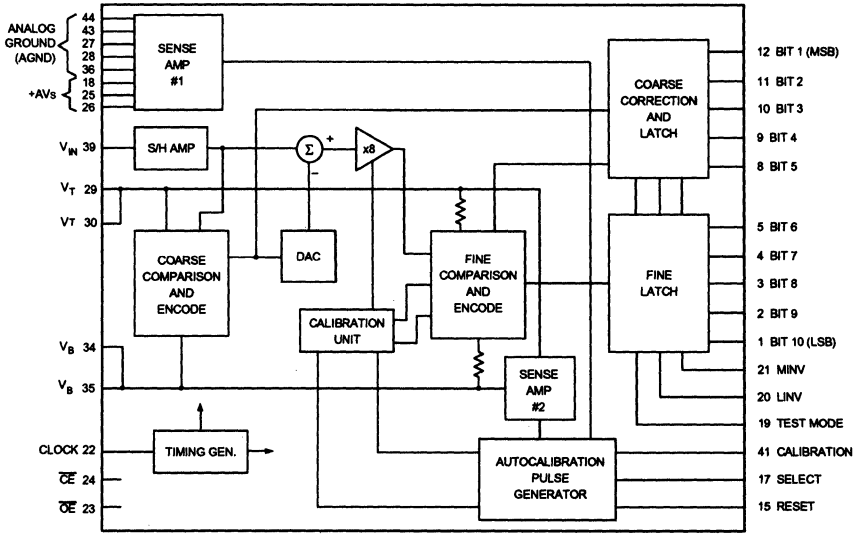


Figure 1. ADS-325A Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS (Ta = +25°C)

PARAMETERS	LIMITS	UNITS
Supply Voltages (+AV_S and +DV_S)	0 to +7	Volts
Reference Voltage (V_T and V_B)	−0.5 to +V_S +0.5	Volts
Input Voltage, Analog (V_{IN})	−0.5 to +V_S +0.5	Volts
Input Voltage, Digital (V_{IH} and V_{IL})	−0.5 to +V_S +0.5	Volts
Output Voltage, Digital (V_{OH} and V_{OL})	−0.5 to +V_S +0.5	Volts

FUNCTIONAL SPECIFICATIONS

(Typical at f_S = 20MHz, +AV_S = +5V, +DV_S = +3.3V, V_B = +2.0V, V_T = +4.0V, and T_A = +25°C unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range, V_{IN}	+1.8	+2	+3	Volts
Offset Voltage				
E_{OT}	+40	+90	+140	mV
E_{OB}	−120	−70	−20	mV
Input Current				
V_{IN} = +4V	—	—	±50	µA
V_{IN} = +2V	—	—	±50	µA
Capacitance, C_{IN}	—	9	—	pF
Bandwidth (−1dB)	—	70	—	MHz
DIGITAL INPUTS				
Input Voltage				
V_{IH}	+2.3	—	—	Volts
V_{IL}	—	—	+0.8	Volts
Current				
I_{IH} ① ②	—	—	+5	µA
I_{IL} ① ③	—	—	−5	µA
Clock Pulse Width				
T_{PW1}	25	—	—	ns
T_{PW0}	25	—	—	ns
Three-State Disable Time				
T_{AH}	20	25	30	ns
T_{HA}	10	15	20	ns
REFERENCE				
Input Voltage				
V_B	+1.8	—	—	Volts
V_T	—	—	+AV_S − 0.4	Volts
Current ④				
I_T	+5	+7	+11	mA
I_B	−11	−7	−5	mA
Resistance (V_T − V_B)	180	280	380	Ω
PERFORMANCE				
Throughput Rate ⑤ (FS)	20	—	—	MHz
Minimum Throughput Rate ⑤	0.5	—	—	MHz
Integral Linearity Error	—	±1.3	±2	LSB
Differential Linearity Error	—	±0.5	±1	LSB
Differential Gain Error ⑥	—	1.0	—	%
Differential Phase Error ⑥	—	0.3	—	Degrees
Output Delay, Td (C_L = 20pF)	8	13	18	ns
Aperture Delay, Ts	2	4	6	ns
Aperture Uncertainty	—	30	—	ps
SNR & Distortion (−0dB)				
f_{IN} = 100kHz	—	53	—	dB
f_{IN} = 500kHz	—	52	—	dB
f_{IN} = 1MHz	—	53	—	dB
f_{IN} = 3MHz	—	54	—	dB
f_{IN} = 7MHz	—	47	—	dB
f_{IN} = 10MHz	—	45	—	dB
SFDR (−0dB)				
f_{IN} = 100kHz	—	60	—	dB
f_{IN} = 500kHz	—	59	—	dB
f_{IN} = 1MHz	—	60	—	dB
f_{IN} = 3MHz	—	65	—	dB
f_{IN} = 7MHz	—	50	—	dB
f_{IN} = 10MHz	—	49	—	dB

DIGITAL OUTPUTS	MIN.	TYP.	MAX.	UNITS
Current ($\overline{OE}$ = AGND; +DVs = Min.)				
I_{OH} ⑦	−3.5	—	—	mA
I_{OL} ⑧	+3.5	—	—	mA
Current ($\overline{OE}$ = +AVs; +DVs = Max.)				
I_{OZH} ⑨	—	—	±1	µA
I_{OZL} ⑩	—	—	±1	µA
POWER REQUIREMENTS				
Power Supply Voltage				
+AVs	+4.75	+5.0	+5.25	Volts
+DVs	+3.05	+3.3	+5.25	Volts
|DGND − AGND|	—	—	100	mV
Power Dissipation	—	145	—	mW
Supply Current				
Analog, IAs	+20	+27	+34	mA
Digital, IDs	—	+3	+5	mA
Standby Current ($\overline{CE}$ = High)				
Analog, I_{AST}	—	—	+1	mA
Digital, I_{DST}	—	—	+1	µA
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range	−20	—	+75	°C
Storage Temperature Range	−55	—	+150	°C
Weight	0.2 grams			
Package	48-pin plastic VQFP			

Footnotes:

① +DV_S = Maximum
② V_{IH} = +DVs
③ V_{IL} = 0V
④ RESET = Low
⑤ f_{IN} = 1kHz
⑥ NTSC 40 IRE mod ramp, f_C = 14.3MHz
⑦ V_{OH} = +DV_S − 0.5V
⑧ V_{OL} = +0.4V
⑨ V_{OH} = +DVs
⑩ V_{OL} = 0V

Table 1. Digital Output Coding

(TEST MODE = 1; LINV, MINV = 0)

Input Signal Voltage	Step	Digital Output Code MSB LSB
V_T	0	1 1 1 1 1 1 1 1 1 1
	↓	↓
↓	511	1 0 0 0 0 0 0 0 0 0
	512	0 1 1 1 1 1 1 1 1 1
	↓	↓
V_B	1023	0 0 0 0 0 0 0 0 0 0

TECHNICAL NOTES

1. It is possible to use +5V rather than +3.3V for +DVs. There will be no difference in electrical switching characteristics.
2. A time differential between supplying both +AVs and +DVs may cause a latch-up problem. DATEL recommends using a common power supply for both +AVs and +DVs to avoid latch-up conditions.
3. Bypass +AVs and +DVs to ground using 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors as shown in the typical connection drawing, Figure 2.
4. DATEL recommends installing additional 0.1µF ceramic capacitors to reduce noise. Refer to the typical connection drawing, Figure 2, for component locations.

DATEL, Inc., 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For immediate assistance 800-233-2765

5. It is recommended that the reference signal sources be capable of driving more than 10mA.

6. It is recommended that the unit be hard-wired for evaluation. Sockets may degrade actual performance.

7. The test signal input/output pins are used in the production process. During normal operation, the test signal input pins (pins 14 and 37) are normally tied to AGND. The test signal input pin (pin 42) is normally tied to +AVs. The test signal output pins (13 and 38) are normally left open.

8. For $\overline{OE}$ (pin 23), output will be enabled with digital low and disabled (high impedance state) with a digital high.

9. For $\overline{CE}$ (pin 24), the normal operating mode is with a digital low input. Standby mode results from a digital high input.

10. For TEST MODE (pin 19), the digital outputs are fixed with a digital low applied. Normal output is achieved with a digital high applied.

11. LINV (pin 20) inverts bits two through bit 10 when a digital high is applied. MINV (pin 21) inverts bit 1 when a digital high is applied.

12. RESET (pin 15) is normally connected to digital high. A negative pulse, at least 1 clock cycle long, will re-initiate start-up calibration.

13. CAL (pin 41) is connected to digital high for internal calibration. Pulses are applied directly to pin 41 for external calibration. See Table 2 and Calibration Procedure.

14. SELECT (pin 17) is connected to digital high for internal calibration and to digital low for external start-up only calibration. See Table 2 and Calibration Procedure.

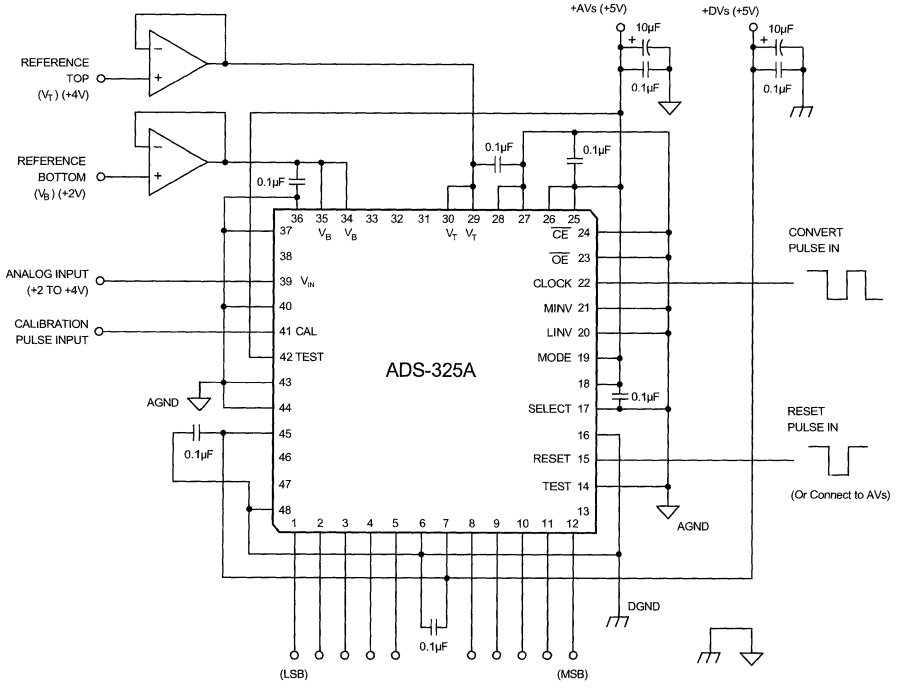


Figure 2. Typical ADS-325A Connection Diagram

Table 2. Calibration Mode Pin Connections

CALIBRATION MODE	Pin 41, CAL	Pin 17, SELECT
External Calibration	Apply external calibration pulses	Connect to AGND
Internal Calibration	Connect to +AVs	Connect to +AVs
Start-Up Calibration Only	Connect to +AVS	Connect to AGND

CALIBRATION PROCEDURE

The ADS-325A achieves its superior linearity using a start-up calibration function and a built-in auto-calibration pulse generation circuit. Figure 3a is a simplified block diagram of this internal calibration pulse generation circuit. The internal calibration circuit can be disabled and external calibration pulses applied, or not, as desired. Whether internal, external, or no calibration is used, the ADS-325A automatically self-calibrates upon start-up.

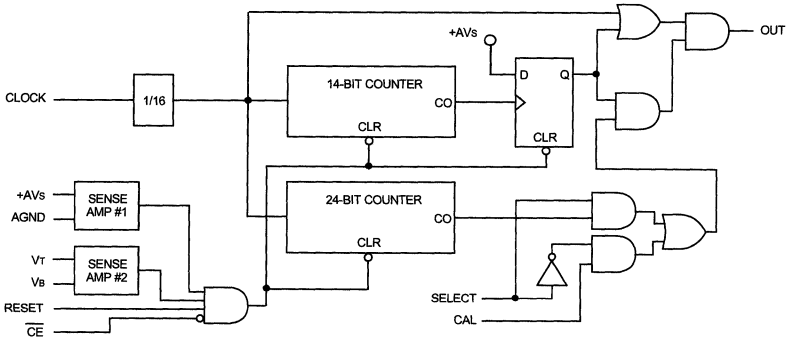


Figure 3a. Internal Calibration Pulse Generation Circuit

Start-up Calibration Function

The start-up calibration process requires over 600 calibration pulses. The internal start-up calibration function automatically supplies these pulses when power is first applied to the ADS-325A. The following five conditions, shown in Figure 3b, must be met to initiate the start-up calibration function:

1. The voltage difference between +AVs and AGND must be at least 2.5 Volts.
2. The voltage difference between V_T and V_B must be at least 1 Volt.
3. Condition 1 must be met before condition 2.
4. The RESET pin (pin 15) must be set high.
5. The $\overline{CE}$ pin (pin 24) must be set low.

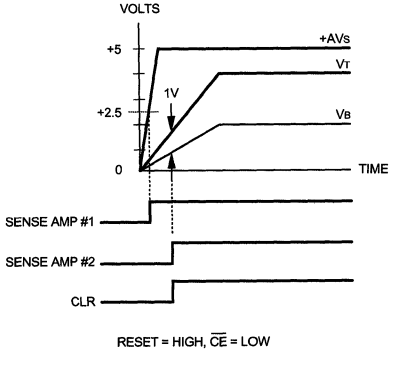


Figure 3b. Conditions for Start-Up Calibration

Once all of the above conditions have been met, the calibration pulses are generated by counting 16 clock cycles on a 14-bit counter and closing the gate when the carry-out occurs. The time required for start-up calibration is determined by the following formula where, for example, a CLOCK frequency of 14.3MHz requires a calibration period of 18.3ms:

Start-up
Calibration Time = CLOCK period x 16 x 16,384
= (1/CLOCK frequency) x 16 x 16,384
= (1/14.3MHz) x 16 x 16,384
= 18.3ms

Start-up Calibration Function Only

Auto or external calibration functions need not be employed after start-up calibration. To use only the start-up calibration function, connect the SELECT pin (pin 17) to AGND and connect the CAL pin (pin 41) to +AVs. This configuration requires that the analog supply voltage and reference voltage fluctuations be constrained to the following limits:

$$+AVs < \pm 100mV \text{ and } |V_T - V_B| < 200mV$$

Auto Calibration Function

After the initial start-up calibration is completed, the internal calibration function periodically and automatically generates calibration pulses so that calibration can be performed. This function counts 16 CLOCK cycles on a 24-bit counter and uses the carry-out as the calibration pulse. The period of the calibration pulse generated is as follows:

Internal Calibration Pulse Generation Cycle
= CLOCK period x 16 x 16,777,216

Therefore, if the CLOCK frequency is 14.3MHz, the calibration pulse generation cycle is 18.8 seconds; since calibration is performed once every seven pulses, the total calibration cycle is approximately 132 seconds. To use this function connect the SELECT pin (pin 17) and the CAL pin (pin 41) to +AVs.

Calibration starts when the falling edge of the CAL pulse (which may be internally generated or supplied externally) is detected.

This occupies the lower comparator for four clock cycles, beginning at least 7 CLOCK cycles after the falling edge of the CAL pulse was detected, as shown in Figure 3c. Note that the time between the falling edge of the CAL pulse and the next rising edge of the CLOCK pulse must be at least 10ns. The lower comparator data remains constant through 4 CLOCK cycles (conversions). Due to the asynchronous nature of the internal calibration function, the lower 5 LSBs of data remaining constant through four conversions may create problems in certain applications.

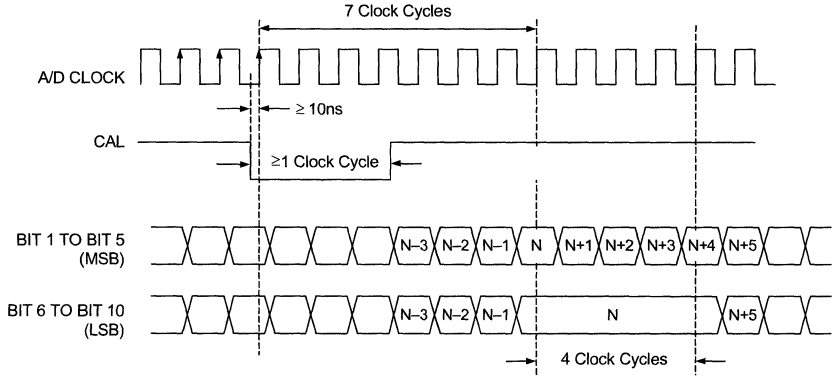


Figure 3c. Calibration Timing Diagram

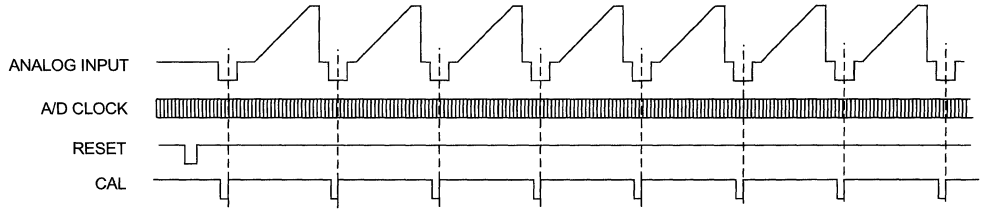


Figure 3d. Applying CAL Pulse Every H Sync.

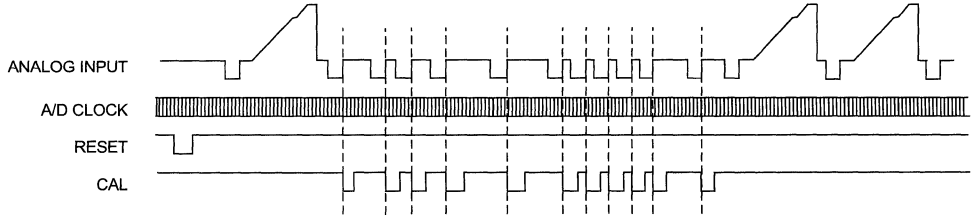


Figure 3e. Applying CAL Pulse Every V Sync.

External Calibration Function

Calibration can be performed synchronously with the input signal by supplying an external calibration pulse. Input the external calibration pulse to the CAL pin (pin 41) with the SELECT pin (pin 17) connected to AGND. As described above for internal calibration, calibration starts when the falling edge of the CAL pulse is detected. For video applications, calibration can be performed outside of the video intervals by using the sync signal to input the CAL pulse. Figures 3d and 3e show examples of inputting the CAL pulse for every H-sync and V-sync, respectively.

Re-initiation Of The Start-up Calibration Function

The start-up calibration function can be re-initiated after the power and reference voltages are supplied by applying a positive pulse to $\overline{CE}$ pin (pin 24) or a negative pulse to the RESET pin (pin 15). The pulses must be wider than or equal to one CLOCK cycle.

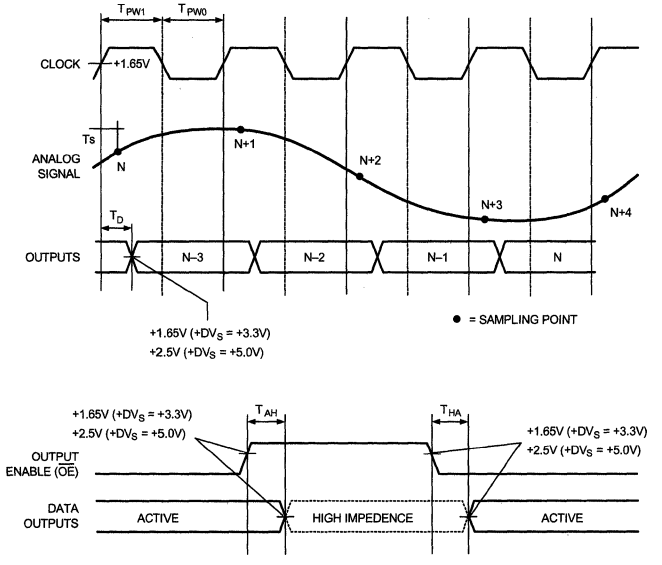
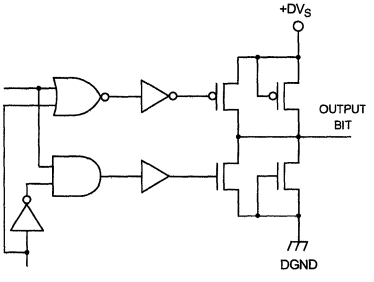
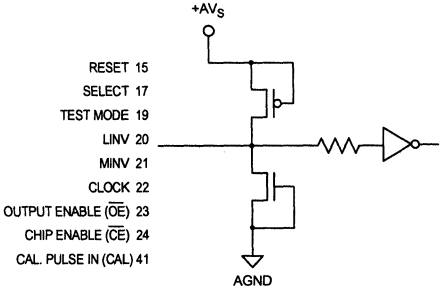


Figure 4. Typical ADS-325A Timing Diagrams

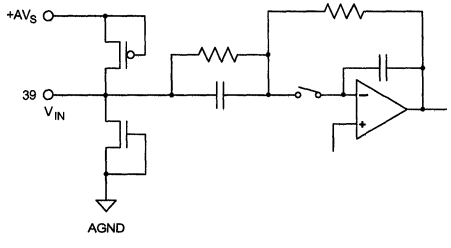
EQUIVALENT CIRCUITS



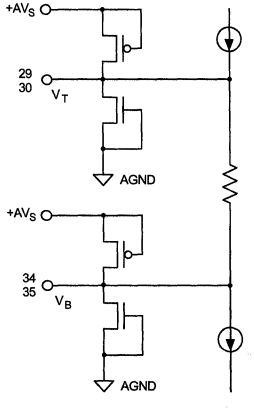
Digital Data Outputs



SEL, CLK, CAL, RESET, OE, CE, Test Mode, LINV and MINV inputs



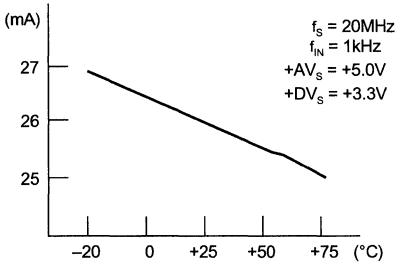
Analog Signal Input



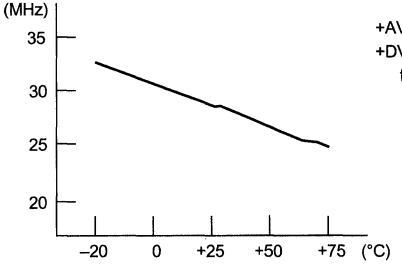
Reference Input

TYPICAL PERFORMANCE CURVES

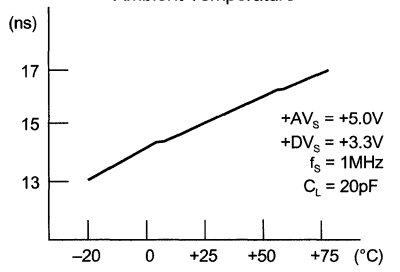
Supply Current vs. Ambient Temperature



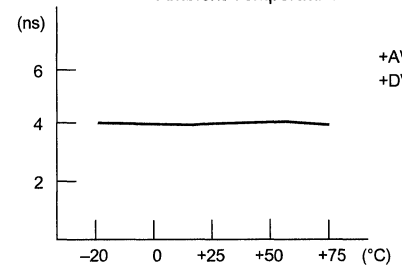
Max. Sampling Rate vs. Ambient Temperature



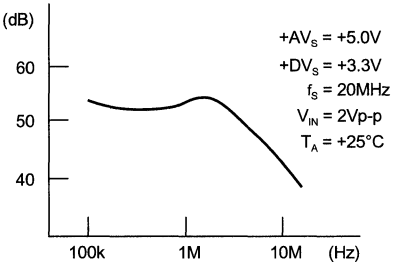
Output Data Delay vs. Ambient Temperature



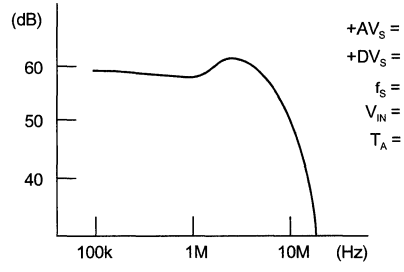
Sampling Delay vs. Ambient Temperature



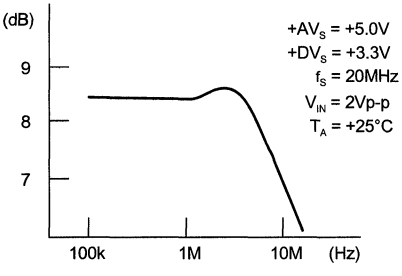
SNR vs. f_{IN}



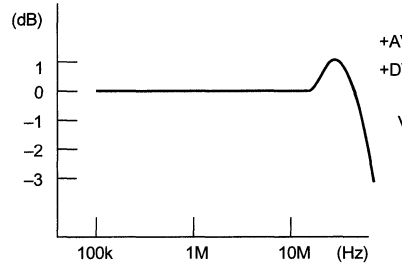
SFDR vs. f_{IN}



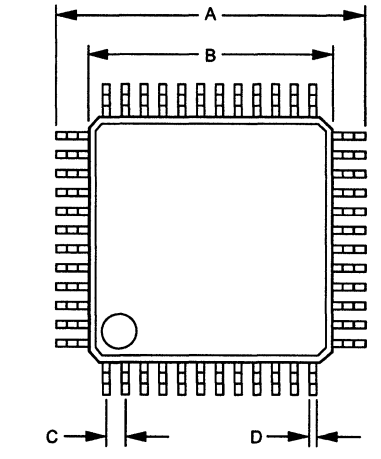
Eff. Bit vs. f_{IN}



Analog Input Bandwidth



MECHANICAL DIMENSIONS



	Inches	mm
A	0.35 ±0.008	9.0 ±0.2
B	0.27 ±0.004	7.0 ±0.1
C	0.02 ±0.003	0.5 ±0.08
D	0.007 $^{+0.003}_{-0.001}$	0.18 $^{+0.08}_{-0.03}$
E	0.315	8.0
F	0.02 ±0.008	0.5 ±0.2
G	0.005 $^{+0.002}_{-0.001}$	0.127 $^{+0.05}_{-0.02}$
H	0.06 $^{+0.008}_{-0.004}$	1.5 $^{+0.2}_{-0.1}$
I	0.004 ±0.004	0.1 ±0.1
J	0.02 ±0.008	0.5 ±0.2
K	0 to 10°	

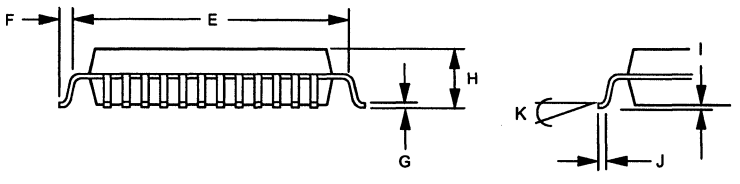


Table 3. Digital Output Truth Table

TEST MODE	LINV	MINV	LSB Bit 10	9	8	7	6	5	4	3	2	MSB Bit 1
1	0	0	P	P	P	P	P	P	P	P	P	P
1	1	0	N	N	N	N	N	N	N	N	N	P
1	0	1	P	P	P	P	P	P	P	P	P	N
1	1	1	N	N	N	N	N	N	N	N	N	N
0	1	1	1	0	1	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	1	0	1	0	0
0	1	0	1	0	1	0	1	0	1	0	1	1
0	0	0	0	1	0	1	0	1	0	1	0	1

P = Positive; N = Negative (Inverted)

ORDERING INFORMATION

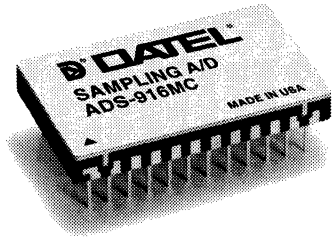
Model Number	Bits/Throughput Rate
ADS-325A	10 Bits/20MHz

DATEL®
INNOVATION and EXCELLENCE

ADS-916
14-Bit, 500kHz, Low-Power Sampling A/D Converters

FEATURES

- **14-Bit resolution**
- **500kHz sampling rate**
- **No missing codes**
- **Functionally complete**
- **Small 24-pin DDIP or SMT package**
- **Low power, 1.8 Watts maximum**
- **Operates from ±15V or ±12V supplies**
- **Unipolar 0 to +10V input range**



GENERAL DESCRIPTION

The ADS-916 is a high-performance, 14-bit, 500kHz sampling A/D converter. This device samples input signals up to Nyquist frequencies with no missing codes. The ADS-916 features outstanding dynamic performance including a THD of –90dB.

Packaged in a small 24-pin DDIP, the functionally complete ADS-916 contains a fast-settling sample/hold amplifier, a subranging (two-pass) A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL.

Requiring ±15V (or ±12V) and +5V supplies, the ADS-916 dissipates only 1.8W (1.6W for ±12V), maximum. The unit is offered with a unipolar input (0 to +10V). Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. Applications include radar, sonar, spectrum analysis, and graphic/medical imaging.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 (LSB)	24	–12V/–15V SUPPLY
2	BIT 13	23	ANALOG GROUND
3	BIT 12	22	+12V/+15V SUPPLY
4	BIT 11	21	+10V REFERENCE OUT
5	BIT 10	20	ANALOG INPUT
6	BIT 9	19	ANALOG GROUND
7	BIT 8	18	BIT 1 (MSB)
8	BIT 7	17	BIT 2
9	BIT 6	16	START CONVERT
10	BIT 5	15	$\overline{\text{EOC}}$
11	BIT 4	14	DIGITAL GROUND
12	BIT 3	13	+5V SUPPLY

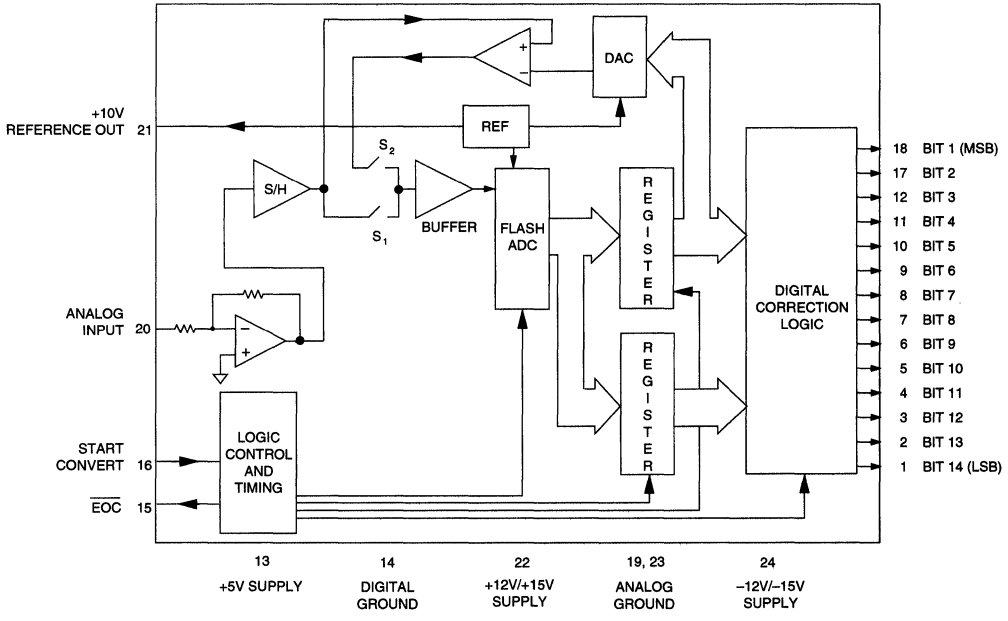


Figure 1. ADS-916 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+12V/+15V Supply (Pin 22)	0 to +16	Volts
–12V/–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 20)	–4 to +17	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–916MC/GC	0	—	+70	°C
ADS–916MM/GM	–55	—	+125	°C
Thermal Impedance				
θjc	—	5	—	°C/Watt
θca	—	22	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V (or ±12V), +V_{DD} = +5V, 500kHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Voltage Range ②	—	0 to +10	—	—	0 to +10	—	—	0 to +10	—	Volts
Input Resistance	—	1	—	—	1	—	—	1	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	200	—	—	200	—	—	200	—	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.5	—	—	±0.75	—	—	±1.5	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.5	±0.95	—	±0.5	±0.95	–0.95	±0.75	+1.25	LSB
Full Scale Absolute Accuracy	—	±0.05	±0.1	—	±0.1	±0.2	—	±0.15	±0.4	%FSR
Unipolar Offset Error (Tech Note 2)	—	±0.1	±0.2	—	±0.1	±0.2	—	±0.15	±0.4	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.25	—	±0.1	±0.25	—	±0.25	±0.4	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–91	–86	—	–91	–86	—	–90	–82	dB
100kHz to 250kHz	—	–84	–79	—	–84	–79	—	–82	–76	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–90	–85	—	–90	–85	—	–87	–81	dB
100kHz to 250kHz	—	–82	–77	—	–82	–77	—	–80	–74	dB
Signal–to–Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 100kHz	77	81	—	77	81	—	76	80	—	dB
100kHz to 250kHz	75	80	—	75	80	—	74	78	—	dB
Signal–to–Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 100kHz	77	80	—	77	80	—	75	78	—	dB
100kHz to 250kHz	72	78	—	72	78	—	70	76	—	dB
Noise	—	310	—	—	310	—	—	360	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, f_s = 500kHz, –0.5dB)	—	–86	—	—	–86	—	—	–86	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	7	—	—	7	—	—	7	—	MHz
Large Signal (–0.5dB input)	—	3	—	—	3	—	—	3	—	MHz
Feedthrough Rejection (f_{in} = 250kHz)	—	84	—	—	84	—	—	84	—	dB
Slew Rate	—	±40	—	—	±40	—	—	±40	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 10V step)	1530	1570	1610	1530	1570	1610	1530	1570	1610	ns
Overvoltage Recovery Time ⑤	—	1400	2000	—	1400	2000	—	1400	2000	ns
A/D Conversion Rate	500	—	—	500	—	—	500	—	—	kHz

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ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/°C
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	4	—	—	4	—	—	4	mA
Logic Loading "0"	—	—	4	—	—	4	—	—	4	mA
Delay, Falling Edge of $\overline{EOC}$ to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Straight Binary									
POWER REQUIREMENTS, ±15V										
Power Supply Range										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+15V Supply	—	+50	+65	—	+50	+65	—	+50	+65	mA
–15V Supply	—	–40	–50	—	–40	–50	—	–40	–50	mA
+5V Supply	—	+70	+85	—	+70	+85	—	+70	+85	mA
Power Dissipation	—	1.6	1.8	—	1.6	1.8	—	1.6	1.8	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V
POWER REQUIREMENTS, ±12V										
Power Supply Range										
+12V Supply	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	Volts
–12V Supply	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+12V Supply	—	+50	+65	—	+50	+65	—	+50	+65	mA
–12V Supply	—	–40	–50	—	–40	–50	—	–40	–50	mA
+5V Supply	—	+70	+80	—	+70	+80	—	+70	+80	mA
Power Dissipation	—	1.4	1.6	—	1.4	1.6	—	1.4	1.6	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time. There is a slight degradation in performance when using ±12V supplies.

② See Ordering Information for availability of ±5V input range. Contact DATEL for availability of other input voltage ranges.

③ A 200ns wide start convert pulse is used for all production testing. Only the rising edge of the start convert pulse is required for the device to operate (edge-triggered).

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-916 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies, as well as the REFERENCE OUTPUT (pin 21), to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-916 as possible.

2. The ADS-916 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. When operating the ADS-916 from ±12V supplies, do not drive external circuitry with the REFERENCE OUTPUT. The reference's accuracy and drift specifications may not be met, and loading the circuit may cause accuracy errors within the converter.

4. Applying a start convert pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") initiates a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

CALIBRATION PROCEDURE (Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit in Figure 2 are guaranteed to compensate for the ADS-916's initial accuracy errors and may not be able to compensate for additional system errors.

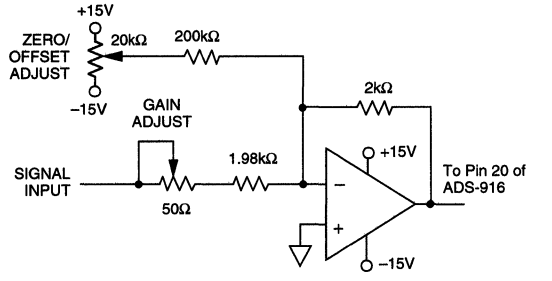

Figure 2. ADS-916 Calibration Circuit

All fixed resistors in Figure 2 should be metal-film types, and multiturn potentiometers should have TCR's of 100ppm/°C or less to minimize drift with temperature.

Table 1. Zero and Gain Adjust

INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V	+305µV	+9.999085V

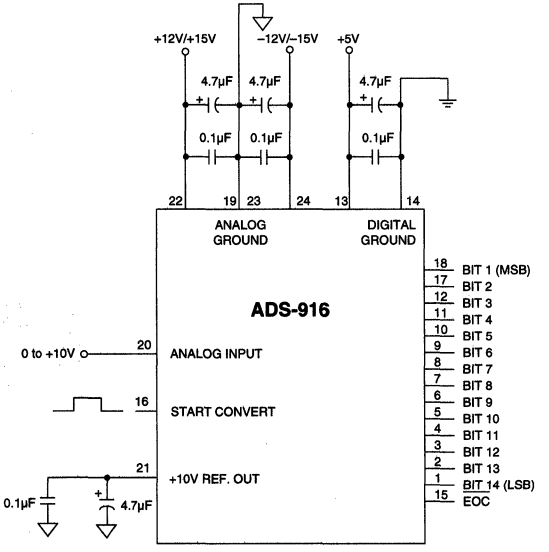

Figure 3. Typical ADS-916 Connection Diagram

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-916, offset adjusting is normally accomplished at the point where all output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+305µV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+9.999085V) .

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +305µV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are all 0's and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +9.999085V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until the output bits are all 1's and the LSB flickers between 1 and 0.

Table 2. Output Coding

INPUT VOLTAGE (0 to +10V)	UNIPOLAR SCALE	DIGITAL OUTPUT MSB LSB
+9.999390	+FS –1LSB	11 1111 1111 1111
+7.500000	+3/4 FS	11 0000 0000 0000
+5.000000	+1/2 FS	10 0000 0000 0000
+2.500000	+1/4 FS	01 0000 0000 0000
+0.000610	+1LSB	00 0000 0000 0001
0	0	00 0000 0000 0000

Coding is straight binary; 1LSB = 610µV

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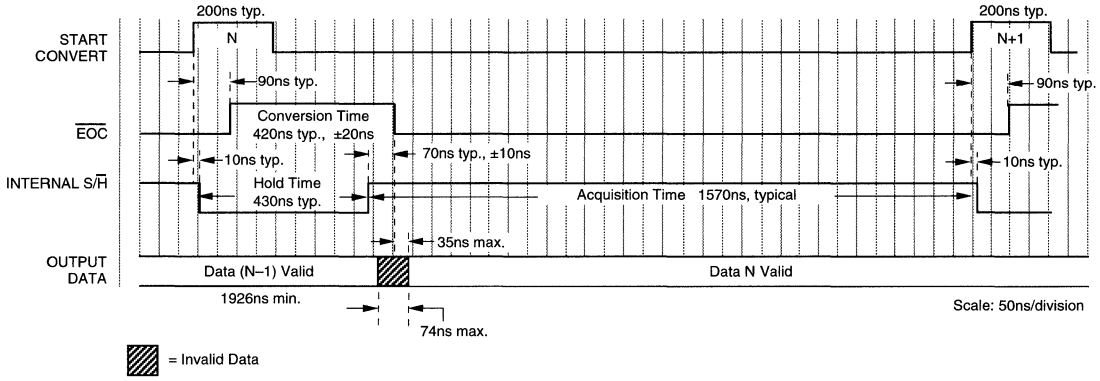


Figure 4. ADS-916 Timing Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to +125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

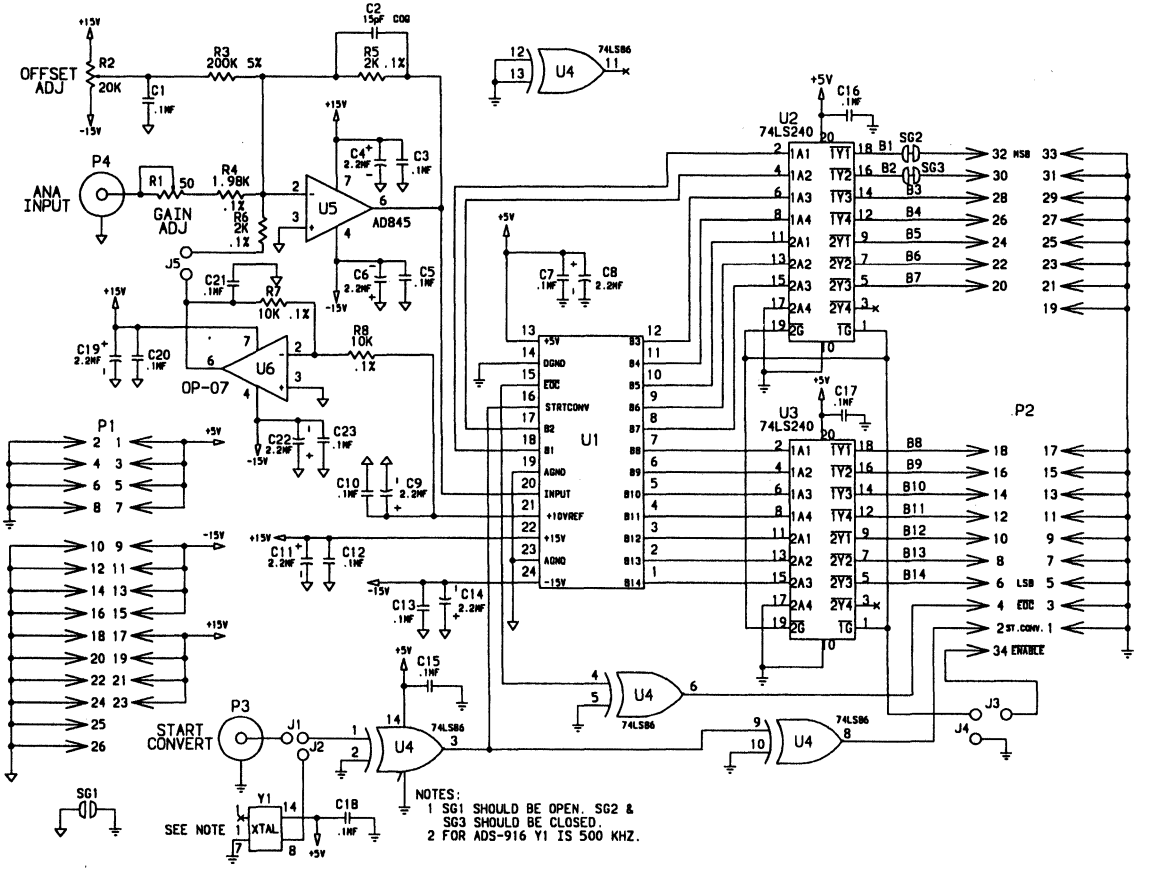


Figure 5. ADS-916 Evaluation Board Schematic

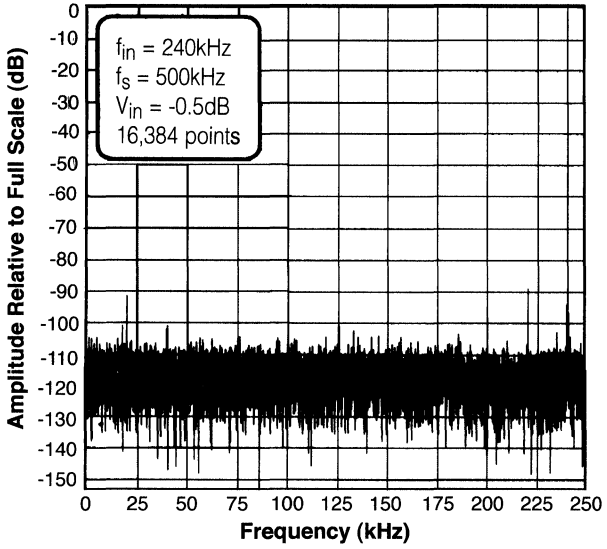


Figure 6. ADS-916 FFT Analysis

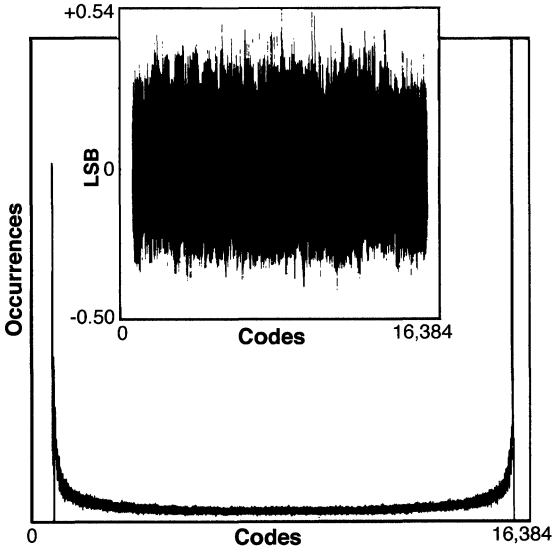
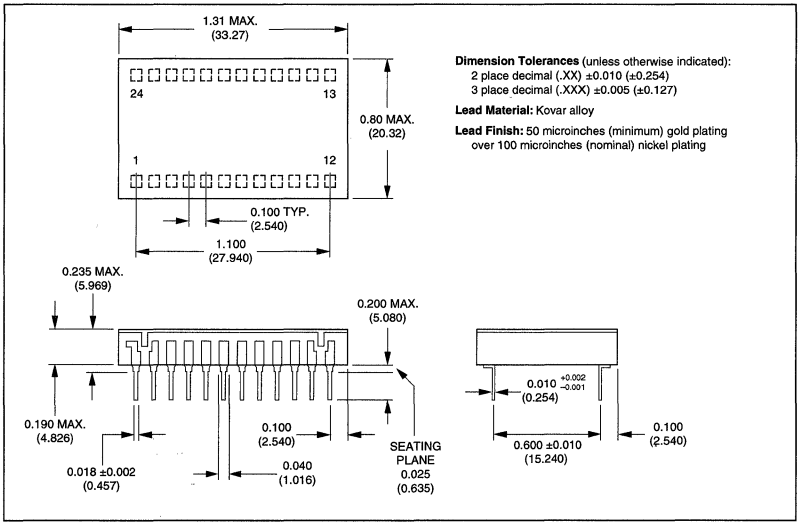


Figure 7. ADS-916 Histogram and Differential Linearity

MECHANICAL DIMENSIONS
INCHES (mm)

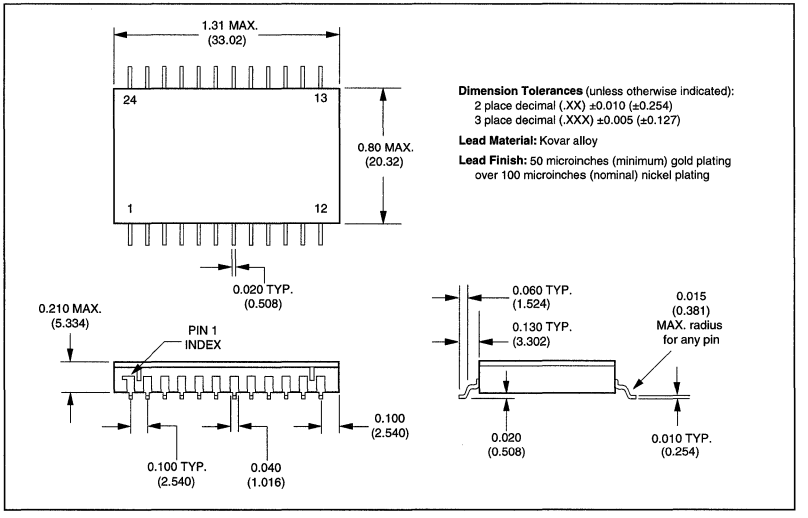
24-Pin DDIP Versions

ADS-916MC
ADS-916MM
ADS-926MC
ADS-926MM
ADS-926/883



24-Pin Surface Mount Versions

ADS-916GC
ADS-916GM
ADS-926GC
ADS-926GM



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-916MC	0 to +70°C	Unipolar (0 to +10V)
ADS-916MM	–55 to +125°C	Unipolar (0 to +10V)
ADS-916GC	0 to +70°C	Unipolar (0 to +10V)
ADS-916GM	–55 to +125°C	Unipolar (0 to +10V)
ADS-926MC	0 to +70°C	Bipolar (±5V)*
ADS-926MM	–55 to +125°C	Bipolar (±5V)*
ADS-926GC	0 to +70°C	Bipolar (±5V)*
ADS-926GM	–55 to +125°C	Bipolar (±5V)*
ADS-926/883	–55 to +125°C	Bipolar (±5V)*

ACCESSORIES

ADS-B916/917	Evaluation Board (without ADS-916)
HS-24	Heat Sink for all ADS-916/926 DDIP models

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product specification or availability of surface mount packaging, contact DATEL.

*For more information, see ADS-926 data sheet.

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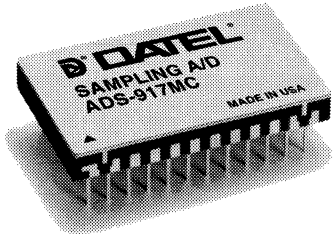
DATEL®
INNOVATION and EXCELLENCE

ADS-917
14-Bit, 1MHz, Low-Power Sampling A/D Converters

1

FEATURES

- **14-Bit resolution**
- **1MHz sampling rate**
- **No missing codes**
- **Functionally complete**
- **Small 24-pin DDIP or SMT package**
- **Low power, 1.9 Watts maximum**
- **Operates from ±15V or ±12V supplies**
- **Unipolar 0 to +10V input range**



GENERAL DESCRIPTION

The ADS-917 is a high-performance, 14-bit, 1MHz sampling A/D converter. This device samples input signals up to Nyquist frequencies with no missing codes. The ADS-917 features outstanding dynamic performance including a THD of –80dB.

Packaged in a small 24-pin DDIP, the functionally complete ADS-917 contains a fast-settling sample/hold amplifier, a subranging (two-pass) A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL.

Requiring ±15V (or ±12V) and +5V supplies, the ADS-917 dissipates only 1.9W (1.6W for ±12V), maximum. The unit is offered with a unipolar input (0 to +10V). Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. Applications include radar, sonar, spectrum analysis, and graphic/medical imaging.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 (LSB)	24	–12V/–15V SUPPLY
2	BIT 13	23	ANALOG GROUND
3	BIT 12	22	+12V/+15V SUPPLY
4	BIT 11	21	+10V REFERENCE OUT
5	BIT 10	20	ANALOG INPUT
6	BIT 9	19	ANALOG GROUND
7	BIT 8	18	BIT 1 (MSB)
8	BIT 7	17	BIT 2
9	BIT 6	16	START CONVERT
10	BIT 5	15	$\overline{\text{EOC}}$
11	BIT 4	14	DIGITAL GROUND
12	BIT 3	13	+5V SUPPLY

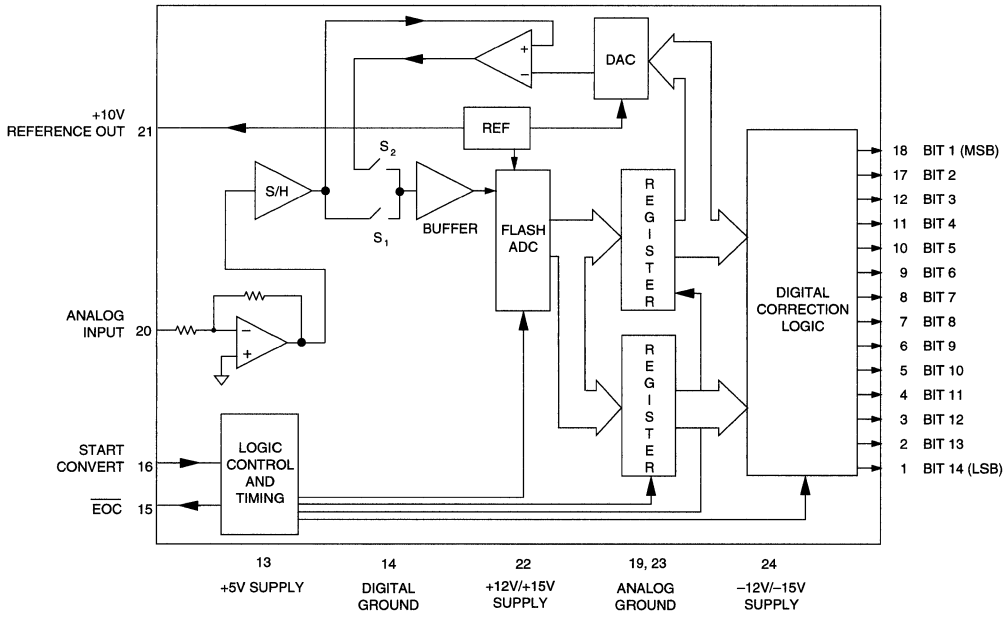


Figure 1. ADS-917 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+12V/+15V Supply (Pin 22)	0 to +16	Volts
–12V/–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to $+V_{DD}$ +0.3	Volts
Analog Input (Pin 20)	–4 to +17	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–917MC/GC	0	—	+70	°C
ADS–917MM/GM	–55	—	+125	°C
Thermal Impedance				
θjc	—	5	—	°C/Watt
θca	—	22	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, $\pm V_{CC}$ = ±15V (or ±12V), $+V_{DD}$ = +5V, 1MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	0 to +10	—	—	0 to +10	—	—	0 to +10	—	Volts
Input Resistance	—	1	—	—	1	—	—	1	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	200	—	—	200	—	—	200	—	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.5	—	—	±0.75	—	—	±1.5	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.5	±0.95	—	±0.5	±0.95	–0.95	±0.75	+1.25	LSB
Full Scale Absolute Accuracy	—	±0.05	±0.1	—	±0.1	±0.2	—	±0.15	±0.4	%FSR
Unipolar Offset Error (Tech Note 2)	—	±0.1	±0.2	—	±0.1	±0.2	—	±0.15	±0.4	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.25	—	±0.1	±0.25	—	±0.25	±0.4	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–87	–82	—	–87	–82	—	–85	–80	dB
100kHz to 500kHz	—	–81	–76	—	–81	–76	—	–79	–74	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–85	–82	—	–85	–82	—	–84	–80	dB
100kHz to 500kHz	—	–80	–76	—	–80	–76	—	–79	–74	dB
Signal–to–Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 100kHz	75	79	—	75	79	—	73	77	—	dB
100kHz to 500kHz	73	78	—	73	78	—	72	76	—	dB
Signal–to–Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 100kHz	74	77	—	74	77	—	72	76	—	dB
100kHz to 500kHz	72	76	—	72	76	—	71	75	—	dB
Noise	—	300	—	—	400	—	—	600	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, f_s = 1MHz, –0.5dB)	—	–87	—	—	–86	—	—	–85	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	7	—	—	7	—	—	7	—	MHz
Large Signal (–0.5dB input)	—	5	—	—	5	—	—	5	—	MHz
Feedthrough Rejection (f_{in} = 500kHz)	—	84	—	—	84	—	—	84	—	dB
Slew Rate	—	±60	—	—	±60	—	—	±60	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 10V step)	530	570	610	530	570	610	530	570	610	ns
Overvoltage Recovery Time ⑤	—	400	1000	—	400	1000	—	400	1000	ns
A/D Conversion Rate	1	—	—	1	—	—	1	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	−55 to +125°C MIN.	−55 to +125°C TYP.	−55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/°C
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	4	—	—	4	—	—	4	mA
Logic Loading "0"	—	—	4	—	—	4	—	—	4	mA
Delay, Falling Edge of EOC to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Straight Binary									
POWER REQUIREMENTS, ±15V										
Power Supply Range										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
−15V Supply	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+15V Supply	—	+50	+65	—	+50	+65	—	+50	+65	mA
−15V Supply	—	−41	−50	—	−41	−50	—	−41	−50	mA
+5V Supply	—	+70	+85	—	+70	+85	—	+70	+85	mA
Power Dissipation	—	1.7	1.9	—	1.7	1.9	—	1.7	1.9	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V
POWER REQUIREMENTS, ±12V										
Power Supply Range										
+12V Supply	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	Volts
−12V Supply	−11.5	−12.0	−12.5	−11.5	−12.0	−12.5	−11.5	−12.0	−12.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+12V Supply	—	+50	+65	—	+50	+65	—	+50	+65	mA
−12V Supply	—	−40	−48	—	−40	−48	—	−40	−48	mA
+5V Supply	—	+70	+80	—	+70	+80	—	+70	+80	mA
Power Dissipation	—	1.4	1.6	—	1.4	1.6	—	1.4	1.6	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② See Ordering Information for availability of ±5V input range. Contact DATEL for availability of other input voltage ranges.

③ A 200ns wide start convert pulse is used for all production testing.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid after the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-917 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies, as well as the REFERENCE OUTPUT (pin 21), to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-917 as possible.

2. The ADS-917 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. When operating the ADS-917 from ±12V supplies, do not drive external circuitry with the REFERENCE OUTPUT. The reference's accuracy and drift specifications may not be met, and loading the circuit may cause accuracy errors within the converter.

4. Applying a start convert pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") initiates a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

CALIBRATION PROCEDURE

(Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit of Figure 2 are guaranteed to compensate for the ADS-917's initial accuracy errors and may not be able to compensate for additional system errors.

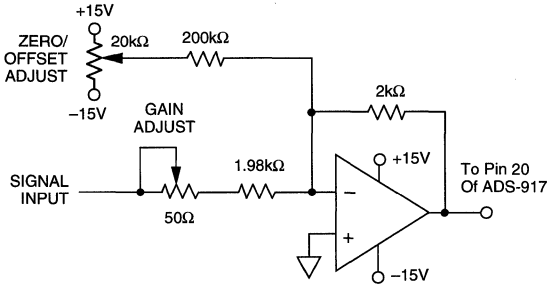


Figure 2. ADS-917 Calibration Circuit

All fixed resistors in Figure 2 should be metal-film types, and multiturn potentiometers should have TCR's of 100ppm/°C or less to minimize drift with temperature.

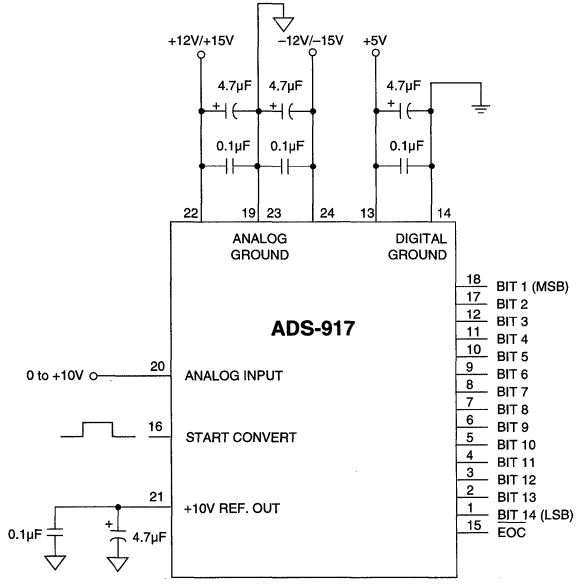


Figure 3. Typical ADS-917 Connection Diagram

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-917, offset adjusting is normally accomplished at the point where all output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+305µV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+9.999085V) .

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +305µV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are all 0's and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +9.999085V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until the output bits are all 1's and the LSB flickers between 1 and 0.

Table 1. Zero and Gain Adjust

INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V	+305µV	+9.999085V

Table 2. Output Coding

INPUT VOLTAGE (0 to +10V)	UNIPOLAR SCALE	DIGITAL OUTPUT MSB LSB
+9.999390	+FS –1LSB	11 1111 1111 1111
+7.500000	+3/4 FS	11 0000 0000 0000
+5.000000	+1/2 FS	10 0000 0000 0000
+2.500000	+1/4 FS	01 0000 0000 0000
+0.000610	+1LSB	00 0000 0000 0001
0	0	00 0000 0000 0000

Coding is straight binary; 1LSB = 610µV

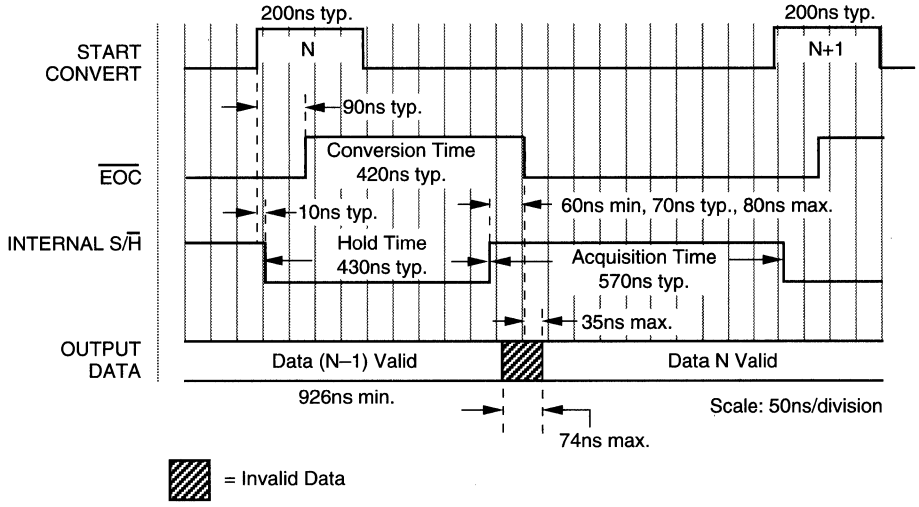


Figure 4. ADS-917 Timing Diagram

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These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

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In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

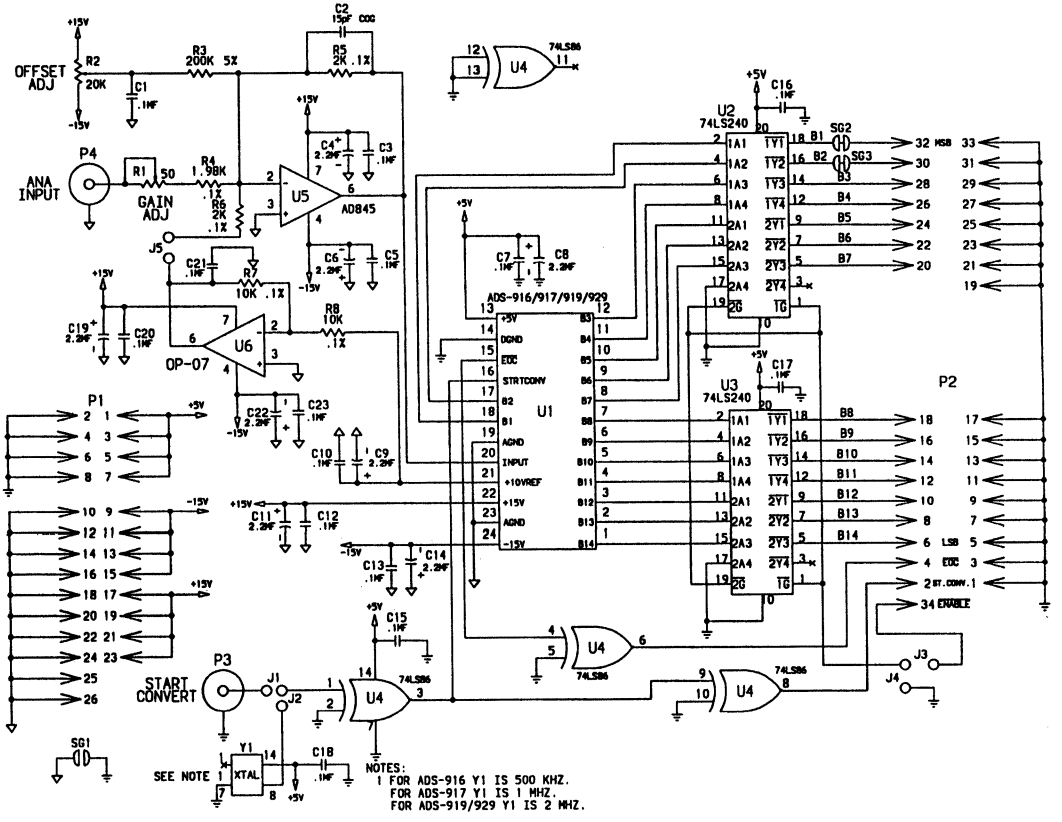


Figure 5. ADS-917 Evaluation Board Schematic

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For Immediate Assistance 800-233-2765

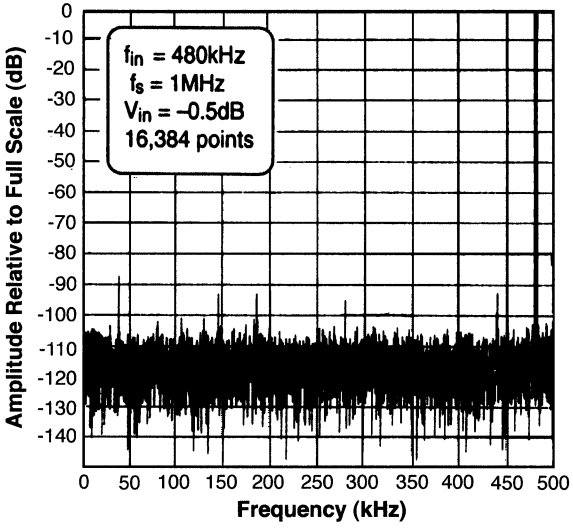


Figure 6. ADS-917 FFT Analysis

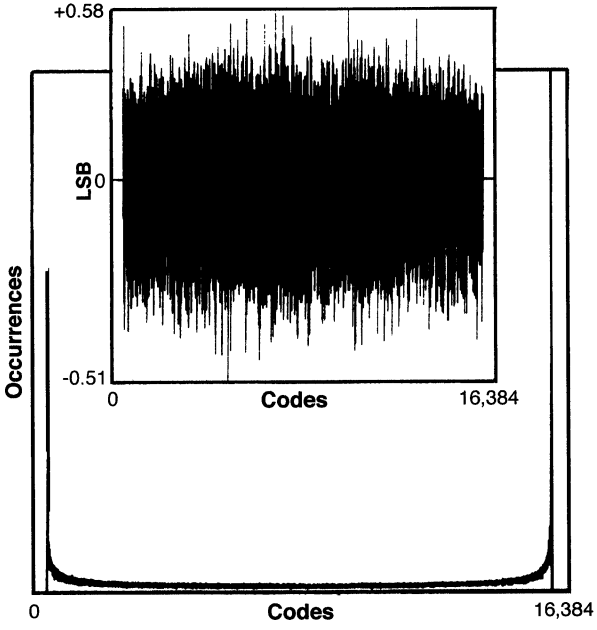
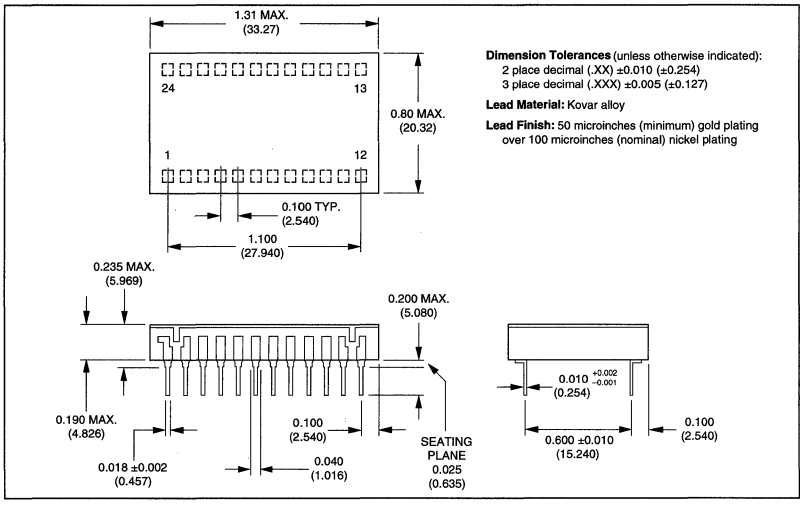


Figure 7. ADS-917 Histogram and Differential Linearity

MECHANICAL DIMENSIONS
INCHES (mm)

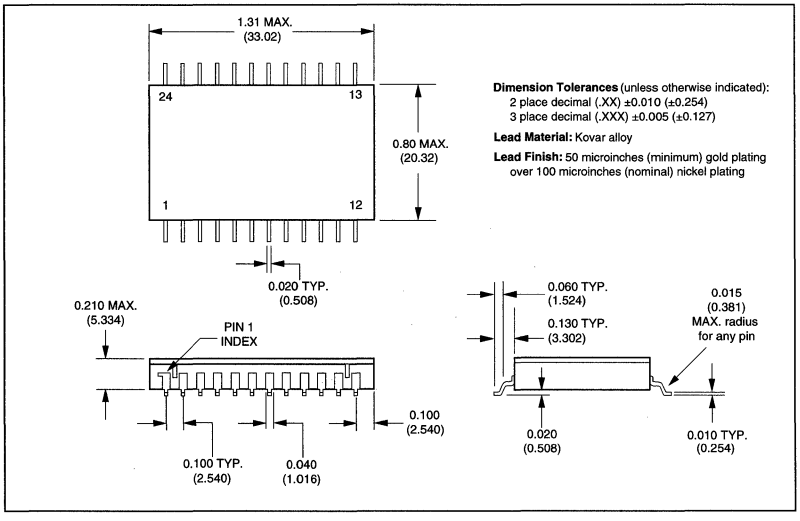
24-Pin DDIP Versions

ADS-917MC
ADS-917MM
ADS-927MC
ADS-927MM
ADS-927/883



24-Pin Surface Mount Versions

ADS-917GC
ADS-917GM
ADS-927GC
ADS-927GM



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-917MC	0 to +70°C	Unipolar (0 to +10V)
ADS-917MM	–55 to +125°C	Unipolar (0 to +10V)
ADS-917GC	0 to +70°C	Unipolar (0 to +10V)
ADS-917GM	–55 to +125°C	Unipolar (0 to +10V)
ADS-927MC	0 to +70°C	Bipolar (±5V)*
ADS-927MM	–55 to +125°C	Bipolar (±5V)*
ADS-927GC	0 to +70°C	Bipolar (±5V)*
ADS-927GM	–55 to +125°C	Bipolar (±5V)*
ADS-927/883	–55 to +125°C	Bipolar (±5V)*

ACCESSORIES

ADS-B916/917	Evaluation Board (without ADS-917)
HS-24	Heat Sink for all ADS-917/927 DDIP models

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product specification or availability of surface mount packaging, contact DATEL.

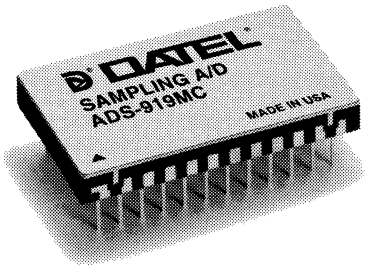
*For more information, see ADS-927 data sheet.

DATEL®
INNOVATION and EXCELLENCE

ADS-919
14-Bit, 2MHz, Low-Power Sampling A/D Converters

FEATURES

- **14-Bit resolution**
- **2MHz sampling rate**
- **No missing codes**
- **Functionally complete**
- **Small 24-pin DDIP or SMT package**
- **Low power, 1.8 Watts**
- **Operates from ±15V or ±12V supplies**
- **Edge-triggered, no pipeline delay**
- **Unipolar 0 to +10V input range**



GENERAL DESCRIPTION

The ADS-919 is a high-performance, 14-bit, 2MHz sampling A/D converter. This device samples input signals up to Nyquist frequencies with no missing codes. The ADS-919 features outstanding dynamic performance including a THD of –74dB.

Packaged in a small 24-pin DDIP, the functionally complete ADS-919 contains a fast-settling sample/hold amplifier, a subranging (two-pass) A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL.

Requiring ±15V (or ±12V) and +5V supplies, the ADS-919 typically dissipates 1.8W (1.5W for ±12V). The unit is offered with a unipolar input (0 to +10V). Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. Applications include radar, sonar, spectrum analysis, and graphic/medical imaging.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 (LSB)	24	–12V/–15V SUPPLY
2	BIT 13	23	ANALOG GROUND
3	BIT 12	22	+12V/+15V SUPPLY
4	BIT 11	21	+10V REFERENCE OUT
5	BIT 10	20	ANALOG INPUT
6	BIT 9	19	ANALOG GROUND
7	BIT 8	18	BIT 1 (MSB)
8	BIT 7	17	BIT 2
9	BIT 6	16	START CONVERT
10	BIT 5	15	$\overline{\text{EOC}}$
11	BIT 4	14	DIGITAL GROUND
12	BIT 3	13	+5V SUPPLY

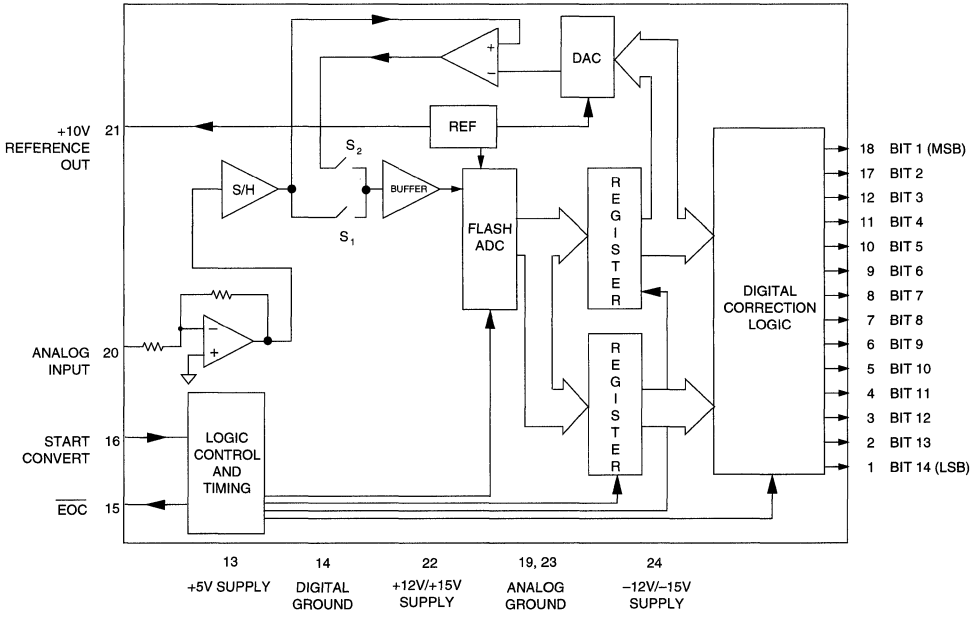


Figure 1. ADS-919 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+12V/+15V Supply (Pin 22)	0 to +16	Volts
–12V/–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 20)	–4 to +17	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–919MC/GC	0	—	+70	°C
ADS–919MM/GM	–55	—	+125	°C
Thermal Impedance				
θjc		6		°C/Watt
θca		24		°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V (or ±12V), +V_{DD} = +5V, 2MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	0 to +10	—	—	0 to +10	—	—	0 to +10	—	Volts
Input Resistance	—	1	—	—	1	—	—	1	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2	—	—	+2	—	—	+2	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	50	200	—	50	200	—	50	200	—	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.5	—	—	±0.75	—	—	±1	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.5	±0.95	—	±0.5	±0.95	—	±0.5	±0.99	LSB
Full Scale Absolute Accuracy	—	±0.1	±0.3	—	±0.2	±0.4	—	±0.4	±0.8	%FSR
Unipolar Offset Error (Tech Note 2)	—	±0.1	±0.25	—	±0.2	±0.4	—	±0.4	±1.25	%FSR
Gain Error (Tech Note 2)	—	±0.13	±0.3	—	±0.3	±0.5	—	±0.5	±1	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 500kHz	—	–76	–72	—	–76	–70	—	–74	–69	dB
500kHz to 1MHz	—	–76	–70	—	–76	–70	—	–74	–69	dB
Total Harmonic Distortion (–0.5dB)										
dc to 500kHz	—	–74	–70	—	–74	–70	—	–73	–69	dB
500kHz to 1MHz	—	–74	–70	—	–74	–70	—	–73	–68	dB
Signal–to–Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 500kHz	74	77	—	74	77	—	71	76	—	dB
500kHz to 1MHz	74	77	—	74	77	—	71	75	—	dB
Signal–to–Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 500kHz	70	74	—	70	74	—	68	73	—	dB
500kHz to 1MHz	70	74	—	70	74	—	68	72	—	dB
Two–tone Intermodulation Distortion (f_{in} = 200kHz, 500kHz, f_s = 2MHz, –0.5dB)	—	–80	—	—	–80	—	—	–79	—	dB
Noise	—	300	—	—	350	—	—	450	—	µVrms
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	9	—	—	9	—	—	9	—	MHz
Large Signal (–0.5dB input)	—	8	—	—	8	—	—	8	—	MHz
Feedthrough Rejection (f_{in} = 1MHz)	—	82	—	—	82	—	—	82	—	dB
Slew Rate	—	±200	—	—	±200	—	—	±200	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 10V step)	150	190	230	150	190	230	150	190	230	ns
Overvoltage Recovery Time ⑤	—	400	500	—	400	500	—	400	500	ns
A/D Conversion Rate	2	—	—	2	—	—	2	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	−55 to +125°C MIN.	−55 to +125°C TYP.	−55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10	+10.05	+9.95	+10	+10.05	+9.95	+10	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/°C
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	4	—	—	4	—	—	4	mA
Logic Loading "0"	—	—	4	—	—	4	—	—	4	mA
Delay, Falling Edge of EOC to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Straight Binary									
POWER REQUIREMENTS, ±15V										
Power Supply Range										
+15V Supply	+14.5	+15	+15.5	+14.5	+15	+15.5	+14.5	+15	+15.5	Volts
−15V Supply	−14.5	−15	−15.5	−14.5	−15	−15.5	−14.5	−15	−15.5	Volts
+5V Supply	+4.75	+5	+5.25	+4.75	+5	+5.25	+4.75	+5	+5.25	Volts
Power Supply Current										
+15V Supply	—	+45	+60	—	+45	+60	—	+45	+60	mA
−15V Supply	—	−45	−60	—	−45	−60	—	−45	−60	mA
+5V Supply	—	+85	+95	—	+85	+95	—	+85	+95	mA
Power Dissipation	—	1.8	2	—	1.8	2	—	1.8	2	Watts
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V
POWER REQUIREMENTS, ±12V										
Power Supply Range										
+12V Supply	+11.5	+12	+12.5	+11.5	+12	+12.5	+11.5	+12	+12.5	Volts
−12V Supply	−11.5	−12	−12.5	−11.5	−12	−12.5	−11.5	−12	−12.5	Volts
+5V Supply	+4.75	+5	+5.25	+4.75	+5	+5.25	+4.75	+5	+5.25	Volts
Power Supply Current										
+12V Supply	—	+45	+65	—	+45	+65	—	+45	+65	mA
−12V Supply	—	−45	−60	—	−45	−60	—	−45	−60	mA
+5V Supply	—	+85	+95	—	+85	+95	—	+85	+95	mA
Power Dissipation	—	1.5	1.7	—	1.5	1.7	—	1.5	1.7	Watts
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time. There is a slight degradation in performance when using ±12V supplies.

② See Ordering Information for availability of ±5V input range. Contact DATEL for availability of other input voltage ranges.

③ A 200ns wide start convert pulse is used for all production testing.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid after the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-919 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies, as well as the REFERENCE OUTPUT (pin 21), to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-919 as possible.

2. The ADS-919 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. When operating the ADS-919 from ±12V supplies, do not drive external circuitry with the REFERENCE OUTPUT. The reference's accuracy and drift specifications may not be met, and loading the circuit may cause accuracy errors within the converter.

Table 1. Zero and Gain Adjust

INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V	+305µV	+9.999085V

CALIBRATION PROCEDURE

(Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit of Figure 2 are guaranteed to compensate for the ADS-919's initial accuracy errors and may not be able to compensate for additional system errors.

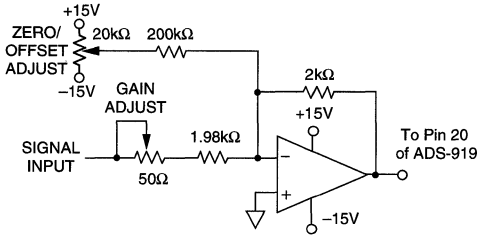


Figure 2. ADS-919 Calibration Circuit

All fixed resistors in Figure 2 should be metal-film types, and multiturn potentiometers should have TCR's of 100ppm/°C or less to minimize drift with temperature.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-919, offset adjusting is normally accomplished at the point where all output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+305µV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+9.999085V) .

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +305µV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are all 0's and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +9.999085V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until the output bits are all 1's and the LSB flickers between 1 and 0.

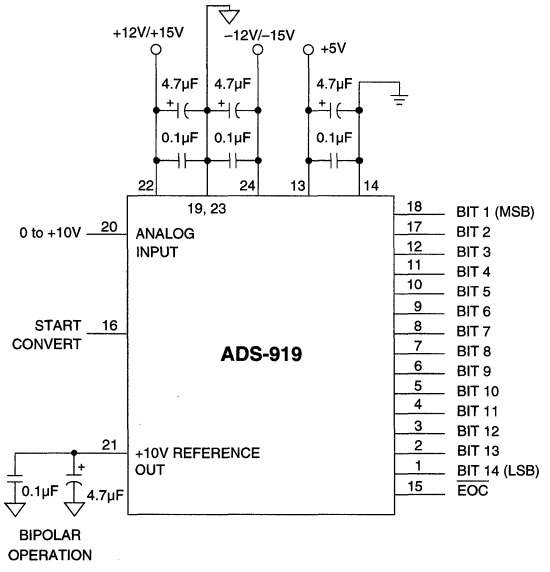


Figure 3. Typical ADS-919 Connection Diagram

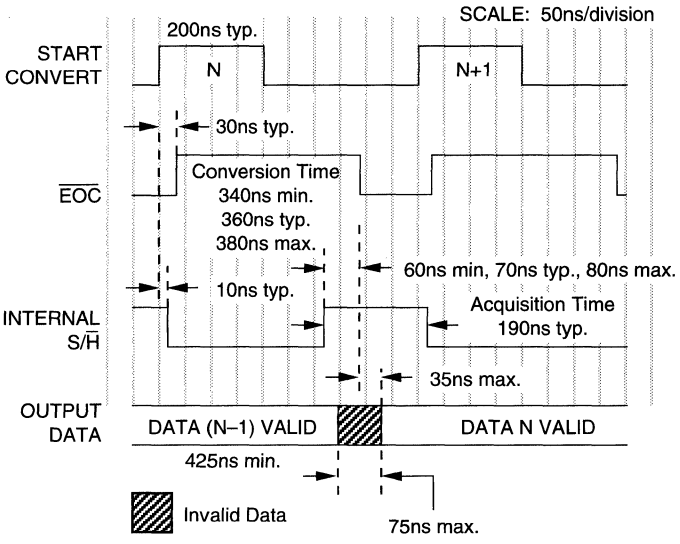


Figure 4. ADS-919 Timing Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

Table 2. Output Coding

INPUT VOLTAGE (0 to +10V)	UNIPOLAR SCALE	DIGITAL OUTPUT MSB LSB
+9.999390	+FS –1LSB	11 1111 1111 1111
+7.500000	+3/4 FS	11 0000 0000 0000
+5.000000	+1/2 FS	10 0000 0000 0000
+2.500000	+1/4 FS	01 0000 0000 0000
+0.000610	+1LSB	00 0000 0000 0001
0	0	00 0000 0000 0000

Coding is straight binary; 1LSB = 610µV

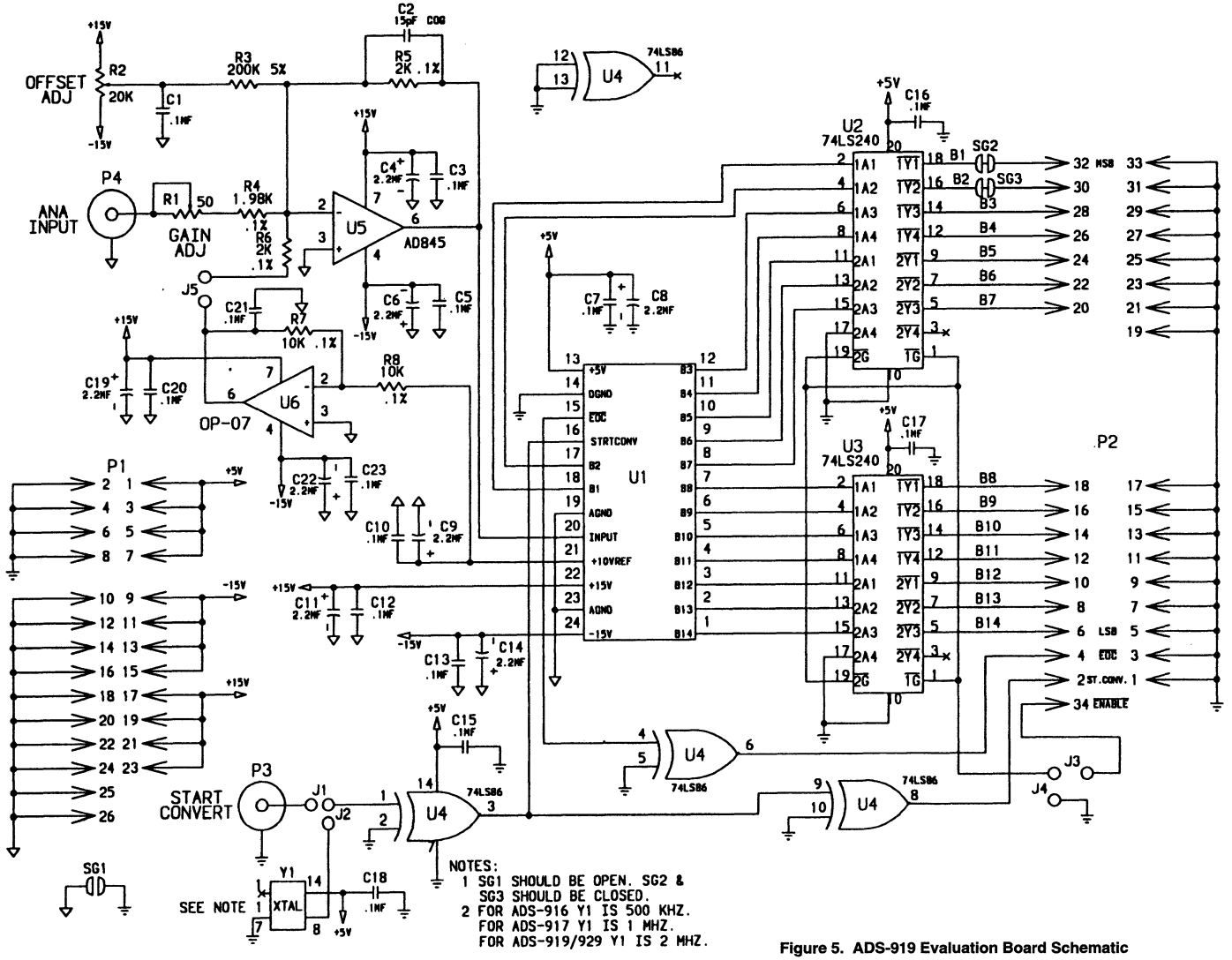


Figure 5. ADS-919 Evaluation Board Schematic

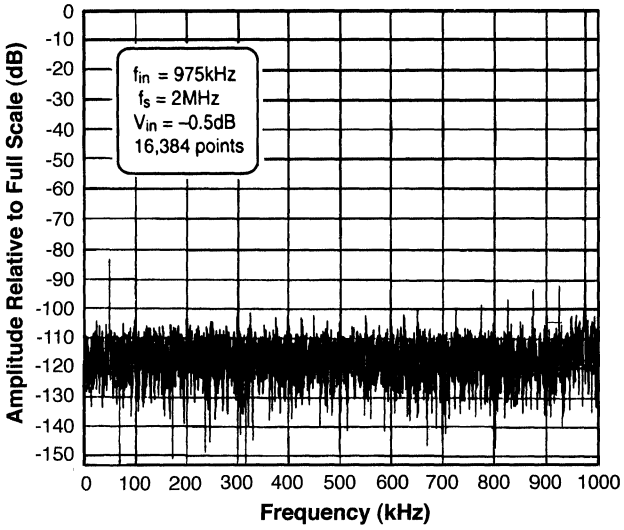


Figure 6. ADS-919 FFT Analysis

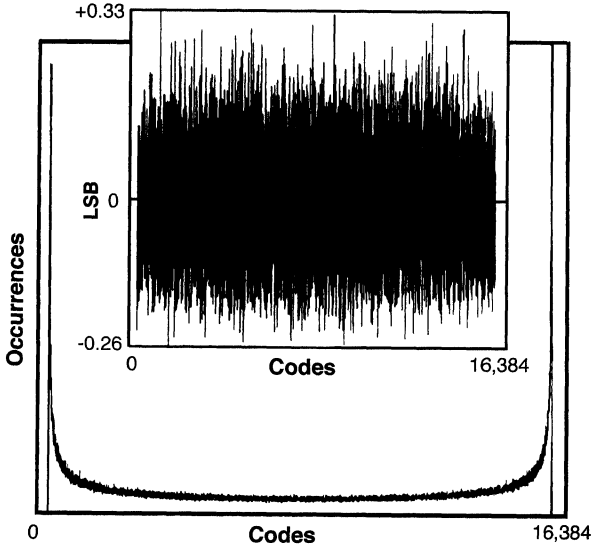
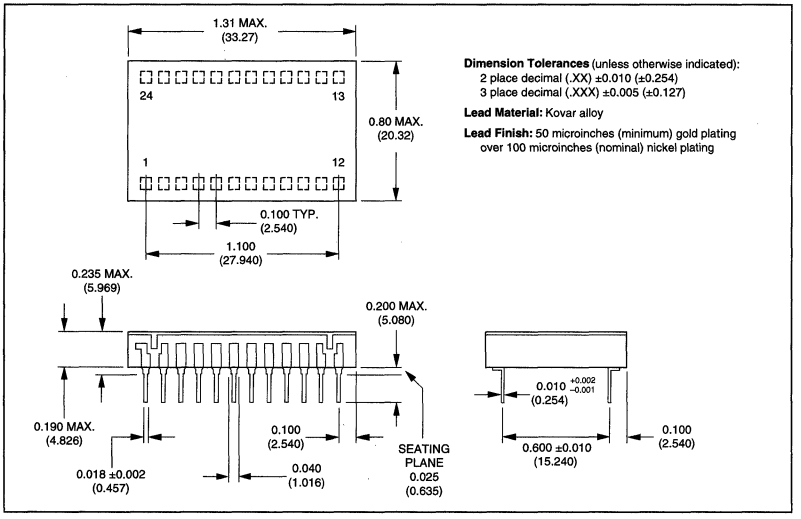


Figure 7. ADS-919 Histogram and Differential Nonlinearity

MECHANICAL DIMENSIONS
INCHES (mm)

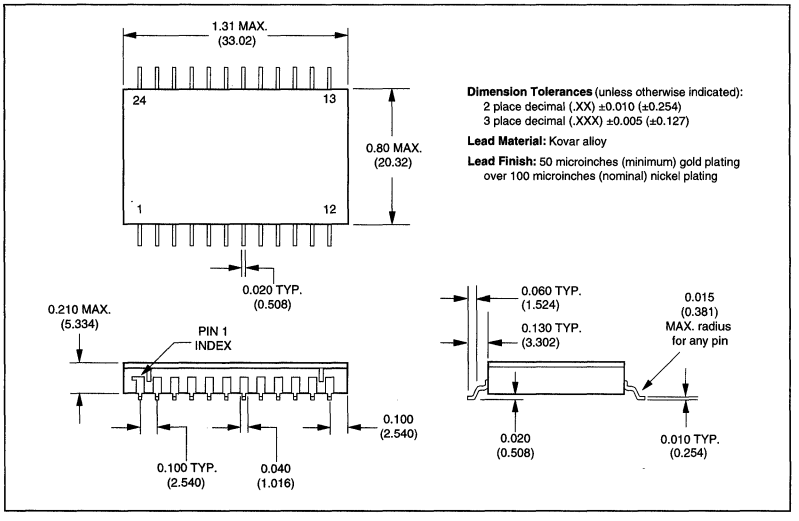
24-Pin DDIP Versions

ADS-919MC
ADS-919MM
ADS-929MC
ADS-929MM
ADS-929/883



Surface Mount Versions

ADS-919GC
ADS-919GM
ADS-929GC
ADS-929GM



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-919MC	0 to +70°C	Unipolar (0 to +10V)
ADS-919MM	–55 to +125°C	Unipolar (0 to +10V)
ADS-919GC	0 to +70°C	Unipolar (0 to +10V)
ADS-919GM	–55 to +125°C	Unipolar (0 to +10V)
ADS-929MC	0 to +70°C	Bipolar (±5V)*
ADS-929MM	–55 to +125°C	Bipolar (±5V)*
ADS-929/883	–55 to +125°C	Bipolar (±5V)*
ADS-929GC	0 to +70°C	Bipolar (±5V)*
ADS-929GM	–55 to +125°C	Bipolar (±5V)*

ACCESSORIES

ADS-B919/929	Evaluation Board (without ADS-919)
HS-24	Heat Sink for all ADS-919/929 DDIP models

Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product specification, contact DATEL.

*For more information, see ADS-929 data sheet.

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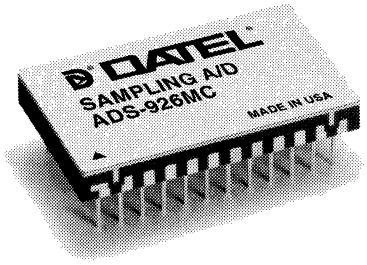
INNOVATION and EXCELLENCE

ADS-926
14-Bit, 500kHz, Low-Power Sampling A/D Converters

FEATURES

- **14-Bit resolution**
- **500kHz sampling rate**
- **No missing codes**
- **Functionally complete**
- **Small 24-pin DDIP or SMT package**
- **Low power, 1.75 Watts maximum**
- **Samples up to Nyquist frequencies**
- **Outstanding dynamic performance**
- **Bipolar ±5V input range**



GENERAL DESCRIPTION

The ADS-926 is a high-performance, 14-bit, 500kHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes and exhibits outstanding dynamic performance that surpasses most 16-bit, 500kHz sampling A/D's. THD and SNR, for example, are typically –90dB and 80dB when converting full-scale input signals up to 100kHz.

Packaged in a small 24-pin DDIP, the functionally complete ADS-926 contains a fast-settling sample-and-hold amplifier, a subranging (two-pass) A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL.

Requiring ±15V and +5V supplies, the ADS-926 dissipates only 1.75W, maximum. The unit is offered with a bipolar input (–5V to +5V). Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 (LSB)	24	–15V SUPPLY
2	BIT 13	23	ANALOG GROUND
3	BIT 12	22	+15V SUPPLY
4	BIT 11	21	+10V REFERENCE OUT
5	BIT 10	20	ANALOG INPUT
6	BIT 9	19	ANALOG GROUND
7	BIT 8	18	BIT 1 (MSB)
8	BIT 7	17	BIT 2
9	BIT 6	16	START CONVERT
10	BIT 5	15	$\overline{\text{EOC}}$
11	BIT 4	14	DIGITAL GROUND
12	BIT 3	13	+5V SUPPLY

Applications include radar, sonar, spectrum analysis, and graphic/medical imaging. Contact DATEL for information on devices screened to MIL-STD-883 or packaged in SMT packages.

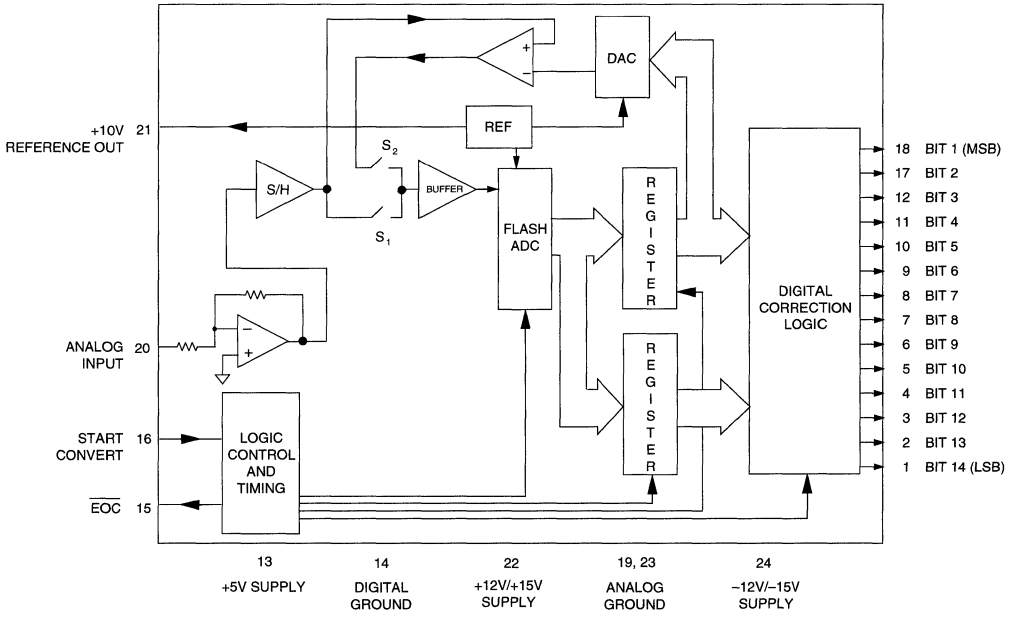


Figure 1. ADS-926 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +16	Volts
–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 20)	±15	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–926MC/GC	0	—	+70	°C
ADS–926MM/GM/883	–55	—	+125	°C
Thermal Impedance				
θjc	—	6	—	°C/Watt
θca	—	24	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V, 500kHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

ANALOG INPUT	+25°C			0 to +70°C			–55 to +125°C			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Voltage Range ②	—	±5	—	—	±5	—	—	±5	—	Volts
Input Resistance	—	1	—	—	1	—	—	1	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	175	200	225	175	200	225	175	200	225	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.5	—	—	±0.75	—	—	±1.5	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.5	±0.95	—	±0.5	±0.95	—	±0.75	±0.99	LSB
Full Scale Absolute Accuracy	—	±0.08	±0.15	—	±0.15	±0.25	—	±0.3	±0.5	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.05	±0.1	—	±0.1	±0.25	—	±0.15	±0.3	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.05	±0.1	—	±0.1	±0.25	—	±0.25	±0.4	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.15	—	±0.15	±0.25	—	±0.25	±0.4	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–92	–88	—	–90	–85	—	–88	–81	dB
100kHz to 250kHz	—	–90	–85	—	–90	–85	—	–86	–80	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–90	–86	—	–89	–82	—	–87	–78	dB
100kHz to 250kHz	—	–87	–82	—	–87	–82	—	–81	–76	dB
Signal–to–Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 100kHz	78	80	—	78	80	—	74	78	—	dB
100kHz to 250kHz	78	80	—	78	80	—	74	77	—	dB
Signal–to–Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 100kHz	77	79	—	77	79	—	74	78	—	dB
100kHz to 250kHz	77	79	—	77	79	—	73	77	—	dB
Noise	—	300	—	—	300	—	—	300	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, f_s = 500kHz, –0.5dB)	—	–87	—	—	–86	—	—	–85	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	7	—	—	7	—	—	7	—	MHz
Large Signal (–0.5dB input)	—	3	—	—	3	—	—	3	—	MHz
Feedthrough Rejection (f_{in} = 250kHz)	—	84	—	—	84	—	—	84	—	dB
Slew Rate	—	±40	—	—	±40	—	—	±40	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time										
(to ±0.003%FSR, 10V step)	1335	1390	1445	1335	1390	1445	1335	1390	1445	ns
Overvoltage Recovery Time ⑤	—	1400	2000	—	1400	2000	—	1400	2000	ns
A/D Conversion Rate	500	—	—	500	—	—	500	—	—	kHz

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ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	−55 to +125°C MIN.	−55 to +125°C TYP.	−55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/°C
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	4	—	—	4	—	—	4	mA
Logic Loading "0"	—	—	4	—	—	4	—	—	4	mA
Delay, Falling Edge of $\overline{EOC}$ to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Offset Binary									
POWER REQUIREMENTS										
Power Supply Range ⑥										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
−15V Supply	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+15V Supply	—	+41	+60	—	+41	+60	—	+41	+60	mA
−15V Supply	—	−23	−40	—	−23	−40	—	−23	−40	mA
+5V Supply	—	+71	+85	—	+71	+85	—	+71	+85	mA
Power Dissipation	—	1.3	1.75	—	1.3	1.75	—	1.3	1.75	Watts
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT pulse) must be present during warmup periods. The device must be continuously converting during this time.

② See Ordering Information for 0 to +10V input range. Contact DATEL for availability of other input ranges.

③ A 200ns wide start convert pulse is used for all production testing. For applications requiring less than a 500kHz sampling rate, a wider start convert pulse can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR} + \text{Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

⑥ The ADS-926 can operate from either ±12V or ±15V supplies. There is, however, a slight degradation in performance when using ±12V supplies.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-926 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies, as well as the REFERENCE OUTPUT (pin 21), to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-926 as possible.

2. The ADS-926 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. Applying a start convert pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") initiates a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

Table 1. Zero and Gain Adjust

INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±5V	+305µV	+4.999085V

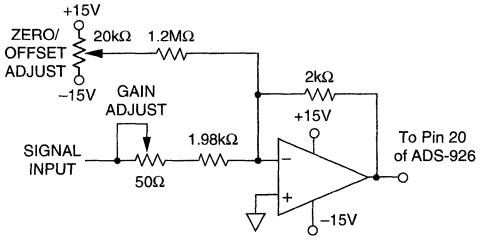

Figure 2. ADS-926 Calibration Circuit

CALIBRATION PROCEDURE
(Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit of Figure 2 are guaranteed to compensate for the ADS-926's initial accuracy errors and may not be able to compensate for additional system errors.

All fixed resistors in Figure 2 should be metal-film types, and multiturn potentiometers should have TCR's of 100ppm/°C or less to minimize drift with temperature.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-926, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+305µV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+4.999085V) .

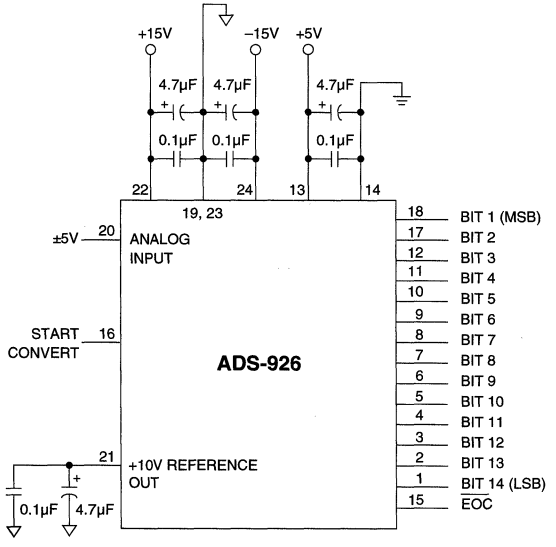

Figure 3. Typical ADS-926 Connection Diagram

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +305µV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are a 1 and all 0's and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +4.999085V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until the output bits are all 1's and the LSB flickers between 1 and 0.

Table 2. Output Coding

OFFSET BINARY MSB LSB	INPUT RANGE ±5V	BIPOLAR SCALE
11 1111 1111 1111	+4.99939	+FS -1 LSB
11 1000 0000 0000	+3.75000	+3/4 FS
11 0000 0000 0000	+2.50000	+1/2 FS
10 0000 0000 0000	0.00000	0
01 0000 0000 0000	−2.50000	−1/2 FS
00 1000 0000 0000	−3.75000	−3/4 FS
00 0000 0000 0001	−4.99939	−FS +1 LSB
00 0000 0000 0000	−5.00000	−FS

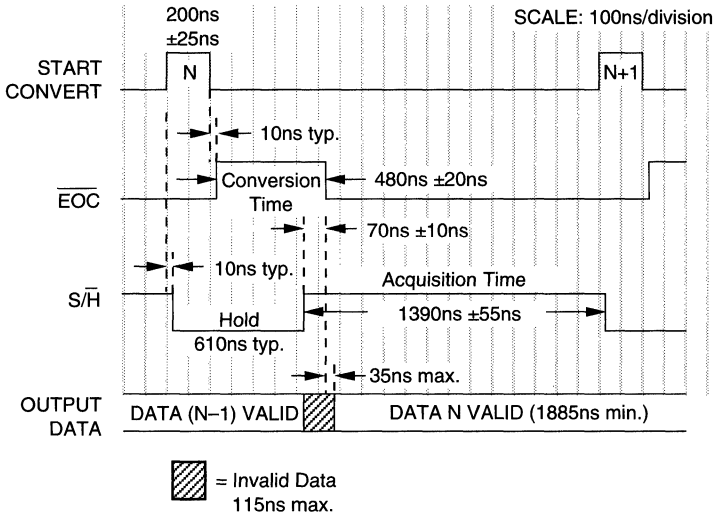

Figure 4. ADS-926 Timing Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

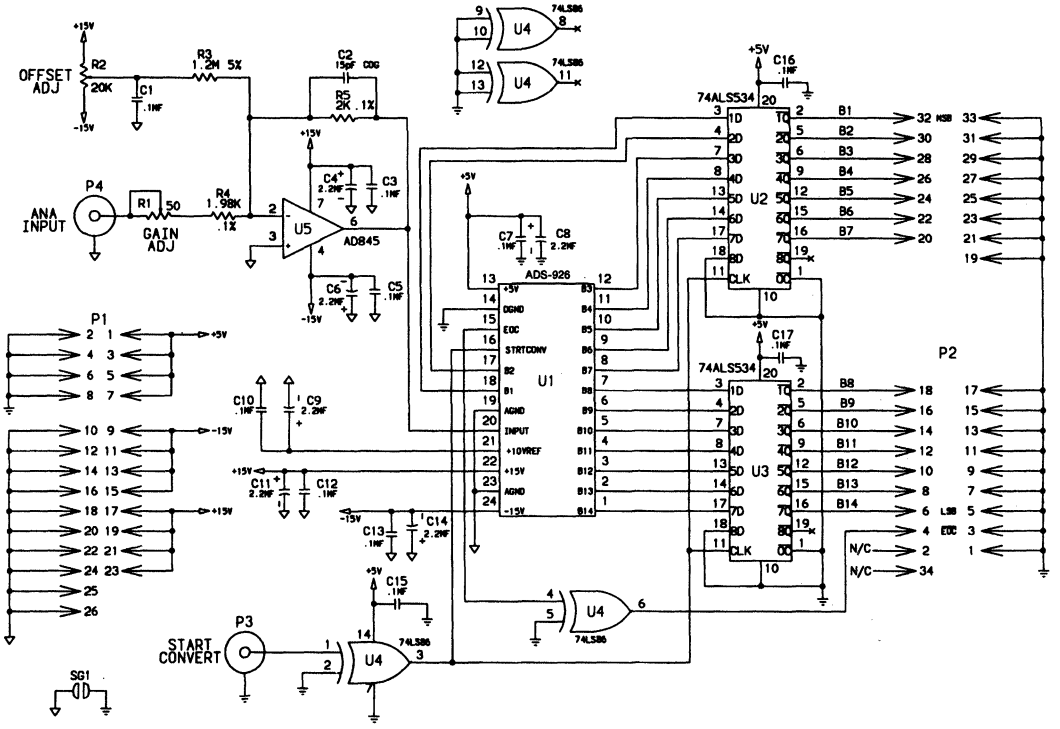

Figure 5. ADS-926 Evaluation Board Schematic

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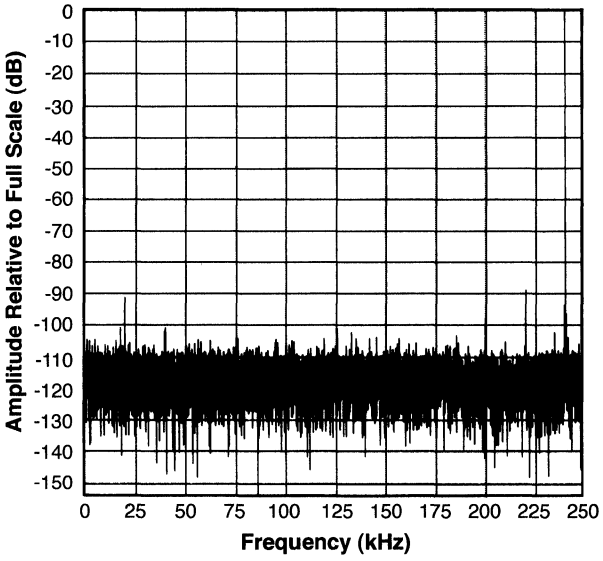


Figure 6. ADS-926 FFT Analysis
(f_{IN} = 240kHz, f_S = 500kHz, V_{IN} = –0.5dB, 16,384 points)

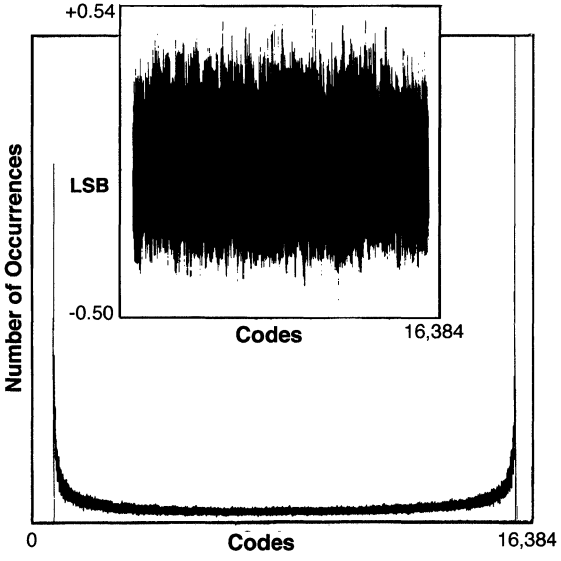
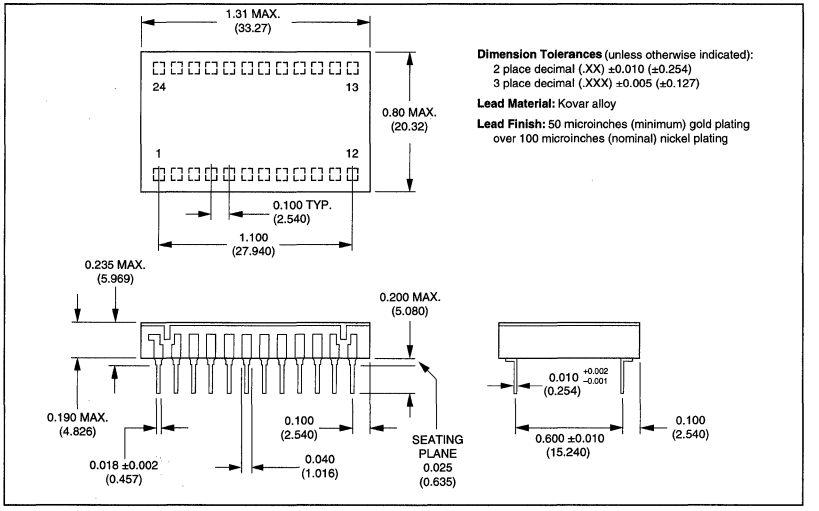


Figure 7. ADS-926 Histogram and Differential Linearity

MECHANICAL DIMENSIONS
INCHES (mm)

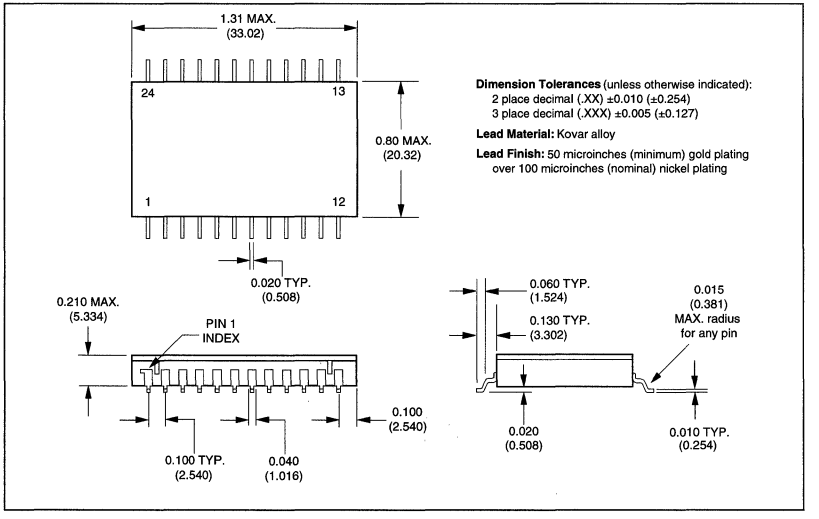
24-Pin DDIP Versions

ADS-926MC
ADS-926MM
ADS-926/883
ADS-916MC
ADS-916MM



24-Pin Surface Mount Versions

ADS-926GC
ADS-926GM
ADS-916GC
ADS-916GM



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-926MC	0 to +70°C	Bipolar (±5V)
ADS-926MM	–55 to +125°C	Bipolar (±5V)
ADS-926/883	–55 to +125°C	Bipolar (±5V)
ADS-926GC	0 to +70°C	Bipolar (±5V)
ADS-926GM	–55 to +125°C	Bipolar (±5V)
ADS-916MC	0 to +70°C	Unipolar (0 to +10V)*
ADS-916MM	–55 to +125°C	Unipolar (0 to +10V)*
ADS-916GC	0 to +70°C	Unipolar (0 to +10V)*
ADS-916GM	–55 to +125°C	Unipolar (0 to +10V)*

ACCESSORIES

ADS-B926/927	Evaluation Board (without ADS-926)
HS-24	Heat Sink for all ADS-916/926 DDIP models

Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product specification or availability of surface mount packaging, contact DATEL.

*For more information, see ADS-916 data sheet.

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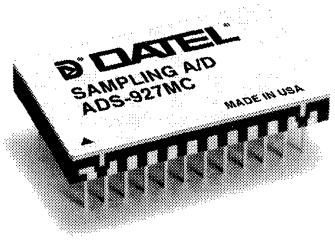
FEATURES

- **14-Bit resolution**
- **1MHz sampling rate**
- **No missing codes**
- **Functionally complete**
- **Small 24-pin DDIP or SMT package**
- **Low power, 1.9 Watts maximum**
- **Operates from ±15V or ±12V supplies**
- **Bipolar ±5V input range**



GENERAL DESCRIPTION

The ADS-927 is a high-performance, 14-bit, 1MHz sampling A/D converter. This device samples input signals up to Nyquist frequencies with no missing codes. The ADS-927 features outstanding dynamic performance including a THD of –80dB.

Packaged in a small 24-pin DDIP, the functionally complete ADS-927 contains a fast-settling sample/hold amplifier, a subranging (two-pass) A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL.

Requiring ±15V (or ±12V) and +5V supplies, the ADS-927 dissipates only 1.95W (1.65W for ±12V), maximum. The unit is offered with a bipolar input (–5V to +5V). Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. Applications include radar, sonar, spectrum analysis, and graphic/medical imaging.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 (LSB)	24	–12V/–15V SUPPLY
2	BIT 13	23	ANALOG GROUND
3	BIT 12	22	+12V/+15V SUPPLY
4	BIT 11	21	+10V REFERENCE OUT
5	BIT 10	20	ANALOG INPUT
6	BIT 9	19	ANALOG GROUND
7	BIT 8	18	BIT 1 (MSB)
8	BIT 7	17	BIT 2
9	BIT 6	16	START CONVERT
10	BIT 5	15	$\overline{EOC}$
11	BIT 4	14	DIGITAL GROUND
12	BIT 3	13	+5V SUPPLY

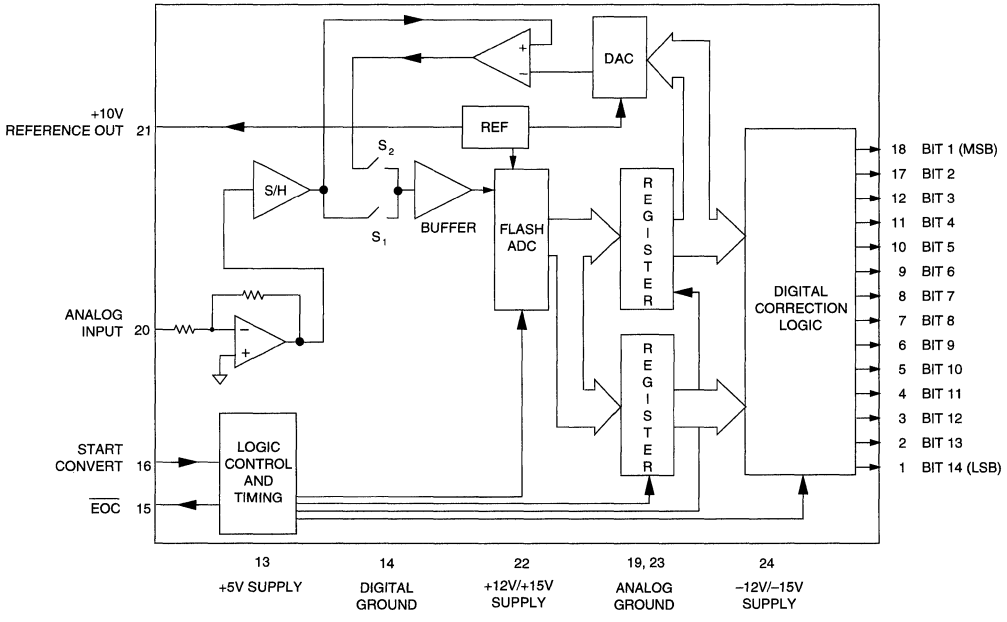


Figure 1. ADS-927 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+12V/+15V Supply (Pin 22)	0 to +16	Volts
–12V/–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 20)	–4 to +17	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–927MC/GC	0	—	+70	°C
ADS–927MM/GM/883	–55	—	+125	°C
Thermal Impedance				
θjc	—	6	—	°C/Watt
θca	—	24	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V (or ±12V), +V_{DD} = +5V, 1MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	±5	—	—	±5	—	—	±5	—	Volts
Input Resistance	—	1	—	—	1	—	—	1	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	175	200	225	175	200	225	175	200	225	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.5	—	—	±0.75	—	—	±1.5	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.5	±0.95	—	±0.5	±0.95	—	±0.75	+0.99	LSB
Full Scale Absolute Accuracy	—	±0.08	±0.15	—	±0.15	±0.25	—	±0.3	±0.5	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.05	±0.1	—	±0.1	±0.25	—	±0.15	±0.3	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.05	±0.1	—	±0.1	±0.25	—	±0.25	±0.4	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.15	—	±0.15	±0.25	—	±0.25	±0.4	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–91	–83	—	–90	—	—	–88	—	dB
100kHz to 500kHz	—	–82	–78	—	–82	–78	—	–80	–77	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–90	–81	—	–89	—	—	–87	—	dB
100kHz to 500kHz	—	–80	–76	—	–80	–76	—	–79	–74	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)										
dc to 100kHz	77	79	—	74	78	—	73	77	—	dB
100kHz to 500kHz	75	78	—	74	78	—	73	76	—	dB
Signal–to–Noise Ratio ④ (& distortion, –0.5dB)										
dc to 100kHz	76	78	—	73	77	—	71	76	—	dB
100kHz to 500kHz	73	76	—	73	76	—	71	75	—	dB
Noise	—	350	—	—	350	—	—	350	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, f_s = 1MHz, –0.5dB)	—	–87	—	—	–86	—	—	–85	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	7	—	—	7	—	—	7	—	MHz
Large Signal (–0.5dB input)	—	5	—	—	5	—	—	5	—	MHz
Feedthrough Rejection (f_{in} = 500kHz)	—	84	—	—	84	—	—	84	—	dB
Slew Rate	—	±60	—	—	±60	—	—	±60	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 10V step)	335	390	445	335	390	445	335	390	445	ns
Overvoltage Recovery Time ⑤	—	400	1000	—	400	1000	—	400	1000	ns
A/D Conversion Rate	1	—	—	1	—	—	1	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/°C
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	4	—	—	4	—	—	4	mA
Logic Loading "0"	—	—	4	—	—	4	—	—	4	mA
Delay, Falling Edge of EOC to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Offset Binary									
POWER REQUIREMENTS, ±15V										
Power Supply Range										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+15V Supply	—	+43	+65	—	+43	+65	—	+43	+65	mA
–15V Supply	—	–25	–45	—	–25	–45	—	–25	–45	mA
+5V Supply	—	+71	+80	—	+71	+80	—	+71	+80	mA
Power Dissipation	—	1.6	1.95	—	1.6	1.95	—	1.6	1.95	Watts
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V
POWER REQUIREMENTS, ±12V										
Power Supply Range										
+12V Supply	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	Volts
–12V Supply	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+12V Supply	—	+42	+65	—	+42	+65	—	+42	+65	mA
–12V Supply	—	–25	–45	—	–25	–45	—	–25	–45	mA
+5V Supply	—	+71	+80	—	+71	+80	—	+71	+80	mA
Power Dissipation	—	1.4	1.65	—	1.4	1.65	—	1.4	1.65	Watts
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② See Ordering Information for 0 to +10V input range. Contact DATEL for availability of other input voltage ranges.

③ A 200ns wide start convert pulse is used for all production testing. For applications requiring less than a 1MHz sampling rate, a wider start convert pulse can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid after the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-927 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies, as well as the REFERENCE OUTPUT (pin 21), to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-927 as possible.

2. The ADS-927 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. When operating the ADS-927 from ±12V supplies, do not drive external circuitry with the REFERENCE OUTPUT. The reference's accuracy and drift specifications may not be met, and loading the circuit may cause accuracy errors within the converter.

4. Applying a start convert pulse while a conversion is in progress (EOC = logic "1") initiates a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

CALIBRATION PROCEDURE

(Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit of Figure 2 are guaranteed to compensate for the ADS-927's initial accuracy errors and may not be able to compensate for additional system errors.

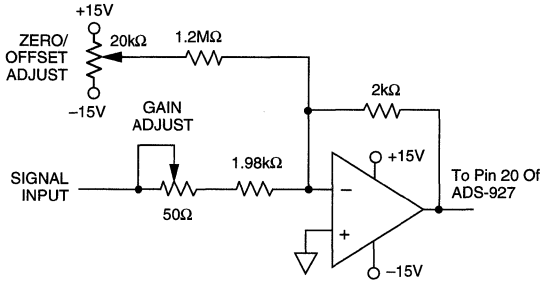


Figure 2. ADS-927 Calibration Circuit

All fixed resistors in Figure 2 should be metal-film types, and multiturn potentiometers should have TCR's of 100ppm/°C or less to minimize drift with temperature.

Table 1. Zero and Gain Adjust

INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±5V	+305µV	+4.999085V

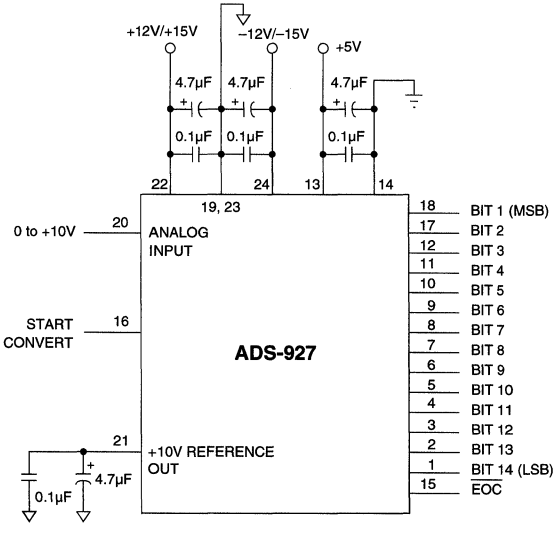


Figure 3. Typical ADS-927 Connection Diagram

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-927, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+305µV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+4.999085V) .

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +305µV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are a 1 and all 0's and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +4.999085V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until the output bits are all 1's and the LSB flickers between 1 and 0.

Table 2. Output Coding

OFFSET BINARY MSB LSB	INPUT RANGE ±5V	BIPOLAR SCALE
11 1111 1111 1111	+4.99939	+FS -1 LSB
11 1000 0000 0000	+3.75000	+3/4 FS
11 0000 0000 0000	+2.50000	+1/2 FS
10 0000 0000 0000	0.00000	0
01 0000 0000 0000	−2.50000	−1/2 FS
00 1000 0000 0000	−3.75000	−3/4 FS
00 0000 0000 0001	−4.99939	−FS +1 LSB
00 0000 0000 0000	−5.00000	−FS

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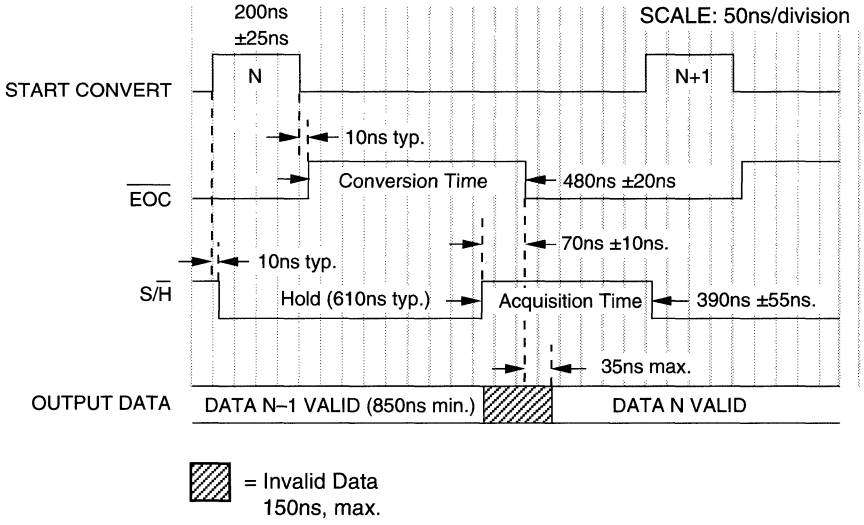


Figure 4. ADS-927 Timing Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

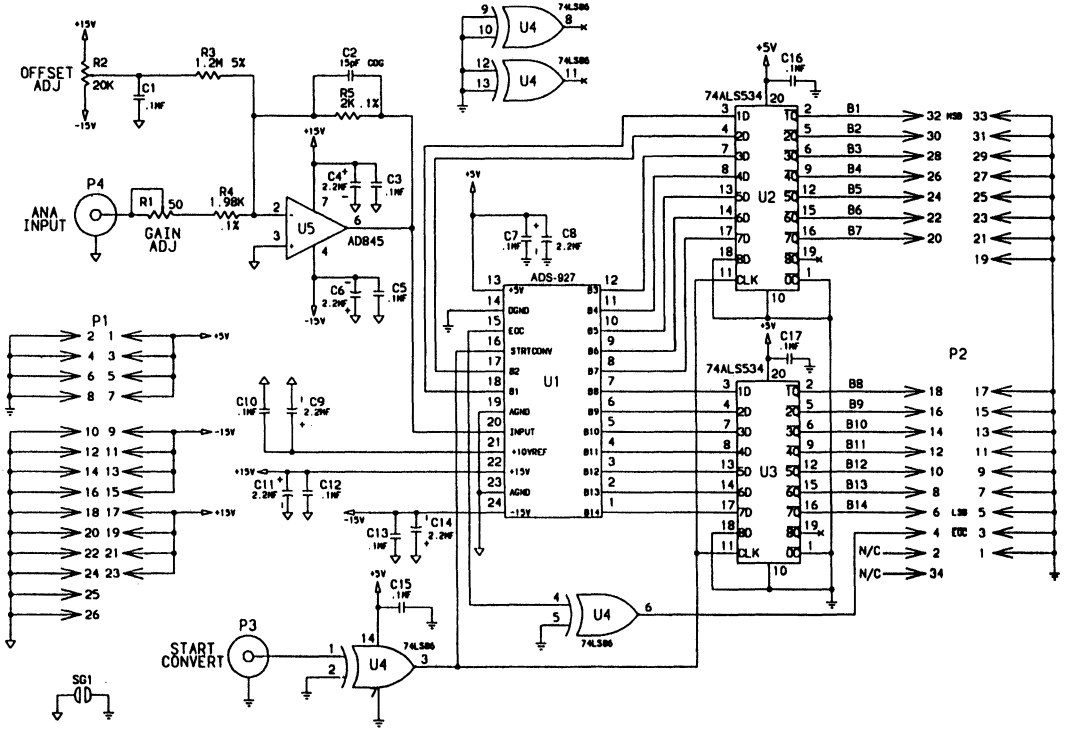


Figure 5. ADS-927 Evaluation Board Schematic

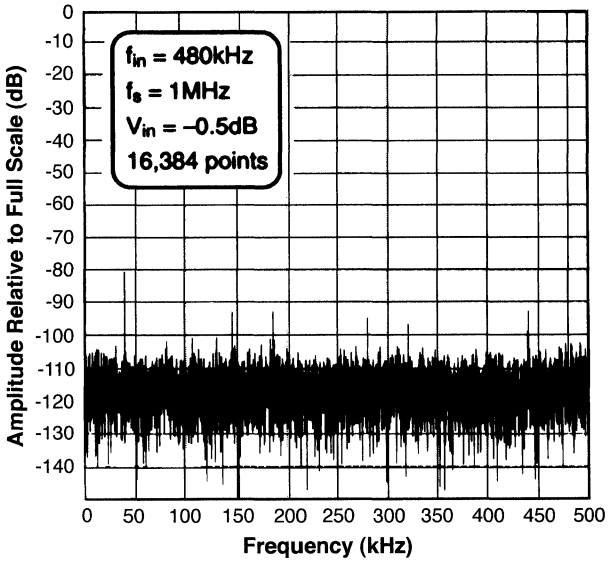


Figure 6. ADS-927 FFT Analysis

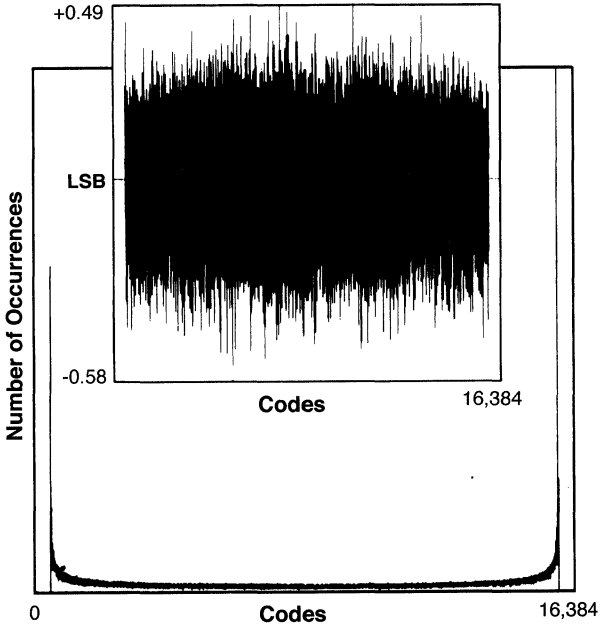
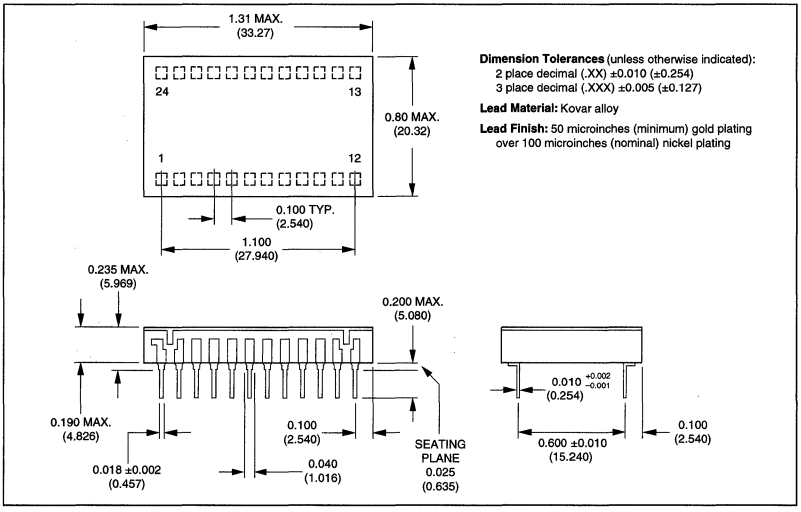


Figure 7. ADS-927 Histogram and Differential Linearity

MECHANICAL DIMENSIONS
INCHES (mm)

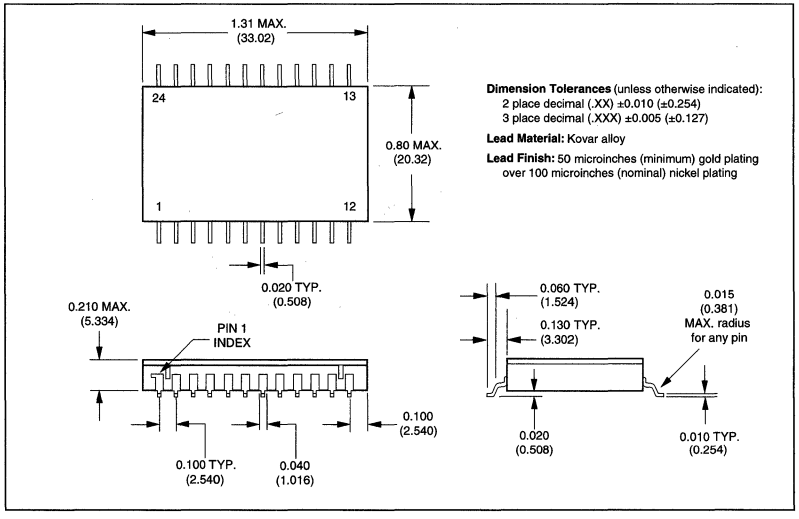
24-Pin DDIP Versions

ADS-927MC
ADS-927MM
ADS-927/883
ADS-917MC
ADS-917MM



24-Pin Surface Mount Versions

ADS-927GC
ADS-927GM
ADS-917GC
ADS-917GM



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-927MC	0 to +70°C	Bipolar (±5V)
ADS-927MM	–55 to +125°C	Bipolar (±5V)
ADS-927GC	0 to +70°C	Bipolar (±5V)
ADS-927GM	–55 to +125°C	Bipolar (±5V)
ADS-927/883	–55 to +125°C	Bipolar (±5V)
ADS-917MC	0 to +70°C	Unipolar (0 to +10V)*
ADS-917MM	–55 to +125°C	Unipolar (0 to +10V)*
ADS-917GC	0 to +70°C	Unipolar (0 to +10V)*
ADS-917GM	–55 to +125°C	Unipolar (0 to +10V)*

ACCESSORIES

ADS-B926/927 Evaluation Board (without ADS-927)
HS-24 Heat Sink for all ADS-917/927 DDIP models

Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product specification or availability of surface mount packaging, contact DATEL.

*For more information, see ADS-917 data sheet.

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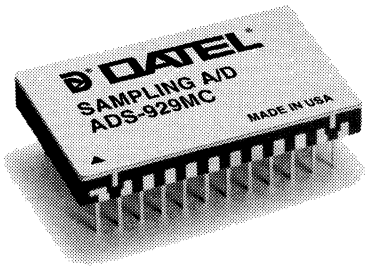
INNOVATION and EXCELLENCE

ADS-929
14-Bit, 2MHz, Low-Power Sampling A/D Converters

1

FEATURES

- **14-Bit resolution**
- **2MHz sampling rate**
- **No missing codes**
- **Functionally complete**
- **Small 24-pin DDIP or SMT package**
- **Low power, 1.7 Watts**
- **Operates from ±15V or ±12V supplies**
- **Edge-triggered, no pipeline delay**
- **Bipolar ±5V input range**



GENERAL DESCRIPTION

The ADS-929 is a high-performance, 14-bit, 2MHz sampling A/D converter. This device samples input signals up to Nyquist frequencies with no missing codes. The ADS-929 features outstanding dynamic performance including a THD of –79dB.

Packaged in a small 24-pin DDIP, the functionally complete ADS-929 contains a fast-settling sample/hold amplifier, a subranging (two-pass) A/D converter, a precise voltage reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL.

Requiring ±15V (or ±12V) and +5V supplies, the ADS-929 typically dissipates 1.7W (1.4W for ±12V). The unit is offered with a bipolar input (–5V to +5V). Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. Applications include radar, sonar, spectrum analysis, and graphic/medical imaging.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 (LSB)	24	–12V/–15V SUPPLY
2	BIT 13	23	ANALOG GROUND
3	BIT 12	22	+12V/+15V SUPPLY
4	BIT 11	21	+10V REFERENCE OUT
5	BIT 10	20	ANALOG INPUT
6	BIT 9	19	ANALOG GROUND
7	BIT 8	18	BIT 1 (MSB)
8	BIT 7	17	BIT 2
9	BIT 6	16	START CONVERT
10	BIT 5	15	$\overline{\text{EOC}}$
11	BIT 4	14	DIGITAL GROUND
12	BIT 3	13	+5V SUPPLY

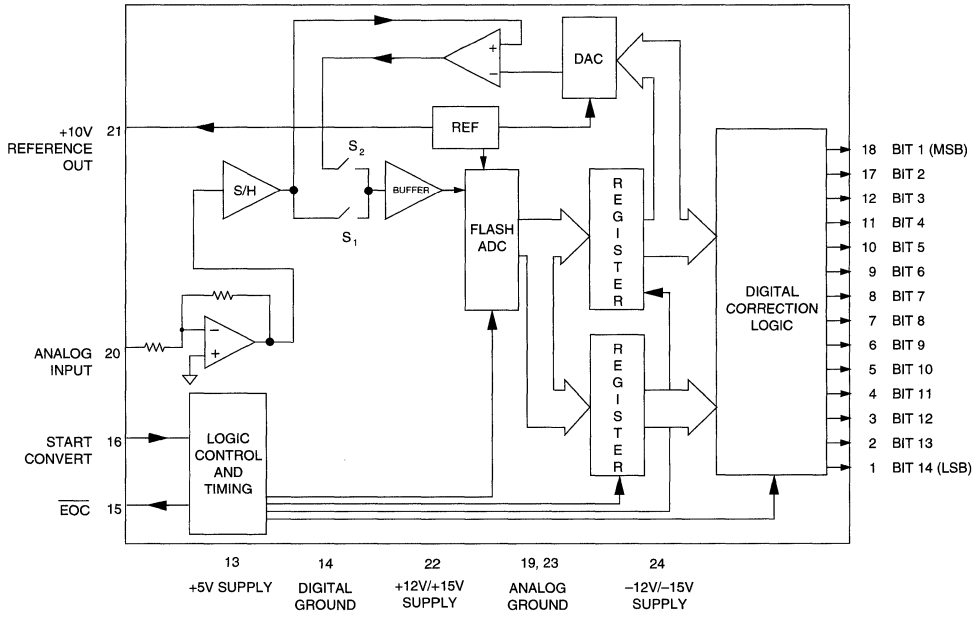


Figure 1. ADS-929 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+12V/+15V Supply (Pin 22)	0 to +16	Volts
–12V/–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 20)	±15	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–929MC/GC	0	—	+70	°C
ADS–929MM/GM/883	–55	—	+125	°C
Thermal Impedance				
θjc		6		°C/Watt
θca		24		°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V (or ±12V), +V_{DD} = +5V, 2MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Voltage Range ②	—	±5	—	—	±5	—	—	±5	—	Volts
Input Resistance	—	1	—	—	1	—	—	1	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	50	200	—	50	200	—	50	200	—	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.5	—	—	±0.75	—	—	±1	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.5	±0.95	—	±0.5	±0.95	—	±0.5	±0.99	LSB
Full Scale Absolute Accuracy	—	±0.05	±0.15	—	±0.15	±0.4	—	±0.3	±0.5	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.05	±0.15	—	±0.1	±0.25	—	±0.4	±0.75	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.05	±0.15	—	±0.15	±0.4	—	±0.4	±0.95	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.3	—	±0.3	±0.5	—	±0.5	±1.25	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 500kHz	—	–80	–75	—	–80	–75	—	–79	–74	dB
500kHz to 1MHz	—	–80	–74	—	–80	–74	—	–74	–67	dB
Total Harmonic Distortion (–0.5dB)										
dc to 500kHz	—	–79	–74	—	–79	–74	—	–77	–72	dB
500kHz to 1MHz	—	–79	–74	—	–79	–74	—	–72	–67	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)										
dc to 500kHz	76	78	—	76	78	—	75	77	—	dB
500kHz to 1MHz	75	77	—	75	77	—	74	76	—	dB
Signal–to–Noise Ratio ④ (& distortion, –0.5dB)										
dc to 500kHz	72	75	—	72	75	—	71	74	—	dB
500kHz to 1MHz	70	75	—	70	75	—	67	73	—	dB
Two–tone Intermodulation Distortion (f_{in} = 200kHz, 500kHz, f_s = 2MHz, –0.5dB)	—	–83	—	—	–82	—	—	–80	—	dB
Noise	—	300	—	—	450	—	—	600	—	µVrms
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	9	—	—	9	—	—	9	—	MHz
Large Signal (–0.5dB input)	—	8	—	—	8	—	—	8	—	MHz
Feedthrough Rejection (f_{in} = 1MHz)	—	82	—	—	82	—	—	82	—	dB
Slew Rate	—	±200	—	—	±200	—	—	±200	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 10V step)	150	190	230	150	190	230	150	190	230	ns
Overvoltage Recovery Time ⑤	—	400	500	—	400	500	—	400	500	ns
A/D Conversion Rate	2	—	—	2	—	—	2	—	—	MHz

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ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/°C
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	4	—	—	4	—	—	4	mA
Logic Loading "0"	—	—	4	—	—	4	—	—	4	mA
Delay, Falling Edge of $\overline{EOC}$ to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Offset Binary									
POWER REQUIREMENTS, ±15V										
Power Supply Range										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+15V Supply	—	+45	+55	—	+45	+55	—	+45	+55	mA
–15V Supply	—	–43	–50	—	–43	–50	—	–43	–50	mA
+5V Supply	—	+80	+90	—	+80	+90	—	+80	+90	mA
Power Dissipation	—	1.7	1.9	—	1.7	1.9	—	1.7	1.9	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V
POWER REQUIREMENTS, ±12V										
Power Supply Range										
+12V Supply	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	Volts
–12V Supply	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+12V Supply	—	+45	+55	—	+45	+55	—	+45	+55	mA
–12V Supply	—	–43	–50	—	–43	–50	—	–43	–50	mA
+5V Supply	—	+80	+90	—	+80	+90	—	+80	+90	mA
Power Dissipation	—	1.4	1.6	—	1.4	1.6	—	1.4	1.6	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V

Footnotes:

(1) All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time. There is a slight degradation in performance when using ±12V supplies.

(2) See Ordering Information for 0 to +10V input range. Contact DATEL for availability of other input voltage ranges.

(3) A 200ns wide start convert pulse is used for all production testing.

(4) Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

(5) This is the time required before the A/D output data is valid after the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-929 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies, as well as the REFERENCE OUTPUT (pin 21), to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-929 as possible.

2. The ADS-929 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. When operating the ADS-929 from ±12V supplies, do not drive external circuitry with the REFERENCE OUTPUT. The reference's accuracy and drift specifications may not be met, and loading the circuit may cause accuracy errors within the converter.

4. Applying a start convert pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") initiates a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

CALIBRATION PROCEDURE

(Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit of Figure 2 are guaranteed to compensate for the ADS-929's initial accuracy errors and may not be able to compensate for additional system errors.

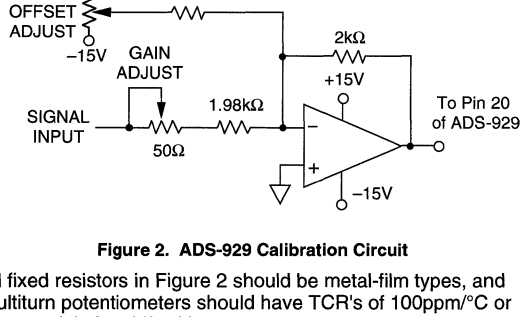

Figure 2. ADS-929 Calibration Circuit

All fixed resistors in Figure 2 should be metal-film types, and multiturn potentiometers should have TCR's of 100ppm/°C or less to minimize drift with temperature.

Table 1. Zero and Gain Adjust

INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±5V	+305µV	+4.999085V

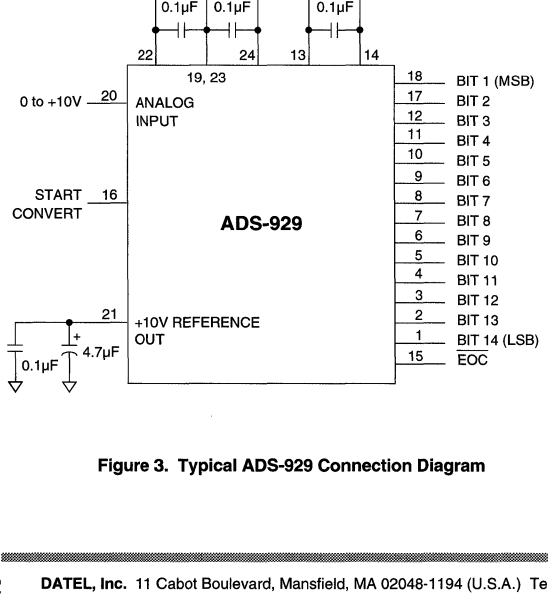

Figure 3. Typical ADS-929 Connection Diagram

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-929, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+305µV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+4.999085V) .

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +305µV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are a 1 and all 0's and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +4.999085V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until the output bits are all 1's and the LSB flickers between 1 and 0.

Table 2. Output Coding

OFFSET BINARY MSB LSB	INPUT RANGE ±5V	BIPOLAR SCALE
11 1111 1111 1111	+4.99939	+FS -1 LSB
11 1000 0000 0000	+3.75000	+3/4 FS
11 0000 0000 0000	+2.50000	+1/2 FS
10 0000 0000 0000	0.00000	0
01 0000 0000 0000	–2.50000	–1/2 FS
00 1000 0000 0000	–3.75000	–3/4 FS
00 0000 0000 0001	–4.99939	–FS +1 LSB
00 0000 0000 0000	–5.00000	–FS

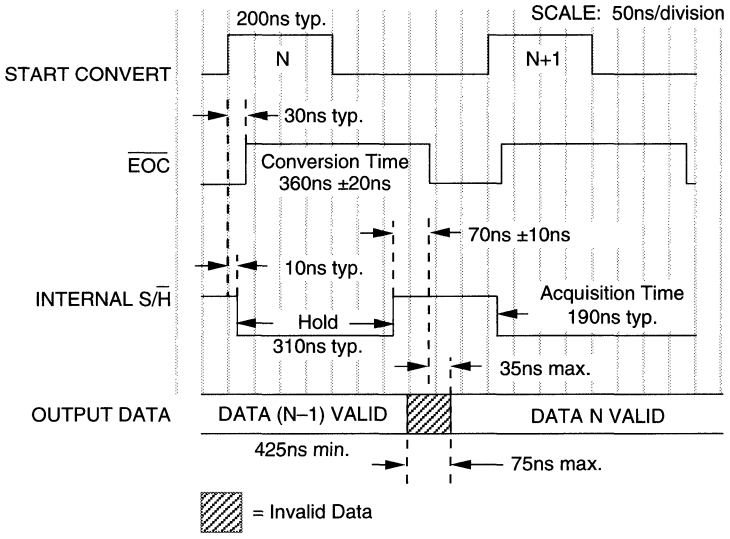

Figure 4. ADS-929 Timing Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

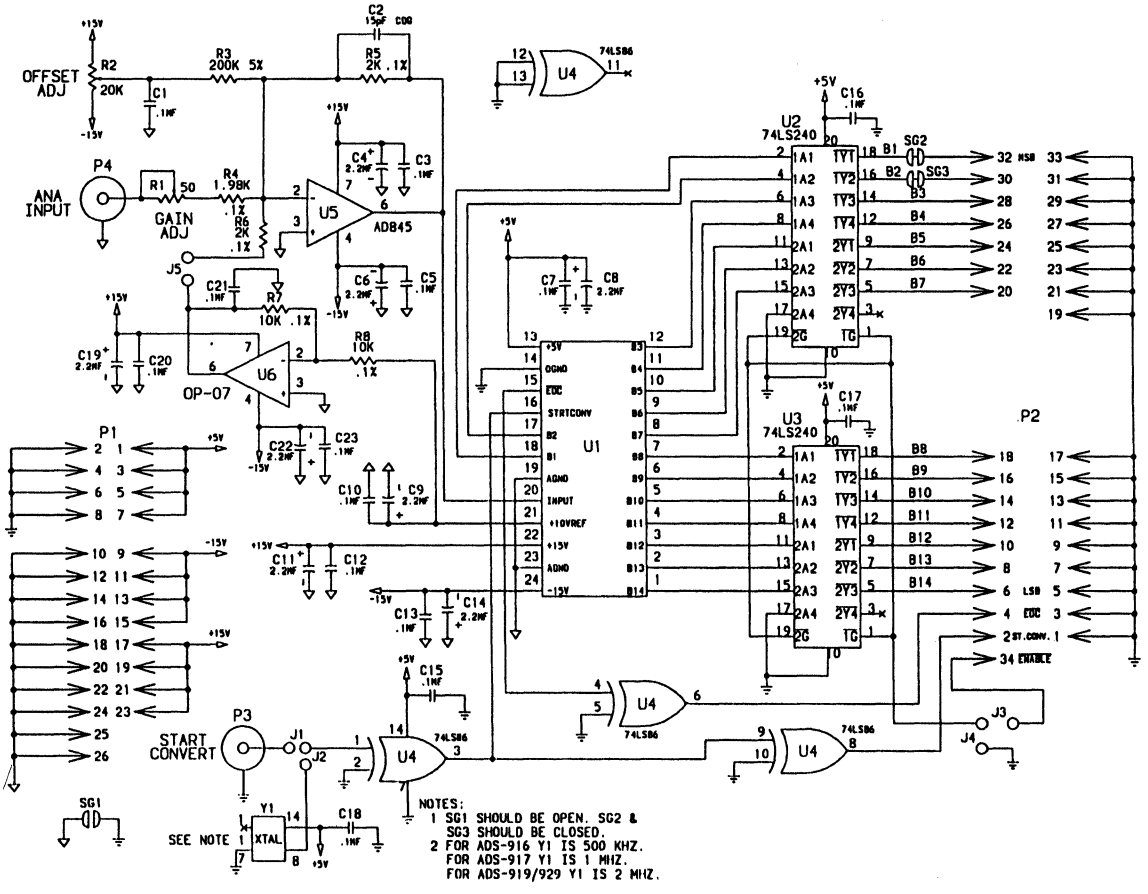

Figure 5. ADS-929 Evaluation Board Schematic

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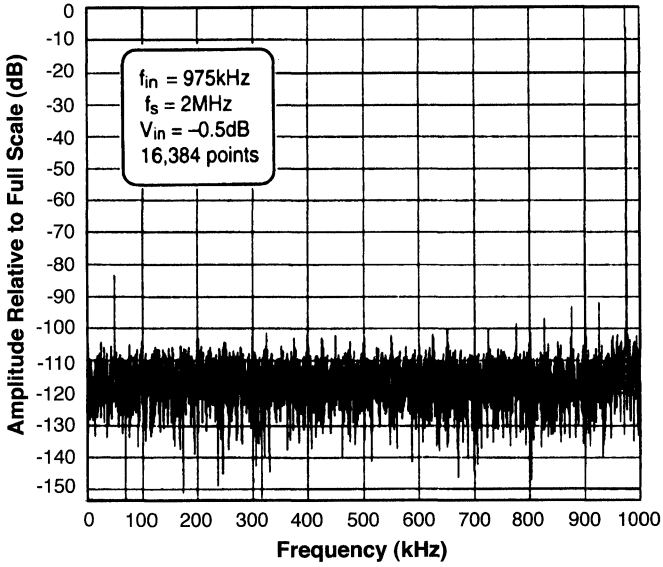


Figure 6. ADS-929 FFT Analysis

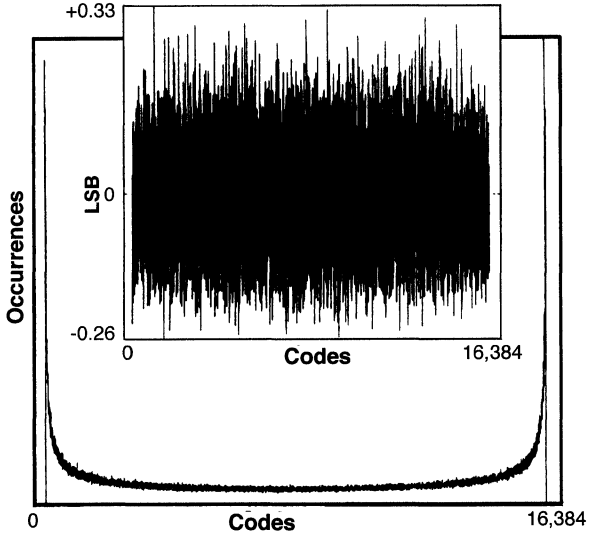
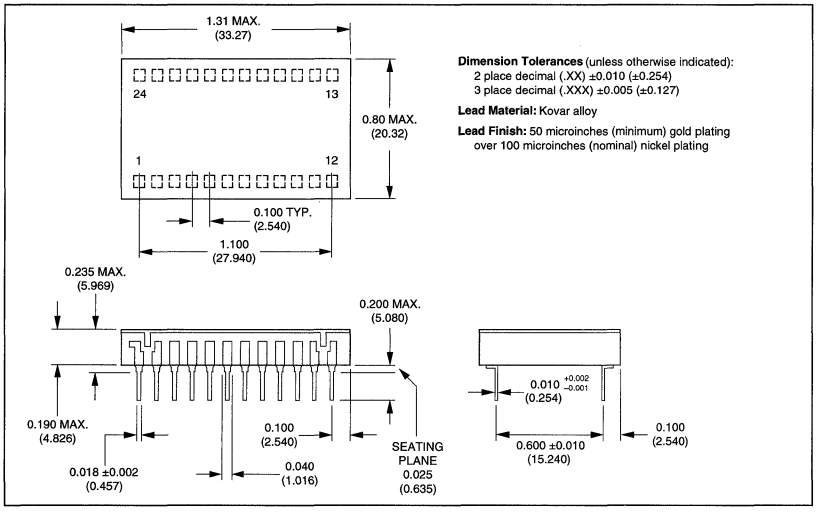


Figure 7. ADS-929 Histogram and Differential Nonlinearity

MECHANICAL DIMENSIONS
INCHES (mm)

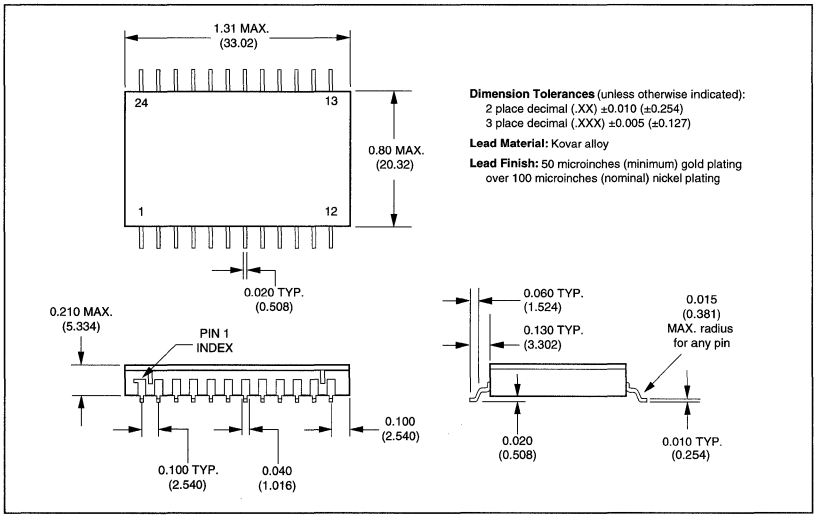
24-Pin DDIP Versions

ADS-929MC
ADS-929MM
ADS-929/883
ADS-919MC
ADS-919MM



24-Pin Surface Mount Versions

ADS-929GC
ADS-929GM
ADS-919GC
ADS-919GM



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-929MC	0 to +70°C	Bipolar (±5V)
ADS-929MM	–55 to +125°C	Bipolar (±5V)
ADS-929/883	–55 to +125°C	Bipolar (±5V)
ADS-929GC	0 to +70°C	Bipolar (±5V)
ADS-929GM	–55 to +125°C	Bipolar (±5V)
ADS-919MC	0 to +70°C	Unipolar (0 to +10V)*
ADS-919MM	–55 to +125°C	Unipolar (0 to +10V)*
ADS-919GC	0 to +70°C	Unipolar (0 to +10V)*
ADS-919GM	–55 to +125°C	Unipolar (0 to +10V)*

ACCESSORIES

ADS-B919/929	Evaluation Board (without ADS-929)
HS-24	Heat Sink for all ADS-919/929 DDIP models

Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.
For MIL-STD-883 product specification, contact DATEL.

*For more information, see ADS-919 data sheet.

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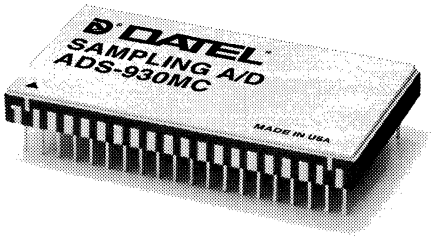
DATEL®
INNOVATION and EXCELLENCE

ADS-930
16-Bit, 500kHz Sampling A/D Converters

FEATURES

- **16-Bit resolution**
- **500kHz sampling rate**
- **Functionally complete**
- **Excellent dynamic performance**
- **83dB SNR, –89dB THD**
- **No missing codes**
- **Small 40-pin TDIP package**
- **3.5 Watts power dissipation**
- **On-board FIFO**



GENERAL DESCRIPTION

The low-cost ADS-930 is a high-performance, 16-bit, 500kHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. The dynamic performance of the ADS-930 is optimized to achieve a THD of –89dB and a SNR of 83dB.

Packaged in a small, 40-pin TDIP, the functionally complete ADS-930 contains a fast-settling sample/hold amplifier, a subranging (three-pass) A/D converter, an internal reference, on-board FIFO, timing and control logic, three-state outputs and error-correction circuitry. Digital inputs/outputs are TTL.

Requiring ±15V and +5V supplies, the ADS-930 typically dissipates 3.5 Watts. The unit is offered with a bipolar input range of ±5V or a unipolar input range of 0 to –10V. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges.

Typical applications include radar, sonar, medical/graphic imaging, and FFT spectrum analysis.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	40	$\overline{\text{BIT 1 (MSB)}}$
2	BIPOLAR	39	BIT 1 (MSB)
3	ANALOG INPUT	38	BIT 2
4	ANALOG GROUND	37	BIT 3
5	OFFSET ADJUST	36	BIT 4
6	GAIN ADJUST	35	BIT 5
7	+15V SUPPLY	34	BIT 6
8	$\overline{\text{COMP. BITS}}$	33	BIT 7
9	$\overline{\text{ENABLE}}$	32	BIT 8
10	FIFO READ	31	BIT 9
11	ANALOG GROUND	30	ANALOG GROUND
12	–15V SUPPLY	29	BIT 10
13	ANALOG GROUND	28	BIT 11
14	OVERFLOW	27	BIT 12
15	$\overline{\text{EOC}}$	26	BIT 13
16	+5V SUPPLY	25	BIT 14
17	START CONVERT	24	DIGITAL GROUND
18	DIGITAL GROUND	23	FIFO/$\overline{\text{DIR}}$
19	FSTAT1	22	BIT 15
20	FSTAT2	21	BIT 16 (LSB)

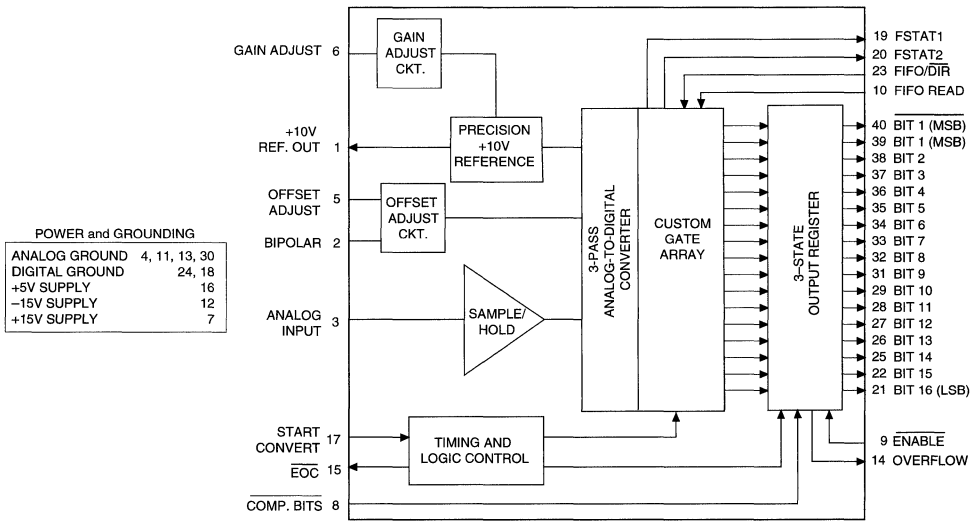


Figure 1. ADS-930 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 7)	0 to +16	Volts
–15V Supply (Pin 12)	0 to –16	Volts
+5V Supply (Pin 16)	0 to +6	Volts
Digital Inputs (Pins 8,9,10,17,23)	–0.3 to $+V_{DD}$ +0.3	Volts
Analog Input (Pin 3)		
Unipolar	–12.5 to +12.5	Volts
Bipolar	–7.5 to +12.5	Volts
Lead Temperature (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-930MC	0	—	+70	°C
ADS-930MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	4	—	°C/Watt
θca	—	18	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	40-pin, metal-sealed, ceramic TDIP			
Weight	0.56 ounces (16 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, 500kHz sampling rate, and a minimum 5 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Ranges										
Bipolar	—	±5	—	—	±5	—	—	±5	—	Volts
Unipolar	—	0 to –10	—	—	0 to –10	—	—	0 to –10	—	Volts
Input Resistance	1.4	1.5	1.7	1.4	1.5	1.7	1.4	1.5	1.7	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0" ②	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	175	200	215	175	200	215	175	200	215	ns
STATIC PERFORMANCE										
Resolution	—	16	—	—	16	—	—	16	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±1.0	—	—	±1.5	—	—	±2.0	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.75	—	—	±1.0	—	—	±1.5	—	LSB
Full Scale Absolute Accuracy	—	±0.05	±0.18	—	±0.2	±0.5	—	±0.5	±0.8	%FSR
Unipolar Zero Error (Tech Note 2)	—	±0.05	±0.085	—	±0.1	±0.25	—	±0.25	±0.5	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.05	±0.085	—	±0.15	±0.25	—	±0.25	±0.5	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.05	±0.15	—	±0.1	±0.25	—	±0.25	±0.5	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.15	—	±0.15	±0.35	—	±0.25	±0.65	%
No Missing Codes (f_{in} = 10kHz)	16	—	—	16	—	—	15	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–91	—	—	–91	—	—	–87	—	dB
100kHz to 250kHz	—	–86	—	—	–86	—	—	–84	—	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–89	–81	—	–89	–81	—	–85	–76	dB
100kHz to 250kHz	—	–84	—	—	–84	—	—	–82	—	dB
Signal-to-Noise Ratio (w/o distortion, –0.5dB)										
dc to 100kHz	81	83	—	81	83	—	75	80	—	dB
100kHz to 250kHz	—	80	—	—	80	—	—	79	—	dB
Signal-to-Noise Ratio ④ (& distortion, –0.5dB)										
dc to 100kHz	78	81	—	77	81	—	72	78	—	dB
100kHz to 250kHz	—	78	—	—	78	—	—	76	—	dB
Two-tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, f_s = 500kHz, –0.5dB)	—	–82	—	—	–82	—	—	–81	—	dB
Noise	—	150	—	—	150	—	—	150	—	µV/rms
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	2	—	—	2	—	—	2	—	MHz
Large Signal (–0.5dB input)	—	1.1	—	—	1.1	—	—	1.1	—	MHz
Feedthrough Rejection (f_{in} = 250kHz)	—	92	—	—	92	—	—	92	—	dB
Slew Rate	—	±80	—	—	±80	—	—	±80	—	V/µs
Aperture Delay Time	—	±10	—	—	±10	—	—	±10	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 10V step)	—	460	545	—	460	545	—	460	545	ns
Overvoltage Recovery Time	—	600	1000	—	600	1000	—	600	1000	ns
A/D Conversion Rate	500	—	—	500	—	—	500	—	—	kHz

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ANALOG OUTPUTS	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±10	—	—	±10	—	—	±10	—	ppm/°C
External Current	—	—	1	—	—	1	—	—	1	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Delay, Falling Edge of ENABLE to Output Data Valid	—	—	10	—	—	10	—	—	10	ns
Output Coding	Straight binary, offset binary, two's complement, complementary binary, complementary offset binary, C2C									
POWER REQUIREMENTS										
Power Supply Ranges										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.75	Volts
Power Supply Currents										
+15V Supply	—	+110	+130	—	+110	+130	—	+110	+130	mA
–15V Supply	—	–100	–125	—	–100	–125	—	–100	–125	mA
+5V Supply	—	+80	+90	—	+80	+90	—	+80	+90	mA
Power Dissipation	—	3.5	4.25	—	3.5	4.25	—	3.5	4.25	Watts
Power Supply Rejection	—	—	±0.02	—	—	±0.02	—	—	±0.02	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② When $\overline{\text{COMP. BITS}}$ (pin 8) is low, logic loading "0" will be –350µA.

③ A 200ns wide start convert pulse is used for all production testing. For applications requiring lower than 500kHz sampling rates, wider start convert pulses can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-930 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (4, 11, 13, 18, 24, and 30) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies and the +10V reference output to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-930 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. When using this circuitry, or any similar offset and gain calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain. Tie pins 5 and 6 to ANALOG GROUND (pin 4) if not using offset and gain adjust circuits.

3. Pin 8 ($\overline{\text{COMP. BITS}}$) is used to select the digital output coding format of the ADS-930. See Tables 3a and 3b. When this pin has a TTL logic "0" applied, it complements all of the ADS-930's digital outputs.

   When pin 8 has a logic "1" applied and the ADS-930 is operated within its unipolar 0 to –10V input range, the output coding is straight binary. Applying a logic "0" to pin 8 under these conditions changes the output coding to complementary binary.

   When pin 8 has a logic "1" applied and the ADS-930 is operated within its bipolar ±5V input range, the output coding is offset binary. Applying a logic "0" to pin 8 under these conditions changes the coding to complementary offset binary. Using the $\overline{\text{MSB}}$ output (pin 40) instead of the MSB output (pin 39) under these conditions changes the respective output codings to two's complement and complementary two's complement.

   Pin 8 is TTL-compatible and can be directly driven with digital logic in applications requiring dynamic control over its function. There is an internal pull-up resistor on pin 8 allowing it to be either connected to +5V or left open when a logic "1" is required.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

5. Applying a start convert pulse while a conversion is in progress ($\overline{\text{EOC}}$ = logic "1") will initiate a new and probably inaccurate conversion cycle.

6. Do not enable/disable or complement the output bits or read from the FIFO during the conversion process (from the falling edge of START CONVERT to the falling edge of $\overline{\text{EOC}}$).

INTERNAL FIFO OPERATION

The ADS-930 contains an internal, user-initiated, 18-bit, 16-word FIFO memory. Each word in the FIFO contains the 16 data bits as well as the MSB and overflow bits. Pins 23 (FIFO/$\overline{\text{DIR}}$) and 10 (FIFO READ) control the FIFO's operation. The FIFO's status can be monitored by reading pins 19 (FSTAT1) and 20 (FSTAT2).

When pin 23 (FIFO/$\overline{\text{DIR}}$) has a logic "1" applied, the FIFO is inserted into the digital data path. When pin 23 has a logic "0" applied, the FIFO is transparent, and the output data goes directly to the output three-state register (whose operation is controlled by pin 9 ($\overline{\text{ENABLE}}$)). Read and write commands to the FIFO are ignored when the ADS-930 is operated in the "direct" mode. It takes a maximum of 20ns to switch the FIFO in or out of the ADS-930's operation.

FIFO WRITE and READ Modes

Once the FIFO has been enabled (pin 23 high), digital data is automatically written to it, regardless of the status of FIFO READ (pin 10). Assuming the FIFO is initially empty, it will accept data (18-bit words) from the next 16 consecutive A/D conversions. As a precaution, pin 10 (which controls the FIFO's READ function) should not be low when data is first written to an empty FIFO.

When the FIFO is initially empty, digital data from the first conversion (the "oldest" data) appears at the output of the FIFO immediately after the first conversion has been completed and remains there until the FIFO is read.

If the output three-state register has been enabled (logic "0" applied to pin 9), data from the first conversion will appear at the output of the ADS-930. Attempting to write a 17th word to a full FIFO will result in that data, and any subsequent conversion data, being lost.

Once the FIFO is full (indicated by FSTAT1 and FSTAT2 both = "1"), it can be read by dropping the FIFO READ line (pin 10) to a logic "0" and then applying a series of 15 rising edges to the read line. Since the first data word is already present at the FIFO output, the first read command (the first rising edge applied to FIFO READ) will bring data from the second conversion to the output. Each subsequent read command/rising edge brings the next word to the output lines. If a read command is issued after the FIFO has been emptied, the last word (the 16th conversion) will remain present at the outputs.

FIFO Reset Feature

At any time, the FIFO can be reset to an empty state by putting the ADS-930 into its "direct" mode (logic "0" applied to pin 23, FIFO/$\overline{\text{DIR}}$) and also applying a logic "0" to the FIFO READ line (pin 10). The empty status of the FIFO will be indicated by FSTAT1 going to a "0" and FSTAT2 going to a "1". The status outputs will change 40ns after the control signals have been applied.

FIFO Status, FSTAT1 and FSTAT2

The status of the data in the FIFO can be monitored by reading the two status pins, FSTAT1 (pin 19) and FSTAT2 (pin 20).

CONTENTS	FSTAT1	FSTAT2
Empty (0 words)	0	1
<half full (≤7 words)	0	0
half-full or more (≥8 words)	1	0
Full (16 words)	1	1

Table 1. FIFO Delays

DELAY	PIN	TRANSITION	MIN.	TYP.	MAX.	UNITS
Direct mode to FIFO enabled	23	0→1	–	10	20	ns
FIFO enabled to direct mode	23	1→0	–	10	20	ns
FIFO READ to output data valid	10	0→1	–	–	40	ns
FIFO READ to status update when changing from <half full (1 word) to empty	10	1→0	–	–	28	ns
FIFO READ to status update when changing from ≥half full (8 words) to <half full (7 words)	10	0→1	–	–	110	ns
FIFO READ to status update when changing from full (16 words) to ≥half full (15 words)	10	0→1	–	–	190	ns
Falling edge of $\overline{\text{EOC}}$ to status update when writing first word into empty FIFO	15	1→0	–	–	190	ns
Falling edge of $\overline{\text{EOC}}$ to status update when changing FIFO from <half full (7 words) to ≥half full (8 words)	15	1→0	–	–	110	ns
Falling edge of $\overline{\text{EOC}}$ to status update when filling FIFO with 16th word	15	1→0	–	–	28	ns

CALIBRATION PROCEDURE

(Refer to Figure 2 and Tables 2, 3a, and 3b)

Connect the converter per Table 2 for the appropriate input voltage range. Any offset/gain calibration procedures should not be implemented until the device is fully warmed up. To avoid interaction, adjust offset before gain. The ranges of adjustment for the circuits in Figure 2 are guaranteed to compensate for the ADS-930's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This is accomplished by connecting LED's to the digital outputs and performing adjustments until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-930, offset adjusting is normally accomplished when the analog input is 0 minus 1/2LSB (–76µV). See Table 4a for the proper bipolar and unipolar output coding.

Gain adjusting is accomplished when the analog input is at nominal full scale minus 1 1/2LSB's (–9.999771V for unipolar and +4.999771V for bipolar).

Note: Connect pin 5 to ANALOG GROUND (pin 4) for operation without zero/offset adjustment. Connect pin 6 to pin 4 for operation without gain adjustment.

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 17) so that the converter is continuously converting.
2. For unipolar or bipolar zero/offset adjust, apply –76.3µV to the ANALOG INPUT (pin 3).
3. For a bipolar input — Adjust the offset potentiometer until the code flickers between 1000 0000 0000 0000 and 0111 1111 1111 1111 with pin 8 tied high (offset binary) or between 0111 1111 1111 1111 and 1000 0000 0000 0000 with pin 8 tied low (complementary offset binary).

   For a unipolar input — Adjust the offset potentiometer until all output bits are 0's and the LSB flickers between 0 and 1 with pin 8 tied high (straight binary) or until all output bits are 1's and the LSB flickers between 0 and 1 with pin 8 tied low (complementary binary).
4. Two's complement coding requires using $\overline{\text{BIT 1 (MSB)}}$ (pin 40). With pin 8 tied high, adjust the trimpot until the output code flickers between all 0's and all 1's.

Gain Adjust Procedure

1. Apply +4.999771V to the ANALOG INPUT (pin 3) for bipolar gain adjust or apply –9.999771V to pin 3 for unipolar gain adjust.
2. For a unipolar input — Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between a 1 and 0 with pin 8 tied high (straight binary) or until all output bits are 0's and the LSB flickers between a 1 and 0 with pin 8 tied low (complementary binary).

   For a bipolar input — Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between a 1 and 0 with pin 8 tied low (complementary offset binary) or until all output bits are 0's and the LSB flickers between a 1 and 0 with pin 8 tied high (offset binary).
3. Two's complement coding requires using pin 40. With pin 8 tied high, adjust the gain trimpot until the output code flickers equally between 1000 0000 0000 0000 and 1000 0000 0000 0001.
4. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 3a.

Table 2. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to –10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to +125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

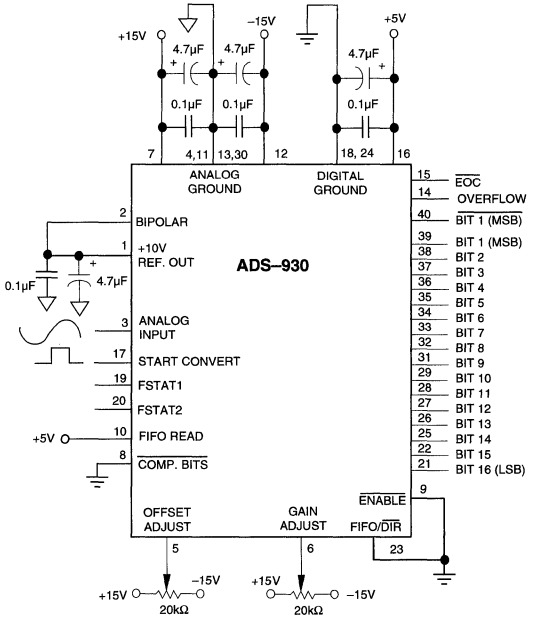


Figure 2. Bipolar Connection Diagram

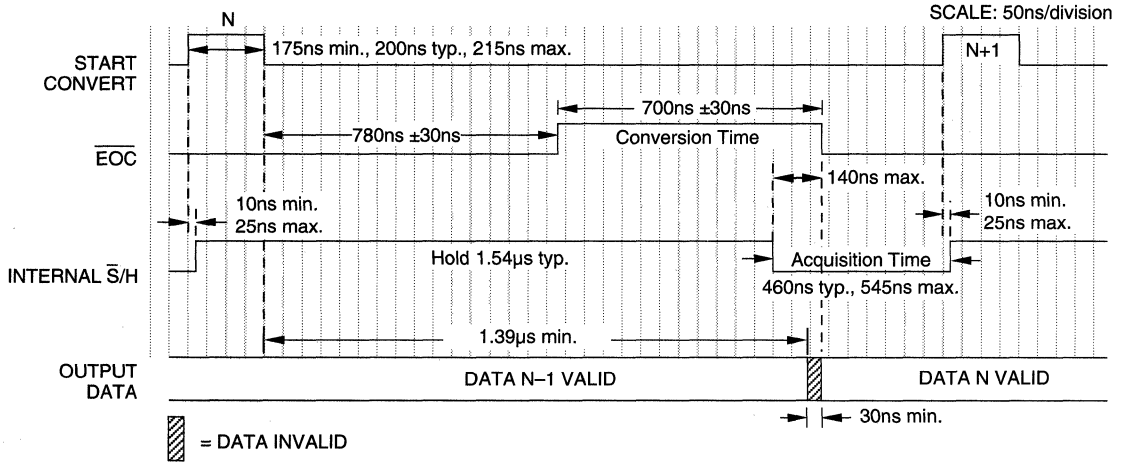


Figure 3. ADS-930 Timing Diagram

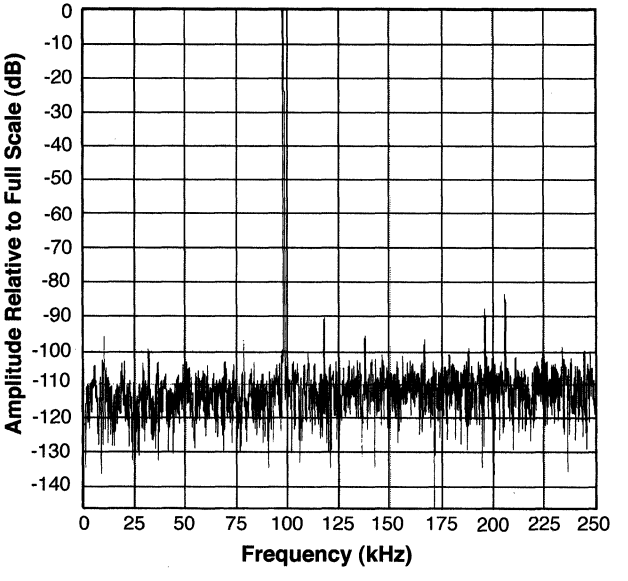


Figure 4. FFT Analysis of ADS-930
(f_S = 500kHz, f_{in} = 98kHz, V_{in} = –0.5dB, 4096-point FFT)

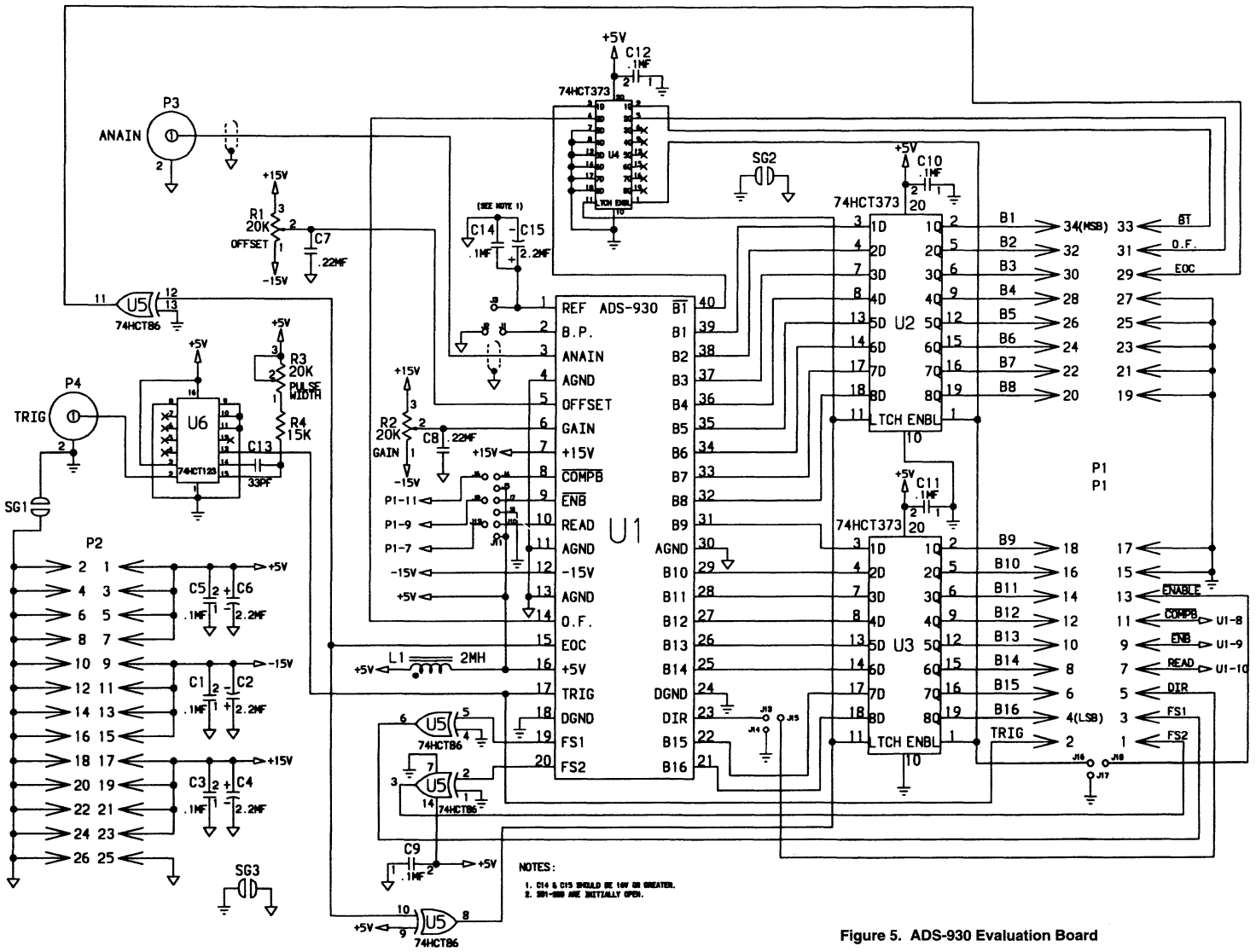


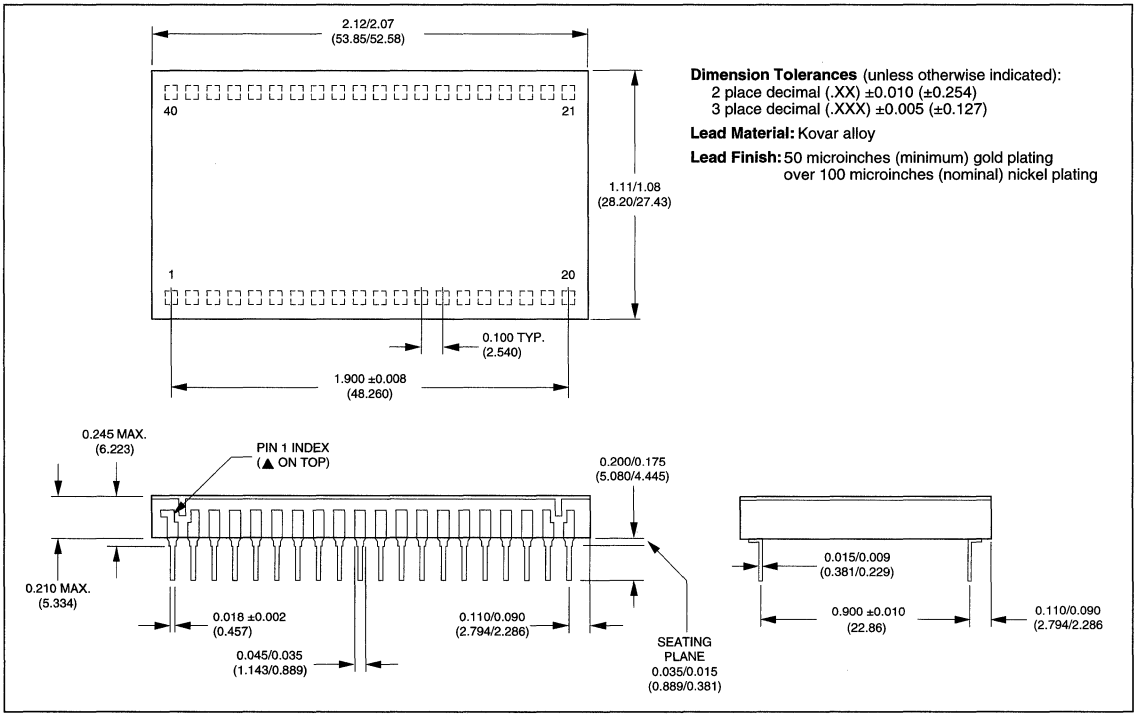
Figure 5. ADS-930 Evaluation Board

Table 3a. Output Coding

UNIPOLAR SCALE	INPUT RANGE 0 to –10V	STRAIGHT BIN. MSB	STRAIGHT BIN. LSB	COMP. BINARY MSB	COMP. BINARY LSB	COMP. OFF. BIN. MSB	COMP. OFF. BIN. LSB	INPUT RANGE ±5V	BIPOLAR SCALE
–FS +1 LSB	–9.999847	1111 1111 1111 1111		0000 0000 0000 0000		0111 1111 1111 1111		1000 0000 0000 0000	+4.999847	+FS –1 LSB
–FS +1 1/2 LSB	–9.999771	LSB "1" to "0"		LSB "0" to "1"		LSB "1" to "0"		LSB "0" to "1"	+4.999771	+FS –1 1/2 LSB
–7/8 FS	–8.750000	1110 0000 0000 0000		0001 1111 1111 1111		0110 0000 0000 0000		1001 1111 1111 1111	+3.750000	+3/4 FS
–3/4 FS	–7.500000	1100 0000 0000 0000		0011 1111 1111 1111		0100 0000 0000 0000		1011 1111 1111 1111	+2.500000	+1/2 FS
–1/2 FS	–5.000000	1000 0000 0000 0000		0111 1111 1111 1111		0000 0000 0000 0000		1111 1111 1111 1111	0.000000	0
–1/2 FS –1/2 LSB	–4.999924	0111 1111 1111 1111		1000 0000 0000 0000		1111 1111 1111 1111		0000 0000 0000 0000	–0.000076	–1/2 LSB
–1/4 FS	–2.500000	0100 0000 0000 0000		1011 1111 1111 1111		1100 0000 0000 0000		0011 1111 1111 1111	–2.500000	–1/2 FS
–1/8 FS	–1.250000	0010 0000 0000 0000		1101 1111 1111 1111		1010 0000 0000 0000		0101 1111 1111 1111	–3.750000	–3/4 FS
–1 LSB	–0.000153	0000 0000 0000 0001		1111 1111 1111 1110		1000 0000 0000 0001		0111 1111 1111 1110	–4.999847	–FS +1 LSB
– 1/2 LSB	–0.000076	LSB "0" to "1"		LSB "1" to "0"		LSB "0" to "1"		LSB "1" to "0"	–4.999924	–FS + 1/2 LSB
0	0.000000	0000 0000 0000 0000		1111 1111 1111 1111		1000 0000 0000 0000		0111 1111 1111 1111	–5.000000	–FS

OFFSET BINARY — COMP. TWO'S COMP. — TWO'S COMP.

MECHANICAL DIMENSIONS
INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	SPECIFIED TEMPERATURE RANGE
ADS-930MC	0 to +70°C
ADS-930MM	–55 to +125°C

ACCESSORIES

ADS-EVAL3	Evaluation Board (without ADS-930)
HS-40	Heat Sink

Receptacles for PC board mounting can be ordered through AMP Inc., Part #3-331272-8 (Component Lead Socket), 40 required. For availability of MIL-STD-883 product, contact DATEL.

Table 3b. Setting Coding Selection (Pin 8) for Desired Output

OUTPUT FORMAT	PIN 8 LOGIC LEVEL
Straight Binary	1
Complementary Binary	0
Offset Binary	1
Complementary Offset Binary	0
Two's Complement (Using $\overline{\text{MSB}}$, pin 40)	1
Complementary Two's Complement (Using $\overline{\text{MSB}}$, pin 40)	0

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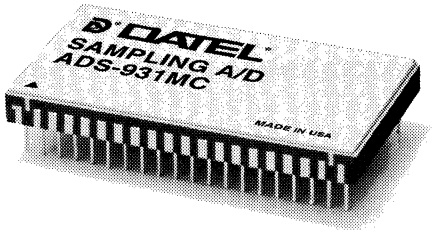
INNOVATION and EXCELLENCE

PRELIMINARY PRODUCT DATA

ADS-931
16-Bit, 1MHz Sampling A/D Converters

FEATURES

- **16-Bit resolution**
- **1MHz sampling rate**
- **Functionally complete**
- **No missing codes over full military temperature range**
- **Edge-triggered**
- **±5V supplies, 1.85 Watts**
- **Small, 40-pin, ceramic TDIP**
- **87dB SNR, –89dB THD**
- **Ideal for both time and frequency-domain applications**



GENERAL DESCRIPTION

The low-cost ADS-931 is a 16-bit, 1MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. The dynamic performance of the ADS-931 has been optimized to achieve a signal-to-noise ratio (SNR) of 87dB and a total harmonic distortion (THD) of –89dB.

Packaged in a 40-pin TDIP, the functionally complete ADS-931 contains a fast-settling sample-hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL. The ADS-931 only requires the rising edge of the start convert pulse to operate.

Requiring only ±5V supplies, the ADS-931 dissipates 1.85 Watts. The device is offered with a bipolar (±2.75V) analog input range. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. A proprietary, auto-calibrating, error-correcting circuit enables the device to achieve specified performance over the full military temperature range. Typical applications include medical imaging, radar, sonar, communications and instrumentation.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+3.2V REF. OUT	40	NO CONNECTION
2	ANALOG GROUND	39	NO CONNECTION
3	ANALOG INPUT	38	+5V ANALOG SUPPLY
4	ANALOG GROUND	37	–5V SUPPLY
5	OFFSET ADJUST	36	ANALOG GROUND
6	GAIN ADJUST	35	$\overline{\text{COMP. BITS}}$
7	DIGITAL GROUND	34	$\overline{\text{OUTPUT ENABLE}}$
8	FIFO/$\overline{\text{DIR}}$	33	OVERFLOW
9	FIFO READ	32	$\overline{\text{EOC}}$
10	FSTAT1	31	+5V DIGITAL SUPPLY
11	FSTAT2	30	DIGITAL GROUND
12	START CONVERT	29	$\overline{\text{BIT 1 (MSB)}}$
13	BIT 16 (LSB)	28	BIT 1 (MSB)
14	BIT 15	27	BIT 2
15	BIT 14	26	BIT 3
16	BIT 13	25	BIT 4
17	BIT 12	24	BIT 5
18	BIT 11	23	BIT 6
19	BIT 10	22	BIT 7
20	BIT 9	21	BIT 8

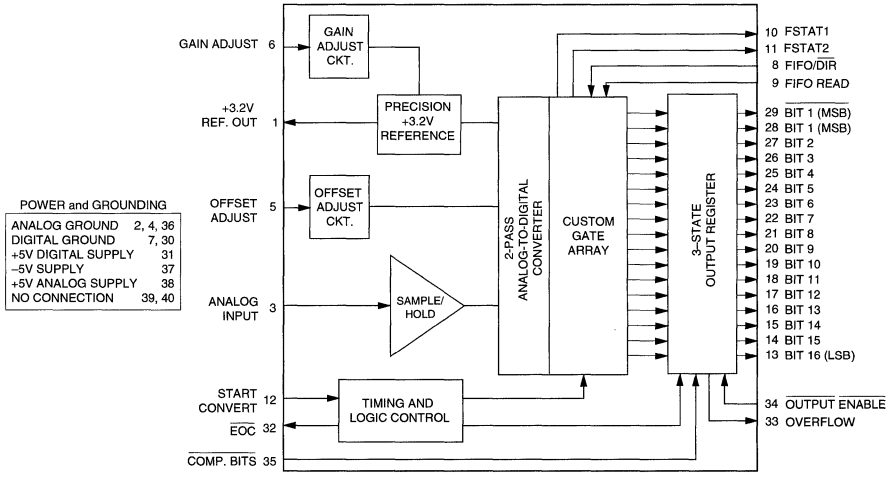


Figure 1. ADS-931 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Supply (Pins 31, 38)	0 to +6	Volts
–5V Supply (Pin 37)	0 to –6	Volts
Digital Inputs (Pins 8,9,12,34,35)	–0.3 to +V_{DD} +0.3	Volt
Analog Input (Pin 3)	±5	Volts
Lead Temperature (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–931MC	0	—	+70	°C
ADS–931MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	4	—	°C/Watt
θca	—	18	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	40-pin, metal-sealed, ceramic TDIP			
Weight	0.56 ounces (16 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±5V, +V_{DD} = +5V, 1MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range										
Bipolar	—	±2.75	—	—	±2.75	—	—	±2.75	—	Volts
Input Resistance	—	500	—	—	500	—	—	500	—	kΩ
Input Capacitance	—	10	15	—	10	15	—	10	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0" ②	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	500	—	—	500	—	—	500	—	ns
STATIC PERFORMANCE										
Resolution	—	16	—	—	16	—	—	16	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±1	—	—	±1.5	—	—	±2	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	–0.95	±0.75	+1.0	–0.95	±0.75	+1.0	–0.95	±0.75	+1.5	LSB
Full Scale Absolute Accuracy	—	±0.15	±0.3	—	±0.3	±0.5	—	±0.5	±0.8	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.4	—	±0.4	±0.6	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.4	—	±0.4	±0.6	%FSR
Gain Error (Tech Note 2)	—	±0.15	±0.3	—	±0.3	±0.5	—	±0.5	±0.8	%
No Missing Codes (f_{in} = 10kHz)	16	—	—	16	—	—	16	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–89	–83	—	–89	–83	—	–89	–79	dB
100kHz to 500kHz	—	–86	–80	—	–86	–80	—	–84	–78	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–89	–81	—	–89	–81	—	–85	–78	dB
100kHz to 500kHz	—	–84	–79	—	–84	–79	—	–82	–77	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)										
dc to 100kHz	82	87	—	82	87	—	80	84	—	dB
100kHz to 500kHz	81	85	—	81	85	—	79	82	—	dB
Signal–to–Noise Ratio ④ (& distortion, –0.5dB)										
dc to 100kHz	80	83	—	80	83	—	78	81	—	dB
100kHz to 500kHz	79	81	—	79	81	—	77	80	—	dB
Noise	—	60	—	—	60	—	—	60	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, f_s = 500kHz, –0.5dB)	—	–87	—	—	–87	—	—	–87	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	2.8	—	—	2.8	—	—	2.8	—	MHz
Large Signal (–0.5dB input)	—	2.3	—	—	2.3	—	—	2.3	—	MHz
Feedthrough Rejection (f_{in} = 500kHz)	—	90	—	—	90	—	—	90	—	dB
Slew Rate	—	±47	—	—	±47	—	—	±47	—	V/µs
Aperture Delay Time	—	–5	—	—	–5	—	—	–5	—	ns
Aperture Uncertainty	—	3	—	—	3	—	—	3	—	ps rms
S/H Acquisition Time (to ±0.001%FSR, 5.5V step)	650	700	750	650	700	750	650	700	750	ns
Overvoltage Recovery Time ⑤	—	500	1000	—	500	1000	—	500	1000	ns
A/D Conversion Rate	1	—	—	1	—	—	1	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	—	+3.2	—	—	+3.2	—	—	+3.2	—	Volts
Drift	—	±30	—	—	±30	—	—	±30	—	ppm/°C
External Current	—	5	—	—	5	—	—	5	—	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Output Coding	Complementary Offset Binary, Complementary Two's Complement, Offset Binary, Two's Complement									
POWER REQUIREMENTS										
Power Supply Range ⑥										
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.9	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	–4.9	–5.0	–5.25	Volts
Power Supply Current										
+5V Supply	—	+220	—	—	+220	—	—	+220	—	mA
–5V Supply	—	–150	—	—	–150	—	—	–150	—	mA
Power Dissipation	—	1.85	2.1	—	1.85	2.1	—	1.85	2.1	Watts
Power Supply Rejection	—	—	±0.07	—	—	±0.07	—	—	±0.07	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② When $\overline{\text{COMP. BITS}}$ (pin 35) is low, logic loading "0" will be –350µA.

③ A 500ns wide start convert pulse is used for all production testing. For applications requiring less than a 1MHz sampling rate, wider start convert pulses can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

⑥ The minimum supply voltages of +4.9V and –4.9V for $\pm V_{DD}$ are required for –55°C operation only. The minimum limits are +4.75V and –4.75V when operating at +125°C.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-931 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (2, 4, 7, 30 and 36) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies and the +3.2V reference output to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-931 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. When using this circuitry, or any similar offset and gain calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain. Tie pins 5 and 6 to ANALOG GROUND (pin 4) if not using offset and gain adjust circuits.

3. Pin 35 ($\overline{\text{COMP. BITS}}$) is used to select the digital output coding format of the ADS-931. See Tables 2a and 2b. When this pin has a TTL logic "0" applied, it complements all of the ADS-931's digital outputs.

   When pin 35 has a logic "1" applied, the output coding is complementary offset binary. Applying a logic "0" to pin 35 changes the coding to offset binary. Using the $\overline{\text{MSB}}$ output (pin 29) instead of the MSB output (pin 28) changes the respective output codings to complementary two's complement and two's complement.

   Pin 35 is TTL compatible and can be directly driven with digital logic in applications requiring dynamic control over its function. There is an internal pull-up resistor on pin 35 allowing it to be either connected to +5V or left open when a logic "1" is required.

4. To enable the three-state outputs, connect $\overline{\text{OUTPUT ENABLE}}$ (pin 34) to a logic "0" (low). To disable, connect pin 34 to a logic "1" (high).

5. Applying a start convert pulse while a conversion is in progress ($\overline{\text{EOC}}$ = logic "1") will initiate a new and probably inaccurate conversion cycle. Data from both the interrupted and subsequent conversions will be invalid.

6. Do not enable/disable or complement the output bits or read from the FIFO during the conversion process (from the rising edge of $\overline{\text{EOC}}$ to the falling edge of $\overline{\text{EOC}}$).

7. The OVERFLOW bit (pin 14) switches from 0 to 1 when the input voltage exceeds that which produces an output of all 1's or when the input equals or exceeds the voltage that produces all 0's. When $\overline{\text{COMP BITS}}$ is activated, the above conditions are reversed.

INTERNAL FIFO OPERATION

The ADS-931 contains an internal, user-initiated, 18-bit, 16-word FIFO memory. Each word in the FIFO contains the 16 data bits as well as the MSB and overflow bits. Pins 8 (FIFO/DIR) and 9 (FIFO READ) control the FIFO's operation. The FIFO's status can be monitored by reading pins 10 (FSTAT1) and 11 (FSTAT2).

When pin 8 (FIFO/DIR) has a logic "1" applied, the FIFO is inserted into the digital data path. When pin 8 has a logic "0" applied, the FIFO is transparent and the output data goes directly to the output three-state register (whose operation is controlled by pin 34 (ENABLE)). Read and write commands to the FIFO are ignored when the ADS-931 is operated in the "direct" mode. It takes a maximum of 20ns to switch the FIFO in or out of the ADS-931's operation.

FIFO WRITE and READ Modes

Once the FIFO has been enabled (pin 8 high), digital data is automatically written to it, regardless of the status of FIFO READ (pin 9). Assuming the FIFO is initially empty, it will accept data (18-bit words) from the next 16 consecutive A/D conversions. As a precaution, pin 9 (which controls the FIFO's READ function) should not be low when data is first written to an empty FIFO.

When the FIFO is initially empty, digital data from the first conversion (the "oldest" data) appears at the output of the FIFO immediately after the first conversion has been completed and remains there until the FIFO is read.

If the output three-state register has been enabled (logic "0" applied to pin 34), data from the first conversion will appear at the output of the ADS-931. Attempting to write a 17th word to a full FIFO will result in that data, and any subsequent conversion data, being lost.

Once the FIFO is full (indicated by FSTAT1 and FSTAT2 both = "1"), it can be read by dropping the FIFO READ line (pin 9) to a logic "0" and then applying a series of 15 rising edges to the read line. Since the first data word is already present at the FIFO output, the first read command (the first rising edge applied to FIFO READ) will bring data from the second conversion to the output. Each subsequent read command/rising edge brings the next word to the output lines. After the 15th rising edge brings the 16th data word to the FIFO output, the subsequent falling edge on READ will update the status outputs (after a 20ns maximum delay) to FAST1 = 0, FAST2 = 1 indicating that the FIFO is empty.

If a read command is issued after the FIFO empties, the last word (the 16th conversion) will remain present at the outputs.

FIFO Reset Feature

At any time, the FIFO can be reset to an empty state by putting the ADS-931 into its "direct" mode (logic "0" applied to pin 8, FIFO/DIR) and also applying a logic "0" to the FIFO READ line (pin 9). The empty status of the FIFO will be indicated by FSTAT1 going to a "0" and FSTAT2 going to a "1". The status outputs change 40ns after applying the control signals.

FIFO Status, FSTAT1 and FSTAT2

The status of the data in the FIFO can be monitored by reading the two status pins, FSTAT1 (pin 10) and FSTAT2 (pin 11).

CONTENTS	FSTAT1	FSTAT2
Empty (0 words)	0	1
<half full (<8 words)	0	0
half-full or more (≥8 words)	1	0
Full (16 words)	1	1

Table 1. FIFO Delays

DELAY	PIN	TRANSITION	MIN.	TYP.	MAX.	UNITS
Direct mode to FIFO enabled	8	0→1	–	10	20	ns
FIFO enabled to direct mode	8	1→0	–	10	20	ns
FIFO READ to output data valid	9	0→1	–	–	40	ns
FIFO READ to status update when changing from <half full (1 word) to empty	9	1→0	–	–	28	ns
FIFO READ to status update when changing from ≥half full (8 words) to <half full (7 words)	9	0→1	–	–	110	ns
FIFO READ to status update when changing from full (16 words) to ≥half full (15 words)	9	0→1	–	–	190	ns
Falling edge of $\overline{EOC}$ to status update when writing first word into empty FIFO	32	1→0	–	–	190	ns
Falling edge of $\overline{EOC}$ to status update when changing FIFO from <half full (7 words) to ≥half full (8 words)	32	1→0	–	–	110	ns
Falling edge of $\overline{EOC}$ to status update when filling FIFO with 16th word	32	1→0	–	–	28	ns

CALIBRATION PROCEDURE

(Refer to Figure 2 and Tables 2a, and 2b)

Connect the converter per Figure 2. Any offset/gain calibration procedures should not be implemented until the device is fully warmed up. To avoid interaction, adjust offset before gain. The ranges of adjustment for the circuit in Figure 2 are guaranteed to compensate for the ADS-931's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This is accomplished by connecting LED's to the digital outputs and performing adjustments until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-931, offset adjusting is normally accomplished when the analog input is 0 minus 1/2LSB (–42µV). See Table 2b for the proper bipolar output coding.

Gain adjusting is accomplished when the analog input is at nominal full scale minus 1 1/2LSB's (+2.749874V).

Note: Connect pin 5 to ANALOG GROUND (pin 4) for operation without zero/offset adjustment. Connect pin 6 to pin 4 for operation without gain adjustment.

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 12) so that the converter is continuously converting.
2. For zero/offset adjust, apply –42µV to the ANALOG INPUT (pin 3).
3. Adjust the offset potentiometer until the code flickers between 1000 0000 0000 0000 and 0111 1111 1111 1111 with pin 35 tied high (complementary offset binary) or between 0111 1111 1111 1111 and 1000 0000 0000 0000 with pin 35 tied low (offset binary).
4. Two's complement coding requires using $\overline{\text{BIT 1 (MSB)}}$ (pin 29). With pin 35 tied low, adjust the trimpot until the output code flickers between all 0's and all 1's.

Gain Adjust Procedure

1. For gain adjust, apply +2.749874V to the ANALOG INPUT (pin 3).
2. Adjust the gain potentiometer until all output bits are 0's and the LSB flickers between a 1 and 0 with pin 35 tied high (complementary offset binary) or until all output bits are 1's and the LSB flickers between a 1 and 0 with pin 35 tied low (offset binary).
3. Two's complement coding requires using $\overline{\text{BIT 1 (MSB)}}$, pin 29. With pin 35 tied low, adjust the gain trimpot until the output code flickers equally between 0111 1111 1111 1111 and 0111 1111 1111 1110.
4. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 2b

Table 2a. Setting Output Coding Selection (Pin 35)

OUTPUT FORMAT	PIN 35 LOGIC LEVEL
Complementary Offset Binary	1
Offset Binary	0
Complementary Two's Complement (Using $\overline{\text{MSB}}$, pin 29)	1
Two's Complement (Using $\overline{\text{MSB}}$, pin 29)	0

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

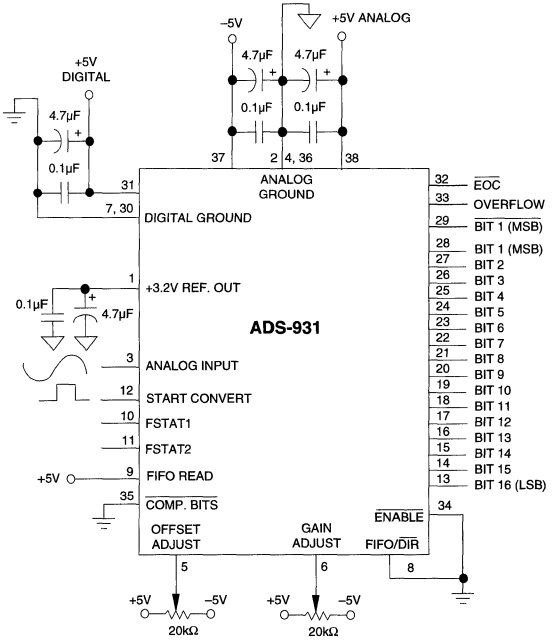
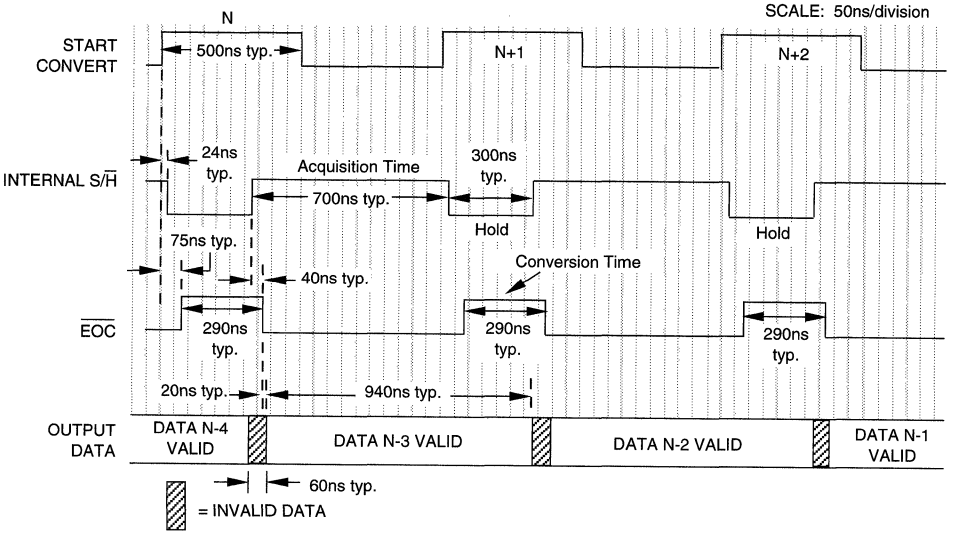


Figure 2. Connection Diagram



Notes:
1. This device has three pipeline delays. Four start convert pulses (clock cycles) must be applied for valid data from the first conversion to appear at the output of the A/D.
2. Scale is approximately 50ns per division.
3. fs = 1MHz

Figure 3. ADS-931 Timing Diagram

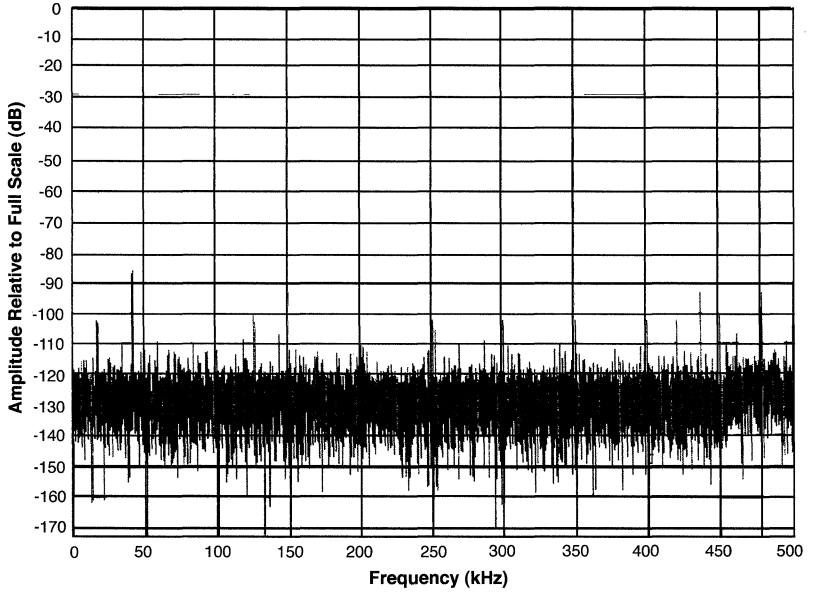


Figure 4. FFT Analysis of ADS-931
(f_S = 1MHz, f_{in} = 485kHz, V_{in} = –0.5dB, 32,768-point FFT)

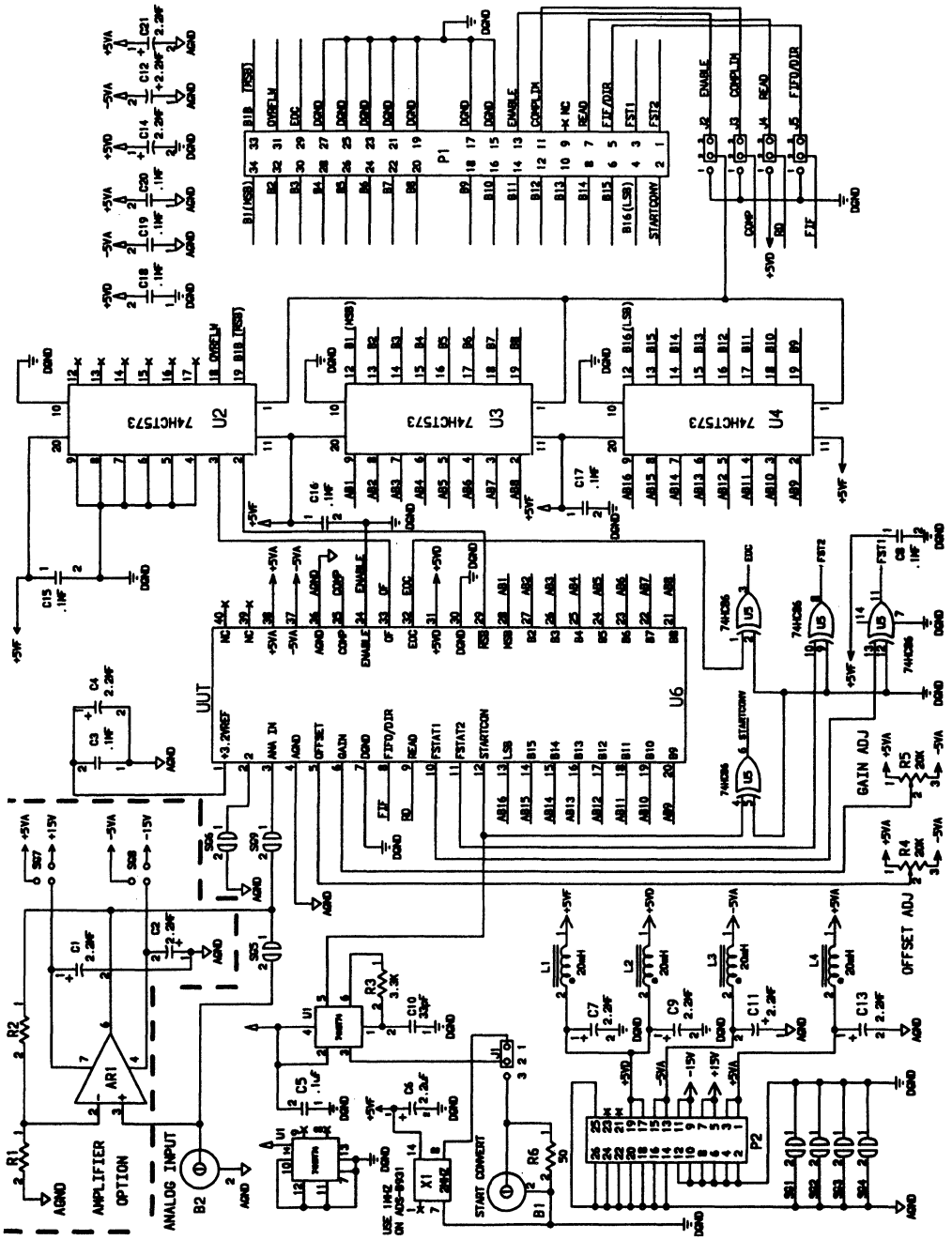


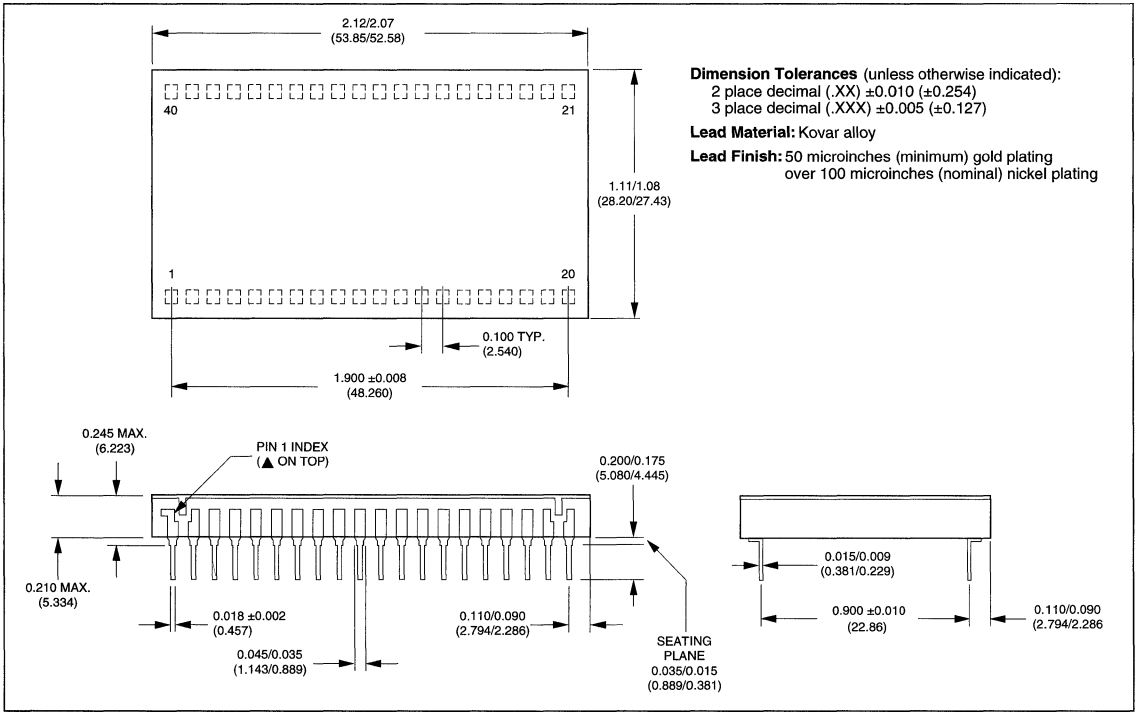
Figure 5. ADS-931 Evaluation Board

Table 2b. Output Coding

OUTPUT CODING				INPUT RANGE ±2.75V	BIPOLAR SCALE
MSB LSB	MSB LSB	$\overline{\text{MSB}}$ LSB	$\overline{\text{MSB}}$ LSB		
1111 1111 1111 1111	0000 0000 0000 0000	0111 1111 1111 1111	1000 0000 0000 0000	+2.749916	+FS –1 LSB
LSB "1" to "0"	LSB "0" to "1"	LSB "1" to "0"	LSB "0" to "1"	+2.749874	+FS –1 1/2 LSB
1110 0000 0000 0000	0001 1111 1111 1111	0110 0000 0000 0000	1001 1111 1111 1111	+2.062500	+3/4 FS
1100 0000 0000 0000	0011 1111 1111 1111	0100 0000 0000 0000	1011 1111 1111 1111	+1.375000	+1/2 FS
1000 0000 0000 0000	0111 1111 1111 1111	0000 0000 0000 0000	1111 1111 1111 1111	0.000000	0
0111 1111 1111 1111	1000 0000 0000 0000	1111 1111 1111 1111	0000 0000 0000 0000	–0.000084	–1 LSB
0100 0000 0000 0000	1011 1111 1111 1111	1100 0000 0000 0000	0011 1111 1111 1111	–1.375000	–1/2 FS
0010 0000 0000 0000	1101 1111 1111 1111	1010 0000 0000 0000	0101 1111 1111 1111	–2.062500	–3/4 FS
0000 0000 0000 0001	1111 1111 1111 1110	1000 0000 0000 0001	0111 1111 1111 1110	–2.749916	–FS +1 LSB
LSB "0" to "1"	LSB "1" to "0"	LSB "0" to "1"	LSB "1" to "0"	–2.749958	–FS + 1/2 LSB
0000 0000 0000 0000	1111 1111 1111 1111	1000 0000 0000 0000	0111 1111 1111 1111	–2.750000	–FS
OFFSET BINARY	COMP. OFF. BIN.	TWO'S COMP.	COMP. TWO'S COMP.		

MECHANICAL DIMENSIONS

INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	SPECIFIED TEMPERATURE RANGE
ADS-931MC	0 to +70°C
ADS-931MM	–55 to +125°C

ACCESSORIES

ADS-B931	Evaluation Board (without ADS-931)
HS-40	Heat Sink

Receptacles for PC board mounting can be ordered through AMP Inc., Part #3-331272-8 (Component Lead Socket), 40 required. For availability of MIL-STD-883 product, contact DATEL.

DATEL®
INNOVATION and EXCELLENCE

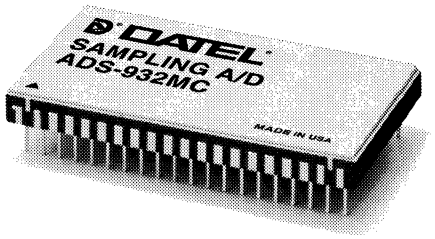
PRELIMINARY PRODUCT DATA

ADS-932
16-Bit, 2MHz Sampling A/D Converters

1

FEATURES

- **16-Bit resolution**
- **2MHz sampling rate**
- **Functionally complete**
- **No missing codes over full military temperature range**
- **Edge-triggered**
- **±5V supplies, 1.85 Watts**
- **Small, 40-pin, ceramic TDIP**
- **86dB SNR, –88dB THD**
- **Ideal for both time and frequency-domain applications**



GENERAL DESCRIPTION

The low-cost ADS-932 is a 16-bit, 2MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. The dynamic performance of the ADS-932 has been optimized to achieve a signal-to-noise ratio (SNR) of 86dB and a total harmonic distortion (THD) of –88dB.

Packaged in a 40-pin TDIP, the functionally complete ADS-932 contains a fast-settling sample/hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL. The ADS-932 only requires the rising edge of the start convert pulse to operate.

Requiring only ±5V supplies, the ADS-932 dissipates 1.85 Watts. The device is offered with a bipolar (±2.75V) analog input range. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. A proprietary, auto-calibrating, error-correcting circuit enables the device to achieve specified performance over the full military temperature range. Typical applications include medical imaging, radar, sonar, communications and instrumentation.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+3.2V REF. OUT	40	NO CONNECTION
2	ANALOG GROUND	39	NO CONNECTION
3	ANALOG INPUT	38	+5V ANALOG SUPPLY
4	ANALOG GROUND	37	–5V SUPPLY
5	OFFSET ADJUST	36	ANALOG GROUND
6	GAIN ADJUST	35	$\overline{\text{COMP. BITS}}$
7	DIGITAL GROUND	34	$\overline{\text{OUTPUT ENABLE}}$
8	FIFO/$\overline{\text{DIR}}$	33	OVERFLOW
9	FIFO READ	32	$\overline{\text{EOC}}$
10	FSTAT1	31	+5V DIGITAL SUPPLY
11	FSTAT2	30	DIGITAL GROUND
12	START CONVERT	29	$\overline{\text{BIT 1 (MSB)}}$
13	BIT 16 (LSB)	28	BIT 1 (MSB)
14	BIT 15	27	BIT 2
15	BIT 14	26	BIT 3
16	BIT 13	25	BIT 4
17	BIT 12	24	BIT 5
18	BIT 11	23	BIT 6
19	BIT 10	22	BIT 7
20	BIT 9	21	BIT 8

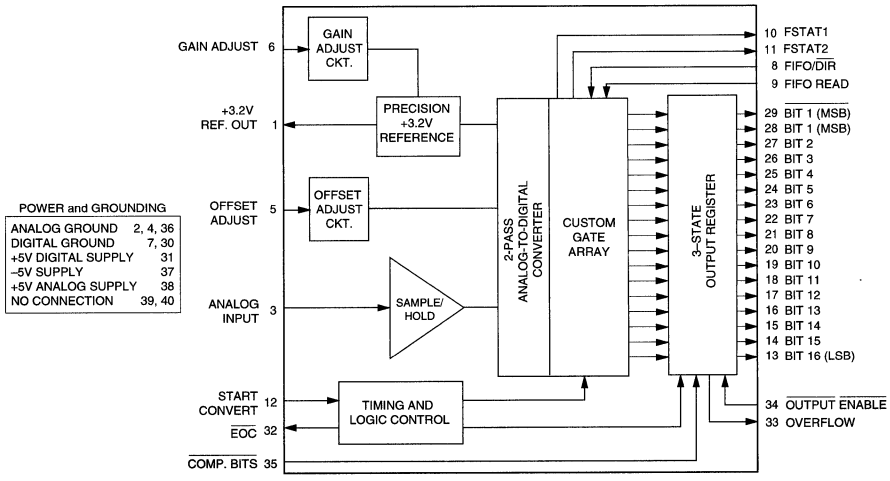


Figure 1. ADS-932 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Supply (Pins 31, 38)	0 to +6	Volts
–5V Supply (Pin 37)	0 to –6	Volts
Digital Inputs (Pins 8, 9, 12, 34, 35)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 3)	±5	Volts
Lead Temperature (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–932MC	0	—	+70	°C
ADS–932MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	4	—	°C/Watt
θca	—	18	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	40-pin, metal-sealed, ceramic TDIP			
Weight	0.56 ounces (16 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±5V, +V_{DD} = +5V, 2MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Voltage Range										
Bipolar	—	±2.75	—	—	±2.75	—	—	±2.75	—	Volts
Input Resistance	—	500	—	—	500	—	—	500	—	kΩ
Input Capacitance	—	10	15	—	10	15	—	10	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0" ②	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	250	—	—	250	—	—	250	—	ns
STATIC PERFORMANCE										
Resolution	—	16	—	—	16	—	—	16	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±1	—	—	±1.5	—	—	±2	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	–0.95	±0.75	+1.0	–0.95	±0.75	+1.0	–0.95	±0.75	+1.5	LSB
Full Scale Absolute Accuracy	—	±0.15	±0.3	—	±0.3	±0.5	—	±0.5	±0.8	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.4	—	±0.4	±0.6	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.4	—	±0.4	±0.6	%FSR
Gain Error (Tech Note 2)	—	±0.15	±0.3	—	±0.3	±0.5	—	±0.5	±0.8	%
No Missing Codes (f_{in} = 10kHz)	16	—	—	16	—	—	16	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 500kHz	—	–89	–81	—	–89	–81	—	–85	–79	dB
500kHz to 1MHz	—	–84	–78	—	–84	–78	—	–83	–77	dB
Total Harmonic Distortion (–0.5dB)										
dc to 500kHz	—	–88	–80	—	–88	–80	—	–84	–77	dB
500kHz to 1MHz	—	–83	–77	—	–83	–77	—	–82	–76	dB
Signal–to–Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 500kHz	81	86	—	81	86	—	80	83	—	dB
500kHz to 1MHz	80	85	—	80	85	—	78	81	—	dB
Signal–to–Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 500kHz	79	82	—	79	82	—	77	80	—	dB
500kHz to 1MHz	78	81	—	78	81	—	76	79	—	dB
Noise	—	70	—	—	70	—	—	70	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 200kHz, 240kHz, f_s = 2MHz, –0.5dB)	—	–87	—	—	–87	—	—	–87	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	4.5	—	—	4.5	—	—	4.5	—	MHz
Large Signal (–0.5dB input)	—	4	—	—	4	—	—	4	—	MHz
Feedthrough Rejection (f_{in} = 2MHz)	—	90	—	—	90	—	—	90	—	dB
Slew Rate	—	±75	—	—	±75	—	—	±75	—	V/µs
Aperture Delay Time	—	–5	—	—	–5	—	—	–5	—	ns
Aperture Uncertainty	—	3	—	—	3	—	—	3	—	ps rms
S/H Acquisition Time										
(to ±0.001%FSR, 5.5V step)	—	200	—	—	200	—	—	200	—	ns
Overvoltage Recovery Time ⑤	—	250	500	—	250	500	—	250	500	ns
A/D Conversion Rate	2	—	—	2	—	—	2	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	−55 to +125°C MIN.	−55 to +125°C TYP.	−55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	—	+3.2	—	—	+3.2	—	—	+3.2	—	Volts
Drift	—	±30	—	—	±30	—	—	±30	—	ppm/°C
External Current	—	5	—	—	5	—	—	5	—	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	−4	—	—	−4	—	—	−4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Output Coding	Complementary Offset Binary, Complementary Two's Complement, Offset Binary, Two's Complement									
POWER REQUIREMENTS										
Power Supply Range ⑥										
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.9	+5.0	+5.25	Volts
−5V Supply	−4.75	−5.0	−5.25	−4.75	−5.0	−5.25	−4.9	−5.0	−5.25	Volts
Power Supply Current										
+5V Supply	—	+220	—	—	+220	—	—	+220	—	mA
−5V Supply	—	−150	—	—	−150	—	—	−150	—	mA
Power Dissipation	—	1.85	2.1	—	1.85	2.1	—	1.85	2.1	Watts
Power Supply Rejection	—	—	±0.07	—	—	±0.07	—	—	±0.07	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② When $\overline{\text{COMP.BITS}}$ (pin 35) is low, logic loading "0" is −350µA.

③ A 250ns wide start convert pulse is used for all production testing. For applications requiring less than a 2MHz sampling rate, wider start convert pulses can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

⑥ The minimum supply voltages of +4.9V and −4.9V for $\pm V_{DD}$ are required for −55°C operation only. The minimum limits are +4.75V and −4.75V when operating at +125°C.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-932 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (2, 4, 7, 30 and 36) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies and the +3.2V reference output to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-932 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. When using this circuitry, or any similar offset and gain calibration hardware, make adjustments following warmup.

   To avoid interaction, always adjust offset before gain. Tie pins 5 and 6 to ANALOG GROUND (pin 4) if not using offset and gain adjust circuits.

3. Pin 35 ($\overline{\text{COMP. BITS}}$) is used to select the digital output coding format of the ADS-932. See Tables 2a and 2b. When this pin has a TTL logic "0" applied, it complements all of the ADS-932's digital outputs.

   When pin 35 has a logic "1" applied, the output coding is complementary offset binary. Applying a logic "0" to pin 35 changes the coding to offset binary. Using the $\overline{\text{MSB}}$ output (pin 29) instead of the MSB output (pin 28) changes the respective output codings to complementary two's complement and two's complement.

   Pin 35 is TTL compatible and can be directly driven with digital logic in applications requiring dynamic control over its function. There is an internal pull-up resistor on pin 35 allowing it to be either connected to +5V or left open when a logic "1" is required.

4. To enable the three-state outputs, connect $\overline{\text{OUTPUT ENABLE}}$ (pin 34) to a logic "0" (low). To disable, connect pin 34 to a logic "1" (high).

5. Applying a start convert pulse while a conversion is in progress ($\overline{\text{EOC}}$ = logic "1") will initiate a new and probably inaccurate conversion cycle. Data from both the interrupted and subsequent conversions will be invalid.

6. Do not enable/disable or complement the output bits or read from the FIFO during the conversion process (from the rising edge of $\overline{\text{EOC}}$ to the falling edge of $\overline{\text{EOC}}$).

7. The OVERFLOW bit (pin 14) switches from 0 to 1 when the input voltage exceeds that which produces an output of all 1's or when the input equals or exceeds the voltage that produces all 0's. When $\overline{\text{COMP BITS}}$ is activated, the above conditions are reversed.

INTERNAL FIFO OPERATION

The ADS-932 contains an internal, user-initiated, 18-bit, 16-word FIFO memory. Each word in the FIFO contains the 16 data bits as well as the MSB and overflow bits. Pins 8 (FIFO/$\overline{\text{DIR}}$) and 9 (FIFO READ) control the FIFO's operation. The FIFO's status can be monitored by reading pins 10 (FSTAT1) and 11 (FSTAT2).

When pin 8 (FIFO/$\overline{\text{DIR}}$) has a logic "1" applied, the FIFO is inserted into the digital data path. When pin 8 has a logic "0" applied, the FIFO is transparent and the output data goes directly to the output three-state register (whose operation is controlled by pin 34 ($\overline{\text{ENABLE}}$)). Read and write commands to the FIFO are ignored when the ADS-932 is operated in the "direct" mode. It takes a maximum of 20ns to switch the FIFO in or out of the ADS-932's operation.

FIFO WRITE and READ Modes

Once the FIFO has been enabled (pin 8 high), digital data is automatically written to it, regardless of the status of FIFO READ (pin 9). Assuming the FIFO is initially empty, it will accept data (18-bit words) from the next 16 consecutive A/D conversions. As a precaution, pin 9 (which controls the FIFO's READ function) should not be low when data is first written to an empty FIFO.

When the FIFO is initially empty, digital data from the first conversion (the "oldest" data) appears at the output of the FIFO immediately after the first conversion has been completed and remains there until the FIFO is read. If the output three-state register has been enabled (logic "0" applied to pin 34), data from the first conversion will appear at the output of the ADS-932. Attempting to write a 17th word to a full FIFO will result in that data, and any subsequent conversion data, being lost.

Once the FIFO is full (indicated by FSTAT1 and FSTAT2 both = "1"), it can be read by dropping the FIFO READ line (pin 9) to a logic "0" and then applying a series of 15 rising edges to the read line. Since the first data word is already present at the FIFO output, the first read command (the first rising edge applied to FIFO READ) will bring data from the second conversion to the output. Each subsequent read command/rising edge brings the next word to the output lines. After the 15th rising edge brings the 16th data word to the FIFO output, the subsequent falling edge on READ will update the status outputs (after a 20ns maximum delay) to FAST1 = 0, FAST2 = 1 indicating that the FIFO is empty.

If a read command is issued after the FIFO has been emptied, the last word (the 16th conversion) will remain present at the outputs.

FIFO Reset Feature

At any time, the FIFO can be reset to an empty state by putting the ADS-932 into its "direct" mode (logic "0" applied to pin 8, FIFO/$\overline{\text{DIR}}$) and also applying a logic "0" to the FIFO READ line (pin 9). The empty status of the FIFO will be indicated by FSTAT1 going to a "0" and FSTAT2 going to a "1". The status outputs will change 40ns after applying the control signals.

FIFO Status, FSTAT1 and FSTAT2

The status of the data in the FIFO can be monitored by reading the two status pins, FSTAT1 (pin 10) and FSTAT2 (pin 11).

CONTENTS	FSTAT1	FSTAT2
Empty (0 words)	0	1
<Half full (<8 words)	0	0
Half-full or more (≥8 words)	1	0
Full (16 words)	1	1

Table 1. FIFO Delays

DELAY	PIN	TRANSITION	MIN.	TYP.	MAX.	UNITS
Direct mode to FIFO enabled	8	0→1	–	10	20	ns
FIFO enabled to direct mode	8	1→0	–	10	20	ns
FIFO READ to output data valid	9	0→1	–	–	40	ns
FIFO READ to status update when changing from <half full (1 word) to empty	9	1→0	–	–	28	ns
FIFO READ to status update when changing from ≥half full (8 words) to <half full (7 words)	9	0→1	–	–	110	ns
FIFO READ to status update when changing from full (16 words) to ≥half full (15 words)	9	0→1	–	–	190	ns
Falling edge of $\overline{\text{EOC}}$ to status update when writing first word into empty FIFO	32	1→0	–	–	190	ns
Falling edge of $\overline{\text{EOC}}$ to status update when changing FIFO from <half full (7 words) to ≥half full (8 words)	32	1→0	–	–	110	ns
Falling edge of $\overline{\text{EOC}}$ to status update when filling FIFO with 16th word	32	1→0	–	–	28	ns

CALIBRATION PROCEDURE

(Refer to Figure 2 and Tables 2a, and 2b)

Connect the converter per Figure 2. Any offset/gain calibration procedures should not be implemented until the device is fully warmed up. To avoid interaction, adjust offset before gain. The ranges of adjustment for the circuit in Figure 2 are guaranteed to compensate for the ADS-932's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This is accomplished by connecting LED's to the digital outputs and performing adjustments until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-932, offset adjusting is normally accomplished when the analog input is 0 minus 1/2LSB (–42µV). See Table 2b for the proper bipolar output coding.

Gain adjusting is accomplished when the analog input is at nominal full scale minus 1 1/2LSB's (+2.749874V).

Note: Connect pin 5 to ANALOG GROUND (pin 4) for operation without zero/offset adjustment. Connect pin 6 to pin 4 for operation without gain adjustment.

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 12) so that the converter is continuously converting.
2. For zero/offset adjust, apply –42µV to the ANALOG INPUT (pin 3).
3. Adjust the offset potentiometer until the code flickers between 1000 0000 0000 0000 and 0111 1111 1111 1111 with pin 35 tied high (complementary offset binary) or between 0111 1111 1111 1111 and 1000 0000 0000 0000 with pin 35 tied low (offset binary).
4. Two's complement coding requires using $\overline{\text{BIT 1 (MSB)}}$ (pin 29). With pin 35 tied low, adjust the trimpot until the output code flickers between all 0's and all 1's.

Gain Adjust Procedure

1. For gain adjust, apply +2.749874V to the ANALOG INPUT (pin 3).
2. Adjust the gain potentiometer until all output bits are 0's and the LSB flickers between a 1 and 0 with pin 35 tied high (complementary offset binary) or until all output bits are 1's and the LSB flickers between a 1 and 0 with pin 35 tied low (offset binary).
3. Two's complement coding requires using $\overline{\text{BIT 1 (MSB)}}$, pin 29. With pin 35 tied low, adjust the gain trimpot until the output code flickers equally between 0111 1111 1111 1111 and 0111 1111 1111 1110.
4. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 2b.

Table 2a. Setting Output Coding Selection (Pin 35)

OUTPUT FORMAT	PIN 35 LOGIC LEVEL
Complementary Offset Binary	1
Offset Binary	0
Complementary Two's Complement (Using $\overline{\text{MSB}}$, pin 29)	1
Two's Complement (Using $\overline{\text{MSB}}$, pin 29)	0

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

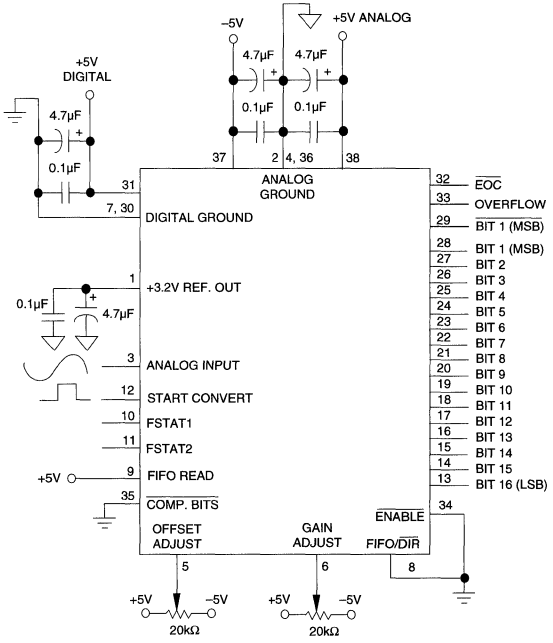
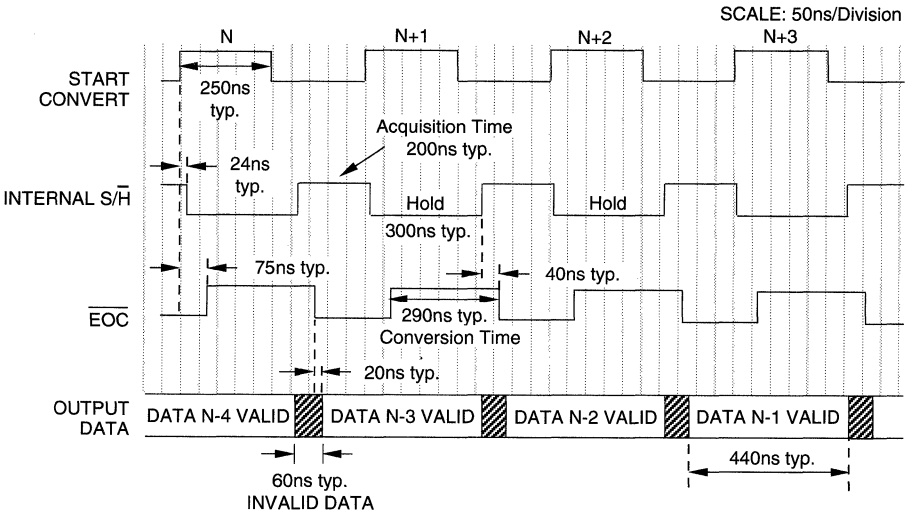


Figure 2. Connection Diagram



Notes:
1. This device has three pipeline delays. Four start convert pulses (clock cycles) must be applied for valid data from the first conversion to appear at the output of the A/D.
2. Scale is approximately 50ns per division.
3. f_S = 2MHz

Figure 3. ADS-932 Timing Diagram

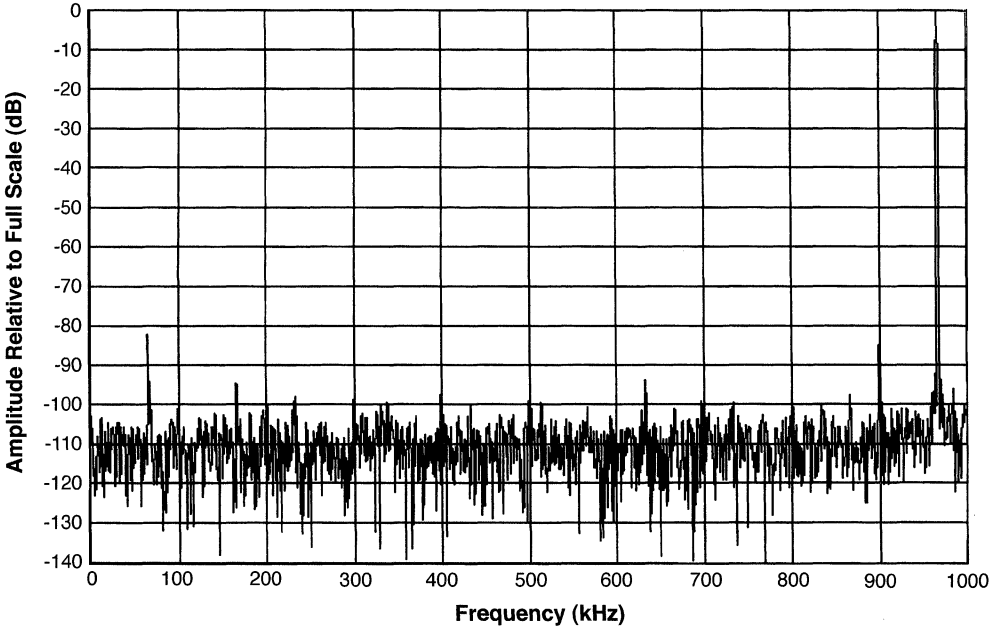


Figure 4. FFT Analysis of ADS-932
(f_S = 2MHz, f_{IN} = 975kHz, V_{IN} = –0.5dB, 32,768-point FFT)

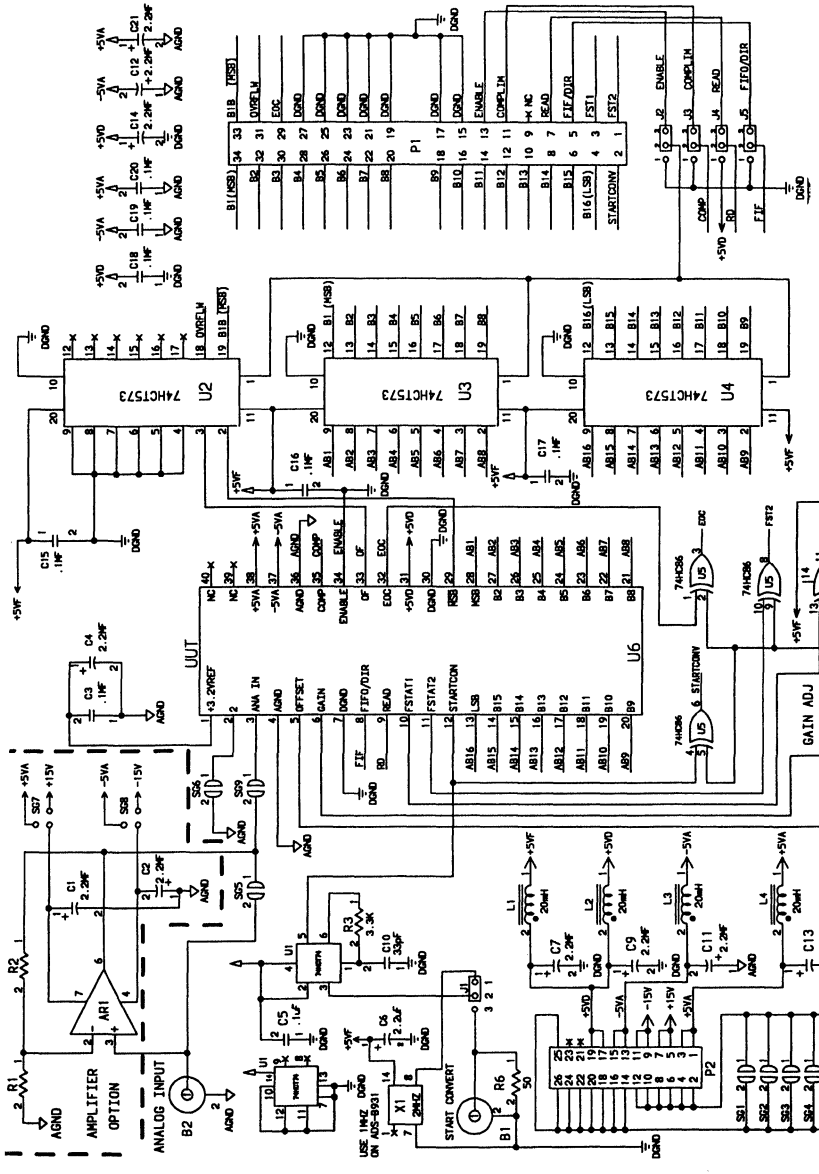
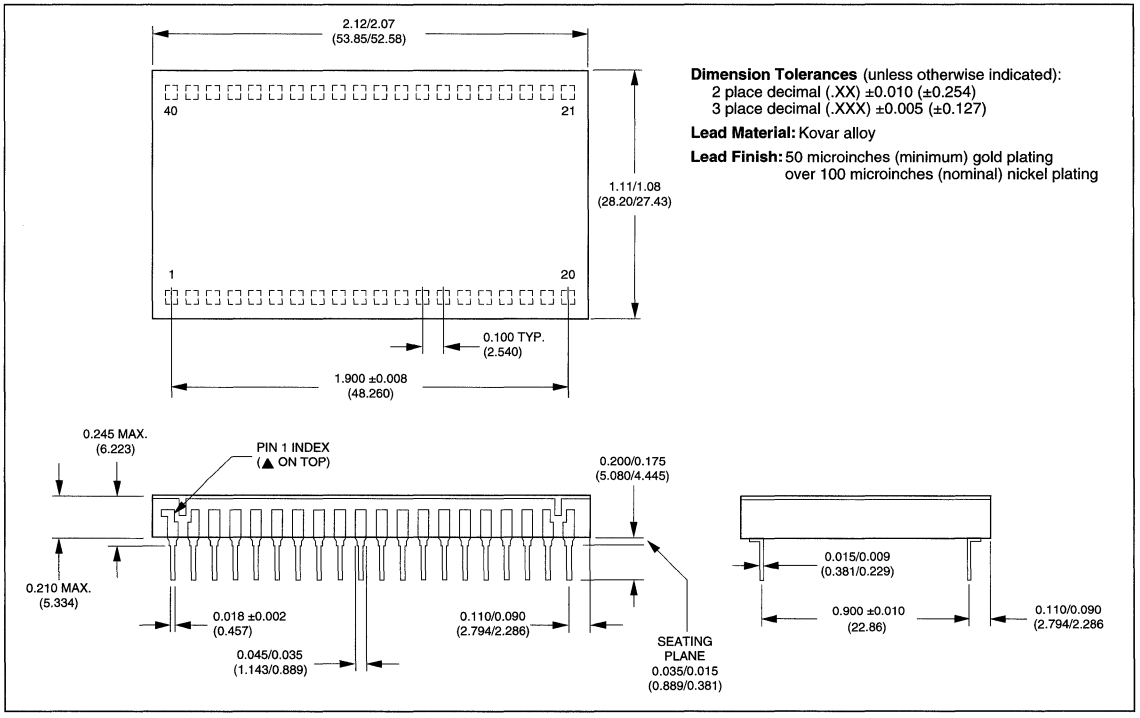


Figure 5. ADS-932 Evaluation Board

Table 2b. Output Coding

OUTPUT CODING				INPUT RANGE ±2.75V	BIPOLAR SCALE
MSB LSB	MSB LSB	$\overline{\text{MSB}}$ LSB	$\overline{\text{MSB}}$ LSB		
1111 1111 1111 1111	0000 0000 0000 0000	0111 1111 1111 1111	1000 0000 0000 0000	+2.749916	+FS –1 LSB
LSB "1" to "0"	LSB "0" to "1"	LSB "1" to "0"	LSB "0" to "1"	+2.749874	+FS –1 1/2 LSB
1110 0000 0000 0000	0001 1111 1111 1111	0110 0000 0000 0000	1001 1111 1111 1111	+2.062500	+3/4 FS
1100 0000 0000 0000	0011 1111 1111 1111	0100 0000 0000 0000	1011 1111 1111 1111	+1.375000	+1/2 FS
1000 0000 0000 0000	0111 1111 1111 1111	0000 0000 0000 0000	1111 1111 1111 1111	0.000000	0
0111 1111 1111 1111	1000 0000 0000 0000	1111 1111 1111 1111	0000 0000 0000 0000	–0.000084	–1 LSB
0100 0000 0000 0000	1011 1111 1111 1111	1100 0000 0000 0000	0011 1111 1111 1111	–1.375000	–1/2 FS
0010 0000 0000 0000	1101 1111 1111 1111	1010 0000 0000 0000	0101 1111 1111 1111	–2.062500	–3/4 FS
0000 0000 0000 0001	1111 1111 1111 1110	1000 0000 0000 0001	0111 1111 1111 1110	–2.749916	–FS +1 LSB
LSB "0" to "1"	LSB "1" to "0"	LSB "0" to "1"	LSB "1" to "0"	–2.749958	–FS + 1/2 LSB
0000 0000 0000 0000	1111 1111 1111 1111	1000 0000 0000 0000	0111 1111 1111 1111	–2.750000	–FS
OFFSET BINARY	COMP. OFF. BIN.	TWO'S COMP.	COMP. TWO'S COMP.		

MECHANICAL DIMENSIONS
INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	SPECIFIED TEMPERATURE RANGE
ADS-932MC	0 to +70°C
ADS-932MM	–55 to +125°C

ACCESSORIES

ADS-B932	Evaluation Board (without ADS-932)
HS-40	Heat Sink

Receptacles for PC board mounting can be ordered through AMP Inc., Part #3-331272-8 (Component Lead Socket), 40 required. For availability of MIL-STD-883 product, contact DATEL.

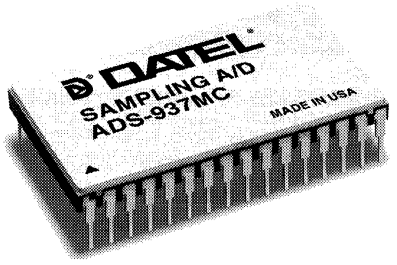
DATEL®
INNOVATION and EXCELLENCE

PRELIMINARY PRODUCT DATA

ADS-937
16-Bit, 1MHz, Low-Power Sampling A/D Converters

FEATURES

- **16-Bit resolution**
- **1MHz minimum sampling rate**
- **No missing codes over full military temperature range**
- **Very low power, 1.1 Watts**
- **Small, 32-pin, side-brazed, ceramic TDIP**
- **Edge-triggered**
- **Excellent performance**
- **Ideal for both time and frequency-domain applications**
- **Low cost**



GENERAL DESCRIPTION

The low-cost ADS-937 is a 16-bit, 1MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. This combined with excellent signal-to-noise ratio (SNR) and total harmonic distortion (THD) make the ADS-937 the ideal choice for both time-domain (medical imaging, scanners, process control) and frequency-domain (radar, telecommunications, spectrum analysis) applications.

Packaged in a 32-pin, side-brazed, ceramic TDIP, the functionally complete ADS-937 contains a fast-settling sample-hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL. The ADS-937 only requires the rising edge of the start convert pulse to operate.

Requiring ±15V and ±5V supplies, the ADS-937 typically dissipates 1.1 Watts. The device is offered with both bipolar (±5V) and unipolar (0 to –10V) analog input ranges. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges.

A proprietary, auto-calibrating, error-correcting circuit enables the device to achieve specified performance over the full military temperature range.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG INPUT	32	BIT 1 (MSB)
2	ANALOG GROUND	31	BIT 2
3	UNIPOLAR	30	BIT 3
4	OFFSET ADJUST	29	BIT 4
5	+5V REFERENCE OUT	28	BIT 5
6	GAIN ADJUST	27	BIT 6
7	COMPENSATION	26	BIT 7
8	–15V SUPPLY	25	BIT 8
9	+15V SUPPLY	24	BIT 9
10	+5V ANALOG SUPPLY	23	BIT 10
11	–5V ANALOG SUPPLY	22	BIT 11
12	ANALOG GROUND	21	BIT 12
13	DIGITIAL GROUND	20	BIT 13
14	+5V DIGITAL SUPPLY	19	BIT 14
15	$\overline{EOC}$	18	BIT 15
16	START CONVERT	17	BIT 16 (LSB)

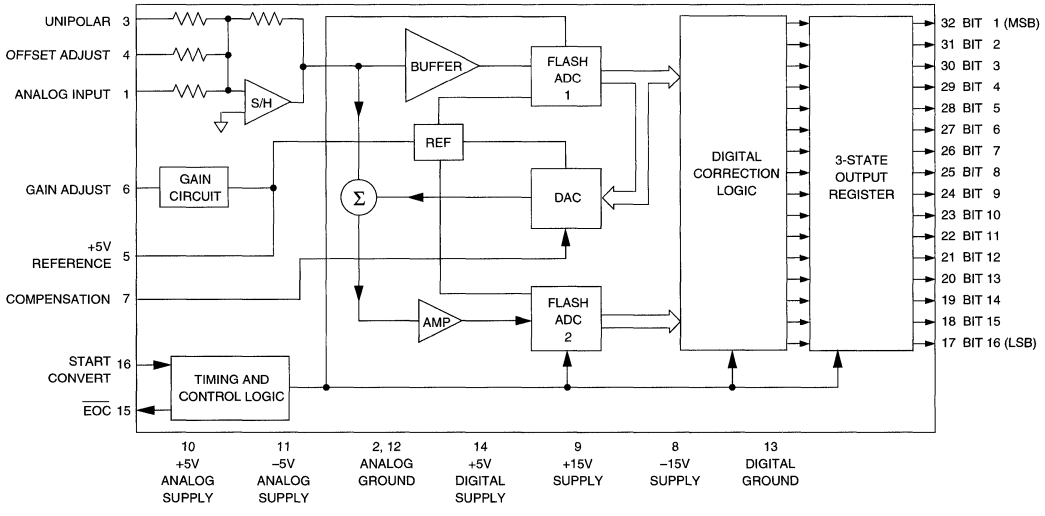


Figure 1. ADS-937 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 9)	0 to +16	Volts
–15V Supply (Pin 8)	0 to –16	Volts
+5V Supply (Pins 10, 14)	0 to +6	Volts
–5V Supply (Pin 11)	0 to –6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 1)	±15	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–937MC	0	—	+70	°C
ADS–937MM	–55	—	+125	°C
Thermal Impedance				
θ_{jc}	—	TBD	—	°C/Watt
θ_{ca}	—	TBD	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	32-pin, side-brazed, ceramic TDIP			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, ±V_{DD} = ±5V, 1MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges ②										
Bipolar	—	±5	—	—	±5	—	—	±5	—	Volts
Unipolar	—	0 to –10	—	—	0 to –10	—	—	0 to –10	—	Volts
Input Resistance	—	2.5	—	—	2.5	—	—	2.5	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2	—	—	+2	—	—	+2	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	500	—	—	500	—	—	500	—	ns
STATIC PERFORMANCE										
Resolution	—	16	—	—	16	—	—	16	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.75	—	—	±1.5	—	—	±2	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	–0.95	±0.5	+1	–0.95	±0.5	+1	–0.95	±0.75	+1.25	LSB
Full Scale Absolute Accuracy	—	±0.1	±0.25	—	±0.25	±0.4	—	±0.4	±0.8	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.1	±0.15	—	±0.15	±0.25	—	±0.25	±0.5	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.3	—	±0.3	±0.6	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.25	—	±0.25	±0.4	—	±0.4	±0.9	%
No Missing Codes (f_{in} = 10kHz)	16	—	—	16	—	—	16	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–87	–83	—	–87	–83	—	–84	–80	dB
100kHz to 500kHz	—	–84	–80	—	–84	–80	—	–81	–77	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–85	–81	—	–85	–81	—	–82	–78	dB
100kHz to 500kHz	—	–82	–77	—	–82	–77	—	–79	–74	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)										
dc to 100kHz	80	84	—	80	84	—	77	82	—	dB
100kHz to 500kHz	77	80	—	77	80	—	74	78	—	dB
Signal–to–Noise Ratio ④ (& distortion, –0.5dB)										
dc to 100kHz	78	82	—	78	82	—	75	79	—	dB
100kHz to 500kHz	75	79	—	75	79	—	72	76	—	dB
Two–tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, f_S =1MHz, –0.5dB)	—	–85	—	—	–84	—	—	–83	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	TBD	—	—	TBD	—	—	TBD	—	MHz
Large Signal (–0.5dB input)	—	TBD	—	—	TBD	—	—	TBD	—	MHz
Feedthrough Rejection (f_{in} = 500kHz)	—	84	—	—	84	—	—	84	—	dB
Slew Rate	—	±60	—	—	±60	—	—	±60	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 10V step)	—	300	—	—	300	—	—	300	—	ns
Overvoltage Recovery Time ⑤	—	500	1000	—	500	1000	—	500	1000	ns
A/D Conversion Rate	1	—	—	1	—	—	1	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+4.95	+5.0	+5.05	+4.95	+5.0	+5.05	+4.95	+5.0	+5.05	Volts
Drift	—	±30	—	—	±30	—	—	±30	—	ppm/°C
External Current	—	1	—	—	1	—	—	1	—	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Output Coding	Straight Binary, Offset Binary									
POWER REQUIREMENTS										
Power Supply Range										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	Volts
Power Supply Current										
+15V Supply	—	+15	—	—	+15	—	—	+15	—	mA
–15V Supply	—	–12	—	—	–12	—	—	–12	—	mA
+5V Supply	—	+152	—	—	+152	—	—	+152	—	mA
–5V Supply	—	–28	—	—	–28	—	—	–28	—	mA
Power Dissipation	—	1.1	1.25	—	1.1	1.25	—	1.1	1.25	Watts
Power Supply Rejection	—	—	±0.05	—	—	±0.05	—	—	±0.05	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② Contact DATEL for availability of other input voltage ranges.

③ A 500ns wide start convert pulse is used for all production testing. For applications requiring less than a 1MHz sampling rate, wider start convert pulses can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-937 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are not connected to each other internally. For optimal performance, tie all ground pins (2, 12 and 13) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies and the +5V reference output to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. Tie a 47µF capacitor between COMPENSATION (pin 7) and the –15V SUPPLY (pin 8).

2. The ADS-937 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. When using this circuitry, or any similar offset and gain calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain. Tie pins 4 and 6 to ANALOG GROUND (pin 2) if not using offset and gain adjust circuits

.3. Applying a start convert pulse while a conversion is in progress (EOC = logic "1") will initiate a new and probably inaccurate conversion cycle.

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

CALIBRATION PROCEDURE

(Refer to Figure 2 and Tables1 and 2)

Connect the converter per Table 1 for the appropriate input voltage range. Any offset/gain calibration procedures should not be implemented until the device is fully warmed up. To avoid interaction, adjust offset before gain. The ranges of adjustment for the circuit in Figure 2 are guaranteed to compensate for the ADS-937's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This is accomplished by connecting LED's to the digital outputs and performing adjustments until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-937, offset adjusting is normally accomplished when the analog input is 0 minus 1/2LSB (–76.3µV). See Table 2 for the proper bipolar and unipolar output coding.

Gain adjusting is accomplished when the analog input is at nominal full scale minus 1 1/2LSB's (–9.999771V for unipolar and –4.999771V for bipolar).

Note: Connect pin 4 to ANALOG GROUND (pin 2) for operation without zero/offset adjustment. Connect pin 6 to ANALOG GROUND (pin 2) for operation without gain adjustment.

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
±5V	Pin 1	Pins 2 and 3
0 to –10V	Pin 1	Pins 3 and 5

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so that the converter is continuously converting.
2. For unipolar or bipolar zero/offset adjust, apply –76.3µV to the ANALOG INPUT (pin 1).
3. For a bipolar input - Adjust the offset potentiometer until the code flickers between 1000 0000 0000 0000 and 0111 1111 1111 1111.

   For a unipolar input - Adjust the offset potentiometer until all output bits are 0's and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply –4.999771V to the ANALOG INPUT (pin 1) for bipolar gain adjust or apply –9.999771V to pin 1 for unipolar gain adjust.
2. For a unipolar input - Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.

   For a bipolar input - Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.
3. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 2.

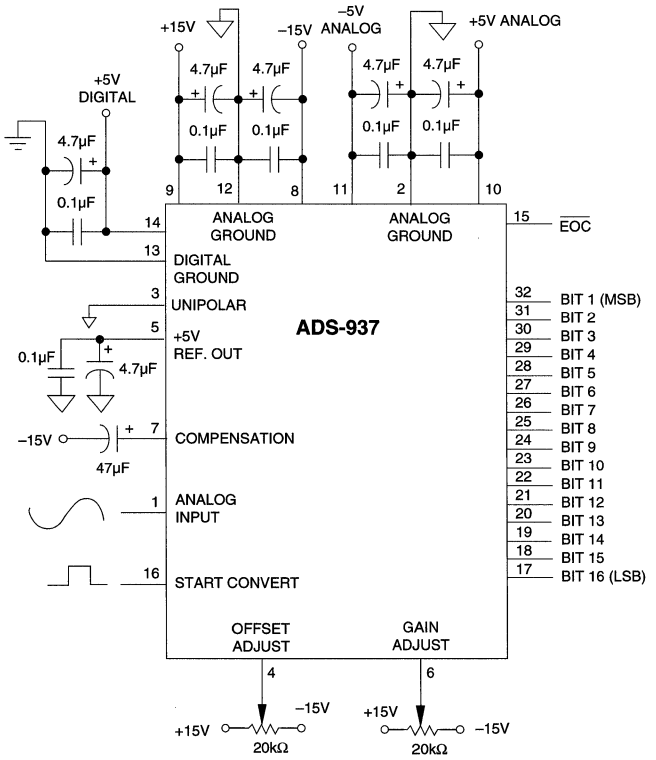


Figure 2. Bipolar Connection Diagram

Table 2. Output Coding

UNIPOLAR SCALE	INPUT RANGE 0 to –10V	OUTPUT CODING MSB LSB	OUTPUT CODING MSB LSB	INPUT RANGE ±5V	BIPOLAR SCALE
		STRAIGHT BIN.			
–FS +1LSB	–9.999847	1111111111111111	0000000000000000	+4.999847	+FS –1LSB
–7/8 FS	–8.750000	1110000000000000	0001111111111111	+3.750000	+3/4 FS
–3/4 FS	–7.500000	1100000000000000	0011111111111111	+2.500000	+1/2 FS
–1/2 FS	–5.000000	1000000000000000	0111111111111111	0.000000	0
–1/4 FS	–2.500000	0100000000000000	1011111111111111	–2.500000	–1/2 FS
–1/8 FS	–1.250000	0010000000000000	1101111111111111	–3.750000	–3/4 FS
–1 LSB	–0.000153	0000000000000001	1111111111111110	–4.999847	–FS +1 LSB
0	0.000000	0000000000000000	1111111111111111	–5.000000	–FS
			OFFSET BIN.		

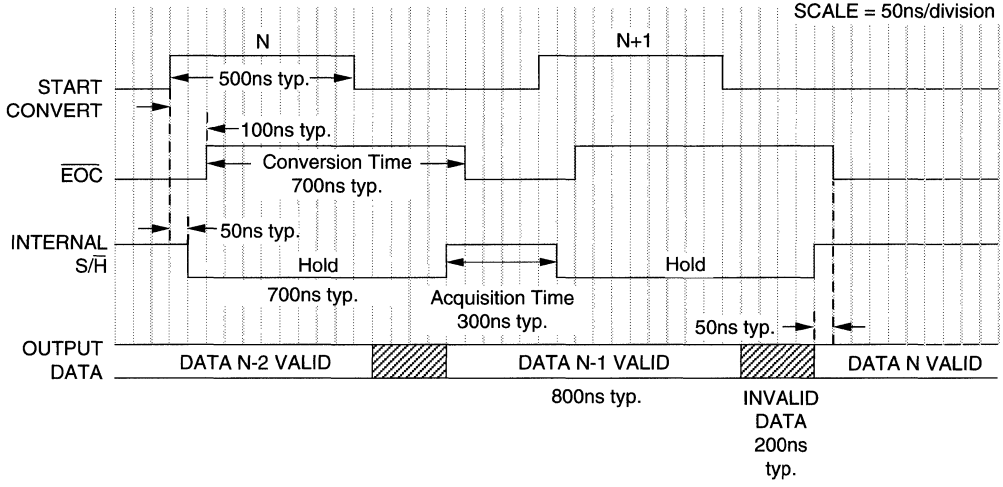
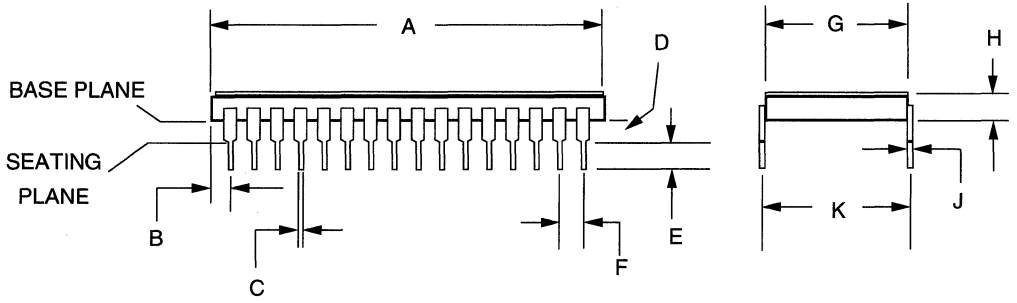


Figure 3. Timing Diagram

MECHANICAL DIMENSIONS



DIM.	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A	1.584	1.616	40.23	41.05
B	0.030	0.070	0.762	1.778
C	0.016	0.020	0.406	0.508
D	0.040	0.060	1.016	1.524
E	0.150	0.200	3.81	5.08
F	0.100, ±0.002		2.54, ±0.0508	
G	0.900	0.920	22.86	23.37
H	0.150, ±0.020		3.81, ±0.508	
J	0.009	0.012	0.229	0.305
K	0.900	0.932	22.86	23.67
Pins	32		32	

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-937MC	0 to +70°C
ADS-937MM	–55 to +125°C

ACCESSORIES

ADS-B937	Evaluation Board (without ADS-937)

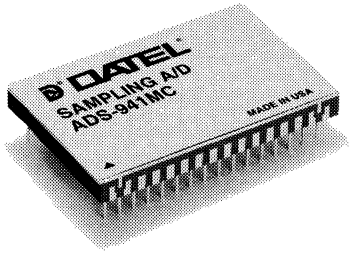
Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

DATEL®
INNOVATION and EXCELLENCE

ADS-941
14-Bit, 1MHz Sampling A/D Converters

FEATURES

- **14-Bit resolution**
- **1MHz minimum sampling rate**
- **Functionally complete**
- **Internal reference and sample/hold**
- **No missing codes**
- **Excellent performance**
- **Full Nyquist-rate sampling**
- **Small 32-pin DIP**
- **Low power, 2.8 Watts**



GENERAL DESCRIPTION

DATEL's ADS-941 is a functionally complete, 14-bit, 1MHz, sampling A/D converter. Its standard, 32-pin, triple-wide ceramic DIP contains a fast-settling sample/hold amplifier, a 14-bit subranging (two-pass) A/D converter, a precision reference, a three-state output register, and all the timing and control logic necessary to operate from a single start convert pulse.

The ADS-941 is optimized for wideband frequency-domain applications and is fully FFT tested. Total harmonic distortion (THD) and signal-to-noise ratio (including distortion) typically run at -85dB and 80dB, respectively, with full-scale inputs up to 100kHz.

The ADS-941 requires ±15V and +5V supplies and typically consumes 2.8 Watts.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	32	START CONVERT
2	BIPOLAR	31	BIT 1 OUT (MSB)
3	ANALOG INPUT	30	BIT 1 OUT (MSB)
4	SIGNAL GROUND	29	BIT 2 OUT
5	OFFSET ADJUST	28	BIT 3 OUT
6	ANALOG GROUND	27	BIT 4 OUT
7	OVERFLOW	26	BIT 5 OUT
8	CODING SELECT	25	BIT 6 OUT
9	ENABLE	24	BIT 7 OUT
10	+5V SUPPLY	23	BIT 8 OUT
11	DIGITAL GROUND	22	BIT 9 OUT
12	+15V SUPPLY	21	BIT 10 OUT
13	-15V SUPPLY	20	BIT 11 OUT
14	ANALOG GROUND	19	BIT 12 OUT
15	ANALOG GROUND	18	BIT 13 OUT
16	EOC	17	BIT 14 OUT (LSB)

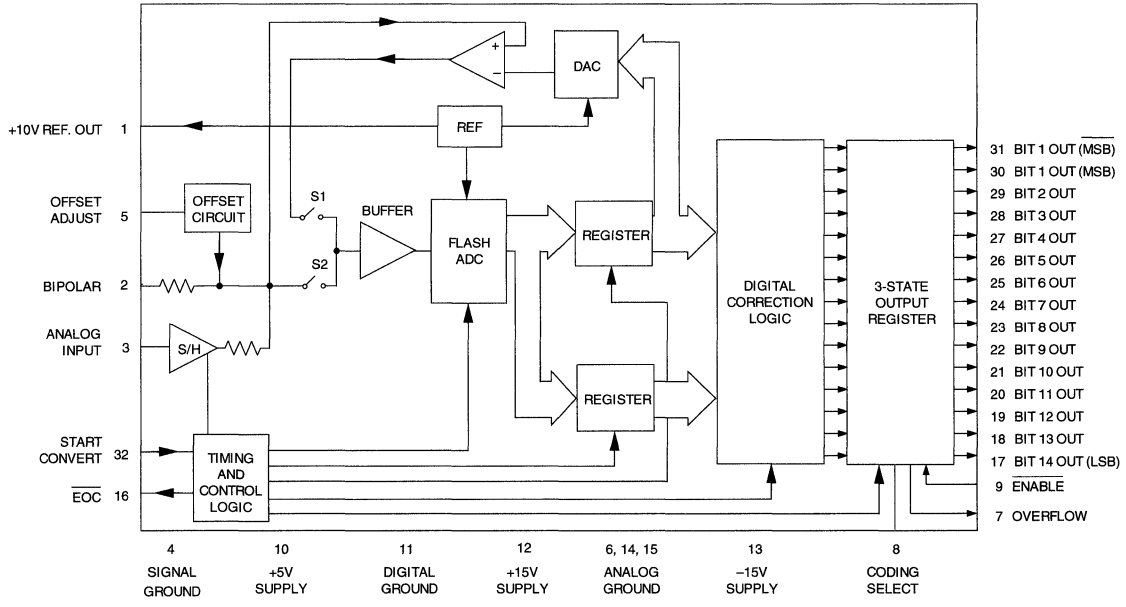


Figure 1. ADS-941 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	0 to +16	Volts
–15V Supply (Pin 13)	0 to –16	Volts
+5V Supply (Pin 10)	0 to +6.0	Volts
Digital Inputs (Pins 8, 9, 32)	–0.3 toV_{DD} +0.3	Volts
Analog Input (Pin 3)	±15	Volts
Lead Temp. (10 seconds)	300	°C

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V, 1MHz sampling rate, and a minimum 7 minute warmup unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
Unipolar	—	0 to +10	—	Volts
Bipolar	—	±5	—	Volts
Input Impedance	2.2	2.5	—	kΩ
Input Capacitance	—	7	15	pF
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Loading "1"	—	—	+10	µA
Logic Loading "0"	—	—	–600	µA
PERFORMANCE				
Integral Nonlinearity (f_{in} = 10kHz)				
+25°C	—	±1	±2	LSB
0 to +70°C	—	±1.5	±2	LSB
–40 to +85°C	—	±2	±3	LSB
Differential Nonlinearity (f_{in} = 10kHz)				
+25°C	–0.75	±0.5	+0.75	LSB
0 to +70°C	–0.95	±0.75	+0.95	LSB
–40 to +85°C	–1	±0.95	+2.5	LSB
Full Scale Absolute Accuracy				
+25°C	—	±0.1	±0.122	%FSR
0 to +70°C	—	±0.12	±0.36	%FSR
–40 to +85°C	—	±0.45	±0.85	%FSR
Unipolar Zero Error				
+25°C (see Figure 3)	—	±0.05	±0.122	%FSR
0 to +70°C	—	±0.1	±0.2	%FSR
–40 to +85°C	—	±0.2	±0.3	%FSR
Bipolar Zero Error				
+25°C (see Figure 3)	—	±0.05	±0.122	%FSR
0 to +70°C	—	±0.1	±0.2	%FSR
–40 to +85°C	—	±0.2	±0.3	%FSR
Bipolar Offset Error,				
+25°C(see Figure 3)	—	±0.05	±0.12	%FSR
0 to +70°C	—	±0.12	±0.3	%FSR
–40 to +85°C	—	±0.6	±0.8	%FSR
Gain Error (see Figure 3)				
+25°C	—	±0.018	±0.12	%
0 to +70°C	—	±0.12	±0.3	%
–40 to +85°C	—	±0.6	±0.8	%
No Missing Codes	0 to +70°C			
14 Bits	14 Bits			
Resolution				

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Output Coding	Straight Binary/Offset Binary/Two's Comp. Comp. Binary/Comp. Offset Binary or Complementary Two's Complement			
Logic Levels				
Logic "1"	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	Volts
Logic Loading "1"	—	—	–160	µA
Logic Loading "0"	—	—	+6.4	mA
Internal Reference Voltage, +25°C	+9.98	+10.0	+10.02	Volts
Drift	—	±13	±30	ppm/°C
External Current	—	—	5	mA
PERFORMANCE				
Slew Rate	—	±250	—	V/µs
Aperture Delay Time	—	—	10	ns
Aperture Uncertainty	—	—	±5	ps
S/H Acquisition Time (to ±0.003%FS, 10V step)	—	250	350	ns
Total Harm. Distort. (–0.5dB)				
dc to 100kHz	–78	–85	—	dB
100kHz to 500kHz	–77	–80	—	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)				
dc to 100kHz	75	80	—	dB
100kHz to 500kHz	74	77	—	dB
Signal–to–Noise Ratio (& distortion, –0.5dB)				
dc to 100kHz	74	80	—	dB
100kHz to 500kHz	73	78	—	dB
Spurious Free Dynamic Range①				
dc to 100kHz	78	86	—	dB
100 to 500kHz	77	83	—	dB
Two–tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, fs=1MHz, –0.5dB)	—	–85	—	dB
Input Bandwidth (–3dB)				
Small Signal (–20dB Input)	—	6	—	MHz
Large Signal (0dB Input)	—	1.75	—	MHz
Feedthrough Rejection (f_{in} = 500kHz)	—	87	—	dB
Overvoltage Recovery	—	1000	2000	ns
A/D Conversion Rate	1	—	—	MHz
Noise	—	250	—	µVrms
POWER REQUIREMENTS				
Power Supply Range				
+15V Supply	+14.25	+15.0	+15.75	Volts
–15V Supply	–14.25	–15.0	–15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Power Supply Current				
+15V Supply	—	+62	+85	mA
–15V Supply	—	–80	–95	mA
+5V Supply	—	+140	+160	mA
Power Dissipation	—	2.8	3.3	Watts
Power Supply Rejection	—	—	±0.02	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Oper. Temp. Range, Case				
ADS-941MC	0	—	+70	°C
ADS-941ME	–40	—	+85	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	32–pin, metal-sealed, ceramic TDIP			
Weight	0.46 ounces (13 grams)			

① Same specification as In-Band Harmonics or Peak Harmonics.

TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected to each other internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

2. Bypass the analog and digital supplies and the +10V REF. OUT (pin 1) to ground with a 4.7µF, 25V tantalum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor.

3. CODING SELECT (pin 8) is compatible with CMOS/TTL logic levels for those users desiring logic control of this function. The device has an internal pull-up resistor on this pin, allowing pin 8 to be connected to +5V or left open when a logic 1 is needed. See the Calibration Procedure for selecting an output coding.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to +10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Table 1 for the appropriate input range. Apply a pulse of 50 nanoseconds minimum to START CONVERT (pin 32) at a rate of 200kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. **Zero Adjustments**
   Apply a precision voltage reference source between ANALOG INPUT (pin 3) and SIGNAL GROUND (pin 4), then adjust the reference source output per Table 2.

Table 2. Zero and Gain Adjust

INPUT RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST FS - 1 1/2 LSB
0 to +10V	+305µV	+9.999085V
±5V	+305µV	+4.999085V

   For unipolar operation, adjust the zero trimpot so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with CODING SELECT (pin 8) tied low (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with pin 8 tied high (complementary binary).

   For bipolar operation, adjust the trimpot until the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied low (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied high (complementary offset binary).

   Two's complement coding requires using BIT 1 OUT ($\overline{\text{MSB}}$) (pin 31). With pin 8 tied low, adjust the trimpot until the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

3. **Full-Scale Adjustment**
   Set the output of the voltage reference used in step 2 to the value shown in Table 2.

   Adjust the gain trimpot until the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 with pin 8 tied low for straight binary/offset binary or between 00 0000 0000 0000 and 00 0000 0000 0001 with pin 8 tied high for complementary binary/complementary offset binary.

   Two's complement coding requires using pin 31. With pin 8 tied low, adjust the gain trimpot until the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

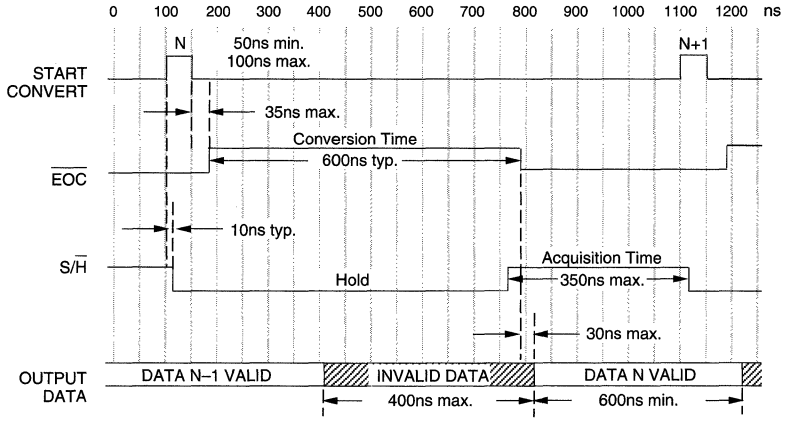


Figure 2. ADS-941 Timing Diagram

Removing System Errors

Use external potentiometers to remove system errors or to reduce the small initial errors to zero. Use a 100Ω trimpot in series with the analog input for gain adjustment. Use a fixed 50Ω resistor instead of the trimpot for operation without adjustment. Use a 20kΩ trimpot with the wiper tied to OFFSET ADJUST (pin 5) for zero/offset adjustment. Connect pin 5 to ANALOG GROUND (pin 6) for operation without zero/offset adjustment.

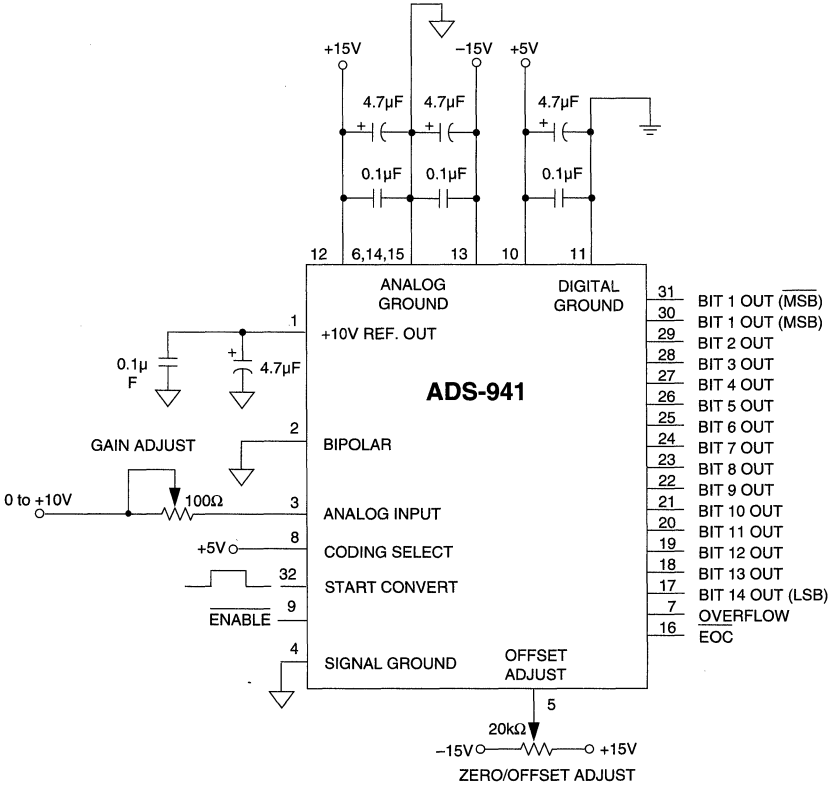


Figure 3. Typical ADS-941 Connection Diagram

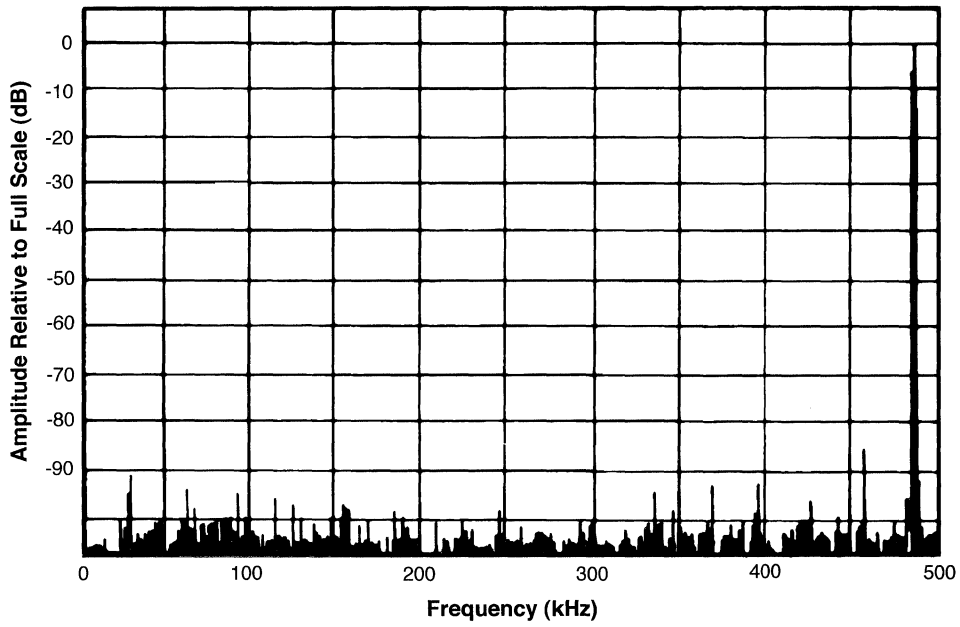
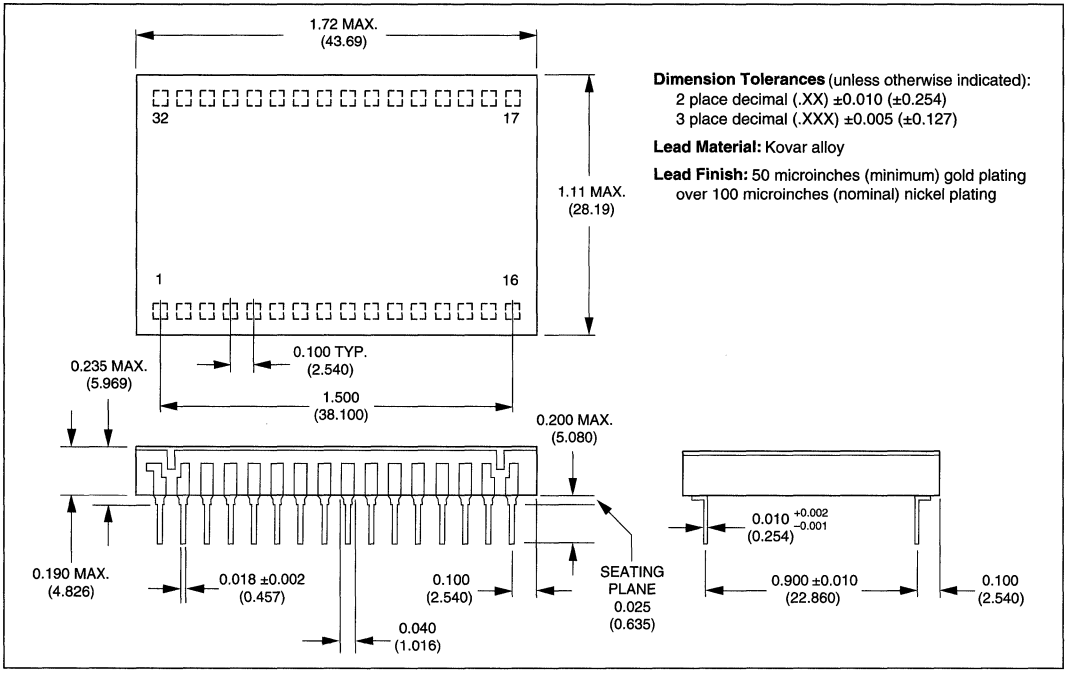


Figure 4. FFT Analysis of ADS-941
(fs = 1MHz, fin = 480kHz, Vin = -0.5dB, 4096 points)

Table 3. Output Coding

		STRAIGHT BIN.	COMP. BINARY			
UNIPOLAR SCALE	INPUT RANGE 0 to +10V	OUTPUT CODING MSB LSB	MSB LSB	MSB LSB	INPUT RANGE ±5V	BIPOLAR SCALE
+FS –1 LSB	+9.999390	11 1111 1111 1111	00 0000 0000 0000	01 1111 1111 1111	+4.999390	+FS –1 LSB
+7/8 FS	+8.750000	11 1000 0000 0000	00 0111 1111 1111	01 1000 0000 0000	+3.750000	+3/4 FS
+3/4 FS	+7.500000	11 0000 0000 0000	00 1111 1111 1111	01 0000 0000 0000	+2.500000	+1/2 FS
+1/2 FS	+5.000000	10 0000 0000 0000	01 1111 1111 1111	00 0000 0000 0000	0.000000	0
+1/4 FS	+2.500000	01 0000 0000 0000	10 1111 1111 1111	11 0000 0000 0000	–2.500000	–1/2 FS
+1/8 FS	+1.250000	00 1000 0000 0000	11 0111 1111 1111	10 1000 0000 0000	–3.750000	–3/4 FS
+1 LSB	+0.000610	00 0000 0000 0001	11 1111 1111 1110	10 0000 0000 0001	–4.999390	–FS +1 LSB
0	0.000000	00 0000 0000 0000	11 1111 1111 1111	10 0000 0000 0000	–5.000000	–FS
		OFF. BINARY	COMP. OFF. BIN.	TWO'S COMP.		

MECHANICAL DIMENSIONS
INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-941MC	0°C to +70°C
ADS-941ME	–40°C to +85°C

ACCESSORIES

ADS-EVAL4	Evaluation Board (without ADS-941)
HS-24	Heat Sink for all ADS-941 models

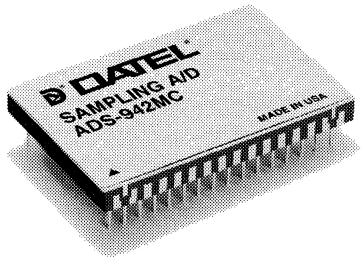
Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

DATEL®
INNOVATION and EXCELLENCE

ADS-942
14-Bit, 2MHz Sampling A/D Converters

FEATURES

- **14-Bit resolution**
- **2MHz minimum throughput**
- **Functionally complete**
- **Internal reference and sample/hold**
- **–85dB total harmonic distortion**
- **78dB signal-to-noise ratio**
- **Full Nyquist-rate sampling**
- **Small 32-pin DIP**
- **Low-power, 2.9 Watts**



GENERAL DESCRIPTION

DATEL's ADS-942 is a functionally complete, 14-bit, 2MHz, sampling A/D converter. Its standard, 32-pin, triple-wide ceramic DIP contains a fast-settling sample/hold amplifier, a 14-bit subranging (two-pass) A/D converter, a precision reference, three-state output register and all the timing and control logic necessary to operate from a single start convert pulse.

The ADS-942 is optimized for wideband frequency-domain applications and is fully FFT tested. The ADS-942 requires ±15V and +5V supplies and typically consumes 2.9 Watts.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	32	START CONVERT
2	BIPOLAR	31	BIT 1 OUT (MSB)
3	ANALOG INPUT	30	BIT 1 OUT (MSB)
4	SIGNAL GROUND	29	BIT 2 OUT
5	OFFSET ADJUST	28	BIT 3 OUT
6	ANALOG GROUND	27	BIT 4 OUT
7	OVERFLOW	26	BIT 5 OUT
8	CODING SELECT	25	BIT 6 OUT
9	ENABLE	24	BIT 7 OUT
10	+5V SUPPLY	23	BIT 8 OUT
11	DIGITAL GROUND	22	BIT 9 OUT
12	+15V SUPPLY	21	BIT 10 OUT
13	-15V SUPPLY	20	BIT 11 OUT
14	ANALOG GROUND	19	BIT 12 OUT
15	ANALOG GROUND	18	BIT 13 OUT
16	EOC	17	BIT 14 OUT (LSB)

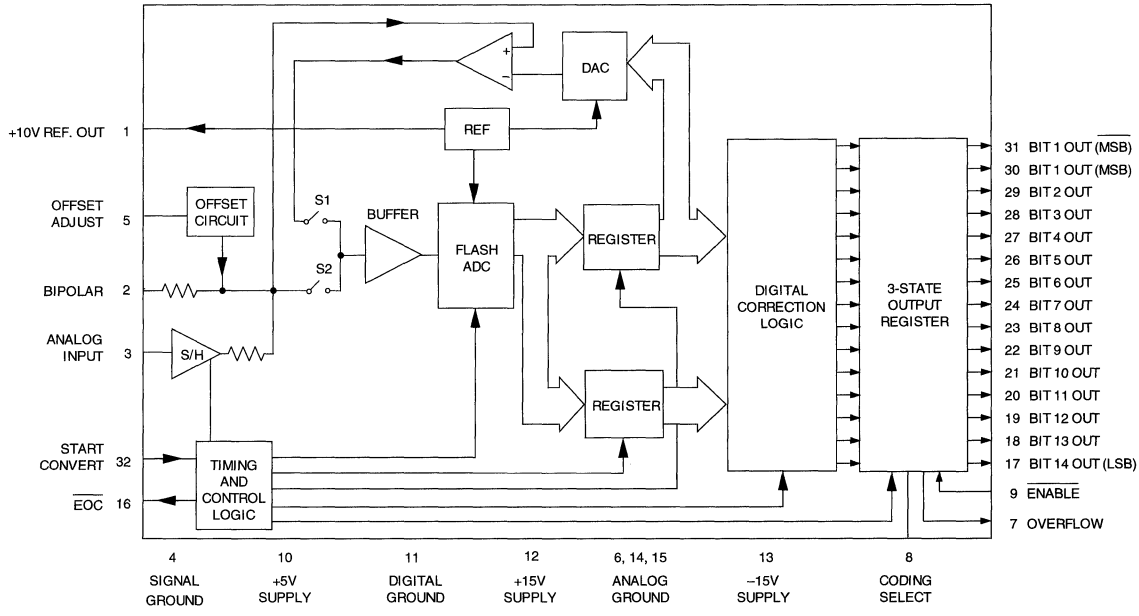


Figure 1. ADS-942 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	0 to +16	Volts
–15V Supply (Pin 13)	0 to –16	Volts
+5V Supply (Pin 10)	0 to +6	Volts
Digital Inputs (Pins 8, 9, 32)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 3)	±15	Volts
Lead Temp. (10 seconds)	300	°C

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V, 2MHz sampling rate, a minimum 7 minute warmup, unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
Unipolar	—	0 to +10	—	Volts
Bipolar	—	±5	—	Volts
Input Impedance	4.9	5	—	kΩ
Input Capacitance	—	7	15	pF
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Loading "1"	—	—	+5	µA
Logic Loading "0"	—	—	–600	µA
PERFORMANCE				
Integral Non–Linearity (fin = 1MHz)				
+25°C	—	±1	±2	LSB
0 to +70°C	—	±1	±2	LSB
–40 to +85°C	—	±2	±3	LSB
Differential Non–Linearity (fin = 1MHz)				
+25°C	–0.75	±0.5	+0.75	LSB
0 to +70°C	–0.95	±0.75	+1.25	LSB
–40 to +85°C	–1	±1	+2.5	LSB
Full Scale Absolute Accuracy				
+25°C	—	±0.1	±0.122	%FSR
0 to +70°C	—	±0.12	±0.36	%FSR
–40 to +85°C	—	±0.45	±0.85	%FSR
Unipolar Zero Error				
+25°C (see Figure 3)	—	±0.05	±0.122	%FSR
0 to +70°C	—	±0.1	±0.2	%FSR
–40 to +85°C	—	±0.2	±0.3	%FSR
Bipolar Zero Error				
+25°C (see Figure 3)	—	±0.05	±0.122	%FSR
0 to +70°C	—	±0.1	±0.2	%FSR
–40 to +85°C	—	±0.2	±0.3	%FSR
Bipolar Offset Error				
+25°C (see Figure 3)	—	±0.1	±0.2	%FSR
0 to +70°C	—	±0.12	±0.3	%FSR
–40 to +85°C	—	±0.5	±0.8	%FSR
Gain Error				
+25°C (see Figure 3)	—	±0.018	±0.122	%
0 to +70°C	—	±0.12	±0.3	%
–40 to +85°C	—	±0.6	±0.8	%
No Missing Codes (fin = 500kHz)	0 to +70°C			
14 Bits	–40 to +85°C			
13 Bits	14 Bits			
Resolution				

① Same specification as In-Band Harmonics or Peak Harmonics.

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Output Coding	Straight Bin./Offset Bin./2's Comp. Comp. Bin./Comp. Offset Bin./C2C			
Logic Levels				
Logic "1"	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	Volts
Logic Loading "1"	—	—	–160	µA
Logic Loading "0"	—	—	+6.4	mA
Internal Reference				
Voltage, +25°C	+9.98	+10.0	+10.02	Volts
Drift	—	±13	±30	ppm/°C
External Current	—	—	5	mA
DYNAMIC PERFORMANCE				
Total Harm. Distort. (–0.5dB)				
dc to 100kHz	—	–85	–76	dB
100kHz to 500kHz	—	–80	–75	dB
500kHz to 1MHz	—	–77	—	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)				
dc to 100kHz	74	78	—	dB
100kHz to 500kHz	73	75	—	dB
500kHz to 1MHz	—	73	—	dB
Signal–to–Noise Ratio (and distortion, –0.5dB)				
dc to 100kHz	73	78	—	dB
100kHz to 500kHz	72	75	—	dB
500kHz to 1MHz	—	72	—	dB
Spurious Free Dyn. Range ①				
dc to 100kHz	—	–86	–77	dB
100 to 500kHz	—	–81	–75	dB
500kHz to 1MHz	—	–78	—	dB
Two–tone Intermodulation Distortion (fin = 100kHz, 240kHz, fs = 2.0MHz, –0.5dB)	–85	—	—	dB
Input Bandwidth (–3dB)				
Small Signal (–20dB input)	—	6	—	MHz
Large Signal (–0.5dB input)	—	1.75	—	MHz
Slew Rate	—	±250	—	V/µs
Aperture Delay Time	—	—	±10	ns
Aperture Uncertainty	—	—	5	ps rms
S/H Acq. Time, (to ±0.003%FSR)				
Sinusoidal (fin = 1MHz)	—	120	150	ns
Step input	—	250	450	ns
Conversion Rate				
Sinusoidal (fin = 1MHz)	2	—	—	MHz
Step input	1.3	—	—	MHz
Feedthrough Rejection (fin = 1MHz)	—	85	—	dB
Overvoltage Recovery, ±12V	—	1000	2000	ns
Noise	—	250	—	µVrms
POWER REQUIREMENTS				
Power Supply Ranges				
+15V Supply	+14.25	+15.0	+15.75	Volts
–15V Supply	–14.25	–15.0	–15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Power Supply Currents				
+15V Supply	—	+65	+87	mA
–15V Supply	—	–80	–98	mA
+5V Supply	—	+150	+165	mA
Power Dissipation	—	2.9	3.4	Watts
Power Supply Rejection	—	—	±0.02	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
ADS-942MC	0	—	+70	°C
ADS–942ME	–40	—	+85	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	32-pin, metal-sealed, ceramic TDIP			
Weight	0.46 ounces (13 grams)			

TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected to each other internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

2. Bypass the analog and digital supplies and the +10V REF. OUT (pin 1) to ground with a 4.7µF, 25V tantalum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor.

3. CODING SELECT(pin 8) is compatible with CMOS/TTL logic levels for those users desiring logic control of this function. The device has an internal pull-up resistor on this pin, allowing pin 8 to be connected to +5V or left open when a logic 1 is needed. See the Calibration Procedure for selection of output coding.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to +10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Table 1 for the appropriate input voltage range. Apply a pulse of 35 nanoseconds minimum to START CONVERT (pin 32) at a rate of 200kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. **Zero Adjustments**
   Apply a precision voltage reference source between ANALOG INPUT (pin 3) and SIGNAL GROUND (pin 4), then adjust the reference source output per Table 2.

   For unipolar, adjust the zero trimpot so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with CODING SELECT (pin 8) tied low (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with pin 8 tied high (complementary binary).

   For bipolar operation, adjust the trimpot until the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied low (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied high (complementary offset binary).

   Two's complement coding requires using BIT 1 OUT $\overline{\text{(MSB)}}$ (pin 31). With pin 8 tied low, adjust the trimpot until the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

3. **Full-Scale Adjustment**
   Set the output of the voltage reference used in step 2 to the value shown in Table 2.

Table 2. Zero and Gain Adjust

INPUT RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST FS - 1 1/2 LSB
0 to +10V	+305µV	+9.999085V
±5V	+305µV	+4.999085V

   Adjust the gain trimpot until the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 with pin 8 tied low for straight binary/offset binary or between 00 0000 0000 0000 and 00 0000 0000 0001 with pin 8 tied high for complementary binary/complementary offset binary.

   Two's complement coding requires using pin 31. With pin 8 tied low, adjust the gain trimpot until the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

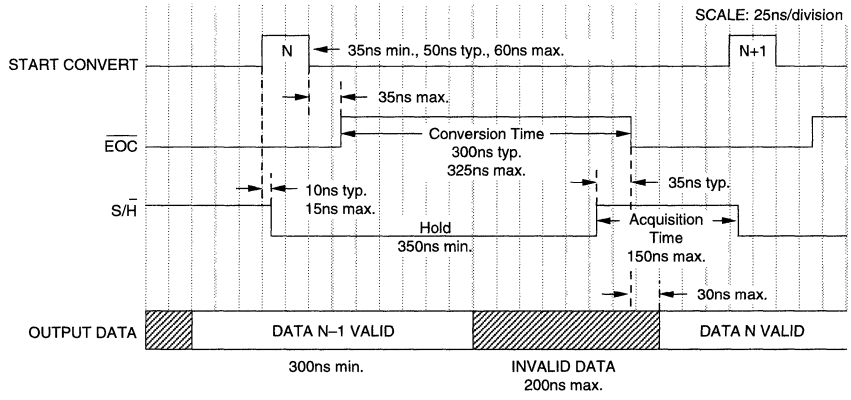


Figure 2. ADS-942 Timing Diagram

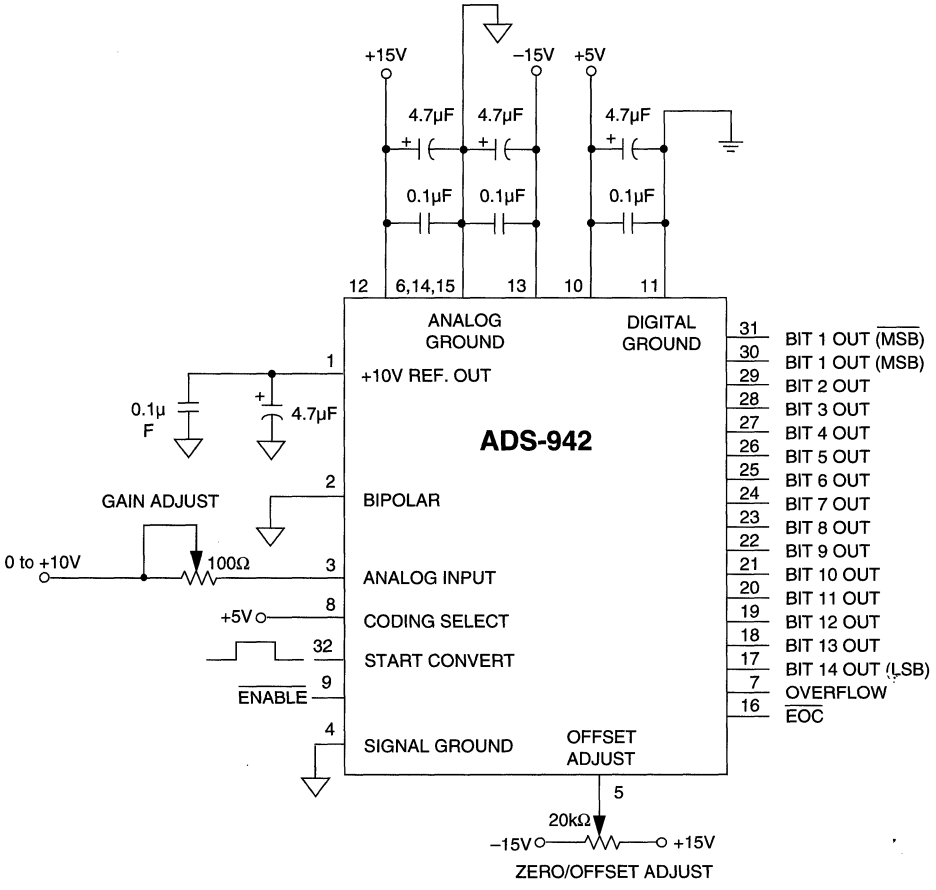


Figure 3. Typical ADS-942 Connection Diagram

Removing System Errors

Use external potentiometers to remove system errors or to reduce the small initial errors to zero. Use a 100Ω trimpot in series with the analog input for gain adjustment. Use a fixed 50Ω resistor instead of the trimpot for operation without adjustment. Use a 20kΩ trimpot with the wiper tied to OFFSET ADJUST (pin 5) for zero/offset adjustment. Connect pin 5 to ANALOG GROUND (pin 6) for operation without zero/offset adjustment.

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

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In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

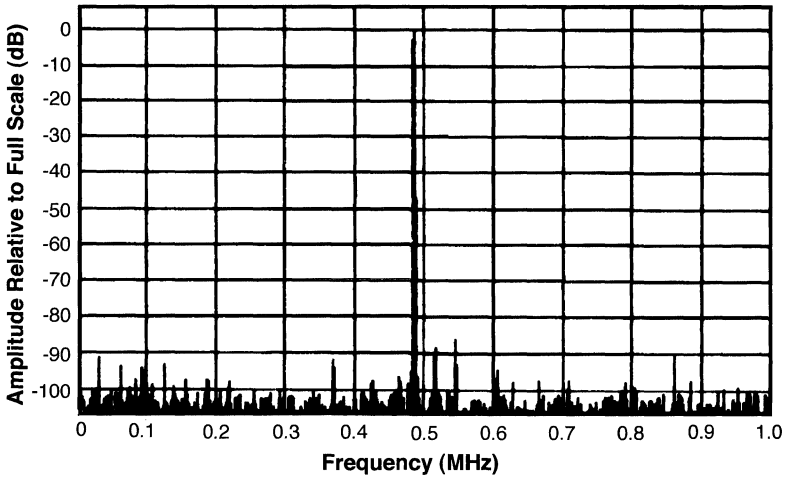
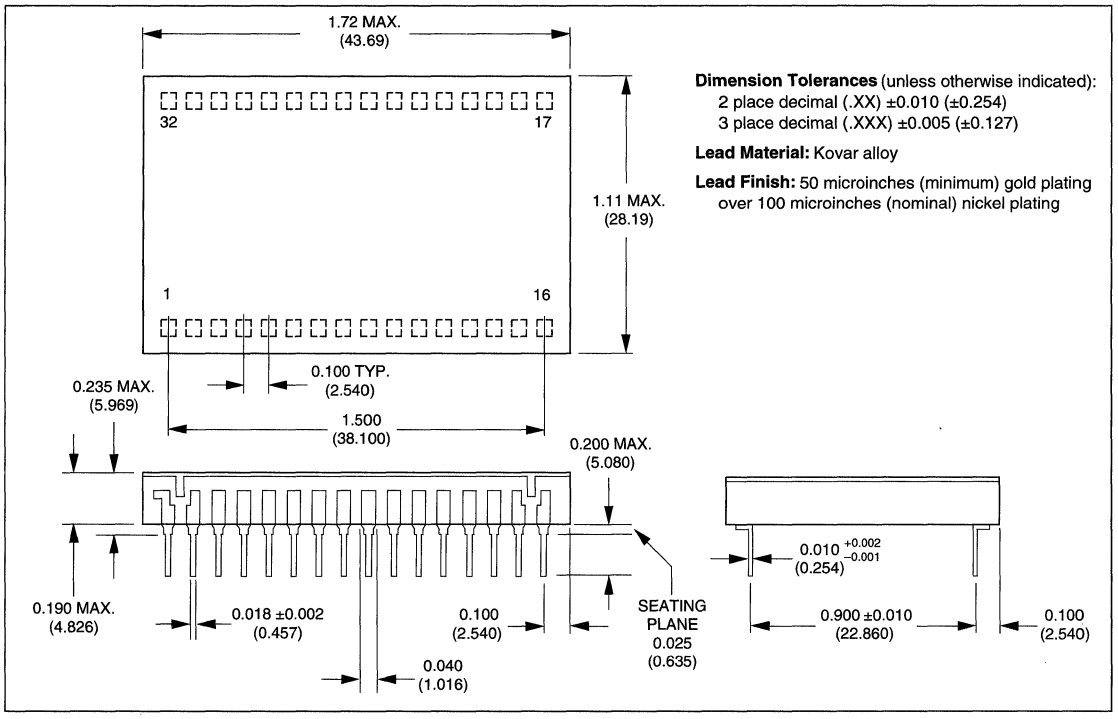


Figure 4. FFT Analysis of ADS-942
(f_S = 2MHz, f_{in} = 490kHz, V_{in} = –0.5dB, 4096 points)

Table 3. Output Coding

		STRAIGHT BIN.	COMP. BINARY			
UNIPOLAR SCALE	**INPUT RANGE 0 to +10V**	**OUTPUT CODING**			**INPUT RANGE ±5V**	**BIPOLAR SCALE**
		MSB LSB	**MSB LSB**	**MSB LSB**		
+FS –1 LSB	+9.999390	11 1111 1111 1111	00 0000 0000 0000	01 1111 1111 1111	+4.999390	+FS -1 LSB
+7/8 FS	+8.750000	11 1000 0000 0000	00 0111 1111 1111	01 1000 0000 0000	+3.750000	+3/4 FS
+3/4 FS	+7.500000	11 0000 0000 0000	00 1111 1111 1111	01 0000 0000 0000	+2.500000	+1/2 FS
+1/2 FS	+5.000000	10 0000 0000 0000	01 1111 1111 1111	00 0000 0000 0000	0.000000	0
+1/4 FS	+2.500000	01 0000 0000 0000	10 1111 1111 1111	11 0000 0000 0000	-2.500000	-1/2 FS
+1/8 FS	+1.250000	00 1000 0000 0000	11 0111 1111 1111	10 1000 0000 0000	-3.750000	-3/4 FS
+1 LSB	+0.000610	00 0000 0000 0001	11 1111 1111 1110	10 0000 0000 0001	-4.999390	-FS +1 LSB
0	0.000000	00 0000 0000 0000	11 1111 1111 1111	10 0000 0000 0000	-5.000000	-FS
		OFF. BINARY	COMP. OFF. BIN.	TWO'S COMP.		

MECHANICAL DIMENSIONS
INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-942MC	0°C to +70°C
ADS-942ME	–40°C to +85°C
ACCESSORIES	
ADS-EVAL4	Evaluation Board (without ADS-942)
HS-24	Heat Sink for all ADS-942 models

Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

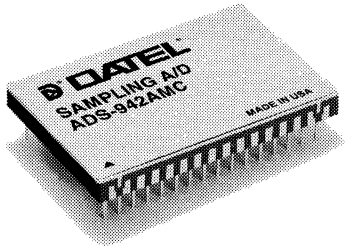
DATEL®
INNOVATION and EXCELLENCE

ADS-942A
14-Bit, 2MHz, Low-Power Sampling A/D Converters

1

FEATURES

- **14-Bit resolution**
- **2MHz minimum throughput**
- **Low-power, 2.2 Watts**
- **Functionally complete**
- **Internal reference and S/H amplifier**
- **78dB signal-to-noise ratio**
- **Full Nyquist-rate sampling**
- **Small 32-pin TDIP**



GENERAL DESCRIPTION

DATEL's ADS-942A is a functionally complete, 14-bit, 2MHz, sampling A/D converter. Packaged in a 32-pin TDIP, the unit contains a fast-settling sample/hold amplifier, a 14-bit subranging (two-pass) A/D converter, a precision reference, three-state output register, and all the timing/control logic necessary to operate from a single start convert pulse.

The ADS-942A is optimized for wideband frequency-domain applications and is fully FFT tested. The ADS-942A requires ±15V and ±5V supplies and typically consumes 2.2 Watts.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	32	START CONVERT
2	BIPOLAR	31	BIT 1 OUT (MSB)
3	ANALOG INPUT	30	BIT 1 OUT (MSB)
4	SIGNAL GROUND	29	BIT 2 OUT
5	OFFSET ADJUST	28	BIT 3 OUT
6	ANALOG GROUND	27	BIT 4 OUT
7	OVERFLOW	26	BIT 5 OUT
8	CODING SELECT	25	BIT 6 OUT
9	ENABLE	24	BIT 7 OUT
10	+5V SUPPLY	23	BIT 8 OUT
11	DIGITAL GROUND	22	BIT 9 OUT
12	+15V SUPPLY	21	BIT 10 OUT
13	–15V SUPPLY	20	BIT 11 OUT
14	–5V SUPPLY	19	BIT 12 OUT
15	ANALOG GROUND	18	BIT 13 OUT
16	EOC	17	BIT 14 OUT (LSB)

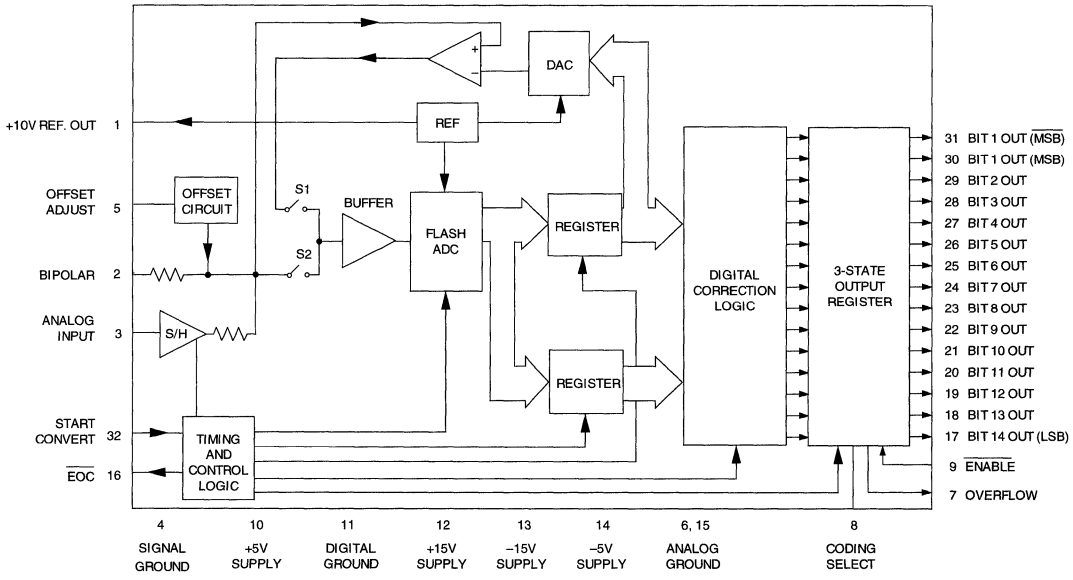


Figure 1. ADS-942A Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	0 to +16	Volts
–15V Supply (Pin 13)	0 to –16	Volts
+5V Supply (Pin 10)	0 to +6	Volts
–5V Supply (Pin 14)	0 to –6	Volts
Digital Inputs (Pins 8, 9, 32)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 3)	±15	Volts
Lead Temp. (10 seconds)	300	°C

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, ±V_{DD} = ±5V, 2MHz sampling rate, a minimum 7 minute warmup, unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
Unipolar	—	0 to +10	—	Volts
Bipolar	—	±5	—	Volts
Input Impedance	2.3	2.5	—	kΩ
Input Capacitance	—	7	15	pF
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Loading "1"	—	—	+10	µA
Logic Loading "0"	—	—	–600	µA
PERFORMANCE				
Integral Non–Linearity				
+25°C	—	±1	±2	LSB
0 to +70°C	—	±1	±2	LSB
–40 to +85°C	—	±2	±3	LSB
Differential Non–Linearity				
+25°C	—	±0.5	±0.75	LSB
0 to +70°C	–0.95	±0.75	+0.95	LSB
–40 to +85°C	–1	±1	+2.5	LSB
Full Scale Absolute Accuracy				
+25°C	—	±0.1	±0.122	%FSR
0 to +70°C	—	±0.12	±0.36	%FSR
–40 to +85°C	—	±0.45	±0.85	%FSR
Unipolar Zero Error				
+25°C	—	±0.05	±0.122	%FSR
0 to +70°C	—	±0.1	±0.2	%FSR
–40 to +85°C	—	±0.2	±0.3	%FSR
Bipolar Zero Error				
+25°C	—	±0.05	±0.122	%FSR
0 to +70°C	—	±0.1	±0.2	%FSR
–40 to +85°C	—	±0.2	±0.3	%FSR
Bipolar Offset Error				
+25°C	—	±0.1	±0.2	%FSR
0 to +70°C	—	±0.12	±0.3	%FSR
–40 to +85°C	—	±0.5	±0.8	%FSR
Gain Error				
+25°C	—	±0.018	±0.122	%
0 to +70°C	—	±0.12	±0.3	%
–40 to +85°C	—	±0.6	±0.8	%
No Missing Codes (fin = 500kHz)	0 to +70°C			
14 Bits	–40 to +85°C			
13 Bits	14 Bits			
Resolution				

① Effective Bits is equal to:

$$\frac{(\text{SNR} + \text{Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

② Same specification as In-Band Harmonics and Peak Harmonics.

③ Two-tone Intermodulation Distortion (IMD) conditions:
f_{in} = 100kHz, 240kHz, f_s = 2MHz, –0.5dB

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Output Coding	Straight Bin./Offset Bin./2's Comp. Comp. Bin./Comp. Offset Bin./C2C			
Logic Levels				
Logic "1"	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	Volts
Logic Loading "1"	—	—	–160	µA
Logic Loading "0"	—	—	+6.4	mA
Internal Reference				
Voltage, +25°C	+9.98	+10.0	+10.02	Volts
Drift	—	±13	±30	ppm/°C
External Current	—	—	5	mA
DYNAMIC PERFORMANCE				
Total Harm. Distort. (–0.5dB)				
dc to 100kHz	—	–85	–76	dB
100kHz to 500kHz	—	–80	–75	dB
500kHz to 1MHz	—	–77	—	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)				
dc to 100kHz	74	78	—	dB
100kHz to 500kHz	73	75	—	dB
500kHz to 1MHz	—	73	—	dB
Signal–to–Noise Ratio (and distortion, –0.5dB) ①				
dc to 100kHz	73	78	—	dB
100kHz to 500kHz	72	75	—	dB
500kHz to 1MHz	—	72	—	dB
Spurious Free Dyn. Range ②				
dc to 100kHz	—	–86	–77	dB
100 to 500kHz	—	–81	–75	dB
500kHz to 1MHz	—	–78	—	dB
Two–tone IMD ③	—	–85	—	dB
Input Bandwidth (–3dB)				
Small Signal (–20dB input)	—	6	—	MHz
Large Signal (–0.5dB input)	—	1.75	—	MHz
Slew Rate	—	±250	—	V/µs
Aperture Delay Time	—	—	±10	ns
Aperture Uncertainty	—	—	5	ps, rms
S/H Acq. Time, (to ±0.003%FSR)				
Sinusoidal (f_{in} = 1MHz)	—	—	150	ns
Step input (10V)	—	250	450	ns
Conversion Rate				
Sinusoidal (f_{in} = 1MHz)	2	—	—	MHz
Step input	1.3	—	—	MHz
Feedthrough Rejection				
(f_{in} = 1MHz)	—	85	—	dB
Overvoltage Recovery, ±12V	—	1000	2000	ns
Noise	—	250	—	µVrms
POWER REQUIREMENTS				
Power Supply Ranges				
+15V Supply	+14.25	+15.0	+15.75	Volts
–15V Supply	–14.25	–15.0	–15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	Volts
Power Supply Currents				
+15V Supply	—	+65	+80	mA
–15V Supply	—	–19	–35	mA
+5V Supply	—	+150	+175	mA
–5V Supply	—	–55	–65	mA
Power Dissipation	—	2.2	2.6	Watts
Power Supply Rejection	—	—	±0.03	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
ADS-942AMC	0	—	+70	°C
ADS–942AME	–40	—	+85	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	32-pin, metal-sealed, ceramic TDIP			
Weight	0.46 ounces (13 grams)			

TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. Connect the digital and analog grounds to one point, the analog ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. SIGNAL GROUND (pin 4) is not internally connected to ANALOG GROUND (pins 6, 15).

2. Bypass the analog and digital supplies and the +10V REF. OUT (pin 1) to ground with a 4.7µF, 25V tantalum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor.

3. CODING SELECT(pin 8) is compatible with CMOS/TTL logic levels for those users desiring logic control of this function. There is an internal pull-up resistor on this pin; connect to +5V or leave open for logic 1. See the Calibration Procedure for selecting an output coding.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

5. OVERFLOW (pin 7) changes from low (logic "0") to high (logic "1") when the input voltage exceeds the input voltage range limits by 1LSB (610µV).

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to +10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Table 1 for the appropriate input voltage range. Apply a pulse of 35 nanoseconds minimum to START CONVERT (pin 32) at a rate of 200kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

Table 2. Zero and Gain Adjust

INPUT RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST FS - 1 1/2 LSB
0 to +10V	+305µV	+9.999085V
±5V	+305µV	+4.999085V

2. **Zero Adjustments**
Apply a precision voltage reference source between ANALOG INPUT (pin 3) and SIGNAL GROUND (pin 4), then adjust the reference source output per Table 2.

For unipolar, adjust the zero trimpot so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with CODING SELECT (pin 8) tied low (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with pin 8 tied high (complementary binary).

For bipolar operation, adjust the trimpot until the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied low (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied high (complementary offset binary).

Two's complement coding requires using pin 31 ($\overline{\text{MSB}}$). With pin 8 tied low, adjust the trimpot until the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

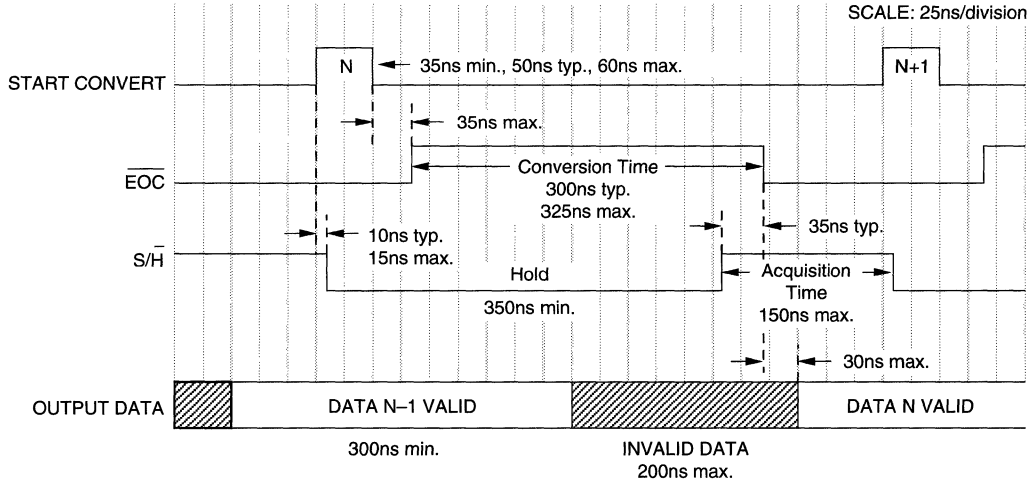


Figure 2. ADS-942A Timing Diagram

3. **Full-Scale (Gain) Adjustment**
   Set the output of the voltage reference used in step 2 to the value shown in Table 2.

   Adjust the gain trimpot until the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 with pin 8 tied low (straight binary/offset binary) or between 00 0000 0000 0000 and 00 0000 0000 0001 with pin 8 tied high (complementary binary/complementary offset binary).

   Two's complement coding requires using pin 31 ($\overline{\text{MSB}}$). With pin 8 tied low, adjust the gain trimpot until the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

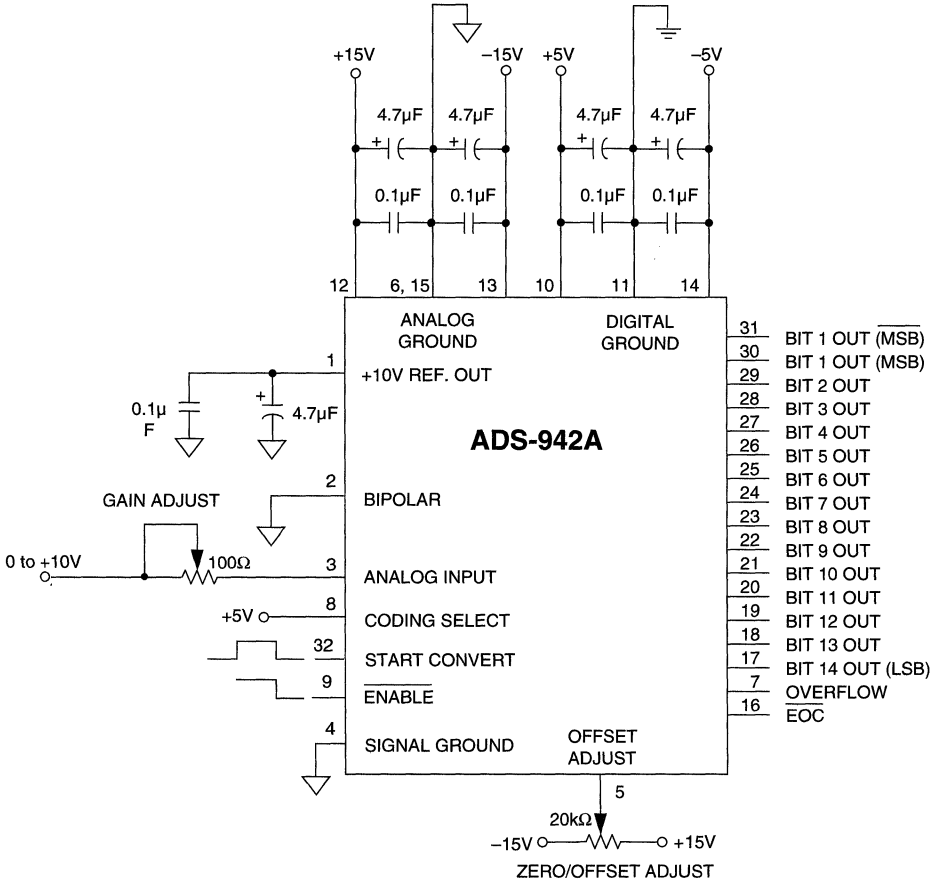


Figure 3. ADS-942A Connection Diagram (Unipolar Input)

Use external trimpots to remove system errors or to reduce small initial errors to zero. Use a 100Ω trimpot in series with the analog input for gain adjustment; use a fixed 50Ω resistor in its place for operation without adjustment.

Use a 20kΩ trimpot with the wiper tied to OFFSET ADJUST (pin 5) for zero/offset adjustment. Connect pin 5 to ANALOG GROUND (pin 6) for operation without zero/offset adjustment.

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

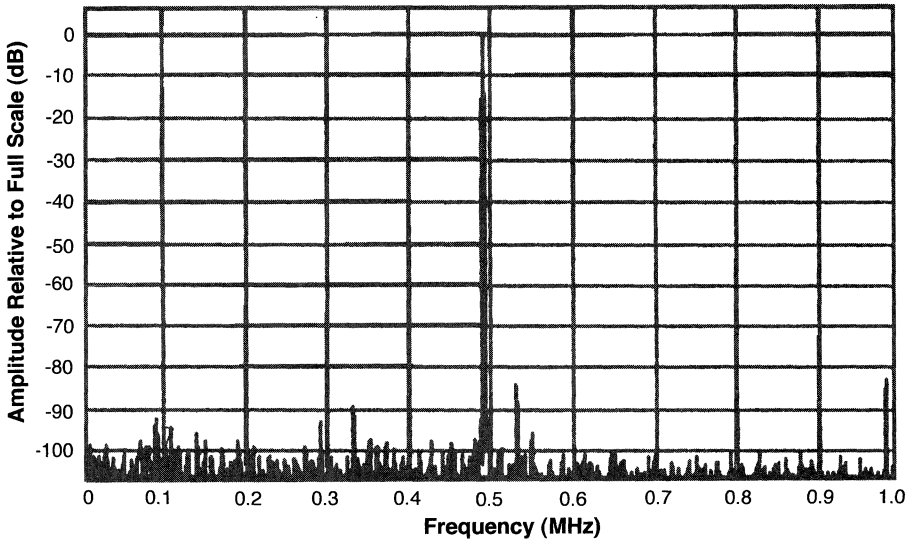


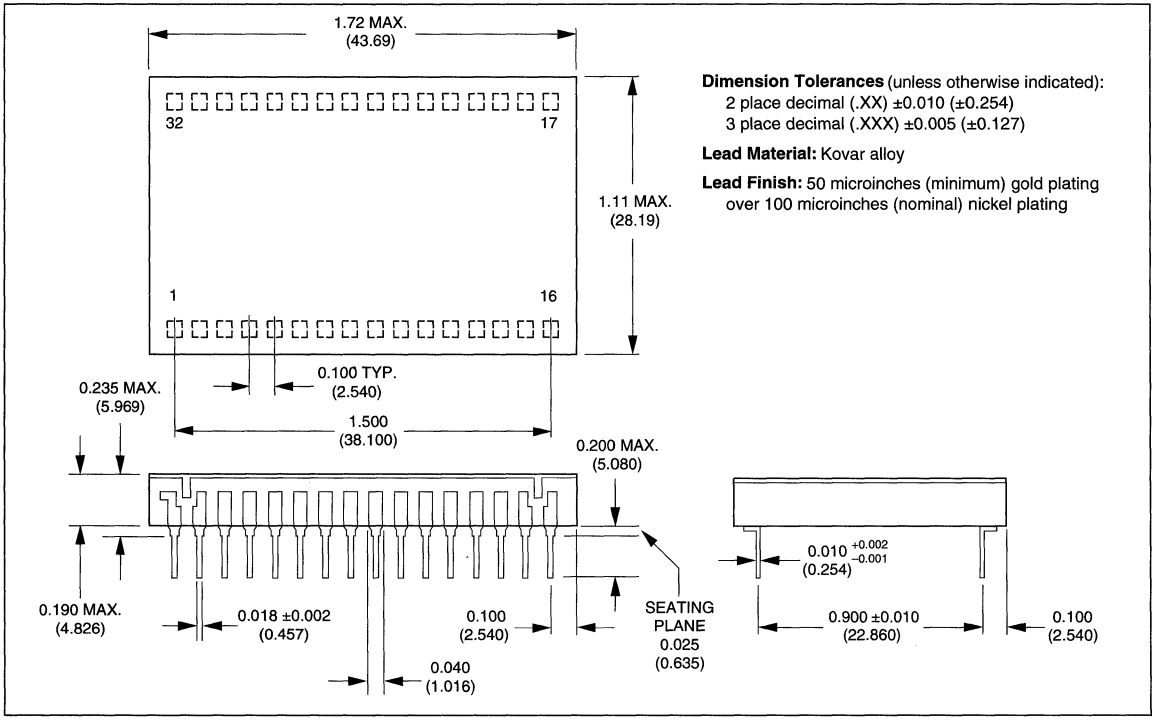
Figure 4. FFT Analysis of ADS-942A
(f_S = 2MHz, f_{in} = 490kHz, V_{in} = –0.5dB, 4096 points)

Table 3. Output Coding

	STRAIGHT BIN.	COMP. BINARY				
UNIPOLAR SCALE	INPUT VOLTAGE 0 to +10V	OUTPUT CODING MSB LSB	MSB LSB	MSB LSB	INPUT VOLTAGE ±5V	BIPOLAR SCALE
+FS –1 LSB	+9.999390	11 1111 1111 1111	00 0000 0000 0000	01 1111 1111 1111	+4.999390	+FS -1LSB
+7/8 FS	+8.750000	11 1000 0000 0000	00 0111 1111 1111	01 1000 0000 0000	+3.750000	+3/4FS
+3/4 FS	+7.500000	11 0000 0000 0000	00 1111 1111 1111	01 0000 0000 0000	+2.500000	+1/2FS
+1/2 FS	+5.000000	10 0000 0000 0000	01 1111 1111 1111	00 0000 0000 0000	0.000000	0
+1/4 FS	+2.500000	01 0000 0000 0000	10 1111 1111 1111	11 0000 0000 0000	-2.500000	-1/2FS
+1/8 FS	+1.250000	00 1000 0000 0000	11 0111 1111 1111	10 1000 0000 0000	-3.750000	-3/4FS
+1 LSB	+0.000610	00 0000 0000 0001	11 1111 1111 1110	10 0000 0000 0001	-4.999390	-FS +1LSB
0	0.000000	00 0000 0000 0000	11 1111 1111 1111	10 0000 0000 0000	-5.000000	-FS
	OFF. BINARY	COMP. OFF. BIN.	TWO'S COMP.			

MECHANICAL DIMENSIONS

INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-942AMC	0 to +70°C
ADS-942AME	–40 to +85°C

ACCESSORIES

ADS-EVAL4	Evaluation Board (without ADS-942)
HS-32	Heat Sink for all ADS-942 models

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

DATEL®
INNOVATION and EXCELLENCE

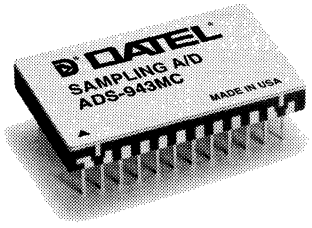
PRELIMINARY PRODUCT DATA

ADS-943
14-Bit, 3MHz, Low-Distortion Sampling A/D Converters

1

FEATURES

- **14-Bit resolution**
- **3MHz minimum sampling rate**
- **Ideal for both frequency and time-domain applications**
- **Excellent peak harmonics, –85dB**
- **Excellent signal-to-noise ratio, 79dB**
- **No missing codes over full military temperature range**
- **±5V supplies, 1.8 Watts**
- **Small, 24-pin ceramic DDIP**
- **Low cost**



GENERAL DESCRIPTION

The low-cost ADS-943 is a 14-bit, 3MHz sampling A/D converter optimized to meet the demanding dynamic-range and sampling-rate requirements of contemporary digital telecommunications applications. The ADS-943's outstanding dynamic performance is evidenced by a peak harmonic specification of –85dB and a signal-to-noise ratio (SNR) of 79dB. Additionally, the ADS-943 easily achieves the 2.2MHz minimum sampling rate required by digital receivers in certain ADSL, HDSL and ATM applications. The ADS-943 also addresses size and power constraints normally associated with these types of applications. This device requires just ±5V supplies, dissipates 1.8 Watts, and is packaged in a very small 24-pin DDIP.

Although optimized for frequency-domain applications, the ADS-943's DNL and noise specifications are also outstanding, thereby making it an equally impressive device for time-domain applications (graphic and medical imaging, process control, etc.). In fact, the ADS-943 guarantees no missing codes to the 14-bit level over the full military operating temperature range.

The functionally complete ADS-943 contains a fast-settling sample-hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL. The unit is edge-triggered, requiring only the rising edge of a start convert pulse to initiate a conversion.

The device is offered with a bipolar input range of ±2V. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. A proprietary, auto-calibrating, error-correcting circuit allows the device to achieve specified performance over the full military temperature range.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	24	ANALOG GROUND
2	BIT 2	23	OFFSET ADJUST
3	BIT 3	22	+5V ANALOG SUPPLY
4	BIT 4	21	ANALOG INPUT
5	BIT 5	20	–5V SUPPLY
6	BIT 6	19	ANALOG GROUND
7	BIT 7	18	START CONVERT
8	BIT 8	17	$\overline{EOC}$
9	BIT 9	16	BIT 14 (LSB)
10	BIT 10	15	BIT 13
11	BIT 11	14	DIGITAL GROUND
12	BIT 12	13	+5V DIGITAL SUPPLY

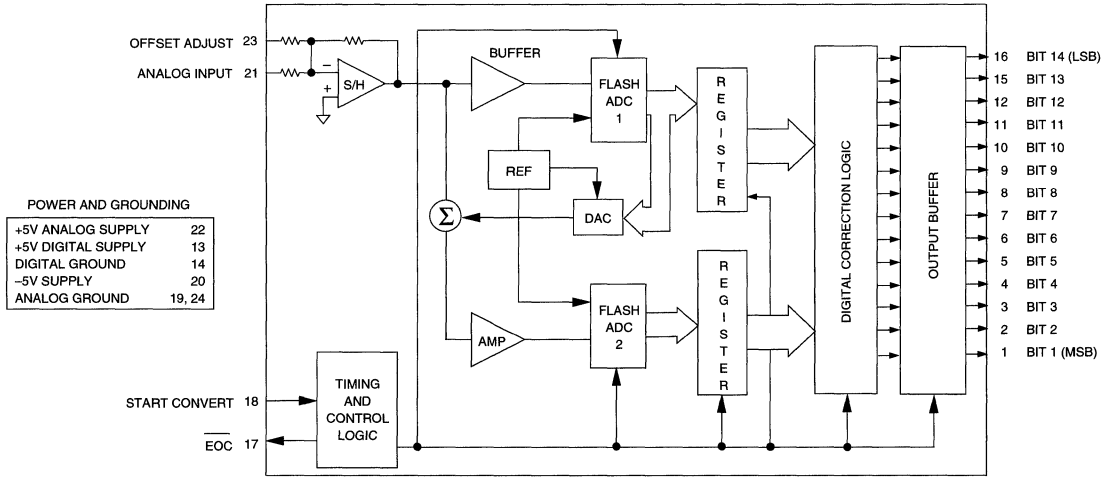


Figure 1. ADS-943 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Supply (Pins 13, 22)	0 to +6	Volts
–5V Supply (Pin 20)	0 to –6	Volts
Digital Input (Pin 18)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 21)	±5	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–943MC	0	—	+70	°C
ADS–943MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	6	—	°C/Watt
θca	—	23	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{DD} = ±5V, 3MHz sampling rate, and a minimum 3 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	±2	—	—	±2	—	—	±2	—	Volts
Input Resistance	—	300	—	—	300	—	—	300	—	Ω
Input Capacitance	—	6	15	—	6	15	—	6	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	150	—	—	150	—	—	150	—	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.75	—	—	±0.75	—	—	±1	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	–0.95	±0.5	+1.25	–0.95	±0.5	+1.25	–0.95	±0.5	+1.5	LSB
Full Scale Absolute Accuracy	—	±0.15	±0.4	—	±0.15	±0.4	—	±0.4	±0.8	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.1	±0.3	—	±0.1	±0.3	—	±0.3	±0.6	%FSR
Gain Error (Tech Note 2)	—	±0.2	±0.4	—	±0.2	±0.4	—	±0.4	±1.5	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 500kHz	—	–85	–78	—	–85	–77	—	–81	–74	dB
500kHz to 1MHz	—	–80	–74	—	–80	–74	—	–77	–70	dB
1MHz to 1.5MHz	—	–79	–73	—	–79	–73	—	–73	–68	dB
Total Harmonic Distortion (–0.5dB)										
dc to 500kHz	—	–83	–76	—	–83	–75	—	–78	–72	dB
500kHz to 1MHz	—	–78	–72	—	–78	–72	—	–74	–68	dB
1MHz to 1.5MHz	—	–77	–71	—	–77	–71	—	–71	–66	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)										
dc to 500kHz	75	79	—	75	79	—	73	76	—	dB
500kHz to 1MHz	75	79	—	75	79	—	73	76	—	dB
1MHz to 1.5MHz	73	76	—	73	76	—	72	76	—	dB
Signal–to–Noise Ratio ④ (& distortion, –0.5dB)										
dc to 500kHz	72	75	—	72	75	—	70	74	—	dB
500kHz to 1MHz	71	75	—	71	75	—	68	72	—	dB
1MHz to 1.5MHz	70	74	—	70	74	—	66	70	—	dB
Noise	—	150	—	—	150	—	—	150	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 975kHz, 1.2MHz, f_s = 3MHz, –0.5dB)	—	–82	—	—	–82	—	—	–82	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	30	—	—	30	—	—	30	—	MHz
Large Signal (–0dB input)	—	10	—	—	10	—	—	10	—	MHz
Feedthrough Rejection (f_{in} = 1.5MHz)	—	85	—	—	85	—	—	85	—	dB
Slew Rate	—	±400	—	—	±400	—	—	±400	—	V/µs
Aperture Delay Time	—	+5	—	—	+5	—	—	+5	—	ns
Aperture Uncertainty	—	2	—	—	2	—	—	2	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 4V step)	—	228	235	—	228	235	—	228	235	ns
Overvoltage Recovery Time ⑤	—	100	333	—	100	333	—	100	333	ns
A/D Conversion Rate	3	—	—	3	—	—	3	—	—	MHz

DIGITAL OUTPUTS	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Output Coding	Offset Binary									
POWER REQUIREMENTS										
Power Supply Ranges ⑥										
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.9	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	–4.9	–5.0	–5.25	Volts
Power Supply Currents										
+5V Supply	—	+220	+260	—	+220	+260	—	+220	+260	mA
–5V Supply	—	–110	–130	—	–110	–130	—	–110	–130	mA
Power Dissipation	—	1.8	2	—	1.8	2	—	1.8	2	Watts
Power Supply Rejection	—	—	±0.1	—	—	±0.1	—	—	±0.1	%FSR/%V

Footnotes:

① All power supplies should be on before applying a start convert pulse. All supplies and the clock (start convert pulses) must be present during warmup periods. The device must be continuously converting during this time.

② Contact DATEL for other input voltage ranges.

③ A 150ns wide start convert pulse is used for all production testing. For applications requiring less than a 3MHz sampling rate, wider start convert pulses can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range. This time is only guaranteed if the input does not exceed ±2.2V.

⑥ The minimum supply voltages of +4.9V and –4.9V for $\pm V_{DD}$ are required for –55°C operation only. The minimum limits are +4.75V and –4.75V when operating at +125°C.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-943 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19 and 24) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-943 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figures 2 and 3.

   When using this circuitry, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. Applying a start convert pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") will initiate a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

4. A passive bandpass filter is used at the input of the A/D for all production testing.

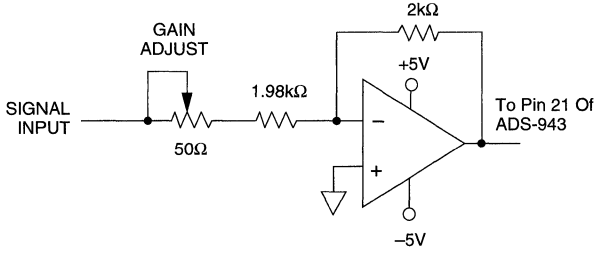


Figure 2. Optional ADS-943 Gain Adjust Calibration Circuit

CALIBRATION PROCEDURE

(Refer to Figures 2 and 3 and Tables 1 and 2)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuits in Figures 2 and 3 are guaranteed to compensate for the ADS-943's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

Offset adjusting for the ADS-943 is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+122µV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+1.99963V).

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 18) so the converter is continuously converting.
2. Apply +122µV to the ANALOG INPUT (pin 21).
3. Adjust the offset potentiometer until the output bits are 1000 0000 00000 and the LSB flickers between 0 and 1.

Table 1. Gain and Zero Adjust

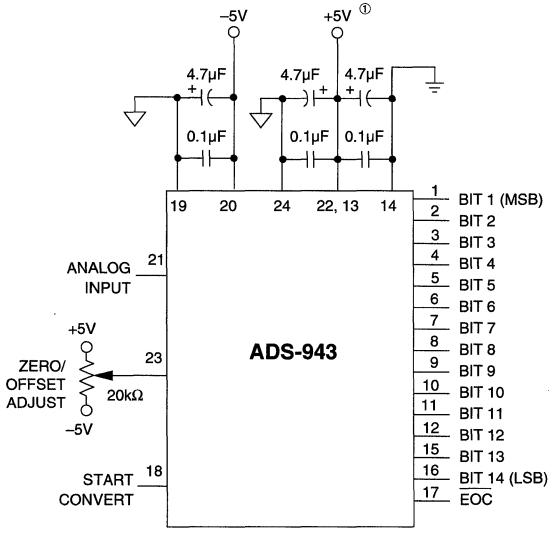
INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS–1 1/2 LSB
±2V	+122µV	+1.99963V

Gain Adjust Procedure

1. Apply +1.99963V to the ANALOG INPUT (pin 21).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.
3. To confirm proper operation of the device, vary the input signal to obtain the output coding listed in Table 2.

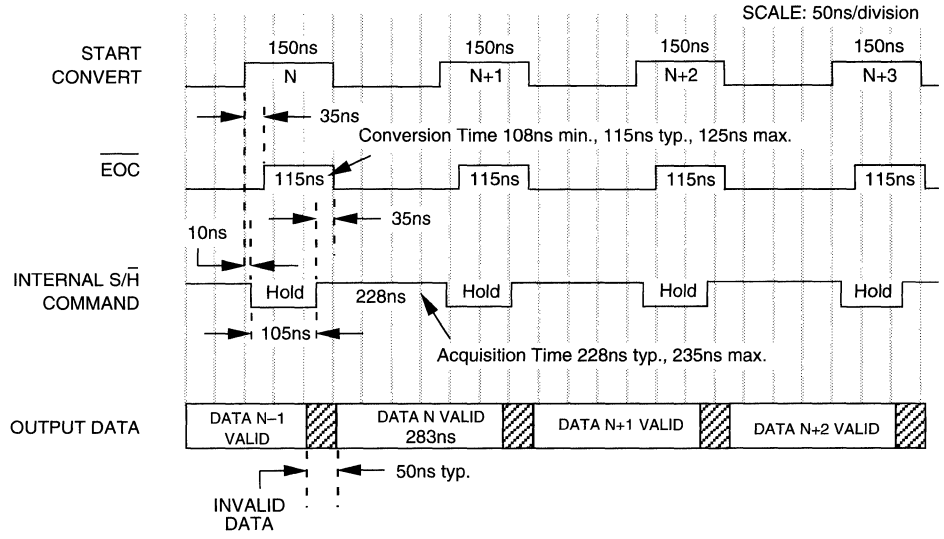
Table 2. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT VOLTAGE (±2V RANGE)	OFFSET BINARY MSB LSB
+FS –1 LSB	+1.99976	11 1111 1111 1111
+3/4 FS	+1.50000	11 1000 0000 0000
+1/2 FS	+1.00000	11 0000 0000 0000
0	0.00000	10 0000 0000 0000
–1/2 FS	–1.00000	01 0000 0000 0000
–3/4 FS	–1.50000	00 1000 0000 0000
–FS +1 LSB	–1.99976	00 0000 0000 0001
–FS	–2.00000	00 0000 0000 0000



① A single +5V supply should be used for both the +5V analog and +5V digital. If separate supplies are used, the difference between the two cannot exceed 100mV.

Figure 3. Connection Diagram



Notes:
1. Scale is 50ns/division, sampling rate = 3MHz.
2. The START CONVERT pulse must be between 20 and 70ns wide or between 130 and 250ns wide when sampling at 3MHz.

Figure 4. ADS-943 Timing Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

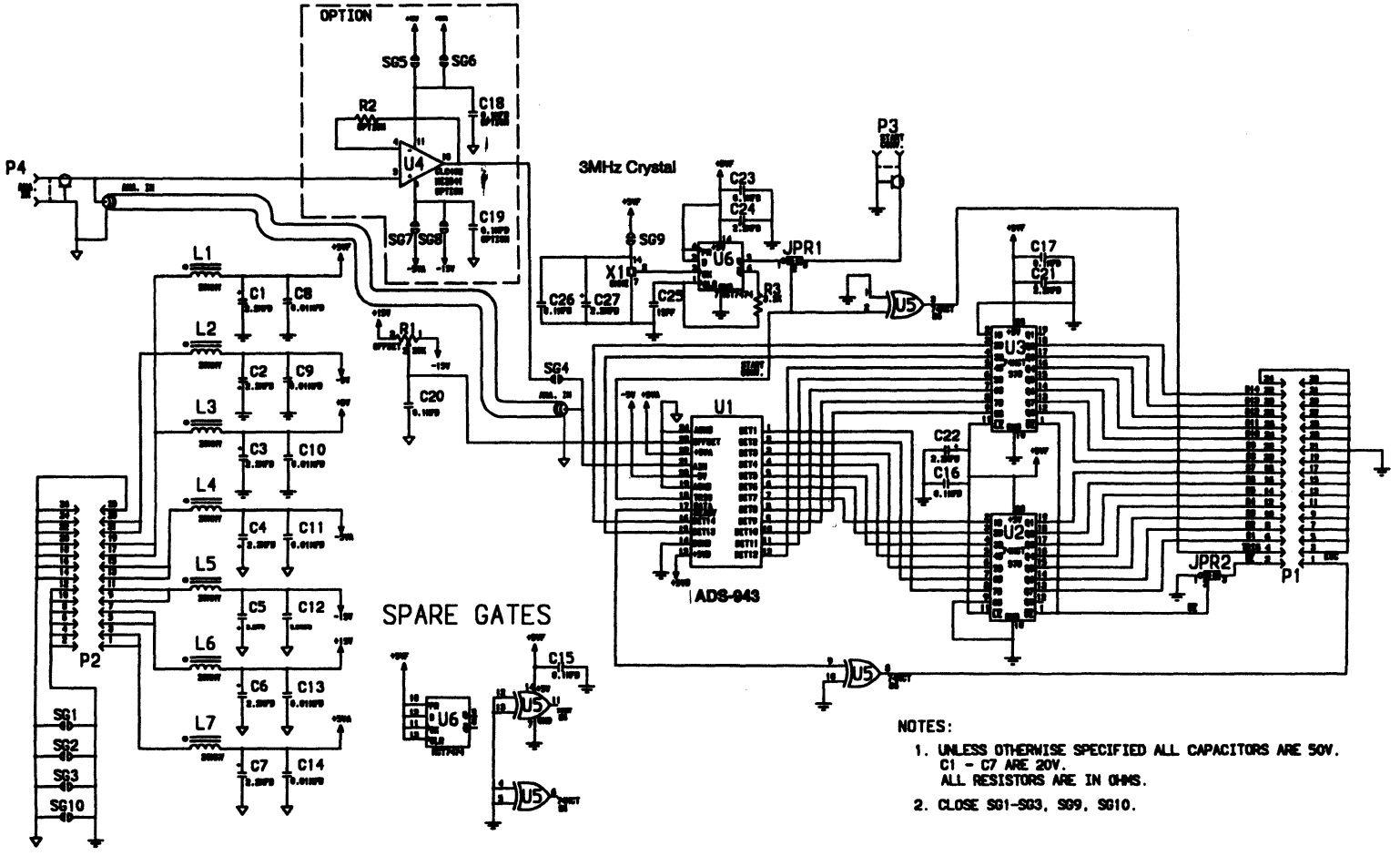


Figure 5. ADS-943 Evaluation Board Schematic

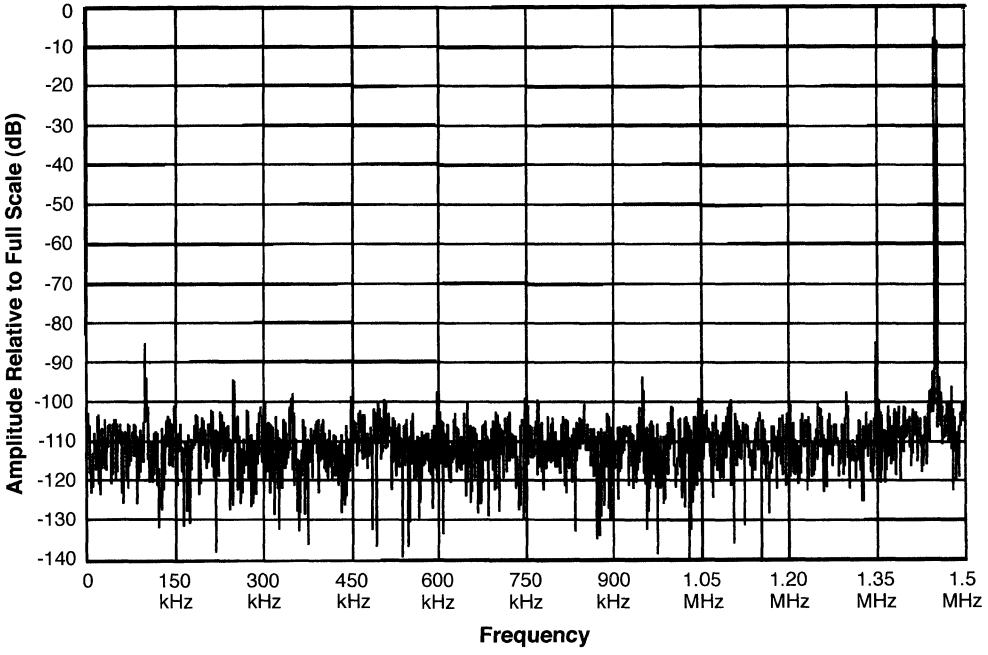
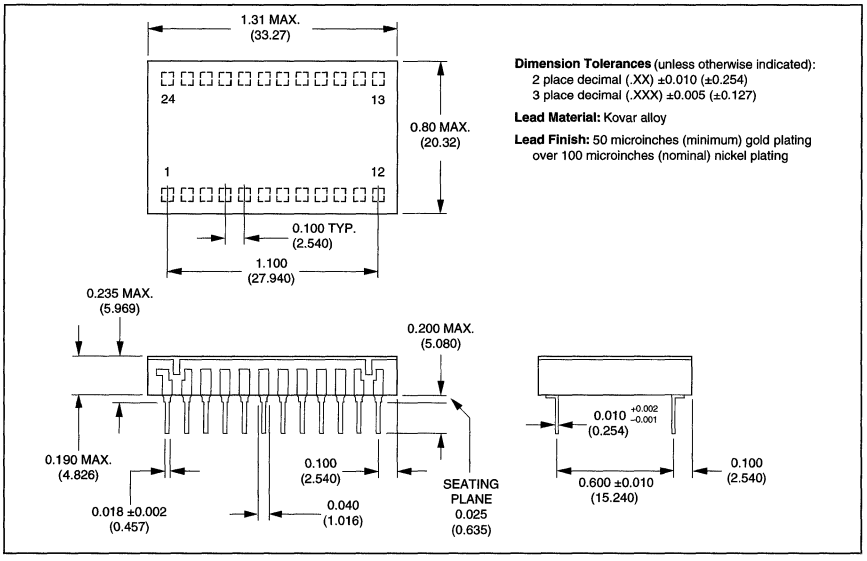


Figure 5. FFT Analysis of ADS-943
(f_S = 3MHz, f_{in} = 1.485MHz, V_{in} = –0.5dB, 16,384-point FFT)

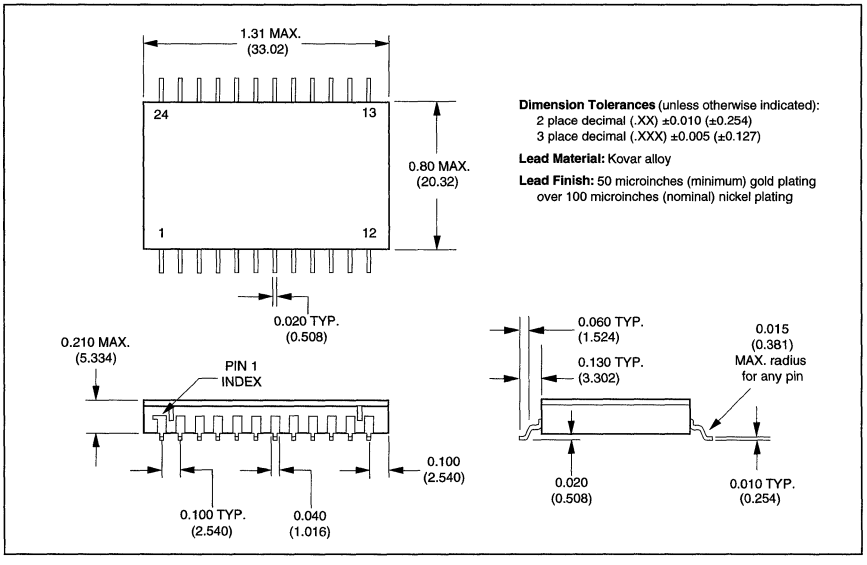
MECHANICAL DIMENSIONS
INCHES (mm)

24-Pin DDIP Versions

ADS-943MC
ADS-943MM



24-Pin Surface Mount Version



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-943MC	0 to +70°C	Bipolar (±2V)
ADS-943MM	–55 to +125°C	Bipolar (±2V)

ACCESSORIES

ADS-B943	Evaluation Board (without ADS-943)
HS-24	Heat Sink for all ADS-943 DDIP models

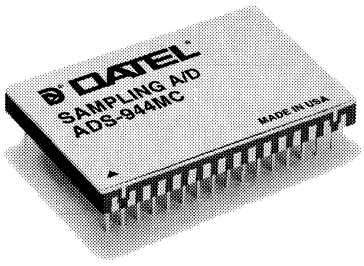
Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product, or surface-mount packaging, contact DATEL.

DATEL®
INNOVATION and EXCELLENCE

ADS-944
14-Bit, 5MHz Sampling A/D Converters

FEATURES

- **14-Bit resolution**
- **5MHz minimum sampling rate**
- **No missing codes over full military temperature range**
- **Edge-triggered, no pipeline delay**
- **Low power, 2.95 Watts**
- **Small, 32-pin, ceramic TDIP package**
- **SMT package available**
- **Excellent dynamic performance**
- **MIL-STD-883 screening or DESC SMD available**



GENERAL DESCRIPTION

The low-cost ADS-944 is a high-performance, 14-bit, 5MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. The dynamic performance of the ADS-944 has been optimized to achieve a THD of –77dB and a SNR of 76dB.

Packaged in a small, 32-pin TDIP, the functionally complete ADS-944 contains a fast-settling sample-hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing and control logic, three-state outputs, and error-correction circuitry. Digital input and output levels are TTL.

Requiring ±15V,+5V and –5.2V supplies, the ADS-944 typically dissipates 2.95 Watts. The unit is offered with a bipolar input range of ±1.25V. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. Typical applications include radar signal analysis, medical/graphic imaging, and FFT spectrum analysis.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V ANALOG SUPPLY	32	START CONVERT
2	–5.2V DIGITAL SUPPLY	31	$\overline{\text{BIT 1 (MSB)}}$
3	ANALOG INPUT	30	BIT 1 (MSB)
4	ANALOG GROUND	29	BIT 2
5	OFFSET ADJUST	28	BIT 3
6	ANALOG GROUND	27	BIT 4
7	GAIN ADJUST	26	BIT 5
8	COMP. BITS	25	BIT 6
9	$\overline{\text{OUTPUT ENABLE}}$	24	BIT 7
10	+5V DIGITAL SUPPLY	23	BIT 8
11	ANALOG GROUND	22	BIT 9
12	+15V SUPPLY	21	BIT 10
13	–15V SUPPLY	20	BIT 11
14	–5.2V ANALOG SUPPLY	19	BIT 12
15	DIGITAL GROUND	18	BIT 13
16	$\overline{\text{EOC}}$	17	BIT 14 (LSB)

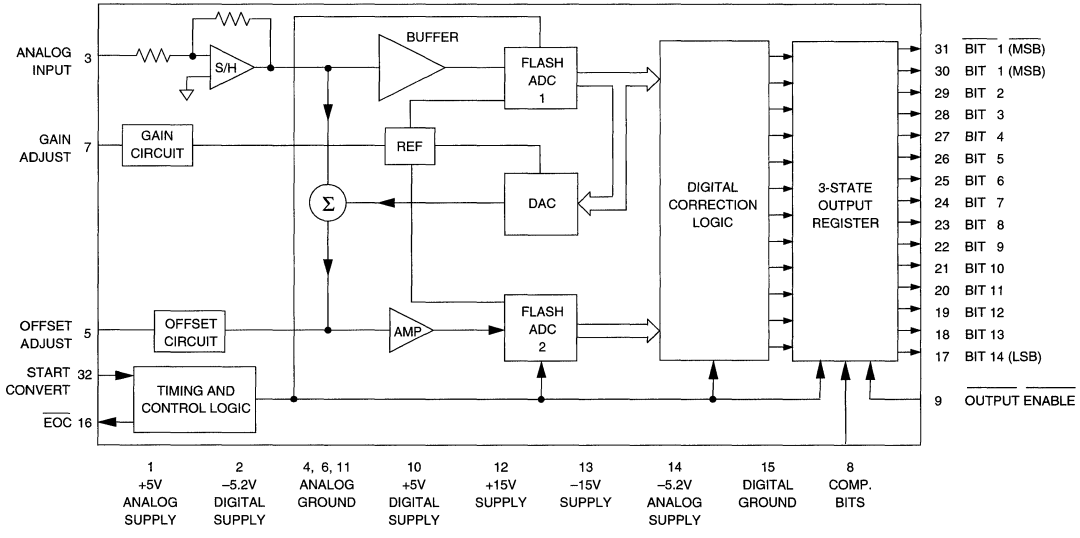


Figure 1. ADS-944 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	0 to +16	Volts
–15V Supply (Pin 13)	0 to –16	Volts
+5V Supply (Pins 1, 10)	0 to +6	Volts
–5.2V Supply (Pins 2, 14)	0 to –6	Volts
Digital Inputs (Pins 8, 9, 32)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 3)	–5 to +5	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-944MC	0	—	+70	°C
ADS-944MM/883	–55	—	+125	°C
Thermal Impedance				
θjc	—	7	—	°C/Watt
θca	—	21	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	32-pin, metal-sealed, ceramic TDIP or SMT			
Weight	0.46 ounces (13 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V, –V_{DD} = –5.2V, 5MHz sampling rate, and a minimum 3 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	—	±1.25	—	—	±1.25	—	—	±1.25	—	Volts
Input Resistance	500	550	—	500	550	—	500	550	—	Ω
Input Capacitance	—	6	15	—	6	15	—	6	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0" ②	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width③	40	80	—	40	80	—	40	80	—	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.75	—	—	±0.75	—	—	±1.0	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	–0.95	±0.5	+1.2	–0.95	±0.5	+1.2	–0.95	±0.5	+1.5	LSB
Full Scale Absolute Accuracy	—	±0.15	±0.4	—	±0.15	±0.4	—	±0.4	±0.8	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.1	±0.3	—	±0.1	±0.3	—	±0.3	±0.6	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.2	±0.4	—	±0.2	±0.4	—	±0.3	±0.9	%FSR
Gain Error (Tech Note 2)	—	±0.2	±0.4	—	±0.2	±0.4	—	±0.4	±1.5	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–85	–77	—	–85	–75	—	–81	–71	dB
100kHz to 1MHz	—	–78	–71	—	–78	–70	—	–75	–67	dB
1MHz to 2.5MHz	—	–75	–70	—	–75	–68	—	–71	–61	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–82	–76	—	–82	–74	—	–78	–70	dB
100kHz to 1MHz	—	–77	–70	—	–77	–70	—	–73	–65	dB
1MHz to 2.5MHz	—	–73	–68	—	–73	–65	—	–70	–60	dB
Signal–to–Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 100kHz	73	76	—	73	76	—	71	75	—	dB
100kHz to 1MHz	73	76	—	73	76	—	71	75	—	dB
1MHz to 2.5MHz	73	75	—	73	75	—	71	75	—	dB
Signal–to–Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 100kHz	71	75	—	71	75	—	68	73	—	dB
100kHz to 1MHz	70	73	—	69	73	—	65	71	—	dB
1MHz to 2.5MHz	68	71	—	66	71	—	62	69	—	dB
Noise	—	135	—	—	135	—	—	135	—	µVrms
Two–tone Intermodulation Distortion (f_{in} = 2.45MHz, 1.975MHz, f_s = 5MHz, –0.5dB)	—	–82	—	—	–82	—	—	–82	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	20	—	—	20	—	—	20	—	MHz
Large Signal (–0dB input)	—	13	—	—	13	—	—	13	—	MHz
Feedthrough Rejection (f_{in} = 2.5MHz)	—	90	—	—	90	—	—	90	—	dB
Slew Rate	—	±110	—	—	±110	—	—	±110	—	V/µs
Aperture Delay Time	—	±10	—	—	±10	—	—	±10	—	ns
Aperture Uncertainty	—	3	—	—	3	—	—	3	—	ps rms
S/H Acquisition Time										
(to ±0.003%FSR, 2.5V step)	—	85	90	—	85	90	—	85	90	ns
Overvoltage Recovery Time ⑤	—	200	—	—	200	—	—	200	—	ns
A/D Conversion Rate	5	—	—	5	—	—	5	—	—	MHz

DIGITAL OUTPUTS	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Delay, Edge of ENABLE to Output Data Valid/Invalid	—	—	10	—	—	10	—	—	10	ns
Output Coding	Offset Binary, Complementary Offset Binary, Two's Complement									
POWER REQUIREMENTS										
Power Supply Ranges ⑥										
+15V Supply	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	Volts
–15V Supply	–14.25	–15.0	–15.75	–14.25	–15.0	–15.75	–14.25	–15.0	–15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.9	+5.0	+5.25	Volts
–5.2V Supply	–4.95	–5.2	–5.45	–4.95	–5.2	–5.45	–5.1	–5.2	–5.45	Volts
Power Supply Currents ⑦										
+15V Supply	—	+36	+45	—	+36	+45	—	+36	+45	mA
–15V Supply	—	–55	–65	—	–55	–65	—	–55	–65	mA
+5V Supply	—	+155	+168	—	+155	+168	—	+155	+168	mA
–5.2V Supply	—	–167	–175	—	–167	–175	—	–167	–175	mA
Power Dissipation	—	2.95	3.3	—	2.95	3.3	—	2.95	3.3	Watts
Power Supply Rejection	—	—	±0.05	—	—	±0.05	—	—	±0.05	%FSR/%V

Footnotes:

① All power supplies should be on before applying a start convert pulse. All supplies and the clock (start convert pulses) must be present during warmup periods. The device must be continuously converting during this time.

② When COMP. BITS (pin 8) is low, logic loading "0" will be –350µA for this pin.

③ An 80ns wide start convert pulse is used for all production testing. The start convert pulse should be between 40 – 80ns or 130 – 160ns to ensure proper operation. The latter range could be used for those applications requiring less than a 5MHz sampling rate.

④ Effective bits is equal to:

$$\text{(SNR + Distortion)} - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}} \right]$$

$$6.02$$

⑤ This is the time required before the A/D output is valid after the analog input is back within its specified range.

⑥ The minimum supply voltages of +4.9V and –5.1V for $\pm V_{DD}$ are required for –55°C operation only. The minimum limits are +4.75V and –4.95V when operating at +125°C.

⑦ Typical +5V and –5.2V current drain breakdowns are as follows:

$+5V_{Analog}$	= +85mA	$-5.2V_{Analog}$	= –114mA
$+5V_{Digital}$	= +70mA	$-5.2V_{Digital}$	= –53mA
$+5V_{Total}$	= +155mA	$-5.2V_{Total}$	= –167mA

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-944 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems *are not* connected to each other internally. For optimal performance, tie all ground pins (4, 6, 11, and 15) directly to a large ***analog*** ground plane beneath the package. Bypass all power supplies to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. ***It is very important that the bypass capacitors be located as close to the unit as possible.*** Inductors or ferrite beads can also be used to improve the power supply filtering. Refer to Figure 4, the ADS-944 Evaluation Board Schematic, for more details.
2. The ADS-944 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. When using this circuitry, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.
3. Pin 8 (COMP. BITS) selects the ADS-944's digital output coding. When a logic "1" is applied to pin 8, the output coding is complementary offset binary. When pin 8 has a logic "0" applied, the output coding becomes offset binary. The MSB output (pin 31) may be used under these conditions to achieve two's complement coding. Pin 8 is TTL-compatible and can be driven with digital logic for those who want dynamic control of its function. There is an internal pull-up resistor on this pin, allowing pin 8 to be either connected to +5V or left open when a logic "1" is needed.
4. To enable the three-state outputs, apply a logic "0" (low) to OUTPUT ENABLE (pin 9). To disable, apply a logic "1" (high) to pin 9.
5. Applying a start convert pulse while a conversion is in progress (EOC = logic "1") initiates a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.
6. A passive bandpass filter is used at the input of the A/D for all production testing.
7. Though the ADS-944's digital outputs are capable of driving multiple LSTTL or HCT loads, we recommend the output bits and the EOC line each drive only a single gate. These gates should be located as close to the unit as possible. If they can not, 33Ω resistors placed in series with each output can aid in isolating pc run inductances. The ADS-944 digital outputs should not be connected directly to noisy digital busses.
8. Do not enable/disable or complement the output bits during the conversion process (from the falling edge of START CONVERT to the falling edge of EOC).

CALIBRATION PROCEDURE

(Refer to Figure 2 and Table 1)

Note: Connect pin 5 to ANALOG GROUND (pin 6) for operation without zero/offset adjustment. Connect pin 7 to ANALOG GROUND (pin 6) for operation without gain adjustment.

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit in Figure 2 are guaranteed to compensate for the ADS-944's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-944, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is $+^1/_2$LSB (+76.3µV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus $1^1/_2$ LSB's (+1.249771) .

Note: Due to inherent system noise, the averaging of several conversions may be needed to accurately adjust both offset and gain to 1LSB of accuracy.

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 32) so the converter is continuously converting.
2. Apply +76.3µV to the ANALOG INPUT (pin 3).
3. Adjust the offset potentiometer until the output bits are 10 0000 0000 0000 and the LSB flickers between 0 and 1 with pin 8 tied low (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied high (complementary offset binary).
4. Two's complement coding requires using $\overline{\text{BIT 1}}$ ($\overline{\text{MSB}}$) (pin 31). With pin 8 tied low, adjust the trimpot until the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

Gain Adjust Procedure

1. Apply +1.249771V to the ANALOG INPUT (pin 3).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0 with pin 8 tied low (offset binary) or until all bits are 0's and the LSB flickers between 1 and 0 with pin 8 tied high (complementary offset binary).
3. Two's complement coding requires using pin 31. With pin 8 tied low, adjust the gain trimpot until the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.
4. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 1.

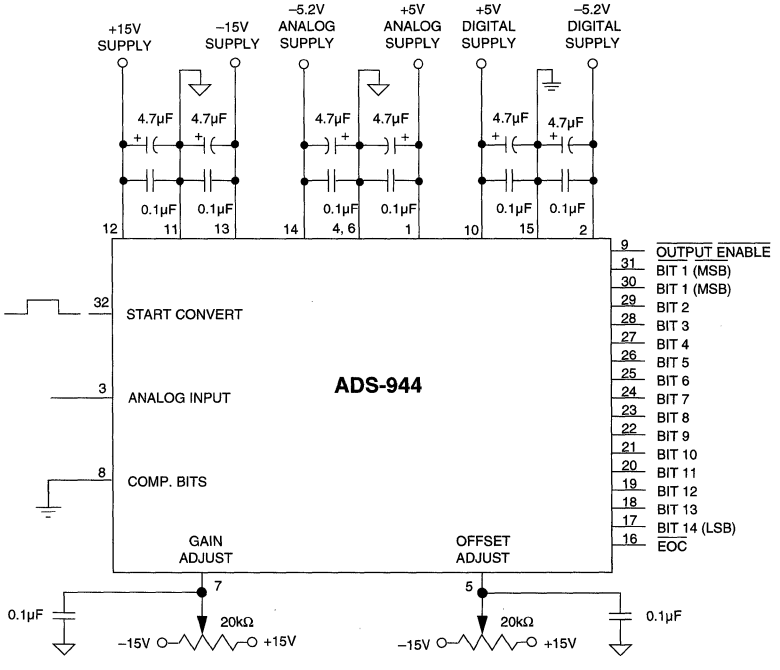
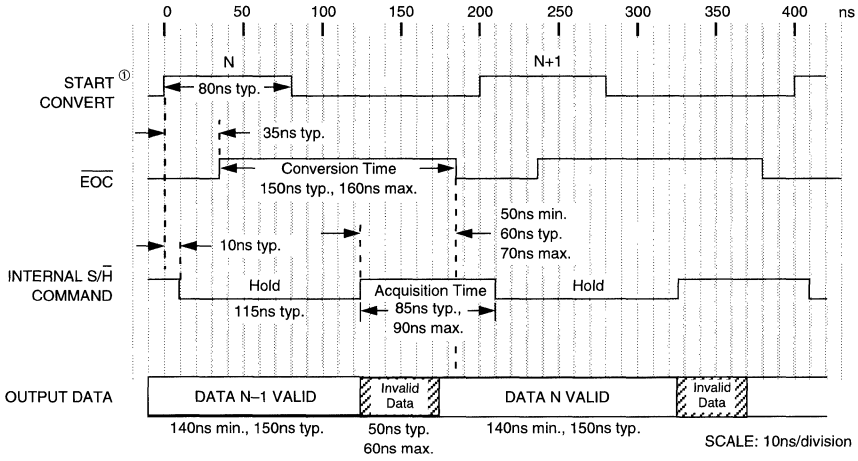


Figure 2. ADS-944 Connection Diagram



① START CONVERT pulse width: 40 to 80ns or 130 to 160ns

Figure 3. ADS-944 Timing Diagram

TIMING

The ADS-944 is an edge-triggered device. A conversion is initiated by the rising edge of the start convert pulse and no additional external timing signals are required. The device does not employ "pipeline" delays to increase its throughput rate. It does not require multiple start convert pulses to bring valid digital data to its output pins.

Approximately 10ns after the rising edge of the start convert signal, the ADS-944's internal sample-hold amplifier is driven into the hold mode by the internal S/H control line. After a 35ns delay to allow for S/H output transient settling, the conversion process begins, and the $\overline{EOC}$ line (pin 16) is driven high. The complete A/D conversion requires approximately 150ns. The falling of $\overline{EOC}$ signals that the conversion is now complete and digital output data is now valid.

This device actually guarantees that digital output data will be valid for 10ns prior to the falling edge of $\overline{EOC}$. Therefore, $\overline{EOC}$ can be used to latch data into external registers that have appropriate setup times. Any other available timing edges, including a delayed $\overline{EOC}$ or the rising edge of the next $\overline{EOC}$ pulse, can also be used for this purpose.

The falling edge of the start convert pulse, though irrelevant to device timing, can cause conversion errors if it occurs at certain times. Therefore, the recommended start convert pulse width is between 40 and 80ns or between 130 and 160ns. DATEL performs ADS-944 production testing at the full 5MHz sampling rate using 80ns start convert pulses.

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

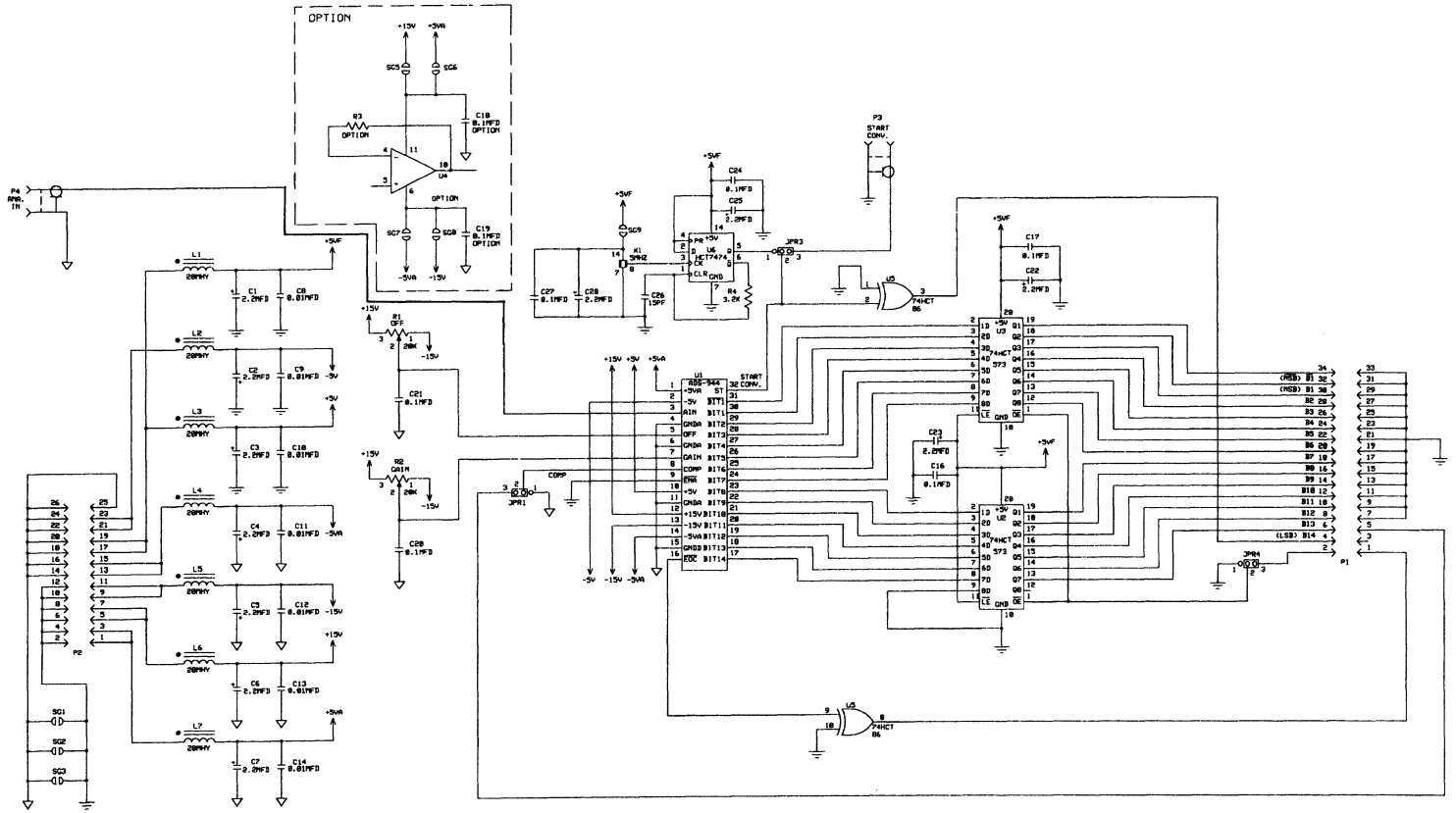
These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

Table 1. Output Coding

OUTPUT CODING						INPUT RANGE	BIPOLAR
MSB	LSB	MSB	LSB	$\overline{MSB}$	LSB	±1.25V	SCALE
11 1111 1111 1111		00 0000 0000 0000		01 1111 1111 1111		+1.249847	+FS -1 LSB
11 1000 0000 0000		00 0111 1111 1111		01 1000 0000 0000		+0.937500	+3/4 FS
11 0000 0000 0000		00 1111 1111 1111		01 0000 0000 0000		+0.625000	+1/2 FS
10 0000 0000 0000		01 1111 1111 1111		00 0000 0000 0000		0.000000	0
01 0000 0000 0000		10 1111 1111 1111		11 0000 0000 0000		–0.625000	–1/2 FS
00 1000 0000 0000		11 0111 1111 1111		10 1000 0000 0000		–0.937500	–3/4 FS
00 0000 0000 0001		11 1111 1111 1110		10 0000 0000 0001		–1.249847	–FS +1 LSB
00 0000 0000 0000		11 1111 1111 1111		10 0000 0000 0000		–1.250000	–FS
OFF. BINARY		COMP. OFF. BIN.		TWO'S COMP.			



NOTES
1. UNLESS OTHERWISE SPECIFIED
   ALL CAPACITORS ARE 50V
   C1 - C6 ARE 20V
   ALL RESISTORS ARE IN OHMS

Figure 4. ADS-944 Evaluation Board Schematic

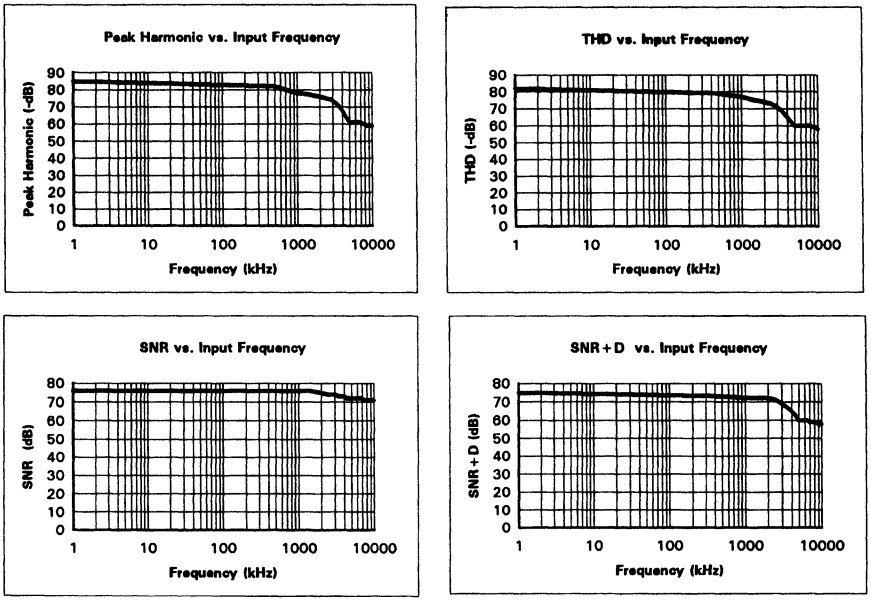


Figure 5. Typical ADS-944 Dynamic Performance vs. Input Frequency at +25°C

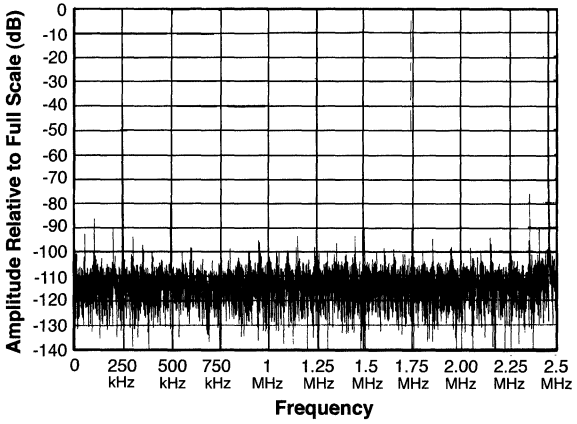


Figure 6. ADS-944 FFT
(f_{in} = 2.45MHz, f_S = 5MHz, V_{in} = –0.5dB, 16,384 points)

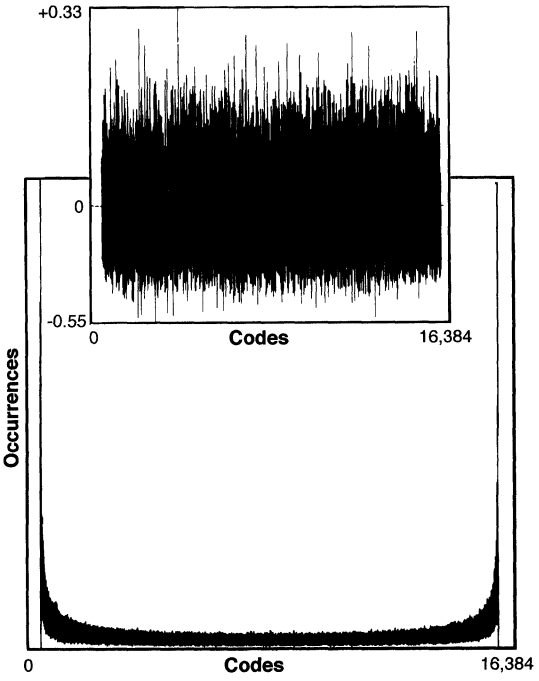
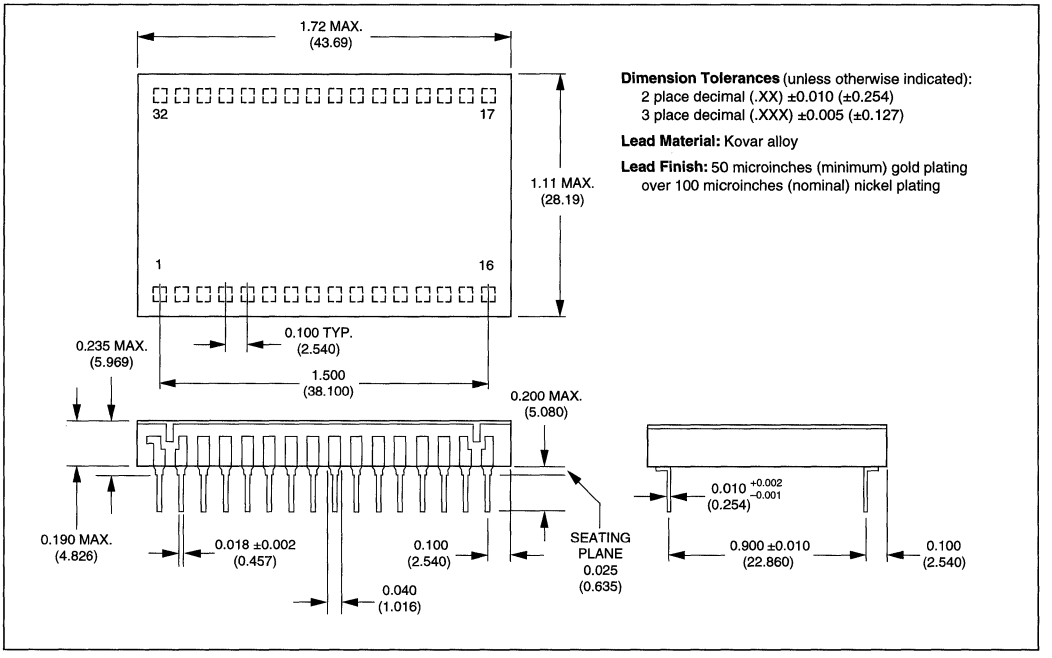


Figure 7. ADS-944 Histogram and Differential Nonlinearity

MECHANICAL DIMENSIONS
INCHES (mm)



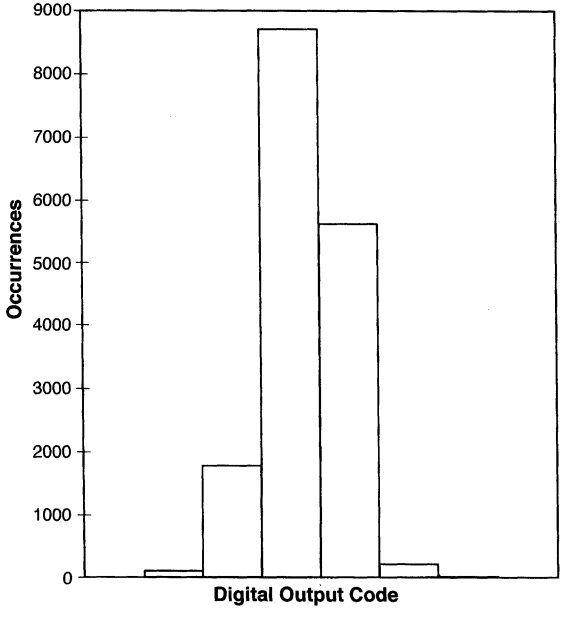


Figure 8. ADS-944 Grounded Input Histogram

This histogram represents the typical peak-to-peak noise (including quantization noise) associated with the ADS-944. 16,384 conversions were processed with the input to the ADS-944 tied to analog ground.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-944MC	0 to +70°C
ADS-944MM	–55 to +125°C
ADS-944/883	–55 to +125°C

Contact DATEL for availability of surface-mount (J-lead) packaging or for MIL-STD-883 or DESC SMD product specifications.

ACCESSORIES

ADS-B944	Evaluation Board (without ADS-944)
HS-32	Heat sink for ADS-944 DDIP models

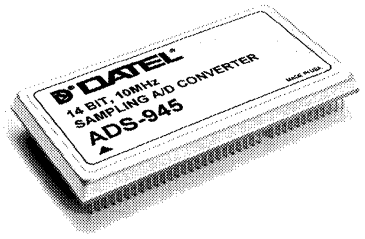
Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

DATEL®
INNOVATION and EXCELLENCE

ADS-945
14-Bit, 10MHz Sampling A/D Converters

FEATURES

- **14-Bit resolution**
- **10MHz minimum throughput**
- **Functionally complete**
- **No missing codes**
- **Low power, 4.2W**
- **Excellent dynamic performance**
- **Internally clamped input**
- **Edge triggered**
- **TTL compatible**
- **2" x 4" module**
- **Very low profile**



GENERAL DESCRIPTION

The low-cost ADS-945 is a high-performance, 14-bit, 10MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. The dynamic performance of the ADS-945 has been optimized to achieve a THD of –82dB and a SNR of 79dB.

Packaged in a 2" x 4" module, the functionally complete ADS-945 contains a fast-settling sample/hold amplifier, a subranging (two-pass) A/D converter, a precise voltage reference, timing/control logic, three-state outputs, and error-correction circuitry. Digital inputs and outputs are TTL compatible (except for pins 29 and 30 which are ECL).

Requiring ±15V, +5V and –5.2V supplies, the ADS-945 typically dissipates 4.2W. The unit is offered with a bipolar input range of ±1.25V. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. Typical applications include radar signal analysis, medical/graphic imaging, and FFT spectrum analysis.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1-3	ANALOG GROUND	70-76	ANALOG GROUND
4	ANALOG INPUT	69	+5V ANALOG SUPPLY
5-6	ANALOG GROUND	64-68	ANALOG GROUND
7	+10V REFERENCE OUT	63	–5.2V ANALOG SUPPLY
8	ANALOG GROUND	62	ANALOG GROUND
9	GAIN ADJUST	61	NO CONNECT
10-11	DO NOT CONNECT	58-60	DIGITAL GROUND
12	–15V SUPPLY	57	–5.2V DIGITAL SUPPLY
13	ANALOG GROUND	56	DO NOT CONNECT
14	+15V SUPPLY	55	+5V DIGITAL SUPPLY
15-17	ANALOG GROUND	54	DIGITAL GROUND
18	OFFSET ADJUST	53	BIT 1 (MSB)
19-25	ANALOG GROUND	52	BIT 2
26	MISSING PIN	51	BIT 3
27	DIGITAL GROUND	50	BIT 4
28	DIGITAL GROUND	49	BIT 5
29	T/H STATUS	48	BIT 6
30	T/$\overline{H}$ STATUS	47	BIT 7
31	DIGITAL GROUND	46	BIT 8
32	START CONVERT	45	BIT 9
33	$\overline{\text{OVERFLOW}}$	44	BIT 10
34	$\overline{\text{OUTPUT ENABLE}}$	43	BIT 11
35	DIGITAL GROUND	42	BIT 12
36	O.S. 3 *	41	BIT 13
37	DIGITAL GROUND	40	BIT 14 (LSB)
38	DIGITAL GROUND	39	DIGITAL GROUND

* Refer to Timing Diagram notes

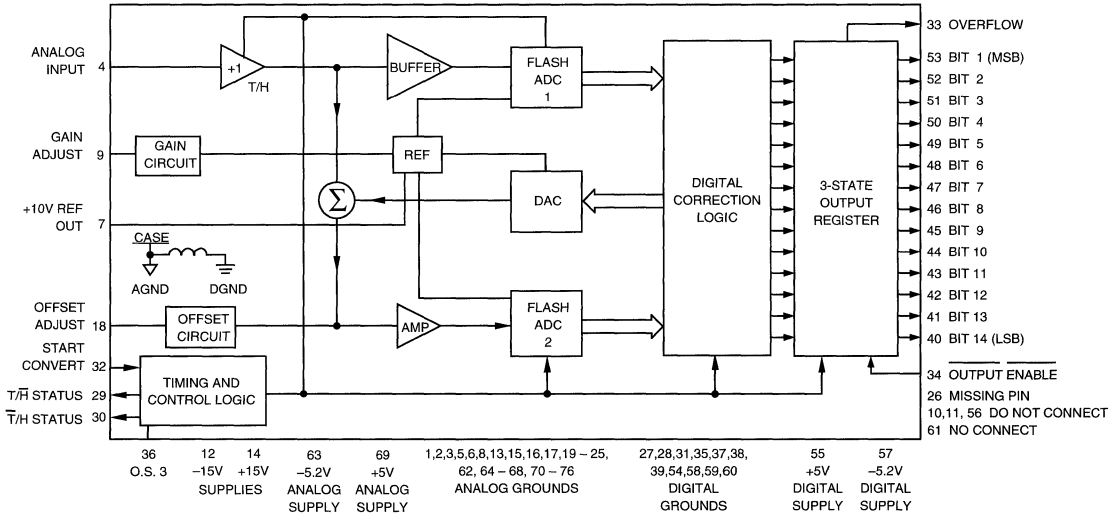


Figure 1. ADS-945 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 14)	0 to +17	Volts
–15V Supply (Pin 12)	0 to –17	Volts
+5V Supply (Pins 55, 69)	0 to +6	Volts
–5.2V Supply (Pins 57, 63)	0 to –6	Volts
Digital Inputs (Pins 32, 34)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 4)	–5 to +5	Volts
Lead Temperature (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-945	0	—	+70	°C
ADS-945EX	–55	—	+125	°C
Thermal Impedance				
θjc	—	2	—	°C/Watt
θca	—	8	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	2" x 4" module			
Weight	2.1 oz. (60 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V, –V_{DD} = –5.2V, 10MHz sampling rate, and a minimum 10 minute warmup① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Voltage Range ②	—	±1.25	—	—	±1.25	—	—	±1.25	—	Volts
Input Resistance	300	500	—	300	500	—	300	500	—	kΩ
Input Capacitance	—	10	15	—	10	15	—	10	15	pF
Input Bias Current	—	±3	—	—	±3	—	—	±3	—	µA
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width③	10	50	—	10	50	—	10	50	—	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.5	—	—	±0.75	—	—	±0.75	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.5	±0.75	—	±0.5	±0.75	–0.95	±0.75	+1.5	LSB
Full Scale Absolute Accuracy	—	±0.2	±0.4	—	±0.3	±0.5	—	±0.3	±0.7	%FSR
Bipolar Offset Error (Tech Note 2)	—	±0.15	±0.25	—	±0.25	±0.5	—	±0.3	±0.7	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.2	—	±0.2	±0.4	—	±0.3	±0.7	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 1MHz	—	–86	–78	—	–86	–78	—	–80	–72	dB
1MHz to 2.5MHz	—	–82	–75	—	–82	–75	—	–79	–70	dB
2.5MHz to 5MHz	—	–79	–74	—	–79	–74	—	–78	–70	dB
Total Harmonic Distortion (–0.5dB)										
dc to 1MHz	—	–82	–76	—	–82	–76	—	–78	–70	dB
1MHz to 2.5MHz	—	–80	–74	—	–80	–74	—	–76	–68	dB
2.5MHz to 5MHz	—	–78	–73	—	–78	–73	—	–76	–68	dB
Signal-to-Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 1MHz	76	79	—	76	79	—	70	78	—	dB
1MHz to 2.5MHz	76	78	—	76	78	—	70	77	—	dB
2.5MHz to 5MHz	75	77	—	75	77	—	70	75	—	dB
Signal-to-Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 1MHz	73	77	—	73	77	—	67	74	—	dB
1MHz to 2.5MHz	72	76	—	72	76	—	67	74	—	dB
2.5MHz to 5MHz	71	74	—	71	74	—	66	72	—	dB
Noise	—	110	—	—	110	—	—	110	—	µVrms
Two-tone Intermodulation Distortion (f_{in} = 1.975MHz, 2.45MHz, fs=10MHz, –0.5dB)	—	–84	—	—	–84	—	—	–84	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	100	—	—	100	—	—	100	—	MHz
Large Signal (–0dB input)	—	50	—	—	50	—	—	50	—	MHz
Feedthrough Rejection (f_{in} = 4.85MHz)	—	90	—	—	90	—	—	90	—	dB
Slew Rate	—	±850	—	—	±850	—	—	±850	—	V/µs
Aperture Delay Time	—	+8	—	—	+8	—	—	+8	—	ns
Aperture Uncertainty	—	2	—	—	2	—	—	2	—	ps rms
S/H Acquisition Time										
(to ±0.003%FSR, 2.5V step)	—	40	—	—	40	—	—	40	—	ns
Overvoltage Recovery Time ⑤	—	30	100	—	30	100	—	30	100	ns
A/D Sampling Rate	10	—	—	10	—	—	10	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	−55 to +125°C MIN.	−55 to +125°C TYP.	−55 to +125°C MAX.	UNITS
Reference Output	+9.99	+10	+10.01	+9.99	+10	+10.01	+9.99	+10	+10.01	Volts
Reference Temperature Drift	—	±40	—	—	±40	—	—	±40	—	ppm/°C
Reference Load Current	—	—	2.0	—	—	2.0	—	—	2.0	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.7	—	—	+2.7	—	—	+2.7	—	—	Volts
Logic "0"	—	—	+0.5	—	—	+0.5	—	—	+0.5	Volts
Logic Loading "1"	—	—	−0.4	—	—	−0.4	—	—	−0.4	mA
Logic Loading "0"	—	—	+8	—	—	+8	—	—	+8	mA
Delay, Falling Edge of T/H to Output Data Valid	—	55	—	—	55	—	—	55	—	ns
Delay, Edge of ENABLE to Output Data Valid/Invalid	—	18	—	—	18	—	—	18	—	ns
Output Coding	Complementary Offset Binary									
POWER REQUIREMENTS										
Power Supply Ranges										
+15V Supply	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	Volts
−15V Supply	−14.25	−15.0	−15.75	−14.25	−15.0	−15.75	−14.25	−15.0	−15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
−5.2V Supply	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	Volts
Power Supply Currents ⑥										
+15V Supply	—	+35	+45	—	+35	+45	—	+35	+45	mA
−15V Supply	—	−55	−65	—	−55	−65	—	−55	−65	mA
+5V Supply	—	+140	+160	—	+140	+160	—	+140	+160	mA
−5.2V Supply	—	−430	−460	—	−430	−460	—	−430	−460	mA
Power Dissipation	—	4.2	4.5	—	4.2	4.5	—	4.2	4.5	Watts
Power Supply Rejection	—	—	±0.04	—	—	±0.04	—	—	±0.04	%FSR/%V

Footnotes:

① All power supplies should be on before applying a start convert pulse. All supplies and the clock (start convert pulses) must be present during warmup periods. The device must be continuously converting during this period.

② The input to the ADS-945 is internally clamped at ±2.3V.

③ A 50ns wide start convert pulse is used for all production testing. For applications requiring less than a 10MHz sampling rate, a wider start convert pulse can be used.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output is valid once the analog input is back within the specified range.

⑥ Typical +5V and −5.2V current drain breakdowns are as follows:

$+5V_{Analog}$	=	+100mA	$-5.2V_{Analog}$	=	−210mA
$+5V_{Digital}$	=	+40mA	$-5.2V_{Digital}$	=	−220mA
$+5V_{Total}$	=	+140mA	$-5.2V_{Total}$	=	−430mA

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-945 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems *are* connected to each other internally. For optimal performance, tie all ground pins directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies to ground with 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. ***The bypass capacitors should be located as close to the unit as possible.***

2. The ADS-945 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figure 2. The typical adjustment range is ±0.2%FSR for this circuitry.

   When using this circuitry, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. To enable the three-state outputs, apply a logic "0" (low) to OUTPUT ENABLE (pin 34). To disable, apply a logic "1" (high) to pin 34.

4. A passive bandpass filter (Allen Avionics F4202 Series) is used at the input of the A/D for all production testing.

5. The ADS-945's digital outputs should not be directly connected to a noisy data bus. Drive the bus with 573 or 574 type latches and use "low-noise" logic, such as the 74LS series.

CALIBRATION PROCEDURE

(Refer to Figure 2 and Table 1)

Note: Connect pin 18 to ANALOG GROUND (pin 19) for operation without zero/offset adjustment. Connect pin 9 to ANALOG GROUND (pin 8) for operation without gain adjustment.

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit in Figure 2 are guaranteed to compensate for the ADS-945's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-945, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+76.3µV).

Gain adjusting is accomplished when all bits are 0's and the LSB just changes from a 0 to a 1. This transition ideally occurs when the analog input is at +full scale minus 1 1/2LSB's (+1.249771V) .

Note: Due to inherent system noise, the averaging of several conversions may be needed to accurately adjust both offset and gain to 1LSB of accuracy.

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 32) so the converter is continuously converting.
2. Apply +76.3µV to the ANALOG INPUT (pin 4).
3. Adjust the offset potentiometer until the output bits are 10 0000 0000 0000 and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +1.249771V to the ANALOG INPUT (pin 4).
2. Adjust the gain potentiometer until all output bits are 0's and the LSB flickers between 0 and 1.
3. To confirm proper operation of the device, vary the applied input voltage to obtain the output coding listed in Table 1.

Note: A single +5V supply can be used for both the +5V ANALOG and the +5V DIGITAL. If separate supplies are used, the difference between the two can not exceed 100mV. This also applies to the –5.2V supply requirements.

Datel recommends using ferrite beads to separate the analog and digital supplies (FAIR-RITE # 2643000301.)

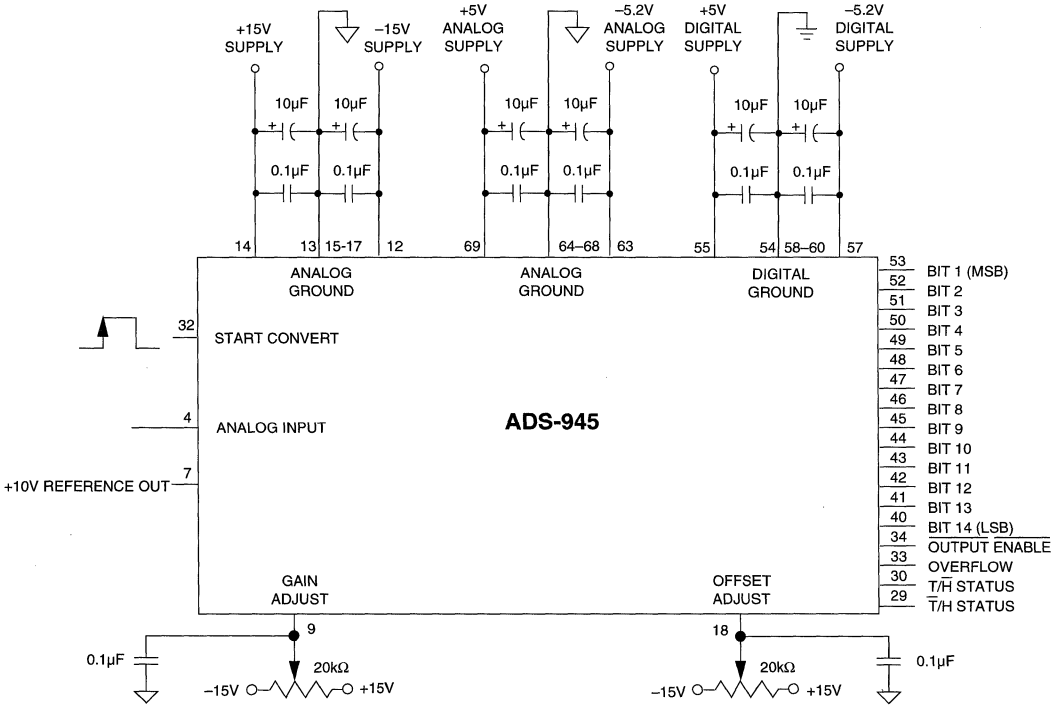


Figure 2. ADS-945 Connection Diagram

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For Immediate Assistance 800-233-2765

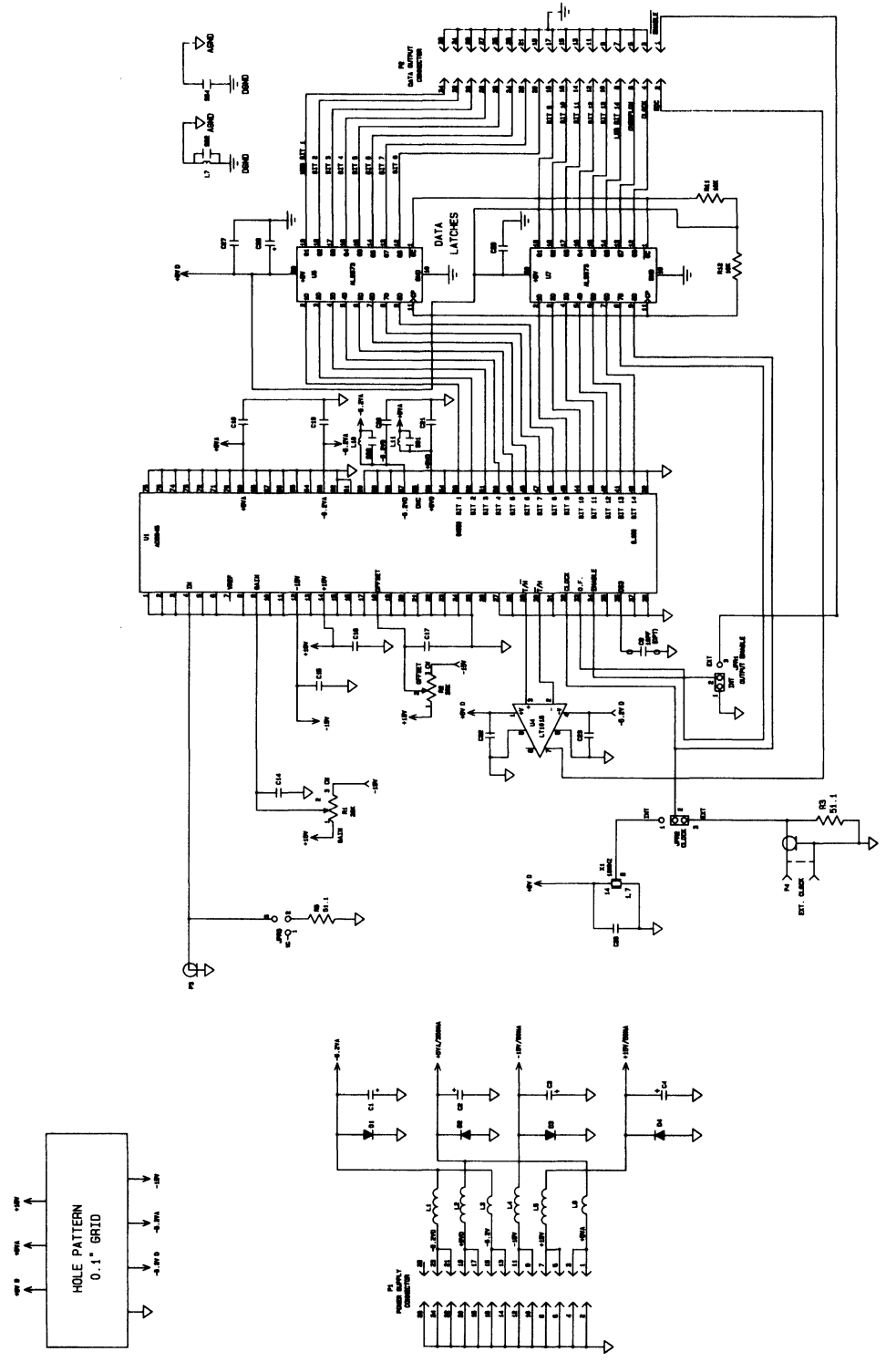
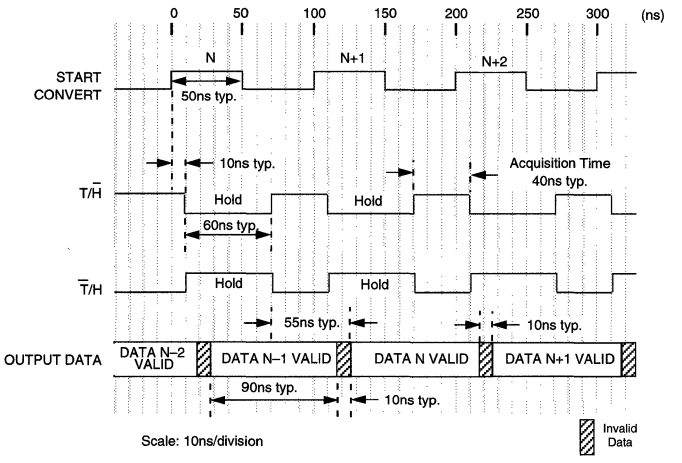


Figure 3. ADS-945 Evaluation Board Schematic (DATEL Dwg. # A-23442)



Timing Notes:

1. The ADS-945 is an edge-triggered device requiring no additional external timing signals. The rising edge of the start convert pulse initiates a conversion.
2. A start convert pulse of 50ns is recommended when sampling at 10MHz.
3. The falling edge of the subsequent start convert pulse (N+1) or the rising edge of the N+2 pulse can be used to latch data from conversion N (1 pipeline delay).
4. For a sampling rate of 10MHz, do not connect pin 36.
5. For sampling rates between 7.75 and 8.25MHz, place a 22pF capacitor to digital ground on pin 36.

Figure 4. ADS-945 Timing Diagram

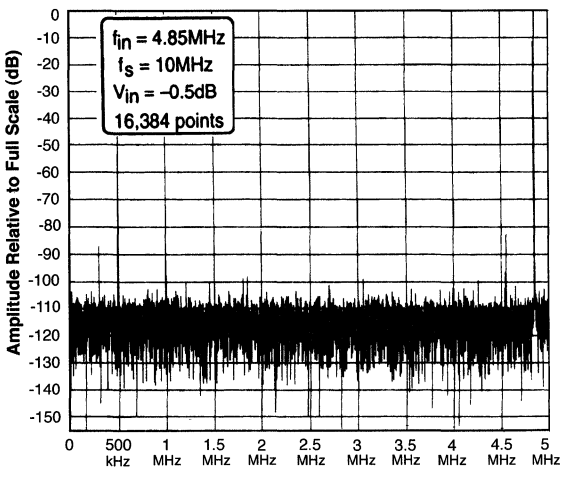


Figure 5. ADS-945 FFT Analysis

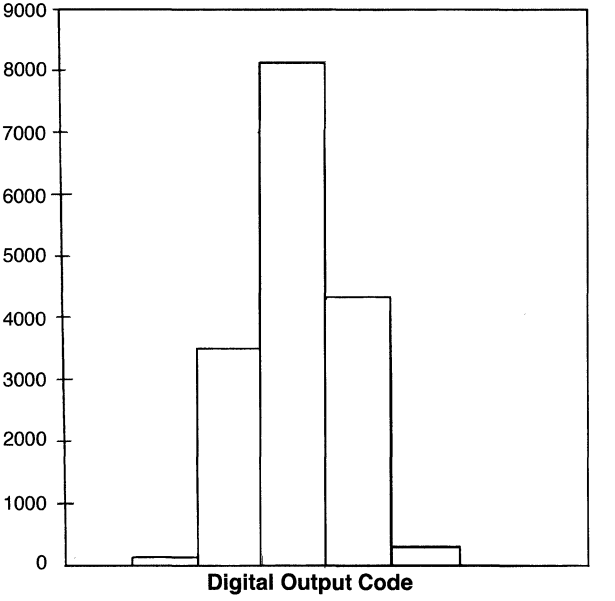


Figure 6. ADS-945 Grounded Input Histogram

This histogram represents the typical peak-to-peak noise (including quantization noise) associated with the ADS-945. 16,384 conversions were processed with the input to the ADS-945 tied to analog ground.

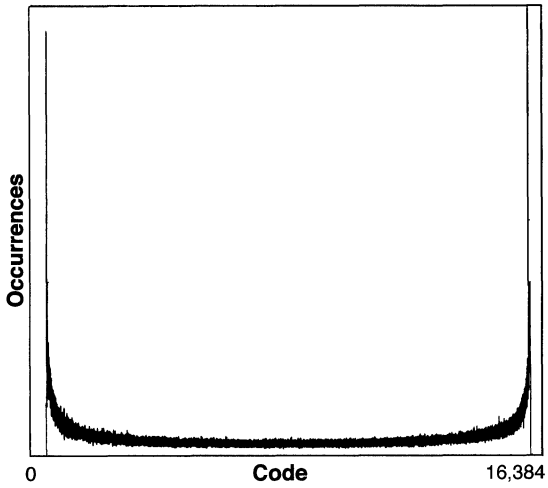


Figure 7. ADS-945 Histogram

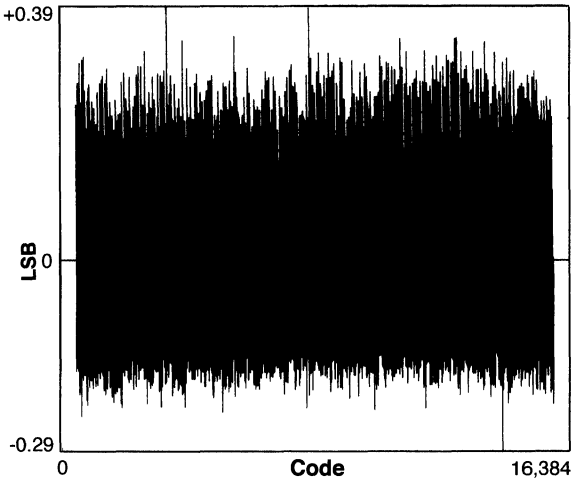


Figure 8. ADS-945 Differential Nonlinearity

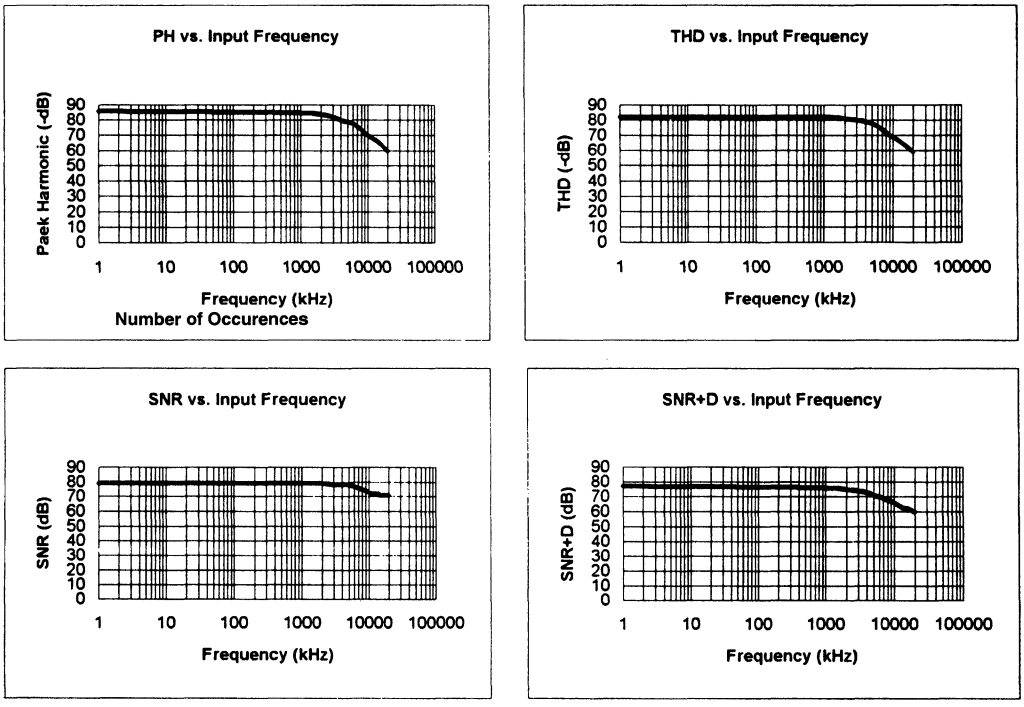


Figure 9. ADS-945 Dynamic Performance vs. Input Frequency at +25°C

MECHANICAL DIMENSIONS
INCHES (mm)

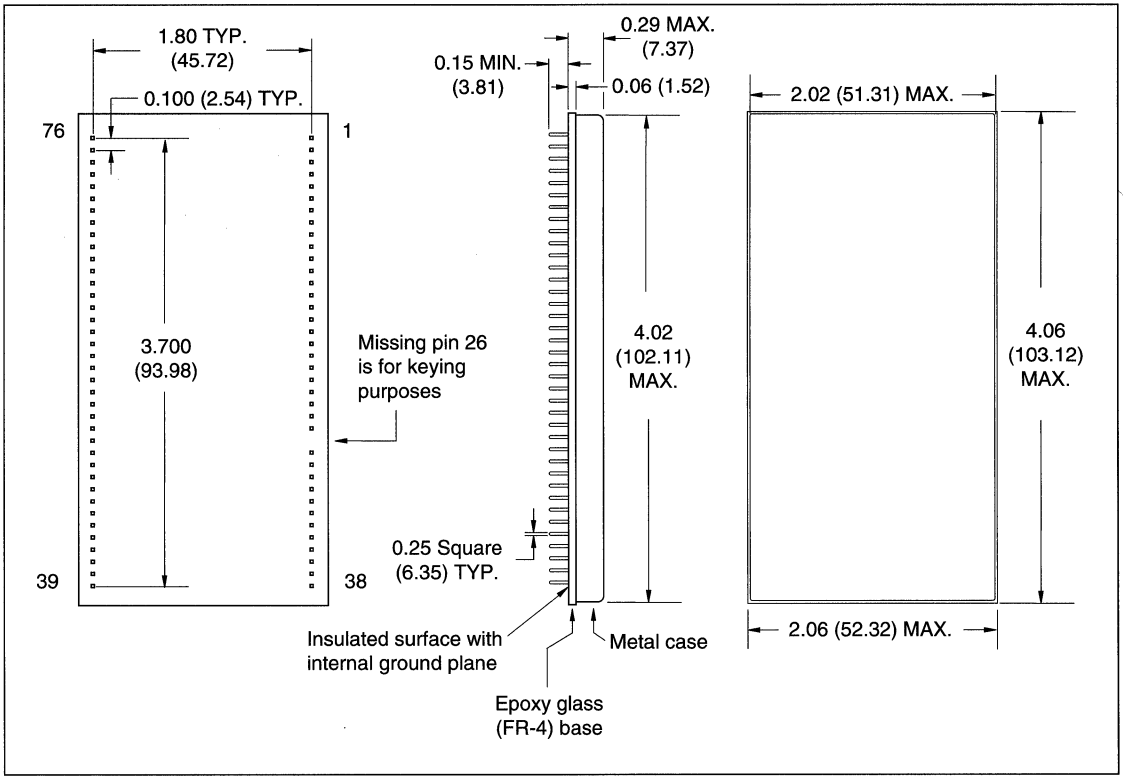


Table 1. Output Coding

OUTPUT CODING MSB LSB	INPUT RANGE ±1.25V	BIPOLAR SCALE
00 0000 0000 0000	+1.249847	+FS -1 LSB
00 1000 0000 0000	+0.937500	+3/4 FS
01 0000 0000 0000	+0.625000	+1/2 FS
10 0000 0000 0000	0.000000	0
11 0000 0000 0000	–0.625000	–1/2 FS
11 1000 0000 0000	–0.937500	–3/4 FS
11 1111 1111 1110	–1.249847	–FS +1 LSB
11 1111 1111 1111	–1.250000	–FS

COMP. OFF. BINARY

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-945	0 to +70°C
ADS-945EX	–55 to +125°C
ACCESSORIES	
ADS-B945	Evaluation Board (without ADS-945)

Socket strips for PC board mounting can be ordered through SAMTEC, their SSW and SSQ series (0.025" square socket strips). Receptacles (75 required) can be ordered through MILL-MAX (P/N 0330-0-15-01-47-27-10-0).

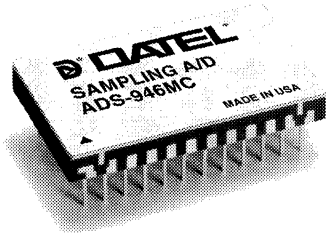
DATEL®
INNOVATION and EXCELLENCE

PRELIMINARY PRODUCT DATA

ADS-946
14-Bit, 8MHz Sampling A/D Converters

FEATURES

- **14-Bit resolution**
- **8MHz minimum sampling rate**
- **No missing codes over full military temperature range**
- **Ideal for both time and frequency-domain applications**
- **Excellent THD (–81dB) and SNR (76dB)**
- **Edge-triggered, no pipeline delays**
- **Small, 24-pin, ceramic DDIP or SMT**
- **Requires only ±5V supplies**
- **Low-power, 1.9 Watts**
- **Low cost**



GENERAL DESCRIPTION

The low-cost ADS-946 is a 14-bit, 8MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. Excellent differential nonlinearity error (DNL), signal-to-noise ratio (SNR), and total harmonic distortion (THD) make the ADS-946 the ideal choice for both time-domain (CCD/FPA imaging, scanners, process control) and frequency-domain (radar, telecommunications, spectrum analysis) applications .

The functionally complete ADS-946 contains a fast-settling sample/hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL. The ADS-946 only requires the rising edge of a start convert pulse to operate.

Requiring only ±5V supplies, the ADS-946 typically dissipates just 1.9 Watts. The device is offered with a bipolar input range of ±2V. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. A proprietary, auto-calibrating, error-correcting circuit allows the device to achieve specified performance over the full military temperature range.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	24	ANALOG GROUND
2	BIT 2	23	OFFSET ADJUST
3	BIT 3	22	+5V ANALOG SUPPLY
4	BIT 4	21	ANALOG INPUT
5	BIT 5	20	–5V SUPPLY
6	BIT 6	19	ANALOG GROUND
7	BIT 7	18	START CONVERT
8	BIT 8	17	$\overline{\text{EOC}}$
9	BIT 9	16	BIT 14 (LSB)
10	BIT 10	15	BIT 13
11	BIT 11	14	DIGITAL GROUND
12	BIT 12	13	+5V DIGITAL SUPPLY

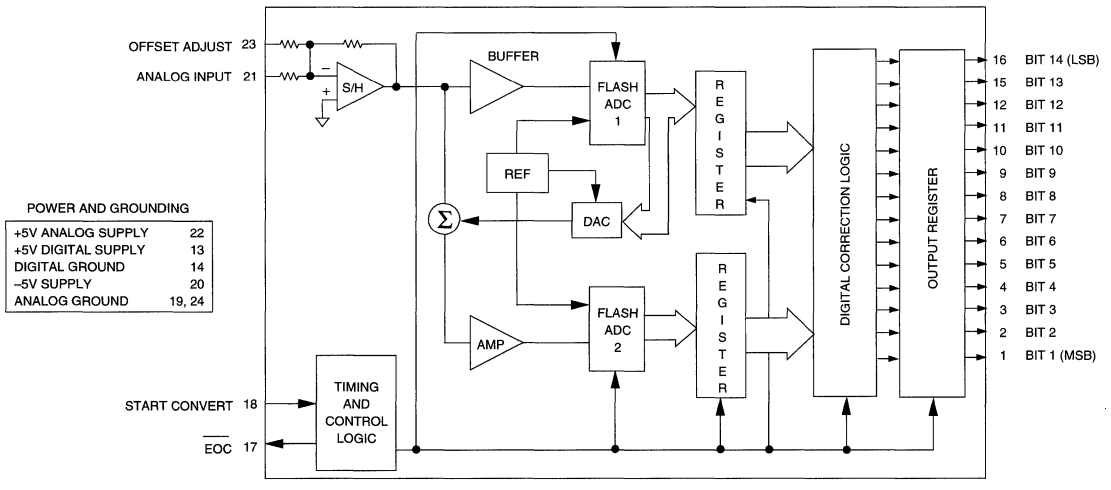


Figure 1. ADS-946 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Supply (Pins 13, 22)	0 to +6	Volts
–5V Supply (Pin 20)	0 to –6	Volts
Digital Input (Pin 18)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 21)	±5	Volts
Lead Temperature (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-946MC	0	—	+70	°C
ADS-946MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	6	—	°C/Watt
θca	—	23	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP or SMT			
Weight	0.46 ounces (13 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{DD} = ±5V, 8MHz sampling rate, and a minimum 3 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	±2	—	—	±2	—	—	±2	—	Volts
Input Resistance	—	200	—	—	200	—	—	200	—	Ω
Input Capacitance	—	6	15	—	6	15	—	6	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2	—	—	+2	—	—	+2	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	20	—	—	20	—	—	20	—	ns
STATIC PERFORMANCE										
Resolution	—	14	—	—	14	—	—	14	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.75	—	—	±0.75	—	—	±1	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	–0.95	±0.5	+1.25	–0.95	±0.5	+1.25	–0.95	±0.5	+1.5	LSB
Full Scale Absolute Accuracy	—	±0.15	±0.4	—	±0.15	±0.4	—	±0.4	±0.8	%FSR
Bipolar Zero Error (Tech Note 2)	—	±0.1	±0.3	—	±0.1	±0.3	—	±0.3	±0.6	%FSR
Gain Error (Tech Note 2)	—	±0.2	±0.4	—	±0.2	±1.4	—	±0.4	±1.5	%
No Missing Codes (f_{in} = 10kHz)	14	—	—	14	—	—	14	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 500kHz	—	–83	–76	—	–83	–75	—	–79	–71	dB
500kHz to 1MHz	—	–78	–72	—	–78	–72	—	–73	–68	dB
1MHz to 4MHz	—	–76	–71	—	–76	–71	—	–71	–65	dB
Total Harmonic Distortion (–0.5dB)										
dc to 500kHz	—	–81	–74	—	–81	–74	—	–77	–70	dB
500kHz to 1MHz	—	–76	–71	—	–76	–71	—	–72	–66	dB
1MHz to 4MHz	—	–74	–69	—	–74	–69	—	–69	–63	dB
Signal-to-Noise Ratio (w/o distortion, –0.5dB)										
dc to 500kHz	73	76	—	73	76	—	71	75	—	dB
500kHz to 1MHz	73	76	—	73	76	—	71	75	—	dB
1MHz to 4MHz	72	75	—	72	75	—	71	75	—	dB
Signal-to-Noise Ratio ④ (& distortion, –0.5dB)										
dc to 500kHz	70	74	—	70	74	—	68	73	—	dB
500kHz to 1MHz	70	74	—	70	74	—	66	71	—	dB
1MHz to 4MHz	69	73	—	69	73	—	65	70	—	dB
Noise	—	150	—	—	150	—	—	150	—	µVrms
Two-tone Intermodulation Distortion (f_{in} = 2.45MHz, 1.975MHz, f_s = 8MHz, –0.5dB)	—	–82	—	—	–82	—	—	–82	—	dB
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	30	—	—	30	—	—	30	—	MHz
Large Signal (–0dB input)	—	10	—	—	10	—	—	10	—	MHz
Feedthrough Rejection (f_{in} = 4MHz)	—	85	—	—	85	—	—	85	—	dB
Slew Rate	—	±400	—	—	±400	—	—	±400	—	V/µs
Aperture Delay Time	—	+5	—	—	+5	—	—	+5	—	ns
Aperture Uncertainty	—	2	—	—	2	—	—	2	—	ps rms
S/H Acquisition Time (to ±0.003%FSR, 4V step)	—	55	60	—	55	60	—	55	60	ns
Overvoltage Recovery Time ⑤	—	100	125	—	100	125	—	100	125	ns
A/D Conversion Rate	8	—	—	8	—	—	8	—	—	MHz

DIGITAL OUTPUTS	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Output Coding	Offset Binary									
POWER REQUIREMENTS										
Power Supply Ranges ⑥										
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.9	+5.0	+5.25	Volts
–5V Supply	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	–4.9	–5.0	–5.25	Volts
Power Supply Currents										
+5V Supply	—	+220	+270	—	+220	+270	—	+220	+280	mA
–5V Supply	—	–120	–160	—	–120	–160	—	–120	–160	mA
Power Dissipation	—	1.9	2.1	—	1.9	2.1	—	1.9	2.1	Watts
Power Supply Rejection	—	—	±0.1	—	—	±0.1	—	—	±0.1	%FSR/%V

Footnotes:

1. All power supplies should be on before applying a start convert pulse. All supplies and the clock (start convert pulses) must be present during warmup periods. The device must be continuously converting during this time.
2. Contact DATEL for other input voltage ranges.
3. A 20ns wide start convert pulse is used for all production testing. For applications requiring less than an 8MHz sampling rate, a wider start convert pulse can be used.
4. Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

5. This is the time required before the A/D output data is valid once the analog input is back within the specified range. This time is only guaranteed if the input does not exceed ±2.2V.
6. The minimum supply voltages of +4.9V and –4.9V for $\pm V_{DD}$ are required for –55°C operation only. The minimum limits are +4.75V and –4.75V when operating at +125°C.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-946 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19 and 24) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-946 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figures 2 and 3.

   When using this circuitry, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. Applying a start convert pulse while a conversion is in progress (EOC = logic "1") will initiate a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

4. A passive bandpass filter is used at the input of the A/D for all production testing.

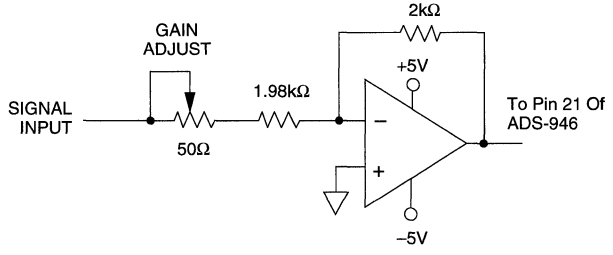


Figure 2. Optional ADS-946 Gain Adjust Calibration Circuit

CALIBRATION PROCEDURE

(Refer to Figures 2 and 3 and Tables 1 and 2)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuits in Figures 2 and 3 are guaranteed to compensate for the ADS-946's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

Offset adjusting for the ADS-946 is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+122µV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+1.99963V).

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 18) so the converter is continuously converting.
2. Apply +122µV to the ANALOG INPUT (pin 21).
3. Adjust the offset potentiometer until the output bits are 1000 0000 00000 and the LSB flickers between 0 and 1.

Table 1. Gain and Zero Adjust

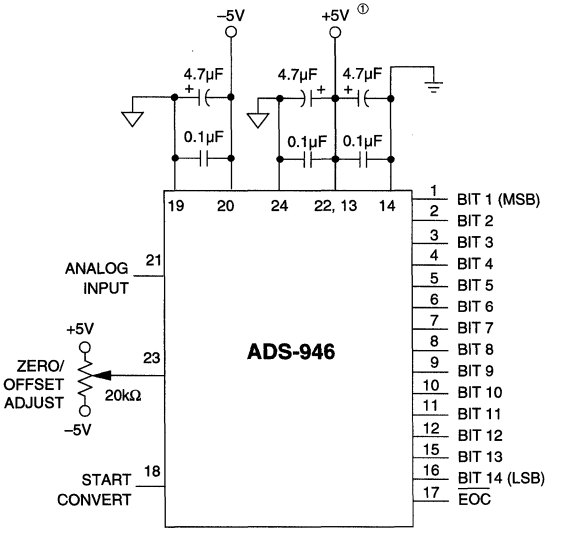
INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS–1 1/2 LSB
±2V	+122µV	+1.99963V

Gain Adjust Procedure

1. Apply +1.99963V to the ANALOG INPUT (pin 21).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.
3. To confirm proper operation of the device, vary the input signal to obtain the output coding listed in Table 2.

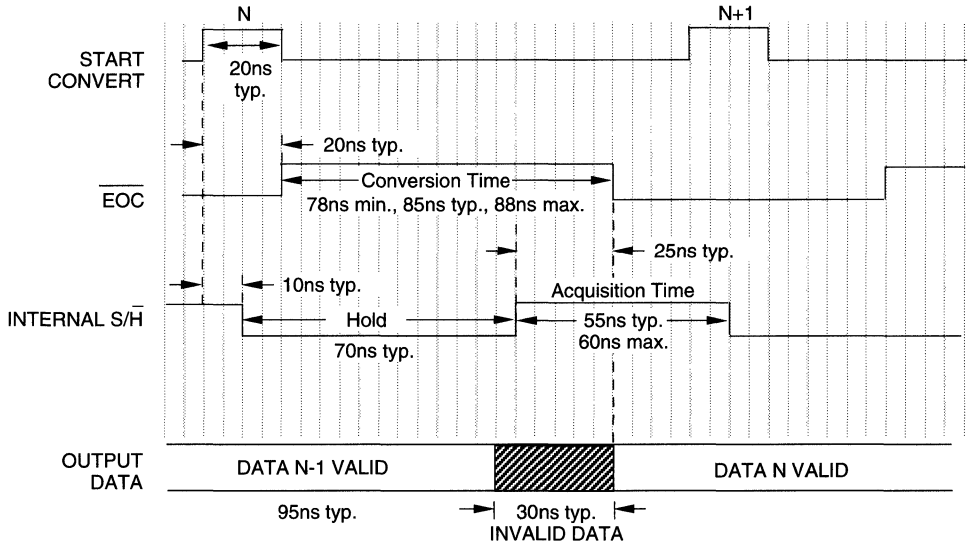
Table 2. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT VOLTAGE (±2V RANGE)	OFFSET BINARY MSB LSB
+FS –1 LSB	+1.99976	11 1111 1111 1111
+3/4 FS	+1.50000	11 1000 0000 0000
+1/2 FS	+1.00000	11 0000 0000 0000
0	0.00000	10 0000 0000 0000
–1/2 FS	–1.00000	01 0000 0000 0000
–3/4 FS	–1.50000	00 1000 0000 0000
–FS +1 LSB	–1.99976	00 0000 0000 0001
–FS	–2.00000	00 0000 0000 0000



① A single +5V supply should be used for both the +5V analog and +5V digital. If separate supplies are used, the difference between the two cannot exceed 100mV.

Figure 3. ADS-946 Connection Diagram



Notes:
1. Scale is approximately 5ns per division. Sampling rate = 8MHz
2. The start convert pulse must be between 20 and 50ns wide or between 80 and 110ns wide when sampling at 8MHz.

Figure 4. ADS-946 Timing Diagram

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to +125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

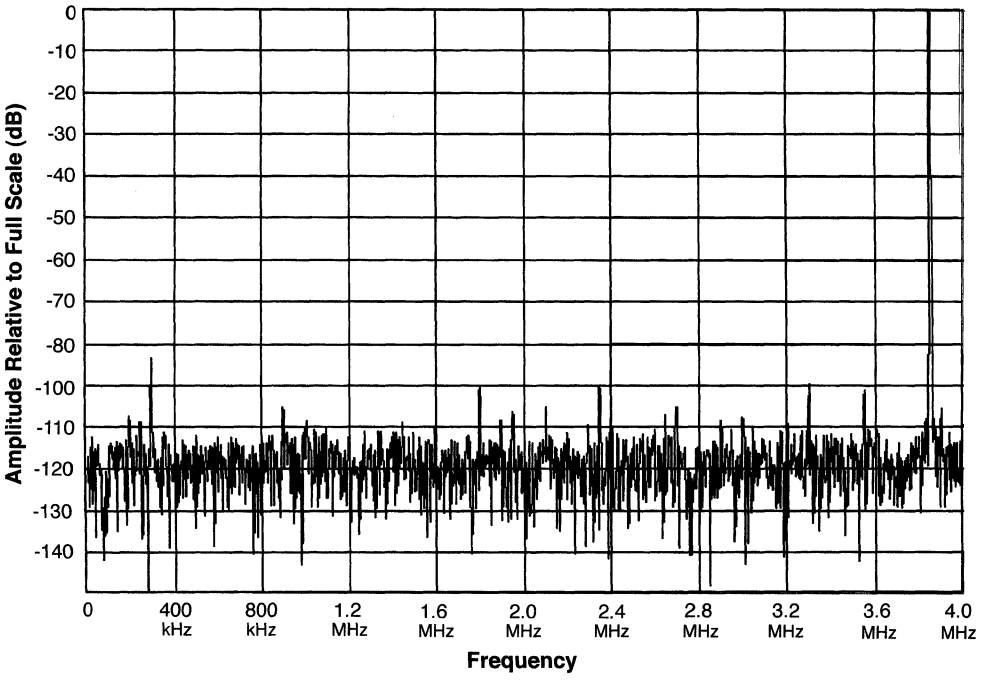


Figure 5. FFT Analysis of ADS-946
(f_S = 8MHz, f_{IN} = 3.85MHz, V_{IN} = –0.5dB, 16,384-point FFT)

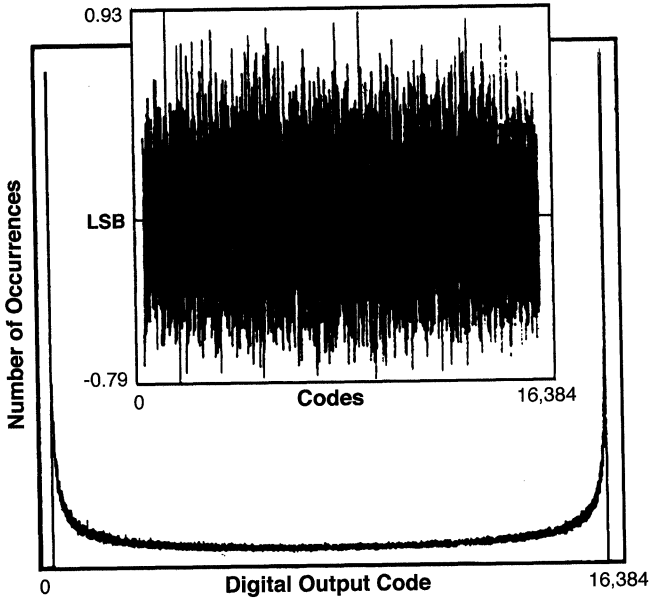


Figure 6. ADS-946 Histogram and Differential Nonlinearity

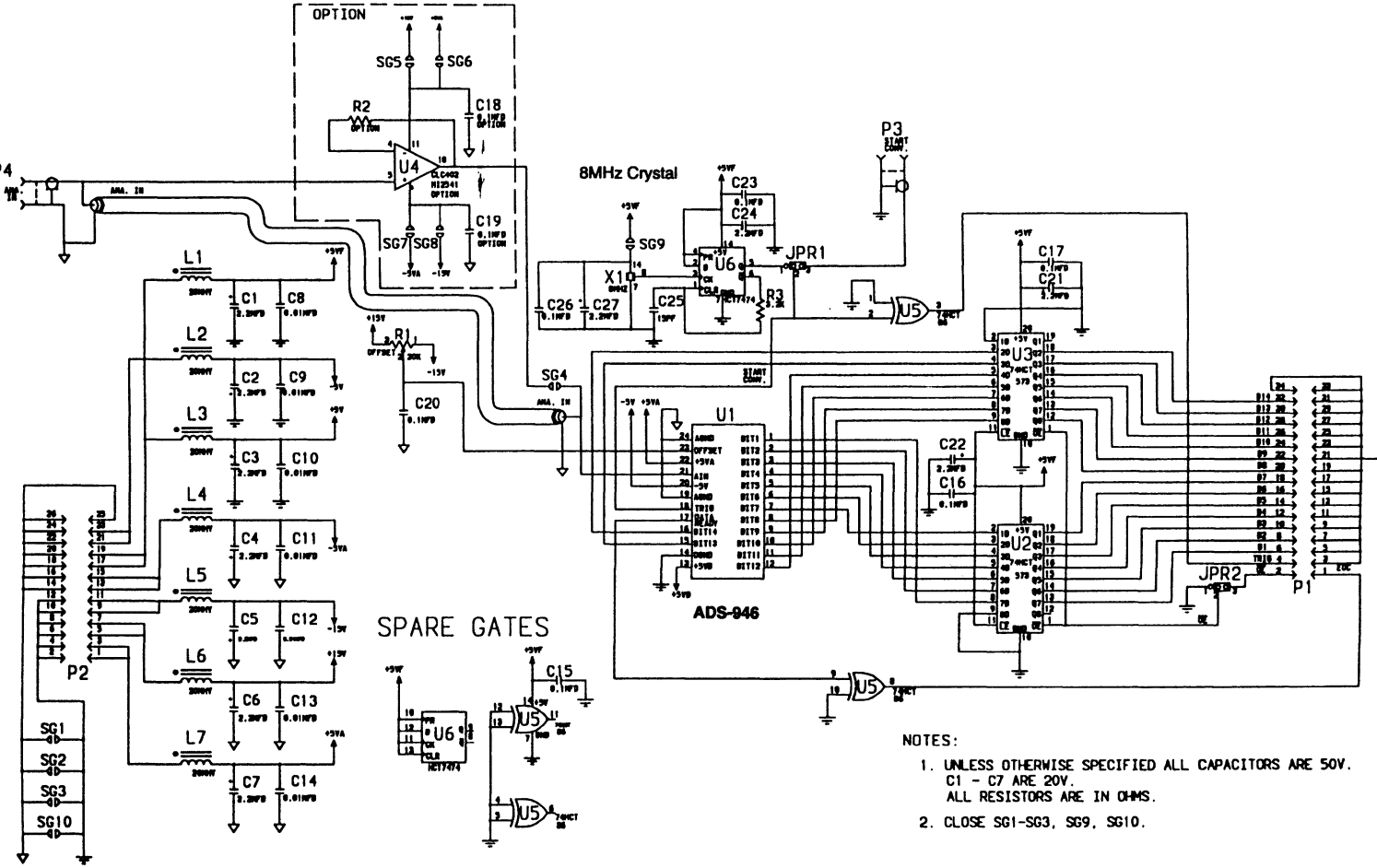
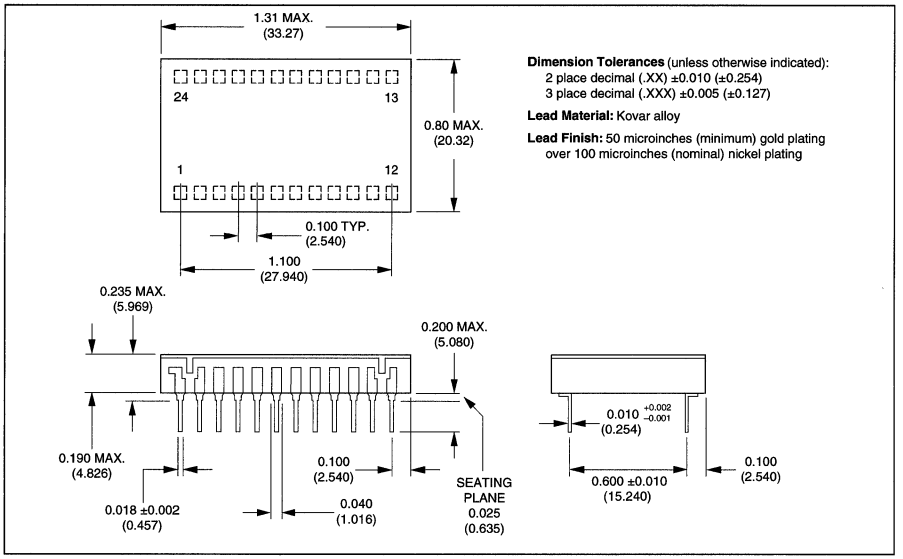


Figure 5. ADS-946 Evaluation Board Schematic (ADS-B946)

MECHANICAL DIMENSIONS
INCHES (mm)

24-Pin DDIP Versions

ADS-946MC
ADS-946MM

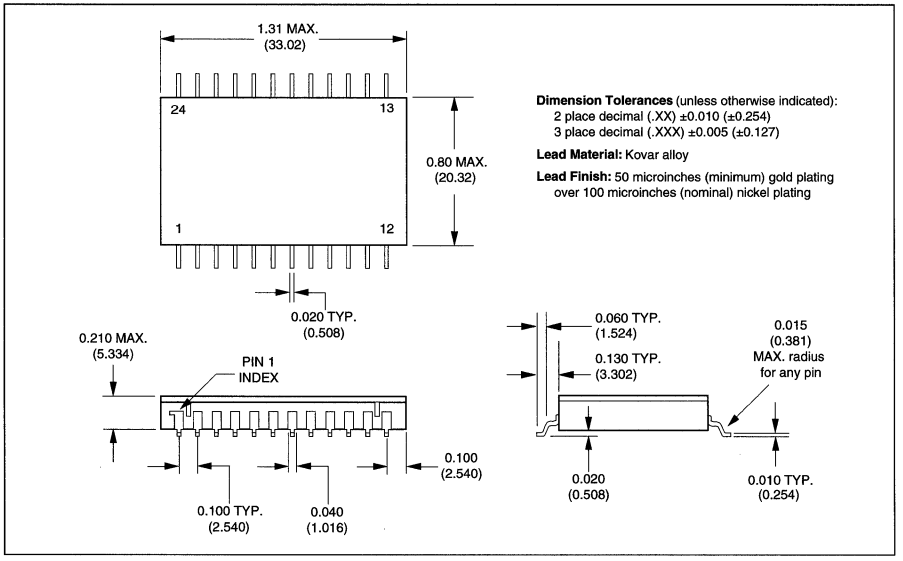


Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

24-Pin Surface Mount Version



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-946MC	0 to +70°C	Bipolar (±2V)
ADS-946MM	–55 to +125°C	Bipolar (±2V)

ACCESSORIES

ADS-B946	Evaluation Board (without ADS-946)
HS-24	Heat Sink for all ADS-946 models

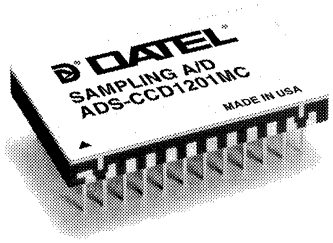
Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product, or surface mount packaging, contact DATEL.

DATEL®
INNOVATION and EXCELLENCE

ADS-CCD1201
12-Bit, 1.2MHz, Sampling A/D's Optimized for CCD Applications

FEATURES

- **Unipolar input range (0 to +10V)**
- **1.2MHz sampling rate**
- **4096-to-1 dynamic range (72.2dB)**
- **Low noise, 400µVrms (1/6 of an LSB)**
- **Outstanding differential nonlinearity error (±0.35 LSB max.)**
- **Small, 24-pin ceramic DDIP**
- **Low power, 1.7 Watts**
- **Operates from ±12V or ±15V supplies**
- **Edge-triggered, no pipeline delay**



GENERAL DESCRIPTION

The functionally complete, easy-to-use ADS-CCD1201 is a 12-bit, 1.2MHz Sampling A/D Converter whose performance and production testing have been optimized for use in electronic imaging applications, particularly those employing charge coupled devices (CCD's) as their photodetectors. The ADS-CCD1201 delivers the lowest noise (400µVrms) and the best differential nonlinearity error (±0.35LSB max.) of any commercially available 12-bit A/D in its speed class. It can respond to full scale input steps (from empty to full well) with less than a single count of error, and its input is immune to overvoltages that may occur due to blooming.

Packaged in an industry-standard, 24-pin, ceramic DDIP, the ADS-CCD1201 requires ±15V (or ±12V) and +5V supplies and typically consumes 1.7 (1.4) Watts. The device is 100% production tested for all critical performance parameters and is fully specified over both the 0 to +70°C and –55 to +125°C operating temperature ranges.

For those applications using correlated double sampling, the ADS-CCD1201 can be supplied without its internal sample-hold amplifier. DATEL will also entertain discussions about including the CDS circuit internal to the ADS-CCD1201. Please contact us for more details.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	24	–12V/–15V SUPPLY
2	BIT 11	23	GROUND
3	BIT 10	22	+12V/+15V SUPPLY
4	BIT 9	21	+10V REFERENCE OUT
5	BIT 8	20	ANALOG INPUT
6	BIT 7	19	GROUND
7	BIT 6	18	NO CONNECT
8	BIT 5	17	NO CONNECT
9	BIT 4	16	START CONVERT
10	BIT 3	15	$\overline{\text{EOC}}$
11	BIT 2	14	GROUND
12	BIT 1 (MSB)	13	+5V SUPPLY

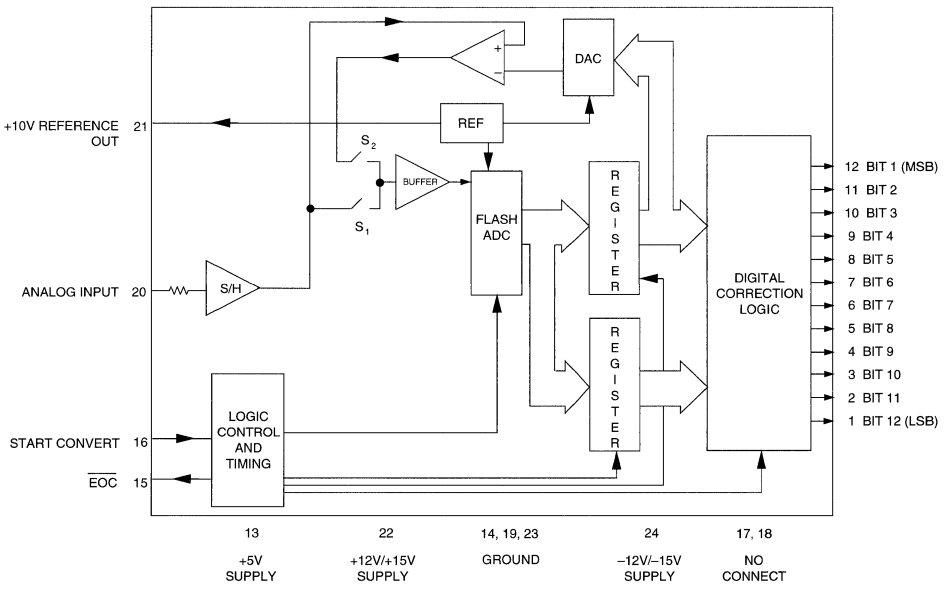


Figure 1. ADS-CCD1201 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+12V/+15V Supply (Pin 22)	0 to +16	Volts
–12V/–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to $+V_{DD}$ +0.3	Volts
Analog Input (Pin 20)	–4 to +17	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–CCD1201MC	0	—	+70	°C
ADS–CCD1201MM	–55	—	+125	°C
Thermal Impedance				
θjc		5		°C/Watt
θca		24		°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, $\pm V_{CC}$ = ±15V (or ±12V), $+V_{DD}$ = +5V, 1.2MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	0 to +10	—	—	0 to +10	—	—	0 to +10	—	Volts
Input Resistance	—	1	—	—	1	—	—	1	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	50	100	—	50	100	—	50	100	—	ns
STATIC PERFORMANCE										
Resolution	—	12	—	—	12	—	—	12	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.5	—	—	±0.5	—	—	±1	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.25	±0.35	—	±0.25	±0.35	—	±0.35	±0.75	LSB
Full Scale Absolute Accuracy	—	±0.1	±0.3	—	±0.2	±0.5	—	±0.3	±0.5	%FSR
Offset Error (Tech Note 2)	—	±0.05	±0.15	—	±0.1	±0.15	—	±0.15	±0.4	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.3	—	±0.2	±0.5	—	±0.3	±0.5	%
No Missing Codes (f_{in} = 10kHz)	12	—	—	12	—	—	12	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–86	–80	—	–86	–80	—	–82	–76	dB
100kHz to 500kHz	—	–84	–78	—	–84	–78	—	–81	–75	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–84	–79	—	–84	–79	—	–77	–71	dB
100kHz to 500kHz	—	–82	–77	—	–82	–77	—	–76	–70	dB
Signal–to–Noise Ratio (w/o distortion, –0.5dB)										
dc to 100kHz	72	73	—	72	73	—	70	72	—	dB
100kHz to 500kHz	71	72	—	71	72	—	70	72	—	dB
Signal–to–Noise Ratio ④ (& distortion, –0.5dB)										
dc to 100kHz	71	73	—	71	73	—	68	71	—	dB
100kHz to 500kHz	71	72	—	71	72	—	68	71	—	dB
Two–tone Intermodulation Distortion (f_{in} = 100kHz, 240kHz, f_s = 1.2MHz, –0.5dB)	—	–85	—	—	–84	—	—	–83	—	dB
Noise	—	400	—	—	500	—	—	700	—	µVrms
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	7.5	—	—	7.5	—	—	7.5	—	MHz
Large Signal (–0.5dB input)	—	6	—	—	6	—	—	6	—	MHz
Feedthrough Rejection (f_{in} = 500kHz)	—	84	—	—	84	—	—	84	—	dB
Slew Rate	—	±60	—	—	±60	—	—	±60	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.01%FSR, 10V step)	360	400	440	360	400	440	360	400	440	ns
Overvoltage Recovery Time ⑤	—	400	833	—	400	833	—	400	833	ns
A/D Conversion Rate	1.2	—	—	1.2	—	—	1.2	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	−55 to +125°C MIN.	−55 to +125°C TYP.	−55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/°C
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	−4	—	—	−4	—	—	−4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Delay, Falling Edge of EOC to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Straight Binary									
POWER REQUIREMENTS, ±15V										
Power Supply Range										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
−15V Supply	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+15V Supply	—	+50	+65	—	+50	+65	—	+50	+65	mA
−15V Supply	—	−40	−50	—	−40	−50	—	−40	−50	mA
+5V Supply	—	+70	+85	—	+70	+85	—	+70	+85	mA
Power Dissipation	—	1.7	1.9	—	1.7	1.9	—	1.7	1.9	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V
POWER REQUIREMENTS, ±12V										
Power Supply Range										
+12V Supply	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	Volts
−12V Supply	−11.5	−12.0	−12.5	−11.5	−12.0	−12.5	−11.5	−12.0	−12.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+12V Supply	—	+50	+65	—	+50	+65	—	+50	+65	mA
−12V Supply	—	−40	−48	—	−40	−48	—	−40	−48	mA
+5V Supply	—	+70	+80	—	+70	+80	—	+70	+80	mA
Power Dissipation	—	1.4	1.6	—	1.4	1.6	—	1.4	1.6	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② Contact DATEL for availability of other input voltage ranges.

③ A 100ns wide start convert pulse is used for all production testing.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-CCD1201 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies, as well as the REFERENCE OUTPUT (pin 21), to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-CCD1201 as possible.

2. The ADS-CCD1201 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. When operating the ADS-CCD1201 from ±12V supplies, do not drive external circuitry with the REFERENCE OUTPUT (pin 21). The reference's accuracy and drift specifications may not be met, and loading the circuit may cause accuracy errors within the converter.

4. A passive bandpass filter is used at the input of the A/D for all production testing.

5. Applying a start pulse while a conversion is in progress (EOC = logic "1") initiates a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

Table 1. Zero and Gain Adjust

INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V	+1.2207mV	+9.99634V

CALIBRATION PROCEDURE

(Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit of Figure 2 are guaranteed to compensate for the ADS-CCD1201's initial accuracy errors and may not be able to compensate for additional system errors.

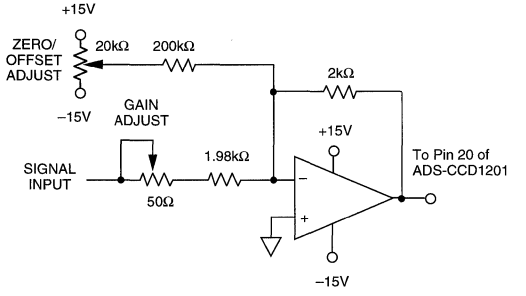


Figure 2. ADS-CCD1201 Calibration Circuit

All fixed resistors in Figure 2 should be metal-film types, and multi-turn potentiometers should have TCR's of 100ppm/°C or less to minimize drift with temperature. In many applications, the CCD will require an offset-adjust (black balance) circuit near its output and also a gain stage, presumably with adjust capabilities, to match the output voltage of the CCD to the input range of the A/D. If one is performing a "system I/O calibration" (from light in to digital out), these circuits can be used to compensate for the relatively small initial offset and gain errors of the A/D. This would elliminate the need for the circuit shown in Figure 2.

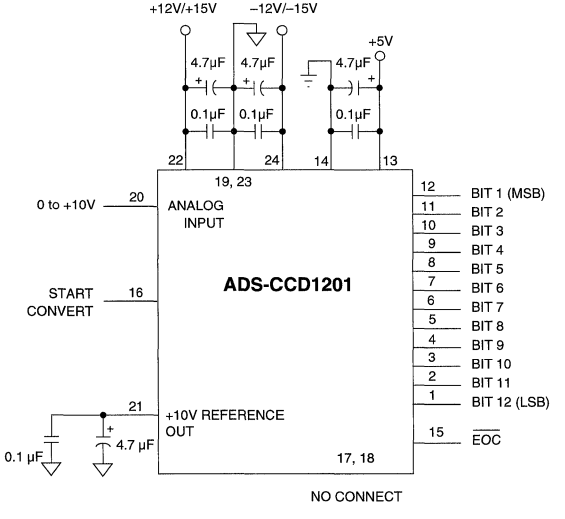


Figure 3. Typical ADS-CCD1201 Connection Diagram

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-CCD1201, offset adjusting is normally accomplished at the point where all output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+1.2207mV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+9.99634V) .

Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +1.2207mV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are 0000 0000 00000 and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +9.99634V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.

Table 2. ADS-CCD1201 Output Coding

INPUT VOLTAGE (0 to +10V)	UNIPOLAR SCALE	DIGITAL OUTPUT MSB LSB
+9.9976	+FS –1LSB	1111 1111 1111
+7.5000	+3/4 FS	1100 0000 0000
+5.0000	+1/2 FS	1000 0000 0000
+2.5000	+1/4 FS	0100 0000 0000
+0.0024	+1LSB	0000 0000 0001
0	0	0000 0000 0000

Coding is straight binary; 1LSB = 2.44mV

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

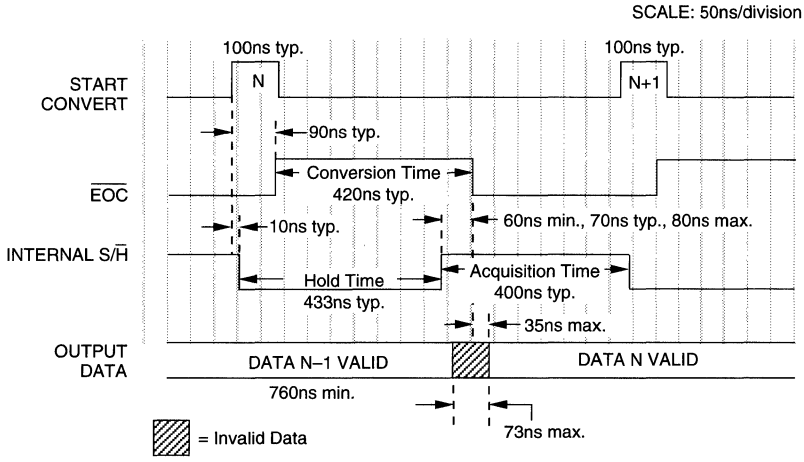


Figure 4. ADS-CCD1201 Timing Diagram

TIMING

The ADS-CCD1201 is an edge-triggered device. A conversion is initiated by the rising edge of the start convert pulse and no additional external timing signals are required. The device does not employ "pipeline" delays to increase its throughput rate. It does not require multiple start convert pulses to bring valid digital data to its output pins.

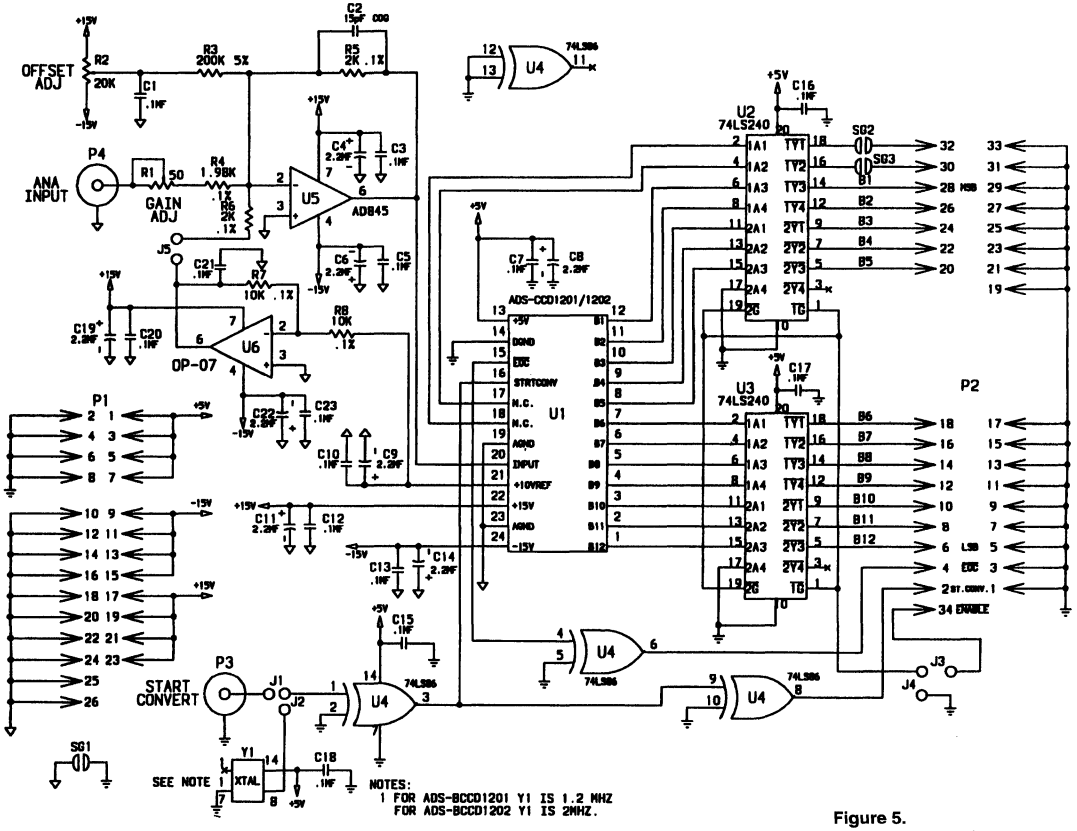


Figure 5.
ADS-CCD1201 Evaluation Board Schematic

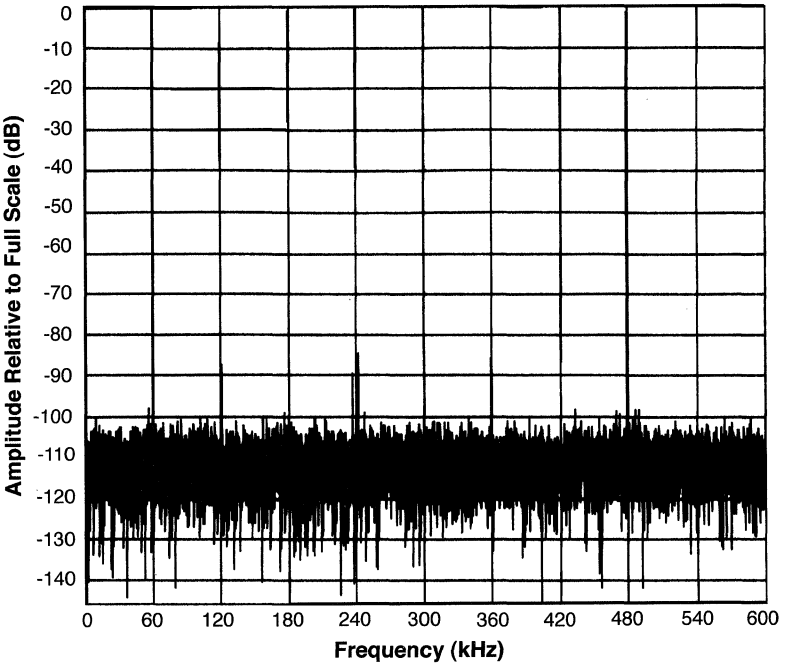


Figure 6. ADS-CCD1201 FFT
(f_{in} = 480kHz, f_S = 1.2MHz, V_{in} = –0.5dB, 16,384 points)

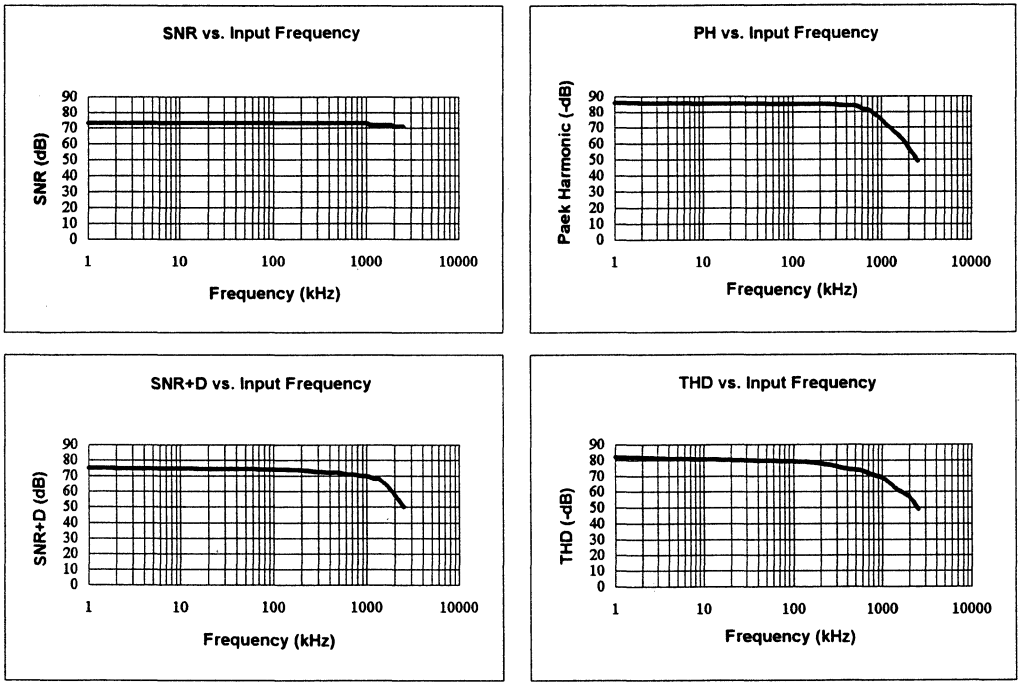
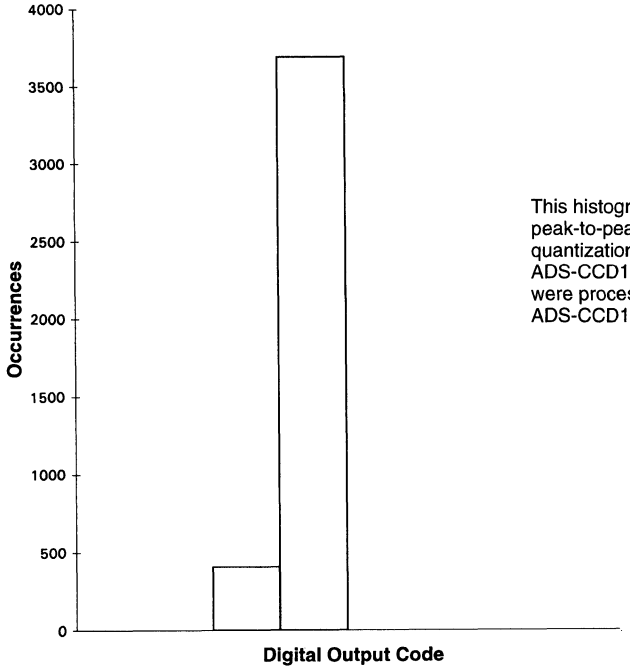


Figure 7. Typical ADS-CCD1201 Dynamic Performance vs. Input Frequency at +25°C
(V_{in} = –0.5dB, f_S = 1.2MHz)



This histogram represents the typical peak-to-peak noise (including quantization noise) associated with the ADS-CCD1201. 4,096 conversions were processed with the input to the ADS-CCD1201 tied to analog ground.

Figure 8. ADS-CCD1201 Grounded Input Histogram

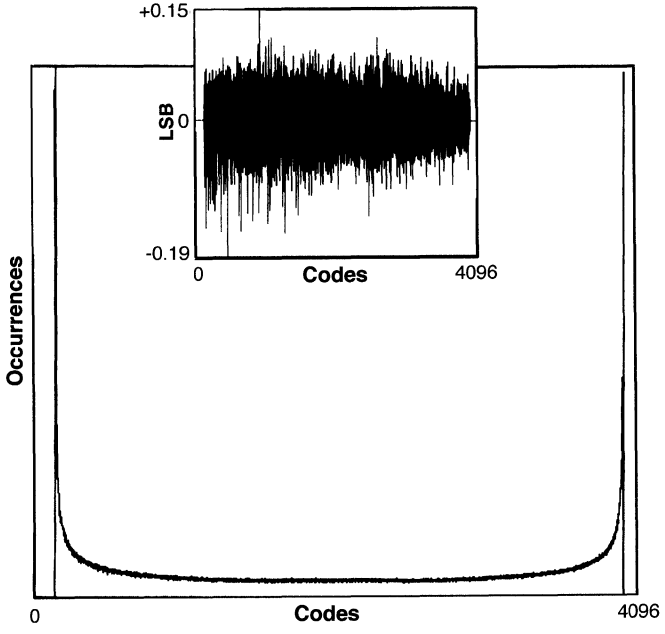
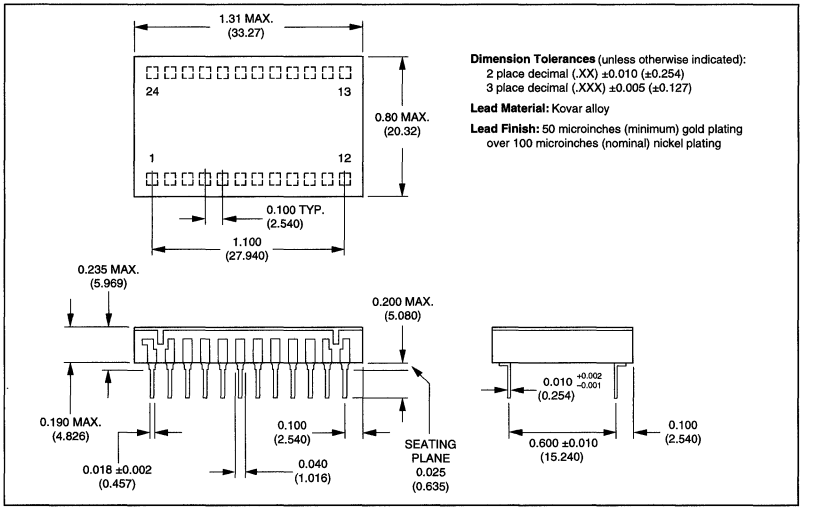


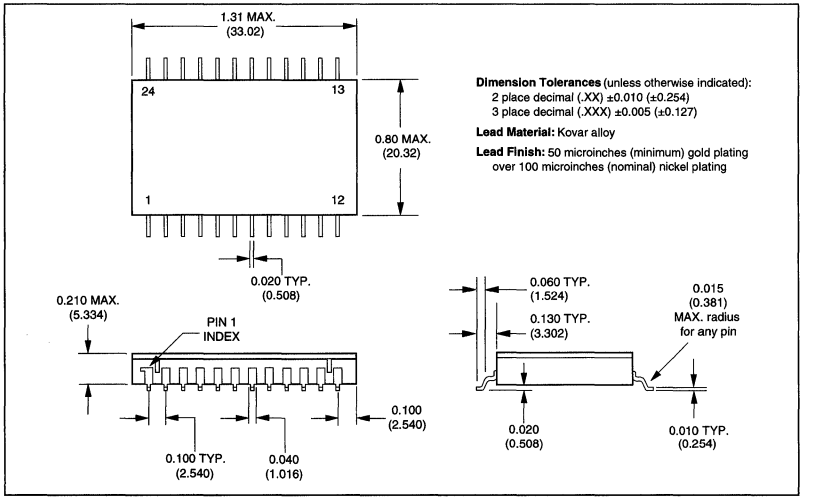
Figure 9. ADS-CCD1201 Histogram and Differential Nonlinearity

MECHANICAL DIMENSIONS
INCHES (mm)

24-Pin DDIP Version



24-Pin Surface Mount Version



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-CCD1201MC	0 to +70°C	Unipolar (0 to +10V)
ADS-CCD1201MM	–55 to +125°C	Unipolar (0 to +10V)

Contact DATEL for availability of surface-mount packaging or high-reliability screening.

ACCESSORIES

ADS-BCCD1201 Evaluation Board (without ADS-CCD1201)
HS-24 Heat Sink for all ADS-CCD1201 models

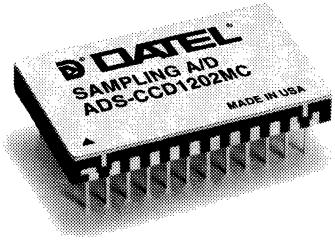
Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

DATEL®
INNOVATION and EXCELLENCE

ADS-CCD1202
12-Bit, 2MHz, Sampling A/D's for CCD Imaging Applications

FEATURES

- **Unipolar input range (0 to +10V)**
- **2MHz sampling rate**
- **4096-to-1 dynamic range (72.2dB)**
- **Low noise, 600µVrms (1/4th of an LSB)**
- **Outstanding differential nonlinearity error (±0.45LSB max.)**
- **Small, 24-pin ceramic DDIP**
- **Low power, 1.75 Watts**
- **Operates from ±12V or ±15V supplies**
- **Edge-triggered, no pipeline delay**
- **Low cost**



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	24	–12V/–15V SUPPLY
2	BIT 11	23	GROUND
3	BIT 10	22	+12V/+15V SUPPLY
4	BIT 9	21	+10V REFERENCE OUT
5	BIT 8	20	ANALOG INPUT
6	BIT 7	19	GROUND
7	BIT 6	18	NO CONNECT
8	BIT 5	17	NO CONNECT
9	BIT 4	16	START CONVERT
10	BIT 3	15	$\overline{\text{EOC}}$
11	BIT 2	14	GROUND
12	BIT 1 (MSB)	13	+5V SUPPLY

GENERAL DESCRIPTION

The functionally complete, easy-to-use ADS-CCD1202 is a 12-bit, 2MHz Sampling A/D Converter whose performance and production testing have been optimized for use in CCD applications. This device delivers the lowest noise (600µVrms) and the best differential linearity error (±0.45LSB maximum) of any commercially available 12-bit A/D in its speed class. It can respond to full scale input steps (from empty to full well) with less than a single count of error, and its input is immune to overvoltages that may occur due to blooming.

Packaged in an industry-standard, 24-pin, ceramic DDIP, the ADS-CCD1202 requires ±15V (or ±12V) and +5V supplies and typically consumes 1.75 (1.45) Watts. The device is 100% production tested for all critical performance parameters and is fully specified over both the 0 to +70°C and –55 to +125°C operating temperature ranges.

For those applications using correlated double sampling, the ADS-CCD1202 can be supplied without its internal sample-hold amplifier and achieve conversion rates up to 2.5MHz. DATEL will also entertain discussions about including the CDS circuit internal to the ADS-CCD1202. Please contact us for more details.

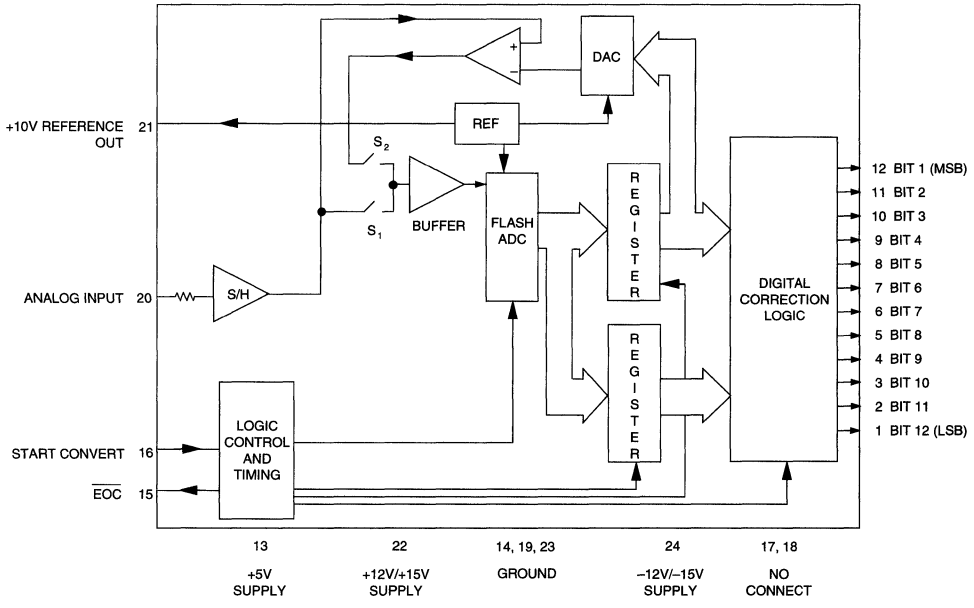


Figure 1. ADS-CCD1202 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+12V/+15V Supply (Pin 22)	0 to +16	Volts
-12V/–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 20)	–5 to +14	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS–CCD1202MC	0	—	+70	°C
ADS–CCD1202MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	5	—	°C/Watt
θca	—	24	—	°C/Watt
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V (or ±12V), +V_{DD} = +5V, 2MHz sampling rate, and a minimum 1 minute warmup ① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Voltage Range ②	—	0 to +10	—	—	0 to +10	—	—	0 to +10	—	Volts
Input Resistance	0.99	1	1.01	0.99	1	1.01	0.99	1	1.01	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2	—	—	+2	—	—	+2	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	200	—	—	200	—	—	200	—	ns
STATIC PERFORMANCE										
Resolution	—	12	—	—	12	—	—	12	—	Bits
Integral Nonlinearity (f_{in} = 10kHz)	—	±0.5	—	—	±0.5	—	—	±1	—	LSB
Differential Nonlinearity (f_{in} = 10kHz)	—	±0.25	±0.45	—	±0.25	±0.45	—	±0.35	±0.75	LSB
Full Scale Absolute Accuracy	—	±0.1	±0.3	—	±0.2	±0.5	—	±0.3	±0.8	%FSR
Offset Error (Tech Note 2)	—	±0.15	±0.3	—	±0.2	±0.5	—	±0.5	±1.2	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.4	—	±0.4	±0.8	—	±0.5	±1.4	%
No Missing Codes (f_{in} = 10kHz)	12	—	—	12	—	—	12	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 500kHz	—	–80	–75	—	–80	–75	—	–76	–72	dB
500kHz to 1MHz	—	–77	–71	—	–77	–71	—	–73	–66	dB
Total Harmonic Distortion (–0.5dB)										
dc to 500kHz	—	–76	–73	—	–76	–73	—	–74	–70	dB
500kHz to 1MHz	—	–75	–70	—	–75	–70	—	–71	–65	dB
Signal–to–Noise Ratio										
(w/o distortion, –0.5dB)										
dc to 500kHz	71	72	—	71	72	—	71	72	—	dB
500kHz to 1MHz	71	72	—	71	72	—	70	72	—	dB
Signal–to–Noise Ratio ④										
(& distortion, –0.5dB)										
dc to 500kHz	70	71	—	70	71	—	68	70	—	dB
500kHz to 1MHz	68	71	—	68	71	—	65	69	—	dB
Two–tone Intermodulation Distortion (f_{in} = 200kHz, 500kHz, f_s = 2MHz, –0.5dB)	—	–83	—	—	–82	—	—	–81	—	dB
Noise	—	600	—	—	600	—	—	600	—	µVrms
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	9	—	—	9	—	—	9	—	MHz
Large Signal (–0.5dB input)	—	8	—	—	8	—	—	8	—	MHz
Feedthrough Rejection (f_{in} = 1MHz)	—	82	—	—	82	—	—	82	—	dB
Slew Rate	—	±200	—	—	±200	—	—	±200	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.01%FSR, 10V step)	150	190	230	150	190	230	150	190	230	ns
Overvoltage Recovery Time ⑤	—	400	500	—	400	500	—	400	500	ns
A/D Conversion Rate	2	—	—	2	—	—	2	—	—	MHz

ANALOG OUTPUT	+25°C MIN.	+25°C TYP.	+25°C MAX.	0 to +70°C MIN.	0 to +70°C TYP.	0 to +70°C MAX.	–55 to +125°C MIN.	–55 to +125°C TYP.	–55 to +125°C MAX.	UNITS
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/°C
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Delay, Falling Edge of $\overline{EOC}$ to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Straight Binary									
POWER REQUIREMENTS, ±15V										
Power Supply Range										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+15V Supply	—	+43	+55	—	+43	+55	—	+43	+55	mA
–15V Supply	—	–48	–55	—	–48	–55	—	–48	–55	mA
+5V Supply	—	+82	+95	—	+82	+95	—	+82	+95	mA
Power Dissipation	—	1.75	1.95	—	1.75	1.95	—	1.75	1.95	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V
POWER REQUIREMENTS, ±12V										
Power Supply Range										
+12V Supply	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	Volts
–12V Supply	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+12V Supply	—	+43	+55	—	+43	+55	—	+43	+55	mA
–12V Supply	—	–48	–55	—	–48	–55	—	–48	–55	mA
+5V Supply	—	+82	+95	—	+82	+95	—	+82	+95	mA
Power Dissipation	—	1.45	1.65	—	1.45	1.65	—	1.45	1.65	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time.

② Contact DATEL for availability of other input voltage ranges.

③ A 200ns wide start convert pulse is used for all production testing.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-CCD1202 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies, as well as the REFERENCE OUTPUT (pin 21), to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-CCD1202 as possible.

2. The ADS-CCD1202 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. When operating the ADS-CCD1202 from ±12V supplies, do not drive external circuitry with the REFERENCE OUTPUT. The reference's accuracy and drift specifications may not be met, and loading the circuit may cause accuracy errors within the converter.

4. Applying a start convert pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") initiates a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

Table 1. Zero and Gain Adjust

INPUT VOLTAGE RANGE	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V	+1.2207mV	+9.99634V

CALIBRATION PROCEDURE

(Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit of Figure 2 are guaranteed to compensate for the ADS-CCD1202's initial accuracy errors and may not be able to compensate for additional system errors.

All fixed resistors in Figure 2 should be metal-film types, and multiturn potentiometers should have TCR's of 100ppm/°C or

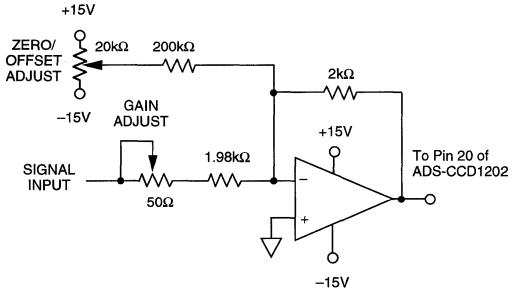


Figure 2. ADS-CCD1202 Calibration Circuit

less to minimize drift with temperature. In many applications, the CCD will require an offset-adjust (black balance) circuit near its output and also a gain stage, presumably with adjust capabilities, to match the output voltage of the CCD to the input range of the A/D. If one is performing a "system I/O calibration" (from light in to digital out), these circuits can be used to compensate for the relatively small initial offset and gain errors of the A/D. This would obviate the need for the circuit shown in Figure 2.

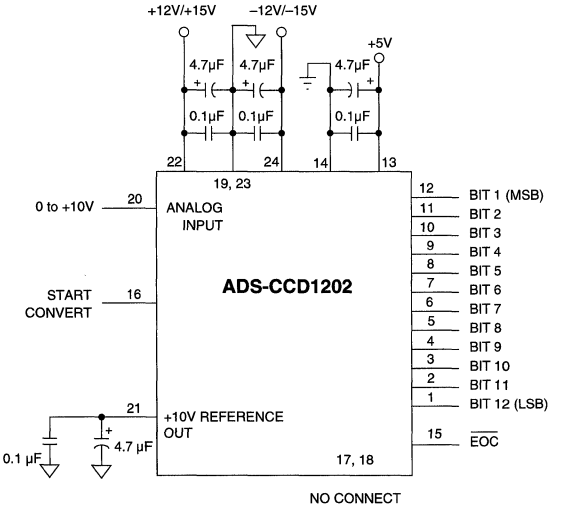


Figure 3. Typical ADS-CCD1202 Connection Diagram

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-CCD1202, offset adjusting is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+1.2207mV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+9.99634V) .

Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +1.2207mV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are all 0's and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +9.99634V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.

Table 2. ADS-CCD1202 Output Coding

INPUT VOLTAGE (0 to +10V)	UNIPOLAR SCALE	DIGITAL OUTPUT MSB LSB
+9.9976	+FS –1LSB	1111 1111 1111
+7.5000	+3/4 FS	1100 0000 0000
+5.0000	+1/2 FS	1000 0000 0000
+2.5000	+1/4 FS	0100 0000 0000
+0.0024	+1LSB	0000 0000 0001
0	0	0000 0000 0000

Coding is straight binary; 1LSB = 2.44mV

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and –55 to + 125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed", and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters", or contact DATEL directly, for additional information.

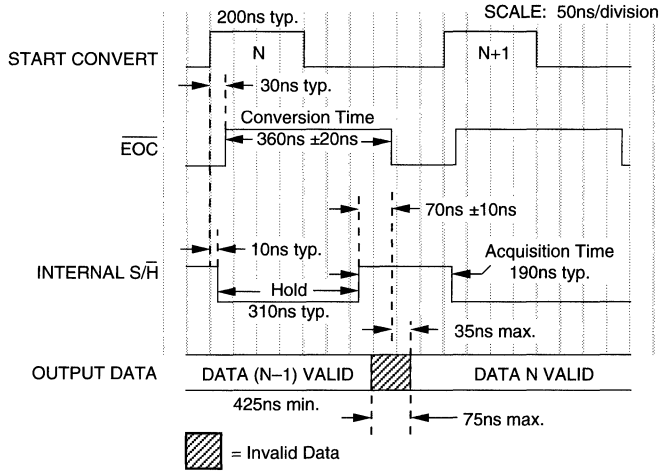


Figure 4. ADS-CCD1202 Timing Diagram

TIMING

The ADS-CCD1202 is an edge-triggered device. A conversion is initiated by the rising edge of the start convert pulse and no additional external timimg signals are required. The device does not employ "pipeline" delays to increase its throughput rate. It does not require multiple start convert pulses to bring valid digital data to its output pins.

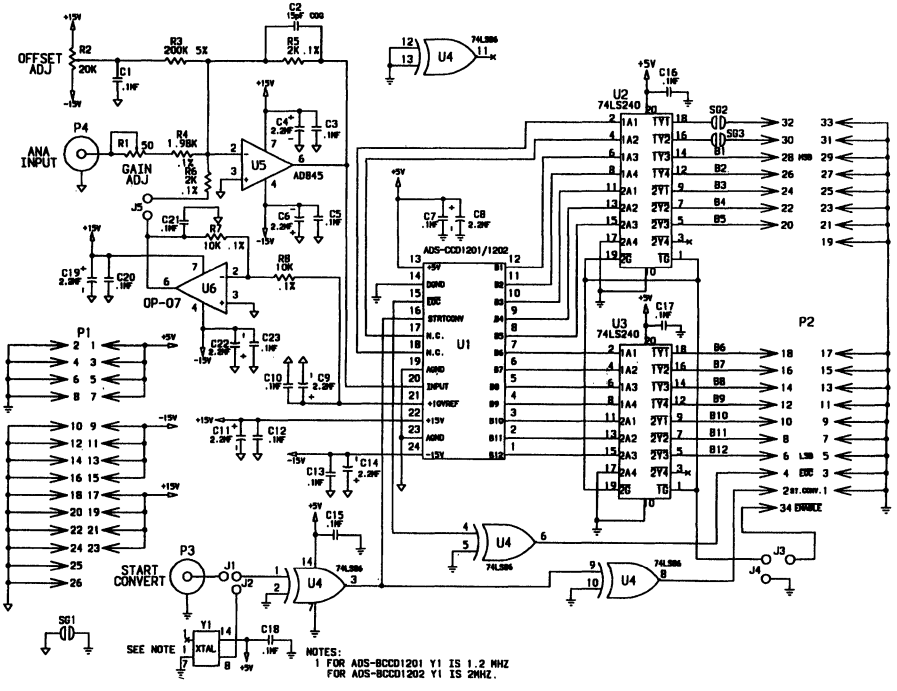


Figure 5. ADS-CCD1202 Evaluation Board Schematic

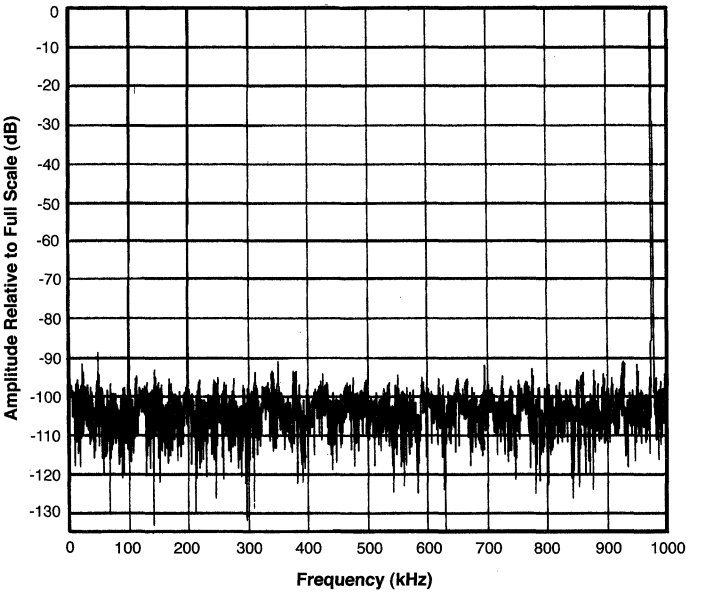
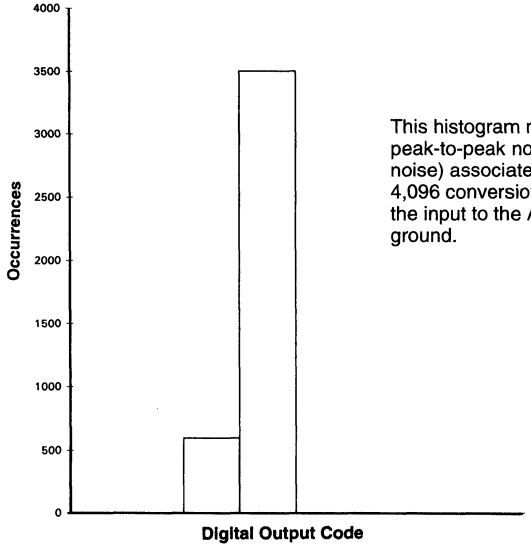


Figure 6. ADS-CCD1202 FFT
(f_{in} = 975kHz, f_S = 2MHz, V_{in} = –0.5dB, 4,096 points)



This histogram represents the typical peak-to-peak noise (including quantization noise) associated with the ADS-CCD1202. 4,096 conversions were processed with the input to the ADS-CCD1202 tied to ground.

Figure 7. ADS-CCD1202 Grounded Input Histogram

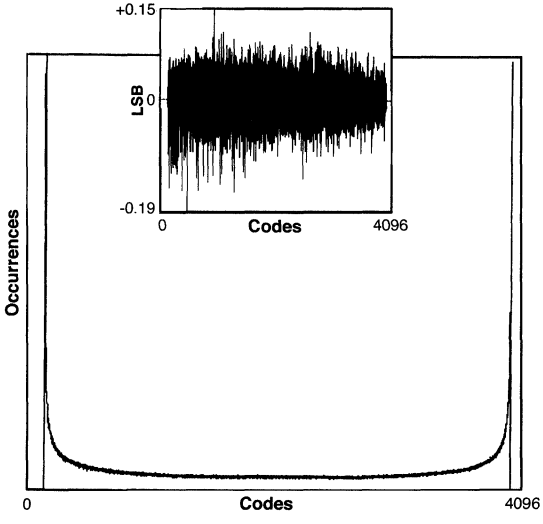
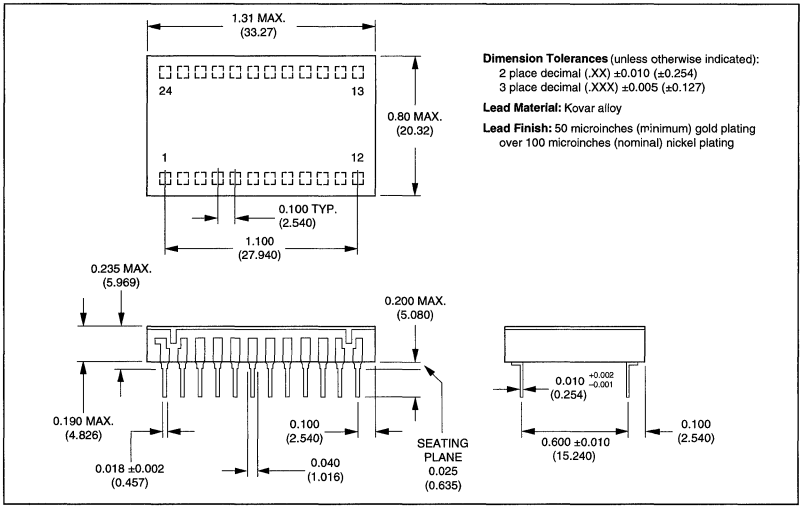


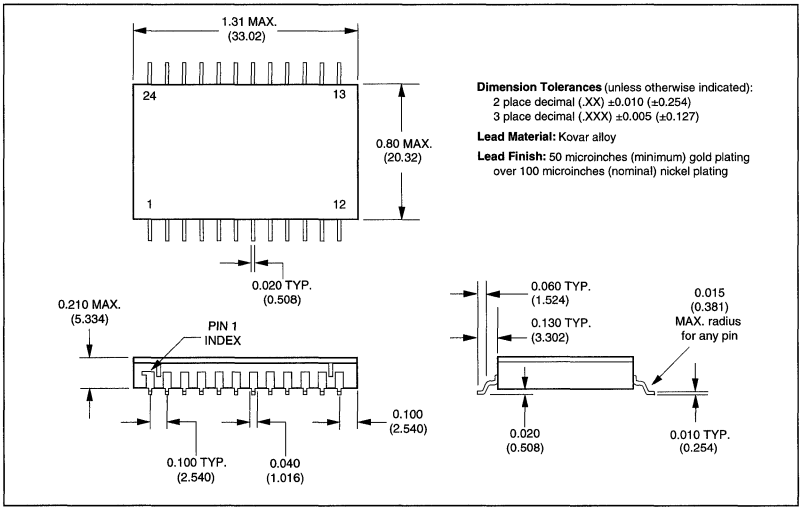
Figure 8. ADS-CCD1202 Histogram and Differential Nonlinearity

MECHANICAL DIMENSIONS
INCHES (mm)

24-Pin DDIP Version



24-Pin Surface Mount Version



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-CCD1202MC	0 to +70°C	Unipolar (0 to +10V)
ADS-CCD1202MM	–55 to +125°C	Unipolar (0 to +10V)

Contact DATEL for availability of surface-mount packaging or high-reliability screening.

ACCESSORIES

ADS-BCCD1202 Evaluation Board (without ADS-CCD1202)
HS-24 Heat Sink for all ADS-CCD1202 DDIP models

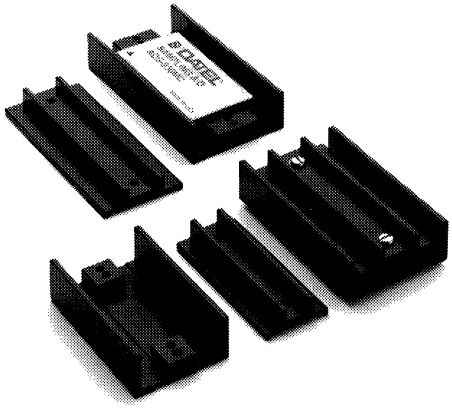
Receptacles for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

DATEL®
INNOVATION and EXCELLENCE

HS-24, HS-32, HS-40
Heat Sinks for 24-Pin, 32-Pin and 40-Pin DIPS

FEATURES

- **Supports hybrid or monolithic components**
- **Drastically decreases thermal resistance, θca**
- **Improves hybrid performance and reliability**
- **Anodized aluminum construction**
- **Low cost**

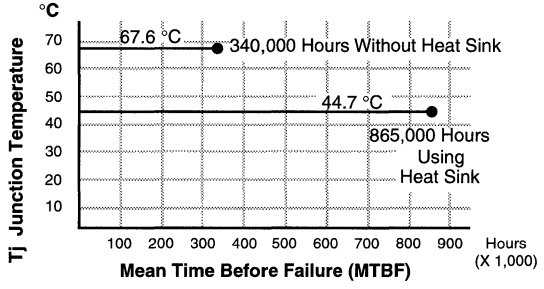


GENERAL DESCRIPTION

To further increase both the electrical performance and reliability of hybrid components, DATEL has developed a series of aluminum heat sinks for conventional 24-pin DDIP, 32-pin TDIP, and 40-pin TDIP packages.

The HS Series of heat sinks is suitable for use with both side- and bottom-brazed dual in-line packages. The heat sinks consist of a top and bottom assembly (cover and base) which together enclose the package. A compressible, thermally-conductive silicone preform is used to seal the top and bottom components to the respective surfaces of the package, maximizing thermal contact. The HS-24, HS-32, and HS-40 heat sinks are designed for printed circuit board mounting. The HS heat sinks are made of anodized aluminum which provides high levels of heat conduction and dissipation.

Performance improvements include a typical increase in MTBF of 250 percent and an average reduction in case temperature (Tc) of 35 percent. This corresponds to an average decrease in junction temperature of approximately 30 percent.



SPECIFICATIONS

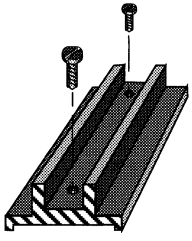
Package	θca (typ.)	Units
24-pin without HS-24	23	°C/W
24-pin with HS-24	9	°C/W
32-pin without HS-32	18	°C/W
32-pin with HS-32	7	°C/W
40-pin without HS-40	17	°C/W
40-pin with HS-40	6	°C/W

ORDERING INFORMATION

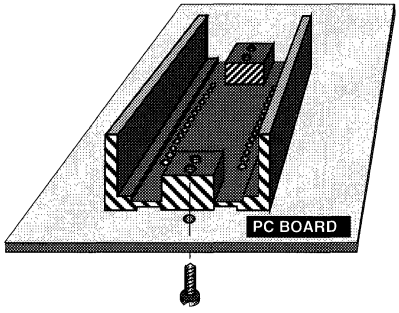
PART NUMBER	PACKAGE TYPE
HS-24	24-pin DDIP
HS-32	32-pin TDIP
HS-40	40-pin TDIP

For additional information, request DATEL Application Note AN-8

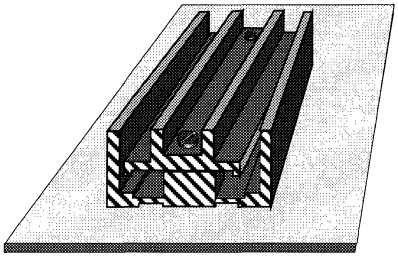
COVER



BASE

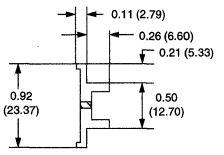


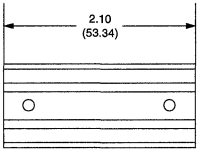
ASSEMBLED (DIP not Visible)



MECHANICAL DIMENSIONS
Inches (mm)

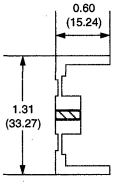
Cover, end view

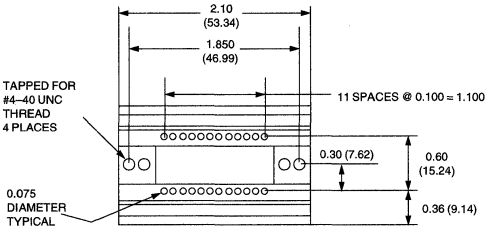




Cover, top view

Base, end view

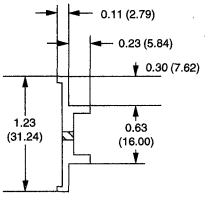


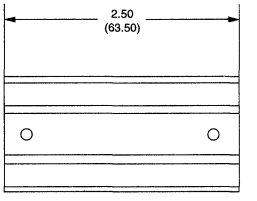


Base, top view

Heat Sink for 24-Pin DDIP Packages

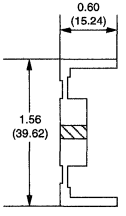
Cover, end view

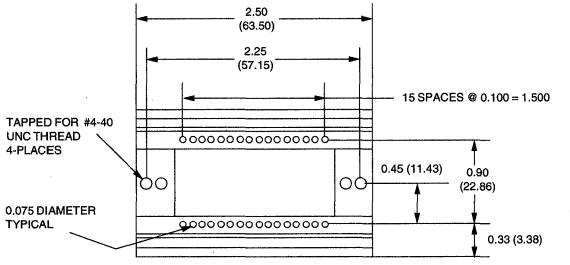




Cover, top view

Base, end view

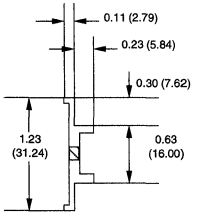


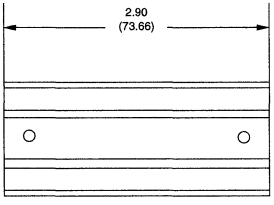


Base, top view

Heat Sink for 32-Pin TDIP Packages

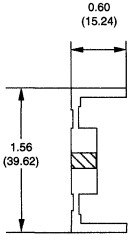
Cover, end view

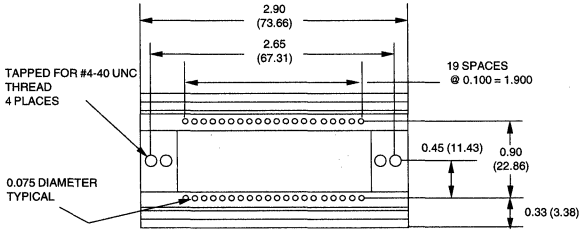




Cover, top view

Base, end view





Base, top view

Heat Sink for 40-Pin TDIP Packages

Analog-to-Digital Converters

Table of Contents

Selection Guide

Model ①	Resolution (Bits)	Guaranteed Conversion Rate/Time	Differential Linearity Error, Max. (LSB)	Integral Linearity Error, Max. (LSB)	Input Range(s) (Volts)	Power Supplies (Volts)	Power Dissipation (mW)	Page
ADC-207	7	20MHz	±0.5	±1	+5	+5	250	**2-3**
ADC-228 ②	8	20MHz	±0.5	±0.5	+5	+5, ±15	1.5 ③	**2-9**
ADC-304	8	20MHz	±0.5	±0.5	–2	+5 or ±5	355	**2-13**
ADC-305	8	20MHz	±0.5	±0.5 ④	+2	+5	60	**2-18**
ADC-317	8	125MHz	±0.7	±0.8	–2	–5.2	870	**2-23**
ADC-HZ	12	8µs	±0.75	±0.5	+5/10, ±2.5/5/10	+5, ±15	1.1 ③	**2-28**
ADC-HX	12	20µs	±0.75	±0.5	+5/10, ±2.5/5/10	+5, ±15	1.1 ③	**2-28**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① MIL-STD-883 screening available on all models except ADC-304/305/317.
② The ADC-228 is a "complete" flash A/D with reference, input buffer, 3-state output, etc.
③ Watts.
④ Listed specification is a typical.

For literature or technical assistance

800-233-2765

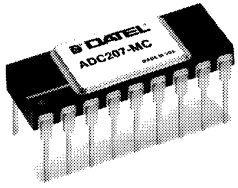
or contact your local DATEL Sales Office or Representative

DATEL®
INNOVATION and EXCELLENCE

ADC-207
7-Bit, 20MHz, CMOS Flash A/D Converters

FEATURES

- 7-bit flash A/D converter
- 20MHz sampling rate
- Low power (250mW)
- Single +5V supply
- 1.2 micron CMOS technology
- 7-bit latched 3-state output with overflow bit
- Surface-mount versions
- High-reliability version
- No missing codes



2

GENERAL DESCRIPTION

The ADC-207 is the industry's first 7-bit flash converter using an advanced high-speed VLSI 1.2 micron CMOS process. This process offers some very distinctive advantages over other processes, making the ADC-207 unique. The smaller geometrics of the process achieve high speed, better linearity and superior temperature performance.

Since the ADC-207 is a CMOS device, it also has very low power consumption (250mW). The device draws power from a single +5V supply and is conservatively rated for 20MHz operation. The ADC-207 allows using sampling apertures as small as 12ns, making it more closely approach an ideal sampler. The small sampling apertures also let the device operate at greater than 20MHz.

The ADC-207 has 128 comparators which are auto-balanced on every conversion to cancel out any offsets due to temperature and/or dynamic effects. The resistor ladder has a midpoint tap for use with an external voltage source to improve integral linearity beyond 7 bits. The ADC-207 also provides the user with 3-state outputs for easy interfacing to other components.

There are six models of the ADC-207 covering two operating temperature ranges, 0 to +70°C and –55 to +125°C. Two high-reliability "QL" models are also available.

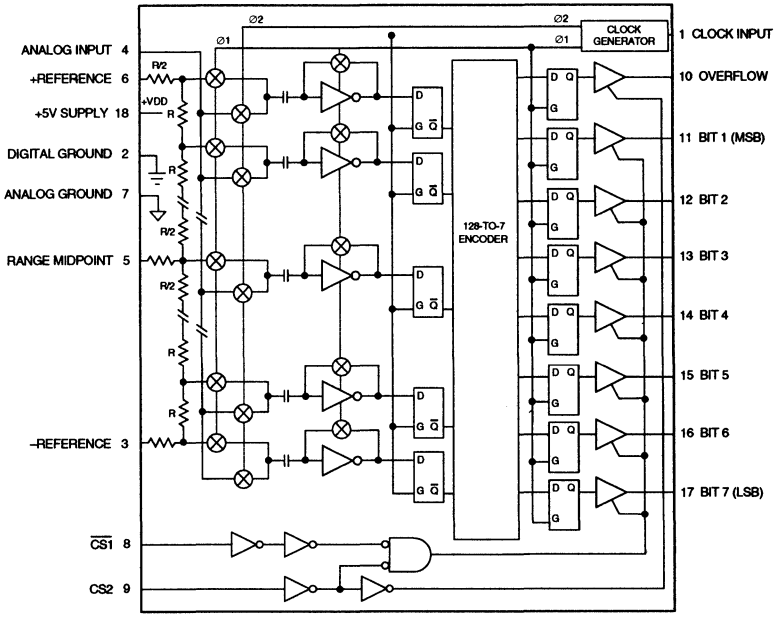


Figure 1. ADC-207 Functional Block Diagram (DIP Pinout)

INPUT/OUTPUT CONNECTIONS

DIP PINS	FUNCTION	LCC PINS
1	CLOCK INPUT	1
2	DIGITAL GROUND	4
3	–REFERENCE	5
4	ANALOG INPUT	6
5	MIDPOINT	7
6	+REFERENCE	8
7	ANALOG GROUND	9
8	$\overline{CS1}$	11
9	CS2	12
10	OVERFLOW	13
11	BIT 1 (MSB)	14
12	BIT 2	16
13	BIT 3	17
14	BIT 4	19
15	BIT 5	20
16	BIT 6	21
17	BIT 7 (LSB)	23
18	+5V SUPPLY	24

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
Power Supply Voltage (+V_{DD})	–0.5 to +7	Volts
Digital Inputs	–0.5 to +5.5	Volts
Analog Input	–0.5 to (+V_{DD} +0.5)	Volts
Reference Inputs	–0.5 to +V_{DD}	Volts
Digital Outputs	–0.5 to +5.5	Volts
(short circuit protected to ground)		
Lead Temperature (10 sec. max.)	+300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case:				
LC/MC Versions	0	—	+70	°C
MM/LM/QL Versions	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type				
DIP	18-pin ceramic DIP			
LCC	24-pin ceramic LCC			

FUNCTIONAL SPECIFICATIONS

(Typical at +5V power, +25°C, 20MHz clock, +REFERENCE = +5V, –REFERENCE = ground, unless noted)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Type	Single-ended, non-isolated			
Input Range (dc-20MHz)	0	—	+5	Volts
Input Impedance	—	1000	—	Ohms
Input Capacitance (Full Range)	—	10	—	pF
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+3.2	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Loading "1"	—	±1	±5	microamps
Logic Loading "0"	—	±1	±5	microamps
Sample Pulse Width				
(During Sampling Portion of Clock)	12	—	—	ns
Reference Ladder Resistance	225	330	—	Ohms
PERFORMANCE				
Conversion Rate ①	20	25	—	MHz
Harmonic Distortion ②				
(8MHz 2nd Order Harmonic)	—	–40	—	dB
Differential Gain ③	—	3	—	%
Differential Phase ③	—	1.5	—	degrees
Aperture Delay	—	8	—	ns
Aperture Jitter	—	50	—	ps
No Missing Codes				
LC/MC grade	0	—	+70	°C
LM/MM grade	–55	—	+125	°C
Integral Linearity ④	—	±0.8	±1	LSB
Over Temperature Range	—	±1	—	LSB
Differential Nonlinearity	—	±0.3	±0.5	LSB
Over Temperature Range	—	±0.4	±0.6	LSB
Power Supply Rejection	—	±0.02	—	%FSR/%Vs
DIGITAL OUTPUTS				
Data Coding	Straight binary			
Data Output Resolution	7	—	—	Bits
Logic Levels				
Logic "1"	+2.4	+4.5	—	Volts
Logic "0" (at 1.6mA)	—	—	+0.4	Volts
Logic Loading "1"	–4	—	—	mA
Logic Loading "0"	+4	—	—	mA
Output Data Valid Delay				
(From Rising Edge)	—	15	17	ns
POWER REQUIREMENTS				
Power Supply Range (+V_{DD})	+3.0	+5.0	+5.5	Volts
Power Supply Current	—	+50	+70	mA
Power Dissipation	—	250	385	mW

Footnotes:
① At full power input and chip selects enabled.
② At 4MHz input and 20MHz clock.
③ For 10-step, 40 IRE NTSC ramp test.
④ Adjustable using reference ladder midpoint tap. See ADC-207 Operation.

TECHNICAL NOTES

1. Input Buffer Amplifier – Since the ADC-207 has a switched capacitor type input, the input impedance of the 207 is dependent on the clock frequency. At relatively slow conversion rates, a general purpose type input buffer can be used; at high conversion rates DATEL recommends either the HA-5033 or Elantec 2003. See Figure 2 for typical connections.

2. Reference Ladder – Adjusting the voltage at +REFERENCE adjusts the gain of the ADC-207. Adjusting the voltage at –REFERENCE adjusts the offset or zero of the ADC-207. The midpoint pin is usually bypassed to ground through a 0.1µF capacitor, although it can be tied to a precision voltage halfway between +REFERENCE and –REFERENCE. This would improve integral linearity beyond 7 bits.

3. Clock Pulse Width – To improve performance at Nyquist bandwidths, the clock duty cycle can be adjusted so that the low portion of the clock pulse is 12ns wide. The smaller aperture allows the ADC-207 to closely resemble an ideal sampler. See Figure 4.

4. At sampling rates less than 100kHz, there may be some degradation in offset and differential nonlinearity. Performance may be improved by increasing the clock duty cycle (decreasing the time spent in the sample mode).

CAUTION

Since the ADC-207 is a CMOS device, normal precautions against static electricity should be taken. Use ground straps, grounded mats, etc. The Absolute Maximum Ratings of the device MUST NOT BE EXCEEDED as irrevocable damage to the ADC-207 will occur.

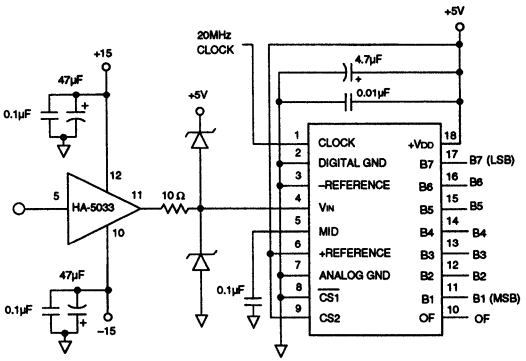


Figure 2. Typical Connections for Using the ADC-207

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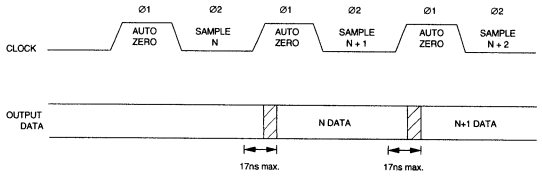
OUTPUT CODING

(+REFERENCE = +5.12V, –REFERENCE = ground, MIDPOINT = no connection)

NOTE: The reference should be held to ±0.1% accuracy or better. Do not use the +5V power supply as a reference input without precision regulation and high frequency decoupling.

Values shown here are for a +5.12V reference. Scale other references proportionally. Calibration equipment should test for code changes at the midpoints between these center values shown in Table 1. For example, at the half-scale major carry, set the input to 2.54V and adjust the reference until the code flickers equally between 63 and 64. Note also that the weighting for the comparator resistor network leaves the first and last thresholds within 1/2LSB of the end points to adjust the code transition to the proper midpoint values.

TIMING DIAGRAM



2

Table 1. ADC-207 Output Coding

Analog Input (Center Value)	Code	Overflow	1 MSB	2	3	4	5	6	7 LSB	Decimal	Hexadecimal (Incl. 0V)
0.00V	Zero	0	0	0	0	0	0	0	0	0	00
+0.04V	+1LSB	0	0	0	0	0	0	0	1	1	01
+1.28V	+1/4FS	0	0	1	0	0	0	0	0	32	20
+2.52V	+1/2FS – 1LSB	0	0	1	1	1	1	1	1	63	3F
+2.56V	+1/2FS	0	1	0	0	0	0	0	0	64	40
+2.60V	+1/2FS + 1LSB	0	1	0	0	0	0	0	1	65	41
+3.84V	+3/4FS	0	1	1	0	0	0	0	0	96	60
+5.08V	+FS	0	1	1	1	1	1	1	1	127	7F
+5.12V	Overflow	1	1	1	1	1	1	1	1	255*	FF

*Note that the overflow code does not clear the data bits.

ADC-207 OPERATION

The ADC-207 uses a switched capacitor scheme in which there is an auto-zero phase and a sampling phase. See Figure 1 and Timing Diagram. The ADC-207 uses a single clock input. When the clock is at a high state (logic 1), the ADC-207 is in the auto-zero phase (Ø1). When the clock is at a low state (logic 0), the ADC-207 is in the sampling phase (Ø2). During phase 1, the 128 comparator outputs are shorted to their inputs through CMOS switches. This serves the purpose of bringing the inputs and outputs to the transition levels of the respective comparators. The inputs to the comparators are also connected to 128 sampling capacitors. The other end of the 128 capacitors are also shorted to 128 taps of a resistor ladder, via CMOS switches. Therefore, during phase 1 the sampling capacitors are charged to the differential voltage between a resistor tap and its respective comparator transition voltage.

This eliminates offset differences between comparators and yields better temperature performance. During phase 2 (Ø2) the input voltage is applied to the 128 capacitors, via CMOS switches. This forces the comparators to trip either high or low. Since the comparators during phase 1 were sitting at their transition point, they can trip very quickly to the correct state. Also during phase 2, the outputs of the comparators are loaded into internal latches which in turn feed a128-to-7 encoder. When going back into phase 1, the output of the encoder is loaded into an output latch. This latch then feeds the 3-state output buffer.

This means that the ADC-207 is of pipeline design. To do a single conversion, the ADC-207 requires a positive pulse followed by a negative pulse followed by a positive pulse. Continuous conversion requires one cycle/sample (one positive pulse and one negative pulse). The 3-state buffer has two enable lines, $\overline{CS1}$ and CS2. Table 2 shows the truth table for chip select signals. $\overline{CS1}$ has the function of enabling/disabling bits 1 through 7. CS2 has the function of enabling/disabling bits 1 through 7 and the overflow bit. Also, a full-scale input produces all ones, including the overflow bit at the output. The ADC-207 has an adjustable resistor ladder string. The top end, idle point, and bottom end are brought out for use with applications circuits.

These pins are called +REFERENCE, MIDPOINT and –REFERENCE, respectively. In typical operation +REFERENCE is tied to +5V, –REFERENCE is tied to ground, and MIDPOINT is bypassed to ground. Such a configuration results in a 0 to +5V input voltage range. The MIDPOINT pin can also be tied to a +2.5V source to further improve integral linearity. This is usually not necessary unless better than 7-bit linearity is needed.

Table 2. Chip Select Truth Table

$\overline{CS1}$	CS2	Bits 1-7	Overflow Bit
0	0	3-State Mode	3-State Mode
1	0	3-State Mode	3-State Mode
0	1	Data Outputed	Data Outputed
1	1	3-State Mode	Data Outputed

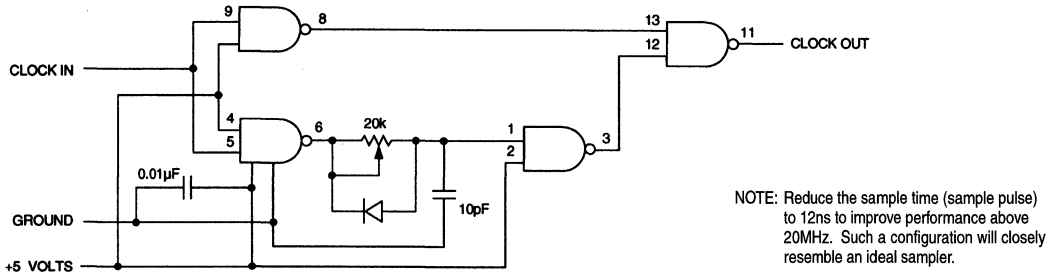


Figure 3. Optional Pulse Shaping Circuit

USING TWO ADC-207'S FOR 8-BIT RESOLUTION

Two ADC-207's (A and B) are cascadable for applications requiring 8-bit resolution. The device A provides a typical 7-bit output. The OVERFLOW signal of device A turns off device A and turns on the device B. The OVERFLOW signal of device A is also used as MSB for 8-bit operation. The device B provides the other seven bits from the input signal. Figure 4 shows the circuit connections for the application.

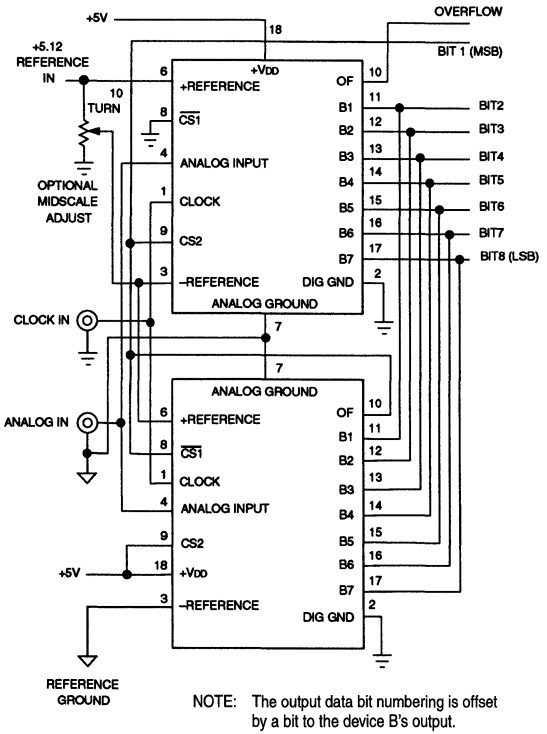


Figure 4. Using Two ADC-207's for 8-Bit Operation

BEAT FREQUENCY AND ENVELOPE TESTS

Figure 5 shows an actual ADC-207 plot of the Beat Frequency Test. This test uses a 20MHz clock input to the ADC-207 with a 20.002MHz full-scale sine wave input. Although the converter would not normally be used in this mode because the input frequency violates Nyquist criteria for full recovery of signal information, the test is an excellent demonstration of the ADC-207's high-frequency performance.

The effect of the 2kHz frequency difference between the input and the clock is that the output will be a 2kHz sinusoidal digital data array which "walks" along the actual input at the 2kHz beat note frequency. Any inability to follow the 20.002MHz input will be immediately obvious by plotting the digital data array. Further arithmetic analysis may be done on the data array to determine spectral purity, harmonic distortion, etc. This test is an excellent indication of:

1. Full power input bandwidth of all 128 comparators. (Any gain loss would show as signal distortion.)
2. Phase response linearity vs. instantaneous signal magnitude. (Phase problems would show as improper codes.)
3. Comparator slew rate limiting.

Figure 6 shows an actual ADC-207 plot of the Envelope Test. This test is a variation of the previous test but uses a 10.002MHz sinewave input to give two overlapping cycles when the data is reconstructed by a D/A converter output to an oscilloscope. The scope is triggered by the 20MHz clock used by the A/D. Any asymmetry between positive and negative portions of the signal will be very obvious. This test is an excellent indication of slew rate capability. At the peaks of the envelope, consecutive samples swing completely through the input voltage range.

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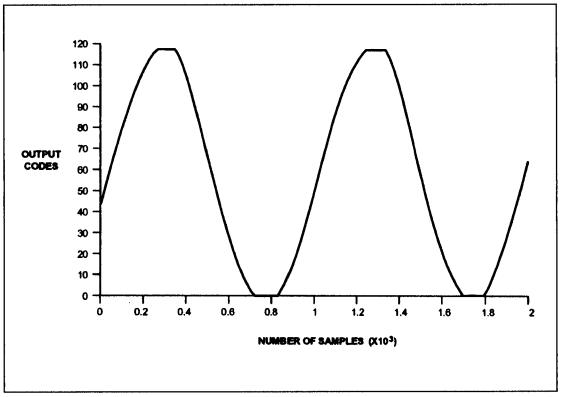


Figure 5. Beat Frequency Test at 20MHz

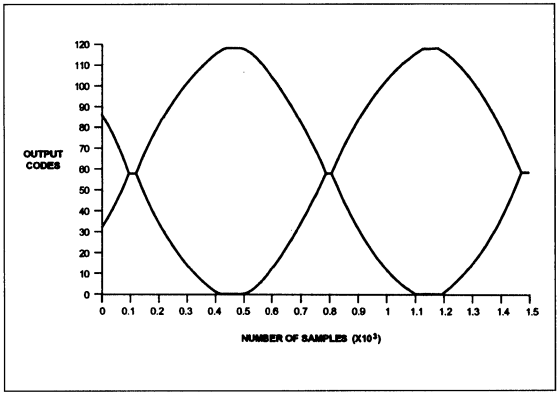


Figure 6. 10MHz Envelope Test

FFT TEST

This test actually produces an amplitude versus frequency graph (Figure 7) which indicates harmonic distortion and signal-to-noise ratio. The theoretical rms signal-to-noise ration for a 7-bit converter is +43.8dB.

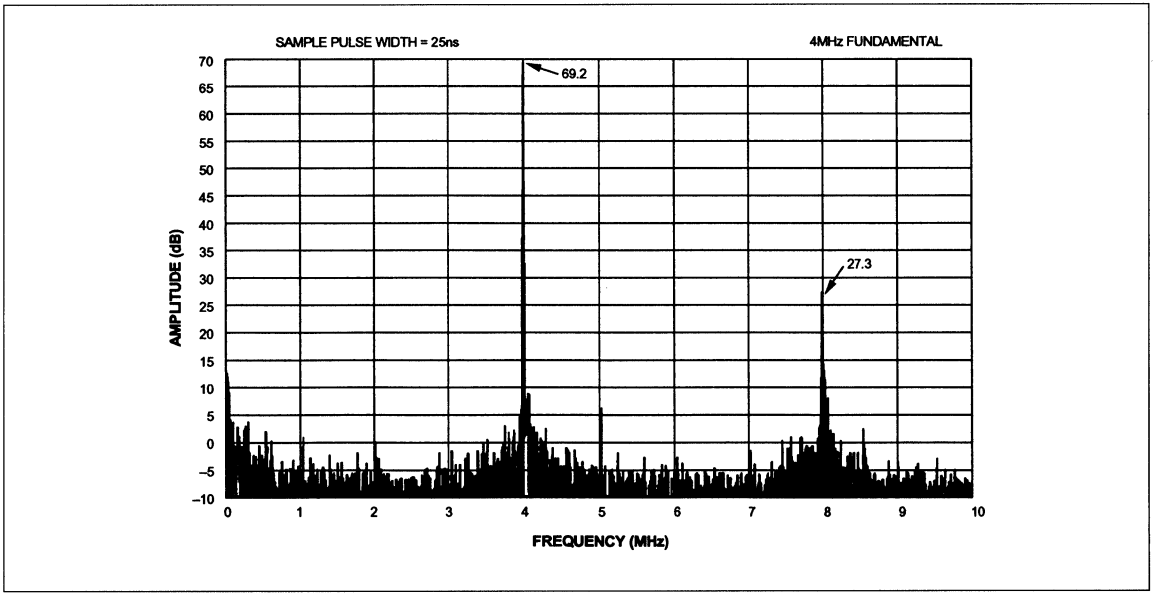
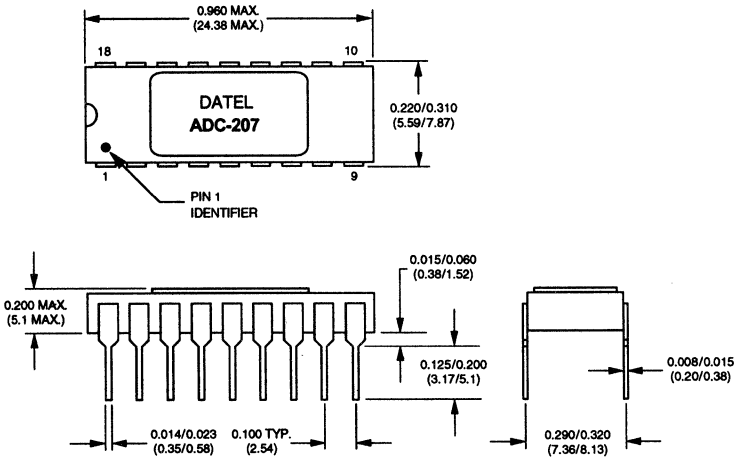


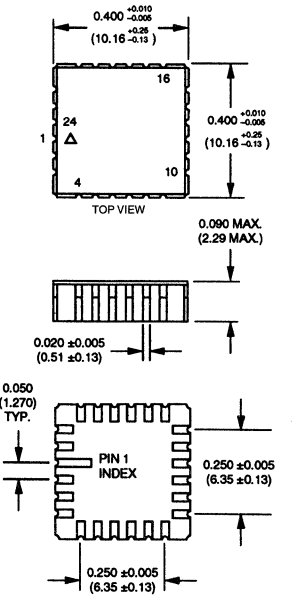
Figure 7. FFT Test Using the ADC-207

MECHANICAL DIMENSIONS INCHES (MM)

18-Pin Ceramic DIP



24-Pin Ceramic LCC



ORDERING INFORMATION

MODEL	TEMP. RANGE	PACKAGE
ADC-207MC	0 to +70°C	18-pin DIP
ADC-207MM	–55 to +125°C	18-pin DIP
ADC-207MM-QL	–55 to +125°C	18-pin DIP
ADC-207LC	0 to +70°C	24-pin CLCC
ADC-207LM	–55 to +125°C	24-pin CLCC
ADC-207LM-QL	–55 to +125°C	24-pin CLCC
ACCESSORIES		
ADC-B207/208	Evaluation Board for DIP Version (without ADC-207)	

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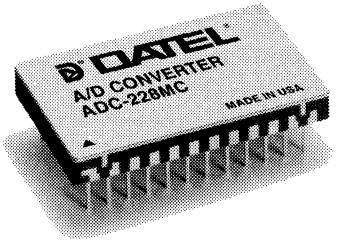
ADC-228
8-Bit, 20MHz, Complete Flash A/D Converter

FEATURES

- **8-Bit flash A/D converter**
- **20MHz sampling rate**
- **Complete support circuitry**
- **Low power, 1.5W**
- **7MHz full power bandwidth**
- **Sample-hold not required**
- **Three-state outputs**
- **MIL-STD-883 versions**



GENERAL DESCRIPTION

The ADC-228 combines analog front-end circuitry and a flash A/D converter to digitize high-speed analog signals at a rate of 20 million samples per second. The ADC-228 contains an 8-bit, 20MHz, flash A/D, a wideband analog input buffer, a precision voltage reference, temperature compensation circuitry, reference trims, and a three-state output buffer in a 24-pin package.

The ADC-228 offers significant savings by combining all of the circuitry in a single package. Valuable board real estate is saved, and design time and manufacturing costs are reduced.

The ADC-228 is housed in a 24-pin ceramic DDIP package and is available in the commercial, 0 to +70°C, or military, –55 to +125°C, temperature ranges. A MIL-STD-883 version is also available. Operation is from ±15V and +5V power supplies.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V SUPPLY	24	BIT 8 (LSB)
2	GROUND	23	BIT 7
3	+5V REFERENCE OUT	22	BIT 6
4	GROUND	21	BIT 5
5	ANALOG INPUT	20	NO CONNECTION
6	GROUND	19	+15V SUPPLY
7	GROUND	18	CLOCK INPUT
8	NLINV	17	BIT 4
9	NMINV	16	BIT 3
10	–15V SUPPLY	15	BIT 2
11	$\overline{CS1}$	14	BIT 1 (MSB)
12	CS1	13	NO CONNECTION

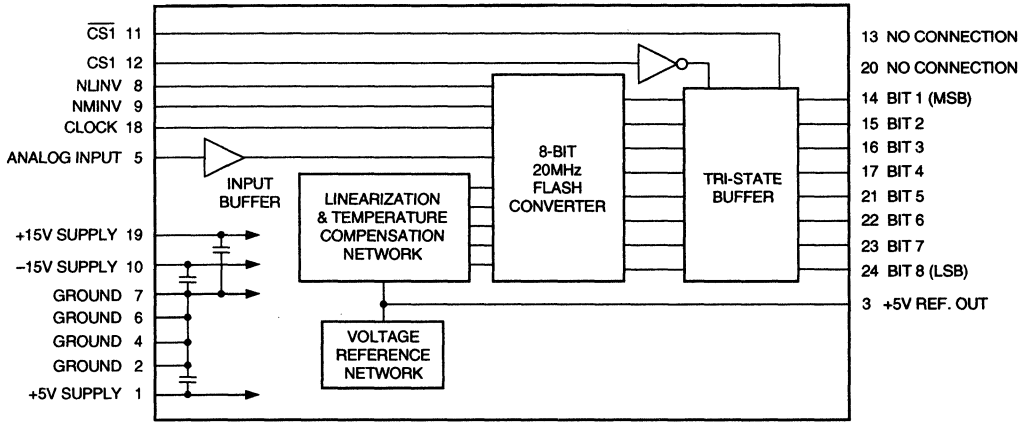


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETER	LIMITS
Power Supply Voltage, Pin 1	–0.5 to +7V
Pin 19	–0.3 to +18V
Pin 10	+0.3 to –18V
Digital Inputs, Pins 8,9,11,12,18	–0.5 to +5.5V
Analog Input, Pin 5	–6 to +7.5V
Digital Outputs	–0.5 to +5.5V (short circuit protected to ground)
Lead Temp. (10 seconds)	+300°C

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range with 20MHz clock and ±15V and +5V power supply voltages, unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Single-Ended, Non-Isolated Input Range, dc-20MHz	0	—	+5.0	Volts
Input Resistance	2.45	2.5	2.55	kΩ
Input Capacitance	—	5	10	pF
DIGITAL INPUTS				
Logic Levels				
Logic 1	+2.0	—	—	Volts
Logic 0	—	—	+0.8	Volts
Logic Loading				
Logic 1	—	—	+160	µA
Logic 0	—	—	–0.5	mA
Clock Pulse Widths				
"High"	25	—	—	ns
"Low"	19	—	—	ns
DIGITAL OUTPUTS				
Coding	Straight bin., comp. bin., two's comp., comp. two's comp.			
Resolution	8 bits			
Logic Levels				
Logic 1	+2.4	—	—	Volts
Logic 0	—	—	+0.4	Volts
Logic Loading				
Logic 1	—	—	–1	mA
Logic 0	—	—	+1	mA
Output Data Valid Delay				
From Rising Edge	—	30	40	ns
Output Hold Time	5	—	—	ns
PERFORMANCE				
Sampling Rate ①	20	—	—	MHz
Differential Linearity ②				
Code Transitions	—	±0.5	±0.75	LSB
Code Centers	—	±0.25	±0.5	LSB
Integral Linearity, +25°C				
End-point	—	±0.5	±0.75	LSB
Best-fit Line	—	±0.35	±0.5	LSB
Over Temperature End-point	—	—	±1	LSB
Best-fit Line	—	—	±1	LSB
Zero-Scale Offset				
Code "0" to "1" Transition +25°C	—	—	±0.5	LSB
–55 to +125°C	—	±0.5	±1.5	LSB
Gain error	—	±0.5	±1.5	LSB
Full Scale Absolute Accuracy	—	±0.5	±1.5	LSB
Differential Gain ③	—	2	—	%
Differential Phase ③	—	1	—	deg.
Aperture Delay	—	8	—	ns
Aperture Jitter	—	50	—	ps
No Missing Codes	Over the operating temperature range			
Power Supply Rejection	±0.02% FSR/%V_S maximum			

DYNAMIC PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Total Harm. Distortion, –0.5dB				
DC to 2.5 MHz	—	–55	–53	dB
2.5 MHz to 5 MHz	—	–50	–48	dB
5 MHz to 10 MHz	—	–39	–36	dB
Signal-to-Noise Ratio and Distortion, –0.5dB				
DC to 2.5 MHz	44	49	—	dB
2.5 MHz to 5 MHz	43	46	—	dB
5 MHz to 10 MHz	35	38	—	dB
Signal-to-Noise Ratio w/o Distortion, –0.5 dB				
DC to 2.5 MHz	45	48	—	dB
2.5 MHz to 5 MHz	45	48	—	dB
5 MHz to 10 MHz	42	45	—	dB
Effective Bits, –0.5dB				
DC to 2.5 MHz	7.1	7.75	—	Bits
2.5 MHz to 5 MHz	6.9	7.4	—	Bits
5 MHz to 10 MHz	5.6	6.1	—	Bits
Input Bandwidth				
Full Power	7	—	—	MHz
Small Signal (–20dB)	40	—	—	MHz
POWER SUPPLY				
Power Supply Range				
+15V Supply	+11	+15	+15.75	Volts
–15V Supply	–11	–15	–15.75	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Current				
+15V Supply	—	—	+30	mA
–15V Supply	—	—	–10	mA
+5V Supply	—	—	+230	mA
Power Dissipation				
±12V, +5V Nominal	—	1.4	1.65	Watts
Over full supply range	—	1.6	1.85	Watts
±15V, +5V Nominal	—	1.5	1.75	Watts
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
ADC-228MC	0 to +70°C			
ADC-228MM, ADC-228/883	–55 to +125°C			
Storage Temp. Range	–65 to +150°C			
Package Type	24-pin, ceramic DDIP			
Weight	0.3 ounces (8.5 grams)			

Footnotes:

① At full power input and chip selects enabled.

② See Technical Note 3.

③ For 10-step, 40 IRE NTSC ramp test.

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TECHNICAL NOTES

1. Rated performance requires using good high-frequency techniques. The analog and digital ground pins are connected to each other internally. Avoid ground related problems by connecting the grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

2. Bypass all the analog and digital supplies and the +5V REFERENCE (pin 3) to ground with a 4.7µF, 25V tantalum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor.

3. DATEL uses conservative definitions when specifying integral linearity (end-point) and differential linearity (code transition). The specifications using the less conservative definitions have also been provided as a comparative specification for products specified this way.

4. Single conversions (one-shot mode) would require another clock edge to read out data. Users desiring to provide just a single clock pulse could use the circuit shown in Figure 2 to obtain the data.

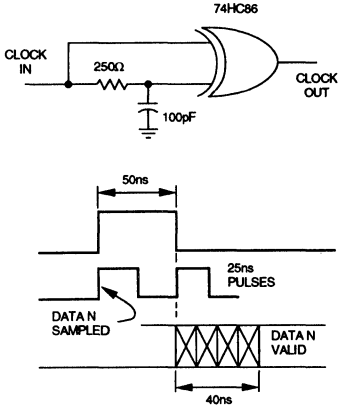


Figure 2. ADC-228 Single Clock Pulse Circuit and Operation

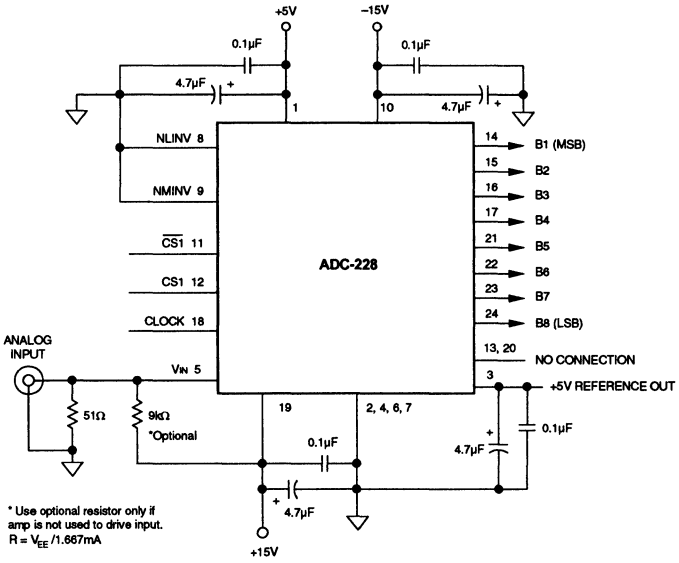


Figure 3. ADC-228 Typical Connections

Table 1. ADC-228 Unipolar Output Coding

ANALOG INPUT	CODE	STRAIGHT BIN. NMINV = 0 NLINV = 0	COMP. BIN. NMINV = 1 NLINV = 1
+4.96V	+FS – 1 LSB	1111 1110	0000 0001
+3.75V	+ 3/4 FS	1100 0000	0011 1111
+2.50V	+ 1/2 FS	1000 0000	0111 1111
+1.25V	+ 1/4 FS	0100 0000	1011 1111
+0.02V	+ 1 LSB	0000 0001	1111 1110
0.00V	ZERO	0000 0000	1111 1111

Table 2. ADC-228 Bipolar Output Coding (Assumes analog input is externally offset)

ANALOG INPUT	CODE	TWO'S COMP. NMINV = 1 NLINV = 0	COMP. TWO'S COMP. NMINV = 0 NLINV = 1
+2.480V	+FS – 1 LSB	0111 1111	1000 0000
+1.250V	+1/2 FS	0100 0000	1011 1111
+0.020V	+1 LSB	0000 0001	1111 1110
+0.000V	ZERO	0000 0000	1111 1111
–1.250V	–1/2 FS	1100 0000	0011 1111
–2.480V	–FS + 1 LSB	1000 0001	0111 1110
–2.500V	–FS	1000 0000	0111 1111

Table 3. Chip Select Truth Table

CS1 Pin 12	$\overline{CS1}$ Pin 11	Bits 1-8
0	0	Three State Mode
0	1	Three State Mode
1	0	Data Outputted
1	1	Three State Mode

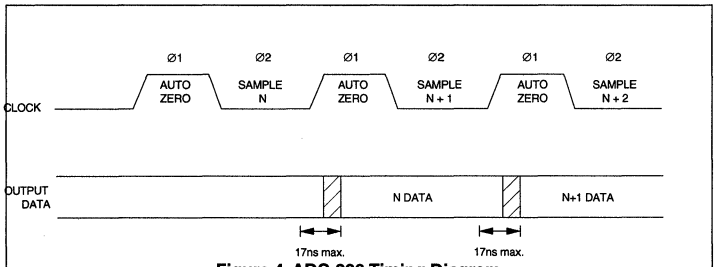
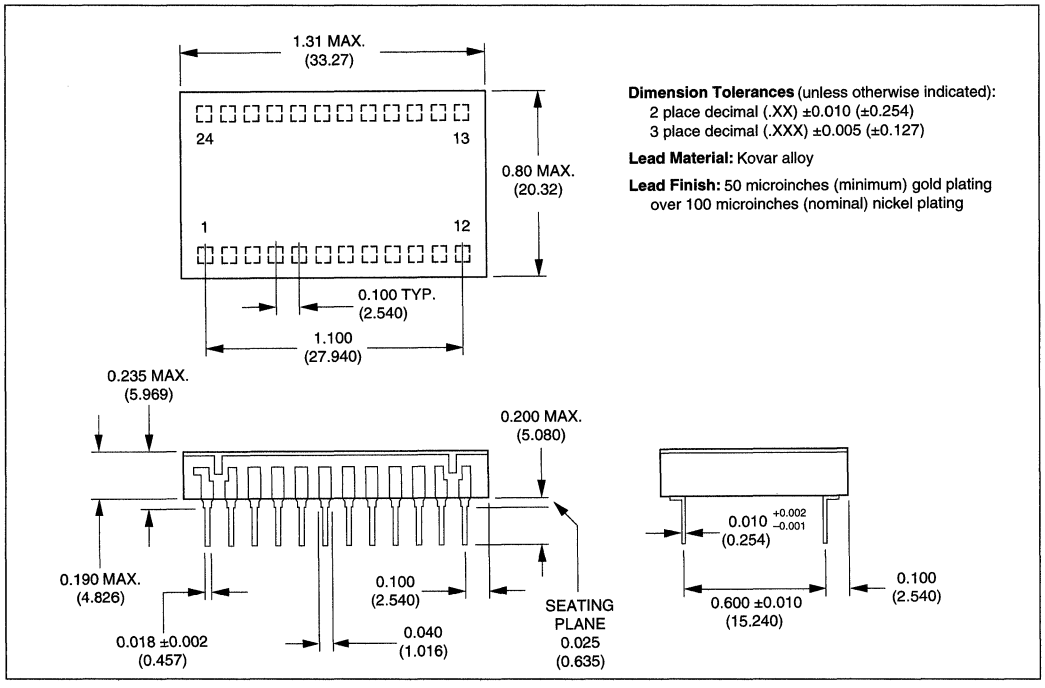


Figure 4. ADC-228 Timing Diagram

MECHANICAL DIMENSIONS
INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-228MC	0 to +70°C
ADC-228MM	–55 to +125°C
ADC-228/883	–55 to +125°C

Receptacle for PC board mounting can be ordered through AMP Inc., part # 3-331272-8 (component lead socket), 24 required.
Contact DATEL for 883 product specifications

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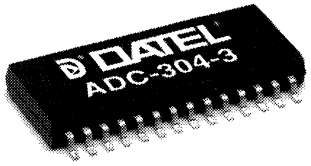
ADC-304
8-Bit, 20MHz, Low-Power Flash A/D Converters

FEATURES

- **8-bit resolution**
- **20MHz conversion rate**
- **±1/2LSB maximum nonlinearity**
- **8MHz input bandwidth**
- **Low power consumption, 375mW**
- **TTL compatible**
- **Single or dual supply operation**



2

GENERAL DESCRIPTION

Datel's ADC-304 is an 8-bit, 20MHz analog-to-digital flash converter. The ADC-304 offers many performance features not obtainable from other flash A/D's.

Key reatures include a low power dissipation of 375mW and TTL-compatible outputs. A wide analog input bandwidth of 8MHz (–3dB) allows operation without the need of a sample-hold. Also, single +5V supply operation is obtainable with an input range of +3 to +5V, eliminating the need for an additional power supply. A 0 to –2V input range is available with ±5V supply operation.

Another novel feature of the ADC-304 is its user-selectable output coding. The MINV and LINV pins allow selection of binary, complementary binary, and if external offset circuitry is used for bipolar inputs, offset binary, two's complement and complementary two's complement coding.

The ADC-304 is supplied in a 28-pin plastic DIP or a 28-pin plastic SOP package. Operating temperature range is –20 to +75°C. Storage temperature range is –55 to +150°C.

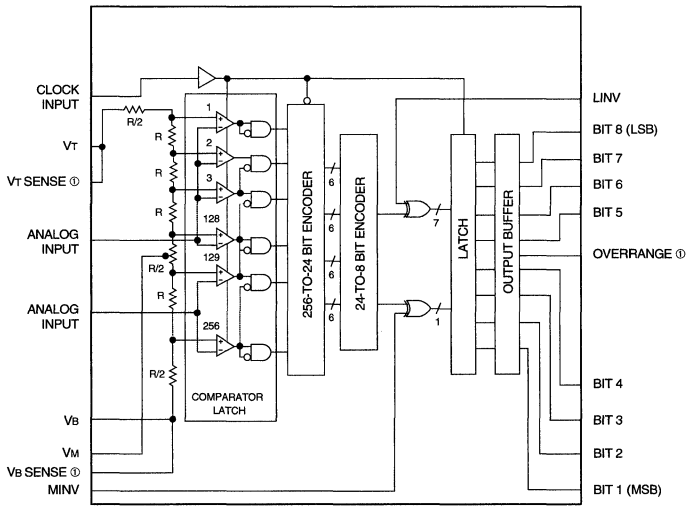


Figure 1. ADC-304 Functional Block Diagram

INPUT/OUTPUT CONNECTIONS PLASTIC DIP PACKAGE

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	MINV
2	BIT 2	27	V_M
3	BIT 3	26	V_B
4	BIT 4	25	ANALOG GND
5	DIGITAL GND	24	NO CONNECT
6	+5V POWER	23	ANALOG INPUT
7	–5.2V POWER	22	NO CONNECT
8	–5.2V POWER	21	ANALOG INPUT
9	–5.2V POWER	20	NO CONNECT
10	+5V POWER	19	ANALOG GND
11	DIGITAL GND	18	V_T
12	LINV	17	CLOCK INPUT
13	BIT 5	16	BIT 8 (LSB)
14	BIT 6	15	BIT 7

INPUT/OUTPUT CONNECTIONS PLASTIC SOP PACKAGE

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG INPUT	28	ANALOG INPUT
2	V_B SENSE	27	V_T SENSE
3	ANALOG GND	26	ANALOG GND
4	V_B	25	V_T
5	V_M	24	CLOCK INPUT
6	NO CONNECT	23	BIT 8 (LSB)
7	MINV	22	BIT 7
8	BIT 1 (MSB)	21	BIT 6
9	BIT 2	20	BIT 5
10	BIT 3	19	LINV
11	BIT 4	18	DIGITAL GND
12	DIGITAL GND	17	+5V POWER
13	+5V POWER	16	OVERRANGE
14	–5.2V POWER	15	–5.2V POWER

ABSOLUTE MAXIMUM RATINGS

PARAMETERS		LIMITS	UNITS
Supply Voltages	$+V_S$ to GND	0 to +6	Volts
	$-V_S$ to GND	0 to –6	Volts
Input Voltage (Analog)	Vin (dual power supply)	$-V_S$ to (ANA GND + 0.3)	Volts
Input Voltage (Reference)	V_T, V_B, V_M (dual power supply)	$-V_S$ to (ANA GND + 0.3)	Volts
	$\lvert V_T - V_B \rvert$	2.5	Volts
Input Current	I_M	–3.0 to +3.0	mA
Input Voltage (Digital)	Digital Inputs	–0.5 to $+V_S$	Volts

FUNCTIONAL SPECIFICATIONS

Unless otherwise noted, the following specifications apply to the ADC-304 when used either with a single or dual power source. The test conditions are:

For single power supply operation:
$+V_S$ = +5V, DIG GND = 0V
$-V_S$ = 0V, V_T = +5V
V_B = +3V, TA = +25°C
ANA GND = +5V, f_S = 20MHz

For dual power supply operation:
$+V_S$ = +5V, DIG GND = 0V
$-V_S$ = –5.2V, V_T = 0V,
V_B = –2V, TA = +25°C
ANA GND = 0V, f_S = 20MHz

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Range	V_B		V_T	Volts
Input Capacitance	—	30	35	pF
Input Bias Current	15	50	100	µA
Offset Voltage				
V_T	–8	–13	–19	mV
V_B	0	+5	+11	mV
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Input Currents				
Logic "1"	—	–100	–150	µA
Logic "0"	–0.1	–0.32	–0.5	mA
PERFORMANCE				
Conversion Rate ①	20	—	—	MHz
Integral Nonlinearity	—	—	±1/2	LSB
Differential Nonlinearity	—	—	±1/2	LSB
Differential Gain Error ②	—	—	1.5	%
Differential Phase Error ②	—	—	0.5	degrees
Aperture Delay Ta	5	7	9	ns
Aperture Uncertainty	—	30	—	ps
Signal-to-Noise and Distortion (Vin = full scale, f_S = 20MHz)				
f_{in} = 1MHz		47		dB
f_{in} = 5MHz		43		dB
f_{in} = 10MHz		35		dB
Clock Pulse Width				
Tpw1	35	—	—	ns
Tpw0	10	—	—	ns
Reference Pin Current	11	15	18	mA
Reference Resistance (V_T to V_B)	—	130	—	Ohms
Reference Input (dual supply)				
V_T	–0.1	0	+0.1	Volts
V_B	–1.8	–2.0	–2.2	Volts

Footnotes:
① f_{in} = 1kHz, ramp
② NTSC 40 IRE-modulated ramp, f_S = 14.3MHz

DIGITAL OUTPUTS	MIN.	TYP.	MAX.	UNITS
Resolution and Output Coding	8 Straight binary Complementary binary Two's complement Complementary two's complement			bits
Logic Levels				
Logic "1"	+2.7	+3.4	—	Volts
Logic "0"	—	—	+0.5	Volts
Logic Loading "1"	—	–500	—	µA
Logic Loading "0"	—	—	+3	mA
Output Data Delay				
TDLH	15	20	30	ns
TDHL	22	26	35	ns
POWER REQUIREMENTS				
Single Power Supply				
Supply Voltage = $+V_S$	+4.75	+5.0	+5.25	Volts
Supply Voltage = $-V_S$	—	0	—	Volts
Supply Current = $+I_S$	+56	+71	+91	mA
Power Dissipation	280	355	455	mW
Dual Power Supply				
Supply Voltage = $+V_S$	+4.75	+5.0	+5.25	Volts
Supply Voltage = $-V_S$	–4.75	–5.2	–5.5	Volts
Supply Current = $+I_S$	+7	+10	+14	mA
Supply Current = $-I_S$	–50	–62	–78	mA
Power Dissipation	295	375	476	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temperature	–20	—	+75	°C
Storage Temperature	–55	—	+150	°C

TECHNICAL NOTES

1. The two DIGITAL GND pins (pins 5 and 11 on the DIP, pins 12 and 18 on the SOP) are not connected to each other internally and neither are the two +5V POWER pins (6 and 10 on the DIP, 13 and 17 on the SOP). All four pins must be externally connected to the appropriate pcb patterns. Also, the DIGITAL GND and ANALOG GND pins are not connected to each other internally.

2. Layout of the analog and digital sections should be separated to reduce interference from noise. To further guard against unwanted noise, it is recommended to bypass, as close as possible, the voltage supply pins to their respective ground pins with 1µF tantalum and 0.01µF ceramic disk capacitors in parallel.

3. The input capacitance of the analog input is much smaller than that of a typical flash A/D converter. It is necessary to use an amplifier with sufficient bandwidth and driving power. The analog input pins are separated internally, so they should be connected together externally. If the ADC-304 is driven with a low output impedance amplifier, parasitic oscillations may occur.

   These parasitic oscillations can be prevented by introducing a small resistance of 2 to 10Ω between the amplifier output and the ADC-304's A/D input. This resistance must have a very low value of series inductance at high frequencies.

   Note that each of the analog input pins is divided in this manner with these resistances. Connect the driving amplifier as close as possible to the A/D input of the ADC-304.

4. The voltage between V_T and V_B is equivalent to the dynamic range of the analog input. Bypass V_B to ANALOG GND USING a 1µF and a 0.01µF capacitor in parallel. To balance the characteristics of the ADC-304 at high frequencies, bypass V_M with a 0.01µF capacitor to ANALOG GND.

   Also, V_M can be used as a trimming pin for more precise linearity compensation. A stable voltage source with a potential equal to V_B and a 1kΩ potentiometer can be connected to V_M as shown in Figure 2 for this purpose.

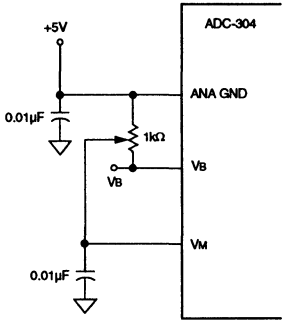
5. Separate the clock input, CLOCK, from other leads as much as possible, observing proper EMI and RFI wiring techniques. This reduces the inductive pick-up of this lead from interfering with the "clean" operation of the ADC-304.

6. The analog input signal is sampled on the positive-going edge of CLOCK. Corresponding digital data appears at the output on the negative-going edge of the CLOCK pulse after a brief delay of 31ns maximum (TDLH, TDHL). Refer to the Timing Diagram (Figure 3) for more information.

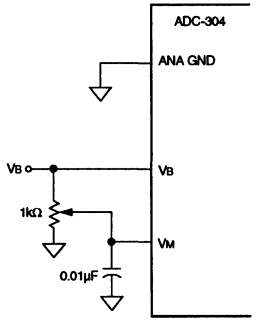
7. Connect all free pins to ANALOG GND to reduce unwanted noise.

   The analog input range is equal to a 2V spread. The voltage on V_T-V_B will equal 2V. The connection of V_T and ANALOG GND is 2V higher than V_B. Whether using a single or dual power supply, the analog input will range from the value of V_T to V_B. If V_T equals +5V, then V_B will equal +3V and the analog input range will be from +3 to +5V.

2



SINGLE SUPPLY OPERATION



DUAL SUPPLY OPERATION

Figure 2.
Improving Linearity Compensation

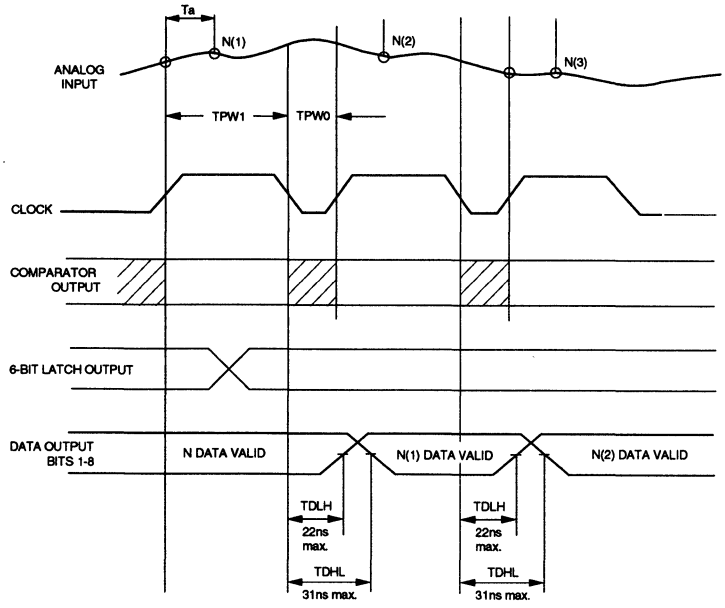


Figure 3. ADC-304 Timing Diagram

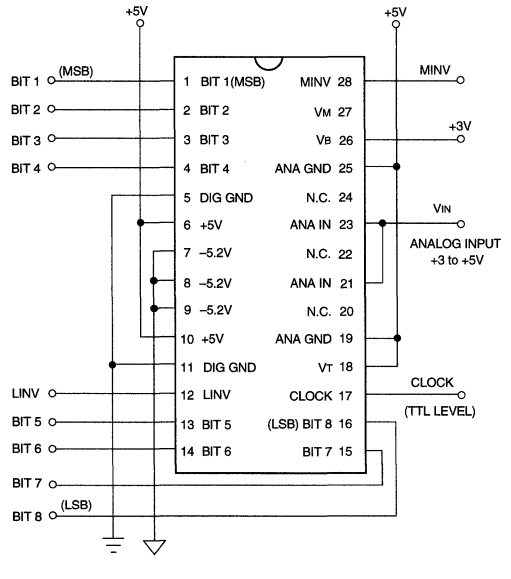
Table 1. Output Coding for +5V Power Supply Operation (+3 to +5V Signal Input)

		Straight Binary	Complementary Two's Complement	Two's Complement	Complementary Binary
Unipolar Scale	MINV	0	0	1	1
	LINV	0	1	0	1
+FS – 1SLB	+4.9922V	11111111	10000000	01111111	00000000
+7/8FS	+4.7500V	11011111	10100000	01011111	00100000
+3/4FS	+4.5000V	10111111	11000000	00111111	01000000
+1/2FS	+4.0000V	01111111	00000000	11111111	10000000
+1/4FS	+3.5000V	00111111	01000000	10111111	11000000
+1/8FS	+3.2500V	00011111	01100000	10011111	11100000
+1LSB	+3.0078V	00000001	01111110	10000001	11111110
Zero	+3.0000V	00000000	01111111	10000000	11111111

Table 2. Output Coding for ±5V Power Supply Operation (0 to –2V Signal Input)

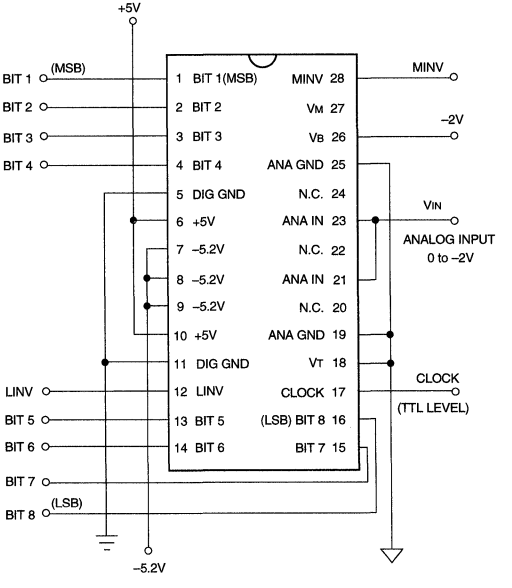
		Straight Binary	Complementary Two's Complement	Two's Complement	Complementary Binary
Unipolar Scale	MINV	0	0	1	1
	LINV	0	1	0	1
Zero	0.0000V	11111111	10000000	01111111	00000000
–1LSB	–0.0078V	11111110	10000001	01111110	00000001
–1/8FS	–0.2500V	11011111	10100000	01011111	00100000
–1/4FS	–0.5000V	10111111	11000000	00111111	01000000
–1/2FS	–1.0000V	01111111	00000000	11111111	10000000
–3/4FS	–1.5000V	00111111	01000000	10111111	11000000
–7/8FS	–1.7500V	00011111	01100000	10011111	11100000
–FS + 1SLB	–1.9922V	00000000	01111111	10000000	11111111

APPLICATION CIRCUITS



NOTE: 28-pin DIP package shown

Figure 4. Connections for +5V Power Supply Operation



NOTE: 28-pin DIP package shown

Figure 5. Connections for ±5V Power Supply Operation

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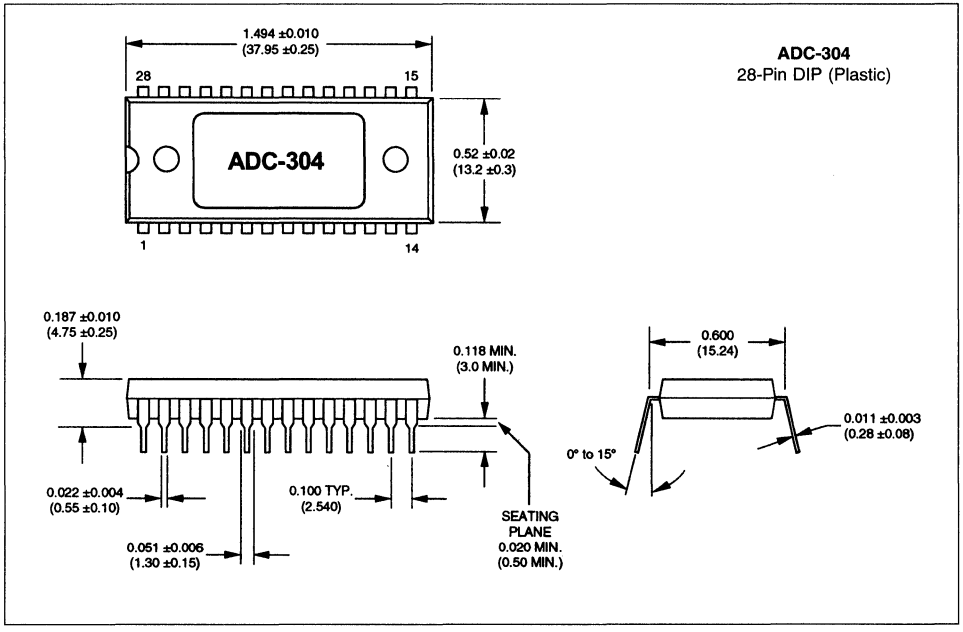
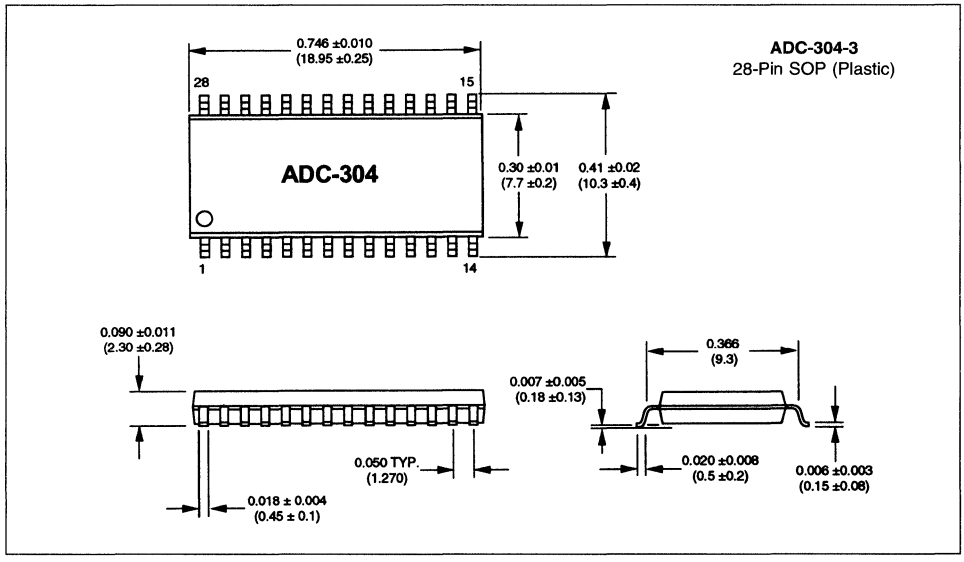
MECHANICAL DIMENSIONS





ORDERING INFORMATION

MODEL	PACKAGE
ADC-304	28-pin DIP (plastic)
ADC-304-3	28-pin SOP (plastic)

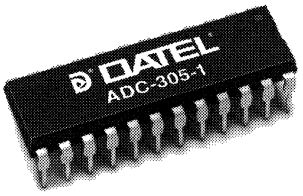
ADC-305

8-Bit, 20MHz, Low-Power Video A/D Converters

DATEL® INNOVATION and EXCELLENCE

FEATURES

- **8-bit resolution**
- **20MHz conversion rate**
- **±1/2LSB nonlinearity**
- **Built-in S/H circuit**
- **Low power consumption (60mW)**
- **TTL compatibile**
- **Single-supply operation (+5V)**



GENERAL DESCRIPTION

DATEL's ADC-305 is an 8-bit, 20MHz CMOS analog-to-digital converter using a 2-step parallel conversion technique.

Its main features include a low power dissipation of only 60mW at a 20MHz conversion rate. This monolithic silicon-gate CMOS IC operates from a single +5V supply. The technology used allows operation up to and beyond the minimum specified conversion rate without the need of an external sample-hold.

Another novel feature allows the self generation of reference voltages via pins V_{TS} and V_{BS}. The ADC-305 is supplied in a 24-pin plastic DIP or SOP package and operates over a –20 to +75°C temperature range. Storage temperature ranges from –55 to +150°C.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{OUTPUT ENABLE}}$ ($\overline{\text{OE}}$)	24	DIGITAL GROUND
2	DIGITAL GROUND	23	V_B
3	BIT 8 (LSB)	22	V_{BS}
4	BIT 7	21	ANALOG GROUND
5	BIT 6	20	ANALOG GROUND
6	BIT 5	19	ANALOG INPUT
7	BIT 4	18	+5V ANALOG SUPPLY
8	BIT 3	17	V_T
9	BIT 2	16	V_{TS}
10	BIT 1 (MSB)	15	+5V ANALOG SUPPLY
11	+5V DIGITAL SUPPLY	14	+5V ANALOG SUPPLY
12	CLOCK INPUT	13	+5V DIGITAL SUPPLY

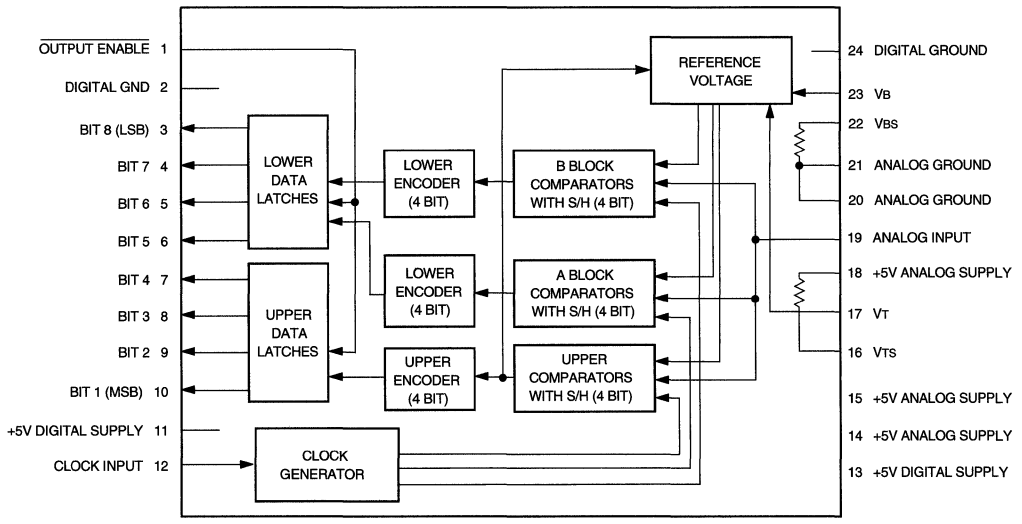


Figure 1. Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

PARAMETERS	LIMITS	UNITS
Supply Voltage (+Vs)	+7	Volts
Reference Voltage (V_T, V_B)	+Vs to GND	Volts
Analog Input Voltage (V_{IN})	+Vs to GND	Volts
Digital Input Voltage (CLOCK)	+Vs to GND	Volts
Digital Output Voltage (V_{OH}, V_{OL})	+Vs to GND	Volts

FUNCTIONAL SPECIFICATIONS

(Typical at T_A = +25°C, +V_S = +5.0V, V_T = +2.6V, V_B = +0.6V, and f_S = 20MHz unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	V_B	+0.6 to +2.6	V_T	Volts
Input Capacitance	—	11	—	pF
Offset Voltage				
V_T	–10	–35	–60	mV
V_B	0	+15	+45	mV
DIGITAL INPUTS				
Input Voltage				
V_{IH}	+4.0	—	—	Volts
V_{IL}	—	—	+1.0	Volts
Input Current				
I_{IH}	—	—	+5	µA
I_{IL}	—	—	–5	µA
PERFORMANCE				
Conversion Rate	20	35	—	MHz
Integral Nonlinearity	—	±0.5	±1.3	LSB
Differential Nonlinearity	—	±0.3	±0.5	LSB
Differential Gain Error	—	1.0	—	%
Differential Phase Error	—	0.5	—	deg.
SNR & Distortion(V_{IN} = Full Scale, f_S = 20MHz, f_{IN} = 1MHz)	—	46	—	dB
Input Signal Bandwidth Full Scale (–3dB)	—	60	—	MHz
Aperture Uncertainty	—	30	—	ps
Aperture Delay, Ta	—	4	—	ns
Clock Pulse Width				
T_{PW1}	25	—	—	ns
T_{PW0}	25	—	—	ns
OUTPUTS				
Output Coding	See Table 1			
Output Voltage	3-State TTL compatible			
Output Current				
I_{OH}	–1.1	—	—	mA
I_{OL}	+3.7	—	—	mA
Resolution	—	8	—	Bits
Data Delay, Td	—	18	30	ns
REFERENCE				
Reference Input Voltage				
V_B	0 and above			Volts
V_T	+2.8 and below			Volts
Reference Pin Current	4.5	6.6	8.7	mA
Reference Resistance				
V_T to V_B	230	300	450	Ω
Self Bias 1 ①				
V_B	+0.60	+0.64	+0.68	Volts
$V_T - V_B$	+1.96	+2.09	+2.21	Volts
Self Bias 2 ②				
V_T	+2.25	+2.39	+2.53	Volts

Footnotes:

① Short V_B to V_{BS}. Short V_T to V_{TS}. ② Short V_T to V_{TS}. V_B = analog ground.

POWER SUPPLY	MIN.	TYP.	MAX.	UNITS
Supply Voltage				
+Vs	+4.75	+5.0	+5.25	Volts
+Is	—	+12	+17	mA
Dig Gnd - Ana Gnd	—	0 to 100	—	mV
Power Dissipation	—	60	90	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temperature	–20 to +75			°C
Storage Temperature	–55 to +150			°C

TECHNICAL NOTES

1. To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog +5V pins, use a ceramic capacitor of about 0.1µF set as close as possible to the pin to bypass to the respective GND's.
2. The guaranteed sampling rate of the ADC-305 is 20MHz min. It is, however, not recommended to use sampling rates below 500kHz since this will cause too much droop. This is due to the fact that each pair of the internal 4-bit lower comparator groups with S/H work alternately, i.e., one group is in hold mode while the other one is in conversion mode.
3. Compared with a traditional flash type A/D converter, the input capacitance of the analog input is very small. However, it is necessary to drive the input with an amplifier featuring sufficient bandwidth and driving capability. When driving with an amplifier of low output impedance, parasitic oscillations may occur. This may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and the A/D input.
4. The voltage between V_T and V_B determines the dynamic range of the analog input. Stable characteristics are obtained by bypassing V_T and V_B pins to GND using 0.1µF capacitors. By shorting V_T to V_{TS} and V_B to V_{BS}, the self bias function generates +2.6V on V_T and +0.6V on V_B.
5. The analog input is sampled with the falling edge of the clock. Following a delay of 2.5 clock cycles, the digital data is output on the rising edge of the clock. The delay from the clock rising edge to the data output is about 18ns.
6. By connecting $\overline{OE}$ (pin 1) to GND, output enable is obtained. Connecting to +5V will disable the output.
7. The clock line wiring should be as short as possible. To avoid any interference with other signals, it should also be separated from other circuits.
8. The analog and digital supplies should be from a common source. This is to avoid latch up due to a possible voltage difference between supplies when power is turned on.

Table 1. Digital Output Coding

INPUT	CODE	STEP DEC	STEP HEX	DATA BITS OUT MSB	DATA BITS OUT LSB
V_B	Zero	0	00	0000	0000
	↓	↓	↓	↓	↓
↓	+1/2FS–1LSB	127	7F	0111	1111
	+1/2FS	128	80	1000	0000
	↓	↓	↓	↓	↓
V_T	+FS	255	FF	1111	1111

THEORY OF OPERATION

(See Functional Block Diagram, Figure 1, and Timing Chart, Figure 4)

1. The DATEL ADC-305 is a 2-step parallel A/D converter featuring a 4-bit upper comparator group and two 4-bit lower comparator groups, each with built-in sample and hold. A reference voltage equal to the voltage between $(V_T–V_B)/16$ is constantly applied to the 4-bit upper comparator block. A voltage corresponding to the upper data is fed through the reference supply to the lower data. V_{TS} and V_{BS} pins provde the self generation function for V_T (reference voltage top) and V_B (reference voltage bottom) voltages.

2. This converter uses an offset cancelation type comparator and operates synchronously with the external clock. It features various operating modes which are shown in the Timing Chart (Figure 4) by the symbols S, H and C. These characters stand for Input **S**ampling (Auto Zero) Mode, Input **H**old Mode and **C**omparison Mode.

3. The operation of the respective parts is as indicated in the chart. For instance, input voltage N(1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block. Input voltage N(2) is sampled with the falling edge of the second clock by means of the upper comparator block and lower comparator B block. The upper comparator block finalizes comparison data MD(1) with the rising edge of the second clock. Simultaneously the reference supply generates the lower reference voltage RV(1) that corresponds to the upper results. The lower comparator block finalizes comparison data LD(1) with the rising edge of the third clock. MD(1) and LD(1) are combined and routed to the output as Out(1) with the rising edge of the fourth clock. Thus there is a 2.5 clock delay from the analog input sampling point to the digital data output.

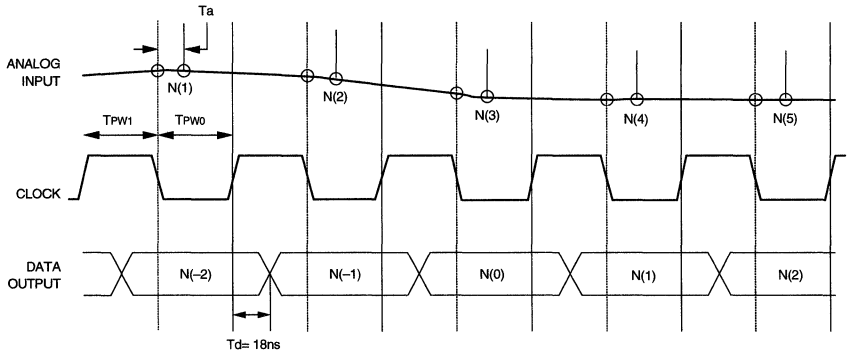

Figure 2. Timing Diagram

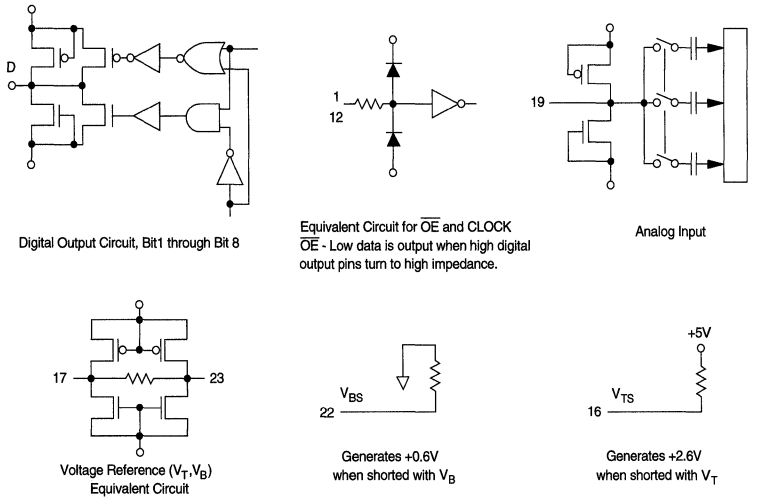

Figure 3. Equivalent Circuits

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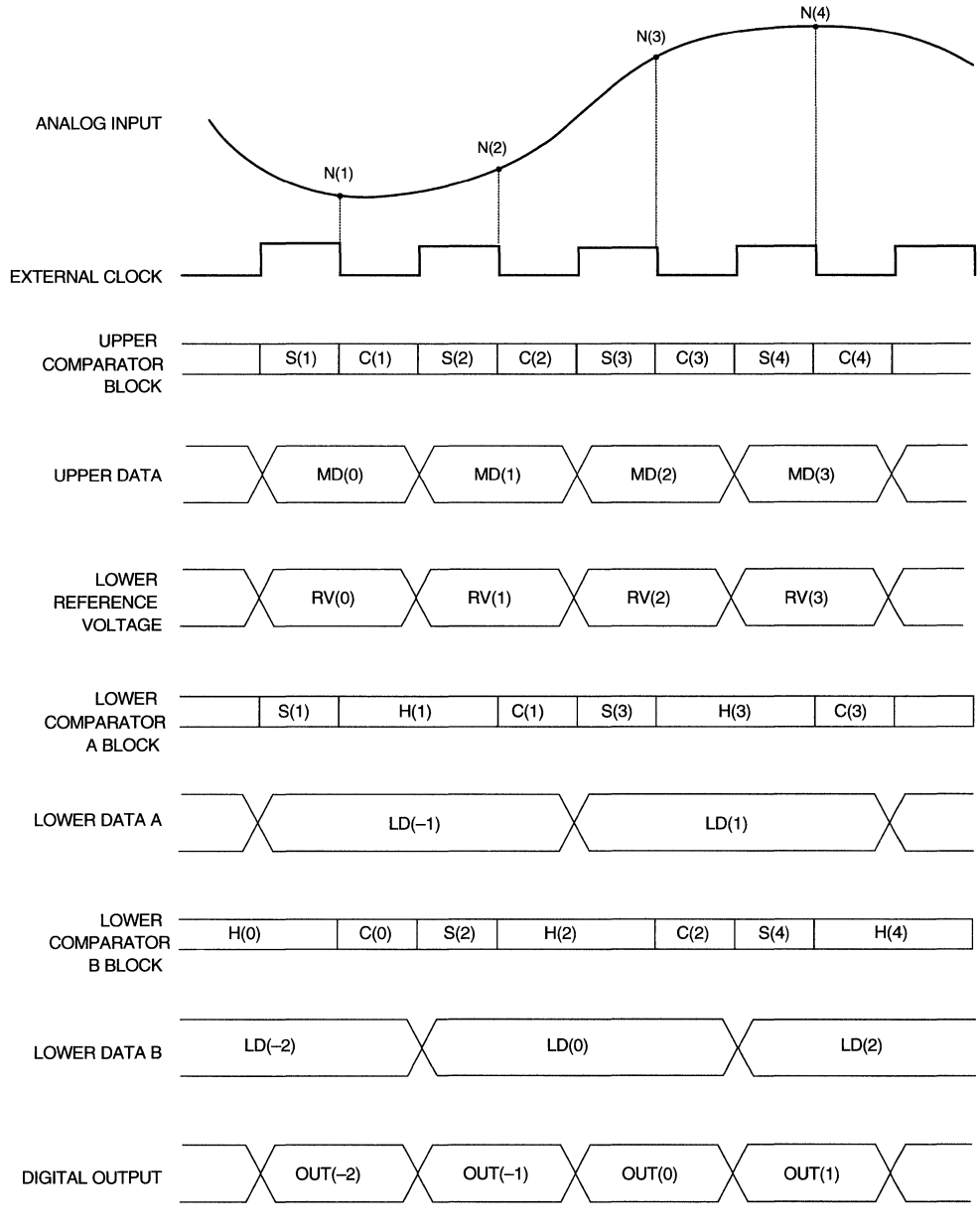
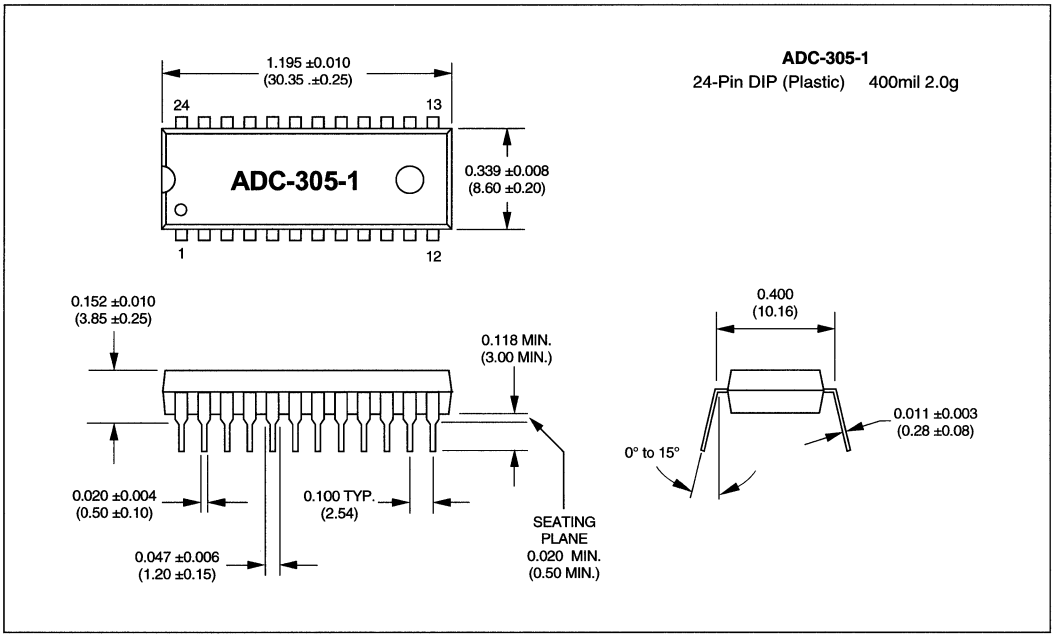


Figure 4. Timing Chart

MECHANICAL DIMENSIONS



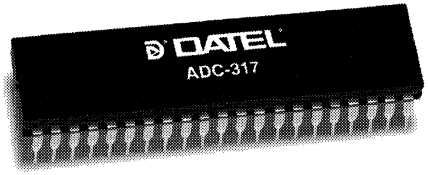
ORDERING INFORMATION

MODEL NUMBER	PACKAGE
ADC-305-1	24-Pin Plastic DIP
ADC-305-3	24-Pin Plastic SOP

ADC-317
8-Bit, 125MHz, Low-Power Flash A/D Converter

FEATURES

- **8-Bit resolution**
- **±1/2LSB integral and differential nonlinearity**
- **125MHz minimum conversion rate**
- **Low power consumption (870mW)**
- **Wide input bandwidth (200MHz)**
- **Low input capacitance (18pF)**
- **Single –5.2V supply**



GENERAL DESCRIPTION

DATEL's ADC-317 is an 8-bit, high-speed flash A/D converter capable of digitizing analog signals at a guaranteed rate of 125MHz. The ADC-317 is virtually free of sparkle code errors up to Nyquist conditions and has a built-in integral nonlinearity (INL) compensation circuit that keeps the INL at typically ±0.5LSB. The ADC-317 is available in a 42-pin, plastic, dual-in-line package and operates over the extended commercial temperature range of –20 to +75°C. The digital I/O levels of this A/D converter are compatible with ECL 100K/10KH/10K families.

Compared with earlier devices, the ADC-317's performance is superior due to the incorporation of advanced processing, new circuit design, and carefully considered layout.

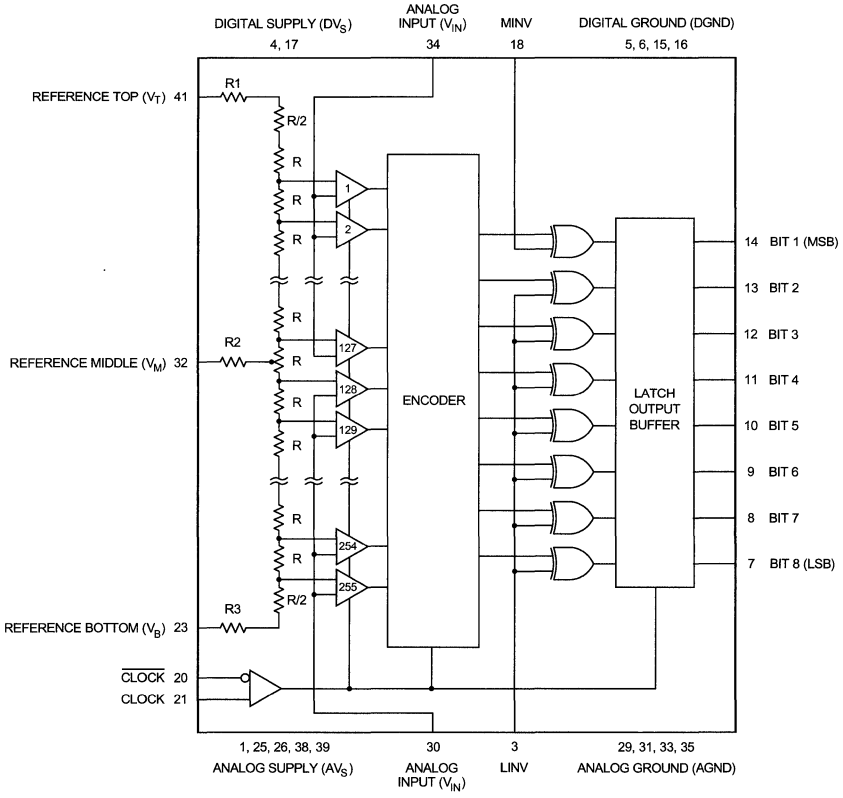


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
Supply Voltages AV_S, DV_S	+0.5 to –7	Volts
Input Voltage V_{IN}	+0.5 to –2.7	Volts
Reference Voltages V_T, V_B, V_M	+0.5 to –2.7	Volts
Reference Voltage $\|V_T - V_B\|$	2.5	Volts
Digital Inputs	+0.5 to –4	Volts
|Clock – $\overline{\text{Clock}}$|	2.7	Volts
V_M Input Current	–3 to +3	mA
Digital Output Currents	0 to –30	mA

FUNCTIONAL SPECIFICATIONS

(Specifications are typical at T_A = +25°C, AVs = DVs = –5.2V, V_T = 0V, V_B = –2.0V, f_S = 125MHz unless otherwise specified.)

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Input Voltage	—	0 to –2	—	Volts
Analog Input Capacitance				
(V_{IN} = –1V + 0.07Vrms)	—	18	—	pF
Analog Input Resistance	50	190	—	kΩ
Analog Input Bias Current				
(V_{IN} = –1V)	+20	+130	+400	µA
Digital Input Voltage				
V_H	–1.13	—	—	Volts
V_L	—	—	–1.50	Volts
Digital Input Current				
I_H (@ V_H = –0.8V)	0	—	+50	µA
I_L (@ V_L = –1.6V)	–50	—	+50	µA
Digital Input Capacitance	—	7	—	pF
Clock Pulse Width				
T_{PW1}	3.8	—	—	ns
T_{PW0}	3.8	—	—	ns
REFERENCE INPUTS				
Reference Input Voltage ①				
V_B	–2.2	–2.0	–1.8	Volts
V_T	–0.1	0	+0.1	Volts
Reference Resistance, V_T to V_B	75	110	155	Ω
Offset Voltage				
V_B	0	+9	+24	mV
V_T	–8	–17	–32	mV
PERFORMANCE				
Resolution	8	—	—	Bits
Conversion Rate	125	160	—	MHz
Integral Non-linearity	—	±0.5	±0.8	LSB
Differential Non-linearity	—	±0.5	±0.7	LSB
Differential Gain Error	—	1.0	—	%
Differential Phase Error	—	0.5	—	deg.
Aperture Jitter (Tj)	—	10	—	ps
Sampling Delay (Tsd)	0.3	1.5	3.0	ns
DYNAMIC CHARACTERISTICS ②				
Full Scale Input Bandwidth				
V_{IN} = 2V peak-to-peak				
Bandwidth (@ –3dB)	200	—	—	MHz
Signal-to-Noise Ratio				
Input = 1MHz, FS	—	46	—	dB
Input = 31.249MHz, FS	—	40	—	dB
Error Rate				
Input = 31.249MHz, FS				
(Error = 16 LSB min.)	—	10^{-14}	10^{-9}	TPS ③

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Digital Output ④				
Logic High Level	–1.10	—	—	Volts
Logic Low Level	—	—	–1.62	Volts
Output Delay (Td)	3.0	3.6	4.2	ns
Output Rise Time (Tr)	0.5	0.9	1.2	ns
Output Fall Time (Tf)	0.5	1.0	1.3	ns
POWER REQUIREMENTS				
Supply Voltage AV_S, DV_S	–4.95	–5.2	–5.5	Volts
Supply Current	—	–160	–230	mA
Power Dissipation	—	870	—	mW
DGND - AGND	—	—	±50	mV
AV_S - DV_S	—	—	±50	mV
PHYSICAL/ENVIRONMENTAL				
Operating Temperature, Ambient	–20	—	+75	°C
Storage Temperature	–65	—	+150	°C
Thermal Impedance, θja	—	62	—	°C/W
Package	42-pin plastic DIP			
Weight	0.23 ounces (6.4 grams)			

Footnotes:

① Refer to Functional Block Diagram, Figure 1.
② For conversion rate of 125MHz.
③ TPS = Times per sample. Each unit is production tested for 10 seconds.
④ 220Ω pull-down resistors required on digital outputs.

TECHNICAL NOTES

1. Even with its low input capacitance of 18pF, the ADC-317 still requires an input amplifier with good drive capability. The amplifier will require wide bandwidth and high slew rate (±250V/µs typical) to take full advantage of the converter's input bandwidth.

2. The input impedance of the A/D is primarily capacitive which may result in the input amplifier becoming unstable and causing oscillations. Stop oscillations by placing a 2-to-4Ω resistor between the amplifier and the converter's input.

3. CLOCK and $\overline{\text{CLOCK}}$ (ECL) are usually differentially driven. The ADS-317 is operable without $\overline{\text{CLOCK}}$ input, but using complementary inputs is recommended to obtain stable high-speed performance.

4. The polarity of the output data is controlled by input MINV, which controls the MSB alone, and LINV, which controls bits 2 through 8 (LSB). The combination of "0" and "1" on these inputs offer the user various code options shown in Table 1. Leave the inputs open for a logic level "0"; connect a 3.9kΩ resistor to GND for logic level "1".

5. Digital output bits 1 through 8 require 220Ω pull-down resistors connected to the negative supply rail. Refer to Figure 2.

6. The reference voltage range (–2.0V to 0V typical) determines the dynamic range of the input voltage. Adjustments to this range can be made within the range of V_B = –2 ±0.2V and V_T = 0V ±0.1V. The reference input V_B should be decoupled to GND using 1µF and 0.01µF capacitors. Improvement in the high-frequency stability can be achieved by decoupling terminal V_M using a 0.01µF capacitor.

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7. The V_M input (pin 32) is used to achieve a more accurate linearity than that specified. The connection diagram shows an external circuit designed to maximize the ADC-317's linearity.

8. Tie all pins not being used to ground.

9. Substantial analog and digital ground planes must be provided. It is recommended that these ground planes are taken to a common point, the power ground plane, as close to the ADC as possible.

10. The analog and digital power supply inputs (–5.2V) are internally connected through a resistance of 4 to 6 Ohms, and it is possible to use one power source for both inputs. For best performance, the power supplied to the analog and digital inputs (–5.2V) should be supplied from separate, isolated power supplies. If one of the power supplies fails or is shorted to ground for more than 1 second, the device may be destroyed. Both –5.2V lines should be decoupled using 1µF and 0.01µF capacitors located as close to the pins as possible.

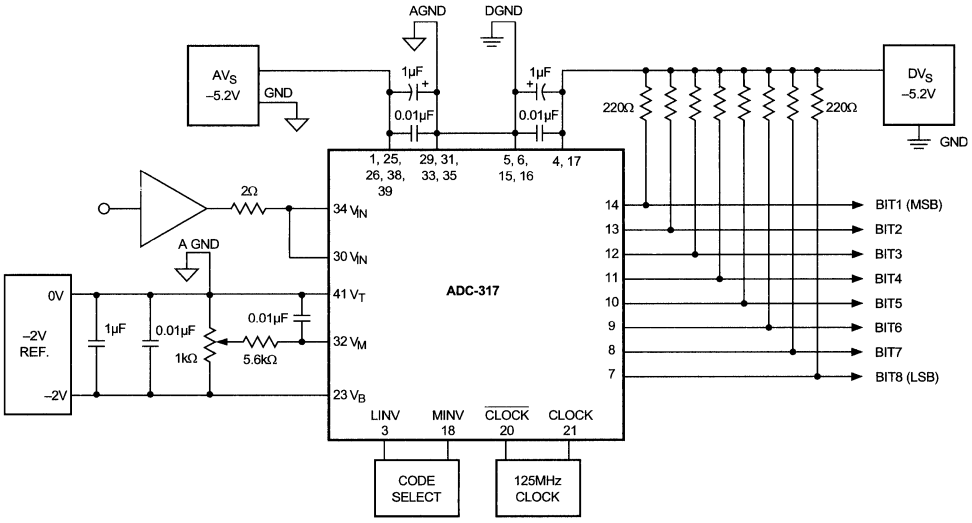

Figure 2. ADC-317 Typical Connection Drawing

Table 1. Digital Output

This table and the Timing Diagram indicate the compatibility between the analog input and the digital output code.

	MINV	1	0	1	0
V_{IN}	LINV	1	1	0	0
0.0000V		000 . . . 00	100 . . . 00	011 . . . 11	111 . . . 11
–0.0078V		000 . . . 01	100 . . . 01	011 . . . 10	111 . . . 10
–0.9922V		011 . . . 11	111 . . . 11	000 . . . 00	100 . . . 00
–1.0000V		100 . . . 00	000 . . . 00	111 . . . 11	011 . . . 11
–1.9844V		111 . . . 10	011 . . . 10	100 . . . 01	000 . . . 01
–1.9922V		111 . . . 11	011 . . . 11	100 . . . 00	000 . . . 00

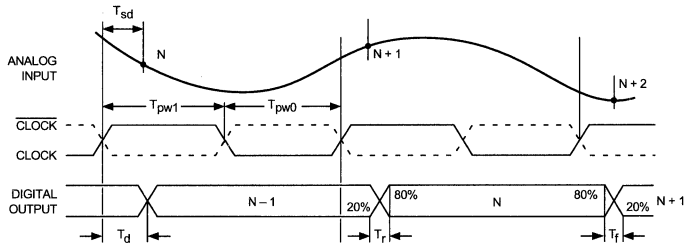

Figure 3. ADC-317 Simplified Timing Diagram

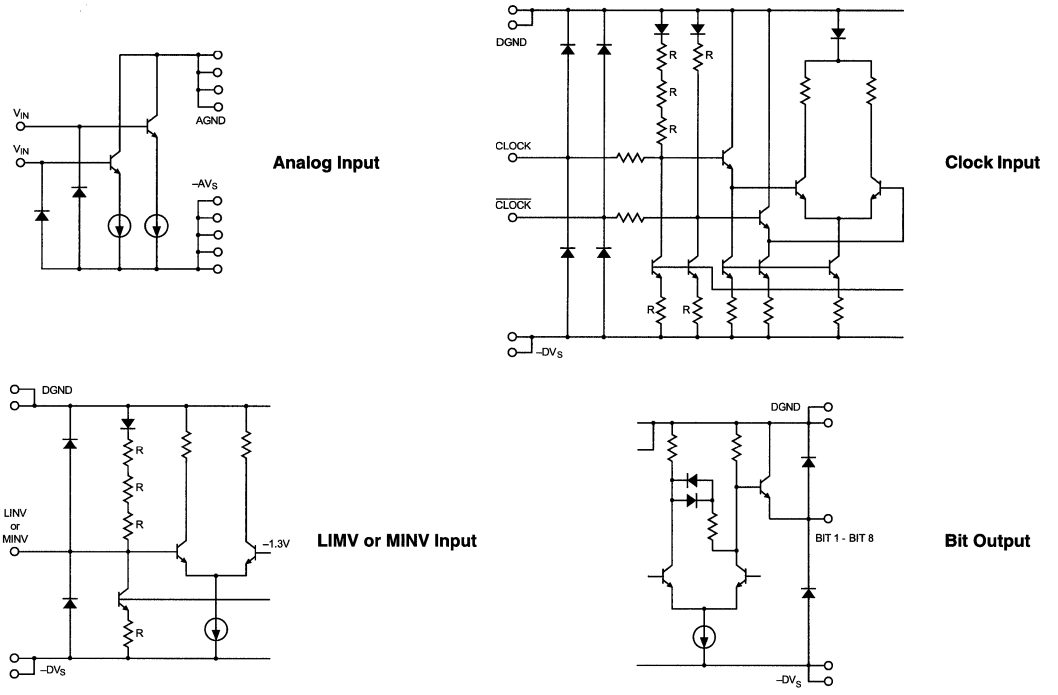

Figure 4. Equivalent Circuits

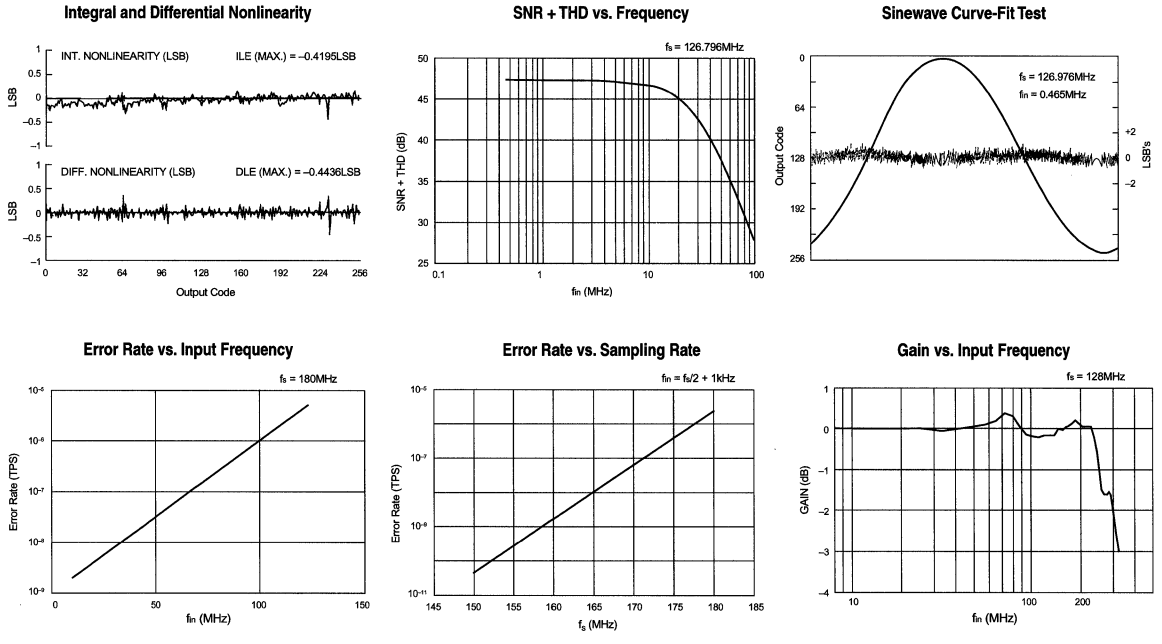

Figure 5. Typical Performance Curves

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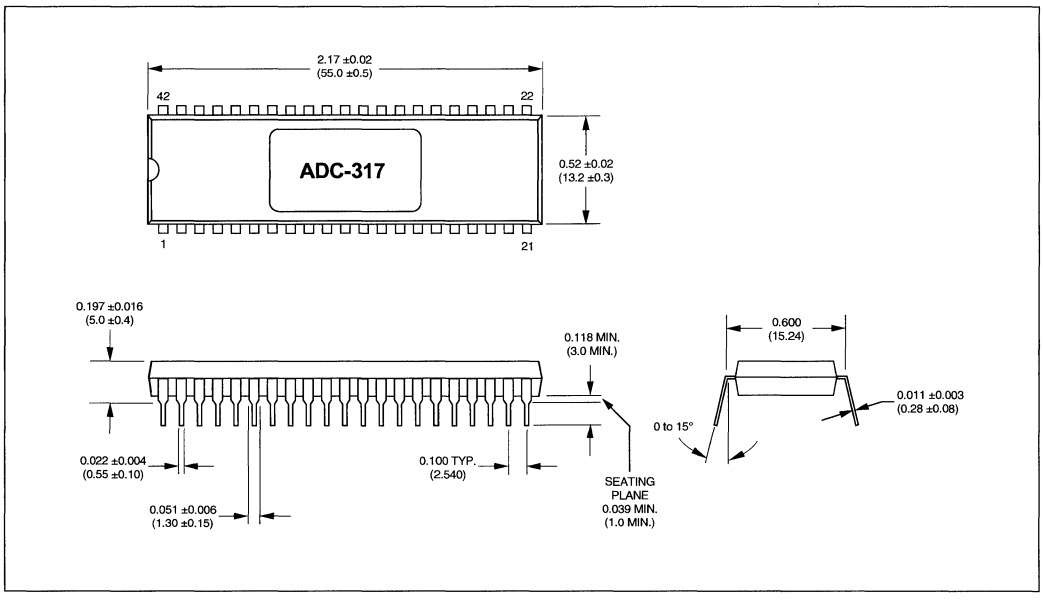
MECHANICAL DIMENSIONS
INCHES (mm)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG SUPPLY (AV_S)	42	NO CONNECTION
2	NO CONNECTION	41	REFERENCE TOP (V_T)
3	LINV	40	NO CONNECTION
4	DIGITAL SUPPLY (DV_S)	39	ANALOG SUPPLY (AV_S)
5	DIGITAL GROUND	38	ANALOG SUPPLY (AV_S)
6	DIGITAL GROUND	37	NO CONNECTION
7	BIT 8 (LSB)	36	NO CONNECTION
8	BIT 7	35	ANALOG GROUND
9	BIT 6	34	ANALOG INPUT (V_{IN})
10	BIT 5	33	ANALOG GROUND
11	BIT 4	32	REF. MIDDLE (V_M)
12	BIT 3	31	ANALOG GROUND
13	BIT 2	30	ANALOG INPUT (V_{IN})
14	BIT 1 (MSB)	29	ANALOG GROUND
15	DIGITAL GROUND	28	NO CONNECTION
16	DIGITAL GROUND	27	NO CONNECTION
17	DIGITAL SUPPLY (DV_S)	26	ANALOG SUPPLY (AV_S)
18	MINV	25	ANALOG SUPPLY (AV_S)
19	NO CONNECTION	24	NO CONNECTION
20	$\overline{\text{CLOCK}}$	23	REF. BOTTOM (V_B)
21	CLOCK	22	NO CONNECTION

ORDERING INFORMATION

ADC-317	8-Bit, 125MHz Low-Power Flash A/D Converter

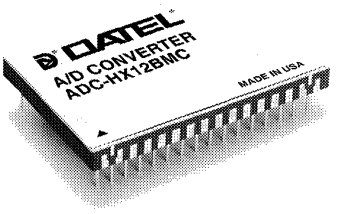
ADC-HX, ADC-HZ Series

12-Bit, 8 and 20µsec Analog-to-Digital Converters

DATEL®
INNOVATION and EXCELLENCE

FEATURES

- **12-bit resolution**
- **8 or 20 microsecond conversion times**
- **5 input voltage ranges**
- **Internal high Z input buffer**
- **Short-cycle operation**
- **MIL-STD-883 models available**



GENERAL DESCRIPTION

The ADC-HX and ADC-HZ Series are self-contained, high-performance, 12-bit A/D converters manufactured with thick and thin-film hybrid technology. They use the successive approximation conversion technique to achieve a 12-bit conversion in 20 and 8 microseconds, respectively. Five input voltage ranges are programmable by external pin connection. An internal buffer amplifier is also provided for applications in which 50 megohm input impedance is required.

These converters utilize a fast 12-bit monolithic DAC which includes a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12-bit successive approximation register, a clock and a monolithic buffer amplifier. Nonlinearity is specified at ±1/2LSB maximum.

Both models have identical operation except for conversion speed. They can be short-cycled to give faster conversions in lower-resolution applications. Use of the internal buffer amplifier increases conversion time by 3 microseconds, the settling time of the amplifier. Output coding is complementary binary, complementary offset binary, or complementary two's complement. Serial data is also brought out. The package is a 32-pin ceramic TDIP. Models are available for use in either commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges. MIL-STD-883 and DESC Standard Military Drawing models are also available.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	32	SERIAL DATA OUTPUT
2	BIT 11	31	–15V POWER
3	BIT 10	30	BUFFER INPUT
4	BIT 9	29	BUFFER OUTPUT
5	BIT 8	28	+15V POWER
6	BIT 7	27	GAIN ADJUST
7	BIT 6	26	ANALOG COMMON
8	BIT 5	25	20V INPUT RANGE
9	BIT 4	24	10V INPUT RANGE
10	BIT 3	23	BIPOLAR OFFSET
11	BIT 2	22	COMPARATOR INPUT
12	BIT 1 (MSB)	21	START CONVERT
13	BIT 1 ($\overline{\text{MSB}}$)	20	E.O.C. (STATUS)
14	SHORT CYCLE	19	CLOCK OUT
15	DIGITAL COMMON	18	REFERENCE OUT
16	+5V POWER	17	CLOCK RATE

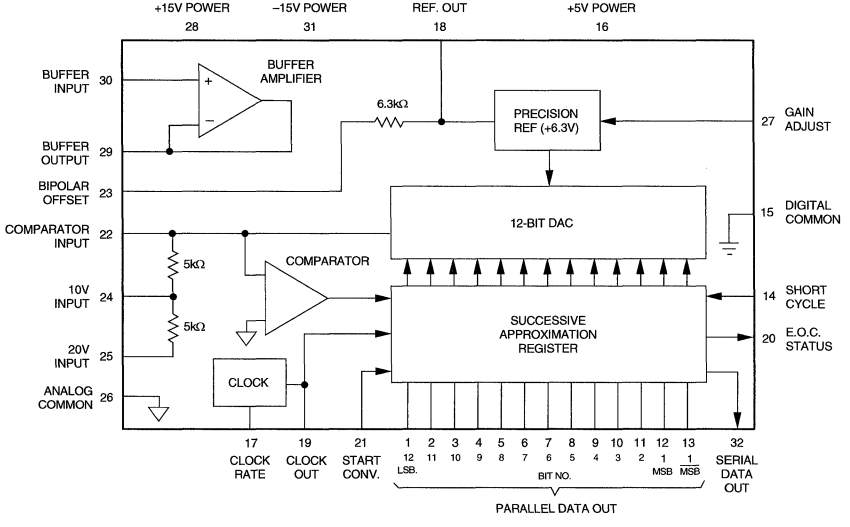


Figure 1. Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply, Pin 28	+18	Volts
–15V Supply, Pin 31	–18	Volts
+5V Supply, Pin 16	+7	Volts
Digital Inputs, Pins 14, 21	±5.5	Volts
Analog Inputs, Pins 24, 25	±25	Volts
Buffer Input, Pin 30	±15	Volts
Lead Temperature (10 seconds)	300	°C

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V and +5V supplies unless otherwise noted)

INPUTS	ADC-HX12B	ADC-HZ12B
Analog Input Ranges		
Unipolar	0 to +5V, 0 to +10V	
Bipolar	±2.5V, ±5V, ±10V	
Input Impedance	2.5k (0 to +5V, ±2.5V) 5k (0 to +10V, ±5V) 10k (±10V)	
Input Impedance with Buffer	50 megohms	
Input Bias Current of Buffer	125nA typical, 250nA max.	
Start Conversion	+2V min. to +5.5V max. positive pulse with duration of 100ns min. Rise and fall times <30ns. Logic "1" to "0" transition resets converter and initiates next conversion. Loading: 2 TTL loads.	
PERFORMANCE		
Resolution	12 bits	
Nonlinearity	±1/2LSB max.	
Differential Nonlinearity	±3/4LSB max.	
Accuracy Error ①		
Gain (before adjustment)	±0.2%	
Zero, Unipolar (before adj.)	±0.1% of FSR ②	
Offset, Bipolar (before adj.)	±0.2% of FSR ②	
Temperature Coefficient		
Gain	±20ppm/°C max.	
Zero, Unipolar	±5ppm/°C of FSR max. ②	
Offset, Bipolar	±10ppm/°C of FSR max. ②	
Diff. Nonlinearity Tempco	±2ppm/°C of FSR max. ②	
No Missing Codes	Over opererating temperature range	
Conversion Time ③		
12 Bits	20µs max.	8µs max.
10 Bits ④	15µs max.	6µs max.
8 Bits ④	10µs max.	4µs max.
Buffer Settling Time (10V step)	3µs to ±0.01%	
Power Supply Rejection	±0.004%/% supply max.	
OUTPUTS ⑤		
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V	
Unipolar Coding	Complementary binary	
Bipolar Coding	Complementary offset binary Complementary two's complement	
Serial Output Data	NRZ successive decision pulses out, MSB first. Compl. binary or compl. offset binary coding.	
End of Conversion (Status)	Conversion status signal. Output is logic "1" during reset and conversion and logic "0" when conversion complete.	
Clock Output	Train of positive going +5V 100ns pulses. 600kHz for ADC-HX and 1.5MHz for ADC-HZ (pin 17 grounded).	
Internal Reference	+6.3V	
Reference Tempco	±20ppm/°C max.	
External Reference Current	2.5mA max.	

POWER REQUIREMENTS	
Power Supply Voltages	+15V ±0.5V at +20mA –15V ±0.5V at –25mA +5V ±0.25V at +85mA
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range, Case	0 to +70°C or –55 to +125°C
Storage Temperature Range	–65 to +150°C
Package Type	32-pin ceramic TDIP
Weight	0.5 ounces (14 grams)
Thermal Impedance	
θ_{JC}	6°C/W
θ_{JA}	30°C/W

Footnotes:

① Adjustable to zero.

② FSR is full scale range and is 10V for 0 to +10V or ±5V inputs and 20V for ±10V input, etc.

③ Without buffer amplifier used. ADC-HZ may require external adjustment of clock rate.

④ Short cycled operation.

⑤ All digital outputs can drive 2 TTL loads.

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a 0.01µF ceramic capacitor in parallel with a 1µF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 10µF electrolytic capacitor as shown in the connection diagrams. In addition, GAIN ADJUST (pin 27) should be bypassed to ground with a 0.01µF ceramic capacitor. These precautions will assure noise free operation of the converter.

2. DIGITAL COMMON (pin 15) and ANALOG COMMON (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V ground should be run to pin 15.

3. External adjustment of zero or offset and gain are made by using trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10k and 100k Ohms and should be 100ppm/°C cermet types. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8-bit short-cycled operation, external adjustment may not be necessary.

4. Short-cycled operation results in shorter conversion times when the conversion is truncated to less than 12 bits. This is done by connecting SHORT CYCLE (pin 14) to the output bit following the last bit desired. For example, for an 8-bit conversion, pin 14 is connected to the bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases, the clock rate is accelerated by connecting the CLOCK RATE adjust (pin 17) to +5V (10 bits) or +15V (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, as missing codes will result.

5. Note that output coding is complementary coding. For unipolar operation it is complementary binary, and for bipolar operation it is complementary offset binary or complementary two's complement. In cases in which bipolar coding of offset binary or two's complement is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of –1). The converter is then calibrated so that –FS analog input gives an output code of 0000 0000 0000, and +FS – 1LSB gives 1111 1111 1111.

6. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (pin 21). The rate of the external clock must be lower than the rate of the internal clock as adjusted (see Short Cycle Operation tables) for the converter resolution selected. The pulse width of the external clock should be between 100 and 300 nanoseconds. Each N-bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8-bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N-bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.

7. When the input buffer amplifier is used, a delay equal to its settling time must be allowed between the input level change, such as a multiplexer channel change, and the negative-going edge of the START CONVERT pulse. If the buffer is not required, BUFFER INPUT (pin 30) should be tied to ANALOG COMMON (pin 26). This prevents the unused amplifier from introducing noise into the converter. For applications not using the buffer, the converter must be driven from a source with an extremely low output impedance.

CODING TABLE UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING
0 to +10V	0 to +5V	MSB LSB
+9.9976V	+4.9988V	0000 0000 0000
+8.7500	+4.3750	0001 1111 1111
+7.5000	+3.7500	0011 1111 1111
+5.0000	+2.5000	0111 1111 1111
+2.5000	+1.2500	1011 1111 1111
+1.2500	+0.6250	1101 1111 1111
+0.0024	+0.0012	1111 1111 1110
0.0000	0.0000	1111 1111 1111

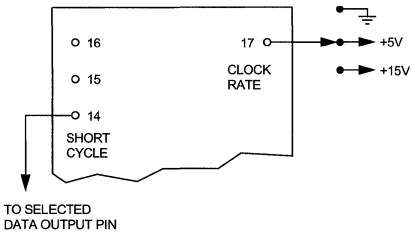
CODING TABLE BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY	COMP. TWO'S COMPLEMENT
±10V	±5V	±2.5V	MSB LSB	MSB LSB
+9.9951V	+4.9976V	+2.4988V	0000 0000 0000	1000 0000 0000
+7.5000	+3.7500	+1.8750	0001 1111 1111	1001 1111 1111
+5.0000	+2.5000	+1.2500	0011 1111 1111	1011 1111 1111
0.0000	0.0000	0.0000	0111 1111 1111	1111 1111 1111
–5.0000	–2.5000	–1.2500	1011 1111 1111	0011 1111 1111
–7.5000	–3.7500	–1.8750	1101 1111 1111	0101 1111 1111
–9.9951	–4.9976	–2.4988	1111 1111 1110	0111 1111 1110
–10.0000	–5.0000	–2.5000	1111 1111 1111	0111 1111 1111

SHORT CYCLE OPERATION

Refer to Technical Note 4 for methods of reducing the ADC-HX or ADC-HZ conversion times.

CONNECTIONS



CLOCK RATE VS. VOLTAGE

PIN 17 VOLTAGE	CLOCK RATE ADC-HX	CLOCK RATE ADC-HZ
0V	600kHZ	1.5MHZ
+5V	720kHZ	1.8MHz
+15V	880kHz	2.2MHz

8, 10 & 12-BIT CONVERSION TIMES

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-HX Conversion Time	20µs	15µs	10µs
ADC-HZ Conversion Time	8µs	6µs	4µs
Connect These Pins Together	17 & 15 14 & 16	17 & 16 14 & 2	17 & 28 14 & 4

PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO	RES. (BITS)	PIN 14 TO
1	PIN 11	7	PIN 5
2	PIN 10	8	PIN 4
3	PIN 9	9	PIN 3
4	PIN 8	10	PIN 2
5	PIN 7	11	PIN 1
6	PIN 6	12	PIN 16

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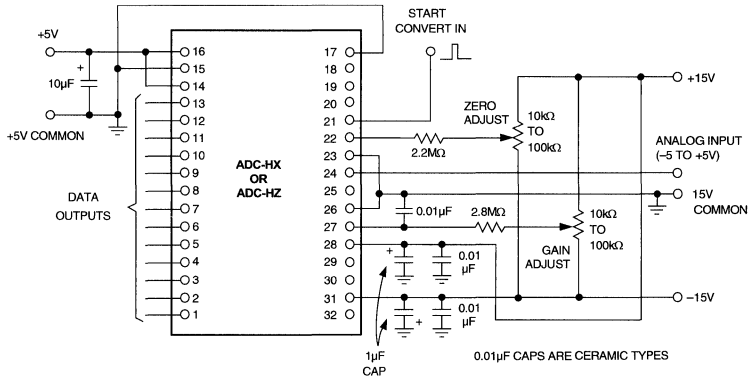


Figure 2. Bipolar Operation, –5 to +5V

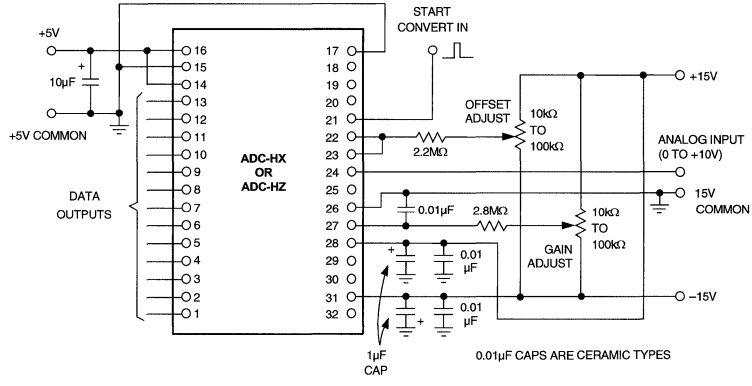


Figure 3. Unipolar Operation, 0 to +10V

CONNECTIONS AND CALIBRATION

INPUT CONNECTIONS

INPUT VOLTAGE RANGE	WITHOUT BUFFER			WITH BUFFER			
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER		
0 to +5V	24	22 & 25	23 & 26	30	22 & 25	23 & 26	29 & 24
0 to +10V	24	—	23 & 26	30	—	23 & 26	29 & 24
±2.5V	24	22& 25	23 & 22	30	22 & 25	23 & 22	29 & 24
±5V	24	—	23 & 22	30	—	23 & 22	29 & 24
±10V	25	—	23 & 22	30	—	23 & 22	29 & 25

CALIBRATION PROCEDURE

1. Connect the converter for bipolar or unipolar operation. Use the input connection table for the desired input voltage range and input impedance. Apply START CONVERT pulses of 100 nanoseconds minimum duration to pin 21. The spacing of the pulses should be no less than the maximum conversion time.

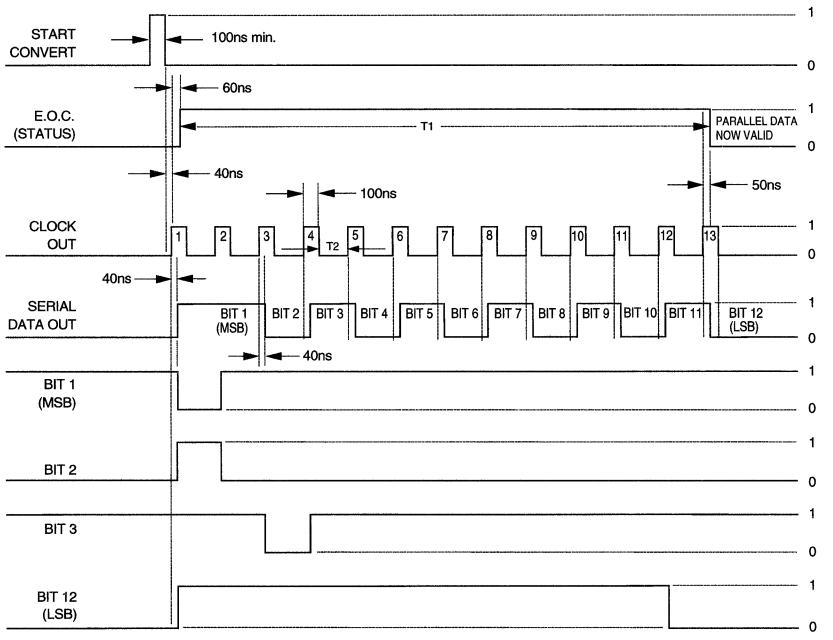
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero + 1/2LSB) or the bipolar offset adjustment (–FS + 1/2LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.

3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS – 1.5LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

CALIBRATION TABLE

	RANGE	ADJUST.	INPUT VOLTAGE
UNIPOLAR	0 to +5V	Zero Gain	+0.6mV +4.9982V
	0 to +10V	Zero Gain	+1.2mV +9.9963V
BIPOLAR	±2.5V	Offset Gain	–2.4994V +2.4982V
	±5V	Offset Gain	–4.9988V +4.9963V
	±10V	Offset Gain	–9.9976V +9.9927V

TIMING DIAGRAM FOR ADC-HX, ADC-HZ OUTPUT: 101010101010



TIMING DIAGRAM OPERATING PERIODS

	ADC-HX	ADC-HZ
T_1	20µs	8µs
T_2	1.56µs	0.56µs

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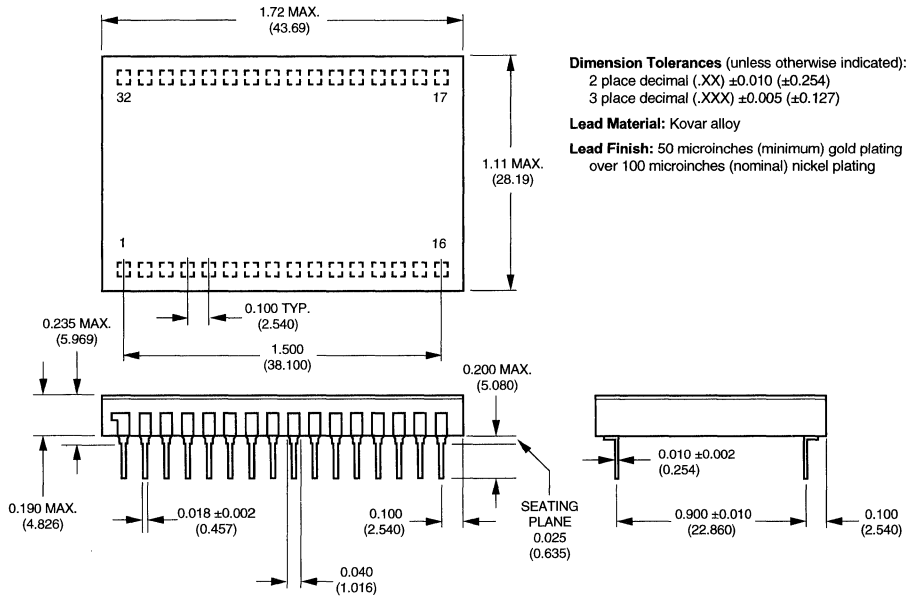
MECHANICAL DIMENSIONS
INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

2

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-HX12BGC	0 to +70°C
ADC-HX12BMC	0 to +70°C
ADC-HX12BMM	–55 to +125°C
ADC-HX12BMM-QL	–55 to +125°C
ADC-HX/883	–55 to +125°C
ADC-HZ12BGC	0 to +70°C
ADC-HZ12BMC	0 to +70°C
ADC-HZ12BMM	–55 to +125°C
ADC-HZ12BMM-QL	–55 to +125°C
ADC-HZ/883	–55 to +125°C

MIL-STD-883B units are available under DESC Drawing Number 5962-88508. Contact DATEL for 883 product specification.

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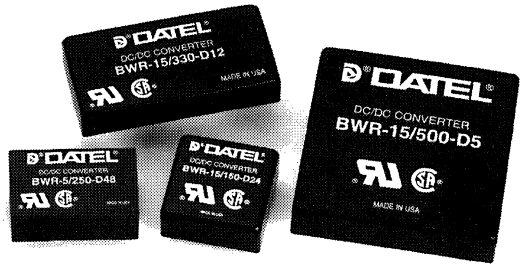

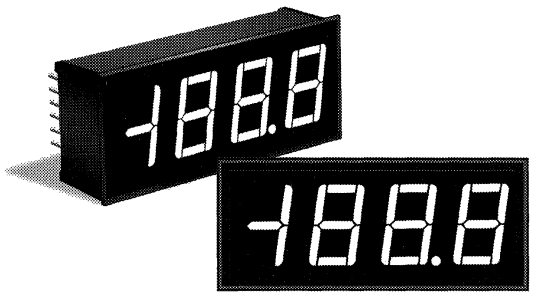

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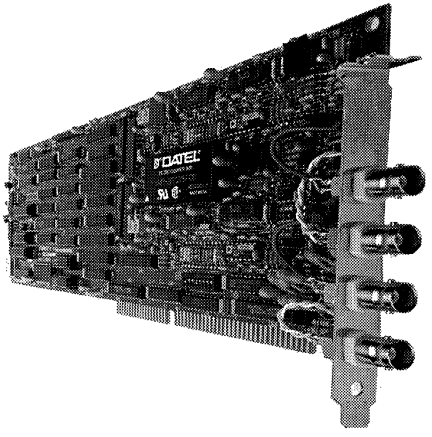
- COMM ports link directly to array processors
- Virtual Instruments:
  - Arbitrary waveform generators (2-16 channels)
  - Programmable power supplies
  - Power-supply test cards
- Windows and LabVIEW® bridge software



For literature or technical assistance

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or contact your local DATEL Sales Office or Representative

Sample-Hold Amplifiers

Table of Contents

Selection Guide

Model ①	Acquisition Time to ±0.01% (nsec)	Linearity (%)	Aperture Jitter (psec)	Input Range (Volts)	Gain	Small Signal Bandwidth (MHz)	Hold-Mode Droop Rate (µV/µsec)	Power Supplies (Volts)	Power Dissipation (mW)	Page
SHM-12	20	±0.01	1	±1.5	+1	120	±500	±5	250	**3-3**
SHM-14	25	±0.002	1	±2.5	+1	250	±2000	±5	250	**3-9**
SHM-43	25	±0.01	1	±1	+1	150	±1	±5, +15	545	**3-21**
SHM-49	160	±0.01	25	±10	–1	16	±0.5	+5, ±15	365	**3-27**
SHM-4860	160	±0.01	50	±10	–1	16	±0.5	+5, ±15	730	**3-24**
SHM-945	275 ②	±0.0004	10	±10	–1	16	±0.5	+5, ±15	305	**3-30**
SHM-30C	650	±0.01	100	±10	+1	4.5	±0.01	±15	735	**3-18**
MSH-840 ③	775	±0.01	15	±10	+1/10	13	±1.5	+5, ±15	2.25 ④	**3-33**
SHM-20C	1000	±0.01	300	±10	+1	2	±0.08	±15	330	**3-15**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① High-reliability screening available on all models except SHM-20C and SHM-30C.
② To ±0.003%.
③ The MSH-840 is a quad simultaneous S/H (SSH) with built-in output multiplexer.
④ Watts.

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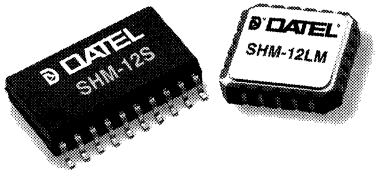
INNOVATION and EXCELLENCE

SHM-12
Ultra-Fast, 12-Bit Linear Monolithic Sample-Hold Amplifiers

FEATURES

- **Fast acquisition time:**
  - **10ns to ±0.1%**
  - **15ns to ±0.024%**
  - **20ns to ±0.012%**
- **±0.006% Nonlinearity**
- **65µVrms output noise**
- **120MHz small signal bandwidth**
- **55MHz full power bandwidth**
- **–80dB feedthrough**
- **1ps Aperture jitter**
- **250mW power dissipation**
- **Low cost**



3

INPUT/OUTPUT CONNECTIONS (CLCC and SOIC-20 Packages)

PIN	FUNCTION	PIN	FUNCTION
1	–5V SUPPLY	20	+5V SUPPLY
2	–5V SUPPLY	19	SAMPLE/$\overline{\text{HOLD}}$
3	NOT CONNECTED	18	$\overline{\text{SAMPLE}}$/HOLD
4	ANALOG INPUT	17	+5V SUPPLY
5	–5V SUPPLY	16	GROUND
6	DO NOT CONNECT	15	EXT. CAPACITOR
7	–5V SUPPLY	14	GROUND
8	DO NOT CONNECT	13	+5V SUPPLY
9	–5V SUPPLY	12	+5V SUPPLY
10	–5V SUPPLY	11	ANALOG OUTPUT

GENERAL DESCRIPTION

The SHM-12 is an extremely high-speed and accurate monolithic sample-and-hold amplifier designed for fast data acquisition applications. The SHM-12 is accurate (±1LSB at 12 bits over the full military temperature range) and is very fast (10ns and 15ns acquisition times to accuracies of 10 and 12-bits, respectively). With this high performance and a full power bandwidth of 55MHz, the SHM-12 is an ideal device for driving flash and high-resolution subranging A/D converters.

A careful design optimizes the device for accuracy and speed over the full military temperature range. The droop rate is a low ±0.5mV/µs. The 30mA output current and guaranteed specifications for a 100Ω load provide high drive capability. Operating from ±5V supplies, the SHM-12 consumes only 250mW of power.

The SHM-12 is built using a fast complementary bipolar process. The device is available in both military and industrial temperature ranges. The SHM-12 is packaged in a 20-pin plastic SOIC or ceramic LCC.

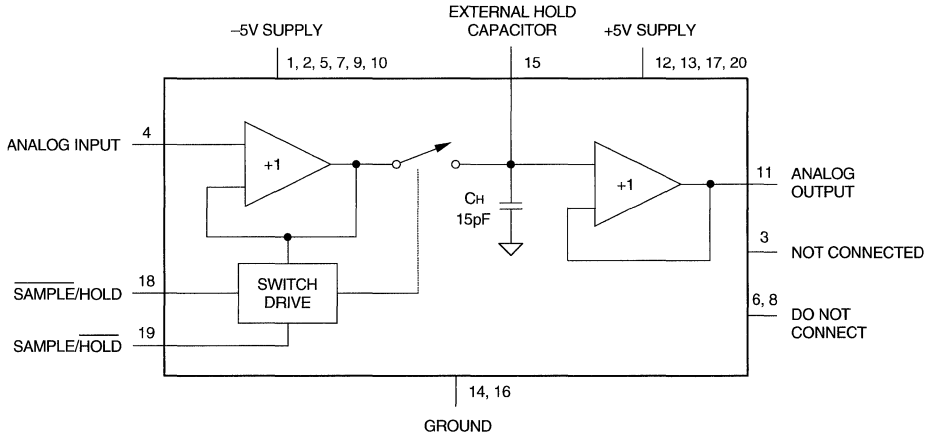


Figure 1. SHM-12 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Supply	0 to +6	Volts
–5V Supply	0 to –6	Volts
Analog Input	+5V Supply –1	Volts
	–5V Supply +1	Volts
Continuous Output Current	±50	mA
Digital Inputs	<Supply Voltages	Volts
Junction Temperature	+175	°C
Lead Temperature (10 seconds)	+300	°C

Output shorted to any supply will cause permanent damage.

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range using a 100Ω resistive load, 10pF capacitive load, ECL digital input levels, a 47pF external hold capacitor, and ±5V nominal supplies, unless otherwise specified.)

INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	–1.5	—	+1.5	Volts
Input Impedance	0.3	1	—	MΩ
Digitals Inputs (Balanced ECL)				
Logic Levels				
Logic 1	–0.8	—	+1.8	Volts
Logic 0	–2.5	—	–1.8	Volts
Logic Loading				
Logic 1	—	+10	+50	µA
Logic 0	—	–30	–150	µA
OUTPUTS				
Output Voltage Range	–1.5	—	+1.5	Volts
Output Current ①	± 30	—	—	mA
Output Impedance (dc)	—	0.3	1	Ω
Stable Capacitive Load	—	—	50	pF
PERFORMANCE				
Nonlinearity (±1V)				
+25°C	—	±0.006	—	%
–40 to +85°C	—	—	±0.024	%
–55 to +125°C	—	—	±0.024	%
Sample Mode Offset				
+25°C	—	±12	—	mV
–40 to +85°C	—	—	±20	mV
–55 to +125°C	—	—	±30	mV
Pedestal				
+25°C	—	±3	—	mV
–40 to +85°C	—	—	±20	mV
–55 to +125°C	—	—	±20	mV
Gain, +25°C	+0.98	+0.995	—	V/V
Gain Drift (±1V)				
–40 to +85°C	—	—	±20	ppm/°C
–55 to +125°C	—	—	±30	ppm/°C
Aperture Delay				
–40 to +85°C	—	2	—	ns
–55 to +125°C	—	2	—	ns
Aperture Jitter				
–40 to +85°C	—	1	—	ps rms
–55 to +125°C	—	1	—	ps rms
Harmonic Distortion (±1V)				
dc to 1MHz	—	–75	—	dB
dc to 10MHz				
+25°C	—	–62	—	dB
–40 to +85°C	—	—	–56	dB
–55 to +125°C	—	—	–54	dB
Acquisition Time (±0.012%, ±1V)				
–40 to +85°C	—	20	—	ns
–55 to +125°C	—	30	—	ns
Acquisition Time (±0.024%, ±1V)				
–40 to +85°C	—	15	30	ns
–55 to +125°C	—	25	40	ns
Acquisition Time (±0.05%, ±1V)				
–40 to +85°C	—	12	25	ns
–55 to +125°C	—	15	30	ns

PERFORMANCE (Cont.)	MIN.	TYP.	MAX.	UNITS
Acquisition Time (±0.1%, ±1V)				
–40 to +85°C	—	10	20	ns
–55 to +125°C	—	10	20	ns
Hold Mode Settling (±0.012%)				
–40 to +85°C	—	10	—	ns
–55 to +125°C	—	10	—	ns
Hold Mode Settling (±0.024%)				
–40 to +85°C	—	7	18	ns
–55 to +125°C	—	7	18	ns
Hold Mode Settling (±0.05%)				
–40 to +85°C	—	6	15	ns
–55 to +125°C	—	6	15	ns
Hold Mode Settling (±0.1%)				
–40 to +85°C	—	5	12	ns
–55 to +125°C	—	5	12	ns
Slew Rate	±220	±350	—	V/µs
Full Power Bandwidth (±1V)	35	55	—	MHz
Small Signal Bandwidth	50	120	—	MHz
Output Noise, Hold Mode	—	65	—	µVrms
Feedthrough (2V Step)	—	–80	—	dB
Droop Rate				
+25°C	—	±0.5	±1.5	mV/µs
–40 to +85°C	—	±2	±5	mV/µs
–55 to +125°C	—	±2.5	±10	mV/µs
POWER SUPPLY REQUIREMENTS				
Power Supply Range				
+5V Supply	+4.5	+5	+5.5	Volts
–5V Supply	–5.5	–5	–4.5	Volts
Power Supply Current				
+5V Supply	+17	+25	+30	mA
–5V Supply	–17	–25	–30	mA
Power Dissipation	170	250	300	mW
Power Supply Rejection Ratio	40	60	—	dB
ENVIRONMENTAL				
Operating Temp. Range, Case				
SHM-12S, SHM-12L	–40	—	+85	°C
SHM-12LM	–55	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Package Type				
SHM-12S	20-Pin plastic SOIC			
SHM-12L, SHM-12LM	20-Pin ceramic LCC			

Footnotes:
① Short circuit protection at ±50mA.

TECHNICAL NOTES

The SHM-12 employs an open loop architecture to achieve its superior high-speed characteristics. The first stage buffer amplifier incorporates the sample-and-hold switch. This allows for a fast acquisition time which is not limited by slew current like the traditional Schottky diode bridge switch. The output amplifier uses a closed loop voltage feedback design which provides a low (0.3Ω, typical) output impedance. Gain and linearity are not affected by heavy loads.

The design has been optimized to achieve the high accuracy associated with fast transient responses over the military temperature range. During the track-to-hold transient, the integral nonlinearity is not affected and the pedestal remains constant over the full ±1.5V input range.

An innovative circuit design ensures an extremely low droop rate. An external hold capacitor can be added to the 15pF internal hold capacitor to obtain a lower droop rate (the droop rate is proportional to the inverse of the total hold capacitor value) without increasing transient response times by more than a few ns. The external hold capacitor should not exceed 100pF.

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GROUNDING AND LAYOUT

Obtaining fully specified performance from the SHM-12 requires careful attention to pc-board layout and power supply decoupling.

For optimal performance, tie all grounds directly to a large analog ground plane beneath and around the package. Bypass all power supplies to ground with 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors.

Locate the bypass capacitors as close to the unit as possible.

For best performance, controlled impedance transmission line techniques, such as microstrip, should be used. Mount all components as close to the required pins as possible. It is strongly recommended that the SHM-12 not be socket-mounted.

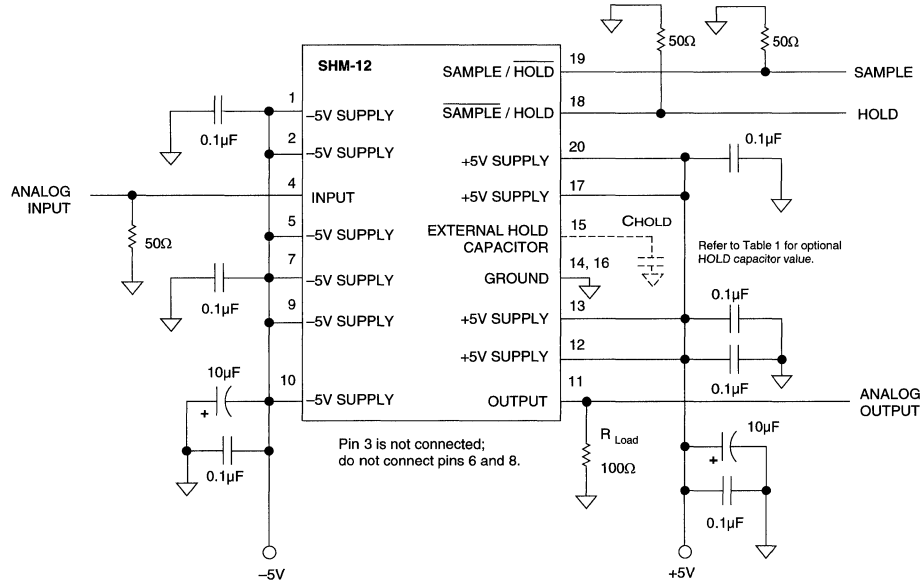

Figure 2. SHM-12 Simplified Connection Diagram

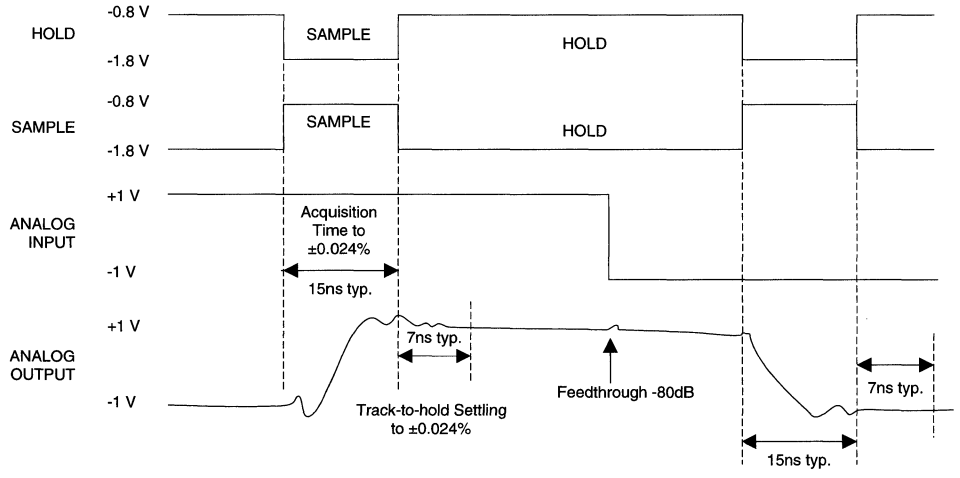

Figure 3. SHM-12 Control and Timing

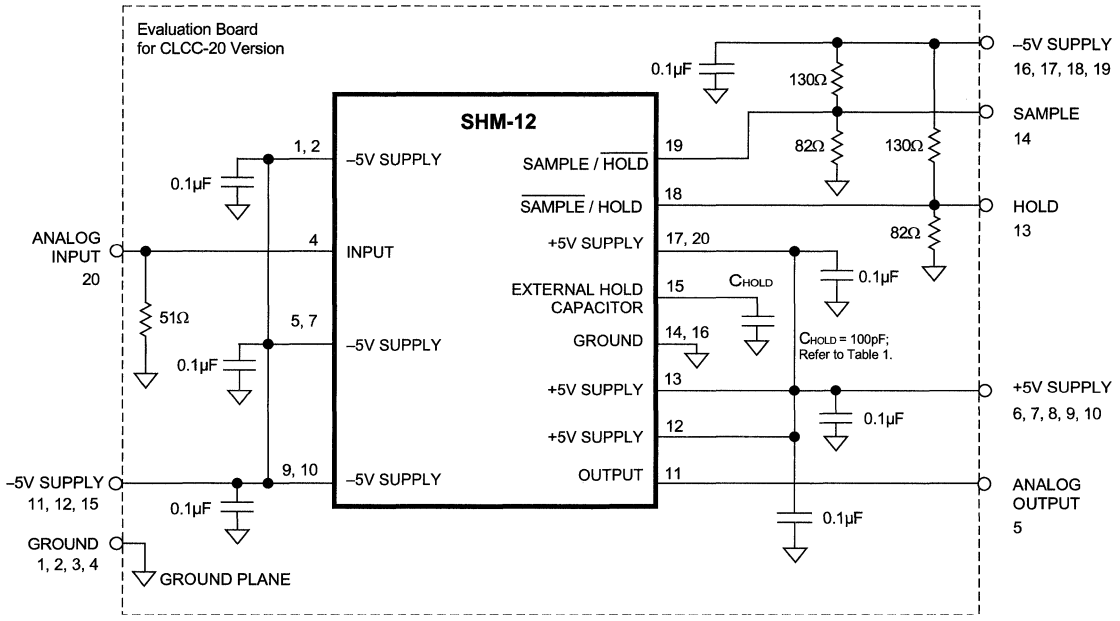

Figure 4. SHM-12 Evaluation Board Schematic

Table 1. Optional External HOLD Capacitor

Model	Operating Temperature Range	Type of HOLD Capacitor (Ceramic, ≤100pF, ±10%)
SHM-12L, -12S	–40 to +85°C	Type I or II, NPO or X7R
SHM-12LM	–55 to +125°C	Type I or NPO

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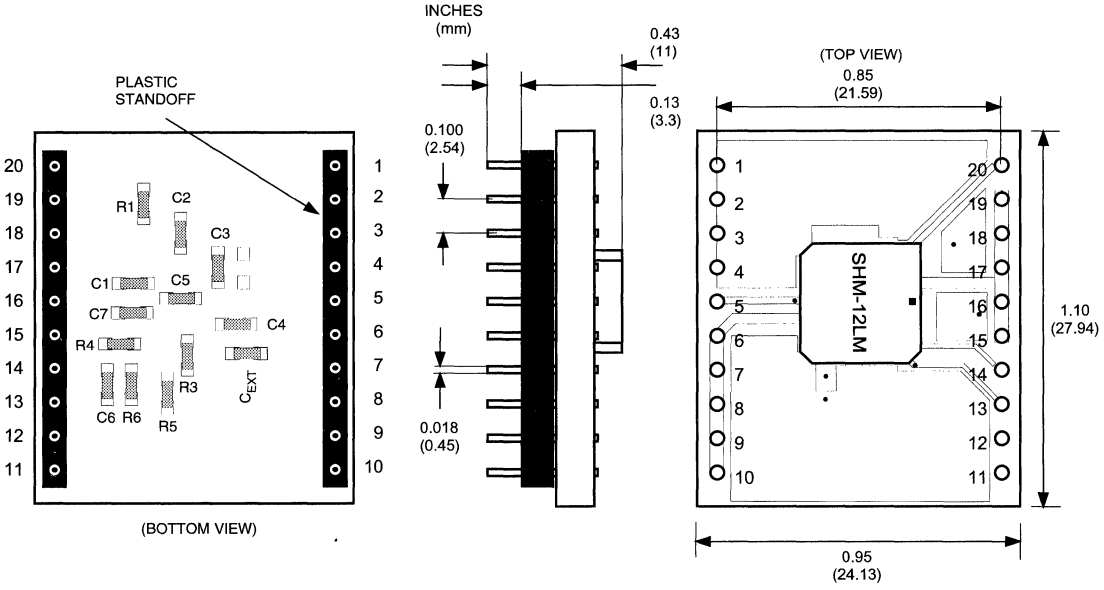


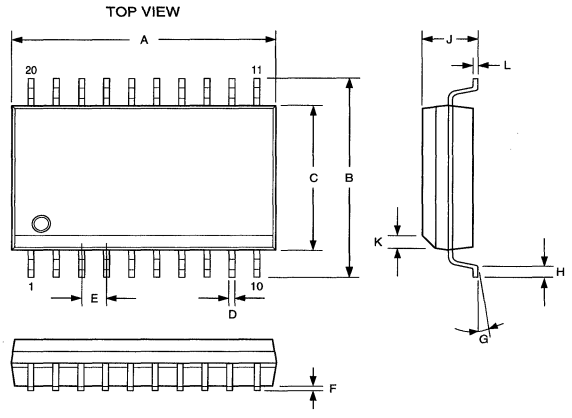
Figure 5. SHM-12 Evaluation Board Dimensions

SHM-12 Evaluation Board Connections

PIN	FUNCTION
1	GROUND
2	GROUND
3	GROUND
4	GROUND
5	ANALOG OUTPUT
6	+5V SUPPLY
7	+5V SUPPLY
8	+5V SUPPLY
9	+5V SUPPLY
10	+5V SUPPLY
11	–5V SUPPLY
12	–5V SUPPLY
13	HOLD
14	SAMPLE
15	–5V SUPPLY
16	–5V SUPPLY
17	–5V SUPPLY
18	–5V SUPPLY
19	–5V SUPPLY
20	ANALOG INPUT

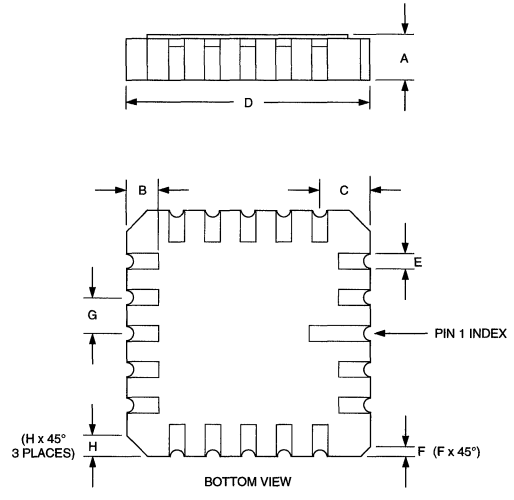
MECHANICAL DIMENSIONS

SOIC-20 Package



	INCHES		MILLIMETERS	
SYMBOL	MIN.	MAX.	MIN.	MAX.
A	0.500	0.510	12.70	12.95
B	0.400	0.410	10.16	10.41
C	0.292	0.299	7.40	7.60
D	0.014	0.019	0.35	0.48
E	0.0500 BSC		1.27 BSC	
F	0.0039	0.0112	0.10	0.30
G	0°	8°	0°	8°
H	0.020	0.040	0.51	1.02
J	0.097	0.104	2.46	2.64
K	0.010	0.020	0.25	0.51
L	0.0091	0.0125	0.23	0.32

CLCC-20 Package



	INCHES		MILLIMETERS	
SYMBOL	MIN.	MAX.	MIN.	MAX.
A	0.064	0.100	1.63	2.54
B	0.045	0.055	1.14	1.40
C	0.075 REF		1.91 REF	
D	0.342	0.358	8.69	9.09
E	0.022	0.028	0.56	0.71
F	0.020 REF		0.51	
G	0.050 BSC		1.27 BSC	
H	0.040 REF		1.02	

ORDERING INFORMATION

MODEL NUMBER	PACKAGE	TEMPERATURE RANGE
SHM-12S	SOIC-20	–40 to +85°C
SHM-12L	CLCC-20	–40 to +85°C
SHM-12LM	CLCC-20	–55 to +125°C
EVB-SHM12	Evaluation Board (with SHM-12LM)	

Contact DATEL for availability of high-reliability models.

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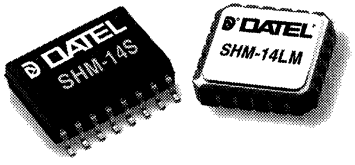
SHM-14

Ultra-Fast, 14-Bit Linear Monolithic Sample-Hold Amplifiers

FEATURES

- **Fast acquisition time:**
  - **10ns to ±0.1%**
  - **20ns to ±0.024%**
  - **25ns to ±0.012%**
- **±0.0012% Nonlinearity**
- **65µV rms output noise**
- **250MHz small signal bandwidth**
- **70MHz full power bandwidth**
- **–80dB feedthrough**
- **1ps Aperture jitter**
- **250mW power dissipation**
- **Low cost**



GENERAL DESCRIPTION

The SHM-14 is an extremely high-speed and accurate monolithic sample-and-hold amplifier designed for fast data acquisition applications. The SHM-14 is accurate (±0.5 LSB to 14-bits over the full military temperature range) and is very fast (10ns and 20ns acquisition times to accuracies of 10 and 12 bits respectively). With this high performance and a full power bandwidth of 70MHz, the SHM-14 is an ideal device for driving flash and high-resolution subranging A/D converters.

A careful design optimizes the device for accuracy and speed over the full military temperature range. The droop rate is a low ±2mV/µs and can be further reduced by adding an optional external hold capacitor. The 30mA output current and guaranteed specifications for a 100Ω load provide high drive capability. Operating from ± 5V supplies, the SHM-14 consumes only 250mW of power.

The SHM-14 is built using a fast complementary bipolar process. The device is available in both military and industrial temperature ranges. The SHM-14 is packaged in a 16-pin plastic SOIC or in a 20-pin ceramic LCC.

INPUT/OUTPUT CONNECTIONS — SOIC

PIN	FUNCTION	PIN	FUNCTION
1	–5V SUPPLY	16	SAMPLE/$\overline{\text{HOLD}}$
2	DO NOT CONNECT	15	SAMPLE/HOLD
3	ANALOG INPUT	14	+5V SUPPLY
4	DO NOT CONNECT	13	EXT. CAPACITOR
5	–5V SUPPLY	12	GROUND
6	DO NOT CONNECT	11	+5V SUPPLY
7	DO NOT CONNECT	10	+5V SUPPLY
8	–5V SUPPLY	9	ANALOG OUTPUT

INPUT/OUTPUT CONNECTIONS — CLCC

PIN	FUNCTION	PIN	FUNCTION
1	NOT CONNECTED	20	NOT CONNECTED
2	–5V SUPPLY	19	SAMPLE/$\overline{\text{HOLD}}$
3	NOT CONNECTED	18	SAMPLE/$\overline{\text{HOLD}}$
4	ANALOG INPUT	17	+5V SUPPLY
5	NOT CONNECTED	16	NOT CONNECTED
6	DO NOT CONNECT	15	EXT. CAPACITOR
7	–5V SUPPLY	14	GROUND
8	DO NOT CONNECT	13	+5V SUPPLY
9	DO NOT CONNECT	12	+5V SUPPLY
10	–5V SUPPLY	11	ANALOG OUTPUT

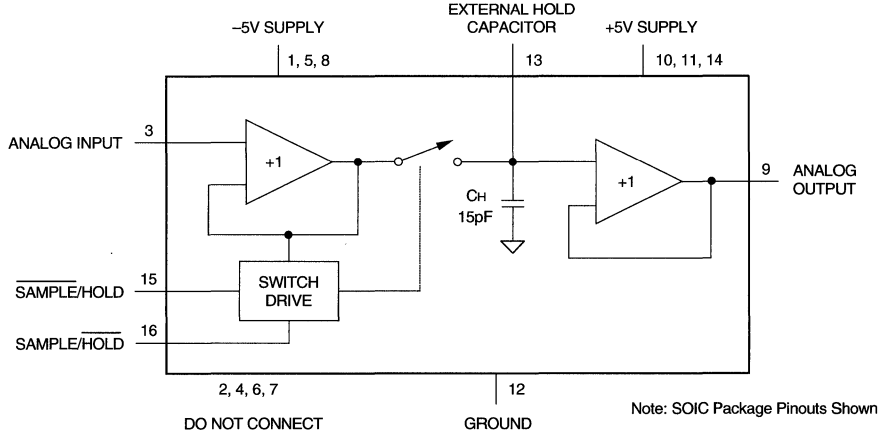


Figure 1. SHM-14 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Supply	0 to +6	Volts
–5V Supply	0 to –6	Volts
Analog Input	+5V Supply –1	Volts
	–5V Supply +1	Volts
Continuous Output Current	±50	mA
Digital Inputs	<Supply Voltages	Volts
Junction Temperature	+175	°C
Lead Temperature (10 seconds)	+300	°C

Output shorted to any supply will cause permanent damage.

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range using a 100Ω resistive load, 10pF capacitive load, ECL digital input levels, and ±5V nominal supplies, unless specified.)

INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	–2.5	—	+2.5	Volts
Input Impedance	0.3	1	—	MΩ
Digitals Inputs (Balanced ECL)				
Logic Levels				
Logic 1	–0.8	—	+1.8	Volts
Logic 0	–2.5	—	–1.8	Volts
Logic Loading				
Logic 1	—	+10	+50	µA
Logic 0	—	–30	–150	µA
OUTPUTS				
Output Voltage Range	–2.5	—	+2.5	Volts
Output Current ①	± 30	—	—	mA
Output Impedance (dc)	—	0.3	1	Ω
Stable Capacitive Load	—	—	50	pF
PERFORMANCE				
Nonlinearity (±1V)				
+25°C	—	±0.0012	—	%
–40 to +85°C	—	—	±0.002	%
–55 to +125°C	—	—	±0.003	%
Sample Mode Offset				
+25°C	—	±12	—	mV
–40 to +85°C	—	—	±20	mV
–55 to +125°C	—	—	±30	mV
Pedestal				
+25°C	—	±3	—	mV
–40 to +85°C	—	—	±20	mV
–55 to +125°C	—	—	±20	mV
Gain, +25°C	+0.98	+0.995	—	V/V
Gain Drift (±1V)				
–40 to +85°C	—	—	±20	ppm/°C
–55 to +125°C	—	—	±30	ppm/°C
Aperture Delay				
–40 to +85°C	—	2	—	ns
–55 to +125°C	—	2	—	ns
Aperture Jitter				
–40 to +85°C	—	1	—	ps rms
–55 to +125°C	—	1	—	ps rms
Harmonic Distortion (±1V)				
dc to 1MHz	—	–72	—	dB
dc to 10MHz				
+25°C	—	–58	—	dB
–40 to +85°C	—	—	–50	dB
–55 to +125°C	—	—	–48	dB
Acquisition Time (±0.012%, ±2V)				
–40 to +85°C	—	25	—	ns
–55 to +125°C	—	35	—	ns
Acquisition Time (±0.024%, ±2V)				
–40 to +85°C	—	20	35	ns
–55 to +125°C	—	25	40	ns
Acquisition Time (±0.05%, ±2V)				
–40 to +85°C	—	19	30	ns
–55 to +125°C	—	20	35	ns

PERFORMANCE (Cont.)	MIN.	TYP.	MAX.	UNITS
Acquisition Time (±0.1%, ±2V)				
–40 to +85°C	—	10	16	ns
–55 to +125°C	—	10	19	ns
Hold Mode Settling (±0.012%)				
–40 to +85°C	—	12	—	ns
–55 to +125°C	—	15	—	ns
Hold Mode Settling (±0.024%)				
–40 to +85°C	—	7	18	ns
–55 to +125°C	—	7	18	ns
Hold Mode Settling (±0.05%)				
–40 to +85°C	—	6	16	ns
–55 to +125°C	—	6	16	ns
Hold Mode Settling (±0.1%)				
–40 to +85°C	—	5	12	ns
–55 to +125°C	—	5	12	ns
Slew Rate	±300	±430	—	V/µs
Full Power Bandwidth (±1V)	45	70	—	MHz
Small Signal Bandwidth	100	250	—	MHz
Output Noise, Hold Mode	—	65	—	µVrms
Feedthrough (2V Step)	—	–80	—	dB
Droop Rate				
+25°C	—	±2	±6	mV/µs
–40 to +85°C	—	±5	±15	mV/µs
–55 to +125°C	—	±10	±30	mV/µs
POWER SUPPLY REQUIREMENTS				
Power Supply Range				
+5V Supply	+4.5	+5	+5.5	Volts
–5V Supply	–5.5	–5	–4.5	Volts
Power Supply Current				
+5V Supply	+17	+25	+30	mA
–5V Supply	–17	–25	–30	mA
Power Dissipation	170	250	300	mW
Power Supply Rejection Ratio	40	60	—	dB
ENVIRONMENTAL				
Operating Temp. Range, Case				
SHM-14S, SHM-14L	–40	—	+85	°C
SHM-14LM	–55	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Package Type				
SHM-14S	16-Pin plastic SOIC			
SHM-14L, SHM-14LM	20-Pin ceramic LCC			

Footnotes:

① Short circuit protection at ±50mA.

TECHNICAL NOTES

The SHM-14 employs an open loop architecture in order to achieve its superior high-speed characteristics. The first stage buffer amplifier, which charges the hold capacitor, incorporates the sample-and-hold switch into its design. This technique allows for a fast acquisition time which is not limited by slew current like the traditional Schottky diode bridge switch. The output amplifier uses a closed loop voltage feedback design which provides a low (0.3Ω, typical) output impedance. Gain and linearity are not affected by heavy loads.

The design has been optimized to achieve the high accuracy associated with fast transient responses over the full military temperature range. During the track-to-hold transient, the integral nonlinearity is not affected and the pedestal remains constant over the full ±2.5V input range.

An external hold capacitor can be added to the 15pF internal hold capacitor to obtain a lower droop rate (the droop rate is proportional to the inverse of the total hold capacitor value) without increasing transient response times by more than few ns. Settling and acquisition times are typically increased by 5ns and 10ns respectively for 47pF and 100pF external hold capacitors. The external hold capacitor should not exceed 100pF.

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GROUNDING AND LAYOUT

Obtaining fully specified performance from the SHM-14 requires careful attention to pc-board layout and power supply decoupling.

For optimal performance, tie all grounds directly to a large analog ground plane beneath and around the package. Bypass all power supplies to ground with 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors.

Locate the bypass capacitors as close to the unit as possible.

For best performance, controlled impedance transmission line techniques, such as microstrip, should be used. Mount all components as close to the required pins as possible. It is strongly recommended that the SHM-14 not be socket-mounted.

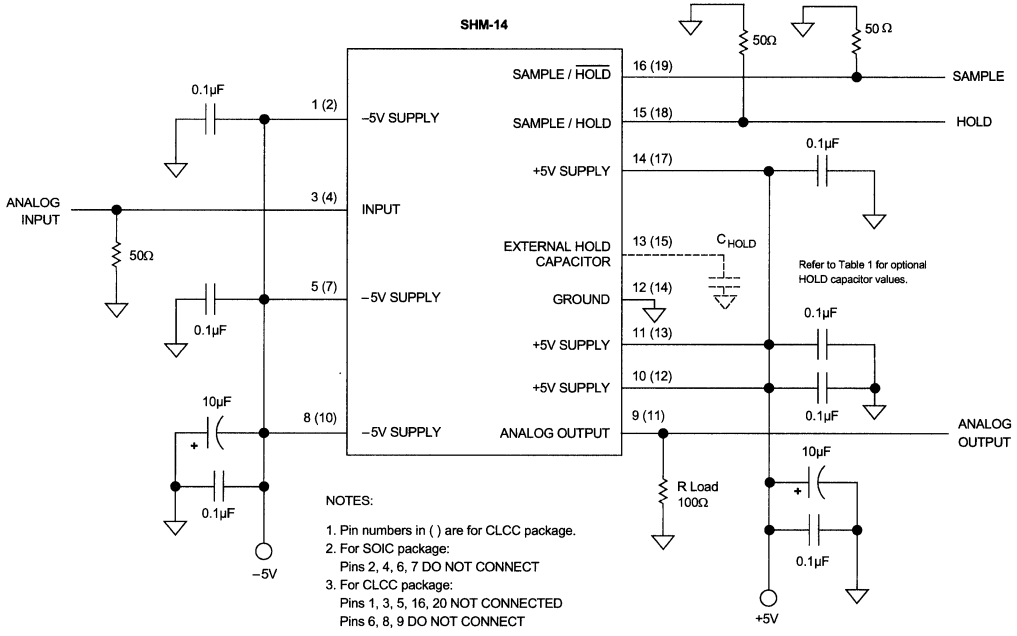


Figure 2. SHM-14 Simplified Connection Diagram

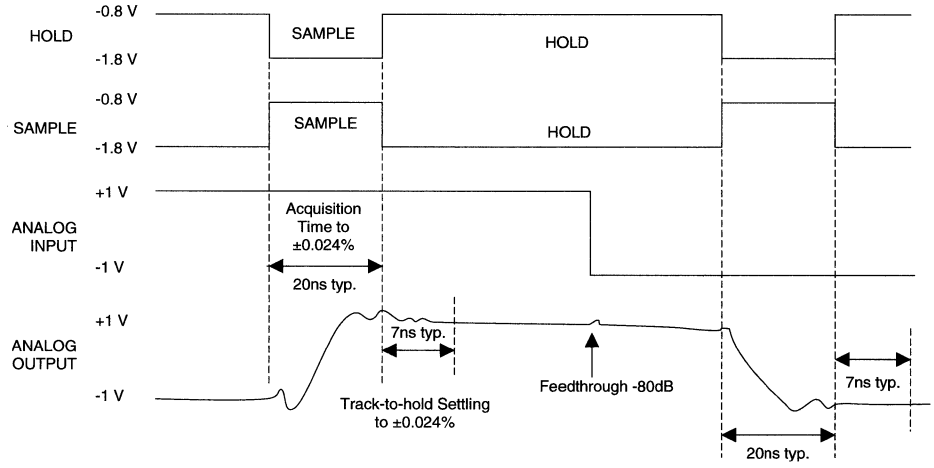


Figure 3. SHM-14 Control and Timing

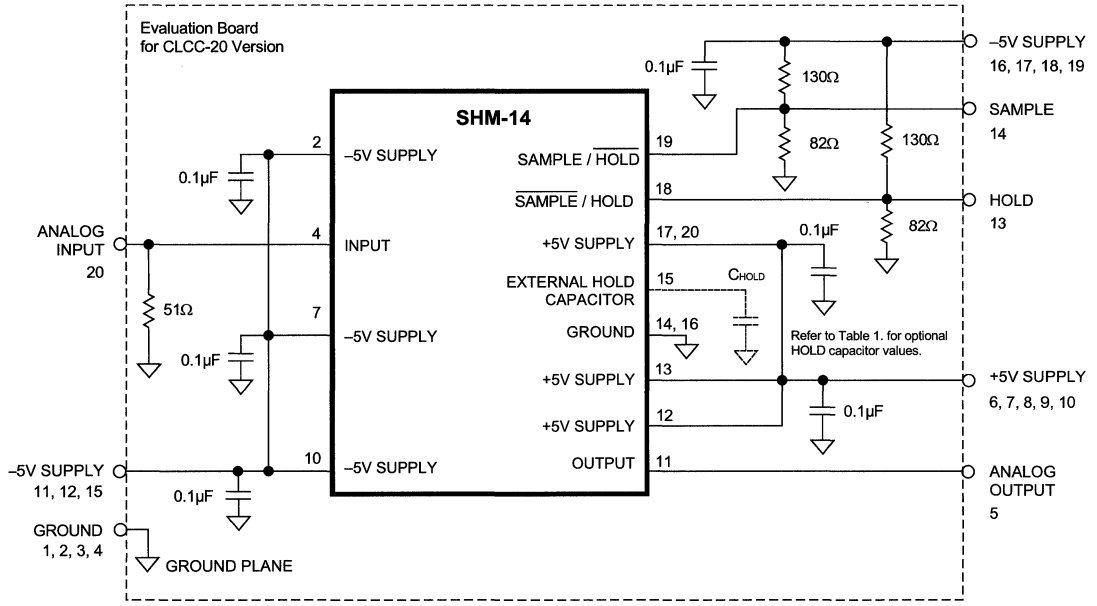


Figure 4. SHM-14 Evaluation Board Schematic

Table 1. Optional External HOLD Capacitor

Model	Operating Temperature Range	Type of HOLD Capacitor (Ceramic, ≤100pF, ±10%)
SHM-14L, -14S	–40 to +85°C	Type I or II, NPO or X7R
SHM-14LM	–55 to +125°C	Type I or NPO

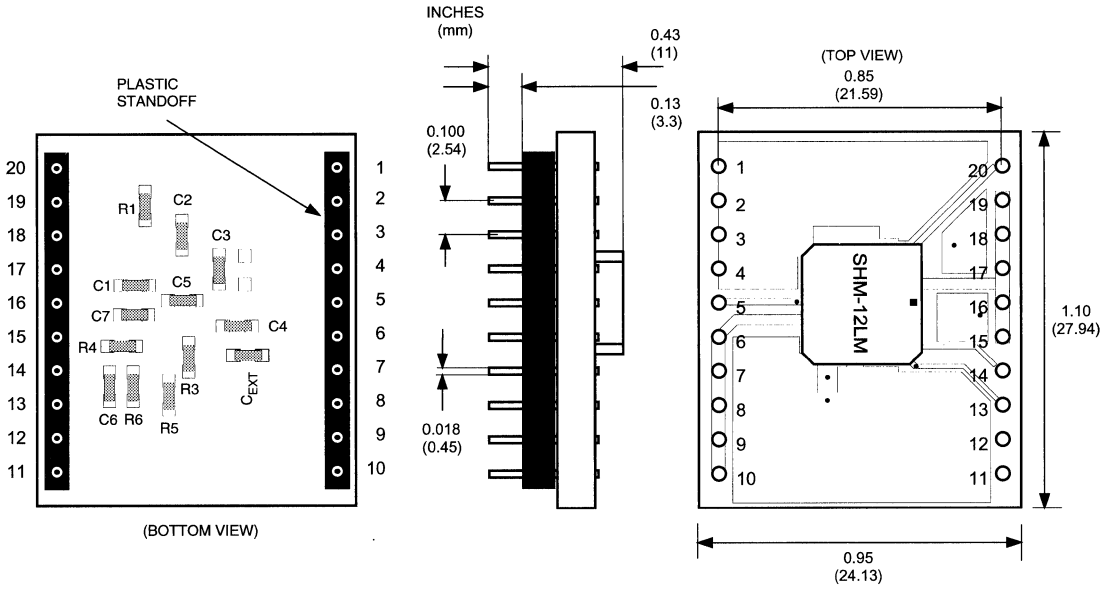


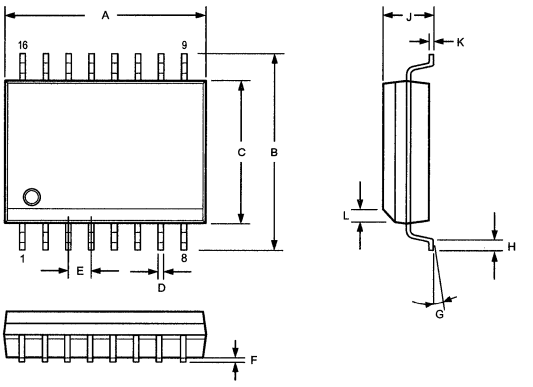
Figure 5. SHM-14 Evaluation Board Dimensions

SHM-14 Evaluation Board Connections

PIN	FUNCTION
1	GROUND
2	GROUND
3	GROUND
4	GROUND
5	ANALOG OUTPUT
6	+5V SUPPLY
7	+5V SUPPLY
8	+5V SUPPLY
9	+5V SUPPLY
10	+5V SUPPLY
11	–5V SUPPLY
12	–5V SUPPLY
13	HOLD
14	SAMPLE
15	–5V SUPPLY
16	–5V SUPPLY
17	–5V SUPPLY
18	–5V SUPPLY
19	–5V SUPPLY
20	ANALOG INPUT

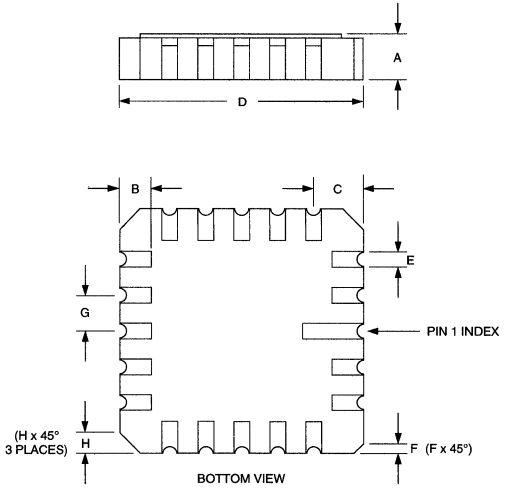
MECHANICAL DIMENSIONS

SOIC-16 Package



	INCHES		MILLIMETERS	
SYMBOL	MIN.	MAX.	MIN.	MAX.
A	0.402	0.412	10.21	10.46
B	0.400	0.410	10.16	10.41
C	0.292	0.299	7.40	7.60
D	0.014	0.019	0.35	0.48
E	0.0500 BSC		1.27 BSC	
F	0.0039	0.0112	0.10	0.30
G	0°	8°	0°	8°
H	0.020	0.040	0.51	1.02
J	0.097	0.104	2.46	2.64
K	0.010	0.020	0.25	0.51
L	0.0091	0.0125	0.23	0.32

CLCC-20 Package



	INCHES		MILLIMETERS	
SYMBOL	MIN.	MAX.	MIN.	MAX.
A	0.064	0.100	1.63	2.54
B	0.045	0.055	1.14	1.40
C	0.075 REF		1.91 REF	
D	0.342	0.358	8.69	9.09
E	0.022	0.028	0.56	0.71
F	0.020 REF		0.51	
G	0.050 BSC		1.27 BSC	
H	0.040 REF		1.02	

ORDERING INFORMATION

MODEL NUMBER	PACKAGE	TEMPERATURE RANGE
SHM-14S	SOIC-16	–40 to +85°C
SHM-14L	CLCC-20	–40 to +85°C
SHM-14LM	CLCC-20	–55 to +125°C
EVB-SHM14	Evaluation Board (with SHM-14LM)	

Contact DATEL for availability of high reliability models.

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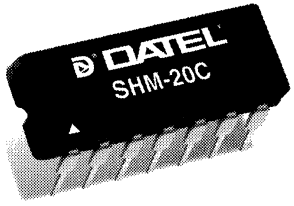
SHM-20
High-Speed, ±0.01% Monolithic Sample-Hold

FEATURES

- **Internal hold capacitor**
- **1µs Acquisition time to ±0.01%**
- **0.3ns Aperture uncertainty**
- **3 x 105 DC gain**
- **±0.08µV/µs droop rate**
- **Differential inputs**



GENERAL DESCRIPTION

DATEL's SHM-20 is a low-cost, complete, monolithic sample-hold amplifier which includes an internal 100pF MOS hold capacitor. Primarily designed for high-speed analog signal processing applications, the SHM-20 features a typical acquisition time of 1µsec for a 10V input step to ±0.01%. Aperture uncertainty is typically 0.3ns, and droop rate is as low as ±0.08µV/µs.

The SHM-20 consists of an input transconductance amplifier, a low-leakage analog switch, an output integrating amplifier, and a 100pF MOS hold capacitor. Charge injection on the hold cap (and the resulting ±1mV pedestal error) is constant over the entire ±10V input/output voltage range. If necessary, the pedestal error can be eliminated using the external offset-adjust capability. For improved droop rate, additional hold capacitance may be added externally at the expense of acquisition time.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	–INPUT
2	+INPUT
3	OFFSET ADJUST
4	OFFSET ADJUST
5	–15V SUPPLY
6	SIGNAL GROUND
7	OUTPUT
8	INTEGRATOR COMPENSATION
9	+15V SUPPLY
10	NO CONNECTION
11	EXTERNAL HOLD CAPACITOR
12	NO CONNECTION
13	POWER GROUND
14	$\overline{S}$/H CONTROL

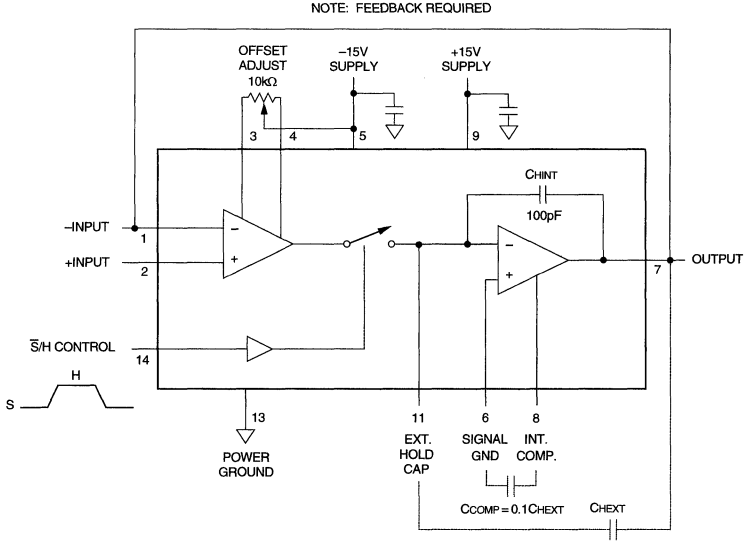


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins (9 & 5)	40V
Differential Input Voltage	±24V
Digital Input Voltage, Pin 14	–15 to +8V
Output Current, Continuous ①	±20mA
Junction Temperature	+175°C

FUNCTIONAL SPECIFICATIONS

(Typical at T_A = +25°C with ±15V supplies, using internal hold capacitor, unless noted.)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Range ②	±10	—	—	Volts
Input Impedance	1	—	—	MΩ
Input Capacitance	—	—	3	pF
Input Offset Voltage	—	—	±1.5	mV
Input Offset Voltage Drift ②	—	—	±20	µV/°C
Input Bias Current ②	—	—	±300	nA
Input Offset Current ②	—	—	±300	nA
Common Mode Range ②	±10	—	—	Volts
CMRR (V_{CM} = ±5V)	72	—	—	dB
DIGITAL INPUTS				
Logic Levels				
Logic "1" (Hold Mode)	+2.0	—	—	Volts
Logic "0" (Sample Mode)	—	—	+0.8	Volts
Logic Loading "1"	—	—	+0.1	µA
Logic Loading "0"	—	—	–10	µA
OUTPUT				
Output Voltage Range ②	±10	—	—	Volts
Output Current ③	±10	—	—	mA
Output Impedance, Hold Mode	—	1	—	Ω
PERFORMANCE				
Accuracy	—	±0.01	—	%
DC Gain	3 x 10^5	—	—	V/V
Gain Error Tempco	—	—	±0.6	ppm/°C
Gain Bandwidth Product ④	—	2	—	MHz
Gain Bandwidth Product (C_H = 1000pF) ④	—	0.18	—	MHz
Full Power Bandwidth ⑤	—	600	—	kHz
Hold Mode Feedthrough, 10Vp-p, 100kHz ②	—	2	—	mVp-p
Droop Rate	—	±0.08	—	µV/µs
Droop Rate ②	—	±1.2	—	µV/µs
Charge Transfer ⑥	—	0.1	—	pC
Pedestal Error ⑥ ⑦	—	±1	—	mV
Total Output Noise, DC to 10MHz	—	—	200	µVrms
Power Supply Rejection Ratio ②				
+15V Supply	—	80	—	dB
–15V Supply	—	65	—	dB
DYNAMIC CHARACTERISTICS				
Acquisition Time				
10V Step to ±0.1%	—	0.8	—	µs
10V Step to ±0.01%	—	1.0	—	µs
Aperture Delay Time	—	30	—	ns
Aperture Uncertainty Time	—	0.3	—	ns
Aperture Time	—	25	—	ns
Hold Mode Settling Time, To ±0.01% ②	—	185	—	ns
Rise Time	—	100	—	ns
Overshoot	—	15	—	%
Slew Rate ⑧	—	±45	—	V/µs

POWER REQUIREMENTS ⑨	
Positive Supply, Pin 9	+15V, ±0.5V at 11mA
Negative Supply, Pin 5	–15V, ±0.5V at –11mA
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range, Ambient	0 to +70°C
Storage Temp. Range	–65 to +150°C
Package Type	14-pin ceramic DIP

Footnotes:

① Internal power dissipation may limit output current below ±20mA.

② Over full operating temperature range.

③ Output is not short-circuit protected. Only momentary short circuits to ground can be tolerated

④ Output voltage = 200mVp-p; load resistance = 2kΩ; load capacitance = 50pF.

⑤ Output voltage = 20Vp-p; load resistance = 2kΩ; load capacitance = 50pF.

⑥ Input voltage = 0V; digital input voltage = +3.5V.

⑦ For C_H = 100pF. For C_H = 1000pF, pedestal error is ±0.1mV. For C_H = 0.01µF, pedestal error is ±0.01mV.

⑧ Output voltage = 20V step.

⑨ A power supply voltage as low as ±12V may be used. However, this will cause some degradation in performance.

TECHNICAL NOTES

1. The SHM-20 has the uncommitted differential inputs of an op amp. This allows the sample-and-hold function to be combined with conventional op-amp circuits. Figure 1 shows the SHM-20 connected in a unity-gain non-inverting amplifier configuration.

2. A printed circuit board with ground plane is recommended for best performance. The supply pins (pins 5 and 9) should be bypassed to ground with a 0.01 to 0.1µF ceramic capacitors as close to the pins as possible.

3. If an external hold capacitor (C_{HEXT}) is connected between pins 7 and 11, then a noise bandwidth capacitor with a value of 10% of the value of the external hold capacitor should be connected from pin 8 to signal ground, pin 6. Exact value and type are not critical.

4. The hold capacitor (C_{HEXT}) should have high insulation resistance and low dielectric absorption to minimize droop error. For operating temperatures up to +70°C, polystyrene dielectric is a good choice. Any pc connections to the hold capacitor terminal (pin 11) should be kept short and "guarded" by the ground plane to avoid errors due to drift currents from nearby signal lines or power supply voltages.

5. The offset adjust may be used to eliminate the pedestal error by connecting a 10k Ohm pot between pins 3 and 4 and connecting the wiper to the –15V supply, pin 5.

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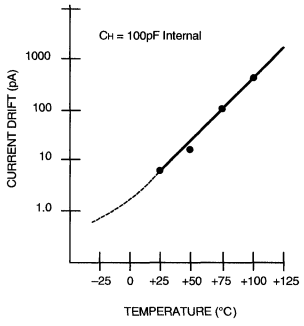
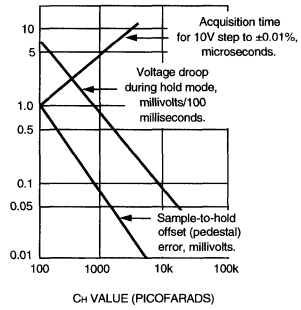
DRIFT CURRENT VS. TEMPERATURE



TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLD CAPACITOR



OPEN LOOP GAIN AND PHASE RESPONSE

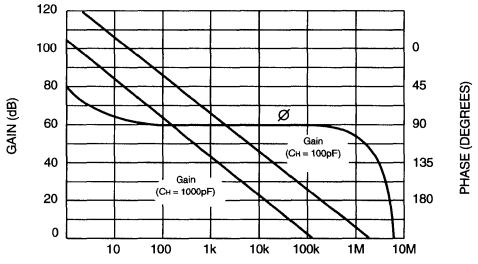


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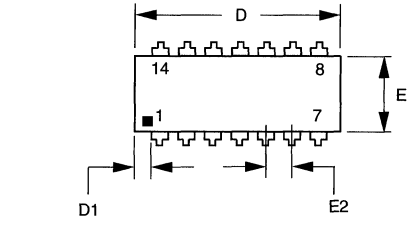
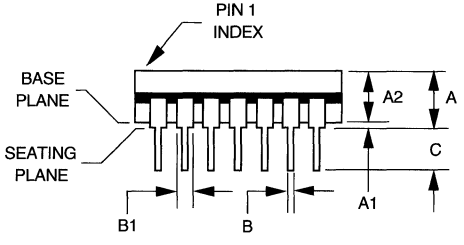
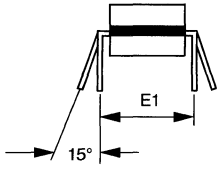
Figure 2. Typical Performance Characteristics

MECHANICAL DIMENSIONS







	INCHES		MILLIMETERS	
SYMBOL	MIN.	MAX.	MIN.	MAX.
A	—	0.200	—	5.08
A1	0.015	0.060	0.38	1.52
A2	—	0.140	—	3.56
B	0.014	0.026	0.36	0.66
B1	0.045	0.065	1.14	1.65
C	0.125	0.200	3.18	5.08
D	—	0.785	—	19.94
D1	0.005	—	0.13	—
E	0.220	0.310	5.59	7.87
E1	0.300 BSC		7.62 BSC	
E2	0.100 BSC		2.54 BSC	

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
SHM-20C	0 to +70°C

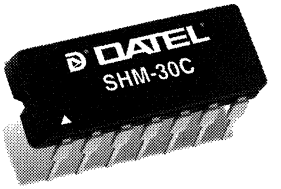
SHM-30

Very High-Speed, ±0.01% Monolithic Sample-Hold

DATEL® INNOVATION and EXCELLENCE

FEATURES

- **650ns Acquisition time to ±0.01%**
- **Internal hold capacitor**
- **Low droop, ±0.01μV/μs**
- **±90V/μs Slew rate**
- **Low ±0.2mV typical offset voltage**
- **Fully differential inputs**



GENERAL DESCRIPTION

DATEL's SHM-30 is a complete monolithic sample-hold amplifier which includes an internal 90pF MOS hold capacitor. Primarily designed to be used in precision, high-speed data acquisition applications, the SHM-30 features an acquisition time of 650ns typical to ±0.01% and a droop rate of ±0.01μV/μs. Other salient features of the SHM-30 include an aperture uncertainty time of 0.1ns, a slew rate of ±90V/μs, and a fully differential input.

The SHM-30 is composed of an input amplifier designed to deliver large amounts of current, a low-leakage switch, and an integrator. The low pedestal error of ±0.5mV can be trimmed to zero with a single potentiometer for demanding applications.

The SHM-30 is packaged in a 14-pin ceramic DIP and operates over the 0 to +70°C temperature range. It requires ±15V supplies and has a maximum power consumption of 735mW.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+INPUT
2	NO CONNECTION
3	OFFSET ADJUST
4	OFFSET ADJUST
5	–15V SUPPLY (–Vs)
6	NO CONNECTION
7	OUTPUT
8	S/H CONTROL
9	NO CONNECTION
10	+15V SUPPLY (+Vs)
11	POWER GROUND
12	SIGNAL GROUND
13	NO CONNECTION
14	–INPUT

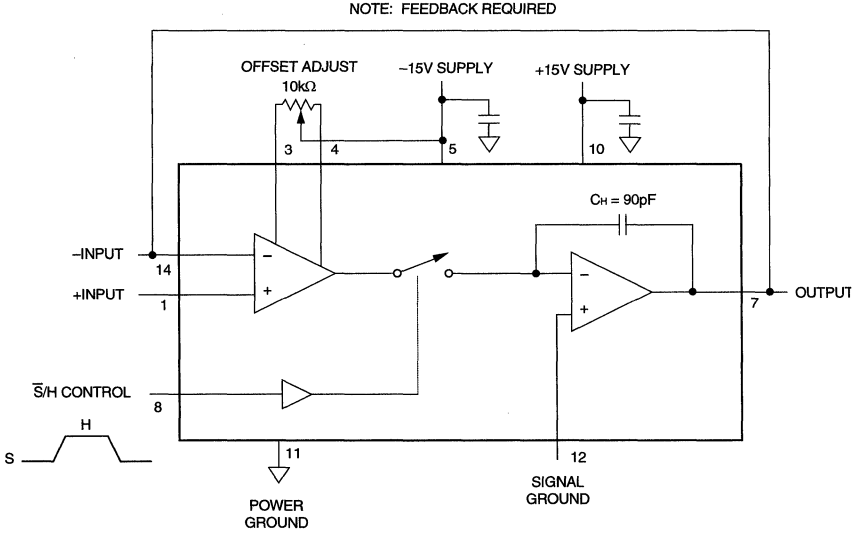


Figure 1. Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS

Voltage Between +Vs and PWR/SIG GND	+20V
Voltage Between –Vs and PWR/SIG GND	–20V
Differential Voltage Between SIG and PWR GND	±2V
Differential Input Voltage	±24V
Digital Input Voltage	–6 to +8V
Output Current, Continuous ①	±17mA
Junction Temperature	+175°C

FUNCTIONAL SPECIFICATIONS

(Typical at T_A = +25°C with ±15V supplies and unity-gain configuration, unless noted.)

ANALOG INPUT	MIN.	TYP.	MAX.	UNITS
Input Voltage Range ②	±10	—	—	Volts
Input Impedance	5	—	—	MΩ
Input Capacitance	—	3	—	pF
Input Offset Voltage	—	±0.2	±1.5	mV
Input Offset Voltage Drift ②	—	—	±10	µV/°C
Input Bias Current ②	—	—	±300	nA
Input Offset Current ②	—	—	±300	nA
Common Mode Range ②	±10	—	—	Volts
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Loading "1"	—	—	+40	µA
Logic Loading "0"	—	—	–40	µA
ANALOG OUTPUT				
Output Voltage Range ②	±10	—	—	Volts
Output Current ②	±10	—	—	mA
Output Impedance, Hold Mode	—	0.2	—	Ohms
PERFORMANCE				
DC Gain ②	2 x 10^6	—	—	V/V
Gain Bandwidth Product ③	—	4.5	—	MHz
Hold Mode Feedthrough, 20Vp-p, 100kHz ②	—	–88	—	dB
Droop Rate	—	±0.01	—	µV/µs
Droop Rate ②	—	—	±10	µV/µs
Pedestal Error ④	—	±0.5	—	mV
Total Output Noise, DC to 4MHz				
Sample Mode	—	230	—	µVrms
Hold Mode	—	190	—	µVrms
Power Supply Rej. Ratio ②⑤	86	—	—	dB
Common Mode Rejection Ratio ②⑥	86	—	—	dB
DYNAMIC CHARACTERISTICS				
Acquisition Time				
10V step to ±0.1%	—	500	—	ns
Over full temp. range	—	—	700	ns
10V step to ±0.01%	—	650	—	ns
Over full temp. range	—	—	900	ns
Aperture Delay Time	—	–25	—	ns
Aperture Uncertainty Time	—	0.1	—	ns
Hold Mode Settling Time, ±0.01%	—	—	200	ns
Rise Time ⑦	—	70	—	ns
Overshoot ⑦	—	10	—	%
Slew Rate ⑦	—	±90	—	V/µs
POWER REQUIREMENTS ⑧				
Positive Supply, Pin 10	+15V, ±0.5V at 24mA max.			
Negative Supply, Pin 5	–15V, ±0.5V at 25mA max.			

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0 to +70°C
Storage Temperature Range	–55 to +150°C
Package Type	14-pin ceramic DIP

Footnotes:

① Internal power dissipation may limit output current below ±17mA.

② Over full operating temperature range.

③ V_O = 200mVp-p, R_L = 2kΩ, C_L = 50pF.

④ V_{IN} = 0V; $\overline{S}$/H control signal +3.5V with 20ns rise time from 0V to +3.5V.

⑤ Based on a three-volt delta in each supply, i.e., 15V = ±1.5V.

⑥ V_{CM} = ±10Vdc.

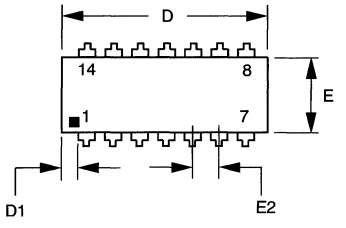
⑦ V_O = 20V step, R_L = 2kΩ, C_L = 50pF.

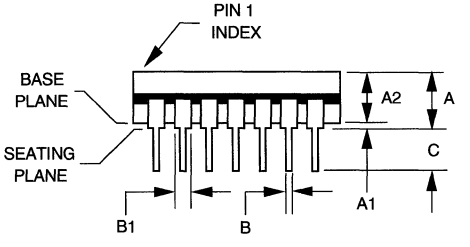
⑧ Power supply voltages as low as ±11 Volts may be used. However, this will cause some degradation in performance.

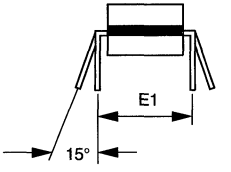
TECHNICAL NOTES

1. The SHM-30 has the uncommitted differential inputs of an operational amplifier. This permits the sample-and-hold function to be combined with most conventional op-amp circuits. Figure 1 shows the SHM-30 in a non-inverting, unity-gain configuration.
2. A printed circuit board design with extensive ground plane is recommended for optimum performance. Bypass capacitors (0.01 to 0.1µF ceramic) should be provided from each power supply pin to the PWR GND terminal on pin 11.
3. The internal hold capacitor is 90pF MOS.
4. The output circuit is not short-circuit protected. Only momentary short-circuits to ground are permissable.
5. Offset and pedestal adjustments may be performed by using a 10kΩ trimpot between pins 3 and 4 with the wiper connected to –15 Volts.

MECHANICAL DIMENSIONS







	INCHES		MILLIMETERS	
SYMBOL	MIN.	MAX.	MIN.	MAX.
A	—	0.200	—	5.08
A1	0.015	0.060	0.38	1.52
A2	—	0.140	—	3.56
B	0.014	0.026	0.36	0.66
B1	0.045	0.065	1.14	1.65
C	0.125	0.200	3.18	5.08
D	—	0.785	—	19.94
D1	0.005	—	0.13	—
E	0.220	0.310	5.59	7.87
E1	0.300 BSC		7.62 BSC	
E2	0.100 BSC		2.54 BSC	

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
SHM-30C	0 to +70°C

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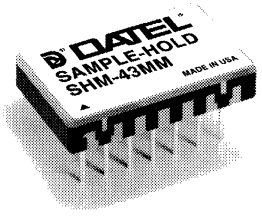
SHM-43
High-Speed, ±0.01% Hybrid Sample-Hold Amplifiers

FEATURES

- **35ns maximum acquisition time to ±0.01%**
- **30ns maximum hold-mode settling to ±0.01%**
- **1ps aperture uncertainty**
- **150MHz small signal bandwidth**
- **545mW power dissipation**
- **Small 14-pin DIP package**
- **CMOS control signal**



GENERAL DESCRIPTION

The SHM-43 sample-hold utilizes a proprietary architecture to deliver acquisition times of 35 nanoseconds maximum to ±0.01% accuracy and 25 nanoseconds maximum to ±0.1% accuracy.

Operation requires +15V and ±5V supplies, and the analog input range is ±1V. Packaged in a small 14-pin DIP, the SHM-43 offers a CMOS compatible sample command while dissipating just 545 milliwatts.

The SHM-43 has been designed for applications that demand fast acquisition times (25ns, ±0.01%), fast hold-mode settling (20ns, ±0.01%), wide bandwidth, and the ability to drive resistive (100Ω) and capacitive (50pF) loads with no compromise in performance. These features make the SHM-43 an ideal choice for driving flash A/D converters in applications such as radar and communications.

Two temperature ranges are offered; commercial 0 to +70°C and military –55 to +125°C.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	INPUT
2	REF BYPASS
3	POWER GROUND
4	DIGITAL +5V SUPPLY
5	S/$\overline{H}$ OR $\overline{S}$/H
6	S/H CONTROL
7	DIGITAL GROUND
8	S/H OUTPUT
9	+5V BYPASS
10	–5V BYPASS
11	ANALOG GROUND
12	+15V SUPPLY
13	–5V SUPPLY
14	ANALOG +5V SUPPLY

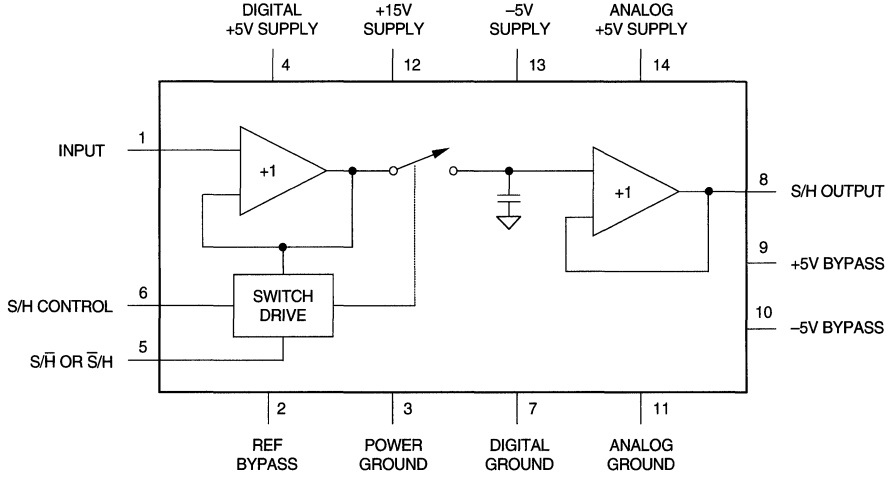


Figure 1. SHM-14 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply, Pin 12	–0.5 to +18	Volts
+5V Supplies, Pins 4, 14	–0.5 to +7	Volts
–5V Supply, Pin 13	+0.5 to –7	Volts
Analog Input , Pin 1	+5V Supply +1	Volts
	–5V Supply –1	Volts
Digital Inputs, Pins 5, 6	–0.5 to +7	Volts
Lead Temperature (10 seconds)	300	°C
Short circuit to ground	70	mA

Output shorted to any supply will cause permanent damage.

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range with ±1V input range, 100Ω load, +15V and ±5V nominal supplies, unless otherwise specified.)

INPUTS	MIN	TYP	MAX	UNITS
Input Voltage Range	±1	±2	—	Volts
Input Impedance	50	160	—	kΩ
Digital Inputs				
(Digital Supply = +5V)				
Logic Levels				
Logic 1	+3.8	—	—	Volts
Logic 0	—	—	+1.35	Volts
Logic Loading				
Logic 1	—	+1	+5	µA
Logic 0	—	–1	–5	µA
OUTPUTS				
Voltage Range	±1	±2	—	Volts
Output Current	±30	—	—	mA
Output Impedance (dc)	—	0.1	0.25	Ohms
Stable Capacative Load	50	—	—	pF
PERFORMANCE				
Nonlinearity, DC (±1V)				
+25°C	—	—	±0.01	%
0 to +70°C	—	—	±0.01	%
–55 to +125°C	—	—	±0.02	%
Sample Mode Offset, +25°C	—	±5	±30	mV
0 to +70°C	—	±25	±35	mV
–55 to +125°C	—	±25	±35	mV
Pedestal, +25°C	—	±5	±15	mV
0 to +70°C	—	—	±20	mV
–55 to +125°C	—	—	±20	mV
Gain, +25°C	—	1	—	V/V
Gain Error, +25°C	—	—	±2	%
0 to +70°C	—	—	±2.25	%
–55 to +125°C	—	—	±2.25	%
Aperture Delay, +25°C	—	5	10	ns
0 to +70°C	—	10	20	ns
–55 to +125°C	—	10	20	ns
Aperture Jitter, +25°C	—	1	3	ps
0 to +70°C	—	2	6	ps
–55 to +125°C	—	2	6	ps
Slew Rate	±190	±250	—	V/µs
Full Power BW, ±1.5V	20	25	—	MHz
Small Signal Bandwidth	100	150	—	MHz
Harmonic Distortion				
±1V, DC to 5MHz	–70	–74	—	dB
±1V, 5 to 10MHz, +25°C	–60	–70	—	dB
0 to +70°C	–50	—	—	dB
–55 to +125 °C	–50	—	—	dB
Acq.Time ±0.01%, ±1V, +25°C ①	—	25	35	ns
0 to +70°C	—	—	35	ns
–55 to +125°C	—	—	45	ns
Acq.Time ±0.1%, ±1V, +25°C ①	—	15	25	ns
0 to +70°C	—	—	35	ns
–55 to +125°C	—	—	35	ns

PERFORMANCE (Cont.)	MIN.	TYP.	MAX.	UNITS
Hold Mode Settling ±0.01%, +25°C	—	20	30	ns
0 to +70°C	—	—	50	ns
–55 to +125°C	—	—	50	ns
Hold Mode Settling, ±0.1%, +25°C	—	—	20	ns
0 to +70°C	—	—	35	ns
–55 to +125°C	—	—	35	ns
Output Noise, Hold Mode	—	270	—	µVrms
Feedthrough Rejection 2V Step	76	80	—	dB
Droop Rate, +25°C	—	±1	±5	µV/µs
0 to + 70°C	—	—	±50	µV/µs
–55 to +125°C	—	±25	±50	µV/µs
POWER SUPPLY REQUIREMENTS				
Range				
Analog +5V	+4.75	+5.0	+5.25	Volts
Digital +5V	+4.75	+5.0	+5.25	Volts
–5V	–4.75	–5.0	–5.25	Volts
+15V	+14.25	+15.0	+15.75	Volts
Current Drain				
Analog +5V	—	+38	+45	mA
Digital +5V	—	+10	+50	mA
–5V	—	–47	–50	mA
+15V	—	8	12	mA
Power Dissipation	—	545	655	mW
Power Supply Rejection Ratio	52	60	—	dB
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
SHM-43MC	0	—	+70	°C
SHM-43MM	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type	14-pin ceramic DIP			

① DATEL uses the conservative definition of acquisition time, which includes the aperture delay time.

TECHNICAL NOTES

1. Bypass the ±5V and +15V supplies with a 1µF, 25V tantalum capacitor in parallel with a 0.01µF ceramic capacitor mounted as close to the pin as possible.

To achieve optimum performance —

2. Additional bypass capacitors are necessary, because of internal high switching speeds and the high slew rates of internal components. REF BYPASS (pin 2), +5V BYPASS (pin 9), and –5V BYPASS (pin 10) are internal connections that must be bypassed with a minimum 1µF tantalum capacitor mounted as close to the pins as possible. The polarity of the connections are shown in Figure 2.

3. As with all high-speed analog circuits, it is essential that good grounding techniques be used. Tie all ground pins together at a single ground point beneath the device, and use a short low-impedance run to the ground of the analog power supplies. The ground point should be a solid ground plane under the device and any associated data converter.

4. The offset, pedestal and gain errors of the SHM-43 are laser trimmed at DATEL, and no external compensation capabilities have been provided. This prevents introducing noise through the offset adjust terminals of the S/H amplifier and guarantees excellent gain linearity, offset drift and pedestal performance.

5. A true sample/hold, the SHM-43 will return to the sample mode after three to four microseconds in the hold mode.

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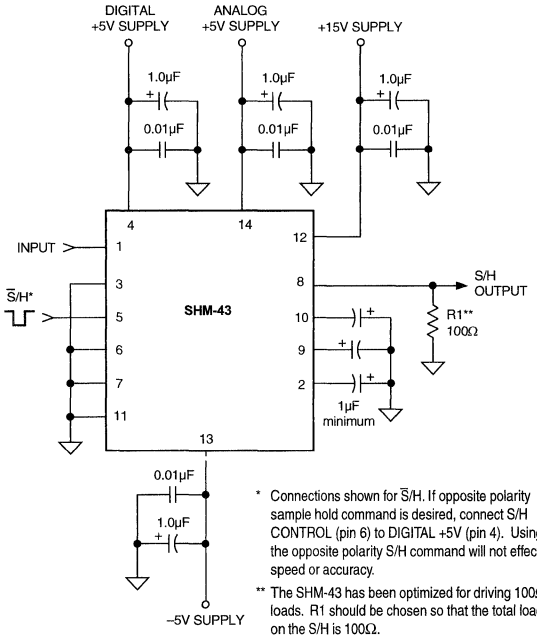


* Connections shown for $\overline{S/H}$. If opposite polarity sample hold command is desired, connect S/H CONTROL (pin 6) to DIGITAL +5V (pin 4). Using the opposite polarity S/H command will not effect speed or accuracy.

** The SHM-43 has been optimized for driving 100Ω loads. R1 should be chosen so that the total load on the S/H is 100Ω.

Figure 2. Test Circuit Connections

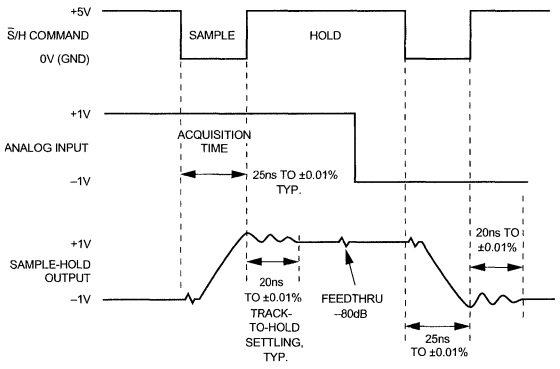
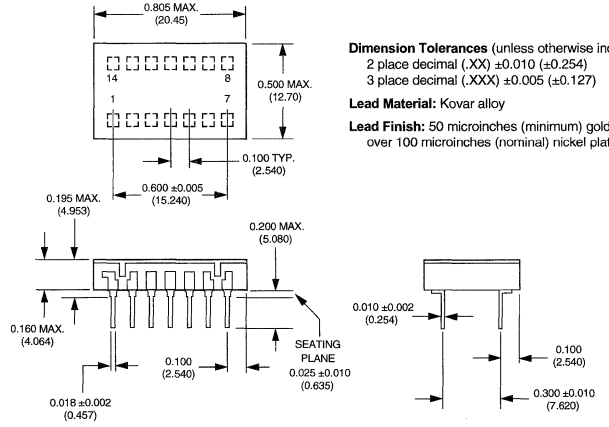


Figure 3. Test Method for Circuit Shown in Figure 2

3

MECHANICAL DIMENSIONS
INCHES (MM)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NO.	TEMPERATURE RANGE
SHM-43MC	0 to +70 °C
SHM-43MM	–55 to +125 °C

Receptacles for pc board mounting are available from Amp, Inc. part number 3-331272-8 (component lead socket), 14 required.

Contact DATEL for availability of a high-reliability (QL) version.

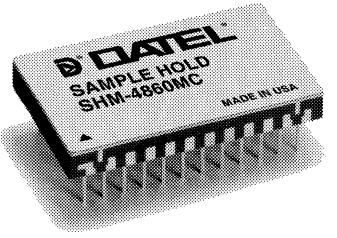
SHM-4860

Industry-Standard, High-Speed ±0.01% Sample-Hold Amplifiers

DATEL INNOVATION and EXCELLENCE

FEATURES

- **200ns Maximum acquisition time**
- **±0.01% Accuracy**
- **100ns Maximum sample-hold settling time**
- **74dB Feedthrough attenuation**
- **±50ps Aperture uncertainty**
- **Industry standard**



GENERAL DESCRIPTION

DATEL's SHM-4860 is a high-speed, highly accurate sample-hold amplifier designed for precision, high-speed analog signal processing applications. Manufactured using modern, high-quality hybrid technology, the SHM-4860 features excellent dynamic specifications including a maximum acquisition time of only 200ns for a 10V step to ±0.01%. Sample-to-hold settling time, to ±0.01% accuracy, is 100ns maximum with an aperture uncertainty of ±50ps.

The SHM-4860 is a complete sample-hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, a FET-input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT	24	+15V SUPPLY
2	N.C.	23	GROUND
3	N.C.	22	–15V SUPPLY
4	N.C.	21	GROUND
5	N.C.	20	N.C.
6	N.C.	19	N.C.
7	N.C.	18	N.C.
8	N.C.	17	N.C.
9	+5V SUPPLY	16	N.C.
10	GROUND	15	GROUND
11	HOLD COMMAND	14	N.C.
12	$\overline{\text{HOLD COMMAND}}$	13	INPUT

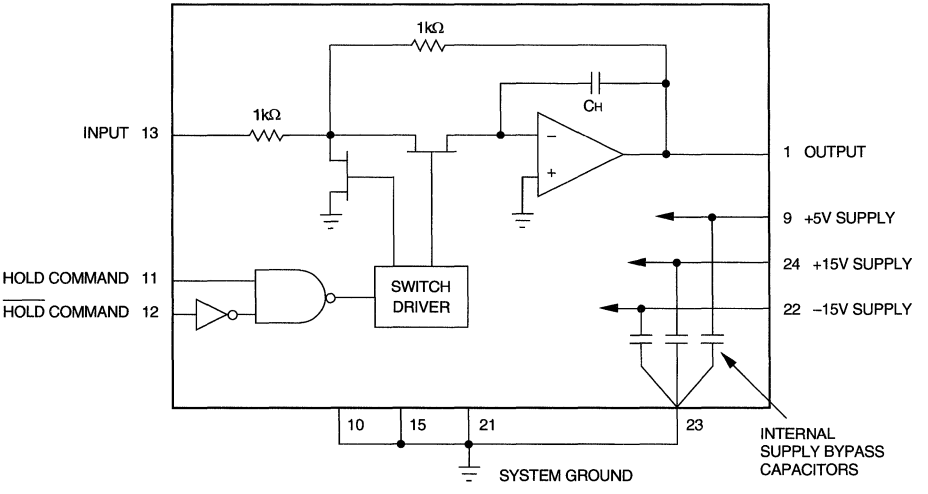


Figure 1. Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS

±15V Supply Voltages, Pins 24, 22	±18V
+5V Supply Voltage, Pin 9	–0.5V to +7V
Analog Input, Pin 13 ①	±18V
Digital Inputs, Pins 11, 12	–0.5V to +7V
Output Current ②	±65mA

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C with ±15V and +5V supplies unless otherwise noted.)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range ①	±10.25	±11.25	—	V
Input Impedance	—	1	—	kΩ
Output Current ②	—	—	±40	mA
Output Impedance		0.1	—	kΩ
Maximum Capacitive Load	—	250	—	pF
DIGITAL INPUT				
Input Logic Level				
Logic "1"	+2.0	—	+5.0	V
Logic "0"	0	—	+0.8	V
Loading				
Logic "1"	—	—	+40	µA
Logic "0"	—	—	–1.6	mA
TRANSFER CHARACTERISTICS				
Gain	—	–1	—	V/V
Gain Accuracy	—	±0.05	±0.1	%
Gain Linearity Error ③	—	±0.005	±0.01	%FS
Sample-Mode Offset Voltage	—	±0.5	±5	mV
Sample-to-Hold Offset Error ④ (Pedestal)	—	±2.5	±20	mV
Gain Tempco (Drift)	—	±0.5	±5	ppm/°C
Sample-Mode Offset Drift	—	±3	±15	⑤
Sample-to-Hold Offset Drift	—	±4	—	⑤
DYNAMIC CHARACTERISTICS				
Acquisition Time				
10V to ±0.01%FS	—	160	200	ns
10V to ±0.1%FS	—	100	170	ns
10V to ±1%FS	—	90	—	ns
1V to ±1%FS	—	75	—	ns
Sample-to-Hold Settling Time				
10V to ±0.01%FS	—	60	100	ns
10V to ±0.1%FS	—	40	—	ns
Sample-to-Hold Transient	—	180	—	mV p-p
Aperture Delay Time	—	6	—	ns
Aperture Uncertainty (Jitter)	—	±50	—	ps
Output Slew Rate	—	±300	—	µV/µs
Small Signal Bandwidth (–3dB)	—	16	—	MHz
Droop: +25°C	—	±0.5	±5	µV/µs
+70°C	—	±15	—	µV/µs
+125°C	—	±1.2	—	mV/µs
Feedthrough Attenuation	—	74	—	dB
Overload Recovery Time				
Positive	—	200	—	ns
Negative	—	700	—	ns
POWER REQUIREMENTS				
Voltage Range: ±15V Supplies	—	±3	—	%
+5V Supply	—	±5	—	%
Power Supply Rejection Ratio	—	±0.5	—	mV/V
Quiescent Current Drain				
+15V Supply	—	+21	+25	mA
–15V Supply	—	–22	–25	mA
+5V Supply	—	+17	+25	mA
Power Consumption	—	730	875	mW

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Ranges	
SHM-4860MC	0 to +70°C (ambient)
SHM-4860MM, 883	–55 to +125°C (case)
Storage Temperature Range	–65 to +150°C
Package Type	24-pin ceramic DDIP

Footnotes:

① Input signal should not exceed the supply voltage.

② The SHM-4860's output is current limited at approximately ±65mA. The device can withstand a sustained short to ground. However, shorts from the output to either supply will cause permanent damage. For normal operation, the load current should not exceed ±40mA.

③ Full Scale (FS) = 10V. Full Scale Range (FSR) = 20V.

④ Sample-to-Hold Offset Error (Pedestal) is constant regardless of input/output level.

⑤ Units are ppm of FSR/°C.

TECHNICAL NOTES

1. All ground pins (10, 15, 21, 23) should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder all four ground pins directly to it. Care must be taken to ensure that no ground potentials can exist between Pin 10 and the other ground pins.

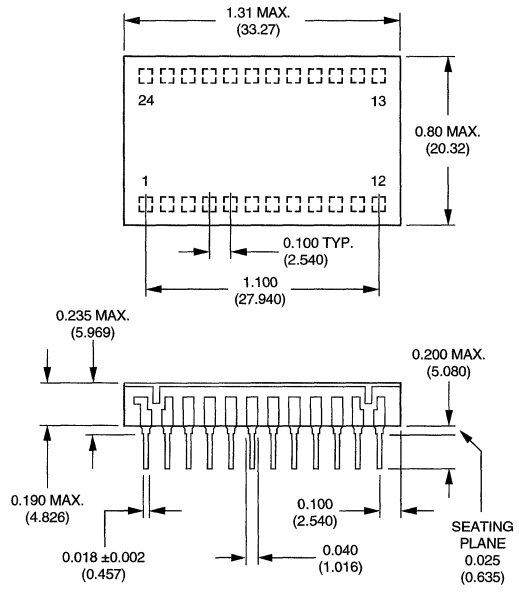
2. Although the power supply pins (9, 22, 24) are internally bypassed to ground with 0.01µF ceramic capacitors, additional external 0.1µF to 1µF tantalum bypass capacitors may be required in critical applications.

3. A logic "0" on the HOLD COMMAND input (Pin 11), or a logic "1" on the $\overline{\text{HOLD}}$ COMMAND input (Pin 12), will put the device in the sample mode. In this mode, the device acts as an inverting unity-gain amplifier, and its output will track its input. A logic "1" on Pin 11 (logic "0" on Pin 12) will put the device in the hold mode, and the output will be held constant at the last input level present when the hold command was given.

   If the HOLD COMMAND input (Pin 11) is used to control the device, Pin 12 must be tied to digital ground. If $\overline{\text{HOLD}}$ COMMAND input (Pin 12) is used to control the device, Pin 11 must be tied to +5V.

4. The maximum capacitive load to avoid oscillation is typically 250pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50pF. However, higher capacitances will affect both acquisition and settling time.

MECHANICAL DIMENSIONS
INCHES (mm)



24-PIN DDIP

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
SHM-4860MC	0 to +70°C
SHM-4860MM	–55 to +125°C
SHM-4860/883	–55 to +125°C

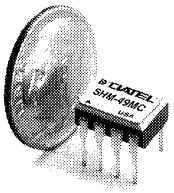
Contact DATEL for 883 product specifications.

DATEL, Inc., 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For immediate assistance 800-233-2765

SHM-49
Miniature, High-Speed ±0.01% Sample-Hold Amplifiers

FEATURES

- **Small 8-pin DIP package**
- **200ns max. acquisition time to ±0.01%**
- **100ns max. sample-to-hold settling time to ±0.01%**
- **16MHz small signal bandwidth**
- **74dB feedthrough attenuation**
- **±25 picoseconds aperture uncertainty**
- **415mW maximum power dissipation**



GENERAL DESCRIPTION

DATEL's SHM-49 is a high-speed, highly accurate sample/hold designed for precision, high-speed analog signal processing applications. The SHM-49 features excellent dynamic specifications including a maximum acquisition time of only 200 nanoseconds for a 10V step to ±0.01%.

Sample-to-hold settling time, to ±0.01% accuracy, is 100 nanoseconds maximum with an aperture uncertainty of ±25 picoseconds.

The SHM-49 is a complete sample/hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, a FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+5V SUPPLY
2	S/$\overline{H}$ CONTROL
3	ANALOG INPUT
4	ANALOG RETURN
5	–15V SUPPLY
6	ANALOG OUTPUT
7	+15V SUPPLY
8	POWER GROUND

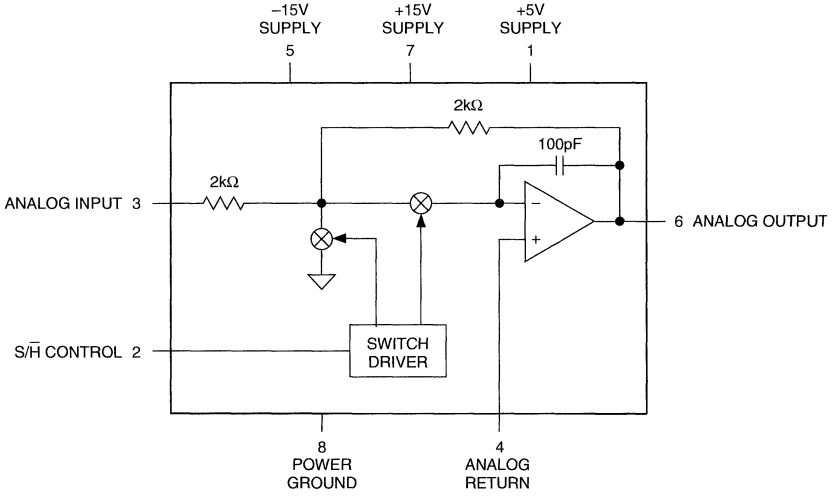


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

±15V Supply Voltage	±18V
+5V Supply Voltage	−0.5V to +7V
Analog Input	±18V
Digital Input	−0.5V to +5.5V
Output Current	±65 mA

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range with ±15V and +5V supplies unless otherwise specified.)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range				
±15V Nominal Supplies	±10	±11.5	—	Volts
±12V Nominal Supplies	±7	±8.5	—	Volts
Input Impedance	1.75	2	—	kΩ
Output Current	—	—	±40	mA
Output Impedance	—	0.1	—	Ω
Capacitive Load	100	250	—	pF
DIGITAL INPUT				
Input Logic Levels				
Logic 1	+2.0	—	+5.0	Volts
Logic 0	0	—	+0.8	Volts
Loading				
Logic 1	—	—	+5	µA
Logic 0	—	—	−5	µA
TRANSFER CHARACTERISTICS				
Gain	—	−1	—	V/V
Gain Error, +25°C	—	±0.05	±0.5	%
Linearity Error ①	—	±0.005	±0.01	%FS
Sample Mode Offset , +25°C	—	±2	±7	mV
Sample-to-Hold Offset (Pedestal), +25°C ②	—	±2.5	±25	mV
Gain Drift	—	±0.5	±15	ppm/°C
Sample Mode Offset Drift ①	—	±3	±15	ppm of FSR/°C
Sample-to-Hold Off. (Pedestal) Drift	—	±5	±20	ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time				
10V to ±0.01%FS (±1 mV)				
+25 °C	—	160	200	ns
−55 to +125 °C	—	—	265	ns
10V to ±0.1%FS (±10 mV)				
+25 °C	—	100	150	ns
−55 to +125 °C	—	—	215	ns
10V to ±1%FS (±100 mV)	—	90	—	ns
1V to ±1%FS (±10 mV)	—	75	—	ns
Sample-to-Hold Settling Time				
10V to ±0.01%FS (±1 mV)	—	60	100	ns
10V to ±0.1%FS (±10 mV)	—	40	80	ns
Sample-to-Hold Transient	—	100	—	mVp-p
Aperture Delay Time	—	10	15	ns
Aperture Uncertainty (Jitter)	—	±25	±50	ps
Output Slew Rate	±200	±300	—	V/µs
Small Signal BW (−3dB)	10	16	—	MHz
Output Droop				
+25 °C	—	±0.5	±10	µV/µs
0 to +70 °C	—	±15	±30	µV/µs
−55 to +125 °C	—	±1.2	±2.4	mV/µs
Feedthrough Rejection	69	74	—	dB

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Voltage Range				
+15V Supply	+11.5	+15.0	+15.5	Volts
−15V Supply	−11.5	−15.0	−15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Power Supply Rejection Ratio	—	±0.5	±1	mV/V
Quiescent Current Drain				
+15V Supply	—	+12	+13.5	mA
−15V Supply	—	−12	−13.5	mA
+5V Supply	—	+1	+1.5	mA
Power Consumption	—	365	415	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
SHM-49MC	0 to +70 °C			
SHM-49MM	−55 to +125 °C			
Storage Temperature Range	−65 to +150 °C			
Thermal Impedance				
θjc	15°C/W			
θca	35°C/W			
Package Type	8-pin ceramic DIP			

Footnotes:

① Full Scale (FS) = 10V. Full Scale Range (FSR) = 20V.

② Sample-to-hold offset error (pedestal) is constant regardless of input/output level.

TECHNICAL NOTES

1. All ground pins should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder ground pins directly to it. Take care to ensure that no ground potentials can exist between ground pins.

2. External 0.1µF to 1µF tantalum bypass capacitors are required in critical applications.

3. A logic 1 on S/$\overline{H}$ puts the unit in the sample mode. A logic 0 puts the unit in hold mode.

4. The maximum capacitive load to avoid oscillation is typically 250pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50pF. Greater load capacitances will affect both acquisition and settling time.

5. Gain and offset adjusting can be accomplished using the external circuitry shown in Figure 2. Adjust offset with a 0V input. Adjust gain with a ±FS input. Adjust so that the output in the hold mode matches the input.

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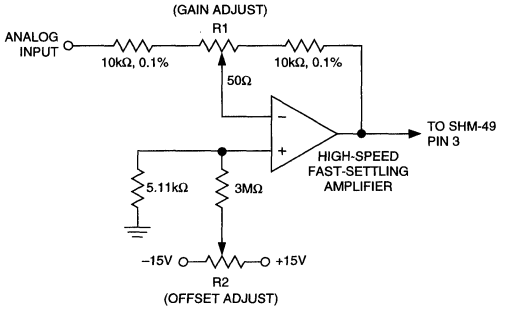
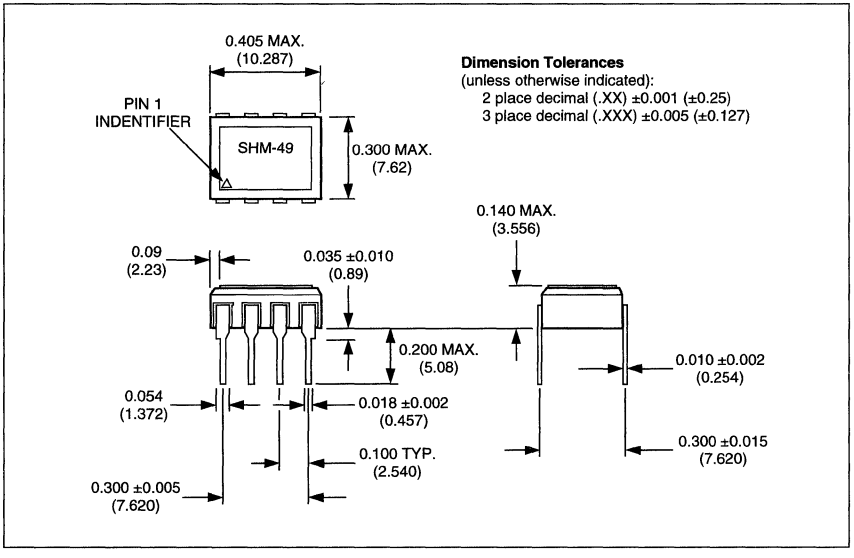


Figure 2. Offset and Gain Adjustments

3

MECHANICAL DIMENSIONS
INCHES (mm)



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
SHM-49MC	0 to +70°C
SHM-49MM	–55 to +125°C

For availability of high-reliability versions of the SHM-49, contact DATEL.

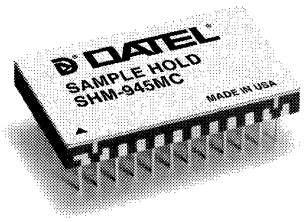
SHM-945

Precision, High-Speed Sample-Hold Amplifiers

DATEL INNOVATION and EXCELLENCE

FEATURES

- **500ns maximum acquisition time to ±0.00076%**
- **Differential input**
- **±0.0004% maximum linearity error**
- **16-bit performance over military temperature range**
- **Small 24-pin DDIP package**
- **User-selectable gain (–0.5, –1, –2)**



GENERAL DESCRIPTION

DATEL's SHM-945 is a precision, high-speed, sample-and-hold amplifier featuring a maximum acquisition time of 500 nanoseconds to ±0.00076% accuracy. Differential inputs are provided to reject common-mode signals found in applications requiring 16-bit accuracy. A range pin allows gain selections of –0.5, –1 and –2.

The SHM-945 contains an internal hold capacitor with internal compensation networks for pedestal error, feedthrough and dielectric absorption.

Packaged in a small, 24-pin, metal-sealed, ceramic DDIP, the SHM-945 requires ±15V and +5V supplies and dissipates 385mW maximum. Its active state can be controlled from either positive or inverted logic.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG OUTPUT	24	+15V SUPPLY
2	N.C.	23	POWER GROUND
3	N.C.	22	–15V SUPPLY
4	N.C.	21	ANALOG GROUND
5	N.C.	20	N.C.
6	N.C.	19	N.C.
7	POWER GROUND	18	N.C.
8	DIGITAL GROUND	17	N.C.
9	+5V SUPPLY	16	N.C.
10	ANALOG INPUT LOW	15	RANGE RETURN
11	$\overline{\text{SAMPLE/HOLD}}$	14	RANGE
12	SAMPLE/$\overline{\text{HOLD}}$	13	ANALOG INPUT HIGH

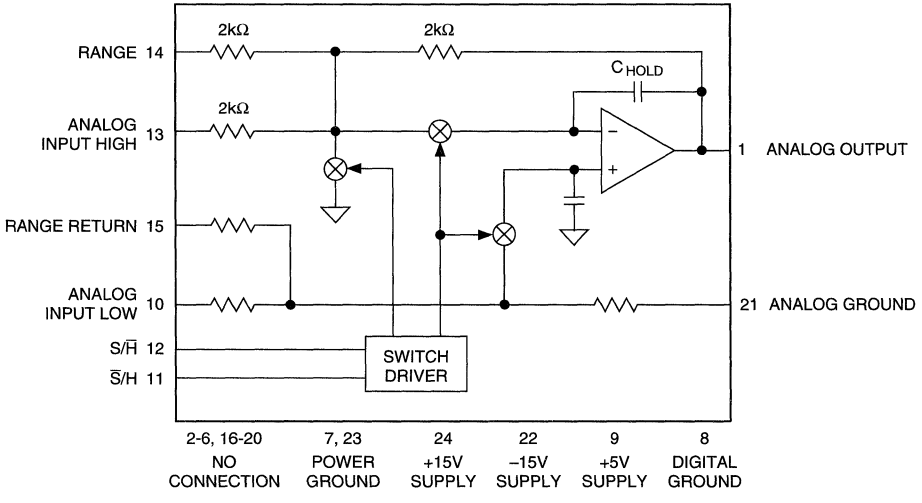


Figure 1. Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (+Vs), Pin 24	–0.5 to +18	Volts
–15V Supply (–Vs), Pin 22	+0.5 to –18	Volts
+5V Supply, Pin 9	–0.5 to +7	Volts
Digital Inputs, Pins 11,12	–0.5 to +7	Volts
Analog Input, Pin 13	–Vs to +Vs	Volts
Lead Temperature (10 seconds)	300	°C
Short Circuit to Ground	50	mA

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range with ±15V and +5V supplies unless otherwise specified. Gain = –1.)

INPUTS	MIN.	TYP.	MAX.	UNITS
Voltage Range	±10	±10.5	—	Volts
Common Mode Voltage Range	±100	—	—	mV
Common Mode Rejection Ratio	86	—	—	dB
Digital Inputs				
Logic 1 Level	+2.0	—	—	Volts
Logic 0 Level	—	—	+0.8	Volts
Logic 1 Loading	—	—	±1	µA
Logic 0 Loading	—	—	±1	µA
OUTPUT				
Voltage Range	±10	±10.5	—	Volts
Output Current	±30	±35	—	mA
Stable Capacitive Load	—	—	50	pF
Output Impedance	—	0.05	0.25	Ohms
PERFORMANCE				
Nonlinearity (DC ±10V)				
+25°C	—	—	±0.0004	%FS
–55 to +125°C	—	—	±0.00076	%FS
Sample Mode Offset Error				
+25°C	—	±0.5	±2	mV
0 to +70°C	—	—	±2.5	mV
–55 to +125°C	—	—	±3	mV
S/H Offset (Pedestal) Error				
+25°C	—	±2	±5	mV
0 to +70°C	—	±5	±7.5	mV
–55 to +125°C	—	±7	±10	mV
Pedestal Nonlinearity	—	—	±0.00076	%FS
Gain	—	–1	—	V/V
Gain Error				
+25°C	—	—	±0.02	%
0 to +70°C	—	—	±0.035	%
–55 to +125°C	—	—	±0.05	%
Harmonic Distortion (Below FS) ①	–96	—	—	dB
Acq. Time, ±0.003%FS, 10V Step				
+25°C	—	275	350	ns
0 to +70°C	—	—	350	ns
–55 to +125°C	—	—	425	ns
Acq. Time, ±0.003%FS, 20V Step				
+25°C	—	375	400	ns
0 to +70°C	—	—	450	ns
–55 to +125°C	—	—	500	ns
Acq. Time, ±0.00076%FS, 10V Step				
+25°C	—	400	500	ns
0 to +70°C	—	—	550	ns
–55 to +125°C	—	—	600	ns
Acq. Time, ±0.00076%FS, 20V Step				
+25°C	—	550	650	ns
0 to +70°C	—	—	700	ns
–55 to +125°C	—	—	750	ns

PERFORMANCE (Cont.)	MIN.	TYP.	MAX.	UNITS
Aperture Delay, +25°C	—	5	10	ns
–55 to +125°C	—	—	13	ns
Aperture Uncertainty, +25°C	—	10	15	ps
–55 to +125°C	—	—	30	ps
Slew Rate	±120	±150	—	V/µs
Full Power BW (±FS)	1.6	1.9	—	MHz
Small Signal BW (–3dB)	12	16	—	MHz
Hold Mode Settling, ±0.003%FS				
+25°C	—	130	150	ns
0 to +70°C	—	—	150	ns
–55 to +125°C	—	—	175	ns
Hold Mode Settling, ±0.00076%FS				
+25°C	—	200	250	ns
0 to +70°C	—	—	250	ns
–55 to +125°C	—	—	300	ns
Feedthrough Rejection, 10V Step	92	100	—	dB
Droop Rate, +25°C	—	±0.5	±1	µV/µs
0 to +70°C	—	—	±50	µV/µs
–55 to +125°C	—	250	±500	µV/µs
Output Noise, Hold Mode	—	580	—	µVrms
POWER SUPPLY REQUIREMENTS				
Range, +15V	+14.25	+15.0	+15.75	Volts
–15V	–14.25	–15.0	–15.75	Volts
+5V	+4.75	+5.0	+5.25	Volts
Current, +15V	—	+10	+12	mA
–15V	—	–10	–12	mA
+5V	—	+0.5	+1.5	mA
Power Dissipation	—	305	385	mW
Power Supply Rejection	88	110	—	dB
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
SHM-945MC	0	—	+70	°C
SHM-945MM	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type	24-pin ceramic DDIP			
Weight	0.28 ounces (8 grams)			

① DC to 1 MHz, 10Vp-p.

TECHNICAL NOTES

1. Bypass the ±15V and +5V supplies with 1µF, 25V tantalum electrolytic capacitors in parallel with a 0.01µF ceramic capacitors mounted as close to the pins as possible.

2. Tie all ground pins together at a single ground point beneath the device and use a short, low-impedance run to the ground of the analog power supplies. The ground point should be a solid ground plane under the sample/hold and related A/D converter.

3. Differential amplifier - high-resolution applications frequently require the ability to sense ground at a distant signal source. To avoid errors due to different ground potentials, use the SHM-945's Analog Input Low (pin 10) to sense the ground at the signal source. In noisy applications, using shielded twisted pair wire, with one end of the shield tied to ground at the sample/hold, is recommended. Analog Input Low and Range Return (when used) must be ≤100mV maximum with respect to Analog Ground.

4. For gain range selection refer to Figure 2 and Table 1.

5. When using the $\overline{\text{Sample}}$/Hold control pin (pin 11), connect pin 12 to Digital Ground. If using the Sample/$\overline{\text{Hold}}$ control pin (pin 12), tie pin 11 to +5V.

6. The offset, pedestal and gain errors of the SHM-945 are laser trimmed at DATEL and no external compensation capabilities have been provided. This prevents introducing noise through the offset adjust terminals of the S/H amplifier and guarantees excellent gain linearity, offset drift, and pedestal performance.

Most A/D converters provide offset and gain adjustment capabilities with a range capable of eliminating the gain and offset contributions of the SHM-945. The offset errors in the SHM-945 include the sample-mode offset error and the error incurred when going into the hold mode (pedestal error). These combined offset errors should be adjusted with the Sample-Hold being actively sampled and held to assure the pedestal error is removed.

Table 1. SHM-945 Gain Range Selection

GAIN	Connect Pin 14 to:	Connect Pin 15 to:
–0.5	Pin 1	Pin 21 (Ground)
–1.0	Do Not Connect	Do Not Connect
–2.0	Pin 13	Pin 21 (Ground)

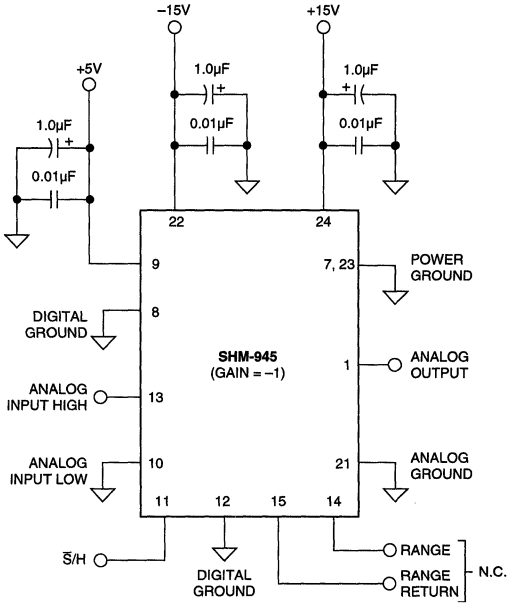
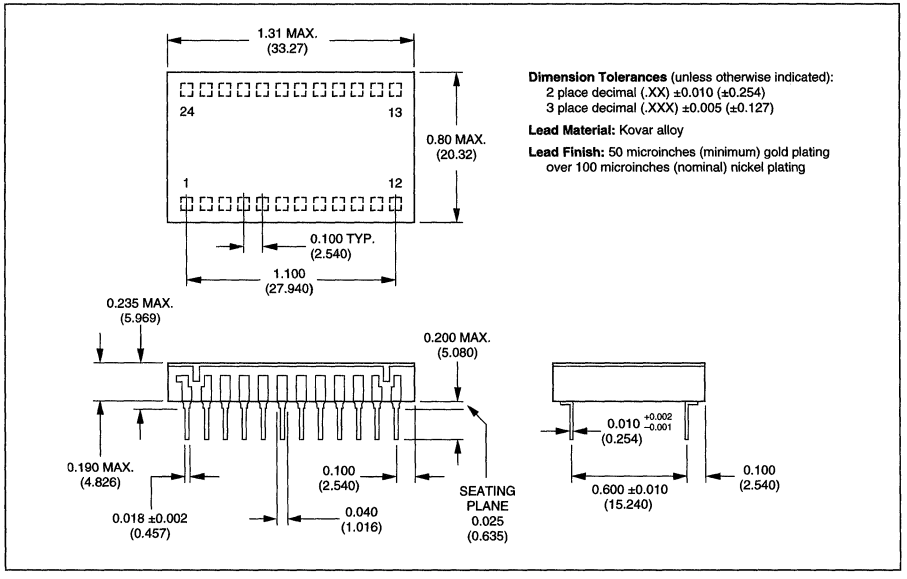


Figure 2. SHM-945 Typical Connection Diagram

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
SHM-945MC	0 to +70°C
SHM-945MM	–55 to +125°C

For availability of MIL-STD-883 decices, contact DATEL.

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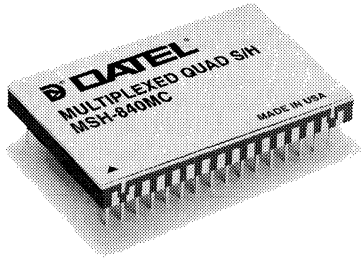
MSH-840
Quad, Simultaneous Sample-Hold with Multiplexer

FEATURES

- **4 Simultaneous sample-hold amplifiers**
- **Internal 4-channel multiplexer**
- **775ns acquisition time**
  10V step to ±0.01% (including multiplexer)
- **2 Channels with optional X10 gain**
- **Control logic for interfacing to A/D's**
- **100MΩ minimum input impedance**
- **Low power, 2.25 Watts**
- **Small, 32-pin, ceramic TDIP**
- **–55°C to +125°C versions**



GENERAL DESCRIPTION

The MSH-840 is a quad, simultaneous sample-hold featuring an acquisition time (including the internal multiplexer!) of 775 ns for a 10V step to ±0.01% accuracy. Control logic is provided for strobing the channels simultaneously and for interfacing to A/D's. A four-channel multiplexer allows individual S/H outputs to be selected.

The MSH-840 requires ±15V and +5V power supplies and dissipates just 2.25 Watts. Packaged in a small, 32-pin, ceramic TDIP, both commercial 0 to +70°C and military –55 to +125°C operating temperature range models are offered.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIGITAL GROUND	32	$\overline{\text{RESET}}$
2	+5V SUPPLY	31	$\overline{\text{EOC}}$ IN
3	SSH1 IN	30	$\overline{\text{S/H}}$ IN
4	OFFSET ADJUST 1	29	CONVERT IN
5	SSH1 OUT	28	START CONVERT OUT
6	SSH2 IN	27	CA0
7	OFFSET ADJUST 2	26	CA1
8	SSH2 OUT	25	ANALOG GROUND
9	SSH3 IN	24	MUX IN1
10	OFFSET ADJUST 3	23	MUX IN2
11	GX10 CH3	22	MUX IN3
12	SSH3 OUT	21	MUX IN4
13	SSH4 IN	20	MUX OUTPUT
14	OFFSET ADJUST 4	19	–15V SUPPLY
15	GX10 CH4	18	POWER GROUND
16	SSH4 OUT	17	+15V SUPPLY

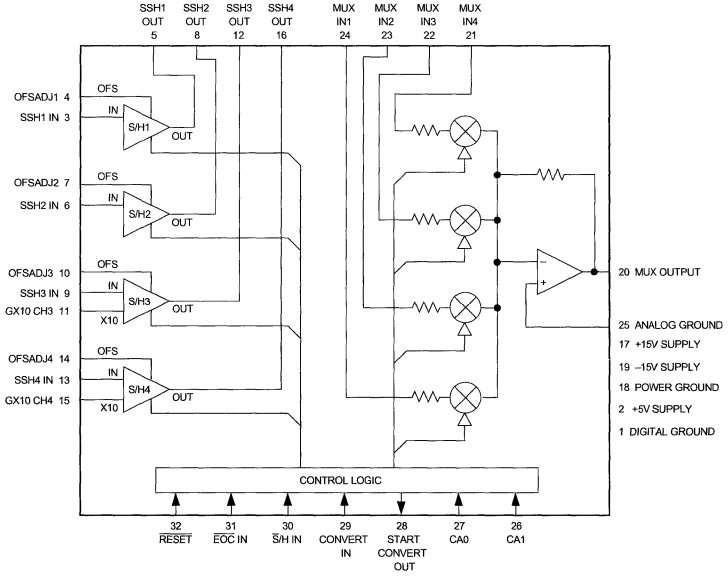


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETER	LIMITS	UNITS
+15V Supply, Pin 17	0 to +18	Volts
–15V Supply, Pin 19	0 to -18	Volts
+5V Supply, Pin 2	–0.5 to +7.0	Volts
Digital Inputs, Pins 26-27, 29-32	–0.3 to +5.5	Volts
Analog Inputs, Pins 3, 4, 6, 7, 9, 10, 13, 14	–Vcc to +Vcc	Volts
Lead Temperature (10 seconds)	300	°C
Output Short Circuit To Ground	50	mA

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range and at ±15V and +5V unless specified.)

INPUTS	MIN.	TYP.	MAX.	UNITS
Input Type		Single-Ended		
Input Voltage Ranges	—	±10V	—	Volts
Input Impedance	100	—	—	MΩ
Digital Inputs				
Logic Levels				
Logic 1	+2.0	—	—	Volts
Logic 0	—	—	+0.8	Volts
Logic Loading				
Logic 1	—	—	+1.0	µA
Logic 0	—	—	–1.0	µA
CONVERT IN Minimum Pulse Width				
+25°C	20	—	—	ns
0 to +70°C	25	—	—	ns
–55 to +125°C	40	—	—	ns
OUTPUTS				
Output Range	±10	—	—	Volts
Output Current	—	—	±20	mA
Stable Capacitive Load	100	—	—	pF
Output Impedance	—	0.003	—	Ω
START CONVERT OUT Pulse Width	40	50	60	ns
CONVERT IN to START CONVERT OUT delay				
+25°C	—	—	60	ns
0 to +70°C	—	—	75	ns
–55 to +125°C	—	—	90	ns
PERFORMANCE				
Nonlinearity ⑤	—	±0.005	±0.01	%FS
Nonlinearity TC	—	—	±1	④
Sample Mode Offset Error (Gain =1)	—	±2	±15	mV
Sample Mode Offset Error (Gain =10)	—	±20	±150	mV
Sample Mode Offset Tempco	—	±2	±4	④
Offset Adjustment Range	±0.5			%FS
S/H Offset (Pedestal) Error (Over Full Input)	—	—	±10	mV
Gain	—	+1	—	V/V
Gain Tempco (+ tempco of gain pot. or resistor)	—	±2	±5	ppm/°C
Gain Adjustment Range	±1	—	—	%
Gain Error (Externally Adjustable to Zero)				
25Ω gain resistor	—	—	±0.3	%
50Ω gain resistor	—	—	±0.3	%
No gain resistor (shorted)	—	—	±0.3	%
Harmonic Distortion (dc to 500kHz, 20Vp-p)	–69	–70	—	dB

PERFORMANCE (Cont.)	MIN.	TYP.	MAX.	UNITS
Acquisition Time ①				
±0.1%FS, 20V Step	—	800	850	ns
±0.01%FS, 10V Step ②	—	775	900	ns
±0.01%FS, 20V Step	—	1.2	1.4	µs
±0.003%FS, 20V Step	—	1.5	2.0	µs
Aperture Delay	—	15	60	ns
Aperture Uncertainty	—	15	50	psec
Slew Rate	±45	—	—	V/µs
Full Power BW	300	500	—	kHz
Small Signal BW (–3dB)	8	13	—	MHz
Hold Mode Settling Time				
To ±10mV	—	—	100	ns
To ±1mV	—	—	200	ns
To ±0.3mV	—	—	300	ns
Feedthrough Rejection (20V Step)	—	–74	–70	dB
Hold Mode Crosstalk ③	—	–74	–70	dB
Droop Rate				
+25°C	—	—	±1.5	µV/µs
0 to +70°C	—	—	±25	µV/µs
–55 to +125°C	—	—	±3	mV/µs
Output Noise, Hold Mode	—	—	600	µVrms
POWER REQUIREMENTS				
Ranges				
+15V Supply	+14.25	+15	+15.75	Volts
–15V Supply	–14.25	–15	–15.75	Volts
+5V Supply	+4.5	+5	+5.25	Volts
Currents				
+15.75V Supply	—	+75	+90	mA
–15.75V Supply	—	–75	–90	mA
+5V Supply	—	—	+1.0	mA
Power Dissipation	—	2.25	2.75	Watts
Power Supply Rejection	—	—	±0.006	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
MSH-840MC	0	—	+70	°C
MSH-840MM	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type	32-pin, metal-sealed, ceramic DIP			
Weight	0.5 ounces (14.2 grams)			

Footnotes:

① Includes multiplexer.
② +25°C
③ 500kHz
④ Units are ppm of FS/°C.
⑤ FS = full scale = 10V.

TECHNICAL NOTES

1. Avoid ground related problems by connecting the analog, power and digital grounds to one point, the ground plane beneath the MSH-840. The analog, power and digital grounds are not connected to each other internally.
2. Bypass the analog and digital supplies to ground with a 2.2µF, 25V tantalum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor.
3. Offset adjustments are provided by connecting the offset adjust pins (OFSADJ1-4) to the wipers of 20kΩ trimpots connected between the ±15 Volt power supplies. For operation without offset adjustments, connect these pins to ground.

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4. Gain adjustments are made by connecting 50Ω trimpots between each SSH OUT pin and its respective MUX IN pin. See the typical connection diagram in Figure 4. For the most accurate operation without adjustment, use a 25Ω fixed resistor instead of a trimpot. A short between the respective SSH OUT and MUX IN pins can also be used for operation without adjustment, but with increased gain error.
5. A gain of 10 is possible on channels 3 and 4 by grounding pins GX10 CH3 (pin 11) or GX10 CH4 (pin 15) respectively. Do not connect GX10 CH3/CH4 for gain = 1 operation.

Scan Mode (Simultaneous Sample-Hold)

The MSH-840's scan mode allows sampling up to four channels at the same time. There are two ways to put the MSH-840 into a sampling mode:

1. Toggling the $\overline{\text{RESET}}$ line (pin 32) low and then high again, upon power-up for instance, puts the four sample-holds into the sampling mode.

2. The four sample-holds can also be put into the sampling mode by using the $\overline{\text{S/H}}$ IN control line (pin 30). Using pin 30 is preferred over toggling the $\overline{\text{RESET}}$ line because pin 30 can also put the MSH-840 into the hold mode.

After waiting for the appropriate acquisition time, all four sample-holds can be simultaneously put into the hold mode by bringing the $\overline{\text{S/H}}$ IN pin to a high state.

External A/D conversions can begin after waiting for the appropriate hold mode settling time. The rising edge of a signal on CONVERT IN (pin 29) generates a 50ns start convert pulse on the START CONVERT OUT line (pin 28). An external A/D converter requiring 50ns start convert pulses could use these pulses to begin conversions.

Refer to Table 1 to see how channel address selectors CA0 and CA1 (pins 27, 26) select the particular channel to be digitized by the A/D converter. $\overline{\text{EOC}}$ IN serves no function in this simultaneous scan mode and should be tied to ground.

$\overline{\text{RESET}}$ = Resets all sample-holds to the sample mode ($\overline{\text{S/H}}$ must be low during the negative transition of $\overline{\text{RESET}}$)

$\overline{\text{S/H}}$ IN = Sets all sample-holds to hold mode

= Sets all sample-holds to sample mode

CONVERT IN = Internally generates a start convert pulse for use with an external A/D converter

$\overline{\text{EOC}}$ IN = No function during scan (while $\overline{\text{S/H}}$ is high)

START CONVERT OUT = A 50 nanosecond positive pulse generated by CONVERT IN

CA0 and CA1 = A two-bit binary word to select one of the four multiplexer channels

Table 1. Output Channel Selection

	CA1	CA0
Channel 1	0	0
Channel 2	0	1
Channel 3	1	0
Channel 4	1	1

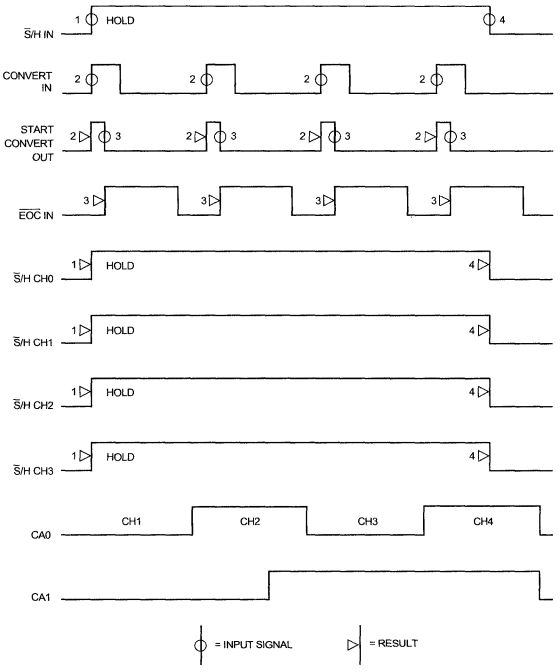

Figure 2. MSH-840 Scan Mode Timing

Random Single Channel Mode

The MSH-840's single channel mode can randomly select a particular channel(s) for digitization by an external A/D converter. Once again, the $\overline{\text{RESET}}$ function can set all sample-holds to the sample mode on initial power-up. Channels are selected using the CA0 and CA1 channel address pins. The S/H IN pin serves no function in this mode and should be tied to ground.

A high-to-low falling edge on $\overline{\text{EOC}}$ IN (pin 31) puts the particular channel chosen into the sample mode. After the initial falling edge on $\overline{\text{EOC}}$ IN, this signal could be derived from the A/D converter's EOC or status pin, which would indicate completion of the previous conversion. The sample-hold could then be put back into the sample mode.

A low-to-high rising edge on the CONVERT IN pin puts the selected channel into the hold mode. After putting the sample-hold into hold, this same edge generates a 50 ns wide start convert signal on START CONVERT OUT (pin 28). An external A/D converter requiring 50ns start convert pulses could use these pulses to begin conversions.

$\overline{\text{RESET}}$ = Resets all sample-holds to the sample mode ($\overline{\text{S}}$/H must be low during the negative transition of RESET)

$\overline{\text{S}}$/H IN = Tie to ground

CONVERT IN = Sets the channel selected by CA0 and CA1 to hold and internally generates a start convert pulse for use with an external A/D converter

$\overline{\text{EOC}}$ IN = Sets the selected sample-hold to the sample mode

START CONVERT OUT = A 50 nanosecond positive pulse generated by CONVERT IN

CA0 and CA1 = A two-bit binary word to select one of the four multiplexer channels

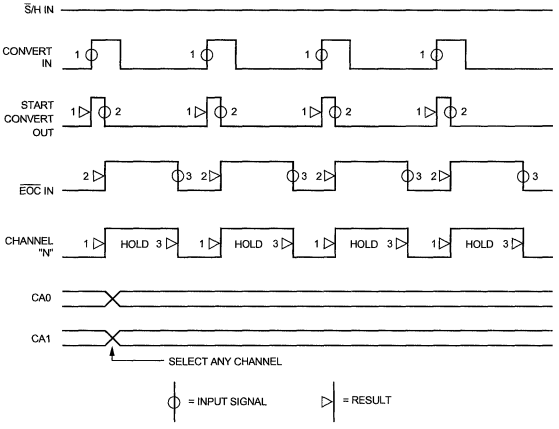

Figure 3. MSH-840 Single-Channel Mode Timing

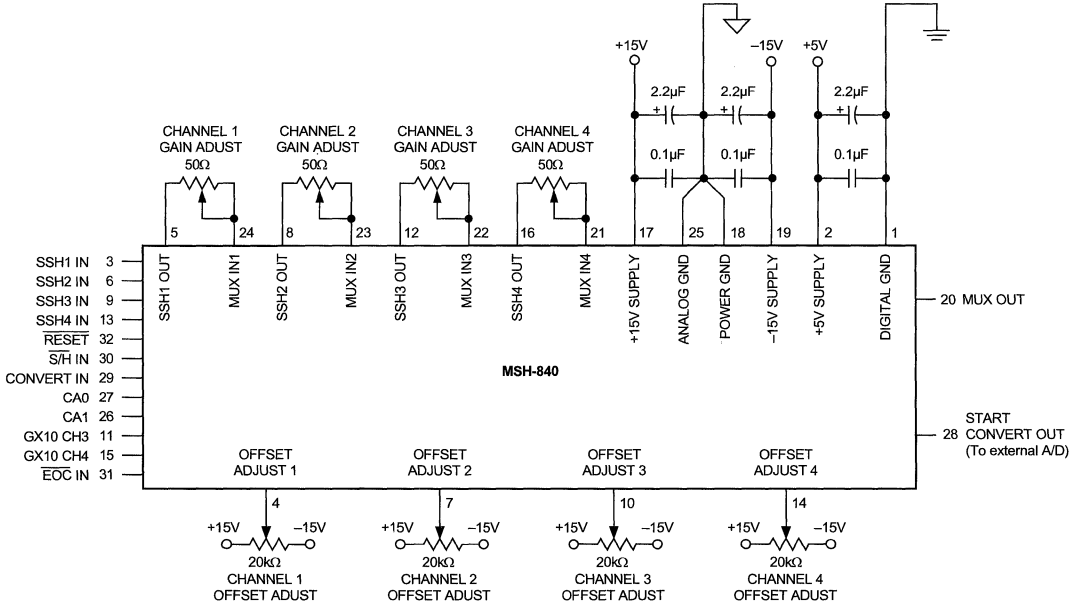

Figure 4. Typical Connection Diagram

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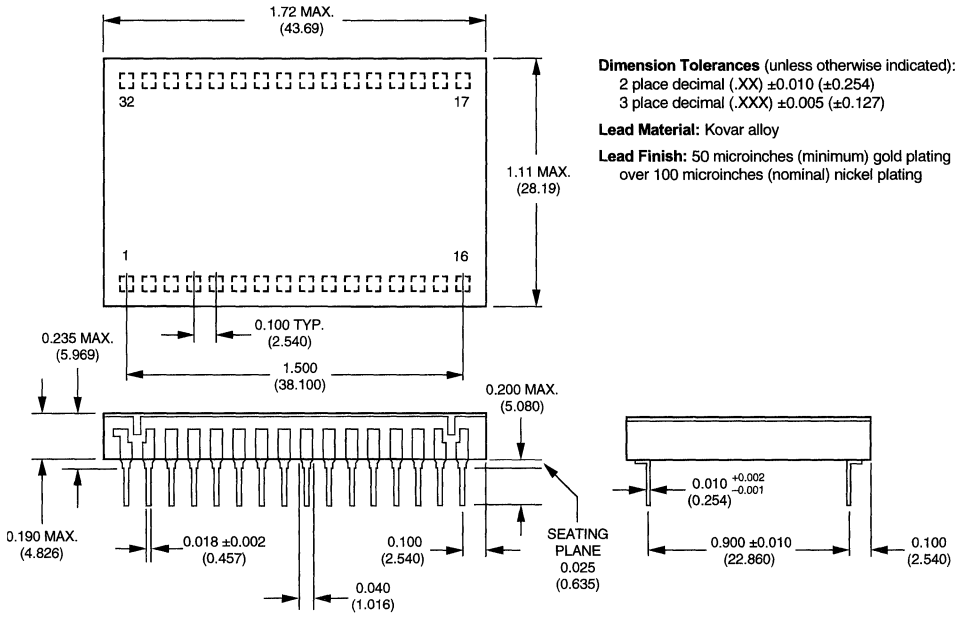
MECHANICAL DIMENSIONS
INCHES (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

3

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE
MSH-840MC	0 to +70°C
MSH-840MM	–55 to +125°C

ACCESSORIES
Receptacle for PC board mounting is available from AMP, Inc. Part Number 3-331272-8 (Component Lead Socket), 32 required.

For availability of a MIL-STD-883 version, contact DATEL.

Other DATEL Literature

ISO 9001 REGISTERED

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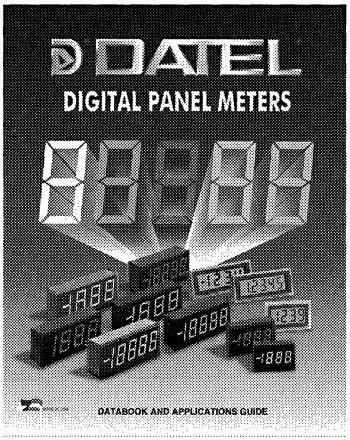
NEW 152-page, full-color catalog! Data sheets and applications for high-quality, low-cost, modular DC/DC Converters: 3-50W, single/dual/triple outputs, wide-range inputs (4.6-13.2V, 9-36V, 18-72V), isolated and non-isolated, many 3.3V devices. New Products: 5W in 1" x 1"; 40W/12A, non-isolated, 5V-to-3.3V; 20W triples in 2" x 2"; 30W triples. 50 pages on theory, testing and applications. Quality assurance, custom capabilities and EMI/EMC facilities described.

Digital Panel Voltmeters & Instruments



NEW 100-page, full-color catalog! Selection guides, performance specs and a full set of application notes for 200 3 1/2 and 4 1/2 digit, low-cost, miniature, panel or board-mount DPM's. 12-pin DIP packages. LED/LCD displays. LCD meters operate from +5V or 9V batteries. 7 LED colors. New, low-power LED meters compete with LCD's. Ap notes for ammeters, tachometers, battery monitors, 4-20mA, etc. Includes "plug-in" ac meters, "plug-on" application boards, self-powered instruments and smart displays.

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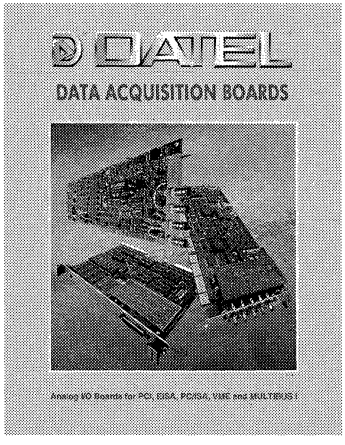

NEW 216-page catalog! Data sheets, applications and sample software for industry's leading line of high-speed analog I/O boards for PCI, EISA, PC/ISA, VME and Multibus. Streaming data acquisition with FIFO's, RAM's, COMM ports and DSP's. 1-256 input channels. 12/14/16-bit A/D's to 10MHz. Simultaneous sampling with 2-16 A/D's. Arbitrary waveform generators (2-16 channels). Programmable power supplies. Power-supply test cards. Windows and LabVIEW® bridge software.

Application Notes

DATEL publishes a set of 8 application notes for data acquisition applications as listed below. Our DC/DC Converter and Panel Meter catalogs also include extensive applications sections.

- **AN-1** High-Speed A/D Converter Designs: Layout and Interfacing Pitfalls
- **AN-2** Picking the Right S/H Amp for Various Data Acquisition Needs
- **AN-3** Data Converters: Getting to Know Dynamic Specs
- **AN-4** Understanding Data Converter Frequency Domain Specifications
- **AN-5** Subranging ADC's: Architectures, Specifications and Testing
- **AN-6** Seeing is Believing: A/D Converters Make the Difference in Imaging Applications
- **AN-7** Modifying Start Convert Pulses Using Commercially Available Devices
- **AN-8** Heat Sinks for DIP Data Converters

For literature or technical assistance

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DATEL's new CDS-1401 (±10V input, 1.25MHz pixel rate in a 14-bit system) and CDS-1402 (±2.5V input, 5MHz pixel rate in a 14-bit system) are complete, single-channel, CDS circuits that implement the critical analog-signal-processing function at the output of CCD's (charge coupled devices) in electronic-imaging applications. Each is a reasonably priced, extremely versatile device that exploits a new "sample-subtract-sample" architecture optimized for both speed (throughput) and dynamic range (signal-to-noise ratio).

DATEL is extremely adept at developing high-speed, wide-dynamic-range sampling and A/D-conversion functions for electronic-imaging applications. Our MCM (multi-chip-module) technology enables us to combine different components, fabricated using different semiconductor process technologies, into a single-package function that exploits the best capabilities of each technology.

We recognize that no two imaging systems are the same and welcome the opportunity, for OEM applications, to tailor an application-specific solution that gives your system the cost/performance advantage it needs to beat your competition. Please contact our applications engineering group to discuss your requirements.

A summary listing of DATEL's high-performance Sampling A/D Converters appears on the following page.

Table of Contents

Selection Guide

Model	Minimum Guaranteed Pixel Rate (MHz)①	Full Scale Input Range (Volts)	Broadband Noise (μVrms)	Dynamic Range (dB)	Signal Acquisition Time (nsec)	Power Supplies (Volts)	Power Dissipation (mW)	Page
CDS-1401	1.25	±10	200	91	250 ②	±15, +5	700	4-3
CDS-1402	5	±2.5	200	79	65 ③	±5	350	4-11

① When used in a 14-bit application. Higher throughputs obtainable at lower resolutions.
② 5V step acquired to ±1mV accuracy.
③ 2V step acquired to ±1mV accuracy.

Selection Guides

Sampling Analog-to-Digital Converters

10-Bit and 12-Bit Resolution ①

Model ②	Sampling Rate (MHz)	Input Range(s) (Volts)	DNL (LSB)	No Missing Codes ③	SNR (dB)	THD (–dB)	Power Supplies (Volts)	Power Dissipation (Watts)	Package	MIL-STD-883 Screening	Page
ADS-325A	20	+2 to +4	±0.5	Yes	54	65	+5	0.15	48-Pin VQFP	No	**1-31**
ADS-112	1	±5, 0 to +10	±0.5	Yes	72	78	±15, +5	1.3	24-Pin DDIP	Yes	**1-3**
ADS-CCD1201④	1.2	0 to +10	±0.25	Yes	73	84	±15, +5	1.7	24-Pin DDIP	No	**1-167**
ADS-117	2	±5, 0 to +10	±0.5	Yes	70	73	±15, +5	1.6	24-Pin DDIP	Yes	**1-9**
ADS-CCD1202④	2	0 to +10	±0.25	Yes	71	78	±15, +5	1.7	24-Pin DDIP	No	**1-175**
ADS-118	5	±1	±0.5	Yes	69	71	±5	1.3	24-Pin DDIP	No	**1-15**
ADS-118A	5	±1.25	±0.5	Yes	69	71	±5	1.3	24-Pin DDIP	No	**1-15**
ADS-119	10	±1.5	±0.5	Yes	69	68	±5	1.8	24-Pin DDIP	Yes	**1-23**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① The ADS-325A has 10-bit resolution. All other devices in this table are 12-bit converters.
② DATEL offers MC (0 to +70°C) and MM (–55 to +125°C) versions of each model. ③ Guaranteed over the full military temperature range (–55 to +125°C).
④ The ADS-CCD1201/2 have been optimized for electronic-imaging applications. They are pin-compatible and operate from either ±12V or ±15V supplies.

14-Bit Resolution

Model ①	Sampling Rate (MHz)	Input Range(s) (Volts)	DNL (LSB)	No Missing Codes ②	SNR (dB)	THD (–dB)	Power Supplies (Volts)	Power Dissipation (Watts)	Package	MIL-STD-883 Screening	Page
ADS-916 ③	0.5	0 to +10	±0.5	Yes	80	82	±15, +5	1.6	24-Pin DDIP	No	**1-39**
ADS-926 ③	0.5	±5	±0.5	Yes	80	87	±15, +5	1.6	24-Pin DDIP	Yes	**1-63**
ADS-917 ③	1	0 to +10	±0.5	Yes	78	80	±15, +5	1.7	24-Pin DDIP	No	**1-47**
ADS-927 ③	1	±5	±0.5	Yes	78	80	±15, +5	1.7	24-Pin DDIP	Yes	**1-71**
ADS-941	1	±5, 0 to +10	±0.5	Yes	78	83	±15, +5	2.8	32-Pin TDIP	No	**1-117**
ADS-919 ③	2	0 to +10	±0.5	Yes	77	76	±15, +5	1.7	24-Pin DDIP	No	**1-55**
ADS-929 ③	2	±5	±0.5	Yes	77	79	±15, +5	1.7	24-Pin DDIP	Yes	**1-79**
ADS-942	2	±5, 0 to +10	±0.5	Yes	75	80	±15, +5	2.9	32-Pin TDIP	No	**1-123**
ADS-942A	2	±5, 0 to +10	±0.5	Yes	75	80	±15, ±5	2.2	32-Pin TDIP	No	**1-129**
ADS-943	3	±2	±0.5	Yes	79	78	±5	1.8	24-Pin DDIP	Yes ④	**1-135**
ADS-944	5	±1.25	±0.5	Yes	76	77	±15, +5, –5.2	2.95	32-Pin TDIP	Yes	**1-143**
ADS-946	8	±2	±0.5	Yes	76	76	±5	1.9	24-Pin DDIP	Yes ④	**1-159**
ADS-945	10	±1.25	±0.5	Yes	78	80	±15, +5, –5.2	4.2	Custom DIP	No	**1-151**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① DATEL offers MC (0 to +70°C) and MM (–55 to +125°C) versions of each model. ② Guaranteed over the full military temperature range (–55 to +125°C).
③ ADS-916, 917, 919, 926, 927 and 929 are all pin-compatible and operate from either ±12V or ±15V supplies. ④ Available Q4-96.

16-Bit Resolution

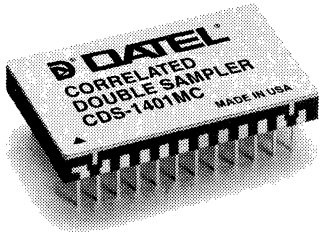
Model ①	Sampling Rate (MHz)	Input Range(s) (Volts)	DNL (LSB)	No Missing Codes ②	SNR (dB)	THD (–dB)	Power Supplies (Volts)	Power Dissipation (Watts)	Package	MIL-STD-883 Screening	Page
ADS-930	0.5	±5, 0 to –10	±0.5	Yes	83	89	±15, +5	3.5	40-Pin TDIP	No	**1-87**
ADS-931	1	±2.75	±0.5	Yes	87	89	±5	1.85	40-Pin TDIP	No	**1-95**
ADS-937	1	±5, 0 to –10	±0.5	Yes	84	85	±15, ±5	1.1	32-Pin TDIP	No	**1-111**
ADS-932	2	±2.75	±0.5	Yes	86	88	±5	1.85	40-Pin TDIP	No	**1-103**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① DATEL offers MC (0 to +70°C) and MM (–55 to +125°C) versions of each model. ② Guaranteed over the full military temperature range (–55 to +125°C).

CDS-1401
14-Bit, Fast-Settling Correlated Double Sampling Circuit

FEATURES

- **Use with 10 to 14-bit A/D converters**
- **1.25 Megapixels/second minimum throughput (14 bits)**
- **±10V input/output ranges, Gain = –1**
- **Low noise, 200µVrms**
- **Two independent S/H amplifiers**
- **Gain matching between S/H's**
- **Offset adjustments for each S/H**
- **Four external A/D control lines**
- **Small package, 24-pin ceramic DDIP**
- **Low power, 700mW**
- **Low cost**



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OFFSET ADJUST V1	24	+15V ANALOG SUPPLY
2	OFFSET ADJUST I1	23	ANALOG GROUND
3	ANALOG INPUT 1	22	V OUT
4	ANALOG INPUT 2	21	ANALOG GROUND
5	ANALOG GROUND	20	$\overline{\text{A/D CLOCK2}}$
6	S/H1 OUT	19	A/D CLOCK2
7	S/H1 ROUT	18	A/D CLOCK1
8	S/H2 SUMMING NODE	17	$\overline{\text{A/D CLOCK1}}$
9	OFFSET ADJUST V2	16	+5V DIGITAL SUPPLY
10	OFFSET ADJUST I2	15	DIGITAL GROUND
11	S/$\overline{\text{H1}}$ COMMAND	14	ANALOG GROUND
12	S/$\overline{\text{H2}}$ COMMAND	13	–15V ANALOG SUPPLY

GENERAL DESCRIPTION

The CDS-1401 is an application-specific, correlated double sampling (CDS) circuit designed for electronic-imaging applications that employ CCD's (charge coupled devices) as their photodetector. The CDS-1401 has been optimized for use in digital video applications that employ 10 to 14-bit A/D converters. The low-noise CDS-1401 can accurately determine each pixel's true video signal level by sequentially sampling the pixel's offset signal and its video signal and subtracting the two. The result is that the consequences of residual charge, charge injection and low-frequency "kTC" noise on the CCD's output floating capacitor are effectively eliminated. The CDS-1401 can also be used as a dual sample-hold amplifier in a data acquisition system.

The CDS-1401 contains two sample-hold amplifiers and appropriate support/control circuitry. Features include independent offset-adjust capability for each S/H, adjustment for matching gain between the two S/H's, and four control lines for triggering the A/D converter used in conjunction with the CDS-1401. The CDS circuit's "ping-pong" timing approach (the offset signal of the "n+1" pixel can be acquired while the video output of the "nth" pixel is being converted) guarantees a minimum throughput, in a 14-bit application, of 1.25MHz. In other words, the true video signal (minus offset) will be available

(continued on page 4-5)

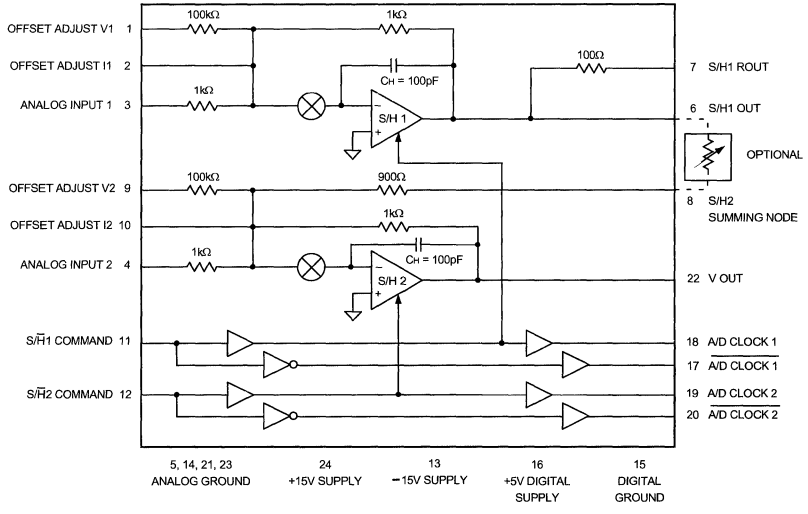


Figure 1. CDS-1401 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 24)	0 to +16	Volts
–15V Supply (Pin 13)	0 to –16	Volts
+5V Supply (Pin 16)	0 to +6	Volts
Digital Inputs (Pins 11, 12)	–0.3 to +V_{DD} +0.3	Volts
Analog Inputs (Pins 3, 4)	±12	Volts
Lead Temp. (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
CDS-1401MC	0	—	+70	°C
CDS-1401MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	5	—	°C/W
θca	—	22	—	°C/W
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP			
Weight	0.42 ounces(12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V, pixel rate = 1.25MHz, and a minimum warmup time of two minutes unless otherwise noted.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUTS ①	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range	±10	—	—	±10	—	—	±10	—	—	Volts
Input Resistance	—	1000	—	—	1000	—	—	1000	—	Ohms
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2	—	—	+2	—	—	+2	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+10	—	—	+10	—	—	+10	µA
Logic Loading "0"	—	—	–10	—	—	–10	—	—	–10	µA
PERFORMANCE										
Sample Mode Offset Error - S/H1	—	±1	±10	—	±2	±10	—	±4	±10	mV
Gain Error - S/H1	—	±0.2	±1	—	±0.25	±1	—	±0.3	±1.5	%
Pedestal - S/H1	—	±15	±35	—	±15	±35	—	±15	±35	mV
Sample Mode Offset Error - S/H2	—	±1	±10	—	±2	±10	—	±4	±10	mV
Gain Error - S/H2	—	±0.2	±1	—	±0.25	±1	—	±0.3	±1.5	%
Pedestal - S/H2	—	±15	±35	—	±15	±35	—	±15	±35	mV
Sample Mode Offset Error - CDS	—	±1	±10	—	±2	±10	—	±4	±10	mV
Differential Gain Error - CDS	—	±0.25	±1	—	±0.3	±1	—	±0.35	±1.5	%
Pedestal - CDS	—	±15	±35	—	±15	±35	—	±15	±35	mV
Pixel Rate (14-bit settling) ②	1.25	—	—	1.25	—	—	1.25	—	—	MHz
Input Bandwidth, ±5V										
Small Signal (–20dB input)	—	7	—	—	7	—	—	7	—	MHz
Large Signal (–0.5dB input)	—	5	—	—	5	—	—	5	—	MHz
Slew Rate	—	±80	—	—	±80	—	—	±80	—	V/µs
Aperture Delay Time	—	10	—	—	10	—	—	10	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time ②										
(to ±0.003%, 10V step)	—	340	400	—	350	400	—	350	400	ns
Hold Mode Settling Time										
(to ±0.15mV)	—	TBD	—	—	TBD	—	—	TBD	—	ns
Noise	—	200	—	—	200	—	—	200	—	µVrms
Feedthrough Rejection	—	72	—	—	72	—	—	72	—	dB
Overvoltage Recovery Time	—	400	—	—	400	—	—	400	—	ns
S/H Saturation Voltage	—	±12.5	—	—	±12.5	—	—	±12.5	—	Volts
Droop Rate	—	±0.004	±0.02	—	±0.4	±2	—	±0.8	±4	mV/µs
ANALOG OUTPUTS ③										
Output Voltage Range	±10	—	—	±10	—	—	±10	—	—	Volts
Output Impedance	—	0.5	—	—	0.5	—	—	0.5	—	Ohms
Output Current	—	—	±20	—	—	±20	—	—	±20	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+3.9	—	—	+3.9	—	—	+3.9	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA

① Pins 3 and 4. ② See Figure 4 for relationship between input voltage, accuracy, and acquisition time. ③ Pins 6 and 22.

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POWER REQUIREMENTS	+25°C			0 to +70°C			−55 to +125°C			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Power Supply Ranges										
+15V Supply	+14.75	+15.0	+15.25	+14.75	+15.0	+15.25	+14.75	+15.0	+15.25	Volts
−15V Supply	−14.75	−15.0	−15.25	−14.75	−15.0	−15.25	−14.75	−15.0	−15.25	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Currents										
+15V Supply	—	+23	+27	—	+23	+27	—	+23	+27	mA
−15V Supply	—	−23	−27	—	−23	−27	—	−23	−27	mA
+5V Supply	—	+1	+2	—	+1	+2	—	+1	+2	mA
Power Dissipation	—	700	850	—	700	850	—	700	850	mW
Power Supply Rejection	—	100	—	—	100	—	—	100	—	dB

GENERAL DESCRIPTION (continued)

at the output of the CDS-1401 every 800ns. This correlates with the fact that an acquisition time of 400ns is required for each internal S/H amplifier (10V step setting to ±0.003%). The input and output of the CDS-1401 can swing up to ±10 Volts.

The functionally complete CDS-1401 is packaged in a single, 24-pin, ceramic DDIP. It operates from ±15V and +5V supplies and consumes 700mW. Though the CDS-1401's approach to CDS appears straightforward (see Description of Operation), the circuit actually exploits an elegant architecture whose tradeoffs enable it to offer wide-bandwidth, low-noise and high-throughput combinations unachievable until now. The CDS-1401 is a generic type of circuit that can be used with almost any 10 to 14-bit A/D converter. However, DATEL does offer A/D converters that are optimized for use with the CDS-1401.

TECHNICAL NOTES

1. To achieve specified performance, all power supply pins should be bypassed with 2.2µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. All ANALOG GROUND (pins 5, 14, 21 and 23) and DIGITAL GROUND (pin 15) pins should be tied to a large analog ground plane beneath the package.
2. In the CDS configuration, to avoid saturation of the S/H amplifiers, the maximum analog inputs and conditions are as follows:
   ANALOG INPUT 1 < ±12V
   (ANALOG INPUT 1 − ANALOG INPUT 2) < ±12V
3. The combined video and reference/offset signal from the CCD array must be applied to S/H2, while the reference/offset signal is applied to S/H1.
4. To use as a CDS circuit, tie pin 8 (S/H2 SUMMING NODE) to either pin 6 (S/H1 OUT), through a 200 Ohm potentiometer, or directly to pin 7 (S/H1 ROUT). In both cases, the CCD's output is tied to pins 3 (ANALOG INPUT 1) and 4 (ANALOG INPUT 2). As shown in Figure 5, the 200Ω potentiometer is for gain matching.
5. To use as a dual S/H, leave pin 7 (S/H1 ROUT) and pin 8 (S/H2 SUMMING NODE) floating. Pin 6 (S/H1 OUT) will be the output of S/H1 and pin 22 (V OUT) will be the output of S/H2.
6. See Figure 4 for acquisition time versus accuracy and input voltage step amplitude.

FUNCTIONAL DESCRIPTION

Correlated Double Sampling

All photodetector elements (photodiodes, photomultiplier tubes, focal plane arrays, charge coupled devices, etc.) have unique output characteristics that call for specific analog-signal-processing (ASP) functions at their outputs. Charge coupled devices (CCD's), in particular, display a number of unique characteristics. Among them is the fact that the "offset error" associated with each individual pixel (i.e., the apparent photonic content of that pixel after having had no light incident upon it) changes each and every time that particular pixel is accessed.

Most of us think of an offset as a constant parameter that either can be compensated for (by performing an offset adjustment) or can be measured, recorded, and subtracted from subsequent readings to yield more accurate data. Contending with an offset that varies from reading to reading requires measuring and recording (or capturing and storing) the offset each and every time, so it can be subtracted from each subsequent data reading.

The "double sampling" aspect of CDS refers to the operation of sampling and storing/recording a given pixel's offset and then sampling the same pixel's output an instant later (with both the offset and the video signal present) and subsequently subtracting the two values to yield what is referred to as the "valid video" output for that pixel.

The "correlated" in CDS refers to the fact that the two samples must be taken close together in time because the offset is constantly varying. Reasons for this phenomena are discussed below.

At the output of all CCD's, transported pixel charge (electrons) is converted to a voltage by depositing the charge onto a capacitor (usually called the output or "floating" capacitor). The voltage that develops across this capacitor is obviously proportional to the amount of deposited charge (i.e., the number of electrons) according to $\Delta V = \Delta Q/C$. Once settled, the resulting capacitor voltage is buffered and brought to the CCD's output pin as a signal whose amplitude is proportional to the total number of photons incident upon the relevant pixel.

After the output signal has been recorded, the floating capacitor is discharged ("reset", "clamped", "dumped") and made ready to accept charge from the next pixel. This is when the problems begin. (This is a somewhat oversimplified

4

explanation in that the floating capacitor is not usually "discharged" but, in fact, "recharged" to some predetermined dc voltage, usually called the "reference level". The pixel offset appears as an output deviation from that reference level.)

The floating capacitor is normally discharged (charged) via a shunt switch (typically a FET structure) that has a non-zero "on" resistance. When the switch is on, its effective series resistance exhibits thermal noise (Johnson noise) due to the random motion of thermally energized charge. Because the shunt switch is in parallel with the floating capacitor, the instantaneous value of the thermal noise (expressed in either Volts or electrons) appears across the cap. When the shunt switch is opened, charge/voltage is left on the floating cap.

The magnitude of this "captured noise voltage" is a function of absolute temperature (T), the value of the floating capacitor (C) and Boltzman's constant (k). It is commonly referred to as "kTC" noise.

The second contributor to the constantly varying pixel offsets is the fact that, at high pixel rates, the floating capacitor never has time to fully discharge (charge) during the period in which its shunt switch is closed. There is always some "residual" charge left on the cap, and the amount of this charge varies as a function of what was the total charge held during the previous pixel. This amount of residual charge is, in fact, deterministic (if you know the previous charge and the number of time constants in the discharge period), however, it is less of a contributor than kTC noise.

The third major contributor to pixel offset is the fact that as the shunt FET is turned off, the voltage across (and the charge stored on) its parasitic junction capacitances changes. The result is an "injection" of excess charge onto the floating cap causing a voltage step normally called a "pedestal".

The fourth major contributor to pixel offset is a low-frequency noise component (usually called 1/f noise or pink noise) associated with the CCD's output buffer amplifier.

Due to all of these contributing factors, "pixel offsets" vary from sample to sample in an inconsistent, unpredictable manner.

Traditional Approach to CDS

There are a number of techniques for dealing with the varying-offset idiosyncrasy of CCD's. The most prevalent has been what can be called the "sample-sample-subtract" technique. This approach requires the use of two high-speed sample-hold (S/H) amplifiers and a difference amplifier. The first S/H is used to acquire and hold a given pixel's offset. Immediately after that, the second S/H acquires and holds the same pixel's offset+video signal. After both the S/H outputs have fully settled, the difference amplifier subtracts the offset from the offset+video yielding the valid video signal.

CDS-1401 Approach (See Figure 1)

The DATEL CDS-1401 takes a slightly different, though clearly superior, approach to CDS. It can be called the "sample-subtract-sample" approach.

Note that the CDS-1401 has been configured to offer the greatest amount of user flexibility. Its two S/H circuits function independently. They have separate input and output pins. Each has its own independent control lines. The control-line signals are delayed, buffered, and brought back out of the

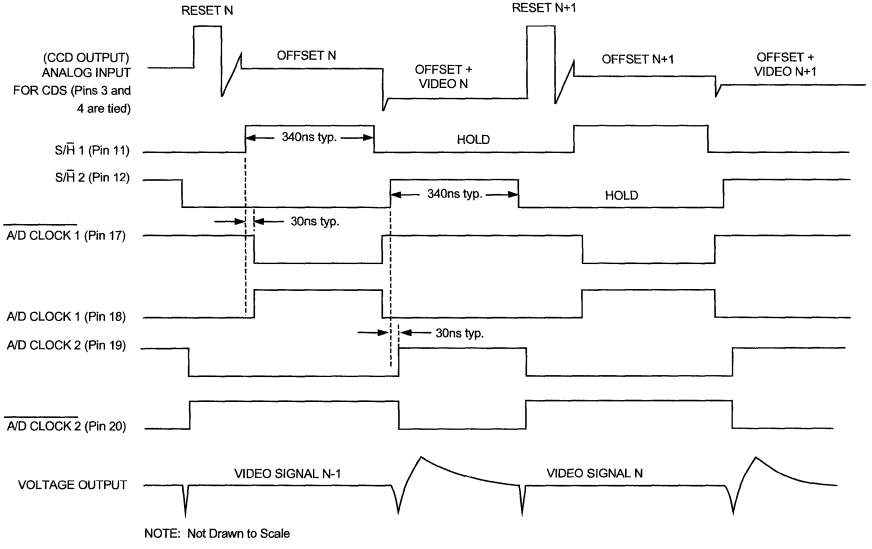

Figure 2. CDS-1401 Typical Timing Diagram

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package so they can be used to control other circuit functions. Each S/H has two pins for offset adjusting (if required), one for current and one for voltage.

In normal operation, the output signal of the CCD is applied simultaneously to the inputs (pins 3 and 4) of both S/H amplifiers. S/H1 will normally be used to capture and hold each pixel's offset signal. Therefore, S/H1 is initially in its signal-acquisition mode (logic "1" applied to pin 11, S/$\overline{H}$1 COMMAND). This is also called the sample or track mode. Following a brief interval during which the output of the CCD and the output of S/H1 are allowed to settle, S/H1 is driven into its hold mode by applying a logic "0" to pin 11. S/H1 is now holding the pixel's offset value.

In most straightforward configurations, the output of S/H1 is connected to the summing node of S/H2 by connecting pin 7 (S/H1 ROUT) to pin 8 (S/H2 SUMMING NODE).

When the offset+video signal appears at the output of the CCD, S/H2 is driven into its signal acquisition mode by applying a logic "1" to pin 12 (S/$\overline{H}$2 COMMAND). S/H2 employs a current-summing architecture that subtracts the output of S/H1 (the offset) from the output of the CCD (offset+video) while acquiring only the difference signal (i.e., the valid video). A logic "0" subsequently applied to pin 12 drives S/H2 into its hold mode, and after a brief transient settling time, the valid video signal appears at pin 22 (V OUT).

Timing Notes

See Figure 2, Typical Timing Diagram. It is advisable that neither of the CDS-1401's S/H amplifiers be in their sample/track mode when large, high-speed transients (normally associated with clock edges) are occurring throughout the system. This could result in the S/H amplifiers being driven into saturation, and they may not recover in time to accurately acquire their next signal.

For example, S/H1 should not be commanded into the sample mode until all transients associated with the opening of the shunt switch have begun to decay. Similarly, S/H2 should not be driven into the sample mode until all transients associated with the clocking of pixel charge onto the output capacitor have begun to decay. Therefore, it is generally not a good practice to use the same clock edge to drive S/H1 into hold (holding the offset) and S/H2 into sample (to acquire the offset + video signal).

S/H's that are in their signal-acquisition modes should be left there as long as possible (so all signals can settle) and be driven into their hold modes before any system transients occur. In Figure 2, S/H1 is driven into the sample mode shortly after the transient from the shunt switch has begun to decay. S/H1 is then kept in the sample mode while the offset signal and the S/H output settle. S/H1 is driven into hold just prior to the system clock pulse(s) that transfers the next pixel charge onto the output capacitor.

As soon as the transients/noise associated with the charge transport begins to decay, S/H2 can be driven into the sample mode. S/H2 can then be left in the sample mode until just before the reset pulse for the output capacitor.

In Figure 2, S/H's 1 and 2 both have the same acquisition time. If the pixel-to-pixel amplitude variation of offset signals is much

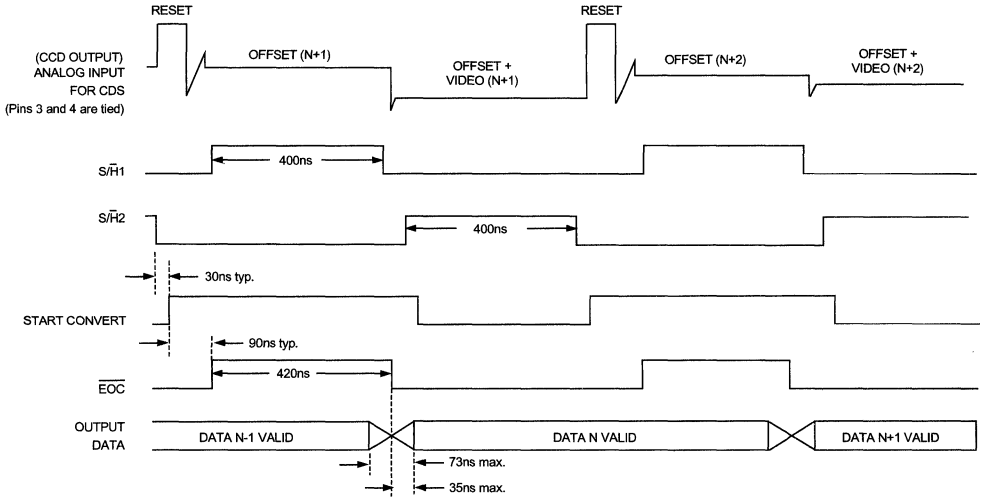

Figure 3. CDS-1401 in Front of ADS-CCD1201 at f_{CLK} = 1MHz

less than that of video signals, it may not be necessary for the allocated acquisition time of S/H1 to be as long as that of S/H2.

As shown in the plot (Figure 4) of acquisition times vs. input signal step size, the S/H's internal to the CDS-1401 acquire smaller-amplitude signals quicker than they acquire larger-amplitude signals. In "maximum-throughput" applications, assuming "asymmetric" timing can be accommodated, each S/H should only be given the time it requires, and no more, to acquire its input signal. Leaving a S/H amp in the sample mode for a longer period of time has little added benefit.

As an example, the graph shows that it takes 160ns to acquire a 500mV step to within 10mV of accuracy and 260ns to acquire a 500mV step to within 0.5mV of accuracy. The figures in this graph are typical values at room temperature.

The CDS-1401 brings out 4 control lines that can be used to trigger an A/D converter connected to its output. If the A/D is a sampling type, system timing should be such that the A/D's input S/H amplifier is acquiring the output of the CDS-1401 at the same time the output is settling to its final value.

For most sampling A/D's, the rising edge of the start-convert pulse drives the internal S/H into the hold mode under the assumption the S/H has already fully acquired and is tracking the input signal. In this case, the same edge can not be used to drive S/H2 into the hold mode and simultaneously initiate the A/D conversion. The output of S/H2 needs time to settle its sample-to-hold switching transient, and the input S/H of the A/D needs time to fully acquire its new input signal.

As shown in Figure 1, output line A/D CLOCK1 (pin 18) is a slightly delayed version of the signal applied to pin 11 (S/$\overline{H}$1 COMMAND), and $\overline{\text{A/D CLOCK1}}$ (pin 17) is its complement. A/D CLOCK2 (pin 19) is a delayed version of the signal applied to pin 12 (S/$\overline{H}$2 COMMAND), and $\overline{\text{A/D CLOCK2}}$ (pin 20) is its complement. Any one of these signals, as appropriate, may be used to trigger the A/D conversion.

Figure 3 is a typical timing diagram for a CDS-1401 in front of DATEL's 12-bit, 1.2MHz sampling A/D, the ADS-CCD1201.

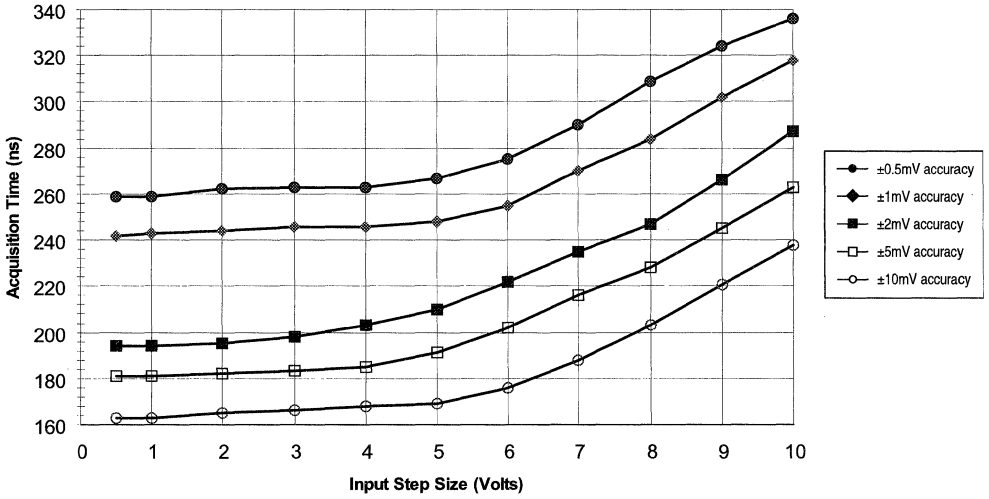

Figure 4. Acquisition Time versus Accuracy and Step Size

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CALIBRATION PROCEDURE

Offset Adjust (Figure 5)

Offset and pedestal errors may be compensated for by applying external voltages to pin 1 (OFFSET ADJUST V1) and/or pin 9 (OFFSET ADJUST V2) using either voltage-output DAC's or potentiometers configured to appear as voltage sources.

Offset and pedestal errors may also be compensated for by applying external currents to pin 2 (OFFSET ADJUST I1) and/or pin 10 (OFFSET ADJUST I2) by using either current-output DAC's or potentiometers configured to appear as current sources.

1. Connect pin 8 (S/H2 SUMMING NODE) either directly to pin 7 (S/H1 ROUT) or through a 200 Ohm potentiometer to pin 6 (S/H1 OUT).
2. Tie pins 3 (ANALOG INPUT 1) and 4 (ANALOG INPUT 2) to pin 5 (ANALOG GROUND).
3. Adjust OFFSET ADJUST V1 or OFFSET ADJUST I1 (while S/H1 is in the hold mode) until pin 6 (S/H1 OUT) equals 0V.
4. Adjust OFFSET ADJUST V2 or OFFSET ADJUST I2 (while S/H2 is in the hold mode) until pin 22 (VOUT) equals 0V.
5. To negate the effect of output droop on the offset-adjust process, each S/H must be continually switched between its sample and hold modes and adjusted so its output equals zero immediately after going into the hold mode.

The sensitivity of the voltage offset adjustments is 100mV per Volt. The sensitivity of the current offset adjustments is 1V per mA. Pins 1, 2, 9 and 10 should be left open (floating) when not being used for offset adjustment.

Gross Offset Adjustment

For gross offset adjustments use pin 2 (OFFSET ADJUST I1) and/or pin 10 (OFFSET ADJUST I2). All connections made to pin 2 and pin 10 should be very short because these are very sensitive points.

Sourcing 1mA into OFFSET ADJUST I1 will cause a –1V offset change at pin 6 (S/H1 OUT). It will also cause a +1V offset change at pin 22 (V OUT) if pin 7 (S/H1 ROUT) is connected to pin 8 (S/H2 SUMMING NODE).

Sourcing 1mA into OFFSET ADJUST I2 will cause a –1V offset change at pin 22 (V OUT).

Gain Matching Adjustment (Differential Gain) between S/H1 and S/H2

The user can adjust the gain matching (differential gain) between S/H1 and S/H2 by leaving pin 7 (S/H1 ROUT) floating (open) and connecting a 200 Ohm potentiometer between pin 6 (S/H1 OUT) and pin 8 (S/H2 SUMMING NODE). Note, offset adjustment should take place before gain matching adjustment.

Apply a full-scale input to both pins 3 (ANALOG INPUT 1) and 4 (ANALOG INPUT 2). Adjust the 200 Ohm potentiometer (with both S/H's in the sample mode) until pin 22 (V OUT) is 0V.

If gain matching adjustment is not required, leave pin 6 (S/H1 OUT) floating (open) and tie pin 7 (S/H1 ROUT) to pin 8 (S/H2 SUMMING NODE).

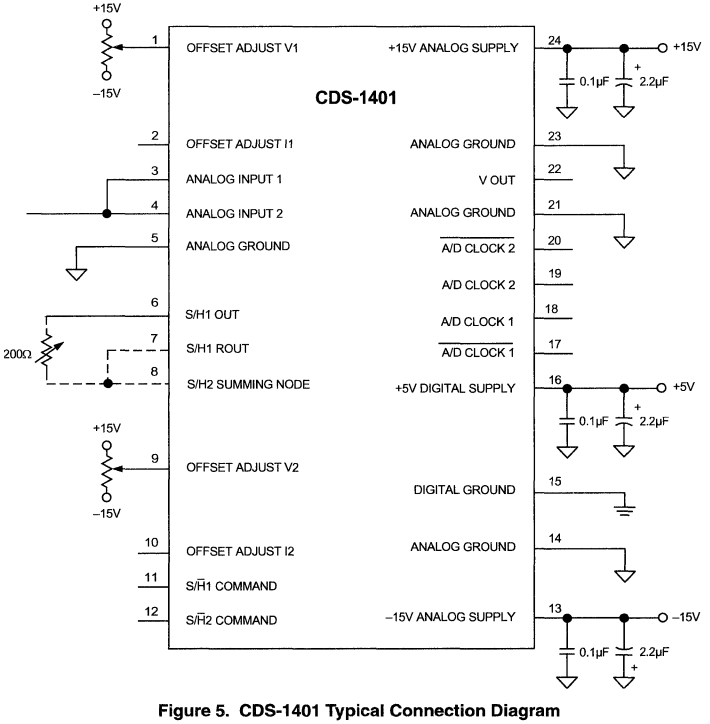
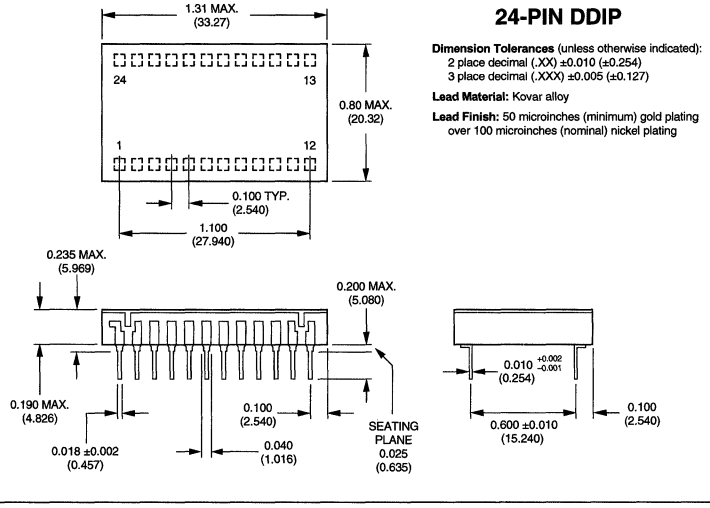


Figure 5. CDS-1401 Typical Connection Diagram

MECHANICAL DIMENSIONS INCHES (mm)

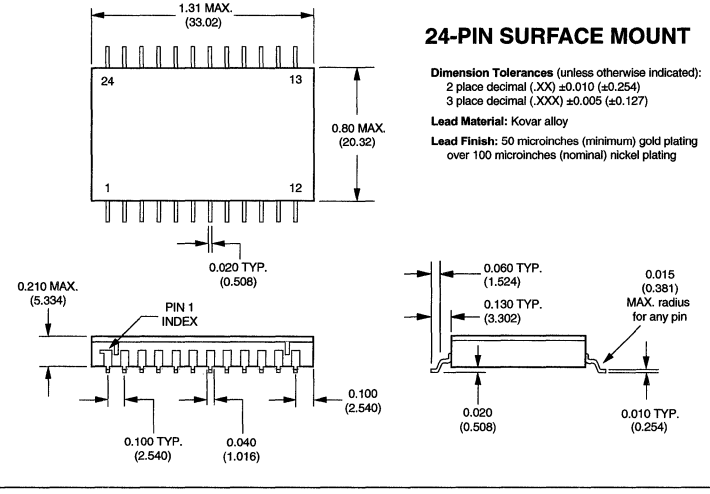


24-PIN DDIP

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating



24-PIN SURFACE MOUNT

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT	PACKAGE TYPE
CSD-1401MC	0 to +70°C	±10V	DDIP
CDS-1401MM	–55 to +125°C	±10V	DDIP

Accessories

HS-24 Heat Sink for CDS-1401 DDIP models

Receptacles for pc board mounting can be ordered through Amp Inc., part number 3-331272-8 (component lead socket), 24 required. For MIL-STD-883 products, or availability of surface mount packaging, contact DATEL.

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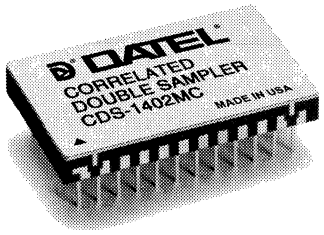
CDS-1402

14-Bit, Faster-Settling Correlated Double Sampling Circuit

PRELIMINARY PRODUCT DATA

FEATURES

- **Use with 10 to 14-bit A/D converters**
- **5 Megapixels/second minimum throughput (14 bits)**
- **±2.5V input/output ranges, Gain = –1**
- **Low noise, 200µVrms**
- **Two independent S/H amplifiers**
- **Gain matching between S/H's**
- **Offset adjustments for each S/H**
- **Four external A/D control lines**
- **Small package, 24-pin ceramic DDIP**
- **Low power, 350mW**
- **Low cost**



GENERAL DESCRIPTION

The CDS-1402 is an application-specific, correlated double sampling (CDS) circuit designed for electronic-imaging applications that employ CCD's (charge coupled devices) as their photodetector. The CDS-1402 has been optimized for use in digital video applications that employ 10 to 14-bit A/D converters. The low-noise CDS-1402 can accurately determine each pixel's true video signal level by sequentially sampling the pixel's offset signal and its video signal and subtracting the two. The result is that the consequences of residual charge, charge injection and low-frequency "kTC" noise on the CCD's output floating capacitor are effectively eliminated. The CDS-1402 can also be used as a dual sample-hold amplifier in a data acquisition system.

The CDS-1402 contains two sample-hold amplifiers and appropriate support/control circuitry. Features include independent offset-adjust capability for each S/H, adjustment for matching gain between the two S/H's, and four control lines for triggering the A/D converter used in conjunction with the CDS-1402. The CDS circuit's "ping-pong" timing approach (the offset signal of the "n+1" pixel can be acquired while the video output of the "nth" pixel is being converted) guarantees a minimum throughput, in a 14-bit application, of 5MHz. In other words, the true video signal (minus offset) will be available

(continued on page 4-13)

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OFFSET ADJUST V1	24	+5V ANALOG SUPPLY
2	DO NOT CONNECT	23	ANALOG GROUND
3	ANALOG INPUT 1	22	V OUT
4	ANALOG INPUT 2	21	ANALOG GROUND
5	ANALOG GROUND	20	$\overline{\text{A/D CLOCK2}}$
6	S/H1 OUT	19	A/D CLOCK2
7	S/H1 ROUT	18	A/D CLOCK1
8	S/H2 SUMMING NODE	17	$\overline{\text{A/D CLOCK1}}$
9	OFFSET ADJUST V2	16	+5V DIGITAL SUPPLY
10	DO NOT CONNECT	15	DIGITAL GROUND
11	$\text{S/}\overline{\text{H}}\text{1}$ COMMAND	14	ANALOG GROUND
12	$\text{S/}\overline{\text{H}}\text{2}$ COMMAND	13	–5V ANALOG SUPPLY

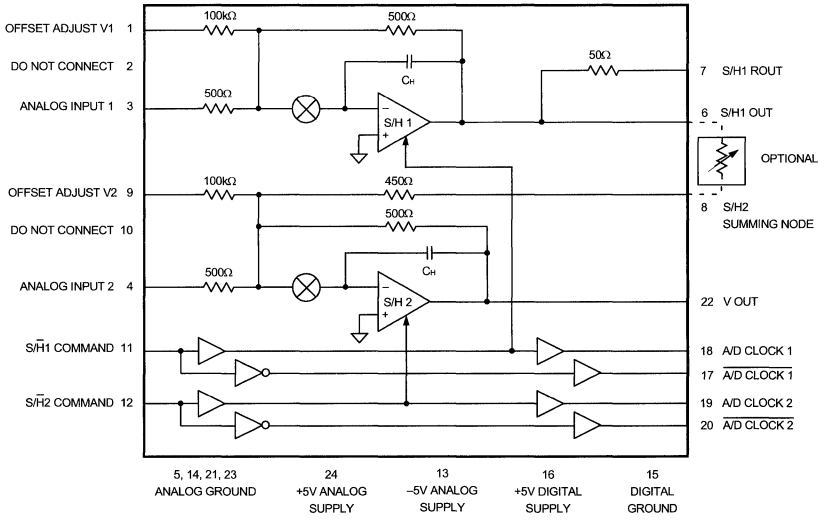


Figure 1. CDS-1402 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+5V Analog Supply (Pin 24)	0 to +6.3	Volts
–5V Analog Supply (Pin 13)	0 to –6.3	Volts
+5V Digital Supply (Pin 16)	0 to +6	Volts
Digital Inputs (Pins 11, 12)	–0.3 to +V_{DD} +0.3	Volts
Analog Inputs (Pins 3, 4)	±3.2	Volts
Lead Temperature (10 seconds)	300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
CDS-1402MC	0	—	+70	°C
CDS-1402MM	–55	—	+125	°C
Thermal Impedance				
θjc	—	5	—	°C/W
θca	—	22	—	°C/W
Storage Temperature Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP			
Weight	0.42 ounces(12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±V_{CC} = ±5V, +V_{DD} = +5V, pixel rate = 5MHz, and a minimum warmup time of two minutes unless otherwise noted.)

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG INPUTS ①	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range	±2.5	—	—	±2.5	—	—	±2.5	—	—	Volts
Input Resistance	—	500	—	—	500	—	—	500	—	Ohms
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+10	—	—	+10	—	—	+10	µA
Logic Loading "0"	—	—	–10	—	—	–10	—	—	–10	µA
PERFORMANCE										
Sample Mode Offset Error - S/H1	—	±3	—	—	±4	—	—	±5	—	mV
Gain Error - S/H1	—	±0.1	—	—	±0.2	—	—	±0.4	—	%
Pedestal - S/H1	—	±10	—	—	±10	—	—	±15	—	mV
Sample Mode Offset Error - S/H2	—	±3	—	—	±4	—	—	±5	—	mV
Gain Error - S/H2	—	±0.1	—	—	±0.2	—	—	±0.4	—	%
Pedestal - S/H2	—	±10	—	—	±10	—	—	±15	—	mV
Sample Mode Offset Error - CDS	—	±1	—	—	±4	—	—	±5	—	mV
Differential Gain Error - CDS	—	±0.1	—	—	±0.2	—	—	±0.4	—	%
Pedestal - CDS	—	±10	—	—	±10	—	—	±15	—	mV
Pixel Rate (14-bit settling) ②	5	—	—	5	—	—	5	—	—	MHz
Input Bandwidth, ±2.5V										
Small Signal (–20dB input)	—	TBD	—	—	TBD	—	—	TBD	—	MHz
Large Signal (–0.5dB input)	—	TBD	—	—	TBD	—	—	TBD	—	MHz
Slew Rate	—	±500	—	—	±500	—	—	±500	—	V/µs
Aperture Delay Time	—	10	—	—	10	—	—	10	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time ①										
(to ±0.01%, 5V step)	—	100	—	—	100	—	—	100	—	ns
Hold Mode Settling Time										
(to ±0.15mV)	—	TBD	—	—	TBD	—	—	TBD	—	ns
Noise	—	200	—	—	200	—	—	200	—	µVrms
Feedthrough Rejection	—	TBD	—	—	TBD	—	—	TBD	—	dB
Overvoltage Recovery Time	—	200	—	—	200	—	—	200	—	ns
S/H Saturation Voltage	—	±3.2	—	—	±3.2	—	—	±3.2	—	V
Droop Rate	—	±5	—	—	±10	—	—	±25	—	mV/µs
ANALOG OUTPUTS ③										
Output Voltage Range	±2.5	—	—	±2.5	—	—	±2.5	—	—	Volts
Output Impedance	—	0.5	—	—	0.5	—	—	0.5	—	Ohms
Output Current	—	—	±20	—	—	±20	—	—	±20	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+3.9	—	—	+3.9	—	—	+3.9	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA

① Pins 3 and 4. ② See Figure 5 for relationship between input voltage, accuracy, and acquisition time. ③ Pins 6 and 22.

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POWER REQUIREMENTS	+25°C			0 to +70°C			−55 to +125°C			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Power Supply Ranges										
+5V Analog Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
−5V Analog Supply	−4.75	−5.0	−5.25	−4.75	−5.0	−5.25	−4.75	−5.0	−5.25	Volts
+5V Digital Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Currents										
+5V Analog Supply	—	+35	+45	—	+35	+45	—	+35	+45	mA
−5V Analog Supply	—	−35	−45	—	−35	−45	—	−35	−45	mA
+5V Digital Supply	—	+2	+5	—	+2	+5	—	+2	+5	mA
Power Dissipation	—	350	450	—	350	450	—	350	450	mW
Power Supply Rejection	—	60	—	—	60	—	—	60	—	dB

GENERAL DESCRIPTION (continued)

at the output of the CDS-1402 every 200ns. This correlates with the fact that an acquisition time of 100ns is required for each internal S/H amplifier (5V step acquired to ±0.003% accuracy). The input and output of the CDS-1402 can swing up to ±2.5 Volts.

The functionally complete CDS-1402 is packaged in a single, 24-pin, ceramic DDIP. It operates from ±5V analog and +5V digital supplies and consumes 350mW. Though the CDS-1402's approach to CDS appears straightforward (see Description of Operation), the circuit actually exploits an elegant architecture whose tradeoffs enable it to offer wide-bandwidth, low-noise and high-throughput combinations unachievable until now. The CDS-1402, a generic type of circuit, can be used with most 10 to 14-bit A/D converters. However, DATEL offers A/D converters optimized for use with CDS-1402.

TECHNICAL NOTES

1. To achieve specified performance, all popwer supply pins should be bypassed with 2.2µF tantalum capacitors in parallel with 0.01µF ceramic capacitors. All ANALOG GROUND (pins 5, 14, 21 and 23) and DIGITAL GROUND (pin 15) pins should be tied to a large analog ground plane beneath the package.
2. In the CDS configuration, to avoid saturation of the S/H amplifiers, the maximum analog inputs and conditions are as follows:
   ANALOG INPUT 1 < ±3.2V
   (ANALOG INPUT 1 − ANALOG INPUT 2) < ±3.2V
3. The combined video and reference/offset signal from the CCD array must be applied to S/H2, while the reference/offset signal is applied to S/H1.
4. To use as a CDS circuit, tie pin 8 (S/H2 SUMMING NODE) to either pin 6 (S/H1 OUT), through a 100 Ohm potentiometer, or directly to pin 7 (S/H1 ROUT). In both cases, the CCD's output is tied to pins 3 (ANALOG INPUT 1) and 4 (ANALOG INPUT 2). As shown in Figure 5, the 100Ω potentiometer is for gain matching.
5. To use as a dual S/H, leave pin 7 (S/H1 ROUT) and pin 8 (S/H2 SUMMING NODE) floating. Pin 6 (S/H1 OUT) will be the output of S/H1 and pin 22 (V OUT) will be the output of S/H2.
6. See Figure 4 for acquisition time versus accuracy and input voltage step amplitude.

FUNCTIONAL DESCRIPTION

Correlated Double Sampling

All photodetector elements (photodiodes, photomultiplier tubes, focal plane arrays, charge coupled devices, etc.) have unique output characteristics that call for specific analog-signal-processing (ASP) functions at their outputs. Charge coupled devices (CCD's), in particular, display a number of unique characteristics. Among them is the fact that the "offset error" associated with each individual pixel (i.e., the apparent photonic content of that pixel after having had no light incident upon it) changes each and every time that particular pixel is accessed.

Most of us think of an offset as a constant parameter that either can be compensated for (by performing an offset adjustment) or can be measured, recorded, and subtracted from subsequent readings to yield more accurate data. Contending with an offset that varies from reading to reading requires measuring and recording (or capturing and storing) the offset each and every time, so it can be subtracted from each subsequent data reading.

The "double sampling" aspect of CDS refers to the operation of sampling and storing/recording a given pixel's offset and then sampling the same pixel's output an instant later (with both the offset and the video signal present) and subsequently subtracting the two values to yield what is referred to as the "valid video" output for that pixel.

The "correlated" in CDS refers to the fact that the two samples must be taken close together in time because the offset is constantly varying. Reasons for this phenomena are discussed below.

At the output of all CCD's, transported pixel charge (electrons) is converted to a voltage by depositing the charge onto a capacitor (usually called the output or "floating" capacitor). The voltage that develops across this capacitor is obviously proportional to the amount of deposited charge (i.e., the number of electrons) according to $\Delta V = \Delta Q/C$. Once settled, the resulting capacitor voltage is buffered and brought to the CCD's output pin as a signal whose amplitude is proportional to the total number of photons incident upon the relevant pixel.

After the output signal has been recorded, the floating capacitor is discharged ("reset", "clamped", "dumped") and made ready to accept charge from the next pixel. This is when the problems begin. (This is a somewhat oversimplified

explanation in that the floating capacitor is not usually "discharged" but, in fact, "recharged" to some predetermined dc voltage, usually called the "reference level". The pixel offset appears as an output deviation from that reference level.)

The floating capacitor is normally discharged (charged) via a shunt switch (typically a FET structure) that has a non-zero "on" resistance. When the switch is on, its effective series resistance exhibits thermal noise (Johnson noise) due to the random motion of thermally energized charge. Because the shunt switch is in parallel with the floating capacitor, the instantaneous value of the thermal noise (expressed in either Volts or electrons) appears across the cap. When the shunt switch is opened, charge/voltage is left on the floating cap.

The magnitude of this "captured noise voltage" is a function of absolute temperature (T), the value of the floating capacitor (C) and Boltzman's constant (k). It is commonly referred to as "kTC" noise.

The second contributor to the constantly varying pixel offsets is the fact that, at high pixel rates, the floating capacitor never has time to fully discharge (charge) during the period in which its shunt switch is closed. There is always some "residual" charge left on the cap, and the amount of this charge varies as a function of what was the total charge held during the previous pixel. This amount of residual charge is, in fact, deterministic (if you know the previous charge and the number of time constants in the discharge period), however, it is less of a contributor than kTC noise.

The third major contributor to pixel offset is the fact that as the shunt FET is turned off, the voltage across (and the charge stored on) its parasitic junction capacitances changes. The result is an "injection" of excess charge onto the floating cap causing a voltage step normally called a "pedestal".

The fourth major contributor to pixel offset is a low-frequency noise component (usually called 1/f noise or pink noise) associated with the CCD's output buffer amplifier.

Due to all of these contributing factors, "pixel offsets" vary from sample to sample in an inconsistent, unpredictable manner.

Traditional Approach to CDS

There are a number of techniques for dealing with the varying-offset idiosyncrasy of CCD's. The most prevalent has been what can be called the "sample-sample-subtract" technique. This approach requires the use of two high-speed sample-hold (S/H) amplifiers and a difference amplifier. The first S/H is used to acquire and hold a given pixel's offset. Immediately after that, the second S/H acquires and holds the same pixel's offset+video signal. After both the S/H outputs have fully settled, the difference amplifier subtracts the offset from the offset+video yielding the valid video signal.

CDS-1402 Approach (See Figure 1)

The DATEL CDS-1402 takes a slightly different, though clearly superior, approach to CDS. It can be called the "sample-subtract-sample" approach.

Note that the CDS-1402 has been configured to offer the greatest amount of user flexibility. Its two S/H circuits function independently. They have separate input and output pins. Each has its own independent control lines. The control-line

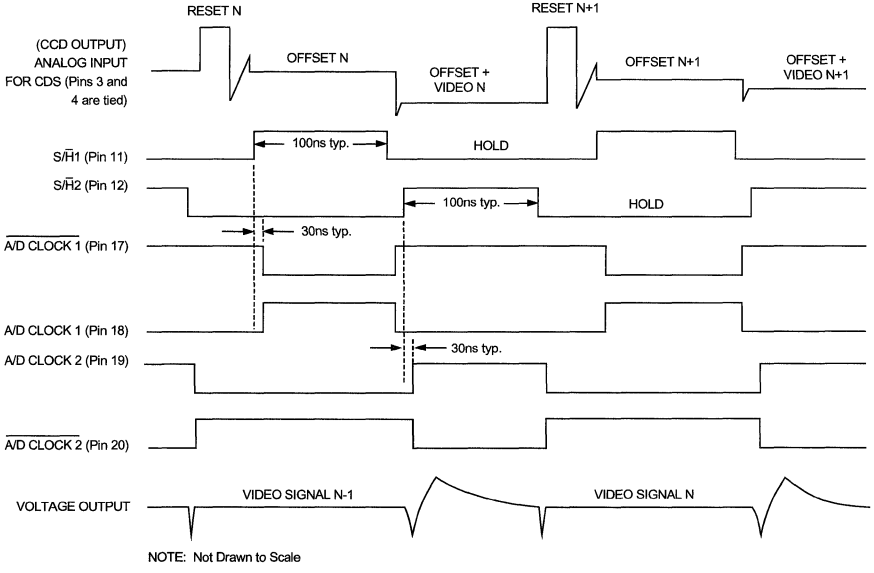

Figure 2. CDS-1402 Typical Timing Diagram

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signals are delayed, buffered, and brought back out of the package so they can be used to control other circuit functions. Each S/H has two pins for offset adjusting (if required), one for current and one for voltage.

In normal operation, the output signal of the CCD is applied simultaneously to the inputs (pins 3 and 4) of both S/H amplifiers. S/H1 will normally be used to capture and hold each pixel's offset signal. Therefore, S/H1 is initially in its signal-acquisition mode (logic "1" applied to pin 11, S/$\overline{H1}$ COMMAND). This is also called the sample or track mode. Following a brief interval during which the output of the CCD and the output of S/H1 are allowed to settle, S/H1 is driven into its hold mode by applying a logic "0" to pin 11. S/H1 is now holding the pixel's offset value.

In most straightforward configurations, the output of S/H1 is connected to the summing node of S/H2 by connecting pin 7 (S/H1 ROUT) to pin 8 (S/H2 SUMMING NODE).

When the offset+video signal appears at the output of the CCD, S/H2 is driven into its signal acquisition mode by applying a logic "1" to pin 12 (S/$\overline{H2}$ COMMAND). S/H2 employs a current-summing architecture that subtracts the output of S/H1 (the offset) from the output of the CCD (offset+video) while acquiring only the difference signal (i.e., the valid video). A logic "0" subsequently applied to pin 12 drives S/H2 into its hold mode, and after a brief transient settling time, the valid video signal appears at pin 22 (V OUT).

Timing Notes

See Figure 2, Typical Timing Diagram. It is advisable that neither of the CDS-1402's S/H amplifiers be in their sample/track mode when large, high-speed transients (normally associated with clock edges) are occurring throughout the system. This could result in the S/H amplifiers being driven into saturation, and they may not recover in time to accurately acquire their next signal.

For example, S/H1 should not be commanded into the sample mode until all transients associated with the opening of the shunt switch have begun to decay. Similarly, S/H2 should not be driven into the sample mode until all transients associated with the clocking of pixel charge onto the output capacitor have begun to decay. Therefore, it is generally not a good practice to use the same clock edge to drive S/H1 into hold (holding the offset) and S/H2 into sample (to acquire the offset + video signal).

S/H's that are in their signal-acquisition modes should be left there as long as possible (so all signals can settle) and be driven into their hold modes before any system transients occur. In Figure 2, S/H1 is driven into the sample mode shortly after the transient from the shunt switch has begun to decay. S/H1 is then kept in the sample mode while the offset signal and the S/H output settle. S/H1 is driven into hold just prior to the system clock pulse(s) that transfers the next pixel charge onto the output capacitor.

As soon as the transients/noise associated with the charge transport begins to decay, S/H2 can be driven into the sample mode. S/H2 can then be left in the sample mode until just before the reset pulse for the output capacitor.

In Figure 2, S/H's 1 and 2 both have the same acquisition time. If the pixel-to-pixel amplitude variation of offset signals is much less than that of video signals, it may not be necessary for the allocated acquisition time of S/H1 to be as long as that of S/H2.

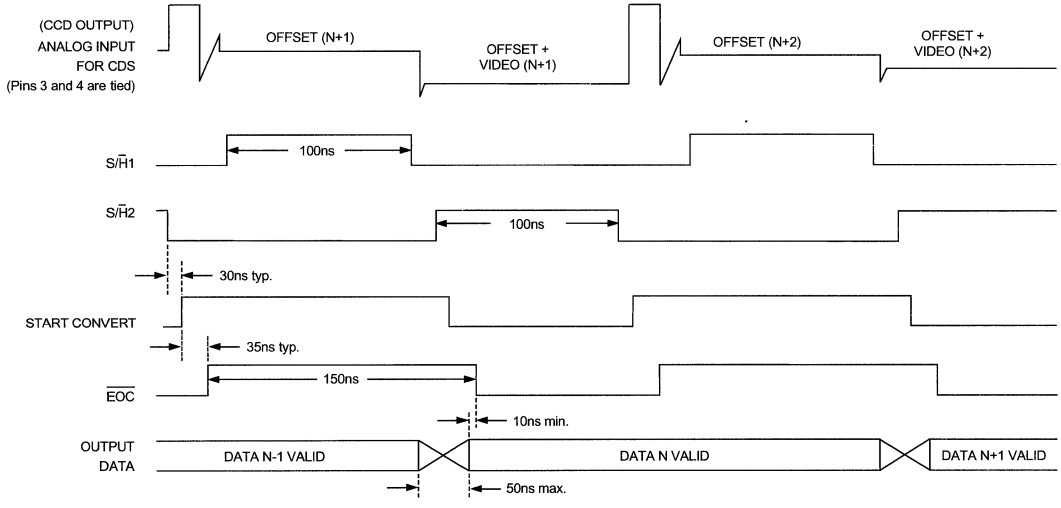

Figure 3. CDS-1402 in Front of DATEL's ADC-944 at f_{CLK} = 4MHz

As shown in the plot (Figure 4) of acquisition times vs. input signal step size, the S/H's internal to the CDS-1402 acquire smaller-amplitude signals quicker than they acquire larger-amplitude signals. In "maximum-throughput" applications, assuming "asymmetric" timing can be accommodated, each S/H should only be given the time it requires, and no more, to acquire its input signal. Leaving a S/H amp in the sample mode for a longer period of time has little added benefit.

As an example, the graph shows that it takes 32ns to acquire a 500mV step to within 10mV of accuracy and 73ns to acquire a 500mV step to within 0.5mV of accuracy. The figures in this graph are typical values at room temperature.

The CDS-1402 brings out 4 control lines that can be used to trigger an A/D converter connected to its output. If the A/D is a sampling type, system timing should be such that the A/D's input S/H amplifier is acquiring the output of the CDS-1402 at the same time the output is settling to its final value.

For most sampling A/D's, the rising edge of the start-convert pulse drives the internal S/H into the hold mode under the assumption the S/H has already fully acquired and is tracking the input signal. In this case, the same edge can not be used to drive S/H2 into the hold mode and simultaneously initiate the A/D conversion. The output of S/H2 needs time to settle its sample-to-hold switching transient, and the input S/H of the A/D needs time to fully acquire its new input signal.

As shown in Figure 1, output line A/D CLOCK1 (pin 18) is a slightly delayed version of the signal applied to pin 11 (S/$\overline{H1}$ COMMAND), and $\overline{\text{A/D CLOCK1}}$ (pin 17) is its complement. A/D CLOCK2 (pin 19) is a delayed version of the signal applied to pin 12 (S/H2 COMMAND), and $\overline{\text{A/D CLOCK2}}$ (pin 20) is its complement. Any one of these signals, as appropriate, may be used to trigger the A/D conversion.

Figure 3 is a typical timing diagram for a CDS-1402 in front of DATEL's 14-bit, 5MHz sampling A/D, the ADS-944.

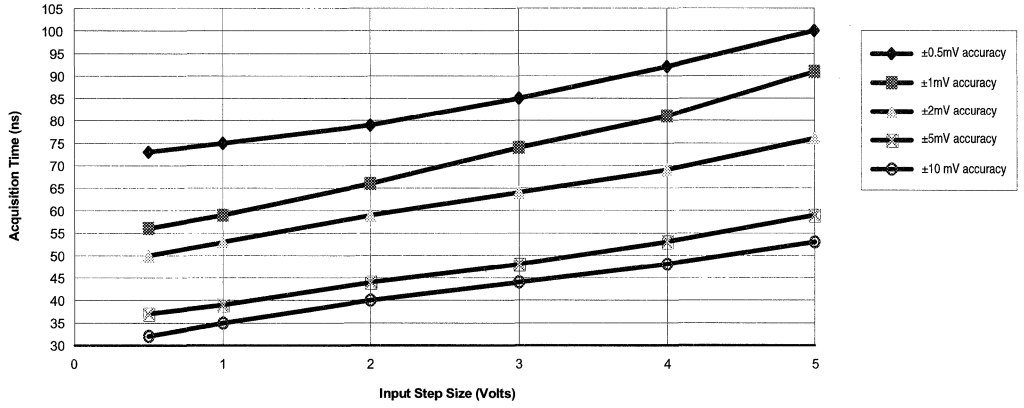

Figure 4. Acquisition Time versus Accuracy and Step Size

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CALIBRATION PROCEDURE

Offset Adjust (Figure 5)
Offset and pedestal errors may be compensated for by applying external voltages to pin 1 (OFFSET ADJUST V1) and/or pin 9 (OFFSET ADJUST V2) using either voltage-output DAC's or potentiometers configured to appear as voltage sources.

1. Connect pin 8 (S/H2 SUMMING NODE) either directly to pin 7 (S/H1 ROUT) or through a 100 Ohm potentiometer to pin 6 (S/H1 OUT).

2. Tie pins 3 (ANALOG INPUT 1) and 4 (ANALOG INPUT 2) to pin 5 (ANALOG GROUND).

3. Adjust OFFSET ADJUST V1 (while S/H1 is in the hold mode) until pin 6 (S/H1 OUT) equals 0V.

4. Adjust OFFSET ADJUST V2 (while S/H2 is in the hold mode) until pin 22 (V OUT) equals 0V.

5. To negate the effect of output droop on the offset-adjust process, each S/H must be continually switched between its sample and hold modes and adjusted so its output equals zero immediately after going into the hold mode.

The sensitivity of the voltage offset adjustments is 5mV per Volt. Pins 1 and 9 should be left open (floating) when not being used for offset adjustment.

Gain Matching Adjustment (Differential Gain) between S/H1 and S/H2
The user can adjust the gain matching (differential gain) between S/H1 and S/H2 by leaving pin 7 (S/H1 ROUT) floating (open) and connecting a 100 Ohm potentiometer between pin 6 (S/H1 OUT) and pin 8 (S/H2 SUMMING NODE). Note, offset adjustment should take place before gain matching adjustment.

Apply a full-scale input to both pin 3 (ANALOG INPUT 1) and pin 4 (ANALOG INPUT 2). Adjust the 100 Ohm potentiometer (with both S/H's in the sample mode) until pin 22 (V OUT) is 0V.

If gain matching adjustment is not required, leave pin 6 (S/H1 OUT) floating (open) and tie pin 7 (S/H1 ROUT) to pin 8 (S/H2 SUMMING NODE).

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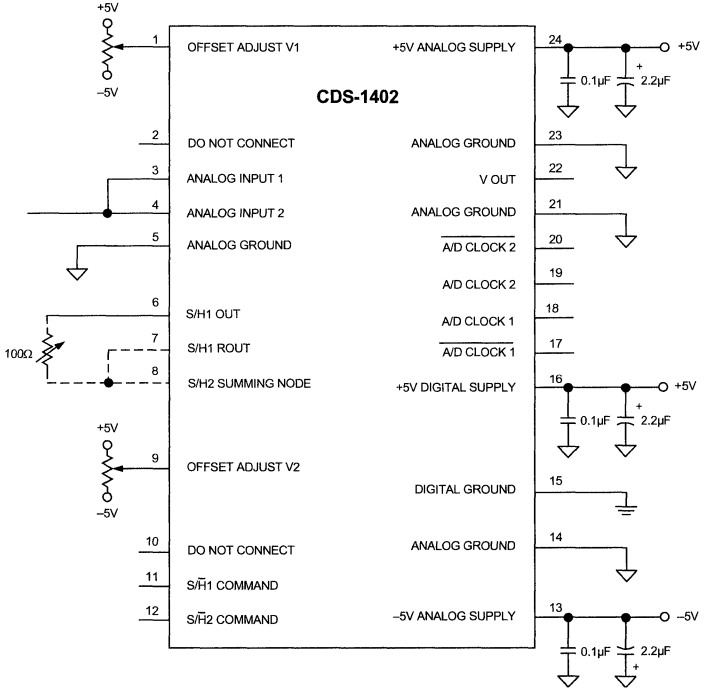
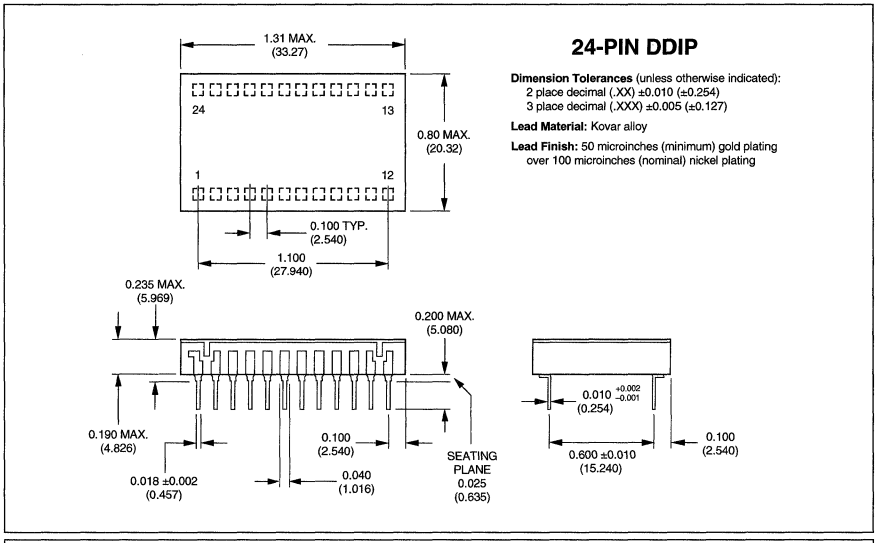


Figure 5. CDS-1402 Typical Connection Diagram

MECHANICAL DIMENSIONS INCHES (mm)

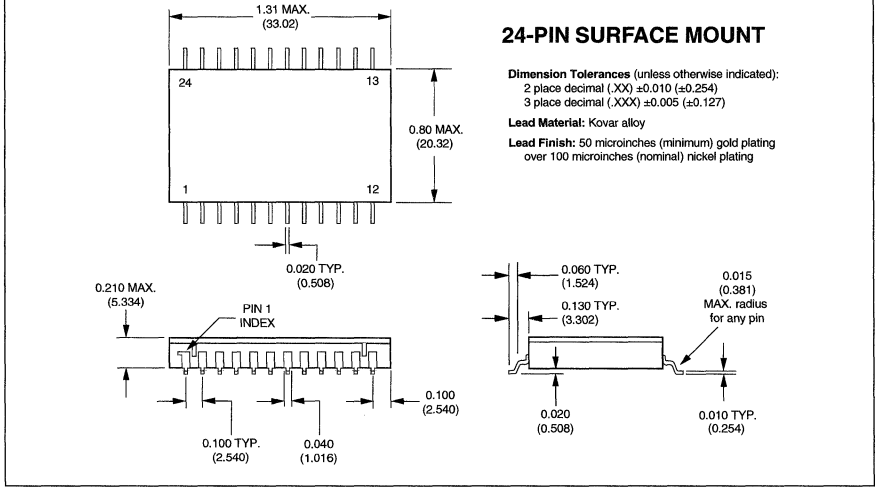


24-PIN DDIP

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating



24-PIN SURFACE MOUNT

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT	PACKAGE TYPE
CSD-1402MC	0 to +70°C	±2.5V	DDIP
CDS-1402MM	–55 to +125°C	±2.5V	DDIP

Accessories

HS-24	Heat Sink for CDS-1402 DDIP models

Receptacles for pc board mounting can be ordered through Amp Inc., part number 3-331272-8 (component lead socket), 24 required. For MIL-STD-883 products, or availability of surface mount packaging, contact DATEL.

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Analog Multiplexers

Table of Contents

Selection Guide

Model	Channels	Settling Time to ±0.01% (µsec)	Access Time (nsec)	Input Range (Volts)	On Resistance (Ohms)	Input Leakage		Power Supplies (Volts)	Maximum Power Dissipation (mW)	Page
						Off Channel (pA)	On Channel (pA)			
MX-850	4SE	0.04 ①	20	±10	90	20	400	+5, ±15	270	**5-21**
MX-826 ③	8SE	0.150 ②	20	±10	2500	—	—	+5, ±15	575	**5-18**
MX-818C	8SE/4D	0.8	130	±15	750	10	15	±15	540	**5-13**
MX-1616C	16SE/8D	0.8	130	±15	750	10	40	±15	900	**5-13**
MV-1606	16SE	2.4	300	±15	270	30	1000	±15	60	**5-3**
MVD-807	8D	2.4	300	±15	270	30	1000	±15	60	**5-3**
MV-808	8SE	2.8	350	±15	250	20	100	+5, ±15	28	**5-3**
MVD-409	4D	2.8	350	±15	250	20	50	+5, ±15	28	**5-3**
MX-1606	16SE	3.5	500	±15	1500	30	100	±15	45	**5-8**
MX-808	8SE	3.5	500	±15	1500	30	100	±15	45	**5-8**
MXD-409	4D	3.5	500	±15	1500	30	100	±15	45	**5-8**
MXD-807	8D	3.5	500	±15	1500	30	100	±15	45	**5-8**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① 80ns to ±0.001%.
② 300ns to ±0.003%.
③ MIL-STD-883 models available.

For literature or technical assistance

800-233-2765

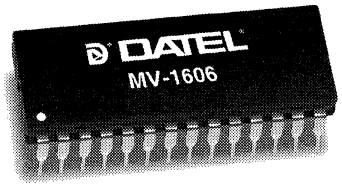
or contact your local DATEL Sales Office or Representative

DATEL®
INNOVATION and EXCELLENCE

MV/MVD Series
Low ON Resistance CMOS, Analog Multiplexers

FEATURES

- ±0.01% accuracy
- Low "ON" resistance
- Break-before-make switching
- Dielectrically isolated CMOS technology
- Single-ended or differential inputs
- Fast settling times
- DTL/TTL/CMOS compatible
- 350kHz sampling rates



GENERAL DESCRIPTION

The MV and MVD Series analog multiplexers are 4, 8 and 16-channel monolithic devices featuring a low ON resistance of 270 Ohms. These units are manufactured with CMOS technology using the dielectric isolation process. There are 8 and 16-channel single-ended models and 4 and 8-channel differential models in this Series. Channel addressing is done with a 2, 3 or 4-bit binary code. An inhibit input enables or disables the entire device to permit expansion of the numbers of channels by using several devices together. Another important feature is break-before-make switching, which ensures that no two channels are ever momentarily shorted together.

With a high impedance load, transfer accuracies of ±0.01% can be achieved at channel sampling rates up to 350kHz. These multiplexers are ideal for multichannel data acquisition systems where the multiplexer operates into a high-impedance load such as a sample-hold, buffer amplifier, or instrumentation amplifier.

These multiplexers are packaged in 16 and 28-pin ceramic DIP's. Standard versions operate over 0 to +70°C while the MVD-409M and the MV-1606M operate from –55 to +125°C. The MV and MVD Series are similar in specifications to DATEL's MX and MXD Series multiplexers. The MX and MXD Series are recommended where input over-voltage protection to 20 Volts above supply voltage is required and where higher channel ON resistance can be tolerated.

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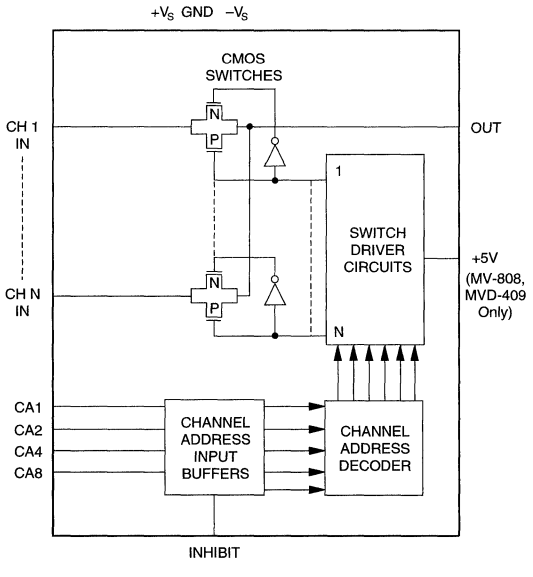

Figure 1. MV Series Functional Block Diagram

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION MV-808	FUNCTION MVD-409	PIN	FUNCTION MV-808	FUNCTION MVD-409
1	CA2	CA2	16	CA1	CA1
2	+5V	+5V	15	–VS	–VS
3	INHIBIT	INHIBIT	14	+VS	+VS
4	CA4	B OUT	13	1 IN	1A IN
5	8 IN	4B IN	12	OUT	A OUT
6	7 IN	3B IN	11	2 IN	2A IN
7	6 IN	2B IN	10	3 IN	3A IN
8	5 IN	1B IN	9	4 IN	4A IN

PIN	FUNCTION MV-1606	FUNCTION MVD-807	PIN	FUNCTION MV-1606	FUNCTION MVD-807
1	+VS	+VS	28	OUT	A OUT
2	N.C.	B OUT	27	–VS	–VS
3	N.C.	N.C.	26	8 IN	8A IN
4	16 IN	8B IN	25	7 IN	7A IN
5	15 IN	7B IN	24	6 IN	6A IN
6	14 IN	6B IN	23	5 IN	5A IN
7	13 IN	5B IN	22	4 IN	4A IN
8	12 IN	4B IN	21	3 IN	3A IN
9	11 IN	3B IN	20	2 IN	2A IN
10	10 IN	2B IN	19	1 IN	1A IN
11	9 IN	1B IN	18	INHIBIT	INHIBIT
12	GND	GND	17	CA1	CA1
13	N.C.	N.C.	16	CA2	CA2
14	CA8	N.C.	15	CA4	CA4

NOTES: CA = Channel address V_S = Supply voltage N.C. = No connection

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MV-808	MV-1606 MV-1606M	MVD-409 MVD-409M	MVD-807
Power Supply				
Analog	±20V	±20V	±20V	±20V
Digital	+30V	—	+30V	—
Input Voltage				
Analog	$\pm IV_S + 2VI$	$\pm IV_S + 2VI$	$\pm IV_S + 2VI$	$\pm IV_S + 2VI$
Digital	$\pm V_S$	$\pm IV_S + 4VI$	$\pm V_S$	$\pm IV_S + 4VI$
Power Dissipation	780mW	1200mW	780mW	1200mW

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V supplies (and +5V supply for MV-808 and MVD-409), unless otherwise noted.)

ANALOG INPUTS	MV-808	MV-1606 MV-1606M	MVD-409 MVD-409M	MVD-807
Number of Channels	8	16	4	8
Type	Single-ended	Single-ended	Differential	Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON				
Resistance ①	250Ω	270Ω	250Ω	270Ω
Resistance Over Temperature (maximum) ②	500Ω	500Ω	500Ω	500Ω
Leakage	100pA	1nA	50pA	1nA
Channel OFF				
Input Leakage	20pA	30pA	20pA	30pA
Output Leakage	100pA	1nA	50pA	1nA
Input Capacitance	4pF	10pF	4pF	10pF
Output Capacitance	20pF	52pF	10pF	30pF
DIGITAL INPUTS ③				
Logic "0" Threshold (maximum)	+0.4V	+0.8V	+0.4V	+0.8V
Logic "1" Threshold (minimum) ④	+4.0V	+2.4V	+4.0V	+2.4V
Input Current (maximum, high or low)	1µA	1µA	1µA	1µA
Channel Address Coding	3 bits	4 bits	2 bits	3 bits
Channel Inhibit (all channels OFF)	Logic "1"	Logic "0"	Logic "1"	Logic "0"
PERFORMANCE				
Transfer Error (maximum)	±0.01%	±0.01%	±0.01%	±0.01%
Crosstalk (10kHz)	–86dB	–86dB	–86dB	–86dB
Common Mode Rejection	—	—	120dB	120dB
Settling Time (20V to ±0.1%)	1.1µs	1.2µs	1.1µs	1.2µs
Settling Time (20V to ±0.01%)	2.8µs ⑤	2.4µs	2.8µs ⑤	2.4µs
Turn ON Time	350ns	300ns	350ns	300ns
Turn OFF Time	250ns	220ns	250ns	220ns
Inhibit/Enable Delay	300ns	300ns	300ns	300ns
Break-Before-Make Delay	100ns	80ns	100ns	80ns
POWER REQUIREMENTS				
Power Supply Voltage	±15V	±15V	±15V	±15V
Power Supply Current (maximum)	+0.5, –1mA	+3, –1mA	+0.5, –1mA	+3, –1mA
Digital Supply Voltage	+5V	—	+5V	—
Digital Supply Current (maximum)	+1mA	—	+1mA	—
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range	0 to +70°C	0 to +70°C	0 to +70°C	0 to +70°C
MV-1606M and MVD-409M Operating Temperature Range	—	–55 to +125°C	–55 to +125°C	—
Storage Temperature Range	–65 to +150°C	–65 to +150°C	–65 to +150°C	–65 to +150°C
Package	16-pin DIP	28-pin DIP	16-pin DIP	28-pin DIP

Footnotes:

① For MV-1606M, typical value is 170 Ohms.

② For MV-1606M, maximum value is 400 Ohms.

③ Channel address and inhibit inputs.

④ For MV-808 and MVD-409: to drive from DTL/TTL logic, 1k pull-up resistors to +5V should be used.

⑤ Settling to ±0.025%.

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TECHNICAL NOTES

1. The transfer accuracy of the MV Series multiplexers depends on both the source resistance and load resistance. For example, with zero source resistance and assuming 500 Ohms maximum channel ON resistance, the load impedance must be at least 5 megohms to achieve 0.01% accuracy. In practice, it is recommended that a load impedance of 10^8 Ohms or more be used. This is a typical input impedance value for most IC operational amplifiers connected in the follower mode or for IC sample-holds (see DATEL's SHM-1C-1, SHM-LM-2, or SHM-20). Source resistance should be kept as low as possible so that accuracy or settling time are not degraded. Less than 250 Ohms is recommended.
2. For differential operation, either two unity-gain buffers or an instrumentation amplifier (such as DATEL's AM-551) is recommended as the output load. To maintain high CMR, source impedance unbalance must be kept to a minimum, and amplifiers with high CMR should be used.
3. The maximum analog input overvoltage for the MV series is $\pm|V_S + 2V|$. It should be noted that the logic (channel address) inputs are protected with resistors and clamp diodes but the analog inputs are not. Because the analog inputs are not protected, the low ON resistance is achieved.
4. Channel expansion is accomplished by use of the inhibit input of the multiplexers. To expand the number of channels, use multiple multiplexers with the inhibit inputs connected to a decoder. See Figure 2.
5. For the MV-808 and MVD-409, it is recommended that 1k pull-up resistors to the +5V logic supply be used when the logic inputs are driven from DTL or TTL circuits. Only these two models require a +5V logic supply.

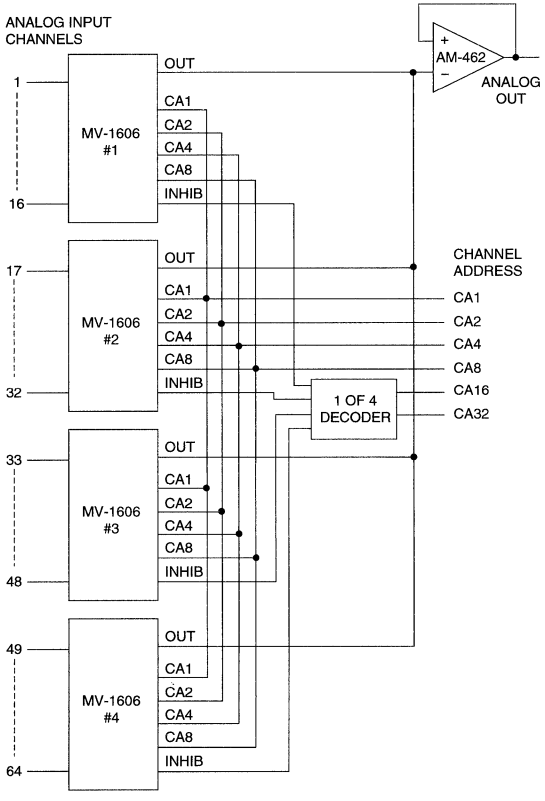


Figure 2. Expansion to 64 Channels

CHANNEL ADDRESSING

MV-808, MVD-807

CA 4	CA 2	CA 1	MVD-807 Inhibit	MV-808 Inhibit	ON Channel
X	X	X	0	1	None
0	0	0	1	0	1
0	0	1	1	0	2
0	1	0	1	0	3
0	1	1	1	0	4
1	0	0	1	0	5
1	0	1	1	0	6
1	1	0	1	0	7
1	1	1	1	0	8

MV-1606

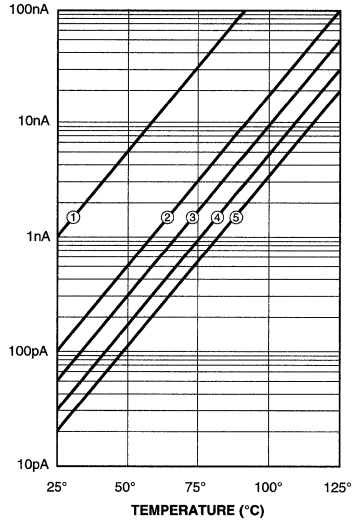
CA 8	CA 4	CA 2	CA 1	Inhibit	ON Channel
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

MVD-409

CA2	CA1	Inhibit	ON Channel
X	X	1	None
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

5

PERFORMANCE GRAPHS



① MV-1606, MVD-807 CHANNEL OFF OUTPUT LEAKAGE
② MV-808 CHANNEL OFF OUTPUT LEAKAGE
③ MVD-409 CHANNEL OFF OUTPUT LEAKAGE
④ MV-1606, MVD-807 CHANNEL OFF INPUT LEAKAGE
⑤ MV-808, MVD-409 CHANNEL OFF INPUT LEAKAGE

Figure 3. Leakage Current vs. Temperature

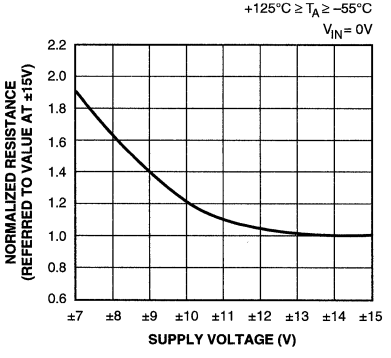


Figure 4. Normalized ON Resistance vs. Supply Voltage

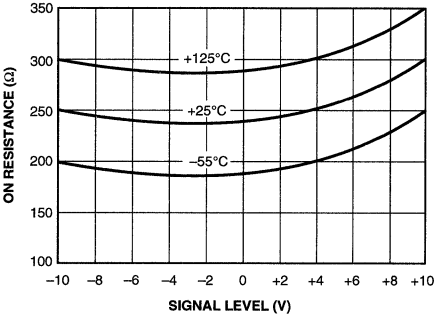


Figure 5. ON Resistance vs. Temperature

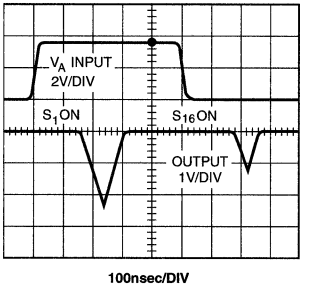


Figure 6. Break-Before-Make Delay (t_{OPEN})

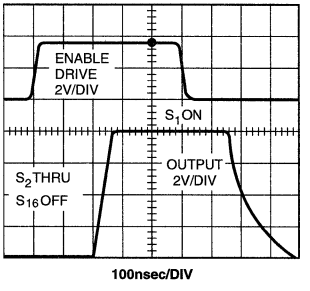


Figure 7. Enable Delay ($t_{ON(EN)}$, $t_{OFF(EN)}$)

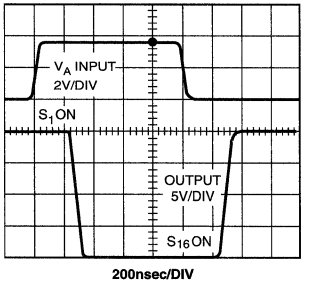


Figure 8. Access Time

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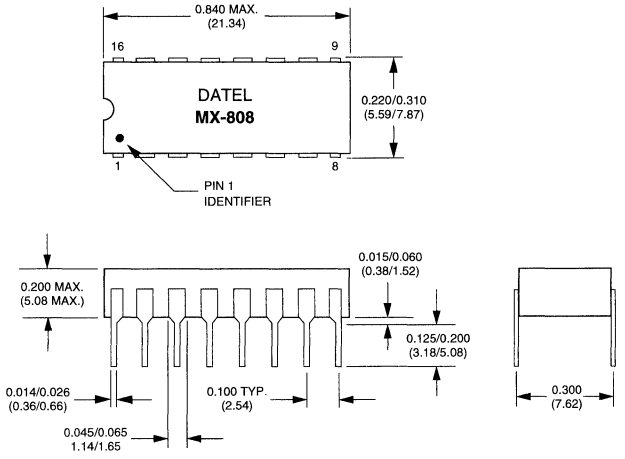
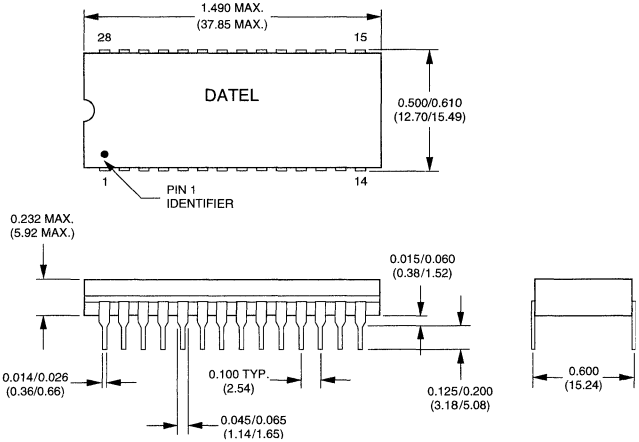
MECHANICAL DIMENSIONS INCHES (mm)

MV-808, MVD-409



MV-1606, MVD-807



ORDERING INFORMATION

MODEL	CHANNELS	OPERATING TEMP. RANGE
MV-808	8 S.E.	0 to +70°C
MV-1606	16 S.E.	0 to +70°C
MV-1606M	16 S.E.	–55 to +125°C
MVD-409	4 Diff.	0 to +70°C
MVD-409M	4 Diff.	–55 to +125°C
MVD-807	8 Diff.	0 to +70°C

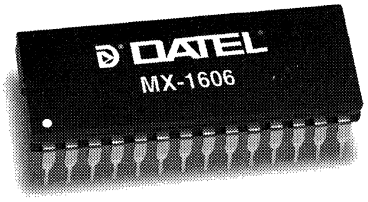
MX/MXD Series

4/8/16-Channel, Input Protected CMOS, Analog Multiplexers

DATEL®
INNOVATION and EXCELLENCE

FEATURES

- **200kHz sampling rates**
- **±0.01% accuracy**
- **Dielectrically isolated CMOS technology**
- **Break-before-make switching**
- **Single-ended or differential inputs**
- **Overvoltage protection, ±35V**
- **DTL/TTL/CMOS compatible**
- **7.5mW standby power**



GENERAL DESCRIPTION

The MX and MXD Series analog multiplexers are 4, 8, and 16-channel monolithic devices manufactured with a dielectrically isolated complementary MOS process. The circuits incorporate analog and digital input protection which protects the units from both overvoltage and loss of power. The digital inputs are DTL/TTL/CMOS compatible and address the proper channel by means of a 2, 3, or 4-bit binary code. An inhibit input enables or disables the entire device and thus permits expansion of the number of channels by using several devices together. Another important feature of these multiplexers is the use of break-before-make switching to ensure that no two channels are ever momentarily shorted together.

Transfer accuracies of ±0.01% can be achieved at channel sampling rates up to 200kHz and over ±10V signal ranges. These multiplexers are ideal for multichannel data acquisition systems where the multiplexer operates into a high-impedance load such as a sample-hold, buffer amplifier, or instrumentation amplifier.

Power consumption is only 7.5mW at standby and 15mW at 100kHz switching rates. Power supply range is ±5V to ±20V. The devices are packaged in 16 or 28-pin DIP's and operate over the 0 to +70°C temperature range.

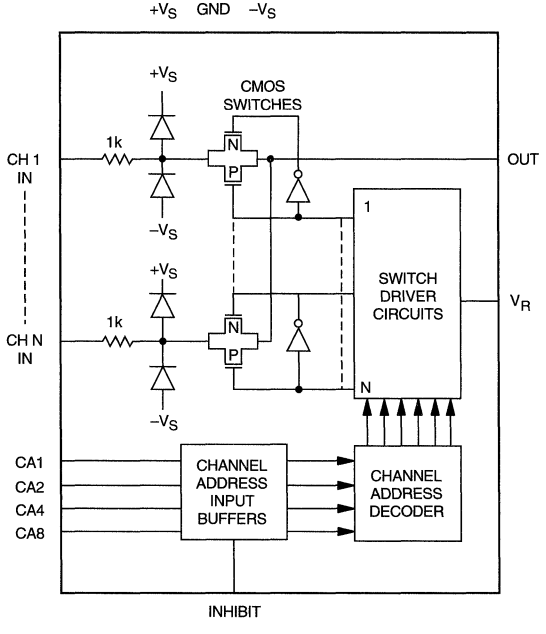


Figure 1. MX Series Functional Block Diagram

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION MX-808	FUNCTION MXD-409	PIN	FUNCTION MX-808	FUNCTION MXD-409
1	CA1	CA1	16	CA2	CA2
2	INHIBIT	INHIBIT	15	CA4	GND
3	–VS	–VS	14	GND	+VS
4	1 IN	1A IN	13	+VS	1B IN
5	2 IN	2A IN	12	5 IN	2B IN
6	3 IN	3A IN	11	6 IN	3B IN
7	4 IN	4A IN	10	7 IN	4B IN
8	OUT	A OUT	9	8 IN	B OUT

PIN	FUNCTION MX-1606	FUNCTION MXD-807	PIN	FUNCTION MX-1606	FUNCTION MXD-807
1	+VS	+VS	28	OUT	A OUT
2	N.C.	B OUT	27	–VS	–VS
3	N.C.	N.C.	26	8 IN	8A IN
4	16 IN	8B IN	25	7 IN	7A IN
5	15 IN	7B IN	24	6 IN	6A IN
6	14 IN	6B IN	23	5 IN	5A IN
7	13 IN	5B IN	22	4 IN	4A IN
8	12 IN	4B IN	21	3 IN	3A IN
9	11 IN	3B IN	20	2 IN	2A IN
10	10 IN	2B IN	19	1 IN	1A IN
11	9 IN	1B IN	18	INHIBIT	INHIBIT
12	GND	GND	17	CA1	CA1
13	VR	VR	16	CA2	CA2
14	CA8	N.C.	15	CA4	CA4

NOTES: CA = Channel address VS = Supply voltage
VR = Reference voltage N.C. = No connection

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MX-808	MX-1606	MXD-409	MXD-807
Voltage Between Supply Pins	40V	40V	40V	40V
V_{REF} to Ground, V + to Ground	+20V	+20V	+20V	+20V
Input Overvoltage				
Digital	$\pm\|V_S + 4V\|$	$\pm\|V_S + 4V\|$	$\pm\|V_S + 4V\|$	$\pm\|V_S + 4V\|$
Analog	$\pm\|V_S + 20V\|$	$\pm\|V_S + 20V\|$	$\pm\|V_S + 20V\|$	$\pm\|V_S + 20V\|$
Power Dissipation	725mW	1200mW	725mW	1200mW

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, ±15V supplies and R source <1k, unless otherwise noted.)

ANALOG INPUTS	MX-808	MX-1606	MXD-409	MXD-807
Number of Channels	8	16	4	8
Type	Single-ended	Single-ended	Differential	Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON				
Resistance	1.5kΩ	1.5kΩ	1.5kΩ	1.5kΩ
Resistance Over Temperature (maximum)	2kΩ	2kΩ	2kΩ	2kΩ
Leakage	100pA	100pA	100pA	100pA
Channel OFF				
Input Leakage	30pA	30pA	30pA	30pA
Output Leakage	0.1nA	0.1nA	0.1nA	0.1nA
Input Capacitance	12pF	12pF	12pF	12pF
Output Capacitance	25pF	50pF	12pF	30pF
DIGITAL INPUTS ①				
Logic "0" Threshold (maximum)	+0.8V	+0.8V	+0.8V	+0.8V
Logic "1" Threshold, TTL (minimum) ②	+4.0V	+4.0V	+4.0V	+4.0V
Logic"1" Threshold, CMOS (minimum) ③	—	+6.0V	—	+6.0V
Input Current (maximum, high or low)	5µA	5µA	5µA	5µA
Channel Address Coding	3 bits	4 bits	2 bits	3 bits
Channel Inhibit (all channels OFF)	Logic "0"	Logic "0"	Logic "0"	Logic "0"
PERFORMANCE				
Transfer Error (maximum)	±0.01%	±0.01%	±0.01%	±0.01%
Crosstalk (1kHz)	0.005%	0.005%	0.005%	0.005%
Common Mode Rejection	—	—	120dB	120dB
Settling Time (20V to ±0.1%) ④	1.2µs	1.2µs	1.2µs	1.2µs
Settling Time (20V to ±0.01%) ④	3.5µs	3.5µs	3.5µs	3.5µs
Turn ON Time	500ns	500ns	500ns	500ns
Turn OFF Time	300ns	300ns	300ns	300ns
Inhibit/Enable Delay	300ns	300ns	300ns	300ns
Break-Before-Make Delay	80ns	80ns	80ns	80ns
POWER REQUIREMENTS				
Rated Power Supply Voltage	±15V	±15V	±15V	±15V
Power Supply Voltage Range	±5 to ±20V	±5 to ±20V	±5 to ±20V	±5 to ±20V
Quiescent Current (maximum)	+2, −1mA	+2, −1mA	+2, −1mA	+2, −1mA
Power Consumption (10kHz sampling)	7.5mW	7.5mW	7.5mW	7.5mW
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range	0 to +70°C	0 to +70°C	0 to +70°C	0 to +70°C
Storage Temperature Range	−65 to +150°C	−65 to +150°C	−65 to +150°C	−65 to +150°C
Package	16-pin DIP	28-pin DIP	16-pin DIP	28-pin DIP

Footnotes:

① The digital inputs are the channel address inputs and the inhibit input.

② To drive from DTL/TTL circuits, 1k pull-up resistors to +5V are recommended. With models MX-1606 and MXD-807, pin 13 should be left open.

③ For a +6.0V threshold with models MX-1606 and MXD-807, pin 13 is connected to +10V.

④ With a load impedance of >100 megohms in parallel with 2pF.

5

TECHNICAL NOTES

1. The transfer accuracy of these multiplexers depends on both the source resistance and the load resistance. With zero source resistance, and assuming 2k Ohms maximum channel ON resistance, the load impedance should be at least 20 megohms to achieve 0.01% accuracy. In practice, it is recommended that a load impedance of at least 100 megohms be used to minimize errors. This can be done by using a good high-gain, high-CMR operational amplifier (such as DATEL's AM 462) as a buffer. Source resistance should be kept as low as possible so that accuracy is not affected; less than 1k Ohms is recommended. Higher source resistance, in addition to affecting accuracy, will degrade the settling time of the multiplexer.
2. For differential operation, two buffer amplifiers or a good quality instrumentation amplifier should be used. To maintain high CMR, source impedance unbalance should be kept to a minimum, the highest possible load impedance should be used, and an amplifier with high CMR should be chosen.
3. Channel expansion is accomplished using the inhibit input of the multiplexer. A logic "0" on this input disables the multiplexer. The expansion technique shown in Figure 2 applies to all of the multiplexer models.
4. The reference terminal (V_R) sets the noise immunity level of the input logic for models MX-1606 and MXD-807. In most cases, this terminal is left open (TTL inputs). For higher level inputs (+6V minimum), this terminal should be connected to +10V. When addressing from DTL/TTL logic, use 1k Ohm pull-up resistors to the +5V supply.

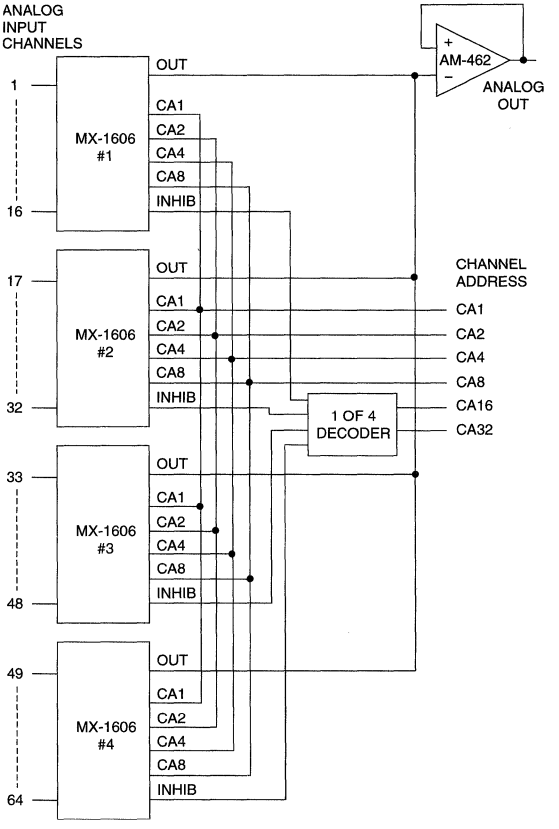

Figure 2. Expansion to 64 Channels

CHANNEL ADDRESSING

MX-1606

CA 8 4 2 1	Inhibit	ON Channel
X X X X	0	None
0 0 0 0	1	1
0 0 0 1	1	2
0 0 1 0	1	3
0 0 1 1	1	4
0 1 0 0	1	5
0 1 0 1	1	6
0 1 1 0	1	7
0 1 1 1	1	8
1 0 0 0	1	9
1 0 0 1	1	10
1 0 1 0	1	11
1 0 1 1	1	12
1 1 0 0	1	13
1 1 0 1	1	14
1 1 1 0	1	15
1 1 1 1	1	16

MX-808, MXD-807

CA 4 2 1	Inhibit	ON Channel
X X X	0	None
0 0 0	1	1
0 0 1	1	2
0 1 0	1	3
0 1 1	1	4
1 0 0	1	5
1 0 1	1	6
1 1 0	1	7
1 1 1	1	8

MXD-409

CA 2 1	Inhibit	ON Channel
X X	0	None
0 0	1	1
0 1	1	2
1 0	1	3
1 1	1	4

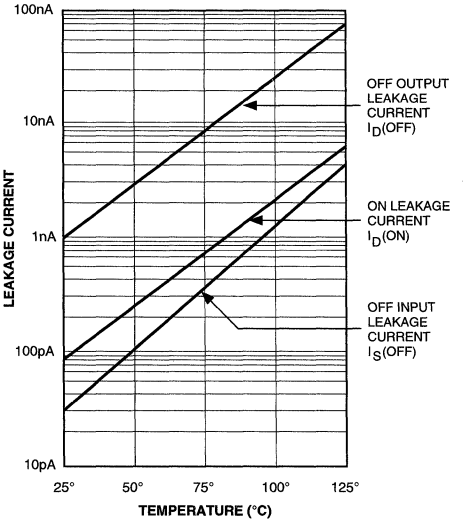

Figure 3. Leakage Current vs. Temperature

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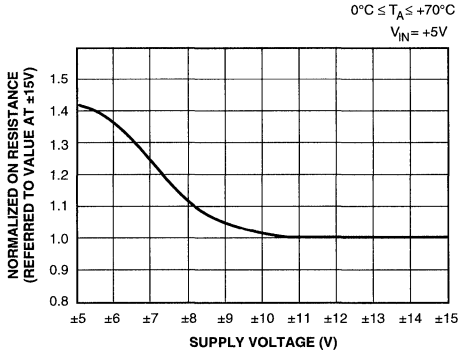


Figure 4. Normalized ON Resistance vs. Supply Voltage

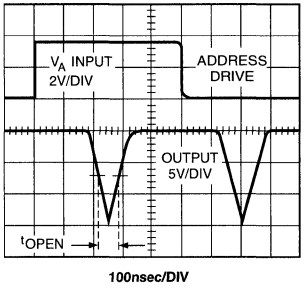


Figure 6. Break-Before-Make Delay (t_{OPEN})

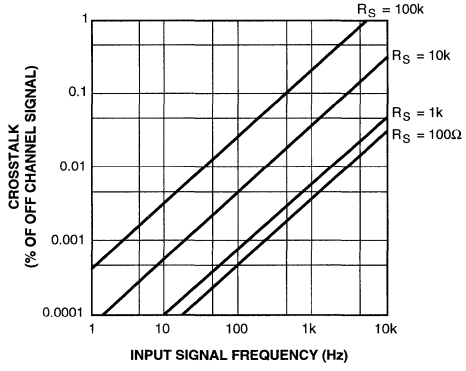


Figure 5. Crosstalk vs. Frequency of Input Signal

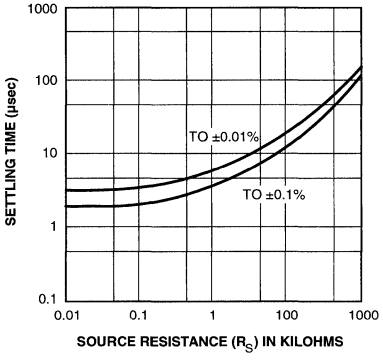


Figure 7. Settling Time vs. Source Resistance (20V Step)

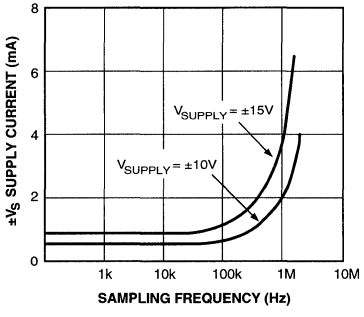
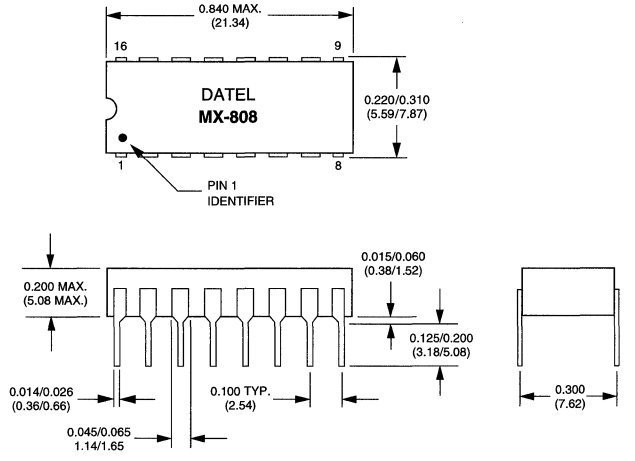


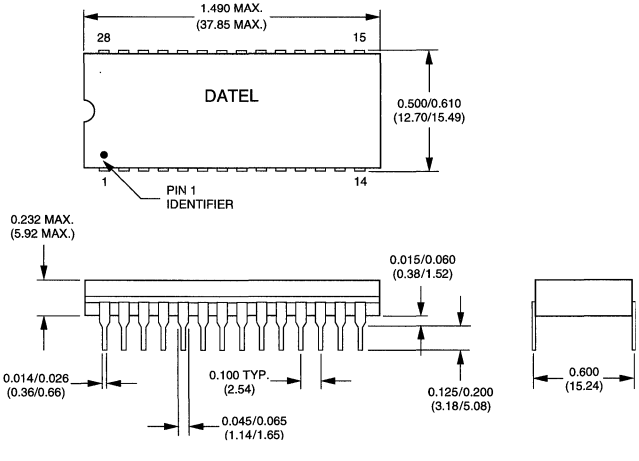
Figure 8. Supply Current vs. Sampling Frequency

MECHANICAL DIMENSIONS
INCHES (mm)

MX-808, MXD-409



MX-1606, MXD-807



ORDERING INFORMATION

MODEL	CHANNELS	OPERATING TEMP. RANGE
MX-808	8 S.E.	0 to +70°C
MX-1606	16 S.E.	0 to +70°C
MXD-409	4 Diff.	0 to +70°C
MXD-807	8 Diff.	0 to +70°C

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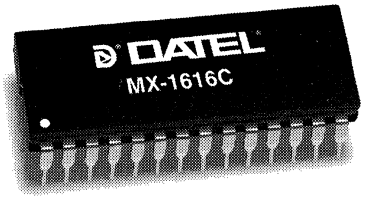
MX-1616, MX-818
High-Speed, CMOS, Programmable Analog Multiplexers

FEATURES

- **800 nanoseconds settling time to ±0.01%**
- **Programmable SE or differential input modes**
- **Break-before-make switching**
- **Dielectrically isolated CMOS technology**
- **TTL/CMOS compatible channel addressing**



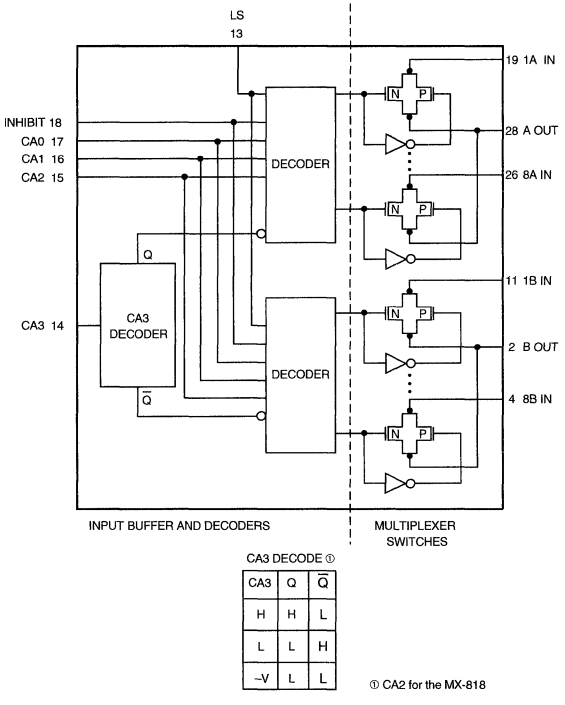
GENERAL DESCRIPTION

The MX-1616 and MX-818 are high-speed, high-performance analog multiplexers manufactured with a dielectrically isolated CMOS process. Both devices achieve transfer accuracies of ±0.01% at channel sampling rates of up to 1.25MHz over ±10V signal ranges. These multiplexers are ideal for high-speed, multichannel data acquisition systems where the multiplexer operates into a high-impedance load such as a sample-hold, buffer amplifier or instrumentation amplifier.

A unique feature of these circuits is the ability of the user to program their inputs for either single-ended or differential operation. The MX-1616 is user programmable either as a single-ended 16-channel or as a differential 8-channel multiplexer while the MX-818 is user programmable either as a single-ended 8-channel or as a differential 4-channel multiplexer.

Digital inputs are user selectable for either TTL or CMOS compatibility. The proper channel is addressed by means of a 3 or 4-bit binary word. An inhibit function enables or disables the entire device, permitting expansion of the number of channels by using several devices together. Another important feature of these devices is the use of break-before-make switching to ensure that no two channels are ever momentarily shorted together.

These multiplexers are packaged in 18 and 28-pin ceramic DIP's and operate over the 0 to +70°C operating temperature range.



CA3 DECODE ①

CA3	Q	Q̄
H	H	L
L	L	H
–V	L	L

① CA2 for the MX-818

Figure 1. Functional Block Diagram (MX-1616 Pinout Shown)

INPUT/OUTPUT CONNECTIONS

MX-1616

PIN	FUNCTION	PIN	FUNCTION
1	+V_S	28	A OUT
2	B OUT	27	–V_S
3	N.C.	26	8A IN
4	8B IN	25	7A IN
5	7B IN	24	6A IN
6	6B IN	23	5A IN
7	5B IN	22	4A IN
8	4B IN	21	3A IN
9	3B IN	20	2A IN
10	2B IN	19	1A IN
11	1B IN	18	INHIBIT
12	GND	17	CA0
13	LS	16	CA1
14	CA3	15	CA2

MX-818

PIN	FUNCTION	PIN	FUNCTION
1	+V_S	18	A OUT
2	B OUT	17	–V_S
3	4B IN	16	4A IN
4	3B IN	15	3A IN
5	2B IN	14	2A IN
6	1B IN	13	1A IN
7	GND	12	INHIBIT
8	LS	11	CA0
9	CA2	10	CA1

NOTES: CA = Channel address; LS = Logic select; V_S = Supply voltage; N.C. = No connection

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MX-1616C	MX-818C
Voltage Between Supply Pins	33Vdc	33Vdc
Analog Input Voltage	$\pm\lvert V_S \pm 2V\rvert$	$\pm\lvert V_S \pm 2V\rvert$
Digital Input Voltage:		
TTL ①	–6V < Logic "1" < +6V	–6V < Logic "1" < +6V
	CA3 = $\pm\lvert V_S \pm 2V\rvert$	CA2 = $\pm\lvert V_S \pm 2V\rvert$
CMOS ②	$+V_S + 2V$	$+V_S + 2V$
	GND – 2V	GND – 2V
Power Dissipation	1200mW	725mW

Footnotes:

① For TTL compatibility, the LS (logic select) pin (MX-1616 pin 13, MX-818 pin 8) is grounded or left open.

② For CMOS compatibility, the LS (logic select) pin (MX-1616 pin 13, MX-818 pin 8) is tied to the system logic supply ($+V_{DD}$).

③ Vin = ±10V, Iout = –100µA

④ 225nsec maximum at full rated operating temperature.

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V supplies, unless otherwise noted.)

ANALOG INPUTS	MX-1616C	MX-818C
Number of Channels	16 single-ended 8 differential	8 single-ended 4 differential
Input Voltage Range	±15V	±15V
Channel ON		
Resistance (max.) ③	750Ω	750Ω
Resistance Over Temp. (max.) ③	1kΩ	1kΩ
Leakage	40pA	15pA
Channel OFF		
Input Leakage	10pA	10pA
Output Leakage	35pA	15pA
Input Capacitance (max.)	10pF	5pF
Output Capacitance (max.)	25pF	10pF
DIGITAL INPUTS ① ②		
Logic "0" Threshold (max.)		
TTL	+0.8V	+0.8V
CMOS	$+0.3V_{DD}$	$+0.3V_{DD}$
Logic "1" Threshold (min.)		
TTL	+2.4V	+2.4V
CMOS	$+0.7V_{DD}$	$+0.7V_{DD}$
Input Leakage Current (max.)		
High	1µA	1µA
Low	25µA	20µA
Channel Address Coding	4 bits	3 bits
Channel Inhibit		
(all channels OFF)	Logic "0"	Logic "0"
PERFORMANCE		
Transfer Error (max.)	±0.01%	±0.01%
Settling Time		
10V Step to ±0.1%	250ns	250ns
10V Step to ±0.01%	800ns	800ns
Access Time (max.)	130ns ④	130ns ④
Enable Delay ON (max.)	175ns	175ns
Enable Delay OFF (max.)	175ns	175ns
Break-Before-Make Delay	20ns	20ns
POWER REQUIREMENTS		
Rated Power Supply Voltage	±15V	±15V
Quiescent Current (max.)	±30mA	±18mA
Power Dissipation (max.)	900mW	540mW
PHYSICAL/ENVIRONMENTAL		
Operating Temperature Range	0 to +70°C	0 to +70°C
Storage Temperature Range	–65 to +155°C	–65 to +155°C
Package	28-pin DIP	18-pin DIP

TECHNICAL NOTES

1. The transfer accuracy of the MX-1616 and MX-818 depends upon both the source and the load resistances. With zero source resistance and assuming 1kΩ maximum channel ON resistance, the load impedance must be at least 10MΩ to achieve 0.01% accuracy. This can be done by using a good high-gain, high-CMR operational amplifier as a buffer. Source resistance should be kept as low as possible so that accuracy and settling time are not degraded. Less than 500Ω is recommended.
2. For differential operation, two buffer amplifiers or a good instrumentation amplifier should be used. To maintain high CMR, source impedance unbalance should be kept to a minimum, the highest possible load impedance should be used and an amplifier with high CMR should be chosen.
3. These devices have the added feature of being programmable for single-ended or differential operation. The MX-1616 is user programmed for single-ended 16-channel operation by connecting A OUT (pin 28) to B OUT (pin 2) and using CA3 (pin 14) as a digital address input. To program the MX-1616 for differential 8-channel operation, CA3 (pin 14) is simply connected to $-V_S$ (pin 27). The MX-818 may be programmed as a single-ended 8-channel multiplexer by connecting A OUT (pin 18) to B OUT (pin 2) and using CA2 (pin 9) as a digital input address, or as a differential 4-channel multiplexer by connecting CA2 (pin 9) to $-V_S$ (pin 17). Refer to the truth tables for channel addressing.
4. Both devices are selectable for either TTL or CMOS compatibility. For TTL compatibility, the LS (logic select) pin (MX-1616 pin 13, MX-818 pin 8) is left open or grounded. For CMOS compatibility, the LS pin should be connected to the system logic supply ($+V_{DD}$).
5. Channel expansion is accomplished by the use of the inhibit input of the multiplexers. To expand the number of channels, use multiple multiplexers with the inhibit inputs connected to a decoder.

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CHANNEL ADDRESSING

MX-1616 USED AS 16-CHANNEL MULTIPLEXER

USE CA3 AS A DIGITAL ADDRESS INPUT				ON CHANNEL TO		
3	2	1	0	Inhibit	Output A	Output B
X	X	X	X	0	None	None
0	0	0	0	1	1A	—
0	0	0	1	1	2A	—
0	0	1	0	1	3A	—
0	0	1	1	1	4A	—
0	1	0	0	1	5A	—
0	1	0	1	1	6A	—
0	1	1	0	1	7A	—
0	1	1	1	1	8A	—
1	0	0	0	1	—	1B
1	0	0	1	1	—	2B
1	0	1	0	1	—	3B
1	0	1	1	1	—	4B
1	1	0	0	1	—	5B
1	1	0	1	1	—	6B
1	1	1	0	1	—	7B
1	1	1	1	1	—	8B

MX-1616 USED AS DUAL 8-CHANNEL MULTIPLEXER

CONNECT CA3 TO –V SUPPLY			ON CHANNEL TO		
2	1	0	Inhibit	Output A	Output B
X	X	X	0	None	None
0	0	0	1	1A	1B
0	0	1	1	2A	2B
0	1	0	1	3A	3B
0	1	1	1	4A	4B
1	0	0	1	5A	5B
1	0	1	1	6A	6B
1	1	0	1	7A	7B
1	1	1	1	8A	8B

MX-818 USED AS 8-CHANNEL MULTIPLEXER

USE CA2 AS A DIGITAL ADDRESS INPUT			ON CHANNEL TO		
2	1	0	Inhibit	Output A	Output B
X	X	X	0	None	None
0	0	0	1	1A	—
0	0	1	1	2A	—
0	1	0	1	3A	—
0	1	1	1	4A	—
1	0	0	1	—	1B
1	0	1	1	—	2B
1	1	0	1	—	3B
1	1	1	1	—	4B

MX-818 USED AS DUAL 4-CHANNEL MULTIPLEXER

CONNECT CA2 TO –V SUPPLY			ON CHANNEL TO	
1	0	Inhibit	Output A	Output B
X	X	0	None	None
0	0	1	1A	1B
0	1	1	2A	2B
1	0	1	3A	3B
1	1	1	4A	4B

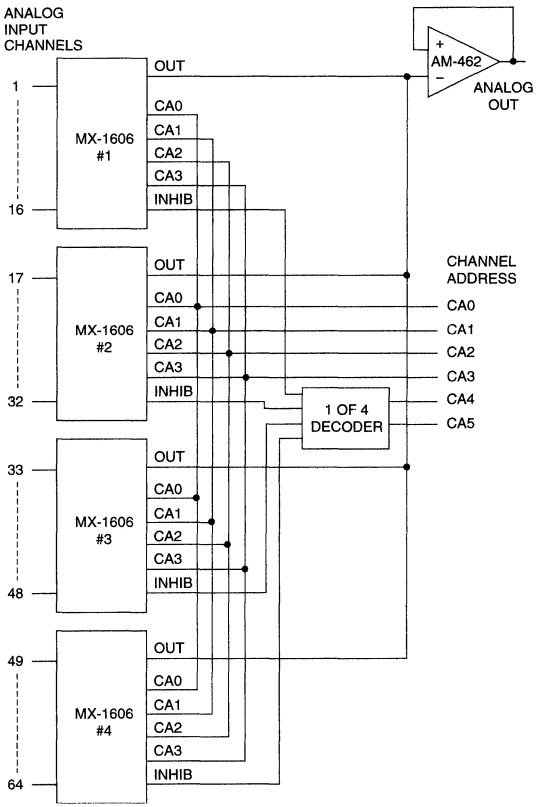
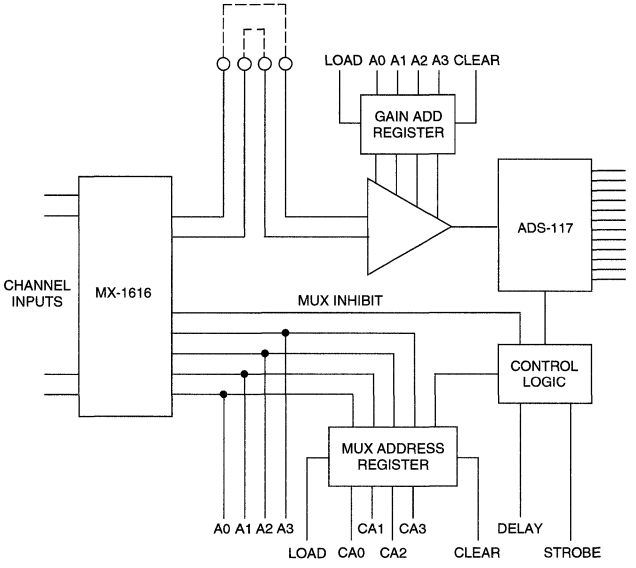
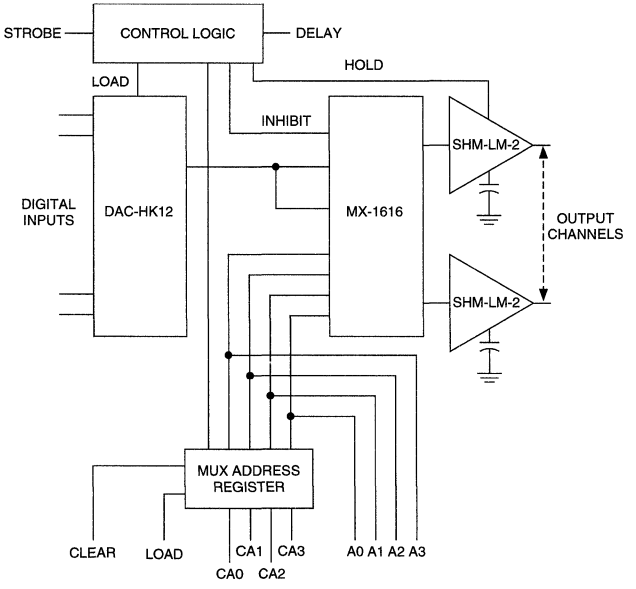


Figure 2. Expansion to 64 Channels

APPLICATIONS



NOTE: This application diagram shows a high-speed data acquisition system with 8 differential inputs and 12-bit resolution that utilizes the MX-1616. If the control logic is timed so that the sampling A/D section is converting one analog value while the mux-amplifier section is allowed to settle to the next input value, throughput rates approaching 1MHz can be achieved. The MX-1616 is used with DATEL's ADS-117, a 12-bit sampling A/D with a 2MHz conversion rate.



NOTE: The switches in a CMOS multiplexer will conduct equally well in either direction, making it feasible to use them as single input-selected multiple output switches. The circuit shown is capable of sample rates of 78kHz for inputs of ±10V. The MX-1616 is used with DATEL's DAC-HK12, a 12-bit hybrid D/A with input registers and the SHM-LM-2, a low-cost monolithic sample-hold.

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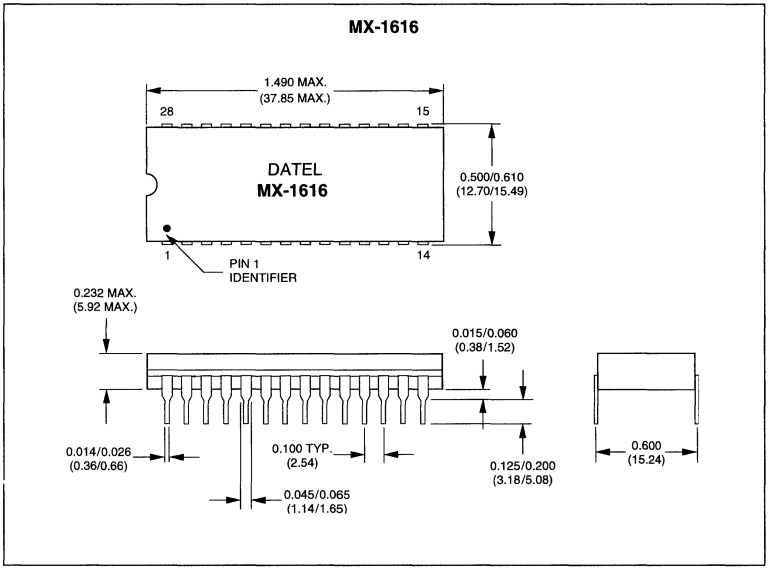
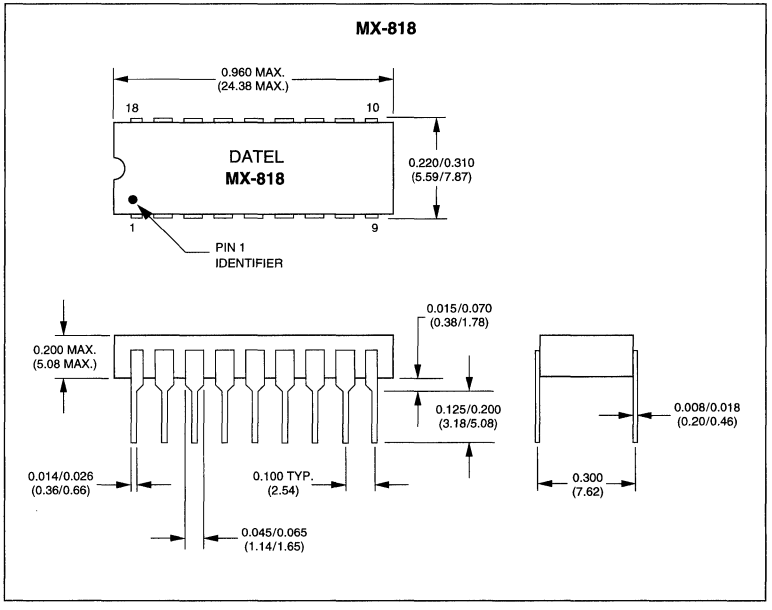
MECHANICAL DIMENSIONS INCHES (mm)

MX-1616



MX-818



ORDERING INFORMATION

MODEL	CHANNELS	OPERATING TEMP. RANGE
MX-818C	8 S.E. or 4 Diff.	0 to +70°C
MX-1616C	16 S.E. or 8 Diff.	0 to +70°C

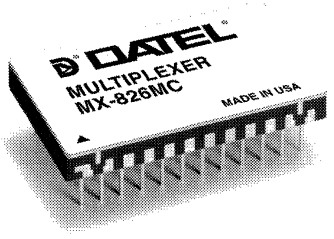
MX-826

Precision, High-Speed 8-Channel, Analog Multiplexers

DATEL®
INNOVATION and EXCELLENCE

FEATURES

- **170ns maximum settling time to ±0.1%**
- **225ns maximum settling time to ±0.01%**
- **400ns maximum settling time to ±0.003%**
- **8 Channels single-ended inputs**
- **395mW power dissipation**
- **Small, 24-pin DDIP package**



GENERAL DESCRIPTION

The MX-826 is a precision, high-speed multiplexer characterized for 10, 12 and 14-bit applications. The performance benchmarks are its 225 nanoseconds maximum settling time to ±0.01% accuracy and its unprecedented specification of accuracy to ±0.003%.

The MX-826 provides eight single-ended inputs. Channel addressing is done by a three-bit binary code and break-before-make switching assures that no two channels are ever momentarily shorted together.

The MX-826 operates from ±15V and +5V power supplies. Models are available in two operating temperature ranges: 0 to +70°C and –55 to +125°C. MIL-STD-883 screening is optional.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	A0	24	+5V SUPPLY
2	A1	23	GROUND
3	A2	22	N.C.
4	IN1	21	N.C.
5	IN2	20	N.C.
6	IN3	19	–15V SUPPLY
7	IN4	18	GROUND
8	IN5	17	GROUND
9	IN6	16	+15V SUPPLY
10	IN7	15	N.C.
11	IN8	14	N.C.
12	GROUND	13	OUTPUT

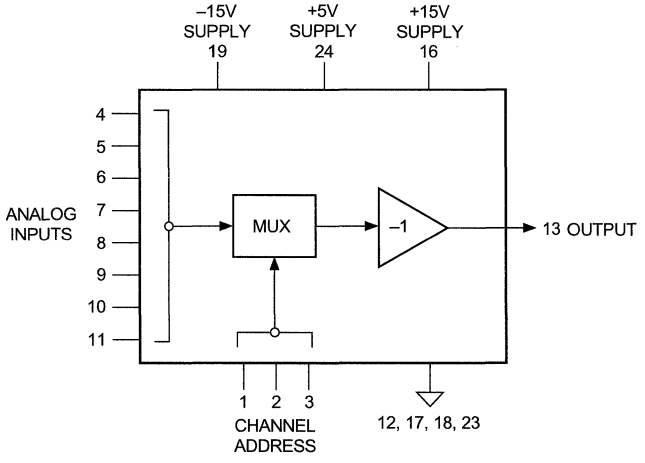


Figure 1. Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS
+15V Supply, Pin 16	0 to +18V
–15V Supply, Pin 19	0 to –18V
+5V Supply, Pin 24	–0.5 to +7V
Digital Inputs, Pins 1, 2, 3	–0.3 to +5.5V
Analog Inputs, Pins 4-11	–15 to +15V
Lead Temperature (10s)	300°C
Short Circuit to Ground , Pin 13	Continuous

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range and over the operating power supply range unless otherwise specified.)

INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	±10	±10.5	—	Volts
Digital Input, Logic Levels				
Logic 1	+2.0	—	—	Volts
Logic 0	—	—	+0.8	Volts
Logic Loading				
Logic 1	—	—	+10	µA
Logic 0	—	—	–10	µA
OUTPUTS				
Output Range	±10.0	±10.5	—	Volts
Output Current	±15	—	—	mA
Stable Capacitive Load	100	—	—	pF
Output Impedance DC	—	0.1	—	Ohms
PERFORMANCE				
Gain	—	–1	—	V/V
Gain Error, 25°C	—	—	±0.03	%FS
Gain Tempco				
–55 to +125°C	—	±0.5	±5	ppm/°C
Offset, 25°C	—	±0.1	±0.5	mV
Offset Voltage Drift	—	<5	±15	µV/°C
Slew Rate	±250	±300	—	V/µs
Cross Talk				
100kHz	—	–90	–83	dB
1MHz	—	–80	–75	dB
Bandwidth				
3dB Small Signal	8	8.5	—	MHz
Full Power	3	4.5	—	MHz
Input Impedance	2.45	2.5	2.55	kΩ
Output Settling Time				
(10V step, +25°C) 500Ω Load				
±0.1% 10 Bits	—	100	170	ns
±0.01% 12 Bits	—	150	225	ns
±0.003% 14 Bits	—	300	400	ns
(20V step, + 25°C) 1kΩ Load				
±0.1% 10 Bits	—	150	200	ns
±0.01% 12 Bits	—	200	300	ns
±0.003% 14 Bits	—	600	720	ns
Switching Characteristics				
Break-Before-Make Delay	8	15	25	ns
Turn On Time	—	20	50	ns
Turn Off Time	—	20	50	ns
Harmonic Distortion				
DC to 500kHz, 10Vp-p	—	–90	–80	dB
Signal-to-Noise Ratio				
With Distortion	—	72	69	dB
Without Distortion	—	80	75	dB

POWER REQUIREMENTS	MIN	TYP	MAX	UNITS
Range				
+15V Supply	+14.5	+15	+15.5	Volts
–15V Supply	–14.5	–15	–15.5	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Current (Quiescent)				
+15V Supply	—	+13	+21	mA
–15V Supply	—	–13	–21	mA
+5V Supply	—	<1	+1	mA
Power Supply Rejection Ratio	86	—	—	dB
Power Dissipation	—	395	575	mW
PHYSICAL/ENVIRONMMENTAL				
Operating Temp. Range, Case				
MC Model	0	—	+70	°C
MM Model	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type	24-pin, metal-sealed, ceramic DDIP			
Weight	0.42 oz. (12 grams)			

TECHNICAL NOTES

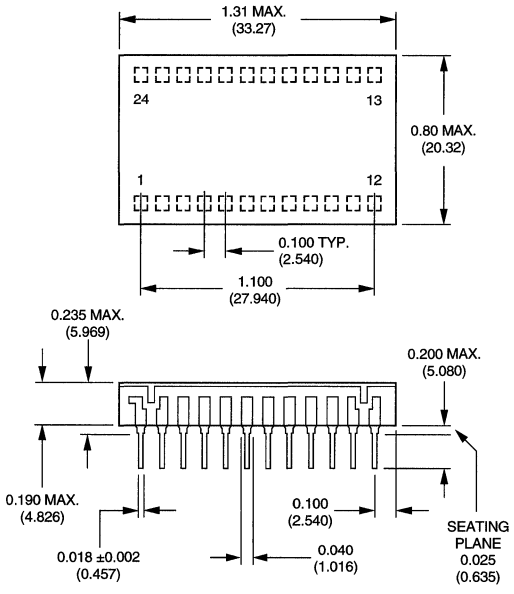
1. Bypass the ±15V and +5V power supplies with a 1µF, 25V tantalum electrolytic capacitors in parallel with a 0.1µF ceramic capacitors.
2. Analog signals up to ±15V may be present while the MUX power supplies are off.
3. The absence of an RON specification or output leakage specification is related to the architecture of the switching network. The inputs see a constant 2.5k Ohm input impedance whether the channel is on or off.
4. Typical recovery time from an overvoltage condition of >±3V is approximately 200 nanoseconds from a negative overdrive and 700 nanoseconds from a positive overdrive.
5. Double-level multiplexing may be used to provide up to 64 channels (nine MX-826's required).

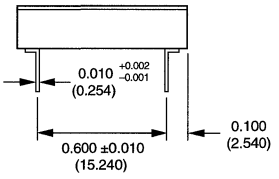
Table 1. Channel Addressing

On Channel	MUX Address A2	A1	A0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

5

MECHANICAL DIMENSIONS
INCHES (mm)





24-PIN DDIP

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NO.	CHANNELS	OPER. TEMP. RANGE
MX-826MC	8SE	0 to +70°C
MX-826MM	8SE	–55 to +125°C
MX-826/883	8SE	–55 to +125°C

DESC drawing available: Drawing Number 5962-9450601.
For MIL-STD-883 product specifications, contact DATEL.

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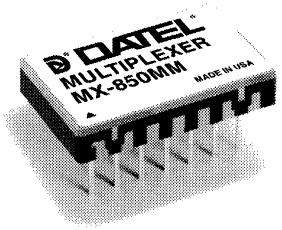
MX-850

Precision, Higher-Speed 4-Channel, Analog Multiplexers

FEATURES

- **50ns settling time to ±0.01%**
- **70ns settling time to ±0.003%**
- **100ns settling time to ±0.001%**
- **4 Channels, single-ended inputs**
- **100mW power dissipation**
- **Small, 14-pin DIP package**



GENERAL DESCRIPTION

The MX-850 is a precision, high-speed multiplexer characterized for 10, 12, 14 and 16-bit applications. The performance benchmarks are its 50 nanosecond maximum settling time to ±0.01% accuracy and its unprecedented ±0.001% accuracy specification.

Packaged in a miniature, 14-pin, ceramic DIP, the MX-850 operates from ±15V and +5V supplies and consumes a maximum 270mW. Models are available for either 0 to +70°C or –55 to +125°C operation.

Table 1. Channel Addressing

ON CHANNEL	MUX ADDRESS $\overline{EN}$	A_1	A_0
Disable	1	X	X
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	$\overline{ENABLE}$
2	A0
3	A1
4	CH1 INPUT
5	CH2 INPUT
6	CH3 INPUT
7	CH4 INPUT
8	OUTPUT
9	GROUND
10	+15V SUPPLY
11	GROUND
12	+5V SUPPLY
13	GROUND
14	–15V SUPPLY

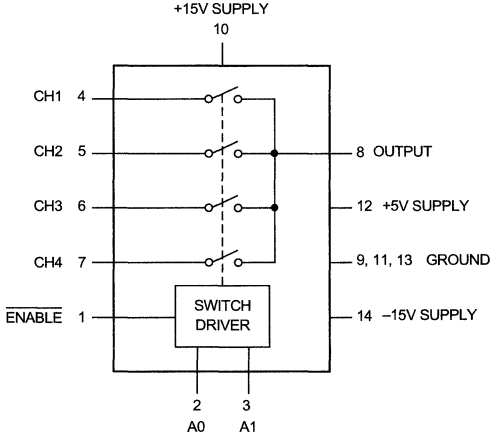


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETER	LIMITS	UNITS
+15V Supply, Pin 10	–0.5 to +16.5	Volts
–15V Supply, Pin 14	+0.5 to –16.5	Volts
+5V Supply, Pin 12	–0.5 to +7	Volts
Digital Inputs, Pins 1, 2, 3	–0.5 to +6	Volts
Analog Inputs, Pins 4, 5, 6, 7	–10.5 to +10.5	Volts
Analog Input Current	±20	mA
Lead temperature (10 seconds)	300	°C
Switching Frequency/Duty Cycle	10/50	MHz/%

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range and over the operating power supply range unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range	±10	—	—	Volts
On Resistance, +25°C	—	18	90	Ohms
0 to +70°C	—	—	120	Ohms
–55 to +125°C	—	—	140	Ohms
R_{ON} versus V_{IN}	See Figure 2			
Input Leakage Current (Off)				
+25°C	—	±0.02	±0.2	nA
0 to +70°C	—	—	±10	nA
–55 to +125°C	—	—	±25	nA
Output Leakage Current (Off)				
+25°C	—	±0.02	±0.2	nA
0 to +70°C	—	—	±20	nA
–55 to +125°C	—	—	±40	nA
On Channel Leakage Current				
+25°C	—	±0.4	±1	nA
0 to +70°C	—	—	±25	nA
–55 to +125°C	—	—	±35	nA
Channel Input Capacitance				
Off	—	4	6	pF
On	—	10	12	pF
Channel Output Capacitance				
On	—	8	10	pF
Nonlinearity	—	—	±0.001	%FSR
Large signal bandwidth (–3dB)	80	100	—	MHz
DIGITAL INPUTS				
Logic levels				
Logic "1"	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	Volts
Logic Loading "1"	—	—	+10	µA
Logic Loading "0"	—	—	–10	µA
SWITCHING CHARACTERISTICS				
Access Time	—	—	20	ns
Break-Before-Make Delay Time	—	—	10	ns
Enable Delay (On, Off)	—	3	10	ns
Settling Time, 10M Load				
10V step to ±0.1%	—	25	30	ns
10V step to ±0.01%	—	40	50	ns
10V step to ±0.003%	—	60	70	ns
10V step to ±0.001%	—	80	100	ns
Settling Time, 5k Load				
10V step to ±0.1%	—	25	30	ns
10V step to ±0.01%	—	40	50	ns
10V step to ±0.003%	—	60	70	ns
10V step to ±0.001%	—	80	100	ns
Settling Time, 10M Load				
20V step to ±0.1%	—	30	35	ns
20V step to ±0.01%	—	50	60	ns
20V step to ±0.003%	—	75	85	ns
20V step to ±0.001%	—	100	120	ns

SWITCHING CHAR. (cont.)	MIN.	TYP.	MAX.	UNITS
Settling Time, 5k Load				
20V step to ±0.1%	—	30	35	ns
20V step to ±0.01%	—	50	60	ns
20V step to ±0.003%	—	75	85	ns
20V step to ±0.001%	—	100	120	ns
Crosstalk ①				
10kHz (20Vp-p)	—	–105	–100	dB
1MHz (20Vp-p)	—	–94	–92	dB
10MHz (5Vp-p)	—	–76	–71	dB
20MHz (3Vp-p)	—	–64	–62	dB
POWER REQUIREMENTS				
Power Supply Range				
+15V Supply	+14.5	+15	+15.5	Volts
–15V Supply	–14.5	–15	–15.5	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Current, Quiescent				
+15V Supply	—	+3	+4	mA
–15V Supply	—	–10	–12	mA
+5V Supply	—	+3	+3.5	mA
Power Supply Rejection Ratio	80	90	—	dB
Power Supply Dissipation, Quiescent				
+25°C	—	207	270	mW
0 to +70°C	—	—	270	mW
–55 to +125°C	—	—	280	mW
Pd versus Frequency	See Figure 4			
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
MX-850MC	0	—	+70	°C
MX-850MM	–55	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	14-pin, metal-sealed, ceramic DIP			
Weight	0.1 ounces (2.8 grams)			

① See Figures 3a and 3b.

TECHNICAL NOTES

1. Proper operation of the MX-850 multiplexer is dependent upon good board layout and connection practices. Bypass supplies as shown in the connection diagrams. Mount bypass capacitors directly to the supply pins whenever possible.
2. All grounds pins (9, 11, 13) should be tied together and connected to ground as close to the multiplexer as possible.
3. When power is off, current limit input signals on pins 4, 5, 6, and 7 to 20mA. Failure to current limit can cause permanent damage to the device since, when powering up or down it is possible that two switches might be on at the same time. Excessive current (greater than 20mA) will flow from the more positive input to the more negative input, permanently damaging the device. Applications in which the power supply for the multiplexer also powers the signal sources may not require limiting resistors. See Figure 4.

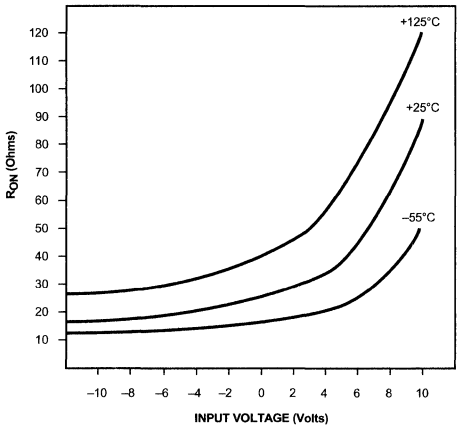


Figure 2. Channel On Resistance Versus Input Voltage

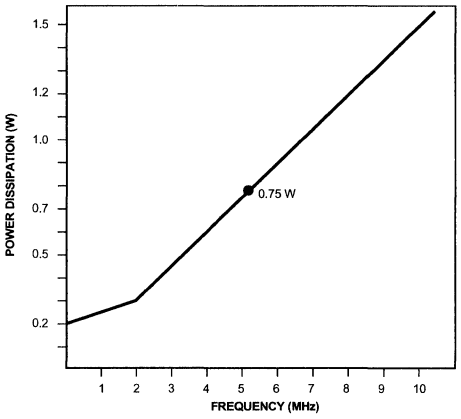


Figure 4. Power Dissipation Versus Switching Frequency

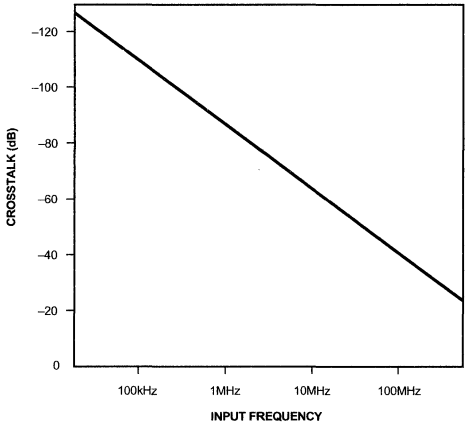


Figure 3a. Small Signal Crosstalk Versus Input Frequency

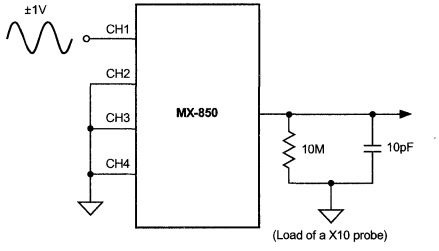


Figure 3b. Crosstalk Test Circuit

CURRENT LIMITING RESISTORS

As noted in Technical Note 3, some current limiting technique must be employed to protect the device. The following lists the suggested resistor values for the current limiting resistors shown in Figure 5.

Input Range	Limiting Resistors
±10V	R = 500Ω
±5V	R = 250Ω
≤±1V	No current limiting needed

Other current limiting circuits can be used, such as a current limited op amp drive, depending upon the application.

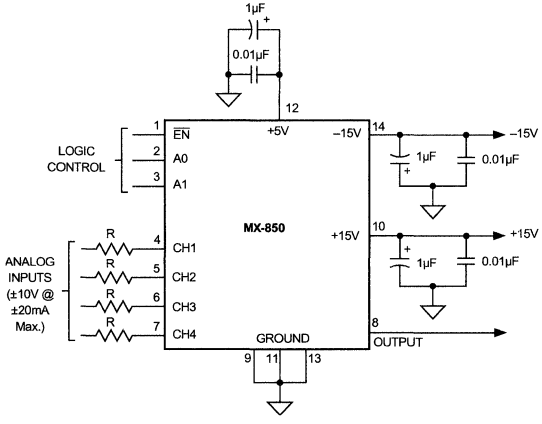


Figure 5. Typical Connections

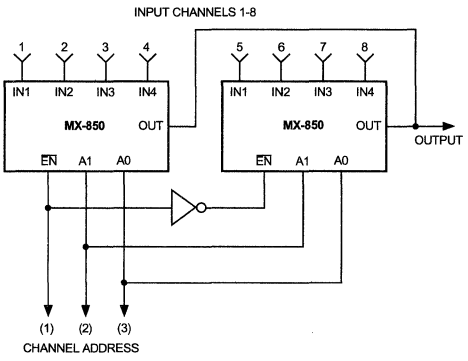


Figure 6. Cascading Multiple MX-850's

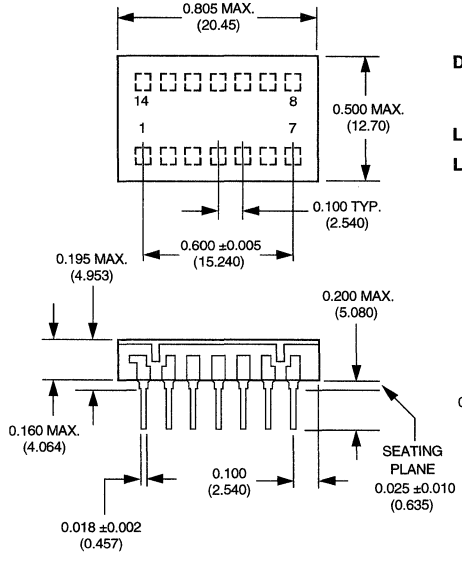
Table 2. 8 Channel Addressing

ON CHANNEL	MUX ADDRESS 1	2	3
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

CHANNEL EXPANSION

The MX-850's $\overline{\text{ENABLE}}$ input provides a means of channel expansion. As shown in Figure 6 and in Table 2, multiple multiplexers may be used by using the $\overline{\text{ENABLE}}$ input as an address line.

MECHANICAL DIMENSIONS
INCHES (mm)

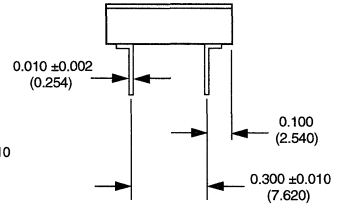


14-PIN DIP

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
MX-850MC	0 to +70°C
MX-850MM	–55 to +125°C

For availability of a high-reliability (QL) version, contact DATEL.

DATEL, Inc., 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For immediate assistance 800-233-2765

Digital-to-Analog Converters

Table of Contents

Selection Guide

Model ①	Resolution (Bits)	Settling Time (µsec)	Output	Differential Linearity Error, Max. (LSB)	Integral Linearity Error, Max. (LSB)	Coding	Power Supplies (Volts)	Maximum Power Dissipation (mW)	Page
DAC-HF8B	8	0.025	+5, ±2.5mA	±0.5	±0.5	Bin	±15	750	**6-3**
DAC-HF10B	10	0.025	+5, ±2.5mA	±0.5	±0.5	Bin	±15	825	**6-3**
DAC-HF12B	12	0.05	+5, ±2.5mA	±0.5	±0.5	Bin	±15	975	**6-3**
DAC-HK12B	12	3	+5/10, ±2.5/5/10V	±0.75	±0.5	Bin, 2C	+5, ±15	1000 ②	**6-7**
DAC-HZ12B	12	3	+5/10, ±2.5/5/10V	±0.75	±0.5	CBin	±15	500	**6-15**
DAC-HZ12D	3-Digit	3	+2.5/5/10V	±0.25	±0.25	CBCD	±15	500	**6-15**
DAC-HP16B	16	15	+10, ±5/10V	±2	±2	CBin	±15	675 ②	**6-11**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① MIL-STD-883 models available for all listed products except DAC-HZ Series.
② Typical.

For literature or technical assistance

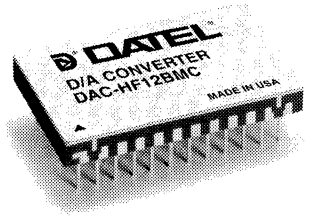
800-233-2765

or contact your local DATEL Sales Office or Representative

DAC-HF Series
Ultra-Fast, 8/10/12-Bit Digital-to-Analog Converters

FEATURES

- **8, 10 and 12-Bit resolutions**
- **Settling times to 25ns**
- **±20ppm/°C max. gain tempco**
- **Unipolar or bipolar operation**
- **Current output**
- **Internal feedback resistors**
- **High-reliability MIL-STD-883 models**



GENERAL DESCRIPTION

The DAC-HF Series of hybrid DAC's are ultra high-speed, current output devices. They incorporate state-of-the-art performance in a miniature package, achieving maximum output settling times of 25ns for the 8 and 10-bit models and 50ns for the 12-bit model. They can be used to drive a resistor load directly for up to ±1V output or a fast operational ampifier (such as DATEL's AM-500) for higher voltage outputs with sub-microsecond settling times. A tapped feedback resistor and a bipolar offset resistor are included internally to give five programmable output voltage ranges with an external operational amplifier.

The DAC-HF design combines proven hybrid construction techniques with advanced circuit design to realize high-speed current switching. The design incorporates fast PNP current switches driving a low-impedance R-2R thin-film ladder network. The nichrome thin-film resistor network is deposited by electron beam evaporation on a low-capacitance substrate to assure high-speed performance. The resistors are then functionally trimmed by laser for optimum linearity.

INPUT/OUTPUT CONNECTIONS, DAC-HF12B

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	24	+15V SUPPLY
2	BIT 2	23	GROUND
3	BIT 3	22	–15V SUPPLY
4	BIT 4	21	REFERENCE OUT
5	BIT 5	20	BIPOLAR OFFSET
6	BIT 6	19	10V RANGE
7	BIT 7	18	OUTPUT
8	BIT 8	17	20V RANGE
9	BIT 9 *	16	REFERENCE IN
10	BIT 10 *	15	GROUND
11	BIT 11 *	14	GROUND
12	BIT 12 (LSB) *	13	GROUND

* See note in Figure 1

6

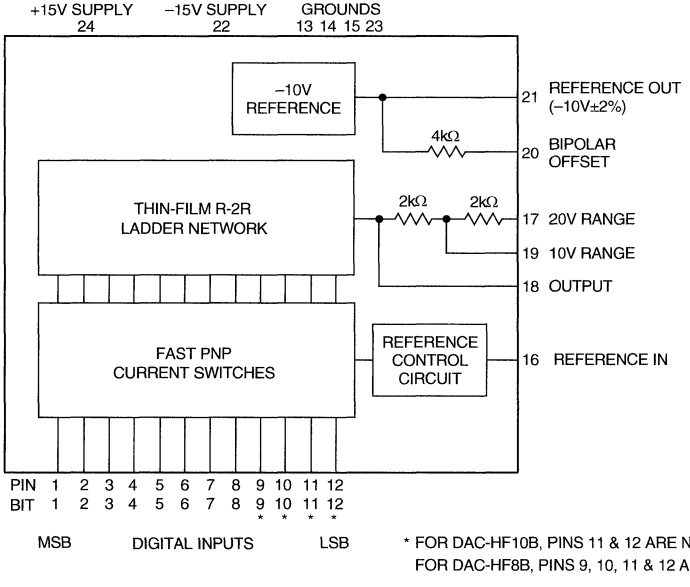


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS, ALL MODELS

Positive Supply, Pin 24	+18V
Negative Supply, Pin 22	–18V
Digital Input Voltage, Pins 1–12	+15V
Lead Temperature (soldering, 10s)	300°C

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V supplies unless otherwise noted.)

DESCRIPTION	8B	10B	12B
INPUTS			
Resolution, Bits	8	10	12
Coding, Unipolar Output	Straight binary		
Coding, Bipolar Output	Offset binary		
Input Logic Level, Bit ON ("1")	+2.0V to +5.5V at +40µA		
Input Logic Level, Bit OFF ("0")	0V to +0.8V at –2.6mA		
PERFORMANCE			
Nonlinearity Error, max.	±0.012%		
T_{MIN} to T_{MAX}	±0.024%		
Differential Nonlinearity Error, max.	±0.012%		
T_{MIN} to T_{MAX}	±0.024%		
Monotonicity	Guaranteed over oper. temp. range		
Gain Tempco, max.	±20ppm/°C		
Offset Tempco, Bipolar, max.	±10ppm/°C of FSR ②		
Zero Tempco, max.	±1.5ppm/°C of FSR ②		
Settling Time, ns max. ③	25	25	50
Power Supply Sensitivity	±0.01%/% Supply		
OUTPUTS			
Output Current Range, Unipolar	0 to +5mA		
Output Current Range, Bipolar	±2.5mA		
Output Compliance Voltage	±1.2V		
Output Voltage Ranges ①	0 to –5V 0 to –10V ±2.5V ±5V ±10V		
Output Resistance	400 Ohms ±20%		
Output Capacitance	15pF		
Output Leakage Current, All Bits OFF	15nA		
POWER REQUIREMENTS			
Supply Voltages	±15V ±0.5V		
Positive Quiescent Current, max.	35mA	40mA	50mA
Negative Quiescent Current, max.	15mA	15mA	15mA
PHYSICAL ENVIRONMENTAL			
Operating Temperature Range, Case	0°C to +70°C (BMC) –55°C to +125°C (BMM, 883)		
Storage Temperature Range	–65°C to +150°C		
Package Type	24-pin ceramic DDIP		
Weight	0.22 ounces (6.3 grams)		

Footnotes

① With external operational amplifier.

② FSR is Full Scale Range, or the difference between minimum and maximum output values.

③ Full-scale current change to ±1LSB with 400Ω load.

TECHNICAL NOTES

1. Proper operation of the DAC-HF Series converters is dependent on good board layout and connection practices. Bypass supplies as shown in the connection diagrams. Mount bypass capacitors close to the converter, directly to the supply pins where possible.

2. Use of a ground plane is particularly important in high-speed D/A converters as it reduces high-frequency noise and aids in decoupling the digital inputs from the analog output. Avoid ground loop problems by connecting all grounds on the board to the ground plane. The remainder of the ground plane should include as much of the circuit board as possible.

3. When the converter is configured for voltage output with an external operational amplifier, keep the leads from the converter to the output amplifier as short as possible.

4. The high-speed current switching technique used in the DAC-HF Series inherently reduces the amplitude and duration of large transient spikes at the output ("glitches"). The most severe glitches occur at half-scale, the major carry transition from 011 ... 1 to 100 ... 0 or vice versa. At this time, a skewing of the input codes can create a transition state code of 111 ... 1. The duration of the "transition state code" is dependent on the degree of skewing, but its effect is dependent on the speed of the DAC (an ultra-fast DAC will respond to these brief spurious inputs to a greater degree than a slow DAC).

   Minimize the effects of input skewing by using a high-speed input register to match input switching times. The input register recommended for use with the DAC-HF is easily implemented with two Texas Instruments SN74S174 hex D-type flip-flops. This register will reduce glitches to a very low level and ensure fast output settling times.

5. Test the DAC-HF using a low-capacitance test probe (such as a 10X probe). Take care to assure the shortest possible connection between probe ground and circuit ground. Long probe ground leads may pick up environmental E.M.I. causing artifacts on the scope display, i.e., signals that do not originate at the unit under test.

6. Passive components used with the DAC-HF may be as indicated here: 0.1µF and 1µF bypass capacitors should be ceramic type and tantalum type respectively; the 400Ω output load is a ±0.1%, 10ppm/°C, metal-film type; adjustment potentiometers are ceremet types; other resistors may be ±10% carbon composition types.

7. Output voltage compliance is ±1.2V to preserve the linearity of the converter. In the bipolar mode, the DAC-HF can be operated with no load to give an output voltage of ±1.0V. In the unipolar mode, the load resistance must be less than 600Ω to give less than +1.2V output. The specified output currents of 0 to +5mA and ±2.5mA are measured into a short circuit or an operational amplifier summing junction.

CONNECTION AND CALIBRATION

CALIBRATION PROCEDURE

Unipolar Output Current

1. Connect the converter as shown in Figure 2.
2. Set all inputs low and adjust the ZERO ADJUST potentiometer for a reading of 0V at the output.
3. Set all inputs high and adjust the GAIN ADJUST potentiometer for a reading of –F.S. + 1LSB (See Table 1).

Bipolar Output Current

1. Connect the converter as shown in Figure 3.
2. Set all inputs low and adjust the OFFSET ADJUST potentiometer for an output reading of +F.S. (See Table 2).
3. Set all inputs high and adjust the GAIN ADJUST potentiometer for an output reading of –F.S. + 1LSB (See Table 2).

Table 1. 12-Bit Unipolar Output Coding

UNIPOLAR SCALE	INPUT CODING STRAIGHT BINARY	ANALOG OUTPUT		
		0 to 1V F.S.	0 to –5V F.S.	0 to –10V F.S.
–F.S. + 1LSB	1111 1111 1111	+0.9998V	–4.9988V	–9.9976V
–3/4F.S.	1100 0000 0000	+0.7500V	–3.7500V	–7.5000V
–1/2F.S.	1000 0000 0000	+0.5000V	–2.5000V	–5.0000V
–1/4F.S.	0100 0000 0000	+2.5000V	–1.2500V	–2.5000V
–1LSB	0000 0000 0001	+0.0002V	–0.0012V	–0.0024V
0	0000 0000 0000	0.0000V	0.0000V	0.0000V

Table 2. 12-Bit Bipolar Output Coding

BIPOLAR SCALE	INPUT CODING OFFSET BINARY	ANALOG OUTPUT			
		±0.5V F.S.	±2.5V F.S.	±5V F.S.	±10V F.S.
–F.S. + 1LSB	1111 1111 1111	+0.4998V	–2.4988V	–4.9976V	–9.9951V
–1/2F.S.	1100 0000 0000	+0.1250V	–1.2500V	–2.5000V	–5.0000V
–1LSB	1000 0000 0001	+0.0002V	–0.0012V	–0.0024V	–0.0049V
0	1000 0000 0000	0.0000V	0.0000V	0.0000V	0.0000V
+1/2F.S.	0100 0000 0000	–0.1250V	+1.2500V	+2.5000V	+5.0000V
+F.S. – 1LSB	0000 0000 0001	–0.4998V	+2.4988V	+4.9976V	+9.9951V
+F.S.	0000 0000 0000	–0.5000V	+2.5000V	+5.0000V	+10.0000V

Table 3. Programmable Output Range Pin Connections

OUTPUT VOLTAGE RANGE	FEEDBACK CONNECTIONS	CONNECT THESE PINS TOGETHER
0 to –5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 23
0 to –10V	PIN 19	PIN 20 to PIN 23
±2.5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 18
±5V	PIN 19	PIN 20 to PIN 18
±10V	PIN 17	PIN 20 to PIN 18

In all programmable output ranges, pin 18 connects to external operational amplifier inverting input.

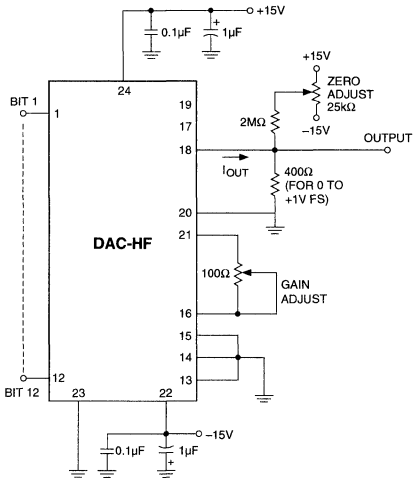


Figure 2. Unipolar Current Output Connections

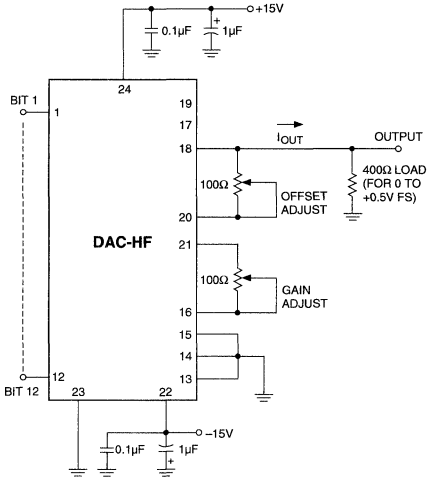
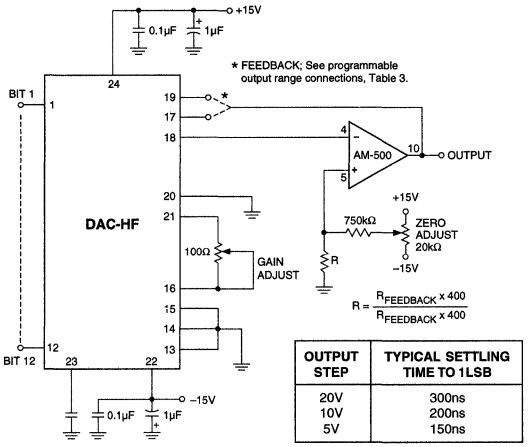


Figure 3. Bipolar Current Output Connections

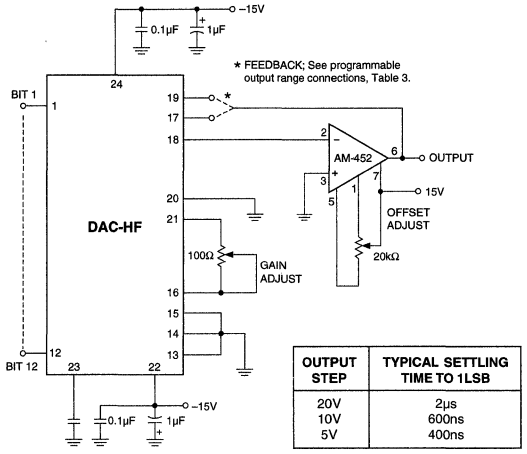
6

APPLICATIONS



OUTPUT STEP	TYPICAL SETTLING TIME TO 1LSB
20V	300ns
10V	200ns
5V	150ns

Figure 4. Unipolar Ultra-Fast Voltage Output Circuit



OUTPUT STEP	TYPICAL SETTLING TIME TO 1LSB
20V	2µs
10V	600ns
5V	400ns

Figure 5. Unipolar Fast Voltage Output Circuit

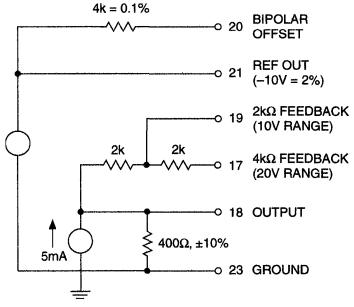
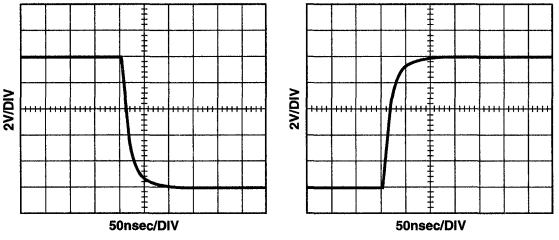


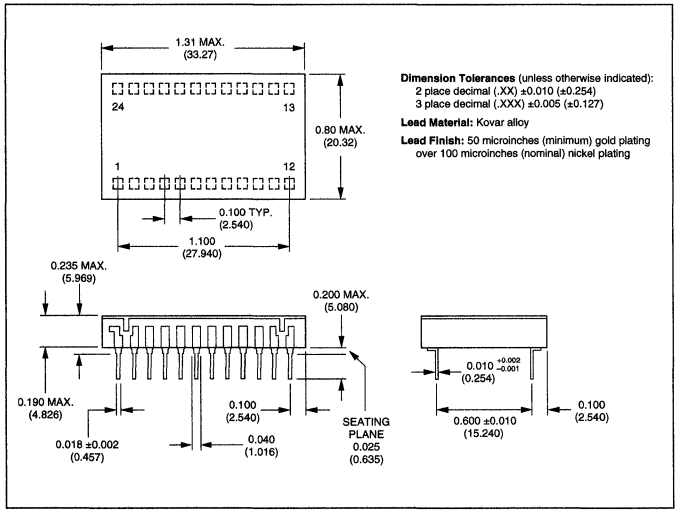
Figure 6. Equivalent Output Circuit



DAC-HF with AM-500, ±5V output full scale (10V) step

Figure 7. Voltage Output Waveforms

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	BITS
DAC-HF8BMC	0 to +70°C	8
DAC-HF8BMM	–55 to +125°C	8
DAC-HF8/883 ①	–55 to +125°C	8
DAC-HF10BMC	0 to +70°C	10
DAC-HF10BMM	–55 to +125°C	10
DAC-HF10/883 ①	–55 to +125°C	10
DAC-HF12BMC	0 to +70°C	12
DAC-HF12BMM	–55 to +125°C	12
DAC-HF12/883 ①	–55 to +125°C	12

① Contact DATEL for 883 product specification.

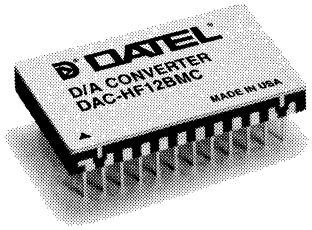
DATEL, Inc., 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For immediate assistance 800-233-2765

DATEL®
INNOVATION and EXCELLENCE

DAC-HK Series
High-Performance, 12-Bit DAC's with Input Registers

FEATURES

- **12-Bit resolution**
- **Integral nonlinearity error ±1/2LSB, max.**
- **Differential nonlinearity error ±3/4LSB, max.**
- **MIL-STD-883 high-reliability versions available**
- **Input register**
- **3µs fast settling time**
- **Guaranteed monotonicity over full temperature range**



GENERAL DESCRIPTION

The DAC-HK Series hybrid D/A converters are high-performance 12-bit devices with a fast settling voltage output. They incorporate a level-controlled input storage register and are specifically designed for systems applications such as data bus interfacing with computers. When the "load" input is high, data in the storage register is held, and when the load input is low, data is transferred through to the DAC. There are two basic models available by coding option: binary and two's complement. The output voltage ranges are externally pin-programmable and include: 0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V.

The DAC-HK Series contains a precision zener reference circuit. This eliminates code-dependent ground currents by routing current from the positive supply to the internal ground node as determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resistors, enhancing temperature performance. The excellent tracking of the resistors results in a differential nonlinearity tempco of ±2ppm/°C maximum. The temperature coefficient of gain is ±20ppm/°C maximum, and the tempco of zero is ±5ppm/°C maximum.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	24	REFERENCE OUT
2	BIT 2	23	GAIN ADJUST
3	BIT 3	22	+15V SUPPLY
4	BIT 4	21	GROUND
5	BIT 5	20	SUMMING JUNCTION
6	BIT 6	19	20V RANGE
7	BIT 7	18	10V RANGE
8	BIT 8	17	BIPOLAR OFFSET
9	BIT 9	16	LOAD
10	BIT 10	15	VOLTAGE OUTPUT
11	BIT 11	14	–15V SUPPLY
12	BIT 12 (LSB)	13	+5V SUPPLY

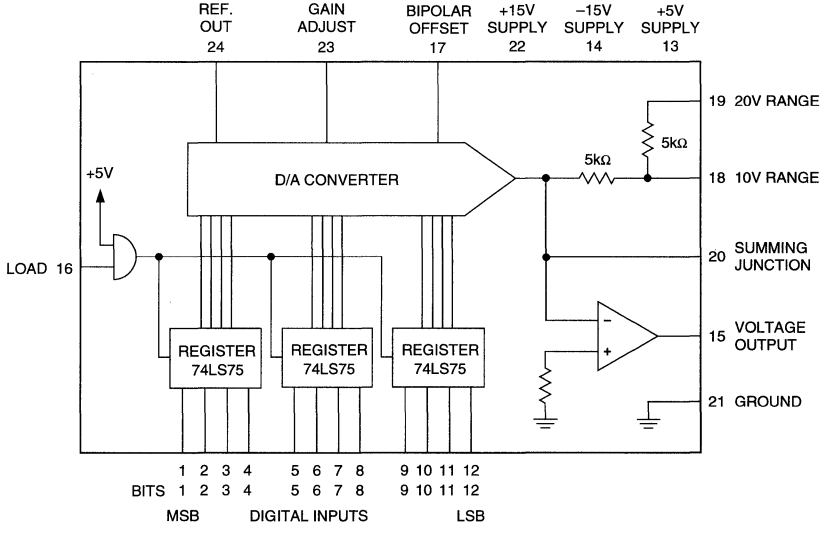


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Positive Supply, Pin 22	+18V
Negative Supply, Pin 14	–18V
Logic Supply, Pin 13	+5.25V
Digital Input Voltage, Pins 1–12 & 16	+5.5V
Output Current, Pin 15	±20mA
Lead Temperature (soldering, 10s)	300°C

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V and +5V supplies unless otherwise noted.)

INPUTS	
Resolution	12 bits
Coding, Unipolar Output	Straight binary
Coding, Bipolar Output	Offset binary, two's complement ①
Input Logic Level, Bit ON ("1")	+2.0V to +5.5V
Input Logic Level, Bit OFF ("0")	0V to +0.8V
Logic Loading	1 LSTTL load
Load Input ②	High ("1") = hold data Low ("0") = transfer data
Load Input Loading	3 LSTTL loads
PERFORMANCE ④	
Nonlinearity Error, max.	±1/2LSB
Differential Nonlinearity Error, max.	±3/4LSB
Gain Error, Before Trimming	±0.1% ③
Zero Error, Before Trimming	±0.1% of FSR ③
Gain Tempco, max.	±20ppm/°C
Zero Tempco, Unipolar, max.	±5ppm/°C of FSR
Offset Tempco, Bipolar, max.	±10ppm/°C of FSR
Diff. Nonlinearity Tempco, max.	±2ppm/°C of FSR
Monotonicity	Guaranteed over temperature
Settling Time, 5V Change	3µs
Settling Time, 10V Change	3µs
Settling Time, 20V Change	4µs
Settling Time, 1LSB Change	800ns
Slew Rate	±20V/µs
Power Supply Rejection	±0.002%FSR/%
OUTPUTS	
Output Voltage Ranges, Unipolar ⑤	0 to +5V, 0 to +10V
Output Voltage Ranges, Bipolar ⑤	±2.5V ±5V ±10V
Output Current	±5mA min.
Output Impedance	0.05 Ohm
POWER REQUIREMENTS	
Power Supply Voltages ⑥	+15V, ±0.5V at 15mA –15V, ±0.5V at 30mA +5V, ±0.25V at 65mA
PHYSICAL ENVIRONMENTAL	
Operating Temperature Range, Case	0°C to +70°C (BGC, BMC) –55°C to +125°C (BMM, 883)
Storage Temperature Range	–65°C to +125°C
Package Type	24-pin DDIP
Weight	0.22 ounces (6.3 grams)

Footnotes:

① For two's complement coding, order the "-2" model as described in Ordering Information.
② Logic levels are the same as for data inputs.
③ Initial errors are trimmable to zero. See Connection Diagram.
④ FSR is full scale range and is 10V for 0 to +10V output range, 20V for ±10V output range, etc.
⑤ By external pin connection.
⑥ For ±12V, +5V operation, contact factory.

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1µF (tantalum type) at the +15V, –15V and +5V supply pins. The capacitors should be connected as close to the pins as possible. In high RFI noise environments, these capacitors should be shunted with 0.01µF ceramic capacitors.
2. The analog, digital and power grounds should be separated from each other as close as possible to pin 21 where they all must come together.
3. The "load" control pin is a level-triggered input which causes the register to hold data with a high input and transfer data to the DAC with a low input.
4. A setup time of 50ns minimum must be allowed for the input data. The DAC output voltage begins to change when the register output changes.
5. If the reference output terminal (pin 24) is used, an operational amplifier in non-inverting mode should be used as a buffer. Current drawn from pin 24 should be limited to ±10µA in order not to affect the T.C. of the reference

CALIBRATION PROCEDURE

Select the desired output voltage range and connect the converter as shown in the Output Range Selection Table and the Connection Diagrams. Refer to the Coding Tables.

Unipolar Operation

1. **Zero Adjustment.** Set the input digital code to 0000 0000 0000 and adjust the ZERO ADJ. potentiometer to give 0.0000V output.
2. **Gain Adjustment.** Set the input digital code to 1111 1111 1111 (straight binary) and adjust the GAIN ADJ. potentiometer to give the full-scale output voltage shown in Table 1.

Bipolar Operation

1. **Offset Adjustment.** Set the digital input code to 0000 0000 0000 (offset binary) or 1000 0000 0000 (two's complement) and adjust the OFFSET ADJ. potentiometer to give the negative full-scale output voltage shown in Table 2.
2. **Gain Adjustment.** Set the digital input code to 1111 1111 1111 (offset binary) or 0111 1111 1111 (two's complement) and adjust the GAIN ADJ. potentiometer to give the positive full-scale output voltage shown in Table 2.

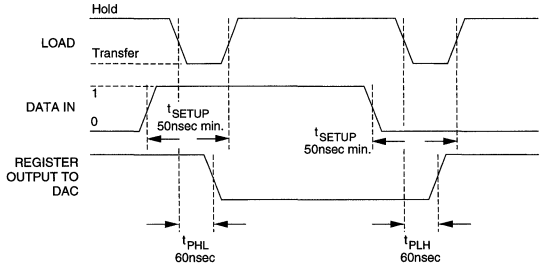


Figure 2. DAC-HK Timing

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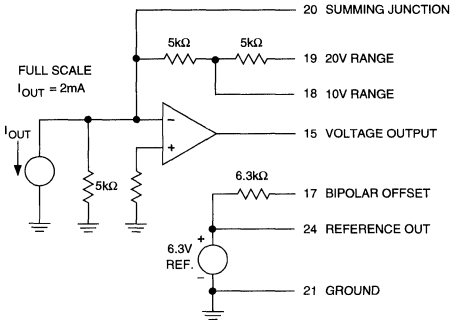

Figure 3. Output Circuit

CONNECTION DIAGRAMS

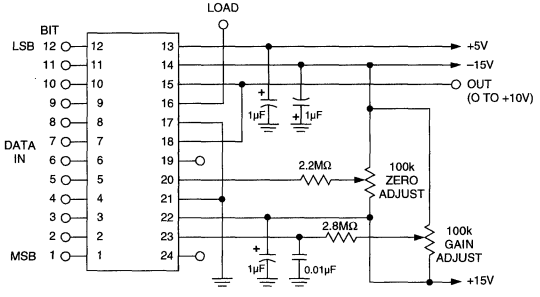

Figure 4. Unipolar Operation (0 to +10V)

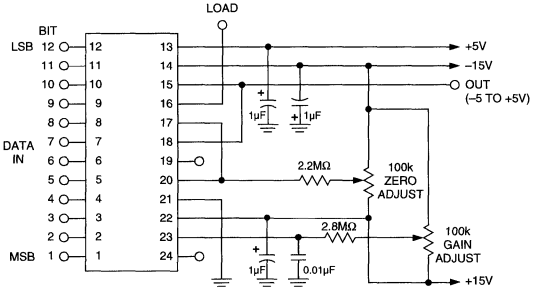

Figure 5. Bipolar Operation (±5V)

APPLICATIONS

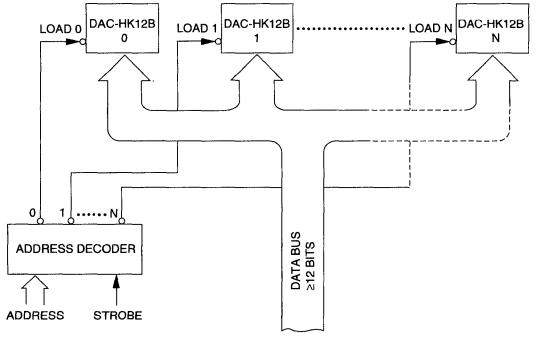

Figure 6. Interfacing to ≥12-Bit Data Bus

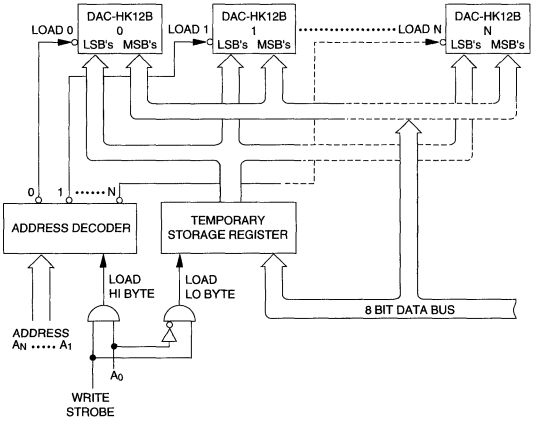

Figure 7. Interfacing to 8-Bit Data Bus

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CODING TABLES

Table 1. Unipolar Operation

STRAIGHT BINARY MSB		LSB	OUTPUT RANGES 0 TO +10V	0 TO +5V
1 1 1 1	1 1 1 1	1 1 1 1	+9.9976	+4.9988
1 1 0 0	0 0 0 0	0 0 0 0	+7.5000	+3.7500
1 0 0 0	0 0 0 0	0 0 0 0	+5.0000	+2.5000
0 1 0 0	0 0 0 0	0 0 0 0	+2.5000	+1.2500
0 0 0 0	0 0 0 0	0 0 0 1	+0.0024	+0.0012
0 0 0 0	0 0 0 0	0 0 0 0	0.0000	0.0000

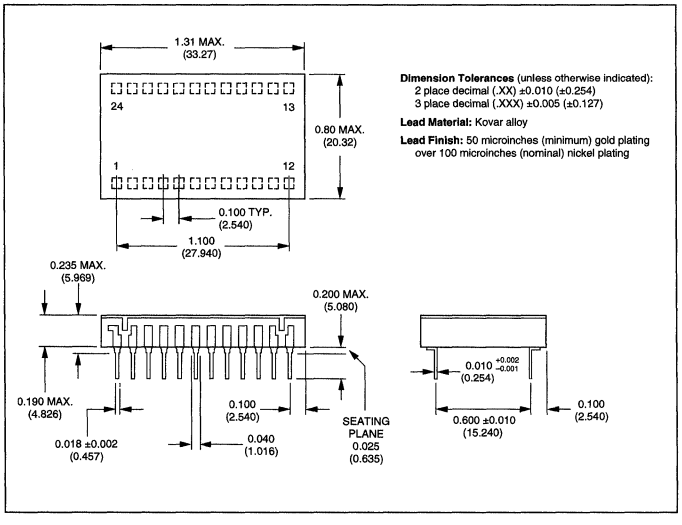
Table 2. Bipolar Operation

OFFSET BINARY MSB		LSB	TWO'S COMPLEMENT MSB		LSB	OUTPUT RANGES ±10V	±5V	±2.5V
1 1 1 1	1 1 1 1	1 1 1 1	0 1 1 1	1 1 1 1	1 1 1 1	+9.9951	+4.9976	+2.4988
1 1 0 0	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0	+5.0000	+2.5000	+1.2500
1 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0.0000	0.0000	0.0000
0 1 0 0	0 0 0 0	0 0 0 0	1 1 0 0	0 0 0 0	0 0 0 0	–5.0000	–2.5000	–1.2500
0 0 0 0	0 0 0 0	0 0 0 1	1 0 0 0	0 0 0 0	0 0 0 1	–9.9951	–4.9976	–2.4988
0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0	0 0 0 0	–10.0000	–5.0000	–2.5000

Table 3. Output Range Selection

RANGE	CONNECT THESE PINS TOGETHER		
±10V	15 & 19	17 & 20	
±5V	15 & 18	17 & 20	
±2.5V	15 & 18	17 & 20	19 & 20
+10V	15 & 18	17 & 21	
+5V	15 & 18	17 & 21	19 & 20

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
Binary Coding	
DAC-HK12BGC	0 to +70°C
DAC-HK12BMC	0 to +70°C
DAC-HK12BMM	–55 to +125°C
DAC-HKB/883	–55 to +125°C
Two's Complement Coding	
DAC-HK12BGC-2	0 to +70°C
DAC-HK12BMC-2	0 to +70°C
DAC-HK12BMM-2	–55 to +125°C
DAC-HKB-2/883	–55 to +125°C

The MIL-STD-883 units are available under DESC Drawing Number 5962-89528. Contact DATEL for 883 product specifications

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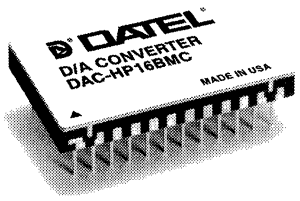
DATEL®
INNOVATION and EXCELLENCE

DAC-HP Series
16-Bit, High-Performance Digital-to-Analog Converters

FEATURES

- **16-Bit resolution**
- **3 Output voltage ranges**
- **±15ppm/°C maximum gain tempco**
- **Integral nonlinearity error ±0.003%FSR, max.**
- **14 Bits monotonic from +10°C to +40°C**
- **High-reliability MIL-STD–883 models available**



GENERAL DESCRIPTION

The DAC-HP Series are high-resolution hybrid digital-to-analog converters with voltage outputs. The Series has 16-bit binary resolution with ±0.003% integral nonlinearity. These units are self-contained, including a low-tempco Zener reference circuit and an output amplifier, in a miniature 24-pin DDIP package.

The DAC-HP Series offers both unipolar and bipolar modes with outputs of 0 to +10V and ±5V respectively. Devices with a bipolar output range of ±10V are also available and are designated with a "-1" suffix after the model designation. Input coding is complementary binary and complementary offset binary.

The DAC-HP design incorporates thin and thick-film hybrid technology. The design also includes an on-board amplifier and a precision Zener reference circuit. This eliminates code dependent ground currents by routing currents from the positive supply to the internal ground node as determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resistors, enhancing temperature stability and performance. The excellent tracking of the resistors results in tempcos for differential nonlinearity, gain and zero of ±2, ±15 and ±5ppm/°C max., respectively.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	24	REFERENCE OUT
2	BIT 2	23	+15V SUPPLY
3	BIT 3	22	GAIN ADJUST
4	BIT 4	21	SUMMING JUNCTION
5	BIT 5	20	GROUND
6	BIT 6	19	–15V SUPPLY
7	BIT 7	18	BIPOLAR OFFSET
8	BIT 8	17	OUTPUT
9	BIT 9	16	BIT 16 (LSB)
10	BIT 10	15	BIT 15
11	BIT 11	14	BIT 14
12	BIT 12	13	BIT 13

The DAC-HP Series operates off of ±15V supplies and offers models with temperature performance covering the 0 to +70°C commercial or –55 to +125°C military temperature ranges. High reliability MIL-STD-883 versions are also available.

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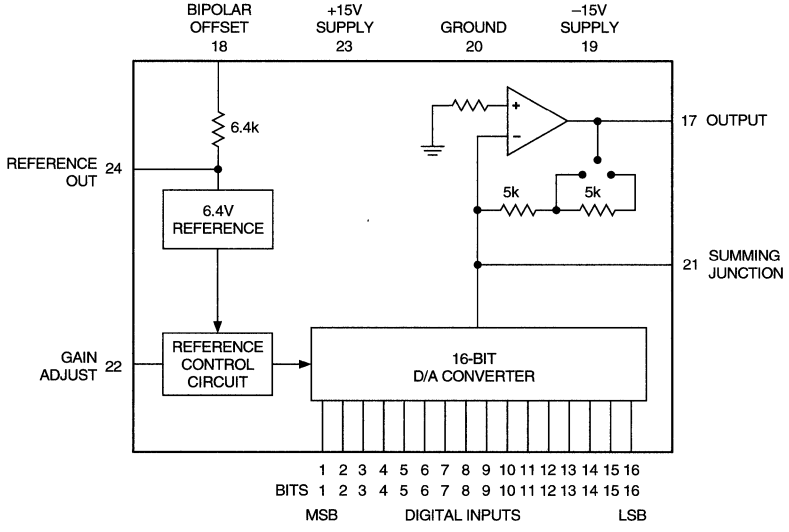


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Positive Supply, Pin 23	+18V
Negative Supply, Pin 19	–18V
Digital Input Voltage, Pins 1–16	+5.5V
Output Current, Pin 17	±20mA
Lead Temperature (soldering, 10s)	300°C

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V supplies unless otherwise noted.)

INPUTS	
Resolution	16 bits
Coding, Unipolar Output	Complementary binary
Coding, Bipolar Output	Complementary offset binary
Input Logic Level, Bit ON ("0") ①	0V to +0.8V at –1mA
Input Logic Level, Bit OFF ("1") ①	+2.4V to +5.5V at +40µA
Logic Loading	1 TTL load
PERFORMANCE ②	
Nonlinearity Error, max.	±0.003% of FSR
Monotonicity, +10°C to +40°C	14 bits
Gain Error, Before Trimming	±0.1%
Zero Error, Before Trimming	±0.1% of FSR
Gain Tempco, max. ③	±15ppm/°C of FSR
Gain Tempco, max. BGC	±20ppm/°C of FSR
Zero Tempco, Unipolar, max.	±5ppm/°C of FSR
Offset Tempco, Bipolar, max.	±8ppm/°C of FSR
Differential Nonlinearity Tempco, max.	±2ppm/°C of FSR
Settling Time, 10V Change ④	15µs
Slew Rate	±20V/µs
Power Supply Rejection	±0.003%FSR/% ⑤
OUTPUTS	
Output Voltage Range, Unipolar ⑥	0 to +10V
Output Voltage Range, Bipolar	±5V
Output Voltage Range, "–1" Suffix	±10V
Output Current, min. ⑦	±5mA
Output Impedance	0.05Ω
POWER REQUIREMENTS	
Quiescent, All Bits High	+15V, ±0.5V at 20mA –15V, ±0.5V at 25mA ±12V operation ⑧
PHYSICAL ENVIRONMENTAL	
Operating Temperature Range, Case	0°C to +70°C (BMC, BGC) –55°C to +125°C (BMM, 883)
Storage Temperature Range	–65°C to +150°C
Package Type	24-pin DDIP
Weight	0.22 ounces (6.3 grams)

Footnotes

① Drive from TTL output with only the DAC-HP as load.
② FSR is full-scale range and is 10V for 0 to +10V or –5V to +5V outputs, 20V for ±10V output, etc
③ For all models except DAC-HP16BGC
④ Settling to ±0.5mV
⑤ ±0.006%FSR/% maximum over full military temperature range for MM and 883 models.
⑥ Unipolar output range for suffix "–1" models, 0 to +10V, is reached at the 1/2 scale point.
⑦ Pin 17.
⑧ For ±12V operation, consult factory.

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1µF (tantalum type) at the +15V and –15V supply pins. The capacitors should be connected as close to the pins as possible. In high-frequency noise environments, an additional 0.01µF ceramic capacitor should be used in parallel with each tantalum bypass.
2. When laying out the circuit board for this device, isolate the analog, digital and power grounds as much as possible from each other before joining them at pin 20.
3. If the reference output (pin 24) is used, it must be buffered by an operational amplifier in the noninverting mode. See Figure 2. Current drawn from pin 24 should be limited to ±10µA in order that the temperature coefficient of the reference circuit not be affected. This is sufficient current for the bias current requirements of most popular operational amplifier types.

CALIBRATION PROCEDURE

For bipolar operation, connect Bipolar Offset (pin 18) to Summing Junction (pin 21). For unipolar operation, connect Bipolar Offset (pin 18) to Ground (pin 20). In making the following adjustments, refer to the Coding Tables and Connection Diagrams.

1. **Zero Adjustment.** Set the input digital code to 1111 1111 1111 1111 and adjust the ZERO ADJ. potentiometer to give 0.00000V output for unipolar operation or –FS output for bipolar operation.
2. **Gain Adjustment.** Set the input digital code to 0000 0000 0000 0000 and adjust the GAIN ADJ. potentiometer to give +FS – 1LSB output for either unipolar or bipolar operation.

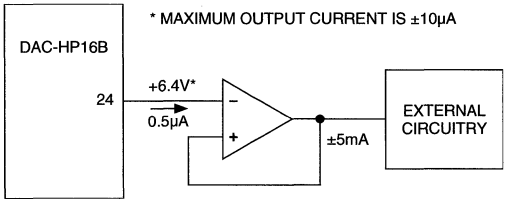


Figure 2. Use of Reference Output

CODING TABLES

Table 1. Bipolar Output — Complementary Offset Binary

INPUT CODE MSB			LSB	SCALE	OUTPUT VOLTAGE	OUTPUT VOLTAGE SUFFIX "-1"
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	+FS – 1LSB	+4.99985V	+9.99969V
0 0 1 1	1 1 1 1	1 1 1 1	1 1 1 1	+1/2FS	+2.50000	+5.00000
0 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0	0.00000	0.00000
1 0 1 1	1 1 1 1	1 1 1 1	1 1 1 1	–1/2FS	–2.50000	–5.00000
1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 0	–FS + 1LSB	–4.99985	–9.99969
1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	–FS	–5.00000V	–10.00000V

Table 2. Unipolar Output — Complementary Binary

INPUT CODE MSB			LSB	SCALE	OUTPUT VOLTAGE
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	+FS – 1LSB	+9.99985V
0 0 1 1	1 1 1 1	1 1 1 1	1 1 1 1	+3/4FS	+7.50000
0 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	+1/2FS	+5.00000
1 0 1 1	1 1 1 1	1 1 1 1	1 1 1 1	+1/4FS	+2.50000
1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 0	+1LSB	+153µV
1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0	0

CONNECTION DIAGRAMS

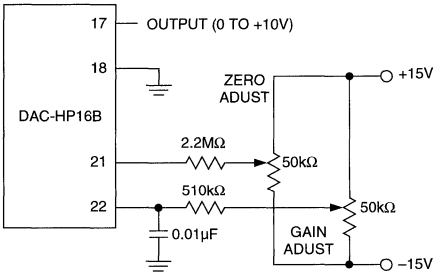


Figure 3. Unipolar Operations

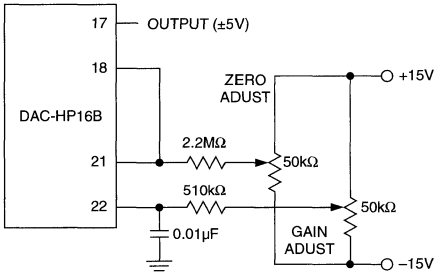


Figure 4. Bipolar Operations

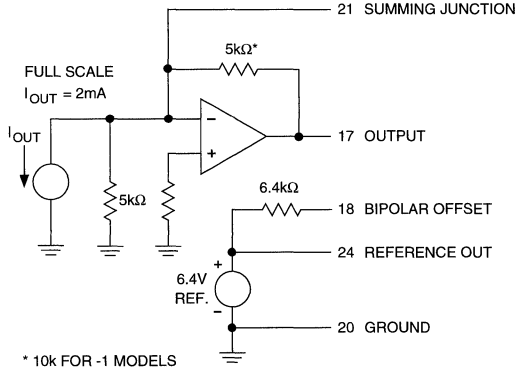
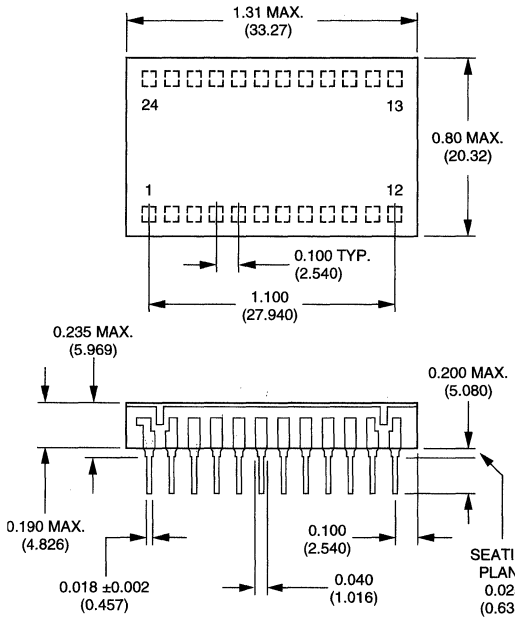


Figure 5. Output Circuit

MECHANICAL DIMENSIONS Inches (mm)



Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
DAC-HP16BGC	0 to +70°C
DAC-HP16BMC	0 to +70°C
DAC-HP16BMM	–55 to +125°C
DAC-HPB/883	–55 to +125°C
DAC-HP16BGC-1	0 to +70°C
DAC-HP16BMC-1	0 to +70°C
DAC-HP16BMM-1	–55 to +125°C
DAC-HPB-1/883	–55 to +125°C

The MIL-STD-883 units are available under DESC Drawing Number 5962-89531. Contact DATEL for 883 product specifications.

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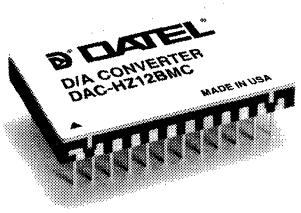
DAC-HZ Series
12-Bit, Industry-Standard Digital-to-Analog Converters

FEATURES

- **12-Bit binary and 3-digit BCD models**
- **7 Output ranges**
- **3µs V_{OUT} settling time**
  300ns I_{OUT} settling time
- **Guaranteed monotonicity over full temperature range**
- **Integral nonlinearity ±1/2LSB (binary) and ±1/4LSB (BCD), maximum**
- **Differential nonlinearity ±3/4LSB (binary) and ±1/4LSB (BCD), maximum**
- **High-reliability QL versions available**



GENERAL DESCRIPTION

The DAC-HZ Series are high-performance, monolithic, 12-bit binary and 3-digit BCD, digital-to-analog converters. The DAC-HZ Series are complete and self-contained with a precision internal reference and fast output operational amplifier. Pin programmable output voltage and current ranges are provided for a high degree of application flexibility; the binary versions offer 5 output voltage ranges and two current ranges while the BCD models offer 3 and 1 output ranges, respectively.

The DAC-HZ Series contains a precision embedded Zener reference circuit. This eliminates code-dependent ground currents by routing current from the positive supply to the internal ground node as determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resistors, enhancing temperature performance. The excellent tracking of the resistors results in temperature coefficients for differential nonlinearity, zero and gain of ±2, ±3 and ±20ppm/°C maximum, respectively.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	24	REFERENCE OUT
2	BIT 2	23	GAIN ADJUST
3	BIT 3	22	+15V SUPPLY
4	BIT 4	21	GROUND
5	BIT 5	20	CURRENT OUTPUT
6	BIT 6	19	20V RANGE
7	BIT 7	18	10V RANGE
8	BIT 8	17	BIPOLAR OFFSET
9	BIT 9	16	REFERENCE IN
10	BIT 10	15	VOLTAGE OUTPUT
11	BIT 11	14	–15V SUPPLY
12	BIT 12 (LSB)	13	NO CONNECTION

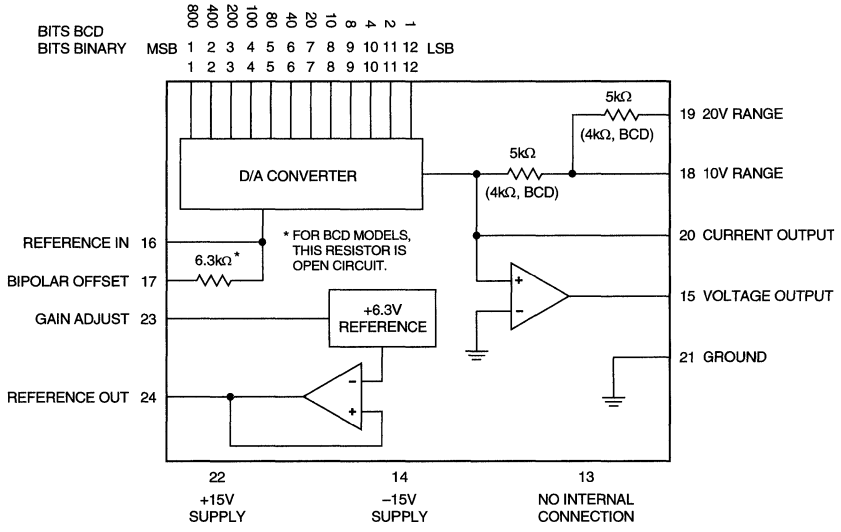


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Positive Supply, Pin 22	+18V
Negative Supply, Pin 14	–18V
Digital Input Voltage, Pins 1–12	+5.5V
Output Current, Pin 15	±20mA
Lead Temperature (soldering, 10s)	300°C

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V supplies unless otherwise noted.)

INPUTS	DAC-HZ12B (BINARY)	DAC-HZ12D (BCD)
Resolution	12 binary bits	3 BCD digits
Coding, Unipolar Output	Comp. binary	Comp. BCD
Coding, Bipolar Output	Comp. off. binary	—
Input Logic Level, Bit ON ("0")	0V to +0.8V at –1mA	
Input Logic Level, Bit OFF ("1")	+2.4V to +5.5V at +40µA	
Logic Loading	1 TTL load	
PERFORMANCE ①		
Voltage Output Nonlinearity	±1/2LSB max.	±1/4LSB max.
Differential Nonlinearity	±3/4LSB max	±1/4LSB max.
Gain Error, Before Trimming	±0.1% ②	*
Zero Error, Before Trimming	±0.1% of FSR ②	*
Gain Tempco, maximum	±20ppm/°C	*
Zero Tempco, Unipolar, max.	±3ppm/°C of FSR	*
Offset Tempco, Bipolar, max.	±10ppm/°C of FSR	*
Diff. Nonlinearity Tempco, max.	±2ppm/°C of FSR	*
Monotonicity	Over oper. temp. range	*
Settling Time, Iout to ±1/2LSB ③	300ns	*
Settling Time, Vout to ±1/2LSB	3µs ④	*
Slew Rate	±10V/µs	*
Power Supply Rejection	±0.006%FSR/%Sup.	*
OUTPUTS		
Output Current, Unipolar	0 to –2mA, ±20%	0 to –1.25mA, ±10%
Output Current, Bipolar	±1mA, ±20%	—
Compliance Voltage, Iout	±2.5V	*
Output Impedance, Iout, Unipolar	2kΩ	*
Output Impedance, Iout, Bipolar	2kΩ	—
Output Voltage Ranges, Unipolar	0 to +5V 0 to +10V	0 to +2.5V 0 to +5V 0 to +10V
Output Voltage Ranges, Bipolar	±2.5V ±5V ±10V	— — —
Output Current, Vout	±5mA min.	*
Output Impedance, Vout	0.05Ω	*
POWER REQUIREMENTS		
Power Supply Voltages	+15V, ±0.5V at 16mA –15V, ±0.5V at 20mA ±12V operation ⑤	
Power Dissipation, maximum	500mW	
PHYSICAL ENVIRONMENTAL		
Operating Temp. Ranges, Case	0°C to +70° and –55°C to +125°C	
Storage Temp. Range	–65°C to +150°C	
Thermal Impedance		
θjc	7.4°C/W	
θca	36.6°C/W	
Package Type	24-pin DDIP	
Weight	0.22 ounces (6.3 grams)	

* Specifications same as first column.
— No equivalent specifications

Footnotes

① FSR is full-scale range and is 10V for 0 to +10V or –5V to +5V outputs, 20V for ±10V output, etc.
② Initial gain and offset errors are trimmable to zero. See Connection Diagrams.
③ Current output mode.
④ For 2.5kΩ or 5kΩ feedback. For 10kΩ feedback, the settling time is 4µs.
⑤ For ±12V operation of binary models, contact factory.

TECHNICAL NOTES

1. The DAC-HZ12 Series converters are designed and factory calibrated to give ±1/2LSB linearity (binary version) and ±1/4LSB linearity (BCD version) with respect to a straight line between end points. This means that if zero and full scale are exactly adjusted externally, the relative accuracy will be ±1/2LSB (±1/4LSB, BCD version) everywhere over the full output range without any additional adjustments.
2. These converters must be operated with local supply by-pass capacitors from +15V to ground and –15V to ground. Tantalum type capacitors of 1µF are recommended and should be mounted as close as possible to the converter. If the converters are used in a high-frequency noise environment, a 0.01µF ceramic capacitor should be used across each tantalum capacitor.
3. When operating in the current output mode, the equivalent internal current source of 2mA (1.25mA, BCD) must drive both the internal source resistances and the external load resistor. A 300ns output settling time is achieved for the voltage across a 100Ω load resistor; for higher value resistors the settling time becomes longer due to the output capacitance of the converter. For fastest possible voltage output for a large transition, an external fast-settling amplifier such as DATEL's AM-500 should be used in the inverting mode. Settling time of less than 1µs can be achieved. See application diagram.

CALIBRATION PROCEDURE

1. Select the desired output range and connect the converter as shown in the Output Range Selection tables and the connection diagrams.
2. To calibrate, refer to the coding tables. Note that complementary coding is used.
3. **Zero and Offset Adjustments**
   For unipolar operation set all digital inputs to "1" (+2.0 to +5.5V) and adjust the ZERO ADJ. potentiometer for zero output voltage or current. For bipolar operation set all digital inputs to "1" and adjust the OFFSET ADJ. potentiometer for the negative full scale (for voltage out) or positive full scale (for current out) output value shown in the coding table.
4. **Gain Adjustment**
   Set all digital inputs to "0" (0V to +0.8V) and adjust the GAIN ADJ. potentiometer for the positive full scale (for voltage out) or negative full scale (for current out) output value shown in the coding table.

OUTPUT RANGE SELECTION TABLES

Table 1. DAC-HZ12B Binary Output Range Selection

V_{OUT} RANGE	CONNECT THESE PINS TOGETHER			
±10V	15 & 19	17 & 20	—	16 & 24
±5V	15 & 18	17 & 20	—	16 & 24
±2.5V	15 & 18	17 & 20	19 & 20	16 & 24
+10V	15 & 18	17 & 21	—	16 & 24
+5V	15 & 18	17 & 21	19 & 20	16 & 24
±1mA	—	17 & 20	—	16 & 24
–2mA	—	17 & 21	—	16 & 24

Voltage output is at pin 15; current output is at pin 20.

Table 2. DAC-HZ12D BCD Output Range Selection

V_{OUT} RANGE	CONNECT THESE PINS TOGETHER			
+10V	15 & 19	17 & 21	—	16 & 24
+5V	15 & 18	17 & 21	—	16 & 24
+2.5V	15 & 18	17 & 21	19 & 20	16 & 24
–1.25mA	—	17 & 21	—	16 & 24

Voltage output is at pin 15; current output is at pin 20.

UNIPOLAR OUTPUT CODING TABLES

Table 3. Unipolar Output, Complementary Binary

BINARY INPUT CODE			UNIPOLAR OUTPUT RANGES		
MSB		LSB	0 to +10V	0 to +5V	0 to –2mA
0000	0000	0000	+9.9976V	+4.9988V	–1.9995
0011	1111	1111	+7.5000	+3.7500	–1.5000
0111	1111	1111	+5.0000	+2.5000	–1.0000
1011	1111	1111	+2.5000	+1.2500	–0.5000
1111	1111	1110	+0.0024	+0.0012	–0.0005
1111	1111	1111	0.0000	0.0000	0.0000

Table 4. Unipolar Output, Complementary BCD

BCD INPUT CODE			UNIPOLAR OUTPUT RANGES			
MSB		LSB	0 to +10 VOLTS	0 to +5 VOLTS	0 to +2.5 VOLTS	0 to –2 mA
0110	0110	0110	+9.990	+4.995	+2.498	–1.2488
1000	1010	1111	+7.500	+3.750	+1.875	–0.9375
1010	1111	1111	+5.000	+2.5000	+1.250	–0.6250
1101	1010	1111	+2.5000	+1.250	+0.625	–0.3125
1111	1111	1110	+0.0100	+0.005	+0.003	–0.0013
1111	1111	1111	0.0000	0.0000	0.0000	0.0000

BIPOLAR OUTPUT CODING TABLE

Table 5. Bipolar Output, Complementary Offset Binary

INPUT CODE			BIPOLAR OUTPUT RANGES			
MSB		LSB	±10V	±5V	±2.5V	±1mA
0000	0000	0000	+9.9951	+4.9976	+2.4988	–0.9995
0011	1111	1111	+5.0000	+2.5000	+1.2500	–0.5000
0111	1111	1111	0.0000	0.0000	0.0000	0.0000
1011	1111	1111	–5.0000	–2.5000	–1.2500	+0.5000
1111	1111	1110	–9.9951	–4.9976	–2.4988	+0.9995
1111	1111	1111	–10.0000	–5.0000	–2.5000	+1.0000

CONNECTION DIAGRAMS

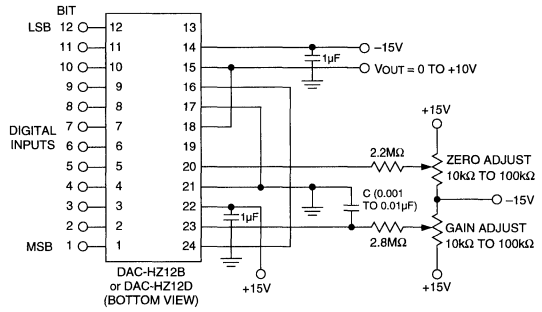


Figure 2. Unipolar Voltage Output Connections

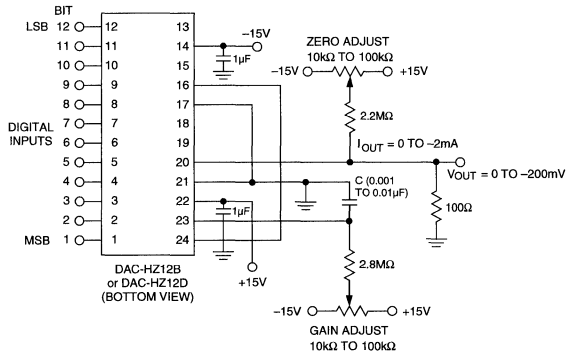
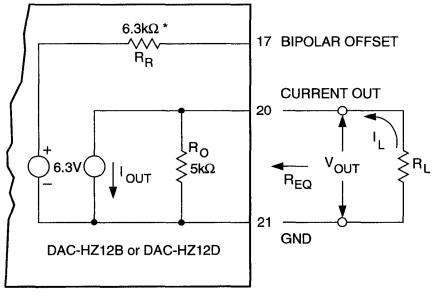


Figure 3. Unipolar Current Output Connections



*This resistor is open circuit for BCD models

V_{OUT} = ±2.5V Maximum
(Output compliance voltage)

$R_{EQ} = R_O$ = 5k for unipolar operation

$R_{EQ} = R_R \parallel R_O$ = 2.8k for bipolar operation

I_{OUT} = 2mA binary
= 1.25mA BCD

Figure 4. Equivalent Current Mode Output Circuit

6

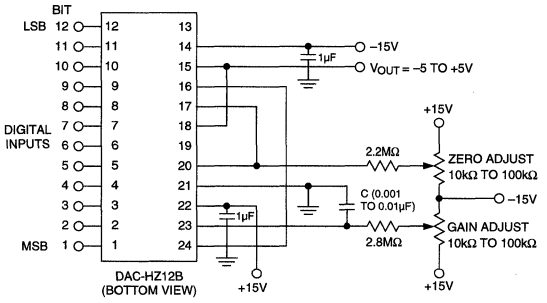


Figure 5. Bipolar Voltage Output Connections

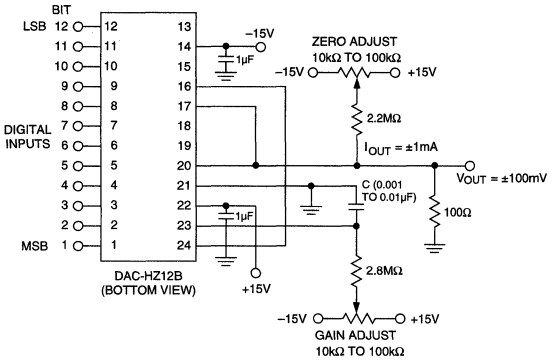
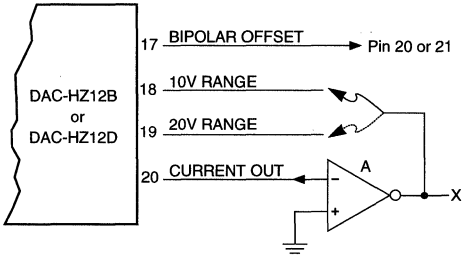


Figure 6. Bipolar Current Output Connections

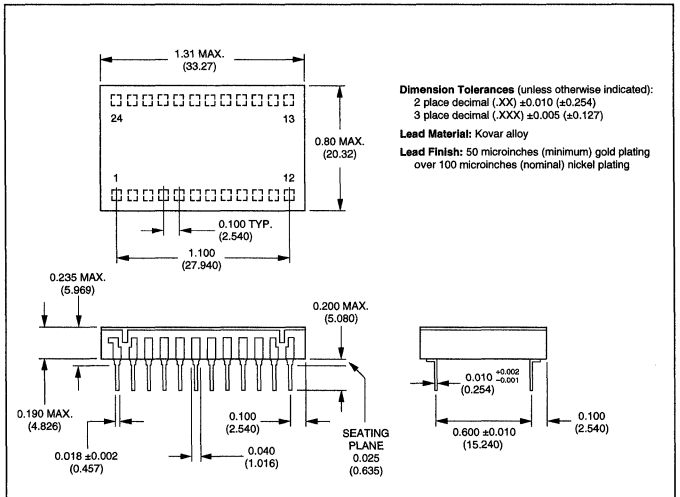


A = External high-speed inverting op amp; use DATEL's AM-500 for less than 1µsec output settling.

Refer to the output range selection tables, Tables 1 and 2. Wherever pin 15 appears, use pin X of the external amplifier and scale as desired.

Figure 7. Using a High-Speed External Op Amp for Faster Settling

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	OUTPUT CODING
DAC-HZ12BGC	0 to +70°C	Binary
DAC-HZ12BMC	0 to +70°C	Binary
DAC-HZ12BMM	–55 to +125°C	Binary
DAC-HZ12BMM-QL	–55 to +125°C	Binary
DAC-HZ12DGC	0 to +70°C	BCD
DAC-HZ12DMC	0 to +70°C	BCD
DAC-HZ12DMM	–55 to +125°C	BCD
DAC-HZ12DMM-QL	–55 to +125°C	BCD

Contact DATEL for information concerning our QL high-reliability screening program.

Operational & Instrumentation Amplifiers

Table of Contents

Selection Guide

Operational Amplifiers

Model	Open Loop Gain (000)	Gain Bandwidth Product (MHz)	Slew Rate (V/µsec)	Input Offset Voltage (mV)	Offset Voltage Drift (µV/°C)	Input Bias Current (nA)	Output (±V@±mA)	Power Dissipation (±V@±mA)	Page
AM-500	1000	130	±1000	±0.5	±1	±1	10/50	15/22	**7-7**
AM-1435	100	1000	±300	±2	±5	±20µA	7/14	15/22	**7-3**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.

Instrumentation Amplifiers

Model	Input Impedance ($10^{12}\Omega$)	Slew Rate (V/µsec)	Settling Time, G=1 (µsec)	Gain	Gain Accuracy (%, Max.)	Gain Nonlinearity (%, Max.)	Input Offset Voltage (±mV, Max.)	Output (±V@±mA)	Power Dissipation (±V@±mA)	Page
AM-551 ①	1 ②	±23	3	1-1000	±0.04	±0.01	1 x gain	11/5	15/27	**7-10**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① 2-stage design. Front-end gain is resistor programmable. Back-end gain of 1 or 10 is pin selectable.
② CMV = ±11V, CMRR = 100dB.

For literature or technical assistance

800-233-2765

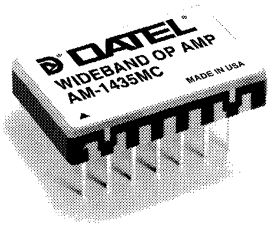
or contact your local DATEL Sales Office or Representative

DATEL®
INNOVATION and EXCELLENCE

AM-1435
Ultra-Fast, Wideband Operational Amplifiers

FEATURES

- **70 nanosecond settling to ±0.01%**
- **1GHz gain bandwidth product**
- **100dB open loop gain**
- **80dB minimum CMRR**
- **–55 to +125°C operation**
- **Industry standard**



GENERAL DESCRIPTION

DATEL's AM-1435 is an ultrafast settling, wideband operational amplifier. Utilizing precision thin-film hybrid construction and differential input operational amplifier design techniques, the AM-1435 achieves a settling time of only 70 nanoseconds for a 10V step to ±0.01% accuracy. High-speed performance is optimized with high open-loop gain, flat frequency response beyond 10kHz, and a roll-off of 6dB/octave to beyond 100MHz. Typically, gain bandwidth product is 1GHz, and slew rate is ±300V/microsecond.

AM-1435's dc characteristics include a dc open loop gain of 100dB, 1MΩ input impedance, and an initial input offset voltage of only ±2mV. Input offset voltage drift is typically ±5µV/°C. Also featured is a minimum common mode rejection ratio of 80dB and full power frequency of 8MHz.

The AM-1435 is designed specifically for applications requiring high accuracy in the amplification of complex wideband waveforms. Such applications include radar and sonar signal processing, video instrumentation, ultrafast A/D and D/A converters and sample-hold amplifiers.

Power supply requirements are ±15V at 30mA maximum quiescent current. Models are specified for operation over the commercial (0 to +70°C) and military (–55 to +125°C) temperature ranges. A high-reliability version manufactured and screened to DATEL's QL screening program is also available. The package is a 14-pin ceramic DIP.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OPTIONAL BYPASS CAPACITOR
2	OUTPUT
3	COMPENSATION CAPACITOR
4	+15V SUPPLY (+V_S)
5	OFFSET ADJUST
6	OFFSET ADJUST
7	–INPUT
8	+INPUT
9	N.C.
10	N.C.
11	N.C.
12	–15V SUPPLY (–V_S)
13	OUTPUT CURRENT SINK
14	COMMON

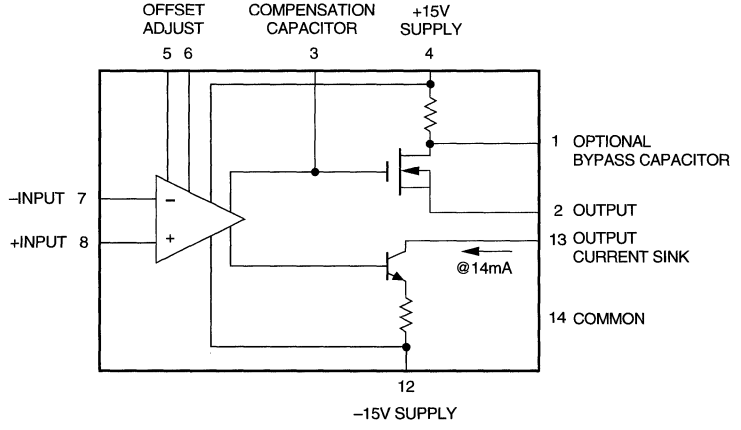


Figure 1. Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V supplies, unless otherwise noted.)

INPUT	MIN.	TYP.	MAX.	UNITS
Differential Between Inputs	—	—	±4	Volts
Common Mode Voltage Range ①	±7	±8.5	—	Volts
Common Mode Rejection Ratio				
1MHz	—	70	—	dB
DC	80	100	—	dB
Input Impedance				
Common Mode	—	1 ‖ 2	—	MΩ ‖ pF
Differential Mode	—	2.5 ‖ 2	—	kΩ ‖ pF
Input Bias Current	—	±20	40	µA
Input Offset Current	—	±0.3	—	µA
Input Offset Voltage ②	—	±2	±5	mV
PERFORMANCE				
DC Open Loop Gain ③	90	100	—	dB
Input Offset Voltage Drift	—	±5	±25	µV/°C
Input Bias Current Drift	—	±50	±100	nA/°C
Input Offset Current Drift	—	±2	—	nA/°C
Input Voltage Noise				
0.01Hz to 10Hz	—	15	—	µVp-p
100Hz to 10kHz	—	1.6	—	µVrms
10Hz to 1MHz	—	5.2	—	µVrms
Input Current Noise ④				
0.01Hz to 10Hz	—	2.5	—	nAp-p
100Hz to 10kHz	—	2.5	—	nArms
10Hz to 1MHz	—	3.5	—	nArms
Power Supply Rejection Ratio	—	±0.15	—	mV/V
DYNAMIC CHARACTERISTICS				
Gain Bandwidth Product	700	1000	—	MHz
Unity Gain Bandwidth	—	150	—	MHz
Full Power Frequency ⑤	8	10	—	MHz
Settling Time				
10V to ±0.025% ⑥	—	60	75	ns
10V to ±0.01% ⑥	—	70	—	ns
5V to ±1.0%	—	25	—	ns
5V to ±0.1%	—	40	60	ns
1V to ±1.0%	—	10	—	ns
1V to ±0.1%	—	20	—	ns
Slew Rate ⑤	±250	±300	—	V/µs
Overshoot	—	1	—	%
Propagation Delay	—	5	—	ns
Rise Time (10V step)	—	40	—	ns
Overload Recovery Time	—	50	—	ns
OUTPUT				
Output Voltage ③	±5	±7	—	Volts
Output Current ③	±10	±14	—	mA
Stable Capacitative Load ⑦	—	1000	—	pF
POWER REQUIREMENTS				
Rated Supply Voltages	±12	±15	±16	Volts
Quiescent Current	—	±22	±30	mA

Footnotes:

① Specified for dc linear operation. Common mode voltage range prior to fault condition is ±10V maximum.

② Adjustable to zero.

③ R_L = 500Ω.

④ Referred to input.

⑤ C1 = 0.5pF.

⑥ C1 = 1pF.

⑦ C1 = 3pF, noise gain >2.

⑧ Requires 18°C/W heat sink above +85°C.

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
AM-1435MC	0	—	+70	°C
AM-1435MM, MM-QL ⑧	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type	14-pin, metal-sealed, ceramic DIP			

TECHNICAL NOTES

1. The use of good high-frequency circuit board layout techniques is required for rated performance. The extensive use of a ground plane for all common connections is recommended. Lead lengths should be kept to a minimum with point-to-point connections wired directly to the amplifier pins. 1µF tantalum bypass capacitors should be used at the ±15V supply pins.
2. Operation of the AM-1435MM and MM-QL over the +85 to +125°C temperature range requires additional thermal dissipation to achieve rated performance. Use of an 18°C/W heat sink is recommended.
3. No input protection is provided so as to maximize frequency response. As a result, several precautions must be observed. Do not apply the positive supply voltage before the negative supply. Do not apply signals to either input prior to power-up. If frequency response is not critical, installation of an external input-protection circuit is recommended.
4. A 1µF bypass capacitor (C4) connected from OPTIONAL BYPASS CAPACITOR (pin 1) to COMMON (pin 14) may be required to inhibit output oscillation when driving capacitive loads.
5. To ensure stable operation when the noise gain is less than 10, a 2pF compensation capacitor (C1) must be connected between pins 3 and 7. The value of the compensation capacitor may be application sensitive.
6. The AM-1435 is a prime choice as a current-to-voltage converter due to its excellent E_{OS} and I_{OS} temperature coefficient ratings. Input bias currents are easily compensated by adding a resistor from pin 8 to ground, which is equal to the parallel combination of the feedback resistor and input impedance.

ABSOLUTE MAXIMUM RATINGS, ALL MODELS

Positive Supply, Pin 4	+18V
Negative Supply, Pin 12	–18V
Lead Temperature (soldering, 10s)	300°C

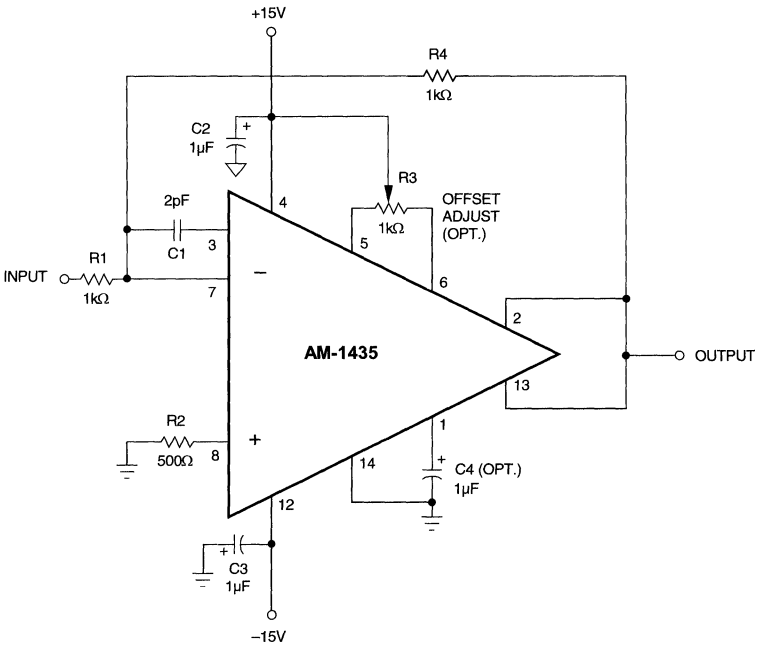


Figure 2. Typical Connection Diagram

TYPICAL CONNECTION AND COMPENSATION

The typical connection diagram (above) shows the AM-1435 in a unity-gain inverting configuration. When used in any conventional operational-amplifier configuration, the AM-1435 (as a non-inverting amplifier) requires a noise gain of at least two (noise gain = 1 + R4/R1).

The 2pF compensation capacitor, C1, at pin 3 is required for stable operation when the noise gain is less than 10. Compensation for bias current is provided by R2 and its value is determined by the formula:

$$R2 = \frac{(R1) \times (R4)}{R1 + R4}$$

The offset adjust potentiometer R3 and the compensation capacitor C4 are optional. Note, however, that C4 should be implemented when driving capacitive loads to prevent oscillation of the output stage.

Operation of the AM-1435 at low impedances requires careful attention to include the feedback resistor as a part of the total output load.

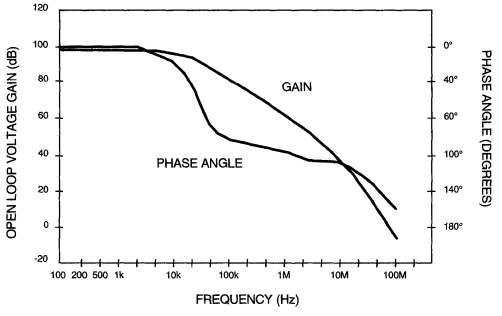


Figure 3. Gain and Phase vs. Frequency (Uncompensated)

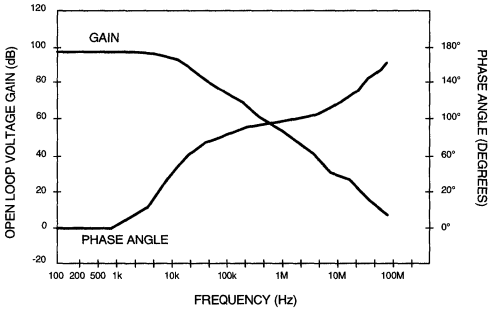


Figure 4. Gain and Phase vs. Frequency (Compensated 2pF)

PERFORMANCE CHARTS

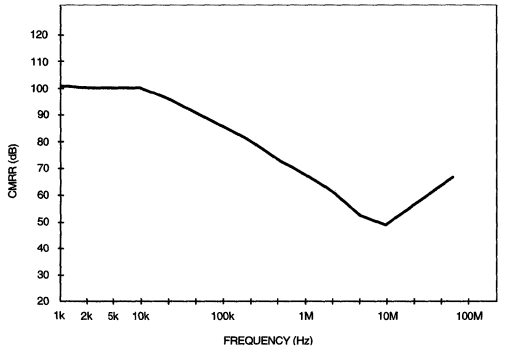


Figure 5. CMRR vs. Frequency

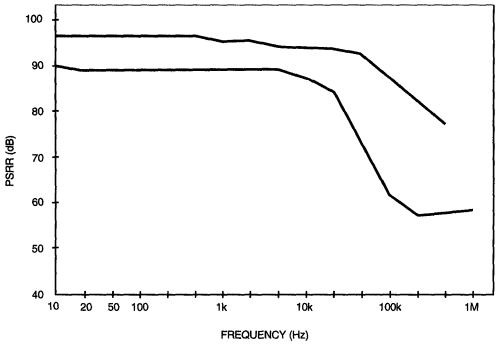
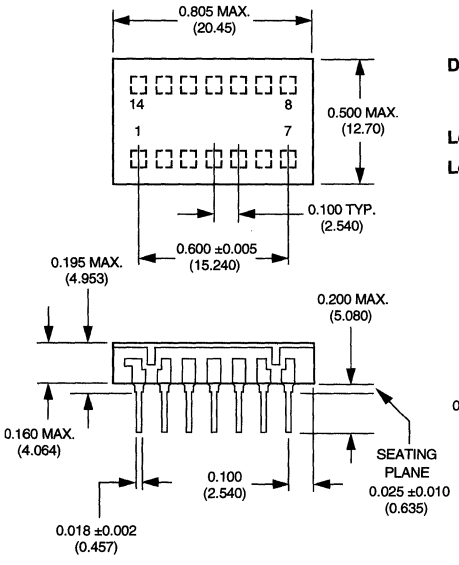


Figure 6. PSRR vs. Frequency

MECHANICAL DIMENSIONS
INCHES (mm)

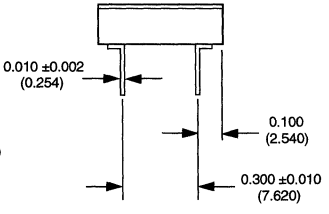


14-PIN DIP

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
AM-1435MC	0 to +70°C
AM-1435MM	–55 to +125°C
AM-1435MM-QL	–55 to +125°C

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DATEL®
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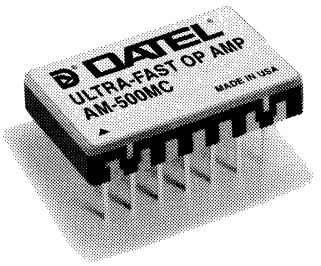
AM-500
High-Speed, Wideband Operational Amplifiers

FEATURES

- **200 nanosecond settling to ±0.01%**
- **±1000V/µsec slew rate**
- **100MHz minimum gain bandwidth product**
- **10^6 open loop gain**
- **±1µV/°C offset drift**
- **±50mA output current**



GENERAL DESCRIPTION

The AM-500 Series amplifiers are fast-settling operational amplifiers for use in inverting applications. A unique feedforward amplifier design combines the characteristics of a low-drift dc amplifier with those of a very fast ac amplifier. For optimum fast-settling performance, this amplifier has an open loop gain roll-off of 6dB per octave to beyond 100MHz.

Output settling time is 200 nanoseconds maximum to ±0.01% for a 10V step change. Slew rate is 1000V/microsecond for positive output transitions and 1800V/microsecond for negative transitions. This high slew rate permits undistorted reproduction of a full-load, 20V peak-to-peak sinewave out to 16MHz. Gain bandwidth product is 100MHz minimum.

AM-500 Series dc characteristics include a dc open loop gain of 10^6, 30 megohm input impedance, and ±1 nanoampere bias current. Input offset voltage is ±0.5mV, and input offset voltage drift is ±1 microvolt/°C. Although these amplifiers do not operate differentially, a dc offset voltage in the range of ±5V can be applied to the positive input terminal.

Power supply requirements are ±15V at 22mA quiescent current. The amplifiers will operate over a supply range of ±10 to ±18V. Output current capability is ±50mA with output short-circuit protection. Four versions are available: AM-500GC and AM-500MC for 0 to +70°C operation; AM-500MM for –55 to +125°C operation; and AM-500MM-QL for high-reliability operation over the military temperature range.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	N.C.
2	N.C.
3	N.C.
4	–INPUT
5	+INPUT
6	–15V SUPPLY
7	N.C.
8	COMMON
9	DO NOT CONNECT
10	OUTPUT
11	+15V SUPPLY
12	N.C.
13	N.C.
14	N.C.

NOTE: Do not connect pin 9 to ground or any other pin.

7

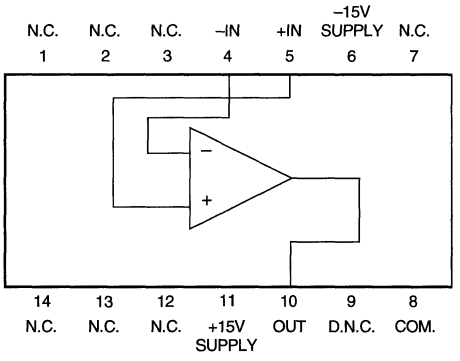


Figure 1. AM-500 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MIN.	TYP.	MAX.	UNITS
+15V Supply (Pin 11)	—	+18	—	Volts
–15V Supply (Pin 6)	—	–18	—	Volts
Analog Inputs (Pins 4, 5)	—	±18	—	Volts
Lead Temperature (soldering, 10 seconds)	—	300	—	°C
Short Circuit to Ground	Continuous			

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V supplies, unless otherwise noted.)

INPUT	MIN.	TYP.	MAX.	UNITS
Input Common Mode Voltage Range ①	—	—	±5	Volts
Differential Input Impedance	1	30	—	megohms
Input Bias Current	—	±1	±4	nA
Input Offset Current	—	±0.5	±8	nA
Input Offset Voltage	—	±0.5	±3	mV
PERFORMANCE				
DC Open Loop Gain	10^5	10^6	—	V/V
Input Offset Voltage Drift				
0 to +70°C	—	±1	±5	µV/°C
–55 to +125°C	—	±5	±10	µV/°C
Input Bias Current Drift				
–55 to +70°C	—	–20	—	pA/°C
+70 to +125°C	Doubles every 10°C			
Input Voltage Noise ②				
0.01Hz to 1Hz	—	5	25	µVp-p
100Hz to 10kHz	—	1	5	µVrms
1Hz to 10MHz	—	20	100	µVrms
Power Supply Rejection Ratio (–55 to +125°C)	60	—	—	dB
DYNAMIC CHARACTERISTICS				
Gain Bandwidth Product	100	130	—	MHz
Slew Rate (positive going)	800	1000	—	V/µs
Slew Rate (negative going)	800	1800	—	V/µs
Full Power Bandwidth (20Vp-p)	—	16	—	MHz
Settling Time (±10V step) ③				
To ±0.01% (+25°C)	—	—	200	ns
To ±0.01% (–55 to +125°C)	—	—	600	ns
To ±0.1% (–55 to +125°C)	—	100	300	ns
To ±1.0% (–55 to +125°C)	—	70	200	ns
Overload Recovery Time	—	10	30	µs
OUTPUT				
Output Voltage	±10	—	—	Volts
Output Current (S.C. protected)	±25	±50	—	mA
Stable Capacitive Load	—	100	—	pF
Output Impedance	—	25	—	Ω
POWER REQUIREMENTS				
Voltage (rated performance)	—	±15	—	Volts
Voltage (operating)	±10	—	±18	Volts
Quiescent Current	—	±22	±37	mA

Footnotes:

① dc only

② –3dB single-pole bandwidth

③ 1kΩ input and feedback resistors, 2.4pF feedback capacitor

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
AM-500GC, MC	0	—	+70	°C
AM-500MM, MM-QL	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Thermal Impedance				
θ_{JC}	—	48	—	°C/W
θ_{CA}	—	57	—	°C/W
Package Type	14-pin ceramic DIP			
Weight	0.09 ounces (2.5 grams)			

TECHNICAL NOTES

1. Figure 2 shows the connection of the AM-500 Series for fast settling operation with a closed loop gain of –1. It can be used for fast settling at closed loop gains up to –10. The equivalent resistance seen by the summing junction should be 500Ω or less. For gains greater than –1, use an input resistor of 500Ω and pick a feedback resistor for the required closed loop gain (1kΩ for –2, 1.5kΩ for –3, etc.).

2. Use a small feedback capacitor across the feedback resistor. Determine C in nanofarads using the following formula:

$$C = \frac{1 + |G|}{0.816Rf}$$

where G is closed loop gain and Rf is in kΩ.

3. Summing point leads must be kept as short as possible. Input and feedback resistors should be soldered close to the body of the amplifier directly to the summing point (pin 4). Summing point capacitance to ground must be kept very low.

4. Low output impedance power supplies should be used with 1µF tantalum bypassing capacitors at the amplifier supply terminals. The amplifier has internal 0.03µF ceramic bypass capacitors.

5. Although these amplifiers are designed for inverting mode only, a dc voltage in the range of ±5V may be applied to the positive input terminal to offset the amplifier.

6. For interrupted power applications, apply power to the AM-500 three (3) seconds before operating the device.

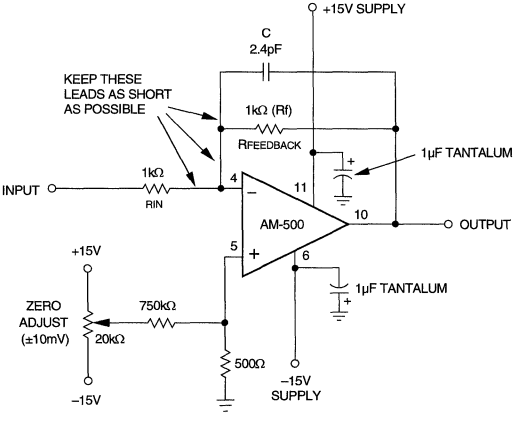


Figure 2. Connection for Fast Settling with Gain of –1

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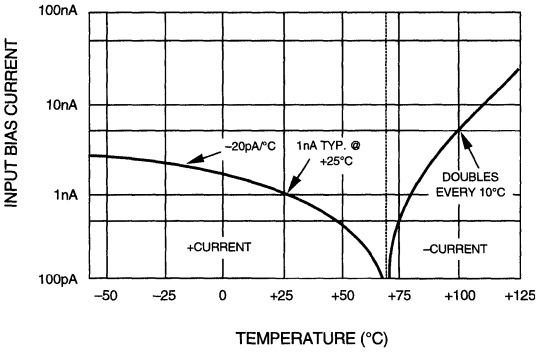
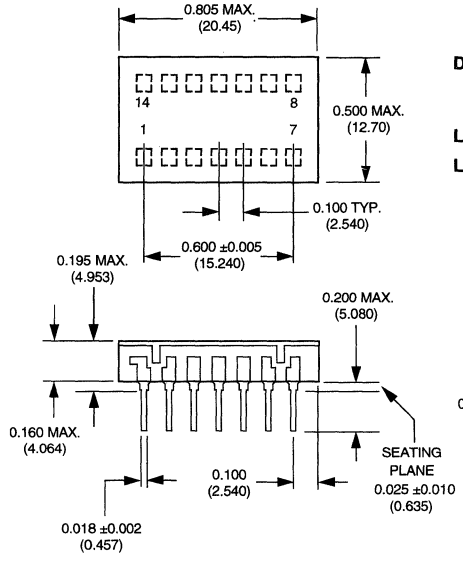
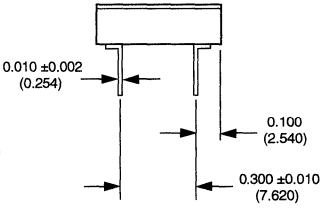


Figure 3. Input Bias Current vs. Temperature

MECHANICAL DIMENSIONS
INCHES (mm)





14-PIN DIP

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

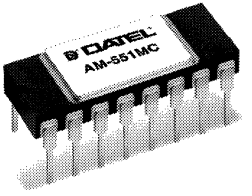
MODEL	OPERATING TEMP. RANGE
AM-500GC	0 to +70°C
AM-500MC	0 to +70°C
AM-500MM	–55 to +125°C
AM-500MM-QL	–55 to +125°C

DATEL®
INNOVATION and EXCELLENCE

AM-551
High-Speed, Programmable-Gain Instrumentation Amplifiers

FEATURES

- **1 to 50 gain range**
- **±0.01% maximum nonlinearity**
- **3µs settling time**
- **100dB CMRR**
- **600kHz small signal bandwidth**
- **Resistor and pin programmable**



GENERAL DESCRIPTION

DATEL's AM-551 is a high-performance, programmable-gain instrumentation amplifier manufactured with hybrid thin-film technology. Gain is adjustable over a range of 1 to 50 with a single external resistor and a simple user-selectable pin-strapping option. Maximum gain nonlinearity is ±0.01%.

The AM-551 dynamic characteristics include a settling time of 3µs for a 20V step to ±0.01% accuracy. Slew rate is ±23V/µs, and small signal bandwidth is 600kHz. Other specifications include a CMRR of 100dB, a $10^{12}\Omega$ input impedance and a minimum output voltage swing of ±11V. Maximum offset drift is ±15µV/°C.

The AM-551 is a functionally complete device containing a high-impedance variable-gain voltage follower input stage followed by a differential output stage with user-selectable gains of 1 or 10. High-accuracy, ultra-low-drift, thin-film technology is used for all interconnected resistor networks.

The combination of accuracy, speed and rugged hybrid construction make the AM-551 an ideal choice for applications involving the amplification of low-level signals produced by thermocouples, strain gages and RTD's, high-performance data acquisition systems and instrumentation systems.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	INPUT OFFSET ADJUST
2	R_G (Gain Resistor)
3	+INPUT
4	R_G (Gain Resistor)
5	–INPUT
6	–15V SUPPLY
7	SIGNAL COMMON
8	OUTPUT OFFSET ADJ. WIPER
9	OUTPUT OFFSET ADJUST
10	OUTPUT OFFSET ADJUST
11	OUTPUT
12	OUTPUT GAIN SELECT
13	GUARD
14	+15V SUPPLY
15	INPUT OFFSET ADJUST
16	INPUT OFFSET ADJ. WIPER

Power requirements are ±15V, and all devices are cased in miniature, 16-pin ceramic DIP's. Models are available for commercial (0 to +70°C) or military (–55 to +125°C) operating temperature ranges.

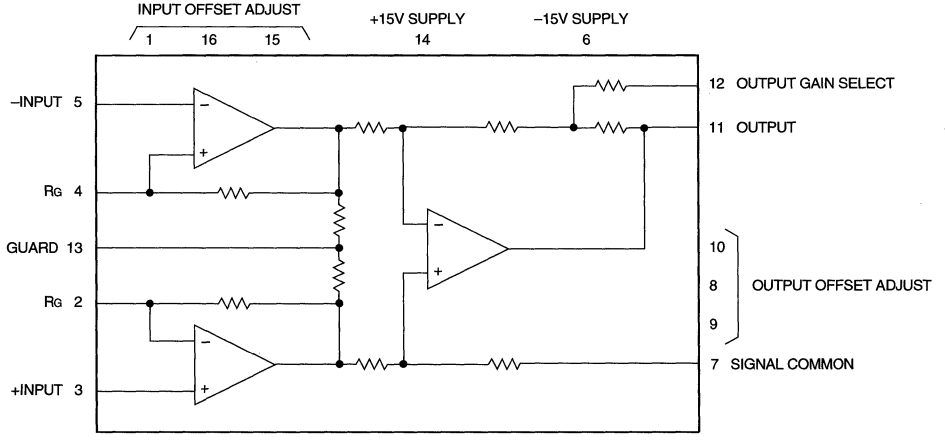


Figure 1. AM-551 Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MIN.	TYP.	MAX.	UNITS
+15V Supply (Pin 14)	—	+18	—	Volts
–15V Supply (Pin 6)	—	–18	—	Volts
Input Voltage Range	—	±18	—	Volts
Differential Input Voltage Range	—	±30	—	Volts
Lead Temperature (soldering, 10 seconds)	—	300	—	°C
Output Short Circuit	Continuous			

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V supplies, unless otherwise noted.)

INPUT	MIN.	TYP.	MAX.	UNITS
Common Mode Voltage Range	±11	—	—	Volts
Input Impedance (differential or common mode)	—	10^{12}	—	Ω
Input Bias Current	—	—	±100	pA
Input Offset Current	—	—	±20	pA
Input Offset Voltage (unadj.) ①	—	—	±1	mV x gain
PERFORMANCE				
Gain Range ②	1	—	50	V/V
Gain Equation ③	$G = (1 + 20k/R_G)\ G_2$			
Gain Accuracy				
G = 1	—	—	±0.04	%
G = 10	—	—	±0.1	%
G = >10	—	—	±0.2	%
Gain Nonlinearity	—	—	±0.01	%
Gain Tempco ④	—	—	±50	ppm/°C
Offset Voltage Drift	—	—	±15	µV/°C
Input Bias Current Drift	Doubles every 10°C			
Input Voltage Noise (dc to 100Hz)	—	20	—	$nV/\sqrt{Hz}$
Power Supply Rejection Ratio	70	82	—	dB
Common Mode Reject. Ratio ⑤				
1kHz	—	70	—	dB
100Hz	—	90	—	dB
DC	—	100	—	dB
Slew Rate	±9	±23	—	V/µs
Small Signal Bandwidth (–3dB)				
G = 1	—	600	—	kHz
G = 10	—	600	—	kHz
G = 50	—	200	—	kHz
Settling Time (20V to ±0.01%)				
G = 1	—	3	—	µs
G = 10	—	4	—	µs
G = 50	—	11	—	µs
OUTPUT				
Output Voltage Range ⑥	±11	—	—	Volts
Output Current	±5	—	—	mA
Output Impedance ⑦	—	0.5	—	Ω
Output Offset Voltage (unadj.) ①	—	—	±1	mV x gain
POWER REQUIREMENTS				
Rated Power Supply Voltages	—	±15	—	Volts
Power Supply Range	±5	—	±18	Volts
Supply Current	—	—	±27	mA

Footnotes:

① Adjustable to zero.

② To 0.01% accuracy. Higher gains are achievable, but performance will degrade.

③ See Technical Note 3.

④ Tempco of R_G = ±0ppm/°C. For R_G = ∞, gain tempco = ±5ppm/°C.

⑤ 1kΩ source imbalance.

⑥ R_L = 2kΩ.

⑦ At 1kHz, for all gain ranges.

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
AM-551MC	0	—	+70	°C
AM-551MM	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type	16-pin ceramic DIP			

TECHNICAL NOTES

1. A 100kΩ trimpot may be used for both input and output offset adjusts. The trimpot is connected across the INPUT OFFSET ADJUST pins (pins 1, 15) and the wiper is connected to pin 16.

   For output offset adjust, the trimpot is connected across the OUTPUT OFFSET ADJUST pins (pins 10, 9) with the wiper connected to pin 8.

2. For unity gain, R_G is left open and OUTPUT GAIN SELECT (pin 12) is tied to OUTPUT (pin 11). To avoid oscillation in the unity-gain configuration, the connection between OUTPUT GAIN SELECT and OUTPUT should be kept as short as possible.

3 Gain selection is accomplished in two stages. The input stage gain (G_1) is selected by an external gain resistor (R_G) connected across the R_G pins (pins 2, 4), and is expressed as follows:

$$G_1 = 1 + \frac{20k}{R_G}$$

The output stage gain (G_2) is selected by external pin-strapping. For G_2 = 1, connect OUTPUT GAIN SELECT (pin 12) to OUTPUT (pin 11). For G_2 = 10, connect OUTPUT GAIN SELECT (pin 12) to SIGNAL COMMON (pin 7).

The total gain of the amplifier is as follows:

$$G_t = G_1 \times G_2 = \left(1 + \frac{20k}{R_G}\right) G_2$$

4. Both power supplies should be bypassed to ground with 0.1µF ceramic capacitors.

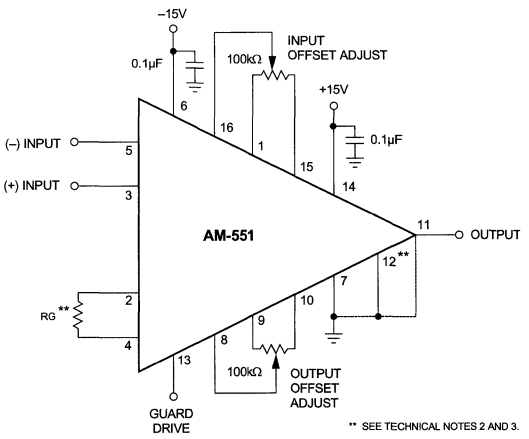
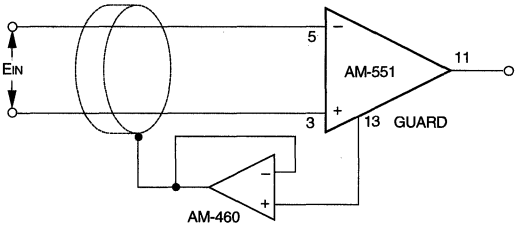


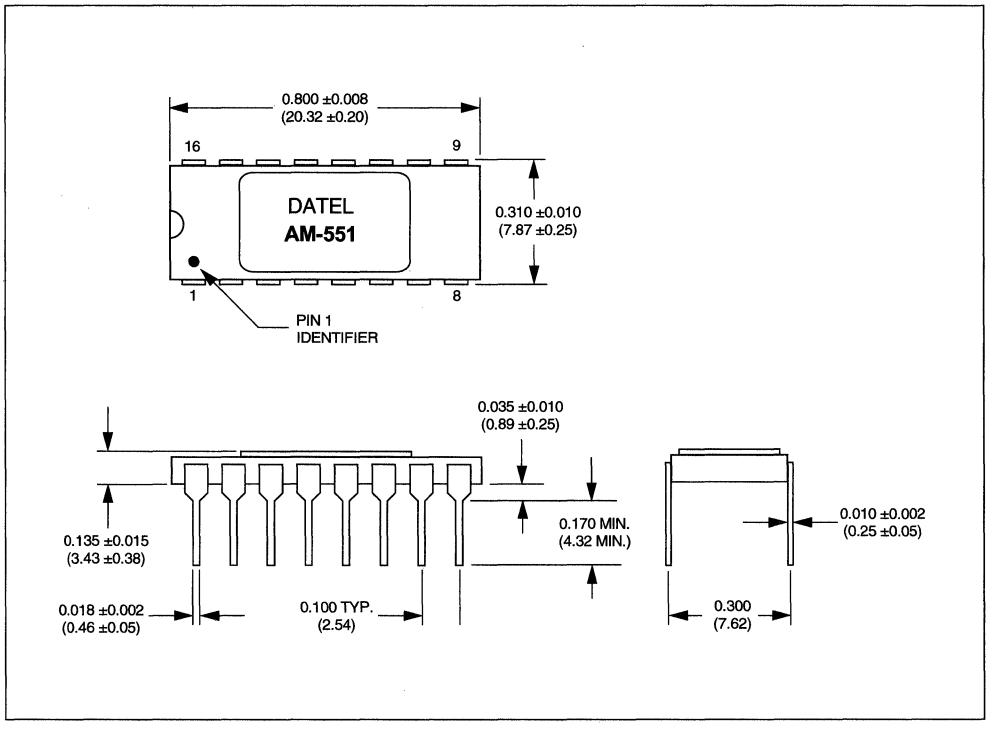
Figure 2. Typical Connections

GUARD DRIVE CONNECTION

A GUARD (pin 13) is provided to improve ac common mode rejection by compensating for unbalanced capacitance due to long input leads. Use of the guard function is recommended whenever input leads are longer than a few inches. In cases in which the input leads are very long or when system bandwidth is very high, the addition of a buffer amplifier is recommended. The diagram to the right shows a typical guard drive connection to the AM-551 using DATEL's AM-460.



MECHANICAL DIMENSIONS
INCHES (mm)



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
AM-551MC	0 to +70°C
AM-551MM	–55 to +125°C

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DATEL
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Complete Data Acquisition Systems

Table of Contents

Selection Guide

Model ①	Resolution (Bits)	Input Channels	Throughput Rate, Min. (kHz)	Differential Linearity Error, Max. (LSB)	Integral Linearity Error, Max. (LSB)	Total Harmonic Distortion (–dB)	Power Supplies (Volts)	Maximum Power Dissipation (Watts)	Page
HDAS-16	12	16SE	50	±1	±1	—	+5, ±15	1.25	**8-3**
HDAS-8	12	8D	50	±1	±1	—	+5, ±15	1.25	**8-3**
HDAS-75	12	8SE	75	±1	±1	73	+5, ±15	0.7	**8-15**
HDAS-76	12	4D	75	±1	±1	73	+5, ±15	0.7	**8-15**
HDAS-528	12	8SE	400	±0.75	±0.75	73	+5, ±15	3	**8-10**
HDAS-524	12	4D	400	±0.75	±0.75	73	+5, ±15	3	**8-10**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① MIL-STD-883 models available for all listed products except HDAS-524.

For literature or technical assistance

800-233-2765

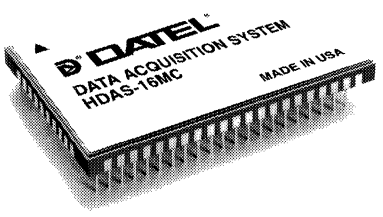
or contact your local DATEL Sales Office or Representative

DATEL®
INNOVATION and EXCELLENCE

HDAS-16, HDAS-8
12-Bit, 50kHz, Complete Data Acquisition Systems

FEATURES

- **Miniature 62-pin cermanic package**
- **12-Bit resolution, 50kHz throughput**
- **Full-scale input range from 50mV to 10V**
- **Three-state outputs**
- **16 S.E. or 8 differential input channels**
- **Auto-sequencing channel addressing**
- **MIL-STD-883 versions**
- **No missing codes**



GENERAL DESCRIPTION

Using thin and thick-film hybrid technology, DATEL offers complete low-cost data acquisition systems with superior performance and reliability.

The HDAS-8 (with 8 differential input channels) and the HDAS-16 (with 16 single-ended input channels) are complete, high-performance, 12-bit data acquisition systems in 62-pin packages. Each HDAS may be expanded up to 32 single-ended or 16 differential channels by adding external multiplexers.

Internal channel address sequencing is automatic after each conversion, or the user may supply external channel addresses.

Internal HDAS circuitry includes:

- **Analog input multiplexer (16 S.E. or 8 diff.)**
- **Resistor-programmable instrumentation amplifier**
- **Sample-and-hold circuit complete with MOS hold capacitor**
- **10 Volt buffered reference**
- **12-bit A/D converter with three-state outputs and control logic**

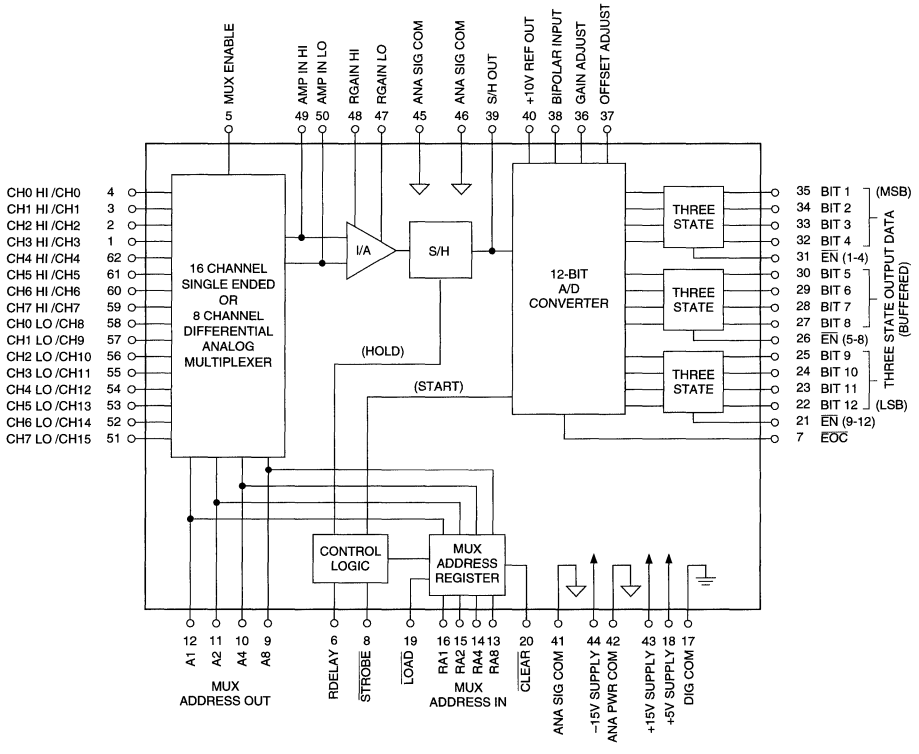


Figure 1. HDAS-16 and HDAS-8 Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MIN.	TYP.	MAX.	UNITS
+15V Supply (pin 43)	–0.5	—	+18	Volts
–15V Supply (pin 44)	+0.5	—	–18	Volts
+5V Supply (pin 18)	–0.5	—	+7	Volts
Analog Inputs ①	–35	—	+35	Volts
Digital Inputs	–0.5	—	+7	Volts
Thermal Resistances:				
Junction-Case	—	—	15	°C/Watt
Case-Ambient	—	—	15	°C/Watt
Junction-Ambient	—	—	30	°C/Watt
Lead Temp. (10 seconds)	—	—	300	°C

FUNCTIONAL SPECIFICATIONS

(The following specifications apply over the operating temperature range and power supply range unless otherwise indicated.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Signal Range, Unipolar				
Gain = 1	0	—	+10	Volts
Gain = 200	—	—	+50	mV
Signal Range, Bipolar				
Gain = 1	–10	—	+10	Volts
Gain = 200	–50	—	+50	mV
Input Gain Equation ②	Gain = 1 + (20kΩ/RGAIN)			
Gain Equation Error	—	—	±0.1	%
Instrumentation Amplifier				
Input Impedance	10^8	10^{12}	—	Ohms
Input Bias Current:				
+25°C	—	—	±250	pA
–55 to +125°C	Doubles every 10°C			
Input Offset Current:				
+25°C	—	—	±1	nA
–55 to +125°C	Doubles every 10°C			
Multiplexer				
Channel ON Resistance	—	—	2	kΩ
Channel OFF Input Leakage	—	±30	—	pA
Channel OFF Output Leakage	—	±1	—	nA
Channel ON Leakage	—	±100	—	pA
Input Capacitance				
HDAS-16, Channel ON	—	100	—	pF
HDAS-8, Channel ON	—	50	—	pF
+25°C, Channel OFF	—	5	—	pF
Input Offset Voltage				
Gain = 1, +25°C	—	—	±2	mV
–55 to +125°C (max.)	(±3ppm/°C x Gain) ±20ppm/°C			
Gain = 200, +25°C	—	—	±100	mV
–55 to +125°C (max.)	(±3ppm/°C x Gain) ±20ppm/°C			
Common Mode Range	±10	—	—	Volts
CMRR, Gain = 1, at 60Hz	70	82	—	dB
Input Voltage Noise, Gain = 1 (Referred to input)	—	150	200	µVrms
Channel Crosstalk	—	—	–80	dB
PERFORMANCE				
Resolution	12	—	—	Bits
Integral Nonlinearity				
0 to +70°C	—	—	±1	LSB
–55 to +125°C	—	—	±1	LSB
Differential Nonlinearity				
0 to +70°C	—	—	±1	LSB
–55 to +125°C	—	—	±1	LSB
No Missing Codes	Over the operating temperature range			

PERFORMANCE (cont.)	MIN.	TYP.	MAX.	UNITS
Unipolar Zero Error				
+25°C ③	—	—	±0.1	%FSR
–55 to +125°C	—	—	±0.3	%FSR
Bipolar Zero Error				
+25°C ③	—	—	±0.1	%FSR
–55 to +125°C	—	—	±0.3	%FSR
Bipolar Offset Error				
+25°C ③	—	—	±0.1	%FSR
–55 to +125°C	—	—	±0.3	%FSR
Gain Error				
+25°C ③	—	—	±0.2	%
–55 to +125°C	—	—	±0.3	%
DYNAMIC CHARACTERISTICS				
Acquisition Time, Gain = 1				
+25°C	—	9	10	µs
–55 to +125°C	—	—	15	µs
Aperture Delay Time	—	—	500	ns
Aperture Uncertainty	—	—	1	ns
S/H Droop Rate	—	—	±1	µV/µs
Feedthrough	—	—	±0.01	%
A/D Conversion Time				
+25°C	—	6	8	µs
–55 to +125°C	—	—	10	µs
Throughput Rate				
+25°C	50	66	—	kHz
–55 to +125°C	33	—	—	kHz
DIGITAL INPUTS				
Logic Levels				
(Pins 8, 13–16, 19–21, 26, 31)				
Logic 1	+2.0	—	+5.5	Volts
Logic 0	0	—	+0.8	Volts
(Pin 5)				
Logic 1	+4.0	—	+5.5	Volts
Logic 0	0	—	+0.8	Volts
Logic Loading				
(Pins 5, 8, 13–16, 19–21, 26, 31)				
Logic 1	—	—	±10	µA
Logic 0	—	—	±10	µA
Multiplexer Address Set-up Time	20	—	—	ns
$\overline{\text{ENABLE}}$ to Data Valid Delay	—	20	30	ns
$\overline{\text{STROBE}}$ ④	40	—	—	ns
OUTPUTS				
Logic Levels (Output Data)				
Logic 1	+2.4	—	—	Volts
Logic 1 (pin 7)	+2.5	—	—	Volts
Logic 0	—	—	+0.4	Volts
(Pins 9, 10, 11, and 12)				
Logic 1	+2.5	—	—	Volts
Logic 0	—	—	+0.4	Volts
Logic Loading				
Logic 1	—	—	–400	µA
Logic 0	—	—	+4	mA
Internal Reference:				
Voltage, +25°C	+9.99	+10.00	+10.01	Volts
Drift	—	—	±20	ppm/°C
External Current	—	—	1	mA
Output Data Coding	Straight binary (unipolar) or offset binary (bipolar)			

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FUNCTIONAL SPECIFICATIONS (Continued)

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Power Supply Ranges				
+15V Supply	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	Volts
+5V Suppy	+4.75	+5.0	+5.25	Volts
Power Supply Currents				
+15V Supply	—	—	+33	mA
–15V Supply	—	—	–30	mA
+5V Suppy	—	—	+15	mA
Power Dissipation	—	—	1.25	Watts
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
MC Models	0	—	+70	°C
MM/883 Models	–55	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Weight	1.4 ounces (39.7 grams)			
Package Type	62-pin cermanic DIP			

Footnotes:

① Analog inputs will withstand ±35V with power on. If the power is off, the maximum safe input (no damage) is ±20V.

② The gain equation error is guaranteed before external trimming and applies at gains less than 50. This error increases at gains over 50.

③ Adjustable to zero.

④ $\overline{\text{STROBE}}$ pulse width must be less than $\overline{\text{EOC}}$ period to achieve maximum throughput rate.

TECHNICAL NOTES

1. Input channels are protected to 20 Volts beyond the power supplies. All digital output pins have one second short-circuit protection.
2. To retain high system throughput rates while digitizing low-level signals, apply external high-gain amplifiers for each channel. DATEL's AM-551 is suggested for such amplifier-per-channel applications.
3. The HDAS devices have self-starting circuits for free-running sequential operation. If, however, in a power-up condition the supply voltage slew rate is less than 3V per microsecond, the free running state might not be initialized. Apply a negative pulse to the $\overline{\text{STROBE}}$, to eliminate this condition.
4. For unipolar operation, connect BIPOLAR INPUT (pin 38) to S/H OUT (pin 39). For bipolar operation, connect BIPOLAR INPUT (pin 38) to +10V REFERENCE OUT (pin 40).
5. RDELAY may be a standard value 5% carbon composition or film-type resistor.
6. RGAIN must be very accurate with low temperature coefficients. If necessary, fabricate the gain resistor from a precision metal-film type in series with a low value trim resistor or potentiometer. The total resistor temperature coefficient must be no greater than ±10ppm/°C.
7. ANALOG SIGNAL COMMON, POWER COMMON and DIGITAL COMMON are connected internally. For optimal performance, tie all ground pins (17, 41, 42, 45, 46) directly to a large analog ground plane beneath the package.
8. For HDAS-16, tie pin 50 to a "signal source common" if possible. Otherwise tie pin 50 to pin 41 (ANA SIG COM).

INPUT/OUTPUT CONNECTIONS

PIN NO.	HDAS-16	HDAS-8
1	CH3 IN	CH3 HIGH IN
2	CH2 IN	CH2 HIGH IN
3	CH1 IN	CH1 HIGH IN
4	CH0 IN	CH0 HIGH IN
5	MUX ENABLE	*
6	RDELAY	*
7	$\overline{\text{EOC}}$	*
8	$\overline{\text{STROBE}}$	*
9	A8 MULTIPLEXER	*
10	A4 ADDRESS	*
11	A2 OUT	*
12	A1	*
13	RA8 MULTIPLEXER	*
14	RA4 ADDRESS	*
15	RA2 IN	*
16	RA1	*
17	DIGITAL COMMON	*
18	+5V SUPPLY	*
19	$\overline{\text{LOAD}}$	*
20	$\overline{\text{CLEAR}}$	*
21	$\overline{\text{ENABLE}}$ (Bits 9–12)	*
22	BIT 12 (LSB)	*
23	BIT 11	*
24	BIT 10	*
25	BIT 9	*
26	$\overline{\text{ENABLE}}$ (Bits 5–8)	*
27	BIT 8	*
28	BIT 7	*
29	BIT 6	*
30	BIT 5	*
31	$\overline{\text{ENABLE}}$ (Bits 1–4)	*
32	BIT 4	*
33	BIT 3	*
34	BIT 2	*
35	BIT 1 (MSB)	*
36	GAIN ADJUST	*
37	OFFSET ADJUST	*
38	BIPOLAR INPUT	*
39	SAMPLE/HOLD OUT	*
40	+10V REFERENCE OUT	*
41	ANALOG SIGNAL COMMON	*
42	ANALOG POWER COMMON	*
43	+15V SUPPLY	
44	–15V SUPPLY	*
45	ANALOG SIGNAL COMMON	*
46	ANALOG SIGNAL COMMON	*
47	RGAIN LOW	*
48	RGAIN HIGH	*
49	AMP. IN HIGH ①	*
50	AMP. IN LOW ①	*
51	CH15 IN	CH7 LOW IN
52	CH14 IN	CH6 LOW IN
53	CH13 IN	CH5 LOW IN
54	CH12 IN	CH4 LOW IN
55	CH11 IN	CH3 LOW IN
56	CH10 IN	CH2 LOW IN
57	CH9 IN	CH1 LOW IN
58	CH8 IN	CH0 LOW IN
59	CH7 IN	CH7 HIGH IN
60	CH6 IN	CH6 HIGH IN
61	CH5 IN	CH5 HIGH IN
62	CH4 IN	CH4 HIGH IN

* Same as HDAS-16

① Caution: Pins 49 and 50 do not have overvoltage protection; therefore, protected multiplexers, such as DATEL's MX-1606 and MX-808 are recommended. See the General Operation description.

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Table 1. Description of Pin Functions

FUNCTION	LOGIC STATE	DESCRIPTION
DIGITAL INPUTS		
$\overline{\text{STROBE}}$	1 to 0	Initiates acquisition and conversion of analog signal
$\overline{\text{LOAD}}$	0	Random address mode initiated on falling edge of STROBE
	1	Sequential address mode
$\overline{\text{CLEAR}}$	0	Allows next STROBE pulse to reset MULTIPLEXER ADDRESS to CH0 overriding LOAD COMMAND
MUX ENABLE	0 1	Disables internal multiplexer Enables internal multiplexer
MUX ADDRESS IN		Selects channel for random address mode 8, 4, 2, 1 natural binary coding
DIGITAL OUTPUTS		
$\overline{\text{EOC}}$ (STATUS)	0	Conversion complete
	1	Conversion in process
$\overline{\text{ENABLE}}$ (1–4)	0	Enables three-state outputs bits 1-4
	1	Disables three-state outputs bits 1-4
$\overline{\text{ENABLE}}$ (5–8)	0	Enables three-state outputs bits 5-8
	1	Disables three-state outputs bits 5-8
$\overline{\text{ENABLE}}$ (9–12)	0	Enables three-state outputs bits 9-12
	1	Disables three-state outputs bits 9-12
MUX ADDRESS OUT		Output of multiplexer address register 8, 4, 2, 1 natural binary coding
ANALOG INPUTS		**DESCRIPTION**
CHANNEL INPUTS		Limit voltage to ±20V beyond power supplies
BIPOLAR INPUT		For unipolar operation, connect to pin 39 (S/H OUT). For bipolar operation, connect to in 40 (+10V OUT)
AMP. IN LOW AMP. IN HIGH		These pins are direct inputs to the instrumentation amplifier for external channel expansion beyond 16SE or 8D channels.
ANALOG OUTPUTS		
S/H OUT		Sample/hold output
+10V REFERENCE OUT		Buffered +10V reference output
ADJUSTMENT PINS		
ANALOG SIGNAL COMMON		Low level analog signal return
GAIN ADJUSTMENT		External gain adjustment. See calibration instructions.
OFFSET ADJUSTMENT		External offset adjustment. See calibration instructions.
RGAIN		Optional gain selection point. Factory adjusted for G = 1 when left open.
RDELAY		Optional acquisition time adjustment when connected to +5V. Factory adjusted for 9µs. Must be connected to +5V either directly or through a resistor.

Table 2. Calibration Table

UNIPOLAR RANGE	ADJUST	INPUT VOLTAGE
0 to +5V	ZERO GAIN	+0.6mV +4.9982V
0 to +10V	ZERO GAIN	+1.2mV +9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	–2.4994V +2.4982V
±5V	OFFSET GAIN	–4.9988V +4.9963V
±10V	OFFSET GAIN	–9.9976V +9.9927V

CALIBRATION PROCEDURES

1. Offset and gain adjustments are made by connecting two 20k trim potentiometers as shown in Figure 2.
2. Connect a precision voltage source to pin 4 (CH0 IN). If the HDAS-8 is used, connect pin 58 (CH0 LOW IN) to analog ground. Ground pin 20 ($\overline{\text{CLEAR}}$) and momentarily short pin 8 ($\overline{\text{STROBE}}$). Trigger the A/D by connecting pin 7 ($\overline{\text{EOC}}$) to pin 8 ($\overline{\text{STROBE}}$). Select proper value for RGAIN and RDELAY by referring to Table 3.
3. Adjust the precision voltage source to the value shown in Table 2 for the unipolar zero adjustment (ZERO + 1/2LSB) or the bipolar offset adjustment (–FS + 1/2LSB). Adjust the offset trim potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
4. Change the output of the precision voltage source to the value shown in Table 2 for the unipolar or bipolar gain adjustment (+FS – 1 1/2LSB). Adjust the gain trim potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

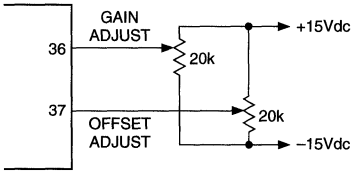

Figure 2. External Adjustment

GENERAL OPERATION

The HDAS devices accept either 16 single-ended or 8 differential input signals. For single-ended circuits, the AMP IN LOW (pin 50) input to the instrumentation amplifier must terminate at ANALOG SIGNAL COMMON (pin 41). For differential circuits, both the HIGH and LOW signal inputs must terminate externally for each channel. Tie unused channels to the ANALOG SIGNAL COMMON (pin 41). To obtain additional channels, connect external multiplexers to the AMP IN HIGH (pin 49) and AMP IN LOW (pin 50). Using this scheme, the HDAS-16 can provide 32 single-ended expansion channels while the HDAS-8 can provide up to 16 differential expansion channels. DATEL's MX Series multiplexers are recommended.

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The acquisition time is the amount of time the multiplexer, instrumentation amplifier, and sample/hold require to settle within a specified range of accuracy after STROBE (pin 8) goes low. The acquisition time period can be observed by measuring how long EOC is low after the falling edge of STROBE (see Figure 4). For higher gains, increase the acquisition time. Do this by connecting a resistor from RDELAY (pin 6) to +5V (pin 18). An external resistor, RGAIN, can be added to increase the gain value. The gain is equal to 1 without an RGAIN resistor. Table 3 refers to the appropriate RDELAY and RGAIN resistors required for various gains.

The HDAS devices enter the hold mode and are ready for conversion as soon as the one-shot (controlling acquisition time) times out. An internal clock is gated ON, and a start-convert pulse is sent to the 12-bit A/D converter, driving the EOC output high.

The HDAS devices can be configured for either bipolar or unipolar operation (see Table 2). The conversion is complete within a maximum of 10 microseconds. The EOC now returns low, the data is valid and sent to the three-state output buffers. The sample/hold amplifier is now ready to acquire new data. The next falling edge of the STROBE pulse repeats the process for the next conversion.

MULTIPLEXER ADDRESSING

The HDAS devices can be configured in either random or sequential addressing modes. Refer to Table 5 and the subsequent descriptions. The number of channels sequentially addressed can be truncated using the MUX ADDRESS OUT (pins 9, 10, 11 and 12) and appropriate decoding circuitry for the highest channel desired. The decoding circuit can drive the CLEAR (pin 20) function low to reset the addressing to channel 0.

Table 3. Input Range Parameters (Typical)

INPUT RANGE ①②	GAIN	RGAIN (Ω)	RDELAY (Ω) ③	THROUGHPUT ④	SYSTEM ACCURACY (% OF FSR)
±10V	1	OPEN	0 (SHORT)	66.6kHz	±0.009
±5V	2	20.0k	0 (SHORT)	66.6kHz	±0.009
±2.5V	4	6.667k	0 (SHORT)	66.6kHz	±0.009
±1V	10	2.222k	0 (SHORT)	66.6kHz	±0.009
±200mV	50	408.2	7k	40.0kHz	±0.010
±100mV	100	202.0	21k	25.6kHz	±0.011
±50mV	200	100.5	51k	14.5kHz	±0.016

Notes

$$\text{RGAIN } (\Omega) = \frac{20{,}000}{(\text{GAIN} - 1)}$$

RDELAY (Ω) = [Total Acquisition Delay (μs) x 1000] – 9000

① The analog input range to the A/D converter is 0 to +10V for unipolar signals and ±10V for bipolar signals.
② Full scale can be accommodated for analog signal ranges of ±50mV to ±10V.
③ For gains between 1 and 10, RDELAY (pin 6) must be shorted to +5V (pin 18).
④ Throughput period equals acquisition and settling delay, plus A/D conversion period (10 microseconds maximum).

Table 4. Output Coding

UNIPOLAR			STRAIGHT BINARY		
INPUT	0 to +10V	0 to +5V	MSB		LSB
+FS – 1LSB	+9.9976	+4.9988	1111	1111	1111
+1/2FS	+5.0000	+2.5000	1000	0000	0000
+1LSB	+0.0024	+0.0012	0000	0000	0001
ZERO	0.0000	0.0000	0000	0000	0000

BIPOLAR			OFFSET BINARY*		
INPUT	±10V	±5V	MSB		LSB
+FS – 1LSB	+9.9951	+4.9976	1111	1111	1111
+1/2FS	+5.0000	+2.5000	1100	0000	0000
+1LSB	+0.0049	+0.0024	1000	0000	0001
ZERO	0.0000	0.0000	1000	0000	0000
–FS + 1LSB	–9.9951	–4.9976	0000	0000	0001
–FS	–10.000	–5.0000	0000	0000	0000

* For 2's complement coding, add an inverter to the MSB line.

Table 5. Mux Channel Addressing

PIN					ON CHANNEL	
	MUX ADDRESS					
5	13	14	15	16		
MUX ENABLE	RA8	RA4	RA2	RA1		
0	X	X	X	X	NONE	
1	0	0	0	0	0	HDAS-8 (3-BIT ADDRESS)
1	0	0	0	1	1	
1	0	0	1	0	2	
1	0	0	1	1	3	
1	0	1	0	0	4	
1	0	1	0	1	5	
1	0	1	1	0	6	
1	0	1	1	1	7	
1	1	0	0	0	8	HDAS-16 (4-BIT ADDRESS)
1	1	0	0	1	9	
1	1	0	1	0	10	
1	1	0	1	1	11	
1	1	1	0	0	12	
1	1	1	0	1	13	
1	1	1	1	0	14	
1	1	1	1	1	15	

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RANDOM ADDRESSING

Set pin 19 (LOAD) to logic 0. The next falling edge of STROBE will load the MUX CHANNEL ADDRESS present on pin 13 to pin 16. Digital address inputs must be stable 20ns before and after falling edge of the STROBE pulse.

FREE RUNNING SEQUENTIAL ADDRESSING

Set pin 19 (LOAD) and pin 20 (CLEAR) to logic 1 or leave open. Connect pin 7 (EOC) to pin 8 (STROBE). The falling edge of EOC will increment channel address. This means that when the EOC is low, the digital output data is valid for the previous channel (CHn – 1) rather than the channel indicated on MUX ADDRESS OUTPUT. The HDAS will continually scan all channels.

Example:
CH4 has been addressed and a conversion takes place. The EOC goes low. That channel's (CH4's) data becomes valid, but MUX ADDRESS OUTPUT is now CH5.

TRIGGERED SEQUENTIAL ADDRESSING

Set pin 19 (LOAD) and pin 20 (CLEAR) to logic 1 or leave open. Apply a falling edge trigger pulse to pin 8 (STROBE). This negative transition causes the contents of the address counter to be incremented by one, followed by an A/D conversion in 9 microseconds.

INPUT VOLTAGE PROTECTION

As shown in Figure 3, the multiplexer has reversed biased diodes which protect the input channels from being damaged by overvoltage signals. The HDAS input channels are protected up to 20V beyond the supplies and can be increased by adding series resistors (Ri) to each channel. The input resistor must limit the current flowing through the protection diodes to 10mA.

The value of Ri for a specific voltage protection range (Vp) can be calculated by the following formula:

$$Vp = (Rsignal + Ri + R_{ON})\ (10mA)$$
where $R_{ON} = 2k$

NOTE: Increased input series resistance will increase multiplexer settling time significantly.

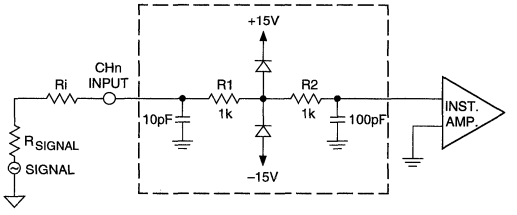

Figure 3. Multiplexer Equivalent Circuit

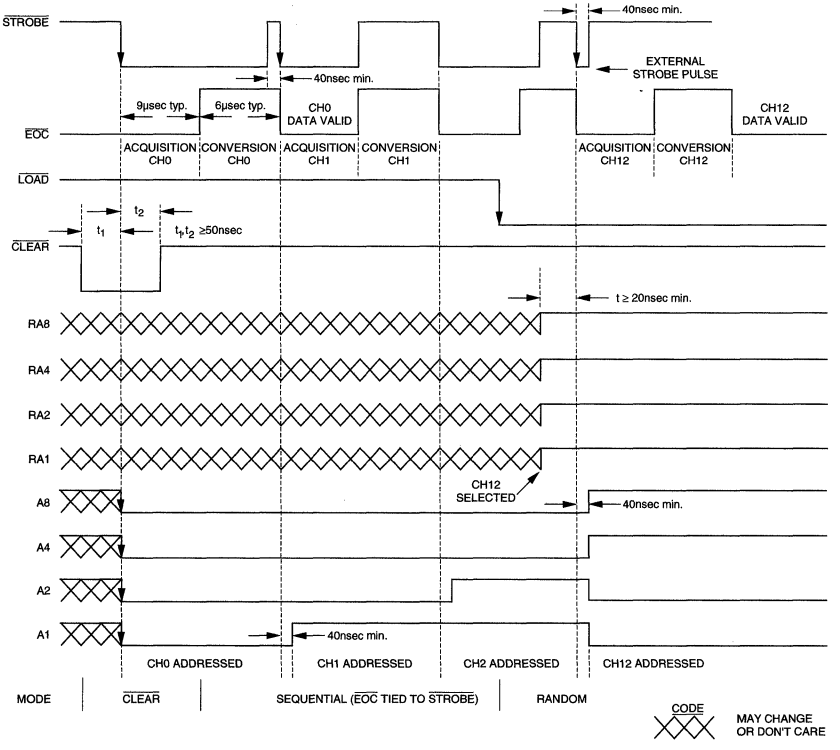

Figure 4. HDAS Timing Diagram

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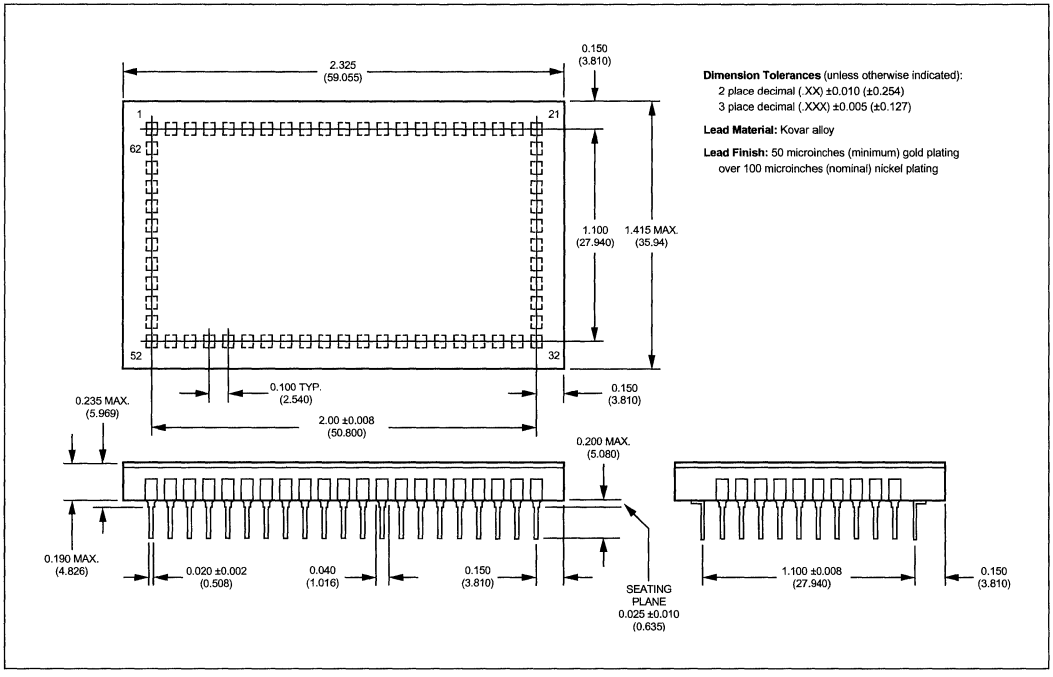
MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
HDAS-16MC	0 to +70°C
HDAS-16MM	–55 to +125°C
HDAS-16/883	–55 to +125°C
HDAS-8MC	0 to +70°C
HDAS-8MM	–55 to +125°C
HDAS-8/883	–55 to +125°C

Receptacles for PC board mounting can be ordered through AMP Inc., Part #3-331272-4 (Component Lead Spring Socket), 62 required.

Contact DATEL, Inc. for MIL-STD-883 product specifications.

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HDAS-524, HDAS-528

12-Bit, 400kHz, Complete Data Acquisition Systems

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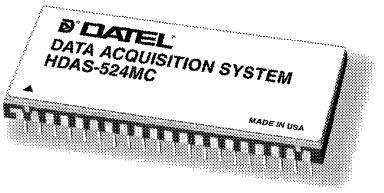
INNOVATION and EXCELLENCE

FEATURES

- **12-Bit resolution, 400kHz throughput**
- **8 Channels single-ended or 4 channels differential**
- **Miniature, 40-pin, ceramic DDIP**
- **Full scale input range from 100mV to 10V**
- **Three-state outputs**
- **No missing codes**



GENERAL DESCRIPTION

The HDAS-524 and HDAS-528 are complete data acquisition systems. Each contains an internal multiplexer, instrumentation amplifier, sample-hold, analog-to-digital converter and three-state outputs. Packaged in miniature, 40-pin, double-dip packages, the HDAS-524/528 have a low power dissipation of 2.6 Watts.

The HDAS-524 provides 4 differential inputs, and the HDAS-528 provides 8 single-ended inputs. An internal instrumentation amplifier is characterized for gains of 1, 2, 4, 8, 10 and 100. The gain range is selectable through a single external resistor.

HDAS-524/528 OPERATION

The HDAS devices accept either 8 single-ended or 4 differential input signals. Tie unused channels to SIGNAL GROUND, pin 14. Channel selection is accomplished using the multiplexer address pins as shown in Table 1. Obtain additional channels by connecting external multiplexers.

The acquisition time is the amount of time the multiplexer, instrumentation amplifier and sample-hold require to settle within a specified range of accuracy. The acquisition time can be measured by how long $\overline{EOC}$ is low before the rising edge

Continued on page 8-12

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH0/CH0 HI	40	START CONVERT
2	CH1/CH1 HI	39	CA2
3	CH2/CH2 HI	38	CA1
4	CH3/CH3 HI	37	CA0
5	CH7/CH3 LO	36	+5V SUPPLY
6	CH6/CH2 LO	35	DIGITAL GROUND
7	CH5/CH1 LO	34	$\overline{ENABLE}$
8	CH4/CH0 LO	33	BIT 1 (MSB)
9	$\overline{COMP\ BIN}$	32	BIT 2
10	RGAIN LO	31	BIT 3
11	RGAIN HI	30	BIT 4
12	S/H OUT	29	BIT 5
13	+10V REFERENCE OUT	28	BIT 6
14	SIGNAL GROUND	27	BIT 7
15	GAIN ADJUST	26	BIT 8
16	OFFSET ADJUST	25	BIT 9
17	BIPOLAR	24	BIT 10
18	–15V SUPPLY	23	BIT 11
19	ANALOG GROUND	22	BIT 12 (LSB)
20	+15V SUPPLY	21	$\overline{EOC}$

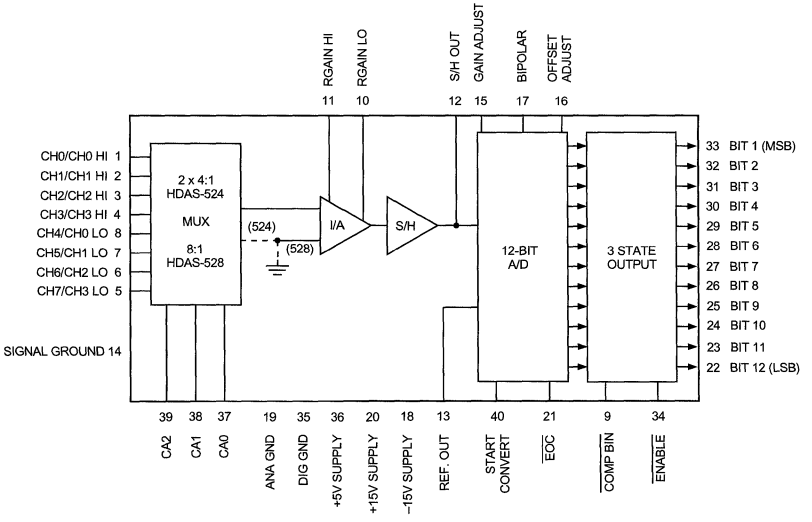


Figure 1. Functional Block Diagram

DATEL, Inc., 11 Cabot Boulevard, Mansfield, MA 02048-1194 (U.S.A.) Tel: 508-339-3000 Fax: 508-339-6356 • For immediate assistance 800-233-2765

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MIN.	TYP.	MAX.	UNITS
+15V Supply, Pin 20	0	—	+18	Volts
–15V Supply, Pin 18	0	—	–18	Volts
+5V Supply, Pin 36	–0.5	—	+7	Volts
Digital Inputs, Pins 9, 34, 37-40	–0.3	—	$+V_{DD}$ +0.3	Volts
Analog Inputs, Pins 1–8	–15	—	+15	Volts
Lead Temperature (10 seconds)	—	—	300	°C

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range with ±15V and +5V supplies unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Inputs				
HDAS-524	4 differential inputs			
HDAS-528	8 single-ended inputs			
Input Voltage Ranges				
Gain = 1	0 to +10V, ±10V			
Gain = 100	0 to +100mV, ±100mV			
I.A. Gain Ranges	1, 2, 4, 8, 10, 100			
Input Impedance				
CH On, CH Off	10^{11}	10^{12}	—	Ohms
Input Capacitance				
(-524) CH On, CH Off	—	—	12	pF
(-528) CH On, CH Off	—	—	25	pF
Input Bias Current	—	—	±200	pA
Input Offset Current	—	—	±50	pA
Input Offset Voltage	—	—	±10	mV
Common Mode Voltage Range	±11	—	—	Volts
CMRR, G = 1, @10Hz, Vcm = 1Vp-p	72	80	—	dB
Voltage Noise (RMS)				
Gain = 1	—	—	200	µV
Gain = 8	—	—	50	µV
MUX Crosstalk @125kHz	–72	—	—	dB
MUX ON Resistance	—	450	500	Ohms
Bias Current Tempco	Doubles (max.) every 10°C above +70°C			
Offset Current Tempco	Doubles (max.) every 10°C above +70°C			
Offset Voltage Tempco	(±30ppm/°C x gain) ±20ppm/°C (max.)			
Input Gain Equation	$GAIN = \frac{2k\Omega}{R_{GAIN}} + 1$			
DIGITAL INPUTS				
Logic Levels				
Logic 1	+2.0	—	—	Volts
Logic 0	—	—	+0.5	Volts
Logic Loading				
Logic 1	—	—	+5	µA
Logic 0	—	—	–600	µA
OUTPUTS				
Logic Levels				
Logic 1	+2.4	—	—	Volts
Logic 0	—	—	+0.4	Volts
Logic Loading				
Logic 1	—	—	–160	µA
Logic 0	—	—	+6.4	mA
Internal Reference				
Voltage, +25°C	+9.9	+10.0	+10.1	Volts
Drift	—	±5	±35	ppm/°C
External Current	—	—	1.5	mA
Output Coding	Straight binary/Offset binary Comp. binary/Comp. offset binary			

Footnotes:

① Specifications valid at +25°C and over the temperature ranges of 0 to +70°C or –55 to +125°C.

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Resolution	12	—	—	Bits
Integral Nonlinearity, +25°C	—	—	±0.75	LSB
0 to +70°C	—	—	±0.75	LSB
–55 to +125°C	—	—	±1.5	LSB
Differential Nonlinearity, +25°C	—	—	±0.75	LSB
0 to +70°C	—	—	±0.75	LSB
–55 to +125°C	—	—	±1	LSB
F.S. Abs. Accuracy, +25°C	—	±0.13	±0.3	%FSR
0 to +70°C	—	±0.15	±0.5	%FSR
–55 to +125°C	—	±0.25	±0.78	%FSR
Unipolar Zero Error, +25°C	—	±0.074	±0.15	%FSR
Unipolar Zero Tempco	—	±15	±30	ppm/°C
Bipolar Zero Error, +25°C	—	±0.074	±0.15	%FSR
Bipolar Zero Tempco	—	±5	±10	ppm/°C
Bipolar Offset Error, +25°C	—	±0.1	±0.25	%FSR
Bipolar Offset Tempco	—	±20	±40	ppm/°C
Gain Error, +25°C	—	±0.1	±0.25	%
Gain Tempco	—	±20	±40	ppm/°C
Harmonic Distortion (–FS)				
(DC to 5kHz, 10Vp-p) ①	—	–73	–65	dB
No Missing Codes	Over operating temperature range			
SIGNAL TIMING				
$\overline{\text{Enable}}$ to Data Valid Delay	—	—	10	ns
MUX Address Set-up Time	400	—	—	ns
Start Convert Pulse Width	50	100	—	ns
Data Valid After				
EOC Signal Goes Low	—	—	20	ns
Conversion Time, +25°C	—	—	800	ns
0 to +70°C	—	—	850	ns
–55 to +125°C	—	—	880	ns
Throughput Rates ①				
Gain = 1	400	—	—	kHz
Gain = 2	325	—	—	kHz
Gain = 4	275	—	—	kHz
Gain = 8	225	—	—	kHz
Gain = 10	175	—	—	kHz
Gain = 100	40	—	—	kHz
S/H PERFORMANCE				
Acquisition Time				
Full-Scale Step to ±0.01%	—	500	900	ns
Full-Scale Step to ±0.1%	—	400	750	ns
Aperture Delay	–50	–20	0	ns
Aperture Uncertainty	—	—	±150	ps
Slew Rate	±70	±90	—	V/µs
Hold Mode Settling Time				
To ±1mV	—	100	200	ns
To ±10mV	—	75	150	ns
Feedthrough Rejection	80	88	—	dB
Droop Rate ①	—	±0.1	±100	µV/µs
POWER SUPPLIES				
Range, +15V Supply	+14.25	+15.0	+15.75	Volts
–15V Supply	–14.25	–15.0	–15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Current, +15V Supply	—	+78	+90	mA
–15V Supply	—	–72	–82	mA
+5V Supply	—	+75	+95	mA
Power Dissipation	—	2.6	3	Watts
Power Supply Rejection	—	—	±0.05	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Oper. Temp. Range, Case, -MC,	0	—	+70	°C
-MM, 883	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type	40-pin ceramic DDIP			
Weight	0.56 ounces (16 grams)			

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HDAS-524/528 OPERATION (Continued)

of the START CONVERT pulse for continuous operation. Higher gains require the use of the R_{GAIN} resistor to increase the acquisition time. The gain is equal to 1 without an R_{GAIN} resistor. Table 2 refers to the appropriate R_{GAIN} resistors for various throughputs.

The HDAS devices enter the hold mode and are ready for conversion upon the start convert going high. The conversion is complete within a maximum of 800ns (+25°C). $\overline{EOC}$ returns low, the data is valid and sent to the three-state output buffers. The sample/hold is now ready to acquire new data.

Table 1. MUX Channel Addressing

MUX ADDRESS PINS 39 CA2	38 CA1	37 CA0	CHANNEL	
0	0	0	0	
0	0	1	1	HDAS-524
0	1	0	2	(2-BIT ADDRESS)
0	1	1	3	
1	0	0	4	
1	0	1	5	HDAS-528
1	1	0	6	(3-BIT ADDRESS)
1	1	1	7	

Table 2. Input Range Parameters

INPUT RANGE	GAIN	R_{GAIN}	THROUGHPUT
0 to +10V	1	OPEN	400kHz
0 to +5V	2	2kΩ	325kHz
0 to +2.5V	4	665Ω	275kHz
0 to +1.25V	8	287Ω	225kHz
0 to +1V	10	221Ω	175kHz
0 to +100mV	100	20Ω	40kHz
±10V	1	OPEN	400kHz
±5V	2	2kΩ	325kHz
±2.5V	4	665Ω	275kHz
±1.25V	8	287Ω	225kHz
±1V	10	221Ω	175kHz
±100mV	100	20Ω	40kHz

$$R_{GAIN} = \frac{2k\Omega}{(GAIN - 1)} \qquad GAIN = \frac{2k\Omega}{R_{GAIN}} + 1$$

Table 3. Zero and Gain Adjust

INPUT RANGE	ZERO ADJUST +1/2LSB	GAIN ADJUST +FS – 1 1/2LSB
0 to +10V	+1.22mV	+9.9963V
±10V	+2.44mV	+9.9927V

CALIBRATION PROCEDURE

1. Connect the converter per Figure 2 and Tables 2 and 3 for the appropriate input range. Apply a pulse of 100 nanoseconds (typical) to the START CONVERT input (pin 40) at a rate of 100kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. Zero Adjustments

   Apply a precision voltage reference source between the analog input and SIGNAL GROUND (pin 14). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the $\overline{COMP\ BIN}$ (pin 9) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the $\overline{COMP\ BIN}$ (pin 9) tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with $\overline{COMP\ BIN}$ (pin 9) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with $\overline{COMP\ BIN}$ (pin 9) tied low (complementary offset binary).
3. Full-Scale Adjustment

   Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 or 0000 0000 0001 and 0000 0000 0000 for complementary coding.
4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

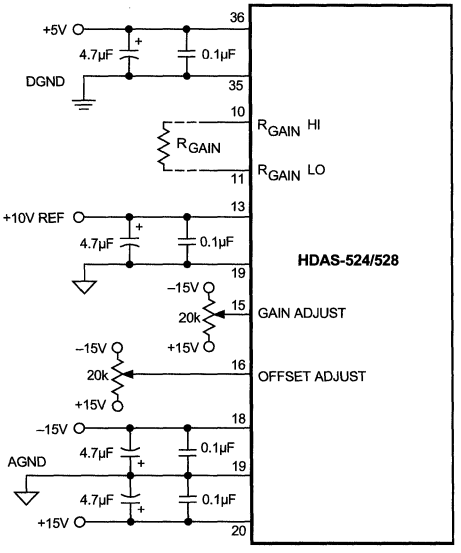

Figure 2. Typical Connection Diagram

Notes:

1. For unipolar operation, connect pin 12 to pin 17.
2. For bipolar operation, connect pin 13 to pin 17.
3. Position R_{GAIN} as close as possible to pins 10 and 11. Use RN55C, 1% resistors.
4. If gain and offset adjusts are not used, connect pin 15 to ground and leave pin 16 open.

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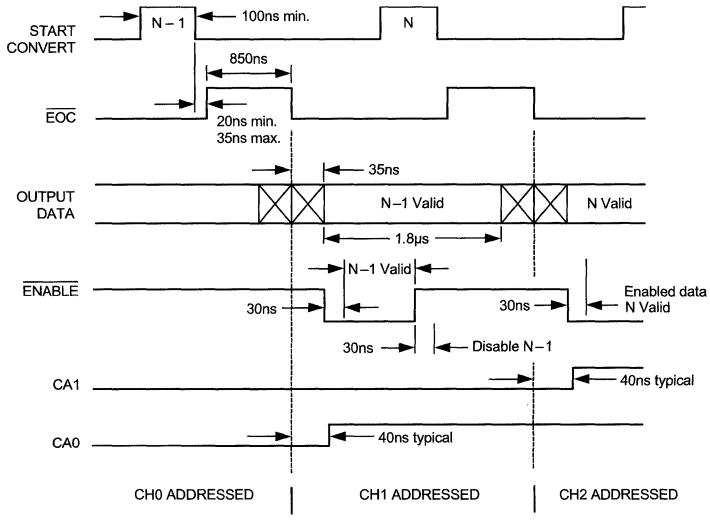
TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital ground pins are not connected to each other internally. Avoid ground-related problems by connecting the analog, signal and digital grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital grounds separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

2. Double-level multiplexing allows expanding the multiplexer channel capacity of the HDAS-528 from 8 single-ended channels to 128 single-ended channels or the HDAS-524 from 4 differential channels to 32 differential channels.

3. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 9) to +5V or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 9 to ground. The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 34) to a logic "0" (low). To disable, connect pin 34 to a logic "1" (high).



Notes:

1. A START CONVERT pulse greater than 150ns will slow the throughput.
2. Retriggering START CONVERT before $\overline{\text{EOC}}$ goes low will not start a new conversion.
3. Times shown apply over the 0 to +70°C operating temperature range.

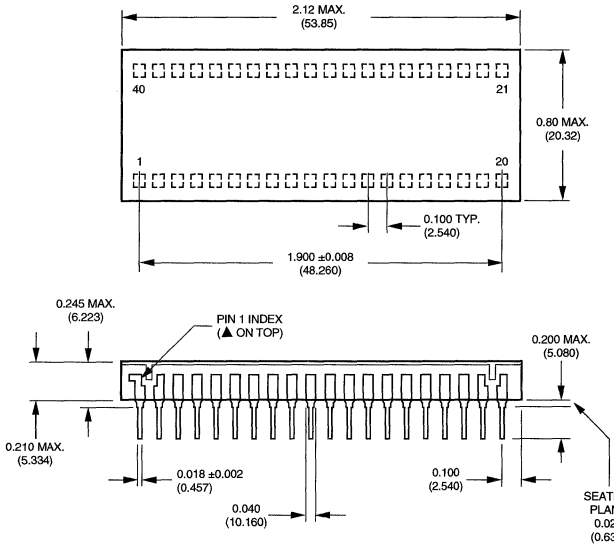
Figure 3. HDAS-524/528 Timing Diagram

Table 4. Output Coding

		STRAIGHT BINARY	COMP. BINARY		
UNIPOLAR SCALE	**INPUT RANGE 0 to +10V**	**OUTPUT CODING MSB LSB**	**MSB LSB**	**INPUT RANGE ±10V**	**BIPOLAR SCALE**
+FS – 1LSB	+9.9976V	1111 1111 1111	0000 0000 0000	+9.9951V	+FS – 1LSB
+7/8FS	+8.7500V	1110 0000 0000	0001 1111 1111	+7.5000V	+3/4FS
+3/4FS	+7.5000V	1100 0000 0000	0011 1111 1111	+5.0000V	+1/2FS
+1/2FS	+5.0000V	1000 0000 0000	0111 1111 1111	0.0000V	0
+1/4FS	+2.5000V	0100 0000 0000	1011 1111 1111	–5.0000V	–1/2FS
+1/8FS	+1.2500V	0010 0000 0000	1101 1111 1111	–7.5000V	–3/4FS
+1LSB	+0.0024V	0000 0000 0001	1111 1111 1110	–9.9951V	–FS + 1LSB
0	0.0000V	0000 0000 0000	1111 1111 1111	–10.0000V	–FS
		OFFSET BINARY	COMP. OFF. BINARY		

8

MECHANICAL DIMENSIONS
INCHES (mm)



40-PIN DDIP

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NO.	INPUT	OPERATING TEMP. RANGE
HDAS-524MC	4D Channels	0 to +70°C
HDAS-524MM	4D Channels	–55 to +125°C
HDAS-528MC	8SE Channels	0 to +70°C
HDAS-528MM	8SE Channels	–55 to +125°C
HDAS-528/883	8SE Channels	–55 to +125°C

Receptacle for PC board mounting can be ordered through AMP Inc., Part #3-331272-8 (Component Lead Socket), 40 required.

Contact DATEL, Inc. for MIL-STD-883 product specifications.

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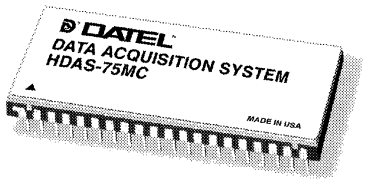
INNOVATION and EXCELLENCE

HDAS-75, HDAS-76
12-Bit, 75kHz, Complete Data Acquisition Systems

FEATURES

- **12-Bit resolution, 75kHz throughput**
- **8 Channels single-ended or 4 channels differential**
- **Miniature 40-pin DDIP**
- **Full-scale input range from 100mV to 10V**
- **High-impedance output state**
- **No missing codes**



GENERAL DESCRIPTION

The HDAS-75 and HDAS-76 are complete data acquisition systems. Each contains an internal multiplexer, instrumentation amplifier, sample-hold, analog-to-digital converter and three-state outputs. Packaged in miniature, 40-pin, double-dip packages and requiring ±15V and +5V supplies, each system dissipates a mere 500 milliwatts.

The HDAS-76 provides 4 differential inputs, and the HDAS-75 provides 8 single-ended inputs. An internal instrumentation amplifier is characterized for gains of 1, 2, 4, 8, 10 and 100. The gain range is selectable through an external resistor.

TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital ground pins are connected to each other internally. Avoid ground-related problems by connecting the analog, signal and digital grounds to one point, the ground plane beneath the converter.
2. Double-level multiplexing allows expanding the multiplexer channel capacity of the HDAS-75 from 8 to 128 single-ended channels or the HDAS-76 from 4 to 32 differential channels.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH0/CH0 HI	40	START CONVERT
2	CH1/CH1 HI	39	CA2
3	CH2/CH2 HI	38	CA1
4	CH3/CH3 HI	37	CA0
5	CH7/CH3 LO	36	+5V SUPPLY
6	CH6/CH2 LO	35	DIGITAL GROUND
7	CH5/CH1 LO	34	DIGITAL GROUND
8	CH4/CH0 LO	33	BIT 1 (MSB
9	NO CONNECTION	32	BIT 2
10	RGAIN LO	31	BIT 3
11	RGAIN HI	30	BIT 4
12	INST. AMP OUT	29	BIT 5
13	+10V REFERENCE OUT	28	BIT 6
14	SIGNAL GROUND	27	BIT 7
15	GAIN ADJUST	26	BIT 8
16	OFFSET ADJUST	25	BIT 9
17	BIPOLAR	24	BIT 10
18	–15V SUPPLY	23	BIT 11
19	ANALOG GROUND	22	BIT 12 (LSB)
20	+15V SUPPLY	21	$\overline{EOC}$

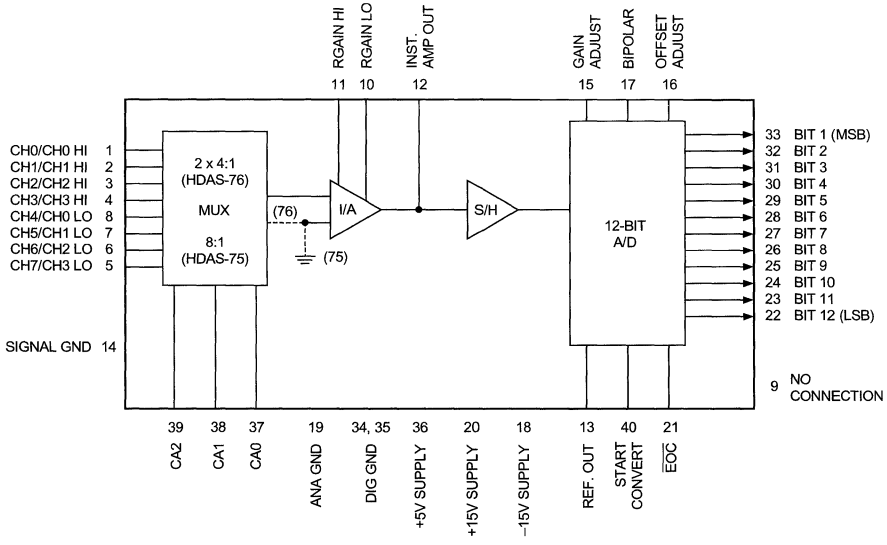


Figure 1. Functional Block Diagram

8

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MIN.	TYP.	MAX.	UNITS
+15V Supply, Pin 20	0	—	+18	Volts
–15V Supply, Pin 18	0	—	–18	Volts
+5V Supply, Pin 36	–0.5	—	+7	Volts
Digital Inputs, Pins 37–40	–0.3	—	+6	Volts
Analog Inputs, Pins 1–8	–25	—	+25	Volts
Lead Temperature (10 seconds)	—	—	300	°C

FUNCTIONAL SPECIFICATIONS

(Apply over the operating temperature range with ±15V and +5V supplies unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Inputs				
HDAS-75	8 single-ended inputs			
HDAS-76	4 differential inputs			
Input Voltage Ranges				
Gain = 1	0 to +10V, ±10V			
Gain = 100	0 to +100mV, ±100mV			
I.A. Gain Ranges	1, 2, 4, 8, 10, 100			
Input Impedance				
CH On, CH Off	10^{11}	10^{12}	—	Ohms
Input Capacitance				
(-75) CH On, CH Off	—	—	25	pF
(-76) CH On, CH Off	—	—	12	pF
Input Bias Current	—	—	±200	pA
Input Offset Current	—	—	±50	pA
Input Offset Voltage	—	—	±10	mV
Common Mode Voltage Range	±11	—	—	V
CMRR, G = 1, @10Hz, Vcm = 1Vp-p	75	80	—	dB
Voltage Noise (RMS)				
Gain = 1	—	—	200	µV
Gain = 8	—	—	50	µV
MUX Crosstalk @125kHz	—	—	–72	dB
MUX ON Resistance	—	450	500	Ohms
Bias Current Tempco	Doubles (max.) every 10°C above +70°C			
Offset Current Tempco	Doubles (max.) every 10°C above +70°C			
Offset Voltage Tempco	(±30ppm/°C x gain) ±20ppm/°C (max.)			
Input Gain Equation	$G = \frac{2k\Omega}{Rgain} + 1$			
DIGITAL INPUTS				
Logic Levels				
Logic 1	+2.4	—	—	Volts
Logic 0	—	—	+0.8	Volts
Logic Loading				
Logic 1	—	—	+30	µA
Logic 0	—	—	–30	µA
OUTPUTS				
Logic Levels				
Logic 1	+2.4	—	—	Volts
Logic 0	—	—	+0.4	Volts
Logic Loading				
Logic 1	—	—	–500	µA
Logic 0	—	—	+1.6	mA
Internal Reference				
Voltage, +25°C	+9.9	+10.0	+10.1	Volts
Drift	—	±5	±35	ppm/°C
External Current	—	—	1.5	mA
Output Coding	Straight binary/Offset binary			

Footnotes:

① Specifications valid at +25°C and over the temperature ranges of 0 to +70°C or –55 to +125°C.

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Resolution	12	—	—	Bits
Integral Nonlinearity, +25°C	—	—	±1	LSB
0 to +70°C	—	—	±1	LSB
–55 to +125°C	—	—	±1.5	LSB
Differential Nonlinearity, +25°C	—	—	±1	LSB
0 to +70°C	—	—	±1	LSB
–55 to +125°C	—	—	±1	LSB
F.S. Abs. Accuracy, +25°C	—	±0.13	±0.3	%FSR
0 to +70°C	—	±0.15	±0.5	%FSR
–55 to +125°C	—	±0.25	±0.78	%FSR
Unipolar Zero Error, +25°C	—	±0.074	±0.15	%FSR
Unipolar Zero Tempco	—	±15	±30	ppm/°C
Bipolar Zero Error, +25°C	—	±0.074	±0.15	%FSR
Bipolar Zero Tempco	—	±5	±10	ppm/°C
Bipolar Offset Error, +25°C	—	±0.1	±0.25	%FSR
Bipolar Offset Tempco	—	±20	±40	ppm/°C
Gain Error, +25°C	—	±0.1	±0.25	%
Gain Tempco	—	±20	±40	ppm/°C
Harmonic Distortion (–FS)				
(DC to 5kHz, 10Vp-p) ①	—	–73	–65	dB
No Missing Codes	Over operating temperature range			
SIGNAL TIMING				
MUX Address Set-up Time	400	—	—	ns
Start Convert Pulse Width	0.05	1	—	µs
Data Valid Before				
$\overline{EOC}$ Signal Goes Low	300	—	—	ns
Conversion Time, +25°C	—	—	12	µs
0 to +70°C	—	—	13	µs
–55 to +125°C	—	—	13	µs
Throughput Rates ①				
Gain = 1	75	80	—	kHz
Gain = 2	60	70	—	kHz
Gain = 4	50	60	—	kHz
Gain = 8	45	50	—	kHz
Gain = 10	40	45	—	kHz
Gain = 100	10	20	—	kHz
S/H PERFORMANCE				
Acquisition Time				
Full-Scale Step to ±0.01%	—	1.4	1.8	µs
Full-Scale Step to ±0.1%	—	0.8	1.4	µs
Aperture Delay	–50	–20	0	ns
Aperture Uncertainty	—	—	±200	ps
Slew Rate	±70	±90	—	V/µs
Hold Mode Settling Time				
To ±1mV	—	200	400	ns
To ±10mV	—	150	300	ns
Feedthrough Rejection	80	88	—	dB
Droop Rate ①	—	—	±100	µV/µs
POWER SUPPLIES				
Range, +15V Supply	+14.25	+15.0	+15.75	Volts
–15V Supply	–14.25	–15.0	–15.75	Volts
+5V Supply	+4.75	+5.0	+5.25	Volts
Current, +15V Supply	—	+15	+20	mA
–15V Supply	—	–10	–15	mA
+5V Supply	—	+25	+35	mA
Power Dissipation	—	500	700	mW
Power Supply Rejection	—	—	±0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Oper. Temp. Range, Case, -MC	0	—	+70	°C
-MM, 883	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type	40-pin ceramic DDIP			
Weight	0.32 ounces (9 grams)			

HDAS-75/76 OPERATION

The HDAS devices accept either 8 single-ended or 4 differential input signals. Tie unused channels to SIGNAL GROUND, pin 14.

Channel selection is accomplished using the multiplexer address pins as shown in Table 1. Obtain additional channels by connecting external multiplexers.

The acquisition time is the amount of time the multiplexer, instrumentation amplifier and sample-hold require to settle within a specified range of accuracy after the start convert goes high. The acquisition time can be measured by how long $\overline{EOC}$ is low before the rising edge of the START CONVERT pulse for continuous operation. Higher gains require the use of the R_{GAIN} resistor to increase the acquisition time. The gain is equal to 1 without an R_{GAIN} resistor. Table 2 refers to the appropriate R_{GAIN} resistors for various throughputs.

Table 1. MUX Channel Addressing

MUX ADDRESS PINS 39 CA2	38 CA1	37 CA0	CHANNEL	
0	0	0	0	
0	0	1	1	HDAS-76
0	1	0	2	(2-BIT ADDRESS)
0	1	1	3	
1	0	0	4	
1	0	1	5	HDAS-75
1	1	0	6	(3-BIT ADDRESS)
1	1	1	7	

Table 2. Input Range Parameters

INPUT RANGE	GAIN	R_{GAIN}	THROUGHPUT
0 to +10V	1	OPEN	75kHz
0 to +5V	2	2kΩ	60kHz
0 to +2.5V	4	665Ω	50kHz
0 to +1.25V	8	287Ω	45kHz
0 to +1V	10	221Ω	40kHz
0 to +100mV	100	20Ω	10kHz
±10V	1	OPEN	75kHz
±5V	2	2kΩ	60kHz
±2.5V	4	665Ω	50kHz
±1.25V	8	287Ω	45kHz
±1V	10	221Ω	40kHz
±100mV	100	20Ω	10kHz

$$R_{GAIN} = \frac{2k\Omega}{(GAIN - 1)} \qquad GAIN = \frac{2k\Omega}{R_{GAIN}} + 1$$

Table 3. Zero and Gain Adjust

INPUT RANGE	ZERO ADJUST +1/2LSB	GAIN ADJUST +FS – 1 1/2LSB
0 to +10V	+1.22mV	+9.9963V
±10V	+2.44mV	+9.9927V

CALIBRATION PROCEDURE

1. Connect the converter per Figure 2 and Tables 2 and 3 for the appropriate input range. Apply a pulse of 1µs (typical) to the START CONVERT input (pin 40) at a rate of 75kHz. This rate is chosen to reduce flicker if LEDs are used on the outputs for calibration purposes.
2. Zero Adjustments

   Apply a precision voltage reference source between the analog input and SIGNAL GROUND (pin 14). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001.
3. Full-Scale Adjustment

   Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.
4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

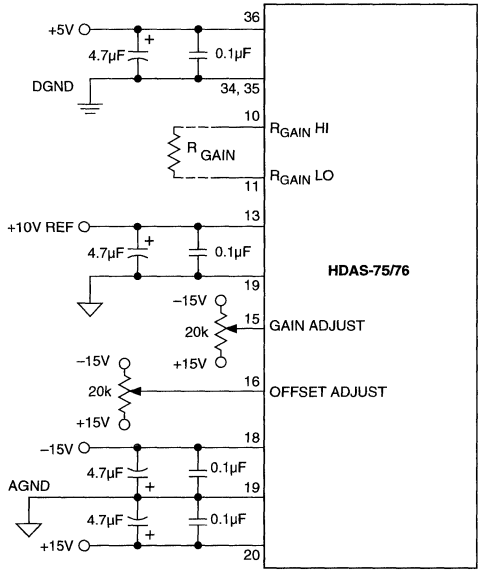


Figure 2. Typical Connection Diagram

Notes:

1. For unipolar operation, connect pin 12 to pin 17.
2. For bipolar operation, connect pin 13 to pin 17.
3. Ground pin 15 if gain adjust is not used.
4. Leave pin 16 open if offset adjust is not used.
5. Position R_{GAIN} as close as possible to pins 10 and 11. Use RN55C, 1% resistors.

8

TIMING

The $\overline{EOC}$ output signal, when high, indicates that a conversion is in process. During a conversion, the digital output buffers are in a high-impedance state, preventing data from being read. A START CONVERT input received during a conversion has no effect on the existing conversion. As shown in Figure 3, data can be read while START CONVERT is high and $\overline{EOC}$ is low.

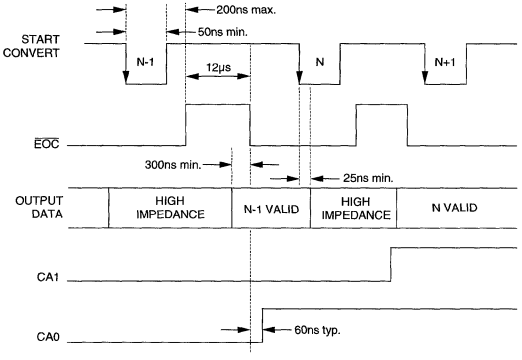


Figure 3. Data Valid with START CONVERT Immediately Returned High

The A/D conversion begins on the falling edge of a start convert command. If START CONVERT stays low after $\overline{EOC}$ becomes low, the output buffers stay in a high-impedance state. Valid data can be read 150ns maximum after START CONVERT goes high. Figure 4 shows how to use the START CONVERT pulse to control when the output data becomes valid.

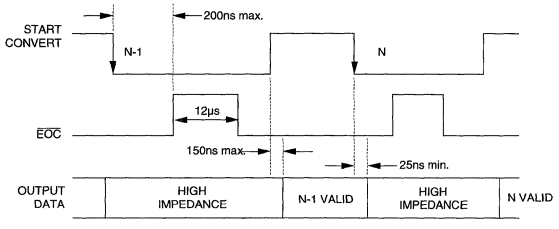


Figure 4. Data Valid with START CONVERT Returned High Later

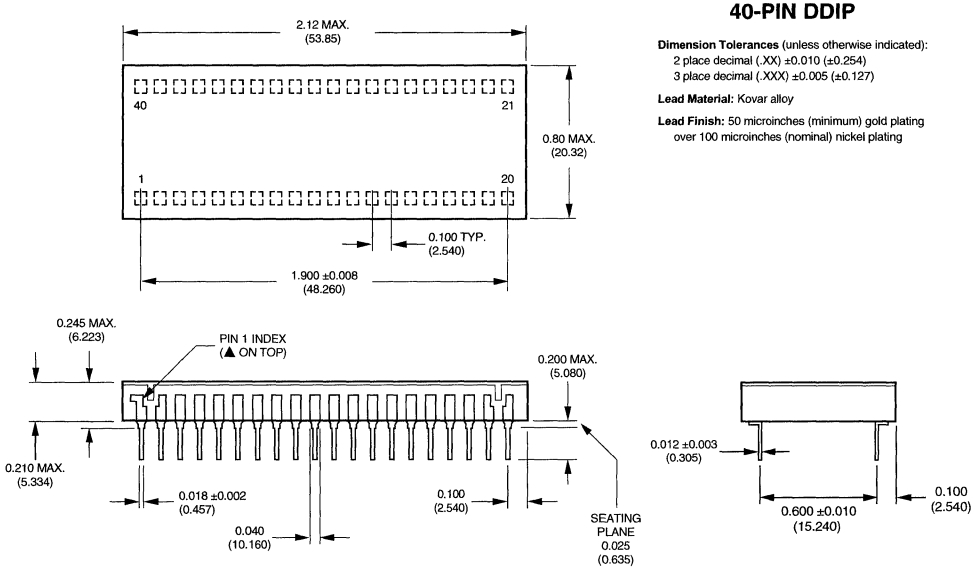
Notes:

1. A START CONVERT pulse greater than 5µs will slow the overall throughput.
2. Retriggering START CONVERT before $\overline{EOC}$ goes low will not initiate a new conversion.
3. Timing specifications apply over the full operating temperature range.

Table 4. Output Coding

		STRAIGHT BINARY		
UNIPOLAR SCALE	**INPUT RANGE 0 to +10V**	**OUTPUT CODING MSB LSB**	**INPUT RANGE ±10V**	**BIPOLAR SCALE**
+FS – 1LSB	+9.9976V	1111 1111 1111	+9.9951V	+FS – 1LSB
+7/8FS	+8.7500V	1110 0000 0000	+7.5000V	+3/4FS
+3/4FS	+7.5000V	1100 0000 0000	+5.0000V	+1/2FS
+1/2FS	+5.0000V	1000 0000 0000	0.0000V	0
+1/4FS	+2.5000V	0100 0000 0000	–5.0000V	–1/2FS
+1/8FS	+1.2500V	0010 0000 0000	–7.5000V	–3/4FS
+1LSB	+0.0024V	0000 0000 0001	–9.9951V	–FS + 1LSB
0	0.0000V	0000 0000 0000	–10.000V	–FS
		OFFSET BINARY		

MECHNICAL DIMENSIONS
INCHES (mm)



40-PIN DDIP

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NO.	INPUT	OPERATING TEMP. RANGE
HDAS-75MC	8SE Channels	0 to +70°C
HDAS-75MM	8SE Channels	–55 to +125°C
HDAS-75/883	8SE Channels	–55 to +125°C
HDAS-76MC	4D Channels	0 to +70°C
HDAS-76MM	4D Channels	–55 to +125°C
HDAS-76/883	4D Channels	–55 to +125°C

Receptacles for PC board mounting can be ordered through AMP Inc., Part #3-331272-8 (Component Lead Socket), 40 required.

Contact DATEL, Inc. for MIL-STD-883 product specifications.

8

Other DATEL Products

ISO 9001
REGISTERED

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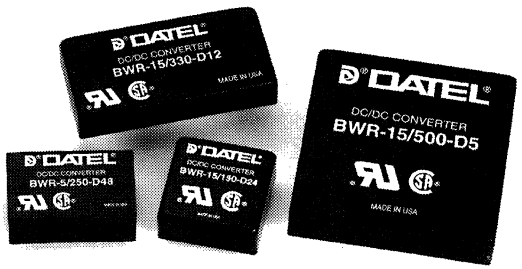

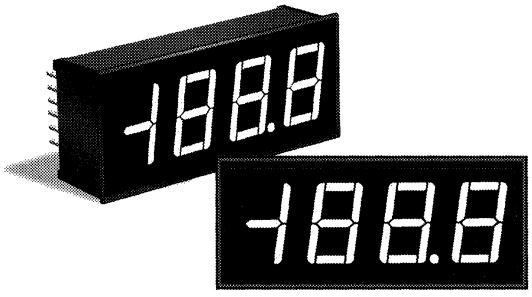

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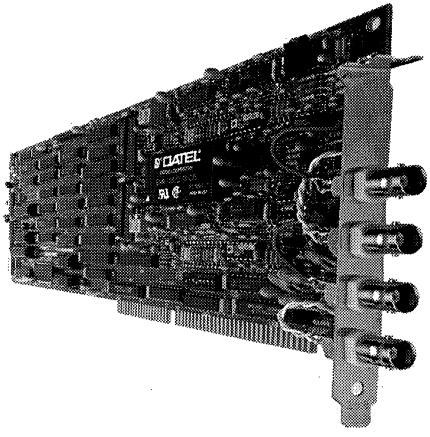
  - Arbitrary waveform generators (2-16 channels)
  - Programmable power supplies
  - Power-supply test cards
- Windows and LabVIEW® bridge software



For literature or technical assistance

800-233-2765

or contact your local DATEL Sales Office or Representative

Tunable Active Filters

Table of Contents

Selection Guide

Model	Tuning Technique	Poles	Filter Type ①	Low Pass	High Pass	Band Pass	Band Reject	Rolloff (dB/Octave)	Frequency Cutoff Range (f_C)	Page
FLT-U2 ②	Resistors	2	BU, CH, BE, CA	X	X	X		12	0.001Hz-200kHz	**9-11**
FLJ-D Series	3-Digit BCD	2	BU, CH, BE	X	X	X	X	12	0.1Hz-160kHz	**9-2**
FLJ-UR Series	Resistors	2, 4	BU, CH	X	X	X	X	12, 24, 42	40Hz-20kHz	**9-2**
FLJ-V Series	Voltage	4	BU	X	X	X		12, 24	20Hz-100kHz	**9-2**
FLJ-HR Series ③	Resistors	2, 4	BU, CH, BE, CA	X	X	X		12, 24, 42	10Hz-100kHz	**9-3**
FLJ-D5/D6	3-Bit Binary	5, 6	CH	X				60, 80	10Hz-20kHz	**9-2**
FLJ-R Series	Resistors	6, 8	CA	X		X		100, 135	10Hz-20kHz	**9-2**

Listed specifications are typical at T_A = +25°C, with nominal supplies, unless otherwise indicated.
① BU = Butterworth, BE = Bessel, CA = Cauer/elliptical, CH = Chebyshev
② Commercial and military temperature ranges available.
③ High-reliability and military temperature range models available.

Digitally Programmable and Resistor/Voltage-Tunable Active Filters

	Digitally Programmable		Voltage-Tunable	Resistor-Tunable	
Parameter ①	**FLJ-DC, D1, D2 Models**	**FLJ-D5, D6 Models**	**FLJ-VL, VB, VH Models**	**FLJ-R Series**	**FLJ-UR Series**
Frequency Control	3-Digit BCD	3-Bit Binary	FLJ-VL/VH, 0.01-10V FLJ-VB, 0.1-10V	6 or 8 Resistors	2 or 4 Resistors
Filter Characteristics	LP, HP, BP, BR	LP	FLJ-VL, LP BU BE FLJ-VB, BP BU FLJ-VH, HP BU	See below	See below
Filter Types	CH, BE, BU	CH			
Frequency Range	FLJ-DC, 0.1Hz-159.9kHz FLJ-D1, 1.0Hz-1.599kHz FLJ-D2, 100Hz-159.9kHz	Suffix "1" Models, 10Hz-2kHz Suffix "2" Models, 100Hz-20kHz	FLJ-VL, 100Hz-100kHz FLJ-VB, 200Hz-20kHz FLJ-VH, 20Hz-20kHz	See below	See below
Input/Output Range	±10 Volts	±10 Volts	FLJ-VL/VH, ±10 Volts FLJ-VB, ±2 Volts	±10 Volts	±10 Volts
Input Impedance	300kΩ	50kΩ min.	50kΩ min.	50kΩ min.	50kΩ min.
Gain	–1 to –10	1	1	1	1
Number of Poles	2 (1-pole pair)	FLJ-D5LA1/2, 5 FLJ-D6LA1/2, 6	FLJ-VL/VH, 4 FLJ-VB, 2-pole pair	See below	See below
Rolloff	LP/HP, 12dB/octave BP/BR 6dB/octave	FLJ-D5LA1/2, 60dB/octave FLJ-D6LA1/2, 80dB/octave	FLJ-VL/VH, 24dB/octave FLJ-VB, 12dB/oct. (Q=5)	See below	See below
Attenuation Volume	—	FLJ-D5LA1/2, 60dB (1.8fc) FLJ-D6LA1/2, 74dB (1.9fc)	—	See below	See below
Q	$1/3 < Q < 10^6/fc$	—	FLJ-VB, Q = 5	See below	See below
Noise	HP, 100μVrms LP, 35μVrms BP, 30μVrms	140μVrms max.	300μVrms	140μVrms max.	140μVrms max.
Ripple	—	0.13dBp-p	—	0.15dBp-p	0.28dBp-p (CH)
Distortion	0.002%	0.05%	0.1% max.	See below	See below
Slew Rate	±8V/μsec	—	—	—	±2V/μsec
Supply Voltages	+5, ±15 Volts	±15 Volts	±15 Volts	±15 Volts	±15 Volts
Power Dissipation	780mW	990mW max.	1080mW	975mW	240-600mW
Operating Temp.	–20 to +70°C	–20 to +70°C	–20 to +70°C	–20 to +70°C	–20 to +70°C
Package	40-pin QDIP	40-pin QDIP	40-pin QDIP	40-pin QDIP	20-pin SIP

Support Products: FLJ-ACO1 Oscillator Adapter for the FLJ-DC, D1 and D2. FLJ-ACR1/2 BCD Logic Controlled Resistor Networks for FLJ-UR Series.

FLJ-R/UR Series

Model	Characteristic and Type	Frequency Range Suffix "1" Models	Frequency Range Suffix "2" Models	Poles	Rolloff (dB/octave)	Distortion (%)	Q	Attenuation Volume
FLJ-R3BA1/2	BP, CA	10Hz-2kHz	100Hz-20kHz	3-pole pair	-	0.005	4.3	18dB/oct.
FLJ-R8LA1/2	LP, CA	10Hz-2kHz	100Hz-20kHz	8	135	0.005	-	86dB (1.6fc)
FLJ-R8LB1/2	LP, CA	10Hz-2kHz	100Hz-20kHz	8	100	0.005	-	92dB (2fc)
FLJ-UR4LA1/2	LP, BU	40Hz-1.6kHz	400Hz-20kHz	4	24	0.01	-	24dB (2fc)
FLJ-UR4LB1/2	LP, CH	40Hz-1.6kHz	400Hz-20kHz	4	42	0.01	-	55dB (2fc)
FLJ-UR4HA1/2	HP, BU	40Hz-1.6kHz	400Hz-5kHz	4	24	0.1	-	24dB (0.5fc)
FLJ-UR4HB1/2	HP, CH	40Hz-1.6kHz	400Hz-5kHz	4	42	0.1	-	55dB (0.5fc)
FLJ-UR2LH1/2	LP, BU	40Hz-1.6kHz	400Hz-20kHz	2	12	0.1	-	12dB (2fc)
FLJ-UR1BA1/2	BP, BU	40Hz-1.6kHz	400Hz-10kHz	1-pole pair	-	0.01	1.8-50	17.5dB ②
FLJ-UR2BA1/2	BP, BU	40Hz-1.6kHz	400Hz-10kHz	2-pole pair	-	0.01	5	35dB ②
FLJ-UR2EA1/2	BR, BU	40Hz-1.6kHz	400Hz-10kHz	2-pole pair	-	0.01	5	—

① Characteristics: LP = Lowpass, HP = Highpass, BP = Bandpass, BR = Bandreject (notch)
Types: CH = Chebyshev, BE = Bessel, BU = Butterworth, CA = Cauer/Elliptical

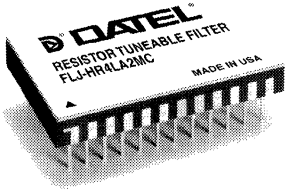
② For bandpass filters, attenuation volume spec applies at both 2fc and 0.5fc.

DATEL®
INNOVATION and EXCELLENCE

FLJ-HR Series
Resistor-Tunable Active Filter

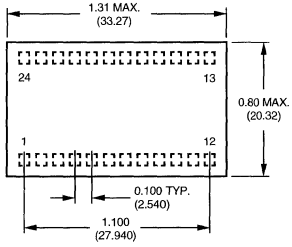
FEATURES

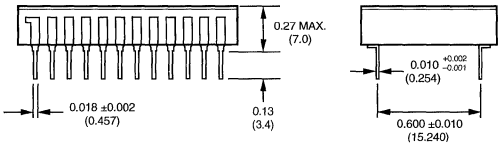
- **Cutoff or center frequency is set by only four resistors**
- **High-reliability (QL) versions**
- **Wide operating temperature ranges**
- **Small, 24-pin ceramic DDIP package**
- **A variety of functions and families**



GENERAL DESCRIPTION

DATEL's FLJ-HR Series are a new type of resistor-tunable active filters designed to have long life and high-reliability features. The FLJ-HR Series are packaged in 24-pin ceramic DDIP's and operate over the –40 to +85°C (MC version) temperature range. Units that operate over the –55 to +125°C military temperature range (MM versions) and devices with high-reliability screening (-QL versions) are also available. All versions have passed very severe qualification tests to prove their high reliability and longevity. The FLJ-HR Series employ state-variable methods, as does DATEL's FLJ-UR Series, to allow system designers to expand their functions. The cutoff or center frequency can easily be set by only four external resistors.





MECHANICAL DIMENSIONS
Inches (mm)

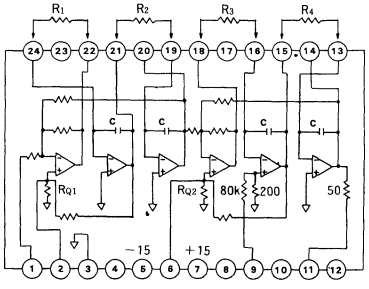
Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

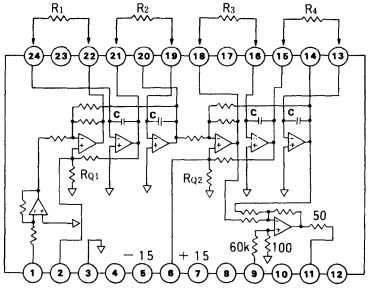
Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

BLOCK DIAGRAMS

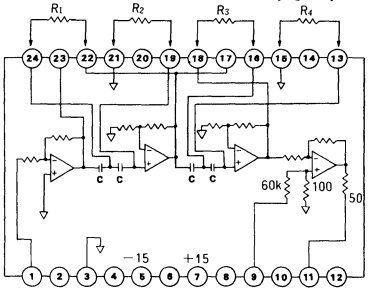
FLJ-HR4LA1/2
4-POLE LOWPASS BUTTERWORTH (Fig.1-1)



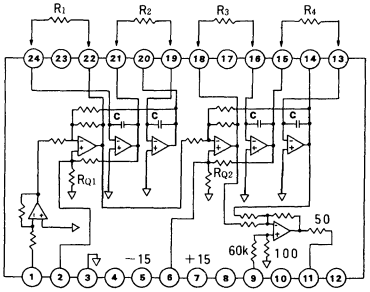
FLJ-HR4LB1/2
4-POLE LOWPASS CAUER (Fig.1-2)



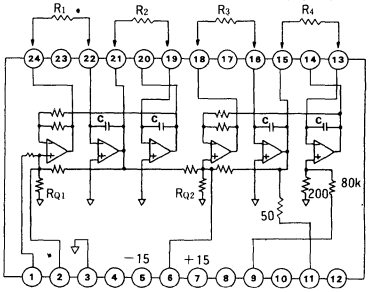
FLJ-HR4HA1/2
4-POLE HIGHPASS BUTTERWORTH (Fig.1-3)



FLJ-HR4HB1/2
4-POLE HIGHPASS CAUER (Fig.1-4)



FLJ-HR2BA1/2
2-POLE PAIR BANDPASS BUTTERWORTH (Fig.1-5)



9

SPECIFICATIONS

Typical at Rf=31.8kΩ, +25°C and ±15Vdc supplies unless otherwise specified.

COMMON SPECIFICATIONS TO ALL MODELS

ABSOLUTE RATINGS

Supply voltage (±Vs) ..... ±18V
Input voltage ..... ±Vs

FREQUENCY CHARACTERISTICS

fc accuracy ..... ±3% max.
fc setting ..... By 4 external Rf resistors

INPUT CHARACTERISTICS

Input Impedance ..... 50kΩ min.
Input Voltage ..... ±10V min.

OUTPUT CHARACTERISTICS

Output Impedance ..... 100Ω max.
Output Voltage ..... ±10V min.
Load Resistance ..... 10kΩ min.
Offset Voltage ..... ±30mV max. Zero adjustable

POWER SUPPLY, TEMPERATURE RANGE AND PACKAGE

Supply Voltage ..... ±15V
Supply Voltage Range ..... Suffix 1 model ..... ±1.5V to ±18V
Supply Voltage Range ..... Suffix 2 model ..... ±5V to ±18V
Operating Temperature -MC ..... -40°C to +85°C
Operating Temperature -MM ..... -55°C to +125°C
Storage Temperature ..... -65°C to+150°C
Package ..... 24-pin DDIP

Poles/characteristics		4-pole lowpass	4-pole lowpass	4-pole highpass	4-pole highpass	2-pole pair bandpass
Type		Butterworth	Cauer	Butterworth	Cauer	Butterworth
Model		FLJ-HR4LA1/2	FLJ-HR4LB1/2	FLJ-HR4HA1/2	FLJ-HR4HB1/2	FLJ-HR2BA1/2
fc(-3dB) characteristics						
Range	Suffix 1 model	10Hz to 1.6kHz	*Same as left	*Same as left	*Same as left	*Same as left
	Suffix 2 model	100Hz to 100kHz	*	100Hz to 50kHz	*	*
Pass band characteristics						
Gain	fc < 20kHz	0±0.3dB max.	*	0±0.5dB max.	*	0±1dB max.
	fc ≧ 20kHz*1	0±0.3dB max.	*	0±1dB max.	*	0±2dB max.
Ripple		—	0.28dBp-p	—	0.28dBp-p	—
Upper-limit fc (small signal)	suffix 1	—	—	100kHz±1dB	*	—
	suffix 2	—	—	400kHz±1dB	*	—
Rolloff characteristics						
Rolloff		24dB/oct	42dB/oct equiv.	24dB/oct	42dB/oct equiv.	12dB/oct BW
Attenuation (1/2 fc or 2 fc)		24dB	55dB	24dB	55dB	35dB
Q		—	—	—	—	5±5%
Minimum attenuation		—	46dB	—	46dB	—
Attenuation at 1 MHz		70dB min.	60dB min.	—	—	70dB min.
Output characteristics						
Offset drift		5μV/°C	16μV/°C	10μV/°C	5μV/°C	*
Distortion rate	suffix 1	0.004%	0.01%	0.02%	0.04%	0.004%
	suffix 2	0.003%	0.005%	0.02%	*	0.002%
Slew rate	suffix 1 model	—	—	10V/μsec	*	—
	suffix 2 model	—	—	25V/μsec	*	—
Noise	suffix 1 model	100μVrms max.	150μVrms max.	200μVrms max.	300μVrms max.	100μVrms max.
	suffix 2 model	100μVrms max.	150μVrms max.	200μVrms max.	300μVrms max.	120μVrms max.
Quiescent current						
Current	Suffix 1 model	±1.5mA	±2mA	±1mA	±2mA	±1.5mA
	Suffix 2 model	±15mA	±20mA	±10mA	±20mA	±15mA

*1. suffix 2 model only

TECHNICAL NOTES

1. Do not use a switching regulator; instead, use a well-regulated ±15V power supply. Install 0.01μF ceramic and 4.7μF tantalum supply bypass capacitors in parallel as close to the filter as possible.
2. Use metal film resistors of 1% tolerance for fc setting. When making a higher-order filter, use more accurate resistors. Connect external resistors with short leads as close to the filter as possible.
3. Use external capacitors with good stability and high dielectric resistance. It is recommended to use multi-layer ceramic capacitors or plastic film capacitors.
4. The relationship between fc and external resitors/capacitors: Cutoff or center frequency can be set by 4 external resistors. The values of the 4 external resistors (Rf) can be calculated as follows for normal use.

$$Rf = \frac{15.9 \times 10^3}{fc\ (Hz)}\ (k\Omega)\quad \text{Suffix 1 model}$$

$$Rf = \frac{159 \times 10^3}{fc\ (Hz)}\ (k\Omega)\quad \text{Suffix 2 model}$$

In the applications given later, the resistance of the 4 resistors may be changed. R1 to R4 shown in the block diagrams are the external resistors explained here. The fc setting range can be expanded to a lower band by adding 4 external capacitors.

$$Rf = \frac{159}{(Cf+0.01)\,fc}\ (k\Omega)\quad \text{Suffix 1 model}$$

$$Rf = \frac{159}{(Cf+0.001)\,fc}\ (k\Omega)\quad \text{Suffix 2 model}$$

where Cf is measured in μF and fc in Hz.
See Fig. 3-1 and 3-2.

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5. How to tune fo:
   As shown in the specifications, the fc or fo setting accuracy is 3% depending on the accuracy of the elements used. There is no practical problem in tuning when they are used as a lowpass or a highpass filter. However, bandpass filters may require sharp tuning. Such filters can be tuned with external trimmers as shown in Figure 3-3 as follows:

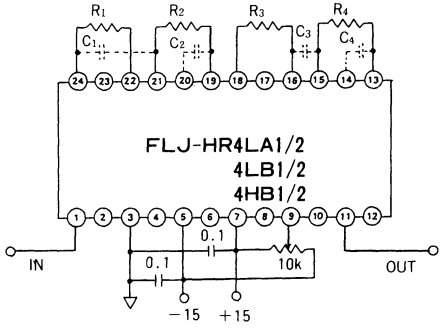
- An input signal of 1.0734 x fo is provided.
- Tune VR1 until a lissajous composed with the input signal and the output of pin 21 shows a Y = -X straight line on an oscilloscope in the XY mode.
- Then tune VR2 until a lissajous composed of the input signal and the output of pin 11 shows a Y = X straight line.

6. How to change Q value of FLJ-HR2BA1/2:
   Basically it is not recommended to change the value of Q of FLJ-HR2BA1/2. However, it is possible to change the value of Q to 10 (standard Q is 5) by adding two additional external resistors Rq1 and Rq2. It is also necessary to change the values of Rf1, Rf2, Rf3 and Rf4. See Fig. 3-4.

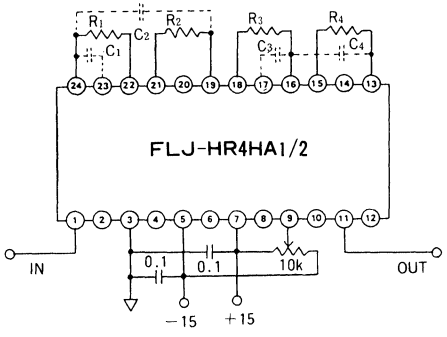
7. No offset adjustment is required when the FLJ-HR Series is used with AC coupling connections. In the case of DC coupling, offset can be adjused with an external trimmer. See Fig. 3-1, -2 and -3. All pins not used should be left open.

BASIC CONNECTIONS (Fig.3)

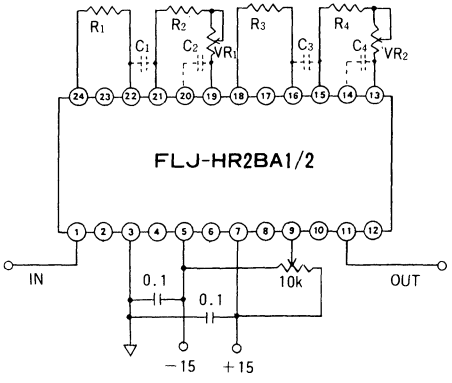
FLJ-HR4LA1/2, 4LB1/2, 4HB1/2 **(Fig.3-1)**



FLJ-HR4HA1/2 **(Fig.3-2)**

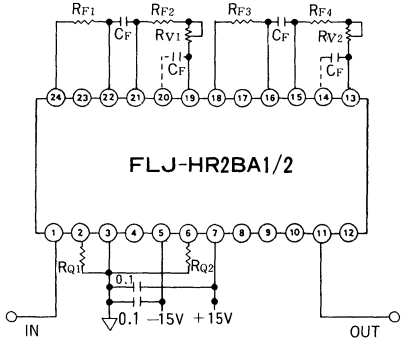


FLJ-HR2BA1/2 **(Fig.3-3)**



$R_F = R_1 = R_3$, $R_2 = R_4 = 0.95R_F$,
$VR_1 = VR_2 = 0.1R_F$

FLJ-HR2BA1/2 **(Fig.3-4)**

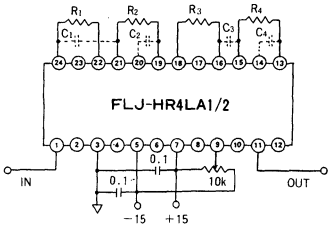


Rf1 = 1.0355 x Rf Rf2 = 0.95 x Rf1
Rf3 = 0.9657 x Rf Rf4 = 0.95 x Rf3
Rv1 > 0.1Rf1 Rv2 > 0.1Rf3
See technical note 4. for the values of Rf.
Rq1 = Rq2 = 3.92kΩ

9

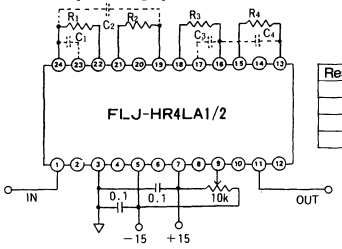
APPLICATIONS

1. A 4-pole lowpass Bessel or Chebyshev (0.5dB ripple) (Fig. 4-1)



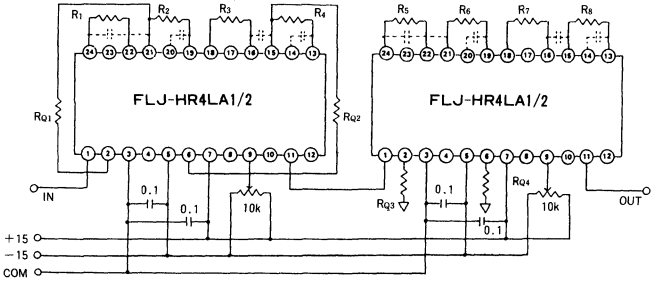
Resistor	Bessel	Chebyshev
R_1	$0.673R_F$	$2.182R_F$
R_2	$0.712R_F$	$1.286R_F$
R_3	$0.384R_F$	$2.178R_F$
R_4	$1.014R_F$	$0.432R_F$

2. A 4-pole highpass Chebyshev (0.5dB ripple) (Fig. 4-2)



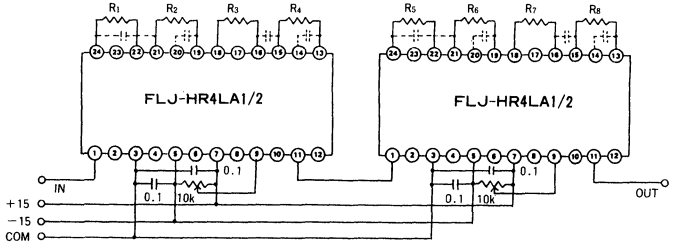
Resistor	Chebyshev
R_1	$0.726R_F$
R_2	$0.491R_F$
R_3	$0.386R_F$
R_4	$2.757R_F$

3. An 8-pole lowpass Butterworth (Fig. 4-3)



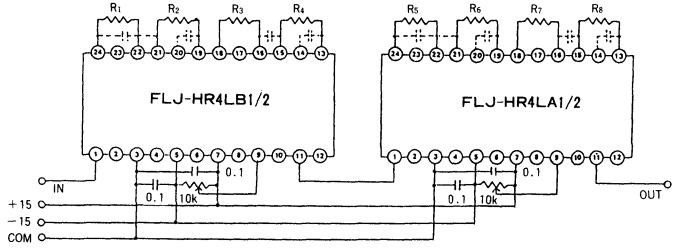
$R_{Q1} = 316k\Omega$, $R_{Q2} = 21.5k\Omega$
$R_{Q3} = 52.3k\Omega$, $R_{Q4} = 15.0k\Omega$
$R_F = R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R_7 = R_8$

4. An 8-pole lowpass Butterworth, Bessel or Chebyshev (0.05dB ripple) (Fig. 4-4)



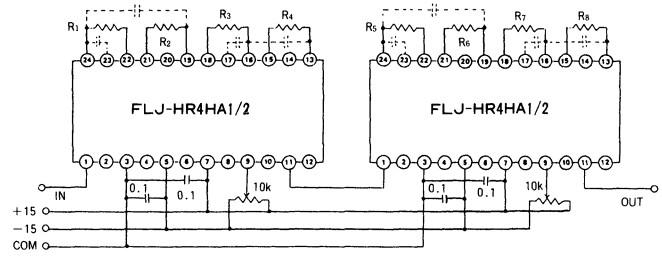
Resistor	Butterworth	Bessel	Chebyshev
R_1	$1.416R_F$	$0.526R_F$	$2.519R_F$
R_2	$0.706R_F$	$0.601R_F$	$2.232R_F$
R_3	$0.915R_F$	$0.233R_F$	$1.839R_F$
R_4	$1.093R_F$	$1.277R_F$	$0.6543R_F$
R_5	$1.111R_F$	$0.673R_F$	$2.972R_F$
R_6	$0.900R_F$	$0.390R_F$	$0.7504R_F$
R_7	$0.391R_F$	$0.428R_F$	$5.237R_F$
R_8	$2.561R_F$	$0.488R_F$	$0.1733R_F$

5. An 8-pole lowpass Cauer (0.53dB ripple) (Fig. 4-5)



$R_1 = R_2 = R_3 = R_4 = R_F$
$R_5 = 1.801R_F$ $R_6 = 1.221R_F$
$R_7 = 1.797R_F$ $R_8 = 0.4788R_F$

6. An 8-pole highpass Butterworth, Chebyshev (0.05dB ripple) (Fig. 4-6)



Resistor	Butterworth	Chebyshev
R_1	$0.942R_F$	$0.5619R_F$
R_2	$1.062R_F$	$0.3165R_F$
R_3	$0.689R_F$	$0.3762R_F$
R_4	$1.452R_F$	$2.209R_F$
R_5	$1.111R_F$	$0.7039R_F$
R_6	$0.900R_F$	$0.6371R_F$
R_7	$1.962R_F$	$0.3287R_F$
R_8	$0.510R_F$	$3.352R_F$

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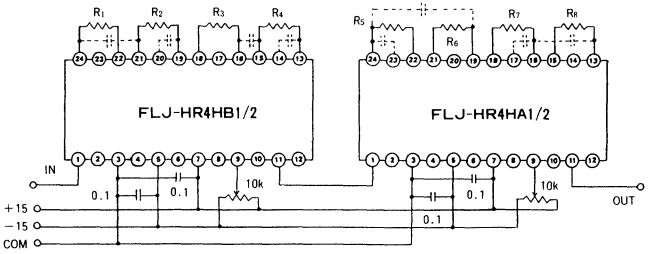
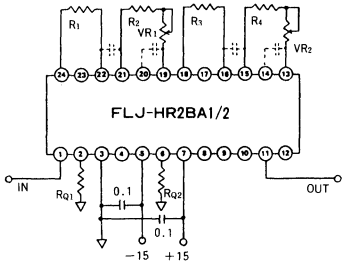
7. An 8-pole highpass Cauer (0.53dB ripple) (Fig. 4-7)



$R_1 = R_2 = R_3 = R_4 = R_F$
$R_5 = 0.845R_F$ $R_6 = 0.538R_F$
$R_7 = 0.422R_F$ $R_8 = 2.751R_F$

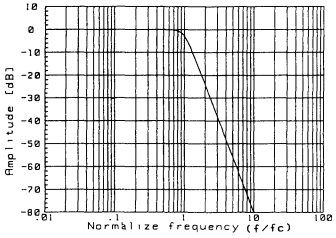
8. A 2-pole pair bandpass Butterworth (Fig. 4-8.)



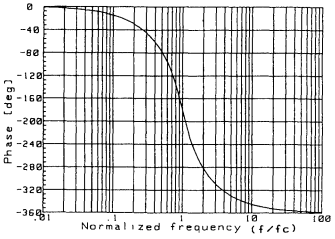
$R_1 = 1.0355R_F$ $R_2 = 0.95R_1$ $R_3 = 0.9657R_F$ $R_4 = 0.95R_3$
$VR_1 \geq 0.1R_1$ $VR_2 \geq 0.1R_3$ $R_{Q1} = R_{Q2} = 3.92k\Omega$

PERFORMANCE CURVES

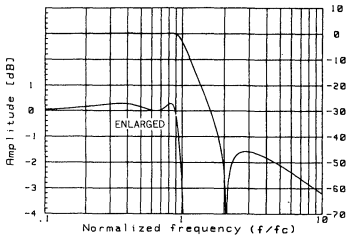
FLJ-HR4LA1/2 Frequency Response (Fig. 5-1)



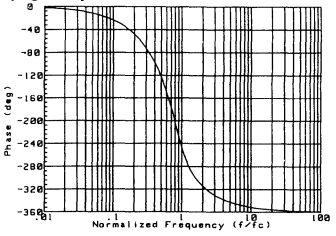
FLJ-HR4LA1/2 Phase Response (Fig. 5-2)



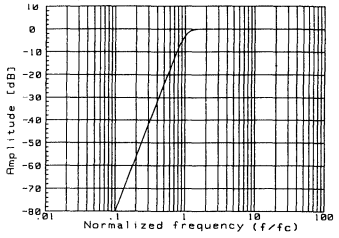
FLJ-HR4LB1/2 Frequency Response (Fig. 5-3)



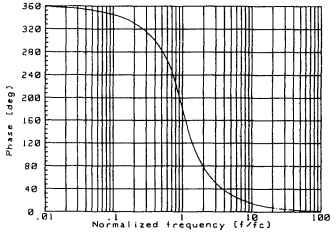
FLJ-HR4LB1/2 Phase Response (Fig. 5-4)



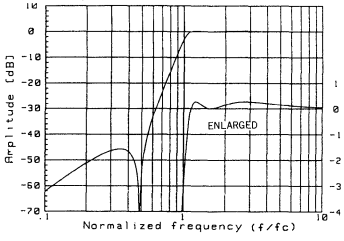
FLJ-HR4HA1/2 Frequency Response (Fig. 5-5)



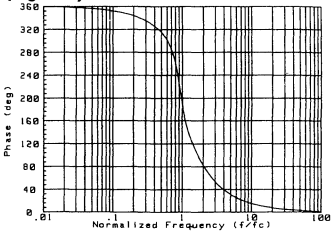
FLJ-HR4HA1/2 Phase Response (Fig. 5-6)



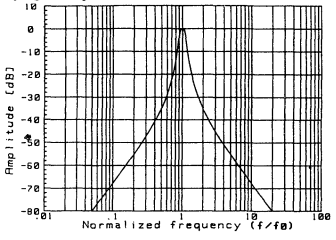
FLJ-HR4HB1/2 Frequency Response (Fig. 5-7)



FLJ-HR4HB1/2 Phase Response (Fig. 5-8)



FLJ-HR2BA1/2 Frequency Response (Fig. 5-9)



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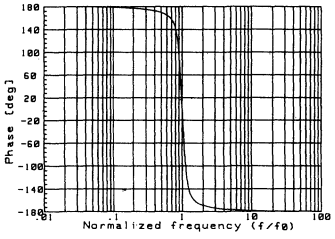
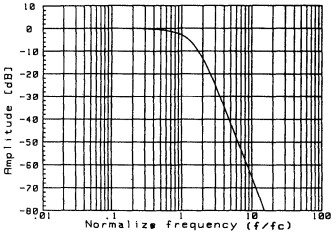
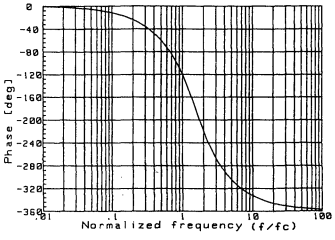
FLJ-HR2BA1/2 Phase Response (Fig. 5-10)



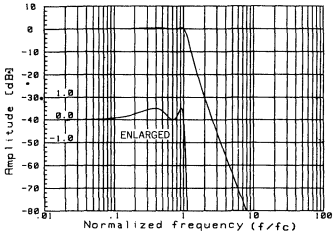
4-pole lowpass Bessel Frequency Response (Fig. 5-11)



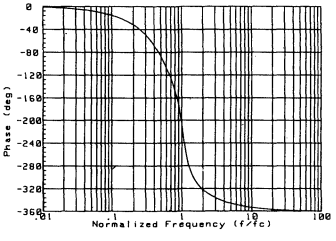
4-pole lowpass Bessel Phase Response (Fig. 5-12)



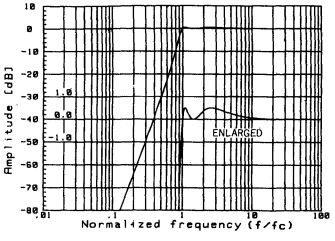
4-pole lowpass Chebyshev (0.5dB ripple) Frequency Response (Fig. 5-13)



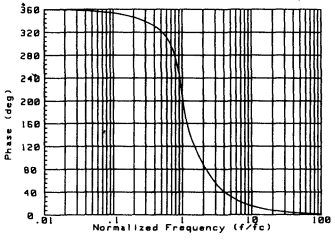
4-pole lowpass Chebyshev (0.5dB ripple) Phase Response (Fig. 5-14)



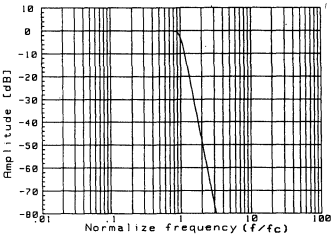
4-pole highpass Chebyshev (0.5dB ripple) Frequency Response (Fig. 5-15)



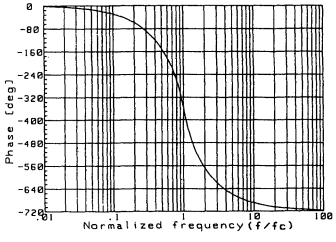
4-pole highpass Chebyshev (0. 5dB ripple) Phase Response (Fig. 5-16)



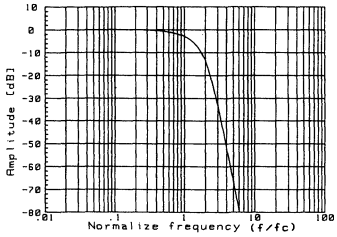
8-pole lowpass Butterworth Frequency Response (Fig. 5-17)



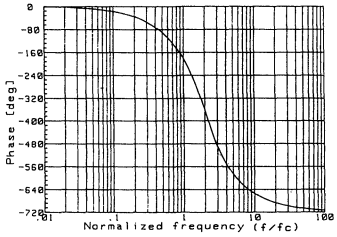
8-pole lowpass Butterworth Phase Response (Fig. 5-18)



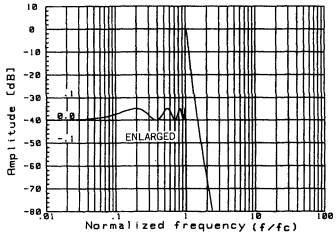
8-pole lowpass Bessel Frequency Response (Fig. 5-19)



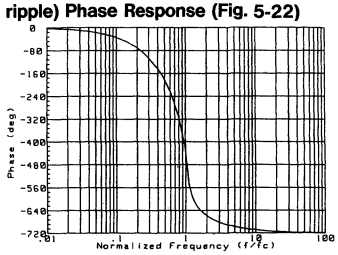
8-pole lowpass Bessel Phase Response (Fig. 5-20)



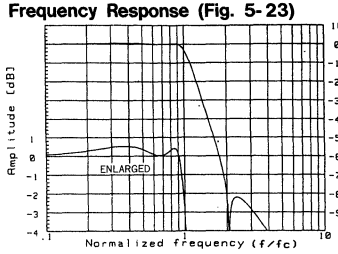
8-pole lowpass Chebyshev (0. 05dB ripple) Frequency Response (Fig. 5-21)



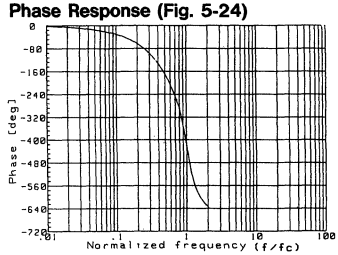
8-pole lowpass Chebyshev (0. 05dB ripple) Phase Response (Fig. 5-22)



8-pole lowpass Cauer (0.53dB ripple) Frequency Response (Fig. 5- 23)



8-pole lowpass Cauer (0.53dB ripple) Phase Response (Fig. 5-24)



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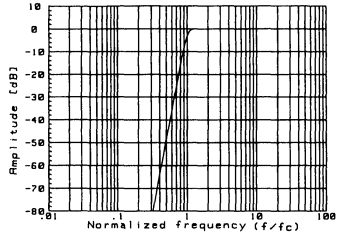
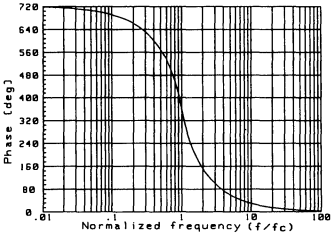
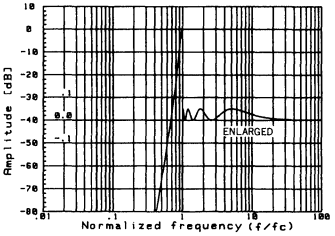
8-pole highpass Butterworth Frequency Response (Fig. 5-25)



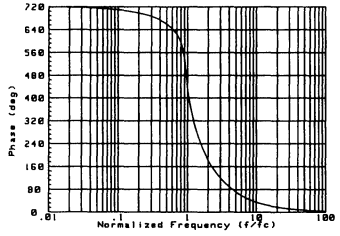
8-pole highpass Butterworth Phase Response (Fig. 5-26)



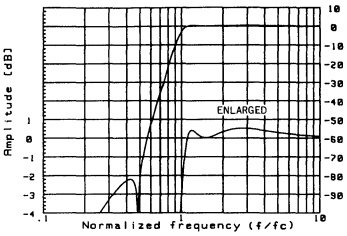
8-pole highpass Chebyshev (0.05dB ripple) Frequency Response (Fig. 5-27)



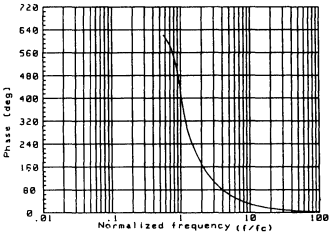
8-pole highpass Chebyshev (0.05dB ripple) Phase Response (Fig. 5-28)



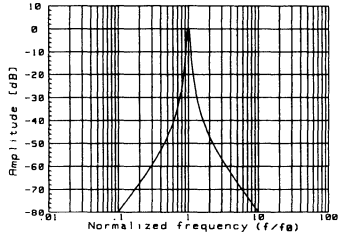
8-pole highpass Cauer (0.53dB ripple) Frequency Response (Fig. 5-29)



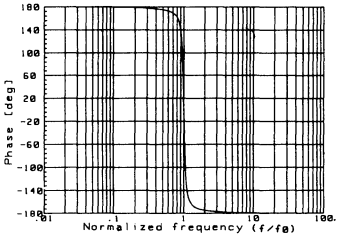
8-pole highpass Cauer (0.53dB ripple) Phase response (Fig. 5-30)



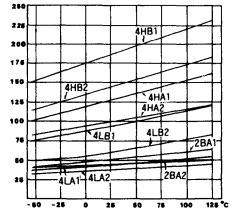
2-pole pair bandpass (Q = 10) Butterworth Frequency Response (Fig. 5-31)



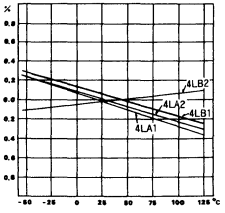
2-pole pair bandpass (Q = 10) Butterworth Phase Response (Fig. 5-32)



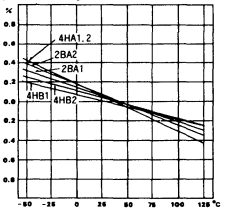
Noise vs Temperature (Fig. 5-33)



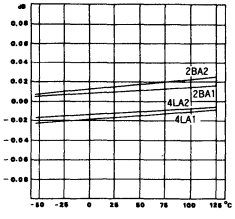
fc drift vs Temperature 1 (Fig. 5-34)



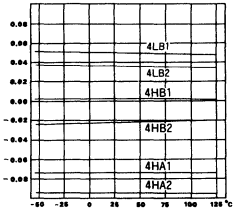
fo drift vs Temperature 2 (Fig.5-35)



Passband gain drift vs Temperature 1 (Fig. 5-36)



Passband gain drift vs Temperature 2 (Fig. 5-37)



9

RELIABILITY TESTS AND SCREENING

RELIABILITY TESTS

Reliability tests in compliance with MIL-STD-883 test methods are conducted on all products before they are released. The accompanying tables illustrate these qualification tests.

Group	Sub G.	Test	Method	Condition	Sample*	Notes
A.	1.	Mechanical dimensions	2016		2 (0)	
		Anti solvents	2015		4 (0)	
		Internal visual	2014		2 (0)	
		Bond strength	2011	C or D	2 (0)	
		Die shear strength	2019		2 (0)	
		Solderability	2003		2 (0)	Solder temp. 240 °C + 5°C
	2.	Static discharge	3015		3	Category A.
		Final electrical	-			
B.	1.	External visual	2009		5 (0)	
		Temperature cycle	1010	C	5 (0)	-65 to +150°C, 10 cycles
		Constant acceleration	2001	A	5 (0)	5000g Y1, 1 min.
		Fine leak	1014	A	5 (0)	
		Gross leak	1014	C	5 (0)	
		Final electrical	-		5 (0)	
	2.	Normal life	1005	B	5 (0)	+125°C 1000 hrs.
		Final electrical	-		5 (0)	
C.	1.	Heat shock	1011	C	3 (0)	-65 to +150°C, 15 cycles
		Stabilization bake	1008	C	3 (0)	+150°C 1 hrs.
		Lead	2004	B2	3 (0)	
		Fine leak	1014	A	3 (0)	
		Gross leak	1014	C	3 (0)	
	2.	Package insulation	-		3 (0)	600Vdc, 100nA
	3.	Salt spray	1009		5 (0)	24 hrs.
D.	1.	Vibration	2007	B	5 (0)	20 to 200Hz, 50g
		Shock	2002	B	5 (0)	1500g, 0.5mSec.
		Final electrical	-		5 (0)	
		External visual	2009		5 (0)	
		Fine leak	1014	A	5 (0)	
		Gross leak	1014	C	5 (0)	
E.	1.	Temperature cycle	1010	C	5 (0)	-65 to +150°C, 500cycles
		Final electrical	-		5 (0)	
		External visual	2009		5 (0)	
		Fine leak	1014	A	5 (0)	
		Gross leak	1014	C	5 (0)	

*Number of samples (defects allowed).

SCREENING

Wide operating temperature range versions of FLJ-HR Series are suffixed with MM and can operate from -55°C to +125°C. These versions are also screened in compliance with MIL-STD-883 test methods and can be ordered with a -QL suffix. Example: FLJ-HR4LA1MM-QL.

Test	Process	Method
1. Internal visual	Precap visual check with x10 to x80 microscope.	2017
2. Stabilization bake	+150 °C, 24 hrs.	1008
3. Temperature cycle	Low temp.: -65 °C +0/-10 °C High temp.:+150°C -0/+15°C >10 minutes, 10cycles	1010
4. Constant acceleration	5000g, Y1, 1 minute	2001
5. Pre burn-in test	Electrical performance	-
6. Burn-in	+85°C, 48 hrs.	1015
7. Final electrical	Per specifications	-
8. Leak, fine	Helium gas	1014
gross	FC-43, +125°C	
9. External visual		2009

ORDERING GUIDE

1. MC version: -40°C to+85°C operating temperature range

Filter type	Low fc type 10Hz to 1.6kHz	High fc type 100Hz to 50kHz/100kHz
4-pole lowpass Butterworth	FLJ-HR4LA1MC	FLJ-HR4LA2MC
4-pole lowpass Cauer	FLJ-HR4LB1MC	FLJ-HR4LB2MC
4-pole highpass Butterworth	FLJ-HR4HA1MC	FLJ-HR4HA2MC
4-pole highpass Cauer	FLJ-HR4HB1MC	FLJ-HR4HB2MC
2-pole pair bandpass Butterworth	FLJ-HR2BA1MC	FLJ-HR2BA2MC

2. MM version: -55°C to+125°C operating temperature range
Example: FLJ-HR4LA1MM

3. QL screening version
Example: FLJ-HR4LA1MM-QL

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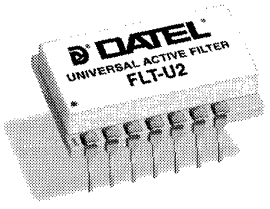
DATEL®
INNOVATION and EXCELLENCE

FLT-U2
Universal Active Filter

FEATURES

- **State variable filter**
- **Output to 200kHz**
- **2-Pole response**
- **LP, BP or HP functions**
- **Q range from 0.1 to 1,000**
- **Resonant frequency accuracy ±5%**
- **Frequency stability ±0.01%/°C**
- **Low-noise operational amplifiers**
- **–55 to +125°C operation**
- **Low cost**



GENERAL DESCRIPTION

The FLT-U2 is a universal active filter that uses the state-variable active-filter principle to implement a second order transfer function. Three committed operational amplifiers are used for the second-order function, while a fourth uncommitted operational amplifier can be used as a gain stage, summing amplifier, buffer amplifier, or to add another independent real pole.

Two-pole lowpass, bandpass and highpass transfer functions are available simultaneously from three different outputs, and notch and allpass functions are available by combining these outputs in the uncommitted operational amplifier. To realize higher order filters, several FLT-U2s can be cascaded. Frequency tuning is done by two external resistors and Q tuning by a third external resistor. For resonant frequencies below 50Hz, two external tuning capacitors must be added. Precise tuning of the resonant frequency is done by varying one of the resistors around its calculated value.

The internal operational amplifiers in the FLT-U2 have 3MHz gain-bandwidth products and a wideband input noise specification of only 10nV/$\sqrt{Hz}$. This results in considerably improved operation over most other competitive active filters which employ lower-performance amplifiers. By proper selection of external components, any of the popular filter types such as Butterworth, Bessel, Chebyshev or Elliptic may be designed.

Two models are available for operation over the commercial, 0 to +70°C, and military, –55 to 125°C, temperature ranges.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	R_Q	16	NO PIN
2	R_{IN}	15	NO PIN
3	HIGHPASS OUTPUT	14	STAGE 2 INPUT
4	+15V SUPPLY	13	BANDPASS OUTPUT
5	LOWPASS OUTPUT	12	–15V SUPPLY
6	+IN BUFFER	11	BUFFERED OUTPUT
7	STAGE 3 INPUT	10	–IN BUFFER
8	NO PIN	9	GROUND

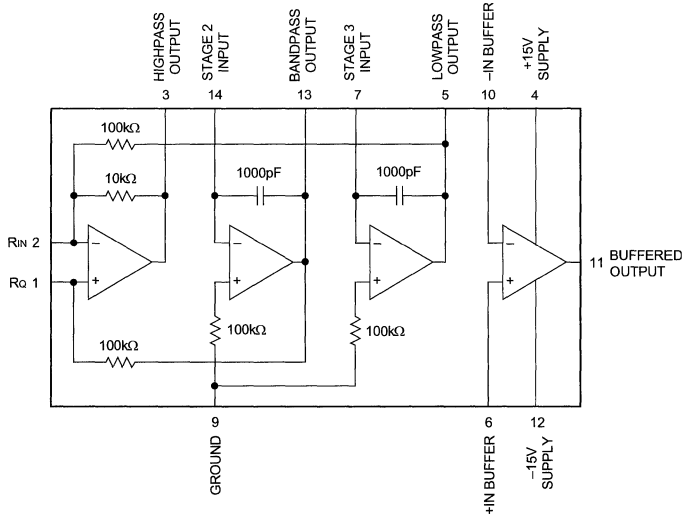


Figure 1. Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V supplies unless otherwise noted.)

FILTER CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Frequency Range ①		10-6 to 200		kHz
Q Range ①		0.1 to 1,000		
f_0 Accuracy		±5		%
f_0 Temperature Coefficient		±0.01		%/°C
Voltage Gain ①		0.1 to 1.0		V/V
AMPLIFIER CHARACTERISTICS				
Input Offset Voltage	—	±0.5	±6	mV
Input Bias Current	—	±40	±500	nA
Input Offset Current	—	±5	±200	nA
Input Impedance	—	5	—	MΩ
Input Com. Mode Voltage Range	±12	—	—	Volts
Input Voltage Noise, wideband	—	10		nV/√Hz
Output Voltage Range	±10	—	—	Volts
Output Current	±5	—	—	mA
Open Loop Voltage Gain	—	300,000	—	
Common Mode Rejection Ratio	—	100	—	dB
Power Supply Rejection	—	10	—	µV/V
Unity Gain Bandwidth	—	3	—	MHz
Slew Rate	—	±1	—	V/µs
POWER SUPPLY REQUIREMENTS				
Voltage, rated performance	—	±15	—	Volts
Voltage Range, operating	±5	—	±18	Volts
Quiescent Current	—	—	±11.5	mA
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range				
FLT-U2		0 to +70°C		
FLT-U2-M		–55 to +125°C		
Storage Temperature Range		–55 to +125°C		
Package		Ceramic 16-pin DIP (double spaced)		

Footnote:

① $f_0Q = 5 \times 10^5$ optimally.

TECHNICAL NOTES

1. The FLT-U2 has simultaneous lowpass, bandpass and highpass transfer functions. The chosen output for a particular function will be at unity gain based on Tables II and III. This means that the other two unused outputs will be at other gain levels. The gain of the lowpass output is always 10dB higher than the gain of the bandpass output and 20dB higher than the gain of the highpass output.
2. When tuning the filter and checking it over its frequency range, the outputs should be checked with a scope to make sure there is no waveform clipping present, as this will affect the operation of the filter. In particular, the lowpass output should be checked since its gain is the highest.
3. Check f_1, the center frequency for bandpass and the cutoff frequency for lowpass or highpass, at the bandpass output (pin 13). Here the peaking frequency can easily be determined for high-Q filters and the 0° or 180° phase frequency can easily be determined for low-Q filters (depending on whether inverting or noninverting).
4. Tuning resistors should be 1% metal-film types with 100ppm/°C temperature stability or better for best performance. Likewise, external tuning capacitors should be NPO ceramic or other stable capacitor types.

THEORY OF OPERATION

The FLT-U2 block diagram is shown in Figure 2. This is a second-order state-variable filter using three operational amplifiers. Lowpass, bandpass and highpass transfer functions are simultaneously produced at its three output terminals. These three transfer functions are characterized by the following second order equations:

$$H(S) = \frac{K_1}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \quad \text{LOWPASS} \qquad \frac{\omega_0}{Q}$$

$$H(S) = \frac{K_2 S}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \quad \text{BANDPASS}$$

$$H(S) = \frac{K_3 S^2}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \quad \text{HIGHPASS}$$

where K_1, K_2 and K_3 are arbitrary gain constants.

A second-order system is characterized by the location of its poles in the s-plane as shown in Figure 3. The natural radian frequency of this system is ω_0. In Hertz this is $f_0 = \frac{\omega_0}{2\pi}$.

The resonant radian frequency of the circuit is different from the natural radian frequency and is:

$$\omega_1 = \omega_0 \sin\theta = \sqrt{\omega_0^2 - \sigma_1^2}$$

The damping factor d determines the amount of peaking in the filter frequency response and is defined as:

$$d = \cos\theta$$

The point at which the peaking becomes zero is called critical damping and is $d = \sqrt{2}/2$.

Q is found from d and is a measure of the sharpness of the resonance of the peaking:

$$Q = \frac{1}{2d}$$

$$\text{Also, } Q = \frac{f_0}{-3\text{dB Bandwidth}} = \frac{\omega_0}{2\sigma_1}$$

For high-Q filters, the natural frequency and resonant frequency are approximately equal.

$$\omega_1 \approx \omega_0 \quad \text{or} \quad f_1 \approx f_0$$

This is true since $\omega_1 = \omega_0 \sin\theta$ and $\sin\theta \approx 1$ as the poles move close to the $j\omega$ axis in the s-plane.

For high Q's (Q > 1), we therefore have for the second order filter:

$f_0 \approx$ Bandpass center frequency
$\approx$ Lowpass corner frequency
$\approx$ Highpass corner frequency

In the simplified tuning procedure which follows, the tuning is accomplished by independently setting the natural frequency and Q of the filter. This is done most simply by assuming unity gain for the output of the desired filter function. Unity gain means a gain of one (±) at dc for lowpass, at center frequency for bandpass, and at high frequency ($f >> f_0$) for highpass. Unity gain does not apply to all outputs simultaneously but only to the chosen output based on the component values given in the tables. Figure 4 shows the relative gains of the three simultaneous outputs assuming the bandpass gain is set to unity. Note that lowpass gain is always 10dB higher than bandpass gain, and highpass gain is always 10dB lower than bandpass gain.

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SIMPLIFIED TUNING PROCEDURE

1. Select the desired transfer function (lowpass, bandpass or highpass) and inverted or noninverted output. From this determine the filter configuration (inverting or noninverting) using Table 1.
2. Starting with the desired natural frequency and Q (determined from the filter transfer function or s-plane diagram), compute f_0Q. For $f_0Q > 10^4$, the actual realized Q will exceed the calculated value. At $f_0Q = 10^4$, the increase is about 1%, and at $f_0Q = 10^5$ it is about 20%.
3. **Inverting Configuration.** Using the value of Q from Step 2, find R_1 and R_3 from Table II. R_2 is open, or infinite.
4. **Noninverting Configuration.** Using the value of Q from Step 2, find R_2 and R_3 from Table III. R_1 is open, or infinite.
5. Using the value of f_0 from Step 2, set the natural frequency of the filter by finding R_4 and R_5 from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{f_0}$$

where R_4 and R_5 are in Ohms and f_0 is in Hertz. The natural frequency varies as $\sqrt{R_4R_5}$ and therefore one value may be increased and the other decreased and the natural frequency will be constant if the geometric mean is constant. To maintain constant bandwidth at the bandpass output while varying center frequency, fix R_4 and vary R_5.

6. For $f_0 < 50$Hz, the internal 1000pF capacitors should be shunted with external capacitors across pins 5 & 7 and 13 & 14. If equal value capacitors are used, R_4 and R_5 are then computed from:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0C} \quad (C \text{ in pF})$$

For unequal value capacitors this becomes:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0\sqrt{C_1C_2}} \quad (C_1 \text{ and } C_2 \text{ in pF})$$

In both cases, the capacitance is the sum of the external values and the internal 1000pF values.

Table I. Filter Configuration

	LP	BP	HP
Inverting Input	Inverting	Non-Inv.	Inverting
Noninverting Input	Non-Inv.	Inverting	Non-Inv.

Table II. Inverting Configuration

	R_1	R_2	R_3
Lowpass	100k	Open	$\frac{100k}{3.8Q-1}$
Bandpass	Q x 31.6k	Open	$\frac{100k}{3.48Q}$
Highpass	10k	Open	$\frac{100k}{6.64Q-1}$

Table III. Noninverting Configuration

	R_1	R_2	R_3
Lowpass	Open	$\frac{316k}{Q}$	$\frac{100k}{3.16Q-1}$
Bandpass	Open	100k	$\frac{100k}{3.48Q-1}$
Highpass	Open	$\frac{31.6k}{Q}$	$\frac{100k}{0.316Q-1}$

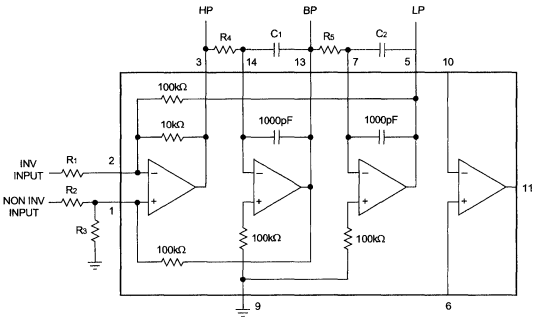

Figure 2. FLT-U2 Block Diagram

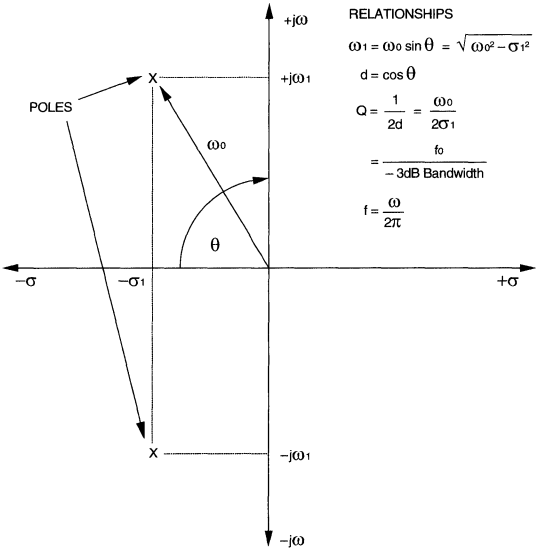

Figure 3. S-Plane Diagram

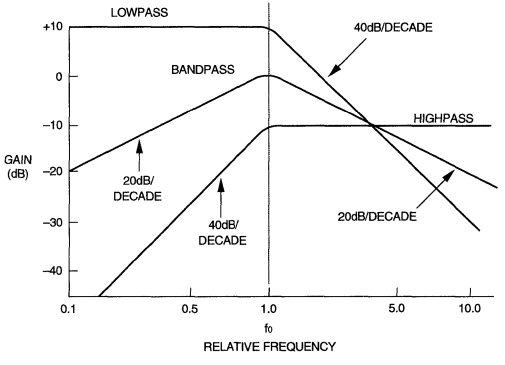

Figure 4. Relative Gains of Simultaneous Outputs, Q = 1

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SIMPLIFIED TUNING PROCEDURE (continued)

7. This procedure is based on unity gain output for the desired function. For additional gain, the fourth (uncommitted) operational amplifier should be used as an inverting or noninverting gain stage following the selected output. See Figure 5. A third pole on the real axis of the s-plane may also be added to the transfer function by adding a capacitor to the gain stage as shown in Figure 6.

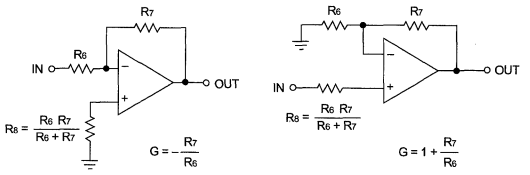

Figure 5. Uncommitted Op Amp Gain Configurations

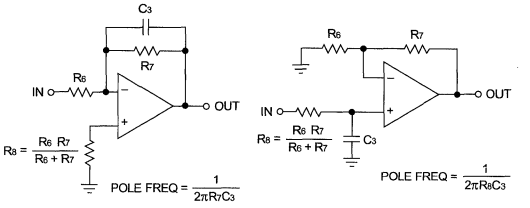

Figure 6. Using the Uncommitted Op Amp to Add a Real Axis Pole

FILTER DESIGN EXAMPLES

Bandpass Filter with 1kHz Center Frequency Q = 10 and Inverted Output

1. From Table I, the noninverting configuration is chosen to realize an inverted bandpass output $f_0Q = 10^4$ which means the realized Q will be about 1% higher than calculated.

2. From Table III, using Q = 10, we find:

$$R_1 = \text{open}$$

$$R_2 = 100k\Omega$$

$$R_3 = \frac{100k\Omega}{3.48Q - 1} = \frac{100k\Omega}{33.8} = 2.96k\Omega$$

3. Using f_0 of 1kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{1000} = 50.3k\Omega$$

4. This completes the filter design which is shown in Figure 7. To choose the nearest 1% standard value resistors either 49.9k or 51.1k Ohms could be used; likewise one value of 49.9k and one of 51.1k could be used giving the geometric mean of $\sqrt{R_4R_5} = \sqrt{49.9k \times 51.1k} = 50.5k$ which is even closer. But due to the filter ±5% frequency tolerance, it may be better to hold R_4 constant while varying R_5 to tune it exactly.

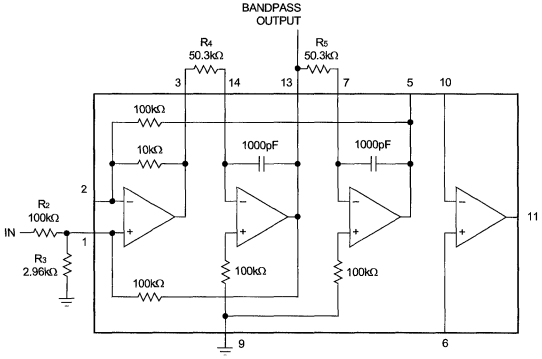

Figure 7. Bandpass Filter Example

Three-Pole Noninverting Butterworth Lowpass Filter with dc Gain of 10 and Cutoff Frequency of 5kHz

The s-plane diagram of the 3-pole Butterworth filter is shown in Figure 8. We will use a second-order filter to realize the two complex conjugate poles and the uncommitted operational amplifier to provide the third real axis pole and a dc gain of 10.

1. From Table I, the noninverting filter configuration would normally be used to give a noninverting lowpass output. In this case, however, we choose an inverting uncommitted op amp with a gain of 10 and therefore we use the inverting configuration for the filter. By comparing the second-order portion of the Butterworth function $S^2 + \omega_0 S = \omega_0^2$ to the standard second-order function $S^2 + \omega_0 S = \omega_0^2$ we find Q = 1. f_0Q is then 5×10^3 so that Q will not exceed its specified value.

2. From Table II, using Q = 1, we find:

$$R_1 = 100k\Omega$$

$$R_2 = \text{open}$$

$$R_3 = \frac{100k}{3.80Q - 1} = 35.7k\Omega$$

3. Using f_0 of 5kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{5000} = 10.1k\Omega$$

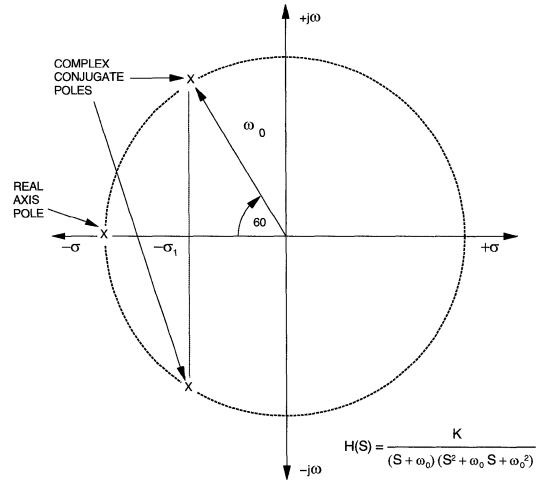

Figure 8. S-Plane diagram of 3-Pole Butterworth Lowpass Filter

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FILTER DESIGN EXAMPLES (continued)

4. For the uncommitted output amplifier, a gain of –10 is required. This defines $R_7/R_6 = 10$ and we arbitrarily choose $R_6 = 2k$, $R_7 = 20k\Omega$. R_8 becomes approximately $2k\Omega$.

5. The final step is to realize the real axis pole of the Butterworth filter. This pole is at 5kHz and is set by using capacitor C_3 across the feedback resistor R_7:

$$C_3 = \frac{1}{2\pi f R_7} = \frac{1}{6.28 \times 5 \times 10^3 \times 20 \times 10^3} = 1590pF$$

6. This completes the 3-pole Butterworth filter which is shown in Figure 9.

Highpass Filter with Gain of –1, 20kHz Cutoff Frequency, and Critical Damping

1. From Table I, the inverting configuration must be used to realize a highpass gain of –1. An s-plane diagram of this function is shown in Figure 10. Critical damping requires the pole positions to be on a line 45° with respect to the real axis and this results in no frequency peaking. The damping factor d is:

$$d = \cos\theta = \cos 45° = 0.707$$

and $$Q = \frac{1}{2d} = \frac{1}{2(0.707)} = 0.707$$

Because this is a low-Q system, the natural frequency will not be the same as the highpass cutoff frequency f_1. From Figure 10:

$$f_0 = \frac{f_1}{\cos\theta} = \frac{20kHz}{(0.707)} = 28.3kHz$$

Then $f_0Q = 0.707 \times 28.3 \times 10^3 = 2 \times 10^4$, and the Q will exceed its desired value by slightly more than 1%.

2. From Table II, using Q = 0.707 we find:

$$R_1 = 10k\Omega$$

$$R_2 = \text{open}$$

$$R_3 = \frac{100k\Omega}{6.64Q - 1} = \frac{100k\Omega}{3.69} = 27.1k\Omega$$

3. Using $f_0 = 28.3kHz$, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{28.3 \times 10^3} = 1.78k\Omega$$

4. This completes the highpass filter design which is shown in Figure 11. When using this filter, care should be exercised so that clipping does not occur due to excessive input levels. If clipping occurs, the filter will not operate properly. Clipping will first occur at the lowpass output around f_0 since its gain is 20dB higher than the highpass output. The signal level should be reduced so that clipping does not occur anywhere in the frequency range used. If a higher signal level is required, the highpass output should be amplified by a gain stage using the uncommitted operational amplifier.

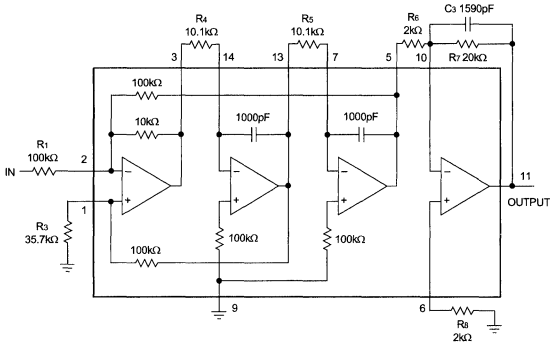


Figure 9. Three-Pole Butterworth Lowpass Filter Example

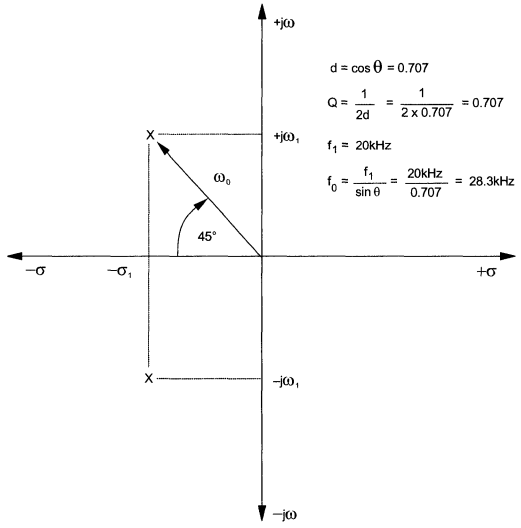


Figure 10. S-Plane Diagram of Highpass Filter with Critical Damping

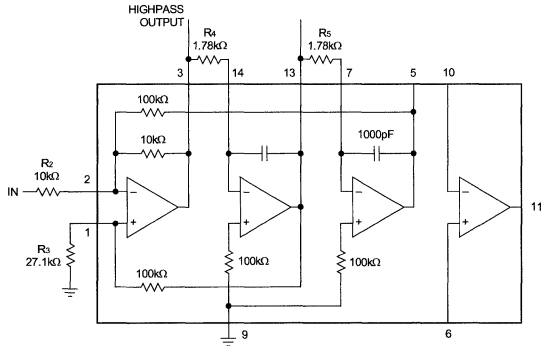


Figure 11. Highpass Filter Example

ADVANCED FILTERS

All of the common filter types can be realized using cascaded FLT-U2 stages. This includes multi-pole Butterworth, Bessel, Chebyshev and Elliptic types. The basic procedure is to implement each pole pair with a single FLT-U2 and cascade enough units to realize all poles. A real-axis pole is implemented by an uncommitted operational amplifier stage. Each stage should be separately tuned with an oscillator and scope and then the stages connected together and checked. See Figure 12.

A notch filter can be constructed in several ways. The first way is to use the FLT-U2 as an inverting bandpass filter and sum the output of the filter with the input signal by means of the uncommitted operational amplifier. This produces a net subtraction at the center frequency of the bandpass which produces a null at the output of the amplifier. See Figure 13. Likewise, lowpass and highpass outputs (which are always in phase) can be combined with each other through an external operational amplifier. The highpass output must have some gain added to it, however, so that its gain is equal to that of the lowpass output. A third method is to use two separate FLT-U2s, one as a two-pole lowpass filter and the other as a two-pole highpass filter. Again, the outputs are combined through an operational amplifier. This method permits independent tuning of the two sections to get the best null response.

Further discussion of filter designs is beyond the scope of this data sheet and the user is referred to the various texts on filter design, some of which are listed below.

Estep, G.J., *The State Variable Active Filter Configuration Handbook,* 2nd Edition, Agoura, CA., 1974.

Reference Data for Radio Engineers, Howard W. Sams & Co., Inc., 5th Edition.

Christian, E. and Eisenmann, E., *Filter Design Tables and Graphs,* McGraw-Hill Book Co., 1974.

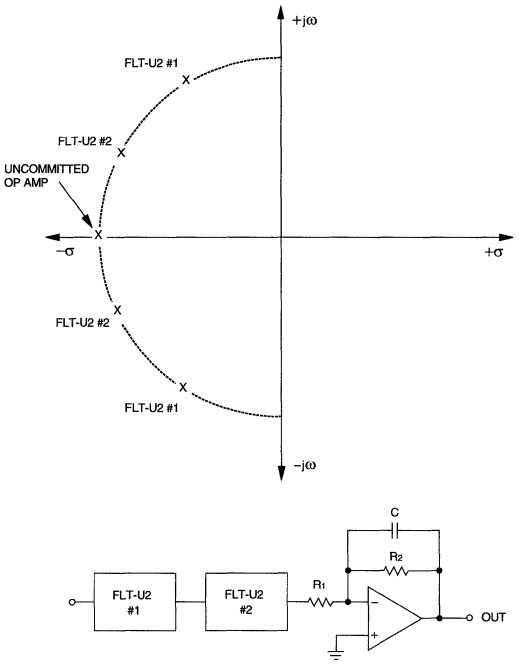


Figure 12. Realization of a Complex Multi-Pole Filter

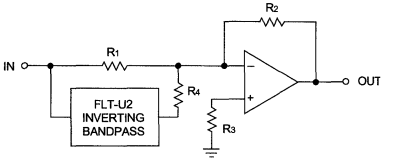
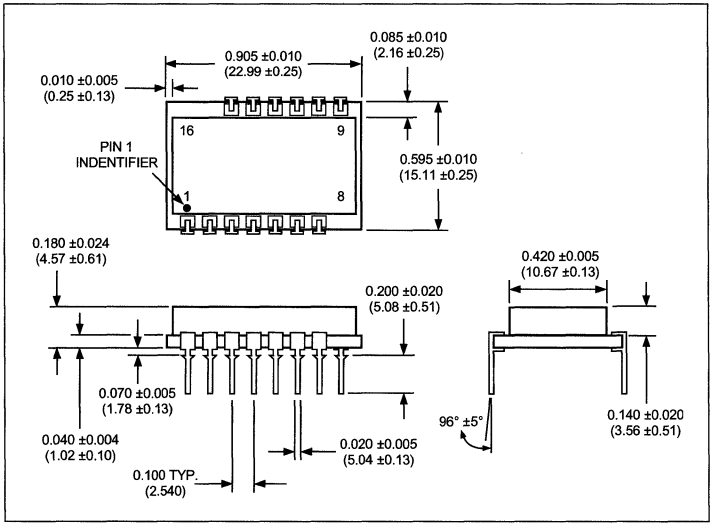


Figure 13. Realization of a Notch Filter

MECHANICAL DIMENSIONS INCHES (mm)



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MODEL	OPERATING TEMP. RANGE
FLT-U2	0 to +70°C
FLT-U2-M	−55 to +125°C

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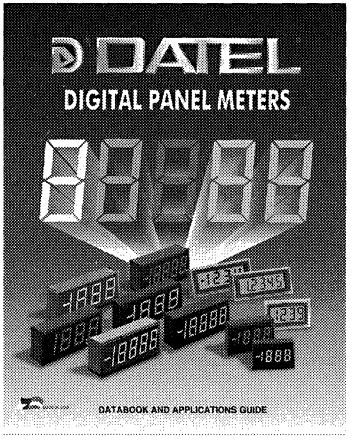

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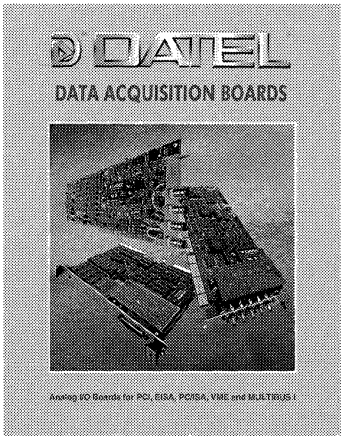

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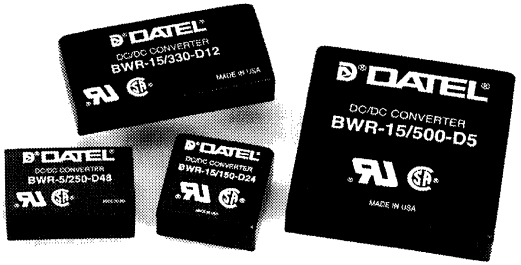

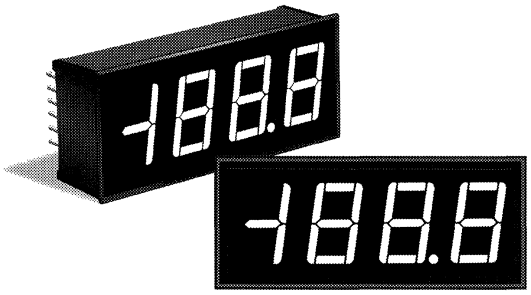

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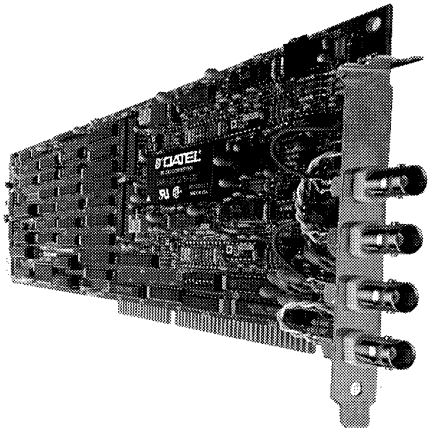

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Meiji Seimei Gotanda Building, 3F
2-27-4 Nishigotanda
Shinagawa-Ku, Tokyo 141, Japan
Tel: 3-3779-1031
Fax: 3-3779-1030

Yachiyo Building, Higashikan
2-Kita 1-21, Tenjinbashi
Kita-Ku, Osaka 530, Japan
Tel: 6-354-2025
Fax: 6-354-2064

INNOVATION and EXCELLENCE

Corporate Office

DATEL, Inc.
11 Cabot Boulevard
Mansfield, MA 02048-1194
Tel: 508-339-3000
Fax: 508-339-6356

International Sales Offices

DATEL GmbH
Postfach 150826
D-80045 Munchen
Germany
Tel: 89-544334-0
Fax: 89-536337

DATEL S.A.R.L.
Zone d'Activities du Pas du Lac Nord
9, Rue Michael Faraday
78180 Montigny Le Bretonneux, France
Tel: 1-34-60-01-01
Fax: 1-30-58-21-30

DATEL (UK) LTD.
Unit 15, Campbell Court Business Park
Campbell Road, Bramley, Tadley
Hampshire, RG26 5EG, England
Tel: (01256) 880444
Fax: (01256) 880706

DATEL KK
Meiji Seimei Gotanda Building, 3F
2-27-4 Nishigotanda
Shinagawa-Ku, Tokyo 141, Japan
Tel: 3-3779-1031
Fax: 3-3779-1030

Yachiyo Building, Higashikan
2-Kita 1-21, Tenjinbashi
Kita-Ku, Osaka 530, Japan
Tel: 6-354-2025
Fax: 6-354-2064

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