DALLAS SEMICONDUCTOR 1989

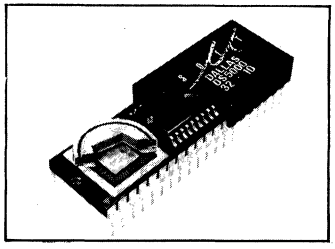
DALLAS

SEMICONDUCTOR

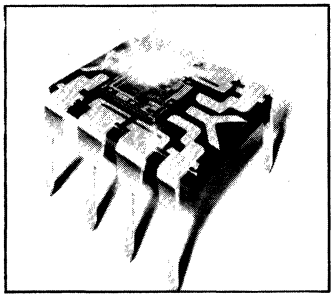
Dallas Semiconductor

Late definition Technologies

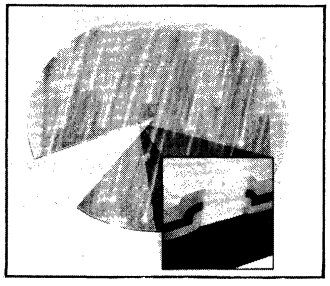
Through the use of special late definition technologies, products can be tailored to meet an exact application after wafer fabrication is complete. Modifications may be made either by Dallas Semiconductor or in the field by the user. Certain products are also capable of self-modification based on feedback information.



Embedded Lithium Power Sources:
Dallas Semiconductor has the ability to integrate in a single package, its ultra low power CMOS circuits and a miniature lithium power source. Chips designed in this way can accept change and remember data throughout their operating life.



Direct Laser Writing:
Lasers provide a low cost means for Dallas Semiconductor to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication.Proprietary software controls the laser to make each chip unique.



High Energy Ion Implantation:
Circuits on nearly finished wafers are defined to exact customer specifications. Using a million-volt implanter, wafers are bombarded by a cloud of super charged ions. The ions penetrate specific layers of silicon to economically tailor chips to specific functions.

DALLAS
SEMICONDUCTOR

not the only name behind our products...

Quality Completes Our Promotion

Dallas Semiconductor
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General Information

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Corporate Fact Sheet

CORPORATE FACT SHEET
Dallas Semiconductor designs, manufactures and markets CMOS integrated circuits using special Late Definition technology. Late Definition permits the exact definition of a product to be postponed until end use, thereby increasing flexibility.

PRODUCTS
Founded Febuary 1, 1984, Dallas Semiconductor has a multiproduct strategy to serve the needs of the computer and communications industry. Our optimism stems from the ability to sell "Soft Silicon"™ which can be readily tailored to solve the specific problems of our customers. Soft Silicon results from the Late Definition technologies of lithium, laser , and implant. Lithium postpones definition until end use, thereby making the chip adaptive in the system. Laser postpones definition until just before the chip is placed in the package, and implant postpones definition until the last wafer process step.

LITHIUM
Advances in CMOS circuitry have reduced power requirements to the point that a chip,using appropriate circuitry, can be packaged with a miniature lithium energy source which will last the useful life of the equipment. This allows Dallas Semiconductor to make chips which don't forget. Our initial product offerings exploited this capability to make the much sought-after nonvolatile RAM. In November 1984 we began shipping 64K Nonvolatile SRAMs.

Keeping track of human time has not been an easy task for computers until our July 1985 announcement of the DS1216 SmartWatch. It precisely keeps calendar time down to the hundredth of a second,replacing what heretofore consumed a whole printed circuit board full of electronics. A lithium cell provides power for life.

The adaptive nature of CMOS/Lithium products is made evident by the April 1987 introduction of the DS5000 Soft Microcontroller. Designed with change in mind, it offers unprecedented software adaptability and crashproof operation. The capabilities of the Soft Microcontroller take it beyond mere update change and into the realm of learning. The DS5000 can capture a large amount of data in real time and remember it indefinitely. With the proper application software, the microcontroller can improve its performance based on that cumulative knowledge. July 1988 marked the shipment of the DS5000T Time Microcontroller, the first permanently powered microcontroller that logs events and schedules activities according to calendar time.

LASER
The laser creates uniqueness on a chip at low cost. A sub-micron positioning laser and formidable control software developed at Dallas can engrave individual chips with digital patterns making each one different. These after-the-fact changes to completed circuits give our laser-based products a competitive edge.

The first product that demonstrated our special laser technology was an extremely accurate time base, commonly referred to as a delay line. Before the August 1985 announcement date, it had only been possible to build such devices using a dozen components in a hybrid assembly.The DS1000 Silicon Delay Line series is a direct replacement tor hybrid delay lines which are widely used in conjunction with DRAMs and magnetic disks.

Other products use the laser to protect sensitive information and intellectual property by creating a powerful security mechanism in micro chips. The DS1204U Electronic Key is an example of a product which benefits from the laser in this regard. Exclusive blank Keys are defined by laser for each customer, adding to the overall security mechanism. Other products use the laser to tailor the option content of the chip for a particular customer. In short, the laser lets Dallas Semiconductor define each chip uniquely after it is already operational.

Difficult system problems have been solved by relying on these special technologies, experience, and creativity, to offer our customers a more complete solution than the chip alone can provide. Often this requires a greater emphasis on packaging than traditional semiconductor producers have been accustomed. Sixty-five base products were put into production prior to October 1988, unified by our own CMOS technology.

MANUFACTURING AND FACILITIES

Dallas Semiconductor manufactures products at a 114,000 square-foot facility located at the company's headquarters in north Dallas. This location includes an advanced Class One wafer fabrication facility completed in 1987. Six-inch wafers are processed with circuits utilizing submicron geometries. Automated modular process technology provides substantial flexibility in the manufacturing process and significantly reduces the number of people required for operation, thereby decreasing manufacturing costs. The company's wafer fabrication facility contains a 10,000-square-foot cleanroom. The sensitivity of the manufacturing process to particulates and other contaminants requires a highly controlled, clean environment. All products are shipped from Dallas after final quality assurance testing.

MARKETING AND SALES

Dallas Semiconductor sells its products to a large and diverse customer base of both mature and emerging OEMs in the computer, telecommunications, instrumentation, and factory automation markets. The company coordinates its selling activity from its Dallas, Texas headquarters. Six area sales offices are staffed in Cherry Hill, New Jersey; Boca Raton, Florida; Cupertino, California; Los Angeles, California; Carmel, Indiana; and Birmingham, England. The six area sales managers call on OEM accounts and coordinate the activities of 44 sales representative offices in North America and 23 in Europe and Asia. Dallas Semiconductor also markets its products in North America through a national stocking distributor and through twelve regional distributors.

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Alfatron GmbH
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Rancho Cordova, CA
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Houston, TX
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Utah
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Washington
Redmond, WA
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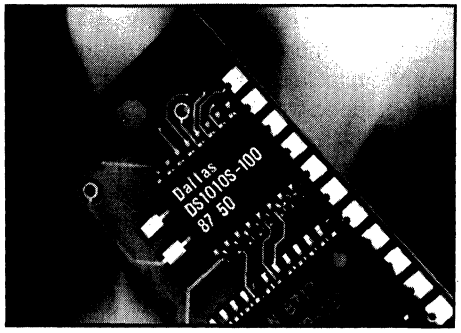
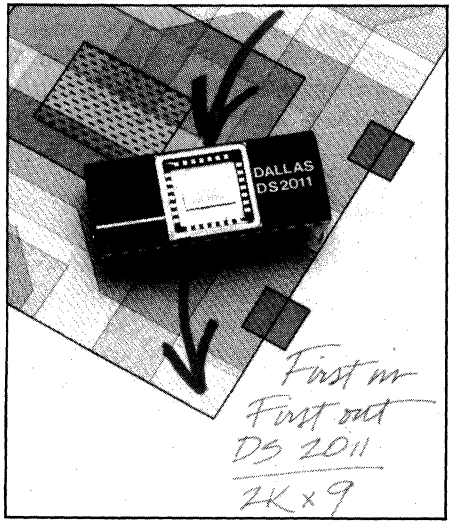
Product Overview



SILICON TIMED CIRCUITS

Electronic systems require exact timing to control the transmission of data between their component parts. Timing requirements vary across systems. Historically, systems designers have not been able to use semiconductors as timing references because of their lack of precision; they consequently achieved the required accuracy by using, in combination, quartz crystals and hybrid passive components, known as delay lines. All silicon delay lines offer single chip reliability, economy and significantly greater precision due to their laser-defined specifications. Direct laser writing provides precise accuracy and, because the products are defined in the final stage of manufacturing, a broad product mix is available without losing the economic benefits of standard intergrated circuit production. Customers are provided maximum flexibility, as well as the option of purchasing tailor-made products at the approximate cost of standard, off-the-shelf solutions. These all silicon products can be retrofitted into existing systems which otherwise utilize hybrid approaches as well as designed into new systems.

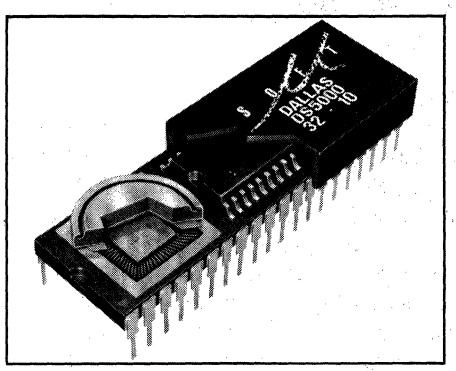
DS1000 5 TAP Delay Line
DS1010 10 TAP Delay Line
DS1013 3 in 1 Delay Line
DS1007 7 in 1 Delay Line



MULTIPORT MEMORY

The existence of many different data transmission rates and standards has created a problem in transporting data among different systems. A receiving system may be too slow to keep up with data sent from another system. First In, First Out (FIFO) memories are capable of providing the necessary elasticity between different data rates.

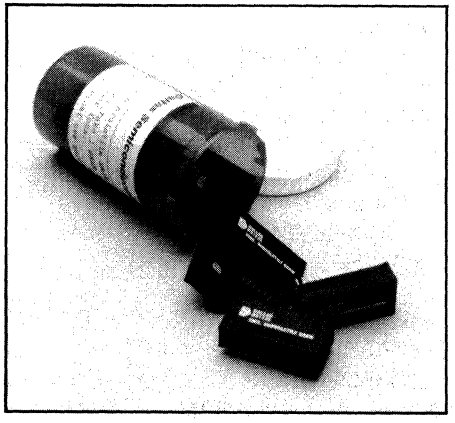
DS2009 512 x 9 FIFO
DS2010 1K x 9 FIFO
DS2011 2K x 9 FIFO
DS2012 4K x 9 FIFO
DS2013 8K x 9 FIFO
DS2015 4X64 Quadport Serial RAM
DS9050 PC InterLink



MICROCONTROLLER

The DS5000 Soft Microcontroller stays up-to-date because it was designed for change. Unlike rigid ROM or EPROM based microcontrollers, all of the Soft Microcontroller memory is high performance, read/write, and nonvolatile for more than ten years. The DS5000 is equipped with up to 64K bytes of nonvolatile SRAM which can be dynamically partitioned to fit program and data storage requirements of a particular task. As a result of sophisticated crashproofing circuitry, processing of a task can resume after a power outage. A built-in encrypter prevents unauthorized access to resident application software. The pinout and instruction set match the industry standard 8051 microcontroller. The DS5000T Time Microcontroller can log events and schedule activities according to calendar time. Additional information is available in a special publication called the Soft Microcontroller User Guide. The DS5000TK evaluation kit includes a sample DS5000T, documentation, in-system loader hardware and DOS compatible software for use with a personal computer. For extensive development work the DS5000DK in circuit emulator is recommended.

DS5000 Soft Microcontroller
DS5000T Time Microcontroller
DS5000K Evaluation Kit
DS5000DK Development Kit

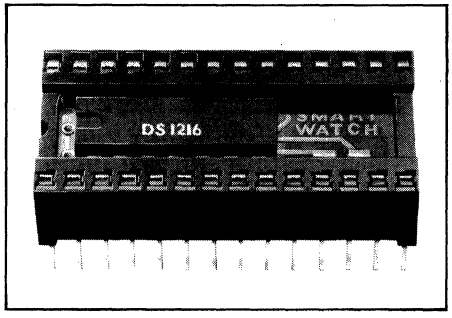


NONVOLATILE SRAM

SRAMs have always had the undesirable characteristics of data loss when power is disrupted . Dallas Semiconductor has combined its knowledge of ultra low power CMOS SRAMs with improvements in long life embedded lithium power sources to develop a family of Nonvolatile SRAMs. Nonvolatile SRAMs integrate a lithium power source and intelligent control circuitry to retain data even in the absence of system power. The control circuit, by monitoring the level of system voltage available to the memory at all times, switches to the lithium power source when necessary, and also protects the memory contents against inadvertent change during system power fluctuations. A lithium power source provides backup power for more than 10 years in the absence of system power. Nonvolatile SRAMs are packaged to fit into existing sockets and can replace other widely used memory devices. These products perform

EPROMs, or shadow RAMs because they provide unlimited data write cycles, safeguard against corrupted data and write data in as fast as 70ns.

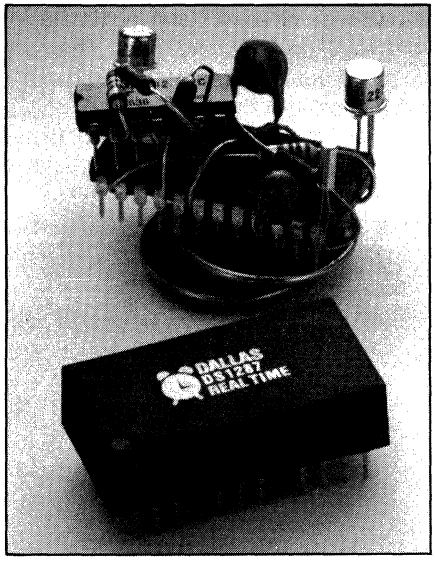
DS1220 2K x 8 24 pin Nonvolatile SRAM
DS1225 8K x 8 28 pin Nonvolatile SRAM
DS1235 32K x 8 28 pin Nonvolatile SRAM
DS1245 128K x 8 32 pin Nonvolatile SRAM
DS1200 1024 bit Serial SRAM



INTELLIGENT SOCKETS

Often, after a design is complete, the manufacturer may desire to enhance functionality because of increased competition from newer products. The equipment manufacturer is forced either to avoid adding features or design a new system. Dallas Semiconductor has incorporated active electronics in connectors which can be plugged into a system and add capabilities without requiring substantive changes in the existing system. For example, many systems manufacturers desire the capability to make RAMs in existing systems nonvolatile. In this instance, they can unplug a memory circuit in a system currently in use, plug the SmartSocket into that space, and plug the memory circuit into the SmartSocket. Another example is a requirement in many existing systems to monitor and record time of day.The SmartWatch plugs into existing systems and keeps time of day to hundredths of a second while also making memory circuits nonvolatile.

DS1213 SmartSocket-makes CMOS RAM nonvolatile
DS1216 SmartWatch- adds the ability to time stamp and date events
DS1264 LCA SmartSocket-maintains logic in the absence of power



TIMEKEEPING

Systems benefit by knowing the time-of-day, but the use of this feature has been limited by its expense and high component count. A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. The DS1287 RealTime replaces 20 parts previously used in the IBM AT and PS/2 compatible computers including an MC146818 Real Time Clock plus RAM.

DS1202 Serial Timekeeper
DS1215 Timechip
DS1287 Real Time
DS1286 WatchDog

USER INSERTABLE MEMORY

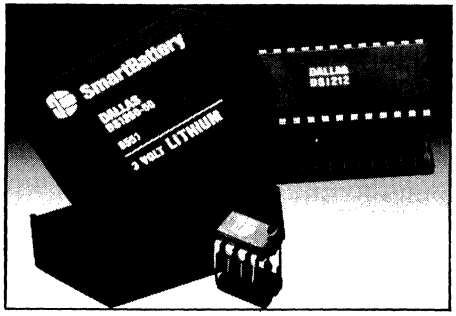
Manufacturers of equipment often wish to facilitate user configuration of their standard products. In many instances, user insertable solid state memories offer distinct advantages over alternative media, such as magnetic tape or disk. Such memories, however, demand specialized packaging capable of withstanding harsher environmental conditions than those normally encountered by semiconductor memory circuits. A family of Nonvolatile SRAMs has been specifically developed to address this application sector. These products range in density from1024 bits to 32,000,000 bits, the largest of which replaces rotating memory subsystems in certain personal computer systems.

DS1201 1K bit Electronic Tag
DS1217A up to 256K bit Nonvolatile Read/Write Cartridge
DS1217M up to 4M bit Nonvolatile Read/Write Cartridge
DS6010 P.C. Port
DS9020 Cartridge Clip

SECURITY PRODUCTS

In an information age, there is an increasing demand to provide security for intellectual property and other data beyond legal measures currently available. Prominent examples are publishers and authors of premium-priced personal computer software who have strong motivation to protect their products from unauthorized use. Software based copy protection systems interfere with the need to make legitimate backup copies or execution from hard disks. The Electronic Key is a postage stamp-sized package that is distributed with each software package sold and must be present whenever users want to use the controlling access to buildings, automobiles and other equipment.

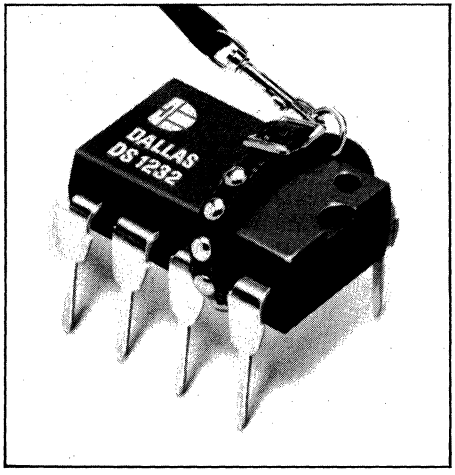
DS1204 Electronic Key
DS1207 Time Key
DS1255 Key Ring
DS1255C Evaluation Kit for IBM P.C.



INTEGRATED BATTERY BACKUP

Microprocessor based systems lose information when affected by a loss of power. When system power is resumed, the task that was being performed at the time of power loss must be re-started. Uninterruptible power supplies have historically been provided as relatively expensive, bulky, external units. A solution to this problem is necessitated in industrial automation applications and in systems which are located in remote sites or otherwise difficult to reprogram when information is lost. Integrated Battery Backup consists of a three part chip set which operates in three steps. First, the Power Monitor warns a microprocessor of an impending power failure before it happens, providing time for critical data to be stored in nonvolatile memory before system power is lost. Second, the Nonvolatile Controller/ Decoder converts RAM into nonvolatile memories and safeguards against RAM data loss during power up and down transients, by automatically switching to battery power when system power failure occurs. Third, the SmartBattery supplies uninterruptible power in the absence of system power to maintain data in nonvolatile memory.

DS1210 Single RAM Controller
DS1221 Four RAM Controller
DS1211 Eight RAM Controller
DS1212 Sixteen RAM Controller
DS1234 Conditional RAM Controller
DS1231 Power Monitor
DS1260 SmartBattery
DS1259 BatteryManager
DS1237 DRAM Nonvolatizer

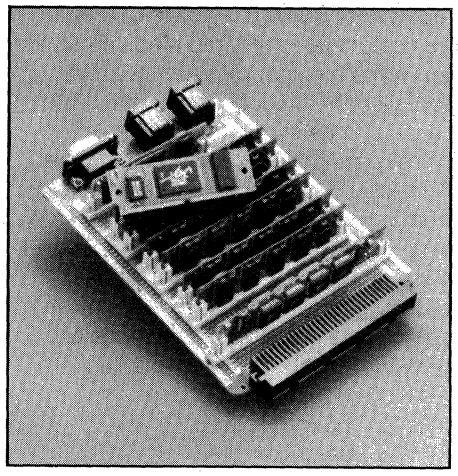


SYSTEM EXTENSION

These CMOS products extend the usefulness of systems without encumbering design. The MicroMonitor acts as a "watchdog" for system malfunction by checking the three most important indicators of correct microprocessor operation-power supply, software execution and override push-button. If it detects a problem, the MicroMonitor shuts down the system, then resets it for correct operation. The Eliminator replaces the equivalent of an 8 or 16 station manual DIP switch, thus eliminating burdensome hand setting of mechanical switches. Five volt powered RS232 transceivers are available in both dual and triple versions. The same five volt supply

that powers logic generates RS232 voltage levels.

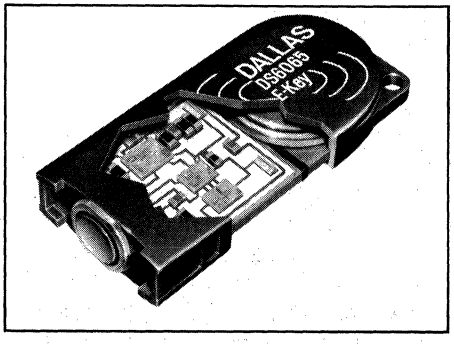
DS1232 MicroMonitor
DS1236 MicroManager
DS1290/91 Eliminator, 8-Station
DS1292/93 Eliminator,16-Station
DS1206 Phantom Interface
DS1223 Configurator
DS1222 Bank Switch
DS232/DS1228 R232 Transceiver, Dual
DS1229 RS232 Transceiver, Triple
DS1275 RS-232 Line Powered Transceiver



SipStik™Prefabs

Systems snap together with SipStik sub-assemblies from Dallas Semiconductor. SipStiks are leadless carriers of components with high silicon content using JEDEC standard configurations. These low profile form factor permits high density yet offers the advantages of modularity. Their major building blocks are pretested and ready for final assembly into a planar motherboard fitted with AMP MicroEdge connectors as required by a particular application.

DS2217 SRAM SipStik
DS2219 DRAM SipStik
DS2250 Soft Micro SipStik
DS2250T Time Micro SipStik
DS2245 Soft Modem SipStik
DS2249 Data Access Arrangement SipStik
DS2212 FIFO SipStik
DS2280 T1 SipStik
DS2268 Speech Compression SipStik
DS6040 Wireless SipStik

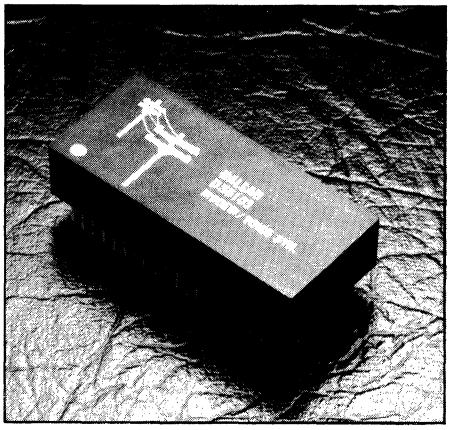


WIRELESS PRODUCTS

Proximity Tags and Proximity Keys can communicate with a personal computer using CMOS Micropower Receiver/1-or-2-to 3 Wire Converter chips and a base RF Communicator. The chips contain wake-up circuitry, amplifiers, filters, timing generators, waveform interpreters, formating and control logic necessary to form a bi-directional short-range link between portable units and bases. The ultra low power consumption of the chips enable a single 3 volt lithium energy cell to be a permanent source of power for receiving, storing, and transmitting data.

DS1203 MicroPower Receiver
DS1209 1 or 2-to 3-Wire Converter
DS1280 Bytewide to Serial Converter

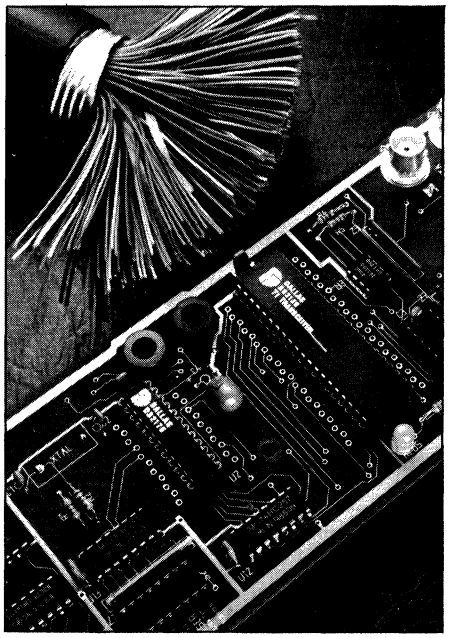
DS6068 RF Communicator
DS6065 Proximity Key
DS6066 Proximity Tag
DS2265 Wireless SipStik
DS6068K Wireless Starter Kit



MODEM

These miniature components comply with FCC part 68 registration. The DS6101 Modem is Bell 212A compatible (1200/300 bps) with DTMF generation/ detection,audio mode operation, and advanced line monitoring functions. The DS6103 Modem provides voice synthesis. The DS6112 and DS2249 Data Access Arrangements (DAA) are also available as a stand alone interface to the public switch telephone network.

DS6101 1200 bps Modem
DS6103 1200 bps Modem with Voice
DS6112 DAA
DS2245 1200 bps Soft Modem SipStik
DS2249 DAA SipStik
DS6070 Tele Micro Cartridge



T1/CEPT TELECOMMUNICATONS

An emerging and rapidly growing market exists for high capacity voice, data and video transmission. High capacity digital links in North America and Europe are known as T-1 and CEPT, respectively. Circuits designed for these protocols can substantially shorten the time required for OEMs to develop products that access these networks and can reduce system sizes. A comprehensive chip set developed by Dallas Semiconductor addresses the requirements of these protocols and includes an integrated circuit that doubles the capacity of existing voice communication links through digital signal processing compression techniques. Complete product specifications available in a supplemental 1989 telecommunications data book .

DS2180A Transceiver, T1
DS2181 Transceiver, CEPT
DS2175 Transmit/Receive Elastic Store
DS2176 Receive Elastic Store
DS2186 Transmit Line Interface
DS2187 Receive Line Interface
DS2190 Network Interface Unit
DS2167 ADPCM Processor
DS2280 T1 SipStik
DS2268 Speech Compression SipStik

Product Data Sheets

Silicon Timed Circuits

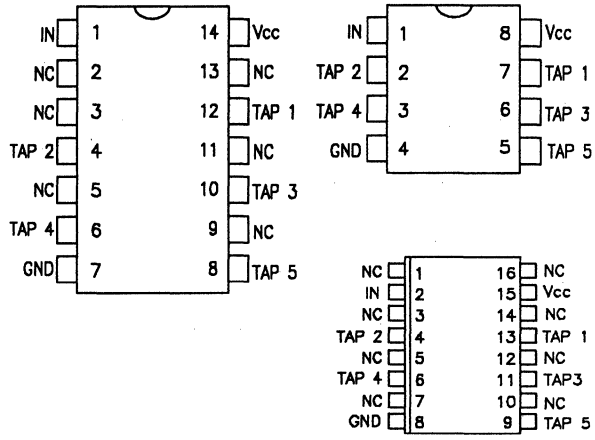
Dallas Semiconductor
5 Tap Silicon Delay Line

DS1000 14-Pin DIP
DS1000M 8-Pin DIP
DS1000S 16-Pin SOIC

FEATURES

- All silicon time delay
- 5 taps equally spaced
- Delays are stable and precise
- Both leading and trailing edge accuracy
- Standard 14-pin DIP, 8-pin DIP or 16-pin SOIC
- Delay tolerance +/- 5%
- Economical
- Auto-insertable
- Low power CMOS
- TTL compatible
- Custom delays available

PIN CONNECTIONS



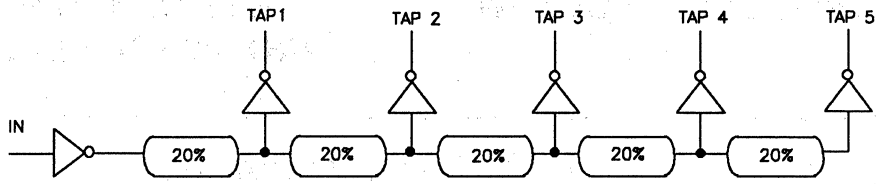
PIN NAMES

TAP 1-TAP 5	- TAP Output Number
Vcc	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1000 Series Delay Lines have five equally spaced TAPS providing delays from 10 ns to 500 ns. These devices are offered in a standard 14-pin DIP, which is pin compatible with hybrid delay lines. Alternatively, 8-pin DIPs and surface mount packages are available to save p.c. board area. Since the DS1000 series is an all silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1000 Series Delay Lines provide a nominal accuracy of +/- 5% or +/- 2 ns, which ever is greater. The DS1000 Delay Line reproduces the input logic level at the output after a fixed delay as specified by the dash number extension of the part number. The DS1000 is designed to reproduce both leading and trailing edge with equal precision. Each tap is capable of driving up to ten 74LS type loads.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP2	TAP3	TAP4	TAP5
DS1000-50	10ns	20ns	30ns	40ns	50ns
DS1000-60	12ns	24ns	36ns	48ns	60ns
DS1000-75	15ns	30ns	45ns	60ns	75ns
DS1000-100	20ns	40ns	60ns	80ns	100ns
DS1000-125	25ns	50ns	75ns	100ns	125ns
DS1000-150	30ns	60ns	90ns	120ns	150ns
DS1000-175	35ns	70ns	105ns	140ns	175ns
DS1000-200	40ns	80ns	120ns	160ns	200ns
DS1000-250*	50ns	100ns	150ns	200ns	250ns
DS1000-500*	100ns	200ns	300ns	400ns	500ns

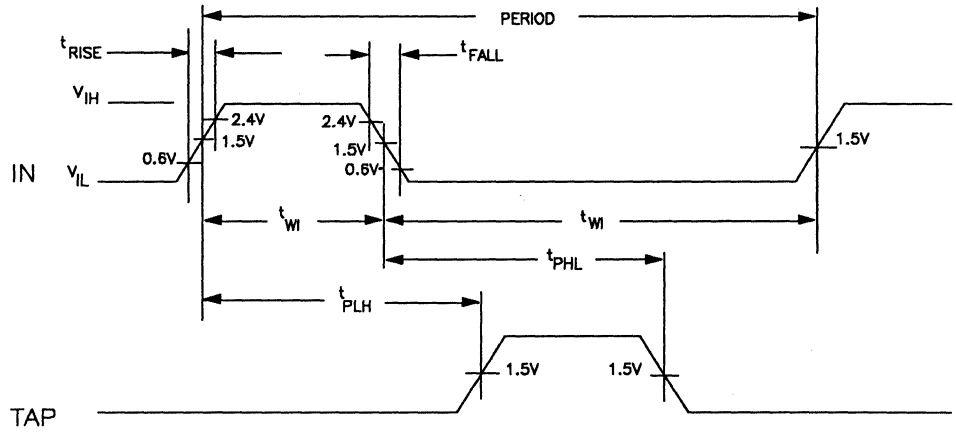
*These products will be discontinued in 1989 and replaced by equivilant delay times with the DS1005

ABSOLUTE MAXIMUM RATINGS*

Voltage on a pin to ground:-1.0Vto + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C
Soldering
temperature: 260°C for 10 seconds
Short circuit output current: 50mA for 1 second

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TIMING DIAGRAM SILICON DELAY LINE Figure 2



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time) The elapsed time between the 80% and the 20% point on the railing edge of the input pulse.

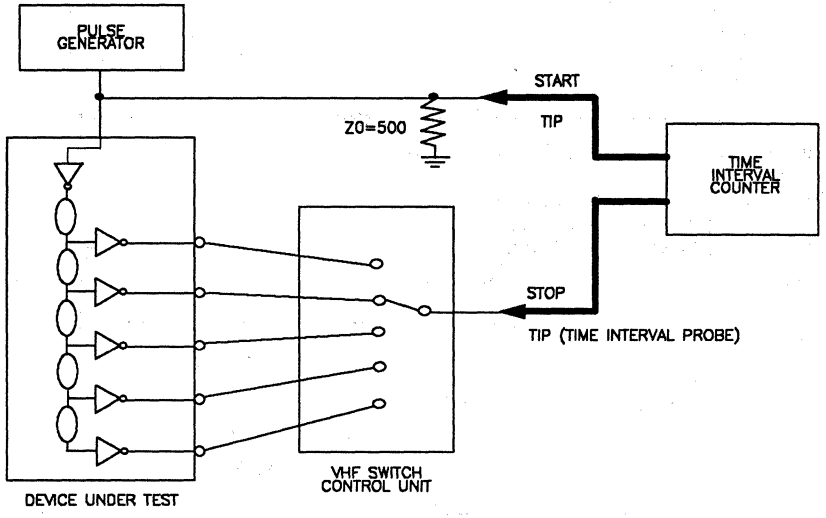
t_{PLH} (Time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling) The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

NOTES:

1.)All voltages are referenced to ground.
2.)Measured with outputs open, minimum period.
3.)Vcc=5V @25°C Delays accurate on both rising and falling edges within +/- 2 ns, or 5%.
4.)See Test Conditions (following page).

TEST CIRCUIT Figure 3



TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1000. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

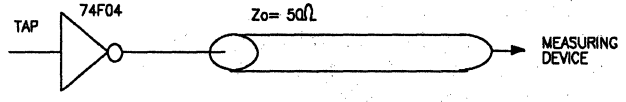
Ambient Temperature: 25°C+/-3°C
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High = 3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50 ohm Max.
Rise and Fall Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 500 ns
Period= 1 us

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:

Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.



D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5.0V +/- 5%)

PARAMETER	SYMBOL COND.	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		5.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \leq VI \leq Vcc$	-1.0		1.0	uA	
Active Current	I_{CC}	Vcc= Max; Period= Min.			35.0	mA	2
High Level Output Current	I_{OH}	Vcc= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	Vcc= Min. V_{OL}= 0.5V	12.0			mA	

A.C. ELECTRICAL CHARACTERISTICS

(T_A= 25°C, Vcc=5V+/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of TAP 5			ns	
Input to TAP delay (leading edge)	t_{PLH}	note 3	Table 1	note 3	ns	4
Input to TAP Delay (trailing edge)	t_{PHL}	note 3	Table 1	note 3	ns	4
	Period	4 (t_{WI})			ns	

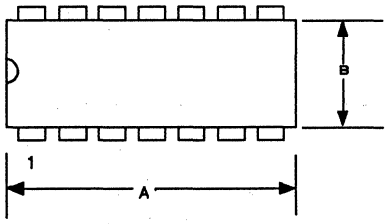
CAPACITANCE

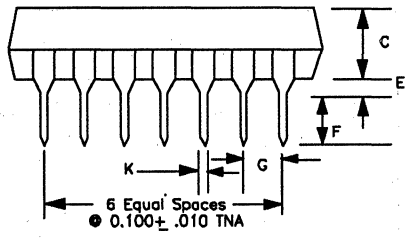
(T_A= 25° C)

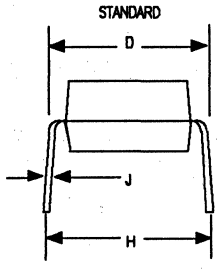
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

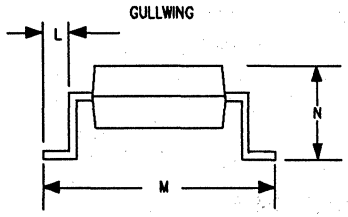
SILICON DELAY LINE
DS1000
14-PIN DIP

DIM	INCHES	
	MIN.	MAX.
A	0.740	0.780
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.310
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021
L	0.040	0.060
M	0.370	0.420
N	0.160	0.180



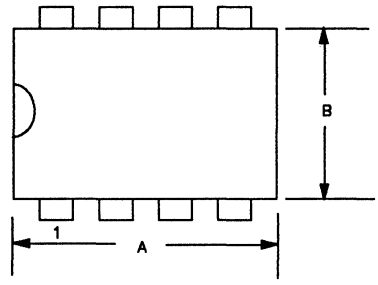


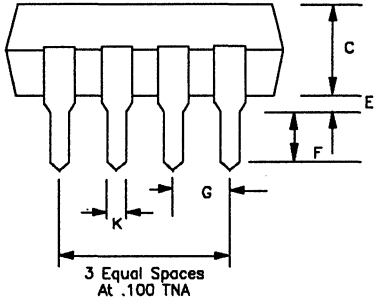


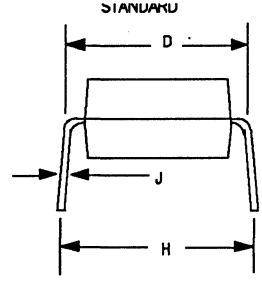


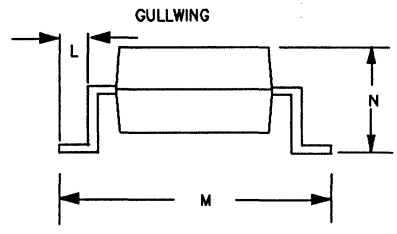
SILICON DELAY LINE
DS1000M
8-PIN DIP

DIM	INCHES	
	MIN.	MAX.
A	0.345	0.400
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021
L	0.040	0.060
M	0.370	0.420
N	0.160	0.180



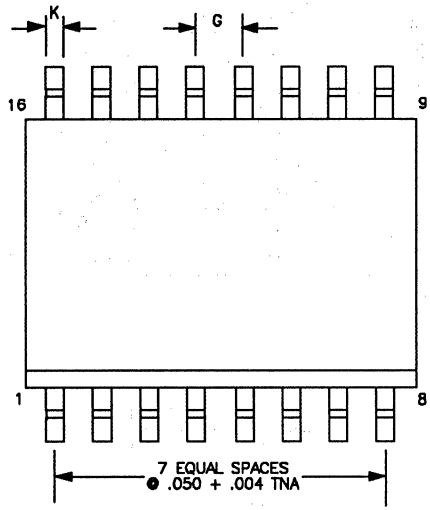


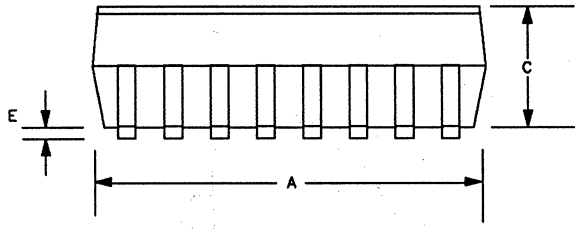


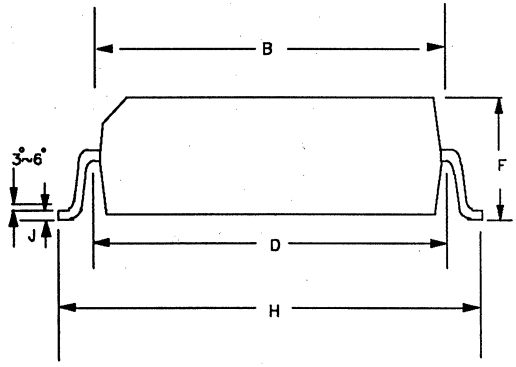


SILICON DELAY LINE
DS1000S
16-PIN SOIC

DIM	INCHES	
	MIN.	MAX.
A	0.403	0.411
B	0.290	0.296
C	0.089	0.095
D	0.325	0.330
E	0.008	0.012
F	0.097	0.105
G	0.046	0.054
H	0.402	0.410
J	0.006	0.011
K	0.013	0.019





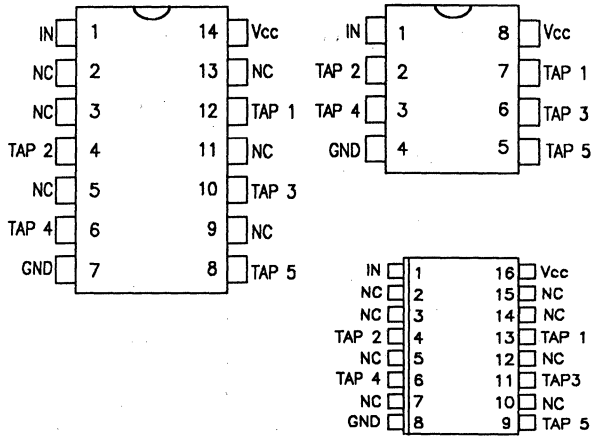


Dallas Semiconductor
5 TAP SILICON DELAY LINE

DS1005 14-Pin DIP
DS1005M 8-Pin DIP
DS1005S 16-Pin SOIC

FEATURES
- All silicon time delay
- 5 TAPS equally spaced. Delay tolerance ± 2 ns or ± 2% whichever is greater
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Auto-insertable
- Low power CMOS
- TTL compatible
- Custom delays available

PIN CONNECTIONS



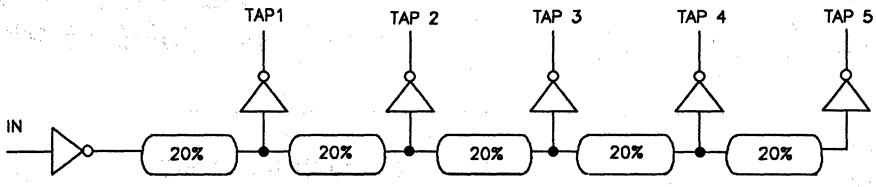
PIN NAMES

TAP 1-TAP 5	- TAP Output Number
Vcc	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1005 Delay Line Product Family provides five equally spaced TAPS with delays ranging from 10 ns to 500 ns, with an accuracy of ± 2 ns or 2%. These devices are offered in a standard 14 pin DIP, compatible with existing delay line products. A space saving 8 pin -DIP is also available. The 14 pin DIP, the 8 pin -DIP, and SOIC packaging are available in a surface mountable "gullwing" construction. Since the DS1005 is an all silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1005 Delay Line reproduces the input logic level at each TAP after the fixed delay specified by the "dash number" in Table 1. The device is designed to produce both the leading and trailing edge delays with equal precision. Each TAP is capable of driving up to ten 74LS loads.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP2	TAP3	TAP4	TAP5
DS1005-75*	15ns	30ns	45ns	60ns	75ns
DS1005-100	20ns	40ns	60ns	80ns	100ns
DS1005-125	25ns	50ns	75ns	100ns	125ns
DS1005-150	30ns	60ns	90ns	120ns	150ns
DS1005-175	35ns	70ns	105ns	140ns	175ns
DS1005-200	40ns	80ns	120ns	160ns	200ns
DS1005-250*	50ns	100ns	150ns	200ns	250ns
DS1005-500*	100ns	200ns	300ns	400ns	500ns

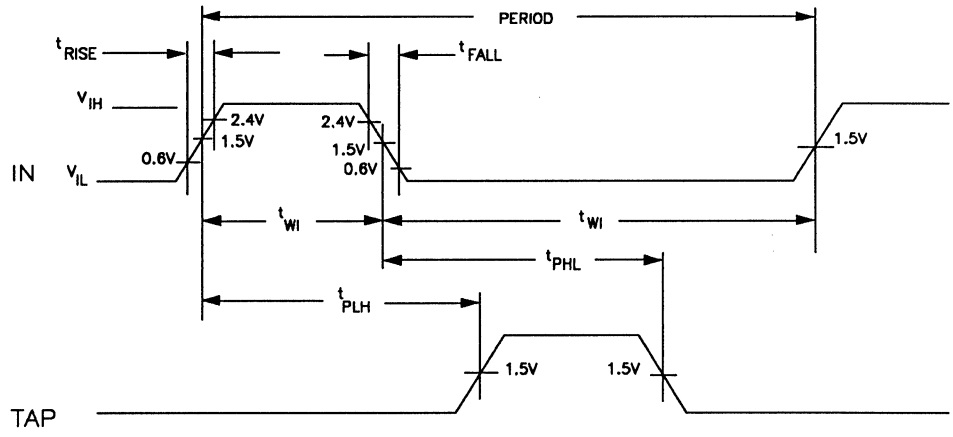
*Consult Dallas Semiconductor for availability

ABSOLUTE MAXIMUM RATINGS*

Voltage on a pin to ground: -1.0Vto + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C
Soldering temperature: 260°C for 10 seconds
Short circuit output current: 50mA for 1 second

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TIMING DIAGRAM- SILICON DELAY LINE Figure 2



TERMINOLOGY

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time) The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

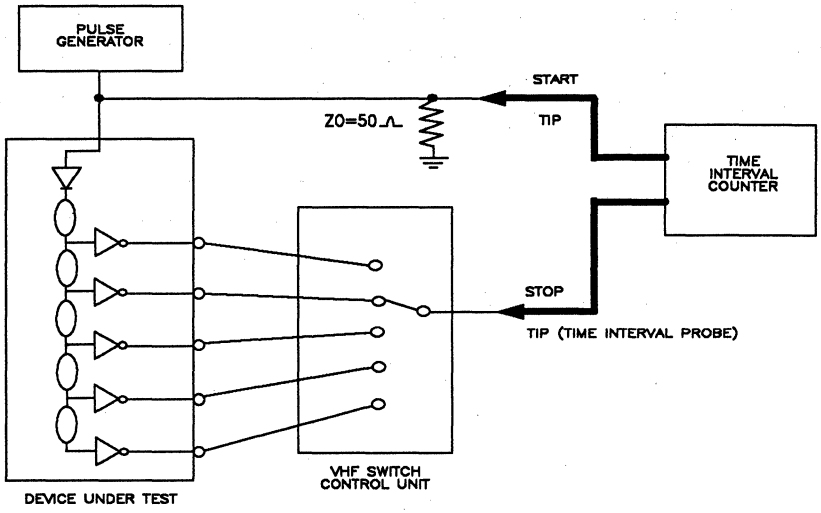
t_{PLH} (Time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

t_{PHL} (Time Delay, Falling) The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any TAP output pulse.

NOTES

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period.
3. Vcc=5V @25°C Delays accurate on both rising and falling edges within +/- 2 ns.
4. See Test Conditions (following page).
5. The combination of temperature variations between 0°C and 70°C and voltage variations between 4.75 volts and 5.25 volts produce a worst case delay shift of +/- 5%.

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1005. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS-INPUT:

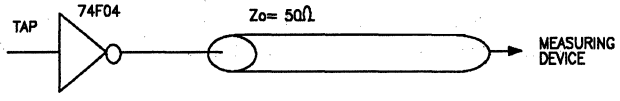
Ambient Temperature: 25°C+/-3°C
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High = 3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50 ohm Max.
Rise and Fall Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 500 ns
Period= 1us

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:

Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.



D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, Vcc = 5.0V +/- 5%)

PARAMETER	SYMBOL	TEST COND.	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	Vcc		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		5.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	0.0V≤ VI≤Vcc	-1.0		1.0	uA	
Active Current	I_{CC}	Vcc= Max; Period= Min.		40.0	70.0	mA	2
High Level Output Current	I_{OH}	Vcc= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	Vcc=Min V_{OL}=0.5V	12.0			mA	

A.C. ELECTRICAL CHARACTERISTICS (T_A= 25°C, Vcc=5V+/- 5%)

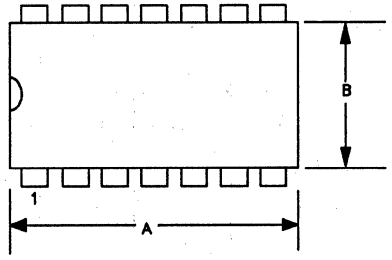
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Pulse Width	t_{WI}	40%ofTAP5			ns	
Input to TAP delay (leading edge)	t_{PLH}	note 3	Table 1	note 3	ns	4,5
Input to TAP Delay (trailing edge)	t_{PHL}	note 3	Table 1	note 3	ns	4,5
	Period	4 (tWI)			ns	

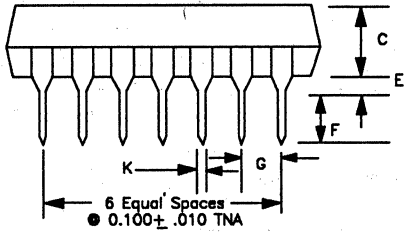
CAPACITANCE (T_A=25°C)

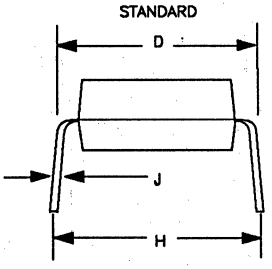
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Capacitance	C_N		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

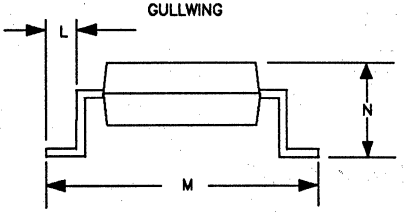
Silicon Delay Line
DS1005
14-Pin DIP

DIM.	INCHES	
	MIN.	MAX.
A	0.740	0.780
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	.320	.370
J	0.008	0.012
K	0.015	0.021
L	0.040	0.060
M	0.370	0.420
N	0.160	0.180



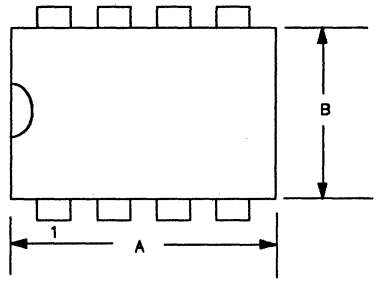


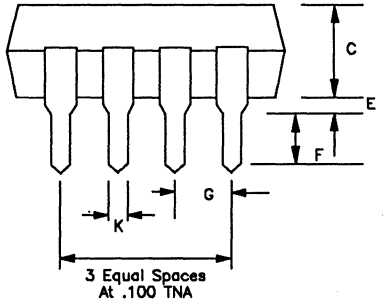


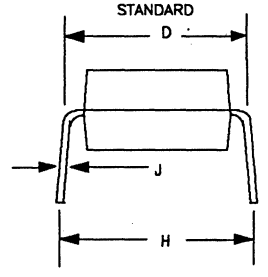


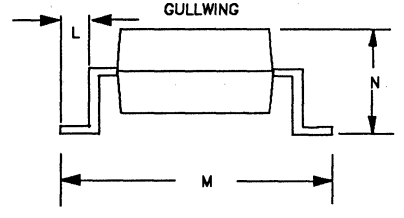
Silicon Delay Line
DS1005M
8-Pin DIP

DIM.	INCHES	
	MIN.	MAX.
A	0.345	0.400
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	.320	.370
J	0.008	0.012
K	0.015	0.021
L	0.040	0.060
M	0.370	0.420
N	0.160	0.180

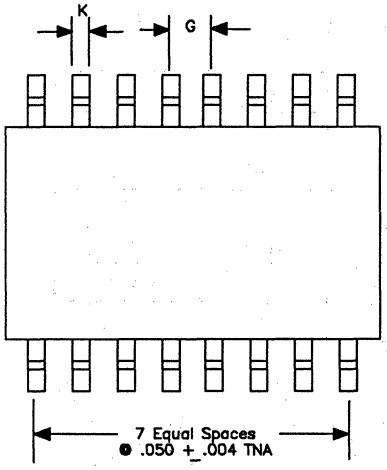




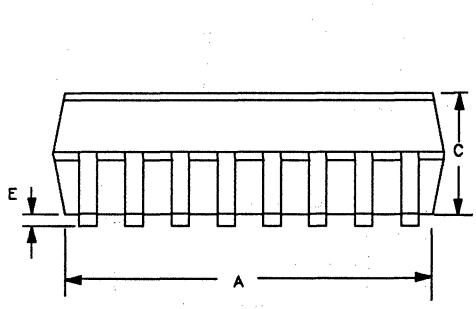


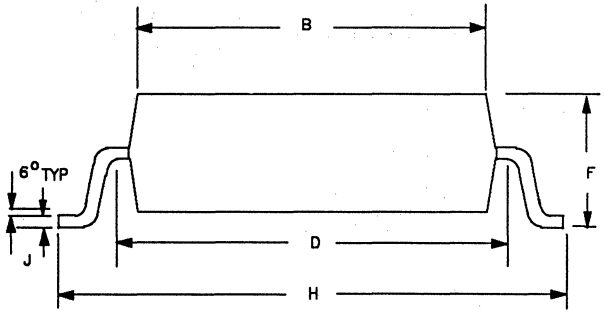


Silicon Delay Line
DS1005S
16-Pin SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019





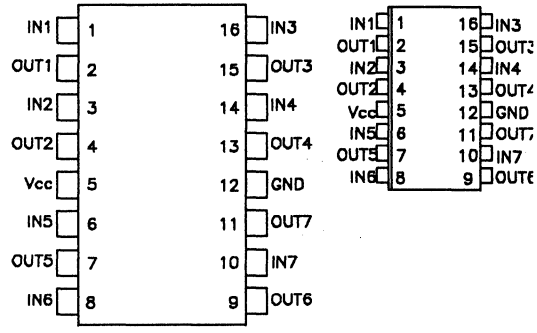
Dallas Semiconductor
7 -In-1 Silicon Delay Line

PRELIMINARY
DS1007 16-Pin DIP
DS1007S 16-Pin SOIC

FEATURES

- All silicon time delay
- 7 independent logic buffered delays
- Accuracy of +/- 2 ns @ 25°C
- Four delays can be custom set between 3 ns and 7 ns
- Three delays can be custom set between 8 ns and 20 ns
- Leading edge precision
- Auto-insertable 16 pin DIP
- Surface mount 16 pin SOIC
- Low power CMOS
- TTL compatible

PIN CONNECTIONS



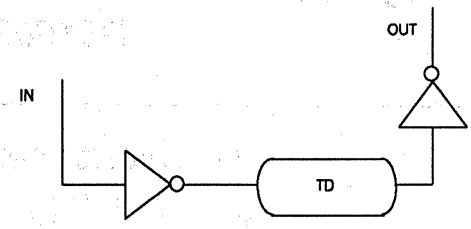
PIN NAMES

IN1 - IN7	- Inputs
Out1- Out7	- Outputs
GND	- Ground
Vcc	- +5 Volts

DESCRIPTION

The DS1007 Delay Line provides seven independent delay times which are set by Dallas Semiconductor to the customer's specification. The delay times can be set from 3 ns to 20 ns with an accuracy of +/- 2 ns at room temperature. The device is offered in both a 16 pin DIP and a 16 pin SOIC. Since the DS1007 is an all silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1007 reproduces the input logic level at the output after the fixed delay as specified by the customer specification.

LOGIC DIAGRAM Figure 1



INPUT PULSE WIDTH > 100% OF DELAY

PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

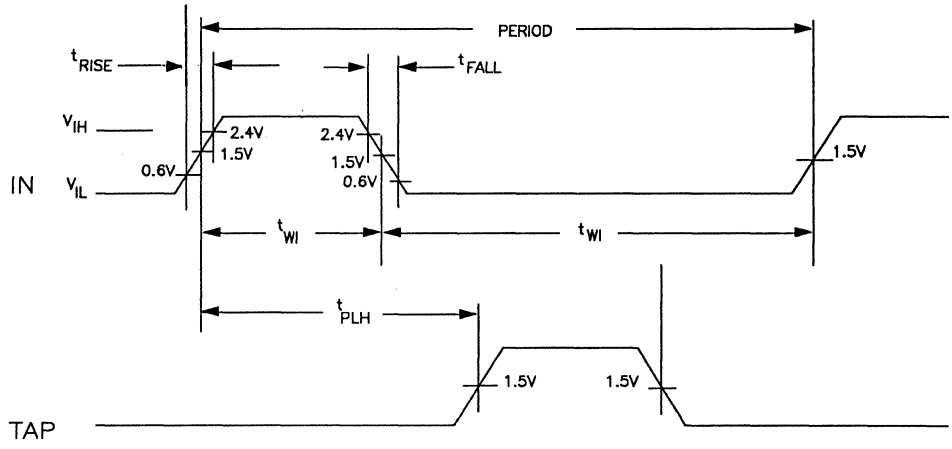
INPUT NO.	OUTPUT DELAY
INPUT 1	3ns-8ns
INPUT 2	3ns-8ns
INPUT 3	3ns-8ns
INPUT 4	3ns-8ns
INPUT 5	9ns-20ns
INPUT 6	9ns-20ns
INPUT 7	9ns-20ns

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin to ground: -1.0Vto + 7.0V
Operating temperature: 0°C° to 70°C
Storage temperature: -55°C to + 125°C
Soldering temperature: 260°C for 10 seconds
Short circuit output current: 50mA for 1 second

* This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TIMING DIAGRAM SILICON DELAY LINE Figure 2



TERMINOLOGY

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

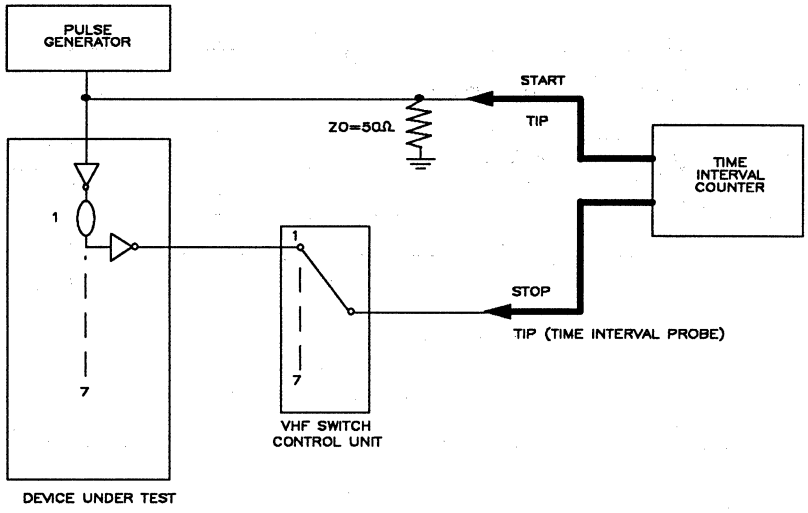
t_{FALL} (Input Fall Time) The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

NOTES:

1.) All voltages are referenced to ground.
2.) Measured with outputs open, minimum period.
3.) Vcc=5V @25°C Delays accurate on rising edges within +/- 2 ns.
4.) See Test Conditions (following page).

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1007. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature: 25°C+/-3°C
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High = 3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50 ohm Max.
Rise and Fall Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 100ns

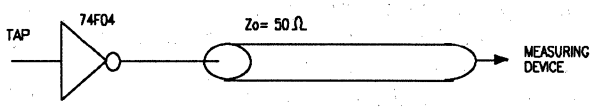
OUTPUT:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

NOTE:

Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising edge.

Period = 200ns



D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5.0V+/- 5%)

PARAMETER	SYMBOL COND.	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vcc		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		5.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	0.0V≤VI≤Vcc	-1.0		1.0	uA	
Active Current	I_{CC}	Vcc= Max; Period= Min.		40.0	70.0	mA	2
High Level Output Current	I_{OH}	Vcc= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	Vcc= Min. V_{OL}= 0.5V	1.0			mA	

A.C. ELECTRICAL CHARACTERISTICS

(T_A= 25°C, Vcc=5V+/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100%			ns	
Input to Output (leading edge)	t_{PLH}	note 3		note 3	ns	4
	Period	3 (t_{WI})			ns	

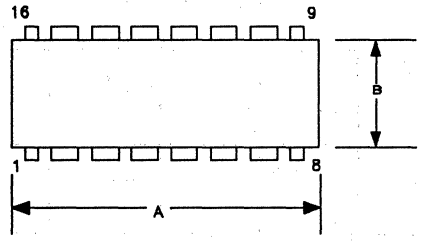
CAPACITANCE

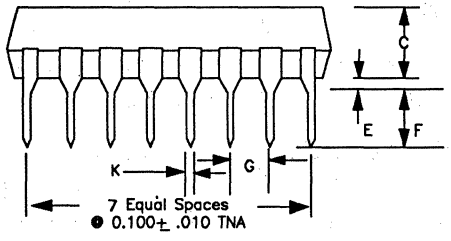
(T_A= 25° C)

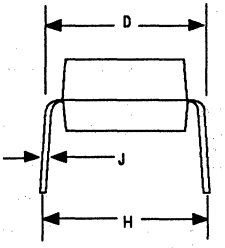
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

SILICON DELAY LINE
DS1007
16 Pin DIP

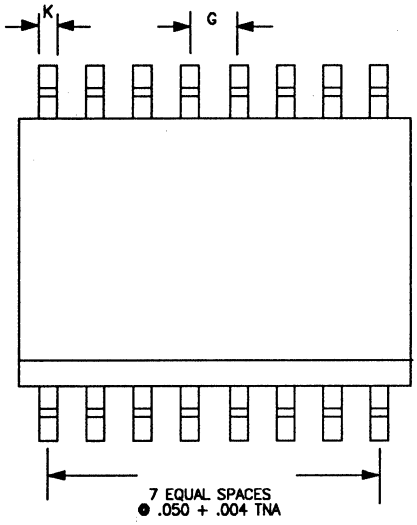
DIM.	INCHES	
	MIN.	MAX.
A	0.740	0.780
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021



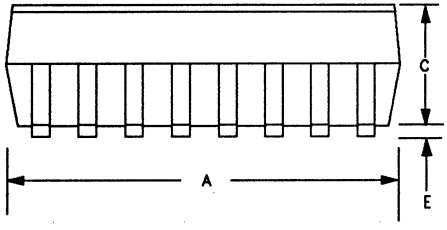


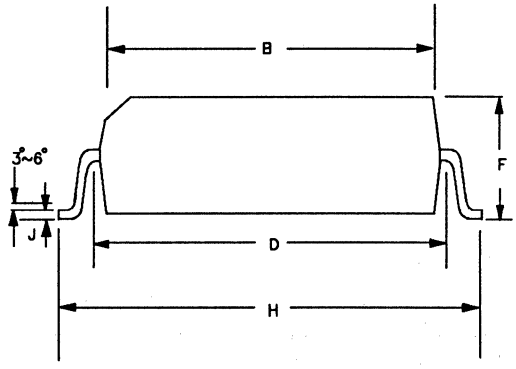


SILICON DELAY LINE
DS1007S
16 Pin SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



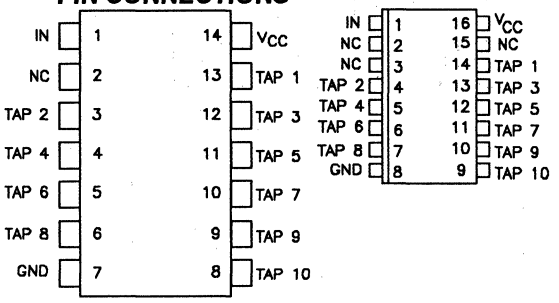


Dallas Semiconductor
10 TAP Silicon Delay Line

DS1010 14 Pin Dip
DS1010S 16 Pin SOIC

FEATURES
- All silicon time delay 10 TAPS equally spaced
- Delays are stable and precise
- Leading and trailing edge accuracy
- Standard 14 pin DIP or 16 pin SOIC
- Delay tolerance +/- 5%
- Economical
- Auto-insertable
- Low power CMOS
- TTL compatible
- Custom delays available

PIN CONNECTIONS



PIN NAMES

TAP1-TAP10	- TAP Output Number
Vcc	- 5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1010 Series Delay Line has ten equally spaced TAPS providing delays from 10 ns to 500 ns. The devices are offered in a standard 14 pin DIP which is pin compatible with hybrid delay lines. Alternatively, a 16 pin SOIC is available for surface mount technology which reduces P.C. board area. Since the DS1010 Series Delay Line is an all silicon solution, better economy is achieved when compared to older methods of using hybrid techniques.

The DS1010 Series Delay Lines provide a nominal accuracy of +/- 5% or +/- 2 ns, which ever is greater. The DS1010 Delay Line reproduces the input logic level at the output after a fixed delay as specified by the dash number extension of the part number. The DS1010 is designed to produce both leading and trailing edge with equal precision. Each TAP is capable of driving up to ten 74LS type loads.

LOGIC DIAGRAM Figure1

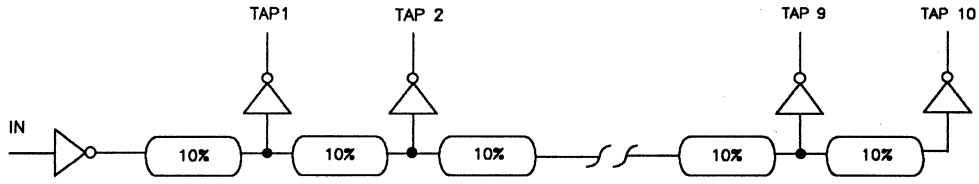


TABLE 1: PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH})

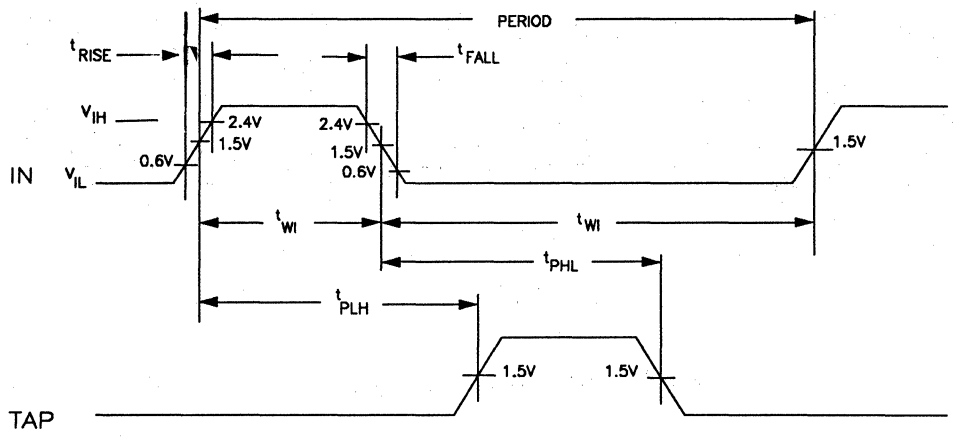
CATALOG P/N	TOTAL DELAY	DELAY/TAP (NS)
DS1010-100	100	10
DS1010-150	150	15
DS1010-200	200	20
DS1010-250	250	25
DS1010-300	300	30
DS1010-350	350	35
DS1010-400	400	40
DS1010-500	500	50

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin
to ground: -1.0Vto + 7.0V
Operating temperature: 0°Co to 70°Co
Storage temperature: -55°C to + 125°C
Soldering
temperature: 260°C for 10 seconds
Short circuit output
current: 50mA for 1 second

*This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TERMINOLOGY

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time) The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

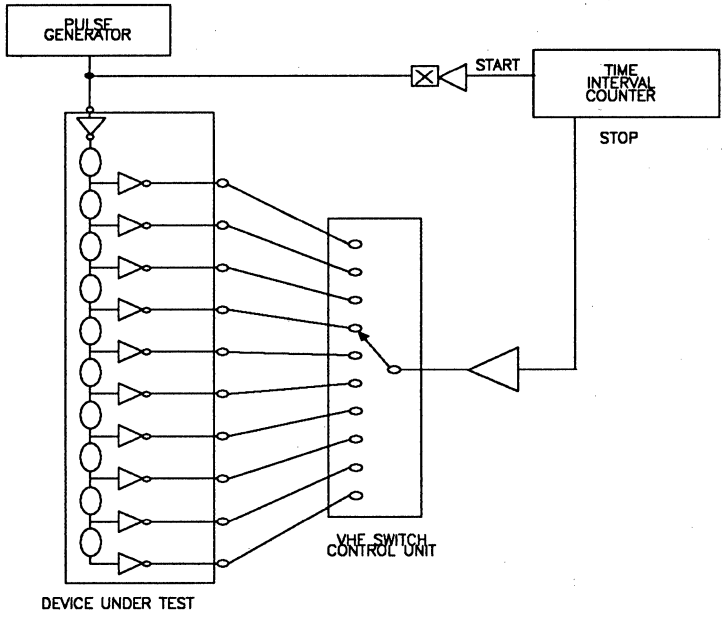
t_{PLH} (Time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

t_{PHL} (Time Delay, Falling) The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any TAP output pulse.

NOTES

1.) All voltages are referenced to ground.
2.) Measured with outputs open, minimum period.
3.) Vcc=5V @25°C Delays accurate on both rising and falling edges within +/- 2 ns,or 5%.
4.) See Test Conditions (following page).

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1010. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

Input:

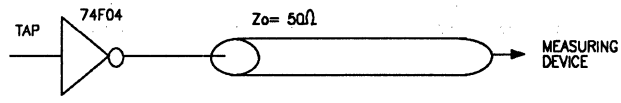
Ambient Temperature: 25°C+/-3°
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High=3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50 ohm Max.
Rise and Fall Time: 3.0 ns Max.
(measured between 0.6V and 2.4V) Width = 500 nsPeriod= 1us

NOTE:

Above conditions are for test only and do not restrict the operation of the device under otherdata sheet conditions.

Output:

Each output is loaded with a 74FO4. delay is measured at the 1.5V level on the rising and falling edge.



D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc+ 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	Vcc		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		5.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_L	$0.0 \leq V_I \leq V_{cc}$	-1.0		1.0	uA	
Active Current	I_{cc}	Vcc=Max: Period=Min.		40.0	75.0	mA	2
High Level Output Current	I_{OH}	Vcc=Min. V_{OH}=2.4V		-1.0		mA	
Low Level Output Current	I_{OL}	Vcc=Min. V_{OL}=0.5V	12.0			mA	

A.C ELECTRICAL CHARACTERISTICS

(TA= 25°C, Vcc= 5V ± 5%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Pulse Width	t_{WI}	30% of TAP 10			ns	
Input to TAP Delay (leading edge)	t_{PLH}	note 3	Table 1	note 3	ns	4
Input to TAP Delay (trailing edge)	t_{PHL}	note 3	Table 1	note 3	ns	4
	Period	$3(t_{WI})$			ns	

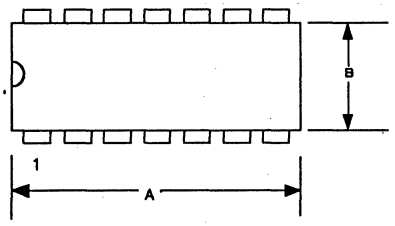
CAPACITANCE

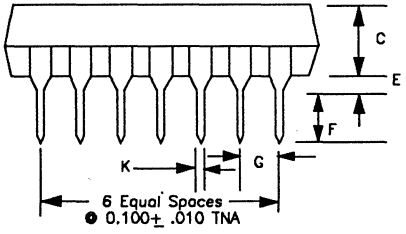
(tA= 25°C)

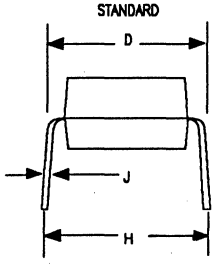
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Capacitance	CIN		5	10	pF	
Output Capacitance	COUT		5	10	pF	

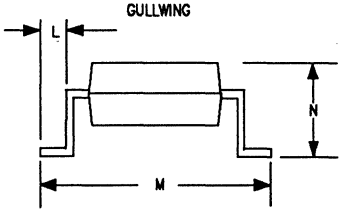
Silicon Delay Line
DS1010
14 Pin Dip

DIM.	INCHES	
	MIN.	MAX.
A	0.740	0.780
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	.320	.370
J	0.008	0.012
K	0.015	0.021
L	0.040	0.060
M	0.370	0.420
N	0.160	0.180

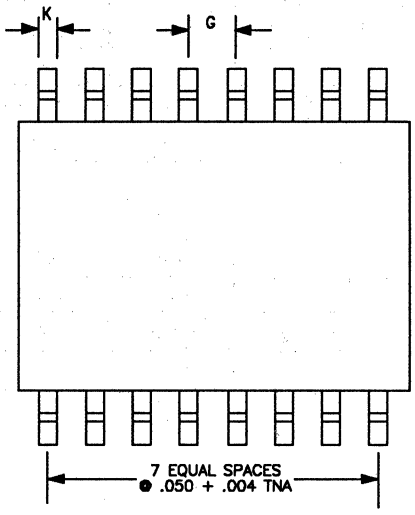




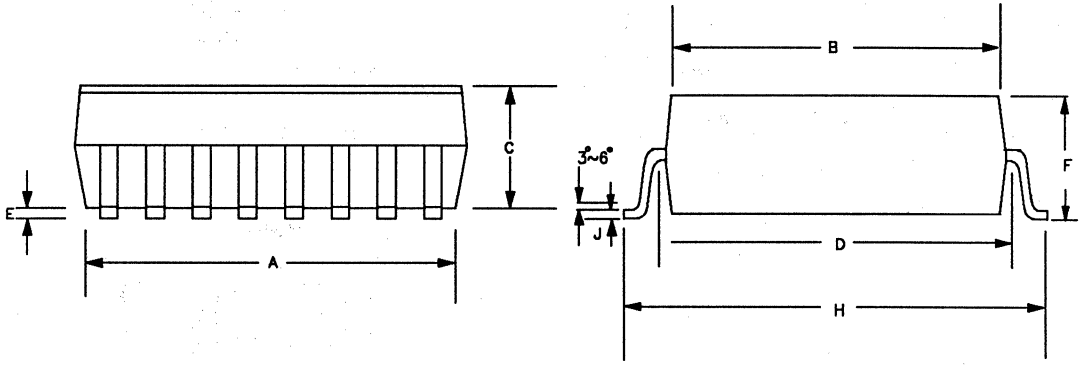




Silicon Delay Line
DS1010S
16 Pin SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



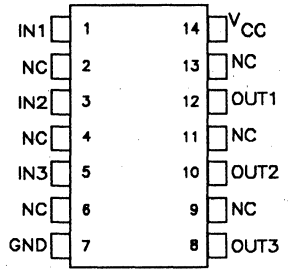
Dallas Semiconductor
3 In 1 Silicon Delay Line

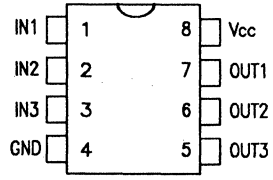
DS1013 14-Pin DIP
DS1013M 8-Pin DIP
DS1013S 16-Pin SOIC

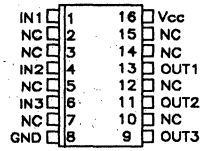
FEATURES

- All silicon time delay
- 3 independent logic buffered delays
- Delay tolerance +/- 2 ns
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Standard 14-pin DIP, 8-pinDIP or 16-pin SOIC
- Auto-insertable
- Low power CMOS
- TTL compatible
- Custom delays available

PIN CONNECTIONS







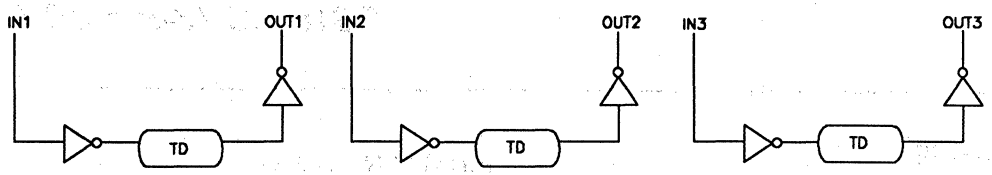
PIN NAMES

IN1, IN2, IN3	- Inputs
Out1, Out2, Out3	- Outputs
GND	- Ground
V_{CC}	- +5 Volts

DESCRIPTION

The DS1013 Series of Delay Lines has three independent logic buffered delays in a single package. The devices are offered in a standard 14-pin DIP which is pin compatible with hybrid delay lines. Alternatively 8-pin DIPS and surface mount packages are available which save P.C. board area. Since the DS1013 Series is an all silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1013 Series Delay Lines provide a nominal accuracy of +/- 2 ns for delay times ranging from 10 ns to 100 ns. The DS1013 Delay line reproduces the input logic level at the output after a fixed delay as specified by the dash number extension of the part number. The DS1013 is designed to reproduce both leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS type loads.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE Table 1 (T_{PHL}, T_{PLH})

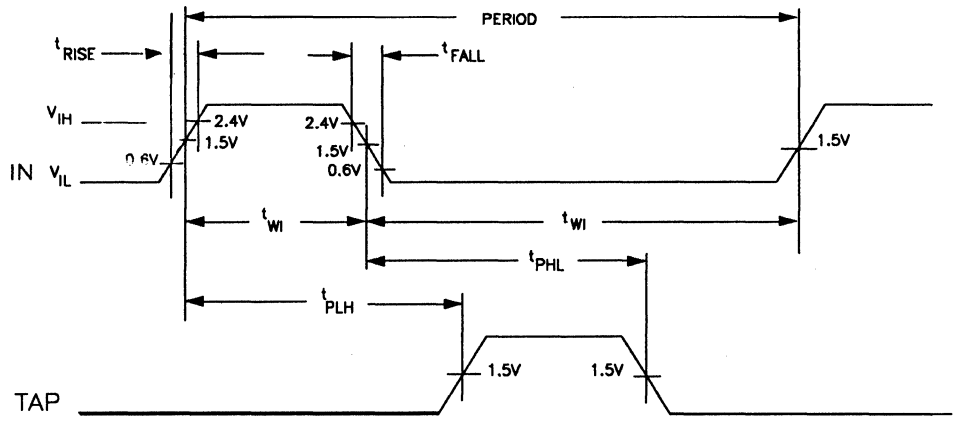
PART NO.	DELAY PER OUTPUT (ns)
DS1013-10	10/10/10
DS1013-15	15/15/15
DS1013-20	20/20/20
DS1013-25	25/25/25
DS1013-30	30/30/30
DS1013-40	40/40/40
DS1013-50	50/50/50
DS1013-60	60/60/60
DS1013-70	70/70/70
DS1013-75	75/75/75
DS1013-80	80/80/80
DS1013-90	90/90/90
DS1013-100	100/100/100

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin
to ground: -1.0Vto + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C
Soldering
temperature: 260°C for 10 seconds
Short circuit output
current: 50mA for 1 second

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TERMINOLOGY

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time) The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

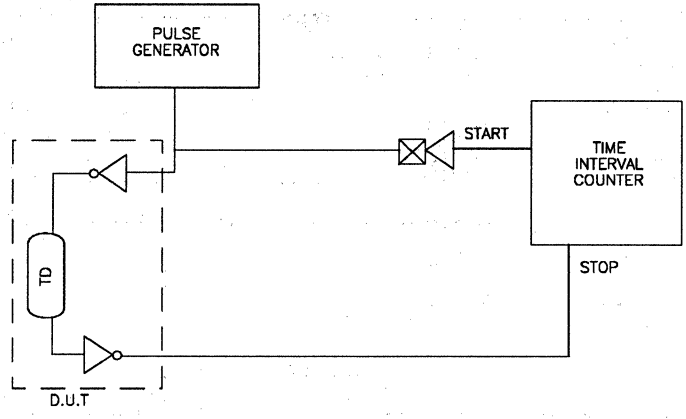
t_{PLH} (time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

t_{PHL} (Time Delay, Falling) The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any TAP output pulse.

NOTES

1.) All voltages are referenced to ground.
2.) Measured with outputs open, minimum period
3.) Vcc=5V @25°C Delays accurate on both rising and falling edges within +/- 2 ns.
4.) See Test Conditions (following page).
5.) The combination of temperature variations between 0° C and 70° C and voltage variations between 4.75 volts and 5.25 volts produce a worst case delay shift of +/- 5%.

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



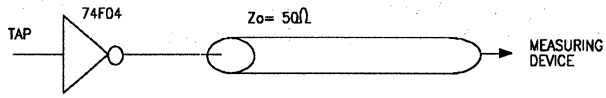
TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1013. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

Test Conditions
Input:
Ambient Temperature: 25°C+/-3°C
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High = 3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50Ω Max.
Rise and Fall Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 500 ns
Period= 1us

Note:
Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

Output:
Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.



D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C,Vcc= 5.0V+/- 5%)

PARAMETER	SYMBOL	TEST COND.	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		5.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \leq V_I \leq V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max Period= Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC}= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min V_{OL}=0.5V	12.0			mA	

A.C ELECTRICAL CHARACTERISTICS

(T_A= 25°C, Vcc=5.0V+/-5%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Pulse Width	t_{WI}	100%	t_{PLH}		ns	
Input to TAP Delay (leading edge)	t_{PLH}	note 3	Table 1	note 3	ns	4,5
Input to TAP Delay (trailing edge)	t_{PHL}	note 3	Table 1	note 3	ns	4,5
	Period	$3(t_{WI})$			ns	

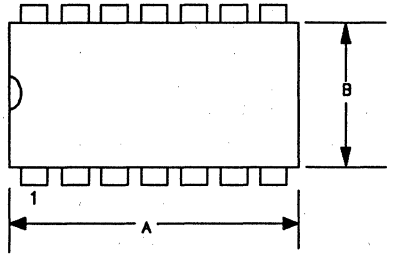
CAPACITANCE

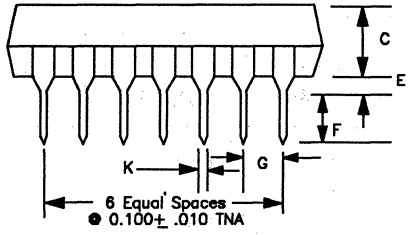
(t_A=25°C)

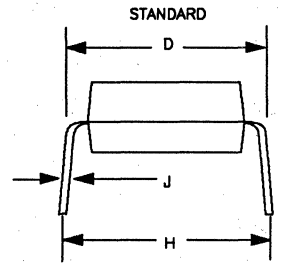
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Capacitance	C_N		5	10	pF	
Output Capacitance	C_{OUT}		5	10	pF	

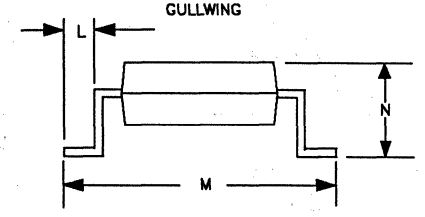
Silicon Delay Line
DS1013
14-Pin DIP

DIM.	INCHES	
	MIN.	MAX.
A	0.740	0.780
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021
L	0.040	0.060
M	0.370	0.420
N	0.160	0.180

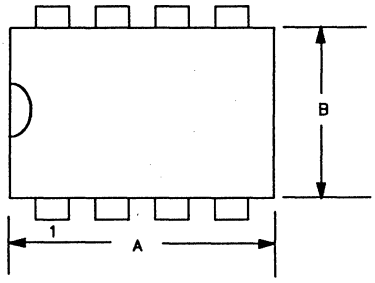




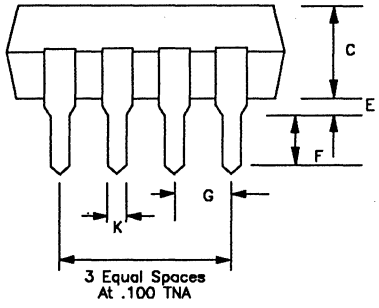


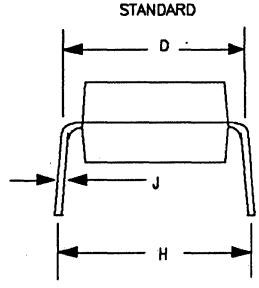


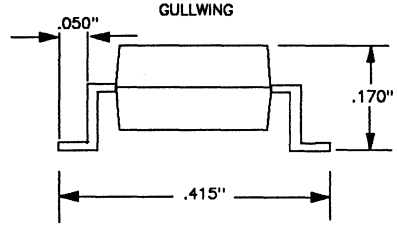
Silicon Delay Line
DS1013M
8-Pin DIP



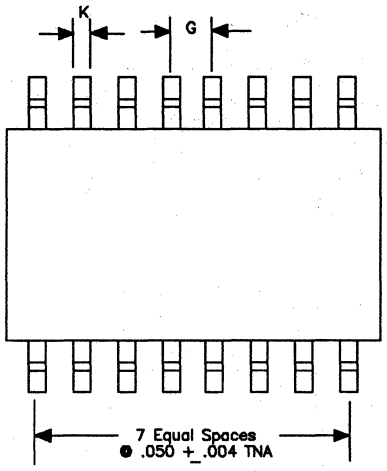
DIM.	INCHES	
	MIN.	MAX.
A	.345	.400
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021



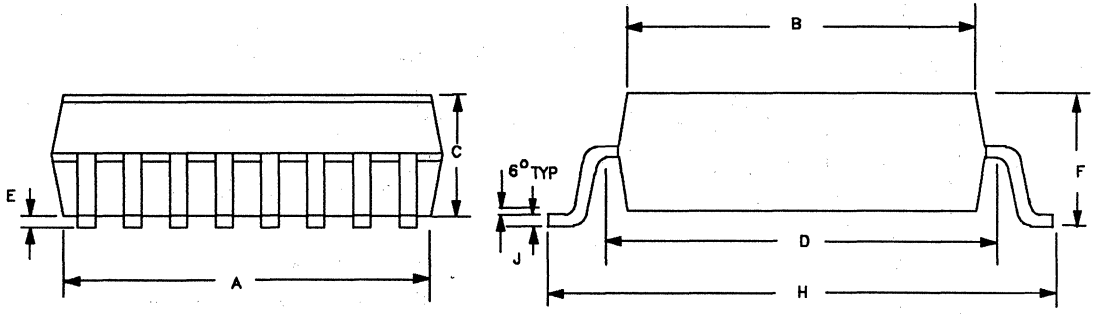




Silicon Delay Line
DS1013S
16 Pin SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



Multiport Memory

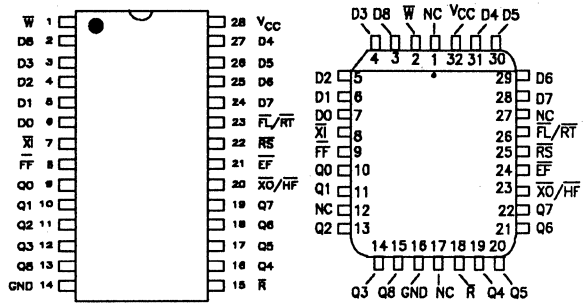
Dallas Semiconductor
512 x 9 FIFO

DS2009 28-Pin DIP
DS2009R 32-Pin PLCC

FEATURES

- First-in, first-out memory based architecture
- Flexible 512 x 9 organization
- Low power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35ns, 50ns, 65ns, and 80ns access times
- Industrial temperature range -40°C to +85°C available designated N

PIN CONNECTIONS



28-PIN DIP 32-PIN PLCC

PIN NAMES

$\overline{W}$	-WRITE
$\overline{R}$	-READ
$\overline{RS}$	-RESET
$\overline{FL/RT}$	-First Load/Retransmit
D_{0-8}	-Data In
Q_{0-8}	-Data Out
$\overline{XI}$	-Expansion In
$\overline{XO/HF}$	-Expansion Out/Half Full
$\overline{FF}$	-Full Flag
$\overline{EF}$	-Empty Flag
V_{CC}	-5 Volts
GND	-Ground
NC	-No Connect

DESCRIPTION

The DS2009 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The DS2009 is functionally and electrically equivalent to the DS2011 2K x 9 FIFO with the following exceptions: active current (I_{CC1}) is 80 mA max except for 35ns and industrial grade devices which is 100 mA max and power-down current (I_{CC3}) is 500 uA max. Refer to the DS2011 data sheet for detailed device description.

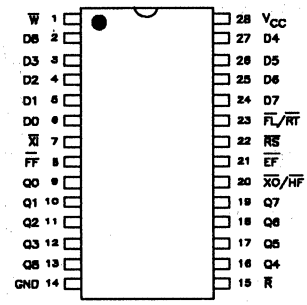
Dallas Semiconductor
1024 x 9 FIFO

DS2010 28-Pin DIP
DS2010R 32-Pin PLCC

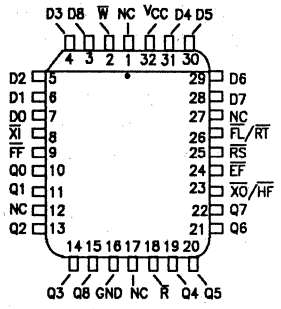
FEATURES

- First-in, first-out memory based architecture
- Flexible 1024 x 9 organization
- Low power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 35ns, 50ns, 65ns, and 80ns access times
- Industrial temperature range -40°C to +85°C available designated N

PIN CONNECTIONS



28-PIN DIP



32-PIN PLCC

PIN NAMES

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL}/\overline{RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO}/\overline{HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2010 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The DS2010 is functionally and electrically equivalent to the DS2011 2K x 9 FIFO with the following exception: power-down current (I_{CC3}) is 1 mA max. Refer to the DS2011 data sheet for detailed device description.

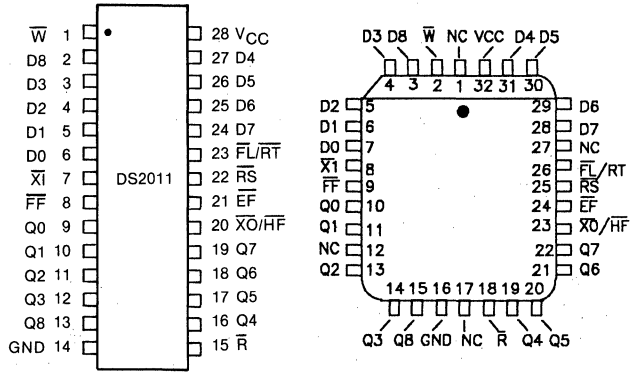
Dallas Semiconductor
2048 x 9 FIFO

DS2011 28-Pin DIP
DS2011R 32-Pin PLCC

FEATURES

- First-in, first-out memory based architecture
- Flexible 2048 x 9 organization
- Low power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35ns, 50ns, 65ns and 80ns access times
- Industrial temperature range −40°C to +85°C available designated IND

PIN CONNECTIONS



PIN NAMES

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL}/\overline{RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO}/\overline{HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2011 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The main application of the DS2011 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the WRITEs and READs are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

OPERATION

Unlike conventional shift register based FIFOs, the DS2011 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the DS2011 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

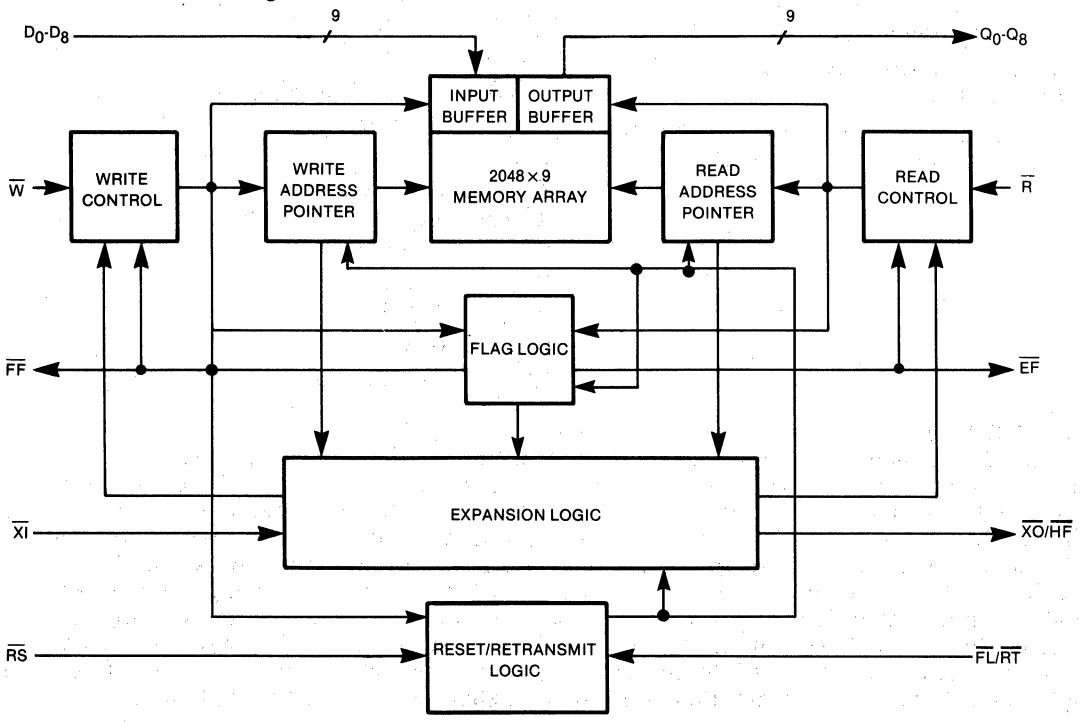
Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 2047. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2011 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2011 allows connecting the read, write, data in, and data out lines of the DS2011 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins, as appropriate (see the Expansion Timing section for a more complete discussion).

BLOCK DIAGRAM Figure 1



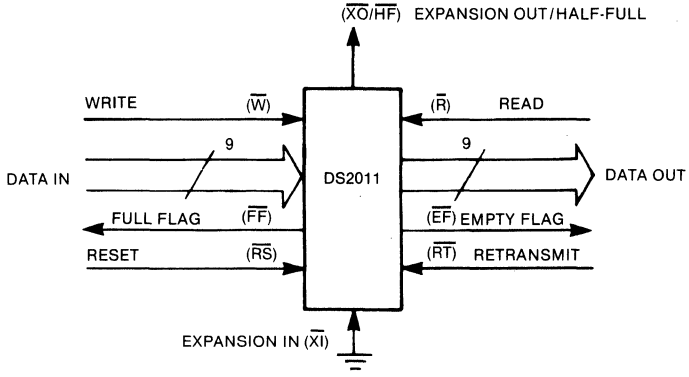
SINGLE DEVICE CONFIGURATION

A single DS2011 may be used when application requirements are for 2048 words or less. The DS2011 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 2).

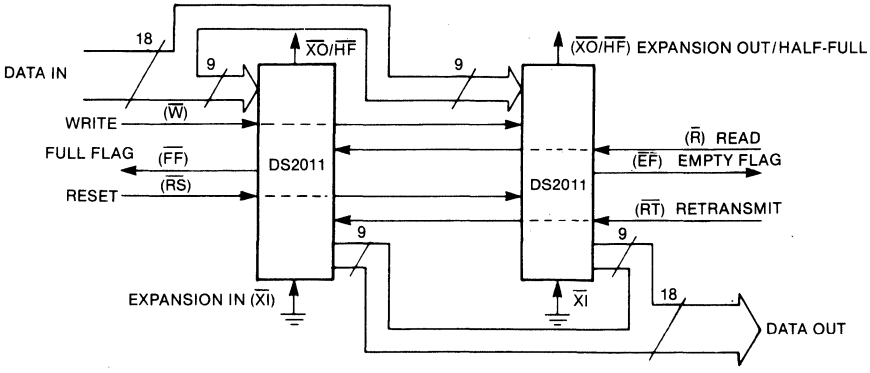
WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 3 demonstrates an 18-bit word width by using two DS2011s. Any word width can be attained by adding additional DS2011s.

A SINGLE 2048 x 9 FIFO CONFIGURATION Figure 2



A 2048 x 18 FIFO CONFIGURATION (WIDTH EXPANSION) Figure 3



NOTE:

Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

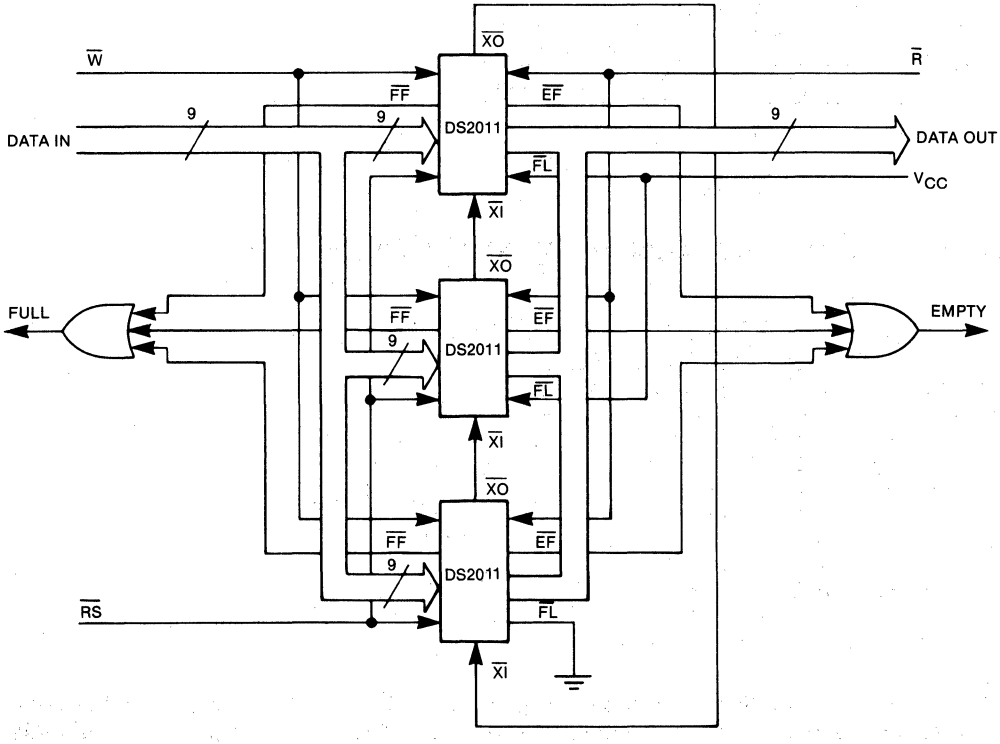
The DS2011 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 4 demonstrates Depth Expansion using three DS2011s. Any depth can be attained by adding additional DS2011s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The DS2011 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The half-full capability is not allowed in depth expansion.

A 6144 x 9 FIFO CONFIGURATION (DEPTH EXPANSION) Figure 4



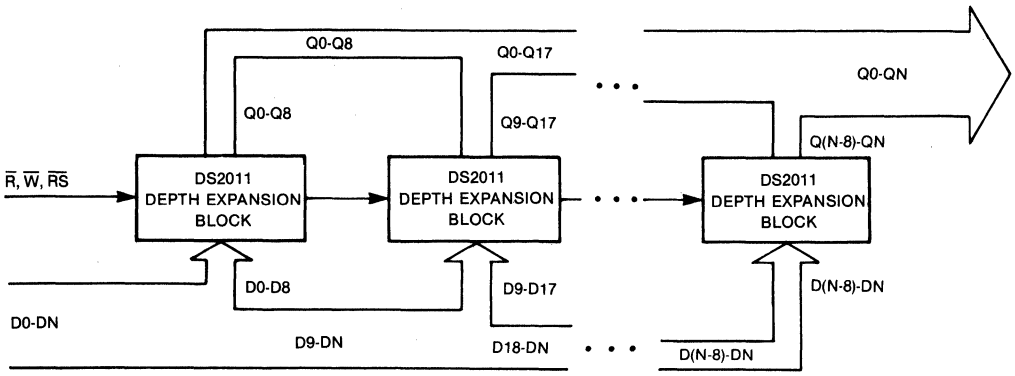
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing DS2011s, as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

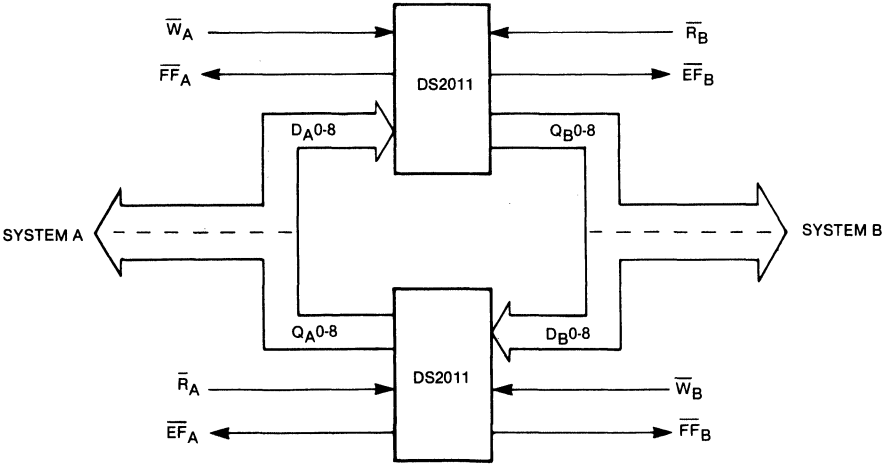
COMPOUND FIFO EXPANSION Figure 5



NOTES:

1. For depth expansion block see DEPTH EXPANSION section and Figure 4.
2. For flag operation see WIDTH EXPANSION section and Figure 3.

BIDIRECTIONAL FIFO APPLICATION Figure 6



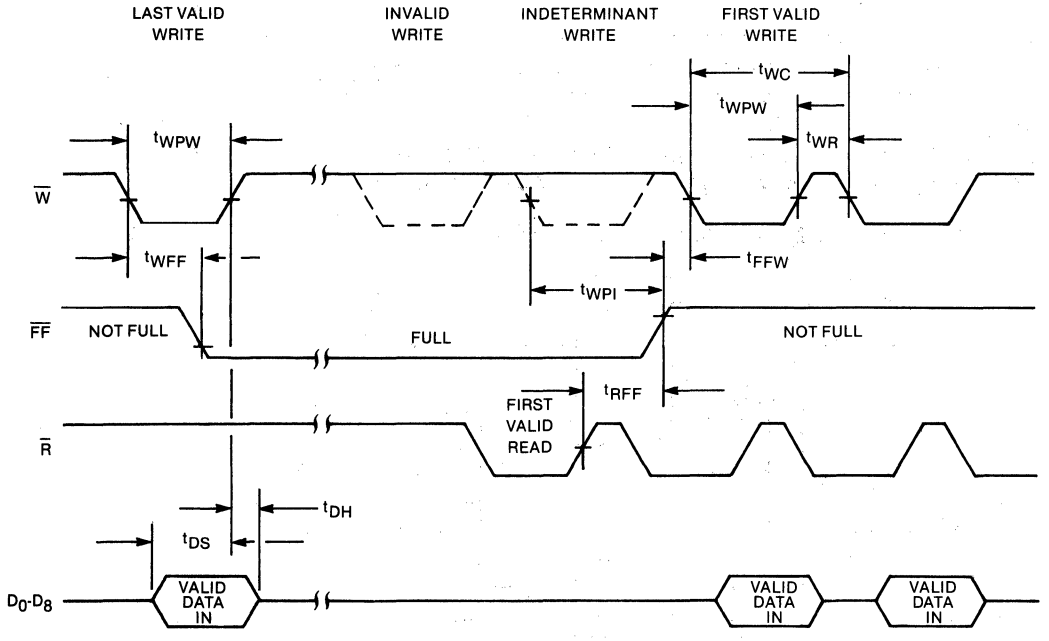
HALF-FULL CAPABILITY

In the single-device and width-expansion modes, the $\overline{XO}/\overline{HF}$ output acts as an indication of a half-full memory. ($\overline{XI}$ must be tied low.) After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain low until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset (forced high) by the rising edge of the read operation.

WRITE MODE

The DS2011 initiates a Write Cycle (see Figure 7) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the DS2011 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

WRITE AND FULL FLAG TIMING Figure 7



WRITE A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

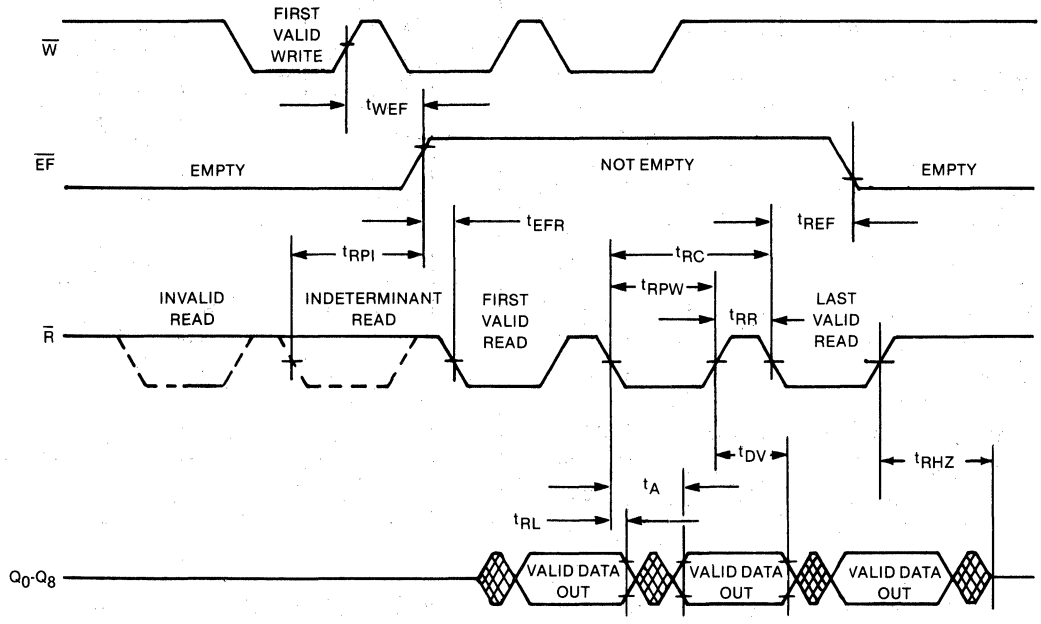
		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write Cycle Time	t_{WC}	45		65		80		100		ns	
Write Pulse Width	t_{WPW}	35		50		65		80		ns	1
Write Recovery Time	t_{WR}	10		15		15		20		ns	
Data Set Up Time	t_{DS}	15		20		25		30		ns	
Data Hold Time	t_{DH}	5		5		10		10		ns	
$\overline{W}$ Low to $\overline{FF}$ Low	t_{WFF}		30		45		60		70	ns	2
$\overline{FF}$ High to Valid Write	t_{FFW}		5		5		10		10	ns	2
$\overline{R}$ High to $\overline{FF}$ High	t_{RFF}		30		45		60		70	ns	2
Write Protect Indeterminant	t_{WPI}		15		20		25		25	ns	2

READ MODE

The DS2011 initiates a Read Cycle (see Figure 8) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the DS2011 provides a fast access to data from 9 of 18,432 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

READ AND EMPTY FLAG TIMING Figure 8



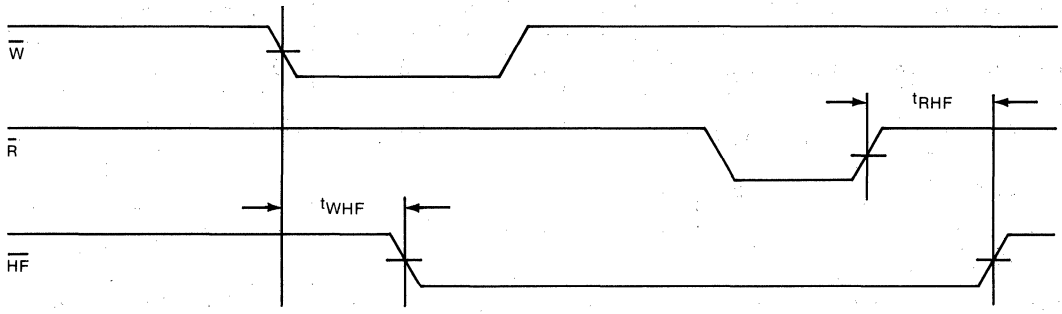
READ A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	45		65		80		100		ns	
Access Time	t_A		35		50		65		80	ns	2
Read Recovery Time	t_{RR}	10		15		15		20		ns	
Read Pulse Width	t_{RPW}	35		50		65		80		ns	1
$\overline{R}$ Low to Low Z	t_{RL}	5		10		10		10		ns	2
Data Valid from $\overline{R}$ High	t_{DV}	5		5		5		5		ns	2
$\overline{R}$ High to High Z	t_{RHZ}		20		25		25		25	ns	2
$\overline{R}$ Low to $\overline{EF}$ Low	t_{REF}		30		45		60		70	ns	2
$\overline{EF}$ High to Valid Read	t_{EFR}		5		5		10		10	ns	2
$\overline{W}$ High to $\overline{EF}$ High	t_{WEF}		30		45		60		70	ns	2
Read Protect Indeterminant	t_{RPI}		15		20		25		25	ns	2

HALF-FULL MODE

Unlike the Full Flag and Empty Flag, the Half-Full Flag does not prevent device reads and writes. The flag is set by the next falling edge of write when the memory is 1024 locations full. The flag will remain set until the memory is less than or equal to 1024 locations full. The read operation (rising edge), which results in the memory being 1024 locations full, removes the flag.

HALF-FULL FLAG TIMING Figure 9



HALF-FULL FLAG A.C. CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

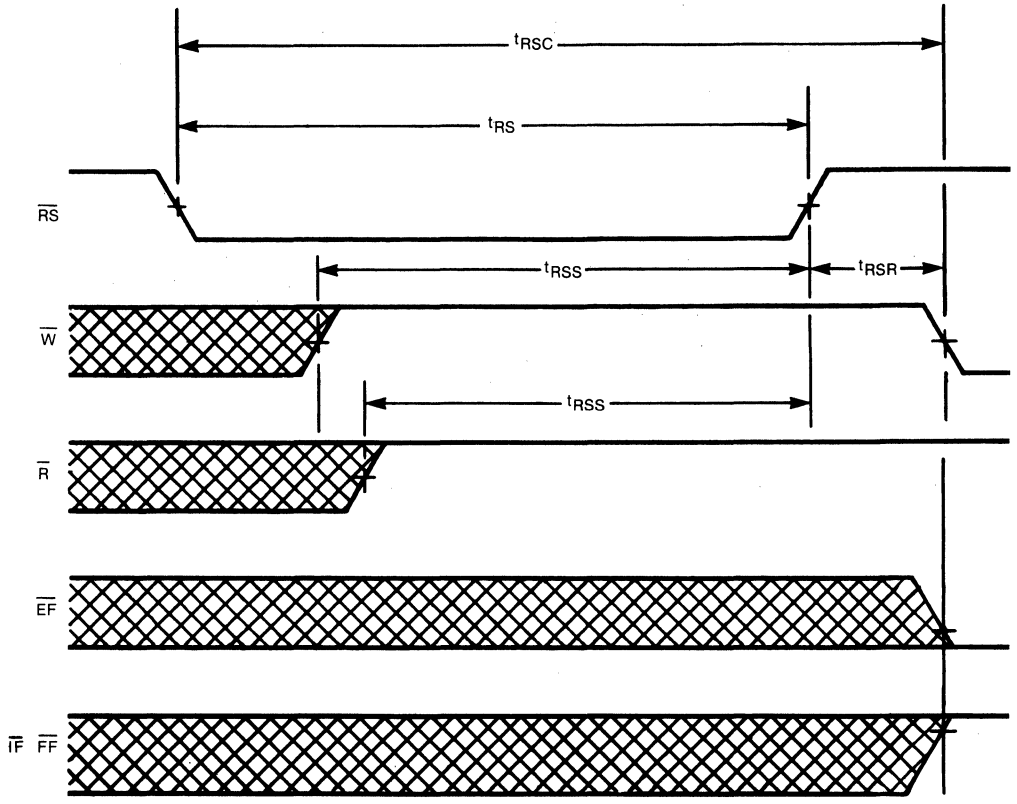
		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write Low to Half-Full Flag Low	t_{WHF}		45		65		80		100	ns	
Read High to Half-Full Flag High	t_{RHF}		45		65		80		100	ns	

RESET

The DS2011 is reset (see Figure 10) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after a power up, before a Write operation can begin.

Although neither $\overline{W}$ nor $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

RESET Figure 10



NOTE:

$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.

RESET A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Reset Cycle Time	t_{RSC}	45		65		80		100		ns	
Reset Pulse Width	t_{RS}	35		50		65		80		ns	1
Reset Recovery Time	t_{RSR}	10		15		15		20		ns	
Reset Set Up Time	t_{RSS}	30		40		50		60		ns	

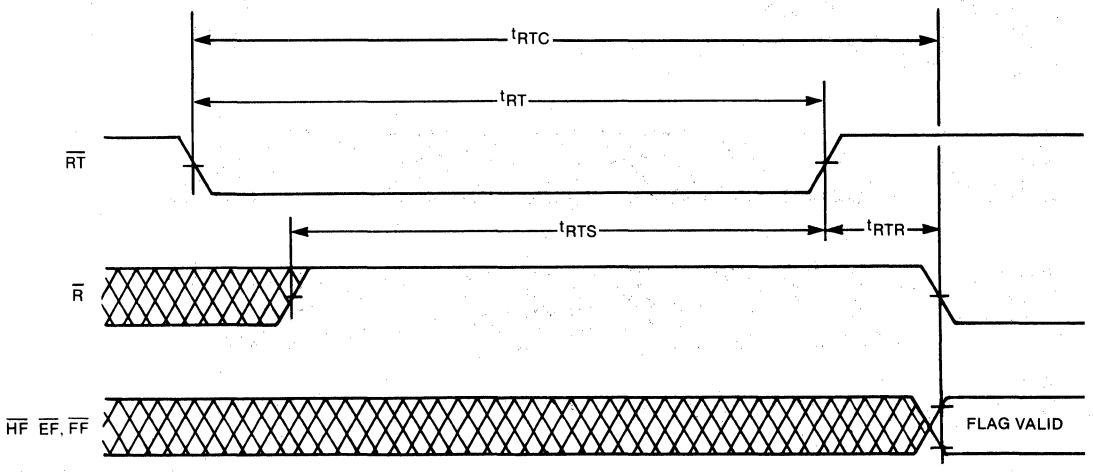
RETRANSMIT

The DS2011 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 11).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

RETRANSMIT Figure 11



NOTE:

$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

RETRANSMIT
A.C. ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC} = 5.0V ± 10%)

		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Retransmit Cycle Time	t_{RTC}	45		65		80		100		ns	
Retransmit Pulse Width	t_{RT}	35		50		65		80		ns	1
Retransmit Recovery Time	t_{RTR}	10		15		15		20		ns	
Retransmit Set Up Time	t_{RTS}	30		40		50		60		ns	

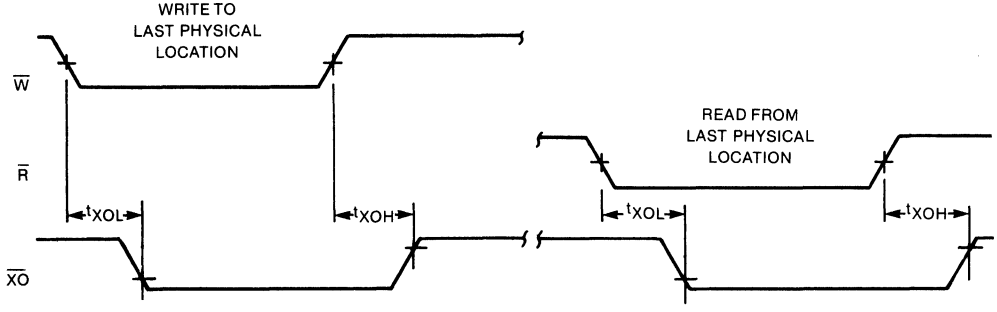
EXPANSION TIMING

Figures 12 and 13 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

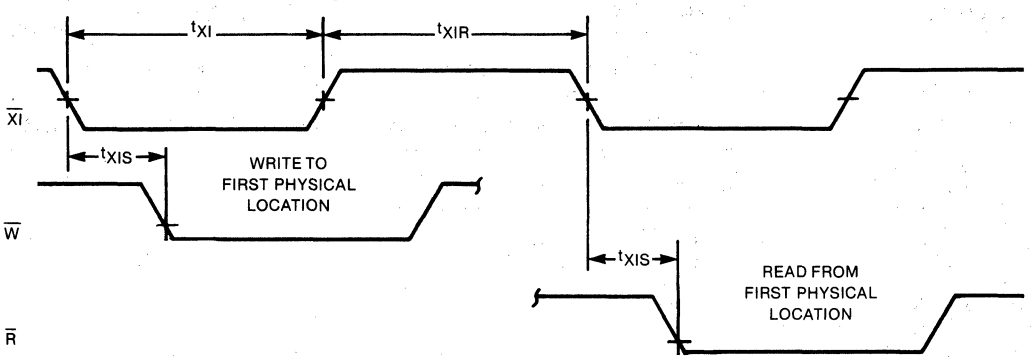
Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

When in Depth Expansion mode, a given DS2011 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A DS2011 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

EXPANSION OUT TIMING Figure 12



EXPANSION IN TIMING Figure 13



EXPANSION LOGIC
A.C. ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC} = 5.0V ± 10%)

		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Out Low	t_{XOL}		30		45		55		70	ns	
Expansion Out High	t_{XOH}		30		45		55		70	ns	
Expansion In Pulse Width	t_{XI}	35		50		65		80		ns	1
Expansion In Recovery Time	t_{XIR}	10		15		15		20		ns	
Expansion In Set Up Time	t_{XIS}	15		20		25		30		ns	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin relative to Ground -0.5V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Total Device Power Dissipation 1 Watt
Output Current per Pin 20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Ground	GND		0		V	
Logic "1" Voltage All Inputs	V_{IH}	2.0		$V_{CC}+0.3$	V	3
Logic "0" Voltage	V_{IL}	−0.3		+0.8	V	3,4

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C) (V_{CC} = 5.0 volts ± 10%)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current (Any Input)	I_{IL}	−1	1	uA	5
Output Leakage Current	I_{OL}	—10	10	uA	6
Output Logic "1" Voltage I_{OUT} = −1 mA	V_{OH}	2.4		V	3
Output Logic "0" Voltage I_{OUT} = 4 mA	V_{OL}		0.4	V	3
Average V_{CC} Power Supply Current	I_{CC1}		120	mA	7
Average Standby Current ($\overline{R} = \overline{W} = \overline{RST} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{CC2}		8	mA	7
Power Down Current (All Inputs = V_{CC} − 0.2V)	I_{CC3}		2	mA	7

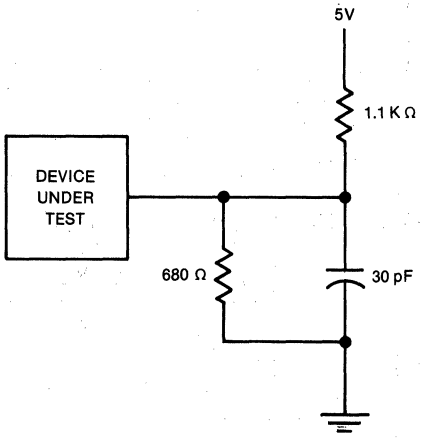
CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I	7	pF	
Capacitance on Output Pins	C_O	12	pF	8

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to Ground.
4. – 1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.

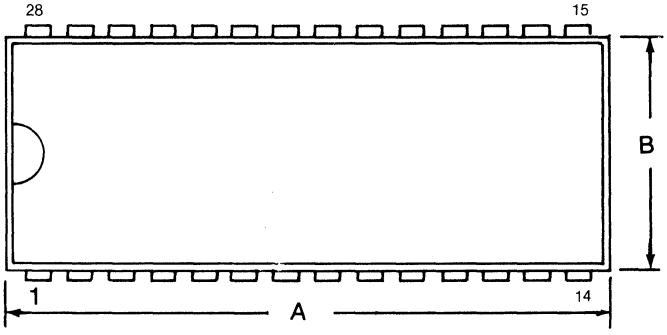
OUTPUT LOAD Figure 14



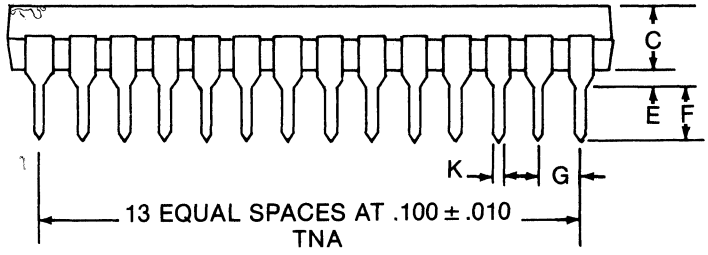
A.C. TEST CONDITIONS:

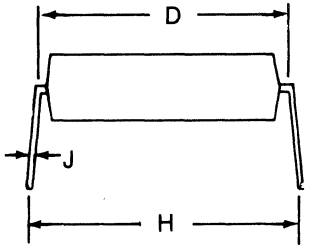
Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Level	0.8 V and 2.2 V
Ambient Temperature	0 °C to 70 °C
V_{CC}	5.0 V ± 10%

DS2011
2K x 9 FIFO
28-Pin DIP



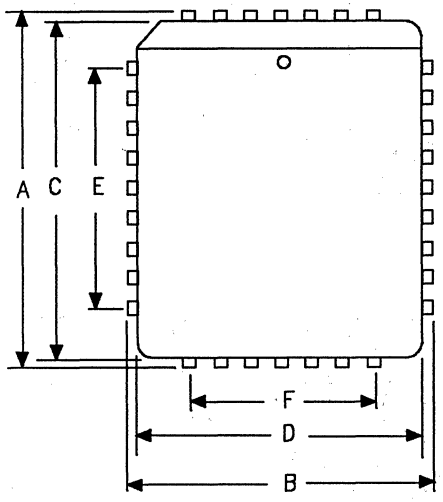
DIM.	INCHES	
	MIN.	MAX.
A	1.440	1.480
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.620	.670
J	.008	.012
K	.015	.021

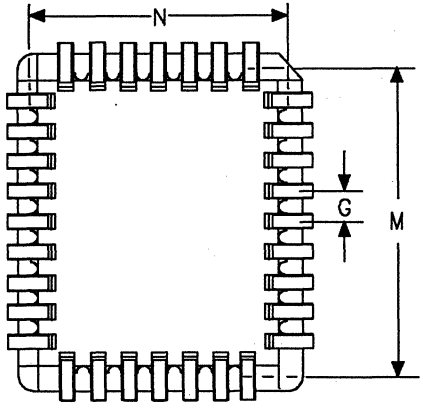


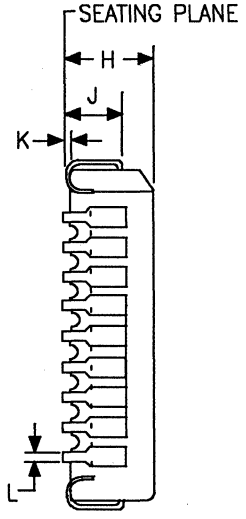


DS2011R
2K x 9 FIFO
32-Pin PLCC

DIM.	INCHES	
	MIN.	MAX.
A	.587	.593
B	.487	.493
C	.545	.555
D	.445	.455
E	.390	.410
F	.290	.310
G	.045	.055
H	.100	.140
J	.060	.095
K	.015	
L	.013	.021
M	.490	.530
N	.390	.430







Dallas Semiconductor
4096 x 9 FIFO

PRELIMINARY
DS2012 28-Pin DIP
DS2012R 32-Pin PLCC

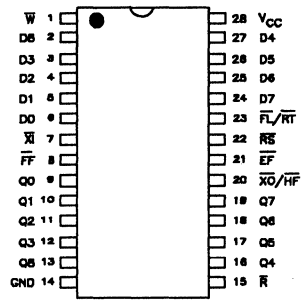
FEATURES

- First-in, first-out memory based architecture
- Flexible 4096 x 9 organization
- Low power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, and 80 ns access times
- Industrial temperature range -40°C to +85°C available designated N

DESCRIPTION

The DS2012 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, and empty flags, and unlimited expansion capability in both word size and depth. The main application of the DS2012 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a First-In, First-Out

PIN CONNECTIONS



28-PIN DIP 32-PIN PLCC

PIN NAMES

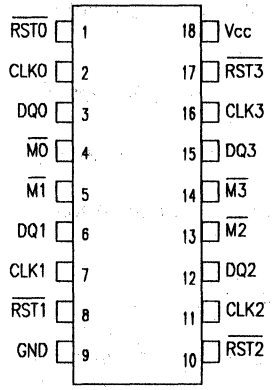
$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL/RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO/HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

(FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the WRITEs and READs are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-densinty devices. The ninth bit is provided to support control or parity functions. Refer to DS2011 data sheet for detailed device description.

FEATURES

- Four partitioned easy access ports
- No arbitration required
- Message flag for each port
- Low pin count serial access
- Simultaneous multiport reads
- Message length of up to eight bytes
- Low power CMOS
- Space saving 18 pin DIP
- Directly interfaces to the DS1206 Phantom interface
- Provides a low cost interconnect for up to four microprocessor based systems

PIN CONNECTIONS



PIN NAMES

$\overline{RST0}$-$\overline{RST3}$	Port 0 - Port 3 Reset
D/Q0-D/Q3	Port 0 - Port 3 Data I/O
CLK0-CLK3	Port 0 - Port 3 Clock
$\overline{M0}$-$\overline{M3}$	Port 0 - Port 3 Message Ready
GND	Ground
Vcc	+5 Volts

DESCRIPTION

The DS2015 Quad Port Serial RAM is a low cost device which can be used to loosely couple up to four microprocessors or microcontrollers. Arbitration is handled by protocol and a message center which forces discipline and prevents collisions. Each port has access to all other ports for reading information and can write information only in its own memory area. The memory space for each port is 64 bits. Access to and from each port takes place over a three wire serial bus. The serial bus keeps pin count low while affording sufficient bandwidth to accommodate loosely coupled system communication. Each port also has a message flag which can be used to warn of message ready conditions.

OPERATION

The DS2015 has four separate three wire serial ports. Each port has direct read and write access to eight message bytes of RAM which are designated as belonging to that particular port. In addition, each port has read only access to three groups of eight message bytes each which are designated as belonging to the three other ports. Messages are sent between any port by reading and writing the eight message bytes of the four ports. An optional check byte is provided for each group of eight message bytes to verify data integrity (see Figure 1). All of the cells within the RAM matrix are quad-ported and can be read simultaneously from four different directions. This reduces arbitration to concerns of write operations only.

Each of the four three wire serial ports contains a three byte protocol register which defines access to the RAM, and sets the discipline which controls arbitration between the four ports.

Protocol Register

The first byte of the protocol register is called the port select (see Figure 2). This byte contains an eight bit pattern which must match the first 8 bits sent on an active port or any further activity will be ignored (Figure 3). A port is active when the reset line is inactive (high) and the CLK input is transitioning. The first eight bits are sent into a port on the D/Q line. The second byte of the protocol register contains eight bits of status information about activity on all four ports. This byte, called the message center, is read only and divided into two nibbles; messages sent and mailbox. The first four bits tell which messages the port has sent to other ports that have not been received. By reading these four bits, the inquiring port knows not to send new messages because all the receiving ports have not read to a previously sent message. Each message sent bit is cleared when the receiving port reads the last bit of its message or the $\overline{RST}$ input of the receiving port is driven low. The next four bits of the message center provide each port with the knowledge of pending messages which are ready for reading and the number of the port or ports which are sending the message(s). These bits are set by the destination bits of each port when a sending port finishes writing the last bit of a message. The mailboxes are read only bits. All message center bits are driven out on the DQ line while $\overline{RST}$ is inactive and the clock is transitioning. The third byte of the protocol register contains the execution code. The execution code byte is also divided into two four bit nibbles; the action code and the destination. This byte is write only and data is input on the D/Q line with $\overline{RST}$ inactive and the CLK input transitioning. The action code bits have only three patterns which will allow subsequent action to take place (Figure 3). An action code of four zeros (0000) calls for a read message action to occur in one of the four sections of the Quad Port RAM as specified by the destination bits. A read message can occur to only one port and, therefore, only one destination bit can be set for an action code of 0000. Once a destination bit is set, a complete message of eight bytes must be read in order to reset the message sent bit in the sending port's protocol register. An action code of a one and three zeros (1000) calls for a write message action to be performed. A write message can only be written in the section of the Quad Port RAM that is identified with the sending port. However, a message which is written by a sending port can be directed to one or more ports by the destination bits. The destination bits will cause the mailbox bits in the protocol register of each port which is to receive the message to be set to logic one as soon as the last bit of the message is written by the sending port. An action code of two ones and two zeros (1100) calls for a write message action to be performed with more

FIGURE 1: QUAD PORT BLOCK DIAGRAM

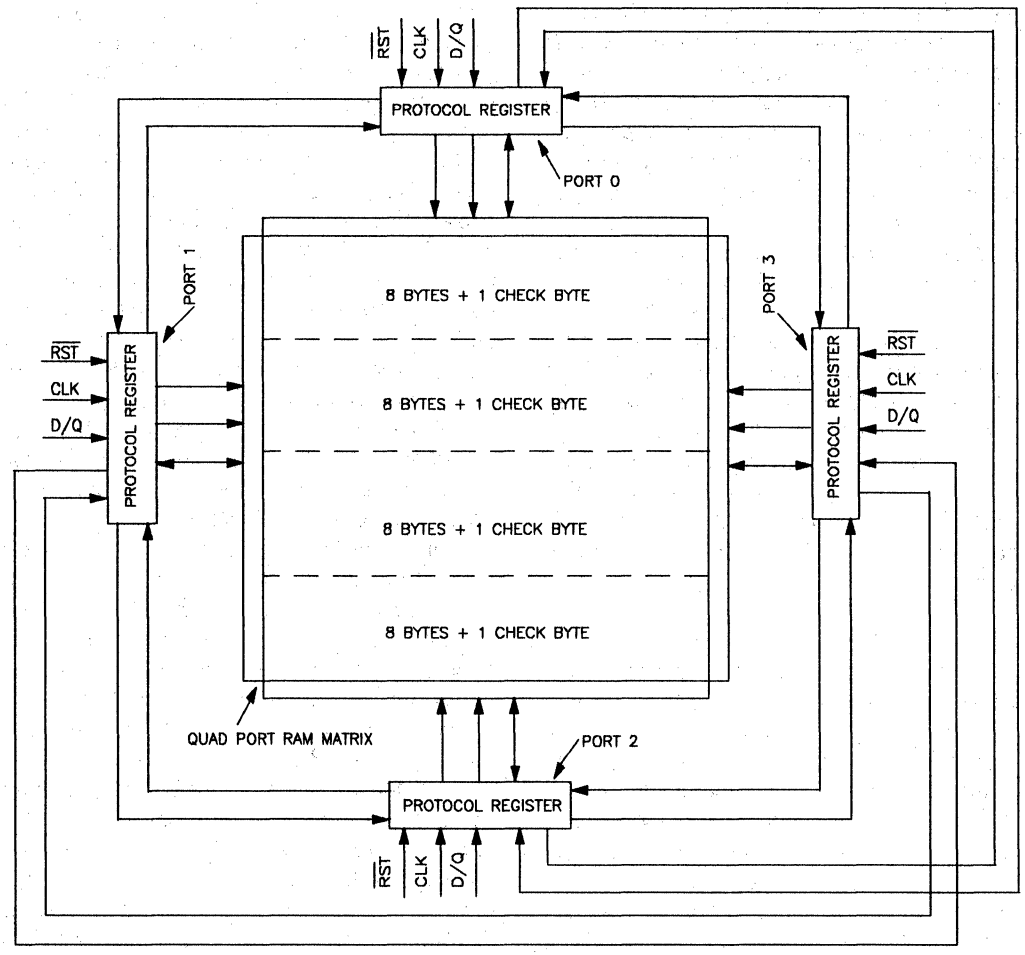
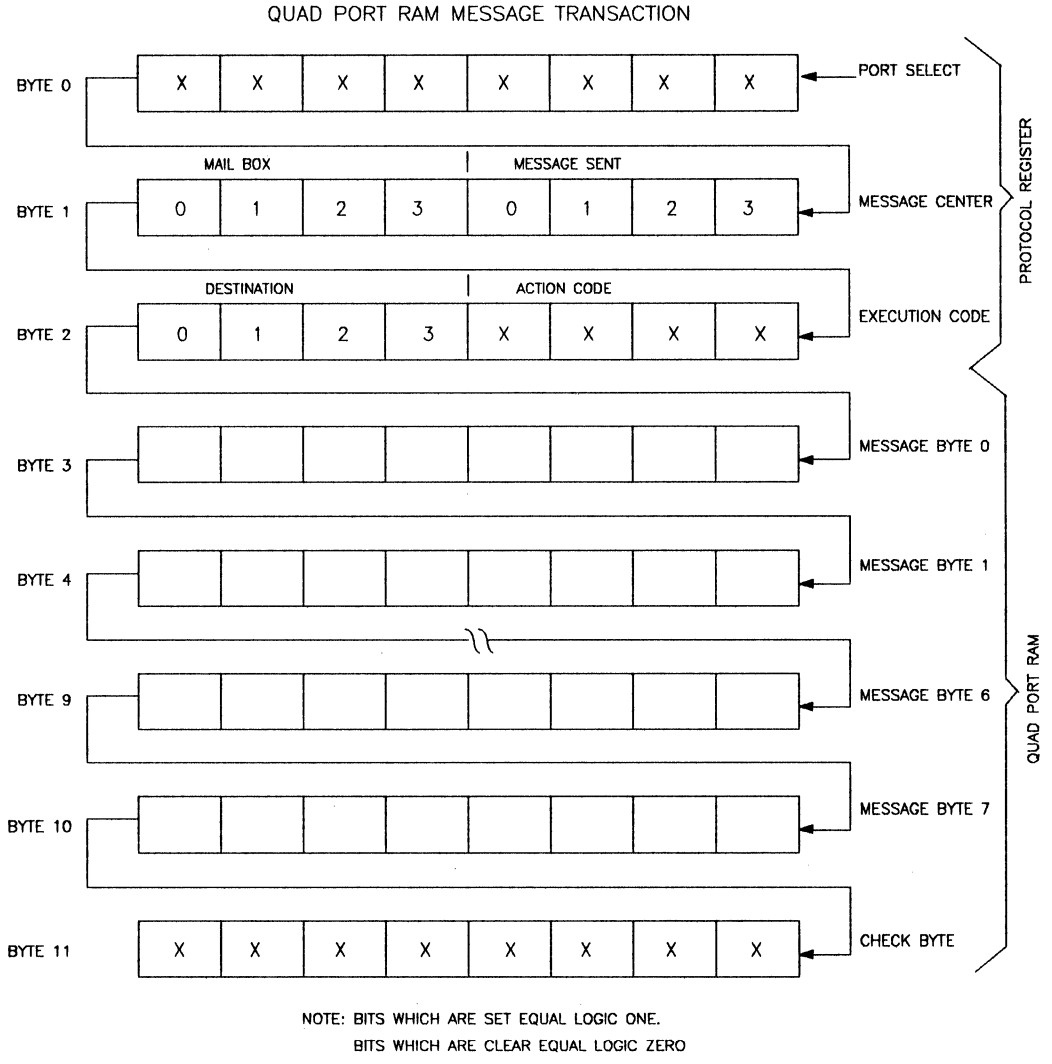
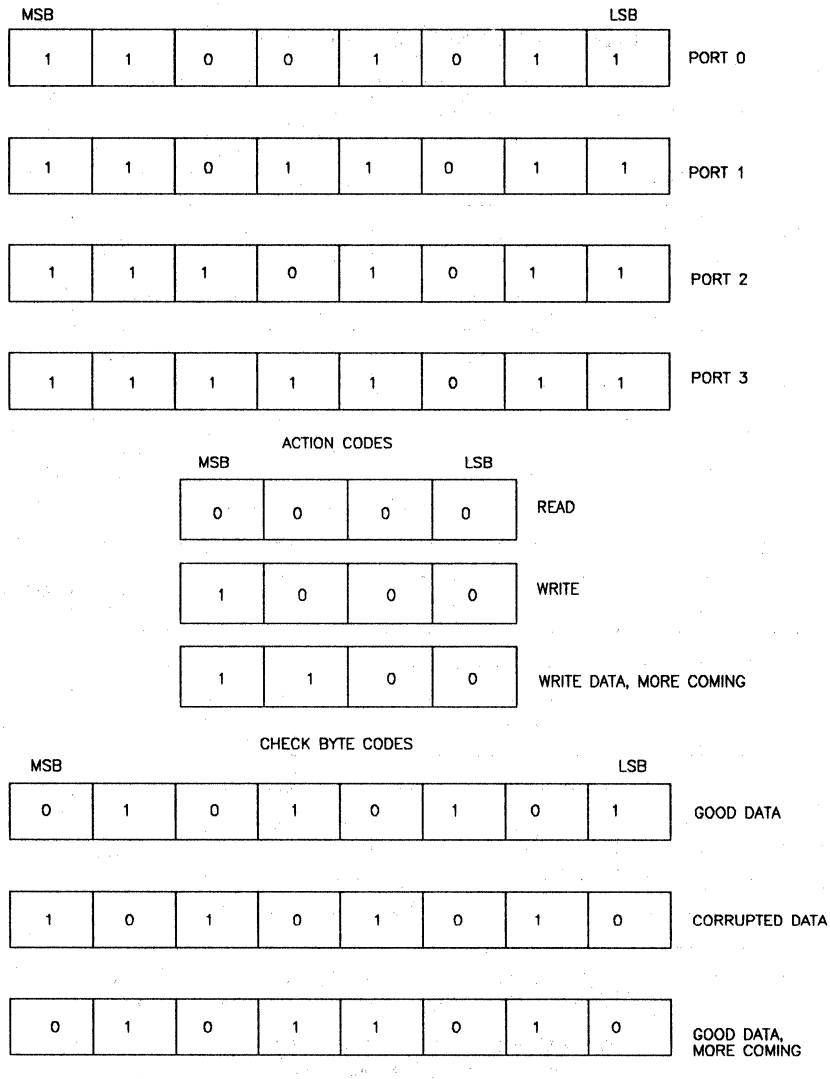


FIGURE 2: QUAD PORT RAM MESSAGE TRANSACTION



NOTE: BITS WHICH ARE SET EQUAL LOGIC ONE.
BITS WHICH ARE CLEAR EQUAL LOGIC ZERO

FIGURE 3: PORT SELECT CODE



data coming. This action code works exactly the same as a standard write message action with one exception. The check byte which follows an eight byte message is driven to a special code which, when read by a receiving port, indicates that more messages will be coming. This information can be used by a receiving port to reduce the overhead of constantly polling for new messages.

Quad Port RAM

As mentioned, each port has direct read and write access to eight message bytes and read access to three groups of eight message bytes. Once the protocol register has been correctly accessed, one of the four sections of the Quad Port will be read or that section of the Quad Port RAM which is dedicated to the transmitting port will be written. When sending a message, all eight message bytes must be written. When receiving a message, all eight of the message bytes should be read. If fewer than all eight bytes are accessed, the message centers may be incorrect and errant communications between ports can result.

Check Byte

A check byte (byte 11) is provided at the end of each of the eight message byte groups. The check byte is read only and provides information to a receiving port. Reading the check byte code is optional and may not be necessary in applications where software discipline is stringent enough to avoid accidental collisions between messages sent and messages received. Three different codes give status to a receiving port about the message which has just been read (Figure 3): good data, corrupted data, and good data with more data coming. When the check byte is read with a good data code, the data which is read by a receiving port is correct and valid. This check byte code assures the receiving port that a sending port is not writing a new message while the receiving port is attempting to read the previous message. When the check byte is read with a corrupted data code, the data which is read by a receiving port is suspect. This check byte warns the receiving port that the sending port is writing a new message while the receiving port is reading an older message. When the check byte is read with a good data and more coming code, the data which is read by a receiving port is correct and valid and additional messages will follow. This check byte code can be used by a receiving port to reduce the overhead of constant polling. If the check byte indicates that a new message will follow, the receiving port is warned to expect a new message.

Polling vs. Message Flags

The DS2015 Quad Port RAM has two methods of warning the sending and receiving ports of impending message status. The software method of polling avoids the complication of additional hardware which is required to connect the message ready pins to a host sending/receiving unit. Polling is accomplished with a receiving unit by satisfying the port select byte of the protocol register and reading the message center. When a port is being polled, care should be taken to avoid entering the execution code portion of the protocol register. When polling a port, communications can be terminated by taking the $\overline{RST}$ input signal low. An alternate method of alerting a host sending/receiving unit of impending message status is to use the message ready signals to interrupt when a message is ready to be read. The message ready pins ($\overline{M0}$-$\overline{M3}$) are driven to an active state (low) when a sending port has written the last bit of the eight message bytes and $\overline{RST}$ of the sending port is set to the inactive state (low),

provided the appropriate destination bit is set. When the message ready pin is set to an active state, a receiving unit can execute a software routine to service the interrupt and read the pending message.

$\overline{RST}$ Control

All message transactions are initiated by driving the $\overline{RST}$ port input high. The $\overline{RST}$ input serves two functions. First, it turns on control logic which allows access to the protocol register. Second, the $\overline{RST}$ signal provides a method of terminating message transfer. Care must be taken when terminating a message transfer to avoid errant information in the message center. The following rules will avoid all problems.

1. While polling the message center for new messages, always terminate the transaction by driving $\overline{RST}$ low after completing a read of the message center byte and before entering the execution code byte.

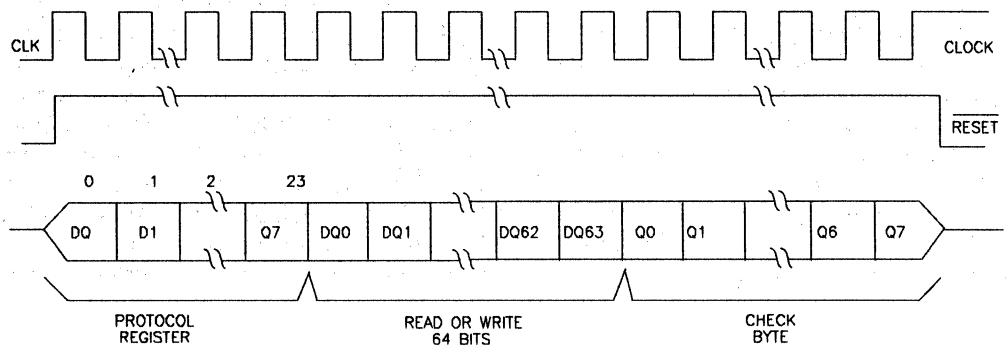
2. When sending a message, all eight messsage bytes must be written. If fewer than eight bytes are written, the mailbox bit of the destination port(s) may not be set and the check byte may indicate corrupted data.

3. When receiving a message, all eight bytes should be read. However, if $\overline{RESET}$ is used to terminate a message which is being read, the message sent bit and the mailbox bit are cleared as $\overline{RST}$ is driven low. When reading a message, the check byte is optional and can be either read or ignored.

Clock Control

A clock cycle is a sequence of a falling edge followed by a rising edge. For message inputs, the data must be valid during the rising edge of the clock cycle. Protocol bits and message bits are input on the rising edge of the clock. Protocol bits and message bits are output on the falling edge of the clock. All message transfer terminates if $\overline{RST}$ is low and the D/Q pins will then go to a high impedance state. When message transfer is terminated using $\overline{RST}$, the transition of $\overline{RST}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Figure 4 illustrates message transfer.

FIGURE 4: QUAD PORT MESSAGE TRANSFER



ABSOLUTE MAXIMUM RATINGS*

Voltage on a pin to ground: -1.0 to + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Logic 1	V_{IH}	2.0		Vcc+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	Vcc	4.5	5.0	5.5	V	1

D.C ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5V+/- 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	*u*A	
Output Leakage	I_{LO}			1	*u*A	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
Supply Current	I_{CC}			6	mA	2

CAPACITANCE

(T_A=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_N	5	pF	
Output Capacitance	C_{OUT}	7	pF	

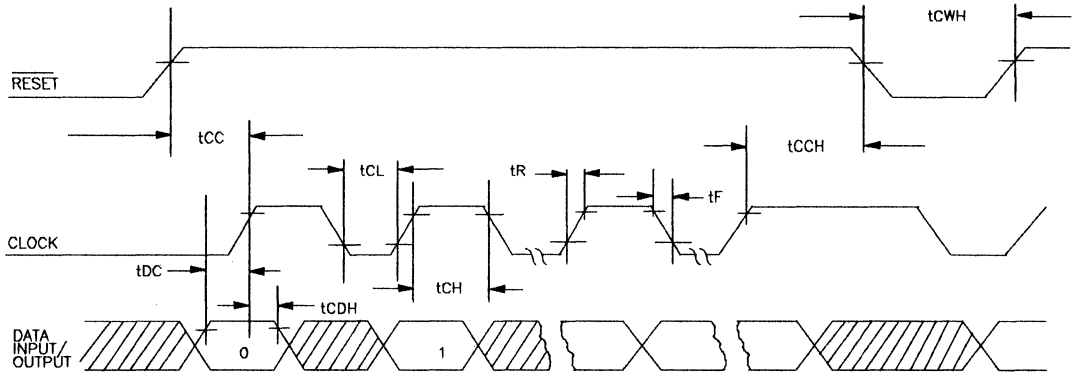
A.C ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5V+/- 10%)

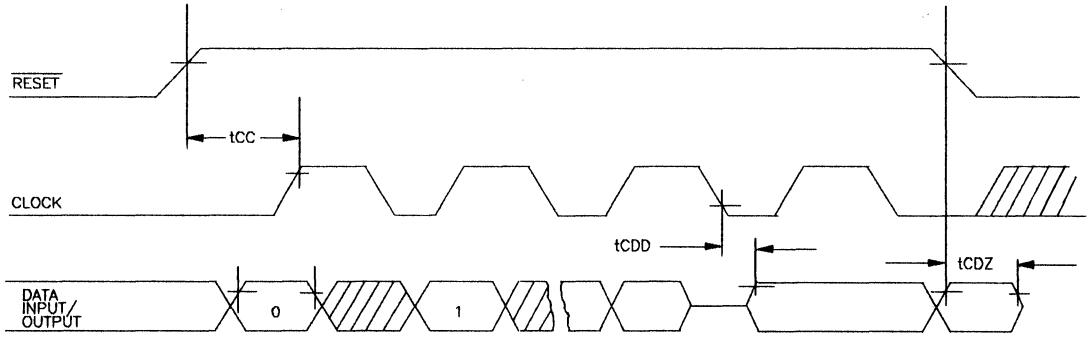
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	
CLK to Data Hold	t_{CDH}	40			ns	
CLK to Data Delay	t_{CDD}			125	ns	
CLK Low Time	t_{CL}	125			ns	
CLK High Time	t_{CH}	125			ns	
CLK Frequency	f_{CLK}	D.C		4.0	MHZ	
CLK Rise and Fall	t_R,t_F			500	ns	
$\overline{\text{RST}}$ to CLK Set Up	t_{CC}	1			us	
CLK to $\overline{\text{RST}}$ Hold	t_{CCH}	40			ns	
$\overline{\text{RST}}$ Inactive Time	t_{CWH}	125			ns	
$\overline{\text{RST}}$ to I/O High Z	t_{CDZ}			50	ns	
$\overline{\text{RST}}$ to Message Ready	t_{RF}			100	ns	

QUAD SERIAL PORT RAM TIMING DIAGRAM

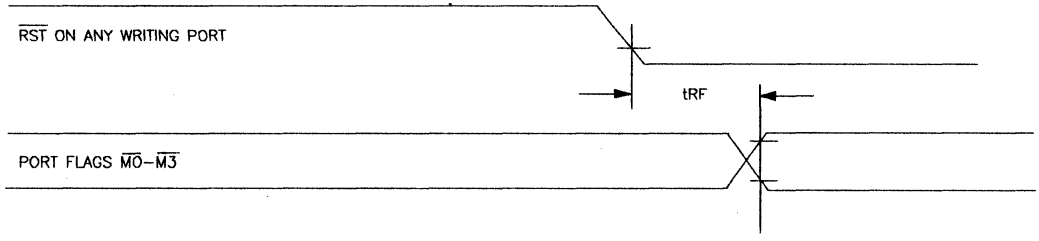
TIMING DIAGRAM-WRITE DATA TRANSFER



TIMING DIAGRAM-READ DATA TRANSFER



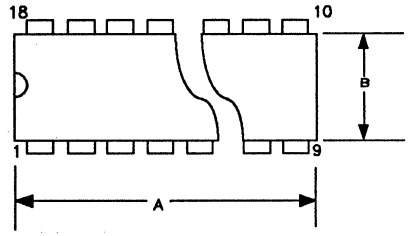
TIMING DIAGRAM~MESSAGE READY



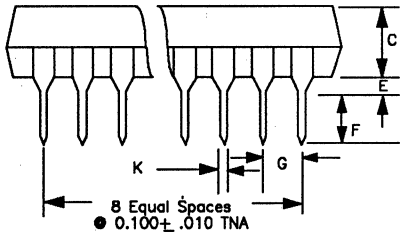
Notes

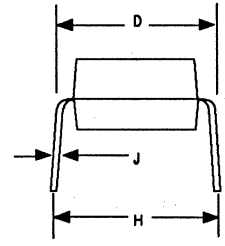
1. All voltages are referenced to ground.
2. All outputs are open.

DS2015
Quad Port Serial RAM
18 Pin DIP



DIM.	INCHES	
	MIN.	MAX.
A	0.860	0.940
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	.320	.370
J	0.008	0.012
K	0.015	0.021

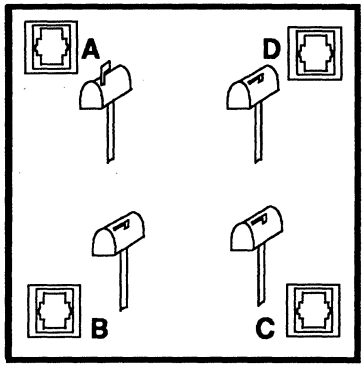




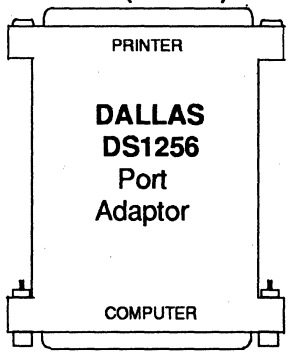
FEATURES

- Low cost P.C. network
- Links up to four personal computers
- Inexpensive four conductor jacketed telephone cable for connection
- No external power source
- Simultaneous communication with auto arbitration
- Simple user installation
- P.C. separation up to 100 feet
- Modular expansion
- Rugged and durable
- Interfaces via parallel printer port of an IBM XT, AT, PS/2 or compatible PC without using up expansion slots or ports
- Normal computer/printer operation is unaffected

FOUR WAY JUNCTION (DS9030)



PORT ADAPTOR (DS1256)



DESCRIPTION

P.C. InterLink is a low cost network designed to link up to four personal computers. The network consists of a Port Adaptor for each computer, a Four Way Junction and software to activate computer communications. As supplied by Dallas Semiconductor the DS9050 consists of two Port Adaptors, one Four Way Junction, and software. Additional DS1256 Port Adaptors can be ordered separately for a third and fourth computer. Interface to the personal computer is established via the parallel printer port by connecting the Port Adaptor. This adaptor connection is external to the computer cabinet and does not affect either the computer or printer operation. Connection from the Port Adaptors to the Four Way Junction is made with standard four wire telephone cable terminated with modular plugs (six position type). Having completed hardware connections between computers, software is loaded and communication is established.

HARDWARE INSTALLATION

Hardware installation begins with connecton of a Port Adaptor (D.S.C. part number DS1256) to the printer port of each personal computer in the network. If a printer cable is connected to the computer printer port, remove it by loosening both retaining screws and unplugging the cable. Next, install the Port Adaptor by plugging the male side of the adaptor into the female printer port. Note that the Port Adaptor is marked to indicate both computer side and printer side to help avoid incorrect installation. Tighten both retaining screws to prevent accidental disconnection. If a printer is to be used, plug the printer cable into the Port Adaptor. Again, tighten both retaining screws. This procedure must be repeated for each P.C. to be used in the P.C. InterLink system (up to four).

Once the Port Adaptors (DS1256) are installed, they must be connected to the Four Way Junction (DS9030). Standard six position 4-wire jacketed phone cable terminated with 6-position modular plugs at each end are used to connect the Four Way Junction at any physical location between computers. The total length of wire between any two computers must be limited to 100 feet (see Figure 2). Connection to the Four Way Junction is made by inserting the modular plug at one end of the wire into the modular jack on the DS1256 Port Adaptor. The modular plug at the other end of the wire can then be inserted into any of the four modular jacks marked A through D residing within the Four Way Junction. Note that any PC may be connected to any port of the Four Way Junction, and will automatically assume the correct identification upon network activation. The user may procure any of several standard lengths of telephone cable as appropriate for the desired network layout. Again, the total length of wire between any two computers must not exceed 100 feet.

At this point hardware installation is complete, as operation of the P.C. InterLink is transparent to the user and requires no external power. An internal lithium energy source supplies power to a quad port memory (D.S.C. part number DS2015) within the Four Way Junction. If a technical description of the Quad Port Memory is desired, the DS2015 data sheet should be studied.

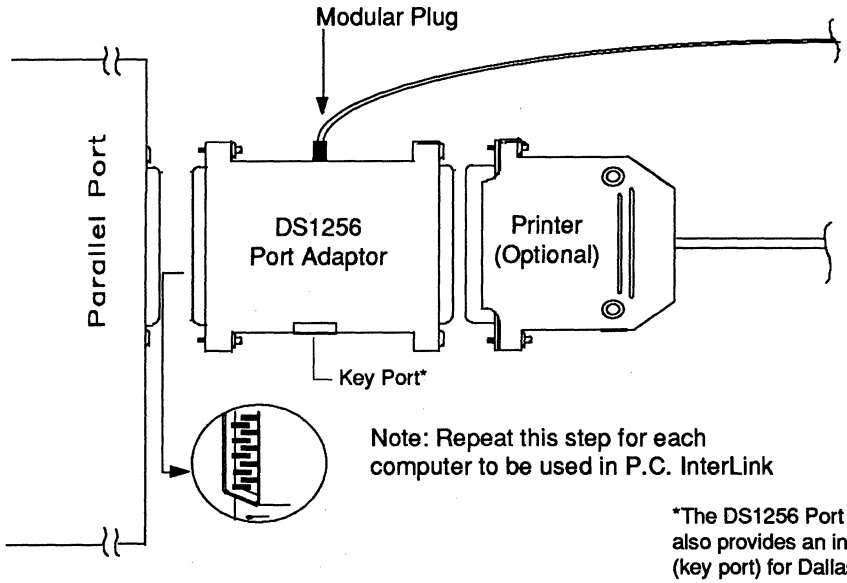
SOFTWARE INSTALLATION

Software for P.C. InterLink is supplied on a standard D9 floppy diskette and a 3 1/4" QD15 diskette marked *DS9050 Utilities.* These diskettes contains both an instruction manual depicting proper installation procedures and a program to activate operation of the P.C. InterLink. The instruction manual may be retrieved by inserting the diskette into the default drive and typing TYPE DS9050.MEM. The print command may also be used for a paper copy. The manual should be read completely before system start up, then followed carefully during network activation.

Upon completion of network activation, personal computers can transfer information within the link under keyboard control.

INSTALLATION DIAGRAM Figure 1

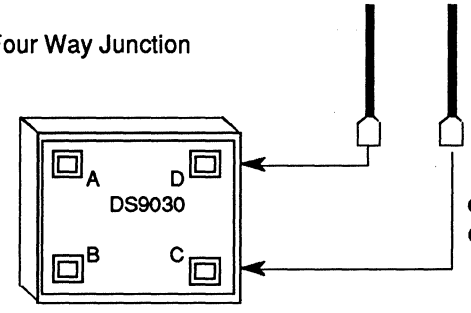
1. Install the Port Adapter and connect cables



Note: Repeat this step for each computer to be used in P.C. InterLink

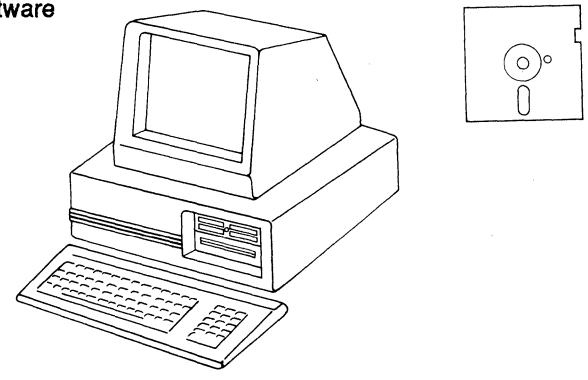
*The DS1256 Port Adaptor also provides an interface (key port) for Dallas Semiconductor Electronic Keys. These devices are used by some software companies for copy protection.

2. Connect the Four Way Junction

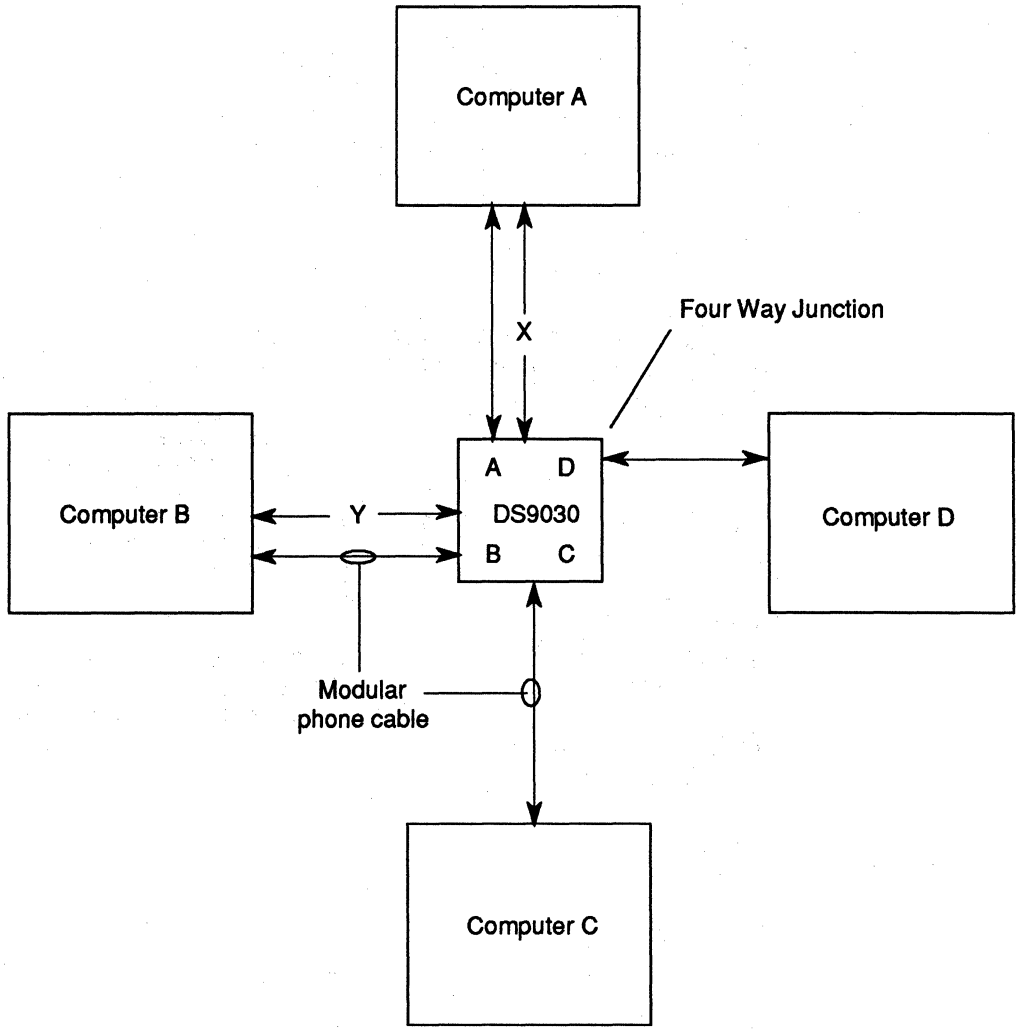


Note: 2, 3, or 4 connections depending on the number of computers in P.C. InterLink

3. Install software



DS9050 INTERCONNECTION DIAGRAM Figure 2



X + Y must not exceed 100 feet

Microcontroller

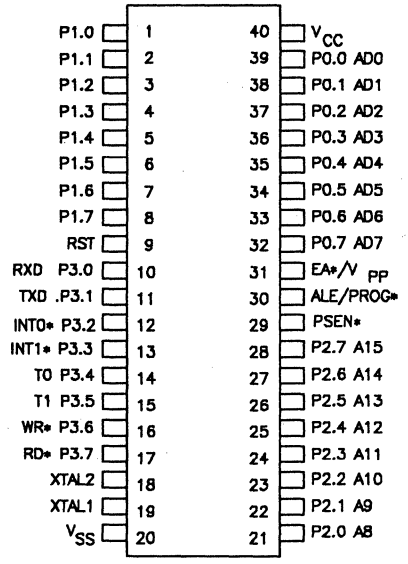
Dallas Semiconductor
Soft Microcontroller

PRELIMINARY
DS5000

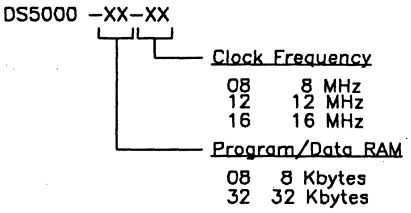
FEATURES

- 8-bit uC adapts to task-at-hand:
  - 8 or 32 Kbytes of high performance nonvolatile RAM for Program and/or RAM for Program and/or Data Memory storage
  - Initial downloading of software in end system via on-chip serial port
  - Capable of modifying its own Program and/or Data Memory in end use
  - 128 internal nonvolatile registers for variable retention
- Crashproof operation:
  - Maintains all nonvolatile resources for 10 years in the absence of V_{CC}
  - Orchestrates orderly shutdown and automatic restart on power up/down
  - Automatic restart on detection of errant software execution
- Software Security Feature:
  - Executes encrypted software to prevent unauthorized disclosure
- On-chip full duplex serial I/O port
- Two on-chip timer/event counters
- 32 parallel I/O lines
- Compatible with industry standard 8051 instruction set and pinout

PIN CONNECTIONS



ORDERING INFORMATION



DESCRIPTION

The DS5000 is a high performance 8-bit CMOS microcontroller that offers "softness" in all aspects of its application. This is accomplished through the comprehensive use of nonvolatile technology to preserve all information in the absence of system V_{CC}. The entire Program/Data Memory space is implemented using high speed, nonvolatile

static CMOS RAM. Two memory size versions are available which offer either 8 Kbytes or 32 Kbytes of NVRAM for Program/Data storage. Furthermore, internal data registers and key configuration registers are also nonvolatile.

A major benefit resulting from its nonvolatility is that the Soft Microcontroller allows Program Memory to be changed at any time, even after the device has been installed in the end system. Additionally, the size of the Program and Data Memory areas in the embedded RAM is variable and can be set either when the application software is initially loaded or by the software itself during execution.

Initial loading of the application software into the DS5000 is possible from either a parallel or serial interface to a host system. This function allows initialization of the nonvolatile areas of the device including Program/Data RAM and the configuration parameters. Serial loading uses the on-chip serial I/O port to accept incoming data from a host computer with an RS232 port, such as a PC-based development system. Not only is it possible to initially boot via the serial port in the end system but any subsequent software reloading can be made at will during system operation without the need for removal of the device.

The softness also provides the ultimate in adaptive system design by allowing either the Data RAM or the Data Registers to retain information in the absence of V_{CC}. As a result, a virtually unlimited number of variables and/or data tables can be updated and maintained over the life of the product, as opposed to their being lost during a power fluctuation. This capability allows software to be developed which updates variables and data tables to reflect the cumulative knowledge of the control system from the time that it was put into service. Consequently, control systems may be given the ability to learn from experience and react by altering processing steps in response to operating conditions which change over extended periods of time.

The DS5000 Soft Microcontroller incorporates control functions which provide crashproof operation when system power is momentarily disrupted, or removed entirely. These functions include the Power Fail Warning interrupt, Automatic Power Down, and Power On Restart. The Power Fail Warning interrupt provides an early warning of a potential power failure so that the operational state of the system may be stored prior to a complete removal of system V_{CC}. The Automatic Power Down feature causes all nonvolatile resources to be sustained at low current from the embedded lithium energy source while system power is removed. When V_{CC} voltage is applied once again, the processor is automatically restarted with an internal flag set indicating that a Power On sequence has just been performed. Regardless of whether the power merely fluctuates or is absent for years, upon its return the Soft Microcontroller has the ability to resume execution when power is reapplied as if the power failure had not occurred at all.

The Soft Microcontroller's tolerance of power cycling provides an alternative for battery-powered hand-held systems which typically drain their batteries during periods of idle time, when processing is not being performed. On/off power cycling can be employed to cause such systems to consume battery power only during processing to ensure a dramatic reduction of the overall power dissipation.

The DS5000 also provides extensive software security with its unique on-chip software encryption logic. This feature prevents un-

authorized individuals from reading and disassembling Program/Data RAM. When activated, the device loads and executes the software in an encrypted form, rendering the contents of the RAM and the execution of the program unintelligible to the outside observer. The encryption algorithm uses an internally stored and protected 40-bit key which is programmed by the user. Any attempt to discover the key value results in its erasure, rendering the contents of the Program/Data RAM useless. In this manner, the investment represented by the resident software is protected from piracy.

The DS5000 incorporates these unique functions in a device which is instruction set and pin compatible with the industry standard 8051 microcontroller architecture. Development work for new designs based on the DS5000 may be performed utilizing existing development tools and software packages which support the 8051 architecture.

The DS5000 also provides a full complement of I/O functions including two 16-bit event counter/timers, a full duplex serial I/O port capable of asynchronous or synchronous operation, 32 parallel I/O lines, and a watchdog timer. If additional external memory is desired beyond the embedded Program/Data RAM, 18 parallel I/O lines may be assigned to serve the Expanded Bus function.

PIN DESCRIPTION

NOTE: All inverted signal names are denoted with a asterisk (*) as a suffix to the signal name (e.g. INT0*). This convention is followed throughout this document.

V_{CC}, GND	Power Supply inputs.
P0.7-P0.0	Port 0: Bidirectional I/O; open drain These pins also serve the function of:
AD7-AD0	Address/Data Bus: Bidirectional
P1.7-P1.0	Port 1: Bidirectional I/O
P2.7-P2.0	Port 2: Bidirectional I/O These pins also serve the function of:
A15-A8 -	Address Bus: Outputs
P3.7-P3.0	Port 3: Bidirectional I/O Each of the pins on Port 3 may be selected to serve an alternate function; as described below:
RD* **(P3.7)**	Expanded Data Memory Read Strobe: Output; active low

WR* (P3.6)	Expanded Data Memory Write Strobe: Output; active low
T1,T0 (P3.5,P3.4)	Timer/Counter pins: Inputs; active high
INT1*, INT0* (P3.3,P3.2)	External interrupt pins: Inputs; active low
TXD (P3.1)	Transmit Data: Output
RXD (P3.0)	Receive Data: Input
RST	Reset: Input; active high
ALE (PROG*)	Address Latch Enable: Output; active high (or Program Byte Enable: Input; active low)
PSEN*	Program Store Enable: Output; active low
EA* (VPP)	External Access Enable: Input; active low (or VPP programming voltage input)
XTAL1, XTAL2	Crystal inputs

INSTRUCTION SET

The DS5000 executes an instruction set which is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages which have been written for the 8051 are compatible with the DS5000 including cross-assemblers, high-level language compilers, and debugging tools.

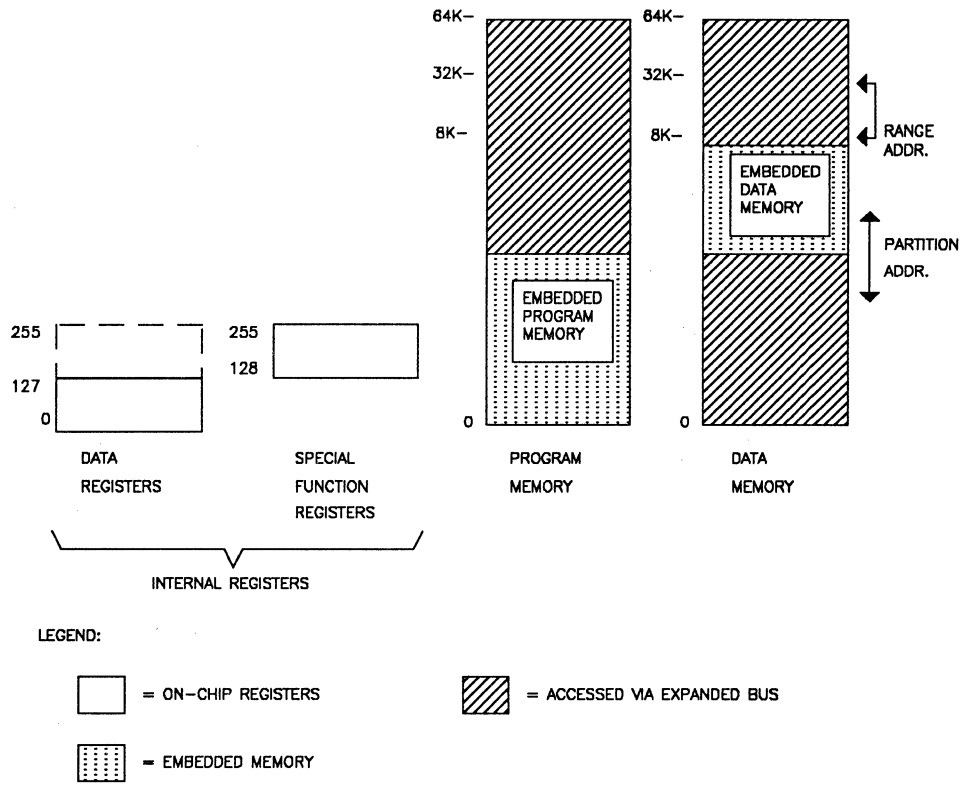
A complete description for the DS5000 instruction set is available in the DS5000 User's Guide (part # DS5000G).

MEMORY ORGANIZATION

Figure 1 illustrates the address spaces which are accessed by the DS5000. As illustrated in the figure, separate address spaces exist for Program and Data Memory. Since the basic addressing capability of the machine is 16-bits, a maximum of 64 Kbytes of Program Memory and 64 Kbytes of Data Memory can be accessed by the DS5000 CPU. The 8K or 32K byte embedded RAM area can be used to contain both Program and Data Memory.

The Internal Register space is divided into two parts: Data Registers and Special Function Registers. There are a total of 128 Data Registers including four 8-byte banks of working registers (R0-R7). The Special Function Registers include the CPU Registers as well as registers which provide control and status information for the Program and Data Memory mapping, non-volatile operation, and on-chip I/O functions.

DS5000 LOGICAL ADDRESS SPACES Figure 1



SPECIAL FUNCTION REGISTERS

There are a total of 23 Special Function Registers which have been implemented in the DS5000. Table 5-1 lists each of these along with their respective addresses, reset values, and functional descriptions.

DS5000 SPECIAL FUNCTION REGISTER MAP Table 1

New or Modified Register	Label	Direct Register Address	Reset Value	Bit address-able	Functional Description
	B	0F0H	00H	X	B Register
	A	0E0H	00H	X	Accumulator
	PSW	0D0H	00H	X	Program Status Word
X	TA	0C7H	055H		Timed Access
X	MCON	0C6H	RT		Memory Control
X	IP	0B8H	00H	X	Interrupt Priority Ctl.
	P3	0B0H	0FFH	X	Port 3 Parallel I/O
	IE	0A8H	00H	X	Interrupt Enable Ctl.
	P2	0A0H	0FFH	X	Port 2 Parallel I/O
	SBUF	099H	??		Serial Data Buffer
	SCON	098H	00H	X	Serial Control
	P1	090H	0FFH	X	Port 1 Parallel I/O
	TH1	08DH	00H		Timer 1 High Byte
	TH0	08CH	00H		Timer 0 High Byte
	TL1	08BH	00H		Timer 1 Low Byte
	TL0	08AH	00H		Timer 0 Low Byte
	TMOD	089H	00H		Timer Mode Select
	TCON	088H	00H	X	Timer Control
X	PCON	087H	RT		Power Control
	DPH	083H	00H		Data Pointer High Byte
	DPL	082H	00H		Data Pointer Low Byte
	SP	081H	07H		Stack Pointer
	P0	080H	0FFH	X	Port 0 Parallel I/O

NOTES:

?? indicates that the register value is indeterminate on reset.
RT indicates that the initialization performed on the register is dependent on the type of the reset.

The Power Control (PCON), Interrupt Priority (IP), Memory Control (MCON), and Timed Access (TA) registers represent modifications from the 8051 implementation, as denoted in the above table. The following is a detailed summary of these registers.

POWER CONTROL REGISTER

Label: PCON **Register Address: 087H**

D7	D6	D5	D4	D3	D2	D1	D0
SMOD	POR	PFW	WTR	EPFW	EWT	STOP	IDL

Bit Description:

PCON.7 SMOD
"Double Baud Rate" : When set to a 1, the baud rate is doubled when the serial port is being used in modes 1, 2, or 3.
Initialization: Cleared to a 0 on any reset.
Read Access: Can be read normally at any time.
Write Access: Can be written normally at any time.

PCON.6 POR*
"Power On Reset": Indicates that the previous reset was initiated during a Power On sequence.
Initialization: Cleared to a 0 when a Power On Reset occurs. Remains at 0 until it is set to a 1 by software.
Read Access: Can be read normally at any time.
Write Access: Can be written only by using the Timed Access Register.

PCON.5: PFW
"Power Fail Warning": Indicates that a potential power failure is in progress. Set to 1 whenever V_{CC} voltage is below the V_{PFW} threshold. Cleared to a 0 immediately following a read operation of the PCON register. Once set, it will remain set until the read operation occurs regardless of activity on V_{CC}.
Initialization: Cleared to a 0 during a Power On Reset.
Read Access: Can be read normally anytime.
Write Access: Not writeable.

PCON.4: WTR
"Watchdog Timer Reset" Set to a 1 when a reset was issued as a result of a Watchdog Timer timeout. Cleared to 0 immediately following a read of the PCON register

Initialization: Set to a 1 after a Watchdog Timeout Reset. Cleared to a 0 on a No-V_{LI} Power on Reset. Remains unchanged during other types of resets.

Read Access: May be read normally anytime.

Write Access: Cannot be written

PCON.3: EPFW
"Enable Power Fail Interrupt": Used to enable or disable the Power Fail interrupt. When EPFW is set to a 1 it will be enabled; it will be disabled when EPFW is cleared to a 0.

Initialization: Cleared to a 0 on any type of reset.

Read Access: Can be read normally anytime.

Write Access: Can be written normally anytime.

PCON.2: EWT
"Enable Watch-dog Timer" Used to enable or disable the Watchdog Timeout Reset. The Watch dog Timer is enabled if EWT is set to a 1 and will be disabled if EWT is cleared to a 0.

Initialization: Cleared to a 0 on a No-V_{LI} Power on Reset. Remains unchanged during other types of resets.

Read Access: May be read normally anytime.

Write Access: Can be written only by using the Timed Access register.

PCON.1: STOP
"Stop": Used to invoke the Stop Mode. When set to a 1 program execution will terminate immediately and Stop Mode operation will commence. Cleared to a 0 when program execution resumes following a hardware reset.

Initialization: Cleared to a 0 on any type of reset

Read Access: Can be read anytime.

Write Access: Can be written only by using the Timed Access register.

PCON.0: IDL
"Idle": Used to invoke the Idle Mode. When set to a 1 program execution will be halted and will resume when the Idle bit is cleared to 0 follow ing an interrupt or a hardware reset.

Initialization: Cleared to 0 on any type of reset or interrupt.

Read Access: Can be read normally anytime.

Write Access: Can be written normally anytime.

INTERRUPT PRIORITY REGISTER

Label: IP **Register Address: 0B8H**

D7	D6	D5	D4	D3	D2	D1	D0
RWT	–	–	PS	PT1	PX1	PT0	PX0

Bit Description:

IP.7: RWT "Reset Watch-Timer": When set to a 1 the Watchdog Timer count will be reset, and counting will begin again. The RWT bit will then automatically be cleared again to 0. Writing a 0 into this bit has no effect.
Initialization: Cleared to a 0 on any reset.
Read Access: Cannot be read.
Write Access: Can be written only by using the Timed Access register.

All of the following bits are read/write at any time and are cleared to 0 following any hardware reset.

IP.4: PS "Serial Port Priority": Programs Serial Port interrupts for high priority when set to 1. Low priority is selected when cleared to 0.

IP.3: PT1 "Timer 1 Priority": Programs Timer 1 interrupt for high priority when set to 1. Low priority is selected when cleared to 0.

IP.2: PX1 "Ext. Int. 1 Priority": Programs External Interrupt 1 for high priority when set to 1. Low priority is selected when cleared to 0.

IP.1: PT0 "Timer 0 Priority": Programs Timer 0 interrupt for high priority when set to 1. Low priority is selected when cleared to 0.

IP.0: PX0 "Ext. Int. 0 Priority": Programs External Interrupt 0 for high priority when set to 1. Low priority is selected when cleared to 0.

MEMORY CONTROL REGISTER

Label: MCON **Register Address: 0C6H**

D7	D6	D5	D4	D3	D2	D1	D0
PA3	PA2	PA1	PA0	RA32/8	ECE2	PAA	—

Bit Description:
MCON.7-4: PA3-0

"Partition Address": Used to select the starting address of Data Memory in Embedded RAM. Program space lies below the Partition Address.

Selection:

PA3	PA2	PA1	PA0	Partition Address
0	0	0	0	0000H
0	0	0	1	0800H
0	0	1	0	1000H
0	0	1	1	1800H
0	1	0	0	2000H
0	1	0	1	2800H
0	1	1	0	3000H
0	1	1	1	3800H
1	0	0	0	4000H
1	0	0	1	4800H
1	0	1	0	5000H
1	0	1	1	5800H
1	1	0	0	6000H
1	1	0	1	6800H
1	1	1	0	7000H *
1	1	1	1	8000H *

*** A 4 Kbyte increment (not 2 Kbytes) in the Partition Address takes place between bit field values 1110B and 1111B.**

Initialization: Set to all 1's on a No V_{LI} Power On Reset or when the Security Lock bit is cleared to a 0 from a previous 1 state. These bits are also set to all 1's when any attempt is made to have them cleared to all 0's with the SL bit set to a 1 (illegal condition).

Read Access: May be read anytime.
Write Access: PAA bit must = 1 in order to write PA3-0. Timed Access is not required to write to PA3-0 once PAA = 1.

MCON.3: RA32/8
"Range Address": Sets the maximum usable address in Embedded Memory.
RA32/8 = 0 sets Range Address = 1FFFH (8K)
RA32/8 = 1 sets Range Address = 7FFFH (32K)

Initialization: Set to a 1 during a No V_{LI} Power On Reset and when the Security Lock bit (SL) is cleared to a 0 from a previous 1 state. Remains unchanged on all other types of resets.
Read Access: May be read normally anytime.
Write Access: Cannot be modified by the application software; can only be written during Program Load Mode.

MCON.2: ECE2
"Enable Chip Enable 2": Used to enable or disable the CE2* signal to additional Embedded RAM Data Memory space. This bit should always be cleared to 0 in the DS5000 8 and DS5000 32 versions.
Initialization: Cleared to 0 only during a No V_{LI} Power On Reset.
Read Access: Read normally anytime.
Write Access: Can be written normally at any time.

MCON.1: PAA
"Partition Address Access": Used to protect the programming of the Partition Address select bits. PA3-0 cannot be written when PAA = 0. PAA can be written only via the Timed Access register.
Initialization: PAA is cleared only on a No-V_{LI} Power On Reset
Read Access: PAA may be read anytime.
Write Access: The Timed Access register must be used to perform any type of write operation on the PAA bit

TIMED ACCESS REGISTER

Label: TA **Register Address: 0C7H**

D7	D6	D5	D4	D3	D2	D1	D0

Bit Description:

TAn.n: (All Timed Access bits)

"Timed Access": Used to invoke a Timed Access procedure required to write to any of the Timed Access protected bits including EWT, RWT, STOP, PAA. Timed Access is activated by three sequential write operations as in the example shown below:

```
MOV   0C7H, 0AAH      ; Write 0AAH to TA register
MOV   0C7H, 055H      ; Write 055H to TA register
ORL   IP,#80H         ; Reset Watchdog Timer
```

Initialization: Written with the value of 055H following any type of reset.

Read Access: Cannot be read from the application software

PROGRAM LOAD MODES

The Program Load Modes allow initialization of the embedded Program/Data Memory and nonvolatile Internal Registers. This initialization may be performed in one of two ways:

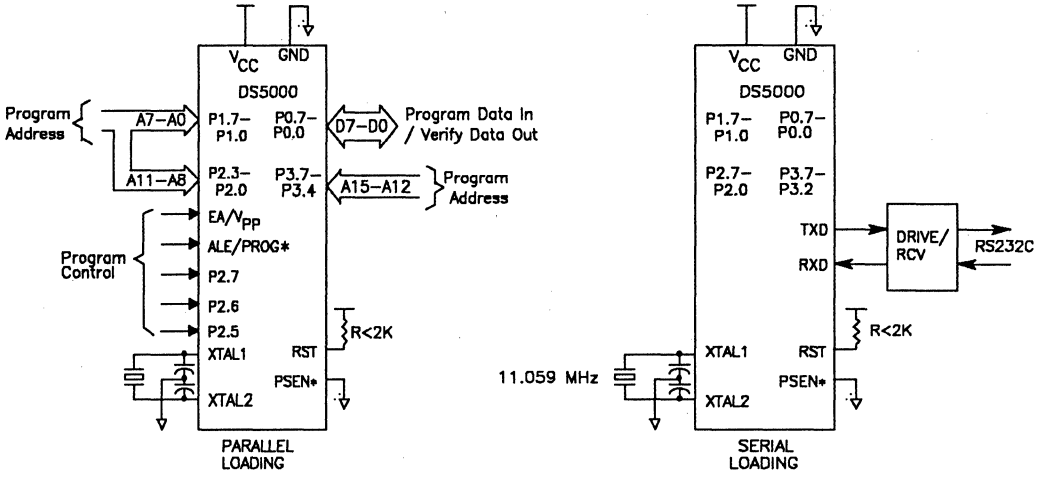
1) Parallel Program Load cycles which perform the initial loading from parallel address/data information presented on the I/O port pins. This mode is timing-set compatible with the 8751H microcontroller programming mode.

2) Serial Program Loading which is capable of performing bootstrap loading of the DS5000. This feature allows the loading of the application program to be delayed until the DS5000 is installed in the end system.

The DS5000 is placed in its Program Load configuration by simultaneously applying a logic 1 to the RST pin and forcing the PSEN* line to a logic 0 level. Immediately following this action, the DS5000 will look for a Parallel Program Load pulse, or a serial ASCII carriage return (0DH) character received at 9600, 2400, 1200, or 300 bps over the serial port.

The hardware configurations used to select these modes of operation are illustrated in Figure 2.

PROGRAM LOADING CONFIGURATIONS Figure 2



The table below summarizes the selection of the available Parallel Program Load cycles. Figure 5 illustrates the timing associated with these cycles.

PARALLEL PROGRAM LOAD CYCLES Table 2

Mode	RST	PSEN*	PROG*	EA*	P2.7	P2.6	P2.5
Program	1	0	0	VPP	1	0	X
Security Set	1	0	0	VPP	1	1	X
Verify	1	X	X	1	0	0	X
Prog Expanded	1	0	0	VPP	0	1	0
Verify Expanded	1	0	1	1	0	1	0
Prog MCON or key registers	1	0	0	VPP	0	1	1
Verify MCON reg	1	0	1	1	0	1	1

The Program Cycle is used to load a byte of data into a register or memory location within the DS5000. The Verify Cycle is used to read this byte back for comparison with the originally loaded value to verify proper loading. The Security Set Cycle may be used to enable and disable the Software Security feature of the DS5000. One may also enter bytes for the MCON register or for the 5 encryption registers using the Program MCON cycle. When using this cycle, the absolute register address must be presented at Ports 1 and 2 as in the normal Program cycle (Port 2 should be 00H). The MCON contents can likewise be verified using the Verify MCON cycle.

When the DS5000 first detects a Parallel Program Strobe pulse or a Security Set Strobe

pulse while in the Program Load Mode following a Power On Reset, the internal hardware of the DS5000 is initialized so that an existing 4 Kbyte program can be programmed into a DS5000 with little or no modification. This initialization automatically sets the Range Address for 8 Kbytes and maps the lowest 4 Kbyte bank of Embedded RAM as Program Memory. The next 4 Kbytes of Embedded RAM are mapped as Data Memory.

In order to program more than 4 Kbytes of program code, the Program/Verify Expanded cycles can be used. Up to 32 Kbytes of program code can be entered and verified. Note that the expanded 32Kbyte Program/Verify cycles take much longer than the normal 4 Kbyte Program/Verify cycles.

A typical parallel loading session would follow this procedure. First, set the contents of the MCON register with the correct range and partition only if using expanded programming cycles. Next, the encryption registers can be loaded to enable encryption of the program/data memory (not required). Then, program the DS5000 using either normal or expanded Program cycles and check the memory contents using Verify cycles. The last operation would be to turn on the security lock feature by either a Security Set cycle or by explicitly writing to the MCON register and setting MCON.0 to a 1.

SERIAL LOAD MODE

The Serial Program Load Mode is the easiest, fastest, most reliable, and most complete method of initially loading application software into the DS5000's nonvolatile RAM. Communication can be performed over a standard asynchronous serial communications port. A typical application would use a simple RS232C serial interface to program the DS5000 as a final production procedure. The hardware configuration which is required for the Serial Program Load Mode is illustrated in Figure 2. *Port pins 2.7 and 2.6 must be either open or pulled high to avoid placing the DS5000 in a parallel load cycle.* Although an 11.0592 MHz crystal is shown in Figure 2, a variety of crystal frequencies and loader baud rates are supported which are shown in Table 3. The serial loader is designed to operate across a three wire interface from a standard UART. The receive, transmit and ground wires are all that are necessary to establish communication with the DS5000.

The Serial Loader implements an easy-to-use command line interface which allows an application program in an Intel Hex representation to be loaded into and read back from the device. Intel Hex is the typical format which existing 8051 cross-assemblers output. The serial loader responds to 11 single character commands which are summarized below:

COMMAND	FUNCTION
C	Return CRC-16 checksum of embedded RAM
D	Dump Intel Hex File
F	Fill Embedded RAM block with constant
K	Load 40-bit Encryption Key
L	Load Intel Hex File
R	Read MCON register
T	Trace (Echo) incoming Intel Hex data
U	Clear Security Lock
V	Verify Embedded RAM with incoming Intel Hex
W	Write MCON register
Z	Set Security Lock

SERIAL LOADER BAUD RATES FOR DIFFERENT CRYSTAL FREQUENCIES*

Table 3

Crystal freq (MHz)	Baud Rate				
	300	1200	2400	4800	9600
16.000000		Y	Y		
15.000000		Y	Y	Y	Y
14.318180		Y	Y	Y	Y
12.000000		Y	Y	Y	
11.059200	Y	Y	Y	Y	Y
11.000000	Y	Y	Y	Y	Y
10.000000		Y	Y	Y	
9.216000	Y	Y	Y	Y	Y
8.000000		Y			
7.372800	Y	Y	Y	Y	Y
6.144000	Y	Y	Y		
6.000000	Y	Y	Y		
5.990400	Y	Y	Y		
5.120000	Y	Y	Y		
5.068800	Y	Y	Y		
5.000000	Y	Y	Y		
4.915200	Y	Y	Y		
4.608000	Y	Y	Y	Y	
4.433620	Y	Y	Y	Y	
4.194300	Y				
4.096000	Y				
4.032000	Y				
3.579545	Y	Y	Y	Y	Y
2.457600	Y	Y			
2.000000	Y				
1.843200	Y	Y	Y	Y	Y

* Y indicates that the baud rate for that particular crystal is supported by the DS5000 serial loader auto-baud detection scheme.

POWER MANAGEMENT

The DS5000 is implemented using CMOS circuitry for low power consumption during full operation. Two software initiated modes are available for further power reduction for times when processing is not required and V_{CC} is at normal operating voltage. These are the Idle and Stop Modes. In addition, internal control circuitry automatically places the the DS5000 in its Data Retention Mode in the absence of V_{CC}.

The on-chip nonvolatile control circuitry monitors the V_{CC} for three below nominal operating voltage (Figure 3). When the voltage drops below the Power Fail Warning threshold (V_{PFW}) an interrupt will be generated to signal the processor of an impending power fail condition. This is to allow time for a service routine to save the operational state of the microcontroller prior to the V_{CC} dropping below the V_{CCmin} threshold. When this occurs, processor operation is automatically terminated by internally halting the clock after the entire circuit has been made ready for the Data Retention Mode. Finally, once V_{CC} voltage drops below the Lithium cell voltage threshold (V_{LI}) power from the embedded lithium cell is applied to place the device in its Data Retention Mode.

When V_{CC} voltage is again applied to the system, an internal Power On Reset cycle is executed without the need for any external components on the RST pin. In addition, internal status is available to distinguish the Power On Reset from other types of resets.

SOFTWARE SECURITY

The Software Security feature is implemented using Address and Data Encryptor circuitry which is present on the DS5000 die. Operation of the Software Security feature is performed by mainpulation of the 40-bit Encryption Key word and the Security Lock bit while in one of the Program Load modes. Encryption operation is first intiated by loading the 40-bit Encryption Key word.

When Software Encryption Operation is in effect and the Security Lock is disabled, the application software may be initially stored in an encrypted form during the initial loading of the device using one of the Program Load modes. As the loading is performed, the Data Encryptor logic transforms the opcode, operand, and data byte defined at each memory location defined by the software. Similarly, the Address Encryptor translates the "logical" address of each location into an encrypted address at which the byte is actually stored. Although each encryptor uses its own algorithm for encrypting data, both depend on the 40-bit key word which is contained in the Encryption Key registers (EK0-4).

As long as the Security Lock remains disabled, the actual unencrypted contents of the embedded Program/Data RAM may be read back for verification while in the Program Load mode. Once the contents have been verified, the final action performed during the Program Load Mode should be the enabling of the Security Lock bit. From this point on it will be impossible to read back the unencrypted contents of the Program/Data RAM or the contents of the Encryption Key registers.

When the application software is executed, the Address and Data Encryptors provide the opcodes, operands, and data to the CPU that execution of the application software can take place as normal. This action also takes place in real time so that no additional delays are imposed on the execution time of the software. Thus, the Software Encryption Operation is transparent to the application software.

The Software Encryption Operation is disabled and the contents of the Encryption Key regis-

ters are automatically erased whenever the Security Lock bit is cleared to a 0 from a previous 1 condition. This action renders the contents of the embedded Program/Data RAM useless, so that the application software can no longer be correctly interpreted by the DS5000 CPU. Although the contents of the Program/Data RAM can at this point be read back in a Program Load Mode, they cannot be de-encrypted since the original 40-bit key word has been lost.

ADDITIONAL INFORMATION

A complete description for all operational aspects of the DS5000, including an instruction set description, timing details, and electrical specifications is available in the DS5000 User's Guide (part # DS5000G).

DEVELOPMENT SUPPORT

Dallas Semiconductor offers two kit packages for developing and testing user code. The DS5000K Evaluation Kit allows the user to download Intel hex formatted code directly to the DS5000 from a PC-XT/AT or compatible computer. The kit consists of a DS5000-32-08, an interface pod, demo software, and an RS-232 connector that attaches to the COM1 or COM2 serial port of a PC.

The DS5000DK Development Kit consists of an assembler and a real-time in-circuit emulator that interfaces to a PC-XT/AT or compatible. See the DS5000K and DS5000DK data sheets for further details.

SELECTED ELECTRICAL CHARACTERISTICS

The following are selected electrical operating characteristics of the DS5000. A full set of electrical characterics is available in the DS5000 User's Guide.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to ground	-0.1 to 7.0V
Operating Temperature	-0 deg. to 70 deg. C
Storage Temperature	-40 deg. C to +70 deg. C
Soldering Temperature	260 deg. C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

D.C. CHARACTERISTICS

(T_A = 0 deg. C to 70 deg. C; V_{CC} = 5V ± 10%)

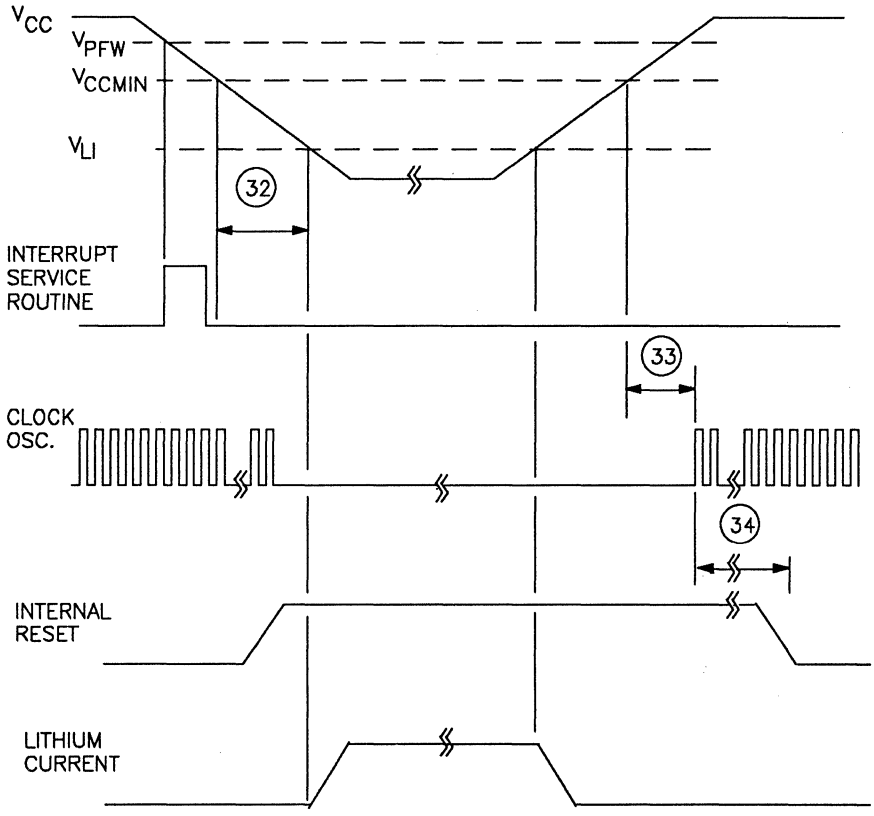
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	NOTES
Stop Mode Current	I_{SM}			80	uA	4
Power Fail Warning Voltage	V_{PFW}	4.15	4.6	4.75	V	
Minimum Operating Voltage	V_{CCmin}	4.05	4.5	4.65	V	
Lithium Supply Voltage	V_{LI}			3.3	V	
Programming Supply Voltage (Parallel Program Mode)	V_{PP}	12.5		13.0	V	
Program Supply Current	I_{pp}		9.2	15	mA	
Operating Current DS5000 8 DS5000 32	I_{CC}		20 25	43.2 48.2	mA	
Idle Mode Current	I_{CC}			6.2	mA	

A.C. CHARACTERISTICS
POWER CYCLING TIMING

(T_A = 0°C to 70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN.	MAX.	UNITS
32	Slew rate from V_{CCmin} to V_{LImax}	t_F	40		µs
33	Crystal start up time	t_{CSU}	(note 5)		
34	Power On Reset Delay	t_{POR}	2150*4t_{CLK}		µs

POWER CYCLING TIMING DIAGRAM Figure 3



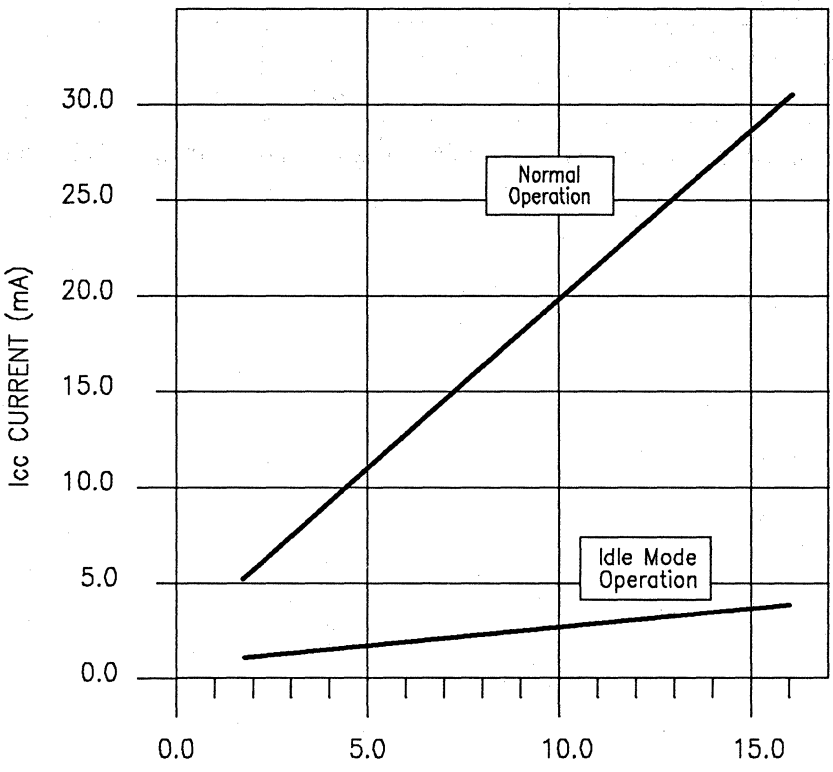
A.C.CHARACTERISTICS (T_A= 0°C to 70°C; V_{CC}= 5V ±10%)
PARALLEL PROGRAM LOAD TIMING

#	PARAMETER	SYMBOL	MIN.	MAX.	UNITS
40	Oscillator Frequency	$1/t_{CLK}$	1.0	12.0	MHz
41	Address Setup to PROG* low	t_{AVPRL}	0		t_{CLK}
42	Address Hold After PROG* high	t_{PRHAV}	0		t_{CLK}
43	Data Setup to PROG* low	t_{DVPRL}	0		t_{CLK}
44	Data Hold After PROG* low	t_{PRHDV}	0		t_{CLK}
45	P2.7, 2.6, 2.5 Setup to V_{PP}	t_{P2XHVP}	0		t_{CLK}
46	V_{PP} Setup to PROG* low	t_{VPHPRL}	0		t_{CLK}
47	V_{PP} Hold After PROG* low	t_{PRHVPL}	0		t_{CLK}
48	PROG* Width low	t_{PRW}	2400		t_{CLK}
49	Data Output from Address Valid	t_{AVDV}		48 1800*	t_{CLK} t_{CLK}
50	P2.7, 2.6 active to data valid	t_{DVP2XA}		48 1800*	t_{CLK} t_{CLK}
51	Data Hold after P2.7, 2.6 inactive	t_{P2XHDI}	0	48 240*	t_{CLK} t_{CLK}
52	Delay to Reset/PSEN* active after Power On	t_{PORPV}	26304		t_{CLK}
53	Reset/PSEN* active (or Verify inactive) to V_{PP} high		1200		t_{CLK}

54	V_{PP} inactive (between Program cycles)		1200		t_{CLK}
55	Verify active time	t_{VFT}	48 2400		t_{CLK} t_{CLK}

* Second set of numbers refer to expanded memory programming up to 32Kbytes.

DS5000 Icc VS FREQUENCY Figure 4



Normal operation is measured using

1) External crystals on XTAL1 and 2
2) All port pins disconnected
3) RST = 0 Volts and EA = VCC.
4) Part performing endless loop writing to internal memory.

Idle mode operation is measured using

1) External clock source at XTAL1; XTAL 2 floating
2) All port pins disconnected
3) RST = 0 Volts and EA = VCC
4) Part set in IDLE mode by software.

NOTES:

1. All voltages are referenced to ground.

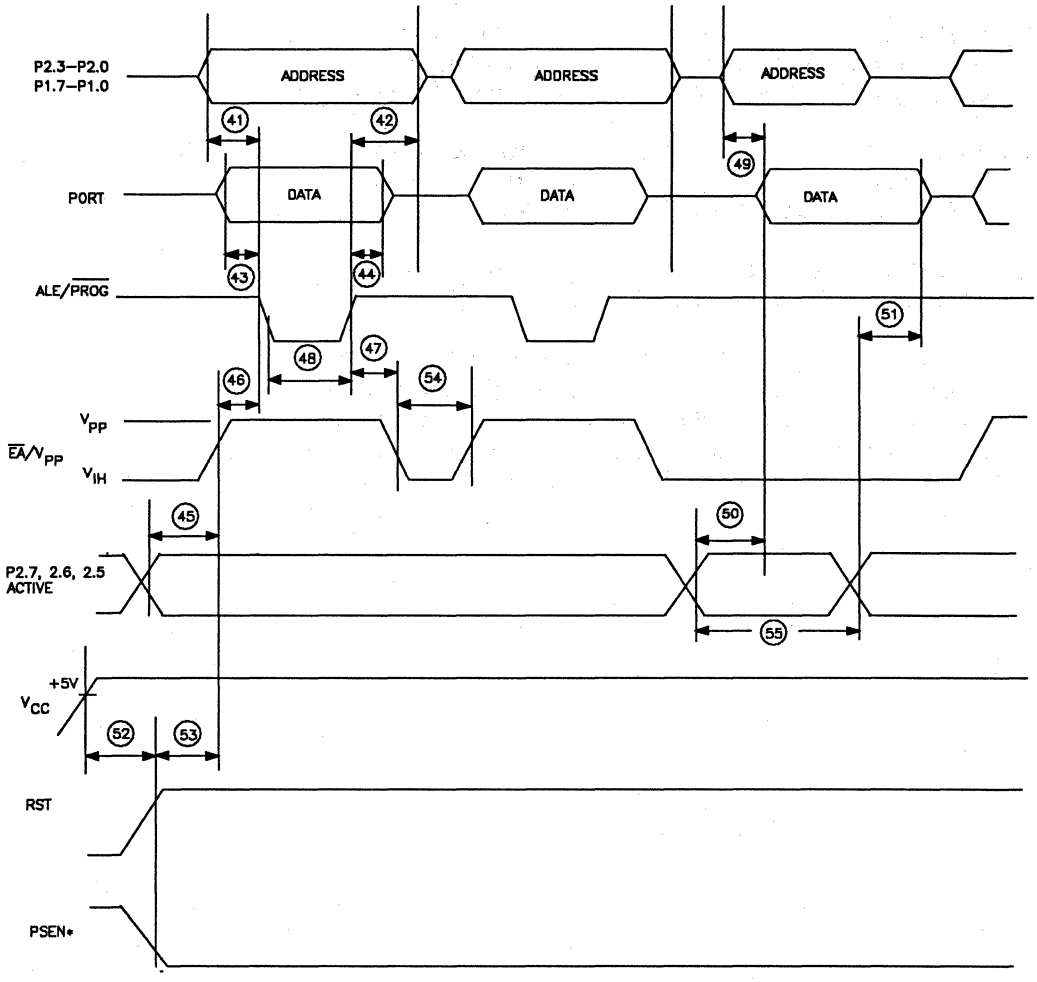
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V, V_{IH} = 4.5V; XTAL2 disconnected; EA*=RST=PORT0=V_{CC}.

3. Idle Mode I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V, V_{IH} = 4.5V; XTAL2 disconnected; EA*=RST=PORT0=V_{CC}.

4. Stop Mode I_{CC} is measured with all output pins disconnected; EA*=PORT0=V_{CC}; XTAL2 not connected; RST = V_{SS}.

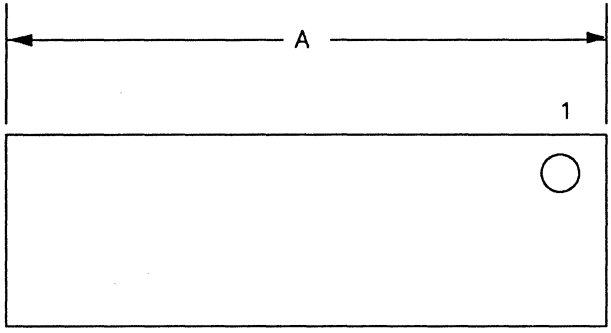
5. Crystal start up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on-chip oscillator. The user should check with the crystal vendor for a worst case spec on this time.

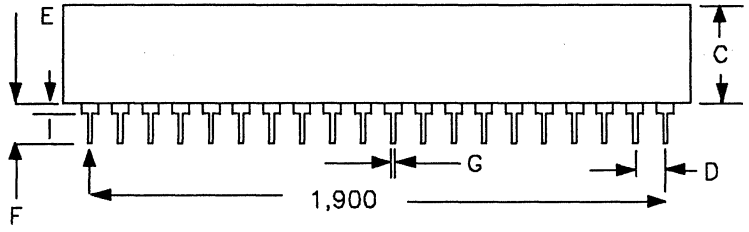
PARALLEL PROGRAM LOAD TIMING Figure 5

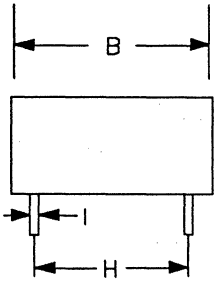


DS5000
Soft Microcontroller

DIM.	INCHES	
	MIN.	MAX.
A	2,080	2,100
B	.680	.700
C	.290	.310
D	.090	.110
E	.040	.060
F	.165	.185
G	.016	.020
H	.590	.610
I	.009	.012







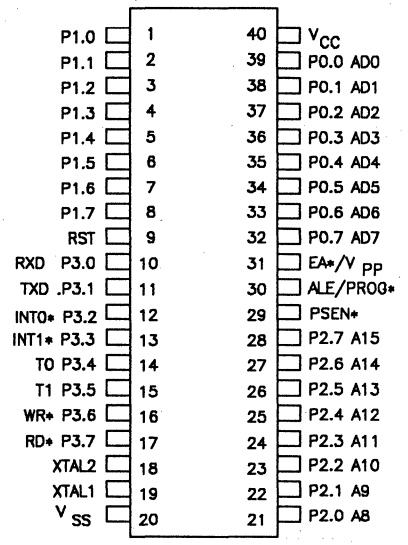
Dallas Semiconductor
Time Microcontroller

PRELIMINARY
DS5000T

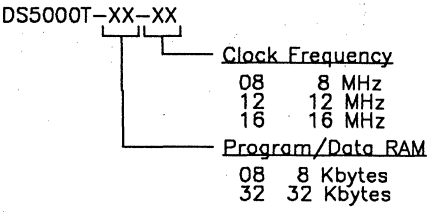
FEATURES

- DS5000 Soft Microcontroller with embedded clock/calendar
- Internal lithium cell preserves clock function in the absence of V_{CC}
- Permits logging of events with time and date stamp
- 8 or 32 Kbytes of embedded nonvolatile program/data RAM
- Program loading via on-chip full-duplex serial port
- User-selectable program/data memory partition
- All 4 ports available for system control
- Resident encryptor protects program from piracy
- Power sequencer and watchdog timer help ensure crash-proof operation
- Compatible with industry standard 8051 instruction set and pinout
- Clock accuracy is better than 2 min/month @25 deg C

PIN CONNECTIONS



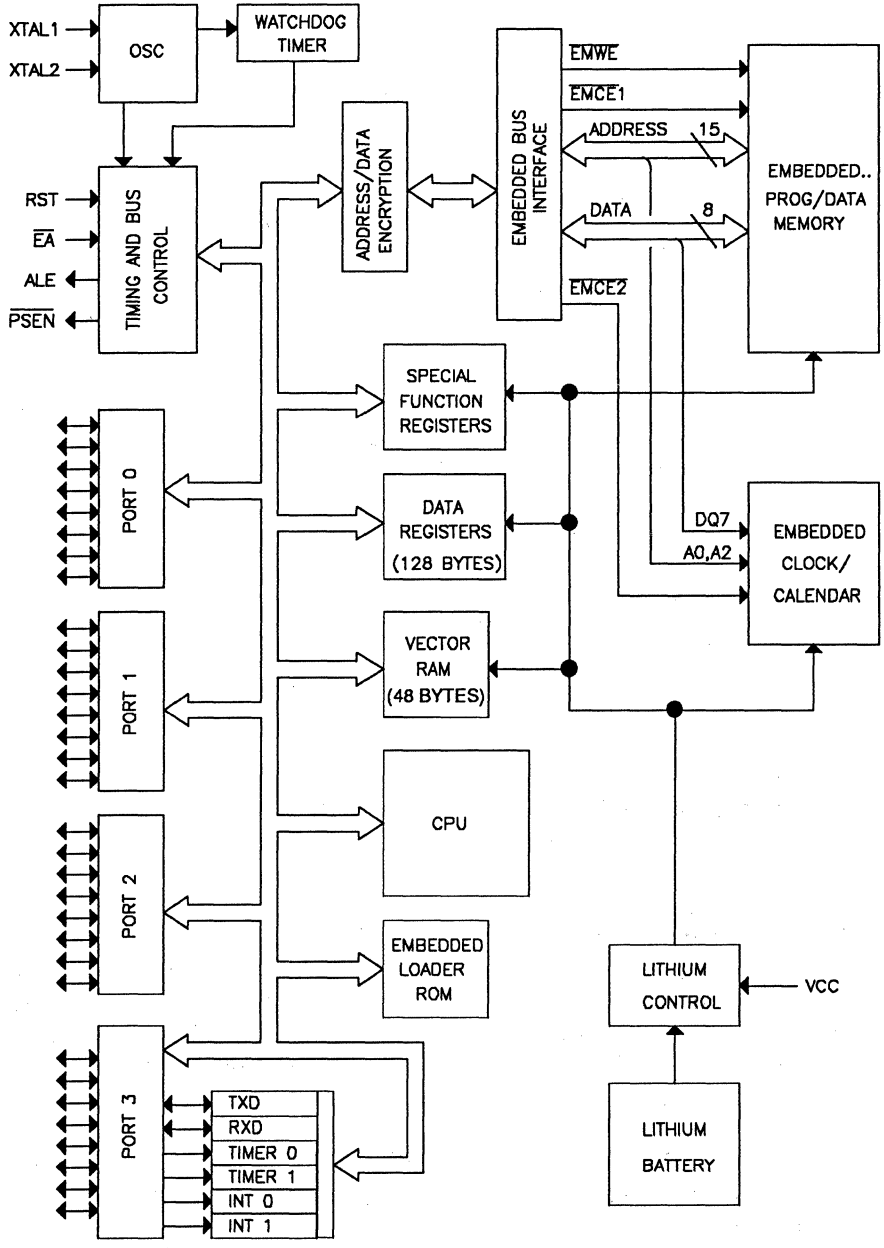
ORDERING INFORMATION



DESCRIPTION

The DS5000T Time Microcontroller offers all the features of the DS5000 with the added benefit of an embedded real-time clock/calendar function. The clock function itself is accessed as though it were a part of the embedded Data RAM so that the 32 I/O pins are free for the application use. With this feature, new and existing microcontrolled systems can now log events, schedule activities and time operations. The combination of DS5000T's "soft" features together with a real-time clock/calendar provides a powerful controller that adapts to the needs of time-driven applications.

DS5000T TIME MICROCONTROLLER BLOCK DIAGRAM Figure 1



ECC COMPARISON REGISTER DESCRIPTION Figure 2

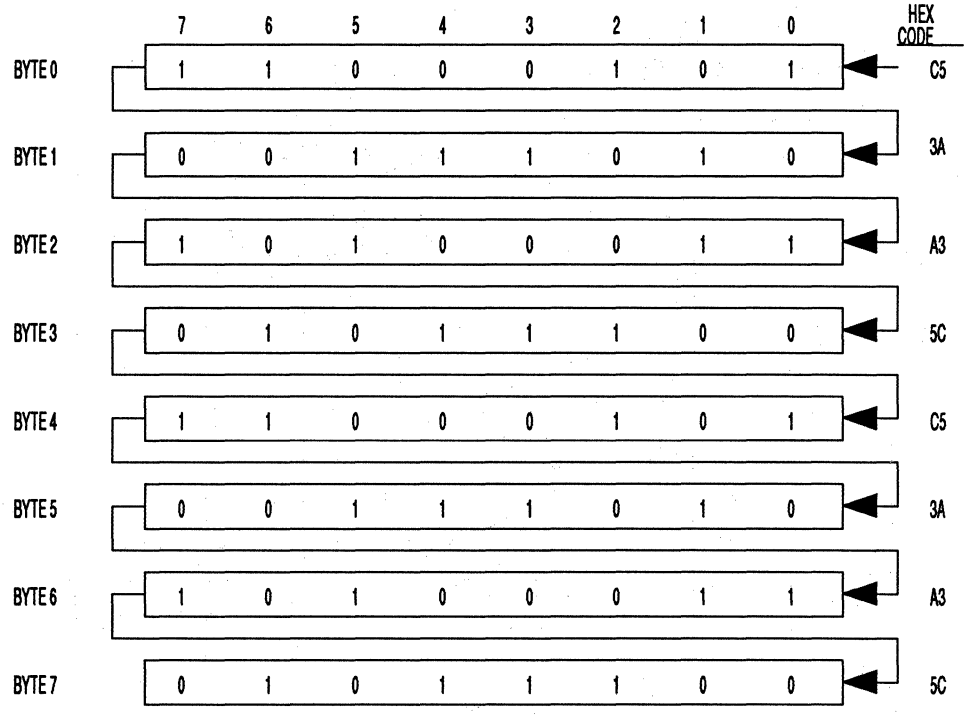


Figure 1 is the block diagram of the DS5000T, illustrating how the embedded program/data memory and the embedded clock/calendar (ECC) are connected to the CPU. The time parameters available are hundreths of seconds, seconds, minutes, hours, days, dates, months and years. Entry to the time function is identical to the serial communication method used by the DS1215 TimeChip. Basically, the time function appears as a slice of embedded data memory that is enabled by the ECE2 bit in the MCON special function register. This bit must be set to a logic 1 in order to select this new data memory map so that the time function appears to the CPU as simply a read/write memory location.

Aside from the clock/calendar function, the DS5000T operates just like the DS5000 Soft Microcontroller so that existing DS5000 code is upward compatible with the DS5000T. Features such as nonvolatile data/program memory, watchdog timer, power sequencer and software encryption are all preserved in the DS5000T. Please refer to the DS5000 data sheet and the User's Guide for full details on its operation.

EMBEDDED CLOCK/CALENDAR OPERATION

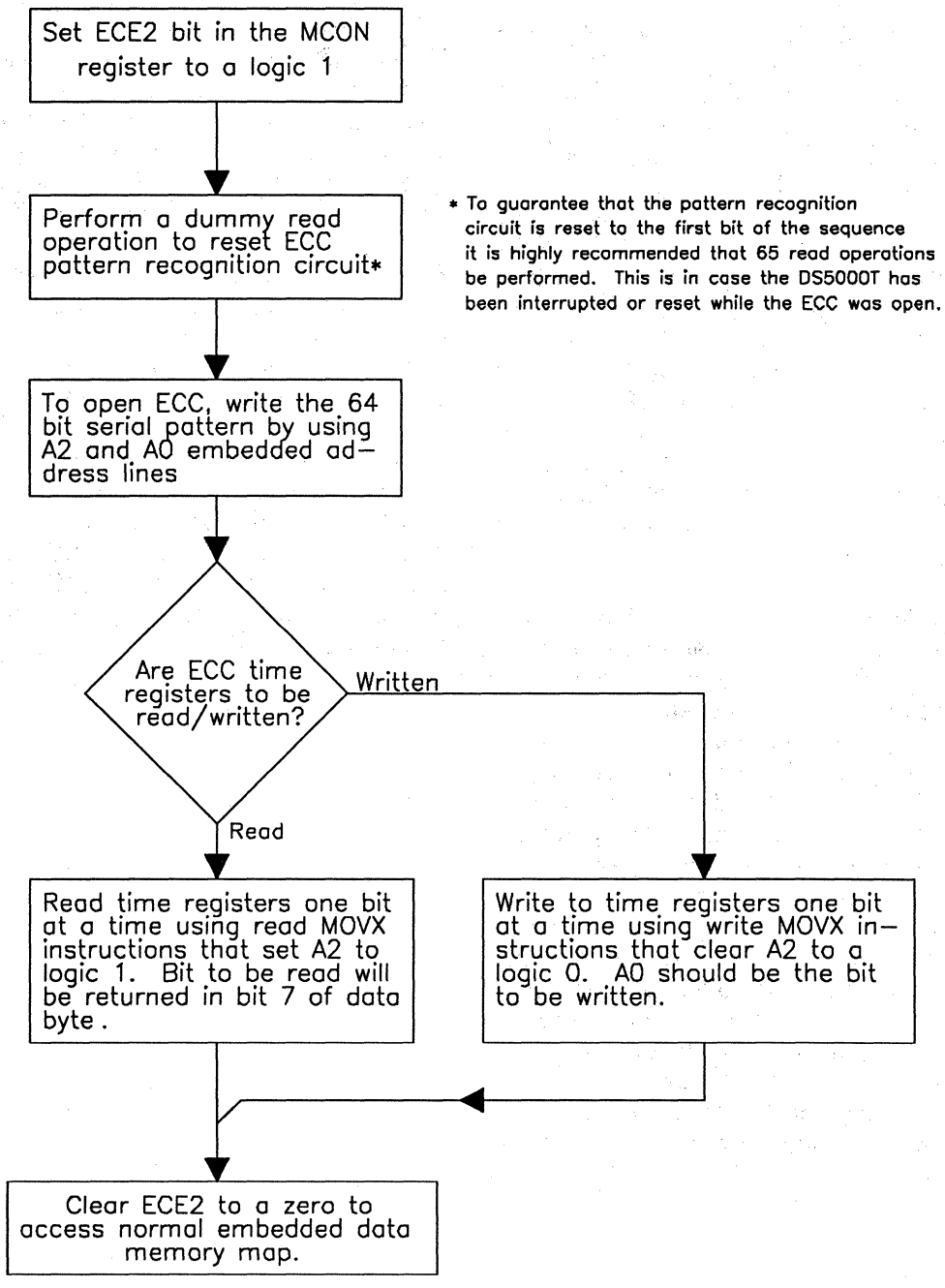
The embedded clock/calendar (ECC) operates much like the DS1215 TimeChip in that a 64 bit serial pattern must be written before time information can be read or written. The ECC has a pattern recognition circuit that checks incoming data to see that if it matches the necessary sequence which is illustrated in Figure 2. After all 64 bits match, the ECC is ready allow the time registers to either be written or read. To reset the pattern recognition circuit so as to look for bit 1 of the sequence, a read cycle must be performed. Then the 64 bits of the recognition sequence must be written to the ECC. If any bit should mismatch, the pattern recognition circuit will halt its operation and only a read cycle will be able to reset this circuit.

Communication to the ECC involves the use of the memory map enabled by bit ECE2 in the MCON register. Once this bit is set to a 1, all embedded memory read/write operations are directed to the ECC address space instead of the normal 8/32 Kbytes of embedded program/data memory. Actual read/write operations use embedded address lines A0 and A2 of the ECE2 memory map. To write a data bit to ECC, a MOVX instruction that forces A2 low and A0 to the state of the bit must be performed. *All other address lines should be set to a logic 0.* Address line A2 can be thought of as the write enable to the ECC and A0 as the write bit. Therefore, to write the 64 bits of the pattern recognition sequence, 64 MOVX instructions must be executed.

To read a data bit from the ECC once the 64-bit pattern has been entered, a read MOVX instruction (MOVX A,@Ri or MOVX A,@DPTR) must be executed that sets A2 to a 1. The data bit desired will be then be returned in bit 7 of the accumulator. Therefore, to retrieve the 8 bytes of time information in the ECC, 64 read MOVX instructions must be executed.

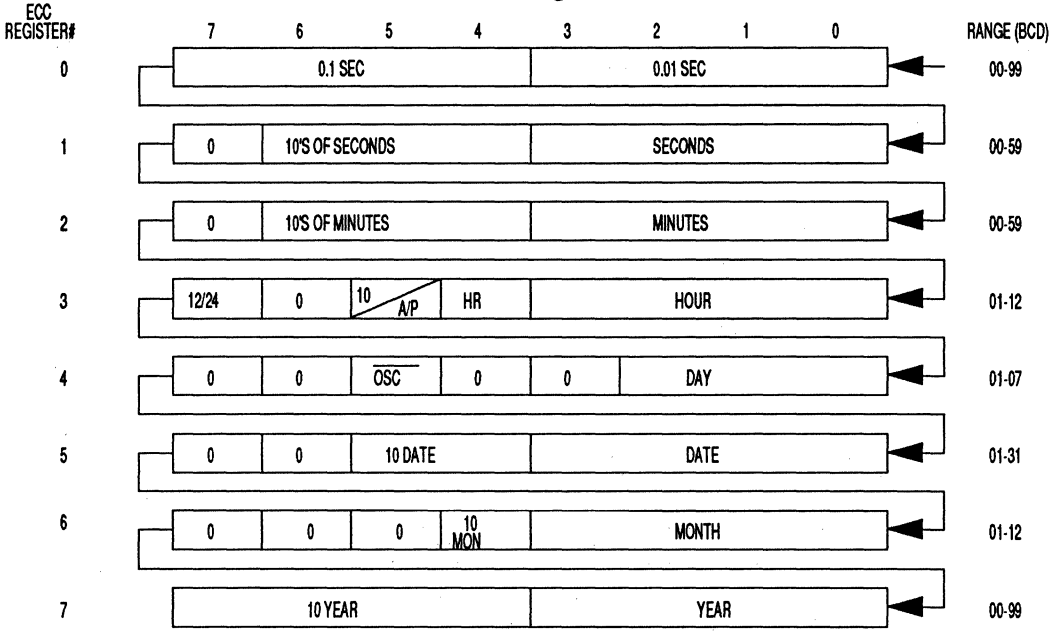
A flowchart is shown in Figure 3 which summarizes how to access the ECC for time retrieval and modification. Also, Appendix 1 lists a program called DEMODS5T which contains sample subroutines for communicating with the ECC that can be downloaded into the DS5000T (via the DS5000K for example). When DEMODS5T is run, a dumb terminal can retrieve the time from the DS5000T through the serial port (RXD,TXD). Please contact the Marketing Department for any assistance.

ECC REGISTER ENTRY FLOWCHART Figure 3



* To guarantee that the pattern recognition circuit is reset to the first bit of the sequence it is highly recommended that 65 read operations be performed. This is in case the DS5000T has been interrupted or reset while the ECC was open.

ECC TIME REGISTERS DESCRIPTION Figure 4



ECC REGISTERS

The time information in the ECC is contained in eight registers that are each 8 bits long. After the 64 bit recognition pattern has been received, data in these registers is accessed one bit at a time which is shown conceptually in Figure 4. It is recommended that data written to or read from the ECC include all 64 bits of the 8 time registers.

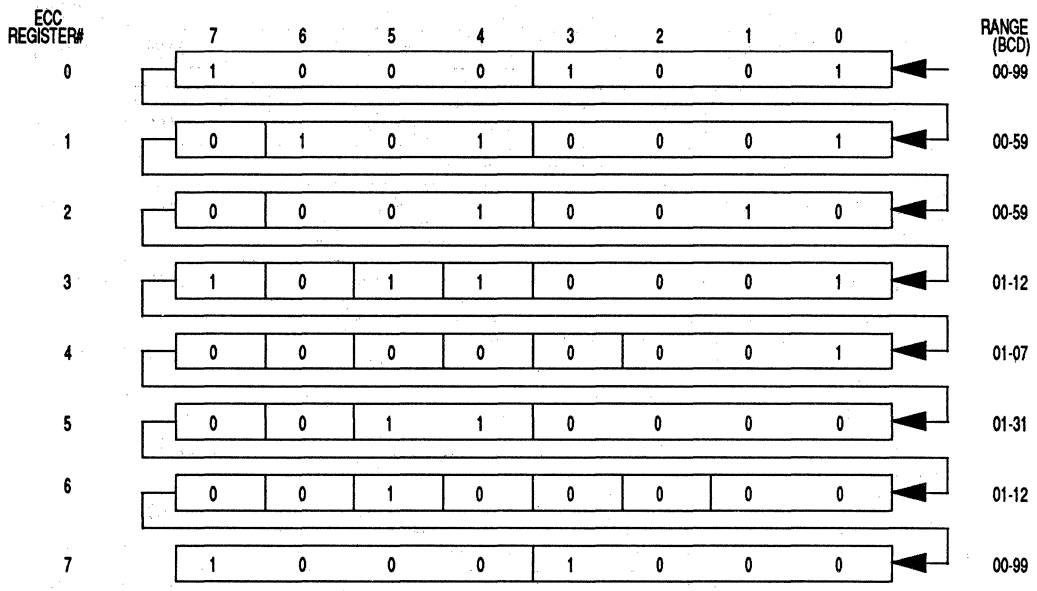
Register data is always in the BCD format except for the hours register (Reg 3) whose format changes depending upon the state of bit 7. If bit 7 is a one, the 12 hour mode is selected and bit 5 of the hours register becomes an AM/PM indicator; PM is indicated by a logic 1 while AM is a logic zero. If bit 7 is a zero, the 24 hour mode is selected and bit 5 becomes the second 10 hour bit (20-23 hours). Figure 5 contains examples that illustrate the content of these registers for different modes and times.

ECC SPECIAL BITS

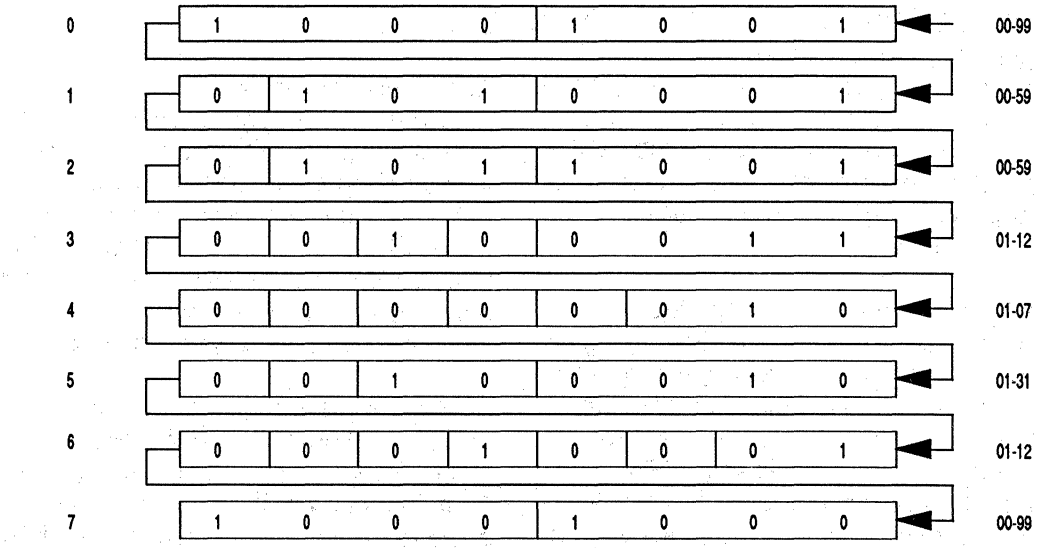
Bit 5 of the days register (REG 4) is the control bit for the ECC micro-power oscillator and it operates similiarly to that in the DS1215. Clearing bit 5 to a logic 0 enables the oscillator for normal operation; setting bit 5 to a logic 1 disables the oscillator and halts the ECC timekeeping. It is recommended that bit 5 always be cleared to 0.

Bit 4 of the days register does not affect ECC operation and can be set to any state. Register locations shown as logic 0's in Figure 6 will always return a 0 when being read. Write operations to these bit locations are ignored by the ECC and have no effect on its operation.

ECC TIME REGISTER EXAMPLES Figure 5



The time indicated is 11 o'clock PM, 12 minutes, 51.89 seconds.
The date indicated is Sunday, October 30th, 1988.



The time indicated is 2300 hour, 59 minutes, 51.89 seconds.
The date indicated is Monday, November 22th, 1988.

APPENDIX 1.
DS5000T DEMONSTRATION SOFTWARE

```
;    Program DEMODS5T
;
;    This program responds to commands received over the serial
;    I/O port to send or receive the date/time information between
;    the Embedded Clock/calendar (ECC) in the DS5000T and the
;    serial I/O port. This allows an external program access to the
;    date/time information.
;
;    The program first sets up the serial port for transmission at
;    9600 baud with eight data bits, no parity, and one stop bit.
;
;    Next, the program begins execution of a loop waiting for an
;    instruction from the serial port. Two valid instructions, R
;    and W, are recognized:
;
;        Receipt of the R character causes the DEMODS5T program
;        to read eight bytes of date/time information from
;        the DS1215 and send them out over the serial port.
;
;        Receipt of the W character causes the DEMODS5T program
;        to wait for eight bytes of date/time information
;        from the serial port and write them to the ECC.
;
;    Any other byte received from the serial port is incremented
;    and then sent back out to the serial port.
;
;
PCON    EQU     87H
MCON    EQU     0C6H
TA      EQU     0C7H
;
        CSEG    at    0
        SJMP    START
        CSEG    at    30H
START:                                  ; Initialization.
        MOV     TA,   #0AAH             ; Timed
        MOV     TA,   #55H              ;   access.
        MOV     PCON, #0                ; Reset watchdog timer.
```

```
        MOV     MCON,  #0F8H    ; Turn off CE2 for memory access.
        LCALL   CLOSE           ; Close date/time registers.

        MOV     IE,    #0
        MOV     TMOD,  #20H     ; Initialize the
        MOV     TH1,   #0FAH    ;   serial port
        MOV     TL1,   #0FAH    ;     for 9600
        ORL     PCON,  #80H     ;       baud.
        MOV     SCON,  #52H
        MOV     TCON,  #40H
L:
        JNB     RI,    L        ; Wait for character.
        CLR     RI              ; Clear the receiver.
        MOV     A,     SBUF     ; Load in the character.
        CJNE    A,#'R',H        ; Skip if not a read.
        LCALL   OPEN            ; Set up to read date/time.
        MOV     B,     #8       ; Set up to send 8 bytes.
F:
        LCALL   RBYTE           ; Read a byte of date/time.
G:
        JNB     TI,    G        ; Wait for end of previous send.
        CLR     TI              ; Clear transmitter.
        MOV     SBUF,           ; Send out the byte.
        DJNZ    B,     F        ; Loop for 8 bytes.
        SJMP    L               ; Return to main loop.
H:
        CJNE    A,#'W',J        ; Skip if not a write.
        LCALL   OPEN            ; Set up to read date/time.
        MOV     B,     #8       ; Set to receive 8 bytes.
I:
        JNB     RI,    I        ; Wait to receive a byte.
        CLR     RI              ; Clear the receiver.
        MOV     A,     SBUF     ; Bring in the byte.
        LCALL   WBYTE           ; Write a byte of date/time.
        DJNZ    B,     I        ; Loop for 8 bytes.
        SJMP    L               ; Return to main loop.
J:
        JNB     TI,    J        ; If it is neither an R nor a W,
        CLR     TI              ;   increment the character,
        INC     A               ;   send it back out to the
        MOV     SBUF,           ;   serial port, and then
        SJMP    L               ;   return to the main loop.
```

```
;
;*************************************************************************************
;** SUBROUTINE TO OPEN THE EMBEDDED CLOCK/CALENDAR (ECC)**
;*************************************************************************************
;
;  This subroutine executes the sequence of reads and writes which
;  is required in order to open communication with the timekeeper.
;  The subroutine returns with the timekeeper opened for data
;  access and with both the accumulator and B register modified.
;
OPEN:    LCALL   CLOSE           ; Make sure it is closed.
         MOV     B,#4            ; Set pattern period count.
         MOV     A,#0C5H         ; Load first byte of pattern.
OPENA:   LCALL   WBYTE           ; Send out the byte.
         XRL     A,#0FFH         ; Generate next pattern byte.
         LCALL   WBYTE           ; Send out the byte.
         SWAP    A               ; Generate next pattern byte.
         DJNZ    B,OPENA         ; Repeat until 8 bytes sent.
         RET                     ; Return.
;
;*********************************************
;**** SUBROUTINE TO CLOSE ECC **
;*********************************************
;
;  This subroutine insures that the registers of the timekeeper
;  are closed by executing 9 successive reads of the date and time
;  registers.  The subroutine returns with both the accumulator
;  and the B register modified.
;
CLOSE:   MOV     B,#9            ; Set up to read 9 bytes.
CLOSEA:  LCALL   RBYTE           ; Read a byte;
         DJNZ    B,CLOSEA        ; Loop for 9 byte reads.
         RET                     ; Return.
;
;*************************************************************
;**** SUBROUTINE TO READ A DATA BYTE****
;*************************************************************
;
;  This subroutine performs a "context switch" to the CE2 data
;  space and then reads one byte from the timekeeping device.
;  Then it switches back to the CE1 data space and returns
;  the byte read in the accumulator, with all other registers
```

```
; unchanged.
;
RBYTE:  PUSH   DPL          ; Save the data
        PUSH   DPH          ;   pointer on stack.
        PUSH   MCON         ; Save MCON register.
        ORL    MCON,#4      ; Switch to CE2.
        PUSH   B            ; Save the B register.
        MOV    DPL ,#4      ; Set up for data input.
        MOV    DPH, #0      ; Set high address byte.
        MOV    B,  #8       ; Set the bit count.
LI:     PUSH   ACC          ; Save the accumulator.
        MOVX   A,  @DPTR    ; Input the data bit.
        RLC    A            ; Move it to carry.
        POP    ACC          ; Get the accumulator.
        RRC    A            ; Save the data bit.
        DJNZ   B,  LI       ; Loop for a whole byte.
        POP    B            ; Restore the B register.
        POP    MCON         ; Restore MCON register.
        POP    DPH          ; Restore the data
        POP    DPL          ;   pointer from stack.
        RET                 ; Return.
;
;*************************************************************
;**** SUBROUTINE TO WRITE A DATA BYTE *****
;*************************************************************
;
; This subroutine performs a "context switch" to the CE2 data
; space and then writes one byte from the accumulator to the
; timekeeping device. Then it switches back to the CE1 data
; space and returns with all registers unchanged.
;
WBYTE:  PUSH   DPL          ; Save the data
        PUSH   DPH          ;   pointer on stack.
        PUSH   MCON         ; Save MCON register.
        ORL    MCON,#4      ; Switch to CE2.
        PUSH   B            ; Save the B register.
        MOV    DPH, #0      ; Set high address byte.
        MOV    B,  #8       ; Set the bit count.
LO:     PUSH   ACC          ; Save the accumulator.
        ANL    A,  #1       ; Set up bit for output.
        MOV    DPL, A       ; Set address to write bit.
        MOVX   A,  @DPTR    ; Output the data bit.
```

```
        POP     ACC             ; Restore the accumulator.
        RR      A               ; Position next bit.
        DJNZ    B,  LO          ; Loop for a whole byte.
        POP     B               ; Restore the B register.
        POP     MCON            ; Restore MCON register.
        POP     DPH             ; Restore the data
        POP     DPL             ;   pointer from stack.
        RET                     ; Return.
;
;*****************************************
;
;**** END OF PROGRAM **********
;*****************************************
;
;
        END                     ; End of program.
```

SELECTED ELECTRICAL CHARACTERISTICS

The following are selected electrical operating characteristics of the DS5000T. A full set of electrical characterics is available in the DS5000 User's Guide.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to ground	- 0.1 to 7.0V
Operating Temperature	- 0° to 70° C
Storage Temperature	- 40°C to +70° C
Soldering Temperature	- 260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ± 10%)

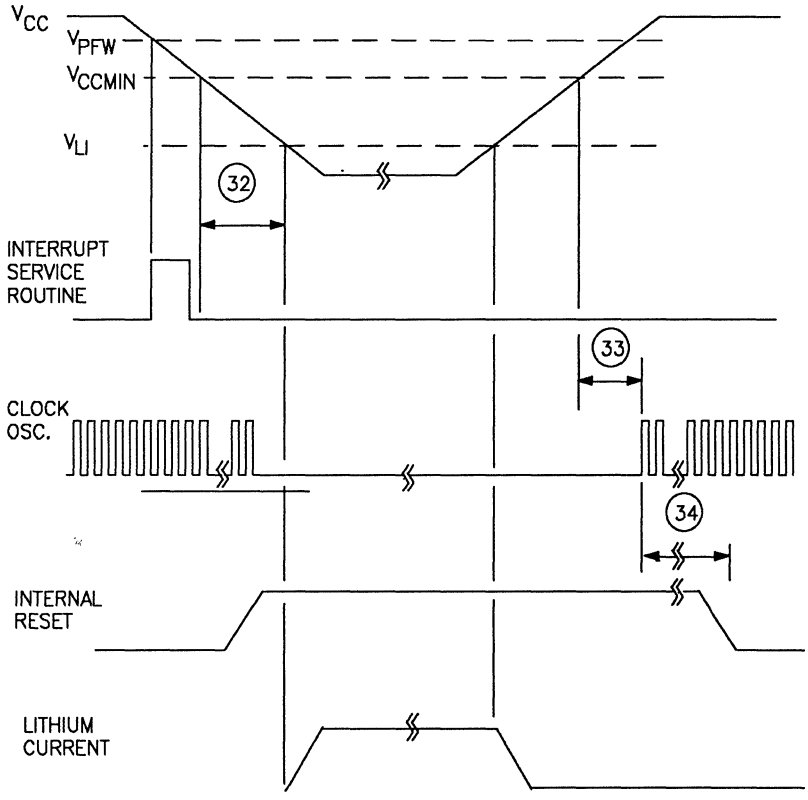
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	NOTES
Stop Mode Current	I_{SM}		45	80	uA	4
Power Fail Warning Voltage	V_{PFW}	4.15	4.6	4.75	V	
Minimum Operating Voltage	V_{CCmin}	4.05	4.5	4.65	V	
Lithium Supply Voltage	V_{LI}			3.3	V	
Programming Supply Voltage (Parallel Program Mode)	V_{PP}	12.5		13.0	V	
Program Supply Current	I_{pp}		9.2	15	mA	
Operating Current DS5000 8 (@12 MHz) DS5000 32	I_{CC}		20 25	43.2 48.2	mA	2
Idle Mode Current (@12 MHz)	I_{CC}			6.2	mA	3

A.C. CHARACTERISTICS
POWER CYCLING TIMING

(T_A = 0°C to 70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN.	MAX.	UNITS
32	Slew rate from V_{CCmin} to V_{LImax}	t_F	40		µs
33	Crystal start up time	t_{CSU}	(note 5)		
34	Power On Reset Delay	t_{POR}	2150*4t_{CLK}		µs

POWER CYCLING TIMING DIAGRAM Figure 6

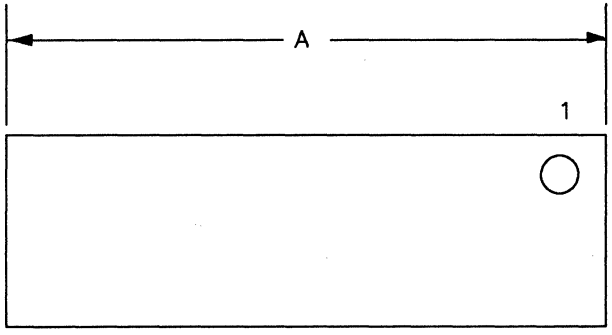


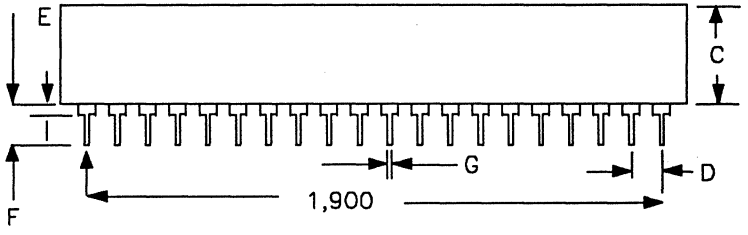
NOTES:

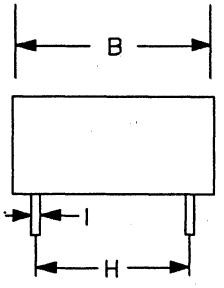
1. All voltages are referenced to ground.
2. Maximum operating ICC is measured with all output pins disconnected; XTAL1 driven with a clock source at 12 MHz with tCLKR, tCLKF = 10 ns, VIL =0.5V, VIH = 4.5V; XTAL2 disconnected; /EA=RST=PORT0=VCC.
3. Idle Mode ICC is measured with all output pins disconnected; XTAL1 driven with tCLKR, tCLKF = 10 ns, VIL = 0.5V, VIH = 4.5V; XTAL2 disconnected; EA=RST= PORT0=VCC.
4. Stop Mode ICC is measured with all output pins disconnected; EA=PORT0=VCC; XTAL2 not connected; RST = VSS.
5. Crystal start up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on-chip oscillator. The user should check with the crystal vendor for a worst case spec on this time.

DS5000T
Time Microcontroller

DIM.	INCHES	
	MIN.	MAX.
A	2,080	2,100
B	.680	.700
C	.290	.310
D	.090	.110
E	.040	.060
F	.165	.185
G	.016	.020
H	.590	.610
I	.009	.012



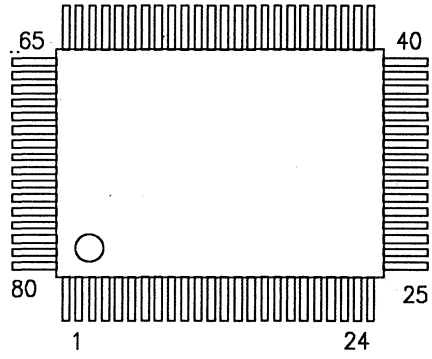




FEATURES

- Offers the microcontroller die used in the DS5000 DIP packaged in an 80-pin Quad Flat Pack (QFP)
- Provides access to Embedded Address/Data Bus signals not available on the DS5000 DIP
- Embedded Address/Data bus frees up port pins for I/O use
- Direct interface to byte wide memories
- Supports up to 64 KBytes of Program/Data memory
- Incorporates battery switching/monitoring circuitry for powering external memory devices in the absence of Vcc
- Ultra-low standby current--less than 75 nA
- Fully compatible with 8051 instruction set

PIN CONNECTIONS



ORDERING INFORMATION

DS5000FP-XX	-08	08 MHz
	-12	12 MHz
	-16	16 MHz

DESCRIPTION

The DS5000FP 80-pin Quad Flat Pack (QFP) version contains a stand-alone DS5000 die which normally resides in a 40-pin DS5000 DIP package. It retains all the hardware features of a DS5000 DIP and can be used much like ROM-less versions of the 8051 except that with the DS5000FP all four ports are freed up for general-purpose I/O. An external battery can be attached to this chip to power external SRAM(s) in the absence of Vcc. This gives the user the flexibility of using his own batteries and memories to implement a non-volatile microcontroller solution with the "soft" features inherent in the DS5000 DIP. EPROM devices can be used for program memory in applications not requiring reloadable software.

Of the 80-pins on the package, only 68 are actually tied to pads on the die. The rest of the pins are no-connects. 40-pins of the 68 signal pins are identical in function to the 40 pins of a standard DS5000. The other 28-pins are normally used to interface to the Embedded RAM and the lithium source on the standard DS5000 DIP products.

PIN DESCRIPTION (by pin number)

The pin assignments for this package according to pin number are summarized below (names with an * suffix indicate active low signals):

PIN	SIGNAL	DESCRIPTION
1	P0.4	Port 0 bit 4
2	NC	No Connect
3	NC	No Connect
4	EA9	Embedded Address line 9
5	P0.3	Port 0 bit 3
6	EA8	Embedded Address line 8
7	P0.2	Port 0 bit 2
8	EA13*	Embedded Address line 13
9	P0.1	Port 0 bit 1
10	ER/W*	Read/Write
11	P0.0	Port 0 bit 0
12	V_{cco}	V_{cc} output to CMOS static RAM V_{cc} pin
13	V_{cc}	V_{cc} input from system power supply
14	V_{cc}	V_{cc} input from system power supply
15	P1.0	Port 1 bit 0
16	EA14*	Embedded Address line 14
17	P1.1	Port 1 bit 1
18	EA12	Embedded Address line 12
19	P1.2	Port 1 bit 2
20	EA7	Embedded Address line 7
21	P1.3	Port 1 bit 3
22	NC	No Connect
23	NC	No Connect
24	EA6	Embedded Address line 6
25	P1.4	Port 1 bit 4
26	EA5	Embedded Address line 5
27	P1.5	Port 1 bit 5
28	EA4	Embedded Address line 4
29	P1.6	Port 1 bit 6
30	EA3	Embedded Address line 3
31	P1.7	Port 1 bit 7
32	NC	No Connect - internally tied to substrate
33	EA2	Embedded Address line 2
34	RST	Reset
35	EA1	Embedded Address line 1
36	P3.0 / RXD	Port 3 bit 0 / Receive Data Input
37	EA0	Embedded Address line 0
38	P3.1 / TXD	Port 3 bit 1 / Transmit Data Output

39	P3.2 / INT0*	Port 3 bit 2 / External Interrupt Input 0
40	P3.3 / INT1*	Port 3 bit 3 / External Interrupt Input 1
41	P3.4 / T0	Port 3 bit 4 / Timer Counter Input 0
42	NC	No Connect
43	NC	No Connect
44	P3.5 / T1	Port 3 bit 5 / Timer Counter Input 1
45	P3.6 / WR*	Port 3 bit 6 / Write Enable
46	P3.7 / RD*	Port 3 bit 7 / Read Enable
47	XTAL2	Crystal Input 2
48	XTAL1	Crystal Input 1
49	P2.0	Port 2 bit 0
50	P2.1	Port 2 bit 1
51	P2.2	Port 2 bit 2
52	GND	Ground
53	GND	Ground
54	V_{LI}	Lithium Voltage Input
55	ED0	Embedded Data line 0
56	P2.3	Port 2 bit 3
57	ED1	Embedded Data line 1
58	P2.4	Port 2 bit 4
59	ED2	Embedded Data line 2
60	P2.5	Port 2 bit 5
61	ED3	Embedded Data line 3
62	NC	No Connect
63	NC	No Connect
64	P2.6	Port 2 bit 6
65	ED4	Embedded Data line 4
66	P2.7	Port 2 bit 7
67	ED5	Embedded Data line 5
68	PSEN*	Program Store Enable
69	ED6	Embedded Data line 6
70	ALE	Address Latch Enable
71	ED7	Embedded Data line 7
72	NC	No Connect - internally tied to substrate
73	EA*	External Access Enable
74	ECE1*	Embedded Chip Enable 1
75	P0.7	Port 0 bit 7
76	EA10	Embedded Address line 10
77	P0.6	Port 0 bit 6
78	ECE2*	Embedded Chip Enable 2
79	P0.5	Port 0 bit 5
80	EA11	Embedded Address line 11

PIN DESCRIPTION (by pin function)

The following is a pin description organized by pin function:

PIN	SIGNAL	DESCRIPTION
13,14	V_{cc}	V_{cc} input from system power supply
52-53	GND	Ground
47	XTAL2	Crystal Input 2
48	XTAL1	Crystal Input 1
68	PSEN*	Program Store Enable
70	ALE	Address Latch Enable
73	EA*	External Access Enable
34	RST	Reset
75	P0.7	Port 0 bit 7
77	P0.6	Port 0 bit 6
79	P0.5	Port 0 bit 5
1	P0.4	Port 0 bit 4
5	P0.3	Port 0 bit 3
7	P0.2	Port 0 bit 2
9	P0.1	Port 0 bit 1
11	P0.0	Port 0 bit 0
31	P1.7	Port 1 bit 7
29	P1.6	Port 1 bit 6
27	P1.5	Port 1 bit 5
25	P1.4	Port 1 bit 4
21	P1.3	Port 1 bit 3
19	P1.2	Port 1 bit 2
17	P1.1	Port 1 bit 1
15	P1.0	Port 1 bit 0
66	P2.7	Port 2 bit 7
64	P2.6	Port 2 bit 6
60	P2.5	Port 2 bit 5
58	P2.4	Port 2 bit 4
56	P2.3	Port 2 bit 3
51	P2.2	Port 2 bit 2
50	P2.1	Port 2 bit 1
49	P2.0	Port 2 bit 0
46	P3.7 / RD*	Port 3 bit 7 / Read Enable

45	P3.6 / WR*	Port 3 bit 6 / Write Enable
44	P3.5 / T1	Port 3 bit 5 / Timer Counter Input 1
41	P3.4 / T0	Port 3 bit 4 / Timer Counter Input 0
40	P3.3 / INT1*	Port 3 bit 3 / External Interrupt Input 1
39	P3.2 / INT0*	Port 3 bit 2 / External Interrupt Input 0
38	P3.1 / TXD	Port 3 bit 1 / Transmit Data Output
36	P3.0 / RXD	Port 3 bit 0 / Receive Data Input
12	V_{cco}	V_{cc} output to CMOS static RAM V_{cc} pin
54	V_{LI}	Lithium Voltage Input
16	EA14*	Embedded Address line 14
8	EA13*	Embedded Address line 13
18	EA12	Embedded Address line 12
80	EA11	Embedded Address line 11
76	EA10	Embedded Address line 10
4	EA9	Embedded Address line 9
6	EA8	Embedded Address line 8
20	EA7	Embedded Address line 7
24	EA6	Embedded Address line 6
26	EA5	Embedded Address line 5
28	EA4	Embedded Address line 4
30	EA3	Embedded Address line 3
33	EA2	Embedded Address line 2
35	EA1	Embedded Address line 1
37	EA0	Embedded Address line 0
71	ED7	Embedded Data line 7
69	ED6	Embedded Data line 6
67	ED5	Embedded Data line 5
65	ED4	Embedded Data line 4
61	ED3	Embedded Data line 3
59	ED2	Embedded Data line 2
57	ED1	Embedded Data line 1
55	ED0	Embedded Data line 0
74	ECE1*	Embedded Chip Enable 1
78	ECE2*	Embedded Chip Enable 2
10	ER/W*	Embedded Bus Read/Write

The following discussion provides information specifically for use with the DS5000FP. Consult the DS5000 DIP data sheet and user's guide for a complete explanation of the DS5000s' features and operation.

EMBEDDED ADDRESS/DATA BUS

The embedded address and data busses are used on the DS5000FP to connect to external byte-wide memory devices. Pins A0-A14 address up to 32 KBytes of Program/Data memory which is transferred over pins ED0-ED7 (a bidirectional port). An additional 32 KBytes of data memory (cannot be used for program memory) can be addressed by using ECE2* (manipulation of ECE2* is described in the DS5000 data sheet). The ER/W* signal connects to the WE* inputs of the memory devices to indicate a read or write operation. Figure 1 shows a typical connection using 32Kx8 SRAM devices while Figure 2 shows one with 8Kx8 devices.

The ECE1* signal is used to enable a single memory device for program and/or data memory. The address partition between program and data memory is determined by the contents of the MCON register just like in the normal DS5000 DIP. Also the range bit in the MCON register must match the size of the memory attached: either 8 or 32 KBytes. The timing characteristics of the embedded address/data bus and its associated control signals (ECE1*, ECE2* and ER/W*) are given at the back of this data sheet.

MEMORY SELECTION

When using battery-backed SRAM with the DS5000FP, the most important parameter to be cognizant of is the standby current drain of the SRAM. This parameter together with the capacity of the battery determine the how long data will remain nonvolatile. Some recommended SRAM's that offer low standby current are shown below:

8K x 8	32K x 8
Toshiba TC5564	
NEC uPD4464	
Sharp LH5164	
Hitachi HM6264LP-SL	HM62256LP-SL

Typically, larger memory sizes (e.g. 32K x 8) consume more dynamic and standby current; consequently a larger capacity battery may be required for an acceptable data retention lifespan.

BATTERY SELECTION

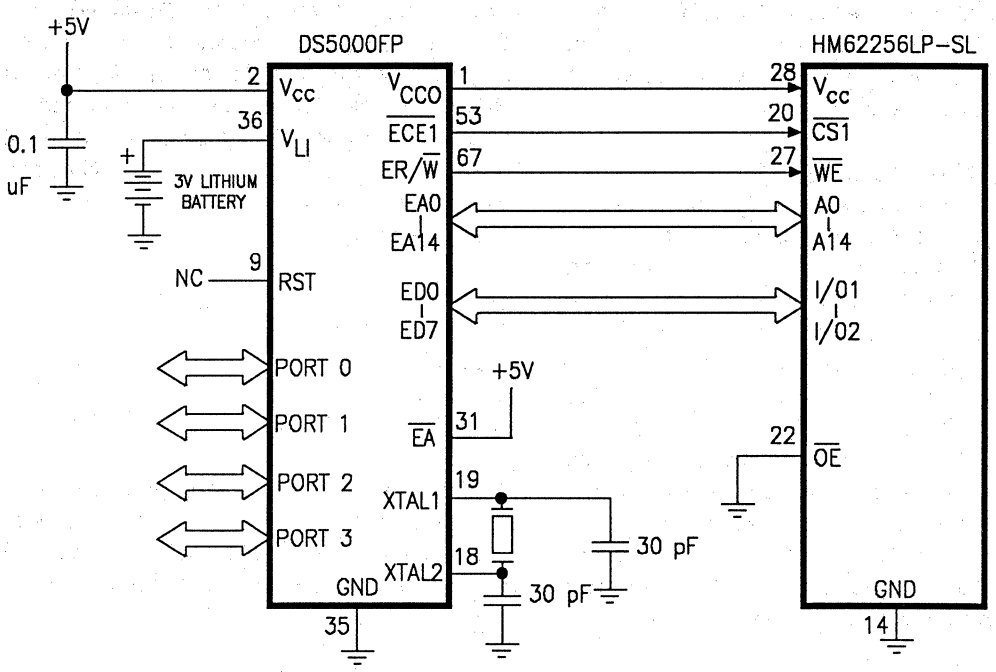
To maintain a data retention lifespan of 10 years or greater, the lithium enery source offers a compact, reliable choice. Typical lithium sources offer 10 years of shelf life and capacities exceeding 200 mA-hours (mAH). For example, a type CR2330 manganese dioxide 3V lithium battery (260 mAH) when used with a Hitachi HM62256LP-SL can typically provide 14.8 years of continuous data retention at 25 degrees C. The calculation which should be used is shown below and can be used to estimate data retention lifespans with different memory/battery combinations:

$$\text{Data retention} = \frac{(\text{battery capacity in mAH})/(\text{memory standby current} + 75\ \text{nA})}{(24\ \text{hours})(365\ \text{days/year})}$$

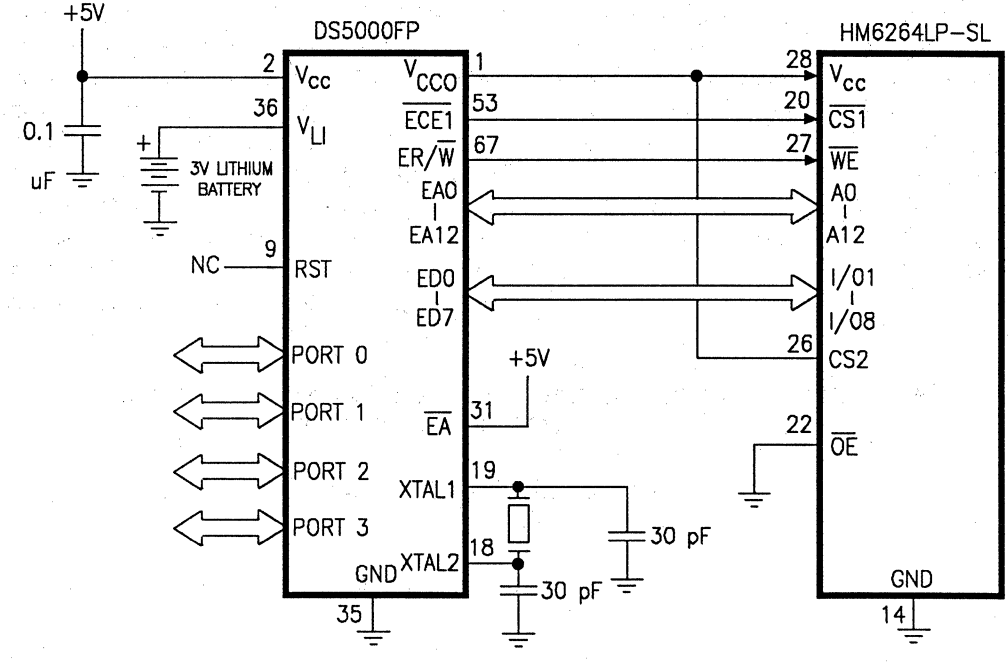
$$= \frac{(260\text{mAH})/(0.002\ \text{mA typical})}{(24)(365)}$$

$$= 14.8\ \text{years typical.}$$

DS5000 INTERCONNECTION WITH 32K x 8 SRAM Figure 1



DS5000FP INTERCONNECTION WITH 8K x 8 SRAM Figure 2



The 75 nA figure refers to the maximum internal leakage current of the DS5000FP when it is operating in the data retention mode (V_{CC} is absent). Type CR batteries are highly recommended because their voltage variability under load is very stable. This is important because the battery voltage is used to define the trip point at which the DS5000FP enters the data retention mode (when the battery is switched in to power the SRAM and the internal registers). Some recommended 3V lithium batteries are shown below:

Source & P/N	Capacity
Panasonic CR1620	60 mAH
Panasonic CR2330	260 mAH
Sanyo CR1620	60 mAH
Sanyo CR2430	270 mAH

The cheaper, smaller capacity batteries are listed for applications where the SRAM's are screened to lower standby currents (published SRAM standby currents are usually very conservative).

If battery voltages other than 3V are used, it should be noted that most CMOS SRAM's are guaranteed to retain data only to 2V. The internal voltage drop from the VLI input (pin 36) to V_{CCO} (pin 1) is typically 0.5V which means that a 3V battery will cause an actual 2.5 volts to appear at V_{CCO}, resulting in a 0.5V margin. V_{CCO} would be connected to the V_{CC} input(s) of the connected SRAM(s). Lower battery voltages than 3V will of course result in less margin.

POWER MANAGEMENT

The trip points that use the battery voltage at V_{LI} as a reference are V_{PFW}, V_{CCMIN} and V_{LI}. V_{PFW} (Power Fail Warning) is the voltage threshold for V_{CC} which causes the PCON.5 bit to be set. In addition, a Power Fail Warning interrupt will be generated if so enabled by the EPFW bit (PCON.3). Full processor operation continues at this point. However, if V_{CC} dips below V_{CCMIN}, ECE1*, ECE2* and EA14* go high to protect the external RAM contents. (EA14* stays high for use with 8Kx8 RAMs). The processor is shut down and all other pins are three-stated. The V_{CC} source still powers all circuitry at this time. When V_{CC} dips further to below V_{LI}, the battery source present at V_{LI} will begin to supply current to the DS5000 and to devices powered from the V_{CCO} output. ECE1*, ECE*2 and EA14 remain high, although high at whatever V_{CCO} is at (which typically is VLI - 0.5V). Consult the DS5000 USER's GUIDE for further details about the power management features.

In the DS5000 DIP spec, absolute numbers are given for the V_{PFW}, V_{CCMIN} and V_{LI} since the battery used is internal and not a variable determined by the user. In the DS5000FP however, the battery used is a variable and affects the trip points accordingly. To determine the resultant trip points for a given battery voltage, use the following equations (V_{LI} refers to the actual battery voltage):

V_{PFW} = 1.45 X VLI
V_{CCMIN} = 1.40 X VLI
V_{LI}(trip) = 1.00 X VLI

ENCRYPTION NOTES

The resident encryptor of the DS5000FP operates identically as in the DIP version. When encryption is enabled by loading the encryption key registers with a 40-bit key, the DS5000FP will encrypt both data and addresses using this key value as a seed. Encryption only operates on program/data memory controlled by ECE1*; *data memory controlled by ECE2* will not be encrypted.*

ABSOLUTE MAXIMUM RATINGS *

Voltage on any pin relative to ground	-0.1 to 7.0V
Operating Temperature	-0 deg. to 70 deg. C
Storage Temperature	-40 deg. C to +70 deg. C
Soldering Temperature	260 deg. C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

The DS5000FP adheres to all of the published A.C. and D.C. specifications for the DS5000. The following are additional operating characteristics which apply only to the DS5000FP. In the following specifications 1 TCLK machine cycle = 12 oscillator cycles.

D.C. CHARACTERISTICS (T_A = 0 to 70 deg C; V_{CC} = 5V± 10%)

PARAMETER	SYM.	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input High Voltage (all pins except XTAL1 and RST)	V_{IH1}	2.0		V_{CC}+0.3	V	
Input High Voltage (RST, XTAL1)	V_{IH2}	3.5		V_{CC}+0.3	V	
Output Low Voltage @ I_{OL} = 1.6 mA (Ports 1,2,3)	V_{OL1}		0.15	0.45	V	
Output Low Voltage @ I_{OL} = 3.2 mA (Port 0, ALE, PSEN*, EA0-14, EAD0-7, ER/W*, ECE1*, ECE2*)	V_{OL2}		0.15	0.45	V	
Output High Voltage @ I_{OH} = -80 uA (Ports 1,2,3)	V_{OH1}	2.4	4.8		V	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output High Voltage @ I_{OH} = -400 uA (Port 0, ALE, PSEN*, EA0-14, EAD0-7, ER/W*, ECE1*, ECE2*)	V_{OH2}	2.4	4.8		V	
Input Low Current @ V_{IN} = 0.45 V (Ports 1,2,3)	I_{IL}			-50	uA	
Transition Current 1 to 0; V_{IN} = 2.0 V (Ports 1,2,3)	I_{TL}			-500	uA	
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0)	I_{L1}			± 10	uA	
Input Leakage Current 0.0 ≤ V_{IN} ≤ 0.1 or V_{CC} - 0.1 ≤ V_{IN} ≤ V_{CC} (ED0-7)	I_{L2}			± 100	uA	
Input Leakage Current 0.1 < V_{IN} < V_{CC} - 0.1 (ED0-7)	I_{L3}			± 1	mA	
RST, EA* pull-down resistor	R_{RE}	40		125	Kohm	
Operating Supply Current @ 12 MHz	I_{CC}		25		mA	1
Stop Mode Current	I_{SM}			80	uA	2
Idle Mode Current @ 12 MHz	I_{IM}		4.0	6.2	mA	3
Lithium battery voltage (V_{LI})	V_{LB}	3.1		3.25	V	4
Output supply voltage (V_{CCO})	V_{CCO1}	V_{CC}-0.3			V	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output supply voltage battery-backed mode (V_{CCO}, ECE1*, ECE2* EA14*)	V_{CCO2}		V_{LI}-0.5		V	
Output supply current @ $V_{CCO} = V_{CC}$ - 0.3V	I_{CCO1}			80	mA	5
Battery-backed quiescent current	I_{LI}		5	75	nA	6

NOTES:

1. Maximum operating I_{CC} is measured with all port pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V, V_{IH} = 4.5V; XTAL2 disconnected; EA* = RST = Port 0 = V_{CC}.

2. Stop mode I_{CC} is measured with all ouput pints disconnected; EA* = Port 0= V_{CC}; XTAL2 disconnected; RST = VSS.

3. Idle mode I_{CC} is measured with all ouput pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V, V_{IH} = 4.5V; XTAL2 disconnected; EA* = Port 0 = V_{CC}, RST = VSS.

4. Measured with no load on the battery. The range given guarantees that the DS5000FP will meet all published specifications for the DS5000, especially those concerning power management trip points (V_{FW} and V_{CC} min).

5. I_{CCO1} is the maximum average operating current that can be drawn from V_{CCO} in normal operation.

6. I_{LI} is the current drawn from V_{LI} input when V_{CC} = 0V and V_{CCO} is disconnected.

EMBEDDED ADDRESS/DATA BUS TIMING
A.C. CHARACTERISTICS

(T_A = 0° to 70° C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN.	MAX.	UNITS
56	Delay to Embedded Address Valid from ECE1* low during opcode fetch	t_{CE1LPA}		20	ns
57	ECE1* or ECE2* Pulse Width	t_{CEPW}	4TCLK-15		ns
58	Embedded Address Hold after ECE1* high during opcode fetch	t_{CE1HPA}	2TCLK-20		ns
59	Embedded Data setup to ECE1* high during opcode fetch	t_{OVCE1H}	1TCLK+40		ns
60	Embedded Data hold after ECE1* high during opcode fetch	t_{CE1HOV}	10		ns
61	Embedded Address Hold after ECE1* or ECE2* high during MOVX	t_{CEHDA}	4TCLK-30		ns
62	Delay from Embedded Address Valid to ECE1* or ECE2* low during MOVX	t_{CELDA}	4TCLK-25		ns
63	Embedded Data setup to ECE1* or ECE2* high during MOVX (read)	t_{DACEH}	1TCLK+40		ns
64	Embedded Data hold after ECE1* or ECE2* high during MOVX (read)	t_{CEHDV}	10		ns
65	Embedded Address Valid to ER/W* active during MOVX (write)	t_{AVRWL}	3TCLK-35		ns
66	Delay from ER/W* low to Valid Data Out during MOVX (write)	t_{RWLDV}	20		ns
67	Valid Data Out hold time from ECE1* or ECE2* high	t_{CEHDV}	1TCLK-15		ns
68	Valid Data Out hold time from ER/W* high	t_{RWHDV}	0		ns
69	Write pulse width (ER/W* low time)	t_{RWLPW}	6TCLK-20		ns

EMBEDDED ADDRESS/DATA BUS OPCODE FETCH CYCLE Figure 3

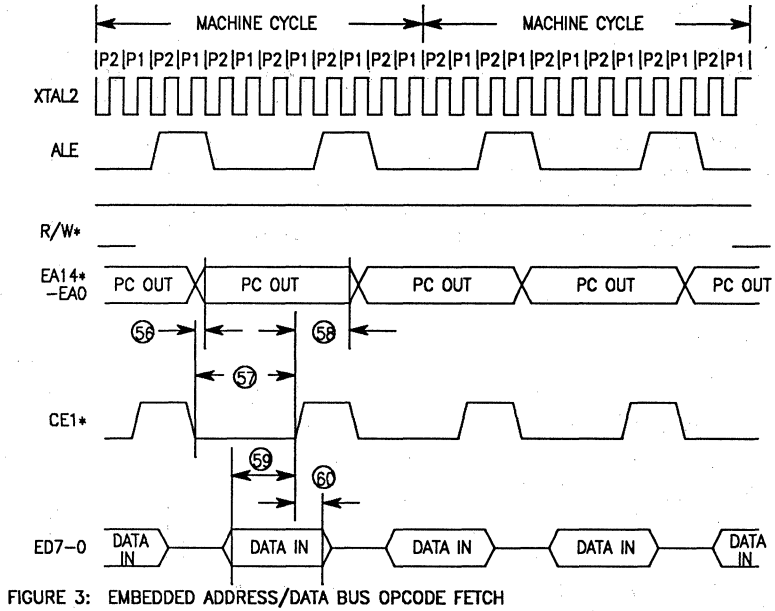
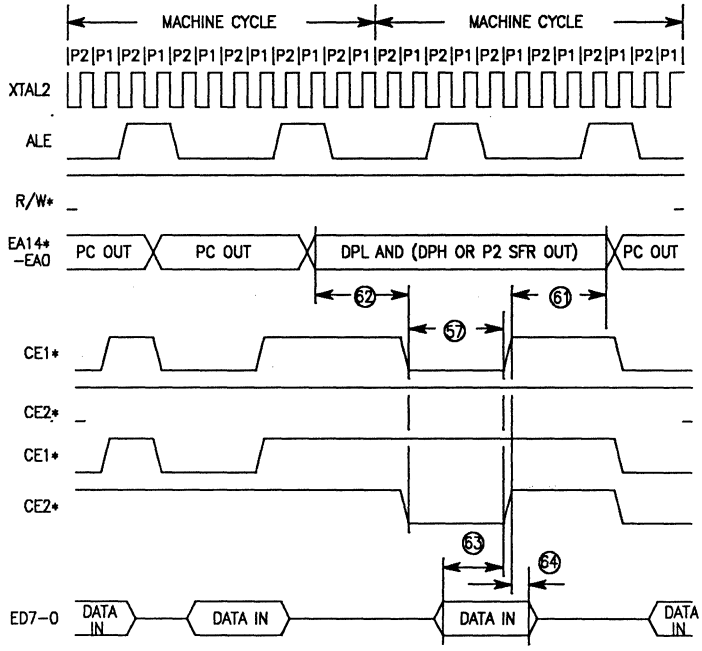
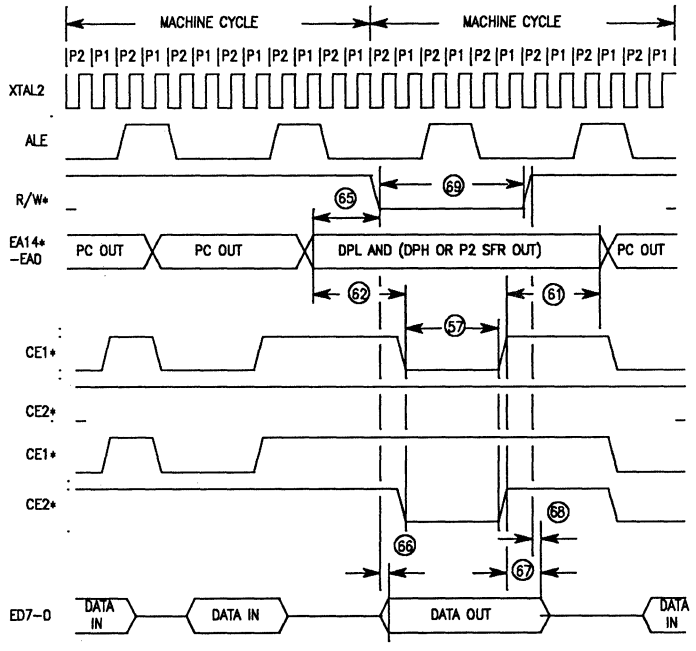


FIGURE 3: EMBEDDED ADDRESS/DATA BUS OPCODE FETCH WITH EMBEDDED DATA MEMORY READ

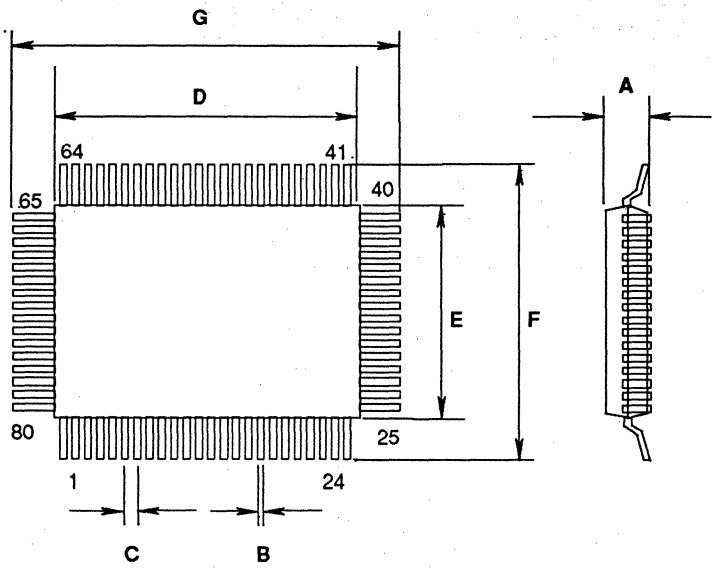
EMBEDDED ADDRESS/DATA BUS OPCODE FETCH WITH EMBEDDED DATA MEMORY READ Figure 4

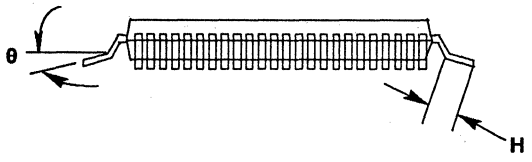


EMBEDDED ADDRESS/DATA BUS OPCODE FETCH WITH EMBEDDED DATA MEMORY WRITE Figure 5



DS5000FP
CMOS MICROCONTROLLER





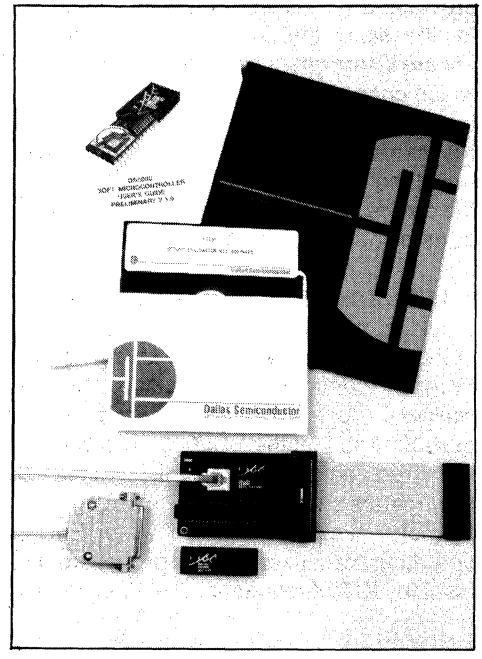
DIM	MILLIMETERS		
	MIN.	NOM	MAX.
A	—	2.91	3.15
B	.25	.35	.45
C	—	0.80	—
D	19.85	20.00	20.15
E	13.85	14.00	14.15
F	17.40	17.86	18.20
G	23.40	23.86	24.20
H	0.40	—	1.3
θ	0°	5°	10°

Dallas Semiconductor
Evaluation Kit

PRELIMINARY
DS5000TK

FEATURES:

- Allows immediate evaluation of DS5000T or DS5000 in an existing application
- Supplied with DS5000T 32, software diskette, DS5000 User's Guide, In System Loader hardware
- Supports in-system serial downloading of DS5000T from an IBM PC host
- DS5000T supports all functions of DS5000 with addition of real-time clock
- Downloads/verifies Intel Hex absolute object files residing on IBM PC
- User-friendly software prompts user for required system configuration information
- Supports serial download rates up to 9600 bps
- Requires no support circuit overhead on target system



DESCRIPTION

The DS5000TK is a development support system which is designed to allow immediate evaluation of the DS5000T Time Microontroller in a system application. The DS5000TK is an upgraded version of the DS5000K. Since the DS5000T performs all of the functions associated with the DS5000 Soft Microcontroller, it may also be used for evaluation of any of the versions of a DS5000 for a new or existing design.

Materials provided with the kit include a DS5000T with 32 Kbytes of RAM, full documentation on the DS5000 and DS5000T, In System Loader serial download hardware, and software for the IBM PC (KIT5K). Using the Evaluation Kit, the user can quickly configure the DS5000T for operation in the target system. This configuration can be performed without detailed knowledge of the operation of the DS5000's Serial Load Mode. The DS5000T Evaluation Kit not only serves as a first-time evaluation system for the DS5000 or the DS5000T, but also performs the equivalent function of an EPROM programming system throughout the prototyping phase of the design cycle.

The Evaluation Kit's In System Loader hardware allows application software to be loaded into the DS5000T while it is connected to the target system, eliminating the need for removal of the device when reprogramming is required. The In System Loader hardware consists of an RS232 cable that connects to the RS232 Fixture which houses the appropriate interface circuitry and provides a 40-pin Zero-Insertion-Force socket for the either the DS5000 or DS5000T. The Fixture in turn attaches to the 40-pin target cable which connects to the microcontroller socket in the target system. The hardware provides the mechanism for the KIT5K software to take control of the DS5000T via the RS232 cable, place the device in its Serial Program Load Mode, and transmit new software to the device.

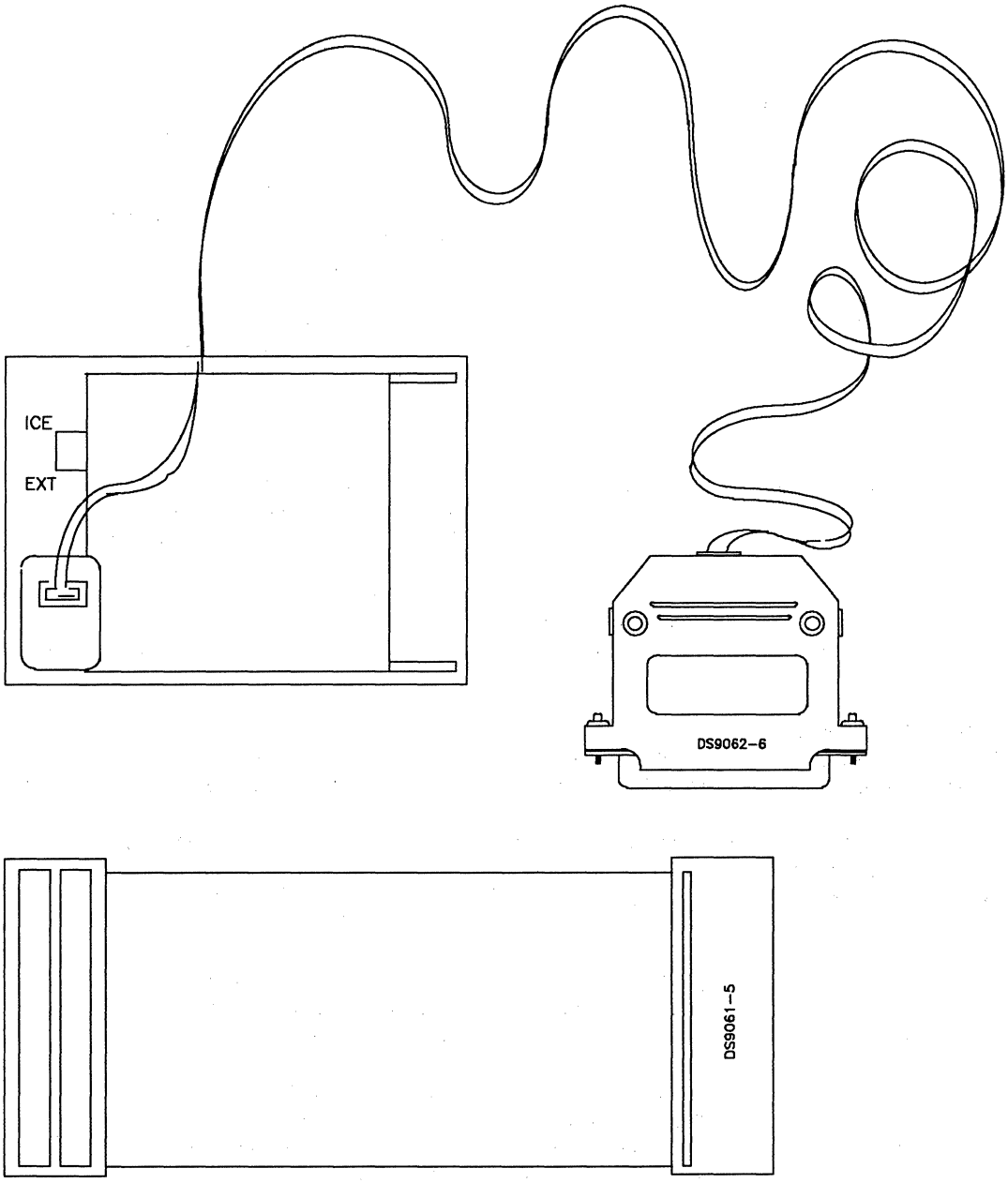
KIT5K is a user-friendly software package which provides a high-level user interface to the DS5000T via its Serial Load Mode. When the Program command is executed, the user is walked through a series of system configuration questions so that the DS5000T can be properly initialized before downloading takes place. Parameters such as the device's Program/Data Memory mapping and Software Encryption operation are initialized in the proper order in this fashion. KIT5K manages all of the communication with the DS5000T during the downloading process, so that the details of the serial download operation can remain transparent to the user. For more advanced users, KIT5K provides a number of commands which allow individual manipulation of the DS5000's resources. For example, these commands allow the direct initialization of the MCON register, loading of the 40-bit Encryption Key word, and setting and clearing of the Security Lock. In addition, an individual memory location examine and change capability is provided to allow patches to be made to the application software. When the loading operation is completed, the device can be released on command from the PC to run the application software.

SYSTEM REQUIREMENTS

The Evaluation Kit requires an IBM PC or compatible with DOS 2.0 or later and at least 128K bytes of memory. In addition an RS232 port must be available which is configured as COM1 (03F8H, IRQ4) or COM2 (02F8H, IRQ3). Displays which are supported include monochrome, color graphics, or enhanced graphics (Mode 3).

Power (+5V) must be supplied to the RS232 fixture from the V_{CC} pin of the target system via the Target Cable (see figure 1).

DS5000T EVALUATION KIT: IN SYSTEM LOADER HARDWARE FIGURE 1



The In System Loader hardware consists of the components which are depicted in Figure 1, and which are described below:

Name	Dallas Part #	Description
RS232 Connector	DS9062-6	Adaptor with cable. Adaptor provides DB25 female connector for connection to an RS232C IBM PC COM port on one side and RJ11 female on the other side. Cable carries RS232 signals required by the kit with two male RJ11 jacks on either end.
RS232 Fixture	DS9060	RS232 serial interface for DS5000. Provides RJ11 female for RS232 signal connection, 40-pin DIP IC socket for DS5000, and 40-pin PC edge connector for connection to target cable.
Target Cable	DS9061-5	40-pin adaptor cable which connects the 40-pin edge connector on the RS232 Fixture to the target system microcontroller socket.

The purpose of the In System Loader hardware is to serially download the DS5000T on command from the KIT5K software in such a manner that it will be transparent to the hardware on the target system.

KIT5K COMMANDS

KIT5K is the software environment supplied with the DS5000T Evalution Kit. It provides a high-level interface for loading application software to the DS5000T or for setting its configuration parameters.

After KIT5K has been invoked and the prompt has been displayed (as described above), commands may be entered by the user. KIT5K operates either in interactive mode, or in batch mode. The user will not see any of the communication between KIT5K and the DS5000T (except when debug is on). The following is a summary of commands recognized by the KIT5K software.

cd	Change to another directory or show the default directory.
com	Specify the COM port for the In System Loader hardware.
dir	List the default directory or specified path.
display	List Embedded RAM contents in debug format.
do	Execute a list of KIT5K commands from a file.
dump	Dump Embedded RAM in Intel Hex to a file.
edit	Individual examine/change Embedded RAM bytes in DS5000T.
exit	Exit the KIT5K program; return to MS-DOS.
fill	Fill Embedded RAM with a constant value.
help	Describe the function and syntax of KIT5K commands.

key	Load the 40-bit Encryption Key word.
load	Load Embedded RAM from an Intel Hex object file.
lock	Set the Security Lock on the DS5000T.
logoff	Disable logging of KIT5K commands.
logto	Log KIT5K commands to the specified file.
mcon	Set the MCON register with a specified value.
partition	Set the Partition Address with a specified value.
pgmode	Place the DS5000T in its Serial Load Mode.
program	Program the automatically with a configuration file.
quit	Same as exit; leave the KIT5K program; return to MS-DOS.
range	Set the Range Address to 8K or 32K.
run	Disable Serial Load Mode; begin execution.
speed	Specify the serial baud rate to be used during loading.
status	Display status.
type	Type the requested filename to the screen.
unlock	Clear Security Lock.
verify	Verify Embedded RAM with the specified Intel Hex file.

ELECTRICAL SPECIFICATIONS

Operating Temperature Range	0 to +50 degrees C
System Power Supply Requirements from Target System (DS5000 installed in target system; no load on port pins, PSEN*, ALE)	+5V @ 100 mA max; 50 mA typical

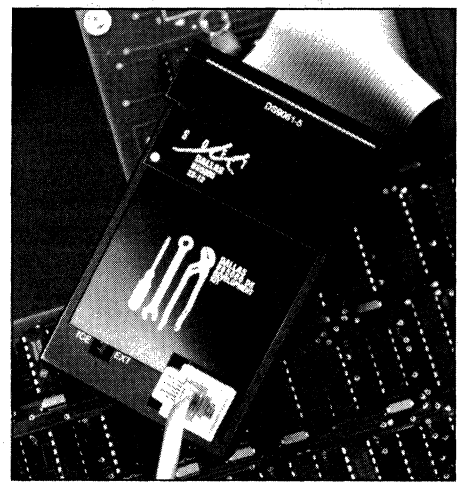
INTERFACE

Connectors:
25-pin RS232 'D' type to RJ11 jack adaptor
RJ11 on RS232 Fixture
40-pin card edge (0.1" centers) on RS232 Fixture
40-pin edge connector on Target Cable
40-pin DIP plug on Target Cable

Dallas Semiconductor
DS5000 Development Kit

PRELIMINARY
DS5000DK

FEATURES



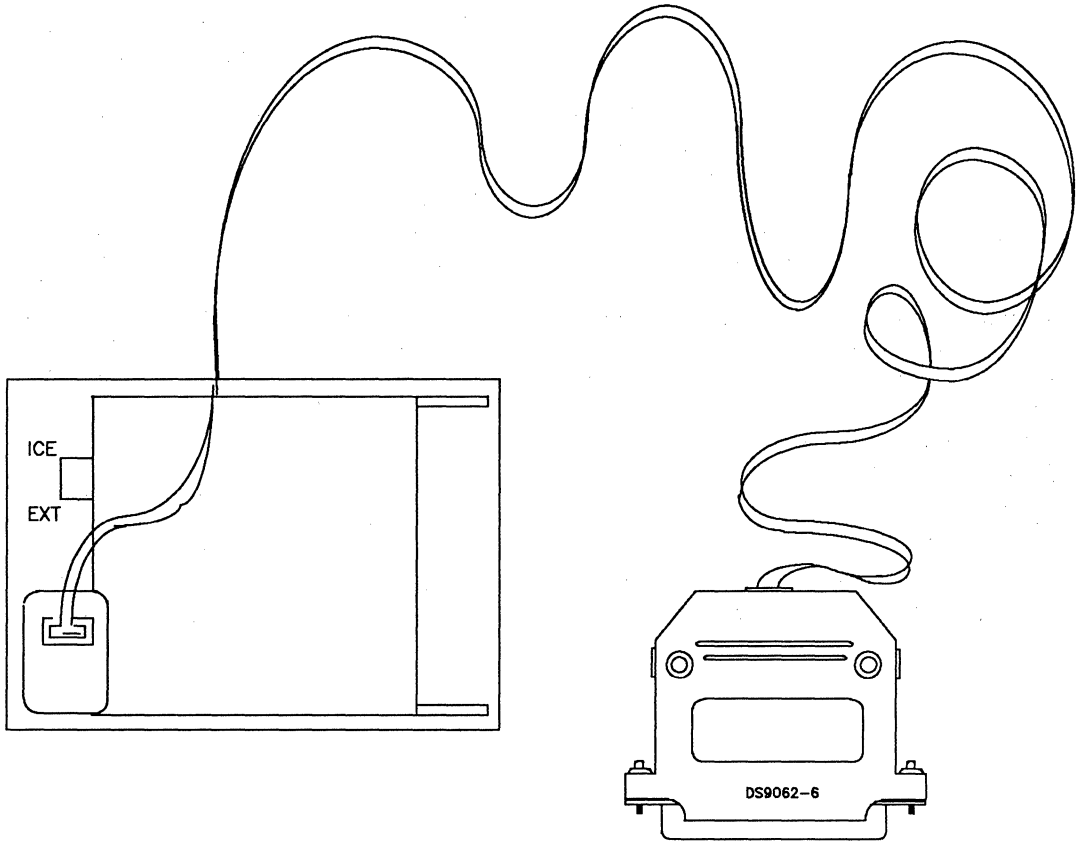
- Low-cost real-time in-circuit emulation system for DS5000
- Supports memory examine/change, register examine/change, breakpoints, single-step operation
- Based on IBM-PC or compatible
- Unique, multi-windowed, dynamic display provides user-friendly interface
- Source code window supports symbolic program listing
- Register window provides easy access to Special Function and Data registers
- Symbolic data access by type of symbol
- Flowgraph window provides either a histograph or flowchart during program execution.
- On-line help facility
- Provides direct debugging support for programs written in Archimedes C-51

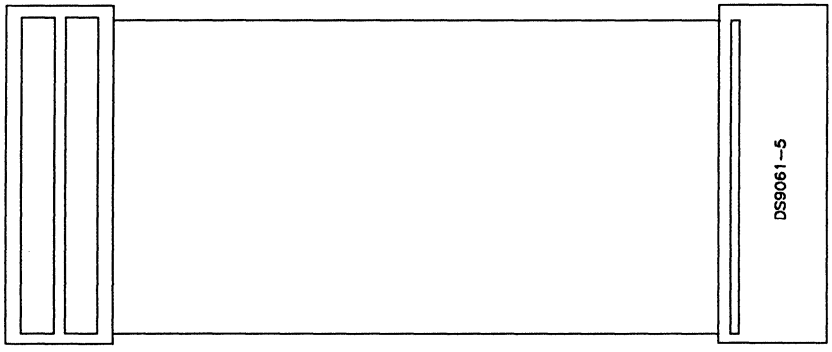
DESCRIPTION

The DS5000DK supports symbolic real-time development of software for the DS5000 Soft Microcontroller from an IBM PC. It features a dynamic, multi-windowed user interface which can shorten development times for DS5000 applications. The multiple windows allow the engineer to view the entire dynamic state of the Soft Microcontroller at a glance. Both assembly language as well as "C" language development are supported. The DS5000DK runs on any IBM PC or compatible.

The DS5000DK is supplied with a compact in-circuit emulation hardware module which connects to the IBM PC via a COM port. A 40-pin plug is used for insertion into the DS5000 socket in the user's application (or target) system. No specialized hardware is required on the PC bus.

DS5000DK DEVELOPMENT KIT: EMULATION MODULE FIGURE 1





Software diskettes are supplied which contain the CYS5000™ software package (which includes a cross assembler) and the ICE5000™ control software.

The DS5000DK not only supports the 8051 compatible features of the DS5000, but also the unique features of the DS5000. These include the dynamic partitioning of the program and data memory space, the power fail interrupt and watchdog timer for crashproof operation, and encryption operation for software security.

The ICE5000 control program with its dynamic user interface provides a unique and easy access to all DS5000 resources. Multiple windows are used to view the activities in Program space, Data Register space, Data RAM space, Bit space, and Special Function Register space. All special bits and registers are automatically labeled when you access them.

The DS5000DK supports development of programs written in C that utilize the C compiler from Archimedes Software, Inc., of San Francisco, CA.

The DS5000DK is being sold by Dallas Semiconductor through a special arrangement with Cybernetic Microsystems, San Gregorio, CA. ICE5000 and CYS8051 are registered trademarks of Cybernetic Microsystems.

SYSTEM REQUIREMENTS

The development kit requires an IBM PC or compatible with DOS 2.0 or later and at least 128K bytes of memory. In addition an RS232 port must be available which is configured as COM1 (03F8H, IRQ4) or COM2 (02F8H, IRQ3). Displays which are supported include monochrome, color graphics, or enhanced graphics (Mode 3).

Power (+5V) on the V_{CC} pin, system ground on GND, and a system clock or crystal on XTAL1 and XTAL2 must be supplied to the emulation module from the target system via the appropriate pins on the Target Cable (see below).

DS5000DK HARDWARE

The development kit hardware consists of the components which are depicted in Figure 1, and which are described below:

Name	Description
RS232 Connector	Adaptor with cable. Adaptor provides DB25 female connector for connection to an RS232C IBM PC COM port on one side and RJ11 female on the other side. Cable carries RS232 signals required by the development kit with two male RJ11 jacks on either end.
Emulation Module	Real-time emulation hardware module. Provides RJ11 female for RS232 signal connection, and 40-pin PC edge connector for connection to target cable.
Target Cable	40-pin adaptor cable which connects the 40-pin edge connector on the RS232 Fixture to the target system microcontroller socket.

The DS5000DK hardware provides all of the necessary control circuitry to facilitate memory examine/change, single-step/multi-step capability, and breakpoint detection. In addition, real-time in-circuit emulation of the application program in the target system is supported with no wait states.

CYS8051 SOFTWARE

The CYS8051 software package is a set of programs that runs on an IBM PC that are used for software development for the DS5000 or for any microcontroller in the 8051 family. The package consists of a number of different programs and utilities which support assembly language program development for these microcontrollers.

The main part of the package is the symbolic macro assembler. It accepts source code from an input file, written in the 8051 assembly language, and generates a list file and an Intel format Hex file as output. The assembler supports macros, conditional assemblies, and a number of new directives. The source programs can be written using standard mnemonics. Source programs are written by the user before entering the package, an can be generated by a standard system text editor, such as Sidekick or Wordstar.

The software package also includes a number of utility commands, such as saving a HEX file from internal memory, displaying internal memory, typing a file, and setting various operating parameters. Finally, the software package also includes some commands implemented through DOS. A directory command gives a listing of the current directory, and a general DOS command allows the user to send any command to the operating system.

ICE5000 SOFTWARE

The ICE5000 control software provided with the DS5000DK provides a unique, multi-windowed user interface which allows the user to have a complete view of the internal state of the DS5000 during execution of the application program.

Operation of the DS5000DK begins by connecting the RS232/DB25 connector to COM 1 of an IBM PC or PS system, then plugging the 40-pin connector of the flat cable terminator into an 8051 compatible socket in the target circuit.

Power is then applied to the target circuit and the ICE5000 software is executed in the PC.The system will then display the following command summary menu:

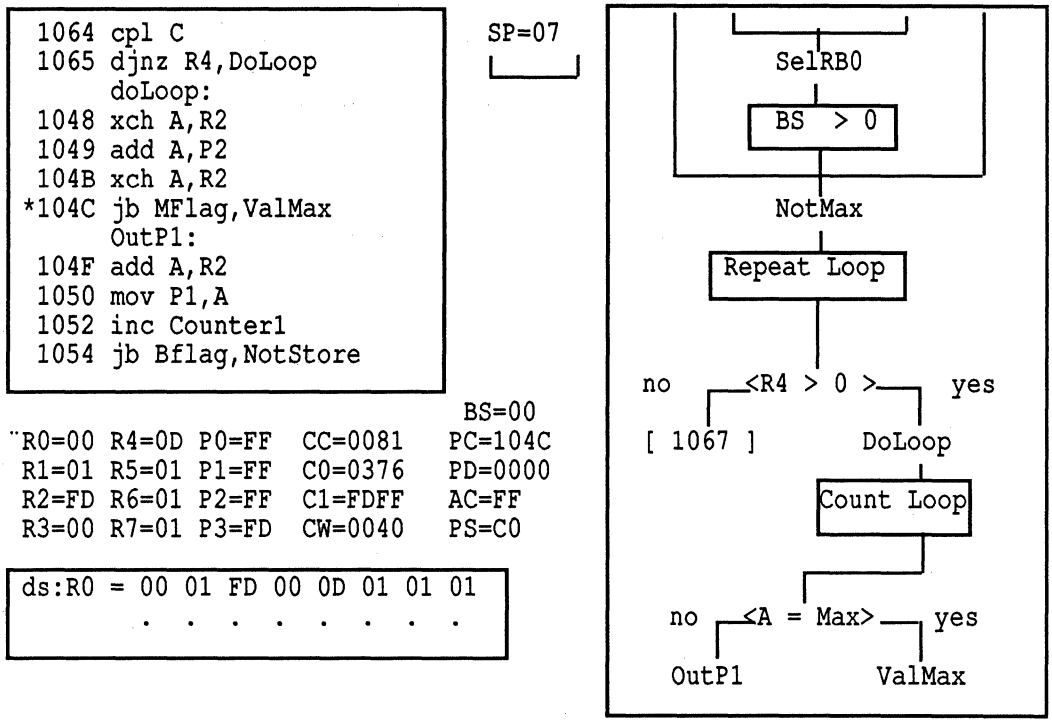
```
ICE5000 (TM) v3.2  Serial #
 Copyright  Cybernetic Micro Systems  1984,85,86,87,88

 User Interface and Control Program ... Ed Klingman
 DS5000 Simulation and Communication .. Dieter Giessler

Ctrl-A       reserved for future use          A Accumulator  AC = Value
Ctrl-B       set Breakpoint address           B Bank switch command
Ctrl-D       Delay (slow down) step rate      D Display all breakpoints
Ctrl-E       Execute (run full speed)         E Enable External access
Ctrl-F       Faster single step rate          F oFfset address for C-51
Ctrl-G       Graph on/off toggle              G Go From... To...
Ctrl-H       Hi-Level Flow Window on/off      H Hex arithmetic (sum/dif)
Ctrl-I       Initialize the microcomputer     I Interrupt Activation
Ctrl-K       Clear Windows                    K Klear active screen
Ctrl-P       Print Flow-Graph                 P PC, PS, Pn = value <CR>
Ctrl-Q       Quit stepping (toggle on/off)    Q Quit debug, ret to DOS
Ctrl-R       Run and generate Histograph      R Register commands
Ctrl-T       Trace Code (toggle on/off)       T Trace number of steps
Ctrl-V       Value Trap (in memory)           V Visible Trace all code
Ctrl-W       reserved command                 W Wait I/O command
Ctrl-X       Xray register while running      ; Pass REMARK to Printer
Scan Symbol Spaces  . for Data  : for Code  % for Bit  ? for Help
F1 = Help  F2 = Color  F3 = Baud  F4 = Save
enter 2 for COM2 or <cr> for COM1:
```

The user must now enter the COM port to which the emulation hardware is attached. Once this is done, the software will prompt the user for a hex file to be loaded as follows:

```
enter HEX file:
```

The user will then enter the name of the Intel Hex file of the application program under development. The ICE5000 software will then read the file and produce its multi-windowed display. If a compatible list file is available, source code debugging is provided. An example of this display is shown in Figure 2:

EXAMPLE DISPLAY FOR SINGLESTEP OPERATION FIGURE 2



A code window shows the source code referenced from the current state of the program counter. Symbolic debugging is facilitated by displaying all symbols and labels from the source code. An asterisk points to the next instruction to be executed from the current state of the machine.

A register window displays the current state of key registers within the 8051 compatible CPU. These include the working registers (R0-R7), port (P0-P3), the two on-chip 16-bit timers (C0-C1), watchdog timer (CW), program counter (PC), data pointer (PD) accumulator (AC), and program status word (PS). Also displayed are the stack pointer (SP) and the currently selected working register bank (BS).

The memory window allows access to program memory, data memory, bit addresses, or special function register either directly or indirectly through pointers. Source code can be patched and variables or registers can be modified through this window.

A flowchart of the application software is generated as it is executed in the flow window. Alternatively, a histograph can be displayed in this window.

Three basic modes of software execution can be initiated by the DS5000DK. These include single step, run, and full-speed execution.

Single-stepping is intiated by depressing the space bar of the PC. The single-step mode shows the results of individual instructions as they are executed. The state of the DS5000 is displayed after each step. Global and local symbols are monitored during single-step exe-

cution, and the flow graph charts the path of the application software. Disassembled source statements are shown in the code window. Auto-stepping (invoked by **Ctrl-Q** or by **T**) steps through multiple program statements at a variable rate.

In run mode, the DS5000DK generates a histograph which is a statistical summary produced by sampling the program counter every "n" cycles. The histograph thereby graphically illustrates where time is spent in program execution. Also in run mode, the "x-ray" register command may be used to sample all of the register contents for examination. An example of the histograph display is shown below:

EXAMPLE DISPLAY FOR RUN MODE OPERATION FIGURE 3

```
 1064 cpl C                  SP=07
 1065 djnz R4,DoLoop
      doLoop:
 1048 xch A,R2
 1049 add A,P2
 104B xch A,R2
*104C jb MFlag,ValMax
      OutP1:
 104F add A,R2
 1050 mov P1,A
 1052 inc Counter1
 1054 jb Bflag,NotStore
                             BS=00
R0=00 R4=0A P0=FF  CC=09F9   PC=104C
R1=08 R5=08 P1=FF  C0=4FEE   PD=0000
R2=FA R6=01 P2=FF  C1=FDFF   AC=FF
R3=00 R7=02 P3=FD  CW=04FC   PS=C0

ds:R0 = 00 08 FA 00 0A 08 01 02
    .  .  .  .  .  .  .  .

Execution stopped, enter command ...
 >
```

```
[0023]»
[    ]
[    ]
[    ]
[1023]»
[    ]
[    ]
[1044]»
[104C]»
[1059]
[1062]
[1065]
[1072]
[107B]»
[    ]
[    ]
[1098]»
[10A8]
Ext Int 0...Serial...0005
Timer 0...PwrFail....
Ext Int 1......Reset
Timer 1......  .....
```

Real time execution of the DS5000 can be initiated via the **Ctrl-E** command. A single breakpoint address can be entered via the **Ctrl-B** command. In execution mode, the application software is executed at full real-time speed until a breakpoint is encountered. The entire state of the machine at the time of the breakpoint can then be examined from the code and register windows.

ELECTRICAL SPECIFICATIONS

Operating Temperature Range	0 to +50 degrees C
System Power Supply Requirements from Target System (DS5000 installed in target system; no load on port pins, PSEN*, ALE)	.+5 @ 100 mA max; 50 mA typical

INTERFACE

Connectors:
25-pin RS232 'D' type to RJ11 jack adaptor
RJ11 on RS232 Fixture
40-pin card edge (0.1" centers) on RS232 Fixture
40-pin edge connector on Target Cable
40-pin DIP plug on Target Cable

Nonvolatile Static RAM

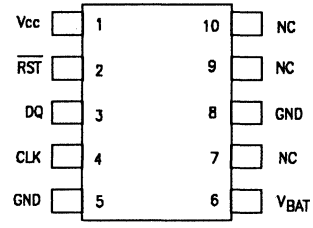
Dallas Semiconductor
SERIAL RAM

DS1200 10-PIN DIP
DS1200S 16-PIN SOIC

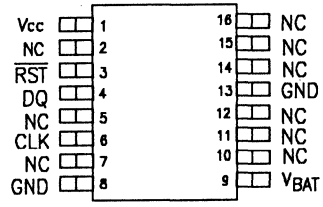
FEATURES

- 1024 bits of read/write memory
- Low data retention current for battery backup applications
- 4 million bits/second data rate
- Single byte or multiple byte data transfer capability
- No restrictions on the number of write cycles
- Low power CMOS circuitry
- Applications include:
  - software authorization
  - computer identification
  - system access control
  - secure personnel areas
  - calibration
  - automatic system setup
  - traveling work record

PIN CONNECTIONS



10-Pin DIP



16-Pin SOIC

PIN NAMES

V_{CC}	- +5 Volts
$\overline{RST}$	- $\overline{RESET}$
DQ	- DATA INPUT/OUTPUT
CLK	- CLOCK
GND	- GROUND
V_{BAT}	- Battery (+)
NC	- No Connection

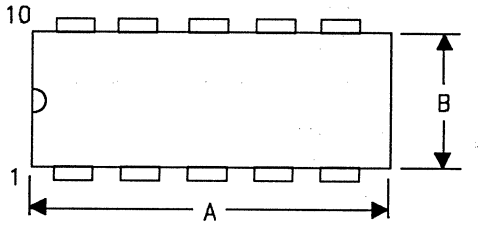
DESCRIPTION

The DS1200 Serial RAM is a miniature read/write memory which can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{RESET}$, and DATA INPUT/OUTPUT.

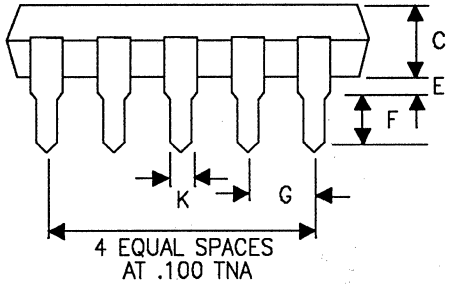
Nonvolatility may be achieved by connecting a battery with a voltage of 2 to 4 volts at the battery input V_{BAT}. A load of 0.5 uA should be used to size the external battery for the required data retention time. If nonvolatility is not required the V_{BAT} pin should be grounded.

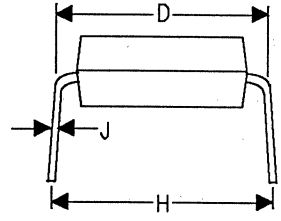
For a complete description of operating conditions, electrical characteristics, bus timing, and signal descriptions other than V_{BAT}, see the DS1201 data sheet.

DS1200
10-Pin DIP

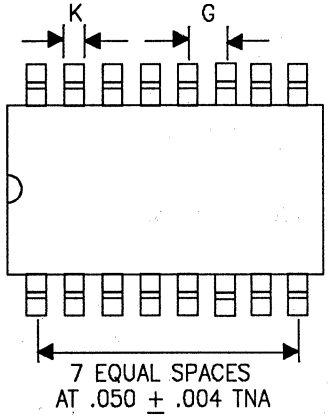


DIM.	INCHES	
	MIN	MAX
A	0.480	0.520
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021

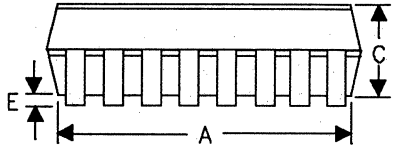


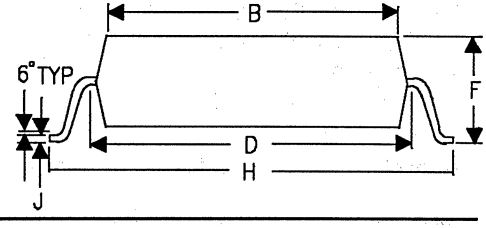


DS1200S
16-Pin SOIC



DIM.	INCHES	
	MIN	MAX
A	0.480	0.520
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021



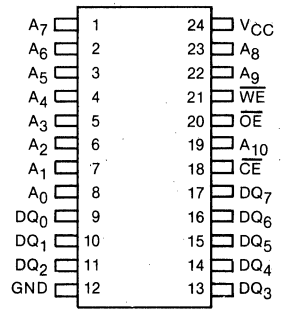


Dallas Semiconductor
16K Nonvolatile SRAM

DS1220AB
DS1220AD

FEATURES
- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 24-pin JEDEC pinout
- Available in either 150 or 200 ns read access time
- Read cycle time equals write cycle time
- Optional 5% and 10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

PIN CONNECTIONS



PIN NAMES
A_0-A_{10}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable

DESCRIPTION
The DS1220AB and DS1220AD are 16,384-bit, fully static, nonvolatile RAMs organized as 2048 words by 8 bits. Each nonvolatile static RAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out of tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 2K x 8 static RAM directly conforming to the popular byte wide 24 pin DIP standard. The DS1220AB also matches the pinout of the 2716 EPROM or the 2816 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1220AB and DS1220AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1220AB and DS1220AD are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1220AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5V. The DS1220AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1220AD and 4.75 volts for the DS1220AB.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1220AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1220AD Power Supply Voltage	V_{CC}	4.50	5.0	5.50	V	
Input Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	
Input Logic 0	V_{IL}	−0.3		+0.8	V	

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10% for DS1220AD)
(0°C to 70°C, V_{CC} = 5V ± 5% for DS1220AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	uA	
I/O Leakage Current	I_{LO}	−5.0		+5.0	uA	
Output Current @ 2.4V	I_{OH}	−1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{DDS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC} − 0.5V	I_{DDS2}		3.0	5.0	mA	
Operating Current	I_{DDO1}			75	mA	
Write Protection Voltage (DS1220AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1220AD)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

($t_A = 25°C$)

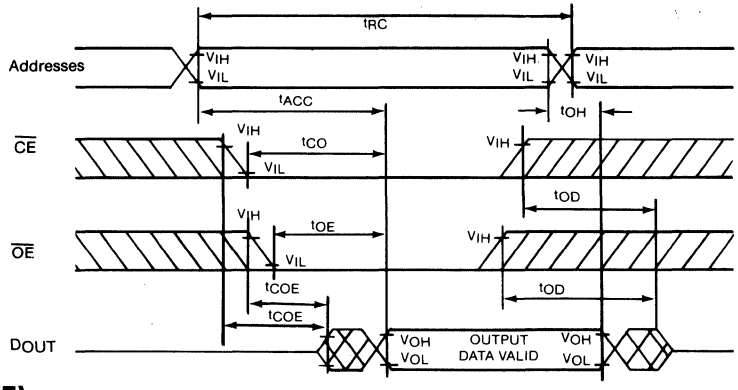
PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

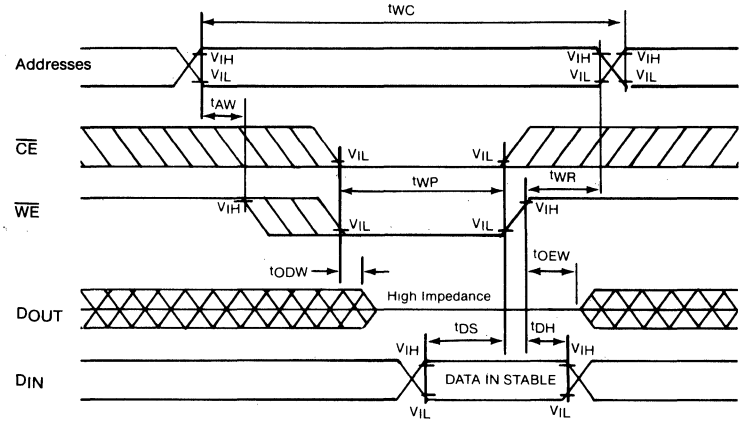
(0°C to 70°C, $V_{CC} = 5.0V \pm 10\%$ for DS1220AD)
(0°C to 70°C, $V_{CC} = 5.0V \pm 5\%$ for DS1220AB)

		DS1220AD-150 DS1220AB-150		DS1220AD-200 DS1220AB-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		70		100	ns	5
Output Hold From Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		170		ns	3
Address Set Up Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		10		ns	
Output High Z From $\overline{WE}$	t_{ODW}		70		80	ns	5
Output Active From $\overline{WE}$	t_{OEW}	10		10		ns	5
Data Setup Time	t_{DS}	60		90		ns	4
Data Hold Time	t_{DH}	20		20		ns	4

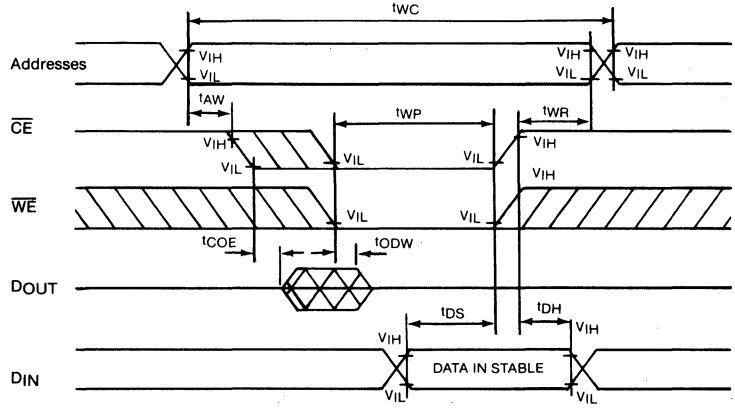
READ CYCLE (1)



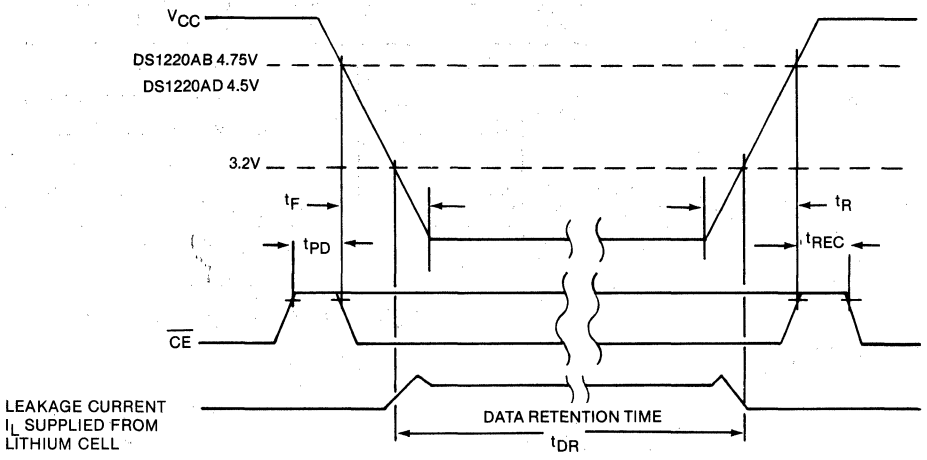
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		us	
t_F	V_{CC} slew from 4.75V to 0V ($\overline{CE}$ at V_{IH})	300		us	DS1220AB
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		us	DS1220AD
t_R	V_{CC} slew from 0V to 4.75V ($\overline{CE}$ at V_{IH})	0		us	DS1220AB
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		us	DS1220AD
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	

($t_A = 25°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1220AB is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

5

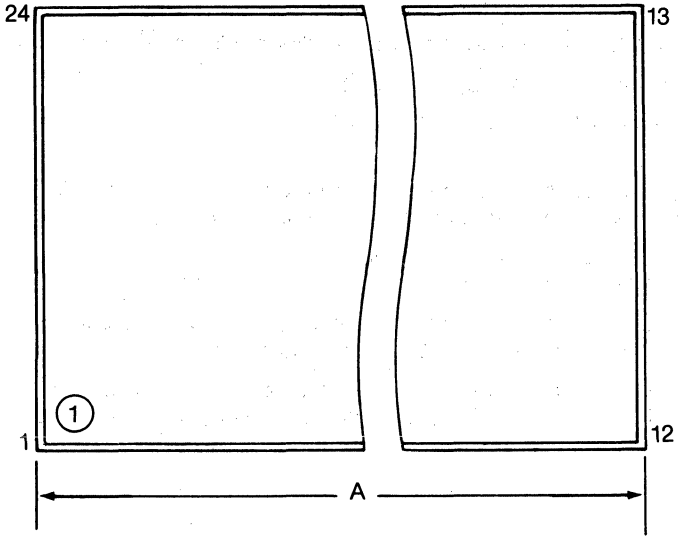
D.C. TEST CONDITIONS

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

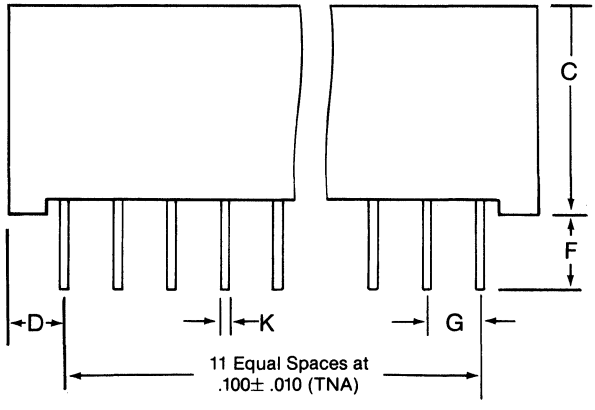
A.C. TEST CONDITIONS

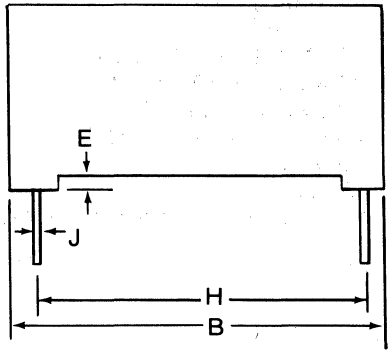
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS1220AD
DS1220AB
Nonvolatile RAM



DIM.	INCHES	
	MIN.	MAX.
A	1.320	1.340
B	.695	.720
C	.395	.410
D	.090	.130
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021



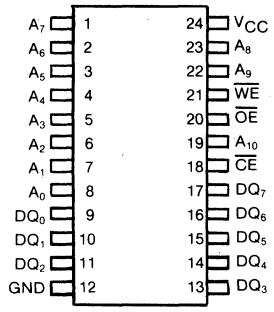


Dallas Semiconductor
16K Nonvolatile SRAM

DS1220Y

FEATURES
- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 2K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 24-pin JEDEC pinout
- Available in either 150 or 200 ns read access time
- Read cycle time equals write cycle time
- Full ± 10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

PIN CONNECTIONS



PIN NAMES
A_0-A_{10} - Address Inputs
$\overline{CE}$ - Chip Enable
GND - Ground
DQ_0-DQ_7 - Data In/Data Out
V_{CC} - Power (+5V)
$\overline{WE}$ - Write Enable
$\overline{OE}$ - Output Enable

5

DESCRIPTION
The DS1220Y is a 16,384 bit fully static nonvolatile RAM organized as 2048 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out of tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 2K × 8 static RAM directly conforming to the popular byte wide 24 pin DIP standard. The DS1220Y also matches the pinout of the 2716 EPROM or the 2816 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1220Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1220Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1220Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	
Input Logic 0	V_{IL}	−0.3		+0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	uA	
I/O Leakage Current	I_{LO}	−5.0		+5.0	uA	
Output Current @ 2.4V	I_{OH}	−1.0	−2.0		mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{DDS1}		3.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC} − 0.5V	I_{DDS2}		2.0	4.0	mA	
Operating Current	I_{DDO1}			75	mA	
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

($t_A = 25°C$)

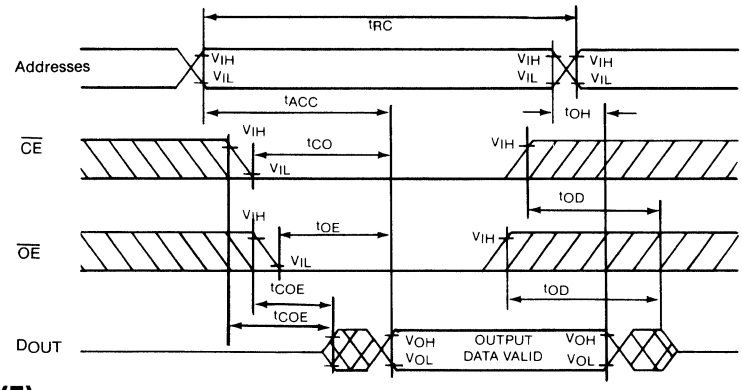
PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

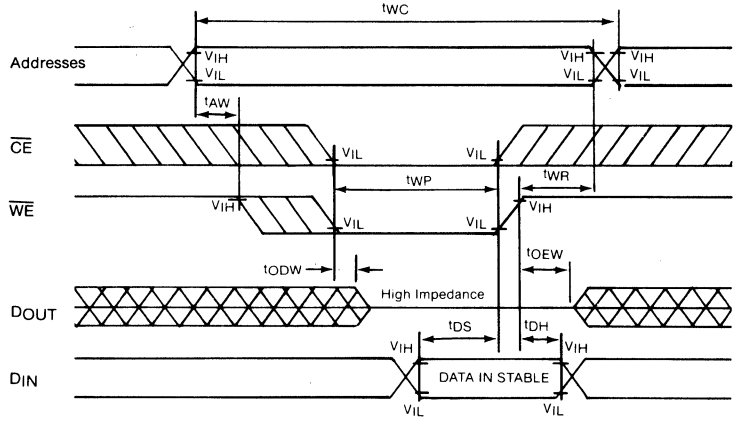
(0°C to 70°C, V_{CC} = 5.0V ± 10%)

		DS1220Y-150		DS1220Y-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		70		100	ns	5
Output Hold From Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		170		ns	3
Address Set Up Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		10		ns	
Output High Z From $\overline{WE}$	t_{ODW}		70		80	ns	5
Output Active From $\overline{WE}$	t_{OEW}	10		10		ns	5
Data Setup Time	t_{DS}	60		90		ns	4
Data Hold Time	t_{DH}	20		20		ns	4

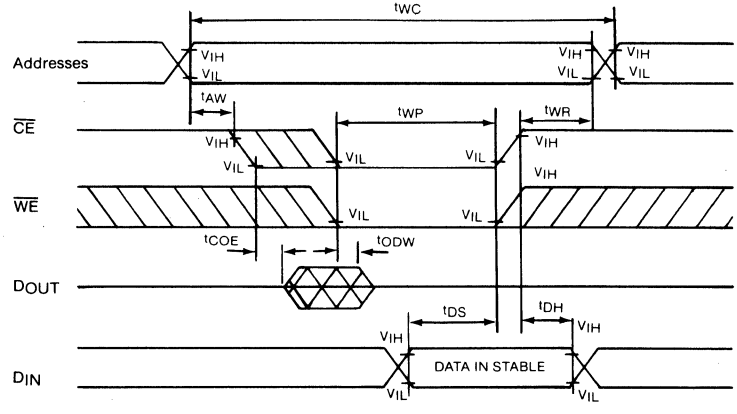
READ CYCLE (1)



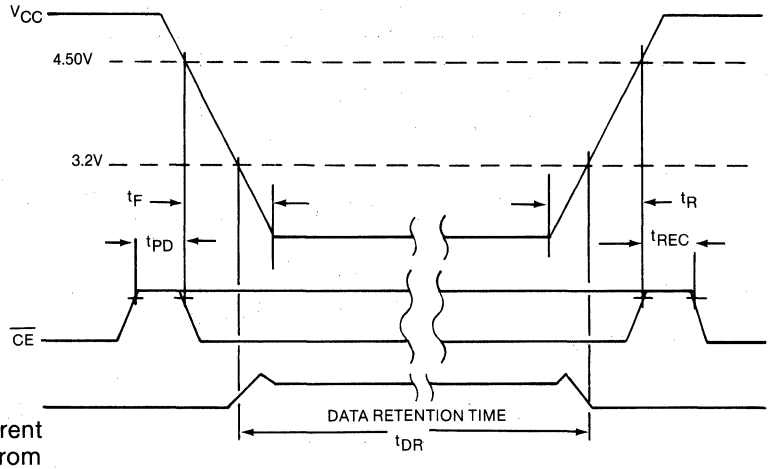
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		μs	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		μs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		μs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up		2	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1220Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

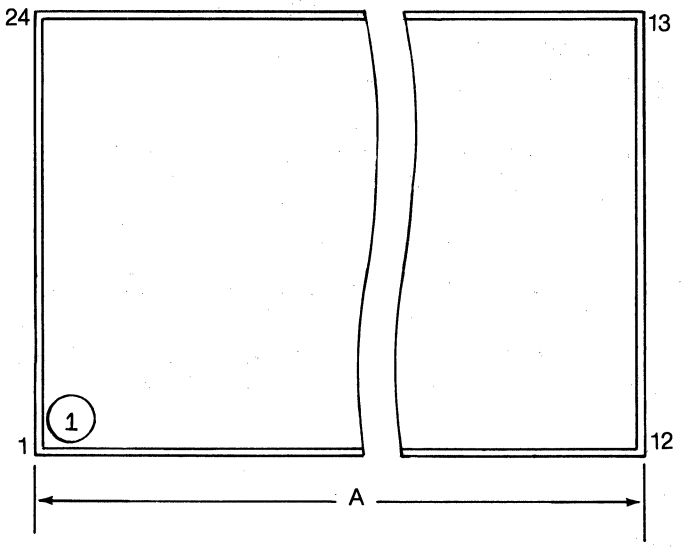
D.C. Test Conditions

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

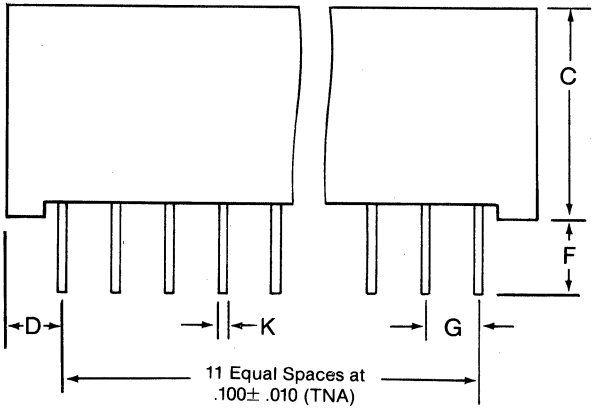
A.C. Test Conditions

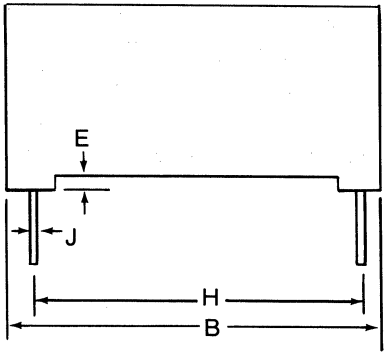
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS1220Y
Nonvolatile RAM



DIM.	INCHES	
	MIN.	MAX.
A	1.320	1.340
B	.695	.720
C	.395	.410
D	.090	.130
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021



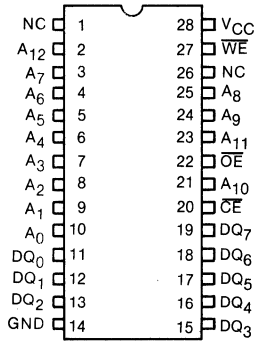


Dallas Semiconductor
64K Nonvolatile SRAM

DS1225AB
DS1225AD

FEATURES
- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in either 150 or 200 ns read access time
- Read cycle time equals write cycle time
- Optional 5% and 10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

PIN CONNECTIONS



PIN NAMES

A_0-A_{12}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
NC	- No Connect

DESCRIPTION
The DS1225AB and DS1225AD are 65,536-bit, fully static, nonvolatile RAMs organized as 8192 words by 8 bits. Each nonvolatile static RAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 8K x 8 static RAM directly conforming to the popular byte wide 28-pin DIP standard. The DS1225AB also matches the pinout of the 2764 EPROM or the 2864 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1225AB and DS1225AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225AB and DS1225AD are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1225AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5V. The DS1225AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1225AD and 4.75 volts for the DS1225AB.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1225AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1225AD Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	
Input Logic 0	V_{IL}	−0.3		+0.8	V	

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10% for DS1225AD)
(0°C to 70°C, V_{CC} = 5V ± 5% for DS1225AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	uA	
I/O Leakage Current	I_{LO}	−1.0		+1.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$ = V_{CC} − 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CC01}			75	mA	10
Write Protection Voltage (DS1225AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1225AD)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

($t_A = 25°C$)

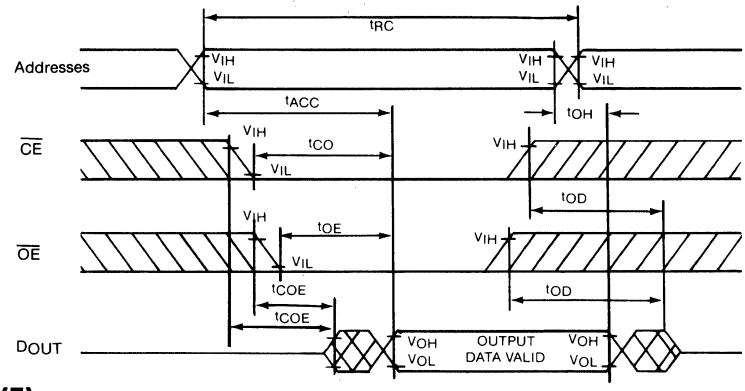
PARAMETER	SYMBOL	TYP.	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

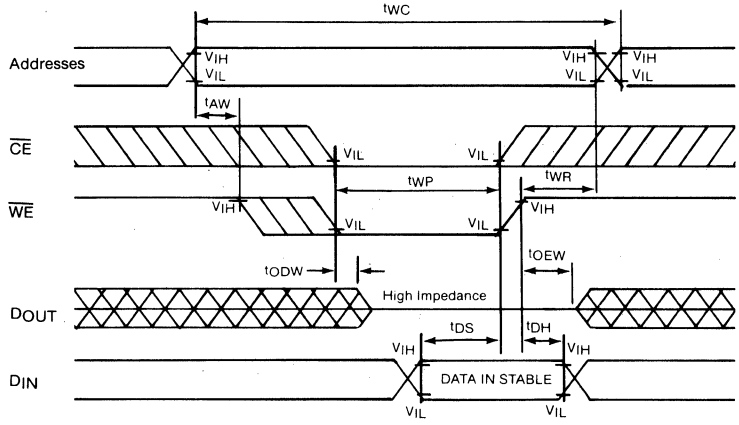
(0°C to 70°C, $V_{CC} = 5.0V \pm 10\%$ for DS1225AD)
(0°C to 70°C, $V_{CC} = 5.0V \pm 5\%$ for DS1225AB)

		DS1225AD-150 DS1225AB-150		DS1225AD-200 DS1225AB-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		70		100	ns	5
Output Hold From Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		150		ns	3
Address Set Up Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		10		ns	
Output High Z From $\overline{WE}$	t_{ODW}		70		80	ns	5
Output Active From $\overline{WE}$	t_{OEW}	10		10		ns	5
Data Setup Time	t_{DS}	60		80		ns	4
Data Hold Time	t_{DH}	20		20		ns	4

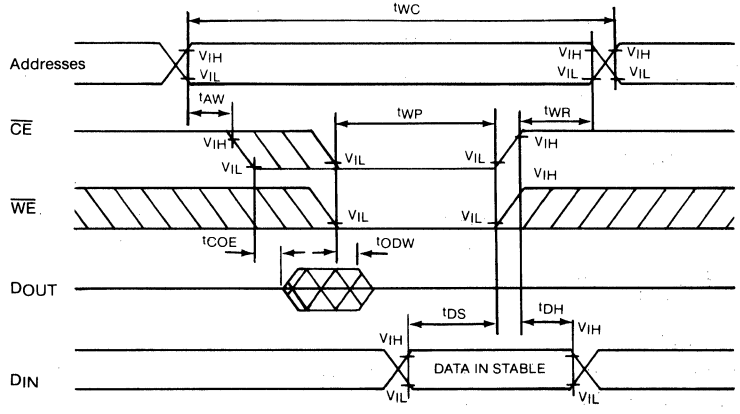
READ CYCLE (1)



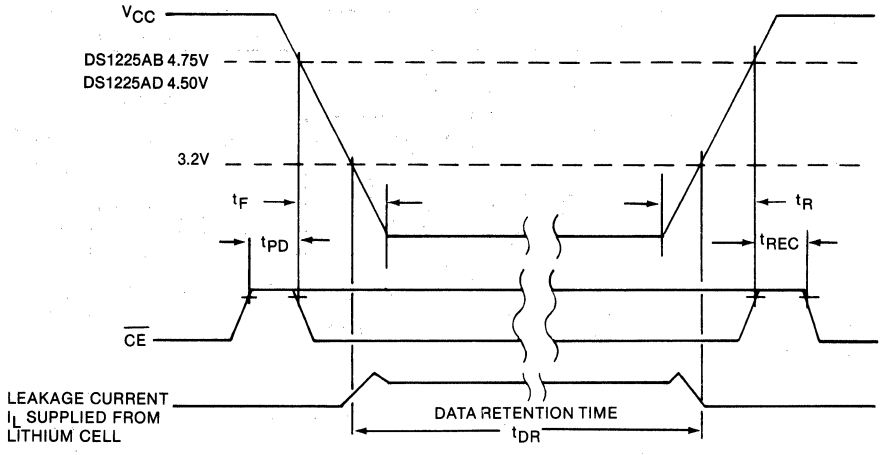
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		us	
t_F	V_{CC} slew from 4.75V to 0V ($\overline{CE}$ at V_{IH})	300		us	DS1225AB
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		us	DS1225AD
t_R	V_{CC} slew from 0V to 4.75V ($\overline{CE}$ at V_{IH})	0		us	DS1225AB
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		us	DS1225AD
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25 °C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1225AB is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. 85 mA for industrial grade part.

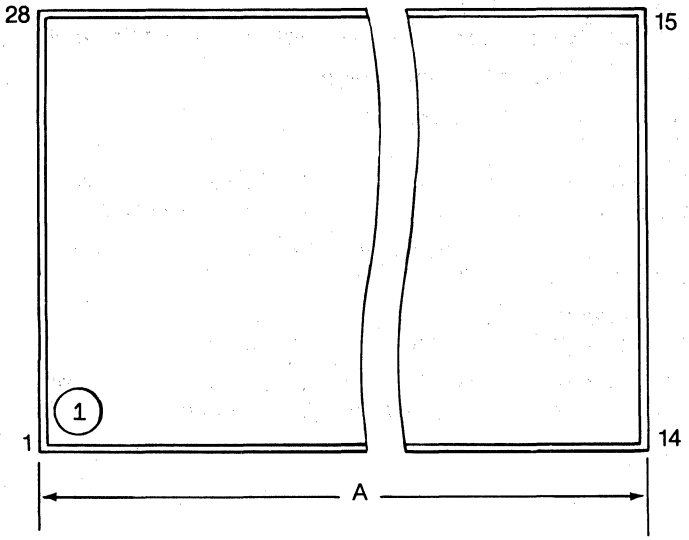
D.C. TEST CONDITIONS

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

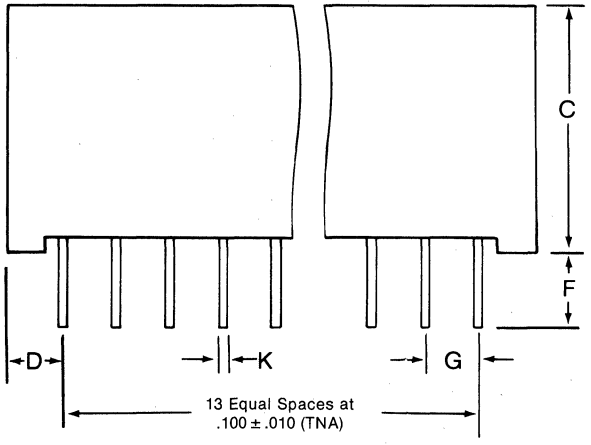
A.C. TEST CONDITIONS

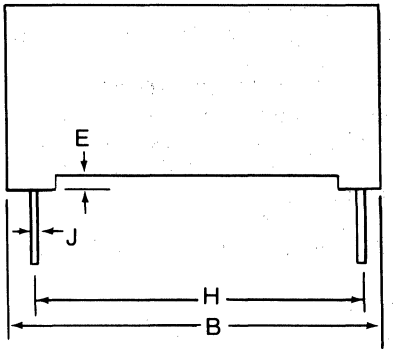
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

DS1225AD
DS1225AB
64K Nonvolatile RAM



DIM.	INCHES	
	MIN.	MAX.
A	1.520	1.540
B	.695	.720
C	.395	.410
D	.090	.120
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021



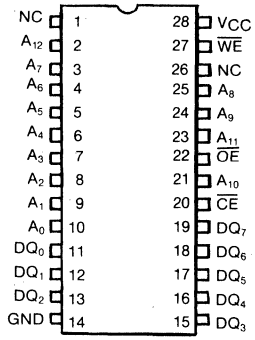


Dallas Semiconductor
64K Nonvolatile SRAM

DS1225Y

FEATURES
- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 8K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in either 150 or 200 ns read access time
- Read cycle time equals write cycle time
- Full ±10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

PIN CONNECTIONS



PIN NAMES

A_0-A_{12}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
NC	- No Connect

DESCRIPTION
The DS1225Y is a 65,536-bit, fully static, nonvolatile RAM organized as 8192 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 8K × 8 static RAM directly conforming to the popular byte wide 28-pin DIP standard. The DS1225Y also matches the pinout of the 2764 EPROM or the 2864 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1225Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1225Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1225Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	
Input Logic 0	V_{IL}	−0.3		+0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	*u*A	
I/O Leakage Current	I_{LO}	−1.0		+1.0	*u*A	
Output Current @2.4V	I_{OH}	−1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}=2.2V$	I_{CCS1}		3.0	7.0	mA	
Standby Current $\overline{CE}=V_{CC}-0.5V$	I_{CCS2}		2.0	4.0	mA	
Operating Current	I_{CC01}			75	mA	10
Write Protection Voltage	V_{TP}		4.25		V	

CAPACITANCE

($t_A = 25°C$)

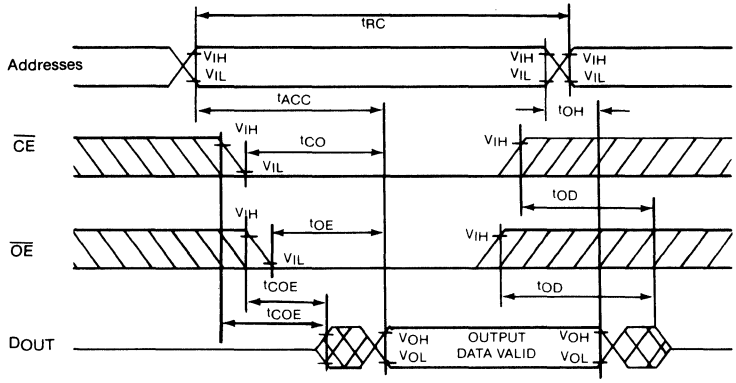
PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

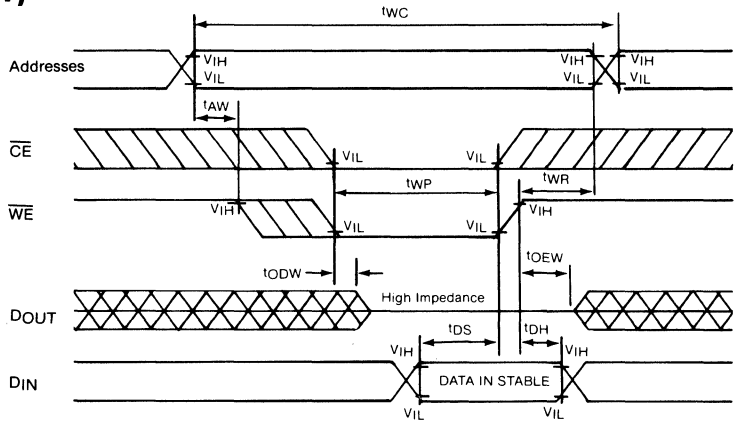
(0 °C to 70 °C, $V_{CC} = 5.0V \pm 10\%$)

		DS1225Y-150		DS1225Y-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		70		100	ns	5
Output Hold From Address Change	t_{OH}	10		10		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		150		ns	3
Address Set Up Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	10		10		ns	
Output High Z From $\overline{WE}$	t_{ODW}		70		80	ns	5
Output Active From $\overline{WE}$	t_{OEW}	10		10		ns	5
Data Setup Time	t_{DS}	60		80		ns	4
Data Hold Time	t_{DH}	20		20		ns	4

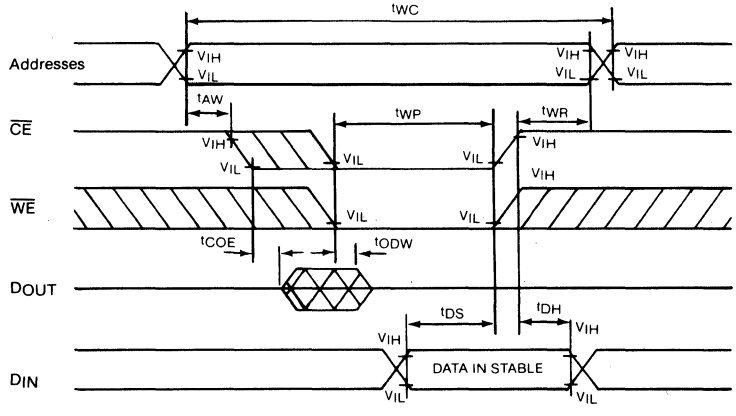
READ CYCLE (1)



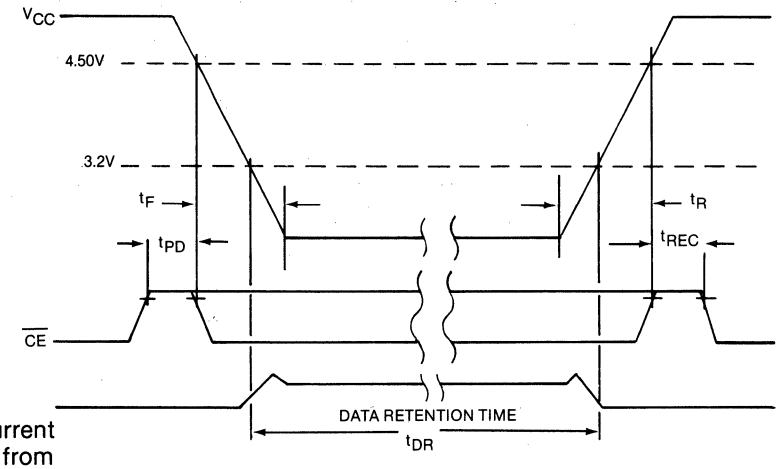
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		μs	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		μs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		μs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up		2	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1225Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. 85 mA for industrial grade part.

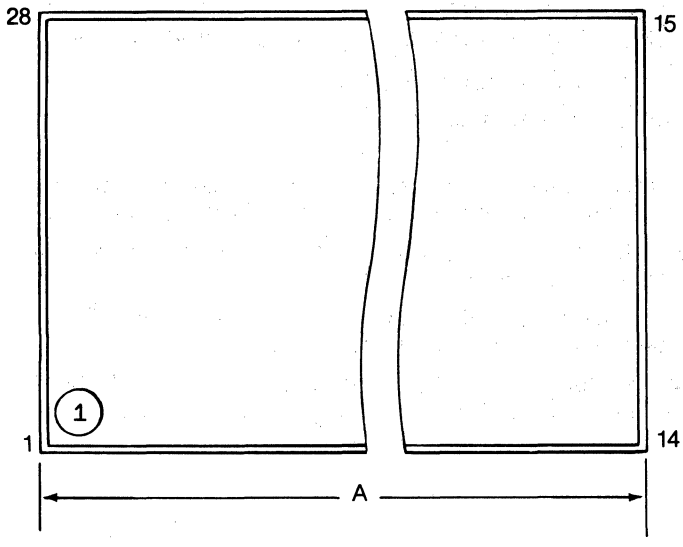
D.C. Test Conditions

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

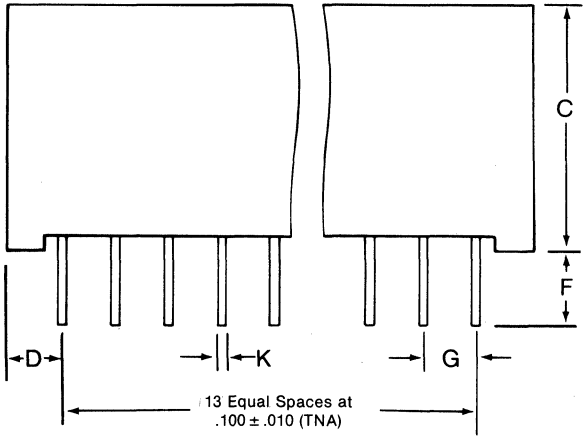
A.C. Test Conditions

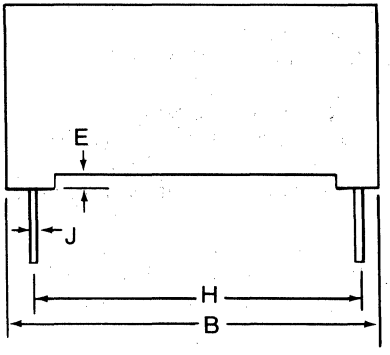
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

DS1225Y
64K Nonvolatile RAM



DIM.	INCHES	
	MIN.	MAX.
A	1.520	1.540
B	.695	.720
C	.395	.410
D	.090	.120
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021



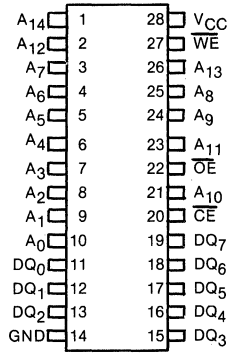


Dallas Semiconductor
256K Nonvolatile SRAM

PRELIMINARY
DS1230Y
DS1230AB

FEATURES
- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 32K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in either 55, 70, or 100 ns read access time
- Read cycle time equals write cycle time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

PIN CONNECTIONS



PIN NAMES
A_0-A_{14} - Address Inputs
$\overline{CE}$ - Chip Enable
GND - Ground
DQ_0-DQ_7 - Data In/Data Out
V_{CC} - Power (+5V)
$\overline{WE}$ - Write Enable
$\overline{OE}$ - Output Enable

DESCRIPTION
The DS1230AB and DS1230Y are 262,144-bit, fully static, nonvolatile RAMs organized as 32,768 words by 8 bits. Each nonvolatile static RAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 32K × 8 static RAM directly conforming to the popular byte wide 28-pin DIP standard. The DS1230AB also matches the pinout of the 28256 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1230AB and DS1230Y execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A_0-A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1230AB and DS1230Y are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1230AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5V. The DS1230Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1230Y and 4.75 volts for the DS1230AB.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1230AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1230Y Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	
Input Logic 0	V_{IL}	−0.3		+0.8	V	

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10% for DS1230Y)
(0°C to 70°C, V_{CC} = 5V ± 5% for DS1230AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	uA	
I/O Leakage Current	I_{LO}	−1.0		+1.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		3.0	5.0	mA	
Standby Current $\overline{CE}$ V_{CC} − 0.5V	I_{CCS2}			15	mA	
Operating Current	I_{CC01}			120	mA	
Write Protection Voltage (DS1230AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1230Y)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

($t_A = 25°C$)

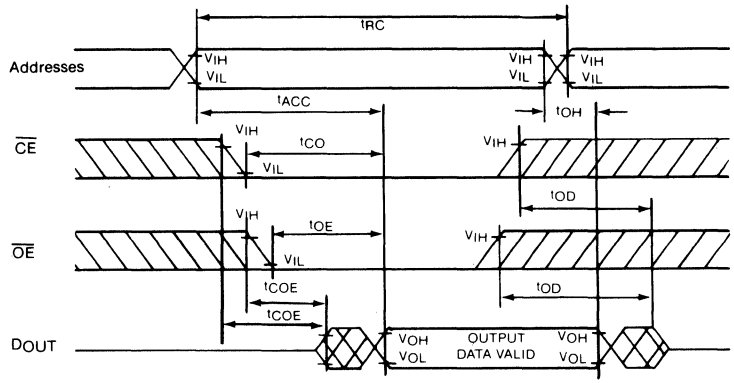
PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

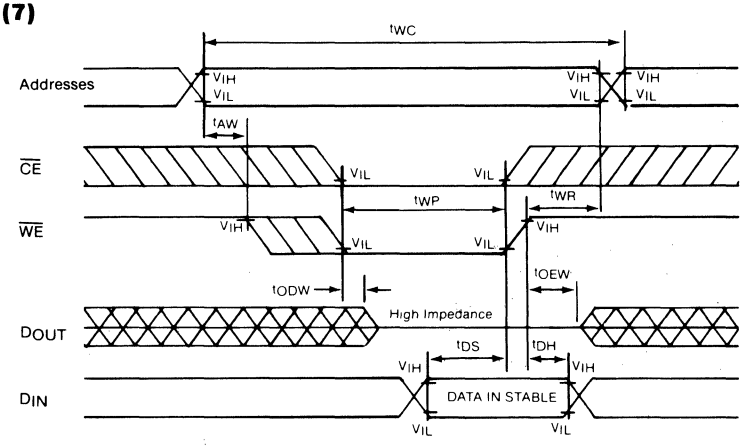
(0°C to 70°C, $V_{CC} = 5.0V \pm 10\%$ for DS1230Y)
(0°C to 70°C, $V_{CC} = 5.0V \pm 5\%$ for DS1230AB)

		DS1230Y-55 DS1230AB-55		DS1230Y-70 DS1230AB-70		DS1230Y-100 DS1230AB-100			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	45		70		100		ns	
Access Time	t_{ACC}		45		70		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		20		30		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		45		70		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	
Output High Z From Deselection	t_{OD}		15		30		35	ns	
Output Hold From Address Change	t_{OH}	10		10		10		ns	
Write Cycle Time	t_{WC}	45		70		100		ns	
Write Pulse Width	t_{WP}	25		55		75		ns	3
Address Set-Up Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	0		0		0		ns	
Output High Z From $\overline{WE}$	t_{ODW}		20		30		35	ns	
Output Active From $\overline{WE}$	t_{OEW}	5		5		5		ns	8
Data Set-Up Time	t_{DS}	40		40		40		ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	0		0		0		ns	4,5

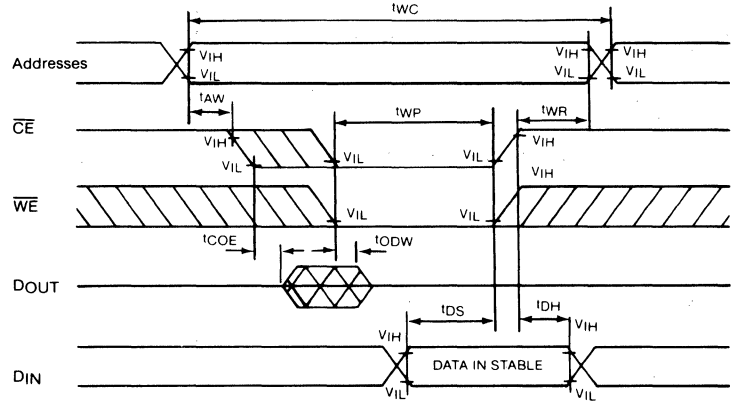
READ CYCLE (1)



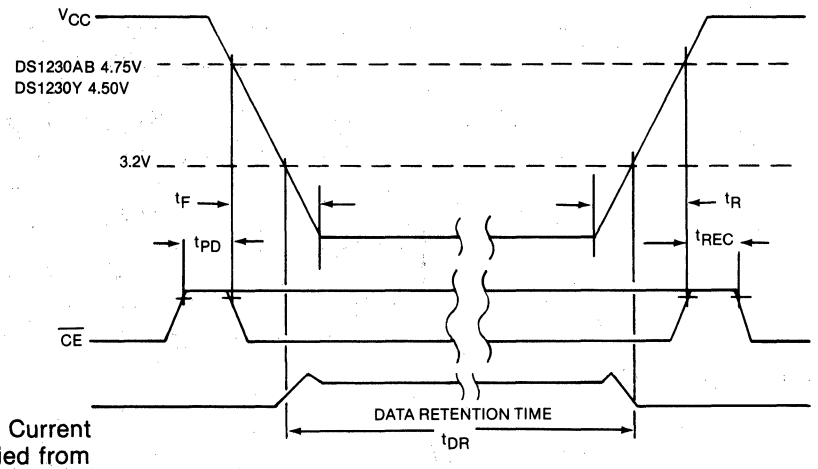
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		*u*s	
t_F	V_{CC} slew from 4.75V to 0V ($\overline{CE}$ at V_{IH})	300		*u*s	DS1230AB
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		*u*s	DS1230Y
t_R	V_{CC} slew from 0V to 4.75V ($\overline{CE}$ at V_{IH})	0		*u*s	DS1230AB
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		*u*s	DS1230Y
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25 °C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1230AB or DS1230Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

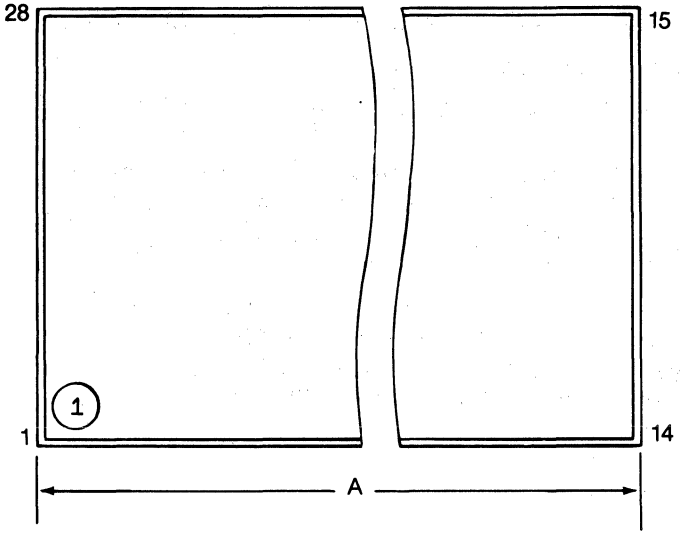
D.C. Test Conditions

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

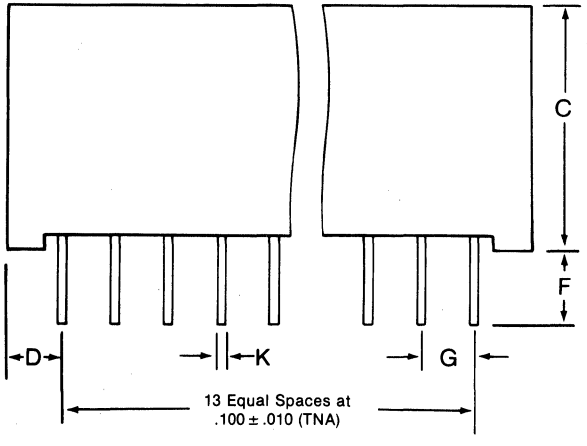
A.C. Test Conditions

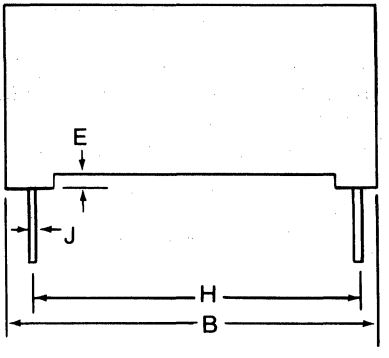
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

DS1230Y
DS1230AB
256K Nonvolatile RAM



DIM.	INCHES	
	MIN.	MAX.
A	1.520	1.540
B	.695	.720
C	.395	.410
D	.090	.120
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





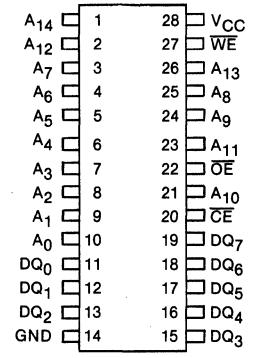
Dallas Semiconductor
256K Nonvolatile SRAM

DS1235Y
DS1235AB

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 32K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS—low power operation
- Standard 28-pin JEDEC pinout
- Available in either 120, 150, or 200 ns read access time
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1235Y)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% operating range (DS1235AB)

PIN CONNECTIONS



PIN NAMES

A_0-A_{14}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable

DESCRIPTION

The DS1235Y is a 262,144-bit, full-static, nonvolatile SRAM organized as 32,768 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 32K × 8 static RAM directly conforming to the popular byte wide 28256 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1235Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A_0-A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$, rather than address access.

WRITE MODE

The DS1235Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{OWD} from its falling edge.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.37 V nominal (V_{CC} greater than 4.75 V and write protect at 4.62 V nominal for DS1235AB). Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1235Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all the outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts (4.75 volts for DS1235AB).

The DS1235Y is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied at a level of greater than 4.25 volts, the lithium energy source is switched on such that energy will be supplied to RAM when V_{CC} is less than approximately 3.0 volts. The lithium energy source can be subsequently turned off by taking V_{CC} to a negative 3 volts for 1 ms.

Battery redundancy is also provided to ensure reliability. The DS1235Y contains two lithium energy cells separated by an internal isolation switch. During battery back-up time the cell with the highest voltage is selected for use. If one battery fails, the other battery will automatically take over. The switch between batteries is transparent to the user.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	
Logic 0	V_{IL}	−0.3		+0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V\pm10\%$ for DS1235Y) (0°C to 70°C, $V_{CC}=5V\pm5\%$ for DS1235AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	uA	
I/O Leakage Current	I_{LO}	−5.0		+5.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}=2.2V$	I_{DDS1}		5.0	10.0	mA	
Standby Current $\overline{CE}=V_{CC}-0.5V$	I_{DDS2}		3.0	5.0	mA	
Operating Current	I_{DD}			85	mA	
Write Protection Voltage (DS1235Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1235AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE ($t_A=25°C$)

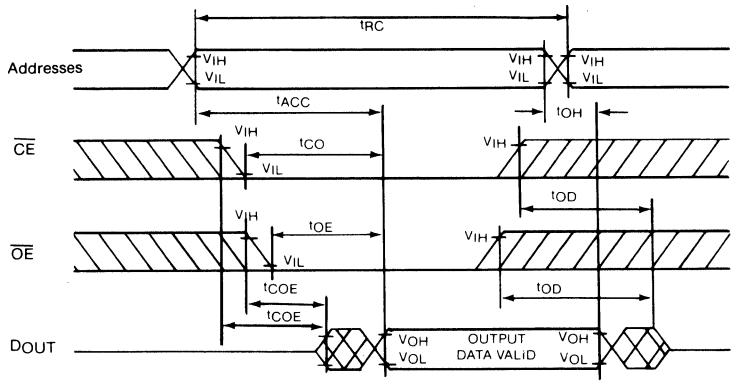
PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

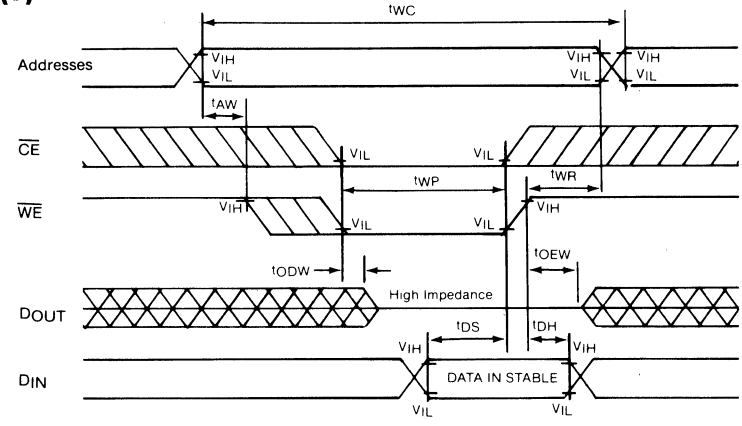
(0 °C to 70 °C, V_{CC} = 5.0V ± 10% for DS1235Y)
(0 °C to 70 °C, V_{CC} = 5.0V ± 5% for DS1235AB)

		DS1235Y-120		DS1235Y-150		DS1235Y-200			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	
Output High Z From Deselection	t_{OD}		40		70		100	ns	
Output Hold From Address Change	t_{OH}	10		10		10		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		170		ns	3
Address Set-Up Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	0		10		10		ns	
Output High Z From $\overline{WE}$	t_{ODW}		40		70		80	ns	
Output Active From $\overline{WE}$	t_{OEW}	5		10		10		ns	8
Data Set-Up Time	t_{DS}	50		60		80		ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	0		0		0		ns	4,5

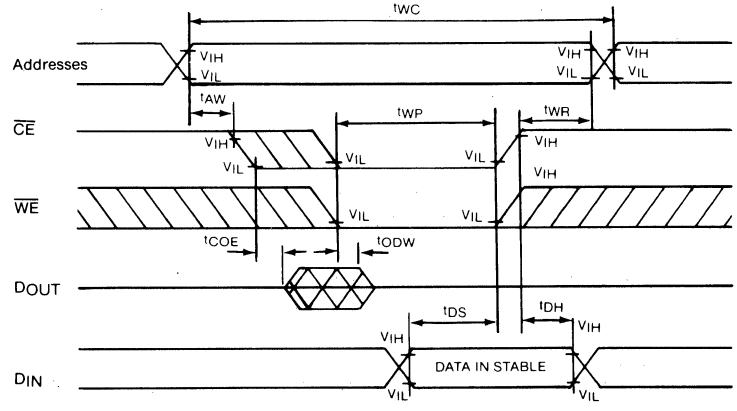
READ CYCLE (1)



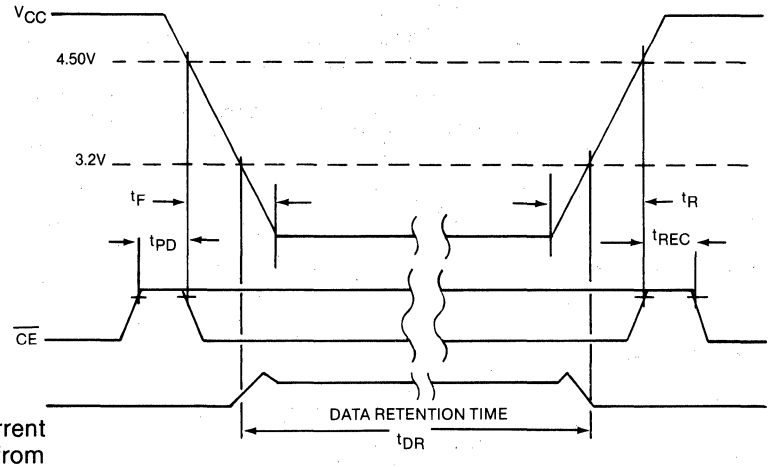
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		μs	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		μs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		μs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up	2	125	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	5		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then t_{DH} = 20ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1235Y has a built-in switch which disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

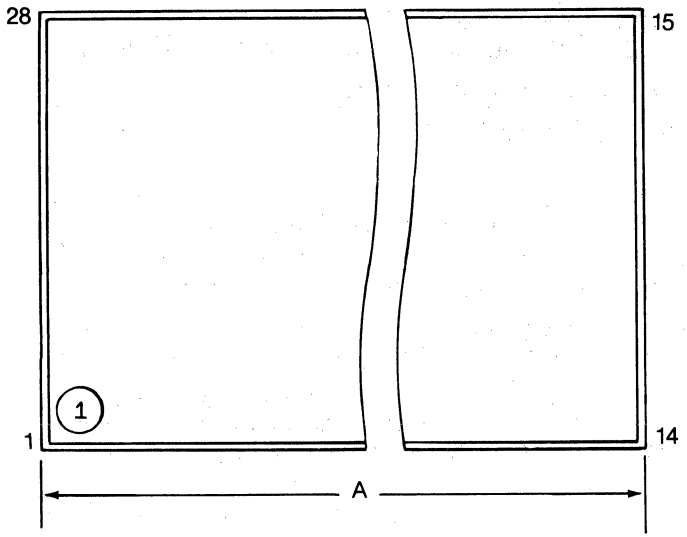
D.C. Test Conditions

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

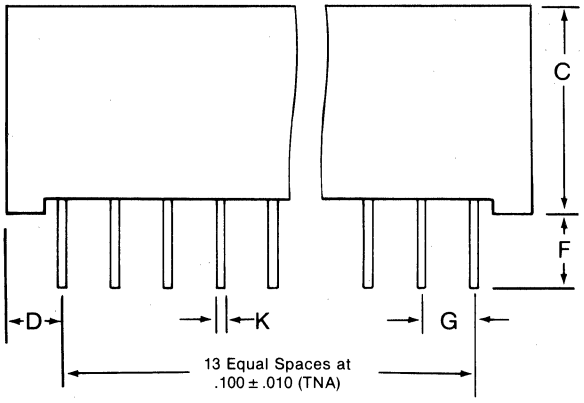
A.C. Test Conditions

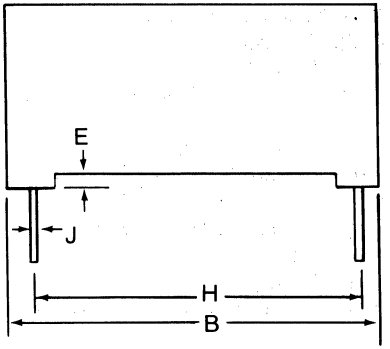
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS1235Y
256K Nonvolatile RAM



DIM.	INCHES	
	MIN.	MAX.
A	1.520	1.540
B	.695	.720
C	.395	.410
D	.090	.120
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





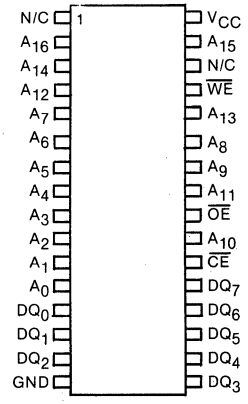
Dallas Semiconductor
1024K Nonvolatile SRAM

PRELIMINARY
DS1245Y
DS1245AB

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 128K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS—low power operation
- Standard 32-pin JEDEC pinout
- Available in either 70, 100 or 120 ns read access time
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1245Y)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% operating range (DS1245AB)

PIN CONNECTIONS



PIN NAMES

A_0-A_{16}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
N/C	- No Connect

DESCRIPTION

The DS1245Y is a 1,048,576-bit full-static, nonvolatile SRAM organized as 131,072 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 128K × 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1245Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A_0-A_{16}) defines which of the 131,072 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that the $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_O for $\overline{CE}$ or t_{OE} for $\overline{OE}$, rather than address access.

WRITE MODE

The DS1245Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{OWD} from its falling edge.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.37 V nominal (V_{CC} greater than 4.75 and write protect at 4.62 V nominal for DS1245AB). Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1245Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all the outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts (4.75 V for DS1245AB).

The DS1245Y is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied at a level of greater than 4.25 volts, the lithium energy source is switched on such that energy will be supplied to RAM when V_{CC} is less than approximately 3.0 volts. The lithium energy source can be subsequently turned off by taking V_{CC} to a negative 3 volts for 1 ms.

Battery redundancy is also provided to ensure reliability. The DS1245Y contains two lithium energy cells separated by an internal isolation switch. During battery back-up time the cell with the highest voltage is selected for use. If one battery fails, the other battery will automatically take over. The switch between batteries is transparent to the user.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	
Logic 0	V_{IL}	−0.3		+0.8	V	

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 5% for DS1245AB)
(0°C to 70°C, V_{CC} = 5V ± 10% for DS1245Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	uA	
I/O Leakage Current	I_{LO}	−5.0		+5.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{DDS1}		3.0	5.0	mA	
Standby Current $\overline{CE}$ = V_{CC} − 0.5V	I_{DDS2}		5.0	10.0	mA	
Operating Current	I_{DD}			85	mA	
Write Protection Voltage (DS1245Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1245AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

($t_A = 25°C$)

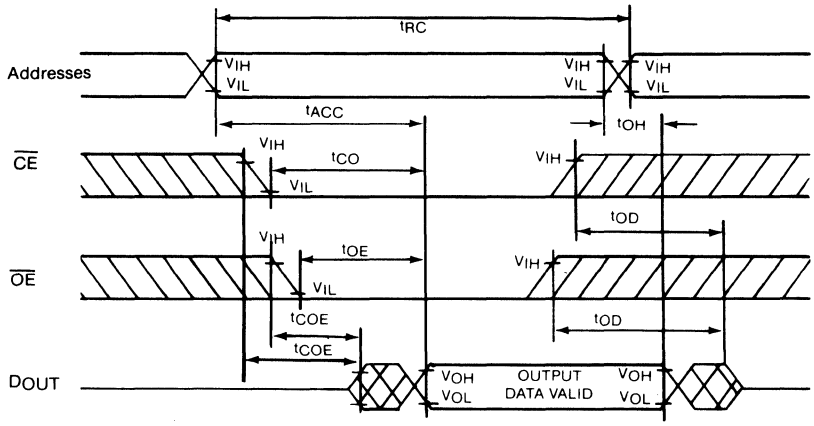
PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

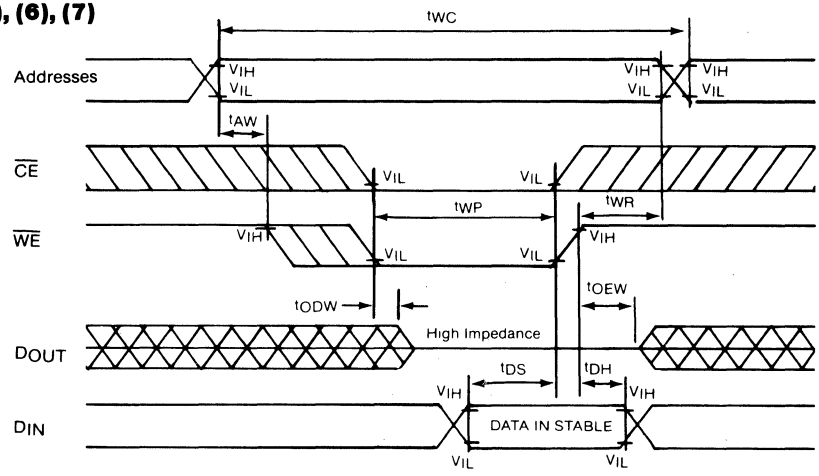
(0°C to 70°C, $V_{CC} = 5V \pm 5\%$ for DS1245AB)
(0°C to 70°C, $V_{CC} = 5V \pm 10\%$ for DS1245Y)

		DS1245Y-70		DS1245Y-100		DS1245Y-120			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70		100		120		ns	
Access Time	t_{CO}		70		100		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		20		50		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70		100		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	
Output High Z From Deselection	t_{OD}		20		35		40	ns	
Output Hold From Address Change	t_{OH}	10		10		10		ns	
Write Cycle Time	t_{WC}	70		100		120		ns	
Write Pulse Width	t_{WP}	55		75		90		ns	3
Address Set-Up Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	10		10		10		ns	
Output High Z From $\overline{WE}$	t_{ODW}		30		35		40	ns	
Output Active From $\overline{WE}$	t_{OEW}	5		5		5		ns	8
Data Set-Up Time	t_{DS}	40		40		50		ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	0		0		0		ns	4,5

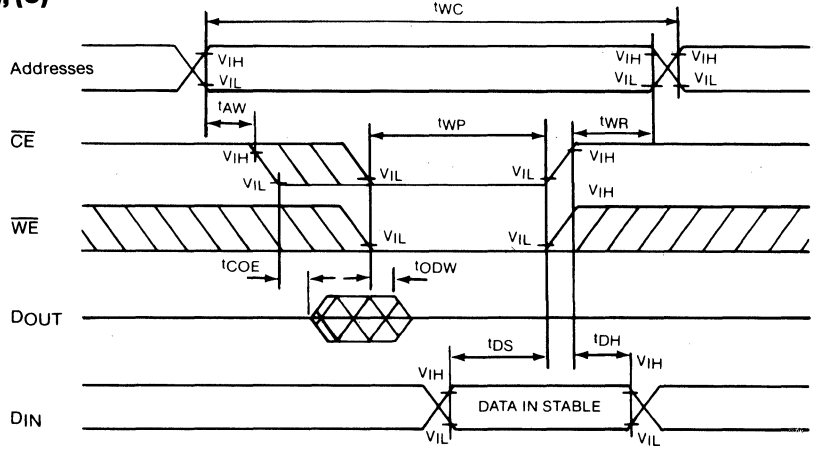
READ CYCLE (1)



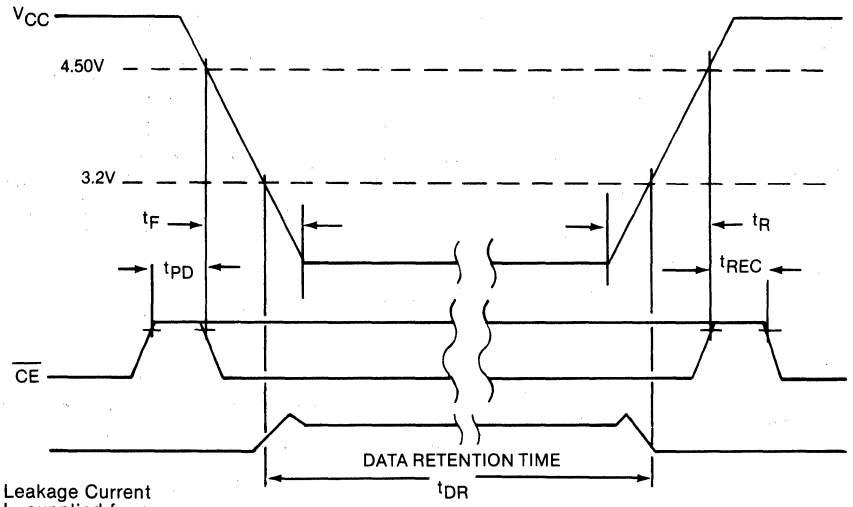
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		*us*	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		*us*	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		*us*	
t_{REC}	$\overline{CE}$ at V_{IH} after Power-Up	2	125	ms	

($t_A = 25\,°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	5		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1245Y has a built-in switch which disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

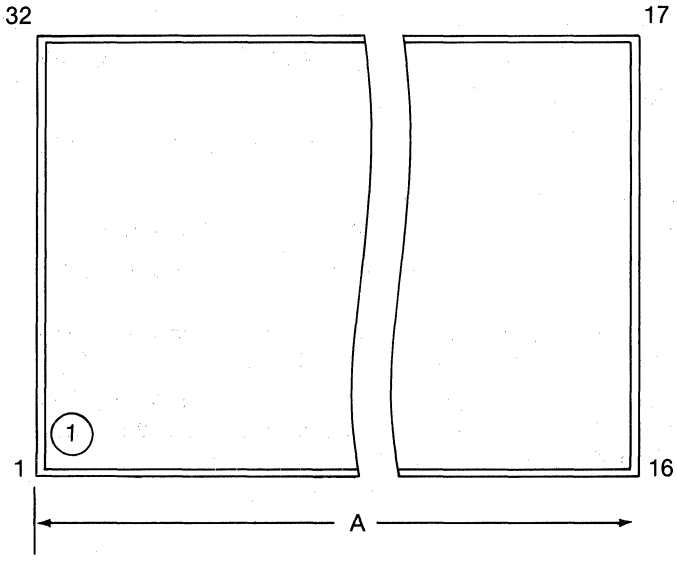
D.C. Test Conditions

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

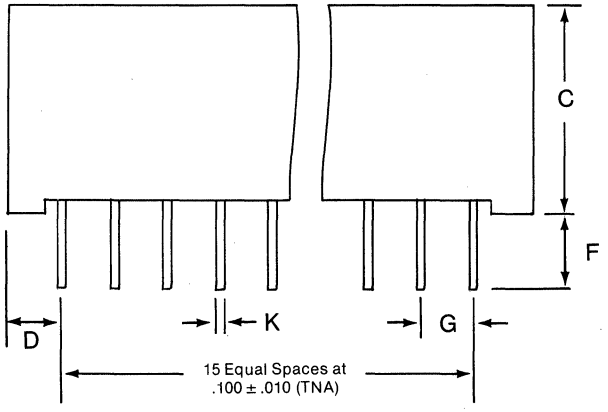
A.C. Test Conditions

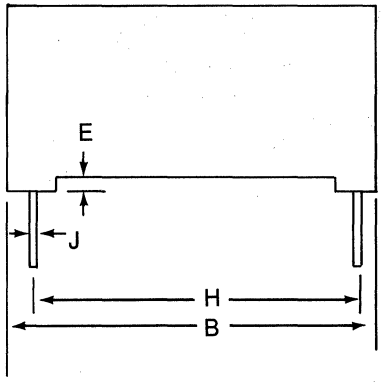
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

DS1245Y
1024K Nonvolatile RAM



DIM.	INCHES	
	MIN.	MAX.
A	1.720	1.740
B	.695	.720
C	.395	.410
D	.090	.120
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





Intelligent Sockets

6

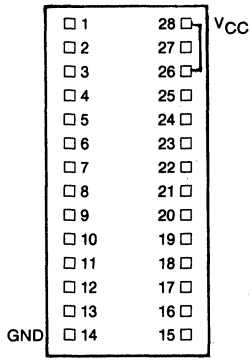
Dallas Semiconductor
SmartSocket 16/64K

DS1213

FEATURES

- Accepts standard 2K × 8 and 8K × 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 2K × 8 to 8K × 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN CONNECTIONS



6

PIN NAMES

All pins pass through except 20, 26, 28.

Pin 20 $\overline{CE}$ - Conditioned Chip Enable
Pin 26 V_{CC} - Switched V_{CC} for 24-pin RAM
Pin 28 V_{CC} - Switched V_{CC} for 28-pin RAM
Pin 14 GND - Ground

DESCRIPTION

The DS1213 is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either 28-pin 8K × 8 or 24-pin 2K × 8 lower-justified JEDEC byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 28, 26, 20 and 14 for RAM control. All other pins are passed straight through to the socket receptacle.

OPERATION

The DS1213 SmartSocket performs five circuit functions required to battery back-up a CMOS memory. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartSocket provides is power fail detection. Power fail detection occurs between 4.75 and 4.5 volts. The DS1213 constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable. The third function accomplishes write protection by holding the chip enable signal to the memory to within 0.2 volts of VCC or battery supply. If the chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal will be passed through to the socket receptacle with a maximum propagation delay of 20 ns. The fourth function the DS1213 performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function which the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to insure reliability. The DS1213 SmartSocket provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two lithium cells contains 35 mAhr capacity, making the total 70 mAhr.

NOTE: As shipped from Dallas Semiconductor, the lithium energy cell cannot be measured from the V_{CC} pin. In order to read the cell potential, apply V_{CC} and then remove power. The cell potential will then be available on Pins 26, 28, and 20.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1,3
Logic 1 PIN 20 L	V_{IH}	2.2		V_{CC}+0.3	V	1,3
Logic 0 PIN 20 L	V_{IL}	-0.3		+0.8	V	1,3

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Current	I_{CC}			5	mA	3, 4, 5
PIN 26 U, PIN 28 U Supply Voltage	V_{CCO}	V_{CC} -0.2			V	3, 8
PIN 26 U, PIN 28 U Supply Current	I_{CCO}			80	mA	3, 8
PIN 20 L $\overline{CE}$ Input Leakage	I_{IL}	-1.0		+1.0	μA	3, 4
PIN 20 U $\overline{CE}$ Output @ 2.4V	I_{OH}	-1.0			mA	2, 3
PIN 20 U $\overline{CE}$ Output @ .4V	I_{OL}			4.0	mA	2, 3

(0°C to 70°C, V_{CC} < 4.5V)

PIN 20 U Output	V_{OHL}	V_{CC} -0.2 V_{BAT} -0.2			V	3
PIN 26 U, PIN 28 U Battery Current	I_{BAT}			1	μA	3, 6
PIN 26 U, PIN 28 U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE ($t_A = 25\,°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance PIN 20 L	C_{IN}	5	pF	3
Output Capacitance PIN 20 U	C_{OUT}	7	pF	3

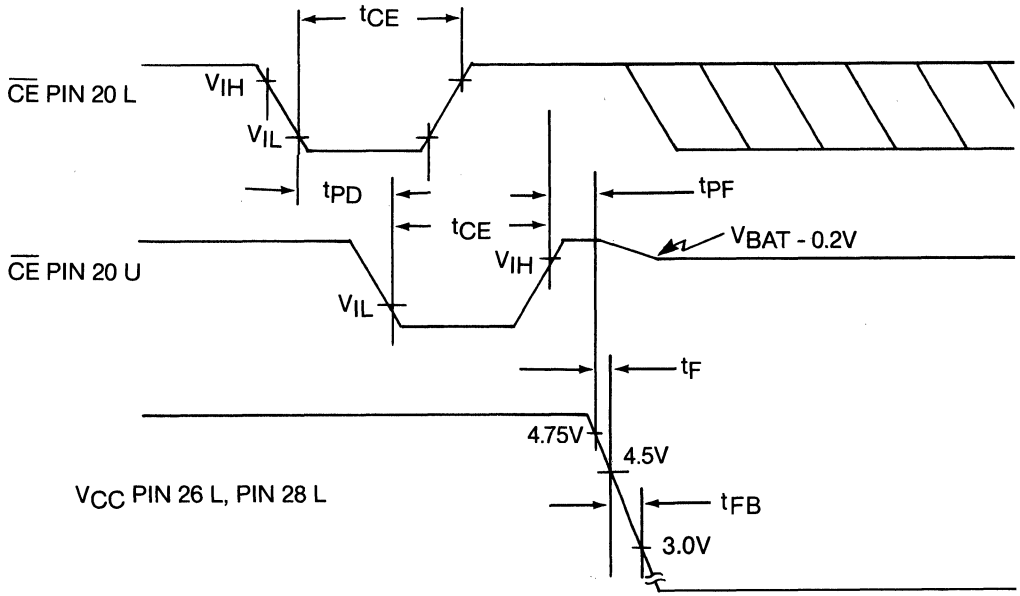
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,9
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

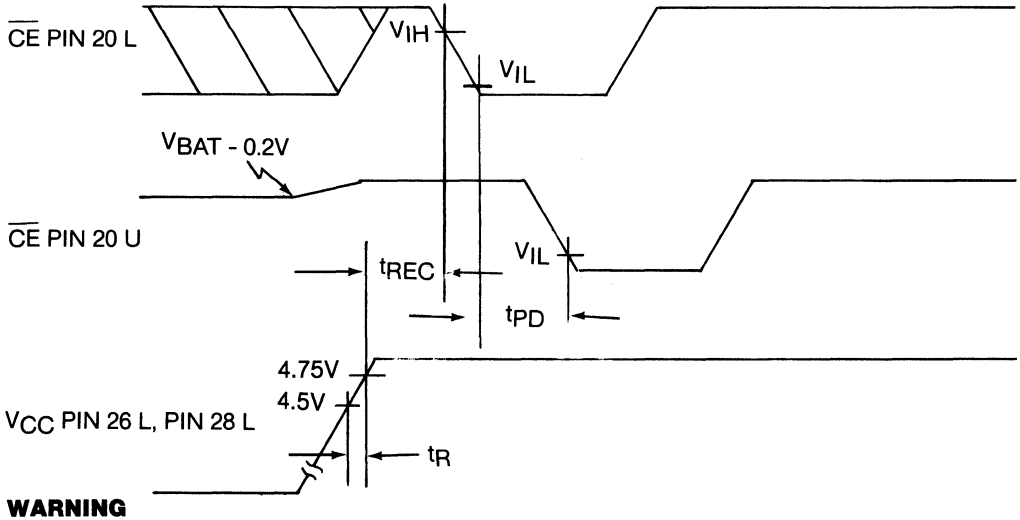
(0° to 70 °C, V_{CC} = 4.75 to 5.5 V)

Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate 4.75 - 4.5 V	t_F	300			*us*	
V_{CC} Slew Rate 4.5 - 3 V	t_{FB}	10			*us*	
V_{CC} Slew Rate 4.5 - 4.75 V	t_R	0			*us*	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	*us*	7

TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP



WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

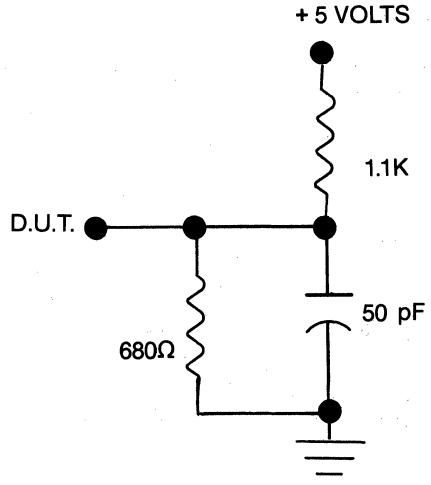
Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

NOTES:

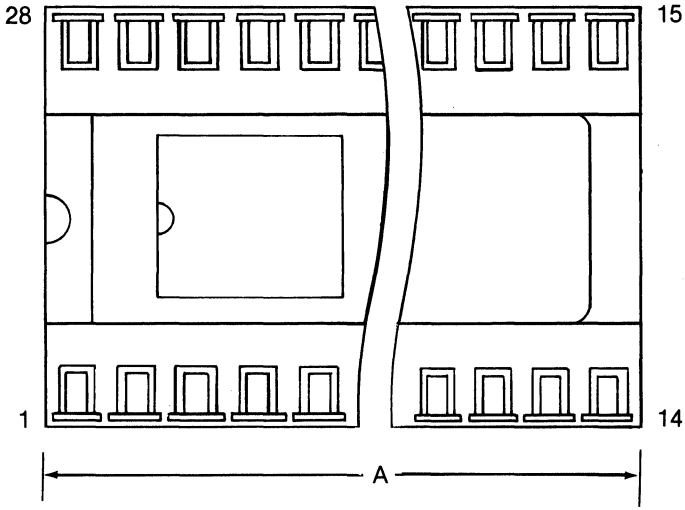
1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26 L may be connected to V_{CC} or left disconnected at the P.C. board.
6. I_{BAT} is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. t_{CE} max. must be met to insure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.

OUTPUT LOAD

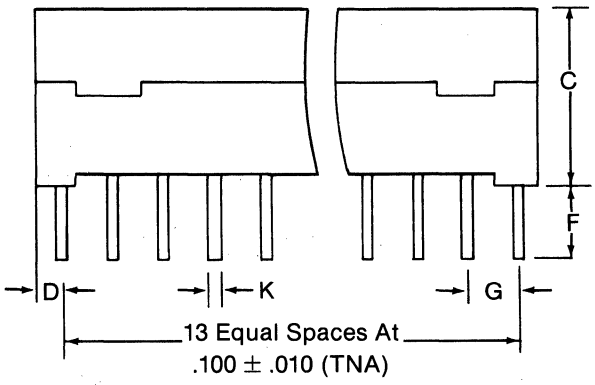
Figure 1

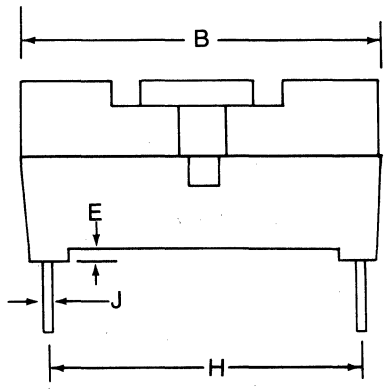


DS1213
SmartSocket



DIM.	INCHES	
	MIN.	MAX.
A	1.390	1.420
B	.695	.720
C	.350	.385
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





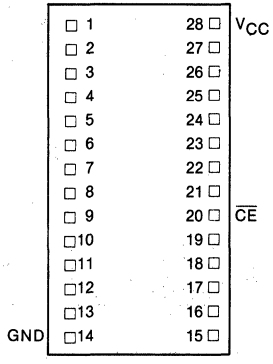
Dallas Semiconductor
SmartSocket 64/256K

DS1213C

FEATURES

- Accepts standard 8K × 8 and 32K × 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 8K × 8 to 32K × 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN CONNECTIONS



PIN DEFINITIONS

All pins pass through except 20, 28.

Pin 20 conditioned Chip Enable

Pin 28 switched V_{CC}

Pin 14 ground

DESCRIPTION

The DS1213C is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K × 8 or a 32K × 8 JEDEC byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 28 and 20 for RAM control. All other pins are passed straight through to the socket receptacle.

See the DS1213 data sheet for technical details.

Dallas Semiconductor
SmartSocket 64/256K/1M

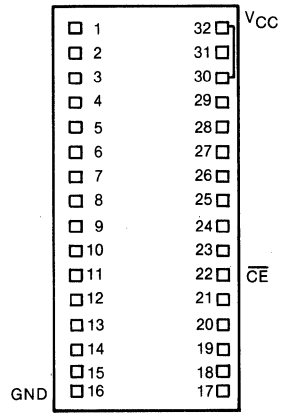
PRELIMINARY

DS1213D

FEATURES

- Accepts standard 8K × 8, 32K × 8, 128K × 8, and 512K × 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 128K × 8 to 512K × 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN CONNECTIONS



PIN DEFINITIONS

All pins pass through except 22, 30 and 32.

Pin 22 $\overline{CE}$ - Conditioned Chip Enable
Pin 32 V_{CC} - Switched V_{CC} for 32-pin RAM
Pin 30 V_{CC} - Switched V_{CC} for 28-pin RAM
Pin 16 GND - Ground

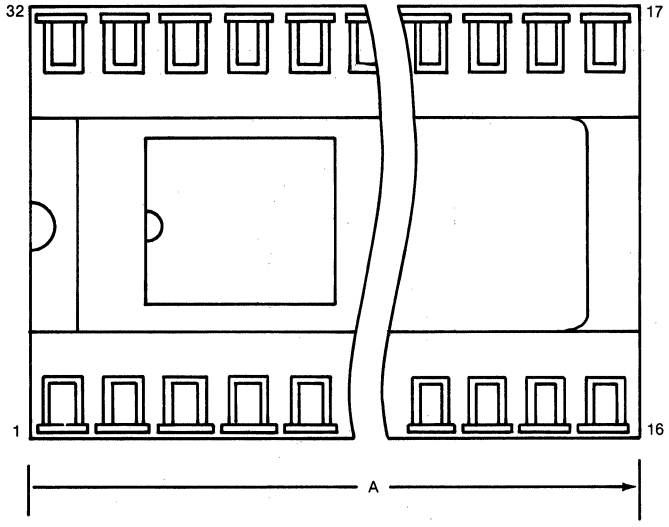
DESCRIPTION

The DS1213D is a 32-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K × 8, 32K × 8, 128K × 8 or 512K × 8 byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket mónitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

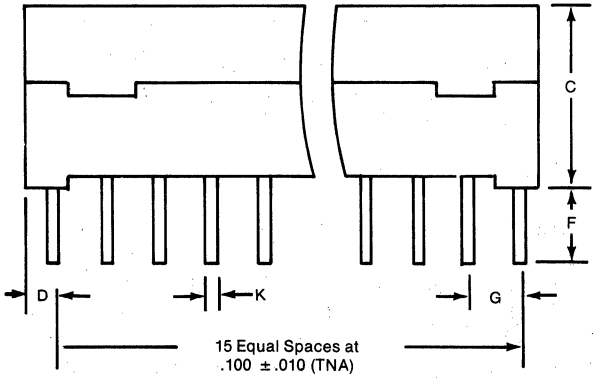
Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 22, 30 and 32 for RAM control. All other pins are passed straight through to the socket receptacle.

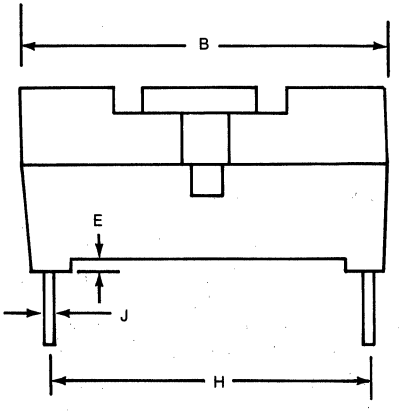
See the DS1213 data sheet for technical details.

DS1213D
SmartSocket



DIM.	INCHES	
	MIN.	MAX.
A	1.590	1.620
B	.695	.720
C	.350	.385
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





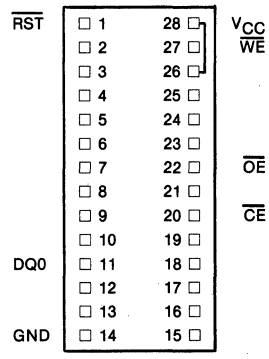
Dallas Semiconductor
SmartWatch/RAM 16/64K

DS1216

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 2K × 8 and 8 K×8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0 °C to 70 °C
- Accuracy is better than ±1 min./month @25 °C

PIN CONNECTIONS



PIN DEFINITIONS

All Pins Pass Through Except
20, 26, 28
Pin 20 Conditioned Chip Enable
Pin 26 Switched V_{CC} for 24 Pin RAM
Pin 28 Switched V_{CC} for 28 Pin RAM
Pin 1 $\overline{RESET}$
Pin 22 Output Enable
Pin 27 Write Enable
Pin 11 Data Input/Output 0
Pin 14 Ground

DESCRIPTION

The DS1216 is a 28-pin 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either 24-pin 2K × 8 or 28-pin 8K × 8 JEDEC Bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM. The SmartWatch monitors V_{CC} for an out of tolerance condition. When such a condition occurs, an internal

lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated RAM take up no more area than the memory alone. The SmartWatch uses pins 28, 27, 26, 22, 20, 11, and 1 for RAM and watch control. All other pins are passed straight through to the socket receptacle.

The SmartWatch provides time keeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

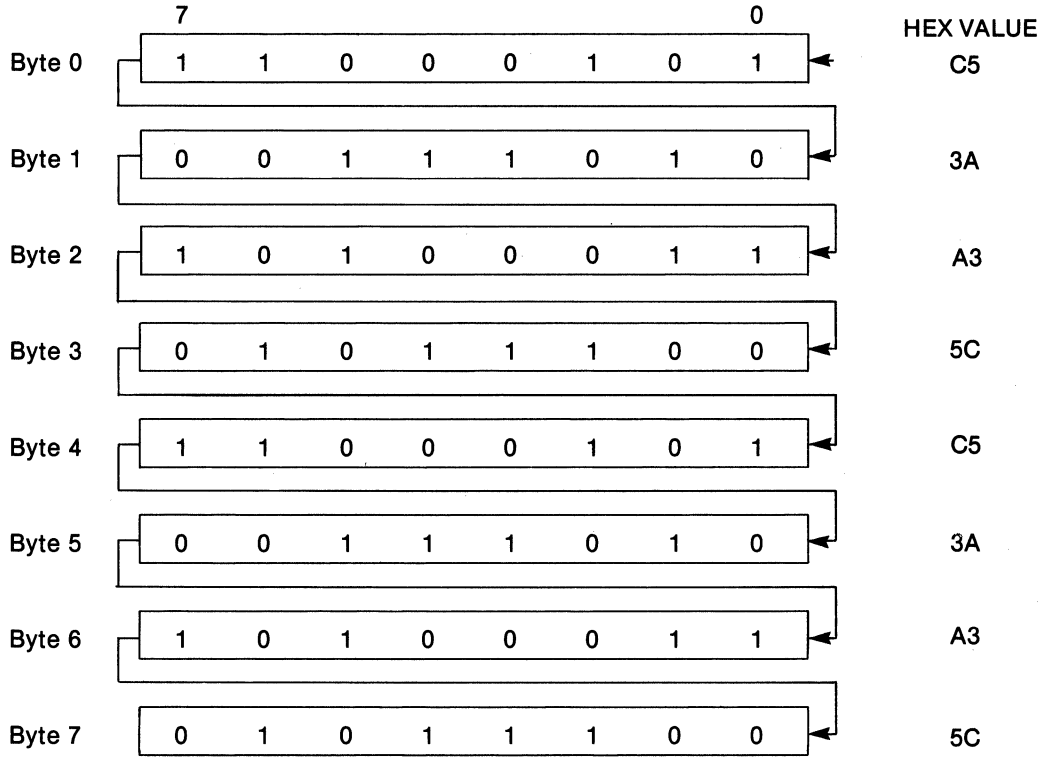
OPERATION

Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64 bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch, memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CE}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch, therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1



NOTE:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in 10^{19}.

NONVOLATILE CONTROLLER OPERATION
The DS1216 SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2 volts. The second function which is involved provides is power fail detection. Power fail detection occurs at typically 4.25 volts. The DS1216 constantly monitors the V_{CC} supply. When V_{CC} goes out of tolerance, a comparator outputs a power fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory within 0.2 volts of V_{CC} or battery. During nominal power supply conditions the memory chip enable signal will track the chip enable signal sent to the socket with a maximum propagation delay of 20 ns.

SMARTWATCH REGISTER INFORMATION
The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64 bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

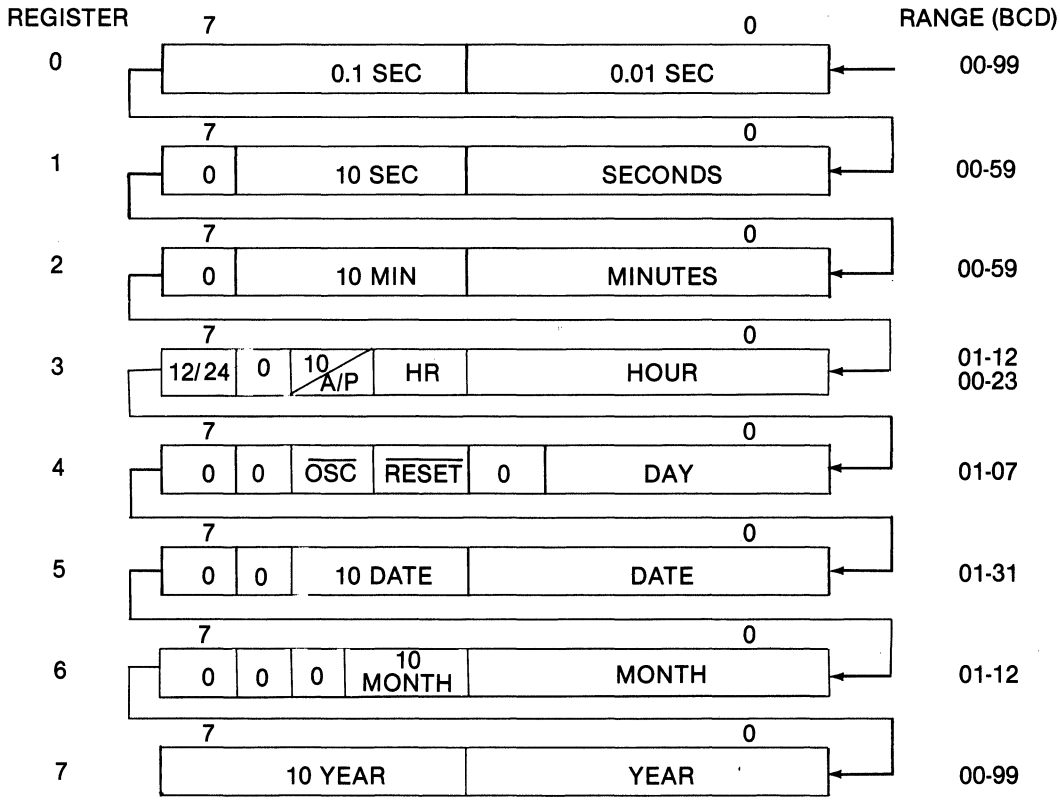
Data contained in the SmartWatch register are in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE
Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12 hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24 hour mode, bit 5 is the second 10-hour bit (20-23 hours).

OSCILLATOR AND RESET BITS
Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logical 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logical 0, a low input on the $\overline{\text{RESET}}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from Dallas Semiconductor set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

ZERO BITS
Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

SMARTWATCH REGISTER DEFINITION Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −1.0V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1, 10
Logic 0	V_{IL}	−0.3		+0.8	V	1, 10

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PIN 26L, PIN 28L Supply	I_{CCI}			5	mA	3, 4, 5
PIN 26U, PIN 28U Supply Voltage	V_{CCO}	$V_{CC}-0.2$			V	3, 8
PIN 26U, PIN 28U Supply Current	I_{CCO}			80	mA	3, 8
Input Leakage	I_{IL}	−1.0		+1.0	μA	4,10, 13
Output @ 2.4V	I_{OH}	−1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

(0°C to 70°, V_{CC} < 4.5V)

PIN 20U Output	V_{OHL}	$V_{CC}-0.2$ $V_{BAT}-0.2$			V	3
PIN 26U, PIN 28U Battery Current	I_{BAT}			1	μA	3, 6
Pin 26U, PIN 28U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

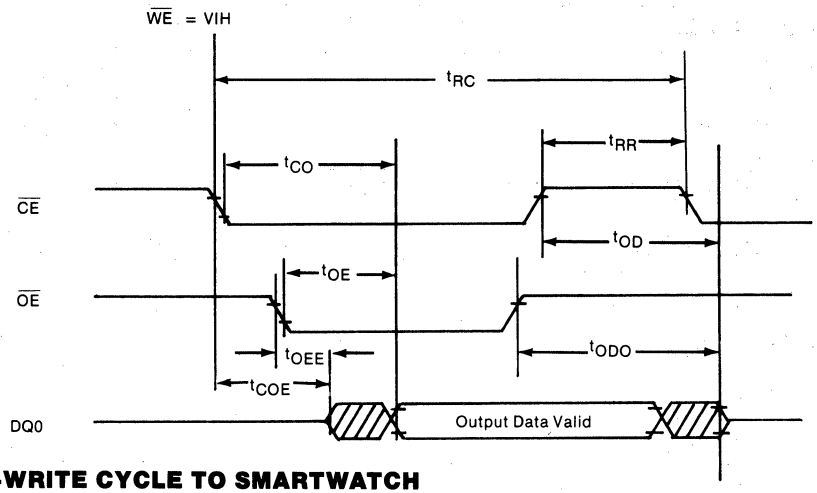
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ To Output High Z	t_{OD}			100	ns	
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	11
Data Set Up Time	t_{DS}	100			ns	12
Data Hold Time	t_{DH}	0			ns	12
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
Reset Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 9
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

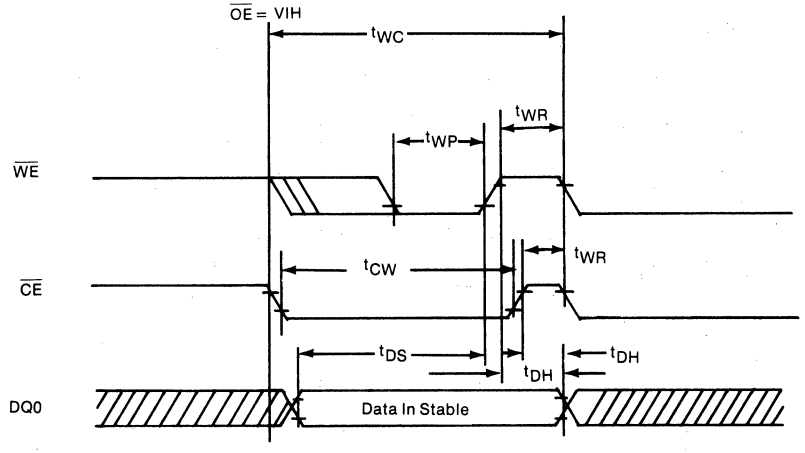
(0°C to 70°C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3V	t_F	0			μs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	μs	7

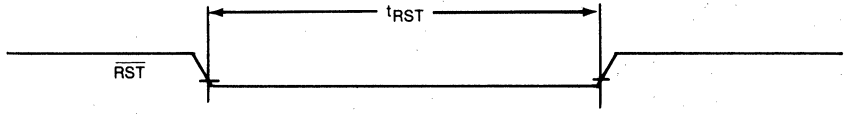
TIMING DIAGRAM—READ CYCLE TO SMARTWATCH



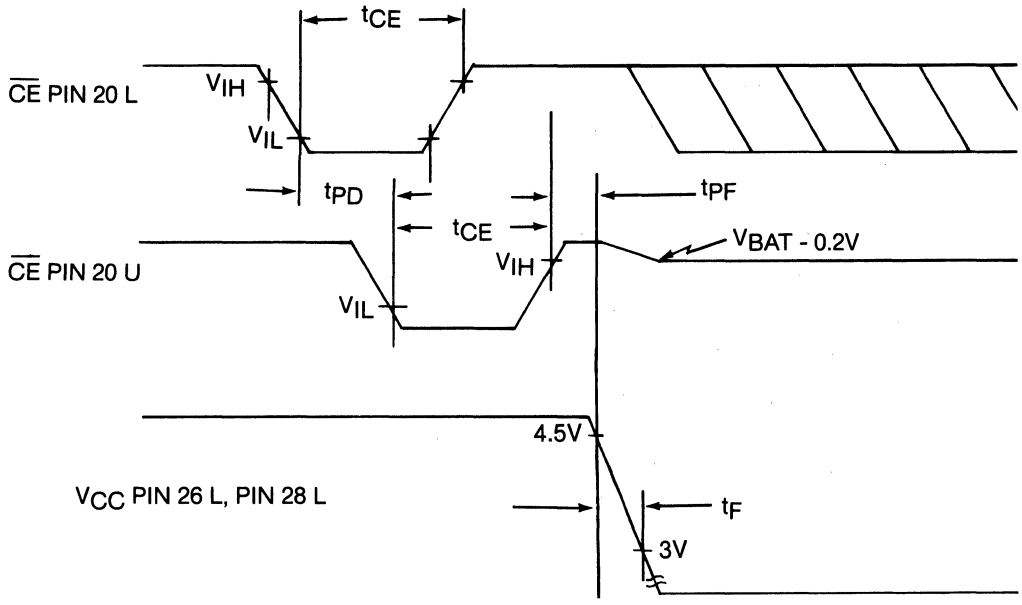
TIMING DIAGRAM—WRITE CYCLE TO SMARTWATCH



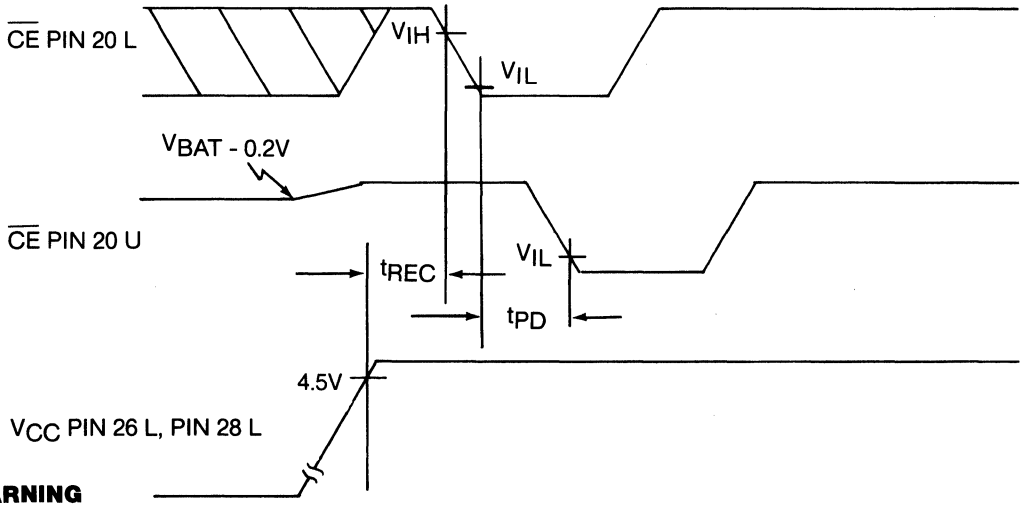
TIMING DIAGRAM—RESET FOR SMARTWATCH



TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP



WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

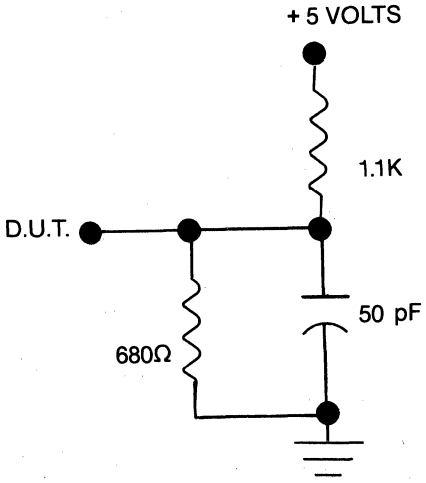
Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

NOTES

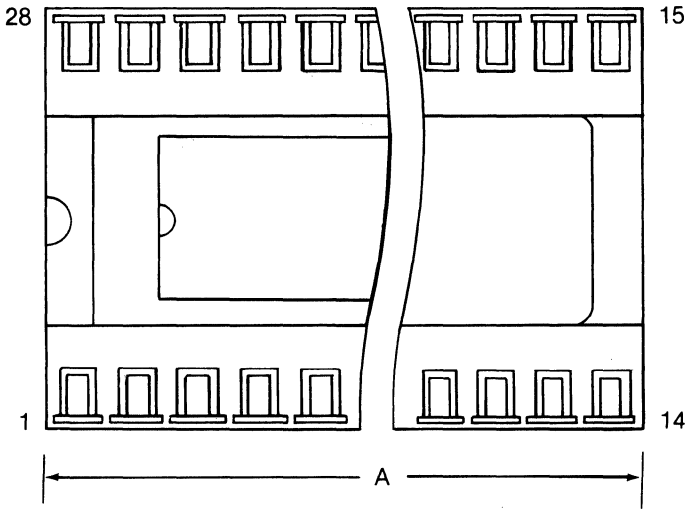
1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 3.
3. PIN locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. PIN 26 L may be connected to V_{CC} or left disconnected at the P.C. board.
6. I_{BAT} is the maximum current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. t_{CE} max. must be met to insure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.
10. Applies to Pins 1 L, 11 L, 20 L, 22 L, and 27 L
11. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$
12. t_{DH} and t_{DS} are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$
13. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

OUTPUT LOAD

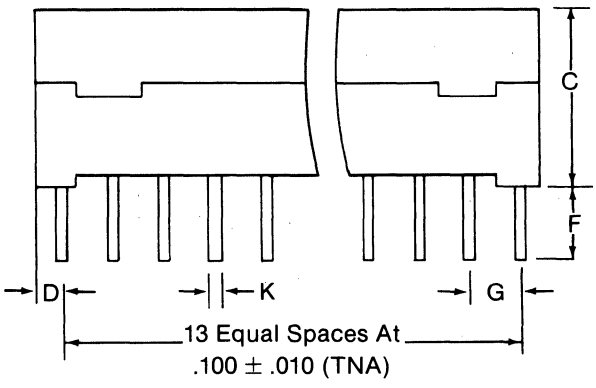
Figure 3

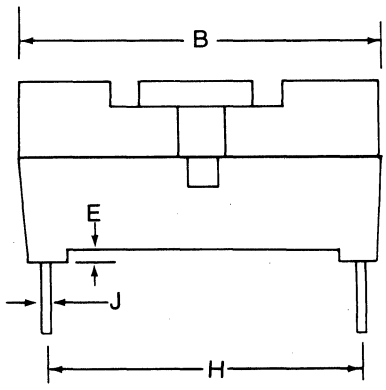


DS1216
SmartWatch



DIM.	INCHES	
	MIN.	MAX.
A	1.390	1.420
B	.695	.720
C	.350	.385
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





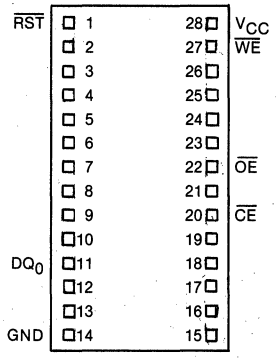
Dallas Semiconductor
SmartWatch/RAM 64/256K

DS1216C

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 8K × 8 and 32K × 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @25°C

PIN CONNECTIONS



PIN DEFINITIONS

All Pins Pass Through Except 20, 28
Pin 20 Conditioned Chip Enable
Pin 28 Switched V_{CC}
Pin 1 $\overline{RESET}$
Pin 22 Output Enable
Pin 27 Write Enable
Pin 11 Data Input/Output 0
Pin 14 Ground

DESCRIPTION

The DS1216C is a 28-pin 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K × 8 or a 32K × 8 JEDEC Bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216 data sheet for technical details.

Dallas Semiconductor
SmartWatch/RAM 256K/1M

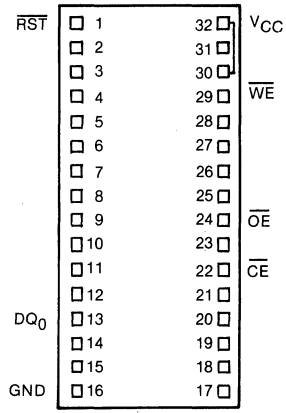
PRELIMINARY

DS1216D

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 8K × 8, 32K × 8, 128K × 8, and 512K × 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0 °C to 70 °C
- Accuracy is better than ± 1 min./month @25 °C

PIN CONNECTIONS



PIN DEFINITIONS

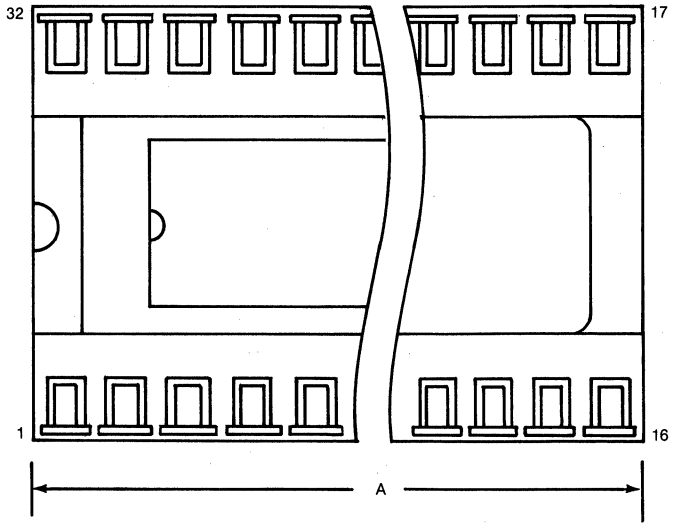
All pins pass through except 22, 30, and 32.
Pin 22 - Conditioned Chip Enable
Pin 32 - Switched V_{CC} for 32-pin RAM
Pin 1 - $\overline{\text{RESET}}$
Pin 24 - Output Enable
Pin 29 - Write Enable
Pin 13 - Data Input/Output 0
Pin 16 - Ground
Pin 30 - Switched V_{CC} for 28-pin RAM

DESCRIPTION

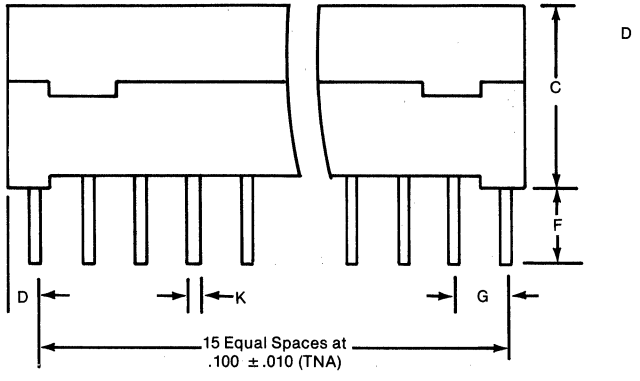
The DS1216D is a 32-pin 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K × 8, 32K × 8, 128K × 8, or 512K × 8 JEDEC Bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

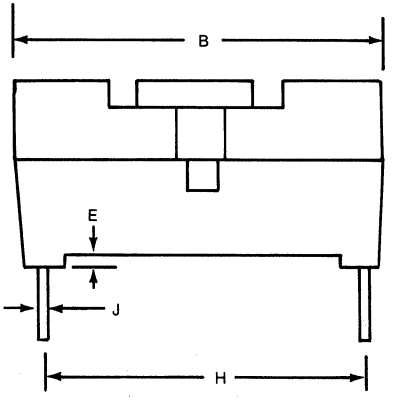
See the DS1216 data sheet for technical details.

DS1216D
SmartWatch



DIM.	INCHES	
	MIN.	MAX.
A	1.590	1.620
B	.695	.720
C	.350	.385
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





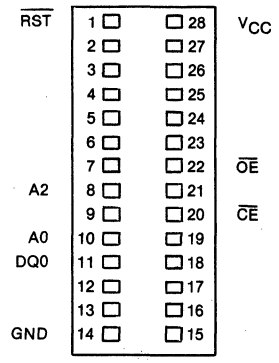
Dallas Semiconductor
SmartWatch/ROM 64/256K

DS1216E

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of month, months, and years
- Adds timekeeping to any 28-pin JEDEC Byte Wide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accurate to within 1 min./month @25°C

PIN CONNECTIONS



PIN NAMES

Pin 1 $\overline{RST}$ - Reset
Pin 8 A2 - Address Bit 2 (READ/$\overline{WRITE}$)
Pin 10 A0 - Address Bit 0 (Data Input)
Pin 11 DQ0 - I/O_0 (Data Output)
Pin 14 GND - Ground
Pin 20 $\overline{CE}$ - Conditioned Chip Enable
Pin 22 $\overline{OE}$ - Output Enable
Pin 28 V_{CC} - +5 VDC to the Socket

All pins pass through to the Socket except 20.

DESCRIPTION

The DS1216E is a 28-pin, 600-mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 28-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device take up no more area than the memory alone. The SmartWatch uses pins 1, 8, 10, 11, 20 and 22 for timekeeper control. All pins pass through to the socket receptacle except for pin 20 ($\overline{CE}$) which is inhibited during the transfer of time information.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, days, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

OPERATION

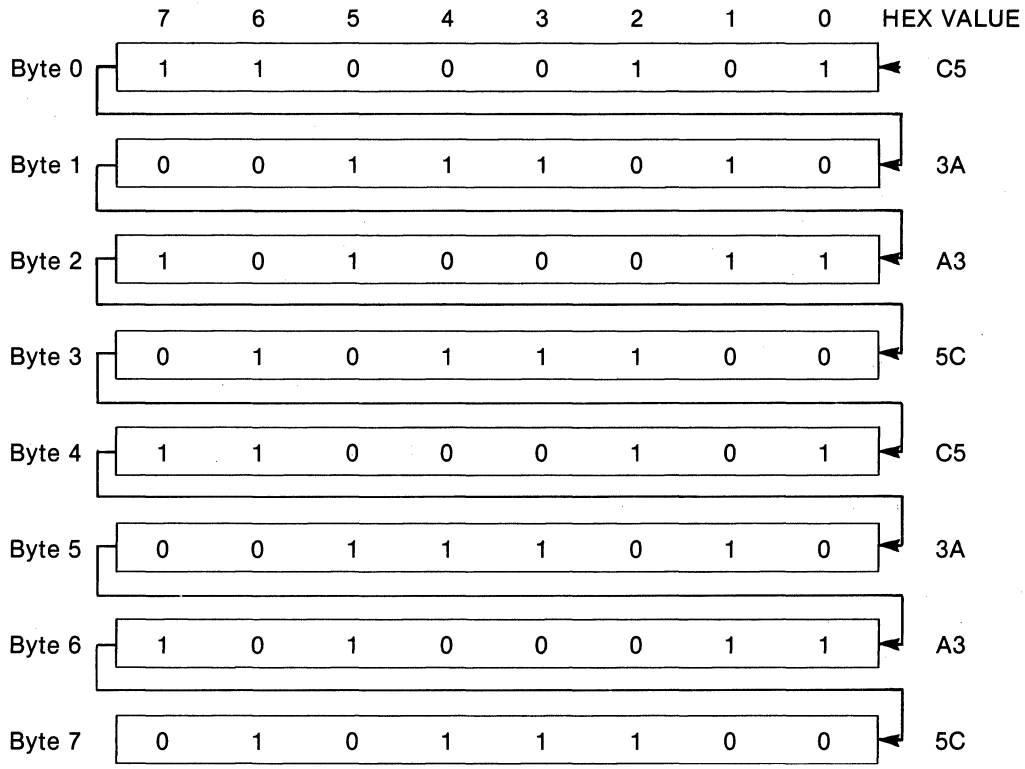
A highly structured sequence of 64 cycles is used to gain access to time information and temporarily disconnect the mated memory from the system bus. Information transfer into and out of the SmartWatch is achieved by using address bits A0 and A2, control signals $\overline{OE}$ and $\overline{CE}$, and Data I/O line DQ0. All SmartWatch data transfers are accomplished by executing read cycles to the mated memory address space. Write and read functions are determined by the level of address bit A2. When address bit A2 is low, a write cycle is enabled and data must be input on address bit A0. When address bit A2 is high, a read cycle is enabled and data is output on data I/O line DQ0. Either control signal ($\overline{OE}$ or $\overline{CE}$) must transition low to begin and high to end memory cycles which are directed to the SmartWatch. However, both control signals must be in an active state during a memory cycle. Communication with the SmartWatch is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles, placing address bit A2 low with the proper data on address bit A0. The 64 write cycles are used only to gain access to the SmartWatch. Prior to executing the first of 64 write cycles, a read cycle should be executed by holding A2 high. The read cycle will reset the comparison register pointer within the SmartWatch insuring the pattern recognition starts with the first bit of the sequence. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above, until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive data on Data In (A0) or transmit data on Data Out (DQ0), depending on the level of READ/$\overline{WRITE}$ (A2). Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ and $\overline{OE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

An unconditional reset to the SmartWatch occurs by either bringing A14 ($\overline{RESET}$) low, if enabled, or on power up. This $\overline{RESET}$ can occur during pattern recognition or while accessing the SmartWatch registers. $\overline{RESET}$ causes access to abort and forces the comparison register pointer back to Bit 0 without changing registers.

NONVOLATILE CONTROLLER OPERATION

The DS1216E SmartWatch performs circuit functions required to make the timekeeping function nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. The second function provides power fail detection. Power fail detection occurs at typically 4.25 volts. Finally the nonvolatile controller protects the SmartWatch register contents by ignoring any inputs after power fail detection has occurred. Power fail detection also has the same effect on data transfer as the RESET input.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1



NOTE:
The pattern recognition sequence in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern accidentally occurring and causing inadvertent entry to the SmartWatch is less than 1 in 10^{19}.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch registers are in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

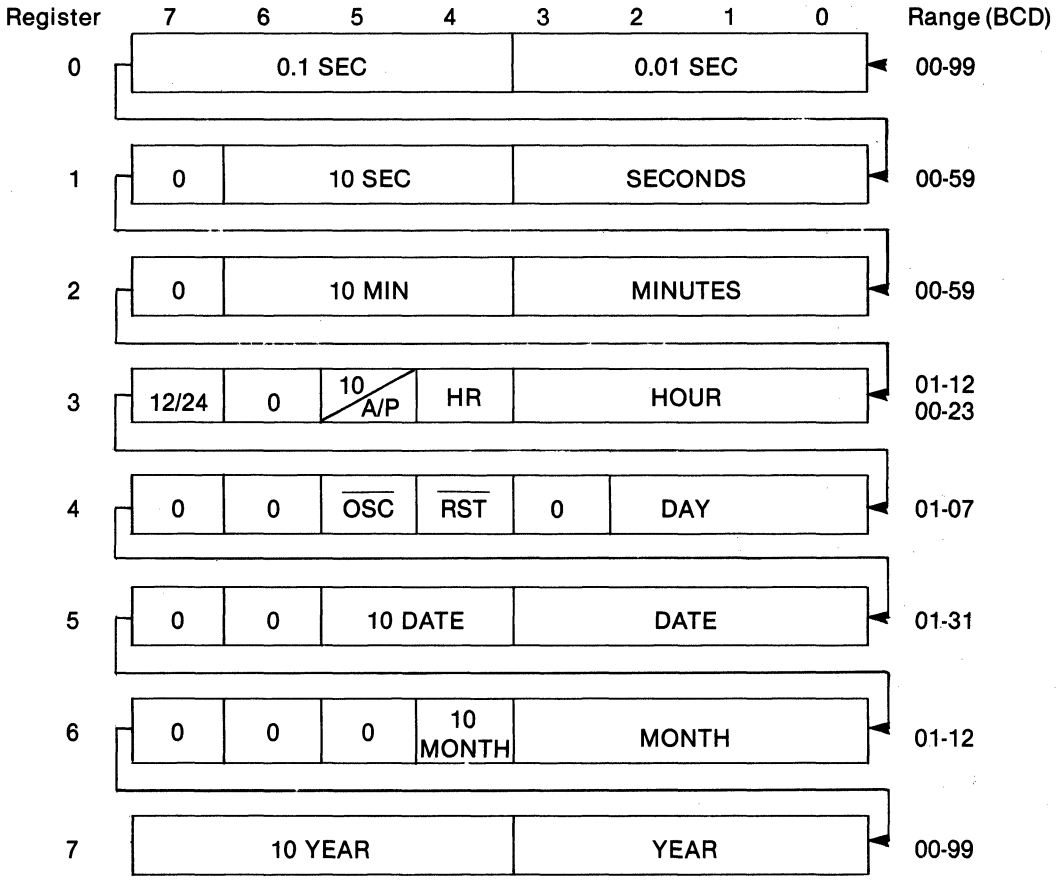
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logical 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logical 0, a low input on the $\overline{\text{RESET}}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from Dallas Semiconductor set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

SMARTWATCH REGISTER DEFINITION Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to 70°C
Soldering Temperature	260°C for 10 Sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1,3
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1,6
Logic 0	V_{IL}	−0.3		+0.8	V	1,6

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28L Supply Current	I_{CC}			5	mA	3,4
Input Leakage	I_{IL}	−1.0		+1.0	uA	4,6,10
Output @2.4V	I_{OH}	−1.0			mA	2
Output @0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

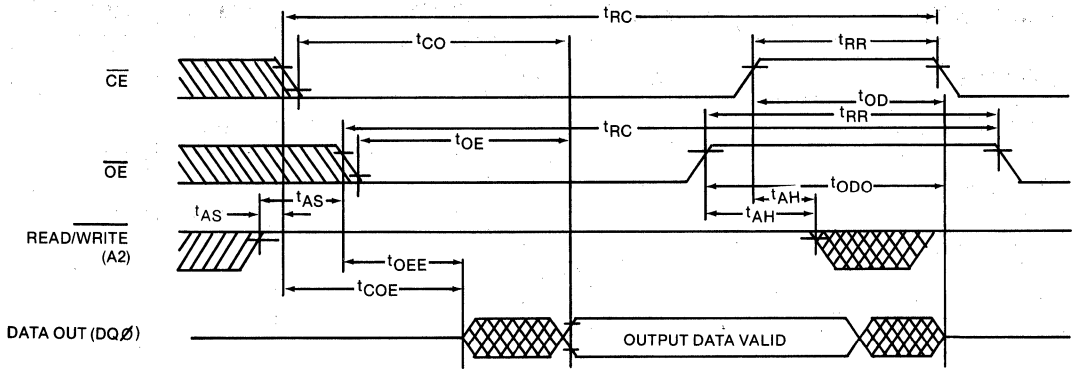
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			200	ns	
$\overline{CE}$ to Output in Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output in Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output in High Z	t_{OD}			100	ns	
$\overline{OE}$ to Output in High Z	t_{ODO}			100	ns	
Address Set Up Time	t_{AS}	20			ns	9
Address Hold Time	t_{AH}			10	ns	8
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
$\overline{OE}$ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	7
Data Set Up Time	t_{DS}	100			ns	8
Data Hold Time	t_{DH}	10			ns	8
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

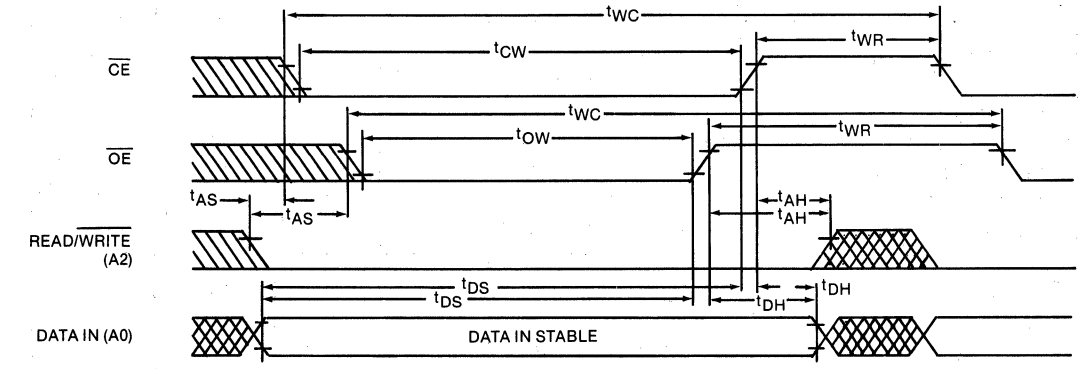
(0 °C to 70 °C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 -3V	t_F	0			ms	

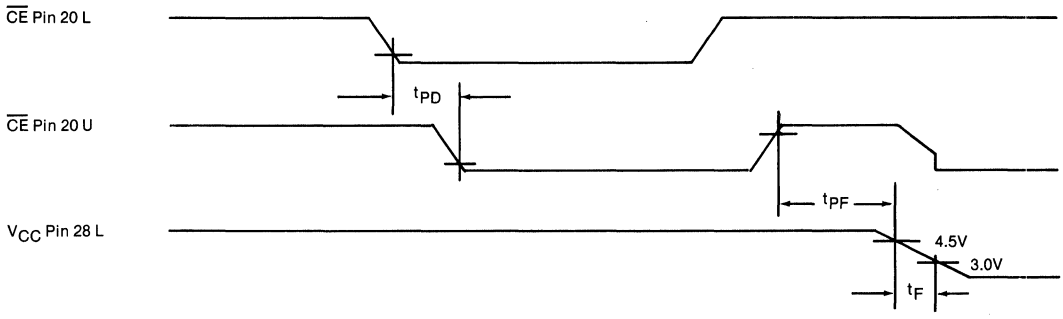
TIMING DIAGRAM— READ CYCLE



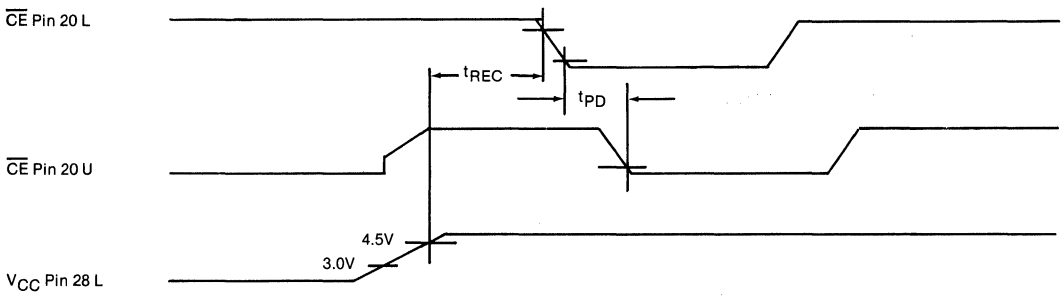
TIMING DIAGRAM—WRITE CYCLE



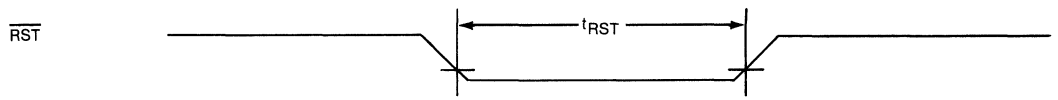
TIMING DIAGRAM— POWER DOWN



TIMING DIAGRAM— POWER UP



TIMING DIAGRAM—RESET FOR SMARTWATCH



WARNING

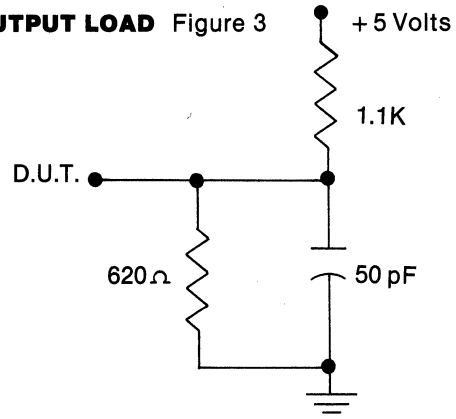
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

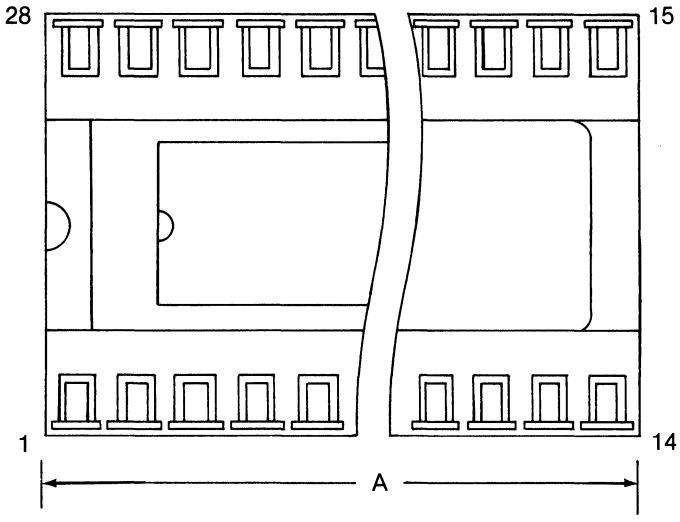
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Input pulse rise and fall times equal 10 ns.
6. Applies to Pins 1 L, 8 L, 10 L, 20 L, and 22 L.
7. t_{WR} and t_{RR} are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
8. t_{AH}, t_{DS} and t_{DH} are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
9. t_{AS} is a function of the latter occurring edge of $\overline{OE}$ or $\overline{CE}$.
10. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

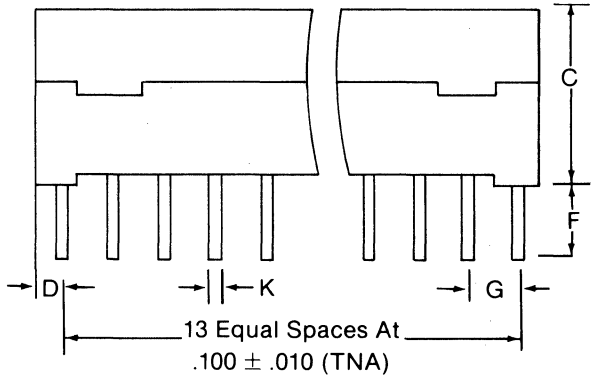
OUTPUT LOAD Figure 3

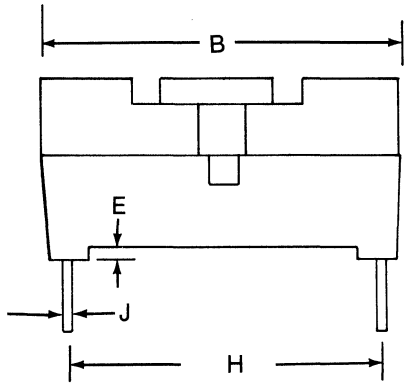


DS1216E
SmartWatch



DIM.	INCHES	
	MIN.	MAX.
A	1.390	1.420
B	.695	.720
C	.350	.385
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





6

Dallas Semiconductor
SmartWatch/ROM 64/256K/1M

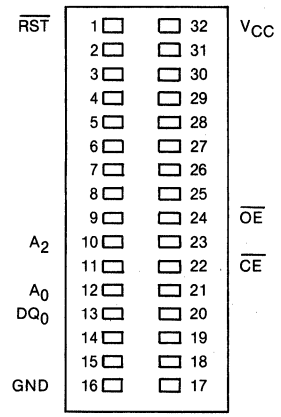
PRELIMINARY

DS1216F

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adds timekeeping to any 32-pin JEDEC Byte Wide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accuracy to within 1 min./month @25°C

PIN CONNECTIONS



PIN NAMES

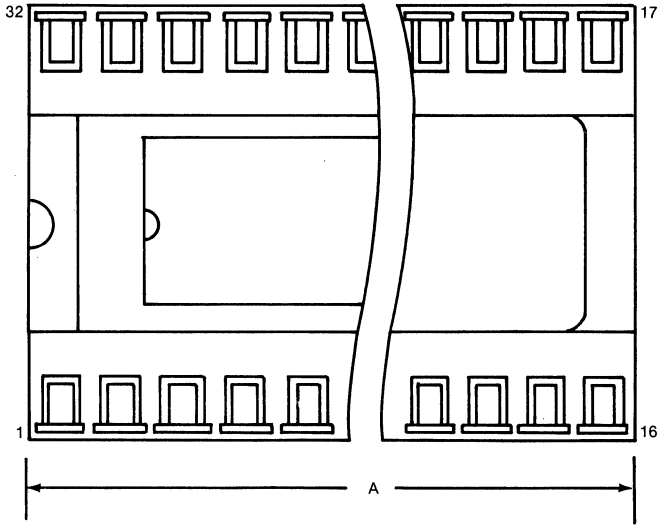
Pin 1 $\overline{RST}$ - Reset
Pin 10 A_2 - Address Bit 2 (READ/$\overline{WRITE}$)
Pin 12 A_0 - Address Bit 0 (Data Input)
Pin 13 DQ_0 - I/O_0 (Data Output)
Pin 16 GND - Ground
Pin 22 $\overline{CE}$ - Conditioned Chip Enable
Pin 24 $\overline{OE}$ - Output Enable
Pin 32 V_{CC} - +5 VDC to the Socket
All pins pass through to the Socket except 22.

DESCRIPTION

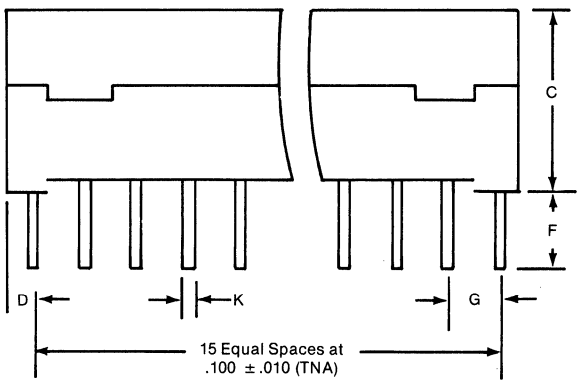
The DS1216F is a 32-pin 600-mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 32-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

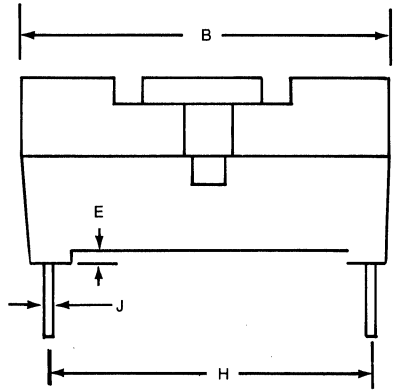
Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device take up no more area than the memory alone. The SmartWatch uses pins 1, 10, 12, 13, 22 and 24 for timekeeper control. All pins pass through to the socket receptacle except for pin 22 ($\overline{CE}$) which is inhibited during the transfer of time information.

See the DS1216E data sheet for technical details and SmartWatch operation.



DIM.	INCHES	
	MIN.	MAX.
A	1.590	1.620
B	.695	.720
C	.350	.385
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





Dallas Semiconductor
LCA SmartSocket

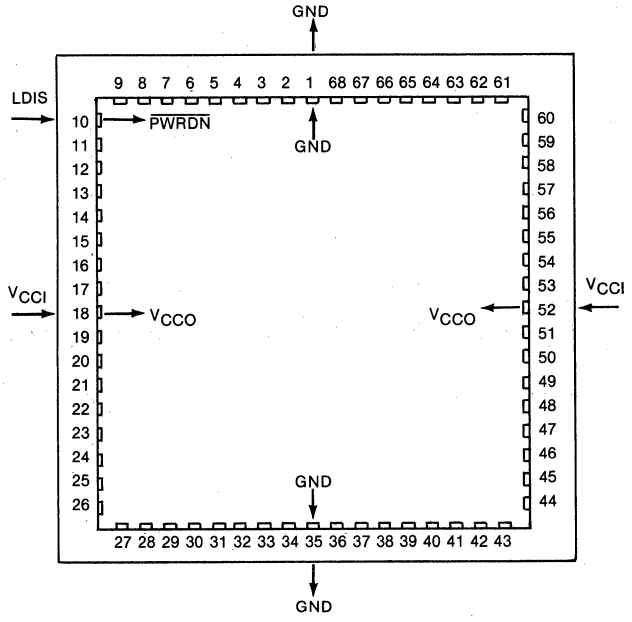
PRELIMINARY

DS1264

FEATURES

- SmartSocket keeps logic defined in Xilinx/MMI LCA's in the absence of power
- Accepts Xilinx/MMI 2064 68-pin LCA
- Eliminates need for external memory to hold a copy of the logic configuration data
- Logic configuration already defined on power-up; no time required for initial loading
- Embedded IC provides power-fail detection, $\overline{PWRDN}$ pin control and automatic switching between system V_{CC} and lithium voltage
- Electronic freshness seal (lithium save) insures full lithium capacity after shipping and handling
- 68- pin sockets accept JEDEC plastic chip carriers with tin-plated leads

DS1264 PIN DESCRIPTION



PIN DESCRIPTION

All pins pass straight through to the LCA in the 68-pin socket except for the following:

LDIS (active pulsed low)—Lithium Disconnect: Lithium Disconnect may be used to disconnect the lithium source during periods of time when nonvolatility is not required. This function is brought out in place of the LCA's $\overline{PWRDN}$ pin. The LCA's $\overline{PWRDN}$ pin is connected to the Power Fail ($\overline{PF}$) output signal of the controller IC embedded within the socket.

V_{CC}—Power Supply: System power is routed to the embedded control IC which switches power to the LCA between the system supply when it is applied during full operation and the lithium power source for nonvolatility in the absence of system power.

The table below summarizes the assignments for these pins for the LCA SmartSocket:

	DS1264 for 2064 68-pin LCA
SIGNAL	**PIN #**
LDIS	10
V_{CC}	18, 52
GND	1, 35

DESCRIPTION

The DS1264 is a 68-pin PLCC socket with a built-in CMOS IC controller circuit and an encapsulated lithium energy source. It is specifically designed to provide nonvolatile support for the Xilinx/MMI Logic Cell Array (LCA). The DS1264 accommodates the 68-pin 2064 LCA.

The 2064 LCA is a CMOS logic array device in which the internal configuration is determined by self-contained bits of RAM storage. The data contained in this RAM is used to define logic block functions, configuration of I/O blocks, routing of internal signals, and other options. As a result, the user can quickly implement complex digital logic functions directly without the requirement for masking or other vendor performed programming steps. In addition, the use of internal RAM allows logic design changes to be quickly implemented and verified in the prototype system. Complete reconfiguration "on-the-fly" of the final production system is also possible.

The use of RAM for holding the LCA's configuration data allows a maximum amount of flexibility in a programmable logic device. Without nonvolatile support, however, the device must be re-loaded from external memory each time that the configuration data is lost due to a power down or to a brownout condition. This not only requires additional memory to contain the logic configuration data, but also a considerable amount of time following power up to perform the reload operation.

The DS1264 alleviates these problems by providing nonvolatile support with a minimum impact on system hardware. No additional circuitry is required for nonvolatile operation, and no additional printed circuit board area is used since the combination of the SmartSocket and the LCA uses no more area than the LCA alone. When the socket is mated with the LCA, it provides a complete, self-contained solution for nonvolatile support. Only three pins are used for nonvolatile control of the LCA. All other pins are passed straight through to the socket receptacle.

POWER CYCLING OPERATION

The schematic shown in Figure 1 illustrates the internal connection of the LCA SmartSockets. The timing diagram in Figure 2 illustrates the timing operation of the system when power to the system is cycled off and on. During normal system operation, incoming V_{CC} voltage is monitored by the DS1259 for two thresholds below nominal operating voltage. Both of these thresholds are detected by the SmartSocket as V_{CC} decays in a power-down situation. The first (highest) threshold which is detected during a power-down is the Power Fail Voltage (V_{PF}). When V_{CC} falls below this value the $\overline{PWRDN}$ pin on the LCA is pulled down to its active low level by the $\overline{PF}$ output from the embedded control IC. This action will force the LCA to suspend all operation and go into its low power consumption mode. All clocks will be stopped within the device and all outputs are placed into high impedance state. All configuration data is maintained in the device when $\overline{PWRDN}$ is held at its active low level.

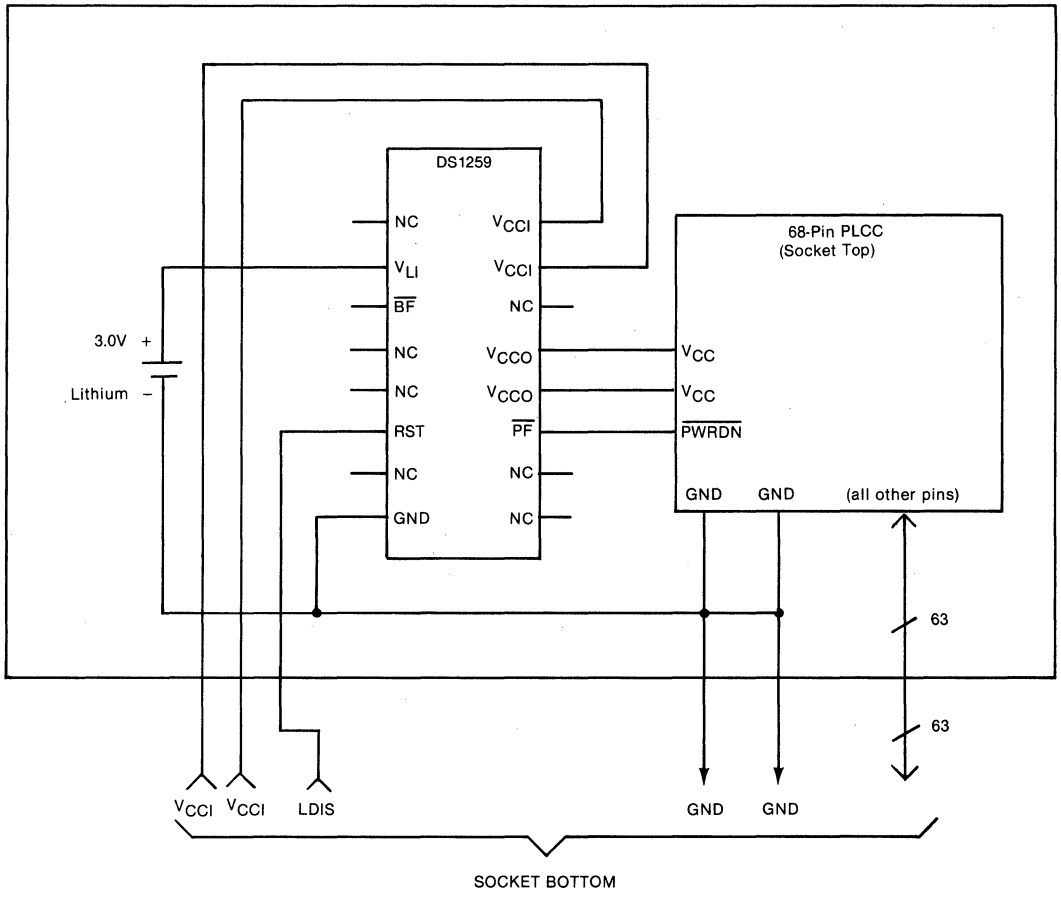
As V_{CC} voltage continues to decay during a power-down, it will eventually drop below the second (lower) threshold detected by the SmartSocket, which is Power Down Voltage (V_{PD}). When this occurs the internal lithium source is automatically switched to the V_{CC} pins on the LCA device and the $\overline{PWRDN}$ input will continue to be held in its active state. At this point the configuration data will be maintained by power supplied from the lithium source.

During a power-up, the reverse of the sequence described above will take place. When V_{CC} rises above the V_{PD} threshold, the V_{CC} lines of the LCA will be switched from the lithium source to the system V_{CC} lines. When V_{CC} subsequently rises above the V_{PF} threshold, the $\overline{PWRDN}$ pin of the LCA will be driven to its inactive high level, and full operation of the device can then take place.

LITHIUM DISCONNECT

The Lithium Disconnect (LDIS) input to the LCA SmartSocket can be used to disconnect the lithium source from the LCA V_{CC} lines. This feature is useful in situations where the system is to be powered down for a long period of time without the need for data retention, as might be the case when the system is stored in a stockroom. By disconnecting the lithium source, its full energy capacity can be assured at the time when use of the system begins. Accidental discharge is also prevented during shipping and handling. This feature is activated with a high-going pulse to the LDIS input while system power is being applied above the V_{PF} threshold. When system power is removed following this action the LCA's V_{CC} lines will be isolated from the lithium source. The next time that power is applied normal operation will again take place when V_{CC} rises above the V_{PF} threshold, and the LCA's V_{CC} lines once again will be connected to the lithium source when the system is powered down. The timing diagram in Figure 2 illustrates the operation of the SmartSocket in response to the LDIS input.

DS1264 LCA SMARTSOCKET INTERNAL SCHEMATIC Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.1V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Inputs: V_{CCL}	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage: LDIS	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Input Low Voltage: LDIS	V_{IL}	0		0.8	V	

D.C. ELECTRICAL CHARACTERISTICS

(V_{CC} voltage applied) (0°C to 70°C V_{CC} = 4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage LDIS	I_L	−1.0		+1.0	μA	10
Output High Current LDIS V_{OH} = 0.4V	I_{OH}	−1.0			mA	1,2,10
Output Low Current LDIS V_{OL} = 0.4V	I_{OL}			4.0	mA	1,2,10
Input Supply Current: V_{CCL}	I_{CC}			5	mA	3,10
Output Supply Current: V_{CCU}	I_{CCO}			250	mA	10
Power Fail Detect Voltage	V_{PF}		4.25	4.5	V	4
Power Down Detect Voltage	V_{PD}		V_{LI}		V	6

D.C. ELECTRICAL CHARACTERISTICS

(V_{CC} voltage removed) (0 °C to 70 °C $V_{CC} \leq V_{PF}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Lithium Voltage	V_{LI}		3		V	7,9,10
Lithium Supply Current: V_{CCU}	I_{LI}			10	nA	3
				1	μA	8

CAPACITANCE

($t_A = 25$ °C)

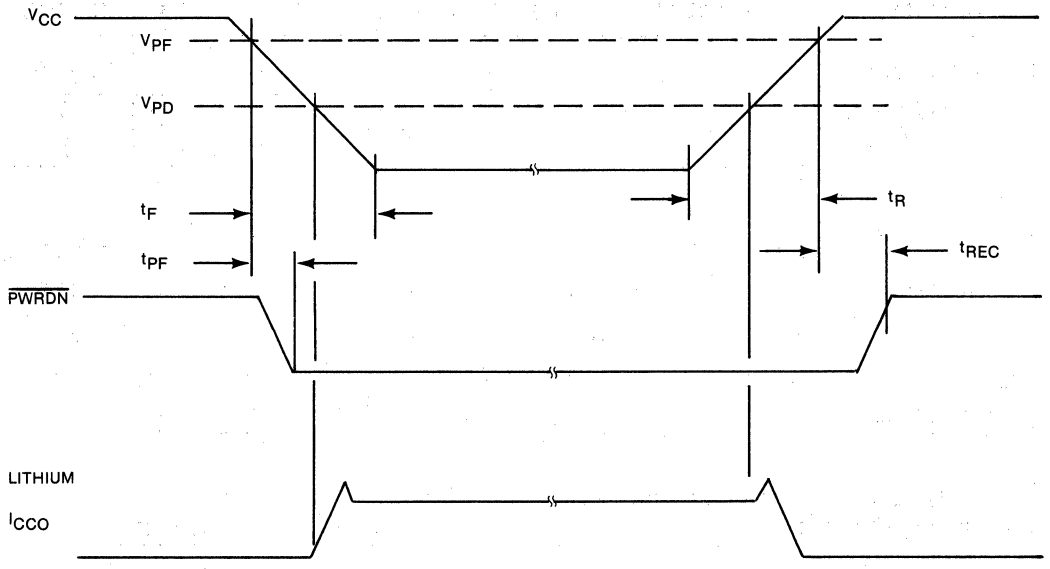
PARAMETER	SYMBOL	TYP	MAX	UNITS
Output Capacitance	C_O	5	10	pF
Input Capacitance	C_I	5	10	pF

A.C. ELECTRICAL CHARACTERISTICS

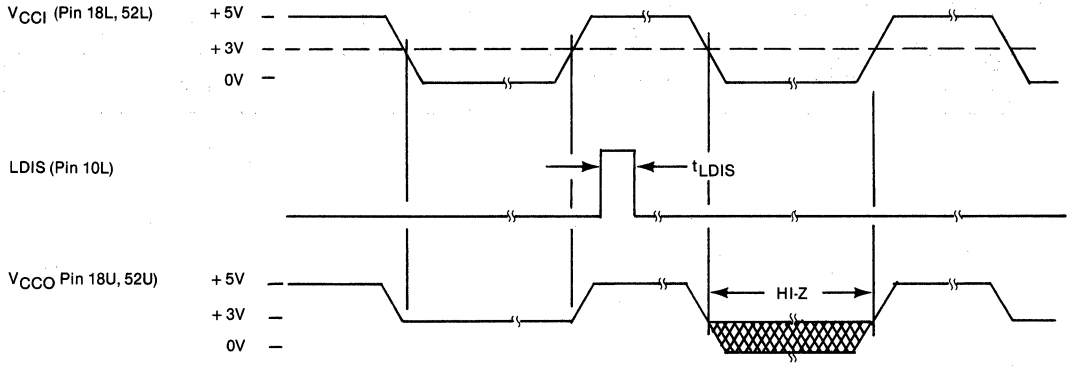
(V_{CC} voltage applied) (0 °C to 70 °C, $V_{CC} = 4.0$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Slew Rate (Falling edge)	t_F	300			us	
V_{CC} Slew Rate (Rising edge)	t_R	1			us	
Power Fail to $\overline{\text{PWRDN}}$ low	t_{PF}	0			us	
$\overline{\text{PWRDN}}$ High after Power Up	t_{REC}	2	10	20	ms	

POWER CYCLING OPERATION Figure 2



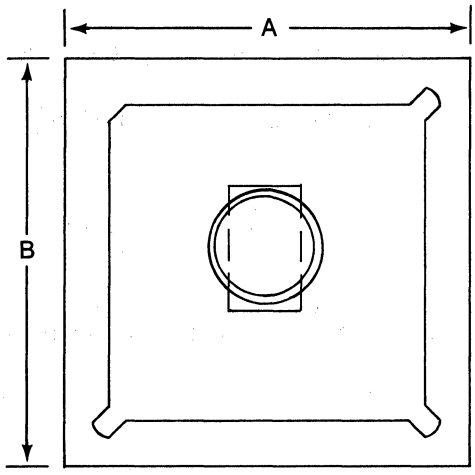
LITHIUM DISCONNECT TIMING Figure 3



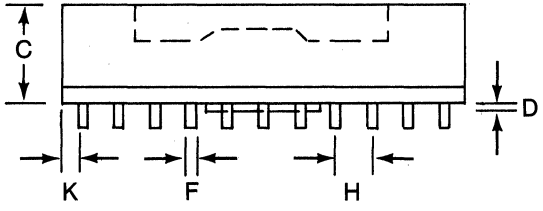
NOTES:

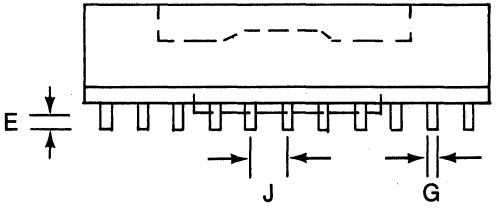
1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with socket empty.
4. V_{PF} is the point that $\overline{PWRDN}$ is driven low.
5. Both V_{CCO} outputs will meet the rated voltage and current as the lithium energy source retains at least 10% of its original capacity.
6. V_{PD} is the point that power is switched from system V_{CC} to the lithium source tied to the V_{LI} pin.
7. V_{LI} is the internal lithium energy source voltage.
8. Measured with LCA in socket; maximum value allowed for 10 yr. data retention at 25°C.
9. Storage loss is less than 1% per year at 25°C.
10. Pin names designated with a "U" suffix refer to the signal applied to the LCA pin on the at-the-socket receptacle. Pin names designated with the "L" suffix refer to the signal coming into the socket on the lower pin.

DS1264
LCA SMARTSOCKET



DIM.	INCHES	
	MIN.	MAX.
A	1.180	1.220
B	1.180	1.220
C	.455	.485
D	.025	.035
E	.115	.145
F	.015	.022
G	.015	.022
H	.090	.110
J	.090	.110
K	.085	.115





Timekeeping

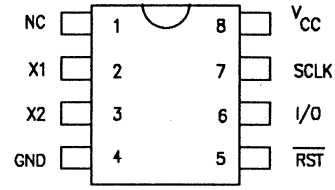
Dallas Semiconductor
Serial Timekeeper

PRELIMINARY
DS1202 8-Pin DIP
DS1202S 16-Pin SOIC

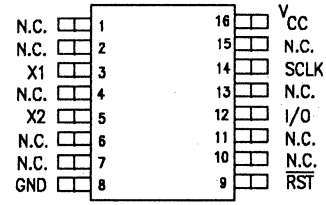
FEATURES

- Real Time clock counts seconds, minutes, hours, date of the month, day of the week and year with Leap Year compensation
- 24 x 8 RAM for scratch pad data storage
- Serial I/O for minimum pin count
- 3 volt clock operation
- Uses less than1 uA at 3 volts
- Single byte or multiple byte (burst mode) data transfer for read or write of clock or RAM data
- 8-pin DIP or optional 16-pin SOIC for surface mount
- Simple 3-wire interface
- TTL compatible (V_{CC} = 5V)

PIN CONNECTIONS



8-Pin DIP



16-Pin SOIC

PIN NAMES

N.C.	-No Connection
X1, X2	-32.768 KHz Crystal Input
GND	-Ground
$\overline{RST}$	- Reset
I/O	-Data Input/Output
SCLK	-Serial Clock
V_{cc}	-Power Supply Pin

DESCRIPTION

The DS1202 contains a RealTime Clock/Calendar, 24 bytes of static RAM, and communicates with a microprocessor via a simple serial interface. The RealTime Clock/Calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for Leap Year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Interfacing the DS1202 with a microprocessor is simplified using synchronous serial communication. Only three wires are required to communicate with the Clock /RAM: (1) $\overline{RST}$ (Reset), (2) I/O (Data line), and (3) SCLK (Serial Clock). Data can be transferred to and from the Clock/RAM one byte at a time or in a burst of up to 24 bytes. The DS1202 is designed to operate on very low power and retain data and clock information on less than 1 uA with voltage input, (V_{cc}) as low as three volts.

OPERATION

The main elements of the serial Timekeeper are shown in Figure 1, namely, shift register, control logic, oscillator, RealTime Clock and RAM. To initiate any transfer of data, $\overline{RST}$ is taken high and eight bits are loaded into the shift register providing both address and command information. Each bit is serially input on the rising edge of the clock input. The first eight bits specify which of 32 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have occurred which load the command word into the shift register, additional clocks will output data for a read, or input data for a write. The number of clock pulses equals eight plus eight for byte mode or eight plus up to 192 for burst mode.

ADDRESS/COMMAND BYTE

The address/command byte is shown in Figure 2. Each data transfer is initiated by a one byte input called the address/command byte. As defined, the MSB (Bit 7) must be a logical one. If zero, further action will be terminated. Bit 6 specifies a clock/calendar register if logic zero or a RAM location if Logical One. Bits one through five specify the designated registers to be input or output and the LSB (Bit 0) specifies a write operation (input) if logical zero or read operation output if logical one.

BURST MODE

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits one through five = logical one). As before, bit six specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at location 8 through 31 in the Clock/Calendar Registers or locations 24 through 31 in the RAM Registers.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves two functions. First, $\overline{RST}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a method of terminating either single byte or multiple byte data transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. All data transfer terminates if the $\overline{RST}$ input is low and the I/O pin goes to a high impedance state. When data transfer is terminated to the Real-Time Clock or to RAM using $\overline{RST}$, the transition of $\overline{RST}$ must occur while the clock is at high level to avoid disturbing the last bit of data and write cycle transfer must occur in 8-bit groups. Data transfer is illustrated in Figure 3

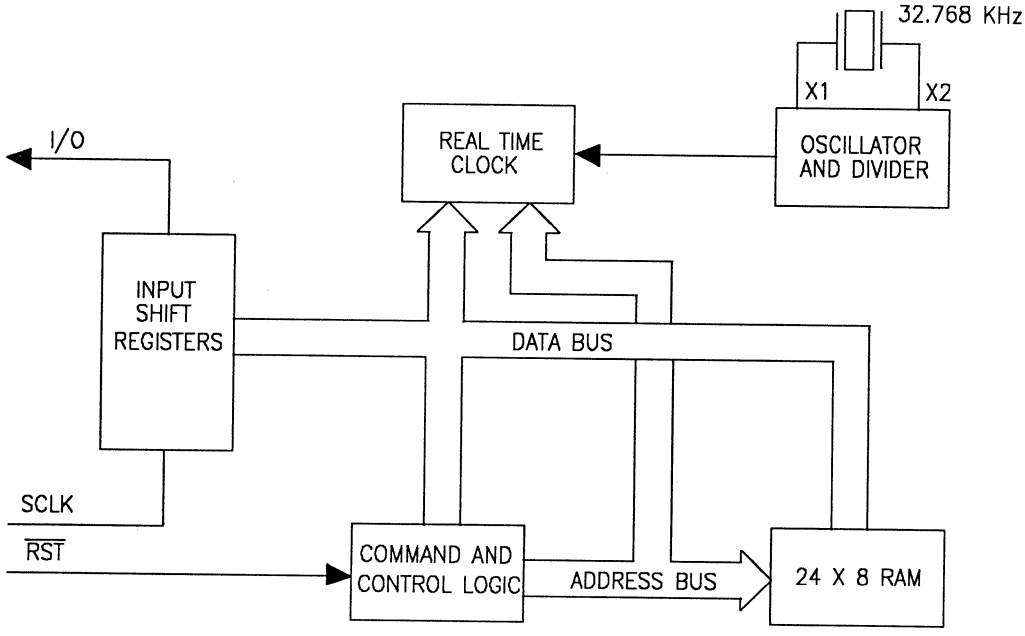
DATA INPUT

Following the eight SCLK cycles that input the write mode address/command byte (Bit 0 = Logical 0), a data byte is input on the rising edge of the next eight SCLK cycles (per byte, if burst mode is specified). Additional SCLK cycles are ignored should they inadvertently occur.

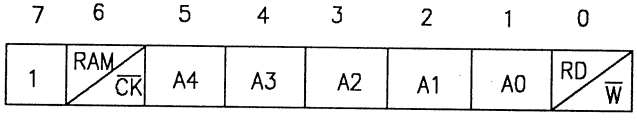
DATA OUTPUT

Following the eight SCLK cycles that input the read mode address/command byte (Bit 0 = Logical 1), a data byte is output on the falling edge of the next eight SCLK cycles (per byte, if the burst mode is specified). Note that the first data bit to be transmitted from the clock/RAM occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{RST}$ remains high. This operaton permits continuous burst read mode capability.

DS1202 BLOCK DIAGRAM Figure 1

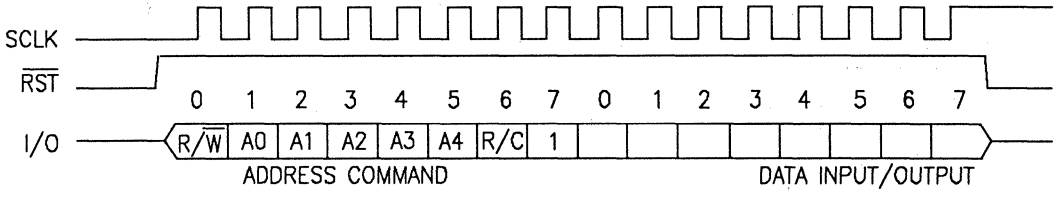


ADDRESS/COMMAND BYTE Figure 2

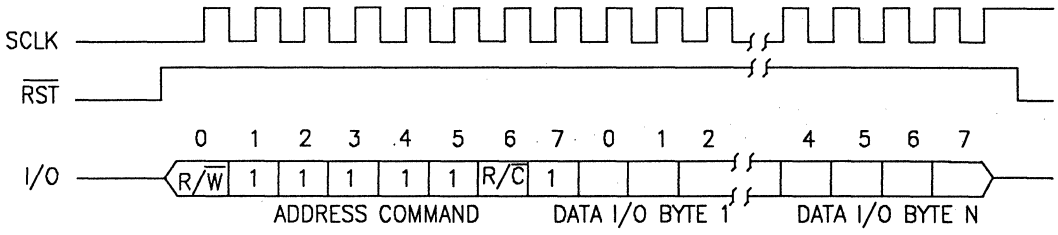


DATA TRANSFER SUMMARY Figure 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	24	200

CLOCK/CALENDAR

The Clock/Calendar is contained in eight writeable/readable registers as shown in Figure 4. Data contained in the clock/calendar registers is in binary coded decimal format (BCD) except the control byte which is binary.

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic one, the clock oscillator is stopped and the DS1202 is placed into a low power standby mode with a current drain of less than .1 microamp. When this bit is written to logical zero, the clocks oscillator will run and keep time count from the entered value.

AM-PM/12-24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

TEST MODE BITS

Bit 7 of the date register and bit 7 of the day register are test mode bits. These bits are forced to zero under normal operation and will always read logical zero when read.

CONTROL BYTE AND WRITE PROTECT BIT

Byte 7 of the clock/calendar registers is the write protect byte. The first seven bits (bits 0-6) are forced to zero and will always read a zero when read. Bit 7 of the user byte is the write protect flag. Bit seven is set to logical one on power up and may be set high or low by writing the byte . When high, the write protect flag prevents a write operation to any internal register including both clock and RAM. Further, logic is included such that the write protect bit may be reset to a logical zero by a write operation.

CLOCK/ CALENDAR BURST MODE

Address 31 decimal of the clock/calendar address space specifies burst mode operation. In this mode the eight clock/calendar registers may be consecutively read or written. Addresses above seven (user byte) are non-existent; only addresses 0-7 are accessible.

RAM

The static RAM is contained in 24 writeable/ readable registers, addressed consecutively in the RAM address space beginning at location zero.

RAM BURST MODE

Addresses 31 decimal of the RAM address space specifies burst mode operation. In this mode, the 24 RAM registers may be consecutively read or written. Addresses above the maximum RAM address location are non-existent and are not accessible.

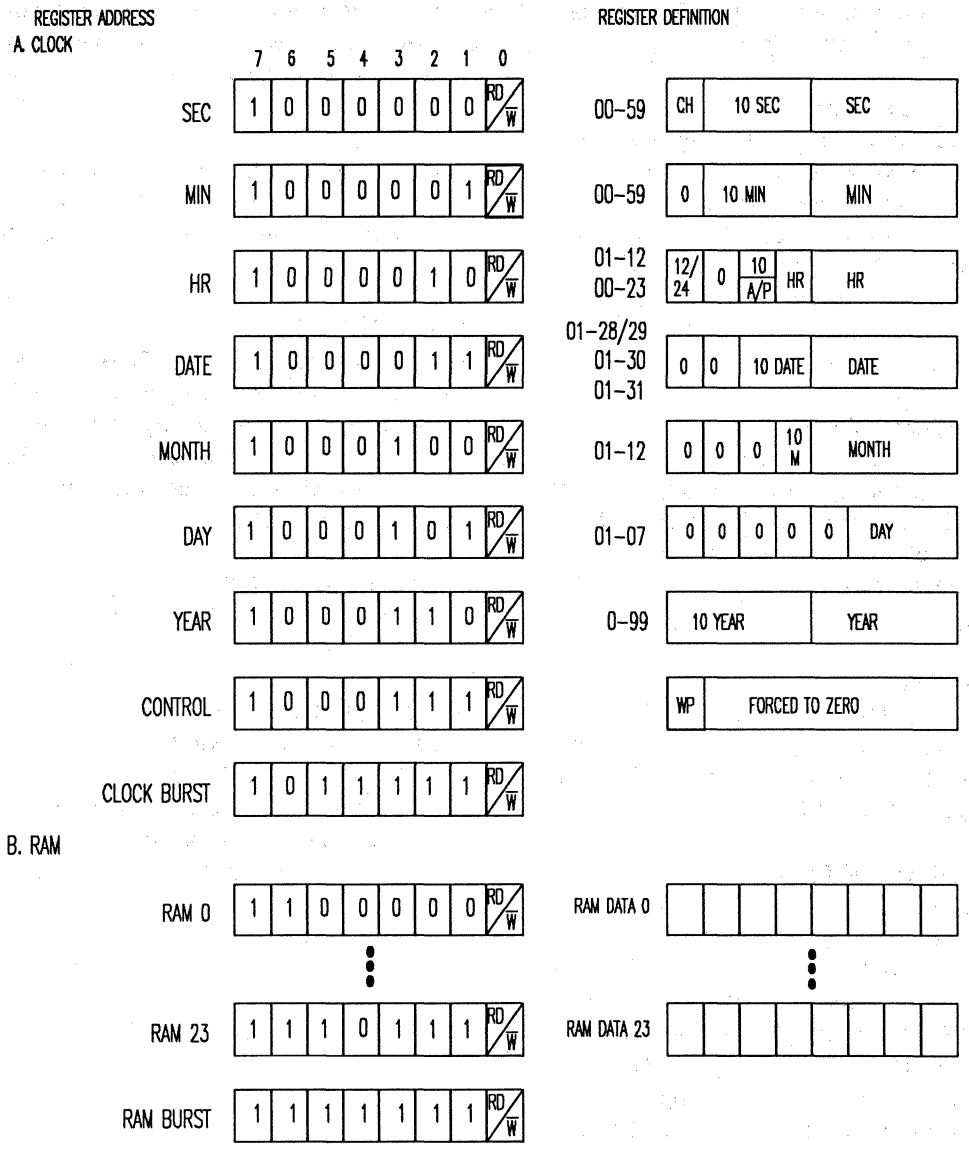
REGISTER SUMMARY

A register data format summary is shown in Figure 4.

CRYSTAL SELECTION

A 32.768 KHZ crystal, Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, can be directly connected to the DS1202 via pins 2 and 3 (x1, x2). The crystal selected for use should have a specified load capacitance (C_L) of 6 pF.

REGISTER ADDRESS/DEFINITION Figure 4



ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON ANY PIN RELATIVE TO GROUND -0.5V TO +7.0V
OPERATING TEMPERATURE 0°C TO +70°C
STORAGE TEMPERATURE -55°C TO +125°C
SOLDERING TEMPERATURE -260°C FOR 10 SEC

RECOMMENDED D.C. OPERATING CONDITIONS

(0^{o} to $+70^{o}C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply voltage	V_{CC}	4.5	5.0	5.5	VOLTS	1
Standby Supply Voltage	V_{CC1}	3.0		5.5	VOLTS	1
Logic 1 Input	V_{IH}	2.0		V_{CC}	VOLTS	1
Logic 0 Input	V_{IL}	-0.5		0.8	VOLTS	1

D.C. ELECTRICAL CHARACTERISTICS

(0^{o} to $+70^{o}C$, V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}			+500	uA	6
I/O Leakage	I_{LO}			+500	uA	6
Logic 1 Output	V_{OH}	2.4			VOLTS	2
Logic 0 Output	V_{OL}			0.4	VOLTS	3
Active Supply Current	I_{CC}			4	mA	4
Standby Supply Current	I_{CC1}			1	uA	5
StandbySupply Current	I_{CC2}			100	nA	10

CAPACITANCE

(TA =25°C)

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	C_X		6		pF	

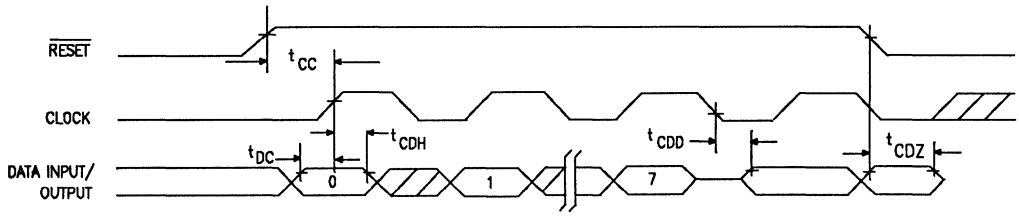
A.C. ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V ±10% 0°C TO 70°C)

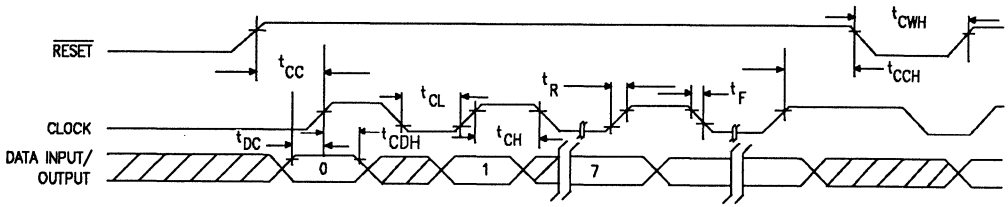
PARAMETER	SYMBOL	MIIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	50			ns	7
CLK To Data Hold	t_{CDH}	70			ns	7
CLK To Data Delay	t_{CDD}			200	ns	7,8,9
CLK Low Time	t_{CC}	250			ns	7
CLK High Time	t_{CH}	250			ns	7
CLK Frequency	f_{CLK}	D.C.		2.0	MHz	7
CLK Rise &Fall	t_F			500	ns	
RST To CLK Setup	t_{CC}	1			us	7
CLK To RST Hold	t_{CCH}	60			ns	7
RST Inactive Time	t_{CWH}	1			us	7
RST To I/O High Z	t_{CDZ}			70	us	7

TIMING DIAGRAM - READ/WRITE DATA TRANSFER Figure 5

WRITE DATA TRANSFER



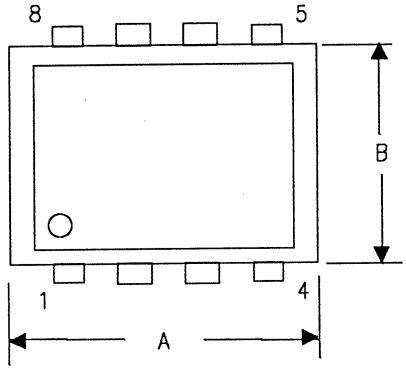
READ DATA TRANSFER



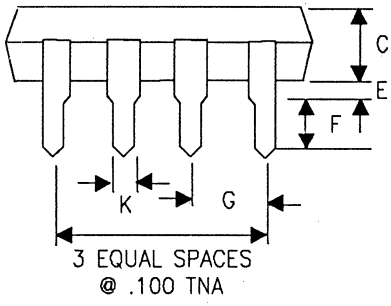
NOTES

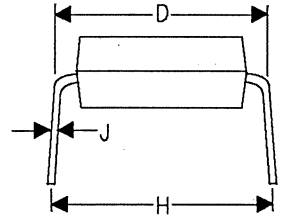
1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 MA.
3. Logic zero voltages are specified at a sink current of 4 MA.
4. I_{CC} is specified with the I/O pin open.
5. I_{CC1} is specified with V_{CC} at 3.0 volts and $\overline{RST}$, I/O, and SCLK are open.
6. $\overline{RST}$, SCLK and I/O all have 40 K ohm pull down resistors to ground.
7. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10 ms maximum rise and fall time.
8. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
9. Load capacitance = 50 pF.
10. I_{CC2} is specified with V_{CC} at 3.0 volts and $\overline{RST}$, I/O, and SCLK are open. The clock halt flag must also be set to logic one.

DS1202
SERIAL TIMEKEEPER
8-PIN DIP



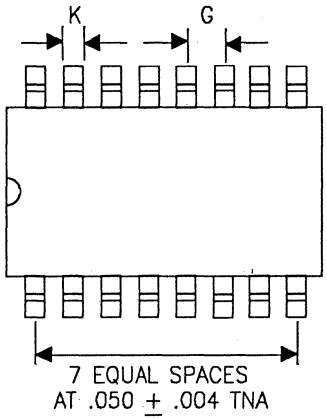
DIM.	INCHES	
	MIN.	MAX.
A	.345	.400
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

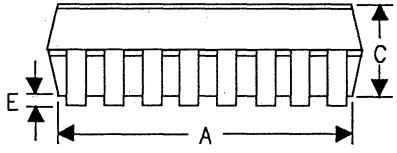


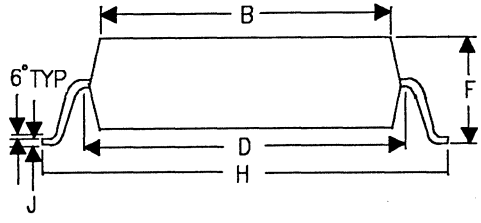


DS1202S
SERIAL TIMEKEEPER
16-PIN SOIC

DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019







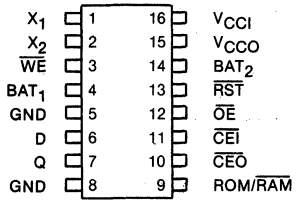
Dallas Semiconductor
TimeChip

DS1215

FEATURES

- TimeChip keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Leap year automatically corrected
- No address space required
- Provides nonvolatile controller functions for battery backing up RAM
- Supports redundant batteries for high-rel applications
- Uses a 32.768 KHz watch crystal
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Space saving 16-pin DIP package

PIN CONNECTIONS



PIN NAMES

Pins 1 & 2	-	X_1, X_2	- 32.768 KHz Crystal Connections
Pin 3	-	$\overline{WE}$	- Write Enable
Pin 4	-	BAT_1	- Battery 1 Input
Pins 5 & 8	-	GND	- Ground
Pin 6	-	D	- Data In
Pin 7	-	Q	- Data Out
Pin 9	-	ROM/ $\overline{RAM}$	- ROM-RAM Select
Pin 10	-	$\overline{CEO}$	- Chip Enable Out
Pin 11	-	$\overline{CEI}$	- Chip Enable Input
Pin 12	-	$\overline{OE}$	- Output Enable
Pin 13	-	$\overline{RST}$	- Reset
Pin 14	-	BAT_2	- Battery 2 Input
Pin 15	-	V_{CCO}	- Switched Supply Output
Pin 16	-	V_{CCI}	- +5V DC Input

NOTE: Both pins 5 and 8 must be grounded.

DESCRIPTION

The DS1215 is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch provides hundredths of seconds, seconds, minutes, hours, day, date, month, and year information, while the nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

The last date of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator, or a 24-hour mode.

The nonvolatile memory controller portion of the circuit is designed to handle power fail detection, memory write protection, and battery redundancy. In short, the controller changes standard CMOS memories into nonvolatile memories, and provides continuous power to the TimeChip. Alternatively the TimeChip can be used with ROM memory by controlling the Chip Enable Output signal ($\overline{CEO}$) while the TimeChip is being accessed.

OPERATION

The block diagram of Figure 3 illustrates the main elements of the TimeChip. Communication with the TimeChip is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on Data In (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the Chip Enable Output pin ($\overline{CEO}$).

After recognition is established, the next 64 read or write cycles either extract or update data in the TimeChip and Chip Enable Output remains high during this time, disabling the connected memory.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CEI}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the TimeChip starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the TimeChip. These 64 write cycles are used only to gain access to the TimeChip.

When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is *not* found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 1). With a correct match for 64 bits, the TimeChip is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the TimeChip to either receive data on D, or transmit data on Q, depending on the level of $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CEI}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the TimeChip.

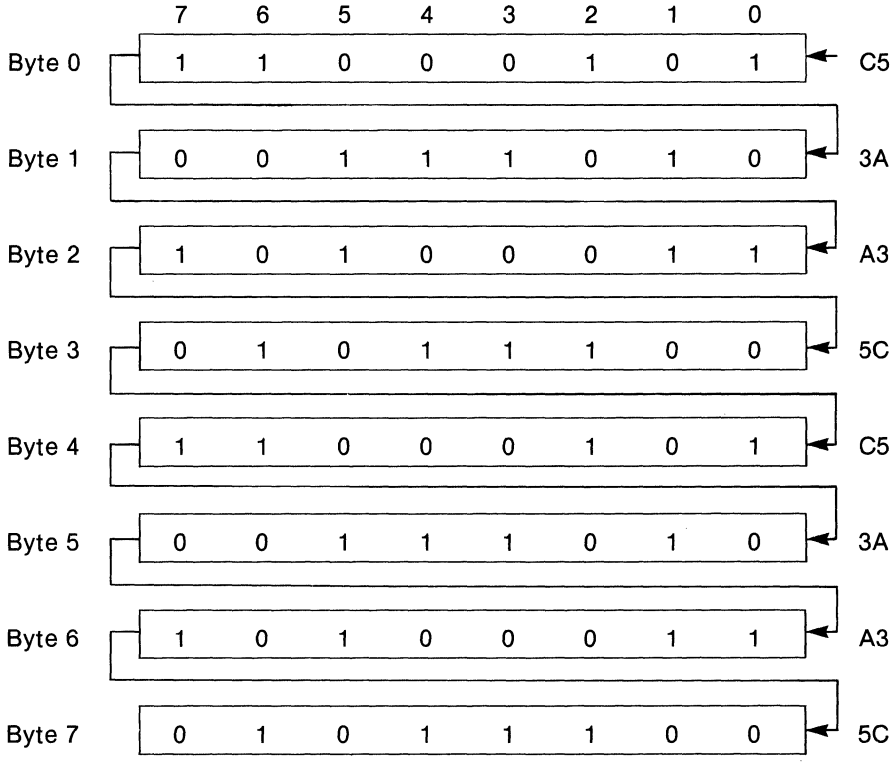
A 32,768 Hz quartz crystal, Daiwa part no. DT-26S or equivalent, can be directly connected to the DS1215 via pins 1 and 2 (X_1, X_2). The crystal selected for use should have a specified load capacitance of 6 pF.

NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the TimeChip is determined by the level of the ROM/$\overline{\text{RAM}}$ select pin. When ROM/$\overline{\text{RAM}}$ is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make static CMOS RAM and the timekeeping function nonvolatile. First a switch is provided to direct power from the battery inputs or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.2 volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS static RAM. The DS1215 also performs redundant battery control for high reliability. On power fail the battery with the highest voltage is automatically switched to V_{CCO}. If only one battery is used in the system, the unused battery input should be connected to ground. The DS1215 provides the function of safeguarding the TimeChip and RAM data by power fail detection and write protection. Power fail detection occurs when V_{CCI} falls below VTP which is equal to $1.26 \times V_{BAT}$. The DS1215 constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than VTP, a comparator outputs a power fail signal to the control logic. The power fail signal forces the chip enable output ($\overline{\text{CEO}}$) to V_{CCI} or $V_{BAT} - 0.2$ volts for external RAM write protection. During nominal supply conditions, $\overline{\text{CEO}}$ will track $\overline{\text{CEI}}$ with a maximum propagation delay of 20 ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the TimeChip registers and prevents future access until V_{CCI} exceeds VTP. A typical RAM/TimeChip interface is illustrated in Figure 4.

When the ROM/$\overline{\text{RAM}}$ pin is connected to V_{CCO}, the controller is set in the ROM mode. Since ROM is a read-only device which retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will not force $\overline{\text{CEO}}$ high when power fails. However, the TimeChip does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power fail as V_{CCI} falls below the level of V_{BAT}. A typical ROM/TimeChip interface is illustrated in Figure 5.

TIMECHIP COMPARISON REGISTER DEFINITION Figure 1

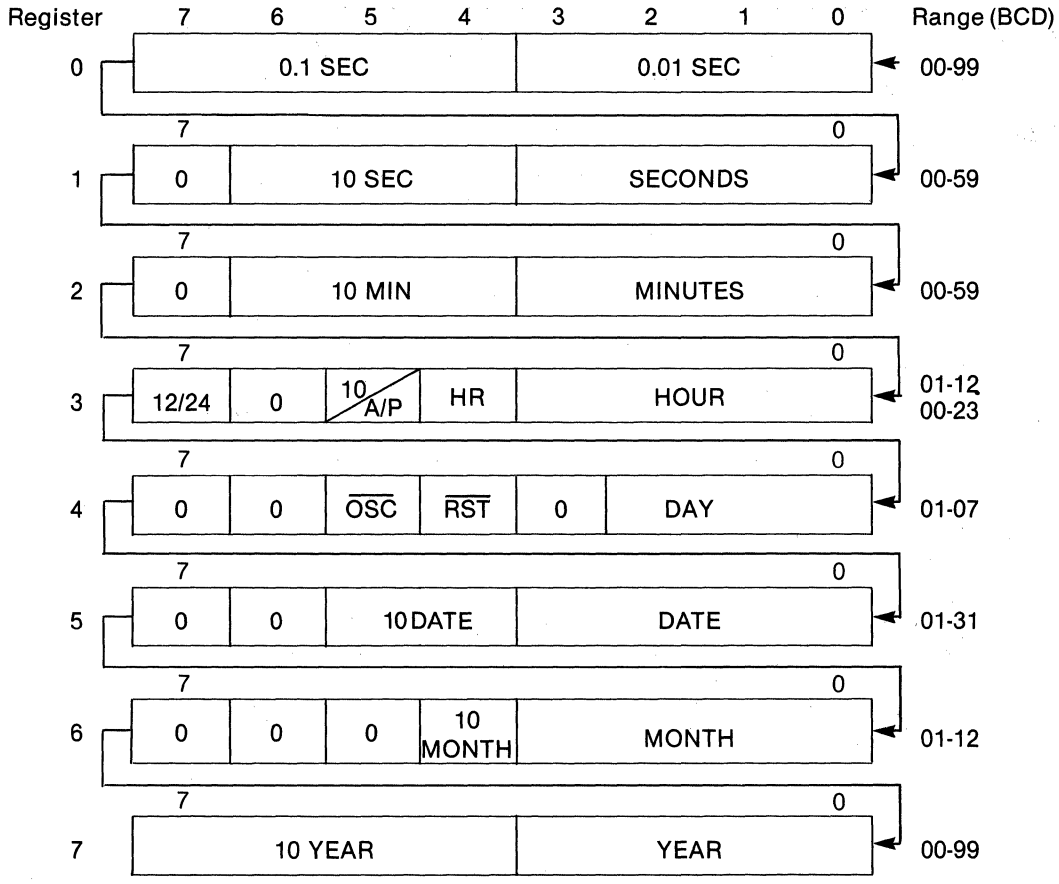


Note:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the TimeChip is less than 1 in 10^{19}.

TIMECHIP REGISTER INFORMATION
The TimeChip information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the TimeChip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the TimeChip registers are not binary coded decimal format (BCD) in 12-hour mode. Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

TIMECHIP REGISTER DEFINITION Figure 2

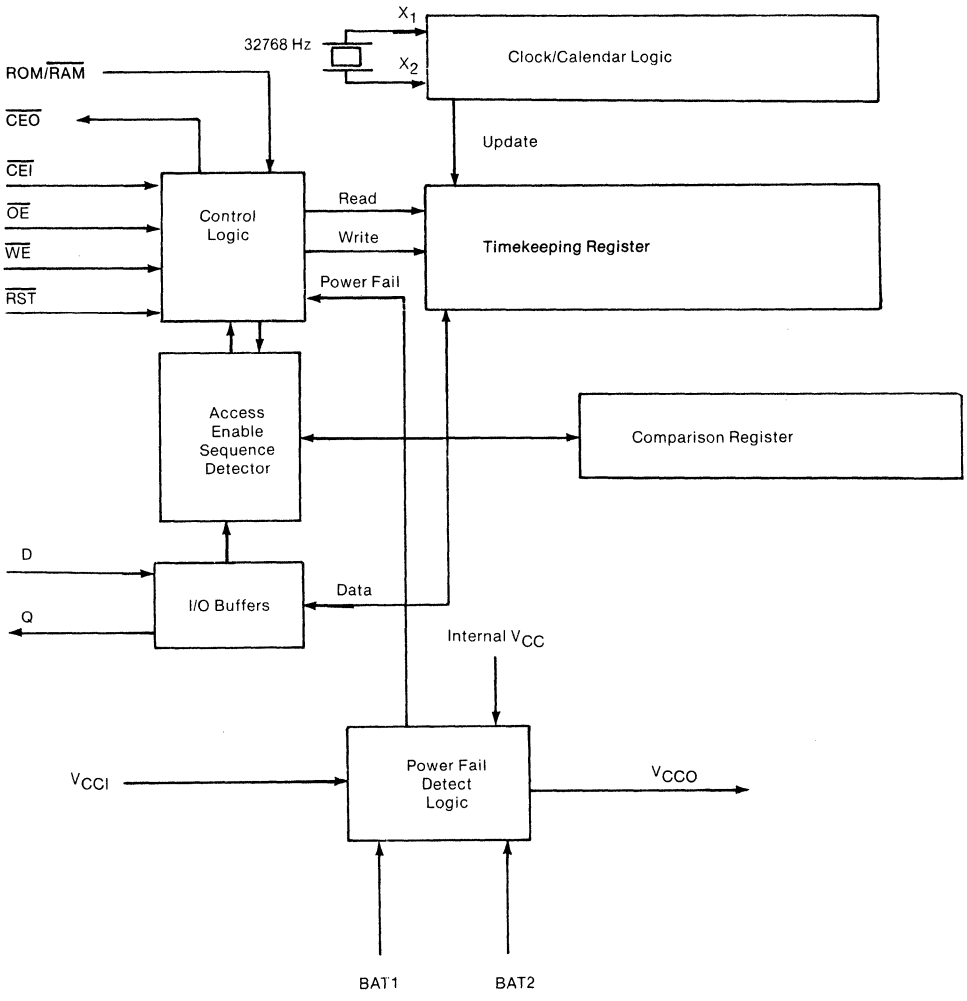


AM-PM/12/24 MODE
Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

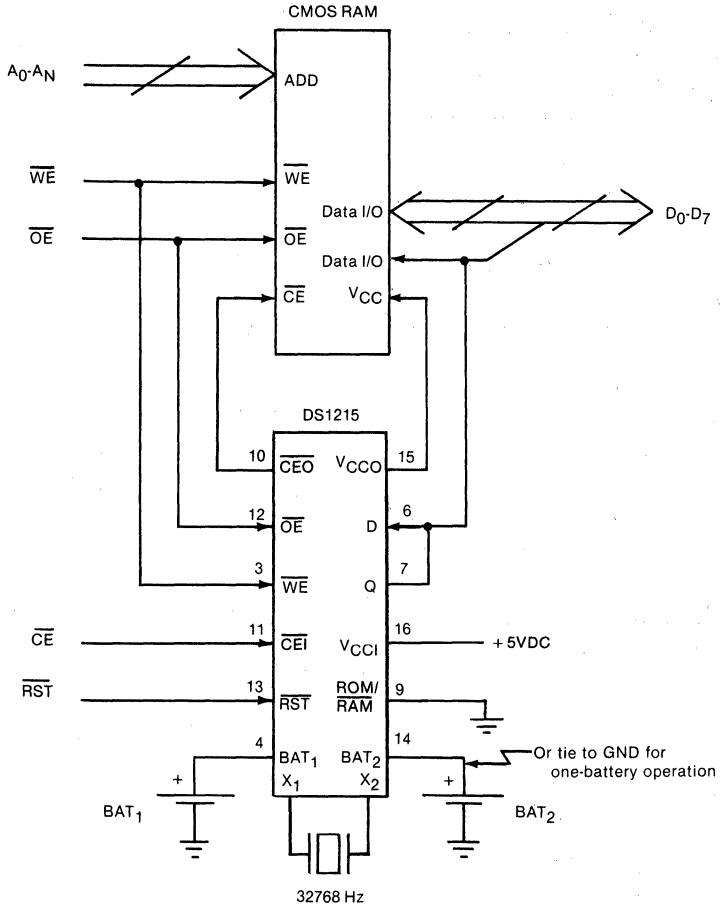
OSCILLATOR AND RESET BITS
Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logical 1, the reset input pin is ignored. When the reset bit is set to logical 0, a low input on the reset pin will cause the TimeChip to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to Logic 0 the oscillator turns on and the watch becomes operational.

ZERO BITS
Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

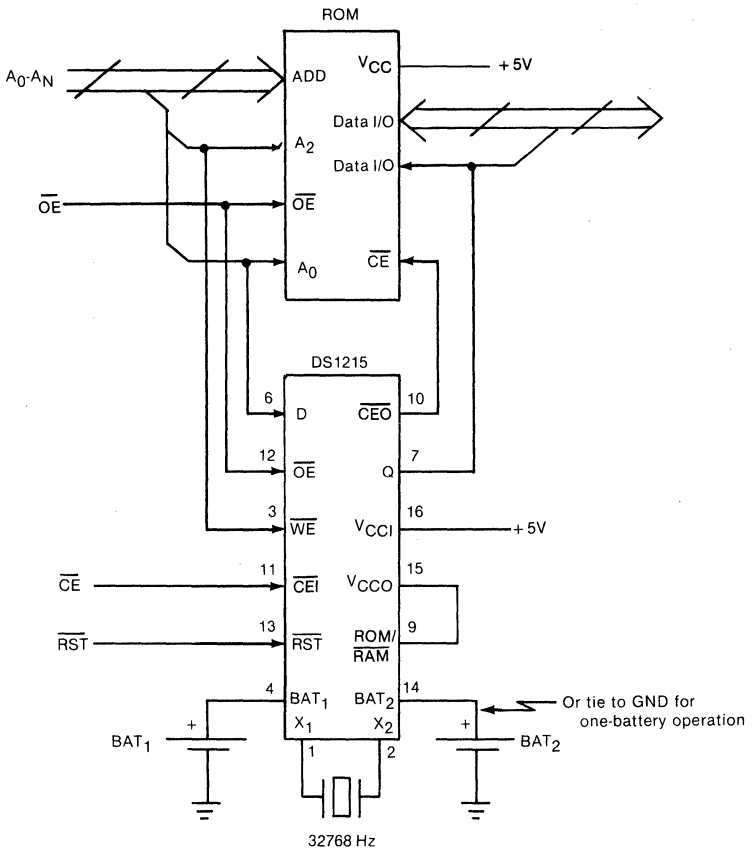
TIMECHIP BLOCK DIAGRAM Figure 3



RAM/TIMECHIP INTERFACE Figure 4



ROM/TIMECHIP INTERFACE Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0	V_{IL}	−0.3		+0.8	V	1
V_{BAT1} or V_{BAT2} Battery Voltage	V_{BAT}	2.5		3.7	V	7

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

Supply Current	I_{CCI}			5	mA	6
Supply Current $V_{CCO}=V_{CCI}-0.2$	I_{CCO1}			80	mA	8
Input Leakage	I_{IL}	−1.0		+1.0	μA	
Output Leakage	I_{LO}	−1.0		+1.0	μA	
Output @2.4V	I_{OH}	−1.0			mA	2
Output @0.4V	I_{OL}			4.0	mA	2

(0°C to 70°C, V_{CC} ◁ 4.5V)

$\overline{CEO}$ Output	V_{OH1}	V_{CCI} or $V_{BAT}-0.2$			V	9
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			1	μA	6
Battery Backup Current @$V_{CCO}=V_{BAT}-0.2V$	I_{CCO2}			10	μA	10

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

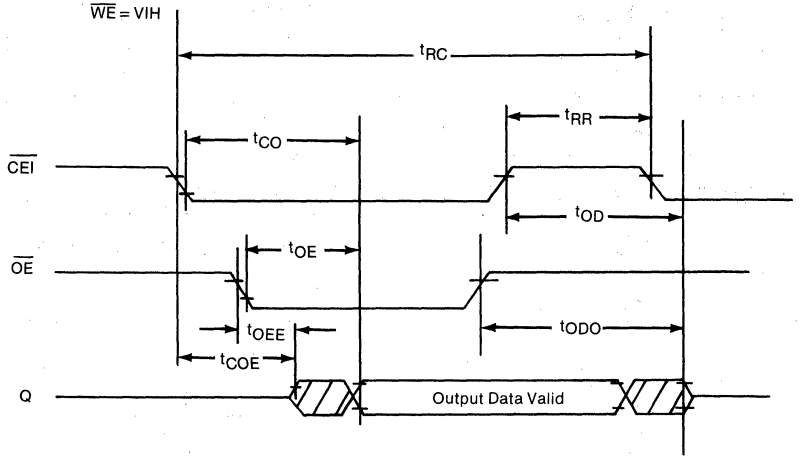
A.C. ELECTRICAL CHARACTERISTICS ROM/$\overline{RAM}$ = GND (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$I Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$I To Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$I To Output High Z	t_{OD}			100	ns	
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Set Up	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{CE}$I Pulse Width	t_{CW}	170			ns	
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$I Propagation Delay	t_{PD}	5	10	20	ns	2, 3
$\overline{CE}$I High to Power Fail	t_{PF}			0	ns	

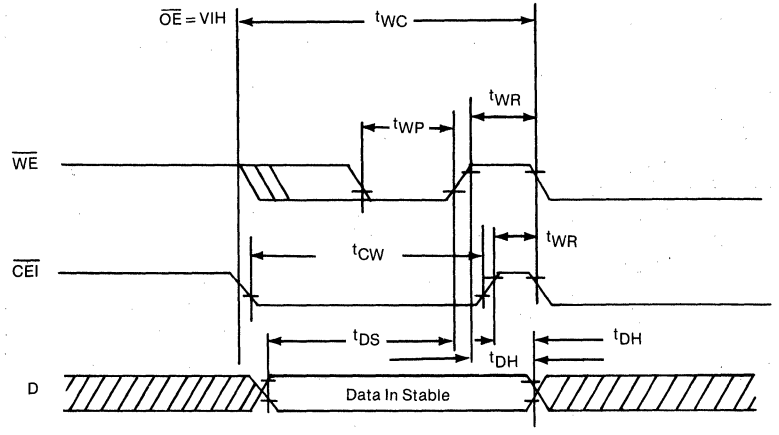
(0°C to 70°C, V_{CC}<4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

TIMING DIAGRAM—READ CYCLE TO TIMECHIP ROM/$\overline{\text{RAM}}$ = GND



TIMING DIAGRAM—WRITE CYCLE TO TIMECHIP ROM/$\overline{\text{RAM}}$ = GND



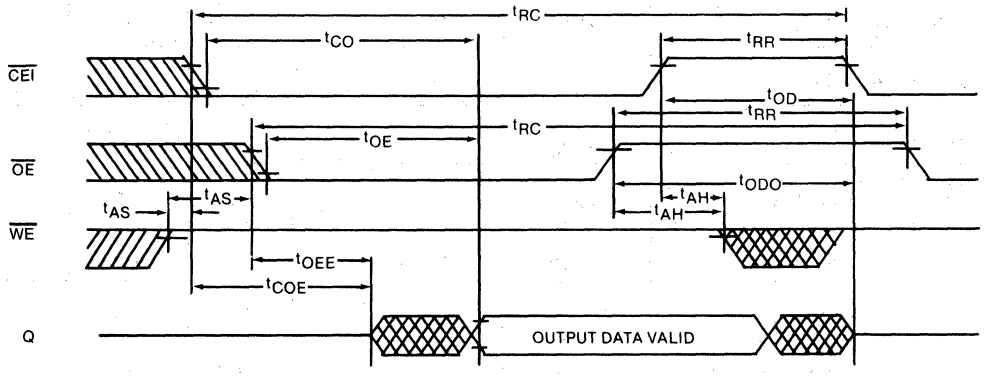
A.C. ELECTRICAL CHARACTERISTICS ROM/$\overline{\text{RAM}}$ = V_{CCO} (0 °C to 70 °C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{\text{CE}}$I Access Time	t_{CO}			200	ns	
$\overline{\text{OE}}$ Access Time	t_{OE}			200	ns	
$\overline{\text{CE}}$I to Output in Low Z	t_{COE}	10			ns	
$\overline{\text{OE}}$ to Output in Low Z	t_{OEE}	10			ns	
$\overline{\text{CE}}$I to Output in High Z	t_{OD}			100	ns	
$\overline{\text{OE}}$ to Output in High Z	t_{ODO}			100	ns	
Address Set Up Time	t_{AS}	20			ns	
Address Hold Time	t_{AH}			10	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
$\overline{\text{CE}}$I Pulse Width	t_{CW}	170			ns	
$\overline{\text{OE}}$ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Set Up Time	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
$\overline{\text{RST}}$ Pulse Width	t_{RST}	200			ns	
$\overline{\text{CE}}$I Propagation Delay	t_{PD}	5	10	20	ns	2,3
$\overline{\text{CE}}$I High to Power Fail	t_{PF}			0	ns	

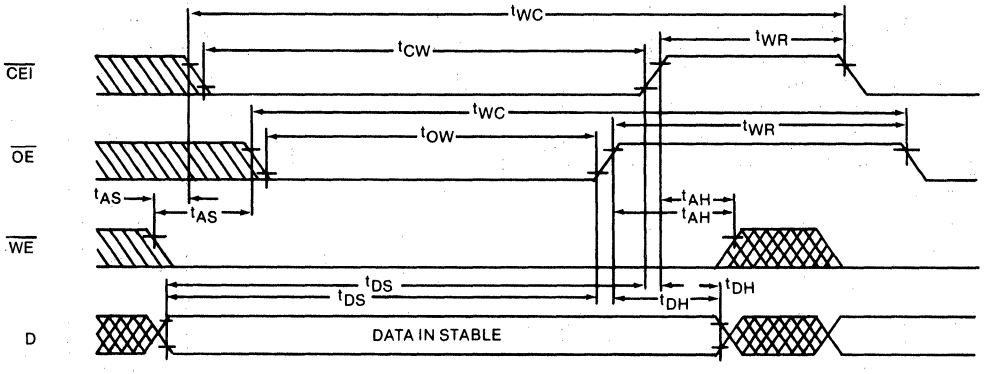
(0 °C to 70 °C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 -3V	t_F	0			ms	

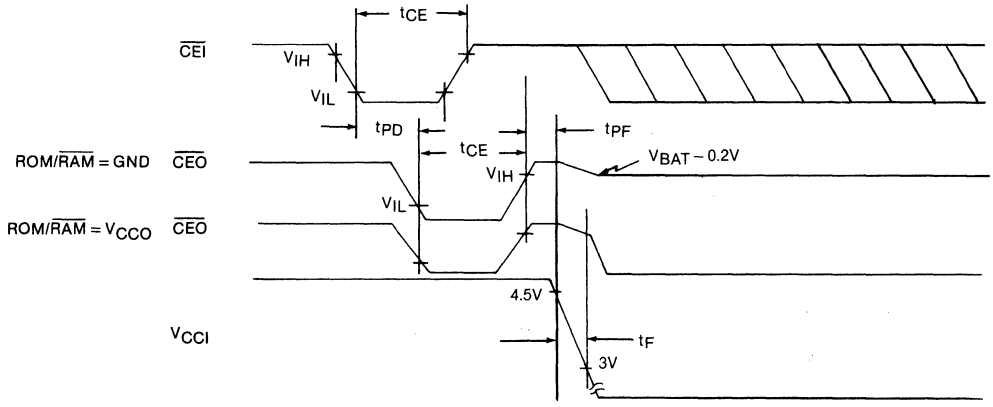
TIMING DIAGRAM—READ CYCLE ROM/$\overline{\text{RAM}}$ = V_{CCO}



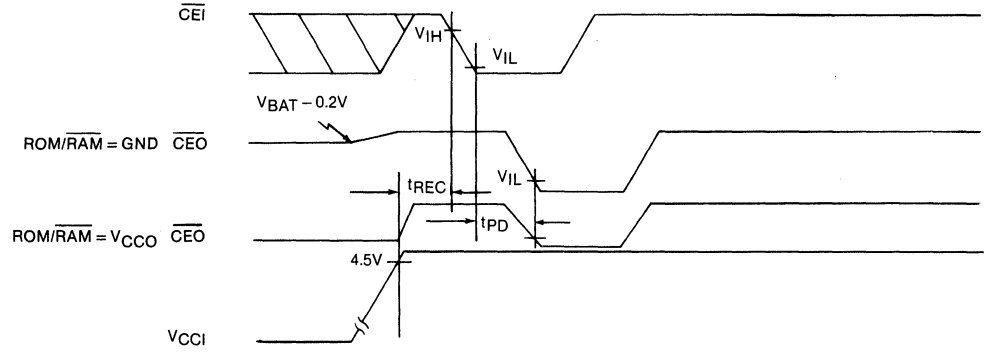
TIMING DIAGRAM—WRITE CYCLE ROM/$\overline{\text{RAM}}$ = V_{CCO}



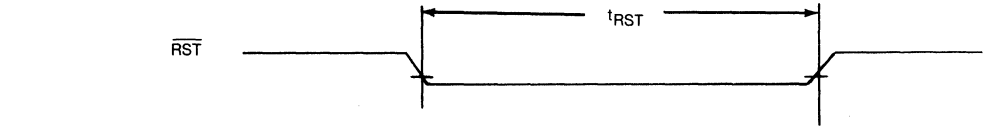
TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP



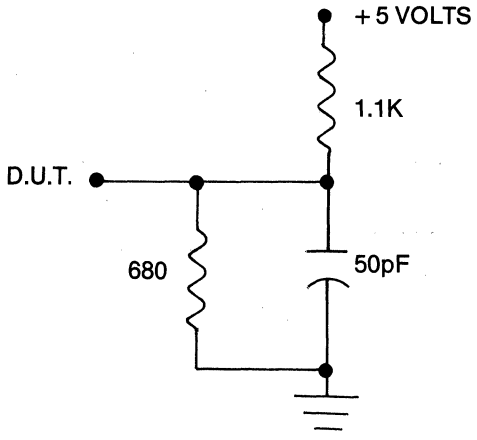
TIMING DIAGRAM—RESET FOR TIMECHIP



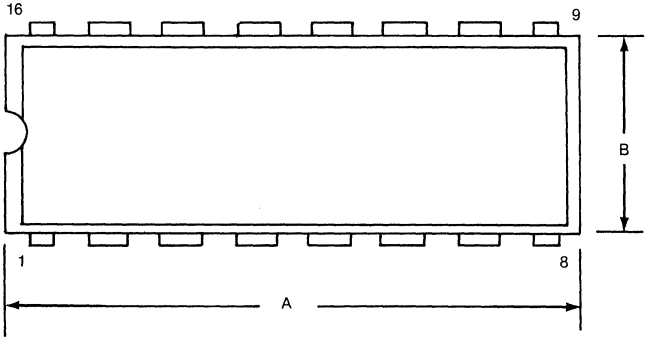
NOTES

1. All voltages are referenced to ground.
2. Measured with load shown in Figure 6.
3. Input pulse rise and fall times equal 10 ns.
4. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
5. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
6. Measured without RAM connected.
7. Trip point voltage for power fail detect. $V_{TP} = 1.26 \times V_{BAT}$ For 10% operation $V_{BAT} = 3.5V$ max.; for 5% operation $V_{BAT} = 3.7V$ max.
8. I_{CCO1} is the maximum average load current the DS1215 can supply to memory.
9. Applies to $\overline{CEO}$ with the ROM/$\overline{RAM}$ pin grounded. When the ROM/$\overline{RAM}$ pin is connected to V_{CCO}, $\overline{CEO}$ will go to a low level as V_{CCI} falls below V_{BAT}.
10. I_{CCO2} is the maximum average load current which the DS1215 can supply to memory in the battery backup mode.
11. Applies to all input pins except $\overline{RST}$. $\overline{RST}$ is pulled internally to V_{CCI}.

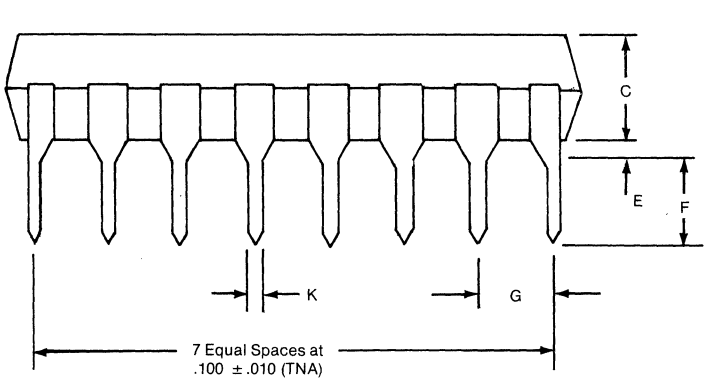
OUTPUT LOAD Figure 6

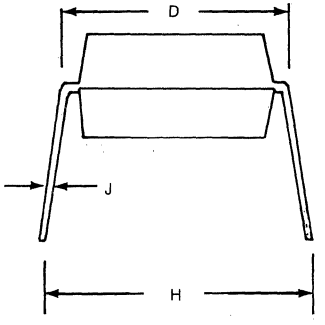


DS1215
TimeChip
16-Pin DIP



DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021





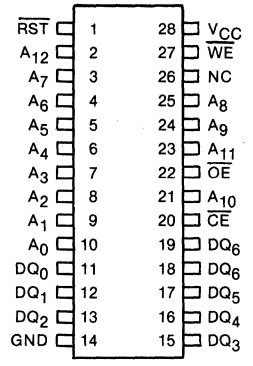
Dallas Semiconductor
Clock Plus 64K NV SRAM

DS1243Y

FEATURES

- Real Time Clock keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- 8K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min/month @25°C
- Over 5 years of data retention in the absence of power
- Unlimited write cycles

PIN CONNECTIONS

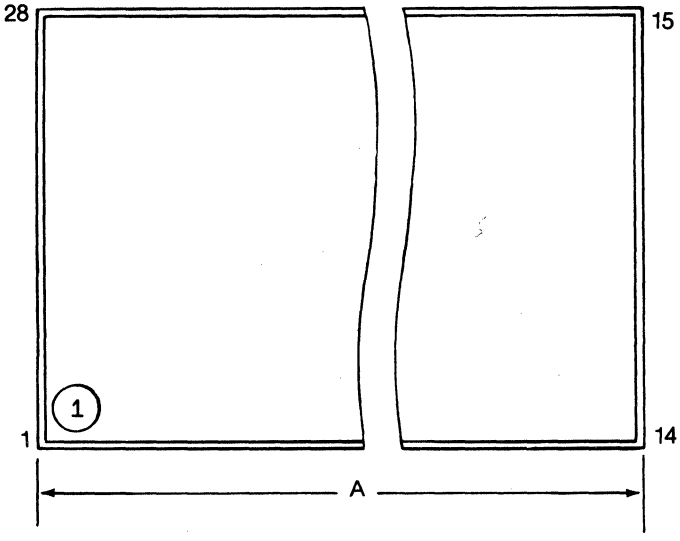


PIN NAMES

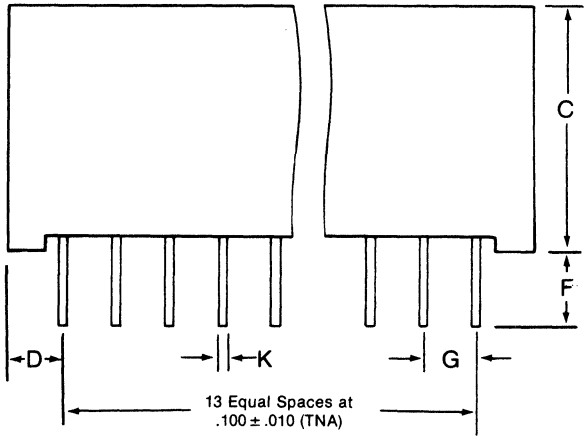
A_0-A_{12}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
NC	- No Connect
$\overline{RST}$	- Reset

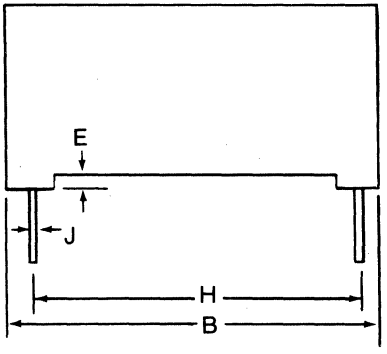
DESCRIPTION

The DS1243Y is a fully static nonvolatile RAM (organized as 8192 words by 8 bits) with built-in Real Time Clock. This memory and real time clock has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock. For complete information and operation, electrical characteristics, and timing as it relates to the 8K x 8 nonvolatile memory, please reference the DS1225Y data sheet. For complete information on operation, access control, electrical characteristics and timing of the real time clock, reference the DS1216 data sheet.



DIM.	INCHES	
	MIN.	MAX.
A	1.520	1.540
B	.695	.720
C	.395	.410
D	.090	.120
E	.020	.030
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





Dallas Semiconductor
Watchdog Timekeeper

PRELIMINARY
DS1284 28-Pin DIP
DS1284Q 28-Pin PLCC

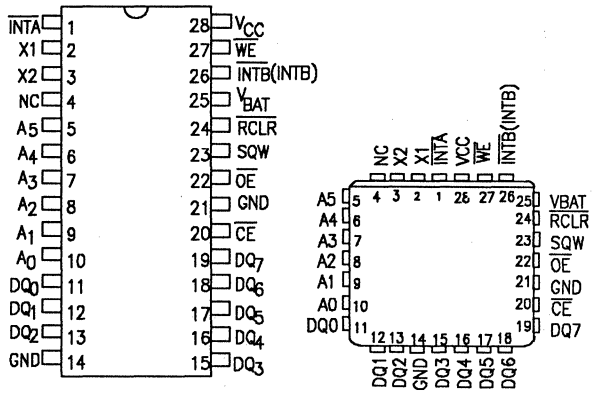
FEATURES

- Watchdog Timekeeper keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months and years
- Watchdog Timer restarts an out of control processor
- Alarm function schedules real time related activities
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than 1 minute/month at 25° C
- 50 bytes of user NV RAM
- Optional 28-pin PLCC surface mount package
- Low power CMOS circuitry is maintained on less than 0.5 uA when power is supplied from battery input

DESCRIPTION

The DS1284 Watchdog Timekeeper is a self contained real time clock, alarm, Watchdog Timer, and interval timer in a 28-pin JEDEC DIP package or a 28-pin PLCC surface mount package. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other that X1, X2, V_{BAT}, and $\overline{RCLR}$, see the DS1286 data sheet.

PIN DESCRIPTION



PIN NAMES

$\overline{INTA}$	- Interrupt Output A
INTB(INTB)	- Interrupt Output B
A0-A5	- Address Inputs
DQ0-DQ7	- Data Input/Output
$\overline{CE}$	- Chip Enable
$\overline{OE}$	- Output Enable
$\overline{WE}$	- Write Enable
Vcc	- +5 Volts
GND	- Ground
N.C.	- No Connection
SQW	- Square Wave Output
X1,X2	- 32.768 KHz Crystal Connections
V_{BAT}	- +3 Volt Battery Input
$\overline{RCLR}$	- RAM Clear

PIN DESCRIPTION

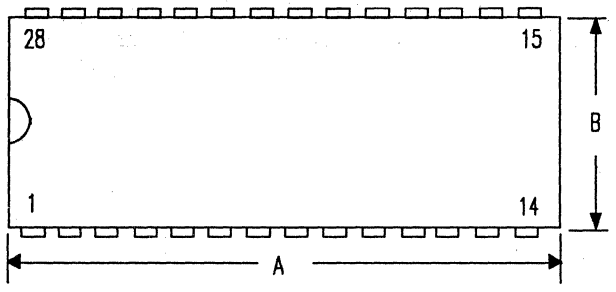
X1, X2 - Connections for a standard 32.768 KHz quartz crystal, Daiwa part part no. DT-26S, Seiko part no. DS-VT-200 or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6 pF. A trimming capacitor can be used to trim in the oscillator frequency.

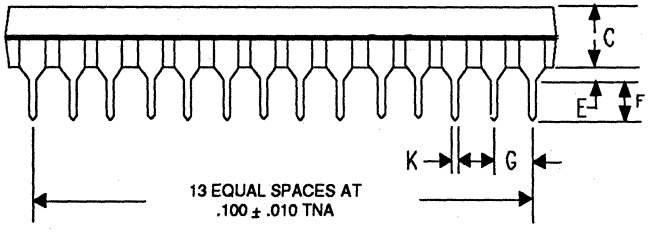
V_{BAT} - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.4 and 4 volts for proper operation. The nominal write protect trip point voltage at which access to registers containing time, watchdog, alarm, and RAM information is denied is set by internal circuitry as 1.26 x V_{BAT}. A maximum load of 0.5 uA at 25°C in the absence of power should be used to size the external energy source. An optional ground pin is provided for connection to battery negative. This pin should be grounded but can be left floating.

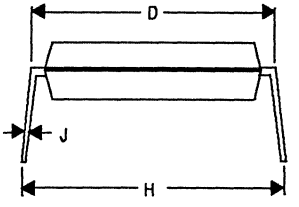
$\overline{RCLR}$ - The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of user NVRAM but does not effect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (-0.3 to 0.8 volts) during battery backup mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground or by switch) and not be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

DS1284 28-Pin DIP
WATCHDOG TIMEKEEPER

DIM.	INCHES	
	MIN.	MAX.
A	1.440	1.480
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.620	.670
J	.008	.012
K	.015	.021

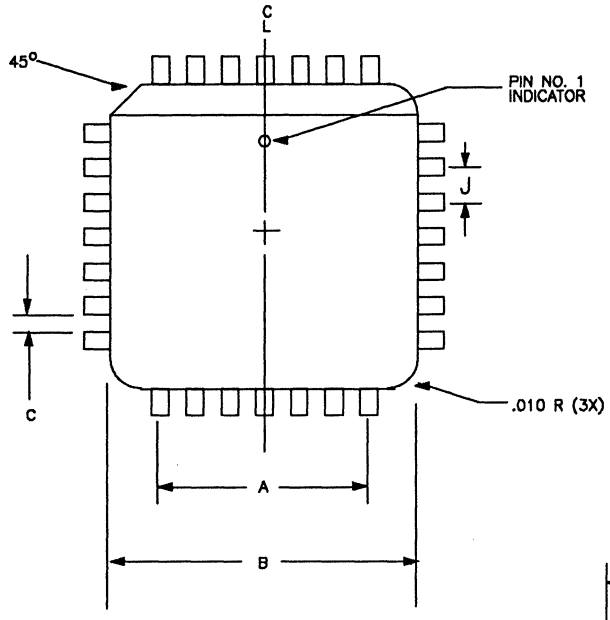


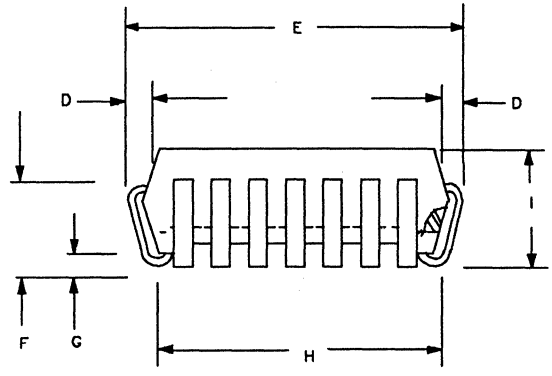




DS1284Q 28-Pin PLCC
WATCHDOG TIMEKEEPER

DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
I	.165	.180





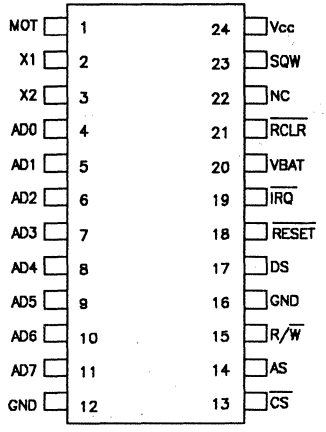
Dallas Semiconductor
Real Time Clock

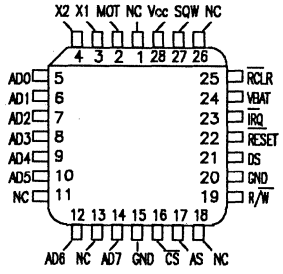
DS1285 24-Pin DIP
DS1285Q 28-Pin PLCC

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin configuration closely matches MC146818A
- Counts seconds, minutes, hours, days, day of the week, date, month and year with leap year compensation
- Binary or BCD representation of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122us to 500ms
  - End of clock update cycle
- Optional 28 pin PLCC surface mount package

PIN CONNECTIONS





PIN NAMES

AD0-AD7- Multiplexed Address/Data Bus
N.C. - No Connection
MOT - Bus Type Selection
$\overline{CS}$ - Chip Select
AS - Address Strobe
$R/\overline{W}$ - Read/Write Input
$\overline{DS}$ - Data Strobe
$\overline{RESET}$ - Reset Input
$\overline{IRQ}$ - Interrupt Request Output
SQW - Square Wave Output
Vcc - +5 Volt Supply
GND - Ground
X1,X2 - 32.768 KHz Crystal Connections
V_{BAT} - +3 volt Battery Input
$\overline{RCLR}$ - RAM Clear

DESCRIPTION

The DS1285 Real Time Clock Plus RAM is designed as a direct replacement for the MC146818A in IBM AT computer clock/calendar and other applications. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1,X2, V_{BAT}, and RCLR, see the DS1287 data sheet.

PIN DESCRIPTION

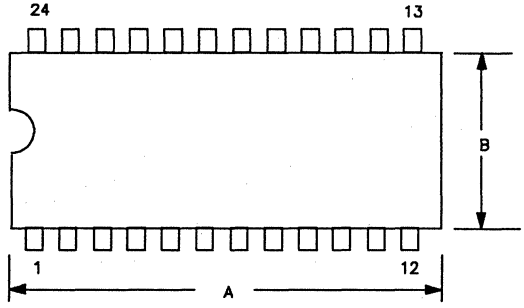
X1,X2 - Connections for a standard 32.768 KHz quartz crystal, Daiwa part number DT-26S or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. A variable triming capacitor may be required for extremely high precision timekeeping applications.

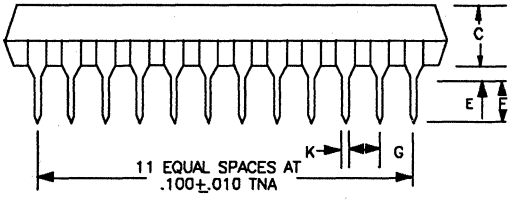
V_{BAT} - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2 and 4 volts for proper operation. The nominal write protect trip point voltage at which access to the Real Time Clock and User RAM is denied is set by the internal circuitry as 1.26 x V_{BAT}. A maximum load of .5uA at 25°C in the absence of power should be used to size the external energy source.

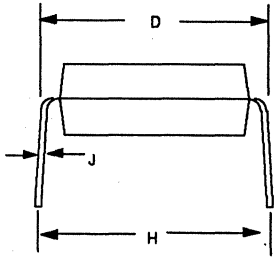
$\overline{RCLR}$ - The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not effect the RAM associated with the Real Time Clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (-0.3 to 0.8 volts) during battery back up mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up.

DS1285
REAL TIME CLOCK PLUS RAM
24-PIN DIP

DIM.	INCHES	
	MIN.	MAX.
A	1.240	1.280
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.620	.670
J	.008	.012
K	.015	.021

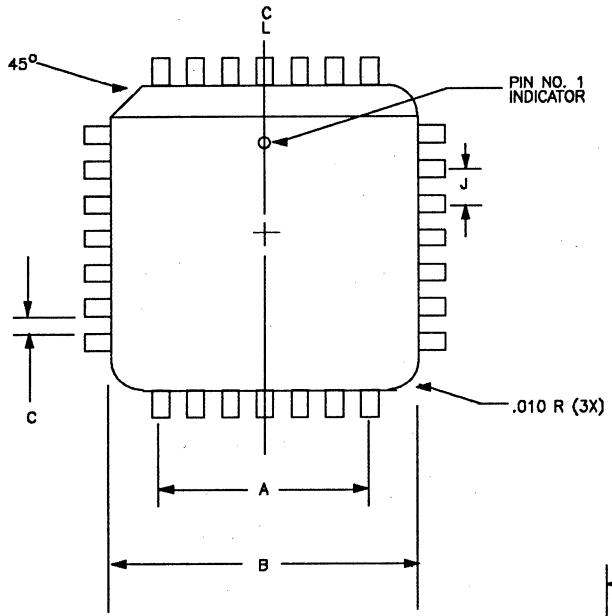


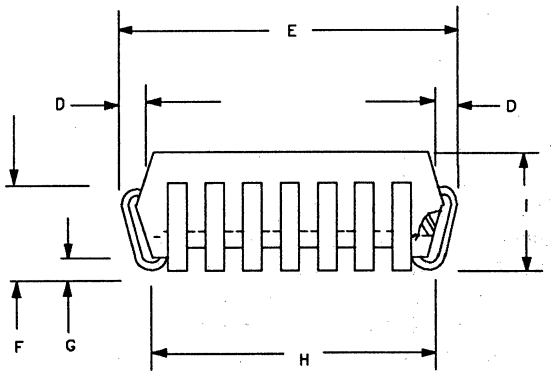




DS1285Q
REAL TIME CLOCK PLUS RAM
28-PIN PLCC

DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
I	.165	.180





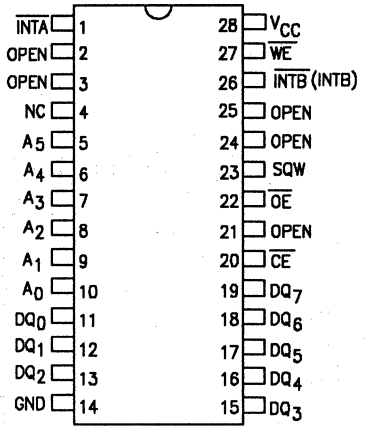
Dallas Semiconductor
WATCHDOG TIMEKEEPER

PRELIMINARY
DS1286

FEATURES

- Watchdog Timekeeper keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months and years
- Watchdog Timer restarts an out of control processor
- Alarm function schedules real time related activities
- Embedded lithium energy cell maintains time, Watchdog, user RAM and alarm information
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than 1 minute/month at 25° C
- Greater than 10 years of timekeeping in the absence of Vcc
- 50 bytes of user NV RAM

PIN DESCRIPTION



PIN NAMES

INTA	- Interrupt Output A
INTB(INTB)	- Interrupt Output B
A0-A5	- Address Inputs
DQ0-DQ7	- Data Input/Output
CE	- Chip Enable
OE	- Output Enable
WE	- Write Enable
Vcc	- +5 Volts
GND	- Ground
N.C.	- No Connection
OPEN	- Pin Missing
SQW	- Square Wave Output

DESCRIPTION

The DS1286 Watchdog Timekeeper is a self contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package. The DS1286 contains an embedded lithium energy source and a quartz crystal which eliminates need for any external circuitry. Data contained within 64 eight bit registers can be read or written in the same manner as bytewide static RAM. Data is maintained in the Watchdog Timekeeper by intelligent control circuitry which detects the status of Vcc and write protects memory when Vcc is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of Vcc. The Watchdog Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Watchdog Timekeeper operates in either 24 hour or 12 hour format with an AM/PM indicator. The Watchdog timer provides alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week.

OPERATION - READ REGISTERS

The DS1286 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (High) and $\overline{CE}$ and $\overline{OE}$ are active (LOW). The unique address specified by the six address inputs (A0-A5) defines which of the 64 registers is to be accessed. Valid data will be available to the eight data output drivers within t_{Acc} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE REGISTERS

The DS1286 is in the write mode whenever the $\overline{WE}$ (Write Enable) and $\overline{CE}$ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. The $\overline{OE}$ control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

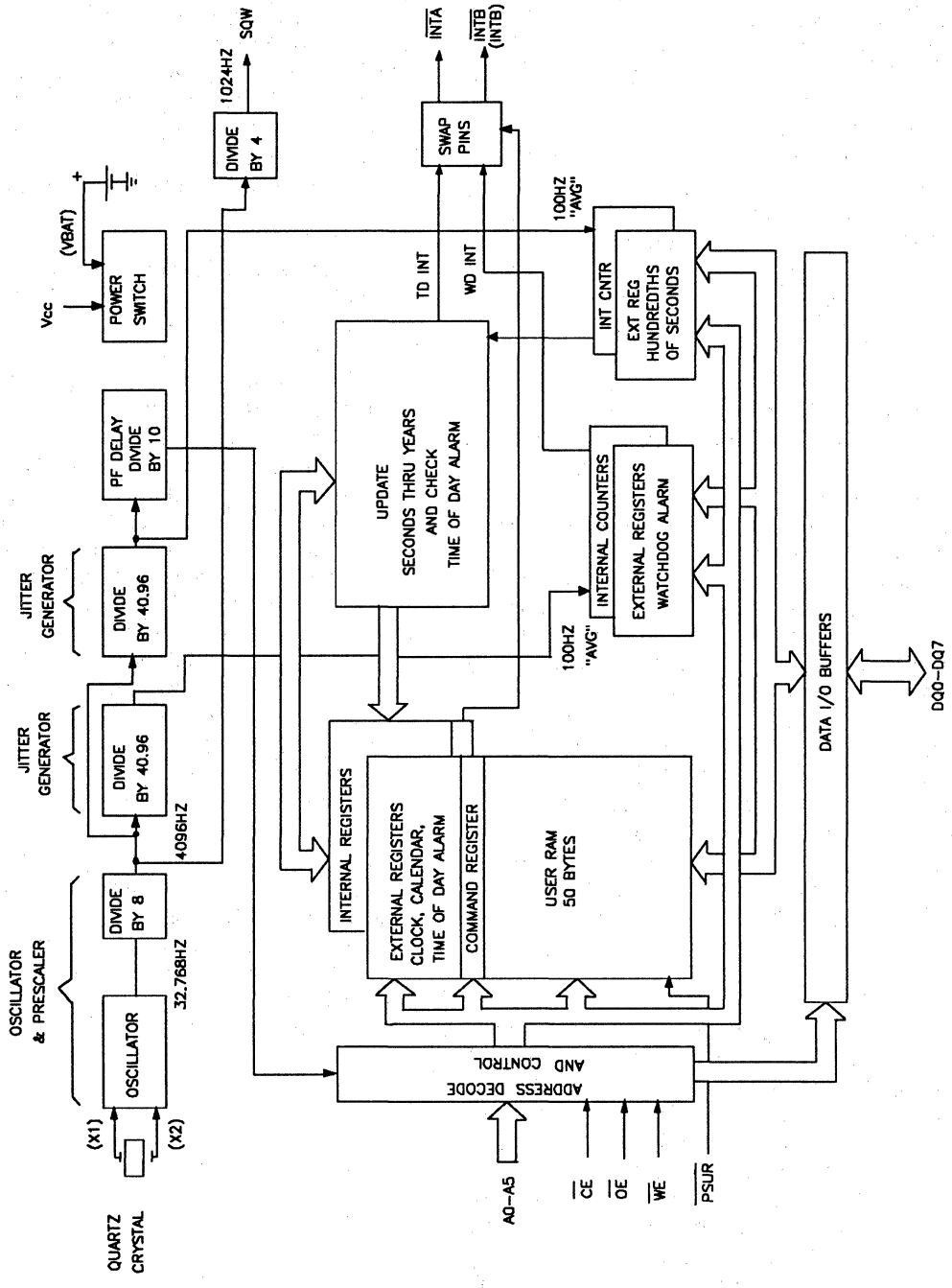
DATA RETENTION

The Watchdog Timekeeper provides full functional capability when Vcc is greater than 4.5 volts and write protects the register contents at 4.25 volts typical. Data is maintained in the absence of Vcc without any additional support circuitry. The DS1286 constantly monitors Vcc. Should the supply voltage decay, the Watchdog TimeKeeper will automatically write protect itself and all inputs to the registers become Don't Care. The two interrupts $\overline{INTA}$ and $\overline{INTB}$ (INTB) and the internal clock and timers continue to run regardless of the level of Vcc. As Vcc falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power up, when Vcc rises above approximately 3.0 volts, the power switching circuit connects external Vcc and disconnects the internal lithium energy source. Normal operation can resume after Vcc exceeds 4.5 volts for a period of 150 ms.

WATCHDOG TIMEKEEPER REGISTERS

The Watchdog Timekeeper has 64 registers which are eight bits wide that contain all of the Timekeeping, Alarm, Watchdog, Control, and Data information. The Clock, Calendar, Alarm and Watchdog Registers are memory locations which contain external (user accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 50 bytes of RAM registers can only be accessed from the external address and data bus. Register 0, 1, 2, 4, 6, 8, 9 and A contain time of day and date information (see Figure 2). Time of Day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Register C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Register E through Register 3F are user bytes and can be used to contain data at the user's discretion.

BLOCK DIAGRAM Figure 1



TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9 and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logical zero, $\overline{EOSC}$ (Bit 7) enables the Real Time Clock oscillator. This bit is set to logical one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (pin 24). When set to logical zero, the Square Wave Output Pin will output a 1024 HZ Square Wave Signal. When set to logic one the Square Wave Output Pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12 or 24 Hour Select Bit. When set to logic one, the 12 Hour Format is selected. In the 12 Hour Format, Bit 5 is the AM/PM Bit with logical one being PM. In the 24 Hour Mode, Bit 5 is the Second 10 Hour bit (20-23 hours). The Time of Day Registers are updated every .01 seconds from the Real Time Clock, except when the TE bit (Bit 7 of Register B) is set low or the clock oscillator is not running.

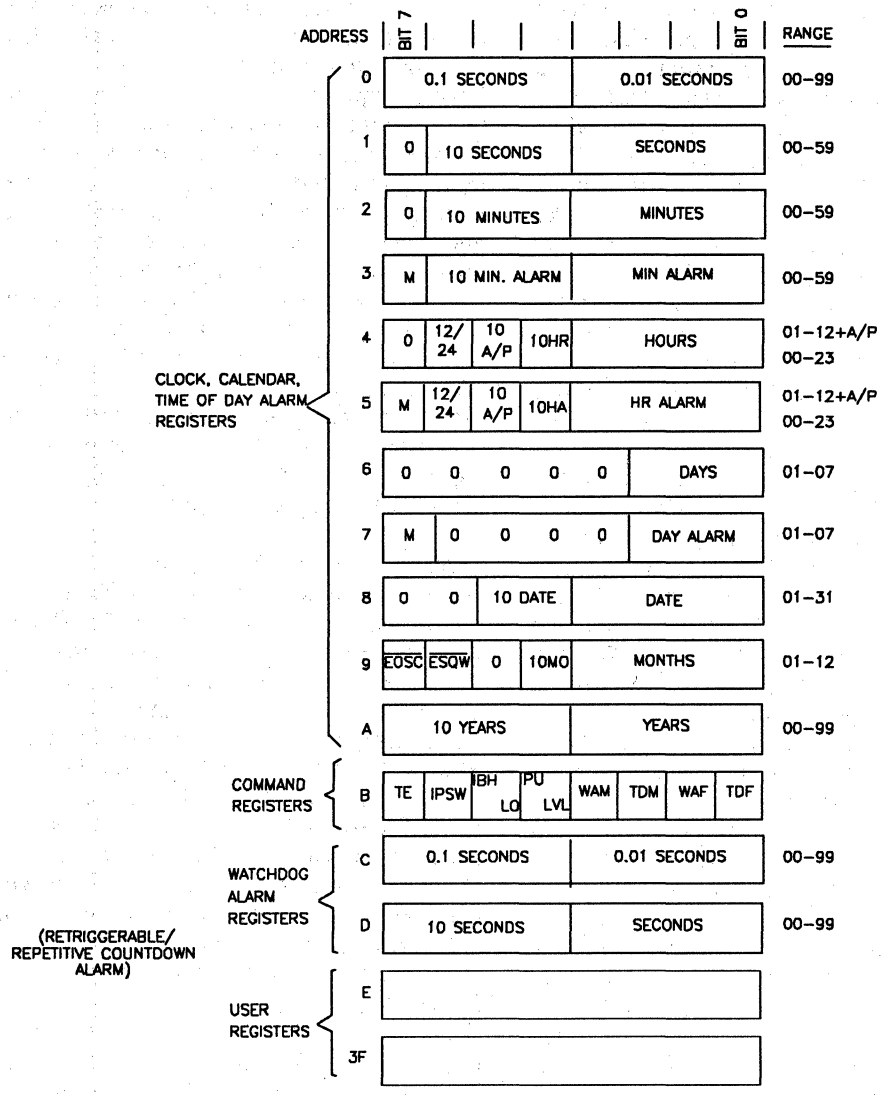
The preferred method of synchronizing data access to and from the Watchdog Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic zero. This will freeze the External Time of Day Registers at the present recorded time allowing access to occur without danger of simultaneous update. When the watch registers have been read or written a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day Registers back to being updated every .01 second. No time is lost in the Real Time Clock because the internal copy of the Time of Day Register buffers are continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day Registers is to ignore synchronization. However, any single read may give erroneous data as the Real Time Clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented and Time of Day Alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the Watchdog Timekeeper.

TIME OF DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logical zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when Bit 7 of Register 7 is set to a logical one. Similarly, an alarm is generated every hour when Bit 7 of Registers 7 and 5 is set to a logical 1. When Bit 7 of Registers 7, 5, and 3 is set to a logical 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm Registers are read or written.

DS1286 WATCHDOG TIMEKEEPER REGISTERS Figure 2



TIME OF DAY ALARM MASK BITS Figure 3

MINUTES	HOURS	DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from ever going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual count down register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

COMMAND REGISTER

Address location 0B is the Command Register where mask bits, control bits, and flag bits reside. Bit 0 is the Time of Day Alarm Flag (TDF). When this bit is set internally to a logical one, an alarm has occurred. The time of the alarm can be determined by reading the Time of Day Alarm Registers. However, if the transfer enable bit is set to logical zero the Time of Day registers may not reflect the exact time that the alarm occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm Registers are read. Bit 1 is the Watchdog Alarm Flag (WAF). When this bit is set internally to a logical one, a Watchdog Alarm has occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm Registers are accessed. Bit 2 of the Command Register contains the Time of Day Alarm Mask Bit (TDM). When this bit is written to a logical one, the Time of Day Alarm Interrupt Output is deactivated regardless of the value of the Time of Day Alarm Flag. When TDM is set to logical zero, the Time of Day Interrupt Output will go to the active state which is determined by bits 0, 4, 5, and 6 of the Command Register. Bit 3 of the Command Register contains the Watchdog Alarm Mask Bit (WAM). When this bit is written to a logical one, the Watchdog Interrupt Output is deactivated regardless of the value in the Watchdog Alarm Registers. When WAM is set to logic zero, the Watchdog Interrupt Output will go to the active state which is determined by bits 1, 4, 5, and 6 of the Command Register. These four bits define how Interrupt Output Pins $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ (INTB) will be operated. Bit 4 of the Command Register determines whether both interrupts will output a pulse or level when activated. If Bit 4 is set to logic one, the pulse mode is selected and $\overline{\text{INTA}}$ will sink current for a minimum of 3 ms and then release. Output $\overline{\text{INTB}}$ (INTB) will either sink or source current for a minimum of 3 ms depending on the level of Bit 5. When Bit 5 is set to logic one, the B interrupt will source current. When Bit 5 is set to logical zero, the B interrupt will sink current. Bit 6 of the Command Register directs which type of interrupt will be present on interrupt pins $\overline{\text{INTA}}$ or $\overline{\text{INTB}}$ (INTB). When set to logical one, $\overline{\text{INTA}}$ becomes the Time of Day Alarm Interrupt Pin and $\overline{\text{INTB}}$ (INTB) becomes the Watchdog Interrupt Pin. When Bit 6 is set to logical zero, the interrupt functions are reversed such that the Time of Day Alarm will be output on $\overline{\text{INTB}}$ (INTB) and the Watchdog Interrupt will be output on $\overline{\text{INTA}}$. Caution should be exercised when dynamically setting this bit as the interrupts will be reversed even if in an active state. Bit 7 of the Command Register is for Transfer Enable (TE). The function of this bit is described in the Time of Day Registers.

ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON ANY PIN RELATIVE TO GROUND -0.3V TO +7.0V
OPERATING TEMPERATURE 0°C TO 70°C
STORAGE TEMPERATURE -40°C TO +70°C
SOLDERING TEMPERATURE 260°C FOR 10 SEC.

RECOMMENDED D.C. OPERATING CONDITIONS

(0° C to 70° C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{cc}	4.5	5.0	5.5	V	10
INPUT LOGIC 1	V_{IH}	2.2		V_{cc} + 0.3	V	10
INPUT LOGIC 0	V_{IL}	-0.3		+0.8	V	10

D.C. ELECTRICAL CHARACTERISTICS

(0° C to 70° C, Vcc =5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT	I_{IL}	-1.0		+1.0	uA	
OUTPUT LEAKAGE CURRENT	I_{LO}	-1.0		+1.0	uA	
I/O LEAKAGE CURRENT	I_{LIO}	-1.0		+1.0	uA	
OUTPUT CURRENT @ 2.4V	I_{OH}	-1.0			mA	
OUTPUT CURRENT @ 0.4V	I_{OL}	2.0			mA	13
STANDBY CURRENT $\overline{CE}$= 2.2V	I_{CCS1}		3.0	7.0	mA	
STANDBY CURRENT $\overline{CE} \geq$ Vcc -0.5	I_{CCS2}			4.0	mA	
ACTIVE CURRENT	I_{CC}			15	mA	
WRITE PROTECTION VOLTAGE	V_{TP}		4.25		V	

CAPACITANCE

(T_A=25° C)

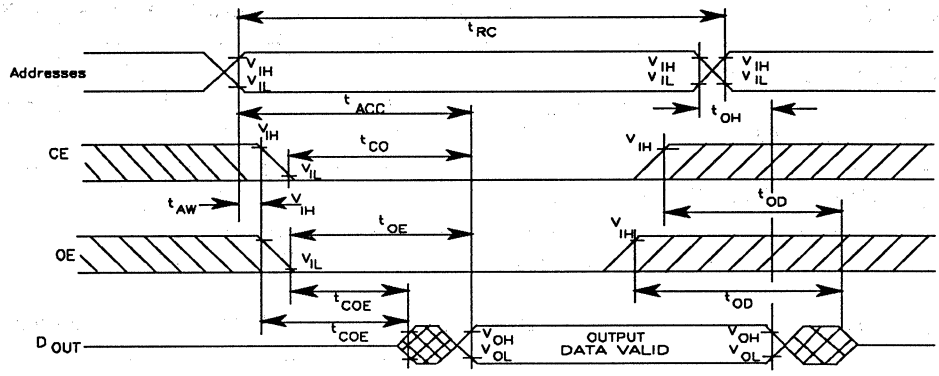
PARAMETER	SYMBOL	TYP.	MAX	UNITS	NOTES
INPUT CAPACITANCE	C_{IN}	7	10	pF	
OUTPUT CAPACITANCE	C_{OUT}	7	10	pF	
INPUT/OUTPUT CAPACITANCE	$C_{I/O}$	7	10	pF	

A.C. ELECTRICAL CHARACTERISTICS

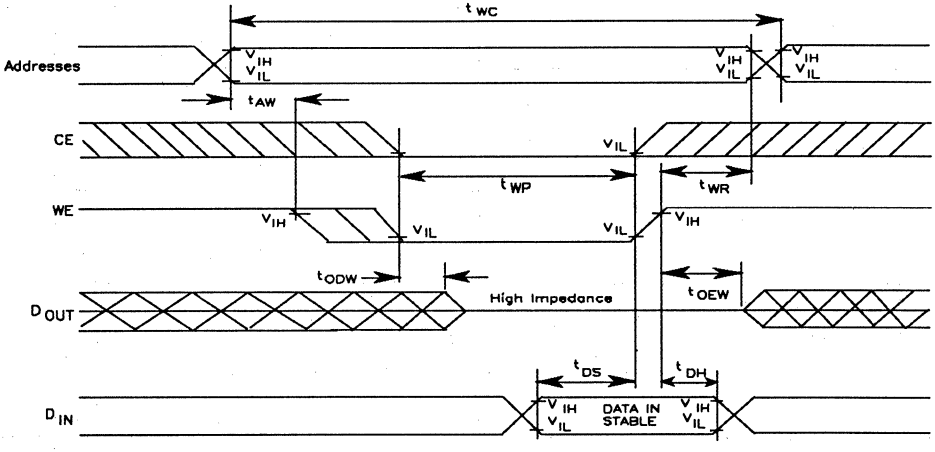
(0° C to 70° C, Vcc = 4.5v to 5.5v)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
READ CYCLE TIME	t_{RC}	150			ns	1
ADDRESS ACCESS TIME	t_{ACC}			150	ns	
$\overline{CE}$ ACCESS TIME	t_{CO}			150	ns	
$\overline{OE}$ ACCESS TIME	t_{OE}			75	ns	
$\overline{OE}$ OR $\overline{CE}$ TO OUTPUT ACTIVE	t_{COE}	10			ns	
OUTPUT HIGH Z FROM DESELECT	t_{OD}			75	ns	
OUTPUT HOLD FROM ADDRESS CHANGE	t_{OH}	10			ns	
WRITE CYCLE TIME	t_{WC}	150			ns	
WRITE PULSE WIDTH	t_{WP}	140			ns	3
ADDRESS SETUP TIME	t_{AW}	0			ns	
WRITE RECOVERY TIME	t_{WR}	10			ns	
OUTPUT HIGH Z FROM $\overline{WE}$	t_{ODW}			50	ns	
OUTPUT ACTIVE FROM $\overline{WE}$	t_{OEW}	10			ns	
DATA SETUP TIME	t_{DS}	60			ns	4
DATA HOLD TIME	t_{DH}	0			ns	4,5
$\overline{INTA}$, $\overline{INTB}$ PULSE WIDTH	t_{IPW}	3			ms	11,12

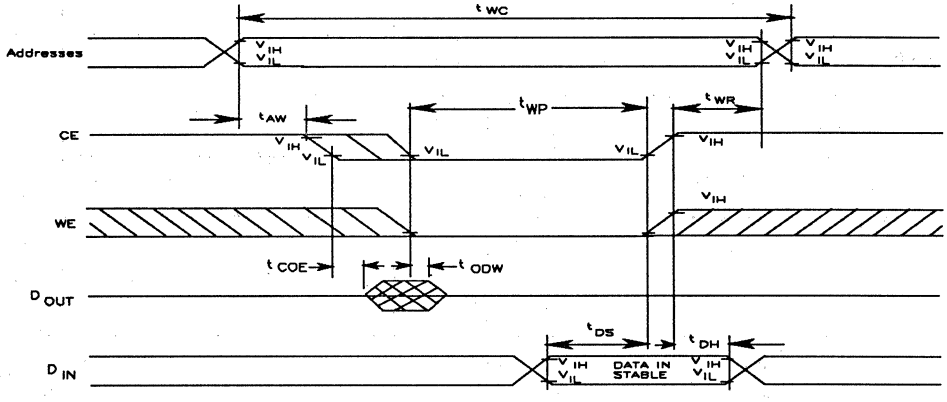
READ CYCLE (1)



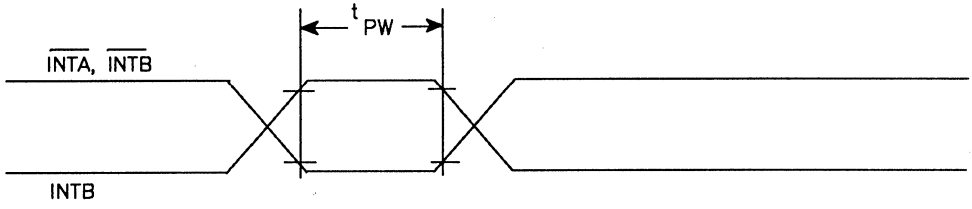
WRITE CYCLE 1 (2), (6), (7)



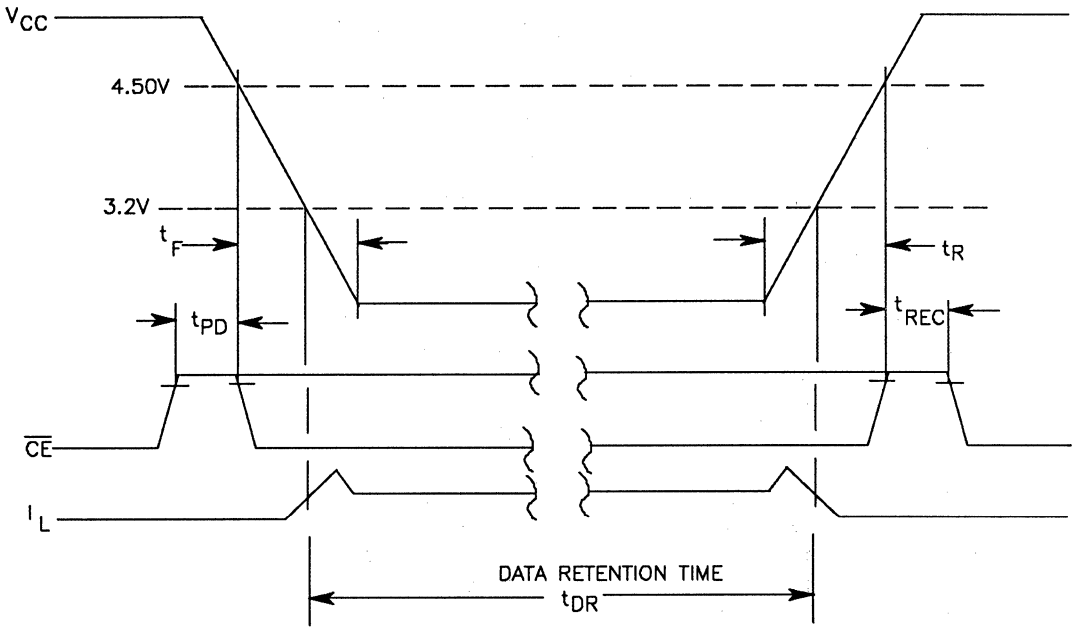
WRITE CYCLE 2 (2), (8)



TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



POWER-DOWN/POWER-UP CONDITION



LEAKAGE CURRENT I_L SUPPLIED FROM LITHIUM CELL

POWER-UP/POWER-DOWN CONDITION

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at VIH before Power Down	0		us	
t_F	VCC slew from 4.5V to 0V ($\overline{CE}$ at VIH)	350		us	
t_R	VCC slew from 0V to 4.5V ($\overline{CE}$ at VIH	100		us	
t_{REC}	$\overline{CE}$ at VIH after Power Up		150	ms	

(t_A=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

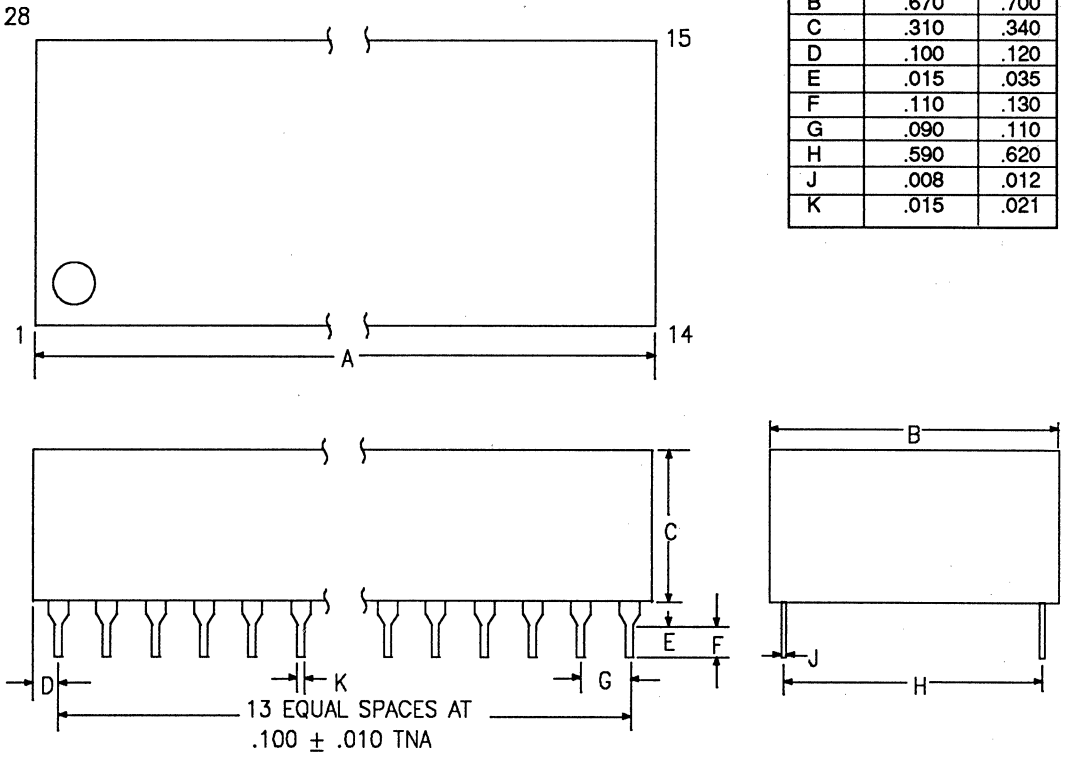
1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the Output Buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "and" of the $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} or t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle, then t_{DH} = 20 ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS1286 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt Output occurs within 100 ns on the alarm condition existing.
13. Both $\overline{INTA}$ and $\overline{INTB}$ (INTB) are open drain outputs.

A.C. TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

DS1286
WATCHDOG TIMEKEEPER

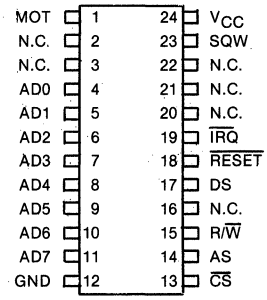
DIM.	INCHES	
	MIN	MAX
A	1.520	1.540
B	.670	.700
C	.310	.340
D	.100	.120
E	.015	.035
F	.110	.130
G	.090	.110
H	.590	.620
J	.008	.012
K	.015	.021



FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month and year with leap year compensation
- Binary or BCD representation of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 *u*s to 500 ms
  - End of clock update cycle

PIN CONNECTIONS



PIN NAMES

AD0 - AD7	-	Multiplexed Address/Data Bus
N.C.	-	No Connection
MOT	-	Bus Type Selection
$\overline{CS}$	-	Chip Select
AS	-	Address Strobe
R/$\overline{W}$	-	Read/Write Input
DS	-	Data Strobe
$\overline{RESET}$	-	Reset Input
$\overline{IRQ}$	-	Interrupt Request Output
SQW	-	Square Wave Output
V_{CC}	-	+5 Volt Supply
GND	-	Ground

DESCRIPTION

The DS1287 RealTime Clock Plus RAM is designed to be a direct replacement for the MC146818A. A lithium energy source, quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS1287 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The RealTime Clock Plus RAM is distinctive in that time-of-day and memory are maintained even in the absence of power.

OPERATION

The block diagram in Figure 1 shows the pin connection with the major internal functions of the DS1287 Real Time Clock Plus RAM. The following paragraphs describe the function of each pin.

POWER DOWN/POWER UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS1287 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin and DS1287 is, therefore, write-protected. When the DS1287 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and an internal Lithium energy source supplies power to the Real Time Clock and the RAM memory.

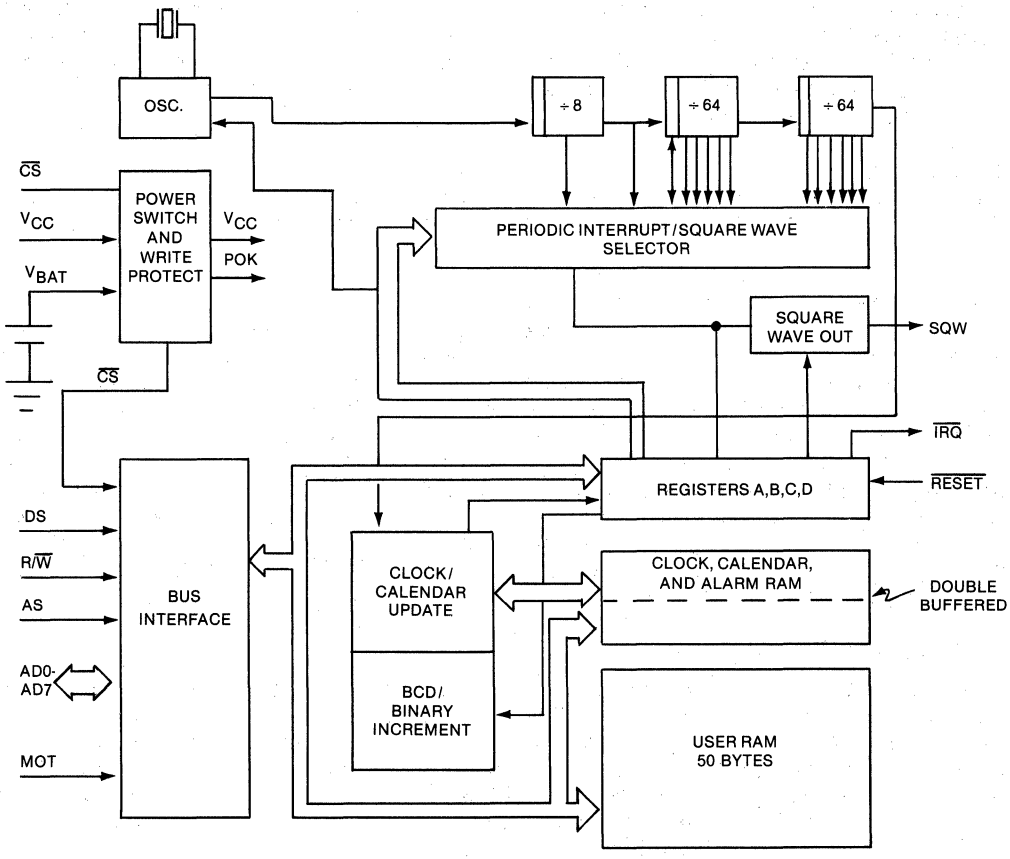
SIGNAL DESCRIPTIONS

GND, V_{CC}—D.C. power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts is applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and TimeKeeper are switched over to an internal Lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select)—The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 KΩ.

SQW (Square Wave Output)—The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin may be changed by programming Register A. As shown in Table 1, the SQW signal may be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

BLOCK DIAGRAM DS1287 Figure 1



PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 1

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 *us*	8.192 KHz
0	1	0	0	244.141 *us*	4.096 KHz
0	1	0	1	488.281 *us*	2.048 KHz
0	1	1	0	976.5625 *us*	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bi-Directional Address/Data Bus)—Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are presented during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1287 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS1287 latches the address from AD0 to AD5. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS1287 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

AS (Address Strobe Input)—A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS1287.

DS (Data Strobe or Read Input)—The DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS1287 is to drive the bi-directional bus. In write cycles the trailing edge of DS causes the DS1287 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read ($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS1287 drives the bus with read data. The $\overline{RD}$ signal is the same definition as the Output Enable ($\overline{OE}$) signal on a typical memory.

R/$\overline{W}$ (Read/Write Input)—The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active low signal called $\overline{WR}$. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{WE}$) on generic RAMs.

$\overline{CS}$ (Chip Select Input)—The Chip Select signal ($\overline{CS}$) must be asserted low for a bus cycle in which the DS1287 is to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the DS1287 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the Real Time Clock data and RAM data during power outages.

$\overline{IRQ}$ (Interrupt Request Output)—The $\overline{IRQ}$ pin is an active low output of the DS1287 that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices may be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pullup resistor.

RESET (Reset Input)—The $\overline{\text{RESET}}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{\text{RESET}}$ pin may be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{\text{RESET}}$ is held low is dependent on the application. However, if $\overline{\text{RESET}}$ is used on power up, the time $\overline{\text{RESET}}$ is low should exceed 200 ms to make sure that the internal timer which controls the DS1287 on power-up has timed out. When $\overline{\text{RESET}}$ is low and V_{CC} is above 4.25 volts, the following occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.
B. Alarm Interrupt Enable (AIE) bit is cleared to zero.
C. Update Ended Interrupt Flag (UF) bit is cleared to zero.
D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.
E. Periodic Interrupt Flag (PF) bit is cleared to zero.
F. The device is not accessible until $\overline{\text{RESET}}$ is returned high.
G. Alarm Interrupt Flag (AF) bit is cleared to zero.
H. $\overline{\text{IRQ}}$ pin is in the high impedance state.
I. Square Wave Output Enable ($\overline{\text{SQWE}}$) bit is cleared to zero.
J. Update Ended Interrupt Enable (UIE) is cleared to zero.

In a typical application $\overline{\text{RESET}}$ may be connected to V_{CC}. This connection will allow the DS1287 to go in and out of power fail without affecting any of the control registers.

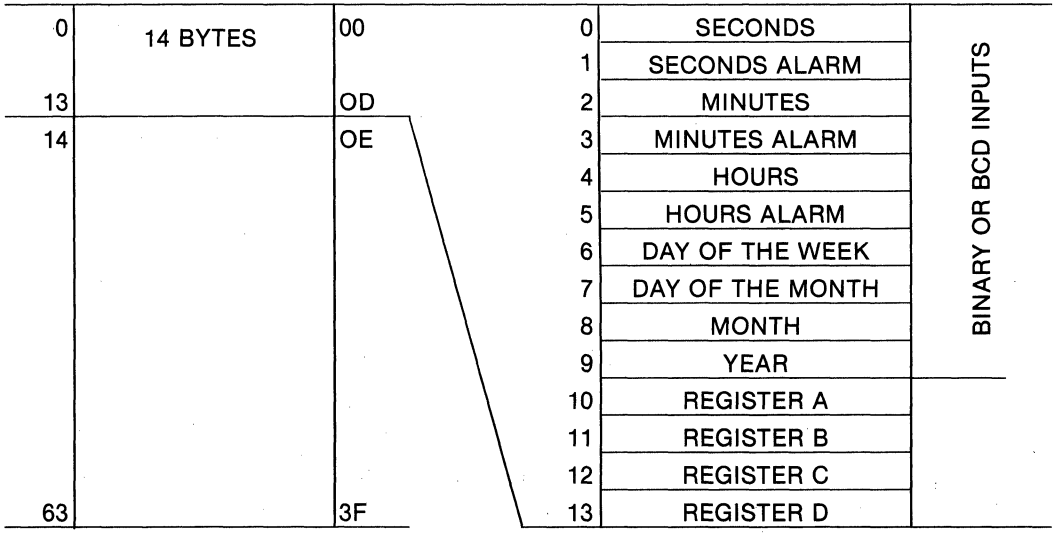
ADDRESS MAP

The Address Map of the DS1287 is shown in Figure 2. The address map consists of 50 bytes of user RAM, 10 bytes of RAM which contain the RTC time, calendar and alarm data, and 4 bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four control registers (A, B, C, and D) are described in the "Register" section.

ADDRESS MAP DS1287 Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar and alarm bytes may be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logical one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar and alarm registers in a selected format (Binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the Real Time Clock to update the time and calendar bytes. Once initialized, the Real Time Clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the Binary and BCD formats of the ten time, calendar and alarm locations. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists that seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

TIME CALENDAR AND ALARM DATA MODES Table 2

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours - 12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours - 24-hr Mode	0-23	00-17	00-23
5	Hours Alarm - 12-hr	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours Alarm - 24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

The three alarm bytes may be used in two ways. First, when the alarm time is written in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any

hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at Logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

NONVOLATILE RAM

The 50 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1287. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt may be programmed to occur at rates from once per second to once per day. The periodic interrupt may be selected for rates from 500 ms to 122 *u*s. The update-ended interrupt may be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a Logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to Logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two or three bits may be set when reading Register C. Each utilized flag bit should be examined when read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in Bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1287. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS
When the DS1287 is shipped from the factory, the internal oscillator is turned off. This feature prevents the Lithium energy cell from being used until it is installed in system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION
Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION
The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 *u*s. This function is separate from the alarm interrupt which may be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs,create output intervals, or await the next needed software function.

UPDATE CYCLE
The DS1287 executes an update cycle once per second regardless of the set bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information are consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

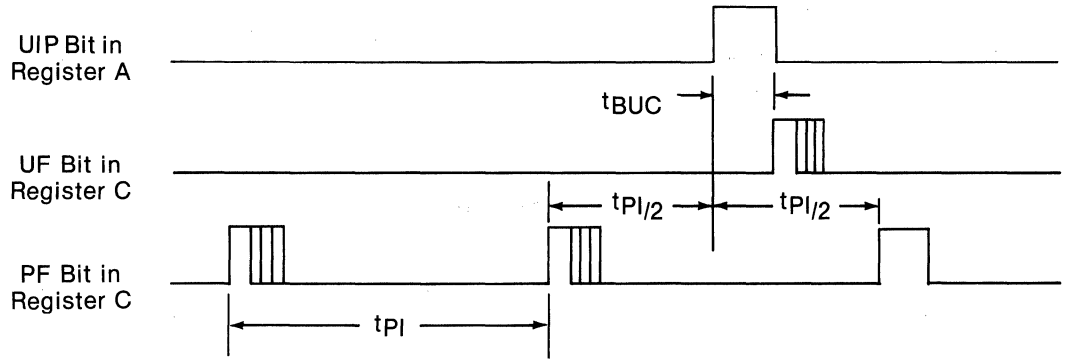
There are three methods which can be employed to handle access of the Real Time Clock which avoids any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 *u*s later. If a low is read on the UIP bit, the user has at least

244 *us* before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 *us*.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($T_{PI}/2+t_{BUC}$) to insure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.

t_{BUC} = Delay time before update cycle = 244 *us*.

REGISTERS

The DS1287 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP
The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 *us*. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a "1" inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2
These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits which will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1 and DV2.

RS3, RS2, RS1, RS0
These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user may do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

REGISTER B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET
When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit which is not modified by $\overline{\text{RESET}}$ or internal functions of the DS1287.

PIE
The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to cause the $\overline{\text{IRQ}}$ pin to be driven low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3 through RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1287 functions, but is cleared to zero on $\overline{\text{RESET}}$.

AIE
The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a one permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The $\overline{RESET}$ pin clears AIE to zero. The internal functions of the DS1287 do not affect the AIE bit.

UIE
The Update Ended Interrupt Enable (UIE) bit is a read/write bit which enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The $\overline{RESET}$ pin going low or the SET bit going high clears the UIE bit.

SQWE
When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the $\overline{RESET}$ pin. SQWE is a read/write bit.

DM
The Data Mode (DM) bit indicates whether time and calendar information are in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{RESET}$. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12
The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is a read/write and is not affected by internal functions or $\overline{RESET}$.

DSE
The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF
The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1

AF = AIE = 1

UF = UIE = 1

i.e., IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a one the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

PF
The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{RESET}$ or a software read of Register C.

AF
A one in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A $\overline{RESET}$ or a read of Register C will clear AF.

UF
The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or a $\overline{RESET}$.

BIT 0 THROUGH BIT 3
These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT
The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal Lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RESET}$.

BIT 6 THROUGH BIT 0
The remaining bits of Register D are not usable. They cannot be written and when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Input Logic 0	V_{IL}	−0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		7	15	mA	2
Input Leakage	I_{IL}	−1.0		+1.0	uA	3
I/O Leakage	I_{LO}	−1.0		+1.0	uA	4
Input Current	I_{MOT}	−1.0		+500	uA	3
Output @2.4V	I_{OH}	−1.0			mA	1,5
Output @0.4V	I_{OL}			4.0	mA	1

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

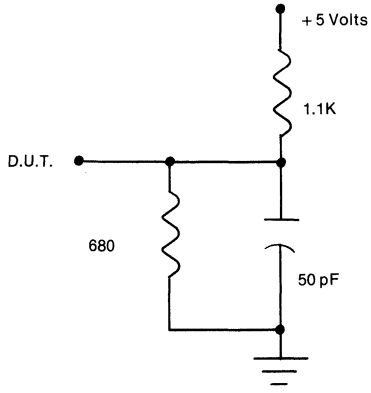
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		D.C.	ns	
Pulse Width, DS/E Low or RD/WR High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/WR Low	PW_{EH}	125			ns	
Input Rise and Fall Time	t_R, t_F			30	ns	
R/W Hold Time	t_{RWH}	10			ns	
R/W Set-Up Time Before DS/E	t_{RWS}	50			ns	
Chip Select Set-Up Time Before DS, WR or RD	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	25			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time From DS/E or RD	t_{DDR}	20		120	ns	6
Data Set-Up Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			*us*	
IRQ Release from DS	t_{IRDS}			2	*us*	
IRQ Release from RESET	t_{IRR}			2	*us*	

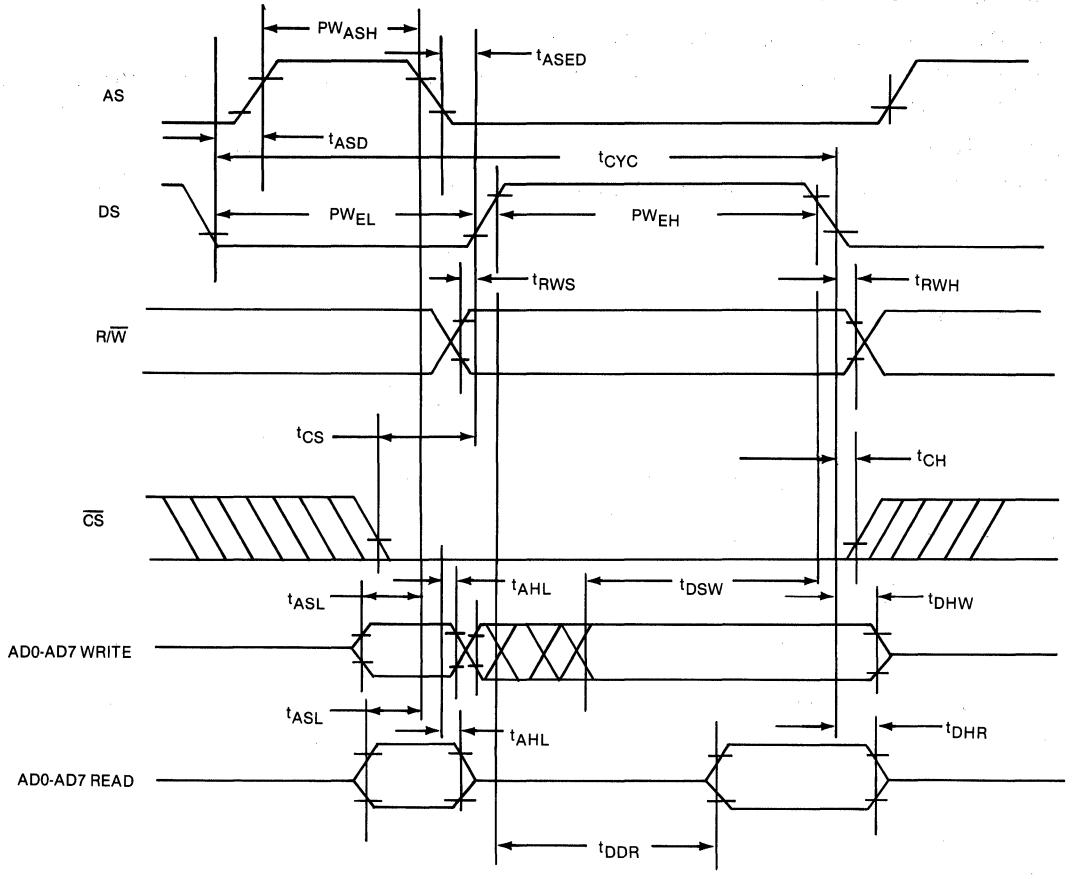
NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pulldown of 20KΩ.
4. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin and the SQW pin when each is in the high impedance state.
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 4.

OUTPUT LOAD Figure 4

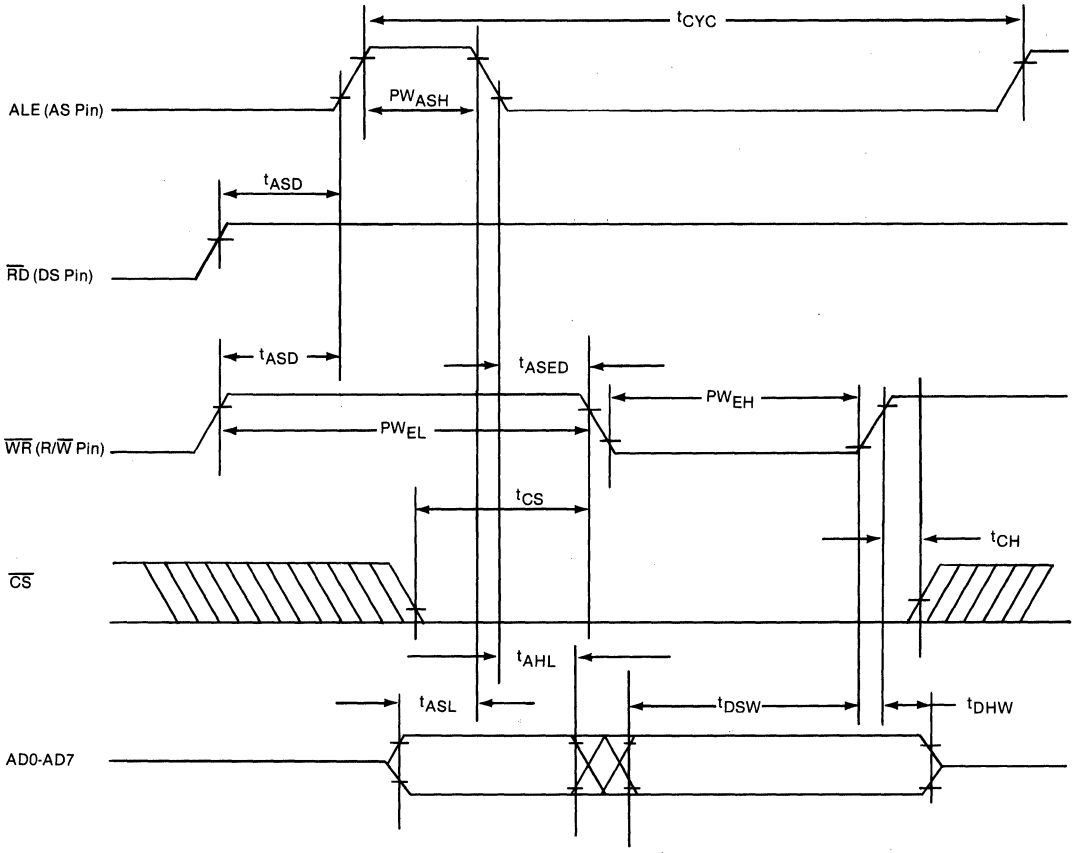


DS1287 BUS TIMING FOR MOTOROLA INTERFACE



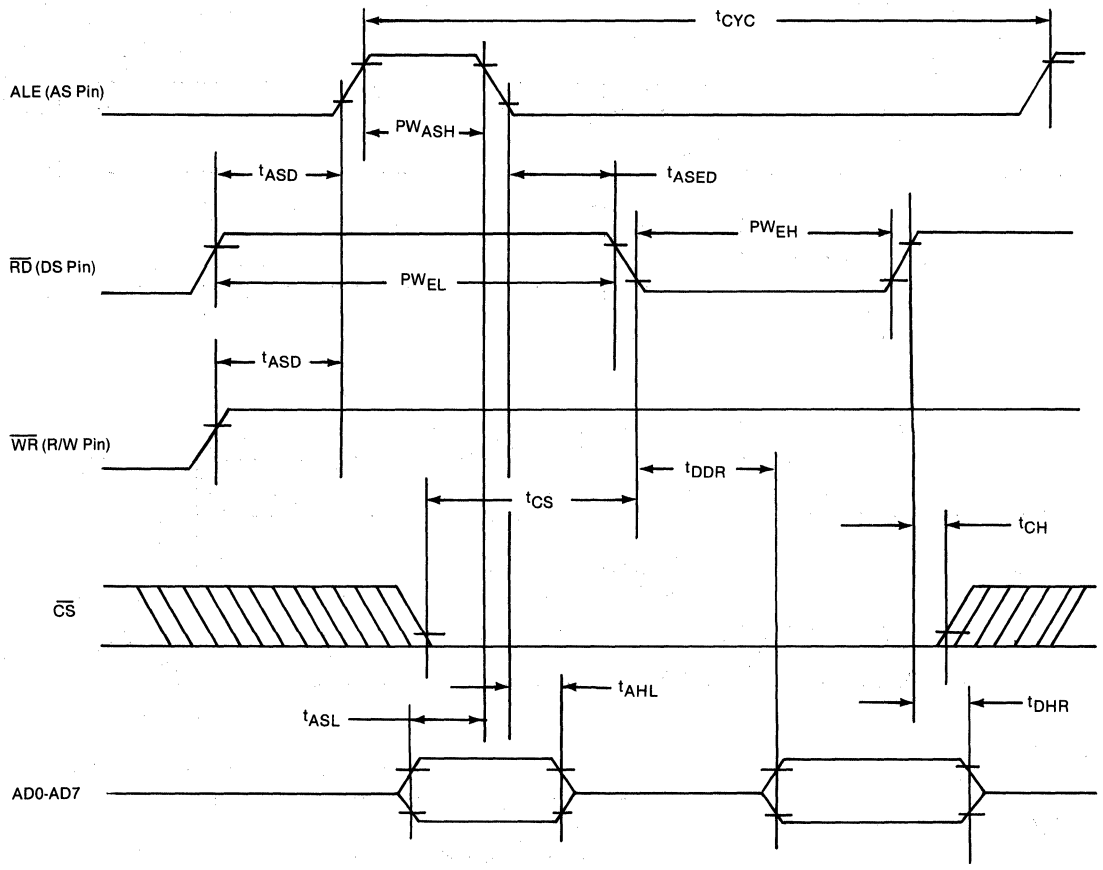
NOTE: Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

DS1287 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



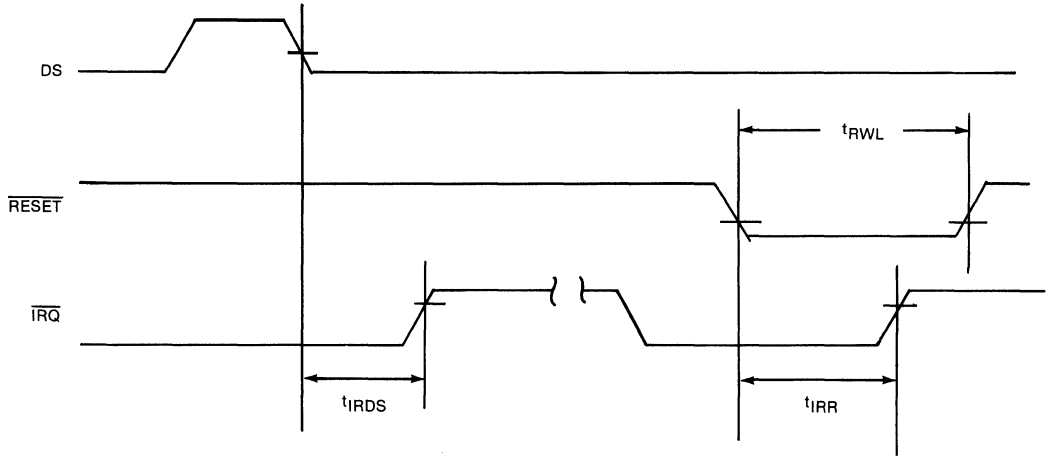
NOTE: Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

DS1287 BUS TIMING FOR INTEL INTERFACE READ CYCLE



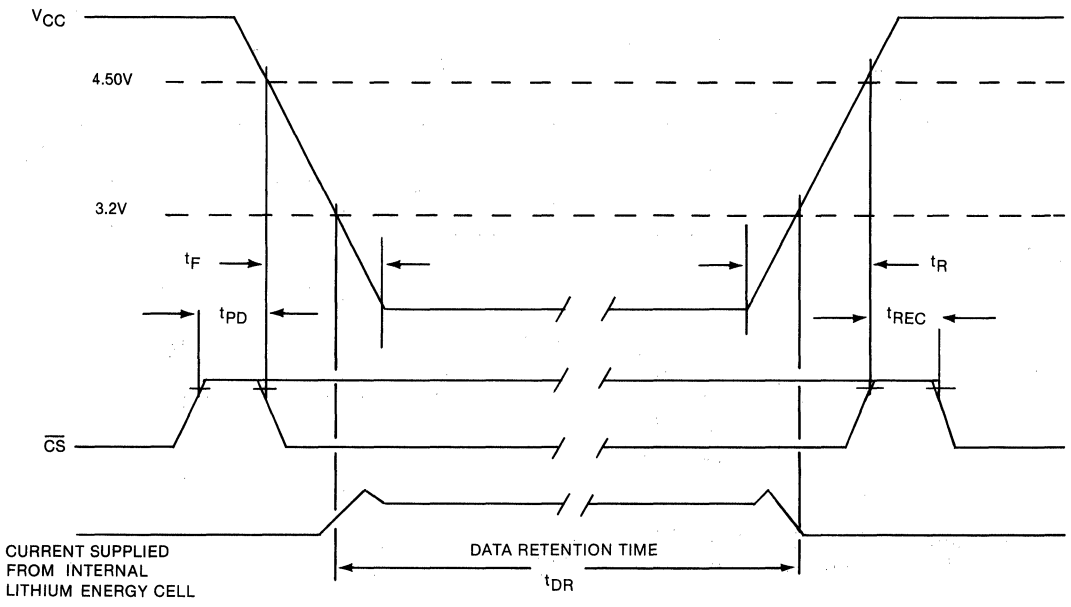
NOTE: Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

DS1287 IRQ RELEASE DELAY TIMING



NOTE: Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

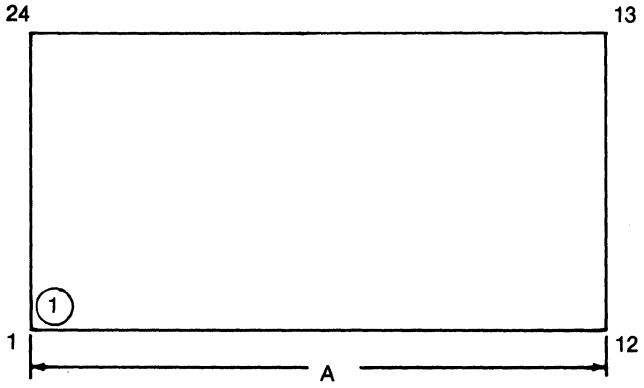
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		*u*s	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		*u*s	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	100		*u*s	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up	20	200	ms	

($t_A = 25°C$)

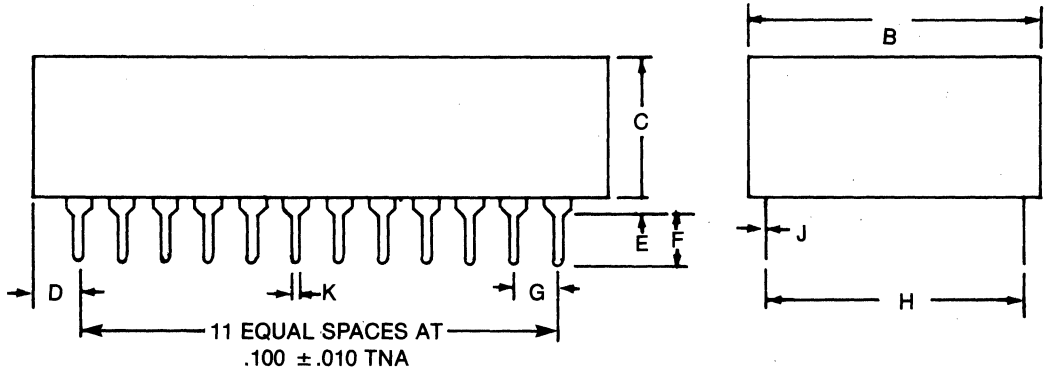
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention	10		years	

NOTE:
The real time clock will keep time to an accuracy of ± 1 minute per month during data retention time for the period of t_{DR}.

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.



DIM.	INCHES	
	MIN.	MAX.
A	1.320	1.335
B	.685	.700
C	.345	.360
D	.100	.120
E	.015	.030
F	.110	.130
G	.090	.110
H	.590	.620
J	.008	.012
K	.015	.021



NOTE: Pins 2, 3, 16, 20, 21 and 22 are missing by design.

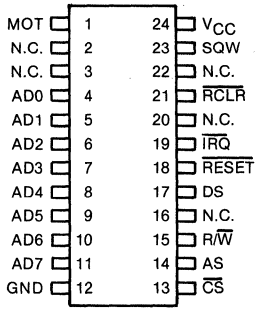
Dallas Semiconductor
Real Time Clock

DS1287A

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month and year with leap year compensation
- Binary or BCD representation of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 *us* to 500 ms
  - End of clock update cycle

PIN CONNECTIONS

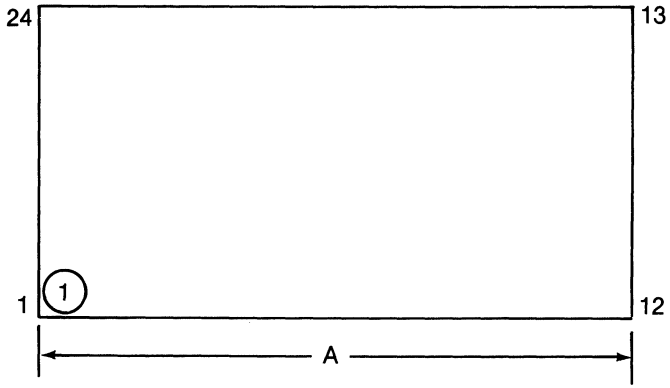


PIN NAMES

AD0 - AD7	- Multiplexed Address/Data Bus
N.C.	- No Connection
MOT	- Bus Type Selection
$\overline{CS}$	- Chip Select
AS	- Address Strobe
R/$\overline{W}$	- Read/Write Input
DS	- Data Strobe
$\overline{RESET}$	- Reset Input
$\overline{IRQ}$	- Interrupt Request Output
SQW	- Square Wave Output
V_{CC}	- +5 Volt Supply
GND	- Ground
$\overline{RCLR}$	- RAM Clear

NOTE—The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not affect the RAM associated with the Real Time Clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (−0.3 to 0.8 volts) during battery back-up mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers.All other operation, description and specification is identical to the DS1287.

DS1287A
RealTime Clock Plus RAM



DIM.	INCHES	
	MIN.	MAX.
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F	.110	.130
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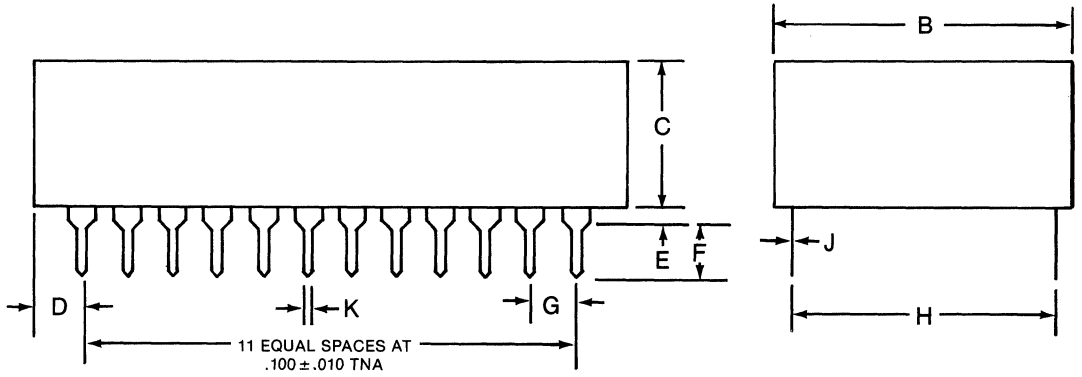
H	.590	.620
J	.008	.012
K	.015	.021



NOTE: Pins 2, 3, 16, 20 and 22 are missing by design.

NOTE: This device cannot be stored or shipped in conductive material which will give a continuity path between the RAM clear pin and ground.

User Insertable Memory

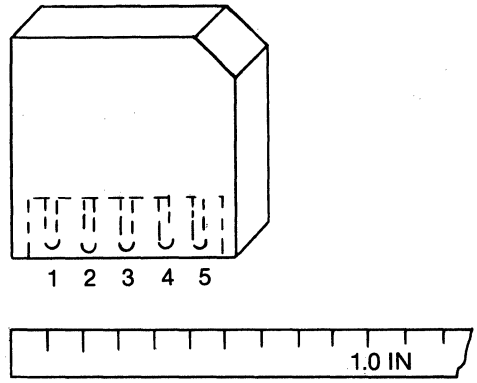
Dallas Semiconductor
Electronic Tag

DS1201

FEATURES

- User insertable
- Nonvolatile—greater than 10 years of data retention
- 1024 bits of read/write memory
- Miniature and transportable
- Durable and rugged
- Impervious to handling
- 4 million bits/second data rate
- Single byte or multiple byte data transfer capability
- No restrictions on the number of write cycles
- Low power CMOS circuitry
- Applications include software authorization, computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work record

PIN CONNECTIONS



PIN NAMES

Pin 1 — V_{CC}	+5 VOLTS
Pin 2 — $\overline{RST}$	$\overline{RESET}$
Pin 3 — DQ	DATA INPUT/OUTPUT
Pin 4 — CLK	CLOCK
Pin 5 — GND	GROUND

DESCRIPTION

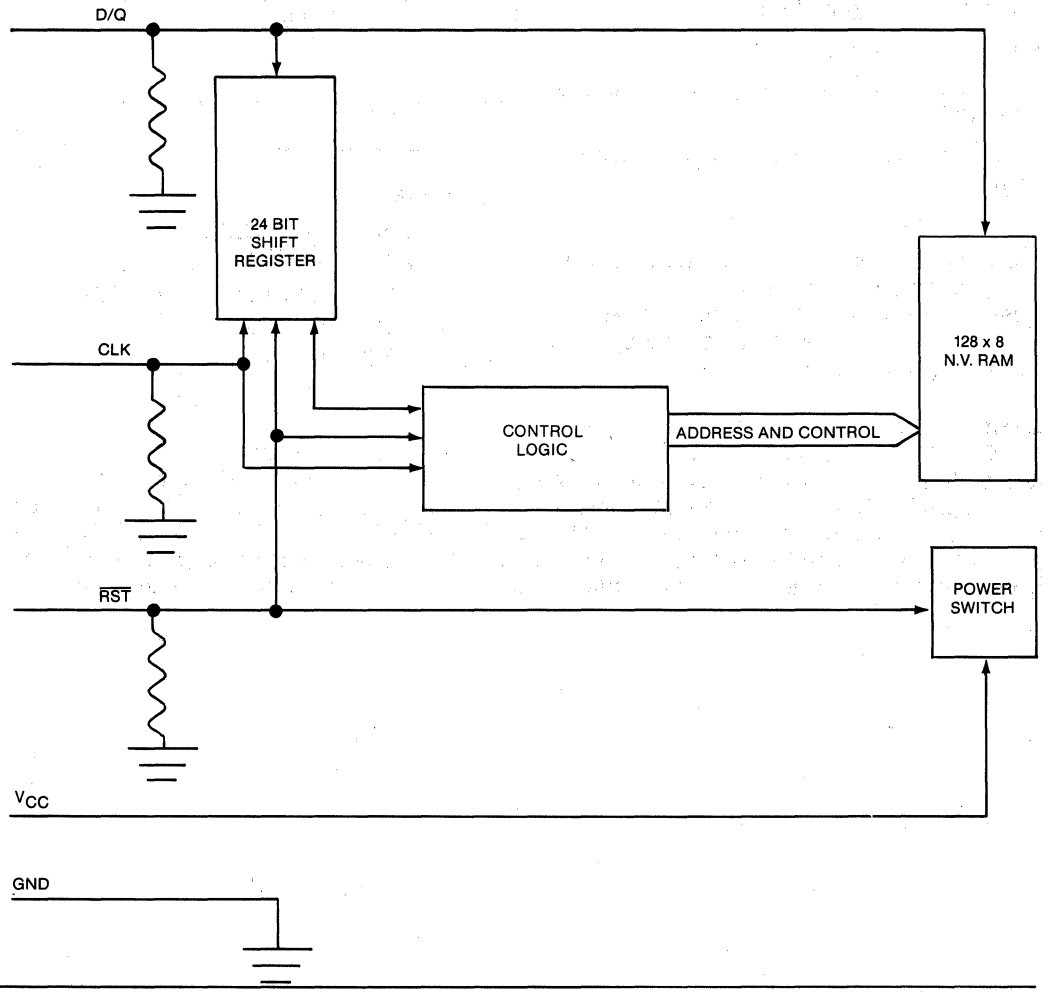
The DS1201 Electronic Tag is a miniature nonvolatile, read/write memory system which can randomly access individual 8-bit strings (bytes) or sequentialy access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{RESET}$, and DATA INPUT/OUTPUT. Low pin count and a guided entry for a mating receptacle overcomes mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user.

OPERATION

The block diagram (Figure 1) of the electronic tag illustrates the main elements of the device; namely, shift register, control logic, nonvolatile RAM, and power switch. To initiate a memory cycle $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the shift register providing both address and command information. Each bit is serial input on the rising edge of the CLOCK input. Seven address bits specify one of the 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 CLOCKs which load the shift register, additional CLOCKs will output data for a read, or input data for a write. The number of CLOCK pulses equals 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

The tag can be used as a four-pin or five-pin device, depending on the application. For hard-wired aplications, active power is supplied by the V_{CC} pin. Alternatively, for user insertable applications, power can be supplied by the $\overline{\text{RESET}}$ pin.

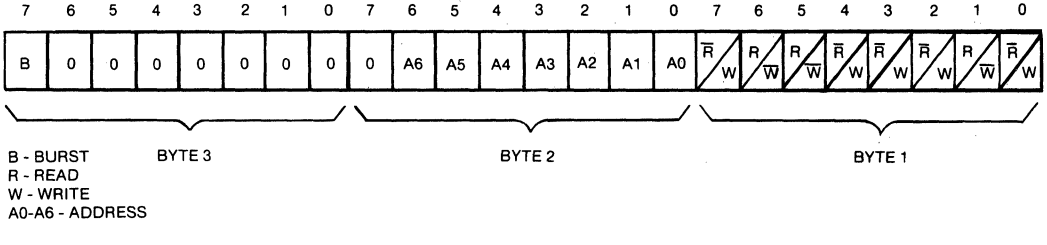
ELECTRONIC TAG BLOCK DIAGRAM Figure 1



ADDRESS/COMMAND

Each memory transfer consists of a three-byte address/command input called the address/command. The address/command is shown in Figure 2. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address/command fails to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the tag are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address inputs A0 in bit 0 through A6 in bit 6. Bit 7 of the second byte of the address/command word must be set to logical 0. This bit is reserved for future higher density versions of the tag. If bit 7 does not equal logical 0, the cycle is aborted and all future inputs to the tag are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The third byte of the address/command is also set aside for future expansion. Bits 0 through 6 must be set to logical 0 or the cycle will be aborted and all future inputs are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. Bit 7 of byte three of the address/command is used along with address bits A0 through A6 to define burst mode. When A0 through A6 equals logical 0 and bit 7 of byte three of the address/command equals logical 1, the tag will enter the burst mode after the address/command sequence is complete.

FIGURE 2



BURST MODE

Burst mode is specified for the electronic tag when all address bits (A0-A6) of the address/command are set to logical 0 and bit 7 of byte three to logical 1. The burst mode causes 128 consecutive bytes to be read or written. Burst mode terminates when the $\overline{\text{RESET}}$ input is driven low.

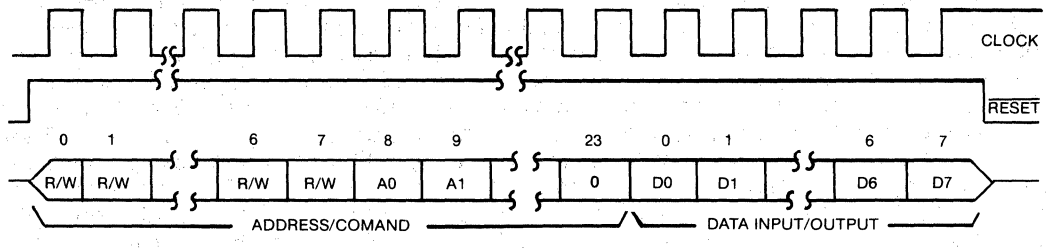
RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{\text{RESET}}$ input high. The $\overline{\text{RESET}}$ input serves three functions. First, $\overline{\text{RESET}}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{\text{RESET}}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{\text{RESET}}$ of 2 mA @ 3.8 volts is required. However, if the V_{CC} pin is connected to a 5 volt source within nominal limits, then $\overline{\text{RESET}}$ pin is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 *u*A. Finally, the $\overline{\text{RESET}}$ signal provides a method of terminating either single byte or multiple byte data transfers. A CLOCK cycle is a sequence of falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of CLOCK cycle. Address/command bits and data bits are input on the rising edge of the CLOCK and data bits are output on the falling edge of the CLOCK. All data transfer terminates if the $\overline{\text{RESET}}$ input is low and D/Q pin goes to a high impedance state. When data transfer to the tag is terminated using reset, the transition of $\overline{\text{RESET}}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 3.

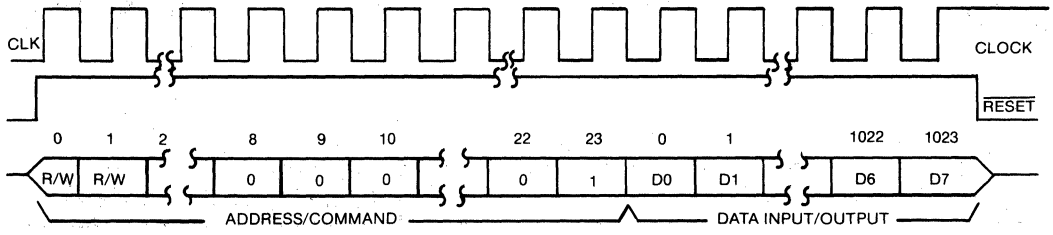
DATA TRANSFER

FIGURE 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



NOTES
1.) DATA INPUT SAMPLED ON RISING EDGE OF CLOCK
2.) DATA OUTPUT CHANGES ON FALLING EDGE OF CLOCK

DATA INPUT

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next 8 CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit5 = 0;bit 6 = 0; bit 7 = 1).

DATA OUTPUT

Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for the data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

TAG CONNECTIONS

The tag is designed to be plugged into a standard 5-pin, 0.1-inch-center SIP receptacle. A key is provided to prevent the tag from being plugged in backwards and to aid in alignment of the receptacle. For portable applications, contact to the tag pins can be determined to insure connection integrity before data transfer begins. CLOCK, $\overline{\text{RESET}}$, and DATA INPUT/OUTPUT all have internal 20K Ohm pull down resistors to ground which can be sensed by a reading device.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1,2,10
Logic 0	V_{IL}	-0.3		0.8	V	1
$\overline{RESET}$ Logic 1	V_{IHE}	3.8			V	1,7,11
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	μA	5
Output Leakage	I_{LO}			+500	μA	5
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
$\overline{RST}$ Input RESISTANCE	Z_{RST}	10		40	KΩ	1
D/Q Input RESISTANCE	Z_{DQ}	10		40	KΩ	1
CLK Input RESISTANCE	Z_{CLK}	10		40	KΩ	1
Active Current	I_{CC1}			6	mA	8
Standby Current	I_{CC2}			2.5	mA	8
$\overline{RST}$ Current	I_{RST}				mA	7,8,13

CAPACITANCE (t_A = 25°C)

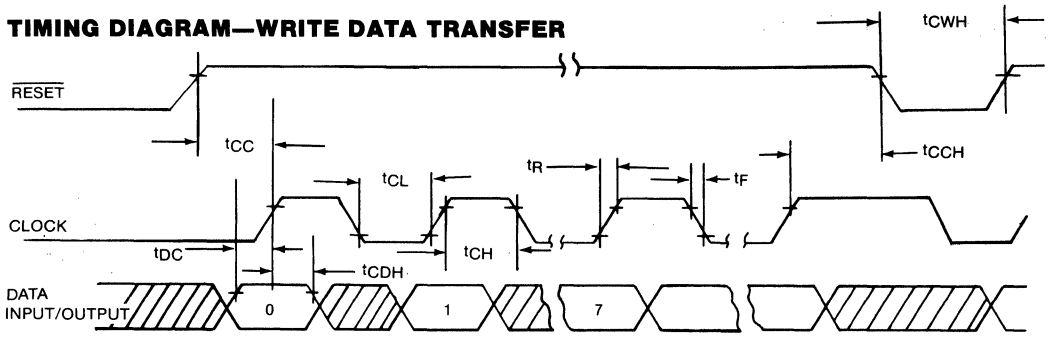
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = +5V ± 10%)

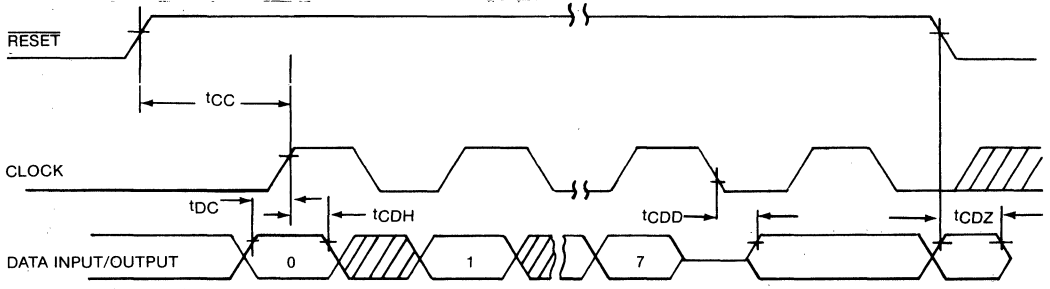
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	35			ns	3,9
Data To CLK Hold	t_{CDH}	40			ns	3,9
Data To CLK Delay	t_{CDD}			125	ns	3,4,6,9
CLK Low Time	t_{CL}	125			ns	3,9
CLK High Time	t_{CH}	125			ns	3,9
CLK Frequency	f_{CLK}	D.C.		4.0	MHZ	3,9
CLK Rise & Fall	t_R,t_F			500	ns	9
$\overline{RST}$ To CLK Set Up	t_{CC}	1			μs	3, 9
CLK To $\overline{RST}$ Hold	t_{CCH}	40			ns	3,9
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	3,9,14
$\overline{RST}$ To I/O High Z	t_{CDZ}			50	ns	3,9

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	12

TIMING DIAGRAM—WRITE DATA TRANSFER



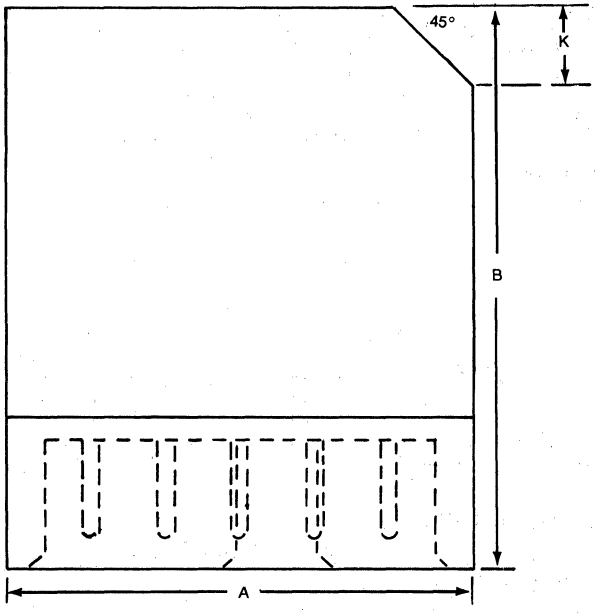
TIMING DIAGRAM—READ DATA TRANSFER



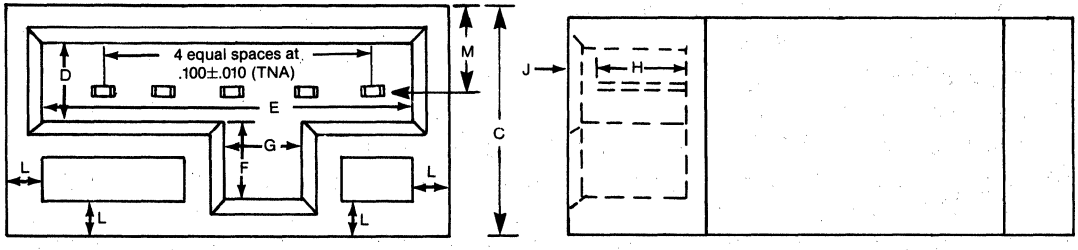
NOTES

1. All voltages and resistances are referenced to GND.
2. Input levels apply to CLK, D/Q, and $\overline{RST}$ while V_{CC} is within nominal limits. When V_{CC} is not connected to the tag, then the $\overline{RST}$ input reverts to V_{IHE}.
3. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8V$ and 10 ns maximum rise and fall time.
4. Measured at $V_{OH} = 2.4$ volts and $V_{OL} = 0.4$ volts.
5. For CLK, D/Q, $\overline{RST}$, and V_{CC} at 5 volts.
6. Load capacitance = 50 pF.
7. Applies to $\overline{RST}$ when $V_{CC} < 3.8$ V.
8. Measured with outputs open.
9. Measured at V_{IH} of $\overline{RST} \geq 3.8V$ when $\overline{RST}$ supplies power.
10. Logic 1 maximum is $V_{CC} + 0.3$ volts if the V_{CC} pin supplies power and $\overline{RST} + 0.3$ volts if the $\overline{RST}$ pin supplies power.
11. $\overline{RST}$ logic 1 maximum is $V_{CC} + 0.3$ volts if the V_{CC} pin supplies power and 5.5 volts maximum if $\overline{RST}$ supplies power.
12. Each DS1201 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13. Average A.C. $\overline{RST}$ current can be determined using the following formula:
    $I_{TOTAL} = 2 + I_{LOAD\ D.C.} + (4 \times 10^{-3})(C_L + 140) f$
    I_{TOTAL} and I_{LOAD} are in mA; C_L is in pF; f is in MHZ.
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHZ gives an I_{TOTAL} current of 5 mA.
14. When $\overline{RST}$ is supplying power t_{CWH} must be increased to 100 ms.

Electronic Tag
DS1201



DIM.	INCHES	
	MIN.	MAX.
A	.610	.630
B	.740	.760
C	.310	.330
D	.100	.110
E	.515	.525
F	.100	.110
G	.100	.110
H	.110	.130
J	.030	.050
K	.045	.055
L	.045	.055
M	.100	.110



Dallas Semiconductor
Nonvolatile Read/Write Cartridge — *DS1217A*

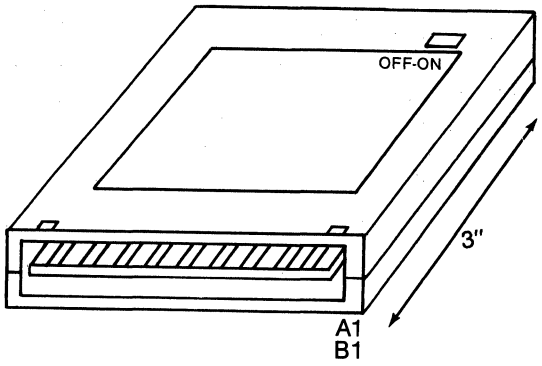
FEATURES

- User insertable
- Capacity up to 32K x 8
- Standard Bytewide pinout facilitates connection to JEDEC 28 pin DIP via ribbon cable
- Data retention greater than 10 years
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0-70°C

SIGNAL CONNECTIONS

Name	Position		Name
Ground	A1	B1	No Connect
+5 Volts	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data (DQ0)
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground

PACKAGE



DESCRIPTION

The DS1217A is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge is available in density ranges from 2K × 8 to 32K × 8 in 8K-byte increments. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a 28-conductor ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28-pin Bytewide memory sites.

The DS1217A cartridge has a lifetime energy source to retain data and circuitry needed to automatically protect memory content. Reading and writing the memory locations is the same as using conventional static RAM. If the user wants to convert from read/write memory to read-only memory, a manual switch is provided to unconditionally protect memory content.

READ MODE

The DS1217A is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217A is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write protected.

DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217A constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM. To retain data during power up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217A checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge provides battery redundancy. The DS1217A provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems which contain 28-pin Bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin ribbon cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push out may occur as the distance between the cartridge and driving circuitry is increased.

CARTRIDGE NUMBERING Table 1

PART NO.	DENSITY	UNUSED ADDRESS INPUTS
DS1217A/16K-25	2K x 8	*ADDRESS 11, 12, 13, 14
DS1217A/64K-25	8K x 8	*ADDRESS 13, 14
DS1217A/128K-25	16K x 8	*ADDRESS 14
DS1217A/192K-25	24K x 8	
DS1217A/256K-25	32K x 8	

*Unused address inputs must be held low (V_{IL}).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Connection Relative to Ground −0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		+0.8	V

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	−60		+60	*u*A
I/O Leakage Current	I_{LO}	−10		+10	*u*A
Output Current @2.4V	I_{OH}	−1.0	−2.0		mA
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA
Standby Current $\overline{CE}=2.2V$	I_{CC}		5.0	10	mA
Operating Current	I_{CC}		35	75	mA

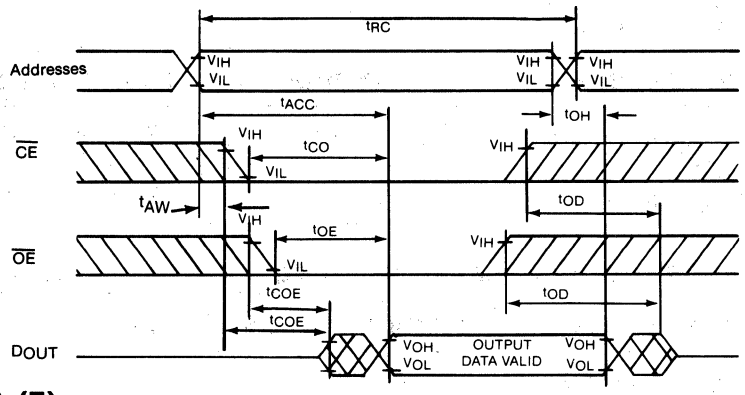
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	75	pF	
Input/Output Capacitance	$C_{I/O}$	75	pF	

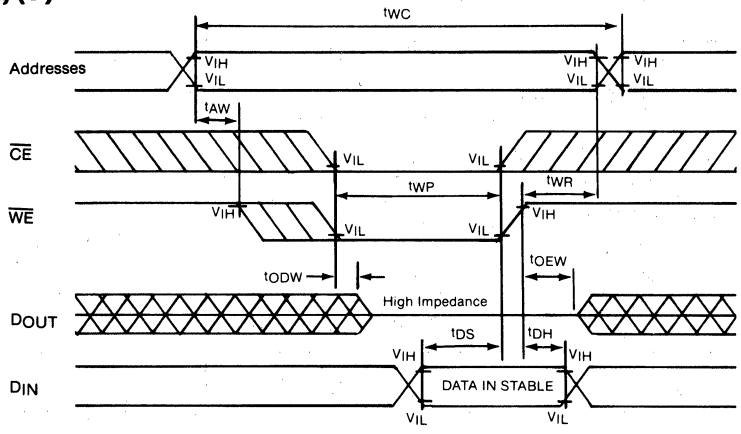
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
$\overline{OE}$ to Output Valid	t_{OE}			125	ns	
$\overline{CE}$ to Output Valid	t_{CO}			250	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10			ns	
Output High Z From Deselection	t_{OD}			125	ns	
Output Hold From Address Change	t_{OH}	10			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Set Up Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z From $\overline{WE}$	t_{ODW}			100	ns	
Output Active From $\overline{WE}$	t_{OEW}	10			ns	
Data Set Up Time	t_{DS}	100			ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	0			ns	4,5

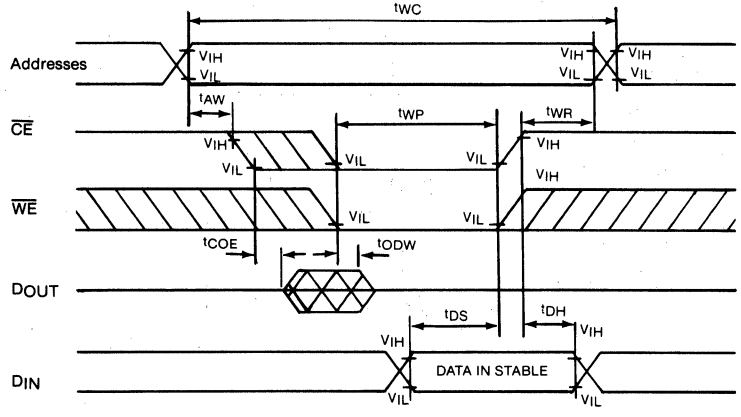
READ CYCLE (1)



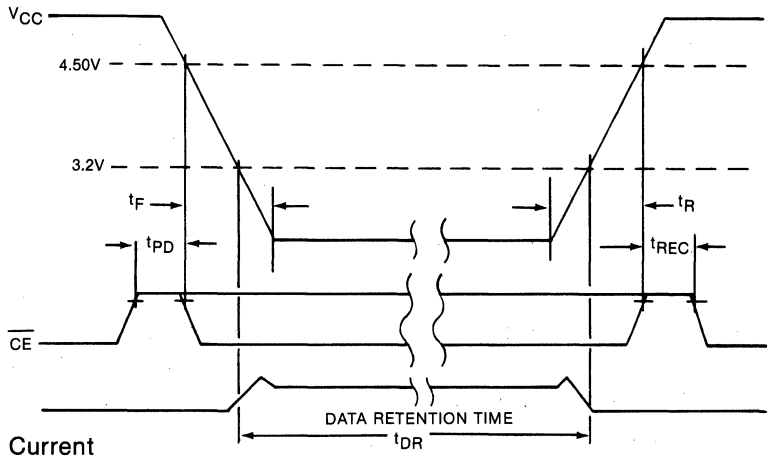
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		μs	10
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		μs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		μs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up	2	125	ms	10

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

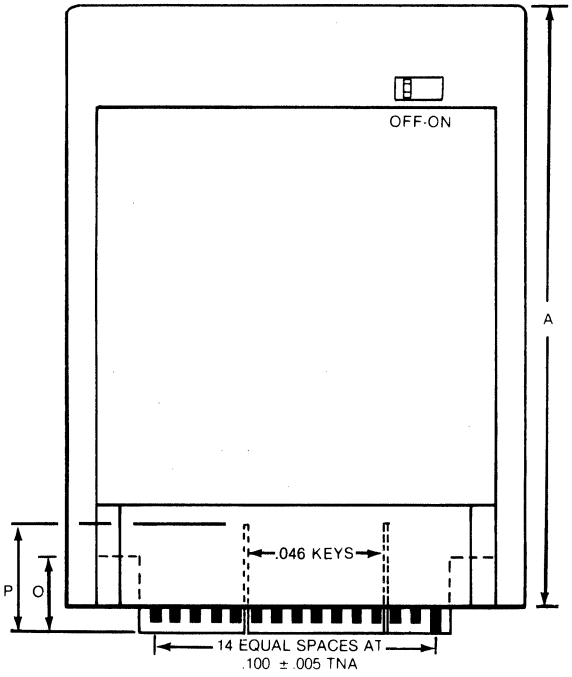
NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20ns$.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1217A is market with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

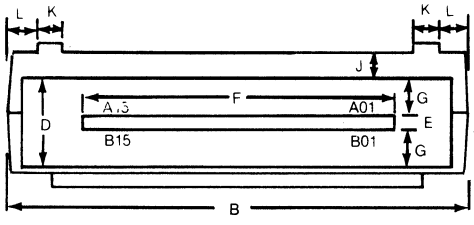
D.C. Test Conditions
Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

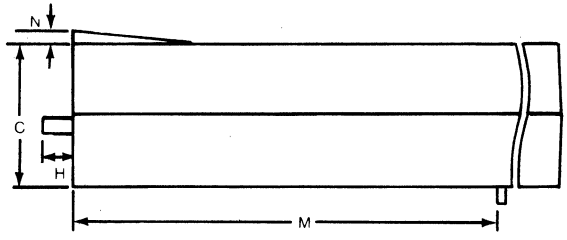
A.C. Test Conditions
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

Nonvolatile Read/Write Cartridge
DS1217A



DIM.	INCHES	
	MIN.	MAX.
A	3.020	3.040
B	2.280	2.300
C	.590	.620
D	.440	.460
E	.060	.065
F	1.590	1.607
G	.190	.220
H	.115	.135
J	.115	.135
K	.115	.135
L	.140	.160
M	1.760	1.790
N	.040	.060
O	.039	.405
P	.405	.425





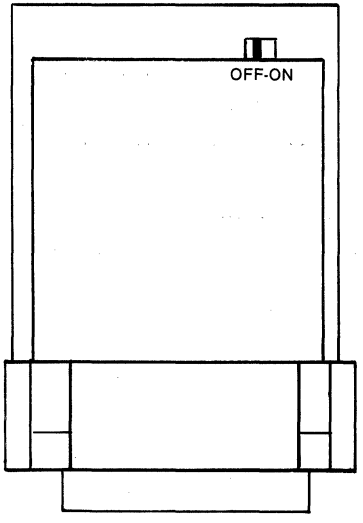
Dallas Semiconductor
Nonvolatile Read/Write Cartridge — *DS1217I*

FEATURES

- User insertable
- Data retention greater than 5 years
- Capacity up to 512K × 8
- Employs high-reliability, 32-position DIN connector
- Software controlled banks maintain 32K × 8 JEDEC 28-pin compatibility
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0-70°C

SIGNAL CONNECTIONS

No Connect	A_0	B_0	No Connect
Ground	A_1	B_1	No Connect
+5 Volts	A_2	B_2	Address 14
$\overline{\text{Write Enable}}$	A_3	B_3	Address 12
Address 13	A_4	B_4	Address 7
Address 8	A_5	B_5	Address 6
Address 9	A_6	B_6	Address 5
Address 11	A_7	B_7	Address 4
$\overline{\text{Output Enable}}$	A_8	B_8	Address 3
Address 10	A_9	B_9	Address 2
$\overline{\text{Cartridge Enable}}$	A_{10}	B_{10}	Address 1
Data I/O 7	A_{11}	B_{11}	Address 0
Data I/O 6	A_{12}	B_{12}	Data I/O 0
Data I/O 5	A_{13}	B_{13}	Data I/O 1
Data I/O 4	A_{14}	B_{14}	Data I/O 2
Data I/O 3	A_{15}	B_{15}	Ground

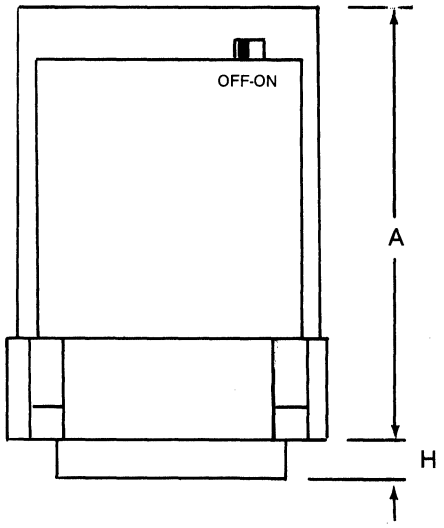


DESCRIPTION

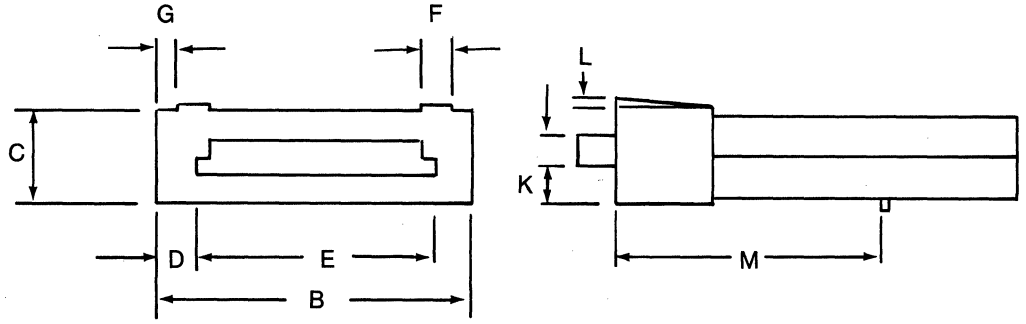
The DS1217I is a portable nonvolatile SRAM designed for industrial applications requiring a connection scheme which is protected from contamination in shop floor and other similar harsh environments. The high-reliability DIN connector design allows for multiple insertions and withdrawals even with power applied. A male 30-position vertical P.C. board mountable connector with first-make/last-break contacts is provided with each DS1217I memory cartridge. Right angle connectors are available as an option. The DS1217I may be purchased with densities ranging from 64K × 8 to 512K × 8.

See DS1217M for all electrical specifications.

Nonvolatile Read/Write Cartridge
DS1217I



DIM.	INCHES	
	MIN.	MAX.
A	3.290	3.310
B	2.400	2.415
C	.710	.730
D	.315	.345
E	1.735	1.755
F	.220	.240
G	.125	.145
H	.200	.220
J	.230	.240
K	.220	.240
L	.030	.040
M	2.035	2.065



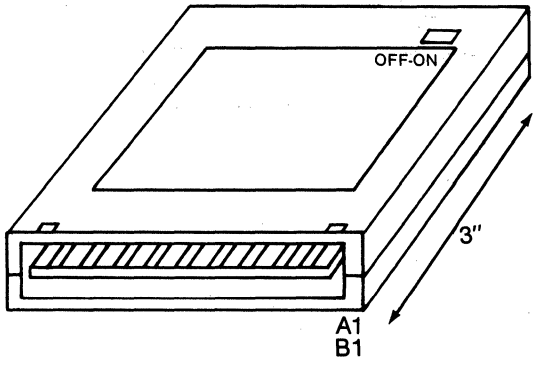
Dallas Semiconductor

Nonvolatile Read/Write Cartridge — *DS1217M*

FEATURES

- User insertable
- Data retention greater than 5 years
- Capacity up to 512K × 8
- Standard Bytewide pinout facilitates connection to JEDEC 28 pin DIP via ribbon cable
- Software controlled banks maintain 32K × 8 JEDEC 28 pin compatability
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0-70°C

PACKAGE



SIGNAL CONNECTIONS

NAME	POSITION		NAME
Ground	A1	B1	No Connect
+5 Volts	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground

DESCRIPTION

The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 64K × 8 to 512K × 8. The cartridge is accessed in continuous 32K byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required for connection to a host system. A standard 30 pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28 pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28 Pin bytewide memory sites.

READ MODE

The DS1217M is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217M is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write protected.

DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217M constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217M checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge provides battery redundancy. The DS1217M provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

BANK SWITCHING

Bank switching is accomplished via address lines A8, A9, A10 and A11. Initially, on power up all banks are deselected so that multiple cartridges can reside on a common bus. Bank switching requires that a predefined pattern of 64 bits is matched by sequencing 4 address inputs (A8 through A11) 16 times while ignoring all other address inputs. Prior to entering the 64 bit pattern which will set the bank switch, a read cycle of 1111 (address inputs A8 through A11) must be executed to guarantee that pattern entry starts with the first set of 4 bits. Each set of address inputs are entered into the DS1217M by executing read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 2. The last five cycles must match the exact bit pattern for addresses A9, A10 and A11. However, address line 8 defines which of the 16 banks that is to be enabled, or all banks deselected, as per Table 3.

Switching from one bank to another occurs as the last of the 16 read cycles is completed. A single bank is selected at any one time. A selected bank will remain active until a new bank is selected, all banks are deselected, or until power is lost. (See DS1222 BankSwitch data sheet for more detail.)

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems which contain 28 pin Bytewide sockets can be retrofitted using a 28 pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28 pin site after the memory is removed. Connection to the cartridge is accomplished via a 28 pin cable connected to a 30 contact card edge connector, AMP Part Number 499188-4. The 28 pin ribbon cable must be right-justified, such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push out may occur as the distance between the cartridge and the driving circuitry is increased.

TABLE 1 — CARTRIDGE NUMBERING

PART NO.	DENSITY	NO. OF BANKS
DS1217M 1/2-25	64K × 8	2
DS1217M 1-25	128K × 8	4
DS1217M 2-25	256K × 8	8
DS1217M 3-25	384K × 8	12
DS1217M 4-25	512K × 8	16

TABLE 2 — ADDRESS INPUT PATTERN

ADDRESS INPUTS	BIT SEQUENCE															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A_8	1	0	1	0	0	0	1	1	0	1	0	X	X	X	X	X
A_9	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_{10}	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_{11}	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X = See Table 3

TABLE 3 — BANK SELECT TABLE

BANK SELECTED	A_8 BIT SEQUENCE				
	11	12	13	14	15
BANKS OFF	0	X	X	X	X
BANK 0	1	0	0	0	0
BANK 1	1	0	0	0	1
BANK 2	1	0	0	1	0
BANK 3	1	0	0	1	1
BANK 4	1	0	1	0	0
BANK 5	1	0	1	0	1
BANK 6	1	0	1	1	0
BANK 7	1	0	1	1	1
BANK 8	1	1	0	0	0
BANK 9	1	1	0	0	1
BANK 10	1	1	0	1	0
BANK 11	1	1	0	1	1
BANK 12	1	1	1	0	0
BANK 13	1	1	1	0	1
BANK 14	1	1	1	1	0
BANK 15	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS*

Voltage on Connection Relative to Ground $-0.3V$ to $+7.0V$
Operating Temperature 0°C to 70°C
Storage Temperature $-40°C$ to $+70°C$

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		+0.8	V

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	−60		+60	uA
I/O Leakage Current	I_{LO}	−10		+10	uA
Output Current @2.4V	I_{OH}	−1.0	−2.0		mA
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA
Standby Current $\overline{CE}=2.2V$	I_{CC}		15	25	mA
Operating Current	I_{CC}		50	100	mA

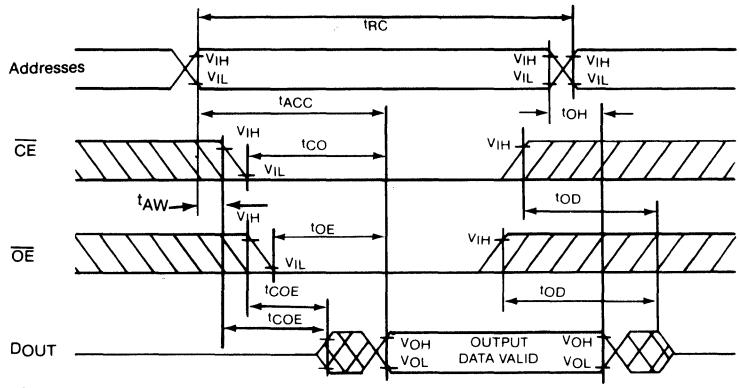
CAPACITANCE ($t_A = 25\,°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	100	pF	
Input/Output Capacitance	C_{OUT}	100	pF	

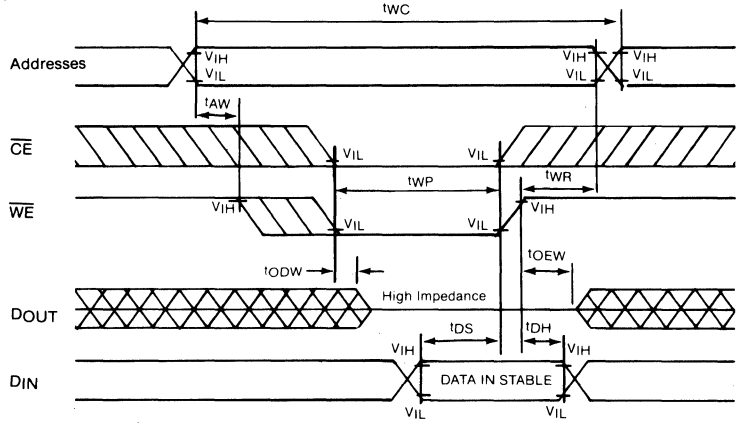
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			210	ns	
$\overline{OE}$ to Output Valid	t_{OE}			125	ns	
$\overline{CE}$ to Output Valid	t_{CO}			210	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	10			ns	
Output High Z From Deselection	t_{OD}			125	ns	
Output Hold From Address Change	t_{OH}	10			ns	
Read Recovery Time	t_{RR}	40			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Set Up Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z From $\overline{WE}$	t_{ODW}			100	ns	
Output Active From $\overline{WE}$	t_{OEW}	10			ns	
Data Set Up Time	t_{DS}	100			ns	4
Data Hold Time From $\overline{WE}$	t_{DH}	0			ns	4,5

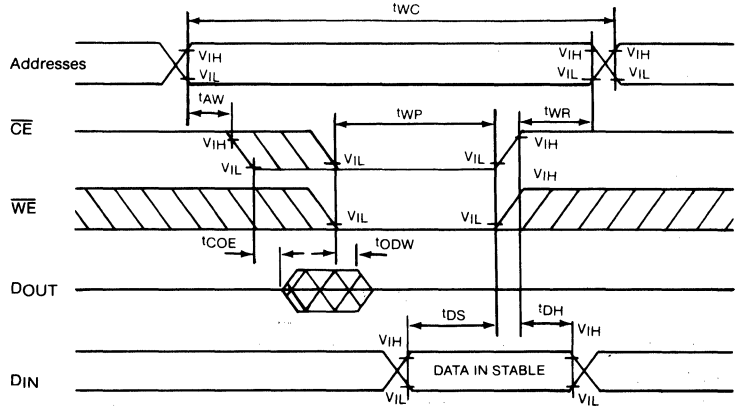
READ CYCLE (1)



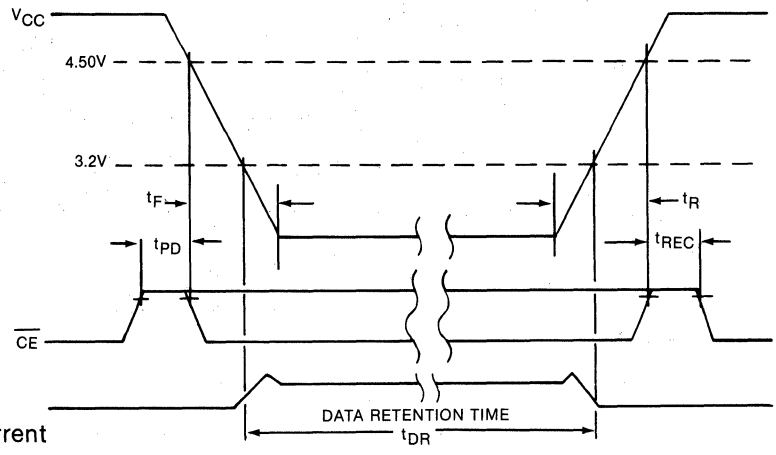
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		μs	10
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		μs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		μs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up	2	125	ms	10

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	5		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

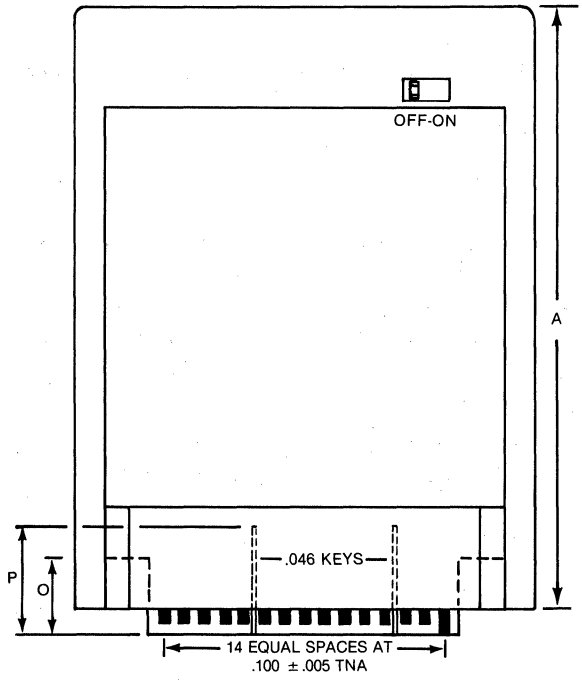
NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1217M is market with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

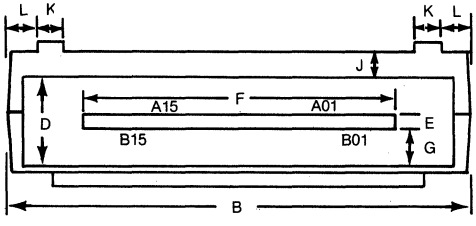
D.C. Test Conditions
Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

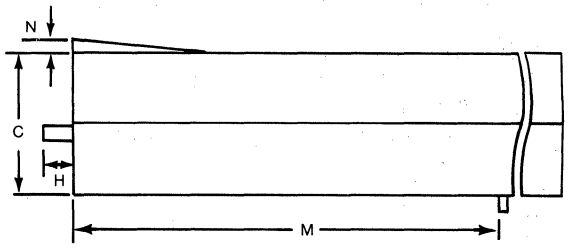
A.C. Test Conditions
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

Nonvolatile Read/Write Cartridge
DS1217M



DIM.	INCHES	
	MIN.	MAX.
A	3.020	3.040
B	2.280	2.300
C	.600	.630
D	.440	.460
E	.060	.065
F	1.590	1.607
G	.220	.250
H	.115	.135
J	.115	.135
K	.115	.135
L	.140	.160
M	1.760	1.790
N	.040	.060
O	.039	.405
P	.405	.425





Dallas Semiconductor
KeyRing

DS1250

FEATURES

- Low cost add-on fixture for Electronic Keys and Tags
- No hardware changes needed to retrofit existing systems
- Layman installation
- Normal system operation unaffected
- Key or Tag communication totally controlled by software
- Typical 50 K bits/s communication rate
- Up to 5 Keys and/or Tags resident at one time

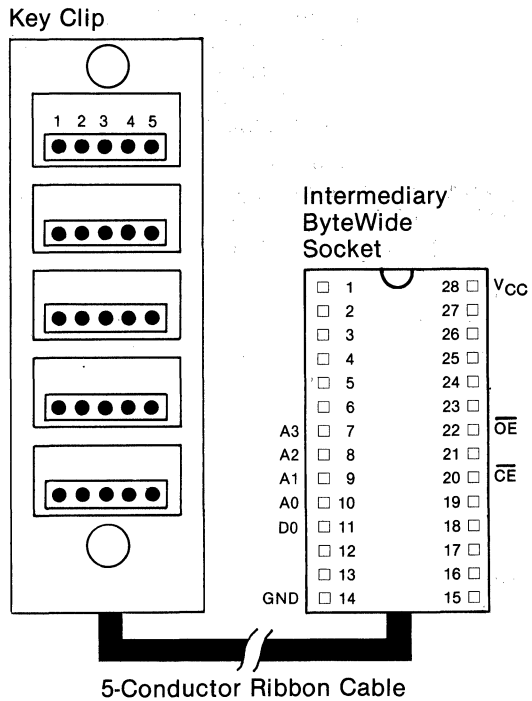
PIN CONNECTIONS AND DEFINITIONS

Intermediary ByteWide Socket
Pins 7-10 - Address Inputs
Pin 11 - D0
Pin 20 - conditioned Chip Enable
Pin 22 - Output Enable
Pin 14 - Ground
Pin 28 - V_{CC}

All pins pass through except 20

Key Clip

Pin 1 - V_{CC} +5 Volts
Pin 2 - $\overline{RST}$ - $\overline{RESET}$
Pin 3 - DQ - Data In/Out
Pin 4 - CLK - CLOCK
Pin 5 - GND - Ground



DESCRIPTION

The DS1250 KeyRing adapts low pin count Electronic Keys (DS1204), TimeKeys (DS1207) or Tags (DS1201) to JEDEC ByteWide memory signals without affecting system operation. A simple, layman procedure is all that is needed to retrofit an existing system. Any 28 pin RAM, ROM, or EPROM can be removed, placed in the intermediary socket, and then reinstalled in the original location leaving the system intact. The emanating 5 conductor ribbon cable can be routed out of the system enclosure if desired and the clip can be attached where convenient with the adhesive provided. Up to 5 Keys and/or Tags can be inserted in the clip at the same time. The intermediary socket contains a CMOS integrated circuit which redirects information flow from the ByteWide memory to the inserted keys/tags. A special software generated address sequence causes the redirection to take place. Typical data transfer rates of 50 K bits/s are possible with an assembly language software driver.

HARDWARE IMPLEMENTATION 28-PIN ROM SOCKET

Bytewide KeyRing application begins with a system board which contains a 28-pin socket with or without a ROM contained in the socket. In most system implementations and all PCs, there is at least one ROM which is used for boot sequences, basic I/O system implementation, EPROM storage, or some form of dedicated software monitor application.

Installation of the Bytewide KeyRing requires the removal of the existing 28-pin ROM and the insertion of the Bytewide KeyRing socket pins into the system board socket. After this is accomplished, the original ROM is reinserted into the socket at the top of the Bytewide KeyRing. Then the five-conductor ribbon cable which connects the clip to the Bytewide socket is routed to the outside of the computer cabinet. Finally the clip can be attached to a convenient place on the computer cabinet using the supplied adhesive.

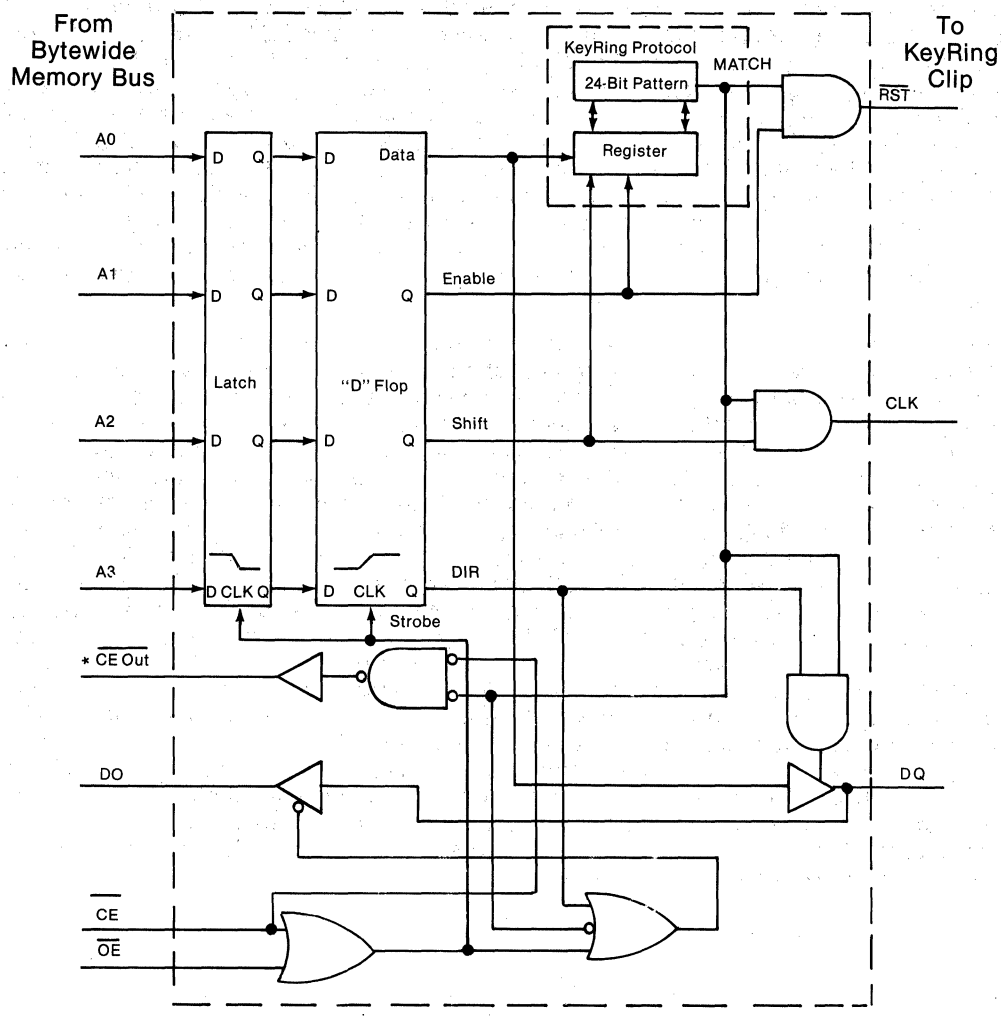
Under normal conditions, the system ROM will function as before, with address and data lines being transparently ported through the Bytewide KeyRing socket and presented to the system ROM as in the original configuration. As a result, existing non-Key-protected software will run on the system unaffected. However, if certain address lines are probed with specific patterns under software control, the KeyRing is activated and the system ROM becomes electrically disconnected from the system board. Instead, the address and data bus become electrically tied to the KeyRing bus. At this point, communication to the system board ROM socket is passed on transparently to any device(s) which are inserted into the KeyRing clip.

KEYRING OPERATION

The main parts of the KeyRing are shown in the block diagram of Figure 1. Information presented on address inputs of the ROM are latched into the KeyRing on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}$ In and $\overline{OE}$ In. The $\overline{CE}$ input is connected to the memory bus $\overline{CE}$ and the $\overline{OE}$ input is connected to the memory bus $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 24-bit KeyRing protocol and to logic which will generate signals for Keys and Tags. The KeyRing protocol is derived from address inputs A0, A1 and A2. A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially the A1 input must be set high to enable communications. A1 must remain high during the pattern recognition sequence and subsequent communications with Keys after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and access is denied.

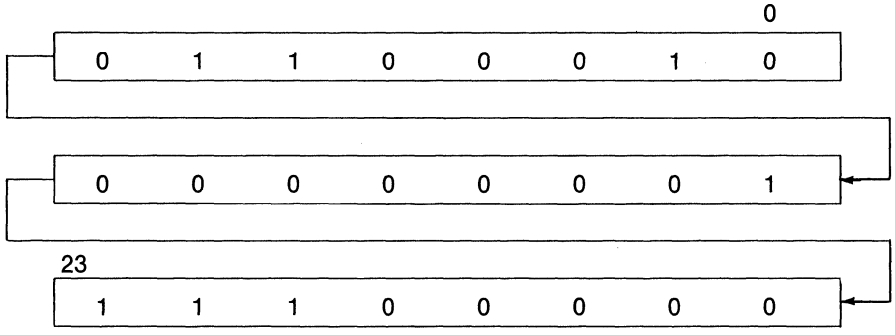
Data transfer through the KeyRing occurs by matching a 24-bit pattern, as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Therefore, data is input for comparison to the KeyRing protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles. The first memory cycle sets A2 low, establishing the shift clock low. The second memory cycle sets A2 high, causing the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the same level for both memory cycles. Address input A3 is used to control the direction of data going to and from Keys. This input is not used during pattern recognition of the KeyRing protocol. After the 24-bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for Keys. The match signal is also used to disable Chip Enable to the topside memory and enable a gate which allows Key DQ to drive D0 line to the memory bus. When $\overline{RST}$ is driven high, devices attached to the KeyRing become active. Subsequent shift signals derived from A2 will now be recognized as the Key clock. The data signal for the Key is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on Key DQ. When A3 is set low, devices attached to the KeyRing can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the Key DQ.

KEYRING BLOCK DIAGRAM Figure 1

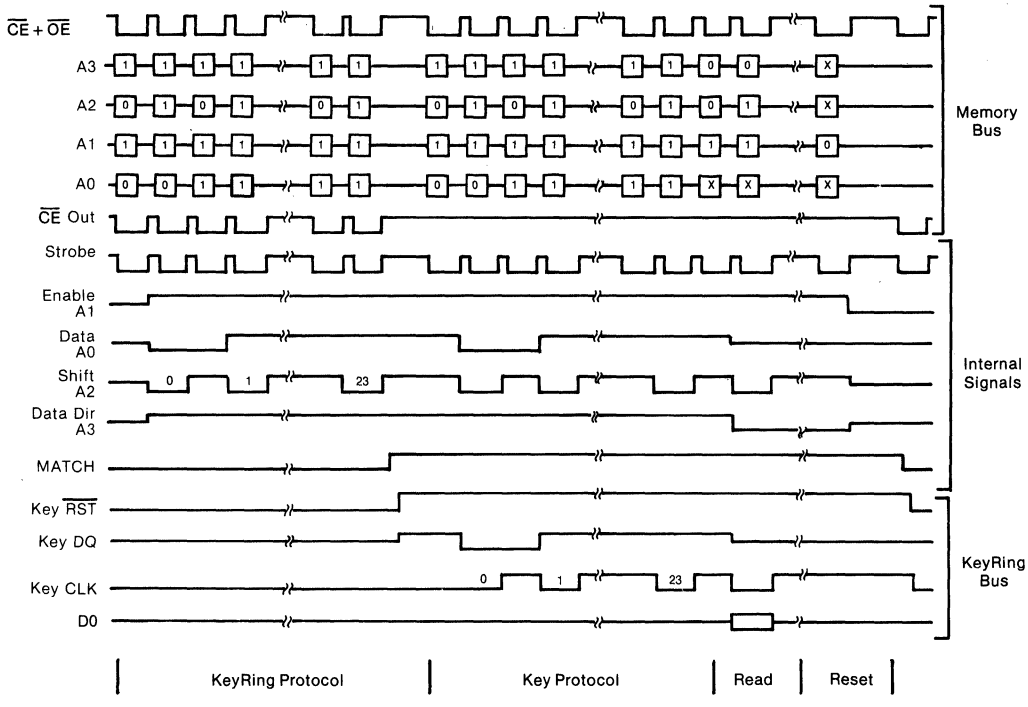


* Socket Receptacle

KEYRING PROTOCOL Figure 2



KEYRING SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Logic 0 Input	V_{IL}	−0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	−1		1	*u*A	
Output Leakage	I_{LO}			1	*u*A	
Output Current @2.4V	I_{OH}	−1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
$\overline{RST}$ Output Current @3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

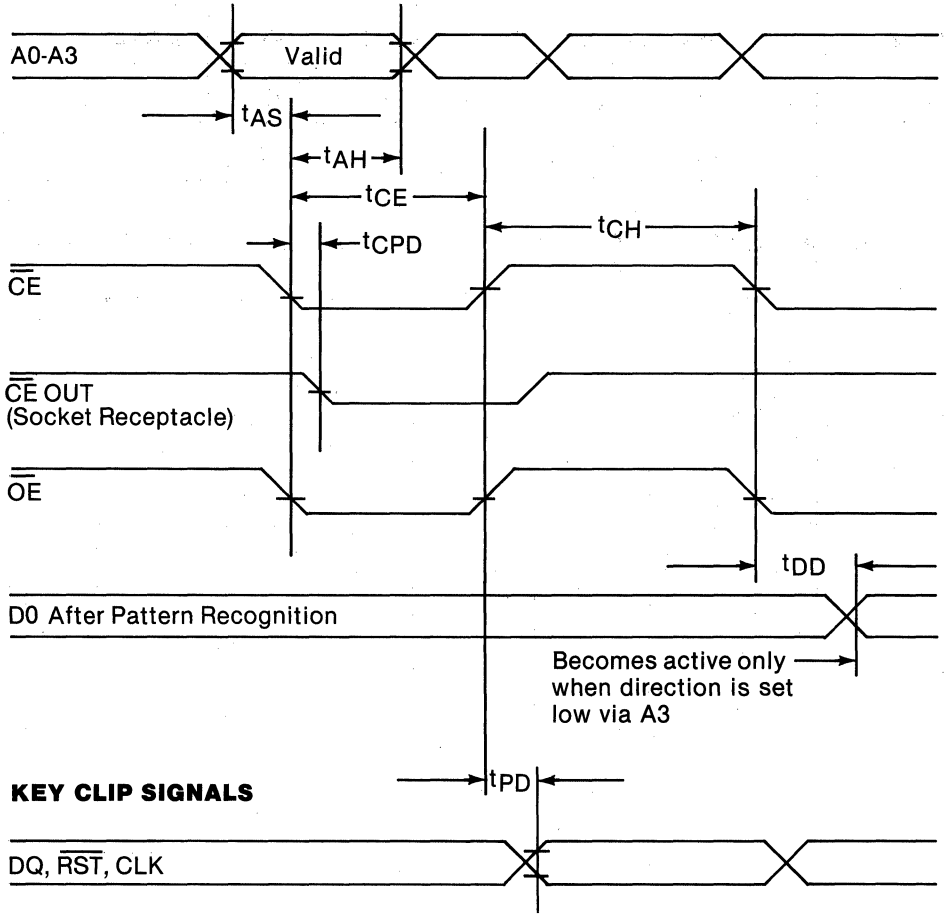
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output	$C_{I/O}$	5	10	pF	

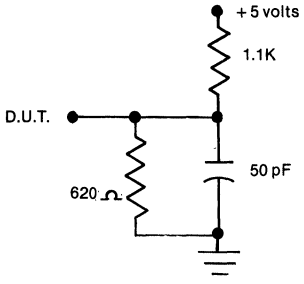
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Set Up	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
$\overline{CE}$ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
$\overline{CE}$ Inactive	t_{CH}	30			ns	
$\overline{CE}$ Propagation Delay	t_{CPD}			10	ns	

BYTEWIDE MEMORY BUS



OUTPUT LOAD Figure 4



NOTES:

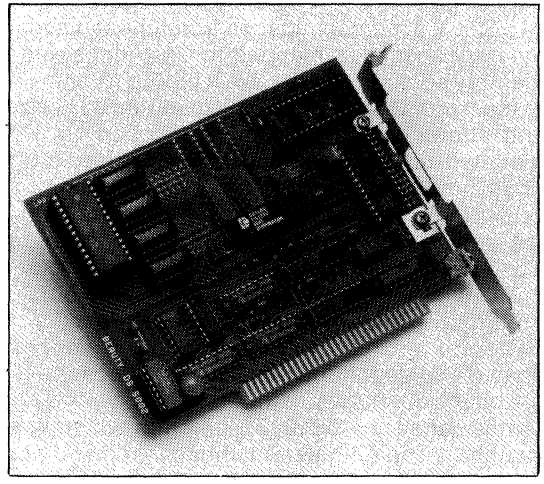
1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Measured with a load as shown in Figure 4.

Dallas Semiconductor
P.C. Port

DS6010

FEATURES

- Half-size expansion card which interfaces the PC, XT and AT compatible computers with Dallas Semiconductor cartridges and cartridge clips
- Software included which supports the installation and controls operation
- Responds to all PC DOS commands
- Self-booting on power-up after installation
- Occupies only two 32K x 8 blocks of the PC memory map
- Provides the equivalent of a four-megabyte solid-state disk drive when used with the cartridge clip
- Contains a real-time clock for time stamping and dating of file transactions
- Software-controlled DIP switch simplifies installation
- High performance data transfer
- Low operating power
- Optional software protection and access control is available by using the DS1204U Electronic Key



DESCRIPTION

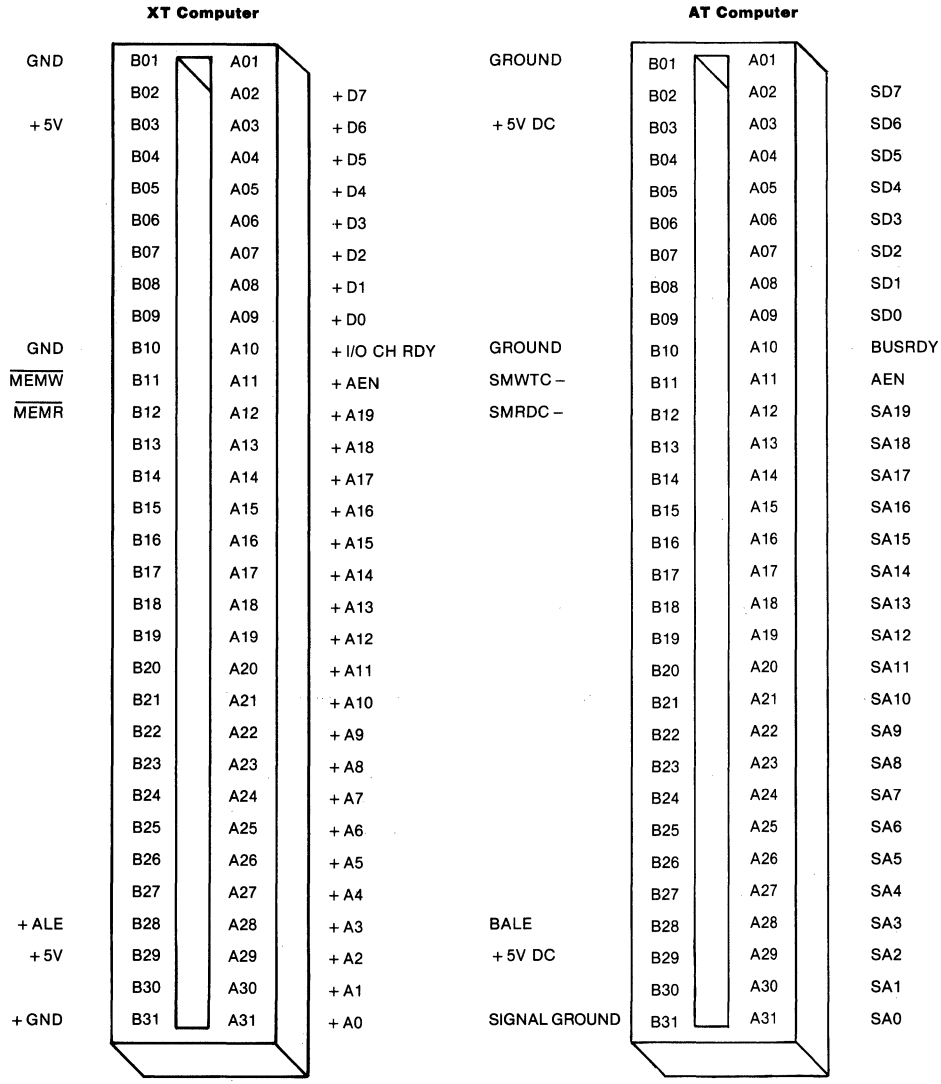
The DS6010 is a half-size expansion slot card which interfaces DS1217 cartridges and DS9020 Cartridge Clips to the IBM PC, XT, AT or compatible computers. Included is a software package which is used to both install and operate the expansion port. After user interaction between the software and the operator, Cartridges and Cartridge Clips will operate under DOS 3.0 commands as a disk drive. Up to eight Cartridges can be modularly added to a computer with each DS6010. This system addition allows compatible computers to be used in environments which are unsuitable for rotating mass memory. The PC port occupies only two 32K x 8 blocks of memory space by using software-controlled bank switching techniques. The SmartWatch, also included on the card, time stamps and dates file transactions.

TECHNICAL DESCRIPTION

The DS6010 PC Port uses several Dallas Semiconductor devices which perform the decoding and control functions of the PC Port. The discussion which follows assumes some understanding of each specific device. If a more detailed explanation of any device is required, the individual data sheet of each part should be studied. These data sheets are supplied in the Dallas Semiconductor Data Book.

The signals from the expansion bus which are used by the DS6010 arrive through the 62-position card edge connector as shown in Figure 1. These signals are used by the DS6010 to develop two 32K x 8 memory spaces from unused sections of the computer memory map. One of the memory spaces is mapped to Cartridges and Cartridge Clips through two 28-pin Bytewide memory sockets which have a pinout as shown in Figure 2. The two sockets are bused directly together. One socket (U10) is mounted horizontal to the IBM expansion slot seating plane and allows for convenient connection via ribbon cable to a Cartridge or Cartridge Clip mounted within the computer cabinet (see Figure 3). The second socket (U11) is mounted vertically and is positioned near the mounting bracket of the DS6010. This socket provided convenient connection via ribbon cable to a Cartridge or Cartridge Clip mounted externally to the computer cabinet. The second memory space developed by the DS6010 contains the DS1216 SmartWatch and 32K x 8 of nonvolatile static RAM. The decoding scheme of the DS6010 is both flexible and soft. The two 32K x 8 blocks of memory space can be located anywhere within the one megabyte memory map of the system. Normally the lower 640K bytes are reserved for DRAM so the decoder would be set for some area in upper memory space. The decoder scheme is soft because the software supplied with DS6010 can set the decoder boundaries using software commands. The software commands are directed to a device called the DS1292 Eliminator which is an electronic replacement for mechanical DIP switches. The Eliminator is nonvolatile and once the switches are set they will remain in the programmed state indefinitely. The interface between the system bus and the Eliminator is developed by the DS1206 Phantom Interface. The DS1206 has the ability to decipher memory cycles which do not impact other system operation into the signals which set the DS1292 to the proper address boundaries. Once the Eliminator is properly set, the logic locks out future changes to the decoder settings.

IBM EXPANSION BUS 62-PIN CONNECTION Figure 1

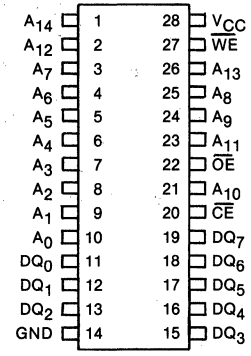


28-PIN BYTEWIDE SOCKET PINOUT Figure 2

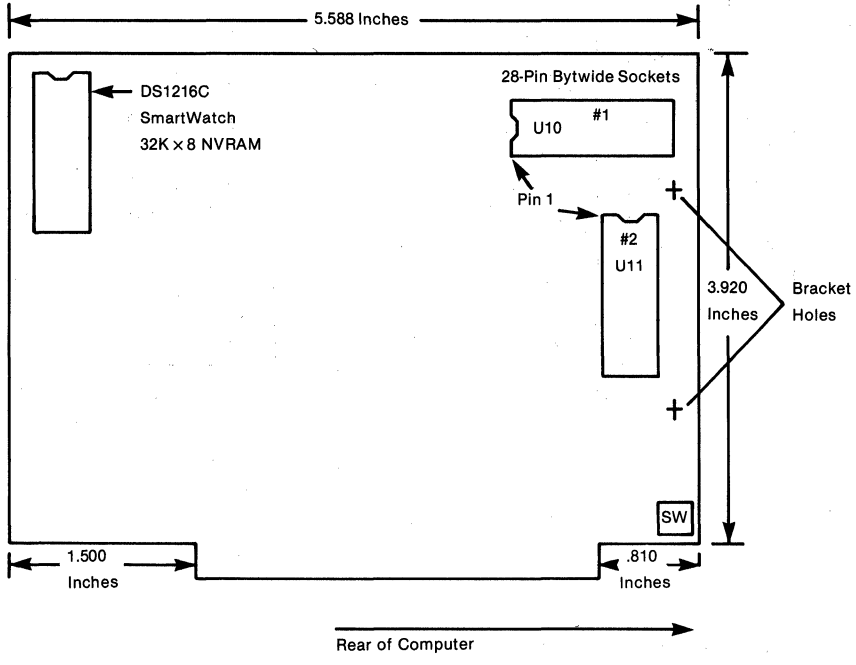
PIN NAMES

A_0-A_{14}	Address Inputs
$\overline{CE}$	Chip Enable
GND	Ground
DQ_0-DQ_7	Data In/Data Out
V_{CC}	Power (+5 V)
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable

PIN CONNECTIONS



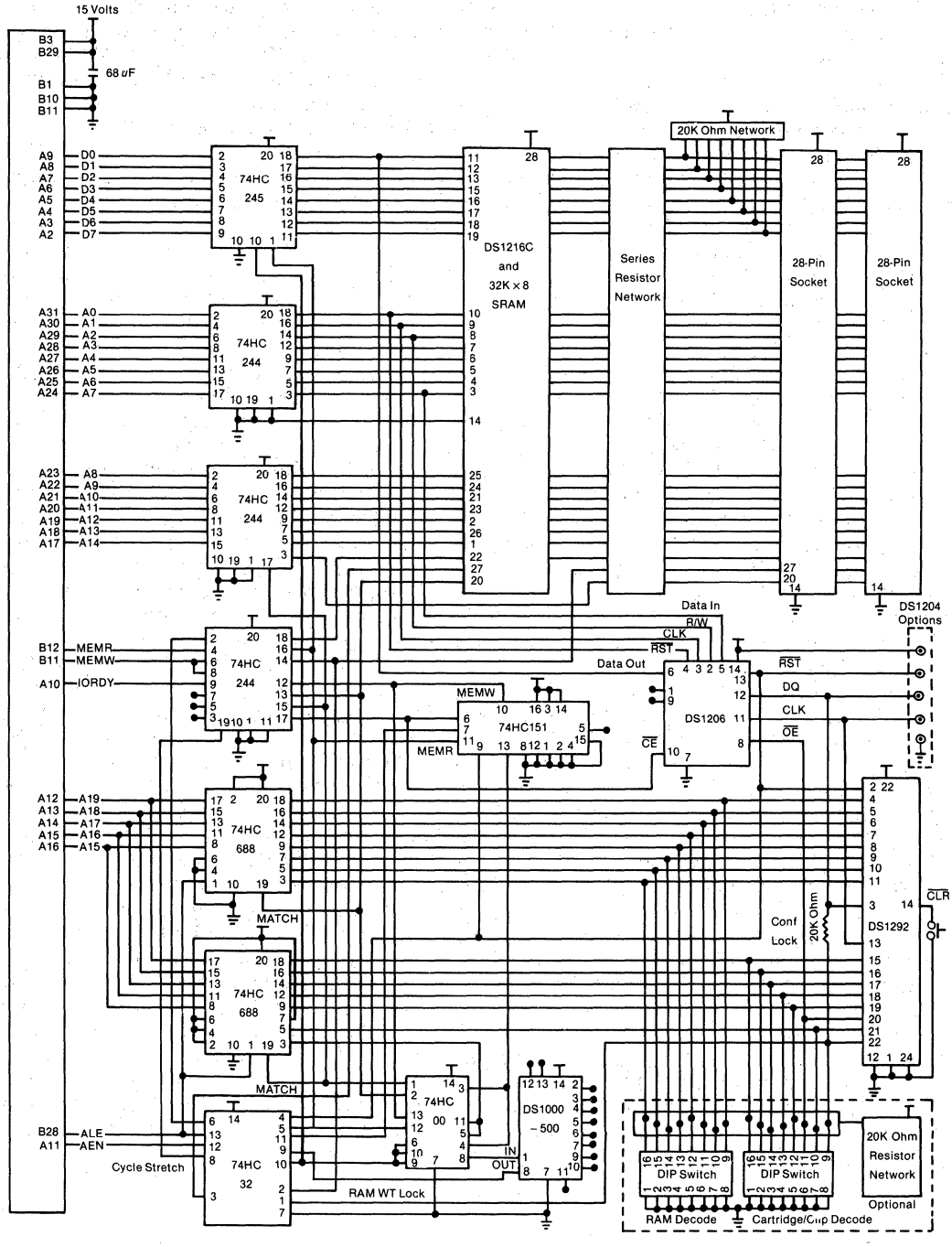
28-PIN BYTEWIDE SOCKET LOCATIONS Figure 3



ELECTRICAL OPERATION

The address bus A0 through A14 arrives at the inputs of two 74HC244 line receivers through the 62-position card edge connector (see Figure 4). Since both of the gate signals are grounded, the 74HC244 acts only as a buffer. All 15 address lines are bused directly through to the Bytewide memory socket sights. A third 74HC244 is used to buffer control signals $\overline{MEMR}$ (Memory Read), $\overline{MEMW}$ (Memory Write) and IORDY (I/O Ready). $\overline{MEMR}$ and $\overline{MEMW}$ are both logically ORed with signals developed by the decoder logic which will be discussed later in this text. The results of this logic produces the $\overline{OE}$ (Output Enable) and the $\overline{WE}$ (Write Enable) signals for the Bytewide memory socket sites. The IORDY line is an output signal from the PC Port card to the computer expansion bus. When this signal is active, the current bus cycle is extended. The DS6010 drives this line low when either a memory read or a write cycle is being executed to one of the 32K × 8 memory blocks. A set of four NAND gates (1-74HC00) and a delay line DS1000 generate a "cycle stretch" signal which controls the length of time that the IBM PC Port will hold the IORDY signal active. As shipped by Dallas Semiconductor, this length of time is set at 500 ns. However, this length of time can be shortened or lengthened by changing the value of the DS1000 delay line. The length of time allotted must be long enough to allow for the propagation delay of the buffers and the access time of the cartridges or cartridge clip which is installed into the 32K × 8 socket sites. The data bus D0 through D7 arrives at a 74HC245 octal transceiver through the 62-position card edge connector. The 74HC245 has both a gate and a direction control. The direction control is set via the $\overline{MEMR}$ signal which is buffered by a 74HC244 line receiver. The direction control will, therefore, set the 74HC245 to drive the system bus whenever the $\overline{MEMR}$ signal is in the active state and when the gate signal is also active. The gate on the 74HC245 is controlled by the logical combinations of $\overline{MEMR}$ and $\overline{MEMW}$ and the match output pin of two 74HC688 8-bit identity comparators. The logic combination of these four signals is accomplished using three two-input NAND gates. The output pins of the 74HC688 also become the $\overline{CE}$ (Chip Enable) inputs for the two 32K × 8 memory blocks. The $\overline{CE}$ signal for the 28-pin sockets for cartridge and cartridge clip connection is buffered through a 74HC244. The gates of the 74HC688 are enabled by the ALE (Address Latch Enable) signal from the computer expansion bus which is active when system bus addresses are valid. Address lines A15 through A19 are connected to the "P" input sides of the 8-bit binary comparator. The Q input sides are connected for the most part to the Eliminator. The comparison of the P and Q sides will, therefore, produce a match output and select one of the 32K × 8 memory boundaries when the Eliminator settings compare to the levels on address lines A15 through A19. The 74HC688, which is used to decode the 32K × 8 block of nonvolatile static RAM, is driven by eight Eliminator outputs to the Q inputs. Since only five address lines are used on the P side, three inputs are tied to fixed levels. The Pin 2 input is connected to V_{CC} and pins 4 and 6 are grounded. The 74HC688, which is used to decode the 32K × 8 block of memory for cartridges or cartridge clips, is driven directly by only 6 Eliminator outputs to the Q inputs. One of the remaining Q inputs is connected to a read or write signal which allows the identity comparator to only output a chip enable signal when a valid read or write cycle is occurring. The other Q input is unused and connected to a fixed high level. Again only five address lines are connected to the P side. The remaining P inputs are tied to a fixed high level. As mentioned earlier, only 6 Eliminator outputs were used by the 74HC688, which is used to decode the memory block for cartridges or cartridge clips. The other two outputs have special functions. The output on pin 22 of the Eliminator is used to lock out the write enable signal which goes to the nonvolatile RAM site. This allows a convenient way in which software can be used to write protect the nonvolatile RAM. The other output on pin 20 of the eliminator is used to lock out the DS1206 Phantom Interface by disabling the $\overline{OE}$ (Output Enable) signal after the

DS6010 PC PORT ELECTRICAL SCHEMATIC Figure 4



Eliminator is set for proper system configuration. Communications to the Eliminator, which allows the system configuration to take place, is handled by the DS1206 Phantom Interface, which is controlled by the 74HC151 data selector and software. Bus cycles which set proper address patterns on address lines A0, A1, A2 and A7 are clocked into the DS1206 using consecutive $\overline{CE}$ cycles. The $\overline{CE}$ for the DS1206 is generated under two different sets of conditions by the 74HC151 based on the state of $\overline{MEMR}$ and $\overline{MEMW}$. Initially, the DS1206 must receive 24 bits of data which must match exactly with the code embedded into the DS1206. (Consult the DS1206 data sheet for exact details on the DS1206 operation.) Prior to this condition, the DS1206 is a passive listener on the bus and will not output any signals to the Eliminator. During this time the $\overline{CE}$ input to the DS1206 from the 74HC151 will be active only when $\overline{MEMW}$ is active (see Table 1). Since write cycles can be accomplished to known memory addresses where ROM resides, no memory alterations occur and these cycles can be transparent to the rest of the system. However, as soon as the 24-bit pattern match is completed, the DS1206 will pass signals to the DS1292 from the address bus. Address line A0 will be passed through as the $\overline{RST}$ (Reset) signal; address line A1 becomes the CLK (Clock); A2 defines whether data is to be read or written; and address A7 becomes the data input to the Eliminator. (Consult the DS1292 data sheet for exact details on Eliminator.) The first requirements for entering data into the Eliminator is to set the $\overline{RST}$ input to a high level. This signal is also sent as an input to the 74HC151 data selector. This new input now allows $\overline{CE}$ for the DS1206 to be active when $\overline{MEMW}$ is active and also when $\overline{MEMR}$ is active and either of the two 74HC688 is outputting a match signal indicating that one of the two 32K × 8 blocks of memory is being accessed. This new set of circumstances allows the Eliminator status to be read back via the system bus DQ0 line. Bus contention is avoided from either of the two 32K × 8 memory blocks as the $\overline{OE}$ signal to the memory blocks is inhibited as long as $\overline{RST}$ to the DS1292 is at a high level. Data is passed back through the DS1206 by the feedback resistor which couples the Eliminator output back to the input. Once the Eliminator is set and verified, system configuration can be terminated and locked by making sure the bit which is output on pin 20 of the Eliminator is set to logic one when the $\overline{RST}$ signal is driven low. The Eliminator can always be put back in an unconfigured state by depressing the $\overline{CLR}$ (Clear) button which forces all of the Eliminator outputs low.

1206 ENABLE Table 1

$\overline{RST}$	$\overline{MEMW}$	$\overline{MEMR}$	$\overline{MATCH}$	$\overline{ENABLE}$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1

$\overline{RST}$	$\overline{MEMW}$	$\overline{MEMR}$	$\overline{MATCH}$	$\overline{ENABLE}$
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

ELECTRICAL OPTIONS

The DS6010 has provisions for mechanical DIP switches and pull-up resistors which can be used in place of the Eliminator. While the DS6010 is not shipped with these components, they can be added if needed for a specific application (see Figure 4). If DIP switches and pullup resistors are used, the Eliminator should be removed from its socket. The DS6010 can also be optioned with the Dallas Semiconductor DS1204 Key for software protection and access control. Under special contract with Dallas Semiconductor, these options can be supplied to customer specifications.

NOTE:

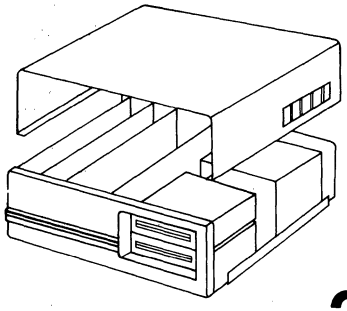
Contact Dallas Semiconductor Sales Office for ordering information.

INSTALLATION

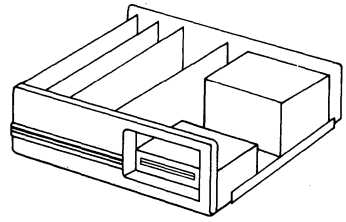
In order to install the DS6010 into a computer it will be necessary for the computer cabinet to be removed (Figure 5). Prior to installation, the computer should be tested to make sure it is operating properly. After the computer has been tested disconnect any peripheral equipment that is attached to the computer and make sure that the A.C. power is unplugged. Then consult the owner's manual on the computer for instructions which explain how to remove the cabinet. After the cabinet is removed, the DS6010 can be installed in any available I/O slot except PC XT Slot B. It is a good idea to connect the ribbon cable which will connect either the Cartridge or the Cartridge Clip to the appropriate 28-pin socket. If the Cartridge or Cartridge Clip is mounted within the computer cabinet, the horizontal 28-pin socket on the top of the PC board would be the proper choice (see Figure 3). When mounting the Cartridge or Cartridge Clip external to the computer, the vertical 28-pin socket should be used. The

INSTALLATION Figure 5

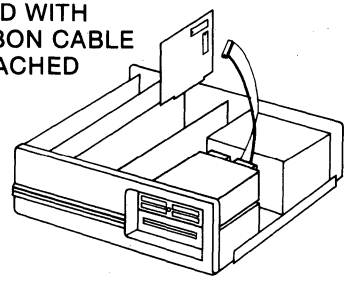
1. REMOVE COVER



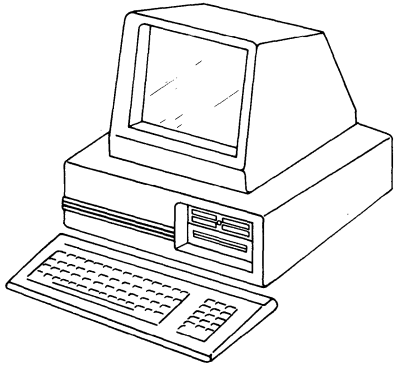
2. REMOVE FLOPPY DISK DRIVE



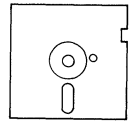
3. INSTALL THE CARTRIDGE CLIP, INSERT THE PC PORT I/O CARD WITH RIBBON CABLE ATTACHED



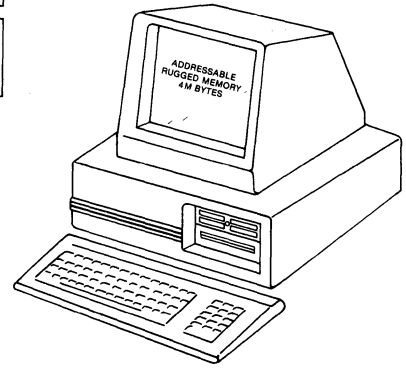
4. REASSEMBLE COMPUTER



5. INSTALL SOFTWARE



6. FUNCTIONAL SOLID-STATE COMPUTER



data sheet on the DS9020 Cartridge Clip can be used for mounting dimensions. The Cartridge Clip will fit in the place of any half-high disk drive. If a DS1217 Cartridge is being used, the DS1217 data sheet can be used to provide mechanical dimensions. Mechanical hardware for mounting the DS1217 is not supplied by Dallas Semiconductor; however, the DS9000 ribbon cable is available to provide electrical connection between the Cartridge and the DS6010. When connecting the ribbon cable to the DS6010, care should be taken to avoid incorrect connection. Pin 1 on the ribbon cable must match Pin 1 on the 28-pin socket. Figure 3 identifies the Pin 1 locations on the 28-pin sockets. Pin 1 is on the opposite end of a color stripe on the ribbon cable. (See the data sheet on the DS9020.) When using the DS9000 ribbon cable with a Cartridge, Pin 1 is on the same end as the color stripe. ***NOTE:*** *Improper connection of the ribbon cable can damage the Cartridge Clip, Cartridge and PC Port.* After the installation is complete the computer cabinet should be replaced and the peripheral devices reconnected. When power is applied to the computer, it should function the same as before the DS6010 was installed. It will be necessary to install the supplied software to make the PC Port operational.

SOFTWARE INSTALLATION

The floppy disk provided with the PC Port contains both the software and the instructions for installing the software. The instructions for installation can be retrieved by installing the floppy disk marked "DS6010 Software" into the default disk drive and typing "TYPE DS6010.MEM" The print command can be used to make a hard copy. This manual should be read and followed carefully while doing the software installation. After the software installation is complete, the system will respond to all DOS commands and the IBM PC Port, Cartridge and Cartridge Clip will appear to behave as added disk storage.

DS6010 PC PORT SPECIFICATION

ORGANIZATION: Two 32K × 8 Memory Blocks
INPUT CONNECTION: IBM PC XT AT Expansion Bus
OUTPUT CONNECTION: JEDEC 28-Pin Bytewide Sockets
ACCESS TIME: 1 *u*S per Byte Maximum*
TEMPERATURE RANGE: 0 °C to 70 °C
SIZE: 1/2 Length I/O Card
5.5 Inches Long × 3.2 Inches High
REAL TIME CLOCK ACCURACY: ± 1 Minute/Month @ 25 °C
SOFTWARE: PC DOS Compatible
POWER CONSUMPTION: 500 MW Maximum
ADDRESS MAP RANGE: 1 Megabyte

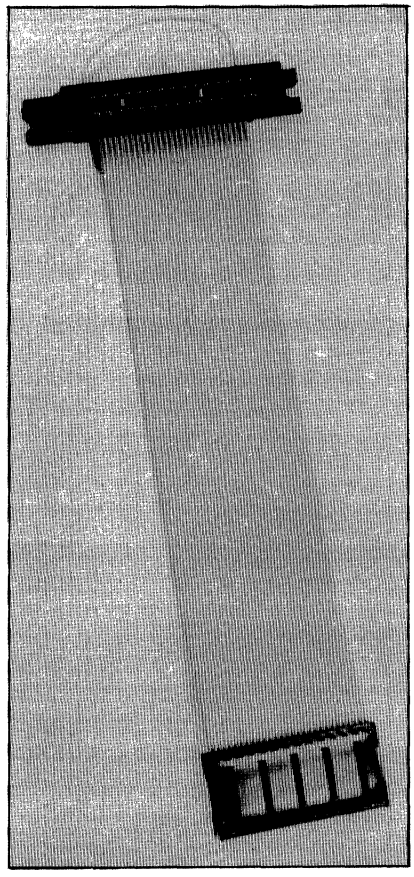
*Performance can be enhanced by lowering the value of the cycle stretch delay line.

Dallas Semiconductor
Byte Wide Cable Harness

DS9000

FEATURES

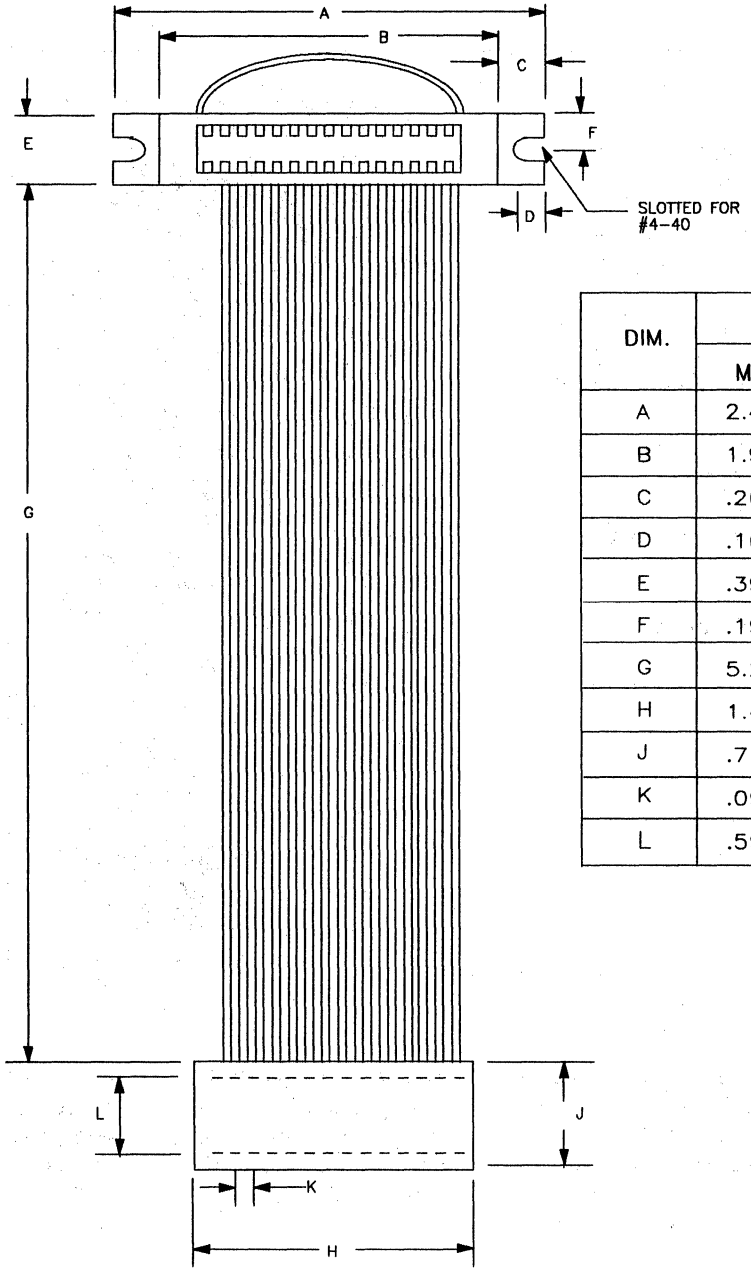
- Converts 30 position card edge to popular byte wide 28 pin socket
- Bifurcated cantilever beam card edge design provides redundant contact
- Mechanical keys provide proper insertion and withdrawal of Dallas Semiconductor DS1217 Nonvolatile Memory Cartridges
- 28 position dip plug inserts into any standard 28 position I.C. Socket
- Color stripe indicates pin one on 28 pin dip plug
- Standard six inch cable length
- Interfaces directly to the DS6010 P.C. Port



DESCRIPTION

The DS9000 is a specially designed cable harness which converts Dallas Semiconductor DS1217 Nonvolatile Memory Cartridges or any other 30 position card edge to the popular Byte Wide 28 Pin Socket. An additional ground lead, and dual key positions allow for proper insertion and withdrawal of Nonvolatile Memory Cartridges. A six inch cable length allows for flexibility in end application but does not substantially effect the performance characteristics of the DS1217 Memory Cartridge.

DS9000
Byte Wide Cable Harness



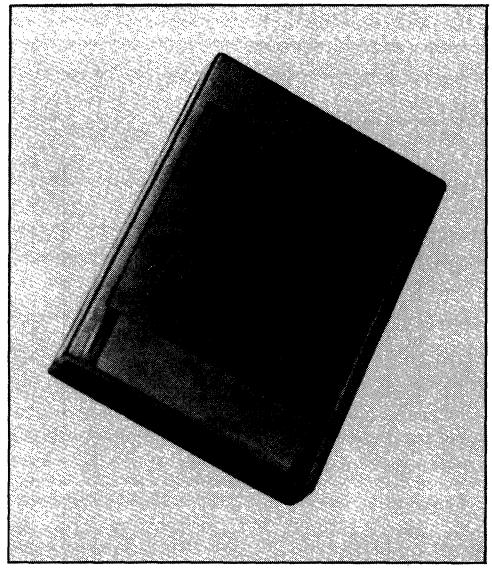
DIM.	INCHES	
	MIN.	MAX.
A	2.480	2.520
B	1.940	1.980
C	.260	.280
D	.160	.175
E	.395	.415
F	.195	.205
G	5.25	5.65
H	1.470	1.500
J	.715	.735
K	.090	.110
L	.590	.610

Dallas Semiconductor
Cartridge Housing

DS9002

FEATURES

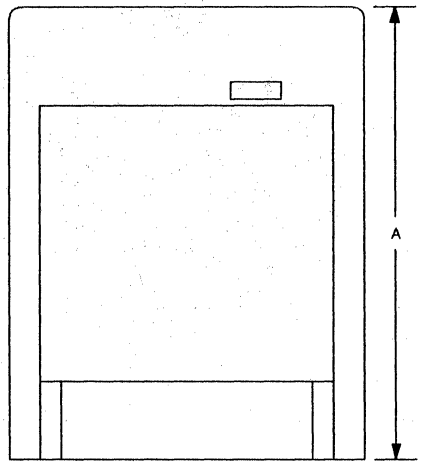
- Two piece snap together construction
- Matches form factor of Dallas Semiconductor nonvolatile memory cartridges
- Made of rugged, flame retarded ABS plastic
- Accepts DS9003 prototype cartridge P.C.B.
- Openning for switch or jumper
- Component clearance of .175" solder side, .200" circuit side using .062" P.C.B.



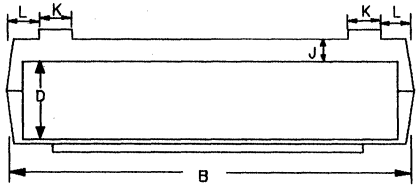
DESCRIPTION

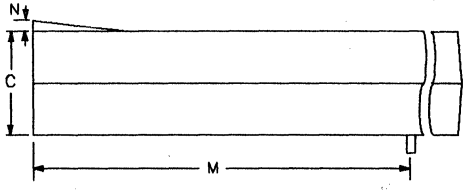
The DS9002 is a rugged, two piece snap together cartridge housing designed for use in any portable cartridge application. Components can be either thru hole mounted or surface mounted on both sides depending upon density requirement and board design. The outside profile of the P.C.B. should match the DS9003 prototype P.C.B. Applications include Nonvolatile Static RAM, ROM, or EPROM memory cartridges.

Cartridge Housing
DS9002



DIM.	INCHES	
	MIN.	MAX.
A	3.020	3.040
B	2.280	2.300
C	.590	.610
D	.440	.460
J	.115	.135
K	.115	.135
L	.140	.160
M	1.760	1.790
N	.040	.060



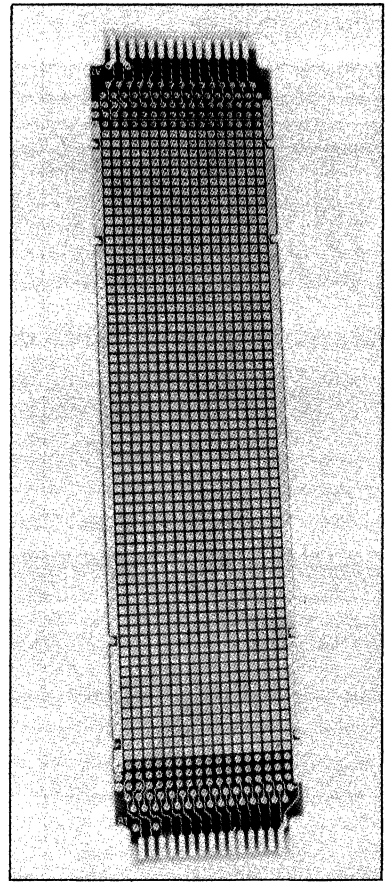


Dallas Semiconductor
Cartridge Proto Board

DS9003

FEATURES

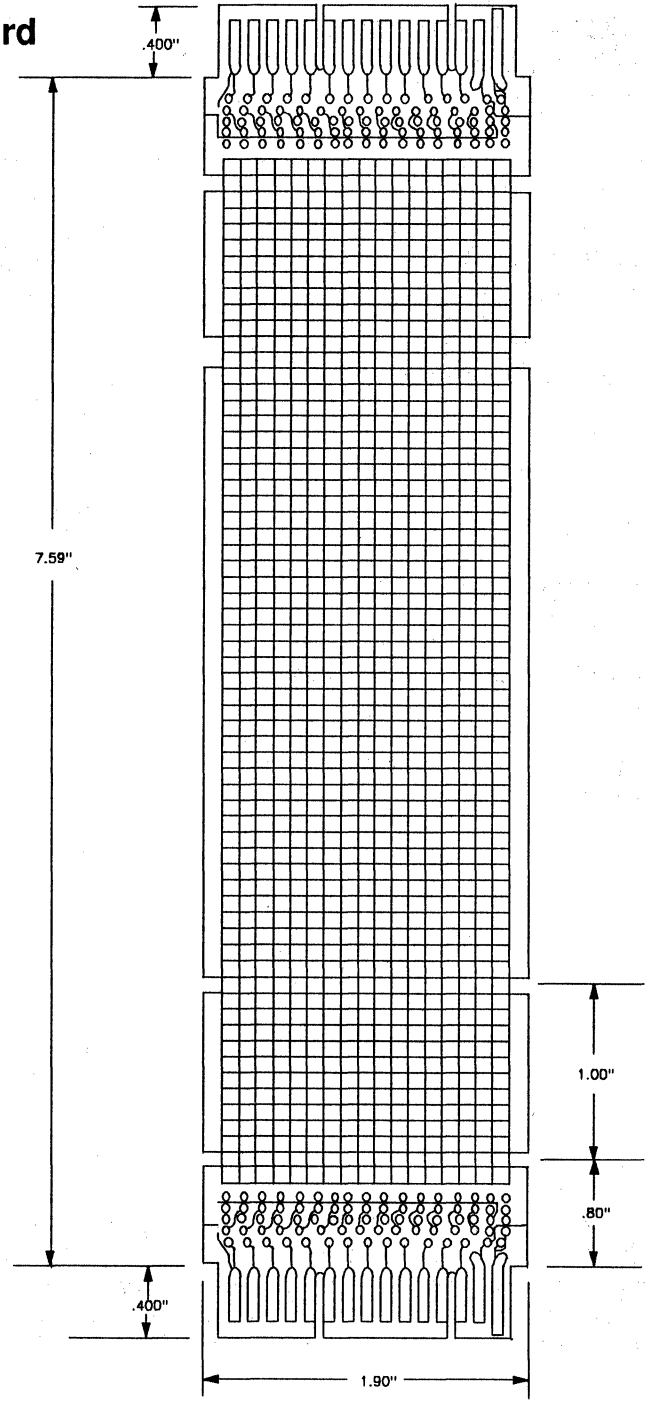
- Matches profile of DS1217 Nonvolatile memory cartridges
- Plated through hole pattern for wire wrap or solder mount development
- Allows for a single double sized cartridge or two standard size cartridges
- Gold plated card edge fingers
- Connects to standard 28 pin bytewide socket via DS9000
- Key slots provide for proper insertion and removal
- Separate full length power and ground buses for ease of layout



DESCRIPTION

The DS9003 is a developmental printed circuit board for prototyping portable hand held cartridges . Thirty gold plated card edge connections conform to the popular 28 pin bytewide socket pin-out when used with the DS9000 cable harness . The card profile matches that of the DS1217 nonvolatile memory cartridges and can be used with the DS9002 cartrige housing.

Cartridge Proto Board
DS9003



Dallas Semiconductor
Cartridge Clip

DS9020

FEATURES

- Holds up to eight nonvolatile read/write memory Cartridges
- Fits within the panel opening of a half-height 5¼″ disk drive
- Mounts with same brackets as disk drive
- Accepts Cartridges ranging from 16K to 4M bits for capacity of up to 4M bytes
- Four user-insertable Cartridges plug into the front
- Four removable Cartridges plug into the rear
- Standard Bytewide pinout connects to JEDEC 28-pin DIP socket via ribbon cable
- Software-controlled banks maintain 32K × 8 JEDEC pin compatability
- Indicator illuminates red while data is transferring
- Rugged and durable construction
- Wide operating temperature range of 0°C to 70°C

DESCRIPTION

The DS9020 Cartridge Clip is a housing with circuitry designed to interface up to eight nonvolatile read/write memory Cartridges to a computer memory bus. The complete unit will fit in the same space which could otherwise hold a standard 5¼″ half-height floppy or hard disk drive. Using a total of 8 DS1217M-4 memory Cartridges in the DS9020 gives a density of 4 megabytes of transportable nonvolatile memory with access time of Static RAM. Four user-insertable memory Cartridges plug into the front of the Cartridge Clip while four removable Cartridges plug into the rear. The Cartridge Clip connects to the computer via a ribbon cable into a standard Bytewide JEDEC 28-pin DIP socket. Software-controlled bank switching techniques provide an expandable memory through a 32K × 8 window within the host computer's memory map. The DS9020 Cartridge Clip provides a rugged, solid-state storage alternative to rotating magnetic memory.

OPERATION

The DS9020 Cartridge Clip includes switching circuitry for up to 8 DS1217 Cartridges. Connection to a computer memory bus is made via a 28-pin DIP adapter with the pinout as shown in Figure 1. Normal read and write memory cycles are directed through the 28-pin DIP and ribbon cable to one of eight Cartridges. (See the data sheet on the DS1217A and DS1217M cartridges for normal read and write cycle timing.) Cartridges are selected by a software-controlled switch which selects only one Cartridge at a time. An indicator on the front of the Cartridge Clip illuminates while the data is being transferred.

CARTRIDGE SELECTION

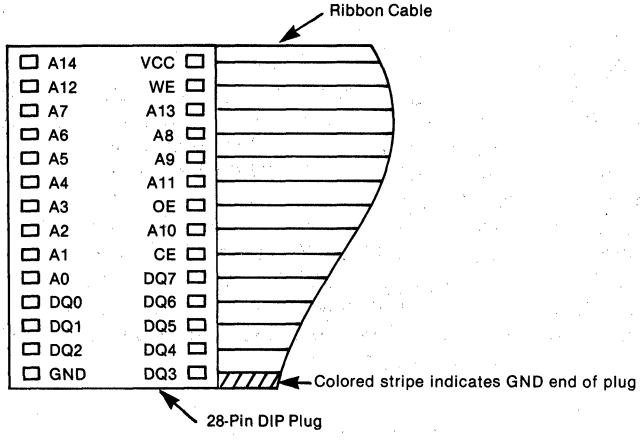
Initially, on power up, all of eight possible Cartridges in the Cartridge Clip are deselected. Cartridge selection is accomplished by matching a predefined pattern stored within the cartridge Clip with a 16-cycle sequence on address lines A_0, A_1, A_2 and A_3. Prior to sending the 16-cycle sequence which will set the bank switch, a read cycle with bit patern 1111 on address inputs A_0, A_1, A_2 and A_3 must be executed to initiate pattern entry. Each set of address inputs is clocked into the the Cartridge Clip when the $\overline{CE}$ pin (Cartridge Clip enable) is driven low. All 16 inputs to the Cartridge Clip must be consecutive read or write cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for address inputs A_1, A_2 and A_3; however, address line A_0 defines the Cartridge number to be enabled as per Table 2.

Switching to a selected Cartridge occurs on the rising edge of Cartridge Clip enable when the last set of bits is input and a match has been established. After Cartridge selection, subsequent Cartridge Clip enables will be directed to the selected Cartridge with additional propagation delay of 150 ns. (Note: this additional delay must be added to the respective DS1217 Cartridge performance specifications when considering overall read and write cycle times.) The selected Cartridge position can be determined from Figure 2. Figure 3 is a block diagram and Figure 4 is an electrical wiring diagram of the DS9020. Figure 5 shows the mechanical and dimensional considerations for the Cartridge Clip.

ADDITIONAL ACCESSORIES AVAILABLE

Dallas Semiconductor offers the DS6010 PC Port which is an I/O expansion board that will connect the DS9020 into PC, XT, AT and compatible computers. For additional information contact Dallas Semiconductor.

CARTRIDGE CLIP Figure 1
28-Pin DIP Plug Interface Pinout



ADDRESS INPUT PATTERN Table 1

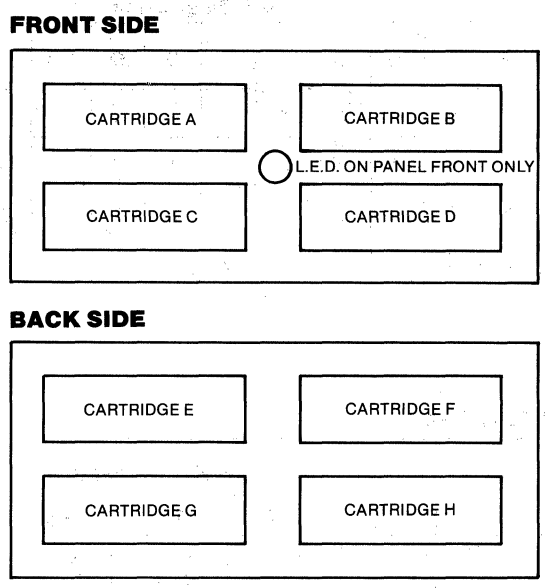
	Bit Sequence															
Address Inputs	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_0	1	0	1	0	0	0	1	1	0	1	0	×	×	×	×	×
A_1	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_2	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_3	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

× See Table 2

BANK SELECT CONTROL Table 2

Bank Selected	**A_0 Bit Sequence**				
	11	**12**	**13**	**14**	**15**
All Cartridges Off	0	DON'T CARE	DON'T CARE	DON'T CARE	DON'T CARE
Cartridge A	1	0	0	0	0
Cartridge B	1	0	0	0	1
Cartridge C	1	0	0	1	0
Cartridge D	1	0	0	1	1
Cartridge E	1	0	1	0	0
Cartridge F	1	0	1	0	1
Cartridge G	1	0	1	1	0
Cartridge H	1	0	1	1	1

Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 85°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28 Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Level	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Input Low Level	V_{IL}	−0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{CC1}		6	50	ma	2
Operating Current	I_{CC2}		15		ma	3
Operating Current	I_{CC3}		40		ma	4
Input Drive Low Level	I_{IL}			1.0	ma	5
Input Drive High Level	I_{LO}			0.5	ma	5
Output Drive @2.4V	I_{OH}	– 1.0			ma	6
Output Drive @0.4V	I_{OL}	2.0			ma	6

CAPACITANCE (t_A = 25 °C)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	500	750	pF	2
D/Q Capacitance	$C_{D/Q}$	500	750	pF	2

A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{CC} = 5V ± 10%)

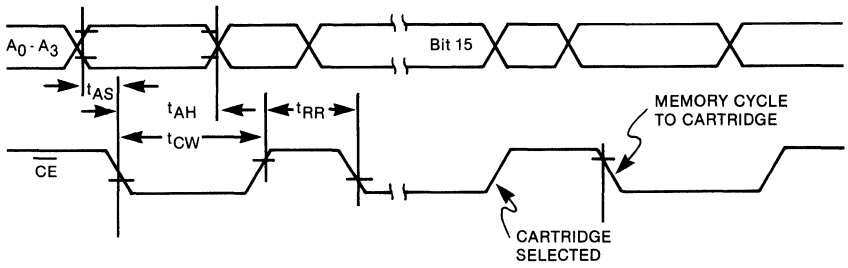
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Set-Up	t_{AS}	20			ns	
Address Hold	t_{AH}	100			ns	
Read Recovery	t_{RR}	80			ns	

DS1217M CARTRIDGE TIMING WHILE INSTALLED IN THE DS9020
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	440			ns	
Access Time	t_{ACC}			400	ns	
$\overline{OE}$ to Output Valid	t_{OE}			275	ns	
$\overline{CE}$ to Output Valid	t_{CO}			400	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	50			ns	
Output High Z From Deselection	t_{OD}			125	ns	
Output Hold From Address Change	t_{OH}	10			ns	
Read Recovery Time	t_{RR}	40			ns	
Write Cycle Time	t_{WC}	440			ns	
Write Pulse Width	t_{WP}	350			ns	
Address Set Up Time	t_{AW}	40			ns	
Write Recovery Time	t_{WR}	40			ns	
Output High Z From $\overline{WE}$	t_{ODW}			100	ns	
Output Active From $\overline{WE}$	t_{OEW}	10			ns	
Data Set Up Time	t_{DS}	280			ns	
Data Hold Time From $\overline{WE}$	t_{DH}	25			ns	

See DS1217M data sheet for timing diagrams.

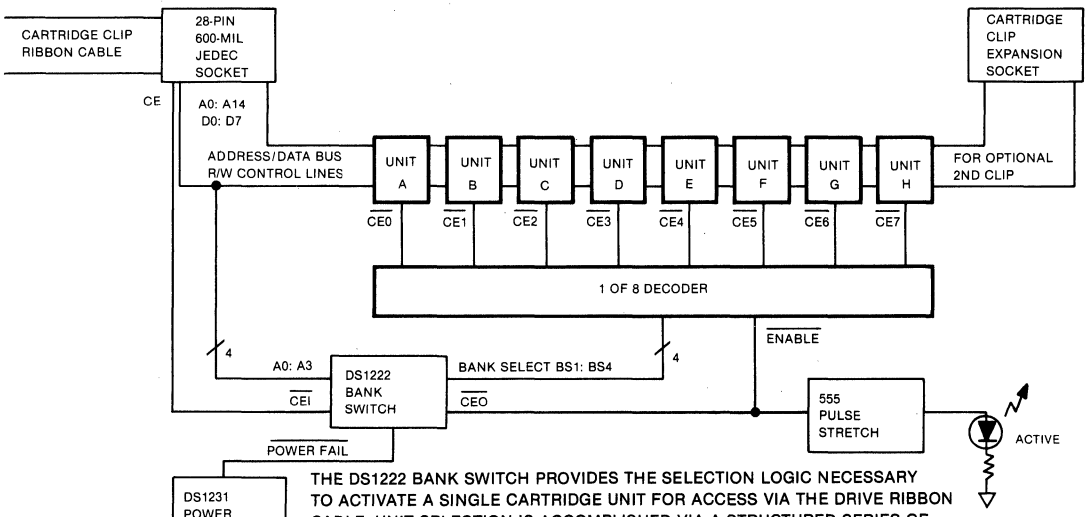
TIMING DIAGRAM—CARTRIDGE SELECTION



NOTES:

1. All voltages are referenced to ground (Pin 14).
2. Cartridge Clip empty.
3. Cartridge Clip loaded to capacity with $\overline{CE}$ at high level.
4. Cartridge Clip loaded to capacity with $\overline{CE}$ at low level.
5. Includes all address, data and control lines.
6. Output drive comes from installed Cartridge.

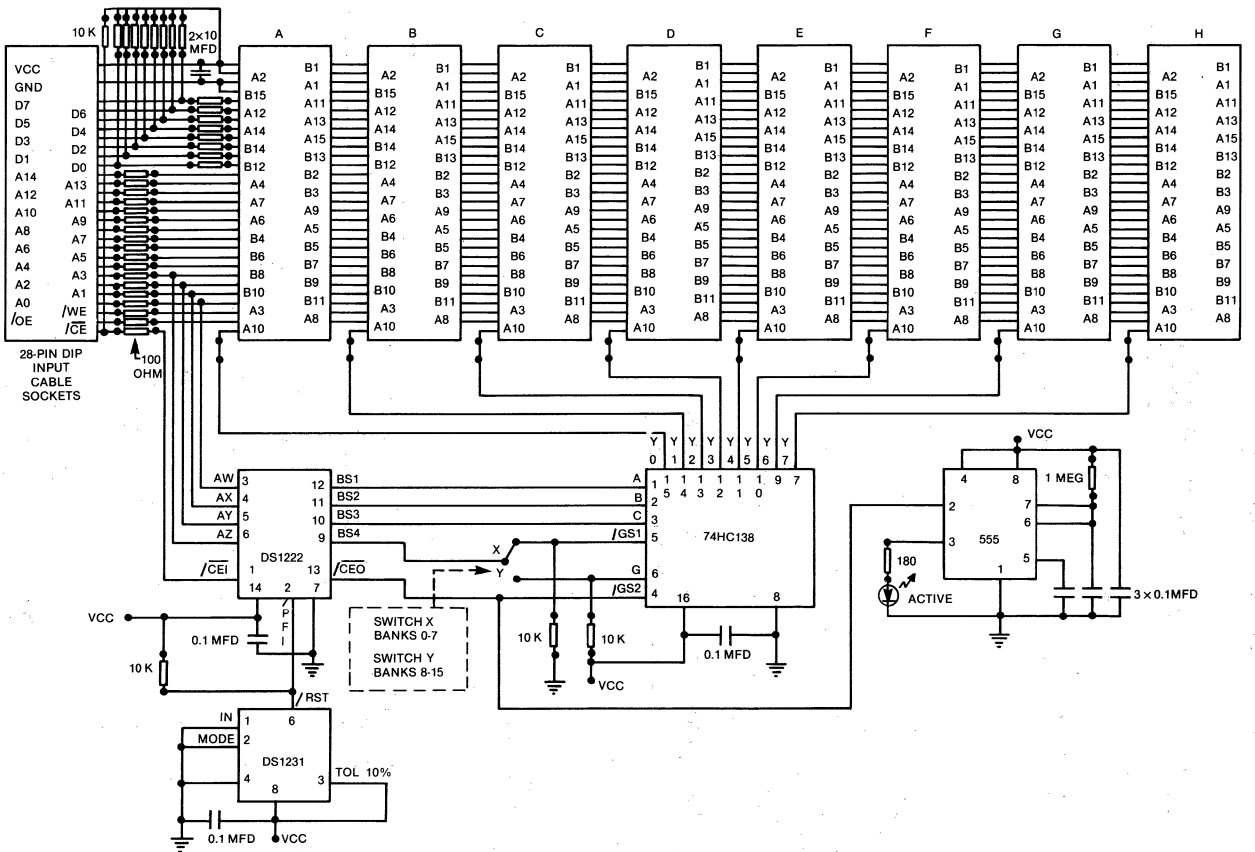
Figure 3



THE DS1222 BANK SWITCH PROVIDES THE SELECTION LOGIC NECESSARY TO ACTIVATE A SINGLE CARTRIDGE UNIT FOR ACCESS VIA THE DRIVE RIBBON CABLE. UNIT SELECTION IS ACCOMPLISHED VIA A STRUCTURED SERIES OF READ CYCLES TO THE CARTRIDGE CLIP.

THE DS1231 POWER MONITOR PROVIDES FAIL DETECTION AND POWER-UP RESET FUNCTIONS. ACCESS TO THE CARTRIDGE UNITS IS DENIED WHEN POWER IS LOW AND UNTIL UNIT SELECTION PROTOCOL IS ACTIVATED ON SYSTEM POWER-UP.

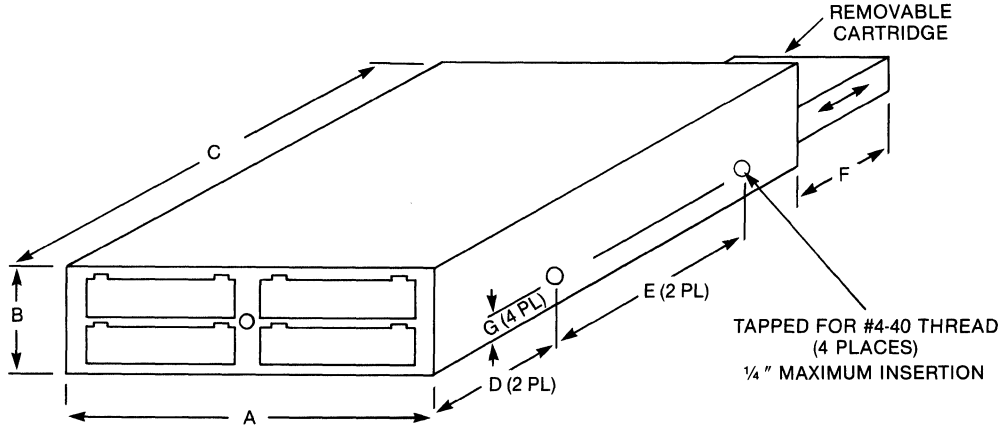
Figure 4


10 K
2×10 MFD
A
B
C
D
E
F
G
H
VCC
GND
D7
D5
D3
D1
A14
A12
A10
A8
A6
A4
A2
A0
/OE
D6
D4
D2
D0
A13
A11
A9
A7
A5
A3
A1
/WE
/CE
28-PIN DIP INPUT CABLE SOCKETS
100 OHM
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
AW
AX
AY
AZ
/CEI
DS1222
BS1
BS2
BS3
BS4
/CEO
A
B
C
/GS1
G
/GS2
74HC138
X
Y
VCC
0.1 MFD
10 K
PFI
/RST
SWITCH X BANKS 0-7
SWITCH Y BANKS 8-15
IN
MODE
DS1231
TOL 10%
0.1 MFD
VCC
10 K
10 K
0.1 MFD
VCC
180
ACTIVE
555
1 MEG
3×0.1MFD

DS9020
Cartridge Clip

Figure 5

DIM.	INCHES	
	MIN.	MAX.
A	5.700	5.760
B	1.605	1.635
C	6.460	6.500
D	2.045	2.065
E	3.100	3.120
F	1.210	1.510
G	.390	.410

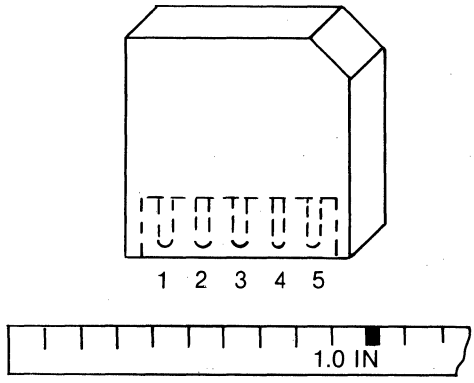


Security Products

FEATURES

- Cannot be deciphered by reverse engineering
- Partitioned memory thwarts pirating
- User insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64 bit reprogrammable memory
- Unreadable 64 bit security match code virtually prevents deciphering by exhaustive search with over 10^{19} possibilities
- 128 bits of secure read/write memory creates additional barriers against hackers by permitting data changes as often as needed
- Rapid erasure of identification security match code, and secure read/write memory can occur if tampering is detected
- User insertable
- Over 10 years of data retention with no limitations or restrictions on write cycle
- Low power CMOS circuitry
- 4 million bits/second data rate
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

PIN CONNECTIONS



PIN NAMES

Pin 1 — V_{CC}	+5 VOLTS
Pin 2 — $\overline{RST}$	$\overline{RESET}$
Pin 3 — DQ	DATA INPUT/OUTPUT
Pin 4 — CLK	CLOCK
Pin 5 — GND	GROUND

9

DESCRIPTION

The DS1204U Electronic Key is a miniature security system which stores 64 bits of user definable identification code and a 64 bit security match code which protects 128 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the key via a special program mode operation. After programming, the key follows a special procedure with a serial format to retrieve or update data.

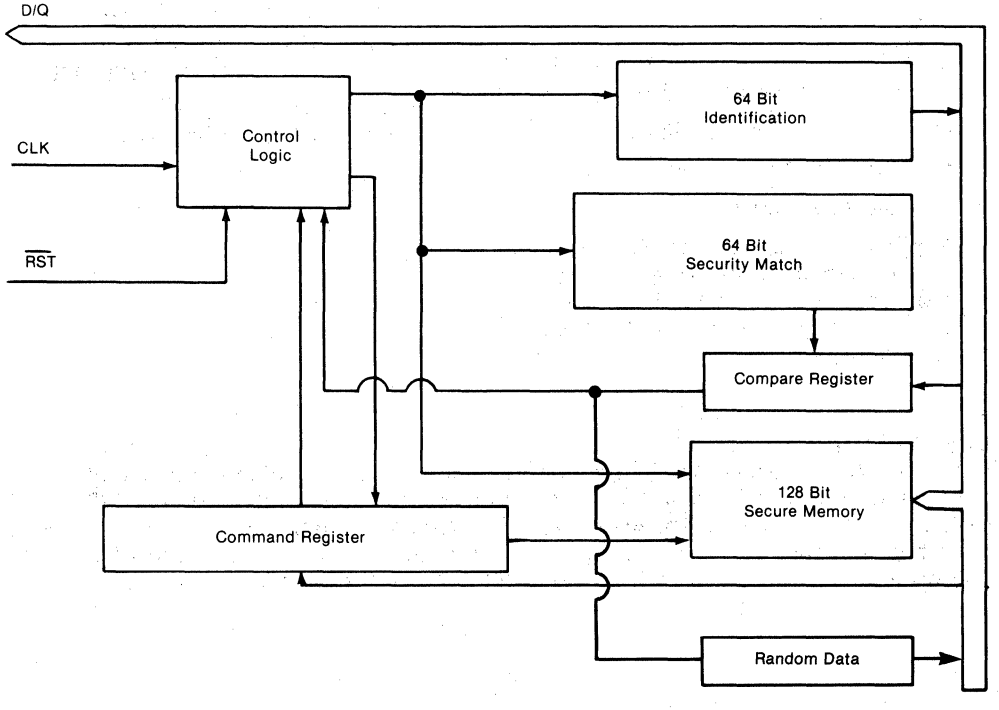
Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfer with only three signals: CLOCK, RESET, and DATA INPUT/OUTPUT.

Low pin count and a guided entry for a mating receptacle overcomes mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user insertable.

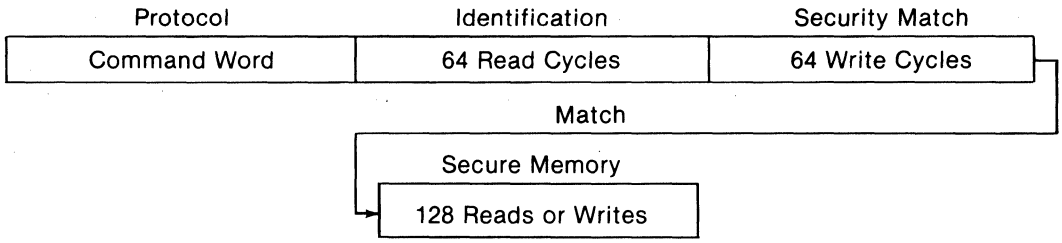
OPERATION—NORMAL MODE

The Electronic Key has two modes of operation: the normal mode and the program mode. The block diagram (Figure 1) illustrates the main elements of the key when used in the normal mode. To initiate data transfer with the key, RST is taken high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact bit pattern which defines normal operation for read or write or communications is ignored. If the command register is loaded properly, communications are allowed to continue. The next 64 cycles to the key are read. Data is clocked out of the key on the high to low transition of the clock from the identification memory. Next, 64 write cycles must be written to the compare register. These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, random data is output for the next 128 cycles when reading data. If write cycles are being executed, the write cycles are ignored. If a match is found, access is permitted to a 128-bit read/write nonvolatile memory. Figure 2 is a summary of normal mode operation and Figure 3 is a flow chart of the normal mode sequence.

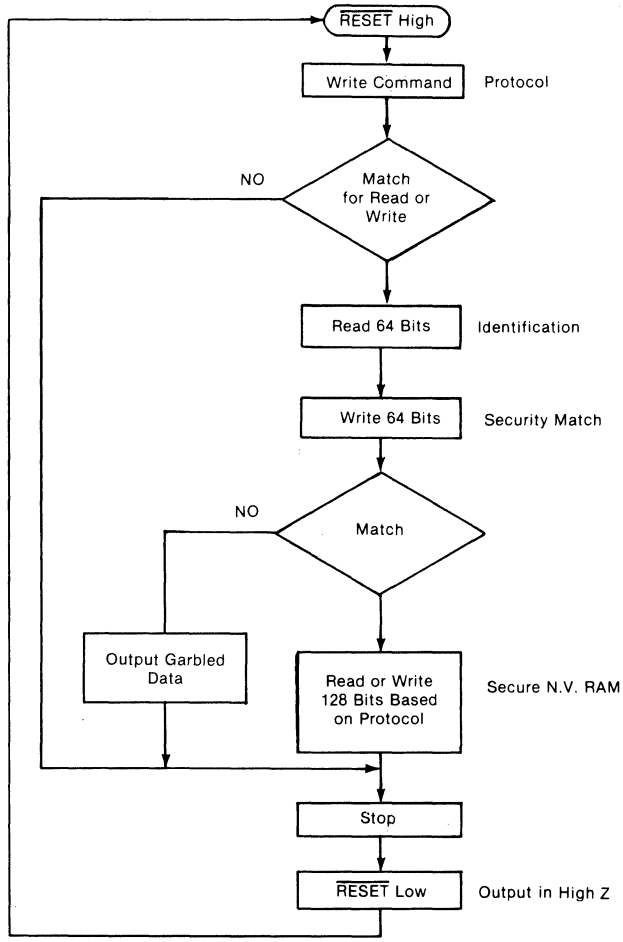
BLOCK DIAGRAM — NORMAL MODE Figure 1



SEQUENCE — NORMAL MODE Figure 2



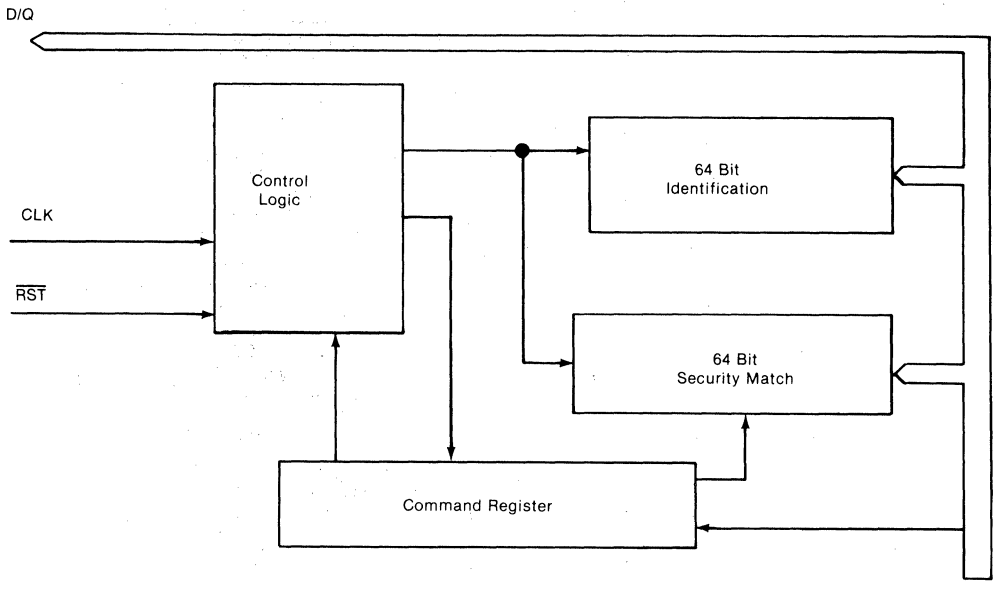
FLOW CHART — NORMAL MODE Figure 3



PROGRAM MODE

The block diagram of Figure 4 illustrates the main elements of the key when used in the program mode. To initiate the program mode, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact pattern which defines program operation. If an exact match is not found, the remainder of the program cycle is ignored. If the command register is properly loaded, then the next 128 bits which follow are written to the identification memory and the security match memory. Figure 5 is a summary of program mode operation and Figure 6 is a flow chart of program mode operation.

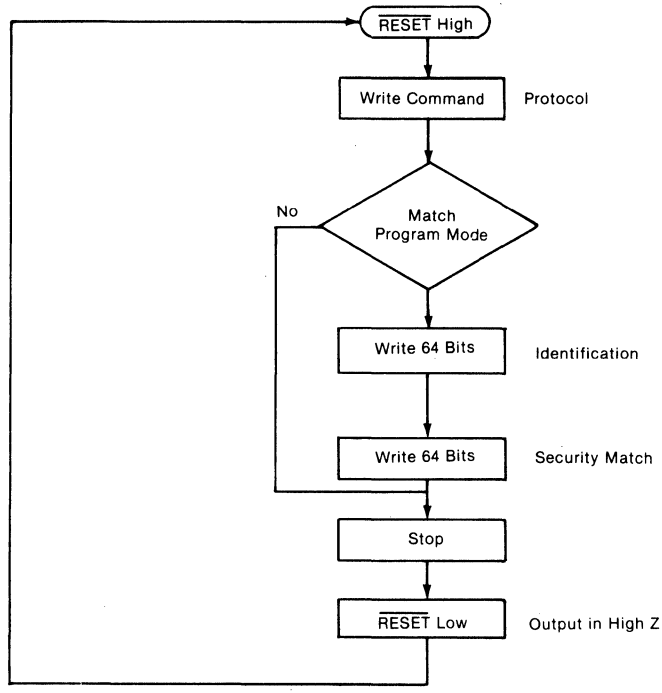
BLOCK DIAGRAM — PROGRAM MODE Figure 4



SEQUENCE — PROGRAM MODE Figure 5

Protocol	Identification	Security Match
Command Word	64 Write Cycles	64 Write Cycles

FLOW CHART — PROGRAM MODE Figure 6



COMMAND WORD

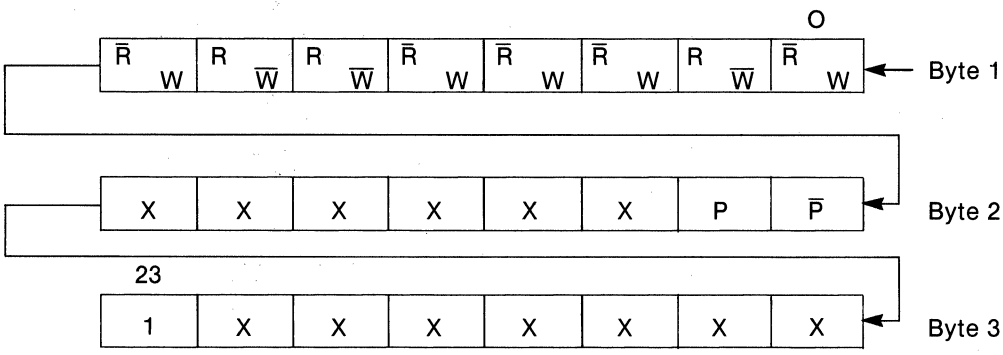
Each data transfer for the normal and program mode begins with a three byte command word as shown in Figure 7. As defined, the first byte of the command word specifies whether the 128 bit nonvolatile memory will be written into or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted.

The 8 bit pattern for read is 01100010. The pattern for write is 10011101. The first two bits of the second byte of the command word specify whether the data transfer to follow is a program or normal cycle. The bit pattern for program is 0 in bit 0 and 1 in bit 1. The program mode can be selected only when the first byte of the command word specifies a write. If the program mode is specified and the first byte of the command word does not specify a write, data transfer will be aborted. The bit pattern which selects the normal mode of operation is 1 in bit 0 and 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause data transfer to abort.

The remaining 6 bits of byte 2 and the first 7 bits of byte 3 form unique patterns which allow multiple keys to reside on a common bus. As such, each respective code pattern must be written exactly for a given device or data transfer will abort. Dallas Semiconductor has 5 patterns available as standard products per the chart in Figure 7. Each pattern corresponds to a specific part number. Under special contract with Dallas Semiconductor the user may specify any bit pattern other than that specified by Dallas Semiconductor as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last bit of byte 3 of the command word must be written to logic 1 or data transfer will abort.

NOTE: Contact Dallas Semiconductor Sales Office for special command word code assignment which makes possible an exclusive blank key.

COMMAND WORD Figure 7



DS1204U-1	0	0	0	0	0	0	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-2	0	0	0	0	0	1	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-3	0	0	0	0	1	0	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-4	0	0	0	0	1	1	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-5	0	0	0	1	0	0	P	$\overline{P}$	Byte 2
	1	0	1	0	0	0	0	0	Byte 3

RESET AND CLOCK CONTROL

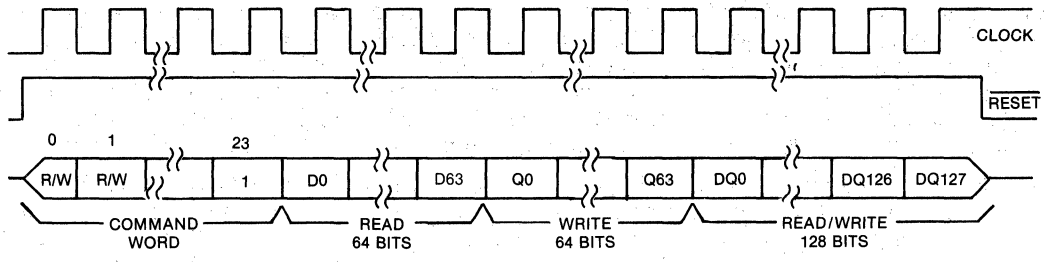
All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2 mA @ 3.0 volts is required. However, if the V_{CC} pin is connected to a 5 volt source within nominal limits, then $\overline{RST}$ is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 uA. Third, the $\overline{RST}$ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates if the $\overline{RST}$ pin is low and the DQ pin goes to a high impedance state. When data transfer to the key is terminated and using $\overline{RST}$, the transition of $\overline{RESET}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 8 for normal mode and Figure 9 for program mode.

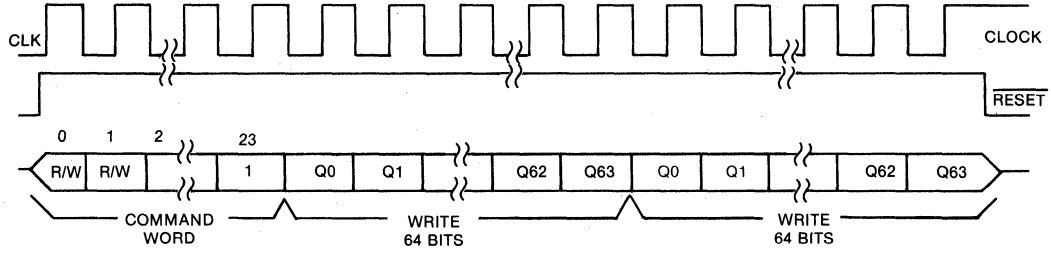
KEY CONNECTIONS

The key is designed to be plugged into a standard 5 pin 0.1 inch center SIP receptacle. A guide is provided to prevent the key from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the key pins can be determined to insure connection integrity before data transfer begins. CLK, $\overline{RST}$, and DATA INPUT/OUTPUT all have internal 20K Ohm pull down resistors to ground which can be sensed by a reading device.

DATA TRANSFER — NORMAL MODE Figure 8



DATA TRANSFER — PROGRAM MODE Figure 9



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	−1.0V to +7V
OPERATING TEMPERATURE	—	0°C to 70°C
STORAGE TEMPERATURE	—	−40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1,8,10
Logic 0	V_{IL}	−0.3		+0.8	V	1
$\overline{\text{RESET}}$ Logic 1	V_{IHE}	3.0			V	1,9,11
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	μA	4
Output Leakage	I_{LO}			+500	μA	
Output Current @ 2.4V	I_{OH}	−1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
$\overline{\text{RST}}$ Input Resistance	Z_{RST}	10		40	KΩ	
D/Q Input Resistance	Z_{DQ}	10		40	KΩ	
CLK Input Resistance	Z_{CLK}	10		40	KΩ	
$\overline{\text{RST}}$ Current @3.0V	I_{RST}			2	mA	6,9,13
Active Current	I_{CC1}			6	mA	6
Standby Current	I_{CC2}			2.5	mA	6

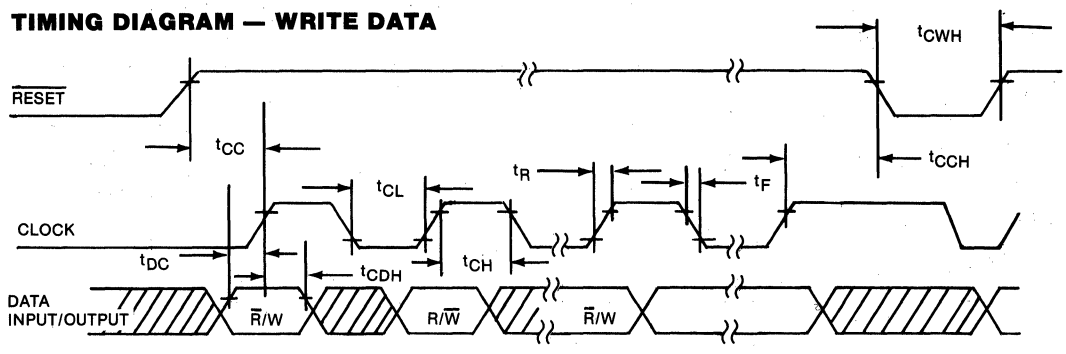
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

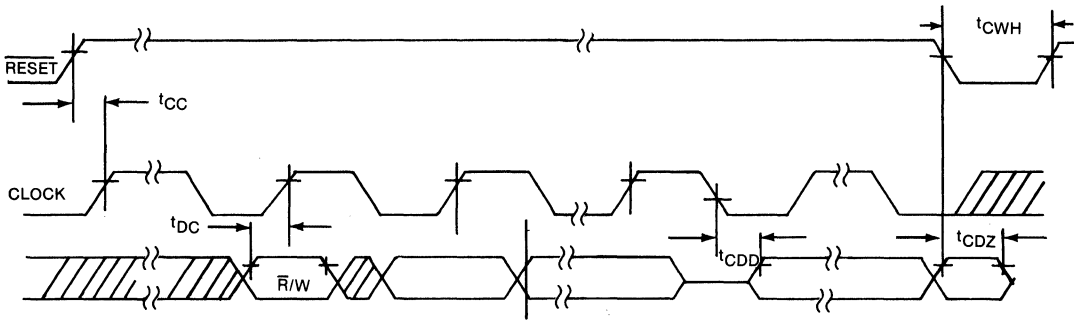
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	35			ns	2,7
CLK to Data Hold	t_{CDH}	40			ns	2,7
CLK to Data Delay	t_{CDD}			100	ns	2,3,5,7
CLK Low Time	t_{CL}	125			ns	2,7
CLK High Time	t_{CH}	125			ns	2,7
CLK Frequency	f_{CLK}	D.C.		4.0	MHZ	2,7
CLK Rise & Fall	t_R, t_F			500	ns	2,7
$\overline{RST}$ To CLK Set Up	t_{CC}	1			us	2, 7
CLK To $\overline{RST}$ Hold	t_{CCH}	40			ns	2, 7
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	2,7,14
$\overline{RST}$ To I/O High Z	t_{CDZ}			50	ns	2, 7

TIMING DIAGRAM — WRITE DATA



TIMING DIAGRAM — READ DATA



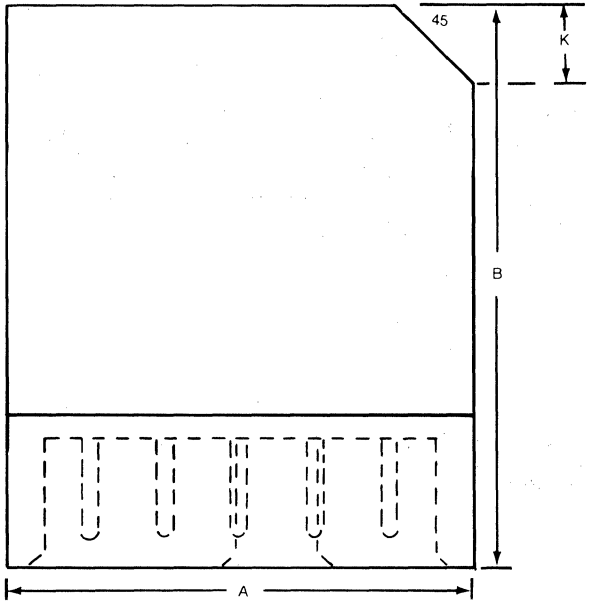
1. All voltages are referenced to GND.
2. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8V$ and 10 ns maximum rise and fall time.
3. Measured at $V_{OH} = 2.4$ volts and $V_{OL} = 0.4$ volts.
4. For CLK, D/Q, and $\overline{RST}$
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at V_{IH} of $\overline{RST} \geq 3.0V$ when $\overline{RST}$ supplies power.
8. Logic 1 maximum is V_{CC} + 0.3 volts if the V_{CC} pin supplies power and $\overline{RST}$ + 0.3 volts if the $\overline{RST}$ pin supplies power.
9. Applies to $\overline{RST}$ when $V_{CC} < 3.0$ V.
10. Input levels apply to CLK, DQ, and $\overline{RST}$ while V_{CC} is within nominal limits. When V_{CC} is not connected to the key, then $\overline{RST}$ input reverts to V_{IHE}.
11. $\overline{RST}$ Logic 1 maximum is V_{CC} + 0.3 volts if the V_{CC} pin supplies power and 5.5 volts maximum if $\overline{RST}$ supplies power.
12. Each DS1204U is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13. Average A.C. $\overline{RST}$ current can be determined using the following formula:

    $$I_{TOTAL} = 2 + I_{LOAD\ D.C.} + (4 \times 10^{-3})(C_L + 140)\ f$$

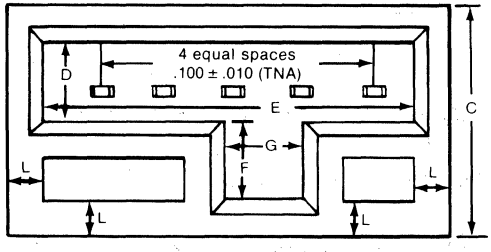
    I_{TOTAL} and I_{LOAD} are in mA; C_L is in pF; f is in MHZ.

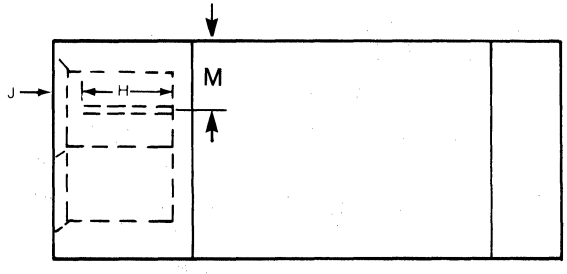
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHZ gives an I_{TOTAL} of 5 MA.
14. When $\overline{RST}$ is supplying power t_{CWH} must be increased to 100 ms.

Electronic Key
DS1204U

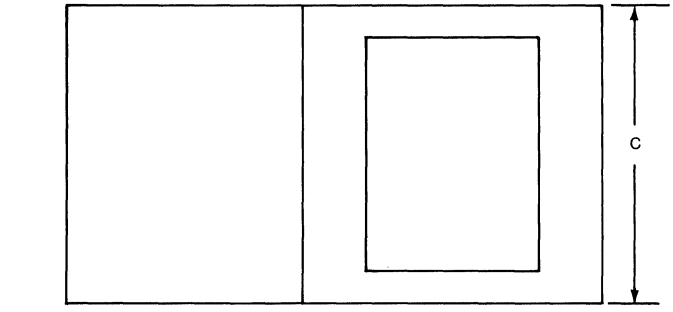


DIM.	INCHES	
	MIN.	MAX.
A	.610	.630
B	.740	.760
C	.310	.330
D	.100	.110
E	.515	.525
F	.100	.110
G	.100	.110
H	.110	.130
J	.030	.050
K	.045	.055
L	.045	.055
M	.100	.110

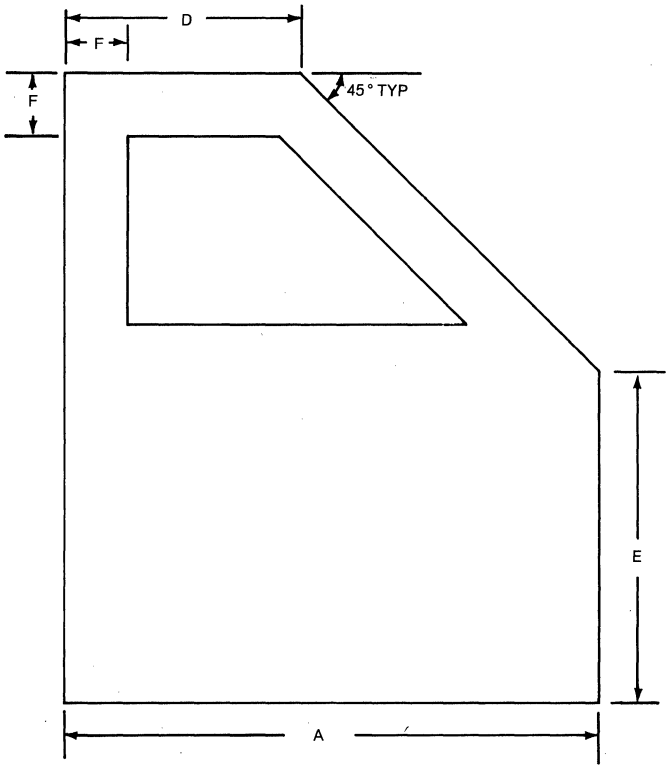


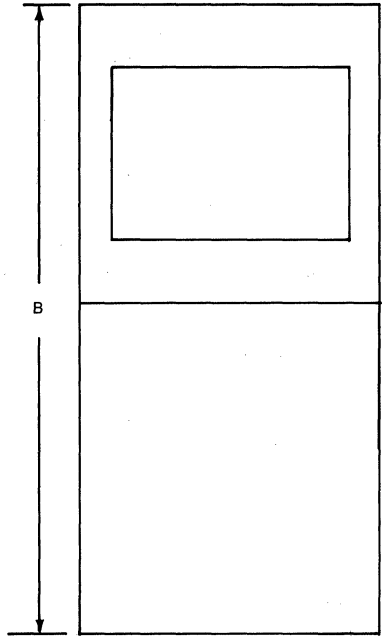


Key/Tag Holder
DS9090



DIM.	INCHES	
	MIN.	MAX.
A	.670	.690
B	.790	.810
C	.370	.390
D	.290	.310
E	.410	.430
F	.070	.090





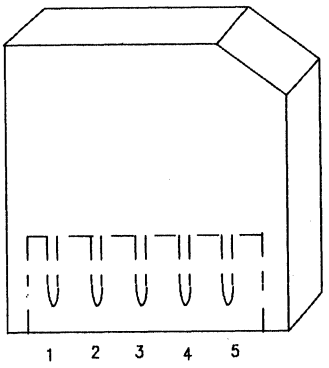
Dallas Semiconductor
TIMEKEY

PRELIMINARY
DS1207

FEATURES

- Cannot be deciphered by reverse engineering
- Time allotment from 1 day to 512 days for trial periods, rentals, and leasing
- Partitioned memory thwarts pirating
- User insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64 bit reprogrammable memory
- Unreadable 64 bit match code virtually prevents discovery by exhaustive search with over 10^{19} possibilities
- Random data generation on incorrect match codes obscures real accesses
- 384 bits of secure read/write memory creates additional barriers against hackers by permitting data changes as often as needed
- Rapid erasure of identification security match code, and secure read/write memory can occur if tampering is detected
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

PIN CONNECTIONS



PIN NAMES

pin 1- no connection
pin 2- $\overline{RST}$ reset
pin 3- DQ data input/output
pin 4- CLK clock
pin 5- GND ground

DESCRIPTION

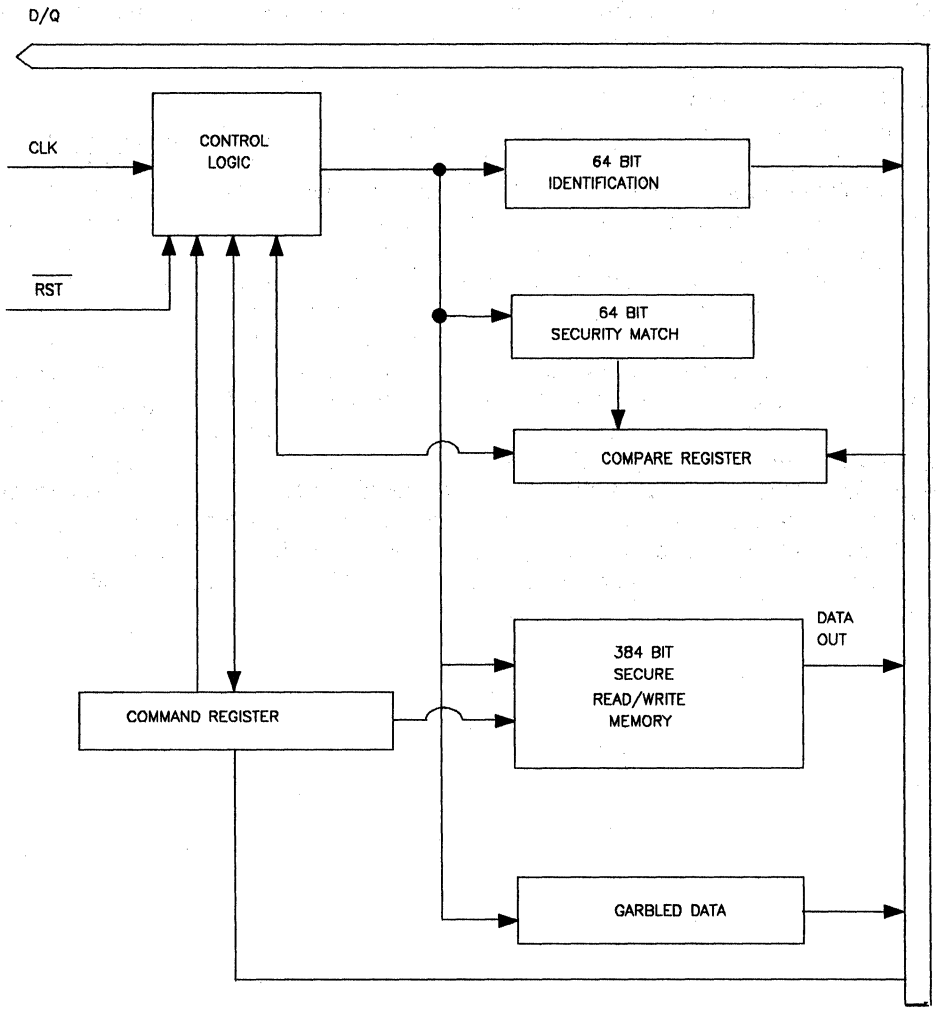
The DS1207 TimeKey is a miniature security system which stores 64 bits of user definable identification code and a 64 bit security match code which protects 384 bits of read/write nonvolatile memory. The 64 bit identification code, and the security match code, are programmed into the TimeKey via a special program mode operation. After programming, the TimeKey follows a special procedure with a serial format to retreive or update data. The TimeKey is set to expire in from one day to 512 days or infinity, as specified by the customer. The TimeKey starts its countdown from the first access by the end user.

Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfer with only three signals: CLOCK, $\overline{\text{RESET}}$, and DATA INPUT/OUTPUT. Low pin count and a guided entry for a mating receptacle overcomes mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user insertable.

OPERATION - NORMAL MODE

The TimeKey has two modes of operation: The normal mode and the program mode. The normal mode of operation provides the functions of reading and writing the 384 bit secure memory. The block diagram (Figure 1) illustrates the main elements of the TimeKey when used in the normal mode. To initiate data transfer with the TimeKey $\overline{\text{RST}}$ is taken high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact bit pattern which defines normal operations with a function code of read or write. If one of these patterns is not matched, communication is ignored. If the command register is loaded properly, communications are allowed to continue. Data is clocked out of the TimeKey on the high to low transition of the clock. If the pattern matched in the command register calls for a normal read or write, the next 64 cycles following the command word are read and data is clocked out of the identification memory. The next 64 write cycles are written to the compare register (Figure 2). These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, if normal read mode is selected, random garbled data is output for the next 384 cycles. If a normal write cycle is selected and a match is not achieved, the TimeKey will ignore any additional information. However, when a security match is achieved, access is permitted to the 384 bit secure memory.

FIGURE 1
BLOCK DIAGRAM-NORMAL MODE



OPERATION - PROGRAM MODE

The program mode of operation provides the functions of programming the identification and security match memory and setting and reading the amount of time the TimeKey can be used. The block diagram of Figure 3 illustrates the main elements of the TimeKey when used in the program mode. To initiate the program mode, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact bit pattern which defines program mode for the identification and security match bits or program mode for setting and reading the amount of time for which the TimeKey can be used. If an exact match for one of the seven function codes of the program mode is not found, the remainder of the program mode is ignored. When the command register is properly loaded for programming the identification and security match bits, the next 128 bits which follow are written to the identification and security match memory (Figure 4). When this mode of operation is invoked, all memory contents are erased.

SETTING AND READING TIME REMAINING

There are six functions of the program mode which are used to set or read the amount of time in which the TimeKey will allow full operation. To initiate any of the six functions of the program mode used for setting and reading time remaining, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low to high transition of the CLK input. If the command register is properly loaded with the function code for reading the 20 bit day clock counter, the next 20 bits will be output (LSB first) as a binary count of the amount of time elapsed in the current day (see Figure 5). The time can be calculated by dividing this count reading by 2^{20} (20 bits is equal to 1,048,576 counts). One minus this result is the fraction of a day remaining. The 20 bit day clock counter is driven by an internal oscillator which has a period of 82.4 ms. If the command register is properly loaded with the function code for reading the 9 bit number of days counter, the next 9 bits will be output (LSB first) as a binary count of the days remaining (see Figure 6). This count is decremented each time the day clock counter rolls over to zero. When the number of days remaining counter rolls through zero, normal and program mode write cycles are inhibited. If program mode read cycle to the number of days counter is attempted, the nine bits will be returned as all ones.

If the command register is properly loaded with the function code for writing the nine bit number of days counter, the next nine bits will be input (LSB first) as a binary count of the desired number of days in which the TimeKey will be fully functional (see Figure 7). The number of days counter can be changed by writing over an entered value as often as required until the lock command is entered. The lock command is given when the command register is properly loaded with the function code for locking up the number of days counter. The lock command consists of the 24 bit command word only (see Figure 8). Once the lock command is given, all future write cycles to the number of days register is ignored. After the correct value has been written and locked into the number of days counter, the DS1207 will start counting the time from the entered value to zero after the first access to the TimeKey is executed provided the arm oscillator bit is set. The arm oscillator bit is set when the command register has been properly loaded with the function code for arming the oscillator. The arm oscillator command consists of the 24 bit command word only (see Figure 9). One other command is also available for use in setting and reading time remaining. A stop oscillator command is given when the command register is properly loaded with the function code for stopping the oscillator. The stop oscillator command consists of the 24 bit command word only (see Figure 10). This command will only execute prior

FIGURE 2

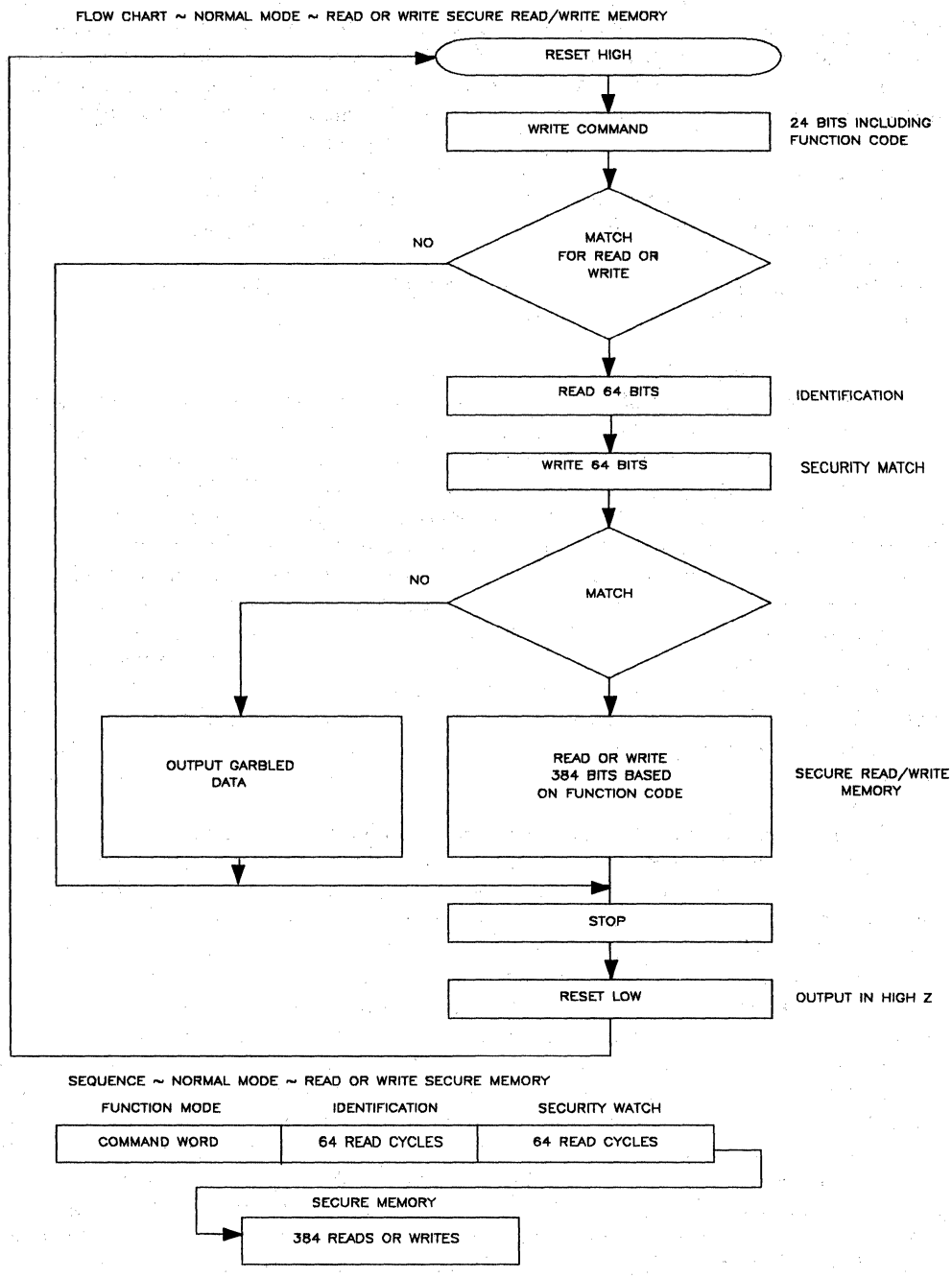

FLOW CHART ~ NORMAL MODE ~ READ OR WRITE SECURE READ/WRITE MEMORY
RESET HIGH
WRITE COMMAND
24 BITS INCLUDING FUNCTION CODE
NO
MATCH FOR READ OR WRITE
READ 64 BITS
IDENTIFICATION
WRITE 64 BITS
SECURITY MATCH
NO
MATCH
OUTPUT GARBLED DATA
READ OR WRITE 384 BITS BASED ON FUNCTION CODE
SECURE READ/WRITE MEMORY
STOP
RESET LOW
OUTPUT IN HIGH Z
SEQUENCE ~ NORMAL MODE ~ READ OR WRITE SECURE MEMORY
FUNCTION MODE
IDENTIFICATION
SECURITY WATCH
COMMAND WORD
64 READ CYCLES
64 READ CYCLES
SECURE MEMORY
384 READS OR WRITES

FIGURE 3

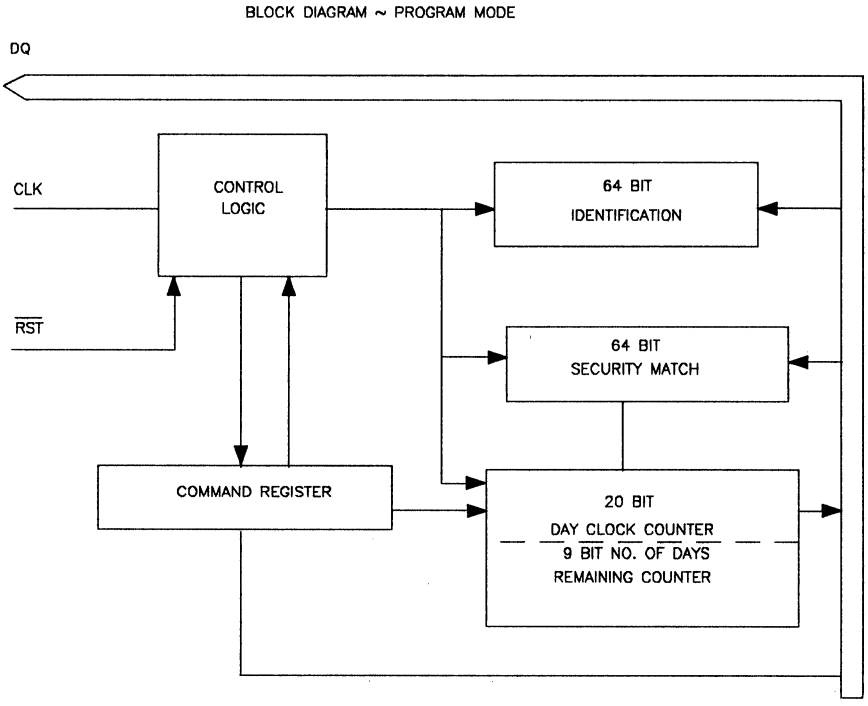
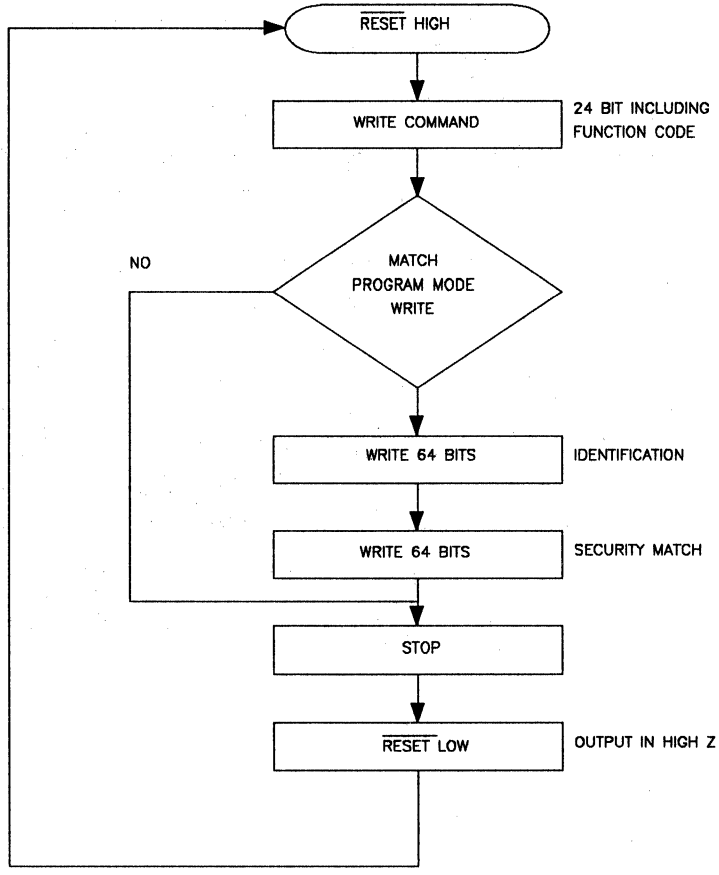

BLOCK DIAGRAM ~ PROGRAM MODE
DQ
CLK
CONTROL LOGIC
64 BIT IDENTIFICATION
RST
64 BIT SECURITY MATCH
COMMAND REGISTER
20 BIT DAY CLOCK COUNTER
9 BIT NO. OF DAYS REMAINING COUNTER

FIGURE 4

PROGRAM MODE ~ PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY

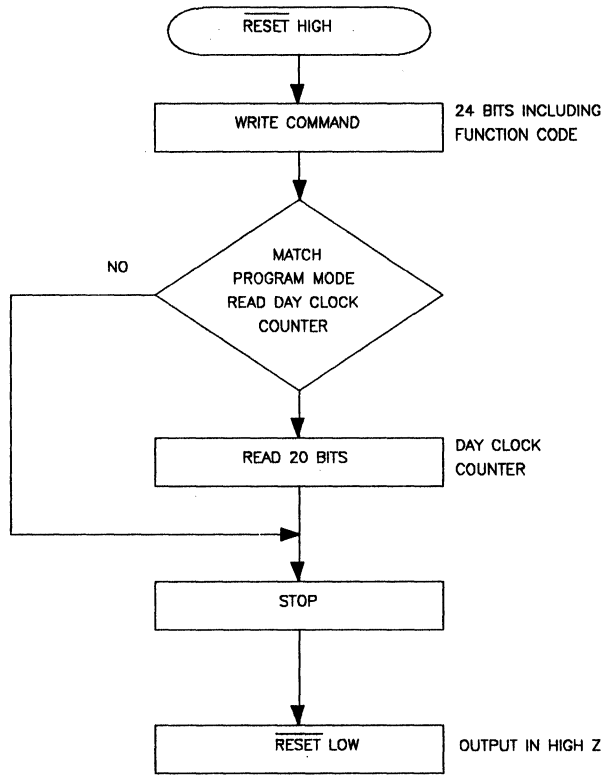


SEQUENCE–PROGRAM MODE–PROGRAM IDENTIFICATION AND SECURITY MATCH BITS

FUNCTION MODE	IDENTIFICATION	SECURITY WATCH
COMMAND WORD	64 WRITE CYCLES	64 WRITE CYCLES

FIGURE 5

FLOW CHART – PROGRAM MODE ~ READING THE 20 BIT DAY CLOCK COUNTER



SEQUENCE – PROGRAM MODE – READING THE 20 BIT DAY CLOCK COUNTER

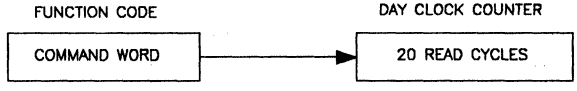
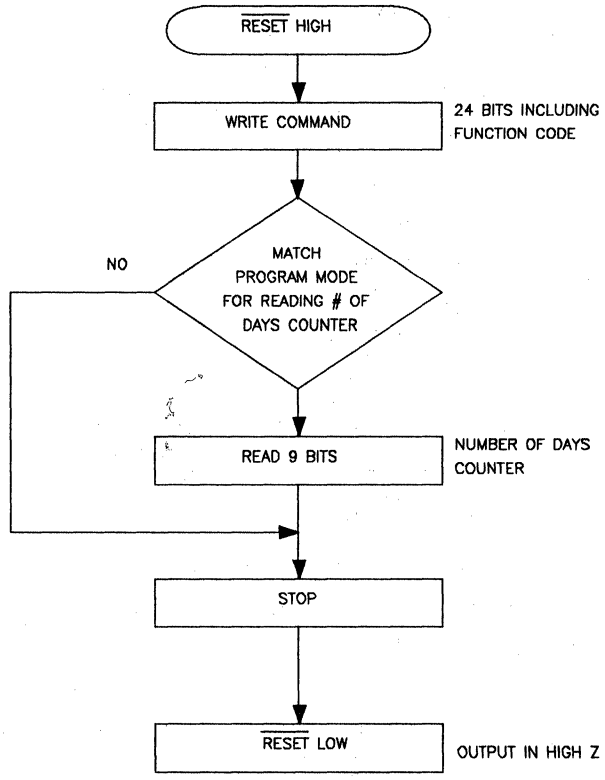


FIGURE 6

FLOW CHART – PROGRAM ~ READING THE 9 BIT NUMBER OF DAYS COUNTER



SEQUENCE – PROGRAM MODE – READING THE 9 BIT NUMBER OF DAYS COUNTER

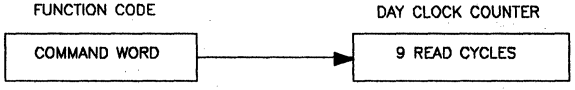
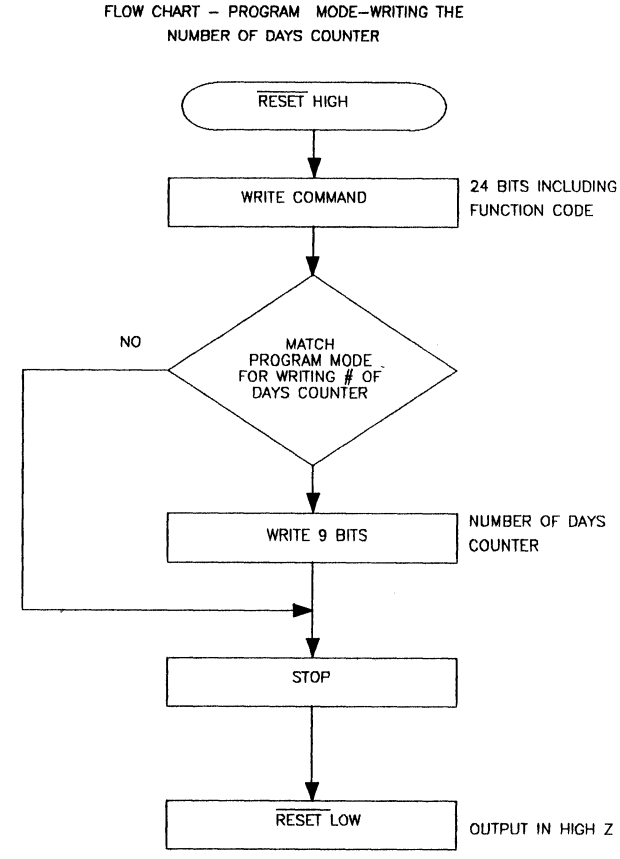


FIGURE 7


FLOW CHART – PROGRAM MODE–WRITING THE NUMBER OF DAYS COUNTER
RESET HIGH
WRITE COMMAND
24 BITS INCLUDING FUNCTION CODE
NO
MATCH PROGRAM MODE FOR WRITING # OF DAYS COUNTER
WRITE 9 BITS
NUMBER OF DAYS COUNTER
STOP
RESET LOW
OUTPUT IN HIGH Z

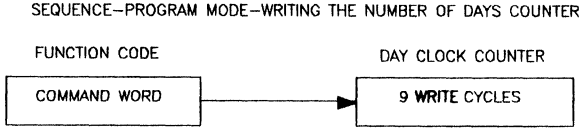
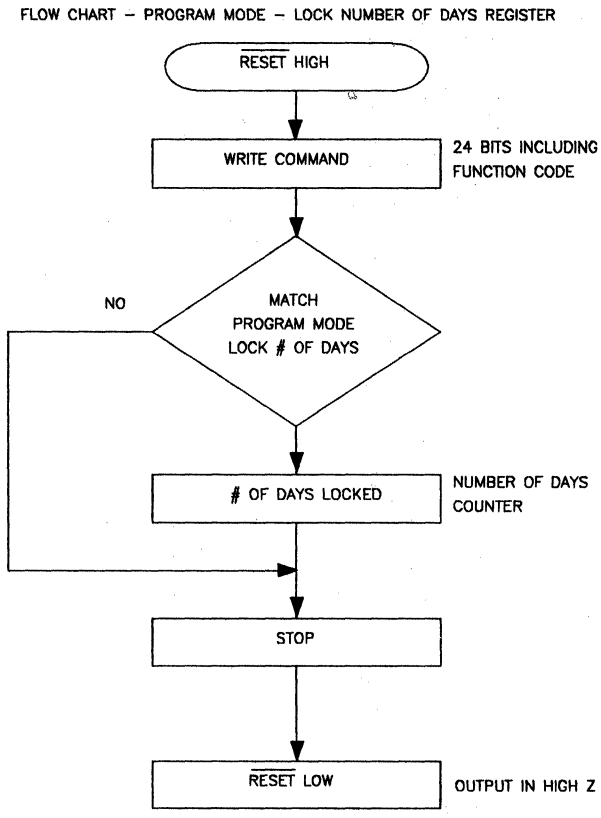

SEQUENCE–PROGRAM MODE–WRITING THE NUMBER OF DAYS COUNTER
FUNCTION CODE
DAY CLOCK COUNTER
COMMAND WORD
9 WRITE CYCLES

FIGURE 8


FLOW CHART – PROGRAM MODE – LOCK NUMBER OF DAYS REGISTER
RESET HIGH
WRITE COMMAND
24 BITS INCLUDING FUNCTION CODE
NO
MATCH PROGRAM MODE LOCK # OF DAYS
OF DAYS LOCKED
NUMBER OF DAYS COUNTER
STOP
RESET LOW
OUTPUT IN HIGH Z

to issuing a lock command. After the lock command is issued, stop oscillator commands are ignored.

A sequence for properly setting the expiration time of the DS1207 is as follows (see Figure 11): First program the identification and security match bits to the desired value. Also use normal mode operation to write the appropriate secure data. Second, write the number of days remaining register to the desired value. This number can be immediately verified by reading the number of days remaining. Next, arm the oscillator by writing the appropriate command. Then do a normal mode read. This action will start the internal oscillator. Now read the 20 bit day clock counter several times to verify that the oscillator is running. After oscillator activity has been verified, issue the stop oscillator command. Now the lock command should be issued followed by the arm oscillator command. The TimeKey will start to count down to expiration on the next access. The oscillator verification portion of this sequence is not required and can be deleted when speed in setting time remaining is important.

FIGURE 9

FLOW CHART – PROGRAM MODE–ARM OSCILLATOR

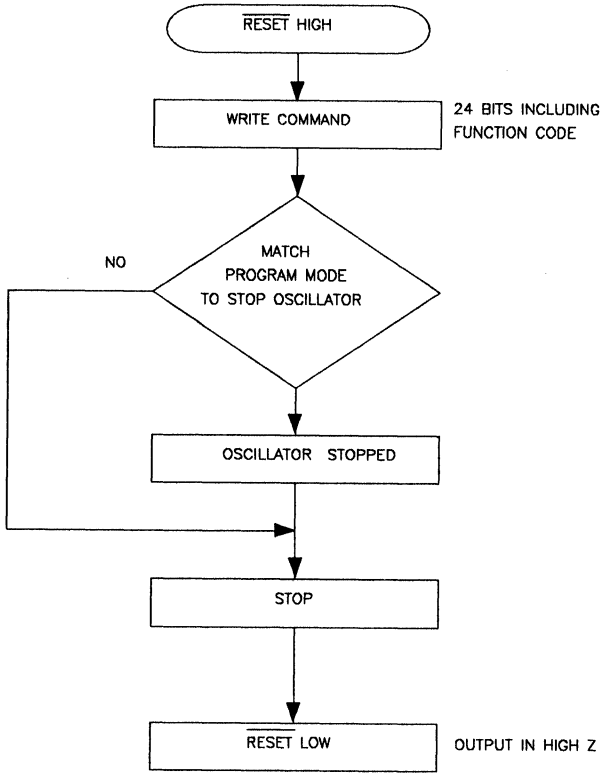


FIGURE 10

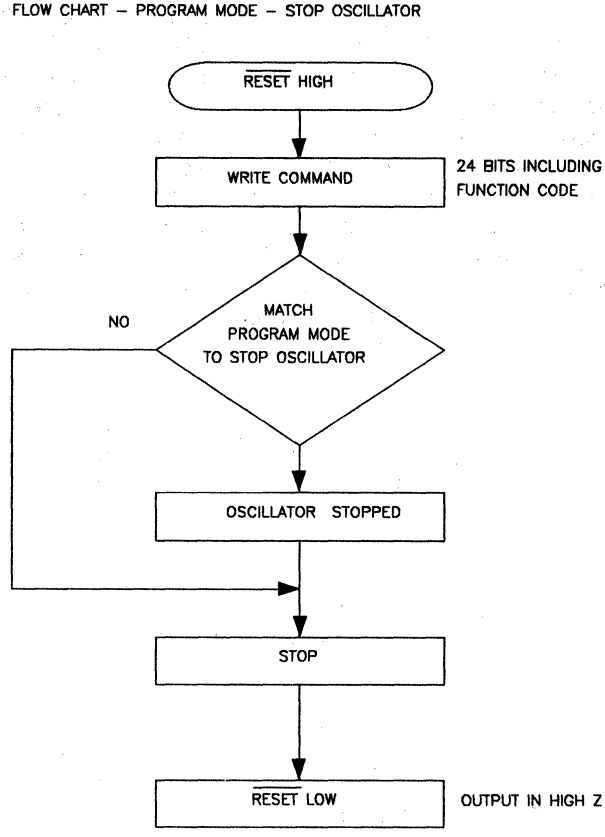

FLOW CHART – PROGRAM MODE – STOP OSCILLATOR
RESET HIGH
WRITE COMMAND
24 BITS INCLUDING
FUNCTION CODE
NO
MATCH
PROGRAM MODE
TO STOP OSCILLATOR
OSCILLATOR STOPPED
STOP
RESET LOW
OUTPUT IN HIGH Z

FIGURE 11
SETTING THE TIME UNTIL EXPIRATION OF THE DS1207

Step 1	Program identification memory Program security match bits Write normal mode secure data
Step 2	Program write the number of days remaining Program read the number of days remaining for verification
Step 3	Issue arm oscillator command
Step 4	Do a read of any kind
Step 5	Program read the day clock counter several times (verify that the oscillator is running)
Step 6	Issue the stop oscillator command
Step 7	Issue the lock command
Step 8	Issue arm oscillator command (time of expiration will start on first access)

Note: Step 3 through Step 6 are not required. Dallas Semiconductor tests and guarantees that the oscillator will start without verification

COMMAND WORD

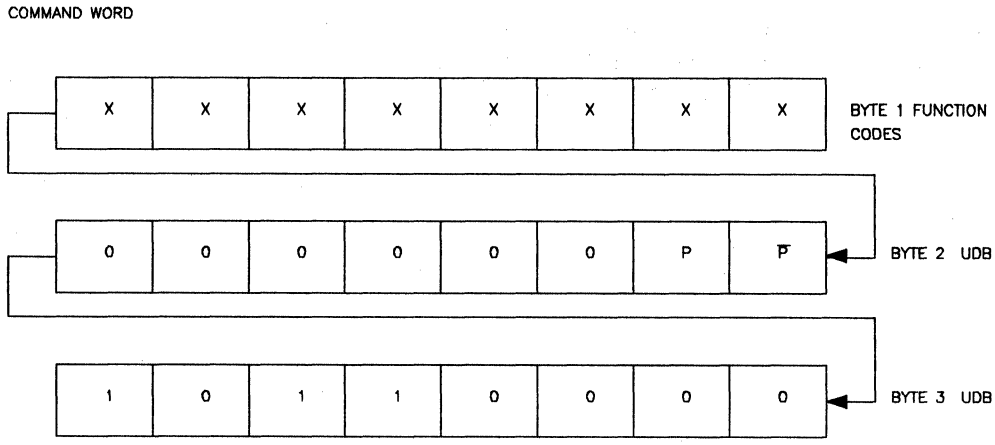
Each data transfer for normal and program mode begins with a three byte command word as shown in Figure 12. As defined, the first byte of the command word specifies the function code. There are eight function codes which are acceptable (Figure 13). If any one of the bits of the first byte of the command word fails to meet one of the exact patterns for function codes, the data transfer will be aborted.

The first two bits of the second byte of the command word specify whether the data transfer to follow is program or normal mode. The bit pattern for program mode is 0 in bit 0 and 1 in bit 1. The bit pattern for normal mode is a 1 in bit 0 and a 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause transfer to abort. The program mode can be invoked with one of seven function codes; program identification and security match, read the 20 bit day clock counter, read the number of days count, write the number of days count, lock number of days count, arm oscillator, and stop oscillator.

The remaining 6 bits of byte 2 and the first 4 bits of byte 3 must be written to logic 0 or data transfer will abort. Under special contract with Dallas Semiconductor, these bits may be defined by the user as any bit pattern other than that specified by Dallas Semiconductor as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last four bits of byte 3 of the command word must be written 1011 or data transfer will abort. Table 1 is a summary of the command words in hexidecimal as they apply to all function codes for both program mode and normal mode.

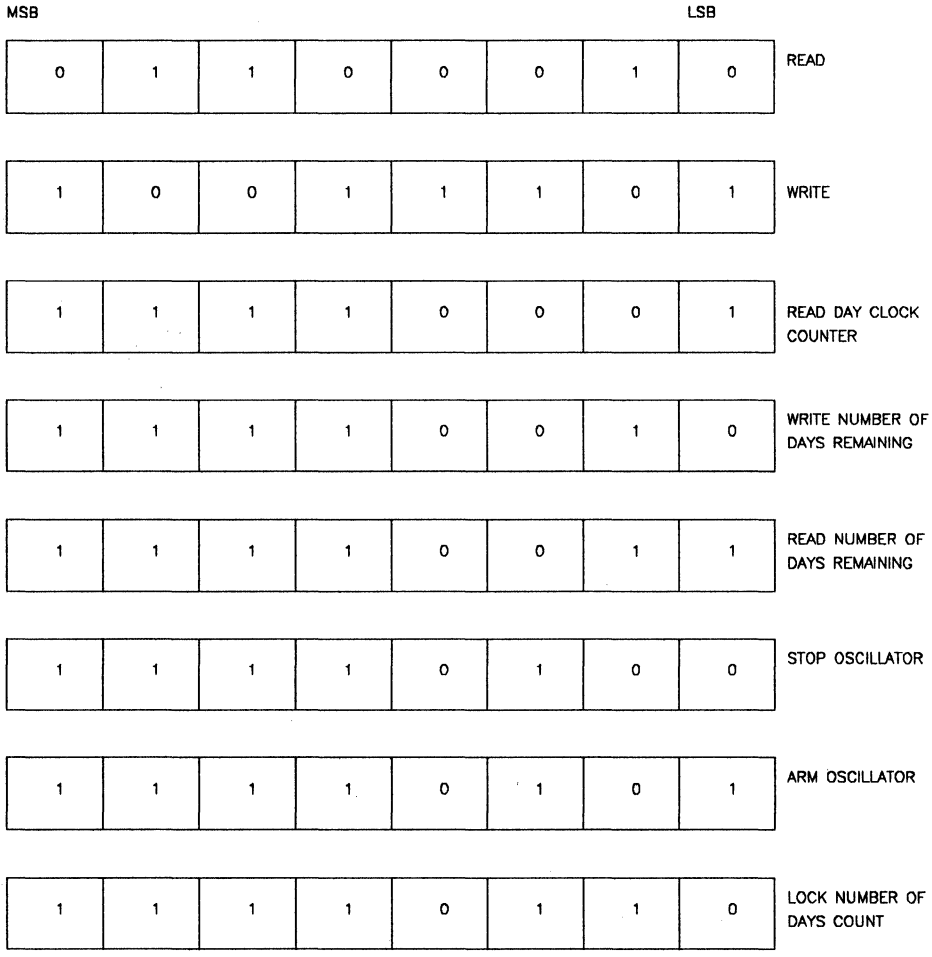
Note: Contact Dallas Semiconductor Sales Office for special command word code assignment which makes possible an exclusive blank TimeKey.

FIGURE 12



USER DEFINABLE BITS (UDB) ~ CONTACT DALLAS SEMICONDUCTOR FOR SPECIAL COMMAND WORD CODE ASSIGNMENT WHICH MAKES AN EXCLUSIVE BLANK KEY.

FIGURE 13: FUNCTION CODES - FIRST BYTE OF COMMAND WORD



RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The reset input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2 MA @ 3.0 volts is required. Third, the $\overline{RST}$ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates if the $\overline{RST}$ pin is low and the DQ pin goes to a high impedance state. Data transfer is illustrated in Figure 14 for normal mode and Figure 15 for program mode.

TIMEKEY CONNECTIONS

The TimeKey is designed to be plugged into a standard 5 pin 0.1 inch center SIP receptacle. A guide is provided to prevent the TimeKey from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the TimeKey pins can be determined to insure connection integrity before data transfer begins. CLK, $\overline{RST}$, and Data Input/Output all have 20K OHM pull down resistors to ground which can be sensed by a reading device.

TABLE 1 IS A SUMMARY OF THE COMMAND WORDS IN HEXIDECIMAL AS THEY APPLY TO ALL FUNCTION CODES FOR BOTH PROGRAM MODE AND NORMAL MODE

TABLE 1

MODE	FUNCTION	COMMAND WORD		
NORMAL	READ	B0	01	62
NORMAL	WRITE	B0	01	9D
PROGRAM	WRITE	B0	02	9D
PROGRAM	READ DAY CLOCK COUNTER	B0	02	F1
PROGRAM	READ DAYS REMAINING	B0	02	F3
PROGRAM	WRITE DAYS REMAINING	B0	02	F2
PROGRAM	ARM OSCILLATOR	B0	02	F5
PROGRAM	LOCK NUMBER OF DAYS COUNT	B0	02	F6
PROGRAM	STOP OSCILLATOR	B0	02	F4

FIGURE 14

DATA TRANSFER – NORMAL MODE READ OR WRITE SECURE READ/WRITE MEMORY

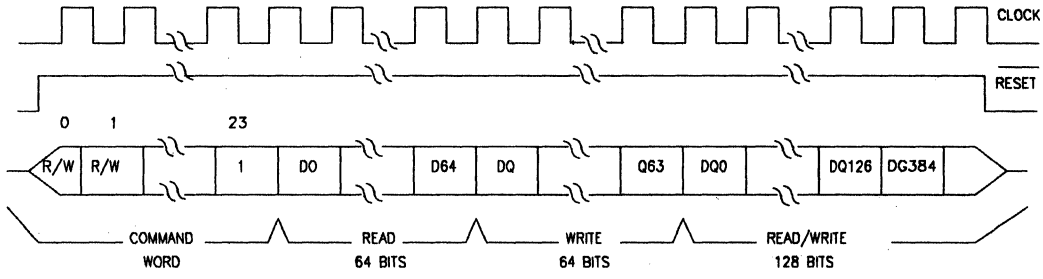
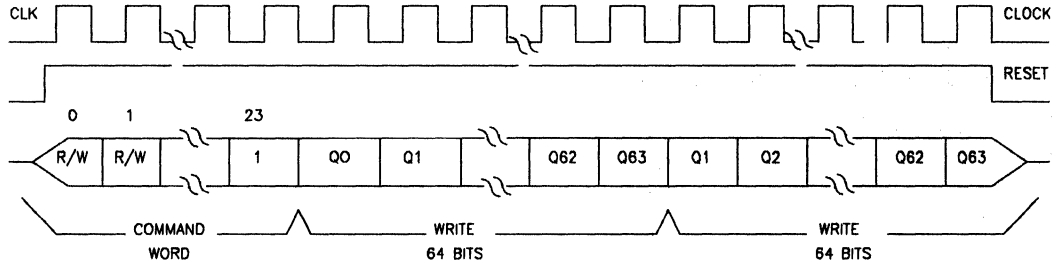
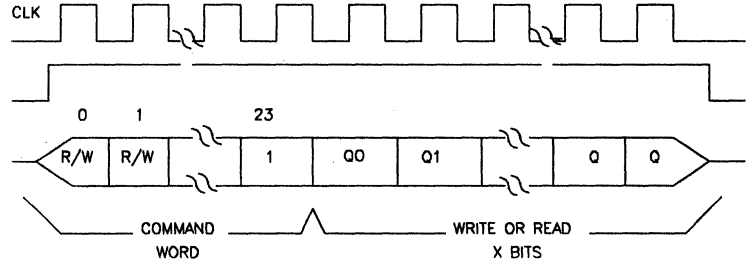


FIGURE 15

DAT TRANSFER – PROGRAM MODE ~ PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY



DATA TRANSFER – PROGRAM MODE



NOTE: THE NUMBER OF BITS WHICH FOLLOW THE COMMAND WORD WILL BE EITHER 0, 9, OR 20 BITS BASED ON THE FUNCTION CODE.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	--1.0V to +7V
OPERATING TEMPERATURE	0°C to 70°
STORAGE TEMPERATURE	- -40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0 °C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
$\overline{\text{RESET}}$ Logic 1	V_{IHE}	3.0			V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $\overline{\text{RST}}$= 3.0V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	N OTES
Input Leakage	I_{IL}			+500	uA	4
Output Leakage	I_{LO}			+500	uA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
$\overline{\text{RST}}$ Input Resistance	Z_{RST}	10		40	KΩ	
D/Q Input Resistance	Z_{DQ}	10		40	KΩ	
CLK Input Resistance	Z_{CLK}	10		40	KΩ	
$\overline{\text{RST}}$ Current 3.0V	I_{RST}			2	mA	6,9

CAPACITANCE

(tA = 25°)

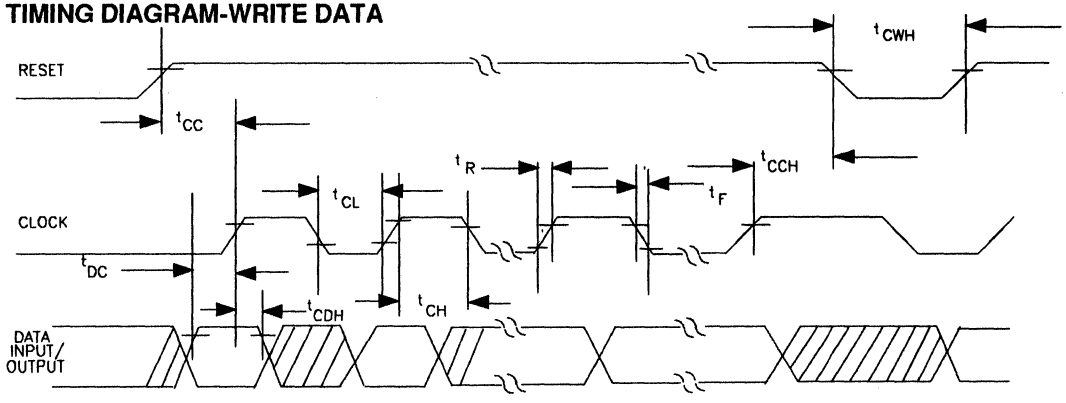
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance CIN	C_N	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS

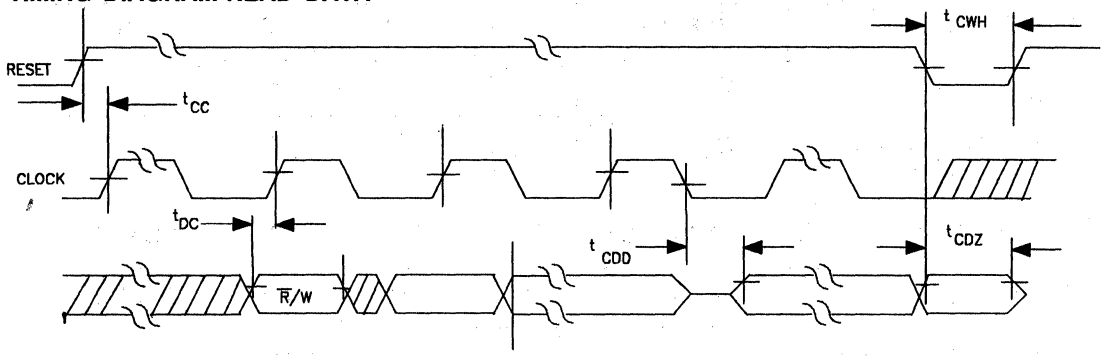
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	50			ns	2,7
CLK to Data Hold	t_{CDH}	70			ns	2,7
CLK to Data Delay	t_{CDD}			200	ns	2,3,5,7
CLK low Time	t_{CL}	250			ns	2,7
CLK High Time	t_{CH}	250			ns	2,7
CLK Frequency	f_{CLK}	D.C.		2.0	MHZ	2,7
CLK Rise & Fall	t_R, t_F			500	ns	2,7
$\overline{RST}$ To CLK Set Up	t_{CC}	1			us	2,7
CLK To $\overline{RST}$ Hold	t_{CCH}	60			ns	2,7
$\overline{RST}$ Inactive Time	t_{CWH}	10			ms	2,7
$\overline{RST}$ To I/O High Z	t_{CDZ}			70	ns	2,7

TIMING DIAGRAM-WRITE DATA



TIMING DIAGRAM-READ DATA



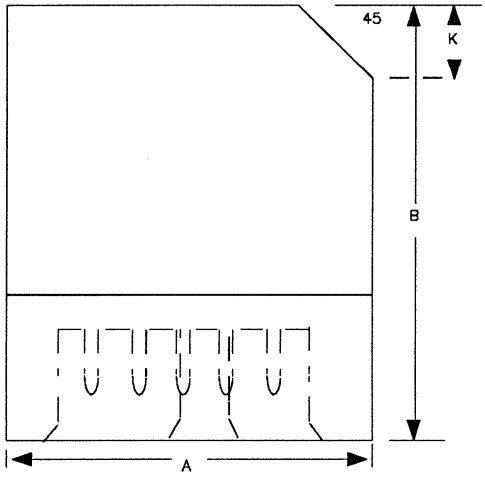
1. All voltages are referenced to GND.
2. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.
3. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
4. For CLK, D/Q, and $\overline{RST}$
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at V_{IH} of $\overline{RST}$ greater than or equal to 3.0V.
8. Each DS1207 is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
9. Average A.C. $\overline{RST}$ current can be determined using the following formula:

$$I_{TOTAL} = 2 + I_{LOAD}\ D.C. + (4 \times 10^{-3})(C_L + 280)f$$

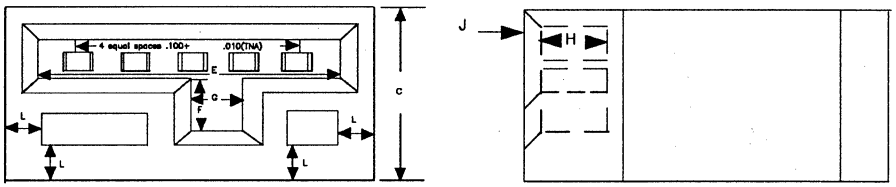
I_{TOTAL} and I_{LOAD} are in mA; CL is in pF; f is in MHZ.

Applying the above formula, a load capacitance of 50 pF running at a frequency of 2.0 MHZ gives an I_{TOTAL} of 1.6 MA.

DS1207
TIMEKEY



DIM.	INCHES	
	MIN.	MAX.
A	.610	.630
B	.740	.760
C	.310	.330
D	.100	.110
E	.515	.525
F	.100	.110
G	.100	.110
H	.110	.130
I	.030	.050
K	.045	..055
J	.045	..055



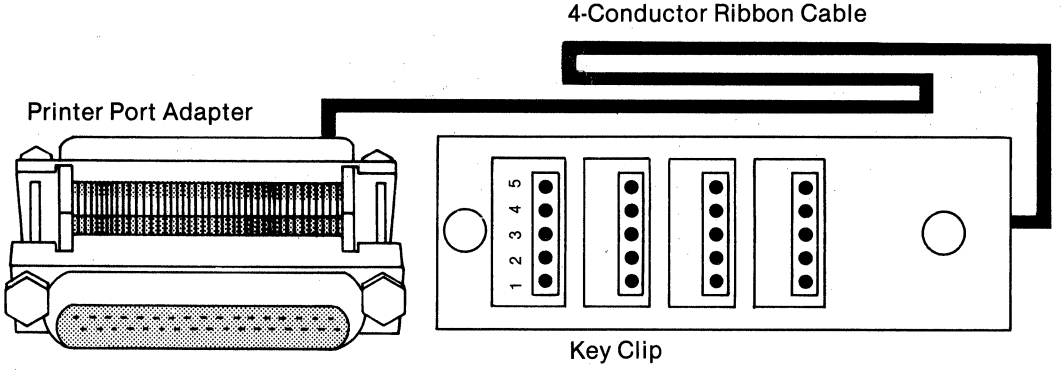
Dallas Semiconductor
Printer Port KeyRing — *DS1253*

FEATURES

- Low cost add on fixture for Electronic Keys, Tags, and TimeKeys
- Connects directly to IBM PC Parallel Printer Port without affecting printer operation
- Plug-in installation
- Key, Tag, and TimeKey communications are totally controlled by software
- Up to four Keys, Tags, and TimeKeys may be resident at one time
- Normal computer operation is unaffected
- Applications include software security, identification, personalization, and portable memory

PIN CONNECTIONS AND DEFINITIONS

Pin 1 - V_{CC} +5 Volts
Pin 2 - $\overline{RST}$ - $\overline{RESET}$
Pin 3 - D/Q - Data In/Out
Pin 4 - CLK - CLOCK
Pin 5 - GND Ground



DESCRIPTION

The DS1253 KeyRing adapts low pin count electronic Keys (DS1204U), Tags (DS1201S), and TimeKeys (DS1207) to the IBM PC Parallel Printer Port without affecting the printer or computer operations. The KeyRing is installed onto any IBM PC or IBM PC-compatible printer by simply disconnecting the printer, installing the printer port adapter, and reconnecting the printer to back connector on the printer port adapter. The emanating 4-conductor ribbon cable can be routed such that the key clip can be attached to the computer cabinet in a convenient location with the adhesive provided. Up to 4 keys and/or tags can be inserted into the key clip at the same time. Communications with keys and tags occur under software control of the parallel printer port. The three control signals ($\overline{RESET}$, Clock, and Data In/Out) for Tags, Keys and TimeKeys are generated by consecutive I/O instructions which control the parallel printer port.

OPERATION

Keys, Tags, and TimeKeys have defined signal patterns which are required for communications. The signals $\overline{RST}$, CLK and DQ must be software controlled to duplicate the behavior as defined in the respective data sheet for Tags, Keys and TimeKeys. Each signal is a function of a specific output or I/O line of the printer port. Pin 4 on the 25-Pin D Connector Parallel Printer Port is called Data Out 2 (D2). This signal is used to provide $\overline{RST}$ for the KeyRing and must be kept at a high level when communicating with Tags, Keys, and TimeKeys. When $\overline{RST}$ is driven low all communication to Tags, Keys, and TimeKeys is terminated. The $\overline{RST}$ signal is also used as a source of power for Tags, Keys and TimeKeys (see respective data sheets). Pin 5 on the 25-Pin D Connector Parallel Printer Port is called Data Out 3 (D3). This signal is used to provide CLK for the KeyRing. The CLK signal times data into and out of Keys, Tags, and TimeKeys. Because the CLK signal provides timing, the relationship between both level and transition from one level to another is critical with respect to data. In fact, data must be valid when a CLK transition occurs which inputs data to Keys, Tags, and TimeKeys and a CLK transition is also required to output data. Because signals change state at the same time on the Parallel Printer Port, set up and hold times do not normally exist. To compensate, two output cycles are required for each transition of the CLK signal. The first cycle is used to establish the correct CLK level. A second cycle will then guarantee that data is valid as the clock changes levels. Pin 17 on the 25-Pin D Connector Parallel Printer Port is called SLCTIN and is used as the data I/O signal for Keys, Tags, and TimeKeys. This is a bi-directional signal. Data is output from this port signal during write cycles, and input from Keys, Tags, and TimeKeys during read cycles. Pin 18 on the 25-Pin D Connector is ground (GND) and supplies ground for the KeyRing.

When communicating with Keys, Tags and TimeKeys, the Parallel Printer Port is being used as a general purpose I/O port. As such, software defines the appropriate commands. In order to avoid having the printer interpret Key, Tag, and TimeKey communications as print commands, the strobe signal (Pin 1 on the D Connector Parallel Printer Port) must be kept low when the data stream is not directed to the printer. The printer must also be kept on when using the KeyRing to avoid clamping the Parallel Printer Port signals.

INSTALLATION

The Parallel Printer Port KeyRing is installed by first removing the printer cable. If the Parallel Printer Port is not used, this step is not necessary. The Parallel Printer Port cable is removed by loosening the top and bottom mounting screws and unplugging the cable. The next step is to install the printer port adapter by loosening the top and bottom mounting screws on the adaptor and plugging the male side of the adapter into the female printer port. The top and bottom screws should then be tightened to avoid accidental disconnection. Next, plug the printer cable into the female end of the printer port adapter. The top and bottom mounting screws of the printer cable should then be tightened to avoid accidental disconnection. After the printer port adapter has been secured, the key clip can be attached to a convenient spot on the computer cabinet with the supplied adhesive.

SOFTWARE

Upon request Dallas Semiconductor can make available demonstration software with source listing for the IBM PC or IBM PC-compatible computers.

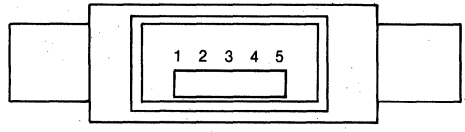
Dallas Semiconductor
Printer Port KeyRing — *DS1255*

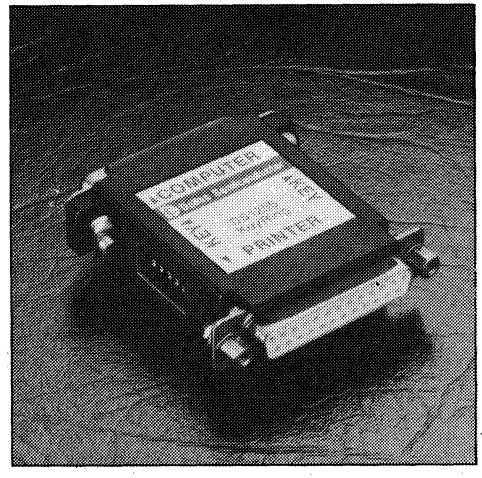
FEATURES

- Self-contained add-on fixture for user insertable Electronic Keys, Tags and TimeKeys
- Connects to the parallel printer port of an IBM XT, AT, RT or compatible computer
- End user installation
- Two Keys may be resident at one time
- Key, Tag and TimeKey communications are totally controlled by software
- Normal computer/printer operation is unaffected
- Applications include software authorization, computer site identification, and access control

PIN CONNECTIONS AND DEFINITIONS

Pin 1 - V_{CC} - +5 Volts
Pin 2 - $\overline{RST}$ - $\overline{RESET}$
Pin 3 - D/Q Data In/Out
Pin 4 - CLK - CLOCK
Pin 5 - GND - GROUND





DESCRIPTION

The DS1255 KeyRing adapts low pin Electronic Keys DS1204U, Tags DS1201S, and TimeKeys DS1207 to the IBM PC parallel printer port without affecting the printer or computer operations. The KeyRing is installed onto any IBM PC or IBM PC-compatible printer by simply disconnecting the printer, installing the KeyRing, and reconnecting the printer to the back connector on the KeyRing. Two Keys or Tags can be resident at the same time. Communication with Keys is established by software controlled sequences to the parallel printer port. The three control signals ($\overline{Reset}$, Clock and Data In/Out) for Keys are generated by the parallel port signals by executing an assembly or DOS level I/O driver.

OPERATION

Keys, Tags and TimeKeys have defined signal patterns which are required for communications. The signals $\overline{RST}$, CLK, and DQ must be software controlled to duplicate the behavior as defined in the respective data sheet for Keys. Each signal is a function of a specific output or I/O line of the printer port (Figure 1). Pin 4 on the 25-pin D Connector parallel printer port is called Data Out 2 (D2). This signal is used to provide $\overline{RST}$ for the KeyRing and must be kept at high level when communicating with Keys. When $\overline{RST}$ is driven low, all communication to Keys is terminated. The $\overline{RST}$ signal is also used as a source of power for Keys (see respective data sheets). Pin 5 on the 25-pin D Connector parallel printer port is called Data Out 3 (D3). This signal is used to provide CLK for the KeyRing. The CLK signal times data into and out of Keys. Because the CLK signal provides timing, the relationship between both level and transition is critical with respect to data. In fact, data must be valid when a CLK transition occurs which inputs data to Keys and a CLK transition is also required to output data. Because signals change state at the same time on the parallel printer port, setup and hold times do not normally exist. To compensate, two output cycles are required for each transition of the CLK signal. The first cycle is used to establish the correct CLK level. A second cycle will guarantee that data is valid as the CLK changes levels. Pin 17 on the 25-pin D Connector parallel printer port is called SLCTIN and is used as the data I/O signal for Keys. This is a bi-directional signal. Data is output from this port signal during write cycles and input from Keys during read cycles. Pin 18 on the 25-pin D Connector is ground (GND) and supplies ground for the KeyRing.

When communicating with Keys, the parallel printer port is being used as a general purpose I/O port. As such, software defines the appropriate commands. In order to avoid having the printer interpret Key communications as print commands, the strobe signal (Pin 1 on the D Connector parallel printer port) must be kept low when the data stream is not directed to the printer. The printer must also be kept on when using the KeyRing to avoid clamping the parallel printer port signals.

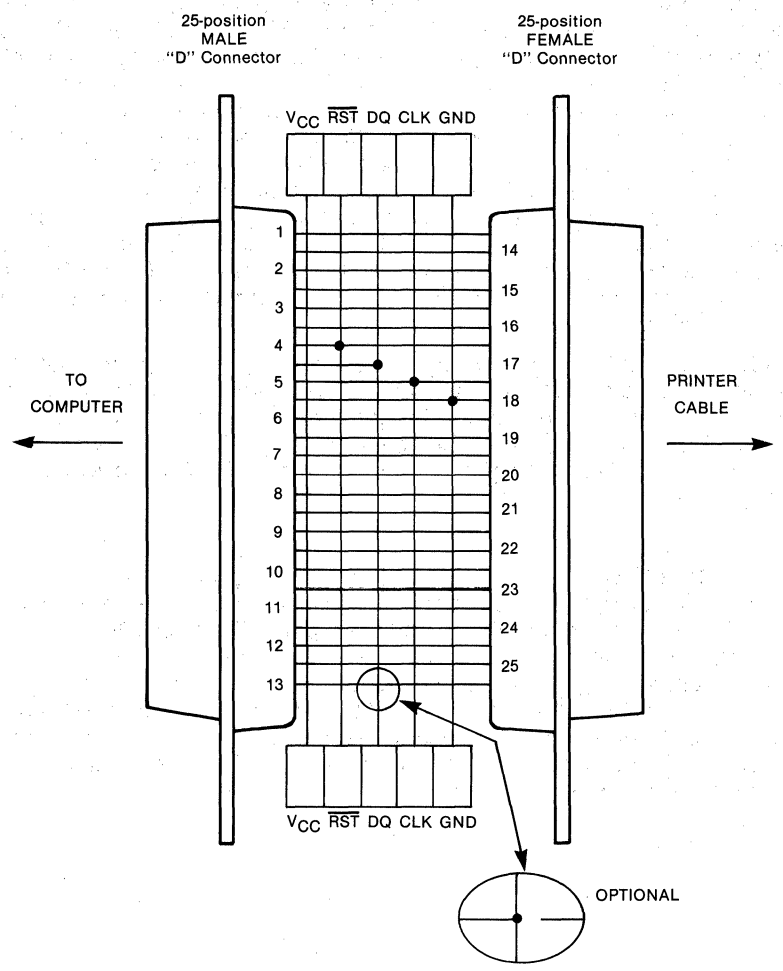
INSTALLATION

The Parallel Printer Port KeyRing is installed by first removing the printer cable. If the parallel printer port is not being used, this step is not necessary. The printer cable is removed by loosening the top and bottom retaining screws and unplugging the cable. The next step is to install the KeyRing by plugging the male side of the KeyRing into the female printer port. The top and bottom retaining screws should be tightened to avoid accidental disconnection. Next, plug the printer cable into the female end of the KeyRing. The top and bottom retaining screws should then be tightened to avoid accidental disconnection. After the printer cable is secure, a Key,Tag,or TimeKey can be plugged into either of two receptacles and the computer and KeyRing are now ready for use.

SOFTWARE

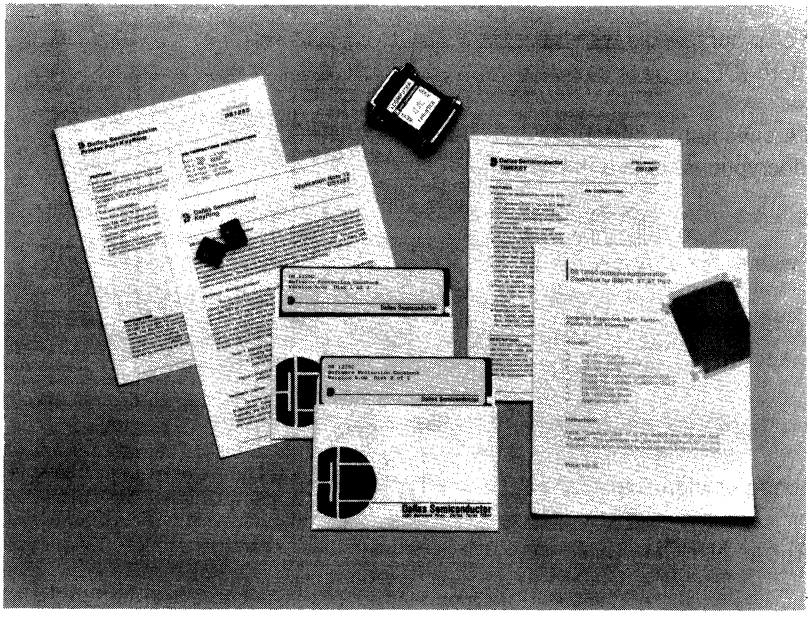
Upon request, Dallas Semiconductor can make available demonstration software with source listing for assemble language and high level language for the IBM PC, XT, AT or compatible computers.

Figure 1



NOTE: An optional feature is available from Dallas Semiconductor which connects Pins 13 and 17 together. This feature allows operation with some nonstandard IBM P.C. Printer Ports. See Application Note 12.

Dallas Semiconductor
Software Authorization Cookbook **DS1255C**



FEATURES

- DS1207 TimeKey
- DS1204U Electronic Key
- DS1255 KeyRing
- Floppy Disk Labeled "Cookbook Disk 1"
- Floppy Disk Labeled "Cookbook Disk 2"
- DS1207 Data Sheet
- DS1255 Data Sheet
- Application Note 12

INSTRUCTION

Install "Cookbook Disk 1" in the default drive and type "RUN ME". This command will give you instructions for printing document files which should be read carefully before proceeding.

LANGUAGES SUPPORTED: BASIC, FORTRAN, PASCAL, C, ASSEMBLY

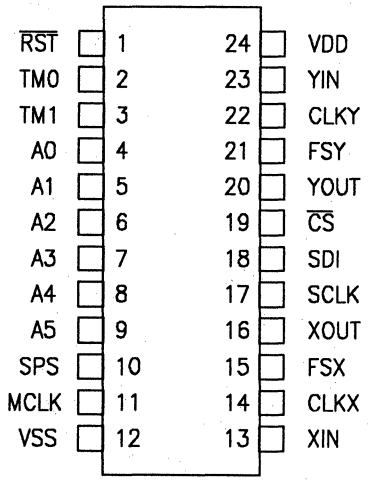
Dallas Semiconductor
DES PROCESSOR

PRODUCT PREVIEW
DS2160
Available Spring 1989

FEATURES

- Voice/data encryption chip compatible with the Data Encryption Standard (DES)
- Dual 64Kbps channel architecture - performs two encryptions, two decryptions, or in a full duplex fashion
- Interconnects directly with u-law or A-law combo-codec devices
- Supports three I/O data formats:
  - 8 bit per 8 KHz (standard)
  - 7 bit per 8 KHz (robbed bit signaling)
  - 4 bit per 8 KHz (32Kbps ADPCM)
- Serial PCM and control port interfaces minimize "glue" logic in multiple channel applications:
  - On-chip channel counters identify input and output time slots in TDM based systems
  - Unique addressing scheme simplifies device control; 3-wire port shared among up to 64 devices
- "Hardware" mode requires no host processor
- Available in 24-pin DIP and 28-pin PLCC

PIN CONNECTIONS



DESCRIPTION

The DS2160 is a programmable digital signal processing (DSP) CMOS chip with the Data Encryption Standard (DES) algorithm coded in firmware. The chip performs encipher/decipher operations on 64-bit words and uses a 64-bit key to provide security as specified by the DES. This algorithm is used in both governmental and commercial applications where sensitive information is passed through unsecured media.

Integrated Battery Backup

Dallas Semiconductor

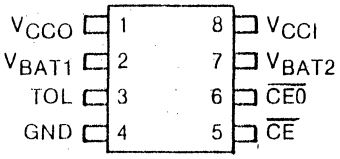
Nonvolatile Controller

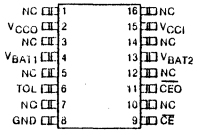
DS1210—8-Pin DIP
DS1210S—16-Pin SOIC

FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin DIP
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Optional 5% or 10% power fail detection
- Low forward voltage drop on the V_{CC} Switch
- Optional 16-pin SOIC surface mount package

PIN CONNECTIONS





PIN NAMES

V_{CCO}	- RAM Supply
V_{BAT1}	- + Battery 1
TOL	- Power Supply Tolerance
GND	- Ground
$\overline{CE}$	- Chip Enable Input
$\overline{CEO}$	- Chip Enable Output
V_{BAT2}	- + Battery 2
V_{CCI}	- + Supply
NC	- No Connect

DESCRIPTION

The DS1210 is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 nonvolatile controller chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

OPERATION

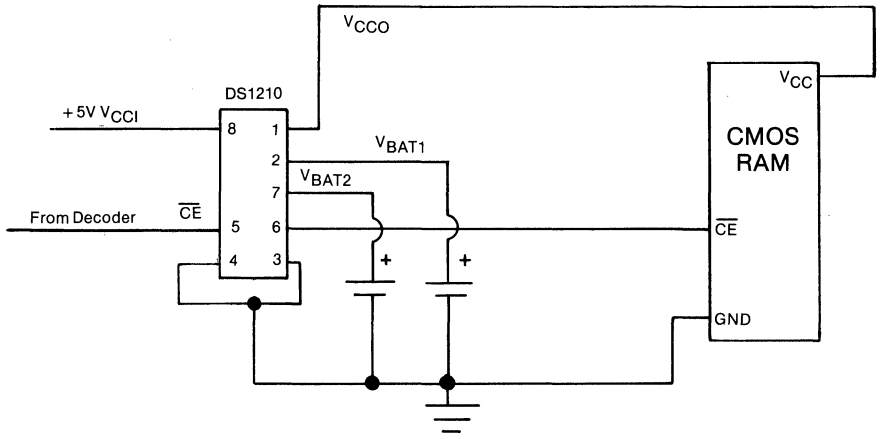
The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.3V. The second function which the nonvolatile controller provides is power fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power fail and inhibits chip enable ($\overline{CEO}$). The third function of write protection is accomplished by holding the $\overline{CEO}$ output signal to within 0.2 volts of the V_{CCI} or battery supply. If $\overline{CE}$ input is low at the time power fail detection occurs, the $\overline{CEO}$ output is kept in its present state until $\overline{CE}$ is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 is connected to V_{CCO}, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CE}$ with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to insure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. In applications where battery reliability is not a concern only one battery need be connected to BAT_1 or BAT_2 pin, with the other battery pin grounded.

NOTE: When batteries are first attached to one or both of the V_{BAT} pins, V_{CCO} will not show the battery potential until V_{CCI} is applied and removed for the first time.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor based system. Section A shows the connections necessary to write protect the RAM when V_{CC} is less than 4.75 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when V_{CC} is less than 4.75 volts and to delay its restart on power up to prevent spurious writes.

FIGURE 1

SECTION A — BATTERY BACKUP

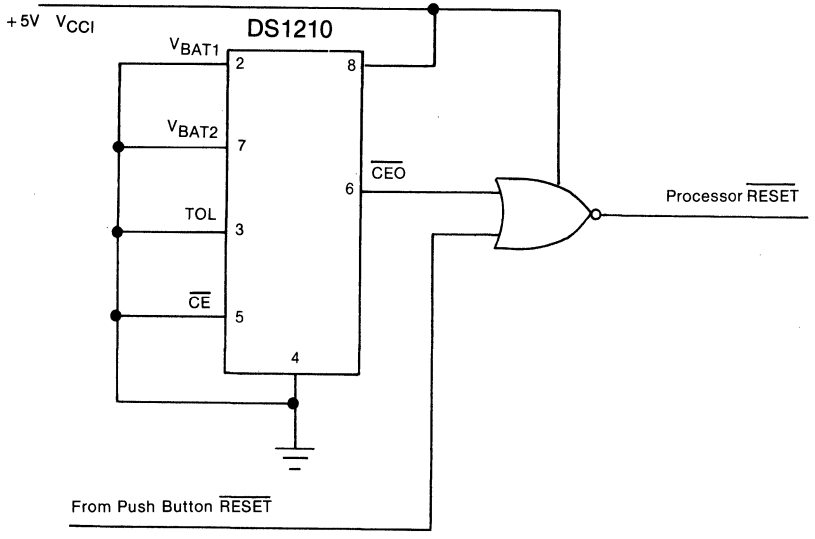


BATTERY BACKUP CURRENT DRAIN EXAMPLE

CONSUMPTION

DS1210 I_{BAT}	- 100 nA
RAM I_{CC02}	- 10 uA
Total Drain	- 10.1*uA*

SECTION B — PROCESSOR RESET



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
PIN 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	−0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1,2

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CCI} = 4.75V to 5.5V, PIN 3 = GND) (V_{CCI} = 4.5 to 5.5V, PIN 3 = V_{CCO})

Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC} − 0.2			V	1
Supply Current	I_{CCO1}			80	mA	4
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Leakage	I_{LO}	−1.0		+1.0	uA	
$\overline{CE0}$ Output @2.4V	I_{OH}	−1.0			mA	5
$\overline{CE0}$ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

(0 °C to 70 °C, $V_{CCI} < V_{BAT}$)

$\overline{CE0}$ Output	V_{OHL}	$V_{BAT} - 0.2$		V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}		100	nA	2,3
Battery Backup Curent @$V_{CCO} = V_{BAT} - 0.3V$	I_{CC02}		50	uA	6,7

CAPACITANCE ($t_A = 25$ °C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS

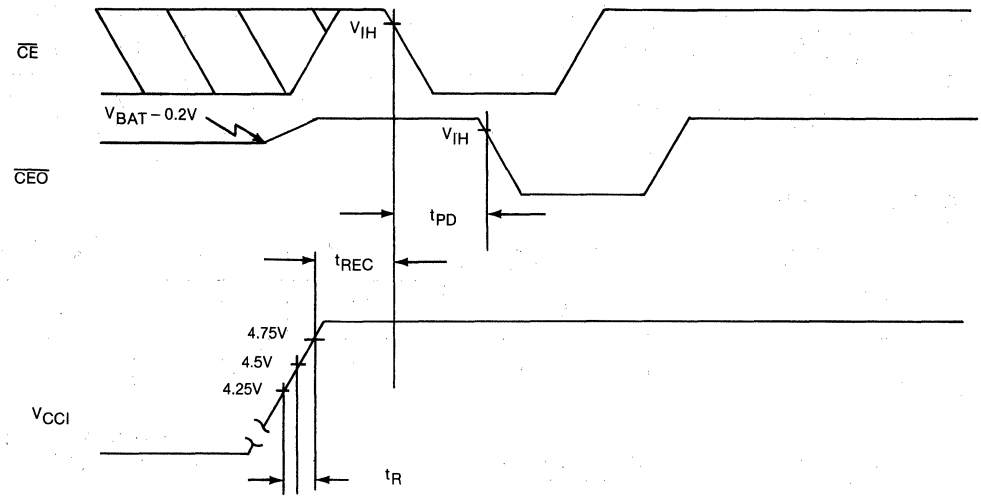
(0 °C - 70 °C, $V_{CCI} = 4.75$ - 5.5V, PIN 3 = GND)
($V_{CCI} = 4.5$ to 5.5V, PIN 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

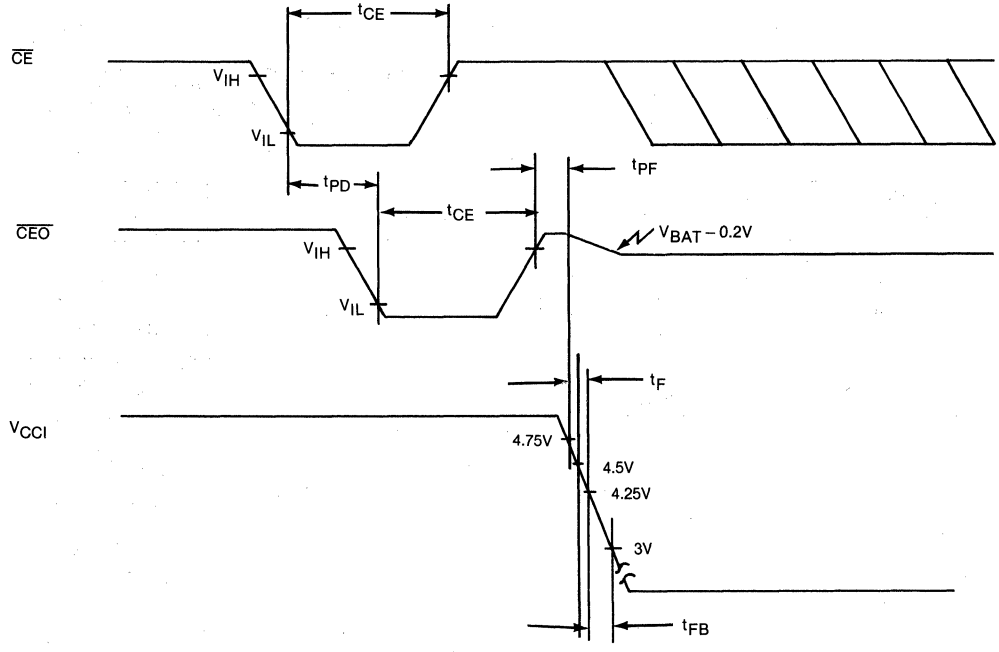
(0 °C to 70 °C, $V_{CCI} < 4.75$V, PIN 3 = GND)
($V_{CCI} < 4.5$V, PIN 3 = V_{CCO})

Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power Down	t_F	300			us	
V_{CC} Slew Rate Power Down	t_{FB}	10			us	
V_{CC} Slew Rate Power Up	t_R	0			us	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	us	7,8

TIMING DIAGRAM — POWER UP

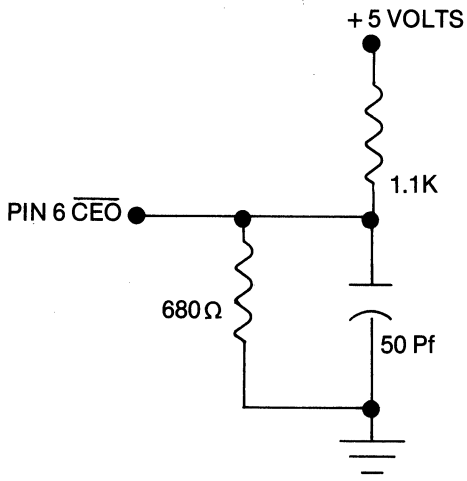


TIMING DIAGRAM — POWER DOWN



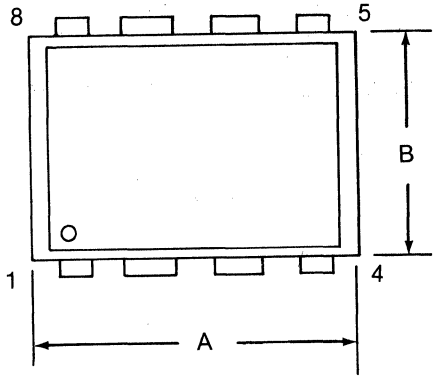
NOTES:

1. All voltages are referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and $\overline{CE0}$ open.
4. I_{CC01} is the maximum average load which the DS1210 can supply to the memories.
5. Measured with a load as shown in Figure 2.
6. I_{CC02} is the maximum average load current which the DS1210 can supply to the memories in the battery backup mode.
7. t_{CE} max must be met to insure data integrity on power loss.
8. Chip Enable Output $\overline{CEO}$ can only sustain leakage current in the battery backup mode.

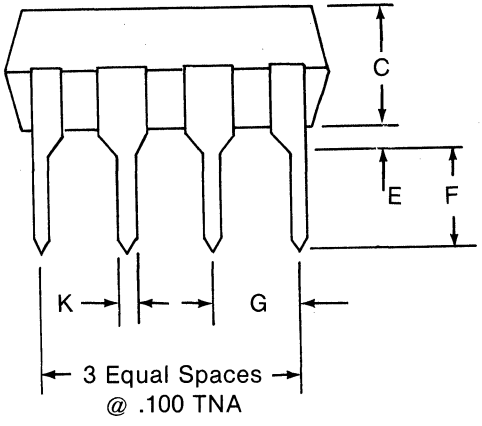


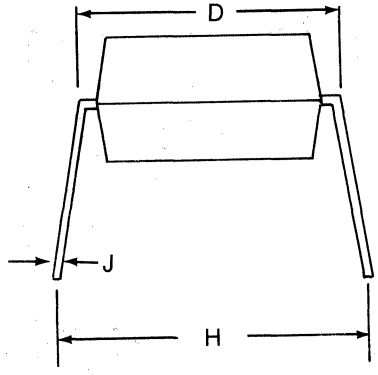
OUTPUT LOAD
Figure 2

DS1210
Nonvolatile Controller

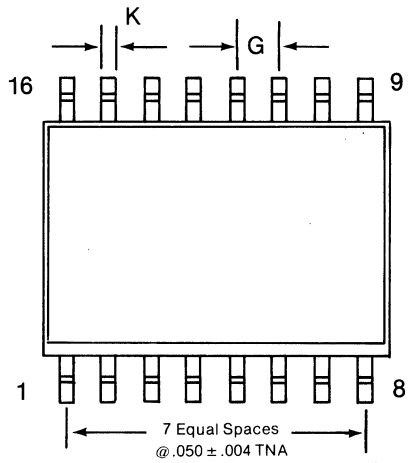


DIM.	INCHES	
	MIN.	MAX.
A	.345	.400
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

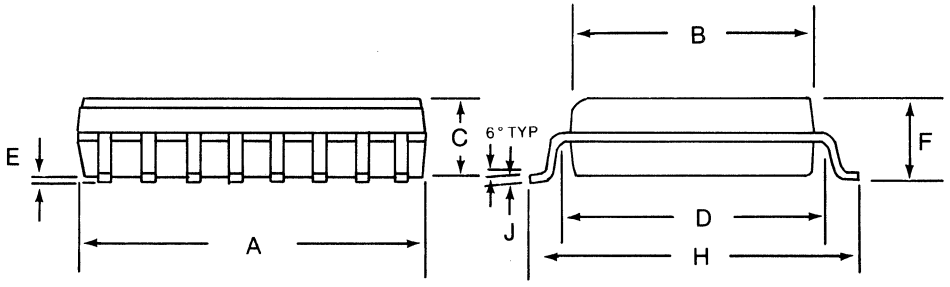




DS1210S
Nonvolatile Controller



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



Dallas Semiconductor

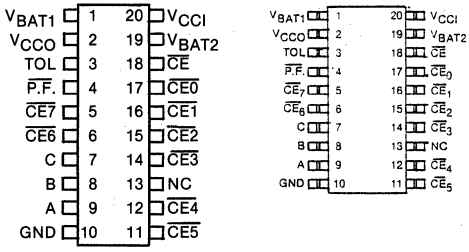
Nonvolatile Controller ×8

DS1211—20-Pin DIP
DS1211S—20-Pin SOIC

FEATURES

- Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 3 to 8 decoder provides control for up to 8 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 20-pin SOIC surface mount package

PIN CONNECTIONS



PIN NAMES

A, B, C	- Address Inputs
$\overline{CE}$	- Chip Enable Input
$\overline{CE0}$-$\overline{CE7}$	- Chip Enable Outputs
GND	- Ground
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
TOL	- Power Supply Tolerance
V_{CCI}	- +5V Supply
V_{CCO}	- RAM Supply
$\overline{P.F.}$	- Power Fail
N.C.	- No Connection

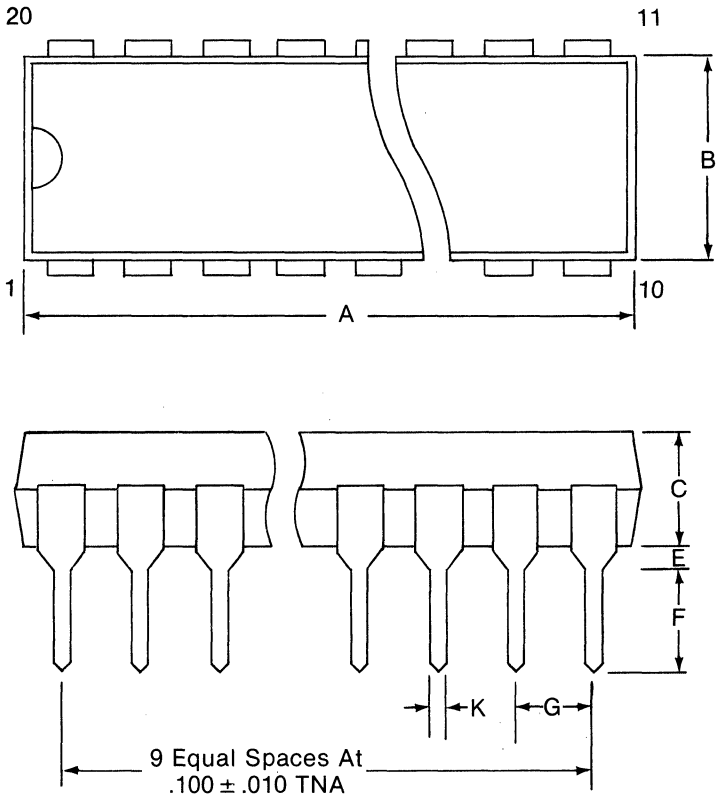
DESCRIPTION

The DS1211 is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption.

By combining the DS1211 nonvolatile controller/decoder chip and lithium batteries, ten years of nonvolatile RAM operation can be achieved for up to eight CMOS memories.

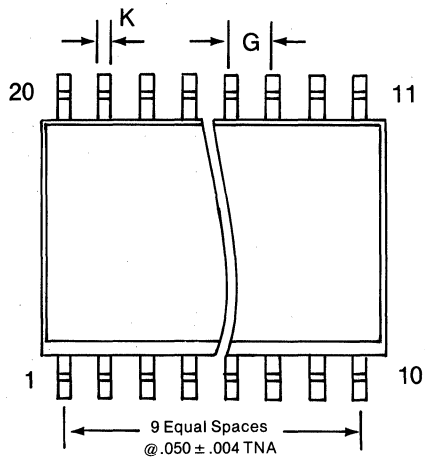
See the data sheet for the DS1212 for electrical specifications and operation.

DS1211
Nonvolatile Controller

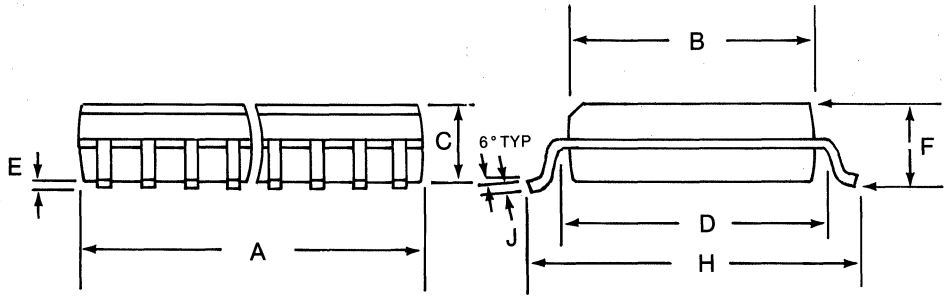


DIM.	INCHES	
	MIN.	MAX.
A	.960	1.040
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

DS1211S
Nonvolatile Controller



DIM.	INCHES	
	MIN.	MAX.
A	.503	.511
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



Dallas Semiconductor

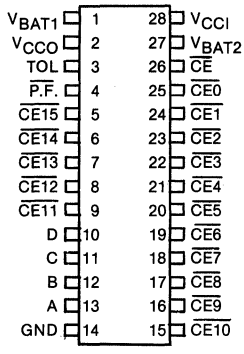
Nonvolatile Controller x 16

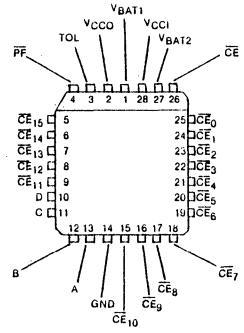
DS1212— 28-Pin DIP DS1212Q— 28-Pin PLCC

FEATURES

- Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 4 to 16 decoder provides control for up to 16 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 28-pin PLCC surface mount package

PIN CONNECTIONS





PIN NAMES

A, B, C, D	- Address Inputs
$\overline{CE}$	- Chip Enable
$\overline{CE0}$-$\overline{CE15}$	- Chip Enable Outputs
GND	- Ground
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
TOL	- Power Supply Tolerance
V_{CCI}	- +5V Supply
V_{CCO}	- RAM Supply
$\overline{P.F.}$	- Power Fail

DESCRIPTION

The DS1212 is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption.

By combining the DS1212 nonvolatile controller/decoder chip and lithium batteries, ten years of nonvolatile RAM operation can be achieved for up to sixteen CMOS memories.

OPERATION

The DS1212 nonvolatile controller/decoder performs six circuit functions required to decode and battery back up a bank of sixteen RAMs. First, the 4 to 16 decoder provides selection of one of sixteen RAMs. Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller/decoder provides is power fail detection. The DS1212 constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.75 volts, or 4.5 volts depending on the level of the tolerance Pin 3, a precision comparator outputs a power fail detect signal to the decoder/chip enable logic and the $\overline{PF}$ signal is driven low. The $\overline{PF}$ signal will remain low until V_{CCI} is back in normal limits. The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$-$\overline{CE15}$) to within 0.2 volts of V_{CCI} or battery supply. If $\overline{CE}$ is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 is connected to V_{CCO}, then power fail occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 4 to 16 decoder, shown in Figure 1. The fifth function the DS1212 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0 volts and data is in danger of being corrupted. The sixth function of the nonvolatile controller/decoder provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to insure reliability. The DS1212 provides an internal isolation switch which allows the connection of two batteries during battery backup operation. The battery with the highest voltage is selected for use. If one battery should fail, the other will then assume the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. For single battery applications the unused battery input must be grounded.

NONVOLATILE CONTROLLER/DECODER Figure 1

INPUTS						OUTPUTS															
V_{CCI}	$\overline{CE}$	D	C	B	A	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$	$\overline{CE5}$	$\overline{CE6}$	$\overline{CE7}$	$\overline{CE8}$	$\overline{CE9}$	$\overline{CE10}$	$\overline{CE11}$	$\overline{CE12}$	$\overline{CE13}$	$\overline{CE14}$	$\overline{CE15}$	$\overline{PF}$
≥ 4.75	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
< 4.75	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
≥ 4.75	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
≥ 4.75	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
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≥ 4.75	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
≥ 4.75	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
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≥ 4.75	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
≥ 4.75	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
≥ 4.75	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
≥ 4.75	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
≥ 4.75	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

H = High Level
L = Low Level
X = Irrelevant

NOTE:
V_{CCI} input is 250 mV lower when TOL PIN 3 = V_{CCO}

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
PIN 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	−0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1,2

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI} = 4.75V to 5.5V, Pin 3 = GND)
(0°C to 70°C, V_{CCI} = 4.5 to 5.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Current @V_{CCO} = V_{CCI} − 0.2	I_{CCO1}			80	mA	1,4,10
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Leakage	I_{LO}	−1.0		+1.0	uA	
$\overline{CE_0}$-$\overline{CE_{15}}$, $\overline{PF}$ Output @2.4V	I_{OH}	−1.0			mA	5
$\overline{CE_0}$-$\overline{CE_{15}}$, $\overline{PF}$ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point ($\overline{TOL}$ = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point ($\overline{TOL}$ = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

(0 °C to 70 °C, $V_{CCI} < V_{BAT}$)

$\overline{CE0}$-$\overline{CE15}$ Output	V_{OHL}	$V_{BAT} - 0.2$			V	3,7
Battery Current	I_{BAT}			0.1	uA	2,3
Battery Backup Current @$V_{CCO} = V_{BATI} - 0.5V$	I_{CC02}			100	uA	6,10,11

CAPACITANCE ($t_A = 25$ °C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

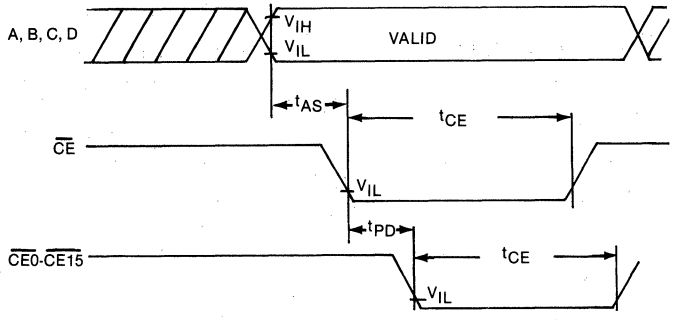
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{CCI} = 4.75 to 5.5V, Pin 3 = GND)
(0 °C to 70 °C , V_{CCI} = 4.5 to 5.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Address Set Up	t_{AS}	20			ns	9

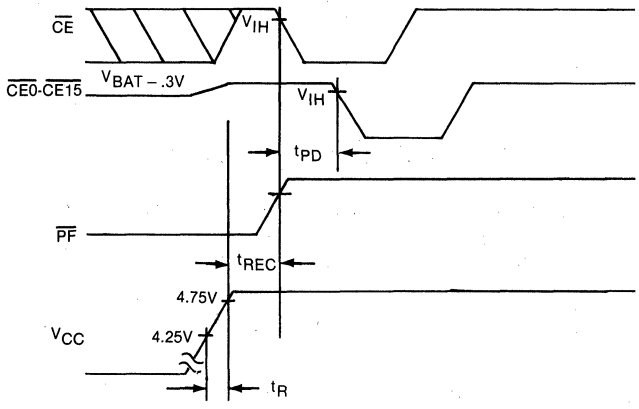
(0 °C to 70 °C, V_{CCI} < 4.75V, Pin 3 = GND)
(0 °C to 70 °C, V_{CCI}< 4.5V, Pin 3 = V_{CCO})

Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power Down	t_F	300			us	
V_{CC} Slew Rate Power Down	t_{FB}	10			us	
V_{CC} Slew Rate Power Up	t_R	0			us	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	us	7,8
Power Fail to $\overline{PF}$ Low	t_{PFL}	300			us	

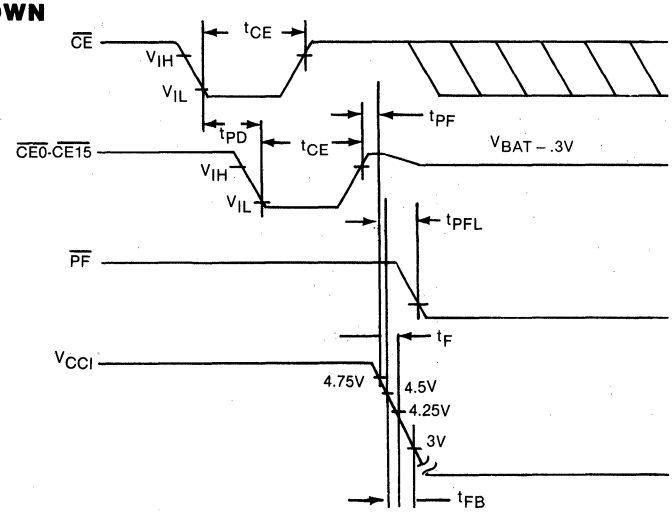
TIMING DIAGRAM—DECODER



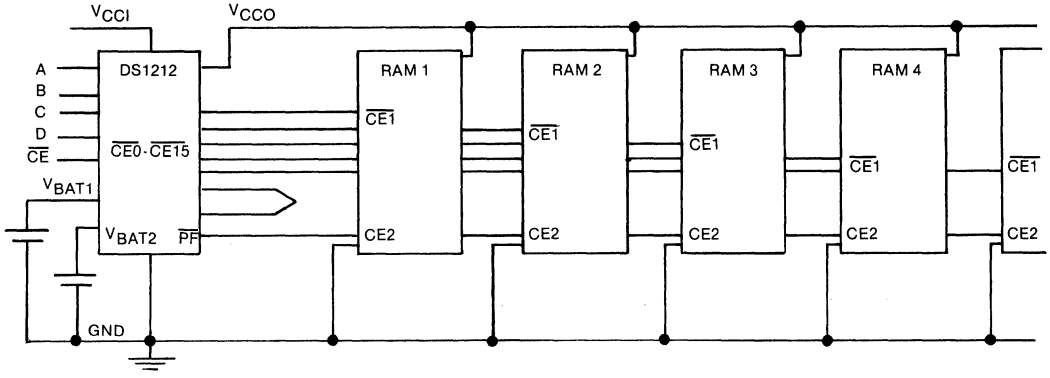
TIMING DIAGRAM—POWER UP



TIMING DIAGRAM—POWER DOWN



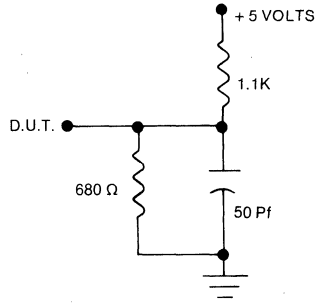
TYPICAL APPLICATION Figure 2



NOTES:

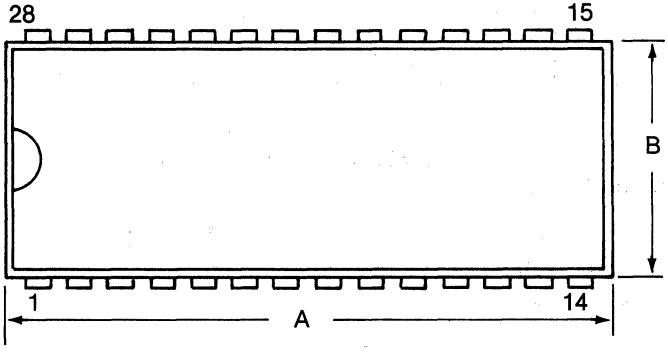
1. All voltages are referenced to ground
2. Only one battery input is required
3. Measured with V_{CCO} and $\overline{CE0}$ - $\overline{CE15}$ open
4. I_{CC01} is the maximum average load which the DS1212 can supply to the memories
5. Measured with a load as shown in Figure 3
6. I_{CC02} is the maximum average load current which the DS1212 can supply to the memories in the battery backup mode.
7. Chip enable outputs $\overline{CE0}$ - $\overline{CE15}$ can only sustain leakage current in the battery backup mode
8. t_{CE} max must be met to insure data integrity on power loss
9. t_{AS} is only required to keep the decoder outputs glitch-free. While $\overline{CE}$ is low, the outputs ($\overline{CE0}$ through $\overline{CE15}$) will be defined by inputs A through D with a propagation delay of t_{PD} from an A through D input change
10. For applications where higher currents are required, please see the Battery Manager data sheet (DS1259)
11. The DS1212 has a 5KΩ resistor in series with the battery input. As current from the battery increases over 100 uA, the voltage drop will increase proportionately. The device cannot be damaged by higher currents in the battery path

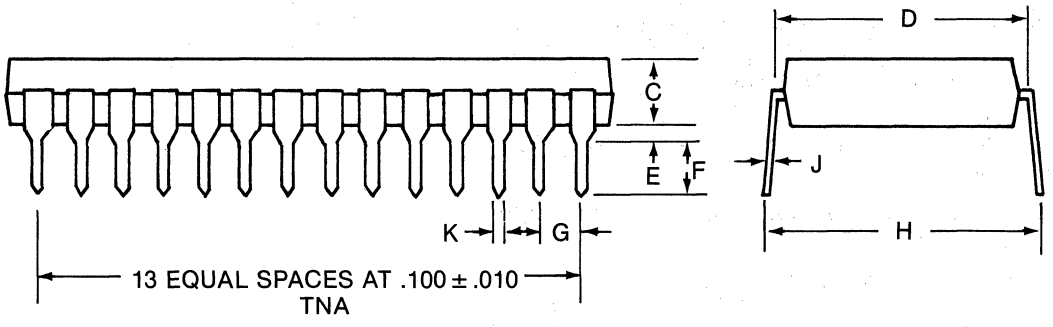
OUTPUT LOAD Figure 3



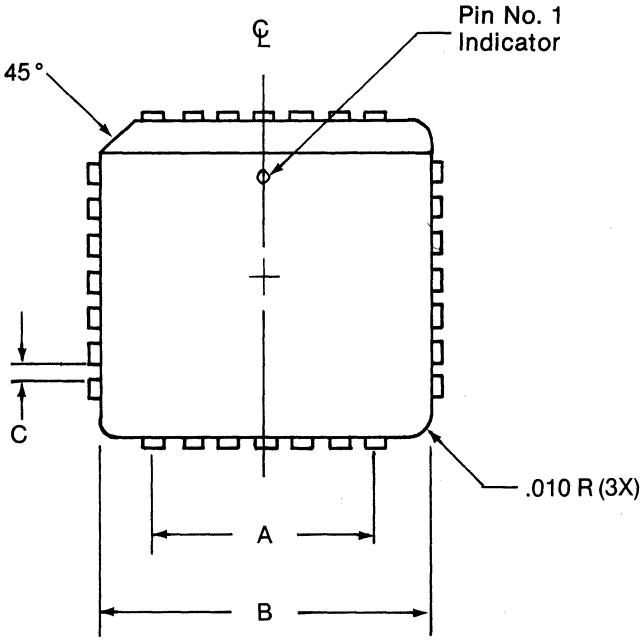
Nonvolatile Controller/Decoder
DS1212

DIM.	INCHES	
	MIN.	MAX.
A	1.440	1.480
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.620	.670
J	.008	.012
K	.015	.021

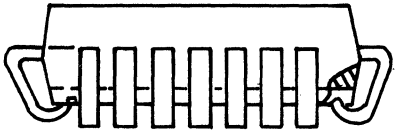


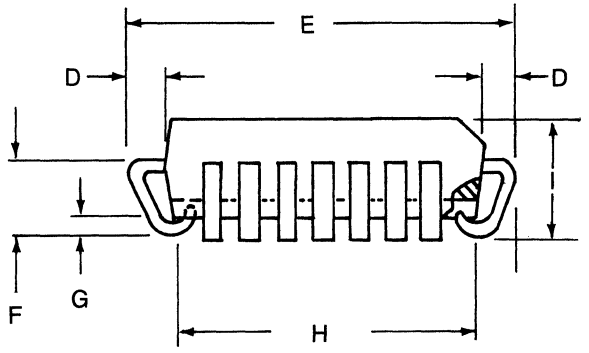


DS 1212Q



DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
I	.167	.173





1

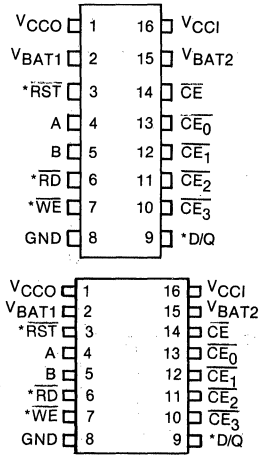
Dallas Semiconductor
Nonvolatile Controller ×4

DS1221—16-Pin DIP
DS1221S—16-Pin SOIC

FEATURES

- Converts CMOS RAMs into Nonvolatile Memories
- Data is automatically protected during power loss
- 2 to 4 Decoder provides for up to 4 CMOS RAMs
- Provides for redundant batteries
- Test battery condition on power up
- Full ±10% operating range
- Unauthorized access can be prevented with optional security feature
- 16-pin 0.3-inch DIP saves P.C. board space
- Optional 16-pin SOIC surface mount package

PIN CONNECTIONS



PIN NAMES

A, B	- Address Inputs
$\overline{CE}$	- Chip Enable Input
$\overline{CE_0}$-$\overline{CE_3}$	- Chip Enable Outputs
V_{BAT1}	- + Battery 1
V_{BAT2}	- + Battery 2
*$\overline{RST}$	- Reset
V_{CCI}	- + 5V Supply
V_{CCO}	- RAM Supply
*$\overline{RD}$	- Read Input
*$\overline{WE}$	- Write Input
*D/Q	- Data Input/Output

*Used with optional security circuit only and must be connected to ground in all other cases.

DESCRIPTION

The DS1221 is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. An optional security code prevents unauthorized users from obtaining access to the memory space. The nonvolatile controller/decoder circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. By combining the DS1221 with up to four CMOS memories and lithium batteries, ten years of nonvolatile operation can be achieved.

CONTROLLER/DECODER OPERATION

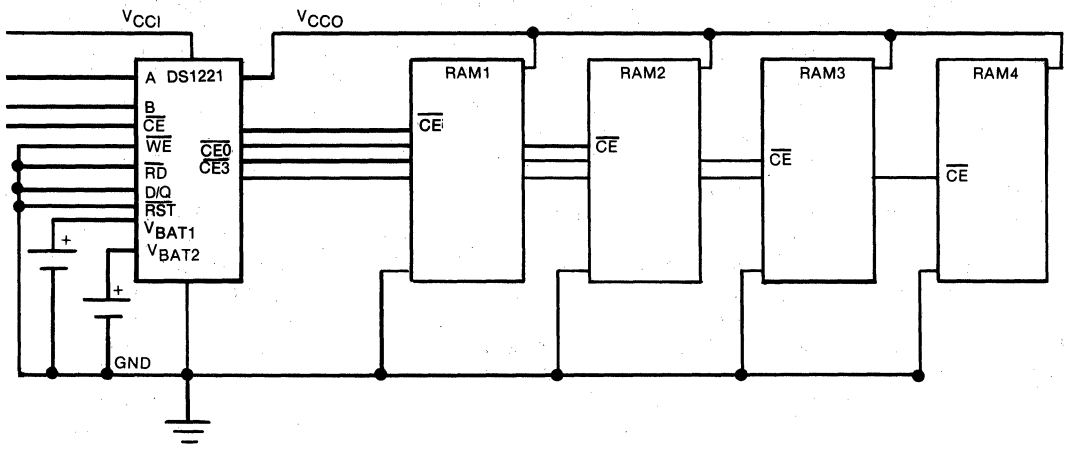
The DS1221 nonvolatile controller/decoder performs six circuit functions required to decode and battery back up a bank of up to four CMOS RAMs. First, a 2 to 4 decoder provides selection of one of four RAMs (See Figure 1). Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater, to the V_{CCO} pin. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller/decoder provides is power fail detection. The DS1221 constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.5 volts, a precision comparator detects the condition and inhibits the RAM chip enables ($\overline{CE0}$ through $\overline{CE3}$). The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$-$\overline{CE3}$) to within 0.2 volts of V_{CCI} or battery supply. If the Chip Enable Input ($\overline{CE}$) is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power failure detection occurs in the range of 4.5 to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 2 to 4 decoder. The fifth function the DS1221 performs is to check battery status to warn of potential data loss. Each time that V_{CCI} power is restored the battery voltage is checked with a precision comparator. If the connected battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memories are questionable. The sixth function of the nonvolatile controller/decoder provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to insure reliability. The DS1221 provides an internal isolation switch which provides for connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. If only one battery is used, the second battery input must be grounded. Figure 2 illustrates the connections required for the DS1221 in a typical application.

NONVOLATILE CONTROLLER/DECODER Figure 1

	INPUTS			OUTPUTS			
V_{CCI}	$\overline{CE}$	B	A	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
≥ 4.5	H	X	X	H	H	H	H
< 4.25	X	X	X	H	H	H	H
≥ 4.5	L	L	L	L	H	H	H
≥ 4.5	L	L	H	H	L	H	H
≥ 4.5	L	H	L	H	H	L	H
≥ 4.5	L	H	H	H	H	H	L

H = High Level
L = Low Level
X = Irrelevant

TYPICAL APPLICATION Figure 2



Battery Backup Current Drain

DS1221	- .1 uA @ 25° C
RAM-5564 × 4	- .8 uA @ 25° C
Total	.9 uA @ 25° C

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to 125°C
Soldering Temperature 260°C for 10 Sec
Short Circuit Output Current 20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0 Input	V_{IL}	−0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1,2

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

Supply Current	I_{CCI}			5	mA	3
Suply Voltage	V_{CCO}	$V_{CC}-0.2$			V	1
Supply Current	I_{CCO1}			80	mA	4,10
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Leakage	I_{LO}	−1.0		+1.0	uA	
$\overline{CE0}$-$\overline{CE3}$, DQ Output @2.4V	I_{OH}	−1.0			mA	5
$\overline{CE0}$-$\overline{CE3}$, DQ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1

(0°C to 70°C, V_{CC}<4.25)

$\overline{CE0}$-$\overline{CE3}$ Output	V_{OHL}	$V_{CC}-0.2$ $V_{BAT}-0.2$			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			0.1	uA	3
Battery Backup Current @$V_{CCO}=V_{BAT}-0.5V$	I_{CCO2}			100	uA	6,7,10

CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

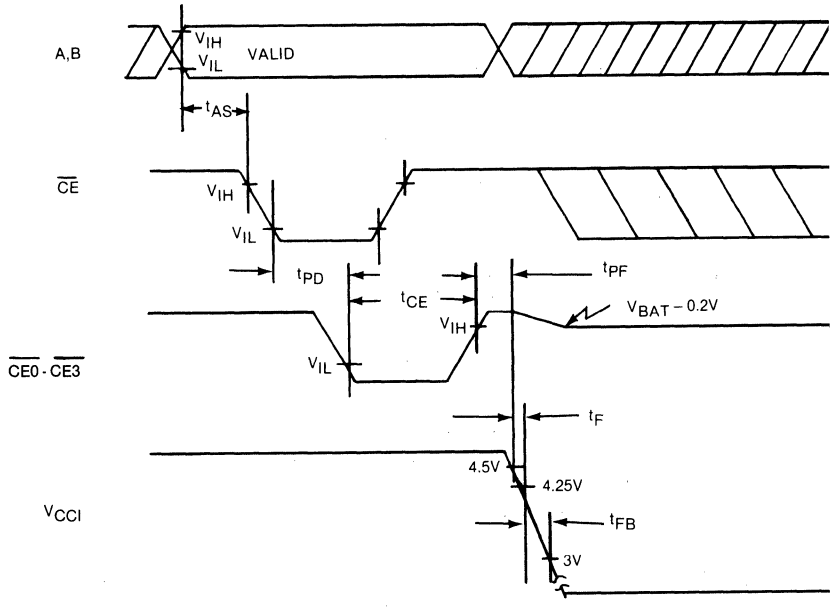
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	
Address Set Up	t_{AS}	20			ns	9

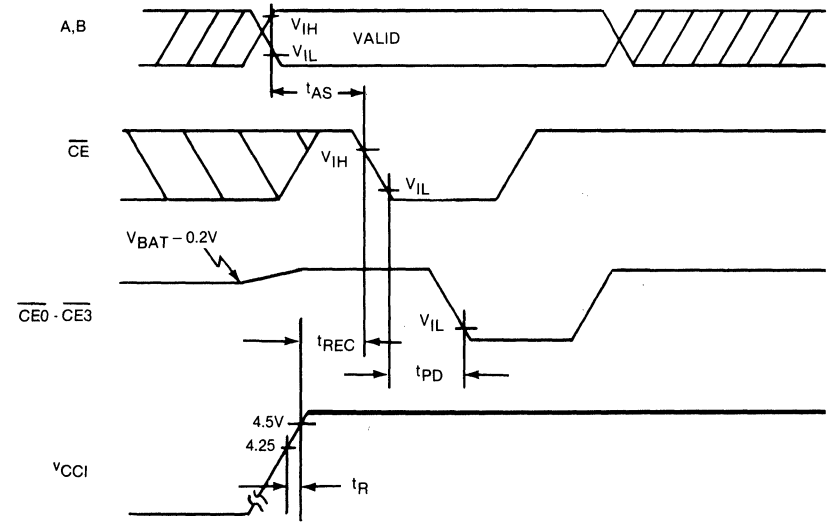
(0°C to 70°C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}	2	5	10	ms	
V_{CC} Slew Rate 4.5 - 4.25V	t_F	300			us	
V_{CC} Slew Rate 4.25 - 3V	t_{FB}	10			us	
V_{CC} Slew Rate 4.25 - 4.5V	t_R	0			us	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	us	7,8

TIMING DIAGRAM—POWER DOWN



TIMING DIAGRAM—POWER UP

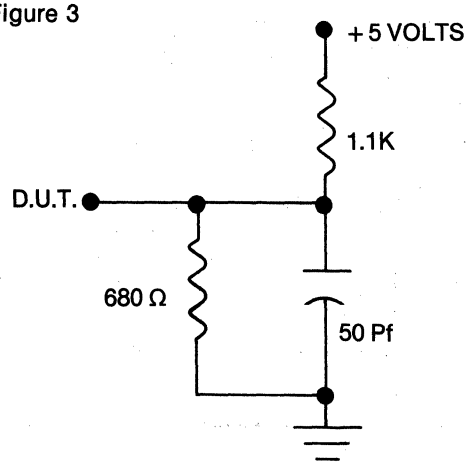


NOTES:

1. All voltages are referenced to ground
2. Only one battery input is required
3. Measured with V_{CCO} and $\overline{CE0}$ - $\overline{CE3}$ open
4. I_{CCO1} is the maximum average load which the DS1221 can supply to the memories
5. Measured with a load as shown in Figure 3
6. I_{CCO2} is the maximum average load current which the DS1221 can supply to the memories in the battery backup mode
7. Chip enable outputs $\overline{CE0}$ - $\overline{CE3}$ can only sustain leakage current in the battery backup mode
8. t_{CE} max must be met to insure data integrity on power loss
9. t_{AS} is only required to keep the decoder outputs glitch-free. While $\overline{CE}$ is low, the outputs ($\overline{CE0}$ through $\overline{CE3}$) will be defined by inputs A and B with a propagation delay of t_{PD} from an A or B input change
10. For applications where higher currents are required, please see the Battery Manager data sheet (DS1259)

OUTPUT LOAD

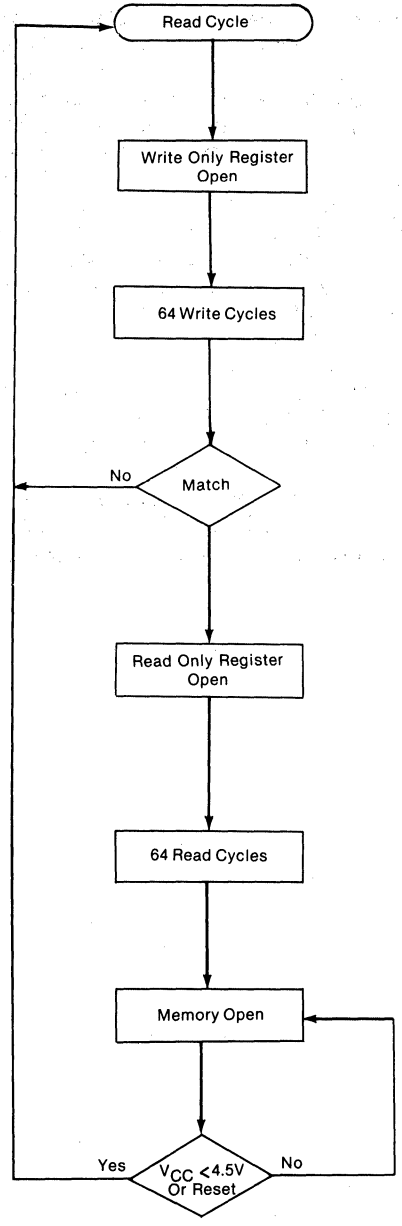
Figure 3



SECURITY OPTION

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 1). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1221 using the write enable signal ($\overline{WE}$), the chip enable signal ($\overline{CE}$), and the data input/output signal (DQ). The code is written to the DS1221 without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1221 by Dallas Semiconductor at time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1221 and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register may be used by software to determine if the DS1221 will be permitted to be used with that particular system. After the 64th read cycle has been executed the DS1221 is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If V_{CC} falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.
Note: Contact Dallas Semiconductor sales office for code assignment.

SECURITY SEQUENCE
Figure 1

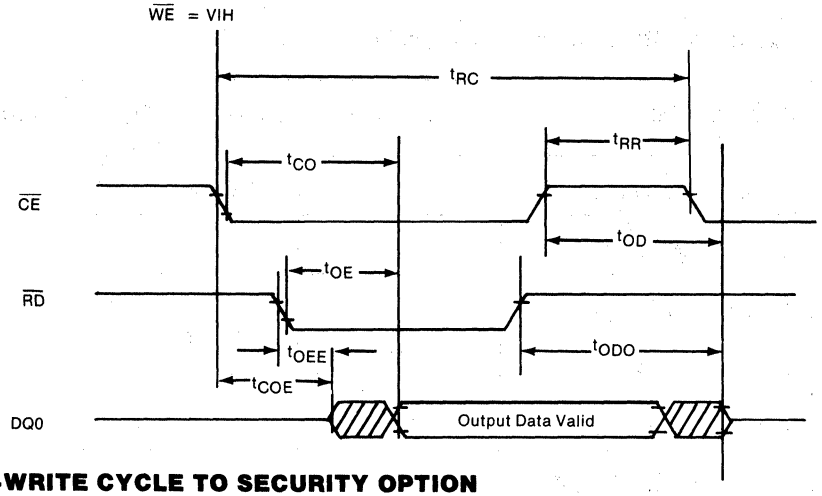


SECURITY OPTION

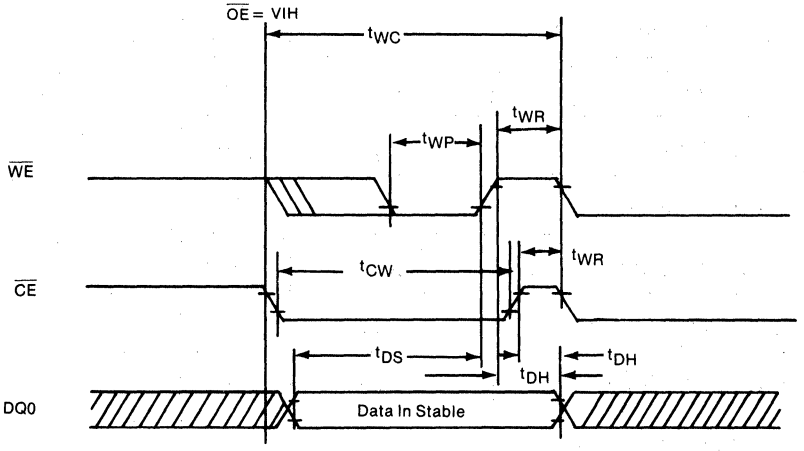
A.C. ELECTRICAL CHARACTERISTICS (0 °C - 70 °C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Read Cycle Time	t_{RC}	250			ns
$\overline{CE}$ Access Time	t_{CO}			200	ns
$\overline{RD}$ Access Time	t_{OE}			100	ns
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns
$\overline{RD}$ To Output Low Z	t_{OEE}	10			ns
$\overline{CE}$ To Output High Z	t_{OD}			100	ns
$\overline{RD}$ To Output High Z	t_{ODO}			100	ns
Read Recovery	t_{RR}	50			ns
Write Cycle	t_{WC}	250			ns
Write Pulse Width	t_{WP}	170			ns
Write Recovery	t_{WR}	50			ns
Data Set Up	t_{DS}	100			ns
Data Hold Time	t_{DH}	0			ns
$\overline{CE}$ Pulse Width	t_{CW}	170			ns
Reset Pulse Width	t_{RST}	200			ns

TIMING DIAGRAM—READ CYCLE TO SECURITY OPTION



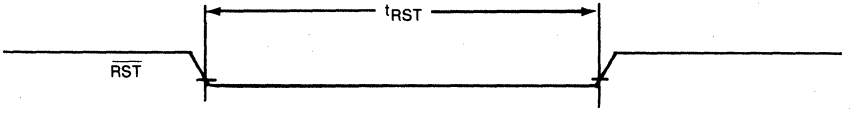
TIMING DIAGRAM—WRITE CYCLE TO SECURITY OPTION

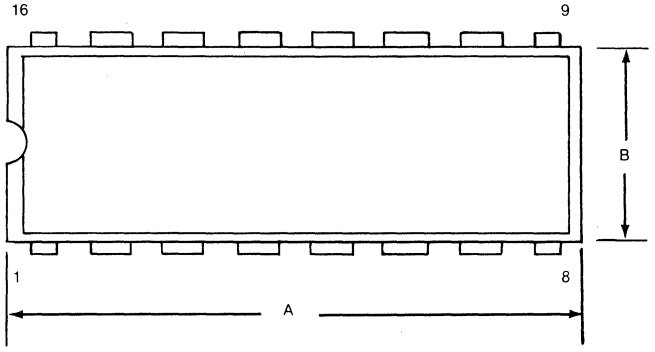


NOTES:

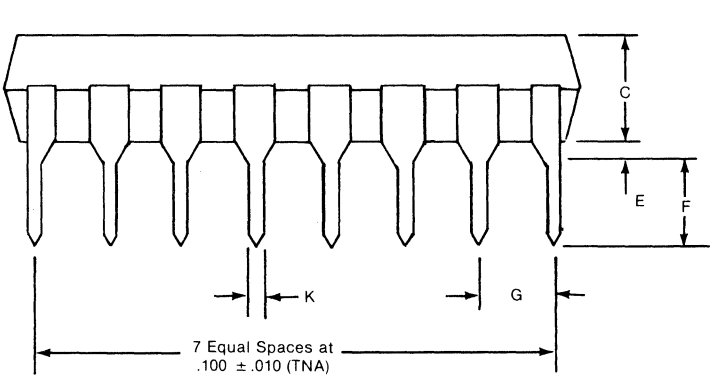
1. t_{DH} and t_{DS} are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
2. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.

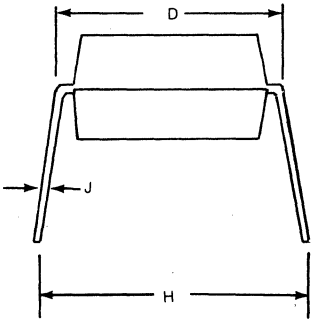
TIMING DIAGRAM—RESET FOR SECURITY OPTION

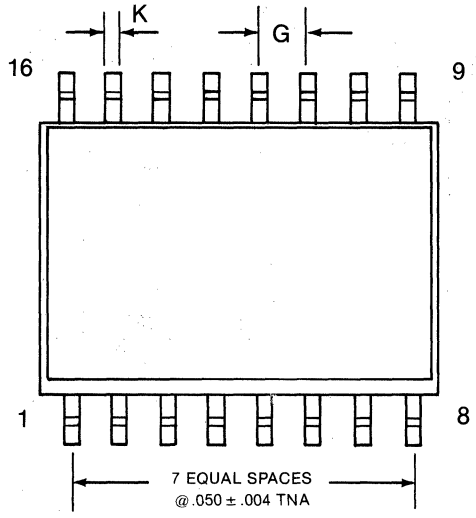




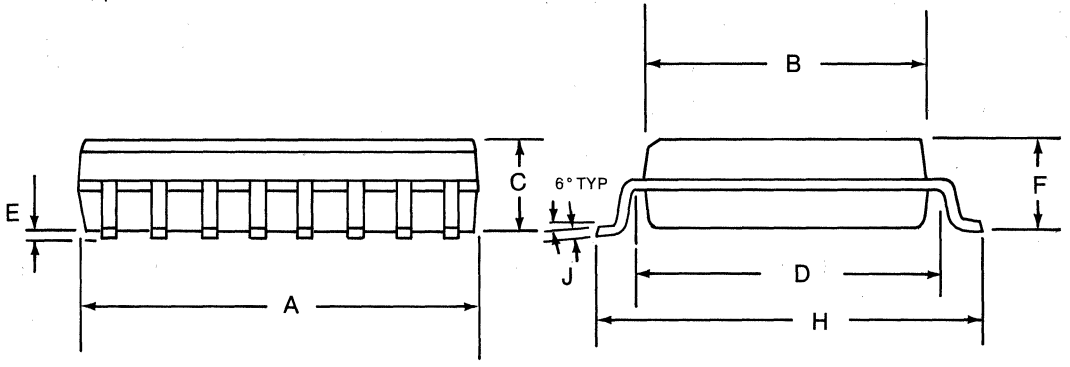
DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021







DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



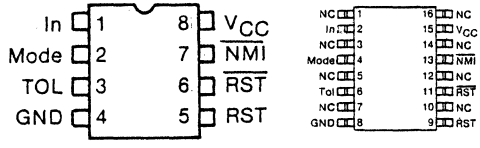
Dallas Semiconductor
Power Monitor

DS1231—8-Pin DIP
DS1231S—16-Pin SOIC

FEATURES

- Warns processor of an impending power failure
- Provides time for an orderly shutdown
- Prevents processor from destroying non-volatile memory during power transients
- Automatically restarts processor after power is restored
- Suitable for linear or switching power supplies
- Adjusts to hold time of the power supply
- Supplies necessary signals for processor interface
- Accurate 5% or 10% V_{CC} monitoring
- Replaces power up reset circuitry
- No external capacitors required
- Optional 16-pin SOIC surface mount package

PIN CONNECTIONS



PIN NAMES

In	- Input
Mode	- Selects input pin characteristics
TOL	- Selects 5% or 10% V_{CC} detect
GND	- Ground
$\overline{RST}$	- Reset (Active High)
RST	- Reset (Active Low, open drain)
$\overline{NMI}$	- Nonmaskable interrupt
V_{CC}	- +5 V Supply
NC	- No Connections

DESCRIPTION

The DS1231 Power Monitor uses a precise temperature compensated reference circuit which provides an orderly shutdown and an automatic restart of a processor-based system. A signal warning of an impending power failure is generated well before regulated DC voltages go out of specification by monitoring high voltage inputs to the power supply regulators. If line isolation is required, a UL-approved opto-isolator can be directly interfaced to the DS1231. The time for processor shutdown is directly proportional to the available hold-up time of the power supply. Just before the hold-up time is exhausted, the power monitor unconditionally halts the processor to prevent spurious cycles by enabling Reset as V_{CC} falls below a selectable 5 or 10 percent threshold. When power returns, the processor is held inactive until well after power conditions have stabilized, safeguarding any nonvolatile memory in the system from inadvertent data changes.

OPERATION

The DS1231 Power Monitor provides the function of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. The main elements of the DS1231 are illustrated in Figure 1. As shown, the DS1231 actually has two comparators, one for monitoring the input (Pin 1) and one for monitoring V_{CC} (Pin 8). The V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6) when V_{CC} falls below a preset trip level as defined by TOL (Pin 3).

When TOL is connected to ground, the RST and $\overline{RST}$ signals will become active as V_{CC} goes below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} goes below 4.5 volts. The RST and $\overline{RST}$ signals are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply to stabilize (see Figure 2).

The comparator monitoring the input pin produces the $\overline{NMI}$ signal (Pin 7) when the input threshold voltage (VTP) falls to a level as determined by mode (Pin 2). When the mode pin is connected to V_{CC}, detection occurs at VTP−. In this mode Pin 1 is an extremely high impedance input allowing for a simple resistor voltage divider network to interface with high voltage signals. When the mode pin is connected to ground, detection occurs at VTP+. In this mode Pin 1 sources 30 uA of current allowing for connection to switched inputs, such as a UL-approved opto-isolator. The flexibility of the input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time allotted between $\overline{NMI}$ and $\overline{RST}$. On power up, $\overline{NMI}$ is released as soon as the input threshold voltage (VTP) is achieved and V_{CC} is within nominal limits. In both modes of operation the input pin has hysteresis for noise immunity (Figure 3).

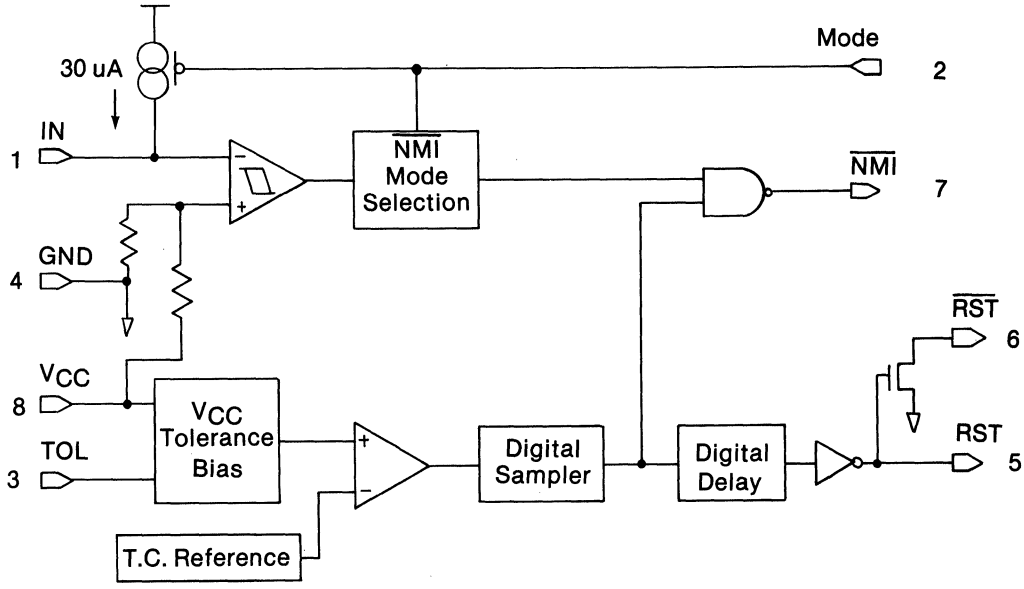
APPLICATION—MODE PIN CONNECTED TO V_{CC}

When the mode pin is connected to V_{CC}, Pin 1 is a high impedance input. The voltage sense point and the level of voltage at the sense point are dependent upon the application (Figure 4). The sense point may be developed from the AC power line by rectifying and filtering the AC. Alternatively, a DC voltage level may be selected which is closer to the AC power input than the regulated +5-volt supply, so that ample time is provided for warning before regulation is lost.

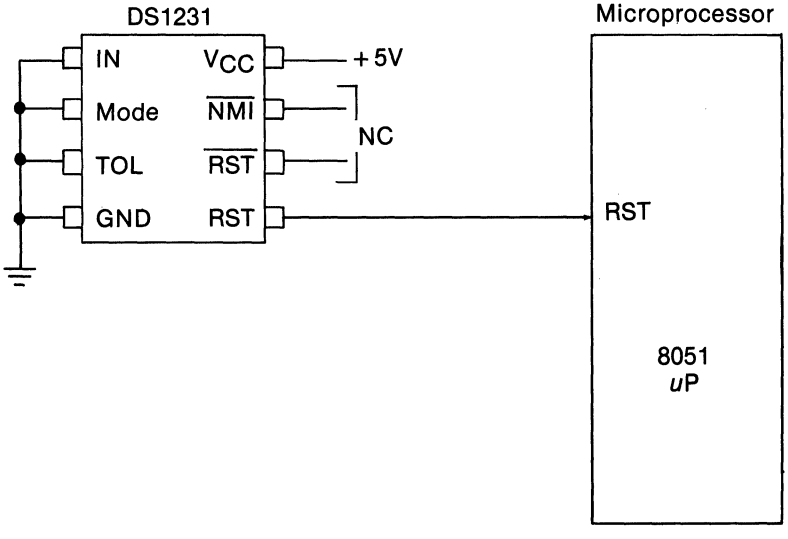
Proper operation of the DS1231 requires a maximum voltage of 5 volts at the input (Pin 1) which must be derived from the maximum voltage at the sense point. This is accomplished with a simple voltage divider network of R1 and R2. Since the IN trip point VTP− is 2.3 volts (using the −20 device), and the maximum allowable voltage on Pin 1 is 5 volts, the dynamic range of voltage at the sense point is set by the ratio of 2.3/5.0 = .46 min. This ratio determines the maximum deviation between the maximum voltage at the sense point and the actual voltage which will generate $\overline{NMI}$.

Having established the desired ratio, and confirming that the ratio is greater than .46 and less than 1, the proper values for R1 and R2 can be determined by the equation as shown in Figure 4. A simple approach to solving this equation is to select a value for R2 which is high impedance to keep power consumption low and solve for R1. Figure 5 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is connected to V_{CC}.

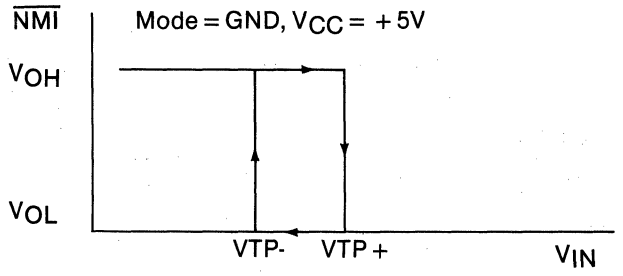
POWER MONITOR BLOCK DIAGRAM Figure 1



POWER UP RESET Figure 2

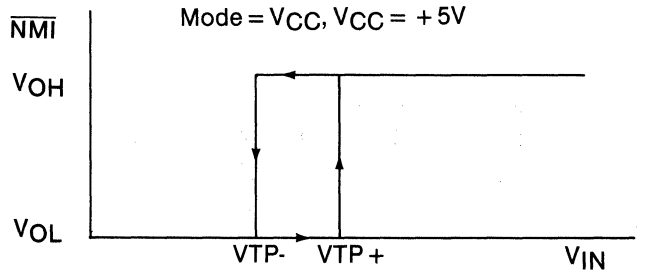


INPUT PIN HYSTERESIS Figure 3

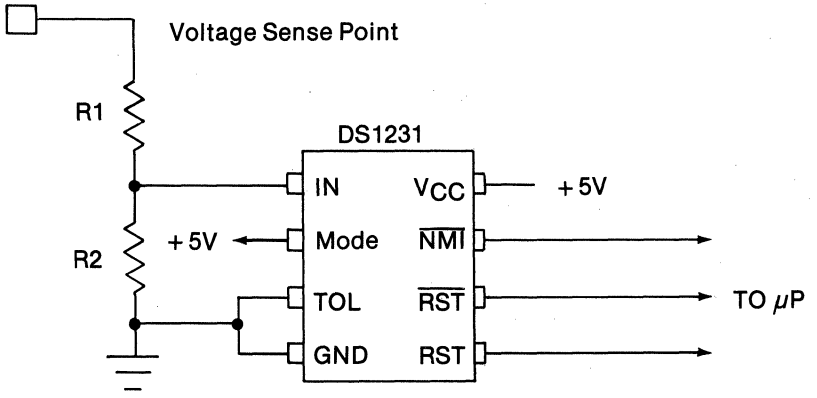


	-20	-35	-50
VTP-	2.3	2.15	2.0
VTP+	2.5	2.5	2.5

NOTE: Hysteresis tolerance is ±60 mV.



APPLICATION WITH MODE PIN CONNECTED TO V_{CC} Figure 4



$$V_{Sense} = \frac{R1 + R2}{R2} \times 2.3 \qquad V_{Max} = \frac{V_{Sense}}{VTP-} \times 5.0$$

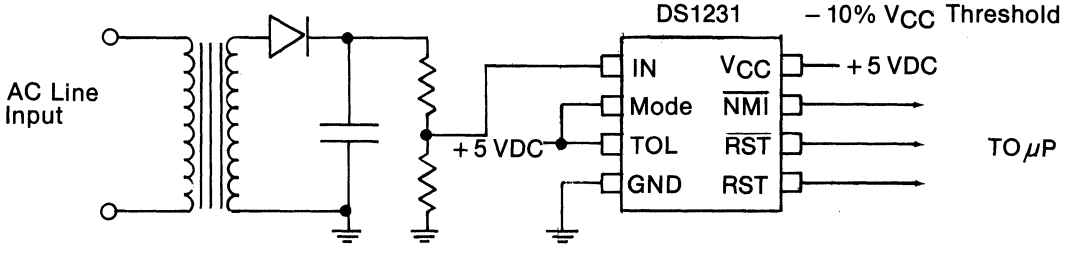
Example: V_{Sense} = 8 volts at Trip Point and a maximum voltage of 17.5V with R2 = 10K

Then $8 = \frac{R1 + 10K}{10K} \times 2.3$ R1 = 25K

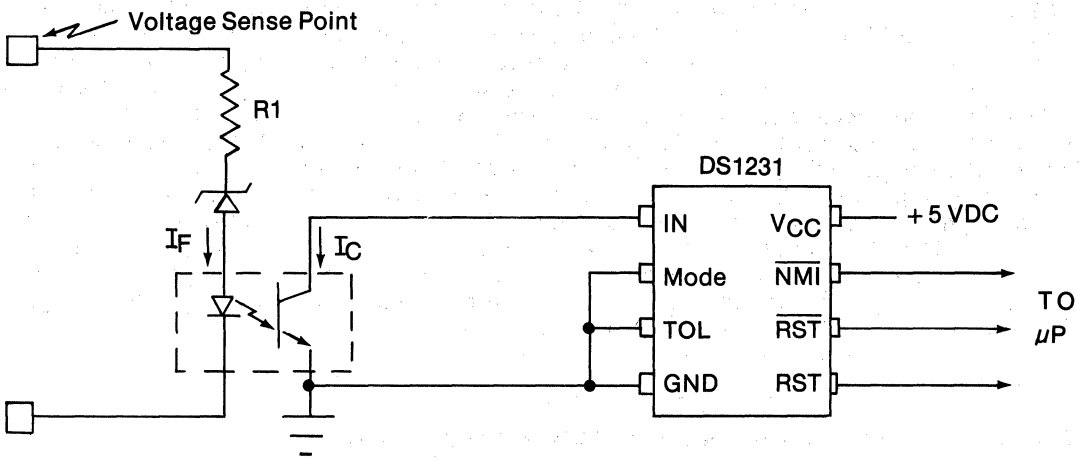
APPLICATION—MODE PIN CONNECTED TO GROUND

When the mode pin is connected to ground, Pin 1 is a current source of 30 uA with a VTP+ of 2.5 volts. Pin 1 is held below the trip point by a switching device like an opto-isolator as shown in Figure 6. Determination of the sense point has the same criteria as discussed in the previous application. However, determining component values is significantly different. In this mode, the maximum dynamic range of the sense point versus desired trip voltage is primarily determined by the selection of a zener diode. As an example, if the maximum voltage at the sense point is 200V and the desired trip point is 150V, then a zener diode of 150V will approximately set the trip point. This is particularly true if power consumption on the high voltage side of the opto-isolator is not an issue. However, if power consumption is a concern, then it is desirable to make the value of R1 high. As the value of R1 increases, the effect of the LED current in the opto-isolator starts to affect the IN trip point. This can be seen from the equation shown in Figure 6. R1 must also be sized low enough to allow the opto-isolator to sink the 30 uA of collector current required by Pin 1 and still have enough resistance to keep the maximum current through the opto-isolator's LED within data sheet limits. Figure 7 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is grounded.

AC VOLTAGE MONITOR WITH TRANSFORMER ISOLATION Figure 5



APPLICATION WITH MODE PIN GROUNDED Figure 6



$$\text{Voltage Sense Point (Trip Value)} = V_Z + \frac{I_C}{CTR} \times R1$$

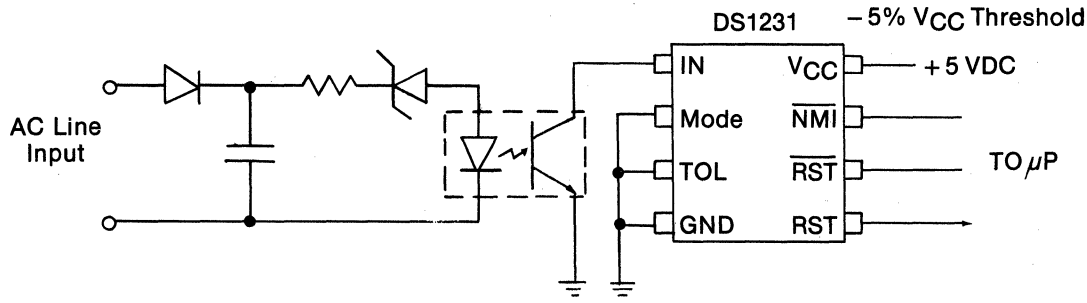
$$CTR = \frac{I_C}{I_F}$$

CTR = Current Transfer Ratio
V_Z = Zener Voltage

Example: CTR = 0.2 $I_C = 30uA$ $I_F = 150uA$
Voltage Sense Point = 105 and $V_Z = 100$ volts

Then $105 = 100 + \frac{30}{0.2} \times R1$ $R1 = 33K$

AC VOLTAGE MONITOR WITH OPTO-ISOLATION Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Pin 1	V_{IN}			V_{CC}	V	1

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	−1.0		+1.0	uA	2
Output Current @2.4V	I_{OH}	1.0	2.0		mA	
Output Current @0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		0.5	2.0	mA	3
Input Pin 1 (Mode = GND)	I_C	15	25	50	uA	
Input Pin 1 (Mode = V_{CC})	I_C			0.1	uA	
IN Trip Point (Mode = GND)	VTP	See Figure 3				1
IN Trip Point (Mode = V_{CC})	VTP					1
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

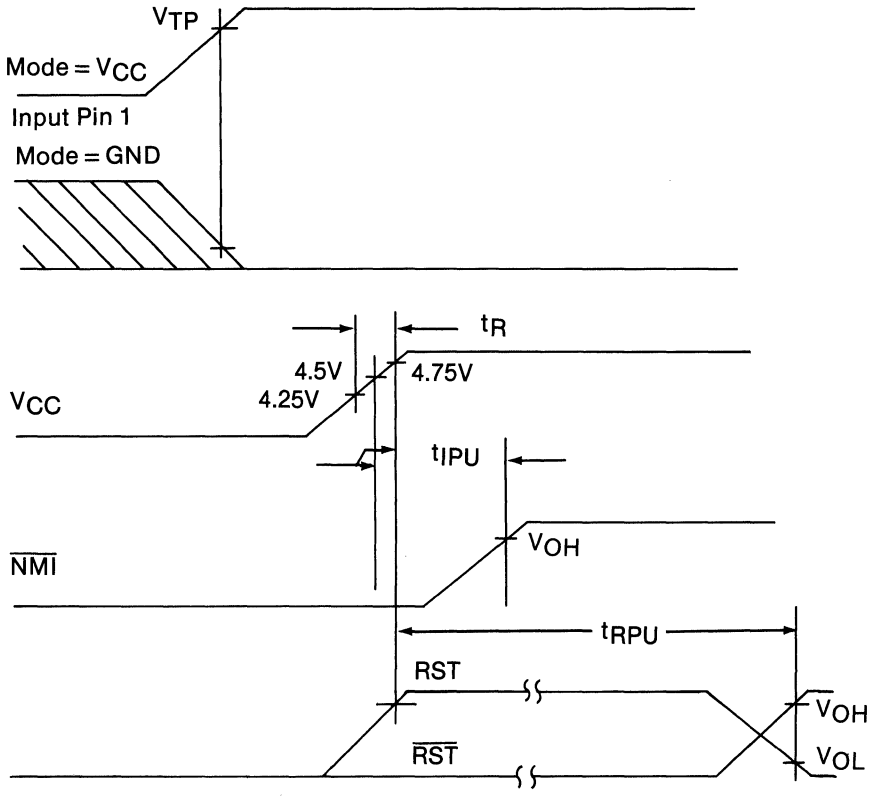
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{TP} to $\overline{NMI}$ Delay	t_{IPD}			1.1	us	
V_{CC} Slew Rate 4.75-4.25V	t_F	300			us	
V_{CC} Detect to $\overline{RST}$ and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Detect to $\overline{NMI}$	t_{IPU}			200	us	4
V_{CC} Detect to $\overline{RST}$ and $\overline{RST}$	t_{RPU}	250	500	1000	ms	4
V_{CC} Slew Rate 4.25-4.75V	t_R	0			ns	

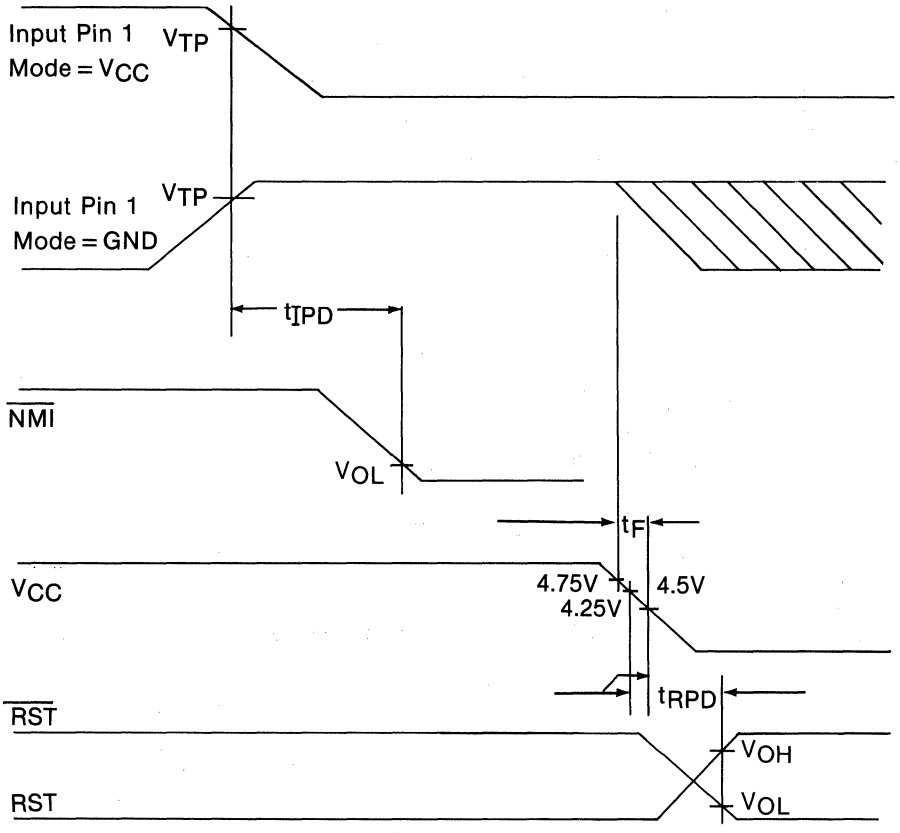
NOTES:

1. All voltages referenced to ground.
2. $V_{CC} = +5.0$ volts with outputs open.
3. Measured with outputs open.
4. $t_R = 5us$.

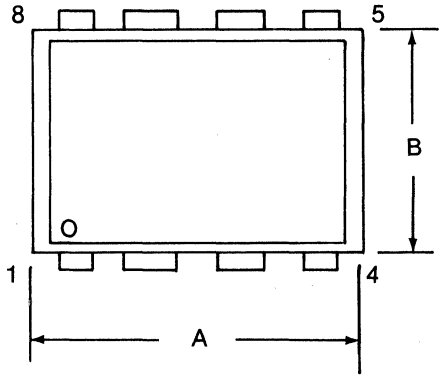
TIMING DIAGRAM—POWER UP



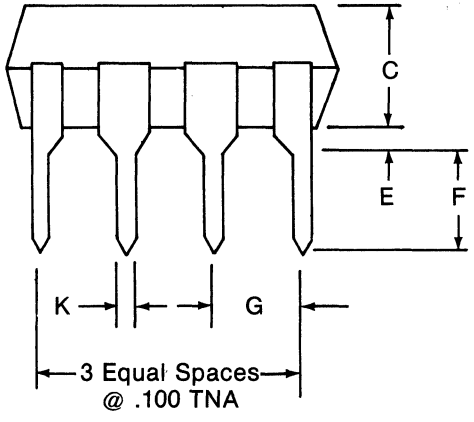
TIMING DIAGRAM—POWER DOWN

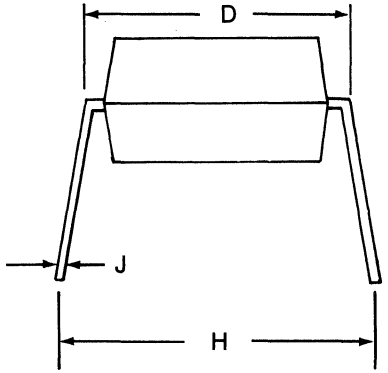


DS1231
Power Monitor

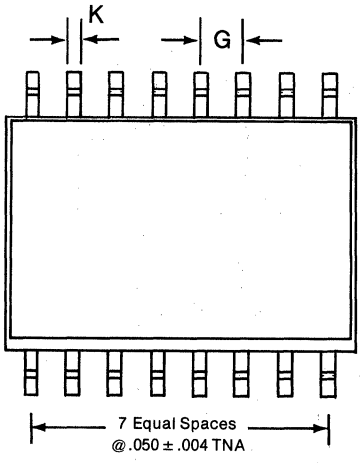


DIM.	INCHES	
	MIN.	MAX.
A	.340	.400
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

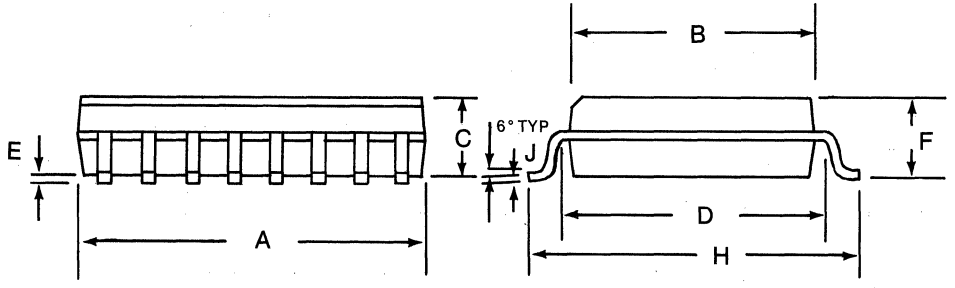




DS1231S
Power Monitor



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



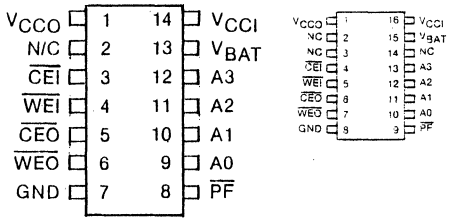
Dallas Semiconductor
Conditional Nonvolatile Controller

DS1234—14-Pin DIP
DS1234S—16-Pin SOIC

FEATURES

- Converts CMOS static RAMs into nonvolatile memories
- Software controlled write inhibit
- Software controlled battery disconnect extends battery life
- Unconditionally write protects when V_{CC} is out of tolerance
- Consumes less than 100 nA of battery current
- Power fail signal can be used to interrupt processor on power failure
- Low forward voltage drop on the V_{CC} switch
- Optional 16-pin SOIC surface mount package

PIN CONNECTIONS



PIN NAMES

Pin 1	- V_{CCO}	RAM Supply
Pin 2	- N/C	No Connection
Pin 3	- $\overline{CEI}$	Chip Enable Input
Pin 4	- $\overline{WEI}$	Write Enable Input
Pin 5	- $\overline{CEO}$	Chip Enable to Ram
Pin 6	- $\overline{WEO}$	Write Enable to RAM
Pin 7	- GND	Ground
Pin 8	- $\overline{PF}$	Power Fail Output
Pins 9-12	- A0-A3	Address Inputs
Pin 13	- V_{BAT}	Battery Input
Pin 14	- V_{CCI}	+5V Supply

DESCRIPTION

The DS1234 is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory with the added features of two software selectable switches. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, Chip Enable and Write Enable to the RAM are inhibited to accomplish write protection and the battery is switched on to supply the memory with uninterrupted power. The two software selectable switches provided by the DS1234 are capable of inhibiting both the write enable to the RAM and the battery back-up circuitry by a pattern recognition sequence across four address lines. Inhibiting the write enable to the nonvolatile RAM provides data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery back-up is not needed.

OPERATION

The DS1234 Conditional Nonvolatile Controller performs three circuit functions required to battery back-up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}), depending on whichever is greater. This switch has a voltage drop of less than 0.2V. The second function which the nonvolatile controller provides is power fail detection. The DS1234 constantly monitors the incoming supply. When the supply goes out of tolerance, a comparator detects power fail and inhibits chip enable and write enable. The threshold voltage, V_{TP}, at which power fail is detected is defined as 1.26 times V_{BAT}. The third function of write protection is accomplished by holding the $\overline{CEO}$ and $\overline{WEO}$ output signals to within 0.2 volts of the V_{CCI} or battery supply. In addition to the nonvolatile controller functions, the DS1234 supplies two software selectable switches for master control of the write enable and the nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (see Tables 1 and 2). Prior to entering the pattern recognition sequence which will define the two switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointer to clock zero. Each four-bit compare word is clocked into the DS1234 on the low-going edge of $\overline{CEI}$. A0, A1 and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven, and the last five are used to define the switch settings. The eleventh address cycle, starting at zero, defines the switch which inhibits the write enable to the RAM ($\overline{WEO}$). A logic one in this location allows read/write operations so that $\overline{WEO}$ will follow $\overline{WEI}$ and data can be updated. A zero on cycle eleven turns the RAM into a read-only memory (ROM). The next four address cycles, 12 through 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010, respectively, activates the nonvolatile controller and data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation. At the completion of the 16th cycle, if the pattern recognition sequence is correct, the switch settings defined in cycles 11 through 15 are transferred and are active for the next memory cycle. When external battery power is applied for the first time, the DS1234 will come up with the nonvolatile controller off. Upon initial V_{CC} power the write enable will be set in read/write operation ($\overline{WEI} = \overline{WEO}$).

ADDRESS INPUT PATTERN Table 1

	Cycle Number														
Address Inputs	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_3	1	0	1	0	0	0	1	1	0	1	0	*	*	*	*	*
A_2	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_1	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_0	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

*See Table 2

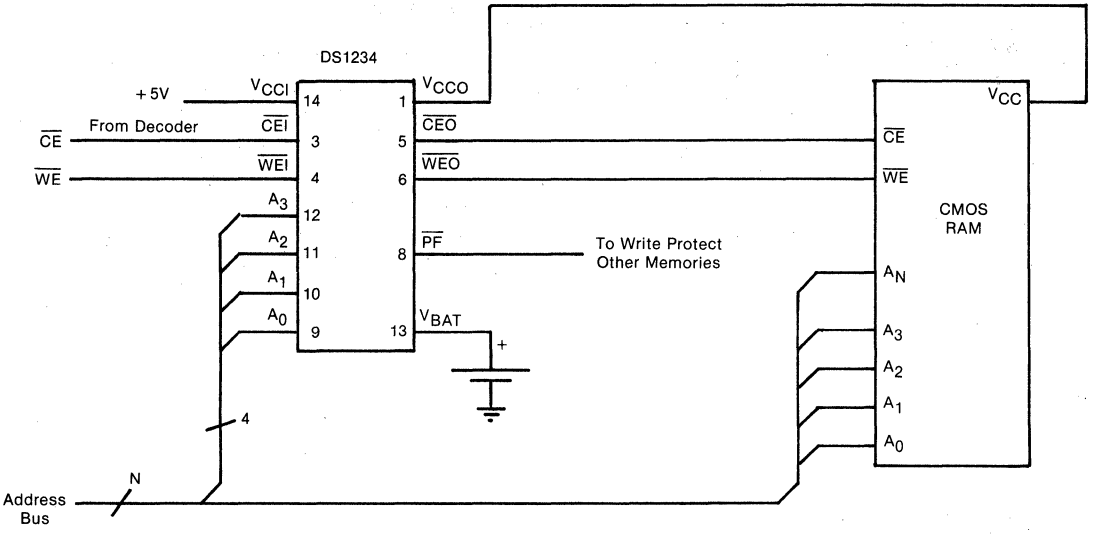
CONTROL SELECT Table 2

$\overline{WE}$	Battery Control				Operation
11	**12**	**13**	**14**	**15**	
0	×	×	×	×	Read Only Operation
1	×	×	×	×	Read/Write Operation
×	1	0	1	0	Enables Nonvolatile Controller*

× Don't Care

*Any other combination turns controller off

Figure 1


DS1234
+5V
V_{CCI}
14
V_{CCO}
1
V_{CC}
From Decoder
$\overline{CEI}$
3
$\overline{CEO}$
5
$\overline{CE}$
$\overline{CE}$
$\overline{WEI}$
4
$\overline{WEO}$
6
$\overline{WE}$
$\overline{WE}$
A_3
12
CMOS
RAM
A_2
11
$\overline{PF}$
8
To Write Protect
Other Memories
A_1
10
A_N
A_0
9
V_{BAT}
13
A_3
A_2
A_1
A_0
4
N
Address
Bus

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Power Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Input Low Voltage	V_{IL}	−0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	2
Supply Current @ $V_{CCO}=V_{CCI}-0.2$	I_{CCO}			80	mA	3
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Leakage	I_{LO}	−1.0		+1.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	4
Output Current @ 0.4V	I_{OL}			4.0	mA	4

(0°C to 70°C, $V_{CCI} < V_{BAT}$)

$\overline{CEO}$, $\overline{WEO}$ Output	V_{OHL}	$V_{BAT}-0.2$			V	6
Battery Current	I_{BAT}			0.1	uA	7
Battery Backup Current @$V_{CCO}=V_{BAT}-0.3V$	I_{CCO1}			100	uA	5

CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

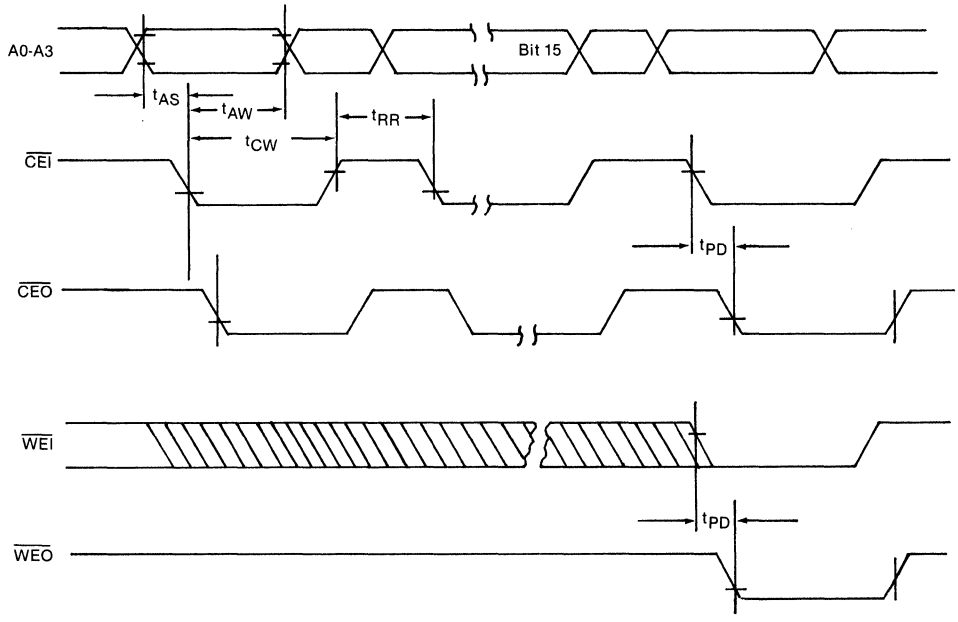
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
$\overline{CEI}$ Pulse Width	t_{CW}	110			ns	
Propagation Delay	t_{PD}			20	ns	

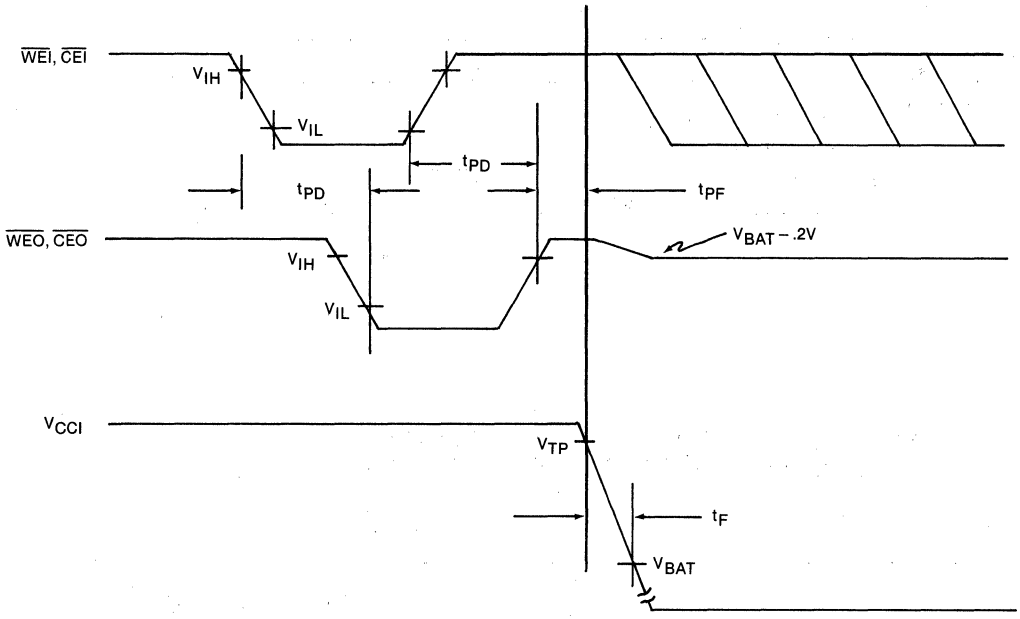
(0°C to 70°C, $V_{CCI} < V_{TP}$)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate Power Down	t_F	0			*us*	
V_{CC} Slew Rate Power Up	t_R	0			*us*	
$\overline{CEI}$ High to Power Fail	t_{PF}	0			ns	

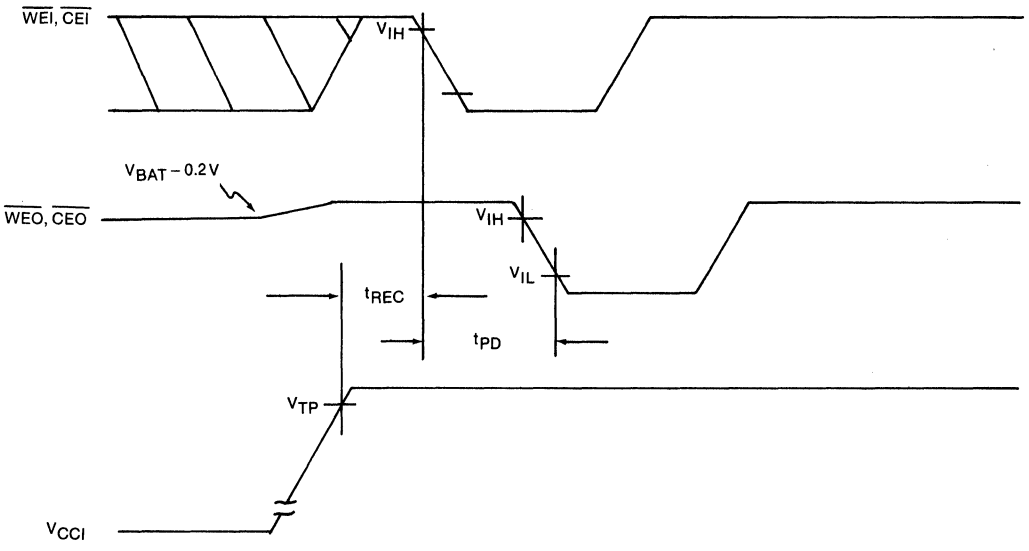
TIMING DIAGRAM—SWITCH SETTING



TIMING DIAGRAM—POWER DOWN



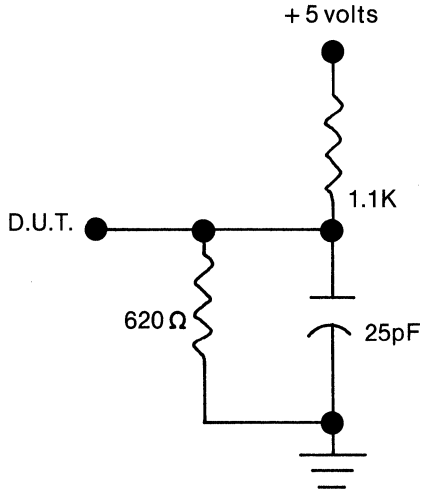
TIMING DIAGRAM—POWER UP



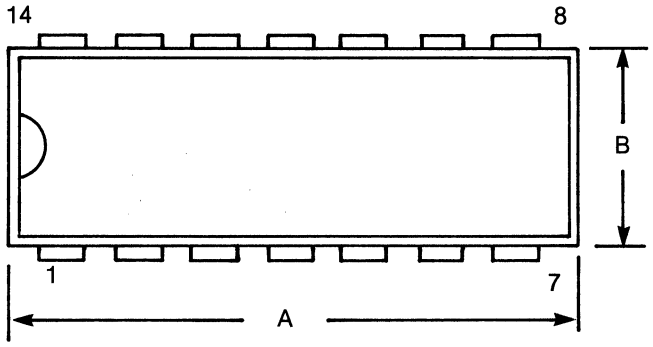
NOTES:

1. All voltages are referenced to ground.
2. Measured with V_{CCO}, $\overline{CE0}$ and $\overline{WE0}$ open.
3. I_{CCO} is the maximum average load which the DS1234 can supply to the memories.
4. Measured with a load as shown in Figure 2.
5. I_{CC01} is the maximum average load current which the DS1234 can supply to the memories in the battery back-up mode.
6. Chip Enable, $\overline{CEO}$, and Write Enable, $\overline{WEO}$, outputs can only sustain leakage current in the battery back-up mode.
7. I_{BAT} is the total load current which the DS1234 uses from the battery input pin with V_{CCO}, $\overline{CEO}$, and $\overline{WEO}$ open.

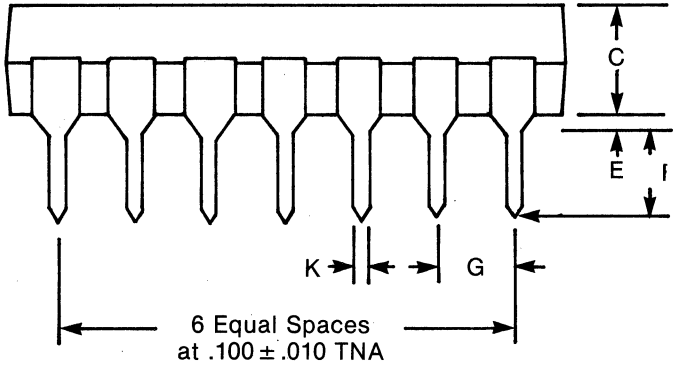
OUTPUT LOAD Figure 2

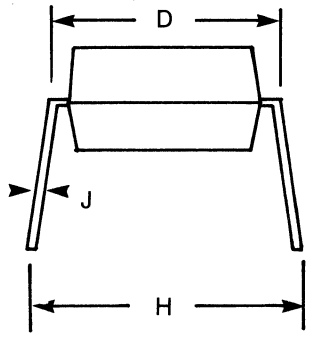


Conditional Nonvolatile Controller DS1234

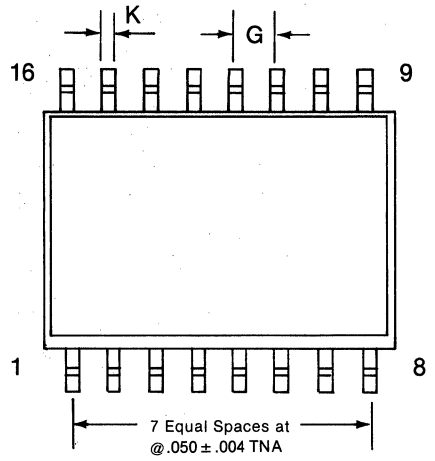


DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

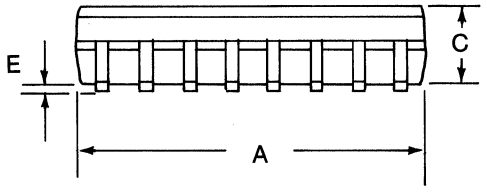


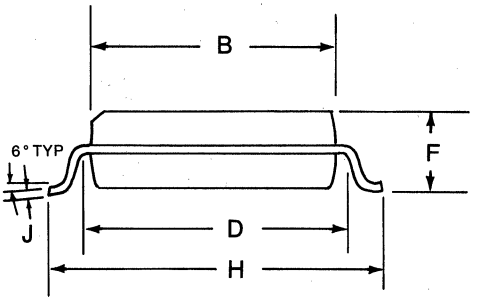


DS1234S
Conditional Nonvolatile Controller



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019





Dallas Semiconductor
DRAM Nonvolatizer

DS1237 16-Pin DIP
DS1237S 16-Pin SOIC

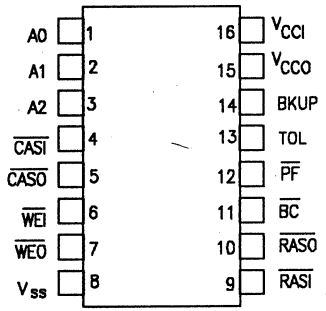
FEATURES

- Converts DRAM into nonvolatile RAM
- Controls any density of DRAM
- Wide backup supply voltage range
- Automatically refreshes when power fail detection occurs
- Power fail detection signal for hardwire interrupt
- Refresh is turned over to the processor after power up under software control
- Space saving 16-pin DIP and 16-pin SOIC for surface mounting
- Low power CMOS
- Built in backup condition circuit warns of impending backup supply failure
- Software controlled backup supply disconnect switch for storage and shipment
- Software controlled counter measures backup supply discharge and charging time
- Optional refresh periods of 7.5 ms, 15 ms, and 30 ms are available to support extended refreshing at reduced power levels

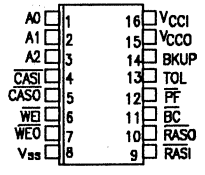
DESCRIPTION

The DS1237 is a CMOS circuit designed to control DRAMs such that information stored in memory is retained and protected during power failure. The DS1237 accomplishes this by monitoring the power supply for an out of tolerance condition. When such a condition occurs, the DRAM is isolated from the system control and the power supply for the DRAM is switched trom V_{CC} to the backup supply. Refresh control is maintained by the DS1237 until the power is within specifications. At this time refresh is returned to the system after a highly structured serial sequence on address lined A0, A1 and A2. Other serial sequences are used to set switches which control a counter used to measure backup supply charging and discharging and electrically connect or disconnect the backup supply.

PIN CONNECTIONS



16–PIN DIP



16–PIN SOIC

PIN NAMES

BKUP	- Backup Supply
$\overline{BC}$	- Backup Condition
TOL	- V_{CCI} Trip Point Select
$\overline{PF}$	- Power Fail Output
A0-A2	- Address Inputs
Vss	- Ground
$\overline{WEI}$	- Write Enable Input
$\overline{WEO}$	- Write Enable Output
$\overline{CASI}$	- $\overline{CAS}$ Input from System
CASO	- $\overline{CAS}$ Output to DRAM
$\overline{RASI}$	- $\overline{RAS}$ Input from System
$\overline{RASO}$	- $\overline{RAS}$ Output to DRAM
V_{CCO}	- V_{CC} Output to DRAM
V_{CCI}	- +5 Volt Input

OPERATION - NORMAL POWER CONDITIONS

Under normal operation system +5 volt power is supplied within the tolerance limits set by Pin 3 (TOL). If pin 3 is connected to V_{CCO}, the DS1237 will operate in the normal mode down to 4.75 volts. When Pin 3 is grounded, the DS1237 will operate in the normal mode down to 4.5 volts. During normal operation the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ inputs are directly rounted to the respective outputs with a maximum propagation delay of 15 ns. The backup supply input is normally connected to either a chargable capacitor or battery, however, any backup supply with a voltage input between the limits of 6.0 volts and 10 volts is suitable. The power fail output ($\overline{PF}$) is at high level and address inputs A0, A1, and A2 are monitored for software driven sequences. The backup condition output $\overline{BF}$ will be in an inactive (high) state provided that the backup input level is greater than 5.5 volts and the backup counter has not reached zero.

OPERATION - POWER LOSS AND DATA RETENTION

When the 5 volt V_{CC} power begins to drop, a precision band gap comparator senses this change. Depending on the level of the Tolerance Pin 3, a power fail signal will be generated as V_{CC} falls below 4.75 volts or 4.5 volts. The power fail output signal is driven low at this time and will stay low until V_{CC} is restored to normal conditions. When the data retention mode is turned on, the DS1237 isolates all control inputs and starts driving the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ outputs. The V_{CCI} input is disconnected from V_{CCO} and the regulated backup supply is connected. A burst $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is generated at a cycle time of 350 ns maximum. This burst refresh continues for 520 or 1032 consecutive cycles depending on the dash number of the device (see Table 1). After the burst refresh is complete, subsequent burst refreshing continues at 7.5, 15, or 30 ms intervals until V_{CCI} returns to normal levels and the system signals the DS1237 that it is ready to assume refresh duties. The $\overline{WE}$ output is held at the high (inactive) level from the time power fail is detected until the system assumes refresh duties.

OPERATION - RETURN TO NORMAL POWER CONDITIONS

When the system +5 volt supply returns and exceeds 4.5 volts or 4.75 volts depending on the tolerance pin, the V_{CCI} input is immediately reconnected to the V_{CCO} output pin while the regulated backup supply is internally disconnected from V_{CCO}. The DS1237 immediately generates a continuous $\overline{CAS}$ before $\overline{RAS}$ refresh at a cycle time of 350 ns maximum. Burst refreshing continues without interruption until the system signals that it is ready to assume the responsibility of refreshing the DRAMs. Refresh duties are shifted from the DS1237 to the system when a software controlled switch is set by sending a specific patern on address lines A0, A1, and A2 for 24 consecutive cycles. This address pattern which sets the software switch is shown in Figure 1. The address pattern is clocked into the DS1237 on the falling edge of $\overline{CAS}$ provided that setup and hold times are met. When the 24th cycle is correctly entered, the system will have full access to RAM and must handle refresh requirements. RAM read and write cycles can resume without restrictions after the software switch is correctly set.

CONSERVATION OF BACKUP SUPPLY

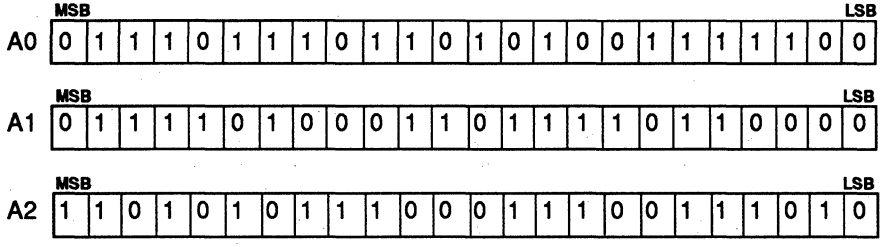
Another software controlled switch allows conservation of the backup supply when data retention is not requrired. The switch is controlled by the same method described for refresh except that the bit pattern is different. The bit patterns shown in Figure 2 turn on or off this switch which disconnects or connects the backup supply.

REFRESH INTERVALS Table 1

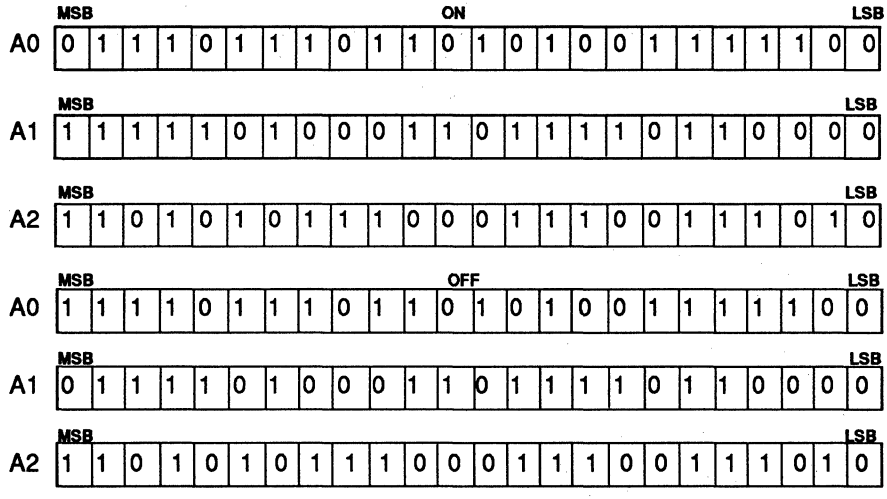
	REFRESH INTERVAL*		
NUMBER OF CYCLES	7.5	15	30
520	-1	-2	-3
1032	-4	-5	-6

*Refresh intervals have a tolerance of +/- 7%.

SOFTWARE SWITCH FOR PROCESSOR CONTROL ON POWER UP Figure 1



SOFTWARE CONTROLLED SWITCH FOR CONSERVATION OF BACKUP SUPPLY Figure 2



BATTERY CONDITION

The DS1237 contains two features which provide information about the condition of the backup supply. First, the DS1237 monitors the backup supply input condition. If this input is below V_{CCI}, the backup condition output pin ($\overline{BC}$) is driven to the active state (low) and will remain in this state until the backup suply voltage is restored to a level above V_{CCI}. This feature is active only while V_{CC} is applied within nominal limits. Whenever the backup supply is supplying power, the $\overline{BC}$ pin remains in a high impedance state. The second feature for monitoring the condition of the backup supply is a counter which is decremented on one second intervals whenever the backup supply is supplying power. This counter is set with a number while V_{CC} is within nominal limits. The value of the counter is entered by sending a 24-bit sequence on address lines A0, A1 and A2 in the same manner as described for refresh control. This sequence is shown in Figure 3. After the 24-bit sequence is correctly entered, the next 24 bits will define the time count in seconds which will start decrementing down when the backup supply is supplying power. This count is 24 bits long and is entered LSB first on address line A0 when $\overline{CAS}$ line goes low. The counter is a binary number representing the time allowed until the backup supply has been discharged. When the counter reaches zero, the $\overline{BC}$ pin will be low as soon as the V_{CC} supply is within nominal limits. The $\overline{BC}$ pin will remain low until a new value is entered into the counter. This time can be calculated by dividing the capacity in amper hours of the backup supply by the average load current of the DRAMs and converting this value into seconds. The value in the counter can be read at any time while V_{CC} is within nominal limits by sending the 24-bit sequence which is shown in Figure 4. This sequence is entered in the same manner as described for refresh control. After this sequence is correctly entered, the next 24 $\overline{CAS}$ cycles will cause the contents of the counter to be shifted out one bit at a time starting with the LSB on the $\overline{BC}$ pin. A logic zero on $\overline{BC}$ while $\overline{CAS}$ is low is a logic zero for that bit.

BACKUP CONDITION APPLICATIONS

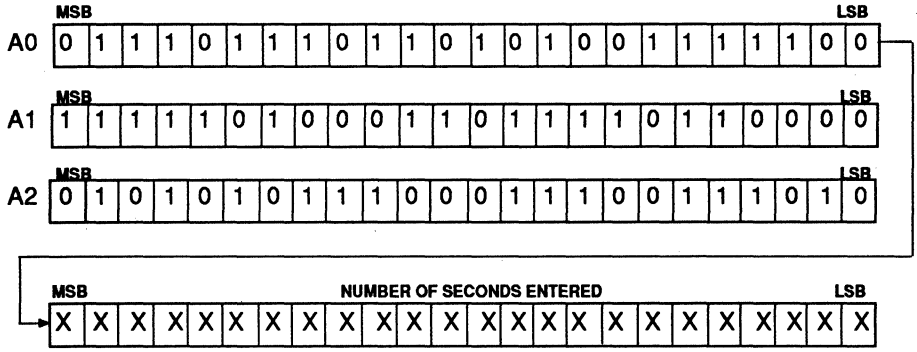
The backup condition features of the DS1237 can supply the system valuable information about the backup supply. A simple application may only use the V_{CC} comparator to tell the system that a battery is weak and should be replaced. A more sophisticated system may use the backup condition counter to measure the time that a primary battery is used to supply power to DRAMs. By knowing the capacity of the battery and the requirements of the DRAM, the time for battery replacement can be predicted. In fact, if worst case primary supply outages can be estimated, the backup battery can be selected so that replacement can always occur prior to backup supply failure. If a rechargable backup supply is used, such as a capacitor or a nicad battery, the backup condition counter can be used to measure both the charge and discharge time. Charge time can be measured by using a system time base and periodically adjusting the battery condition counter under software control to reflect the amount of time (amount of charge) that the system primary power is within nominal limits.

NOTE:

The DS1237 requires capacitive bypassing techniques between V_{CCO} and GND for proper operation. A bypass capacitor between V_{CCO} and BKUP is also essential for proper operation. While applications vary, a 10 uf capacitor value is typically required.

SOFTWARE SEQUENCE FOR SETTING THE BACKUP CONDITION COUNTER

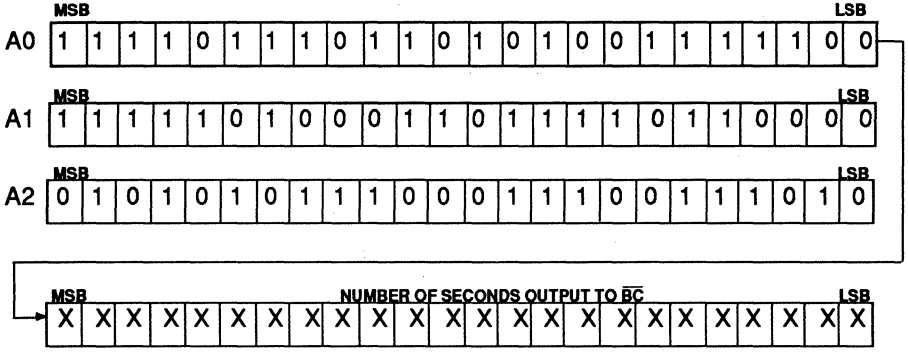
Figure 3



NOTE:
The binary count which is entered into the backup condition counter is a calculated value based on application and has a range of 2^{24} seconds with an accuracy of +/- 20%.

SOFTWARE SEQUENCE FOR READING THE BACKUP CONDITION COUNTER

Figure 4



ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON BATTERY INPUT PINS RELATIVE TO GROUND	-0.3V to +12V
VOLTAGE ON ANY OTHER PIN RELATIVE TO GROUND	-0.3V to +7V
OPERATING TEMPERATURE	0°C to +70°C
STORAGE TEMPERATURE	-55°C to +125°C
SOLDERING TEMPERATURE	260°C for 10 seconds

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	VOLTS	1
Voltage Input Logic 1	V_{IH}	2.0		V_{CC}+0.3V	VOLTS	1
Voltage Input Logic 0	V_{IL}	-0.3		+0.8	VOLTS	1
Backup Supply	BKUP	5.5V	8.0V	10.0	VOLTS	2,3

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.75V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-2.0			mA	1.5
Output Current @ 0.4 V	I_{OL}			+8.0	mA	1.5
Input Supply Current	I_{CCI}		3	7	mA	6
Output Supply Current V_{CCO}=V_{CCI} -0.2 V	I_{CCO}			200	mA	4
$\overline{PF}$ Detect TOL = V_{CCO}	V_{TP}	4.5	4.62	4.75	V	7
$\overline{PF}$ Detect TOL = GND	V_{TP}	4.25	4.37	4.5	V	7
Output Supply Current V_{CCI} < V_{TP}	I_{CCOB}			30	mA	8
Backup Supply Leakage	I_{BKUP}			1	uA	9

CAPACITANCE

PARAMETER	SYMBOL	COND.	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	t_A=25°C	5	7		pF

A.C.ELECTRICAL CHARACTERISTICS - RAPID REFRESH

(0°to 70°C $V_{CCI} < V_{TP}$)

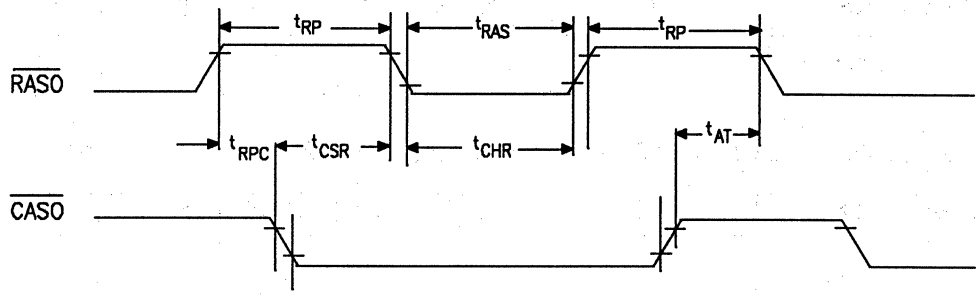
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{RAS}$ Precharge Time	t_{RP}	90		150	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	60		100	ns	
$\overline{CAS}$ Set Up Time	t_{CSR}	30		50	ns	
$\overline{CAS}$ Hold Time	t_{CHR}	60		100	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120		200	ns	
Elapsed Time Between Rapid Refresh Burst	t_{AT}	SEE TABLE 1			ns	

A.C. ELECTRICAL CHARACTERISTICS

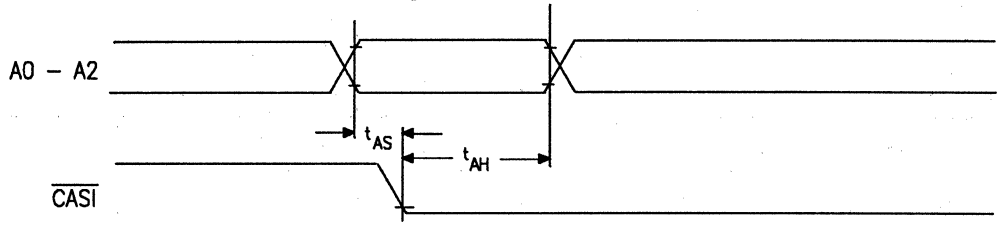
(0°C to 70°C $V_{CCI} > V_{TP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Set Up Time	t_{AS}	0			ns	
Address Hold Time	t_{AH}	20			ns	
Propagation Delay	t_{PD}		7	15	ns	

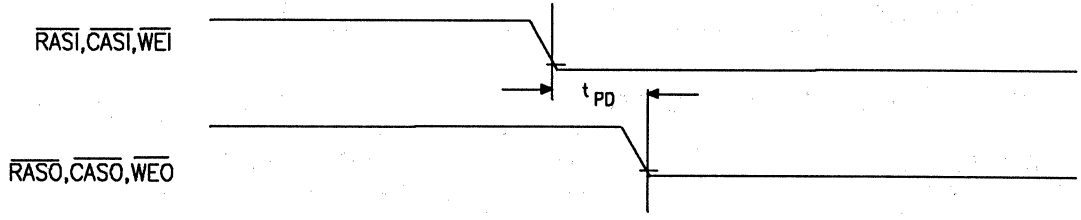
REFRESH CYCLE DURING BURST REFRESH RETENTION (WEO=V_{IH}) Figure 5



SOFTWARE SEQUENCE ENTRY Figure 6



PROPAGATION DELAY - NORMAL OPERATION Figure 7

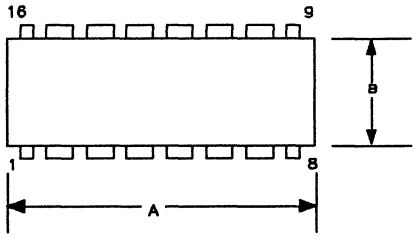


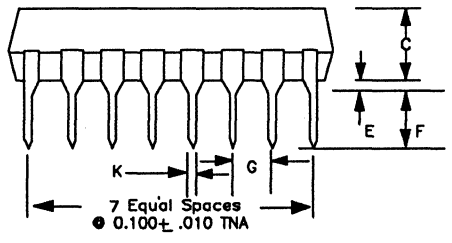
NOTES

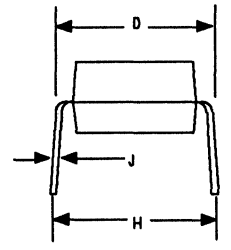
1. All voltages are referenced to ground.
2. The BC pin will be driven active whenever V_{CC} is within nominal limits and the backup supply is below V_{CC}.
3. Backup input voltage is internally regulated within the DS1237 such that V_{CCO} is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
4. I_{CCO} is the maximum current which the DS1237 can supply to RAM through the V_{CCO} pin with a voltage drop of less than 0.2 volts.
5. Load capacity is 300 pF.
6. Measured with all outputs open.
7. V_{TP} is the trip point where the internal switching circuits disconnects V_{CCI} and connects the internally regulated backup supply to V_{CCO}. Rapid refresh is also initiated at this time, and the $\overline{PF}$ output is driven active.
8. I_{CCOB} is the maximum current which the DS1237 can supply to RAM through the V_{CCO} pin from the internally regulated supply while in the data retention mode.
9. Backup leakage is the internal current consumed by the DS1237 in the data retention mode.

DS1237
DRAM NONVOLATIZER
16-PIN DIP

DIM	INCHES	
	MIN.	MAX.
A	0.740	0.780
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021

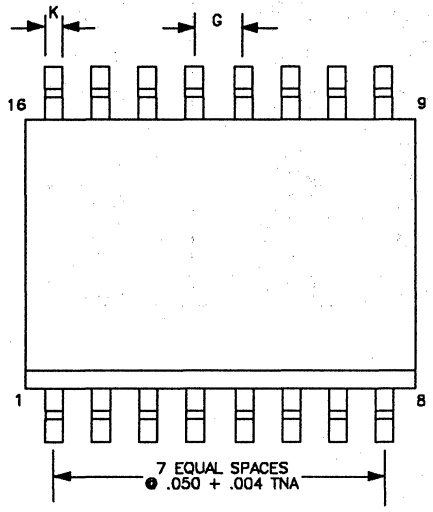


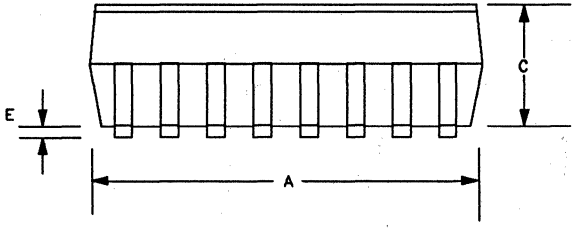


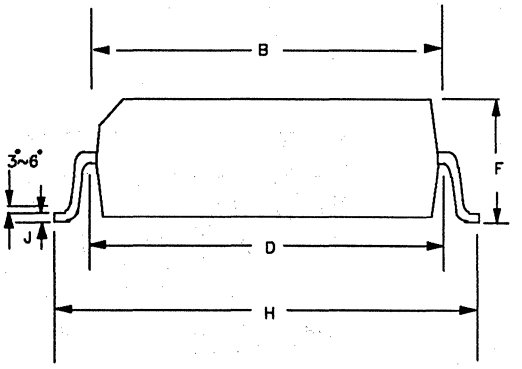


DS1237S
DRAM NONVOLATIZER
16-PIN SOIC

DIM	INCHES	
	MIN.	MAX.
A	0.403	0.411
B	0.290	0.296
C	0.089	0.095
D	0.325	0.330
E	0.008	0.012
F	0.097	0.105
G	0.046	0.054
H	0.402	0.410
J	0.006	0.011
K	0.013	0.019







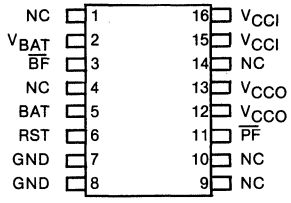
Dallas Semiconductor
Battery Manager

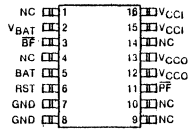
DS1259—16-Pin DIP
DS1259S—16-Pin SOIC

FEATURES

- Facilitates uninterruptable power
- Uses battery only when primary V_{CC} is not available
- Low forward voltage drop
- Power fail signal interrupts processor or write protects memory
- Consumes less than 100 nA of battery current
- Low battery warning signal
- Battery can be electrically disconnected upon command
- Battery will automatically reconnect when V_{CC} is applied
- Mates directly with DS1212 Controller to back up 16 RAMs
- Optional 16-pin SOIC surface mount package

PIN CONNECTIONS





PIN NAMES

NC	-	No Connection
V_{BAT}	-	Battery Input Connection
$\overline{BF}$	-	Battery Fail Output Signal
BAT	-	Battery Output
RST	-	Reset Ground Signal
GND	-	Ground
$\overline{PF}$	-	Power Fail Output Signal
V_{CCO}	-	RAM Supply
V_{CCI}	-	+5 V Supply

1

DESCRIPTION

The DS1259 is a low-cost battery management system for portable and nonvolatile electronic equipment. A battery connected to the battery input pin supplies power to CMOS electronic circuits when primary power is lost through an efficient switch via the V_{CCO} pins. When power is supplied from the battery, the power fail signal is active to warn electronic reset circuits of the power status. Energy loss during shipping and handling is avoided by pulsing reset, thereby causing the battery to be isolated from other elements in the circuits.

OPERATION

During normal operation, V_{CCI} (Pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (Pins 12 and 13) through an internal switch at a voltage level of $V_{CCI} - 0.2$ volts@250 mA. During this time the power fail signal ($\overline{PF}$) is held high indicating valid V_{CCI} voltage (see Figure 1). However, if the V_{CCI} would fall below the trip point (V_{TP}), a level of 1.26 times the battery level (V_{BAT}), the power fail signal is driven low. As V_{CCI} falls below the battery level, power is switched from V_{CCI} to V_{BAT} and the battery supplies power to the uninterruptable output (V_{CCO}) at $V_{BAT} - 0.2$ volts@15 mA.

On power up, as the V_{CCI} supply rises above the battery, the primary energy source, V_{CCI}, becomes the supply. As V_{CCI} rises above the trip point (V_{TP}), the power fail signal is driven back to the high level. During normal operation BAT (Pin 5) stays at the battery level regardless of the level of V_{CCI}.

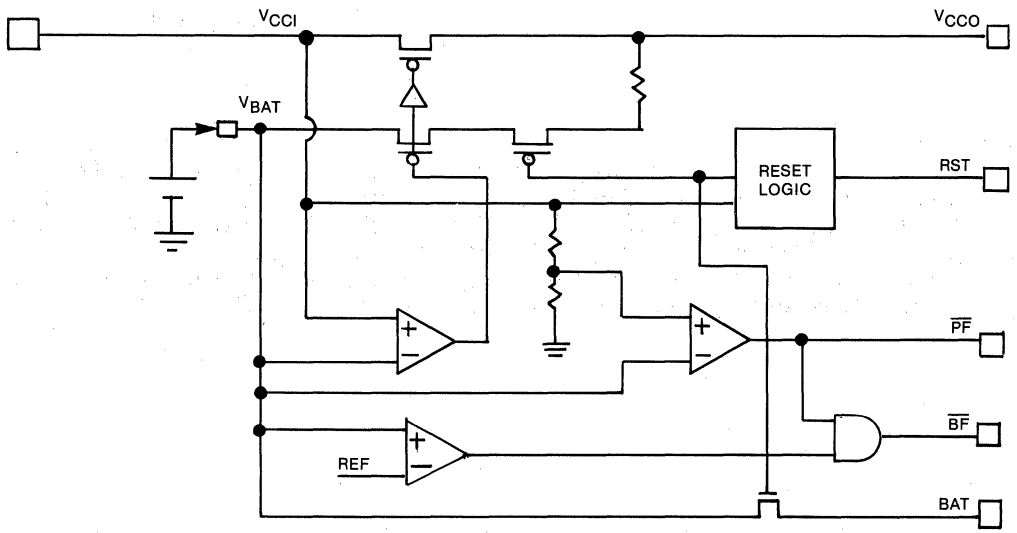
BATTERY FAIL

When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level provided that the attached battery (V_{BAT}) is greater than 2 volts. If the battery level should decrease to below 2 volts, the $\overline{BF}$ signal is driven low indicating a low battery. The $\overline{BF}$ signal is always low when the $\overline{PF}$ signal is low.

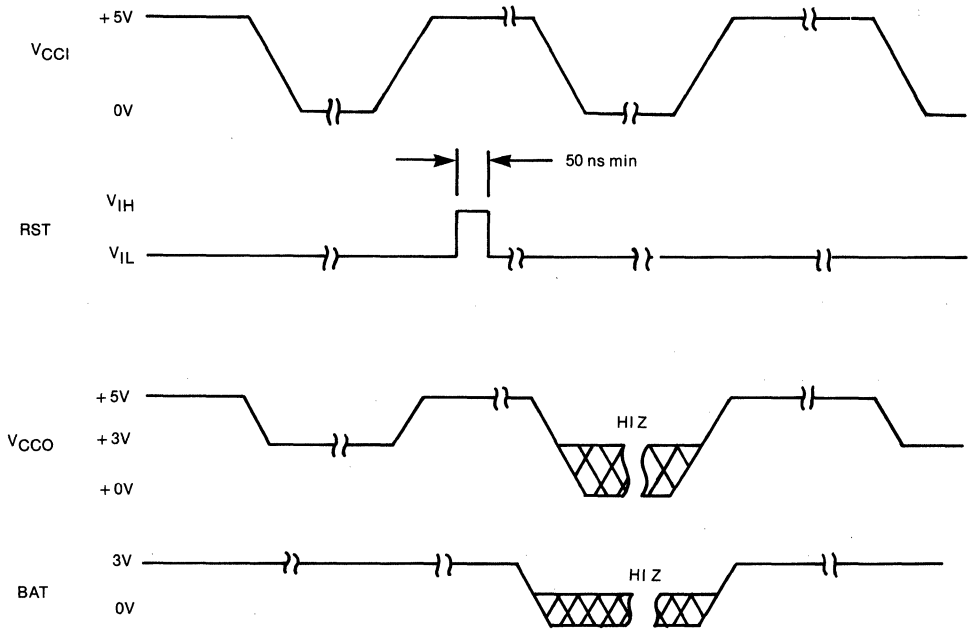
RESET

The reset input can be used to prevent the battery from supplying power to V_{CCO} and BAT even if V_{CCI} falls below the level of the battery. This feature is activated by applying a pulsed input on $\overline{RST}$ to high level for 50 ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to the high impedance. The next time primary power is applied such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the battery or V_{CCI}. The BAT output will also return to the level of the battery. Figure 3 shows the DS1259 in a typical application.

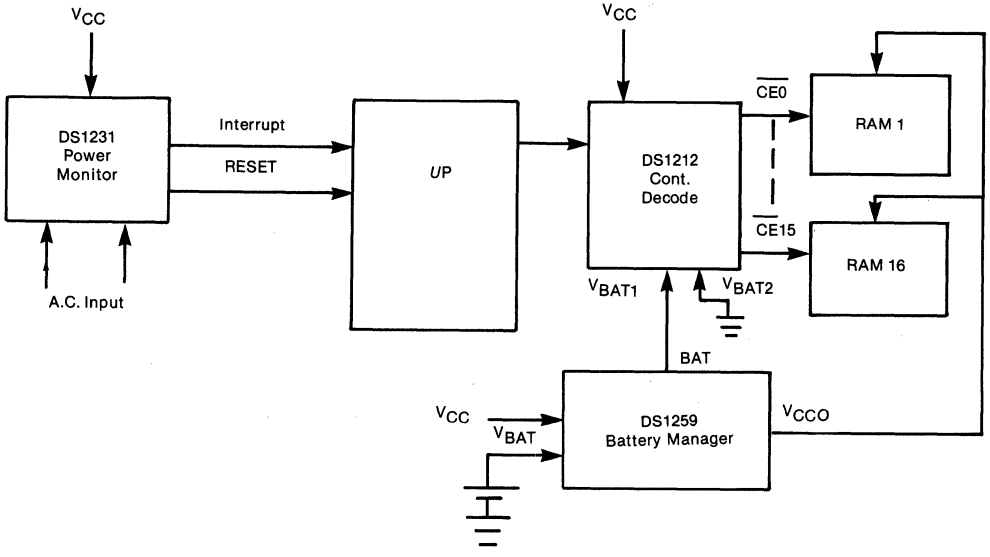
BLOCK DIAGRAM Figure 1



RESET TIMING Figure 2



TYPICAL APPLICATION Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}		5.0	5.5	V	1
Input High Voltage	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Input Low Voltage	V_{IL}	−0.3		+0.8	V	1
Battery Voltage Pin 2	V_{BAT}	2.5	3	3.7	V	6
Battery Output Pin 5	BAT	$V_{BAT}-0.1$			V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_{LO}	−1.0		+1.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	1,2
Output Current @0.4V	I_{OL}			+4.0	mA	1,2
Input Supply Current	I_{CCI}			10	mA	3
Pins 12, 13 $V_{CCO} = V_{CCI}-0.2$	I_{CCO}			250	mA	
Pin 11 $\overline{PF}$ Detect	V_{TP}		$1.26 \times V_{BAT}$		V	4,6
Pin 3 $\overline{BF}$ Detect	V_{BATF}		2.0		V	7

(0 °C to 70 °C, $V_{CCI} < V_{BAT}$)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Pins 12, 13 $V_{CCO} = V_{BAT} - 0.2V$	I_{CCO2}		15	mA	5
Battery Leakage	I_{BAT}		100	nA	8
Pin 5 Battery Output Current	$I_{BAT\ OUT}$		100	*u*A	

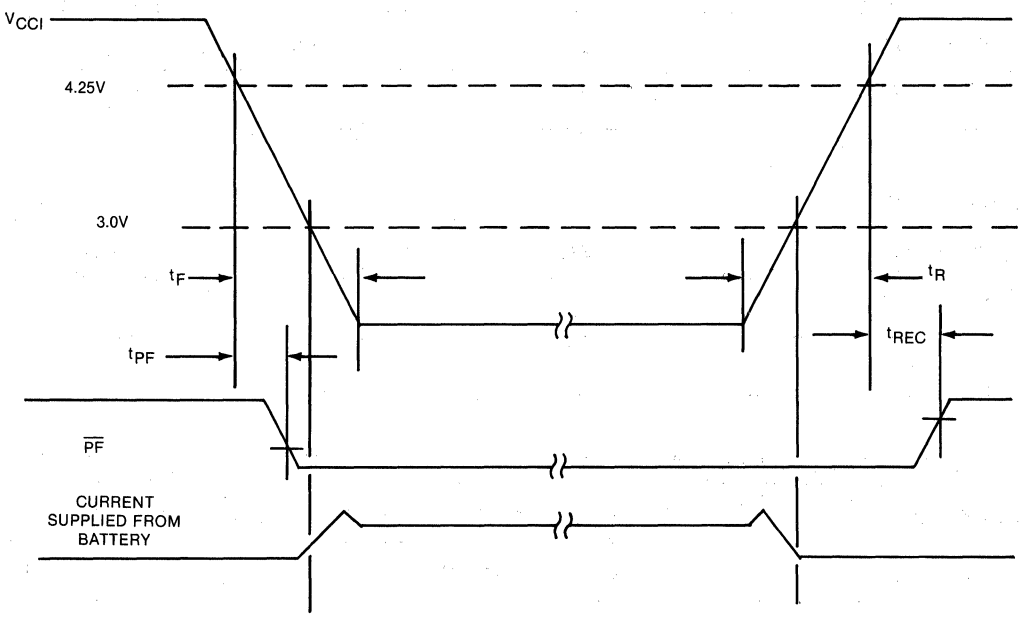
CAPACITANCE ($t_A = 25$ °C)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C_{IN}	5	10	pF
Output Capacitance	C_{OUT}	5	10	pF

A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 4.0$ to 5.5V)

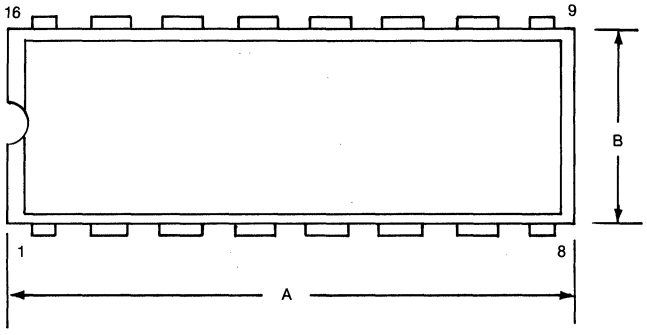
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			*u*s	
V_{CCI} Slew Rate	t_R	1			*u*s	
Power Down to $\overline{PF}$ Low	t_{PF}	0			*u*s	
$\overline{PF}$ High after Power Up	t_{REC}			100	*u*s	

POWER-DOWN/POWER-UP CONDITION

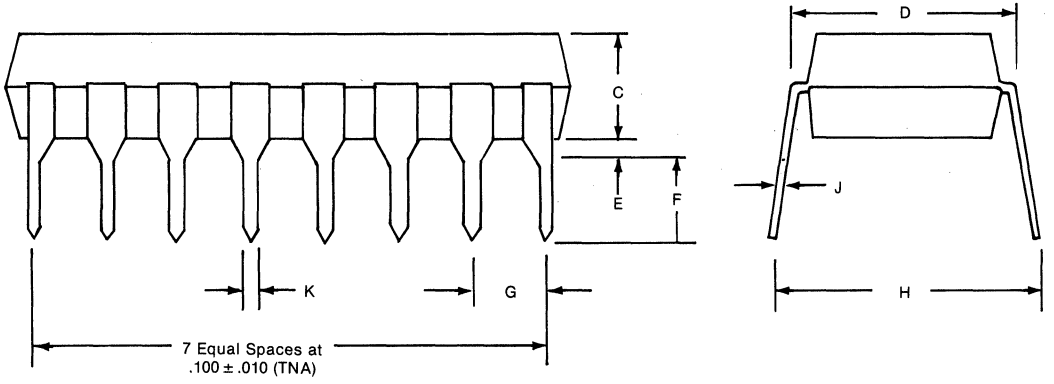


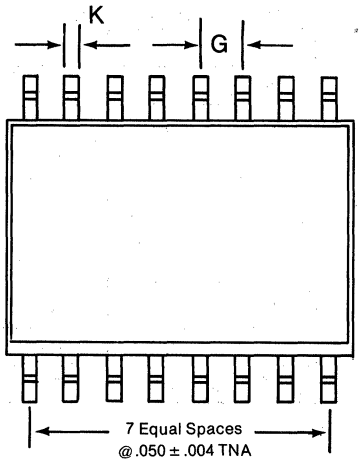
NOTES:

1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13 and 3 open.
4. V_{TP} is the point that $\overline{PF}$ is driven low.
5. I_{CCO2} may be limited by the capability of the battery.
6. Trip Point Voltage for Power Fail Detect:
   $V_{TP} = 1.26 \times V_{BAT}$
   For 5% operation: $V_{BAT} = 3.7V$ Max.
7. V_{BATF} is the point that $\overline{BF}$ is driven low.
8. Battery leakage is the internal energy consumed by the DS1259.

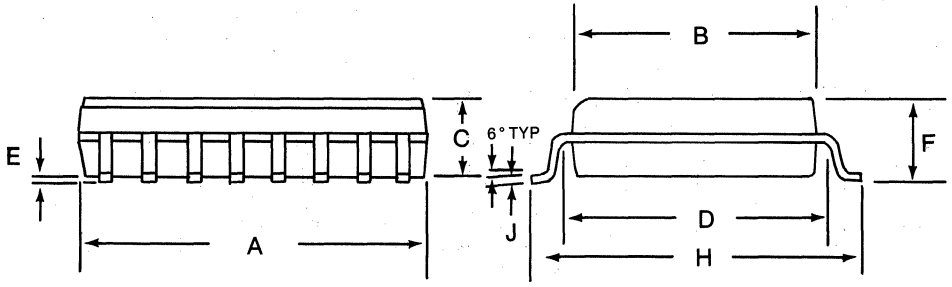


DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021





DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



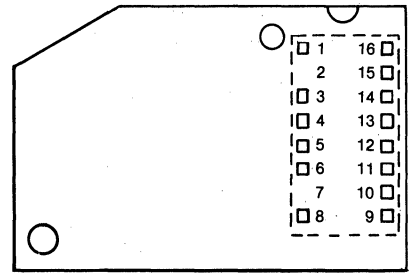
Dallas Semiconductor
SmartBattery

DS1260-25
-50
-100

FEATURES

- Encapsulated lithium energy cell with shelf life beyond 10 years
- Available with energy capacities of 250, 500, and 1,000 MAH @ 3 volts
- Plugs into a standard 16 pin DIP socket
- Lithium cell electrically disconnects from exposed pins upon command
- Battery isolation insures full capacity after shipping and handling
- Lithium cell automatically reconnects when V_{CC} is applied
- Recessed pins prevent bending
- V_{CC} fail signal interrupts processor or write protects memory
- Exhausted energy cell warning signal
- Low profile permits mounting on 0.5 inch printed circuit board centers
- Mates directly with DS1212 controller to back-up 16 SRAMs
- Uninterruptable supply for CMOS and portable devices

PIN CONNECTIONS



PIN NAMES

Pins, 1, 4, 9, 10 and 14 are No-Connects
Pin 2 and pin 7 are missing
Pin 3 is Battery Fail ($\overline{BF}$)
Pin 5 is Battery Out (BAT)
Pin 6 is RESET (RST)
Pin 8 is Ground
Pin 11 is Power Fail ($\overline{PF}$)
Pins 12 and 13 are RAM Supply (V_{CCO})
Pins 15 and 16 are +5V Supply (V_{CCI})

DESCRIPTION

The DS1260 is a low cost backup energy source for portable and nonvolatile electronic equipment. A lithium energy source of up to 1 amp hour can supply power to CMOS electronic circuits when primary power is lost through an intelligent and efficient switch. When power is supplied from the lithium power source, the power fail signal is held low to warn electronic RESET circuits of the power status. Energy loss during shipping and handling is avoided by pulsing RESET, thereby causing the backup energy source to be isolated from the exposed pins. The DS1260 can be plugged into a standard 16-pin low-cost DIP socket, allowing for proven interconnect and simple replacement if the energy has been exhausted.

OPERATION

During normal operation V_{CCI} (Pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (Pins 12 and 13) through an internal switch at a voltage level of $V_{CCI} - 0.2$ volts @ 250 ma. During this time the power fail signal $\overline{PF}$ is held high indicating valid primary voltage (see Figure 1). However, if the V_{CCI} would fall below the level of 4.25 volts, the power fail signal is driven low. As V_{CCI} falls below the level of the lithium supply ($V_{BAT} = 3$ volts) power is switched and the lithium energy source supplies power to the uninterruptable output (V_{CCO}) at $V_{BAT} - 0.2$ volts @ 5 MA.

On power up, as the V_{CCI} supply rises above 3 volts, the primary energy source, V_{CCI}, becomes the supply. As the V_{CCI} input rises above 4.25 volts the power fail signal is driven back to the high level. During normal operation BAT (Pin 5) stays at the battery level of 3 volts, regardless of the level of V_{CCI}.

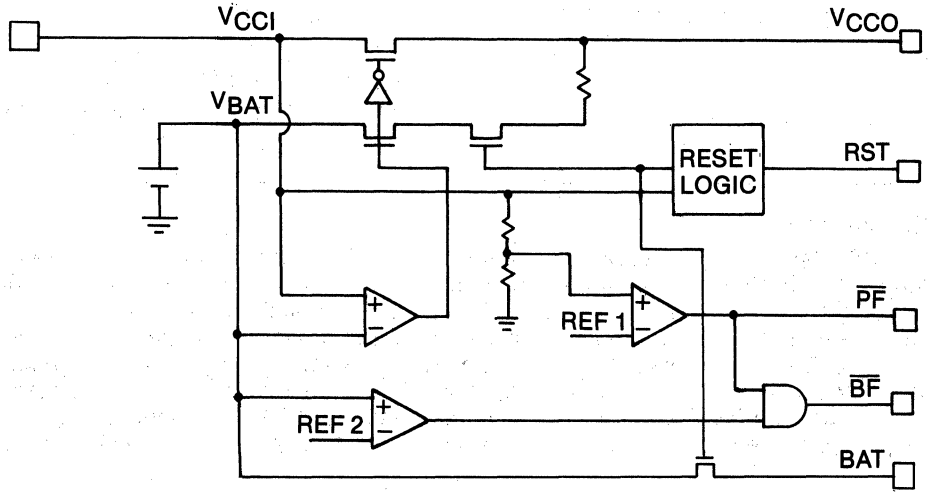
BATTERY FAIL

When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level (V_{OH}) provided that the lithium energy source is greater than 2 volts. If the lithium energy source should decrease to below 2 volts, the $\overline{BF}$ signal is driven low (V_{OL}), indicating an exhausted lithium battery. The $\overline{BF}$ signal is always low when power is being supplied by the lithium energy source.

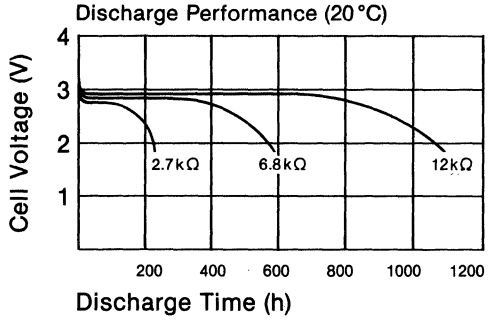
RESET

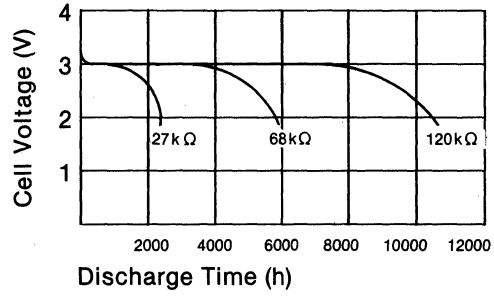
The reset input can be used to prevent the lithium energy source from supplying power to V_{CCO} and BAT even if V_{CCI} falls below 3 volts. This feature is activated by applying a pulsed input on RST to high level (V_{IH}) for 50 ns min. while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to high impedance. The next time primary power is applied, such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the lithium energy source when V_{CCI} again falls below 3 volts. BAT will also return to the level V_{BAT}. Figure 3 shows how the SmartBattery is used in a system application.

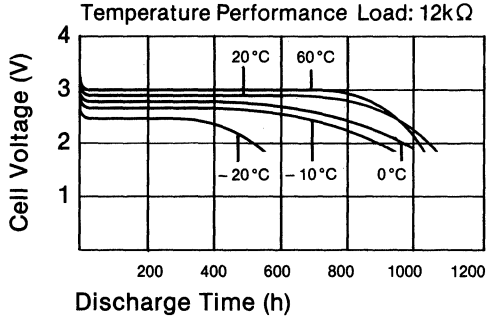
BLOCK DIAGRAM Figure 1

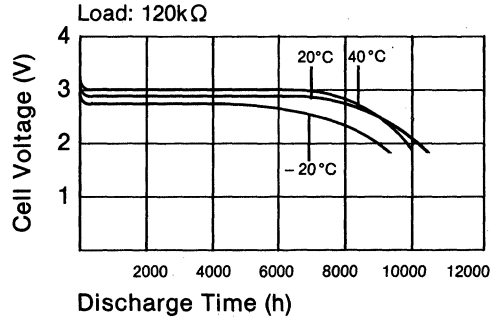


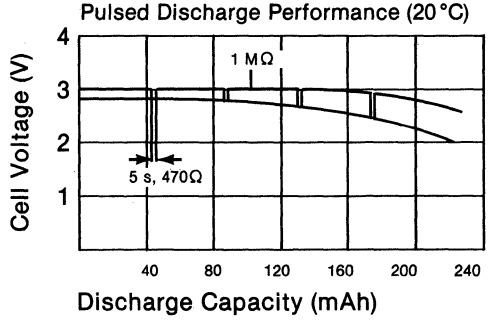
BATTERY PERFORMANCE DS1260-25



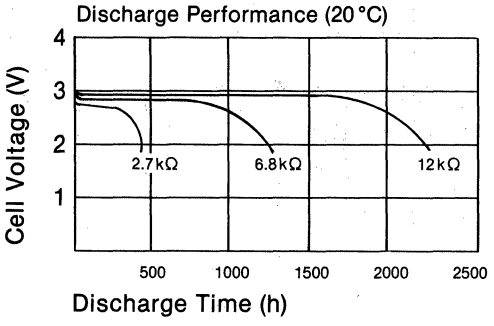


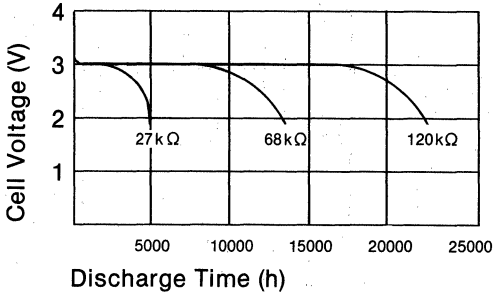


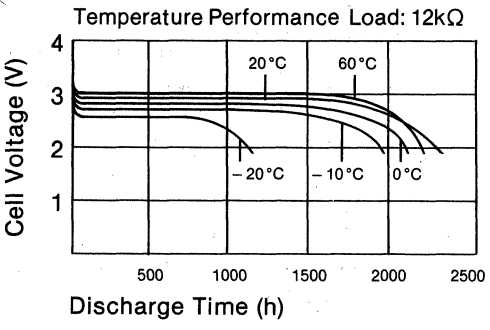


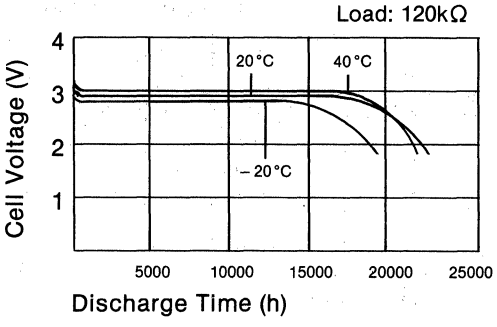


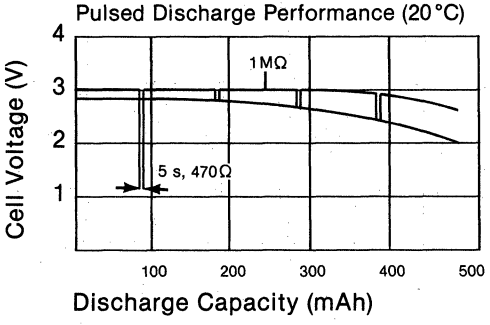
BATTERY PERFORMANCE DS1260-50





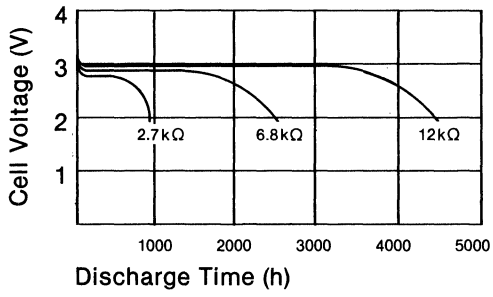


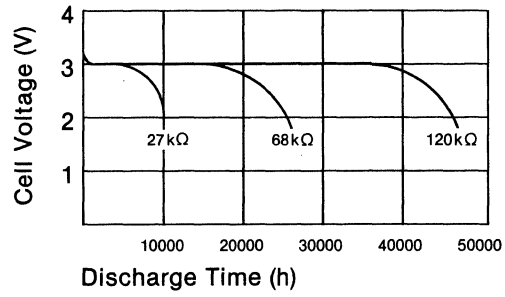




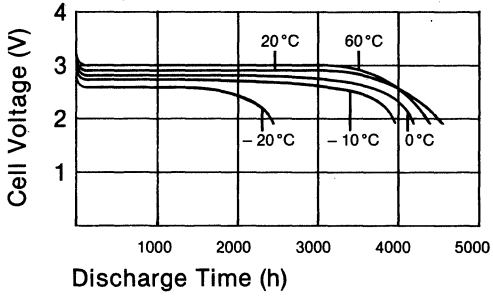
BATTERY PERFORMANCE DS1260-100

Discharge Performance (20 °C)

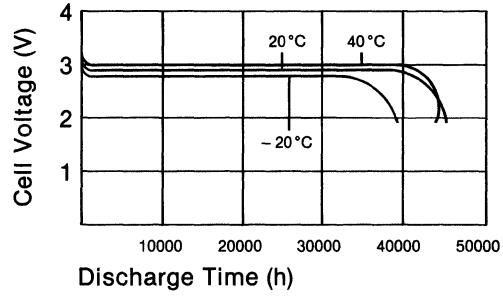




Temperature Performance Load: 12kΩ



Load: 120kΩ



Pulsed Discharge Performance (20 °C)

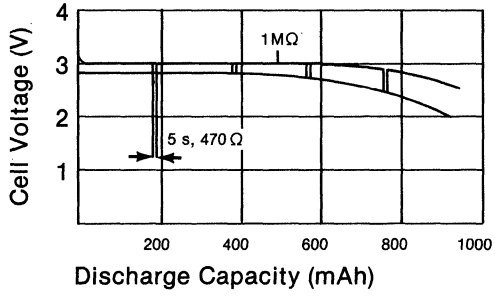
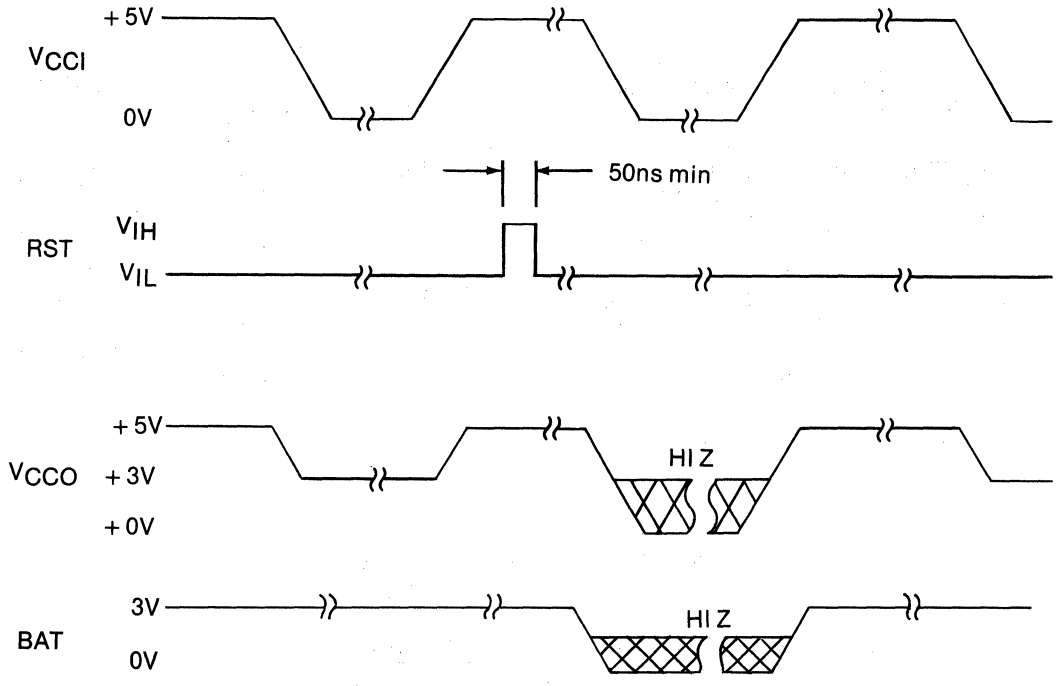


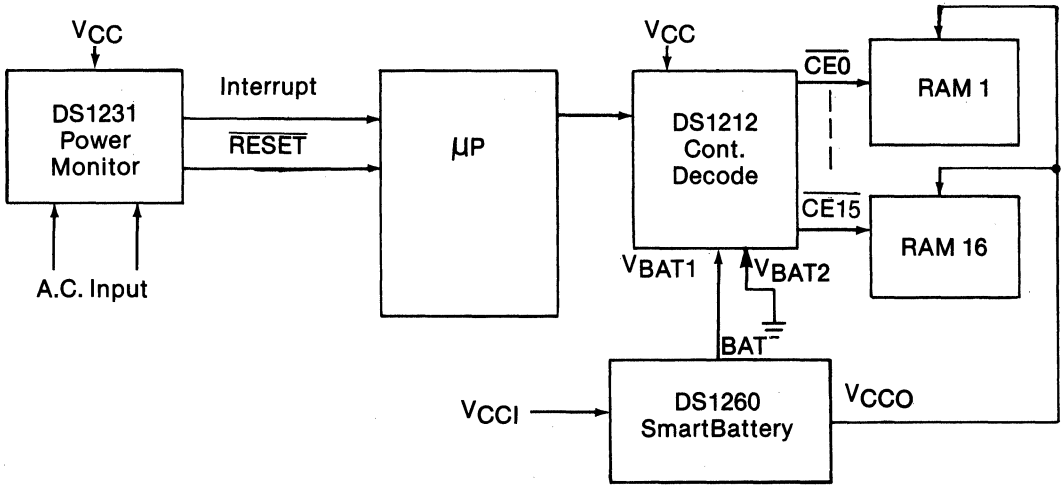
TABLE I

PART NO.	CAPACITY	NOMINAL VOLTAGE
DS1260-25	250 MAH	3 volts
DS1260-50	480 MAH	3 volts
DS1260-100	960 MAH	3 volts

FIGURE 2



INTEGRATED BATTERY BACKUP—APPLICATIONS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Primary Power Supply	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.0		$V_{CCI}+0.3$	V	1
Input Low Voltage	V_{IL}	−0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CCI} = 4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Leakage Current	I_{LO}	−1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	−1.0			mA	1,2
Output Current @ 0.4V	I_{OL}			+4.0	mA	1,2
Input Supply Current	I_{CCI}			5	mA	3
Pins 12,13 $V_{CCO} = V_{CCI} - 0.2$	I_{CCO}			250	mA	
Pin 11 $\overline{PF}$ Detect	V_{TP}		4.25	4.5	V	4
Pin 3 $\overline{BF}$ Detect	V_{BATF}		2.0		V	7

(0°C to 70°C, $V_{CCI} < V_{BAT}$)

Battery Voltage Pin 5	V_{BAT}		3		V	6
Pins 12, 13 $V_{CCO} = V_{BAT} - 0.2V$	I_{CCO2}			15	mA	5
Battery Leakage	I_{BAT}			100	nA	8,9
Pin 5 Battery Output Current	$I_{BAT\ OUT}$			100	uA	

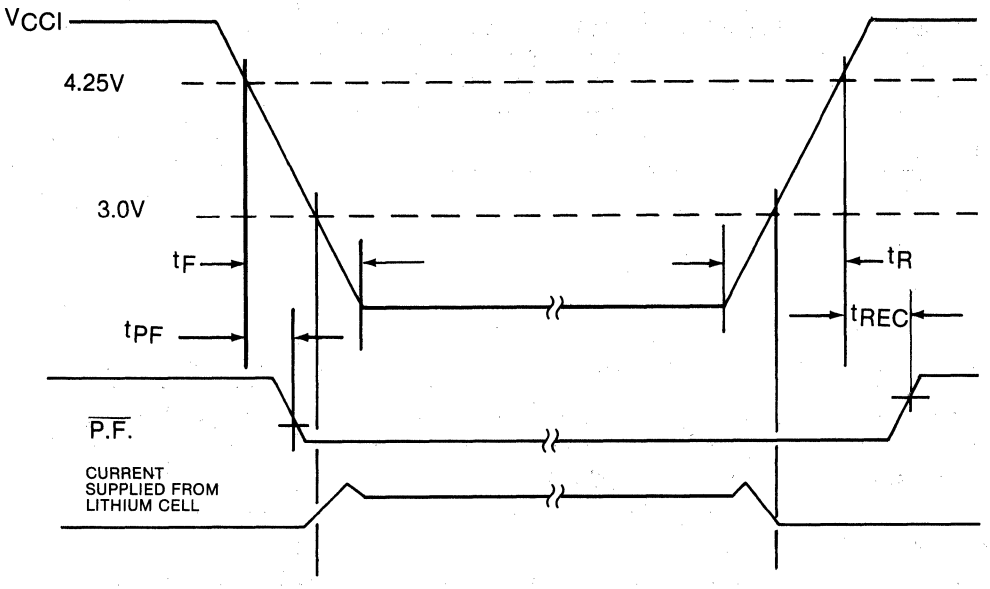
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Output Capacitance	C_O	5	10	pF
Input Capacitance	C_I	5	10	pF

A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			µs	
V_{CCI} Slew Rate	t_R	1			µs	
Power Down to $\overline{PF}$ Low	t_{PF}	0			µs	
$\overline{PF}$ High after Power Up	t_{REC}			100	µs	

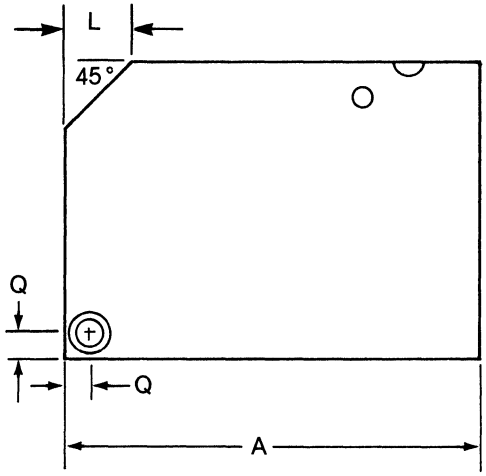
POWER-DOWN/POWER-UP CONDITION



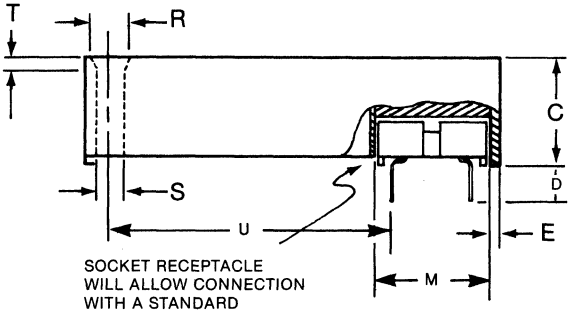
NOTES:

1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13 and 3 open.
4. V_{TP} is the point that $\overline{PF}$ is driven low.
5. Sustained I_{CCO2} currents above 1 mA cause a significant drop in battery voltage.
6. V_{BAT} is the internal lithium energy source voltage.
7. V_{BATF} is the point that $\overline{BF}$ is driven low.
8. Battery leakage is the internal energy consumed by the DS1260.
9. Storage loss is less than 1% per year at 25°C.
10. V_{CCI} = +5 volts; t_A = 25°C.

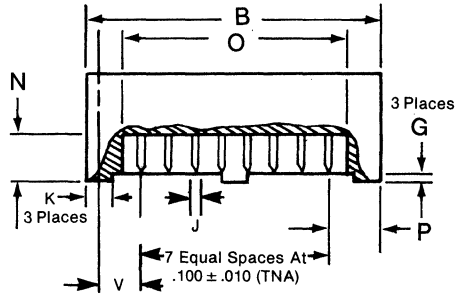
DS1260 - 25
- 50
- 100
SmartBattery



DIM.	INCHES	
	MIN.	MAX.
A	1.480	1.500
B	1.030	1.050
C	.390	.415
D	.120	.140
E	.020	.040
G	.020	.040
J	.022	.026
K	.090	.110
L	.240	.260
M	.420	.440
N	.165	.175
O	.800	.810
P	.160	.180
Q	.098	.109
R	.165	.175
S	.115	.125
T	.052	.058
U	.980	1.000
V	.055	.075



SOCKET RECEPTACLE
WILL ALLOW CONNECTION
WITH A STANDARD
16 DIP SOCKET.
BURNDY DILB16P.-11T
SUPPLIED WITH EACH ORDER.



SOCKET NOT SHOWN

1

System Extension

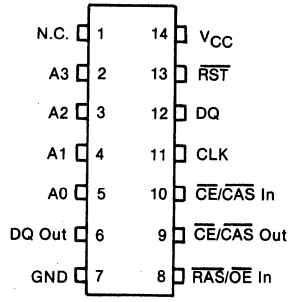
Dallas Semiconductor
Phantom Interface

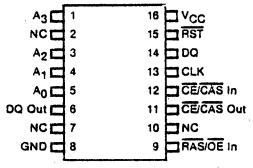
DS1206—14-Pin DIP
DS1206S—16-Pin SOIC

FEATURES

- Minimum expense add-on serial port
- Converts standard bytewide or DRAM memory wave forms into a three wire serial port
- Operation is transparent to memory
- Software generated memory cycles activate serial port and transfer data
- High band width—1bit data transfer per 2 memory cycles
- Intercepts memory signals so that pass through connections can be maintained to memory
- Controls communications for as many as ten DS1201 Tags, DS1204U Keys, DS1207 TimeKeys or DS1290 Eliminators
- Low power CMOS circuitry
- Optional 16-pin SOIC surface mount package

PIN CONNECTIONS





PIN NAMES

N.C.	- No connection
A0-A3	- Memory address bus
DQ Out	- Data out to memory bus
GND	- Ground
$\overline{RAS}/\overline{OE}$ In	- $\overline{RAS}$ Input from memory bus
$\overline{CE}/\overline{CAS}$ Out	- Chip enable or $\overline{CAS}$ to memory
$\overline{CE}/\overline{CAS}$ In	- Chip enable or $\overline{CAS}$ from memory bus
CLK	- Clock for serial port
DQ	- Data I/O for serial port
$\overline{RST}$	- Reset for serial port
V_{CC}	- +5 Volts

DESCRIPTION

The Phantom Interface is a CMOS circuit which intercepts the standardized memory bus found in computer systems and adapts the bus to a three wire serial port. Multiple memory cycles are used as a basis for generating the appropriate signals to control the serial port. In this way, a sequence of software generated memory cycles encode commands and transfer data with low pin count. The serial port signaling is derived from the memory address bus

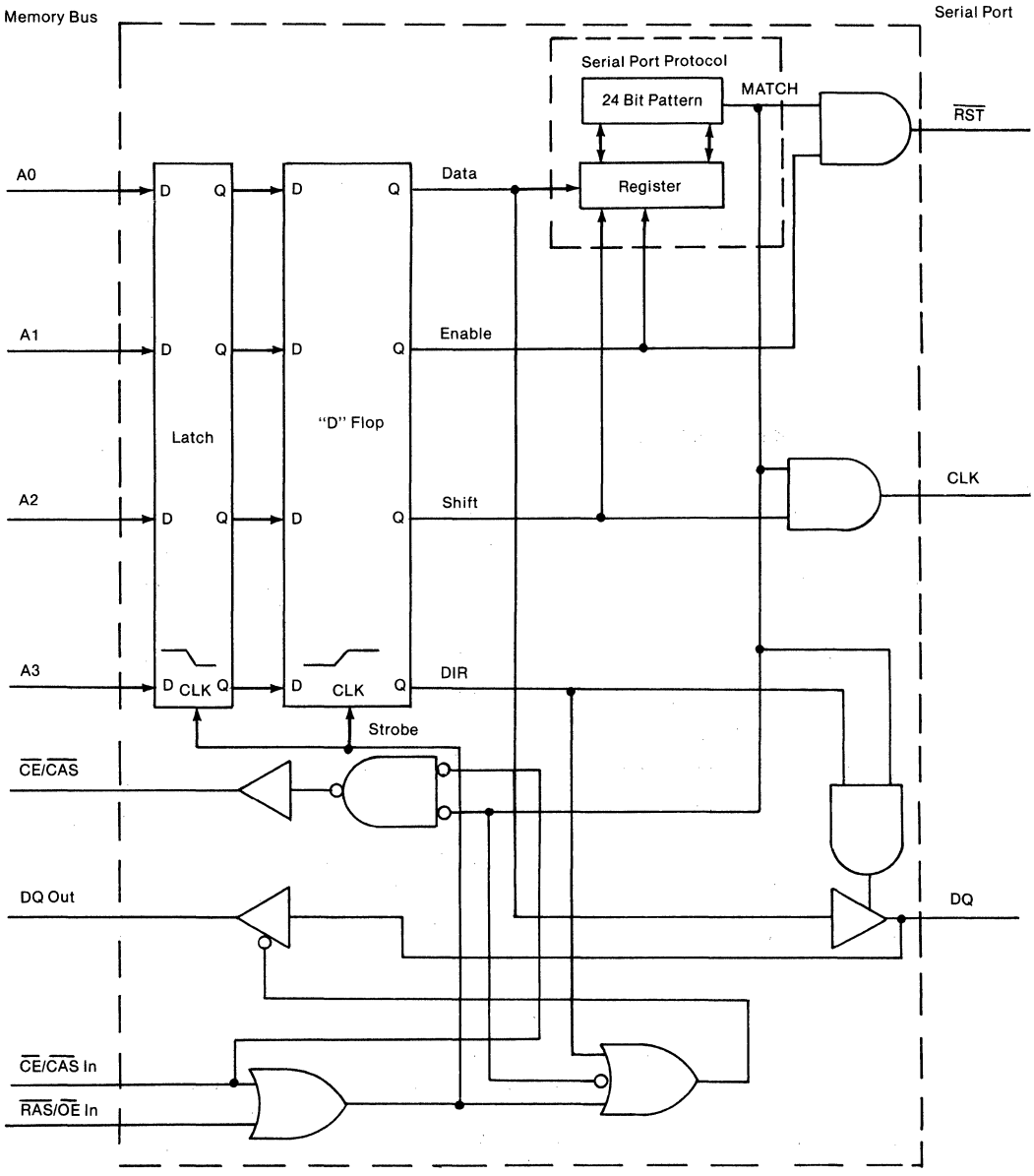
lines A0 through A3, the $\overline{CE}/\overline{CAS}$ signal and $\overline{RAS}/\overline{OE}$ signal, without affecting address space, thereby maintaining transparency to the memory bus. Communication is established under software control by an address pattern recognition sequence (serial port protocol) which disables a ByteWide or DRAM memory via $\overline{CE}/\overline{CAS}$ output. An additional address sequence is required to generate the three wire port signals: $\overline{RESET}$ ($\overline{RST}$), Data (DQ), and Clock (CLK). The add-on serial port provides a minimum cost interface to the DS1201 Tag, the DS1204U Key, the DS1207 TimeKey, the DS1223 Configurator and the DS1290 Eliminator.

OPERATION

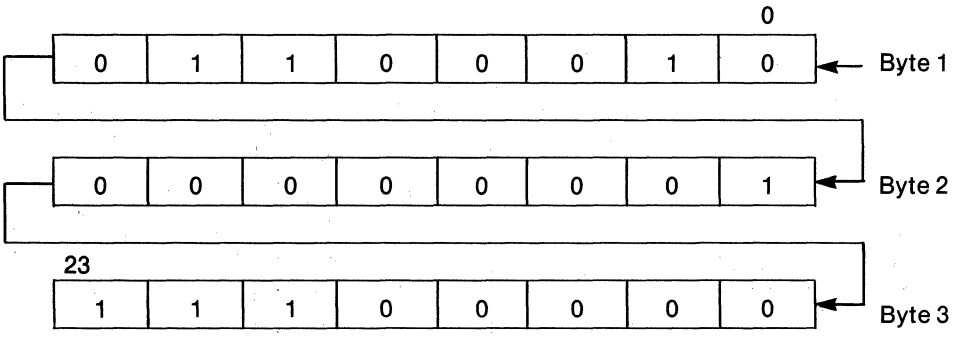
The main parts of the phantom serial interface are shown in the block diagram of Figure 1. Information presented on address inputs are latched into the DS1206 on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}/\overline{CAS}$ In and $\overline{RAS}/\overline{OE}$ In. When redirecting information from a DRAM memory bus, both $\overline{RAS}$ and $\overline{CAS}$ inputs are required and the column addresses are used for signaling. For a ByteWide memory bus, only a $\overline{CE}$ input is required and the $\overline{RAS}/\overline{OE}$ input can be tied low or connected to the memory $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 24-bit serial interface protocol and to logic which will generate signals for the serial port. The serial interface protocol is derived from address inputs A0, A1, and A2. A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially A1 input must be set high to enable serial interface communications. A1 must remain high during the pattern recognition sequence and subsequent communications with the serial port after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and future access to the serial port is denied.

Data transfer through the serial interface occurs by matching a 24 bit pattern as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Therefore, data is input for comparison to the serial interface protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24 bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24 bit register for comparison to the 24 bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles. The first memory cycle sets A2 low, establishing the shift clock low. The second memory cycle sets A2 high, causing the transition necessary to shift a bit of data into the 24 bit register. Data on A0 is kept at the correct level for both memory cycles. Address input A3 is used to control the direction of data going to and from the serial port. This input is not used during pattern recognition of the protocol. After the 24 bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for the serial port. The match signal is also used to disable Chip Enable to the memory bus and enable a gate which allows the serial port DQ to drive the DQ out line to the memory bus. When $\overline{RST}$ is driven high, devices attached to the serial port become active. Subsequent shift signals derived from A2 will now be recognized as the serial port clock. The data signal for the serial bus is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on the serial port DQ. When A3 is set low, devices attached to the serial port can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the serial port DQ.

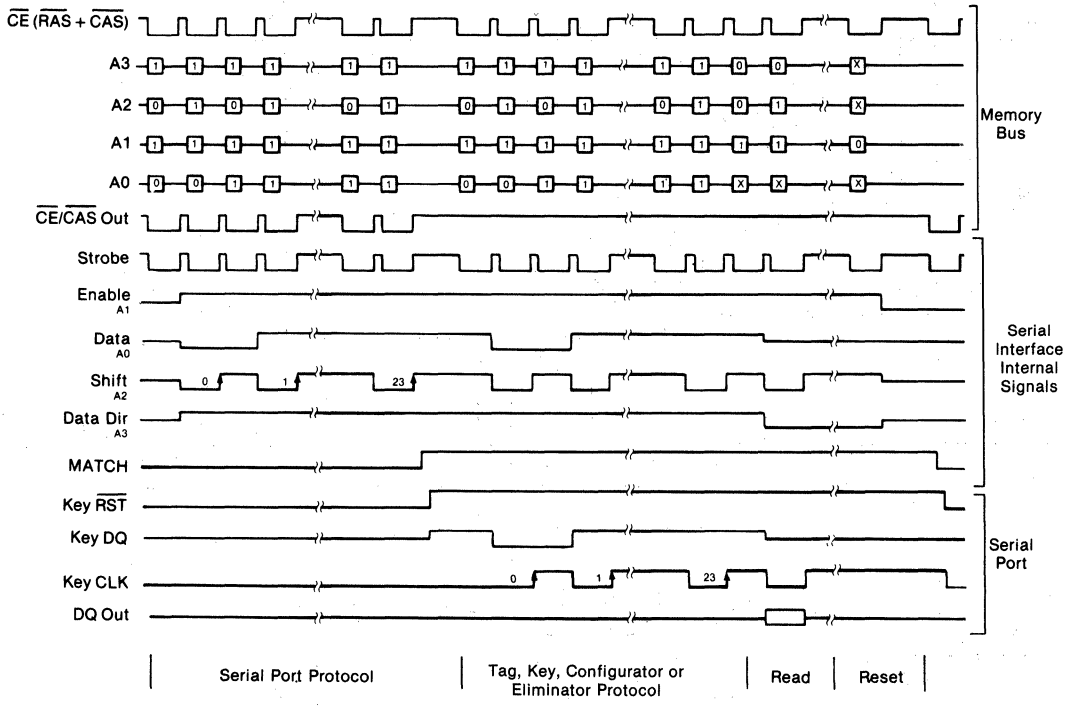
PHANTOM SERIAL INTERFACE BLOCK DIAGRAM Figure 1



SERIAL INTERFACE 24-BIT PROTOCOL Figure 2



PHANTOM SERIAL INTERFACE SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	−1.0V to +7V
OPERATING TEMPERATURE	—	0°C to +70°C
STORAGE TEMPERATURE	—	−55°C to +125°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC}+0.3$	V	1
Logic 0	V_{IL}	−0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	−1		1	μA	
Output Leakage	I_{LO}			1	μA	
Output Current @2.4V	I_{OH}	−1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
$\overline{RST}$ Output Current @3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

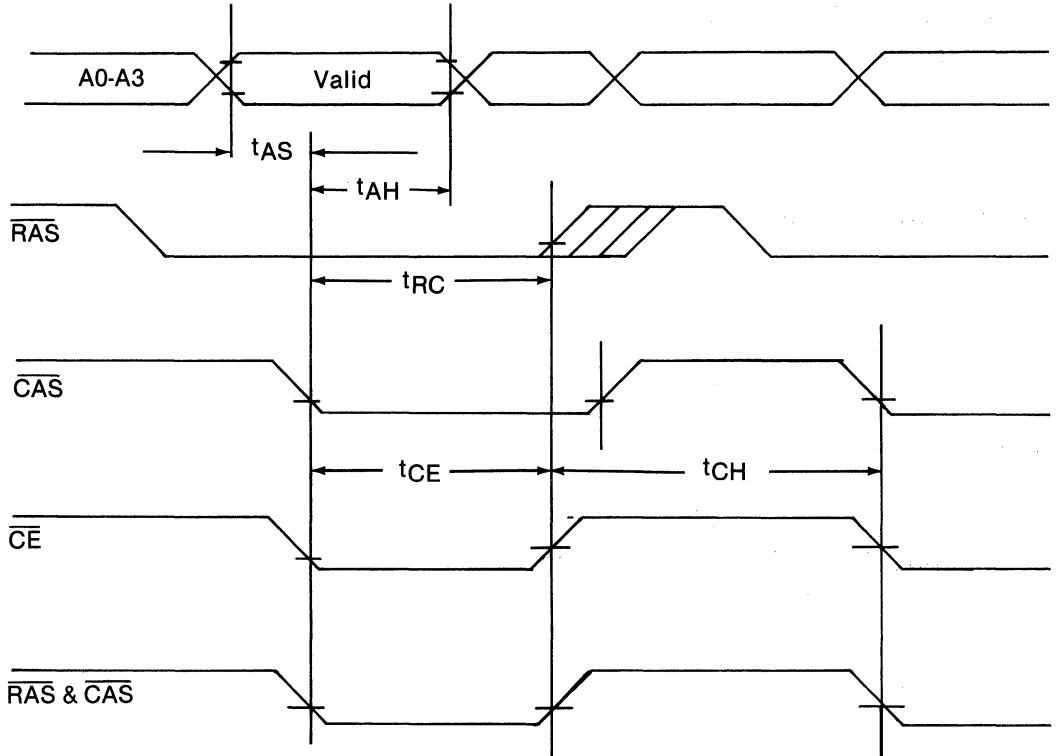
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output	$C_{I/O}$	5	10	pF	

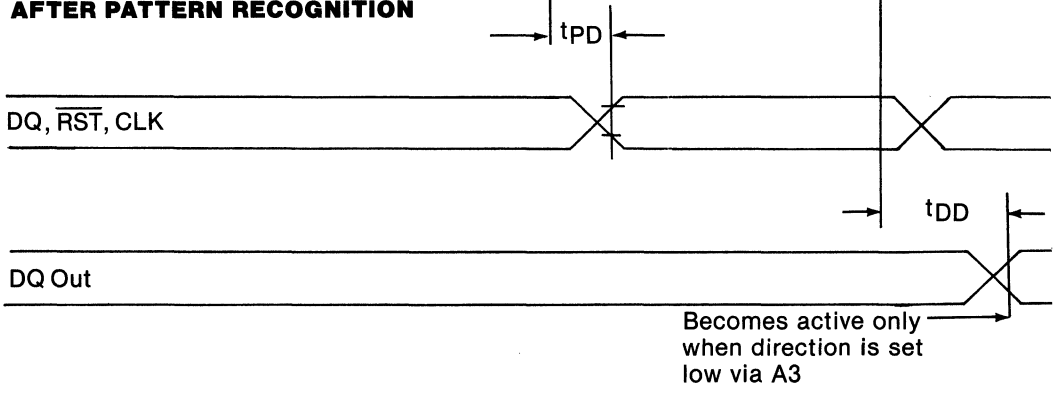
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Set Up	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
$\overline{RAS}$ to $\overline{CAS}$ Overlap	t_{RC}	60			ns	
$\overline{CE}$ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
$\overline{CE}$ Inactive	t_{CH}	30			ns	

MEMORY BUS INPUTS

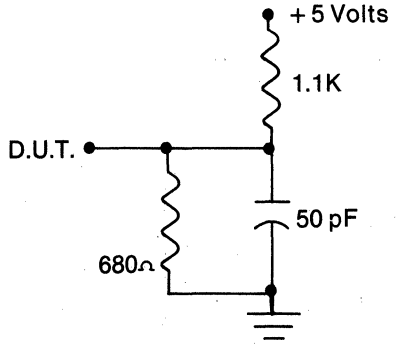


SERIAL PORT
AFTER PATTERN RECOGNITION

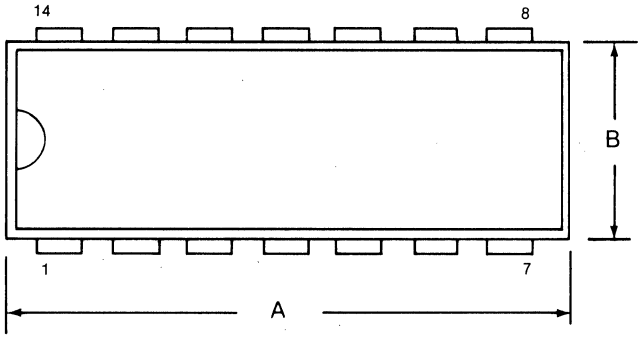


NOTES:
1. All voltages are referenced to ground
2. Measured with outputs open
3. Measured with a load as shown in Figure 4

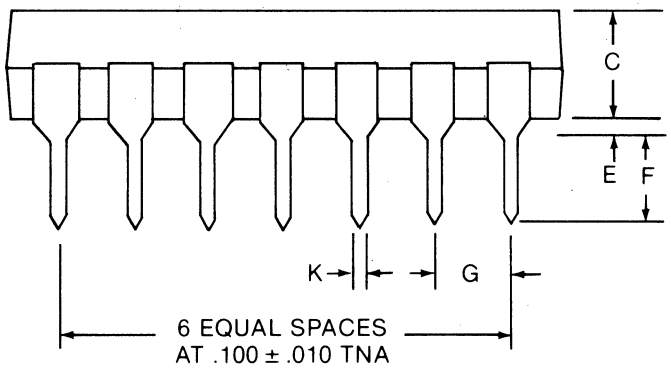
OUTPUT LOAD Figure 4

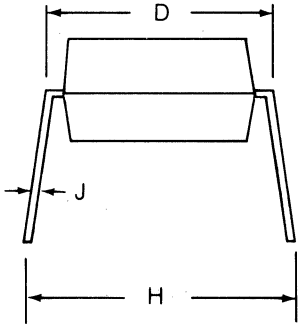


Phantom Serial Interface
DS1206
14-Pin DIP

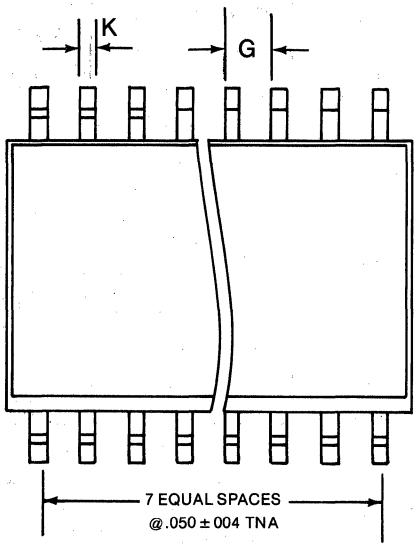


DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

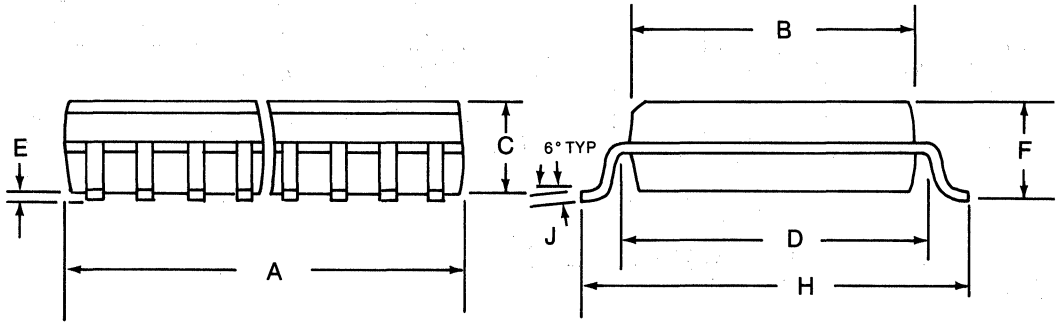




Phantom Serial Interface
DS1206S
16-Pin SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019

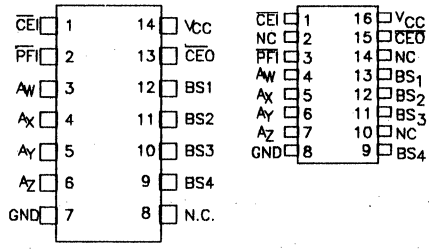


Dallas Semiconductor
BankSwitch

DS1222—14-Pin DIP
DS1222S—16-Pin SOIC

FEATURES
- Provides bank switching for 16 banks of memory
- Bank switching is software controlled by a pattern recognition sequence on four address inputs
- Automatically sets all 16 banks off on power up
- Bank switching logic allows only one bank on at a time
- Special custom recognition patterns are available which can prevent unauthorized access
- Full ±10% operating range
- Low power CMOS circuitry
- Can be used to expand the address range of microprocessors and decoders
- Optional 16-pin SOIC surface mount package

PIN CONNECTIONS



PIN NAMES

A_W - A_Z	- Address Inputs
$\overline{CEI}$	- Chip Enable Input
$\overline{CEO}$	- Chip Enable Output
N.C.	- No Connection
BS1, BS2, BS3, BS4	- Bank Select Outputs
$\overline{PFI}$	- Power Fail Input
V_{CC}	- +5 Volts
GND	- Ground

DESCRIPTION
The DS1222 is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Special custom patterns are available from Dallas Semiconductor which can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212, up to 16 banks of static RAMs can be selected.

OPERATION—BANK SWITCHING

Initially, on power up all four bank select outputs are low and the chip enable output ($\overline{CEO}$) is held high. Note: the power fail input ($\overline{PFI}$) must be low prior to power-up to assure proper initialization. Bank switching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which will set the bank switch, a read cycle of 1111 on address inputs A_W through A_Z should be executed to guarantee that pattern entry starts with Bit 0. Each set of address inputs is clocked into the DS1222 when $\overline{CEI}$ is driven low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses A_X, A_Y, and A_Z. However, address line A_W defines the bank number to be enabled as per Table 2.

Switch to a selected bank of memory occurs on the rising edge of chip enable input when the last set of bits is input and a match has been established. After bank selection $\overline{CEO}$ always follows $\overline{CEI}$ with a maximum propagation delay of 15 ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

ADDRESS INPUT PATTERN Table 1

	Bit Sequence															
Address Inputs	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_W	1	0	1	0	0	0	1	1	0	1	0	×	×	×	×	×
A_X	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_Y	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_Z	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

× See Table 2

BANK SELECT CONTROL Table 2

Bank Selected	A_W Bit Sequence					Outputs			
	11	12	13	14	15	BS1	BS2	BS3	BS4
*Banks Off	0	×	×	×	×	Low	Low	Low	Low
Bank 0	1	0	0	0	0	Low	Low	Low	Low
Bank 1	1	0	0	0	1	High	Low	Low	Low
Bank 2	1	0	0	1	0	Low	High	Low	Low
Bank 3	1	0	0	1	1	High	High	Low	Low
Bank 4	1	0	1	0	0	Low	Low	High	Low
Bank 5	1	0	1	0	1	High	Low	High	Low
Bank 6	1	0	1	1	0	Low	High	High	Low
Bank 7	1	0	1	1	1	High	High	High	Low
Bank 8	1	1	0	0	0	Low	Low	Low	High
Bank 9	1	1	0	0	1	High	Low	Low	High
Bank 10	1	1	0	1	0	Low	High	Low	High
Bank 11	1	1	0	1	1	High	High	Low	High
Bank 12	1	1	1	0	0	Low	Low	High	High
Bank 13	1	1	1	0	1	High	Low	High	High
Bank 14	1	1	1	1	0	Low	High	High	High
Bank 15	1	1	1	1	1	High	High	High	High

*$\overline{CEO} = V_{IH}$ independent of $\overline{CEI}$

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground -0.3V to +7.0V

Operating Temperature 0°C to 70°C

Storage Temperature −55°C to +125°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0	V_{IL}	−0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	−1.0		+1.0	*u*A	
I/O Leakage Current	I_{LO}	−1.0		+1.0	*u*A	
Output Current @2.4V	I_{OH}	−1.0			mA	2
Output Current @0.4V	I_{OL}			+4.0	mA	2
Operating Current	I_{CC}			15	mA	

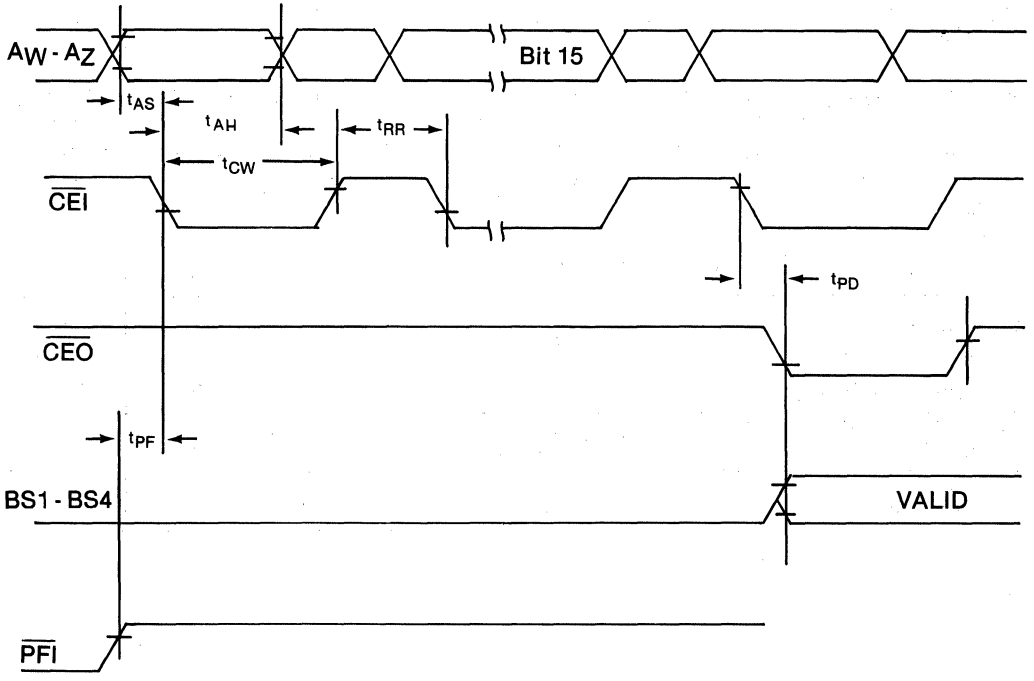
CAPACITANCE ($t_A = 25°$)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Set-Up	t_{AS}	5			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
Propagation Delay	t_{PD}			15	ns	2
Power Fail Input to First $\overline{CE}$	t_{PF}	50			ns	
Chip Enable Low	t_{CW}	110			ns	

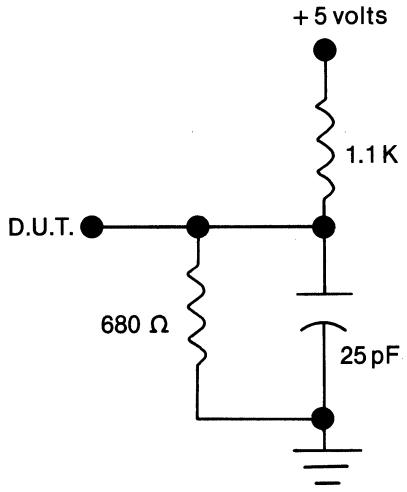
TIMING DIAGRAM—ACCESS TO BANK SWITCH



NOTES: 1. All voltages are referenced to ground.

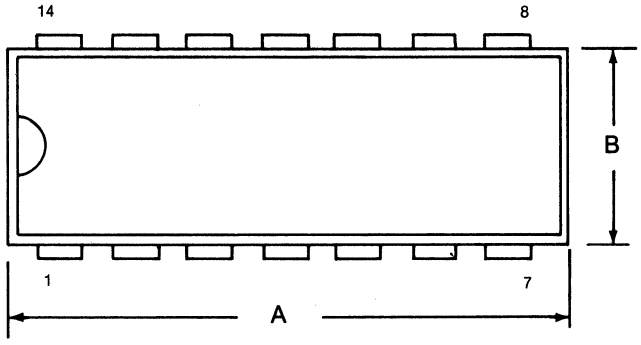
2. Measured with a load as shown in Figure 1.

OUTPUT LOAD Figure 1



Output Load

Bank Select Controller
DS1222
14-Pin DIP



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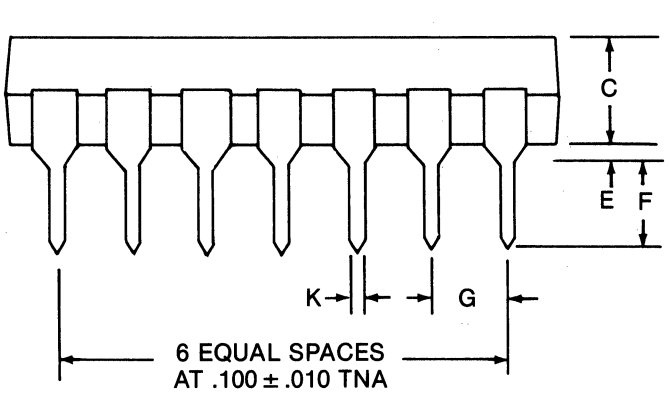
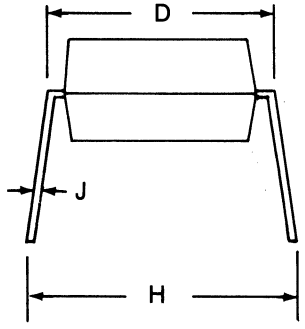
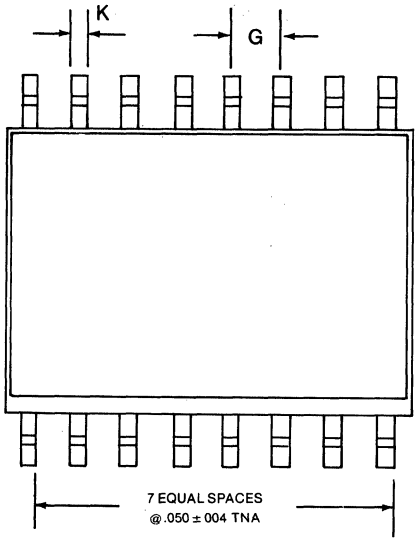




Bank Select Controller
DS1222S
16-Pin SOIC



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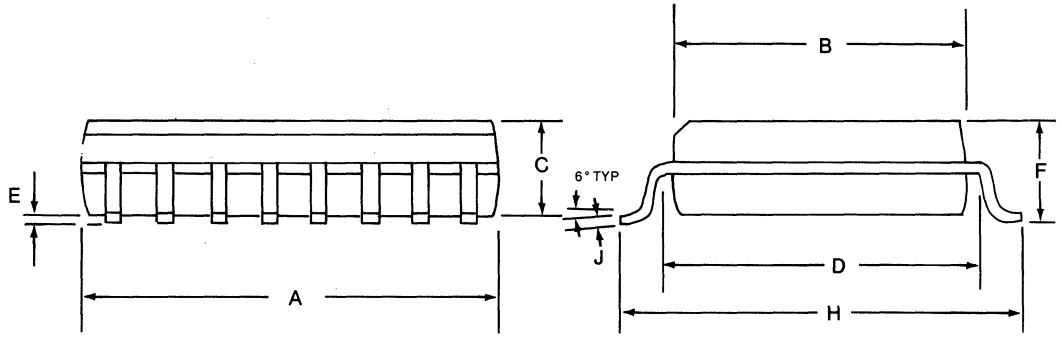
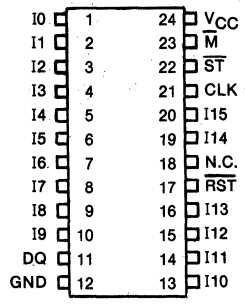


Dallas Semiconductor
Electronic Configurator — *DS1223*

FEATURES
- 16 remote programmable switches
- 9 Bytes of nonvolatile read/write memory
- 16 bit programmable comparator
- 3 pin serial port sets switches and accesses memory
- Greater than 10 years of data retention
- Data and switch settings are automatically protected during power loss
- Full 10% operating range
- Applications include DIP switch replacement; remote P.C. board configuration, mapping, and decoding
- Connects directly to DS1206 Phantom Interface

PIN CONNECTIONS



PIN NAMES

I0-I15	-	Switch, Comparator Input/Outputs
DQ	-	Data Input/Data Output
GND	-	Ground
$\overline{RST}$	-	$\overline{RESET}$
CLK	-	CLOCK
$\overline{ST}$	-	$\overline{STROBE}$
V_{CC}	-	+5 Volts
NC	-	No Connection
$\overline{M}$	-	Comparator Match

DESCRIPTION

The DS1223 Electronic Configurator is a CMOS nonvolatile switch, comparator, and read/write memory circuit designed for personalizing and configurating electronic equipment remotely. The configurator has 16 switches which can be remotely programmed to either Logic 1, Logic 0 or high impedance. Switch pairs can also be connected to simulate 8 SPST switches. In addition, the logic state of 16 inputs can be compared to data contained in nonvolatile memory. There are 16 bytes of nonvolatile read/write memory. Bytes 0, 1, 2, 3, and 4 define switch settings; bytes 5 and 6 relate to the comparator; bytes 7 through 15 are free for any desired use.

A lithium energy source retains information stored in all 16 bytes of memory when power is lost. The electronic configurator monitors V_{CC} for an out of tolerance condition. When such a condition occurs, the lithium energy source is switched on, and write protection is enabled to prevent loss of data. While in the data retention mode the switch/comparator outputs are all in a high impedance mode and all inputs are ignored.

Information is sent to the configurator via a serial input one byte at a time or in a burst where all 16 bytes are either written or read. Interface to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{\text{RESET}}$, Data Input/Output.

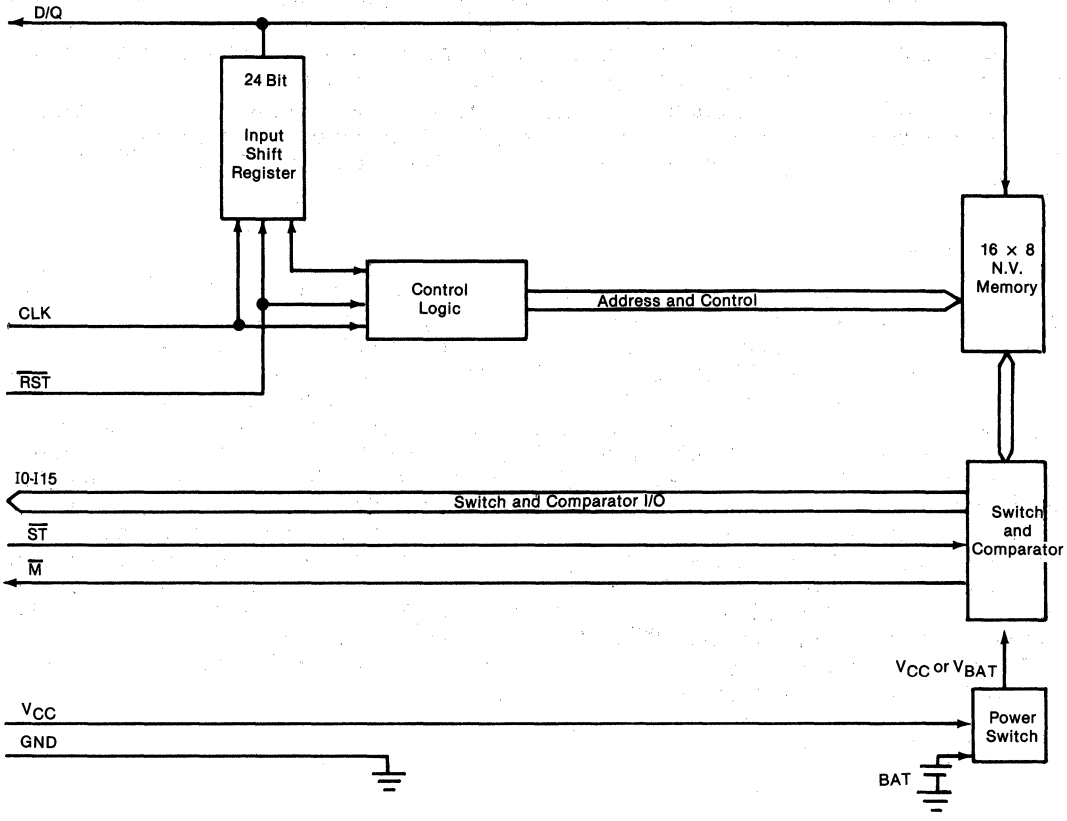
OPERATION

The block diagram (Figure 1) of the electronic configurator illustrates the main elements of the device; namely, input shift register, control logic, nonvolatile memory, switch and comparator circuits, and power switch. To initiate communication with the configurator $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the input shift register providing both address and command information. Each bit is input serially on the rising edge of the clock. Four address bits specify one of 16 nonvolatile memory locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 clocks which load the input shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals 24 plus 8 for byte mode or 24 plus 128 for burst mode.

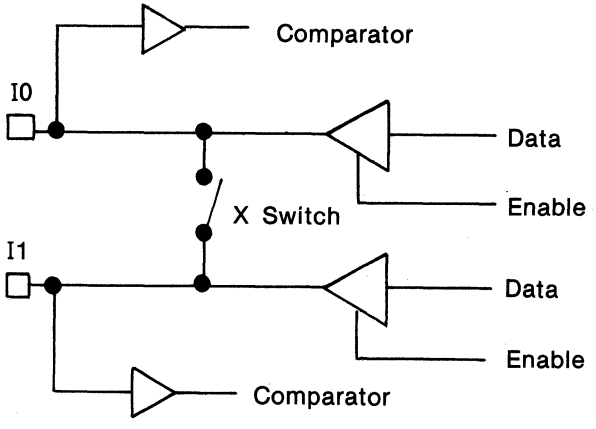
The information stored in the first five bytes of the nonvolatile memory define the status of input/output pins I0-I15. The switch configuration is illustrated in Figure 2. Data stored in nonvolatile memory bytes 6 and 7 contain 16 bits which are compared to the input/output pins I0-I15. When all inputs match the value stored in bytes 6 and 7, the $\overline{\text{MATCH}}$ pin will be latched and driven low when the $\overline{\text{STROBE}}$ input transitions from low to high.

The nine remaining bytes serve as user read/write nonvolatile memory. Figure 3 illustrates the configurator register address and the definition of each bit.

ELECTRONIC CONFIGURATOR BLOCK DIAGRAM Figure 1



CONFIGURATOR SWITCHES Figure 2



X Switch Resistance ≤ 500 Ω

Switch Pairs		
	I0 - I1	I8 - I9
	I2 - I3	I10 - I11
	I4 - I5	I12 - I13
	I6 - I7	I14 - I15

CONFIGURATOR MEMORY ADDRESSES Figure 3

	MSB 7	6	5	4	3	2	1	0 LSB	
Byte 0	I15,I14	I13,I12	I11,I10	I9,I8	I7,I6	I5,I4	I3,I2	I1,I0	X Switch 1 = Closed 0 = Open
Byte 1	I7	I6	I5	I4	I3	I2	I1	I0	Data Out 1 = Logic High 0 = Logic Low
Byte 2	I15	I14	I13	I12	I11	I10	I9	I8	Data Out 1 = Logic High 0 = Logic Low
Byte 3	I7	I6	I5	I4	I3	I2	I1	I0	Enable Out 0 = HIZ
Byte 4	I15	I14	I13	I12	I11	I10	I9	I8	Enable Out 0 = HIZ
Byte 5	I7	I6	I5	I4	I3	I2	I1	I0	Comparison
Byte 6	I15	I14	I13	I12	I11	I10	I9	I8	Comparison
Byte 7									User Byte
Byte 8									User Byte
Byte 9									User Byte
Byte 10									User Byte
Byte 11									User Byte
Byte 12									User Byte
Byte 13									User Byte
Byte 14									User Byte
Byte 15									User Byte

ADDRESS/COMMAND

Each data transfer consists of a three byte address/command input called the address/command. The address/command is shown in Figure 4. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address command fails to meet the exact pattern of read or write the cycle is aborted and all future inputs to the configurator are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The 8 bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address A0 in bit 0, A1 in bit 1, A2 in bit 2, A3 in bit 3. Bits 4 through 7 of the second byte of the address/command must be set at logical 0. If bits 4 through 7 do not equal logical 0, the cycle is aborted and all future inputs to the configurator are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The third byte of the address/command must have a logic 0 in bit 0 through bit 5 and a logical 1 written in bit 6. Bit 7 of byte three of the address/command is used along with bits A0 through A3 in byte 2 to define the burst mode. When A0 through A3 of byte two equals logical 0 and bit 7 of byte three equals logical 1, the configurator will enter the burst mode after the 24 bit address/command sequence is complete.

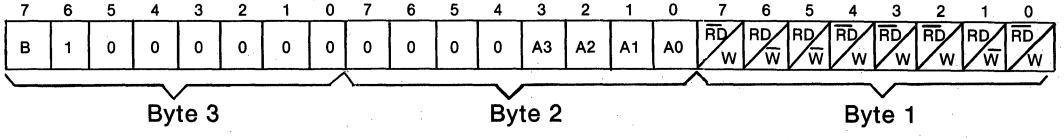
BURST MODE

Burst mode is specified for the electronic configurator when all address bits (A0-A3) of the address/command are set to logical 0 and bit 7 of byte three to logical 1. The burst mode causes 16 consecutive bytes to be read or written. Burst mode terminates when the $\overline{\text{RESET}}$ input is driven low.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{\text{RESET}}$ input high. The input also provides a method of terminating either single byte or multiple byte transfers. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of clock cycles. Address/command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates and D/Q pin goes to a high impedance state if the $\overline{\text{RESET}}$ input is low. The $\overline{\text{RST}}$ input is used only in control of communications with the configurator and has no effect on the nonvolatile memory data. Data transfer is illustrated in Figure 5.

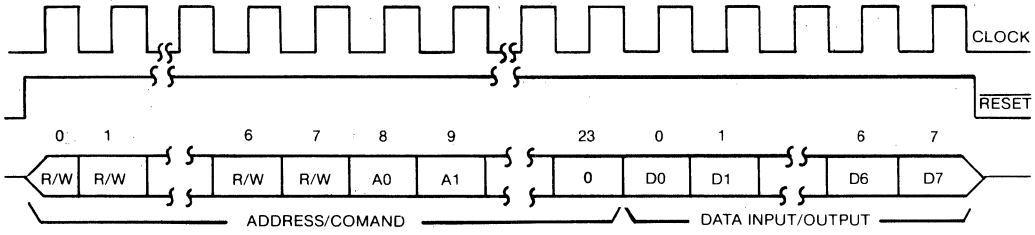
CONFIGURATOR — ADDRESS COMMAND WORD Figure 4



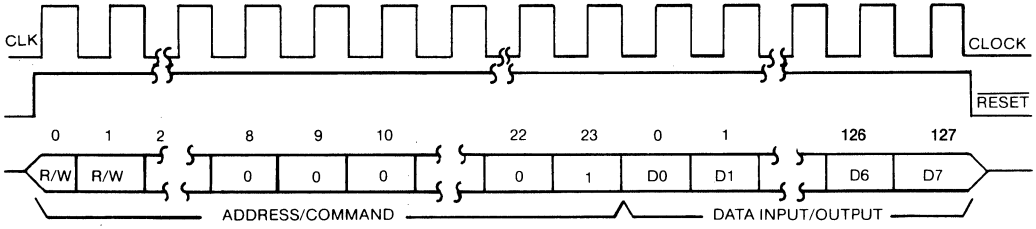
B - Burst
RD - Read
W - Write
A0-A3 - Address

DATA TRANSFER
Figure 5

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



NOTES
1.) DATA INPUT SAMPLED ON RISING EDGE OF CLOCK
2.) DATA OUTPUT CHANGES ON FALLING EDGE OF CLOCK

DATA INPUT

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next 8 CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1 bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

DATA OUTPUT

Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for data output byte 1 bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	−1.0V to +7V
OPERATING TEMPERATURE	—	0°C to 70°C
STORAGE TEMPERATURE	—	−40°C to 70°C
SOLDERING TEMPERATURE	—	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC} +.3	V	1
Logic 0	V_{IL}	−0.3		0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V ± 10%)

Input Leakage	I_{IL}			1	uA	5
Output Leakage	I_{LO}			1	uA	5
Output Current @2.4V	I_{OH}	−1			mA	11
Output Current @ .4V	I_{OL}			+4	mA	11
Output Current @2.4V	I_{OH}	−400			uA	12
Output Current @ .4V	I_{OL}			1.6	mA	12
X Switch Impedance	X			500	Ω	7
Active Current	I_{CC1}			10	mA	8
Standby Current	I_{CC2}			2	mA	8, 2

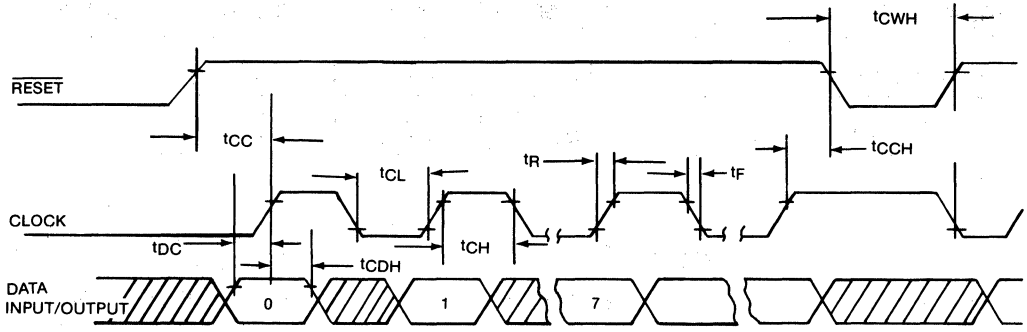
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MIN	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

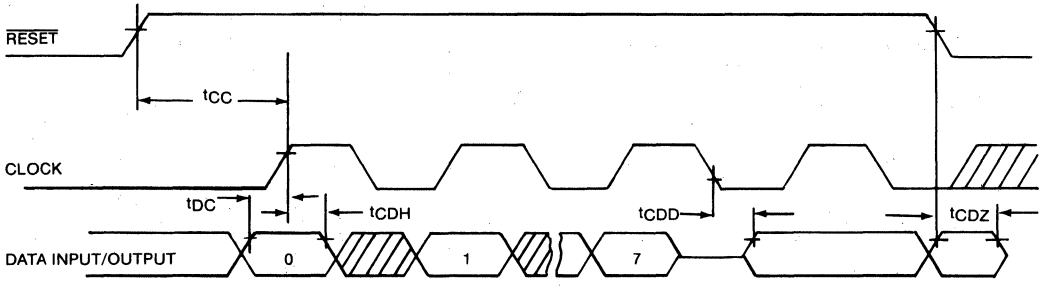
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	3
Data to CLK Hold	t_{CDH}	50			ns	3
CLK to Data Delay	t_{CDD}			200	ns	3, 4, 6
CLK Low Time	t_{CL}	250			ns	3
CLK High Time	t_{CH}	250			ns	3
CLK Frequency	f_{CLK}	D.C.		2.0	MHZ	3
CLK Rise & Fall	t_R, t_F			10	ns	3
$\overline{RST}$ to CLK Set Up	t_{CC}	1			us	3, 9
CLK to $\overline{RST}$ Hold	t_{CCH}	50			ns	3
$\overline{RST}$ Inactive Time	t_{CWH}	1			us	3
$\overline{RST}$ to //O High Z	t_{CDZ}			75	ns	3
Strobe to $\overline{MATCH}$ Valid	t_{SM}			35	ns	3
Input Set-Up	t_{SU}	40			ns	3,4
Input Hold	t_{HD}	10			ns	3,4

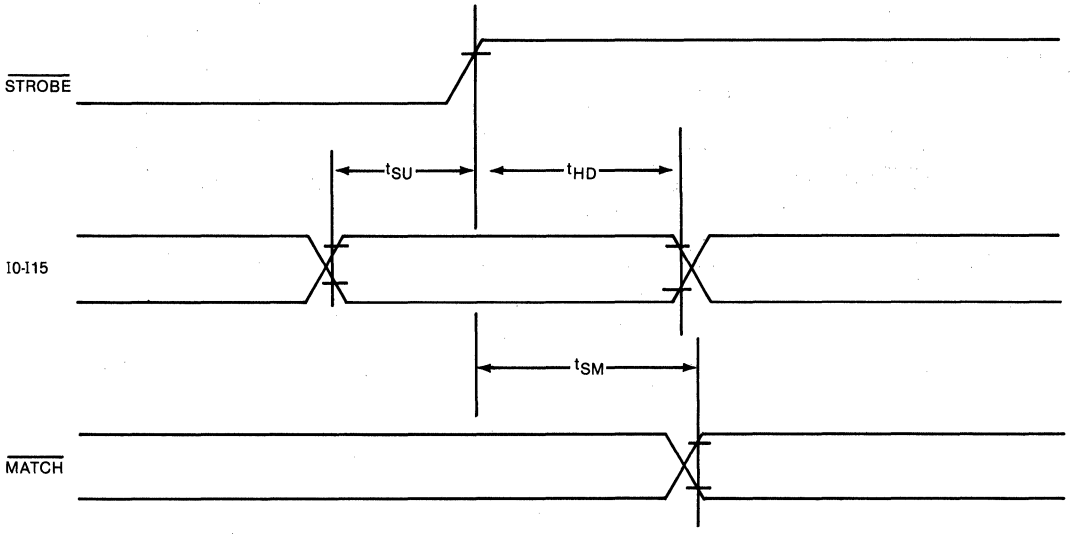
TIMING DIAGRAM—WRITE DATA TRANSFER[10]



TIMING DIAGRAM—WRITE DATA TRANSFER[10]



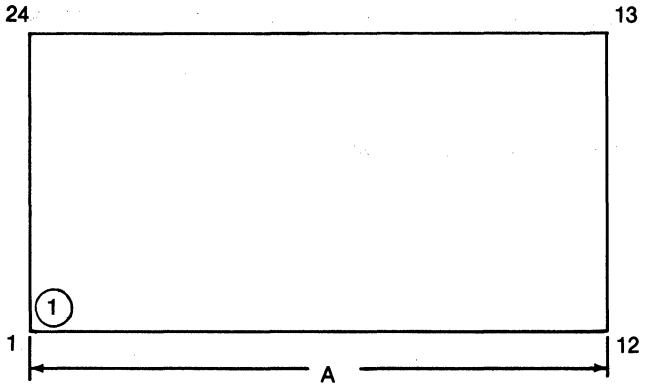
TIMING DIAGRAM—COMPARATOR[10]



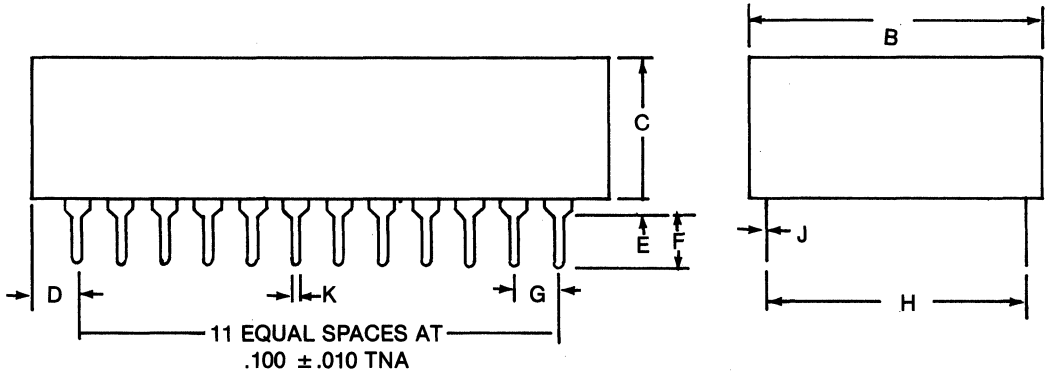
NOTES

1. All voltages are referenced to GND.
2. $\overline{\text{RESET}} = V_{IH}$.
3. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8V$ and 10 ns maximum rise and fall time.
4. Measured at $V_{OH} = 2.4$ volts and $V_{OL} = 0.4$ volts.
5. $V_{CC} = +5$ Volts with outputs open.
6. Load capacitance = 100 pF.
7. X Switch Impedance is the terminal resistance of switch pairs when the X Switch is closed—see Figure 2.
8. Measured with outputs open.
9. Measured at V_{IN} of $\overline{\text{RST}} = 3.8V$.
10. A period of 100 ns must elapse after data transfer before switches and comparator outputs are valid.
11. Applies to DQ and $\overline{\text{MATCH}}$.
12. Applies to switches.

DS1223
Electronic Configurator



DIM.	INCHES	
	MIN.	MAX.
A	1.320	1.335
B	.685	.700
C	.345	.360
D	.100	.120
E	.015	.030
F	.110	.130
G	.090	.110
H	.620	.670
J	.008	.012
K	.015	.021



NOTE: Pin 18 is missing by design.

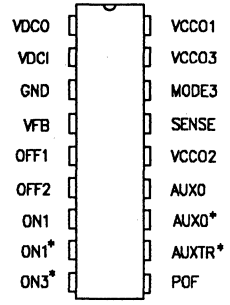
Dallas Semiconductor
KickStarter

PRODUCT PREVIEW
DS1227

FEATURES

- Power management chip for conserving power in battery-operated systems
- Ultra-low standby current drain
- "Kickstarts" system power on via external events such as:
  - Photodiode sensor trip
  - Clock/calendar alarm
  - Any low-level signal transition
- Shuts down power under software control
- Steps up 3V lithium battery voltage to +5V using integral DC-DC converter
- Steps down 6V battery to +5V
- Can place DS5000 Soft Microcontroller in serial load mode for remote downloading of new program code
- Available in 18-pin DIP or 20-pin SOIC surface-mount package

PIN DESCRIPTION



PIN NAMES

VDCO	- Output of DC-DC converter
VDCI	- Input to DC-DC converter
GND	- System ground
VFB	- Feedback voltage sense
OFF1	- Shut-down control for VCCO1
OFF2	- Shut-down control for VCCO2
ON1	- Positive-edge trigger of VCCO1
ON1*	- Negative-edge trigger of VCCO1
ON3*	- Negative-edge trigger of VCCO3
POF	- Power-on indicator flag
AUXTR*	- Negative-edge trigger input for switching AUXO and AUXO*
AUXO*	- Auxilliary output inverted
AUXO	- Auxilliary output
VCCO2	- 5V output 2
SENSE	- Sensor detect input
MODE3	- Mode control for VCCO3
VCCO3	- 5V output 3
VCCO1	- 5V output 1

DESCRIPTION

The DS1227 is a CMOS chip that orchestrates power conservation in battery-operated systems. Using its integral DC-DC converter, the DS1227 will provide +5V to the system from either a 3 or 6 volt battery input. The +5V outputs can be selectively turned on or off based on momentary system events. A circuit using this part can "wake up" from an ultra-low power state, perform a task and then go back to sleep until the DS1227 is signalled to "kickstart" system operation again. "Kickstarting" occurs whenever the DS1227 senses a logic transition or alarm from an external device such as the DS1284 Watchdog Timekeeper. In this scenario a system could wake up at a certain time and date to take a reading from a sensor (storing that reading in the DS5000 Soft Microcontroller) and then go back to a zero-power state.

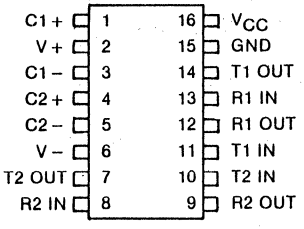
Dallas Semiconductor
+5V Powered Dual RS-232 Transmitter/Receiver

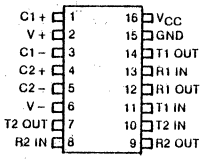
DS232
DS1228—16-Pin DIP
DS1228S—16-Pin SOIC

FEATURES

- Operates from a single 5V power supply
- 2 drivers and 2 receivers
- Meets all EIA RS-232-C specifications
- On-board voltage doubler
- On-board voltage inverter
- ±30 V input levels
- ±9 V output levels with +5 V supply
- Low power CMOS
- Pin compatible with the MAX 232
- −40°C to +85°C temperature range available
- Optional 16-pin SOIC surface mount package

PIN CONNECTIONS





PIN NAMES

C1+, C1	- Capacitor 1 Connections
C2+, C2	- Capacitor 2 Connections
V+, V−	- ±10 Volts
T1 IN, T2 IN	- Transmitter In
T1 OUT, T2 OUT	- Transmitter Out
R1 IN, R2 IN	- Receiver In
R1 OUT, R2 OUT	- Receiver Out
V_{CC}	- +5 Volts
GND	- Ground

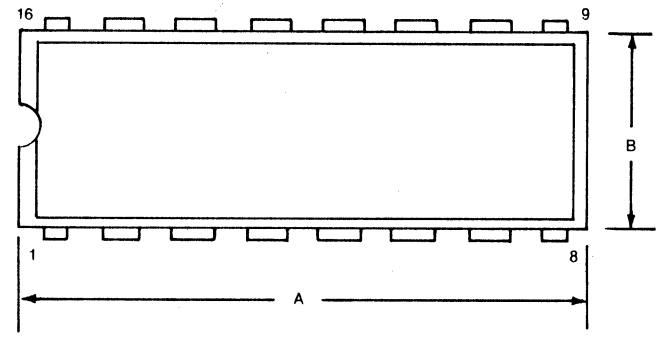
DESCRIPTION

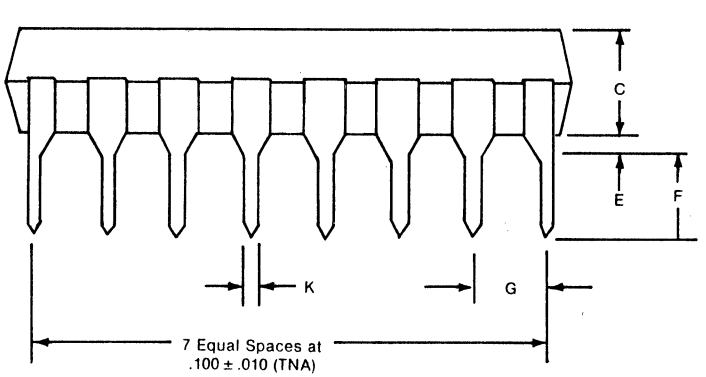
The DS232 is a dual RS-232-C Receiver/Transmitter that meets all EIA specifications while operating from a single +5 volt supply. The DS232 has two internal charge pumps. One of the charge pumps is used to generate +10 volts. The other is used to generate −10 volts. The DS232 also contains four level translators. Two of the level translators are RS-232 transmitters which convert TTL/CMOS inputs into ±9V RS-232 outputs. The other two level translators are RS-232 receivers which convert RS-232 inputs to 5V TTL/CMOS outputs. These receivers are capable of operating with up to ±30V inputs. The DS232 is suitable for all RS-232-C communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS232 supplies ±10 volts from the V_{CC} input.

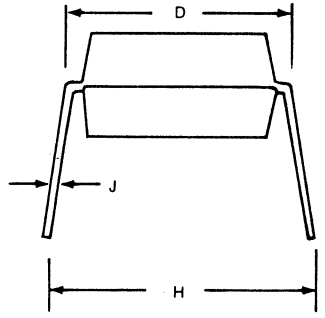
See the data sheet for the DS1229 for electrical specifications and operation.

Dual RS-232 Transmitter/Receiver
DS1228
16-Pin DIP

DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

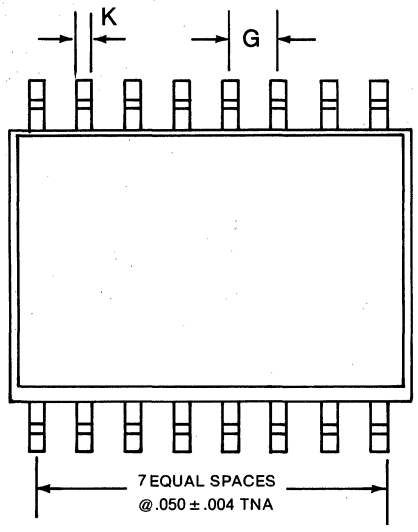




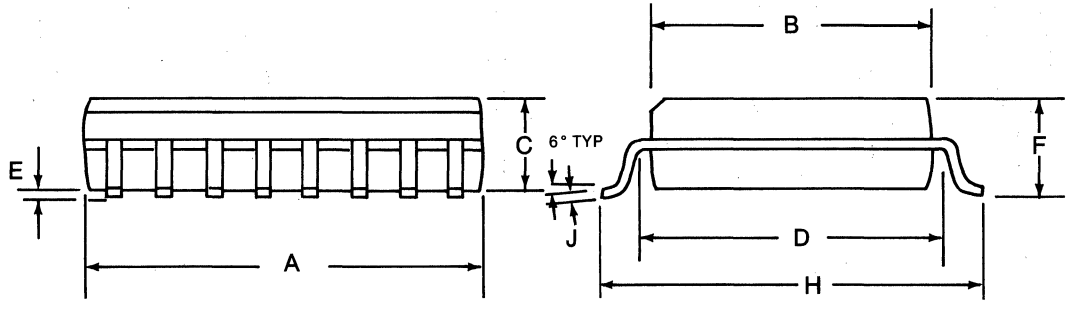


1

Dual RS-232 Transmitter/Receiver
DS1228S
16-Pin SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



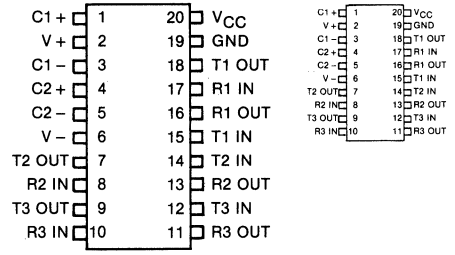
Dallas Semiconductor
+5V Powered Triple RS-232 Transmitter/Receiver

DS1229—20-Pin DIP
DS1229S—20-Pin SOIC

FEATURES

- Operates from a single 5V power supply
- 3 drivers and 3 receivers
- Meets all EIA RS-232-C specifications
- On-board voltage doubler
- On-board voltage inverter
- ±30 V input levels
- ±9 V output levels with +5 V supply
- Low power CMOS
- −40°C to +85°C temperature range available
- Optional 20-Pin SOIC surface mount package

PIN CONNECTIONS



PIN NAMES

C1+, C1	- Capacitor 1 Connections
C2+, C2	- Capacitor 2 Connections
V+, V−	- ±10 Volts
T1 IN, T2 IN, T3 IN	- Transmitter In
T1 OUT, T2 OUT, T3 OUT	- Transmitter Out
R1 IN, R2 IN, R3 IN	- Receiver In
R1 OUT, R2 OUT, R3 OUT	- Receiver Out
V_{CC}	- +5 Volts
GND	- Ground

DESCRIPTION

The DS1229 is a Triple RS-232-C Receiver/Transmitter that meets all EIA specifications while operating from a single +5 volt supply. The DS1229 has two internal charge pumps. One of the charge pumps is used to generate +10 volts. The other is used to generate −10 volts. The DS1229 also contains six level translators. Three of the level translators are RS-232 transmitters which convert TTL/CMOS inputs into ±9V RS-232 outputs. The other three level translators are RS-232 receivers which convert RS-232 inputs to 5V TTL/CMOS outputs. These receivers are capable of operating with up to ±30V inputs. The DS1229 is suitable for all RS-232-C communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS1229 supplies ±10 volts from the V_{CC} input.

OPERATION

The DS1229 has three sections: a triple transmitter, a triple receiver and a dual charge pump which generates ± 10 volts from the 5-volt supply.

CHARGE PUMP SECTION

The dual charge pumps within the DS1229 are used to generate the voltages necessary for level conversion from TTL/CMOS to RS-232. One charge pump uses external capacitor C1 to double the V_{CC} input to + 10 volts. The second charge pump uses external capacitor C2 to invert the +10 volts to −10 volts. Capacitors C3 and C4 are used to filter the + 10 volt and − 10 volt power supply. The recommended size of capacitors C1-C4 is 22 *u*F but the value is not critical. Increasing the value of C3 and C4 will lower the 16 KHz ripple on the ± 10 volt supplies and the RS-232 outputs. The value of C1 and C4 can be lowered to 1 *u*F where size is critical.

TRANSMITTER SECTION

The three transmitters are CMOS inverters powered by the internal ±10 volt supply.The input is TTL/CMOS compatible. Each input has an internal 750 K pull-up resistor so that unused transmitter inputs can be left unconnected. Unused transmitter inputs will force the outputs low. The open circuit output voltage swing is from + 10 volts to − 10 volts. Worst-case conditions for RS-232-C of ± 5 volt driving a 3 K load are met at maximum allowable ambient temperature and a V_{CC} level of 5.0 volts. Typical voltage swings of ± 9 volts occur with outputs of 5 K and V_{CC} equal to 5 volts. The slew rate at the output is limited to less than 30 volts/*u*s and the power-down output impedance will be a minimum of 300 ohms with ± 2 volts applied to the outputs and V_{CC} at zero volts. The outputs are also short-circuit-protected and can be short-circuited to ground indefinitely.

RECEIVER SECTION

The three receivers conform fully to the RS-232-C specifications. The input impedance is between 3 K ohms and 7 K ohms and can withstand up to ± 30 volts with or without V_{CC} applied. The input switching thresholds are within the ± 3 volts limit of RS-232-C specification with a V_{IL} of 0.7 volts and a V_{IH} of 2.4 volts. The receivers have 0.5 volts of hysteresis to improve noise rejection. The TTL/CMOS compatible output of the receiver will be low whenever the RS-232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between + 0.8 V and − 30 V.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} ..... + 7 volts
V+ ..... + 12 volts
V− ..... − 12 volts
Transmitter Inputs ..... − 0.3V to (V_{CC} + 0.3V)
Receiver Inputs ..... ± 30 volts
Transmitter Outputs .. (V+ + 0.3V) to (V− − 0.3V)
Receiver Outputs ..... —0.3V to (V_{CC} + 0.3V)
Storage Temperature ..... − 55 °C to 125 °C

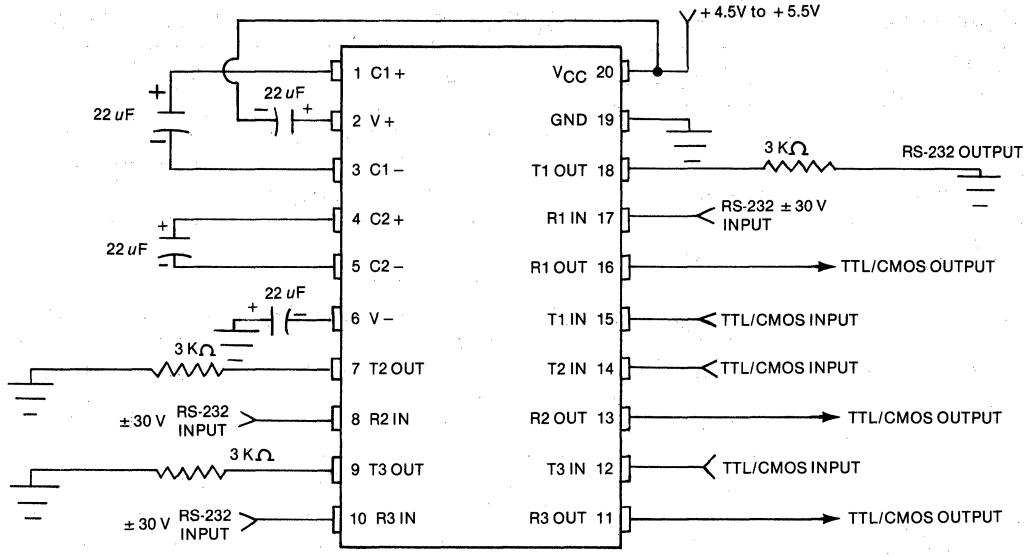
RECOMMENDED D.C. OPERATING CONDITIONS (0 °C to 70 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0 Input	V_{IL}	−0.3		+0.8	V	1
RS-232 Input Voltage	V_{RS}	−30		+30	V	1,2,11

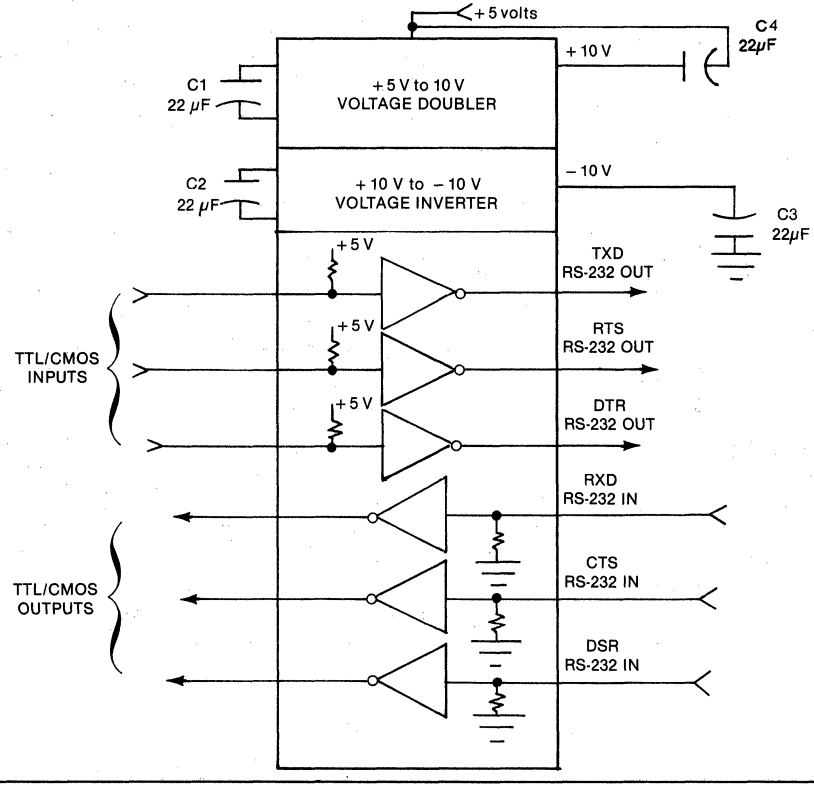
D.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{CC} = +5 volts ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RS-232 Output Voltage	V_{ORS}	±5	±9	±10	V	3,12
Power Supply Current	I_{DD}		5	10	mA	4
Transmitter Pull-up Current	I_{TP}		5	200	*u*A	5
RS-232 Input Threshold Low	V_{TL}	+0.7	+1.2		V	6
RS-232 Input Threshold High	V_{TH}		1.7	2.4	V	6
RS-232 Input Hysteresis	V_{HY}	0.2	0.5	1.0	V	
ReceiverOutput Current @2.4 V	I_{OH}	−1.0			mA	
Receiver Output Current @0.4 V	I_{OL}			+3.2	mA	
Output Resistance	R_{OUT}	300			Ω	7
RS-232 Output Short Circuit	I_{SC}			±25	mA	
Propagation Delay	t_{PD}		3		*u*s	8
Transmitter Output Instantaneous Slew Rate	t_{SR}			30	V/*u*s	9
Transmitter Output Transition Slew Rate	t_{tSR}		3		V/*u*s	10
V+ Supply Voltage	V+	+5.5	9		V	
V− Supply Voltage	V−	−5.5	8.5		V	

DS1229 RS-232 TRANSMITTER/RECEIVER TEST CIRCUIT Figure 1



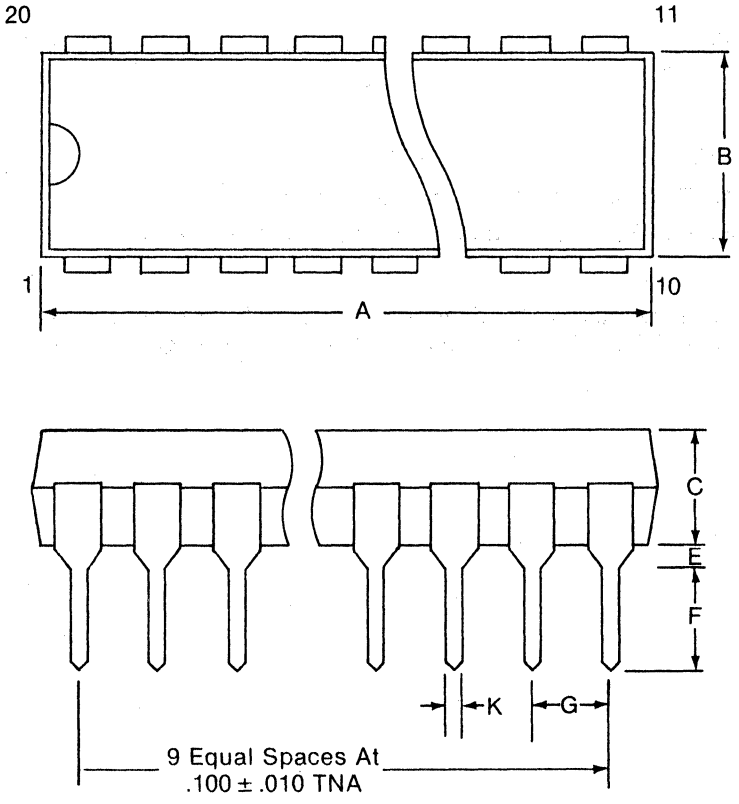
TYPICAL APPLICATIONS Figure 2



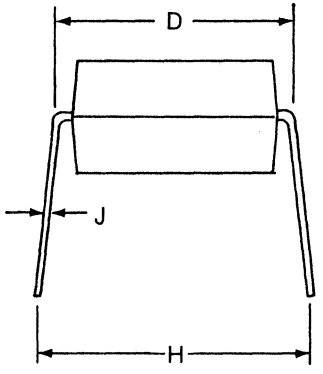
NOTES:

1. All voltages are referenced to ground.
2. Applies to Receiver Inputs only.
3. T1, T2, and T3 loaded with 3K ohms to ground.
4. All outputs are unloaded.
5. T1, T2, and T3 Inputs = 0 volts.
6. V_{CC} = +5 volts.
7. V_{OUT} = ±2 volts.
8. RS-232 to TTL or TTL to RS-232.
9. C_L = 10 pF, RL = 3 K, TA = 0°C. This parameter is sample tested only.
10. R_L = 3 K , C_L = 2500 pF measured from +3 volts to −3 volts or −3 volts to +3 volts.
11. This parameter is sample tested only.
12. Negative output level of −5V is increased to −4.75V for the DS1229 only. Positive output level remains at +5V. Use of a +10%, −5% power supply will restore the negative level to −5V.

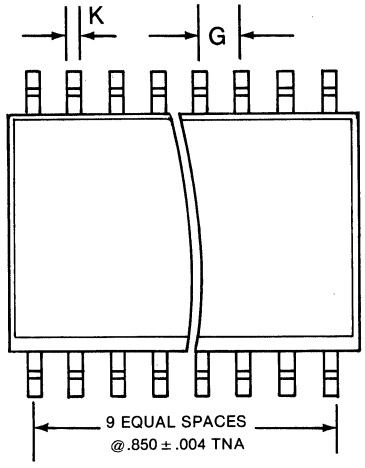
Triple RS-232 Transmitter/Receiver
DS1229
20-Pin DIP



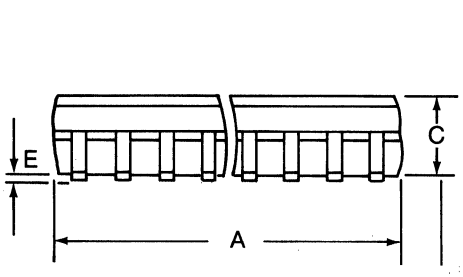
DIM.	INCHES	
	MIN.	MAX.
A	.960	1.040
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

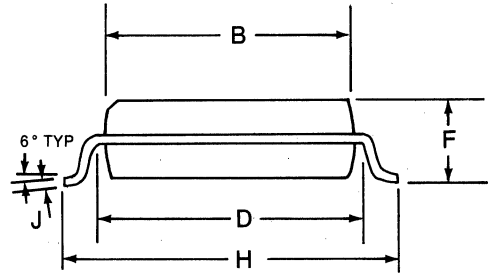


Triple RS-232 Transmitter/Receiver
DS1229S
20-Pin SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.503	.511
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019





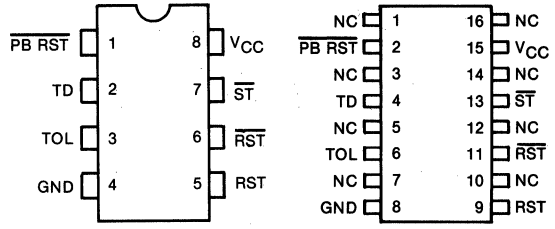
Dallas Semiconductor
MicroMonitor

DS1232—8-Pin DIP
DS1232S—16-Pin SOIC

FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components
- Space saving 8-pin Mini-DIP
- Optional 16-pin SOIC surface mount package

PIN CONNECTIONS



PIN NAMES

$\overline{\text{PB RST}}$	- Push Button Reset Input
TD	- Time Delay Set
TOL	- Selects 5% or 10% V_{CC} Detect
GND	- Ground
RST	- Reset Output (Active High)
$\overline{\text{RST}}$	- Reset Output (Active Low, Open Drain)
$\overline{\text{ST}}$	- Strobe Input
V_{CC}	- +5 Volt Power
NC	- No Connections

DESCRIPTION

The DS1232 monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature compensated reference and comparator circuit is used to monitor the status of power (V_{CC}). When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize. The second function the DS1232 performs is pushbutton reset control. The DS1232 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232 has an internal timer which forces the reset signals to the active state if the strobe input is not driven low prior to time out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION—POWER MONITOR

The DS1232 provides the function of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL (Pin 3), the V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6). When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC} the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

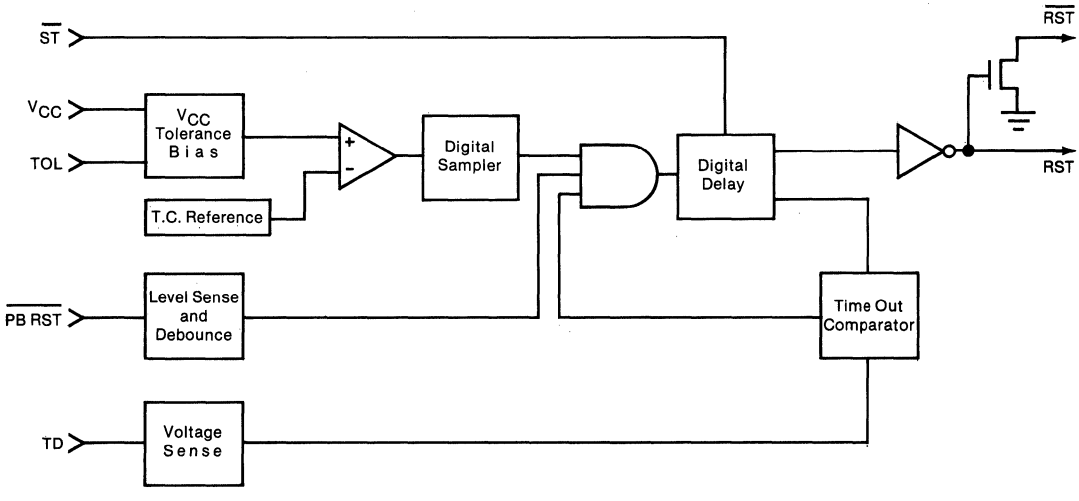
OPERATION—PUSHBUTTON RESET

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

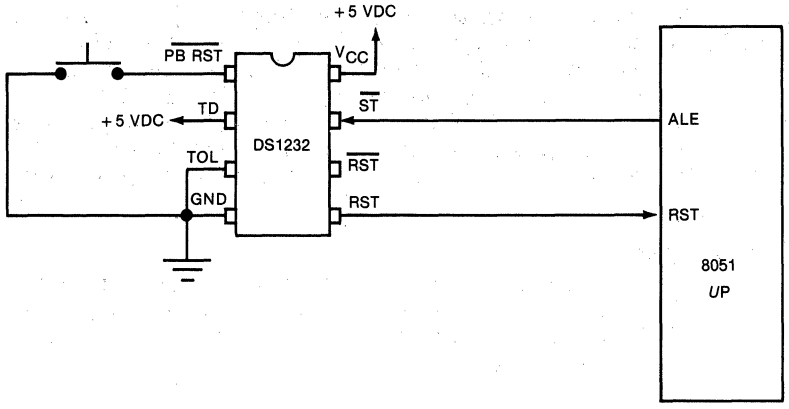
OPERATION—WATCHDOG TIMER

The DS1232 provides a watchdog timer function by forcing RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time out, the watchdog timer is reset and begins to time out again. If the watchdog timer is allowed to time out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time out. A typical example is shown in Figure 3.

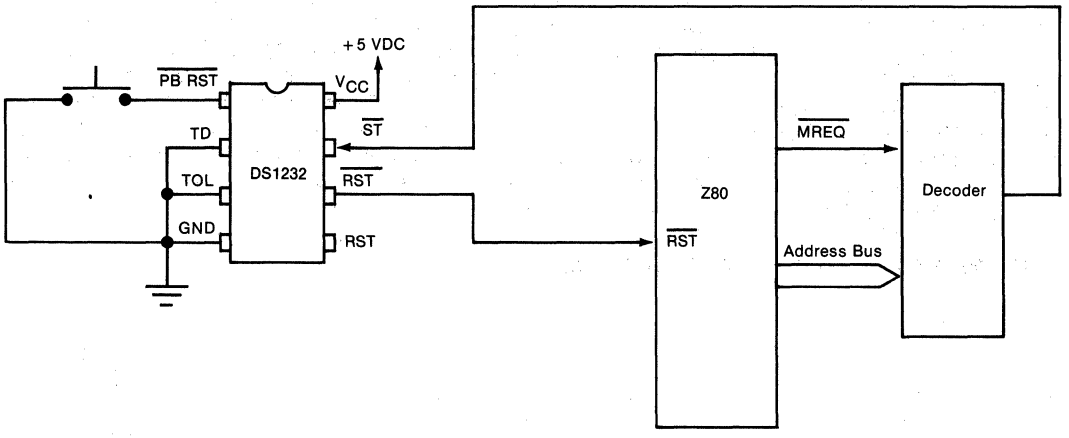
MICROMONITOR BLOCK DIAGRAM Figure 1



PUSHBUTTON RESET Figure 2



WATCHDOG TIMER Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PB\ RST}$ Input High Level	V_{IH}	2.0		$V_{CC}+0.3$	V	1
$\overline{ST}$ and $\overline{PB\ RST}$ Input Low Level	V_{IL}	−0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	−1.0		+1.0	*u*A	3
Output Current @2.4V	I_{OH}	−1.0	−2.0		mA	
Output Current @0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

1

CAPACITANCE ($t_A = 25\,°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

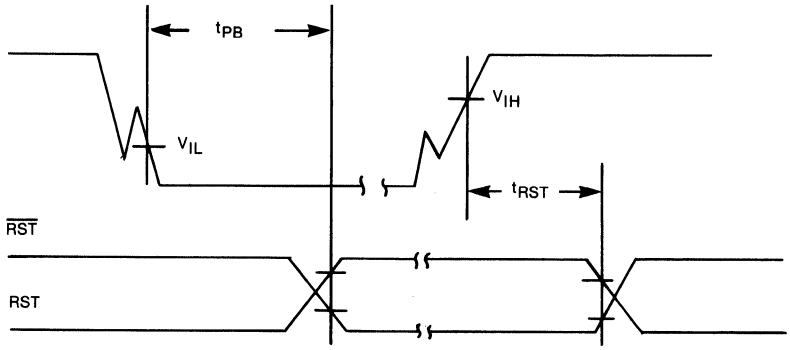
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PB}$ $\overline{RST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	
V_{CC} Detect to $\overline{RST}$ and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate 4.75V - 4.25V	t_F	300			*us*	
V_{CC} Detect to $\overline{RST}$ and $\overline{RST}$	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V - 4.75V	t_R	0			ns	

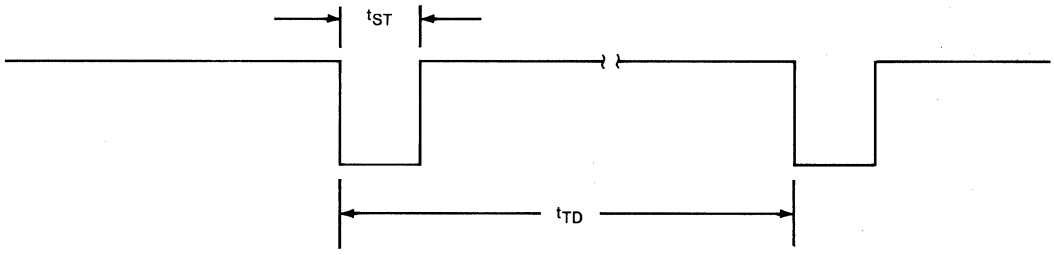
NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open.
3. $\overline{PB}$ $\overline{RST}$ is internally pulled up to V_{CC} with an internal impedance of 10K typical.
4. $t_R = 5$ *us*.
5. $\overline{RST}$ is an open drain output.

TIMING DIAGRAM—PUSHBUTTON RESET



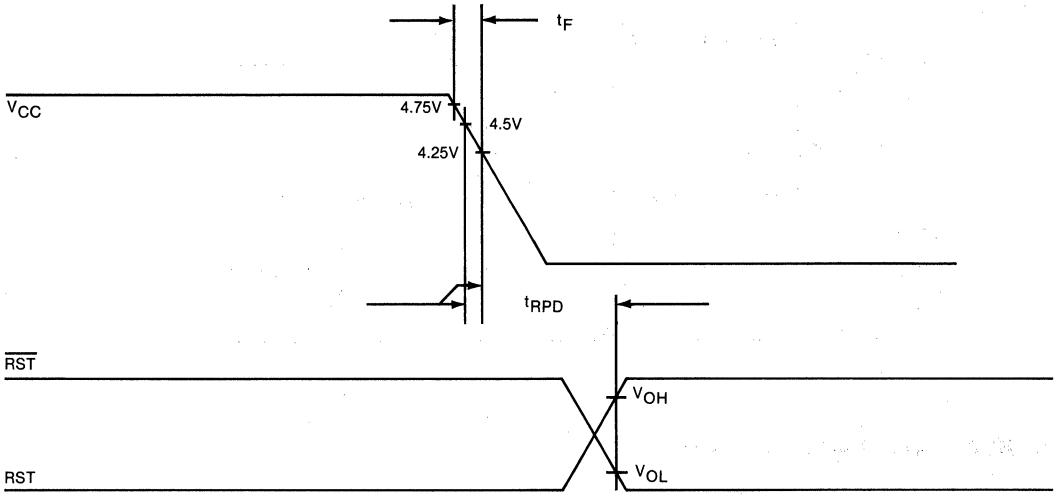
TIMING DIAGRAM—STROBE INPUT



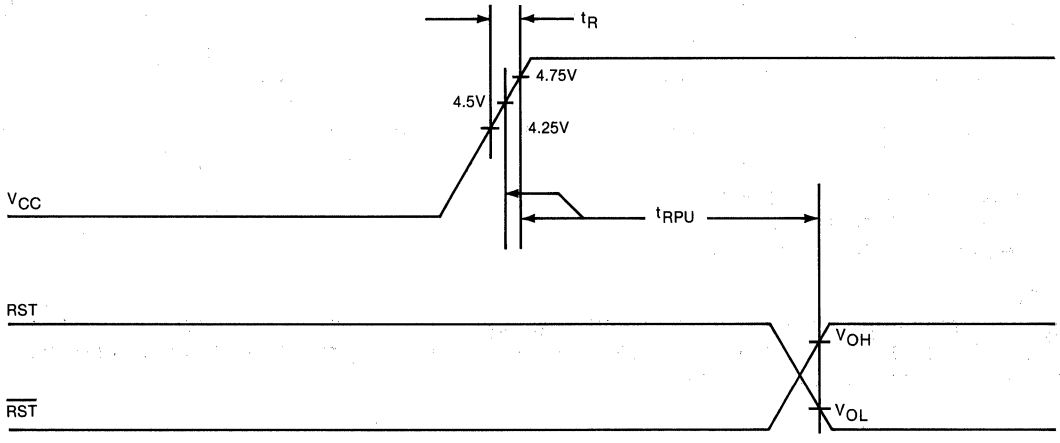
t_{TD} = 250 ms maximum with TD pin at Ground
t_{TD} = 1 sec maximum with TD pin floating
t_{TD} = 2 sec maximum with TD pin connected to V_{CC}

NOTE:
t_{TD} is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of t_{RST}. t_{TD} times are given as maximum. The minimum time is 25% of maximum.

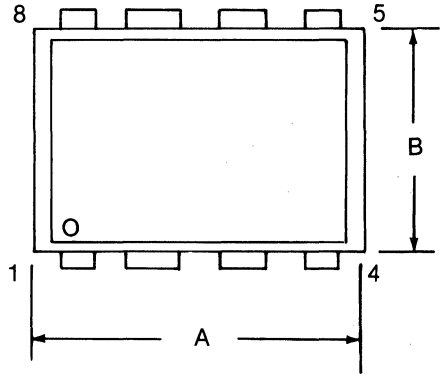
TIMING DIAGRAM—POWER DOWN



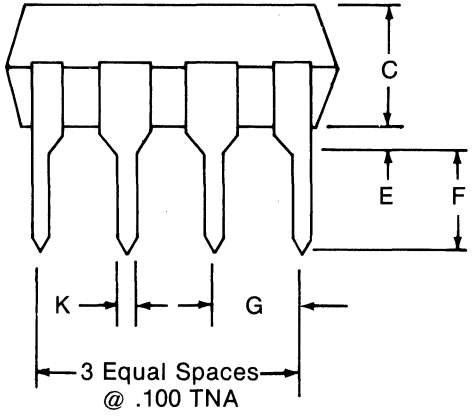
TIMING DIAGRAM—POWER UP

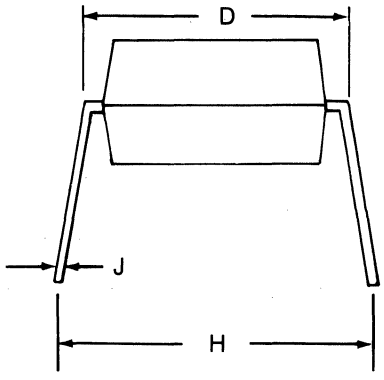


MicroMonitor
DS1232
8-Pin DIP

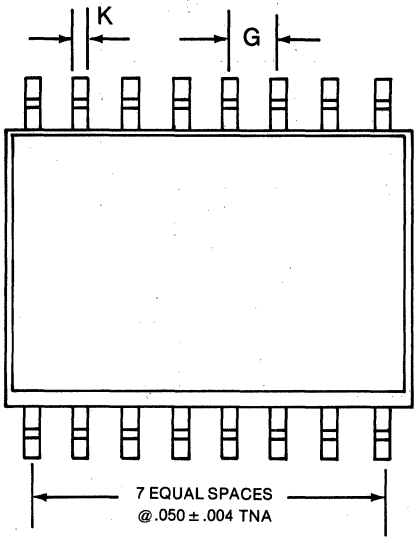


DIM.	INCHES	
	MIN.	MAX.
A	.345	.400
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

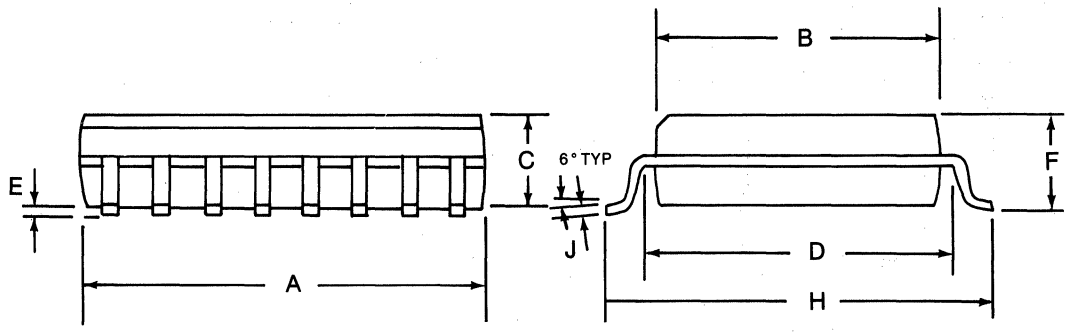




MicroMonitor
DS1232S
16-Pin SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



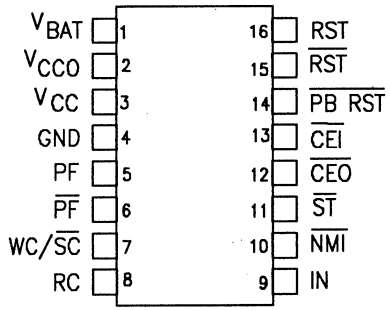
Dallas Semiconductor
Micro Manager

PRELIMINARY
DS1236 16-Pin DIP
DS1236S 16-Pin SOIC

FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors pushbutton for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1236-5
- Standard 16-Pin DIP or space-saving 16-Pin SOIC
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low power "stop mode" in battery operate hand-held applications
- Optional industrial temperature range -40°C to +85°C

PIN CONNECTIONS



PIN NAMES

V_{BAT}	- +3 Volt Battery Input
V_{CCO}	- Switched SRAM Supply Output
V_{CC}	- +5 Volt Power Supply Input
GND	- Ground
PF	- Power Fail (Active High)
$\overline{PF}$	- Power Fail (Active Low)
WC/$\overline{SC}$	- Wake-Up Control (Sleep)
RC	- Reset Control
IN	- Early Warning Input
$\overline{NMI}$	- Non Maskable Interrupt
$\overline{ST}$	- Strobe Input
$\overline{CEO}$	- Chip Enable Output
$\overline{CEI}$	- Chip Enable Input
$\overline{PBRST}$	- Push Button Reset Input
$\overline{RST}$	- Reset Output (Active Low)
RST	- Reset Output (Active High)

DESCRIPTION

The DS1236 Micro Manager provides all necessary functions for power supply monitoring, reset control, and memory back-up in microprocessor based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1236 also provides early warning detection by driving a non maskable

interrupt at a user defined voltage threshold. External reset control is provided by a push-button reset input which is debounced and activates reset outputs. An internal timer also forces the reset outputs to the active state if the strobe input is not driven low prior to time out. Reset control and wake-up/sleep control inputs also provide necessary signals for orderly shut down and start up in battery backup and battery operate applications.

POWER MONITOR

The DS1236 employs a band gap voltage reference and a precision comparator to monitor the 5 volt supply (V_{CC}) in microprocessor based systems. When an out-of-tolerance condition occurs, the RST and $\overline{RST}$ outputs are driven to the active state. The V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1236-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor control as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power up, the RST and $\overline{RST}$ signals are held active for a minimum of 40 ms (60 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize. Note: Operation described above is achieved with the reset control pin (RC) connected to GND. Please review the reset control section for more information.

WATCHDOG TIMER

The DS1236 provides a watchdog timer function by forcing the RST and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is set for 220 ms typically with a maximum time-out of 300 ms. The watchdog timer begins timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time-out, the watchdog timer is reset and begins to time out again. To guarantee the watchdog timer does not time-out, a high-to-low transition must occur at or less than 150 ms from watchdog timer reset. If the watchdog timer is allowed to time out, the RST and $\overline{RST}$ outputs are driven to the active state for 40 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address, data, and/or control signals. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time out. If the watchdog timer is not required, it may be disabled by permanently grounding the In input pin which also disables the $\overline{NMI}$ output. If the $\overline{NMI}$ signal is required, the watchdog may also be disabled by leaving the $\overline{ST}$ input open. The watchdog timer is also disabled as soon as the In input falls to V_{TP} or, if In is not used and grounded, as soon as V_{CC} falls to V_{CCTP}. The watchdog will then become active as V_{CC} rises above V_{CCTP} and the In pin rises above V_{TP}.

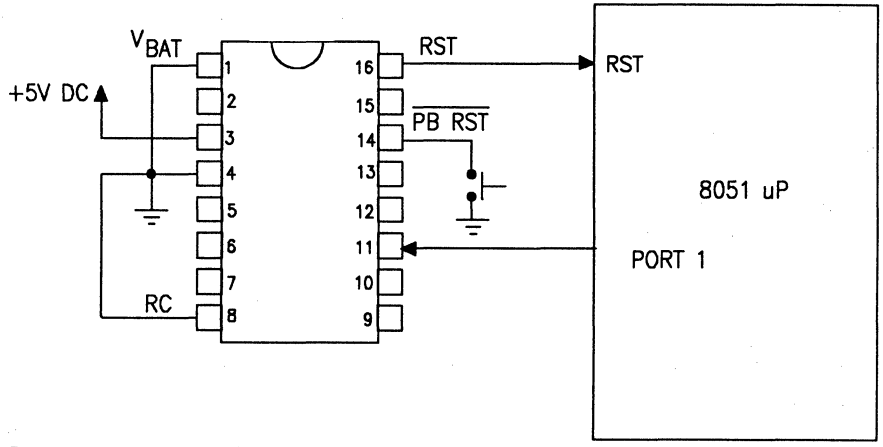
PUSH-BUTTON RESET

An input pin is provided on the DS1236 for direct connection to a push-button. The push-button reset input requires an active low signal. Internally, this input is debounced and timed such that the RST and $\overline{RST}$ outputs are driven to the active state for 40 ms minimum. This 40 ms delay begins as the push-button is released from low level. A typical example of the power monitor, watchdog timer, and pushbutton reset is shown in Figure 2.

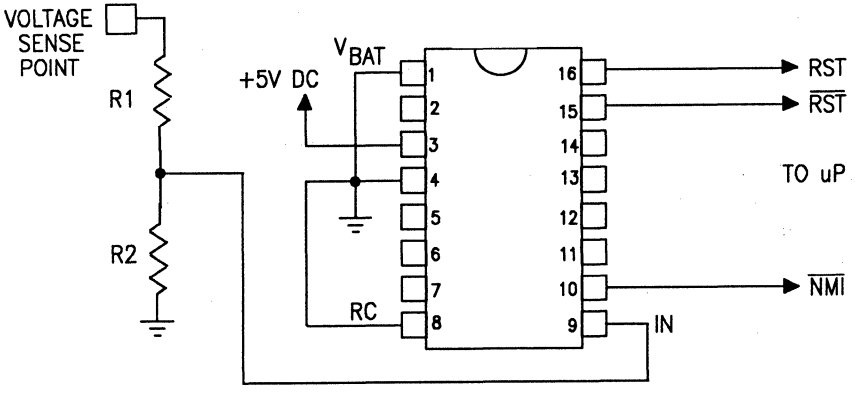
NON MASKABLE INTERRUPT

The DS1236 generates a non maskable interrupt $\overline{NMI}$ for early warning of power failure to a microprocessor. A precision comparator monitors the voltage level at the input pin In relative to a reference generated by the internal band gap. The In pin is a high impedence input allowing for a user defined sense point using a simple resistor voltage divider network (Figure 3) to interface with high voltage signals. This sense point may be derived from the regulated 5 volt supply, or from a higher DC voltage level closer to the AC

POWER MONITOR, WATCHDOG TIMER, AND PUSHBUTTON RESET
Figure 1



NONMASKABLE INTERRUPT Figure 2



$$V_{SENSE} = \frac{R1 + R2}{R2} \times 2.54$$

$$MAX = \frac{V_{SENSE}}{2.54} \times 5.00$$

EXAMPLE 1: 5 VOLT SUPPLY, R2 = 10k OHM, V_{SENSE} = 4.80 VOLTS

$$\therefore\ 4.80 = \frac{R1 + 10K}{10k} \times 2.54 \qquad R1 \cong 8.9K\ OHM$$

EXAMPLE 2: 12 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 9.00 VOLTS

$$\therefore\ 9.00 = \frac{R1 + 10K}{10k} \times 2.54 \qquad R1 \cong 25.4K\ OHM$$

$$V_{MAX} = \frac{9.00}{2.54} \times 5.00 = 17.7\ VOLTS$$

power input. Since the In trip point V_{TP} is 2.54 volts, the proper values for R_1 and R_2 can be determined by the equation as shown. Proper operation of the DS1236 requires that the voltage at the In pin be limited to 5 volts maximum. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown. A simple approach to solving this equation is to select a value for R_2 of high enough impedence to keep power consumption low, and solve for R_1. The flexibility of the In input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$. When the supply being monitored decays to the voltage sense point, the DS1236 drives the $\overline{NMI}$ output to the active state for a minimum of 200 ms but does not hold it active. If the In pin is connected to V_{CC}, the $\overline{NMI}$ output will pulse low as V_{CC} decays to V_{CCTP} is RC pin is at ground (see reset control section). $\overline{NMI}$ will not pulse low if the RC pin is connected to V_{CCO}. The $\overline{NMI}$ power fail detection circuitry also has built in time domain hysterisis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 47 KHz (20 ms/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the In pin to active $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 60 ms or the comparator will reset.

MEMORY BACKUP

The DS1236 provides all necessary functions required to battery back up a static RAM. First, a switch is provided to direct power from the incoming 5 volt supply (V_{CC}) or from a battery (V_{BAT}) whichever is greater. This switched supply (V_{CCO}) can also be used to battery back CMOS microprocessors. Please review the reset control and wake control sections regarding nonvolatile microprocessor applications. Second, the same power fail detection described in the power monitor section is used to inhibit the chip enable input ($\overline{CEI}$) and hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or battery supply. This write protection mechanism occurs as V_{CC} falls below V_{CCTP} as specified previously. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or if $\overline{CEI}$ is held low, $\overline{CEO}$ is held active for t_{CE} maximum. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 4 shows a typical nonvolatile SRAM application. If nonvolatile operation is not required, the battery input pin V_{BAT} must be grounded. In order to conserve battery capacity during storage and/or shipment of a system, the DS1236 provides a freshness seal to electronically disconnect the battery. Figure 5 depicts the three pulses below ground on the In pin required to invoke the freshness seal. The freshness seal will be disconnected and normal operation will begin when V_{CC} is next applied to a level above V_{CCTP}.

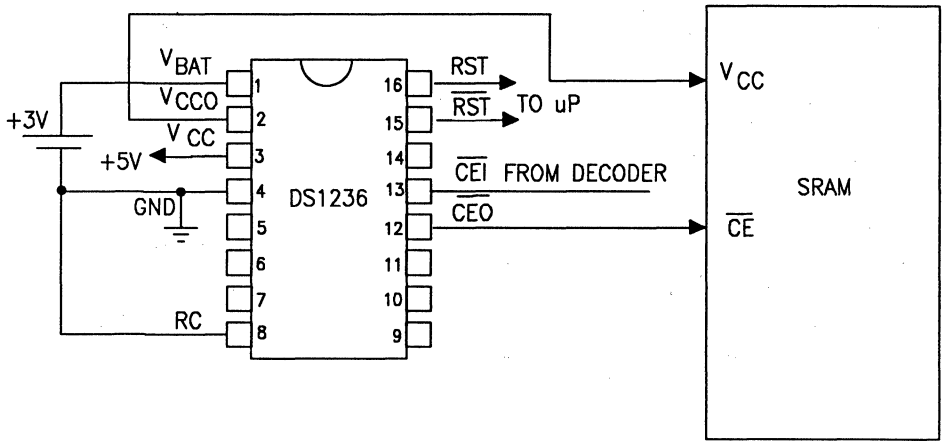
POWER SWITCHING

For certain high current battery backup applications, the 5 volt supply and battery supply switches internal to the DS1236 may not be large enough to support the given load within significant voltage drop. For these applications, the PF and $\overline{PF}$ outputs are provided to gate external switching devices to switch supply from V_{CC} to battery on power down and from battery to V_{CC} on power up. The transition threshold for PF and $\overline{PF}$ is set to the external battery voltage V_{BAT} (see Figure 6). The load applied to the PF pin from the external switch will be supplied by the battery. Therefore, this load should be taken into consideration when sizing the battery.

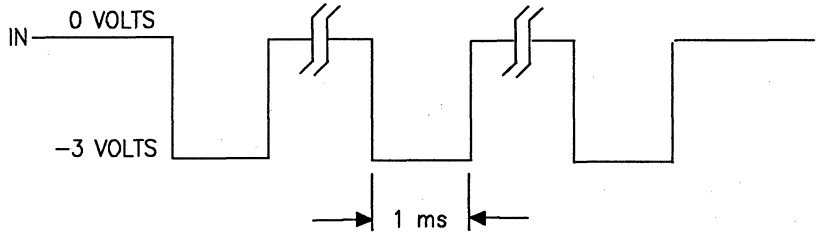
RESET CONTROL

Two modes of operation on power down and power up are available depending upon the level

NONVOLATILE SRAM Figure 3

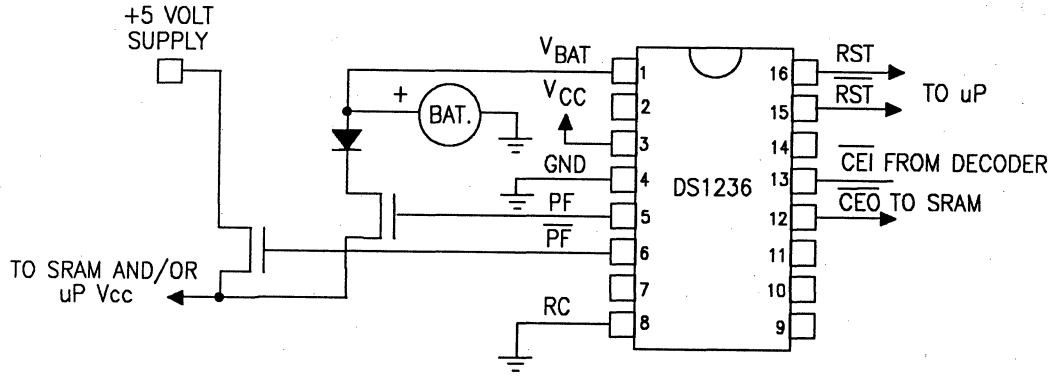


FRESHNESS SEAL Figure 4



NOTE: THIS SERIES OF PULSES MUST BE APPLIED DURING NORMAL 5 VOLT OPERATION

POWER SWITCHING Figure 5



NOTE: Underwriters Laboratories requires a series diode in the battery path for primary cell applications.

of the reset control (RC) input pin. The level of this pin distinguishes timing and level control on RST, $\overline{RST}$, and $\overline{NMI}$ outputs for volatile processor operation versus non-volatile battery backup or battery operate processor applications. With the RC pin tied to ground, operation is as described in the power monitor section where non-volatile processor functionality is not required. Notice that upon V_{CC} out of tolerance at V_{CCTP} the RST and $\overline{RST}$ outputs are driven active within t_{RPD} and that RST and $\overline{NMI}$ follow V_{CC} as the supply decays (see timing diagram). Also, on power up, RST follows V_{CC} and $\overline{RST}$ is held active and both remain active for t_{RST} after valid V_{CC}. $\overline{NMI}$ will pulse low for 500 ms maximum then will follow V_{CC}. With the RC pin tied to V_{CCO}, RST and $\overline{RST}$ are not forced active as V_{CC} collapses to V_{CCTP}, and $\overline{RST}$ is held at a high level by the battery as V_{CC} falls below battery potential. This mode of operation is intended for applications in which the processor is made non-volatile with an external source and allows the processor to power down into a "stop" mode as signaled from $\overline{NMI}$ at an earlier voltage level. The $\overline{NMI}$ output pin will pulse low for t_{NMI} following a low voltage detect at the in pin of V_{TP}. However, $\overline{NMI}$ will also be held at a high level following t_{NMI} by the battery as V_{CC} decays below V_{BAT}. On power up, RST and $\overline{RST}$ are held inactive until V_{CC} reaches power valid V_{CCTP}, then RST and $\overline{RST}$ are driven active for t_{RST}. $\overline{NMI}$ will pulse low for 500 ms maximum then will follow V_{CC} during the power up sequence thus, once $\overline{NMI}$ is driven active, the processor may power down into a "stop" mode and subsequently restarted by any of several different signals. If V_{CC} does not fall below V_{CCTP}, the processor will be restarted by the reset derived from the watchdog timer as the IN input rises above V_{TP}. If V_{CC} falls below V_{CCTP} but not below V_{BAT}, the processor will be restarted as V_{CC} rises above V_{CCTP}. If V_{CC} falls below V_{BAT}, the reset outputs will be forced active the next time V_{CC} rises above V_{CCTP} as shown in th power up timing diagram. If the In pin falls below V_{TP} during an active reset, the reset outputs will be forced inactive by the $\overline{NMI}$ output. An additional $\overline{NMI}$ pulse for "stop" mode control will follow the initial $\overline{NMI}$, by stimulation of the $\overline{ST}$ input, at t_{STN}. The $\overline{PBRST}$ input may be used at any time V_{CC} is above V_{BAT} to drive the reset outputs and thus restart the processor. Please review the power down and power up timing diagrams for RC=GND and RC=V_{CCO} for further information.

WAKE CONTROL/SLEEP CONTROL

The Wake/Sleep Control input WC/$\overline{SC}$ allows the processor to disable all comparators on the DS1236 before entering the "stop" mode. This feature allows the DS1236, processor, and non-volatile static RAM to maintain nonvolatility in the lowest power mode possible. The processor may invoke the sleep mode in battery operate applications to conserve capacity when an absence of activity is detected. The DS1236 may subsequently be restarted by a high to low transition on the $\overline{PBRST}$ input via human interface by a keyboard, touch pad, etc. The processor will then be restarted as the watchdog timer times out and drives RST and $\overline{RST}$ active. The DS1236 can also be woken up by forcing the WC/$\overline{SC}$ pin high from an external source. Also, if the DS1236 is placed in a sleep mode by the processor, and system power is lost, the DS1236 will wake up the next time V_{CC} rises above V_{CCTP}. Remember, when the processor invokes the sleep mode during normal power valid operation, all operation on the DS1236 is disabled, thus leaving the $\overline{NMI}$, RST and $\overline{RST}$ outputs disabled as well as the $\overline{ST}$ and In inputs. The $\overline{PBRST}$ input will also become inactive when the main battery supply falls below the In input at V_{TP} or the backup 3 volt supply at V_{BAT}. Subsequent power up with a new main battery supply will activate the RST and $\overline{RST}$ outputs as the main supply rises above V_{CCTP}. Please review the timing diagram for wake/sleep control. A high to low transition on the WC/$\overline{SC}$ pin must follow a high to low transition on the $\overline{ST}$ pin by t_{WC} to invoke a "sleep" mode for the DS1236.

ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON ANY PIN RELATIVE TO GROUND - -1.0V TO +7.0V
OPERATING TEMPERATURE - 0° TO 70°C
STORAGE TEMPERATURE - -55° TO +125°C
SOLDERING TEMPERATURE - 260° FOR 10 SECONDS

RECOMMENDED D.C. OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	V_{cc}	4.5	5.0	5.5	V	1
Supply Voltage (5% option)	V_{cc}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{cc}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}			V_{cc}	V	1
Battery Input	V_{BAT}	2.7		4.0	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C TO 70°C, V_{cc} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Current	I_{CC}			5	mA	2
Supply Current Output	I_{CC01}			100	mA	3
Supply Voltage Output	V_{CCO}	V_{CC}-0.3			V	1
Input Leakage	I_{LI}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
Output Current @ 0.4V	I_{OL}			4.0	mA	12
Output Current @ 2.4V	I_{OH}	-1.0			mA	13
Power Supply Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip Point (5% option)	V_{CCTP}	4.50	4.62	4.75	V	1
IN Input Pin Current	I_{CCIN}			0.1	uA	
IN Input Trip Point	V_{TP}	2.5	2.54	2.6	V	1

A.C. ELECTRICAL CHARACTERISTICS

(0°C TO 70°C, V_{cc} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC} Fail Detect to RST, $\overline{RST}$	t_{RPD}		50	100	us	
V_{TP} to $\overline{NMI}$	t_{IPD}	30	50	100	us	
RESET Active Time	t_{RST}	40	60	80	ms	
$\overline{NMI}$ Pulse Width	t_{NMI}	200	300	500	us	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	
$\overline{PB\ RST}$ @ V_{IL}	t_{PB}	30			ms	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	300			us	
Chip Enable Propagation Delay	t_{PD}			20	ns	
Chip Enable High to V_{CC} Fail	t_{CF}			20	ns	
V_{CC} Valid to (RST & $\overline{RST}$ RC=1)	t_{FPU}			100	ns	
V_{CC} Valid to RST & $\overline{RST}$	t_{RPU}	40	60	80	ms	5
V_{CC} Slew 4.25V to V_{BAT}	t_{FB1}	10			us	7
V_{CC} Slew 4.25 to V_{BAT}	t_{FB2}	100			us	8
Chip Enable Output Recovery	t_{REC}	80			ms	9
V_{CC} Slew 4.25V to 4.75V	t_R	0			us	
Chip Enable Pulse Width	t_{CE}			5	us	10
Watch Dog Time Delay	t_{TD}	150	220	300	ms	
$\overline{ST}$ to WC/$\overline{SC}$	t_{WC}	0.1		50	us	
V_{BAT} Detect to PF, $\overline{PF}$	t_{PPF}			2	us	7
$\overline{ST}$ to $\overline{NMI}$	t_{STN}			30	ns	11
$\overline{NMI}$ to RST & $\overline{RST}$	t_{NRT}			30	ns	

D.C. ELECTRICAL CHARACTERISTICS

($0^{o}C$ TO $70^{o}C$, $V_{cc} < V_{BAT}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Battery Backup Current	I_{CCO2}			1.0	mA	4
Battery Backup Voltage	V_{CCO}	V_{BAT}-0.7			V	1,6
Battery Current	I_{BAT}			0.1	uA	2
$\overline{CE_o}$ and PF Output Voltage	V_{OHL}	V_{BAT}-0.7			V	1,6

CAPACITANCE

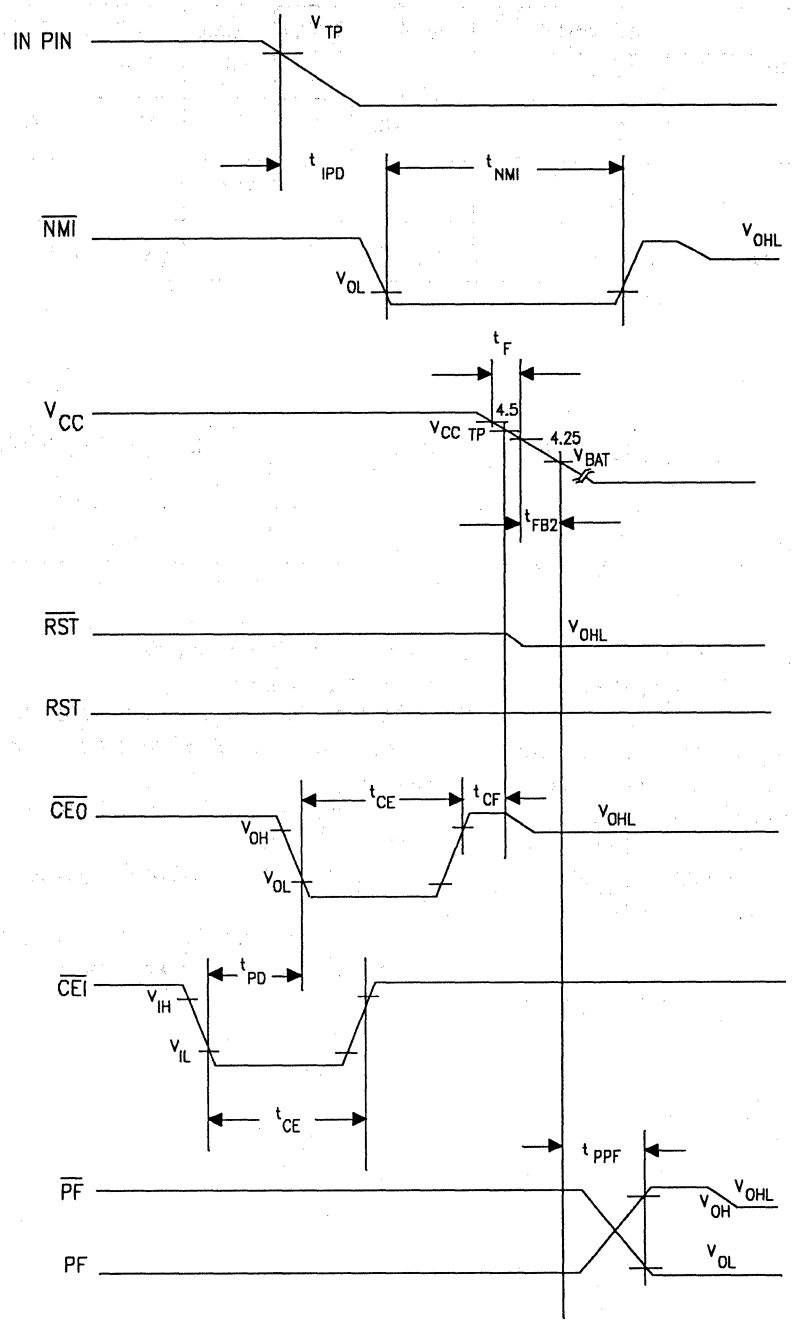
($t_A = 25^{o}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

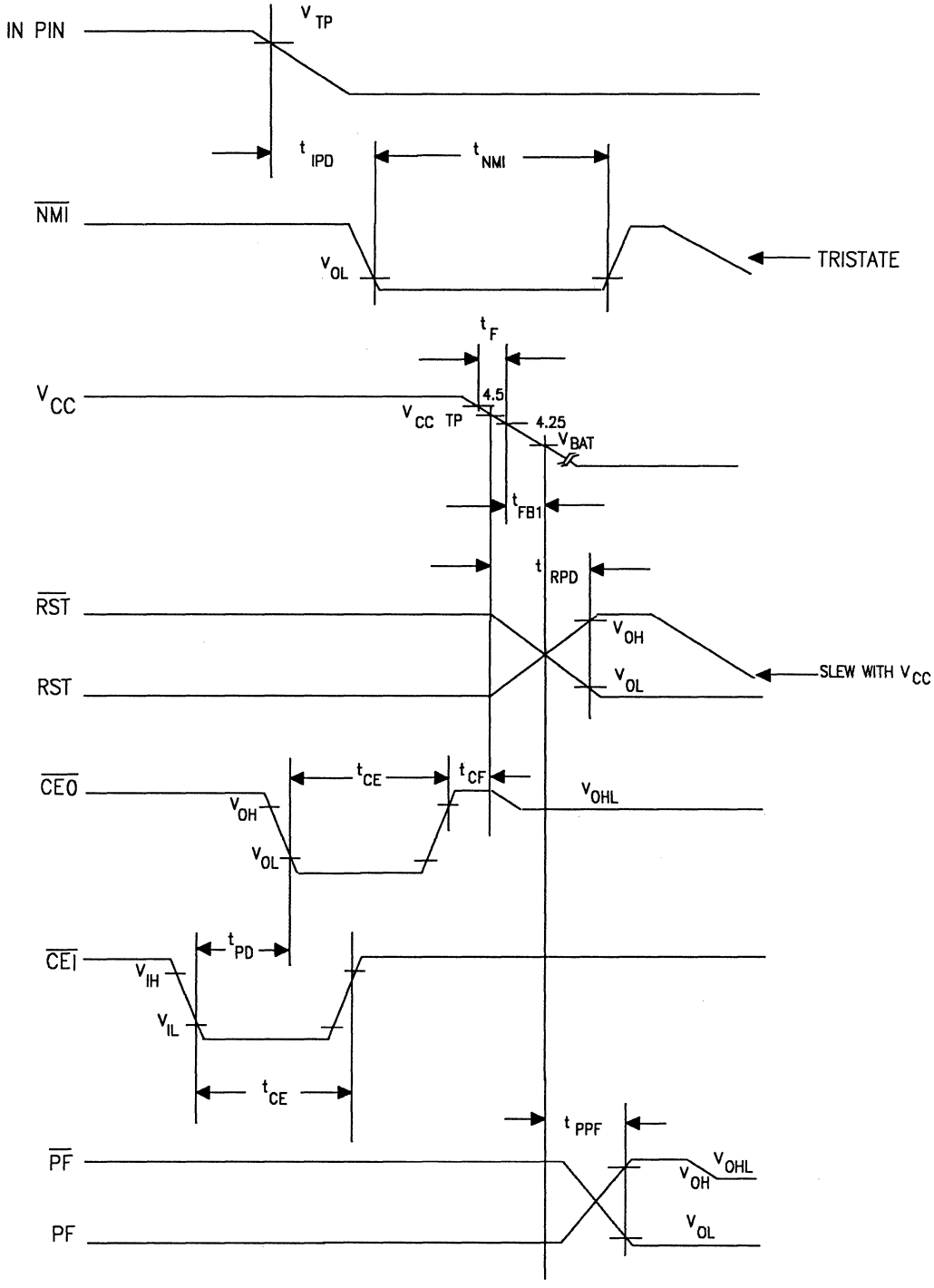
1. All voltages referenced to ground.
2. Measured with V_{CCO} pin, $\overline{CEO}$ pin, PF pin, and $\overline{NMI}$ pin open.
3. I_{CCO1} is the maximum average load which the DS1236 can supply at V_{CC}-.3V through the V_{CCO} pin during normal 5 volt operation.
4. I_{CCO2} is the maximum average load which the DS1236 can supply through the V_{CCO} pin during data retention battery supply operation.
5. With t_R = 5 *us*
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 *ua* load.
7. Sleep mode is not invoked.
8. Sleep mode is invoked.
9. t_{REC} is the minimum time required before memory access to allow for deactivation of RST and $\overline{RST}$.
10. t_{CE} maximum must be met to insure data integrity on power loss
11. In input is less than V_{TP} but V_{CC} greater than V_{CCTP}
12. All outputs except RST which is 50 *ua* max.
13. All outputs except $\overline{RST}$ which is 50 *ua* min.

POWER DOWN - RESET CONTROL = V_{cco} Figure 6

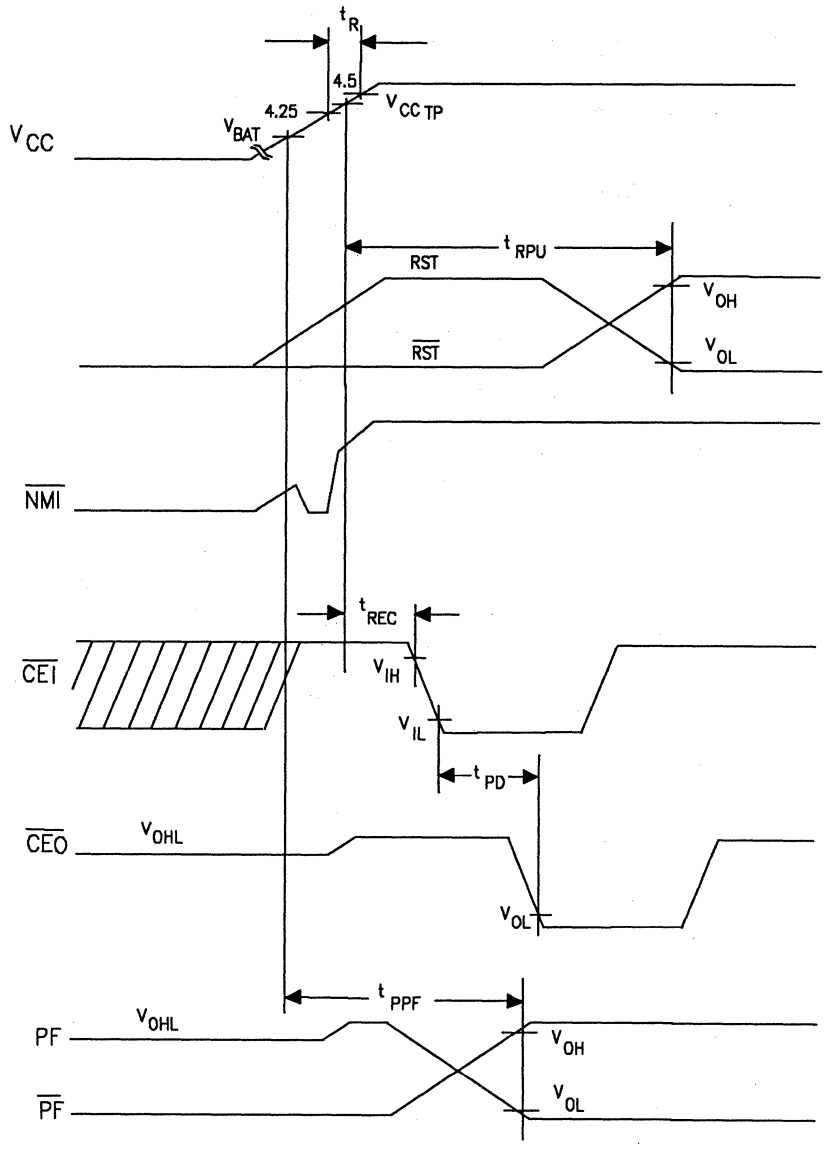


NOTE: If $\overline{RST}$ and RST are active due to pushbutton or watchdog, $\overline{NMI}$ occurance will restore $\overline{RST}$ and RST to an inactive condition . As long as an $\overline{NMI}$ condition exist $\overline{RST}$ and RST cannot occur.

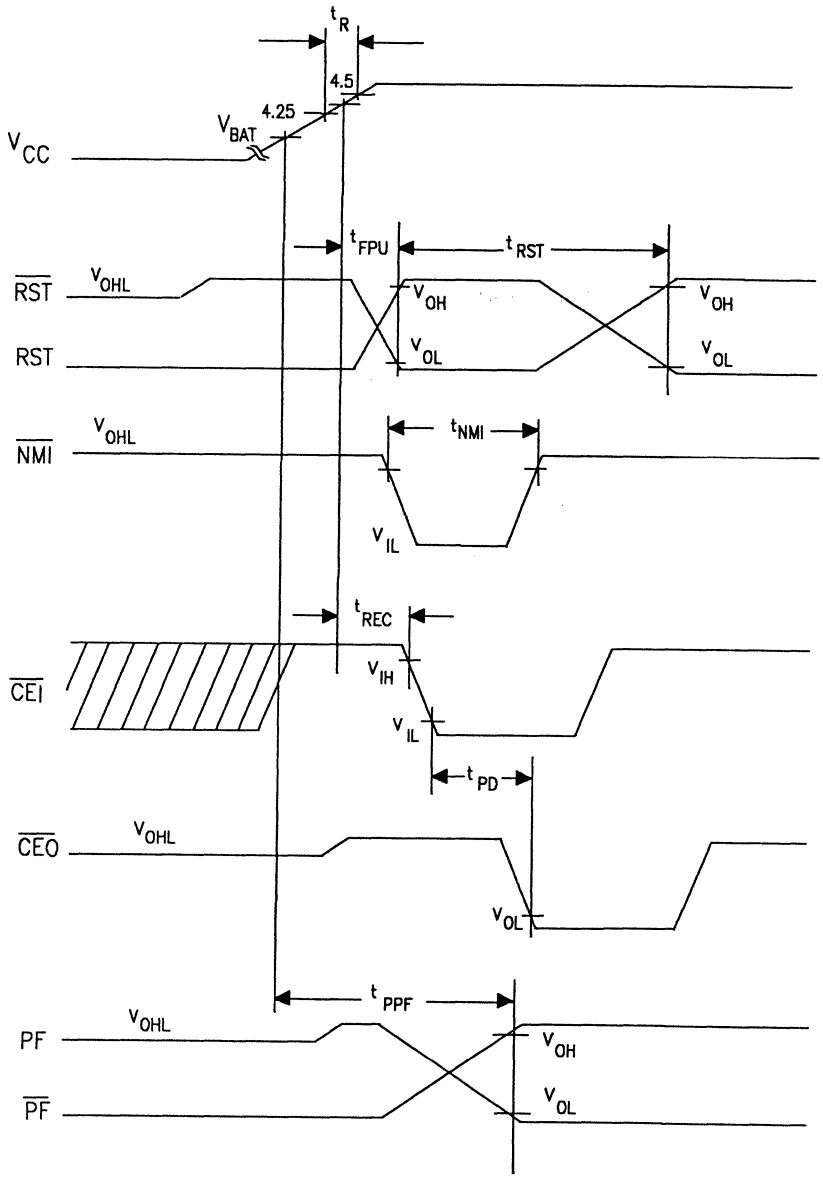
POWER DOWN: RESET CONTROL = GND Figure 7



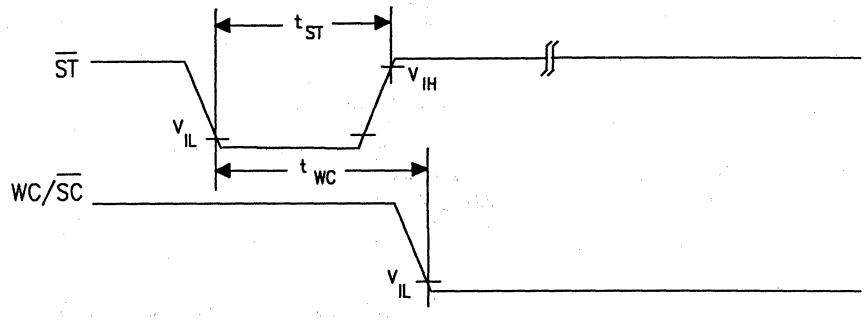
POWER UP - RESET CONTROL = GND Figure 8



POWER UP: RESET CONTROL = V_{CCO} Figure 9

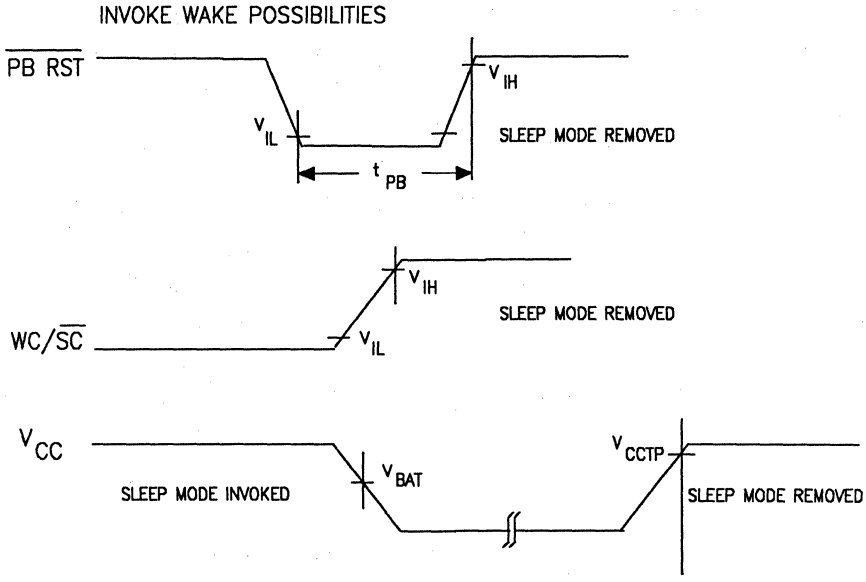


WAKE/SLEEP CONTROL Figure 10

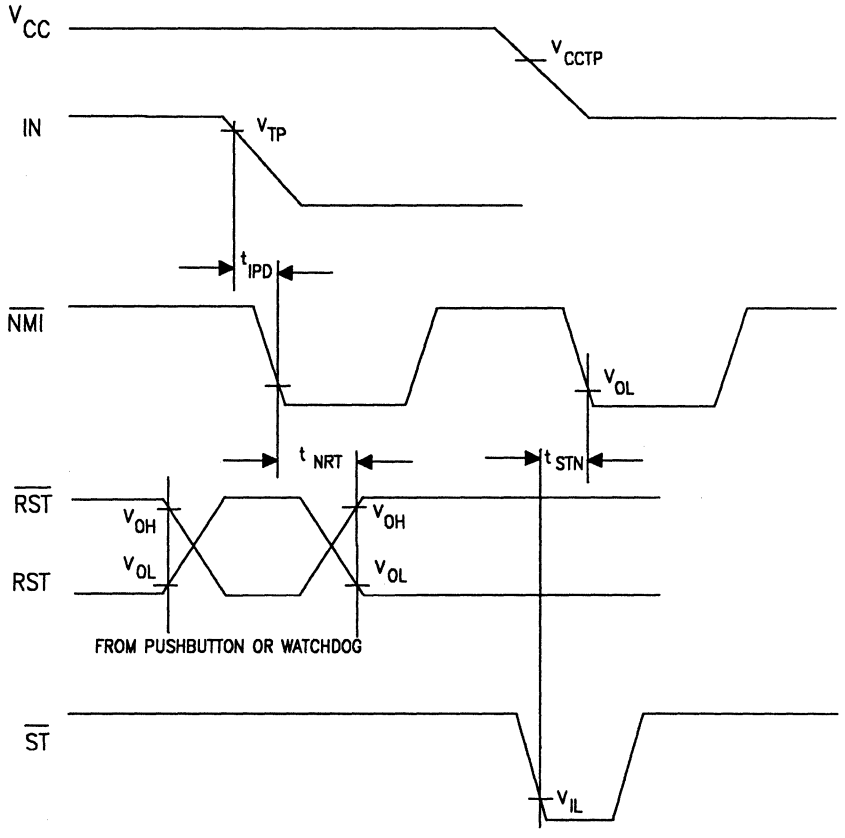


NOTE: Sleep mode will disable $\overline{NMI}$

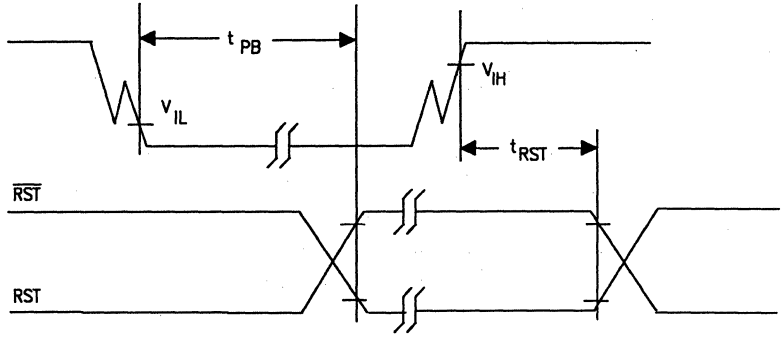
INVOKE WAKE POSSIBILITIES Figure 11



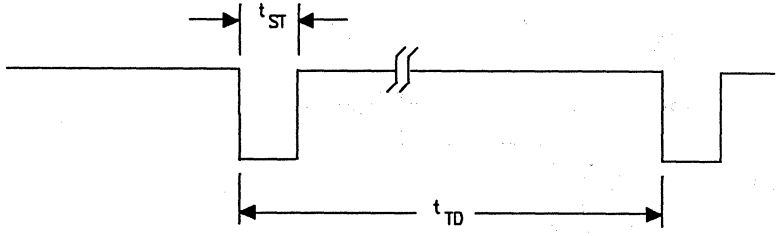
$\overline{\text{NMI}}$ FROM $\overline{\text{ST}}$ Figure 12



PUSHBUTTON RESET Figure 13

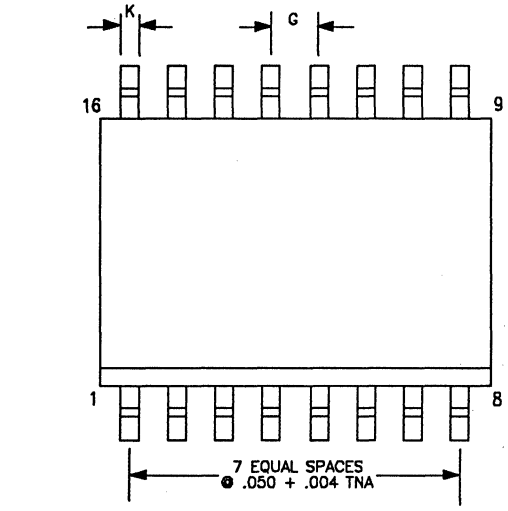


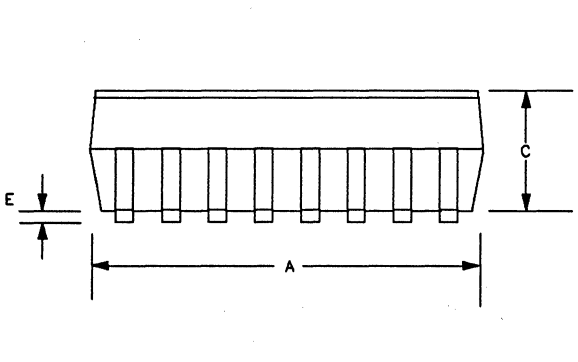
STROBE INPUT Figure 14

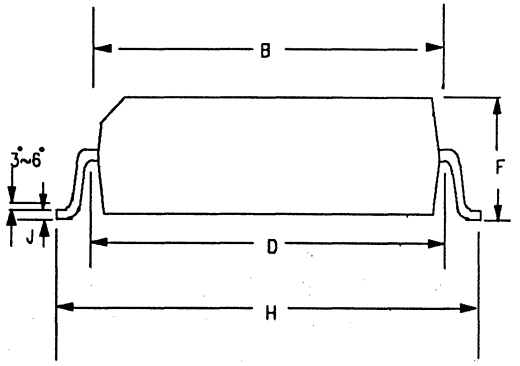


MICRO MANAGER
DS1236
16-Pin SOIC

DIM	INCHES	
	MIN.	MAX.
A	0.403	0.411
B	0.290	0.296
C	0.089	0.095
D	0.325	0.330
E	0.008	0.012
F	0.097	0.105
G	0.046	0.054
H	0.320	0.370
J	0.006	0.011
K	0.013	0.019





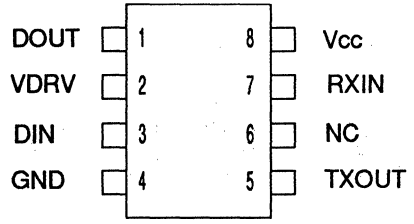


Dallas Semiconductor
Line-Powered RS-232 Transceiver

PRELIMINARY
DS1275 8-pin DIP
DS1275S 8-pin SOIC

FEATURES
- Low-power serial transmitter/receiver for battery-backed systems
- Transmitter steals current from receive signal to save power
- Variable transmitter level from +5 to +12 volts
- Compatible with RS-232 signals
- 8-pin, 150 mil wide SOIC package
- Low-power CMOS

PIN DESCRIPTION

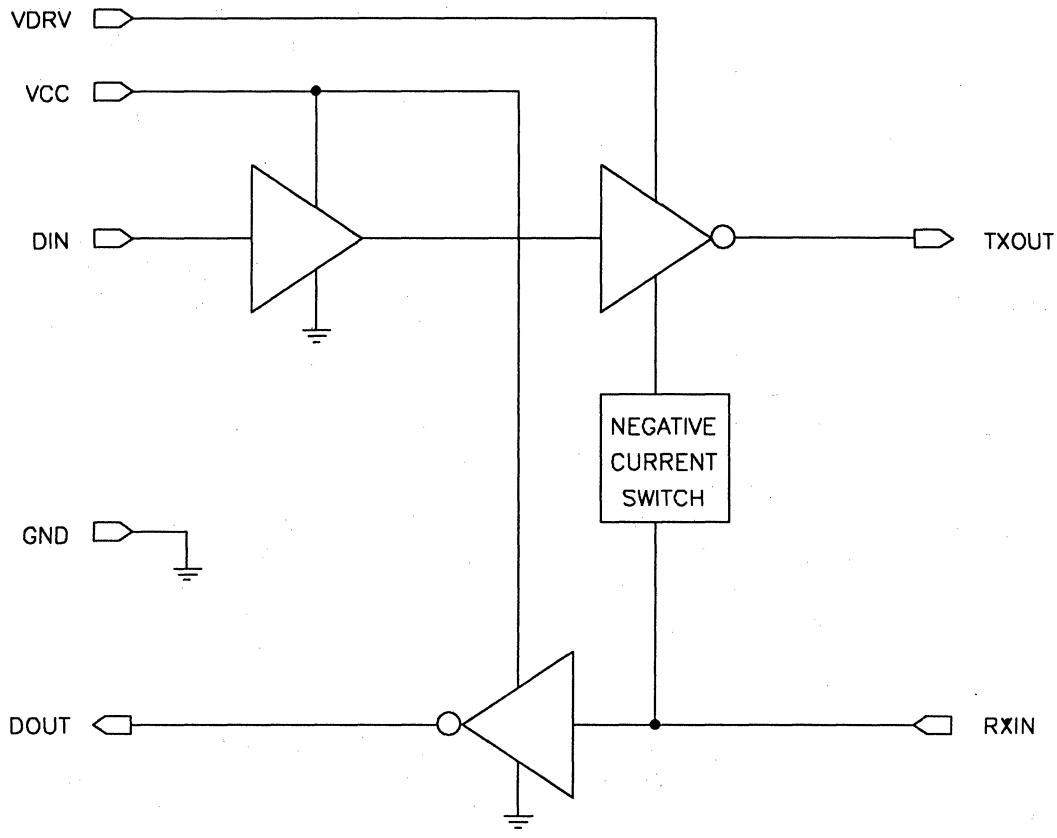


PIN NAMES

DOUT	- Digital data out
VDRV	- Transmit driver +Vcc
DIN	- Digital data in
GND	- System ground (0V)
TXOUT	- Transmit RS-232 out
N.C.	- No connection
RXIN	- Receive RS-232 in
Vcc	- System logic supply (+5V)

DESCRIPTION
The DS1275 is a CMOS device that provides a low-cost, very low-power interface to RS-232 serial ports. The receiver input translates RS-232 signal levels to common CMOS/TTL levels. The transmitter employs a unique circuit which steals current from the receive RS-232 signal when that signal is in a negative state (marking). Since most serial communication ports remain in a negative state statically, using the receive signal for negative power greatly reduces the DS1275's static power consumption. This feature is especially important for battery-powered systems such as laptop computers, remote sensors and portable medical instruments. During an actual communication session, the DS1275's transmitter will use system power (5-12 volts) for positive transitions while still employing the receive signal for negative transitions.

DS1275 BLOCK DIAGRAM Figure 1



OPERATION

Designed for the unique requirements of battery-backed systems, the DS1275 provides a low-power interface to an RS-232 serial port. Typically, a designer must use an RS-232 device which uses his system power during both negative and positive transitions of the transmit signal to the RS-232 port. If the connector to the RS-232 port is left connected for an appreciable time after the communication session has ended, power will statically flow into that port, draining the battery-capacity. The DS1275 eliminates this static current drain by stealing current from the receive line (RXIN) of the RS-232 port when that line is at a negative level (marking). Since most asynchronous communication over an RS-232 connection typically remains in a marking state when data is not being sent, the DS1275 will not consume system power in this condition. System power would only be used when positive-going transitions are needed on the transmit RS-232 output (TXOUT) when data is sent. However, since asynchronous communication sessions typically exhibit a very low duty-cycle, overall system power consumption remains low.

RECEIVER SECTION

The RXIN pin is the receive input for an RS-232 signal whose levels can range from ± 3 to ± 25 volts. A negative signal is called a mark while a positive signal is called a space. These signals are inverted and then level-shifted to normal +5 volt CMOS/TTL logic levels. The logic output associated with RXIN is DOUT which swings from +VCC to ground. Therefore, a mark on RXIN produces a logic 1 at DOUT; a space produces a logic 0.

The input threshold of RXIN is typically around 1.8 volts with 500 millivolts of hysteresis to improve noise rejection. Therefore, an input positive-going signal must exceed 1.8 volts to cause DOUT to switch states. A negative-going signal must now be lower than 1.3 volts to cause DOUT to switch again. An open on RXIN is interpreted as a mark, producing a logic 1 at DOUT.

TRANSMITTER SECTION

DIN is the CMOS/TTL compatible input for digital data from the user system. A logic one at DIN produces a mark at TXOUT while a logic 0 produces a space. As mentioned earlier, the transmitter section employs a unique driver design that uses the RXIN line for swinging to negative levels (marking). The RXIN line must be in a marking or idle state to take advantage of this design; if RXIN is in a spacing state, TXOUT will only swing to ground. When TXOUT needs to transition to a positive level, it uses the VDRV power pin for this level. VDRV can be a voltage supply from between 5 to 12 volts although in many situations it can be tied directly to the +5 volt VCC supply. *It is important to note that VDRV must be greater than or equal to VCC at all times.*

The voltage range on VDRV permits the use of a 9 volt battery in order to provide a higher voltage level when TXOUT is in a space state. When VCC is shut off to the DS1275 and VDRV is still active (as might happen in a battery-backed condition), no current will be drawn from VDRV if TXOUT is floating. If TXOUT is loaded during such a condition, VDRV will not draw current *only* if RXIN is in a negative state. During normal operation (VCC=5 volts), VDRV will draw about 1 uA when TXOUT is marking. Of course, when TXOUT is spacing, VRDV will draw substantially more current -- about 5-10 mA depending upon its voltage and the impedance that TXOUT sees.

The TXOUT output is slew-rate limited to less than 30 volts/us in accordance with RS-232 specifications. In the event TXOUT should be inadvertantly shorted to ground, internal current-limiting circuitry prevents damage, even if continously shorted.

RS-232 COMPATIBILITY

The intent of the DS1275 is not so much to meet <u>all</u> the requirements of the RS-232 specification as to offer a low-power solution that will work with most RS-232 ports with a connector length of less than 10 feet. As a prime example, the DS1275 will not meet the RS-232 requirement that the signal levels be at least + or - 5 volts minimum when terminated by a 3 Kohm load and VDRV= +5 volts. Typically a voltage of 4 volts will be present at TXOUT when spacing. However, since most RS-232 receivers will correctly interpret any voltage over 2 volts as a space, there will be no problem transmitting data.

ABSOLUTE MAXIMUM RATINGS

Vcc	+7 volts
VDRV	+13 volts
RXIN	+ or - 15 volts
DIN	-0.3 to VCC+0.3 volts
TXOUT	+ or - 15 volts
DOUT	-0.3 to VCC+0.3 volts
Storage temperature	-55 to 125 deg C
Operating temperature	0 - 70 deg C

RECOMMENDED D.C. OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic supply	VCC	4.5	5.0	5.5	volts	1
Transmit driver supply	VDRV	4.5	5.0	13.0	volts	1
Logic 1 Input	VIH	2.0		VCC+0.3	volts	2
Logic 0 Input	VIL	-0.3		0.8	volts	
RS-232 Input range (RXIN)	VRS	-15		+15	volts	

NOTES

1. VDRV must be greater than or equal to VCC.
2. VCC=VDRV= 5V ± 10%.

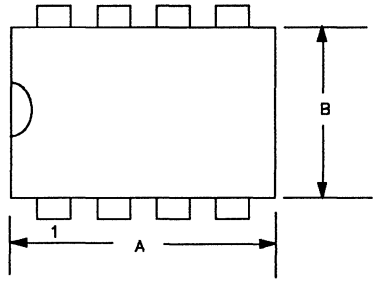
D.C. ELECTRICAL CHARACTERISTICS 0°to 70°C, Vcc=VDRV=+5V ±10%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TXOUT level high	V_{OTXH}	3.5	4.0		volts	3
TXOUT level low	V_{OTXL}	-8.5	-9.0		volts	4
TXOUT output short-circuit	I_{SC}		±20		mA	
TXOUT output slew rate	t_{SR}			30	V/us	
Propagation delay	t_{PD}		3		us	5
RXIN input threshold low	V_{TL}		1.3		volts	
RXIN input threshold high	V_{TH}		1.8		volts	
DOUT output current @2.4 V	V_{OH}	-1.0			mA	
DOUT output current @ 0.4 V	V_{OL}			3.2	mA	

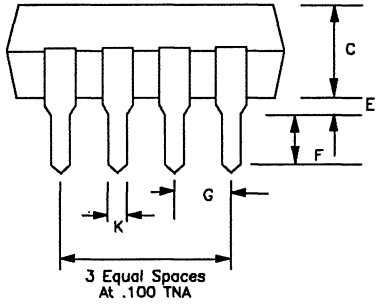
NOTES

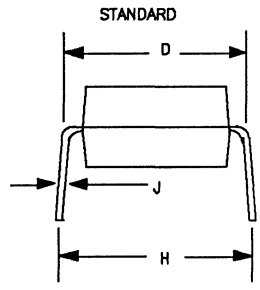
3. DIN = VIL.
4. DIN = VIH and RXIN = -10 volts.
5. DIN to TXOUT or RXIN to DOUT.

LINE-POWERED RS-232 TRANSCEIVER
DS1275
8-PIN DIP



DIM	INCHES	
	MIN.	MAX.
A	0.345	0.400
B	0.240	0.260
C	0.120	0.140
D	0.290	0.310
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	0.320	0.370
J	0.008	0.012
K	0.015	0.021
L	0.040	0.060
M	0.370	0.420
N	0.160	0.180

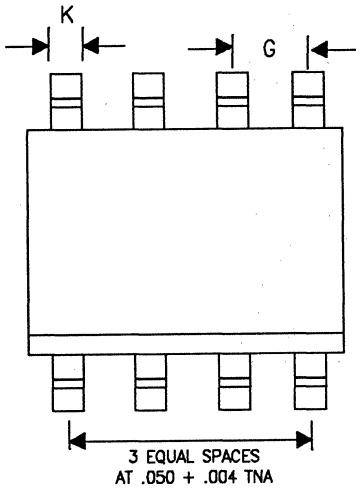


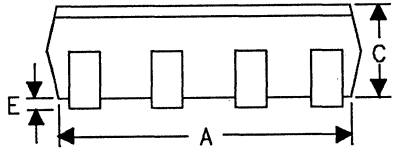


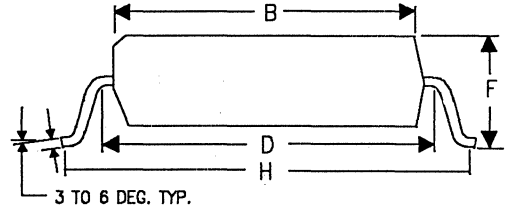
1

LINE-POWERED RS-232 TRANSCEIVER
DS1275S
8-PIN SOIC

DIM	INCHES	
	MIN.	MAX.
A	0.188	0.195
B	0.151	0.157
C	0.052	0.058
D	0.175	0.193
E	0.004	0.010
F	0.058	0.064
G	0.046	0.054
H	0.228	0.240
J	0.006	0.011
K	0.013	0.019







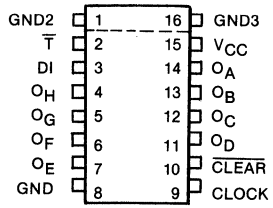
Dallas Semiconductor
Eliminator

DS1290
DS1291

FEATURES

- Replaces 8 hard-to-get-at manual switches
- Option printed circuit board via software
- DS1290 remembers settings in the absence of power
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Interface
- Low power CMOS
- DS1291 Volatile Eliminator
- Change of switch settings occur simultaneously
- Over 10 years of data retention

PIN CONNECTIONS



PIN NAMES

$\overline{T}$	- Transfer
DI	- Data Input
O_AO_H	- Switch Outputs
CLOCK	- Clock Input
$\overline{CLEAR}$	- All Outputs Set Low
V_{CC}	- +5 Volts
GND	Ground
GND2	- Missing on DS1290 Must Be Grounded on DS1291
GND3	- Missing on DS1290 Must Be Grounded on DS1291

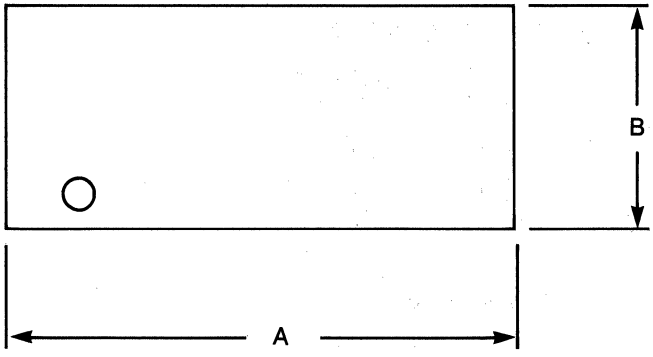
DESCRIPTION

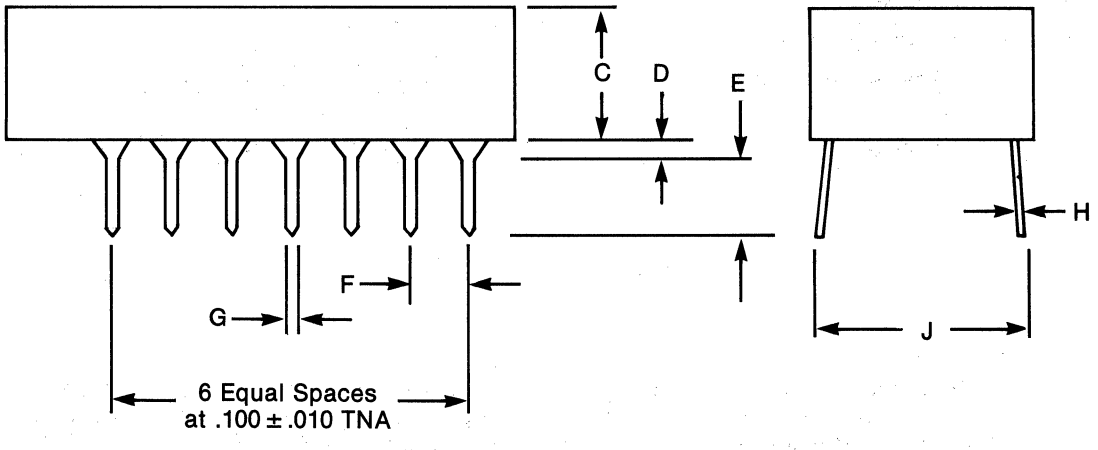
The DS1290 Eliminator replaces manual switches used to option printed circuit boards. Eight output pins can be set to a logic level or interrogated by three signals, clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1290 will maintain high or low level output duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

See the data sheet for the DS1292 for electrical specifications and operation.

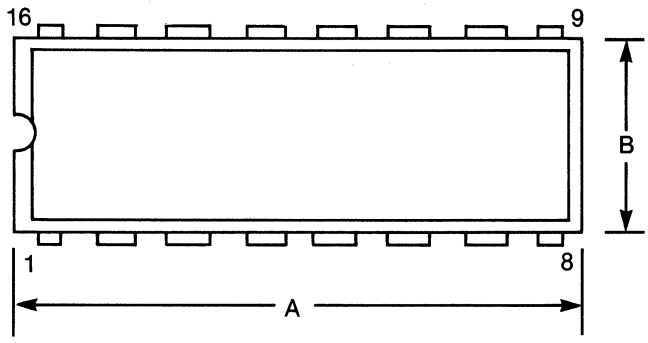
Nonvolatile Eliminator
DS1290

DIM.	INCHES	
	MIN.	MAX.
A	.840	.860
B	.370	.390
C	.230	.265
D	.020	.040
E	.115	.135
F	.090	.110
G	.015	.021
H	.008	.012
J	.320	.370

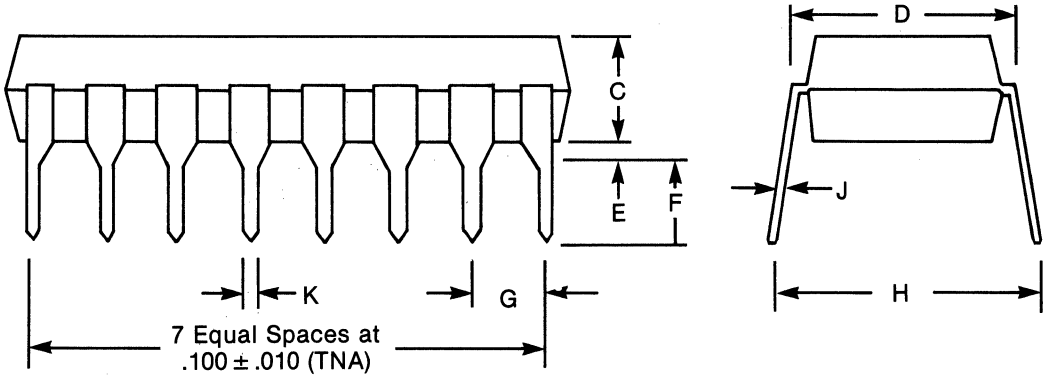




Volatile Eliminator
DS1291
16-Pin DIP



DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021



1

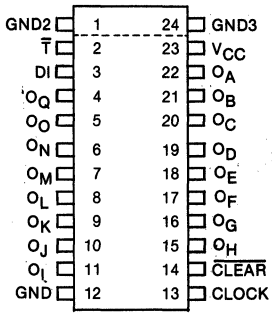
Dallas Semiconductor
Eliminator

DS1292
DS1293

FEATURES

- Replaces 16 hard-to-get-at manual switches
- Option printed circuit board via software
- DS1292 remembers settings in the absence of power
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Interface
- Low power CMOS
- DS1293 Volatile Eliminator
- Change of switch settings occur simultaneously
- **Over 10 years of data retention**

PIN CONNECTIONS



PIN NAMES

$\overline{T}$	- Transfer
DI	- Data Input
$O_A O_Q$	- Switch Outputs
CLOCK	- Clock Input
$\overline{CLEAR}$	- All Outputs Set Low
V_{CC}	- +5 Volts
GND	- Ground
GND2	- Missing on DS1292 Must Be Grounded on DS1293
GND3	- Missing on DS1292 Must Be Grounded on DS1293

DESCRIPTION

The DS1292 Eliminator replaces manual switches used to option printed circuit boards. Sixteen output pins can be set to a logic level or interrogated by three signals, clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1292 will maintain high or low level output duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

OPERATION

The DS1292/DS1293 Eliminator is a 16-bit shift register which has a clocked serial input, an asynchronous clear, and an output transfer control (see Block Diagram, Figure 1). Data can be entered into the 16-bit register only when the transfer input ($\overline{T}$) is at a high level. While at a high level the transfer function allows serial entry of data via the data input pin (DI). The outputs 0_Q through 0_B remain in the state which was set prior to $\overline{T}$ being driven to a high level. Output 0_A will change state as new data is entered. This output provides a method of "feeding back" actual output settings prior to setting the $\overline{T}$ input low (Figure 2). When the $\overline{T}$ input is driven low, new data which has been input into the 16-bit shift register is now locked at outputs 0_Q through 0_A. When the $\overline{T}$ input is low, all clock and data inputs are ignored. Valid data is clocked into the eliminator while $\overline{T}$ is high on the low-to-high transition of the CLOCK input. Data may be changed while the CLOCK input is high or low, but only data meeting the setup requirements will enter the shift register. The $\overline{CLEAR}$ input will always set all outputs to low level regardless of the level of the CLOCK or $\overline{T}$ input.

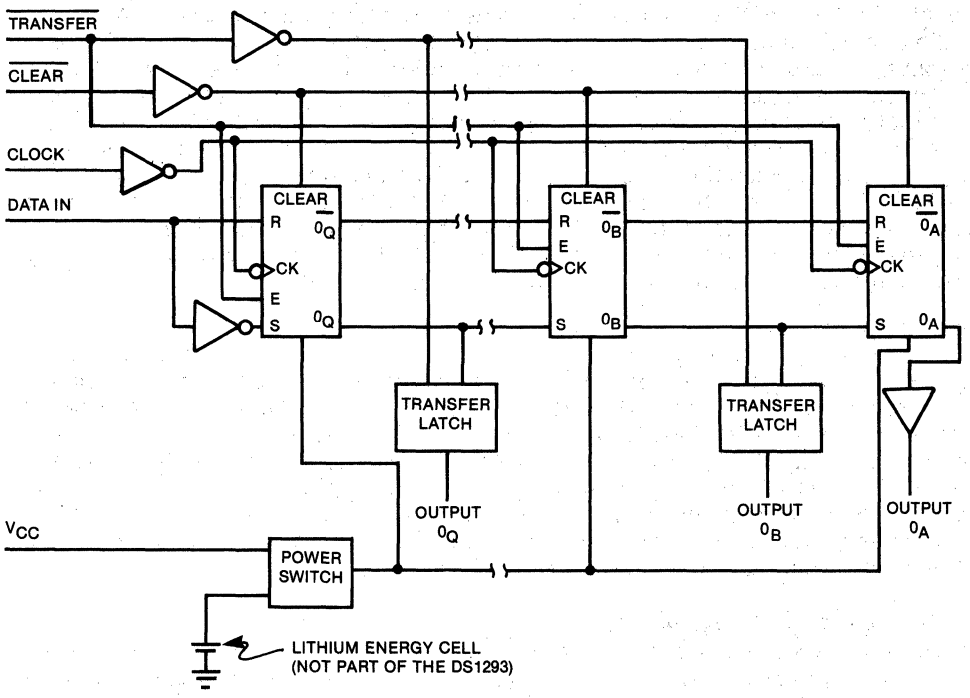
DATA RETENTION MODE

The DS1292 Eliminator provides full functional capability when V_{CC} is greater than 4.5 volts and will ignore all inputs when V_{CC} reaches 4.25 volts typical. In this manner, the settings of each register remain intact during power transients. As V_{CC} falls below approximately 3 volts, an internal power switching circuit connects a lithium energy source to the shift register to maintain data. During power up when V_{CC} rises above approximately 3 volts, the power switching circuit connects external V_{CC} to the shift register and disconnects the lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for a time of 10 MS minimum. During power transients the 16 outputs will track the level of V_{CC} if set to Logic 1 and will remain at ground level if set to Logic Zero.

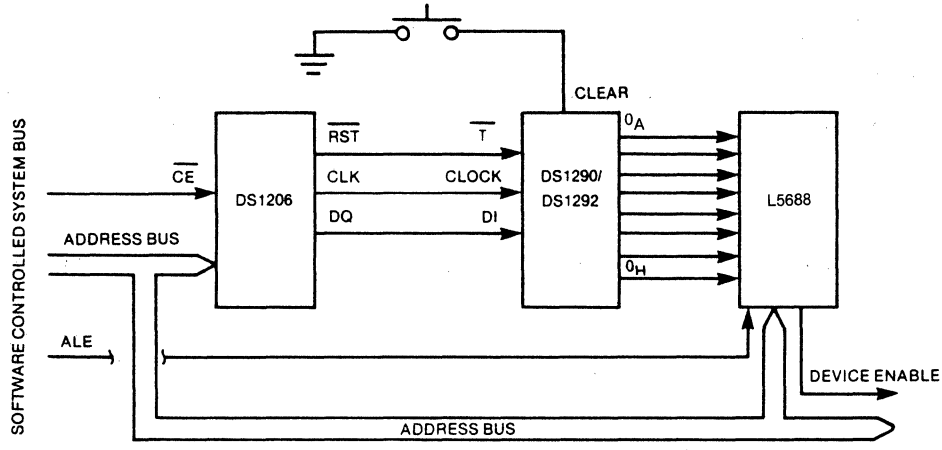
TYPICAL APPLICATION—ELIMINATOR

The DS1292 and DS1206 combine to make a programmable nonvolatile DIP switch which can be transparently set in systems without disturbing other operations. Because the switches are nonvolatile, the switches need only to be set once as they will remain in the programmed state indefinitely. The block diagram of Figure 2 shows the Eliminator implemented with the DS1206 Phantom Interface. The DS1206 samples four address lines and the chip enable signal, looking for a special pattern for 24 consecutive cycles (see the Data Sheet for the DS1206). When a proper match is found, the address lines and one data line become control and data signals which are used to program and verify the settings of the DS1292. All of the signaling sent to the DS1206 and subsequently to the DS1292 are generated by software controlled read cycles which have no effect on the rest of system operation. The clear signal can be used to restore a system back to an unconfigured state.

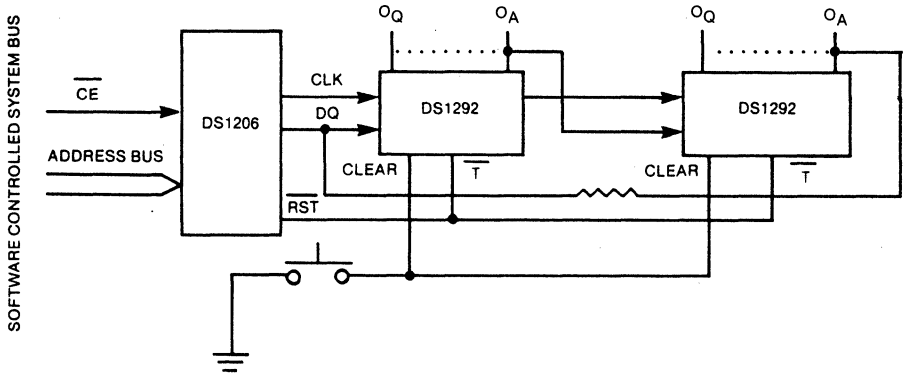
BLOCK DIAGRAM—DS1292/DS1293 Figure 1



PHANTOM INTERFACE AND ELIMINATOR TYPICAL APPLICATION Figure 2



MODULAR EXPANSION OF THE ELIMINATOR Figure 3



1

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -3.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0	V_{IL}	−0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		3	5	mA	
Input Leakage	I_{IL}	−1.0		+1.0	uA	4
Output Leakage	I_{LO}	−1.0		+1.0	uA	
Logic 1 Output @2.4 V	I_{OH}	−1.0			mA	2
Logic 0 Output @0.4 V	I_{OL}			4.0	mA	2

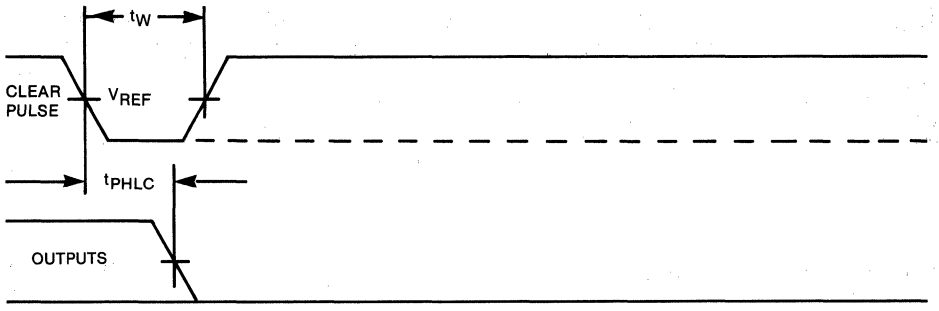
CAPACITANCE ($t_A = 25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

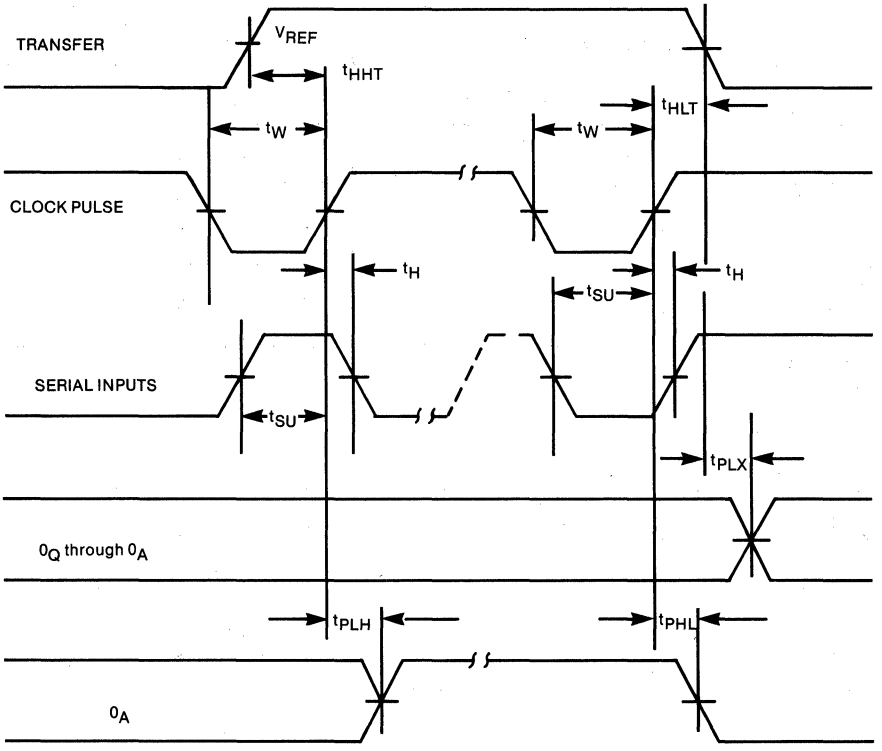
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{CLOCK}			10	MHz	
Width of Clock Pulse	tw_{CLOCK}	50			ns	3
Width of Clear Pulse	tw_{CLEAR}	50			ns	3
Data Set-Up Time	t_{SU}	30			ns	3
Data Hold Time	t_H	10			ns	3
Propagation Delay Time High to Low Level Clear to Output	t_{PHLC}			70	ns	3
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3
Propagation Delay Time High to Low Level Clock to Output	t_{PHL}			50	ns	3
Recovering on Power Up	t_{REC}	10			ms	
Propagation Delay Time High to Low Level Transfer to O Out	t_{PLX}			50	ns	3
Transfer High to Clock Input High	t_{HHT}	50			ns	3
Transfer Low from Clock Input High	t_{HLT}	50			ns	3

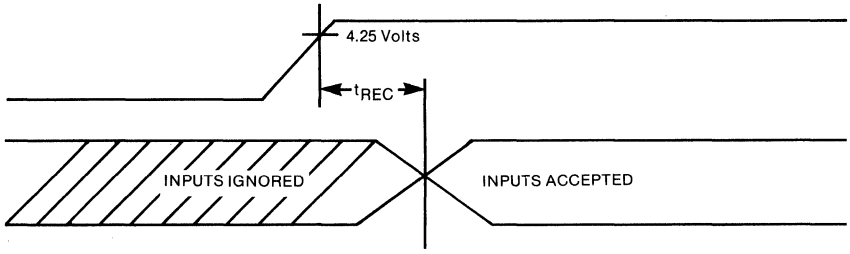
TIMING DIAGRAM—CLEAR CONTROL[3]



TIMING DIGRAM—TRANSFER DATA[3]

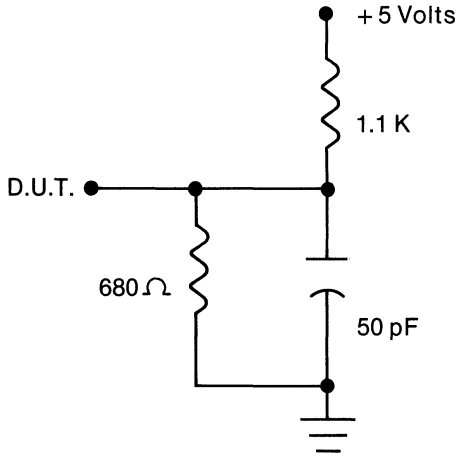


TIMING DIAGRAM—POWER-UP[3]



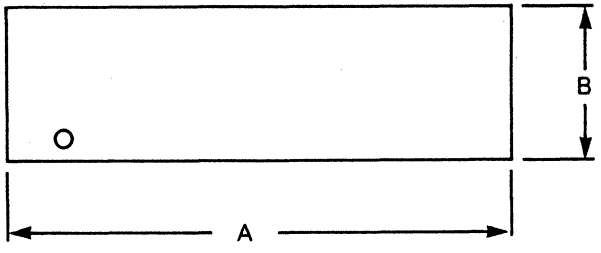
NOTES:
1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 4.
3. $V_{REF} = 1.5$ Volts.
4. Clock and transfer inputs have internal pull-down resistors of 20KΩ typical. Clear has an internal pull-up resistor of 20KΩ typical.

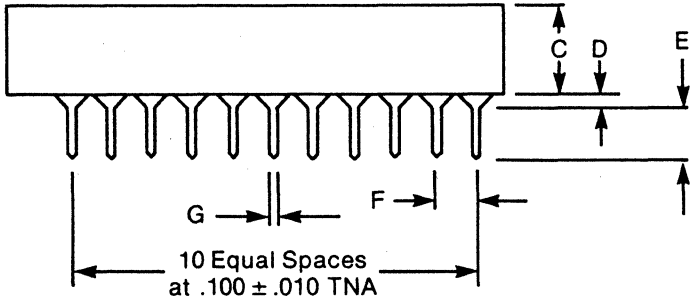
OUTPUT LOAD Figure 4

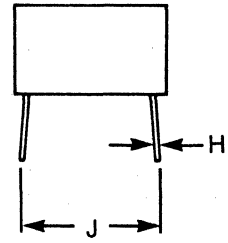


Nonvolatile Eliminator
DS1292

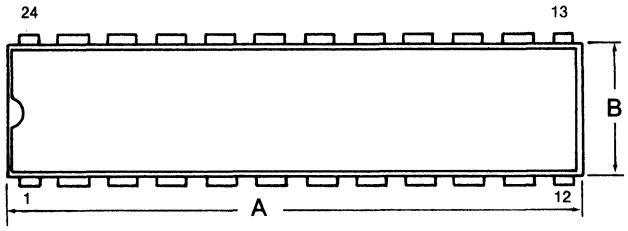
DIM.	INCHES	
	MIN.	MAX.
A	1.236	1.330
B	.370	.390
C	.230	.265
D	.020	.040
E	.115	.135
F	.090	.110
G	.015	.021
H	.008	.012
J	.320	.370



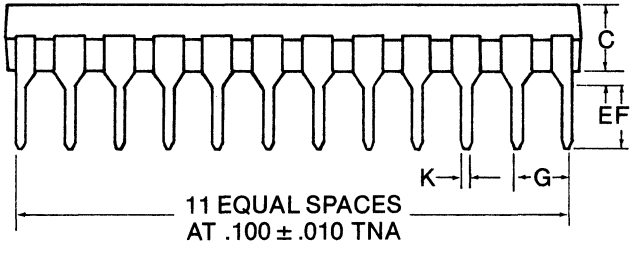


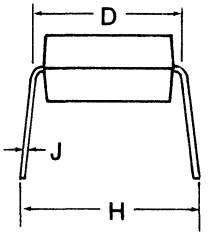


Volatile Eliminator
DS1293
24-Pin DIP (.300")



DIM.	INCHES	
	MIN.	MAX.
A	1.150	1.260
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021





1

SipStik™ Prefabs

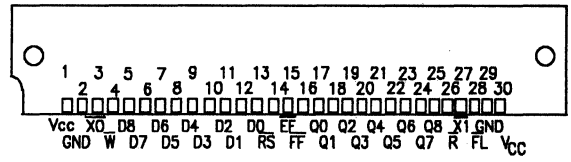
Dallas Semiconductor
FIFO SipStik™

PRELIMINARY
DS2212

FEATURES

- First-In, First-Out memory based architecture
- Flexible 16384 x 9 organization
- Employs Popular JEDEC Standard 30 Position SIMM Connection scheme
- Low Power CMOS Technology
- Self contained logic provides composite full flag and empty flag
- Asynchronous and simultaneous read/ write
- Available in 65 ns, 80 ns and 120 ns access times
- Allows further depth expansion with additional units

PIN CONNECTIONS



PIN NAMES

$\overline{W}$	- Write
$\overline{R}$	- Read
$\overline{RS}$	- Reset
$\overline{FL}$	- First Load
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO}$	- Expansion Out
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground

DESCRIPTION

The DS2212 depth expanded FIFO SipStik provides a high density, high performance rate buffer for asynchronous data exchange applications. Composite full and empty flags prevent data overflow and underflow. The DS2212 contains 4 depth expanded DS2012 4K x 9 FIFO circuits to provide a total of 16K x 9 of First-In, First-Out memory. Expansion-Out, Expansion-In, and first load signals are also provided for further depth expansion.

OPERATION

The DS2212 FIFO SipStik employs a memory-based architecture wherein a byte written into the module is stored at a specific location where it remains until over-written. This architecture is acheived by using four depth expanded DS2012 4K x 9 FIFO intergrated circuits. The memory based architecture allows connection of the read/write, data in, and data out lines of the DS2012 FIFOs in parallel (Figure 1). Please review the DS2012 data sheet for all A.C. timing and characteristics.

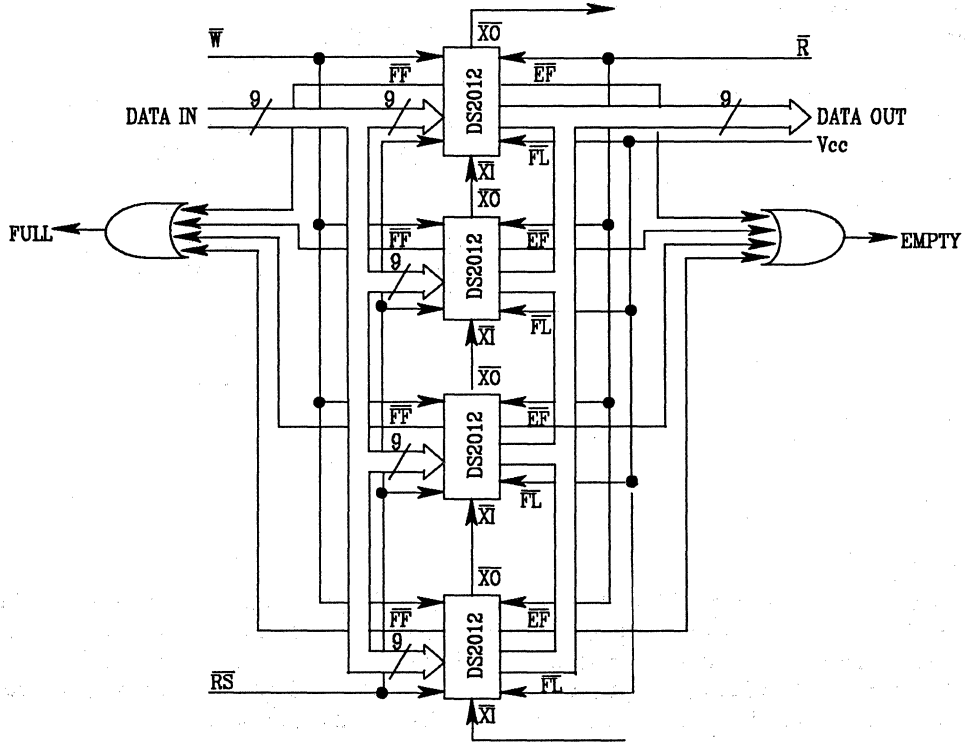
DEPTH EXPANSION

Further depth expansion capability is provided by the DS2212 using the Expansion-Out $\overline{XO}$, Expansion-In $\overline{XI}$, and the First Load FL signals. If two or more SipStiks are required for further depth expansion, the XO pin of each SipStik must be tied to the $\overline{XI}$ pin of the next SipStik. The First Load $\overline{FL}$ pin of only one SipStik in the array should be tied to ground. All other $\overline{FL}$ pins on other SipStiks should be tied to VCC. If only one SipStik is required, the $\overline{XI}$ and $\overline{XO}$ pins should be tied together, and the $\overline{FL}$ pin should be grounded.

EMPTY AND FULL FLAGS

Composite empty flag $\overline{FL}$ and full flag $\overline{FF}$ signals are provided to prevent illogical operations. These status flags are composite in that they are comprised by ORing the $\overline{EF}$ and $\overline{FF}$ of each DS2012 4K x 9 FIFO on the SipStik.* This feature prevents reading of un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). If two or more DS2212 FIFO SipStiks are required for further depth expansion, the $\overline{EF}$ and $\overline{FF}$ outputs from the SipStiks must be ORed by the user for proper operation. Note: $\overline{EF}$ and $\overline{FF}$ output signals will be pushed out by 10 nsec maximum due to propogation delay through the composite OR gates.

Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin relative to Ground	- 0.5V to + 7.0V
Operating Temperature	- 0°C to 70°C
Storage Temperature	- -55°C to +125°C
Output Current per Pin	- 20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Ground	GND		0		V	
Logic "1" Voltage All inputs	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic "0" Voltage	V_{IH}	-0.3		+0.8	V	1,2

D.C. ELECTRICAL CHARACTERISTICS (0° C to 70°C) (V_{CC}=5.0 volts +/-10%)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current (Any input)	I_{IL}	-4	4	uA	3
Output Leakage Current	I_{OL}	-40	40	uA	4
Output Logic"1" Voltage I_{OUT}=-1mA	V_{OH}	2.4		V	1
Output Logic "0"Voltage I_{OUT} +4 mA	V_{OL}		0.4	V	1
Average V_{CC} Power Supply Current	I_{CC1}		150	mA	5
Average Standby Current (R=W=RST=FL/RT=V_{IH})	I_{CC2}		50	mA	5
Power Down Current (All Inputs = V_{CC} -0.2V)	I_{CC3}		10	mA	5

CAPACITANCE

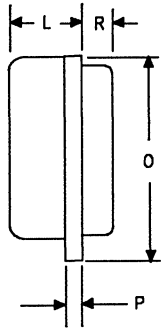
(t_A=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I	30	pF	
Capacitance on Output Pins	C_O	50	pF	6

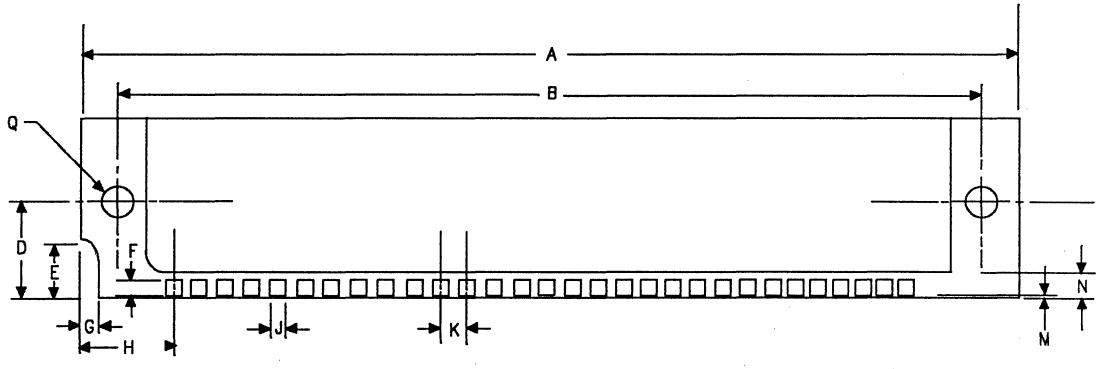
NOTES

1. All voltages are referenced to ground.
2. -1.5 volt undershoots are allowed for 10ns once per cycle.
3. Measured with $0.4 < V_{IN} < V_{CC}$.
4. $R > V_{IH}$, $0.4 > V_{OUT} < V_{CC}$.
5. I_{CC} measurements are made with outputs open.
6. With output buffer deselected.

DS2212
FIFO SipStik



DIM.	INCHES
A	3.500
B	3.234
C	0.133
D	0.400
E	0.250
F	0.070 Min.
G	0.080
H	0.300
J	0.070
K	0.100
L	0.180 Max.
M	0.010 Max.
N	0.100 Min.
O	0.855 Max.
P	0.050 +0.005 -0.004
Q	0.125 Dia. thru



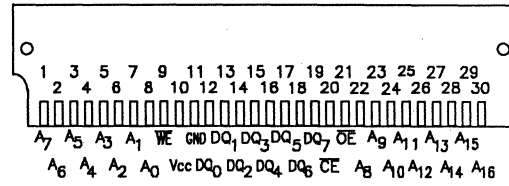
Dallas Semiconductor
SRAM SIPSTIK™

PRELIMINARY
DS2217

FEATURES

- Data retention in the absence of V_{cc}
- Directly replaces volatile SRAM
- Employs popular JEDEC standard 30 position SIMM connection scheme
- Nonvolatile circuitry transparent and independent from host system
- No additional components
- 10 year data retention
- Organized as 128K bytes
- Available in 120ns, 150ns, and 200ns Read Access Time
- Full +/- 10% operating range
- Read cycle time equals write cycle time
- Unlimited write cycles
- Automatic write protection circuitry safeguards against data loss
- Wide operating temperature range of 0°C to 70°C

PIN CONNECTIONS



PIN NAMES

V_{cc}	- +5 volt supply
GND	- Ground
A_0-A_{16}	- Address Inputs
$\overline{DQ_0}$-$\overline{DQ_7}$	- Data Input/Output
$\overline{CE}$	- Chip Enable
$\overline{OE}$	- Output Enable
$\overline{WE}$	- Write Enable

DESCRIPTION

The DS2217 is a self-contained 1,048,576 bit nonvolatile static RAM organized as 131,072 words by 8 bits. The nonvolatile memory contains all necessary control circuitry and energy sources to maintain data integrity in the absence of power for more than 10 years. The DS2217 conforms to the popular 30 position SIMM pinout requiring no additional circuitry.

OPERATION

The DS2217 SRAM SipStik is used like any standard static RAM. All the nonvolatile circuitry resides transparently to the user. Decoding from upper order address lines is also integrated into the nonvolatile controller and is transparent to SRAM operation. Connection to the DS2217 is made by using an industry standard, 30-position SIMM socket (AMP part number 643930-1). These SIMM sockets are also available in double row and low profile angled variations.

READ MODE

The DS2217 is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (chip enable) is active (low). The unique address specified by the 17 address inputs (A_0-A_{16}) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ (chip enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS2217 is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can occur only when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write protected.

DATA RETENTION MODE

The nonvolatile SipStik provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS2217 constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS2217 checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the DS2217 the battery is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The SRAM SipStik provides battery redundancy. The DS2217 provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 85°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3		+0.8	V

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{CC}=5V\pm10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	−60		+60	*u*A
I/O Leakage Current	I_{LO}	−10		+10	*u*A
Output Current @2.4V	I_{OH}	−1.0	−2.0		mA
Output Current @0.4V	I_{OL}	2.0	3.0		mA
Standby Current $\overline{CE}=2.2V$	I_{CC}		15	25	mA
Operating Current	I_{CC}		50	100	mA

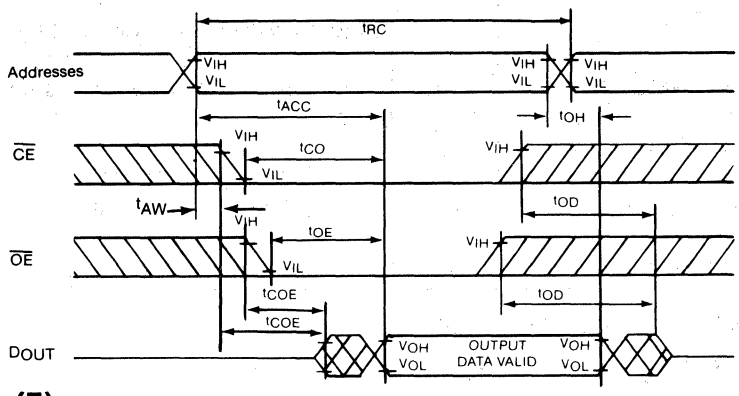
CAPACITANCE ($t_A=25°C$)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	50	pF	
Output Capacitance	C_{OUT}	50	pF	

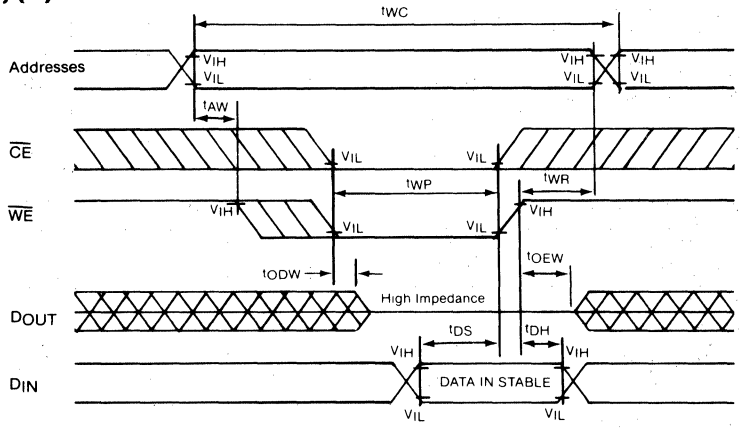
A.C. ELECTRICAL CHARACTERISTICS (0 °C to +70 °C, V_{CC} = 5.0V ± 10%)

		DS2217-120		DS2217-150		DS2217-200			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60		70		100	ns	
$\overline{OE}$ to Output Valid	t_{CO}		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		10		10		ns	
Output High Z from Deselection	t_{OD}		40		70		100	ns	
Output Hold From Address Change	t_{OH}	10		10		10		ns	
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		170		ns	3
Address Set Up Time	t_{AW}	0		0		0		ns	
Write Recovery Time	t_{WR}	0	10		10			ns	
Output High Z From $\overline{WE}$	t_{ODW}		40		70		80	ns	
Output Active From $\overline{WE}$	t_{OEW}	5		10		10		ns	8
Data Set Up Time	t_{DS}	50		60		80		ns	4
Data Hold Time	t_{DH}	0		0		0		ns	4,5

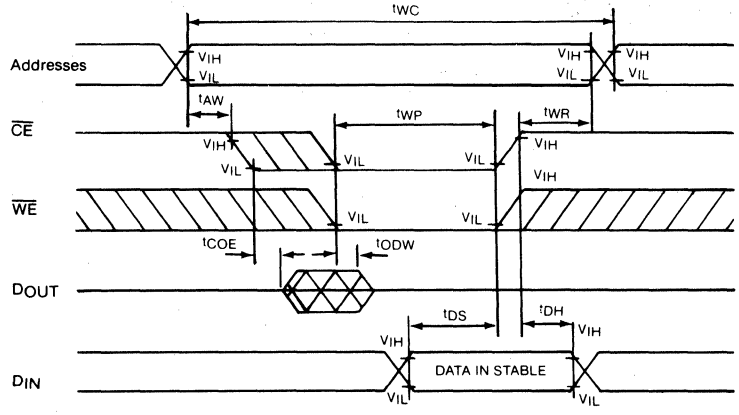
READ CYCLE (1)



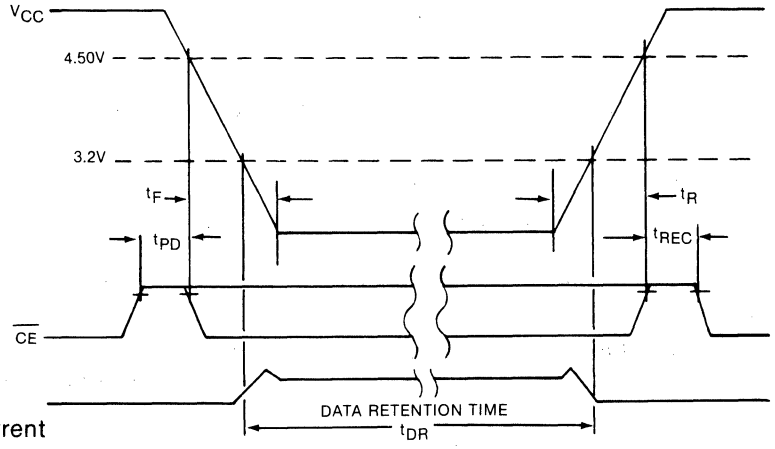
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



Leakage Current
I_L supplied from
lithium cell

POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$ at V_{IH} before Power Down	0		μs	
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	100		μs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		μs	
t_{REC}	$\overline{CE}$ at V_{IH} after Power Up	2	125	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If the $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS2217 is marketed with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

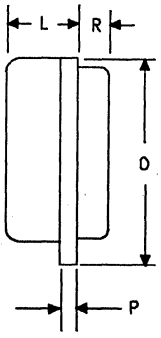
D.C. TEST CONDITIONS

Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

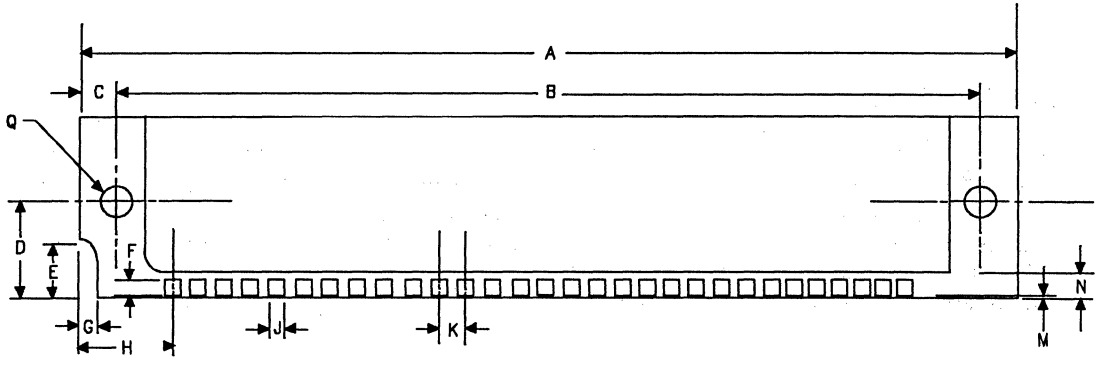
A.C. TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0 V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS2217 SRAM SipStik



DIM.	INCHES
A	3.500
B	3.234
C	0.133
D	0.400
E	0.250
F	0.070 Min.
G	0.080
H	0.300
J	0.070
K	0.100
L	0.180 Max.
M	0.010 Max.
N	0.100 Min.
O	0.855 Max.
P	0.050 +0.005 -0.004
Q	0.125 Dia. thru
R	0.120 Max.



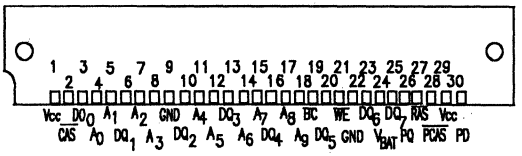
Dallas Semiconductor
DRAM SIPSTIK™

PRODUCT PREVIEW
DS2219

FEATURES

- Maintains data in the absence of system power
- Compatible with existing DRAM SIMM applications
- Normal operating mode completely unaffected
- Nonvolatile circuitry transparent and independent from host system
- No additional components required
- Conforms to popular JEDEC standard 30-position SIMM DRAM module
- Accomodates any 6 volt to 10 volt primary energy cell or rechargable energy source
- Memory array available as 1024K bytes with parity bit
- $\overline{RAS}$ access time of 120ns, or 150ns
- Power fail detection at 10% supply

PIN CONNECTIONS



PIN NAMES

V_{cc}	- +5 volt supply
GND	- Ground
A_0-A_9	- Address Inputs
$\overline{WE}$	- Write Enable
$\overline{RAS}$	- Row Address Strobe
$\overline{CAS}$	- Column Address Strobe
DQ_0-DQ_7	- Data Inputs/Outputs
V_{BAT}	- External Battery Voltage Input
PQ	- Parity Data Output
$\overline{PCAS}$	- Parity Column Address Strobe
PD	-Parity Data Input
$\overline{BC}$	-Battery Condition

DESCRIPTION

The DS2219 nonvolatile DRAM SIMM modules provide all necessary timing, refresh generation, and power down/power up sequencing necessary to maintain data integrity during system power failure. A primary or a rechargable energy source can be used to support data retention. Available in 1,048,576 bytes, the memory module conforms to the standard 30-position SIMM pin configuration. The self contained memory maintenance circuitry resides transparently to host system eliminating the need for any additional components. Normal 5 volt operation is completely unaffected as nonvolatile circuitry is transparent to DRAM.

OPERATION - NORMAL POWER CONDITIONS

Under normal 5 volt operating conditions, the DS2219 Nonvolatile DRAM SipStik behaves exactly like a standard 1024K x 9 DRAM SIMM such as the Hitachi HB56A19B. The $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ inputs to the SipStik are directed through the DS1237 Nonvolatile DRAM Controller IC directly to the individual DRAM circuits. The DS2219 will operate in this mode until the 5 volt supply at V_{CC} decays to 4.5 volts during loss of power. For detailed information on access timing, A.C. characteristics, and operating conditions for the Power Normal mode, please review the Hitachi HB56A19B DRAM Module data sheet.

OPERATION - POWER LOSS AND DATA RETENTION

When the 5 volt V_{CC} power begins to drop the DS1237 senses this change using a precision band gap comparator and isolates all control inputs to the SipStik as V_{CC} falls below 4.5 volts. Power to the individual DRAM circuits is switched from the main 5 volt supply to a backup supply connected at position 24 of the SipStik. This backup supply is typically a chargeable capacitor or battery; however, any supply between 6 volts and 10 volts is suitable. Connection pins are provided for the backup supply at other locations on the SipStik p.c.b. if location 24 is not convenient. All refreshing is accomplished internally within the SipStik and is supported continuously until V_{CC} returns to normal levels and the system signals the SipStik that it is ready to assume refresh duties.

OPERATION - RETURN TO NORMAL POWER CONDITIONS

When the System 5 volt supply returns and exceeds 4.5 volts, the system supply is reconnected to the DRAM circuits and the backup supply is internally disconnected. At this time, a continuous $\overline{CAS}$ before $\overline{RAS}$ refresh is also generated internally at a cycle time of 350 ns maximum. Refreshing continues without interruption until the system signals the SipStik that it is ready to assume refresh responsibility for the DRAMs. Refresh duties are shifted from the SipStik to the system when a software controlled switch is set by sending a specific pattern on address lines A5, A6, and A7 for 24 consecutive cycles. The address pattern which sets the software switch is shown in Figure 1. This address pattern is clocked into the DS1237 resident on the SipStik on the falling edge of $\overline{CAS}$ provided that set up and hold times are met. When the 24th cycle is correctly entered, the system will have full access to RAM and must handle refresh requirements. RAM read and write cycles can then resume without restriction.

CONSERVATON OF BACKUP SUPPLY

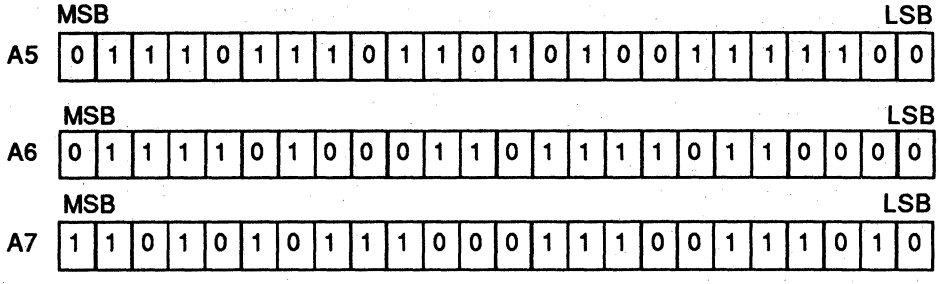
Another software controlled switch allows conservation of the backup supply when data retention is not required. The switch is controlled by the same method described for refresh except that the bit pattern is different. The bit patterns shown in Figure 2 turn on or off this switch which disconnects or connects the backup supply.

BACKUP CONDITION

The DS2219 also contains two features which provide information about the condition of the backup supply. The $\overline{BC}$ Battery Condition pin at location 19 of the SipStik provides the output for the backup supply information. If this feature is to be used, please review the "Backup Condition" section of the DS1237 Nonvolatile SRAM Controller data sheet.

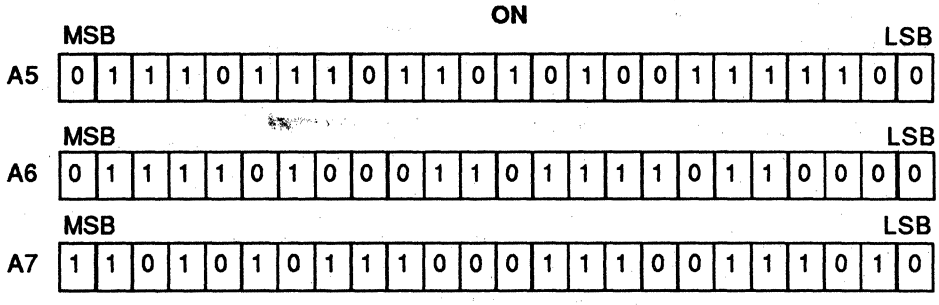
SOFTWARE SWITCH FOR PROCESSOR CONTROL POWER UP

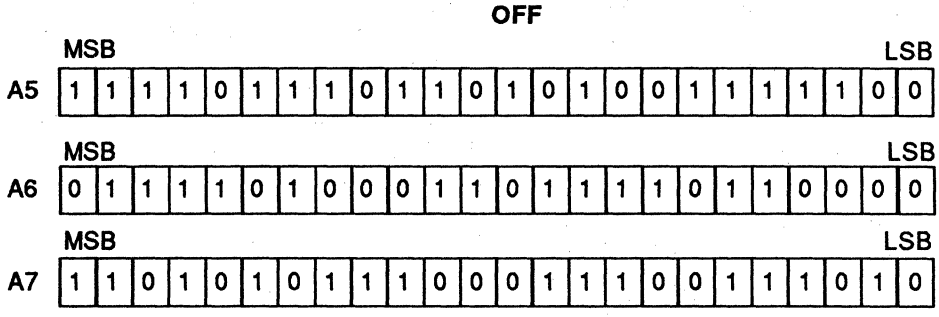
Figure 1



SOFTWARE CONTROLLED SWITCH FOR CONSERVATION OF BACKUP SUPPLY

Figure2





ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON ANY PIN EXCEPT BATTERY INPUTS
RELATIVE TO GROUND -0.3 TO +7V
VOLTAGE ON THE BATTERY INPUT PINS
RELATIVE TO GROUND -0.3V TO +12V
OPERATING TEMPERATURE 0°C TO +70°C
STORAGE TEMPERATURE 55°C TO +125°C

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	VOLTS	1
Voltage Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	VOLTS	1
Voltage Input Logic 0	V_{IL}	-0.3		+0.8	VOLTS	1
Backup Supply	BK_{UP}	6.0	8.0	10.0	VOLTS	2.3

DS ELECTRICAL CHARACTERISTICS (0°C to70°C. V_{CC}=4.5 to 5.5 V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply Current	I_{CC}			15	mA	4
Power Fail Detect	V_{TP}	4.25	4.37	4.5	V	6
Input Leakage	I_{IL}	-1.0		1.0	uA	4

(0°C TO 70°C, V_{CC} <V_{TP})

Data Retention Current	I_{DR}		7	15	mA	5

12

CAPACITANCE

(t_A =25°)

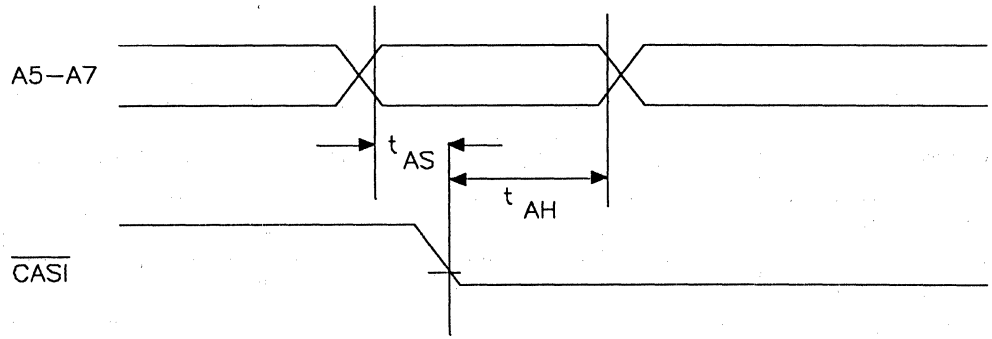
PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input capacitance	C_{IN}		5	7	pF	4

A.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=4.5 to 5.5V)

Address Setup Time	t_{AS}	0			ns	
Address Hold Time	t_{AH}	20			ns	

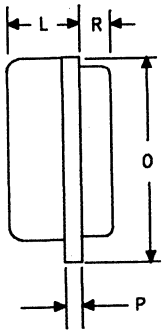
SOFTWARE SEQUENCE ENTRY



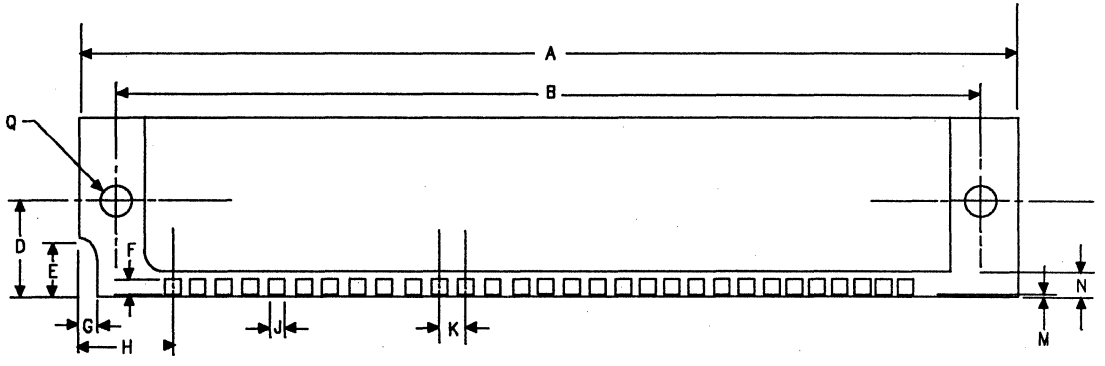
NOTES

1. All voltages are referenced to ground.
2. The $\overline{BC}$ pin will be driven active whenever V_{CC} is within nominal limits and the backup supply is below V_{CC}.
3. Backup input voltage is internally regulated within the DS2219 such that V_{CC} to the DRAMs is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
4. Additive to specification limit for the Hitachi HB56A19B Series DRAM SIMM.
5. This is the average current from the backup supply to maintain memory for the SipStik.
6. V_{TP} is the trip point where the internal switching circuits disconnects V_{CC} and connects the internally regulated backup supply to the DRAMs.Rapid refresh is also initiated at this time.

DS2219 DRAM SipStik



DIM.	INCHES
A	3,500
B	3,234
C	0,133
D	0,400
E	0.250
F	0.070 Min.
G	0.080
H	0.300
J	0.070
K	0.100
L	0.180 Max.
M	0.010 Max.
N	0.100 Min.
O	0.855 Max.
P	0.050 $^{+0.005}_{-0.004}$
Q	0.125 Dia. thru
R	0.120 Max.



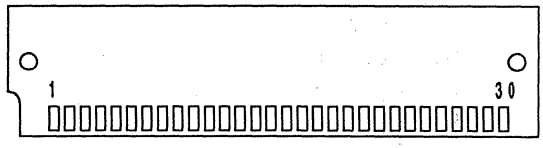
Dallas Semiconductor
SOFT MODEM
SIPSTIK™

PRODUCT PREVIEW
DS2245
DS2245MNP

FEATURES

- Reprogrammable modem subsystem:
  - DS2245-12 is 1200 bps version
  - DS2245-24 is 2400 bps version
- Bell 212A/103 and CCITT V.22bis/22/21compatible
- Parallel interface connects to PC/XT/AT bus
- Companion device to DS2249 DAA SIPSTIK
- Implements standard AT command set
- "Softness" allows program upgrades without replacing expensive EPROMs
- DS2245MNP offers MNP error correction
- Nonvolatile parameter storage
- DTMF generation and detection
- Employs popular JEDEC standard 30-pin SIMM connection scheme
- Single +5 volt supply operation

PIN CONNECTIONS (tentative)



PIN#	SIGNAL	PIN#	SIGNAL
1	AIN	13-20	D0-D7
2	AOUT	21	A0
3	NC	22	A1
4	NC	23	A2
5	AUDIO	24	CS
6	OH	25	INT
7	RI	26	MR
8	VCC	27	NC
9	NC	28	NC
10	GND	29	NC
11	WR	30	NC
12	RD		

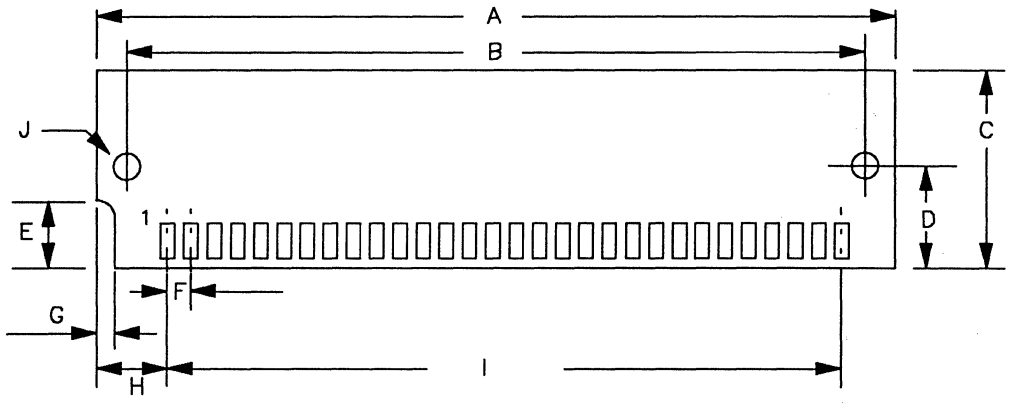
DESCRIPTION

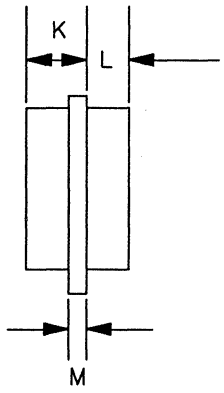
The DS2245 is a microcommunication subsystem that when used with the DS2249 DAA forms a complete 2400/1200/300 bps modem that can be directly connected to the public switched telephone network. Included in the DS2245 are all the modulation/demodulation and filtering circuitry necessary for compatibility with Bell 212A/103 and CCITT V.22/21 type modems. Embedded software responds to the industry standard AT command set for modem control. The parallel interface can connect directly to a PC/XT/AT bus or to any other general-purpose bus architecture.

Special features of this modem include: nonvolatile parameter storage, DTMF tone monitoring, MNP class 4 error correction (DS2245MNP) and a "soft" reload function that permits the user to install program updates without resorting to the replacement of expensive EPROM devices.

Applications include laptop computers, vending machines, pay telephones or any other system requiring communication over the public telephone network.

DS2245
DS2245MNP
SOFT MODEM SIPSTIK





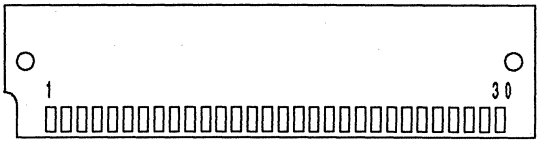
DIM	INCHES
A	3.500
B	3.234
C	0.850
D	0.400
E	0.250
F	0.100
G	0.080
H	0.300
I	2.900
J	0.125 DIA
K	0.250
L	0.125
M	0.062

Dallas Semiconductor
Data Access Arrangement (DAA) SipStik™

PRODUCT PREVIEW
DS2249

FEATURES
- Interfaces voice/data to the public switched telephone network
- FCC Part 68 registered
  - 1500 VDC isolation
  - 800 Volt surge protection
- Companion device to DS2245 SOFT MODEM SIPSTIK
- Employs popular JEDEC standard 30-pin SIMM connection scheme
- Single +5 volts supply operation
- Ring detection
- 2- to 4-wire connector
- Audio monitor output

PIN CONNECTIONS



PIN NAMES

1	- $\overline{OH}$
2	- AUDIO
3	- TXA
4	- RXA
5-9	- N/C
10	- Vcc
11	- GND
12	- $\overline{RI}$
13-26	- N/C
27	- RINGO
28	- TIPO
29	- RING
30	- TIP

DESCRIPTION
The DS2249 is a Data Access Arrangement (DAA) that is designed to connect directly (through an appropriate mechanical connector such as an RJ11 jack) to the public switched telephone network. It is FCC Part 68 Type WP registered to meet hazardous voltage, surge and leakage current requirements.

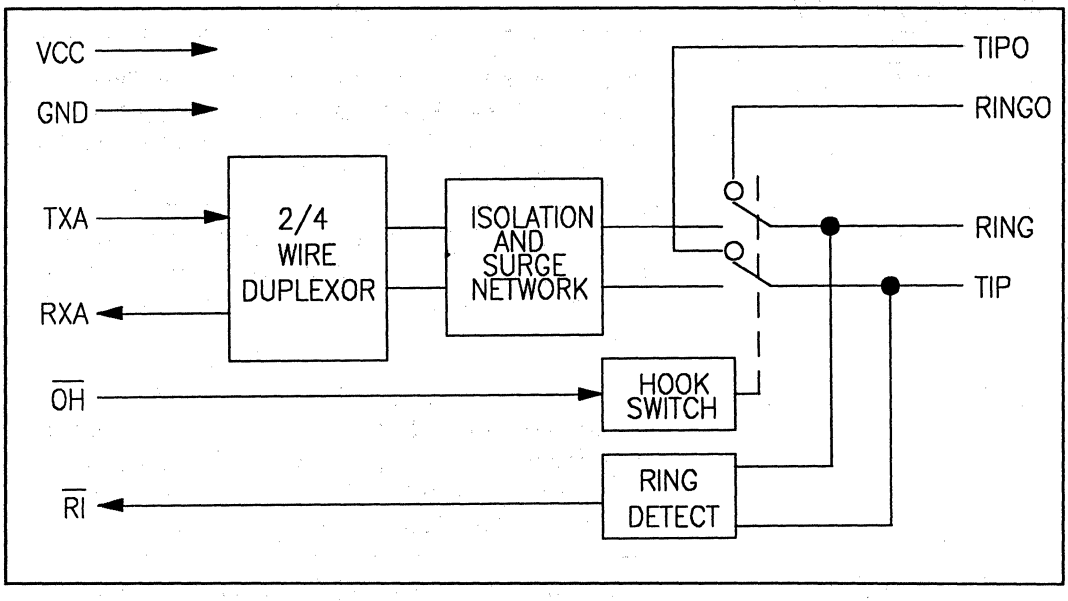
Included in the DS2249 is a ring detect output and a 2- to 4-wire converter for use with modem components such as the DS2245. It operates from a single +5V supply and uses CMOS circuitry for lower power consumption.

Applications include laptop computers, remote data collection, pay phones or any application where data or voice needs to be sent over the telephone network.

PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	$\overline{OH}$	I	Off hook control. A logic low on this pin causes the DAA to go off-hook and sieze the phone line. If this pin is high or left floating, the DAA will be in an on-hook state and be disconnected from the line.
2	AUDIO	O	Audio output. This is a buffered output that can be used for audio monitoring of the call connection. This output can be connected to a speaker amplifier for driving a monitor speaker.
3	TXA	I	Transmit analog data input. The analog output of a modem device would be connected here for transmission to the phone line. This input is buffered from the phone line and does not affect the line matching impedance presented by the DS2249.
4	RXA	O	Receive analog data out. This is the output of the 2/4 wire duplexer which should be connected to the input of the modem device's receive section. The signals at this pin are capacitively coupled to the output of an op-amp.
10	VCC	-	Positive supply. +5 volts.
11	GND	-	Signal ground. 0 volts.
12	$\overline{RI}$	O	Ring detect indicate. This pin indicates the presence of a ring signal on TIP and RING by a logic low state.
5-9 13-26	N/C	-	No connection. Leave these pins open.
27 28	RINGO TIPO	- -	Ring and Tip connections out. When the DS2249 is in an on-hook state, these pins are connected to the TIP and RING telephone line inputs. When the DS2249 is in an off-hook state, these pins are disconnected from any internal circuitry.
29 30	RING TIP	- -	Ring and Tip phone line inputs. Connect these pins to the line through an RJ11 jack.

DS2249 BLOCK DIAGRAM Figure 1



RING DETECTION

Reception of a valid ring signal is indicated by a logic zero at RI. This output is low during the normal 2 second ringing "on" interval and high during the normal 4 second ringing "off" interval. The ring detection circuitry incorporates protection from pulse dialing transients which might otherwise cause false ring indications.

INTERNAL 2- TO 4-WIRE CONVERTER

The 2- to 4-wire converter interfaces separate transmit and receive signal paths to the 2-wire telephone line. A perfect converter would be able to completely remove the transmit signal from the receive signal (at RXA); however due to the wide range of telephone line impedances, only about 10 to 15 dB of *transhybrid loss* can be typically expected. Transhybrid loss is defined as the attenuation between the TXA input to the RXA output specified at a certain frequency. Better transhybrid loss results in better modem performance, primarily when the line is noisy and the receive level is weak (<-35 dBm).

ON/OFF HOOK CONTROL

The telephone line may be seized or taken off-hook by applying a logic zero to the OH pin. Applying a logic one to OH puts the DS2249 in the on-hook state whereby the telephone line is released. The DS2249 does not draw any DC current from the telephone line when in the on-hook state.

Pulse dialing is usually implemented be pulsing the OH input high and low. Typically, a microcontroller would perform this function through the use of a software-controlled port pin.

USE WITH TELEPHONE SETS

A telephone set can be used with the DS2249 by connecting the set's TIP and RING inputs to the

TIPO and RINGO pins. When the DS2249 is in a on-hook state, incoming ring signals will be routed to the telephone set as well as to the DS2249's internal ring detect circuit. Seizure of the line occurs when either the telephone set's receiver is picked up or when the OH pin is taken low. It is recommended that the telephone set only be used (in the off-hook state) while the DS2249 is in the on-hook state.

TELEPHONE LINE CONNECTION INFORMATION

When developing a product that is to be connected to the telephone line, it is necessary to use a circuit described as a Data Access Arrangement (DAA) which is approved by the appropriate governmental agency. In the US, this agency is the Federal Communications Commission (FCC), while in Canada it is the Department of Communications (DOC). These agencies test and approve the product to ensure that it meets their specifications thereby protecting the telephone system from damage and protecting the user from high voltage transients (such as lightning strikes) which may come down the telephone line.

The DS2249 has been designed to meet all requirements for hazardous voltage, surge protection and leakage current, and has been granted a user transferrable Part 68 Type WP Registration under Part 68 of the FCC Rules and regulations. As such, a system developed with the DS2249 as the DAA will be automatically approved for Part 68 Type WP high voltage protection requirements and no further registration is required.

If the system developed transmits data, or DTMF tones on the telephone line, the user must certify that the circuitry which drives the DS2249 meets basic FCC requirements for maximum transmission levels, out of band energy and billing delay. Full details may be obtained from the FCC under Part 68 of the FCC Rules and Regulations, or in Title 47 of the Code of Federal Regulations.

OUTPUT LEVEL REQUIREMENTS OF PART 68

For the normal "permissive" telephone line, equipment which transmits data must not exceed a level of -9 dBm. If the system is capable of DTMF dialing, the maximum DTMF transmission level must be less than 0 dBm averaged over a 3 second interval.

For modem applications, the out of band energy limit is normally ensured by the transmit filter in the modem circuitry. Data equipment must not transmit "out of band" energy on the telephone line which exceeds the limits shown in Table 2.

BILLING DELAY

A minimum delay of 2 seconds is required between the time the DS2249 is taken "off hook" and any data is transmitted. This delay is required to provide time for the Telephone Company's Central Office switching equipment to complete billing information for the call prior to transmission of data.

FCC APPROVAL

The user of the DS2249 in a modem application must certify to the FCC that the final system meets the requirements of Part 68 which include the criteria above as well as the high voltage protection that is provided by the DAA. This is generally accomplished through an independent testing lab which will test the system and submit the proper paperwork to the FCC for approval.

OUT OF BAND ENERGY Table 2

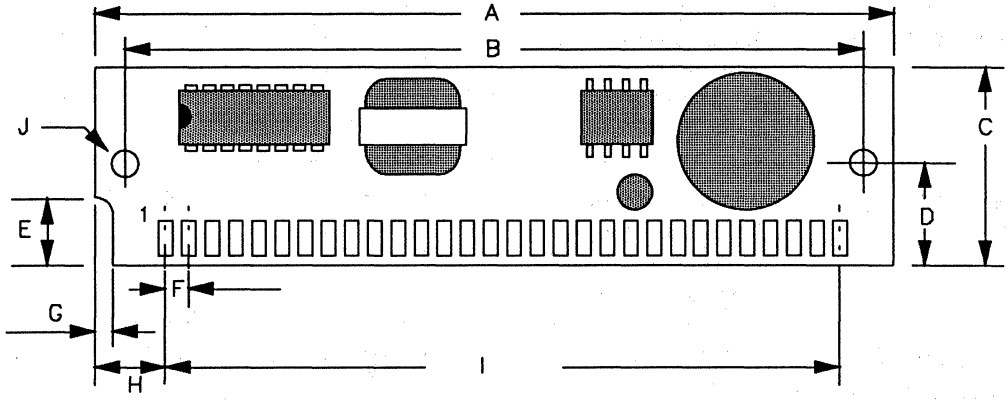
FREQUENCY RANGE	MAXIMUM POWER
200Hz to 3990Hz	- 9 dBm
3990Hz to 4005Hz	-27 dBm
4005Hz to 16kHz	-16 dBm
6kHz to 94kHz	-47 dBm
6kHz to 270kHz	-46 dBm
270kHz to 6MHz	-60 dBm

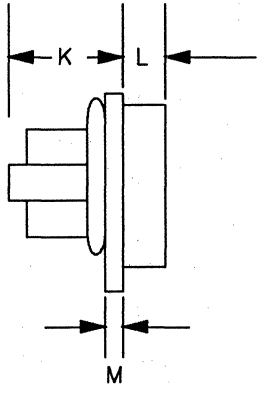
ELECTRICAL SPECIFICATIONS

V_{CC} = +5V +/- 10%, T_A = 0 to 70°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Off-hook (OH = 0)			35	mA
Transmit Gain	Gain between transmit input and telephone line at 1800 Hz with 600 ohm termination	-0.5	0	+0.5	dB
Receive Gain	Gain between telephone line and receive output at 1800 Hz with 600 ohm termination	-0.5	0	+0.5	dB
Telephone Line Input Impedance	at 1800 Hz	540	600	660	Ohms
Transhybrid Loss	Attenuation between the transmitter input and receiver output at 1 kHz with 600 ohm termination	10	18		dB
Attenuation	Receive and Transmit attenuation at 300 Hz with 600 ohm termination	0.8	1.0	3	dB
Transmit Input Impedance	at 1800 Hz	21	20	22	Kohms
Receive Output Impedance	at 1800 Hz (RXA, Audio)		50		Ohms
Ring Detect Sensitivity	Min. AC voltage between Tip & Ring.Type B ringer(on hook)	38			Vrms
Loop Current Switch Control Voltage	ON: (off hook) OFF: (on hook)	3.0	2.0 0.8	 0.5	Volts Volts
Loop Current Switch Control Current			1.0	2.0	mA

DS2249
DAA SipStik





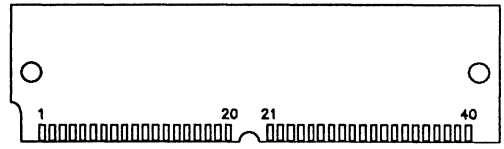
DIM	INCHES
A	3.500
B	3.234
C	0.840
D	0.400
E	0.250
F	0.100
G	0.080
H	0.300
I	2.900
J	0.125 DIA
K	0.450
L	0.125
M	0.062

Dallas Semiconductor
Micro SipStik™
Time Micro SipStik™

PRELIMINARY
DS2250
DS2250T

FEATURES:
- Nonvolatile SRAM for program and/or data
- Capable of modifying its own program and/or data memory
- Program downloading via an on-chip full duplex serial port
- Adjustable partition between program and data memory
- Completely crash-proof: program/data RAM and all data registers are maintained in absence of power
- All 32 port pins available for I/O
- Automatic restart on detection of errant software execution
- Orderly shutdown and automatic restart on power up/down
- Program and data memory secure, with a tamper proof on-chip encryptor
- Compatible with industry standard 8051 instruction set
- DS2250T: Permanently powered clock/calendar
- 40-position SIMM connection scheme

PACKAGE OUTLINE



ORDERING INFORMATION

ORDERING INFORMATION

DS2250 XX–XX MICRO SIPSTIK
DS2250T XX–XX TIME MICRO SIPSTIK

Speed Grade

8	8 MHz
12	12 MHz
16	16 MHz

Program/Data RAM

8	8 Kbytes
16	16 Kbytes
32	32 Kbytes
64	64 Kbytes

DESCRIPTION
The DS2250 Microcontroller SipStik stays up-to-date because it was designed for change. Unlike rigid ROM or EPROM based microcontrollers, all of the Microcontroller Sipstik's memory is high performance, read/write, and nonvolatile for more than ten years. The DS2250 is equipped with nonvolatile SRAM which can be dynamically partitioned to fit program and data storage requirements of a particular task. As a result of sophisticated crashproofing circuitry,

processing of a task can resume after a power outage. A built-in encryptor prevents unauthorized access to resident application software. The DS2250T Time Micro SipStik incorporates all of the features of the DS2250 along with the addition of a built-in real-time clock/calender function.

The DS2250 and DS2250T are the functional equivalents of the DS5000 and DS5000T, respectively, with the exception that the both devices are available with addtional memory size variations, including 16K bytes and 64 Kbytes of nonvolatile memory. The pinout and instruction set of both products match the industry standard 8051 microcontroller. The DS2250 and DS2250T each plug into the SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles.

PIN ASSIGNMENTS

The following table summarizes the pin assignments for the DS2250:

1	P1.0	2	V_{CC}
3	P1.1	4	P0.0 (AD0)
5	P1.2	6	P0.1 (AD1)
7	P1.3	8	P0.2 (AD2)
9	P1.4	10	P0.3 (AD3)
11	P1.5	12	P0.4 (AD4)
13	P1.6	14	P0.5 (AD5)
15	P1.7	16	P0.6 (AD6)
17	RST	18	P0.7 (AD7)
19	P3.0 (RXD)	20	EA* (V_{PP})
21	P3.1 (TXD)	22	ALE (PROG*)
23	P3.2 (INT0*)	24	PSEN*
25	P3.3 (INT1*)	26	P2.7 (A15)
27	P3.4 (T0)	28	P2.6 (A14)
29	P3.5 (T1)	30	P2.5 (A13)
31	P3.6 (WR*)	32	P2.4 (A12)
33	P3.7 (RD*)	34	P2.3 (A11)
35	XTAL2	36	P2.2 (A10)
37	XTAL1	38	P2.1 (A9)
39	GND	40	P2.0 (A8)

16K AND 64K VERSION MEMORY ORGANIZATION

The DS2250(T) 16-XX device incorporates a total of 16K bytes of embedded nonvolatile RAM for program/data storage. Similarly, the DS2250(T) 64-XX incorporates a total of 64K bytes for program/data storage. The following is a description of how this memory may be utilized by the designer. This discussion assumes that the reader is familiar with the programming model of the DS5000, which is described in detail in Section 4 of the DS5000 User's Guide.

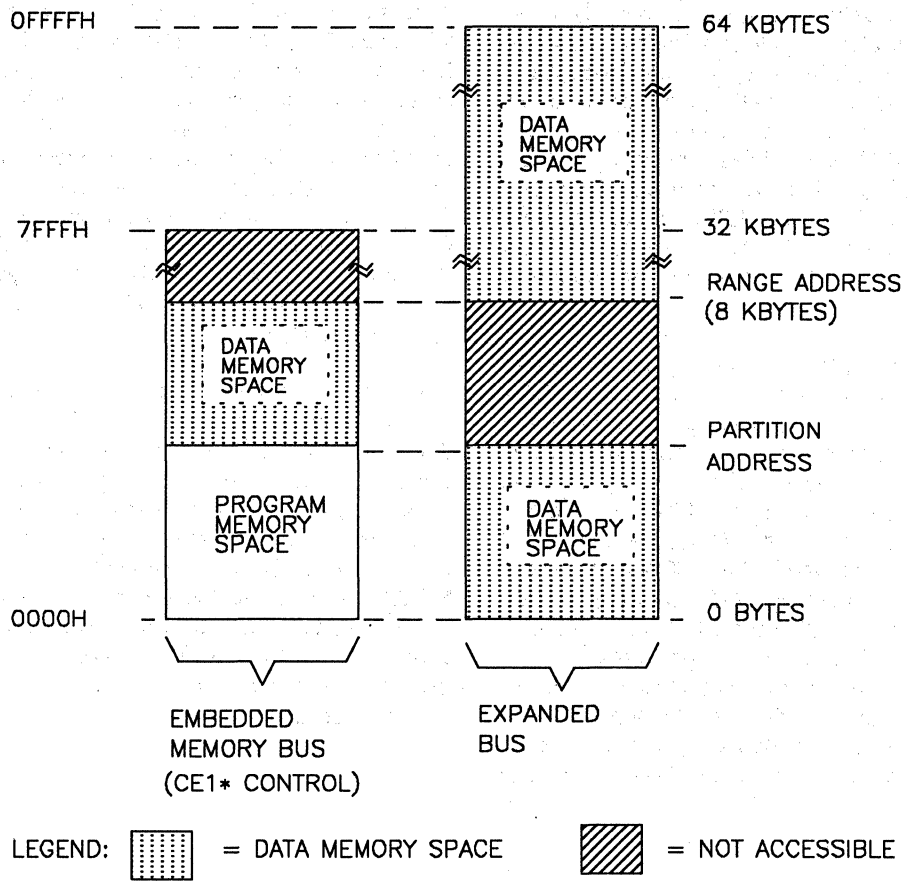
The memory on the DS2250(T) 16-XX and DS2250(T) 64-XX is organized as two separately accessed 8K byte memory devices and two separately accessed 32K byte memory devices, respectively. Each of the devices are

enabled by one of the two separate chip enable signals from the microcontroller die: CE1* and CE2*. These chip enable signals operate under the control of the application software via the ECE2 bit in the MCON Special Function register. For the DS2250(T) 16-XX, a maximum of 8K bytes of Program and/or Data Memory under the control of CE1* is available, with 8K bytes Data Memory under the control of the CE2* map. For the DS2250(T) 64-XX, 32K bytes of Program/ Data memory is under the control of CE1* and 32K bytes of Data Memory is under the control of CE2*.

Figure 1 illustrates the mapping within the embedded RAM which results when the ECE2 bit is cleared to 0. In this case, only the Program/ Data RAM which is under the control of the CE1* signal is accessible and it is mapped in an identical fashion to a 8 or 32K byte version of a DS5000. The Partition Address and the Range Address (as defined in the MCON register) determine the mapping of Program and Data Memory space within the CE1* controlled embedded RAM area. Any program memory access from location 0000H up to (but not including) the Partition Address location will be mapped to the corresponding locations within the embedded Program/Data RAM. Program accesses at or above the Partition and/or Range addresses will be executed via the Expanded Address/Data bus in place of Ports 0 and 2, as long as the Security Lock bit is cleared to 0. If the Security Lock bit is set to a 1, then no external Program Memory accesses are possible. Any data memory access (using a MOVX instruction) from the Partition Address location up to (but not including) the Range address location will be mapped to the corresponding locations within the embedded Program/Data RAM. Any Data Memory access outside of the area between these two addresses will be executed on the Expanded Bus.

Figure 2 illustrates the mapping of Program and Data Memory within the DS2250(T) 16-XX or DS2250(T) 64-XX when the ECE2 bit is set to 1. When ECE2 is set to 1 by the application software, Program Memory accesses to the embedded RAM will still cause only CE1* to be activated. However, any Data Memory access by a MOVX instruction to the embedded RAM will cause CE2* to be activated instead of CE1*. As a result, the memory device under the control of the CE2* signal can only be used for data memory accesses.

16K OR 64K VERSION PROGRAM/DATA MEMORY: ECE2=0 Figure1

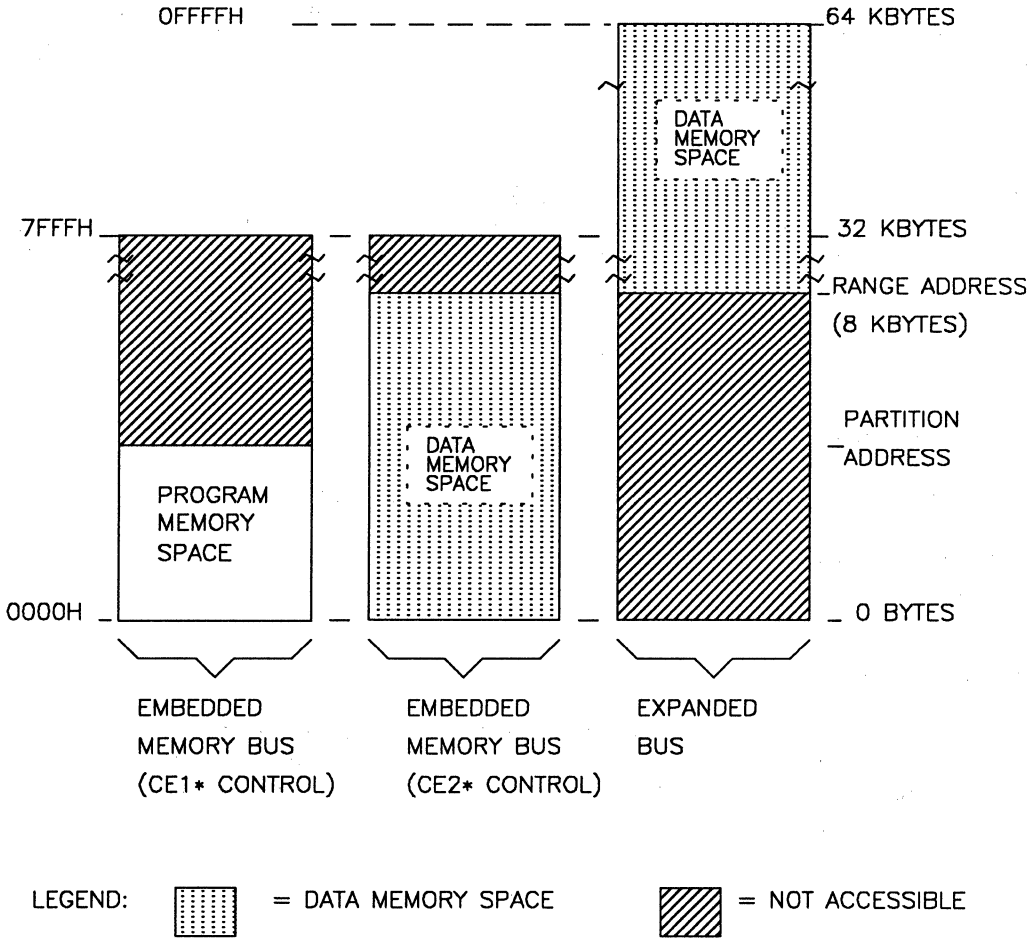


DS2250T CLOCK/CALENDAR

The DS2250T incorporates a permanently powered Embedded Clock/Calendar (ECC) that is identical in function to the DS1215 Timekeeper. The real-time clock is memory-mapped on the internal Embedded RAM address/data bus. As a result, it may be accessed by software as if it were Embedded Data RAM using the "MOVX" set of instructions. Accesses to the ECC take place with no effect on I/O port pins. Detailed operation of the ECC may be found in the DS5000T data sheet.

For the DS2250T 16-XX and DS2250T 64-XX versions, both the ECC and the second memory device are accessed via the CE2* control line from the microcontroller. The CE2* signal is routed

64K PROGRAM/DATA MEMORY: ECE2=0 Figure 2



1

through the ECC so that the CE* signal on the second memory device is conditioned by control logic within the ECC itself. Access to the second memory device by the application software can proceed as normal until communication with the ECC is desired. The application software may then select the ECC by performing the 64-bit pattern recognition CE2* read cycle sequence. Reads and writes can then proceed as described for the DS5000T.

SIPSTIK SOCKET

The DS2250 and DS2250T mate directly with the AMP Micro-Edge™ SIMM connectors, summarized in table 1, which are available either from AMP Inc. or from Dallas Semiconductor. Please refer to the DS9022 data sheet for mechanical specifications on these connectors.

DS2250 COMPATIBLE CONNECTORS Table 1

SOCKET TYPE	PLATING	PART NUMBERS AMP	DALLAS
.050" Centerline Vertical Single Row	Tin	821918-1 or 821918-2	DS9072-40U

SELECTED ELECTRICAL CHARACTERISTICS

The following are selected electrical operating characteristics of the DS2250 and the DS2250T. A partial set of DC and AC operating characteristics which are applicable to the DS2250 and DS2250T are given in the DS5000 and DS5000T data sheets in the Dallas Semiconductor Data Book. A full set of electrical characterics which are applicable to the DS2250 and DS2250T are available in the DS5000 User's Guide.

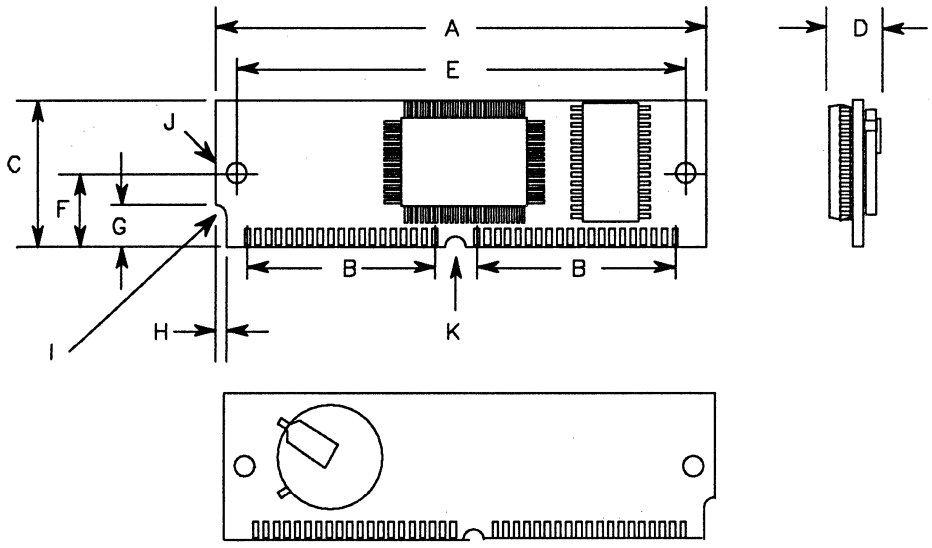
ABSOLUTE MAXIMUM RATINGS *

Voltage on any pin relative to ground	- 0.1 to 7.0V
Operating Temperature	- 0° to +70° C
Storage Temperature	- 0° C to +70° C
Soldering Temperature	- 260° C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is notimplied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

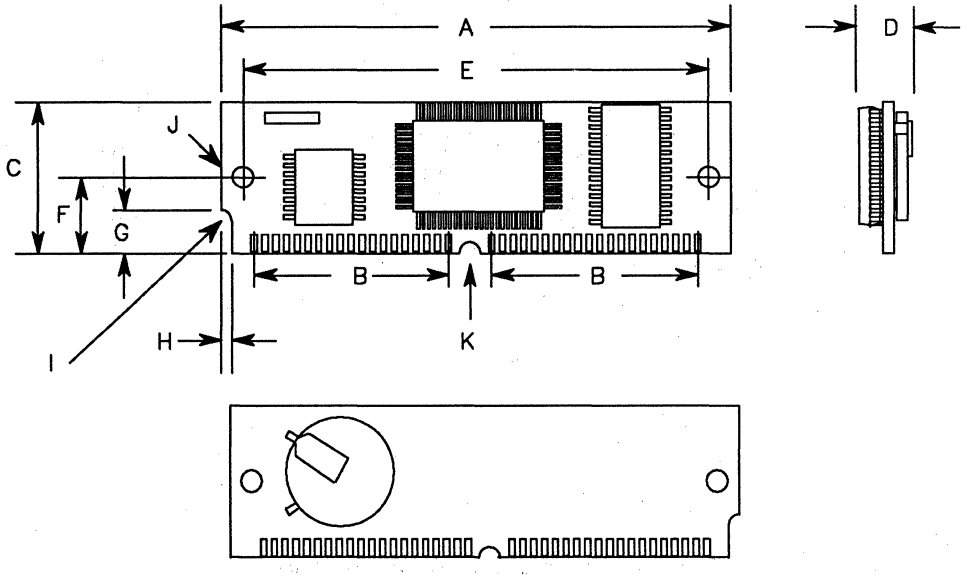
DS2250
Micro SipStik™

DIM.	INCHES
A	2.650
B	0.950
C	0.840
D	0.350
E	2.384
F	0.400
G	0.250
H	0.080
I	R .062
J	D 0.125



DS2250T
Time Micro SipStik™

DIM.	INCHES
A	2.650
B	0.950
C	0.840
D	0.350
E	2.384
F	0.400
G	0.250
H	0.080
I	R .062
J	D 0.125



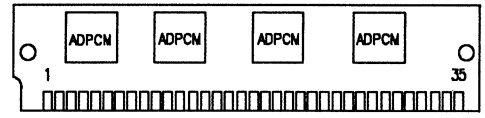
Dallas Semiconductor
ADPCM SipStik

PRELIMINARY
DS2264
DS2268
Available Fall 1988

FEATURES

- Four or eight channels of full duplex operation
- Can be cascaded in multiples of 4 or 8 up to 64 channels
- Based on the DS2167 ADPCM processor which meets T1Y1 recommendations and the "new" CCItt G.721 recommendations
- Dual PCM highway architecture with programmable TSACs
- Simple serial port interfaces to a microprocessor: used to assign timeslots and control processing
- On-board buffers for all critical signals and capacitors for decoupling
- Conforms to JEDEC 35 position SIMM
- CMOS processors for low power consumption
- Single +5V supply operation

PIN CONNECTIONS



PIN NAMES

VDD	-+5V supply
VSS	-Ground
A2HI	-Higher 4 channel select
A2LO	-Lower 4 channel select
A3-A5	-Card address
RST	-Reset
SDI	-Serial data input
SCLK	-Serial clock
CS	-Chip select
MCLK	-10MHz clock
XIN, YIN	-data input
XOUT, YOUT	-Data output
FSX, FSY	-Frame Syncs
CLKX, CLKY	-Clocks for data

1

DESCRIPTION

The DS2264 (4 channel) and DS2268 (8 channel) use the DS2167 in a surface-mount package to achieve a high density ADPCM array. The ADPCM SipStiks can be connected in parallel to obtain 64 channels of full duplex operation. For component information, see the DS2167 data sheet. For detailed product information,contact your local sales office.

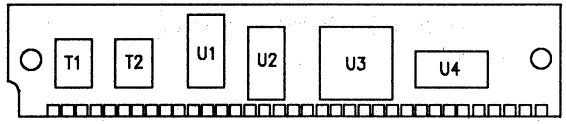
Dallas Semiconductor
T1/CEPT LINE CARD
SipStik

PRELIMINARY
DS2280/DS2281
Available Spring 1989

FEATURES

- Complete T1 or CEPT line card
- Performs the following functions:
  - line interface
  - framing
  - monitoring
  - buffering
- Includes transformers, line terminations, and capacitors
- Interfaces directly to transmit and receive twisted wire pair or coax
- Local and line loopback capability
- Separate analog and digital grounds and supplies for increased analog performance
- Conforms to JEDEC SIMM standard
- Simple serial interface port for use with microprocessor; used to control the card and monitor status of the line and the incoming data
- Fully CMOS for low power consumption
- Can operate off a single +5V supply

COMPONENT PLACEMENT



U1 - DS2186
U2 - DS2187
U3 - DS2180A (for DS2280) or DS2181 (for DS2281)
U4 - DS2175

DESCRIPTION

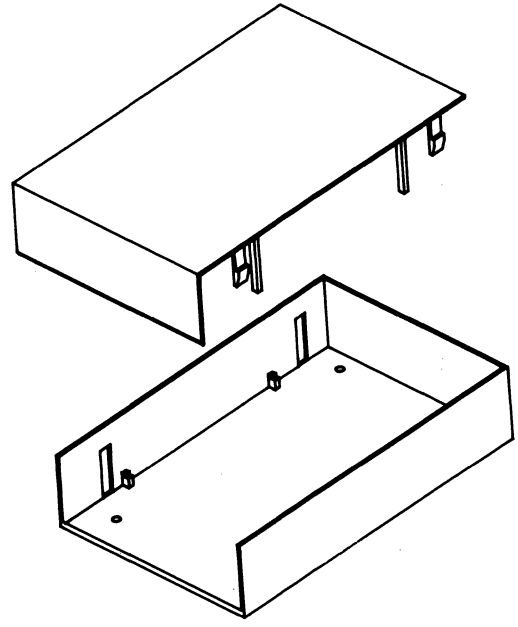
The DS2280 and DS2281 implement a complete line card function on a single 0.85" x 3.85" SIMM card. The DS2280 complies to the T1 standard (DSX-1 interface) while the DS2281 complies to the CEPT standard (0 to -6dB interface). For more component information, see the data sheets on the DS2180A, DS2181, DS2175, DS2186 and DS2187. To obtain detailed product information, contact your local sales office.

Dallas Semiconductor
EUROCARD ENCLOSURE

PRELIMINARY
DS9005

FEATURES

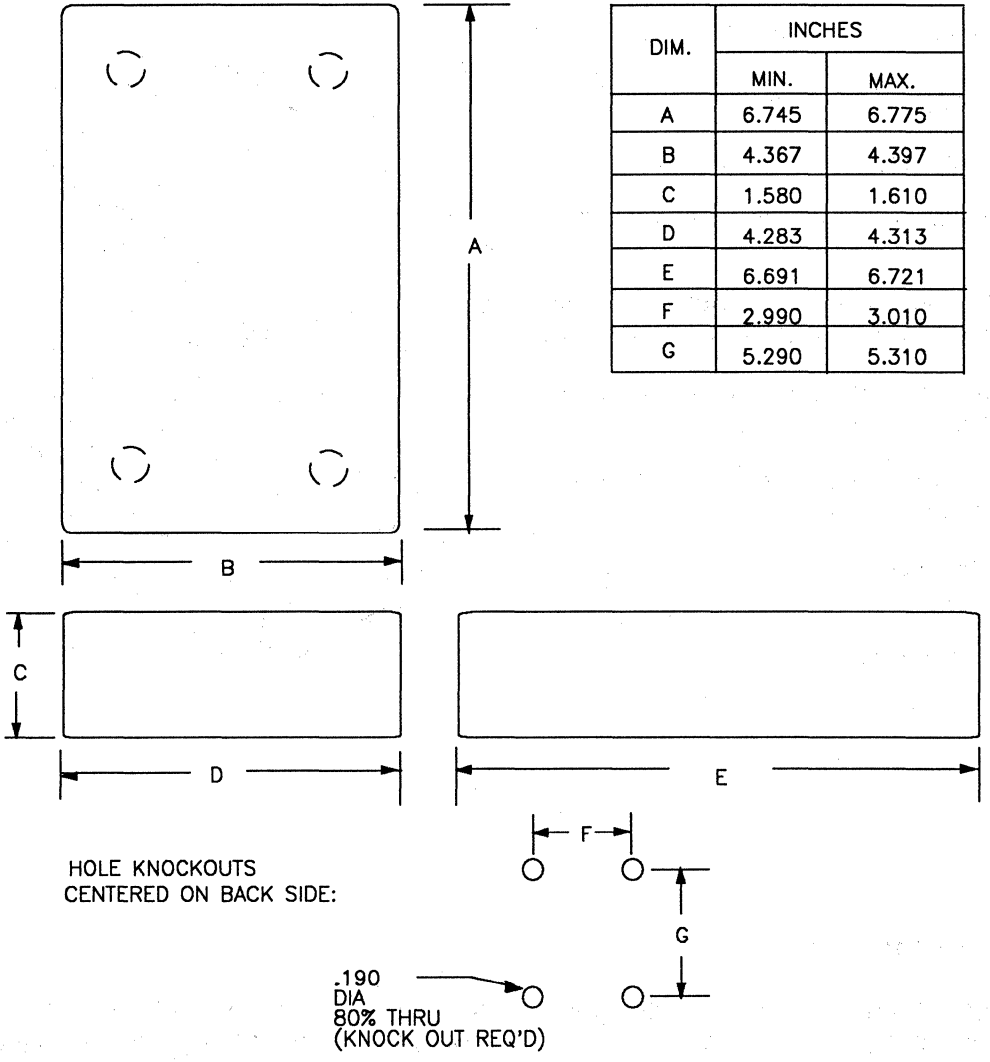
- Low cost molded enclosure
- Two piece snap together construction
- Made of rugged, flame retardant polyester PBT plastic
- Accepts DS9006 SipStik Motherboard or any other single size Eurocard printed circuit board
- Can be custom machined to allow for connector requirements
- Component clearance of .230" solder side, 1.000" circuit side using .062" board
- Smooth indents on bottom side for rubber bumpers
- Hole knockouts for mounting



DESCRIPTION

The DS9005 is a rugged, two piece snap together plastic enclosure for any stand alone system application. The PCB is offset in the enclosure to allow for components such as transformers and SipStiks to be positioned on topside of the board while still leaving room for standard I.C. packages and discretes on bottom side of the board. The housing is constructed of flame retardant polyester PBT to allow for applications requiring a very wide range of temperatures and is highly resistant to most chemicals. The size of the board and location of I/O connectors should match the DS9006 SipStik Motherboard. Applications can include control units, handheld remote communications, and security systems.

DS9005
EUROCARD ENCLOSURE



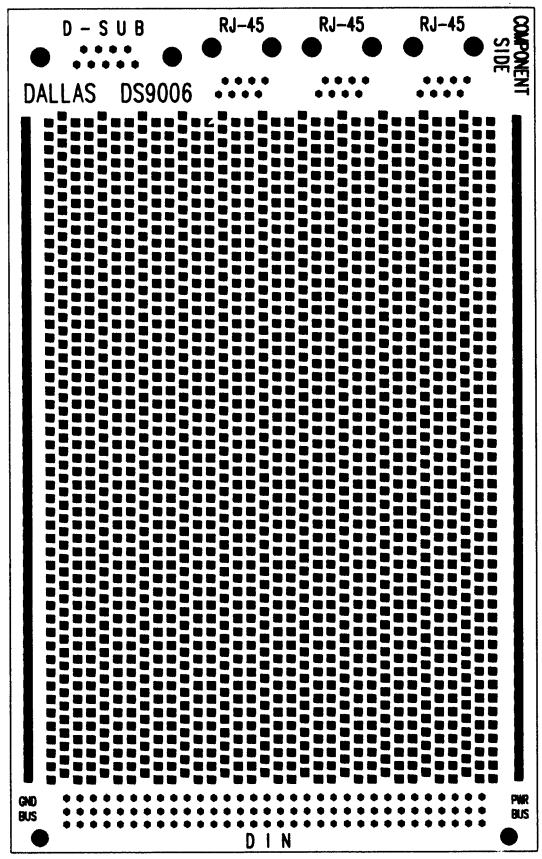
DIM.	INCHES	
	MIN.	MAX.
A	6.745	6.775
B	4.367	4.397
C	1.580	1.610
D	4.283	4.313
E	6.691	6.721
F	2.990	3.010
G	5.290	5.310

Dallas Semiconductor
SipStik™ MOTHERBOARD

PRELIMINARY
DS9006

FEATURES

- Fits into DS9005 molded enclosure
- Plated thru hole pattern for wire wrap or solder mount development
- Allowance for up to 12 SipStik connectors
- Hole layout for RJ45, D-SUB, and Eurocard DIN connectors
- Full length buses for distributing power and ground
- 1700 hole array for 0.1" center I.C.s and SipStiks



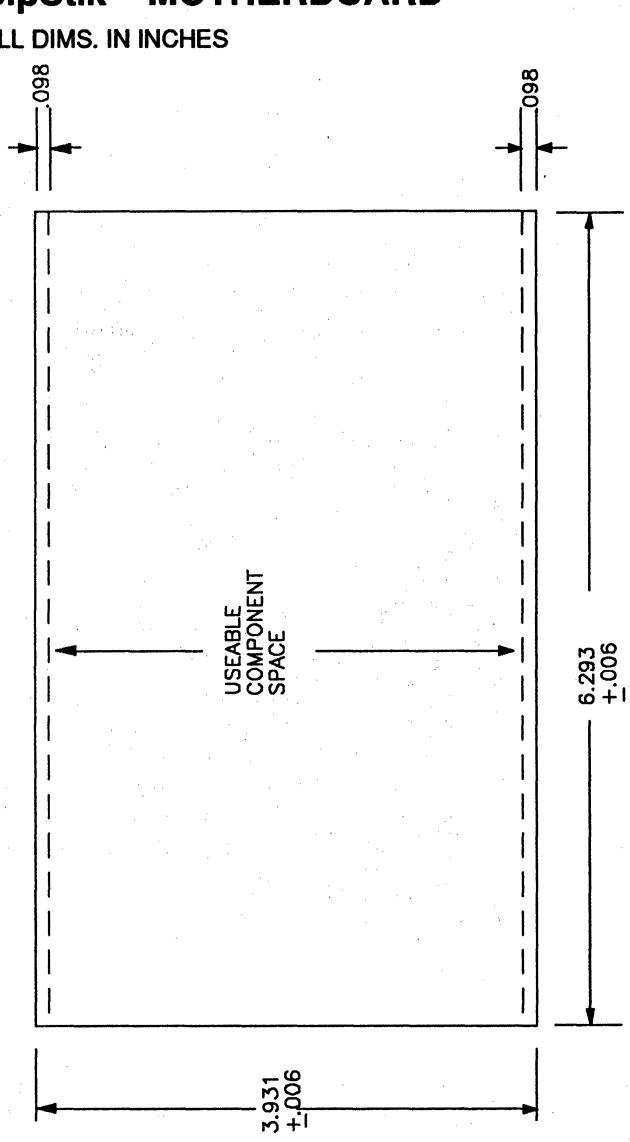
DESCRIPTION

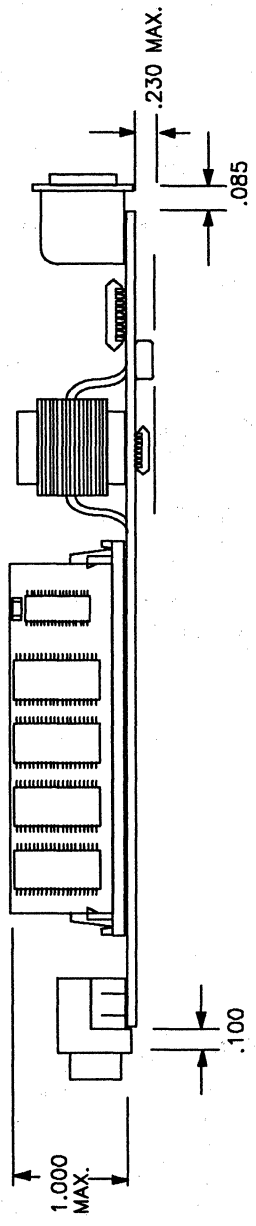
The DS9006 is a developmental printed circuit board for prototyping circuit designs which utilize SipStik prefabs and/or RJ11/45 connector schemes. Many Sipstiks mate with connectors that have staggered rows of pins. This makes it difficult to prototype these modules since most off-the-shelf wire wrap boards have a grid of 0.1" center holes. The DS9006 contains several rows of holes that are offset to accommodate both SipStiks and standard 300 mil and 600 mil DIPs.

Hole patterns for three RJ11/45, one 9-Pin D-SUB, and 64/96 Pin Eurocard connectors are located on ends of PCB in a right angle fashion to enable the finished circuit board assembly to mount in the DS9005 enclosure. This allows the designer to have a "complete" looking unit for presentation while still in the prototyping stage of design.

DS9006
SipStik™ MOTHERBOARD

ALL DIMS. IN INCHES





PCB THICKNESS:
.063" ± .007

SUGGESTED CONNECTOR

PART NUMBERS:

RJ45– AMP #520252–4
9–PIN D–SUB FEMALE– AMP #745781–1
DIN–64 POS. FEMALE AMP# 531796–2

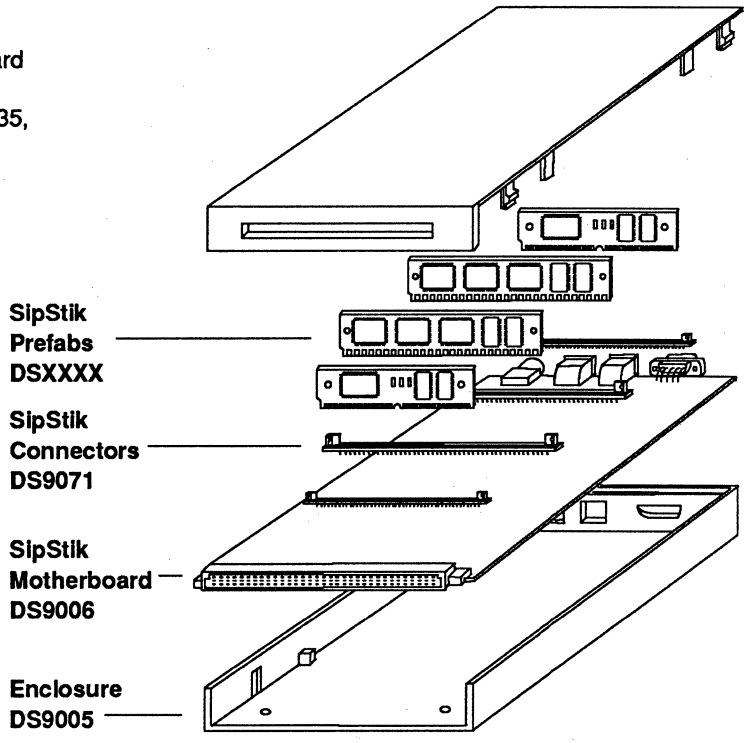
TYPICAL LAYOUT FOR
DS9005 ENCLOSURE

Dallas Semiconductor
SipStik™ PROTOTYPING KIT

PRELIMINARY
DS9006K

FEATURES
- DS9005 Molded Enclosure
- DS9006 SipStik Motherboard
- Sample connectors for 30, 35, and 40 contact SipStiks
- Adaptor pins for wire wrap
- Application note

3-D PACKAGING BOOSTS DENSITY



Eurocard Form Factor Shown.
SipStiks, RJ45, D-Sub, and DIN not included.

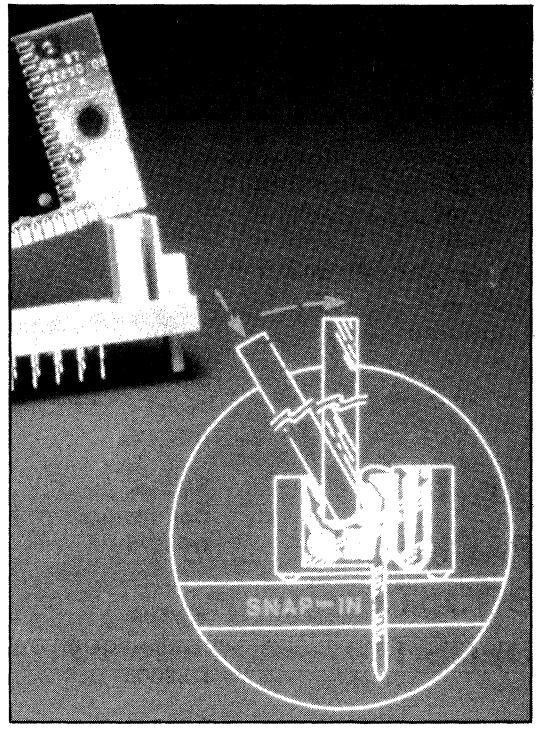
DESCRIPTION
The DS9006K includes a printed circuit board for prototyping SipStiks. The wire-wrapped unit may then be housed in a molded enclosure for stand-alone applications. An application note explains how to maximize the utilization of the DS9006 printed circuit board using SipStiks. See the data sheets for DS9005 and DS9006 for more information on these items.

Dallas Semiconductor
SipStik™ CONNECTORS

PRELIMINARY
DS9071
DS9072

FEATURES

- Provide snap-in connection between SipStiks and Motherboard
- Provide 200 grams min. contact force on JEDEC standard modules
- Redundant contacts
- Low insertion force
- Heat resistant housing (rated at 200 deg. C)
- .050" and .100" centerlines as specified in table below
- Reference AMP Inc. MICROEDGE™ SIMM connector catalog for more detailed specifications.



Part Number	Description	Ref. AMP Part #	Length in.
DS9071-30V	30 contact vertical pos. .100" pitch	821828-2	3.800
-30I	30 contact inclined pos. .100" pitch	821876-2	3.800
-35V	35 contact vertical pos. .100" pitch	821828-3	4.300
-35I	35 contact inclined pos. .100" pitch	821876-3	4.300
DS9072-40V	40 contact vertical pos. .050" pitch	821918-2	2.950

Wireless Products

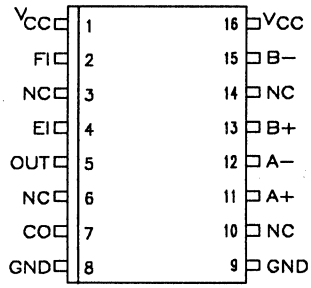
Dallas Semiconductor
MicroPower Receiver

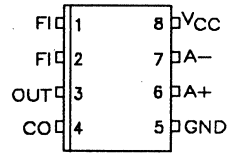
PRELIMINARY
DS1203 8-Pin SOIC
DS1203S 16-Pin SOIC

FEATURES

- Ultra low power listening gives longevity to the 3 volt supply.
- Input channels continuously listen for input signals up to 250 KHZ.
- 30 MV P-P input signal drives output to supply levels.
- Electronics freshness seal eliminates power consumption during storage.
- Dual input channels minimize the effects of antenna nulls.
- Interfaces directly with the DS1209 1-or-2 Wire Converter.
- Optional duty cycling can reduce listening power to even lower levels for special applications.
- Space saving 8 or 16 pin small outline surface pin mount package

PIN CONNECTIONS





PIN NAMES

Vcc	-	3 volt supply
GND	-	Ground
FI	-	Freshness Input
EI	-	Enable Input
OUT	-	Signal Output
CO	-	Cycle Output
A-,A +	-	Channel A Input
B-,B+	-	Channel B Input
NC	-	No Connects

DESCRIPTION

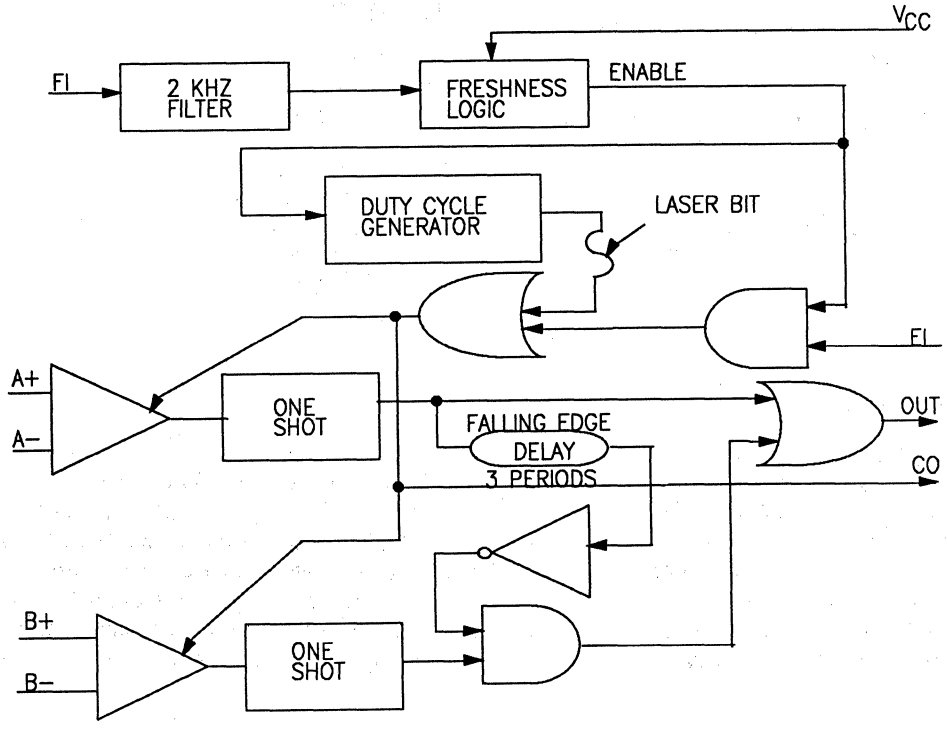
The DS1203 is an ultra low power dual comparator circuit designed to listen for signals of up to 250 KHZ. Input signals as small as 30 MV P-P are presented at the output as full power supply level signals. The dual comparator arrangement automatically selects the stronger of two signal sources, therefore, by using two orthogonal signal sensors null or dead spots are eliminated. The DS1203 makes an ideal front end for wireless communication links via RF, IR, ultra sound or magnetic field. The ultra low power feature allows remote applications to be permanently powered by a single three volt lithium energy source capable of lasting over ten years. A freshness seal can disconnect the power supply so that energy loss is even

avoided during periods of storage. The freshness seal is activated or deactivated via a 2 KHZ signal. In addition, the micropowered receiver has a duty cycle option which is laser definable by Dallas Semiconductor that can further reduce power consumption in special applications.

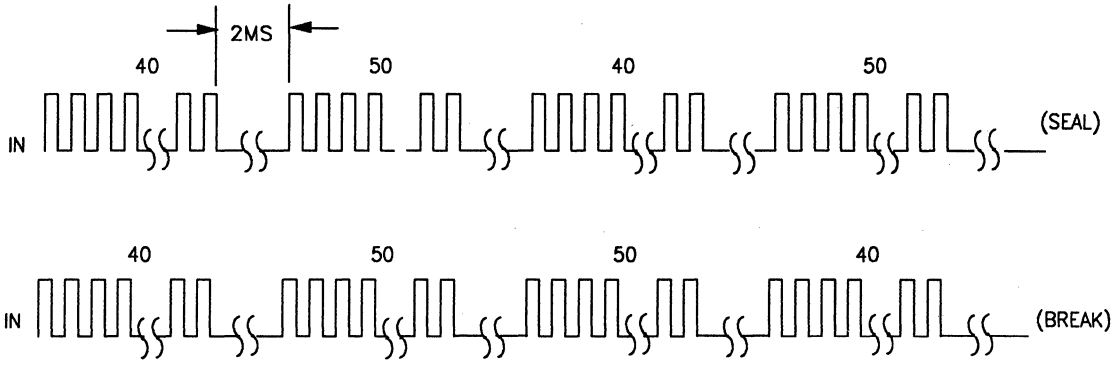
OPERATION

A block diagram of the DS1203 MicroPower Receiver is illustrated in Figure 1. As shown, the device consists of a dual comparator which can be enabled by any of three sources. The enable input (EI) can be used to turn on the comparators directly, provided the freshness seal has been enabled. Alternatively, a duty cycle generator can enable the comparators in percentages of on time and off time. This feature is enabled and disabled via a laser bit by Dallas Semiconductor. When the comparators are enabled, signals present at inputs A+ and A- and inputs B+ and B- of a magnitude of greater than 30 MV peak to peak produce voltage swings between power supply input and ground at the output. The output of comparator "A" is sent to an "OR" gate which normally passes the signal to the output (OUT) pin. However, if comparator "A" does not output a signal for three cycles at 200 KHZ, the "B" comparator output is sent to the "OR" gate which passes this signal to the output pin. In this manner, the output pin will always represent the input signal present at comparator "A" or comparator "B".

DS1203 BLOCK DIAGRAM FIGURE 1



FRESHNESS SEAL FIGURE 2



FREQUENCY RESPONSE
1.3 TO 2.3 KHZ

Freshness Seal

The freshness input (FI) is used to seal or start DS1203 power consumption. This input accepts 2 KHZ pulse packets at a signal level greater than one volt. The type of pulse packet shown in Figure 2 determines the state of the freshness seal. When the seal is broken, comparators "A" and "B" continuously listen for activity at the inputs. When the seal is in tact, no listening occurs and the DS1203 enters a no power consumption mode.

Duty Cycle Generation

An optional duty cycle generator on the DS1203 provides an additional aid in power savings. When engaged by Dallas Semiconductor, the duty cycle generator causes alternating periods of listening time and power down time. The amount of active time versus power down time is also laser settable by Dallas Semiconductor. The active time can be set from 1/64 to 63/64. The amount of on/off time is application dependent and is determined by special agreement between Dallas Semiconductor and the customer.

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to ground	-0.5V to +7V
Operating temperature	-0°C to 70°C
Storage temperature	-55°C to +125°C
Soldering temperature	-260°C for 10 sec.

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.5	3.0	5.5	volts	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	Volts	1,2
Input Logic 0	V_{IL}	-0.3		0.8	Volts	1,2
Input Sensitivity	V_{SIN}	20	30		MVolts	3
FI Input Logic 1	V_{IHF}	1.1		V_{CC}+0.3	Volts	1
FI Input Logic 0	V_{ILF}	-0.3		0.4	Volts	1

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC}=2.5 to 3.5V)

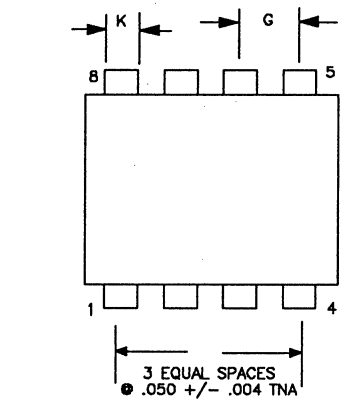
PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		1.0	uA	
Output Logic 1	V_{OH}	V_{CC}-0.3%			Volts	
Output Logic 0	V_{OL}			0.4	Volts	
Operating Current	I_{CC}			3	uA	6
Power Down Current	I_{CC1}			50	nA	4
Output Current Logic 1	I_{OH}			250	uA	
Output Current Logic 0	I_{OL}			500	uA	
Propagation Delay	t_{PD}			30	uS	5

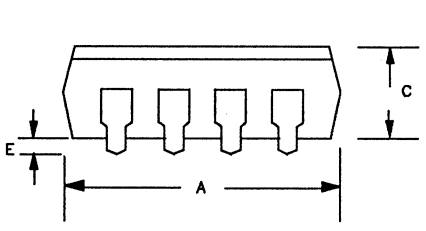
NOTES

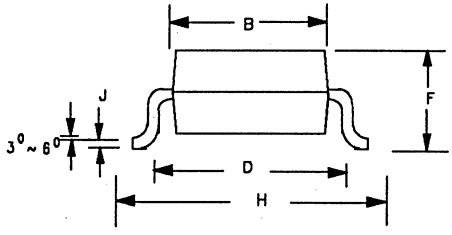
1.) All voltages are references to ground
2.) Applies to the EI pin only
3.) Applies to comparator "A" and "B"
4.) Power drain from Vcc input when freshness seal is on
5.) Propagation delay from "A" or "B" comparator to output
6.) Only for V_{CC}<3.5 volts

DS1203
MicroPower Receiver
8-Pin SOIC

DIM.	INCHES	
	MIN.	MAX.
A	.188	.195
B	.151	.157
C	.052	.058
D	.175	.193
E	.004	.010
F	.058	.064
G	.046	.054
H	.228	.240
J	.006	.011
K	.013	.019

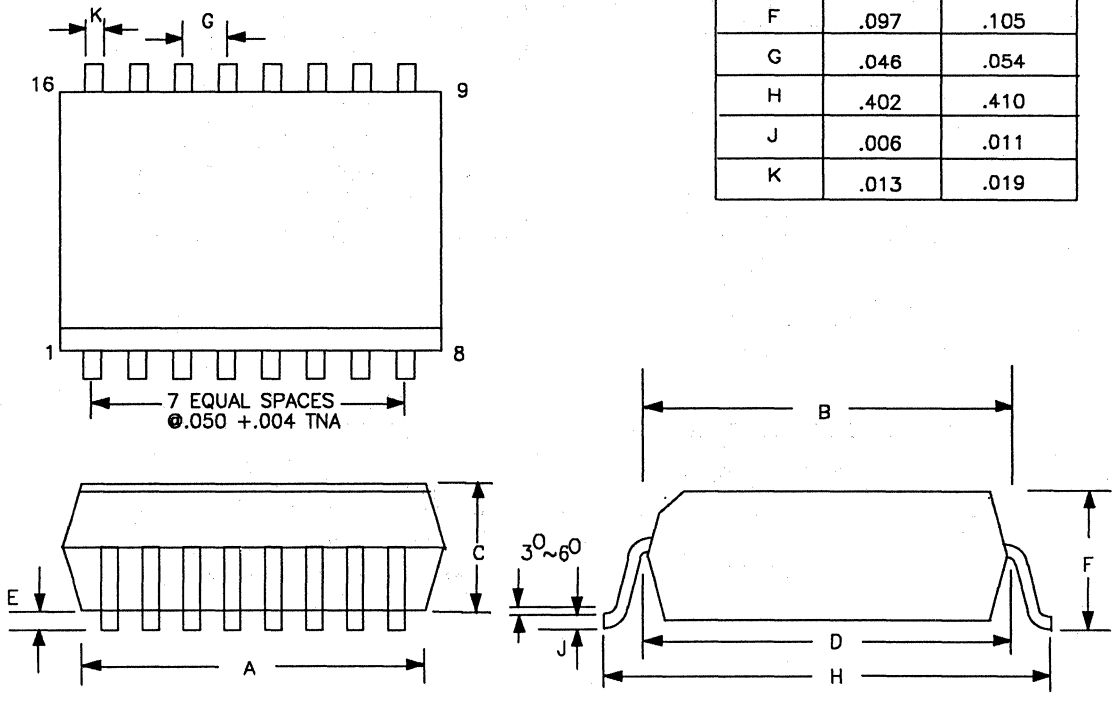






DS1203S
MicroPower Receiver
16-Pin SOIC

DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



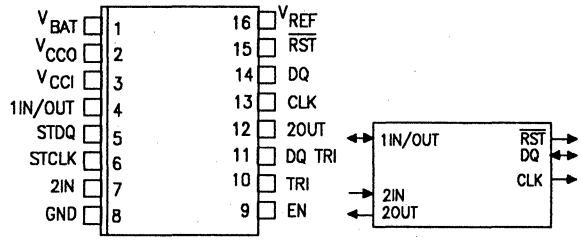
Dallas Semiconductor
1-or-2 to 3 Wire Converter

PRELIMINARY
DS1209S-20

FEATURES

- Adapts a 1-or 2-wire port to a 3-wire DQ, CLK and $\overline{RST}$ serial port
- Counts 200 KHz input pulse packets and generates commands; data Internal state machine interprets commands and routes data to and from the 3-wire serial port
- Input couples directly to the DS1203 Micro Power Receiver
- 3-Wire Serial Port output connects to the DS1201 Tag, DS1204 Key, DS5000 Microcontroller, or DS1280 3-wire to Bytewide Converter
- Stretched clock and data signals simplify microcontroller interface
- Low power operation for both battery backup and battery operate
- Bidirectional 100 KHz 1-wire port overrides 2-wire port
- Space saving 16-pin small outline package for surface mount
- Primary applications include IR, RF, and magnetic half duplex signals to a 3-wire serial port
- Makes allowances for extra or missing pulse induced by noise in the transmission path

PIN CONNECTIONS (tentative)



16–PIN SOIC DIAGRAM

PIN NAMES

V_{REF}	- Battery Reference
V_{BAT}	- +3 Volt Input
V_{CCO}	- Switch V_{BAT} or V_{CCI} output
V_{CCI}	- +5V Input
1IN/OUT	- 100 KHz 1-Wire Port
STDQ	- Stretched Data Input/Output
ST CLK	- Stretched Clock Input
2IN	- 200 KHz 2-Wire Port Input
EN	- Enable Active
GND	- Ground
TRI	- Tristate DQ, CLK, $\overline{RST}$
DQ TRI	- Tristate Only DQ
2OUT	- 2-Wire Port Output
$\overline{RST}$	- RESET 3-Wire Port
CLK	- Clock 3-Wire Port
DQ	-Data Input/ Output 3-Wire Port

DESCRIPTION

The DS1209 is a low power CMOS state machine designed to accept 200 KHz pulse packets at the 2-wire input and interpret these signals for data transfer to and from a 3-wire serial port. Some of the pulse packets are used as commands which control activity; however, most end up as data. This data is written to memory on the 3-wire port or extracted from memory and placed on the 2-wire output pin when data is being read. The output pin provides a return transmission link for data and can gate a variety of transmitting devices. Alternatively, the 1-wire port input/output pin can be used to accept 100 KHz pulse packets for commands and data coming in, and return data on the same pin. This 1-wire port is used as an override for the 2-wire port. The DS1209 also provides stretched clock and stretched DQ signals which can be synchronized to work with a microprocessor. A sophisticated power switching circuit is also provided for both battery backup and battery operate.

PIN DESCRIPTION

V_{BAT} - This input is designed to be connected to a lithium battery with a voltage range between 2.5 and 4 volts. When V_{CCI} is grounded, the DS1209 acts as a battery operate device and power is supplied from the V_{BAT} pin at all times. The V_{BAT} input should be grounded if not used.

V_{CCI} - This input is designed to be connected to a power supply with a voltage range of 4.5 to 5.5 volts. This voltage input is switched to V_{CCO} pin as long as V_{CCI} is greater than V_{BAT}. However, when V_{BAT} is the greater, its voltage will be present. When both V_{CCI} and V_{BAT} inputs are used, the DS1209 is in the battery backup mode. V_{CCI} should be grounded when not being used.

V_{CCO} - Switch V_{BAT} or V_{CCI} output. V_{CCO} will always be the greater of V_{BAT} or V_{CCI}.

V_{REF} - This output pin represents the battery voltage input (V_{BAT}) less 0.6 volts. It is designed to be connected to the battery input pin on the DS1204, DS1207, and DS1201 devices.

1IN/OUT - This input/output pin provides an override for standard 2- to 3-wire converter. The port pin acts as an input pin for 100 KHz pulse packets containing both command and data input to the 3-wire serial port. Data is also output on the same pin when memory content is read via the 3-wire serial port.

STDQ - This output contains the same data as the serial port DQ pin. The difference is that the data output remains valid until the ST CLK is transitioned high via an external source.

ST CLK - This input/output contains the same clock output as the serial port CLK pin. This pin differs in that an external source is required to drive the ST CLK pin high after the DS1209 has asserted it low.

2IN - This input accepts the 200 KHz pulse packets. In typical applications this pin is connected to the signal output pin of the DS1203.

EN - This output pin is active high when the protocol shift register has accepted a command for reading or writing data to the 3-wire serial port. In a typical application this pin is connected to the enable pin of the DS1203.

TRI - This input is used to tristate outputs CLK, $\overline{RST}$, and DQ. The TRI pin is active in a high state.

DQ TRI - This input is used to tristate the DQ pin only. The DQ TRI pin is active in a high state.

2OUT - This output pin contains the data which is output from the 3-wire serial port. In a typical application this pin is used to key the RF transmitter which will send data back to an RF Communicator via a 300 MHz loop.

$\overline{RST}$ - This output signal is the reset signal for the 3-wire serial port. When $\overline{RST}$ is at high level, the 3-wire port is active and data can be written into or read from the port.

CLK - This output signal is the clock signal for the 3-wire serial port. The clock signal synchronizes data into and out of the DQ line of the 3-wire serial port.

DQ - This input/output is the data input/output for the 3-wire serial port. In a typical application, $\overline{RST}$, CLK, and DQ connect directly to the $\overline{RST}$, CLK and DQ pins on the DS1204 Key, DS1201 Tag, DS1207 Timed Key, or DS1280 3-Wire to Bytewide Converter.

GND - This pin is the ground pin for the DS1209.

OPERATION

The principle blocks of circuitry which are contained within the DS1209 are shown in Figure 1. During normal input conditions, pulse packets present on the 2IN pin pass through the input selector to the pulse counter. The 1-wire port input is selected for data input by exception when data is present at the 1-wire port input. This data would override the 2IN pin. The 1-wire port pin will be discussed in more detail later in this text. Input pulses arriving at the pulse counter are deciphered into various command codes which affect the command prefix shift register, the state machine, and ultimately the 3-wire serial port. The various command codes are listed in Table 1.

Pulse packets are input to the pulse counter at 200 KHz with a 50 *us* dead time after the last pulse in each packet. The DS1209 uses the dead time to determine how many pulses were sent and the action to be taken. In addition, if input to the pulse counter is low (inactive) for longer than 1.5 ms, the DS1209 will time out, reset the command prefix shift register, and place the state machine into an inactive state. As can be seen in the Block Diagram of Figure 1 and the Command Codes listed in Table 1, the input pulses are sent in two different directions. If a pulse packet of 50 pulses (greater than 44) arrives at the pulse counter, the next 24 pulse packets are sent to the command prefix shift register, and the state machine is set inactive. The 50-pulse packet always sets the state machine to inactive regardless of any action which may have been occurring (aborts current action/conversation). The 24 pulse packets which go to the command prefix shift register will cause a normal wake-up or mask wake-up, a read of the chip select bits, a write of the chip select bits, or a lock of the chip select bits. The chip select bits make up the first 16 bits of the 24-bit command prefix shift register. The last eight bits comprise the function field. See Figure 2 and Table 2.

NORMAL WAKE-UP AND MASK WAKE-UP

The only difference between normal wake-up and mask wake-up is the number of chip select bits which must be matched to wake-up the state machine. For example, if a function code indicates the use of all chip select bits, then all 16 bits must be correctly matched to enable the main state machine. The following step by step procedure will illustrate normal and mask wake-up:

1. First a 50-pulse packet is sent to the 2IN pin which puts the state machine into a inactive state.

2. Issue wake-up or mask wake-up by sending the 8-bit function code followed by the 16 chip select bits which are proper to enable the state machine. The command prefix register is always loaded by sending write zeroes (10-pulse packets) or write ones (20-pulse packets). The loaded pulse packets are compared to values stored in the 8-bit Function Code Table and the previously stored 16 chip select bits (storing the chip select values will be covered later). When masking is being used, the first bits entered (LSBs) are the last to be masked. For example, Bits 0 and 1 will be the only bits unmasked if mask 2-15 is selected.

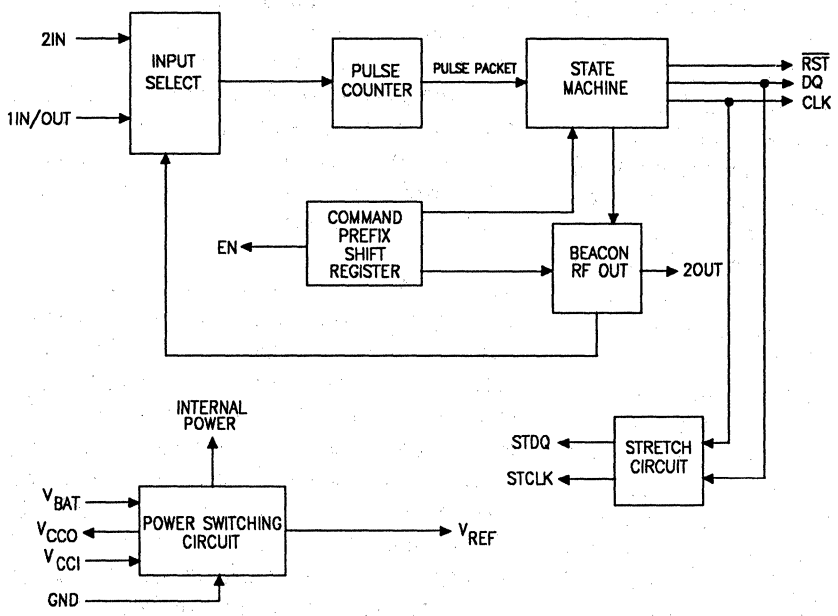
Pulse packets of 25 to 44 pulses are ignored when loading the command prefix shift register. A pulse packet of greater than 45 pulses always initializes the command prefix shift register back to starting with the LSB and aborts any previous transaction. The state machine is also set inactive. After the first 24 bits are received and a valid wake-up is decoded, the command prefix shift register will no longer allow data bits to be written into it and the enable output will become active and remain active until another 50-pulse packet is received to reinitialize. Subsequent pulse packets which are received will be directed to the state machine with action taken corre-

COMMAND CODES Table 1

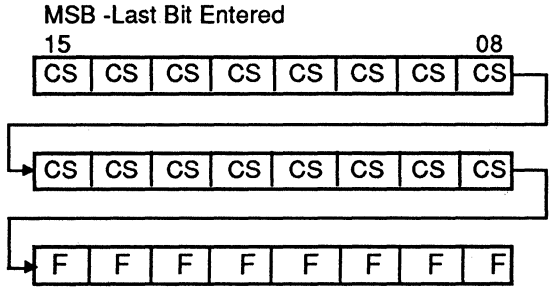
Number of Pulses			Command
Min.	Typ.	Max.	
5	10	14	Write 0 or READ
15	20	24	Write 1
25	30	34	Take $\overline{RST}$ High
35	40	44	Return to Inactive State
45	50		Initialize Protocol and Put State Machine Inactive

NOTE: Pulse packets are sent at 200 KHz with a minimum of 50 us. quiet time after each pulse packet and a maximum quiet time of approximately 1.5 ms.

DS1209 BLOCK DIAGRAM Figure 1



24-BIT COMMAND PREFIX SHIFT REGISTER BIT PATTERN Figure 2



FUNCTION CODES Table 2

FUNCTION	MSB			FUNCTION CODE				LSB	RESULTS
Wakeup	0	0	0	1	1	0	0	0	Mask All Bits
Wakeup	0	0	0	1	0	0	0	1	Mask All CS Bits 14 & 15
Wakeup	0	0	0	1	0	0	1	0	Mask CS Bits 12-15
Wakeup	0	0	0	1	1	0	1	1	Mask CS Bits 10-15
Wakeup	0	0	0	1	0	1	0	0	Mask CS Bits 8-15
Wakeup	0	0	0	1	1	1	0	1	Mask CS Bits 6-15
Wakeup	0	0	0	1	1	1	1	0	Mask CS Bits 4-15
Wakeup	0	0	0	1	0	1	1	1	Mask CS Bits 2-15
Wakeup	0	0	1	0	1	0	0	0	Use all CS Bits
Read CS Bits	0	0	1	0	1	0	1	1	Ignore CS Bits
Store CS Bits	0	0	1	0	1	1	0	1	Write all CS Bits
Lock CS Bits	0	0	1	0	1	1	1	0	Use all CS Bits

sponding to the number of pulses received as shown in Table 1. A pulse packet of a 40 pulses, followed by a 20-pulse packet, followed by a10-pulse packet enables the beacon mode of the state machine. Beacon mode turns on and off the OUT pin at a 5 KHz rate for 100 ms. In a typical application such as the DS6065 E-Key, this signal can be used to key a transmitter, (the DS6065 operates at 300 MHz) which allows a base unit to lock onto the transmitted beacon.

4. The DS1209 is now put into the active state by issuing a 30-pulse packet which takes $\overline{RST}$ high on the 3-wire serial port. This same 30-pulse packet also turns off the beacon if it has not already timed out. With $\overline{RST}$ high a conversation can now take place between devices placed on the 3-wire port (DS1201, DS1204, DS1207, or DS1280) from the 200 KHz input and data is returned to the sending unit via the 2OUT pin. As 200 KHz pulse packets continue to be received, the device attached to the 3-wire port will be written and read using 10- and 20- pulse packets and reset with a 40-pulse packet. When data is read from the 3-wire port, it is always sent to the 2OUT pin for transmission back to the sending 200 KHz unit.

5. If a 200 KHz 40-pulse packet is received, the state machine will go to an inactive state but still remain alert for new 200 KHz pulse packets.

6. If no 200 KHz pulse packets are received for more than 1.5 ms, the DS1209 will time out, initialize the command prefix shift register, and set the state machine back to the inactive state. The DS1209 now waits for new 200 KHz inputs to the protocol serial shift register which begins with a 50-pulse packet.

READING THE CHIP SELECT BITS (CS BITS)

The 16-bit CS value stored in the command prefix shift register can be determined in several ways. In fact, an exhaustive search could be implimented with a trial and error method which would eventually eliminate all but the correct bit pattern. Obviously, this method is painfully slow as 2^{16} possible combinations may need to be tried. In a similar but much more expedient manner, mask bits can be used in a successive approximation manner to determine the value of the CS bits. This procedure is accomplished by gradually increasing the size of the unmasked chip select fields as each set of bits are identified. However, the simplest method of determining the 16-bit CS value is to read the 16-bit value directly. The following step by step procedure will illustrate how to read the chip select bits.

1. Wake up the DS1209 using the mask all function code. This is accomplished by sending a 50-pulse packet followed by 24 10-pulse and 20-pulse packets. The first 8 pulse packets must match the mask all function code. The last 16 pulse packets may be any combination of 10- and 20-pulse packets as the 16 CS bits are masked. Next the beacon mode of the state machine is enabled by sending a 40-pulse packet followed by a 20- and then a 10-pulse packet. The beacon mode must be enabled when using an RF link with a scanning receiver, as the beacon will allow the receiver to lock on to the transmitter frequency. If the 1IN/OUT pin is used directly or if the 2OUT pin is read directly or indirectly by a non-scanning device, this step can be omitted. Finally, if the beacon mode has been enabled, it should be disabled after receiver lock on by sending a 30-pulse packet to the 2IN pin.

2. Now load the DS1209 command prefix shift register with the read CS bits function code. This is accomplished by sending a 50-pulse packet followed by 24 10- or 20-pulse packets. As before, the first 8 pulse packets must match the read CS bits function code. However, the last 16 pulse packets may be any combination of 10- and 20-pulse packets, as the 16 CS bits are ignored. During the 24-bit command prefix shift

register load, pulse packets of 30 and 40 are ignored. As usual, pulse packets of 50 will initialize the command prefix shift register and set the state machine inactive.

3. If the 8-bit function code in the command prefix shift register is correctly matched, then for each 10-pulse packets (read command) received at the 2IN pin, one bit of the 16-bit CS field will be read at the 2OUT pin, the LSB of the field appearing first. Thus, it will receive 16 packets of 10 pulses each to read the entire CS field. If more than 16 read pulse packets are sent to the 2IN pin in this mode, the DS1209 will start over again reading the CS bits, beginning with the first bit. Pulse packets of 20, 30, or 40 pulses are ignored and 50-pulse packets will initialize the command prefix shift register and set the state machine inactive. This is a non-destructive read and can be aborted at any time during the read process.

4. During the entire CS bit read operation, the state machine is disabled. All pulse packets except the 50-pulse packet are ignored by the state machine. As usual, the 50-pulse packet or a time out of 1.5 ms will initialize the command prefix shift register and return the state machine to inactive.

STORING THE CHIP SELECT BITS

In order to store a new value into the chip select bits of the protocol shift register, it is necessary to know the existing stored value. In addition, if the lock bit is set, a new value for the chip select bits cannot be stored unless power is removed and reapplied. The lock function is only useful in applications where power is permanently applied or removed by exception. The existing value of the CS bits should be obtained using the "Read Chip Select Bits" described earlier. After obtaining the existing chip select values, a new value can be entered by using the step-by-step procedure which follows.

1. Load the proper 24-bit pattern into the command prefix shift register for storing the chip select bits. This pattern consists of 24 10-pulse and 20- pulse packets. The first eight packets must match the stored CS bits function code. The last 16 pulse packets must match the existing CS bits. During the 24-bit shift register load, only 10- and 20-pulse packets are accepted while 20-, 30-, and 40-pulse packets are ignored. As always, 50-pulse packets will initialize the command prefix shift register and set the state machine inactive.

2. If the 8-bit function code and the 16 CS bits are correct, the next 16 pulse packets will store a new CS value, overriding the old CS bits. Only 10-pulse and 20-pulse are accepted. Pulse packets of 30 and 40 are ignored and 50-pulse packets cause the stored CS bit command to abort, initializing the command prefix shift register and return the state machine to inactive. The DS1209 does not lock up after 16 pulse packets are sent in this mode. If more packets are sent, the new packets will continue to shift in, storing the last 16 packets that are received.

3. During the entire store CS bits operation, the main state machine is disabled. All pulse packets received will have no effect on the state machine except the 50-pulse packet, which will initialize the commmand prefix shift register and return the state machine to an inactive state. A time out of 1.5 ms will have the same effect as a 50 pulse packet.

LOCKING THE CHIP SELECT BITS

The design of the DS1209 allows for both battery backup and battery operation. The device also consumes only modest amounts of power. As a result, most applications for this device are permanently powered and memory elements within the device, like the command prefix shift register CS bits, are nonvolatile. A speciai latch is provided so that upon initial power up (when battery is first connected) the nonvolatile chip

select bits can be written with a store CS function code. The CS bits can be changed as often as desired, using the store function until a lock CS function code is issued. Once sent, the value of the chip select bits cannot be changed until power is removed (battery disconnected) from the DS1209. The lock CS bit can be accomplished by the following step-by-step procedure.

1. If the CS value is unknown, the procedure for reading the CS bits should be followed so that the value is known.

2. The 8-bit function code for locking the CS bits is transmitted followed by the 16-bit chip select value. Only 10- and 20-pulse packets are accepted and 30- and 40-pulse packets are ignored. A 50-pulse packet will cause the lock CS bits to abort, initializing the command prefix shift register and returning the state machine to the inactive state.

3. Once the 24-bit command prefix shift register is loaded with an exact match for the CS bits and the lock CS function code, the latch is set automatically and no further action is required.

4. The only way the latch can be reset is to remove power (the battery) from the device. During the lock CS operation the main state machine is disabled so that all pulse packets have no effect. As usual, a 50-pulse packet or a time out of 1.5 ms will initialize the command prefix shift register and return the state machine to inactive.

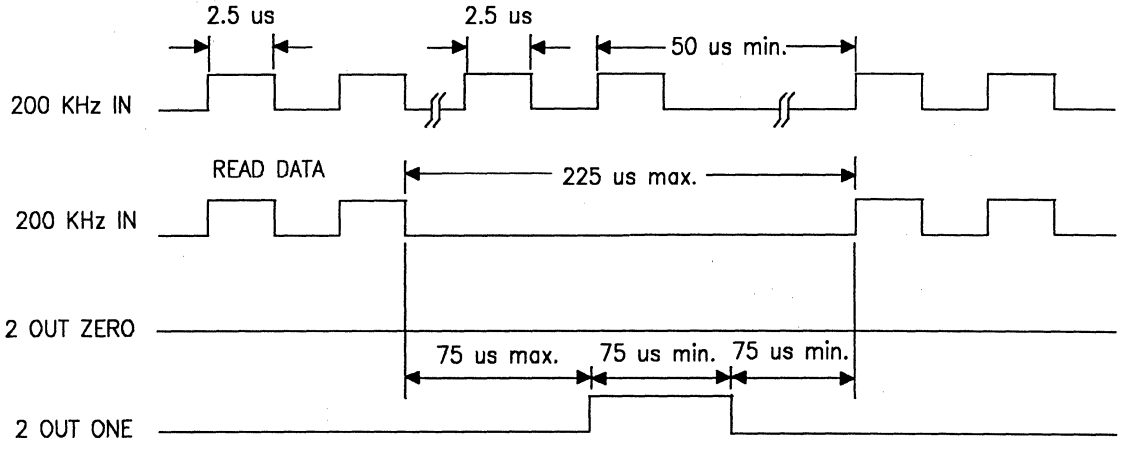
POWER SWITCHING CIRCUIT

As shown in the Block Diagram of Figure 1, the DS1209 can receive its power source from two different sources: namely, the V_{CCI} input or the V_{BAT} input. The DS1209 is designed to work off of a battery supply as low as 2.5 volts. However, if an alternate supply is available, it can be connected to the V_{CCI} pin. A voltage level of 3 volts minimum is required on the V_{CCI} pin for proper operation. With both the V_{CCI} pin and the V_{BAT} pin attached to appropriate power sources, the DS1209 will automatically select the supply input which is the higher level. If only one power source is connected, the other must be grounded for proper operation. The V_{REF} output is designed specifically to supply power to a connected DS1204, DS1201, DS1207 or a DS1280. The V_{REF} output is equal to the V_{BAT} input less a voltage drop of about 0.5 volts. This pin is capable of sourcing a current of 2 mA.

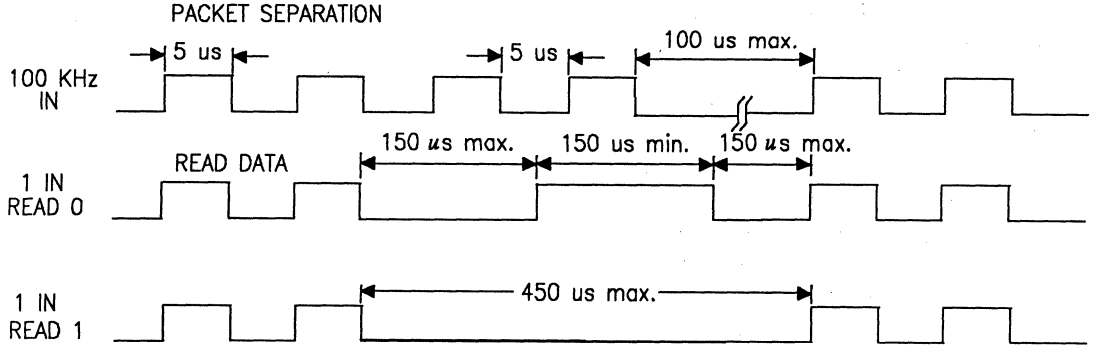
2IN 200 KHz INPUT

The 200 KHz input accepts wave signals with a symmetrical high and low time of 2.5 *us* +/- 20%. The minimum time between pulse packets is 50 *us* and the idle time of 1.5 ms will always cause the protocol shift register to initialize and the state machine to go inactive. Pulse packets range from 10 pulses to 50 pulses, depending on the action to be taken (see Command Codes in Table 1). If a read pulse packet is detected, data is to be read from a device connected on the 3-wire serial port and the 2OUT pin will become active high for a logic one or remain low for a zero. Time is allotted beyond the 50 *us* between pulse packets for the DS1209 to send out a one or a zero. This time is specified as a 225 *us* window. If a logic zero is being sent, the 2OUT pin will remain low for the entire window. If a logic one is being sent, the 2OUT pin will be driven to high level within a maximum of 75 *us* and will remain high for a minimum of an additional 75 *us*. However, if a minimum of four 200 KHz pulses are received at the 200 KHz input, the 2OUT pin activity is terminated on the assumption that a logic one has been received and the sending unit has started the next pulse packet. The 2OUT pin is guaranteed to be inactive after a third 75 *us* time period. The timing diagram of Figure 3 illustrates the 200 KHz 2IN pin and the 2OUT pin timing relationship.

2IN 200 KHz INPUT TIMING Figure 3



1 INPUT/OUTPUT TIMING Figure 4



1INPUT/OUTPUT

This pin is an input/output one-wire signal port designed to override the 200 KHz 2IN pin and multiplex the 2OUT pin on a single connection. Data is input on the Port pin using a 100 KHz frequency with a symmetrical high and low time of 5 *us* +/- 20%. Therefore, the time between pulse packets is 2X the time allotted between pulse packets when 200 KHz is used. If a read pulse packet is detected, time is allotted beyond the 100 *us* between pulse packets for the DS1209 to send out a one or a zero. This time is specified as a 450 *us* window. If a logic one is being sent, the 1IN/OUT pin will remain low for the entire window. If a logic zero is being sent, the 1IN/OUT pin will be driven high within a maximum of 150 *us* and remain high for a maximum of 150 *us*. The 1IN/OUT pin is guaranteed to be inactive after a third 150 *us* time period. The timing diagram of Figure 4 illustrates the 1INPUT/OUTPUT timing.

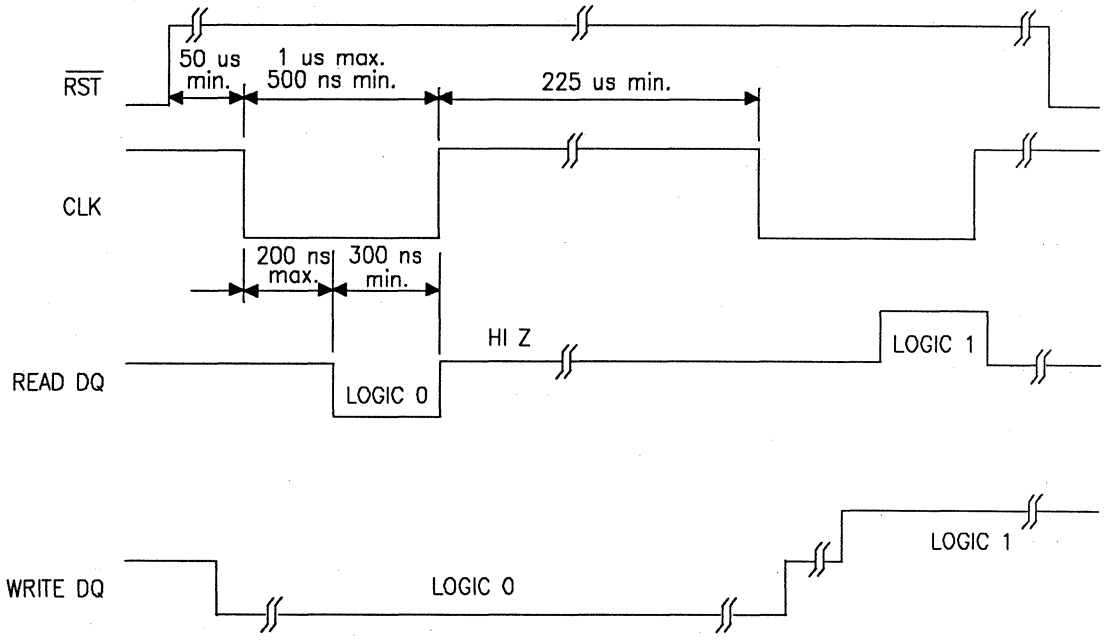
$\overline{\text{RST}}$, CLK, AND DQ

The 3-wire serial port on the DS1209 consists of the $\overline{\text{RST}}$, CLK and DQ signals. These signals are designed to connect directly to the CLK, $\overline{\text{RST}}$ and DQ lines of the DS1204, DS1207, DS1201, or DS1280. The $\overline{\text{RST}}$ pin on the DS1209 is driven to a high level whenever a 30-pulse packet is received by the state machine. The $\overline{\text{RST}}$ signal remains high until a 40- or 50-pulse packet is received or until 1.5 ms has elapsed without activity at the 200 KHz input. The CLK pin on the DS1209 is normally high and will remain high until the $\overline{\text{RST}}$ signal is high. When $\overline{\text{RST}}$ is high and a 10- or 20-pulse packet is received by the state machine (indicating a "read from" or "write to" the 3-wire port), the CLK pin is driven low for a period of 500 ns minimum to 1.0 *us* maximum. If data is being read from a device on the 3-wire serial port, it will become valid within 200 ns of the falling edge of the clock and remain valid until the clock returns high. This data is transferred to the 2OUT pin after a time delay of 75 *us* maximum where the data can be returned to the sending unit. The output will be a high level for a logic one or remain at low level for a logic zero. If data is being written to a device on the 3-wire serial port, then data will be sent from the state machine to the DQ line prior to the falling edge of the clock. This data will remain valid until the clock transitions back to a high level. The 2OUT pin remains low while data is being written to the 3-wire serial port. A timing diagram for the 3-wire serial port is shown in Figure 5. For more detailed information on the 3-wire serial port, see the data sheets on the DS1201, DS1207, or DS1280.

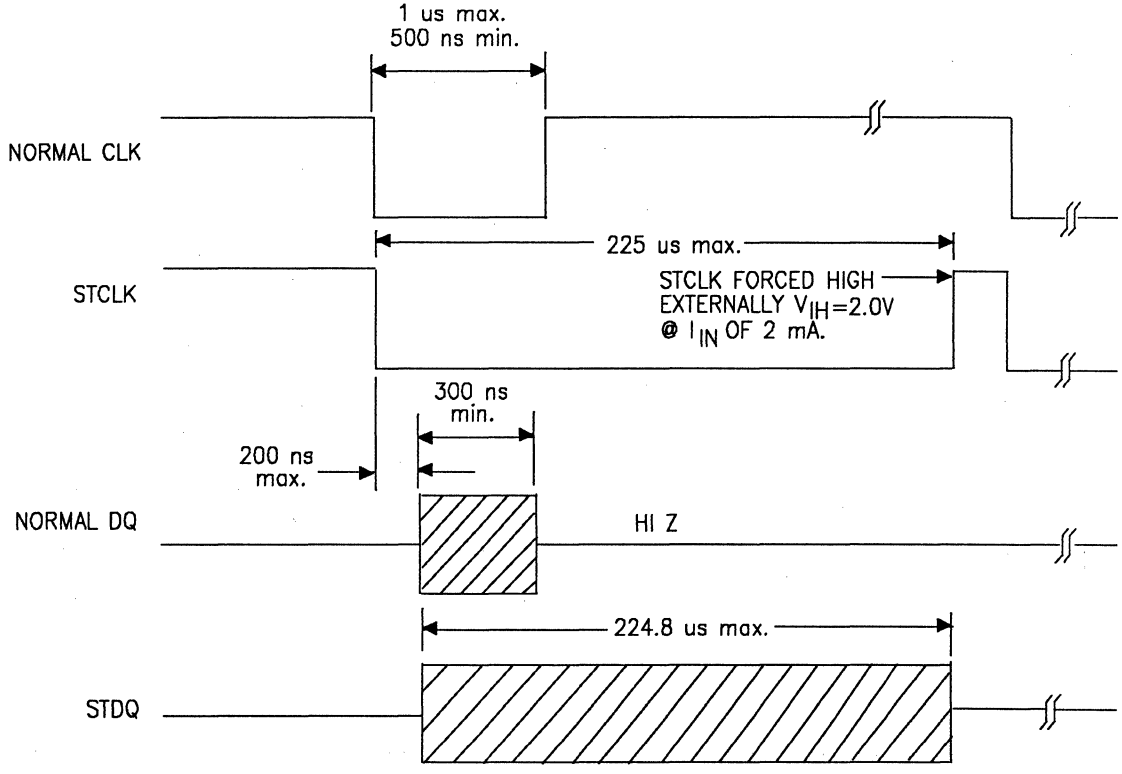
STRETCH DATA OUTPUT AND STRETCH CLOCK

The ST CLK and ST DQ pins are similar to the CLK and DQ pins on the 3-wire serial port. When CLK goes low on the 3-wire serial port, the ST CLK is also pulled low by the DS1209. This signal tells a monitoring device that the ST DQ pin contains data and that this data matches the data on the normal DQ pin. When the normal CLK goes high, however, ST CLK and ST DQ both remain valid. This allows time for a monitoring device to capture the data. Once the monitoring device retrieves data, the ST CLK signal must be forced to high level externally. In this manner the monitoring device will terminate the cycle and the ST DQ line will go to high impedance. Figure 6 illustrates ST DQ and ST CLK timing.

$\overline{\text{RST}}$ CLK AND DQ TIMING Figure 5



ST DQ AND ST CLK TIMING Figure 6



ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	- 0.5V TO +7V
OPERATING TEMPERATURE	- 0° TO 70° C
SOLDERING TEMPERATURE	- 260° FOR 10 SEC.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C TO 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Input	V_{CCI}	3.0	5.0	5.5	Volts	1,2
Battery input	V_{BAT}	2.5		4.0	Volts	1,2
Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	Volts	1,3
Input Logic 0	V_{IL}	-0.3		0.8	Volts	1

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5 VOLTS V_{BAT} =3 VOLTS 0°C TO 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Battery Reference	V_{REF}	V_{BAT} -0.7		V_{BAT}	Volts	1
Switched Voltage Out	V_{CCO}	V_{CCI} -0.3			Volts	1,4
Switched Current Out	I_{CCO}	3	4		mA	5
Operating Current	I_{CC}		2	4	uA	6
Standby Current	I_{cc1}			50	nA	7
Output Logic 1	V_{OH}	V_{CC} -10%			Volts	1,3
Output Logic 0	V_{OL}			0.4	Volts	1
Output Current Logic 1	I_{OH}			250	uA	
Output Current Logic 0	I_{OL}			500	uA	
Leakage Current	I_L	-1.0		1.0	uA	8

NOTES:

1. All voltages are referenced to ground.

2. When both the battery and supply pins are being used, V_{CCI} should be at leat 500 mv higher than V_{BAT} when V_{CCI} is supplying power.

3. V_{CC} applies to the greater of V_{CCI} or V_{BAT} depending on which input is supplying power.

4. V_{CCO} is either V_{CCI} -0.3 V or V_{BAT} -0.3 V.

5. I_{CCO} is current coming from V_{BAT} or V_{CCI} depending on which input is supplying power.

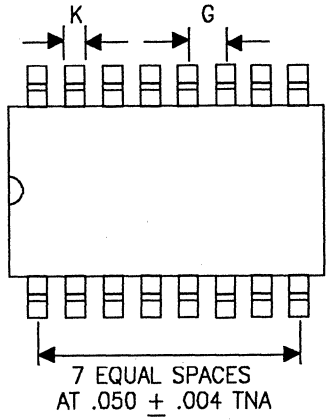
6. Operating current comes from V_{CCI} or V_{BAT} depending on which is supplying power and if power consumed by the DS1209 when 200 KHz or 100 KHz is active.

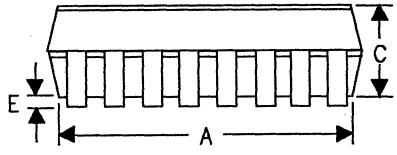
7. Standby current is measured with no 200 KHz or 100 KHz activity and all outputs open.

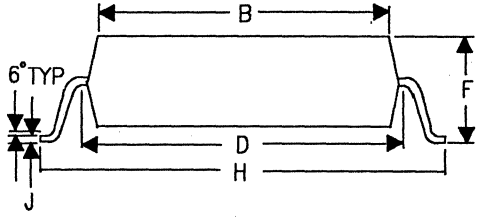
8. Leakage current applies to all inputs except V_{CCI} and V_{BAT}.

1-OR-2 TO 3 WIRE CONVERTER
DS1209S-20
16-PIN SOIC

DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019







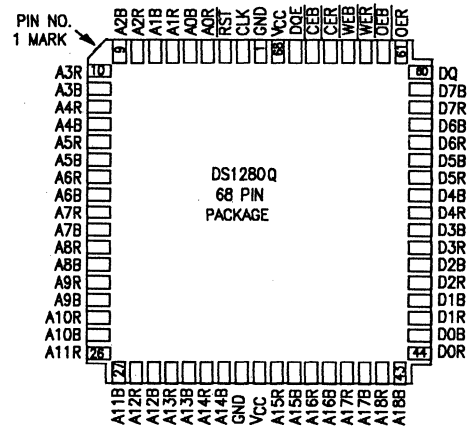
Dallas Semiconductor
Byte Wide To Serial Converter

PRELIMINARY
DS1280Q
DS1280FP

FEATURES

- Adapts JEDEC byte wide memory to a 3 wire serial port
- Supports 512K bytes of memory
- Provides arbitration mechanisms for dual port operation
- CMOS circuitry design for battery backup and battery operate applications
- Cyclic redundancy check monitors serial data transmission for error
- 68 pin PLCC surface mount package.
- Optional 80 pin Quad Flat Pack for high density requirements

PIN CONNECTIONS



PIN NAMES

$\overline{RST}$ - Reset For Serial Port
DQ - Data Input/Output For Serial Port
CLK - Clock Input For Serial Port
$\overline{DQE}$ - Serial Port Active Output
$\overline{CEB}$ - System Bus Enable
$\overline{OEB}$ - System Bus Read Enable
$\overline{WEB}$ - System Bus Write Enable
A0B-A18B - System Address Bus
D0B-D7B - System Data Bus
$\overline{CER}$ - Ram Chip Enable
$\overline{WER}$ - Ram Write Enagle
$\overline{OER}$ - Ram Output Enable
A0R-A18R - Ram Address Bus
D0R-D7R - Ram Data Bus
GND = Ground
Vcc = +5 Volts

DESCRIPTION

The DS1280 adds a 3 wire serial port to a byte wide Static RAM yet maintains the existing bytewide port. Memory capacity of up to 512K bytes can be addressed directly. Arbitration between the serial and byte wide port is accomplished by handshaking or using predictable idle time as an access window. The serial port requires a six byte protocol to set up memory transfers. Cyclic Redundancy Check circuitry is included to monitor serial data transmission for error.

Pin Description

$\overline{RST}$ - The 3 wire serial port selection signal input. When RST is low, all communications to the serial port are inhibited. When high, data is clocked into or out of the serial port.

CLK - The clock input signal is used to input or extract data from the 3 wire serial port. A clock cycle is defined as falling edge followed by a rising edge. Data is driven out onto the 3 wire bus after a falling edge during read cycles and latched into the port on the rising edge during write cycles.

DQ - The DQ signal is the bidirection data signal for the 3 wire serial port.

DQE - The DQE output signal is active (high level) whenever the 3 wire serial port is driving the DQ line. Therefore, this pin will be high whenever data is being read. Otherwise it will be low and the DQ line will be an input. This signal can be used as a means of tri-stating the DQ driver on the other end.

$\overline{CER}$ - Chip enable output to RAM. This signal is asserted active (low) during RAM read or write cycles. This signal is either derived from the system bus chip enable ($\overline{CEB}$) or from a 56-bit protocol provided by the 3 wire serial port and associated timing circuits.

$\overline{WER}$ - Write enable output to RAM. This signal is asserted active (low) during RAM write cycles. This signal is either derived from the system bus write enable ($\overline{WEB}$) or from a 56-bit protocol provided by the 3 wire serial port and associated timing circuits.

$\overline{OER}$ - Output enable to RAM. This signal is asserted active (low) during RAM read cycles. This signal is either derived from the system bus read enable $\overline{OEB}$ or from a 56-bit protocol provided by the 3 wire serial port and associated timing circuits.

A0R-A18R - Addresses supplied to RAM. These signals allow access to up to 512K bytes of RAM controlled by the DS1280. The addresses are either derived from the system address bus (A0B-A18B) or from the protocol and internal binary counter provided by the 3 wire serial port and associated timing circuits.

D0R-D7R - Data bus supplied to RAM. These eight signals comprise the bidirectional data bus between external byte wide RAM and the DS1280. This data bus is either derived from the system data bus (D0B-D7B) or from the protocol and data stream provided by the 3 wire serial port and associated timing circuits.

$\overline{CEB}$ - System bus chip enable to the DS1280. This signal is used to generate the RAM chip enable for transfer of data to and from the parallel system bus to RAM.

$\overline{OEB}$ - System bus output enable (read) for transfer of data from RAM to the parallel system bus.

$\overline{WEB}$ - System bus write enable to the DS1280. This signal is used to generate the RAM write enable for transfer of data from the parallel system bus to the RAM.

A0B-A18B - System bus addresses to the DS1280. These signals are used to specify the address location for data transfer to and from RAM.

D0B-D7B - System data bus to and from the DS1280. This bidirectional bus is used to carry data to and from the parallel system bus and RAM.

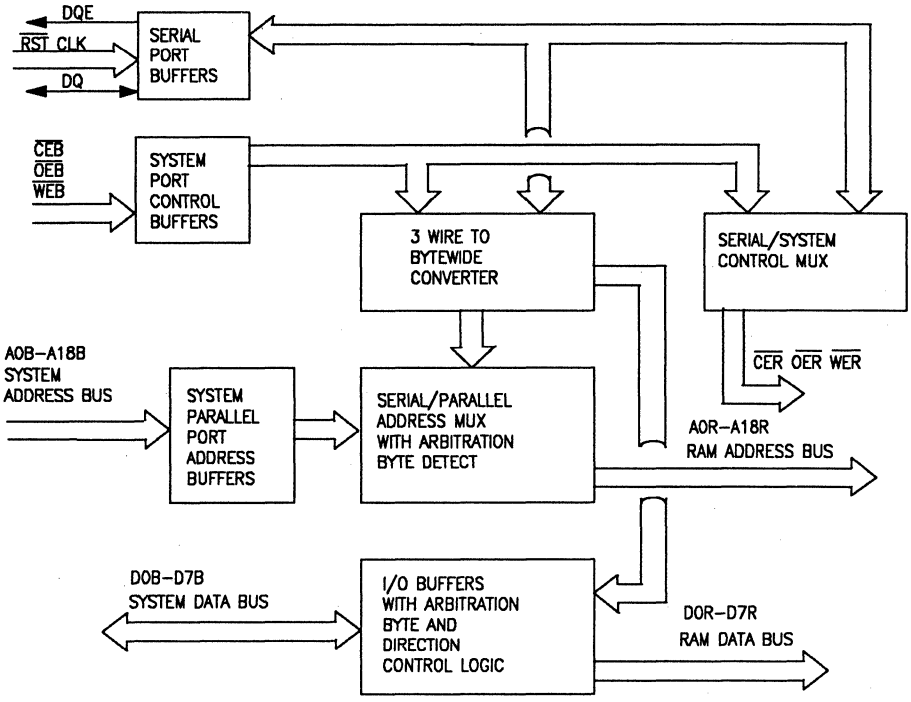
Vcc+5volt power from the DS1280 (2 pins).

GND - Ground for the DS1280 (2 pins).

Operation

The block diagram of Figure 1 illustrates the main elements of the DS1280. As shown, the DS1280 has two major sections; a 3 wire to byte wide converter, and a serial/parallel multiplexer. The source of the serial/parallel multiplexer is either a 3 wire serial port or a byte wide system bus. Arbitration of the serial/parallel multiplexer is controlled by signals from the 3 wire to byte wide converter. The 3 wire serial port, therefore, has priority in accessing the RAM and the methods used to avoid collisions are primarily directed by the 3 wire to byte wide converter.

DS1280 BLOCK DIAGRAM Figure1



Operation - System Byte Wide Parallel Bus
If the RST signal for the 3 wire serial port is low (inactive), the byte wide parallel port can access associated RAM directly. The byte wide parallel bus addresses (A0B-A18B) and control signals (CEB, OEB and WEB) are buffered by the DS1280 and become outputs A0R-A18R, CER, OER, and WER respectively, which are connected directly to RAM. The data input/output signals (D0B-D7B) are internally buffered and sent to RAM on the data input/output signals D0R-D7R. The buffering is designed to handle bidirectional data transfer. Data will be written from the byte wide parallel bus to RAM when CEB and WEB inputs are both active (low). The OEB signal is a "don't care" signal during a write cycle. Data is read from RAM via the byte wide parallel port when CEB and OEB signals are both low and WEB is high.

Operation - 3 Wire Serial Bus
If the RST signal for the 3 wire serial port is active (high), the 3 wire to bytewide converter controls the RAM through the control/address/data multiplexers. The 3 wire to bytewide converter uses a 56-bit protocol written serially using RST, DQ, and CLK to determine the action required and also the starting address location in the RAM to be used. Data is entered into the 3 wire while RST is high on the low to high transition of the CLK signal provided the data is stable on the DQ line with the proper setup and hold times. The last 8 bits of the 56 bit protocol is a cyclic redundancy check byte (CRC) that ensures that all bits of the protocol

have been received correctly. If the 56 bits of protocol have not been received correctly, further action will be aborted. The CRC check byte can catch up to three single bit errors within the 56 bit protocol and can also be used on incoming and outgoing serial data streams to check the integrity of data being read or written. More discussion on CRC use and CRC generation will follow later in this text.

Protocol - 3 Wire Serial Bus

The 3 wire serial bus protocol can cause eight different actions to occur by the DS1280

PROTOCOL COMMANDS Table 1

1.) Burst read
2.) Burst write
3.) Read protocol select bits
4.) Write protocol select bits
5.) Burst read masking portions of the protocol select bits
6.) Read CRC register
7.) Set the address arbitration byte location
8.) Poll arbitration byte for status and control.

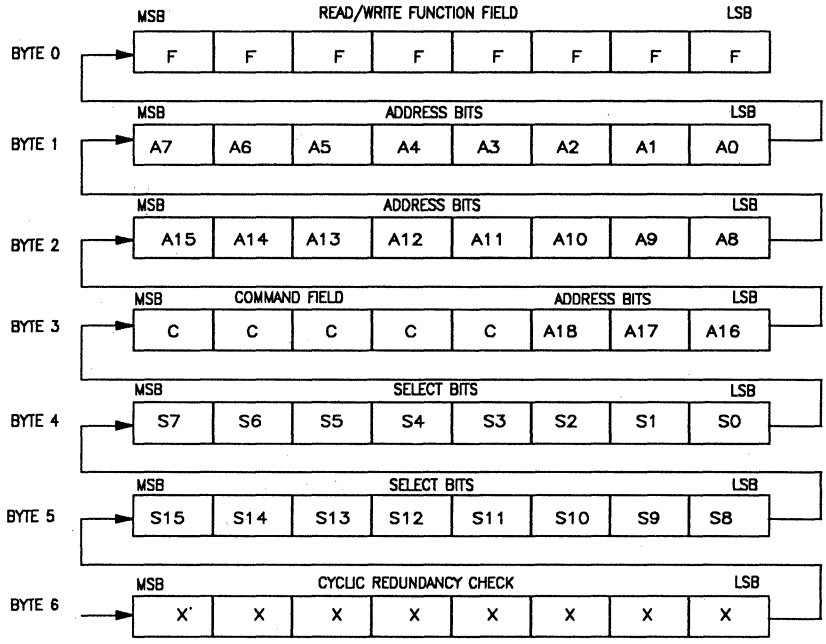
The organization of the 56 bit protocol is shown in Figure 2. As defined, the first byte of protocol determines whether the action which is to occur involves a read or write. A read function is defined by the binary pattern 11101000. This pattern, therefore, applies to commands 1, 3, 5, and 6 of Table 1. A write function is defined by the binary pattern 00010111. This pattern, therefore, applies to commands 2, 4, 7 and 8 of Table 1. Any other pattern which is entered into the read/write field will cause further action to terminate. Additional differentiation as to which read or write command is determined by the last five bits of the third byte of the protocol called the command field. The control field bits are defined in Table 2.

CONTROL FIELD Table 2

CCCCC	Command
00110	Burst read
10001	Burst write
00011	Read CRC register
10110	Set arbitration byte address to 00000 or 3FFFF
01001	Poll arbitration byte for access to RAM
00101	Read protocol select bits
01110	Write protocol select bits
11XXX	Burst read masking portions of the select bits.

A burst read uses a 19 bit address field which consists of the second, third, and bits 0, 1, and 2 of the fourth byte of the protocol to determine the starting address of information to be read from RAM. The byte of data resident in that location is loaded into an eight bit shift register within the DS1280. The byte of data is then transferred from the shift register to the 3 wire bus by driving the DQ line on the falling edge of the next eight clocks with the LSB first. A burst write uses the same 19 bit address field to determine the starting address of information to be written into RAM. Data is shifted from the DQ line of the 3 wire bus into an eight bit shift register within the DS1280 on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock. Burst reads and writes will continue on a byte by byte basis automatically incrementing the selected address by one location for each successive byte.
Termination of a current operation will occur at

PROTOCOL Figure 2

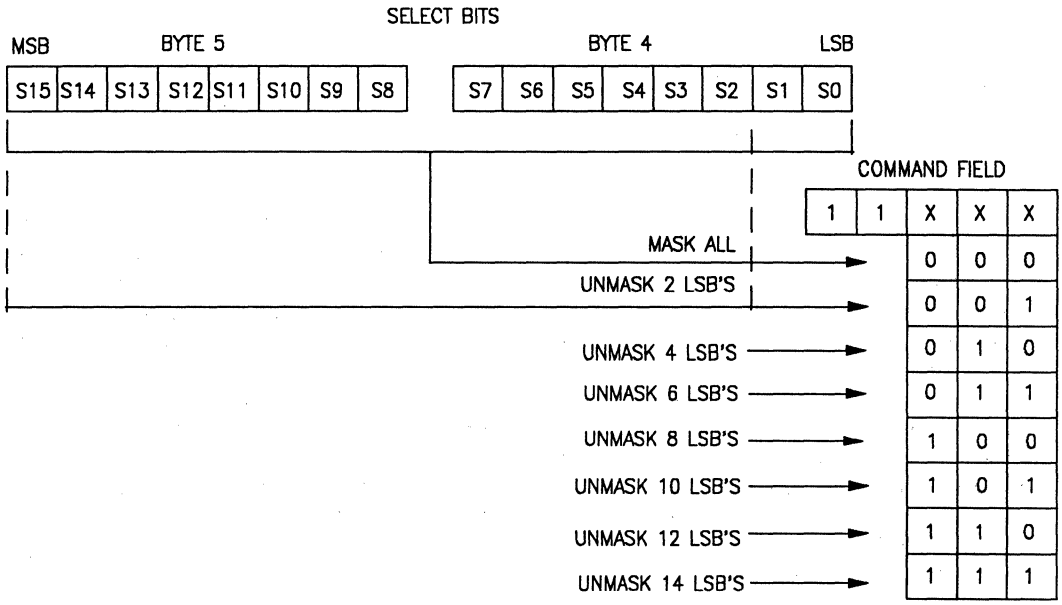


any time when $\overline{RST}$ is taken low. If a byte of data has been loaded into the shift register a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when $\overline{RST}$ goes low, no writing occurs. Reads can be terminated at any point since there is no potential for corruption of data. The read CRC command provides a method for checking the integrity of data sent over the 3 wire bus. The CRC byte resides in the last byte (Byte 6) of the protocol. The eight bit CRC byte not only operates on the protocol bits as they are written in, but also on all data that is written or read from RAM. After a burst read or write has finished and $\overline{RST}$ has gone low, the final value of the CRC is stored in the DS1280. If a read CRC register command is issued, the stored CRC value is driven onto the DQ line by the first eight clock cycles after the protocol is received. The CRC value generated by the DS1280 should match exactly with the value generated in the host system which is transmitting or receiving data on the other end of the 3 wire bus. If it does not, data has been corrupted and a retransmission should occur. It should be noted that the a CRC for previous transaction can only be obtained if a read CRC command is issued immediately after $\overline{RST}$ goes low to reset the DS1280, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever $\overline{RST}$ goes low again, destroying the CRC value of interest.

Generation of the CRC byte by the external unit on the 3 wire bus will be covered later in this text. In any two port system there is a potential for access collisions. To solve this problem, an arbitration byte is provided so that the serial and parallel ports of the DS1280 can determine the status of the other port. A special byte in RAM address space is reserved to allow for handshaking between the two ports. This arbitration byte has a special attribute in that it is simultaneously accessible by both ports. Two commands are used by the 3 wire serial port protocol to manage the arbitration byte. First, since this byte will create a hole in RAM address space for the parallel byte wide port, a command is added to move the arbitration byte to either address location "00000" or address location "3 FFFF." When setting the arbitration byte address location, the correct read/write field and command field must be entered along with all zeroes or all ones in the address field. It is important to note that the arbitration byte is located in the parallel memory location assigned by the serial port using the appropriate commands. However, the physical byte of RAM is located within the DS1280. The existence of this physical byte is transparent to the bytewide parallel port and looks like normal RAM space with some read/write restriction. However, the serial port can still address the actual RAM location at either 00000 or 3 FFFF in addition to accessing the arbitration byte. The second command used by the 3 wire serial port provides for polling of the arbitration byte to determine the status of the parallel port. In addition, the arbitration byte can be set to indicate to the parallel port that the serial port is taking over the RAM. The second command protocol allows the serial port to do a compressed read-write-read operation that causes the arbitration byte to be read by the first eight clocks following the protocol. The next eight clocks cause data to be written into the arbitration byte, and the last eight clock cycles allow for a second read of the data for verification. The 24 cycles occur by entering the 56 bit protocol only once. The protocol pattern entered is a write function in the read/write field (00010111), and the correct command field. Three other commands are used to set the select bits in the protocol. Once the select bits are set to a binary value they must be matched exactly when protocol is sent or further activity is prevented. The bits allow for 65,536 different binary combinations. Therefore, many DS1280 can be connected on the same serial bus and only the appropriate device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field.

To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have a large number of DS1280 in use and uniquely identify each. A read can occur successfully without knowing the select bits but a write cannot occur without matching the current select field. A third command masking specific select bits provides a means for determining the identity of specific DS1280 in the presence of many DS1280. A read in the read/write field and a "11000" in the command field will execute a mask read that ignores all select bits to determine the presence of any DS1280. With the detection of at least one device, a search can begin by masking all but a single pair of DS1280 select bits. A read in the read/write field and a "11001" in the command field will unmask the first two LSB's of byte 4 of the select bits (Figure 3). With these two select bits unmasked, only an exact match of four possible combinations (00, 01, 10, 11) of these two select bits will now allow access through the 3 wire port to RAM. Therefore, repeating the unmasking of the first two bits of the select field up to four times will give the binary value of these select bits. Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of four combinations can proceed as before. In fact, repetition of unmasking select bit pairs will

SELECT BITS MASK Figure 3



yield an exact match of 65,536 possible DS1280 in no more than 32 attempts.

Arbitration

As mentioned earlier, one byte of RAM has been reserved for arbitration between the 3 wire port and the bytewide parallel bus. The location of this byte within the memory map will be at address 00000 or at address 3 FFFF as determined by the protocol input from the 3 wire serial port. The arbitration byte has special restrictions and disciplines so that the 3 wire serial bus and the bytewide parallel bus are never in contention for RAM access. This byte is shown in Figure 4. As defined, the 3 wire serial port can read the whole byte but can only write S2- S0. The bytewide parallel port can read the whole byte but can only write B1-B0.

An internal counter controls C2-C0 that cannot be written by either port. Arbitration is accomplished when the status bits are read and written by the respective ports. If the 3 wire serial port wants to access RAM, the arbitration byte should be polled by the serial port until bit B1 equals zero. If B1 equals zero, the 3 wire serial port should then write a one into bit S2. After the write of bit S2, the 3 wire serial port should then read the arbitration byte to confirm that B1=0 and S2=1. This operation must be executed with the protocol for the compressed read-write-read sequence which minimizes overhead. The 3 wire serial port should always abort any attempt to access RAM if B1 equals one. When the 3 wire serial port completes any transfer of data to or from RAM, Bit S2 should be written back to zero so that the bytewide

ARBITRATION BYTE Figure 4

MSB LSB

P1	P0	S2	S1	S0	C2	C1	C0
PARALLEL BUS STATUS BITS	NOT USED	SERIAL PORT STATUS BITS	NOT USED	NOT USED	COUNT BIT	COUNT BIT	COUNT BIT

parallel port will know that the 3 wire serial port is not using the RAM. The bytewide serial bus can gain access to RAM by polling the arbitration byte until S2 bit equals zero. When S2 equals zero, the bytewide parallel port then writes a one into bit B1. A read cycle verifying that S2 equals zero and B1 equals one confirms that the bytewide parallel port has access to RAM. The bytewide parallel port can then read or write RAM as required. When the entire transaction is complete, the bytewide parallel port should write the B1 bit to zero, signalling the 3 wire serial port that the RAM is not in use. The bits B0, S1, and S0 can be defined by the user to pass additional arbitration information making possible more elaborate handshaking schemes between the two ports. Some typical uses for these bits could be an indication that a port desires access to RAM, or the amount of RAM written. Another method of arbitration between the 3 wire serial port and the bytewide parallel bus is the use of the count bits C0-C2. The 3 wire port reads or writes from RAM only once every eight clock cycles. This action occurs when the internal byte counter transitions from a "111" state to a "000" state. The access occurs regardless of the arbitration byte status bits. C0-C2 are updated as the internal serial bit counter is incremented. The bytewide port can execute reads or writes depending on the status of C0-C2. These bits indicate the number of bits the 3 wire serial port has loaded and, therefore, indicate when a read or write will occur from the 3 wire port. Since the 3 wire port always reads or writes at the ends of a byte (C0-C2 = 1) the bytewide parallel bus should never access RAM if the count bits read all ones. The bytewide parallel port can determine the minimum time left before the 3 wire serial port will access the memory from the count bits and the minimum clock cycle applied to the 3 wire clock input. Essentially the 3 wire serial port is given priority on access to RAM and the bytewide parallel port determines when it can access the RAM to avoid colliding with the 3 wire serial port.

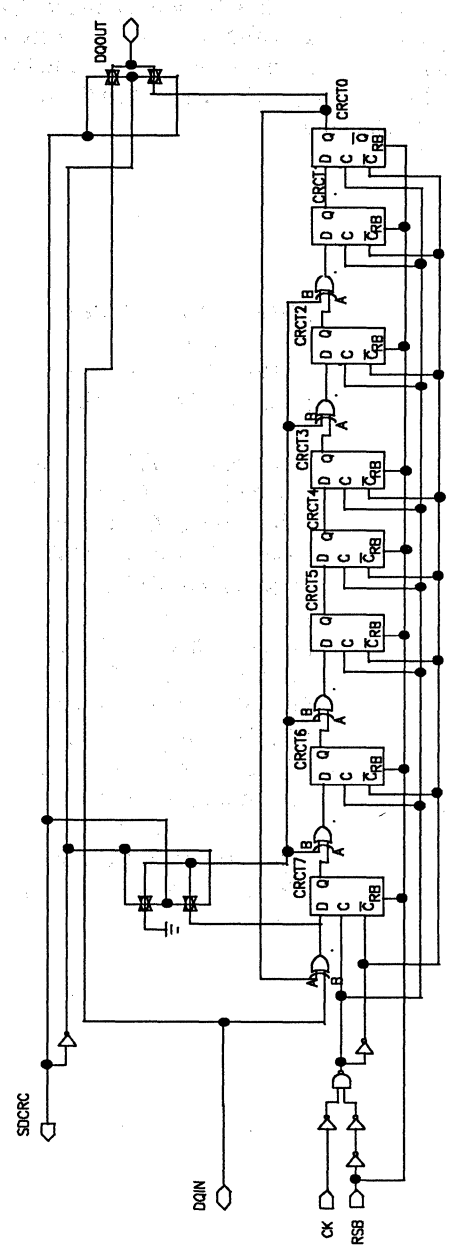
CRC Generation

The logic involved in CRC Generation is shown in Figure 5. Basically, the scheme is comprised of an eight bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQIN to the CRC Generator while each byte is being assembled and at the same time, output data to the output (DQ OUT). When input select CRC (SDCRC) is driven to an active level (high) data is output at DQOUT from the CRC Generator using the clock input (CK) in the same manner as described earlier for operation of the 3 wire serial bus. The reset signal (RSB) must be high while the CRC Generator is being used as an inactive state will disable the eight bit shift register. This signal is the same as the reset described for the 3 wire serial bus. A CRC Generator for serial port communications can be constructed as described above to satisfy the DS1280 CRC requirements. However, another approach is to generate the CRC using software.

An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Microcontroller. The assembly language procedure DO CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

```
DO_CRC:
        PUSH    ACC             ; Save the Accumulator
        PUSH    B               ; Save the B register
        PUSH    ACC             ; Save bits to be shifted
        MOV     B,      #8      ; Set to shift eight bits
CRC_LOOP:
        XRL     A,      CRC     ; Calculate DQIN xor CRCTO
        RRC     A               ; Move it to the last
        MOV     A,      CRC     ; Get the last CRC value
        JNC     ZERO            ; Skip if DQIN xor CRCTO = 0
        XRL     A,      0CCH    ; Update the CRC value
ZERO:
        RRC     A               ; Position the new CRC
        MOV     CRC,    A       : Store the new CRC
        POP     ACC             : Get the remaining bits
        RR      A               ; Position next bit in LSB
        PUSH    ACC             ; Save the remaining bits
        DJNZ    B,      CRC_LOOP ; Repeat for eight bits
        POP     ACC             ; Clean up the stack
        POP     B               ; Restore the B register
        POP     ACC             ; Restore the Accumulator
        RET                     ; Return
```

CRC GENERATION Figure 5



ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON ANY PIN RELATIVE TO GROUND-1.0V TO 7.0V
OPERATING TEMPERATURE- 0°C TO 70°C
STORAGE TEMPERATURE- 55°C TO+125°C
SOLDERING TEMPERATURE- 260°C FOR 10 SEC

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C OPERATING CONDITIONS

t_A=0°C TO 70°C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.0		V_{CC}+0.3 V	V	
Logic 0	V_{IL}	-0.3		+0.8	V	1

D.C. ELECTRICAL CHARACTERISTICS

(t_A=0°C TO 70°C V_{CC}=+5V+/-10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		+1	uA	9
Output Leakage	I_{LO}			1	uA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}	+2			mA	
Supply Current	I_{CC1}			15	mA	2
Supply Current	I_{CC2}			50	mA	3

CAPACITANCE

PARAMETER	SYMBOL	COND.	TYP.	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	tA=25°C	5	10	pF	
Output Capacitance	C_{OUT}	tA=25°C	7	15	pF	

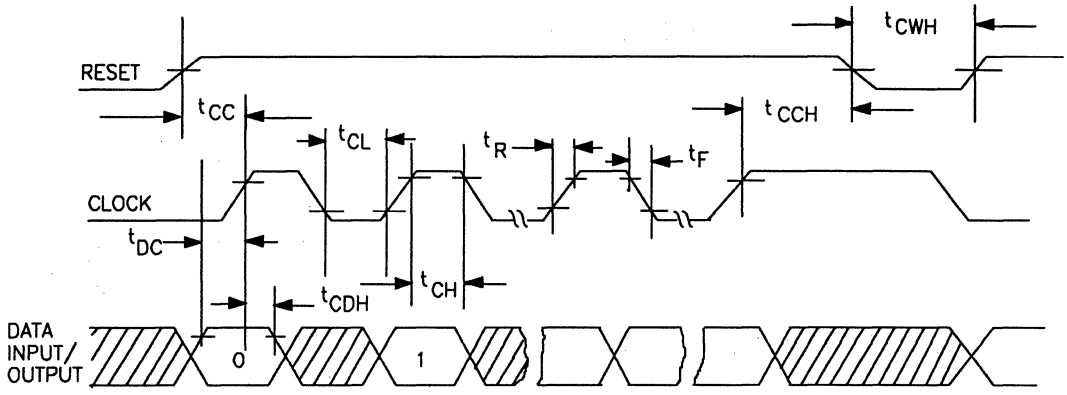
A.C. ELECTRICAL CHARACTERISTICS (V_{CC}=5V+/- 10%, 0°C TO 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	4
Data to CLK Hold	t_{CDH}	40			ns	4
Data to CLK Delay	t_{CDD}			125	ns	4,5,6
CLK Low Time	t_{CL}	500			ns	4
CLK High Time	t_{CH}	500			ns	4
CLK Frequency	f_{CLK}	D.C		1	MHz	4,10
CLK Rise & Fall Time	t_R t_F			100	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			us	4
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	4
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	4
$\overline{RST}$ to D/Q High Z	t_{CDZ}			50	ns	4
Serial Port Active	t_{DA}			25	ns	4,6
Serial Port Inactive	t_{DI}			25	ns	4,6
Parallel Port Propagation	t_{PD}		12	20	ns	4,6,8
Parallel Port Propagation	tPD		12	20	ns	4,6,8

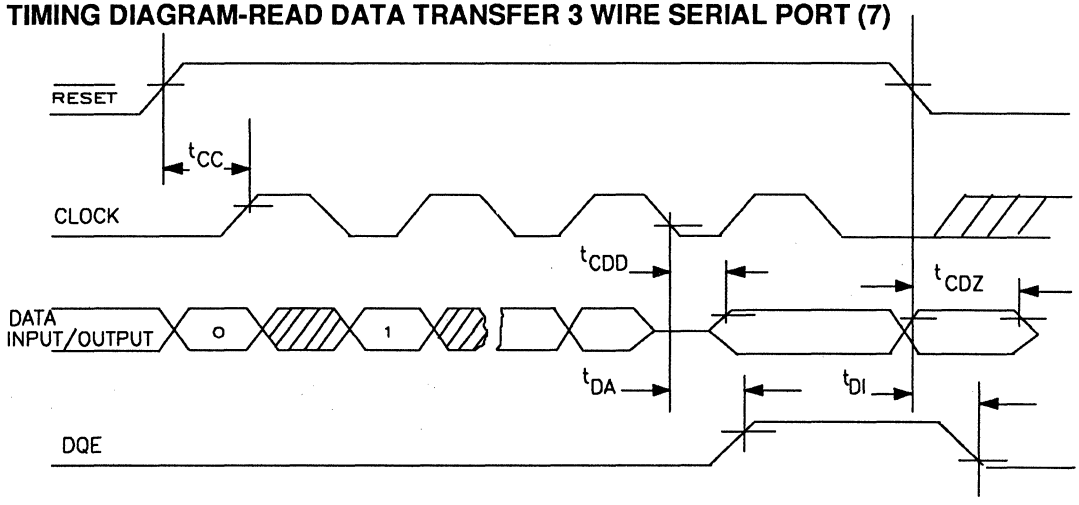
NOTES

1.) All voltages are referenced to ground.
2.) I_{CC1} is measured with all outputs open and both the 3 wire serial port or the bytewide parallel port inactive.
3.) I_{CC2} is measured with all outputs open.
4.) Measured at VIH = 2.0 V or VIL = 0.8 V and 10ns maximum rise and fall time.
5.) Measured at VOH= 2.4 V and VOL = 0.4V.
6.) Measured with a load capacitance of 50 Pf.
7.) The 3 wire serial port will correctly read and write any static RAM with an access time equal to or less than 200ns.
8.) Propagation delay is the same for data going either way on the bytewide parallel bus.
9.) Pins A0B thru A18B, $\overline{RST}$, DQ, $\overline{CEB}$ have pull down resistors which will leak approximately 50uA.
10.) Arbitration byte must be accessed at a maximum clock frequency of 500 KHz with a symetrical waveform.

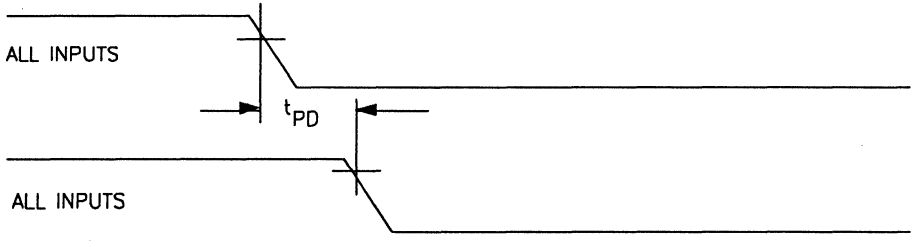
TIMING DIAGRAM-WRITE DATA TRANSFER 3 WIRE SERIAL PORT(7)



TIMING DIAGRAM-READ DATA TRANSFER 3 WIRE SERIAL PORT (7)

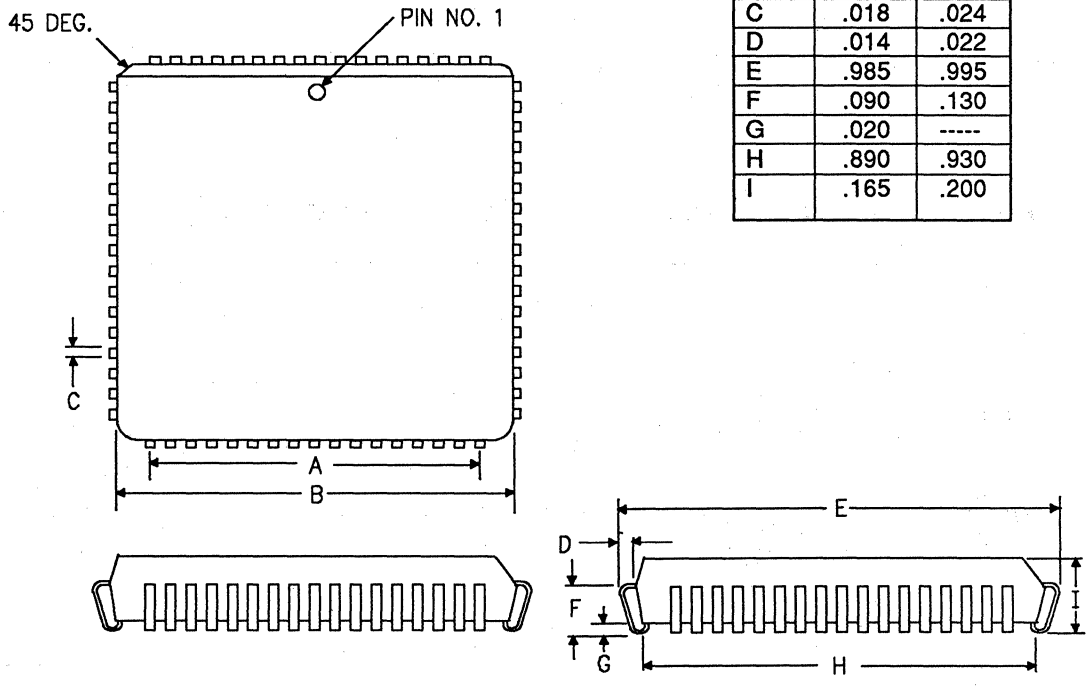


PROPAGATION DELAY-DATA TRANSFER-BYTEWIDE PARALLEL DATA BUS (8)

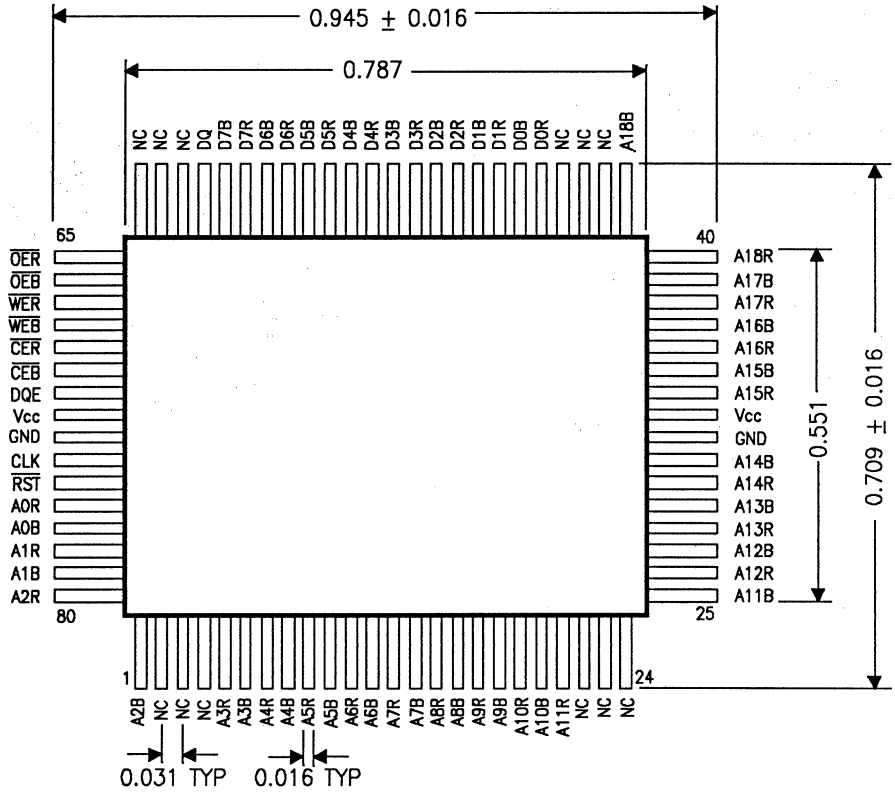


DS1280Q
BYTE WIDE TO SERIAL CONVERTER

DIM	INCHES	
	MIN.	MAX
A	.790	.810
B	.950	.958
C	.018	.024
D	.014	.022
E	.985	.995
F	.090	.130
G	.020	-----
H	.890	.930
I	.165	.200



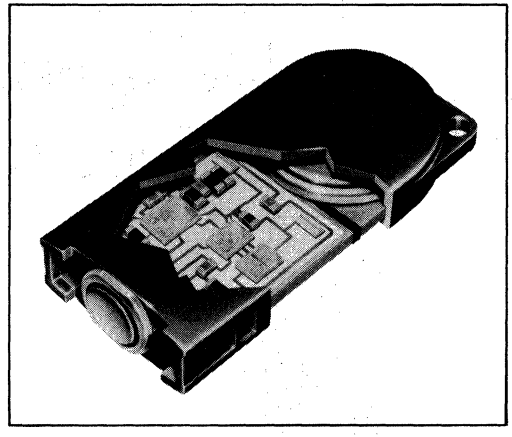
DS1280FP
BYTE WIDE TO SERIAL CONVERTER



Dallas Semiconductor
PROXIMITY KEY

ADVANCED INFORMATION
DS6065

FEATURES
- Connectorless portable read/write nonvolatile memory
- Wireless link has a range of over 5 feet.
- Contains 128 bits of secure read/write memory
- Compact size and shape
- Contains a lithium energy cell capable of 10 years of operation, and one million transactions
- Transmits and receives data directly from the DS6068 RF Communicator.
- Half duplex link uses 200 KHZ receive and 300 MHZ transmit.
- Single touch contact provided for RF link override
- Small enclosure for handling
- Supports individual device selection when multiple keys are within proximity



SIGNAL NAMES

Transmit	- 300 MHZ RF
Receive	- 200 KHZ Magnetic
RF Override	- 100 KHZ Touch Contact

DESCRIPTION
The DS6065 is a miniature transportable electronic memory with a self contained transmitter, receiver, and power supply, providing wireless data transfer between a host system and the key via a DS6068 RF Communicator. Wireless data transfer is accomplished via an RF Magnetic link. The PROXIMITY KEY receives data on a 200 KHZ frequency and transmits data back to the RF Communicator at 300 MHZ. Data communication at distances of over five feet is achieved with this half duplex link. A touch contact is provided which can override the RF link. This one contact port transfers data on a frequency of 100 KHZ. The DS6065 is designed for a life expectancy of over ten years. The small, light weight enclosure makes the device suitable for carrying in a pocket or for direct attachment to any mobile object.

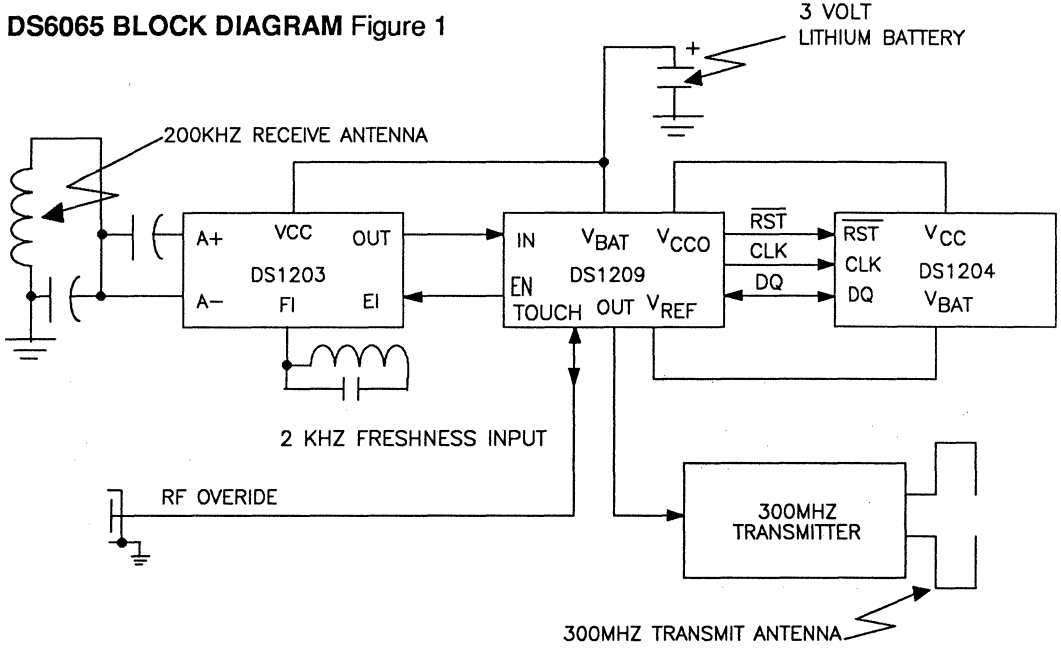
PROXIMITY KEY OVERVIEW

The DS6065 is designed to communicate over a half duplex RF/Magnetic link to a DS6068 RF Communicator. The main elements of the PROXIMITY KEY are shown in the block diagram of Figure 1. As shown, the DS6065 consists primarily of three Dallas Semiconductor chips; namely, the DS1203, the DS1209, and the DS1204. In order to understand the operation of the DS6065, a study of the data sheets of each of the three components is necessary. In addition, knowledge of the DS6068 RF Communicator and associated software is also helpful. The text which follows is only a summary of operation.

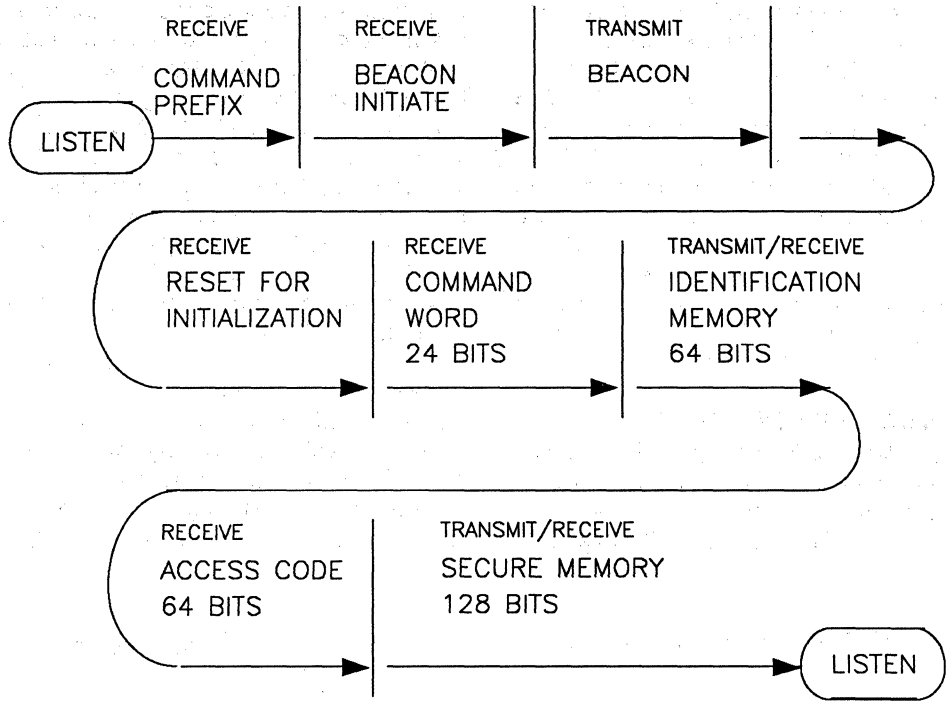
PROXIMITY KEY OPERATION

Magnetic field 200 KHZ pulse packets sent by the DS6068 are picked up by the 200 KHZ receive antenna and arrive at the comparator input terminals of the DS1203. If the freshness seal has been broken, the DS1203 will amplify the 200 KHZ signals from as low as 30 MV at the input to full level signals at the OUT pin (see the DS1203 data sheet for freshness seal operation). The amplified 200 KHZ signal is then sent to the DS1209 for processing and interpretation. Alternatively, the DS1209 accepts inputs via the RF override touch contact at 100 KHZ. The DS1209 is basically a state machine which determines what action is to be taken on the attached DS1204. The DS1204 receives signals from the DS1209 as CLK, $\overline{RST}$, and DQ. These signals either write data into or read data out of the DS1204. The DS1204, called the Electronic Key, is a specially partitioned memory which stores a 64 bit identification code and an access code which protects 128 bits of read/write nonvolatile memory. A typical transaction sequence is shown in Figure 2. When the DS6065 is receiving data to store in the DS1204, the DS1209 generates the CLK, RST

DS6065 BLOCK DIAGRAM Figure 1



TRANSACTION SEQUENCE Figure 2



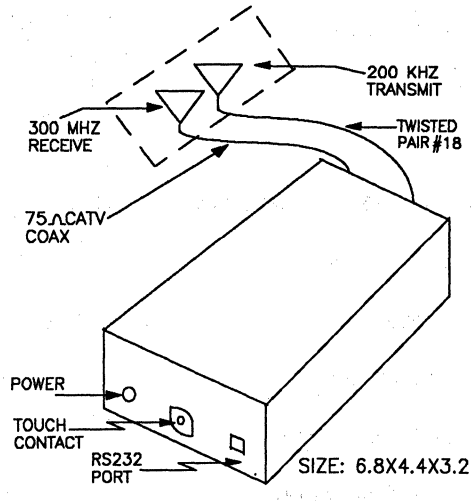
and data signals received from the DS1203. However, when the DS6065 is being read, data is transmitted back to the DS6068 RF Communicator via a 300 MHZ transmitter which is controlled by the DS1209. The digital data sequence transmitted is described in the DS1209 data sheet. The DS6065 is self powered by a lithium energy cell with over one million transactions. The unit is designed to operate for over ten years. The DS1209 and DS1203 control the energy consumption and power distribution within the PROXIMITY KEY.

PROXIMITY KEY SPECIFICATIONS

Communication-	bidirectional, half duplex
Range-	5 feet with DS6068 RF Communicator
Memory Capacity-	Command Prefix 24 Bits Read/Write Programmable Command Word 24 bits write only, Identification Memory 64 bits read/write, Access Code 64 bits write only, Secured Memory 128 bits read/write
Transaction Response Time-	<100 ms with DS6068 RF Communicator
Operating Time-	>10 years after freshness seal is disabled
Endurance-	>1 million transactions
Transmit Frequency-	300 MHZ +/- 15 MHZ RF
Transmit Modulation-	Binary Amplitude Shift Keying
Transmit Output Power-	<200 Micro Volt/Meter @ 3 Meters
Receiver Frequency-	200 KHZ +/- 5 KHZ Magnetic
Receiver Modulation-	Binary Amplitude Shift Keying
Storage Temperature-	-40° to 80° C
Operating Temperature-	-0 to 70° C

FEATURES

- Provides a wireless bidirectional 5 foot link to the Proximity Key or Tag
- Connects directly to a personal computer which can display and process data
- Communications to the base/control unit occur over a standard RS 232 Port
- 200 KHZ magnetic field transmitter and 300 MHZ RF receiver
- Software package provided which executes on IBM PC/XT/AT/PS2 and compatible computers
- Miniature 6 positon RJ11 connector is used for RS 232 interface
- Supplied with wall mounted 12 Volt D.C. UL approved power supply
- Touch contact provided for RF override
- 200 KHZ transmit antenna and 300 MHZ receive antenna supplied
- Contains a Real Time Clock for time and date stamping
- Durable moulded enclosure
- Full half duplex operation



RS232 PORT ~ RJ11 RECEPTACLE

Pin 1 - No Connection
Pin 2 - Transmit Data
Pin 3 - Ground
Pin 4 - Data Terminal Ready
Pin 5 - Receive Data
Pin 6 - No Connection

POWER CONNECTOR

Center Pin =+12 Volts Outer Connector - Ground

TOUCH CONTACT

Inner - 100 KHZ Data In/Data Out Outer - Ground

DESCRIPTION

The DS6068 is a magnetic field transmitter and an RF receiver which will directly interface to a host system, either a personal computer or terminal via a standard RS 232 Port. The RF Communicator is designed to work with the DS6065 Proximity Key or DS6066 Proximity Tag forming a wireless bidirectional RF link with a range of five feet. Its built-in microcontroller sends data to the proximity devices via the 200 KHZ magnetic field transmitter, or receives data from the 300 MHZ RF scanning superhetrodyne receiver. This half duplex link allows conversations to take place between the portable proximity devices and the fixed RF Communicator as people or objects pass within range. Because of the intelligence built into the RF Communicator in the form of the DS5000T Microcontroller, the DS6068 can pick out a single Proximity Key present out of many while managing the Digital to RF and RF to Digital conversion required by the target host system.

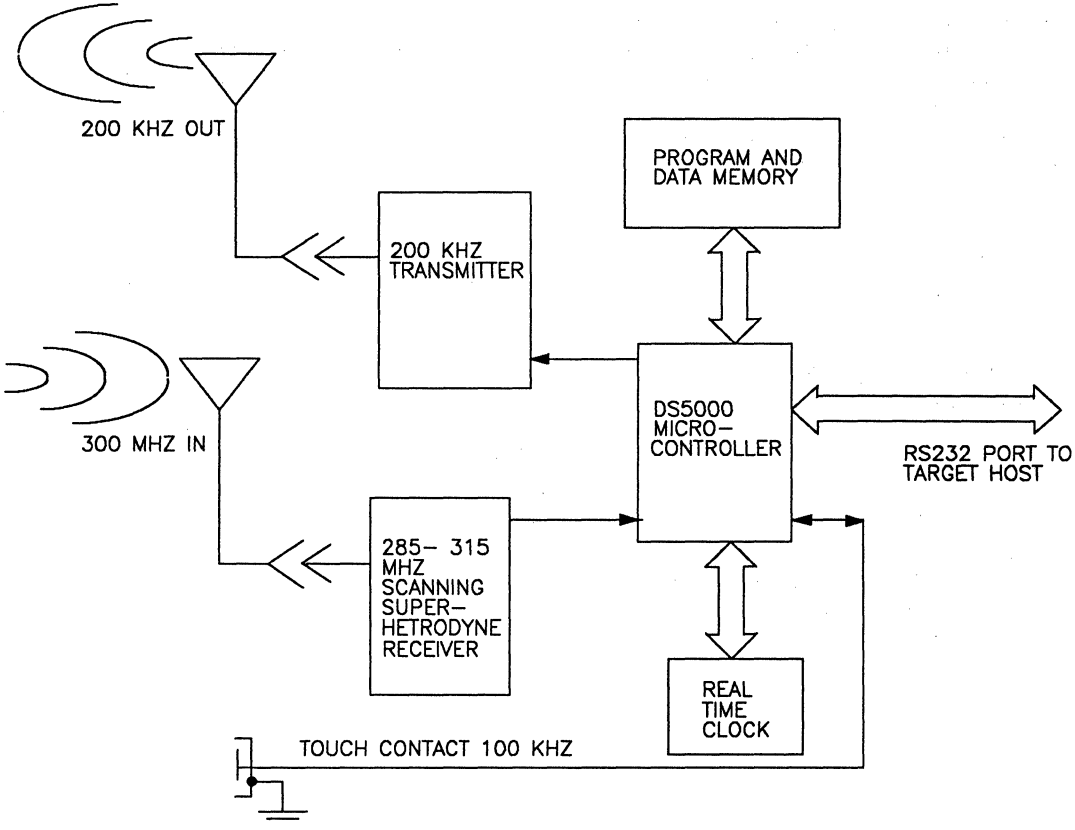
RF COMMUNICATOR OVERVIEW

The DS6068 is designed to communicate over a half duplex link to DS6065 Proximity Keys and DS6066 Tags using commands received from a host unit via an RS 232 Port. In order to understand the protocol and format of the RF/ Magnetic Link, a knowledge of the DS6065 Proximity Key is important. However, using the DS6068 RF Communicator is primarily a function of the software provided for execution on IBM PC and compatible computers. The manual provided with the software package should be studied carefully before attemtping to use the DS6068. The text which follows is only a summary of the RF Communicator.

RF COMMUNICATOR OPERATION

The block diagram shown in Figure 1 illustrates the main components within the DS6068. As shown, digital information received from the base unit is sent to the internal DS5000 Microcontroller via an RS 232 Serial Port. Digital information received by the DS5000 is then converted into signals which excite the 200 KHZ magnetic field transmitter. The 200 KHZ transmitter produces pulse packets of varying sizes. These pulse packets contain both command and data information which is interpreted by the DS6065 Proximity Key. Pulse packet sizes are 10, 20, 30, 40, and 50 pulses. (The definition and use of each type of pulse packet is described in

RF COMMUNICATOR BLOCK DIAGRAM Figure1



the literature written on the DS6065 Proximity Key and will not be covered in this text) When data is being sent to the DS6065, only the 200 KHZ transmitter is active. However, when data is to be retrived from the DS6065, both the 200 KHZ transmitter and the 300 MHZ receiver are used. The RF Communicator sends out commands on the 200 KHZ link and then listens for data being returned on the 300 MHZ Link. The data received is sent to the DS5000T where it is processed and stored in memory. A Real Time Clock is used to time and date stamp all data received. The target system can then retrieve the data at its convenience over the RS 232 Port. A touch contact one wire override is provided on the RF Communicator. This contact is used by placing a DS6065 touch contact surface directly against the touch contact surface of the DS6068. In this mode the DS5000T within the DS6068 communicates directly with the proximity devices, bypassing the RF Link. The pulse packets sent out the touch contact are exactly the same as those sent over the RF Link except that the frequency is at half the rate, 100 KHZ. Data is received from the DS6065 during the quiet after a read command is sent.

TRANSMIT/RECEIVE ANTENNA

Both the transmit and receive antenna reside in the same package. The 200 KHZ antenna is a wound resonant coil. The 300 MHZ antenna is similar to a half wave resonant dipole. The 200 KHZ antenna is attached to the RF Communicator via twisted pair wire which is connected to the terminal block on the back of the DS6068. The 300 MHZ antenna is attached to the RF Communicator via a CATV coaxial 75Ω cable and jack. The lengths of both cables allow the antenna to be mounted up to six feet away from the RF Communicator.

POWER SUPPLY

A wall mounted 120V AC 50/60 HZ to 5V DC power supply is included with each RF Communicator. The power supply is capable of supplying 5 amps continually and is UL approved.

SOFTWARE

The DS6065 is supplied with a software package which runs under all versions of MS-DOS. The manual supplied with the software package should be studied carefully before attempting to use the RF Communicator.

ENCLOSURE

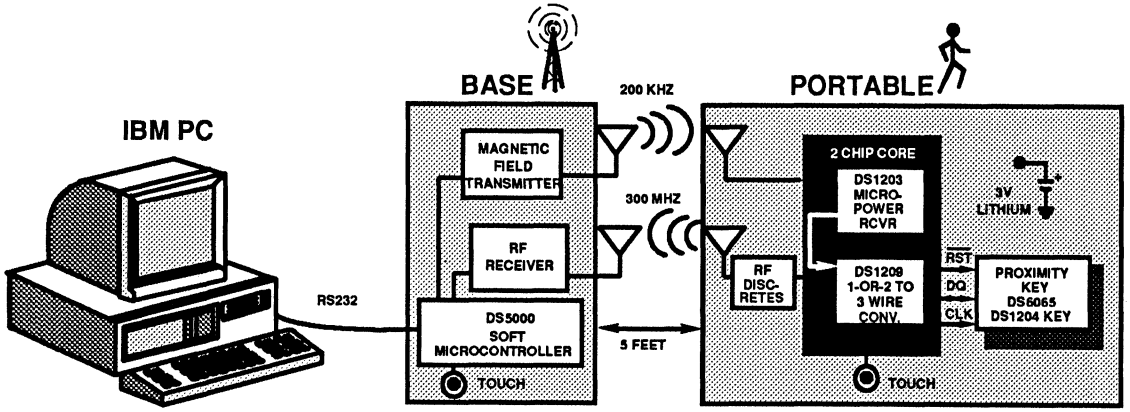
See DS9005 Eurocard Enclosure for dimensions and specifications(two enclosures are stacked).

RF COMMUNICATOR SPECIFICATIONS

Communication	- Bidirectional, Half Duplex
Range	- 5 Feet with DS6065 Proximity Key, DS6066 Proximity Tag
Memory Capacity	- 32 K Bytes with RealTime Clock
Receiver Frequency	- 300 MHZ +/- 15 MHZ
Transmitter Frequency	- 200 KHZ+/- 5 KHZ Magnetic
Transmitter Modulation	- Binary Amplitude Shift Keying
Transmitter Radiated Power	< 463 Millivolts/M @ 10 Meters
Storage Temperature	- -40°C to 80°C
Operating Temperature	- 0°C to +70°C

Dallas Semiconductor
WIRELESS STARTER KIT

FOR EXPERIMENTAL PURPOSES
DS6068K



INCLUDES

- Three DS6065 Proximity Keys with 5 foot range
- DS6068 RF Communicator for two-way information exchange
- RS232 connection cable and 200 KHz/300 MHz Antenna and power supply
- Software for IBM PC compatible computers
- Data sheets, documentation

DESCRIPTION

The DS6068K Wireless Starter Kit provides the basic components needed for rapid evaluation of proximity device performance: three DS6065 Proximity Keys, DS6068 RF Communicator, RS232 cable, application software for IBM PC compatible computers, documentation and data sheets. The Starter Kit can display the contents of the proximity device on a personal computer screen, in so doing, demonstrates that the computer can exchange information with the proximity device over the air waves at a distance up to 5 feet.

INSTRUCTIONS

Insert the software disk into your IBM or compatible computer and type "READ ME." This command enables printing of document files which should be read carefully before proceeding.
Note: Not approved for end use until FCC certificate of compliance can be obtained. Under Dallas Semiconductor's marketing license, authorization for use limited to one year after purchase.

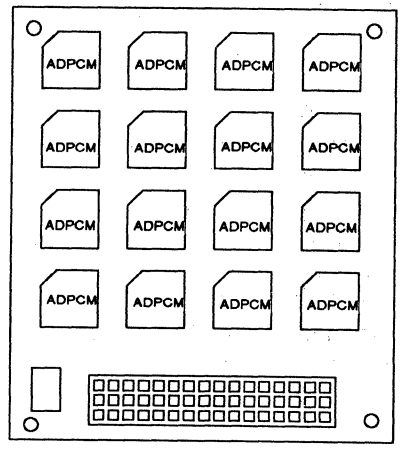
Telecommunications

Dallas Semiconductor
ADPCM ARRAY

PRELIMINARY
DS2157/DS2158
Available January 1989

FEATURES

- High-density, multi-channel speech compression system provides full duplex channels on a 3 x 3 inch board.
- Based on high-performance DS2167/68 ADPCM processors. DS2157 uses the DS2167 and supports the July 1986 T1Y1 recommended algorithm. DS2158 supports the "old" CCITT G.721 algorithm.
- Flexible data bussing scheme to accomodate user's backplane data format and rate.
- Microcontroller-compatible port for system configuration. On-board power monitor provides system reset.



DESCRIPTION

The DS2157 and DS2158 ADPCM Arrays use surface-mount technology and the DS2167/68 ADPCM processors to yield 12 or 24 full-duplex channels in nine square inches. The DS2157 array features the DS2167Q processor which implements the July 1986 T1Y1 recommended ADPCM algorithm. The DS2158 array features the DS2168Q processor which implements the "old" CCITT G.721 algorithm. The PCM data interfaces are organized into four independent busses which may be configured to best suit the data format on the user's system backplane. The array also includes input signal buffering and a power-monitor reset circuit.

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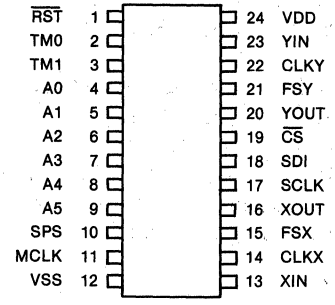
Dallas Semiconductor
ADPCM Processor

DS2167
DS2168

FEATURES

- Speech compression chip compatible with standard ADPCM algorithms:
  - DS2167 supports "new" T1Y1 recommendations (July 1986) and "new" CCITT G.721 recommendations
  - DS2168 supports "old" CCITT G.721 recommendations
- Dual independent channel architecture—device may be programmed to perform full duplex , 2-channel expansions, or 2-channel compressions
- Interconnects directly with *u*-law or A-law combo-codec devices
- Serial PCM and control port interfaces minimize "glue logic" in multiple channel applications
  - On-chip channel counters identify input and output timeslots in TDM-based systems
  - Unique addressing scheme simplifies device control; 3-wire port shared among 64 devices
  - Bypass and idle features allow dynamic allocation of channel bandwidth, minimize system power requirements
- Hardware mode intended for stand-alone use
  - No host processor required
  - Ideal for voice mail applications
- 28-pin surface-mount package available, designated DS2167Q/ DS2168Q

PIN CONNECTIONS



DESCRIPTION

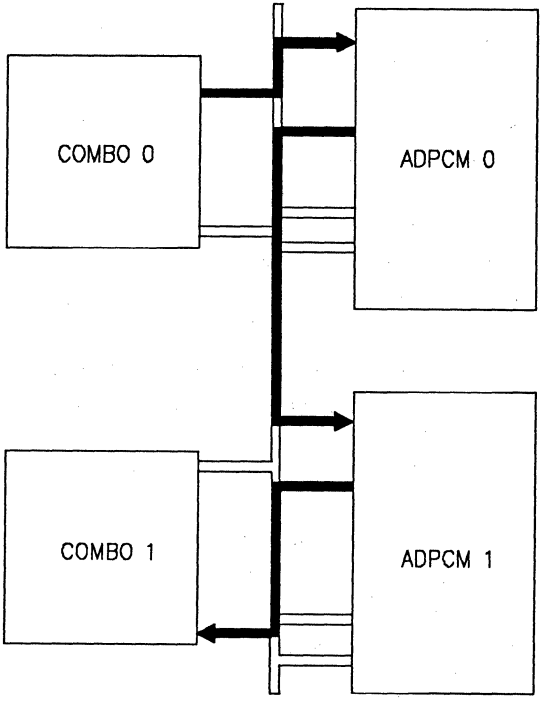
The DS2167 and DS2168 are dedicated digital signal processor (DSP) CMOS chips optimized for Adaptive Differential Pulse Code Modulation (ADPCM) based speech compression algorithms. The devices halve the transmission bandwidth of "toll quality" voice from 64K to 32K bits/second and are utilized in PCM-based telephony networks.

Dallas Semiconductor
ADPCM DESIGN KIT

DS2167K

FEATURES

- Emulates multi-channel applications such as T1 transcoders
- Expedites new designs by eliminating first-pass device prototyping
- Interfaces directly to IBM PC, XT, AT and compatibles
- High-level, graphic software demonstrates chip flexibility and feature set
- Kit components include:
  - DS2167 ADPCM processors (2)
  - Codec-combo devices (2)
  - Timeslot assigner circuit (TSAC) for combos
  - Support logic and clock generation circuitry
  - Printed circuit board
  - Interface cable for PC
  - Documentation and control software diskette



DESCRIPTION

The ADPCM design kit provides everything a user needs to evaluate the DS2167 (DS2167K) ADPCM processors in an actual system environment. The evaluation board connects directly to transmission test sets for performance monitoring of compressed or expanded channels. The board requires ±5 volts. A system control interface connects directly to the PC parallel printer port.

The kit's control software turns the PC into a powerful system controller. The program gives the user full control of system configuration, including timeslot placement, operating modes (comprossion, expansion, bypass or idle), data formats and algorithm reset. The controller program runs under MSDOS or IBM DOS version 2.0 or later. Color monitors are supported but not required.

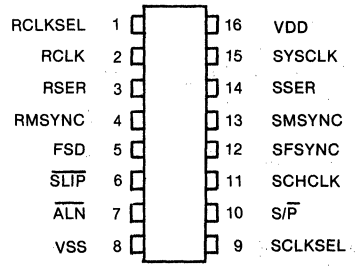
Dallas Semiconductor
T1/CEPT Elastic Store

DS2175

FEATURES

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop-timed and system-timed data streams on frame boundaries
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- Comprehensive on-chip "slip" control logic
  - Slips occur only on frame boundaries
  - Outputs report slip occurrences and direction
  - Align feature allows buffer to be recentered at any time
  - Buffer depth easily monitored
- Compatible with DS2180A DS2181 CEPT Transceivers
- Industrial temperature range of −40° to +85°C available, designated DS2175IND

PIN CONNECTIONS



DESCRIPTION

The DS2175 is a low-power CMOS elastic-store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1—1.544 MHz) and European (CEPT—2.048 MHz) rate networks. The chip has several flexible operating modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

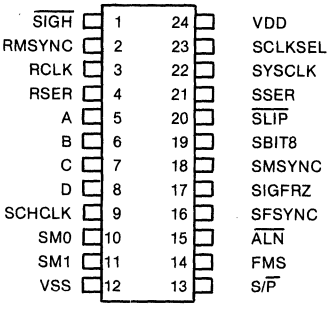
Dallas Semiconductor
T1 Receive Buffer

DS2176

FEATURES

- Synchronizes loop-timed and system-timed T1 data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip-compensated output indicates when signalling updates occur
- Compatible with DS2180A T1 Transceiver
- Surface mount package available, designated DS2176Q
- Industrial temperature range of −40°C to +85°C available, designated DS2176IND

PIN CONNECTIONS



DESCRIPTION

The DS2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24-lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

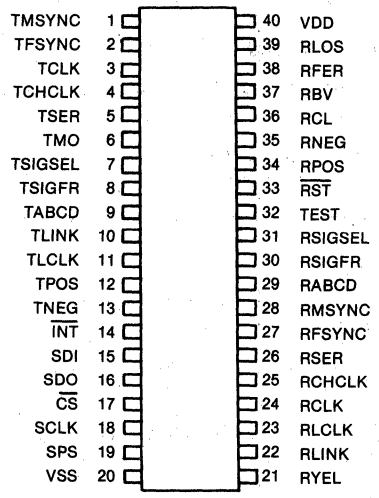
Dallas Semiconductor
T1 Transceiver

DS2180A

FEATURES

- Single chip DS1 rate transceiver
- Supports common framing standards
  - 12 frames/superframe "193S"
  - 24 frames/superframe "193E"
- Three zero suppression modes
  - B7 stuffing
  - B8ZS
  - Transparent
- Simple serial interface used for configuration, control and status monitoring in "processor" mode
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- 5V supply, low power CMOS technology
- Surface mount package available, designated DS2180AQ
- Industrial temperature range of −40 °C to +85 °C available, designated DS2180AN or DS2180AQN

PIN CONNECTIONS



DESCRIPTION

The DS2180A is a monolithic CMOS device designed to implement primary rate (1.544 MHz) T-carrier transmission systems. The 193S framing mode is intended to support existing Ft/Fs applications (12 frames/superframe). The 193E framing mode supports the extended superframe format (24 frames/superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

Several functional blocks exist in the transceiver. The transmit framer/formatter generates appropriate framing bits, inserts robbed bit signaling, supervises zero suppression, generates alarms, and provides output clocks useful for data conditioning and decoding.

Dallas Semiconductor
T1/CEPT Design Kit

PRELIMINARY
DS2180DK/DS2181DK
Available Spring 1989

FEATURES

- Demonstrates entire T1 and CEPT chip family
- Expedites new designs by eliminating first-pass prototyping
- Interfaces directly to IBM PC, XT, AT and compatibles through the parallel printer port
- High-level graphic software controls and monitors board functions
- Kit includes:
  - DS2180A or DS2181
  - DS2186
  - DS2187
  - DS2176
  - DS2175
  - Transmit and receive transformers
  - T1 (1.544 MHz) and CEPT (2.048 MHz) clocks and frame syncs
  - PC board with all necessary support logic
  - Documentation and control software diskette
- Transceiver works in the "software" mode
- Wire-wrap area and easy accessable test points allow customization to meet user's need
- Board comes completely assembled

DESCRIPTION

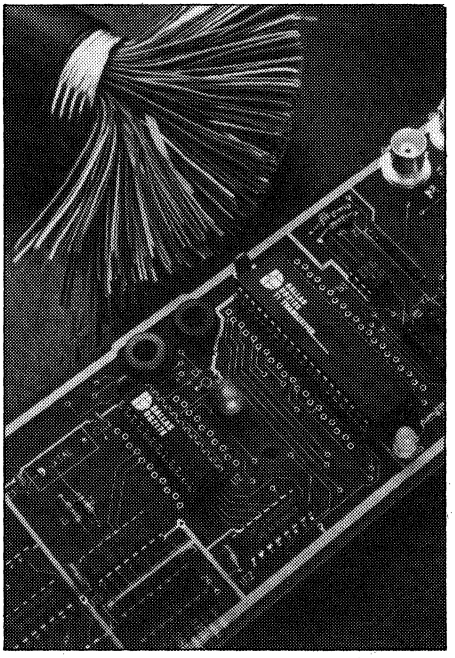
The DS2180DK and DS2181DK allow the user to evaluate the entire T1 or CEPT line card chip set. The design kits can be connected either to transmission test equipment or directly to T1 or CEPT lines. Received data can be run to a simulated backplane or can be looped back directly. The design kits operate off a single +5V supply. The controller program runs under MSDOS or IBM DOS version 2.0 or later.

Dallas Semiconductor
T1 Design Kit

DS2180K

FEATURES

- Demonstrates key "hardware mode" attributes of the DS2180/DS2176 pair, such as:
  - Framing/synchronization
  - Link supervision and control
  - Signaling supervision
  - Rate adaption to equipment backplanes
- Expedites new designs by eliminating first-pass device prototyping
- Easily interfaced to user host controller for "software mode" evaluation
- User-supplied line interface allows direct connection to T1 lines
- Kit components include:
  - DS2180 T1 Transceiver
  - DS2176 T1 Receive Buffer
  - Printed circuit board
  - Support logic and clock generation circuitry
  - Applications and assembly information



DESCRIPTION

The DS2180K allows the user to evaluate the performance of the DS2180 T1 Transceiver and DS2176 T1 Receive Buffer in an actual system environment. The evaluation board requires +5 volts; board inputs and outputs are TTL-compatible. Test points and control options on the board simplify selection of device feature sets required by the system designer.

Kit assembly requires approximately 1 hour. Although designed for hardware mode operation, a small wire-wrap area is provided for user-supplied host processor interface.

See Application Note 11 for further information.

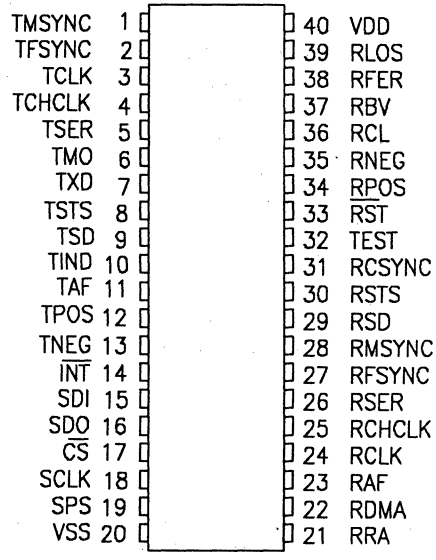
Dallas Semiconductor
CEPT PRIMARY RATE TRANSCEIVER

PRELIMINARY
DS2181

FEATURES

- Single chip primary rate transceiver meets CCITT standards: G.704 and G.732
- Supports new CRC4 based framing standards and CAS and CCS signalling standards
- Simple serial interface used for device configuration and control in "processor" mode
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Comprehensive on-chip alarm generation, alarm detection and error logging logic
- Shares footprint with DS2180A T1 Transceiver
- Companion to DS2175 Transmit/Receive Elastic Store
- 5V supply, low power CMOS technology

PIN CONNECTIONS



DESCRIPTION

The DS2181 is designed for use in CEPT networks and supports all logical requirements of CCITT Red Book Recommendations G.704 and G.732. The transmit side generates framing patterns and CRC4 codes, formats outgoing channel and signalling data and produces network alarm codes when enabled. The receive side decodes the incoming data and establishes frame, CAS multiframe, and CRC4 multiframe alignments. Once synchronized, the device extracts channel, signalling and alarm data.

A serial port allows access to 14 on-chip control and status registers in the processor mode. In this mode, a host processor controls such features such as error logging, per-channel code manipulation and alteration of the receive synchronizer algorithm.

The hardware mode is intended for preliminary system prototyping and/or retrofitting into existing systems. This mode requires no host processor and disables special features available in the processor mode.

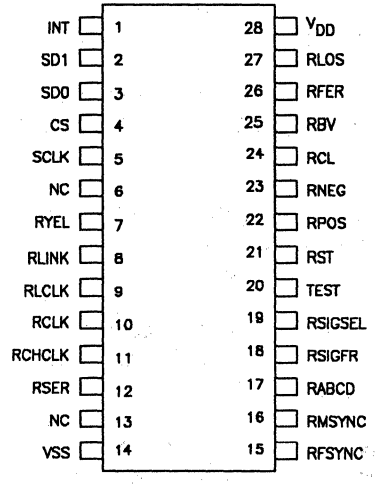
Dallas Semiconductor
T1 Line Monitor

PRODUCT PREVIEW
DS2182
Available Spring 1989

FEATURES

- Performs framing and monitoring functions
- Supports Superframe and Extended Superframe
- Designed to fulfill the requirements outline in TA-147 (DS1 Rate Digital Service Monitoring Unit) and TR-194 (ESF Interface Specification)
- Four on-board error counters
  - -16 bit bipolar violation
  - 8 bit CRC
  - 8 bit OOF
  - 8 bit frame bit error
- Indication of the following
  - yellow and blue alarms
  - incoming B8ZS code words
  - change of frame alignment
  - loss of sync
  - carrier loss
- Simple serial interface used for configuration, control and status monitoring
- Burst mode allow quick access to countes for status update
- Auto counterreset feature
- Single 5V supply, low power CMOS technology
- Available in 28-pin DIP and 28-pin PLCC

PIN CONNECTIONS



DESCRIPTION

The DS1282 is a monolithic CMOS device designed to perform real time performance monitoring on T1 lines. The DS1282 will frame to the data on the line and count errors and supply detailed information about the status and condition of the line. Large on-board counters allow the accumulation of errors for extended periods which permits a single CPU to monitor or a number of T1 lines. Output clocks that are synchronized to the incoming data stream are provided for easy extraction of S-Bits, FDL bits, signaling bits and channel data.

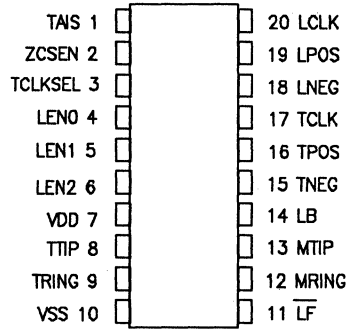
Dallas Semiconductor
Transmit Line Interface

PRELIMINARY
DS2186
Available Spring 1989

FEATURES

- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- On-chip Transmit LBO (line build-out) and line drivers eliminate external components
- Programmable output pulse shape supports short and long loop applications
- Supports bipolar and unipolar input data formats
- Transparent, B8ZS and HDB3 zero code suppression modes
- Compatible with DS2180A T1 and DS2181 CEPT Transceivers
- Companion to the DS2187 Receive Line Interface
- Single 5V supply, low power CMOS technology

PIN CONNECTIONS



DESCRIPTION

The DS2186 interfaces user equipment to North American (T1-1.544 MHz) and European (CEPT-2.048 MHz) primary rate communications networks. The device is compatible with all types of twisted pair and coax cable found in such networks.

Key on-chip components include: programmable waveshaping circuitry, line drivers, remote loopback and zero suppression logic. A line-coupling transformer is the only external component required.

Short loop (DSX-1, 0 to 655 feet) and long loop (CSU; 0 db, -7.5 db and -15 db) pulse templates found in T1 applications are supported. Appropriate CCITT Red Book recommendations are met in the CEPT mode.

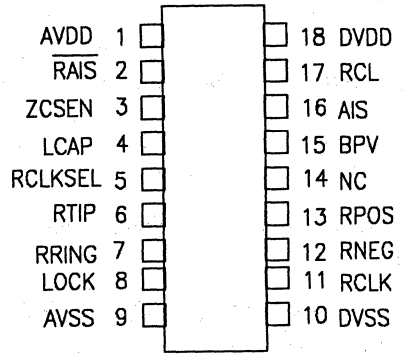
Application areas include DACS, CSU, CPE, channel banks and PABX to computer interfaces such as DMI and CPI. Supports ISDN-PRI (primary rate interface) specifications.

Dallas Semiconductor
RECEIVE LINE INTERFACE

PRELIMINARY
DS2187
Available Spring 1989

FEATURES
- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- Extracts clock and data from twisted pair or coax
- Meets requirements of PUB 43801, PUB 62411 and applicable CCITT G.823
- Precision on-chip PLL eliminates external crystal or LC tank - no tuning required
- Decodes AMI, B8ZS and HDB3 coded signals
- Designed for short loop applications such as terminal equipment to DSX-1
- Reports alarm and error events
- Compatible with the DS2180A T1 and DS2181 CEPT Transceivers
- Companion to the DS2186 Transmit Line Interface
- Single 5V supply, low power CMOS technology

PIN CONNECTIONS



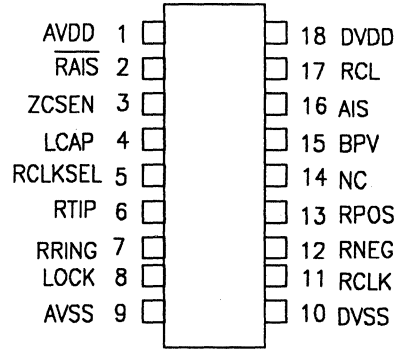
DESCRIPTION
The DS2187 interfaces user equipment to North American (T1 - 1.544 MHz) and European (CEPT 2.048 MHz) primary rate communication networks. The device extracts clock and data from twisted pair or coax transmission media and eliminates expensive discrete components and/or manual tuning required in existing T1 and CEPT line termination electronics.

Application areas include DACS, CSU, CPE, channel banks and PABX to computer interfaces such as DMI and CPI.

FEATURES

- Line interface for T1 (1.544 MHz) primary rate networks
- Extracts clock and data from twisted pair or coax
- Meets requirements of PUB 43801 and PUB 62411
- Precision on-chip PLL eliminates external crystal or LC tank - no tuning required
- Decodes AMI and B8ZS coded signals
- Designed for short loop applications such as terminal equipment to DSX-1
- Reports alarm and error events
- Compatible with the DS2180A T1 Transceiver
- Companion to the DS2186 Transmit Line Interface
- Single 5V supply, low power CMOS technology

PIN CONNECTIONS



DESCRIPTION

The DS2187-T1 performs exactly like the DS2187 with two exceptions. First, it should only be used in T1 applications which implies that the RCLKSEL pin (pin #5) should be tied low. Secondly, to avoid false lock during power-up, the receive signal must not be a repetitive pattern with more than four consecutive zeros. For example, a 1000001000001...pattern is not acceptable. This restriction only applies at initial power-up. Once the device has correctly locked after power-up, it will never, under any conditions, false lock again. Besides these two exceptions, all other specifications and details outlined in the DS2187 data sheet are valid for the DS2187-T1.

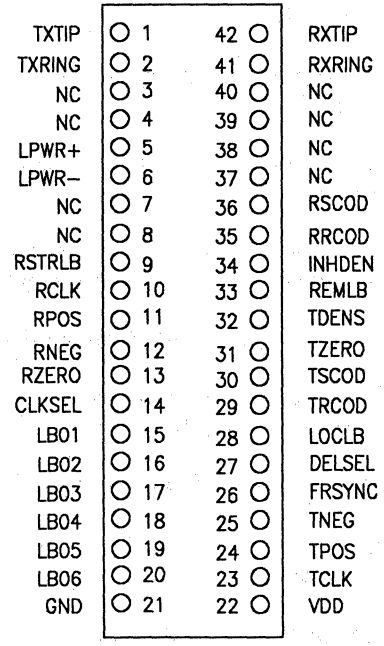
Dallas Semiconductor
T1 NETWORK INTERFACE UNIT (NIU)

PRELIMINARY
DS2190
Available Summer 1989

FEATURES

- Modularized network interface for 1.544 Mbps T1 services
- "Network side" connects directly to T1 line
- Compatible with DS2180A transceiver
- Small size - approximately six square inches permits integration onto line cards
- Compatible with ATT publication 62411
- FCC Part 68 and Part 15 pre-registration
- Extracts clock and data with no external components or tuning
- Detects and generates in-band loopback codes
- Assures proper ones density to network
- Powered by a local +5 volt supply

PIN CONNECTIONS



DESCRIPTION

The DS2190 is a small sealed module designed to meet the recommendations of ATT publication 62411 for interfacing to T1 1.544 Mpbs services (such as Accunet* T1.5, Skynet* T1.5 and High Capacity Digital Service). Because of the DS2190's FCC approval (Parts 68/15) and small footprint, T1 equipment makers can integrate an NIU into their products, reducing cost and increasing total system performance. Basic functions of the DS2190 are: clock and data recovery, isolation and surge protection, loopback detection and generation, and keep-alive signal generation. The DS2190 is compatible with D4 and ESF framing formats as well as B8ZS Clear Channel Coding. Also provided are alarm outputs for transmit and receive line status monitoring.

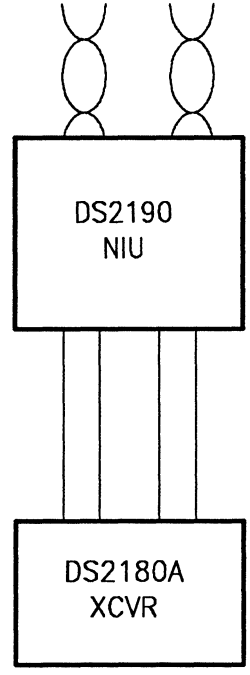
*Service marks of AT&T Communications

Dallas Semiconductor
T1 NETWORK INTERFACE UNIT DESIGN EVALUATION KIT

PRELIMINARY
DS2190DK

FEATURES

- Self-contained system for performance evaluation of the DS2190 Network Interface Unit
- Pre-assembled kit includes DS2190 NIU, DS2180A transceiver, transmit clock and data generator
- Connects directly to test equipment, including T1 frame generator, line simulator, jitter generator and analyzer
- Supports ESF and D4 framing, B8ZS and B7 stuffing
- On-board switches access all NIU mode options; LED indicators for system status, including synchronization loss and CRC errors; test points for additional critical signals
- Prototyping area for user customization
- Powered by single +5V supply



DESCRIPTION

The DS290DK contains all of the interface and framing functions required to connect to a simulated T1 communications line. The board is organized for easy control over and monitoring of the DS2190 operation. It is a helpful tool for evaluating the DS2190 in-system performance.

Additional circuitry may be easily added in the prototyping area to emulate the user's end application. An additional area contains a computer interface so that the DS2180A serial port may be accessed with user-developed software.

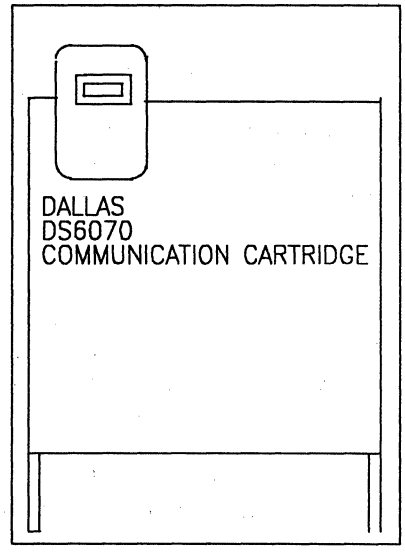
Modems

Dallas Semiconductor
TeleMicro™ Cartridge

PRELIMINARY
DS6070

FEATURES
- Supports teleservicing in new designs or existing systems
- Complete application software changes via a telephone line
- Combines the functions of the DS5000T Time Microcontroller™ with a 1200 bps or 2400 bps modem
- 32K bytes of nonvolatile SRAM for program and/or data
- Downloads/verifies Intel Hex absolute object files
- All DS5000T I/O facilities available to the user
- Connects to 40-pin DS5000T/8051 footprint via ribbon cable
- Integral modem subsystem executes "AT" commands
- Bell 212A/103 compatible
- DTMF and pulse dialing
- Call progress monitoring
- FCC Part 68 and Canadian CS-03 approved DAA
- Provides standard RJ11 connector to telephone line
- Requires no support circuit overhead on target system
- User selectable interrupt for 8250 UART
- +5V only operation

PACKAGE OUTLINE



ORDERING INFORMATION

DS6070 - 12	TeleMicro Cartridge with 1200 bps modem
DS6070 - 24	TeleMicro Cartridge 2400 bps modem

DESCRIPTION
The DS6070 TeleMicro Cartridge is designed to bring instant teleservice capability to systems which are based on the DS5000T Time Microcontroller. Teleservice refers to the ability to perform remote software upgrades and system diagnostics from a desktop computer over a telephone line. The major benefit to the end user is reduced operating costs by eliminating service calls to repair or upgrade equipment in the field.

The integral part of the DS6070 TeleMicro Cartridge is the DS5000T itself. Unlike rigid ROM or EPROM based microcontrollers, all of the Time

Microcontroller's memory is high performance, read/write, and nonvolatile for more than 10 years. The DS5000T is equipped with 32K bytes of nonvolatile SRAM which can be dynamically partitioned to fit program and data storage requirements of a particular task. A major benefit resulting from its nonvolatility is that the Time Microcontroller allows Program Memory to be changed at any time, even after the device has been installed in the end system. Additionally, the size of the Program and Data Memory areas in the embedded RAM is variable and can be set either when the application software is initially loaded or by the software itself during execution. Incorporated within the DS5000T is a permanently powered clock/calendar function which may be used for time stanping and scheduling of events. The DS5000T is instruction set and pin compatible with the industry standard 8051.

The DS6070 TeleMicro Cartridge exploits this capability of the DS5000 with the addition of a complete modem subsystem which resides on the Embedded Address/Data bus of the DS5000. The subsystem accepts the "AT" command set issued from the DS5000 user's software for maximum customer familiarity during software development. The internal circuitry includes a Part 68 registered DAA function, eliminating potential delays for customers with a need to incorporate a modem function in their end system product. The DS5000 is interfaced to the modem subsystem via its Embedded Address/Data bus, so that all of its 40 pins are available for use in the target application.

The DS6070 is housed in a rugged and durable package which is compact enough to fit into a wide variety of applications. Two connectors are provided on the cartridge. The first is a RJ45 female connector which interfaces directly to the telephone line terminated with a standard modular RJ11 male connector. The second is a 40-pin edge connector which brings out the signals associated with the footprint of a DS5000 or 8051. A standard 40-pin connector may be used for direct mount to a printed circuit board. Alternatively, remote mounting may be accomplished with a 40-conductor ribbon cable terminated with a 40-pin DIP plug. The remote method can be used to retrofit existing systems which have a DS5000 or 8051 socket.

HARDWARE

Figure 1 is a block diagram which illustrates the functional elements of the DS6070 TeleMicro Cartridge. There are actually two microcontrollers incorporated within the design. The first is a DS5000 which is used to execute the user's application software. This is referred to as the target DS5000. All of the facilities of the target DS5000 are available for use in the application including the clock/calendar, 32K bytes of nonvolatile Program/Data RAM, serial I/O, parallel I/O, timers, and interrupt facilities.

The second microcontroller in the system is a DS5000 which performs all of the modem housekeeping functions and recognizes Hayes™ AT commands issued from the target (or user's) DS5000. In addition, this DS5000 (hereafter called the modem controller) controls the serial loading of the target DS5000 from over the phone line. As a result, the entire Embedded RAM area of the target DS5000 may be completely reloaded from scratch over the telephone line. This allows all of the application software and data tables within the RAM to be maintained from a remote host computer, such as an IBM PC.

The 82C50 USART is used for serial data transfers from the target DS5000 when connection is established with remote computer over the telephone line. In addition, when a connection is not established and the modem is in the command mode, the USART is used for communication between the target DS5000 and the modem controller. In this manner, a Hayes-compatible interface is established on the target DS5000's

Embedded Address/Data bus.

The DAA provides a "direct connect" interface to a telephone line. It is FCC Part 68 Type WP registered to meet hazardous voltage, surge and leakage current requirements. A system developed with this product as the DAA meets Part 68 Type WP protection requirements and requires no further registration. The DAA is also CS-03 approved for the Canadian public switched telephone network.

In normal operation, the modem subsystem performs the functions required according to the "AT" commands which are issued to it from the target DS5000. The DS5000 in the modem subsystem takes on the additional responsibility of reloading the target DS5000 under certain specific conditions. In these cases, the modem automatically establishes connection with the host and places the target DS5000 in its Serial Loader Mode. During this time, the modem subsystem isolates signals on the target DS5000 which are used to accomplish the serial download task from the target system circuitry. This includes RST, PSEN*, XTAL1, TXD (P3.1), RXD (P3.0).and P2.7. RST is first driven high to initiate a reset within the target DS5000. Following this action, XTAL1 should be driven by a frequency found in Table #1, unless the optional jumper which ties the XTAL1 pin to the on board 11.059 clock oscillator has been selected. Finally, PSEN* is then driven low. This sequence of actions causes the target DS5000 to begin operation in its Serial Program Load Mode at a clock frequency from which 1200 bps can be derived. Communication between the host computer and the DS5000 via its RXD an TXD pins is established. During this time, P2.7 of the target DS5000 is floated to prevent it from being inadvertantly forced into a Parallel Loader Verify Cycle.

DS6070 STANDARD BAUD RATE CLOCK FREQUENCIES (MHz) Table 1

12.000	6.000
11.059	5.990
11.000	5.069
9.216	4.608
7.373	1.843

None of the activity on the RST, TXD, RXD, XTAL1, P2.7 pins is driven out to the target system lines while the modem is controlling the reloading process. During this time, the target DS5000 appears to be in a reset condition to the target system.

AT COMMANDS

The only software which is provided with the TeleMicro cartridge is that which is resident in the modem subsystem's DS5000. During normal operation, this DS5000 manages the modem IC, and communicates with the target DS5000 via "AT" commands issued from the target DS5000 over the USART's serial I/O lines.

EXTENDED COMMANDS

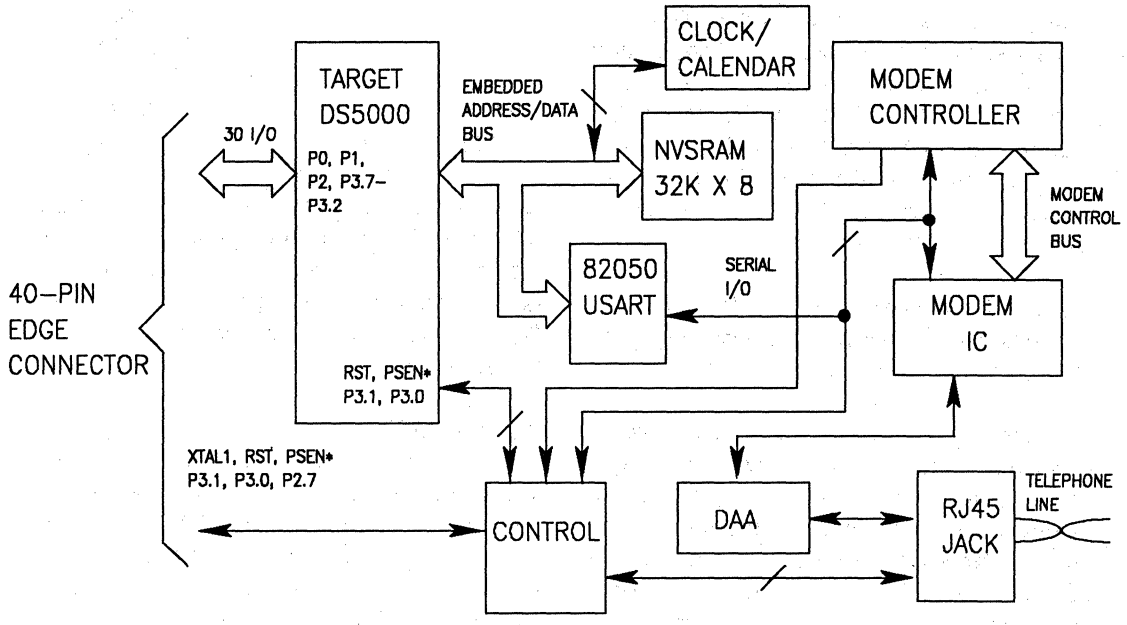
There are a number of commands which have been added to the base AT command set in the TeleMicro Cartridge's internal modem. These additional functions are outlined as follows:

Nn - Number to Memory Register

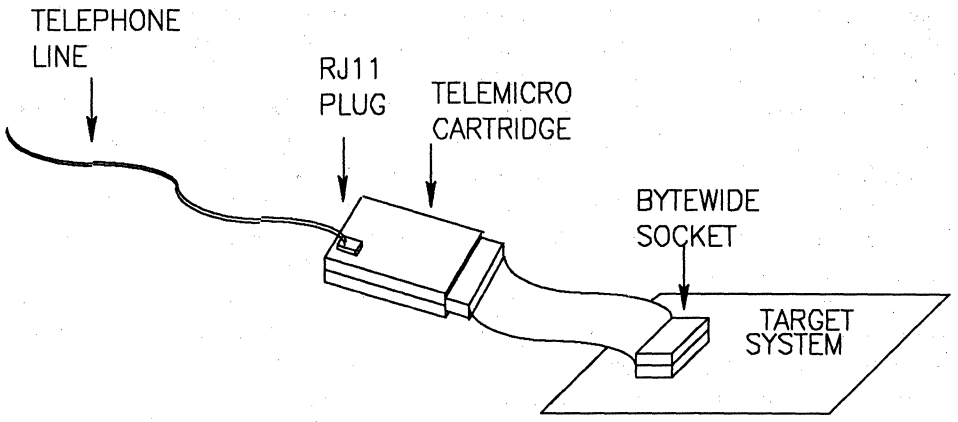
This command may be used to write a telephone number or dialing sequence into one of the 10 nonvolatile memory registers. Each register (designated 0-9) can accept a maximum of 126 entries. The command must include the register destination number, e.g. "N1" stores the number that follows into register number 1. Each number string entered must be terminated with a carriage return.

ATN2DT9,5552287,#289 <CR>

DS6070 BLOCK DIAGRAM Figure 1



TELEMICRO CARTRIDGE INSTALLATION Figure 2



The command causes a specific dialing sequence to be stored in Memory Register 2. The 10 memory registers are nonvolatile, so that they are completely retained in the absence of V_{CC} voltage.

Pn - Print contents of Memory Register
The P command will cause the modem to transmit the contents of the specified memory register. For example, the command **P2** will cause the string **DT9,5552287,#289;** to be returned, assuming the **N2** command was executed as shown above.

#n - Dial from Memory Register
The "#" command is used to execute a command string from one of the nonvolatile memory registers. For example, the command **#2** will cause the modem to use tone dialing to access a number outside of a PBX, pause before dialing, dial the number 5552287, pause, and then issue the PBX transfer code #289.

AUTOMATIC LOG-ON COMMANDS

The modem with the DS6070 provides the capability to have automatic log-on character sequences stored in one of the 10 available Memory Registers. There are seven commands associated with the auto log-on feature. These commands are summarized below:

$ Designates beginning and end of auto log-on strings.

Stop and wait for prompt from the host computer

The following is an example of a Memory Register whose contents include an auto log-on string:

ATDT9W5552344$#<CR>#HOST#ACCOUNT#HOST_PASSWORD[BYE]$

In this example, the modem is programmed to tone dial 9 followed by a wait on second dial tone. Once the dial tone is detected, the phone number "5552344" is dialed. The "$" signifies that an auto log-on character sequence follows. In this case, the modem first waits for a host request (#). Once this is received, a carriiage return character (<CR>) is issued and the modem waits for another host request. Additional information is sent when prompted by the host computer, such as the appropriate account number and password. The auto log-on character sequence is terminated by a second $ command.

NONVOLATILE "S" REGISTERS

The modem within the DS6070 has the capability to retain the "S" registers as nonvolatile data. These registers are used by the modem to hold configuration and operation parameters. In a normal "AT" compatible modem, the S registers are set to their default parameters following a power-on or reset. If nonvolatile operation is desired, then a value of 170 should be written to register S15.

TARGET RELOADING

The host computer can cause the modem controller to take action to force the target DS5000 into its Serial Loader mode using the hardware mechanism described above. This would be done when the host computer needs to perform a complete reload of the application software into the target DS5000. Alternatively, this same action might be taken in a case where the target DS5000 does not respond to communication from the host computer after the modem controller automatically answers the host's call.

In order to perform this operation, the host computer must issue a special "escape sequence" of three ASCII "###". This three character sequence must be preceded and followed by a one second pause. Whenever the modem controller detects this sequence it will request a

password string from the host with the following prompt:

password:

The host must then issue a character string which must match the one which was initially stored in the modem controller's nonvolatile RAM. The password string can contain from 1-11 characters, and must be terminated with a carriage return. Once the password has been correctly entered, the modem controller will force the target DS5000 into its Serial Loader mode and will establish communication between it and the host computer. At this point the host computer is communicating directly with the target DS5000's Serial Loader. Application software can then be loaded into the target DS5000.

Incorrect passwords will cause the DS6070 to respond with prompt "RUNNING". To enter another password, the "###" sequence must be resent.

When the Serial Load operation is complete, the host computer will then issue another escape sequence of three ASCII "$$$" which again must be preceded and followed by a one second pause. When this sequence is detected, the modem controller will allow the target DS5000 to resume execution of its application program.

Both of these special escape sequences can only be issued from the host computer in order for them to be recognized by the modem controller. In addition, the "###" will cause no action in the modem controller if it is issued while the target DS5000 is already in its Serial Load mode. Similarly, the "$$$" sequence will cause no action in the modem controller if it is issued while the target DS5000 is executing its application software.

The intial password string which is recognized by the DS6070 when it is shipped from the factory is the string "password". This string can be modified by the host computer at the time when the old password is entered by suppying a new password as an optional argument. Syntax for this operation is summarized below:

password: **old password [/new password]**

When this character string is entered, the modem controller will request a confirmation of the new password from the host computer as follows:

confirm: **new password**

An example of this entire sequence would be performed as follows:

password: **password /dallas**

confirm: **dallas**

At this point, the originally programmed password string of "password" will have been changed to "dallas".

ELECTRICAL SPECIFICATIONS

Operating Temperature Range	0 to +50 degrees C
System Power Supply Requirements from Target System (no load on port pins, PSEN*, ALE)	+5V @ 150 mA max; 80 mA typical

INTERFACE

Connectors:
RJ45
40-pin card edge (0.1" centers)
40-pin card edge to 40-pin DIP plug on supplied target cable

Notice:
Hayes is a registered trademark of Hayes Microcomputer Products, Inc.

Dallas Semiconductor
Teleservicing Kit

PRODUCT PREVIEW
DS6070K

FEATURES

- IBM PC-based evaluation kit for DS6070 TeleMicro cartridge

- Includes:
  - DS6070 Telemicro Cartridge with 1200 bps Bell 212A modem
  - DS6101 Modem (1200 bps; Bell 212A) on pc board for expansion slot on PC
  - Evaluation software on floppy disk
  - Headset for DS6101 Modem board
  - All necessary cables and documentation

DESCRIPTION

The DS6070K Teleservicing Kit allows immediate evaluation of the DS6070 TeleMicro Cartridge in a target system. The kit supplies all of the necessary hardware, software, and documentation for use with an IBM PC. As a result, the kit provides the tools required to develop a teleserviced system based on the DS6070. Teleservice refers to the ability to perform remote software upgrades and system diagnostics from a desktop computer over a telephone line. The major benefit to the end user is reduced operating costs by eliminating service calls to repair or upgrade equipment in the field.

The hardware included with the DS6070K consists of the DS6070 TeleMicro cartridge, a DS6101 Modem on a pc board, a headset, and all of the cabling necessary to interconnect the system. The DS6070 TeleMicro cartridge provides a connector which interfaces directly to an RJ11 plug to a standard telephone line. In addition, it provides a standard 40-pin edge connector with target cable with may be plugged into a DS5000 or 8051 socket. The DS6101 Modem is installed on a pc board which interfaces directly to an expansion card slot on an IBM PC. The board includes a modular RJ11 telephone

jack for connection to the telephone line. In addition a jack for the headset is mounted on the board. When the DS6101 board is installed in the PC and connected to the telephone line and headset, the user can receive or transmit data or converse in voice. Communication can then take place with a DS6070 over the telephone line, as shown in the recommended configuration in Figure 1.

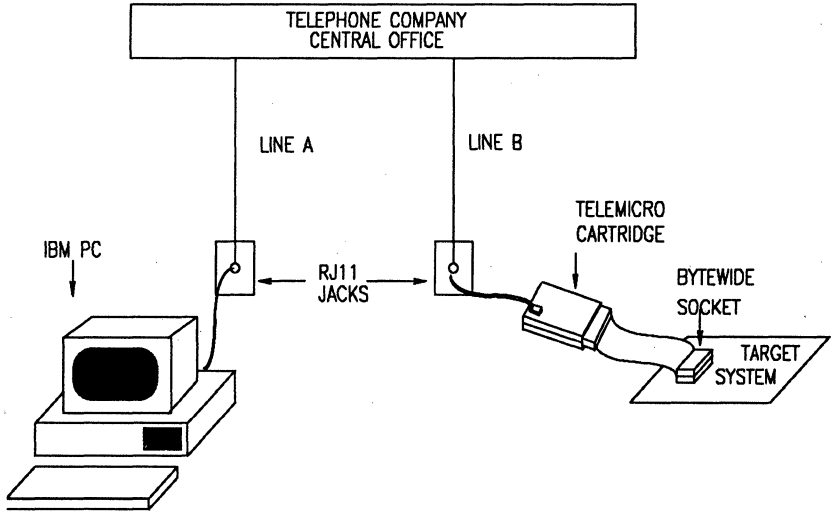
The software included with the DS6070K includes an upgraded version of the KIT5K software which is included with the DS5000TK Evaluation Kit. The upgraded version of KIT5K supports communication to the target DS5000T within the DS6070 through the DS6101 Modem. As a result, a high-level user interface to the target DS5000T is supported such that the user can be walked through a series of system configuration questions so that the target DS5000T can be properly initialized before downloading takes place. Parameters such as the device's Program/Data Memory mapping and Software Encryption operation are initialized in the proper order in this fashion. KIT5K manages all of the communication with the DS5000T during the downloading process, so that the details of the serial download operation can remain transparent to the user. For more advanced users, KIT5K provides a number of commands which allow individual manipulation of the DS5000T's resources. For example, these commands allow the direct initialization of the MCON register, loading of the 40-bit Encryption Key word, and setting and clearing of the Security Lock. In addition, an individual memory location examine and change capability is provided to allow patches to be made to the application software. When the loading operation is completed, the device can be released on command from the PC to run the application software.

Additional software which supports evaluation and operation of the DS6101 Modem Board is also supplied.

SYSTEM REQUIREMENTS

The Teleservicing Kit requires an IBM PC or compatible with DOS 2.0 or later and at least 256K bytes of RAM. Displays which are supported include monochrome, color graphics, or enhanced graphics (Mode 3).

DS6070K RECOMMENDED CONFIGURATION Figure 1



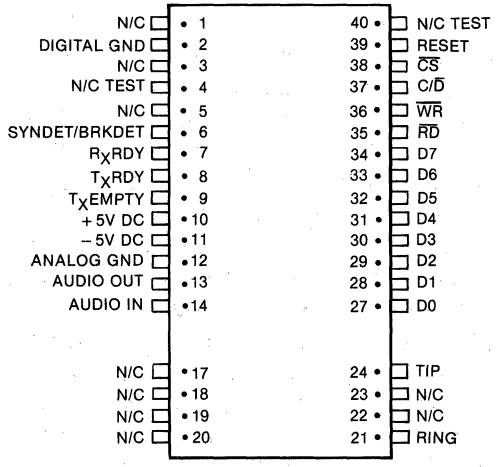
Dallas Semiconductor
212A MODEM Module

DS6101
DS6103

FEATURES

- Very small size - 2.28″ × 1.0″ × 0.5″
- Full Bell 212A/103 Modem compatibility
- FCC Part 68 registered DAA
- Call progress Monitoring
- Tone or pulse dialing
- DTMF sensing and decoding
- Voice sensing
- Soft controlled audio interface
- Voice synthesis option
- Parallel host interface
- ±5 volt power only
- Telephone line diagnostics
- Synchronous/asynchronous operation
- Line frequency monitoring
- Parity generation/checking
- Sync byte detection/insertion

PIN DIAGRAM



DESCRIPTION

The DS6101/6103 Modems are high level communication subsystems manufactured in a component-sized form factor to enable maximum communications capability in minimum amount of space.

The primary function of the Modem is to provide a complete component-sized Bell 212A modem (1200/300 bps) which includes an FCC registered Data Access Arrangement (DAA) in the same package and provides a parallel host interface.

The Modem has an advanced line monitoring capability which allows it to sense the presence of voice or DTMF (touch-tone) signals on the line in addition to its normal call progress monitoring. The Modem may then be switched into an Audio mode for voice communication, or into a DTMF decoding mode which makes it possible to receive information from a remote touch-tone telephone and decode it for the host processor. The DS6103 includes a voice synthesizer for voice prompting in the return path or for the user.

Audio input and output lines are provided with a selection of various functions under host

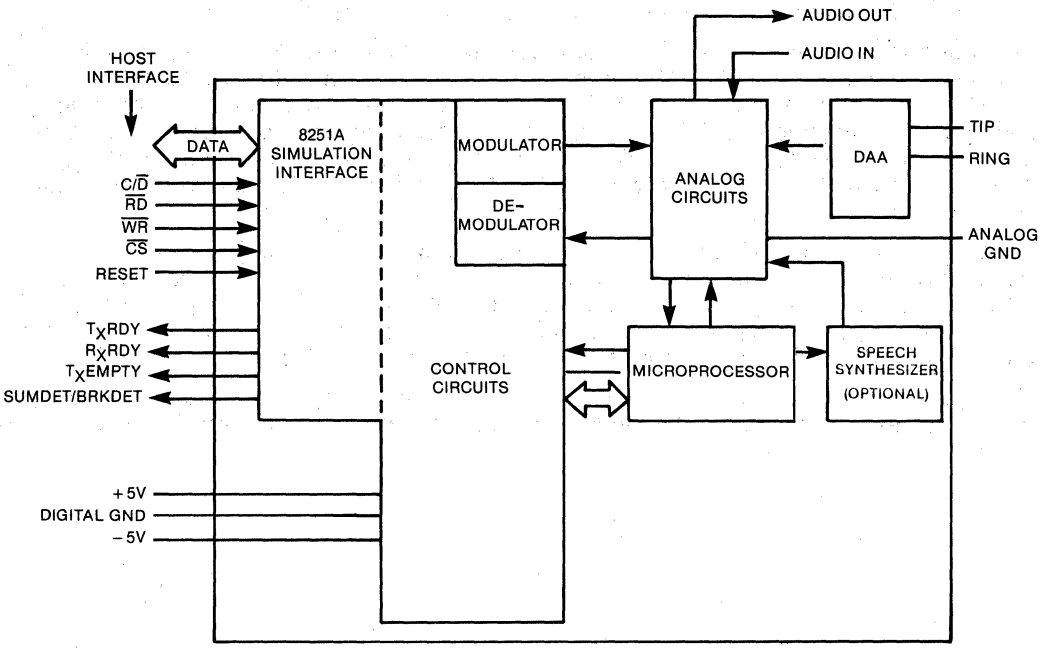
software control. These functions include the use of actual voice communication on the phone line, and modem transmission in the acoustic coupler mode.

The host interface emulates the industry standard 8251A USART with increased bus driving capability. In addition to the 8251A's DATA and COMMAND modes, the DS6101/6103 has a FUNCTION mode. While in the FUNCTION mode, higher level functions such as dialing, answering, line diagnostics, initialization of advanced synchronous communications modes, etc. may be enabled. This provides the internal capability required for an intelligent modem interface while retaining DATA and COMMAND mode compatibility with the simple 8251A standard.

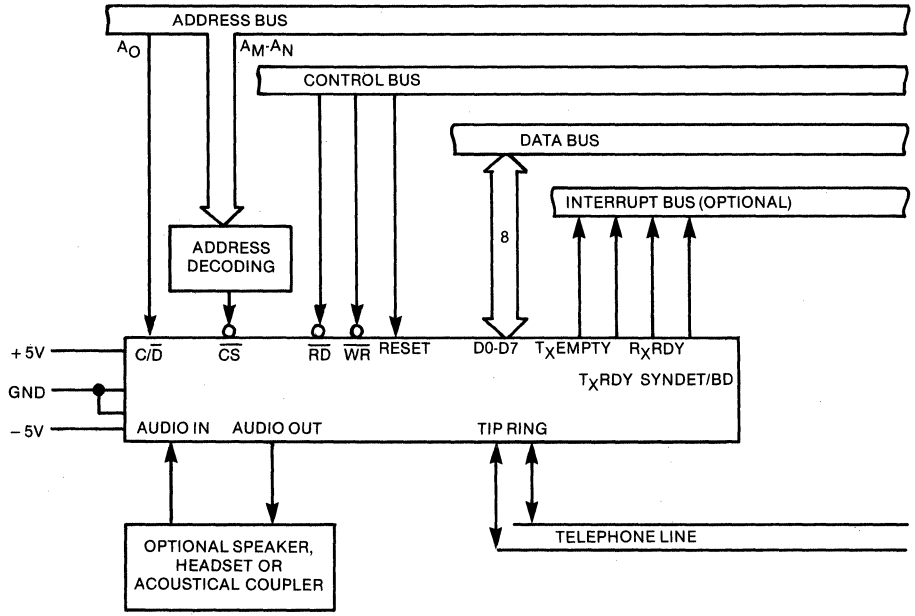
In addition to the basic Bell 212A communications functions and diagnostic modes, the Modems provide both tone and pulse dialing and a comprehensive call progress monitoring capability. A unique telephone line diagnostic capability may be used to report phone line quality to the host, and the Modem's unique internal algorithm automatically uses this diagnostic information to compensate for common line deficiencies.

For complete technical specifications on these and other Dallas Semiconductor's Modem products, the user should obtain the Modem Products Designer's Guide from Dallas Semiconductor.

MODEM BLOCK DIAGRAM



SYSTEM INTERFACE

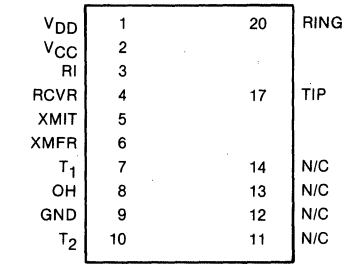


Dallas Semiconductor
Data Access Arrangement (DAA) — *DS6112*

FEATURES

- Interfaces user equipment to public switched telephone network
- FCC Part 68 registered
  - Simplifies system design
  - Minimizes equipment approval cycle
- Ideal for modem applications
- Small size - 1.25″ × 1.0″ × 0.5″
- 2 to 4 wire converter
- 1500 volt isolation
- 800 volt surge protection
- Ring detection

PIN CONNECTIONS



PIN CONFIGURATION

CAUTION
PINS 17 & 20 HAVE 1500V ISOLATION FROM THE REST OF THE CIRCUITRY. THIS ISOLATION SHOULD BE PRESERVED THROUGHOUT THE SYSTEM.

DESCRIPTION

The DS6112 is a communications component that provides a "direct connect" telephone line interface. It is FCC Part 68 Type WP registered to meet hazardous voltage, surge and leakage current requirements. A system developed with this product as the DAA meets Part 68 Type WP protection requirements and requires no further registration.

This component may be used as the direct connect telephone line interface for virtually any application in which voice or data is to be transmitted over the public switched telephone network.

The DS6112 includes both ring detection circuitry and the 2 to 4 wire converter hybrid for use in modem applications. It operates from ±5 volt power supplies and occupies 1.25 square inches of board space.

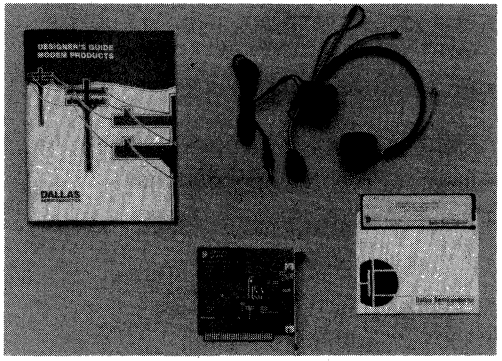
For complete technical specifications the user should obtain the Modem Products Designer's Guide from Dallas Semiconductor.

Dallas Semiconductor
MODEM Evaluation Kit

DS6151
DS6153

FEATURES

- IBM PC-based evaluation kit for DS6101/61103 Modems
- Two versions:
  - DS6151 supplied with DS6101 Modem
  - DS6153 supplied with DS6103 Voice Synthesis Modem
- Printed circuit board provides socket for Modem, RJ11 telephone jack and headset jack; plugs into expansion slot on IBM PC
- Supplied with headset
- Evaluation software on floppy disk
- Supplied with complete operating instructions



DESCRIPTION

The DS6151 and DS6153 Modem Evaluation Kits provide immediate evaluation of the DS6101 and DS6103 Modems. The kits supply all of the necessary hardware, software and documentation for use with an IBM PC. A printed circuit card which sockets the appropriate Modem plugs directly into the backplane of the PC and provides a modular RJ11 connector to a telephone line. In addition, a jack for the headset which is supplied with the kit is mounted on the board. A complete set of documentation with instalation and operating instructions is also supplied. A user need only have a private telephone line with a modular plug to insert into the RJ11 jack and he or she can be using the modem to converse in voice, transmit data or listen to synthesized voice responses in just a few minutes.

For more information on this product, see the Modem Designers Guide.

NOTES

NOTES

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