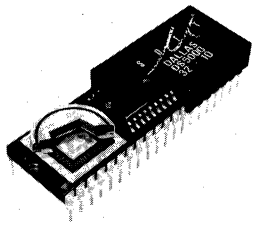

1988 DATA BOOK

**DALLAS**
**SEMICONDUCTOR**

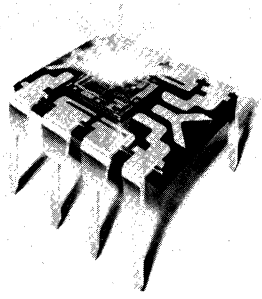
DALLAS SEMICONDUCTOR 1988 DATA BOOK

# Late Definition Technologies

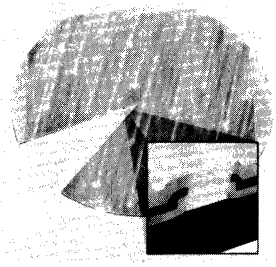
Through the use of special late definition technologies, products can be tailored to meet an exact application after wafer fabrication is complete. Modifications may be made either by the Company or in the field by the user. Certain products are also capable of self-modification based on feedback information.



**Embedded Lithium Power Sources:**
Dallas Semiconductor has the ability to integrate in a single package, its ultra low power CMOS circuits and a miniature lithium power source. Chips designed in this way can accept change and remember data throughout their operating life.



**Direct Laser Writing:**
Lasers provide a low cost means for Dallas Semiconductor to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication. Proprietary software controls the laser to make each chip unique.



**High Energy Ion Implantation:**
Circuits on nearly finished wafers are defined to exact customer specifications. Using a million-volt implanter, wafers are bombarded by a cloud of super charged ions. The ions penetrate specific layers of silicon to economically tailor chips to specific functions.

**DALLAS**
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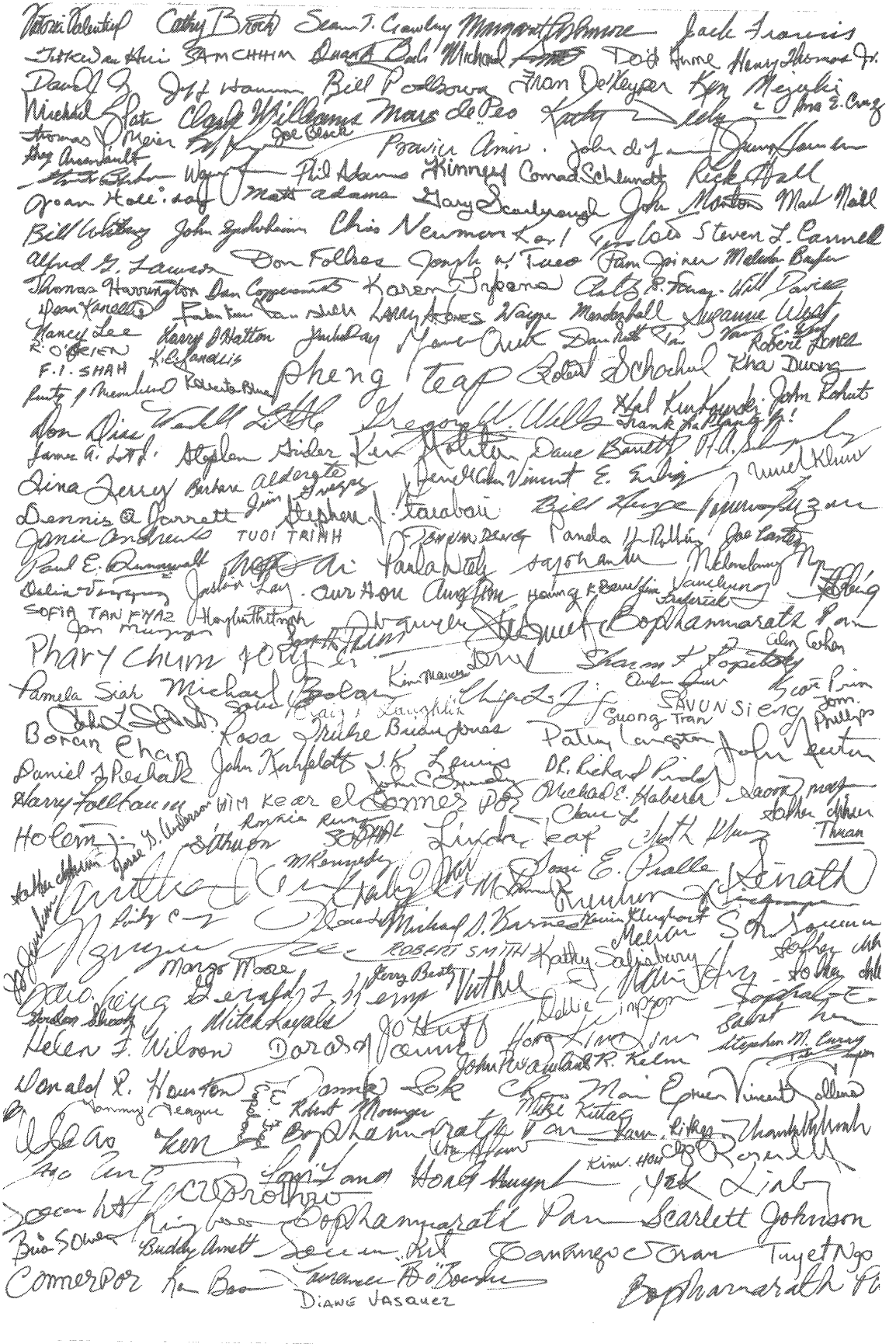
*not the only name behind our products . . .*



# Dallas Semiconductor

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# General Information

# Product List

# Corporate Fact Sheet

Dallas Semiconductor designs, manufactures and markets CMOS integrated circuits using special Late Definition technology. Late Definition permits the exact definition of a product to be postponed until end use, thereby increasing flexibility.

**PRODUCTS**

Founded February 1, 1984, Dallas Semiconductor has a multi-product strategy to serve the needs of the computer and communications industry. Our optimism stems from the ability to sell "Soft Silicon" which can be readily tailored to solve the specific problems of our customers. Soft silicon results from the Late Definition technologies of lithium, laser, and implant. Lithium postpones definition until end use, thereby making the chip adaptive in the system. Laser postpones definition until just before the chip is placed in the package, and implant postpones definition until the last wafer process step.

**LITHIUM**

Advances in CMOS circuitry have reduced power requirements to the point that a chip, using appropriate circuitry, can be packaged with a miniature lithium energy source which will last the useful life of the equipment. This allows Dallas Semiconductor to make chips which don't forget. Our initial product offerings exploited this capability to make the much sought-after nonvolatile RAM. In November 1984 we began shipping 16K, 64K Nonvolatile SRAMs.

Keeping track of human time has not been an easy task for computers until our July 1985 announcement of the DS1216 SmartWatch. It precisely keeps calendar time down to the hundredth of a second, replacing what heretofore consumed a whole printed circuit board full of electronics. A lithium cell provides power for life.

The adaptive nature of CMOS/Lithium products is made evident by the April 1987 introduction of the DS5000 Soft Microcontroller. Designed with change in mind, it offers unprecedented software adaptability and crash-proof operation. The capabilities of the Soft Microcontroller take it beyond mere update change and into the realm of learning. The DS5000 can capture a large amount of data in real time and remember it indefinitely. With the proper application software, the microcontroller can improve its performance based on that cumulative knowledge.

**LASER**

The laser creates uniqueness on a chip at low cost. A sub-micron positioning laser and formidable control software developed at Dallas can engrave individual chips with digital patterns making each one different. These after-the-fact changes to completed circuits give our laser-based products a competitive edge.

The first product that demonstrated our special laser technology was an extremely accurate time base, commonly referred to as a delay line. Before the August 1985 announcement date, it had only been possible to build such devices using a dozen components in a hybrid assembly. The DS1000 Silicon Delay Line series is a direct replacement for hybrid delay lines which are widely used in conjunction with DRAMs and magnetic disks.

Other products use the laser to protect sensitive information and intellectual property by creating a powerful security mechanism in micro chips. The DS1204 Electronic Key is an example of a product which benefits from the laser in this regard. Exclusive blank Keys are defined by laser for each customer, adding to the overall security mechanism. Additional products are on the drawing board whereby the laser tailors the option content of the chip for a particular customer. In short, the laser lets Dallas Semiconductor define each chip uniquely after it is already operational.

**IMPLANT**

Nearly-finished wafers can be defined to meet exact customer requirements in a matter of days with high energy ion implant

technology. A number of products will be offered with an "Express Delivery Service."

Difficult system problems have been solved by relying on these special technologies, experience, and creativity, to offer our customers a more complete solution than the chip alone can provide. Often this requires a greater emphasis on packaging than traditional semiconductor producers have been accustomed. Fifty-one base products were put into production prior to January 1988, unified by our own CMOS technology.

**MANUFACTURING AND FACILITIES**

Dallas Semiconductor manufactures products at a 65,000-square-foot facility, which it owns, located at the company's headquarters in north Dallas. This location includes an advanced Class One wafer fabrication facility completed in 1987. Six-inch wafers are processed with circuits utilizing sub-micron geometries. Automated modular process technology provides substantial flexibility in the manufacturing process and significantly reduces the number of people required for operation, thereby decreasing manufacturing costs. The company's wafer fabrication facility contains a 10,000-square-foot cleanroom. The sensitivity of the manufacturing process to particulates and other contaminants requires a highly controlled, clean environment. All products are shipped from Dallas after final quality assurance testing.

**MARKETING AND SALES**

Dallas Semiconductor sells its products to a large and diverse customer base of both mature and emerging OEMs in the computer, telecommunications, instrumentation, and factory automation markets. The Company coordinates its selling activity from its Dallas, Texas headquarters. Five area sales offices are staffed in Marlton, New Jersey; Cupertino, California; Los Angeles, California; Carmel, Indiana; and Birmingham, England. The Company's five area sales managers call on OEM accounts and coordinate the activities of 45 sales representative offices in North America and 22 in European countries and Asia. Dallas Semiconductor also markets its products in North America through a national stocking distributor and through ten regional distributors.

# North American Sales Offices

**Northern California**
Cupertino, CA
(408) 973-7850

**Southern California**
Newport Beach, CA
(714) 646-7219

**Indiana**
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(317) 844-5044

**New Jersey**
Marlton, NJ
(609) 667-7755

**Texas**
Dallas, TX
(214) 450-0400

# European Sales Office

West Midlands, UK
021-745-8252

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Alfatron Pty, Ltd.
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Vienna
(0222) 824199

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BETEA
Brussels/Benelux
(02) 736-8050

**France**
REA
Levallois Perret
758.11.11

Holland
Alcom Electronics
Rotterdam
010 451 95 33

Tekelec Airtronic
Paris
(1) 534.75.92

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(5) 200922

**India**
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Bangalore
812-564464

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Craigavon
Co. Armagh
0762 339818

**Israel**
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Tel Aviv
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(02) 612-0641

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Mameli
(02) 738-0641

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Systems Marketing, Inc.
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03-254-2751

Microtek Inc.
Tokyo
03-371-1811

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Dynamar Int'l, Ltd.
Singapore
7476188

**Portugal**
Digicontrole
Lisbon
292.39.24

**Scandinavia**
Integrerad Elektronik
Komponenter AB
Bromma
08-80 4685

**Sweden**
Commit Electronics AB
Taby
08 792 3650

**Singapore**
Dynamar Int'l, Ltd.
65-7476188

**South Korea**
Vine Overseas Trading
Seoul
(02) 266-1663

**Spain**
Comelta, S.A.
Madrid
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Kontron Electronic AG
Zurich
01/435 4111

**Taiwan**
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Taipei
(02) 709-3515

**United Kingdom**
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021-643-6999

Ambar Cascom Ltd.
Bucks
296-434-141

Dialogue Distribution Ltd.
Camberly, Surrey
0276-682001

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Martinsried/Munich
(089) 8 57 2086

Astek Elektronik
Kaltenkirchen
4191-8711

Kontron Halbleiter GmbH
Munich
319 01-377

# North American Sales Representatives

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Glen White and Associates
Huntsville, AL
(205) 882-6751

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Thousand Oaks, CA
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Harvey King, Inc.
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Nepean, Ontario
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Pointe Claire, Quebec
(514) 694-0404

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Rolling Meadows, IL
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Towson, MD
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(313) 478-8106

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St. Paul, MN
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Albuquerque, NM
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Giesting & Associates
Cleveland, OH
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Giesting & Associates
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Western Technical Sales
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**Oregon**
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**Washington**
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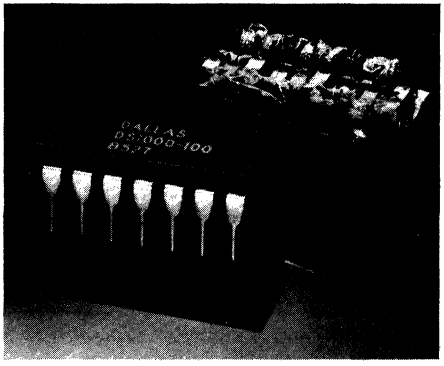
(206) 453-8300

# PRODUCT OVERVIEW



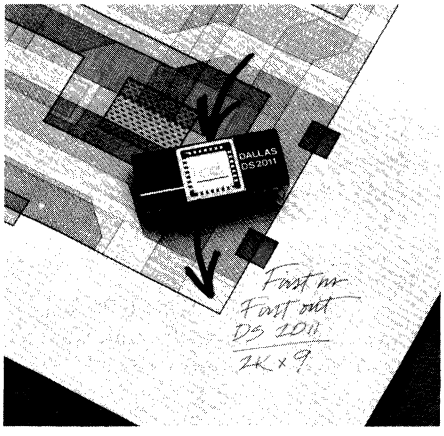
## Silicon Timed Circuits




Electronic systems require exact timing to control the transmission of data between their component parts. Timing requirements vary across systems. Historically, systems designers have not been able to use semiconductors as timing references because of their lack of precision; they consequently achieved the required accuracy by using, in combination, quartz crystals and hybrid passive components, known as delay lines. All silicon delay lines offer single chip reliability, economy and significantly greater precision due to their laser-defined specifications. Direct laser writing provides precise accuracy and, because the products are defined in the final stage of manufacturing, a broad product mix is available without losing the economic benefits of standard integrated circuit production. Customers are provided maximum flexibility, as well as the option of purchasing tailor-made products at the approximate cost of standard, off-the-shelf solutions. These all silicon products can be retrofitted into existing systems which otherwise utilize hybrid approaches as well as designed into new systems.

DS1000 5 TAP Delay Line
DS1010 10 TAP Delay Line
DS1013 3 in 1 Delay Line
DS1007 7 in 1 Delay Line

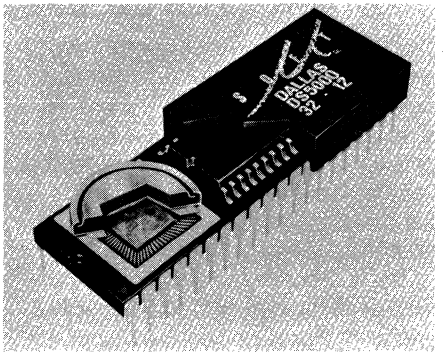
## Multiport Memory




The existence of many different data transmission rates and standards has created a problem in transporting data among different systems. A receiving system may be too slow to keep up with data sent from another system. First In, First Out (FIFO) memories are capable of providing the necessary elasticity between different data rates.

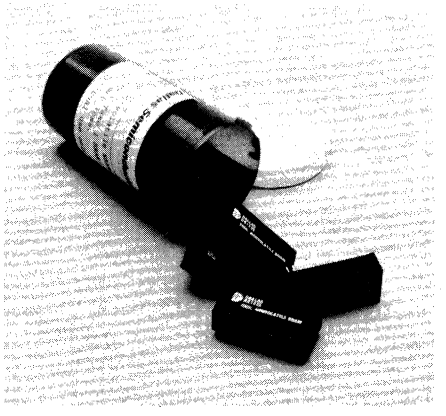
DS2009 512 x 9 FIFO
DS2010 1K x 9 FIFO
DS2011 2K x 9 FIFO
DS2012 4K x 9 FIFO
DS2015 4 x 64 Quadport Serial RAM

## Microcontroller



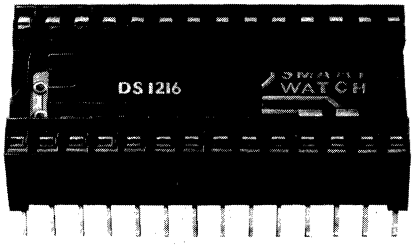
The DS5000 Soft Microcontroller stays up-to-date because it was designed for change. Unlike rigid ROM or EPROM based microcontrollers, all of the Soft Microcontroller memory is high performance, read/write, and nonvolatile for more than ten years. The DS5000 is equipped with 32K bytes of nonvolatile SRAM which can be dynamically partitioned to fit program and data storage requirements of a particular task. As a result of sophisticated crashproofing circuitry, processing of a task can resume after a power outage. A built-in encrypter prevents unauthorized access to resident application software. The pinout and instruction set match the industry standard 8051 microcontroller. Additional information is available in a special publication called the Soft Microcontroller User Guide. The DS5000K evaluation kit includes a sample DS5000, documentation, in-system loader hardware and DOS compatible software for use with a personal computer.

## Nonvolatile SRAM



SRAMS have always had the undesirable characteristic of data loss when power is disrupted. Dallas Semiconductor has combined its knowledge of ultra low power CMOS SRAMs with improvements in long life embedded lithium power sources to develop a family of Nonvolatile SRAMs. Nonvolatile SRAMs integrate a lithium power source and intelligent control circuitry to retain data even in the absence of system power. The control circuit, by monitoring the level of system voltage available to the memory at all times, switches to the lithium power source when necessary, and also protects the memory contents against inadvertent change during system power fluctuatuions. A lithium power source provides backup power for more than 10 years in the absence of system power. Nonvolatile SRAMs are packaged to fit into existing sockets and can replace other widely used memory devices.These products perform better in many applications than EEPROMs, EPROMs, or shadow RAMs because they provide unlimited data write cycles, safeguard against corrupted data and write data in as fast as 70 ns.
DS1220 2K x 8 24 pin Nonvolatile SRAM
DS1225 8K x 8 28 pin Nonvolatile SRAM
DS1230 32K x 8 28 pin Nonvolatile SRAM

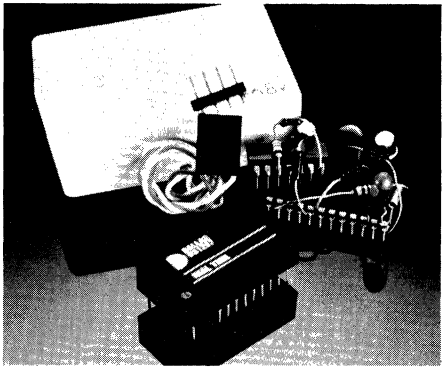
## Intelligent Sockets




Often, after a design is complete, the manufacturer may desire to enhance functionality because of increased competition from newer products. The equipment manufacturer is forced either to avoid adding features or design a new system. Dallas Semiconductor has incorporated active electronics in connectors which can be plugged into a system and add capabilities without requiring substantive changes in the existing system. For example, many systems manufacturers desire the capability to make RAMs in existing systems nonvolatile. In this instance, they can unplug a memory circuit in a system currently in use, plug the SmartSocket into that space, and plug the memory circuit into the SmartSocket. Another example is a requirement in many existing systems to monitor and record time of day. The SmartWatch plugs into existing systems and keeps time of day to hundredths of a second while also making memory circuits nonvolatile.

DS1213 SmartSocket - makes CMOS RAM nonvolatile
DS1216 SmartWatch - adds the ability to time stamp and date events
DS1264 LCA SmartSocket - maintains logic in the absence of power

## TimeKeeping



Systems benefit by knowing the time-of-day, but the use of this feature has been limited by its expense and high component count. A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. The DS1287 Real Time replaces 20 parts used in the IBM AT and PS/2 compatible computers including an MC146818 Real Time Clock plus RAM.

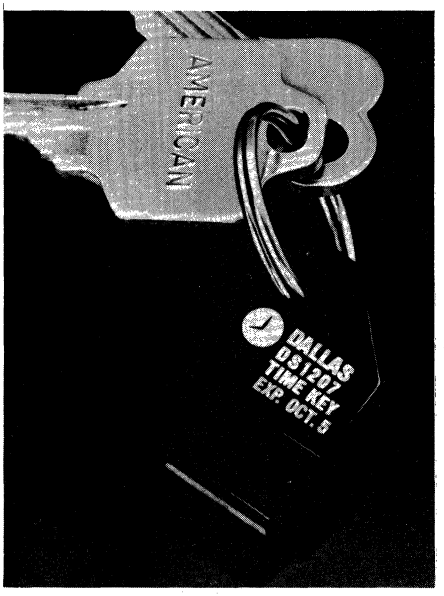
DS1215 TimeChip
DS1287 Real Time
DS1286 WatchDog

## User Insertable Memory


Manufacturers of equipment often wish to facilitate user configuration of their standard products. In many instances, user insertable solid state memories offer distinct advantages over alternative media, such as magnetic tape or disk. Such memories, however, demand specialized packaging capable of withstanding harsher environmental conditions than those normally encountered by semiconductor memory circuits. A family of Nonvolatile SRAMs has been specifically developed to address this application sector. These products range in density from 1024 bits to 32,000,000 bits, the largest of which replaces rotating memory subsystems in certain personal computer systems.

DS1201 1K bit Electronic Tag
DS1217A up to 256K bit Nonvolatile Read/Write Cartridge
DS1217M up to 4M bit Nonvolatile Read/Write Cartridge
DS6010 P.C. Port
DS9020 Cartridge Clip

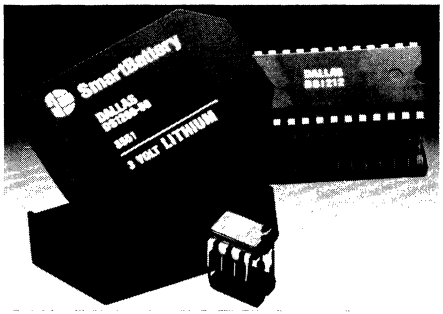
## Security Products




In an information age, there is an increasing demand to provide security for intellectual property and other data beyond legal measures currently available. Prominent examples are publishers and authors of premium-priced personal computer software who have strong motivation to protect their products from unauthorized use. Software based copy protection systems interfere with the need to make legitimate backup copies or execution from hard disks. The Electronic Key is a postage stamp-sized package that is distributed with each software package sold and must be present whenever users want to use the software. This same principle can be applied to controlling access to buildings, automobiles and other equipment.

DS1204 Electronic Key
DS1207 Time Key
DS1255 Key Ring
DS1255C Evaluation Kit for IBM P.C.

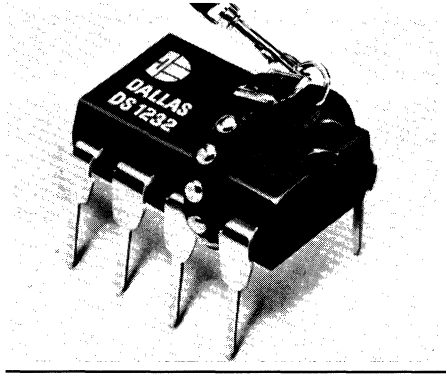
## Integrated Battery Backup




Microprocessor based systems lose information when affected by a loss of power. When system power is resumed, the task that was being performed at the time of power loss must be re-started. Uninteruptible power supplies have historically been provided as relatively expensive, bulky, external units. A solution to this problem is necessitated in industrial automation applications and in systems which are located in remote sites or otherwise difficult to reprogram when information is lost. The Integrated Battery Backup consists of a three part chip set which operates in three steps. First, the Power Monitor warns a microprocessor of an impending power failure before it happens, providing time for critical data to be stored in nonvolatile memory before system power is lost. Second, the Nonvolatile Controller/Decoder converts RAM into nonvolatile memories and safeguards against RAM data loss during power up and down transients, by automatically switching to battery power when system power failure occurs. Third, the SmartBattery supplies uninterruptible power in the absence of system power to maintain data in nonvolatile memory.

DS1210 Single RAM Controller
DS1221 Four RAM Controller
DS1211 Eight RAM Controller
DS1212 Sixteen RAM Controller
DS1234 Conditional RAM controller
DS1231 Power Monitor
DS1260 Smart Battery
DS1259 Battery Manager

## System Extension

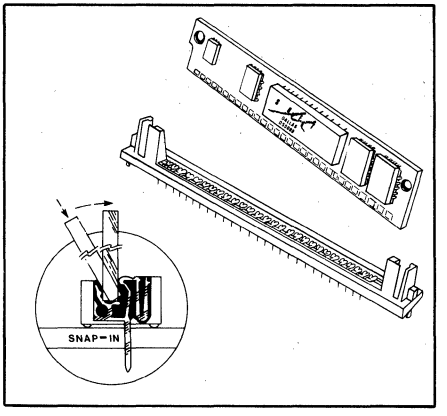



These CMOS products extend the usefulness of systems without encumbering design. The Micro Monitor acts as a "watchdog" for system malfunction by checking the three most important indicators of correct microprocessor operation - power supply, software execution and override push-button. If it detects a problem, the MicroMonitor shuts down the system, then resets it for correct operation. The Eliminator replaces the equivalent of an 8 or 16

station manual DIP switch, thus eliminating burdensome hand setting of mechanical switches. Five volt powered RS232 transceivers are available in both dual and triple versions. The same five volt supply that powers logic generates RS232 voltage levels.

DS1232 MicroMonitor
DS1290/91 Eliminator, 8-Station
DS1292/93 Eliminator, 16-Station
DS1206 Phantom Interface
DS1223 Configurator
DS1222 Bank Switch
DS232/DS1228 RS232 Transceiver, Dual
DS1229 RS232 Transceiver, Triple

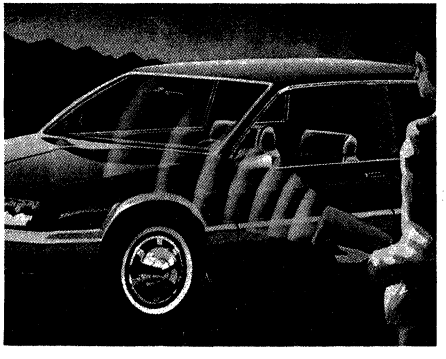
## SipStiks™




Systems snap together with SipStik sub-assemblies from Dallas Semiconductor. SipStiks are leadless carriers of components with high silicon content using JEDEC standard configurations. Their low profile form factor permits high density yet offers the advantages of modularity. These major building blocks are pretested and ready for final assembly into a planar motherboard fitted with AMP MicroEdge connectors as required by a particular application.

DS2217 SRAM SipStik
DS2209 DRAM SipStik
DS2250 Soft Micro SipStik
DS2245 Modem SipStik

## Wireless Products



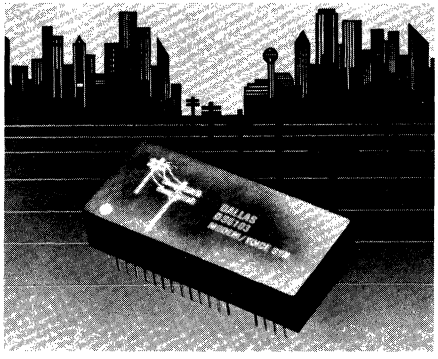
Portable DS1201 Electronic Tags, DS1204 Keys, or DS5000 Soft Microcontrollers can communicate with a personal computer using CMOS Micropower Receiver/2 to 3 Wire Converter chips and a base RF Communicator. The chips contain wake-up circuitry, amplifiers, filters, timing generators, waveform interpreters, formating and control logic necessary to form a bi-directional 5 foot link between portable units and bases. The ultra low power consumption of the chips enable a single 3 volt lithium energy cell to

be a permanant source of power for receiving, storing, and transmitting data.

DS1203 MicroPower Receiver
DS1209 2 to 3 Wire Converter
DS1280 Bytewide to 3 Wire Converter
DS6068 RF Communicator

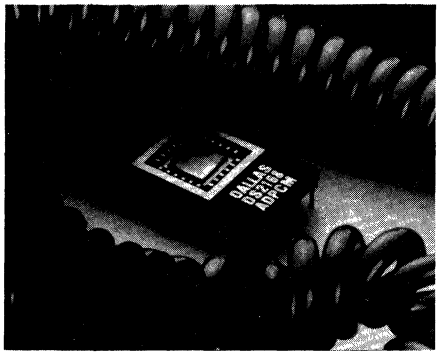


## Modem



These Miniature components comply with FCC part 68 registration. The DS6101 Modem is bell 212A compatible (1200/300 bps) with DTMF generation/ detection, audio mode operation, and advanced line monitoring functions. The DS6103 Modem provides voice synthesis. The DS6112 Data Access Arrangement (DAA) which is included in the Modems above is available as a stand alone interface to the public switch telephone network. DS6151/6153 are Modem evaluation kits that demonstrate the Modem on the IBM/PC/XT/AT.

## Telecommunications



An emerging and rapidly growing market exists for high capacity voice, data and video transmission. High capacity digital links in North America and Europe are known as T-1 and CEPT, respectively. Circuits designed for these protocols can substantially shorten the time required for OEMs to develop products that access these networks and can reduce systems sizes. A comprehensive chip set developed by Dallas Semiconductor addresses the requirements of these protocols and includes an integrated circuit that doubles the capacity of existing voice communication links through digital signal processing compression techniques. Complete product specifications available in a supplemental telecommunication data book.
DS2180 Transceiver, T1
DS2181 Transceiver, CEPT
DS2175 Transmit/Receive Elastic Store
DS2176 Receive Elastic Store
DS2186 Transmit Line Interface
DS2187 Receive Line Interface
DS2190 Network Interface Unit
DS2167 ADPCM Processor
DS2157 Compression Array

# Product Data Sheets

# Silicon Timed Circuits

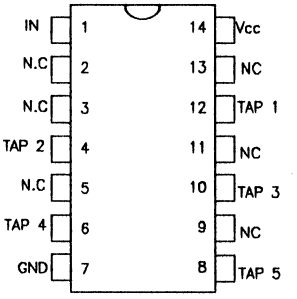
# Dallas Semiconductor
## *5 TAP Silicon Delay Line*

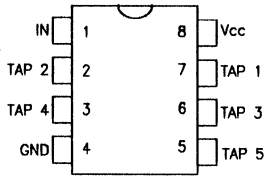
## *DS1000 14 Pin DIP*
## *DS1000M 8 Pin DIP*
## *DS1000S 16 Pin SOIC*

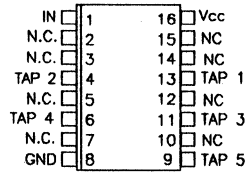
### FEATURES

- All silicon time delay
- 5 TAPS equally spaced.
- Delays are stable and precise
- Both leading and trailing edge accuracy
- Standard 14 pin DIP, 8 pin MINI-DIP, or 16 pin SOIC
- Delay tolerance +/- 5%
- Economical
- Auto-insertable
- Low power CMOS
- TTL compatible

### PIN CONNECTIONS




### PIN NAMES

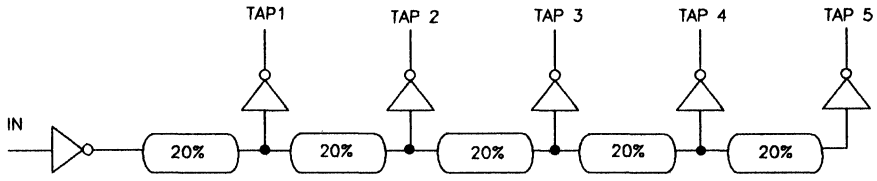
TAP 1-TAP 5 - TAP Output Number
Vcc - +5 Volts
GND - Ground
NC - No Connection
IN - Input

### DESCRIPTION

The DS1000 Series Delay Lines have five equally spaced TAPS providing delays from 10 ns to 500 ns. These devices are offered in a standard 14 pin DIP, which is pin compatible with hybrid delay lines. Alternatively 8 pin MINI-DIPS and surface mount packages are available which saves P.C. board area. Since the DS1000 series is an all silicon solution, better economy is achieved when compared to older methods using hybrid techniques.

The DS1000 Series Delay Lines provide a nominal accuracy of +/-5% or +/- 2 ns, which ever is greater. The DS1000 Delay Line reproduces the input logic level at the output after a fixed delay as specified by the dash number extension of the part number. The DS1000 is designed to reproduce both leading and trailing edge with equal precision. Each TAP is capable of driving up to ten 74LS type loads.

## FIGURE 1: LOGIC DIAGRAM






## TABLE 1: PART NUMBER DELAY TABLE ($t_{PHL}$, $t_{PLH}$)

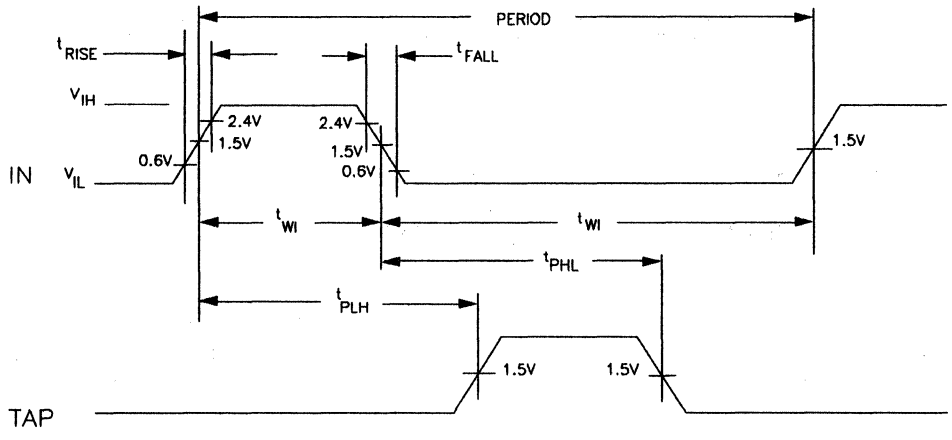
| PART NO. | TAP 1 | TAP2 | TAP3 | TAP4 | TAP5 |
|---|---|---|---|---|---|
| DS1000-50 | 10ns | 20ns | 30ns | 40ns | 50ns |
| DS1000-60 | 12ns | 24ns | 36ns | 48ns | 60ns |
| DS1000-75 | 15ns | 30ns | 45ns | 60ns | 75ns |
| DS1000-100 | 20ns | 40ns | 60ns | 80ns | 100ns |
| DS1000-125 | 25ns | 50ns | 75ns | 100ns | 125ns |
| DS1000-150 | 30ns | 60ns | 90ns | 120ns | 150ns |
| DS1000-175 | 35ns | 70ns | 105ns | 140ns | 175ns |
| DS1000-200 | 40ns | 80ns | 120ns | 160ns | 200ns |
| DS1000-250 | 50ns | 100ns | 150ns | 200ns | 250ns |
| DS1000-500 | 100ns | 200ns | 300ns | 400ns | 500ns |

**ABSOLUTE MAXIMUM RATINGS***

Voltage on a pin to ground:-1.0Vto + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C
Soldering
temperature: 260°C for 10 seconds
Short circuit output current: 50mA for 1 second

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## FIGURE 2: TIMING DIAGRAM SILICON DELAY LINE




### Terminology

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

$t_{WI}$ (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

$t_{RISE}$ (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

$t_{FALL}$ (Input Fall Time) The elapsed time between the 80% and the 20% point on the railing edge of the input pulse.

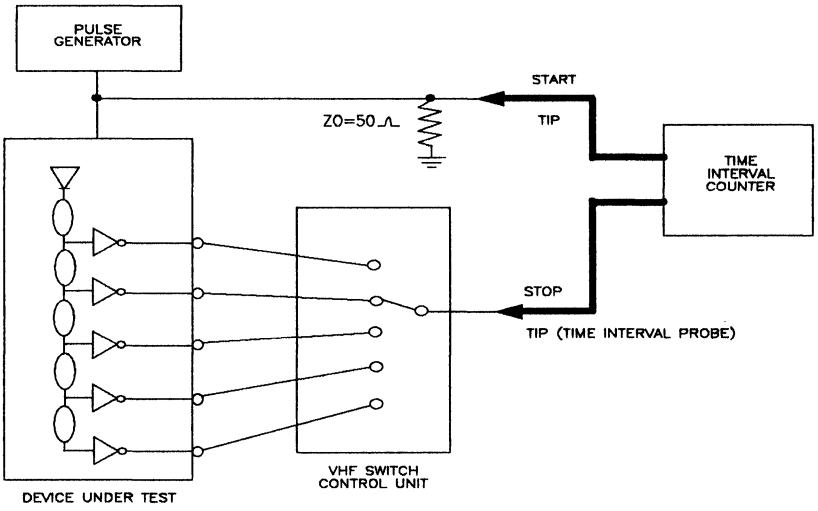
$t_{PLH}$ (Time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

$t_{PHL}$ (Time Delay, Falling) The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any TAP output pulse.

### Notes

1.)All voltages are referenced to ground.
2.)Measured with outputs open, minimum period.
3.)Vcc=5V @25°C Delays accurate on both rising and falling edges within +/- 2 ns, or 5%.
4.)See Test Conditions (following page).

## FIGURE 3: DALLAS SEMICONDUCTOR TEST CIRCUIT






### Test Setup Description

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1000. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit.

The measurement setup is calibrated by TDR (time domain reflectometry) techniques. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

### Test Conditions

**Input:**

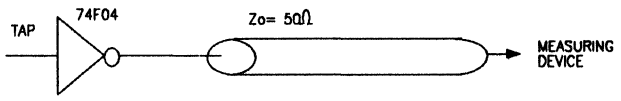
Ambient Temperature: 25°C+/-3°C
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High = 3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50Ω Max.
Rise and FAll Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 500 ns
Period= 1us

**Note:**

Above conditions are for test only and do not restrict the operation of the device under other conditions.

**Output:**

Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.



## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5.0V +/- 5%)

| PARAMETER | SYMBOL COND. | TEST | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | Vcc | | 4.75 | 5.00 | 5.25 | V | 1 |
| High Level Input Voltage | $V_{IH}$ | | 2.2 | | 5.5 | V | 1 |
| Low Level Input Voltage | $V_{IL}$ | | -0.5 | | 0.8 | V | 1 |
| Input Leakage Current | $I_I$ | $0.0V \leq VI \leq Vcc$ | -1.0 | | 1.0 | *u*A | |
| Active Current | $I_{CC}$ | Vcc= Max; Period= Min. | | | 35.0 | mA | |
| High Level Output Current | $I_{OH}$ | Vcc= Min. $V_{OH}$= 2.4V | 1.0 | | | mA | |
| Low Level Output Current | $I_{OL}$ | Vcc= Min. $V_{OL}$= 0.5V | 12.0 | | | mA | |

## A.C. ELECTRICAL CHARACTERISTICS

($T_A$= 25°C, Vcc=5V+/- 5%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Pulse Width | $t_{WI}$ | 40% of TAP 5 | | | ns | |
| Input to TAP delay (leading edge) | $t_{PLH}$ | note 3 | Table 1 | note 3 | ns | 4 |
| Input to TAP Delay (trailing edge) | $t_{PHL}$ | note 3 | Table 1 | note 3 | ns | 4 |
| | Period | 4 ($t_{WI}$) | | | ns | |

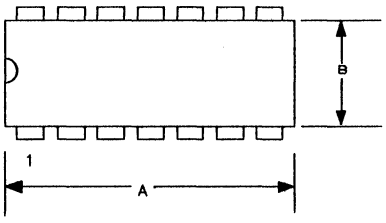
## CAPACITANCE

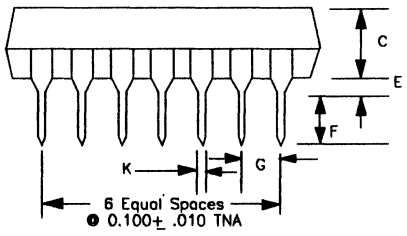
($T_A$= 25°C)

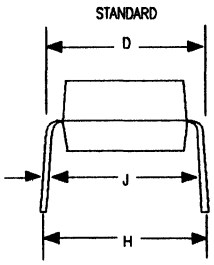
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_N$ | | 5 | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | 5 | 10 | pF | |

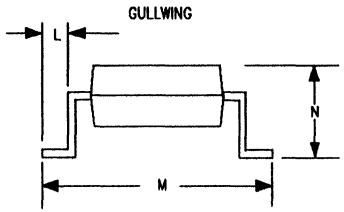
# SILICON DELAY LINE
# DS1000
# 14 Pin DIP

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.740 | 0.780 |
| B | 0.240 | 0.260 |
| C | 0.120 | 0.140 |
| D | 0.290 | 0.310 |
| E | 0.020 | 0.040 |
| F | 0.110 | 0.130 |
| G | 0.090 | 0.110 |
| H | 0.300 | 0.350 |
| J | 0.008 | 0.012 |
| K | 0.015 | 0.021 |
| L | 0.040 | 0.060 |
| M | 0.370 | 0.420 |
| N | 0.160 | 0.180 |

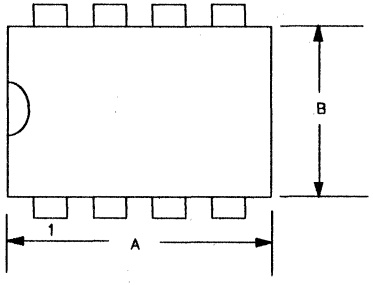


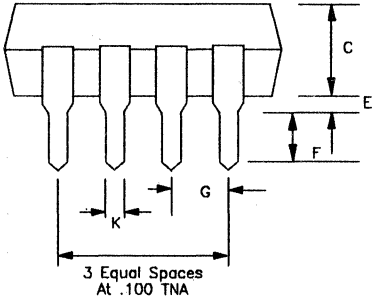



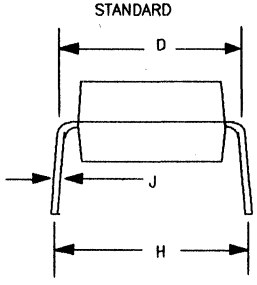



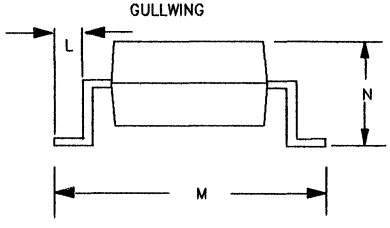
# SILICON DELAY LINE
# DS1000M
# 8 Pin DIP




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.360 | 0.400 |
| B | 0.240 | 0.260 |
| C | 0.120 | 0.140 |
| D | 0.290 | 0.310 |
| E | 0.020 | 0.040 |
| F | 0.110 | 0.130 |
| G | 0.090 | 0.110 |
| H | 0.300 | 0.350 |
| J | 0.008 | 0.012 |
| K | 0.015 | 0.021 |
| L | 0.040 | 0.060 |
| M | 0.370 | 0.420 |
| N | 0.160 | 0.180 |

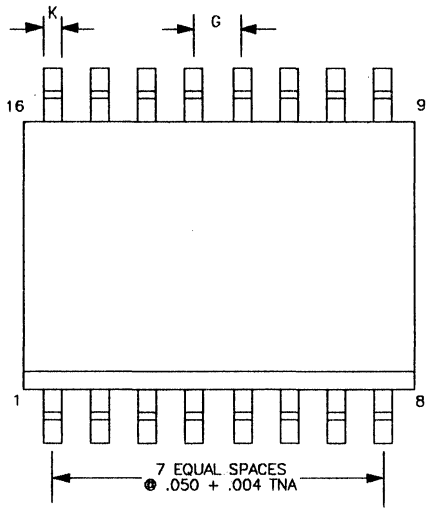


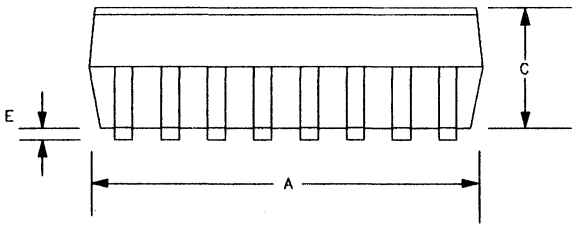



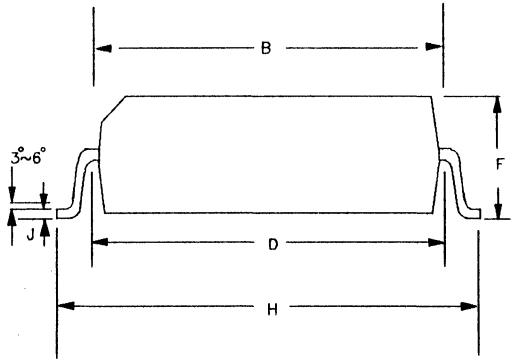
# SILICON DELAY LINE
# DS1000S
# 16 Pin SOIC






| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



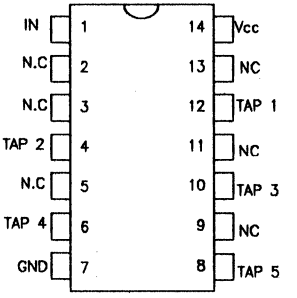
# Dallas Semiconductor
## *5 Tap Silicon Delay Line*

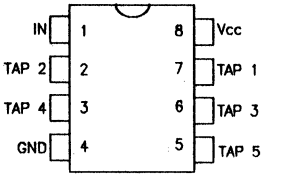
## *DS1005 14 Pin DIP*
## *DS1005M 8 Pin DIP*
## *DS1005S 16 Pin SOIC*

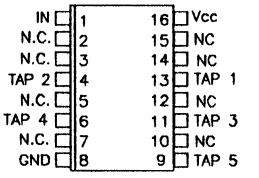
### FEATURES

- All silicon time delay
- 5 TAPS equally spaced. Delay tolerance +/- 2 ns
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Standard 14 pin DIP, 8 pin MINI-DIP, or 16 pin SOIC
- Auto-insertable
- Low power CMOS
- TTL compatible

### PIN CONNECTIONS



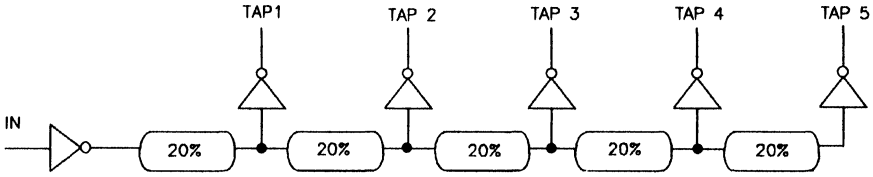

### PIN NAMES

| | |
|---|---|
| TAP 1-TAP 5 | - TAP Output Number |
| Vcc | - +5 Volts |
| GND | - Ground |
| NC | - No Connection |
| IN | - Input |

### DESCRIPTION

The DS1005 Delay Line Product Family provides five equally spaced TAPS with delays ranging from 10 ns to 500 ns, with an accuracy of +/- 2 ns. These devices are offered in a standard 14 pin DIP, compatible with existing delay line products. A space saving 8 pin MINI-DIP is also available. The 14 pin DIP, the 8 pin MINI-DIP, and SOIC packaging are available in a surface mountable "gullwing" construction. Since the DS1005 is an all silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1005 Delay Line reproduces the input logic level at each TAP after the fixed delay specified by the "dash number" in Table 1. The device is designed to produce both the leading and trailing edge delays with equal precision. Each TAP is capable of driving up to ten 74LS loads.

## FIGURE 1: LOGIC DIAGRAM




## TABLE 1 PART NUMBER DELAY TABLE ($t_{PHL}$, $t_{PLH}$)



| PART NO. | TAP 1 | TAP2 | TAP3 | TAP4 | TAP5 |
|---|---|---|---|---|---|
| DS1005-50* | 10ns | 20ns | 30ns | 40ns | 50ns |
| DS1005-60* | 12ns | 24ns | 36ns | 48ns | 60ns |
| DS1005-75* | 15ns | 30ns | 45ns | 60ns | 75ns |
| DS1005-100 | 20ns | 40ns | 60ns | 80ns | 100ns |
| DS1005-125 | 25ns | 50ns | 75ns | 100ns | 125ns |
| DS1005-150 | 30ns | 60ns | 90ns | 120ns | 150ns |
| DS1005-175 | 35ns | 70ns | 105ns | 140ns | 175ns |
| DS1005-200 | 40ns | 80ns | 120ns | 160ns | 200ns |
| DS1005-250 | 50ns | 100ns | 150ns | 200ns | 250ns |
| DS1005-500 | 100ns | 200ns | 300ns | 400ns | 500ns |

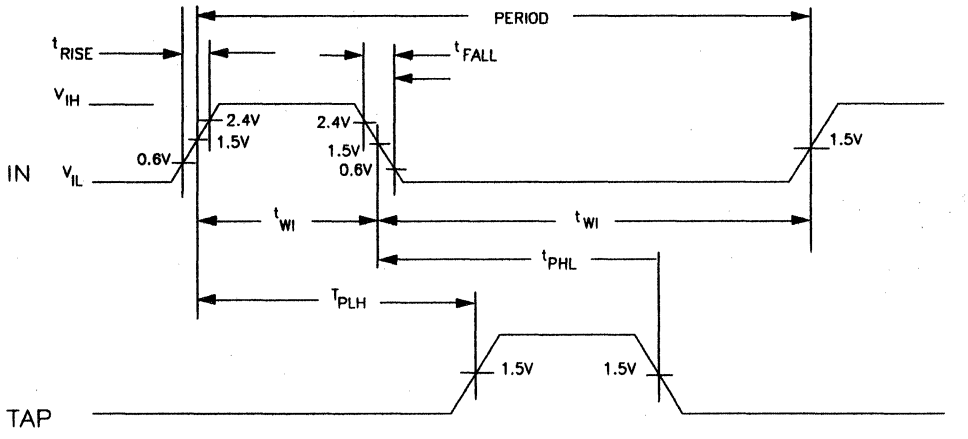
*Consult Dallas Semiconductor for availability

### ABSOLUTE MAXIMUM RATINGS*

Voltage on a pin to ground: -1.0Vto + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C
Soldering temperature: 260°C for 10 seconds
Short circuit output current: 50mA for 1 second

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**FIGURE 2: TIMING DIAGRAM- SILICON DELAY LINE**




## Terminology

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

$t_{WI}$ (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

$t_{RISE}$ (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

$t_{FALL}$ (Input Fall Time) The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

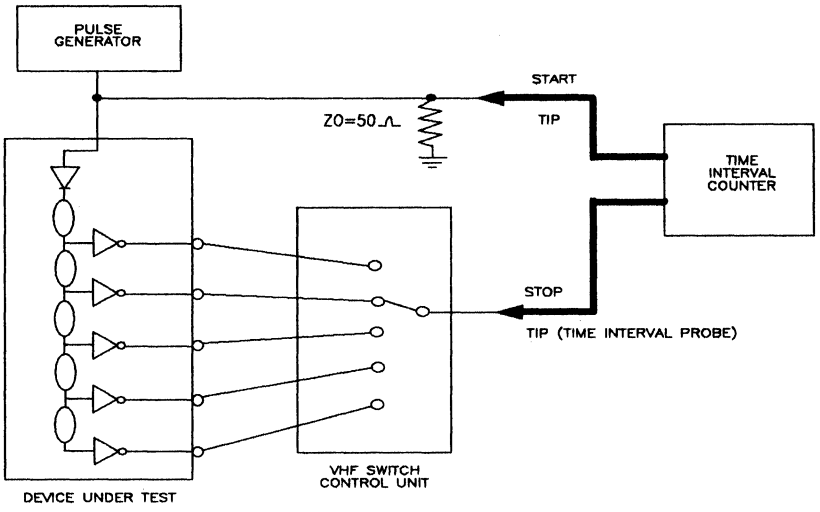
$t_{PLH}$ (Time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

$t_{PHL}$ (Time Delay, Falling) The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any TAP output pulse.

### Notes

1.) All voltages are referenced to ground.
2.) Measured with outputs open, minimum period.
3.) Vcc=5V @25°C Delays accurate on both rising and falling edges within +/- 2 ns.
4.) See Test Conditions (following page).
5.) The combination of temperature variations between 0°C and 70°C and voltage variations between 4.75 volts and 5.25 volts produce a worst case delay shift of +/- 5%.

## FIGURE 3: DALLAS SEMICONDUCTOR TEST CIRCUIT




### Test Setup Description

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1005. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit.

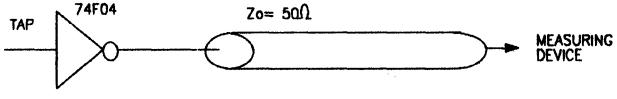
The measurement setup is calibrated by TDR (time domain reflectometry) techniques. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

### Test Conditions

**Input:**
Ambient Temperature: 25°C+/-3°C
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High = 3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50Ω Max.
Rise and FAll Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 500 ns
Period= 1us

**Note:**
Above conditions are for test only and do not restrict the operation of the device under other conditions.

**Output:**
Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.



## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5.0V +/- 5%)

| PARAMETER | SYMBOL | TEST COND. | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | Vcc | | 4.75 | 5.00 | 5.25 | V | 1 |
| High Level Input Voltage | $V_{IH}$ | | 2.2 | | 5.5 | V | 1 |
| Low Level Input Voltage | $V_{IL}$ | | -0.5 | | 0.8 | V | 1 |
| Input Leakage Current | $I_I$ | 0.0V≤ VI≤Vcc | -1.0 | | 1.0 | uA | |
| Active Current | $I_{CC}$ | Vcc= Max; Period= Min. | | 40.0 | 70.0 | mA | 2 |
| High Level Output Current | $I_{OH}$ | Vcc= Min. $V_{OH}$= 2.4V | 1.0 | | mA | | |
| Low Level Output Current | $I_{OL}$ | Vcc=Min $V_{OL}$=0.5V | 12.0 | | | mA | |

## A.C. ELECTRICAL CHARACTERISTICS

($T_A$= 25°C, Vcc=5V+/- 5%)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Pulse Width | $t_{WI}$ | 40%ofTAP5 | | | ns | |
| Input to TAP delay (leading edge) | $t_{PLH}$ | note 3 | Table 1 | note 3 | ns | 4,5 |
| Input to TAP Delay (trailing edge) | $t_{PHL}$ | note 3 | Table 1 | note 3 | ns | 4,5 |
| | Period | 4 (tWI) | | | ns | |

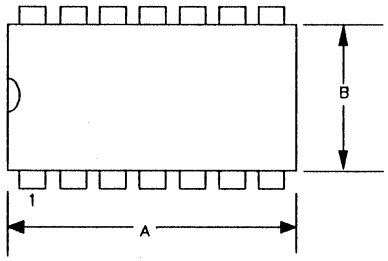
## CAPACITANCE

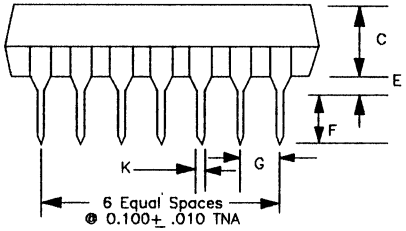
($T_A$=25°C)

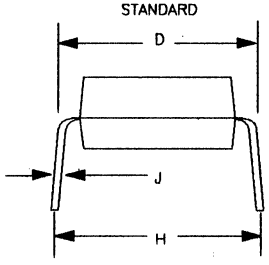
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_N$ | | 5 | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | 5 | 10 | pF | |

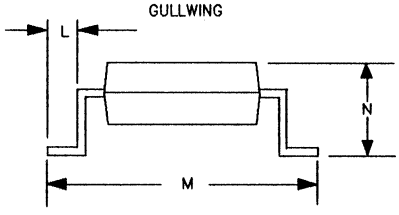
# Silicon Delay Line
# DS1005
# 14 Pin DIP

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.740 | 0.780 |
| B | 0.240 | 0.260 |
| C | 0.120 | 0.140 |
| D | 0.290 | 0.310 |
| E | 0.020 | 0.040 |
| F | 0.110 | 0.130 |
| G | 0.090 | 0.110 |
| H | 0.300 | 0.350 |
| J | 0.008 | 0.012 |
| K | 0.015 | 0.021 |
| L | 0.040 | 0.060 |
| M | 0.370 | 0.420 |
| N | 0.160 | 0.180 |



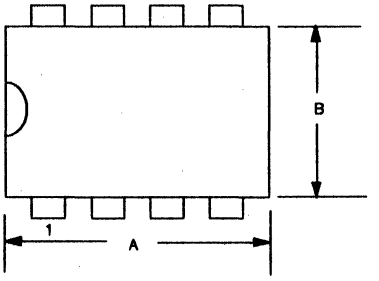



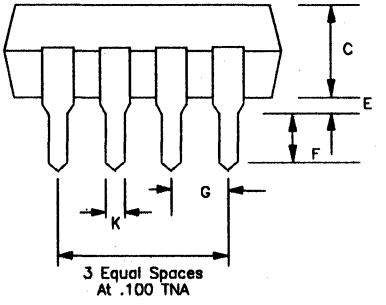



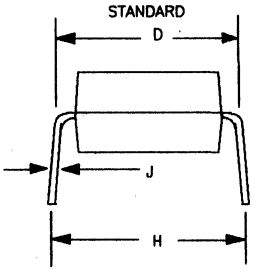



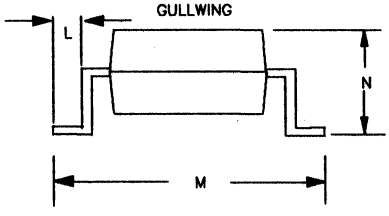
# Silicon Delay Line
# DS1005M
# 8 Pin Mini-DIP

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.360 | 0.400 |
| B | 0.240 | 0.260 |
| C | 0.120 | 0.140 |
| D | 0.290 | 0.310 |
| E | 0.020 | 0.040 |
| F | 0.110 | 0.130 |
| G | 0.090 | 0.110 |
| H | 0.300 | 0.350 |
| J | 0.008 | 0.012 |
| K | 0.015 | 0.021 |
| L | 0.040 | 0.060 |
| M | 0.370 | 0.420 |
| N | 0.160 | 0.180 |



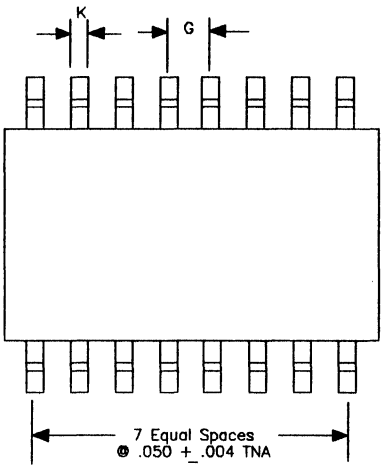



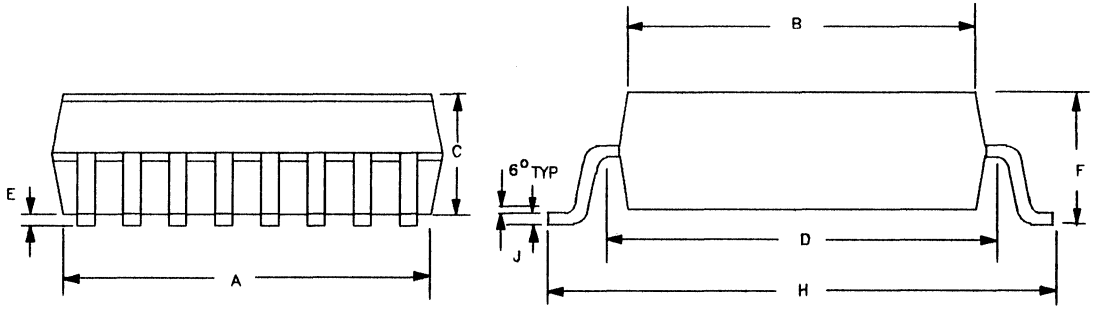



# Silicon Delay Line
# DS1005S
# 16 Pin SOIC



| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



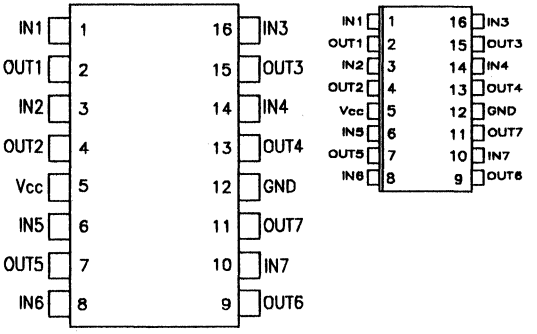
# Dallas Semiconductor
## *7 In 1 Silicon Delay Line*

# PRELIMINARY
## *DS1007 16 Pin DIP*
## *DS1007S 16 Pin SOIC*

### FEATURES

- All silicon time delay
- 7 independent logic buffered delays
- Accuracy of +/- 2 ns @ 25°C
- Four delays can be custom set between 3 ns and 7 ns
- Three delays can be custom set between 8 ns and 20 ns
- Leading edge precision
- Auto-insertable 16 pin DIP
- Surface mount 16 pin SOIC
- Low power CMOS
- TTL compatible

### PIN CONNECTIONS



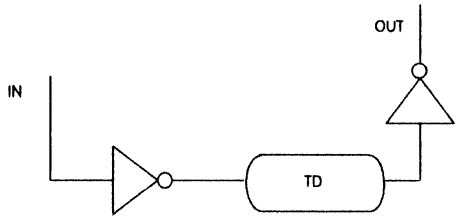

### PIN NAMES

| | |
|---|---|
| IN1 - IN7 | - Inputs |
| Out1- Out7 | - Outputs |
| GND | - Ground |
| Vcc | - +5 Volts |

### DESCRIPTION

The DS1007 Delay Line provides seven independent delay times which are set by Dallas Semiconductor to the customer's specification. The delay times can be set from 3 ns to 20 ns with an accuracy of +/- 2 ns at room temperature. The device is offered in both a 16 pin DIP and a 16 pin SOIC. Since the DS1007 is an all silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1007 reproduces the input logic level at the output after the fixed delay as specified by the customer specification.

## FIGURE 1: LOGIC DIAGRAM




INPUT PULSE WIDTH > 100% OF DELAY



## TABLE 1: PART NUMBER DELAY TABLE ($t_{PHL}$, $t_{PLH}$)

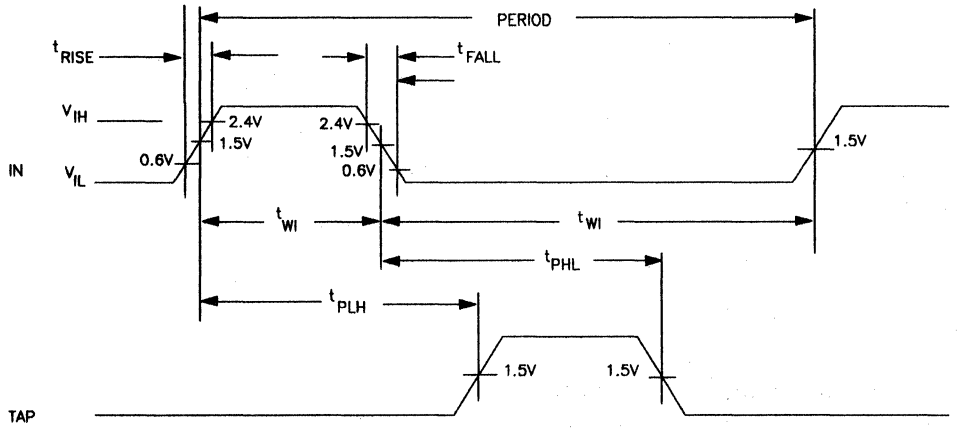
| INPUT NO. | OUTPUT DELAY |
|---|---|
| INPUT 1 | 3ns-7ns |
| INPUT 2 | 3ns-7ns |
| INPUT 3 | 3ns-7ns |
| INPUT 4 | 3ns-7ns |
| INPUT 5 | 8ns-20ns |
| INPUT 6 | 8ns-20ns |
| INPUT 7 | 8ns-20ns |

**Absolute Maximum Ratings***

Voltage on any pin to ground: -1.0Vto + 7.0V
Operating temperature: 0°C° to 70°C
Storage temperature: -55°C to + 125°C
Soldering temperature: 260°C for 10 seconds
Short circuit output current: 50mA for 1 second

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## FIGURE 2: TIMING DIAGRAM SILICON DELAY LINE




### Terminology

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

$t_{WI}$ (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

$t_{RISE}$ (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

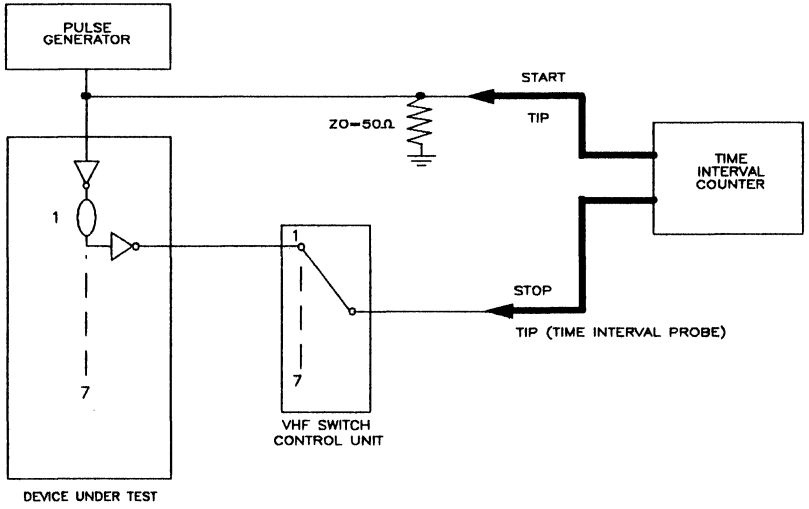
$t_{FALL}$ (Input Fall Time) The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

$t_{PLH}$ (Time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

### Notes

1.) All voltages are referenced to ground.
2.) Measured with outputs open, minimum period.
3.) Vcc=5V @25°C Delays accurate on rising edges within +/- 2 ns.
4.) See Test Conditions (following page).

## FIGURE 3: DALLAS SEMICONDUCTOR TEST CIRCUIT






### Test Setup Description

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1007. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit.

The measurement setup is calibrated by TDR (time domain reflectometry) techniques. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

### Test Conditions

**Input:**

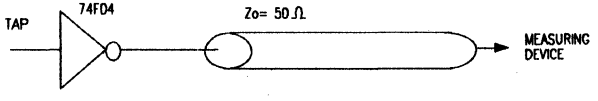
Ambient Temperature: 25°C+/-3°C
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High = 3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50 ΩMax.
Rise and FAll Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 100ns
Period= 200ns

**Note:**

Above conditions are for test only and do not restrict the operation of the device under other conditions.

**Output:**

Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising, edge.



## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5.0V+/- 5%)

| PARAMETER | SYMBOL COND. | TEST | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | Vcc | | 4.75 | 5.00 | 5.25 | V | 1 |
| High Level Input Voltage | $V_{IH}$ | | 2.2 | | 5.5 | V | 1 |
| Low Level Input Voltage | $V_{IL}$ | | -0.5 | | 0.8 | V | 1 |
| Input Leakage Current | $I_I$ | $0.0V \leq VI \leq Vcc$ | -1.0 | | 1.0 | uA | |
| Active Current | $I_{CC}$ | Vcc= Max; Period= Min. | | 40.0 | 70.0 | mA | 2 |
| High Level Output Current | $I_{OH}$ | Vcc= Min. $V_{OH}$= 2.4V | 1.0 | | | mA | |
| Low Level Output Current | $I_{OL}$ | Vcc= Min. $V_{OL}$= 0.5V | 1.0 | | | mA | |

## A.C. ELECTRICAL CHARACTERISTICS

($T_A$= 25°C, Vcc=5V+/- 5%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Pulse Width | $t_{WI}$ | 100% | | | ns | |
| Input to Output (leading edge) | $t_{PLH}$ | note 3 | | note 3 | ns | 4 |
| | Period | 3 ($t_{WI}$) | | | ns | |

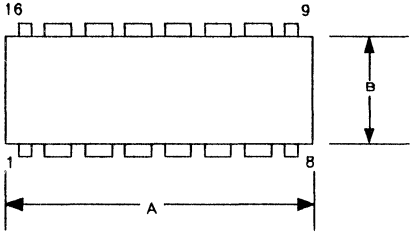
## CAPACITANCE

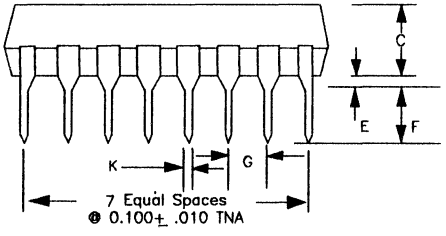
($T_A$= 25°C)

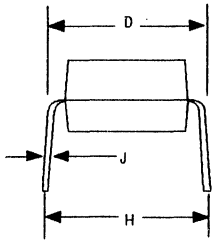
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_N$ | | 5 | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | 5 | 10 | pF | |

# SILICON DELAY LINE
# DS1007
# 16 Pin DIP

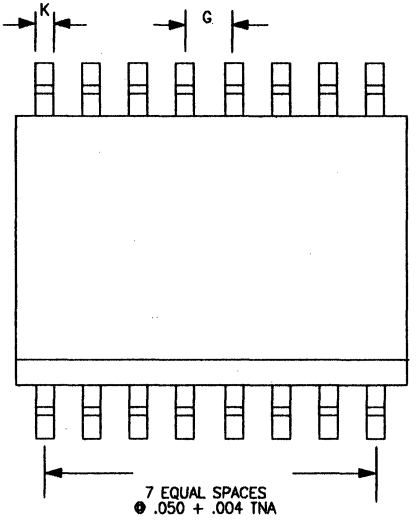
| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.740 | 0.780 |
| B | 0.240 | 0.260 |
| C | 0.120 | 0.140 |
| D | 0.290 | 0.310 |
| E | 0.020 | 0.040 |
| F | 0.110 | 0.130 |
| G | 0.090 | 0.110 |
| H | 0.300 | 0.350 |
| J | 0.008 | 0.012 |
| K | 0.015 | 0.021 |



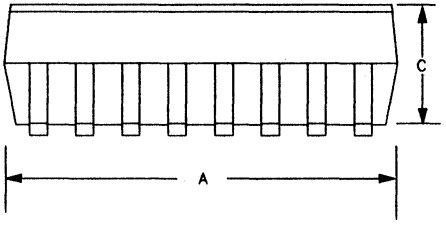



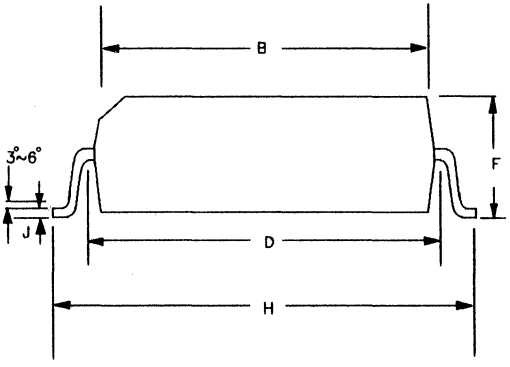



# SILICON DELAY LINE
# DS1007S
# 16 Pin SOIC




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



# Dallas Semiconductor
## *10 TAP Silicon Delay Line*

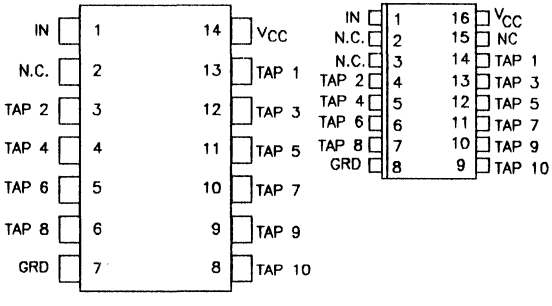
## *DS1010 14 Pin DIP*
## *DS1010S 16 Pin SOIC*



### FEATURES

- All silicon time delay 10 TAPS equally spaced
- Delays are stable and precise
- Leading and trailing edge accuracy
- Standard 14 pin DIP or 16 pin SOIC
- Delay tolerance +/- 5%
- Economical
- Auto-insertable
- Low power CMOS
- TTL compatible

### PIN CONNECTIONS




### PIN NAMES

TAP1-TAP10 - TAP Output Number
Vcc - 5 Volts
GND - Ground
NC - No Connection
IN - Input

### DESCRIPTION

The DS1010 Series Delay Line has ten equally spaced TAPS providing delays from 10 ns to 500 ns. The devices are offered in a standard 14 pin DIP which is pin compatible with hybrid delay lines. Alternatively, a 16 pin SOIC is available for surface mount technology which reduces P.C. board area. Since the DS1010 Series Delay Line is an all silicon solution, better economy is achieved when compared to older methods of using hybrid techniques.

The DS1010 Series Delay Lines provide a nominal accuracy of +/- 5% or +/- 2 ns, which ever is greater. The DS1010 Delay Line reproduces the input logic level at the output after a fixed delay as specified by the dash number extension of the part number. The DS1010 is designed to produce both leading and trailing edge with equal precision. Each TAP is capable of driving up to ten 74LS type loads.

**FIGURE 1: LOGIC DIAGRAM**

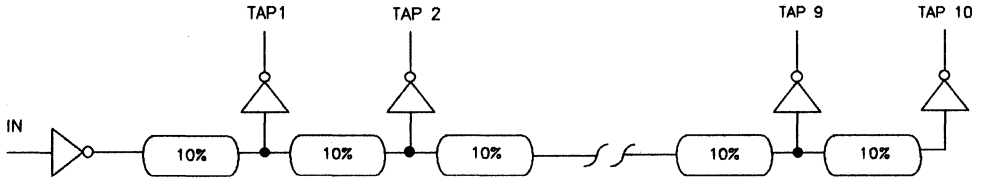


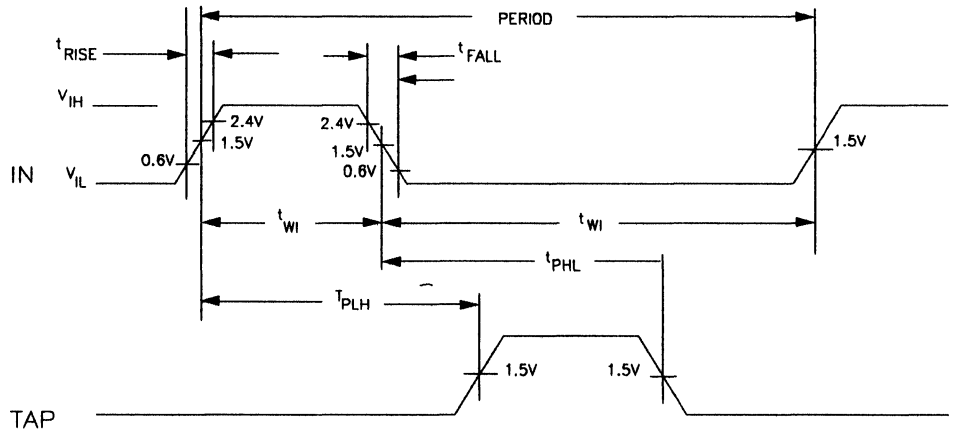

**TABLE 1: PART NUMBER DELAY TABLE ($t_{PHL}$, $t_{PLH}$)**

| CATALOG P/N | TOTAL DELAY | DELAY/TAP (NS) |
|---|---|---|
| DS1010-100 | 100 | 10 |
| DS1010-150 | 150 | 15 |
| DS1010-200 | 200 | 20 |
| DS1010-250 | 250 | 25 |
| DS1010-300 | 300 | 30 |
| DS1010-350 | 350 | 35 |
| DS1010-400 | 400 | 40 |
| DS1010-500 | 500 | 50 |

**Absolute Maximum Ratings***
Voltage on any pin
to ground: -1.0Vto + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C
Soldering
temperature: 260°C for 10 seconds
Short circuit output
current: 50mA for 1 second

*This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## FIGURE 2: TIMING DIAGRAM-SILICON DELAY LINE






### Terminology

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

$t_{WI}$ (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

$t_{RISE}$ (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

$t_{FALL}$ (Input Fall Time) The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

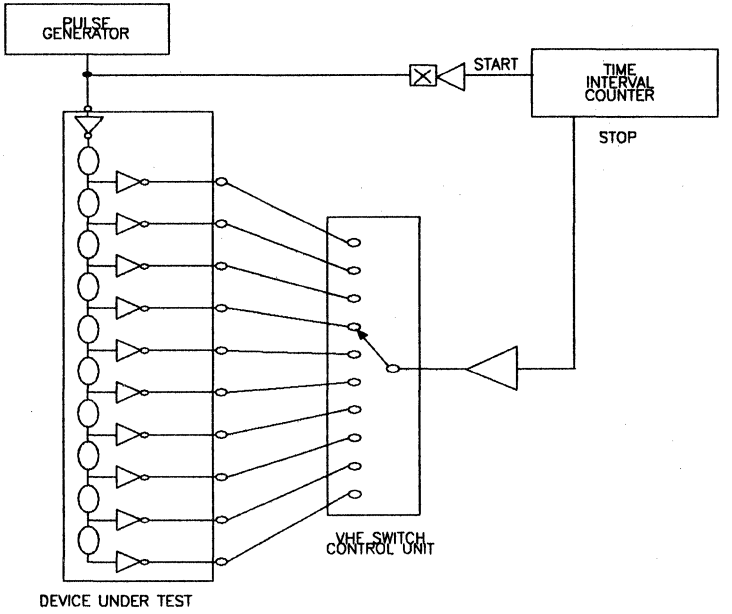
$t_{PLH}$ (Time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

$t_{PHL}$ (Time Delay, Falling) The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any TAP output pulse.

### Notes

1.) All voltages are referenced to ground.
2.) Measured with outputs open, minimum period.
3.) Vcc=5V @25°C Delays accurate on both rising and falling edges within +/- 2 ns,or 5%.
4.) See Test Conditions (following page).

**FIGURE 3: DALLAS SEMICONDUCTOR TEST CIRCUIT**




### Test Setup Description

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1010. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit.

The measurement setup is calibrated by TDR (time domain reflectometry) techniques. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

### Test Conditions

**Input:**

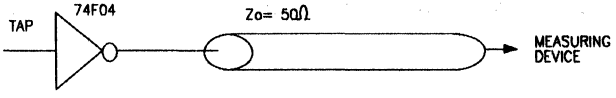
Ambient Temperature: 25°C+/-3°
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High=3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedancc: 50ΩMax.
Rise and FAll Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 500 ns
Period= 1us

**Note:**

Above conditions are for test only and do not restrict the operation of the device under other conditions.

**Output:**

Each output is loaded with a 74F04. delay is measured at the 1.5V level on the rising and falling edge.



## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc= 5.0V +/- 5%)

| PARAMETER | SYMBOL | TEST COND. | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | Vcc | | 4.75 | 5.00 | 5.25 | V | 1 |
| High Level Input Voltage | $V_{IH}$ | | 2.2 | | 5.5 | V | 1 |
| Low Level Input Voltage | $V_{IL}$ | | -0.5 | | 0.8 | V | 1 |
| Input Leakage Current | $I_L$ | $0.0V \leq V_I \leq V_{cc}$ | -1.0 | | 1.0 | uA | |
| Active Current | $I_{CC}$ | Vcc=Max: Period=Min. | | 40.0 | 75.0 | mA | 2 |
| High Level Output Current | $I_{OH}$ | Vcc=Min. $V_{OH}$=2.4V | 1.0 | | | mA | |
| Low Level Output Current | $I_{OL}$ | Vcc=Min. $V_{OL}$=0.5V | 12.0 | | | mA | |

## A.C ELECTRICAL CHARACTERISTICS

($T_A$= 25°C, Vcc= 5V +/- 5%)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Pulse Width | $t_{WI}$ | 30% of TAP 10 | | | ns | |
| Input to TAP Delay (leading edge) | $t_{PLH}$ | note 3 | Table 1 | note 3 | ns | 4 |
| Input to TAP Delay (trailing edge) | $t_{PHL}$ | note 3 | Table 1 | note 3 | ns | 4 |
| | Period | $3(t_{WI})$ | | | ns | |

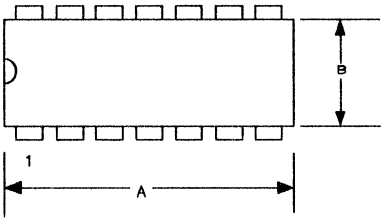
## CAPACITANCE

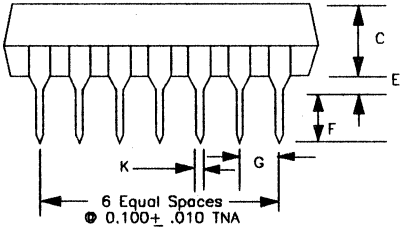
($T_A$= 25°C)

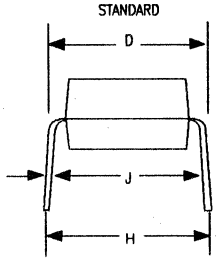
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | CIN | | 5 | 10 | pF | |
| Output Capacitance | COUT | | 5 | 10 | pF | |

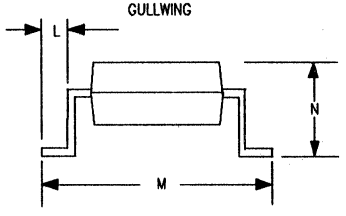
# Silicon Delay Line
# DS1010
# 14 Pin DIP

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.740 | 0.780 |
| B | 0.240 | 0.260 |
| C | 0.120 | 0.140 |
| D | 0.290 | 0.310 |
| E | 0.020 | 0.040 |
| F | 0.110 | 0.130 |
| G | 0.090 | 0.110 |
| H | 0.300 | 0.350 |
| J | 0.008 | 0.012 |
| K | 0.015 | 0.021 |
| L | 0.040 | 0.060 |
| M | 0.370 | 0.420 |
| N | 0.160 | 0.180 |

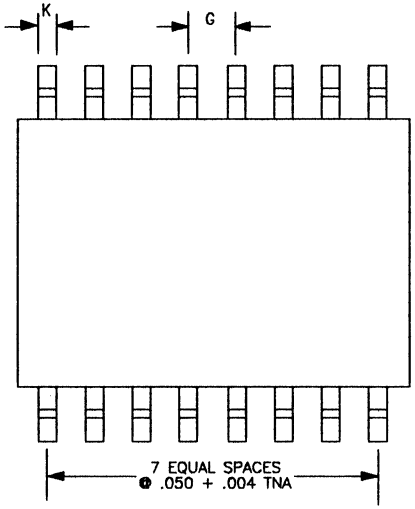


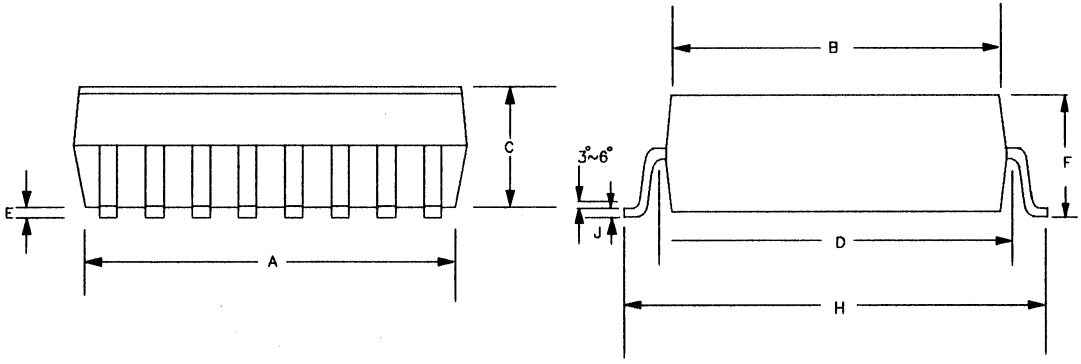



# Silicon Delay Line
# DS1010S
# 16 Pin SOIC




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



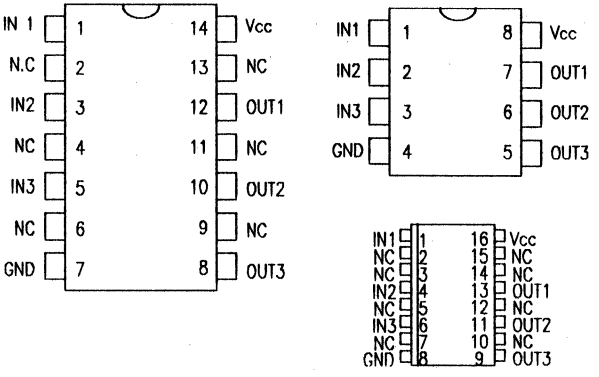
# Dallas Semiconductor
## *3 In 1 Silicon Delay Line*

## *DS1013 14 Pin DIP*
## *DS1013M 8 Pin DIP*
## *DS1013S 16 Pin SOIC*

### FEATURES

- All silicon time delay
- 3 independent logic buffered delays
- Delay tolerance +/- 2 ns
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Standard 14 pin DIP, 8 pin MINI-DIP or 16 pin SOIC
- Auto-insertable
- Low power CMOS
- TTL compatible

### PIN CONNECTIONS



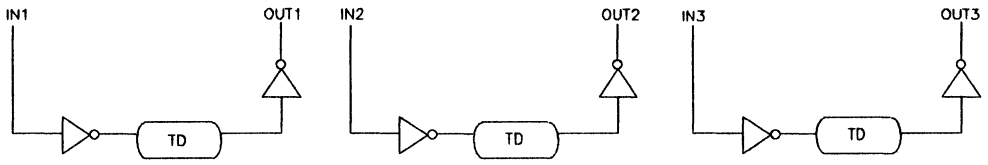

### PIN NAMES

| | |
|---|---|
| IN1, IN2, IN3 | - Inputs |
| Out1, Out2, Out3 | - Outputs |
| GND | - Ground |
| Vcc | - +5 Volts |

### DESCRIPTION

The DS1013 Series of Delay Lines has three independent logic buffered delays in a single package. The devices are offered in a standard 14 pin DIP which is pin compatible with hybrid delay lines. Alternatively 8 pin MINI-DIPS and surface mount packages are available which saves P.C. board area. Since the DS1013 Series is an all silicon solution, better economy is achieved when compared to older methods of using hybrid techniques. The DS1013 Series Delay Lines provide a nominal accuracy of +/- 2 ns for delay times ranging from 10 ns to 100 ns. The DS1013 Delay line reproduces the input logic level at the output after a fixed delay as specified by the dash number extension of the part number. The DS1013 is designed to reproduce both leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS type loads.

## FIGURE 1: LOGIC DIAGRAM





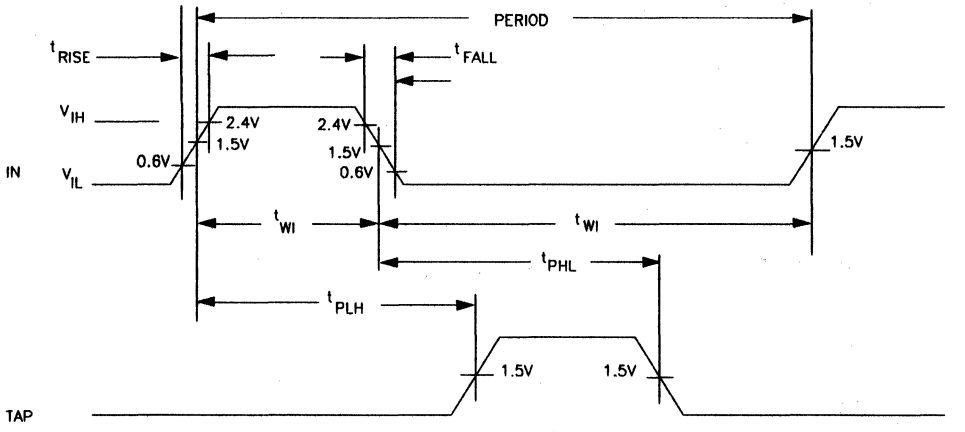

## TABLE 1: PART NUMBER DELAY TABLE ($T_{PHL}$, $T_{PLH}$)

| PART NO. | DELAY PER OUTPUT (ns) |
|---|---|
| DS1013-10 | 10/10/10 |
| DS1013-15 | 15/15/15 |
| DS1013-20 | 20/20/20 |
| DS1013-25 | 25/25/25 |
| DS1013-30 | 30/30/30 |
| DS1013-40 | 40/40/40 |
| DS1013-50 | 50/50/50 |
| DS1013-60 | 60/60/60 |
| DS1013-70 | 70/70/70 |
| DS1013-75 | 75/75/75 |
| DS1013-80 | 80/80/80 |
| DS1013-90 | 90/90/90 |
| DS1013-100 | 100/100/100 |

**Absolute Maximum Ratings***
Voltage on any pin
to ground: -1.0Vto + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C
Soldering
temperature: 260°C for 10 seconds
Short circuit output
current: 50mA for 1 second

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**FIGURE 2: TIMING DIAGRAM-SILICON DELAY LINE**




## Terminology

Period The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

$t_{WI}$ (Pulse Width) The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

$t_{RISE}$ (Input Rise Time) The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

$t_{FALL}$ (Input Fall Time) The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

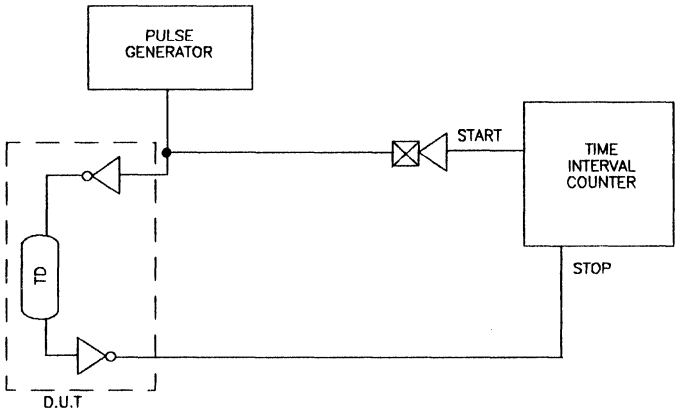
$t_{PLH}$ (time Delay, Rising) The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

$t_{PHL}$ (Time Delay, Falling) The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any TAP output pulse.

## Notes

1.) All voltages are referenced to ground.
2.) Measured with outputs open, minimum period
3.) Vcc=5V @25°C Delays accurate on both rising and falling edges within +/- 2 ns.
4.) See Test Conditions (following page).
5.) The combination of temperature variations between 0° C and 70° C and voltage variations between 4.75 volts and 5.25 volts produce a worst case delay shift of +/- 5%.

## FIGURE 3: DALLAS SEMICONDUCTOR TEST CIRCUIT






### Test Setup Description

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1013. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each TAP. Each TAP is selected and connected to the counter by a VHF switch control unit.

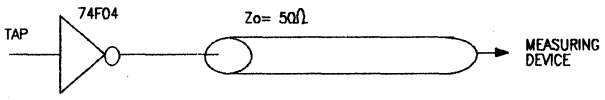
The measurement setup is calibrated by TDR (time domain reflectometry) techniques. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

### Test Conditions

**Input:**
Ambient Temperature: 25°C+/-3°C
Supply Voltage (Vcc): 5.0V+/-0.1V
Input Pulse: High = 3.0V+/-0.1V
Low = 0.0V+/-0.1V
Source Impedance: 50Ω Max.
Rise and Fall Time: 3.0 ns Max.
(measured between 0.6V and 2.4V)
Pulse Width = 500 ns
Period= 1us

**Note:**
Above conditions are for test only and do not restrict the operation of the device under other conditions.

**Output:**
Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.



## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc= 5.0V+/- 5%)

| PARAMETER | SYMBOL | TEST COND. | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 4.75 | 5.00 | 5.25 | V | 1 |
| High Level Input Voltage | $V_{IH}$ | | 2.2 | | 5.5 | V | 1 |
| Low Level Input Voltage | $V_{IL}$ | | -0.5 | | 0.8 | V | 1 |
| Input Leakage Current | $I_I$ | $0.0V \leq V_I \leq V_{CC}$ | -1.0 | | 1.0 | uA | |
| Active Current | $I_{CC}$ | $V_{CC}$= Max Period= Min. | | 40 | 70 | mA | 2 |
| High Level Output Current | $I_{OH}$ | $V_{CC}$= Min. $V_{OH}$= 2.4V | 1.0 | | | mA | |
| Low Level Output Current | $I_{OL}$ | $V_{CC}$=Min $V_{OL}$=0.5V | 12.0 | | | mA | |

## A.C ELECTRICAL CHARACTERISTICS

($T_A$= 25°C, Vcc=5.0V+/-5%)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Pulse Width | $t_{WI}$ | 100% | $t_{PLH}$ | | ns | |
| Input to TAP Delay (leading edge) | $t_{PLH}$ | note 3 | Table 1 | note 3 | ns | 4,5 |
| Input to TAP Delay (trailing edge) | $t_{PHL}$ | note 3 | Table 1 | note 3 | ns | 4,5 |
| | Period | $3(t_{WI})$ | | | ns | |

## CAPACITANCE

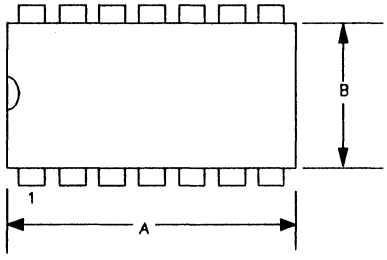
($t_A$=25°C)

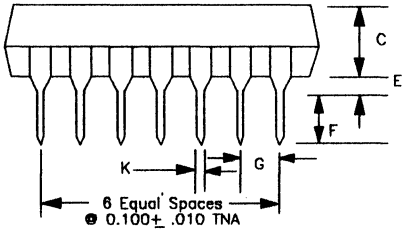
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | 5 | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | 5 | 10 | pF | |

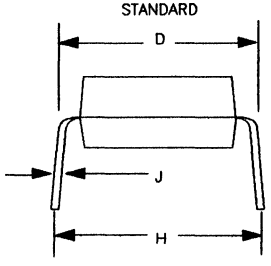
# Silicon Delay Line
# DS1013
# 14 Pin DIP

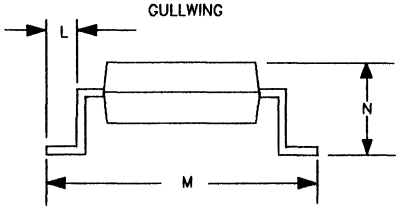


| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.740 | 0.780 |
| B | 0.240 | 0.260 |
| C | 0.120 | 0.140 |
| D | 0.290 | 0.310 |
| E | 0.020 | 0.040 |
| F | 0.110 | 0.130 |
| G | 0.090 | 0.110 |
| H | 0.300 | 0.350 |
| J | 0.008 | 0.012 |
| K | 0.015 | 0.021 |
| L | 0.040 | 0.060 |
| M | 0.370 | 0.420 |
| N | 0.160 | 0.180 |

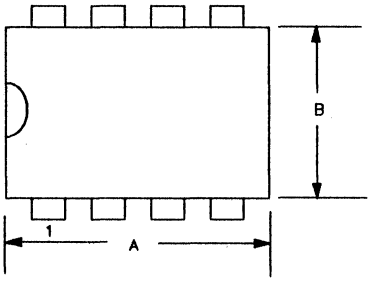


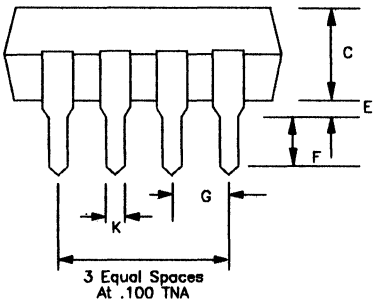



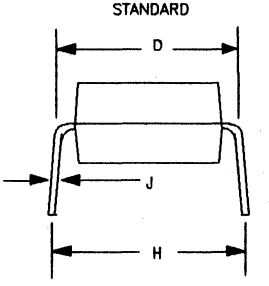



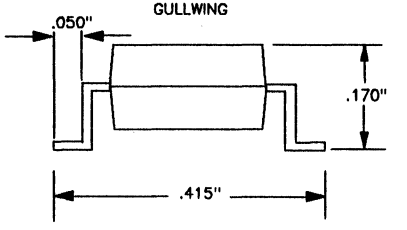
# Silicon Delay Line
# DS1013M
# 8 Pin DIP




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .360 | .400 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |

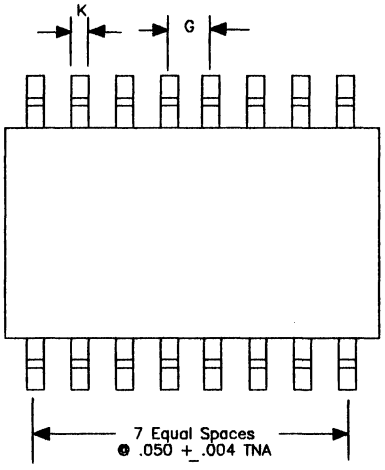


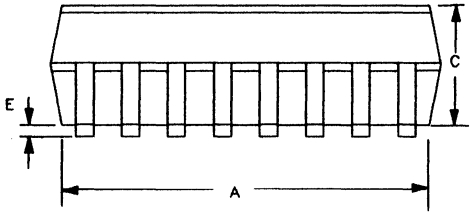



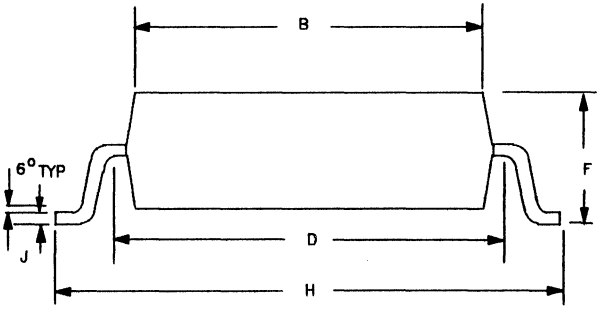



# Silicon Delay Line
# DS1013S
# 16 Pin SOIC

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



# Dallas Semiconductor
## *Constant Density Data Separator*

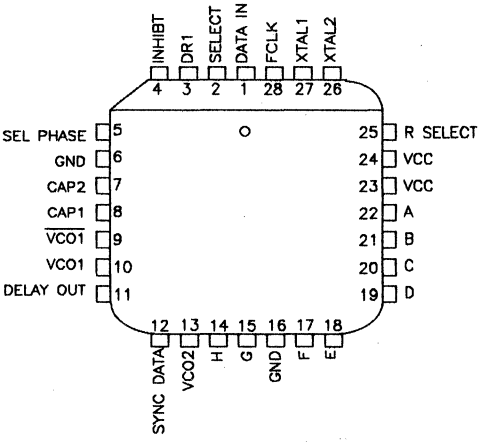
**PRODUCT PREVIEW**
***DS1015***

### FEATURES
- Synthesizes data and clock for constant density data recording
- Two independent voltage controlled oscillators
- Digitally controlled frequency synthesized delay line
- High resolution frequency synthesized VCO
- Programmable phase - frequency detector with full 20 MHZ dynamic range VCO
- High speed balanced charge pump
- Zero phase startup provides fast and predictable lock acquistion
- Integrated crystal oscillator
- Multiple voltage supply pins for isolation of frequency sensitive inputs and digital outputs
- +5 volt operation
- Low power CMOS
- TTL compatable
- Surface mount PLCC

### DESCRIPTION
The DS1015 constant density data separator performs data synchronization of encoded data from rotating media. The DS1015 contains a high performance phase-frequency synthesizer for read data synchronization and a digital controlled frequency which is used to set the amount of delay time of a variable delay line. The combination of these elements produce a precisely timed data and clock signal at the output of the self adjusting data separator.

The DS1015 uses advanced CMOS circuits and design techniques to produce the precise timing syncronization required while operating from a single +5 volt supply at extremely low power consumption. The DS1015 is available in a 28 pin PLCC package.

### PIN CONNECTIONS




### PIN NAMES
Vcc = +5 volts
GND = Ground
A - H = Digital Frequency Control Inputs
R SELECT = Digital Frequency Control Enable
XTAL1 = Crystal Oscillator Input
XTAL2 = Crystal Oscillator Output
INHIBIT = Phase Detector Inhibit
VCO1 = Voltage Controlled Oscillator 1 Output
$\overline{\text{VCO1}}$ = Voltage Controlled Oscillator 1 $\overline{\text{Output}}$
VCO2 = Voltage Controlled Oscillator 2 Output
FCLK = Clock Frequency Input
DATA IN = Data Input
SELECT = Select Data or FCLK
SEL PHASE = Select VCO1 or $\overline{\text{VCO1}}$
CAP1 = VCO1 Filter
DR1 = VCO1 Dynamic Range Adjustmnt
SYNC DATA = Syncrnized Data Output
DELAY OUT = Delay Line Output
CAP2 = VCO2 Filter

# Multiport Memory

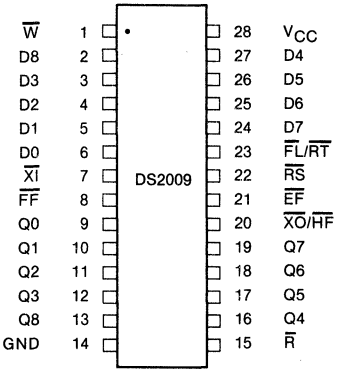
# Dallas Semiconductor
## 512 x 9 FIFO

## DS2009

### FEATURES

- First-in, first-out memory based architecture
- Flexible 512 x 9 organization
- Low power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35ns, 50ns, 65ns and 80ns access times
- Industrial temperature range −40°C to +85°C available designated IND

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $\overline{W}$ | - WRITE |
| $\overline{R}$ | - READ |
| $\overline{RS}$ | - RESET |
| $\overline{FL}/\overline{RT}$ | - First Load/Retransmit |
| $D_{0-8}$ | - Data In |
| $Q_{0-8}$ | - Data Out |
| $\overline{XI}$ | - Expansion In |
| $\overline{XO}/\overline{HF}$ | - Expansion Out/Half Full |
| $\overline{FF}$ | - Full Flag |
| $\overline{EF}$ | - Empty Flag |
| $V_{CC}$ | - 5 Volts |
| GND | - Ground |

### DESCRIPTION

The DS2009 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The DS2009 is functionally and electrically equivalent to the DS2011 2K x 9 FIFO with the following exceptions: active current ($I_{CC1}$) is 80 mA max except for 35ns device which is 100 mA max and power-down current ($I_{CC3}$) is 500 *u*A max. Refer to the DS2011 data sheet for detailed device description.

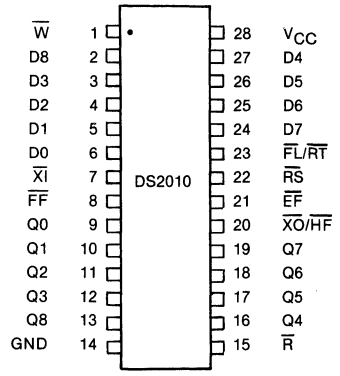
# Dallas Semiconductor
## *1024 x 9 FIFO*

## *DS2010*

### FEATURES

- First-in, first-out memory based architecture
- Flexible 1024 x 9 organization
- Low power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35ns, 50ns, 65ns and 80ns access times
- Industrial temperature range −40°C to +85°C available designated IND

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $\overline{W}$ | - WRITE |
| $\overline{R}$ | - READ |
| $\overline{RS}$ | - RESET |
| $\overline{FL}/\overline{RT}$ | - First Load/Retransmit |
| $D_{0-8}$ | - Data In |
| $Q_{0-8}$ | - Data Out |
| $\overline{XI}$ | - Expansion In |
| $\overline{XO}/\overline{HF}$ | - Expansion Out/Half Full |
| $\overline{FF}$ | - Full Flag |
| $\overline{EF}$ | - Empty Flag |
| $V_{CC}$ | - 5 Volts |
| GND | - Ground |

### DESCRIPTION

The DS2010 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The DS2010 is functionally and electrically equivalent to the DS2011 2K x 9 FIFO with the following exception: power-down current ($I_{CC3}$) is 1 mA max. Refer to the DS2011 data sheet for detailed device description.

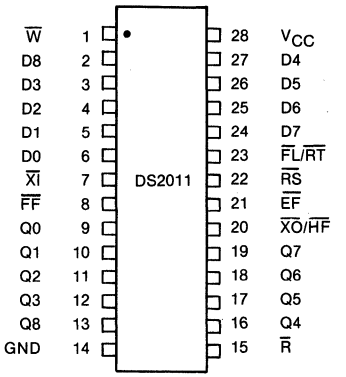
# Dallas Semiconductor
## *2048 x 9 FIFO*

## *DS2011*

### FEATURES

- First-in, first-out memory based architecture
- Flexible 2048 x 9 organization
- Low power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35ns, 50ns, 65ns and 80ns access times
- Industrial temperature range −40°C to +85°C available designated IND

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $\overline{W}$ | - WRITE |
| $\overline{R}$ | - READ |
| $\overline{RS}$ | - RESET |
| $\overline{FL/RT}$ | - First Load/Retransmit |
| $D_{0-8}$ | - Data In |
| $Q_{0-8}$ | - Data Out |
| $\overline{XI}$ | - Expansion In |
| $\overline{XO/HF}$ | - Expansion Out/Half Full |
| $\overline{FF}$ | - Full Flag |
| $\overline{EF}$ | - Empty Flag |
| $V_{CC}$ | - 5 Volts |
| GND | - Ground |

### DESCRIPTION

The DS2011 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The main application of the DS2011 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the WRITEs and READs are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

## OPERATION

Unlike conventional shift register based FIFOs, the DS2011 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the DS2011 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

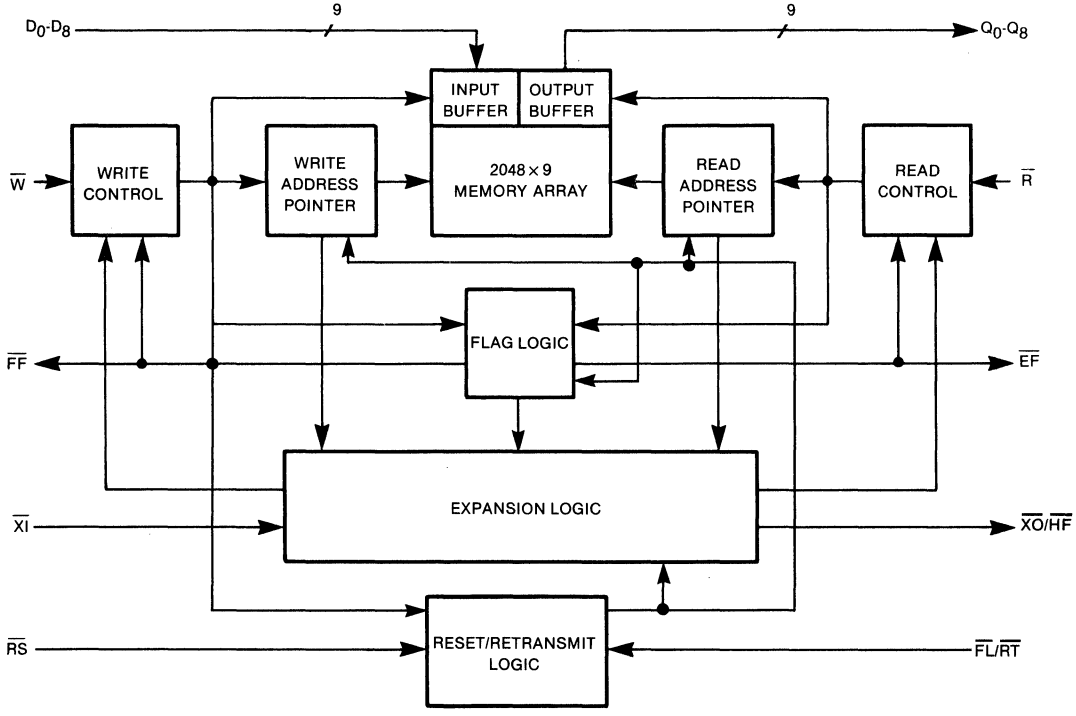
Address pointers automatically loop back to address zero after reaching address 2047. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.



Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2011 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2011 allows connecting the read, write, data in, and data out lines of the DS2011 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins, as appropriate (see the Expansion Timing section for a more complete discussion).

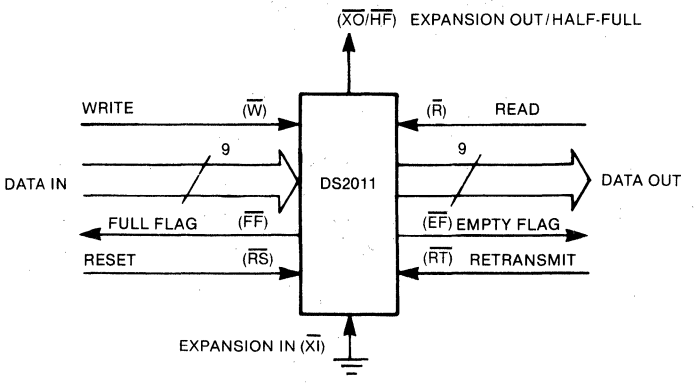
## BLOCK DIAGRAM Figure 1



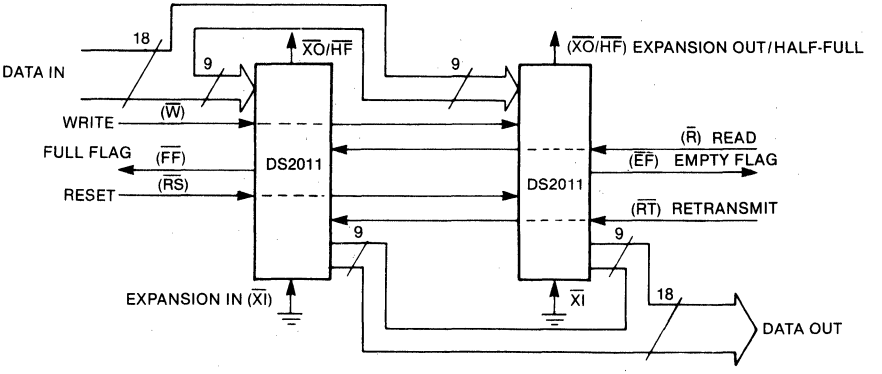
**SINGLE DEVICE CONFIGURATION**
A single DS2011 may be used when application requirements are for 2048 words or less. The DS2011 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 2).

**WIDTH EXPANSION**
Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 3 demonstrates an 18-bit word width by using two DS2011s. Any word width can be attained by adding additional DS2011s.

**A SINGLE 2048 x 9 FIFO CONFIGURATION** Figure 2




**A 2048 x 18 FIFO CONFIGURATION (WIDTH EXPANSION)** Figure 3




**NOTE:**
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

## DEPTH EXPANSION (DAISY CHAIN)

The DS2011 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 4 demonstrates Depth Expansion using three DS2011s. Any depth can be attained by adding additional DS2011s.

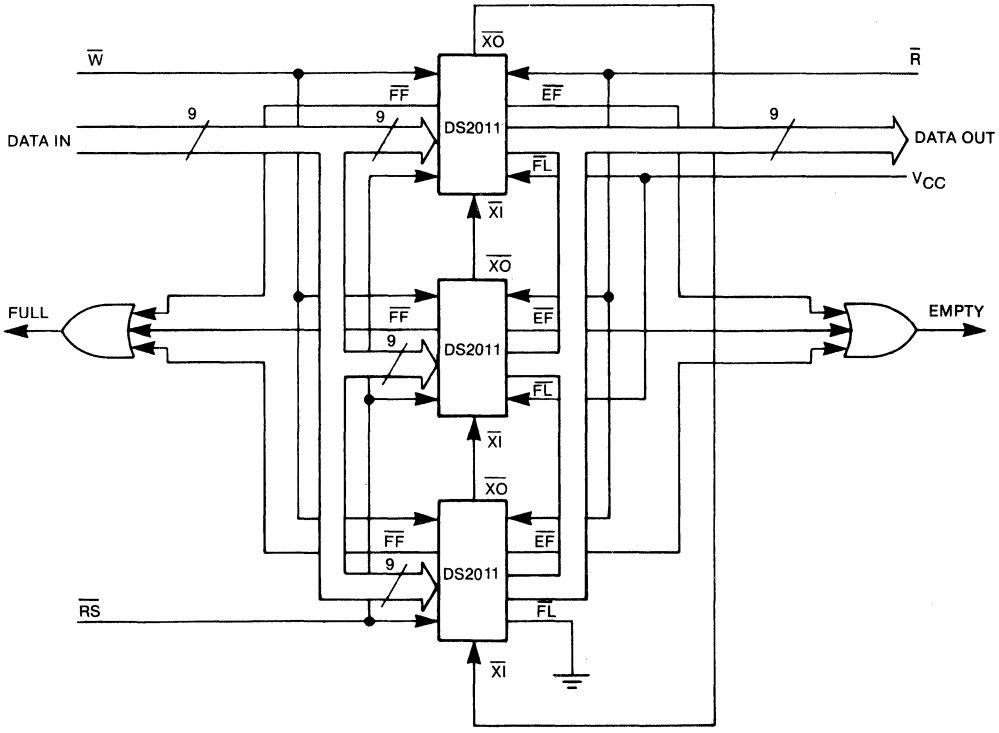
External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The DS2011 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The half-full capability is not allowed in depth expansion.



**A 6144 x 9 FIFO CONFIGURATION (DEPTH EXPANSION)** Figure 4



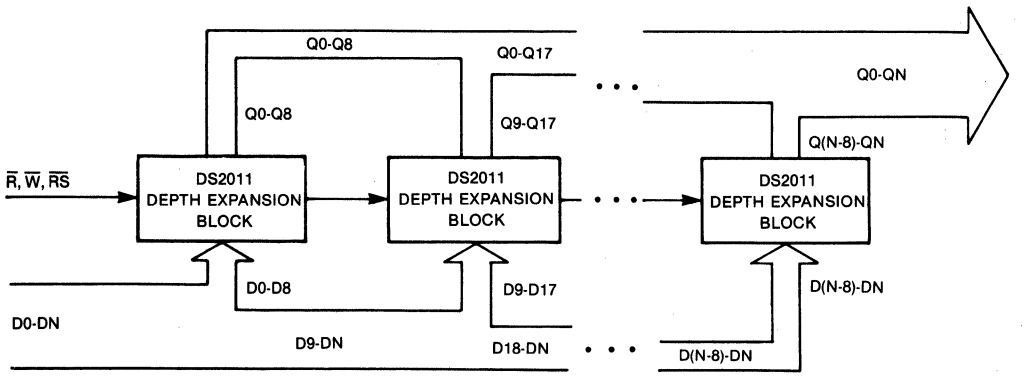
## COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

## BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing DS2011s, as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

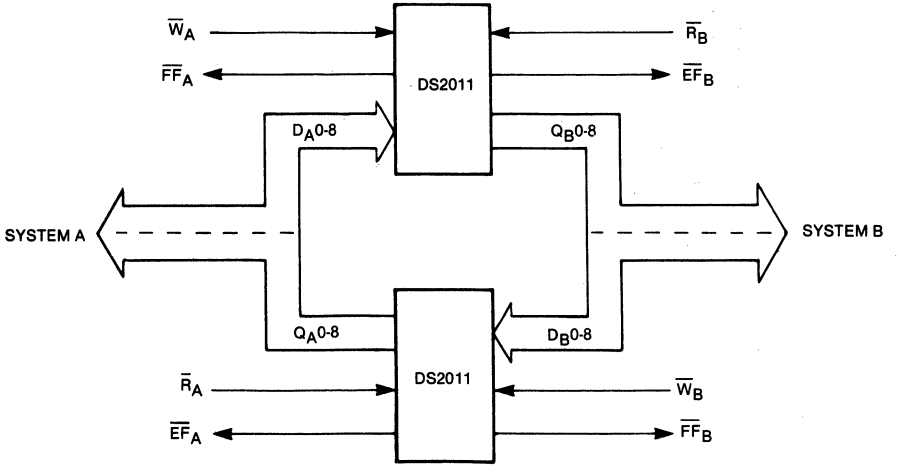
**COMPOUND FIFO EXPANSION** Figure 5




**NOTES:**

1. For depth expansion block see DEPTH EXPANSION section and Figure 4.
2. For flag operation see WIDTH EXPANSION section and Figure 3.

**BIDIRECTIONAL FIFO APPLICATION** Figure 6



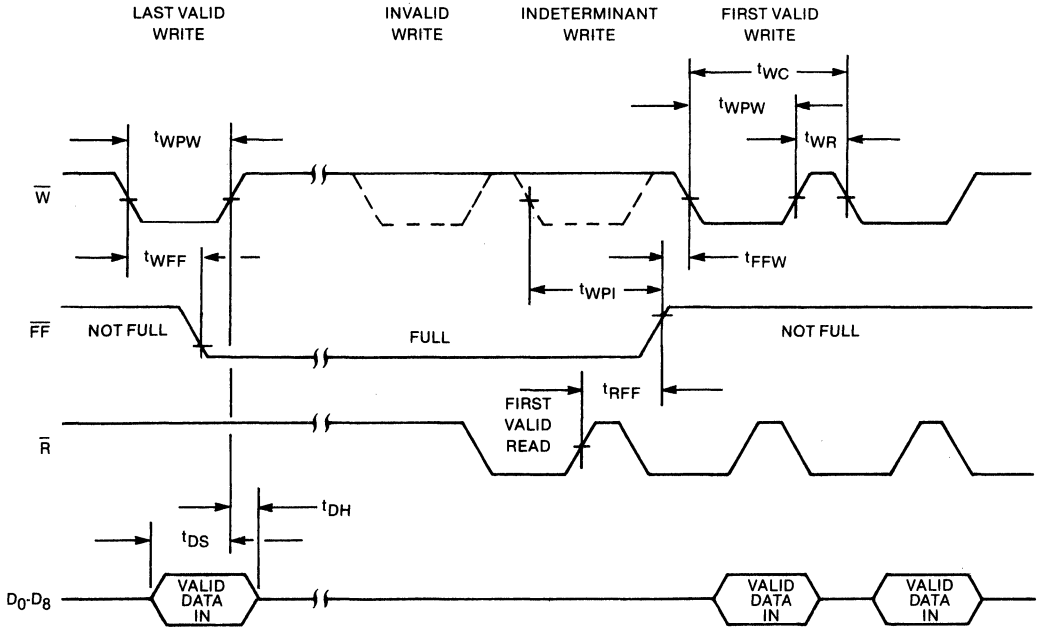
## HALF-FULL CAPABILITY

In the single-device and width-expansion modes, the $\overline{XO}/\overline{HF}$ output acts as an indication of a half-full memory. ($\overline{XI}$ must be tied low.) After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain low until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset (forced high) by the rising edge of the read operation.

## WRITE MODE

The DS2011 initiates a Write Cycle (see Figure 7) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the DS2011 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high $t_{RFF}$ after completion of a valid READ operation. Writes beginning after $\overline{FF}$ goes low and more than $t_{WPI}$ before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than $t_{WPI}$ before $\overline{FF}$ goes high and less than $t_{FFW}$ later may or may not occur (be valid), depending on internal flag status.

**WRITE AND FULL FLAG TIMING** Figure 7



**WRITE A.C. ELECTRICAL CHARACTERISTICS** (0 °C to +70 °C, $V_{CC}$ = 5.0V ± 10%)

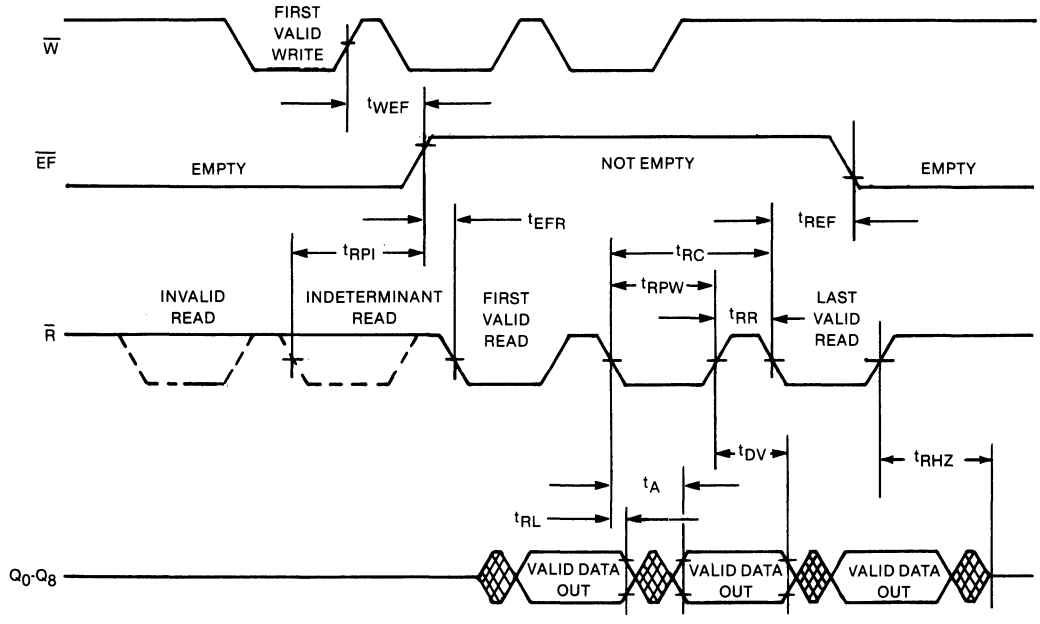
| | | DS2011-35 | | DS2011-50 | | DS2011-65 | | DS2011-80 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Write Cycle Time | $t_{WC}$ | 45 | | 65 | | 80 | | 100 | | ns | |
| Write Pulse Width | $t_{WPW}$ | 35 | | 50 | | 65 | | 80 | | ns | 1 |
| Write Recovery Time | $t_{WR}$ | 10 | | 15 | | 15 | | 20 | | ns | |
| Data Set Up Time | $t_{DS}$ | 15 | | 20 | | 25 | | 30 | | ns | |
| Data Hold Time | $t_{DH}$ | 5 | | 5 | | 10 | | 10 | | ns | |
| $\overline{W}$ Low to $\overline{FF}$ Low | $t_{WFF}$ | | 30 | | 45 | | 60 | | 70 | ns | 2 |
| $\overline{FF}$ High to Valid Write | $t_{FFW}$ | | 5 | | 5 | | 10 | | 10 | ns | 2 |
| $\overline{R}$ High to $\overline{FF}$ High | $t_{RFF}$ | | 30 | | 45 | | 60 | | 70 | ns | 2 |
| Write Protect Indeterminant | $t_{WPI}$ | | 15 | | 20 | | 25 | | 25 | ns | 2 |

**READ MODE**

The DS2011 initiates a Read Cycle (see Figure 8) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the DS2011 provides a fast access to data from 9 of 18,432 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high $t_{WEF}$ after completion of a valid Write operation. Reads beginning $t_{EFR}$ after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than $t_{RPI}$ before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than $t_{RPI}$ before $\overline{EF}$ goes high and less than $t_{EFR}$ later may or may not occur (be valid) depending on internal flag status.

**READ AND EMPTY FLAG TIMING** Figure 8



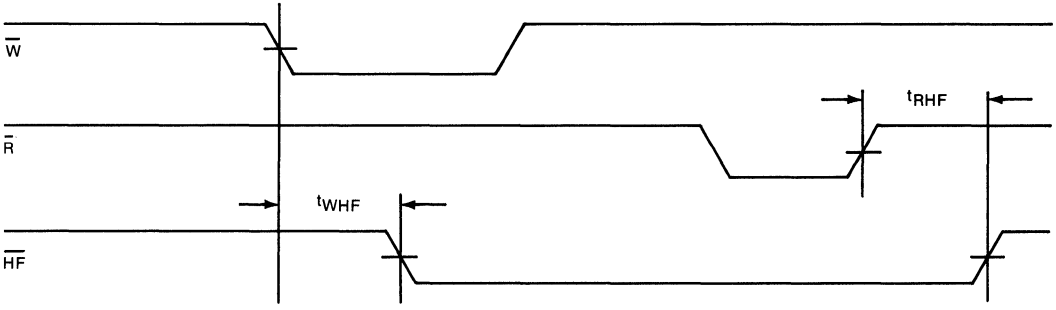
**READ A.C. ELECTRICAL CHARACTERISTICS** (0 °C to +70 °C, $V_{CC}$ = 5.0V ± 10%)

| | | DS2011-35 | | DS2011-50 | | DS2011-65 | | DS2011-80 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Read Cycle Time | $t_{RC}$ | 45 | | 65 | | 80 | | 100 | | ns | |
| Access Time | $t_A$ | | 35 | | 50 | | 65 | | 80 | ns | 2 |
| Read Recovery Time | $t_{RR}$ | 10 | | 15 | | 15 | | 20 | | ns | |
| Read Pulse Width | $t_{RPW}$ | 35 | | 50 | | 65 | | 80 | | ns | 1 |
| $\overline{R}$ Low to Low Z | $t_{RL}$ | 5 | | 10 | | 10 | | 10 | | ns | 2 |
| Data Valid from $\overline{R}$ High | $t_{DV}$ | 5 | | 5 | | 5 | | 5 | | ns | 2 |
| $\overline{R}$ High to High Z | $t_{RHZ}$ | | 20 | | 25 | | 25 | | 25 | ns | 2 |
| $\overline{R}$ Low to $\overline{EF}$ Low | $t_{REF}$ | | 30 | | 45 | | 60 | | 70 | ns | 2 |
| $\overline{EF}$ High to Valid Read | $t_{EFR}$ | | 5 | | 5 | | 10 | | 10 | ns | 2 |
| $\overline{W}$ High to $\overline{EF}$ High | $t_{WEF}$ | | 30 | | 45 | | 60 | | 70 | ns | 2 |
| Read Protect Indeterminant | $t_{RPI}$ | | 15 | | 20 | | 25 | | 25 | ns | 2 |

## HALF-FULL MODE

Unlike the Full Flag and Empty Flag, the Half-Full Flag does not prevent device reads and writes. The flag is set by the next falling edge of write when the memory is 1024 locations full. The flag will remain set until the memory is less than or equal to 1024 locations full. The read operation (rising edge), which results in the memory being 1024 locations full, removes the flag.

**HALF-FULL FLAG TIMING** Figure 9




**HALF-FULL FLAG A.C. CHARACTERISTICS** (0°C to +70°C, $V_{CC}$ = 5.0V ± 10%)

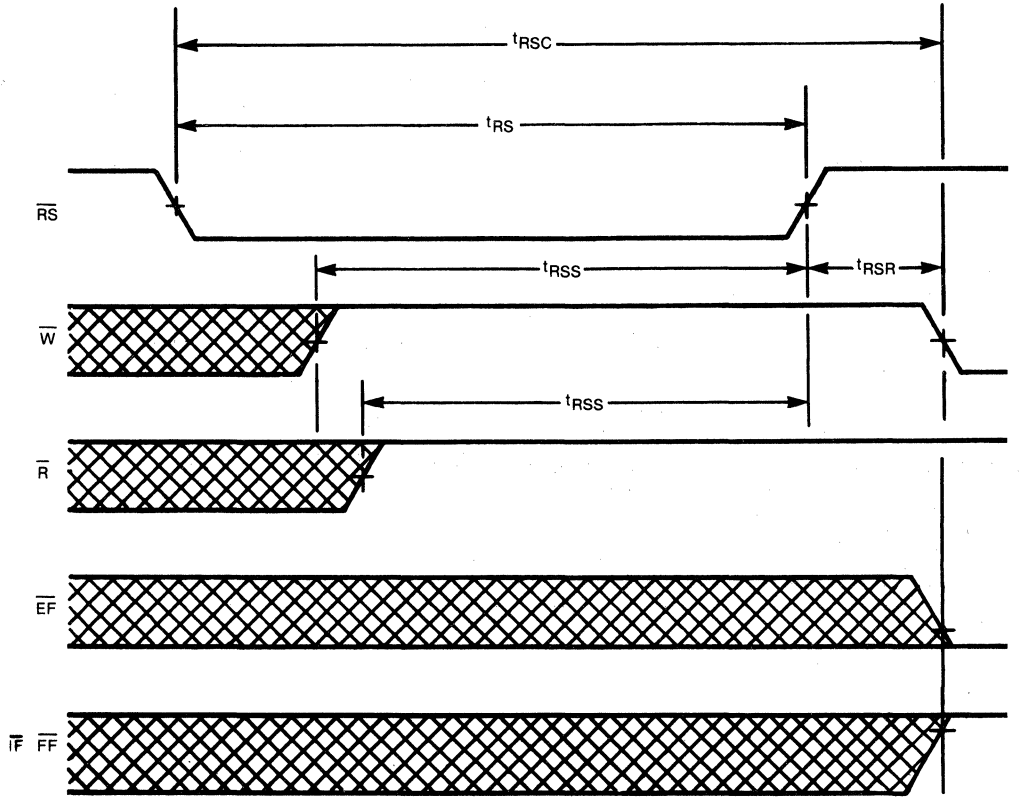
| | | DS2011-35 | | DS2011-50 | | DS2011-65 | | DS2011-80 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Write Low to Half-Full Flag Low | $t_{WHF}$ | | 45 | | 65 | | 80 | | 100 | ns | |
| Read High to Half-Full Flag High | $t_{RHF}$ | | 45 | | 65 | | 80 | | 100 | ns | |

## RESET

The DS2011 is reset (see Figure 10) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after a power up, before a Write operation can begin.

Although neither $\overline{W}$ nor $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high $t_{RSS}$ before $\overline{RS}$ goes high, and must remain high $t_{RSR}$ afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

**RESET** Figure 10




**NOTE:**
$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at $t_{RSC}$.

**RESET A.C. ELECTRICAL CHARACTERISTICS** (0°C to +70°C, $V_{CC}$ = 5.0V ± 10%)

| | | DS2011-35 | | DS2011-50 | | DS2011-65 | | DS2011-80 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Reset Cycle Time | $t_{RSC}$ | 45 | | 65 | | 80 | | 100 | | ns | |
| Reset Pulse Width | $t_{RS}$ | 35 | | 50 | | 65 | | 80 | | ns | 1 |
| Reset Recovery Time | $t_{RSR}$ | 10 | | 15 | | 15 | | 20 | | ns | |
| Reset Set Up Time | $t_{RSS}$ | 30 | | 40 | | 50 | | 60 | | ns | |

3

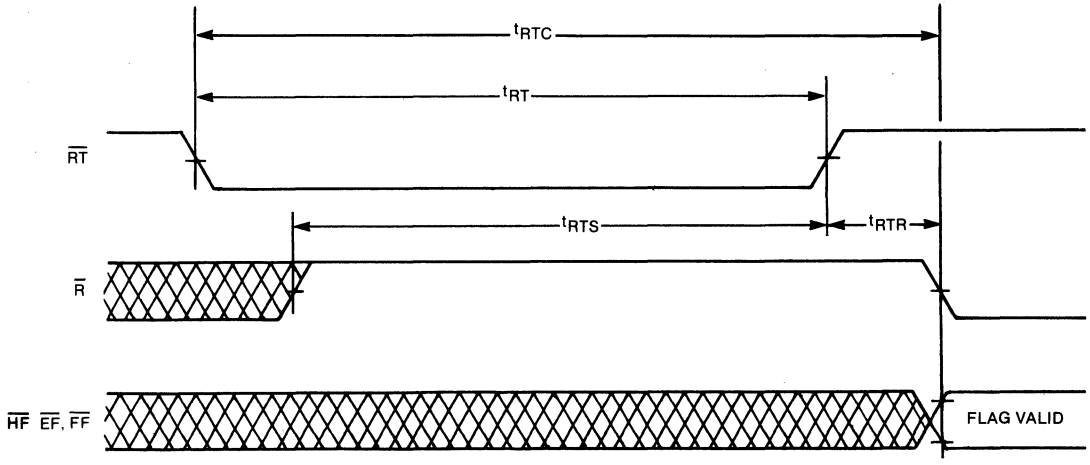
**RETRANSMIT**

The DS2011 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 11).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive $t_{RTS}$ before $\overline{RT}$ goes high, and must remain high for $t_{RTR}$ afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

**RETRANSMIT** Figure 11




**NOTE:**

$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at $t_{RTC}$.

## RETRANSMIT
## A.C. ELECTRICAL CHARACTERISTICS

(0 °C to +70 °C, $V_{CC}$ = 5.0V ± 10%)

| | | DS2011-35 | | DS2011-50 | | DS2011-65 | | DS2011-80 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Retransmit Cycle Time | $t_{RTC}$ | 45 | | 65 | | 80 | | 100 | | ns | |
| Retransmit Pulse Width | $t_{RT}$ | 35 | | 50 | | 65 | | 80 | | ns | 1 |
| Retransmit Recovery Time | $t_{RTR}$ | 10 | | 15 | | 15 | | 20 | | ns | |
| Retransmit Set Up Time | $t_{RTS}$ | 30 | | 40 | | 50 | | 60 | | ns | |

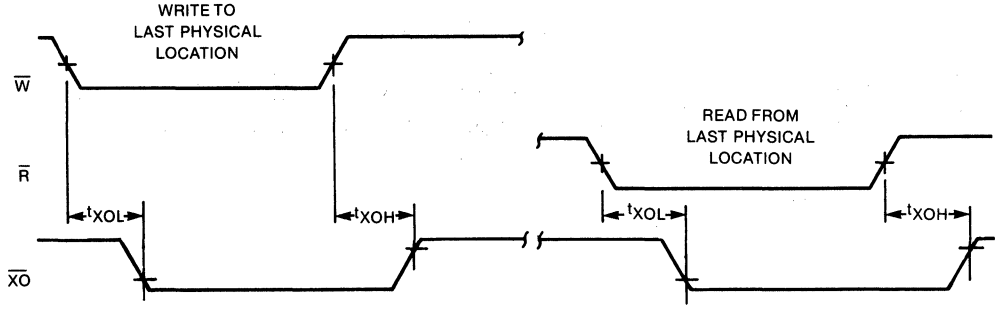
## EXPANSION TIMING

Figures 12 and 13 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

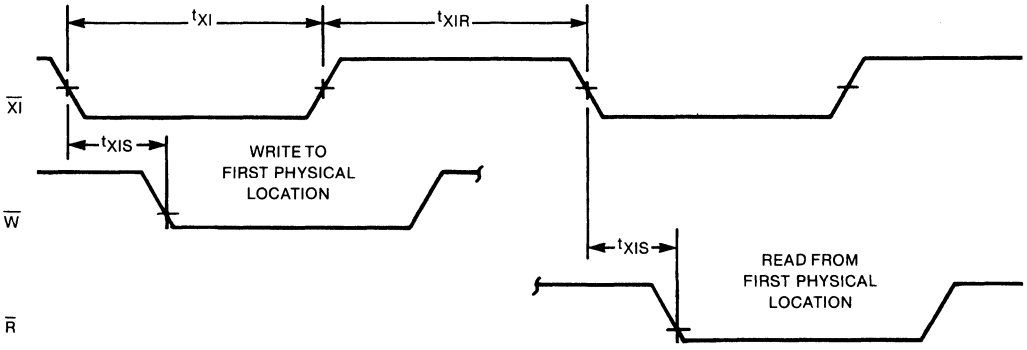
Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by $t_{XOL}$ and $t_{XOH}$. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

When in Depth Expansion mode, a given DS2011 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A DS2011 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur $t_{XIS}$ before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, $t_{XI}$, and recovery time, $t_{XIR}$, must be observed.

**EXPANSION OUT TIMING** Figure 12



**EXPANSION IN TIMING** Figure 13




**EXPANSION LOGIC**
**A.C. ELECTRICAL CHARACTERISTICS** (0°C to +70°C, $V_{CC}$ = 5.0V ± 10%)

| | | DS2011-35 | | DS2011-50 | | DS2011-65 | | DS2011-80 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Expansion Out Low | $t_{XOL}$ | | 30 | | 45 | | 55 | | 70 | ns | |
| Expansion Out High | $t_{XOH}$ | | 30 | | 45 | | 55 | | 70 | ns | |
| Expansion In Pulse Width | $t_{XI}$ | 35 | | 50 | | 65 | | 80 | | ns | 1 |
| Expansion In Recovery Time | $t_{XIR}$ | 10 | | 15 | | 15 | | 20 | | ns | |
| Expansion In Set Up Time | $t_{XIS}$ | 15 | | 20 | | 25 | | 30 | | ns | |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin relative to Ground -0.5V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Total Device Power Dissipation 1 Watt
Output Current per Pin 20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 3 |
| Ground | GND | | 0 | | V | |
| Logic "1" Voltage All Inputs | $V_{IH}$ | 2.0 | | $V_{CC}+0.3$ | V | 3 |
| Logic "0" Voltage | $V_{IL}$ | −0.3 | | +0.8 | V | 3,4 |

## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C) ($V_{CC}$ = 5.0 volts ± 10%)

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Leakage Current (Any Input) | $I_{IL}$ | −1 | 1 | uA | 5 |
| Output Leakage Current | $I_{OL}$ | —10 | 10 | uA | 6 |
| Output Logic "1" Voltage $I_{OUT}$ = −1 mA | $V_{OH}$ | 2.4 | | V | 3 |
| Output Logic "0" Voltage $I_{OUT}$ = 4 mA | $V_{OL}$ | | 0.4 | V | 3 |
| Average $V_{CC}$ Power Supply Current | $I_{CC1}$ | | 120 | mA | 7 |
| Average Standby Current ($\overline{R} = \overline{W} = \overline{RST} = \overline{FL}/\overline{RT} = V_{IH}$) | $I_{CC2}$ | | 8 | mA | 7 |
| Power Down Current (All Inputs = $V_{CC}$ − 0.2V) | $I_{CC3}$ | | 2 | mA | 7 |

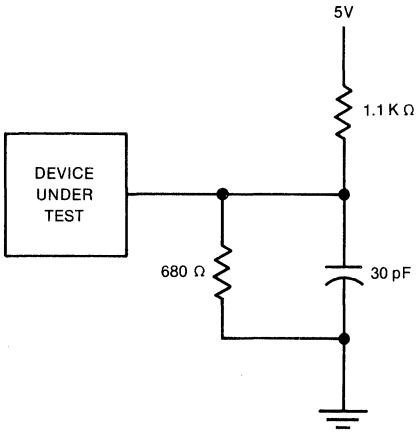
## CAPACITANCE

($t_A$ = 25°C)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Capacitance on Input Pins | $C_I$ | 7 | pF | |
| Capacitance on Output Pins | $C_O$ | 12 | pF | 8 |

**NOTES:**
1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to Ground.
4. – 1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
7. $I_{CC}$ measurements are made with outputs open.
8. With output buffer deselected.

**OUTPUT LOAD** Figure 14

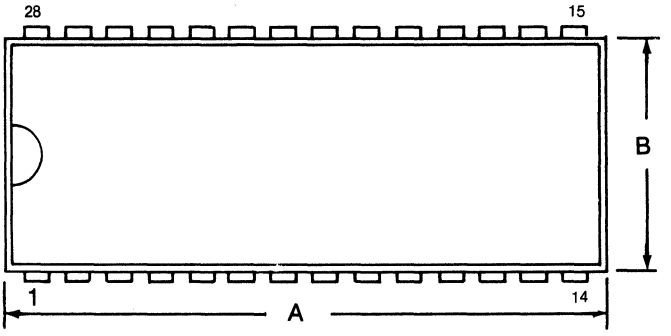


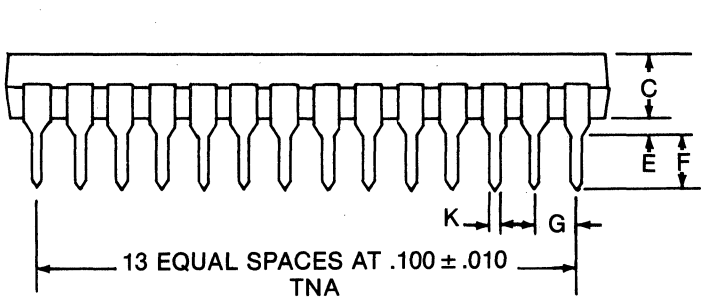

**A.C. TEST CONDITIONS:**

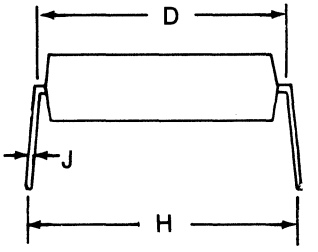
| | |
|---|---|
| Input Levels | GND to 3.0 V |
| Transition Times | 5 ns |
| Input Signal Timing Reference Level | 1.5 V |
| Output Signal Timing Reference Level | 0.8 V and 2.2 V |
| Ambient Temperature | 0 °C to 70 °C |
| $V_{CC}$ | 5.0 V ± 10% |

**PLASTIC DUAL-IN-LINE, 28 PINS** Figure 15

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.440 | 1.480 |
| B | .540 | .560 |
| C | .140 | .160 |
| D | .590 | .610 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .600 | .680 |
| J | .008 | .012 |
| K | .015 | .021 |



# Dallas Semiconductor
## 4096 x 9 FIFO

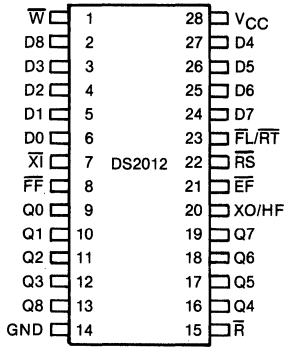
PRELIMINARY
**DS2012**

3

### FEATURES

- First-in, first-out memory based architecture
- Flexible 4096 x 9 organization
- Low power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 50ns, 65ns and 80ns access times
- Industrial temperature range −40°C to +85°C available designated IND
- Military temperature range −55°C to +125°C available designated MIL

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $\overline{W}$ | - WRITE |
| $\overline{R}$ | - READ |
| $\overline{RS}$ | - RESET |
| $\overline{FL}/\overline{RT}$ | - First Load/Retransmit |
| $D_{0-8}$ | - Data In |
| $Q_{0-8}$ | - Data Out |
| $\overline{XI}$ | - Expansion In |
| $\overline{XO}/\overline{HF}$ | - Expansion Out/Half Full |
| $\overline{FF}$ | - Full Flag |
| $\overline{EF}$ | - Empty Flag |
| $V_{CC}$ | - 5 Volts |
| GND | - Ground |

### DESCRIPTION

The DS2012 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the DS2012 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the WRITEs and READs are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

**Refer to DS2011 data sheet for detailed device description.**

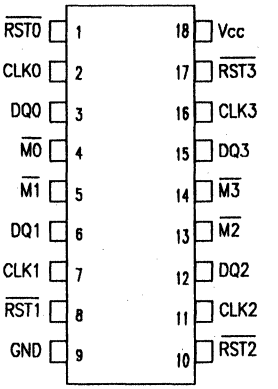
# Dallas Semiconductor
## *Quad Port Serial RAM*

**PRELIMINARY**
***DS2015***

### FEATURES

- Four partitioned easy access ports
- No arbitration required
- Message flag for each port
- Low pin count serial access
- Simultaneous multiport reads
- Message length of up to eight bytes
- Low power CMOS
- Space saving 18 pin DIP
- Directly interfaces to the DS1206 Phantom interface
- Provides a low cost interconnect for up to four microprocessor based systems

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| RST0-RST3 | Port 0 - Port 3 Reset |
| D/Q0-D/Q3 | Port 0 - Port 3 Data I/O |
| CLK0-CLK3 | Port 0 - Port 3 Clock |
| M0-M3 | Port 0 - Port 3 Message Ready |
| GND | Ground |
| Vcc | +5 Volts |

### DESCRIPTION

The DS2015 Quad Port Serial RAM is a low cost device which can be used to loosely couple up to four microprocessors or microcontrollers. Arbitration is handled by protocol and a message center which forces discipline and prevents collisions. Each port has access to all other ports for reading information and can write information only in its own memory area. The memory space for each port is 64 bits. Access to and from each port takes place over a three wire serial bus. The serial bus keeps pin count low while affording sufficient bandwidth to accommodate loosely coupled system communication. Each port also has a message flag which can be used to warn of message ready conditions.

## OPERATION

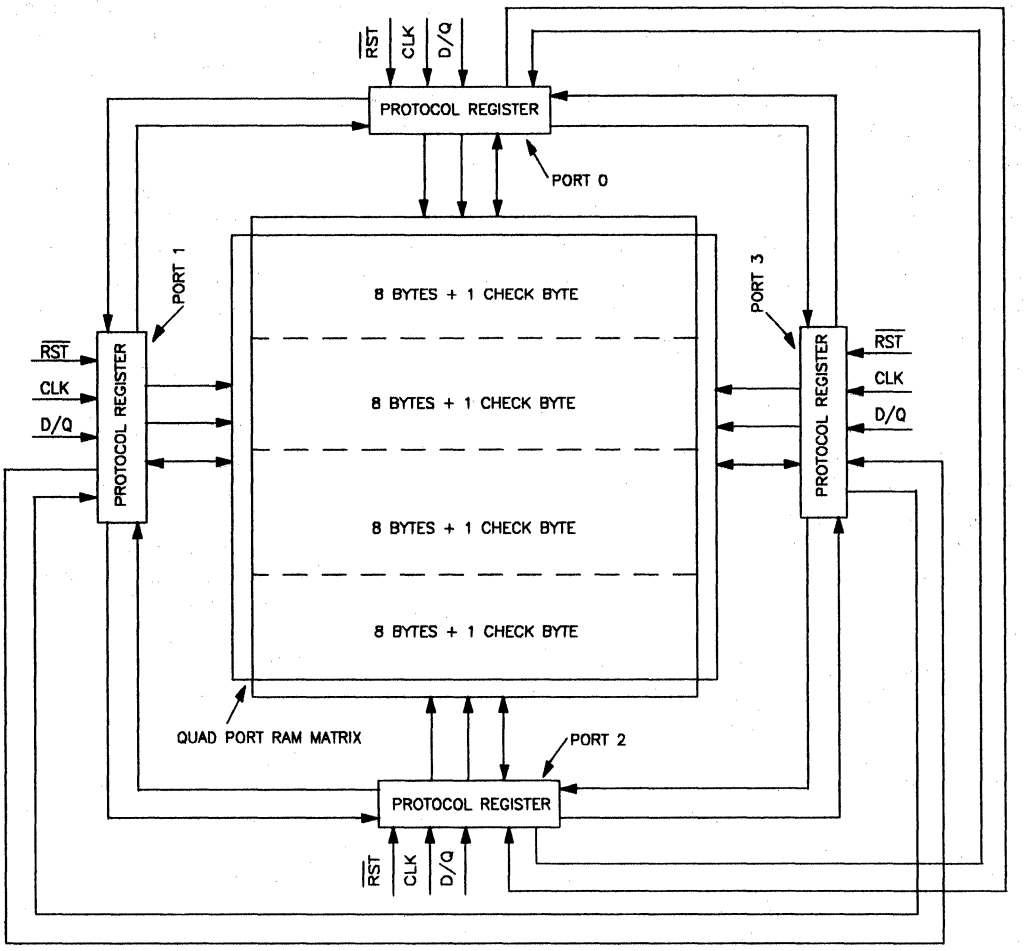
The DS2015 has four separate three wire serial ports. Each port has direct read and write access to eight message bytes of RAM which are designated as belonging to that particular port. In addition, each port has read only access to three groups of eight message bytes each which are designated as belonging to the three other ports. Messages are sent between any port by reading and writing the eight message bytes of the four ports. An optional check byte is provided for each group of eight message bytes to verify data integrity (see Figure 1). All of the cells within the RAM matrix are quad-ported and can be read simultaneously from four different directions. This reduces arbitration to concerns of write operations only.

Each of the four three wire serial ports contains a three byte protocol register which defines access to the RAM, and sets the discipline which controls arbitration between the four ports.

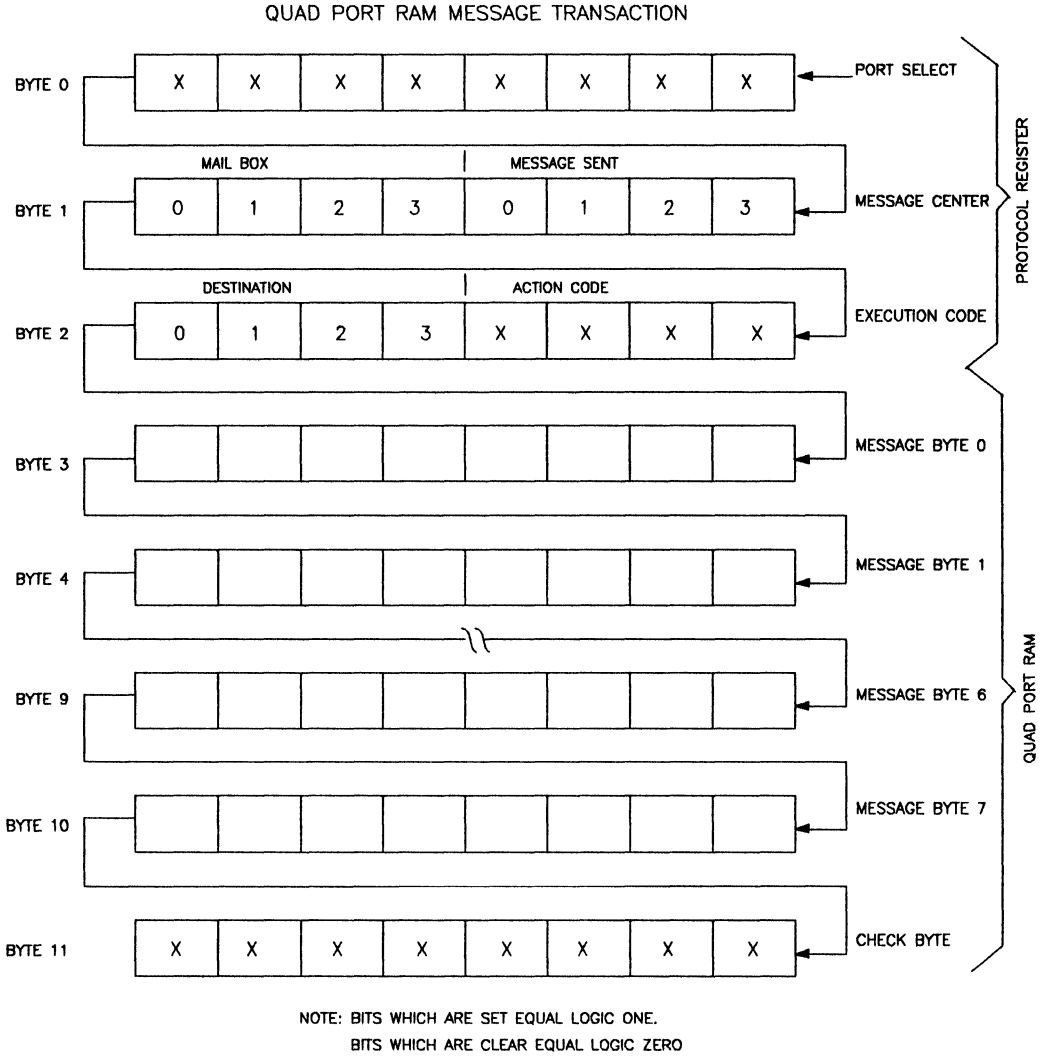
### Protocol Register

The first byte of the protocol register is called the port select (see Figure 2). This byte contains an eight bit pattern which must match the first 8 bits sent on an active port or any further activity will be ignored (Figure 3). A port is active when the reset line is inactive (high) and the CLK input is transitioning. The first eight bits are sent into a port on the D/Q line. The second byte of the protocol register contains eight bits of status information about activity on all four ports. This byte, called the message center, is read only and divided into two nibbles; messages sent and mailbox. The first four bits tell which messages the port has sent to other ports that have not been received. By reading these four bits, the inquiring port knows not to send new messages because all the receiving ports have not read to a previously sent message. Each message sent bit is cleared when the receiving port reads the last bit of its message or the $\overline{RST}$ input of the receiving port is driven low. The next four bits of the message center provide each port with the knowledge of pending messages which are ready for reading and the number of the port or ports which are sending the message(s). These bits are set by the destination bits of each port when a sending port finishes writing the last bit of a message. The mailboxes are read only bits. All message center bits are driven out on the DQ line while $\overline{RST}$ is inactive and the clock is transitioning. The third byte of the protocol register contains the execution code. The execution code byte is also divided into two four bit nibbles; the action code and the destination. This byte is write only and data is input on the D/Q line with $\overline{RST}$ active and the CLK input transitioning. The action code bits have only three patterns which will allow subsequent action to take place (Figure 3). An action code of four zeros (0000) calls for a read message action to occur in one of the four sections of the Quad Port RAM as specified by the destination bits. A read message can occur to only one port and, therefore, only one destination bit can be set for an action code of 0000. Once a destination bit is set, a complete message of eight bytes must be read in order to reset the message sent bit in the sending port's protocol register. An action code of a one and three zeros (1000) calls for a write message action to be performed. A write message can only be written in the section of the Quad Port RAM that is identified with the sending port. However, a message which is written by a sending port can be directed to one or more ports by the destination bits. The destination bits will cause the mailbox bits in the protocol register of each port which is to receive the message to be set to logic one as soon as the last bit of the message is written by the sending port. An action code of two ones and two zeros (1100) calls for a write message action to be performed with more

## FIGURE 1: QUAD PORT BLOCK DIAGRAM

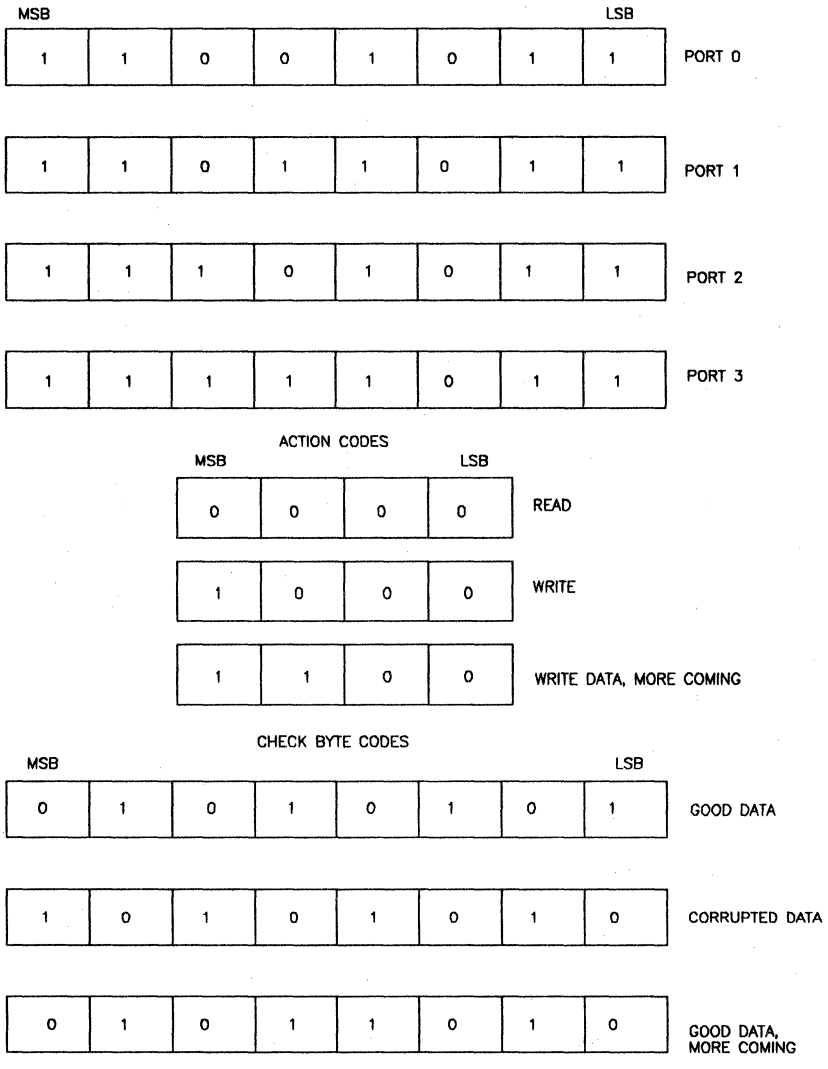


## FIGURE 2: QUAD PORT RAM MESSAGE TRANSACTION




NOTE: BITS WHICH ARE SET EQUAL LOGIC ONE.
BITS WHICH ARE CLEAR EQUAL LOGIC ZERO

## FIGURE 3: PORT SELECT CODE



data coming. This action code works exactly the same as a standard write message action with one exception. The check byte which follows an eight byte message is driven to a special code which, when read by a receiving port, indicates that more messages will be coming. This information can be used by a receiving port to reduce the overhead of constantly polling for new messages.

### Quad Port RAM

As mentioned, each port has direct read and write access to eight message bytes and read access to three groups of eight message bytes. Once the protocol register has been correctly accessed, one of the four sections of the Quad Port will be read or that section of the Quad Port RAM which is dedicated to the transmitting port will be written. When sending a message, all eight message bytes must be written. When receiving a message, all eight of the message bytes should be read. If fewer than all eight bytes are accessed, the message centers may be incorrect and errant communications between ports can result.

### Check Byte

A check byte (byte 11) is provided at the end of each of the eight message byte groups. The check byte is read only and provides information to a receiving port. Reading the check byte code is optional and may not be necessary in applications where software discipline is stringent enough to avoid accidental collisions between messages sent and messages received. Three different codes give status to a receiving port about the message which has just been read (Figure 3): good data, corrupted data, and good data with more data coming. When the check byte is read with a good data code, the data which is read by a receiving port is correct and valid. This check byte code assures the receiving port that a sending port is not writing a new message while the receiving port is attempting to read the previous message. When the check byte is read with a corrupted data code, the data which is read by a receiving port is suspect. This check byte warns the receiving port that the sending port is writing a new message while the receiving port is reading an older message. When the check byte is read with a good data and more coming code, the data which is read by a receiving port is correct and valid and additional messages will follow. This check byte code can be used by a receiving port to reduce the overhead of constant polling. If the check byte indicates that a new message will follow, the receiving port is warned to expect a new message.

### Polling vs. Message Flags

The DS2015 Quad Port RAM has two methods of warning the sending and receiving ports of impending message status. The software method of polling avoids the complication of additional hardware which is required to connect the message ready pins to a host sending/receiving unit. Polling is accomplished with a receiving unit by satisfying the port select byte of the protocol register and reading the message center. When a port is being polled, care should be taken to avoid entering the execution code portion of the protocol register. When polling a port, communications can be terminated by taking the $\overline{RST}$ input signal low. An alternate method of alerting a host sending/receiving unit of impending message status is to use the message ready signals to interrupt when a message is ready to be read. The message ready pins ($\overline{M0}$-$\overline{M3}$) are driven to an active state (low) when a sending port has written the last bit of the eight message bytes and $\overline{RST}$ of the sending port is set to the inactive state (low),

provided the appropriate destination bit is set. When the message ready pin is set to an active state, a receiving unit can execute a software routine to service the interrupt and read the pending message.

**$\overline{RST}$ Control**

All message transactions are initiated by driving the $\overline{RST}$ port input high. The $\overline{RST}$ input serves two functions. First, it turns on control logic which allows access to the protocol register. Second, the $\overline{RST}$ signal provides a method of terminating message transfer. Care must be taken when terminating a message transfer to avoid errant information in the message center. The following rules will avoid all problems.

1. While polling the message center for new messages, always terminate the transaction by driving $\overline{RST}$ low after completing a read of the message center byte and before entering the execution code byte.

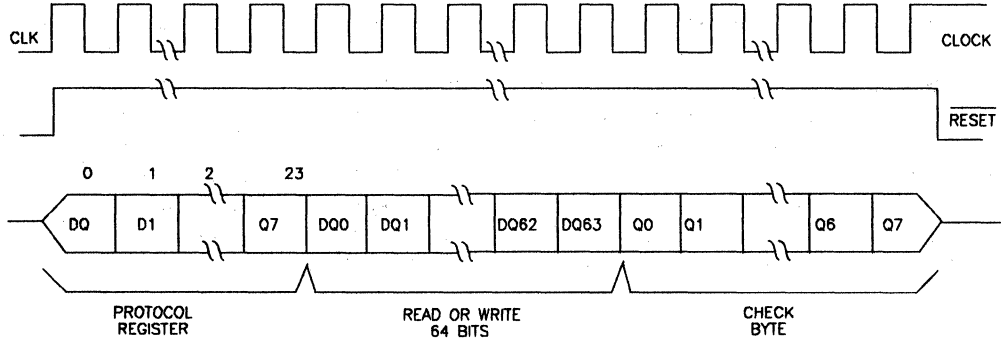
2. When sending a message, all eight messsage bytes must be written. If fewer than eight bytes are written, the mailbox bit of the destination port(s) may not be set and the check byte may indicate corrupted data.

3. When receiving a message, all eight bytes should be read. However, if $\overline{RESET}$ is used to terminate a message which is being read, the message sent bit and the mailbox bit are cleared as $\overline{RST}$ is driven low. When reading a message, the check byte is optional and can be either read or ignored.

**Clock Control**

A clock cycle is a sequence of a falling edge followed by a rising edge. For message inputs, the data must be valid during the rising edge of the clock cycle. Protocol bits and message bits are input on the rising edge of the clock. Protocol bits and message bits are output on the falling edge of the clock. All message transfer terminates if $\overline{RST}$ is low and the D/Q pins will then go to a high impedance state. When message transfer is terminated using $\overline{RST}$, the transition of $\overline{RST}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Figure 4 illustrates message transfer.

**FIGURE 4: QUAD PORT MESSAGE TRANSFER**



## ABSOLUTE MAXIMUM RATINGS*

Voltage on a pin to ground: -1.0 to + 7.0V
Operating temperature: 0°C to 70°C
Storage temperature: -55°C to + 125°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.



## RECOMMENDED D.C OPERATING CONDITIONS (0°C to 70°C)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | Vcc+0.3 | V | 1 |
| Logic 0 | $V_{IL}$ | -0.3 | | +0.8 | V | 1 |
| Supply | Vcc | 4.5 | 5.0 | 5.5 | V | 1 |

## D.C ELECTRICAL CHARACTERISTICS (0°C to 70°C, Vcc = 5V+/- 10%)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | -1 | | 1 | *u*A | |
| Output Leakage | $I_{LO}$ | | | 1 | *u*A | |
| Output Current @ 2.4V | $I_{OH}$ | -1 | | | mA | |
| Output Current @ .4V | $I_{OL}$ | +4 | | | mA | |
| Supply Current | $I_{CC}$ | | | 6 | mA | 2 |

## CAPACITANCE

($T_A$=25°C)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

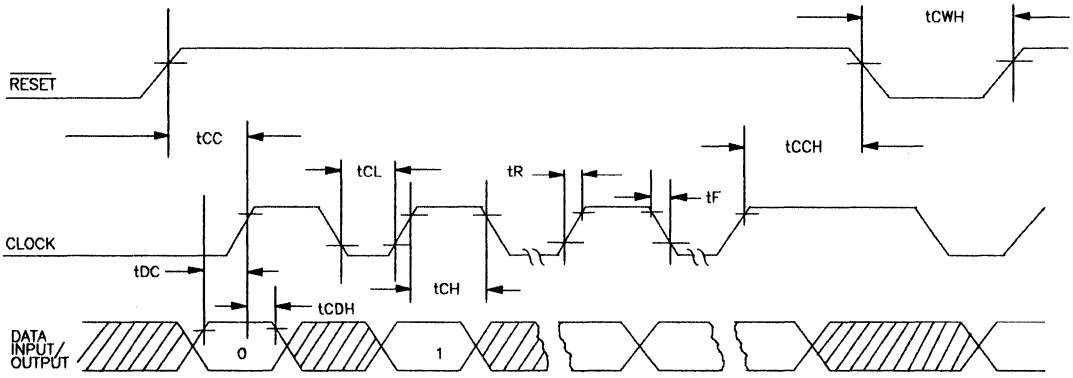
## A.C ELECTRICAL CHARACTERISTICS

(0°C to 70°C, Vcc = 5V+/- 10%)

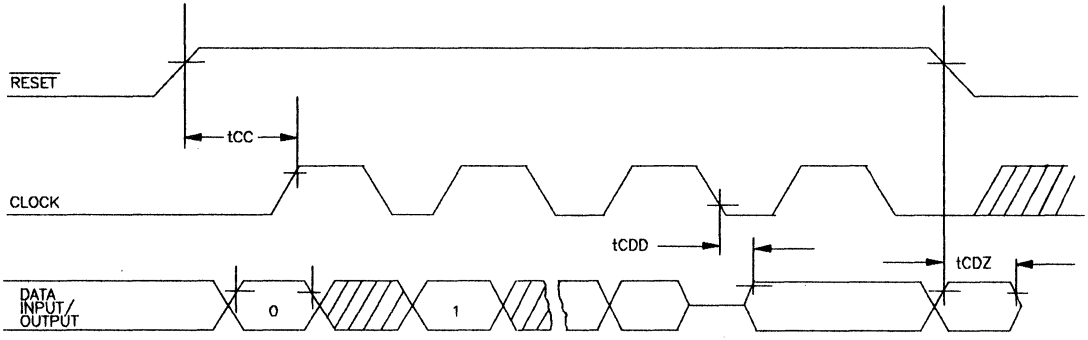
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Data to CLK Setup | $t_{DC}$ | 35 | | | ns | |
| CLK to Data Hold | $t_{CDH}$ | 40 | | | ns | |
| CLK to Data Delay | $t_{CDD}$ | | | 125 | ns | |
| CLK Low Time | $t_{CL}$ | 125 | | | ns | |
| CLK High Time | $t_{CH}$ | 125 | | | ns | |
| CLK Frequency | $f_{CLK}$ | D.C | | 4.0 | MHZ | |
| CLK Rise and Fall | $t_R$,$t_F$ | | | 500 | ns | |
| $\overline{\text{RST}}$ to CLK Set Up | $t_{CC}$ | 1 | | | us | |
| CLK to $\overline{\text{RST}}$ Hold | $t_{CCH}$ | 40 | | | ns | |
| $\overline{\text{RST}}$ Inactive Time | $t_{CWH}$ | 125 | | | ns | |
| $\overline{\text{RST}}$ to I/O High Z | $t_{CDZ}$ | | | 50 | ns | |
| $\overline{\text{RST}}$ to Message Ready | $t_{RF}$ | | | 50 | ns | |

## QUAD SERIAL PORT RAM TIMING DIAGRAM

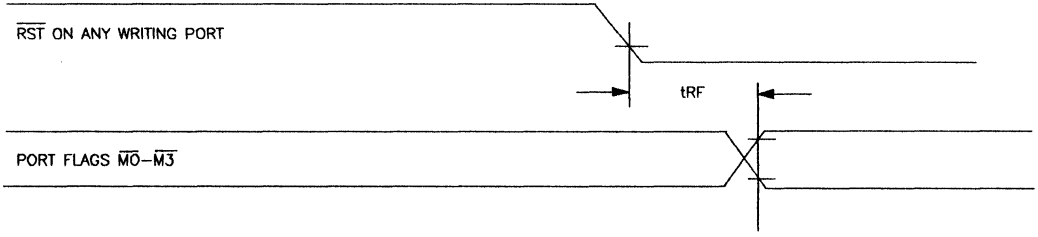
### TIMING DIAGRAM-WRITE DATA TRANSFER




### TIMING DIAGRAM-READ DATA TRANSFER



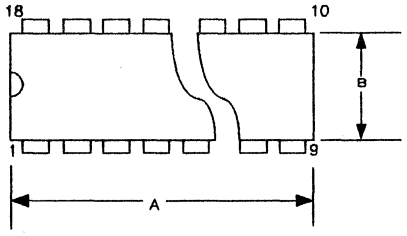

### TIMING DIAGRAM-MESSAGE READY



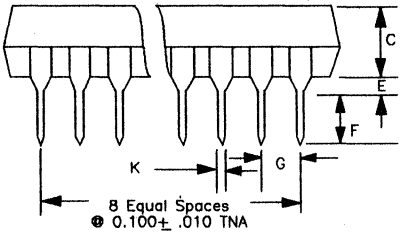

**Notes**

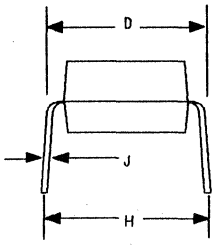
1. All voltages are referenced to ground.
2. All outputs are open.

# DS2015
# Quad Port Serial RAM




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 0.860 | 0.940 |
| B | 0.240 | 0.260 |
| C | 0.120 | 0.140 |
| D | 0.290 | 0.310 |
| E | 0.020 | 0.040 |
| F | 0.110 | 0.130 |
| G | 0.090 | 0.110 |
| H | 0.300 | 0.350 |
| J | 0.008 | 0.012 |
| K | 0.015 | 0.021 |



# Microcontroller

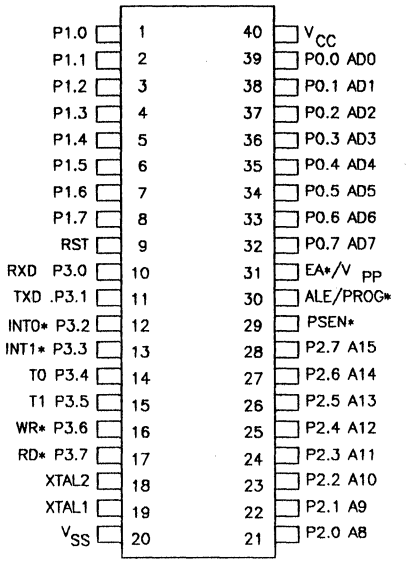
# Dallas Semiconductor
## *DS5000 Soft Microcontroller*

**PRELIMINARY**
***DS5000***

## FEATURES

- 8-bit uC adapts to task-at-hand:
  - 8 or 32 Kbytes of high performance nonvolatile RAM for Program and/or RAM for Program and/or Data Memory storage
  - Initial downloading of software in end system via on-chip serial port
  - Capable of modifying its own Program and/or Data Memory in end use
  - 128 internal nonvolatile registers for variable retention
- Crashproof operation:
  - Maintains all nonvolatile resources for 10 years in the absence of $V_{CC}$
  - Orchestrates orderly shutdown and automatic restart on power up/down
  - Automatic restart on detection of errant software execution
- Software Security Feature:
  - Executes encrypted software to prevent unauthorized disclosure
- On-chip full duplex serial I/O port
- Two on-chip timer/event counters
- 32 parallel I/O lines
- Compatible with industry standard 8051 instruction set and pinout

## PIN CONNECTIONS




## ORDERING INFORMATION

DS5000 XX – XX

| Clock | Freq. |
|---|---|
| –12 | 12MHZ |
| –16 | 16MHZ |

| Program Data RAM | |
|---|---|
| 8 | 8 Kbytes |
| 32 | 32 Kbytes |
| 64 | 64 Kbytes |

## DESCRIPTION

The DS5000 is a high performance 8-bit CMOS microcontroller that offers "softness" in all aspects of its application. This is accomplished through the comprehensive use of nonvolatile technology to preserve all information in the absence of system $V_{CC}$. The entire Program/Data Memory space is implemented using high speed, nonvolatile

static CMOS RAM. Two memory size versions are available which offer either 8 Kbytes or 32 Kbytes of NVRAM for Program/Data storage. Furthermore, internal data registers and key configuration registers are also nonvolatile.

A major benefit resulting from its nonvolatility is that the Soft Microcontroller allows Program Memory to be changed at any time, even after the device has been installed in the end system. Additionally, the size of the Program and Data Memory areas in the embedded RAM is variable and can be set either when the application software is initially loaded or by the software itself during execution.

Initial loading of the application software into the DS5000 is possible from either a parallel or serial interface to a host system. This function allows initialization of the nonvolatile areas of the device including Program/Data RAM and the configuration parameters. Serial loading uses the on-chip serial I/O port to accept incoming data from a host computer with an RS232 port, such as a PC-based development system. Not only is it possible to initially boot via the serial port in the end system but any subsequent software reloading can be made at will during system operation without the need for removal of the device.

The softness also provides the ultimate in adaptive system design by allowing either the Data RAM or the Data Registers to retain information in the absence of $V_{CC}$. As a result, a virtually unlimited number of variables and/or data tables can be updated and maintained over the life of the product, as opposed to their being lost during a power fluctuation. This capability allows software to be developed which updates variables and data tables to reflect the cumulative knowledge of the control system from the time that it was put into service. Consequently, control systems may be given the ability to learn from experience and react by altering processing steps in response to operating conditions which change over extended periods of time.

The DS5000 Soft Microcontroller incorporates control functions which provide crashproof operation when system power is momentarily disrupted, or removed entirely. These functions include the Power Fail Warning interrupt, Automatic Power Down, and Power On Restart. The Power Fail Warning interrupt provides an early warning of a potential power failure so that the operational state of the system may be stored prior to a complete removal of system $V_{CC}$. The Automatic Power Down feature causes all nonvolatile resources to be sustained at low current from the embedded lithium energy source while system power is removed. When $V_{CC}$ voltage is applied once again, the processor is automatically restarted with an internal flag set indicating that a Power On sequence has just been performed. Regardless of whether the power merely fluctuates or is absent for years, upon its return the Soft Microcontroller has the ability to resume execution when power is reapplied as if the power failure had not occurred at all.

The Soft Microcontroller's tolerance of power cycling provides an alternative for battery-powered hand-held systems which typically drain their batteries during periods of idle time, when processing is not being performed. On/off power cycling can be employed to cause such systems to consume battery power only during processing, as a way of dramatically reducing the overall power dissipation.

The DS5000 also provides extensive software security with its unique on-chip software encryption logic. This feature prevents un-

authorized individuals from reading and disassembling Program/Data RAM. When activated, the device loads and executes the software in an encrypted form, rendering the contents of the RAM and the execution of the program unintelligible to the outside observer. The encryption algorithm uses an internally stored and protected 40-bit key which is programmed by the user. Any attempt to discover the key value results in its erasure, rendering the contents of the Program/Data RAM useless. In this manner, the investment represented by the resident software is protected from piracy.

The DS5000 incorporates these unique functions in a device which is instruction set and pin compatible with the industry standard 8051 microcontroller architecture. Development work for new designs based on the DS5000 may be performed utilizing existing development tools and software packages which support the 8051 architecture.

The DS5000 also provides a full complement of I/O functions including two 16-bit event counter/timers, a full duplex serial I/O port capable of asynchronous or synchronous operation, 32 parallel I/O lines, and a watchdog timer. If additional external memory is desired beyond the embedded Program/Data RAM, 18 parallel I/O lines may be assigned to serve the Expanded Bus function.

## PIN DESCRIPTION

**NOTE:** All inverted signal names are denoted with a asterisk (*) as a suffix to the signal name (e.g. INT0*). This convention is followed throughout this document.

| | | |
|---|---|---|
| **$V_{CC}$, GND** | - | Power Supply inputs. |
| **P0.7-P0.0** | - | Port 0: Bidirectional I/O; open drain<br>These pins also serve the function of: |
| **AD7-AD0** | - | Address/Data Bus: Bidirectional |
| **P1.7-P1.0** | - | Port 1: Bidirectional I/O |
| **P2.7-P2.0** | - | Port 2: Bidirectional I/O<br>These pins also serve the function of: |
| **A15-A8** | - | Address Bus: Outputs |
| **P3.7-P3.0** | - | Port 3: Bidirectional I/O<br>Each of the pins on Port 3 may be selected to serve an alternate function; as described below: |
| **RD*<br>(P3.7)** | - | Expanded Data Memory Read Strobe: Output; active low |

| | | |
|---|---|---|
| **WR*** (P3.6) | - | Expanded Data Memory Write Strobe: Output; active low |
| **T1,T0** (P3.5,P3.4) | - | Timer/Counter pins: Inputs; active high |
| **INT1*, INT0*** (P3.3,P3.2) | - | External interrupt pins: Inputs; active low |
| **TXD (P3.1)** | - | Transmit Data: Output |
| **RXD (P3.0)** | - | Receive Data: Input |
| **RST** | - | Reset: Input; active high |
| **ALE (PROG*)** | - | Address Latch Enable: Output; active high (or Program Byte Enable: Input; active low) |
| **PSEN*** | - | Program Store Enable: Output; active low |
| **EA* (VPP)** | - | External Access Enable: Input; active low (or VPP programming voltage input) |
| **XTAL1, XTAL2** | - | Crystal inputs |



## INSTRUCTION SET

The DS5000 executes an instruction set which is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages which have been written for the 8051 are compatible with the DS5000 including cross-assemblers, high-level language compilers, and debugging tools.

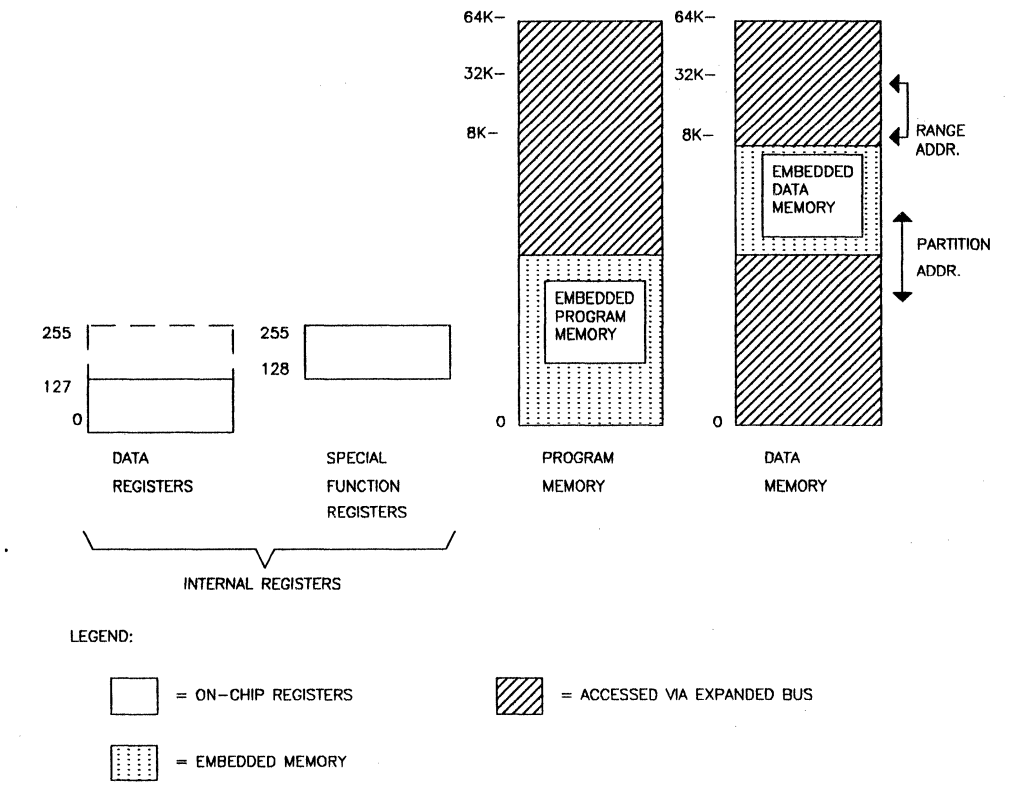
A complete description for the DS5000 instruction set is available in the DS5000 User's Guide (part # DS5000G).

## MEMORY ORGANIZATION

Figure 1 illustrates the address spaces which are accessed by the DS5000. As illustrated in the figure, separate address spaces exist for Program and Data Memory. Since the basic addressing capability of the machine is 16-bits, a maximum of 64 Kbytes of Program Memory and 64 Kbytes of Data Memory can be accessed by the DS5000 CPU. The 8K or 32K byte embedded RAM area can be used to contain both Program and Data Memory.

The Internal Register space is divided into two parts: Data Registers and and Special Function Registers. There are a total of 128 Data Registers including four 8-byte banks of working registers (R0-R7). The Special Function Registers include the CPU Registers as well as registers which provide control and status information for the Program and Data Memory mapping, non-volatile operation, and on-chip I/O functions.

**FIGURE 1: DS5000 LOGICAL ADDRESS SPACES**




## SPECIAL FUNCTION REGISTERS

There are a total of 23 Special Function Registers which have been implemented in the DS5000. Table 5-1 lists each of these along with their respective addresses, reset values, and functional descriptions.

**TABLE 1: DS5000 SPECIAL FUNCTION REGISTER MAP**

| New or Modified Register | Label | Direct Register Address | Reset Value | Bit address-able | Functional Description |
|---|---|---|---|---|---|
| | B | 0F0H | 00H | X | B Register |
| | A | 0E0H | 00H | X | Accumulator |
| | PSW | 0D0H | 00H | X | Program Status Word |
| X | TA | 0C7H | 055H | | Timed Access |
| X | MCON | 0C6H | RT | | Memory Control |
| X | IP | 0B8H | 00H | X | Interrupt Priority Ctl. |
| | P3 | 0B0H | 0FFH | X | Port 3 Parallel I/O |
| | IE | 0A8H | 00H | X | Interrupt Enable Ctl. |
| | P2 | 0A0H | 0FFH | X | Port 2 Parallel I/O |
| | SBUF | 099H | ?? | | Serial Data Buffer |
| | SCON | 098H | 00H | X | Serial Control |
| | P1 | 090H | 0FFH | X | Port 1 Parallel I/O |
| | TH1 | 08DH | 00H | | Timer 1 High Byte |
| | TH0 | 08CH | 00H | | Timer 0 High Byte |
| | TL1 | 08BH | 00H | | Timer 1 Low Byte |
| | TL0 | 08AH | 00H | | Timer 0 Low Byte |
| | TMOD | 089H | 00H | | Timer Mode Select |
| | TCON | 088H | 00H | X | Timer Control |
| X | PCON | 087H | RT | | Power Control |
| | DPH | 083H | 00H | | Data Pointer High Byte |
| | DPL | 082H | 00H | | Data Pointer Low Byte |
| | SP | 081H | 07H | | Stack Pointer |
| | P0 | 080H | 0FFH | X | Port 0 Parallel I/O |

**Notes:**

?? indicates that the register value is indeterminate on reset.
RT indicates that the initialization performed on the register is dependent on the type of the reset.

The Power Control (PCON), Interrupt Priority (IP), Memory Control (MCON), and Timed Access (TA) registers represent modifications from the 8051 implementation, as denoted in the above table. The following is a detailed summary of these registers.

## POWER CONTROL REGISTER

**Label: PCON** **Register Address: 087H**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| SMOD | POR | PFW | WTR | EPFW | EWT | STOP | IDL |

**Bit Description:**

**PCON.7 SMOD**
**"Double Baud Rate" :** When set to a 1, the baud rate is doubled when the serial port is being used in modes 1, 2, or 3.
**Initialization:** Cleared to a 0 on any reset.
**Read Access:** Can be read normally at any time.
**Write Access:** Can be written normally at any time.

**PCON.6 POR***
**"Power On Reset":** Indicates that the previous reset was initiated during a Power On sequence.
**Initialization:** Cleared to a 0 when a Power On Reset occurs. Remains at 0 until it is set to a 1 by software.
**Read Access:** Can be read normally at any time.
**Write Access:** Can be written only by using the Timed Access Register.

**PCON.5: PFW**
**"Power Fail Warning":** Indicates that a potential power failure is in progress. Set to 1 whenever $V_{CC}$ voltage is below the $V_{PFW}$ threshold. Cleared to a 0 immediately following a read operation of the PCON register. Once set, it will remain set until the read operation occurs regardless of activity on $V_{CC}$.
**Initialization:** Cleared to a 0 during a Power On Reset.
**Read Access:** Can be read normally anytime.
**Write Access:** Not writeable.

**PCON.4: WTR**

**"Watchdog Timer Reset"** Set to a 1 when a reset was issued as a result of a Watchdog Timer timeout. Cleared to 0 immediately following a read of the PCON register

**Initialization:** Set to a 1 after a Watchdog Timeout Reset. Cleared to a 0 on a No-$V_{LI}$ Power on Reset. Remains unchanged during other types of resets.

**Read Access:** May be read normally anytime.

**Write Access:** Cannot be written

**PCON.3: EPFW**

**"Enable Power Fail Interrupt":** Used to enable or disable the Power Fail interrupt. When EPFW is set to a 1 it will be enabled; it will be disabled when EPFW is cleared to a 0.

**Initialization:** Cleared to a 0 on any type of reset.

**Read Access:** Can be read normally anytime.

**Write Access:** Can be written normally anytime.

**PCON.2: EWT**

**"Enable Watch-dog Timer"** Used to enable or disable the Watchdog Timeout Reset. The Watch dog Timer is enabled if EWT is set to a 1 and will be disabled if EWT is cleared to a 0.

**Initialization:** Cleared to a 0 on a No-$V_{LI}$ Power on Reset. Remains unchanged during other types of resets.

**Read Access:** May be read normally anytime.

**Write Access:** Can be written only by using the Timed Access register.

**PCON.1: STOP**

**"Stop":** Used to invoke the Stop Mode. When set to a 1 program execution will terminate immediately and Stop Mode operation will commence. Cleared to a 0 when program execution resumes following a hardware reset.

**Initialization:** Cleared to a 0 on any type of reset

**Read Access:** Can be read anytime.

**Write Access:** Can be written only by using the Timed Access register.

**PCON.0: IDL**

**"Idle":** Used to invoke the Idle Mode. When set to a 1 program execution will be halted and will resume when the Idle bit is cleared to 0 follow ing an interrupt or a hardware reset.

**Initialization:** Cleared to 0 on any type of reset or interrupt.

**Read Access:** Can be read normally anytime.

**Write Access:** Can be written normally anytime.

## INTERRUPT PRIORITY REGISTER

**Label: IP** **Register Address: 0B8H**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| RWT | – | – | PS | PT1 | PX1 | PT0 | PX0 |

**Bit Description:**

**IP.7: RWT**
**"Reset Watch-Timer":** When set to a 1 the Watchdog Timer count will be reset, and counting will begin again. The RWT bit will then automatically be cleared again to 0. Writing a 0 into this bit has no effect.
**Initialization:** Cleared to a 0 on any reset.
**Read Access:** Cannot be read.
**Write Access:** Can be written only by using the Timed Access register.

**All of the following bits are read/write at any time and are cleared to 0 following any hardware reset.**

**IP.4: PS**
**"Serial Port Priority":** Programs Serial Port interrupts for high priority when set to 1. Low priority is selected when cleared to 0.

**IP.3: PT1**
**"Timer 1 Priority":** Programs Timer 1 interrupt for high priority when set to 1. Low priority is selected when cleared to 0.

**IP.2: PX1**
**"Ext. Int. 1 Priority":** Programs External Interrupt 1 for high priority when set to 1. Low priority is selected when cleared to 0.

**IP.1: PT0**
**"Timer 0 Priority":** Programs Timer 0 interrupt for high priority when set to 1. Low priority is selected when cleared to 0.

**IP.0: PX0**
**"Ext. Int. 0 Priority":** Programs External Interrupt 0 for high priority when set to 1. Low priority is selected when cleared to 0.

## MEMORY CONTROL REGISTER

**Label: MCON** **Register Address: 0C6H**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| PA3 | PA2 | PA1 | PA0 | RA32/8 | ECE2 | PAA | — |

**Bit Description:**
**MCON.7-4: PA3-0**

**"Partition Address":** Used to select the starting address of Data Memory in Embedded RAM. Program space lies below the Partition Address.

**Selection:**

| PA3 | PA2 | PA1 | PA0 | Partition Address |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0000H |
| 0 | 0 | 0 | 1 | 0800H |
| 0 | 0 | 1 | 0 | 1000H |
| 0 | 0 | 1 | 1 | 1800H |
| 0 | 1 | 0 | 0 | 2000H |
| 0 | 1 | 0 | 1 | 2800H |
| 0 | 1 | 1 | 0 | 3000H |
| 0 | 1 | 1 | 1 | 3800H |
| 1 | 0 | 0 | 0 | 4000H |
| 1 | 0 | 0 | 1 | 4800H |
| 1 | 0 | 1 | 0 | 5000H |
| 1 | 0 | 1 | 1 | 5800H |
| 1 | 1 | 0 | 0 | 6000H |
| 1 | 1 | 0 | 1 | 6800H |
| 1 | 1 | 1 | 0 | 7000H * |
| 1 | 1 | 1 | 1 | 8000H * |

*** A 4 Kbyte increment (not 2 Kbytes) in the Partition Address takes place between bit field values 1110B and 1111B.**

**Initialization:** Set to all 1's on a No $V_{LI}$ Power On Reset or when the Security Lock bit is cleared to a 0 from a previous 1 state. These bits are also set to all 1's when any attempt is made to have them cleared to all 0's with the SL bit set to a 1 (illegal condition).

**Read Access:** May be read anytime.

**Write Access:** PAA bit must = 1 in order to write PA3-0. Timed Access is not required to write to PA3-0 once PAA = 1.

**MCON.3: RA32/8**
**"Range Address":** Sets the maximum usable address in Embedded Memory.
RA32/8 = 0 sets Range Address = 1FFFH (8K)
RA32/8 = 1 sets Range Address = 7FFFH (32K)
**Initialization:** Set to a 1 during a No $V_{LI}$ Power On Reset and when the Security Lock bit (SL) is cleared to a 0 from a previous 1 state. Remains unchanged on all other types of resets.
**Read Access:** May be read normally anytime.
**Write Access:** Cannot be modified by the application software; can only be written during Program Load Mode.

**MCON.2: ECE2**
**"Enable Chip Enable 2":** Used to enable or disable the CE2* signal to additional Embedded RAM Data Memory space. This bit should always be cleared to 0 in the DS5000 8 and DS5000 32 versions.
**Initialization:** Cleared to 0 only during a No $V_{LI}$ Power On Reset.
**Read Access:** Read normally anytime.
**Write Access:** Can be written normally at any time.

**MCON.1: PAA**
**"Partition Address Access":** Used to protect the programming of the Partition Address select bits. PA3-0 cannot be written when PAA = 0. PAA can be written only via the Timed Access register.
**Initialization:** PAA is cleared only on a No-$V_{LI}$ Power On Reset
**Read Access:** PAA may be read anytime.
**Write Access:** The Timed Access register must be used to perform any type of write operation on the PAA bit

## TIMED ACCESS REGISTER

**Label: TA** **Register Address: 0C7H**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

**Bit Description:**

**TAn.n:** (All Timed Access bits)

**"Timed Access":** Used to invoke a Timed Access procedure required to write to any of the Timed Access protected bits including EWT, RWT, STOP, PAA. Timed Access is activated by three sequential write operations as in the example shown below:

```
MOV   0C7H,0AAH      ; Write 0AAH to TA register
MOV   0C7H,055H      ; Write 055H to TA register
ORL   IP,#804        ; Reset Watchdog Timer
```

**Initialization:** Written with the value of 055H following any type of reset.
**Read Access:** Cannot be read from the application software
**Write Access:** Can only be written anytime.

## PROGRAM LOAD MODES

The Program Load Modes allow initialization of the embedded Program/Data Memory and nonvolatile Internal Registers. This initialization may be performed in one of two ways:

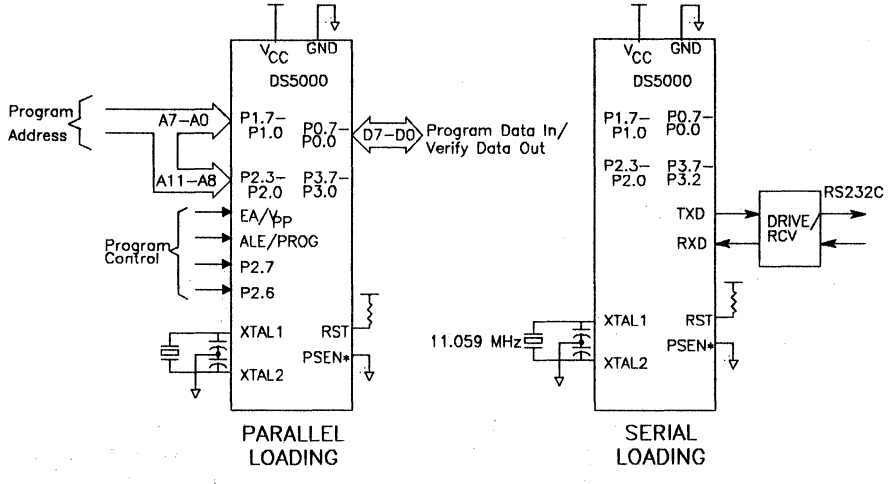
1) Parallel Program Load cycles which perform the initial loading from parallel address/data information presented on the I/O port pins.

2) Serial Program Loading which is capable of performing bootstrap loading of the DS5000. This feature allows the loading of the application program to be delayed until the DS5000 is installed in the end system.

The DS5000 is placed in its Program Load configuration by simultaneously applying a logic 1 to the RST pin and forcing the PSEN* line to a logic 0 level. Immediately following this action, the DS5000 will look for a Parallel Program Load pulse, or a serial ASCII carriage return (0DH) character received at 9600, 2400, 1200, or 300 bps over the serial port.

The hardware configurations used to select these modes of operation are illustrated in Figure 2.

## FIGURE 2: PROGRAM LOADING CONFIGURATIONS




The table below summarizes the selection of the available Parallel Program Load cycles. Figure 4 illustrates the timing associated with these cycles.

## TABLE 1: COMPATIBLE PROGRAM LOAD CYCLES

| Mode | RST | PSEN* | ALE | EA* | P2.7 | P2.6 |
|---|---|---|---|---|---|---|
| Program | 1 | 0 | 0 | VPP | 1 | 0 |
| Security Set | 1 | 0 | 0 | VPP | 1 | 1 |
| Verify | 1 | 0 | 1 | 1 | 0 | 0 |

The Program Cycle is used to load a byte of data into a register or memory location within the DS5000. The Verify Cycle is used to read this byte back for comparison with the originally loaded value to verify proper loading. Finally, the Security Set Cycle may be used to enable and disable the Software Security feature of the DS5000.

When the DS5000 first detects a Parallel Program Strobe pulse or a Security Set Strobe pulse while in the Program Load Mode following a Power On Reset, the internal hardware of the DS5000 is initialized so that an existing 4 Kbyte 87C51 program can be programmed into a DS5000 with little or no modification. This initialization automatically sets the Range Address for 8 Kbytes and maps the lowest 4 Kbyte bank of Embedded RAM as Program Memory. The top 4 Kbytes of Embedded RAM are mapped as Data Memory.

The Serial Program Load Mode is the easiest, fastest, most reliable, and most complete method of initially loading application software into the DS5000's nonvolatile RAM. Communication can be performed over a standard asynchronous serial communications port. The hardware configuration which is required for the Serial Program Load Mode is illustrated in Figure 2. Note that an 11.059 MHz time base is required in order for communication to take place at standard baud rate frequencies. The serial loader is designed to operate across a three wire interface from a standard UART. The receive, transmit and ground wires are all that are necessary to establish communication with the DS5000.

The Serial Loader implements an easy-to-use command line interface which allows an application program in an Intel Hex representation to be loaded into and read back from the device. Intel hex is the typical format which existing 8051 cross-assemblers output.

The serial loader responds to ten single character alphabetic commands which are summarized below:



| COMMAND | FUNCTION |
|---|---|
| D | Dump Intel Hex File |
| F | Fill Embedded RAM block with constant |
| K | Load 40-bit Encryption Key |
| L | Load Intel Hex File |
| R | Read MCON register |
| T | Trace (Echo) incoming Intel Hex data |
| U | Clear Security Lock |
| V | Verify Embedded RAM with incoming Intel Hex |
| W | Write MCON register |
| Z | Set Security Lock |

## POWER MANAGEMENT

The DS5000 is implemented using CMOS circuitry for low power consumption during full operation. Two software initiated modes are available for further power reduction for times when processing is not required and $V_{CC}$ is at normal operating voltage. These are the Idle and Stop Modes. In addition, internal control circuitry automatically places the the DS5000 in its Data Retention Mode in the absence of $V_{CC}$.

The on-chip nonvolatile control circuitry monitors the $V_{CC}$ for three below nominal operating voltage (Figure 3). When the voltage drops below the Power Fail Warning threshold ($V_{PFW}$) an interrupt will be generated to signal the processor of an impending power fail condition. This is to allow time for a service routine to save the operational state of the microcontroller prior to the $V_{CC}$ dropping below the $V_{CCmin}$ threshold. When this occurs, processor op-

eration is automatically terminated by internally halting the clock after the entire circuit has been made ready for the Data Retention Mode. Finally, once $V_{CC}$ voltage drops below the Lithium cell voltage threshold ($V_{LI}$) power from the embedded lithium cell is applied to place the device in its Data Retention Mode.

When $V_{CC}$ voltage is again applied to the system, an internal Power On Reset cycle is executed without the need for any external components on the RST pin. In addition, internal status is available to distinguish the Power On Reset from other types of resets.

## SOFTWARE SECURITY

The Software Security feature is implemented using Address and Data Encryptor circuitry which is present on the DS5000 die. Operation of the Software Security feature is performed by mainpulation of the 40-bit Encryption Key word and the Security Lock bit while in one of the Program Load modes. Encryption operation is first intiated by loading the 40-bit Encryption Key word.

When Software Encryption Operation is in effect and the Security Lock is disabled, the application software may be initially stored in an encrypted form during the initial loading of the device using one of the Program Load modes. As the loading is performed, the Data Encryptor logic transforms the opcode, operand, and data byte defined at each memory location defined by the software. Similarly, the Address Encryptor translates the "logical" address of each location into an encrypted address at which the byte is actually stored. Although each encryptor uses its own algorithm for encrypting data, both depend on the 40-bit key word which is contained in the Encryption Key registers (EK0-4).

As long as the Security Lock remains disabled, the actual unencrypted contents of the embedded Program/Data RAM may be read back for verification while in the Program Load mode. Once the contents have been verified, the final action performed during the Program Load Mode should be the enabling of the Security Lock bit. From this point on it will be impossible to read back the unencrypted contents of the Program/Data RAM or the contents of the Encryption Key registers.

When the application software is executed, the Address and Data Encryptors provide the opcodes, operands, and data to the CPU that execution of the application software can take place as normal. This action also takes place in real time so that no additional delays are imposed on the execution time of the software. Thus, the Software Encryption Operation is transparent to the application software.

The Software Encryption Operation is disabled and the contents of the Encryption Key registers are automatically erased whenever the Security Lock bit is cleared to a 0 from a previous 1 condition. This action renders the contents of the embedded Program/Data RAM useless, so that the application software can no longer be correctly interpreted by the DS5000 CPU. Although the contents of the Program/Data RAM can at this point be read back in a Program Load Mode, they cannot be de-encrypted since the original 40-bit key word has been lost.

## ADDITIONAL INFORMATION

A complete description for all operational aspects of the DS5000, including an instruction set description, timing details, and electrical specifications is available in the DS5000 User's Guide (part # DS5000G).

## SELECTED ELECTRICAL CHARACTERISTICS

The following are selected electrical operating characteristics of the DS5000. A full set of electrical characterics is available in the DS5000 User's Guide.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on any pin relative to ground | -0.1 to 7.0V |
| Operating Temperature | -0 deg. to 70 deg. C |
| Storage Temperature | -40 deg. C to +70 deg. C |
| Soldering Temperature | 260 deg. C for 10 sec. |

* This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.



## D.C. CHARACTERISTICS

($T_A$ = 0 deg. C to 70 deg. C; $V_{CC}$ = 5V ± 10%)

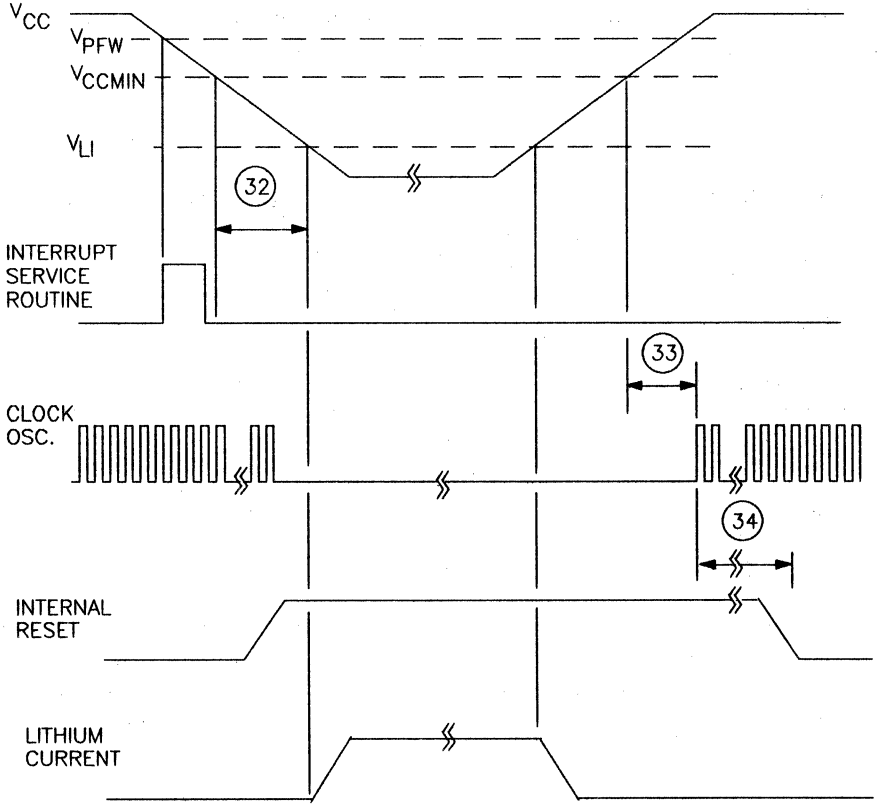
| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Stop Mode Current | $I_{SM}$ | | | 80 | uA | 4 |
| Power Fail Warning Voltage | $V_{PFW}$ | 4.15 | 4.6 | 4.75 | | V |
| Minimum Operating Voltage | $V_{CCmin}$ | 4.05 | 4.5 | 4.65 | V | |
| Lithium Supply Voltage | $V_{LI}$ | | | 3.3 | V | |
| Programming Supply Voltage (Parallel Program Mode) | $V_{PP}$ | 12.5 | | 13.0 | V | |
| Program Supply Current | $I_{PP}$ | | 9.2 | 15 | mA | |
| Operating Current DS5000 8<br>DS5000 32 | $I_{CC}$ | | | 43.2<br>48.2 | mA | |
| Idle Mode Current | $I_{CC}$ | | | 6.2 | mA | |

## A.C. CHARACTERISTICS
## POWER CYCLING TIMING

($T_A$ = 0 deg. C to 70 deg. C; $V_{CC}$ = 5V + 10%)

| # | PARAMETER | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|
| 32 | Slew rate from $V_{CCmin}$ to $V_{LImax}$ | $t_F$ | 40 | | us |
| 33 | Crystal start up time | $t_{CSU}$ | (note 5) | | |
| 34 | Power On Reset Delay | $t_{POR}$ | $2150*4t_{CLK}$ | | us |

**FIGURE 3: POWER CYCLING TIMING DIAGRAM**

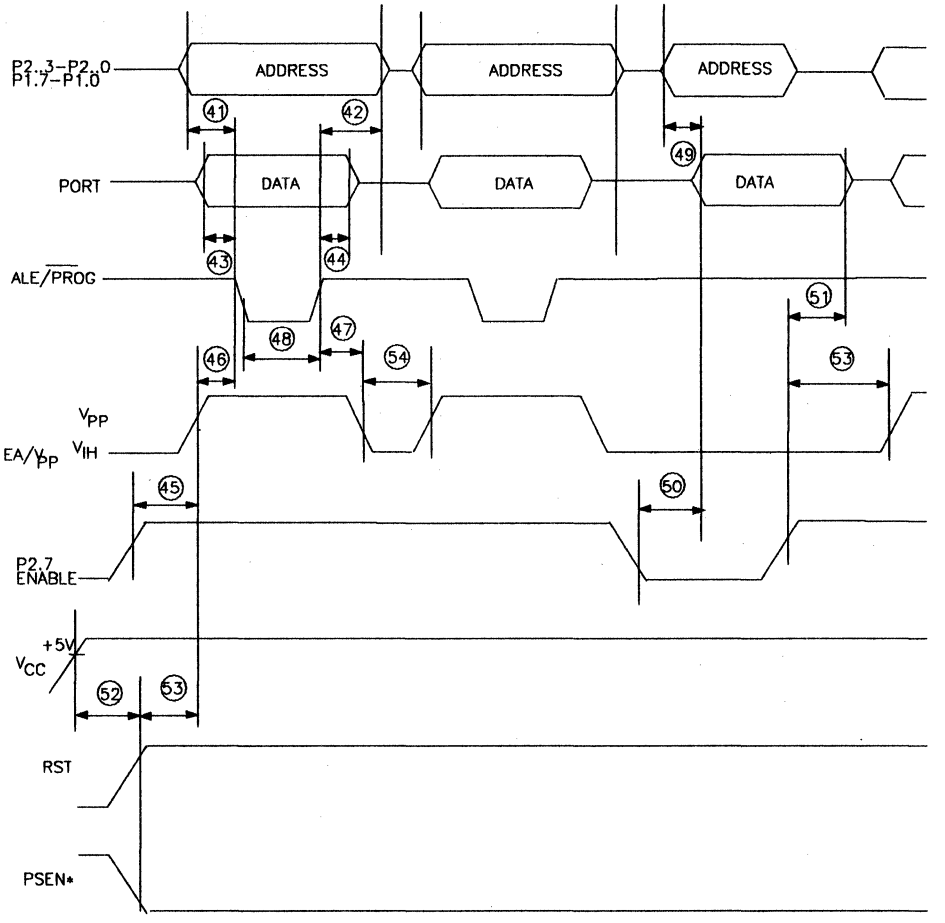


## A.C.CHARACTERISTICS
## PARALLEL PROGRAM LOAD TIMING

($T_A$= 0 deg. C to 70 deg. C; $V_{CC}$= 5V + 10%)

| # | PARAMETER | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|
| 40 | Oscillator Frequency | $1/t_{CLK}$ | 1.0 | 12.0 | MHz |
| 41 | Address Setup to PROG* low | $t_{AVPRL}$ | $48t_{CLK}$ | | |
| 42 | Address Hold After PROG* high | $t_{PRHAV}$ | $48t_{CLK}$ | | |
| 43 | Data Setup to PROG* low | $t_{DVPRL}$ | $48t_{CLK}$ | | |
| 44 | Data Hold After PROG* high | $t_{PRHDV}$ | $48t_{CLK}$ | | |
| 45 | P2.7 High Setup to VPP | $t_{P27HVP}$ | $48t_{CLK}$ | | |
| 46 | VPP Setup to PROG* low | $t_{VPHPRL}$ | 10 | | us |
| 47 | VPP Hold After PROG* low | $t_{PRHVPL}$ | 10 | | us |
| 48 | PROG* Width low | $t_{PRW}$ | $2400t_{CLK}$ | | |
| 49 | Data Output from Address Valid | $t_{AVDV}$ | | $48t_{CLK}$ | |
| 50 | Data Output from P2.7 low | $t_{DVP27L}$ | | $48t_{CLK}$ | |
| 51 | Data Float after P2.7 High | $t_{P27HDZ}$ | 0 | $48t_{CLK}$ | |
| 52 | Delay to Reset/PSEN* active after Power On | $t_{PORPV}$ | 26304 $*t_{CLK}$ | | |
| 53 | Reset/PSEN* active (or Verify inactive) to VPP high | | $1200t_{CLK}$ | | |
| 54 | VPP inactive (between Program cycles) | | $900t_{CLK}$ | | |

## FIGURE 4: PARALLEL PROGRAM LOAD TIMING



Notes:

1. All voltages are referenced to ground.

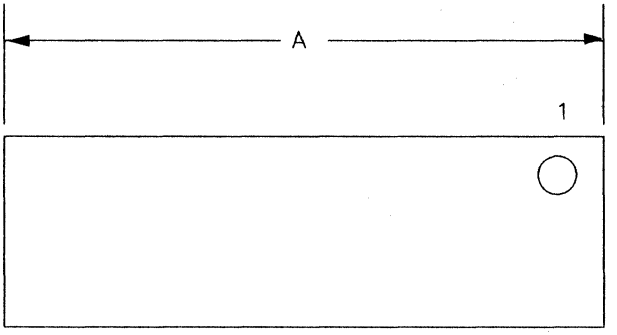
2. Maximum operating ICC is measured with all output pins disconnected; XTAL1 driven with tCLKR, tCLKF = 10 ns, VIL = 0.5V, VIH = 4.5V; XTAL2 disconnected; /EA=RST=PORT0=VCC.

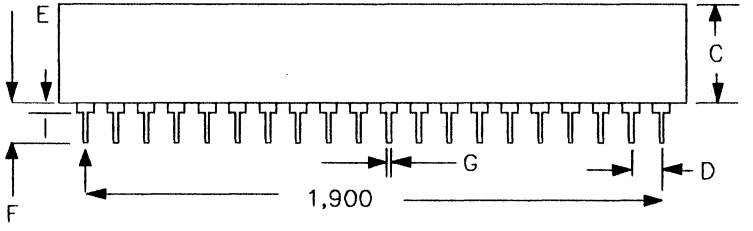
3. Idle Mode ICC is measured with all output pins disconnected; XTAL1 driven with tCLKR, tCLKF = 10 ns, VIL = 0.5V, VIH = 4.5V; XTAL2 disconnected; EA=RST=PORT0=VCC.

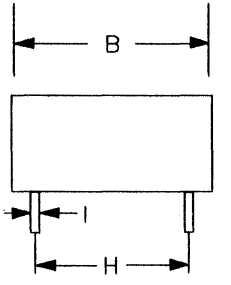
4. Stop Mode ICC is measured with all output pins disconnected; EA=PORT0=VCC; XTAL2 not connected; RST = VSS.

5. Crystal start up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on-chip oscillator. The user should check with the crystal vendor for a worst case spec on this time.

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 2.080 | 2.100 |
| B | .680 | .700 |
| C | .290 | .310 |
| D | .090 | .110 |
| E | .040 | .060 |
| F | .165 | .185 |
| G | .016 | .020 |
| H | .590 | .610 |
| I | .009 | .012 |



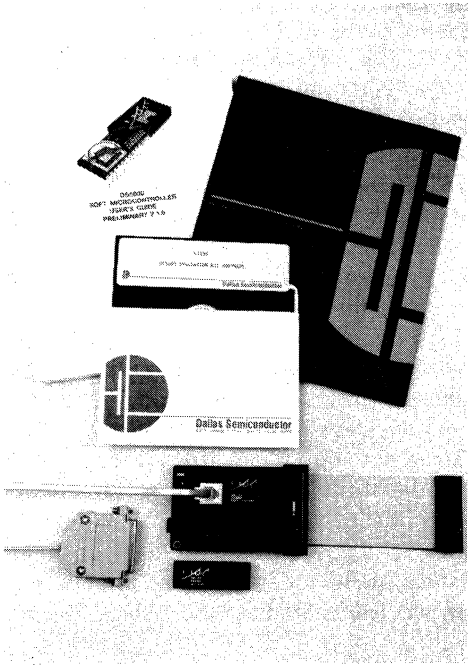



# Dallas Semiconductor
## *DS5000 Evaluation Kit*

## *PRELIMINARY*
## *DS5000K*

### FEATURES

- Allows immediate evaluation of DS5000 in an existing application
- Supplied with DS5000 32, software diskette, DS5000 User's Guide, In System Loader hardware
- Supports in-system serial downloading of DS5000 from an IBM PC host
- Downloads/verifies Intel Hex absolute object files residing on IBM PC
- User-friendly software prompts user for required system configuration information
- Supports serial download rates up to 9600 bps
- Requires no support circuit overhead on target system




4

### DESCRIPTION

The DS5000K is a development support system which is designed to allow immediate evaluation of the DS5000 Soft Microcontroller in a system application. Materials provided with the kit include a DS5000 with 32 Kbytes of RAM, a DS5000 User's Guide, In System Loader serial download hardware, and software for the IBM PC (KIT5K). Using the Evaluation Kit, the user can quickly configure the DS5000 for operation in the target system. This configuration can be performed without detailed knowledge of the operation of the DS5000's Serial Load Mode. The DS5000 Evaluation Kit not only serves as a first-time evaluation system for the DS5000, but also performs the equivalent function of an EPROM programming system throughout the prototyping phase of the design cycle.

The Evaluation Kit's In System Loader hardware allows application software to be loaded into the DS5000 while it is connected to the target system, eliminating the need for removal of the device when reprogramming is required. The In System Loader hardware consists of an RS232 cable that connects to

the RS232 Fixture which houses the appropriate interface circuitry and provides a 40-pin socket for the DS5000. The Fixture in turn attaches to the 40-pin target cable which connects to the microcontroller socket in the target system. The hardware provides the mechanism for the KIT5K software to take control of the DS5000 via the RS232 cable, place the device in its Serial Program Load Mode, and transmit new software to the device.

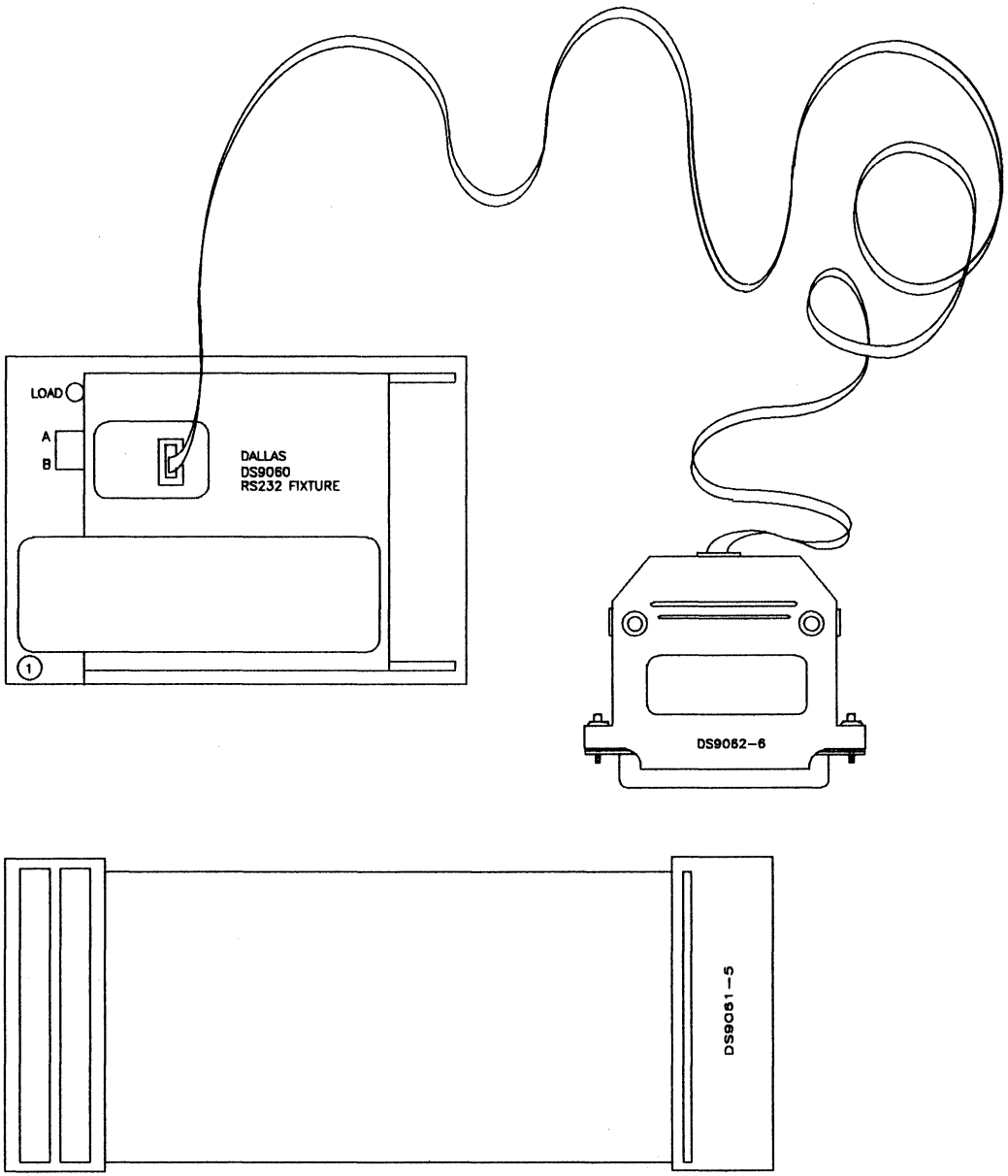
KIT5K is a user-friendly software package which provides a high-level user interface to the DS5000 via its Serial Load Mode. When the Program command is executed, the user is walked through a series of system configuration questions so that the DS5000 can be properly initialized before downloading takes place. Parameters such as the device's Program/Data Memory mapping and Software Encryption operation are initialized in the proper order in this fashion. KIT5K manages all of the communication with the DS5000 during the downloading process, so that the details of the serial download operation can remain transparent to the user. For more advanced users, KIT5K provides a number of commands which allow individual manipulation of the DS5000's resources. For example, these commands allow the direct initialization of the MCON register, loading of the 40-bit Encryption Key word, and setting and clearing of the Security Lock. In addition, an individual memory location examine and change capability is provided to allow patches to be made to the application software. When the loading operation is completed, the device can be released on command from the PC to run the application software.

## SYSTEM REQUIREMENTS

The Evaluation Kit requires an IBM PC or compatible with DOS 2.0 or later and at least 128K bytes of memory. In addition an RS232 port must be available which is configured as COM1 (03F8H, IRQ4) or COM2 (02F8H, IRQ4). Displays which are supported include monochrome, color graphics, or enhanced graphics (Mode 3).

Power (+5V) must be supplied to the RS232 fixture from the $V_{CC}$ pin of the target system via the Target Cable (see next page).

## FIGURE 1: DS5000 EVALUATION KIT: IN SYSTEM LOADER HARDWARE



## IN SYSTEM LOADER

The In System Loader hardware consists of the components which are depicted in Figure 1, and which are described below:

| Name | Dallas Part # | Description |
|---|---|---|
| RS232 Connector | DS9062-6 | Adaptor with cable. Adaptor provides DB25 female connector for connection to an RS232C IBM PC COM port on one side and RJ11 female on the other side. Cable carries RS232 signals required by the kit with two male RJ11 jacks on either end. |
| RS232 Fixture | DS9060 | RS232 serial interface for DS5000. Provides RJ11 female for RS232 signal connection, 40-pin DIP IC socket for DS5000, and 40-pin PC edge connector for connection to target cable. |
| Target Cable | DS9061-5 | 40-pin adaptor cable which connects the 40-pin edge connector on the RS232 Fixture to the target system microcontroller socket. |

The purpose of the In System Loader hardware is to serially download the DS5000 on command from the KIT5K software in such a manner that it will be transparent to the hardware on the target system.

## KIT5K OPERATION

KIT5K is the software environment supplied with the DS5000 Evalution Kit. It provides a high-level interface for loading application software to the DS5000 or for setting its configuration parameters.

KIT5K operates either in interactive mode, or in batch mode. The user will not see any of the communication between KIT5K and the DS5000 (except when debug is on). The following is a summary of commands recognized by the KIT5K software.

| | |
|---|---|
| **cd** | Change to another directory or show the default directory. |
| **com** | Specify the COM port for the In System Loader hardware. |
| **debug** | Turn debugging (DS5000 communication) on or off. |
| **dir** | List the default directory or specified path. |
| **display** | List DS5000 Embedded RAM contents in debug format. |

| | |
|---|---|
| **do** | Execute a list of KIT5K commands from a file. |
| **dump** | Dump DS5000 Embedded RAM in Intel Hex to a file. |
| **edit** | Individual examine/change Embedded RAM bytes in DS5000. |
| **exit** | Exit the KIT5K program; return to MS-DOS. |
| **fill** | Fill Embedded RAM with a constant value. |
| **help** | Describe the function and syntax of KIT5K commands. |
| **key** | Load the DS5000 40-bit Encryption Key word. |
| **load** | Load DS5000 Embedded RAM from an Intel Hex object file. |
| **lock** | Set the Security Lock on the DS5000. |
| **logoff** | Disable logging of KIT5K commands. |
| **logto** | Log KIT5K commands to the specified file. |
| **mcon** | Set the DS5000 MCON register with a specified value. |
| **partition** | Set the DS5000 Partition Address with a specified value. |
| **pgmode** | Place the DS5000 in its Serial Load Mode. |
| **program** | Program the DS5000 automatically with a configuration file. |
| **quit** | Same as exit; leave the KIT5K program; return to MS-DOS. |
| **range** | Set the DS5000 Range Address to 8K or 32K. |
| **run** | Disable DS5000 Serial Load Mode; begin execution. |
| **speed** | Specify the serial baud rate to be used during loading. |
| **status** | Display DS5000 status. |
| **type** | Type the requested filename to the screen. |
| **unlock** | Clear the Security Lock on the DS5000. |
| **verify** | Verify DS5000 Embedded RAM with the specified Intel Hex file. |



## ELECTRICAL SPECIFICATIONS

Operating Temperature Range 0 to +50 degrees C
System Power Supply Requirements +5V @ 100 mA
max; from Target System 50 mA typical
(DS5000 installed in target system; no load on port pins, PSEN*, ALE)

## INTERFACE

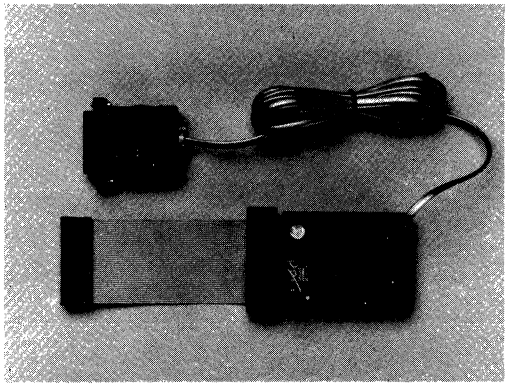
Connectors:
25-pin RS232 'D' type to RJ11 jack adaptor
RJ11 on RS232 Fixture
40-pin card edge (0.1" centers) on RS232 Fixture
40-pin edge connector on Target Cable
40-pin DIP plug on Target Cable

# Dallas Semiconductor
# DS5000 Development Kit

***PRODUCT PREVIEW***
***DS5000DK***

## FEATURES

- Low-cost real-time in-circuit emulation system for DS5000
- Supports memory examine/change, register examine/change, breakpoints, single-step operation
- Based on IBM-PC or compatible
- Unique, multi-windowed, dynamic display provides user-friendly interface
- Source code window supports disassembled symbolic program listing
- Register window provides easy access to Special Function and Data registers
- Symbolic data access by type of symbol
- Flowgraph window provides either a histograph or flowchart during program execution.
- On-line help facillity
- Provides direct debugging support for programs written in Archimedes C-51



## DESCRIPTION

The DS5000 Development Kit plugs into a DS5000 socket on a user's target system and provides real-time development of application software from an IBM-PC or compatible. Mutli-window symbolic access to all DS5000 resources provides a user-friendly development environment. The Development Kit's compact hardware connects to the PC computer via COM1 and into the target system via a 40-pin flat ribbon cable. All power is derived by the hardware from the target system. The software allows control of the target DS5000 in several different execution modes and provides symbolic access to all memory and I/O spaces. Single key control commands allow you to drive the Kit with fingertip control. All Development Kit software is licensed from Cybernetic Microsystems.

# Dallas Semiconductor
## *Soft Microcontroller*

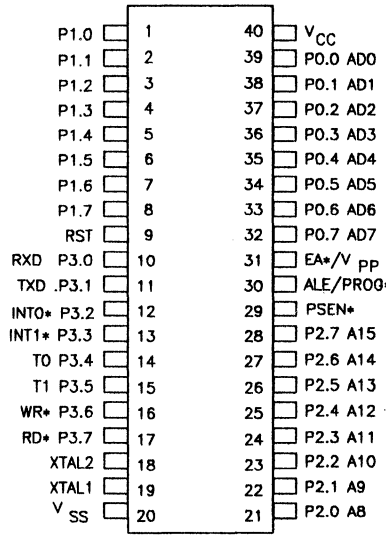
# PRODUCT PREVIEW
## *DS5000T*



## FEATURES

- Soft Microcontroller with embedded real-time clock function
- Capable of modifying its own program and/or data memory
- Program downloading via an on-chip full duplex serial port
- Adjustable partition between program and data memory
- Completely crash-proof: the program and data memories and all data registers are maintained in absence of power
- All 32 port pins available for I/O
- Automatic restart on detection of errant software execution
- Orderly shutdown and automatic restart on power up/down
- Program and data memory secure, with a tamper proof on-chip encryptor
- On-chip full duplex serial I/O port
- Two on-chip timer/event counters
- Compatible with industry standard 8051 instruction set and pinout

## PIN CONNECTIONS




## ORDERING INFORMATION

DS5000T XX XX

Speed Grade

| | |
|---|---|
| 12 | 12 MHz |
| 16 | 16 MHz |

Program/Data RAM

| | |
|---|---|
| 8 | 8 Kbytes |
| 32 | 32 Kbytes |

## DESCRIPTION

The DS5000T Microcontroller incorporates all of the features of the DS5000 along with the addtion of a built-in real-time clock/calender function. This function itself is identical to that performed by the DS1215 Timekeeper. The real-time clock is memory-mapped on the internal Embedded RAM address/data bus. As a result, it may be accessed by software as if it were Embedded Data RAM using the "LDX" set of instructions. Accesses to the real-time clock take place with no effect on I/O port pins.

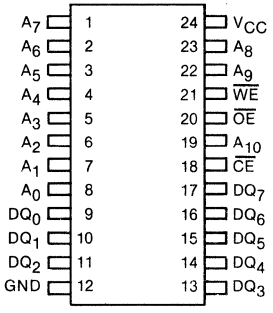
# Nonvolatile Static RAM

# Dallas Semiconductor
## *16K Nonvolatile Static RAM*

## *DS1220AB*
## *DS1220AD*

### FEATURES
- Data retention in the absence of $V_{CC}$
- Data is automatically protected during power loss
- Directly replaces 2K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 24-pin JEDEC pinout
- Available in either 150 or 200 ns read access time
- Read cycle time equals write cycle time
- Optional 5% and 10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

### PIN CONNECTIONS




### PIN NAMES
$A_0$-$A_{10}$ - Address Inputs
$\overline{CE}$ - Chip Enable
GND - Ground
$DQ_0$-$DQ_7$ - Data In/Data Out
$V_{CC}$ - Power (+5V)
$\overline{WE}$ - Write Enable
$\overline{OE}$ - Output Enable

### DESCRIPTION
The DS1220AB and DS1220AD are 16,384-bit, fully static, nonvolatile RAMs organized as 2048 words by 8 bits. Each nonvolatile static RAM has a self-contained lithium energy source and control circuitry which constantly monitors $V_{CC}$ for an out of tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 2K × 8 static RAM directly conforming to the popular byte wide 24 pin DIP standard. The DS1220AB also matches the pinout of the 2716 EPROM or the 2816 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

## OPERATION

### READ MODE

The DS1220AB and DS1220AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 11 address inputs ($A_0$-$A_{10}$) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access.

### WRITE MODE

The DS1220AB and DS1220AD are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

### DATA RETENTION MODE

The DS1220AB provides full functional capability for $V_{CC}$ greater than 4.75 volts and write protects by 4.5V. The DS1220AD provides full functional capability for $V_{CC}$ greater than 4.5 volts and write protects by 4.25V. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The nonvolatile static RAM constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts for the DS1220AD and 4.75 volts for the DS1220AB.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| DS1220AB Power Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V | |
| DS1220AD Power Supply Voltage | $V_{CC}$ | 4.50 | 5.0 | 5.50 | V | |
| Input Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | |
| Input Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | |

**D.C. ELECTRICAL CHARACTERISTICS**

(0°C to 70°C, $V_{CC}=5V\pm10\%$ for DS1220AD)
(0°C to 70°C, $V_{CC}=5V\pm5\%$ for DS1220AB)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −1.0 | | +1.0 | uA | |
| I/O Leakage Current | $I_{LO}$ | −5.0 | | +5.0 | uA | |
| Output Current @ 2.4V | $I_{OH}$ | −1.0 | | | mA | |
| Output Current @ 0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}=2.2V$ | $I_{DDS1}$ | | 3.0 | 5.0 | mA | |
| Standby Current $\overline{CE}=V_{CC}-0.5V$ | $I_{DDS2}$ | | 5.0 | 10.0 | mA | |
| Operating Current | $I_{DDO1}$ | | | 75 | mA | |
| Write Protection Voltage (DS1220AB) | $V_{TP}$ | 4.5 | 4.62 | 4.75 | V | |
| Write Protection Voltage (DS1220AD) | $V_{TP}$ | 4.25 | 4.37 | 4.5 | V | |

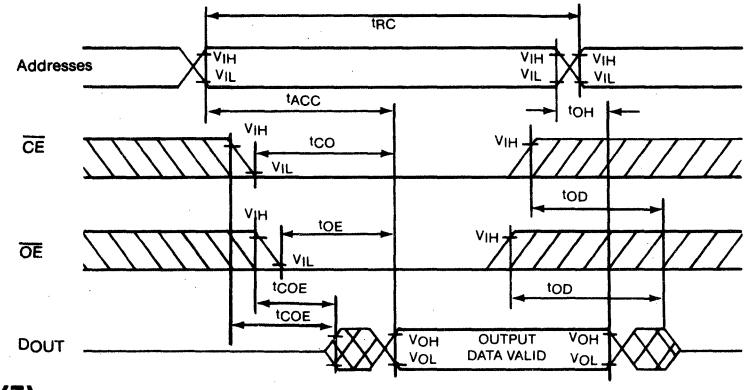
**CAPACITANCE** ($t_A = 25°C$)

| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | 5 | 10 | pF | |

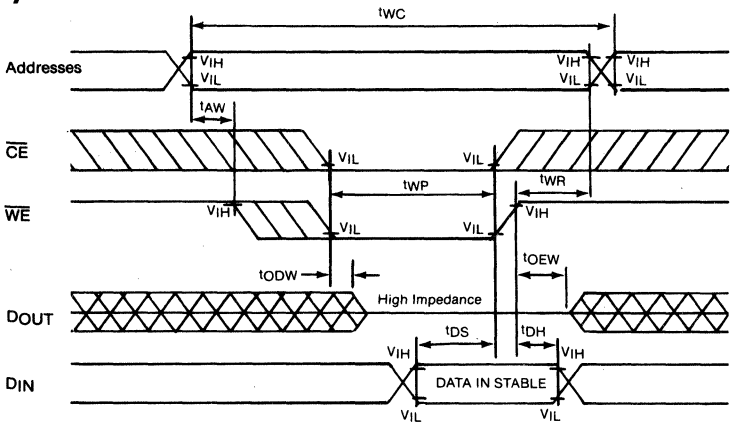
**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC} = 5.0V \pm 10\%$ for DS1220AD)
(0°C to 70°C, $V_{CC} = 5.0V \pm 5\%$ for DS1220AB)

| | | DS1220AD-150 DS1220AB-150 | | DS1220AD-200 DS1220AB-200 | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Read Cycle Time | $t_{RC}$ | 150 | | 200 | | ns | |
| Access Time | $t_{ACC}$ | | 150 | | 200 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 70 | | 100 | ns | |
| $\overline{CE}$ tc Output Valid | $t_{CO}$ | | 150 | | 200 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 10 | | 10 | | ns | |
| Output High Z from Deselection | $t_{OD}$ | | 70 | | 100 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | 10 | | ns | |
| Write Cycle Time | $t_{WC}$ | 150 | | 200 | | ns | |
| Write Pulse Width | $t_{WP}$ | 100 | | 150 | | ns | 3 |
| Address Set Up Time | $t_{AW}$ | 0 | | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 10 | | 10 | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | 70 | | 80 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 10 | | 10 | | ns | |
| Data Setup Time | $t_{DS}$ | 60 | | 90 | | ns | 4 |
| Data Hold Time | $t_{DH}$ | 20 | | 20 | | ns | 4,5 |

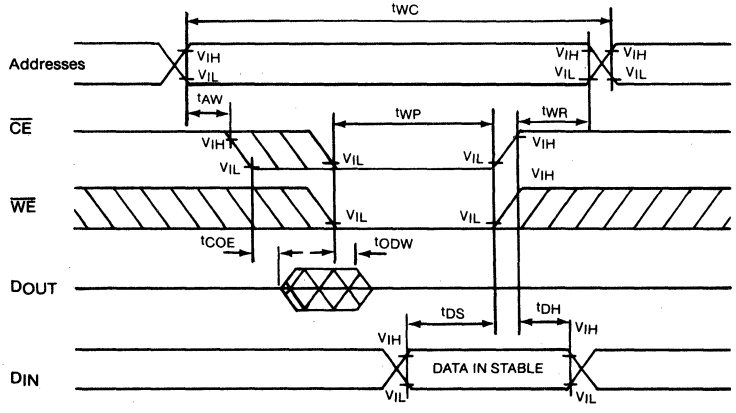
## READ CYCLE (1)



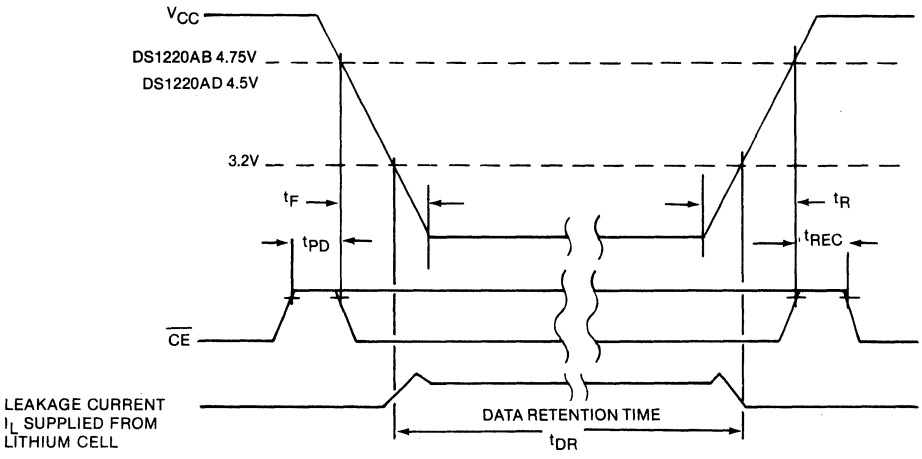

## WRITE CYCLE 1 (2), (6), (7)




## WRITE CYCLE 2 (2), (8)



## POWER-DOWN/POWER-UP CONDITION

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## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | us | |
| $t_F$ | $V_{CC}$ slew from 4.75V to 0V ($\overline{CE}$ at $V_{IH}$) | 300 | | us | DS1220AB |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 300 | | us | DS1220AD |
| $t_R$ | $V_{CC}$ slew from 0V to 4.75V ($\overline{CE}$ at $V_{IH}$) | 0 | | us | DS1220AB |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | us | DS1220AD |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power-Up | 2 | 125 | ms | |

($t_A = 25°C$)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 10 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH}$ = 20ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1220AB is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.

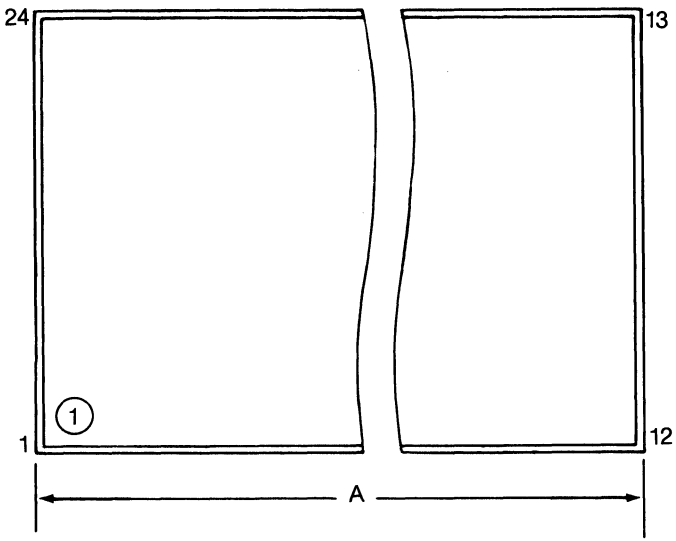
**D.C. TEST CONDITIONS**

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

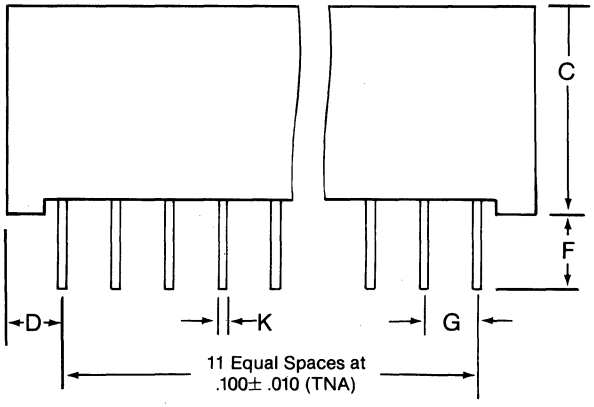
**A.C. TEST CONDITIONS**

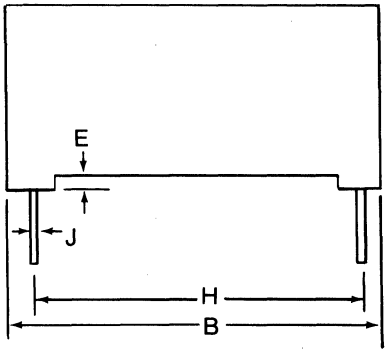
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

# DS1220AD
# DS1220AB
# Nonvolatile RAM




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.320 | 1.340 |
| B | .695 | .720 |
| C | .395 | .410 |
| D | .090 | .130 |
| E | .020 | .030 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |



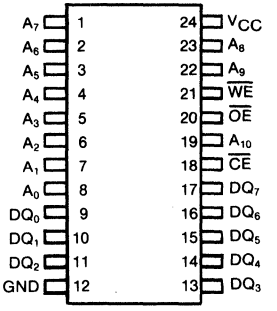




5

# Dallas Semiconductor
## *16K Nonvolatile Static RAM* — *DS1220Y*

### FEATURES
- Data retention in the absence of $V_{CC}$
- Data is automatically protected during power loss
- Directly replaces 2K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 24-pin JEDEC pinout
- Available in either 150 or 200 ns read access time
- Read cycle time equals write cycle time
- Full ± 10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

### PIN CONNECTIONS




### PIN NAMES
$A_0$-$A_{10}$ - Address Inputs
$\overline{CE}$ - Chip Enable
GND - Ground
$DQ_0$-$DQ_7$ - Data In/Data Out
$V_{CC}$ - Power (+5V)
$\overline{WE}$ - Write Enable
$\overline{OE}$ - Output Enable

### DESCRIPTION
The DS1220Y is a 16,384 bit fully static nonvolatile RAM organized as 2048 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors $V_{CC}$ for an out of tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 2K × 8 static RAM directly conforming to the popular byte wide 24 pin DIP standard. The DS1220Y also matches the pinout of the 2716 EPROM or the 2816 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

## OPERATION

### READ MODE

The DS1220Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 11 address inputs ($A_0$-$A_{10}$) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access.

### WRITE MODE

The DS1220Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

### DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for $V_{CC}$ greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The DS1220Y constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | |
| Input Logic 1 | $V_{IH}$ | 2.2 | | $V_{CCI}+0.3$ | V | |
| Input Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}=5V\pm10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −1.0 | | +1.0 | *u*A | |
| I/O Leakage Current | $I_{LO}$ | −5.0 | | +5.0 | *u*A | |
| Output Current @ 2.4V | $I_{OH}$ | −1.0 | −2.0 | | mA | |
| Output Current @ 0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}=2.2V$ | $I_{DDS1}$ | | 3.0 | 7.0 | mA | |
| Standby Current $CE=V_{CC}-0.5V$ | $I_{DDS2}$ | | 2.0 | 4.0 | mA | |
| Operating Current | $I_{DDO1}$ | | | 75 | mA | |
| Write Protection Voltage | $V_{TP}$ | | 4.25 | | V | |

## CAPACITANCE

($t_A = 25°C$)

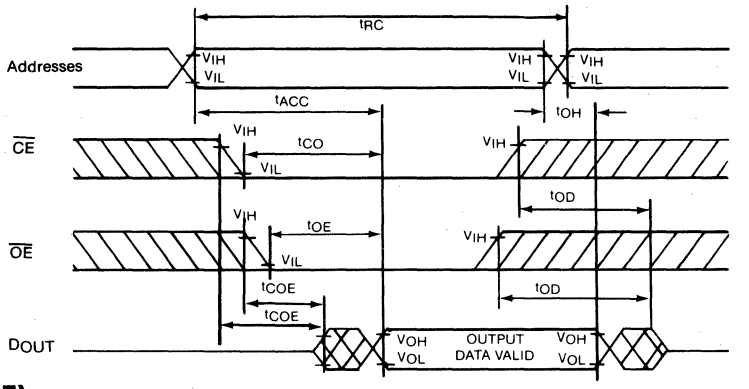
| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | 5 | 10 | pF | |

## A.C. ELECTRICAL CHARACTERISTICS

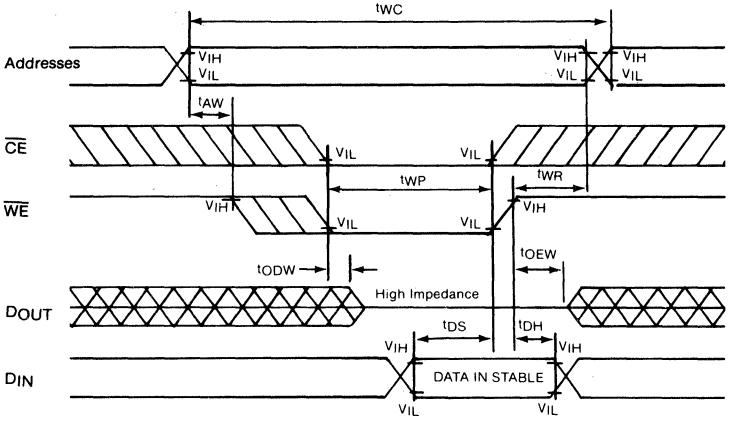
(0°C to 70°C, $V_{CC} = 5.0V \pm 10\%$)

| | | DS1220Y-150 | | DS1220Y-200 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Read Cycle Time | $t_{RC}$ | 150 | | 200 | | ns | |
| Access Time | $t_{ACC}$ | | 150 | | 200 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 70 | | 100 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | 150 | | 200 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 10 | | 10 | | ns | |
| Output High Z from Deselection | $t_{OD}$ | | 70 | | 100 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | 10 | | ns | |
| Write Cycle Time | $t_{WC}$ | 150 | | 200 | | ns | |
| Write Pulse Width | $t_{WP}$ | 100 | | 170 | | ns | 3 |
| Address Set Up Time | $t_{AW}$ | 0 | | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 10 | | 10 | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | 70 | | 80 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 10 | | 10 | | ns | |
| Data Setup Time | $t_{DS}$ | 60 | | 90 | | ns | 4 |
| Data Hold Time | $t_{DH}$ | 20 | | 20 | | ns | 4,5 |

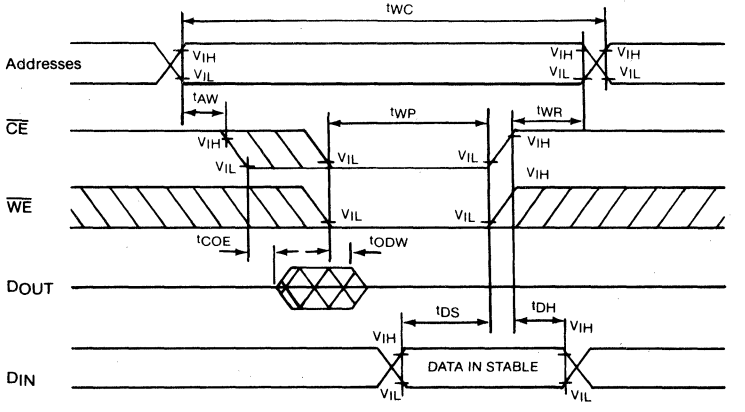
## READ CYCLE (1)



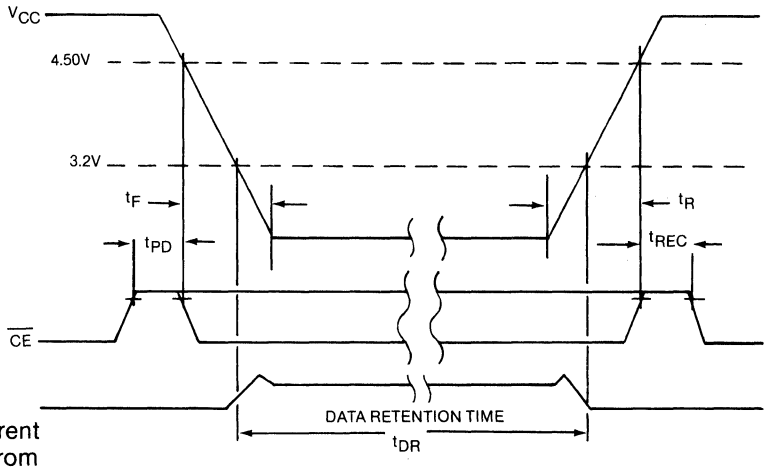

## WRITE CYCLE 1 (2), (6), (7)




## WRITE CYCLE 2 (2), (8)



## POWER-DOWN/POWER-UP CONDITION




Leakage Current
$I_L$ supplied from
lithium cell

5

## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | $\mu$s | |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 100 | | $\mu$s | |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | $\mu$s | |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power Up | | 2 | ms | |

($t_A$ = 25°C)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 10 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH}$ = 20ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1220Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.

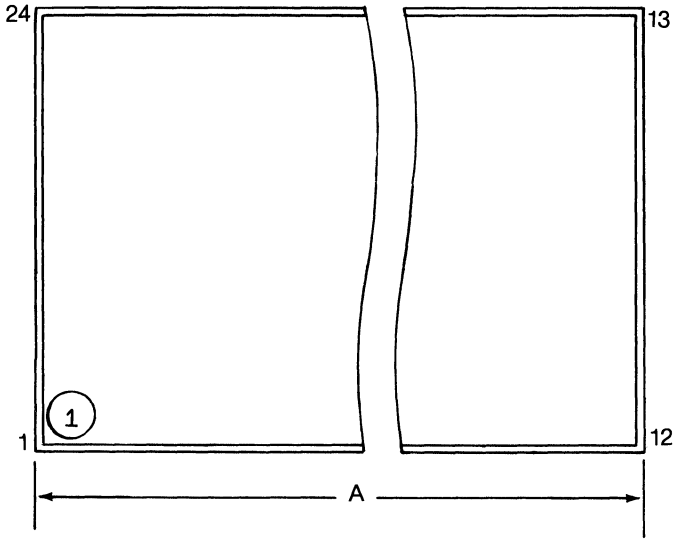
**D.C. Test Conditions**

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

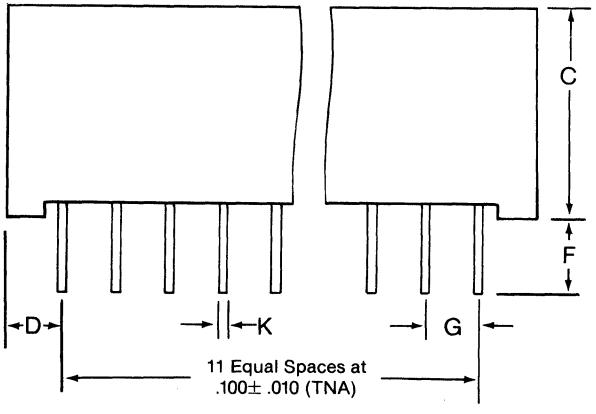
**A.C. Test Conditions**

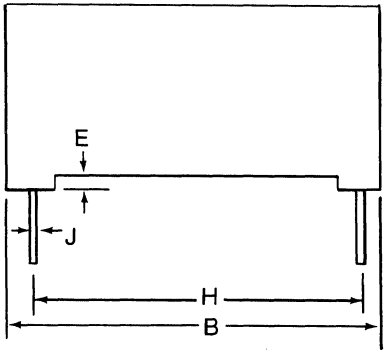
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

# DS1220Y
# Nonvolatile RAM




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.320 | 1.340 |
| B | .695 | .720 |
| C | .395 | .410 |
| D | .090 | .130 |
| E | .020 | .030 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |



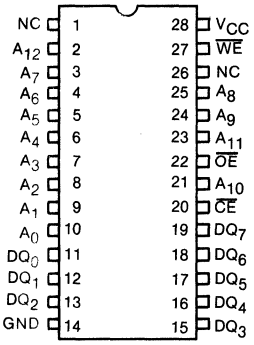



# Dallas Semiconductor
## *64K Nonvolatile Static RAM*

## *DS1225AB*
## *DS1225AD*

### FEATURES
- Data retention in the absence of $V_{CC}$
- Data is automatically protected during power loss
- Directly replaces 8K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in either 170 or 200 ns read access time
- Read cycle time equals write cycle time
- Optional 5% and 10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $A_0$-$A_{12}$ | - Address Inputs |
| $\overline{CE}$ | - Chip Enable |
| GND | - Ground |
| $DQ_0$-$DQ_7$ | - Data In/Data Out |
| $V_{CC}$ | - Power (+5V) |
| $\overline{WE}$ | - Write Enable |
| $\overline{OE}$ | - Output Enable |
| NC | - No Connect |

### DESCRIPTION
The DS1225AB and DS1225AD are 65,536-bit, fully static, nonvolatile RAMs organized as 8192 words by 8 bits. Each nonvolatile static RAM has a self-contained lithium energy source and control circuitry which constantly monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 8K × 8 static RAM directly conforming to the popular byte wide 28-pin DIP standard. The DS1225AB also matches the pinout of the 2764 EPROM or the 2864 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

## OPERATION

### READ MODE

The DS1225AB and DS1225AD execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs ($A_0$-$A_{12}$) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access.

### WRITE MODE

The DS1225AB and DS1225AD are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

### DATA RETENTION MODE

The DS1225AB provides full functional capability for $V_{CC}$ greater than 4.75 volts and write protects by 4.5V. The DS1225AD provides full functional capability for $V_{CC}$ greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The nonvolatile static RAM constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts for the DS1225AD and 4.75 volts for the DS1225AB.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| DS1225AB Power Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V | |
| DS1225AD Power Supply Voltage | $V_{CC}$ | 4.50 | 5.0 | 5.5 | V | |
| Input Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | |
| Input Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | |

**D.C. ELECTRICAL CHARACTERISTICS**

(0°C to 70°C, $V_{CC}=5V\pm10\%$ for DS1225AD)
(0°C to 70°C, $V_{CC}=5V\pm5\%$ for DS1225AB)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −1.0 | | +1.0 | *u*A | |
| I/O Leakage Current | $I_{LO}$ | −1.0 | | +1.0 | *u*A | |
| Output Current @2.4V | $I_{OH}$ | −1.0 | | | mA | |
| Output Current @0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}=2.2V$ | $I_{CCS1}$ | | 3.0 | 5.0 | mA | |
| Standby Current $\overline{CE}=V_{CC}-0.5V$ | $I_{CCS2}$ | | 5.0 | 10.0 | mA | |
| Operating Current | $I_{CC01}$ | | | 50 | mA | |
| Write Protection Voltage (DS1225AB) | $V_{TP}$ | 4.5 | 4.62 | 4.75 | V | |
| Write Protection Voltage (DS1225AD) | $V_{TP}$ | 4.25 | 4.37 | 4.5 | V | |

## CAPACITANCE

($t_A = 25°C$)

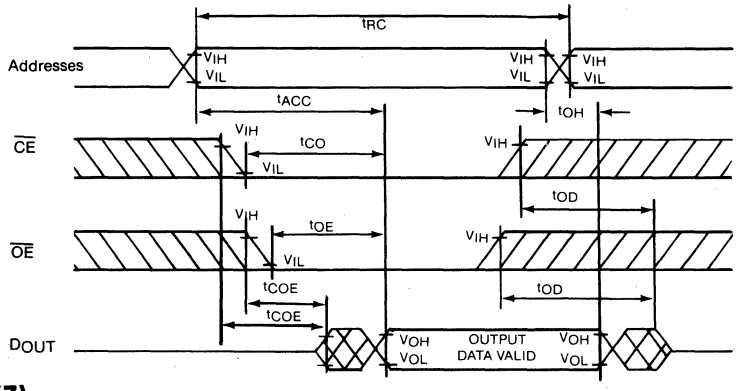
| PARAMETER | SYMBOL | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | 5 | 10 | pF | |

## A.C. ELECTRICAL CHARACTERISTICS

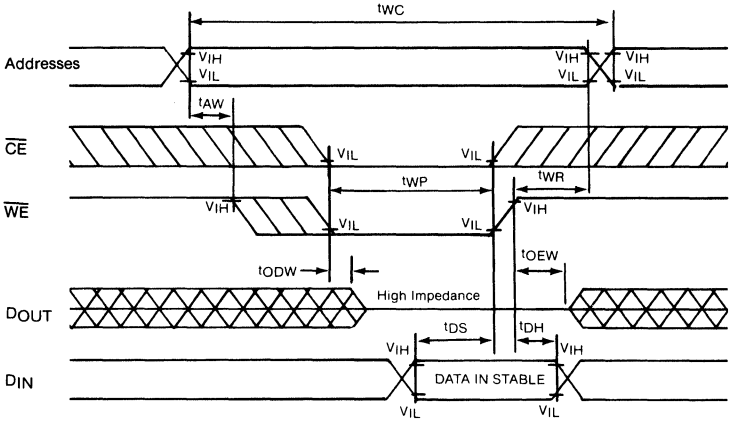
(0°C to 70°C, $V_{CC} = 5.0V \pm 10\%$ for DS1225AD)
(0°C to 70°C, $V_{CC} = 5.0V \pm 5\%$ for DS1225AB)

| | | DS1225AD-170 DS1225AB-170 | | DS1225AD-200 DS1225AB-200 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Read Cycle Time | $t_{RC}$ | 170 | | 200 | | ns | |
| Access Time | $t_{ACC}$ | | 170 | | 200 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 80 | | 100 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | 170 | | 200 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 10 | | 10 | | ns | |
| Output High Z from Deselection | $t_{OD}$ | | 70 | | 100 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | 10 | | ns | |
| Write Cycle Time | $t_{WC}$ | 170 | | 200 | | ns | |
| Write Pulse Width | $t_{WP}$ | 120 | | 150 | | ns | 3 |
| Address Set Up Time | $t_{AW}$ | 0 | | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 10 | | 10 | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | 70 | | 80 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 10 | | 10 | | ns | |
| Data Setup Time | $t_{DS}$ | 70 | | 80 | | ns | 4 |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | ns | 4,5 |

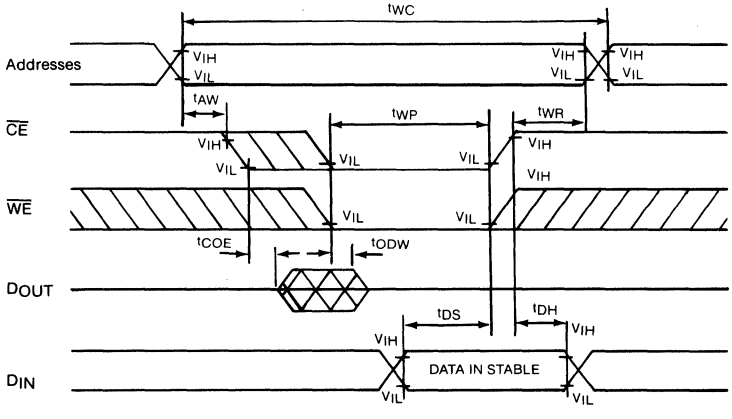
## READ CYCLE (1)



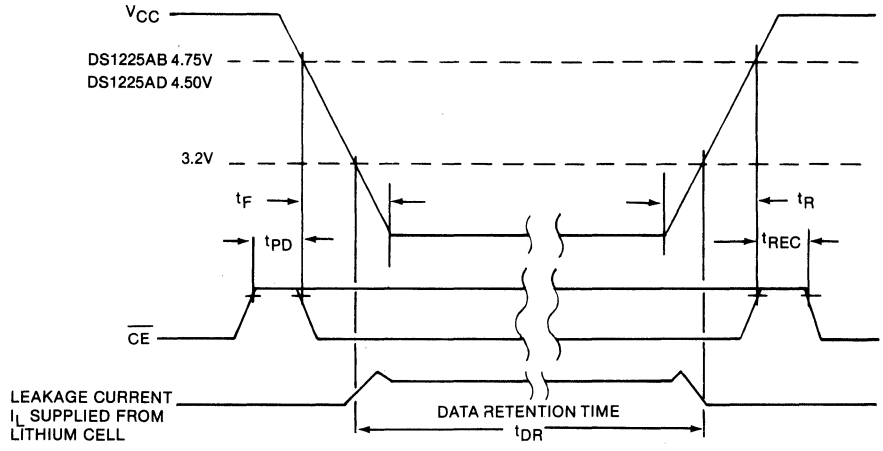

## WRITE CYCLE 1 (2), (6), (7)




## WRITE CYCLE 2 (2), (8)



## POWER-DOWN/POWER-UP CONDITION

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## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | *us* | |
| $t_F$ | $V_{CC}$ slew from 4.75V to 0V ($\overline{CE}$ at $V_{IH}$) | 300 | | *us* | DS1225AB |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 300 | | *us* | DS1225AD |
| $t_R$ | $V_{CC}$ slew from 0V to 4.75V ($\overline{CE}$ at $V_{IH}$) | 0 | | *us* | DS1225AB |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | *us* | DS1225AD |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power-Up | 2 | 125 | ms | |

($t_A = 25°C$)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 10 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1225AB is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.

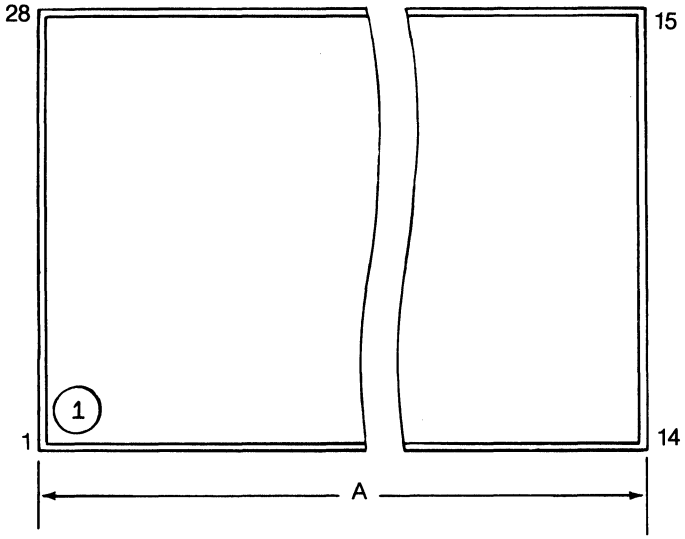
**D.C. TEST CONDITIONS**

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

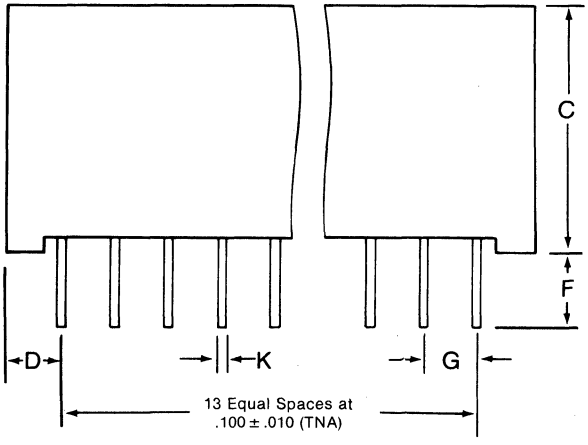
**A.C. TEST CONDITIONS**

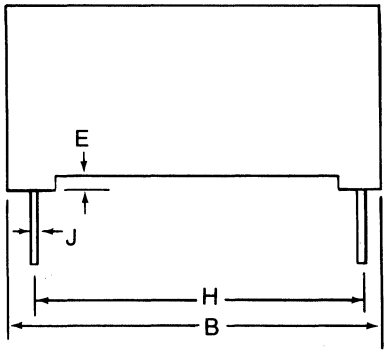
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

# DS1225AD
# DS1225AB
# 64K Nonvolatile RAM




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.520 | 1.540 |
| B | .695 | .720 |
| C | .395 | .410 |
| D | .090 | .120 |
| E | .020 | .030 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |

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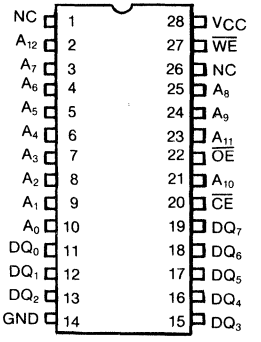
# Dallas Semiconductor
## 64K Nonvolatile Static RAM

## DS1225Y

### FEATURES
- Data retention in the absence of $V_{CC}$
- Data is automatically protected during power loss
- Directly replaces 8K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in either 170 or 200 ns read access time
- Read cycle time equals write cycle time
- Full ±10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $A_0$-$A_{12}$ | - Address Inputs |
| $\overline{CE}$ | - Chip Enable |
| GND | - Ground |
| $DQ_0$-$DQ_7$ | - Data In/Data Out |
| $V_{CC}$ | - Power (+5V) |
| $\overline{WE}$ | - Write Enable |
| $\overline{OE}$ | - Output Enable |
| NC | - No Connect |

### DESCRIPTION
The DS1225Y is a 65,536-bit, fully static, nonvolatile RAM organized as 8192 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 8K × 8 static RAM directly conforming to the popular byte wide 28-pin DIP standard. The DS1225Y also matches the pinout of the 2764 EPROM or the 2864 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

## OPERATION

### READ MODE

The DS1225Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 13 address inputs ($A_0$-$A_{12}$) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access.

### WRITE MODE

The DS1225Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

### DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for $V_{CC}$ greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The DS1225Y constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | |
| Input Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | |
| Input Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}=5V\pm10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −1.0 | | +1.0 | *u*A | |
| I/O Leakage Current | $I_{LO}$ | −1.0 | | +1.0 | *u*A | |
| Output Current @2.4V | $I_{OH}$ | −1.0 | | | mA | |
| Output Current @0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}=2.2V$ | $I_{CCS1}$ | | 3.0 | 7.0 | mA | |
| Standby Current $\overline{CE}=V_{CC}-0.5V$ | $I_{CCS2}$ | | 2.0 | 4.0 | mA | |
| Operating Current | $I_{CC01}$ | | | 50 | mA | |
| Write Protection Voltage | $V_{TP}$ | | 4.25 | | V | |

## CAPACITANCE

($t_A = 25°C$)

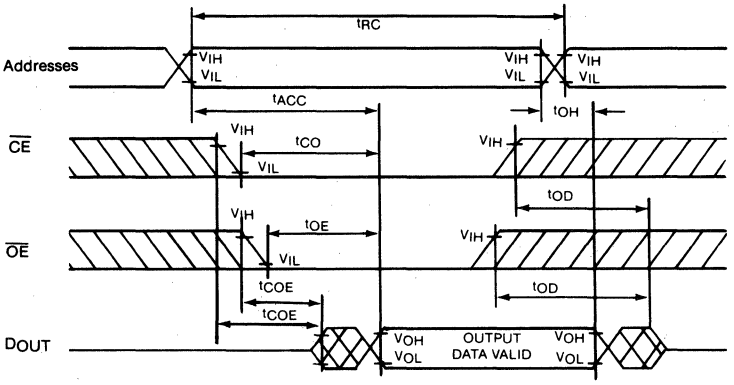
| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | 5 | 10 | pF | |

## A.C. ELECTRICAL CHARACTERISTICS

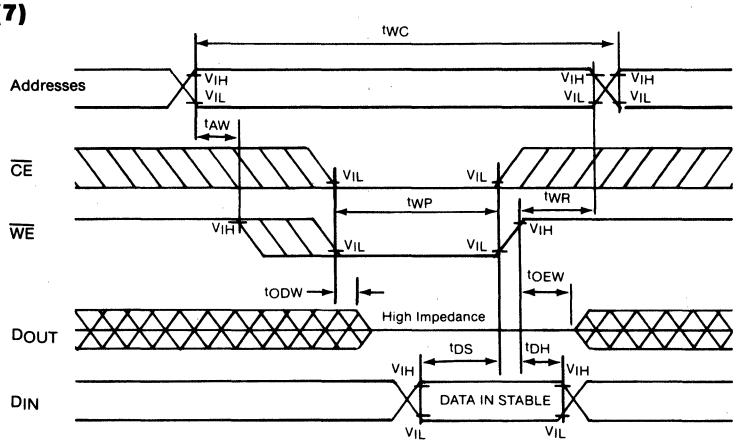
(0 °C to 70 °C, $V_{CC} = 5.0V \pm 10\%$)

| | | DS1225Y-170 | | DS1225Y-200 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Read Cycle Time | $t_{RC}$ | 170 | | 200 | | ns | |
| Access Time | $t_{ACC}$ | | 170 | | 200 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 80 | | 100 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | 170 | | 200 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 10 | | 10 | | ns | |
| Output High Z from Deselection | $t_{OD}$ | | 70 | | 100 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | 10 | | ns | |
| Write Cycle Time | $t_{WC}$ | 170 | | 200 | | ns | |
| Write Pulse Width | $t_{WP}$ | 120 | | 150 | | ns | 3 |
| Address Set Up Time | $t_{AW}$ | 0 | | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 10 | | 10 | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | 70 | | 80 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 10 | | 10 | | ns | |
| Data Setup Time | $t_{DS}$ | 70 | | 80 | | ns | 4 |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | ns | 4,5 |

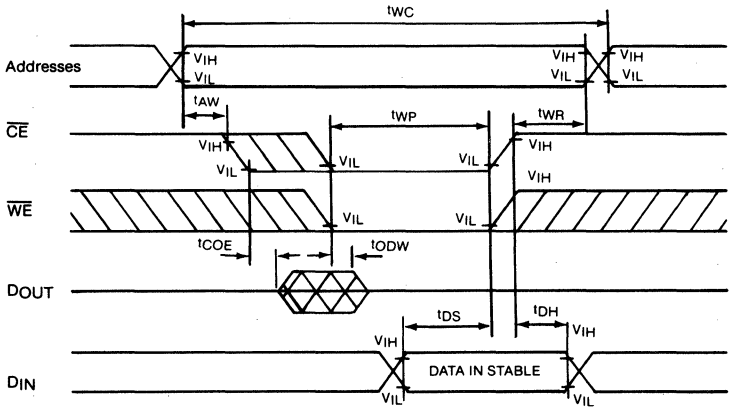
## READ CYCLE (1)



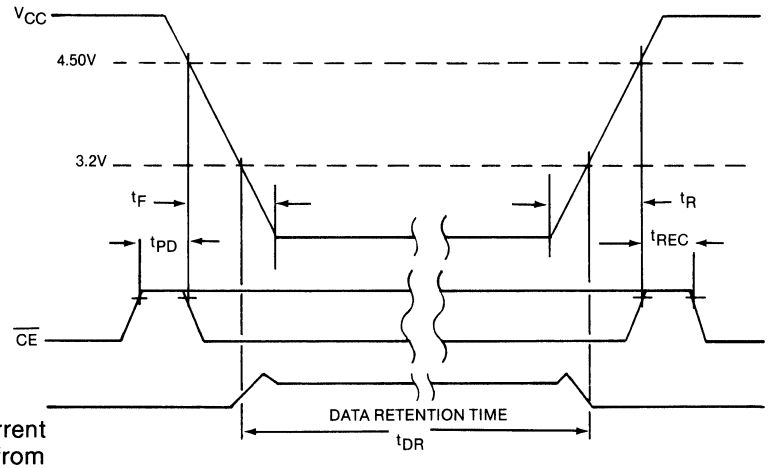

## WRITE CYCLE 1 (2), (6), (7)




## WRITE CYCLE 2 (2), (8)



## POWER-DOWN/POWER-UP CONDITION




Leakage Current
$I_L$ supplied from
lithium cell

5

## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | $\mu$s | |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 100 | | $\mu$s | |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | $\mu$s | |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power Up | | 2 | ms | |

($t_A$ = 25°C)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 10 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ low transition, the output buffers remain in high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1225Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.

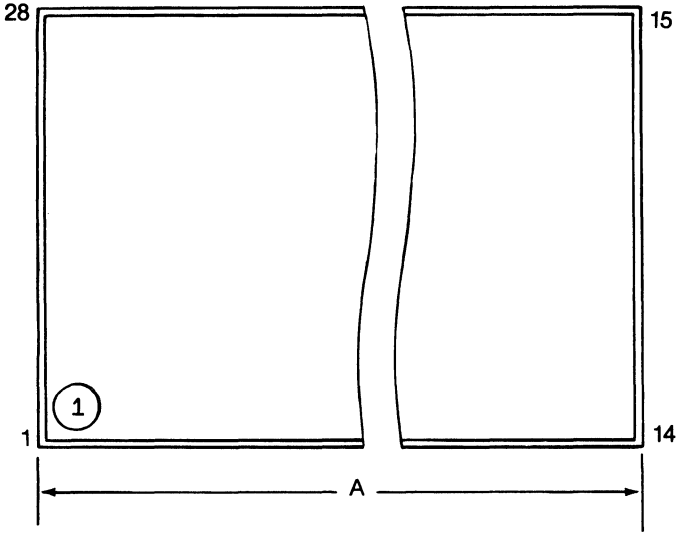
**D.C. Test Conditions**

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

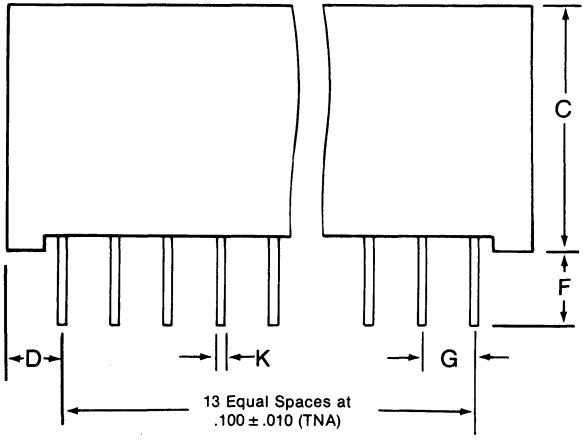
**A.C. Test Conditions**

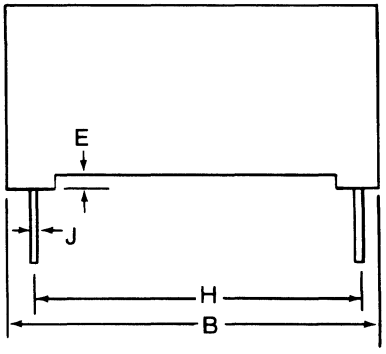
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

# DS1225Y
# 64K Nonvolatile RAM




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.520 | 1.540 |
| B | .695 | .720 |
| C | .395 | .410 |
| D | .090 | .120 |
| E | .020 | .030 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |



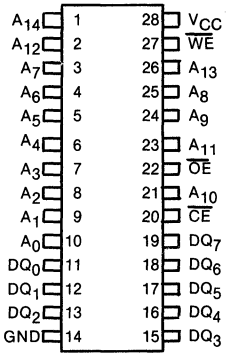



# Dallas Semiconductor
## *256K Nonvolatile Static RAM*

PRELIMINARY
**DS1230Y**
**DS1230AB**

### FEATURES
- Data retention in the absence of $V_{CC}$
- Data is automatically protected during power loss
- Directly replaces 32K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS - low power operation
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in either 55, 70, or 100 ns read access time
- Read cycle time equals write cycle time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of −40°C to +85°C, designated IND

### PIN CONNECTIONS




### PIN NAMES
$A_0$-$A_{14}$ - Address Inputs
$\overline{CE}$ - Chip Enable
GND - Ground
$DQ_0$-$DQ_7$ - Data In/Data Out
$V_{CC}$ - Power (+5V)
$\overline{WE}$ - Write Enable
$\overline{OE}$ - Output Enable

### DESCRIPTION
The DS1230AB and DS1230Y are 262,144-bit, fully static, nonvolatile RAMs organized as 32,768 words by 8 bits. Each nonvolatile static RAM has a self-contained lithium energy source and control circuitry which constantly monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 32K × 8 static RAM directly conforming to the popular byte wide 28-pin DIP standard. The DS1230AB also matches the pinout of the 28256 EEPROM allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

## OPERATION

### READ MODE

The DS1230AB and DS1230Y execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 15 address inputs ($A_0$-$A_{14}$) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access.

### WRITE MODE

The DS1230AB and DS1230Y are in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

### DATA RETENTION MODE

The DS1230AB provides full functional capability for $V_{CC}$ greater than 4.75 volts and write protects by 4.5V. The DS1230Y provides full functional capability for $V_{CC}$ greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The nonvolatile static RAM constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all outputs are high impedance. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts for the DS1230Y and 4.75 volts for the DS1230AB.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| DS1230AB Power Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V | |
| DS1230Y Power Supply Voltage | $V_{CC}$ | 4.50 | 5.0 | 5.5 | V | |
| Input Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | |
| Input Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | |

**D.C. ELECTRICAL CHARACTERISTICS**

(0°C to 70°C, $V_{CC}=5V\pm10\%$ for DS1230Y)
(0°C to 70°C, $V_{CC}=5V\pm5\%$ for DS1230AB)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −1.0 | | +1.0 | *u*A | |
| I/O Leakage Current | $I_{LO}$ | −1.0 | | +1.0 | *u*A | |
| Output Current @2.4V | $I_{OH}$ | −1.0 | | | mA | |
| Output Current @0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}=2.2V$ | $I_{CCS1}$ | | 3.0 | 5.0 | mA | |
| Standby Current $\overline{CE}$ $V_{CC}-0.5V$ | $I_{CCS2}$ | | | 15 | mA | |
| Operating Current | $I_{CC01}$ | | | 120 | mA | |
| Write Protection Voltage (DS1230AB) | $V_{TP}$ | 4.5 | 4.62 | 4.75 | V | |
| Write Protection Voltage (DS1230Y) | $V_{TP}$ | 4.25 | 4.37 | 4.5 | V | |

## CAPACITANCE

($t_A = 25°C$)

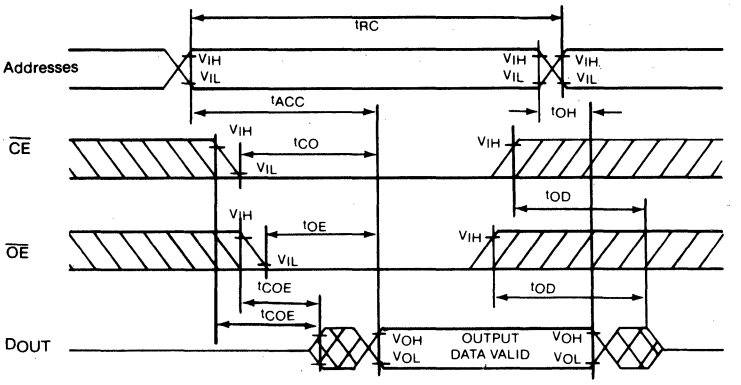
| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | 5 | 10 | pF | |

## A.C. ELECTRICAL CHARACTERISTICS

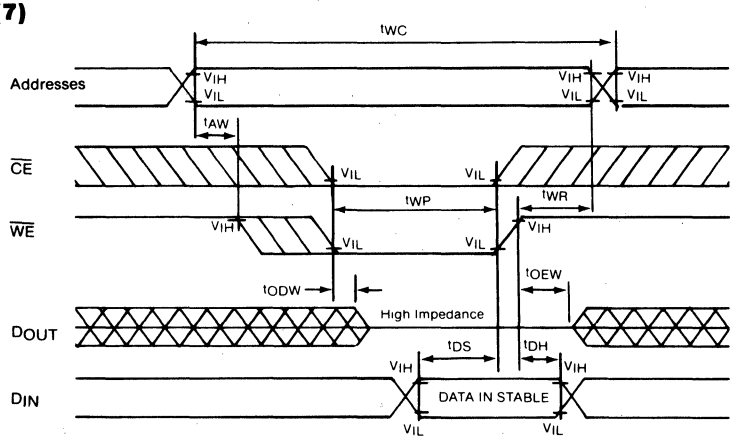
(0°C to 70°C, $V_{CC} = 5.0V \pm 10\%$ for DS1230Y)
(0°C to 70°C, $V_{CC} = 5.0V \pm 5\%$ for DS1230AB)

| | | DS1230Y-55 DS1230AB-55 | | DS1230Y-70 DS1230AB-70 | | DS1230Y-100 DS1230AB-100 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Read Cycle Time | $t_{RC}$ | 45 | | 70 | | 100 | | ns | |
| Access Time | $t_{CO}$ | | 45 | | 70 | | 100 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 20 | | 30 | | 50 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | 45 | | 70 | | 100 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 5 | | 5 | | 5 | | ns | |
| Output High Z From Deselection | $t_{OD}$ | | 15 | | 30 | | 35 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | 10 | | 10 | | ns | |
| Write Cycle Time | $t_{WC}$ | 45 | | 70 | | 100 | | ns | |
| Write Pulse Width | $t_{WP}$ | 25 | | 55 | | 75 | | ns | 3 |
| Address Set-Up Time | $t_{AW}$ | 0 | | 0 | | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 0 | | 0 | | 0 | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | 20 | | 30 | | 35 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 5 | | 5 | | 5 | | ns | 8 |
| Data Set-Up Time | $t_{DS}$ | 40 | | 40 | | 40 | | ns | 4 |
| Data Hold Time From $\overline{WE}$ | $t_{DH}$ | 0 | | 0 | | 0 | | ns | 4,5 |

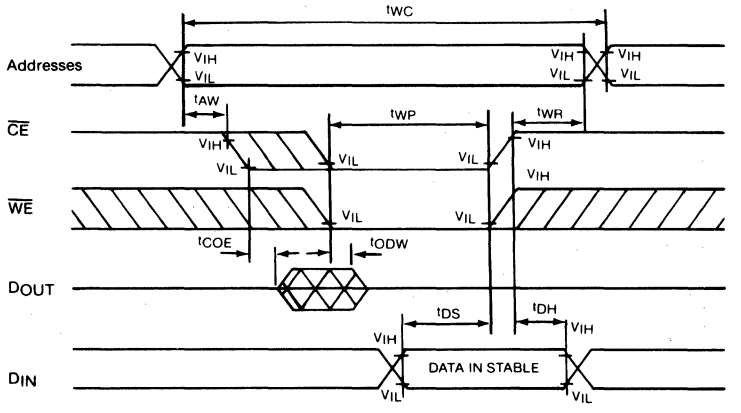
## READ CYCLE (1)



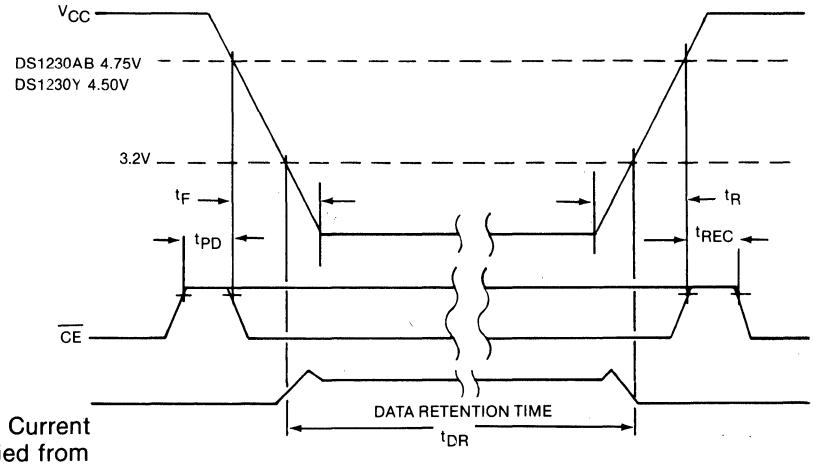

## WRITE CYCLE 1 (2), (6), (7)




## WRITE CYCLE 2 (2), (8)



## POWER-DOWN/POWER-UP CONDITION




Leakage Current $I_L$ supplied from lithium cell

5

## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | *us* | |
| $t_F$ | $V_{CC}$ slew from 4.75V to 0V ($\overline{CE}$ at $V_{IH}$) | 300 | | *us* | DS1230AB |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 300 | | *us* | DS1230Y |
| $t_R$ | $V_{CC}$ slew from 0V to 4.75V ($\overline{CE}$ at $V_{IH}$) | 0 | | *us* | DS1230AB |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | *us* | DS1230Y |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power-Up | 2 | 125 | ms | |

($t_A = 25°C$)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 10 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1230AB or DS1230Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.

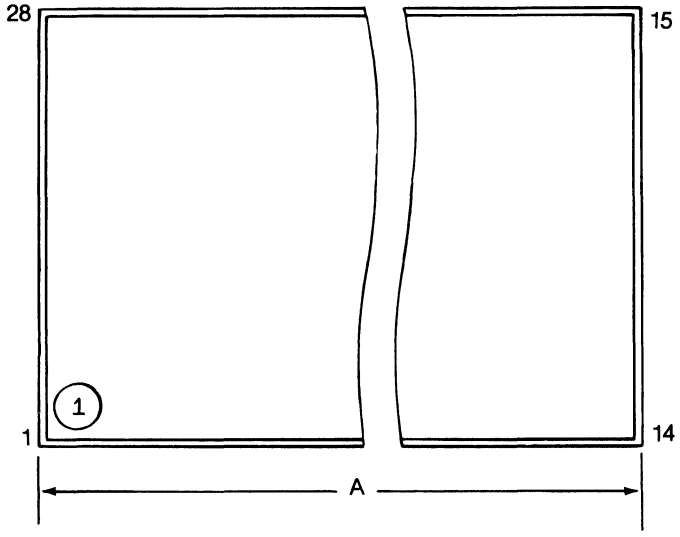
**D.C. Test Conditions**

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

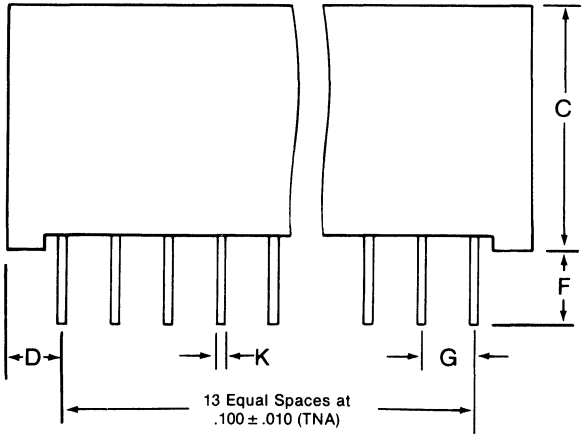
**A.C. Test Conditions**

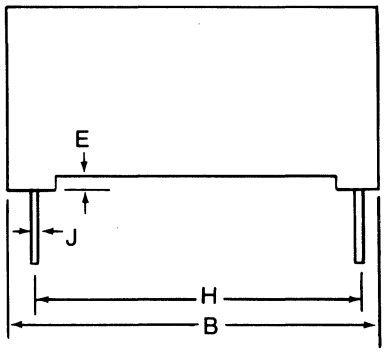
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

# DS1230Y
# DS1230AB
# 256K Nonvolatile RAM




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.520 | 1.540 |
| B | .695 | .720 |
| C | .395 | .410 |
| D | .090 | .120 |
| E | .020 | .030 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |




5

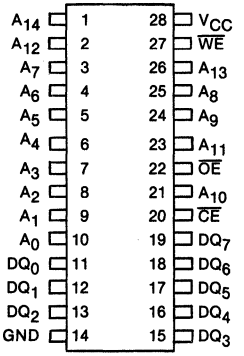
# Dallas Semiconductor
# 256K Nonvolatile Static RAM

# DS1235Y
# DS1235AB

## FEATURES

- Data retention in the absence of $V_{CC}$
- Data is automatically protected during power loss
- Directly replaces 32K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS—low power operation
- Standard 28-pin JEDEC pinout
- Available in either 120, 150, or 200 ns read access time
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1235Y)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% operating range (DS1235AB)

## PIN CONNECTIONS




## PIN NAMES

| | |
|---|---|
| $A_0$-$A_{14}$ | - Address Inputs |
| $\overline{CE}$ | - Chip Enable |
| GND | - Ground |
| $DQ_0$-$DQ_7$ | - Data In/Data Out |
| $V_{CC}$ | - Power (+5V) |
| $\overline{WE}$ | - Write Enable |
| $\overline{OE}$ | - Output Enable |

## DESCRIPTION

The DS1235Y is a 262,144-bit, full-static, nonvolatile SRAM organized as 32,768 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 32K × 8 static RAM directly conforming to the popular byte wide 28256 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

## OPERATION

### READ MODE

The DS1235Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 15 address inputs ($A_0$-$A_{14}$) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$, rather than address access.

### WRITE MODE

The DS1235Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{OWD}$ from its falling edge.

### DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for $V_{CC}$ greater than 4.5 volts and write protects at 4.37 V nominal ($V_{CC}$ greater than 4.75 V and write protect at 4.62 V nominal for DS1235AB). Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The DS1235Y constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all the outputs are high impedance. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts (4.75 volts for DS1235AB).

The DS1235Y is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When $V_{CC}$ is applied at a level of greater than 4.25 volts, the lithium energy source is switched on such that energy will be supplied to RAM when $V_{CC}$ is less than approximately 3.0 volts. The lithium energy source can be subsequently turned off by taking $V_{CC}$ to a negative 3 volts for 1 ms.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | |
| Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | |
| Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}=5V\pm10\%$ for DS1235Y) (0°C to 70°C, $V_{CC}=5V\pm5\%$ for DS1235AB)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −1.0 | | +1.0 | uA | |
| I/O Leakage Current | $I_{LO}$ | −5.0 | | +5.0 | uA | |
| Output Current @2.4V | $I_{OH}$ | −1.0 | | | mA | |
| Output Current @0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}=2.2V$ | $I_{DDS1}$ | | 3.0 | 5.0 | mA | |
| Standby Current $\overline{CE}=V_{CC}-0.5V$ | $I_{DDS2}$ | | 5.0 | 10.0 | mA | |
| Operating Current | $I_{DD}$ | | | 85 | mA | |
| Write Protection Voltage (DS1235Y) | $V_{TP}$ | 4.25 | 4.37 | 4.5 | V | |
| Write Protection Voltage (DS1235AB) | $V_{TP}$ | 4.50 | 4.62 | 4.75 | V | |

**CAPACITANCE** ($t_A=25°C$)

| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | 5 | 10 | pF | |

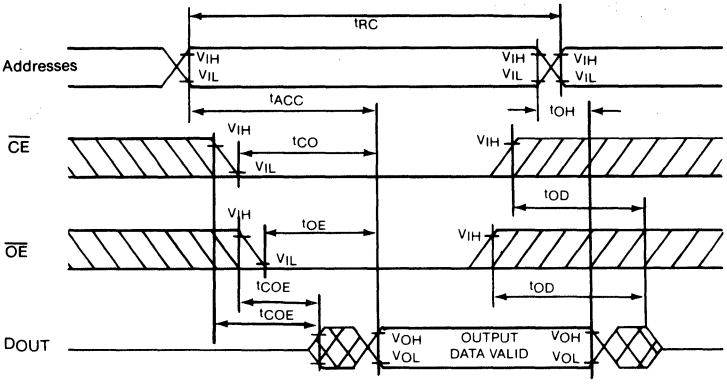
## A.C. ELECTRICAL CHARACTERISTICS

(0 °C to 70 °C, $V_{CC}$ = 5.0V ± 10% for DS1235Y)
(0 °C to 70 °C, $V_{CC}$ = 5.0V ± 5% for DS1235AB)

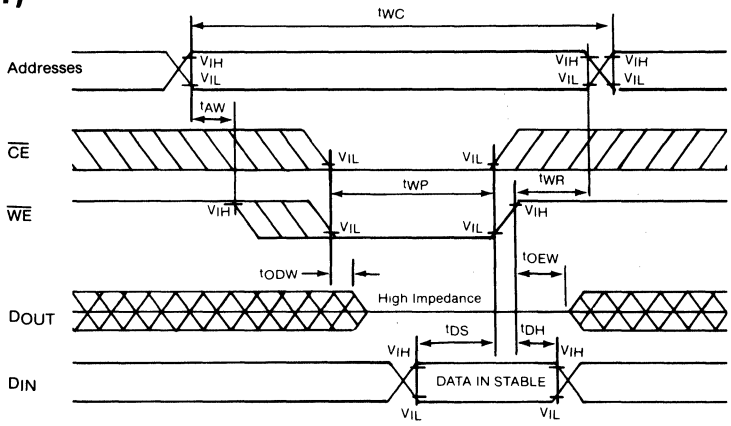
| | | DS1235Y-120 | | DS1235Y-150 | | DS1235Y-200 | | | |
|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Read Cycle Time | $t_{RC}$ | 120 | | 150 | | 200 | | ns | |
| Access Time | $t_{CO}$ | | 120 | | 150 | | 200 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 60 | | 70 | | 100 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | 120 | | 150 | | 200 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 5 | | 10 | | 10 | | ns | |
| Output High Z From Deselection | $t_{OD}$ | | 40 | | 70 | | 100 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | 10 | | 10 | | ns | |
| Write Cycle Time | $t_{WC}$ | 120 | | 150 | | 200 | | ns | |
| Write Pulse Width | $t_{WP}$ | 90 | | 100 | | 170 | | ns | 3 |
| Address Set-Up Time | $t_{AW}$ | 0 | | 0 | | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 0 | | 10 | | 10 | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | 40 | | 70 | | 80 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 5 | | 10 | | 10 | | ns | 8 |
| Data Set-Up Time | $t_{DS}$ | 50 | | 60 | | 80 | | ns | 4 |
| Data Hold Time From $\overline{WE}$ | $t_{DH}$ | 0 | | 0 | | 0 | | ns | 4,5 |

5

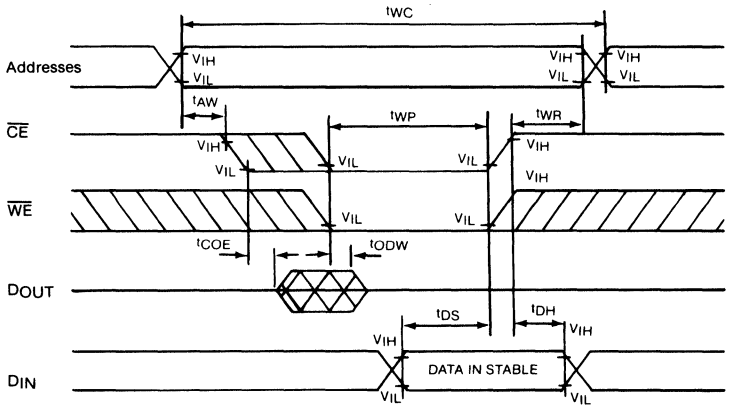
## READ CYCLE (1)



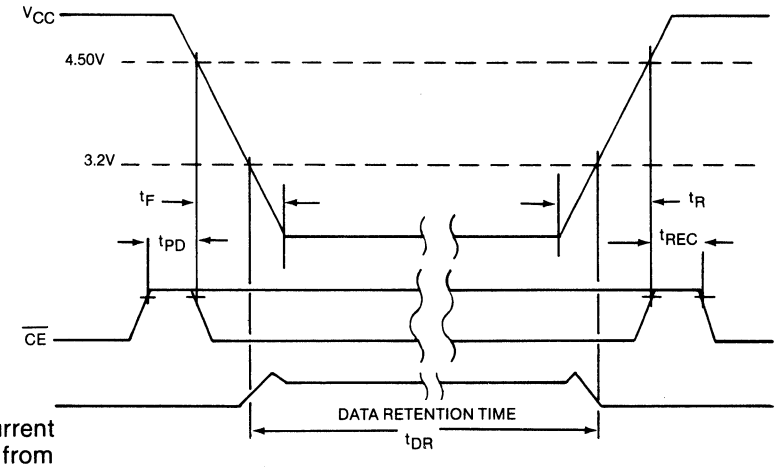

## WRITE CYCLE 1 (2), (6), (7)




## WRITE CYCLE 2 (2), (8)



## POWER-DOWN/POWER-UP CONDITION




Leakage Current
$I_L$ supplied from
lithium cell

5

## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | μs | |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 300 | | μs | |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | μs | |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power Up | 2 | 125 | ms | |

($t_A$ = 25°C)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 5 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH}$ = 20ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1235Y has a built-in switch which disconnects the lithium source until $V_{CC}$ is first applied by the user. The expected $t_{DR}$ is defined as accumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user.

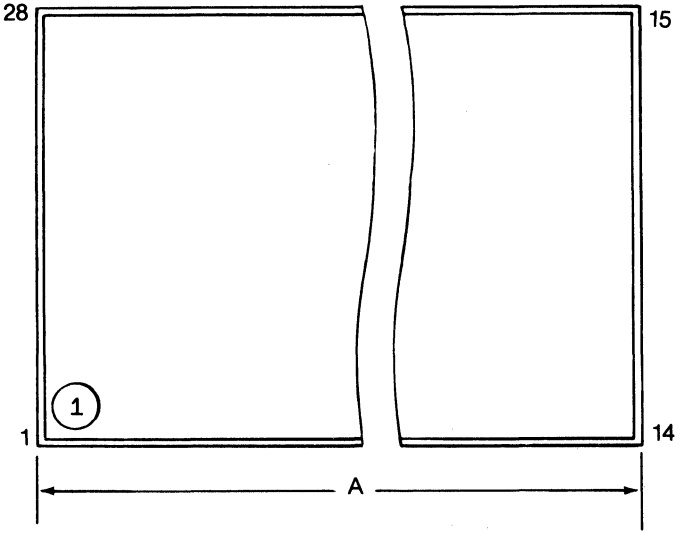
**D.C. Test Conditions**

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

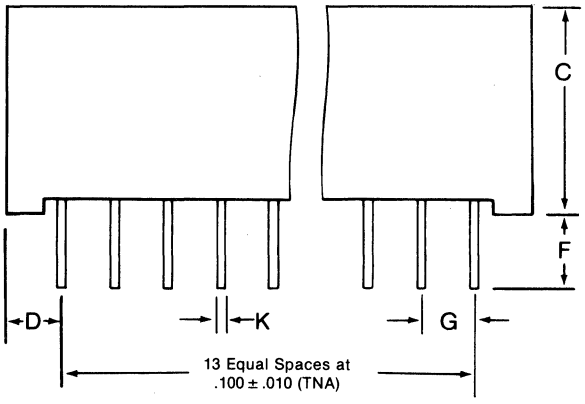
**A.C. Test Conditions**

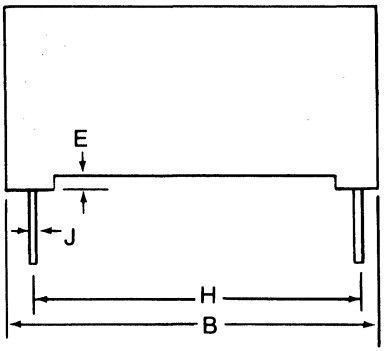
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

# DS1235Y
# 256K Nonvolatile RAM




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.520 | 1.540 |
| B | .695 | .720 |
| C | .395 | .410 |
| D | .090 | .120 |
| E | .020 | .030 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |



# Dallas Semiconductor
## *1024K Nonvolatile Static RAM*

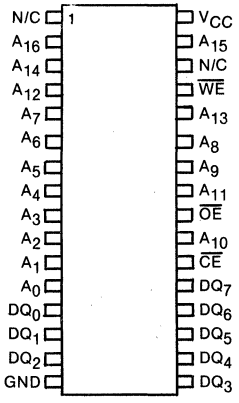
PRELIMINARY

**DS1245Y**
**DS1245AB**

### FEATURES

- Data retention in the absence of $V_{CC}$
- Data is automatically protected during power loss
- Directly replaces 128K × 8 volatile static RAM or EEPROM
- Unlimited write cycles
- CMOS—low power operation
- Standard 32-pin JEDEC pinout
- Available in either 70, 100 or 120 ns read access time
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1245Y)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% operating range (DS1245AB)

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $A_0$-$A_{16}$ | - Address Inputs |
| $\overline{CE}$ | - Chip Enable |
| GND | - Ground |
| $DQ_0DQ_7$ | - Data In/Data Out |
| $V_{CC}$ | - Power (+5V) |
| $\overline{WE}$ | - Write Enable |
| $\overline{OE}$ | - Output Enable |
| N/C | - No Connect |

### DESCRIPTION

The DS1245Y is a 1,048,576-bit full-static, nonvolatile SRAM organized as 131,072 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 128K × 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

## OPERATION

### READ MODE

The DS1245Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 17 address inputs ($A_0$-$A_{16}$) defines which of the 131,072 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that the $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_O$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$, rather than address access.

### WRITE MODE

The DS1245Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{OWD}$ from its falling edge.

### DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for $V_{CC}$ greater than 4.5 volts and write protects at 4.37 V nominal ($V_{CC}$ greater than 4.75 and write protect at 4.62 V nominal for DS1245AB). Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The DS1245Y constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM will automatically write protect itself and all inputs to the RAM become "don't care" and all the outputs are high impedance. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts (4.75 V for DS1245AB).

The DS1245Y is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When $V_{CC}$ is applied at a level of greater than 4.25 volts, the lithium energy source is switched on such that energy will be supplied to RAM when $V_{CC}$ is less than approximately 3.0 volts. The lithium energy source can be subsequently turned off by taking $V_{CC}$ to a negative 3 volts for 1 ms.

Battery redundancy is also provided to ensure reliability. The DS1245Y contains two lithium energy cells separated by an internal isolation switch. During battery back-up time the cell with the highest voltage is selected for use. If one battery fails, the other battery will automatically take over. The switch between batteries is transparent to the user.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | |
| Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | |
| Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}=5V\pm5\%$ for DS1245AB) (0°C to 70°C, $V_{CC}=5V\pm10\%$ for DS1245Y)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −1.0 | | +1.0 | uA | |
| I/O Leakage Current | $I_{LO}$ | −5.0 | | +5.0 | uA | |
| Output Current @2.4V | $I_{OH}$ | −1.0 | | | mA | |
| Output Current @0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}=2.2V$ | $I_{DDS1}$ | | 3.0 | 5.0 | mA | |
| Standby Current $\overline{CE}=V_{CC}-0.5V$ | $I_{DDS2}$ | | 5.0 | 10.0 | mA | |
| Operating Current | $I_{DD}$ | | | 85 | mA | |
| Write Protection Voltage (DS1245Y) | $V_{TP}$ | 4.25 | 4.37 | 4.5 | V | |
| Write Protection Voltage (DS1245AB) | $V_{TP}$ | 4.50 | 4.62 | 4.75 | V | |

## CAPACITANCE

($t_A = 25°C$)

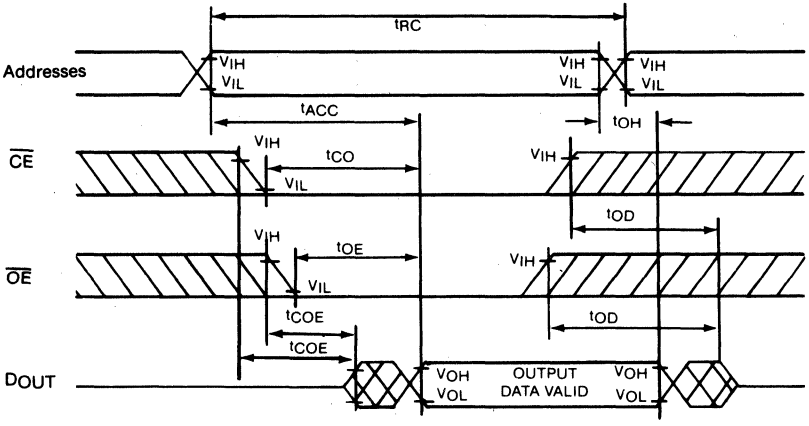
| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | 5 | 10 | pF | |

## A.C. ELECTRICAL CHARACTERISTICS

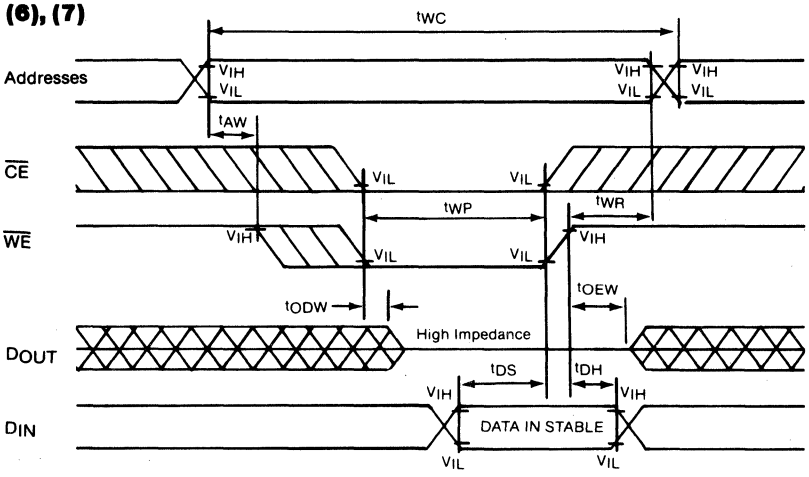
(0°C to 70°C, $V_{CC} = 5V \pm 5\%$ for DS1245AB)
(0°C to 70°C, $V_{CC} = 5V \pm 10\%$ for DS1245Y)

| | | DS1245Y-70 | | DS1245Y-100 | | DS1245Y-120 | | | |
|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Read Cycle Time | $t_{RC}$ | 70 | | 100 | | 120 | | ns | |
| Access Time | $t_{CO}$ | | 70 | | 100 | | 120 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 20 | | 50 | | 60 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | 70 | | 100 | | 120 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 5 | | 5 | | 5 | | ns | |
| Output High Z From Deselection | $t_{OD}$ | | 20 | | 35 | | 40 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | 10 | | 10 | | ns | |
| Write Cycle Time | $t_{WC}$ | 70 | | 100 | | 120 | | ns | |
| Write Pulse Width | $t_{WP}$ | 55 | | 75 | | 90 | | ns | 3 |
| Address Set-Up Time | $t_{AW}$ | 0 | | 0 | | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 10 | | 10 | | 10 | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | 30 | | 35 | | 40 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 5 | | 5 | | 5 | | ns | 8 |
| Data Set-Up Time | $t_{DS}$ | 40 | | 40 | | 50 | | ns | 4 |
| Data Hold Time From $\overline{WE}$ | $t_{DH}$ | 0 | | 0 | | 0 | | ns | 4,5 |

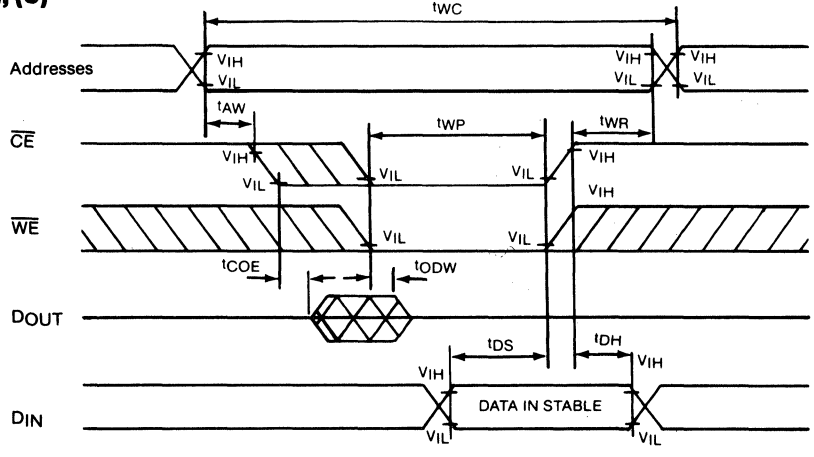
## READ CYCLE (1)



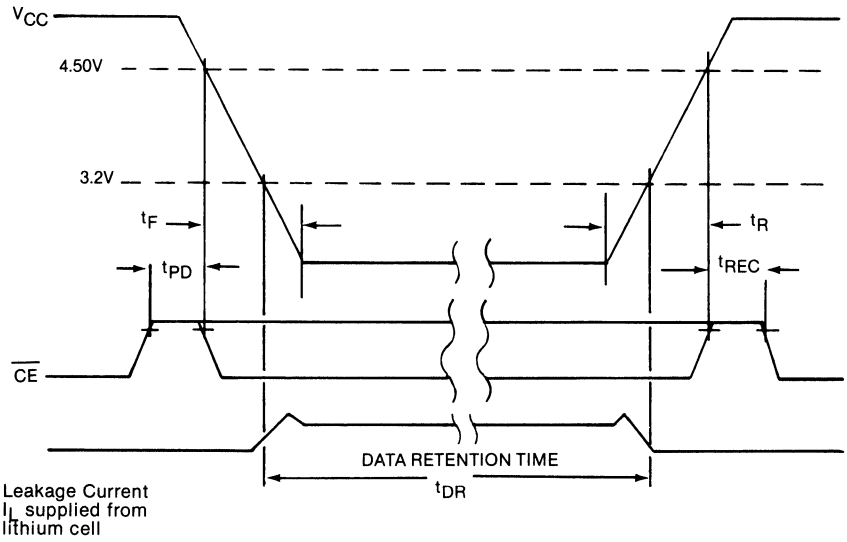

## WRITE CYCLE 1 (2), (6), (7)




## WRITE CYCLE 2 (2), (8)



## POWER-DOWN/POWER-UP CONDITION

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## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | us | |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 300 | | us | |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | us | |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power-Up | 2 | 125 | ms | |

($t_A = 25\,°C$)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 5 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ low transition, the output buffers remain in high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1245Y has a built-in switch which disconnects the lithium source until $V_{CC}$ is first applied by the user. The expected $t_{DR}$ is defined as accumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user.

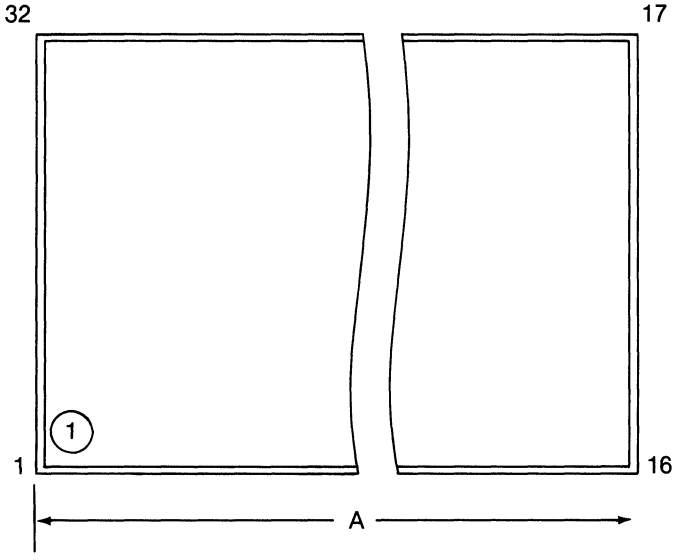
**D.C. Test Conditions**

Outputs Open
t Cycle = 200 ns
All Voltages Are Referenced to Ground

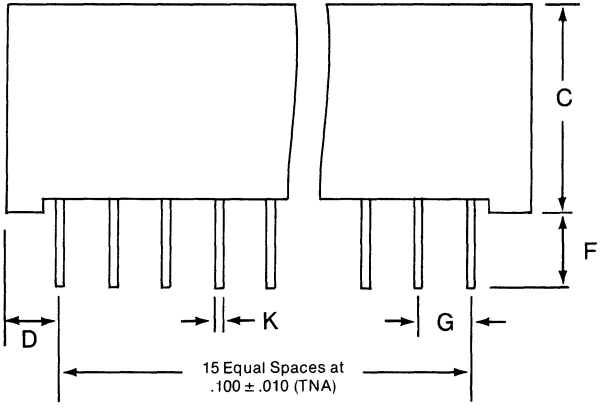
**A.C. Test Conditions**

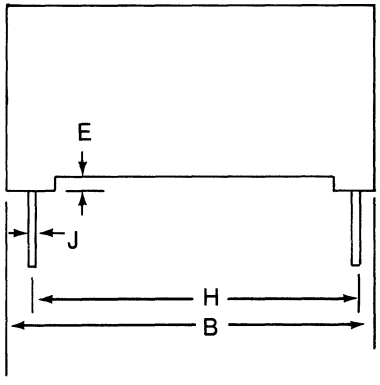
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

# DS1245Y
# 1024K Nonvolatile RAM




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.720 | 1.740 |
| B | .695 | .720 |
| C | .395 | .410 |
| D | .090 | .120 |
| E | .020 | .030 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |



# Intelligent Sockets

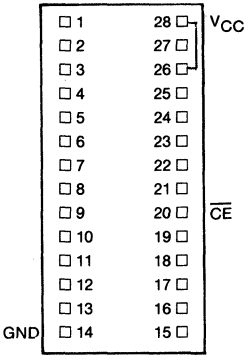
# Dallas Semiconductor

## *SmartSocket* — *DS1213*

### FEATURES

- Accepts standard 2K × 8 and 8K × 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 2K × 8 to 8K × 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0 °C to 70 °C

### PIN CONNECTIONS




### PIN NAMES

All pins pass through except 20, 26, 28.

Pin 20 $\overline{CE}$ - Conditioned Chip Enable
Pin 26 $V_{CC}$ - Switched $V_{CC}$ for 24-pin RAM
Pin 28 $V_{CC}$ - Switched $V_{CC}$ for 28-pin RAM
Pin 14 GND - Ground

### DESCRIPTION

The DS1213 is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either 28-pin 8K × 8 or 24-pin 2K × 8 lower-justified JEDEC byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 28, 26, 20 and 14 for RAM control. All other pins are passed straight through to the socket receptacle.

## OPERATION

The DS1213 SmartSocket performs five circuit functions required to battery back-up a CMOS memory. First, a switch is provided to direct power from the battery or $V_{CC}$ supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartSocket provides is power fail detection. Power fail detection occurs between 4.75 and 4.5 volts. The DS1213 constantly monitors the $V_{CC}$ supply. When $V_{CC}$ falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable. The third function accomplishes write protection by holding the chip enable signal to the memory to within 0.2 volts of VCC or battery supply. If the chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal will be passed through to the socket receptacle with a maximum propagation delay of 20 ns. The fourth function the DS1213 performs is to check battery status to warn of potential data loss. Each time that $V_{CC}$ power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function which the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to insure reliability. The DS1213 SmartSocket provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two lithium cells contains 35 mAhr capacity, making the total 70 mAhr.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| PIN 26 L, PIN 28 L Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.5 | V | 1,3 |
| Logic 1 PIN 20 L | $V_{IH}$ | 2.2 | | $V_{CC}$+0.3 | V | 1,3 |
| Logic 0 PIN 20 L | $V_{IL}$ | -0.3 | | +0.8 | V | 1,3 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 4.75 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| PIN 26 L, PIN 28 L Supply Current | $I_{CC}$ | | | 5 | mA | 3, 4, 5 |
| PIN 26 U, PIN 28 U Supply Voltage | $V_{CCO}$ | $V_{CC}$ -0.2 | | | V | 3, 8 |
| PIN 26 U, PIN 28 U Supply Current | $I_{CCO}$ | | | 80 | mA | 3, 8 |
| PIN 20 L $\overline{CE}$ Input Leakage | $I_{IL}$ | -1.0 | | +1.0 | $\mu$A | 3, 4 |
| PIN 20 U $\overline{CE}$ Output @ 2.4V | $I_{OH}$ | -1.0 | | | mA | 2, 3 |
| PIN 20 U $\overline{CE}$ Output @ .4V | $I_{OL}$ | | | 4.0 | mA | 2, 3 |

(0°C to 70°C, $V_{CC}$ < 4.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| PIN 20 U Output | $V_{OHL}$ | $V_{CC}$ -0.2<br>$V_{BAT}$ -0.2 | | | V | 3 |
| PIN 26 U, PIN 28 U Battery Current | $I_{BAT}$ | | | 1 | $\mu$A | 3, 6 |
| PIN 26 U, PIN 28 U Battery Voltage | $V_{BAT}$ | 2 | 3 | 3.6 | V | 3 |

**CAPACITANCE** ($t_A = 25\,°C$)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance PIN 20 L | $C_{IN}$ | 5 | pF | 3 |
| Output Capacitance PIN 20 U | $C_{OUT}$ | 7 | pF | 3 |

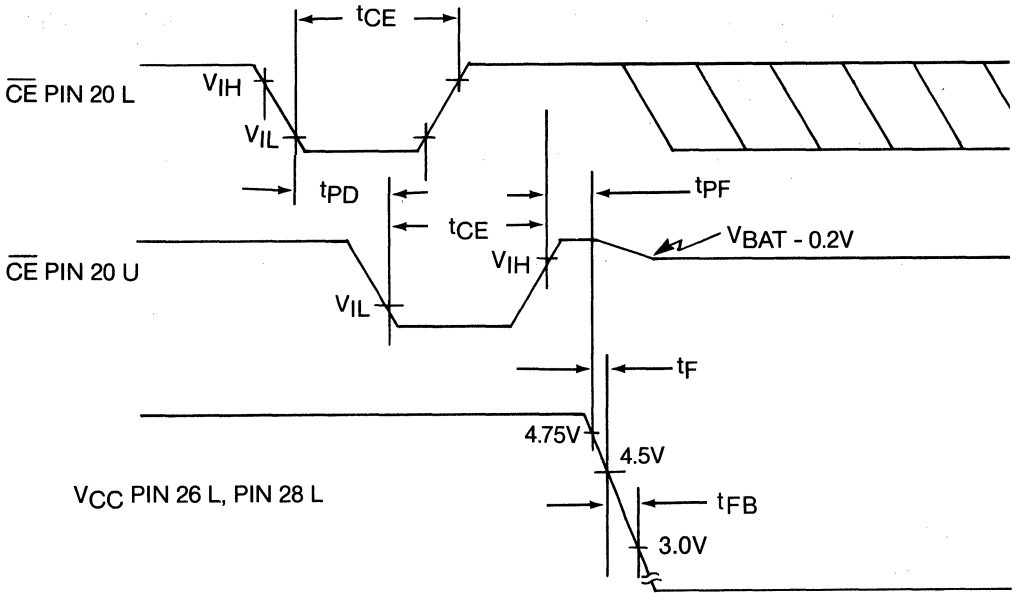
**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC} = 4.75$ to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ Propagation Delay | $t_{PD}$ | 5 | 10 | 20 | ns | 2,9 |
| $\overline{CE}$ High to Power Fail | $t_{PF}$ | | | 0 | ns | |

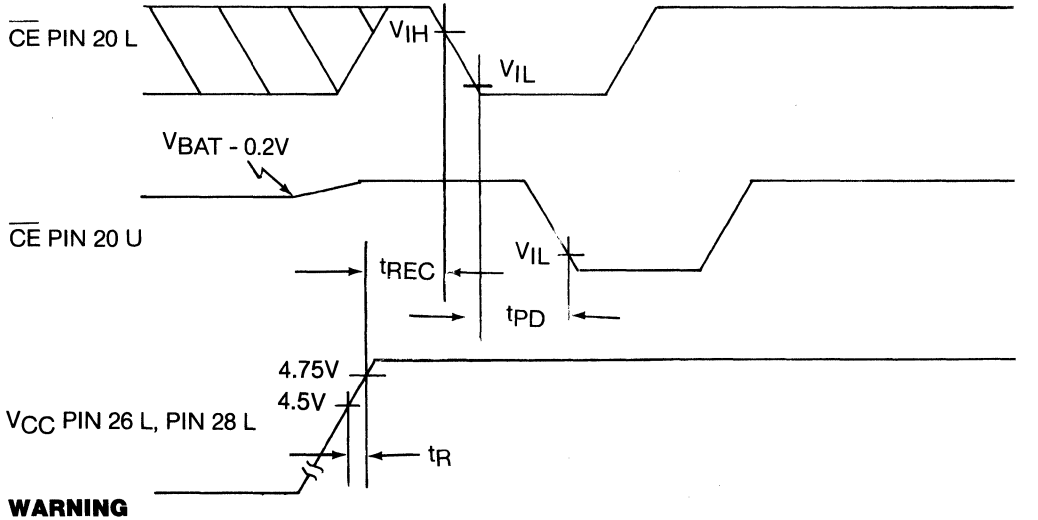
($0°$ to 70 °C, $V_{CC} = 4.75$ to 5.5 V)

| | | | | | | |
|---|---|---|---|---|---|---|
| Recovery at Power Up | $t_{REC}$ | 2 | 80 | 125 | ms | |
| $V_{CC}$ Slew Rate 4.75 - 4.5 V | $t_F$ | 300 | | | *u*s | |
| $V_{CC}$ Slew Rate 4.5 - 3 V | $t_{FB}$ | 10 | | | *u*s | |
| $V_{CC}$ Slew Rate 4.5 - 4.75 V | $t_R$ | 0 | | | *u*s | |
| $\overline{CE}$ Pulse Width | $t_{CE}$ | | | 1.5 | *u*s | 7 |

## TIMING DIAGRAM—POWER DOWN




## TIMING DIAGRAM—POWER UP




**WARNING**

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

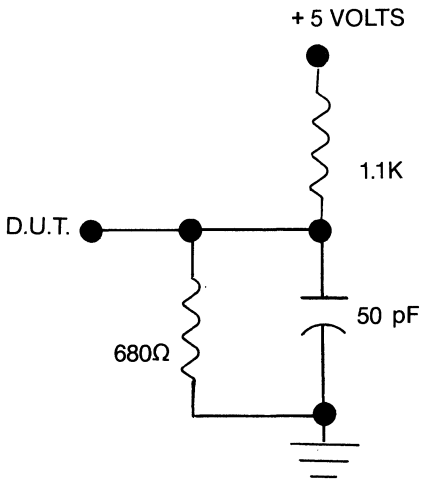
**NOTES:**

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26 L may be connected to $V_{CC}$ or left disconnected at the P.C. board.
6. $I_{BAT}$ is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. $t_{CE}$ max. must be met to insure data integrity on power loss.
8. $V_{CC}$ is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.

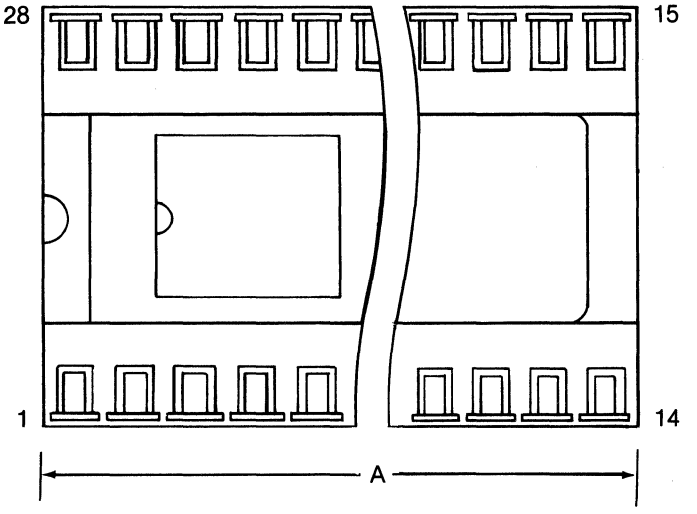


**OUTPUT LOAD**

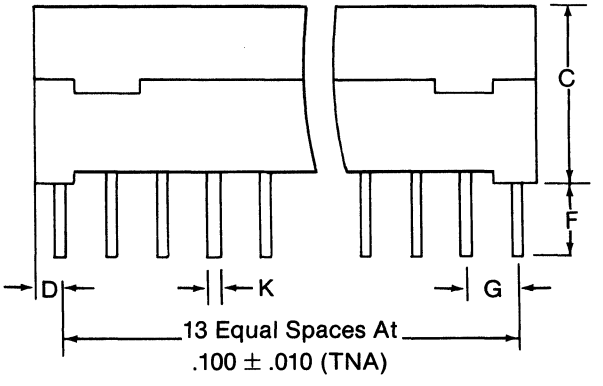
Figure 1

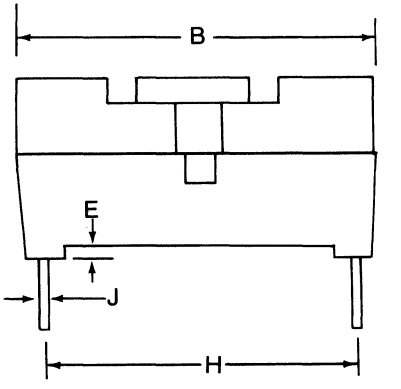


# DS1213
# SmartSocket




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.390 | 1.420 |
| B | .695 | .710 |
| C | .350 | .385 |
| D | .035 | .065 |
| E | .025 | .035 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |



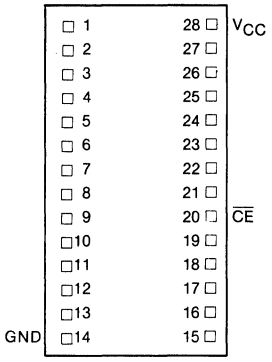
# Dallas Semiconductor
## *SmartSocket*

## *DS1213C*

### FEATURES

- Accepts standard 8K × 8 and 32K × 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 8K × 8 to 32K × 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

### PIN CONNECTIONS




### PIN DEFINITIONS

All pins pass through except 20, 28.

Pin 20 conditioned Chip Enable

Pin 28 switched $V_{CC}$

Pin 14 ground

### DESCRIPTION

The DS1213C is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K × 8 or a 32K × 8 JEDEC byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 28 and 20 for RAM control. All other pins are passed straight through to the socket receptacle.

See the DS1213 data sheet for technical details.

# Dallas Semiconductor
## *SmartSocket*

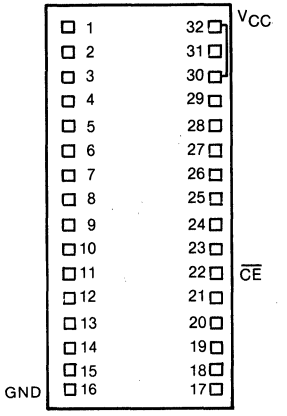
PRELIMINARY

# *DS1213D*

### FEATURES

- Accepts standard 8K × 8, 32K × 8, 128K × 8, and 512K × 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 128K × 8 to 512K × 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

### PIN CONNECTIONS




### PIN DEFINITIONS

All pins pass through except 22, 30 and 32.

Pin 22 $\overline{CE}$ - Conditioned Chip Enable
Pin 32 $V_{CC}$ - Switched $V_{CC}$ for 32-pin RAM
Pin 30 $V_{CC}$ - Switched $V_{CC}$ for 28-pin RAM
Pin 16 GND - Ground

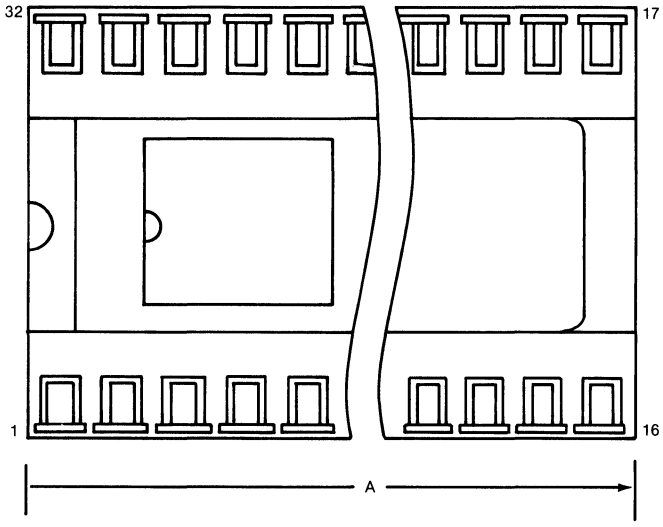
### DESCRIPTION

The DS1213D is a 32-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K × 8, 32K × 8, 128K × 8 or 512K × 8 byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

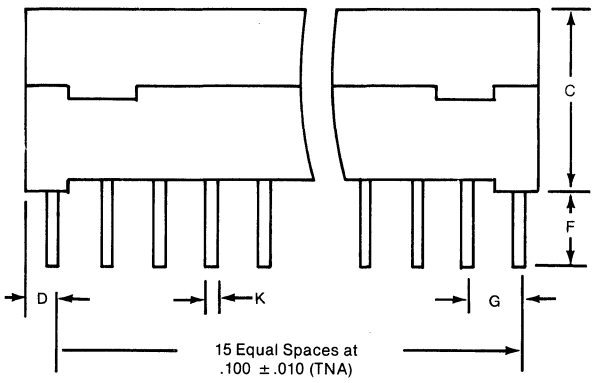
Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 22, 30 and 32 for RAM control. All other pins are passed straight through to the socket receptacle.

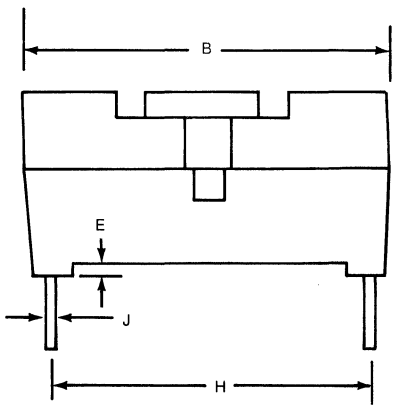
See the DS1213 data sheet for technical details.

# DS1213D
# SmartSocket




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.590 | 1.620 |
| B | .695 | .710 |
| C | .350 | .385 |
| D | .035 | .065 |
| E | .025 | .035 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |



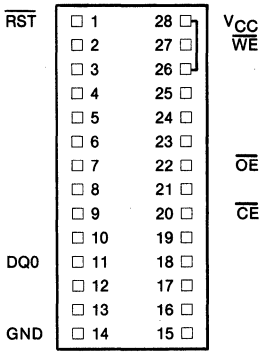



# Dallas Semiconductor
## *SmartWatch* — *DS1216*

### FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 2K × 8 and 8 K×8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @25°C

### PIN CONNECTIONS




### PIN DEFINITIONS

All Pins Pass Through Except
20, 26, 28
Pin 20 Conditioned Chip Enable
Pin 26 Switched $V_{CC}$ for 24 Pin RAM
Pin 28 Switched $V_{CC}$ for 28 Pin RAM
Pin 1 $\overline{\text{RESET}}$
Pin 22 Output Enable
Pin 27 Write Enable
Pin 11 Data Input/Output 0
Pin 14 Ground

### DESCRIPTION

The DS1216 is a 28-pin 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either 24-pin 2K × 8 or 28-pin 8K × 8 JEDEC Bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM. The SmartWatch monitors $V_{CC}$ for an out of tolerance condition. When such a condition occurs, an internal

lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated RAM take up no more area than the memory alone. The SmartWatch uses pins 28, 27, 26, 22, 20, 11, and 1 for RAM and watch control. All other pins are passed straight through to the socket receptacle.

The SmartWatch provides time keeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

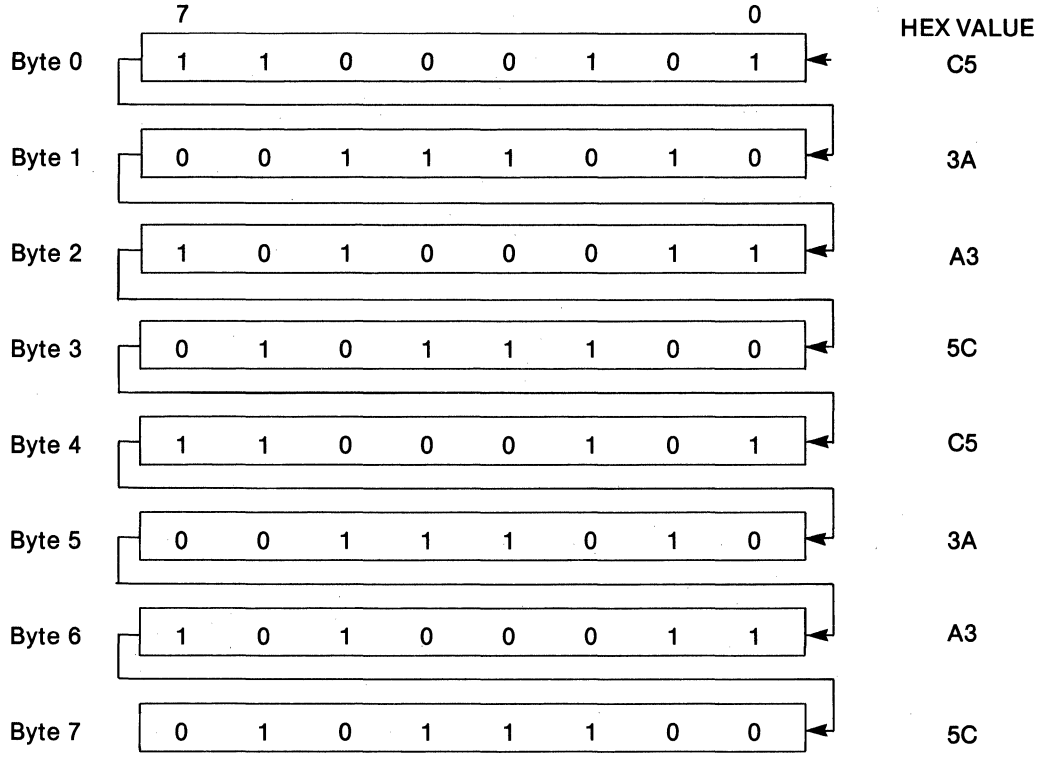
**OPERATION**

Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64 bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch, memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CE}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch, therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

**SMARTWATCH COMPARISON REGISTER DEFINITION** Figure 1




**NOTE:**
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in $10^{19}$.

**NONVOLATILE CONTROLLER OPERATION**
The DS1216 SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or $V_{CC}$ supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2 volts. The second function which is involved provides is power fail detection. Power fail detection occurs at typically 4.25 volts. The DS1216 constantly monitors the $V_{CC}$ supply. When $V_{CC}$ goes out of tolerance, a comparator outputs a power fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory within 0.2 volts of $V_{CC}$ or battery. During nominal power supply conditions the memory chip enable signal will track the chip enable signal sent to the socket with a maximum propagation delay of 20 ns.

## SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64 bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch register are in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

## AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12 hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24 hour mode, bit 5 is the second 10-hour bit (20-23 hours).

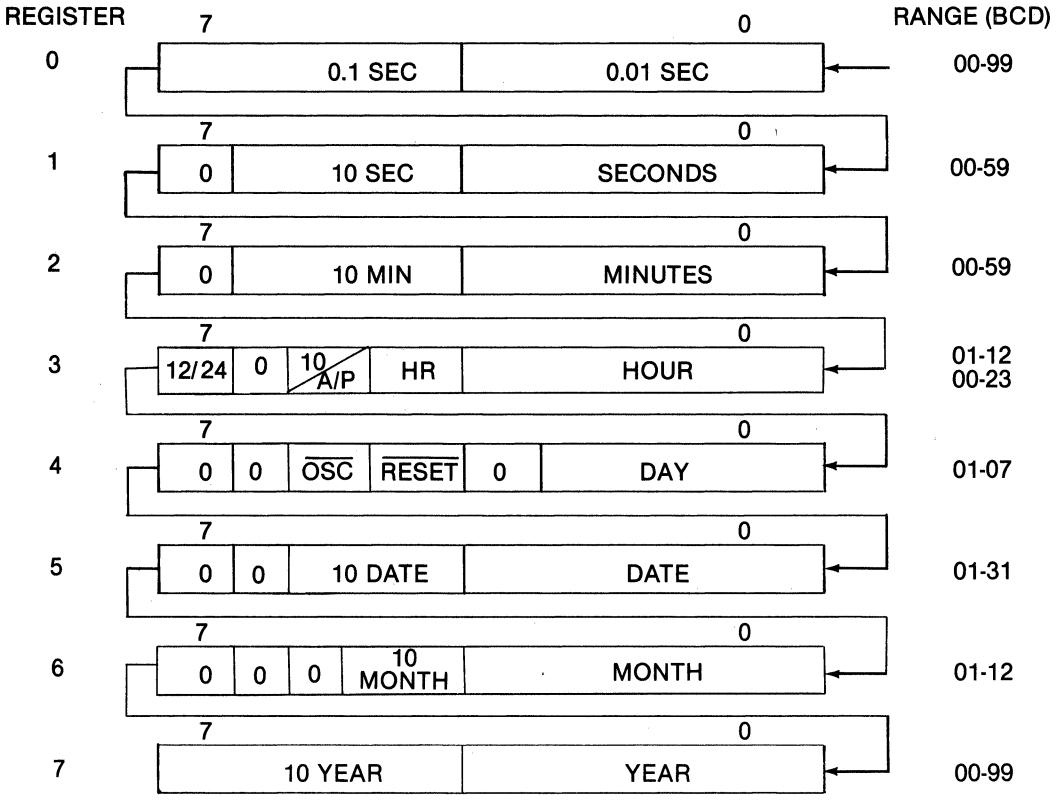
## OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logical 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logical 0, a low input on the $\overline{\text{RESET}}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from Dallas Semiconductor set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

## ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

**SMARTWATCH REGISTER DEFINITION** Figure 2



**ABSOLUTE MAXIMUM RATINGS***

Voltage on Any Pin Relative to Ground −1.0V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| PIN 26L, PIN 28L Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1, 3 |
| Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1, 10 |
| Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | 1, 10 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| PIN 26L, PIN 28L Supply | $I_{CCI}$ | | | 5 | mA | 3, 4, 5 |
| PIN 26U, PIN 28U Supply Voltage | $V_{CCO}$ | $V_{CC}-0.2$ | | | V | 3, 8 |
| PIN 26U, PIN 28U Supply Current | $I_{CCO}$ | | | 80 | mA | 3, 8 |
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | μA | 4,10, 13 |
| Output @ 2.4V | $I_{OH}$ | −1.0 | | | mA | 2 |
| Output @ 0.4V | $I_{OL}$ | | | 4.0 | mA | 2 |

(0°C to 70°, $V_{CC}$ < 4.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| PIN 20U Output | $V_{OHL}$ | $V_{CC}-0.2$ $V_{BAT}-0.2$ | | | V | 3 |
| PIN 26U, PIN 28U Battery Current | $I_{BAT}$ | | | 1 | μA | 3, 6 |
| Pin 26U, PIN 28U Battery Voltage | $V_{BAT}$ | 2 | 3 | 3.6 | V | 3 |

**CAPACITANCE** ($t_A$ = 25°C)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

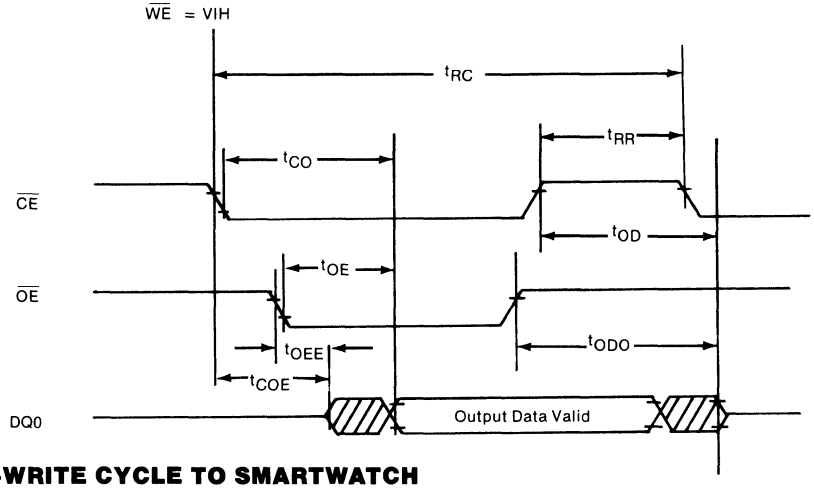
**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 250 | | | ns | |
| $\overline{CE}$ Access Time | $t_{CO}$ | | | 200 | ns | |
| $\overline{OE}$ Access Time | $t_{OE}$ | | | 100 | ns | |
| $\overline{CE}$ To Output Low Z | $t_{COE}$ | 10 | | | ns | |
| $\overline{OE}$ To Output Low Z | $t_{OEE}$ | 10 | | | ns | |
| $\overline{CE}$ To Output High Z | $t_{OD}$ | | | 100 | ns | |
| $\overline{OE}$ To Output High Z | $t_{ODO}$ | | | 100 | ns | |
| Read Recovery | $t_{RR}$ | 50 | | | ns | |
| Write Cycle Time | $t_{WC}$ | 250 | | | ns | |
| Write Pulse Width | $t_{WP}$ | 170 | | | ns | |
| Write Recovery | $t_{WR}$ | 50 | | | ns | 11 |
| Data Set Up Time | $t_{DS}$ | 100 | | | ns | 12 |
| Data Hold Time | $t_{DH}$ | 0 | | | ns | 12 |
| $\overline{CE}$ Pulse Width | $t_{CW}$ | 170 | | | ns | |
| Reset Pulse Width | $t_{RST}$ | 200 | | | ns | |
| $\overline{CE}$ Propagation Delay | $t_{PD}$ | 5 | 10 | 20 | ns | 2, 9 |
| $\overline{CE}$ High to Power Fail | $t_{PF}$ | | | 0 | ns | |

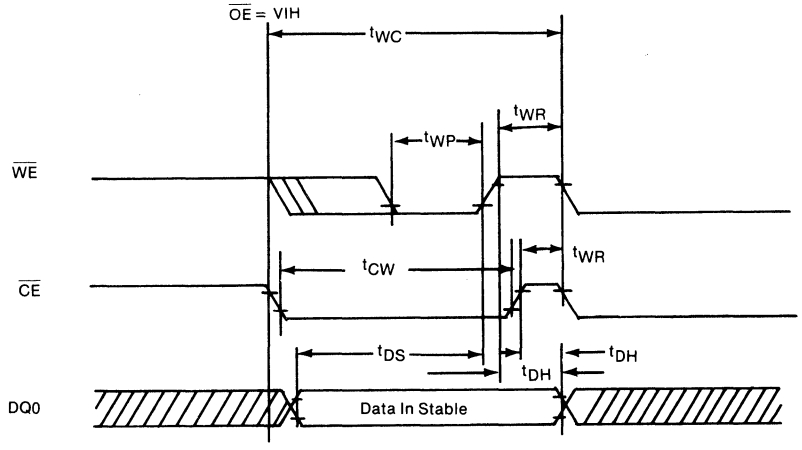
(0°C to 70°C, $V_{CC}$ < 4.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| Recovery at Power Up | $t_{REC}$ | | | 2 | ms | |
| $V_{CC}$ Slew Rate 4.5 - 3V | $t_F$ | 0 | | | $\mu$s | |
| $\overline{CE}$ Pulse Width | $t_{CE}$ | | | 1.5 | $\mu$s | 7 |

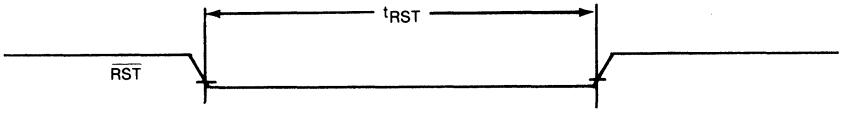
## TIMING DIAGRAM—READ CYCLE TO SMARTWATCH



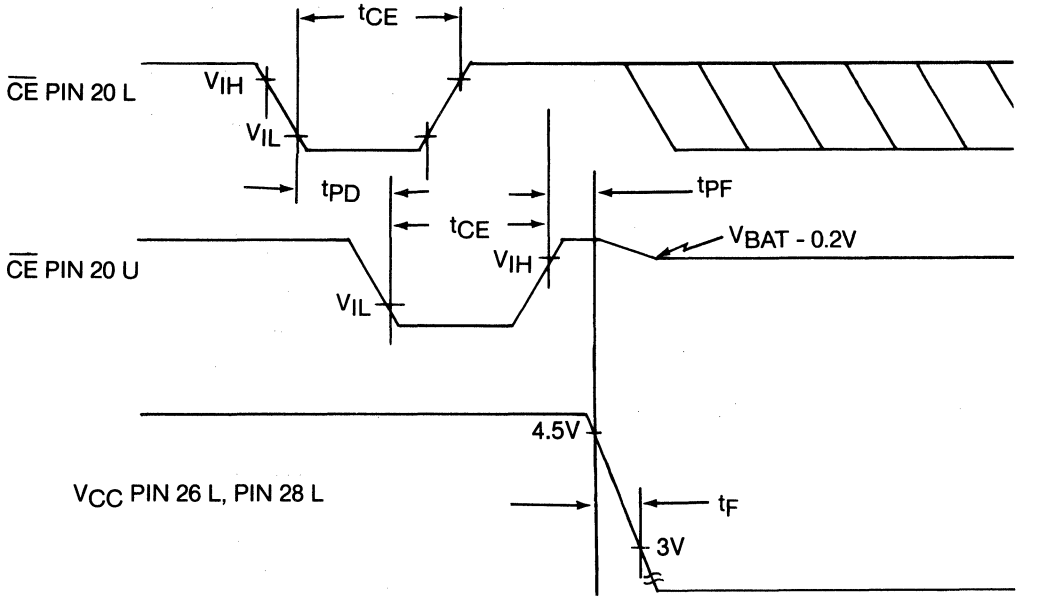

## TIMING DIAGRAM—WRITE CYCLE TO SMARTWATCH



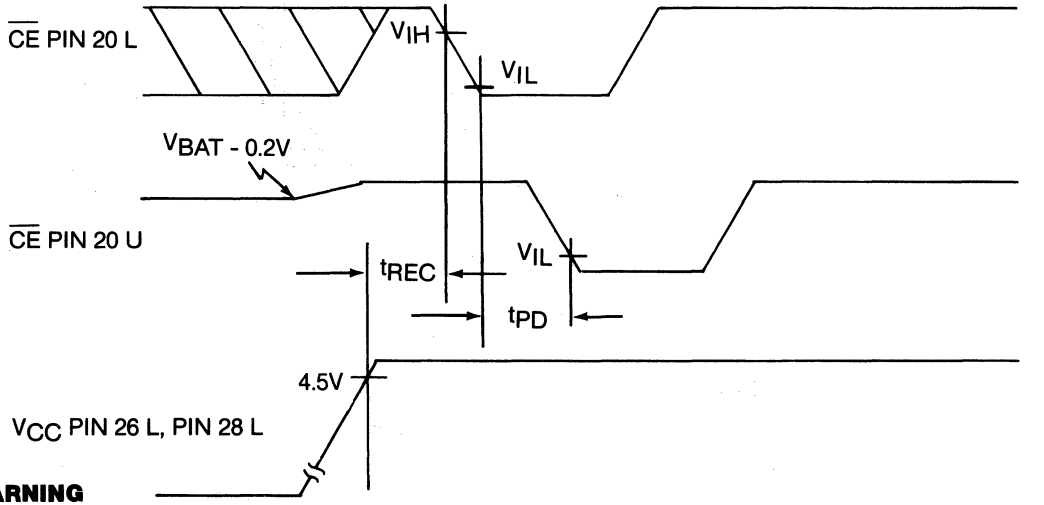

## TIMING DIAGRAM—RESET FOR SMARTWATCH



**TIMING DIAGRAM—POWER DOWN**




**TIMING DIAGRAM—POWER UP**




**WARNING**

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

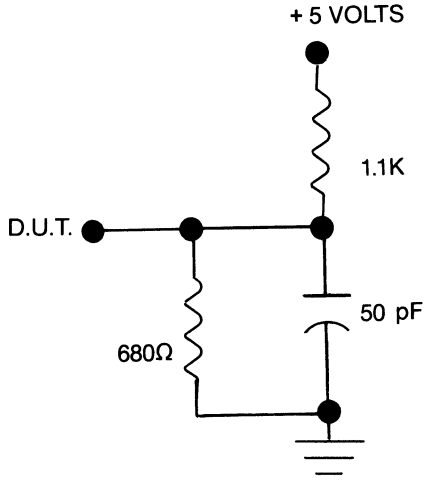
**NOTES**

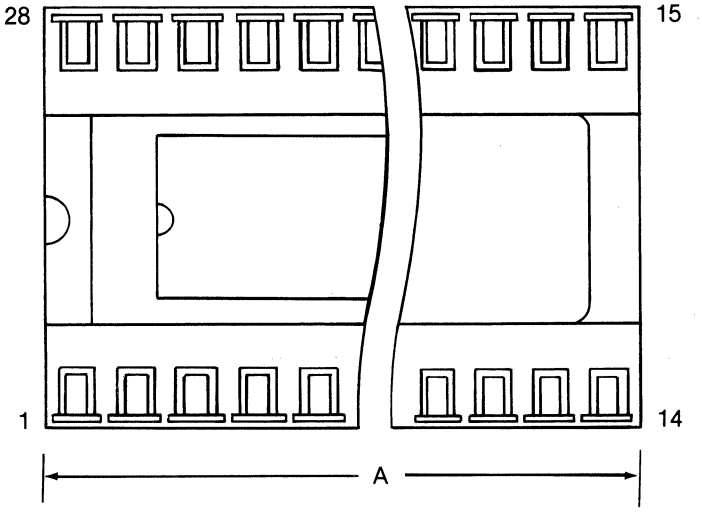
1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 3.
3. PIN locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. PIN 26 L may be connected to $V_{CC}$ or left disconnected at the P.C. board.
6. $I_{BAT}$ is the maximum current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. $t_{CE}$ max. must be met to insure data integrity on power loss.
8. $V_{CC}$ is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.
10. Applies to Pins 1 L, 11 L, 20 L, 22 L, and 27 L
11. $t_{WR}$ is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$
12. $t_{DH}$ and $t_{DS}$ are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$
13. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

6

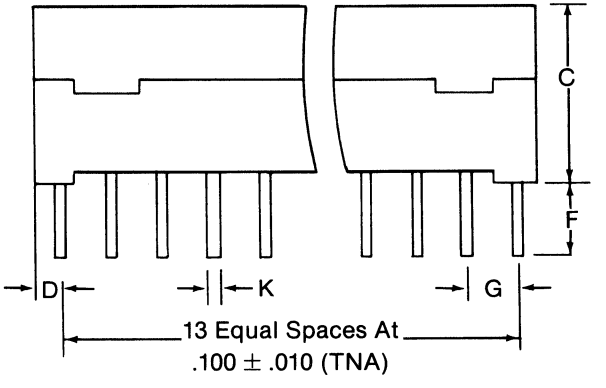
**OUTPUT LOAD**

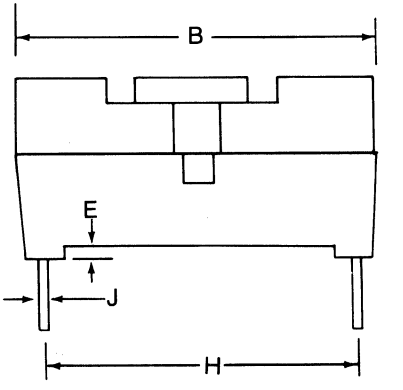
Figure 3






| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.390 | 1.420 |
| B | .695 | .710 |
| C | .350 | .385 |
| D | .035 | .065 |
| E | .025 | .035 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |

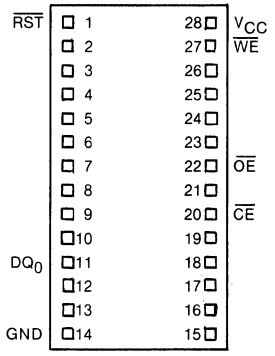


## FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 8K × 8 and 32K × 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ± 1 min./month @25°C

## PIN CONNECTIONS




## PIN DEFINITIONS

All Pins Pass Through Except 20, 28
Pin 20 Conditioned Chip Enable
Pin 28 Switched $V_{CC}$
Pin 1 $\overline{RESET}$
Pin 22 Output Enable
Pin 27 Write Enable
Pin 11 Data Input/Output 0
Pin 14 Ground

## DESCRIPTION

The DS1216C is a 28-pin 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K × 8 or a 32K × 8 JEDEC Bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216 data sheet for technical details.

# Dallas Semiconductor
## *SmartWatch*

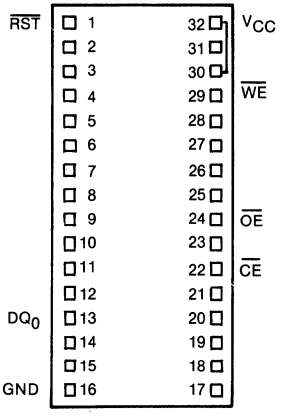
PRELIMINARY

# *DS1216D*

### FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 8K × 8, 32K × 8, 128K × 8, and 512K × 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @25°C

### PIN CONNECTIONS




### PIN DEFINITIONS

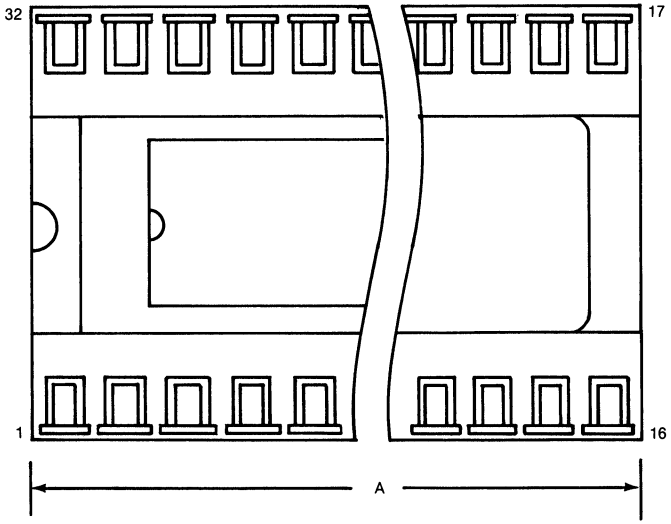
All pins pass through except 22, 30, and 32.
Pin 22 - Conditioned Chip Enable
Pin 32 - Switched $V_{CC}$ for 32-pin RAM
Pin 1 - $\overline{\text{RESET}}$
Pin 24 - Output Enable
Pin 29 - Write Enable
Pin 13 - Data Input/Output 0
Pin 16 - Ground
Pin 30 - Switched $V_{CC}$ for 28-pin RAM

### DESCRIPTION

The DS1216D is a 32-pin 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K × 8, 32K × 8, 128K × 8, or 512K × 8 JEDEC Bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

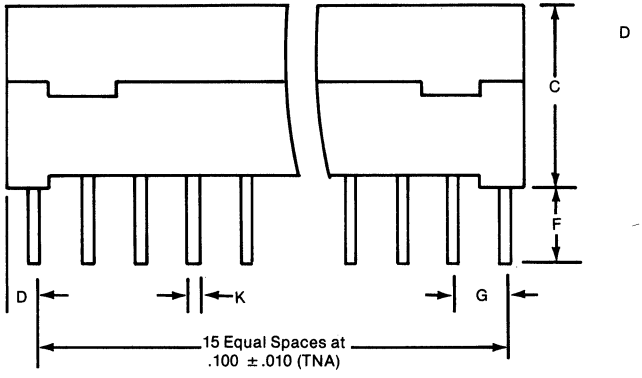
See the DS1216 data sheet for technical details.

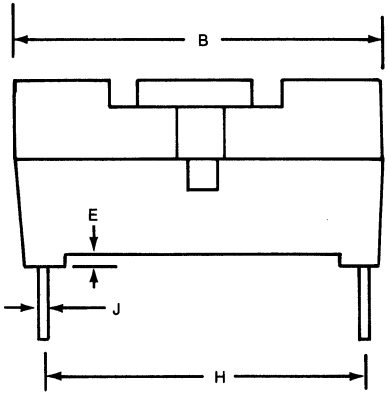
# DS1216D
# SmartWatch




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.590 | 1.620 |
| B | .695 | .710 |
| C | .350 | .385 |
| D | .035 | .065 |
| E | .025 | .035 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |





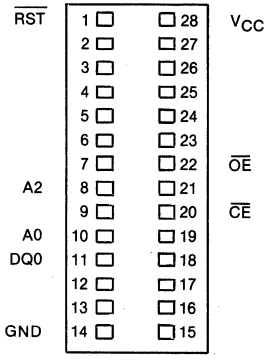
# Dallas Semiconductor
## *SmartWatch*

# *DS1216E*

### FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of month, months, and years
- Adds timekeeping to any 28-pin JEDEC Byte Wide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% $V_{CC}$ operating range
- Operating temperature range 0°C to 70°C
- Accurate to within 1 min./month @25°C

### PIN CONNECTIONS




### PIN NAMES

Pin 1 $\overline{RST}$ - Reset
Pin 8 A2 - Address Bit 2 (READ/$\overline{WRITE}$)
Pin 10 A0 - Address Bit 0 (Data Input)
Pin 11 DQ0 - $I/O_0$ (Data Output)
Pin 14 GND - Ground
Pin 20 $\overline{CE}$ - Conditioned Chip Enable
Pin 22 $\overline{OE}$ - Output Enable
Pin 28 $V_{CC}$ - +5 VDC to the Socket

All pins pass through to the Socket except 20.

### DESCRIPTION

The DS1216E is a 28-pin, 600-mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 28-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device take up no more area than the memory alone. The SmartWatch uses pins 1, 8, 10, 11, 20 and 22 for timekeeper control. All pins pass through to the socket receptacle except for pin 20 ($\overline{CE}$) which is inhibited during the transfer of time information.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, days, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

## OPERATION

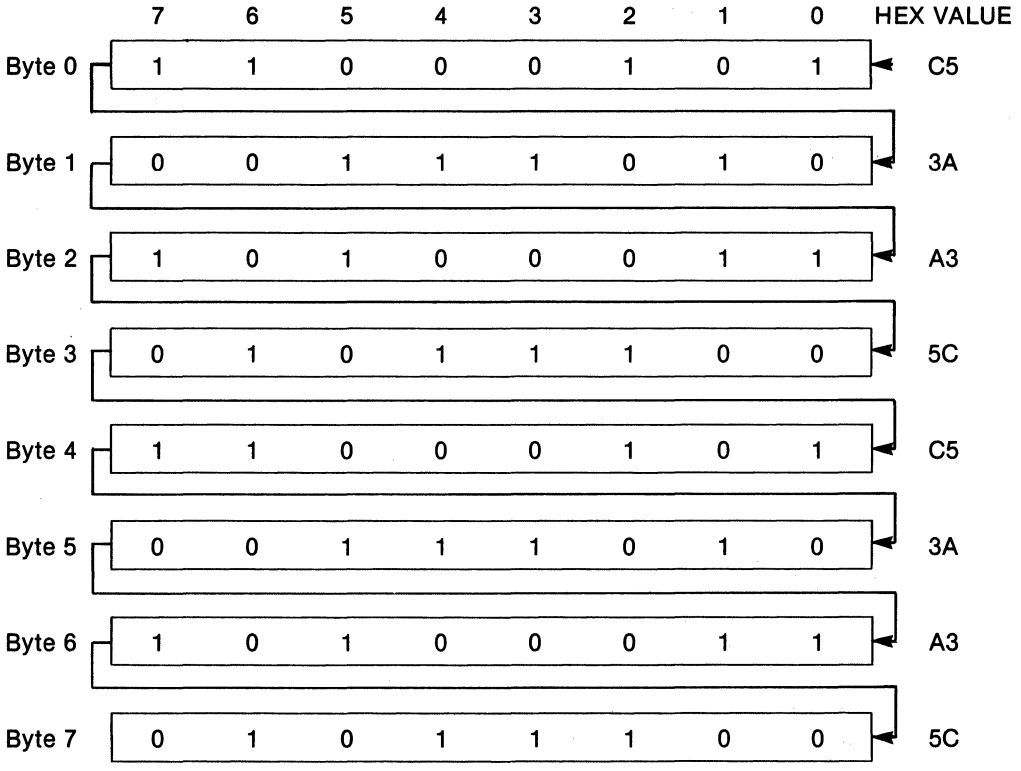
A highly structured sequence of 64 cycles is used to gain access to time information and temporarily disconnect the mated memory from the system bus. Information transfer into and out of the SmartWatch is achieved by using address bits A0 and A2, control signals $\overline{OE}$ and $\overline{CE}$, and Data I/O line DQ0. All SmartWatch data transfers are accomplished by executing read cycles to the mated memory address space. Write and read functions are determined by the level of address bit A2. When address bit A2 is low, a write cycle is enabled and data must be input on address bit A0. When address bit A2 is high, a read cycle is enabled and data is output on data I/O line DQ0. Either control signal ($\overline{OE}$ or $\overline{CE}$) must transition low to begin and high to end memory cycles which are directed to the SmartWatch. However, both control signals must be in an active state during a memory cycle. Communication with the SmartWatch is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles, placing address bit A2 low with the proper data on address bit A0. The 64 write cycles are used only to gain access to the SmartWatch. Prior to executing the first of 64 write cycles, a read cycle should be executed by holding A2 high. The read cycle will reset the comparison register pointer within the SmartWatch insuring the pattern recognition starts with the first bit of the sequence. When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above, until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive data on Data In (A0) or transmit data on Data Out (DQ0), depending on the level of $\overline{READ}/\overline{WRITE}$ (A2). Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ and $\overline{OE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

An unconditional reset to the SmartWatch occurs by either bringing A14 ($\overline{RESET}$) low, if enabled, or on power up. This $\overline{RESET}$ can occur during pattern recognition or while accessing the SmartWatch registers. $\overline{RESET}$ causes access to abort and forces the comparison register pointer back to Bit 0 without changing registers.

## NONVOLATILE CONTROLLER OPERATION

The DS1216E SmartWatch performs circuit functions required to make the timekeeping function nonvolatile. First, a switch is provided to direct power from the battery or $V_{CC}$ supply, depending on which voltage is greater. The second function provides power fail detection. Power fail detection occurs at typically 4.25 volts. Finally the nonvolatile controller protects the SmartWatch register contents by ignoring any inputs after power fail detection has occurred. Power fail detection also has the same effect on data transfer as the $\overline{RESET}$ input.

**SMARTWATCH COMPARISON REGISTER DEFINITION** Figure 1




**NOTE:**
The pattern recognition sequence in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern accidentally occurring and causing inadvertent entry to the SmartWatch is less than 1 in $10^{19}$.

## SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch registers are in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

## AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

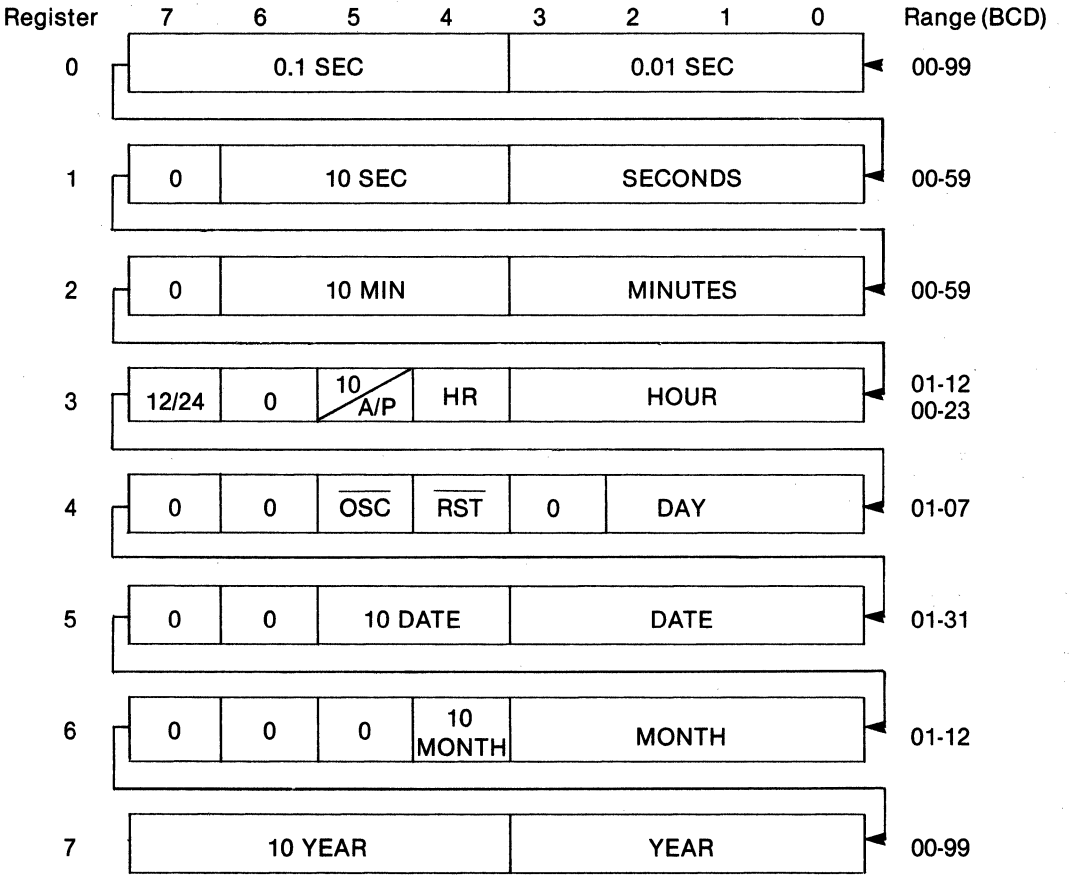
## OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logical 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logical 0, a low input on the $\overline{\text{RESET}}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from Dallas Semiconductor set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

## ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

**SMARTWATCH REGISTER DEFINITION** Figure 2



## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on any Pin Relative to Ground | -1.0V to +7.0V |
| Operating Temperature | 0°C to 70°C |
| Storage Temperature | -40°C to 70°C |
| Soldering Temperature | 260°C for 10 Sec. |

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Pin 28L Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1,3 |
| Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1,6 |
| Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | 1,6 |

## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Pin 28L Supply Current | $I_{CC}$ | | | 5 | mA | 3,4 |
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | uA | 4,6,10 |
| Output @2.4V | $I_{OH}$ | −1.0 | | | mA | 2 |
| Output @0.4V | $I_{OL}$ | | | 4.0 | mA | 2 |

## CAPACITANCE

($t_A$ = 25°C)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

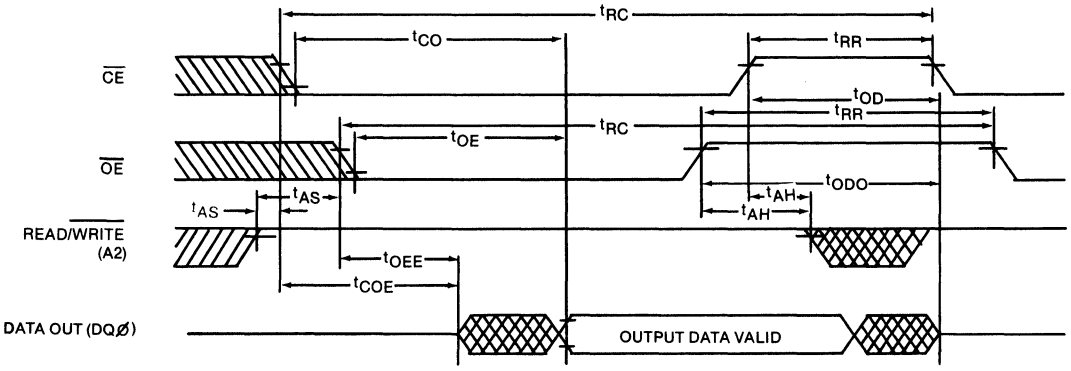
**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 250 | | | ns | |
| $\overline{CE}$ Access Time | $t_{CO}$ | | | 200 | ns | |
| $\overline{OE}$ Access Time | $t_{OE}$ | | | 200 | ns | |
| $\overline{CE}$ to Output in Low Z | $t_{COE}$ | 10 | | | ns | |
| $\overline{OE}$ to Output in Low Z | $t_{OEE}$ | 10 | | | ns | |
| $\overline{CE}$ to Output in High Z | $t_{OD}$ | | | 100 | ns | |
| $\overline{OE}$ to Output in High Z | $t_{ODO}$ | | | 100 | ns | |
| Address Set Up Time | $t_{AS}$ | 20 | | | ns | 9 |
| Address Hold Time | $t_{AH}$ | | | 10 | ns | 8 |
| Read Recovery | $t_{RR}$ | 50 | | | ns | |
| Write Cycle Time | $t_{WC}$ | 250 | | | ns | |
| $\overline{CE}$ Pulse Width | $t_{CW}$ | 170 | | | ns | |
| $\overline{OE}$ Pulse Width | $t_{OW}$ | 170 | | | ns | |
| Write Recovery | $t_{WR}$ | 50 | | | ns | 7 |
| Data Set Up Time | $t_{DS}$ | 100 | | | ns | 8 |
| Data Hold Time | $t_{DH}$ | 10 | | | ns | 8 |
| $\overline{RST}$ Pulse Width | $t_{RST}$ | 200 | | | ns | |
| $\overline{CE}$ Propagation Delay | $t_{PD}$ | 5 | 10 | 20 | ns | 2,5 |
| $\overline{CE}$ High to Power Fail | $t_{PF}$ | | | 0 | ns | |

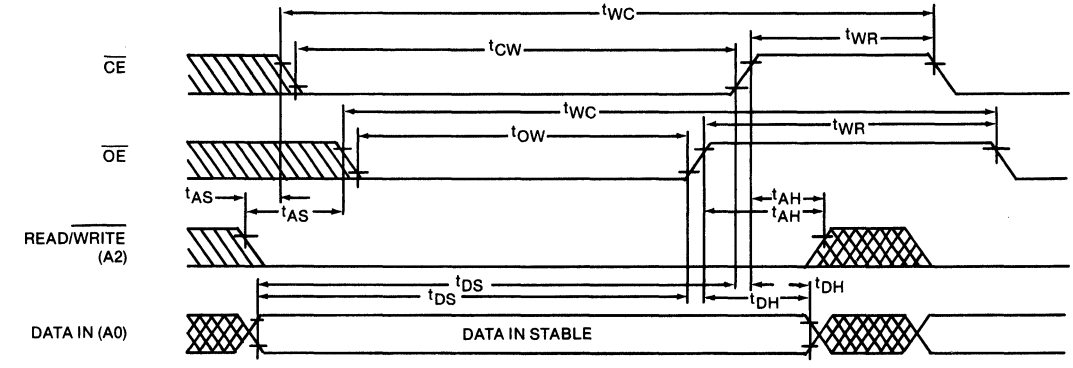
(0 °C to 70 °C, $V_{CC}$ < 4.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| Recovery at Power Up | $t_{REC}$ | | | 2 | ms | |
| $V_{CC}$ Slew Rate 4.5 -3V | $t_F$ | 0 | | | ms | |

## TIMING DIAGRAM— READ CYCLE

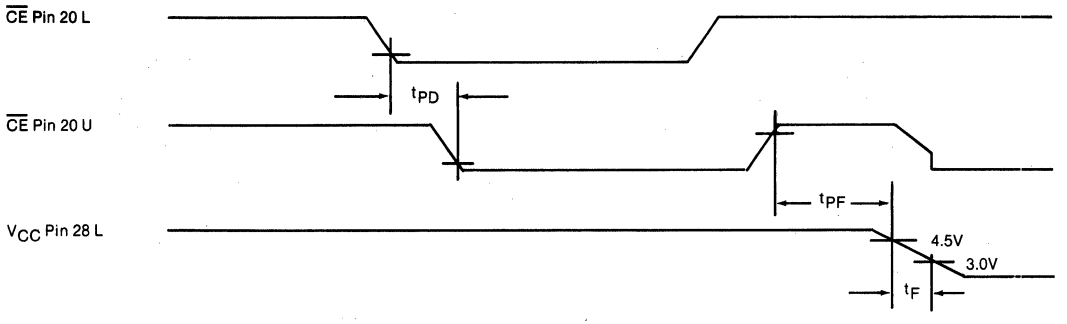



## TIMING DIAGRAM—WRITE CYCLE

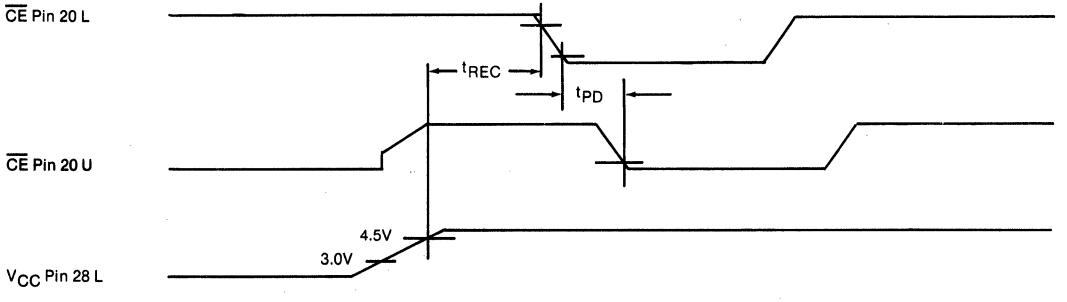



6

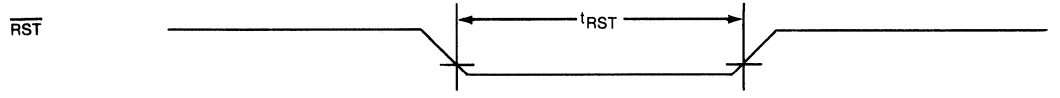
## TIMING DIAGRAM— POWER DOWN




## TIMING DIAGRAM— POWER UP




## TIMING DIAGRAM—RESET FOR SMARTWATCH




**WARNING**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

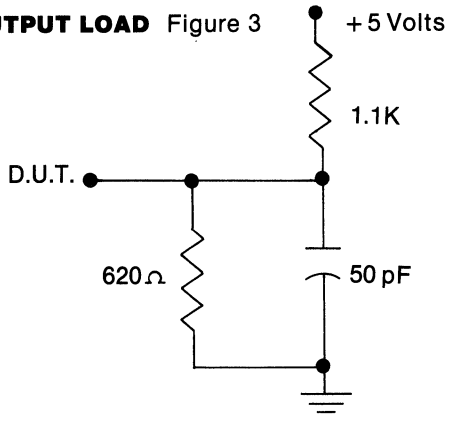
Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

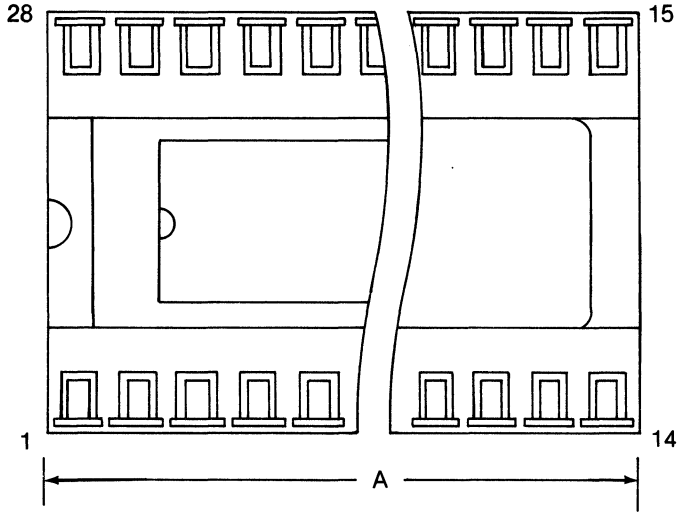
**NOTES:**

1. All voltages are referenced to ground.
2. Measured with a load shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Input pulse rise and fall times equal 10 ns.
6. Applies to Pins 1 L, 8 L, 10 L, 20 L, and 22 L.
7. $t_{WR}$ and $t_{RR}$ are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
8. $t_{AH}$, $t_{DS}$ and $t_{DH}$ are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
9. $t_{AS}$ is a function of the latter occurring edge of $\overline{OE}$ or $\overline{CE}$.
10. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

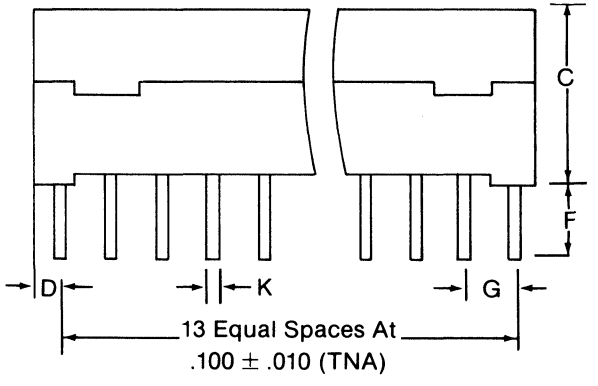


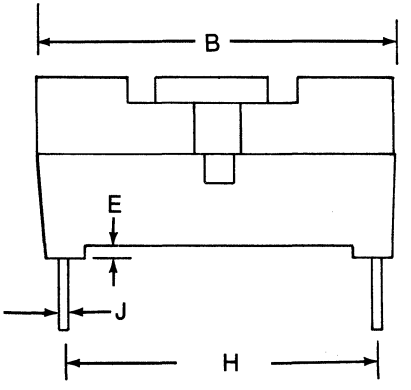
**OUTPUT LOAD** Figure 3






| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.390 | 1.420 |
| B | .695 | .705 |
| C | .350 | .385 |
| D | .035 | .065 |
| E | .025 | .035 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .625 |
| J | .008 | .012 |
| K | .015 | .021 |



# Dallas Semiconductor
## *SmartWatch*

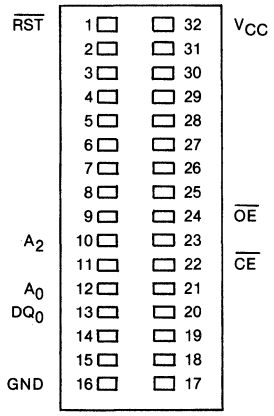
PRELIMINARY

## *DS1216F*

### FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adds timekeeping to any 32-pin JEDEC Byte Wide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% $V_{CC}$ operating range
- Operating temperature range 0°C to 70°C
- Accuracy to within 1 min./month @25°C

### PIN CONNECTIONS




### PIN NAMES

Pin 1 $\overline{RST}$ - Reset
Pin 10 $A_2$ - Address Bit 2 (READ/$\overline{WRITE}$)
Pin 12 $A_0$ - Address Bit 0 (Data Input)
Pin 13 $DQ_0$ - I/$O_0$ (Data Output)
Pin 16 GND - Ground
Pin 22 $\overline{CE}$ - Conditioned Chip Enable
Pin 24 $\overline{OE}$ - Output Enable
Pin 32 $V_{CC}$ - +5 VDC to the Socket

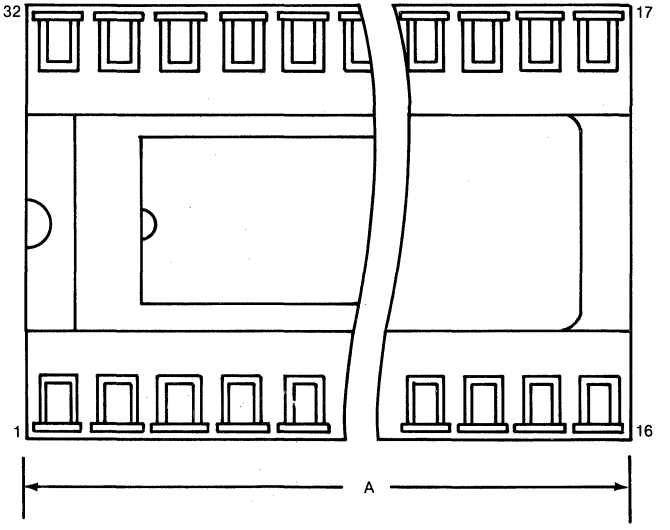
All pins pass through to the Socket except 22.

### DESCRIPTION

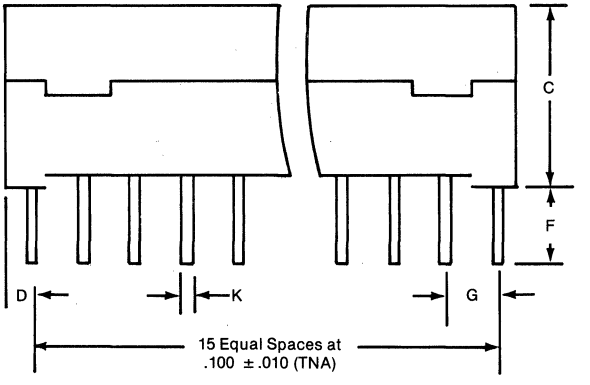
The DS1216F is a 32-pin 600-mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 32-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

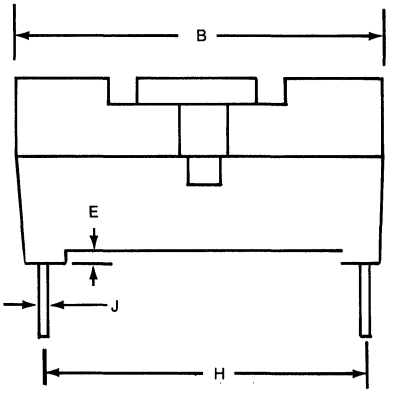
Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device take up no more area than the memory alone. The SmartWatch uses pins 1, 10, 12, 13, 22 and 24 for timekeeper control. All pins pass through to the socket receptacle except for pin 22 ($\overline{CE}$) which is inhibited during the transfer of time information.

See the DS1216E data sheet for technical details and SmartWatch operation.




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.590 | 1.620 |
| B | .695 | .710 |
| C | .350 | .385 |
| D | .035 | .065 |
| E | .025 | .035 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |



PRELIMINARY

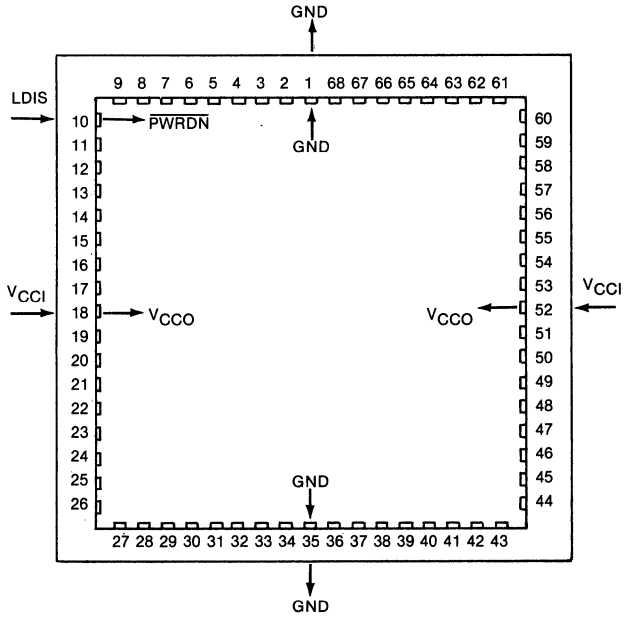
# Dallas Semiconductor
# *LCA SmartSocket*

# *DS1264*
# *DS1265*

## FEATURES

- SmartSocket keeps logic defined in Xilinx/MMI LCA's in the absence of power
- Eliminates need for external memory to hold a copy of the logic configuration data
- Logic configuration already defined on power-up; no time required for initial loading
- Embedded IC provides power-fail detection, $\overline{\text{PWRDN}}$ pin control and automatic switching between system $V_{CC}$ and lithium voltage
- Electronic freshness seal (lithium save) insures full lithium capacity after shipping and handling
- Two versions:
  - DS1264 accepts Xilinx/MMI 2064 68-pin LCA
  - DS1265 accepts Xilinx/MMI 2018 84-pin LCA
- 68- and 84-pin sockets accept JEDEC plastic chip carriers with tin-plated leads

## DS1264 PIN DESCRIPTION

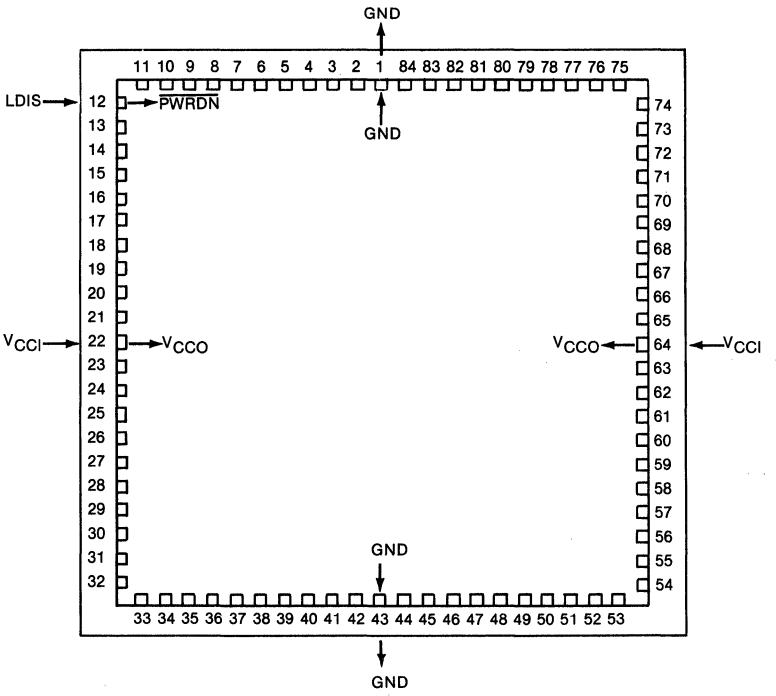



## PIN DESCRIPTION

All pins pass straight through to the LCA in either the 68-pin or the 84-pin socket except for the following:

**LDIS (active pulsed low)**—Lithium Disconnect: Lithium Disconnect may be used to disconnect the lithium source during periods of time when nonvolatility is not required. This function is brought out in place of the LCA's $\overline{\text{PWRDN}}$ pin. The LCA's $\overline{\text{PWRDN}}$ pin is connected to the Power Fail ($\overline{\text{PF}}$) output signal of the controller IC embedded within the socket.

## DS1265 PIN DESCRIPTION




**$V_{CC}$**—Power Supply: System power is routed to the embedded control IC which switches power to the LCA between the system supply when it is applied during full operation and the lithium power source for nonvolatility in the absence of system power.

The table below summarizes the assignments for these pins for the two versions of the SmartSocket:

| | DS1264 for 2064 68-pin LCA | DS1265 for 2018 84-pin LCA |
|---|---|---|
| **SIGNAL** | **PIN #** | **PIN #** |
| LDIS | 10 | 12 |
| $V_{CC}$ | 18, 52 | 22, 64 |
| GND | 1, 35 | 1, 43 |

## DESCRIPTION

The DS1264 and DS1265 are PLCC sockets with a built-in CMOS IC controller circuit and an encapsulated lithium energy source. They are specifically designed to provide nonvolatile support for the Xilinx/MMI Logic Cell Array (LCA) devices. The DS1264 accommodates the 68-pin 2064 LCA while the DS1265 mates up with the 84-pin 2018 LCA.

The 2064 and 2018 LCAs are CMOS logic array devices in which the internal configuration is determined by self-contained bits of RAM storage. The data contained in this RAM is used to define logic block functions, configuration of I/O blocks, routing of internal signals, and other options. As a result, the user can quickly implement complex digital logic functions directly without the requirement for masking or other vendor performed programming steps. In addition, the use of internal RAM allows logic design changes to be quickly implemented and verified in the prototype system. Complete re-configuration "on-the-fly" of the final production system is also possible.

The use of RAM for holding the LCA's configuration data allows a maximum amount of flexibility in a programmable logic device. Without nonvolatile support, however, the device must be re-loaded from external memory each time that the configuration data is lost due to a power down or to a brownout condition. This not only requires additional memory to contain the logic configuration data, but also a considerable amount of time following power up to perform the reload operation.

DS1264 alleviates these problems by providing nonvolatile support with a minimum impact on system hardware. No additional circuitry is required for nonvolatile operation, and no additional printed circuit board area is used since the combination of the SmartSocket and the LCA uses no more area than the LCA alone. When the socket is mated with the LCA, it provides a complete, self-contained solution for nonvolatile support. Only three pins are used for nonvolatile control of the LCA. All other pins are passed straight through to the socket receptacle.

## POWER CYCLING OPERATION

The schematic shown in Figure 1 illustrates the internal connection of the LCA SmartSockets. The timing diagram in Figure 2 illustrates the timing operation of the system when power to the system is cycled off and on. During normal system operation, incoming $V_{CC}$ voltage is monitored by the DS1259 for two thresholds below nominal operating voltage. Both of these thresholds are detected by the SmartSocket as $V_{CC}$ decays in a power-down situation. The first (highest) threshold which is detected during a power-down is the Power Fail Voltage ($V_{PF}$). When $V_{CC}$ falls below this value the $\overline{PWRDN}$ pin on the LCA is pulled down to its active low level by the $\overline{PF}$ output from the embedded control IC. This action will force the LCA to suspend all operation and go into its low power consumption mode. All clocks will be stopped within the device and all outputs are placed into high impedance state. All configuration data is maintained in the device when $\overline{PWRDN}$ is held at its active low level.

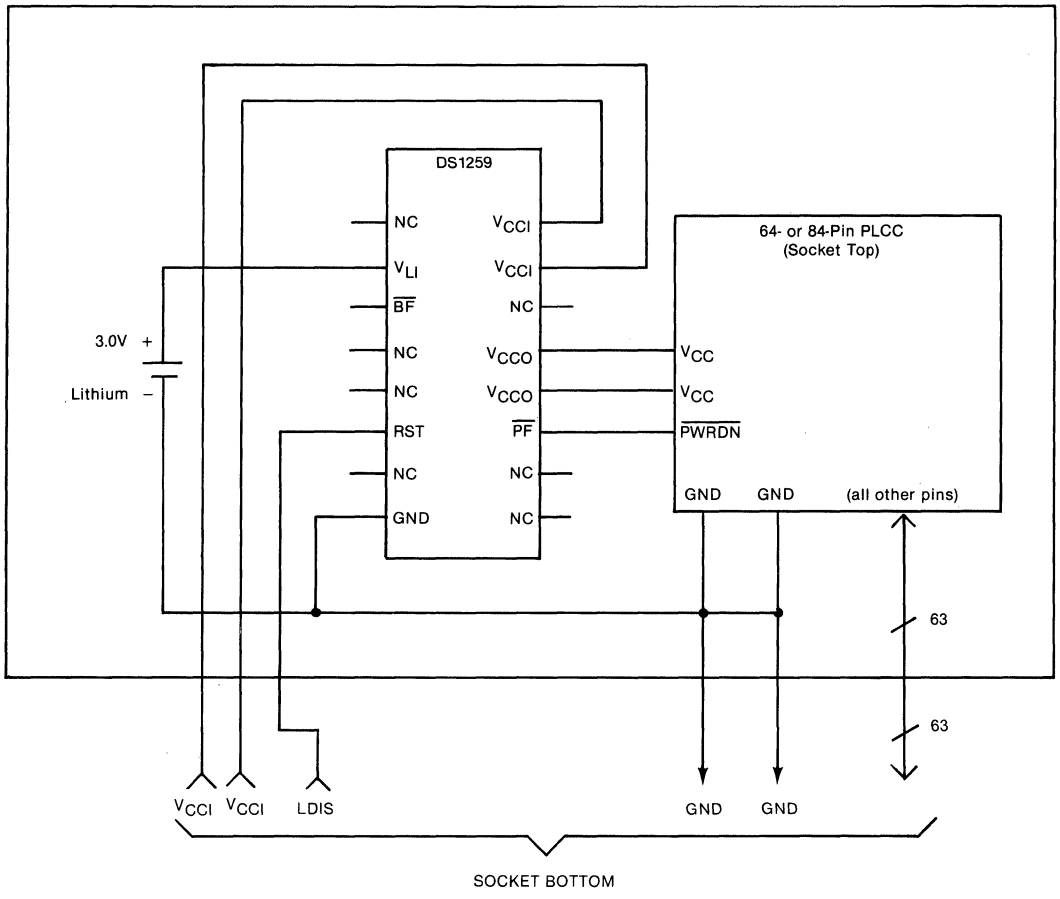
As $V_{CC}$ voltage continues to decay during a power-down, it will eventually drop below the second (lower) threshold detected by the SmartSocket, which is Power Down Voltage ($V_{PD}$). When this occurs the internal lithium source is automatically switched to the $V_{CC}$ pins on the LCA device and the $\overline{PWRDN}$ input will continue to be held in its active state. At this point the configuration data will be maintained by power supplied from the lithium source.

During a power-up, the reverse of the sequence described above will take place. When $V_{CC}$ rises above the $V_{PD}$ threshold, the $V_{CC}$ lines of the LCA will be switched from the lithium source to the system $V_{CC}$ lines. When $V_{CC}$ subsequently rises above the $V_{PF}$ threshold, the $\overline{PWRDN}$ pin of the LCA will be driven to its inactive high level, and full operation of the device can then take place.

## LITHIUM DISCONNECT

The Lithium Disconnect (LDIS) input to the LCA SmartSocket can be used to disconnect the lithium source from the LCA $V_{CC}$ lines. This feature is useful in situations where the system is to be powered down for a long period of time without the need for data retention, as might be the case when the system is stored in a stockroom. By disconnecting the lithium source, its full energy capacity can be assured at the time when use of the system begins. Accidental discharge is also prevented during shipping and handling. This feature is activated with a high-going pulse to the LDIS input while system power is being applied above the $V_{PF}$ threshold. When system power is removed following this action the LCA's $V_{CC}$ lines will be isolated from the lithium source. The next time that power is applied normal operation will again take place when $V_{CC}$ rises above the $V_{PF}$ threshold, and the LCA's $V_{CC}$ lines once again will be connected to the lithium source when the system is powered down. The timing diagram in Figure 2 illustrates the operation of the SmartSocket in response to the LDIS input.

**DS1264/1265 LCA SMARTSOCKET INTERNAL SCHEMATIC** Figure 1



**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.1V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Inputs: $V_{CCL}$ | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input High Voltage: LDIS | $V_{IH}$ | 2.0 | | $V_{CC}+0.3$ | V | 1 |
| Input Low Voltage: LDIS | $V_{IL}$ | 0 | | 0.8 | V | |

**D.C. ELECTRICAL CHARACTERISTICS**

($V_{CC}$ voltage applied) (0°C to 70°C $V_{CC}$ = 4.0 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage LDIS | $I_L$ | −1.0 | | +1.0 | μA | 10 |
| Output High Current LDIS $V_{OH}$ = 0.4V | $I_{OH}$ | −1.0 | | | mA | 1,2,10 |
| Output Low Current LDIS $V_{OL}$ = 0.4V | $I_{OL}$ | | | 4.0 | mA | 1,2,10 |
| Input Supply Current: $V_{CCL}$ | $I_{CC}$ | | | 5 | mA | 3,10 |
| Output Supply Current: $V_{CCU}$ | $I_{CCO}$ | | | 250 | mA | 10 |
| Power Fail Detect Voltage | $V_{PF}$ | | 4.25 | 4.5 | V | 4 |
| Power Down Detect Voltage | $V_{PD}$ | | $V_{LI}$ | | V | 6 |

## D.C. ELECTRICAL CHARACTERISTICS

($V_{CC}$ voltage removed) ($0\,°C$ to $70\,°C$ $V_{CC} \leq V_{PF}$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Lithium Voltage | $V_{LI}$ | | 3 | | V | 7,9,10 |
| Lithium Supply Current: $V_{CCU}$ | $I_{LI}$ | | | 10 | nA | 3 |
| | | | | 1 | $\mu$A | 8 |

## CAPACITANCE

($t_A = 25\,°C$)

| PARAMETER | SYMBOL | TYP | MAX | UNITS |
|---|---|---|---|---|
| Output Capacitance | $C_O$ | 5 | 10 | pF |
| Input Capacitance | $C_I$ | 5 | 10 | pF |

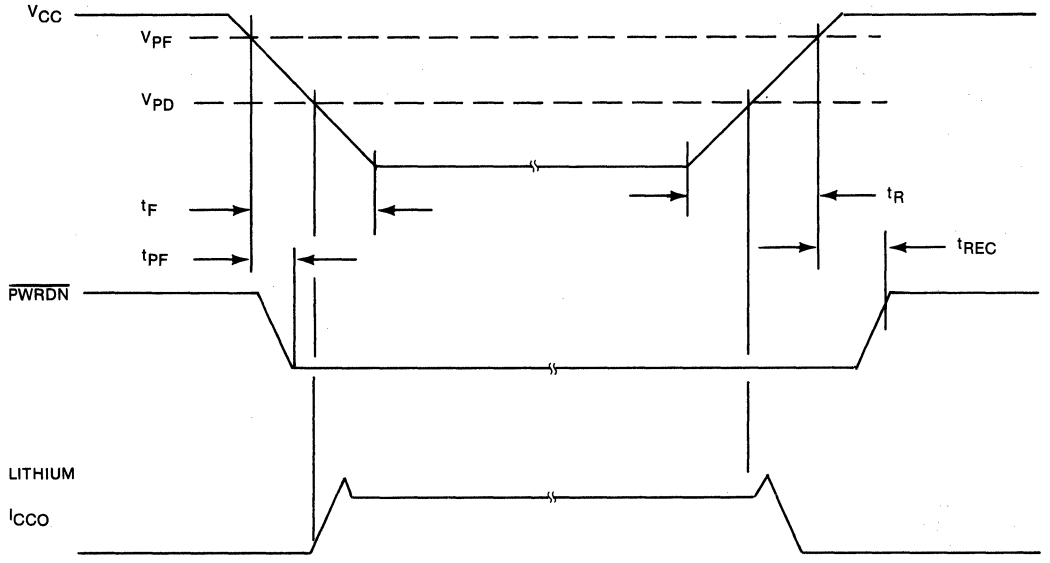
## A.C. ELECTRICAL CHARACTERISTICS

($V_{CC}$ voltage applied) ($0\,°C$ to $70\,°C$, $V_{CC} = 4.0$ to $5.5V$)

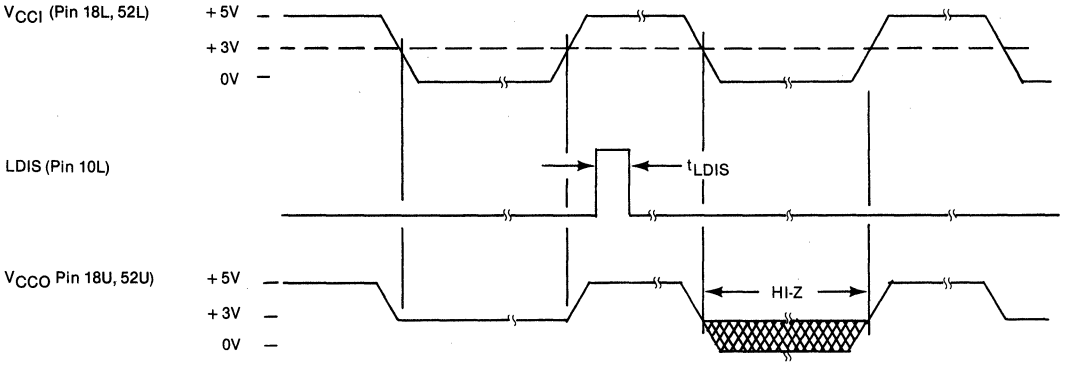
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $V_{CC}$ Slew Rate (Falling edge) | $t_F$ | 300 | | | us | |
| $V_{CC}$ Slew Rate (Rising edge) | $t_R$ | 1 | | | us | |
| Power Fail to $\overline{\text{PWRDN}}$ low | $t_{PF}$ | 0 | | | us | |
| $\overline{\text{PWRDN}}$ High after Power Up | $t_{REC}$ | 2 | 10 | 20 | ms | |

6

**POWER CYCLING OPERATION** Figure 2



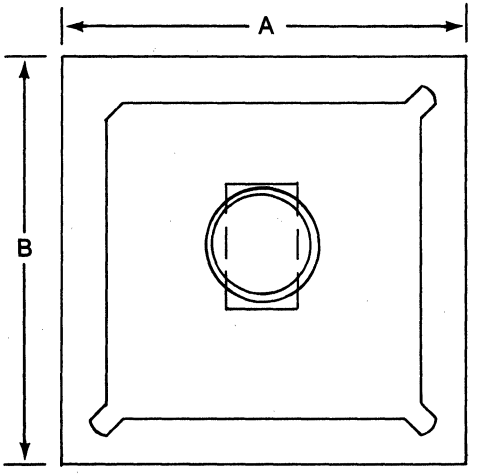

**LITHIUM DISCONNECT TIMING** Figure 3



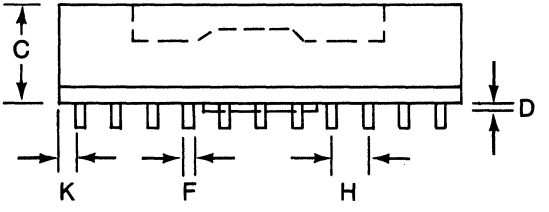
**NOTES:**

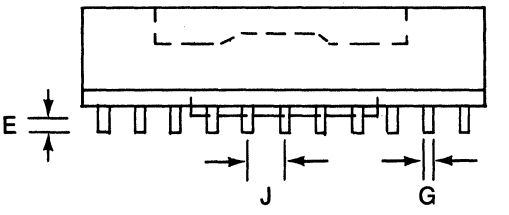
1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with socket empty.
4. $V_{PF}$ is the point that $\overline{\text{PWRDN}}$ is driven low.
5. Both $V_{CCO}$ outputs will meet the rated voltage and current as the lithium energy source retains at least 10% of its original capacity.
6. $V_{PD}$ is the point that power is switched from system $V_{CC}$ to the lithium source tied to the $V_{LI}$ pin.
7. $V_{LI}$ is the internal lithium energy source voltage.
8. Measured with LCA in socket; maximum value allowed for 10 yr. data retention at 25°C.
9. Storage loss is less than 1% per year at 25°C.
10. Pin names designated with a "U" suffix refer to the signal applied to the LCA pin on the at-the-socket receptacle. Pin names designated with the "L" suffix refer to the signal coming into the socket on the lower pin.

# DS1264
# LCA SMARTSOCKET

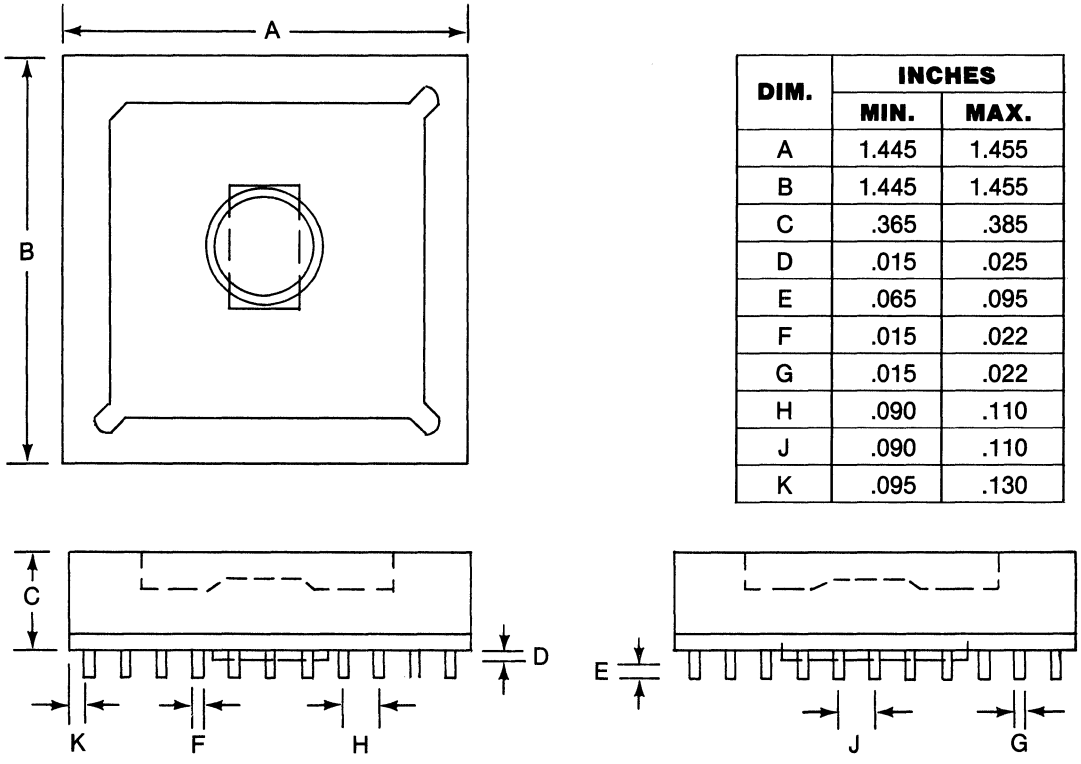



| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.220 | 1.280 |
| B | 1.185 | 1.215 |
| C | .365 | .385 |
| D | .015 | .025 |
| E | .065 | .095 |
| F | .015 | .022 |
| G | .015 | .022 |
| H | .090 | .110 |
| J | .090 | .110 |
| K | .095 | .130 |



# DS1265
# LCA SMARTSOCKET




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.445 | 1.455 |
| B | 1.445 | 1.455 |
| C | .365 | .385 |
| D | .015 | .025 |
| E | .065 | .095 |
| F | .015 | .022 |
| G | .015 | .022 |
| H | .090 | .110 |
| J | .090 | .110 |
| K | .095 | .130 |

# Timekeeping

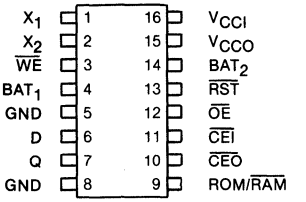
# Dallas Semiconductor
## *TimeChip*

## DS1215

### FEATURES

- TimeChip keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Leap year automatically corrected
- No address space required
- Provides nonvolatile controller functions for battery backing up RAM
- Supports redundant batteries for high-rel applications
- Uses a 32.768 KHz watch crystal
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Space saving 16-pin DIP package

### PIN CONNECTIONS




### PIN NAMES

Pins 1 & 2 - $X_1$, $X_2$ - 32.768 KHz Crystal Connections
Pin 3 - $\overline{WE}$ - Write Enable
Pin 4 - $BAT_1$ - Battery 1 Input
Pins 5 & 8 - GND - Ground
Pin 6 - D - Data In
Pin 7 - Q - Data Out
Pin 9 - ROM/$\overline{RAM}$ - ROM-RAM Select
Pin 10 - $\overline{CEO}$ - Chip Enable Out
Pin 11 - $\overline{CEI}$ - Chip Enable Input
Pin 12 - $\overline{OE}$ - Output Enable
Pin 13 - $\overline{RST}$ - Reset
Pin 14 - $BAT_2$ - Battery 2 Input
Pin 15 - $V_{CCO}$ - Switched Supply Output
Pin 16 - $V_{CCI}$ - +5V DC Input

### DESCRIPTION

The DS1215 is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch provides hundredths of seconds, seconds, minutes, hours, day, date, month, and year information, while the nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

The last date of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator, or a 24-hour mode.

The nonvolatile memory controller portion of the circuit is designed to handle power fail detection, memory write protection, and battery redundancy. In short, the controller changes standard CMOS memories into nonvolatile memories, and provides continuous power to the TimeChip. Alternatively the TimeChip can be used with ROM memory by controlling the Chip Enable Output signal ($\overline{CEO}$) while the TimeChip is being accessed.

**OPERATION**

The block diagram of Figure 3 illustrates the main elements of the TimeChip. Communication with the TimeChip is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on Data In (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the Chip Enable Output pin ($\overline{CEO}$).

After recognition is established, the next 64 read or write cycles either extract or update data in the TimeChip and Chip Enable Output remains high during this time, disabling the connected memory.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CEI}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle using the $\overline{CEI}$ and $\overline{OE}$ control of the TimeChip starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CEI}$ and $\overline{WE}$ control of the TimeChip. These 64 write cycles are used only to gain access to the TimeChip.

When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is *not* found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 1). With a correct match for 64 bits, the TimeChip is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the TimeChip to either receive data on D, or transmit data on Q, depending on the level of $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CEI}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the TimeChip.

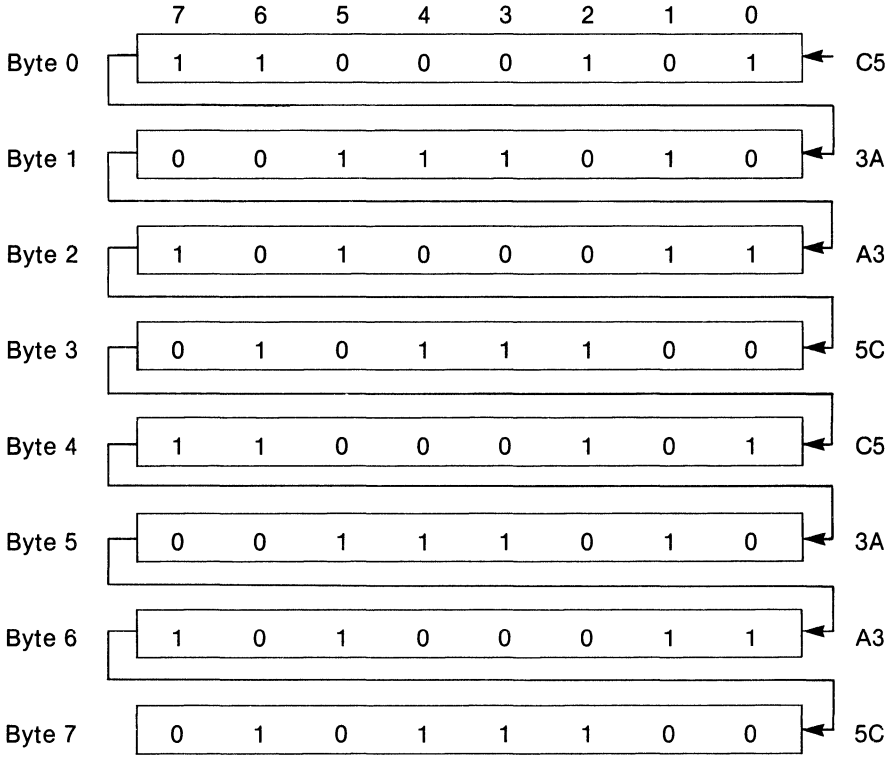
A 32,768 Hz quartz crystal, Seiko part no. DS-VT-200 or equivalent, can be directly connected to the DS1215 via pins 1 and 2 ($X_1$, $X_2$). The crystal selected for use should have a specified load capacitance ($C_L$) of 6 pF.

## NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the TimeChip is determined by the level of the ROM/$\overline{\text{RAM}}$ select pin. When ROM/$\overline{\text{RAM}}$ is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make static CMOS RAM and the timekeeping function nonvolatile. First a switch is provided to direct power from the battery inputs or $V_{CCI}$ to $V_{CCO}$ with a maximum voltage drop of 0.2 volts. The $V_{CCO}$ output pin is used to supply uninterrupted power to CMOS static RAM. The DS1215 also performs redundant battery control for high reliability. On power fail the battery with the highest voltage is automatically switched to $V_{CCO}$. If only one battery is used in the system, the unused battery input should be connected to ground. The DS1215 provides the function of safeguarding the TimeChip and RAM data by power fail detection and write protection. Power fail detection occurs when $V_{CCI}$ falls below VTP which is equal to $1.26 \times V_{BAT}$. The DS1215 constantly monitors the $V_{CCI}$ supply pin. When $V_{CCI}$ is less than VTP, a comparator outputs a power fail signal to the control logic. The power fail signal forces the chip enable output ($\overline{\text{CEO}}$) to $V_{CCI}$ or $V_{BAT} - 0.2$ volts for external RAM write protection. During nominal supply conditions, $\overline{\text{CEO}}$ will track $\overline{\text{CEI}}$ with a maximum propagation delay of 20 ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the TimeChip registers and prevents future access until $V_{CCI}$ exceeds VTP. A typical RAM/TimeChip interface is illustrated in Figure 4.

When the ROM/$\overline{\text{RAM}}$ pin is connected to $V_{CCO}$, the controller is set in the ROM mode. Since ROM is a read-only device which retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will not force $\overline{\text{CEO}}$ high when power fails. However, the TimeChip does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power fail as $V_{CCI}$ falls below the level of $V_{BAT}$. A typical ROM/TimeChip interface is illustrated in Figure 5.

**TIMECHIP COMPARISON REGISTER DEFINITION** Figure 1

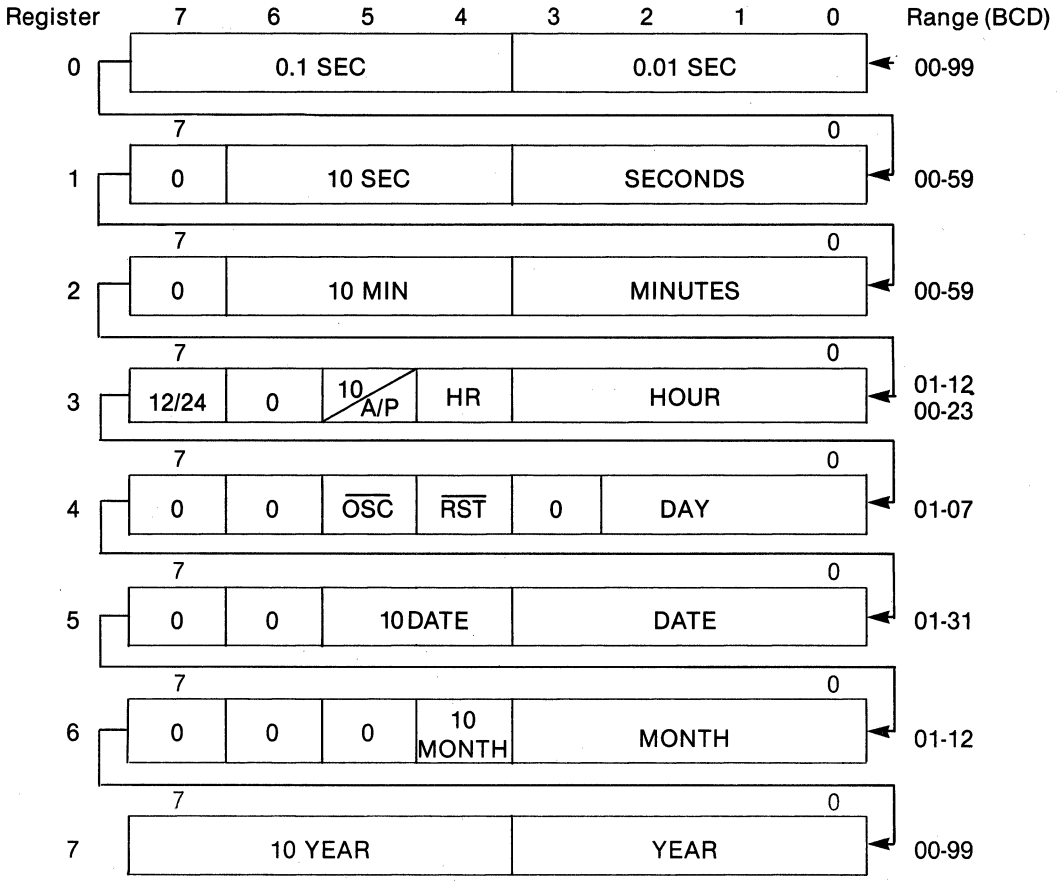



**Note:**
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the TimeChip is less than 1 in $10^{19}$.

**TIMECHIP REGISTER INFORMATION**
The TimeChip information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the TimeChip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the TimeChip registers are not binary coded decimal format (BCD) in 12-hour mode. Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

**TIMECHIP REGISTER DEFINITION** Figure 2

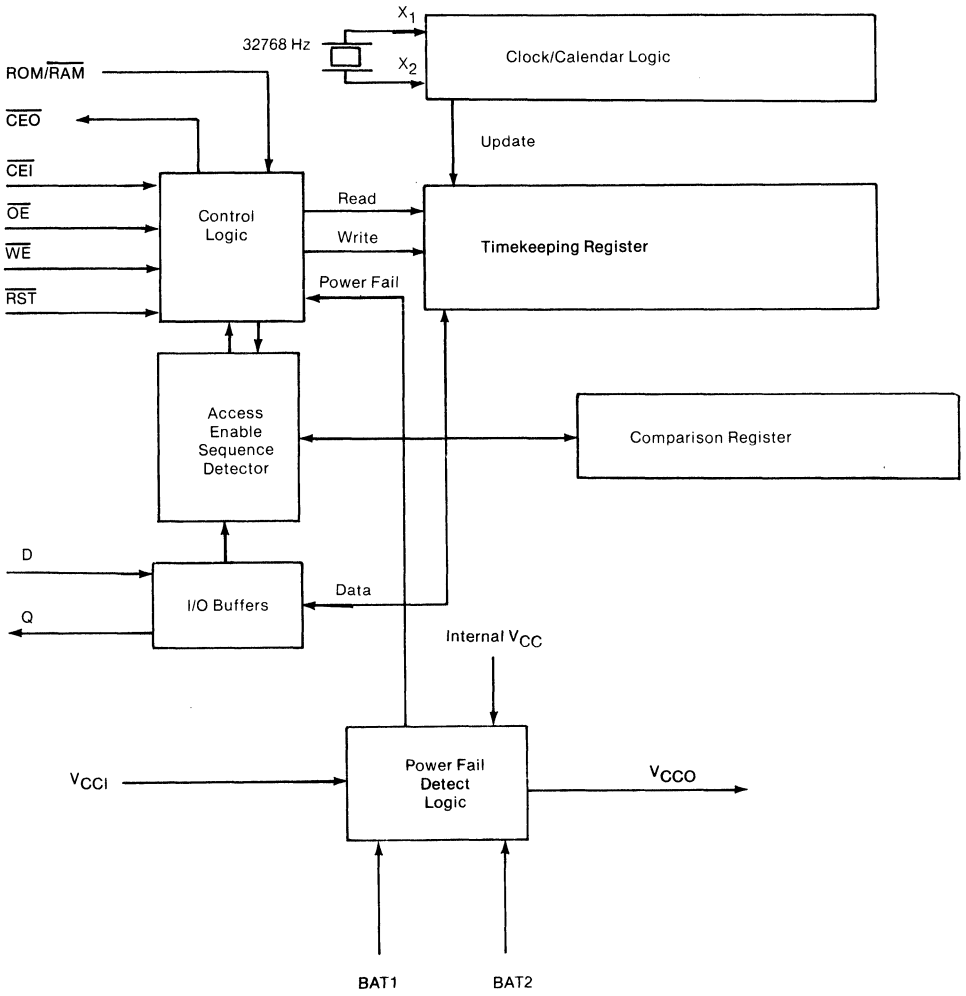



**AM-PM/12/24 MODE**
Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

**OSCILLATOR AND RESET BITS**
Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logical 1, the reset input pin is ignored. When the reset bit is set to logical 0, a low input on the reset pin will cause the TimeChip to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to Logic 0 the oscillator turns on and the watch becomes operational.

**ZERO BITS**
Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

**TIMECHIP BLOCK DIAGRAM** Figure 3

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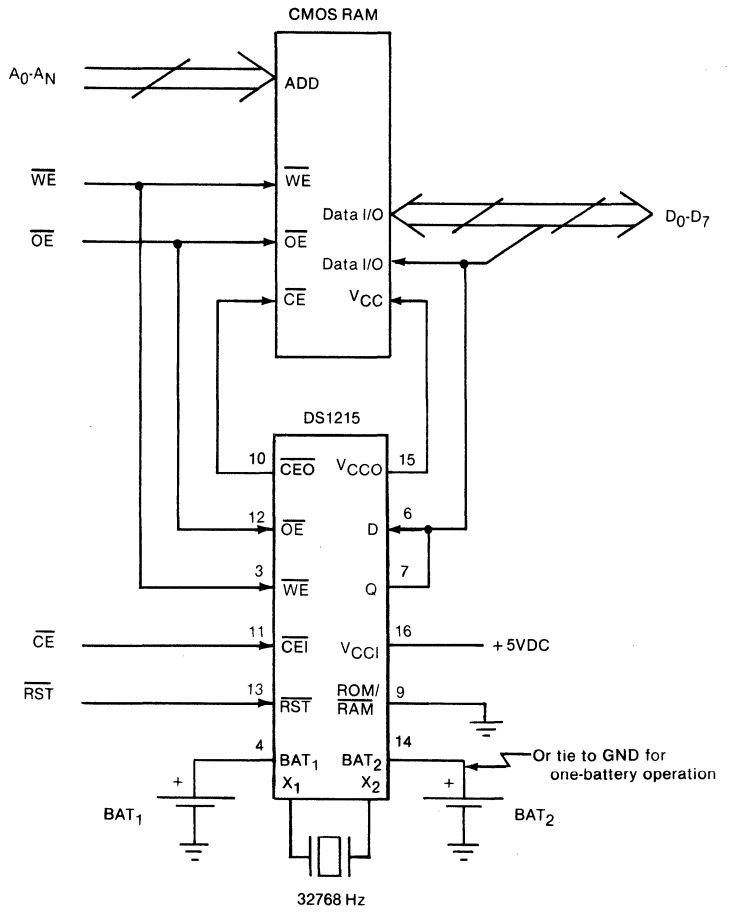
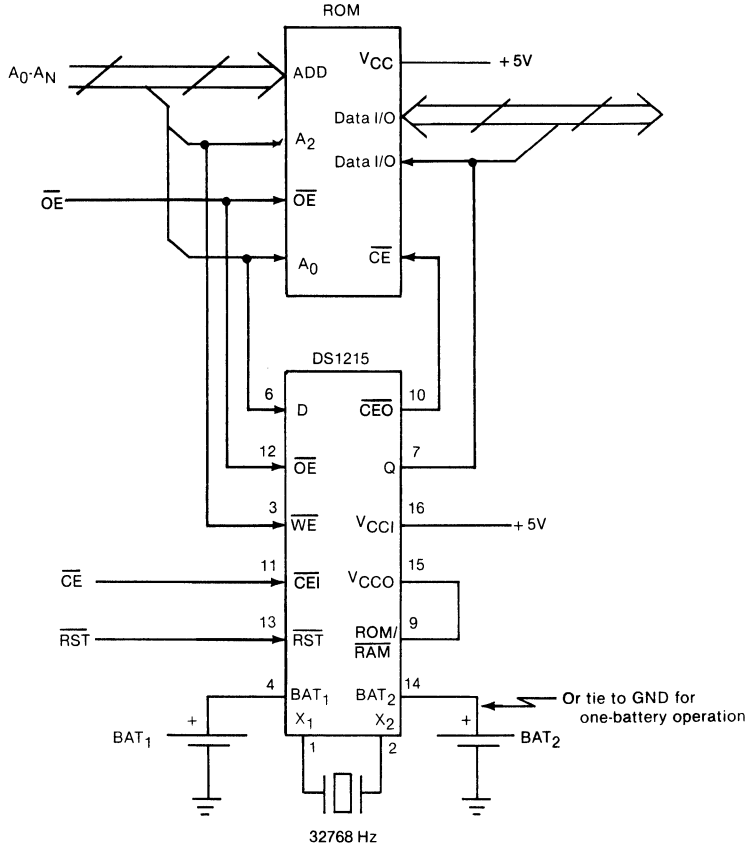
**RAM/TIMECHIP INTERFACE** Figure 4



**ROM/TIMECHIP INTERFACE** Figure 5



**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1 |
| Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| $V_{BAT1}$ or $V_{BAT2}$ Battery Voltage | $V_{BAT}$ | 2.5 | | 3.7 | V | 7 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CCI}$ | | | 5 | mA | 6 |
| Supply Current $V_{CCO}=V_{CCI}-0.2$ | $I_{CCO1}$ | | | 80 | mA | 8 |
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | μA | |
| Output Leakage | $I_{LO}$ | −1.0 | | +1.0 | μA | |
| Output @2.4V | $I_{OH}$ | −1.0 | | | mA | 2 |
| Output @0.4V | $I_{OL}$ | | | 4.0 | mA | 2 |

(0°C to 70°C, $V_{CC}$ ◁ 4.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| $\overline{CEO}$ Output | $V_{OH1}$ | $V_{CCI}$ or $V_{BAT}-0.2$ | | | V | 9 |
| $V_{BAT1}$ or $V_{BAT2}$ Battery Current | $I_{BAT}$ | | | 1 | μA | 6 |
| Battery Backup Current @$V_{CCO}=V_{BAT}-0.2V$ | $I_{CCO2}$ | | | 10 | μA | 10 |

**CAPACITANCE** ($t_A$ = 25°C)

| PARAMETER | SYMBOL | MIN | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

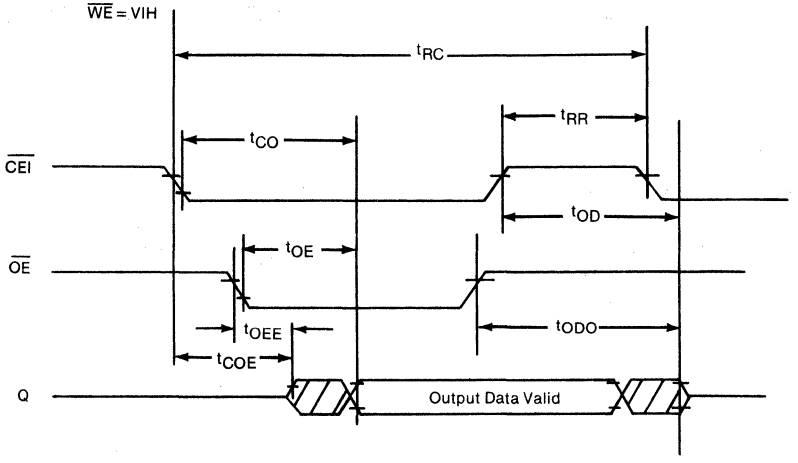
**A.C. ELECTRICAL CHARACTERISTICS** ROM/$\overline{\text{RAM}}$ = GND (0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 250 | | | ns | |
| $\overline{\text{CEI}}$ Access Time | $t_{CO}$ | | | 200 | ns | |
| $\overline{\text{OE}}$ Access Time | $t_{OE}$ | | | 100 | ns | |
| $\overline{\text{CEI}}$ To Output Low Z | $t_{COE}$ | 10 | | | ns | |
| $\overline{\text{OE}}$ To Output Low Z | $t_{OEE}$ | 10 | | | ns | |
| $\overline{\text{CEI}}$ To Output High Z | $t_{OD}$ | | | 100 | ns | |
| $\overline{\text{OE}}$ To Output High Z | $t_{ODO}$ | | | 100 | ns | |
| Read Recovery | $t_{RR}$ | 50 | | | ns | |
| Write Cycle | $t_{WC}$ | 250 | | | ns | |
| Write Pulse Width | $t_{WP}$ | 170 | | | ns | |
| Write Recovery | $t_{WR}$ | 50 | | | ns | 4 |
| Data Set Up | $t_{DS}$ | 100 | | | ns | 5 |
| Data Hold Time | $t_{DH}$ | 10 | | | ns | 5 |
| $\overline{\text{CEI}}$ Pulse Width | $t_{CW}$ | 170 | | | ns | |
| $\overline{\text{RST}}$ Pulse Width | $t_{RST}$ | 200 | | | ns | |
| $\overline{\text{CEI}}$ Propagation Delay | $t_{PD}$ | 5 | 10 | 20 | ns | 2, 3 |
| $\overline{\text{CEI}}$ High to Power Fail | $t_{PF}$ | | | 0 | ns | |

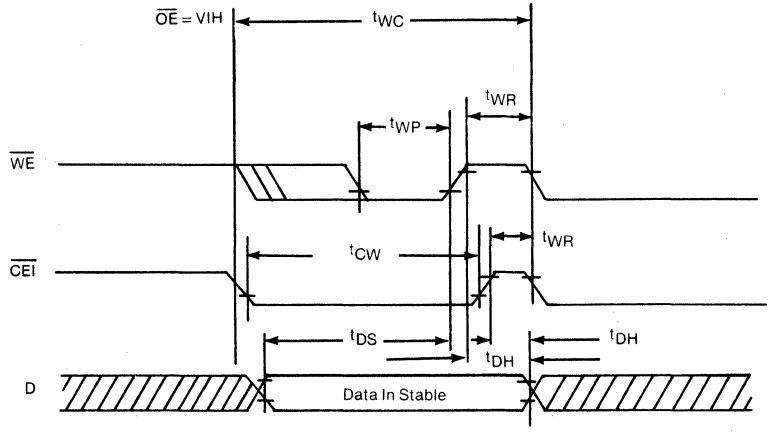
(0°C to 70°C, $V_{CC}$ < 4.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| Recovery at Power Up | $t_{REC}$ | | | 2 | ms | |
| $V_{CC}$ Slew Rate 4.5 - 3.0V | $t_F$ | 0 | | | ms | |

**TIMING DIAGRAM—READ CYCLE TO TIMECHIP** ROM/$\overline{\text{RAM}}$ = GND




**TIMING DIAGRAM—WRITE CYCLE TO TIMECHIP** ROM/$\overline{\text{RAM}}$ = GND



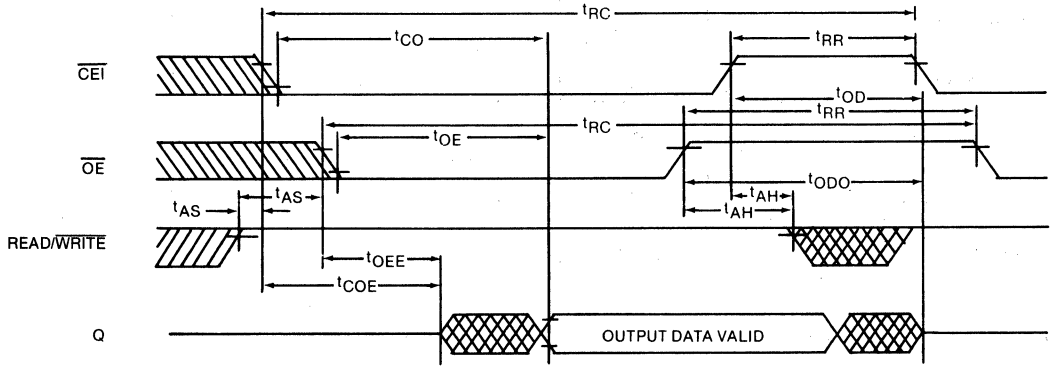
**A.C. ELECTRICAL CHARACTERISTICS** ROM/$\overline{RAM}$ = $V_{CCO}$ (0 °C to 70 °C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 250 | | | ns | |
| $\overline{CE}$I Access Time | $t_{CO}$ | | | 200 | ns | |
| $\overline{OE}$ Access Time | $t_{OE}$ | | | 200 | ns | |
| $\overline{CE}$I to Output in Low Z | $t_{COE}$ | 10 | | | ns | |
| $\overline{OE}$ to Output in Low Z | $t_{OEE}$ | 10 | | | ns | |
| $\overline{CE}$I to Output in High Z | $t_{OD}$ | | | 100 | ns | |
| $\overline{OE}$ to Output in High Z | $t_{ODO}$ | | | 100 | ns | |
| Address Set Up Time | $t_{AS}$ | 20 | | | ns | |
| Address Hold Time | $t_{AH}$ | | | 10 | ns | |
| Read Recovery | $t_{RR}$ | 50 | | | ns | |
| Write Cycle Time | $t_{WC}$ | 250 | | | ns | |
| $\overline{CE}$I Pulse Width | $t_{CW}$ | 170 | | | ns | |
| $\overline{OE}$ Pulse Width | $t_{OW}$ | 170 | | | ns | |
| Write Recovery | $t_{WR}$ | 50 | | | ns | 4 |
| Data Set Up Time | $t_{DS}$ | 100 | | | ns | 5 |
| Data Hold Time | $t_{DH}$ | 10 | | | ns | 5 |
| $\overline{RST}$ Pulse Width | $t_{RST}$ | 200 | | | ns | |
| $\overline{CE}$I Propagation Delay | $t_{PD}$ | 5 | 10 | 20 | ns | 2,3 |
| $\overline{CE}$I High to Power Fail | $t_{PF}$ | | | 0 | ns | |

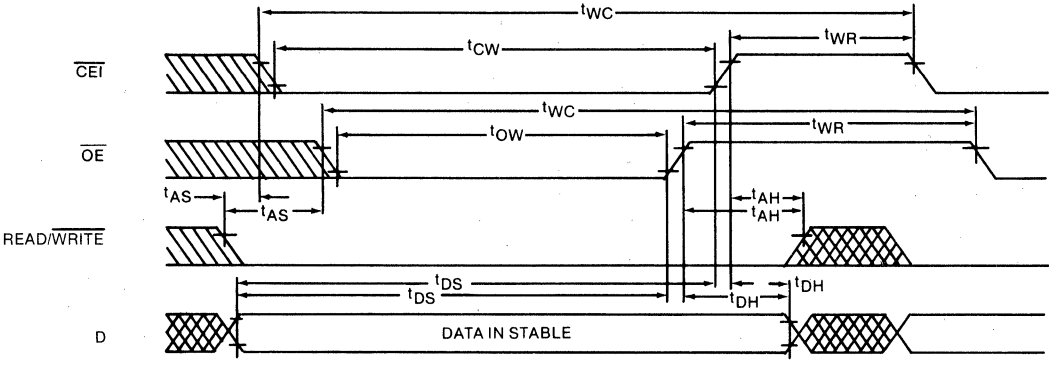
(0 °C to 70 °C, $V_{CC}$ < 4.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| Recovery at Power Up | $t_{REC}$ | | | 2 | ms | |
| $V_{CC}$ Slew Rate 4.5 -3V | $t_F$ | 0 | | | ms | |

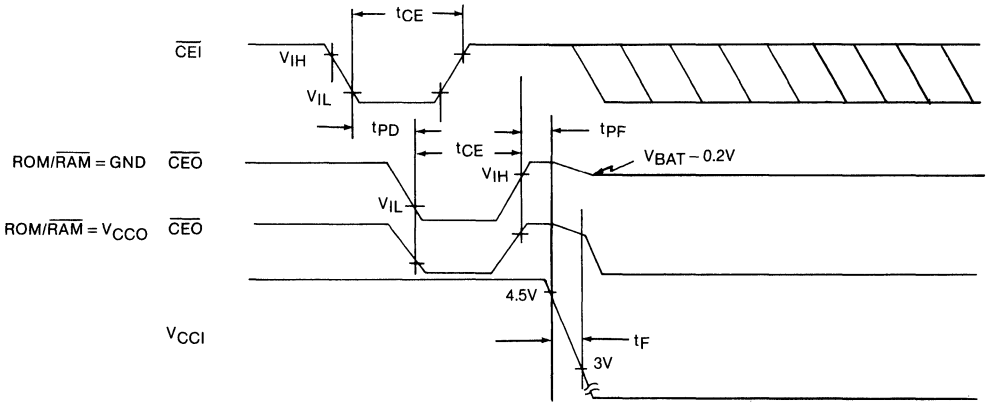
## TIMING DIAGRAM—READ CYCLE ROM/$\overline{\text{RAM}}$ = $V_{CCO}$



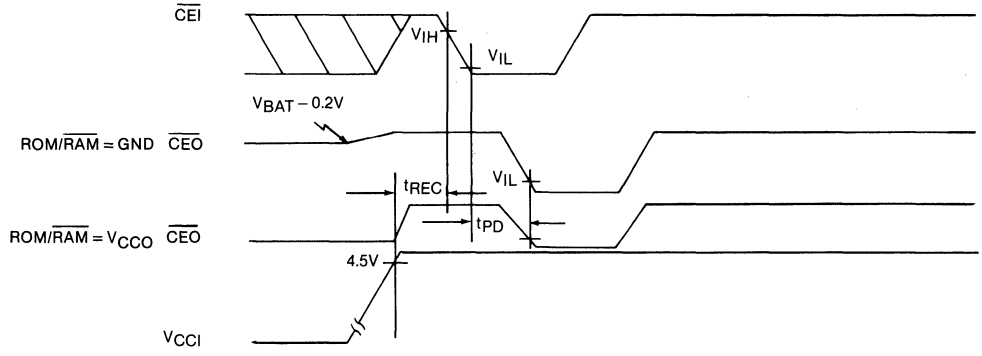

## TIMING DIAGRAM—WRITE CYCLE ROM/$\overline{\text{RAM}}$ = $V_{CCO}$



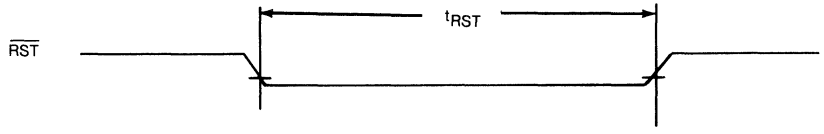
## TIMING DIAGRAM—POWER DOWN




## TIMING DIAGRAM—POWER UP



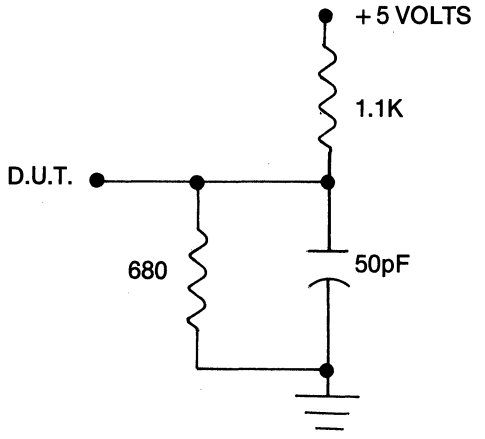

## TIMING DIAGRAM—RESET FOR TIMECHIP



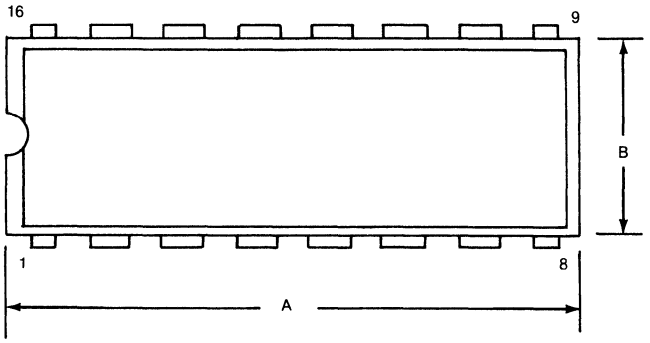
**NOTES**

1. All voltages are referenced to ground.
2. Measured with load shown in Figure 6.
3. Input pulse rise and fall times equal 10 ns.
4. $t_{WR}$ is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
5. $t_{DH}$ and $t_{DS}$ are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$ in RAM mode or $\overline{OE}$ or $\overline{CE}$ in ROM mode.
6. Measured without RAM connected.
7. Trip point voltage for power fail detect. $V_{TP} = 1.26 \times V_{BAT}$ For 10% operation $V_{BAT} = 3.5V$ max.; for 5% operation $V_{BAT} = 3.7V$ max.
8. $I_{CCO1}$ is the maximum average load current the DS1215 can supply to memory.
9. Applies to $\overline{CEO}$ with the ROM/$\overline{RAM}$ pin grounded. When the ROM/$\overline{RAM}$ pin is connected to $V_{CCO}$, $\overline{CEO}$ will go to a low level as $V_{CCI}$ falls below $V_{BAT}$.
10. $I_{CCO2}$ is the maximum average load current which the DS1215 can supply to memory in the battery backup mode.
11. Applies to all input pins except $\overline{RST}$. $\overline{RST}$ is pulled internally to $V_{CCI}$.

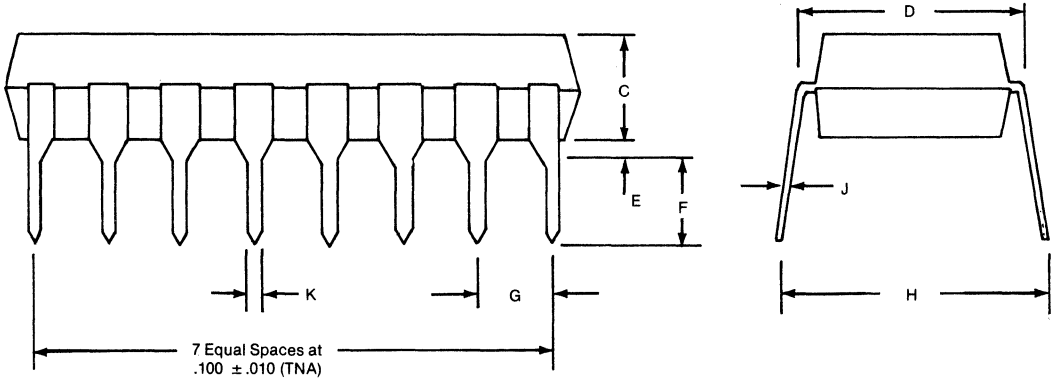
**OUTPUT LOAD** Figure 6



# DS1215
# TimeChip




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .740 | .780 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |



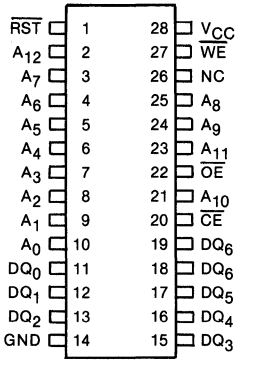

7

# Dallas Semiconductor
## *64K NV SRAM Plus Real Time Clock* — *DS1243Y*

### FEATURES

- Real Time Clock keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- 8K × 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min/month @25°C
- Over 5 years of data retention in the absence of power
- Unlimited write cycles

### PIN CONNECTIONS



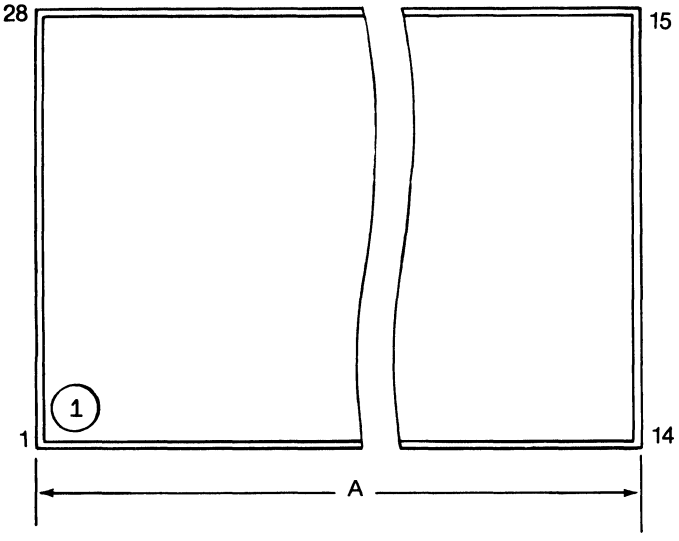

### PIN NAMES

| | |
|---|---|
| $A_0$-$A_{12}$ | - Address Inputs |
| $\overline{CE}$ | - Chip Enable |
| GND | - Ground |
| $DQ_0$-$DQ_7$ | - Data In/Data Out |
| $V_{CC}$ | - Power (+5V) |
| $\overline{WE}$ | - Write Enable |
| $\overline{OE}$ | - Output Enable |
| NC | - No Connect |
| $\overline{RST}$ | - Reset |

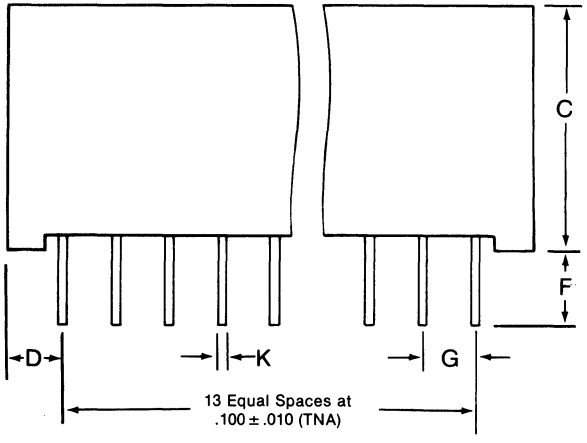
### DESCRIPTION

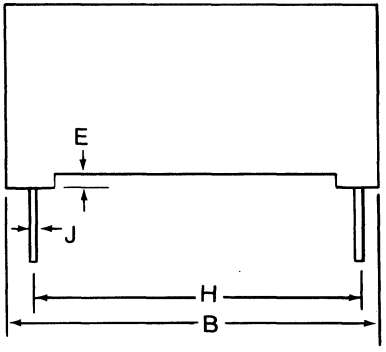
The DS1243Y is a fully static nonvolatile RAM (organized as 8192 words by 8 bits) with built-in Real Time Clock. This memory and real time clock has a self-contained lithium energy source and control circuitry which constantly monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock. For complete information and operation, electrical characteristics, and timing as it relates to the 8K × 8 nonvolatile memory, please reference the DS1225Y data sheet. For complete information on operation, access control, electrical characteristics and timing of the real time clock, reference the DS1216 data sheet.

# DS1243Y
# 64K NV SRAM Plus Real Time Clock




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.520 | 1.540 |
| B | .695 | .720 |
| C | .395 | .410 |
| D | .090 | .120 |
| E | .020 | .030 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |




7

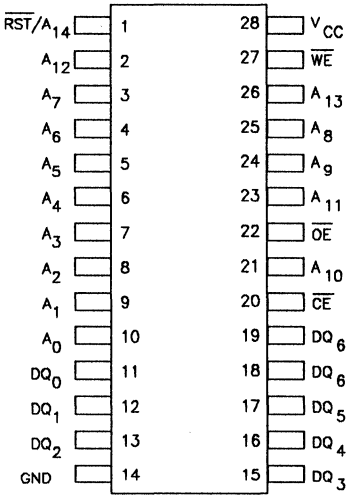
# Dallas Semiconductor
## *256K NV SRAM Plus Real Time Clock*

**PRELIMINARY**
***DS1244Y***

### FEATURES

- Real Time Clock keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- 32K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than +/- 1 min/month @25°C
- Over 5 years of data retention in the absence of power
- Unlimited write cycles

### PIN CONNECTIONS



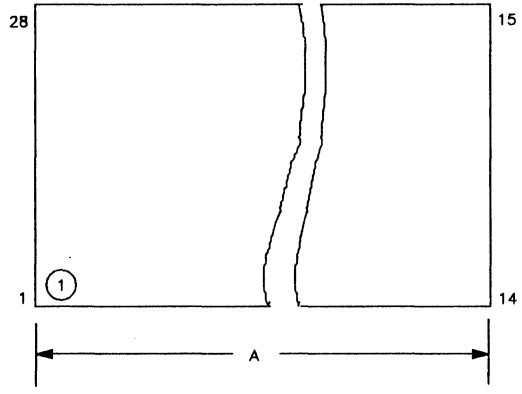

### PIN NAMES

| | |
|---|---|
| $A_0$-$A_{14}$ | - Address Inputs |
| $\overline{CE}$ | - Chip Enable |
| GND | - Ground |
| $DQ_0$-$DQ_7$ | - Data In/Data Out |
| Vcc | - Power (+5V) |
| $\overline{WE}$ | - Write Enable |
| $\overline{OE}$ | - Output Enable |
| $\overline{RST}$ | - Reset |

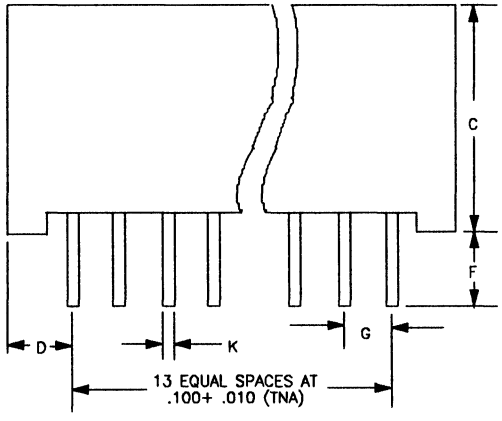
### DESCRIPTION

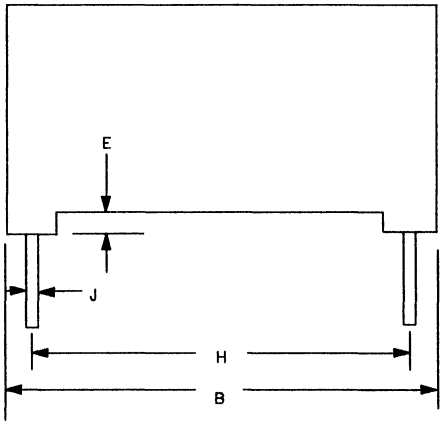
The DS1244Y is a fully static nonvolatile RAM (organized as 32,768 words by 8 bits) with built-in Real Time Clock. This memory and real time clock has a self-contained lithium energy source and control circuitry which constantly monitors Vcc for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock. For complete information and operation, electrical characteristics, and timing as it relates to the 32K x 8 nonvolatile memory, please reference the DS1230Y data sheet. For complete information on operation, access control, electrical characteristics and timing of the real time clock, reference the DS1216 data sheet.

# DS1244Y
# 256K NV SRAM Plus Real Time Clock




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.520 | 1.540 |
| B | .695 | .720 |
| C | .395 | .410 |
| D | .090 | .120 |
| E | .020 | .030 |
| F | .120 | .160 |
| G | .090 | .110 |
| H | .590 | .630 |
| J | .008 | .012 |
| K | .015 | .021 |



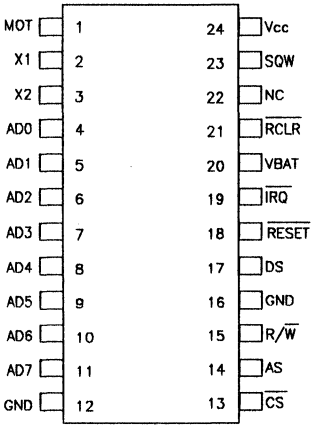
# Dallas Semiconductor
## *Real Time Clock Plus RAM*

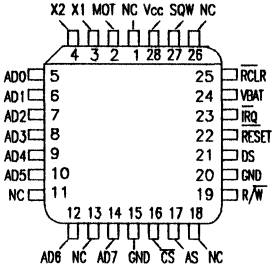
## *DS1285-24 Pin DIP*
## *DS1285Q-28 Pin PLCC*

### FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin configuration closely matches MC146818A
- Counts seconds, minutes, hours, days, day of the week, date, month and year with leap year compensation
- Binary or BCD representation of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122us to 500ms
  - End of clock update cycle
- Optional 28 pin PLCC surface mount package

### PIN CONNECTIONS




### PIN NAMES

AD0-AD7- Multiplexed Address/Data Bus
N.C. - No Connection
MOT - Bus Type Selection
$\overline{CS}$ - Chip Select
AS - Address Strobe
R/$\overline{W}$ - Read/Write Input
DS - Data Strobe
$\overline{RESET}$ - Reset Input
$\overline{IRQ}$ - Interrupt Request Output
SQW - Square Wave Output
Vcc - +5 Volt Supply
GND - Ground
X1,X2 - 32.768 KHz Crystal Connections
$V_{BAT}$ - +3 volt Battery Input
$\overline{RCLR}$ - RAM Clear

### DESCRIPTION

The DS1285 Real Time Clock Plus RAM is designed as a direct replacement for the MC146818 in IBM AT computer clock/calendar and other applications. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and signal descriptions other than X1,X2, $V_{BAT}$, and $\overline{RCLR}$, see the DS1287 data sheet.

## SIGNAL DESCRIPTIONS

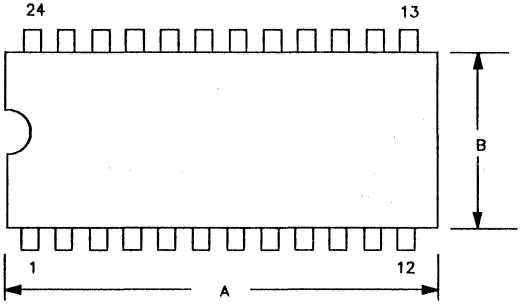
X1,X2 - Connections for a standard 32.768 KHz quartz crystal, Seiko part number DS-VT-200 or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance ($C_L$) of 6pF. A variable triming capacitor may be required for extremely high precision timekeeping applications.

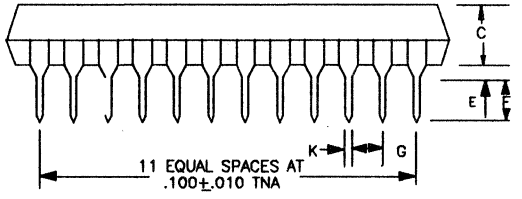
$V_{BAT}$ - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2 and 4 volts for proper operation. The nominal write protect trip point voltage at which access to the Real Time Clock and User RAM is denied is set by the internal circuitry as 1.26 x $V_{BAT}$. A maximum load of .5uA at 25°C in the absence of power should be used to size the external energy source.

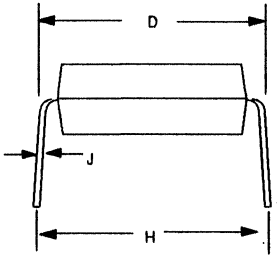
$\overline{RCLR}$ - The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not effect the RAM associated with the Real Time Clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (-0.3 to 0.8 volts) during battery back up mode when $V_{CC}$ is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers.

# DS1285
# REAL TIME CLOCK PLUS RAM

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.240 | 1.280 |
| B | .540 | .560 |
| C | .140 | .160 |
| D | .590 | .610 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .600 | .680 |
| J | .008 | .012 |
| K | .015 | .021 |

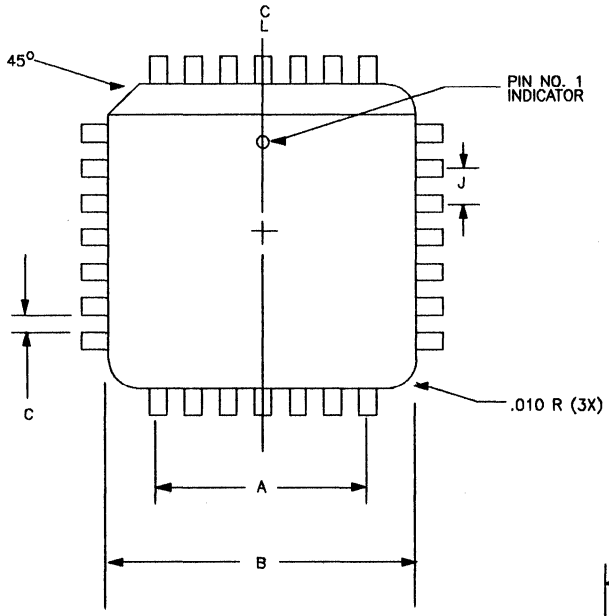


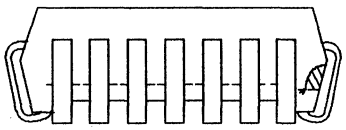



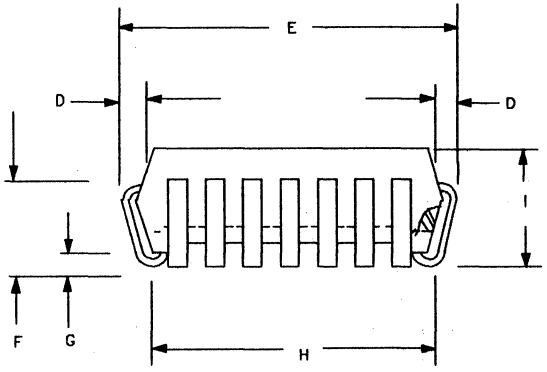



# DS1285Q
# REAL TIME CLOCK PLUS RAM

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .290 | .310 |
| B | .441 | .451 |
| C | .020 | .024 |
| D | .018 | .022 |
| E | .488 | .492 |
| F | .118 | .122 |
| G | .020 | .030 |
| H | .390 | .430 |
| J | ..048 | ..052 |






7

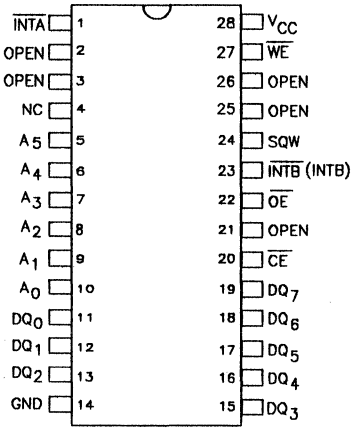
# Dallas Semiconductor
## *Watchdog Timekeeper*

## *PRODUCT PREVIEW*
## *DS1286*

### FEATURES

- Watchdog TimeKeeper keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months and years
- Watchdog Timer restarts an out of control processor
- Alarm function provides notice of real time related occurances
- Embedded lithium energy cell maintains time, Watchdog, and alarm information
- Programmable interrupts and square wave outputs maintain 28 pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than +/- 1 minute/month at 25° C
- Greater than 10 years of data retention in the absence of Vcc
- 50 bytes of user NV RAM

### PIN DESCRIPTION




### PIN NAMES

| | |
|---|---|
| $\overline{INTA}$ | - Interrupt Output A |
| $\overline{INTB}$(INTB) | - Interrupt Output B |
| A0-A5 | - Address Inputs |
| DQ0-DQ7 | - Data Input/Output |
| $\overline{CE}$ | - Chip Enable |
| $\overline{OE}$ | - Output Enable |
| $\overline{WE}$ | - Write Enable |
| Vcc | - +5 Volts |
| GND | - Ground |
| N.C. | - No Connection |
| OPEN | - Pin Missing |
| SQW | - Square Wave Output |

### DESCRIPTION

The DS1286 Watchdog TimeKeeper is a self contained Real Time Clock, Alarm, Watchdog Timer, and Interval Timer in a 28 pin JEDEC DIP package. The DS1286 contains an embedded Lithium energy source and a watch crystal which eliminates need for any external circuitry. Data contained within 64 eight bit registers can be read or written in the same manner as bytewide static RAM. Data is maintained in the Watchdog TimeKeeper by intelligent control circuitry which detects the status of Vcc and write protects memory when Vcc is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of Vcc. The Watchdog Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The data at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The Watchdog TimeKeeper operates in either 24 hour or 12 hour format with an AM/PM indicator. The Watchdog timer provides alarm windows and interval timing between .01 seconds and 99 seconds. The real time alarm provides for preset times of up to one week.

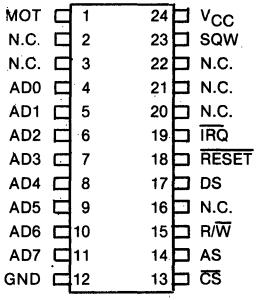
# Dallas Semiconductor
## *RealTime Clock Plus RAM*

## *DS1287*

### FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month and year with leap year compensation
- Binary or BCD representation of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 *us* to 500 ms
  - End of clock update cycle

### PIN CONNECTIONS




### PIN NAMES

| | | |
|---|---|---|
| AD0 - AD7 | - | Multiplexed Address/Data Bus |
| N.C. | - | No Connection |
| MOT | - | Bus Type Selection |
| $\overline{CS}$ | - | Chip Select |
| AS | - | Address Strobe |
| R/$\overline{W}$ | - | Read/Write Input |
| DS | - | Data Strobe |
| $\overline{RESET}$ | - | Reset Input |
| $\overline{IRQ}$ | - | Interrupt Request Output |
| SQW | - | Square Wave Output |
| $V_{CC}$ | - | +5 Volt Supply |
| GND | - | Ground |

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## DESCRIPTION

The DS1287 RealTime Clock Plus RAM is designed to be a direct replacement for the MC146818. A lithium energy source, quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS1287 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The RealTime Clock Plus RAM is distinctive in that time-of-day and memory are maintained even in the absence of power.

## OPERATION

The block diagram in Figure 1 shows the pin connection with the major internal functions of the DS1287 Real Time Clock Plus RAM. The following paragraphs describe the function of each pin.

## POWER DOWN/POWER UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar and alarm memory locations remain nonvolatile regardless of the level of the $V_{CC}$ input. When $V_{CC}$ is applied to the DS1287 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When $V_{CC}$ falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin and DS1287 is, therefore, write-protected. When the DS1287 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When $V_{CC}$ falls below a level of approximately 3 volts, the external $V_{CC}$ supply is switched off and an internal Lithium energy source supplies power to the Real Time Clock and the RAM memory.

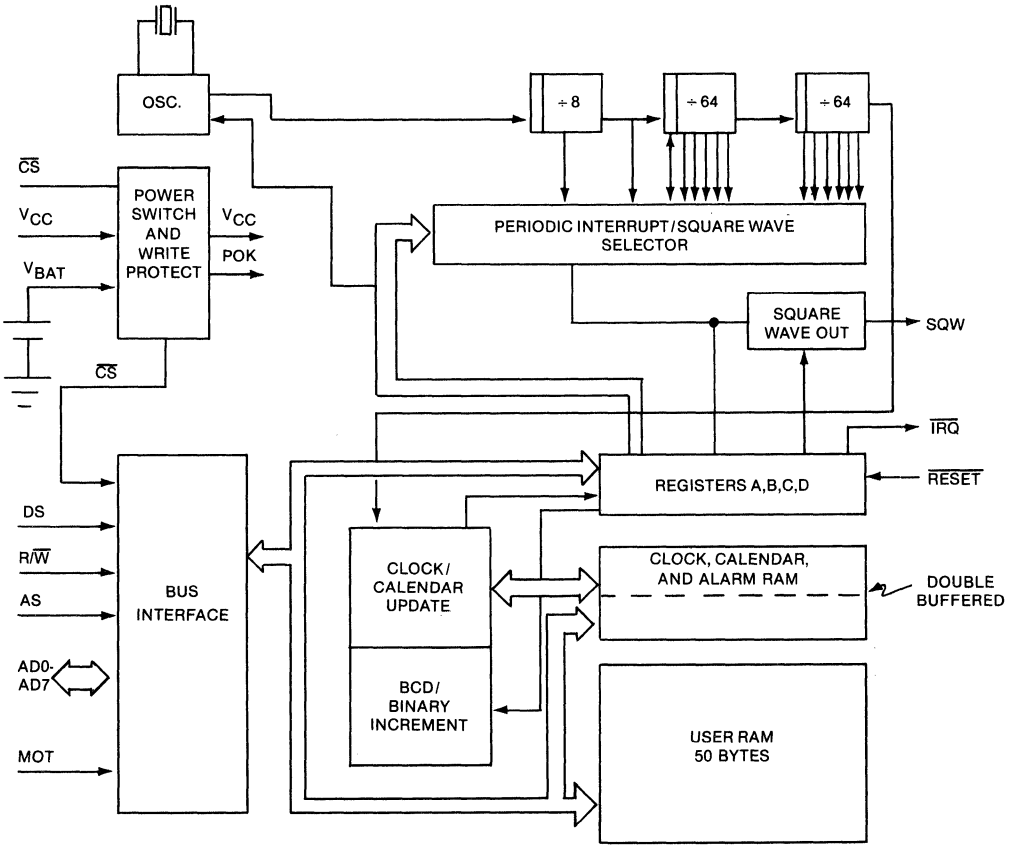
## SIGNAL DESCRIPTIONS

**GND, $V_{CC}$**—D.C. power is provided to the device on these pins. $V_{CC}$ is the +5 volt input. When 5 volts is applied within normal limits, the device is fully accessible and data can be written and read. When $V_{CC}$ is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As $V_{CC}$ falls below 3 volts typical, the RAM and TimeKeeper are switched over to an internal Lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the $V_{CC}$ pin.

**MOT (Mode Select)**—The MOT pin offers the flexibility to choose between two bus types. When connected to $V_{CC}$, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 KΩ.

**SQW (Square Wave Output)**—The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin may be changed by programming Register A. As shown in Table 1, the SQW signal may be turned on and off using the SQWE bit in Register B. The SQW signal is not available when $V_{CC}$ is less than 4.25 volts typical.

**BLOCK DIAGRAM DS1287** Figure 1

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**PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY** Table 1

| SELECT BITS REGISTER A | | | | $t_{PI}$ PERIODIC INTERRUPT RATE | SQW OUTPUT FREQUENCY |
|---|---|---|---|---|---|
| RS3 | RS2 | RS1 | RS0 | | |
| 0 | 0 | 0 | 0 | None | None |
| 0 | 0 | 0 | 1 | 3.90625 ms | 256 Hz |
| 0 | 0 | 1 | 0 | 7.8125 ms | 128 Hz |
| 0 | 0 | 1 | 1 | 122.070 *us* | 8.192 KHz |
| 0 | 1 | 0 | 0 | 244.141 *us* | 4.096 KHz |
| 0 | 1 | 0 | 1 | 488.281 *us* | 2.048 KHz |
| 0 | 1 | 1 | 0 | 976.5625 *us* | 1.024 KHz |
| 0 | 1 | 1 | 1 | 1.953125 ms | 512 Hz |
| 1 | 0 | 0 | 0 | 3.90625 ms | 256 Hz |
| 1 | 0 | 0 | 1 | 7.8125 ms | 128 Hz |
| 1 | 0 | 1 | 0 | 15.625 ms | 64 Hz |
| 1 | 0 | 1 | 1 | 31.25 ms | 32 Hz |
| 1 | 1 | 0 | 0 | 62.5 ms | 16 Hz |
| 1 | 1 | 0 | 1 | 125 ms | 8 Hz |
| 1 | 1 | 1 | 0 | 250 ms | 4 Hz |
| 1 | 1 | 1 | 1 | 500 ms | 2 Hz |

**AD0-AD7 (Multiplexed Bi-Directional Address/Data Bus)**—Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are presented during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1287 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS1287 latches the address from AD0 to AD5. Valid write data must be present and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle the DS1287 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as $\overline{RD}$ transitions high in the case of Intel timing.

**AS (Address Strobe Input)**—A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS1287.

**DS (Data Strobe or Read Input)**—The DS/$\overline{RD}$ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to $V_{CC}$, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS1287 is to drive the bi-directional bus. In write cycles the trailing edge of DS causes the DS1287 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read ($\overline{RD}$). $\overline{RD}$ identifies the time period when the DS1287 drives the bus with read data. The $\overline{RD}$ signal is the same definition as the Output Enable ($\overline{OE}$) signal on a typical memory.

**R/$\overline{W}$ (Read/Write Input)**—The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to $V_{CC}$ for Motorola timing, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active low signal called $\overline{WR}$. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{WE}$) on generic RAMs.

**$\overline{CS}$ (Chip Select Input)**—The Chip Select signal ($\overline{CS}$) must be asserted low for a bus cycle in which the DS1287 is to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during $\overline{RD}$ and $\overline{WR}$ for Intel timing. Bus cycles which take place without asserting $\overline{CS}$ will latch addresses but no access will occur. When $V_{CC}$ is below 4.25 volts, the DS1287 internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the Real Time Clock data and RAM data during power outages.

**$\overline{IRQ}$ (Interrupt Request Output)**—The $\overline{IRQ}$ pin is an active low output of the DS1287 that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices may be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pullup resistor.

**RESET (Reset Input)**—The $\overline{\text{RESET}}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{\text{RESET}}$ pin may be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{\text{RESET}}$ is held low is dependent on the application. However, if $\overline{\text{RESET}}$ is used on power up, the time $\overline{\text{RESET}}$ is low should exceed 200 ms to make sure that the internal timer which controls the DS1287 on power-up has timed out. When $\overline{\text{RESET}}$ is low and $V_{CC}$ is above 4.25 volts, the following occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.
B. Alarm Interrupt Enable (AIE) bit is cleared to zero.
C. Update Ended Interrupt Flag (UF) bit is cleared to zero.
D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.
E. Periodic Interrupt Flag (PF) bit is cleared to zero.
F. The device is not accessible until $\overline{\text{RESET}}$ is returned high.
G. Alarm Interrupt Flag (AF) bit is cleared to zero.
H. $\overline{\text{IRQ}}$ pin is in the high impedance state.
I. Square Wave Output Enable ($\overline{\text{SQWE}}$) bit is cleared to zero.
J. Update Ended Interrupt Enable (UIE) is cleared to zero.

In a typical application $\overline{\text{RESET}}$ may be connected to $V_{CC}$. This connection will allow the DS1287 to go in and out of power fail without affecting any of the control registers.

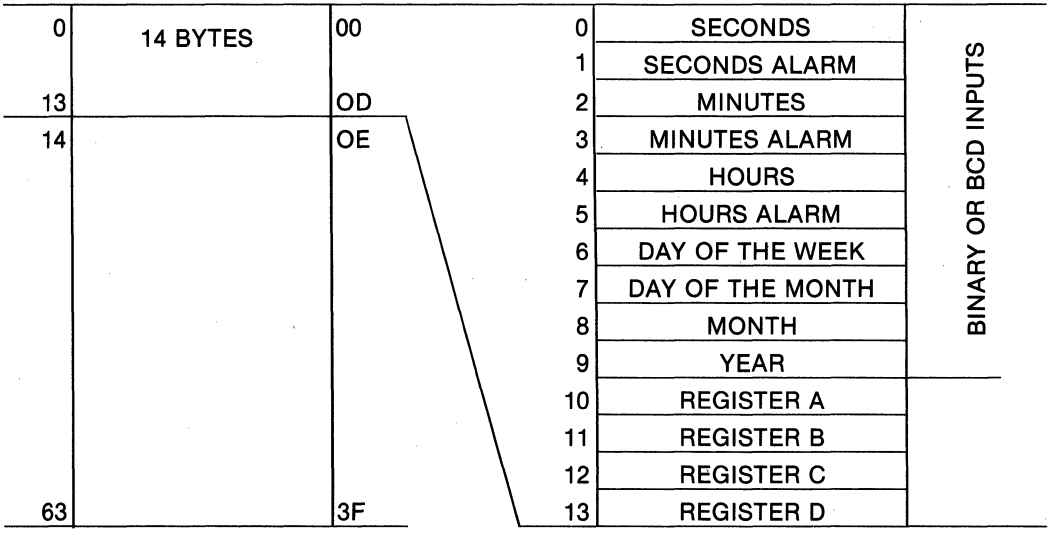
## ADDRESS MAP

The Address Map of the DS1287 is shown in Figure 2. The address map consists of 50 bytes of user RAM, 10 bytes of RAM which contain the RTC time, calendar and alarm data, and 4 bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four control registers (A, B, C, and D) are described in the "Register" section.

**ADDRESS MAP DS1287** Figure 2



**TIME, CALENDAR AND ALARM LOCATIONS**

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar and alarm bytes may be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logical one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar and alarm registers in a selected format (Binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the Real Time Clock to update the time and calendar bytes. Once initialized, the Real Time Clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the Binary and BCD formats of the ten time, calendar and alarm locations. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists that seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

**TIME CALENDAR AND ALARM DATA MODES** Table 2

| ADDRESS LOCATION | FUNCTION | DECIMAL RANGE | RANGE | |
|---|---|---|---|---|
| | | | BINARY DATA MODE | BCD DATA MODE |
| 0 | Seconds | 0-59 | 00-3B | 00-59 |
| 1 | Seconds Alarm | 0-59 | 00-3B | 00-59 |
| 2 | Minutes | 0-59 | 00-3B | 00-59 |
| 3 | Minutes Alarm | 0-59 | 00-3B | 00-59 |
| 4 | Hours - 12-hr Mode | 1-12 | 01-0C AM, 81-8C PM | 01-12 AM, 81-92 PM |
| | Hours - 24-hr Mode | 0-23 | 00-17 | 00-23 |
| 5 | Hours Alarm - 12-hr | 1-12 | 01-0C AM, 81-8C PM | 01-12 AM, 81-92 PM |
| | Hours Alarm - 24-hr | 0-23 | 00-17 | 00-23 |
| 6 | Day of the Week Sunday = 1 | 1-7 | 01-07 | 01-07 |
| 7 | Date of the Month | 1-31 | 01-1F | 01-31 |
| 8 | Month | 1-12 | 01-0C | 01-12 |
| 9 | Year | 0-99 | 00-63 | 00-99 |

The three alarm bytes may be used in two ways. First, when the alarm time is written in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any

hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at Logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

**NONVOLATILE RAM**

The 50 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1287. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

**INTERRUPTS**

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt may be programmed to occur at rates from once per second to once per day. The periodic interrupt may be selected for rates from 500 ms to 122 *u*s. The update-ended interrupt may be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a Logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to Logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two or three bits may be set when reading Register C. Each utilized flag bit should be examined when read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in Bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1287. The act of reading Register C clears all active flag bits and the IRQF bit.

**OSCILLATOR CONTROL BITS**
When the DS1287 is shipped from the factory, the internal oscillator is turned off. This feature prevents the Lithium energy cell from being used until it is installed in system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

**SQUARE WAVE OUTPUT SELECTION**
Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square wave enable bit (SQWE).

**PERIODIC INTERRUPT SELECTION**
The periodic interrupt will cause the $\overline{IRQ}$ pin to go to an active state from once every 500 ms to once every 122 *us*. This function is separate from the alarm interrupt which may be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs,create output intervals, or await the next needed software function.



**UPDATE CYCLE**
The DS1287 executes an update cycle once per second regardless of the set bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information are consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

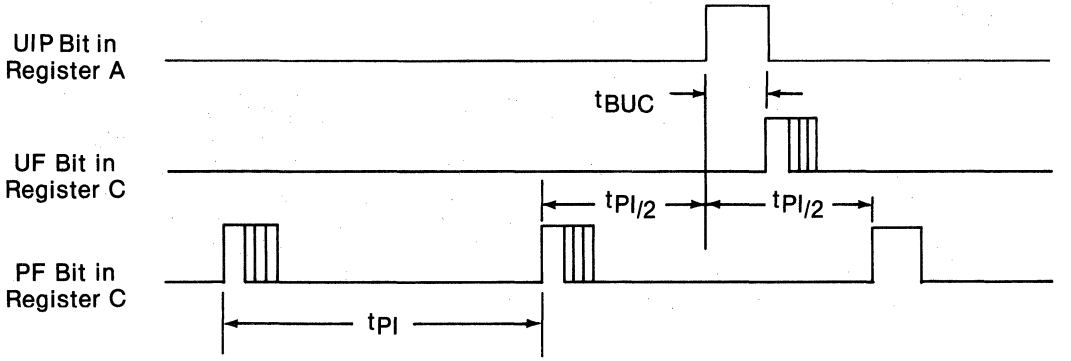
There are three methods which can be employed to handle access of the Real Time Clock which avoids any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 *us* later. If a low is read on the UIP bit, the user has at least

244 *us* before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 *us*.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than $t_{BUC}$ allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($T_{PI}/2+t_{BUC}$) to insure that data is not read during the update cycle.

**UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP** Figure 3




$t_{PI}$ = Periodic interrupt time interval per Table 1.

$t_{BUC}$ = Delay time before update cycle = 244 *us*.

## REGISTERS

The DS1287 has four control registers which are accessible at all times, even during the update cycle.

### REGISTER A

MSB LSB

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| UIP | DV2 | DV1 | DV0 | RS3 | RS2 | RS1 | RS0 |

**UIP**
The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 *us*. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a "1" inhibits any update transfer and clears the UIP status bit.

**DV0, DV1, DV2**
These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits which will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1 and DV2.

**RS3, RS2, RS1, RS0**
These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user may do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and the same rate; or
4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.



**REGISTER B**

MSB LSB

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| SET | PIE | AIE | UIE | SQWE | DM | 24/12 | DSE |

**SET**
When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit which is not modified by $\overline{\text{RESET}}$ or internal functions of the DS1287.

**PIE**
The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to cause the $\overline{\text{IRQ}}$ pin to be driven low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3 through RS0 bits of Register A. A zero in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1287 functions, but is cleared to zero on $\overline{\text{RESET}}$.

**AIE**
The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a one permits the Alarm Flag (AF) bit in register C to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the $\overline{IRQ}$ signal. The $\overline{RESET}$ pin clears AIE to zero. The internal functions of the DS1287 do not affect the AIE bit.

**UIE**
The Update Ended Interrupt Enable (UIE) bit is a read/write bit which enables the Update End Flag (UF) bit in Register C to assert $\overline{IRQ}$. The $\overline{RESET}$ pin going low or the SET bit going high clears the UIE bit.

**SQWE**
When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the $\overline{RESET}$ pin. SQWE is a read/write bit.

**DM**
The Data Mode (DM) bit indicates whether time and calendar information are in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{RESET}$. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

**24/12**
The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is a read/write and is not affected by internal functions or $\overline{RESET}$.

**DSE**
The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET.

**REGISTER C**

MSB LSB

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| IRQF | PF | AF | UF | 0 | 0 | 0 | 0 |

**IRQF**
The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1

AF = AIE = 1

UF = UIE = 1

*i.e.*, IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a one the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

**PF**
The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{RESET}$ or a software read of Register C.

**AF**
A one in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A $\overline{RESET}$ or a read of Register C will clear AF.

**UF**
The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or a $\overline{RESET}$.

**BIT 0 THROUGH BIT 3**
These are unused bits of the status Register C. These bits always read zero and cannot be written.

**REGISTER D**

MSB LSB

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| VRT | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**VRT**
The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal Lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RESET}$.

**BIT 6 THROUGH BIT 0**
The remaining bits of Register D are not usable. They cannot be written and when read, they will always read zero.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1 |
| Input Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Current | $I_{CC1}$ | | 7 | 15 | mA | 2 |
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | uA | 3 |
| I/O Leakage | $I_{LO}$ | −1.0 | | +1.0 | uA | 4 |
| Input Current | $I_{MOT}$ | −1.0 | | +500 | uA | 3 |
| Output @2.4V | $I_{OH}$ | −1.0 | | | mA | 1,5 |
| Output @0.4V | $I_{OL}$ | | | 4.0 | mA | 1 |

**CAPACITANCE** ($t_A$ = 25°C)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC}$ = 4.5V to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Cycle Time | $t_{CYC}$ | 953 | | D.C. | ns | |
| Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High | $PW_{EL}$ | 300 | | | ns | |
| Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low | $PW_{EH}$ | 325 | | | ns | |
| Input Rise and Fall Time | $t_R$, $t_F$ | | | 30 | ns | |
| R/$\overline{W}$ Hold Time | $t_{RWH}$ | 10 | | | ns | |
| R/$\overline{W}$ Set-Up Time Before DS/E | $t_{RWS}$ | 80 | | | ns | |
| Chip Select Set-Up Time Before DS, $\overline{WR}$ or $\overline{RD}$ | $t_{CS}$ | 25 | | | ns | |
| Chip Select Hold Time | $t_{CH}$ | 0 | | | ns | |
| Read Data Hold Time | $t_{DHR}$ | 10 | | 100 | ns | |
| Write Data Hold Time | $t_{DWH}$ | 0 | | | ns | |
| Muxed Address Valid Time to AS/ALE Fall | $t_{ASL}$ | 50 | | | ns | |
| Muxed Address Hold Time | $t_{AHL}$ | 20 | | | ns | |
| Delay Time DS/E to AS/ALE Rise | $t_{ASD}$ | 50 | | | ns | |
| Pulse Width AS/ALE High | $PW_{ASH}$ | 60 | | | ns | |
| Delay Time, AS/ALE to DS/E Rise | $t_{ASED}$ | 60 | | | ns | |
| Output Data Delay Time From DS/E or $\overline{RD}$ | $t_{DDR}$ | 20 | | 240 | ns | 6 |
| Data Set-Up Time | $t_{DSW}$ | 200 | | | ns | |
| Reset Pulse Width | $t_{RWL}$ | 5 | | | *us* | |
| $\overline{IRQ}$ Release from DS | $t_{IRDS}$ | | | 2 | *us* | |
| $\overline{IRQ}$ Release from $\overline{RESET}$ | $t_{IRR}$ | | | 2 | *us* | |

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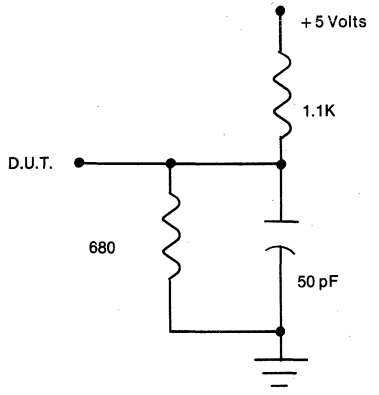
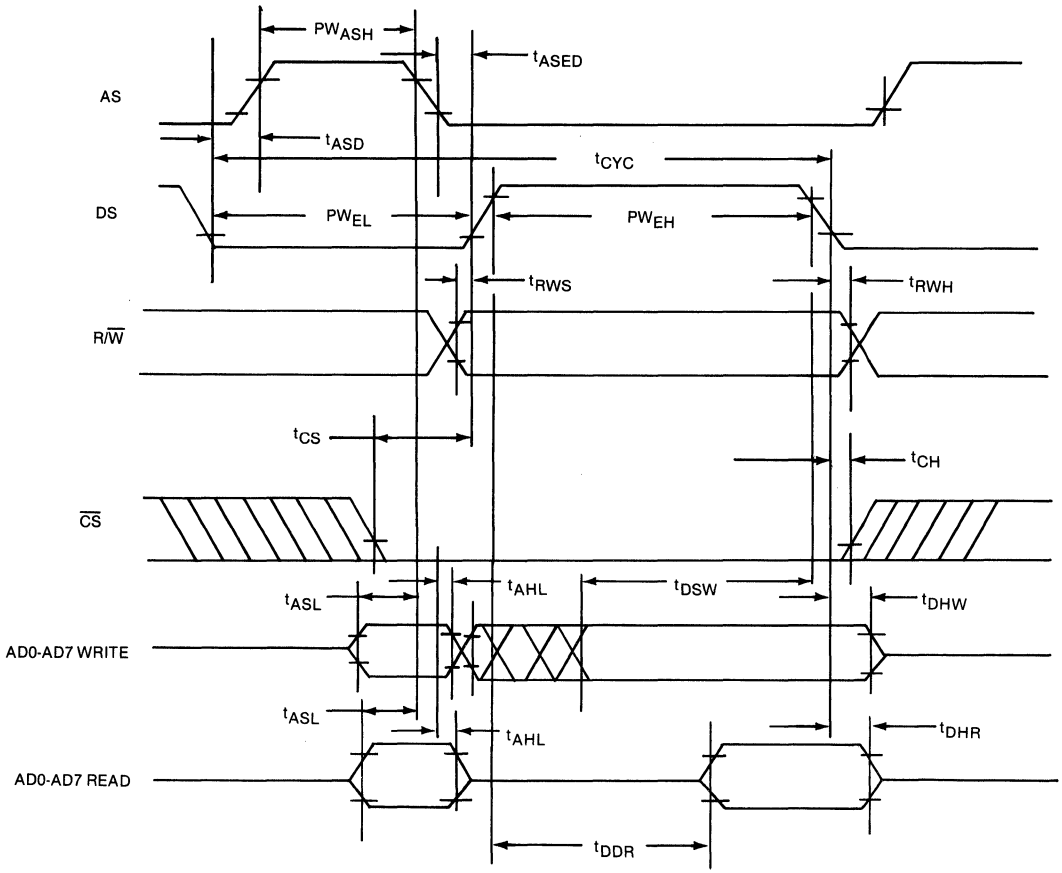
**NOTES:**

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pulldown of 20KΩ.
4. Applies to the AD0-AD7 pins, the $\overline{IRQ}$ pin and the SQW pin when each is in the high impedance state.
5. The $\overline{IRQ}$ pin is open drain.
6. Measured with a load as shown in Figure 4.

**OUTPUT LOAD** Figure 4

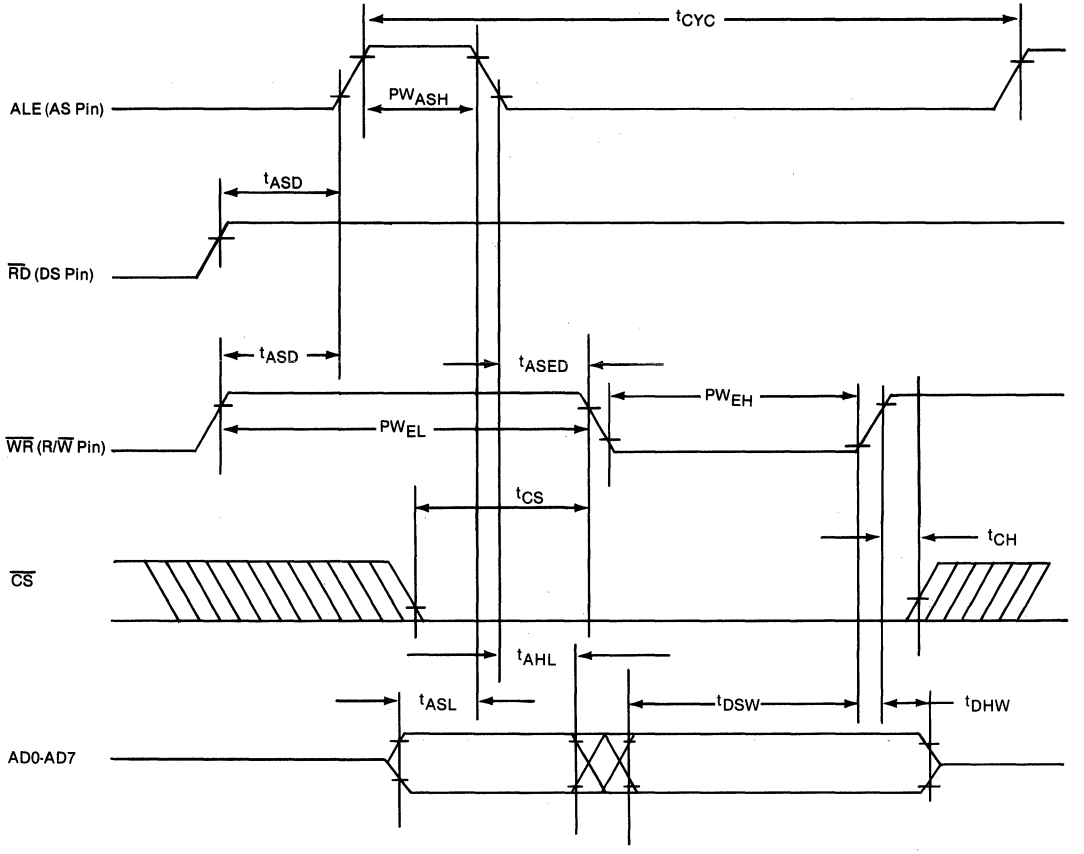


## DS1287 BUS TIMING FOR MOTOROLA INTERFACE



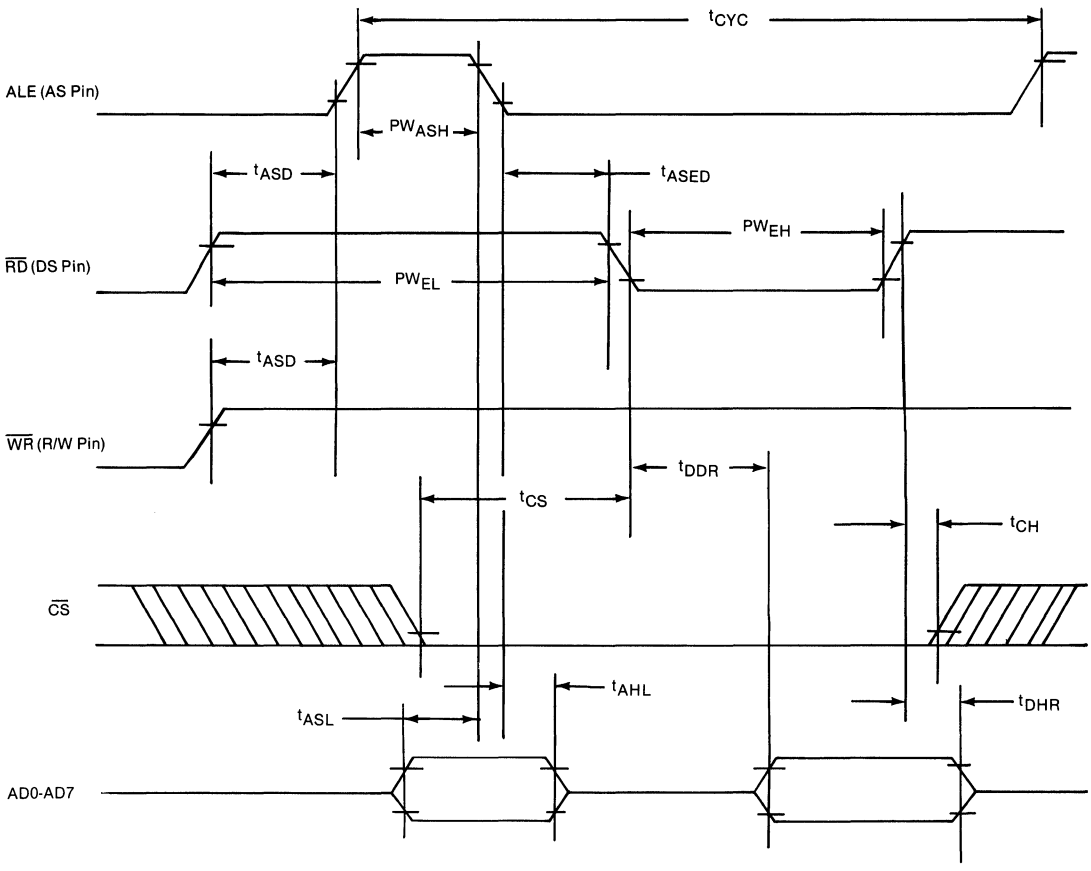

**NOTE:** Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

## DS1287 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



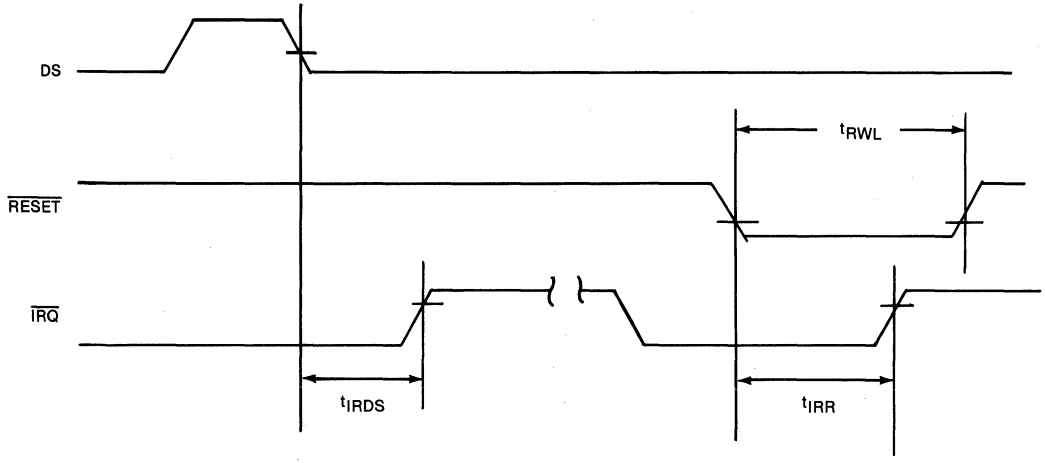

**NOTE:** Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

## DS1287 BUS TIMING FOR INTEL INTERFACE READ CYCLE



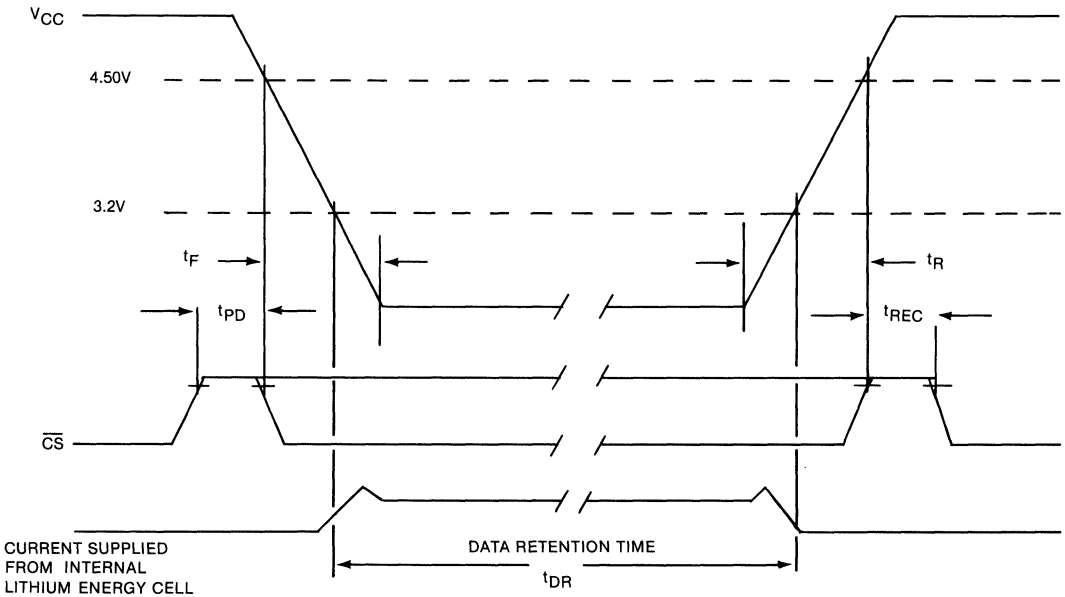

**NOTE:** Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

## DS1287 IRQ RELEASE DELAY TIMING




**NOTE:** Input Levels = 0.8 volts and 2.0 volts.
Output Levels = 0.4 volts and 2.4 volts.

## POWER-DOWN/POWER-UP CONDITION




7

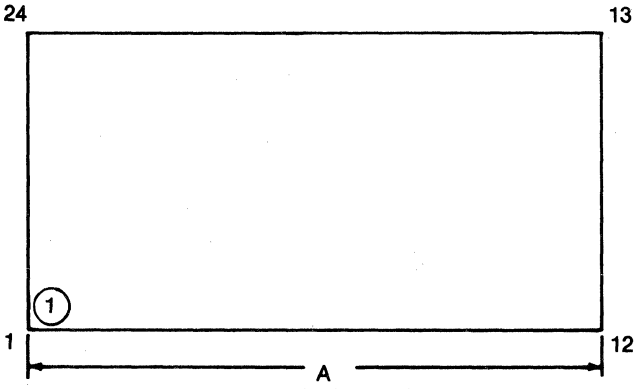
## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | us | |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 300 | | us | |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 100 | | us | |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power Up | 20 | 200 | ms | |

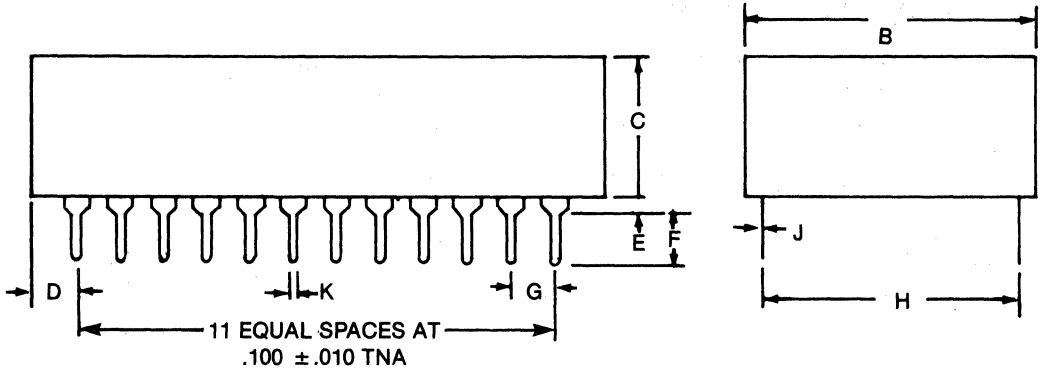
($t_A = 25\,°C$)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention | 10 | | years | |

**NOTE:**
The real time clock will keep time to an accuracy of ± 1 minute per month during data retention time for the period of $t_{DR}$.




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.320 | 1.335 |
| B | .685 | .700 |
| C | .345 | .360 |
| D | .100 | .120 |
| E | .015 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .600 | .650 |
| J | .008 | .012 |
| K | .015 | .021 |

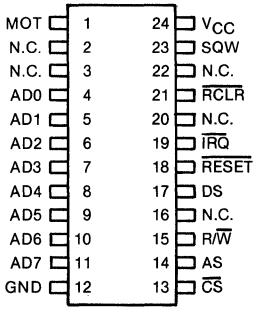



NOTE: Pins 2, 3, 16, 20, 21 and 22 are missing by design.

## FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month and year with leap year compensation
- Binary or BCD representation of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 *us* to 500 ms
  - End of clock update cycle

## PIN CONNECTIONS




## PIN NAMES

| | | |
|---|---|---|
| AD0 - AD7 | - | Multiplexed Address/Data Bus |
| N.C. | - | No Connection |
| MOT | - | Bus Type Selection |
| $\overline{CS}$ | - | Chip Select |
| AS | - | Address Strobe |
| R/$\overline{W}$ | - | Read/Write Input |
| DS | - | Data Strobe |
| $\overline{RESET}$ | - | Reset Input |
| $\overline{IRQ}$ | - | Interrupt Request Output |
| SQW | - | Square Wave Output |
| $V_{CC}$ | - | +5 Volt Supply |
| GND | - | Ground |
| $\overline{RCLR}$ | - | RAM Clear |

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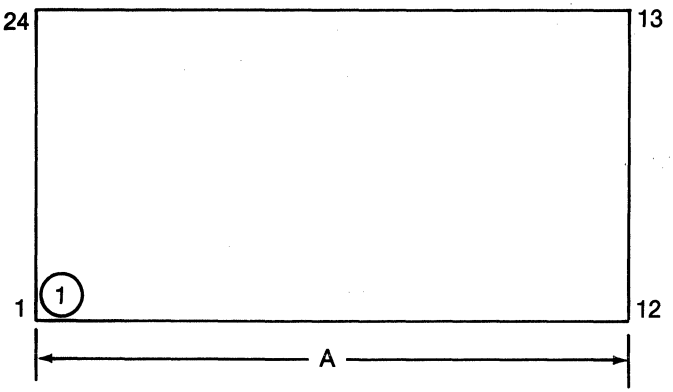
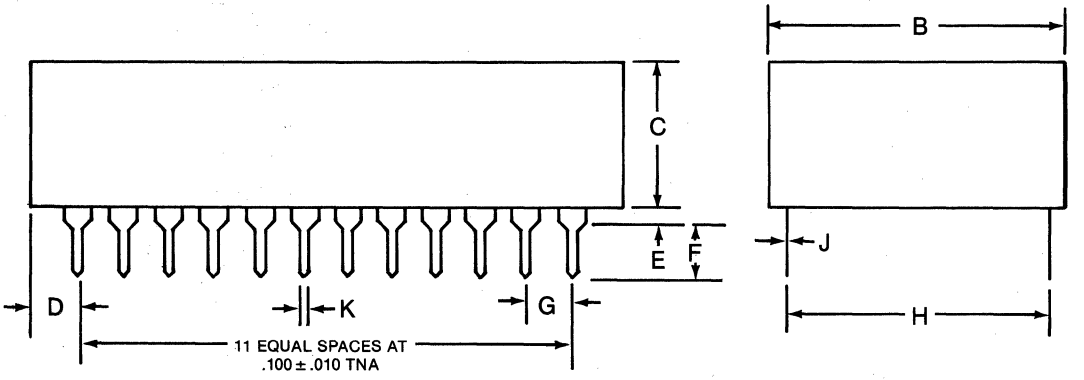
**NOTE**—The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not affect the RAM associated with the Real Time Clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (−0.3 to 0.8 volts) during battery back-up mode when $V_{CC}$ is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. All other operation, description and specification is identical to the DS1287.




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.320 | 1.335 |
| B | .685 | .700 |
| C | .345 | .360 |
| D | .100 | .120 |
| E | .015 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .600 | .650 |
| J | .008 | .012 |
| K | .015 | .021 |




NOTE: Pins 2, 3, 16, 20 and 22 are missing by design.

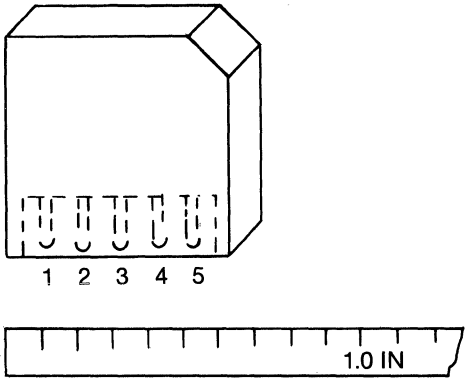
# User Insertable Memory

# Dallas Semiconductor
## *Electronic Tag* — *DS1201*

### FEATURES

- User insertable
- Nonvolatile—greater than 10 years of data retention
- 1024 bits of read/write memory
- Miniature and transportable
- Durable and rugged
- Impervious to handling
- 4 million bits/second data rate
- Single byte or multiple byte data transfer capability
- No restrictions on the number of write cycles
- Low power CMOS circuitry
- Applications include software authorization, computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work record

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| Pin 1 — $V_{CC}$ | +5 VOLTS |
| Pin 2 — $\overline{RST}$ | $\overline{RESET}$ |
| Pin 3 — DQ | DATA INPUT/OUTPUT |
| Pin 4 — CLK | CLOCK |
| Pin 5 — GND | GROUND |

### DESCRIPTION

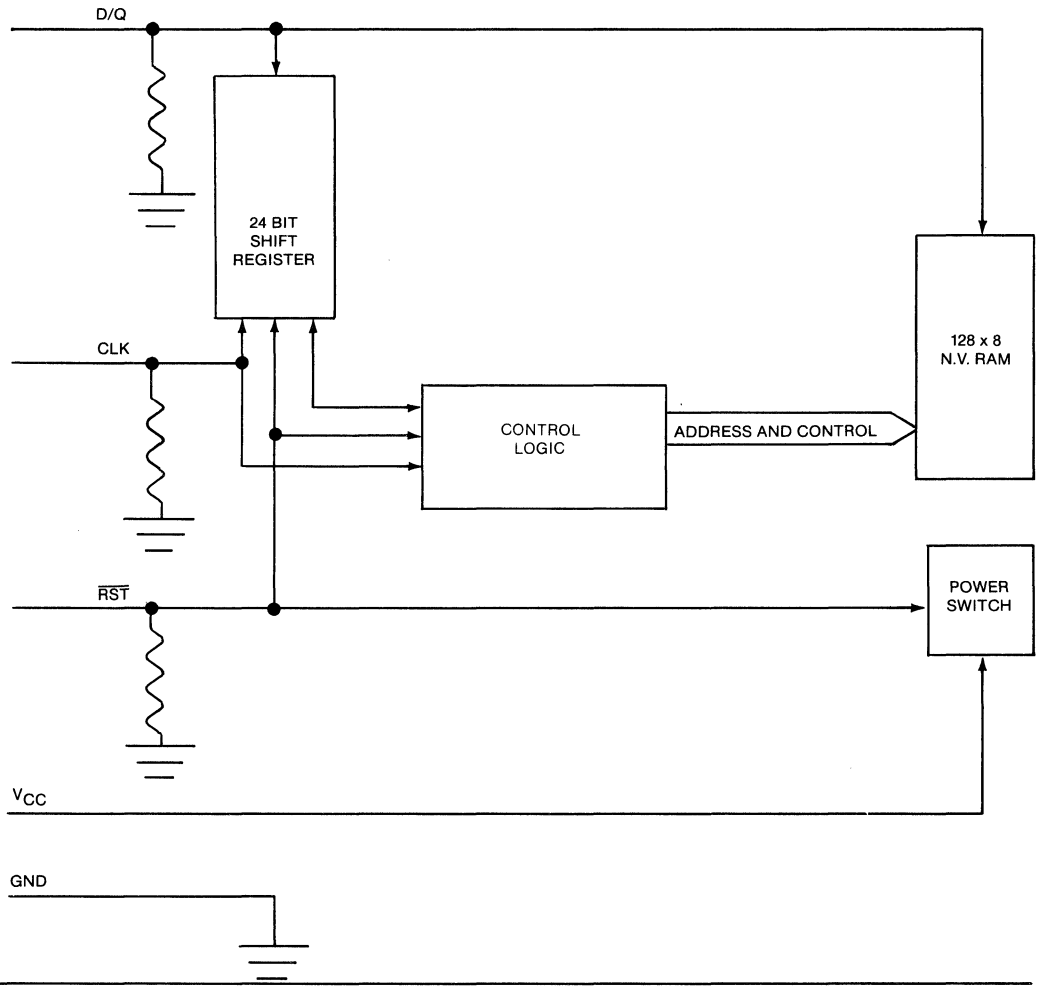
The DS1201 Electronic Tag is a miniature nonvolatile, read/write memory system which can randomly access individual 8-bit strings (bytes) or sequentialy access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{RESET}$, and DATA INPUT/OUTPUT. Low pin count and a guided entry for a mating receptacle overcomes mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user.

## OPERATION

The block diagram (Figure 1) of the electronic tag illustrates the main elements of the device; namely, shift register, control logic, nonvolatile RAM, and power switch. To initiate a memory cycle $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the shift register providing both address and command information. Each bit is serial input on the rising edge of the CLOCK input. Seven address bits specify one of the 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 CLOCKs which load the shift register, additional CLOCKs will output data for a read, or input data for a write. The number of CLOCK pulses equals 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

The tag can be used as a four-pin or five-pin device, depending on the application. For hardwired aplications, active power is supplied by the $V_{CC}$ pin. Alternatively, for user insertable applications, power can be supplied by the $\overline{\text{RESET}}$ pin.

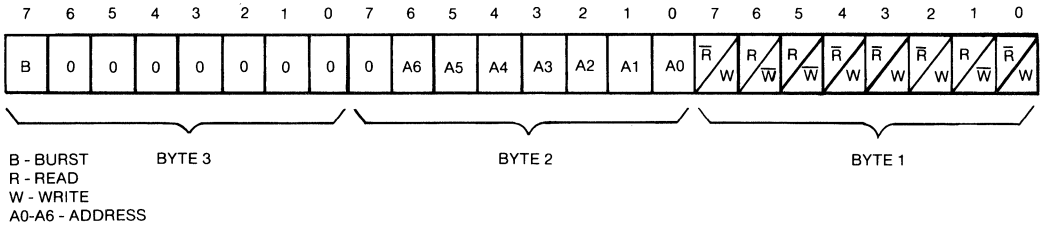
**ELECTRONIC TAG BLOCK DIAGRAM** Figure 1



## ADDRESS/COMMAND

Each memory transfer consists of a three-byte address/command input called the address/command. The address/command is shown in Figure 2. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address/command fails to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the tag are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address inputs A0 in bit 0 through A6 in bit 6. Bit 7 of the second byte of the address/command word must be set to logical 0. This bit is reserved for future higher density versions of the tag. If bit 7 does not equal logical 0, the cycle is aborted and all future inputs to the tag are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The third byte of the address/command is also set aside for future expansion. Bits 0 through 6 must be set to logical 0 or the cycle will be aborted and all future inputs are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. Bit 7 of byte three of the address/command is used along with address bits A0 through A6 to define burst mode. When A0 through A6 equals logical 0 and bit 7 of byte three of the address/command equals logical 1, the tag will enter the burst mode after the address/command sequence is complete.

FIGURE 2




## BURST MODE

Burst mode is specified for the electronic tag when all address bits (A0-A6) of the address/command are set to logical 0 and bit 7 of byte three to logical 1. The burst mode causes 128 consecutive bytes to be read or written. Burst mode terminates when the $\overline{\text{RESET}}$ input is driven low.

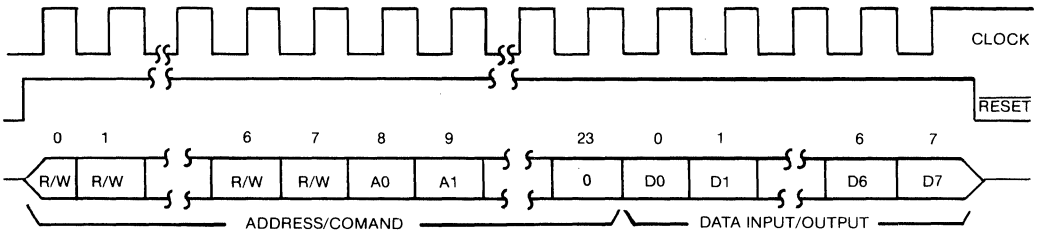
## RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{\text{RESET}}$ input high. The $\overline{\text{RESET}}$ input serves three functions. First, $\overline{\text{RESET}}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{\text{RESET}}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{\text{RESET}}$ of 2 mA @ 3.8 volts is required. However, if the $V_{CC}$ pin is connected to a 5 volt source within nominal limits, then $\overline{\text{RESET}}$ pin is not used as a source of power and input levels revert to normal $V_{IH}$ and $V_{IL}$ inputs with a drive current requirement of 500 $u$A. Finally, the $\overline{\text{RESET}}$ signal provides a method of terminating either single byte or multiple byte data transfers. A CLOCK cycle is a sequence of falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of CLOCK cycle. Address/command bits and data bits are input on the rising edge of the CLOCK and data bits are output on the falling edge of the CLOCK. All data transfer terminates if the $\overline{\text{RESET}}$ input is low and D/Q pin goes to a high impedance state. When data transfer to the tag is terminated using reset, the transition of $\overline{\text{RESET}}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 3.

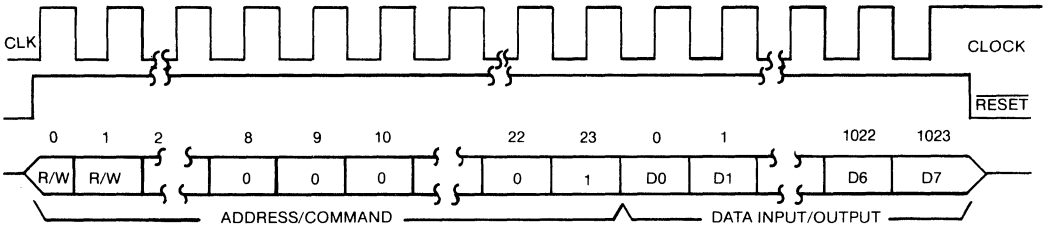
## DATA TRANSFER

FIGURE 3

**SINGLE BYTE TRANSFER**




**BURST MODE TRANSFER**




NOTES
1.) DATA INPUT SAMPLED ON RISING EDGE OF CLOCK
2.) DATA OUTPUT CHANGES ON FALLING EDGE OF CLOCK

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### DATA INPUT

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next 8 CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

### DATA OUTPUT

Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for the data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

### TAG CONNECTIONS

The tag is designed to be plugged into a standard 5-pin, 0.1-inch-center SIP receptacle. A key is provided to prevent the tag from being plugged in backwards and to aid in alignment of the receptacle. For portable applications, contact to the tag pins can be determined to insure connection integrity before data transfer begins. CLOCK, $\overline{\text{RESET}}$, and DATA INPUT/OUTPUT all have internal 20K Ohm pull down resistors to ground which can be sensed by a reading device.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on Any Pin Relative to Ground −1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | | V | 1,2,10 |
| Logic 0 | $V_{IL}$ | -0.3 | | 0.8 | V | 1 |
| $\overline{\text{RESET}}$ Logic 1 | $V_{IHE}$ | 3.8 | | | V | 1,7,11 |
| Supply | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | | | +500 | μA | 5 |
| Output Leakage | $I_{LO}$ | | | +500 | μA | 5 |
| Output Current @ 2.4V | $I_{OH}$ | -1 | | | mA | |
| Output Current @ 0.4V | $I_{OL}$ | | | +2 | mA | |
| $\overline{\text{RST}}$ Input RESISTANCE | $Z_{RST}$ | 10 | | 40 | KΩ | 1 |
| D/Q Input RESISTANCE | $Z_{DQ}$ | 10 | | 40 | KΩ | 1 |
| CLK Input RESISTANCE | $Z_{CLK}$ | 10 | | 40 | KΩ | 1 |
| Active Current | $I_{CC1}$ | | | 6 | mA | 8 |
| Standby Current | $I_{CC2}$ | | | 1 | mA | 8 |
| $\overline{\text{RST}}$ Current | $I_{RST}$ | | | | mA | 7,8,13 |

**CAPACITANCE** ($t_A$ = 25°C)

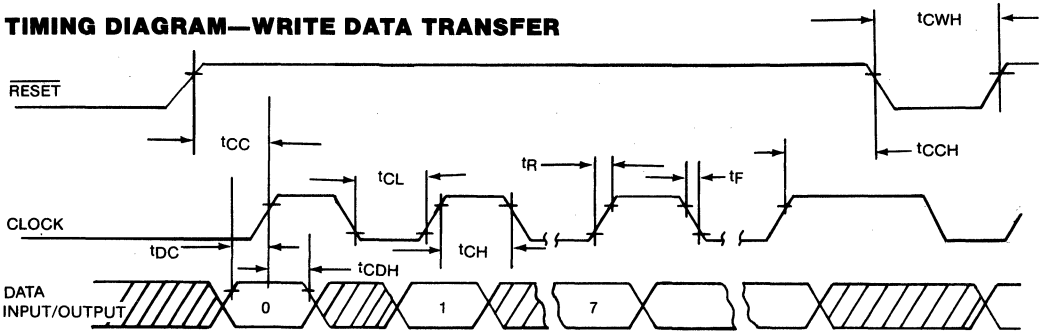
| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = +5V ± 10%)

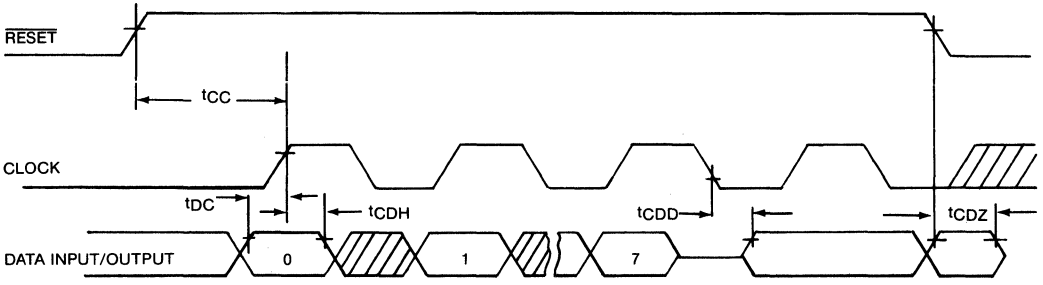
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Data To CLK Setup | $t_{DC}$ | 35 | | | ns | 3,9 |
| Data To CLK Hold | $t_{CDH}$ | 40 | | | ns | 3,9 |
| Data To CLK Delay | $t_{CDD}$ | | | 125 | ns | 3,4,6,9 |
| CLK Low Time | $t_{CL}$ | 125 | | | ns | 3,9 |
| CLK High Time | $t_{CH}$ | 125 | | | ns | 3,9 |
| CLK Frequency | $f_{CLK}$ | D.C. | | 4.0 | MHZ | 3,9 |
| CLK Rise & Fall | $t_R$,$t_F$ | | | 500 | ns | 9 |
| $\overline{RST}$ To CLK Set Up | $t_{CC}$ | 1 | | | $\mu$s | 3, 9 |
| CLK To $\overline{RST}$ Hold | $t_{CCH}$ | 40 | | | ns | 3,9 |
| $\overline{RST}$ Inactive Time | $t_{CWH}$ | 125 | | | ns | 3,9,14 |
| $\overline{RST}$ To I/O High Z | $t_{CDZ}$ | | | 50 | ns | 3,9 |

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Expected Data Retention Time | $t_{DR}$ | 10 | | | years | 12 |

## TIMING DIAGRAM—WRITE DATA TRANSFER



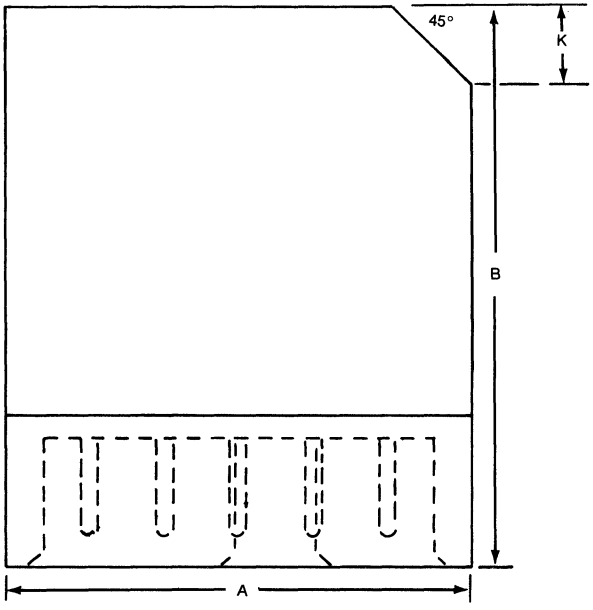

## TIMING DIAGRAM—READ DATA TRANSFER



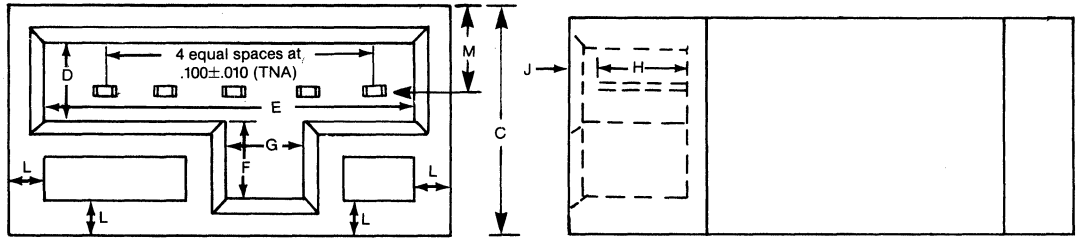

**NOTES**

1. All voltages and resistances are referenced to GND.
2. Input levels apply to CLK, D/Q, and $\overline{RST}$ while $V_{CC}$ is within nominal limits. When $V_{CC}$ is not connected to the tag, then the $\overline{RST}$ input reverts to $V_{IHE}$.
3. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8V$ and 10 ns maximum rise and fall time.
4. Measured at $V_{OH} = 2.4$ volts and $V_{OL} = 0.4$ volts.
5. For CLK, D/Q, $\overline{RST}$, and $V_{CC}$ at 5 volts.
6. Load capacitance = 50 pF.
7. Applies to $\overline{RST}$ when $V_{CC} < 3.8$ V.
8. Measured with outputs open.
9. Measured at $V_{IH}$ of $\overline{RST} \geq 3.8V$ when $\overline{RST}$ supplies power.
10. Logic 1 maximum is $V_{CC} + 0.3$ volts if the $V_{CC}$ pin supplies power and $\overline{RST} + 0.3$ volts if the $\overline{RST}$ pin supplies power.
11. $\overline{RST}$ logic 1 maximum is $V_{CC} + 0.3$ volts if the $V_{CC}$ pin supplies power and 5.5 volts maximum if $\overline{RST}$ supplies power.
12. Each DS1201 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.
13. Average A.C. $\overline{RST}$ current can be determined using the following formula:
    $I_{TOTAL} = 2 + I_{LOAD\ D.C.} + (4 \times 10^{-3})(C_L + 140) f$
    $I_{TOTAL}$ and $I_{LOAD}$ are in mA; $C_L$ is in pF; f is in MHZ.
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHZ gives an $I_{TOTAL}$ current of 5 mA.
14. When $\overline{RST}$ is supplying power $t_{CWH}$ must be increased to 100 ms.

# *Electronic Tag*
# *DS1201*




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .610 | .625 |
| B | .745 | .755 |
| C | .310 | .320 |
| D | .100 | .110 |
| E | .515 | .525 |
| F | .100 | .110 |
| G | .100 | .110 |
| H | .110 | .130 |
| J | .030 | .050 |
| K | .045 | .055 |
| L | .045 | .055 |
| M | .100 | .110 |



# Dallas Semiconductor
## *Nonvolatile Read/Write Cartridge* — *DS1217A*

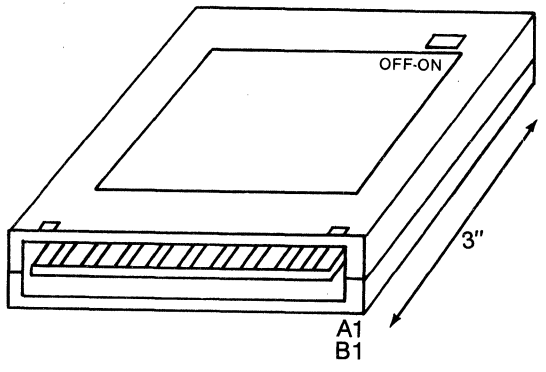
### FEATURES

- User insertable
- Capacity up to 32K x 8
- Standard Bytewide pinout facilitates connection to JEDEC 28 pin DIP via ribbon cable
- Data retention greater than 10 years
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0-70°C
- Unauthorized access can be prevented with optional security feature

### SIGNAL CONNECTIONS

| Name | Position | | Name |
|---|---|---|---|
| Ground | A1 | B1 | $\overline{\text{RESET}}$ |
| +5 Volts | A2 | B2 | Address 14 |
| $\overline{\text{Write Enable}}$ | A3 | B3 | Address 12 |
| Address 13 | A4 | B4 | Address 7 |
| Address 8 | A5 | B5 | Address 6 |
| Address 9 | A6 | B6 | Address 5 |
| Address 11 | A7 | B7 | Address 4 |
| $\overline{\text{Output Enable}}$ | A8 | B8 | Address 3 |
| Address 10 | A9 | B9 | Address 2 |
| $\overline{\text{Cartridge Enable}}$ | A10 | B10 | Address 1 |
| Data I/O 7 | A11 | B11 | Address 0 |
| Data I/O 6 | A12 | B12 | Data (DQ0) |
| Data I/O 5 | A13 | B13 | Data I/O 1 |
| Data I/O 4 | A14 | B14 | Data I/O 2 |
| Data I/O 3 | A15 | B15 | Ground |

### PACKAGE



## DESCRIPTION

The DS1217A is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge is available in density ranges from 2K x 8 to 32K x 8 in 8K-byte increments. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a 28-conductor ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28-pin Bytewide memory sites.

The DS1217A cartridge has a lifetime energy source to retain data and circuitry needed to automatically protect memory content. Reading and writing the memory locations is the same as using conventional static RAM. If the user wants to convert from read/write memory to read-only memory, a manual switch is provided to unconditionally protect memory content.

## READ MODE

The DS1217A is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data I/O pins within $t_{ACC}$ (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access. Read cycles can only occur when $V_{CC}$ is greater than 4.5 volts. When $V_{CC}$ is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

## WRITE MODE

The DS1217A is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge. Write cycles can only occur when $V_{CC}$ is greater than 4.5 volts. When $V_{CC}$ is less than 4.5 volts, the memory is write protected.

## DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for $V_{CC}$ greater than 4.5 volts and guarantees write protection for $V_{CC}$ less than 4.5 volts. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The DS1217A constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM. To retain data during power up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects the external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts.

The DS1217A checks battery status to warn of potential data loss. Each time that $V_{CC}$ power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge provides battery redundancy. The DS1217A provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

**REMOTE CONNECTION VIA A RIBBON CABLE**

Existing systems which contain 28-pin Bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin ribbon cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push out may occur as the distance between the cartridge and driving circuitry is increased.

**CARTRIDGE NUMBERING** Table 1

| PART NO. | DENSITY | UNUSED ADDRESS INPUTS |
|---|---|---|
| DS1217A/16K-25 | 2K × 8 | *ADDRESS 11, 12, 13, 14 |
| DS1217A/64K-25 | 8K × 8 | *ADDRESS 13, 14 |
| DS1217A/128K-25 | 16K × 8 | *ADDRESS 14 |
| DS1217A/192K-25 | 24K × 8 | |
| DS1217A/256K-25 | 32K × 8 | |

*Unused address inputs must be held low ($V_{IL}$).

**ABSOLUTE MAXIMUM RATINGS***

Voltage on Connection Relative to Ground −0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V |
| Input Low Voltage | $V_{IL}$ | −0.3 | | +0.8 | V |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}=5V\pm10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −60 | | +60 | uA |
| I/O Leakage Current | $I_{LO}$ | −10 | | +10 | uA |
| Output Current @2.4V | $I_{OH}$ | −1.0 | −2.0 | | mA |
| Output Current @ 0.4V | $I_{OL}$ | 2.0 | 3.0 | | mA |
| Standby Current $\overline{CE}=2.2V$ | $I_{CC}$ | | 5.0 | 10 | mA |
| Operating Current | $I_{CC}$ | | 35 | 75 | mA |

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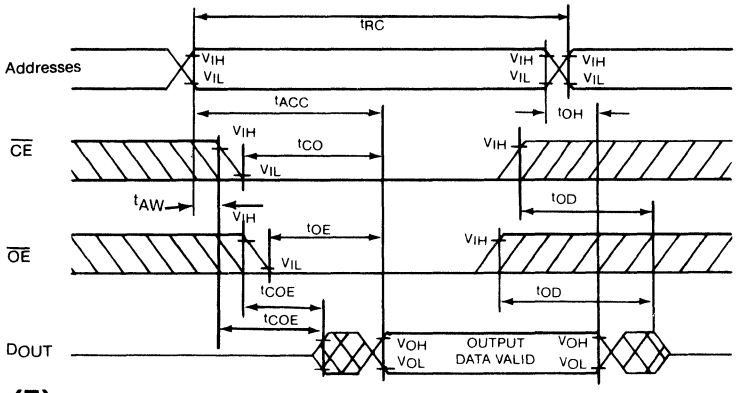
**CAPACITANCE** ($t_A = 25°C$)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 75 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | 75 | pF | |

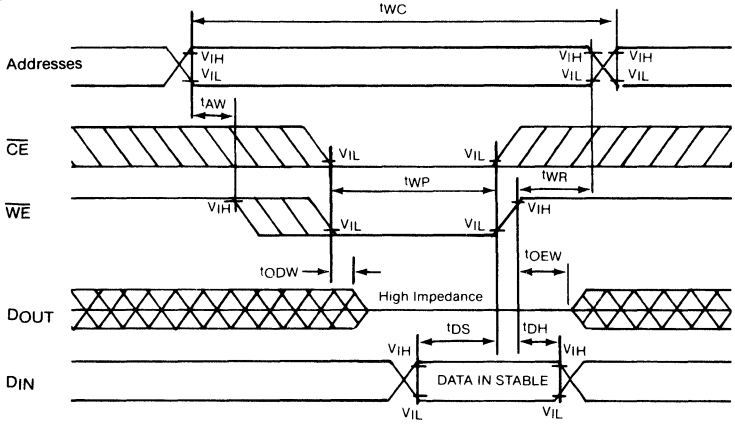
**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 250 | | | ns | |
| Access Time | $t_{ACC}$ | | | 250 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | | 125 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | | 250 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 10 | | | ns | |
| Output High Z From Deselection | $t_{OD}$ | | | 125 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | | ns | |
| Write Cycle Time | $t_{WC}$ | 250 | | | ns | |
| Write Pulse Width | $t_{WP}$ | 170 | | | ns | 3 |
| Address Set Up Time | $t_{AW}$ | 0 | | | ns | |
| Write Recovery Time | $t_{WR}$ | 20 | | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | | 100 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 10 | | | ns | |
| Data Set Up Time | $t_{DS}$ | 100 | | | ns | 4 |
| Data Hold Time From $\overline{WE}$ | $t_{DH}$ | 0 | | | ns | 4,5 |

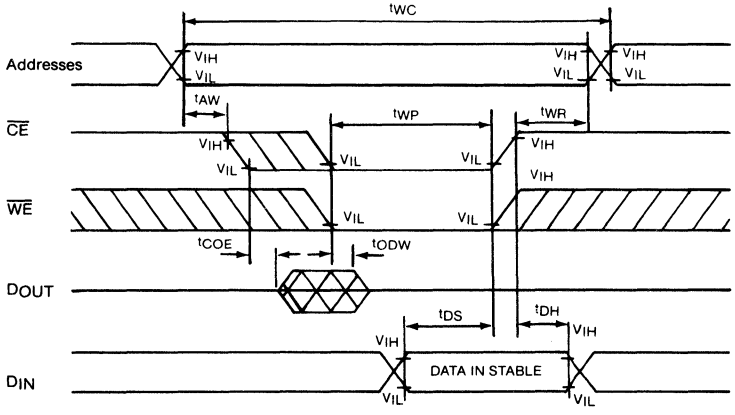
## READ CYCLE (1)




## WRITE CYCLE 1 (2), (6), (7)

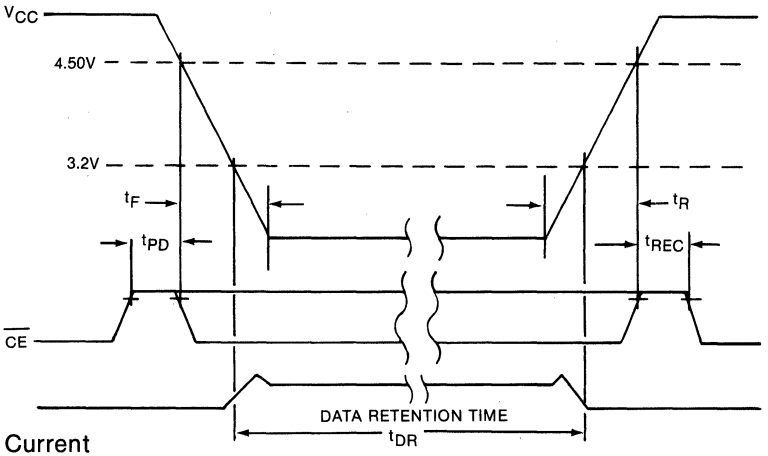



## WRITE CYCLE 2 (2), (8)




8

## POWER-DOWN/POWER-UP CONDITION




Leakage Current
$I_L$ supplied from
lithium cell

## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | $\mu$s | 10 |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 100 | | $\mu$s | |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | $\mu$s | |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power Up | 2 | 125 | ms | 10 |

($t_A$ = 25°C)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 10 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20ns$.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1217A is market with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

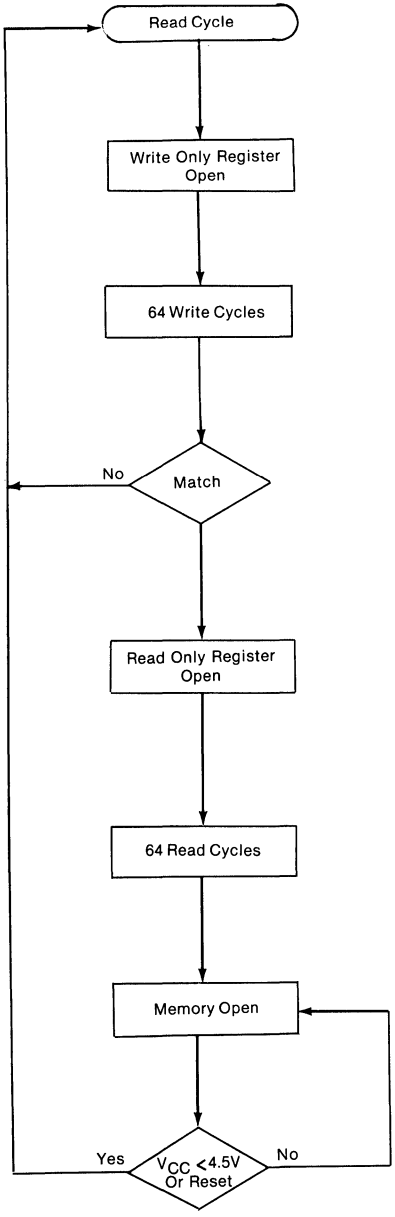
**D.C. Test Conditions**
Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

**A.C. Test Conditions**
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

## SECURITY OPTION

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 1). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1217A using the write enable signal ($\overline{WE}$), the chip enable signal ($\overline{CE}$), and the data input/output signal (DQ). The code is written to the cartridge without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1217A by Dallas Semiconductor at time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1217A and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1217A by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register may be used by software to determine if the cartridge will be permitted to be used with that particular system. After the 64th read cycle has been executed the cartridge is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If $V_{CC}$ falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.
**Note:** Contact Dallas Semiconductor sales office for code assignment.

**SECURITY SEQUENCE.**
Figure 1



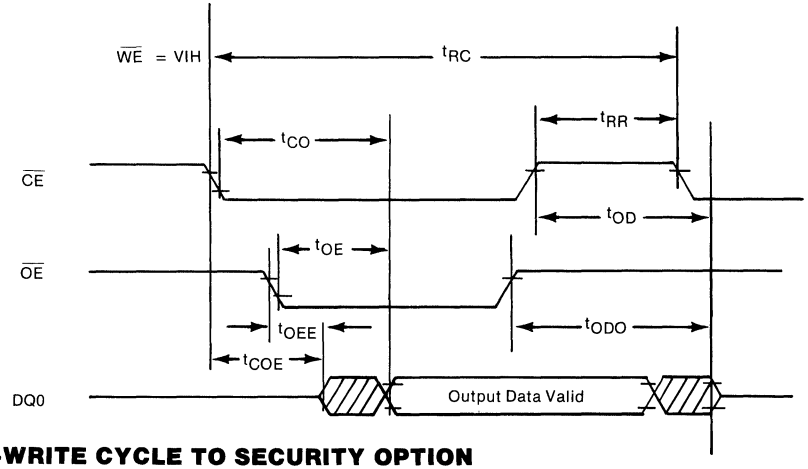
## SECURITY OPTION

### A.C. ELECTRICAL CHARACTERISTICS

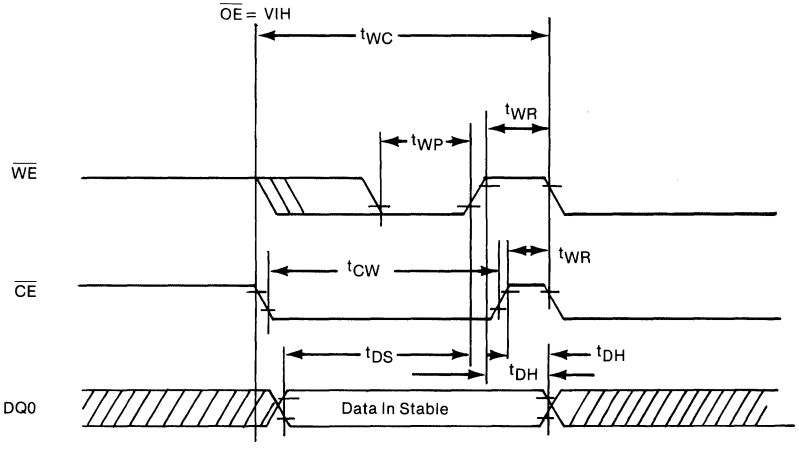
(0 °C - 70 °C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS |
|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 250 | | | ns |
| $\overline{CE}$ Access Time | $t_{CO}$ | | | 200 | ns |
| $\overline{OE}$ Access Time | $t_{OE}$ | | | 100 | ns |
| $\overline{CE}$ To Output Low Z | $t_{COE}$ | 10 | | | ns |
| $\overline{OE}$ To Output Low Z | $t_{OEE}$ | 10 | | | ns |
| $\overline{CE}$ To Output High Z | $t_{OD}$ | | | 100 | ns |
| $\overline{OE}$ To Output High Z | $t_{ODO}$ | | | 100 | ns |
| Read Recovery | $t_{RR}$ | 50 | | | ns |
| Write Cycle | $t_{WC}$ | 250 | | | ns |
| Write Pulse Width | $t_{WP}$ | 170 | | | ns |
| Write Recovery | $t_{WR}$ | 50 | | | ns |
| Data Set Up | $t_{DS}$ | 100 | | | ns |
| Data Hold Time | $t_{DH}$ | 0 | | | ns |
| $\overline{CE}$ Pulse Width | $t_{CW}$ | 170 | | | ns |
| Reset Pulse Width | $t_{RST}$ | 200 | | | ns |

## TIMING DIAGRAM—READ CYCLE TO SECURITY OPTION



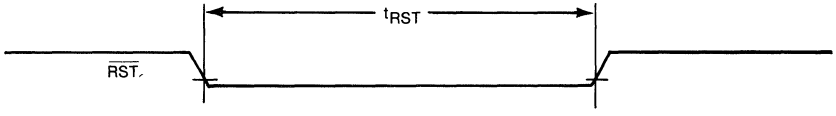

## TIMING DIAGRAM—WRITE CYCLE TO SECURITY OPTION



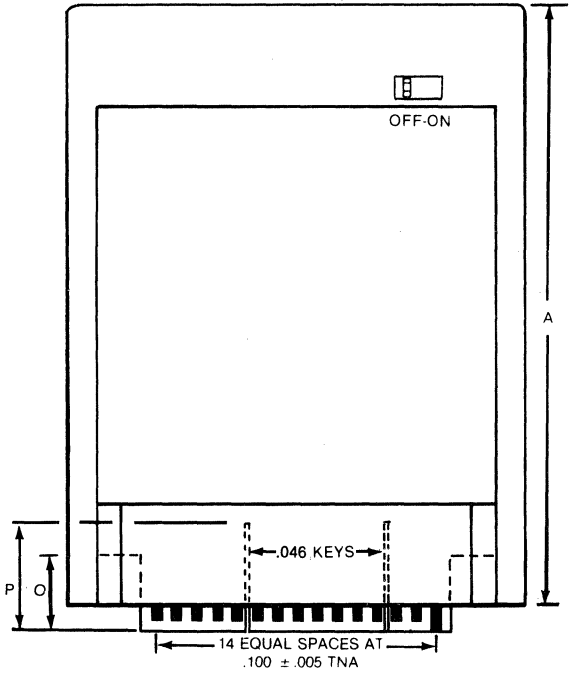

**NOTES:**

1. $t_{DH}$ and $t_{DS}$ are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
2. $t_{WR}$ is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.

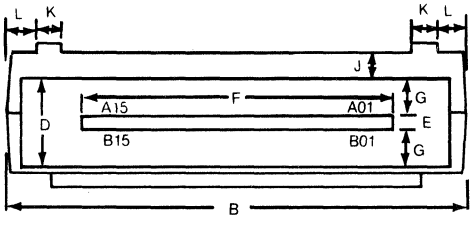
## TIMING DIAGRAM—RESET FOR SECURITY OPTION

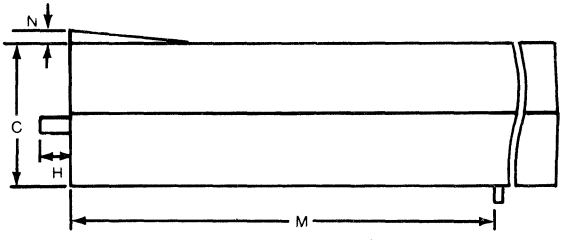


# *Nonvolatile Read/Write Cartridge*
# *DS1217A*




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 3.020 | 3.040 |
| B | 2.280 | 2.300 |
| C | .590 | .620 |
| D | .440 | .460 |
| E | .060 | .065 |
| F | 1.590 | 1.607 |
| G | .190 | .220 |
| H | .115 | .135 |
| J | .115 | .135 |
| K | .115 | .135 |
| L | .140 | .160 |
| M | 1.760 | 1.790 |
| N | .040 | .060 |
| O | .039 | .405 |
| P | .405 | .425 |



# Dallas Semiconductor
## *Nonvolatile Read/Write Cartridge*

PRELIMINARY

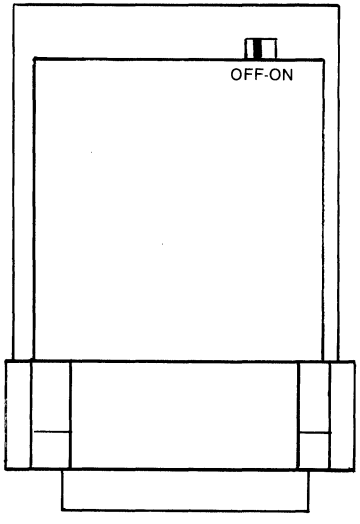
**DS1217I**

### FEATURES

- User insertable
- Data retention greater than 10 years
- Capacity up to 512K x 8
- Employs high-reliability, 32-position DIN connector
- Software controlled banks maintain 32K x 8 JEDEC 28-pin compatibility
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0-70°C

### SIGNAL CONNECTIONS

| | | | |
|---|---|---|---|
| No Connect | $A_0$ | $B_0$ | No Connect |
| Ground | $A_1$ | $B_1$ | No Connect |
| +5 Volts | $A_2$ | $B_2$ | Address 14 |
| $\overline{\text{Write Enable}}$ | $A_3$ | $B_3$ | Address 12 |
| Address 13 | $A_4$ | $B_4$ | Address 7 |
| Address 8 | $A_5$ | $B_5$ | Address 6 |
| Address 9 | $A_6$ | $B_6$ | Address 5 |
| Address 11 | $A_7$ | $B_7$ | Address 4 |
| $\overline{\text{Output Enable}}$ | $A_8$ | $B_8$ | Address 3 |
| Address 10 | $A_9$ | $B_9$ | Address 2 |
| $\overline{\text{Cartridge Enable}}$ | $A_{10}$ | $B_{10}$ | Address 1 |
| Data I/O 7 | $A_{11}$ | $B_{11}$ | Address 0 |
| Data I/O 6 | $A_{12}$ | $B_{12}$ | Data I/O 0 |
| Data I/O 5 | $A_{13}$ | $B_{13}$ | Data I/O 1 |
| Data I/O 4 | $A_{14}$ | $B_{14}$ | Data I/O 2 |
| Data I/O 3 | $A_{15}$ | $B_{15}$ | Ground |

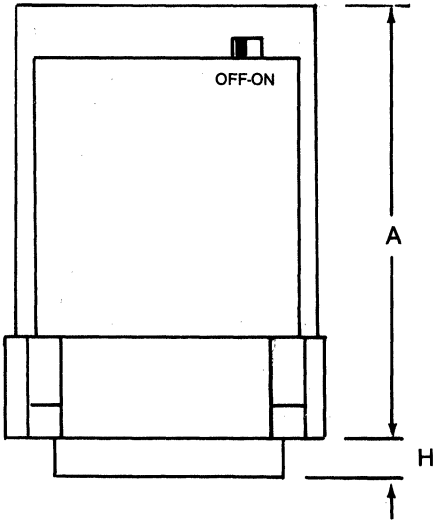



### DESCRIPTION

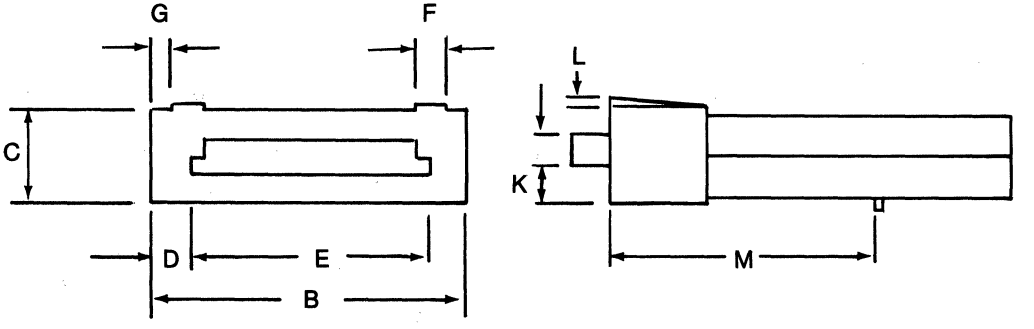
The DS1217I is a portable nonvolatile SRAM designed for industrial applications requiring a connection scheme which is protected from contamination in shop floor and other similar harsh environments. The high-reliability DIN connector design allows for multiple insertions and withdrawals even with power applied. A male 30-position vertical P.C. board mountable connector with first-make/last-break contacts is provided with each DS1217I memory cartridge. Right angle connectors are available as an option. The DS1217I may be purchased with densities ranging from 64K x 8 to 512K x 8.

See DS1217M for all electrical specifications.

# Nonvolatile Read/Write Cartridge
# DS1217I




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 3.290 | 3.310 |
| B | 2.400 | 2.415 |
| C | .710 | .730 |
| D | .315 | .345 |
| E | 1.735 | 1.755 |
| F | .220 | .240 |
| G | .125 | .145 |
| H | .200 | .220 |
| J | .230 | .240 |
| K | .220 | .240 |
| L | .030 | .040 |
| M | 2.035 | 2.065 |

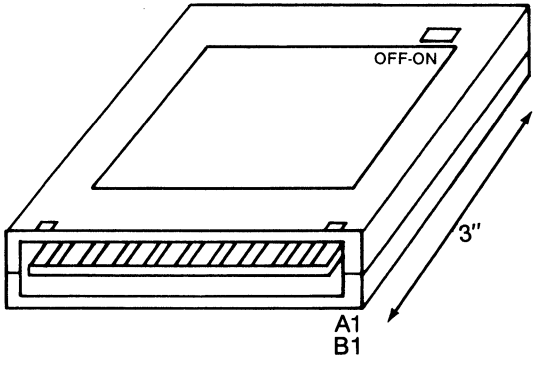


# Dallas Semiconductor
## *Nonvolatile Read/Write Cartridge* — *DS1217M*

### FEATURES

- User insertable
- Data retention greater than 10 years
- Capacity up to 512K × 8
- Standard Bytewide pinout facilitates connection to JEDEC 28 pin DIP via ribbon cable
- Software controlled banks maintain 32K × 8 JEDEC 28 pin compatability
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0-70°C

### PACKAGE




### SIGNAL CONNECTIONS

| NAME | POSITION | | NAME |
|---|---|---|---|
| Ground | A1 | B1 | No Connect |
| +5 Volts | A2 | B2 | Address 14 |
| $\overline{\text{Write Enable}}$ | A3 | B3 | Address 12 |
| Address 13 | A4 | B4 | Address 7 |
| Address 8 | A5 | B5 | Address 6 |
| Address 9 | A6 | B6 | Address 5 |
| Address 11 | A7 | B7 | Address 4 |
| $\overline{\text{Output Enable}}$ | A8 | B8 | Address 3 |
| Address 10 | A9 | B9 | Address 2 |
| $\overline{\text{Cartridge Enable}}$ | A10 | B10 | Address 1 |
| Data I/O 7 | A11 | B11 | Address 0 |
| Data I/O 6 | A12 | B12 | Data I/O 0 |
| Data I/O 5 | A13 | B13 | Data I/O 1 |
| Data I/O 4 | A14 | B14 | Data I/O 2 |
| Data I/O 3 | A15 | B15 | Ground |

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## DESCRIPTION

The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 64K x 8 to 512K x 8. The cartridge is accessed in continuous 32K byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required for connection to a host system. A standard 30 pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28 pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28 Pin bytewide memory sites.

## READ MODE

The DS1217M is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within $t_{ACC}$ (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access. Read cycles can only occur when $V_{CC}$ is greater than 4.5 volts. When $V_{CC}$ is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

## WRITE MODE

The DS1217M is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge. Write cycles can only occur when $V_{CC}$ is greater than 4.5 volts. When $V_{CC}$ is less than 4.5 volts, the memory is write protected.

## DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for $V_{CC}$ greater than 4.5 volts and guarantees write protection for $V_{CC}$ less than 4.5 volts. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The DS1217M constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects the external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts.

The DS1217M checks battery status to warn of potential data loss. Each time that $V_{CC}$ power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge provides battery redundancy. The DS1217M provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

**BANK SWITCHING**

Bank switching is accomplished via address lines A8, A9, A10 and A11. Initially, on power up all banks are deselected so that multiple cartridges can reside on a common bus. Bank switching requires that a predefined pattern of 64 bits is matched by sequencing 4 address inputs (A8 through A11) 16 times while ignoring all other address inputs. Prior to entering the 64 bit pattern which will set the bank switch, a read cycle of 1111 (address inputs A8 through A11) must be executed to guarantee that pattern entry starts with the first set of 4 bits. Each set of address inputs are entered into the DS1217M by executing read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 2. The last five cycles must match the exact bit pattern for addresses A9, A10 and A11. However, address line 8 defines which of the 16 banks that is to be enabled, or all banks deselected, as per Table 3.

Switching from one bank to another occurs as the last of the 16 read cycles is completed. A single bank is selected at any one time. A selected bank will remain active until a new bank is selected, all banks are deselected, or until power is lost. (See DS1222 BankSwitch data sheet for more detail.)

**REMOTE CONNECTION VIA A RIBBON CABLE**

Existing systems which contain 28 pin Bytewide sockets can be retrofitted using a 28 pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28 pin site after the memory is removed. Connection to the cartridge is accomplished via a 28 pin cable connected to a 30 contact card edge connector, AMP Part Number 499188-4. The 28 pin ribbon cable must be right-justified, such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push out may occur as the distance between the cartridge and the driving circuitry is increased.

**TABLE 1 — CARTRIDGE NUMBERING**

| PART NO. | DENSITY | NO. OF BANKS |
|---|---|---|
| DS1217M 1/2-25 | 64K x 8 | 2 |
| DS1217M 1-25 | 128K x 8 | 4 |
| DS1217M 2-25 | 256K x 8 | 8 |
| DS1217M 3-25 | 384K x 8 | 12 |
| DS1217M 4-25 | 512K x 8 | 16 |

**TABLE 2 — ADDRESS INPUT PATTERN**

| ADDRESS INPUTS | BIT SEQUENCE | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| $A_8$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | X | X | X | X | X |
| $A_9$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| $A_{10}$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| $A_{11}$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

X = See Table 3

**TABLE 3 — BANK SELECT TABLE**

| BANK SELECTED | $A_8$ BIT SEQUENCE | | | | |
|---|---|---|---|---|---|
| | 11 | 12 | 13 | 14 | 15 |
| BANKS OFF | 0 | X | X | X | X |
| BANK 0 | 1 | 0 | 0 | 0 | 0 |
| BANK 1 | 1 | 0 | 0 | 0 | 1 |
| BANK 2 | 1 | 0 | 0 | 1 | 0 |
| BANK 3 | 1 | 0 | 0 | 1 | 1 |
| BANK 4 | 1 | 0 | 1 | 0 | 0 |
| BANK 5 | 1 | 0 | 1 | 0 | 1 |
| BANK 6 | 1 | 0 | 1 | 1 | 0 |
| BANK 7 | 1 | 0 | 1 | 1 | 1 |
| BANK 8 | 1 | 1 | 0 | 0 | 0 |
| BANK 9 | 1 | 1 | 0 | 0 | 1 |
| BANK 10 | 1 | 1 | 0 | 1 | 0 |
| BANK 11 | 1 | 1 | 0 | 1 | 1 |
| BANK 12 | 1 | 1 | 1 | 0 | 0 |
| BANK 13 | 1 | 1 | 1 | 0 | 1 |
| BANK 14 | 1 | 1 | 1 | 1 | 0 |
| BANK 15 | 1 | 1 | 1 | 1 | 1 |

**ABSOLUTE MAXIMUM RATINGS***

Voltage on Connection Relative to Ground −0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V |
| Input Low Voltage | $V_{IL}$ | −0.3 | | +0.8 | V |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}=5V\pm10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −60 | | +60 | uA |
| I/O Leakage Current | $I_{LO}$ | −10 | | +10 | uA |
| Output Current @2.4V | $I_{OH}$ | −1.0 | −2.0 | | mA |
| Output Current @ 0.4V | $I_{OL}$ | 2.0 | 3.0 | | mA |
| Standby Current $\overline{CE}=2.2V$ | $I_{CC}$ | | 15 | 25 | mA |
| Operating Current | $I_{CC}$ | | 50 | 100 | mA |

**CAPACITANCE** ($t_A = 25°C$)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 100 | pF | |
| Input/Output Capacitance | $C_{OUT}$ | 100 | pF | |

**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 250 | | | ns | |
| Access Time | $t_{ACC}$ | | | 210 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | | 125 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | | 210 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 10 | | | ns | |
| Output High Z From Deselection | $t_{OD}$ | | | 125 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | | ns | |
| Read Recovery Time | $t_{RR}$ | 40 | | | ns | |
| Write Cycle Time | $t_{WC}$ | 250 | | | ns | |
| Write Pulse Width | $t_{WP}$ | 170 | | | ns | 3 |
| Address Set Up Time | $t_{AW}$ | 0 | | | ns | |
| Write Recovery Time | $t_{WR}$ | 20 | | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | | 100 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 10 | | | ns | |
| Data Set Up Time | $t_{DS}$ | 100 | | | ns | 4 |
| Data Hold Time From $\overline{WE}$ | $t_{DH}$ | 0 | | | ns | 4,5 |

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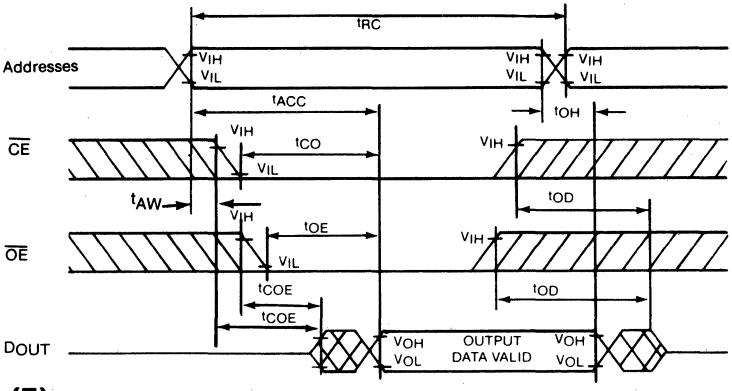
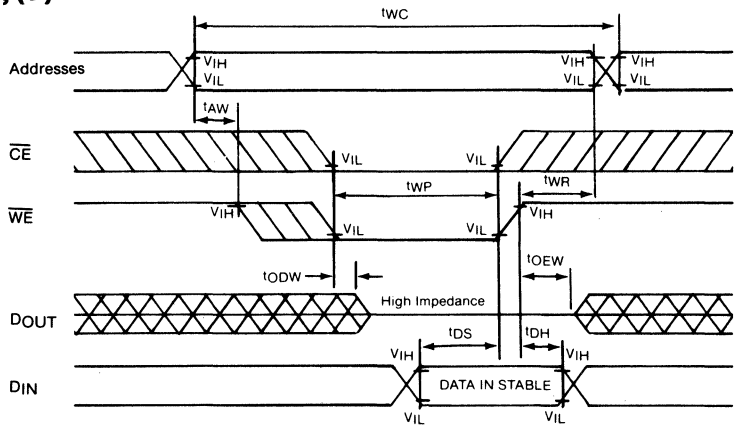
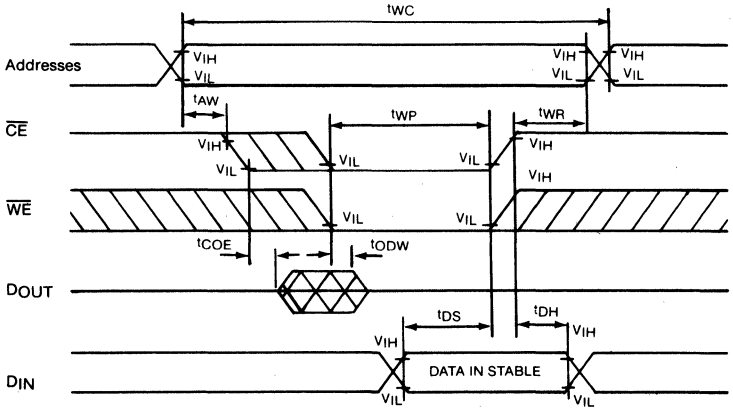
## READ CYCLE (1)



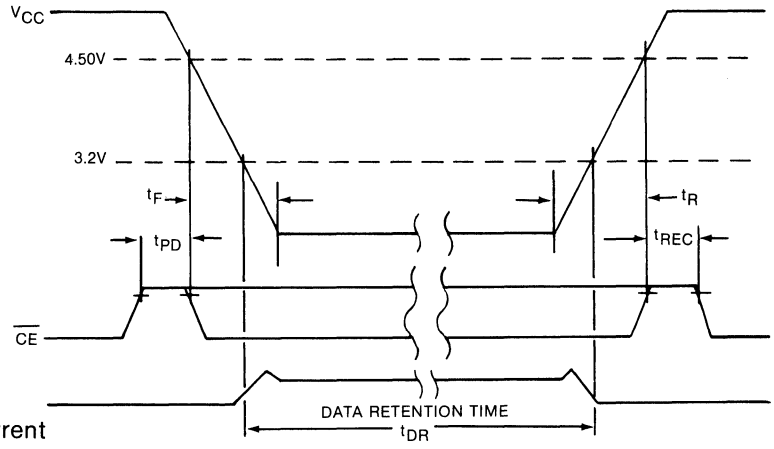

## WRITE CYCLE 1 (2), (6), (7)




## WRITE CYCLE 2 (2), (8)



## POWER-DOWN/POWER-UP CONDITION




Leakage Current
$I_L$ supplied from
lithium cell

## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | $\mu$s | 10 |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 100 | | $\mu$s | |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | $\mu$s | |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power Up | 2 | 125 | ms | 10 |

($t_A$ = 25°C)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 10 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

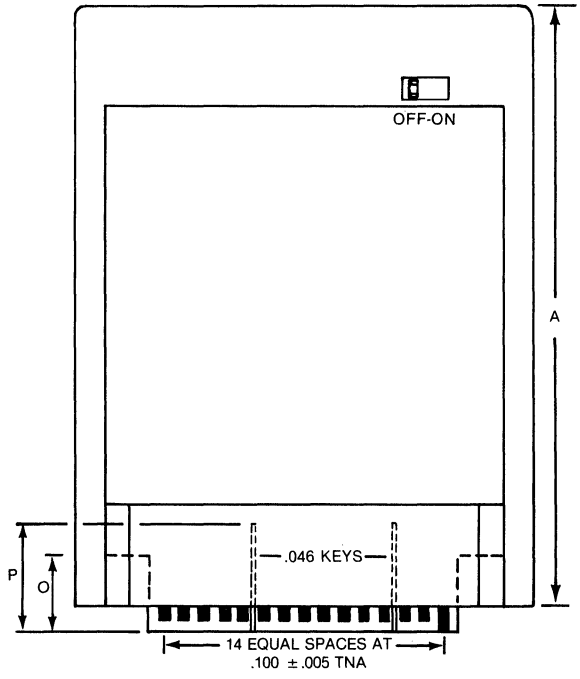
**NOTES:**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20ns$.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.
9. Each DS1217M is market with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

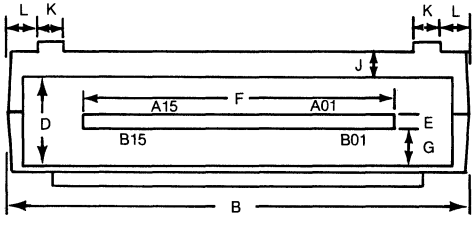
**D.C. Test Conditions**
Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

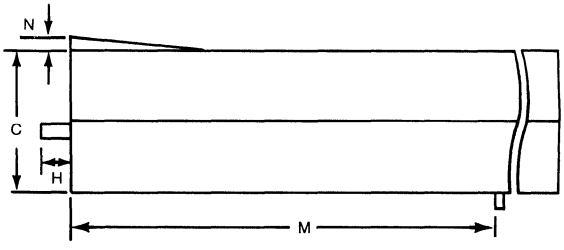
**A.C. Test Conditions**
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

# *Nonvolatile Read/Write Cartridge DS1217M*




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 3.020 | 3.040 |
| B | 2.280 | 2.300 |
| C | .600 | .630 |
| D | .440 | .460 |
| E | .060 | .065 |
| F | 1.590 | 1.607 |
| G | .220 | .250 |
| H | .115 | .135 |
| J | .115 | .135 |
| K | .115 | .135 |
| L | .140 | .160 |
| M | 1.760 | 1.790 |
| N | .040 | .060 |
| O | .039 | .405 |
| P | .405 | .425 |




8

# Dallas Semiconductor
## *KeyRing*

## *DS1250*

### FEATURES

- Low cost add-on fixture for Electronic Keys and Tags
- No hardware changes needed to retrofit existing systems
- Layman installation
- Normal system operation unaffected
- Key or Tag communication totally controlled by software
- Typical 50 K bits/s communication rate
- Up to 5 Keys and/or Tags resident at one time

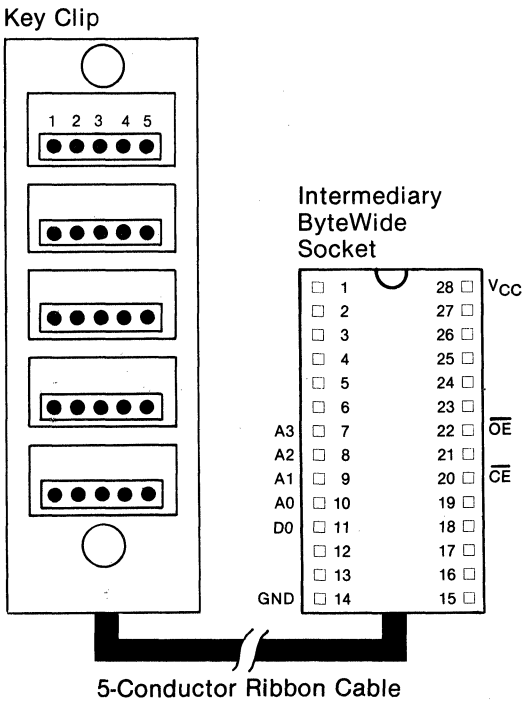
### PIN CONNECTIONS AND DEFINITIONS

Intermediary ByteWide Socket
Pins 7-10 - Address Inputs
Pin 11 - D0
Pin 20 - conditioned Chip Enable
Pin 22 - Output Enable
Pin 14 - Ground
Pin 28 - $V_{CC}$

All pins pass through except 20

Key Clip

Pin 1 - $V_{CC}$ +5 Volts
Pin 2 - $\overline{RST}$ - $\overline{RESET}$
Pin 3 - DQ - Data In/Out
Pin 4 - CLK - CLOCK
Pin 5 - GND - Ground



## DESCRIPTION

The DS1250 KeyRing adapts low pin count Electronic Keys (DS1204), TimeKeys (DS1207) or Tags (DS1201) to JEDEC ByteWide memory signals without affecting system operation. A simple, layman procedure is all that is needed to retrofit an existing system. Any 28 pin RAM, ROM, or EPROM can be removed, placed in the intermediary socket, and then reinstalled in the original location leaving the system intact. The emanating 5 conductor ribbon cable can be routed out of the system enclosure if desired and the clip can be attached where convenient with the adhesive provided. Up to 5 Keys and/or Tags can be inserted in the clip at the same time. The intermediary socket contains a CMOS integrated circuit which redirects information flow from the ByteWide memory to the inserted keys/tags. A special software generated address sequence causes the redirection to take place. Typical data transfer rates of 50 K bits/s are possible with an assembly language software driver.

## HARDWARE IMPLEMENTATION 28-PIN ROM SOCKET

Bytewide KeyRing application begins with a system board which contains a 28-pin socket with or without a ROM contained in the socket. In most system implementations and all PCs, there is at least one ROM which is used for boot sequences, basic I/O system implementation, EPROM storage, or some form of dedicated software monitor application.

Installation of the Bytewide KeyRing requires the removal of the existing 28-pin ROM and the insertion of the Bytewide KeyRing socket pins into the system board socket. After this is accomplished, the original ROM is reinserted into the socket at the top of the Bytewide KeyRing. Then the five-conductor ribbon cable which connects the clip to the Bytewide socket is routed to the outside of the computer cabinet. Finally the clip can be attached to a convenient place on the computer cabinet using the supplied adhesive.

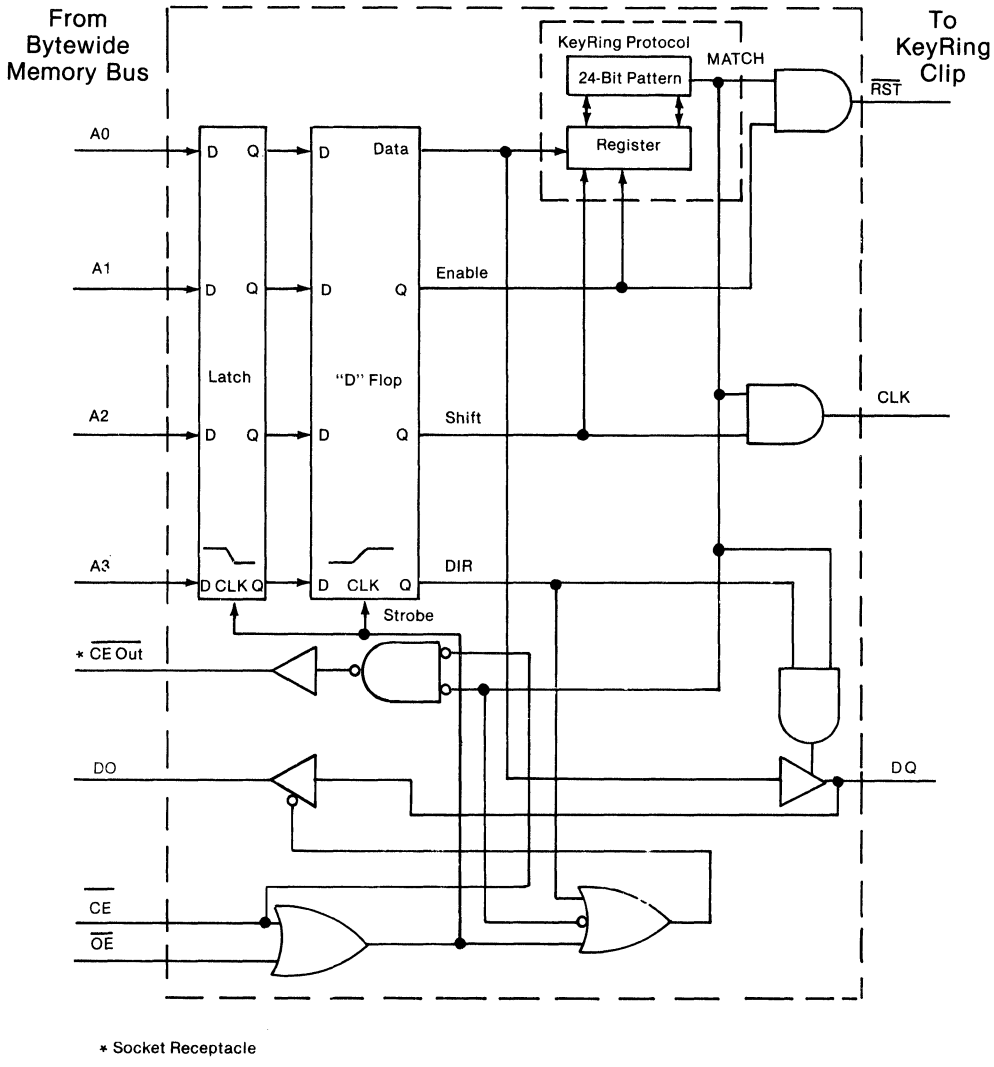
Under normal conditions, the system ROM will function as before, with address and data lines being transparently ported through the Bytewide KeyRing socket and presented to the system ROM as in the original configuration. As a result, existing non-Key-protected software will run on the system unaffected. However, if certain address lines are probed with specific patterns under software control, the KeyRing is activated and the system ROM becomes electrically disconnected from the system board. Instead, the address and data bus become electrically tied to the KeyRing bus. At this point, communication to the system board ROM socket is passed on transparently to any device(s) which are inserted into the KeyRing clip.

## KEYRING OPERATION

The main parts of the KeyRing are shown in the block diagram of Figure 1. Information presented on address inputs of the ROM are latched into the KeyRing on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}$ In and $\overline{OE}$ In. The $\overline{CE}$ input is connected to the memory bus $\overline{CE}$ and the $\overline{OE}$ input is connected to the memory bus $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 24-bit KeyRing protocol and to logic which will generate signals for Keys and Tags. The KeyRing protocol is derived from address inputs A0, A1 and A2. A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially the A1 input must be set high to enable communications. A1 must remain high during the pattern recognition sequence and subsequent communications with Keys after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and access is denied.

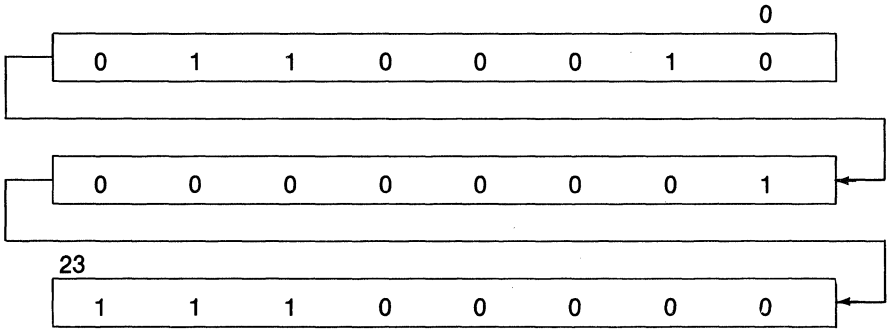
Data transfer through the KeyRing occurs by matching a 24-bit pattern, as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Therefore, data is input for comparison to the KeyRing protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles. The first memory cycle sets A2 low, establishing the shift clock low. The second memory cycle sets A2 high, causing the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the same level for both memory cycles. Address input A3 is used to control the direction of data going to and from Keys. This input is not used during pattern recognition of the KeyRing protocol. After the 24-bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for Keys. The match signal is also used to disable Chip Enable to the topside memory and enable a gate which allows Key DQ to drive D0 line to the memory bus. When $\overline{RST}$ is driven high, devices attached to the KeyRing become active. Subsequent shift signals derived from A2 will now be recognized as the Key clock. The data signal for the Key is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on Key DQ. When A3 is set low, devices attached to the KeyRing can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the Key DQ.

**KEYRING BLOCK DIAGRAM** Figure 1

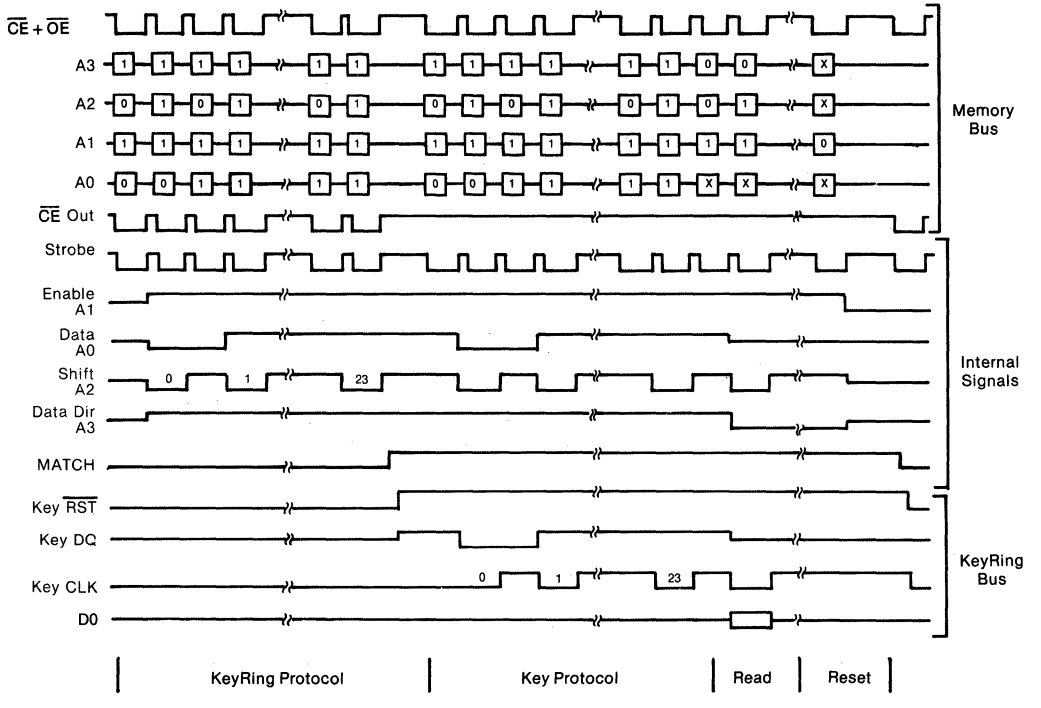



* Socket Receptacle

**KEYRING PROTOCOL** Figure 2




**KEYRING SIGNALS** Figure 3



## ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | $V_{CC}+0.3$ | V | 1 |
| Logic 0 Input | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| Supply | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |

## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}=5V\pm10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | −1 | | 1 | *u*A | |
| Output Leakage | $I_{LO}$ | | | 1 | *u*A | |
| Output Current @2.4V | $I_{OH}$ | −1 | | | mA | |
| Output Current @ .4V | $I_{OL}$ | +4 | | | mA | |
| $\overline{RST}$ Output Current @3.8V | $I_{OHR}$ | 16 | | | mA | |
| Supply Current | $I_{CC}$ | | | 6 | mA | 2 |

8

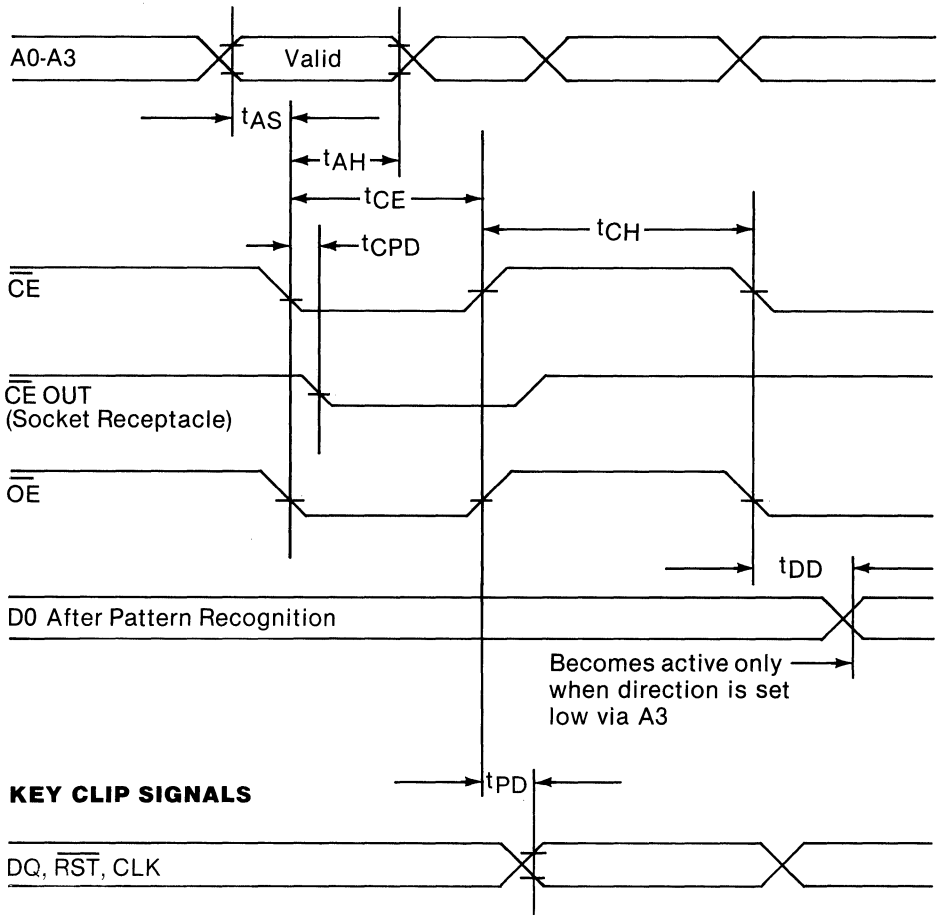
**CAPACITANCE** ($t_A = 25\,°C$)

| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output | $C_{I/O}$ | 5 | 10 | pF | |

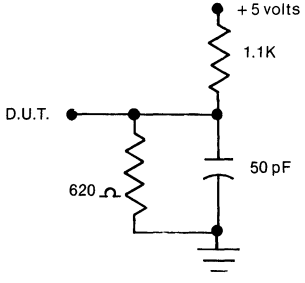
**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Address Set Up | $t_{AS}$ | 0 | | | ns | |
| Address Hold | $t_{AH}$ | 50 | | | ns | |
| $\overline{CE}$ Pulse Width | $t_{CE}$ | 60 | | | ns | |
| Key Signals Valid | $t_{PD}$ | | | 60 | ns | 3 |
| Key Data Out | $t_{DD}$ | 10 | | | ns | 3 |
| $\overline{CE}$ Inactive | $t_{CH}$ | 30 | | | ns | |
| $\overline{CE}$ Propagation Delay | $t_{CPD}$ | | | 10 | ns | |

**BYTEWIDE MEMORY BUS**




**OUTPUT LOAD** Figure 4




**NOTES:**

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Measured with a load as shown in Figure 4.

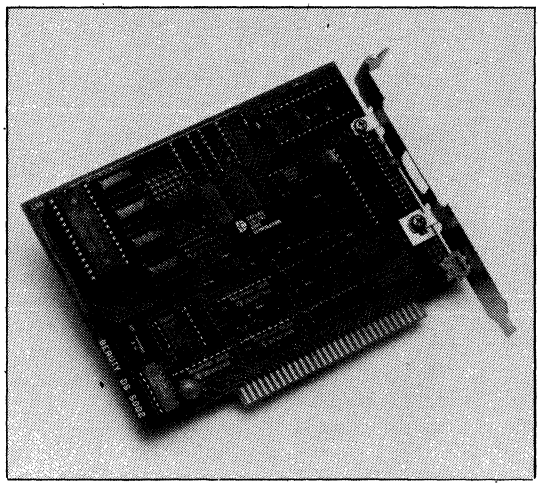
8

# Dallas Semiconductor
## *P.C. Port*

PRELIMINARY
**DS6010**

### FEATURES

- Half-size expansion card which interfaces the PC, XT and AT compatible computers with Dallas Semiconductor cartridges and cartridge clips
- Software included which supports the installation and controls operation
- Responds to all PC DOS commands
- Self-booting on power-up after installation
- Occupies only two 32K x 8 blocks of the PC memory map
- Provides the equivalent of a four-megabyte solid-state disk drive when used with the cartridge clip
- Contains a real-time clock for time stamping and dating of file transactions
- Software-controlled DIP switch simplifies installation
- High performance data transfer
- Low operating power
- Optional software protection and access control is available by using the DS1204U Electronic Key



### DESCRIPTION

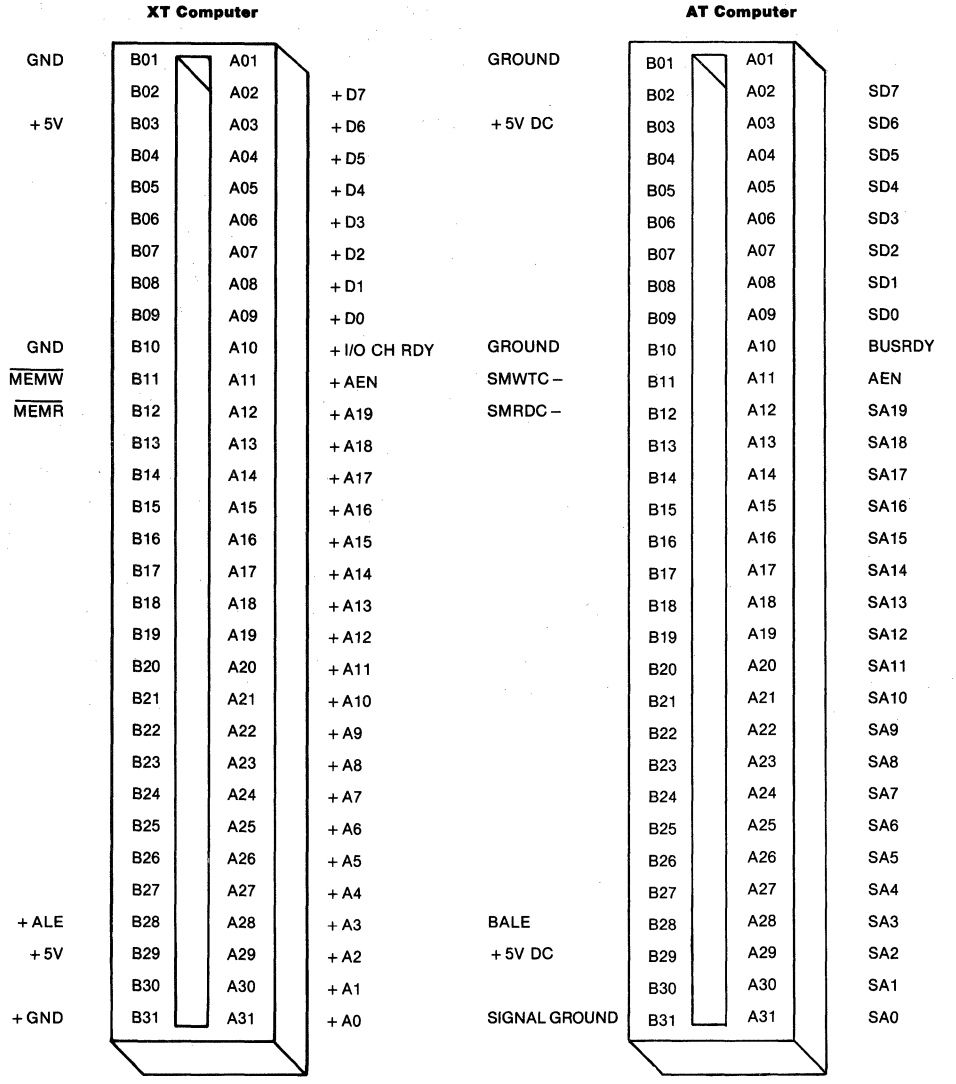
The DS6010 is a half-size expansion slot card which interfaces DS1217 cartridges and DS9020 Cartridge Clips to the IBM PC, XT, AT or compatible computers. Included is a software package which is used to both install and operate the expansion port. After user interaction between the software and the operator, Cartridges and Cartridge Clips will operate under DOS 3.0 commands as a disk drive. Up to eight Cartridges can be modularly added to a computer with each DS6010. This system addition allows compatible computers to be used in environments which are unsuitable for rotating mass memory. The PC port occupies only two 32K x 8 blocks of memory space by using software-controlled bank switching techniques. The SmartWatch, also included on the card, time stamps and dates file transactions.

## TECHNICAL DESCRIPTION

The DS6010 PC Port uses several Dallas Semiconductor devices which perform the decoding and control functions of the PC Port. The discussion which follows assumes some understanding of each specific device. If a more detailed explanation of any device is required, the individual data sheet of each part should be studied. These data sheets are supplied in the Dallas Semiconductor Data Book.

The signals from the expansion bus which are used by the DS6010 arrive through the 62-position card edge connector as shown in Figure 1. These signals are used by the DS6010 to develop two 32K x 8 memory spaces from unused sections of the computer memory map. One of the memory spaces is mapped to Cartridges and Cartridge Clips through two 28-pin Bytewide memory sockets which have a pinout as shown in Figure 2. The two sockets are bused directly together. One socket (U10) is mounted horizontal to the IBM expansion slot seating plane and allows for convenient connection via ribbon cable to a Cartridge or Cartridge Clip mounted within the computer cabinet (see Figure 3). The second socket (U11) is mounted vertically and is positioned near the mounting bracket of the DS6010. This socket provided convenient connection via ribbon cable to a Cartridge or Cartridge Clip mounted externally to the computer cabinet. The second memory space developed by the DS6010 contains the DS1216 SmartWatch and 32K x 8 of nonvolatile static RAM. The decoding scheme of the DS6010 is both flexible and soft. The two 32K x 8 blocks of memory space can be located anywhere within the one megabyte memory map of the system. Normally the lower 640K bytes are reserved for DRAM so the decoder would be set for some area in upper memory space. The decoder scheme is soft because the software supplied with DS6010 can set the decoder boundaries using software commands. The software commands are directed to a device called the DS1292 Eliminator which is an electronic replacement for mechanical DIP switches. The Eliminator is nonvolatile and once the switches are set they will remain in the programmed state indefinitely. The interface between the system bus and the Eliminator is developed by the DS1206 Phantom Interface. The DS1206 has the ability to decipher memory cycles which do not impact other system operation into the signals which set the DS1292 to the proper address boundaries. Once the Eliminator is properly set, the logic locks out future changes to the decoder settings.

**IBM EXPANSION BUS 62-PIN CONNECTION** Figure 1

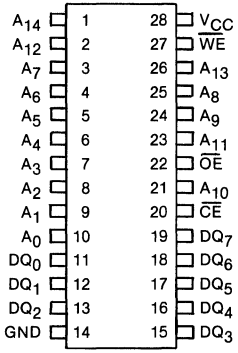


## 28-PIN BYTEWIDE SOCKET PINOUT Figure 2

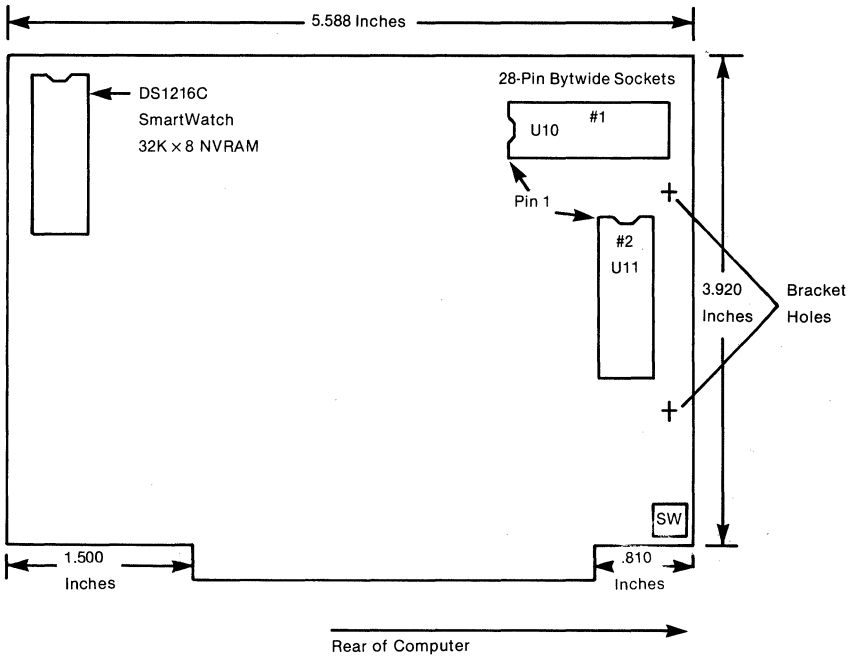
### PIN NAMES

| | |
|---|---|
| $A_0$-$A_{14}$ | Address Inputs |
| $\overline{CE}$ | Chip Enable |
| GND | Ground |
| $DQ_0$-$DQ_7$ | Data In/Data Out |
| $V_{CC}$ | Power (+5 V) |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |

### PIN CONNECTIONS



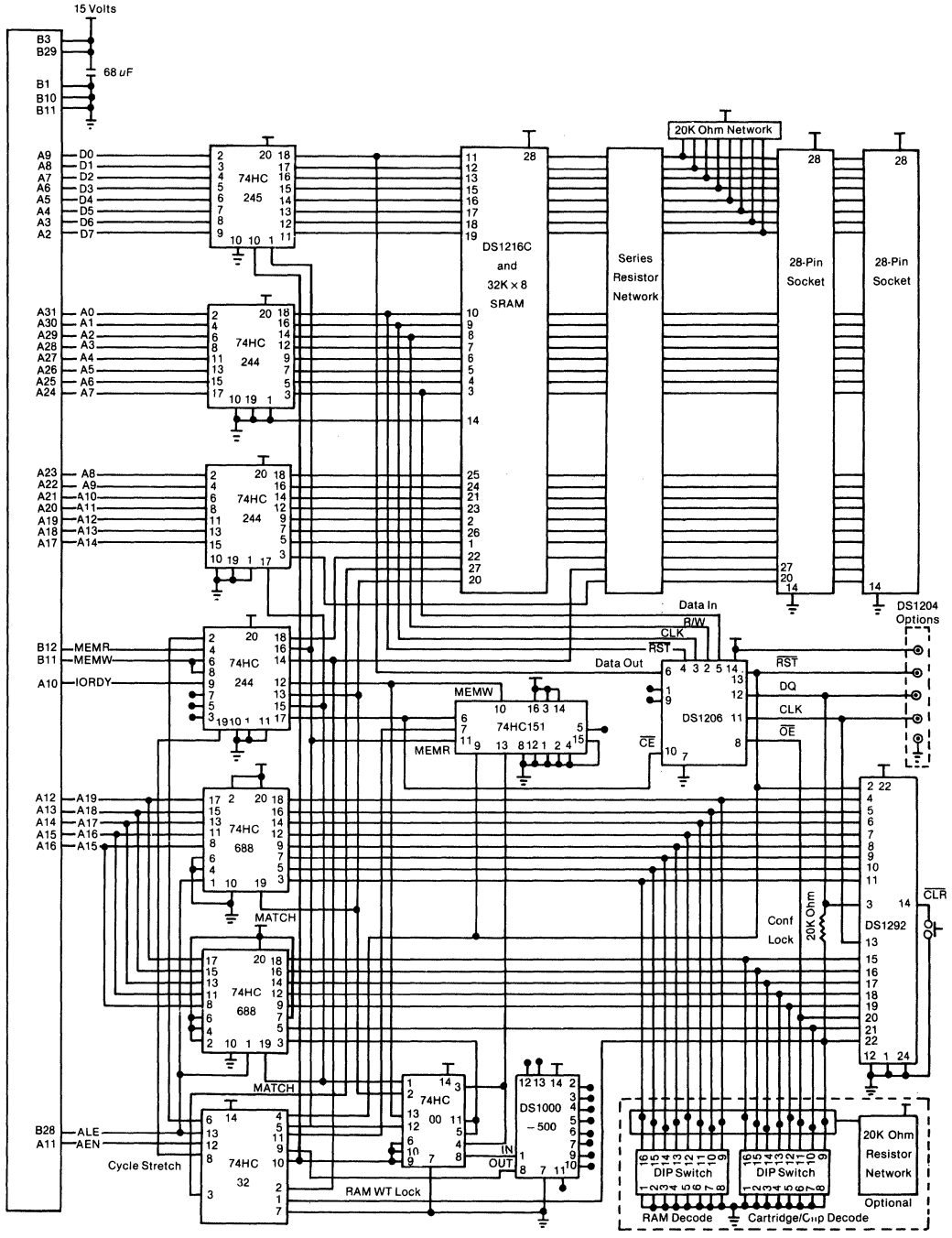

## 28-PIN BYTEWIDE SOCKET LOCATIONS Figure 3



**ELECTRICAL OPERATION**

The address bus A0 through A14 arrives at the inputs of two 74HC244 line receivers through the 62-position card edge connector (see Figure 4). Since both of the gate signals are grounded, the 74HC244 acts only as a buffer. All 15 address lines are bused directly through to the Bytewide memory socket sights. A third 74HC244 is used to buffer control signals $\overline{MEMR}$ (Memory Read), $\overline{MEMW}$ (Memory Write) and IORDY (I/O Ready). $\overline{MEMR}$ and $\overline{MEMW}$ are both logically ORed with signals developed by the decoder logic which will be discussed later in this text. The results of this logic produces the $\overline{OE}$ (Output Enable) and the $\overline{WE}$ (Write Enable) signals for the Bytewide memory socket sites. The IORDY line is an output signal from the PC Port card to the computer expansion bus. When this signal is active, the current bus cycle is extended. The DS6010 drives this line low when either a memory read or a write cycle is being executed to one of the 32K x 8 memory blocks. A set of four NAND gates (1-74HC00) and a delay line DS1000 generate a "cycle stretch" signal which controls the length of time that the IBM PC Port will hold the IORDY signal active. As shipped by Dallas Semiconductor, this length of time is set at 500 ns. However, this length of time can be shortened or lengthened by changing the value of the DS1000 delay line. The length of time allotted must be long enough to allow for the propagation delay of the buffers and the access time of the cartridges or cartridge clip which is installed into the 32K x 8 socket sites. The data bus D0 through D7 arrives at a 74HC245 octal transceiver through the 62-position card edge connector. The 74HC245 has both a gate and a direction control. The direction control is set via the $\overline{MEMR}$ signal which is buffered by a 74HC244 line receiver. The direction control will, therefore, set the 74HC245 to drive the system bus whenever the $\overline{MEMR}$ signal is in the active state and when the gate signal is also active. The gate on the 74HC245 is controlled by the logical combinations of $\overline{MEMR}$ and $\overline{MEMW}$ and the match output pin of two 74HC688 8-bit identity comparators. The logic combination of these four signals is accomplished using three two-input NAND gates. The output pins of the 74HC688 also become the $\overline{CE}$ (Chip Enable) inputs for the two 32K x 8 memory blocks. The $\overline{CE}$ signal for the 28-pin sockets for cartridge and cartridge clip connection is buffered through a 74HC244. The gates of the 74HC688 are enabled by the ALE (Address Latch Enable) signal from the computer expansion bus which is active when system bus addresses are valid. Address lines A15 through A19 are connected to the "P" input sides of the 8-bit binary comparator. The Q input sides are connected for the most part to the Eliminator. The comparison of the P and Q sides will, therefore, produce a match output and select one of the 32K x 8 memory boundaries when the Eliminator settings compare to the levels on address lines A15 through A19. The 74HC688, which is used to decode the 32K x 8 block of nonvolatile static RAM, is driven by eight Eliminator outputs to the Q inputs. Since only five address lines are used on the P side, three inputs are tied to fixed levels. The Pin 2 input is connected to $V_{CC}$ and pins 4 and 6 are grounded. The 74HC688, which is used to decode the 32K x 8 block of memory for cartridges or cartridge clips, is driven directly by only 6 Eliminator outputs to the Q inputs. One of the remaining Q inputs is connected to a read or write signal which allows the identity comparator to only output a chip enable signal when a valid read or write cycle is occurring. The other Q input is unused and connected to a fixed high level. Again only five address lines are connected to the P side. The remaining P inputs are tied to a fixed high level. As mentioned earlier, only 6 Eliminator outputs were used by the 74HC688, which is used to decode the memory block for cartridges or cartridge clips. The other two outputs have special functions. The output on pin 22 of the Eliminator is used to lock out the write enable signal which goes to the nonvolatile RAM site. This allows a convenient way in which software can be used to write protect the nonvolatile RAM. The other output on pin 20 of the eliminator is used to lock out the DS1206 Phantom Interface by disabling the $\overline{OE}$ (Output Enable) signal after the

## DS6010 PC PORT ELECTRICAL SCHEMATIC Figure 4



Eliminator is set for proper system configuration. Communications to the Eliminator, which allows the system configuration to take place, is handled by the DS1206 Phantom Interface, which is controlled by the 74HC151 data selector and software. Bus cycles which set proper address patterns on address lines A0, A1, A2 and A7 are clocked into the DS1206 using consecutive $\overline{CE}$ cycles. The $\overline{CE}$ for the DS1206 is generated under two different sets of conditions by the 74HC151 based on the state of $\overline{MEMR}$ and $\overline{MEMW}$. Initially, the DS1206 must receive 24 bits of data which must match exactly with the code embedded into the DS1206. (Consult the DS1206 data sheet for exact details on the DS1206 operation.) Prior to this condition, the DS1206 is a passive listener on the bus and will not output any signals to the Eliminator. During this time the $\overline{CE}$ input to the DS1206 from the 74HC151 will be active only when $\overline{MEMW}$ is active (see Table 1). Since write cycles can be accomplished to known memory addresses where ROM resides, no memory alterations occur and these cycles can be transparent to the rest of the system. However, as soon as the 24-bit pattern match is completed, the DS1206 will pass signals to the DS1292 from the address bus. Address line A0 will be passed through as the $\overline{RST}$ (Reset) signal; address line A1 becomes the CLK (Clock); A2 defines whether data is to be read or written; and address A7 becomes the data input to the Eliminator. (Consult the DS1292 data sheet for exact details on Eliminator.) The first requirements for entering data into the Eliminator is to set the $\overline{RST}$ input to a high level. This signal is also sent as an input to the 74HC151 data selector. This new input now allows $\overline{CE}$ for the DS1206 to be active when $\overline{MEMW}$ is active and also when $\overline{MEMR}$ is active and either of the two 74HC688 is outputting a match signal indicating that one of the two 32K x 8 blocks of memory is being accessed. This new set of circumstances allows the Eliminator status to be read back via the system bus DQ0 line. Bus contention is avoided from either of the two 32K x 8 memory blocks as the $\overline{OE}$ signal to the memory blocks is inhibited as long as $\overline{RST}$ to the DS1292 is at a high level. Data is passed back through the DS1206 by the feedback resistor which couples the Eliminator output back to the input. Once the Eliminator is set and verified, system configuration can be terminated and locked by making sure the bit which is output on pin 20 of the Eliminator is set to logic one when the $\overline{RST}$ signal is driven low. The Eliminator can always be put back in an unconfigured state by depressing the $\overline{CLR}$ (Clear) button which forces all of the Eliminator outputs low.

**1206 ENABLE** Table 1

| $\overline{RST}$ | $\overline{MEMW}$ | $\overline{MEMR}$ | $\overline{MATCH}$ | $\overline{ENABLE}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |

| $\overline{RST}$ | $\overline{MEMW}$ | $\overline{MEMR}$ | $\overline{MATCH}$ | $\overline{ENABLE}$ |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**ELECTRICAL OPTIONS**

The DS6010 has provisions for mechanical DIP switches and pull-up resistors which can be used in place of the Eliminator. While the DS6010 is not shipped with these components, they can be added if needed for a specific application (see Figure 4). If DIP switches and pullup resistors are used, the Eliminator should be removed from its socket. The DS6010 can also be optioned with the Dallas Semiconductor DS1204 Key for software protection and access control. Under special contract with Dallas Semiconductor, these options can be supplied to customer specifications.

**NOTE:**

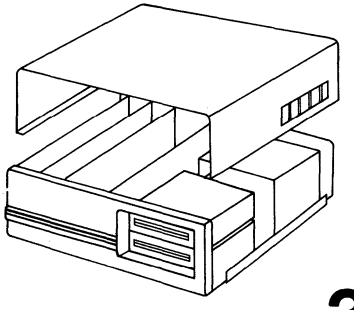
Contact Dallas Semiconductor Sales Office for ordering information.

**INSTALLATION**

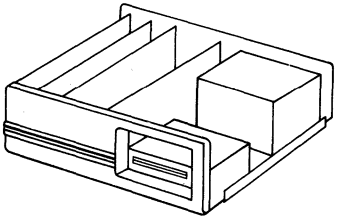
In order to install the DS6010 into a computer it will be necessary for the computer cabinet to be removed (Figure 5). Prior to installation, the computer should be tested to make sure it is operating properly. After the computer has been tested disconnect any peripheral equipment that is attached to the computer and make sure that the A.C. power is unplugged. Then consult the owner's manual on the computer for instructions which explain how to remove the cabinet. After the cabinet is removed, the DS6010 can be installed in any available I/O slot except PC XT Slot B. It is a good idea to connect the ribbon cable which will connect either the Cartridge or the Cartridge Clip to the appropriate 28-pin socket. If the Cartridge or Cartridge Clip is mounted within the computer cabinet, the horizontal 28-pin socket on the top of the PC board would be the proper choice (see Figure 3). When mounting the Cartridge or Cartridge Clip external to the computer, the vertical 28-pin socket should be used. The

**INSTALLATION** Figure 5

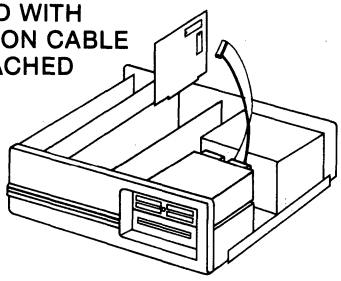
**1.** REMOVE COVER



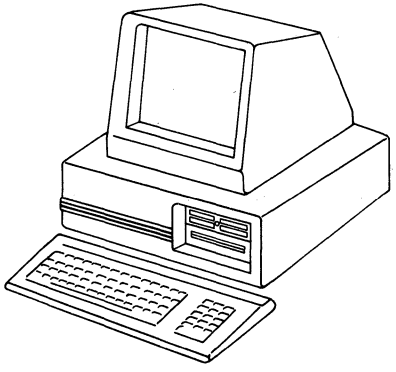
**2.** REMOVE FLOPPY DISK DRIVE



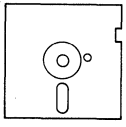
**3.** INSTALL THE CARTRIDGE CLIP, INSERT THE PC PORT I/O CARD WITH RIBBON CABLE ATTACHED



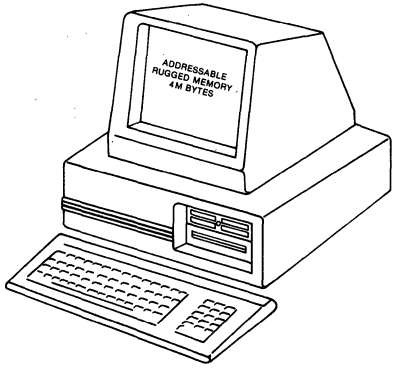
**4.** REASSEMBLE COMPUTER



**5.** INSTALL SOFTWARE



**6.** FUNCTIONAL SOLID-STATE COMPUTER



data sheet on the DS9020 Cartridge Clip can be used for mounting dimensions. The Cartridge Clip will fit in the place of any half-high disk drive. If a DS1217 Cartridge is being used, the DS1217 data sheet can be used to provide mechanical dimensions. Mechanical hardware for mounting the DS1217 is not supplied by Dallas Semiconductor; however, the DS9000 ribbon cable is available to provide electrical connection between the Cartridge and the DS6010. When connecting the ribbon cable to the DS6010, care should be taken to avoid incorrect connection. Pin 1 on the ribbon cable must match Pin 1 on the 28-pin socket. Figure 3 identifies the Pin 1 locations on the 28-pin sockets. Pin 1 is on the opposite end of a color stripe on the ribbon cable. (See the data sheet on the DS9020.) When using the DS9000 ribbon cable with a Cartridge, Pin 1 is on the same end as the color stripe. ***NOTE:*** *Improper connection of the ribbon cable can damage the Cartridge Clip, Cartridge and PC Port.* After the installation is complete the computer cabinet should be replaced and the peripheral devices reconnected. When power is applied to the computer, it should function the same as before the DS6010 was installed. It will be necessary to install the supplied software to make the PC Port operational.

**SOFTWARE INSTALLATION**

The floppy disk provided with the PC Port contains both the software and the instructions for installing the software. The instructions for installation can be retrieved by installing the floppy disk marked "DS6010 Software" into the default disk drive and typing "TYPE DS6010.MEM" The print command can be used to make a hard copy. This manual should be read and followed carefully while doing the software installation. After the software installation is complete, the system will respond to all DOS commands and the IBM PC Port, Cartridge and Cartridge Clip will appear to behave as added disk storage.

**DS6010 PC PORT SPECIFICATION**

ORGANIZATION: Two 32K x 8 Memory Blocks
INPUT CONNECTION: IBM PC XT AT Expansion Bus
OUTPUT CONNECTION: JEDEC 28-Pin Bytewide Sockets
ACCESS TIME: 1 *u*S per Byte Maximum*
TEMPERATURE RANGE: 0°C to 70°C
SIZE: 1/2 Length I/O Card
5.5 Inches Long x 3.2 Inches High
REAL TIME CLOCK ACCURACY: ±1 Minute/Month@25°C
SOFTWARE: PC DOS Compatible
POWER CONSUMPTION: 500 MW Maximum
ADDRESS MAP RANGE: 1 Megabyte

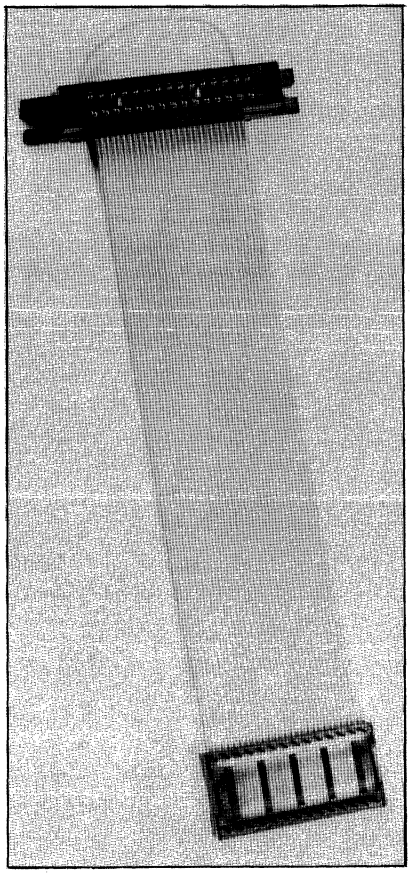
*Performance can be enhanced by lowering the value of the cycle stretch delay line.

# Dallas Semiconductor
## *Byte Wide Cable Harness*

## *DS9000*

### FEATURES

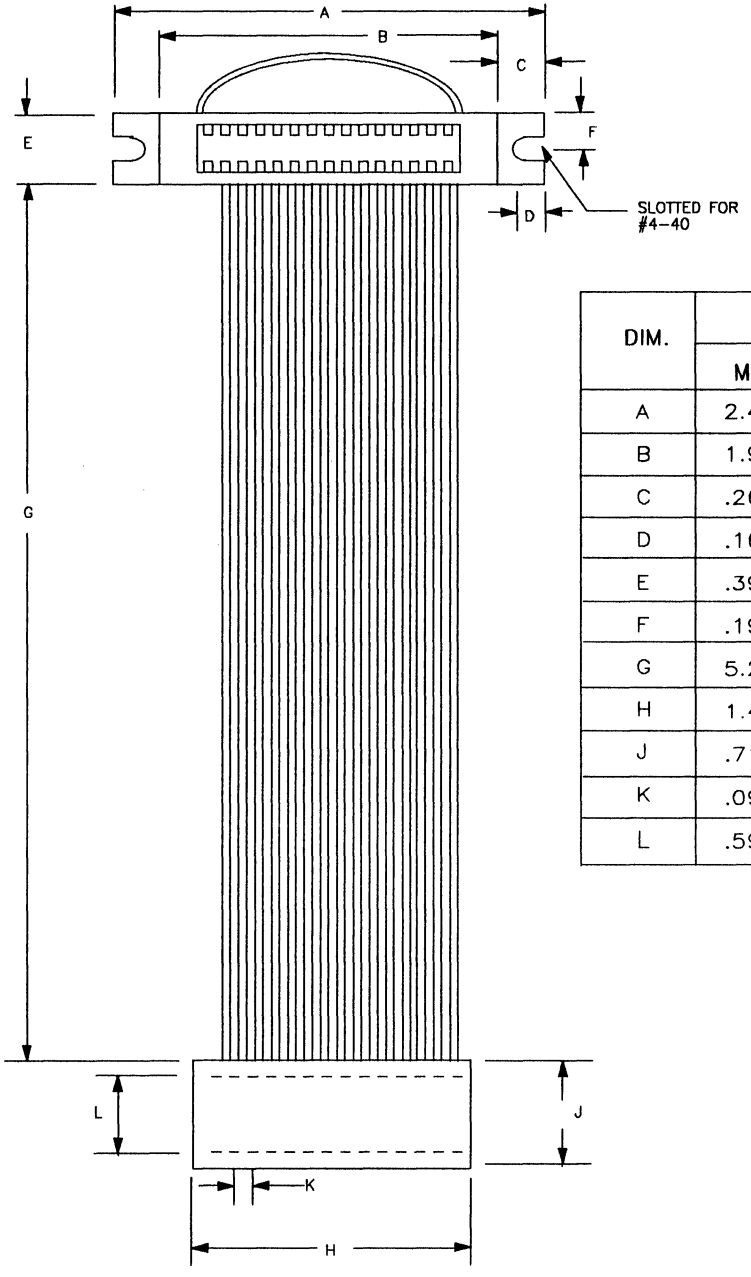
- Converts 30 position card edge to popular byte wide 28 pin socket
- Bifurcated cantilever beam card edge design provides redundant contact
- Mechanical keys provide proper insertion and withdrawal of Dallas Semiconductor DS1217 Nonvolatile Memory Cartridges
- 28 position dip plug inserts into any standard 28 position I.C. Socket
- Color stripe indicates pin one on 28 pin dip plug
- Standard six inch cable length
- Interfaces directly to the DS6010 P.C. Port



### DESCRIPTION

The DS9000 is a specially designed cable harness which converts Dallas Semiconductor DS1217 Nonvolatile Memory Cartridges or any other 30 position card edge to the popular Byte Wide 28 Pin Socket. An additional ground lead, and dual key positions allow for proper insertion and withdrawal of Nonvolatile Memory Cartridges. A six inch cable length allows for flexibility in end application but does not substantially effect the performance characteristics of the DS1217 Memory Cartridge.

# DS9000
# Byte Wide Cable Harness



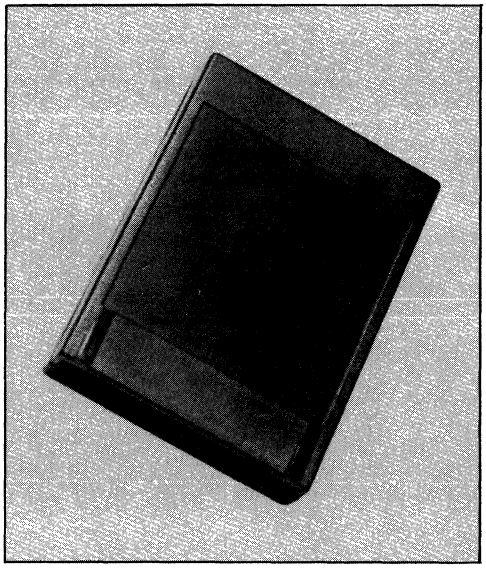

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 2.480 | 2.520 |
| B | 1.940 | 1.980 |
| C | .260 | .280 |
| D | .160 | .175 |
| E | .395 | .415 |
| F | .195 | .205 |
| G | 5.25 | 5.65 |
| H | 1.470 | 1.500 |
| J | .715 | .735 |
| K | .090 | .110 |
| L | .590 | .610 |

# Dallas Semiconductor
## *Cartridge Housing*

## *DS9002*

### FEATURES

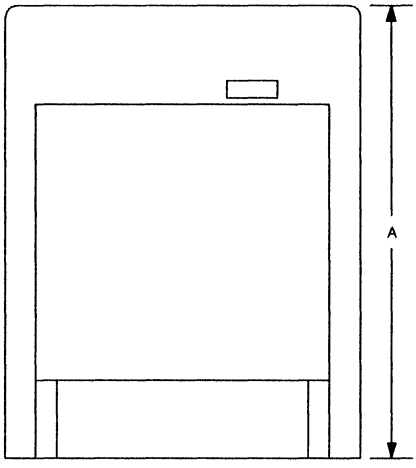
- Two piece snap together construction
- Matches form factor of Dallas Semiconductor nonvolatile memory cartridges
- Made of rugged, flame retarded ABS plastic
- Accepts DS9003 prototype cartridge P.C.B.
- Openning for switch or jumper
- Component clearance of .175" solder side, .200" circuit side using .062" P.C.B.



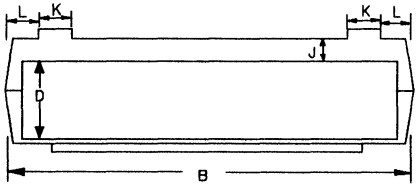
### DESCRIPTION

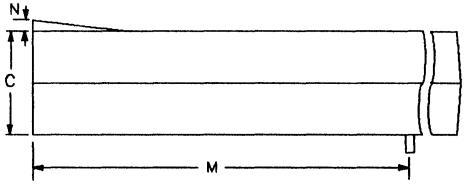
The DS9002 is a rugged, two piece snap together cartridge housing designed for use in any portable cartridge application. Components can be either thru hole mounted or surface mounted on both sides depending upon density requirement and board design. The outside profile of the P.C.B. should match the DS9003 prototype P.C.B. Applications include Nonvolatile Static RAM, ROM, or EPROM memory cartridges.

# Cartridge Housing
# DS9002




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 3.020 | 3.040 |
| B | 2.280 | 2.300 |
| C | .590 | .610 |
| D | .440 | .460 |
| J | .115 | .135 |
| K | .115 | .135 |
| L | .140 | .160 |
| M | 1.760 | 1.790 |
| N | .040 | .060 |



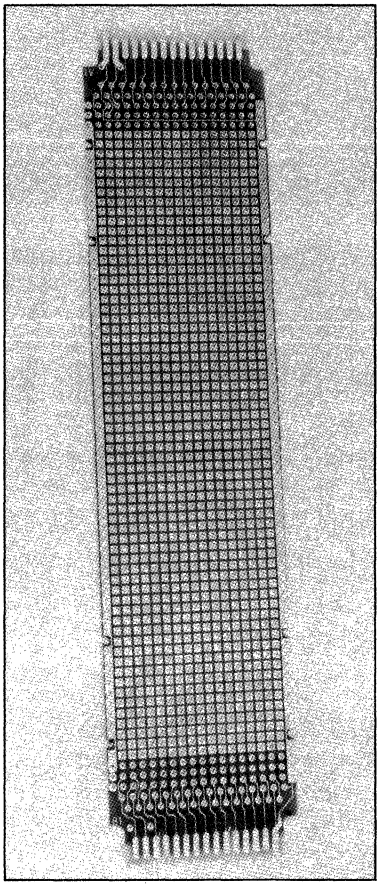



# Dallas Semiconductor
## *Cartridge Proto Board*

## *DS9003*

### FEATURES

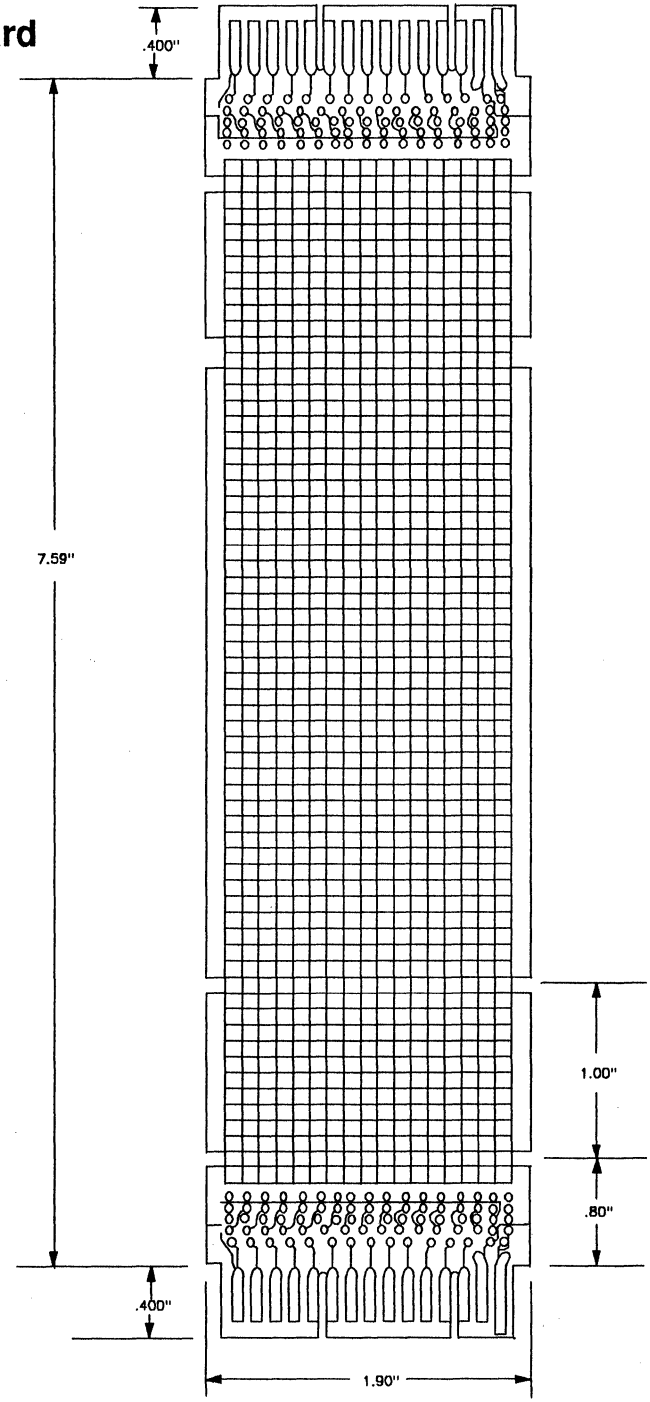
- Matches profile of DS1217 Nonvolatile memory cartridges
- Plated through hole pattern for wire wrap or solder mount development
- Allows for a single double sized cartridge or two standard size cartridges
- Gold plated card edge fingers
- Connects to standard 28 pin bytewide socket via DS9000
- Key slots provide for proper insertion and removal
- Separate full length power and ground buses for ease of layout



### DESCRIPTION

The DS9003 is a developmental printed circuit board for prototyping portable hand held cartridges . Thirty gold plated card edge connections conform to the popular 28 pin bytewide socket pin-out when used with the DS9000 cable harness . The card profile matches that of the DS1217 nonvolatile memory cartridges and can be used with the DS9002 cartrige housing.

# Cartridge Proto Board
# DS9003



# Dallas Semiconductor
## *Cartridge Clip*

PRELIMINARY
**DS9020**

**FEATURES**

- Holds up to eight nonvolatile read/write memory Cartridges
- Fits within the panel opening of a half-height 5¼″ disk drive
- Mounts with same brackets as disk drive
- Accepts Cartridges ranging from 16K to 4M bits for capacity of up to 4M bytes
- Four user-insertable Cartridges plug into the front
- Four removable Cartridges plug into the rear
- Standard Bytewide pinout connects to JEDEC 28-pin DIP socket via ribbon cable
- Software-controlled banks maintain 32K × 8 JEDEC pin compatability
- Indicator illuminates red while data is transferring
- Rugged and durable construction
- Wide operating temperature range of 0°C to 70°C

**DESCRIPTION**

The DS9020 Cartridge Clip is a housing with circuitry designed to interface up to eight nonvolatile read/write memory Cartridges to a computer memory bus. The complete unit will fit in the same space which could otherwise hold a standard 5¼″ half-height floppy or hard disk drive. Using a total of 8 DS1217M-4 memory Cartridges in the DS9020 gives a density of 4 megabytes of transportable nonvolatile memory with access time of Static RAM. Four user-insertable memory Cartridges plug into the front of the Cartridge Clip while four removable Cartridges plug into the rear. The Cartridge Clip connects to the computer via a ribbon cable into a standard Bytewide JEDEC 28-pin DIP socket. Software-controlled bank switching techniques provide an expandable memory through a 32K × 8 window within the host computer's memory map. The DS9020 Cartridge Clip provides a rugged, solid-state storage alternative to rotating magnetic memory.

## OPERATION

The DS9020 Cartridge Clip includes switching circuitry for up to 8 DS1217 Cartridges. Connection to a computer memory bus is made via a 28-pin DIP adapter with the pinout as shown in Figure 1. Normal read and write memory cycles are directed through the 28-pin DIP and ribbon cable to one of eight Cartridges. (See the data sheet on the DS1217A and DS1217M cartridges for normal read and write cycle timing.) Cartridges are selected by a software-controlled switch which selects only one Cartridge at a time. An indicator on the front of the Cartridge Clip illuminates while the data is being transferred.

## CARTRIDGE SELECTION

Initially, on power up, all of eight possible Cartridges in the Cartridge Clip are deselected. Cartridge selection is accomplished by matching a predefined pattern stored within the cartridge Clip with a 16-cycle sequence on address lines $A_0$, $A_1$, $A_2$ and $A_3$. Prior to sending the 16-cycle sequence which will set the bank switch, a read cycle with bit patern 1111 on address inputs $A_0$, $A_1$, $A_2$ and $A_3$ must be executed to initiate pattern entry. Each set of address inputs is clocked into the the Cartridge Clip when the $\overline{CE}$ pin (Cartridge Clip enable) is driven low. All 16 inputs to the Cartridge Clip must be consecutive read or write cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for address inputs $A_1$, $A_2$ and $A_3$; however, address line $A_0$ defines the Cartridge number to be enabled as per Table 2.

Switching to a selected Cartridge occurs on the rising edge of Cartridge Clip enable when the last set of bits is input and a match has been established. After Cartridge selection, subsequent Cartridge Clip enables will be directed to the selected Cartridge with additional propagation delay of 150 ns. (Note: this additional delay must be added to the respective DS1217 Cartridge performance specifications when considering overall read and write cycle times.) The selected Cartridge position can be determined from Figure 2. Figure 3 is a block diagram and Figure 4 is an electrical wiring diagram of the DS9020. Figure 5 shows the mechanical and dimensional considerations for the Cartridge Clip.

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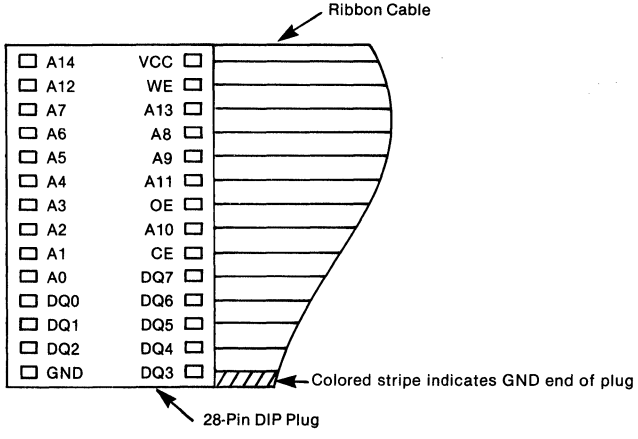
## ADDITIONAL ACCESSORIES AVAILABLE

Dallas Semiconductor offers the DS6010 PC Port which is an I/O expansion board that will connect the DS9020 into PC, XT, AT and compatible computers. For additional information contact Dallas Semiconductor.

**CARTRIDGE CLIP** Figure 1

28-Pin DIP Plug Interface Pinout



**ADDRESS INPUT PATTERN** Table 1

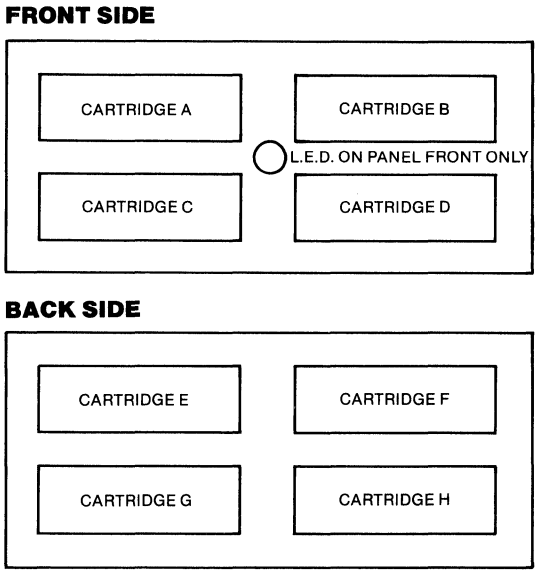
| | Bit Sequence | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Address Inputs** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** |
| $A_0$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | × | × | × | × | × |
| $A_1$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| $A_2$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| $A_3$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

× See Table 2

**BANK SELECT CONTROL** Table 2

| **Bank Selected** | **$A_0$ Bit Sequence** | | | | |
|---|---|---|---|---|---|
| | **11** | **12** | **13** | **14** | **15** |
| All Cartridges Off | 0 | DON'T CARE | DON'T CARE | DON'T CARE | DON'T CARE |
| Cartridge A | 1 | 0 | 0 | 0 | 0 |
| Cartridge B | 1 | 0 | 0 | 0 | 1 |
| Cartridge C | 1 | 0 | 0 | 1 | 0 |
| Cartridge D | 1 | 0 | 0 | 1 | 1 |
| Cartridge E | 1 | 0 | 1 | 0 | 0 |
| Cartridge F | 1 | 0 | 1 | 0 | 1 |
| Cartridge G | 1 | 0 | 1 | 1 | 0 |
| Cartridge H | 1 | 0 | 1 | 1 | 1 |

Figure 2

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**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 85°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Pin 28 Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input High Level | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1 |
| Input Low Level | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Operating Current | $I_{CC1}$ | | 6 | 50 | ma | 2 |
| Operating Current | $I_{CC2}$ | | 15 | | ma | 3 |
| Operating Current | $I_{CC3}$ | | 40 | | ma | 4 |
| Input Drive Low Level | $I_{IL}$ | | | 1.0 | ma | 5 |
| Input Drive High Level | $I_{LO}$ | | | 0.5 | ma | 5 |
| Output Drive @2.4V | $I_{OH}$ | −1.0 | | | ma | 6 |
| Output Drive @0.4V | $I_{OL}$ | 2.0 | | | ma | 6 |

**CAPACITANCE** ($t_A$ = 25 °C)

| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 500 | 750 | pF | 2 |
| D/Q Capacitance | $C_{D/Q}$ | 500 | 750 | pF | 2 |

**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC}$ = 5V ± 10%)

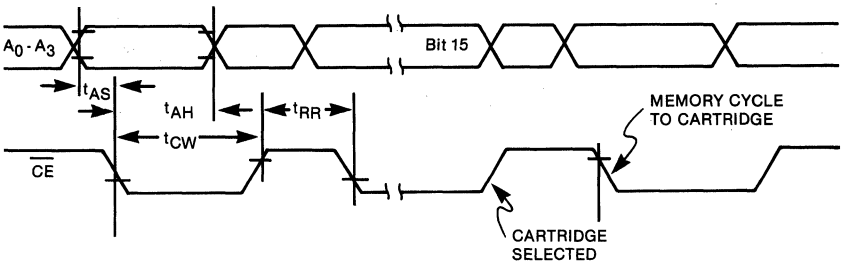
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Address Set-Up | $t_{AS}$ | 20 | | | ns | |
| Address Hold | $t_{AH}$ | 100 | | | ns | |
| Read Recovery | $t_{RR}$ | 80 | | | ns | |

**DS1217M CARTRIDGE TIMING WHILE INSTALLED IN THE DS9020**
**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 440 | | | ns | |
| Access Time | $t_{ACC}$ | | | 400 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | | 275 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | | 400 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 50 | | | ns | |
| Output High Z From Deselection | $t_{OD}$ | | | 125 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | | ns | |
| Read Recovery Time | $t_{RR}$ | 40 | | | ns | |
| Write Cycle Time | $t_{WC}$ | 440 | | | ns | |
| Write Pulse Width | $t_{WP}$ | 350 | | | ns | |
| Address Set Up Time | $t_{AW}$ | 40 | | | ns | |
| Write Recovery Time | $t_{WR}$ | 40 | | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | | 100 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 10 | | | ns | |
| Data Set Up Time | $t_{DS}$ | 280 | | | ns | |
| Data Hold Time From $\overline{WE}$ | $t_{DH}$ | 25 | | | ns | |

See DS1217M data sheet for timing diagrams.

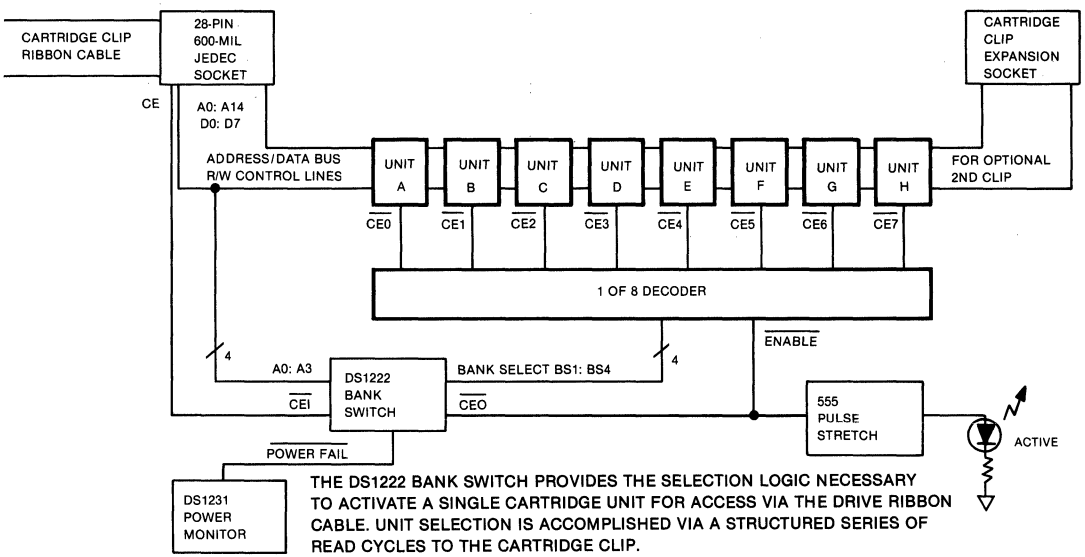
## TIMING DIAGRAM—CARTRIDGE SELECTION




**NOTES:**

1. All voltages are referenced to ground (Pin 14).
2. Cartridge Clip empty.
3. Cartridge Clip loaded to capacity with $\overline{CE}$ at high level.
4. Cartridge Clip loaded to capacity with $\overline{CE}$ at low level.
5. Includes all address, data and control lines.
6. Output drive comes from installed Cartridge.

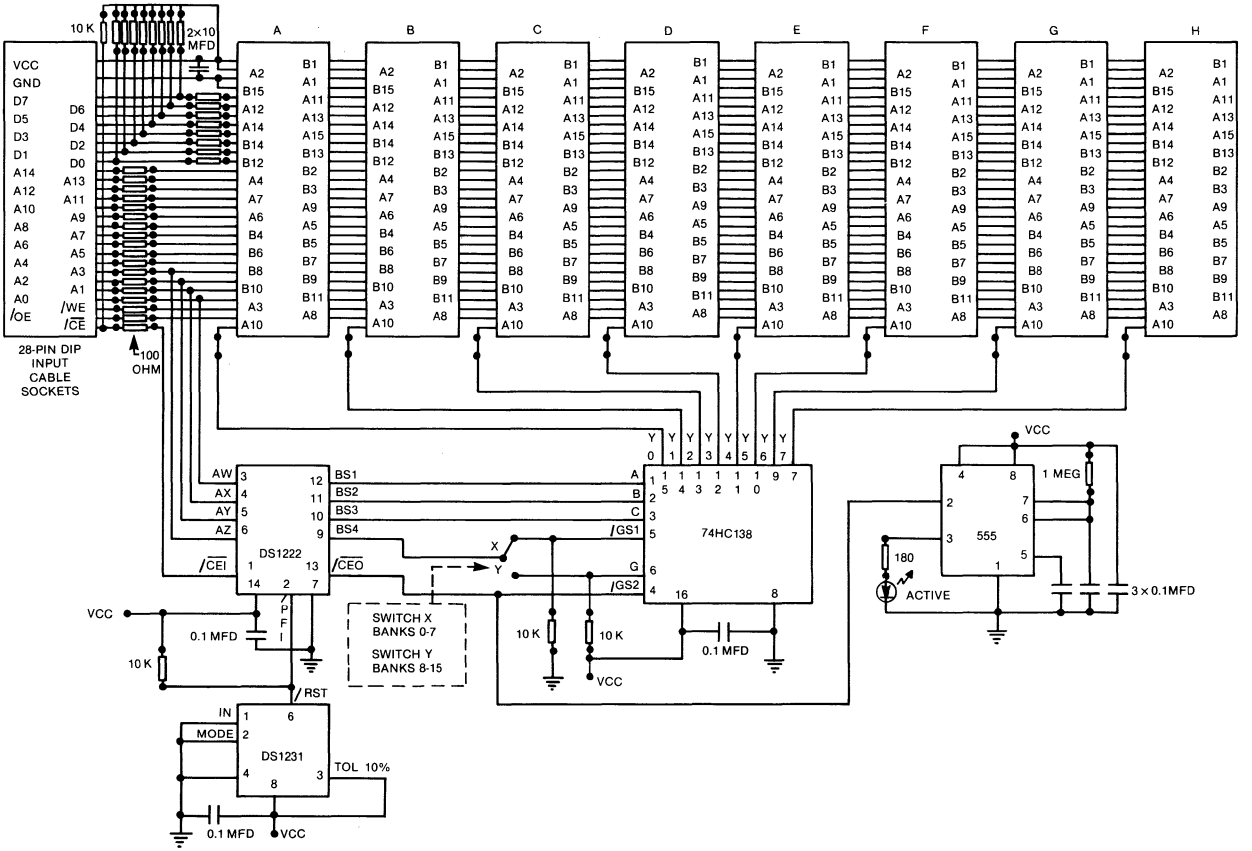
Figure 3




THE DS1222 BANK SWITCH PROVIDES THE SELECTION LOGIC NECESSARY TO ACTIVATE A SINGLE CARTRIDGE UNIT FOR ACCESS VIA THE DRIVE RIBBON CABLE. UNIT SELECTION IS ACCOMPLISHED VIA A STRUCTURED SERIES OF READ CYCLES TO THE CARTRIDGE CLIP.

THE DS1231 POWER MONITOR PROVIDES FAIL DETECTION AND POWER-UP RESET FUNCTIONS. ACCESS TO THE CARTRIDGE UNITS IS DENIED WHEN POWER IS LOW AND UNTIL UNIT SELECTION PROTOCOL IS ACTIVATED ON SYSTEM POWER-UP.

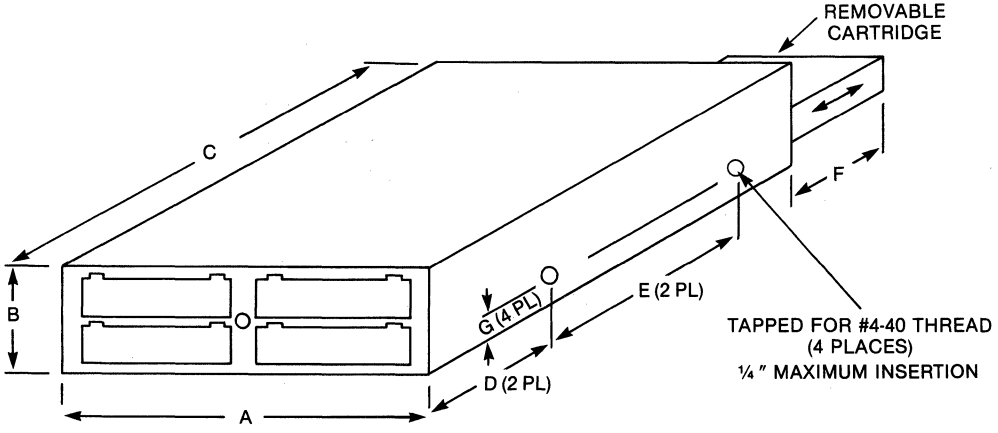
Figure 4


10 K
2x10 MFD
VCC
GND
D7
D5
D3
D1
A14
A12
A10
A8
A6
A4
A2
A0
/OE
D6
D4
D2
D0
A13
A11
A9
A7
A5
A3
A1
/WE
/CE
28-PIN DIP INPUT CABLE SOCKETS
100 OHM
A
B
C
D
E
F
G
H
AW
AX
AY
AZ
DS1222
/CEI
/CEO
BS1
BS2
BS3
BS4
74HC138
/GS1
/GS2
SWITCH X BANKS 0-7
SWITCH Y BANKS 8-15
0.1 MFD
10 K
/RST
IN
MODE
DS1231
TOL 10%
555
1 MEG
180
ACTIVE
3 x 0.1MFD

# *DS9020*
# *Cartridge Clip*

Figure 5

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 5.700 | 5.760 |
| B | 1.605 | 1.635 |
| C | 6.460 | 6.500 |
| D | 2.045 | 2.065 |
| E | 3.100 | 3.120 |
| F | 1.210 | 1.510 |
| G | .390 | .410 |

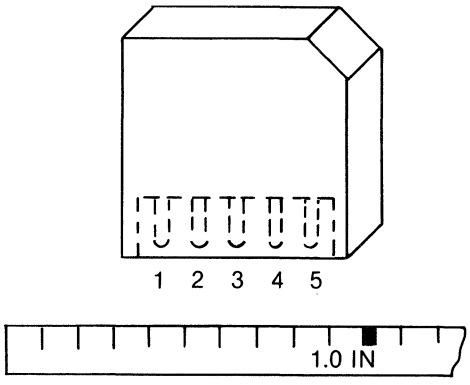


# Security Products

# Dallas Semiconductor
## *Electronic Key* — *DS1204U*

### FEATURES
- Cannot be deciphered by reverse engineering
- Partitioned memory thwarts pirating
- User insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64 bit reprogrammable memory
- Unreadable 64 bit security match code virtually prevents deciphering by exhaustive search with over $10^{19}$ possibilities
- 128 bits of secure read/write memory creates additional barriers against hackers by permitting data changes as often as needed
- Rapid erasure of identification security match code, and secure read/write memory can occur if tampering is detected
- User insertable
- Over 10 years of data retention with no limitations or restrictions on write cycle
- Low power CMOS circuitry
- 4 million bits/second data rate
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| Pin 1 — $V_{CC}$ | +5 VOLTS |
| Pin 2 — $\overline{RST}$ | $\overline{RESET}$ |
| Pin 3 — DQ | DATA INPUT/OUTPUT |
| Pin 4 — CLK | CLOCK |
| Pin 5 — GND | GROUND |

### DESCRIPTION
The DS1204U Electronic Key is a miniature security system which stores 64 bits of user definable identification code and a 64 bit security match code which protects 128 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the key via a special program mode operation. After programming, the key follows a special procedure with a serial format to retrieve or update data.

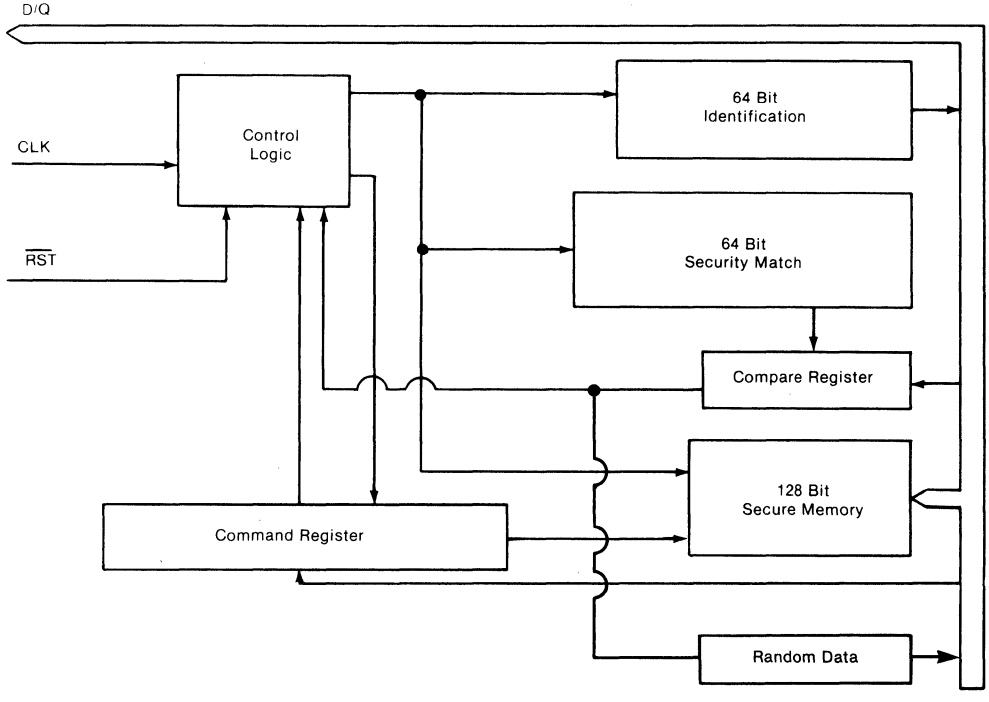
Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfer with only three signals: CLOCK, $\overline{\text{RESET}}$, and DATA INPUT/OUTPUT.

Low pin count and a guided entry for a mating receptacle overcomes mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user insertable.

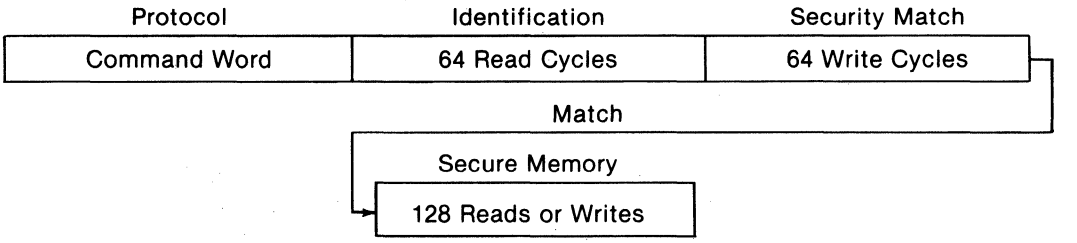
**OPERATION—NORMAL MODE**

The Electronic Key has two modes of operation: the normal mode and the program mode. The block diagram (Figure 1) illustrates the main elements of the key when used in the normal mode. To initiate data transfer with the key, $\overline{\text{RST}}$ is taken high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact bit pattern which defines normal operation for read or write or communications is ignored. If the command register is loaded properly, communications are allowed to continue. The next 64 cycles to the key are read. Data is clocked out of the key on the high to low transition of the clock from the identification memory. Next, 64 write cycles must be written to the compare register. These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, random data is output for the next 128 cycles when reading data. If write cycles are being executed, the write cycles are ignored. If a match is found, access is permitted to a 128-bit read/write nonvolatile memory. Figure 2 is a summary of normal mode operation and Figure 3 is a flow chart of the normal mode sequence.

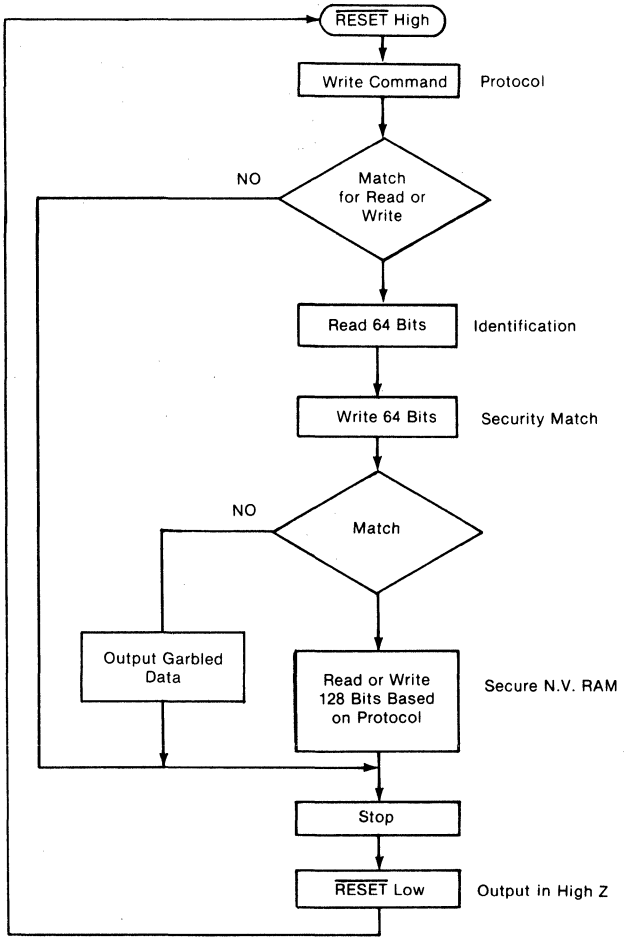
**BLOCK DIAGRAM — NORMAL MODE** Figure 1



**SEQUENCE — NORMAL MODE** Figure 2



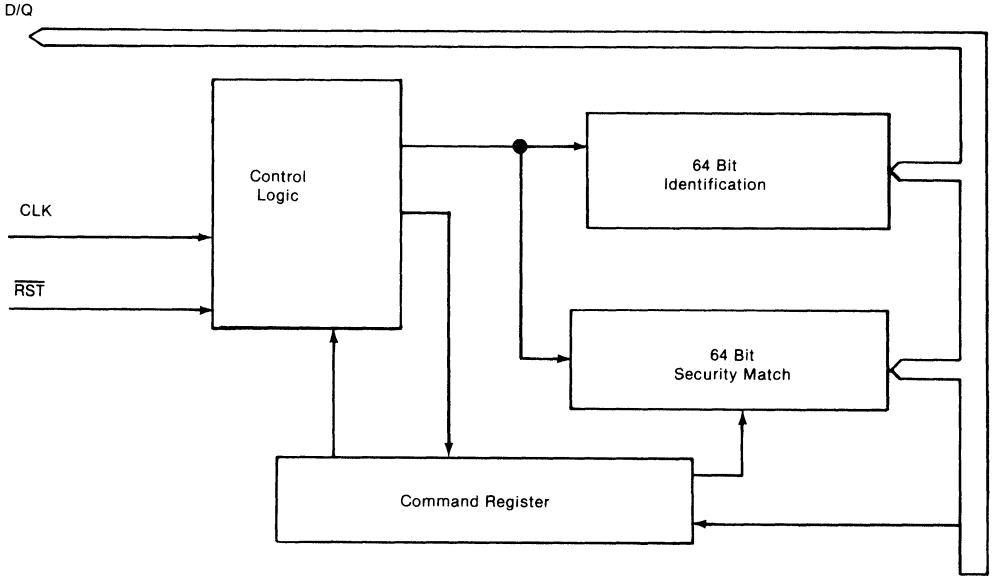

**FLOW CHART — NORMAL MODE** Figure 3



## PROGRAM MODE

The block diagram of Figure 4 illustrates the main elements of the key when used in the program mode. To initiate the program mode, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact pattern which defines program operation. If an exact match is not found, the remainder of the program cycle is ignored. If the command register is properly loaded, then the next 128 bits which follow are written to the identification memory and the security match memory. Figure 5 is a summary of program mode operation and Figure 6 is a flow chart of program mode operation.

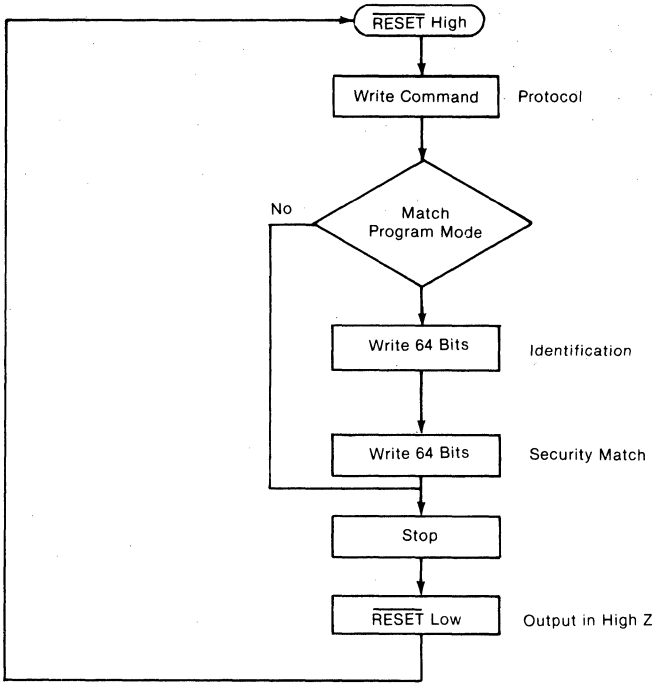
**BLOCK DIAGRAM — PROGRAM MODE** Figure 4




**SEQUENCE — PROGRAM MODE** Figure 5

| Protocol | Identification | Security Match |
|---|---|---|
| Command Word | 64 Write Cycles | 64 Write Cycles |

**FLOW CHART — PROGRAM MODE** Figure 6




**COMMAND WORD**

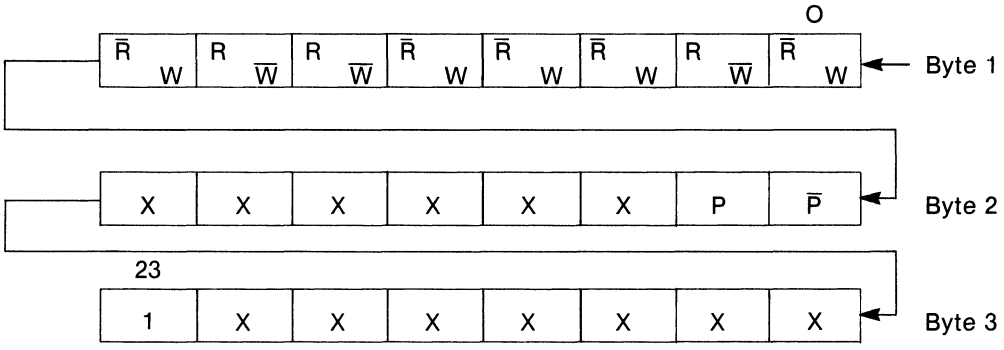
Each data transfer for the normal and program mode begins with a three byte command word as shown in Figure 7. As defined, the first byte of the command word specifies whether the 128 bit nonvolatile memory will be written into or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted.

The 8 bit pattern for read is 01100010. The pattern for write is 10011101. The first two bits of the second byte of the command word specify whether the data transfer to follow is a program or normal cycle. The bit pattern for program is 0 in bit 0 and 1 in bit 1. The program mode can be selected only when the first byte of the command word specifies a write. If the program mode is specified and the first byte of the command word does not specify a write, data transfer will be aborted. The bit pattern which selects the normal mode of operation is 1 in bit 0 and 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause data transfer to abort.

The remaining 6 bits of byte 2 and the first 7 bits of byte 3 form unique patterns which allow multiple keys to reside on a common bus. As such, each respective code pattern must be written exactly for a given device or data transfer will abort. Dallas Semiconductor has 5 patterns available as standard products per the chart in Figure 7. Each pattern corresponds to a specific part number. Under special contract with Dallas Semiconductor the user may specify any bit pattern other than that specified by Dallas Semiconductor as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last bit of byte 3 of the command word must be written to logic 1 or data transfer will abort.

NOTE: Contact Dallas Semiconductor Sales Office for special command word code assignment which makes possible an exclusive blank key.

**COMMAND WORD** Figure 7




| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| DS1204U-1 | 0 | 0 | 0 | 0 | 0 | 0 | P | $\overline{P}$ | Byte 2 |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Byte 3 |
| DS1204U-2 | 0 | 0 | 0 | 0 | 0 | 1 | P | $\overline{P}$ | Byte 2 |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Byte 3 |
| DS1204U-3 | 0 | 0 | 0 | 0 | 1 | 0 | P | $\overline{P}$ | Byte 2 |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Byte 3 |
| DS1204U-4 | 0 | 0 | 0 | 0 | 1 | 1 | P | $\overline{P}$ | Byte 2 |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Byte 3 |
| DS1204U-5 | 0 | 0 | 0 | 1 | 0 | 0 | P | $\overline{P}$ | Byte 2 |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Byte 3 |

## RESET AND CLOCK CONTROL

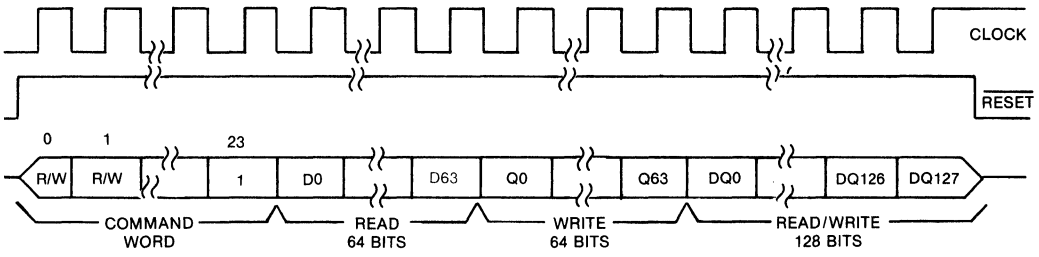
All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2 mA @ 3.0 volts is required. However, if the $V_{CC}$ pin is connected to a 5 volt source within nominal limits, then $\overline{RST}$ is not used as a source of power and input levels revert to normal $V_{IH}$ and $V_{IL}$ inputs with a drive current requirement of 500 uA. Third, the $\overline{RST}$ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates if the $\overline{RST}$ pin is low and the DQ pin goes to a high impedance state. When data transfer to the key is terminated and using $\overline{RST}$, the transition of $\overline{RESET}$ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 8 for normal mode and Figure 9 for program mode.

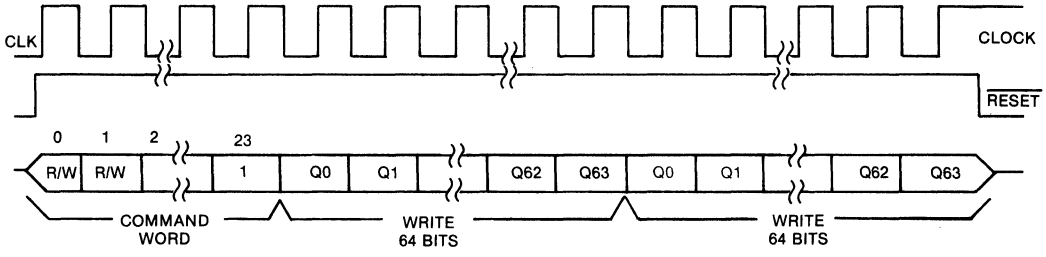
## KEY CONNECTIONS

The key is designed to be plugged into a standard 5 pin 0.1 inch center SIP receptacle. A guide is provided to prevent the key from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the key pins can be determined to insure connection integrity before data transfer begins. CLK, $\overline{RST}$, and DATA INPUT/OUTPUT all have internal 20K Ohm pull down resistors to ground which can be sensed by a reading device.

**DATA TRANSFER — NORMAL MODE** Figure 8




**DATA TRANSFER — PROGRAM MODE** Figure 9




9

## ABSOLUTE MAXIMUM RATINGS*

| | | |
|---|---|---|
| VOLTAGE ON ANY PIN RELATIVE TO GROUND | — | −1.0V to +7V |
| OPERATING TEMPERATURE | — | 0°C to 70°C |
| STORAGE TEMPERATURE | — | −40°C to +70°C |

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | | V | 1,8,10 |
| Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| $\overline{\text{RESET}}$ Logic 1 | $V_{IHE}$ | 3.0 | | | V | 1,9,11 |
| Supply | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |

## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | | | +500 | μA | 4 |
| Output Leakage | $I_{LO}$ | | | +500 | μA | |
| Output Current @ 2.4V | $I_{OH}$ | −1 | | | mA | |
| Output Current @ 0.4V | $I_{OL}$ | | | +2 | mA | |
| $\overline{\text{RST}}$ Input Resistance | $Z_{RST}$ | 10 | | 40 | KΩ | |
| D/Q Input Resistance | $Z_{DQ}$ | 10 | | 40 | KΩ | |
| CLK Input Resistance | $Z_{CLK}$ | 10 | | 40 | KΩ | |
| $\overline{\text{RST}}$ Current @3.0V | $I_{RST}$ | | | 2 | mA | 6,9,13 |
| Active Current | $I_{CC1}$ | | | 6 | mA | 6 |
| Standby Current | $I_{CC2}$ | | | 1 | mA | 6 |

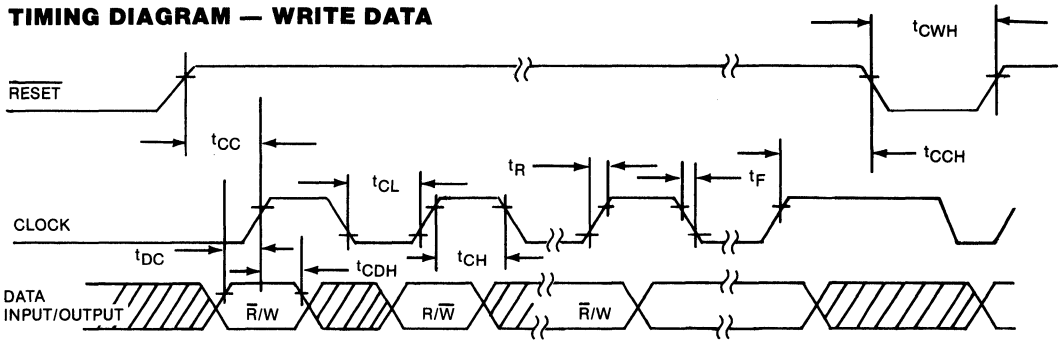
**CAPACITANCE** ($t_A = 25°C$)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

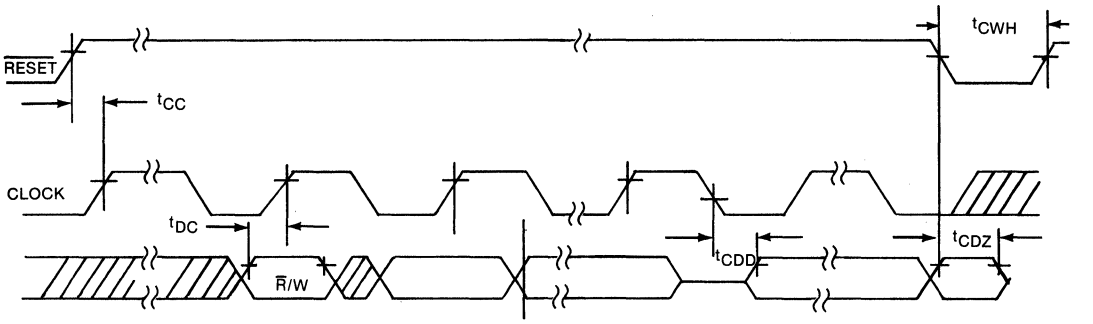
**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Data To CLK Setup | $t_{DC}$ | 35 | | | ns | 2,7 |
| CLK to Data Hold | $t_{CDH}$ | 40 | | | ns | 2,7 |
| CLK to Data Delay | $t_{CDD}$ | | | 100 | ns | 2,3,5,7 |
| CLK Low Time | $t_{CL}$ | 125 | | | ns | 2,7 |
| CLK High Time | $t_{CH}$ | 125 | | | ns | 2,7 |
| CLK Frequency | $f_{CLK}$ | D.C. | | 4.0 | MHZ | 2,7 |
| CLK Rise & Fall | $t_R$, $t_F$ | | | 500 | ns | 2,7 |
| $\overline{RST}$ To CLK Set Up | $t_{CC}$ | 1 | | | us | 2, 7 |
| CLK To $\overline{RST}$ Hold | $t_{CCH}$ | 40 | | | ns | 2, 7 |
| $\overline{RST}$ Inactive Time | $t_{CWH}$ | 125 | | | ns | 2,7,14 |
| $\overline{RST}$ To I/O High Z | $t_{CDZ}$ | | | 50 | ns | 2, 7 |

**TIMING DIAGRAM — WRITE DATA**



## TIMING DIAGRAM — READ DATA



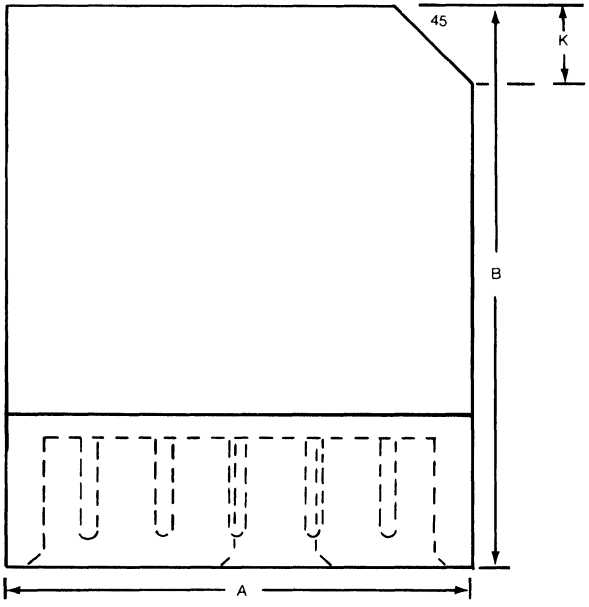

1. All voltages are referenced to GND.
2. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8V$ and 10 ns maximum rise and fall time.
3. Measured at $V_{OH} = 2.4$ volts and $V_{OL} = 0.4$ volts.
4. For CLK, D/Q, and $\overline{RST}$
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at $V_{IH}$ of $\overline{RST} \geq 3.0V$ when $\overline{RST}$ supplies power.
8. Logic 1 maximum is $V_{CC} + 0.3$ volts if the $V_{CC}$ pin supplies power and $\overline{RST} + 0.3$ volts if the $\overline{RST}$ pin supplies power.
9. Applies to $\overline{RST}$ when $V_{CC} < 3.0$ V.
10. Input levels apply to CLK, DQ, and $\overline{RST}$ while $V_{CC}$ is within nominal limits. When $V_{CC}$ is not connected to the key, then $\overline{RST}$ input reverts to $V_{IHE}$.
11. $\overline{RST}$ Logic 1 maximum is $V_{CC} + 0.3$ volts if the $V_{CC}$ pin supplies power and 5.5 volts maximum if $\overline{RST}$ supplies power.
12. Each DS1204U is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.
13. Average A.C. $\overline{RST}$ current can be determined using the following formula:

    $$I_{TOTAL} = 2 + I_{LOAD\ D.C.} + (4 \times 10^{-3})(C_L + 140)\ f$$

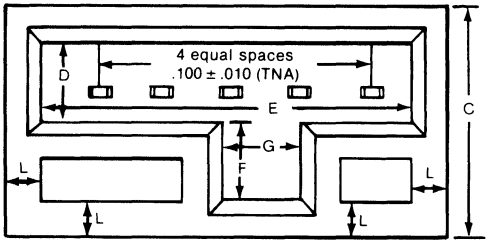
    $I_{TOTAL}$ and $I_{LOAD}$ are in mA; $C_L$ is in pF; f is in MHZ.

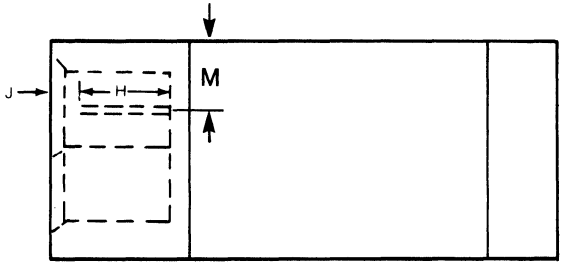
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHZ gives an $I_{TOTAL}$ of 5 MA.
14. When $\overline{RST}$ is supplying power $t_{CWH}$ must be increased to 100 ms.

# *Electronic Key*
# *DS1204U*




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .610 | .625 |
| B | .745 | .755 |
| C | .310 | .325 |
| D | .100 | .110 |
| E | .515 | .525 |
| F | .100 | .110 |
| G | .100 | .110 |
| H | .110 | .130 |
| J | .030 | .050 |
| K | .045 | .055 |
| L | .045 | .055 |
| M | .100 | .110 |

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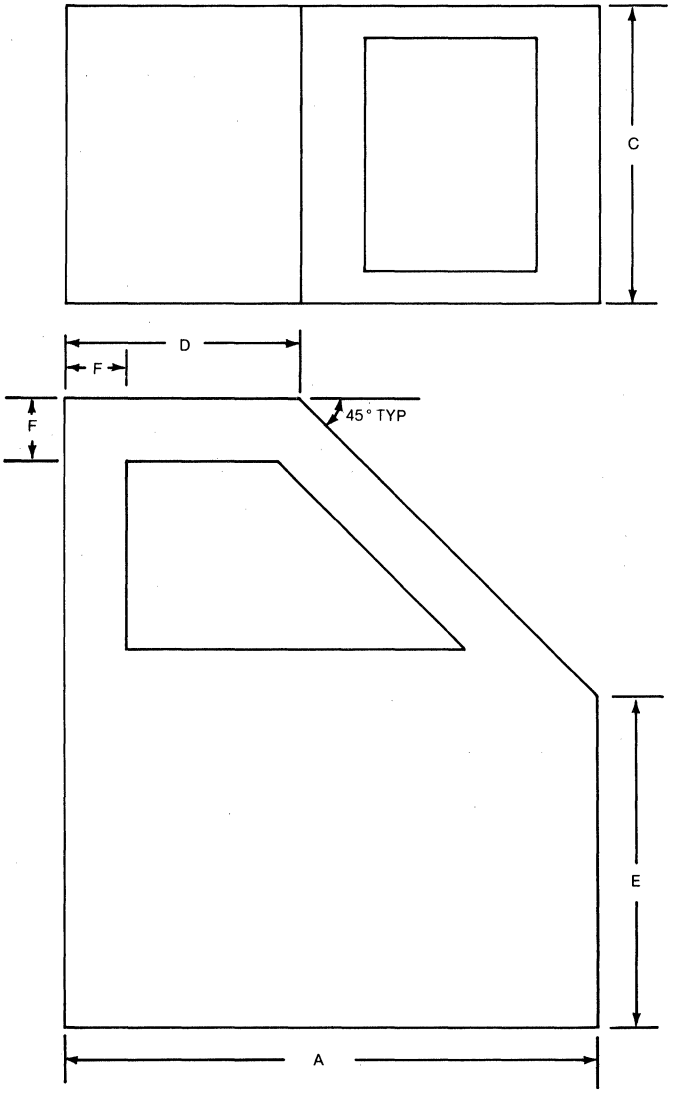
# *Key/Tag Holder*
# *DS9090*




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .670 | .690 |
| B | .790 | .810 |
| C | .370 | .390 |
| D | .290 | .310 |
| E | .410 | .430 |
| F | .070 | .090 |

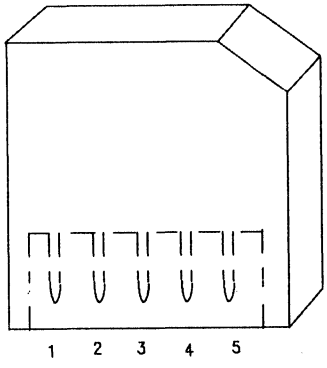
**Dallas Semiconductor**
***TIMEKEY***

**PRELIMINARY**
***DS1207***

## FEATURES

- Cannot be deciphered by reverse engineering
- Time allotment from 1 day to 512 days for trial periods, rentals, and leasing
- Partitioned memory thwarts pirating
- User insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64 bit reprogrammable memory
- Unreadable 64 bit match code virtually prevents discovery by exhaustive search with over $10^{19}$ possibilities
- Random data generation on incorrect match codes obscures real accesses
- 384 bits of secure read/write memory creates additional barriers against hackers by permitting data changes as often as needed
- Rapid erasure of identification security match code, and secure read/write memory can occur if tampering is detected
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

## PIN CONNECTIONS




## PIN NAMES

pin 1- no connection
pin 2- $\overline{RST}$ reset
pin 3- DQ data input/output
pin 4- CLK clock
pin 5- GND ground

## DESCRIPTION

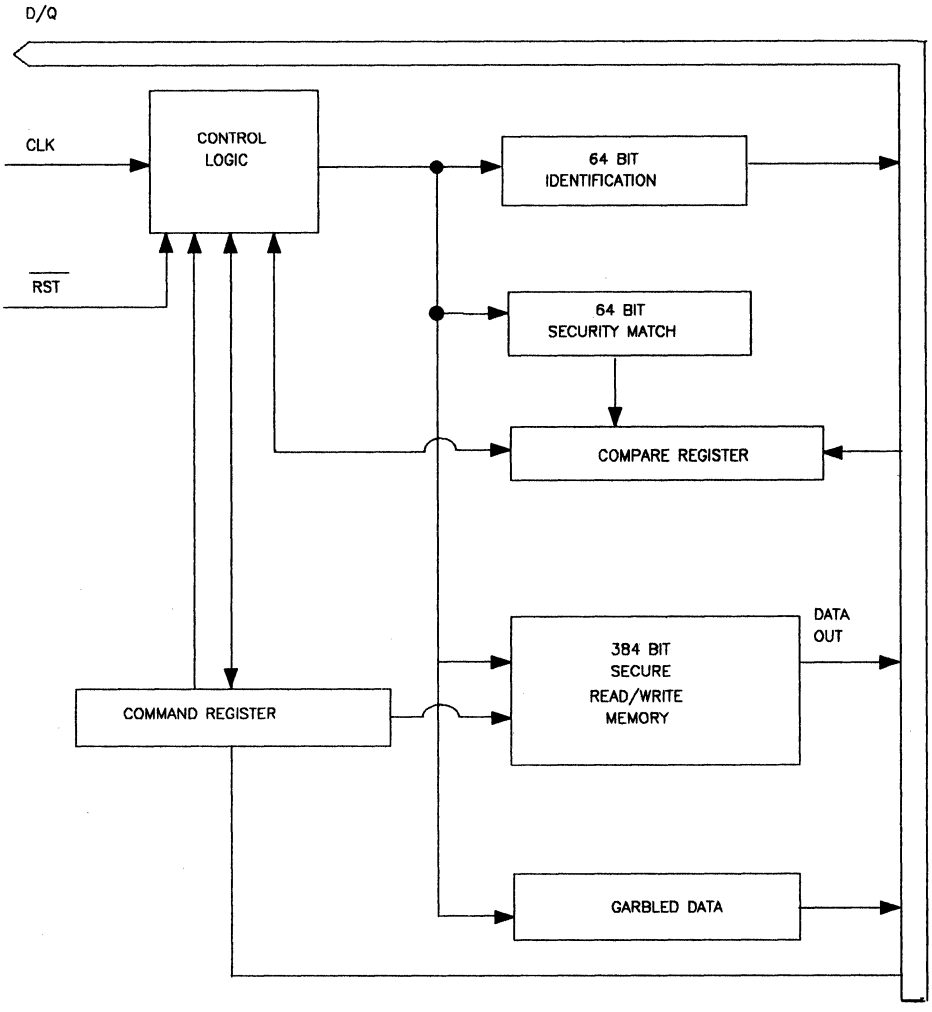
The DS1207 TimeKey is a miniature security system which stores 64 bits of user definable identification code and a 64 bit security match code which protects 384 bits of read/write nonvolatile memory. The 64 bit identification code, and the security match code, are programmed into the TimeKey via a special program mode operation. After programming, the TimeKey follows a special procedure with a serial format to retreive or update data. The TimeKey is set to expire in from one day to 512 days or infinity, as specified by the customer. The TimeKey starts its countdown from the first access by the end user.

Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfer with only three signals: CLOCK, $\overline{\text{RESET}}$, and DATA INPUT/OUTPUT. Low pin count and a guided entry for a mating receptacle overcomes mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user insertable.

**OPERATION - NORMAL MODE**

The TimeKey has two modes of operation: The normal mode and the program mode. The normal mode of operation provides the functions of reading and writing the 384 bit secure memory. The block diagram (Figure 1) illustrates the main elements of the TimeKey when used in the normal mode. To initiate data transfer with the TimeKey $\overline{\text{RST}}$ is taken high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact bit pattern which defines normal operations with a function code of read or write. If one of these patterns is not matched, communication is ignored. If the command register is loaded properly, communications are allowed to continue. Data is clocked out of the TimeKey on the high to low transition of the clock. If the pattern matched in the command register calls for a normal read or write, the next 64 cycles following the command word are read and data is clocked out of the identification memory. The next 64 write cycles are written to the compare register (Figure 2). These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, if normal read mode is selected, random garbled data is output for the next 384 cycles. If a normal write cycle is selected and a match is not achieved, the TimeKey will ignore any additional information. However, when a security match is achieved, access is permitted to the 384 bit secure memory.

**FIGURE 1**
**BLOCK DIAGRAM-NORMAL MODE**



## OPERATION - PROGRAM MODE

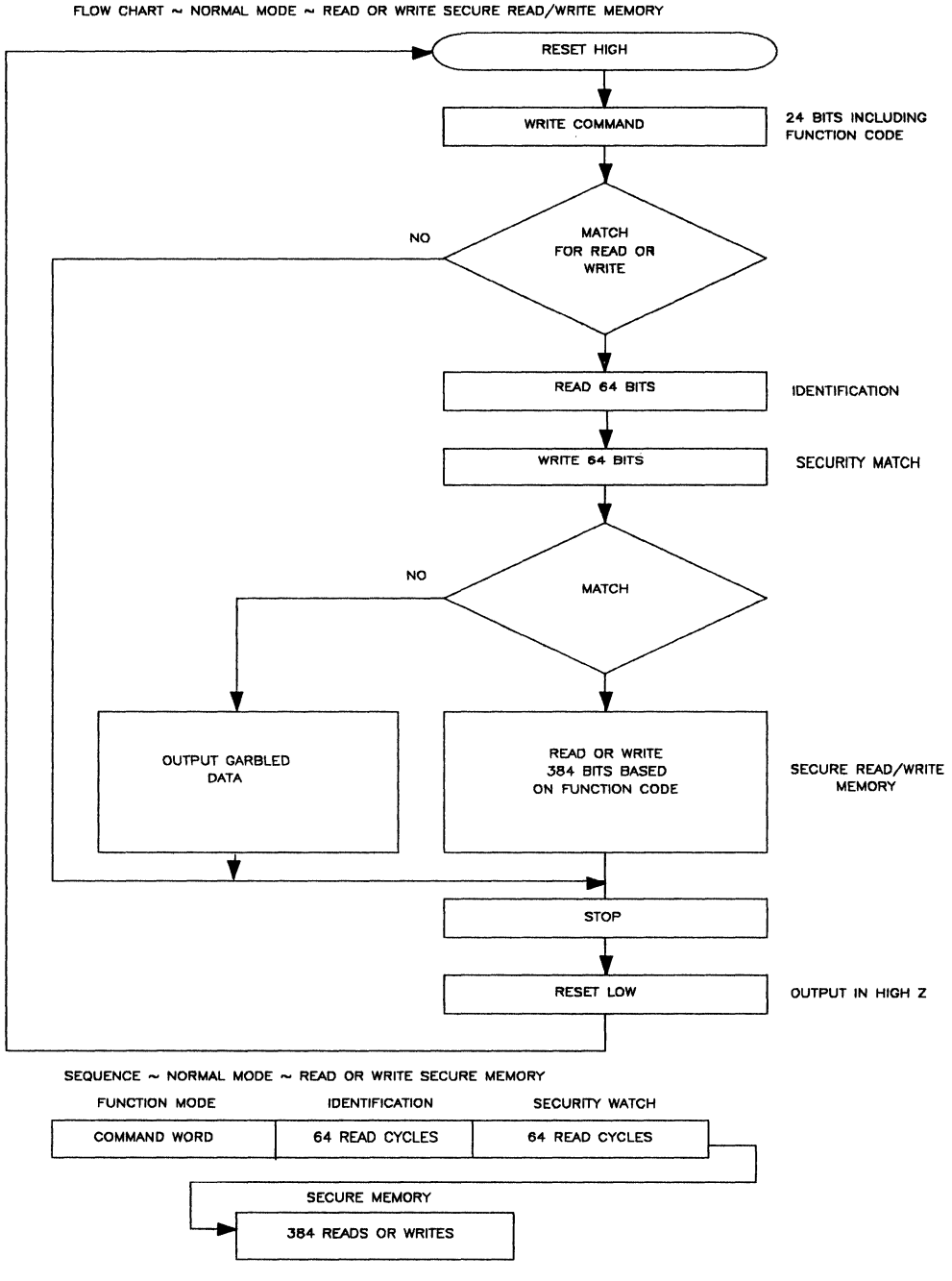
The program mode of operation provides the functions of programming the identification and security match memory and setting and reading the amount of time the TimeKey can be used. The block diagram of Figure 3 illustrates the main elements of the TimeKey when used in the program mode. To initiate the program mode, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact bit pattern which defines program mode for the identification and security match bits or program mode for setting and reading the amount of time for which the TimeKey can be used. If an exact match for one of the seven function codes of the program mode is not found, the remainder of the program mode is ignored. When the command register is properly loaded for programming the identification and security match bits, the next 128 bits which follow are written to the identification and security match memory (Figure 4). When this mode of operation is invoked, all memory contents are erased.

## SETTING AND READING TIME REMAINING

There are six functions of the program mode which are used to set or read the amount of time in which the TimeKey will allow full operation. To initiate any of the six functions of the program mode used for setting and reading time remaining, $\overline{RST}$ is driven high and 24 bits are loaded into the command register on each low to high transition of the CLK input. If the command register is properly loaded with the function code for reading the 20 bit day clock counter, the next 20 bits will be output (LSB first) as a binary count of the amount of time elapsed in the current day (see Figure 5). The time can be calculated by dividing this count reading by $2^{20}$ (20 bits is equal to 1,048,576 counts). One minus this result is the fraction of a day remaining. The 20 bit day clock counter is driven by an internal oscillator which has a period of 82.4 ms. If the command register is properly loaded with the function code for reading the 9 bit number of days counter, the next 9 bits will be output (LSB first) as a binary count of the days remaining (see Figure 6). This count is decremented each time the day clock counter rolls over to zero. When the number of days remaining counter rolls through zero, normal and program mode write cycles are inhibited. If program mode read cycle to the number of days counter is attempted, the nine bits will be returned as all ones.

If the command register is properly loaded with the function code for writing the nine bit number of days counter, the next nine bits will be input (LSB first) as a binary count of the desired number of days in which the TimeKey will be fully functional (see Figure 7). The number of days counter can be changed by writing over an entered value as often as required until the lock command is entered. The lock command is given when the command register is properly loaded with the function code for locking up the number of days counter. The lock command consists of the 24 bit command word only (see Figure 8). Once the lock command is given, all future write cycles to the number of days register is ignored. After the correct value has been written and locked into the number of days counter, the DS1207 will start counting the time from the entered value to zero after the first access to the TimeKey is executed provided the arm oscillator bit is set. The arm oscillator bit is set when the command register has been properly loaded with the function code for arming the oscillator. The arm oscillator command consists of the 24 bit command word only (see Figure 9). One other command is also available for use in setting and reading time remaining. A stop oscillator command is given when the command register is properly loaded with the function code for stopping the oscillator. The stop oscillator command consists of the 24 bit command word only (see Figure 10). This command will only execute prior

## FIGURE 2


FLOW CHART ~ NORMAL MODE ~ READ OR WRITE SECURE READ/WRITE MEMORY
RESET HIGH
WRITE COMMAND
24 BITS INCLUDING FUNCTION CODE
NO
MATCH FOR READ OR WRITE
READ 64 BITS
IDENTIFICATION
WRITE 64 BITS
SECURITY MATCH
NO
MATCH
OUTPUT GARBLED DATA
READ OR WRITE 384 BITS BASED ON FUNCTION CODE
SECURE READ/WRITE MEMORY
STOP
RESET LOW
OUTPUT IN HIGH Z
SEQUENCE ~ NORMAL MODE ~ READ OR WRITE SECURE MEMORY
FUNCTION MODE
IDENTIFICATION
SECURITY WATCH
COMMAND WORD
64 READ CYCLES
64 READ CYCLES
SECURE MEMORY
384 READS OR WRITES

## FIGURE 3

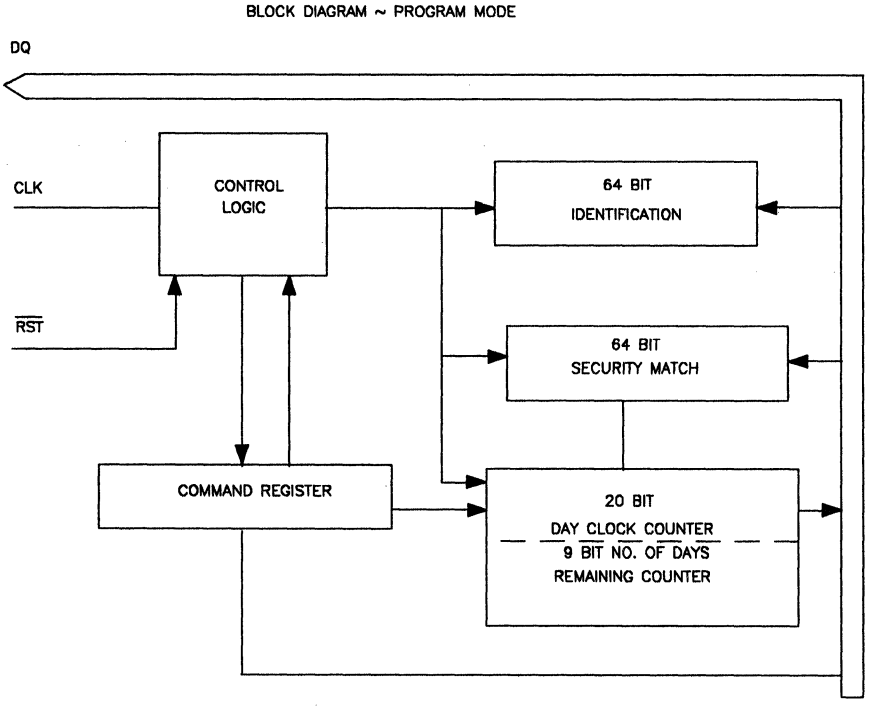
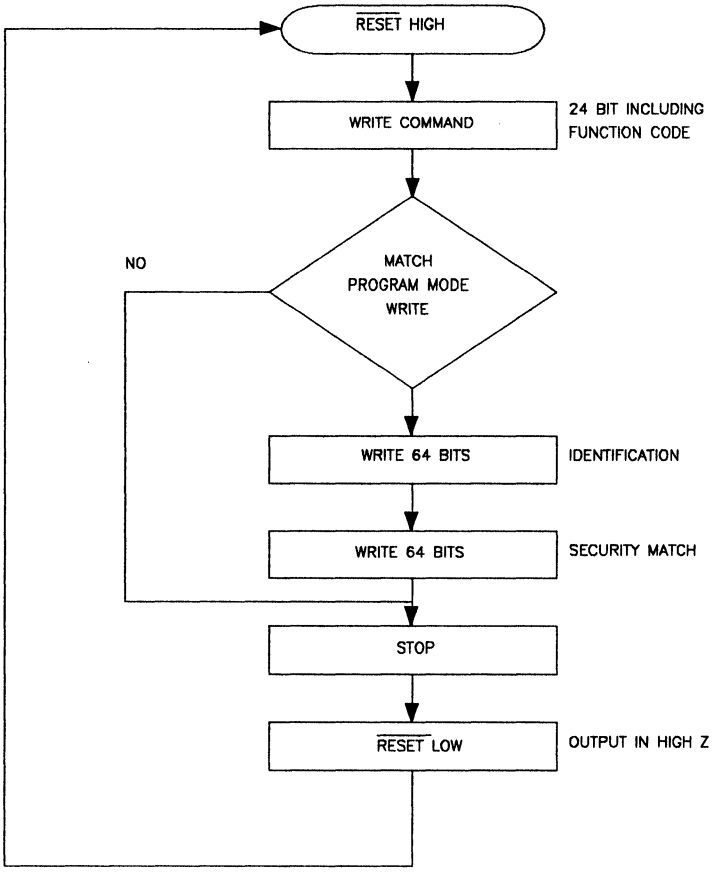

BLOCK DIAGRAM ~ PROGRAM MODE
DQ
CLK
CONTROL LOGIC
64 BIT IDENTIFICATION
RST
64 BIT SECURITY MATCH
COMMAND REGISTER
20 BIT DAY CLOCK COUNTER
9 BIT NO. OF DAYS REMAINING COUNTER

**FIGURE 4**

PROGRAM MODE ~ PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY

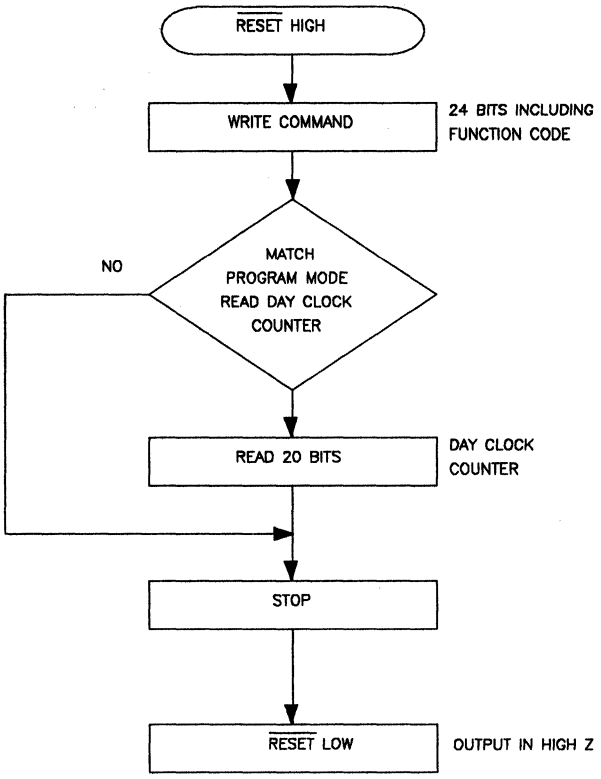



SEQUENCE–PROGRAM MODE–PROGRAM IDENTIFICATION AND SECURITY MATCH BITS

| FUNCTION MODE | IDENTIFICATION | SECURITY WATCH |
|---|---|---|
| COMMAND WORD | 64 WRITE CYCLES | 64 WRITE CYCLES |

**FIGURE 5**

FLOW CHART – PROGRAM MODE ~ READING THE 20 BIT DAY CLOCK COUNTER




SEQUENCE – PROGRAM MODE – READING THE 20 BIT DAY CLOCK COUNTER

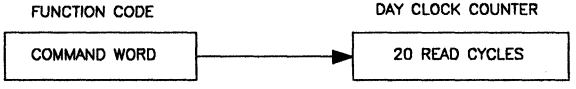
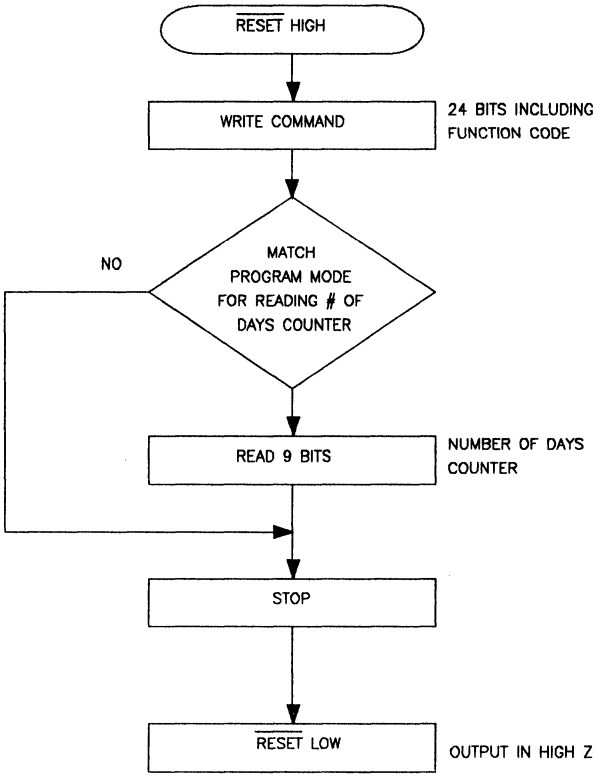
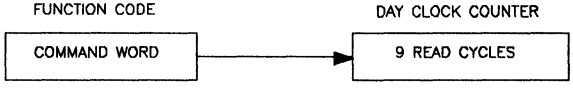


**FIGURE 6**

FLOW CHART – PROGRAM ~ READING THE 9 BIT NUMBER OF DAYS COUNTER

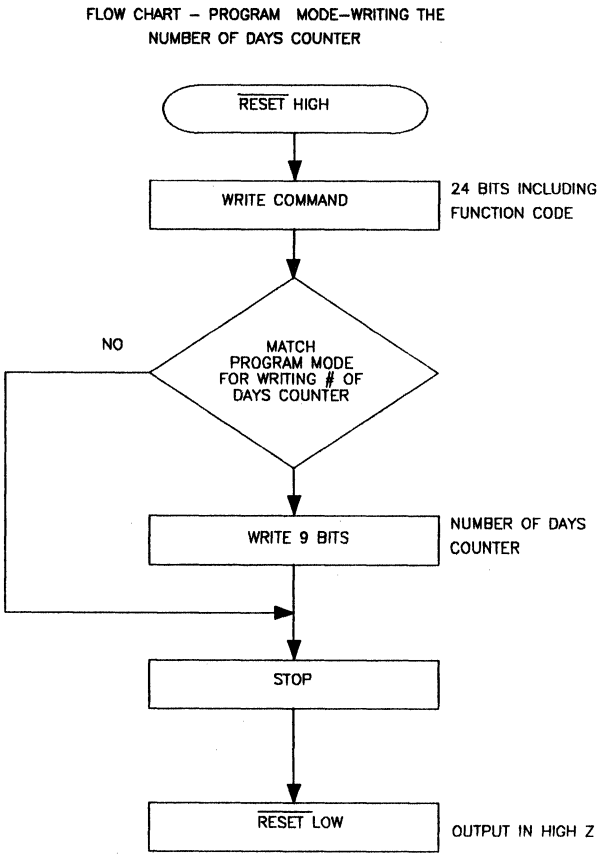


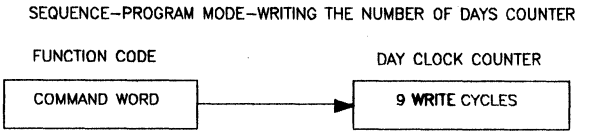

SEQUENCE – PROGRAM MODE – READING THE 9 BIT NUMBER OF DAYS COUNTER



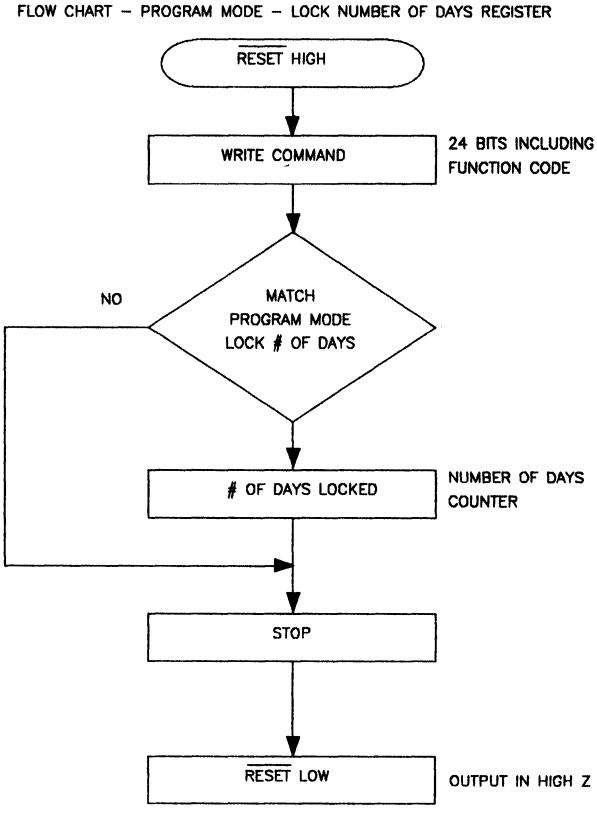

9

**FIGURE 7**


FLOW CHART – PROGRAM MODE–WRITING THE NUMBER OF DAYS COUNTER
RESET HIGH
WRITE COMMAND
24 BITS INCLUDING FUNCTION CODE
NO
MATCH PROGRAM MODE FOR WRITING # OF DAYS COUNTER
WRITE 9 BITS
NUMBER OF DAYS COUNTER
STOP
RESET LOW
OUTPUT IN HIGH Z


SEQUENCE–PROGRAM MODE–WRITING THE NUMBER OF DAYS COUNTER
FUNCTION CODE
DAY CLOCK COUNTER
COMMAND WORD
9 WRITE CYCLES

## FIGURE 8

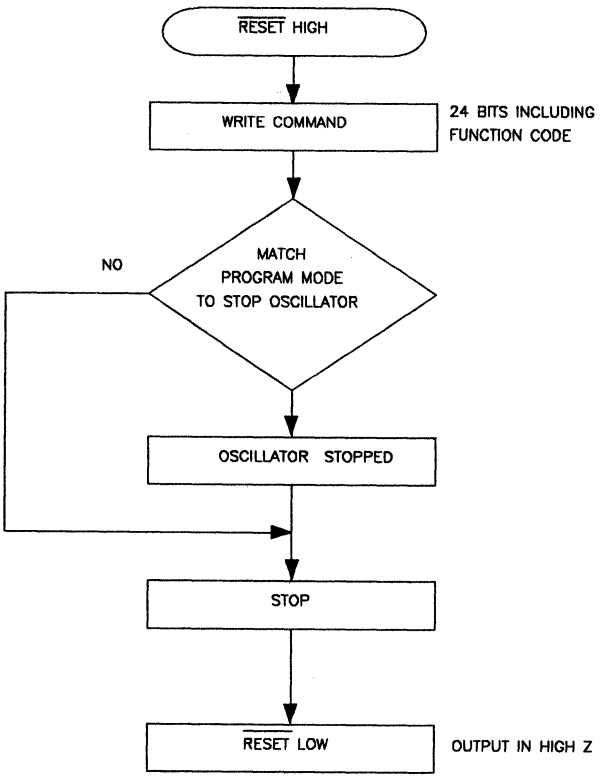

FLOW CHART – PROGRAM MODE – LOCK NUMBER OF DAYS REGISTER
RESET HIGH
WRITE COMMAND
24 BITS INCLUDING FUNCTION CODE
NO
MATCH PROGRAM MODE LOCK # OF DAYS
# OF DAYS LOCKED
NUMBER OF DAYS COUNTER
STOP
RESET LOW
OUTPUT IN HIGH Z

to issuing a lock command. After the lock command is issued, stop oscillator commands are ignored.

A sequence for properly setting the expiration time of the DS1207 is as follows (see Figure 11): First program the identification and security match bits to the desired value. Also use normal mode operation to write the appropriate secure data. Second, write the number of days remaining register to the desired value. This number can be immediately verified by reading the number of days remaining. Next, arm the oscillator by writing the appropriate command. Then do a normal mode read. This action will start the internal oscillator. Now read the 20 bit day clock counter several times to verify that the oscillator is running. After oscillator activity has been verified, issue the stop oscillator command. Now the lock command should be issued followed by the arm oscillator command. The TimeKey will start to count down to expiration on the next access. The oscillator verification portion of this sequence is not required and can be deleted when speed in setting time remaining is important.

**FIGURE 9**

FLOW CHART – PROGRAM MODE–ARM OSCILLATOR



## FIGURE 10

FLOW CHART – PROGRAM MODE – STOP OSCILLATOR

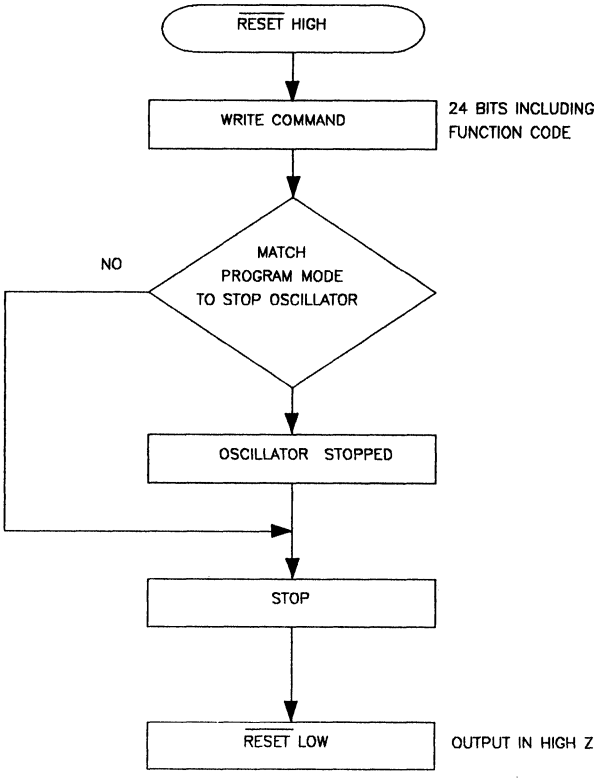


**FIGURE 11**
**SETTING THE TIME UNTIL EXPIRATION OF THE DS1207**

| | |
|---|---|
| Step 1 | Program identification memory<br>Program security match bits<br>Write normal mode secure data |
| Step 2 | Program write the number of days remaining<br>Program read the number of days remaining for verification |
| Step 3 | Issue arm oscillator command |
| Step 4 | Do a read of any kind |
| Step 5 | Program read the day clock counter several times (verify that the oscillator is running) |
| Step 6 | Issue the stop oscillator command |
| Step 7 | Issue the lock command |
| Step 8 | Issue arm oscillator command<br>(time of expiration will start on first access) |

Note: Step 3 through Step 6 are not required. Dallas Semiconductor tests and guarantees that the oscillator will start without verification

## COMMAND WORD

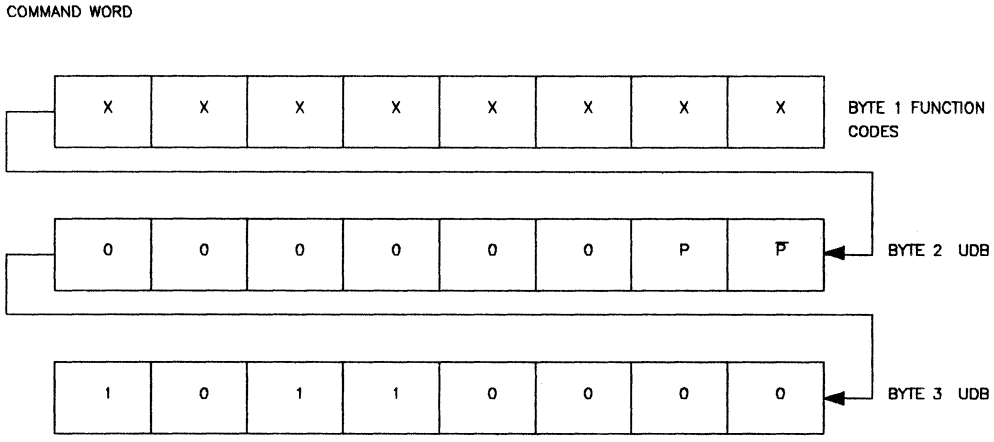
Each data transfer for normal and program mode begins with a three byte command word as shown in Figure 12. As defined, the first byte of the command word specifies the function code. There are eight function codes which are acceptable (Figure 13). If any one of the bits of the first byte of the command word fails to meet one of the exact patterns for function codes, the data transfer will be aborted.

The first two bits of the second byte of the command word specify whether the data transfer to follow is program or normal mode. The bit pattern for program mode is 0 in bit 0 and 1 in bit 1. The bit pattern for normal mode is a 1 in bit 0 and a 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause transfer to abort. The program mode can be invoked with one of seven function codes; program identification and security match, read the 20 bit day clock counter, read the number of days count, write the number of days count, lock number of days count, arm oscillator, and stop oscillator.

The remaining 6 bits of byte 2 and the first 4 bits of byte 3 must be written to logic 0 or data transfer will abort. Under special contract with Dallas Semiconductor, these bits may be defined by the user as any bit pattern other than that specified by Dallas Semiconductor as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last four bits of byte 3 of the command word must be written 1011 or data transfer will abort. Table 1 is a summary of the command words in hexidecimal as they apply to all function codes for both program mode and normal mode.

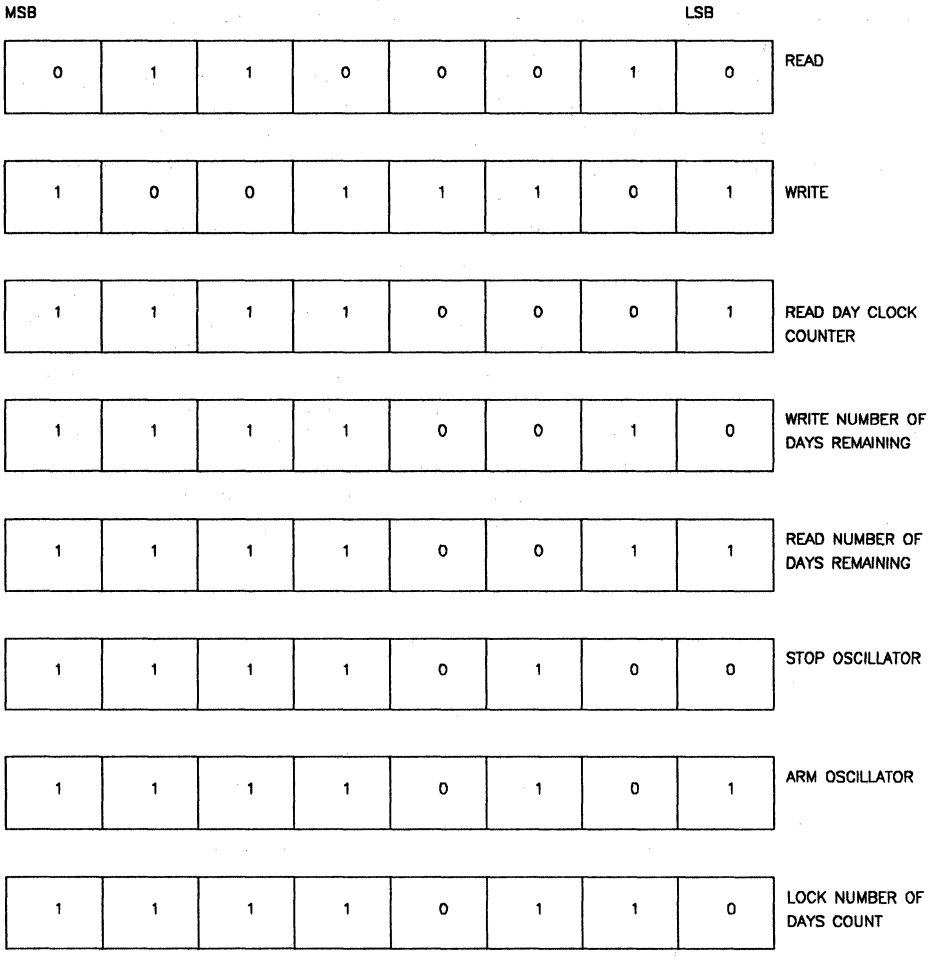
Note: Contact Dallas Semiconductor Sales Office for special command word code assignment which makes possible an exclusive blank TimeKey.

## FIGURE 12




USER DEFINABLE BITS (UDB) ~ CONTACT DALLAS SEMICONDUCTOR FOR SPECIAL COMMAND WORD CODE ASSIGNMENT WHICH MAKES AN EXCLUSIVE BLANK KEY.

## FIGURE 13: FUNCTION CODES - FIRST BYTE OF COMMAND WORD



## RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The reset input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the $\overline{RST}$ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for $\overline{RST}$ of 2 MA @ 3.0 volts is required. Third, the $\overline{RST}$ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates if the $\overline{RST}$ pin is low and the DQ pin goes to a high impedance state. Data transfer is illustrated in Figure 14 for normal mode and Figure 15 for program mode.

## TIMEKEY CONNECTIONS

The TimeKey is designed to be plugged into a standard 5 pin 0.1 inch center SIP receptacle. A guide is provided to prevent the TimeKey from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the TimeKey pins can be determined to insure connection integrity before data transfer begins. CLK, $\overline{RST}$, and Data Input/Output all have 20K OHM pull down resistors to ground which can be sensed by a reading device.

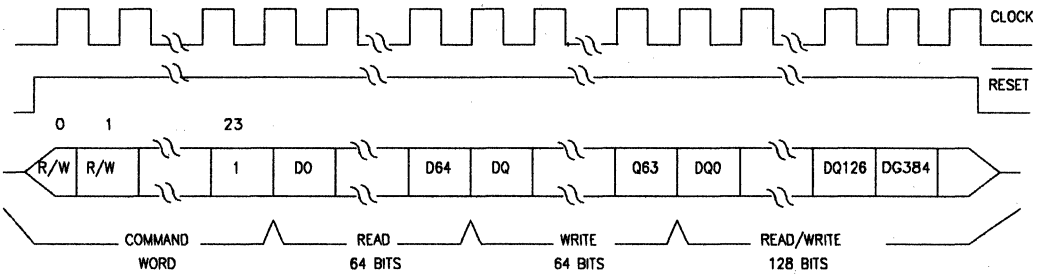
TABLE 1 IS A SUMMARY OF THE COMMAND WORDS IN HEXIDECIMAL AS THEY APPLY TO ALL FUNCTION CODES FOR BOTH PROGRAM MODE AND NORMAL MODE

TABLE 1

| MODE | FUNCTION | COMMAND WORD | | |
|---|---|---|---|---|
| NORMAL | READ | B0 | 01 | 62 |
| NORMAL | WRITE | B0 | 01 | 9D |
| PROGRAM | WRITE | B0 | 02 | 9D |
| PROGRAM | READ DAY CLOCK COUNTER | B0 | 02 | F1 |
| PROGRAM | READ DAYS REMAINING | B0 | 02 | F3 |
| PROGRAM | WRITE DAYS REMAINING | B0 | 02 | F2 |
| PROGRAM | ARM OSCILLATOR | B0 | 02 | F5 |
| PROGRAM | LOCK NUMBER OF DAYS COUNT | B0 | 02 | F6 |
| PROGRAM | STOP OSCILLATOR | B0 | 02 | F4 |

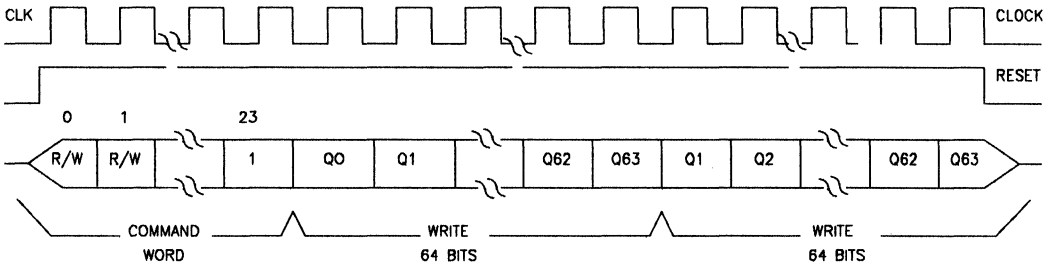
## FIGURE 14

DATA TRANSFER – NORMAL MODE READ OR WRITE SECURE READ/WRITE MEMORY

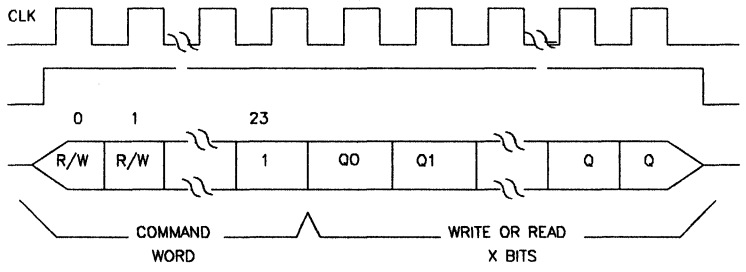



## FIGURE 15

DAT TRANSFER – PROGRAM MODE ~ PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY




DATA TRANSFER – PROGRAM MODE




NOTE: THE NUMBER OF BITS WHICH FOLLOW THE COMMAND WORD WILL BE EITHER 0, 9, OR 20 BITS BASED ON THE FUNCTION CODE.

**ABSOLUTE MAXIMUM RATINGS***

| | |
|---|---|
| VOLTAGE ON ANY PIN RELATIVE TO GROUND | --1.0V to +7V |
| OPERATING TEMPERATURE | 0°C to 70° |
| STORAGE TEMPERATURE | - -40°C to +70°C |

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0 °C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | | V | 1 |
| Logic 0 | $V_{IL}$ | -0.3 | | +0.8 | V | 1 |
| $\overline{\text{RESET}}$ Logic 1 | $V_{IHE}$ | 3.0 | | | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $\overline{\text{RST}}$= 3.0V)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | N OTES |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | | | +500 | uA | 4 |
| Output Leakage | $I_{LO}$ | | | +500 | uA | |
| Output Current @ 2.4V | $I_{OH}$ | -1 | | | mA | |
| Output Current @ 0.4V | $I_{OL}$ | | | +2 | mA | |
| $\overline{\text{RST}}$ Input Resistance | $Z_{RST}$ | 10 | | 40 | KΩ | |
| D/Q Input Resistance | $Z_{DQ}$ | 10 | | 40 | KΩ | |
| CLK Input Resistance | $Z_{CLK}$ | 10 | | 40 | KΩ | |
| $\overline{\text{RST}}$ Current 3.0V | $I_{RST}$ | | | 2 | mA | 6,9 |

## CAPACITANCE

(tA = 25°)

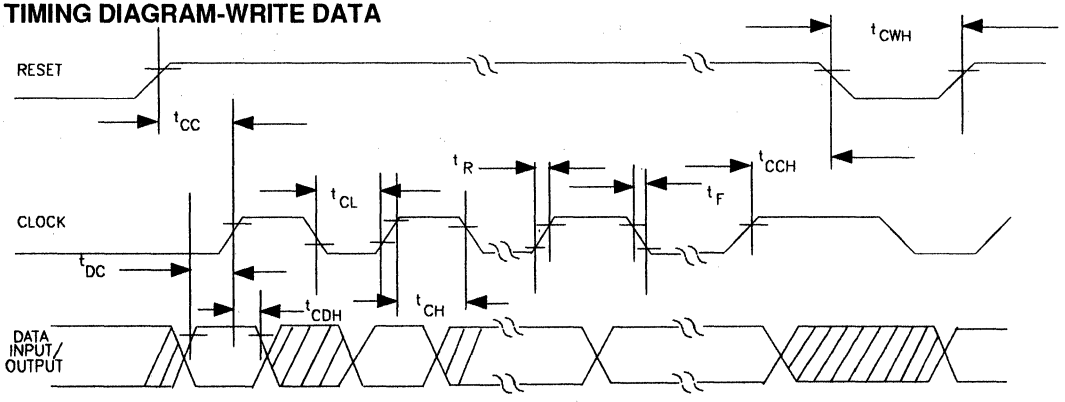
| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance CIN | $C_N$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

## A.C. ELECTRICAL CHARACTERISTICS

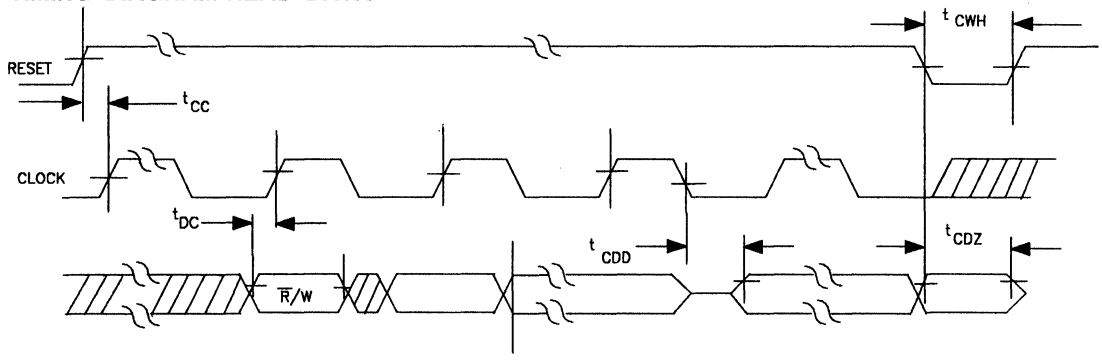
(0°C to 70 °C)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Data To CLK Setup | $t_{DC}$ | 50 | | | ns | 2,7 |
| CLK to Data Hold | $t_{CDH}$ | 70 | | | ns | 2,7 |
| CLK to Data Delay | $t_{CDD}$ | | | 200 | ns | 2,3,5,7 |
| CLK low Time | $t_{CL}$ | 250 | | | ns | 2,7 |
| CLK High Time | $t_{CH}$ | 250 | | | ns | 2,7 |
| CLK Frequency | $f_{CLK}$ | D.C. | | 2.0 | MHZ | 2,7 |
| CLK Rise & Fall | $t_R, t_F$ | | | 500 | ns | 2,7 |
| $\overline{\text{RST}}$ To CLK Set Up | $t_{CC}$ | 1 | | | us | 2,7 |
| CLK To $\overline{\text{RST}}$ Hold | $t_{CCH}$ | 60 | | | ns | 2,7 |
| $\overline{\text{RST}}$ Inactive Time | $t_{CWH}$ | 10 | | | ms | 2,7 |
| $\overline{\text{RST}}$ To I/O High Z | $t_{CDZ}$ | | | 70 | ns | 2,7 |

## TIMING DIAGRAM-WRITE DATA



## TIMING DIAGRAM-READ DATA



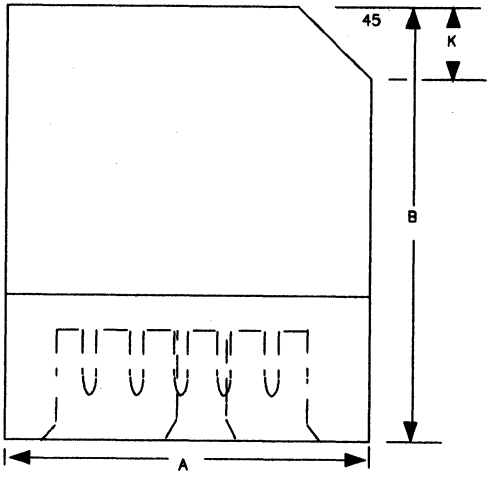

1. All voltages are referenced to GND.
2. Measured at $V_{IH}$ = 2.0 or $V_{IL}$ = .8V and 10 ns maximum rise and fall time.
3. Measured at $V_{OH}$ = 2.4 volts and $V_{OL}$ = 0.4 volts.
4. For CLK, D/Q, and $\overline{RST}$
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at $V_{IH}$ of $\overline{RST}$ greater than or equal to 3.0V.
8. Each DS1207 is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.
9. Average A.C. $\overline{RST}$ current can be determined using the following formula:

$$I_{TOTAL} = 2 + I_{LOAD} \text{ D.C.} + (4 \times 10^{-3})(C_L + 280)f$$

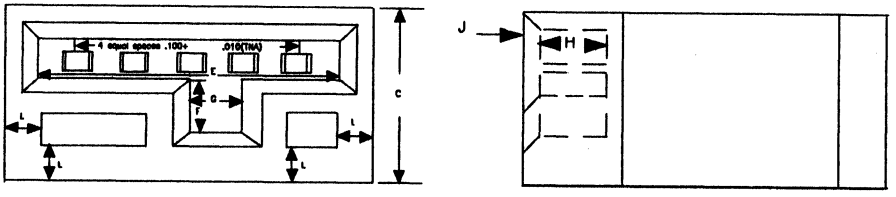
$I_{TOTAL}$ and $I_{LOAD}$ are in mA; CL is in pF; f is in MHZ.

Applying the above formula, a load capacitance of 50 pF running at a frequency of 2.0 MHZ gives an $I_{TOTAL}$ of 1.6 MA.

# DS1207
# TIMEKEY




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .610 | .625 |
| B | .745 | .755 |
| C | .310 | .325 |
| D | .100 | .110 |
| E | .515 | .525 |
| F | .100 | .110 |
| G | .100 | .110 |
| H | .110 | .130 |
| I | .030 | .050 |
| K | .045 | ..055 |
| J | .045 | ..055 |



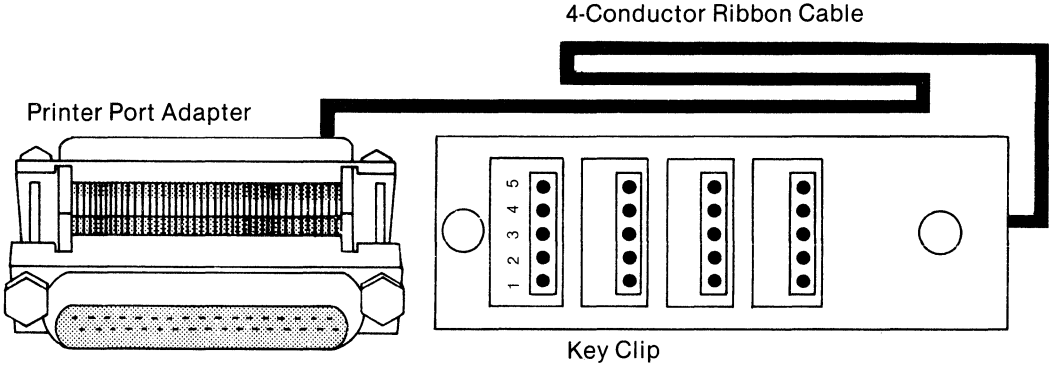
# Dallas Semiconductor
## *Printer Port KeyRing* — *DS1253*

### FEATURES

- Low cost add on fixture for Electronic Keys, Tags, and TimeKeys
- Connects directly to IBM PC Parallel Printer Port without affecting printer operation
- Plug-in installation
- Key, Tag, and TimeKey communications are totally controlled by software
- Up to four Keys, Tags, and TimeKeys may be resident at one time
- Normal computer operation is unaffected
- Applications include software security, identification, personalization, and portable memory

### PIN CONNECTIONS AND DEFINITIONS

Pin 1 - $V_{CC}$ +5 Volts
Pin 2 - $\overline{RST}$ - $\overline{RESET}$
Pin 3 - D/Q - Data In/Out
Pin 4 - CLK - CLOCK
Pin 5 - GND Ground




### DESCRIPTION

The DS1253 KeyRing adapts low pin count electronic Keys (DS1204U), Tags (DS1201S), and TimeKeys (DS1207) to the IBM PC Parallel Printer Port without affecting the printer or computer operations. The KeyRing is installed onto any IBM PC or IBM PC-compatible printer by simply disconnecting the printer, installing the printer port adapter, and reconnecting the printer to back connector on the printer port adapter. The emanating 4-conductor ribbon cable can be routed such that the key clip can be attached to the computer cabinet in a convenient location with the adhesive provided. Up to 4 keys and/or tags can be inserted into the key clip at the same time. Communications with keys and tags occur under software control of the parallel printer port. The three control signals ($\overline{RESET}$, Clock, and Data In/Out) for Tags, Keys and TimeKeys are generated by consecutive I/O instructions which control the parallel printer port.

## OPERATION

Keys, Tags, and TimeKeys have defined signal patterns which are required for communications. The signals $\overline{RST}$, CLK and DQ must be software controlled to duplicate the behavior as defined in the respective data sheet for Tags, Keys and TimeKeys. Each signal is a function of a specific output or I/O line of the printer port. Pin 4 on the 25-Pin D Connector Parallel Printer Port is called Data Out 2 (D2). This signal is used to provide $\overline{RST}$ for the KeyRing and must be kept at a high level when communicating with Tags, Keys, and TimeKeys. When $\overline{RST}$ is driven low all communication to Tags, Keys, and TimeKeys is terminated. The $\overline{RST}$ signal is also used as a source of power for Tags, Keys and TimeKeys (see respective data sheets). Pin 5 on the 25-Pin D Connector Parallel Printer Port is called Data Out 3 (D3). This signal is used to provide CLK for the KeyRing. The CLK signal times data into and out of Keys, Tags, and TimeKeys. Because the CLK signal provides timing, the relationship between both level and transition from one level to another is critical with respect to data. In fact, data must be valid when a CLK transition occurs which inputs data to Keys, Tags, and TimeKeys and a CLK transition is also required to output data. Because signals change state at the same time on the Parallel Printer Port, set up and hold times do not normally exist. To compensate, two output cycles are required for each transition of the CLK signal. The first cycle is used to establish the correct CLK level. A second cycle will then guarantee that data is valid as the clock changes levels. Pin 17 on the 25-Pin D Connector Parallel Printer Port is called SLCTIN and is used as the data I/O signal for Keys, Tags, and TimeKeys. This is a bi-directional signal. Data is output from this port signal during write cycles, and input from Keys, Tags, and TimeKeys during read cycles. Pin 18 on the 25-Pin D Connector is ground (GND) and supplies ground for the KeyRing.

When communicating with Keys, Tags and TimeKeys, the Parallel Printer Port is being used as a general purpose I/O port. As such, software defines the appropriate commands. In order to avoid having the printer interpret Key, Tag, and TimeKey communications as print commands, the strobe signal (Pin 1 on the D Connector Parallel Printer Port) must be kept low when the data stream is not directed to the printer. The printer must also be kept on when using the KeyRing to avoid clamping the Parallel Printer Port signals.

## INSTALLATION

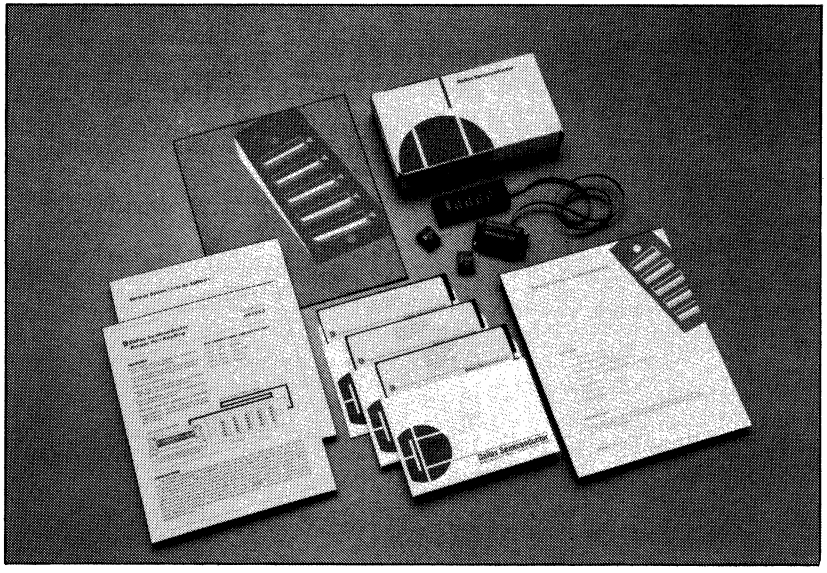
The Parallel Printer Port KeyRing is installed by first removing the printer cable. If the Parallel Printer Port is not used, this step is not necessary. The Parallel Printer Port cable is removed by loosening the top and bottom mounting screws and unplugging the cable. The next step is to install the printer port adapter by loosening the top and bottom mounting screws on the adaptor and plugging the male side of the adapter into the female printer port. The top and bottom screws should then be tightened to avoid accidental disconnection. Next, plug the printer cable into the female end of the printer port adapter. The top and bottom mounting screws of the printer cable should then be tightened to avoid accidental disconnection. After the printer port adapter has been secured, the key clip can be attached to a convenient spot on the computer cabinet with the supplied adhesive.

## SOFTWARE

Upon request Dallas Semiconductor can make available demonstration software with source listing for the IBM PC or IBM PC-compatible computers.

# Dallas Semiconductor
## *Software Authorization Kit*

## *DS1253K*





**FEATURES**

- DS1204U Electronic Key
- DS1253 KeyRing with 4-Position Clip
- Demonstration Software for IBM PC on Floppy Disk
- Documentation
- Source Listing
- Data Sheets

**INSTRUCTION**

Before using the DS1253K, install disk 1 in the default disk drive and type, "TYPE DSC.MEM". This file is the instruction manual which should be read carefully before proceeding.

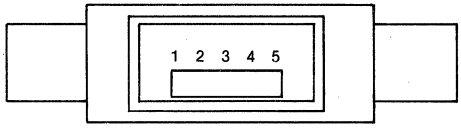
# Dallas Semiconductor
## *Printer Port KeyRing* — *DS1255*

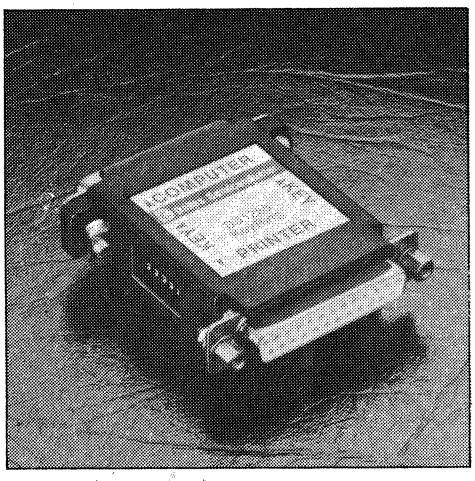
### FEATURES

- Self-contained add-on fixture for user insertable Electronic Keys, Tags and TimeKeys
- Connects to the parallel printer port of an IBM XT, AT, RT or compatible computer
- End user installation
- Two Keys may be resident at one time
- Key, Tag and TimeKey communications are totally controlled by software
- Normal computer/printer operation is unaffected
- Applications include software authorization, computer site identification, and access control

### PIN CONNECTIONS AND DEFINITIONS

Pin 1 - $V_{CC}$ - +5 Volts
Pin 2 - $\overline{RST}$ - $\overline{RESET}$
Pin 3 - D/Q Data In/Out
Pin 4 - CLK - CLOCK
Pin 5 - GND - GROUND



### DESCRIPTION

The DS1255 KeyRing adapts low pin Electronic Keys DS1204U, Tags DS1201S, and TimeKeys DS1207 to the IBM PC parallel printer port without affecting the printer or computer operations. The KeyRing is installed onto any IBM PC or IBM PC-compatible printer by simply disconnecting the printer, installing the KeyRing, and reconnecting the printer to the back connector on the KeyRing. Two Keys or Tags can be resident at the same time. Communication with Keys is established by software controlled sequences to the parallel printer port. The three control signals ($\overline{Reset}$, Clock and Data In/Out) for Keys are generated by the parallel port signals by executing an assembly or DOS level I/O driver.

## OPERATION

Keys, Tags and TimeKeys have defined signal patterns which are required for communications. The signals $\overline{RST}$, CLK, and DQ must be software controlled to duplicate the behavior as defined in the respective data sheet for Keys. Each signal is a function of a specific output or I/O line of the printer port (Figure 1). Pin 4 on the 25-pin D Connector parallel printer port is called Data Out 2 (D2). This signal is used to provide $\overline{RST}$ for the KeyRing and must be kept at high level when communicating with Keys. When $\overline{RST}$ is driven low, all communication to Keys is terminated. The $\overline{RST}$ signal is also used as a source of power for Keys (see respective data sheets). Pin 5 on the 25-pin D Connector parallel printer port is called Data Out 3 (D3). This signal is used to provide CLK for the KeyRing. The CLK signal times data into and out of Keys. Because the CLK signal provides timing, the relationship between both level and transition is critical with respect to data. In fact, data must be valid when a CLK transition occurs which inputs data to Keys and a CLK transition is also required to output data. Because signals change state at the same time on the parallel printer port, setup and hold times do not normally exist. To compensate, two output cycles are required for each transition of the CLK signal. The first cycle is used to establish the correct CLK level. A second cycle will guarantee that data is valid as the CLK changes levels. Pin 17 on the 25-pin D Connector parallel printer port is called SLCTIN and is used as the data I/O signal for Keys. This is a bi-directional signal. Data is output from this port signal during write cycles and input from Keys during read cycles. Pin 18 on the 25-pin D Connector is ground (GND) and supplies ground for the KeyRing.

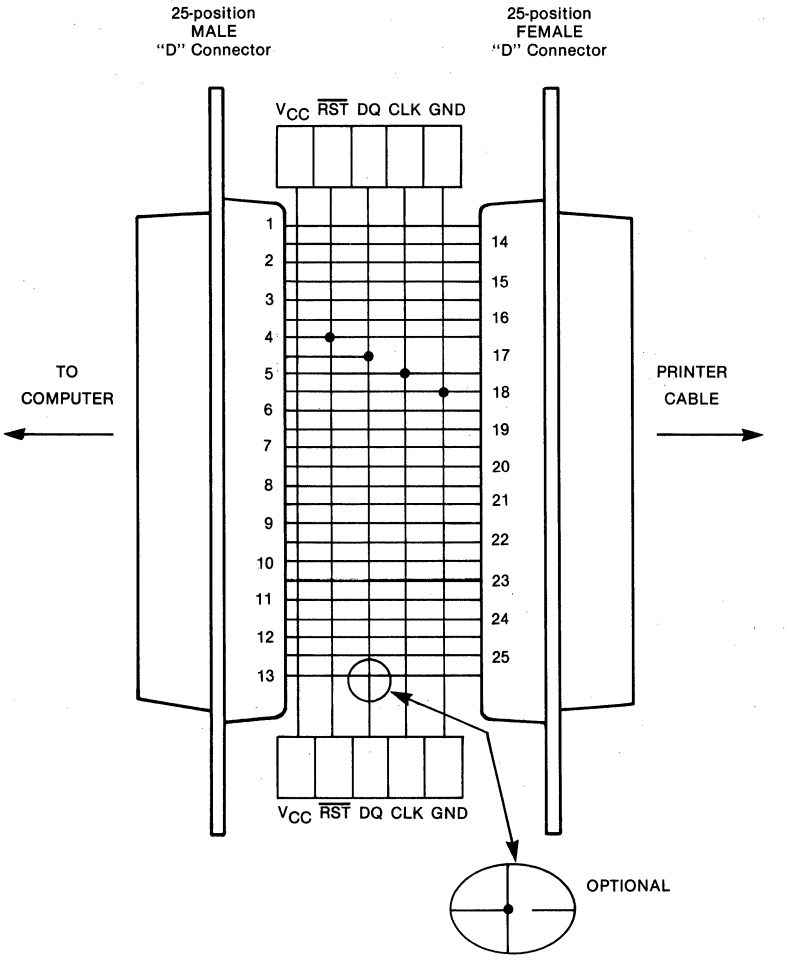
When communicating with Keys, the parallel printer port is being used as a general purpose I/O port. As such, software defines the appropriate commands. In order to avoid having the printer interpret Key communications as print commands, the strobe signal (Pin 1 on the D Connector parallel printer port) must be kept low when the data stream is not directed to the printer. The printer must also be kept on when using the KeyRing to avoid clamping the parallel printer port signals.

## INSTALLATION

The Parallel Printer Port KeyRing is installed by first removing the printer cable. If the parallel printer port is not being used, this step is not necessary. The printer cable is removed by loosening the top and bottom retaining screws and unplugging the cable. The next step is to install the KeyRing by plugging the male side of the KeyRing into the female printer port. The top and bottom retaining screws should be tightened to avoid accidental disconnection. Next, plug the printer cable into the female end of the KeyRing. The top and bottom retaining screws should then be tightened to avoid accidental disconnection. After the printer cable is secure, a Key,Tag,or TimeKey can be plugged into either of two receptacles and the computer and KeyRing are now ready for use.

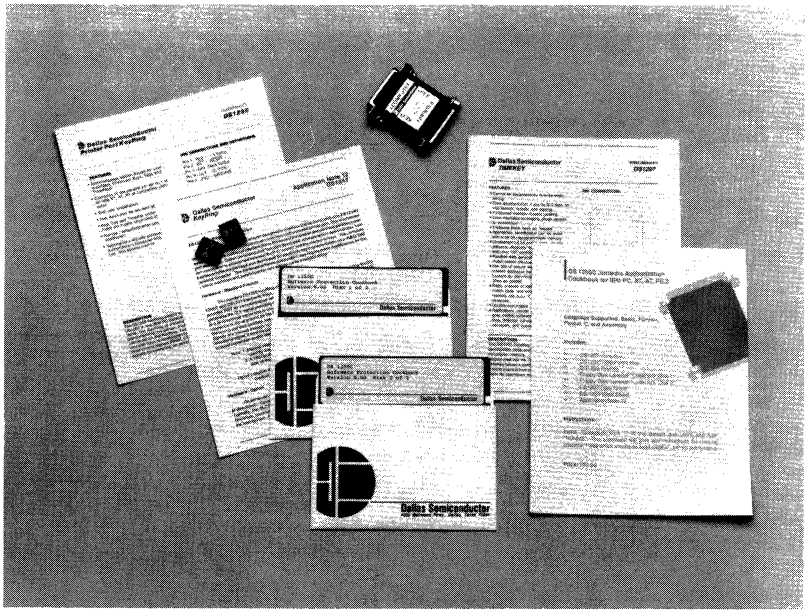
**SOFTWARE**
Upon request, Dallas Semiconductor can make available demonstration software with source listing for assemble language and high level language for the IBM PC, XT, AT or compatible computers.

Figure 1




**NOTE:** An optional feature is available from Dallas Semiconductor which connects Pins 13 and 17 together. This feature allows operation with some nonstandard IBM P.C. Printer Ports. See Application Note 12.

# Dallas Semiconductor
## *Software Authorization Cookbook* — *DS1255C*





**FEATURES**

- DS1207 TimeKey
- DS1204U Electronic Key
- DS1255 KeyRing
- Floppy Disk Labeled "Cookbook Disk 1"
- Floppy Disk Labeled "Cookbook Disk 2"
- DS1207 Data Sheet
- DS1255 Data Sheet
- Application Note 12

**INSTRUCTION**

Install "Cookbook Disk 1" in the default drive and type "RUN ME". This command will give you instructions for printing document files which should be read carefully before proceeding.

**LANGUAGES SUPPORTED: BASIC, FORTRAN, PASCAL, C, ASSEMBLY**

# Integrated Battery Backup

**Dallas Semiconductor**

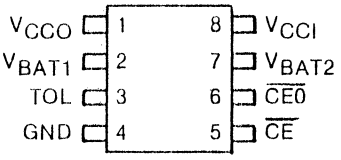
# *Nonvolatile Controller*

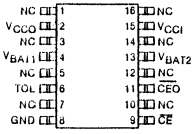
# *DS1210—8-Pin DIP*
# *DS1210S—16-Pin SOIC*

## FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Unconditionally write protects when $V_{CC}$ is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin mini-DIP
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Optional 5% or 10% power fail detection
- Low forward voltage drop on the $V_{CC}$ Switch
- Optional 16-pin SOIC surface mount package

## PIN CONNECTIONS




## PIN NAMES

| | |
|---|---|
| $V_{CCO}$ | - RAM Supply |
| $V_{BAT1}$ | - + Battery 1 |
| TOL | - Power Supply Tolerance |
| GND | - Ground |
| $\overline{CE}$ | - Chip Enable Input |
| $\overline{CEO}$ | - Chip Enable Output |
| $V_{BAT2}$ | - + Battery 2 |
| $V_{CCI}$ | - + Supply |
| NC | - No Connect |

## DESCRIPTION

The DS1210 is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8 pin mini-DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 nonvolatile controller chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

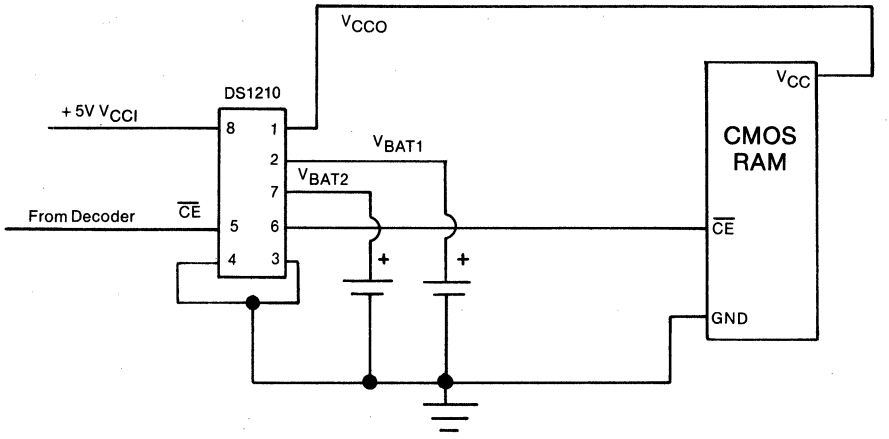
## OPERATION

The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply ($V_{CCI}$) depending on which is greater. This switch has a voltage drop of less than 0.3V. The second function which the nonvolatile controller provides is power fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power fail and inhibits chip enable ($\overline{CEO}$). The third function of write protection is accomplished by holding the $\overline{CEO}$ output signal to within 0.2 volts of the $V_{CCI}$ or battery supply. If $\overline{CE}$ input is low at the time power fail detection occurs, the $\overline{CEO}$ output is kept in its present state until $\overline{CE}$ is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 is connected to $V_{CCO}$, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CE}$ with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to insure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. In applications where battery reliability is not a concern only one battery need be connected to $BAT_1$ or $BAT_2$ pin, with the other battery pin grounded.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor based system. Section A shows the connections necessary to write protect the RAM when $V_{CC}$ is less than 4.75 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when $V_{CC}$ is less than 4.75 volts and to delay its restart on power up to prevent spurious writes.

**FIGURE 1**

**SECTION A — BATTERY BACKUP**

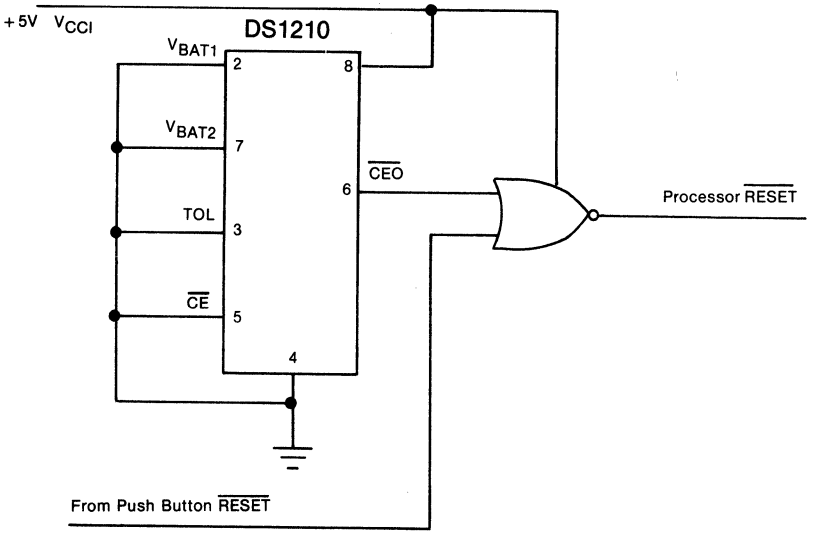



**BATTERY BACKUP CURRENT DRAIN EXAMPLE**

CONSUMPTION

| | |
|---|---|
| DS1210 $I_{BAT}$ | - 100 nA |
| RAM $I_{CC02}$ | - 10 uA |
| Total Drain | -10.1$u$A |

**SECTION B — PROCESSOR RESET**



**ABSOLUTE MAXIMUM RATINGS***

Voltage on Any Pin Relative to Ground −0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| PIN 3 = GND Supply Voltage | $V_{CCI}$ | 4.75 | 5.0 | 5.5 | V | 1 |
| PIN 3 = $V_{CCO}$ Supply Voltage | $V_{CCI}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Logic 1 Input | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1 |
| Logic 0 Input | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| Battery Input | $V_{BAT1}$ $V_{BAT2}$ | 2.0 | | 4.0 | V | 1,2 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CCI}$ = 4.75V to 5.5V, PIN 3 = GND) ($V_{CCI}$ = 4.5 to 5.5V, PIN 3 = $V_{CCO}$)

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CCI}$ | | | 5 | mA | 3 |
| Supply Voltage | $V_{CCO}$ | $V_{CC}-0.2$ | | | V | 1 |
| Supply Current | $I_{CCO1}$ | | | 80 | mA | 4 |
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | uA | |
| Output Leakage | $I_{LO}$ | −1.0 | | +1.0 | uA | |
| $\overline{CE0}$ Output @2.4V | $I_{OH}$ | −1.0 | | | mA | 5 |
| $\overline{CE0}$ Output @ 0.4V | $I_{OL}$ | | | 4.0 | mA | 5 |
| $V_{CC}$ Trip Point (TOL = GND) | $V_{CCTP}$ | 4.50 | 4.62 | 4.74 | V | 1 |
| $V_{CC}$ Trip Point (TOL = $V_{CC}$) | $V_{CCTP}$ | 4.25 | 4.37 | 4.49 | V | 1 |

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(0 °C to 70 °C, $V_{CCI} < V_{BAT}$)

| | | | | | |
|---|---|---|---|---|---|
| $\overline{CE0}$ Output | $V_{OHL}$ | $V_{BAT} - 0.2$ | | V | |
| $V_{BAT1}$ or $V_{BAT2}$ Battery Current | $I_{BAT}$ | | 100 | nA | 2,3 |
| Battery Backup Curent @$V_{CCO} = V_{BAT} - 0.3V$ | $I_{CC02}$ | | 50 | uA | 6,7 |

**CAPACITANCE** ($t_A = 25$ °C)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

**A.C. ELECTRICAL CHARACTERISTICS**

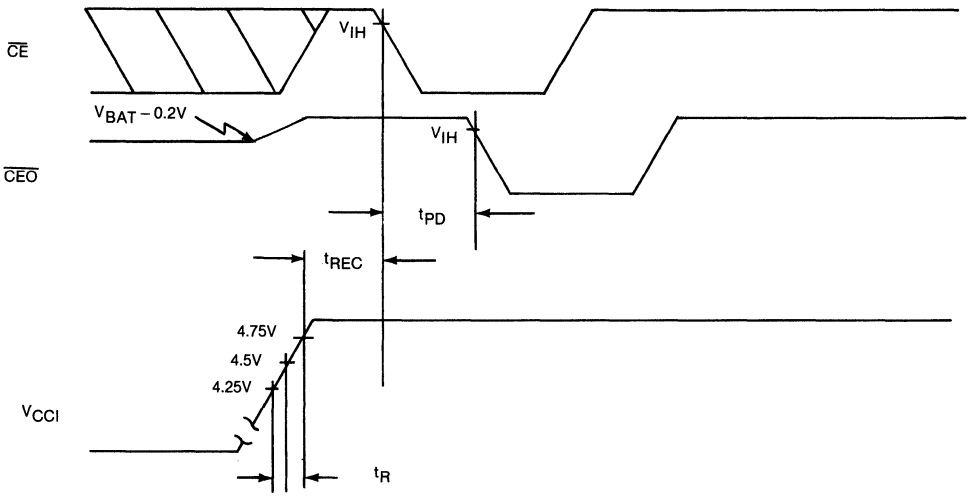
(0 °C - 70 °C, $V_{CCI} = 4.75$ - 5.5V, PIN 3 = GND)
($V_{CCI} = 4.5$ to 5.5V, PIN 3 = $V_{CCO}$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ Propagation Delay | $t_{PD}$ | 5 | 10 | 20 | ns | 5 |
| $\overline{CE}$ High to Power Fail | $t_{PF}$ | | | 0 | ns | |

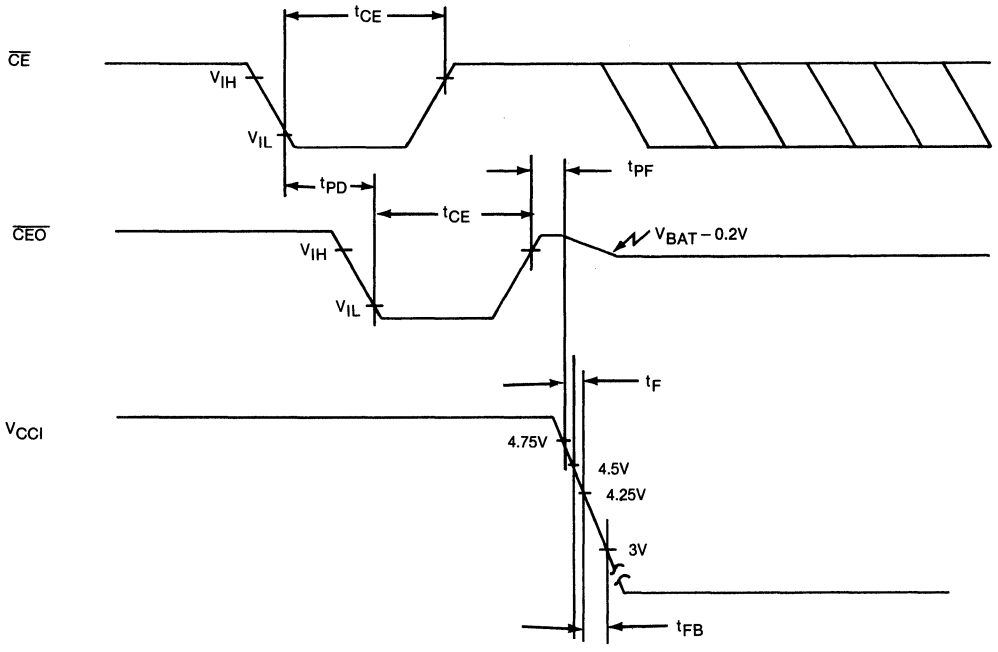
(0 °C to 70 °C, $V_{CCI} < 4.75$V, PIN 3 = GND)
($V_{CCI} < 4.5$V, PIN 3 = $V_{CCO}$)

| | | | | | | |
|---|---|---|---|---|---|---|
| Recovery at Power Up | $t_{REC}$ | 2 | 80 | 125 | ms | |
| $V_{CC}$ Slew Rate Power Down | $t_F$ | 300 | | | us | |
| $V_{CC}$ Slew Rate Power Down | $t_{FB}$ | 10 | | | us | |
| $V_{CC}$ Slew Rate Power Up | $t_R$ | 0 | | | us | |
| $\overline{CE}$ Pulse Width | $t_{CE}$ | | | 1.5 | us | 7,8 |

## TIMING DIAGRAM — POWER UP

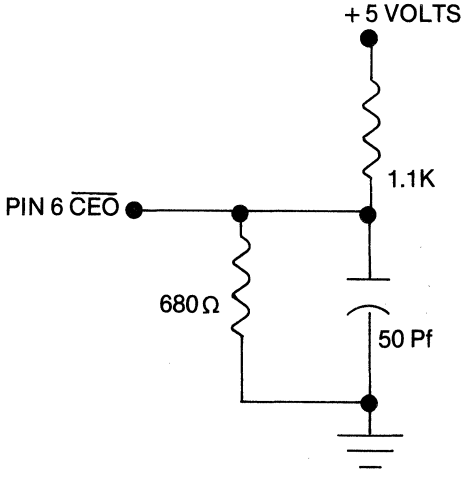



## TIMING DIAGRAM — POWER DOWN



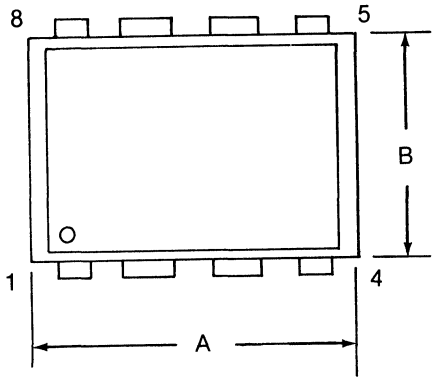
**NOTES:**

1. All voltages are referenced to ground.
2. Only one battery input is required.
3. Measured with $V_{CCO}$ and $\overline{CE0}$ open.
4. $I_{CC01}$ is the maximum average load which the DS1210 can supply to the memories.
5. Measured with a load as shown in Figure 2.
6. $I_{CC02}$ is the maximum average load current which the DS1210 can supply to the memories in the battery backup mode.
7. $t_{CE}$ max must be met to insure data integrity on power loss.
8. Chip Enable Output $\overline{CEO}$ can only sustain leakage current in the battery backup mode.

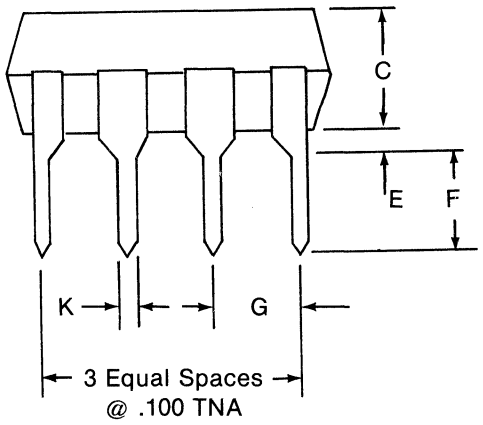


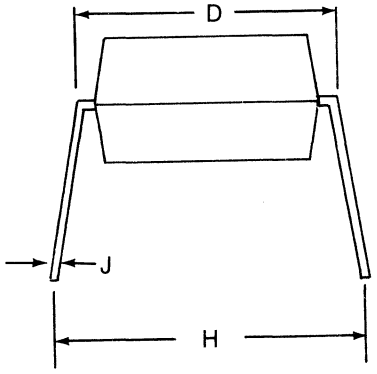

**OUTPUT LOAD**
Figure 2

# DS1210
## Nonvolatile Controller




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .360 | .400 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |

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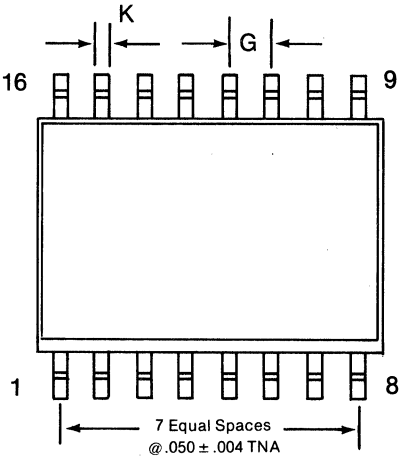
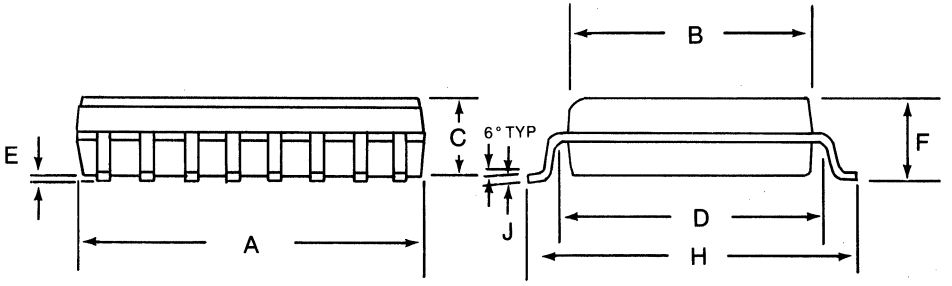
# DS1210S
# Nonvolatile Controller




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



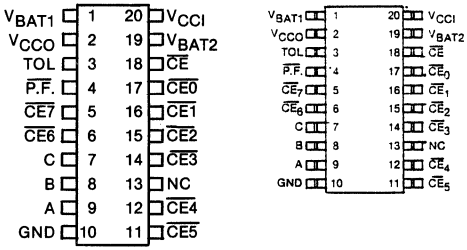
# Dallas Semiconductor

## *Nonvolatile Controller/Decoder DS1211—20-Pin DIP DS1211S—20-Pin SOIC*

### FEATURES

- Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when $V_{CC}$ is out of tolerance
- Automatically switches to battery when power fail occurs
- 3 to 8 decoder provides control for up to 8 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 20-pin SOIC surface mount package

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| A, B, C | - Address Inputs |
| $\overline{CE}$ | - Chip Enable Input |
| $\overline{CE0}$-$\overline{CE7}$ | - Chip Enable Outputs |
| GND | - Ground |
| $V_{BAT1}$ | - + Battery 1 |
| $V_{BAT2}$ | - + Battery 2 |
| TOL | - Power Supply Tolerance |
| $V_{CCI}$ | - +5V Supply |
| $V_{CCO}$ | - RAM Supply |
| $\overline{P.F.}$ | - Power Fail |
| N.C. | - No Connection |

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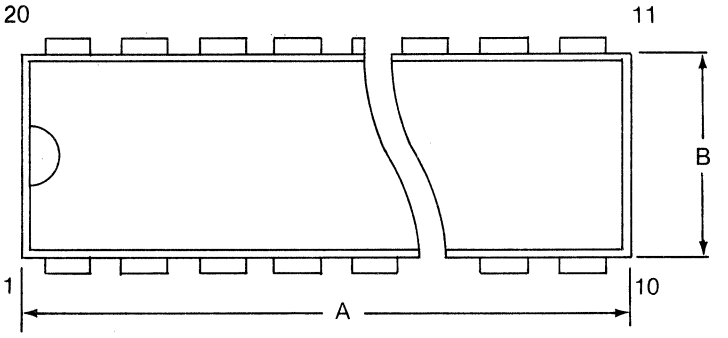
### DESCRIPTION

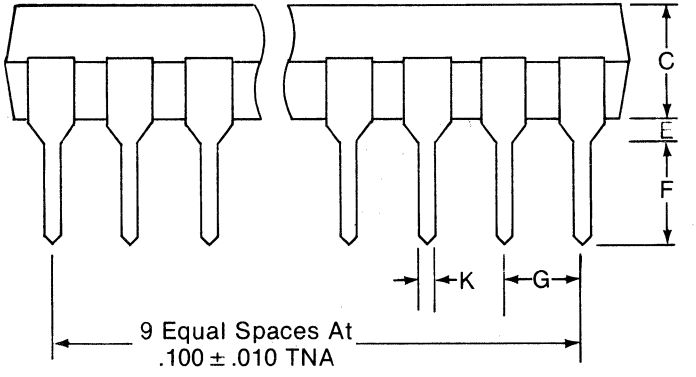
The DS1211 is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption.

By combining the DS1211 nonvolatile controller/decoder chip and lithium batteries, ten years of nonvolatile RAM operation can be achieved for up to eight CMOS memories.

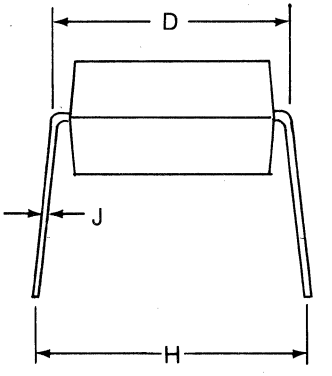
See the data sheet for the DS1212 for electrical specifications and operation.

# DS1211
# Nonvolatile Controller

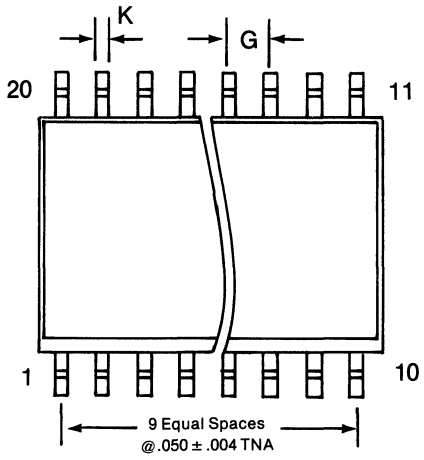


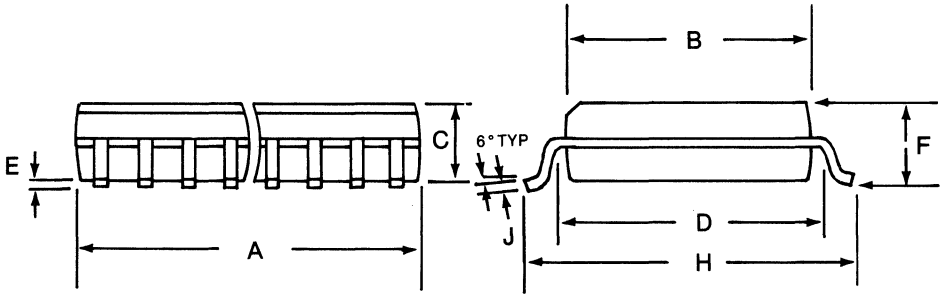

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .960 | 1.040 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |



# DS1211S
## Nonvolatile Controller




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .503 | .511 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



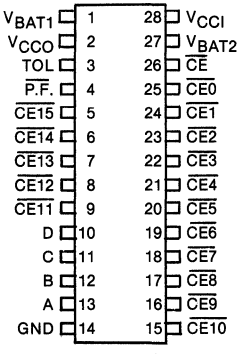
**Dallas Semiconductor**
***Nonvolatile Controller/Decoder***

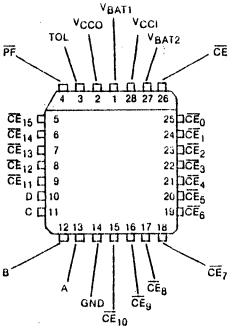
# *DS1212— 28-Pin DIP*
# *DS1212Q— 28-Pin PLCC*

## FEATURES

- Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when $V_{CC}$ is out of tolerance
- Automatically switches to battery when power fail occurs
- 4 to 16 decoder provides control for up to 16 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 28-pin PLCC surface mount package

## PIN CONNECTIONS




## PIN NAMES

| | |
|---|---|
| A, B, C, D | - Address Inputs |
| $\overline{CE}$ | - Chip Enable |
| $\overline{CE0}$-$\overline{CE15}$ | - Chip Enable Outputs |
| GND | - Ground |
| $V_{BAT1}$ | - + Battery 1 |
| $V_{BAT2}$ | - + Battery 2 |
| TOL | - Power Supply Tolerance |
| $V_{CCI}$ | - +5V Supply |
| $V_{CCO}$ | - RAM Supply |
| $\overline{P.F.}$ | - Power Fail |

## DESCRIPTION

The DS1212 is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption.

By combining the DS1212 nonvolatile controller/decoder chip and lithium batteries, ten years of nonvolatile RAM operation can be achieved for up to sixteen CMOS memories.

## OPERATION

The DS1212 nonvolatile controller/decoder performs six circuit functions required to decode and battery back up a bank of sixteen RAMs. First, the 4 to 16 decoder provides selection of one of sixteen RAMs. Second, a switch is provided to direct power from the battery or $V_{CCI}$ supply, depending on which is greater. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller/decoder provides is power fail detection. The DS1212 constantly monitors the $V_{CCI}$ supply. When $V_{CCI}$ falls below 4.75 volts, or 4.5 volts depending on the level of the tolerance Pin 3, a precision comparator outputs a power fail detect signal to the decoder/chip enable logic and the $\overline{PF}$ signal is driven low. The $\overline{PF}$ signal will remain low until $V_{CCI}$ is back in normal limits. The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$-$\overline{CE15}$) to within 0.2 volts of $V_{CCI}$ or battery supply. If $\overline{CE}$ is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 is connected to $V_{CCO}$, then power fail occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 4 to 16 decoder, shown in Figure 1. The fifth function the DS1212 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0 volts and data is in danger of being corrupted. The sixth function of the nonvolatile controller/decoder provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to insure reliability. The DS1212 provides an internal isolation switch which allows the connection of two batteries during battery backup operation. The battery with the highest voltage is selected for use. If one battery should fail, the other will then assume the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. For single battery applications the unused battery input must be grounded.

**NONVOLATILE CONTROLLER/DECODER** Figure 1

| INPUTS | | | | | | OUTPUTS | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{CCI}$ | CE | D | C | B | A | CE0 | CE1 | CE2 | CE3 | CE4 | CE5 | CE6 | CE7 | CE8 | CE9 | CE10 | CE11 | CE12 | CE13 | CE14 | CE15 | PF |
| ≥ 4.75 | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| < 4.75 | X | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| ≥ 4.75 | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| ≥ 4.75 | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| ≥ 4.75 | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| ≥ 4.75 | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| ≥ 4.75 | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| ≥ 4.75 | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| ≥ 4.75 | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| ≥ 4.75 | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| ≥ 4.75 | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| ≥ 4.75 | L | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| ≥ 4.75 | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| ≥ 4.75 | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| ≥ 4.75 | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| ≥ 4.75 | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| ≥ 4.75 | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| ≥ 4.75 | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |

H = High Level
L = Low Level
X = Irrelevant

**NOTE:**
$V_{CCI}$ input is 250 mV lower when TOL PIN 3 = $V_{CCO}$

**ABSOLUTE MAXIMUM RATINGS***

Voltage on Any Pin Relative to Ground −0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| PIN 3 = GND Supply Voltage | $V_{CCI}$ | 4.75 | 5.0 | 5.5 | V | 1 |
| PIN 3 = $V_{CCO}$ Supply Voltage | $V_{CCI}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Logic 1 Input | $V_{IH}$ | 2.2 | | $V_{CC}$ + 0.3 | V | 1 |
| Logic 0 Input | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| Battery Input | $V_{BAT1}$ $V_{BAT2}$ | 2.0 | | 4.0 | V | 1,2 |

**D.C. ELECTRICAL CHARACTERISTICS**

(0°C to 70°C, $V_{CCI}$ = 4.75V to 5.5V, Pin 3 = GND)
(0°C to 70°C, $V_{CCI}$ = 4.5 to 5.5V, Pin 3 = $V_{CCO}$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CCI}$ | | | 5 | mA | 3 |
| Supply Current @$V_{CCO}$ = $V_{CCI}$ − 0.2 | $I_{CCO1}$ | | | 80 | mA | 1,4,10 |
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | uA | |
| Output Leakage | $I_{LO}$ | −1.0 | | +1.0 | uA | |
| $\overline{CE_0}$-$\overline{CE15}$, $\overline{PF}$ Output @2.4V | $I_{OH}$ | −1.0 | | | mA | 5 |
| $\overline{CE_0}$-$\overline{CE15}$, PF Output @ 0.4V | $I_{OL}$ | | | 4.0 | mA | 5 |
| $V_{CC}$ Trip Point ($\overline{TOL}$ = GND) | $V_{CCTP}$ | 4.50 | 4.62 | 4.74 | V | 1 |
| $V_{CC}$ Trip Point ($\overline{TOL}$ = $V_{CC}$) | $V_{CCTP}$ | 4.25 | 4.37 | 4.49 | V | 1 |

10

(0 °C to 70 °C, $V_{CCI} < V_{BAT}$)

| | | | | | | |
|---|---|---|---|---|---|---|
| $\overline{CE}0$-$\overline{CE}15$ Output | $V_{OHL}$ | $V_{BAT} - 0.2$ | | | V | 3,7 |
| Battery Current | $I_{BAT}$ | | | 0.1 | uA | 2,3 |
| Battery Backup Current @$V_{CCO} = V_{BATI} - 0.5V$ | $I_{CC02}$ | | | 100 | uA | 6,10,11 |

**CAPACITANCE** ($t_A = 25$ °C)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

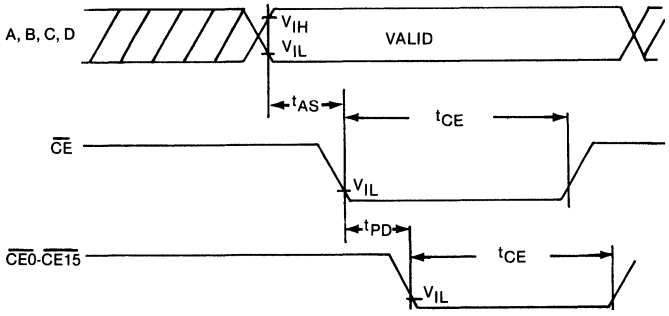
**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CCI} = 4.75$ to 5.5V, Pin 3 = GND)
(0 °C to 70 °C , $V_{CCI} = 4.5$ to 5.5V, Pin 3 = $V_{CCO}$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ Propagation Delay | $t_{PD}$ | 5 | 10 | 20 | ns | 5 |
| $\overline{CE}$ High to Power Fail | $t_{PF}$ | | | 0 | ns | |
| Address Set Up | $t_{AS}$ | 20 | | | ns | 9 |

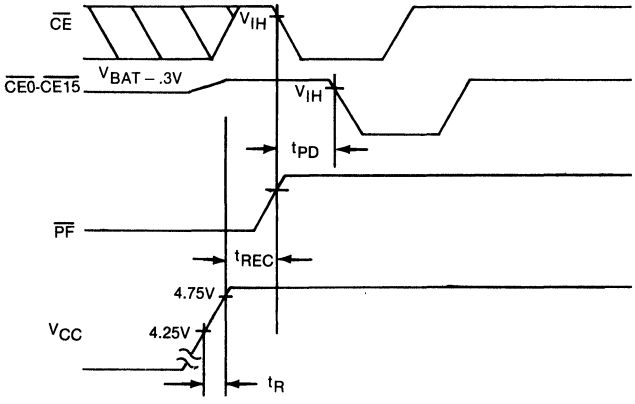
(0 °C to 70 °C, $V_{CCI} < 4.75$V, Pin 3 = GND)
(0 °C to 70 °C, $V_{CCI} < 4.5$V, Pin 3 = $V_{CCO}$)

| | | | | | | |
|---|---|---|---|---|---|---|
| Recovery at Power Up | $t_{REC}$ | 2 | 80 | 125 | ms | |
| $V_{CC}$ Slew Rate Power Down | $t_F$ | 300 | | | us | |
| $V_{CC}$ Slew Rate Power Down | $t_{FB}$ | 10 | | | us | |
| $V_{CC}$ Slew Rate Power Up | $t_R$ | 0 | | | us | |
| $\overline{CE}$ Pulse Width | $t_{CE}$ | | | 1.5 | us | 7,8 |
| Power Fail to $\overline{PF}$ Low | $t_{PFL}$ | 300 | | | us | |

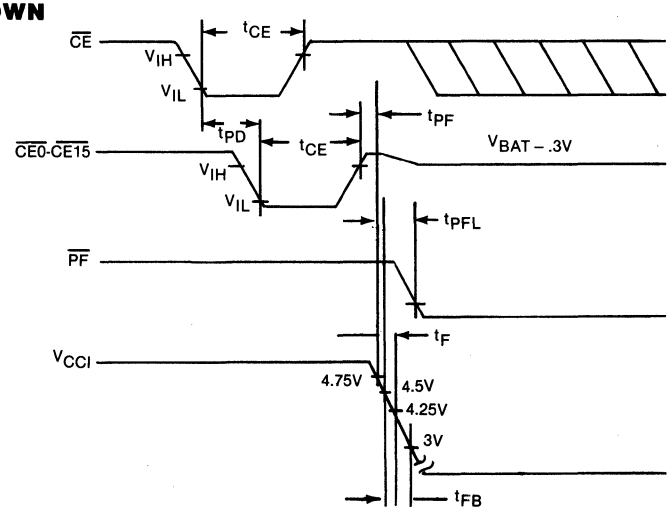
## TIMING DIAGRAM—DECODER




## TIMING DIAGRAM—POWER UP




## TIMING DIAGRAM—POWER DOWN

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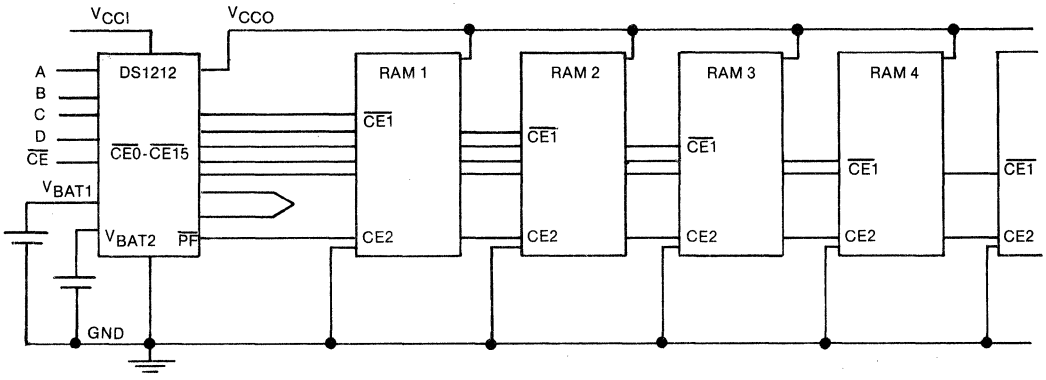
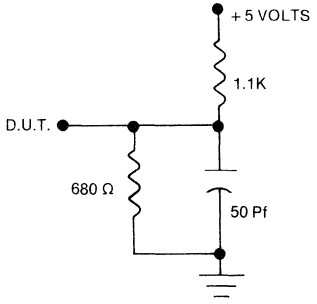
**TYPICAL APPLICATION** Figure 2

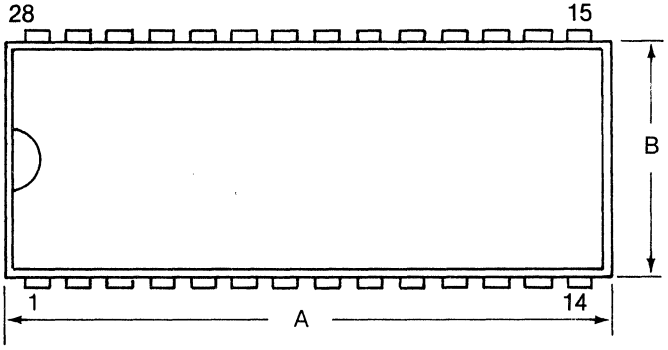



**NOTES:**

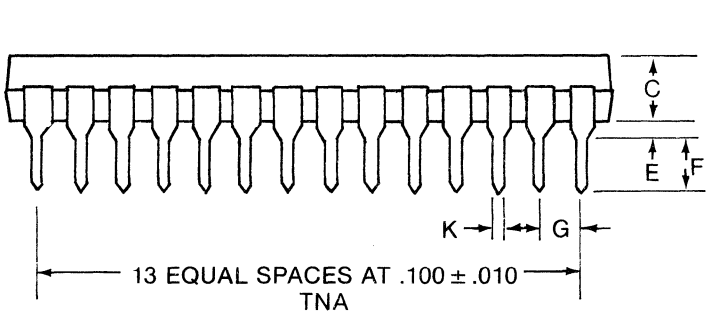
1. All voltages are referenced to ground
2. Only one battery input is required
3. Measured with $V_{CCO}$ and $\overline{CE0}$ - $\overline{CE15}$ open
4. $I_{CC01}$ is the maximum average load which the DS1212 can supply to the memories
5. Measured with a load as shown in Figure 3
6. $I_{CC02}$ is the maximum average load current which the DS1212 can supply to the memories in the battery backup mode.
7. Chip enable outputs $\overline{CE0}$ - $\overline{CE15}$ can only sustain leakage current in the battery backup mode
8. $t_{CE}$ max must be met to insure data integrity on power loss
9. $t_{AS}$ is only required to keep the decoder outputs glitch-free. While $\overline{CE}$ is low, the outputs ($\overline{CE0}$ through $\overline{CE15}$) will be defined by inputs A through D with a propagation delay of $t_{PD}$ from an A through D input change
10. For applications where higher currents are required, please see the Battery Manager data sheet (DS1259)
11. The DS1212 has a 5KΩ resistor in series with the battery input. As current from the battery increases over 100 *u*A, the voltage drop will increase proportionately. The device cannot be damaged by higher currents in the battery path

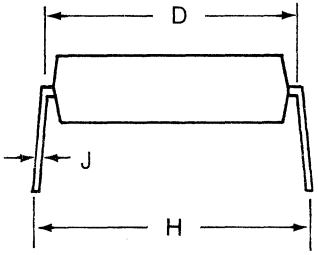
**OUTPUT LOAD** Figure 3



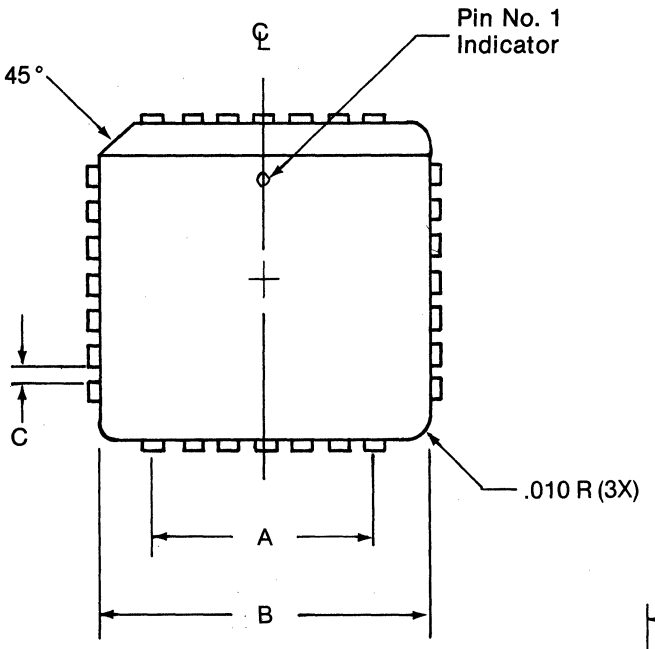



| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.440 | 1.480 |
| B | .540 | .560 |
| C | .140 | .160 |
| D | .590 | .610 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .600 | .680 |
| J | .008 | .012 |
| K | .015 | .021 |

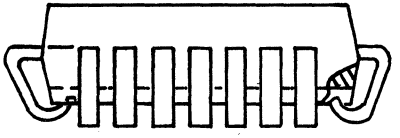


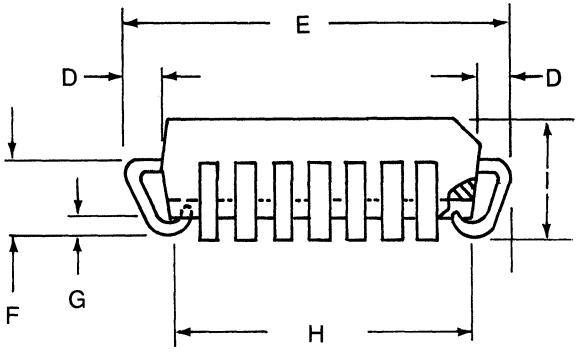



# DS 1212Q




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .290 | .310 |
| B | .441 | .451 |
| C | .020 | .024 |
| D | .018 | .022 |
| E | .488 | .492 |
| F | .118 | .122 |
| G | .020 | .030 |
| H | .390 | .430 |
| I | .167 | .173 |





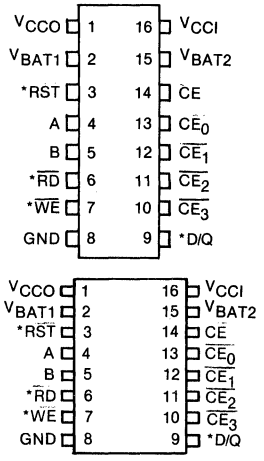
# Dallas Semiconductor
## *Nonvolatile Controller /Decoder*

## *DS1221—16-Pin DIP*
## *DS1221S—16-Pin SOIC*

### FEATURES

- Converts CMOS RAMs into Nonvolatile Memories
- Data is automatically protected during power loss
- 2 to 4 Decoder provides for up to 4 CMOS RAMs
- Provides for redundant batteries
- Test battery condition on power up
- Full ±10% operating range
- Unauthorized access can be prevented with optional security feature
- 16-pin 0.3-inch DIP saves P.C. board space
- Optional 16-pin SOIC surface mount package

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| A, B | - Address Inputs |
| $\overline{CE}$ | - Chip Enable Input |
| $\overline{CE_0}$-$\overline{CE_3}$ | - Chip Enable Outputs |
| $V_{BAT1}$ | - + Battery 1 |
| $V_{BAT2}$ | - + Battery 2 |
| *$\overline{RST}$ | - Reset |
| $V_{CCI}$ | - +5V Supply |
| $V_{CCO}$ | - RAM Supply |
| *$\overline{RD}$ | - Read Input |
| *$\overline{WE}$ | - Write Input |
| *D/Q | - Data Input/Output |

*Used with optional security circuit only and must be connected to ground in all other cases.

### DESCRIPTION

The DS1221 is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out of tolerance condition. When such a condition is detected, the chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. An optional security code prevents unauthorized users from obtaining access to the memory space. The nonvolatile controller/decoder circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. By combining the DS1221 with up to four CMOS memories and lithium batteries, ten years of nonvolatile operation can be achieved.

## CONTROLLER/DECODER OPERATION

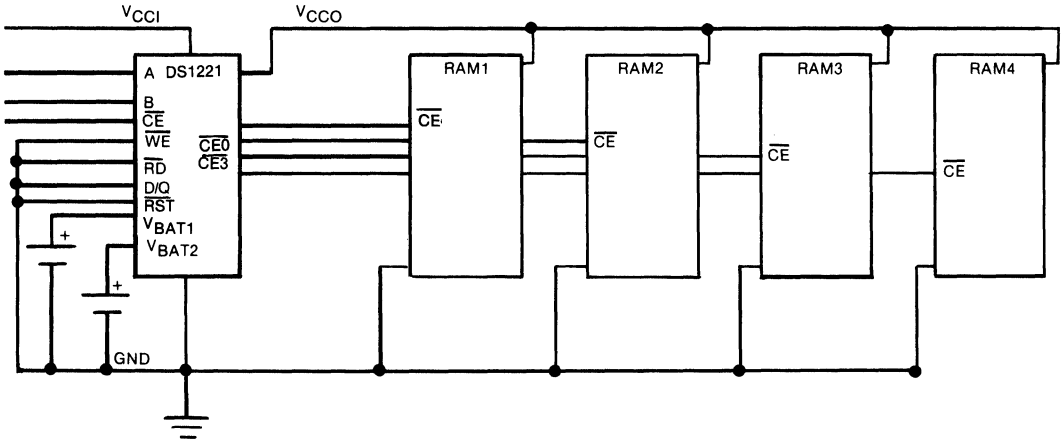
The DS1221 nonvolatile controller/decoder performs six circuit functions required to decode and battery back up a bank of up to four CMOS RAMs. First, a 2 to 4 decoder provides selection of one of four RAMs (See Figure 1). Second, a switch is provided to direct power from the battery or $V_{CCI}$ supply, depending on which is greater, to the $V_{CCO}$ pin. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller/decoder provides is power fail detection. The DS1221 constantly monitors the $V_{CCI}$ supply. When $V_{CCI}$ falls below 4.5 volts, a precision comparator detects the condition and inhibits the RAM chip enables ($\overline{CE0}$ through $\overline{CE3}$). The fourth function of write protection is accomplished by holding all chip enable outputs ($\overline{CE0}$-$\overline{CE3}$) to within 0.2 volts of $V_{CCI}$ or battery supply. If the Chip Enable Input ($\overline{CE}$) is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until $\overline{CE}$ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power failure detection occurs in the range of 4.5 to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 2 to 4 decoder. The fifth function the DS1221 performs is to check battery status to warn of potential data loss. Each time that $V_{CCI}$ power is restored the battery voltage is checked with a precision comparator. If the connected battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memories are questionable. The sixth function of the nonvolatile controller/decoder provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to insure reliability. The DS1221 provides an internal isolation switch which provides for connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. If only one battery is used, the second battery input must be grounded. Figure 2 illustrates the connections required for the DS1221 in a typical application.

**NONVOLATILE CONTROLLER/DECODER** Figure 1

| | INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| $V_{CCI}$ | $\overline{CE}$ | B | A | $\overline{CE0}$ | $\overline{CE1}$ | $\overline{CE2}$ | $\overline{CE3}$ |
| ≥ 4.5 | H | X | X | H | H | H | H |
| < 4.25 | X | X | X | H | H | H | H |
| ≥ 4.5 | L | L | L | L | H | H | H |
| ≥ 4.5 | L | L | H | H | L | H | H |
| ≥ 4.5 | L | H | L | H | H | L | H |
| ≥ 4.5 | L | H | H | H | H | H | L |

H = High Level
L = Low Level
X = Irrelevant

**TYPICAL APPLICATION** Figure 2




Battery Backup Current Drain

| | |
|---|---|
| DS1221 | .1 uA @ 25° C |
| RAM-5564 × 4 | .8 uA @ 25° C |
| Total | .9 uA @ 25° C |

10

**ABSOLUTE MAXIMUM RATINGS***

Voltage on Any Pin Relative to Ground −0.3V to +7V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to 125°C
Soldering Temperature 260°C for 10 Sec
Short Circuit Output Current 20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CCI}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Logic 1 Input | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1 |
| Logic 0 Input | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| Battery Input | $V_{BAT1}$ $V_{BAT2}$ | 2.0 | | 4.0 | V | 1,2 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CCI}$ | | | 5 | mA | 3 |
| Suply Voltage | $V_{CCO}$ | $V_{CC}-0.2$ | | | V | 1 |
| Supply Current | $I_{CCO1}$ | | | 80 | mA | 4,10 |
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | uA | |
| Output Leakage | $I_{LO}$ | −1.0 | | +1.0 | uA | |
| $\overline{CE0}$-$\overline{CE3}$, DQ Output @2.4V | $I_{OH}$ | −1.0 | | | mA | 5 |
| $\overline{CE0}$-$\overline{CE3}$, DQ Output @ 0.4V | $I_{OL}$ | | | 4.0 | mA | 5 |
| $V_{CC}$ Trip Point | $V_{CCTP}$ | 4.25 | 4.37 | 4.50 | V | 1 |

(0°C to 70°C, $V_{CC}$<4.25)

| | | | | | | |
|---|---|---|---|---|---|---|
| $\overline{CE0}$-$\overline{CE3}$ Output | $V_{OHL}$ | $V_{CC}-0.2$ $V_{BAT}-0.2$ | | | V | |
| $V_{BAT1}$ or $V_{BAT2}$ Battery Current | $I_{BAT}$ | | | 0.1 | uA | 3 |
| Battery Backup Current @$V_{CCO}=V_{BAT}-0.5V$ | $I_{CCO2}$ | | | 100 | uA | 6,7,10 |

**CAPACITANCE** ($t_A = 25°C$)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC}$ = 4.5 to 5.5V)

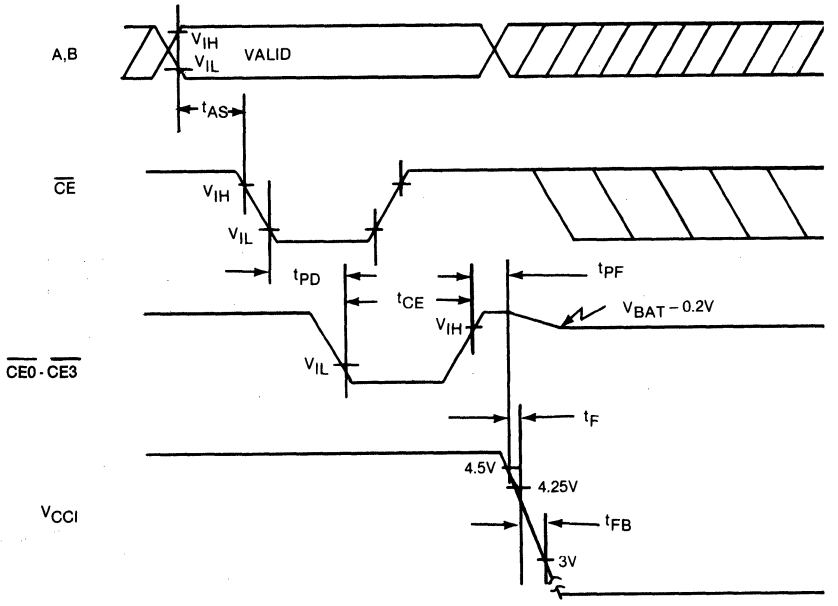
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ Propagation Delay | $t_{PD}$ | 5 | 10 | 20 | ns | 5 |
| $\overline{CE}$ High to Power Fail | $t_{PF}$ | | | 0 | ns | |
| Address Set Up | $t_{AS}$ | 20 | | | ns | 9 |

(0 °C to 70 °C, $V_{CC} < 4.5V$)

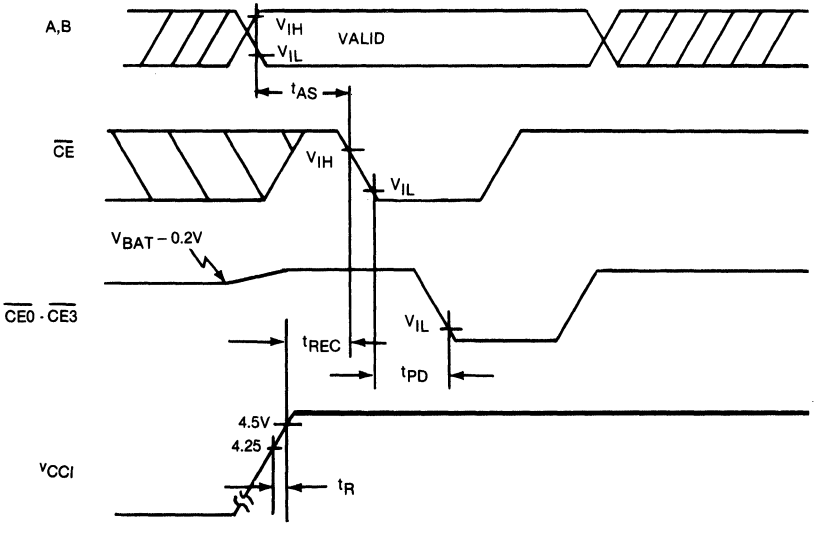
| | | | | | | |
|---|---|---|---|---|---|---|
| Recovery at Power Up | $t_{REC}$ | 2 | 5 | 10 | ms | |
| $V_{CC}$ Slew Rate 4.5 - 4.25V | $t_F$ | 300 | | | us | |
| $V_{CC}$ Slew Rate 4.25 - 3V | $t_{FB}$ | 10 | | | us | |
| $V_{CC}$ Slew Rate 4.25 - 4.5V | $t_R$ | 0 | | | us | |
| $\overline{CE}$ Pulse Width | $t_{CE}$ | | | 1.5 | us | 7,8 |

10

## TIMING DIAGRAM—POWER DOWN




## TIMING DIAGRAM—POWER UP

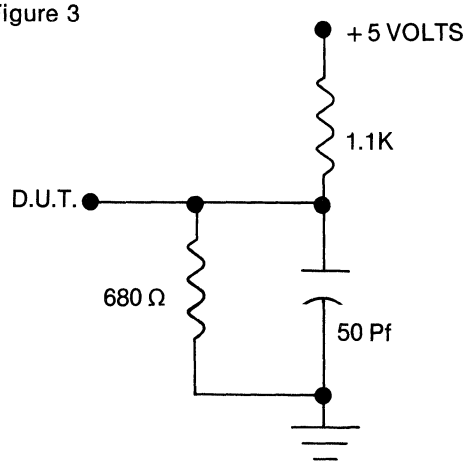


**NOTES:**

1. All voltages are referenced to ground
2. Only one battery input is required
3. Measured with $V_{CCO}$ and $\overline{CE0}$ - $\overline{CE3}$ open
4. $I_{CCO1}$ is the maximum average load which the DS1221 can supply to the memories
5. Measured with a load as shown in Figure 3
6. $I_{CCO2}$ is the maximum average load current which the DS1221 can supply to the memories in the battery backup mode
7. Chip enable outputs $\overline{CE0}$ - $\overline{CE3}$ can only sustain leakage current in the battery backup mode
8. $t_{CE}$ max must be met to insure data integrity on power loss
9. $t_{AS}$ is only required to keep the decoder outputs glitch-free. While $\overline{CE}$ is low, the outputs ($\overline{CE0}$ through $\overline{CE3}$) will be defined by inputs A and B with a propagation delay of $t_{PD}$ from an A or B input change
10. For applications where higher currents are required, please see the Battery Manager data sheet (DS1259)

**OUTPUT LOAD**

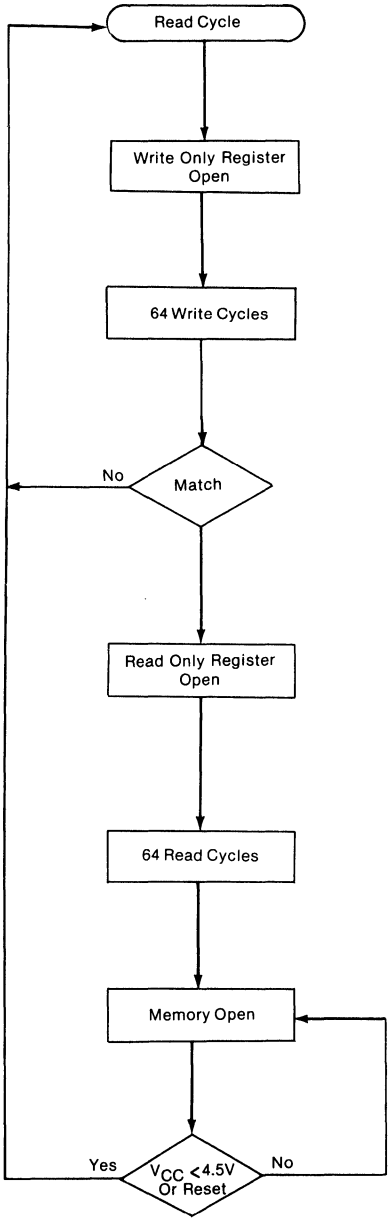
Figure 3



## SECURITY OPTION

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 1). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1221 using the write enable signal ($\overline{WE}$), the chip enable signal ($\overline{CE}$), and the data input/output signal (DQ). The code is written to the DS1221 without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1221 by Dallas Semiconductor at time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1221 and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register may be used by software to determine if the DS1221 will be permitted to be used with that particular system. After the 64th read cycle has been executed the DS1221 is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If $V_{CC}$ falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.
**Note:** Contact Dallas Semiconductor sales office for code assignment.

**SECURITY SEQUENCE**
Figure 1



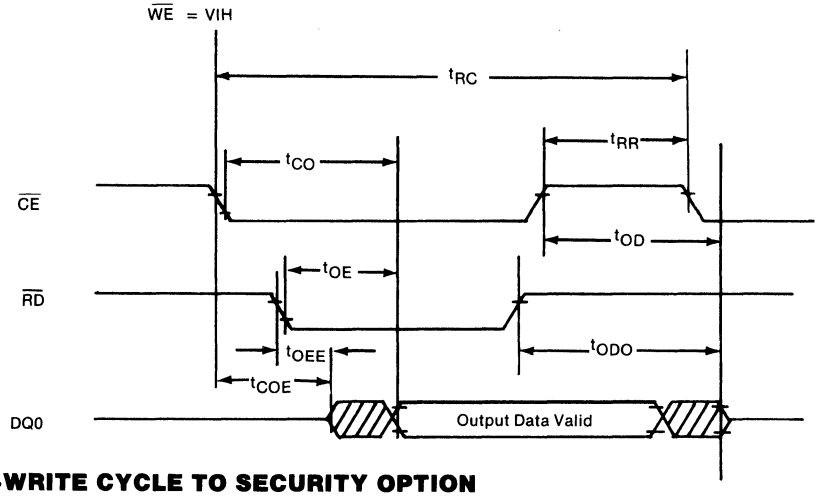
## SECURITY OPTION

### A.C. ELECTRICAL CHARACTERISTICS

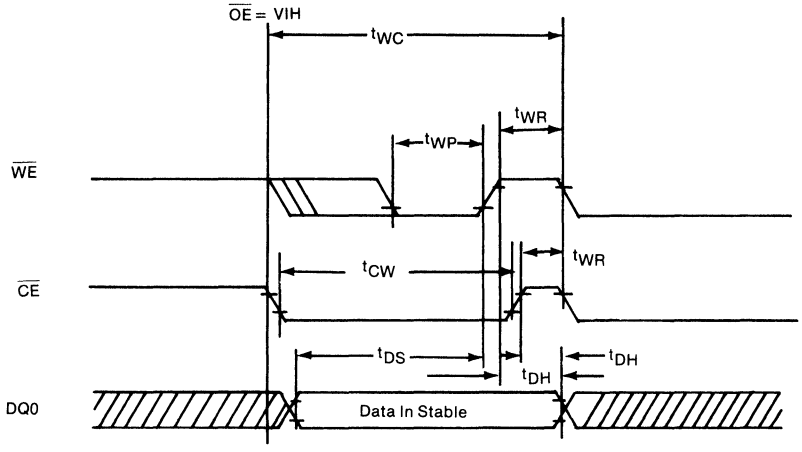
(0 °C - 70 °C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS |
|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 250 | | | ns |
| $\overline{CE}$ Access Time | $t_{CO}$ | | | 200 | ns |
| $\overline{RD}$ Access Time | $t_{OE}$ | | | 100 | ns |
| $\overline{CE}$ To Output Low Z | $t_{COE}$ | 10 | | | ns |
| $\overline{RD}$ To Output Low Z | $t_{OEE}$ | 10 | | | ns |
| $\overline{CE}$ To Output High Z | $t_{OD}$ | | | 100 | ns |
| $\overline{RD}$ To Output High Z | $t_{ODO}$ | | | 100 | ns |
| Read Recovery | $t_{RR}$ | 50 | | | ns |
| Write Cycle | $t_{WC}$ | 250 | | | ns |
| Write Pulse Width | $t_{WP}$ | 170 | | | ns |
| Write Recovery | $t_{WR}$ | 50 | | | ns |
| Data Set Up | $t_{DS}$ | 100 | | | ns |
| Data Hold Time | $t_{DH}$ | 0 | | | ns |
| $\overline{CE}$ Pulse Width | $t_{CW}$ | 170 | | | ns |
| Reset Pulse Width | $t_{RST}$ | 200 | | | ns |

## TIMING DIAGRAM—READ CYCLE TO SECURITY OPTION



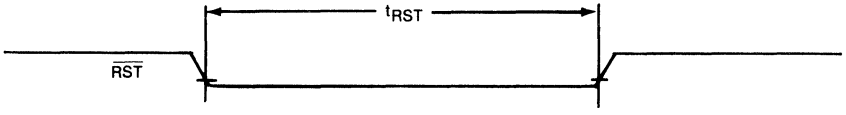

## TIMING DIAGRAM—WRITE CYCLE TO SECURITY OPTION



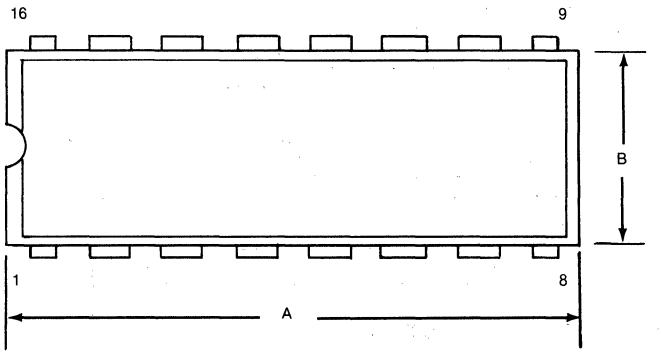

**NOTES:**

1. $t_{DH}$ and $t_{DS}$ are functions of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
2. $t_{WR}$ is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.

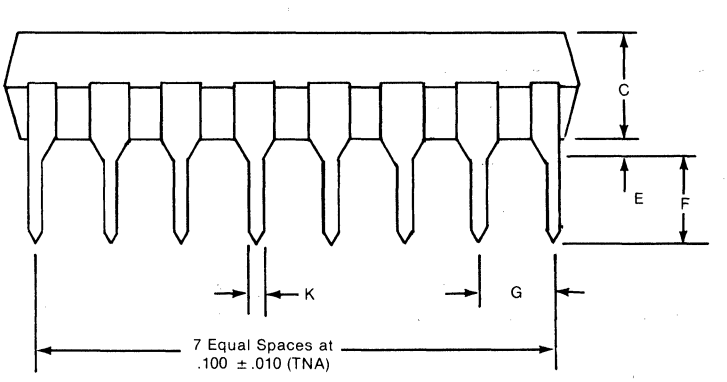
## TIMING DIAGRAM—RESET FOR SECURITY OPTION

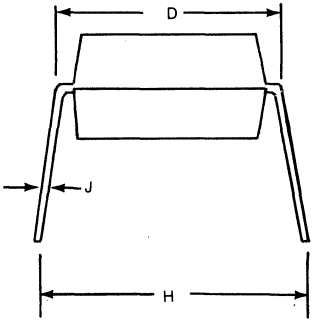


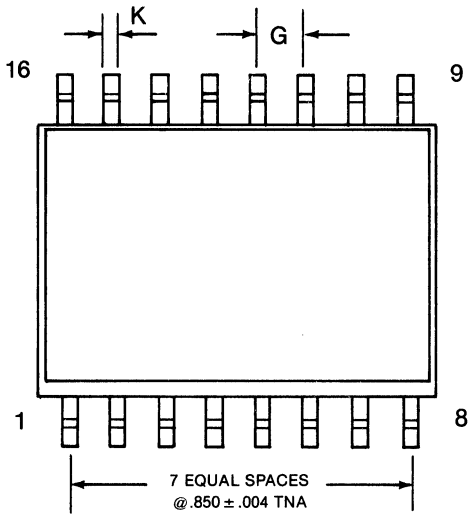
# DS1221
# Nonvolatile Controller/Decoder



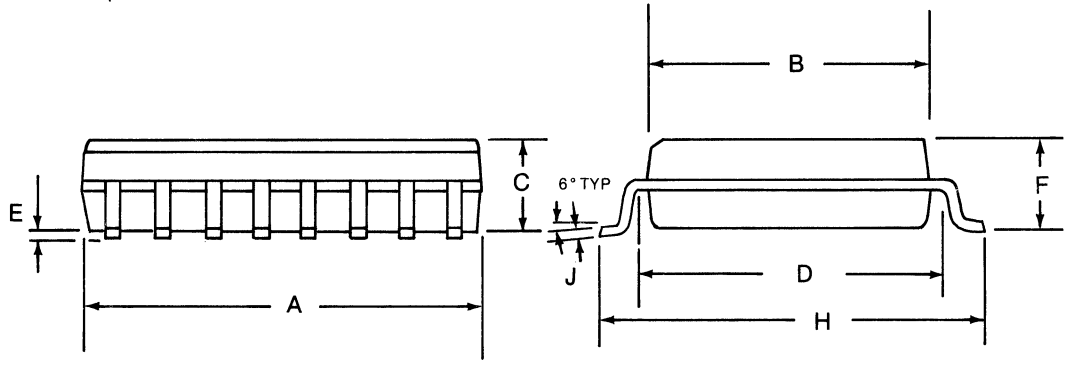

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .740 | .780 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |






| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



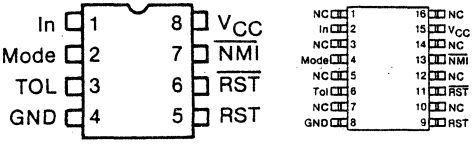
**Dallas Semiconductor**
***Power Monitor***

# *DS1231—8-Pin DIP*
# *DS1231S—16-Pin SOIC*

## FEATURES

- Warns processor of an impending power failure
- Provides time for an orderly shutdown
- Prevents processor from destroying non-volatile memory during power transients
- Automatically restarts processor after power is restored
- Suitable for linear or switching power supplies
- Adjusts to hold time of the power supply
- Supplies necessary signals for processor interface
- Accurate 5% or 10% $V_{CC}$ monitoring
- Replaces power up reset circuitry
- No external capacitors required
- Optional 16-pin SOIC surface mount package

## PIN CONNECTIONS




## PIN NAMES

| | |
|---|---|
| In | - Input |
| Mode | - Selects input pin characteristics |
| TOL | - Selects 5% or 10% $V_{CC}$ detect |
| GND | - Ground |
| $\overline{RST}$ | - Reset (Active High) |
| RST | - Reset (Active Low, open drain) |
| $\overline{NMI}$ | - Nonmaskable interrupt |
| $V_{CC}$ | - +5 V Supply |
| NC | - No Connections |

## DESCRIPTION

The DS1231 Power Monitor uses a precise temperature compensated reference circuit which provides an orderly shutdown and an automatic restart of a processor-based system. A signal warning of an impending power failure is generated well before regulated DC voltages go out of specification by monitoring high voltage inputs to the power supply regulators. If line isolation is required, a UL-approved opto-isolator can be directly interfaced to the DS1231. The time for processor shutdown is directly proportional to the available hold-up time of the power supply. Just before the hold-up time is exhausted, the power monitor unconditionally halts the processor to prevent spurious cycles by enabling Reset as $V_{CC}$ falls below a selectable 5 or 10 percent threshold. When power returns, the processor is held inactive until well after power conditions have stabilized, safeguarding any nonvolatile memory in the system from inadvertent data changes.

## OPERATION

The DS1231 Power Monitor provides the function of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. The main elements of the DS1231 are illustrated in Figure 1. As shown, the DS1231 actually has two comparators, one for monitoring the input (Pin 1) and one for monitoring $V_{CC}$ (Pin 8). The $V_{CC}$ comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6) when $V_{CC}$ falls below a preset trip level as defined by TOL (Pin 3).

When TOL is connected to ground, the RST and $\overline{RST}$ signals will become active as $V_{CC}$ goes below 4.75 volts. When TOL is connected to $V_{CC}$, the RST and $\overline{RST}$ signals become active as $V_{CC}$ goes below 4.5 volts. The RST and $\overline{RST}$ signals are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid $V_{CC}$. On power up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply to stabilize (see Figure 2).

The comparator monitoring the input pin produces the $\overline{NMI}$ signal (Pin 7) when the input threshold voltage (VTP) falls to a level as determined by mode (Pin 2). When the mode pin is connected to $V_{CC}$, detection occurs at VTP−. In this mode Pin 1 is an extremely high impedance input allowing for a simple resistor voltage divider network to interface with high voltage signals. When the mode pin is connected to ground, detection occurs at VTP+. In this mode Pin 1 sources 30 uA of current allowing for connection to switched inputs, such as a UL-approved opto-isolator. The flexibility of the input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time allotted between $\overline{NMI}$ and $\overline{RST}$. On power up, $\overline{NMI}$ is released as soon as the input threshold voltage (VTP) is achieved and $V_{CC}$ is within nominal limits. In both modes of operation the input pin has hysteresis for noise immunity (Figure 3).

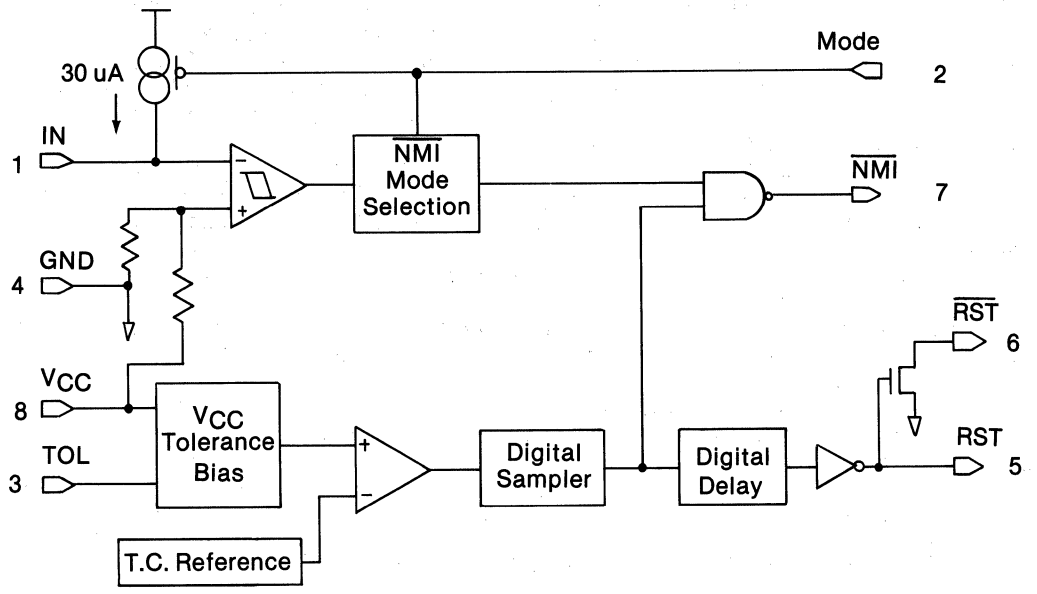
## APPLICATION—MODE PIN CONNECTED TO $V_{CC}$

When the mode pin is connected to $V_{CC}$, Pin 1 is a high impedance input. The voltage sense point and the level of voltage at the sense point are dependent upon the application (Figure 4). The sense point may be developed from the AC power line by rectifying and filtering the AC. Alternatively, a DC voltage level may be selected which is closer to the AC power input than the regulated +5-volt supply, so that ample time is provided for warning before regulation is lost.

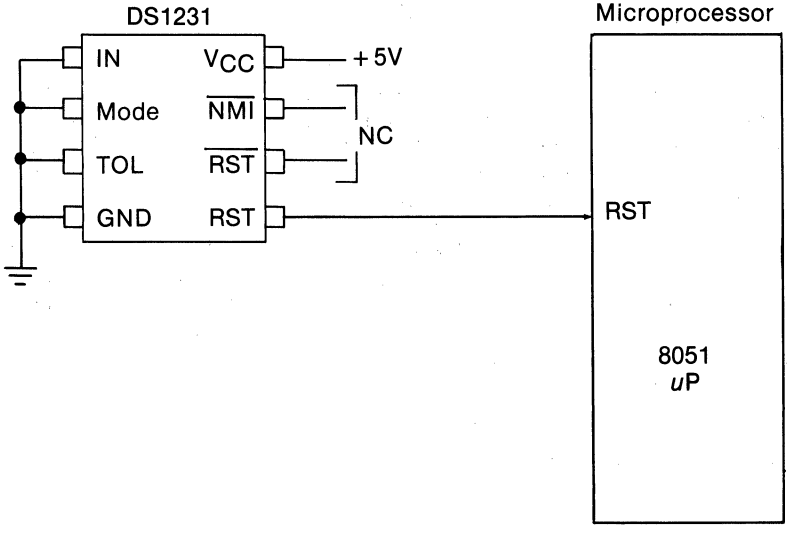
Proper operation of the DS1231 requires a maximum voltage of 5 volts at the input (Pin 1) which must be derived from the maximum voltage at the sense point. This is accomplished with a simple voltage divider network of R1 and R2. Since the IN trip point VTP− is 2.3 volts (using the −20 device), and the maximum allowable voltage on Pin 1 is 5 volts, the dynamic range of voltage at the sense point is set by the ratio of 2.3/5.0 = .46 min. This ratio determines the maximum deviation between the maximum voltage at the sense point and the actual voltage which will generate $\overline{NMI}$.

Having established the desired ratio, and confirming that the ratio is greater than .46 and less than 1, the proper values for R1 and R2 can be determined by the equation as shown in Figure 4. A simple approach to solving this equation is to select a value for R2 which is high impedance to keep power consumption low and solve for R1. Figure 5 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is connected to $V_{CC}$.

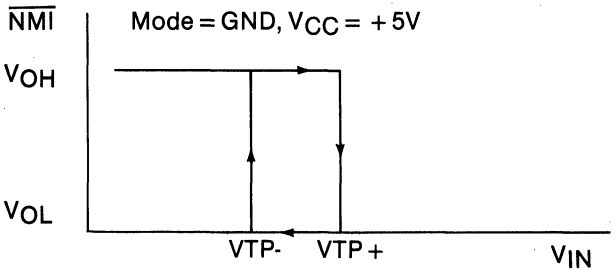
**POWER MONITOR BLOCK DIAGRAM** Figure 1

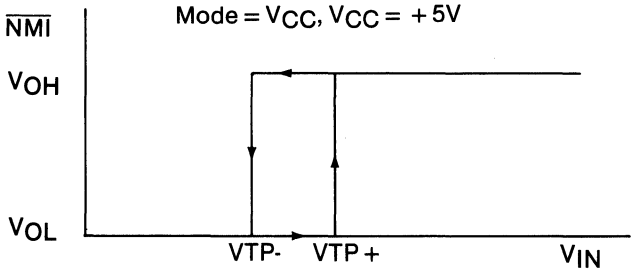



**POWER UP RESET** Figure 2



**INPUT PIN HYSTERESIS** Figure 3

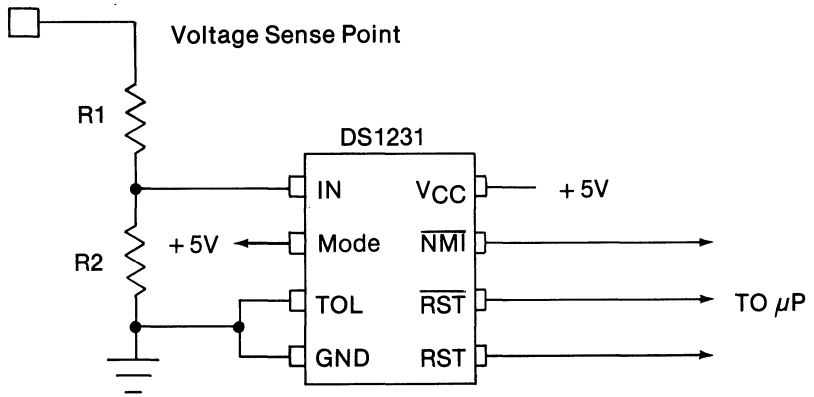



| | -20 | -35 | -50 |
|---|---|---|---|
| VTP- | 2.3 | 2.15 | 2.0 |
| VTP+ | 2.5 | 2.5 | 2.5 |

**NOTE:** Hysteresis tolerance is ±60 mV.

**APPLICATION WITH MODE PIN CONNECTED TO $V_{CC}$** Figure 4




$$V_{Sense} = \frac{R1 + R2}{R2} \times 2.3 \qquad V_{Max} = \frac{V_{Sense}}{VTP-} \times 5.0$$

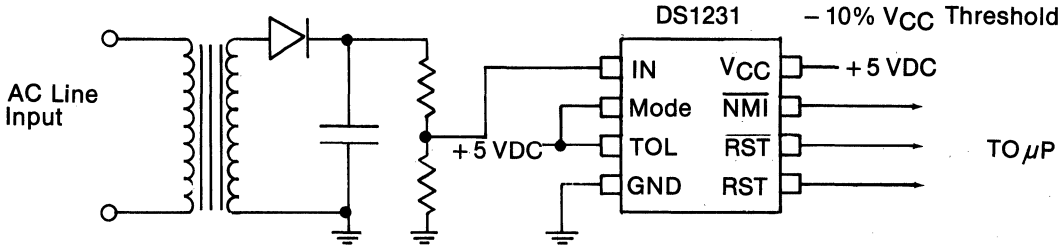
Example: $V_{Sense}$ = 8 volts at Trip Point and a maximum voltage of 17.5V with R2 = 10K

Then $8 = \frac{R1 + 10K}{10K} \times 2.3$ R1 = 25K

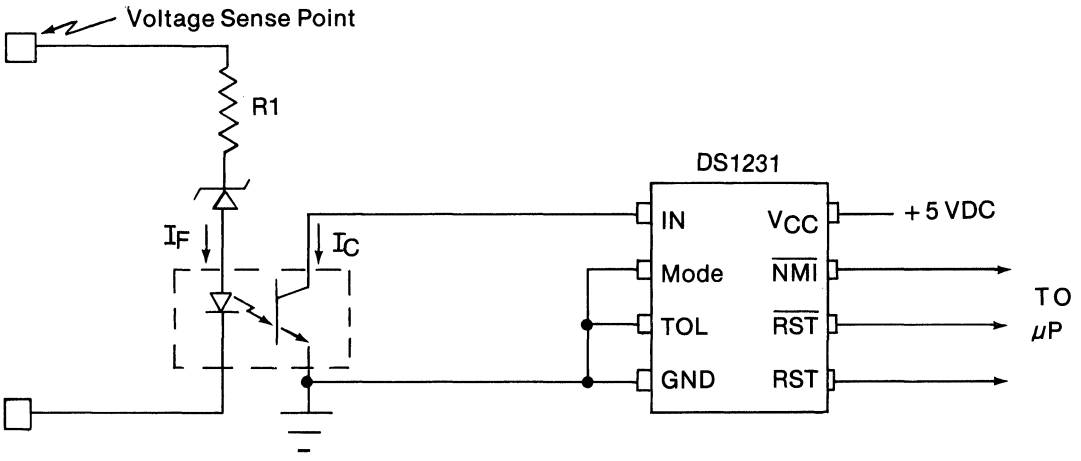
## APPLICATION—MODE PIN CONNECTED TO GROUND

When the mode pin is connected to ground, Pin 1 is a current source of 30 uA with a VTP+ of 2.5 volts. Pin 1 is held below the trip point by a switching device like an opto-isolator as shown in Figure 6. Determination of the sense point has the same criteria as discussed in the previous application. However, determining component values is significantly different. In this mode, the maximum dynamic range of the sense point versus desired trip voltage is primarily determined by the selection of a zener diode. As an example, if the maximum voltage at the sense point is 200V and the desired trip point is 150V, then a zener diode of 150V will approximately set the trip point. This is particularly true if power consumption on the high voltage side of the opto-isolator is not an issue. However, if power consumption is a concern, then it is desirable to make the value of R1 high. As the value of R1 increases, the effect of the LED current in the opto-isolator starts to affect the IN trip point. This can be seen from the equation shown in Figure 6. R1 must also be sized low enough to allow the opto-isolator to sink the 30 uA of collector current required by Pin 1 and still have enough resistance to keep the maximum current through the opto-isolator's LED within data sheet limits. Figure 7 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is grounded.

**AC VOLTAGE MONITOR WITH TRANSFORMER ISOLATION** Figure 5



**APPLICATION WITH MODE PIN GROUNDED** Figure 6




$$\text{Voltage Sense Point (Trip Value)} = V_Z + \frac{I_C}{CTR} \times R1$$

$$CTR = \frac{I_C}{I_F}$$

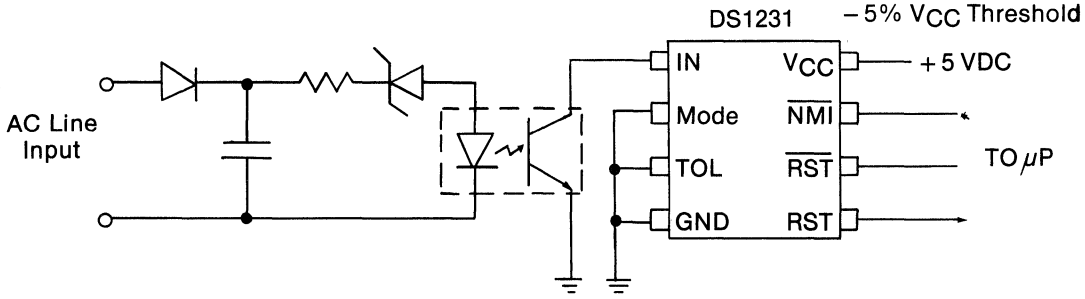
CTR = Current Transfer Ratio
$V_Z$ = Zener Voltage

Example: CTR = 0.2 $I_C$ = 30uA $I_F$ = 150uA
Voltage Sense Point = 105 and $V_Z$ = 100 volts

Then $105 = 100 + \frac{30}{0.2} \times R1$ R1 = 33K

10

**AC VOLTAGE MONITOR WITH OPTO-ISOLATION** Figure 7



## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on any Pin Relative to Ground | -0.3V to +7.0V |
| Operating Temperature | 0°C to 70°C |
| Storage Temperature | -55°C to 125°C |
| Soldering Temperature | 260°C for 10 Sec |

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input Pin 1 | $V_{IN}$ | | | $V_{CC}$ | V | 1 |

## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | uA | 2 |
| Output Current @2.4V | $I_{OH}$ | 1.0 | 2.0 | | mA | |
| Output Current @0.4V | $I_{OL}$ | 2.0 | 3.0 | | mA | |
| Operating Current | $I_{CC}$ | | 0.5 | 2.0 | mA | 3 |
| Input Pin 1 (Mode = GND) | $I_C$ | 15 | 25 | 50 | uA | |
| Input Pin 1 (Mode = $V_{CC}$) | $I_C$ | | | 0.1 | uA | |
| IN Trip Point (Mode = GND) | VTP | See Figure 3 | | | | 1 |
| IN Trip Point (Mode = $V_{CC}$) | VTP | | | | | 1 |
| $V_{CC}$ Trip Point (TOL = GND) | $V_{CCTP}$ | 4.50 | 4.62 | 4.74 | V | 1 |
| $V_{CC}$ Trip Point (TOL = $V_{CC}$) | $V_{CCTP}$ | 4.25 | 4.37 | 4.49 | V | 1 |

**CAPACITANCE** ($t_A = 25°C$)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

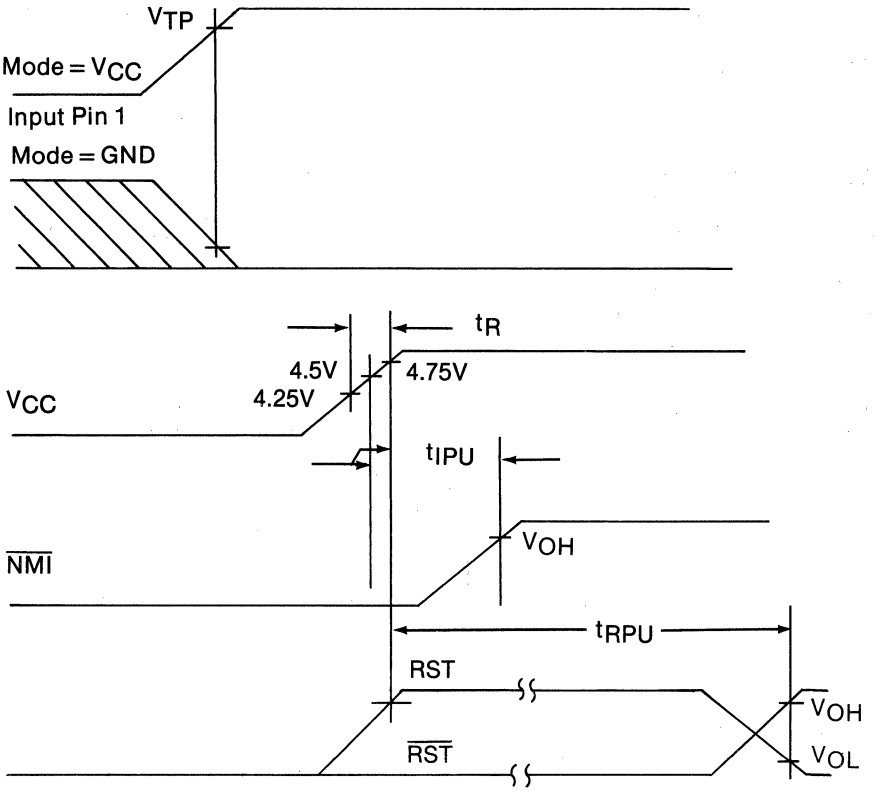
**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $V_{TP}$ to $\overline{NMI}$ Delay | $t_{IPD}$ | | | 1.1 | us | |
| $V_{CC}$ Slew Rate 4.75-4.25V | $t_F$ | 300 | | | us | |
| $V_{CC}$ Detect to $\overline{RST}$ and $\overline{RST}$ | $t_{RPD}$ | | | 100 | ns | |
| $V_{CC}$ Detect to $\overline{NMI}$ | $t_{IPU}$ | | | 200 | us | 4 |
| $V_{CC}$ Detect to $\overline{RST}$ and $\overline{RST}$ | $t_{RPU}$ | 250 | 500 | 1000 | ms | 4 |
| $V_{CC}$ Slew Rate 4.25-4.75V | $t_R$ | 0 | | | ns | |

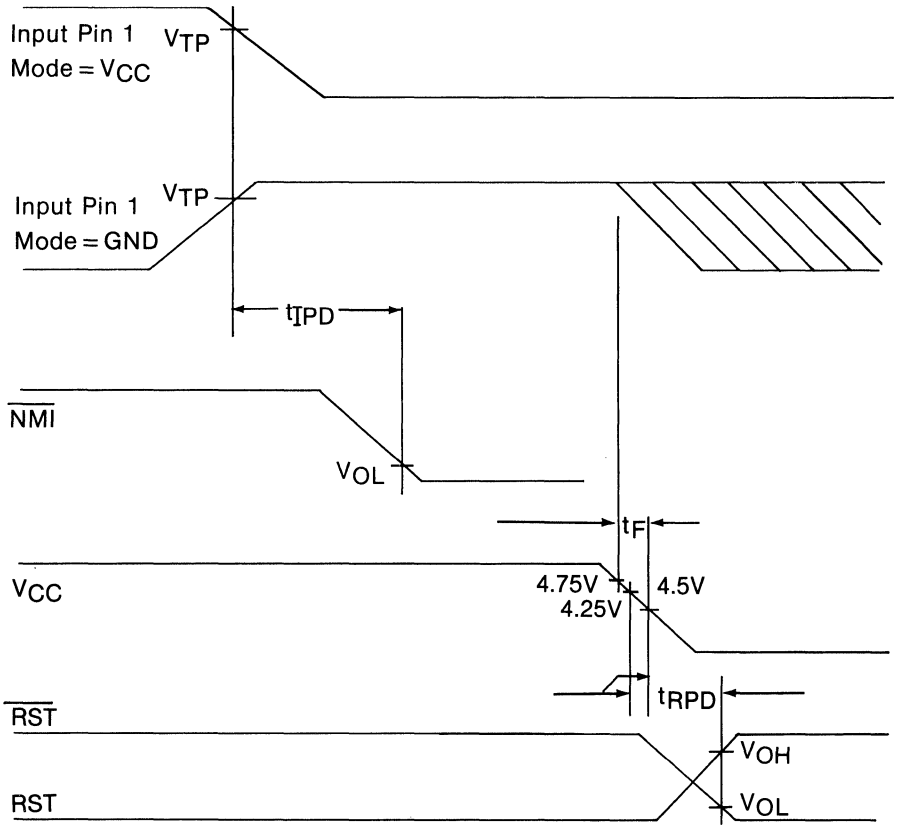
**NOTES:**

1. All voltages referenced to ground.
2. $V_{CC} = +5.0$ volts with outputs open.
3. Measured with outputs open.
4. $t_R = 5us$.

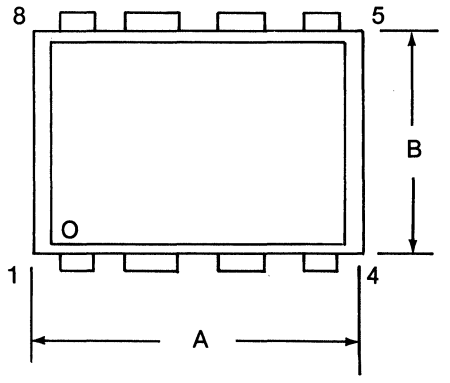
**TIMING DIAGRAM—POWER UP**



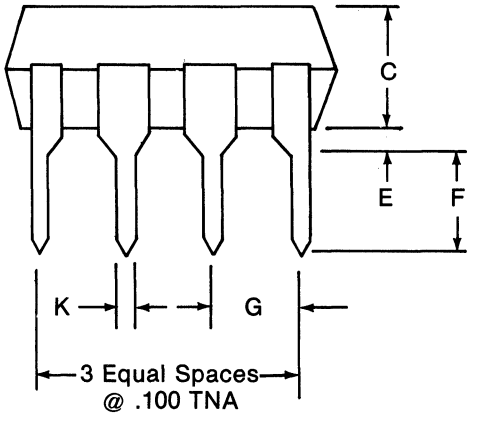
**TIMING DIAGRAM—POWER DOWN**

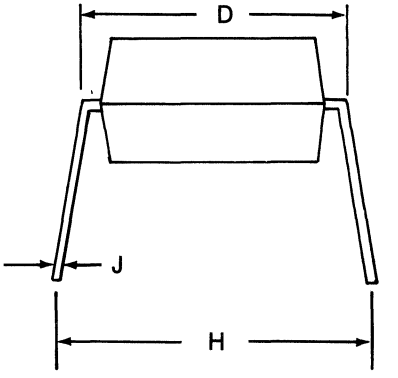


# DS1231
# Power Monitor

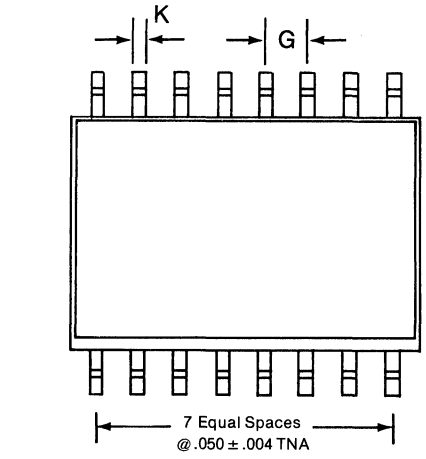



| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .360 | .400 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |

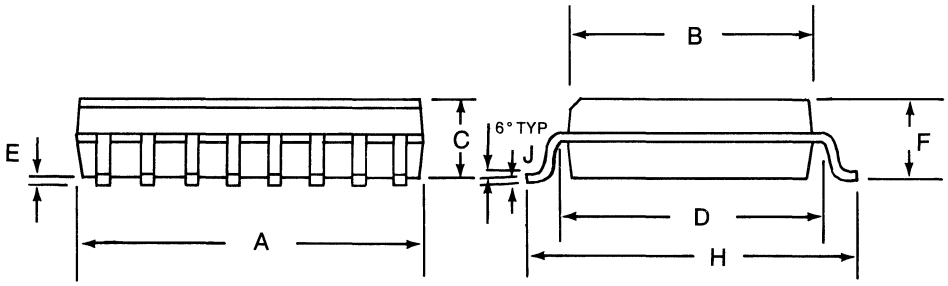


# DS1231S
# Power Monitor




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |




10

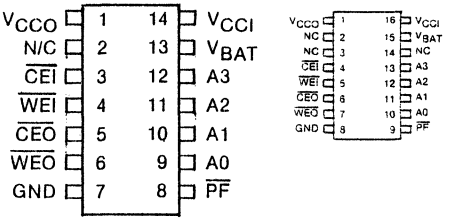
# Dallas Semiconductor
## *Conditional Nonvolatile Controller*

## *DS1234—14-Pin DIP*
## *DS1234S—16-Pin SOIC*

### FEATURES

- Converts CMOS static RAMs into nonvolatile memories
- Software controlled write inhibit
- Software controlled battery disconnect extends battery life
- Unconditionally write protects when $V_{CC}$ is out of tolerance
- Consumes less than 100 nA of battery current
- Power fail signal can be used to interrupt processor on power failure
- Low forward voltage drop on the $V_{CC}$ switch
- Optional 16-pin SOIC surface mount package

### PIN CONNECTIONS




### PIN NAMES

| | | |
|---|---|---|
| Pin 1 | - $V_{CCO}$ | RAM Supply |
| Pin 2 | - N/C | No Connection |
| Pin 3 | - $\overline{CEI}$ | Chip Enable Input |
| Pin 4 | - $\overline{WEI}$ | Write Enable Input |
| Pin 5 | - $\overline{CEO}$ | Chip Enable to Ram |
| Pin 6 | - $\overline{WEO}$ | Write Enable to RAM |
| Pin 7 | - GND | Ground |
| Pin 8 | - $\overline{PF}$ | Power Fail Output |
| Pins 9-12 | - A0-A3 | Address Inputs |
| Pin 13 | - $V_{BAT}$ | Battery Input |
| Pin 14 | - $V_{CCI}$ | +5V Supply |

### DESCRIPTION

The DS1234 is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory with the added features of two software selectable switches. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, Chip Enable and Write Enable to the RAM are inhibited to accomplish write protection and the battery is switched on to supply the memory with uninterrupted power. The two software selectable switches provided by the DS1234 are capable of inhibiting both the write enable to the RAM and the battery back-up circuitry by a pattern recognition sequence across four address lines. Inhibiting the write enable to the nonvolatile RAM provides data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery back-up is not needed.

## OPERATION

The DS1234 Conditional Nonvolatile Controller performs three circuit functions required to battery back-up a RAM. First, a switch is provided to direct power from the battery or the incoming supply ($V_{CCI}$), depending on whichever is greater. This switch has a voltage drop of less than 0.2V. The second function which the nonvolatile controller provides is power fail detection. The DS1234 constantly monitors the incoming supply. When the supply goes out of tolerance, a comparator detects power fail and inhibits chip enable and write enable. The threshold voltage, $V_{TP}$, at which power fail is detected is defined as 1.26 times $V_{BAT}$. The third function of write protection is accomplished by holding the $\overline{CEO}$ and $\overline{WEO}$ output signals to within 0.2 volts of the $V_{CCI}$ or battery supply. In addition to the nonvolatile controller functions, the DS1234 supplies two software selectable switches for master control of the write enable and the nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (see Tables 1 and 2). Prior to entering the pattern recognition sequence which will define the two switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointer to clock zero. Each four-bit compare word is clocked into the DS1234 on the low-going edge of $\overline{CEI}$. A0, A1 and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven, and the last five are used to define the switch settings. The eleventh address cycle, starting at zero, defines the switch which inhibits the write enable to the RAM ($\overline{WEO}$). A logic one in this location allows read/write operations so that $\overline{WEO}$ will follow $\overline{WEI}$ and data can be updated. A zero on cycle eleven turns the RAM into a read-only memory (ROM). The next four address cycles, 12 through 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010, respectively, activates the nonvolatile controller and data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation. At the completion of the 16th cycle, if the pattern recognition sequence is correct, the switch settings defined in cycles 11 through 15 are transferred and are active for the next memory cycle. When external battery power is applied for the first time, the DS1234 will come up with the nonvolatile controller off. Upon initial $V_{CC}$ power the write enable will be set in read/write operation ($\overline{WEI} = \overline{WEO}$).

**ADDRESS INPUT PATTERN** Table 1

| | Cycle Number | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Address Inputs** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** |
| $A_3$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | * | * | * | * | * |
| $A_2$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| $A_1$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| $A_0$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

*See Table 2

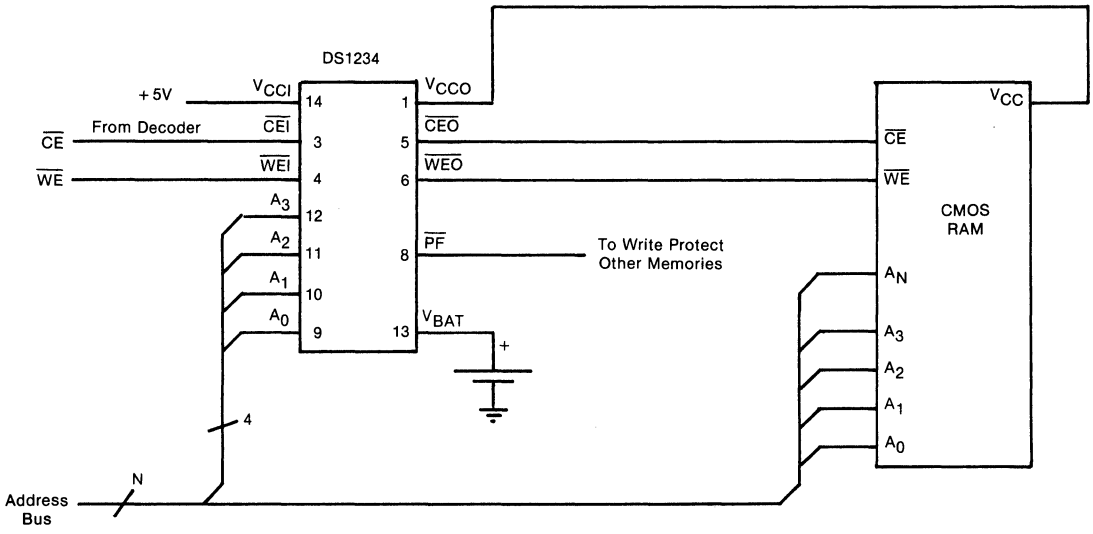
**CONTROL SELECT** Table 2

| $\overline{WE}$ | Battery Control | | | | Operation |
|---|---|---|---|---|---|
| **11** | **12** | **13** | **14** | **15** | |
| 0 | × | × | × | × | Read Only Operation |
| 1 | × | × | × | × | Read/Write Operation |
| × | 1 | 0 | 1 | 0 | Enables Nonvolatile Controller* |

× Don't Care

*Any other combination turns controller off

Figure 1


DS1234
+5V
VCCI
14
VCCO
1
From Decoder
CE
CEI
3
CEO
5
WE
WEI
4
WEO
6
A3
12
A2
11
PF
8
To Write Protect
Other Memories
A1
10
A0
9
VBAT
13
+
4
N
Address
Bus
VCC
CE
WE
CMOS
RAM
AN
A3
A2
A1
A0

10

## ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground −0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CCI}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input High Voltage | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1 |
| Input Low Voltage | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| Battery Voltage | $V_{BAT}$ | 2.5 | | 3.7 | V | |

## D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}=5V\pm10\%$)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CCI}$ | | | 5 | mA | 2 |
| Supply Current @ $V_{CCO}=V_{CCI}-0.2$ | $I_{CCO}$ | | | 80 | mA | 3 |
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | uA | |
| Output Leakage | $I_{LO}$ | −1.0 | | +1.0 | uA | |
| Output Current @2.4V | $I_{OH}$ | −1.0 | | | mA | 4 |
| Output Current @ 0.4V | $I_{OL}$ | | | 4.0 | mA | 4 |

(0°C to 70°C, $V_{CCI} < V_{BAT}$)

| | | | | | | |
|---|---|---|---|---|---|---|
| $\overline{CEO}$, $\overline{WEO}$ Output | $V_{OHL}$ | $V_{BAT}-0.2$ | | | V | 6 |
| Battery Current | $I_{BAT}$ | | | 0.1 | uA | 7 |
| Battery Backup Current @$V_{CCO}=V_{BAT}-0.3V$ | $I_{CCO1}$ | | | 100 | uA | 5 |

**CAPACITANCE** ($t_A = 25°C$)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 7 | pF | |

**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Address Setup | $t_{AS}$ | 0 | | | ns | |
| Address Hold | $t_{AH}$ | 50 | | | ns | |
| Read Recovery | $t_{RR}$ | 40 | | | ns | |
| $\overline{CEI}$ Pulse Width | $t_{CW}$ | 110 | | | ns | |
| Propagation Delay | $t_{PD}$ | | | 20 | ns | |

(0°C to 70°C, $V_{CCI} < V_{TP}$)

| | | | | | | |
|---|---|---|---|---|---|---|
| Recovery at Power Up | $t_{REC}$ | | | 2 | ms | |
| $V_{CC}$ Slew Rate Power Down | $t_F$ | 0 | | | *us* | |
| $V_{CC}$ Slew Rate Power Up | $t_R$ | 0 | | | *us* | |
| $\overline{CEI}$ High to Power Fail | $t_{PF}$ | 0 | | | ns | |

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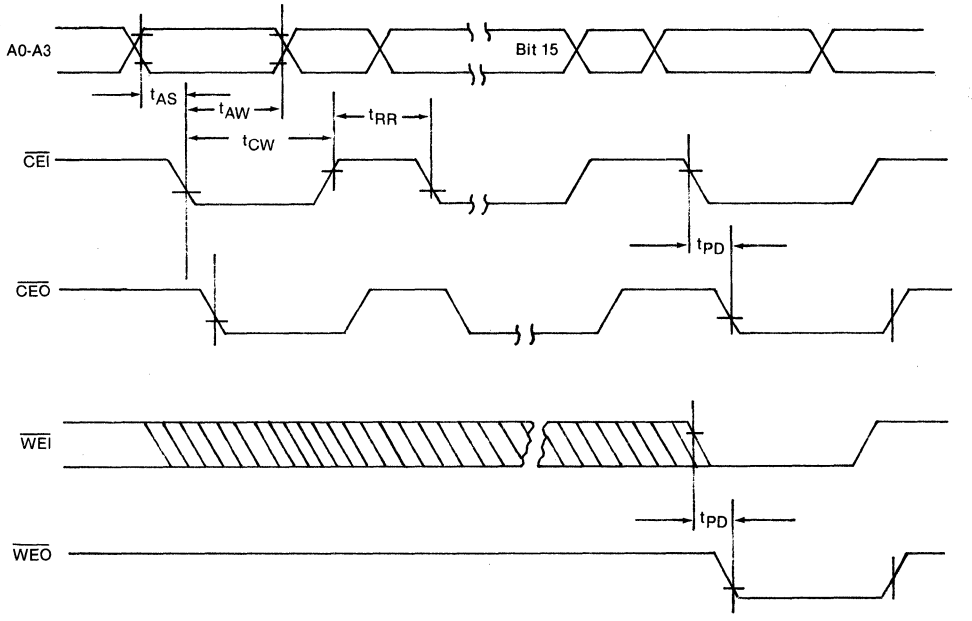
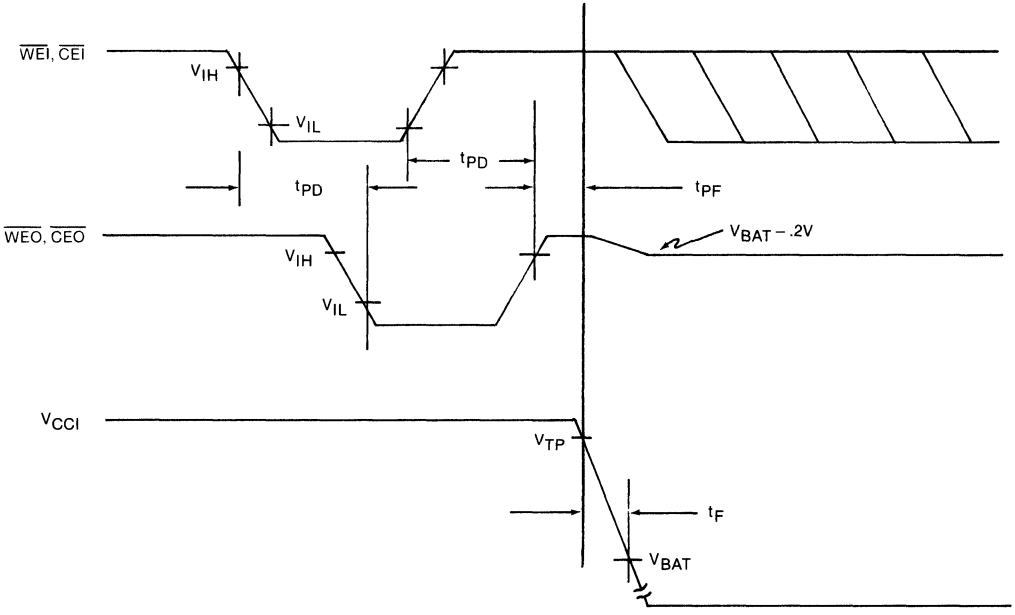
## TIMING DIAGRAM—SWITCH SETTING

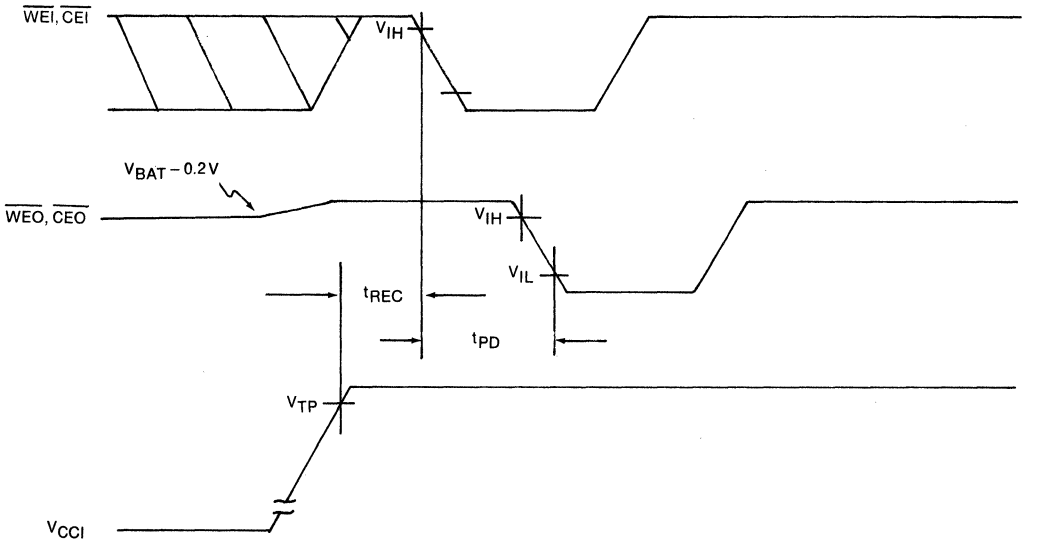


## TIMING DIAGRAM—POWER DOWN




10

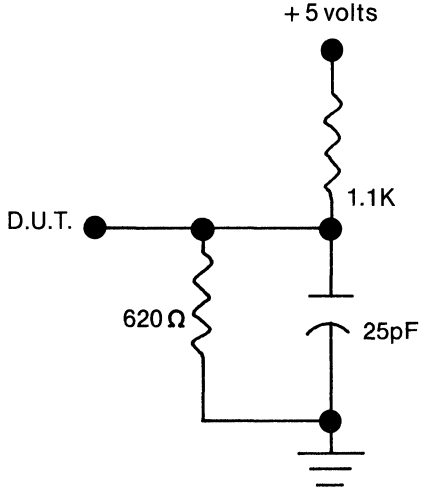
## TIMING DIAGRAM—POWER UP



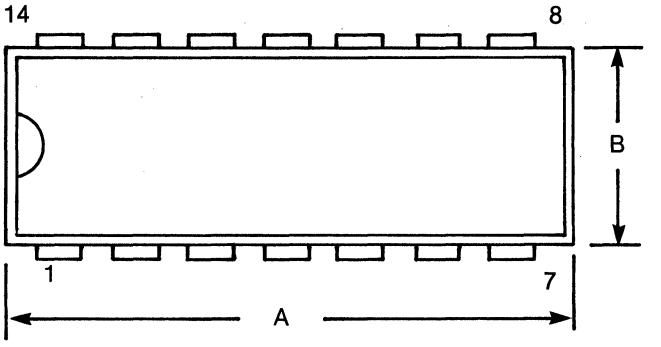
**NOTES:**

1. All voltages are referenced to ground.
2. Measured with $V_{CCO}$, $\overline{CE0}$ and $\overline{WE0}$ open.
3. $I_{CCO}$ is the maximum average load which the DS1234 can supply to the memories.
4. Measured with a load as shown in Figure 2.
5. $I_{CC01}$ is the maximum average load current which the DS1234 can supply to the memories in the battery back-up mode.
6. Chip Enable, $\overline{CEO}$, and Write Enable, $\overline{WEO}$, outputs can only sustain leakage current in the battery back-up mode.
7. $I_{BAT}$ is the total load current which the DS1234 uses from the battery input pin with $V_{CCO}$, $\overline{CEO}$, and $\overline{WEO}$ open.

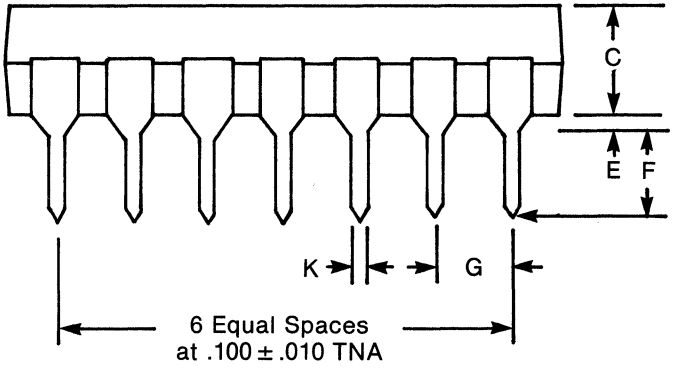
**OUTPUT LOAD** Figure 2

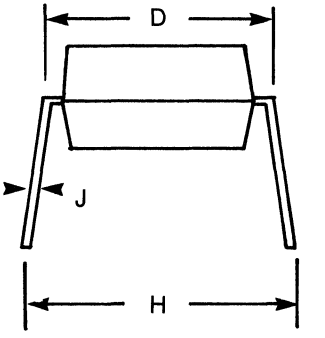


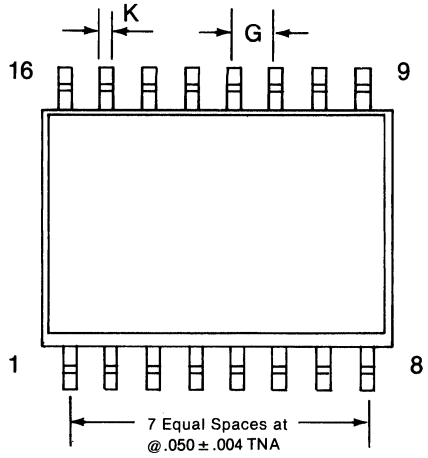
# Conditional Nonvolatile Controller
# DS1234



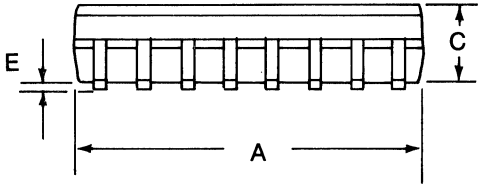

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .740 | .780 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |

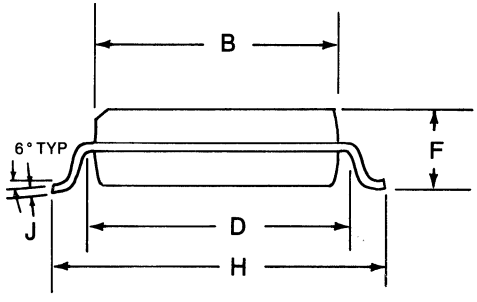





| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



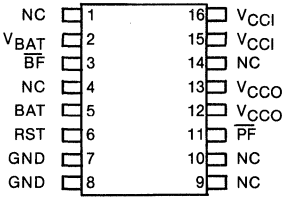
# Dallas Semiconductor
## *Battery Manager*

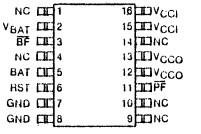
# *DS1259—16-Pin DIP*
# *DS1259S—16-Pin SOIC*

### FEATURES

- Facilitates uninterruptable power
- Uses battery only when primary $V_{CC}$ is not available
- Low forward voltage drop
- Power fail signal interrupts processor or write protects memory
- Consumes less than 100 nA of battery current
- Low battery warning signal
- Battery can be electrically disconnected upon command
- Battery will automatically reconnect when $V_{CC}$ is applied
- Mates directly with DS1212 Controller to back up 16 RAMs
- Optional 16-pin SOIC surface mount package

### PIN CONNECTIONS




### PIN NAMES

NC - No Connection
$V_{BAT}$ - Battery Input Connection
$\overline{BF}$ - Battery Fail Output Signal
BAT - Battery Output
RST - Reset Ground Signal
GND - Ground
$\overline{PF}$ - Power Fail Output Signal
$V_{CCO}$ - RAM Supply
$V_{CCI}$ - +5 V Supply

### DESCRIPTION

The DS1259 is a low-cost battery management system for portable and nonvolatile electronic equipment. A battery connected to the battery input pin supplies power to CMOS electronic circuits when primary power is lost through an efficient switch via the $V_{CCO}$ pins. When power is supplied from the battery, the power fail signal is active to warn electronic reset circuits of the power status. Energy loss during shipping and handling is avoided by pulsing reset, thereby causing the battery to be isolated from other elements in the circuits.

## OPERATION

During normal operation, $V_{CCI}$ (Pins 15 and 16) is the primary energy source and power is supplied to $V_{CCO}$ (Pins 12 and 13) through an internal switch at a voltage level of $V_{CCI} - 0.2$ volts@250 mA. During this time the power fail signal ($\overline{PF}$) is held high indicating valid $V_{CCI}$ voltage (see Figure 1). However, if the $V_{CCI}$ would fall below the trip point ($V_{TP}$), a level of 1.26 times the battery level ($V_{BAT}$), the power fail signal is driven low. As $V_{CCI}$ falls below the battery level, power is switched from $V_{CCI}$ to $V_{BAT}$ and the battery supplies power to the uninterruptable output ($V_{CCO}$) at $V_{BAT} - 0.2$ volts@15 mA.

On power up, as the $V_{CCI}$ supply rises above the battery, the primary energy source, $V_{CCI}$, becomes the supply. As $V_{CCI}$ rises above the trip point ($V_{TP}$), the power fail signal is driven back to the high level. During normal operation BAT (Pin 5) stays at the battery level regardless of the level of $V_{CCI}$.

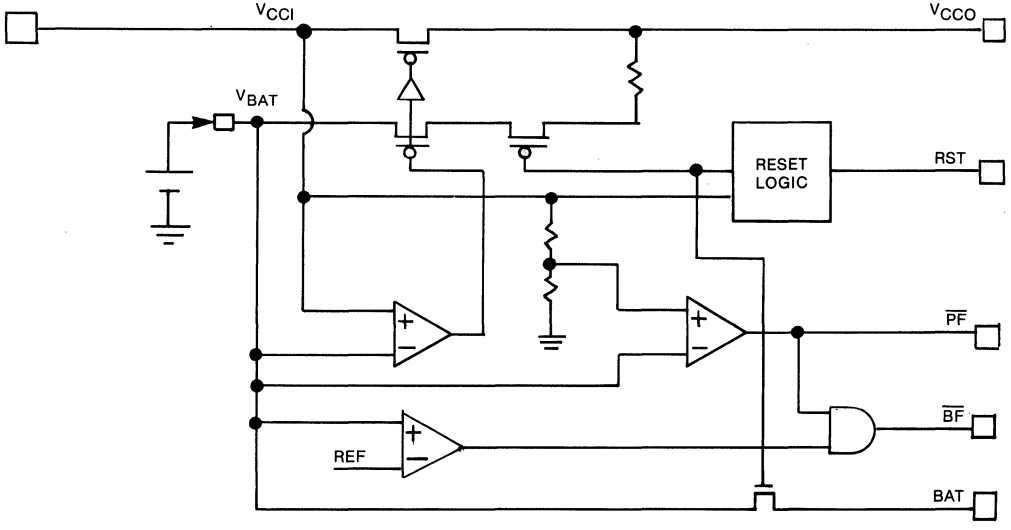
## BATTERY FAIL

When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level provided that the attached battery ($V_{BAT}$) is greater than 2 volts. If the battery level should decrease to below 2 volts, the $\overline{BF}$ signal is driven low indicating a low battery. The $\overline{BF}$ signal is always low when the $\overline{PF}$ signal is low.

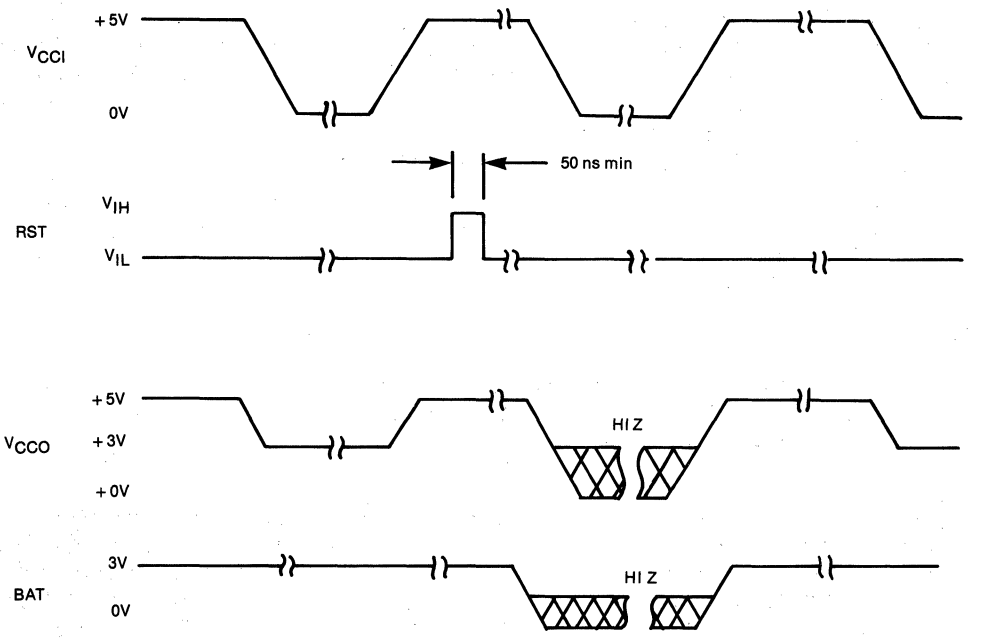
## RESET

The reset input can be used to prevent the battery from supplying power to $V_{CCO}$ and BAT even if $V_{CCI}$ falls below the level of the battery. This feature is activated by applying a pulsed input on $\overline{RST}$ to high level for 50 ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the $V_{CCO}$ output and BAT will go to the high impedance. The next time primary power is applied such that $V_{CCI}$ is greater than $V_{BAT}$, normal operation resumes and $V_{CCO}$ will be supplied by the battery or $V_{CCI}$. The BAT output will also return to the level of the battery. Figure 3 shows the DS1259 in a typical application.

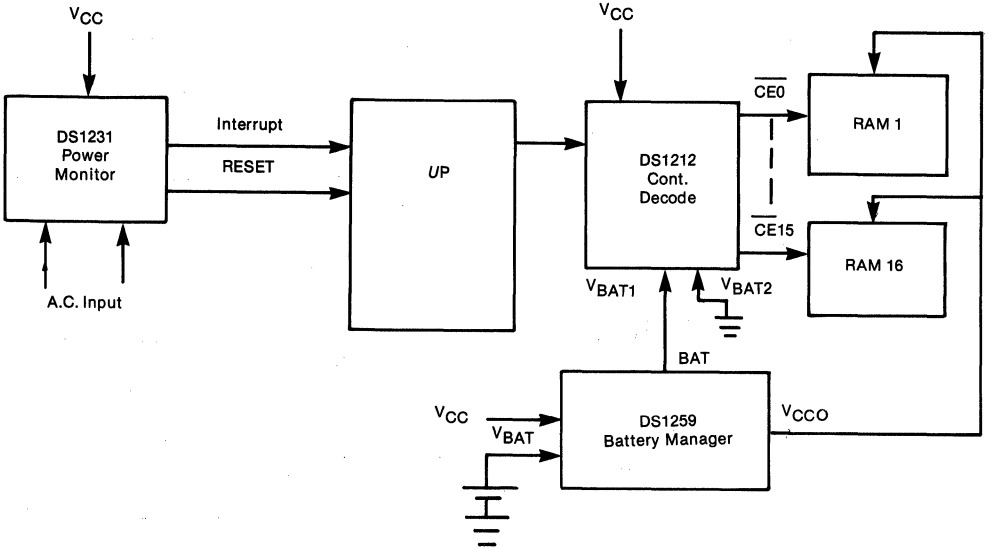
**BLOCK DIAGRAM** Figure 1



**RESET TIMING** Figure 2




**TYPICAL APPLICATION** Figure 3



**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Primary Power Supply | $V_{CCI}$ | | 5.0 | 5.5 | V | 1 |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}+0.3$ | V | 1 |
| Input Low Voltage | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| Battery Voltage Pin 2 | $V_{BAT}$ | 2.5 | 3 | 3.7 | V | 6 |
| Battery Output Pin 5 | BAT | $V_{BAT}-0.1$ | | | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Leakage Current | $I_{LO}$ | −1.0 | | +1.0 | uA | |
| Output Current @2.4V | $I_{OH}$ | −1.0 | | | mA | 1,2 |
| Output Current @0.4V | $I_{OL}$ | | | +4.0 | mA | 1,2 |
| Input Supply Current | $I_{CCI}$ | | | 10 | mA | 3 |
| Pins 12, 13 $V_{CCO} = V_{CCI}-0.2$ | $I_{CCO}$ | | | 250 | mA | |
| Pin 11 $\overline{PF}$ Detect | $V_{TP}$ | | $1.26 \times V_{BAT}$ | | V | 4,6 |
| Pin 3 $\overline{BF}$ Detect | $V_{BATF}$ | | 2.0 | | V | 7 |

(0 °C to 70 °C, $V_{CCI} < V_{BAT}$)

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Pins 12, 13 $V_{CCO} = V_{BAT} - 0.2V$ | $I_{CCO2}$ | | 15 | mA | 5 |
| Battery Leakage | $I_{BAT}$ | | 100 | nA | 8 |
| Pin 5 Battery Output Current | $I_{BAT\ OUT}$ | | 100 | uA | |

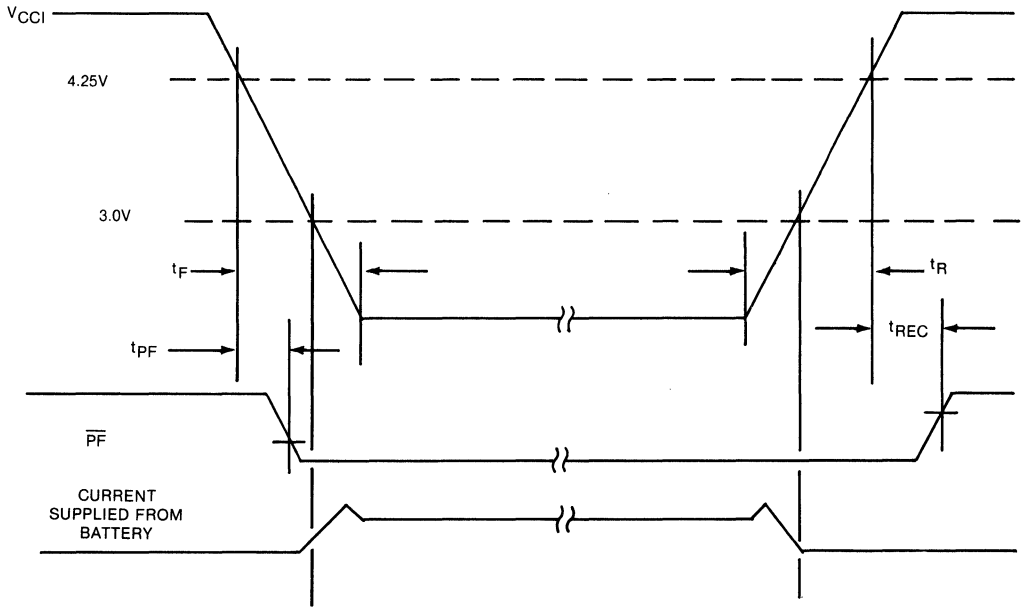
**CAPACITANCE** ($t_A = 25$ °C)

| PARAMETER | SYMBOL | TYP | MAX | UNITS |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF |
| Output Capacitance | $C_{OUT}$ | 5 | 10 | pF |

**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC} = 4.0$ to 5.5V)

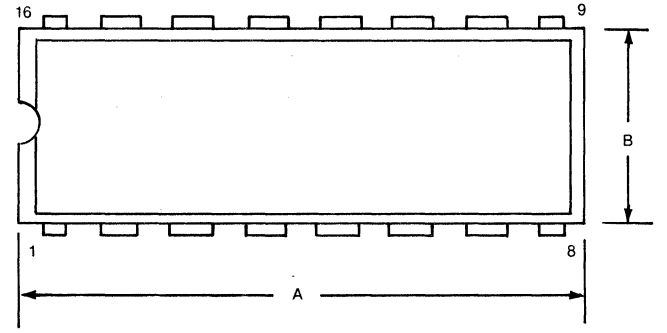
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $V_{CCI}$ Slew Rate | $t_F$ | 300 | | | us | |
| $V_{CCI}$ Slew Rate | $t_R$ | 1 | | | us | |
| Power Down to $\overline{PF}$ Low | $t_{PF}$ | 0 | | | us | |
| $\overline{PF}$ High after Power Up | $t_{REC}$ | | | 100 | us | |

## POWER-DOWN/POWER-UP CONDITION

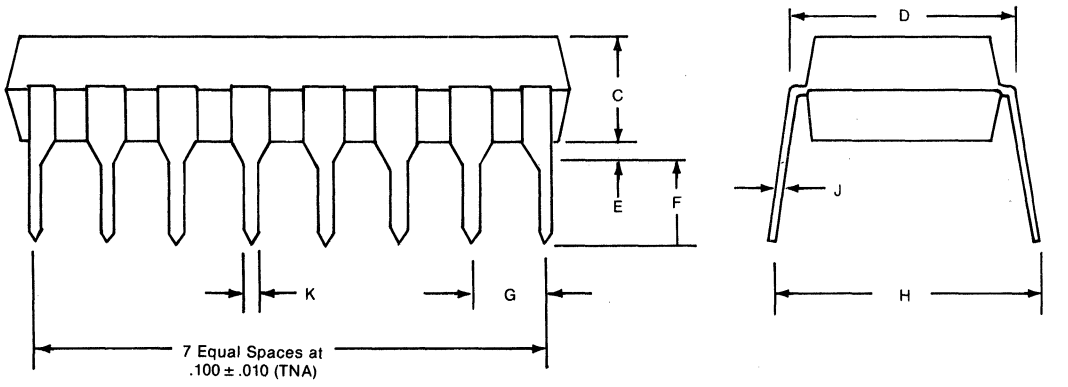


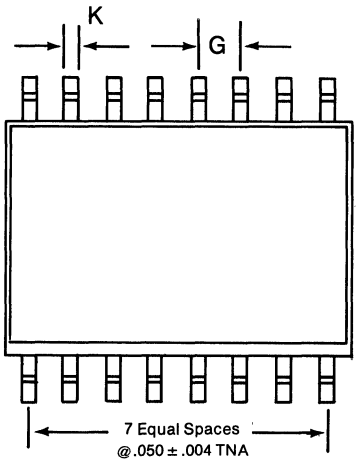

**NOTES:**

1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13 and 3 open.
4. $V_{TP}$ is the point that $\overline{PF}$ is driven low.
5. $I_{CCO2}$ may be limited by the capability of the battery.
6. Trip Point Voltage for Power Fail Detect:
   $V_{TP} = 1.26 \times V_{BAT}$
   For 5% operation: $V_{BAT} = 3.7V$ Max.
7. $V_{BATF}$ is the point that $\overline{BF}$ is driven low.
8. Battery leakage is the internal energy consumed by the DS1259.

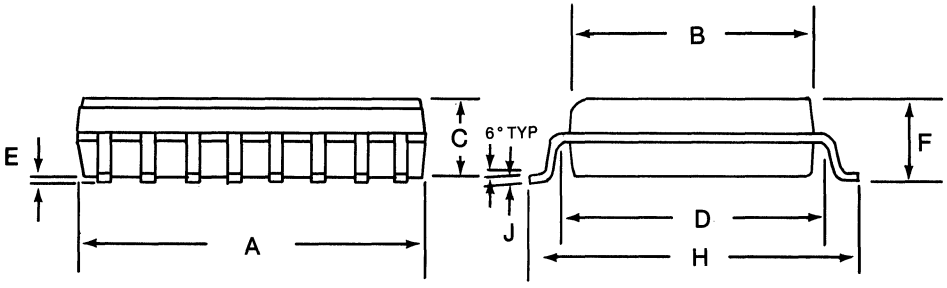



| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .740 | .780 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |






| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



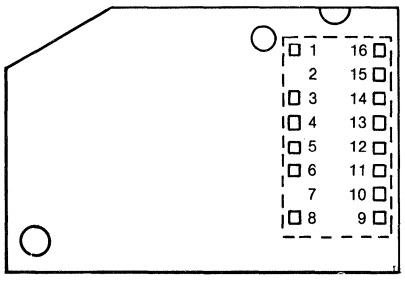
# Dallas Semiconductor
## *SmartBattery*

# *DS1260-25*
# *-50*
# *-100*

### FEATURES

- Encapsulated lithium energy cell with shelf life beyond 10 years
- Available with energy capacities of 250, 500, and 1,000 MAH @ 3 volts
- Plugs into a standard 16 pin DIP socket
- Lithium cell electrically disconnects from exposed pins upon command
- Battery isolation insures full capacity after shipping and handling
- Lithium cell automatically reconnects when $V_{CC}$ is applied
- Recessed pins prevent bending
- $V_{CC}$ fail signal interrupts processor or write protects memory
- Exhausted energy cell warning signal
- Low profile permits mounting on 0.5 inch printed circuit board centers
- Mates directly with DS1212 controller to back-up 16 SRAMs
- Uninterruptable supply for CMOS and portable devices

### PIN CONNECTIONS




### PIN NAMES

Pins, 1, 4, 9, 10 and 14 are No-Connects
Pin 2 and pin 7 are missing
Pin 3 is Battery Fail ($\overline{BF}$)
Pin 5 is Battery Out (BAT)
Pin 6 is RESET (RST)
Pin 8 is Ground
Pin 11 is Power Fail ($\overline{PF}$)
Pins 12 and 13 are RAM Supply ($V_{CCO}$)
Pins 15 and 16 are +5V Supply ($V_{CCI}$)

### DESCRIPTION

The DS1260 is a low cost backup energy source for portable and nonvolatile electronic equipment. A lithium energy source of up to 1 amp hour can supply power to CMOS electronic circuits when primary power is lost through an intelligent and efficient switch. When power is supplied from the lithium power source, the power fail signal is held low to warn electronic RESET circuits of the power status. Energy loss during shipping and handling is avoided by pulsing RESET, thereby causing the backup energy source to be isolated from the exposed pins. The DS1260 can be plugged into a standard 16-pin low-cost DIP socket, allowing for proven interconnect and simple replacement if the energy has been exhausted.

## OPERATION

During normal operation $V_{CCI}$ (Pins 15 and 16) is the primary energy source and power is supplied to $V_{CCO}$ (Pins 12 and 13) through an internal switch at a voltage level of $V_{CCI} - 0.2$ volts @ 250 ma. During this time the power fail signal $\overline{PF}$ is held high indicating valid primary voltage (see Figure 1). However, if the $V_{CCI}$ would fall below the level of 4.25 volts, the power fail signal is driven low. As $V_{CCI}$ falls below the level of the lithium supply ($V_{BAT} = 3$ volts) power is switched and the lithium energy source supplies power to the uninterruptable output ($V_{CCO}$) at $V_{BAT} - 0.2$ volts @ 5 MA.

On power up, as the $V_{CCI}$ supply rises above 3 volts, the primary energy source, $V_{CCI}$, becomes the supply. As the $V_{CCI}$ input rises above 4.25 volts the power fail signal is driven back to the high level. During normal operation BAT (Pin 5) stays at the battery level of 3 volts, regardless of the level of $V_{CCI}$.

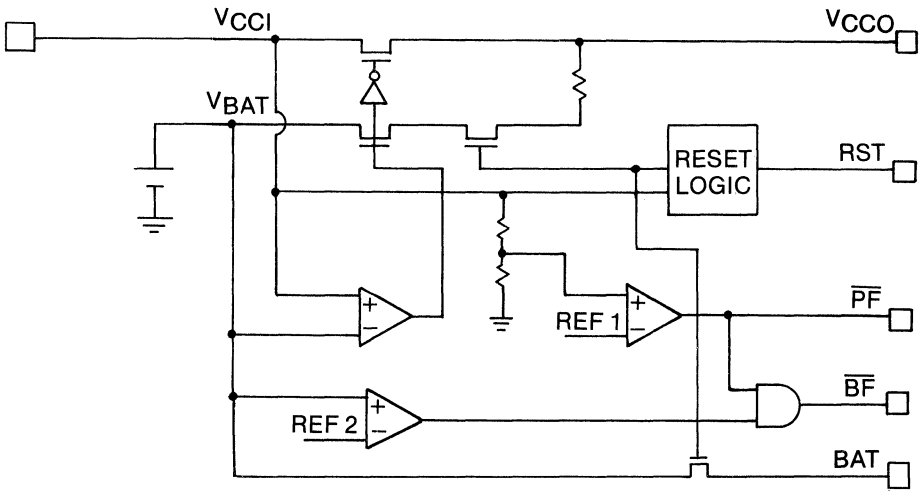
## BATTERY FAIL

When power is being supplied from the primary energy source, $\overline{BF}$ (Pin 3) is held at a high level ($V_{OH}$) provided that the lithium energy source is greater than 2 volts. If the lithium energy source should decrease to below 2 volts, the $\overline{BF}$ signal is driven low ($V_{OL}$), indicating an exhausted lithium battery. The $\overline{BF}$ signal is always low when power is being supplied by the lithium energy source.

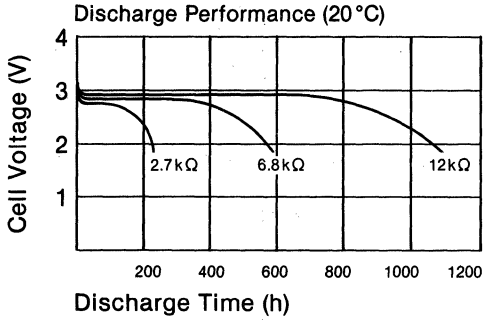
## RESET

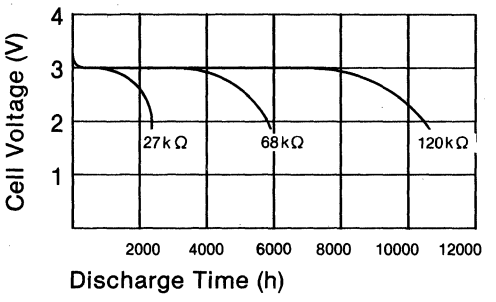
The reset input can be used to prevent the lithium energy source from supplying power to $V_{CCO}$ and BAT even if $V_{CCI}$ falls below 3 volts. This feature is activated by applying a pulsed input on RST to high level ($V_{IH}$) for 50 ns min. while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the $V_{CCO}$ output and BAT will go to high impedance. The next time primary power is applied, such that $V_{CCI}$ is greater than $V_{BAT}$, normal operation resumes and $V_{CCO}$ will be supplied by the lithium energy source when $V_{CCI}$ again falls below 3 volts. BAT will also return to the level $V_{BAT}$. Figure 3 shows how the SmartBattery is used in a system application.

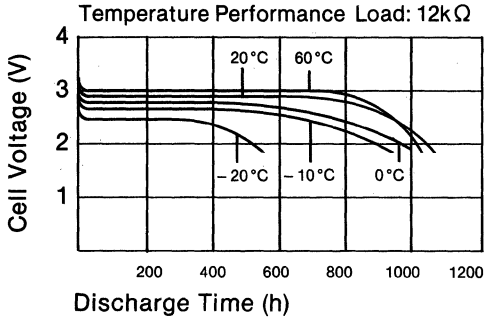
**BLOCK DIAGRAM** Figure 1

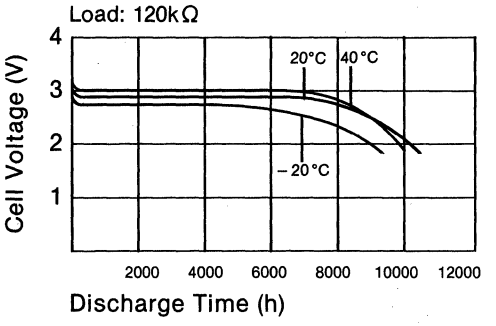


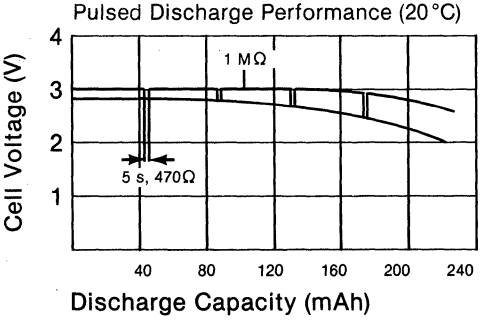
## BATTERY PERFORMANCE DS1260-25



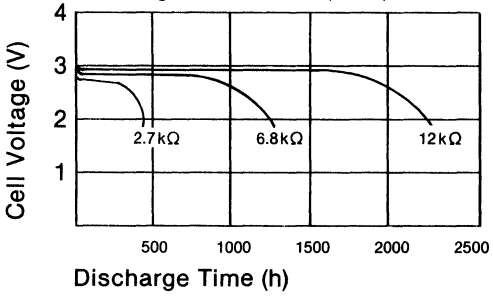



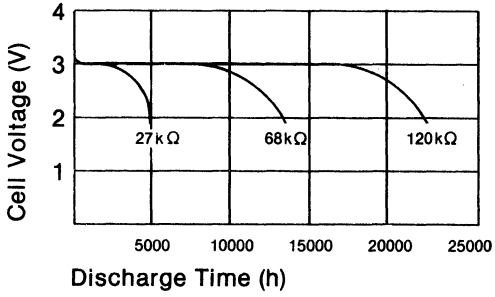



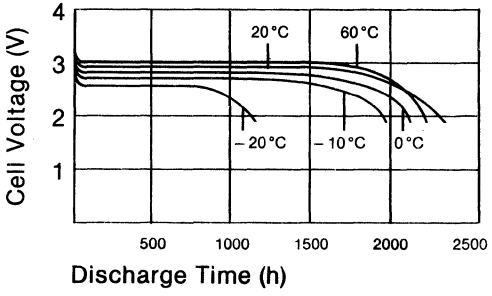
## BATTERY PERFORMANCE DS1260-50

Discharge Performance (20 °C)

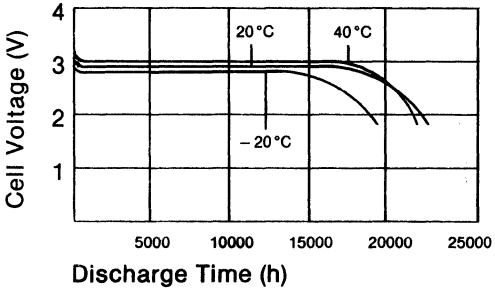


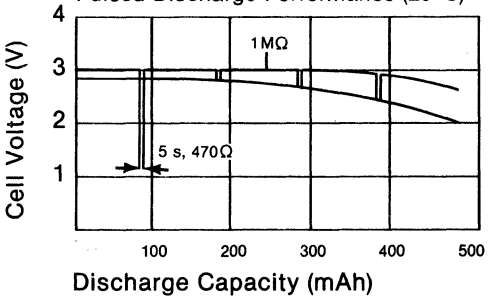

Temperature Performance Load: 12kΩ



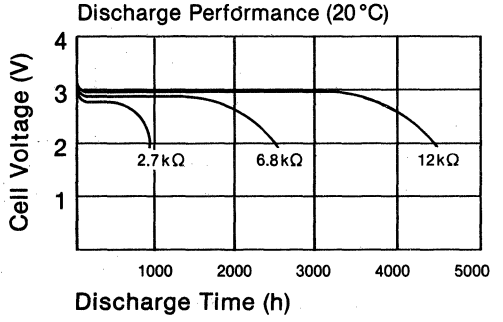

Load: 120kΩ

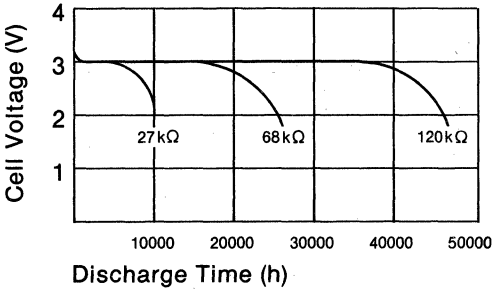


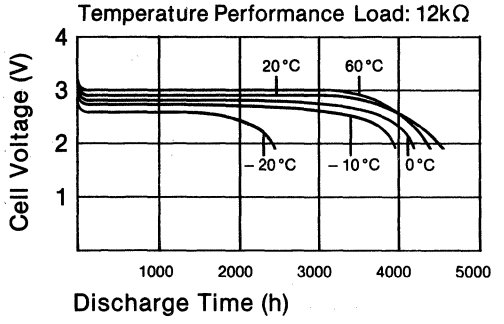

Pulsed Discharge Performance (20 °C)

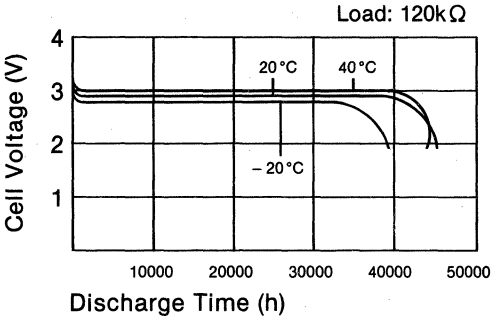


## BATTERY PERFORMANCE DS1260-100



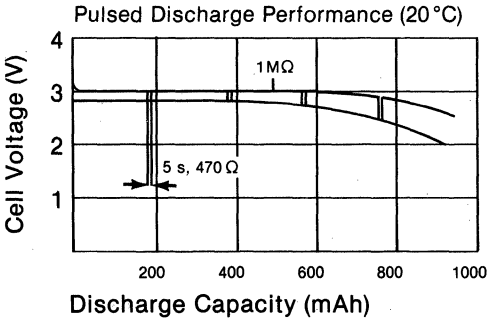
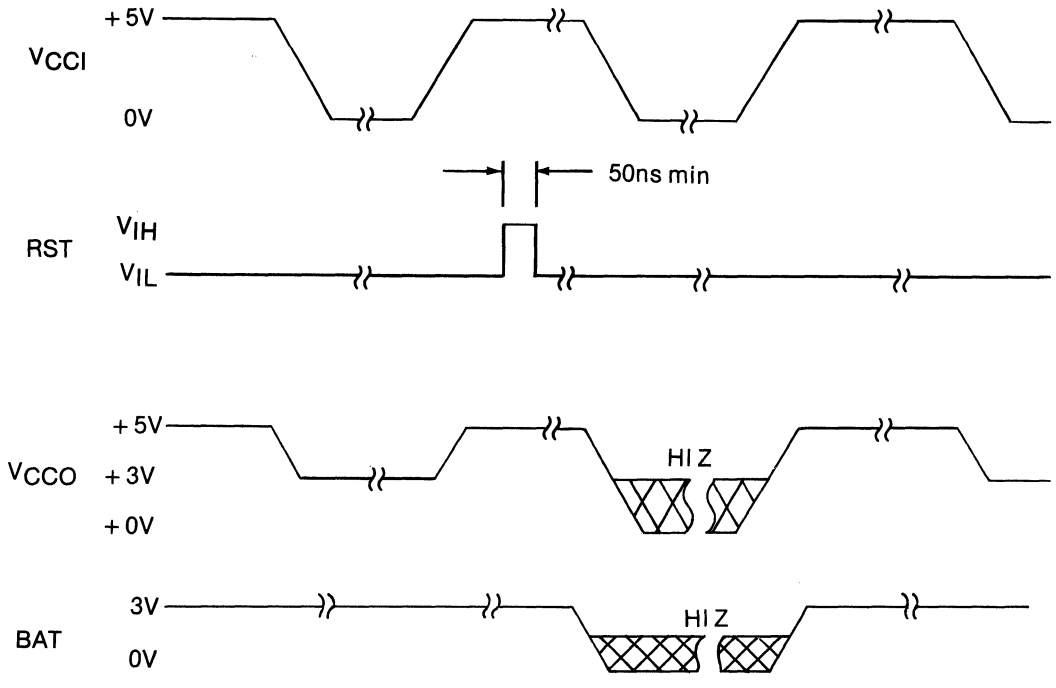



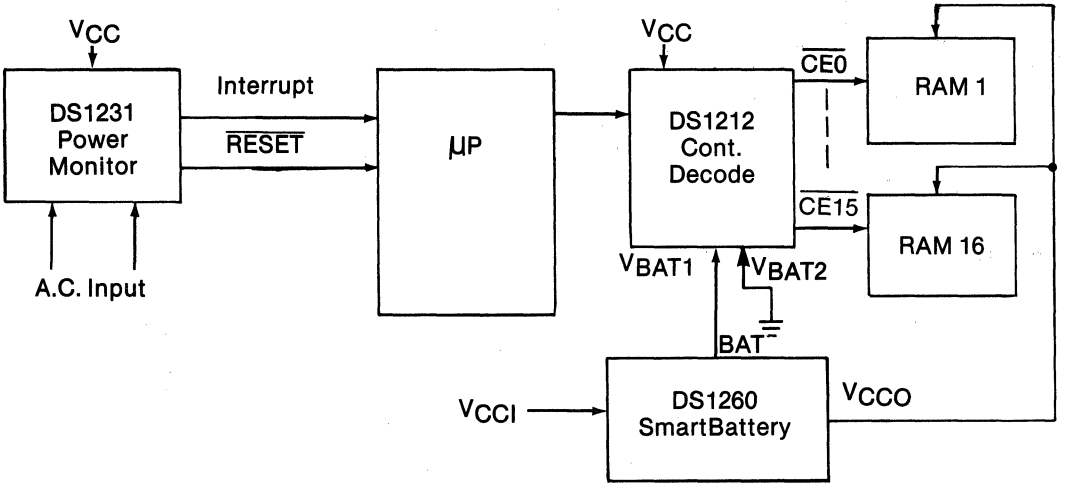
**TABLE I**

| PART NO. | CAPACITY | NOMINAL VOLTAGE |
|---|---|---|
| DS1260-25 | 250 MAH | 3 volts |
| DS1260-50 | 480 MAH | 3 volts |
| DS1260-100 | 960 MAH | 3 volts |

**FIGURE 2**



**INTEGRATED BATTERY BACKUP—APPLICATIONS** Figure 3



**ABSOLUTE MAXIMUM RATINGS***

Voltage on Any Pin Relative to Ground −0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature −40°C to +70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Primary Power Supply | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CCI}+0.3$ | V | 1 |
| Input Low Voltage | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CCI}$ = 4.0 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Leakage Current | $I_{LO}$ | −1.0 | | +1.0 | uA | |
| Output Current @ 2.4V | $I_{OH}$ | −1.0 | | | mA | 1,2 |
| Output Current @ 0.4V | $I_{OL}$ | | | +4.0 | mA | 1,2 |
| Input Supply Current | $I_{CCI}$ | | | 5 | mA | 3 |
| Pins 12,13 $V_{CCO} = V_{CCI} - 0.2$ | $I_{CCO}$ | | | 250 | mA | |
| Pin 11 $\overline{PF}$ Detect | $V_{TP}$ | | 4.25 | 4.5 | V | 4 |
| Pin 3 $\overline{BF}$ Detect | $V_{BATF}$ | | 2.0 | | V | 7 |

(0°C to 70°C, $V_{CCI} < V_{BAT}$)

| | | | | | | |
|---|---|---|---|---|---|---|
| Battery Voltage Pin 5 | $V_{BAT}$ | | 3 | | V | 6 |
| Pins 12, 13 $V_{CCO} = V_{BAT} - 0.2V$ | $I_{CCO2}$ | | | 15 | mA | 5 |
| Battery Leakage | $I_{BAT}$ | | | 100 | nA | 8,9 |
| Pin 5 Battery Output Current | $I_{BAT\ OUT}$ | | | 100 | uA | |

10

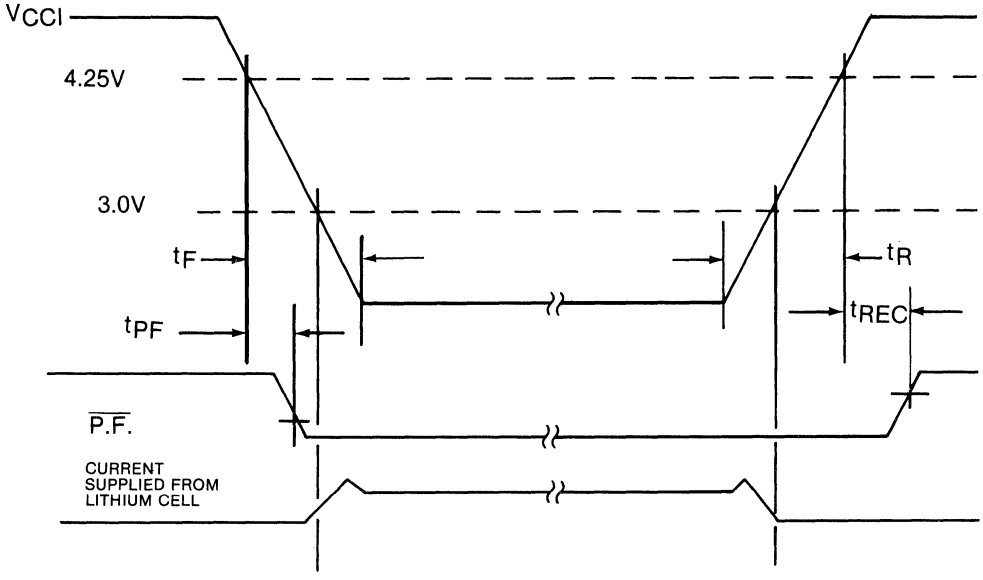
**CAPACITANCE** ($t_A = 25\,°C$)

| PARAMETER | SYMBOL | TYP | MAX | UNITS |
|---|---|---|---|---|
| Output Capacitance | $C_O$ | 5 | 10 | pF |
| Input Capacitance | $C_I$ | 5 | 10 | pF |

**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC} = 4.0$ to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $V_{CCI}$ Slew Rate | $t_F$ | 300 | | | µs | |
| $V_{CCI}$ Slew Rate | $t_R$ | 1 | | | µs | |
| Power Down to $\overline{PF}$ Low | $t_{PF}$ | 0 | | | µs | |
| $\overline{PF}$ High after Power Up | $t_{REC}$ | | | 100 | µs | |

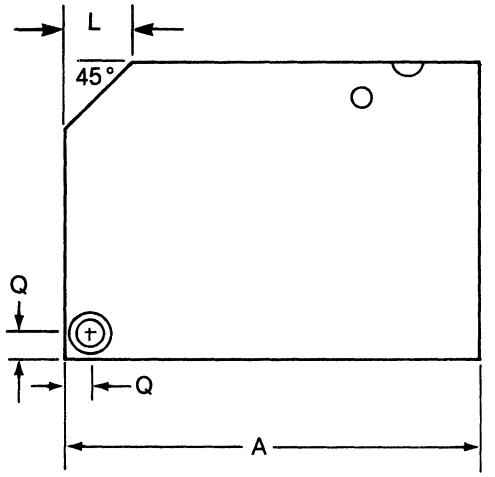
**POWER-DOWN/POWER-UP CONDITION**



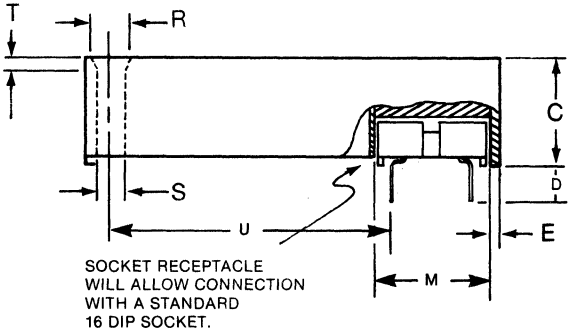

**NOTES:**

1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13 and 3 open.
4. $V_{TP}$ is the point that $\overline{PF}$ is driven low.
5. Sustained $I_{CCO2}$ currents above 1 mA cause a significant drop in battery voltage.
6. $V_{BAT}$ is the internal lithium energy source voltage.
7. $V_{BATF}$ is the point that $\overline{BF}$ is driven low.
8. Battery leakage is the internal energy consumed by the DS1260.
9. Storage loss is less than 1% per year at 25°C.
10. $V_{CCI}$ = +5 volts; $t_A$ = 25°C.

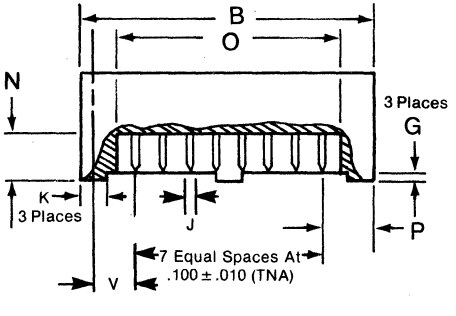
# DS1260 - 25
# - 50
# - 100
# SmartBattery




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.480 | 1.500 |
| B | 1.030 | 1.050 |
| C | .390 | .410 |
| D | .120 | .140 |
| E | .020 | .040 |
| G | .020 | .040 |
| J | .022 | .026 |
| K | .090 | .110 |
| L | .240 | .260 |
| M | .420 | .440 |
| N | .165 | .175 |
| O | .800 | .810 |
| P | .160 | .180 |
| Q | .098 | .109 |
| R | .165 | .175 |
| S | .115 | .125 |
| T | .052 | .058 |
| U | .980 | 1.000 |
| V | .055 | .075 |




SOCKET RECEPTACLE
WILL ALLOW CONNECTION
WITH A STANDARD
16 DIP SOCKET.
BURNDY DILB16P.-11T
SUPPLIED WITH EACH ORDER.




SOCKET NOT SHOWN

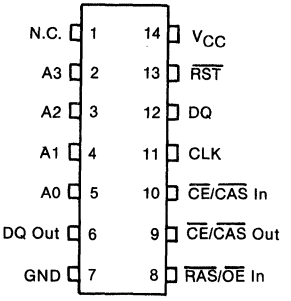
# System Extension

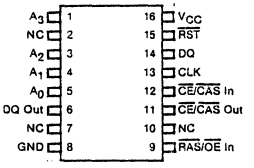
# Dallas Semiconductor
## *Phantom Interface*

# *DS1206—14-Pin DIP*
# *DS1206S—16-Pin SOIC*

### FEATURES
- Minimum expense add-on serial port
- Converts standard bytewide or DRAM memory wave forms into a three wire serial port
- Operation is transparent to memory
- Software generated memory cycles activate serial port and transfer data
- High band width—1bit data transfer per 2 memory cycles
- Intercepts memory signals so that pass through connections can be maintained to memory
- Controls communications for as many as ten DS1201 Tags, DS1204U Keys, DS1207 TimeKeys or DS1290 Eliminators
- Low power CMOS circuitry
- Optional 16-pin SOIC surface mount package

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| N.C. | - No connection |
| A0-A3 | - Memory address bus |
| DQ Out | - Data out to memory bus |
| GND | - Ground |
| $\overline{RAS}/\overline{OE}$ In | - $\overline{RAS}$ Input from memory bus |
| $\overline{CE}/\overline{CAS}$ Out | - Chip enable or $\overline{CAS}$ to memory |
| $\overline{CE}/\overline{CAS}$ In | - Chip enable or $\overline{CAS}$ from memory bus |
| CLK | - Clock for serial port |
| DQ | - Data I/O for serial port |
| $\overline{RST}$ | - Reset for serial port |
| $V_{CC}$ | - +5 Volts |

### DESCRIPTION
The Phantom Interface is a CMOS circuit which intercepts the standardized memory bus found in computer systems and adapts the bus to a three wire serial port. Multiple memory cycles are used as a basis for generating the appropriate signals to control the serial port. In this way, a sequence of software generated memory cycles encode commands and transfer data with low pin count. The serial port signaling is derived from the memory address bus

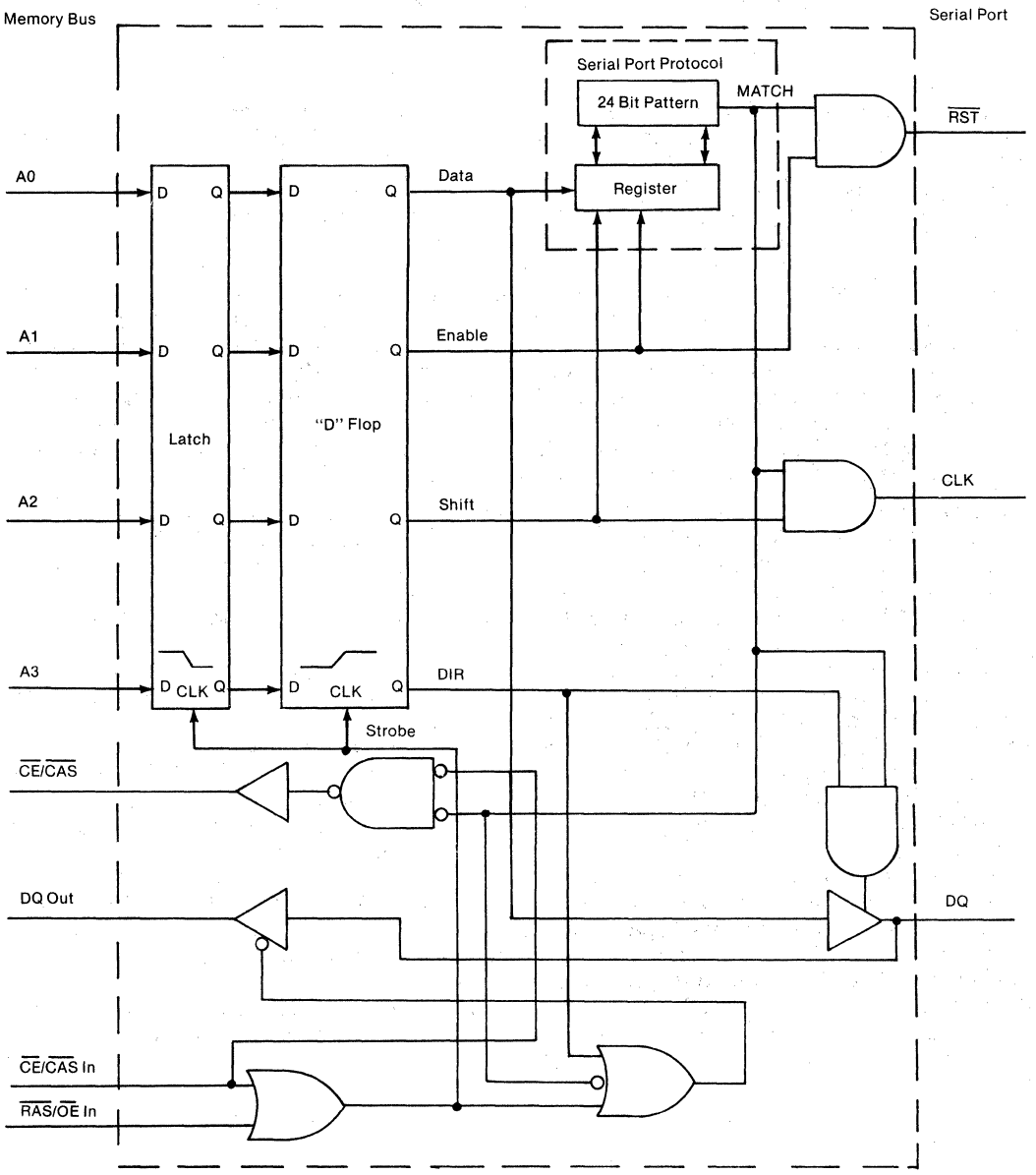
lines A0 through A3, the $\overline{CE}/\overline{CAS}$ signal and $\overline{RAS}/\overline{OE}$ signal, without affecting address space, thereby maintaining transparency to the memory bus. Communication is established under software control by an address pattern recognition sequence (serial port protocol) which disables a ByteWide or DRAM memory via $\overline{CE}/\overline{CAS}$ output. An additional address sequence is required to generate the three wire port signals: $\overline{RESET}$ ($\overline{RST}$), Data (DQ), and Clock (CLK). The add-on serial port provides a minimum cost interface to the DS1201 Tag, the DS1204U Key, the DS1207 TimeKey, the DS1223 Configurator and the DS1290 Eliminator.

**OPERATION**

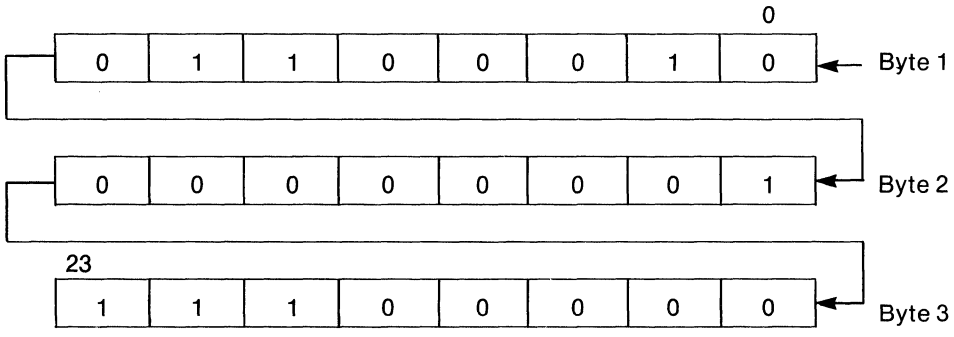
The main parts of the phantom serial interface are shown in the block diagram of Figure 1. Information presented on address inputs are latched into the DS1206 on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}/\overline{CAS}$ In and $\overline{RAS}/\overline{OE}$ In. When redirecting information from a DRAM memory bus, both $\overline{RAS}$ and $\overline{CAS}$ inputs are required and the column addresses are used for signaling. For a ByteWide memory bus, only a $\overline{CE}$ input is required and the $\overline{RAS}/\overline{OE}$ input can be tied low or connected to the memory $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 24-bit serial interface protocol and to logic which will generate signals for the serial port. The serial interface protocol is derived from address inputs A0, A1, and A2. A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially A1 input must be set high to enable serial interface communications. A1 must remain high during the pattern recognition sequence and subsequent communications with the serial port after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and future access to the serial port is denied.

Data transfer through the serial interface occurs by matching a 24 bit pattern as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Therefore, data is input for comparison to the serial interface protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24 bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24 bit register for comparison to the 24 bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles. The first memory cycle sets A2 low, establishing the shift clock low. The second memory cycle sets A2 high, causing the transition necessary to shift a bit of data into the 24 bit register. Data on A0 is kept at the correct level for both memory cycles. Address input A3 is used to control the direction of data going to and from the serial port. This input is not used during pattern recognition of the protocol. After the 24 bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for the serial port. The match signal is also used to disable Chip Enable to the memory bus and enable a gate which allows the serial port DQ to drive the DQ out line to the memory bus. When $\overline{RST}$ is driven high, devices attached to the serial port become active. Subsequent shift signals derived from A2 will now be recognized as the serial port clock. The data signal for the serial bus is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on the serial port DQ. When A3 is set low, devices attached to the serial port can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the serial port DQ.

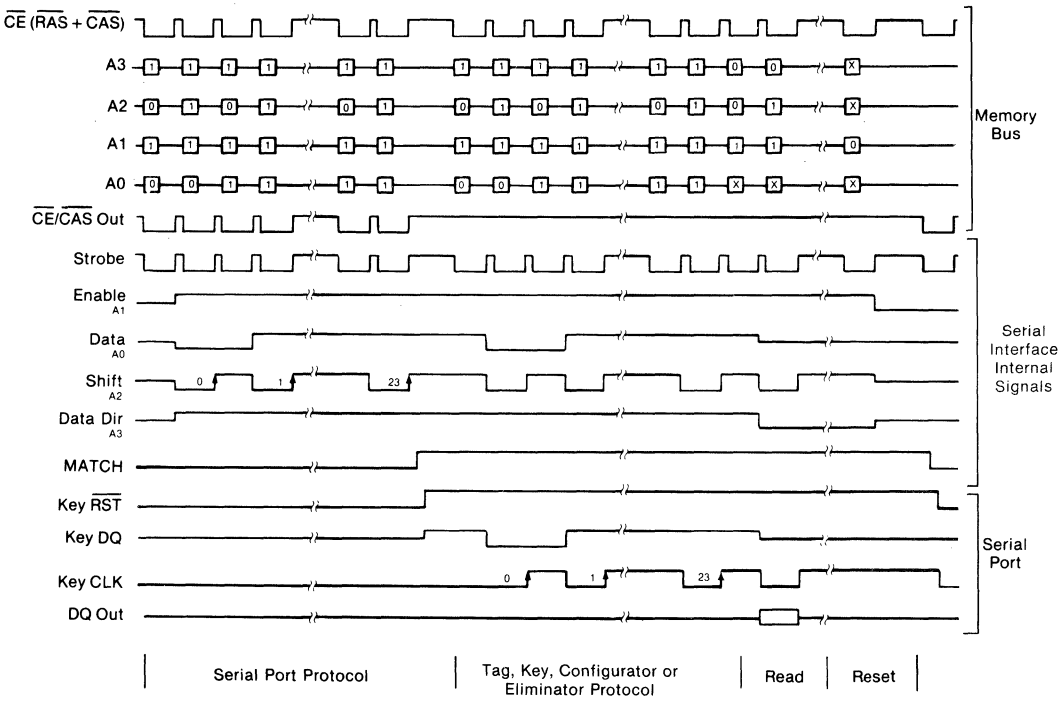
**PHANTOM SERIAL INTERFACE BLOCK DIAGRAM** Figure 1



**SERIAL INTERFACE 24-BIT PROTOCOL** Figure 2




**PHANTOM SERIAL INTERFACE SIGNALS** Figure 3



**ABSOLUTE MAXIMUM RATINGS***

| | | |
|---|---|---|
| VOLTAGE ON ANY PIN RELATIVE TO GROUND | — | −1.0V to +7V |
| OPERATING TEMPERATURE | — | 0°C to +70°C |
| STORAGE TEMPERATURE | — | −55°C to +125°C |

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | $V_{CC}+0.3$ | V | 1 |
| Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| Supply | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | −1 | | 1 | μA | |
| Output Leakage | $I_{LO}$ | | | 1 | μA | |
| Output Current @2.4V | $I_{OH}$ | −1 | | | mA | |
| Output Current @ .4V | $I_{OL}$ | +4 | | | mA | |
| $\overline{RST}$ Output Current @3.8V | $I_{OHR}$ | 16 | | | mA | |
| Supply Current | $I_{CC}$ | | | 6 | mA | 2 |

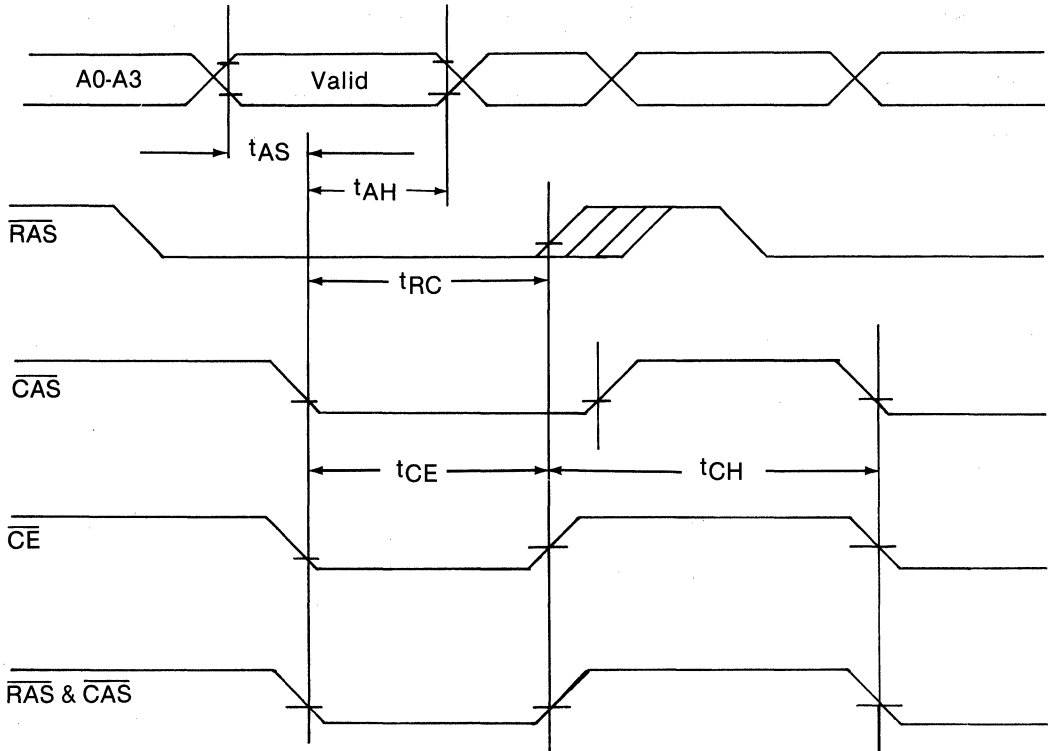
**CAPACITANCE** ($t_A = 25°C$)

| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output | $C_{I/O}$ | 5 | 10 | pF | |

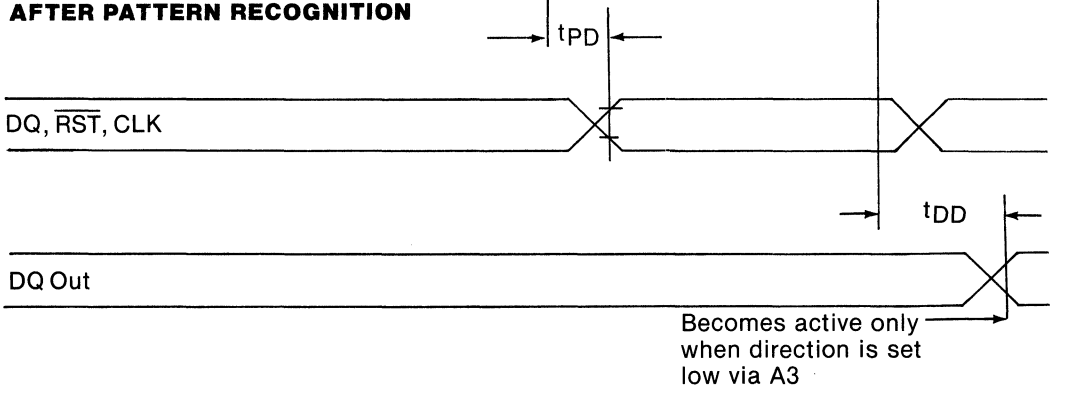
**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Address Set Up | $t_{AS}$ | 0 | | | ns | |
| Address Hold | $t_{AH}$ | 50 | | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Overlap | $t_{RC}$ | 60 | | | ns | |
| $\overline{CE}$ Pulse Width | $t_{CE}$ | 60 | | | ns | |
| Key Signals Valid | $t_{PD}$ | | | 60 | ns | 3 |
| Key Data Out | $t_{DD}$ | 10 | | | ns | 3 |
| $\overline{CE}$ Inactive | $t_{CH}$ | 30 | | | ns | |

**MEMORY BUS INPUTS**

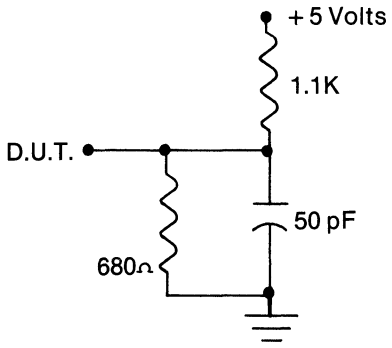



**SERIAL PORT**
**AFTER PATTERN RECOGNITION**

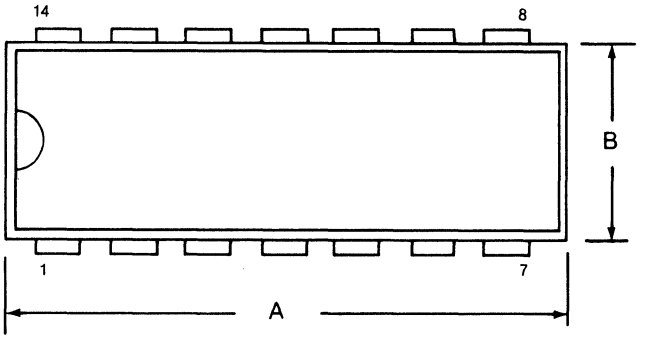


**NOTES:**
1. All voltages are referenced to ground
2. Measured with outputs open
3. Measured with a load as shown in Figure 4

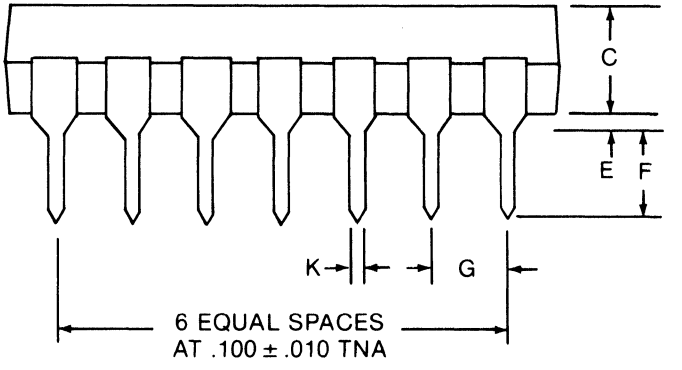
**OUTPUT LOAD** Figure 4

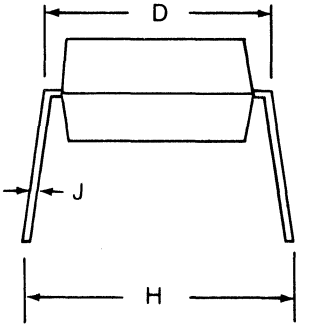


# *Phantom Serial Interface DS1206*

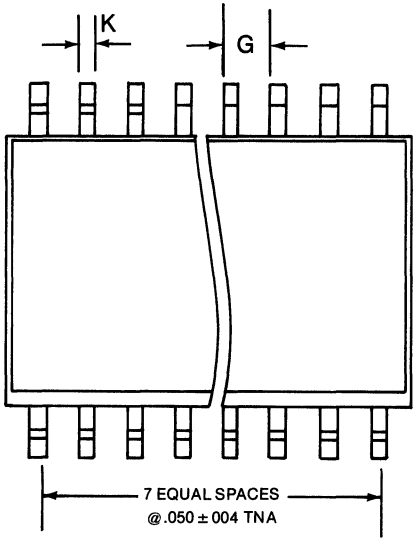



| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .740 | .780 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |

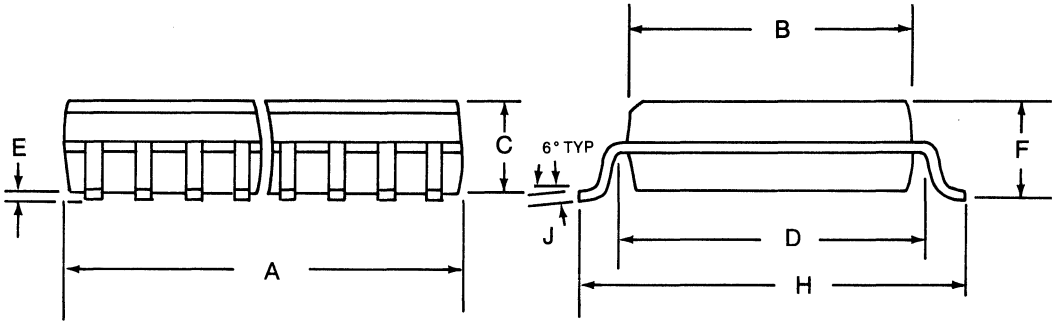


# Phantom Serial Interface
# DS1206S




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



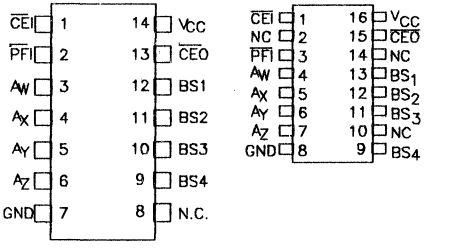

11

# Dallas Semiconductor
## *BankSwitch*

# *DS1222—14-Pin DIP*
# *DS1222S—16-Pin SOIC*

### FEATURES
- Provides bank switching for 16 banks of memory
- Bank switching is software controlled by a pattern recognition sequence on four address inputs
- Automatically sets all 16 banks off on power up
- Bank switching logic allows only one bank on at a time
- Special custom recognition patterns are available which can prevent unauthorized access
- Full ±10% operating range
- Low power CMOS circuitry
- Can be used to expand the address range of microprocessors and decoders
- Optional 16-pin SOIC surface mount package

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $A_W$ - $A_Z$ | - Address Inputs |
| $\overline{CEI}$ | - Chip Enable Input |
| $\overline{CEO}$ | - Chip Enable Output |
| N.C. | - No Connection |
| BS1, BS2, BS3, BS4 | - Bank Select Outputs |
| $\overline{PFI}$ | - Power Fail Input |
| $V_{CC}$ | - +5 Volts |
| GND | - Ground |

### DESCRIPTION
The DS1222 is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Special custom patterns are available from Dallas Semiconductor which can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212, up to 16 banks of static RAMs can be selected.

## OPERATION—BANK SWITCHING

Initially, on power up all four bank select outputs are low and the chip enable output ($\overline{CEO}$) is held high. Note: the power fail input ($\overline{PFI}$) must be low prior to power-up to assure proper initialization. Bank switching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which will set the bank switch, a read cycle of 1111 on address inputs $A_W$ through $A_Z$ should be executed to guarantee that pattern entry starts with Bit 0. Each set of address inputs is clocked into the DS1222 when $\overline{CEI}$ is driven low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses $A_X$, $A_Y$, and $A_Z$. However, address line $A_W$ defines the bank number to be enabled as per Table 2.

Switch to a selected bank of memory occurs on the rising edge of chip enable input when the last set of bits is input and a match has been established. After bank selection $\overline{CEO}$ always follows $\overline{CEI}$ with a maximum propagation delay of 15 ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

**ADDRESS INPUT PATTERN** Table 1

| | **Bit Sequence** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Address Inputs** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** |
| $A_W$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | × | × | × | × | × |
| $A_X$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| $A_Y$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| $A_Z$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

× See Table 2

**BANK SELECT CONTROL** Table 2

| Bank Selected | $A_W$ Bit Sequence | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 11 | 12 | 13 | 14 | 15 | BS1 | BS2 | BS3 | BS4 |
| *Banks Off | 0 | × | × | × | × | Low | Low | Low | Low |
| Bank 0 | 1 | 0 | 0 | 0 | 0 | Low | Low | Low | Low |
| Bank 1 | 1 | 0 | 0 | 0 | 1 | High | Low | Low | Low |
| Bank 2 | 1 | 0 | 0 | 1 | 0 | Low | High | Low | Low |
| Bank 3 | 1 | 0 | 0 | 1 | 1 | High | High | Low | Low |
| Bank 4 | 1 | 0 | 1 | 0 | 0 | Low | Low | High | Low |
| Bank 5 | 1 | 0 | 1 | 0 | 1 | High | Low | High | Low |
| Bank 6 | 1 | 0 | 1 | 1 | 0 | Low | High | High | Low |
| Bank 7 | 1 | 0 | 1 | 1 | 1 | High | High | High | Low |
| Bank 8 | 1 | 1 | 0 | 0 | 0 | Low | Low | Low | High |
| Bank 9 | 1 | 1 | 0 | 0 | 1 | High | Low | Low | High |
| Bank 10 | 1 | 1 | 0 | 1 | 0 | Low | High | Low | High |
| Bank 11 | 1 | 1 | 0 | 1 | 1 | High | High | Low | High |
| Bank 12 | 1 | 1 | 1 | 0 | 0 | Low | Low | High | High |
| Bank 13 | 1 | 1 | 1 | 0 | 1 | High | Low | High | High |
| Bank 14 | 1 | 1 | 1 | 1 | 0 | Low | High | High | High |
| Bank 15 | 1 | 1 | 1 | 1 | 1 | High | High | High | High |

*$\overline{CEO} = V_{IH}$ independent of $\overline{CEI}$

**ABSOLUTE MAXIMUM RATINGS***

Voltage on Any Pin Relative to Ground -0.3V to +7.0V

Operating Temperature 0°C to 70°C

Storage Temperature −55°C to +125°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1 |
| Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}=5V\pm10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −1.0 | | +1.0 | *u*A | |
| I/O Leakage Current | $I_{LO}$ | −1.0 | | +1.0 | *u*A | |
| Output Current @2.4V | $I_{OH}$ | −1.0 | | | mA | 2 |
| Output Current @0.4V | $I_{OL}$ | | | +4.0 | mA | 2 |
| Operating Current | $I_{CC}$ | | | 15 | mA | |

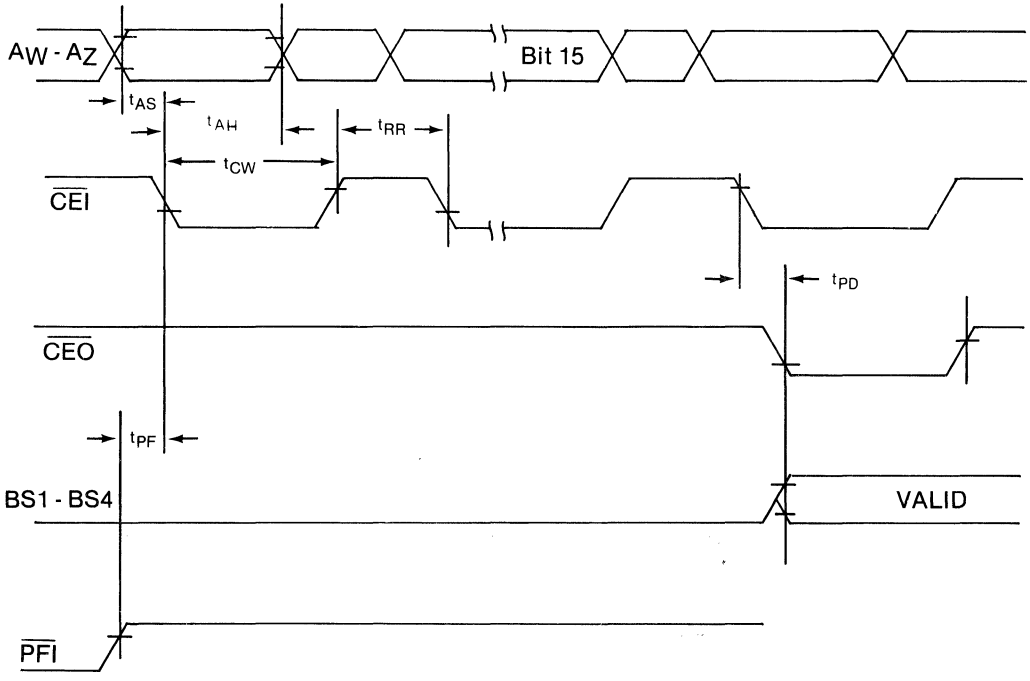
**CAPACITANCE** ($t_A = 25°$)

| PARAMETER | SYMBOL | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | 5 | 10 | pF | |

**A.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Address Set-Up | $t_{AS}$ | 5 | | | ns | |
| Address Hold | $t_{AH}$ | 50 | | | ns | |
| Read Recovery | $t_{RR}$ | 40 | | | ns | |
| Propagation Delay | $t_{PD}$ | | | 15 | ns | 2 |
| Power Fail Input to First $\overline{CE}$ | $t_{PF}$ | 50 | | | ns | |
| Chip Enable Low | $t_{CW}$ | 110 | | | ns | |

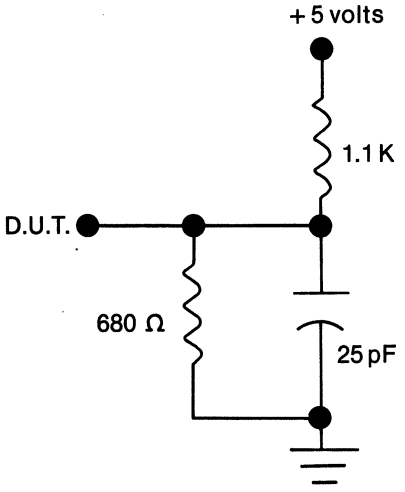
## TIMING DIAGRAM—ACCESS TO BANK SWITCH



**NOTES:** 1. All voltages are referenced to ground.

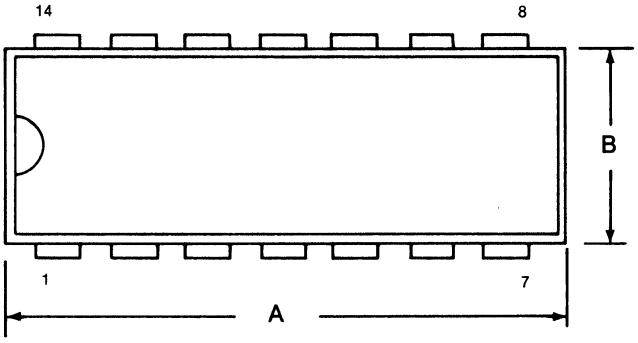
2. Measured with a load as shown in Figure 1.

**OUTPUT LOAD** Figure 1

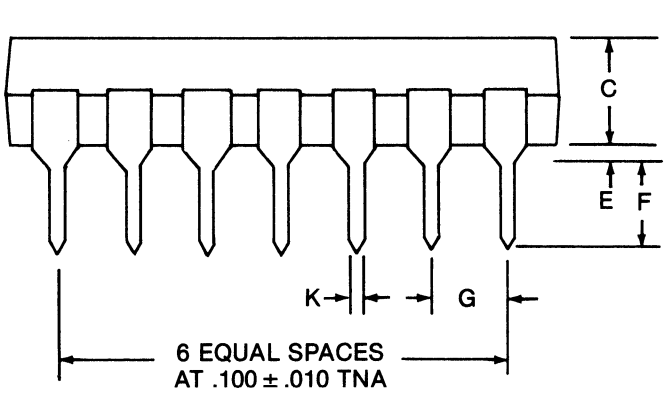


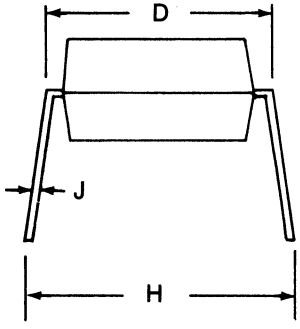

Output Load

# Bank Select Controller
# DS1222




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .740 | .780 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |

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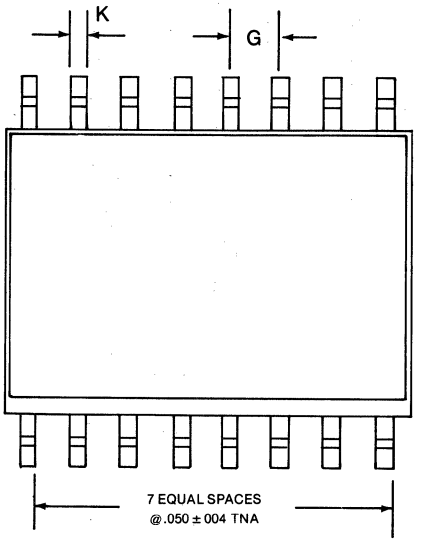
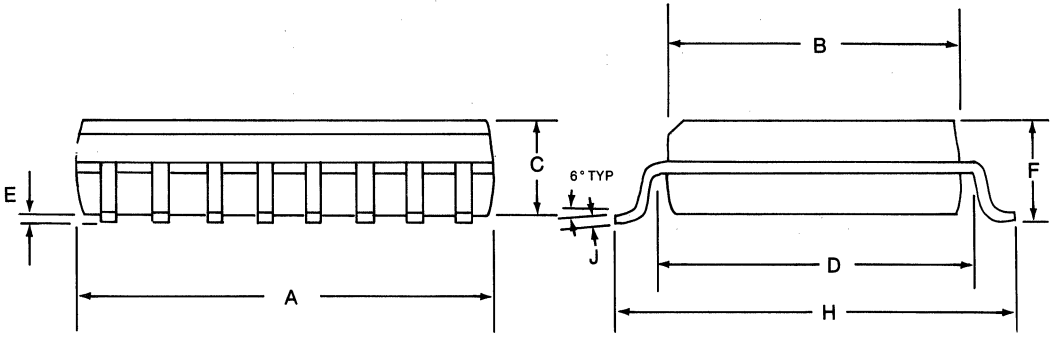
# Bank Select Controller
# DS1222S



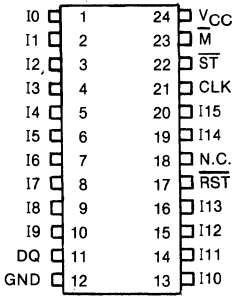

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



# Dallas Semiconductor
## *Electronic Configurator* — *DS1223*

### FEATURES
- 16 remote programmable switches
- 9 Bytes of nonvolatile read/write memory
- 16 bit programmable comparator
- 3 pin serial port sets switches and accesses memory
- Greater than 10 years of data retention
- Data and switch settings are automatically protected during power loss
- Full 10% operating range
- Applications include DIP switch replacement; remote P.C. board configuration, mapping, and decoding
- Connects directly to DS1206 Phantom Interface

### PIN CONNECTIONS




### PIN NAMES
I0-I15 - Switch, Comparator Input/Outputs
DQ - Data Input/Data Output
GND - Ground
$\overline{RST}$ - $\overline{RESET}$
CLK - CLOCK
$\overline{ST}$ - $\overline{STROBE}$
$V_{CC}$ - +5 Volts
NC - No Connection
$\overline{M}$ - Comparator Match

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### DESCRIPTION

The DS1223 Electronic Configurator is a CMOS nonvolatile switch, comparator, and read/write memory circuit designed for personalizing and configurating electronic equipment remotely. The configurator has 16 switches which can be remotely programmed to either Logic 1, Logic 0 or high impedance. Switch pairs can also be connected to simulate 8 SPST switches. In addition, the logic state of 16 inputs can be compared to data contained in nonvolatile memory. There are 16 bytes of nonvolatile read/write memory. Bytes 0, 1, 2, 3, and 4 define switch settings; bytes 5 and 6 relate to the comparator; bytes 7 through 15 are free for any desired use.

A lithium energy source retains information stored in all 16 bytes of memory when power is lost. The electronic configurator monitors $V_{CC}$ for an out of tolerance condition. When such a condition occurs, the lithium energy source is switched on, and write protection is enabled to prevent loss of data. While in the data retention mode the switch/comparator outputs are all in a high impedance mode and all inputs are ignored.

Information is sent to the configurator via a serial input one byte at a time or in a burst where all 16 bytes are either written or read. Interface to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, $\overline{\text{RESET}}$, Data Input/Output.

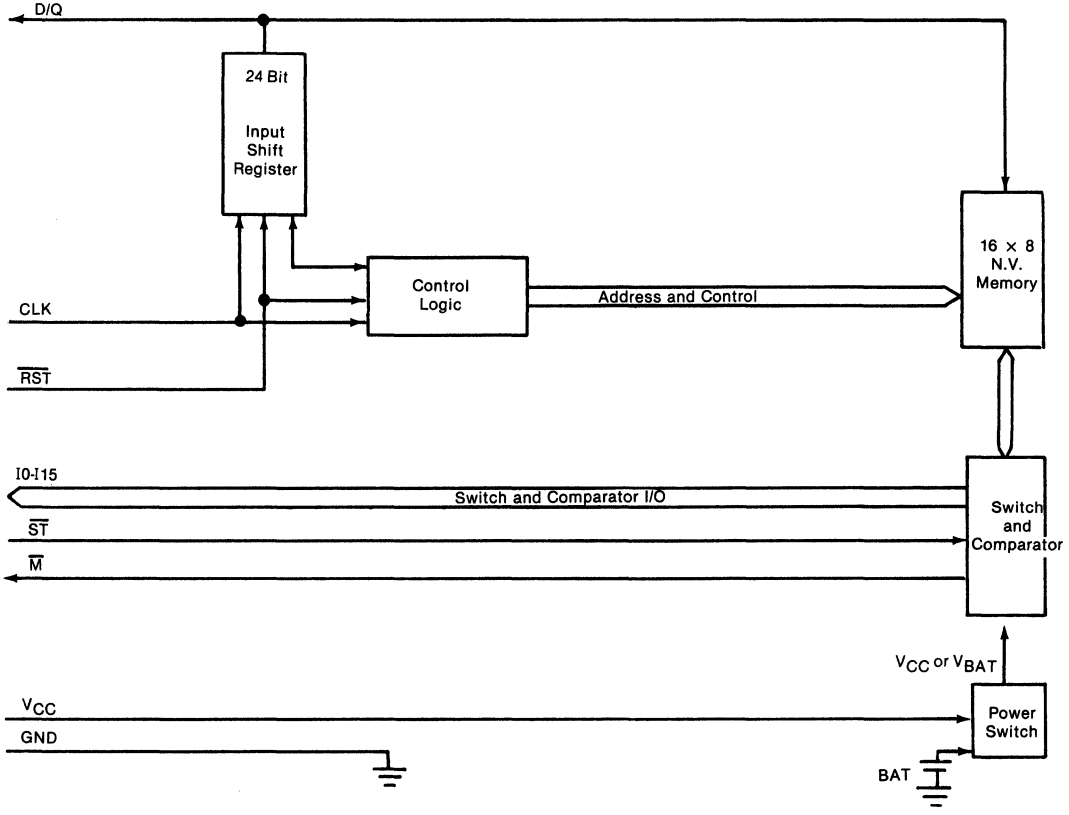
## OPERATION

The block diagram (Figure 1) of the electronic configurator illustrates the main elements of the device; namely, input shift register, control logic, nonvolatile memory, switch and comparator circuits, and power switch. To initiate communication with the configurator $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the input shift register providing both address and command information. Each bit is input serially on the rising edge of the clock. Four address bits specify one of 16 nonvolatile memory locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 clocks which load the input shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals 24 plus 8 for byte mode or 24 plus 128 for burst mode.

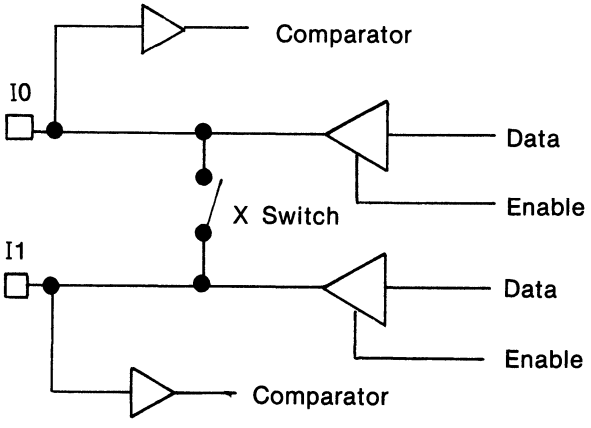
The information stored in the first five bytes of the nonvolatile memory define the status of input/output pins I0-I15. The switch configuration is illustrated in Figure 2. Data stored in nonvolatile memory bytes 6 and 7 contain 16 bits which are compared to the input/output pins I0-I15. When all inputs match the value stored in bytes 6 and 7, the $\overline{\text{MATCH}}$ pin will be latched and driven low when the $\overline{\text{STROBE}}$ input transitions from low to high.

The nine remaining bytes serve as user read/write nonvolatile memory. Figure 3 illustrates the configurator register address and the definition of each bit.

**ELECTRONIC CONFIGURATOR BLOCK DIAGRAM** Figure 1




**CONFIGURATOR SWITCHES** Figure 2




X Switch Resistance ≤ 500 Ω

| Switch Pairs | | |
|---|---|---|
| | I0 - I1 | I8 - I9 |
| | I2 - I3 | I10 - I11 |
| | I4 - I5 | I12 - I13 |
| | I6 - I7 | I14 - I15 |

**CONFIGURATOR MEMORY ADDRESSES** Figure 3

| | MSB 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 LSB | |
|---|---|---|---|---|---|---|---|---|---|
| Byte 0 | I15, I14 | I13, I12 | I11, I10 | I9, I8 | I7, I6 | I5, I4 | I3, I2 | I1, I0 | X Switch 1 = Closed 0 = Open |
| Byte 1 | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 | Data Out 1 = Logic High 0 = Logic Low |
| Byte 2 | I15 | I14 | I13 | I12 | I11 | I10 | I9 | I8 | Data Out 1 = Logic High 0 = Logic Low |
| Byte 3 | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 | Enable Out 0 = HIZ |
| Byte 4 | I15 | I14 | I13 | I12 | I11 | I10 | I9 | I8 | Enable Out 0 = HIZ |
| Byte 5 | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 | Comparison |
| Byte 6 | I15 | I14 | I13 | I12 | I11 | I10 | I9 | I8 | Comparison |
| Byte 7 | | | | | | | | | User Byte |
| Byte 8 | | | | | | | | | User Byte |
| Byte 9 | | | | | | | | | User Byte |
| Byte 10 | | | | | | | | | User Byte |
| Byte 11 | | | | | | | | | User Byte |
| Byte 12 | | | | | | | | | User Byte |
| Byte 13 | | | | | | | | | User Byte |
| Byte 14 | | | | | | | | | User Byte |
| Byte 15 | | | | | | | | | User Byte |

## ADDRESS/COMMAND

Each data transfer consists of a three byte address/command input called the address/command. The address/command is shown in Figure 4. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address command fails to meet the exact pattern of read or write the cycle is aborted and all future inputs to the configurator are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The 8 bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address A0 in bit 0, A1 in bit 1, A2 in bit 2, A3 in bit 3. Bits 4 through 7 of the second byte of the address/command must be set at logical 0. If bits 4 through 7 do not equal logical 0, the cycle is aborted and all future inputs to the configurator are ignored until $\overline{\text{RESET}}$ is brought low and then high again to begin a new cycle. The third byte of the address/command must have a logic 0 in bit 0 through bit 5 and a logical 1 written in bit 6. Bit 7 of byte three of the address/command is used along with bits A0 through A3 in byte 2 to define the burst mode. When A0 through A3 of byte two equals logical 0 and bit 7 of byte three equals logical 1, the configurator will enter the burst mode after the 24 bit address/command sequence is complete.

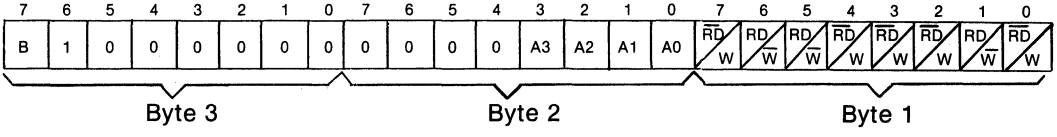
## BURST MODE

Burst mode is specified for the electronic configurator when all address bits (A0-A3) of the address/command are set to logical 0 and bit 7 of byte three to logical 1. The burst mode causes 16 consecutive bytes to be read or written. Burst mode terminates when the $\overline{\text{RESET}}$ input is driven low.

## RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{\text{RESET}}$ input high. The input also provides a method of terminating either single byte or multiple byte transfers. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of clock cycles. Address/command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates and D/Q pin goes to a high impedance state if the $\overline{\text{RESET}}$ input is low. The $\overline{\text{RST}}$ input is used only in control of communications with the configurator and has no effect on the nonvolatile memory data. Data transfer is illustrated in Figure 5.

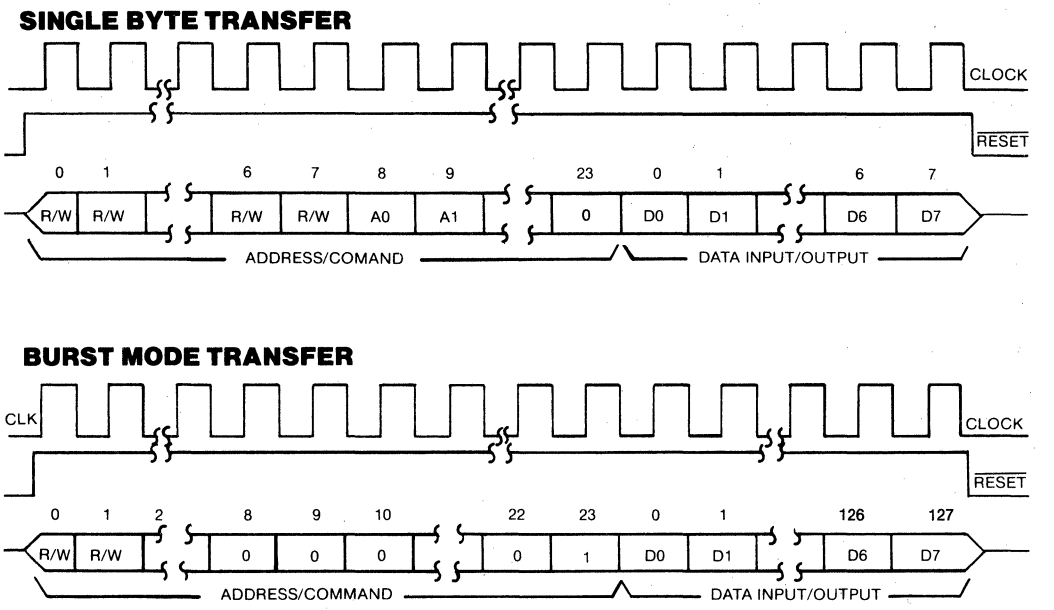
**CONFIGURATOR — ADDRESS COMMAND WORD** Figure 4




B - Burst
RD - Read
W - Write
A0-A3 - Address

**DATA TRANSFER**

Figure 5




NOTES
1.) DATA INPUT SAMPLED ON RISING EDGE OF CLOCK
2.) DATA OUTPUT CHANGES ON FALLING EDGE OF CLOCK

**DATA INPUT**

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next 8 CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1 bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

**DATA OUTPUT**

Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for data output byte 1 bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

**ABSOLUTE MAXIMUM RATINGS***

| | | |
|---|---|---|
| VOLTAGE ON ANY PIN RELATIVE TO GROUND | — | −1.0V to +7V |
| OPERATING TEMPERATURE | — | 0°C to 70°C |
| STORAGE TEMPERATURE | — | −40°C to 70°C |
| SOLDERING TEMPERATURE | — | 260°C for 10 Sec |

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | $V_{CC}$ +.3 | V | 1 |
| Logic 0 | $V_{IL}$ | −0.3 | | 0.8 | V | 1 |
| Supply | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 5V ±10%)

| | | | | | | |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | | | 1 | uA | 5 |
| Output Leakage | $I_{LO}$ | | | 1 | uA | 5 |
| Output Current @2.4V | $I_{OH}$ | −1 | | | mA | 11 |
| Output Current @ .4V | $I_{OL}$ | | | +4 | mA | 11 |
| Output Current @2.4V | $I_{OH}$ | −400 | | | uA | 12 |
| Output Current @ .4V | $I_{OL}$ | | | 1.6 | mA | 12 |
| X Switch Impedance | X | | | 500 | Ω | 7 |
| Active Current | $I_{CC1}$ | | | 10 | mA | 8 |
| Standby Current | $I_{CC2}$ | | | 2 | mA | 8, 2 |

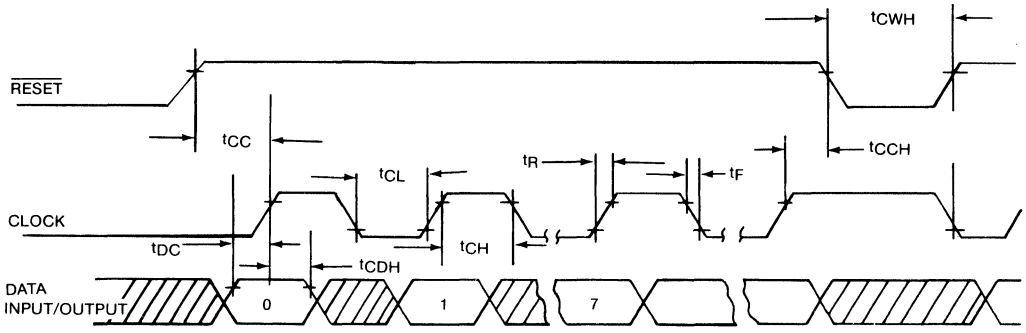
**CAPACITANCE** ($t_A$ = 25 °C)

| PARAMETER | SYMBOL | MIN | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

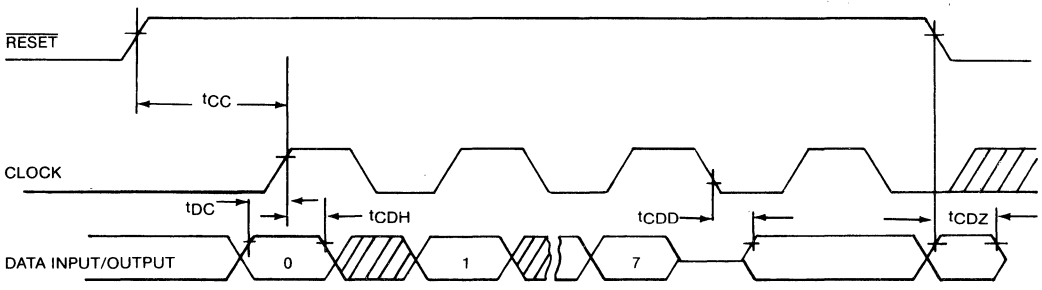
**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Data to CLK Setup | $t_{DC}$ | 50 | | | ns | 3 |
| Data to CLK Hold | $t_{CDH}$ | 50 | | | ns | 3 |
| CLK to Data Delay | $t_{CDD}$ | | | 200 | ns | 3, 4, 6 |
| CLK Low Time | $t_{CL}$ | 250 | | | ns | 3 |
| CLK High Time | $t_{CH}$ | 250 | | | ns | 3 |
| CLK Frequency | $f_{CLK}$ | D.C. | | 2.0 | MHZ | 3 |
| CLK Rise & Fall | $t_R$, $t_F$ | | | 10 | ns | 3 |
| $\overline{RST}$ to CLK Set Up | $t_{CC}$ | 1 | | | us | 3, 9 |
| CLK to $\overline{RST}$ Hold | $t_{CCH}$ | 50 | | | ns | 3 |
| $\overline{RST}$ Inactive Time | $t_{CWH}$ | 1 | | | us | 3 |
| $\overline{RST}$ to //O High Z | $t_{CDZ}$ | | | 75 | ns | 3 |
| Strobe to $\overline{MATCH}$ Valid | $t_{SM}$ | | | 35 | ns | 3 |
| Input Set-Up | $t_{SU}$ | 40 | | | ns | 3,4 |
| Input Hold | $t_{HD}$ | 10 | | | ns | 3,4 |

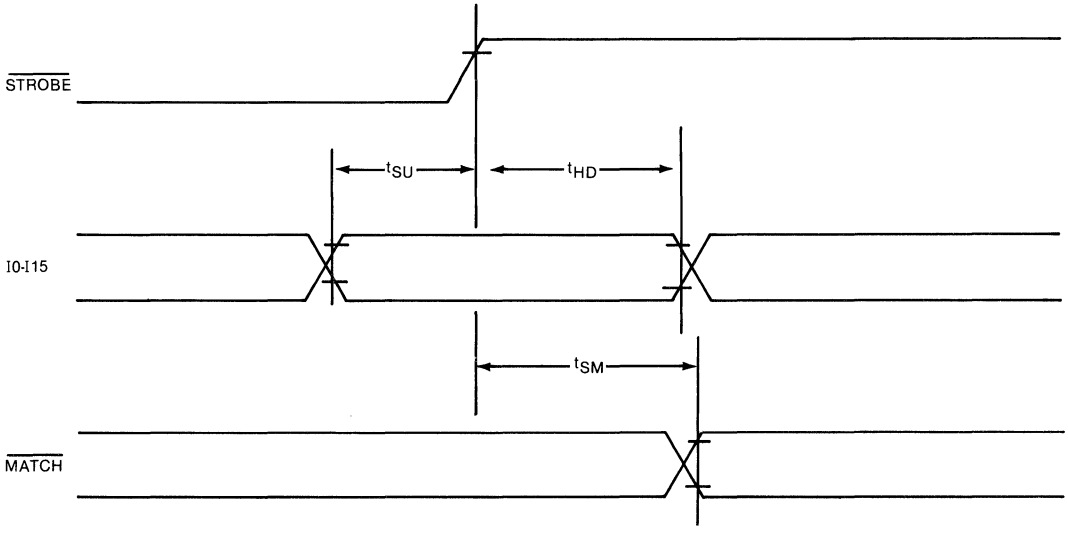
## TIMING DIAGRAM—WRITE DATA TRANSFER[10]




## TIMING DIAGRAM—WRITE DATA TRANSFER[10]




## TIMING DIAGRAM—COMPARATOR[10]

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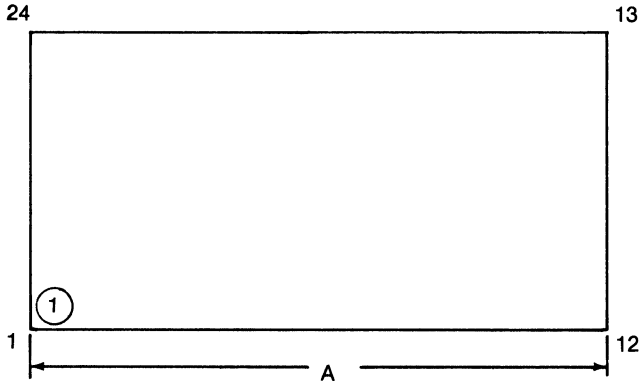
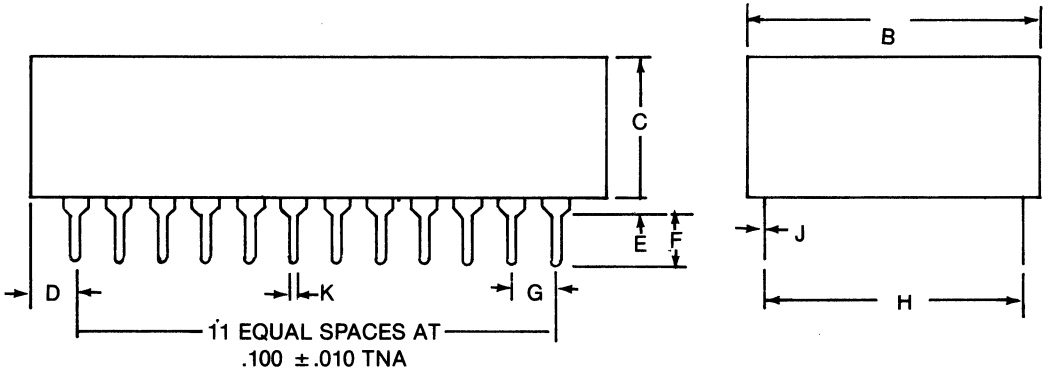
**NOTES**

1. All voltages are referenced to GND.
2. $\overline{\text{RESET}} = V_{IH}$.
3. Measured at $V_{IH} = 2.0$ or $V_{IL} = .8V$ and 10 ns maximum rise and fall time.
4. Measured at $V_{OH} = 2.4$ volts and $V_{OL} = 0.4$ volts.
5. $V_{CC} = +5$ Volts with outputs open.
6. Load capacitance = 100 pF.
7. X Switch Impedance is the terminal resistance of switch pairs when the X Switch is closed—see Figure 2.
8. Measured with outputs open.
9. Measured at $V_{IN}$ of $\overline{\text{RST}} = 3.8V$.
10. A period of 100 ns must elapse after data transfer before switches and comparator outputs are valid.
11. Applies to DQ and $\overline{\text{MATCH}}$.
12. Applies to switches.

# DS1223
## Electronic Configurator




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.320 | 1.335 |
| B | .685 | .700 |
| C | .345 | .360 |
| D | .100 | .120 |
| E | .015 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .600 | .650 |
| J | .008 | .012 |
| K | .015 | .021 |




NOTE: Pin 18 is missing by design.

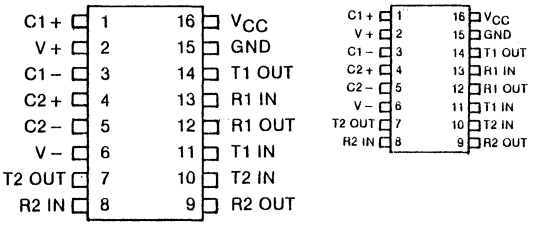
# Dallas Semiconductor
## +5V Powered Dual RS-232 Transmitter/Receiver

## DS232
## DS1228—16-Pin DIP
## DS1228S—16-Pin SOIC

### FEATURES

- Operates from a single 5V power supply
- 2 drivers and 2 receivers
- Meets all EIA RS-232-C specifications
- On-board voltage doubler
- On-board voltage inverter
- ±30 V input levels
- ±9 V output levels with +5 V supply
- Low power CMOS
- Pin compatible with the MAX 232
- −40°C to +85°C temperature range available
- Optional 16-pin SOIC surface mount package

### PIN CONNECTIONS




### PIN NAMES

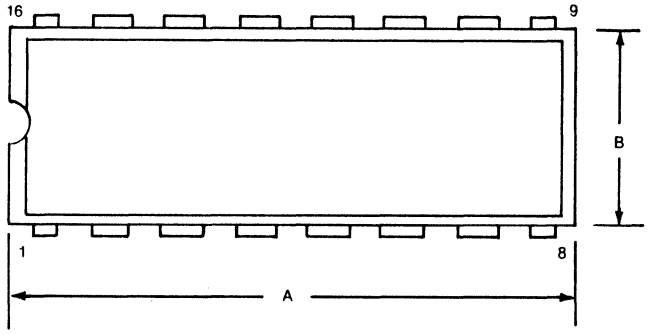
| | |
|---|---|
| C1+, C1 | - Capacitor 1 Connections |
| C2+, C2 | - Capacitor 2 Connections |
| V+, V− | - ±10 Volts |
| T1 IN, T2 IN | - Transmitter In |
| T1 OUT, T2 OUT | - Transmitter Out |
| R1 IN, R2 IN | - Receiver In |
| R1 OUT, R2 OUT | - Receiver Out |
| $V_{CC}$ | - +5 Volts |
| GND | - Ground |

### DESCRIPTION

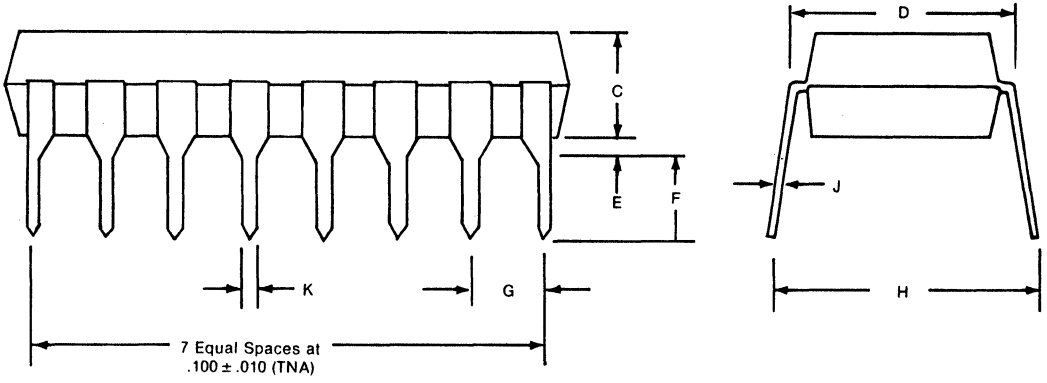
The DS232 is a dual RS-232-C Receiver/Transmitter that meets all EIA specifications while operating from a single +5 volt supply. The DS232 has two internal charge pumps. One of the charge pumps is used to generate +10 volts. The other is used to generate −10 volts. The DS232 also contains four level translators. Two of the level translators are RS-232 transmitters which convert TTL/CMOS inputs into ±9V RS-232 outputs. The other two level translators are RS-232 receivers which convert RS-232 inputs to 5V TTL/CMOS outputs. These receivers are capable of operating with up to ±30V inputs. The DS232 is suitable for all RS-232-C communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS232 supplies ±10 volts from the $V_{CC}$ input.

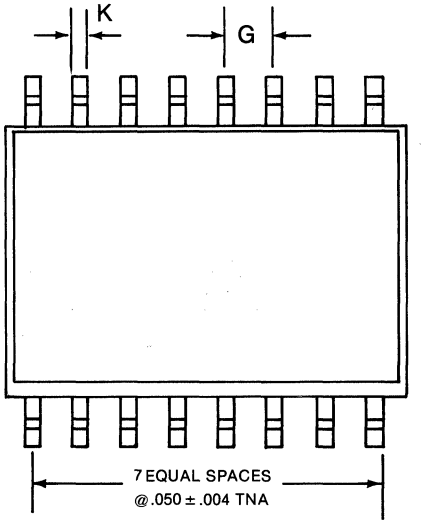
See the data sheet for the DS1229 for electrical specifications and operation.

# Dual RS-232 Transmitter/Receiver
# DS1228

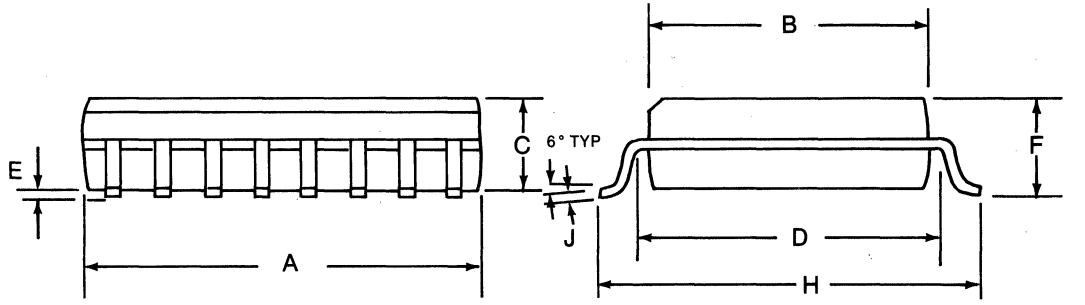



| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .740 | .780 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |






| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



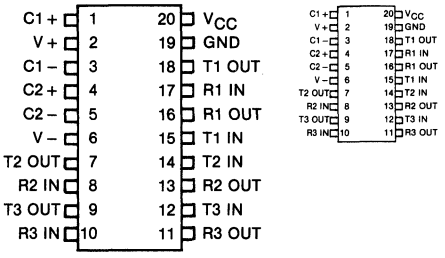
# Dallas Semiconductor
## +5V Powered Triple RS-232 Transmitter/Receiver

## DS1229—20-Pin DIP
## DS1229S—20-Pin SOIC

### FEATURES

- Operates from a single 5V power supply
- 3 drivers and 3 receivers
- Meets all EIA RS-232-C specifications
- On-board voltage doubler
- On-board voltage inverter
- ±30 V input levels
- ±9 V output levels with +5 V supply
- Low power CMOS
- −40°C to +85°C temperature range available
- Optional 20-Pin SOIC surface mount package

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| C1+, C1 | - Capacitor 1 Connections |
| C2+, C2 | - Capacitor 2 Connections |
| V+, V− | - ±10 Volts |
| T1 IN, T2 IN, T3 IN | - Transmitter In |
| T1 OUT, T2 OUT, T3 OUT | - Transmitter Out |
| R1 IN, R2 IN, R3 IN | - Receiver In |
| R1 OUT, R2 OUT, R3 OUT | - Receiver Out |
| $V_{CC}$ | - +5 Volts |
| GND | - Ground |

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### DESCRIPTION

The DS1229 is a Triple RS-232-C Receiver/Transmitter that meets all EIA specifications while operating from a single +5 volt supply. The DS1229 has two internal charge pumps. One of the charge pumps is used to generate +10 volts. The other is used to generate −10 volts. The DS1229 also contains six level translators. Three of the level translators are RS-232 transmitters which convert TTL/CMOS inputs into ±9V RS-232 outputs. The other three level translators are RS-232 receivers which convert RS-232 inputs to 5V TTL/CMOS outputs. These receivers are capable of operating with up to ±30V inputs. The DS1229 is suitable for all RS-232-C communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS1229 supplies ±10 volts from the $V_{CC}$ input.

## OPERATION

The DS1229 has three sections: a triple transmitter, a triple receiver and a dual charge pump which generates ± 10 volts from the 5-volt supply.

## CHARGE PUMP SECTION

The dual charge pumps within the DS1229 are used to generate the voltages necessary for level conversion from TTL/CMOS to RS-232. One charge pump uses external capacitor C1 to double the $V_{CC}$ input to + 10 volts. The second charge pump uses external capacitor C2 to invert the +10 volts to −10 volts. Capacitors C3 and C4 are used to filter the + 10 volt and − 10 volt power supply. The recommended size of capacitors C1-C4 is 22 *u*F but the value is not critical. Increasing the value of C3 and C4 will lower the 16 KHz ripple on the ± 10 volt supplies and the RS-232 outputs. The value of C1 and C4 can be lowered to 1 *u*F where size is critical.

## TRANSMITTER SECTION

The three transmitters are CMOS inverters powered by the internal ±10 volt supply.The input is TTL/CMOS compatible. Each input has an internal 750 K pull-up resistor so that unused transmitter inputs can be left unconnected. Unused transmitter inputs will force the outputs low. The open circuit output voltage swing is from + 10 volts to − 10 volts. Worst-case conditions for RS-232-C of ± 5 volt driving a 3 K load are met at maximum allowable ambient temperature and a $V_{CC}$ level of 5.0 volts. Typical voltage swings of ± 9 volts occur with outputs of 5 K and $V_{CC}$ equal to 5 volts. The slew rate at the output is limited to less than 30 volts/*u*s and the power-down output impedance will be a minimum of 300 ohms with ± 2 volts applied to the outputs and $V_{CC}$ at zero volts. The outputs are also short-circuit-protected and can be short-circuited to ground indefinitely.

## RECEIVER SECTION

The three receivers conform fully to the RS-232-C specifications. The input impedance is between 3 K ohms and 7 K ohms and can withstand up to ± 30 volts with or without $V_{CC}$ applied. The input switching thresholds are within the ± 3 volts limit of RS-232-C specification with a $V_{IL}$ of 0.7 volts and a $V_{IH}$ of 2.4 volts. The receivers have 0.5 volts of hysteresis to improve noise rejection. The TTL/CMOS compatible output of the receiver will be low whenever the RS-232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between + 0.8 V and − 30 V.

## ABSOLUTE MAXIMUM RATINGS*

$V_{CC}$ ..... + 7 volts
V+ ..... + 12 volts
V− ..... − 12 volts
Transmitter Inputs ..... − 0.3V to ($V_{CC}$ + 0.3V)
Receiver Inputs ..... ± 30 volts
Transmitter Outputs .. (V+ + 0.3V) to (V− − 0.3V)
Receiver Outputs ..... —0.3V to ($V_{CC}$ + 0.3V)
Storage Temperature ..... − 55 °C to 125 °C

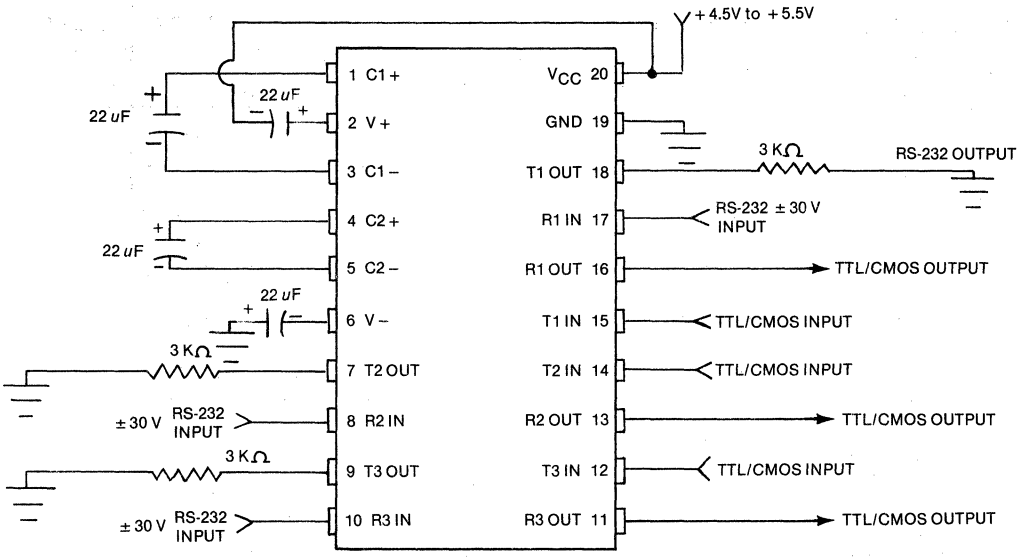
**RECOMMENDED D.C. OPERATING CONDITIONS** (0 °C to 70 °C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Logic 1 Input | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1 |
| Logic 0 Input | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |
| RS-232 Input Voltage | $V_{RS}$ | −30 | | +30 | V | 1,2,11 |

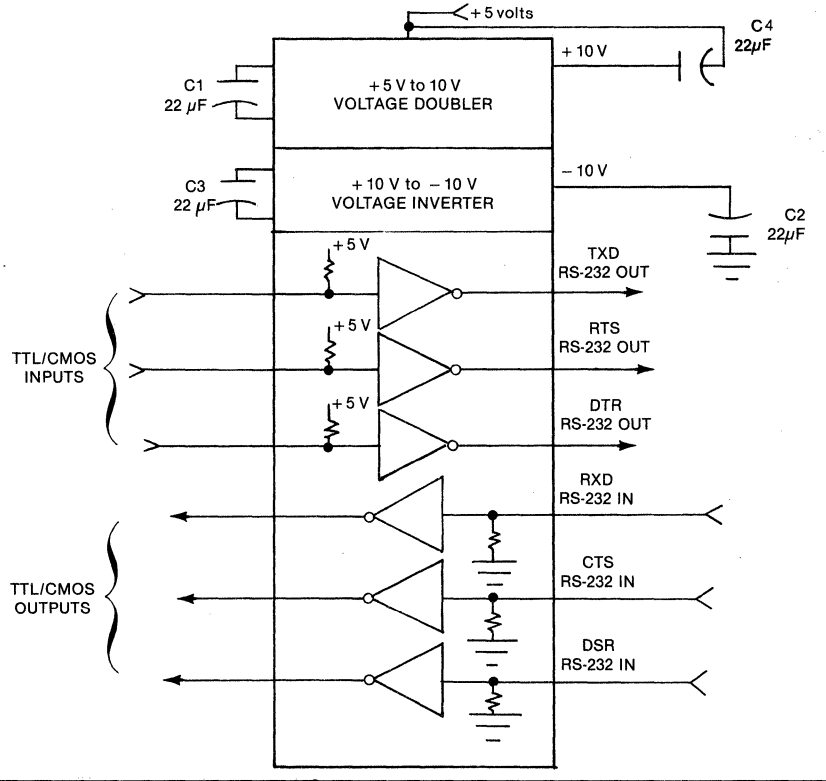
**D.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC}$ = +5 volts ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| RS-232 Output Voltage | $V_{ORS}$ | ±5 | ±9 | ±10 | V | 3,12 |
| Power Supply Current | $I_{DD}$ | | 5 | 10 | mA | 4 |
| Transmitter Pull-up Current | $I_{TP}$ | | 5 | 200 | *u*A | 5 |
| RS-232 Input Threshold Low | $V_{TL}$ | +0.7 | +1.2 | | V | 6 |
| RS-232 Input Threshold High | $V_{TH}$ | | 1.7 | 2.4 | V | 6 |
| RS-232 Input Hysteresis | $V_{HY}$ | 0.2 | 0.5 | 1.0 | V | |
| ReceiverOutput Current @2.4 V | $I_{OH}$ | −1.0 | | | mA | |
| Receiver Output Current @0.4 V | $I_{OL}$ | | | +3.2V | mA | |
| Output Resistance | $R_{OUT}$ | 300 | | | Ω | 7 |
| RS-232 Output Short Circuit | $I_{SC}$ | | | ± 15 | mA | |
| Propagation Delay | $t_{PD}$ | | 3 | | *us* | 8 |
| Transmitter Output Instantaneous Slew Rate | $t_{SR}$ | | | 30 | V/*us* | 9 |
| Transmitter Output Transition Slew Rate | $t_{tSR}$ | | 3 | | V/*us* | 10 |
| V+ Supply Voltage | V+ | +5.5 | 9 | | V | |
| V− Supply Voltage | V− | −5.5 | 8.5 | | V | |

## DS1229 RS-232 TRANSMITTER/RECEIVER TEST CIRCUIT Figure 1



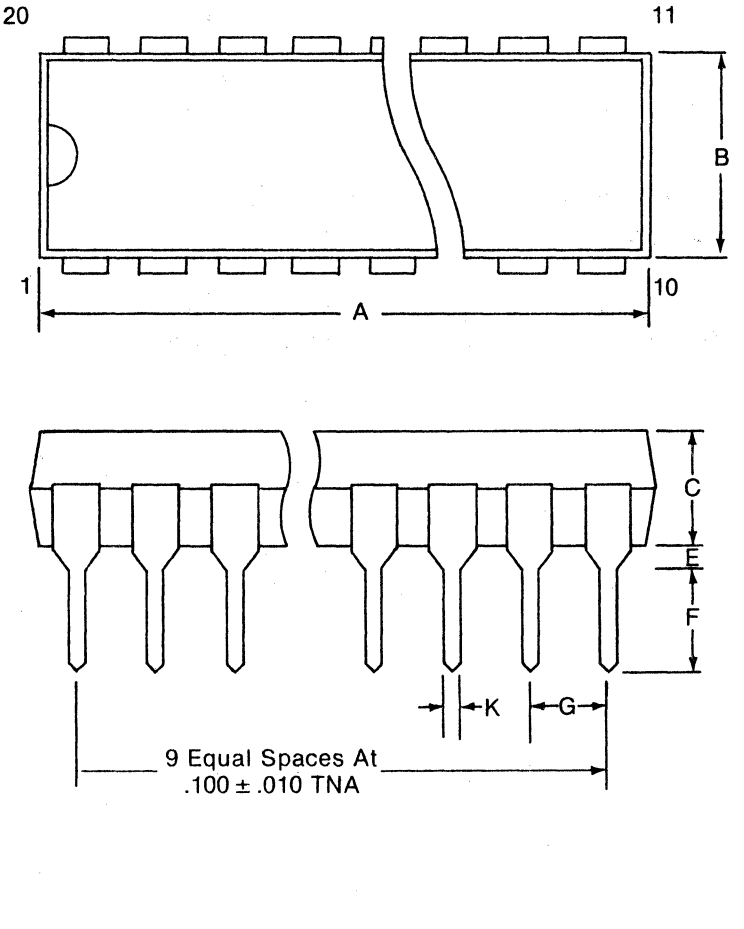

## TYPICAL APPLICATIONS Figure 2



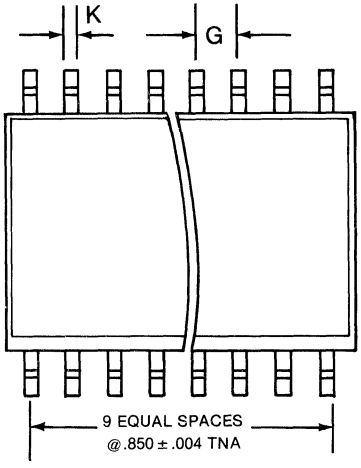
**NOTES:**

1. All voltages are referenced to ground.
2. Applies to Receiver Inputs only.
3. T1, T2, and T3 loaded with 3K ohms to ground.
4. All outputs are unloaded.
5. T1, T2, and T3 Inputs = 0 volts.
6. $V_{CC}$ = +5 volts.
7. $V_{OUT}$ = ±2 volts.
8. RS-232 to TTL or TTL to RS-232.
9. $C_L$ = 10 pF, RL = 3 K, TA = 0°C. This parameter is sample tested only.
10. $R_L$ = 3 K , $C_L$ = 2500 pF measured from +3 volts to −3 volts or −3 volts to +3 volts.
11. This parameter is sample tested only.
12. Negative output level of −5V is increased to −4.75V for the DS1229 only. Positive output level remains at +5V. Use of a +10%, −5% power supply will restore the negative level to −5V.

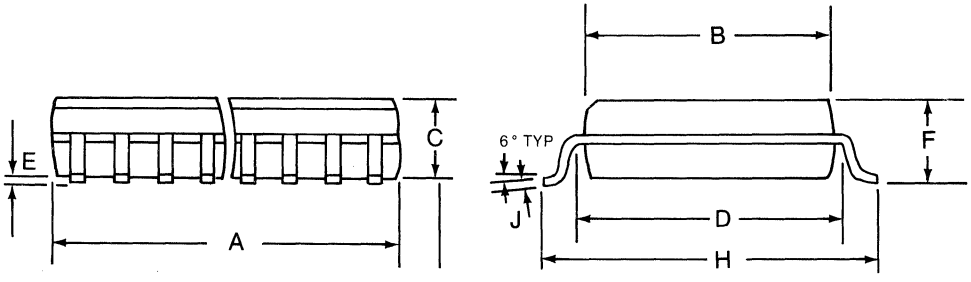
# *Triple RS-232 Transmitter/Receiver*
# *DS1229*




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .960 | 1.040 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .503 | .511 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



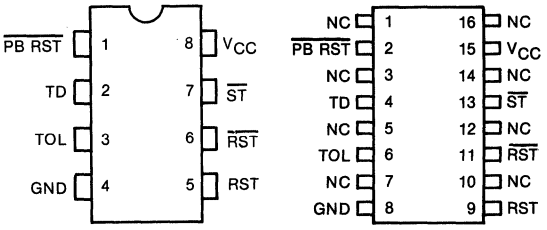
# Dallas Semiconductor
# *MicroMonitor*

# *DS1232—8-Pin DIP*
# *DS1232S—16-Pin SOIC*

## FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components
- Space saving 8-pin Mini-DIP
- Optional 16-pin SOIC surface mount package

## PIN CONNECTIONS




## PIN NAMES

| | |
|---|---|
| $\overline{\text{PB RST}}$ | - Push Button Reset Input |
| TD | - Time Delay Set |
| TOL | - Selects 5% or 10% $V_{CC}$ Detect |
| GND | - Ground |
| RST | - Reset Output (Active High) |
| $\overline{\text{RST}}$ | - Reset Output (Active Low, Open Drain) |
| $\overline{\text{ST}}$ | - Strobe Input |
| $V_{CC}$ | - +5 Volt Power |
| NC | - No Connections |

## DESCRIPTION

The DS1232 monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature compensated reference and comparator circuit is used to monitor the status of power ($V_{CC}$). When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When $V_{CC}$ returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize. The second function the DS1232 performs is pushbutton reset control. The DS1232 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232 has an internal timer which forces the reset signals to the active state if the strobe input is not driven low prior to time out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

## OPERATION—POWER MONITOR

The DS1232 provides the function of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When $V_{CC}$ falls below a preset level as defined by TOL (Pin 3), the $V_{CC}$ comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6). When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as $V_{CC}$ falls below 4.75 volts. When TOL is connected to $V_{CC}$ the RST and $\overline{RST}$ signals become active as $V_{CC}$ falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid $V_{CC}$. On power up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

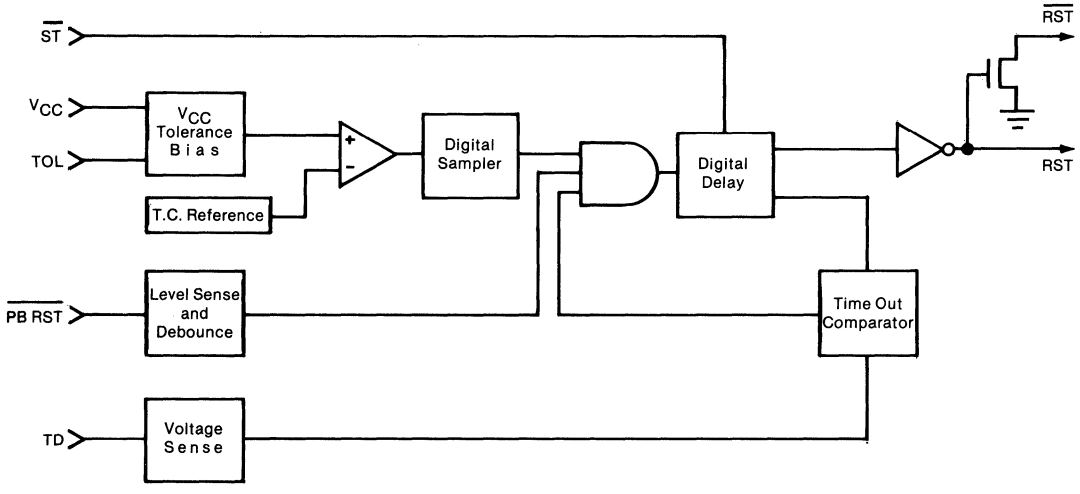
## OPERATION—PUSHBUTTON RESET

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

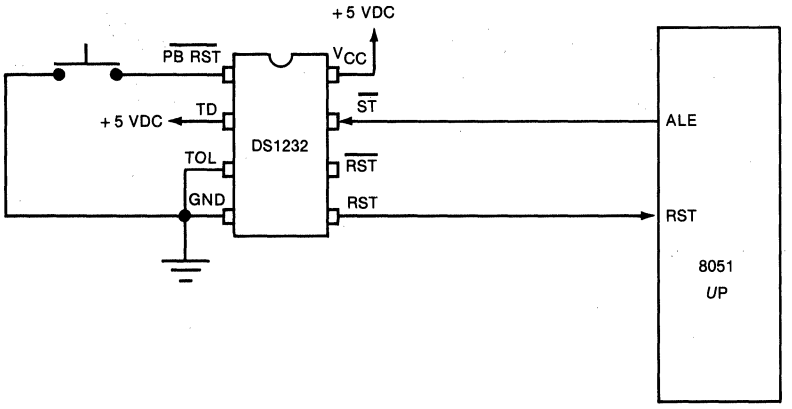
## OPERATION—WATCHDOG TIMER

The DS1232 provides a watchdog timer function by forcing RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to $V_{CC}$. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time out, the watchdog timer is reset and begins to time out again. If the watchdog timer is allowed to time out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time out. A typical example is shown in Figure 3.

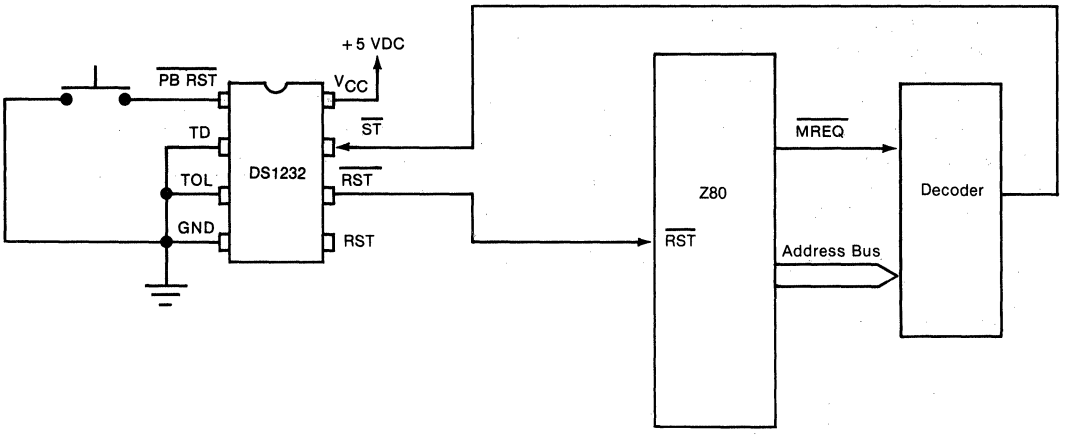
**MICROMONITOR BLOCK DIAGRAM** Figure 1



**PUSHBUTTON RESET** Figure 2




**WATCHDOG TIMER** Figure 3



**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to 125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| $\overline{ST}$ and $\overline{PB\ RST}$ Input High Level | $V_{IH}$ | 2.0 | | $V_{CC}+0.3$ | V | 1 |
| $\overline{ST}$ and $\overline{PB\ RST}$ Input Low Level | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | *u*A | 3 |
| Output Current @2.4V | $I_{OH}$ | −1.0 | −2.0 | | mA | |
| Output Current @0.4V | $I_{OL}$ | 2.0 | 3.0 | | mA | |
| Operating Current | $I_{CC}$ | | 0.5 | 2.0 | mA | 2 |
| $V_{CC}$ Trip Point (TOL = GND) | $V_{CCTP}$ | 4.50 | 4.62 | 4.74 | V | 1 |
| $V_{CC}$ Trip Point (TOL = $V_{CC}$) | $V_{CCTP}$ | 4.25 | 4.37 | 4.49 | V | 1 |

**CAPACITANCE** ($t_A = 25°C$)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

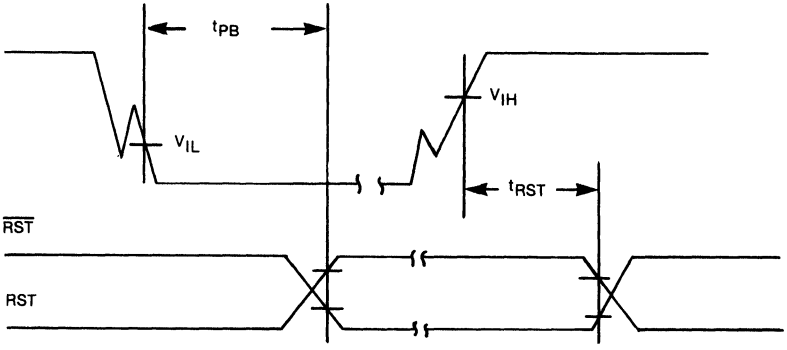
**A.C. ELECTRICAL CHARACTERISTICS** (0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{PB}$ $\overline{RST}$ $V_{IL}$ | $t_{PB}$ | 20 | | | ms | |
| RESET Active Time | $t_{RST}$ | 250 | 610 | 1000 | ms | |
| $\overline{ST}$ Pulse Width | $t_{ST}$ | 20 | | | ns | |
| $V_{CC}$ Detect to $\overline{RST}$ and $\overline{RST}$ | $t_{RPD}$ | | | 100 | ns | |
| $V_{CC}$ Slew Rate 4.75V - 4.25V | $t_F$ | 300 | | | *u*s | |
| $V_{CC}$ Detect to $\overline{RST}$ and $\overline{RST}$ | $t_{RPU}$ | 250 | 610 | 1000 | ms | 4 |
| $V_{CC}$ Slew Rate 4.25V - 4.75V | $t_R$ | 0 | | | ns | |

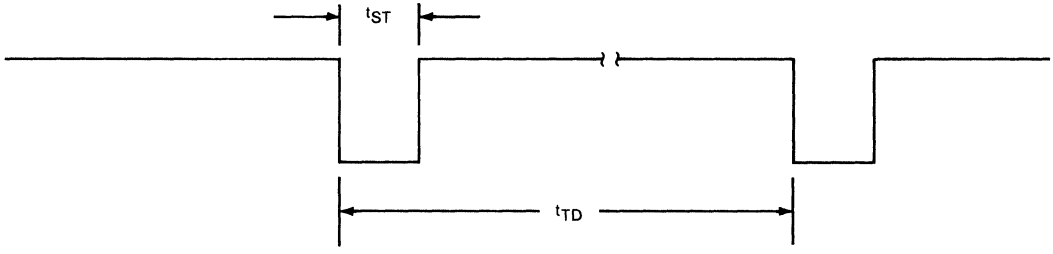
**NOTES:**

1. All voltages referenced to ground.
2. Measured with outputs open.
3. $\overline{PB}$ $\overline{RST}$ is internally pulled up to $V_{CC}$ with an internal impedance of 10K typical.
4. $t_R = 5$ *u*s.
5. $\overline{RST}$ is an open drain output.

## TIMING DIAGRAM—PUSHBUTTON RESET




## TIMING DIAGRAM—STROBE INPUT




$t_{TD}$ = 250 ms maximum with TD pin at Ground

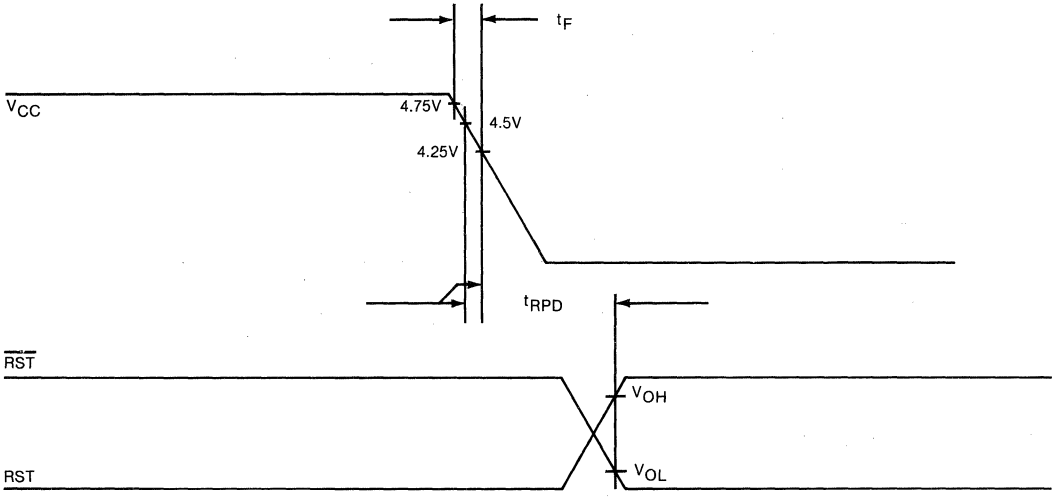
$t_{TD}$ = 1 sec maximum with TD pin floating

$t_{TD}$ = 2 sec maximum with TD pin connected to $V_{CC}$

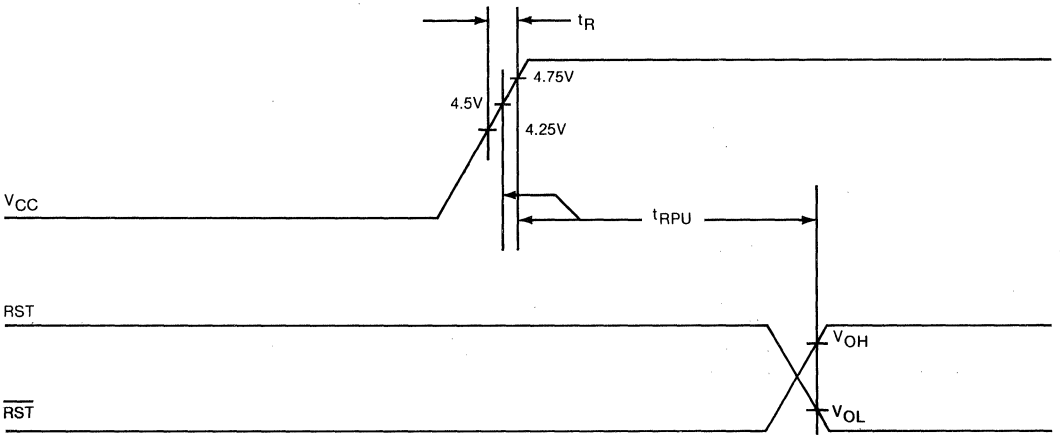
**NOTE:**

$t_{TD}$ is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of $t_{RST}$. $t_{TD}$ times are given as maximum. The minimum time is 25% of maximum.

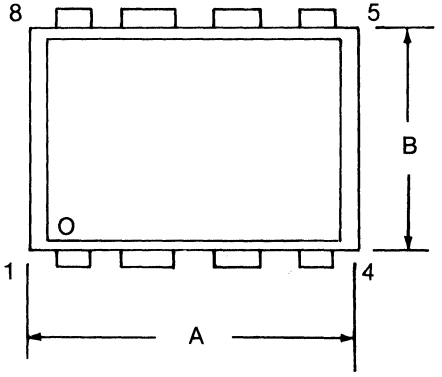
## TIMING DIAGRAM—POWER DOWN



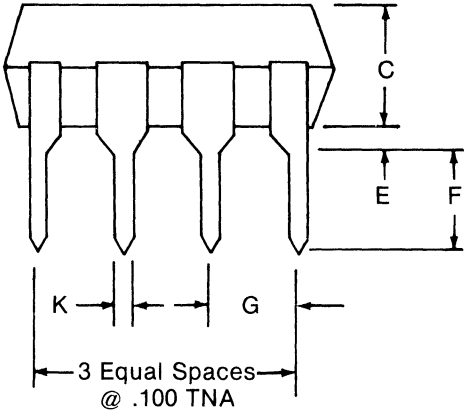

## TIMING DIAGRAM—POWER UP

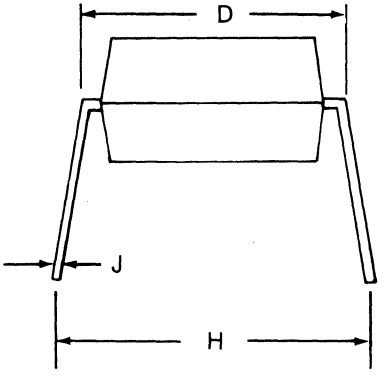


# DS1232
# MicroMonitor




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .360 | .400 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |

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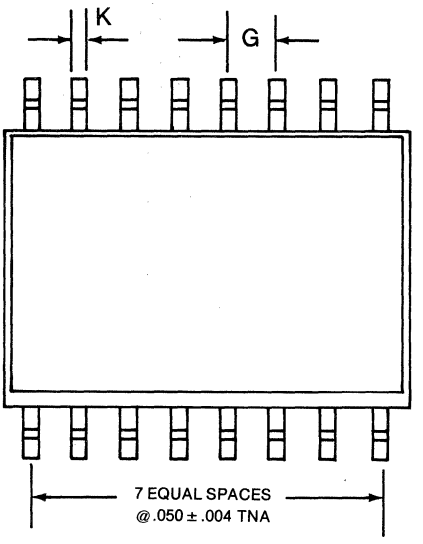
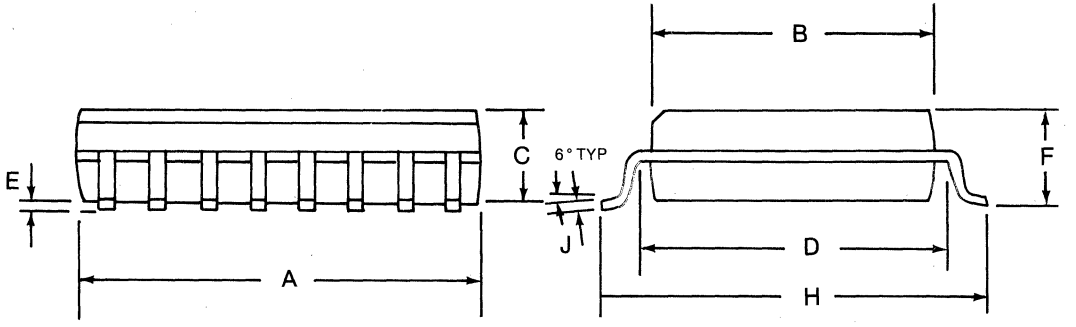
# DS1232S
# MicroMonitor




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .403 | .411 |
| B | .290 | .296 |
| C | .089 | .095 |
| D | .325 | .330 |
| E | .008 | .012 |
| F | .097 | .105 |
| G | .046 | .054 |
| H | .402 | .410 |
| J | .006 | .011 |
| K | .013 | .019 |



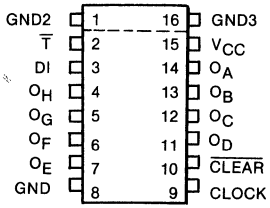
# Dallas Semiconductor
## *Eliminator*

# *DS1290*
# *DS1291*

### FEATURES

- Replaces 8 hard-to-get-at manual switches
- Option printed circuit board via software
- DS1290 remembers settings in the absence of power
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Interface
- Low power CMOS
- DS1291 Volatile Eliminator
- Change of switch settings occur simultaneously
- Over 10 years of data retention

### PIN CONNECTIONS




### PIN NAMES

| | | |
|---|---|---|
| $\overline{T}$ | - | Transfer |
| DI | - | Data Input |
| $O_AO_H$ | - | Switch Outputs |
| CLOCK | - | Clock Input |
| $\overline{CLEAR}$ | - | All Outputs Set Low |
| $V_{CC}$ | - | +5 Volts |
| GND | | Ground |
| GND2 | - | Missing on DS1290<br>Must Be Grounded on DS1291 |
| GND3 | - | Missing on DS1290<br>Must Be Grounded on DS1291 |

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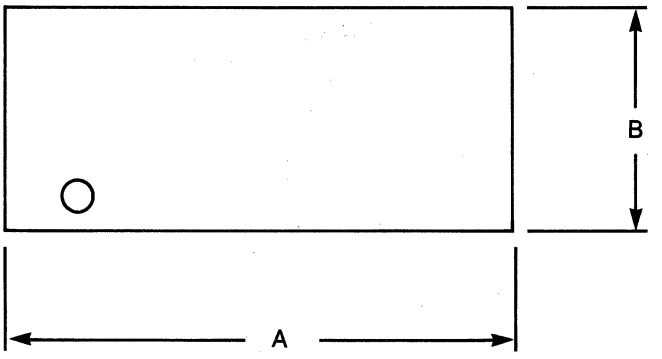
### DESCRIPTION

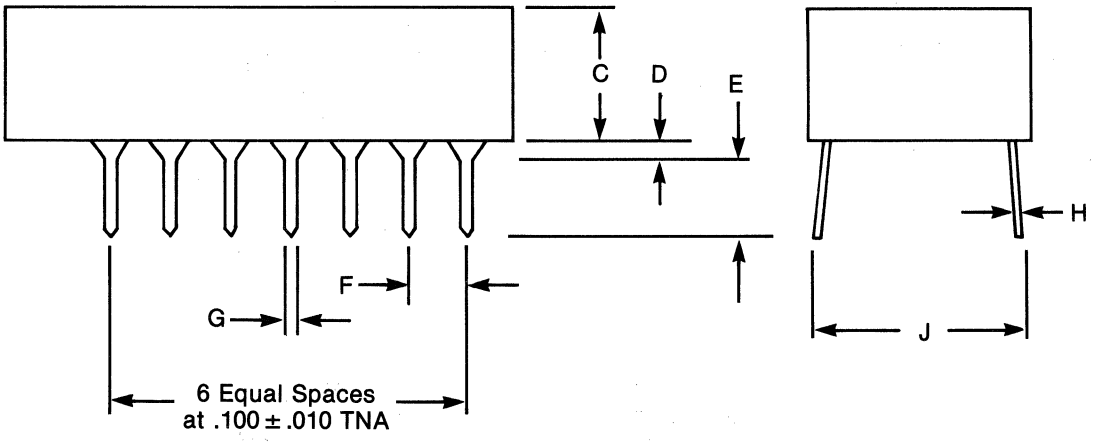
The DS1290 Eliminator replaces manual switches used to option printed circuit boards. Eight output pins can be set to a logic level or interrogated by three signals, clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1290 will maintain high or low level output duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

See the data sheet for the DS1292 for electrical specifications and operation.

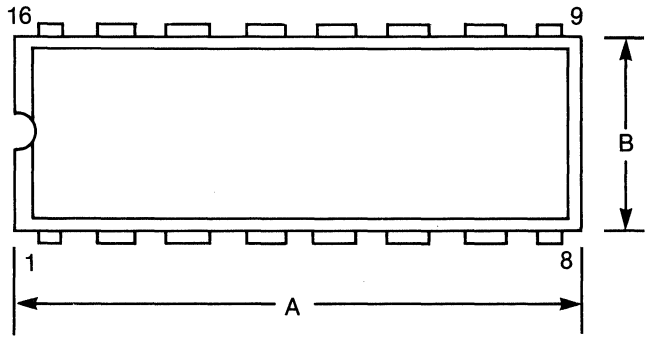
# Nonvolatile Eliminator
# DS1290

| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .840 | .860 |
| B | .370 | .390 |
| C | .230 | .250 |
| D | .020 | .040 |
| E | .115 | .135 |
| F | .090 | .110 |
| G | .015 | .021 |
| H | .008 | .012 |
| J | .300 | .350 |

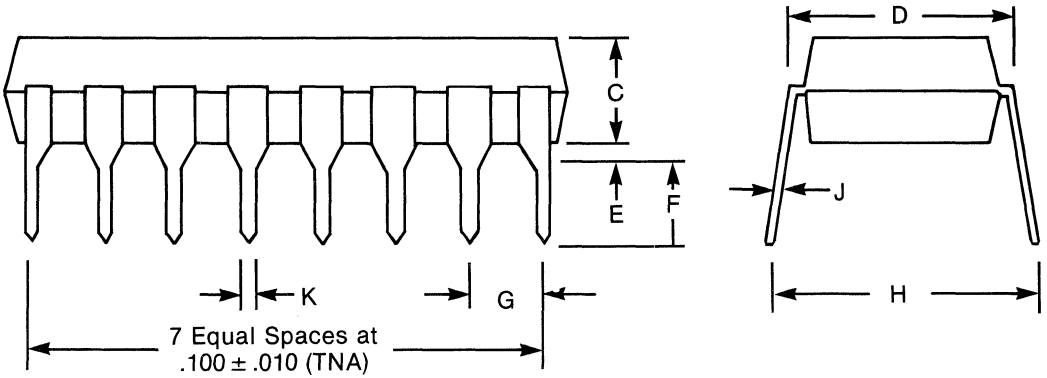


# Volatile Eliminator
# DS1291




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | .740 | .780 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .030 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .300 | .350 |
| J | .008 | .012 |
| K | .015 | .021 |



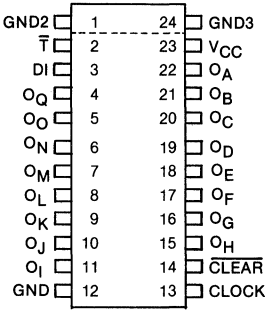
# Dallas Semiconductor
## *Eliminator*

# *DS1292*
# *DS1293*

### FEATURES

- Replaces 16 hard-to-get-at manual switches
- Option printed circuit board via software
- DS1292 remembers settings in the absence of power
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Interface
- Low power CMOS
- DS1293 Volatile Eliminator
- Change of switch settings occur simultaneously
- Over 10 years of data retention

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $\overline{T}$ | - Transfer |
| DI | - Data Input |
| $O_AO_Q$ | - Switch Outputs |
| CLOCK | - Clock Input |
| $\overline{CLEAR}$ | - All Outputs Set Low |
| $V_{CC}$ | - +5 Volts |
| GND | - Ground |
| GND2 | - Missing on DS1292<br>Must Be Grounded on DS1293 |
| GND3 | - Missing on DS1292<br>Must Be Grounded on DS1293 |

### DESCRIPTION

The DS1292 Eliminator replaces manual switches used to option printed circuit boards. Sixteen output pins can be set to a logic level or interrogated by three signals, clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1292 will maintain high or low level output duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

## OPERATION

The DS1292/DS1293 Eliminator is a 16-bit shift register which has a clocked serial input, an asynchronous clear, and an output transfer contro! (see Block Diagram, Figure 1). Data can be entered into the 16-bit register only when the transfer input ($\overline{T}$) is at a high level. While at a high level the transfer function allows serial entry of data via the data input pin (DI). The outputs $0_Q$ through $0_B$ remain in the state which was set prior to $\overline{T}$ being driven to a high level. Output $0_A$ will change state as new data is entered. This output provides a method of "feeding back" actual output settings prior to setting the $\overline{T}$ input low (Figure 2). When the $\overline{T}$ input is driven low, new data which has been input into the 16-bit shift register is now locked at outputs $0_Q$ through $0_A$. When the $\overline{T}$ input is low, all clock and data inputs are ignored. Valid data is clocked into the eliminator while $\overline{T}$ is high on the low-to-high transition of the CLOCK input. Data may be changed while the CLOCK input is high or low, but only data meeting the setup requirements will enter the shift register. The $\overline{CLEAR}$ input will always set all outputs to low level regardless of the level of the CLOCK or $\overline{T}$ input.

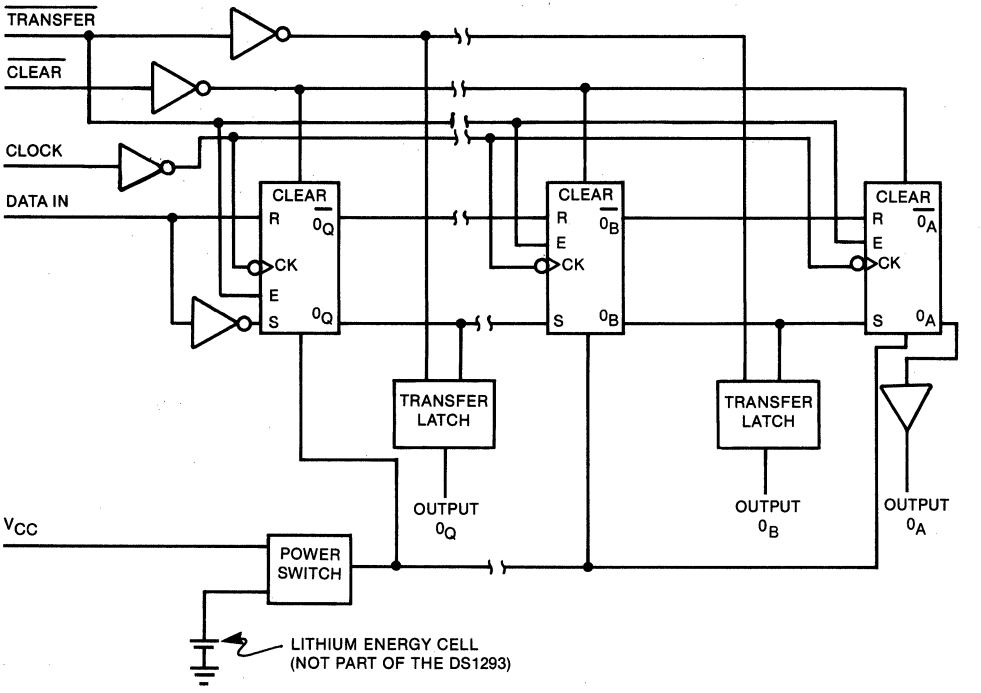
## DATA RETENTION MODE

The DS1292 Eliminator provides full functional capability when $V_{CC}$ is greater than 4.5 volts and will ignore all inputs when $V_{CC}$ reaches 4.25 volts typical. In this manner, the settings of each register remain intact during power transients. As $V_{CC}$ falls below approximately 3 volts, an internal power switching circuit connects a lithium energy source to the shift register to maintain data. During power up when $V_{CC}$ rises above approximately 3 volts, the power switching circuit connects external $V_{CC}$ to the shift register and disconnects the lithium energy source. Normal operation can resume after $V_{CC}$ exceeds 4.5 volts for a time of 10 MS minimum. During power transients the 16 outputs will track the level of $V_{CC}$ if set to Logic 1 and will remain at ground level if set to Logic Zero.

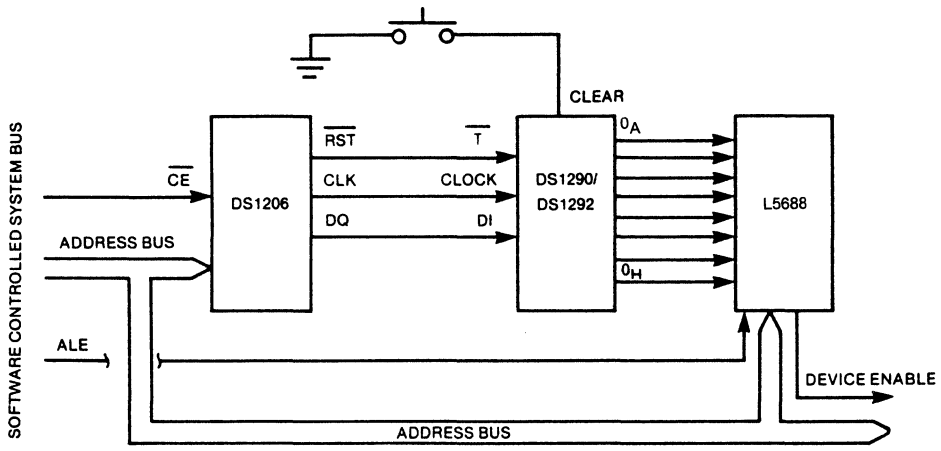
## TYPICAL APPLICATION—ELIMINATOR

The DS1292 and DS1206 combine to make a programmable nonvolatile DIP switch which can be transparently set in systems without disturbing other operations. Because the switches are nonvolatile, the switches need only to be set once as they will remain in the programmed state indefinitely. The block diagram of Figure 2 shows the Eliminator implemented with the DS1206 Phantom Interface. The DS1206 samples four address lines and the chip enable signal, looking for a special pattern for 24 consecutive cycles (see the Data Sheet for the DS1206). When a proper match is found, the address lines and one data line become control and data signals which are used to program and verify the settings of the DS1292. All of the signaling sent to the DS1206 and subsequently to the DS1292 are generated by software controlled read cycles which have no effect on the rest of system operation. The clear signal can be used to restore a system back to an unconfigured state.

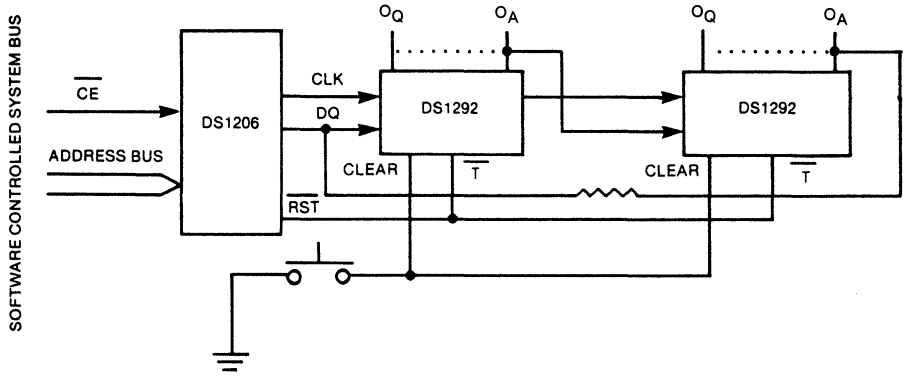
**BLOCK DIAGRAM—DS1292/DS1293** Figure 1



**PHANTOM INTERFACE AND ELIMINATOR TYPICAL APPLICATION** Figure 2




**MODULAR EXPANSION OF THE ELIMINATOR** Figure 3

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**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -3.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 70°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V | 1 |
| Logic 0 | $V_{IL}$ | −0.3 | | +0.8 | V | 1 |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}$ = 4.5 to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CC}$ | | 3 | 5 | mA | |
| Input Leakage | $I_{IL}$ | −1.0 | | +1.0 | uA | 4 |
| Output Leakage | $I_{LO}$ | −1.0 | | +1.0 | uA | |
| Logic 1 Output @2.4 V | $I_{OH}$ | −1.0 | | | mA | 2 |
| Logic 0 Output @0.4 V | $I_{OL}$ | | | 4.0 | mA | 2 |

## CAPACITANCE

($t_A = 25\,°C$)

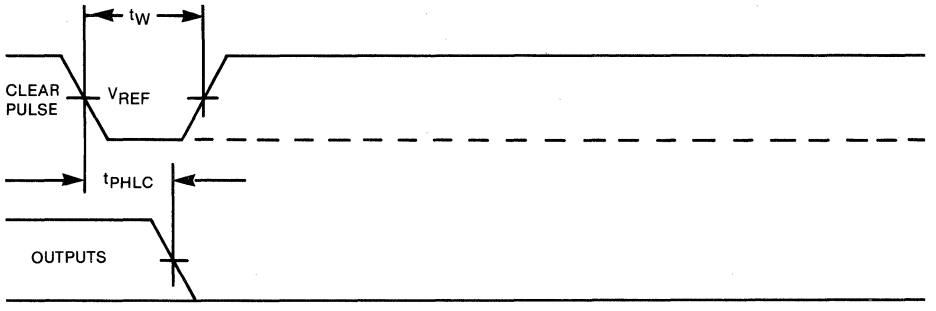
| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | 7 | pF | |

## A.C. ELECTRICAL CHARACTERISTICS

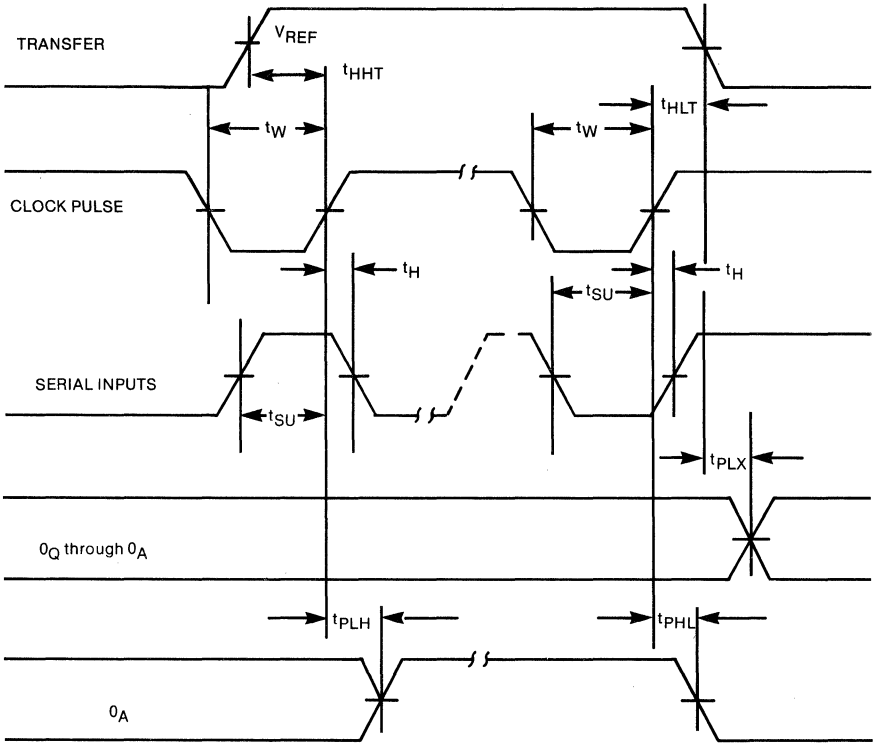
(0 °C to 70 °C, $V_{CC} = 5V \pm 10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Clock Frequency | $f_{CLOCK}$ | | | 10 | MHz | |
| Width of Clock Pulse | $tw_{CLOCK}$ | 50 | | | ns | 3 |
| Width of Clear Pulse | $tw_{CLEAR}$ | 50 | | | ns | 3 |
| Data Set-Up Time | $t_{SU}$ | 30 | | | ns | 3 |
| Data Hold Time | $t_H$ | 10 | | | ns | 3 |
| Propagation Delay Time High to Low Level Clear to Output | $t_{PHLC}$ | | | 70 | ns | 3 |
| Propagation Delay Time Low to High Level Clock to Output | $t_{PLH}$ | | | 50 | ns | 3 |
| Propagation Delay Time High to Low Level Clock to Output | $t_{PHL}$ | | | 50 | ns | 3 |
| Recovering on Power Up | $t_{REC}$ | 10 | | | ms | |
| Propagation Delay Time High to Low Level Transfer to O Out | $t_{PLX}$ | | | 50 | ns | 3 |
| Transfer High to Clock Input High | $t_{HHT}$ | 50 | | | ns | 3 |
| Transfer Low from Clock Input High | $t_{HLT}$ | 50 | | | ns | 3 |

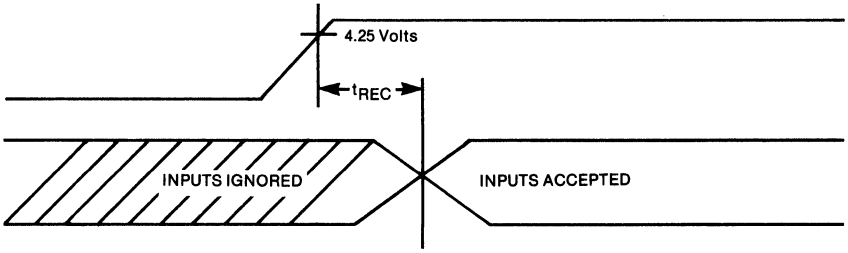
## TIMING DIAGRAM—CLEAR CONTROL[3]




## TIMING DIGRAM—TRANSFER DATA[3]



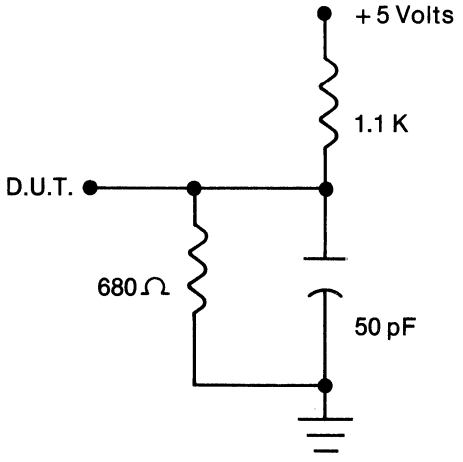
**TIMING DIAGRAM—POWER-UP[3]**




**NOTES:**

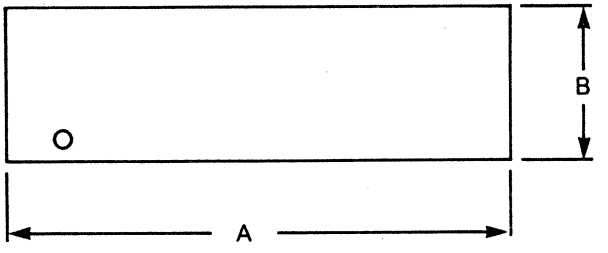
1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 4.
3. $V_{REF}$ = 1.5 Volts.
4. Clock and transfer inputs have internal pull-down resistors of 20KΩ typical. Clear has an internal pull-up resistor of 20KΩ typical.

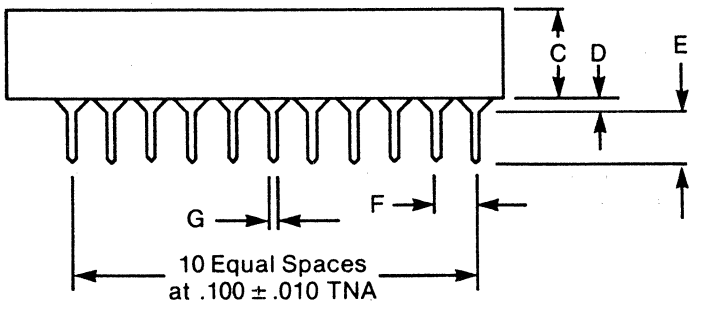
**OUTPUT LOAD** Figure 4

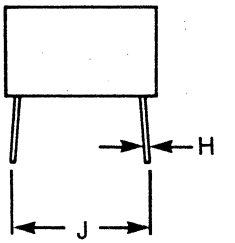


# *Nonvolatile Eliminator*
# *DS1292*

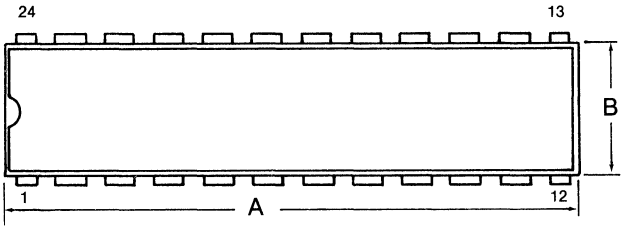
| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.236 | 1.256 |
| B | .370 | .390 |
| C | .230 | .250 |
| D | .020 | .040 |
| E | .115 | .135 |
| F | .090 | .110 |
| G | .015 | .021 |
| H | .008 | .012 |
| J | .300 | .350 |



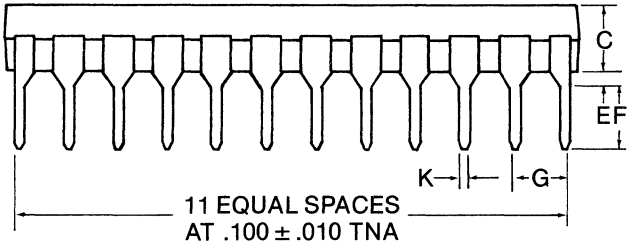



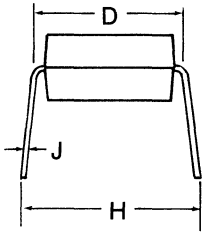



# *Volatile Eliminator*
# *DS1293*




| DIM. | INCHES | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.150 | 1.190 |
| B | .240 | .260 |
| C | .120 | .140 |
| D | .290 | .310 |
| E | .020 | .040 |
| F | .110 | .130 |
| G | .090 | .110 |
| H | .325 | .375 |
| J | .008 | .012 |
| K | .015 | .021 |

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# SipStik™ Products

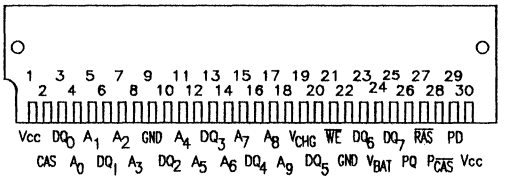
# Dallas Semiconductor
## *DRAM SIPSTIK™*

# PRODUCT PREVIEW
## *DS2209/2219*

### FEATURES

- Maintaines data in the absence of system power.
- Compatible with existing DRAM SIMM applications
- Normal operating mode completely unaffected
- Nonvolatile circuitry transparent and independent from host system
- No additional components required
- Conforms to popular JEDEC standard 30 position SIMM DRAM module
- Accomodates either 6 volt primary energy cell or rechargable energy source
- Memory array available as 256K or 1024K bytes with optional parity bit
- $\overline{RAS}$ access time of 120ns, 150ns, or 200ns

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $V_{cc}$ | -+5 volt supply |
| GND | -Ground |
| $\overline{A_0}$-$\overline{A_8}$/$A_9$ | -Address Inputs |
| $\overline{WE}$ | -Write Enable |
| $\overline{RAS}$ | -Row Address Strobe |
| $\overline{CAS}$ | -Column Address Strobe |
| $DQ_0$-$DQ_7$ | -Data Inputs/Outputs |
| $V_{BAT}$ | -External Voltage Input |
| $V_{CHG}$ | -+12 Volt Supply |
| $\overline{PQ}$ | -Parity Data Output |
| PCAS | -Parity Column Address Strobe |
| PD | -Parity Data Input |

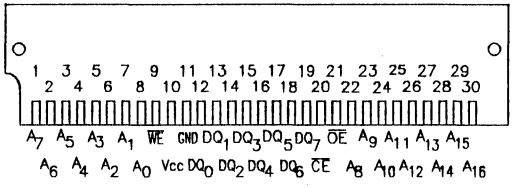
### DESCRIPTION

The DS2208/18 by 8 and DS2209/19 by 9 family of nonvolatile DRAM SIMM modules provide all necessary timing, refresh generation, and power down/power up sequencing necessary to maintain data integrity during system power failure. A 6 volt primary cell or a rechargable energy source can be used to support data retention. Available in 262,144 and 1,048,576 bytes, the memory modules conform to the standard 30 position SIMM pin configuration. The self contained memory maintenance circuitry resides transparently to host system eliminating the need for any additional components.

## FEATURES

- Data retention in the absence of $V_{cc}$
- Directly replaces volatile SRAM
- Employs popular JEDEC standard 30 position SIMM connection scheme
- Nonvolatile circuitry transparent and independent from host system
- No additional components
- 10 year data retention
- Organized as 128K bytes
- Available in 120ns, 150ns, and 200ns Read Access Time
- Full +/- 10% operating range
- Optional +/- 5% operating range
- Read cycle time equals write cycle time
- Unlimited write cycles
- Automatic write protection circuitry safeguards against data loss
- Wide operating temperature range of 0°C to 70°C

## PIN CONNECTIONS




## PIN NAMES

| | |
|---|---|
| $V_{cc}$ | - +5 volt supply |
| GND | - Ground |
| $A_0$-$A_{16}$ | - Address Inputs |
| $DQ_0$-$DQ_7$ | - Data Input/Output |
| $\overline{CE}$ | - Chip Enable |
| $\overline{OE}$ | - Output Enable |
| $\overline{WE}$ | - Write Enable |

## DESCRIPTION

The DS2217 is a self-contained 1,048,576 bit nonvolatile static RAM organized as 131,072 words by 8 bits. The nonvlatile memory contains all necessary control circuitry and energy sources to maintain data integrity in the absence of power for more than 10 years. The DS2217 conforms to the popular 30 position SIMM pinout requiring no additional circuitry.

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## OPERATION

The DS2217 SRAM SIMM is used like any standard static RAM. All of the nonvolatile circuitry resides transparently to the user. Decoding from upper order address lines is also integrated into the nonvolatile controller and is transparent to SRAM operation. Connection to the DS2217 is made by using an industry standard, 30-position SIMM socket (AMP part number 643930-1). These SIMM sockets are also available in double row and low profile angled variations.

## READ MODE

The DS2217 is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (chip enable) is active (low). The unique address specified by the 17 address inputs ($A_0$-$A_{16}$) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within $t_{ACC}$ (access time) after the last address input signal is stable, providing that $\overline{CE}$ (chip enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access. Read cycles can only occur when $V_{CC}$ is greater than 4.5 volts. When $V_{CC}$ is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

## WRITE MODE

The DS2217 is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge. Write cycles can occur only when $V_{CC}$ is greater than 4.5 volts. When $V_{CC}$ is less than 4.5 volts, the memory is write protected.

## DATA RETENTION MODE

The nonvolatile SIMM provides full functional capability for $V_{CC}$ greater than 4.5 volts and guarantees write protection for $V_{CC}$ less than 4.5 volts. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The DS2217 constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects the external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts.

The DS2217 checks battery status to warn of potential data loss. Each time that $V_{CC}$ power is restored to the DS2217 the battery is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The SRAM SIMM provides battery redundancy. The DS2217 provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to 85°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED D.C. OPERATING CONDITIONS** (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | | $V_{CC}+0.3$ | V |
| Input Low Voltage | $V_{IL}$ | −0.3 | | +0.8 | V |

**D.C. ELECTRICAL CHARACTERISTICS** (0°C to 70°C, $V_{CC}=5V\pm10\%$)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | −60 | | +60 | *u*A |
| I/O Leakage Current | $I_{LO}$ | −10 | | +10 | *u*A |
| Output Current @2.4V | $I_{OH}$ | −1.0 | −2.0 | | mA |
| Output Current @0.4V | $I_{OL}$ | 2.0 | 3.0 | | mA |
| Standby Current $\overline{CE}=2.2V$ | $I_{CC}$ | | 15 | 25 | mA |
| Operating Current | $I_{CC}$ | | 50 | 100 | mA |

**CAPACITANCE** ($t_A=25°C$)

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 50 | pF | |
| Output Capacitance | $C_{OUT}$ | 50 | pF | |

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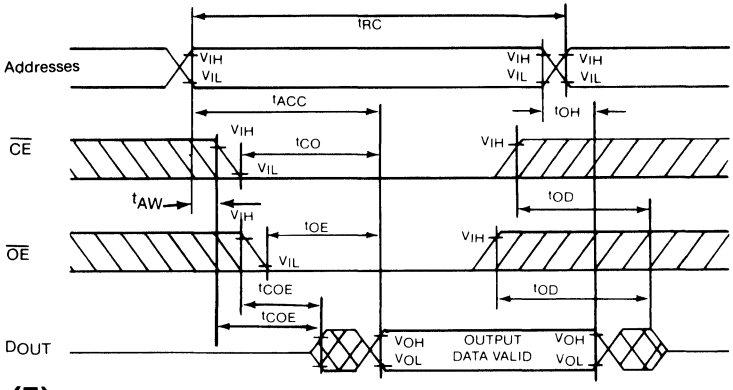
## A.C. ELECTRICAL CHARACTERISTICS

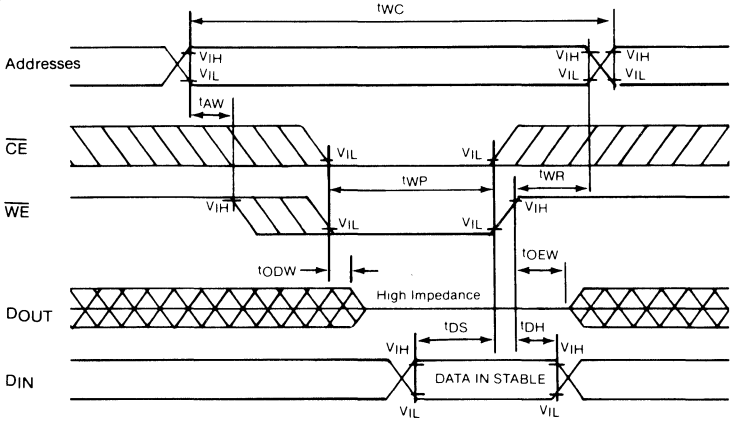
(0 °C to +70 °C, $V_{CC}$ = 5.0V ± 10%)

| | | DS2217-120 | | DS2217-150 | | DS2217-200 | | | |
|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Read Cycle Time | $t_{RC}$ | 120 | | 150 | | 200 | | ns | |
| Access Time | $t_{ACC}$ | | 120 | | 150 | | 200 | ns | |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | 60 | | 70 | | 100 | ns | |
| $\overline{OE}$ to Output Valid | $t_{CO}$ | | 120 | | 150 | | 200 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 5 | | 10 | | 10 | | ns | |
| Output High Z from Deselection | $t_{OD}$ | | 40 | | 70 | | 100 | ns | |
| Output Hold From Address Change | $t_{OH}$ | 10 | | 10 | | 10 | | ns | |
| Write Cycle Time | $t_{WC}$ | 120 | | 150 | | 200 | | ns | |
| Write Pulse Width | $t_{WP}$ | 90 | | 100 | | 170 | | ns | 3 |
| Address Set Up Time | $t_{AW}$ | 0 | | 0 | | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 0 | 10 | | 10 | | | ns | |
| Output High Z From $\overline{WE}$ | $t_{ODW}$ | | 40 | | 70 | | 80 | ns | |
| Output Active From $\overline{WE}$ | $t_{OEW}$ | 5 | | 10 | | 10 | | ns | 8 |
| Data Set Up Time | $t_{DS}$ | 50 | | 60 | | 80 | | ns | 4 |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | ns | 4,5 |

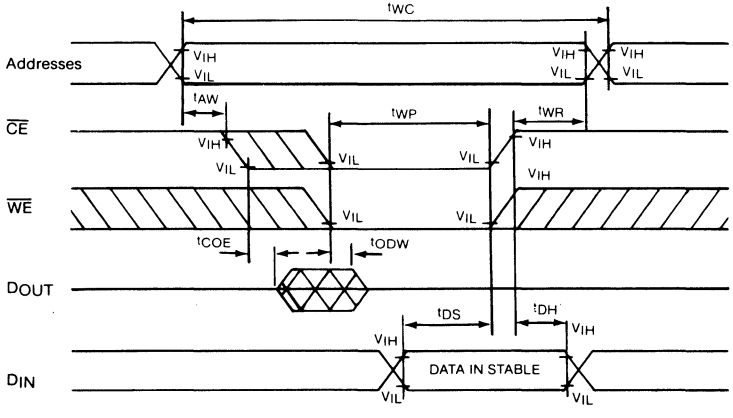
## READ CYCLE (1)




## WRITE CYCLE 1 (2), (6), (7)




## WRITE CYCLE 2 (2), (8)

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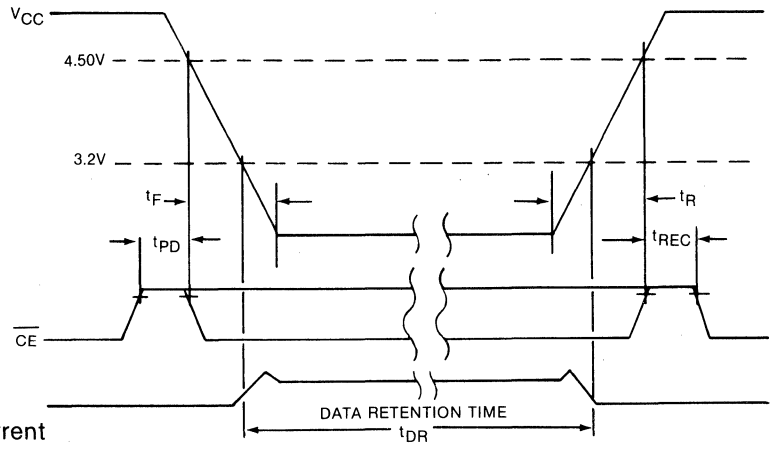
## POWER-DOWN/POWER-UP CONDITION




Leakage Current $I_L$ supplied from lithium cell

## POWER-DOWN/POWER-UP TIMING

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{PD}$ | $\overline{CE}$ at $V_{IH}$ before Power Down | 0 | | $\mu$s | |
| $t_F$ | $V_{CC}$ slew from 4.5V to 0V ($\overline{CE}$ at $V_{IH}$) | 100 | | $\mu$s | |
| $t_R$ | $V_{CC}$ slew from 0V to 4.5V ($\overline{CE}$ at $V_{IH}$) | 0 | | $\mu$s | |
| $t_{REC}$ | $\overline{CE}$ at $V_{IH}$ after Power Up | 2 | 125 | ms | |

($t_A$ = 25°C)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $t_{DR}$ | Expected Data Retention Time | 10 | | years | 9 |

**WARNING:**
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE} = V_{IH}$ or $V_{IL}$. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical "AND" of $\overline{CE}$ and $\overline{WE}$.
   $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. $t_{DH}$ is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then $t_{DH} = 20$ ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If the $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS2217 is marketed with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected $t_{DR}$ is defined as starting at the date of manufacture.

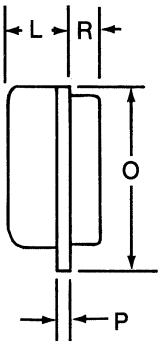
**D.C. TEST CONDITIONS**

Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

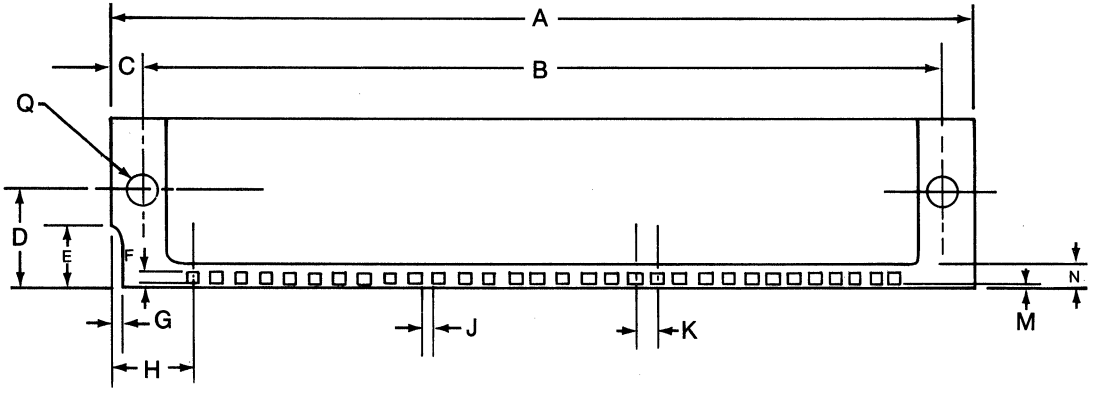
**A.C. TEST CONDITIONS**

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0 V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

# DS2217
# Nonvolatile SRAM SIMM




| DIM. | INCHES | |
|---|---|---|
| A | 3.500 | |
| B | 3.234 | |
| C | 0.133 | |
| D | 0.400 | |
| E | 0.250 | |
| F | 0.070 | Min. |
| G | 0.080 | |
| H | 0.300 | |
| J | 0.070 | |
| K | 0.100 | |
| L | 0.180 | Max. |
| M | 0.010 | Max. |
| N | 0.100 | Min. |
| O | 0.850 | Max. |
| P | 0.050 | $^{+0.005}_{-0.004}$ |
| Q | 0.125 | Dia. thru |
| R | 0.120 | Max. |



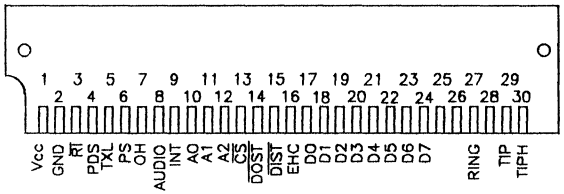
# Dallas Semiconductor
## *MODEM SIPSTIK™*

# PRODUCT PREVIEW
# DS2245

## FEATURES

- Complete modem system interfaces parallel uP bus directly to phone line
- Bell 212A/103 and V.22/21 compatible
- Complete "AT" command set in firmware
- Contains FCC Part 68 and Canadian CS-03 approved DAA
- Employs popular JEDEC standard 30-position SIMM connection scheme with transformer
- Single +5 Volt supply operation
- DTMF and pulse dialing
- Call progress monitoring

## PIN CONNECTIONS




## DESCRIPTION

The DS2245 is a high-level comunications subsystem manufactured in a single in-line figure to permit integration into a variety of applications, especially when space is a concern. An integral FCC and Canadian approved DAA interface allows the DS2245 to be directly connected to the public switched telephone network. Embedded firmware in this component completely implements the standard "AT" command set which assures compatibility with popular communications software. The DS2245 also emulates the 8250B UART which means that it can be directly connected to an IBM-PC/XT/AT system bus. Operation at +5 volts makes this module an attractive choice for low-power applications such as lap-top computers.

Included in the DS2245 are all the modulation/demodulation and filtering circuitry necessary for compatibility with Bell 212A/103 type modems, as well as, the CCITT V.22/21 series modems. Also provided is the capability for call progress monitoring, as well as, DTMF and pulse dialing. Three loopback modes --analog, digital, and remote-- are available for line and component testing. A programmable audio output can be used for monitoring the telephone line signals. The DS2245 plugs into the SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles.

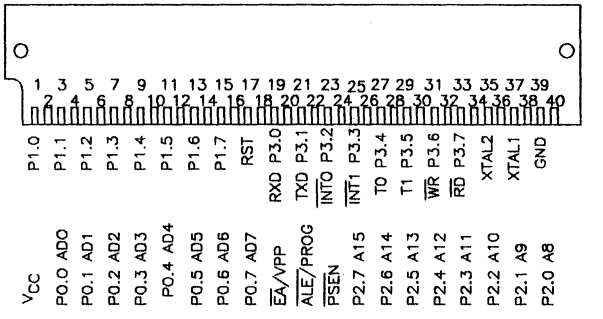
**Dallas Semiconductor**
***Microcontroller SIPSTIK™***

# PRODUCT PREVIEW
## *DS2250*

## FEATURES

- 40-position SIMM connection scheme
- Nonvolatile SRAM for program and/or data
- Capable of modifying its own program and/or data memory
- Program downloading via an on-chip full duplex serial port
- Adjustable partition between program and data memory
- Completely crash-proof: the program and data memories and all data registers are maintained in absence of power
- All 32 port pins available for I/O
- Automatic restart on detection of errant software execution
- Orderly shutdown and automatic restart on power up/down
- Program and data memory secure, with a tamper proof on-chip encryptor

## PIN CONNECTIONS




## ORDERING INFORMATION

DS2250 XX – XX

| CLOCK | FREQ. |
|---|---|
| –12 | 12MHz |
| –16 | 16MHz |

| PROGRAM/DATA RAM | |
|---|---|
| 8 | 8Kbytes |
| 32 | 32Kbytes |
| 64 | 64Kbytes |

## DESCRIPTION

The DS2250 Microcontroller SipStik stays up-to-date because it was designed for change. Unlike rigid ROM or EPROM based microcontrollers, all of the Microcomtroller memory is high performance, read/write, and nonvolatile for more than ten years. the DS2250 is equipped with nonvolatile SRAM which can be dynamically partitioned to fit program and data storage requirements of a particular task. As a result of sophisticated crashproofing circuitry, processing of a task can resume after a power outage. A built-in encryptor prevents unauthorized access to resident application software. The pinout and instruction set match the industry standard 8051 microcontroller. The DS2250 plugs into SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles.

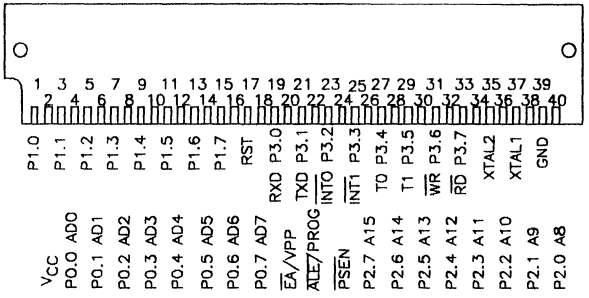
**Dallas Semiconductor**
***Microcontroller SIPSTIK™***

# PRODUCT PREVIEW
# *DS2250T*

## FEATURES

- Soft Microcontroller Siptik with embedded real-time clock function
- Capable of modifying its own program and/or data memory
- Program downloading via an on-chip full duplex serial port
- Adjustable partition between program and data memory
- Completely crash-proof: the program and data memories and all data registers are maintained in absence of power
- All 32 port pins available for I/O
- Automatic restart on detection of errant software execution
- Orderly shutdown and automatic restart on power up/down
- Program and data memory secure, with a tamper proof on-chip encryptor
- On-chip full duplex serial I/O port
- Two on-chip timer/event counters
- Compatible with industry standard 8051 instruction set

## PIN CONNECTIONS




## ORDERING INFORMATION

DS2250T XX XX

Speed Grade

| | |
|---|---|
| 12 | 12 MHz |
| 16 | 16 MHz |

Program/Data RAM

| | |
|---|---|
| 8 | 8 Kbytes |
| 32 | 32 Kbytes |

## DESCRIPTION

The DS2250 Microcontroller SipStik incorporates all of the features of the DS2250 along with the addtion of a built-in real-time clock/calender function. This function itself is identical to that performed by the DS1215 Timekeeper. The real-time clock is memory-mapped on the internal Embedded RAM address/data bus. As a result, it may be accessed by software as if it were Embedded Data RAM using the "LDX" set of instructions. Accesses to the real-time clock take place with no effect on I/O port pins. The DS2250T plugs into the SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles.

# Wireless Products

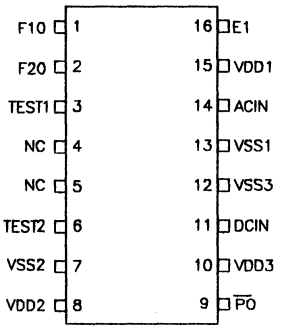
# Dallas Semiconductor
## *Micro Power Receiver*

# PRODUCT PREVIEW
## *DS1203-200*
## *-50*

### FEATURES

- Dual band pass receiver discriminates noise and minimizes power
- Ultra low power listening channel gives longevity to 3 volt lithium supply
- 20 KHZ channel continuously listens then powers up a 200 KHZ channel on demand when used with the DS1209
- Optional 5 KHZ/50 KHZ bandpass (DS1203-50)
- Electronic freshness seal preserves lithium supply during storage
- 100 micro volt input signal drives output to CMOS levels
- Space saving 16 pin small outline package surface mounts
- Interfaces directly with DS1209 2 to 3 Wire Converter

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| VDD1-VDD3 | +3 VOLT SUPPLY |
| F10 | 200 KHZ OR 50 KHZ OUTPUT |
| F20 | 20 KHZ OR 5 KHZ OUTPUT |
| ACIN-DCIN | INPUT SIGNALS |
| E1 | 200 KHZ OR 50 KHZ ENABLE INPUT |
| $\overline{PO}$ | POWER OFF |
| VSS1-VSS3 | SIGNAL GROUND |
| TEST1 TEST2 | TEST SIGNALS |
| NC | NO CONNECTS |

### DESCRIPTION

The DS1203 is a CMOS ultra low power integrated circuit designed to discriminate and amplify a low level input from a wireless communication link such as RF, IR, microwave or magnetic field. The receiver can sleep in a minimized power down state yet wake up for high speed data transfer on demand. This feature allows remote applications to be permanently powered by a single 3 volt lithium supply. A 2 KHZ input signal also provides a "freshness seal" so that the lithium energy source can be electrically disconnected until initial operation. The low power consumption and space-saving 16 pin small outline packaging of the DS1203 make it ideal for portable applications.

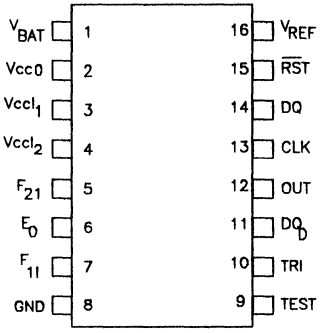
# Dallas Semiconductor
## *2 to 3 Wire Converter*

# PRODUCT PREVIEW
## *DS1209*

### FEATURES

- Adapts a 2 wire serial port to a 3 wire serial port
- Half duplex operation
- Counts the number of incoming pulses then compares to 4 adjustable ranges for interpretation
- Each range represents a specific command
- Ranging tolerates transmission errors
- Low power lithium operate or lithium back-up modes
- Directly interfaces to DS1203 Micro Power Receiver
- Space saving 16 pin small outline package for surface mounting

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| $Vccl_1$-$Vccl_2$ | SUPPLY INPUTS |
| Vcco | SWITCHED OUTPUT |
| $V_{BAT}$ | +3 VOLT LITHIUM INPUT |
| $V_{REF}$ | REFERENCE VOLTAGE |
| $F_{11}$ | 200 KHZ INPUT |
| $F_{21}$ | 20 KHZ INPUT |
| OUT | OUTPUT |
| $E_o$ | 200 KHZ ENABLE OUTPUT |
| $DQ_D$ | DQ DISABLED |
| TRI | 3 WIRE PORT TRISTATE |
| $\overline{RST}$ | RESET |
| DQ | DATA INPUT/OUTPUT |
| CLK | CLOCK |
| GND | GROUND |
| TEST | TEST PIN |

### DESCRIPTION

The DS1209 is a low power CMOS integrated circuit which accepts an up to 256 count pulse train and synthesizes 4 specific control commands. These commands generate a 3 wire communication port. This 3 wire port consists of RST, DQ, and CLK signals which can be used to communicate with Dallas Semiconductor DS1201 Electronic Tag, DS1204 Key, DS1207 Timekey, DS5000 Soft Microcontroller, or any other device employing this industry standard 3 wire port. An output pin is driven for the return transmission link and can in turn gate a variety of transmitting devices. The low power consumption and space-saving 16 pin small outline packaging of the DS1209 make it ideal for portable applications.

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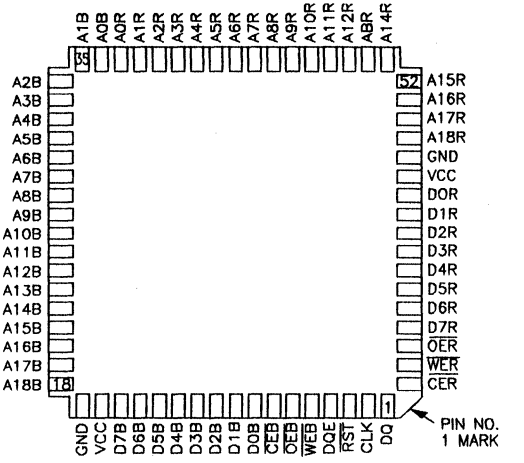
# Dallas Semiconductor
## *Byte Wide To Serial Converter*

# PRODUCT PREVIEW
## *DS1280*

## FEATURES

- Adapts JEDEC byte wide memory to a 3 wire serial port
- Supports 512k bytes of memory
- Provides arbitration mechanisms for dual port operation
- CMOS circuitry design for battery backup and battery operate applications
- Cyclic redundancy check monitors serial data transmission for error
- 68 pin PLCC surface mount package

## PIN CONNECTIONS




## PIN NAMES

$\overline{RST}$ - Reset For Serial Port
DQ - Data Input/Output For Serial Port
CLK - Clock Input For Serial Port
DQE - Serial Port Active Output
$\overline{CEB}$ - System Bus Enable
$\overline{OEB}$ - System Bus Read Enable
$\overline{WEB}$ - System Bus Write Enable
A0B-A18B - System Address Bus
D0B-D7B - System Data Bus
$\overline{CER}$ - Ram Chip Enable
$\overline{WER}$ - Ram Write Enagle
$\overline{OER}$ - Ram Output Enable
A0R-A18R - Ram Address Bus
D0R-D7R - Ram Data Bus
GND = Ground
Vcc = +5 Volts

## DESCRIPTION

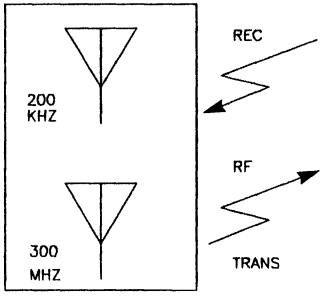
The DS1280 adds a 3 wire serial port to a byte wide Static RAM yet maintains the existing byte wide port. Memory capacity of up to 512K bytes can be addressed directly. Arbitration between the serial and byte wide port is accomplished by handshaking or using predictable idle time as an access window. The serial port requires a six byte protocol to set up memory transfers. Cyclic Redundancy Check circuitry is included to monitor serial data transmission for error.

# Dallas Semiconductor
## *E-Key*

# PRODUCT PREVIEW
## *DS6065*

## FEATURES

- Wireless RF link up to 5 feet
- 256 count pulse train derives specific commands
- Cannot be deciphered by reverse engineering
- Compact size and shape
- Over 10 years of data retention with 10 million transactions
- Unreadable 64 bit security match code prevents deciphering by exhaustive search with over $10^{19}$ possibilities
- Low power listening mode preserves lithium battery
- 100 microvolt input signal wakes up communication link
- Exclusive blank keys upon request
- Rugged and durable
- RF link established directly to DS6068 RF Communicator




## SIGNAL NAMES

TRANS -300 MHZ Transmitter
REC -200 KHZ Receiver

## DESCRIPTION

The DS6065 E-Key is a miniature low power electronic key with a self contained RF transmitter/receiver pair providing a wireless communication link to a host system. Low power listening and wake up functions are provided by the DS1203 micro power receiver. The DS1209 2 to 3 wire converter performs the pulse train derivation of read and write commands to the DS1204 electronic key. All integrated circuits, receiver/transmitter antenna, and energy source are contained in a small, rugged and durable sealed unit. For more information on the micropower receiver, 2 to 3 wire converter, and the electronic key please review the DS1203, DS1209, and DS1204 data sheets respectively.

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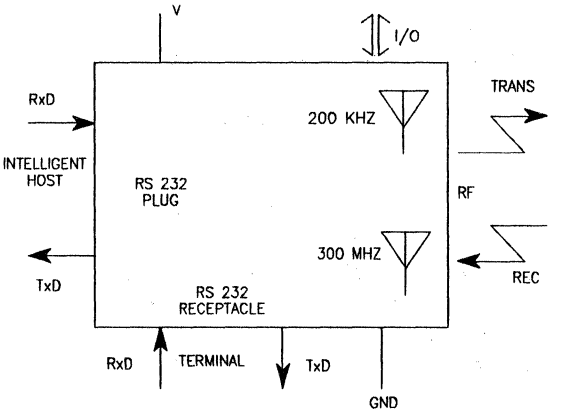
# Dallas Semiconductor
## *RF Communicator*

# PRODUCT PREVIEW
## *DS6068*

### FEATURES

- Provides wireless 5 foot link to DS6065 E-Key, DS6060 Cartridge, DS6040 Portable Transceiver and Hand Held Terminals
- 200 KHZ transmitter and 300 MHZ receiver frequencies
- Flexible microprocessor based subsystem
- Industry standard RS232 interface
- Connects to stand alone host or inserts between existing host/terminal wiring
- Nonvolatile SRAM accepts application software updates and logs transactions
- Miniature 25 position D-sub plug and receptacle for conventional wiring
- Single 12 volt supply
- Optional Real Time Clock
- Optional input/output pins for touch pad and door entry actuator

### PIN CONNECTIONS




### PIN NAMES

| | |
|---|---|
| RxD | RECEIVE DATA |
| TxD | TRANSMIT DATA |
| TRANS | TRANSMITTER 200 KHZ |
| REC | RECEIVER 300 MHZ |
| I/O | INPUT/OUTPUT |
| V | +12 VOLT SUPPLY |
| GND | GROUND |

### DESCRIPTION

The DS6068 is a radio frequency transmitter and receiver which can directly interface to a stand alone host such as a P.C. via an industry standard RS232 serial port. Furthermore, the DS6068 can transparently reside between an intelligent host and slave terminal yet be activated under software command. Internal nonvolatile static RAM and Real Time Clock allows for data logging, software updating, and time stamping transactions.

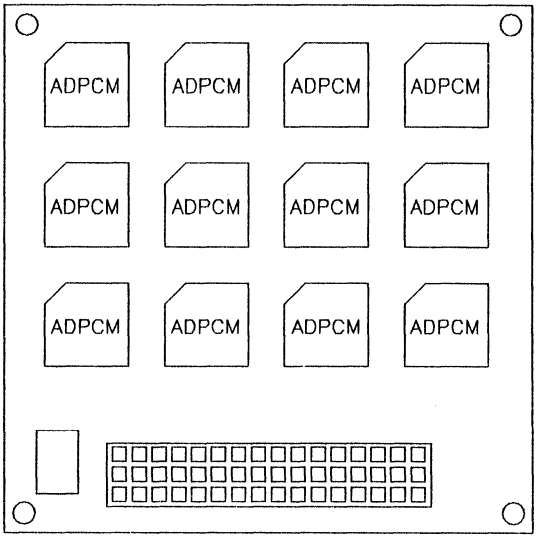
# Telecommunications

# Dallas Semiconductor
## *ADPCM Array*

## *DS2157*
## *DS2158*

### FEATURES

- High-density multi-channel speech compression system. Provides 24 full duplex channels in a 3 x 3 inch board
- Based on high-performance DS2167/68 ADPCM processors. Compatible with standard algorithms. DS2157 supports July 1986 T1Y1 recommended algorithm. DS2158 supports CCITT G.721 algorithm
- Flexible data busing scheme to accommodate user's backplane data format and rate.
- Microcontroller compatible port for system configuration. On-board power monitor provides system reset.
- Arrays are easily cascaded for even higher system density




### DESCRIPTION

The DS2157 and DS2158 Compression Arrays use surface-mount technology and the Dallas Semiconductor DS2167/68 ADPCM processors to yield 24 full-duplex channels in 9 square inches. The DS2157 array features the DS2167 processor which implements the July 1986 T1Y1 recommended ADPCM algorithm. The DS2158 array features the DS2168 processor which implements the CCITT G.721 algorithm. The PCM data interfaces are organized into four independent buses, which may be configured to best suit the data format on the user's system backplane. The array also includes input signal buffering and a power-monitor reset circuit.

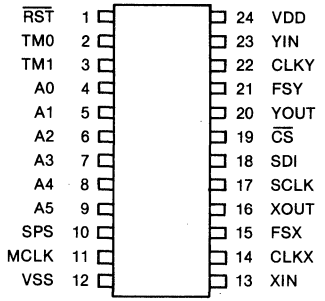
# Dallas Semiconductor
# ADPCM Processor

# DS2167
# DS2168

## FEATURES

- Speech compression chip compatible with standard ADPCM algorithms:
  - DS2167 supports "new" T1Y1 recommendations (July 1986) and "new" CCITT G.721 recommendations
  - DS2168 supports "old" CCITT G.721 recommendations
- Dual independent channel architecture—device may be programmed to perform full duplex , 2-channel expansions, or 2-channel compressions
- Interconnects directly with *u*-law or A-law combo-codec devices
- Serial PCM and control port interfaces minimize "glue logic" in multiple channel applications
  - On-chip channel counters identify input and output timeslots in TDM-based systems
  - Unique addressing scheme simplifies device control; 3-wire port shared among 64 devices
  - Bypass and idle features allow dynamic allocation of channel bandwidth, minimize system power requirements
- Hardware mode intended for stand-alone use
  - No host processor required
  - Ideal for voice mail applications
- 28-pin surface-mount package available, designated DS2167Q/ DS2168Q

## PIN CONNECTIONS




## DESCRIPTION

The DS2167 and DS2168 are dedicated digital signal processor (DSP) CMOS chips optimized for Adaptive Differential Pulse Code Modulation (ADPCM) based speech compression algorithms. The devices halve the transmission bandwidth of "toll quality" voice from 64K to 32K bits/second and are utilized in PCM-based telephony networks.

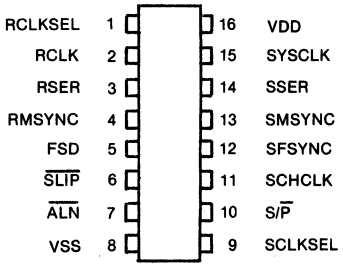
# Dallas Semiconductor
## *T1/CEPT Elastic Store*

## *DS2175*

### FEATURES

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop-timed and system-timed data streams on frame boundaries
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- Comprehensive on-chip "slip" control logic
  - Slips occur only on frame boundaries
  - Outputs report slip occurrences and direction
  - Align feature allows buffer to be recentered at any time
  - Buffer depth easily monitored
- Compatible with DS2180 T1 and DS2181 CEPT Transceivers
- Industrial temperature range of −40° to +85°C available, designated DS2175IND

### PIN CONNECTIONS




### DESCRIPTION

The DS2175 is a low-power CMOS elastic-store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1—1.544 MHz) and European (CEPT—2.048 MHz) rate networks. The chip has several flexible operating modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

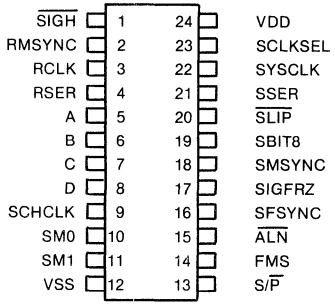
# Dallas Semiconductor
## *T1 Receive Buffer*

## *DS2176*

### FEATURES

- Synchronizes loop-timed and system-timed T1 data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip-compensated output indicates when signalling updates occur
- Compatible with DS2180 T1 Transceiver
- Surface mount package available, designated DS2176Q
- Industrial temperature range of −40°C to +85°C available, designated DS2176IND

### PIN CONNECTIONS




### DESCRIPTION

The DS2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24-lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

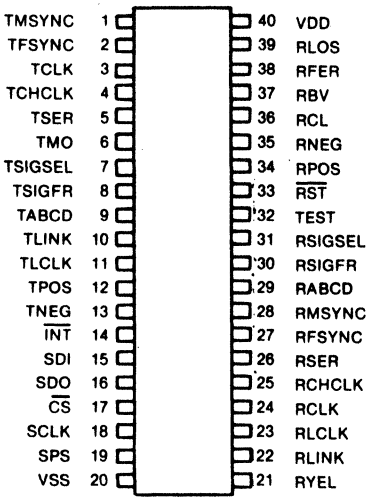
# Dallas Semiconductor
# *T1 Transceiver*

# *DS2180*
# *DS2180A*

## FEATURES

- Single chip DS1 rate transceiver
- Supports common framing standards
  - 12 frames/superframe "193S"
  - 24 frames/superframe "193E"
- Three zero suppression modes
  - B7 stuffing
  - B8ZS
  - Transparent
- Simple serial interface used for configuration, control, and status monitoring in "processor" mode
- DS2180A offers an enhanced feature set in processor mode and is software-compatible with the DS2180
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- 5V supply, low power CMOS technology
- Surface mount package available, designated DS2180Q

## PIN CONNECTIONS




## DESCRIPTION

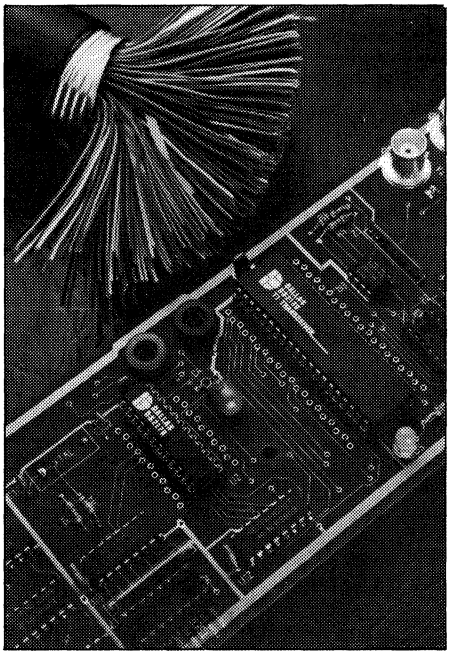
The DS2180 is a monolithic CMOS device designed to implement primary rate (1.544 MHz) T-carrier transmission systems. The 193S framing mode is intended to support existing Ft/Fs applications (12 frames/superframe). The 193E framing mode supports the extended superframe format (24 frames/superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

# Dallas Semiconductor
## *T1 Design Kit*

## *DS2180K*

### FEATURES

- Demonstrates key "hardware mode" attributes of the DS2180/DS2176 pair, such as:
  - Framing/synchronization
  - Link supervision and control
  - Signaling supervision
  - Rate adaption to equipment backplanes
- Expedites new designs by eliminating first-pass device prototyping
- Easily interfaced to user host controller for "software mode" evaluation
- User-supplied line interface allows direct connection to T1 lines
- Kit components include:
  - DS2180 T1 Transceiver
  - DS2176 T1 Receive Buffer
  - Printed circuit board
  - Support logic and clock generation circuitry
  - Applications and assembly information



### DESCRIPTION

The DS2180K allows the user to evaluate the performance of the DS2180 T1 Transceiver and DS2176 T1 Receive Buffer in an actual system environment. The evaluation board requires +5 volts; board inputs and outputs are TTL-compatible. Test points and control options on the board simplify selection of device feature sets required by the system designer.

Kit assembly requires approximately 1 hour. Although designed for hardware mode operation, a small wire-wrap area is provided for user-supplied host processor interface.

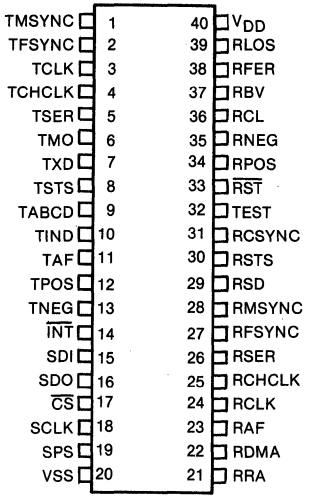
# Dallas Semiconductor
## *CEPT Transceiver*

## *DS2181*

### FEATURES

- Single chip CCITT primary rate transceiver
- Supports new CRC4-based framing standards
- Supports CAS and CCS signaling standards
- Simple serial interface used for device configuration and control in "processor" mode
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Comprehensive on-chip alarm generation, alarm detection and error logging logic
- Shares footprint with DS2180 Bell-T1 Transceiver
- Companion to DS2175 Transmit & Receive Elastic Store
- 5V supply, low power CMOS technology

### PIN CONNECTIONS




### DESCRIPTION

The DS2181 is designed for use in CCITT networks and supports all logical requirements of CCITT Red Book Recommendations G.703, G.704 and G.732.

The transmit side generates framing patterns and CRC4 codes, formats outgoing channel and signaling data, and produces network alarm codes when enabled.

The receive side decodes the incoming data and establishes frame, CAS multiframe, and CRC4 multiframe alignment. Once synchronized, the device extracts channel, signaling, and alarm data.

A serial port allows access to 14 on-chip control and status registers in the processor mode. In this mode, a host processor controls such features as error logging, per-channel code manipulation, and alteration of the receive synchronizer algorithm.

The hardware mode is intended for preliminary system prototyping and/or retrofit into existing systems. This mode requires no host processor and disables special features available in the processor mode.

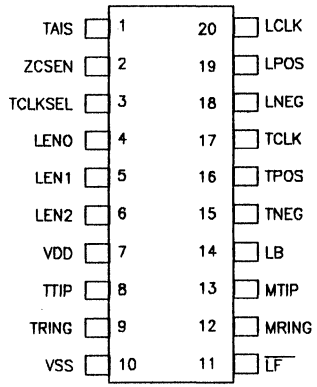
# Dallas Semiconductor
## *Transmit Line Interface*

## *PRELIMINARY*
## *DS2186*

### FEATURES

- Line interface for T1 (1.544Mhz) and CEPT (2.048 Mhz) primary rate networks
- On-chip transmit LBO (line build-out) and line drivers eliminate external components
- Programmable output pulse shape supports short and long loop applications
- Supports bipolar and unipolar input data formats
- Transparent, B8ZS and HDB3 zero suppression modes
- Compatible with the DS2180 T1 and DS2181 CEPT Transceivers
- Companion to the DS2187 Receive Line Interface
- Single 5V supply, low power CMOS technology

### PIN CONNECTIONS




### DESCRIPTION

The DS2186 interfaces user equipment to North American (T1-1.544MHz) and European (CEPT-2.048MHz) primary rate communications networks. The device is compatible with all types of twisted pair and coax cable found in such networks. Key on-chip components include: programmable waveshaping circuitry, line drivers, remote loopback and zero suppression logic. A line coupling transformer is the only external component required. Short loop (DSX-1,0 to 655 feet) and long loop (CSU;0 dB, -7.5 dB and -15 dB) pulse templates found in T1 applications are supported. Appropriate CCITT Red Book recommendations are met in the CEPT mode. Application areas include DACS, CSU, CPE equipment, channel banks and PABX to computer interfaces such as DMI and CPI.

# Dallas Semiconductor
## *Receive Line Interface*

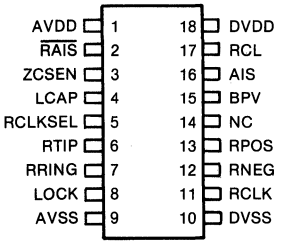
PRELIMINARY

# *DS2187*

### FEATURES

- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- Extracts clock and data from twisted pair or coax
- Meets requirements of PUB 43801, PUB 62411 and applicable CCITT recommendations
- Precision on-chip PLL eliminates external crystal or LC tank—no tuning required
- Decodes AMI, B8ZS and HDB3 coded signals
- Designed for short loop applications such as terminal equipment to DSX-1
- Reports alarm and error events
- Compatible with the DS2180 T1 and DS2181 CEPT Transceivers
- Companion to the DS2186 Transmit Line Interface
- Single 5V supply, low power CMOS technology

### PIN CONNECTIONS




### DESCRIPTION

The DS2187 interfaces user equipment to North American (T1—1.544 MHz) and European (CEPT—2.048 MHz) primary rate communication networks. The device extracts clock and data from twisted pair or coax transmission media and eliminates expensive discrete components and/or manual tuning required in existing T1 and CEPT line termination electronics.

Application areas include DACS, CSU, CPE equipment, channel banks and PABX-to-computer interfaces such as DMI and CPI.

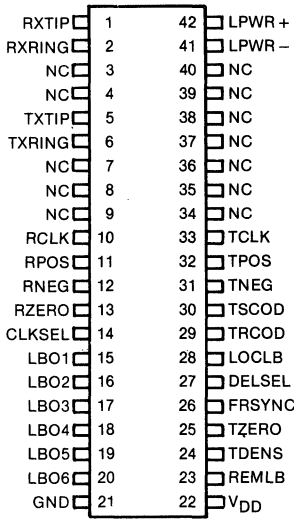
# Dallas Semiconductor
## *T1 Network Interface Unit*

PRELIMINARY
**DS2190**

### FEATURES

- Modularized network interface for connecting to 1.544 Mbps T1 services
- Small size—1.75″ × 2.75″ × 0.5″ high permits integration onto line cards
- Compatible with ATT publication 62411
- FCC Part 68 and Part 15 pre-registration
- Extracts clock and data for use by a transceiver device such as the DS2180
- Loopback code generation and detection
- Assures proper ones density to network
- Powered by a local +5 volt supply

### PIN CONNECTIONS




### DESCRIPTION

The DS2190 is a small sealed module designed to meet the recommendations of ATT publications 62411 for interfacing to T1 1.544 Mbps services (such as Accunet* T1.5, Skynet* T1.5 and High Capacity Digital Service). Because of the DS2190's FCC approval (Parts 68/15) and small footprint, T1 equipment makers can integrate an NIU into their products, reducing cost and increasing total system performance. Basic functions of the DS2190 are clock and data recovery, isolation and surge protection, loopback detection and generation, and keep-alive signal generation. The DS2190 is compatible with D4 and ESF framing formats as well as B8ZS Clear Channel Coding. Also provided are alarm outputs for transmit and receive line status monitoring.

*Service marks of ATT Communications.

# MODEM

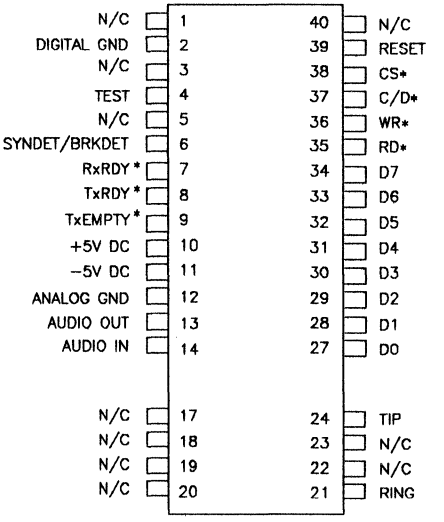
# Dallas Semiconductor
# *MODEM*

# *DS6101/6103*

## FEATURES

- Direct connection to telephone line — incorporates DAA function
- Parallel interface to general purpose uP bus
- Very small size — 2.28" x 1.0" x 0.5"
- Full Bell 212A/103 Modem compatibility
- FCC Part 68 registered DAA
- Call progress Monitoring
- Tone or pulse dialing
- DTMF sensing and decoding
- Voice sensing
- Software controlled audio interface
- Voice synthesis option
- Parallel host interface
- +/- 5 Volt power only
- Telephone line diagnostics
- Synchronous/asynchronous operation
- Line frequency monitoring
- Parity generation/checking
- Sync byte detection/insertion

## PIN CONNECTION




## CAUTION

Pins 17-24 have 1500V isolation from the rest of the modem, this isolation should be preserved throughout the system.

## DESCRIPTION

The DS6101/6103 Modems are high level communication subsystems manufactured in a component sized form factor to enable maximum communications capability in a minimum amount of space. The distinguishing characteristic of these devices is that they allow direct connection to a telephone line from any general purpose microprocessor bus. In contrast to many of the so-called "single-chip modem" IC's, the DS6101/ 6103 Modems provide all of the functions required for a complete, Bell 212A compatible interface. These functions include the host interface, modulation and demodulation circuitry, and Data Access Arrangement (DAA) line interface ciruitry. The Modems' DAA is fully FCC registered, eliminating potential delays for customers with a need to incorporate a modem function in their end system product.

The Modem has an advanced line monitoring capability which allows it to sense the presence of voice or DTMF (touch tone) signals on the line in addition to its normal call progress monitoring. The Modem may then be switched into an Audio mode for voice communication, or into a DTMF decoding mode which makes it possible to receive information from a remote touch tone telephone and decode it for the host processor. The DS6103 includes a voice synthesizer for voice prompting in the return path or for the user.

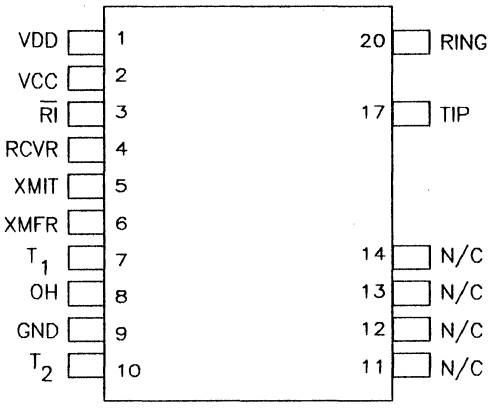
# Dallas Semiconductor
## *Data Access Arrangement*

## *DS6112*

### FEATURES

- Interfaces user equipment to public switched telephone network
- FCC Part 68 Registered
  - Simplifies system design
  - Minimizes equipment approval cycle
- Ideal for modem applications
- Small Size - 1.25" x 1.0" x 0.5"
- 2 to 4 Wire Converter
- 1500 Volt Isolation
- 800 Volt Surge Protection
- Ring Detection

### PIN CONNECTIONS




**CAUTION**
Pins 17 and 20 have 1500V isolation from the rest of the circuitry. This isolation should be preserved throughout the system.

### DESCRIPTION

The DS6112 is a communications component that provides a "direct connect" telephone line interface. It is FCC Part 68 Type WP registered to meet hazardous voltage, surge and leakage current requirements. A system developed with this product as the DAA meets Part 68 Type WP protection requirements and requires no further registration.

This component may be used as the direct connect telephone line interface for virtually any application in which voice or data is to be transmitted over the public switched telephone network.

The DS6112 includes both ring detection circuitry and the 2 to 4 wire converter hybrid for use in modem applications. It operates from +/-5 volt power supplies and occupies 1.25 square inches of board space.

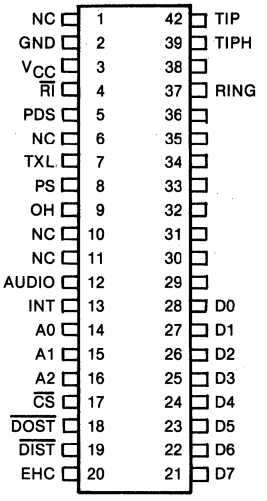
# Dallas Semiconductor
# *1200 BPS MODEM Module*

PRODUCT REVIEW
**DS6122**

## FEATURES

- Complete modem system interfaces parallel *u*P bus directly to phone line
- Bell 212A/103 and V.22/21 compatible
- Complete "AT" command set in firmware
- Contains FCC Part 68 and Canadian CS-03 approved DAA
- Small size—2.28″ × 1.0″ × 0.5″
- Single +5 Volt supply operation
- DTMF and pulse dialing
- Call progress monitoring

## PIN CONNECTIONS




## DESCRIPTION

The DS6122 is a high-level communications subsystem manufactured in a small form factor to permit integration into a variety of applications, especially where space is a concern. An integral FCC and Canadian approved DAA interface allows the DS6122 to be directly connected to the public switched telephone network. Embedded firmware in this component completely implements the standard "AT" command set which assures compatibility with popular communications software. The DS6122 also emulates the 8250B UART which means that it can be directly connected to an IBM-PC/XT/AT system bus. Operation at +5 volts makes this module an attractive choice for low-power applications such as lap-top computers.

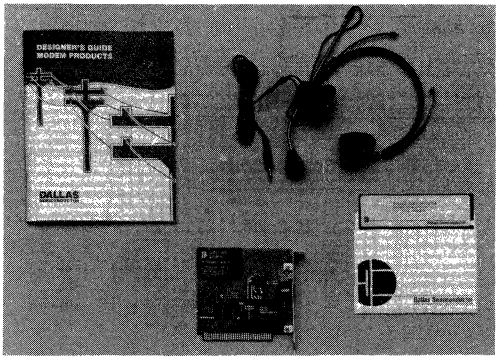
Included in the DS6122 are all the modulation/demodulation and filtering circuitry necessary for compatibility with Bell 212A/103 type modems as well as the CCITT V.22/21 series modems. Also provided is the capability for call progress monitoring as well as DTMF and pulse dialing. 3 loopback modes—analog, digital and remote—are available for line and component testing. A programmable audio output can be used for monitoring the telephone line signals.

# Dallas Semiconductor
## *MODEM Evaluation Kit*

**DS6151**
**DS6153**

### FEATURES

- IBM PC-based evaluation kit for DS6101/61103 Modems
- Two versions:
  - DS6151 supplied with DS6101 Modem
  - DS6153 supplied with DS6103 Voice Synthesis Modem
- Printed circuit board provides socket for Modem, RJ11 telephone jack and headset jack; plugs into expansion slot on IBM PC
- Supplied with headset
- Evaluation software on floppy disk
- Supplied with complete operating instructions




### DESCRIPTION

The DS6151 and DS6153 Modem Evaluation Kits provide immediate evaluation of the DS6101 and DS6103 Modems. The kits supply all of the necessary hardware, software and documentation for use with an IBM PC. A printed circuit card which sockets the appropriate Modem plugs directly into the backplane of the PC and provides a modular RJ11 connector to a telephone line. In addition, a jack for the headset which is supplied with the kit is mounted on the board. A complete set of documentation with instalation and operating instructions is also supplied. A user need only have a private telephone line with a modular plug to insert into the RJ11 jack and he or she can be using the modem to converse in voice, transmit data or listen to synthesized voice responses in just a few minutes.

# Application Notes

# Dallas Semiconductor Nonvolatile Static RAM

*Application Note-1*

## NONVOLATILE STATIC RAM

Vast resources have been expended by the semiconductor industry trying to build a nonvolatile Random Access Read/Write Memory. The effort has been undertaken because nonvolatile RAM offers several advantages over other memory devices—DRAM, Static RAM, Shadow RAM, $E^2$PROM, EPROM and ROM—which were developed to meet specific applications needs.

Characteristics of the ideal nonvolatile RAM are: low power consumption; higher performance; greater reliability; higher density; and the ability to be used in any semiconductor memory application.

While the various memory components designed to date are not appropriate for the ideal memory scenario, each excels in meeting one or more of the sought after attributes (Figure 1).

Figure 1 **MEMORY ATTRIBUTES**

| | COST | INTERFACE EASE | NON-VOLATILE | DENSITY | PERFOR-MANCE | READ/ WRITE | DATA RE-TENTION |
|---|---|---|---|---|---|---|---|
| DRAM | + + | | | + + | + | + + | |
| STATIC RAM | + | + + + | | + | + + + | + + + | |
| SHADOW RAM | | | + | | + | + | + |
| $E^2$PROM | | | + | | | | + |
| EPROM | + + | + + + | + + | + + | | | + + |
| ROM | + + + | + + + | + + + | + + + | + | | + + + |

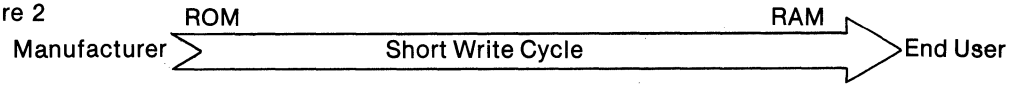
+ = Degree of Excellence

**Many types of memories have been devised to meet varying application needs. Nonvolatile Read/Write Random Access Memories can be substituted for all memory types independent of applications.**

For example, NMOS DRAM memory provides performance and density, but, on the down side, must be constantly refreshed to retain data. At the opposite extreme are ROMs, offering nonvolatility and density, but lacking the ability to be updated with new data because information is burned in only once. Between these two are a wide range of devices that fulfill some characteristics of the ideal memory.

Two popular devices, $E^2$PROMs and Shadow RAMs, are designed to emulate a static RAM but also have the ability to retain data after a power loss. But despite their capability to retain data, both $E^2$PROMs and Shadow RAMs fall short of meeting the industry's needs for several reasons (Figure 2).

Figure 2




**Long Write Cycles prevent $E^2$PROMs from emulating RAM, making them less than ideal memories.**

Most notably, the $E^2$PROM requires a special write cycle. The $E^2$PROM's inability to support standard write cycle hinders performance in applications where memory is updated immediately as new data is available.

Another problem with $E^2$PROMs is their wear out mechanisms. These raise reliability concerns due to the limited number of write cycles allowed—sometimes as few as 10,000. If a static RAM with a 200 ns cycle time had this limitation, it would wear out in a mere 20 ms. An application that requires constant updating, such as the buffer memory of a cashier's checkout terminal or a printer, the $E^2$PROM's wear out mechanism is not acceptable.

Shadow RAMs, on the other hand, have been developed to overcome long write cycles and avoid wear out, but still require special store and recall operations and to date are at densities of less than 4K bits. In addition, the majority of available Shadow RAM devices do not provide a write protection mechanism to prevent losing data when the system experiences out-of-tolerance conditions due to a power loss.

Finally, because of the complexity of programming circuits, the cell structure and the special process technology required, the density of both $E^2$PROMs and Shadow RAM have not kept up with industry demands.

In systems requiring store-and-forward data, the nonvolatile RAM must provide the desired fast write cycle as well as protection of memory in the event of a power loss. Despite the promise of such a memory device and the effort invested by the industry, the ideal nonvolatile RAM is just now becoming available.

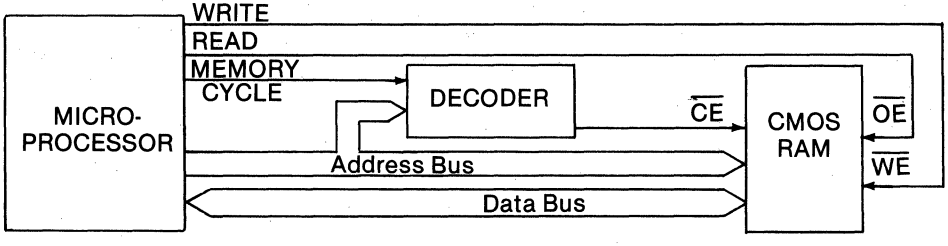
To provide the ideal nonvolatile RAM, Dallas Semiconductor has combined two technologies—intelligent CMOS control circuitry and lithium energy—to offer the first available high-density nonvolatile memory.

Two devices, the DS1220 (2K × 8 bits) and the DS1225 (8K × 8 bits), use this combination and a CMOS static RAM to provide a nonvolatile Random Access Memory solution at a density of 64K bits. These memory devices are the most appropriate answer to date because of the beneficial qualities of CMOS static RAM.

CMOS static RAMs currently available have read and write cycle times of 100 ns, which exceed most system requirements. This alleviates the problem of the $E^2$PROM, because there are no wear-out mechanism or write cycle limitations.

Static RAMs are also the easiest to use and interface because the pin-out configurations are standard throughout the industry. In fact, X8 or bytewide static RAMs can be interfaced directly to microprocessors (Figure 3). In addition, CMOS static RAMs offer low power in both active and standby modes, a characteristic sought by many designers. In most designs, RAMs remain in standby much of the time, keeping power consumption negligible. In the standby mode, current drain consists only of leakage currents in the tens of nanoamperes. The density of static RAM is presently at an impressive 8K × 8 or 64K bits and is doubling every two years.

Figure 3




**Bytewide memories provide easy interface to microprocessors because of the X8 organization and control signal definition.**

## PUTTING LITHIUM AND RAM TOGETHER

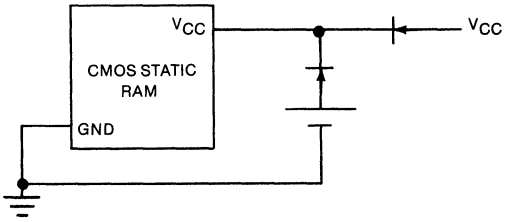
The minute leakage current of CMOS RAMs can be sustained with a backup energy source to yield a most attractive nonvolatile memory. However, the actual solution to the ideal nonvolatile memory involves more than just a CMOS memory and back up energy source (see Figure 4).

Battery Backup design schemes are many and varied. The increase in density and availability of low powered CMOS memories in recent years has made this approach even more attractive. Yet problems still exist with battery backup design due to battery packaging and a lack of the appropriate standard components to implement the support circuitry. One problem is providing isolation between the battery and power supply (see Figure 5). Diodes can provide isolation but produce a voltage drop which requires nonstandard power supplies and also subtracts from the battery voltage. A second problem is the circuitry required to detect power failure and write protect the memory. This additional circuitry must be powered from the battery. Unless these devices draw an extremely modest amount of current, battery selection changes drastically. In fact a current drain of even a couple of microamperes dictates the use of either rechargeable batteries or a replaceable battery scheme. If rechargeable batteries are selected, the recharging circuit can be costly and complex and the best rechargeable battery cannot compare with the electrochemical stability of the lithium primary cell. Even worse, replaceable batteries add maintenance and cost to an in-service system. Battery packaging has also been a serious limitation taking up valuable space and requiring special handling considerations to prevent discharge.

## ENERGY SOURCE

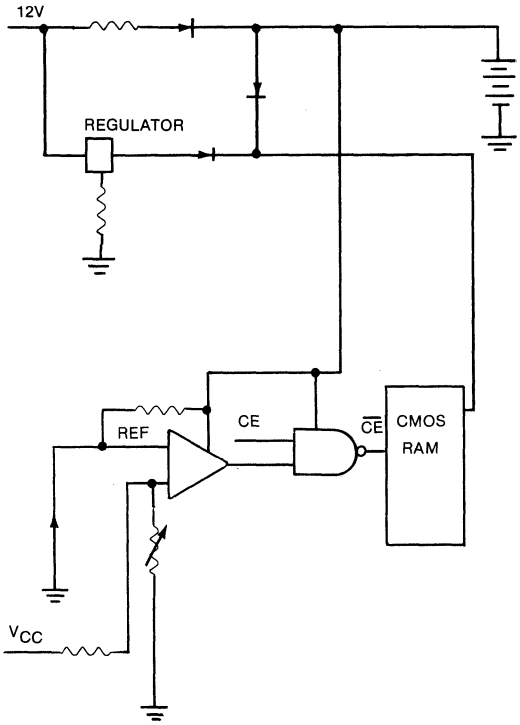
The energy source used to retain data in the ideal memory must be capable of outlasting the usefulness of the end product. The products use the extremely stable electrochemical system lithium polycarbon monofluoride with over 35 mA hours of energy reserve and

**BATTERY BACKUP CIRCUIT?** Figure 4




**CMOS static RAM requires more than just a backup power supply. Data must also be protected during power transients to avoid garbled data.**

Figure 5




**Support circuitry required to produce power fail detection and write protection forces the need for a multicell rechargeable battery or a replacement lithium battery.**

guaranteed shelf life greater than 10 years. The total energy cell load current used by the DS1220 and DS1225 is less than 100 nA at 25 degrees C. This gives a calculated lifetime of more than 40 years in the absence of externally applied power.

## LITHIUM BATTERY BACK UP IS MORE RELIABLE

The lithium energy cell has raised concern about reliability and has been the object of much study[1]. Data taken on the energy cell used in the DS1220 and DS1225 indicates a failure rate less than 0.5% per three million device hours at 70 degrees C.

Additional life studies taken on the same lithium energy source encapsulated in the manufacture of the DS1220 and DS1225 have produced no failures in over 12 million device hours at 70 degrees C. The lithium energy cell, then, is ideal for commercial and industrial semiconductor applications.

## RETROFITTING EXISTING DESIGNS

The pinout of the DS1220 and DS1225 is an established industry standard (Figure 6). The Joint Electronic Devices Engineering Council's Bytewide Version B Standard defines and upgrades from 2K × 8 in density to 32K × 8.

This standard accommodates RAM, ROM, UV EPROMs, and $E^2$PROMs. Because of the flexibility and upgradeability of bytewide memories, the number of existing sockets is in the hundreds of millions. Therefore, many system designs can accommodate direct replacement of RAMs, EPROMs, ROMs, and $E^2$PROMs with the DS1220 and DS1225. These new solutions add real time programmability and/or density upgrades to existing system without redesign. Real time programmability gives the system the ability to be personalized by the end user. In other words, the nonvolatile RAMs can be retrofitted into existing design without change to existing hardware. This retrofitting offers a cost-effective, practical solution for companies who have invested in other memory devices that are less than ideal for their needs. For example, a design using conventional static RAM can be upgraded to nonvolatile memory by substituting a DS1220 or DS1225 for the RAM memory.

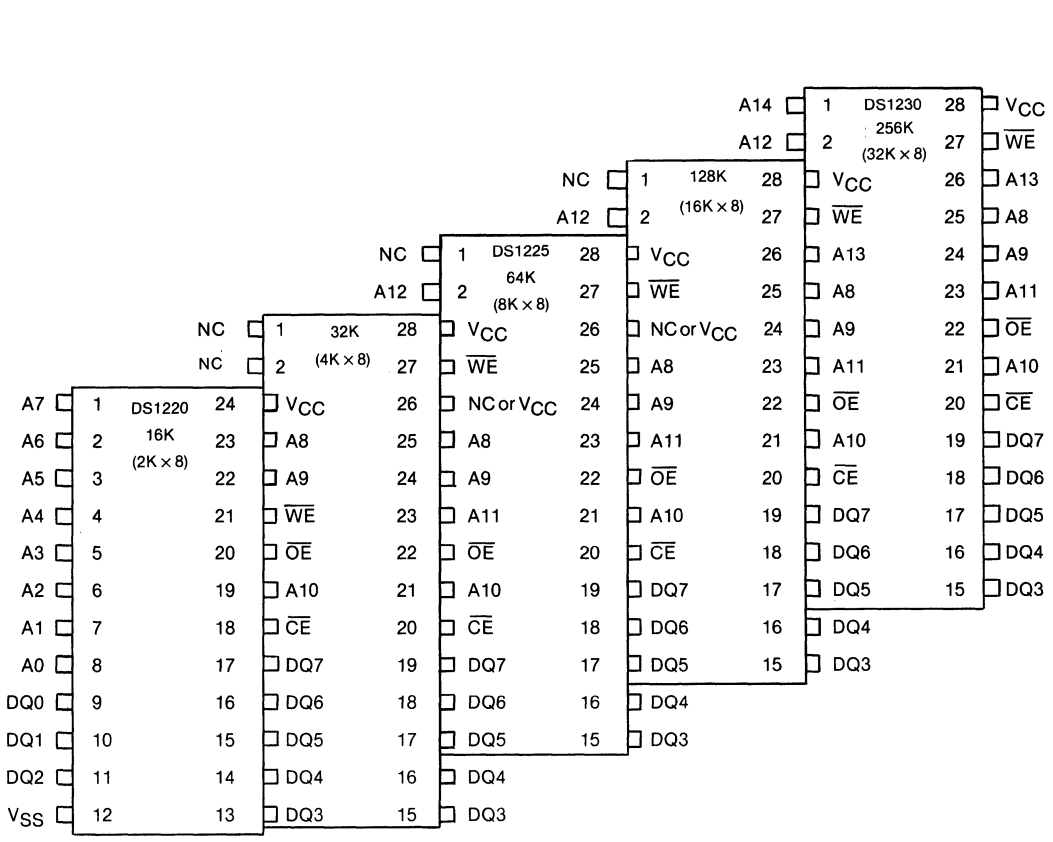
## IN-CIRCUIT PROGRAMMABILITY

The advantages of nonvolatile RAM can be related to the capability of software. Modern systems seek customization for the cost of standard product. In this aspect, software can be adapted in this system to perform specialized functions. It is even possible to totally modify a system personality over the telephone. In-circuit programming also reduces maintenance cost by eliminating service calls to update software. Software stored in RAM can be updated as often as necessary, depending on the configuration or application of the system.

In the immediate future, the density of a nonvolatile CMOS static RAM will continue to increase. By 1986, a 32K × 8 version of the nonvolatile RAM will be available from Dallas Semiconductor. In addition, Dallas Semiconductor will offer a watch function and security options in combination with nonvolatile RAM. Still other devices will be introduced using special packaging techniques to add portability to nonvolatile memories. These packages will offer designers and end users the ability to give their systems unique solution characteristics for value added configurations.

[1]Louis J. Hart and Theodore Ciobanu, "Lithium Batteries for Memory Backup—An Evaluation Program at IBM," published in *Batteries Today*, Summer 1984 issue.

Figure 6 **Bytewide JEDEC Pinout**




Provides for density upgrade to 32K × 8

# Dallas Semiconductor
# User Insertable Nonvolatile RAM

*Application Note-2*

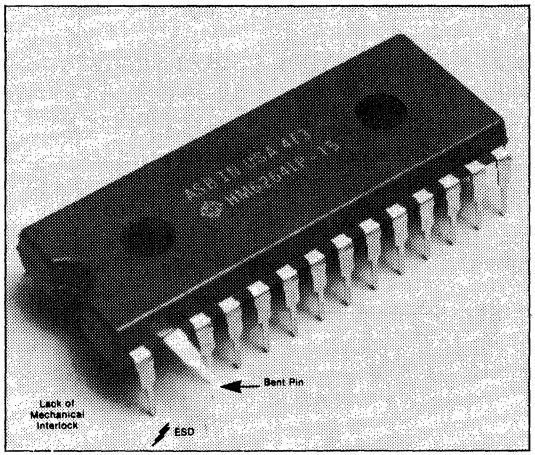
## USER INSERTABLE NONVOLATILE RAM

Semiconductor packaging has precluded the handling of memory by the end users (Figure 1). There are many examples of equipment manufacturers ranging from consumer video game cartridges to speech recognition for industrial automation who have repackaged semiconductor memory to permit handling by the end customer. The underlying reason is to increase the flexibility of a mass produced piece of equipment. Game manufacturers found out that by producing one standard size video console they could meet the diverse interests of their customers with cartridges sold in the after market. More often than not the value of a piece of equipment is tied to how closely it can be adapted to serve a specific need (Figure 2). This is in conflict with the economics of mass production. When a design has no options, it would tend to be lower in cost but offer marginal application fit. Unlike mechanical, electronic equipment has an inherent advantage in adapting to diverse needs largely as a result of the microprocessor and its associated memory. In particular, the cost of creating uniqueness has been drastically lower with the availability of nonvolatile RAM. When nonvolatile RAM is packaged in a user-insertable format, even more possibilities are opened up (Figure 3).

Dallas Semiconductor produces user insertable nonvolatile RAM as an off-the-shelf component ranging from a 1000 bit DS1201 Electronic Tag to a 4 million bit cartridge (Table 1). Careful attention has been given during the design of these products to make them connect directly to microprocessor systems (Figure 4). Being solid state, these devices are rugged and suitable for harsh environments.

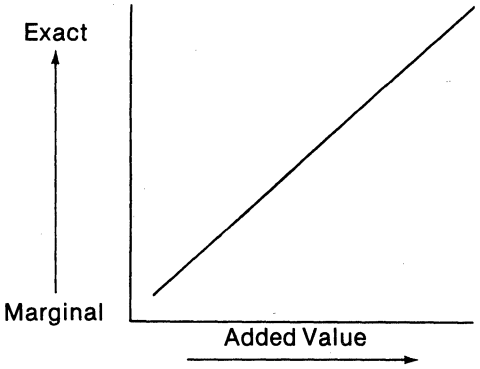
## USER INSERTION PROBLEMS WITH CONVENTIONAL INTEGRATED CIRCUITS

Figure 1




## APPLICATION FIT

Figure 2




## BENEFIT OF NONVOLATILE RAM

Figure 3

- Procedure learning
- Adaptive control
- Automatic firmware updates
- Real time data capture

## ADDED BENEFITS OF USER INSERTABLE MEMORY

- Improved application fit
- Eliminate costly service
- Simplified optioning
- Permits system to evolve
- After market sales

## THE NONVOLATILE READ/WRITE CARTRIDGE

The DS1217 nonvolatile cartridge is a compact, rugged, and portable memory presently available in densities of 2K x 8, 8K x 8, 16K x 8, 24K x 8, 32K x 8 64Kx8, and 128K x 8 (Figure 5).

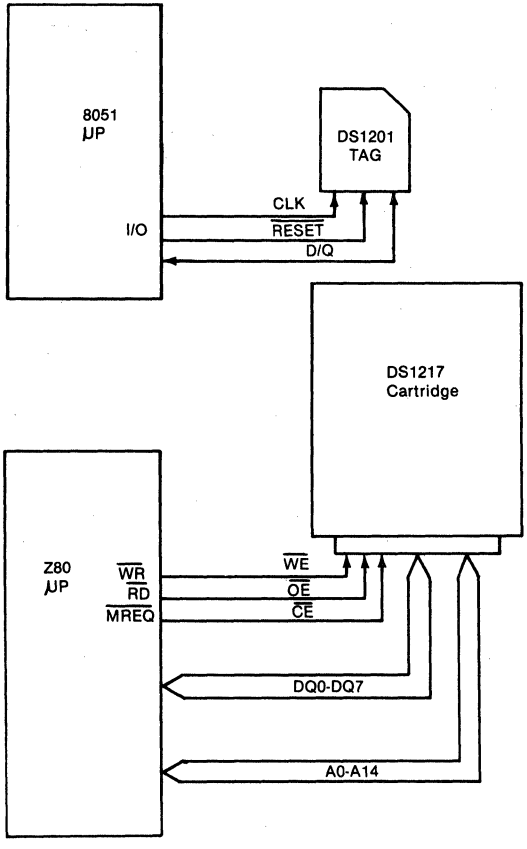
Density is expected to increase to 4M bit, 512K x 8 before 1987. All of the future high density cartridges will have the same package dimensions and connector pinout so that upgrades can be easily accomplished. Data is accessed randomly, one byte at a time via a 15 bit address bus and an 8 bit data bus. Data can be written or read from the cartridge in the same manner as regular static RAM with a read/write cycle time of 250 ns. Because the cartridge is nonvolatile, data is retained when the cartridge is removed from a system. Data retention is handled transparently inside the cartridge via an intelligent controller chip which safeguards data and directs an internal lithium energy source to memories when power is lost. Data is protected from inadvertent loss by preventing memory cycles when the external supply voltage is less than 4.5 volts. Data retention is accomplished by selecting the greater of two voltages, i.e., either the external supply ($V_{CC}$) or the internal lithium energy source. A switch is also provided on the cartridge which unconditionally protects data. When the write protection switch is turned on, the cartridge becomes read only and all write cycles to RAM are ignored.

The lithium energy source used is the extremely stable electrochemical system lithium polycarbon monofluoride. This energy system has the capacity and shelf life needed to retain data for well over ten years in the absence of external power. The lithium energy source has raised concern about reliability and has been the subject of much study[1]. Data taken on the energy source used in the DS1217 indicates a failure rate less than 0.5% per three million device hours at 25°C.

The edge connector on the cartridge has been arranged to meet the JEDEC Standard Bytewide 28-Pin Dip Socket; making it compatible with existing designs. The cartridge can be plugged into a 28-pin socket via a ribbon cable with a 30-position edge connector on one end and a 28-pin plug on the other (Figure 6). This ribbon cable can be purchased directly from AMP or from Dallas Semiconductor (DS9000). The AMP Part Number is 494940-1. The ribbon cable can be used to retrofit existing systems which use the bytewide socket adding nonvolatility, portability, and density upgrade.

## DIRECT CONNECTION

Figure 4



**USER INSERTABLE MEMORY** Table 1
TAGS

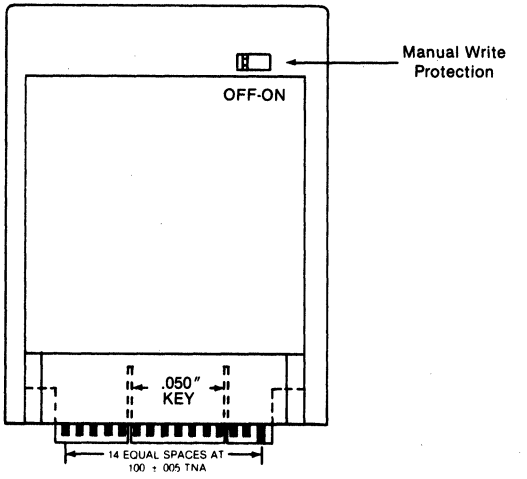
| Part Number | **DS1201** | **DS1205** |
|---|---|---|
| Density (Bits) | 1024 | 4096 |
| Interface | Serial | Serial |
| Data Retention | 10 Years | 10 Years |
| Availability | Now | Future |
| Connection | 5 Pin SIP | 5 Pin SIP |

**CARTRIDGES**

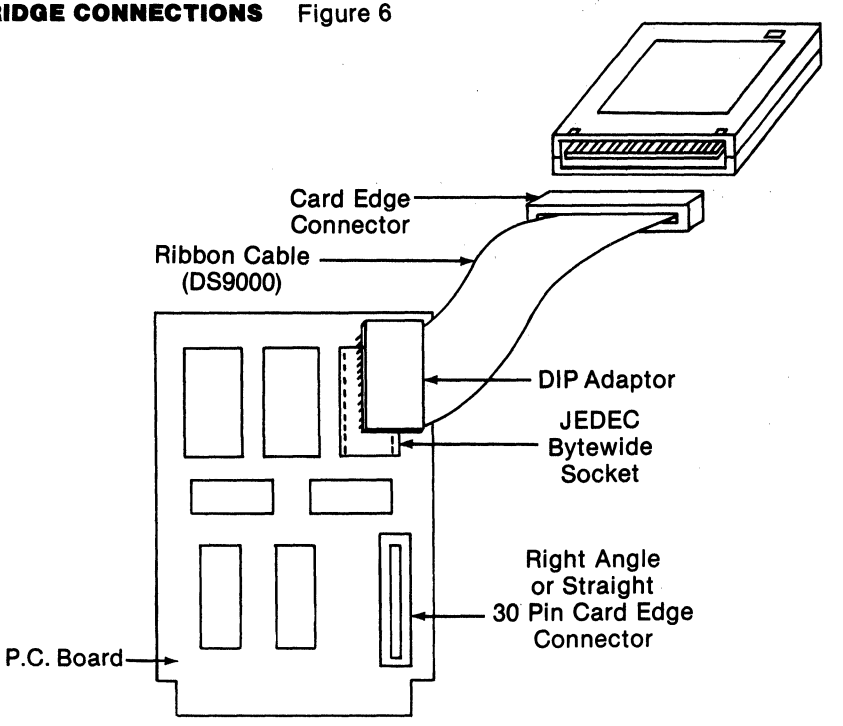
| Part Number | **DS1217/ 16K** | **DS1217/ 64K** | **DS1217/ 128K** | **DS1217/ 196K** |
|---|---|---|---|---|
| Density (Bits) | 16K | 64K | 128K | 196K |
| Interface | Bytewide | Bytewide | Bytewide | Bytewide |
| Data Retention | 10 Years | 10 Years | 10 Years | 10 Years |
| Availability | Now | Now | Now | Now |
| Connection | 30 Pos. Card Edge | 30 Pos. Card Edge | 30 Pos. Card Edge | 30 Pos. Card Edge |

| Part Number | **DS1217/ 256K** | **DS1217/ ½M** | **DS1217/ 1M** | **DS1217/ 4M** |
|---|---|---|---|---|
| Density (Bits) | 256K | 512K | 1M | 4M |
| Interface | Bytewide | Bytewide | Bytewide | Bytewide |
| Data Retention | 10 Years | 10 Years | 10 Years | 10 Years |
| Availability | Now | Now | Now | Now |
| Connection | 30 Pos. Card Edge | 30 Pos. Card Edge | 30 Pos. Card Edge | 30 Pos. Card Edge |

**NONVOLATILE READ/WRITE CARTRIDGE — DS1217** Figure 5




**CARTRIDGE CONNECTIONS** Figure 6



Every precaution has been taken with the design of the cartridge to protect data integrity while handling. The case is made of durable impact resistant plastic capable of sustaining a three foot drop test on a concrete surface. The casing is designed to protect the internal electronics from dust, shock, and other elements of an adverse environment. The cartridge will operate over a wide temperature range of 0°C to +70° C and permit storage with data retention from −40° C to +70° C. Relative humidity can vary between 0 and 95% provided there is no condensation. The mating connector is plated with 50 u inches of gold over 150 u inches of nickel. When the proper mating receptacle (AMP Part Number 494940-1) is used, over 3000 insertions and withdraw cycles can occur without electrical degradation. All signal lines are recessed and the ground connection is extended on the mating connector to prevent electrostatic damage to internal components. The recessed signal paths and extended ground have the added advantage of enhancing data integrity when the cartridge is inserted and withdrawn while power is applied because the possibility of charge injection into the memory is eliminated. To further prevent garbled data while "hot plugging" the cartridge, two offset keys are provided. When both keys are used in the mating receptacle, data integrity is virtually assured.

## OPERATION

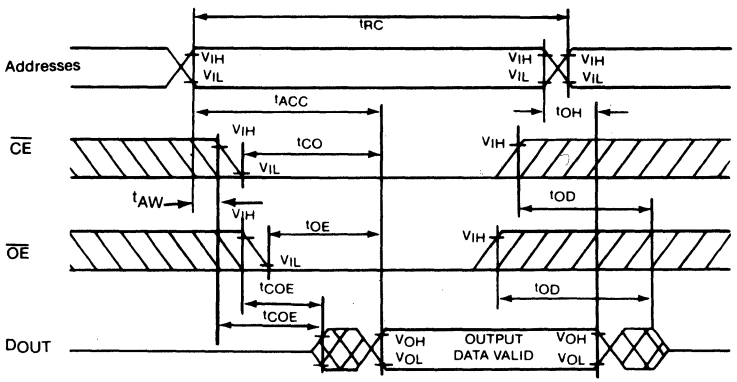
### READ MODE

The DS1217 is executing a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low) (Figure 7). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight date I/O pins within $t_{ACC}$ (access time) after the last address input signal is stable, providing that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satified. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the latter occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access. Read cycles can only occur when $V_{CC}$ is greater than or equal to 4.5 volts. When $V_{CC}$ is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

### WRITE MODE

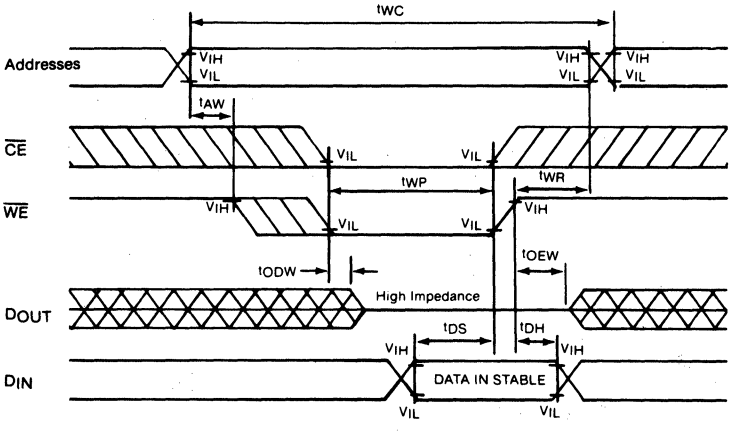
The DS1217 is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable (Figure 8). The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the

**READ CYCLE** Figure 7



write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{OWD}$ from its falling edge. Write cycles can only occur when $V_{CC}$ is greater than 4.5 volts. When $V_{CC}$ is less than 4.5 volts, the memory is write protected.

**WRITE CYCLE** Figure 8




## DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for $V_{CC}$ greater than 4.5 volts and guarantees write protection for $V_{CC}$ less than 4.5 volts (Figure 9). Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The DS1217 constantly monitors $V_{CC}$. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As $V_{CC}$ falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM. To retain data during power up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects the external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 4.5 volts.

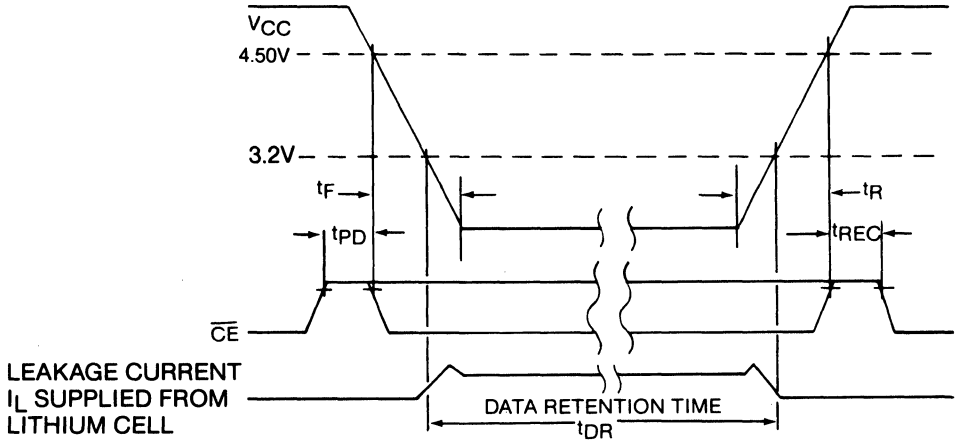
The DS1217 checks battery status to warn of potential data loss. Each time that $V_{CC}$ power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge provides battery redundancy. The DS1217 provides an internal isolation switch which provides for the connection of two batteries. During battery back-up time the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

## OPTIONAL SECURITY FEATURE

Cartridges can be used to add features to a system and as such are often sold as value added extras. In these applications protection of software and guarding sensitive data is often important in avoiding competition. To date the problem of maintaining after market sales has been solved by special

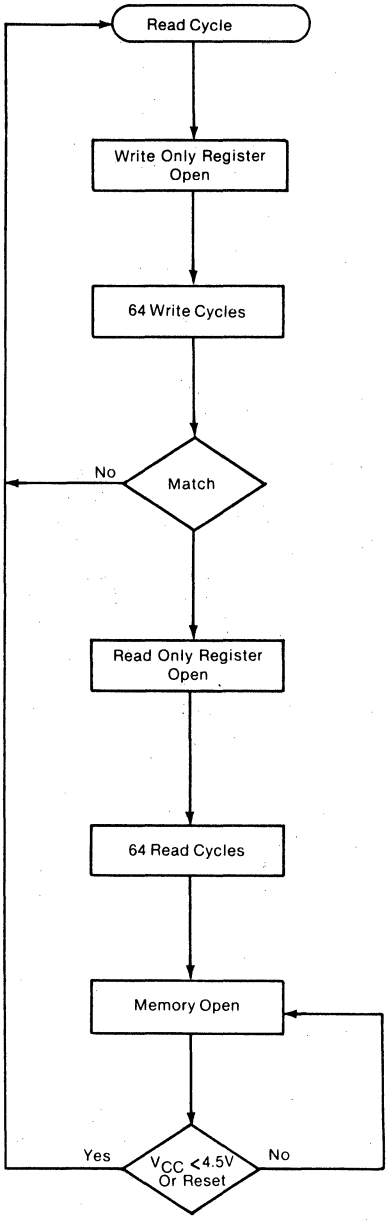
**POWER-DOWN/POWER-UP CONDITION** Figure 9




molded cases and connectors which are unique to each equipment manufacturer. These barriers are relatively easy to overcome by competitors. In contrast, Dallas Semiconductor provides standardized cases and connectors but employs laser technology to make silicon unique. This presents a far more formidable barrier to potential after market competitors and also reduces cost. Dallas Semiconductor cartridges have added security circuitry which makes it usable for only one manufacturer's specific application while maintaining the same form factor and connector system. When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the cartridge (Figure 10). A 64 bit access code must be consecutively written to the cartridge. Actual RAM locations are not written as the security option is intercepting the data rate until access is granted. Following the 64 write cycles a comparison is made to a 64 bit pattern uniquely defined by the user and programmed into the DS1217 by Dallas Semiconductor at the time of manufacture. This pattern can only be interrogated by an intelligent controller within the cartridge and cannot be read by the user. When a correct match is found, the next part of the security sequence begins by reading a 64 bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1217 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user defined read only register is available. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register may be used by software to determine if the cartridge will be permitted to be used with that particular system. After the 64 read cycles the cartridge is unlocked and all subsequent memory cycles will become actual memory accesses based on address inputs. This procedure prevents second party encroachment.

The security feature can also be used for bank switching in and out multiple cartridge in the same memory address space. Entrance to the desired cartridge would take place exactly as described above. Since each cartridge can have a different security code, only the one with the exact pattern match would allow access. To change from one cartridge to another, the reset line must be driven low long enough to exit from the active cartridge. A different cartridge could then be entered by matching the security code.

**SECURITY SEQUENCE** Figure 10




## THE ELECTRONIC TAG

The DS1201 is a miniature nonvolatile read/write memory system. The Tag is organized as a 128 x 8 memory. However, data is accessed in a serial manner to reduce pin count, and to simplify interface requirements while enhancing the reliability of connection. In fact, the Tag can be carried in your pocket, dropped in the water, and even stepped on, and still retain data. Low pin count combined with a special mechanical form factor has been used to make the device compact, rugged, and user insertable.

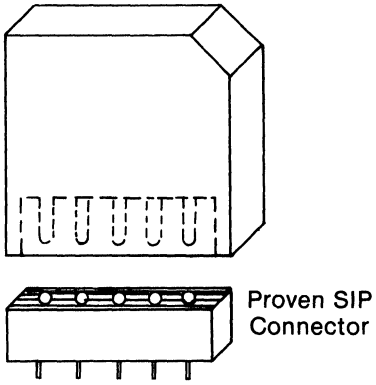
The Tag is permanently powered by a lithium polycarbon monofluoride energy cell which retains data in the absence of power. This energy cell is the same type as that used in the cartridge differing only in size and energy capacity. When connected in a system, power can be supplied via the reset signal or the $V_{CC}$ pin. Reset current of only 2 mA supplies all the energy needed by the Tag. Reset is also used to initialize and terminate all communications with the Tag.

The Tag is designed to be plugged into a standard 5 pin 0.1 inch center SIP receptacle (Figure 11). A key is provided to prevent the Tag from being plugged in backward (Figure 12). Contact to the Tag can be determined to insure connection integrity before data transfer begins. Clock, $\overline{\text{RESET}}$, and data INPUT/OUTPUT all have 25K Ohm pull down resistor to ground which can be sensed by a reading device. While the Tag is designed to be a user insertable device it is not limited to those applications. The Tag can be used inside a system using the same 5 pin SIP strip and become a permanent 1K nonvolatile memory.

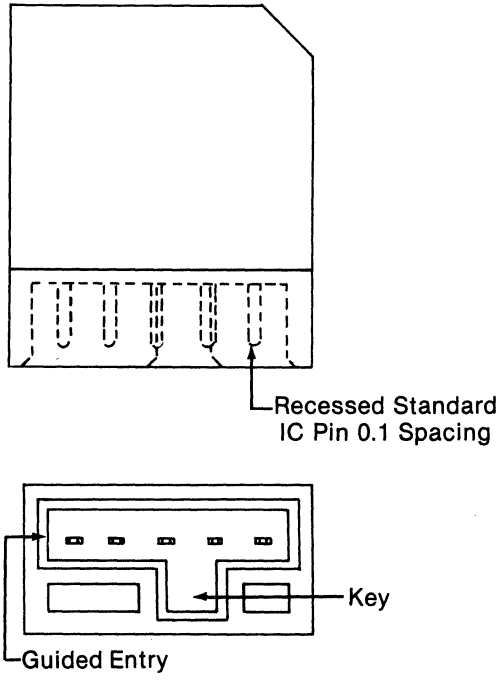
## OPERATION

The block diagram (Figure 13) of the Electronic Tag illustrates the main elements of the device: namely, shift register, control logic, nonvolatile RAM, and power switch. To initiate a memory cycle $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the shift register providing both address and command information. Each bit is serial input on the rising

**TAG CONNECTIONS** Figure 11




**TAG** Figure 12



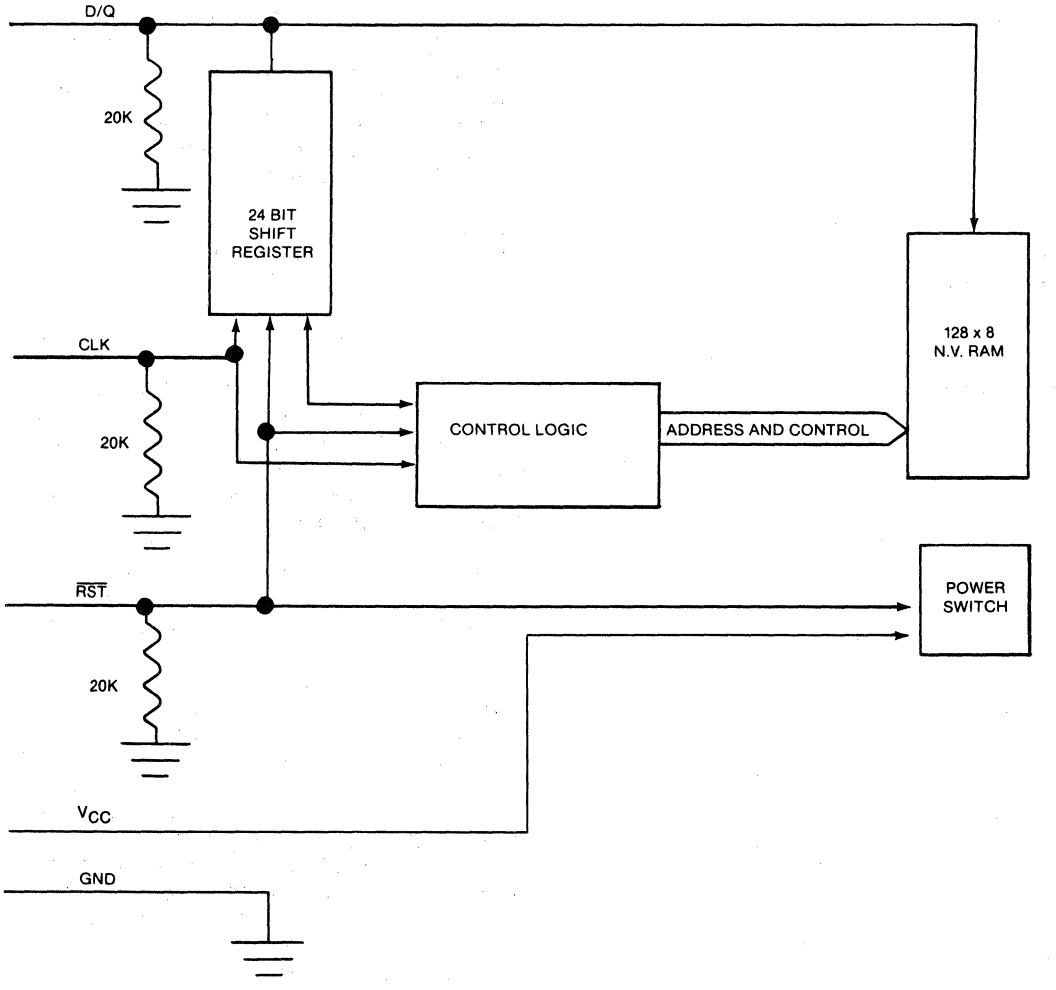

edge of the CLOCK input. Seven address bits specify one of 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 CLOCKS which load the shift register additional CLOCKS will output data for a read, or input data for a write. The number of CLOCK pulses equals 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

**APPLICATIONS**

The portable computer is an example of many applications which can take advantage of user insertable nonvolatile memory. The portable computer approaches the power and capability of a desk top personal computer with the notable exception of mass data storage. The most popular type of mass data storage is the floppy disk. Floppy disks are dense and miniature, but suffer from two drawbacks. First, floppy disks are fragile, making their use prohibitive in many applications. Second, the mechanism to read and write the media is expensive and consumes power. Since portable computers are battery powered, use of floppy disk drive is prohibitive. To compensate, portable computer manufacturers developed software cartridges which are used in place of disk drives. For the most part, cartridges used with portable computers are read only and contain program information. This limitation prevents movement of user data beyond the portable computer. A better approach is the use of a nonvolatile read/write cartridge which could provide both program storage and data storage. The nonvolatile read/write cartridge also avoids problems of different disk sizes and formats.

Both the Tag and the cartridge are well suited for a range of applications. For example, a Tag could be used as a production traveler containing information such as lot number, inspector's identification, and quality control steps. An application in the pharmaceutical industry uses the Tag to keep track of chemical concentrations in liquids. The variables are stored in the Tag and used to precisely control formulation when mixtures are produced. The machine tool indus-

**ELECTRONIC TAG BLOCK DIAGRAM** Figure 13




try could use the cartridge to quickly set up operations instead of involved manual entry procedures. The rugged and durable cartridge package is also ideal for the industrial automation environment. The cartridge can store programs for process control in a factory. Because of the ease in which data can be changed, process parameters could be altered and tracked automatically.

[1]Louis J. Hart and Theodore Ciobanu, "Lithium Batteries for Memory Backup—An Evaluation Program at IBM," published in *Batteries Today*, Summer 1984 issue.

# Dallas Semiconductor SmartSocket—SmartWatch

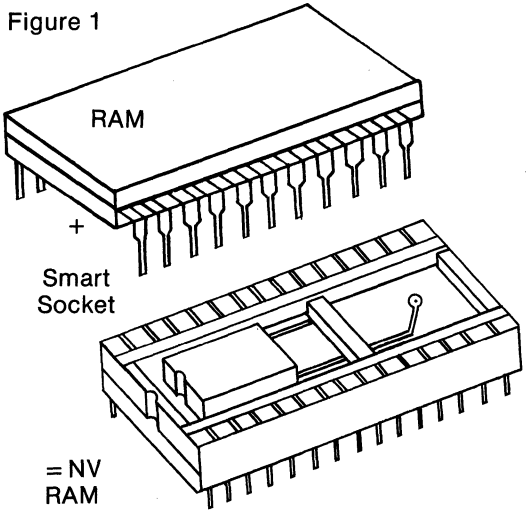
*Application Note-3*

## SMARTSOCKET-SMARTWATCH

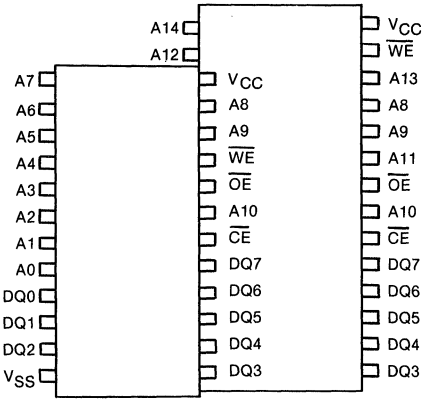
The production rate of CMOS static RAM has become staggering. Millions of units are used each year in systems that require the ideal characteristics and low cost attributed to CMOS static RAM. Now its one drawback, volatility, can be overcome by mating a standard CMOS static RAM with a DS1213 SmartSocket (Figure 1). Contained in the SmartSocket is intelligent control circuitry and a back-up lithium energy source to permanently power the mated RAM, thereby providing data retention in the absence of power. In this way the same high volume production efficiency which has made static RAM so economical can be used to make a nonvolatile RAM. Furthermore the SmartSocket accepts either 2K × 8 8K × 8 or 32K × 8 devices making system design extremely flexible.

The SmartSocket conforms to the JEDEC Bytewide standard for dual in line memory (Figure 2). The identical footprint allows existing sockets to be replaced with SmartSockets thus giving a system the advantage of nonvolatile RAM without redesign. Its physical size is the same as conventional sockets except for an additional height of 0.2 inches needed for mechanical considerations.

Figure 1



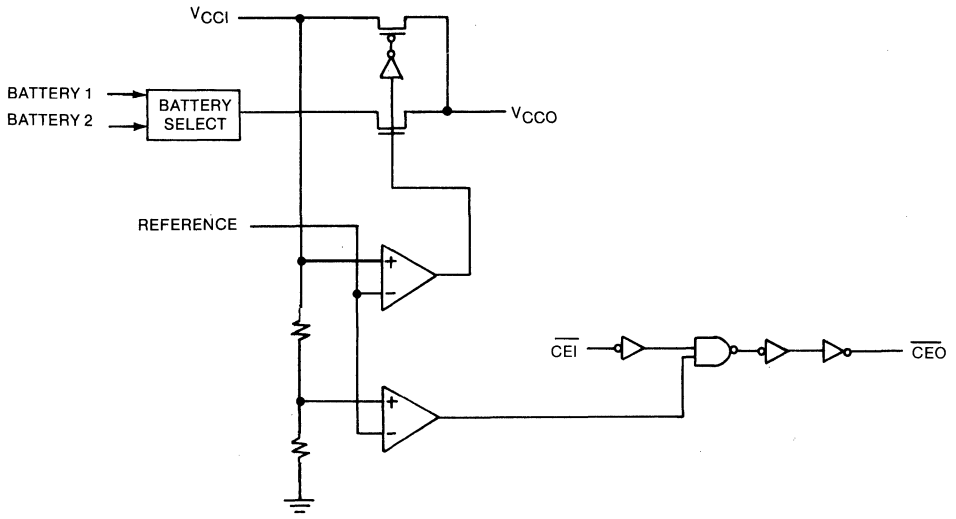

**BYTEWIDE JEDEC PINOUT** Figure 2




## SMARTSOCKET OPERATION

The heart of the DS1213 SmartSocket is the intelligent control circuit designed by Dallas Semiconductor to perform five circuit functions required to battery back-up a CMOS memory (Figure 3). First, a switch is provided to direct power from the battery or $V_{CC}$ supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartSocket provides is power fail detection. Power fail detection occurs between 4.75 and 4.5 volts. The DS1213 constantly monitors the $V_{CC}$ supply. When $V_{CC}$ falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable (Figure 4). The third function accomplishes write protection by holding the chip enable signal to the memory to within 0.2 volts of $V_{CC}$ or battery supply. If the chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal will be passed through to the

**SIMPLIFIED BLOCK DIAGRAM OF THE DS1213 CONTROLLER CHIP** Figure 3



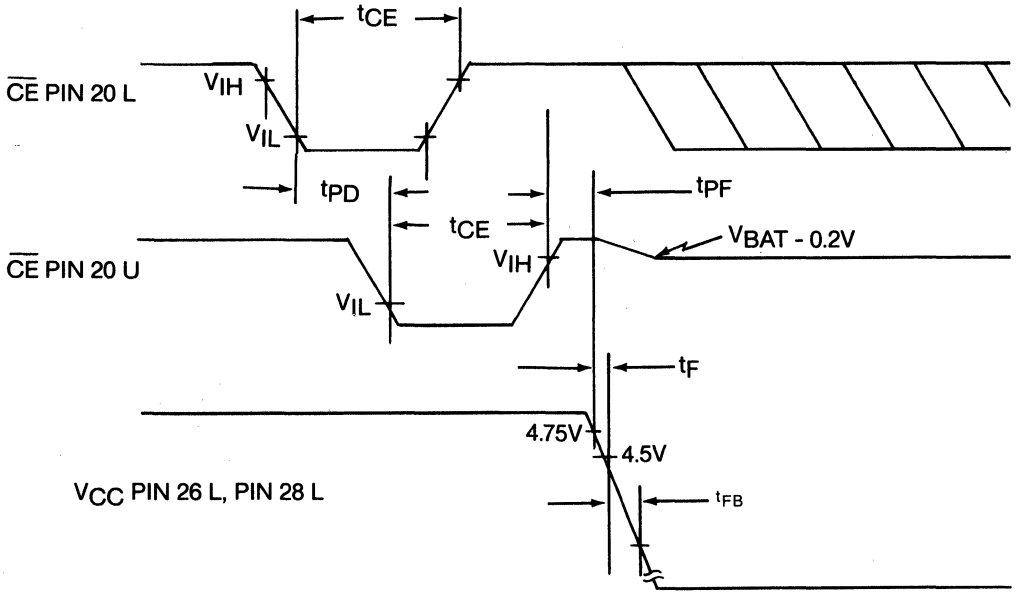

socket receptacle with a maximum propagation delay of 20 ns. The fourth function the DS1213 performs is to check battery status to warn of potential data loss. Each time that $V_{CC}$ power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location,altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function which the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to insure reliability. The DS1213 SmartSocket provides an internal isolation switch which provides for the connection of two batteries. During battery back up time the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

## ENERGY SOURCE

The energy source within the SmartSocket is an extremely stable electrochemical system made up of a lithium anode and polycarbon monofluoride cathode. This energy system has the capacity and shelf life needed to retain data for well over 10 years in the absence of external power when mated with an appropriate CMOS static RAM (Table 1).

The lithium energy source has raised concern about reliability and has been the object of much study[1]. Data taken on the energy source used in the SmartSocket indicates a failure rate less than 0.5% per three million device hours at 70°C.

**TIMING DIAGRAM — POWER DOWN** Figure 4




**TIMING DIAGRAM — POWER UP**

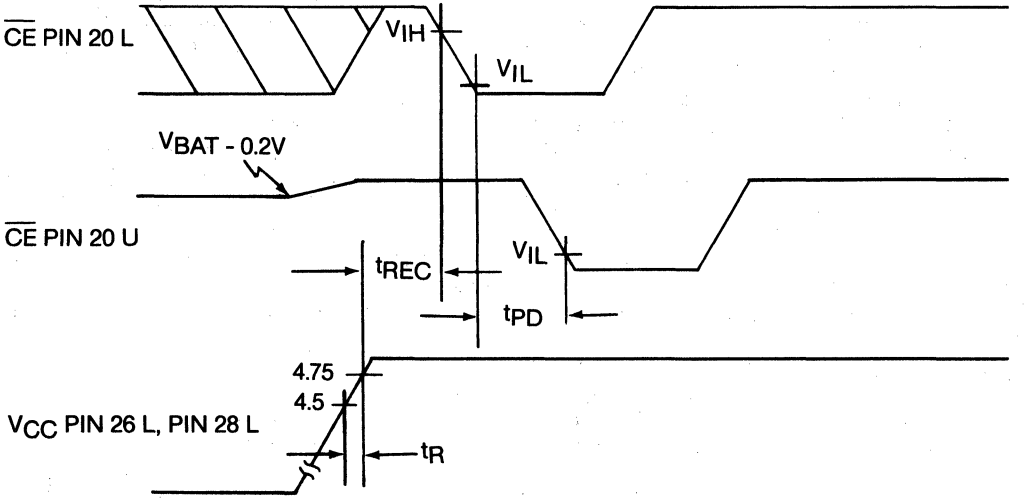


Table I

- Acceptable RAM Choices*

| | 2K × 8 | 8K × 8 | 32K × 8 |
|---|---|---|---|
| Toshiba | TC5517 | TC5564 | |
| NEC | uPD446 | uPD4464 | |
| OKI | MSM5128 | | |
| Fujitsu | MB8416 | | |
| Sharp | | LH5164 | |
| Sony | | | CXK58255P |

*10 Years Data Retention in the Absence of Power

**ADDING A TIME FUNCTION**

A similar second device called the DS1216 SmartWatch retains the nonvolatile RAM capability of the SmartSocket and adds a calendar time function. The SmartWatch maintains time information including hundredths of seconds, seconds, minutes, hours, day, date, month and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. Hours of the day can be tracked in both the 12 and 24 hour format.

The value of adding a clock function to the SmartSocket lies in the amortization of the energy source with additional space saving benefits. The DS1216 SmartWatch includes the quartz crystal and circuits needed for time keeping within the same package as the SmartSocket while remaining compatible with the JEDEC Bytewide memory pinout.

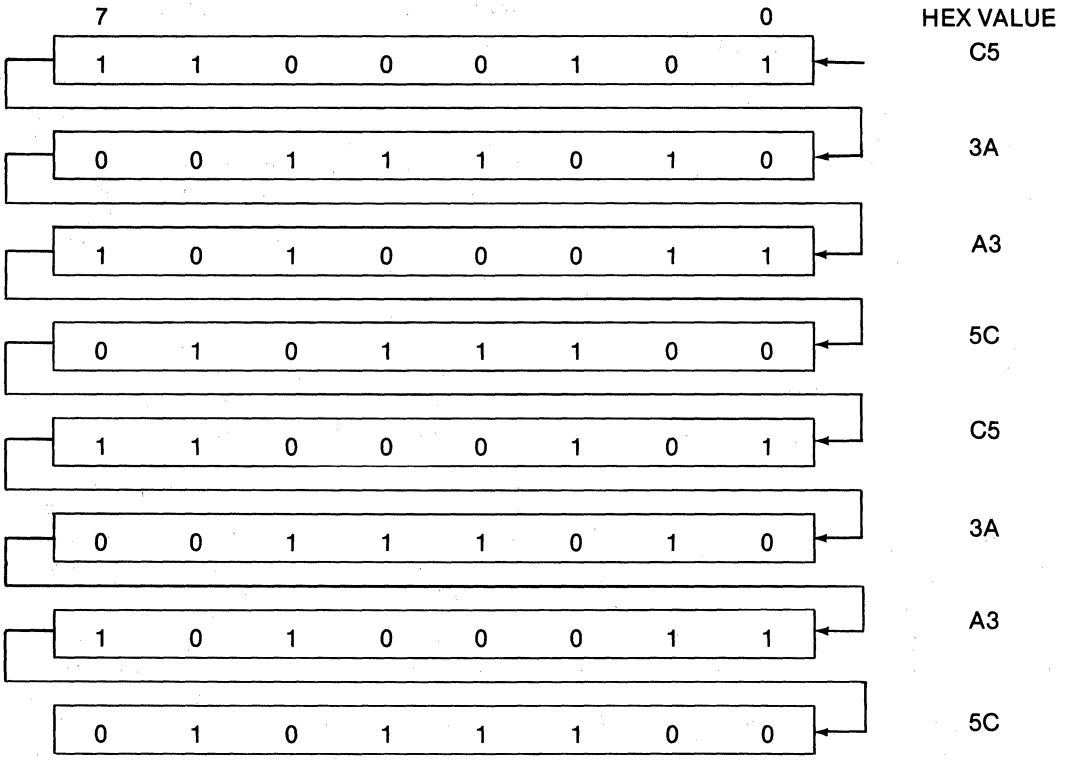
**OPERATION**

Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64 bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch; memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CE}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch, therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 1 of the 64 bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 5). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

**SMARTWATCH COMPARISON REGISTER DEFINITION** Figure 5




NOTE: The pattern recognition in hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in $10^{19}$.

**SMARTWATCH REGISTER INFORMATION**

The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64 bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 6.

Data contained in the SmartWatch registers are in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

**AM-PM/12/24 MODE**

Bit 7 of the hours register is defined as the 12 or 24 hour mode select bit. When high, the 12 hour mode is selected. In the 12 hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24 hour mode, bit 5 is the second 10 hour bit (20-23 hours).

### OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the reset and oscillator function. Bit 4 controls the reset (pin 1). When the reset bit is set to logical 1, the reset input pin is ignored. When the reset bit is set to logical 0, a low input on the reset pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from Dallas Semiconductor set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

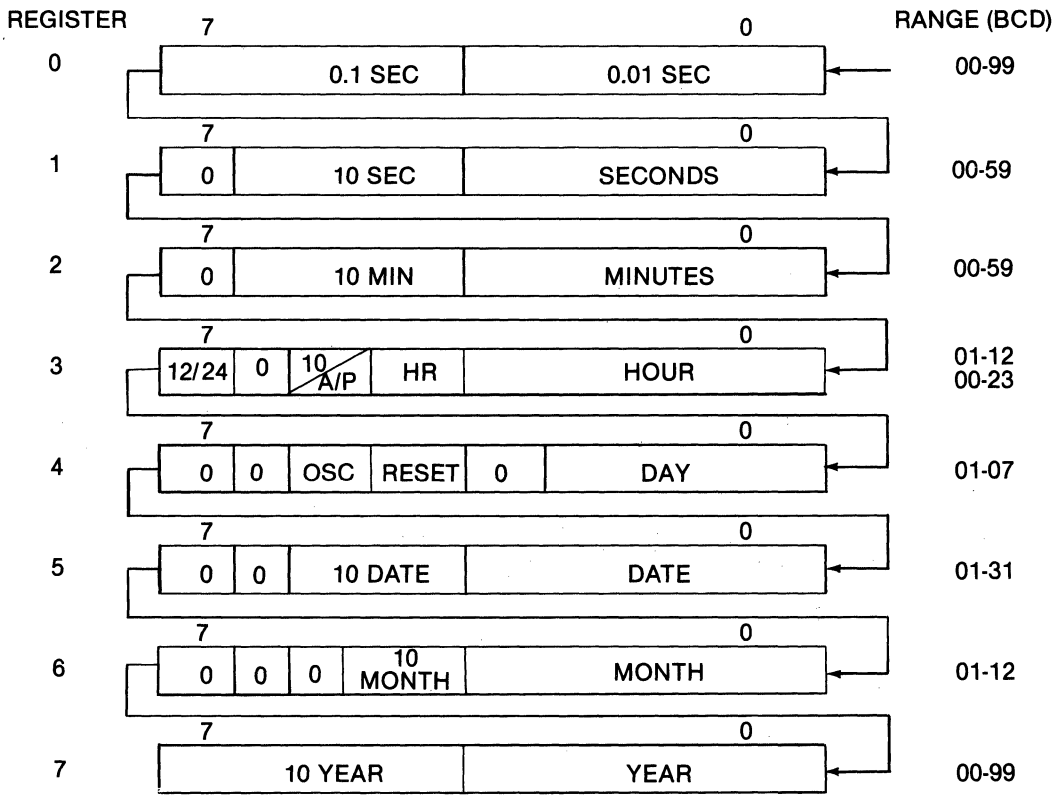
### ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

### HARDWARE RETROFIT

The method by which the time function of the SmartWatch is accessed allows for retrofitting existing designs which use a 28 pin bytewide socket. The hardware design is left intact, and only a software change is required to add a calendar feature to previously designed systems. Moreover, most sys-

**SMARTWATCH REGISTER DEFINITION** Figure 6

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tems only require time information on power up since time is kept track of by the operating system while power is applied. In these applications, the software overhead is reduced to an algorithm which is executed only when the machine is turned on.

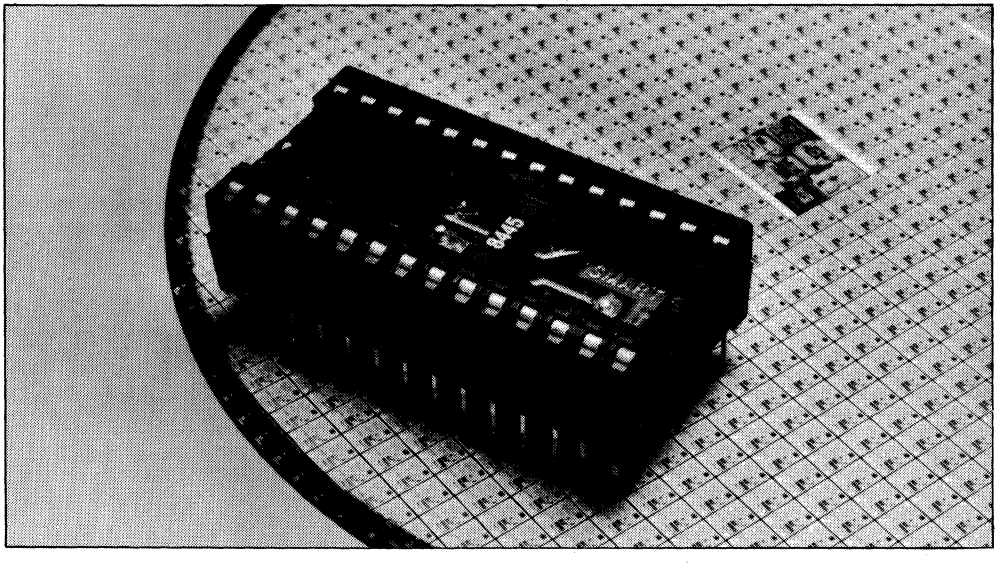
## SOFTWARE

The software needed to cause entry and update for the SmartWatch consists of three subroutines (Table 2). The first, called "PATTREC," will wake up the SmartWatch and get it ready for reading and writing. After pattern recognition has been established one of two subroutines is used to either extract information or update the SmartWatch. The "WRWATCH" routine will write the 8 watch registers of the SmartWatch. The "RDWATCH" will extract information from the SmartWatch. The example shown in Table 2 is written in 8086 assembly language.

The SmartSocket replaces as many as a dozen discrete components needed to implement battery backup for a static RAM (Figure 7). Furthermore, the special control circuit techniques employed in the SmartSocket do not have the drawbacks of the earlier discrete component approach saving printed circuit board area and reducing current consumption from the battery. Manufacturing procedures are simplified by not having to deal with special handling procedures needed to avoid discharging the battery. Reliability is also greatly improved by eliminating battery clips. The SmartWatch goes further by adding a time function without increasing space requirements. Often an entire printed circuit board is used to provide this function.

[1]Louis J. Hart and Theodore Ciobanu, "Lithium Batteries for Memory Backup—An Evaluation Program at IBM," published in *Batteries Today*, Summer 1984 issue.

**SMARTSOCKET** Figure 7



**SMARTWATCH SOFTWARE** Table 2

```
;
;               SET SSSS TO THE SEGMENT OF MEMORY WHERE
;               THE SMARTWATCH WILL BE ACCESSED
;
SWATCH          SEGMENT AT SSSS
;
;               SET OOOO TO THE OFFSET OF THE SCRATCH MEMORY
;               BYTE USED TO COMMUNICATE WITH THE SMARTWATCH
;
SCRATCH         EQU     OOOO
;
SWATCH          ENDS
;
CSEG            SEGMENT PARA PUBLIC 'CODE'
                ASSUME  CS:CSEG,DS:CSEG
;
PAT             DB      0C5H,03AH,0A3H,05CH,0C5H,03AH,0A3H,05CH
;
DTA             DB      0,0,0,0,0,0,0,0
;
PATREC          PROC    NEAR
                PUSH    ES                      ;SAVE ES
                MOV     AX,SEG SWATCH           ;SET ES TO
                MOV     ES,AX                   ; SEGMENT OF SCRATCH
                MOV     CX,64                   ;DO 64 BITS
                MOV     SI,OFFSET PAT           ;SET INDEX TO PATTERN RECOGNITION
                MOV     DI,OFFSET SCRATCH
PR1:            TEST    CX,7                    ;LOAD NEXT BYTE?
                JNZ     PR2                     ;NO!
                LODSB                           ;GET NEXT PATTERN BYTE
PR2:            MOV     ES:[DI],AL              ;WRITE D0
                SHR     AL,1                    ;PREPARE NEXT DATA BIT
                LOOP    PR1                     ;LOOP BACK
                POP     ES                      ;RESTORE ES
                RET                             ;RETURN
PATREC          ENDP
;
WRWATCH         PROC    NEAR
                PUSH    ES                      ;SAVE ES
                MOV     AX,SEG SWATCH           ;SET ES TO
                MOV       ES,AX       ; SEGMENT OF SCRATCH
                MOV       CX,64       ;DO 64 BITS
                MOV     SI,OFFSET DTA           ;SET INDEX TO DATA
                MOV     DI,OFFSET SCRATCH
WW1:            TEST    CX,7                    ;GET NEXT BYTE?
                JNZ     WW2                     ;NO!
                LODSB                           ;GET DATA BYTE
WW2:            MOV     ES:[DI],AL              ;WRITE D0
                SHR     AL,1                    ;PREPARE NEXT DATA BIT
                LOOP    WW1                     ;LOOP BACK
                POP     ES                      ;RESTORE ES
                RET                             ;RETURN
WRWATCH         ENDP
```

```
;
RDWATCH   PROC    NEAR
          PUSH    DS                  ;SAVE DS
          MOV     AX,SEG SWATCH       ;SET DS TO
          MOV     DS,AX               ; SEGMENT OF SCRATCH
          MOV     CX,64               ;DO 64 BITS
          MOV     SI,OFFSET SCRATCH
          MOV     DI,OFFSET DTA       ;SET INDEX TO DATA
RW1:      JCXZ    RW2                 ;DONE?
          MOV     AH,[SI]             ;READ D0
          SHR     AX,1                ;PREPARE NEXT DATA BIT
          DEC     CX                  ;UPDATE COUNTER
          TEST    CX,7                ;SAVE NEXT BYTE?
          JNZ     RW1                 ;NO!
          STOSB                       ;SAVE DATA BYTE
          JMP     RW1
RW2:      POP     DS                  ;RESTORE DS
          RET                         ;RETURN
RDWATCH   ENDP
;
CSEG      ENDS
          END
```

# Dallas Semiconductor
## *Smart Socket/ Smart Watch Options*

## *Application Note-4 DS1213 DS1216*

### SMARTSOCKET/SMARTWATCH OPTIONS

The DS1213 SmartSocket and DS1216 SmartWatch product families are designed to accept several user modifications. Please review the DS1213 and DS1216 data sheets for normal operation before modification.

### DS1213 SMARTSOCKET OPTIONS
(Reference Figure 1)

**Option 1:** Power Supply Tolerance
The standard DS1213 socket products are manufactured such that power fail detection occurs between 4.75 volts and 4.50 volts, giving a 5% supply operating range. This range can be changed to a 10% supply with power fail detection occuring between 4.50 volts and 4.25 volts. Follow the procedure below:

*cut metal trace labeled "TOL"
*short together metal tabs labeled "T"

**Option 2:** Density Upgrade
This option applies to the DS1213 and DS1213D SmartSockets only. The DS1213 can be upgraded from 8K x 8 to 32K x 8 memory and the DS1213D can be upgraded from 128K x 8 to 512K x 8 memory by performing the following:

*cut metal traces identified by a hash mark labeled "'U"
*short together square metal pads labeled "G"

### DS1216 SMARTWATCH OPTIONS
(Reference Figure 2)

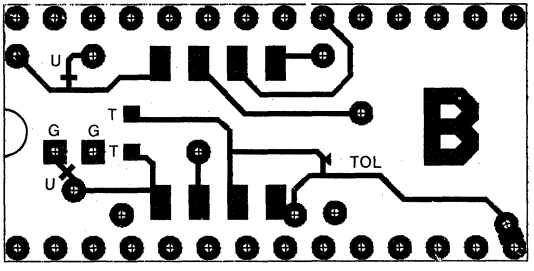
**Option 1:** RESET Disconnect
All DS1216 SmartWatch sockets are manufactured such that the RST signal to the Real Time Clock is located at pin 1 of the socket. If for a given application the RESET signal is not required, or not desired, this signal can be permanantly disconnected as follows:

*cut metal trace labeled "RES"

**Option 2:** Density Upgrade
This option applies to the DS1216 and DS1216D SmartWatch sockets only. As with the DS1213 and DS1213D, the DS1216 and DS1216D can be upgraded from 8K x 8 to 32K x 8 memory and 128K x 8 to 512K x 8 respectively as follows:

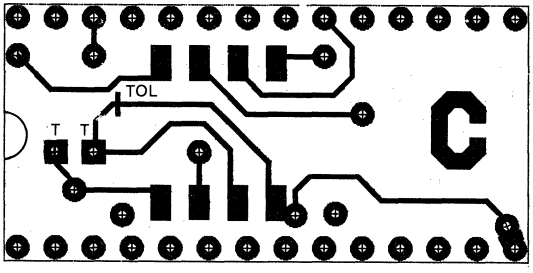
*cut metal traces identified by a hash mark labeled "U"
*short together square metal pads labeled "G"

Figure 1: **DS1213 SMART SOCKET FAMILY**



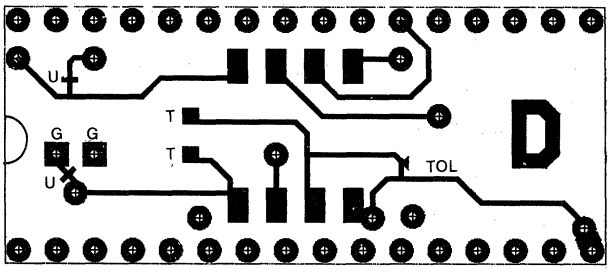

Pin 1

DS1213




Pin 1

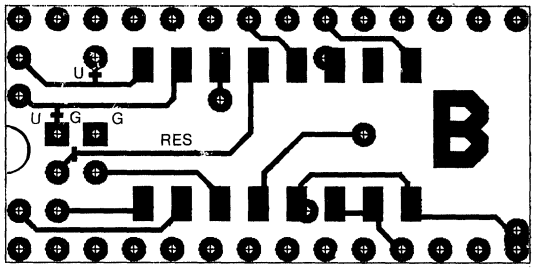
DS1213C




Pin 1

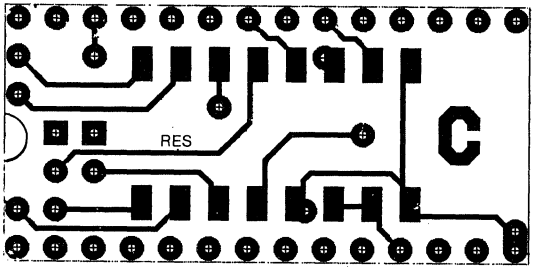
DS1213D

Figure 2: **DS1216 SMART WATCH FAMILY**



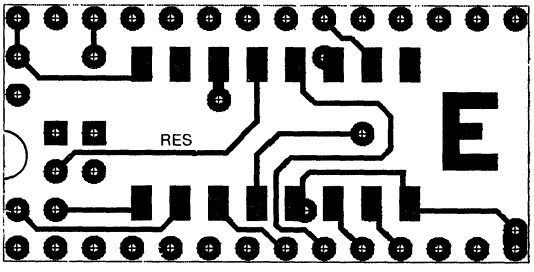

Pin 1

DS1216



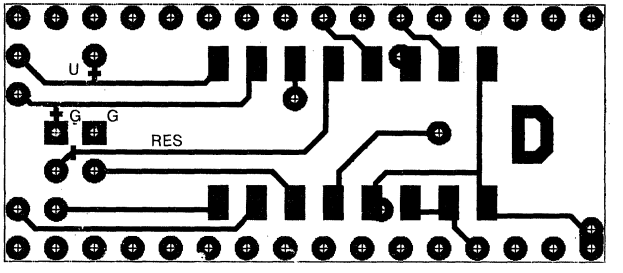

Pin 1

DS1216C



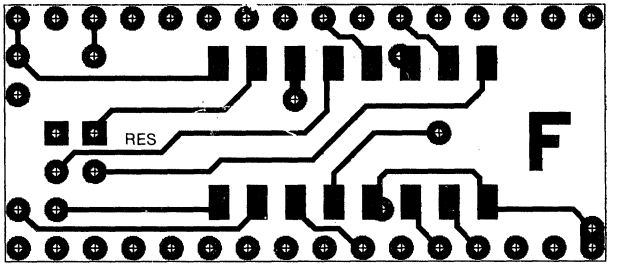

Pin 1

DS1216E




Pin 1

DS1216D




Pin 1

DS1216F

# Dallas Semiconductor
# Integrated Battery Backup

*Application Note-5*

## INTEGRATED BATTERY BACKUP

A CMOS chip set protects critical information in microprocessor-based systems during power loss. Called Integrated Battery Backup, the product provides for the orderly shutdown and automatic restart of processor-based systems. It is, in essence, a micro-level uninterruptable power supply. Particularly useful in industrial automation applications, Integrated Battery Backup allows a system to restart a task where it stopped as if power disruption had not occurred. By saving the data, the system picks up where it left off, thus avoiding wasted efforts and the inconvenience of re-booting.

Integrated Battery Backup is a modular chip set that can be used in its entirety or as individual components according to need. The DS1231 Power Monitor warns a processor of an impending power failure before it happens, providing time for critical data to be stored in nonvolatile memory before system power is lost. The Nonvolatile Controller/Decoder (DS1210, DS1211, DS1212, DS1221) safeguards against RAM data loss during power up and down transients. It automatically switches to battery when power failure occurs and consumes a minute battery current of less than 100 nA. The DS1260 SmartBattery supplies uninterruptable power in the absence of $V_{CC}$ to maintain data in nonvolatile memory for more than 10 years. A supplemental function of software controlled write inhibit can be provided by the DS1234 or DS1222. The DS1215 TimeChip adds the capability of time stamping and dating events.

System designers can use these low-cost chips to protect critical system data and avert the chaos that accompanies unforeseeable power failures.

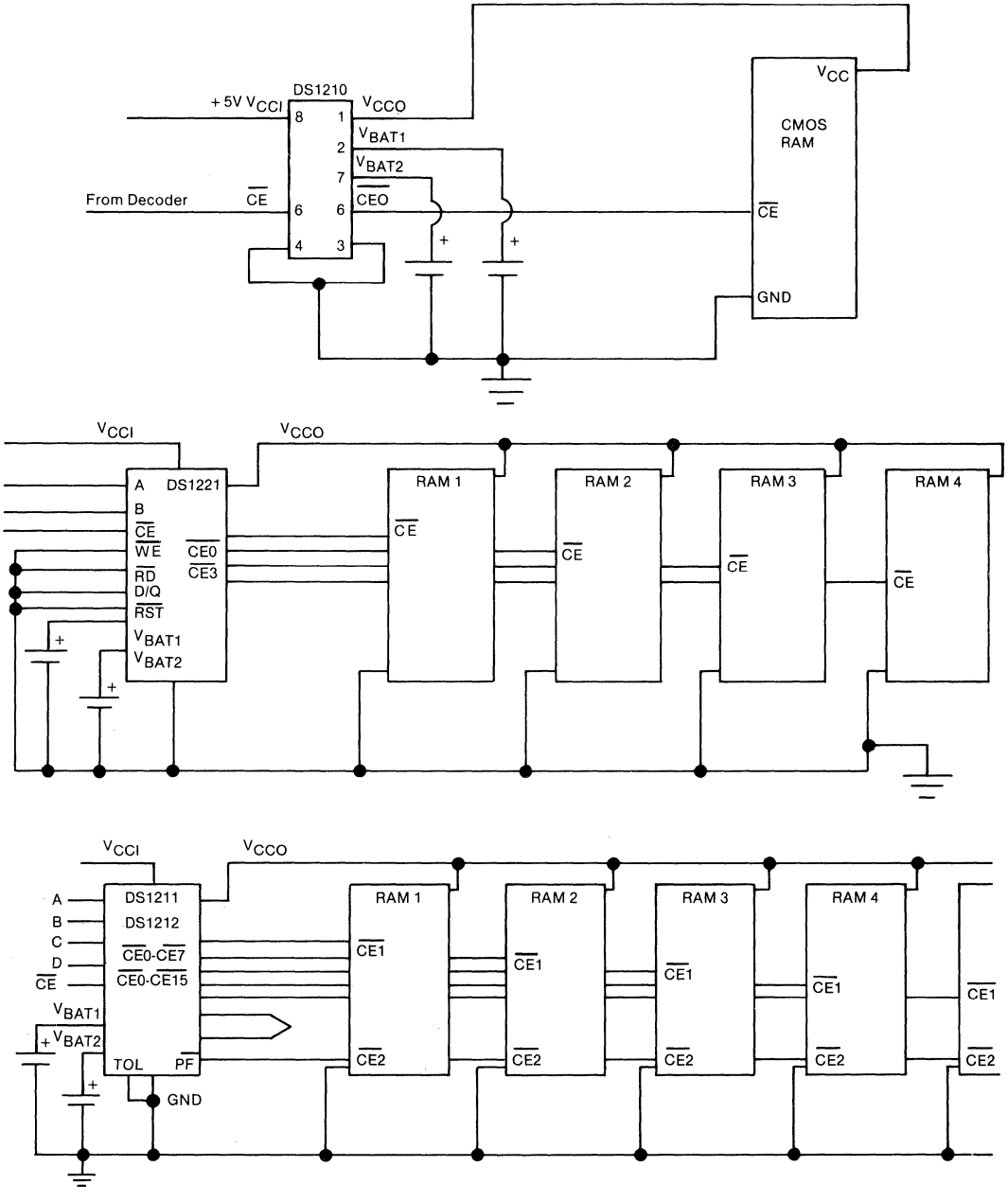
## PROPER BATTERY BACKUP METHODOLOGY

A battery backup scheme which will flawlessly retain data requires a two-part strategy. The first part involves memory itself. For a memory to retain data in the absence of power, it must have a backup energy source, a switch to direct power from the main supply or the backup supply, and detection of power failure so that the memory can be write-protected during power transients. The second part of a battery backup strategy involves control of the microprocessor. The processor should be warned in advance of impending power loss so that last minute housekeeping chores can be orchestrated. As a minimum, enough warning should be provided for an orderly shutdown before power goes out of tolerance. The amount of advance warning required is a function of application. The earliest warning can be given by sensing power supply conditions on the A.C. power line or on the filter capacitor energy reservoir upstream of the regulator. This type of power sensing allows the processor to take advantage of hold up time, which is usually several milliseconds for linear supplies and tens of milliseconds for switching supplies. A power fail signal generated from the power sensing device can be used to interrupt the processor for a software-controlled shutdown routine. After the routine is executed, the processor then enters a wait state before $V_{CC}$ (+5 volts) becomes abnormal. When $V_{CC}$ actually goes out of tolerance, the processor is forced into a reset mode which will drive all control signals to an inactive level and put the data and address bus to a high impedance state. Processor reset prevents further activity from occurring which could disturb nonvolatile memory. Reset circuitry must be designed to clamp reset in the active state until power is restored to an in-tolerance condition and the processor's internal clocks have stabilized. A stabilization period of tens of milliseconds is required. The DS1231 Power Monitor has a built-in timer to meet this requirement.

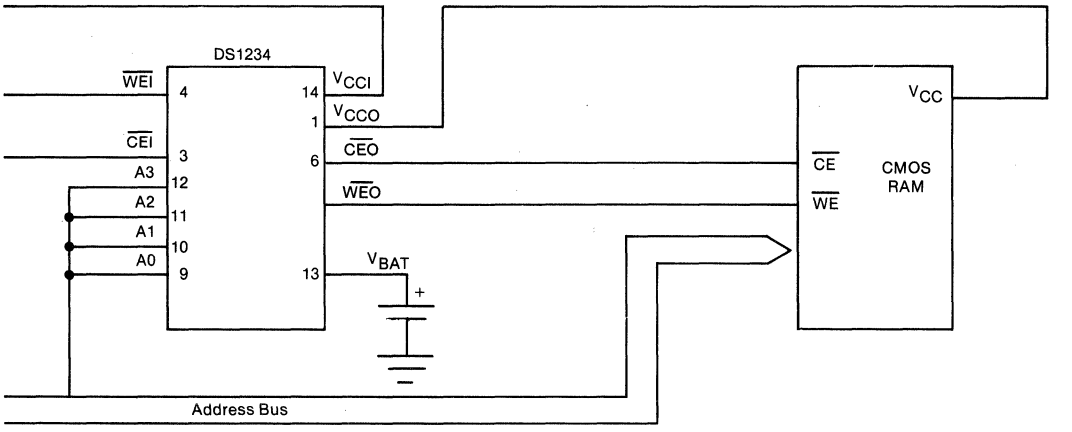
## NONVOLATILE MEMORY CONTROLLER

Converting static CMOS RAM into nonvolatile memories has often been accomplished by a number of power-consuming discrete circuits. Dallas Semiconductor's nonvolatile controllers support from one to sixteen

**NONVOLATILE CONTROLLERS CAN TRANSFORM FROM ONE TO SIXTEEN CMOS STATIC RAMS INTO NONVOLATILE MEMORIES** Figure 1



**CONDITIONAL NONVOLATILE CONTROLLER INHIBITS WRITES AND DISCONNECTS BATTERY VIA SOFTWARE** Figure 2




memories. These controllers consume insignificant battery current and perform all the circuit functions required to battery backup static RAMs, including power switching, power fail detection, write protection, decoding, and optional battery redundancy. The diagrams in Figure 1 illustrate the typical hook-up between the nonvolatile controllers and memory. Each diagram shows redundant batteries. If only one battery is sufficient, the other battery pin must be grounded. The DS1210, DS1211, and DS1212 have a tolerance pin which selects either 5% or 10% write protection points on the 5-volt supply. With the tolerance pin grounded (as shown) power fail detection occurs between 4.75 volts and 4.5 volts. Power fail detection forces the chip enable outputs to memory to a high level, thereby providing write protection. The DS1221 does not have a tolerance pin and power fail detection is fixed to occur between 4.5 volts and 4.25 volts. The DS1221 has a security mode that can be used by special order from Dallas Semiconductor. When this mode is not employed, pins WE, $\overline{RD}$, D/Q, and $\overline{RST}$ must be grounded.

## CONDITIONAL NONVOLATILE MEMORY CONTROLLER

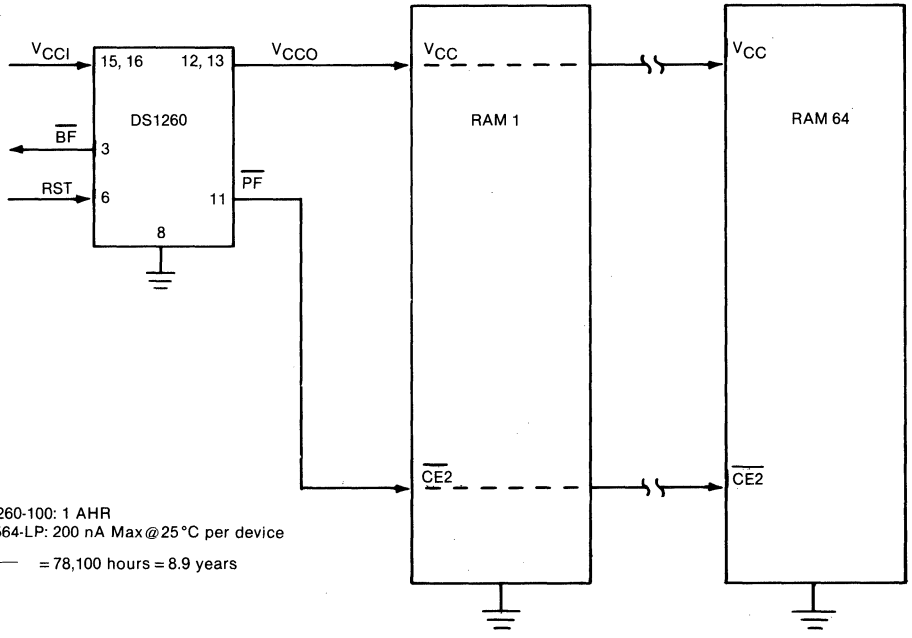
Some applications require a memory which is only written to under special conditions. The DS1234 offers an additional level of write protection for these applications by providing two software-controlled switches (see Figure 2). One switch will inhibit the writes by forcing $\overline{WEO}$ high regardless of the write enable input $\overline{WEI}$. The second switch is used to disconnect the battery, making the connected memory volatile. The switches are set by pattern recognition on address inputs A0 through A3. Pattern recognition is accomplished by presenting 16 consecutive patterns of 4 bits each on the address inputs which are strobed into the device with the chip enable signal. When the switches are set for nonvolatile operation, the DS1234 write protects connected memory via the chip enable signal by forcing the chip enable output signal ($\overline{CEO}$) to a high level when $V_{CC}$ is out of tolerance. Read-only operation is accomplished by restricting $\overline{WEO}$ to a high level. The switch settings can be changed at any time as long as $V_{CC}$ is within tolerance. The switches are nonvolatile as long as battery power is present.

## THE SMARTBATTERY

A critical element in a battery-backed-up memory system is the battery itself. Batteries had been considered unreliable and a maintenance problem. Additional problems with battery handling and mounting have also been cited as major barriers to use. This is no longer true. Dallas Semiconductor's DS1260 SmartBattery supplies 1 amp hour of lithium energy at 3 volts and has a shelf life of more than ten years. Using the proper components and design techniques, this device can be installed in a system to last the useful life of the system. However, the device is designed to be replaceable if discharge rates are so high as to deplete the energy before the system is obsolete. For convenience it has been designed to plug into a standard 16-pin DIP socket. In addition to sourcing energy the SmartBattery incorporates a semiconductor IC to solve system problems associated with battery backup (Figure 3). The SmartBattery automatically switches power as required. Up to 250 mA of $V_{CC}$ power can be routed through and 5 mA can be sourced from the battery when $V_{CC}$ is less than 3 volts. The power fail signal ($\overline{PF}$) can be used to write protect memory when $V_{CC}$ drops below 4.25 volts (typical). The battery fail signal ($\overline{BF}$) can be used to tell the processor if battery is expended. This signal reports when battery voltage is less than 2 volts.

A major concern is how to identify that a battery has full capacity, particularly when batteries are subject to uncertain handling conditions. The SmartBattery has an "electronic seal" implemented with both chip technology and special packaging to ensure absolute freshness. The reset input (RST) causes the battery supply to be disconnected from its pins so that no discharge occurs during storage, shipping and handling; therefore, battery life is maximized. Once reset, the SmartBattery is designed to remain in an off-state and then automatically reactivated when $V_{CC}$ (+5 volts) is applied. Subsequently, the SmartBattery will become uninterruptable even if the +5 volts is removed.

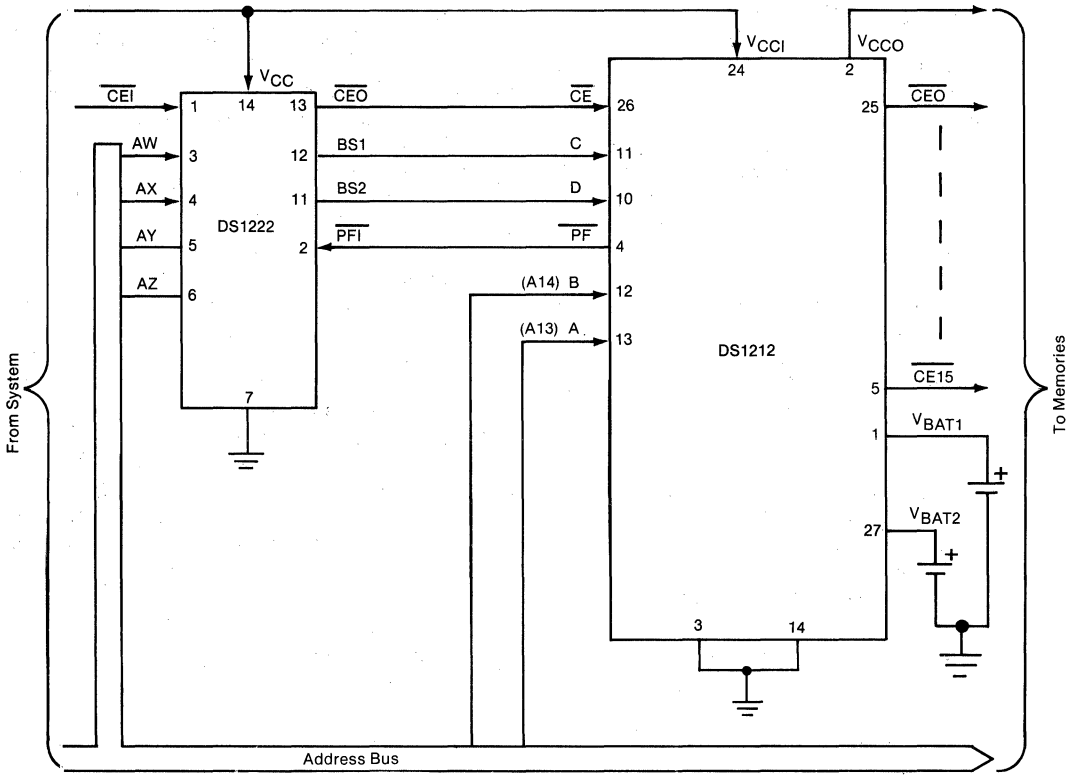
**SMARTBATTERY MAINTAINS 64 8K x 8 RAMS FOR >8 YEARS WITHOUT $V_{CC}$** Figure 3




SmartBattery DS1260-100: 1 AHR
8K x 8 SRAM TC5564-LP: 200 nA Max@25°C per device

$$\frac{1}{200 \times 10^{-9} \times 64} = 78{,}100 \text{ hours} = 8.9 \text{ years}$$

**BANK SWITCHING EXTENDS NONVOLATILE MEMORY SPACE** Figure 4



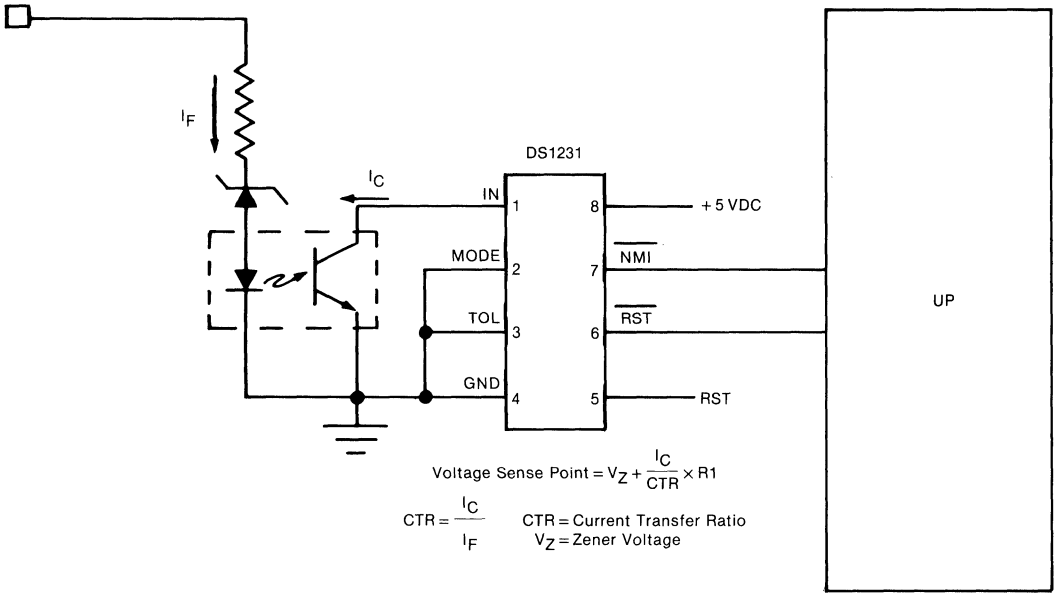

## BANK SWITCHING

While bank switching is not involved in making memory nonvolatile, it does extend the processor's address map for nonvolatile memory. Figure 4 is an example of how the DS1222 and DS1212 connect together. The application, as drawn, controls four banks of 32K × 8 nonvolatile RAM. The bank switching scheme is derived from pattern recognition on four address lines. The pattern is 16 bits deep, which also adds a level of security to memory in addition to the bank switching function.

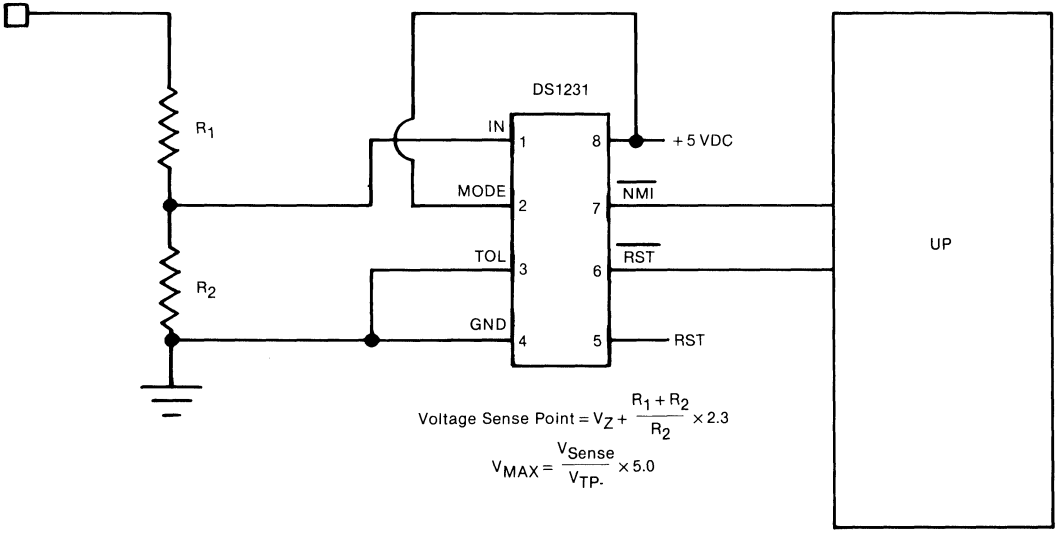
## THE POWER MONITOR

As mentioned earlier, proper battery backup methodology is a two-part strategy that must be followed in order to successfully accomplish reliable nonvolatile RAM operation. So far, controlling memory has been discussed. The second half of the strategy is controlling the processor. The DS1231 Power Monitor is a device designed to control the processor through an orderly shutdown and restart associated with power failure. An advanced warning by sensing power failure as far back into the power suply as possible is critical to an orderly shutdown. Figures 5, 6, 7 and 8 show alternate methods of sensing power levels. Figures 5 and 8 show the Power Monitor in the current mode. In this mode the DS1231 is sourcing 30 *u*A to the opto-isolators through the IN pin. Figures 6 and 7 show the DS1231 in the high impedance mode where the IN pin is a high impedance input to the voltage sense point. Methods of sensing power which provide isolation are often preferred for safety reasons. However, the simple circuit of Figure 6 is adequate for many systems. The IN pin on the DS1231 pro-

**D.C. VOLTAGE MONITOR WITH OPTO-ISOLATION** Figure 5




**D.C. VOLTAGE MONITOR WITHOUT ISOLATION** Figure 6

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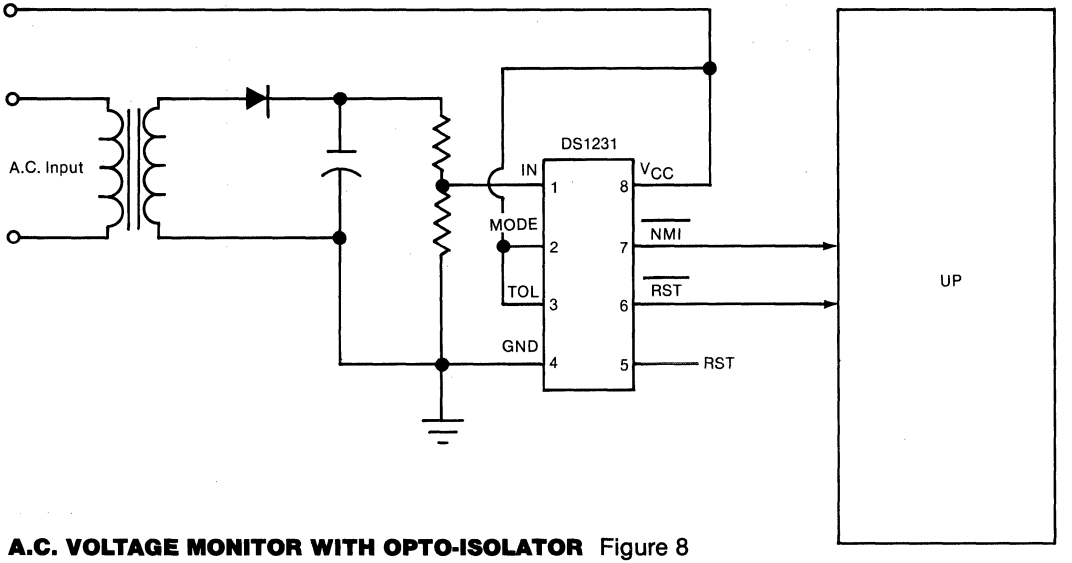
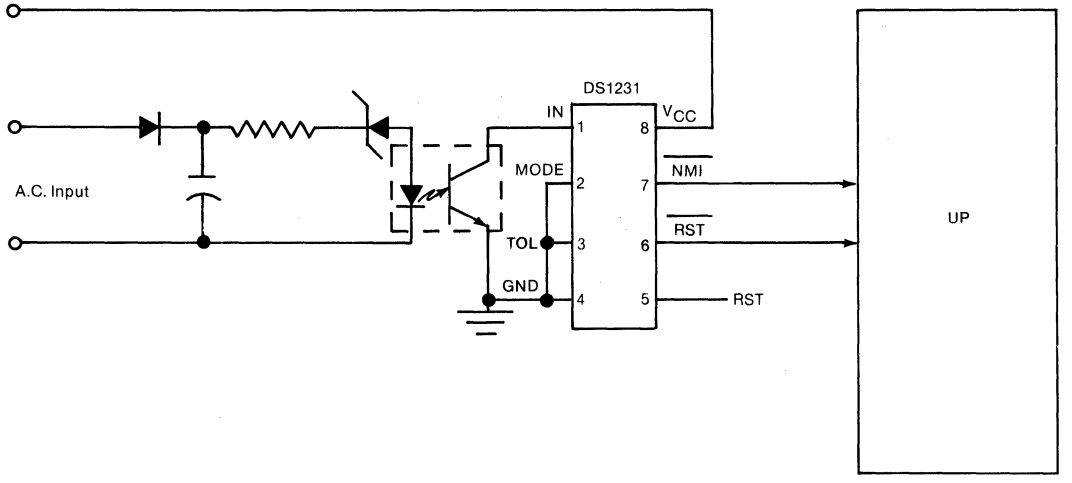
**A.C. VOLTAGE MONITOR WITH TRANSFORMER ISOLATION** Figure 7




**A.C. VOLTAGE MONITOR WITH OPTO-ISOLATOR** Figure 8



**RESET CONTROL OF MICROPROCESSORS**
Figure 9

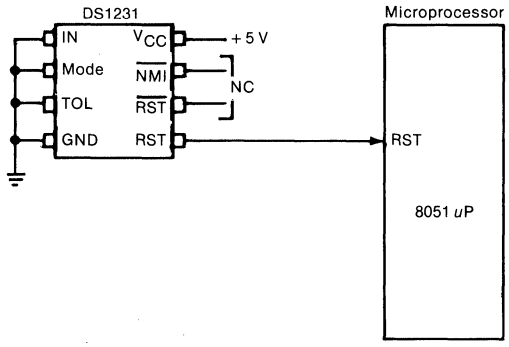
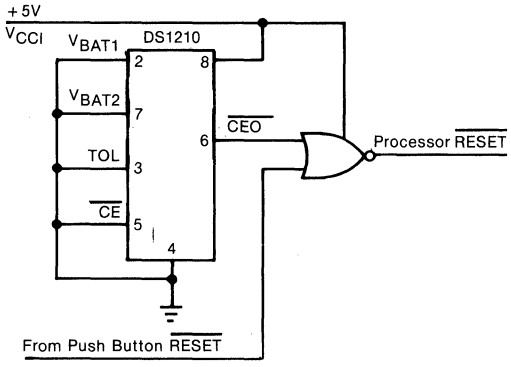



Figure 10



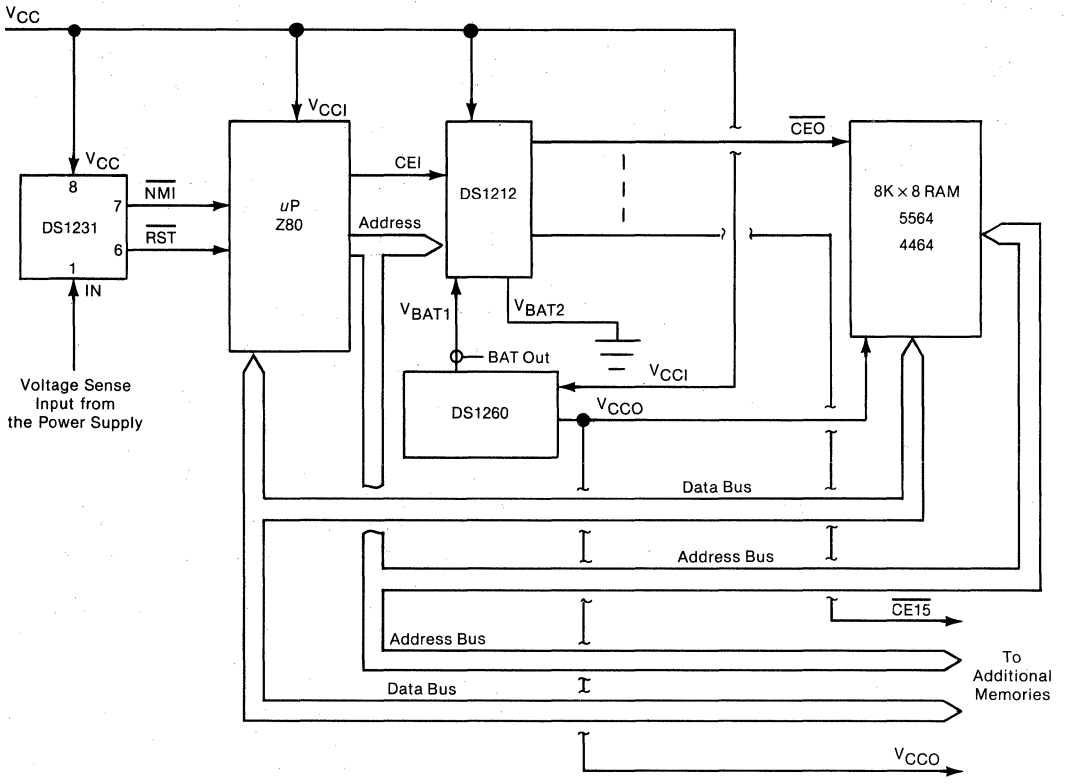

duces NMI as soon as power loss is detected. NMI, nonmaskable interrupt, is normally the highest level of interrupt in a system. Power fail software routines must be executed between the time that NMI occurs and loss of $V_{CC}$. As $V_{CC}$ falls below the trip point which is set by the tolerance pin, reset (RST and RST) will go to the active state. The function of placing a processor in reset stops all activity. The DS1231 holds the RST and RST signals active until +5 volts is back to an intolerance condition and a 250 ms minimum has elapsed. The delay on power up allows the processor to stabilize before executing instructions.

Alternate methods of processor reset control are shown in Figures 9 and 10. Neither of these circuits involves early warning. This is acceptable in applications where a software controlled shutdown is not required. The RST and RST signals must still prevent the processor from inadvertently writing memory on power up and power down. Either of the circuits shown in Figures 9 and 10 can control the processor. The implementation using the DS1210 as a reset controller may not be as cost effective as the DS1231 because of the external gate to correct the level of CEO.

**COMPLETE SYSTEM**

The block diagram of Figure 11 shows a complete nonvolatile memory system. The DS1231 provides for both software notification and hardware control of the processor during power down/up. The DS1212 is used as a decoder and nonvolatile controller for up to 16 memories. Finally the DS1260 SmartBattery sources uninterruptable power for both the DS1212 controller and the memories. A system designed in this manner can be crash proof and can retain data for the useful life of the system. The block diagram of Figure 12 has all of the capability of the circuit just described with two important additions. First, time-of-day information has been added, using a Dallas Semiconductor DS1215 TimeKeeper. Continuous power is supplied to the DS1215 via the SmartBattery. The DS1215 has the advantage of not requiring a decoder. The watch feature is accessed transparent to memory via software controlled pattern recognition similar to that described earlier for the DS1222 and DS1234. The circuit implementation adds a time stamping and dating capability at a very modest increase in cost. The final addition to this circuit is the DS1222 Bank Switch. The Bank Switch is used to selectively inhibit writes to RAM under software control. This is accomplished by routing write command signals from the processor through the DS1222. When the DS1222 is first powered on, the write command to the RAMs is blocked preventing data from being inadvertently changed. After power up write commands can be passed through at the discretion of software. The

**INTEGRATED BATTERY BACKUP** Figure 11



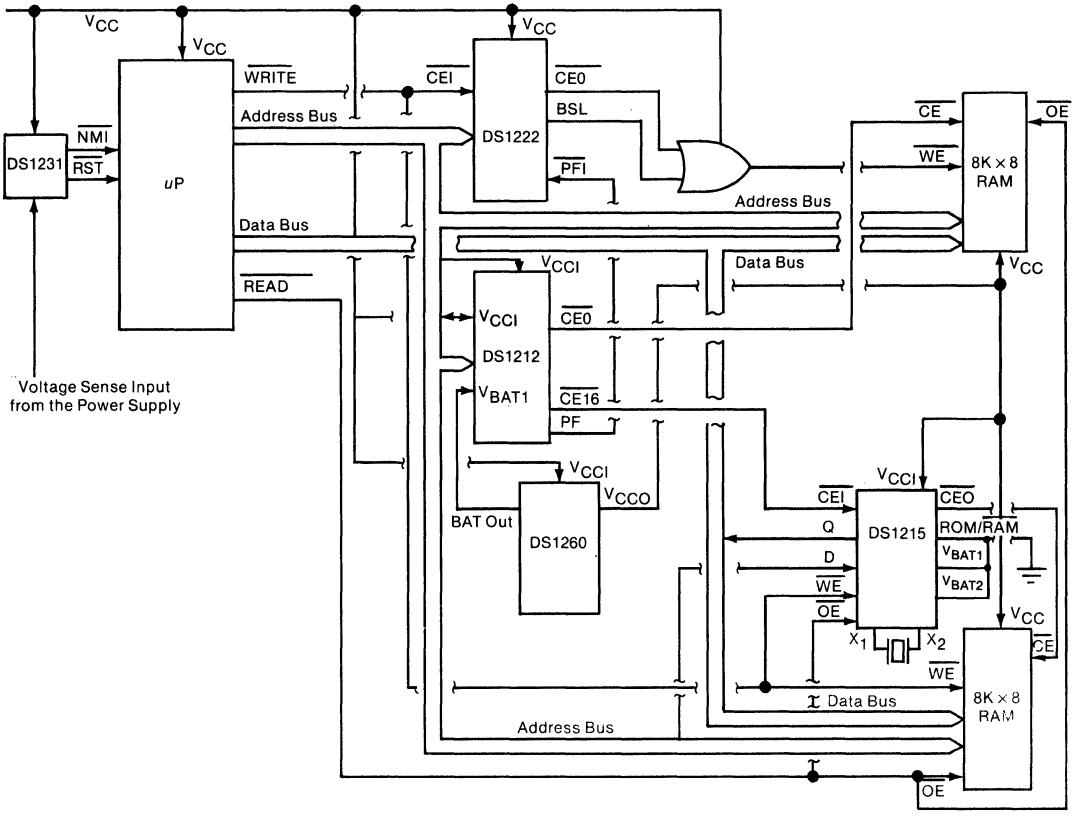

commands can be enabled via pattern recognition on four address lines using the write strobe to gate this pattern into the DS1222. The use of the DS1222 in this manner gives an added level of write protection. A fully implemented version of this circuit supports 16 nonvolatile memories partitioned in four groups. Each group can be selectively write protected with the DS1222 circuit.

## CONCLUSION

Battery backed up memory applications are increasing at a rapid pace. The principal reason for growth is the benefit accrued to the system when RAM can be made to remember. While the need for battery backup has been increasing, methodology and standard circuits to implement designs have been inadequate. In fact, many battery backup implementations lack the thoroughness to reliability protect data during power transients.

A solution to problems of battery backed up memory design is embodied in a modular product line from Dallas Semiconductor called Integrated Battery Backup. This family of products includes the Nonvolatile Controller (DS1210, DS1211, DS1212, DS1221, DS1234), SmartBattery (DS1260), Power Monitor (DS1231), Bank Switch (DS1222) and a TimeChip (DS1215).

**INTEGRATED BATTERY BACKUP SUPPLEMENTED WITH SOFTWARE WRITE PROTECT AND TIMEKEEPING** Figure 12



# Dallas Semiconductor Security System Locks Up Software

*Application Note-8*

## ELECTRONIC DESIGN EXCLUSIVE

Security is a fact of business life. Information and property must be protected from fraud, theft, and misappropriation. Personal computer software represents both these kinds of items, and yet the multibillion-dollar industry has virtually no protection.

Of the methods employed to protect software from illegal copying, the most popular ones use programming tricks. Unfortunately, those methods also stop the legitimate user from backing up valuable disks. To make matters worse, programs have been developed to defeat most software-based schemes for copy protection.

A better solution lies in the marriage of software and hardware. With such a merger in mind, security takes the form of a special key. The DS1204 system permits only legitimately purchased software to be run, and it does not unduly disturb the personal computer user or prevent him or her from making backups to hard disks (see *Electronic Design*, September 5, 1985, p. 219). A package about the size of a postage stamp, which contains an IC and a lithium energy source, stores identification and an unrevealable code word that protects a secure, nonvolatile read/write memory. Upon installation of the DS1250, a simple key ring that consists of a five-contact key receptacle connected through a cable to an intermediate socket, the key ring and key lock-out precoded software from all but rightful keyholders.

The byte wide key ring implementation begins with a system board that contains a 28-pin socket with or without a resident ROM. (In all personal computers, there is at least one ROM that is used for boot sequences, basic I/O system implementation, or some form of dedicated software monitoring.)

## READY TO GO

With the key ring inserted in the ROM socket, the ROM inserted into the key ring, and the key inserted into the clip at the end of the cable, the system ROM functions normally. The address and data lines are transparently sent through the byte wide key ring socket and presented to the system ROM as usual. As a result, existing unprotected software will run on the system.

However, if certain address lines are driven with specific patterns, the software activates the key ring, which disconnects the ROM from the system board and ties the address and data lines to the key ring's own bus. At that point, communication to the system board ROM socket is transparently passed on to any device that is inserted into the key clip.

## A MEMORY BARRIER

A partitioned memory in the key sets up a system of barriers, preventing unauthorized access to software. The first barrier is possession of the key, since the silicon chip inside the key is extremely difficult to copy. If a copy is nevertheless made, the code words and nonvolatile memory are lost during what may otherwise seem to be a successful process of reverse engineering.

The key stores 64 bits of user-definable identification code, and a 64-bit security match code that protects 128 bits of read/write nonvolatile memory. The 64-bit security code in the key, once programmed for one particular disk by the software vendor, cannot be read or derived by the user.

Another barrier can be thrown in the pirate's path: the key manufacturer, using a laser, can brand another 13 bits of key memory with a code unique to the software maker.

A final level of protection is afforded through intricate programming techniques. Because the electronic key functions as a read/write memory, it can "converse" with deeply embedded software locks and actually change its own password from use to use.

## EASY TO USE

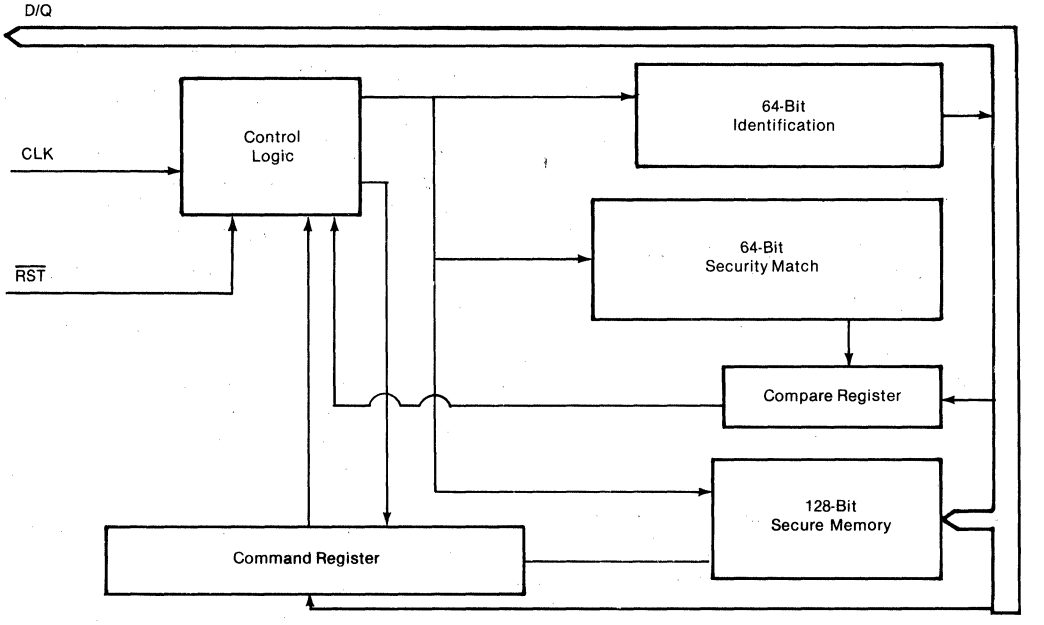
A low pin count and a guided entry to its socket make the device transportable and user insertable. A lithium battery supplies power for decades.

The electronic key has two modes of operation. In the normal mode, data transfer takes

place between the key ring and the key (Fig. 1). To initiate a data exchange, $\overline{\text{RESET}}$ is taken high and 24 bits are loaded into the command register from the computer. That 24-bit protocol stores an unalterable code that includes the 13 burned-in bits. If the key's command register proves to be loaded properly, communication continues (Fig. 2).

Following the 24-bit exchange, 64 read cycles examine the identification RAM in the key. The computer then writes 64 bits to the compare register, also on the key. If that block agrees with the security match RAM, permission is given to read or write the 128-bit nonvolatile memory. If a match is not found, access to additional information is denied. The 128-bit section can be changed indefinitely to meet the needs of a dynamic protection scheme.

Figure 1




**NOTE:**
In the normal mode, data from the computer is applied to the key through the key ring. That data is compared in the command and compare registers. Data from the key is then returned to the computer to complete the verification procedure.

Driving $\overline{\text{RESET}}$ high also initiates the program mode (Fig. 3). The computer software loads 24 bits into the command register on each low-to-high transition of the clock input. If the key's command register is not properly loaded, the remainder of the program cycle is ignored. However, if the command register is properly loaded, then the following 128 bits are written to the identification memory and the security match memory after the data in the 128-bit nonvolatile RAM has been erased by the key.

Dynamic interaction with the key can be maintained throughout program execution. The matching codes of the key and the program on disk are continually updated with a pseudorandom number—say, the check sum of the system address space at a given instant in time.

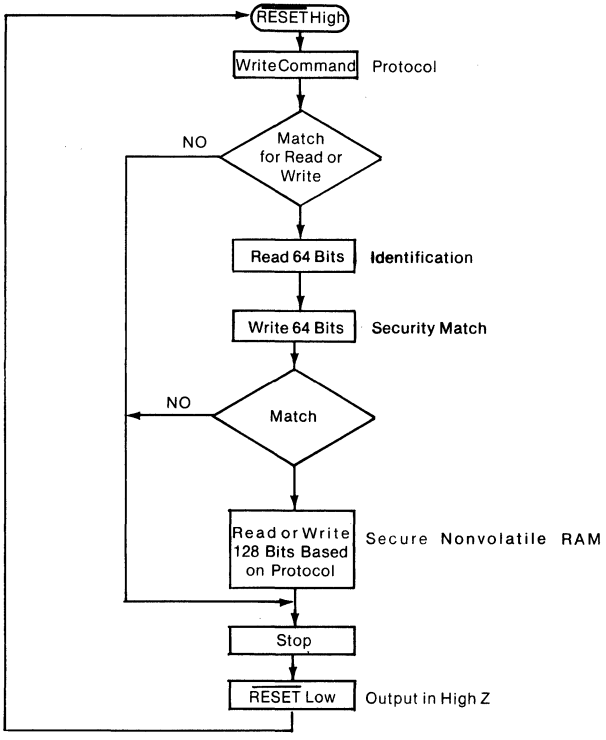
At various points in the program, the checksum value in the application program is matched with the value in the key. If they do not match, program execution is aborted. If they do, another check sum is written to the application program on the disk and to the key, and execution of the program continues.

Alternatively, program parameters or instructions themselves can be stored in the key's 128 bits of nonvolatile memory. Those code fragments are called up, or dynamically loaded, and initiate actions that are crucial to the proper functioning of the application program. If the key is improperly programmed or programmed with invalid information, those code sequences will cause the program to deliver unpredictable and incorrect results to the unauthorized user.

## RUNNING RINGS AROUND THE DATA

The key ring adapts the electronic keys, with their low pin count, to JEDEC standard byte wide memory signals. Any 28-pin RAM, ROM

Figure 2




**NOTE:**
The key is matched against a particular program in a sequenced two-way transfer of data. Previously stored data supplied by the software enables each key to be tailored to a program.

or EPROM device can be removed and placed in the intermediary socket of the key ring. The combination can then be reinstalled in the original ROM location, leaving the system intact. Optional key rings are available for 16-pin dynamic RAM and 24-pin ROM sockets, and for the parallel printer port of IBM or IBM-compatible personal computers.

The intermediary socket contains a CMOS chip that redirects information flow from the byte wide memory to the inserted keys, according to special software-generated address sequences. Data transfer of 50 Kbits/s are possible with an assembly language software driver of less than 500 bytes.

The key ring protocol is derived from address inputs $A_0$, $A_1$ and $A_2$ (Fig. 4). Those addresses are latched on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}/\overline{CAS}_{in}$ and $\overline{RAS}/\overline{OE}_{in}$. $A_0$ defines the data that is compared for recognition. $A_1$ activates the communication sequence, while $A_2$ clocks in information defined by $A_0$.

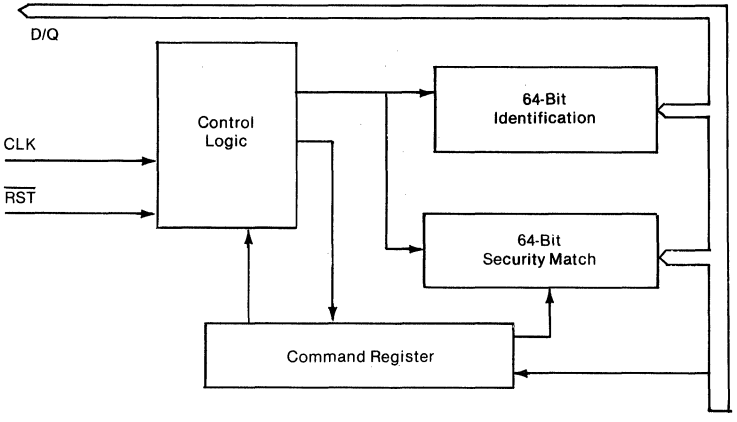
As noted, data transfer through the key ring occurs by first matching a 24-bit pattern from the software. That pattern is presented to a register on each rising edge of a strobe. Therefore, data is entered for comparison to the key ring protocol at the end of each memory cycle.

While keeping $A_1$ high, the proper information must be presented on $A_0$ to match the 24-bit pattern. Address input $A_2$ generates the shift signal that supplies data to the 24-bit register for comparison with the pattern that has been placed in the key by the manufacturer.

Information is loaded one bit at a time on the rising edge of the shift pulse, and each shift cycle must be generated from two memory cycles. The first memory cycle sends $A_2$ low, setting the shift clock low. The second memory cycle sends $A_2$ high, causing the transition necessary to shift a bit of data into the 24-bit register. $A_0$ is kept at the same level for both memory cycles. Address input $A_3$, which controls the direction of data going to and from the keys, is not used during pattern recognition in the key ring protocol.

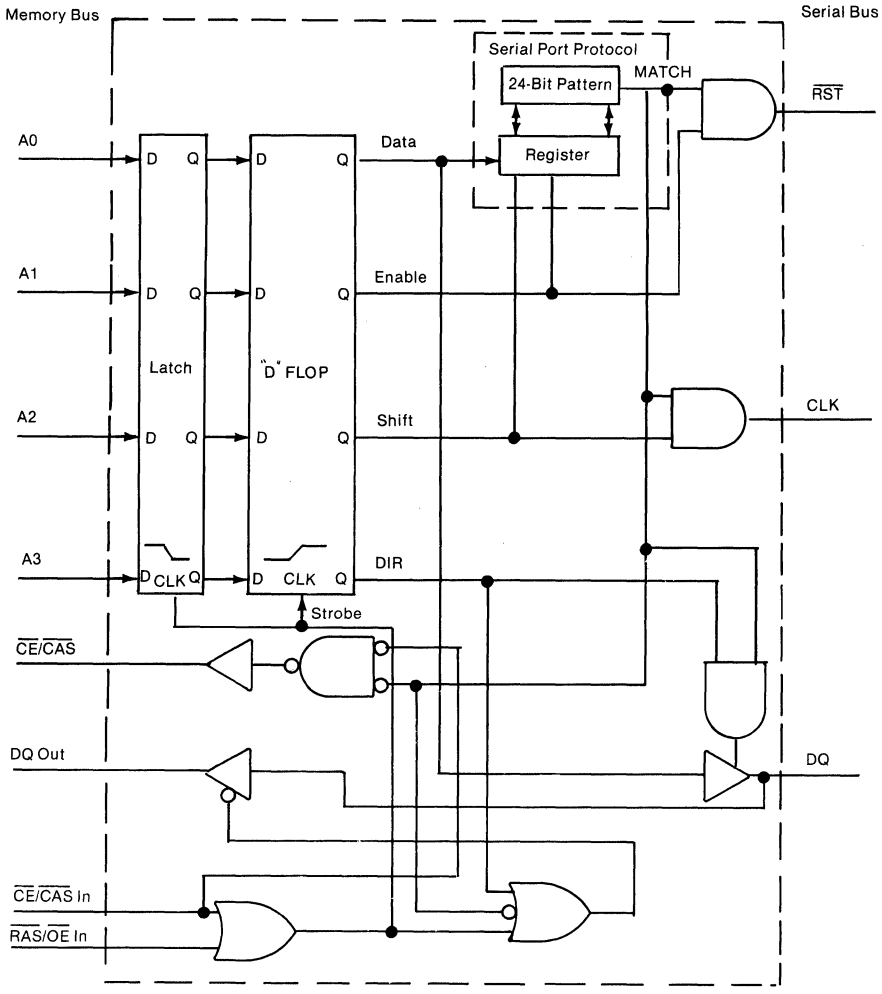
After the 24-bit pattern has been correctly entered, a match signal is generated and logically combined with the enable signal to generate $\overline{RESET}$ for the key. The match signal is also used to disable the original memory device (now plugged into the key ring) and to enable a gate allowing the key's

Figure 3




**NOTE:**
In the programming mode, after the first 24 bits are written, the key checks to see that they contain a valid programming code. If so, 128 bits are written to the identification and security match RAMs.

Figure 4




**NOTE:**
The key ring provides an active interface between the host computer and the key. Key data plus control pulses are provided by the address line.

Data I/O line to drive the computer memory bus. When $\overline{\text{RESET}}$ is driven high, devices attached to the key ring become active and subsequent shift signals derived from $A_2$ will be recognized as the key clock.

The data signal for the key on the $A_0$ line depends on the level of the direction signal on $A_3$. When $A_3$ is high, data as defined by $A_0$ will be sent out on the Data I/O line. When $A_3$ is low, devices attached to the key ring can drive the memory bus output line. The data direction bit must be set low to read key data.

A sophisticated example of interaction between the electronic key and the application software package involves the use of a data encryption algorithm. The application program is encrypted as distributed from the factory, using the Data Encryption Standard or the Rivest, Shamir, Adleman public key encryption algorithm.

The public key is contained on the program media and the private key goes into the electronic key's memory. A kernel, invoked when the application program is activated, decrypts the remainder of the binary version of the running program, producing a functional one. That program then communicates with the electronic key, providing a greater degree of program security.

Dynamic encryption of the application program can be expanded, so that the electronic key contents and the program image are encrypted on program exit. The result: both are different for each operation of the program.

The electronic key is not limited to software security. Because it is small and user-insertable, it can be carried, stored, and used just like conventional keys and credit cards. The electronic key has the added benefit, however, of a nonvolatile read/write memory and a data capacity that surpasses most credit cards and keys in use today.

# Dallas Semiconductor System Configuration

*Application Note-9*

## SYSTEM CONFIGURATION

A common problem facing systems designers is the need to make a product general enough to meet the needs of many customers without unduly restricting its utility for a specific user. Often the solution is to provide some ability for the end-user to tailor the system to his specific needs. Typically, this customization or personalization of a system is accomplished through the use of mechanical dip-switches or jumper wires and pull-up resistors which provide a nonvolatile logic input to finish wiring the system after the fact. Many times these switches must be set manually by non-technically inclined individuals. Asking the user to perform what seems to the designer to be a simple task often results in confusion, which leads to error, ending in expensive one-to-one customer interface to correct. Needless to say, the frustration experienced by the user in these attempts can only have a detrimental effect on a customer's perception of the product. Additional shortcomings of mechanical switches include a physical placement which may be difficult or hazardous to access should they need to be altered as well as virtually precluding the ability to dynamically reconfigure the system.

Dallas Semiconductor has developed a group of products designed to eliminate these problems without compromising the nonvolatility of a system's configuration. By using the DS1206 Phantom Interface and the DS1290/92 Eliminator, a system can now have a nonvolatile switch equivalent which is set through the system bus. Access to the settings may now be something as familiar to most users as a keyboard, in fact remote system configuration over a phone link is possible. Instead of trying to understand the words on a written set of instructions, a customer may configure a system through a software-generated question-and-answer session. This approach makes use of a common interface to configure the system, the result being fewer errors, a higher degree of customer satisfaction and a lower technical support cost.

The DS1290 is a 16-pin, 300-mil package which provides 8-switch equivalents. Unlike mechanical switches which require external pull-up resistors to create a logic 1 state, the pins of the Eliminator provide valid logic levels directly. The switch settings are set and verified through a serial port which allows new states to be entered or the current ones read without disturbing the present configuration. The Clock (CLK), Data In (IN), Transfer ($\overline{T}$) and $O_A$ pins, shown in Figure 1, provide this interface, while the Clear ($\overline{CLR}$) pin causes all switches to be reset to a logic 0. Referring to Figure 2, note that the device is organized internally as a shift register which is clocked on the positive edge of clock with the outputs of all but the last stage being latched to the pin on the falling edge of $\overline{T}$. The last output ($O_A$) is not subject to $\overline{T}$ control and ripples directly to the pin. This feature allows $O_A$ to be connected to IN through an isolation resistor to effectively create a DQ line for system read of settings, or permits any number of Eliminators to be cascaded in serial fashion. Included within the device are power fail protection circuits to hold the output states in the event of system power loss and ignore any spurious CLK, $\overline{T}$, or $\overline{CLR}$ signals that could be generated by power transients. The output drivers are driven directly by system power, but gated by logic driven by internal power, so high settings will track the board supply and low outputs will always pull actively to ground. This effectively emulates the common switch/resistor arrangement by having well defined logic levels under low supply conditions with the obvious advantage of no DC current path through the low or logic 0 switches. The DS1292 is a 16-switch equivalent housed in a 24-pin, 300-mil package.

The DS1206 Phantom Interface, shown in Figure 3, considerably simplifies the interface between the system bus and the serial port of the DS1290/92. The device sits on the bus as a passive listener until a specific pattern of addresses sampled on the later falling edge of $\overline{CE}/\overline{CAS}$ or $\overline{OE}/\overline{RAS}$ has been presented to it. Once the pattern is matched the serial port is enabled with A0 as DATA IN from the system, A1 as $\overline{RST}$ (connected to $\overline{T}$ of the DS1290/92), A2 as CLOCK and A3 is the

direction control which determines whether data is coming from or going to the system. To close or deactivate the port simply hold A1 low on the later falling edge of $\overline{CE}/\overline{CAS}$ or $\overline{OE}/\overline{RAS}$. The pattern recognition requirements on the address bus make it all but impossible that the port could be deactivated accidentally (the probability of an arbitrary set of 48 memory cycles opening the port are 1 in $2^{145}$ or $4.5 \times 10^{43}$).

The simplest implementation of the DS1206/DS129X is one in which the designer neither needs nor desires a direct software verification of the configuration settings. In such a system the DS1206 serial port is opened and the software-determined settings are sent to the DS129X. The port is then closed and the settings are verified by observing the behavior of the system.

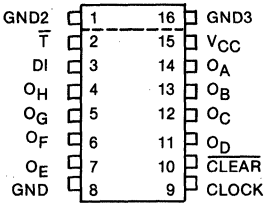
Some designers may desire to verify the settings within the configuration software. The DS1206/DS129X provide a way for the software to directly verify that the settings are what was requested before the board is put in service. Pictured in Figure 4 is an example of a system for the IBM Personal Computer. This board demonstrates the use of the Phantom Interface/Eliminator by allowing a configuration to take place under keyboard control. The configuration will be the board address as well as any other user-defined system attributes (*e.g.*, baud rate). Once the configuration has been set and verified, reads and writes of the memory may be done in the normal fashion, with no interference from the Phantom Interface or Eliminator. A typical sequence of events for installing this board are: 1) The user inserts the board into an expansion slot; 2) After booting the PC, a vendor-supplied floppy is inserted into the drive and a configuration program is executed; 3) The software makes simple inquiries to determine the board address and attributes and translates the user responses into valid settings; 4) The DS1206 is opened and the appropriate settings are written to the DS129X. Note the $\overline{CLR}$ function provides the ability for a manual return to the unconfigured stated should that become necessary.

In using this system configuration approach, one should be aware of several things that are illustrated by the example board. First, it is not necessary to predict an unoccupied memory space in which to place the unconfigured board because the DS1206 on a virgin board can be enabled by any address. In the execution of a sequence of code a processor will perform fetches from memory interspersed with the requested I/O operations. The DS1206 is unable to distinguish the software-requested memory reads from the instruction opcode fetches; therefore the DS1206 on an unconfigured board must be enabled by only write cycles to any address location. After the DS1206 is opened writes through the port are allowed independent of address, but reads only from the current board address. On a virgin board, this may conflict with memory already resident in the system. Contention can be avoided by first opening the Phantom Interface port, setting the Eliminator outputs to some unoccupied address and closing the port. The act of closing the port will bring the $\overline{T}$ line to the DS129X low and update the outputs to the current settings. The protocol for the serial port may be reissued and a read performed at the board address. The board select is accomplished by using a common technique, comparing the address bus to the switch outputs using a 74LS688 TTL comparator. Note that setting the DS1290 output labeled $\overline{CONFIG}$ to a logic 0 will cause the data from the board to come from the serial shift registers of the cascaded DS129Xs, rather than from the memory. The switch settings are read by holding $\overline{T}$ high ($\overline{RST}$ from the DS1206, A3 on the system bus) which holds the old settings at the outputs until it is brought low again, and issuing a clock stream through A1, whose length matches the number of bits on the DS129X chain. The last output on the DS129X is not subject to the $\overline{T}$ control and will therefore toggle as the data stream is brought through the shift register. This unique output allows the settings to be interrogated or Eliminators to be serially cascaded without changing the output states. By connecting the last output of the chain to the DQ line from the DS1206,

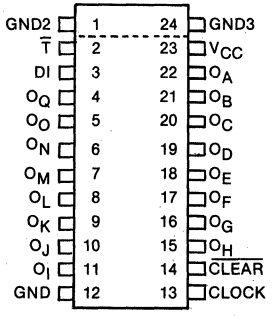
through an isolation resistor, data can be serially shifted to the system and at the same time be fed back into the DS129X chain. When the port is closed the outputs of the DS129X will be updated, but because the number of clocks matches the number of bits in the chain and the last bit of the chain drives the input, the states will not change. Once the software has verified the settings are correct, the port should be opened once again and the same bit stream rewritten, but with the $\overline{\text{CONFIG}}$ bit set high. With the $\overline{\text{CONFIG}}$ bit high the serial port is disabled and no further writes or reads can be done through it. The board is now enabled to respond to reads and writes of its registers at the board address. On this board, the 74LS374 device is the register bank, with the 74SL244 performing the transfer of the data to the system bus during reads. Should it become necessary to change the board address or attributes, one simply brings the $\overline{\text{CLR}}$ pins on the DS129X to ground (or only the particular device which has the $\overline{\text{CONFIG}}$ bit) to return the board to an unconfigured state. The setting sequence may now be repeated as desired. Pulling $\overline{\text{CLR}}$ low may be accomplished in on of several ways, using a normally open, momentary contact-to-ground switch (the $\overline{\text{CLR}}$ pin has an internal pull-up resistor), a simple shunt as a jumper, or even a second DS1206 to allow the protocol match at a hardwired address location to cause a clear under software control.

Mechanical dipswitches are usually perceived as a necessary evil in the design of a system, used only as a last resort to provide some flexibility to the customer base. With the introduction of the DS1206 Phantom Interface and the DS1290/92 Eliminator a designer no longer needs to compromise a system's flexibility for ease of use. A high degree of flexibility can be maintained and at the same time the ability of a user to mold a system to a particular use in enhanced.

**ELIMINATOR** Figure 1

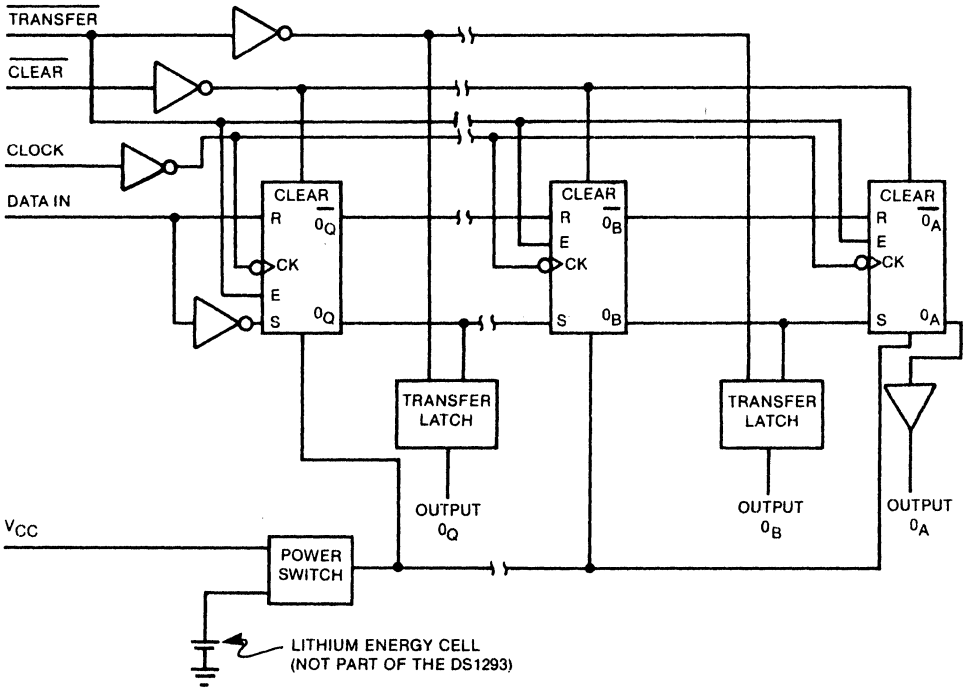



**DS1290**

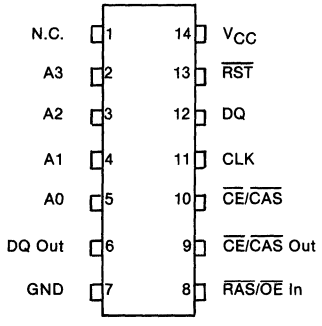



**DS1292**

**BLOCK DIAGRAM—DS1292** Figure 2




**DS1206 PHANTOM INTERFACE** Figure 3

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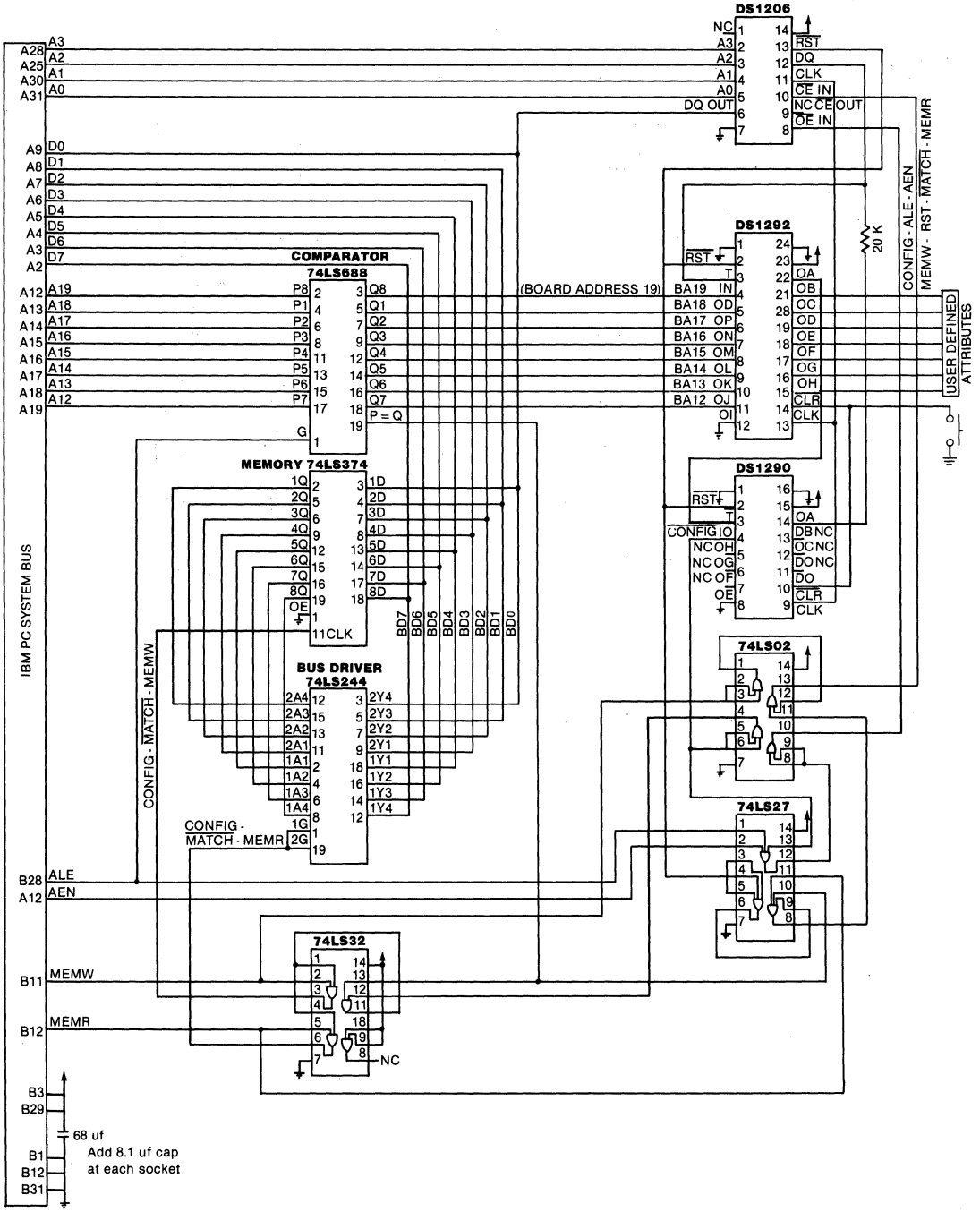
**IBM PC EXPANSION BOARD**
**EXAMPLE SHOWING CASCADED ELIMINATORS** Figure 4



# Dallas Semiconductor Nonvolatile Configurable Logic Using the DS1260 SmartBattery

*Application Note-10*

## INTRODUCTION

This application note describes the use of the DS1260 SmartBattery to provide nonvolatile operation of one or more Xilinx/MMI XC-2064 Logic Cell Arrays.

The LCA is a CMOS logic array device in which the internal configuration is determined by self-contained bits of RAM storage. The data contained in this RAM is used to define logic block functions, configuration of I/O blocks, routing of internal signals, and other options. As a result, the user can quickly implement complex digital logic functions directly without the requirement for masking or other vendor performed programming steps. In addition, the use of internal RAM allows logic design changes to be quickly implemented and verified in the prototype system. Complete re-configuration "on-the-fly" of the final production system is also possible.

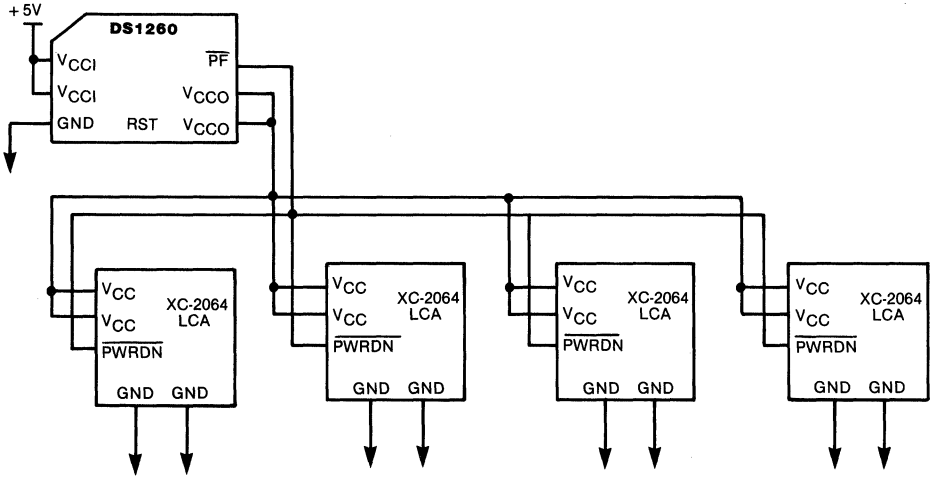
The use of RAM for holding the LCA's configuration data allows a maximum amount of flexibility in a programmable logic device. Without nonvolatile support, however, the device must be re-loaded from external memory each time that the configuration data is lost due to a power down or to a brownout condition. This not only requires additional memory to contain the logic configuration data, but also a considerable amount of time following power-up to perform the re-load operation.

The DS1260 alleviates these problems by providing nonvolatile support with a minimum impact on system hardware. The DS1260 directly interfaces to three pins on the LCA to perform the nonvolatile control function with no additional source circuitry. In addition, the embedded lithium energy source within the SmartBattery provides sufficient capacity to maintain the logic configuration data in several LCAs for 10 years in the absence of $V_{CC}$.

## SCHEMATIC DIAGRAM

The schematic shown in Figure 1 illustrates the required connections between the SmartBattery and one or more Xilinx/MMI LCAs. Two $V_{CCI}$ ($V_{CC}$ In) lines are present on the DS1260 and may be connected to the system power supply line. The two $V_{CCO}$ lines on the DS1260 may be directly connected to the two power supply inputs on LCA as shown. The $V_{CCI}$ lines are internally tied together within the DS1260 as are the $V_{CCO}$ lines, so that there will be no voltage differential across either of these two sets of pins.

**SYSTEM SCHEMATIC** Figure 1



The $\overline{PF}$ line of the DS1260 is used to directly connect to the $\overline{PWRDN}$ input to the LCA. This DS1260 will use this line to automatically place the LCA in its standby state when power is cycled on and off.

Multiplied LCAs may be controlled from a single SmartBattery simply by repeating the same connections to the additional devices as shown in the schematic.

**POWER CYCLING OPERATION**

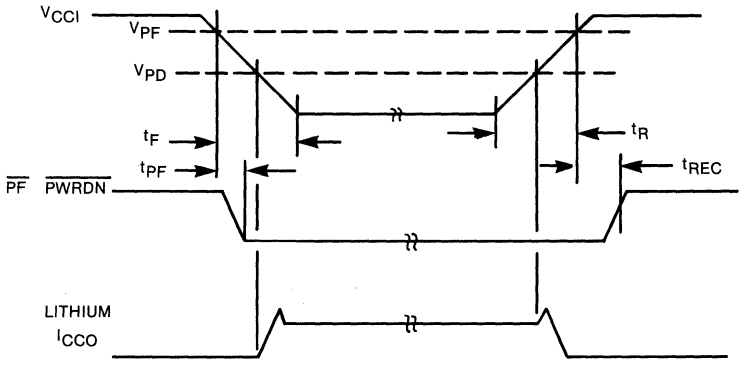
The timing diagram in Figure 2 illustrates the timing operation of the system when power to the system is cycled off and on. During normal system operation, incoming $V_{CC}$ voltage is monitored by the DS1260 for two thresholds below nominal operating voltage. Both of these thresholds are detected by the SmartBattery as $V_{CC}$ decays in a power-down situation. The first (highest) threshold which is detected during a power-down is the Power Fail Voltage ($V_{PF}$). When $V_{CC}$ falls below this value the $\overline{PWRDN}$ pin on the LCA is pulled down to its active low level by the $\overline{PF}$ output from the embedded control IC. This action will force the LCA to suspend all operation and go into its low power consumption mode. All clocks will be stopped within the device and all outputs are placed into high impedance state. All configuration data is maintained in the device when PWRDN is held at its active low level.

As $V_{CC}$ voltage continues to decay during a power-down it will eventually drop below the second (lower) threshold detected by the SmartBattery, which is Power Down Voltage ($V_{PD}$). When this occurs the internal lithium source is automatically switched to the $V_{CC}$ pins on the LCA device and the $\overline{PWRDN}$ input will continue to be held in its active state. At this point the configuration data will be maintained by power supplied from the lithium source.

During a power-up, the reverse of the sequence described above will take place. When $V_{CC}$ rises above the $V_{PD}$ threshold, the $V_{CC}$ lines of the LCA will be switched from the lithium source to the system $V_{CC}$ lines. When $V_{CC}$ subsequently rises above the $V_{PF}$ threshold, the $\overline{PWRDN}$ pin of the LCA will be driven to its inactive high level, and full operation of the device can then take place.

There are only two timing considerations which are of concern to the system designer. The first is the fall time slew rate of the incoming $V_{CCI}$ voltage. As specified in the DS1260 data sheet, the minimum fall time ($t_F$) must be no less than 300 $\mu$s. This is to insure proper operation of the $\overline{PF}$ signal and switching of $V_{CCO}$ from the $V_{CCI}$ input voltage to the embedded lithium source. With a reasonable amount of capacitance on the $V_{CCI}$ line that is normally associated with most power supplies, this timing requirement presents no problem. The minimum rise time slew rate is specified as minimum of 1 $\mu$s, which will be met by default in most designs due to the capacitance described above.

**POWER CYCLING TIMING** Figure 2



The other important timing consideration is the recovery delay time associated with the $\overline{PF}$ output of the DS1260 following a power-up condition. In this case, the delay time is specified at a maximum of 100 *us*. This implies that the LCA will not be allowed to begin operation for this length of time in the worst case. As a result, no logic should be implemented in the LCA which must begin operation within this timeframe.

**RESET (LITHIUM DISCONNECT)**

The Reset input to the SmartBattery can be used to disconnect the lithium source from the LCA $V_{CC}$ lines. This feature is useful in situations where the system is to be powered down for a long period of time without the need for data retention, as might be the case when the system is stored in a stockroom. By disconnecting the lithium source, its full energy capacity can be assured at the time when use of the system begins. Accidental discharge is also prevented during shipping and handling. This feature is activated with a high-going pulse to the RST input while system power is being applied above the $V_{PF}$ threshold. When system power is removed following this action, the LCA's $V_{CC}$ lines will be isolated from the lithium source. The next time that power is applied, normal operation will again take place when $V_{CC}$ rises above the $V_{PF}$ threshold, and the LCA's $V_{CC}$ lines will once again be connected to the lithium source when the system is powered down. The timing diagram in Figure 3 illustrates the operation of the SmartSocket in response to the RST input.

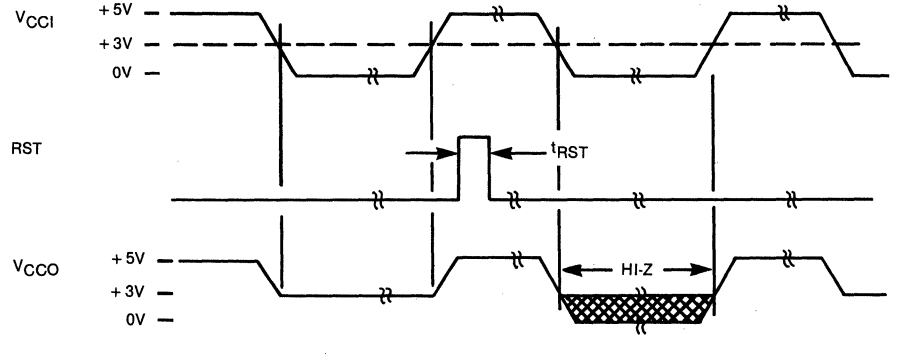
**DATA RETENTION**

The DS1260 SmartBattery is available in three different capacities, including 250, 500 and 1000 maH (milliampere hours). Calculation of the data retention of the LCA(s) in the system with the SmartBattery is simple and straightforward. First, the maximum standby current of the LCA is multiplied times the number of LCAs used in the system. This number is then converted to milliamperes and used to divide into the capacity of the embedded lithium. This gives the data retention time in hours. To convert this number into years, it may be divided by 8760, which is the number of hours in one year.

The worst-case standby current of the Xilinx/MMI XC-2064 is unspecified at the time of this writing, but is said to be around 50 nA by the manufacturer. To be on the safe side, it can be assumed to be 100 nA for the purposes of a design example. Using a DS1260-25 (250 maH) and four LCAs in the system, the calculated data retention time is as follows:

$$\frac{\dfrac{250\ \text{maH}}{4 \times .0001\ \text{mA}}}{8760\ \text{hrs./yr.}} = 71.3\ \text{yrs.}$$

**RESET TIMING** Figure 3



In this example the data retention time is 71.3 years. For most applications, 10 years of data retention in the absence of $V_{CC}$ voltage is more than sufficient to last the life of the product. The maximum amount of current which can be drawn from the 250 maH, 500 maH and 1000 maH versions of the SmartBattery and still provide 10 years of data retention time can be calculated as follows:

$$\frac{250\ \text{maH}}{10\ \text{yrs.} \times 8760\ \text{hrs/yr.}} = .00285\ \text{ma} = 2.85\ u\text{A}$$

$$\frac{500\ \text{maH}}{10\ \text{yrs.} \times 8760\ \text{hrs/yr.}} = .00570\ \text{ma} = 5.70\ u\text{A}$$

$$\frac{1000\ \text{maH}}{10\ \text{yrs.} \times 8760\ \text{hrs/yr.}} = .01140\ \text{ma} = 11.40\ u\text{A}$$

Note that these numbers represent the total amount of data retention capacity available with the SmartBattery when $V_{CC}$ voltage is not present. No lithium power is consumed when system power is applied.

## DS1255 KeyRing Implementation

The DS1255 is a special adaptor designed to interface Dallas Semiconductor DS1204U and DS1207 Electronic Keys to personal computers via the parallel printer port. This mechanism was chosen as the method of interface due to the ease of installation and common parallel printer port availability. Dallas Semiconductor has also developed software which demonstrates how communication is established between the P.C. system and the electronic keys. The complete hardware/software package was developed for electronic key implementation on a 4MHz IBM personal computer. This hardware/software combination may require minor modifications for the various machines and parallel printer port add-on cards available today.

### Hardware - Standard Product

The standard DS1255 KeyRing directs 4 signals from the parallel printer port to the DS 1204U and DS1207 Electronic Keys. Pin 4 of the 25 position D connector, D2 (Data Out 2), provides $\overline{RST}$ for communication with the keys. Pin 5 of the D connector, D3 (Data Out 3), generates the CLK signal providing timing of data in and out of keys. The SLCTIN line (Pin 17) is a bi-directional signal and is used as the data I/O signal for Keys. Finally, Pin 18 of the D connector is signal ground for the KeyRing and Keys. For a more complete understanding of these pins and their function, see the DS1255, DS1204U, and DS1207 data sheets. All of these signals are passed through to the printer except for Pin 17 SLCTIN. Because this is a bi-directional signal, it must be terminated at the KeyRing and not passed on to the printer, in order to avoid contention and/or clamping by the printer.

Note: 1. Manual selection may be necessary on some models of printers if this signal is used by the printer for auto-select.
2. A 180Ω pull down resistor may be placed between pins 17 and 18 at the printer side of the card to select the printer at all times.

Figure 1 depicts the schematic and physical P.C. board design for the DS1255 standard product.

### Hardware - Option

On some non-IBM compatible parallel printer port cards the SLCTIN signal (Pin 17) is not bi-directional. Communication from system to electronic keys must, therefore, be modified. Typically, the SLCTIN pin on these cards is for signaling from the system to the printer only. Therefore, communication to electronic keys from the system is possible, but not from keys to the host system. In this case, Pin 13 of the 25 position D connector (SELECT) is used for data

transmission from keys to the system. As in the standard product, Pin 13 must also be terminated at the electronic key and not passed on to the printer in order to avoid contention and/or signal clamping. This hardware modification can be made very easily as follows:

(1) Disconnect the printer end of Pin 13 by cutting the trace on the DS1255 printed circuit board at the location noted in metal with a hash-mark.

(2) Connect with a jumper wire the two adjacent holes located near the hash-mark above.

Figure 2 depicts the schematic and modification to the physical PC board layout necessary to complete this option.

Note: As with the standard product, if the printer used with this option requires either Pin 17 (SLCTIN) or Pin 13 (SELECT) for auto select, it must be selected manually before operation.

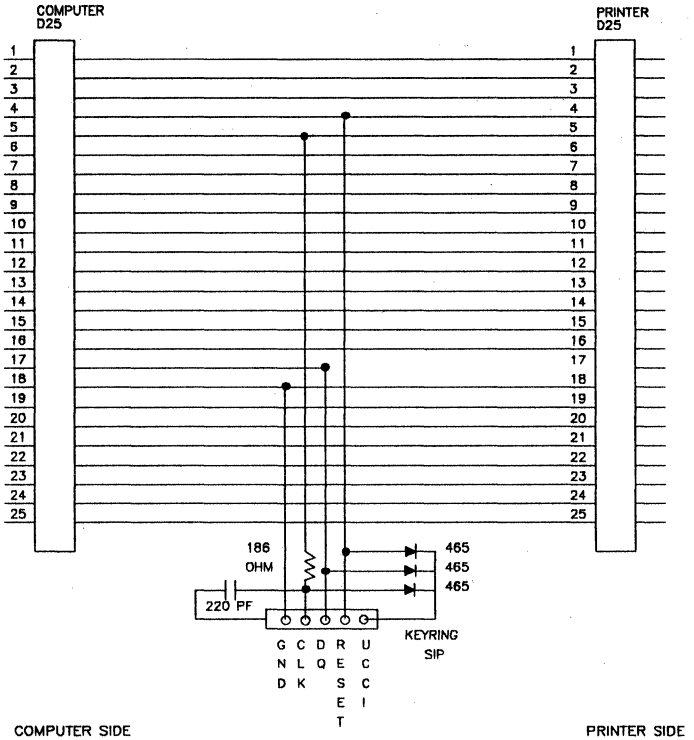
**Hardware - Other Options**

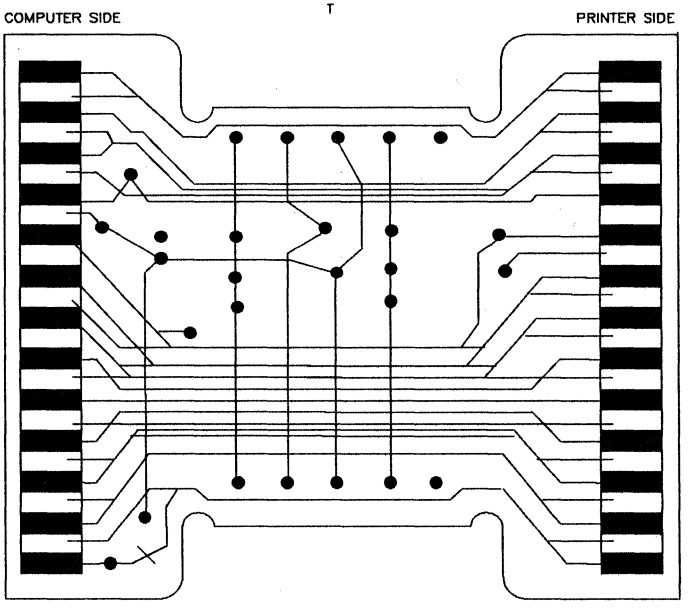
There may be some rare cases where neither the standard product nor the option described above will work. For these uncommon cases and the option described above, the DS1255W should be ordered. The DS1255W is completely assembled as a standard product, but the housing is shipped separately unattached. Thus, any modification to the hardware can quickly be made, and housing reattached.

**Software Options**

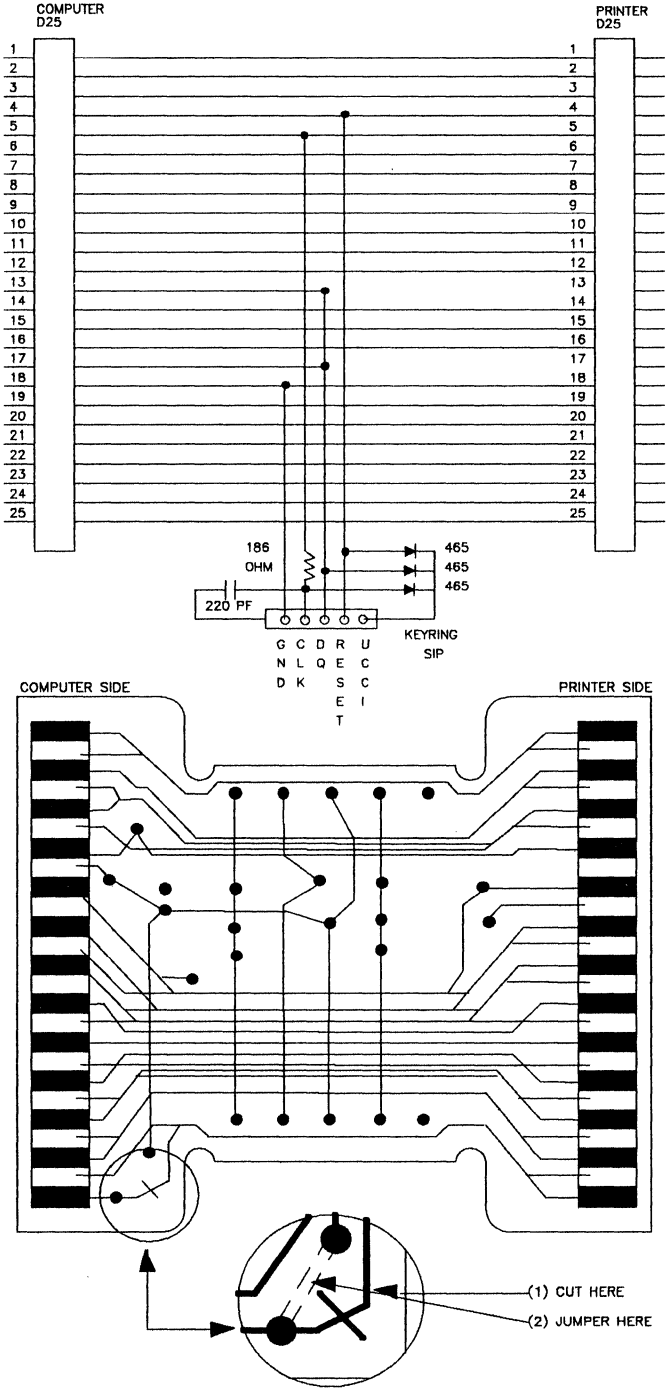
As described above, the software package provided by Dallas Semiconductor has been developed for implementation on a 4 MHz IBM personal computer with the DS1255 standard product. This software package is intended to be used as a demonstration tool as well as a baseline for development. The software should be tailored for a specific end application and must be modified to reflect any hardware option as described above. Also, for personal computers running faster than 4 MHz, some wait states may be necessary within the software due to resistor-capacitor signal (R-C) filtering on the CLK line (Pin 5 of D connector).

## FIGURE 1: STANDARD PRODUCT



## FIGURE 2: HARDWARE OPTION



## DS6010 P.C. Port Implementation

The DS6010 is a unique half-length add-on card for IBM personal computers and compatibles. This card forms the interface between the personal computer expansion bus and Dallas Semiconductor memory cartridges (DS1217M) via a ribbon cable (DS9000) or cartridge clip (DS9020). The software provided with the DS6010 contains drivers and sample configuration files which allow for emulation of floppy disk drives with nonvolatile memory cartridges. This software was developed for use with the MS-DOS operating system on IBM PC/XT/AT and compatible computers. Certain applications may require the use of the nonvolatile memory cartridges in a non-floppy disk emulation format.

## Access With Basic

The DS6010 has been designed such that with minor modifications, DS1217M memory cartridges can be accessed within the "BASIC" programming language on the personal computer. A specific 32K X 8 bit section of the memory map must be allocated for the nonvolatile RAM and SmartWatch on the DS6010 card, and another 32K X 8 bit section of the memory map for the DS1217M cartridge (via DS9000) or cartridges (via DS9020). The function of determining the vacant two sections of 32K X 8 bits is performed automatically under software control by the drivers provided with the standard DS6010 distribution kit. The 32K X 8 bit banks are set with an electronic DIP switch (DS1292) upon power up. For applications requiring access to cartridges in the "BASIC" programming mode, this determination of memory map location can be done with standard 8 position DIP switches (2) rather than the DS1292 Eliminator.

## Hardware Modifications

In order to modify the existing DS6010 hardware, the following must be performed (reference Figure 1):

(1) Remove DS1292 Elilminator from socket (U13)
(2) Solder in place any common 8 position DIP switch (16 pin .300") at locations U6 and U7. Note: Be sure Pin 1 is oriented properly.

## DIP Switch Settings

Any vacant section of memory map may be used for the NVRAM Plus SmartWatch and the DS1217M Cartridge/Cartridge Clip. Selection of memory map location for the NVRAM and SmartWatch is made by setting the DIP switch at U6 with switch number 8 being the most

significant bit. Selection of memory map location for the nonvolatile cartridges is made by setting the DIP switch at U7 with switch number 1 being the most significant bit. Some of the DIP switch settings are not applicable and should be set as described in Table 1. Note that the "off" condition of the switch is a "Logical 1" and the "on" condition is "Logical 0". For explanation purposes, memory map locations "D0XXX" and "D8XXX" are used for the NVRAM Plus SmartWatch and memory cartridges respectively. These are common vacant sections in the memory map and are the default settings when using the standard hardware/software package.

### "BASIC" Access

Access to the NVRAM Plus SmartWatch and the nonvolatile cartridge/cartridge clip may now be accomplished using "Peek" and "Poke" commands from BASIC.

Please review DS1216, DS1217M, and DS9020 data sheets for technical information and access protocol to these devices.

**FIGURE 1**

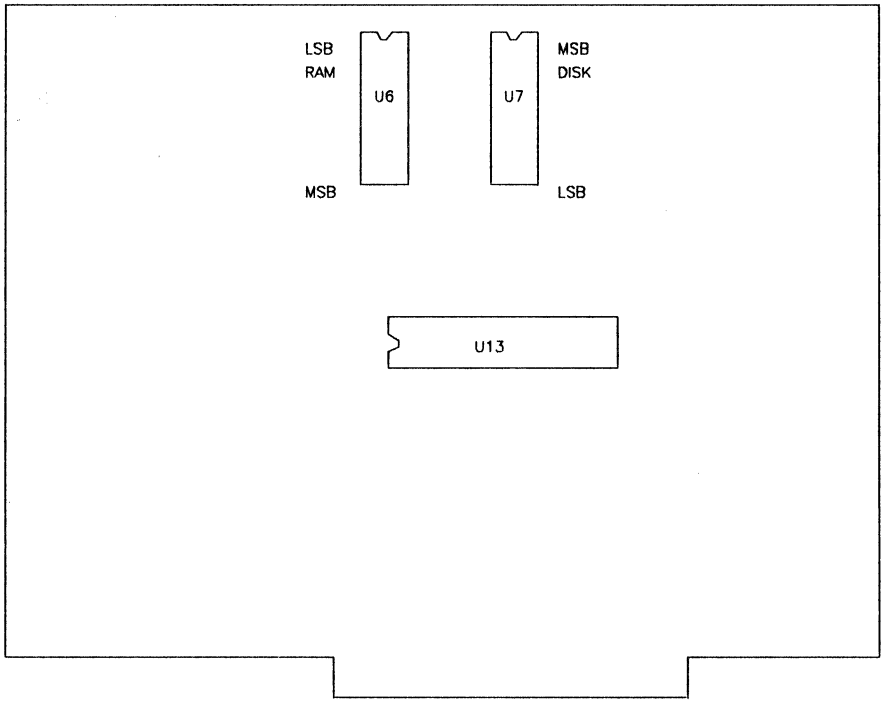


TABLE 1

| DIP SWITCH | SWITCH NUMBER | SETTING | LOGICAL CONDITION | DESCRIPTION | COMMENTS |
|---|---|---|---|---|---|
| U6 NVRAM WATCH DECODE | 1 | OFF | 1 | DECODE ENABLE | MUST BE 1 |
| | 2 | ON | 0 | OPTIONAL ENABLES MUST BE ZERO | FUTURE ADDED FEATURES |
| | 3 | ON | 0 | | |
| | 4 | ON | 0 | LSB A15 | MAY BE ANY UNUSED 32KX8 BIT BANK OF MEMORY MAP |
| | 5 | OFF | 1 | A16 | |
| | 6 | ON | 0 | MAP LOC. DOXXX A17 | |
| | 7 | OFF | 1 | A18 | |
| | 8 | OFF | 1 | MSB A19 | |
| U7 CART-RIDGE DECODE | 1 | OFF | 1 | MSB A19 | MAY BE ANY OTHER UNUSED 32KX8 BIT BANK OF MEMORY MAP |
| | 2 | OFF | 1 | A18 | |
| | 3 | ON | 0 | MAP LOC. D8XXX A17 | |
| | 4 | OFF | 1 | A16 | |
| | 5 | OFF | 1 | LSB A15 | |
| | 6 | | DON'T CARE | CONFIG. LOCK | FOR DS1206/ DS1292 ONLY |
| | 7 | OFF | 1 | DECODE ENABLE | MUST BE 1 |
| | 8 | ON | 0 | WRITE LOCK | MAY BE 1 TO WRITE PROTECT MEMORY |

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