Cyrix® M II™

Mobile CPU
Preliminary Data Sheet

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Cyrix®
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M II™ MOBILE PROCESSOR

Enhanced High Performance CPU

Introduction

♦ Enhanced Sixth-Generation Architecture

- MII-266 and higher
- 64K 4-Way Unified Write-Back Cache
- 2 Level TLB (16 Entry L1, 384 Entry L2)
- Branch Prediction with a 512-entry BTB
- Enhanced Memory Management Unit
- Scratchpad RAM in Unified Cache
- Optimized for both 16- and 32-Bit Code
- High Performance 80-Bit FPU

♦ X86 Instruction Set Includes MMX™ Instructions

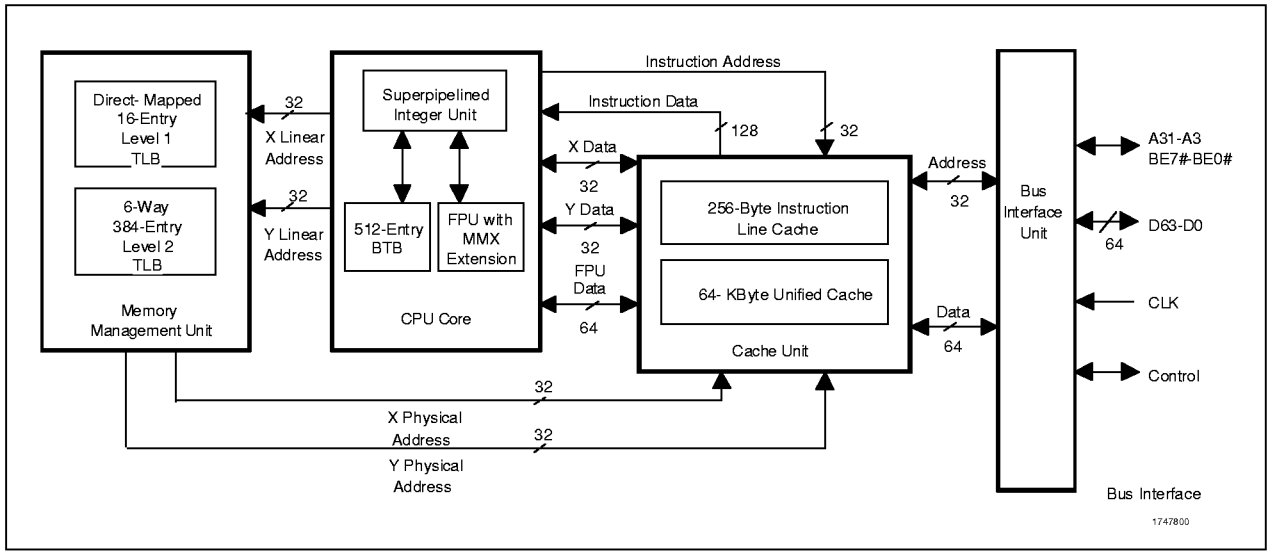
- Compatible with MMX™ Technology
- Runs Windows® 95, Windows 3.x, Windows NT, DOS, UNIX®, OS/2®, Solaris®, and others

♦ Other Features

- Socket 7 Pinout Compatible
- 2.2 V Core, 3.3 V I/O
- Flexible Core/Bus Clock Ratios (2x, 2.5x, 3x, 3.5x, 4x)
- Leverages Existing Socket Infrastructure

The Cyrix M II Mobile CPU™ is an enhanced processor with high speed performance. This processor has a 64K unified write-back cache, a two-level TLB and a 512-entry BTB. The M II CPU contains a scratchpad RAM feature, supports performance monitoring, and allows caching of both SMI code and SMI data. It delivers high 16- and 32-bit performance while running Windows 95, Windows NT, OS/2, DOS, UNIX, and other operating systems.

The M II Mobile CPU achieves top performance through the use of two optimized superpipelined integer units, an on-chip floating point unit, and a 64KByte unified write-back cache. The superpipelined architecture reduces timing constraints and increase frequency scalability. Advanced architectural techniques include register renaming, out-of-order completion, data dependency removal, branch prediction and speculative execution.



PRELIMINARY

November 1998

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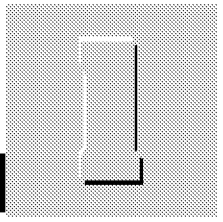

1.0 ELECTRICAL SPECIFICATIONS

1.1 Electrical Connections

This section provides information on electrical connections, absolute maximum ratings, recommended operating conditions, DC characteristics, and AC characteristics. All voltage values in Electrical Specifications are measured with respect to V_{SS} unless otherwise noted.

The M II Mobile CPU operates using two power supply voltages—one for the I/O (3.3 V) and one for the core (2.2 V).

1.1.1 Power and Ground Connections and Decoupling

Testing and operating the M II Mobile CPU requires the use of standard high frequency techniques to reduce parasitic effects. The high clock frequencies used in the M II Mobile CPU and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the V_{CC} and GND pins. The M II Mobile CPU contains 296 pins with 25 pins connected to V_{CC2} (2.2 volts), 28 pins connected to V_{CC3} (3.3 volts), and 53 pins connected to V_{SS} (ground).

1.1.2 Pull-Up/ Pull-Down Resistors

Table 1-1 lists the input pins that are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to V_{CC} and the pull-down resistors are connected to V_{SS}. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted.

Table 1-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	PIN NO.	RESISTOR
BRDYC#	Y3	20-kΩ pull-up
CKMUL0	Y33	20-kΩ pull-down (see text)
CKMUL1	X34	20-kΩ pull-up (see text)
Reserved	AN35	20-kΩ pull-down
Reserved	W35	20-kΩ pull-up
SMI#	AB34	20-kΩ pull-up
SUSP#	Y34	20-kΩ pull-up (see text)
TCK	M34	20-kΩ pull-up
TDI	N35	20-kΩ pull-up
TMS	P34	20-kΩ pull-up
TRST#	Q33	20-kΩ pull-up

1.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 1-1 should be connected either to ground or to V_{CC}. Connect active-high inputs to ground through a 10 kΩ (± 10%) pull-down resistor and active-low inputs to V_{CC} through a 10 kΩ (± 10%) pull-up resistor to prevent possible spurious operation.

1.1.4 NC and Reserved Pins

Pins designated NC have no internal connections. Pins designated RESV or RESERVED should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

1.2 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the M II Mobile CPU processors. Stresses beyond those listed under Table 1-2 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 1-3 (Page 5) is possible. Exposure to conditions beyond Table 1-2 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability.

Table 1-2. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Operating Case Temperature	-65	110	°C	Power Applied
Storage Temperature	-65	150	°C	
Supply Voltage, V_{CC3}	-0.5	4.0	V	
Supply Voltage, V_{CC2}	-0.5	3.3	V	
Voltage On Any Pin	-0.5	V_{CC3} + 0.5	V	Not to exceed Vcc3 max
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

1.3 Recommended Operating Conditions

Table 1-3 presents the recommended operating conditions for the M II Mobile CPU device.

Table 1-3. Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS	NOTES
T_C Operating Case Temperature	0	85	°C	Power Applied
V_{CC3} Supply Voltage (3.3 V)	3.135	3.465	V	
V_{CC2} Supply Voltage (2.2 V)	2.1	2.3	V	
V_{IH} High-Level Input Voltage (except CLK)	2.00	3.55	V	
V_{IH} CLK High-Level Input Voltage	2.0	5.5	V	
V_{IL} Low-Level Input Voltage	-0.3	0.8	V	
I_{OH} High-Level Output Current		-1.0	mA	$V_O=V_{OH(MIN)}$
I_{OL} Low-Level Output Current		5.0	mA	$V_O=V_{OL(MAX)}$

1.4 DC Characteristics

Table 1-4. DC Characteristics (at Recommended Operating Conditions) 1 of 2

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{OL} Low-Level Output Voltage			0.4	V	I_{OL} = 5 mA
V_{OH} High-Level Output Voltage	2.4			V	I_{OH} = -1 mA
I_I Input Leakage Current For all pins (except those listed in Table 4-1).			±15	µA	$0 < V_{IN} < V_{CC3}$ Note 1
I_{IH} Input Leakage Current For all pins with internal pull-downs.			200	µA	V_{IH} = 2.4 V Note 1
I_{IL} Input Leakage Current For all pins with internal pull-ups.			-400	µA	V_{IL} = 0.45 V Note 1
C_{IN} Input Capacitance			15	pF	f = 1 MHz*
C_{OUT} Output Capacitance			20	pF	f = 1 MHz*
C_{IO} I/O Capacitance			25	pF	f = 1 MHz*
C_{CLK} CLK Capacitance			15	pF	f = 1 MHz*

*Note: Not 100% tested.

Table 1-5. DC Characteristics (at Recommended Operating Conditions) 2 of 2

PARAMETER	ICC2 MAX	ICC3 MAX	UNITS	NOTES
I_{CC} Active I_{CC}			mA	
200 MHz (MII-266)	4560	100		Notes 1, 2
233 MHz (MII-300)	5040	100		Notes 1, 2
266 MHz (MII-333)	5650	100		Notes 1, 2
270 MHz (MII-350)	5760	100		Notes 1, 2, 5
I_{CCSM} Suspend Mode Power Dissipation				
200 MHz (MII-266)	54	100	mA	Notes 1, 2, 3
233 MHz (MII-300)	54	100		Notes 1, 2, 3
266 MHz (MII-333)	54	100		Notes 1, 2, 3
270 MHz (MII-350)	54	100		Notes 1, 2, 3, 5
I_{CCSS} Standby I_{CC}				
0 MHz (Suspended/CLK Stopped)	30	50.0	mA	Notes 1, 2, 4

Notes:
1. These values should be used for power supply design. Maximum I_{CC} is determined using the worst-case instruction sequences and functions at maximum Vcc.
2. Frequency (MHz) ratings refer to the internal clock frequency.
3. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA).
4. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).
5. Measured using 90 MHz bus.

Table 1-6. Power Dissipation

PARAMETER	POWER		UNITS	NOTES
	TYP	MAX		
Active Power Dissipation				
200 MHz (MII-266)		10.3	W	Note 1
233 MHz (MII-300)		11.4		Note 1
266 MHz (MII-333)		12.7		Note 1
270 MHz (MII-350)		13.0		Note 1
Suspend Mode Power Dissipation				
200 MHz (MII-266)		0.152	W	Notes 1, 2
233 MHz (MII-300)		0.154		Notes 1, 2
266 MHz (MII-333)		0.156		Notes 1, 2
270 MHz (MII-350)		0.159		Notes 1, 2
Standby Mode Power Dissipation				
0 MHz (Suspended/CLK Stopped)		0.070	W	Notes 1, 3

Notes:
1. Systems must be designed to thermally dissipate the maximum active power dissipation. Maximum power is determined using the worst-case instruction sequences and functions with Vcc2 = 2.2 V and Vcc3 = 3.3 V.
2. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA).
3. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).

1.5 AC Characteristics

Tables 1-7 through 1-12 (Pages 9 through 13) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 1-5 (Page 8) and Figure 1-5 (Page 9). The rising clock edge reference level V_{REF} and other reference levels are shown in Table 1-7. Input or output signals must cross these levels during testing.

Figure 1-5 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

The JTAG AC timing is shown in Table 1-13 (Page 15) supported by Figures 1-6 (Page 15) though 1-8 (Page 16).

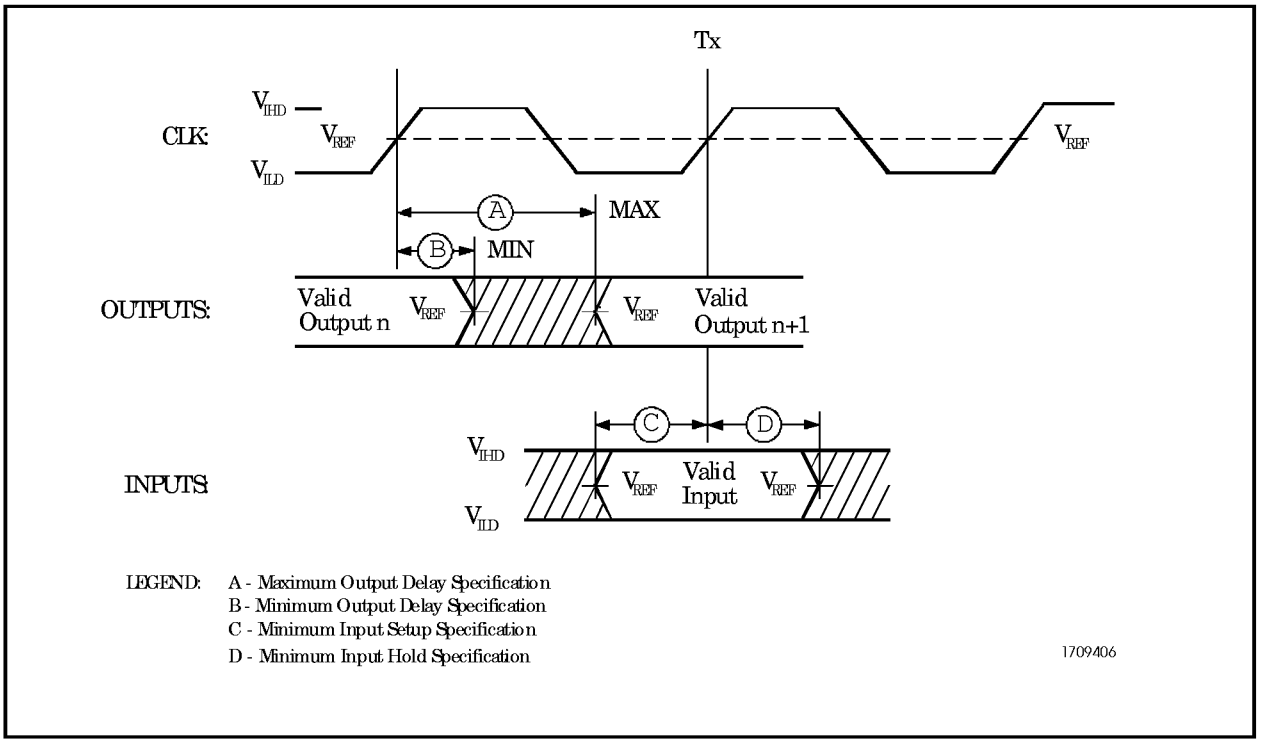

Figure 1-5. Drive Level and Measurement Points for Switching Characteristics

Table 1-7. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	VOLTAGE (Volts)
V_{REF}	1.5
V_{IHD}	2.3
V_{ILD}	0

Note: Refer to Figure 4-1.

Table 1-8. Clock Specifications

T_{CASE} = 0°C to 85°C, See Figure 4-2

	PARAMETER	60-MHz BUS		66-MHz BUS		75-MHz BUS		83-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f	CLK Frequency		60		66.6		75		83	MHz
T1	CLK Period	16.67		15.0		13.33		12.0		ns
T2	CLK Period Stability		±250		±250		±250		±250	ps
T3	CLK High Time	4.0		4.0		4.0		4.0		ns
T4	CLK Low Time	4.0		4.0		4.0		4.0		ns
T5	CLK Fall Time	0.15	1.5	0.15	1.5	0.15	1.5	0.15	1.5	ns
T6	CLK Rise Time	0.15	1.5	0.15	1.5	0.15	1.5	0.15	1.5	ns

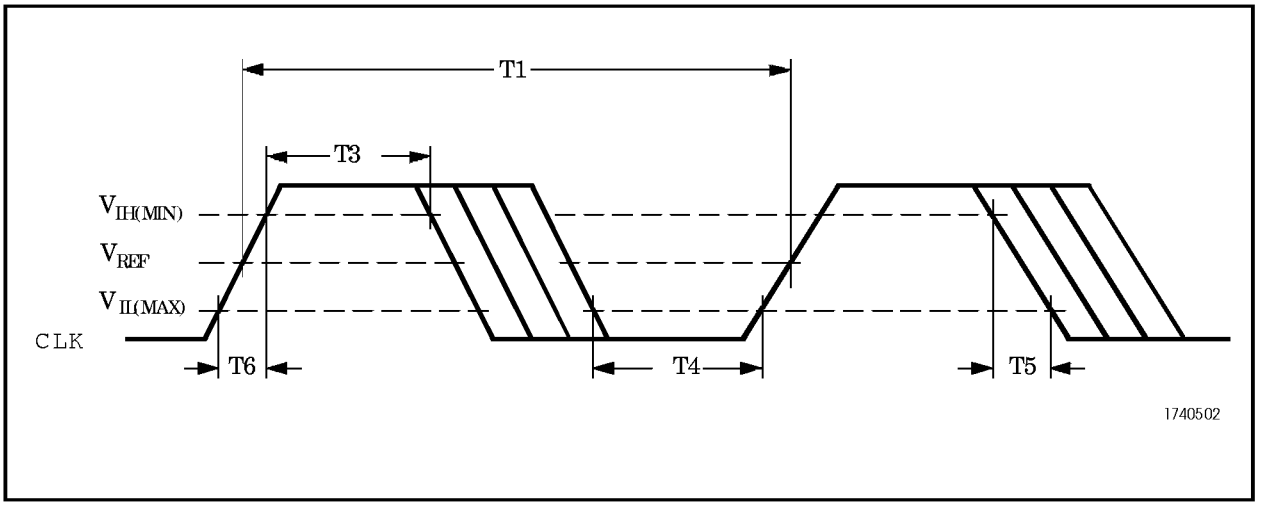

Figure 1-5 CLK Timing and Measurement Points

Table 1-9. Output Valid Delays
C_L = 50 pF, T_{case} = 0°C to 85°C, See Figure 4-3

	PARAMETER	60-MHz BUS		66-MHz BUS		75-MHz BUS		83-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T7a	A31-A3	1.0	7.0	1.0	6.3	1.0	6.3	1.0	5.7	ns
T7b	BE7#-BE0#, CACHE#, D/C#, LOCK#, PCD, PWT, SCYC, SMIACT#, W/R#	1.0	7.0	1.0	7.0	1.0	7.0	1.0	6.0	ns
T7c	ADS#	1.0	7.0	1.0	6.0	1.0	6.0	1.0	5.5	ns
T7d	M/IO#	1.0	7.0	1.0	5.9	1.0	5.9	1.0	5.5	ns
T8	ADSC#	1.0	7.0	1.0	7.0	1.0	7.0	1.0	6.5	ns
T9	AP	1.0	8.5	1.0	8.5	1.0	8.5	1.0	7.5	ns
T10	APCHK#, PCHK#, FERR#	1.0	8.3	1.0	7.0	1.0	7.0	1.0	6.5	ns
T11	D63-D0, DP7-DP0 (Write)	1.3	7.5	1.3	7.5	1.3	7.5	1.3	7.0	ns
T12a	HIT#	1.0	8.0	1.0	6.8	1.0	6.8	1.0	6.0	ns
T12b	HITM#	1.1	6.0	1.1	6.0	1.1	6.0	1.1	5.5	ns
T13a	BREQ	1.0	8.0	1.0	8.0	1.0	8.0	1.0	7.0	ns
T13b	HLDA	1.0	8.0	1.0	6.8	1.0	6.8	1.0	6.0	ns
T14	SUSPA#	1.0	8.0	1.0	8.0	1.0	8.0	1.0	7.0	ns

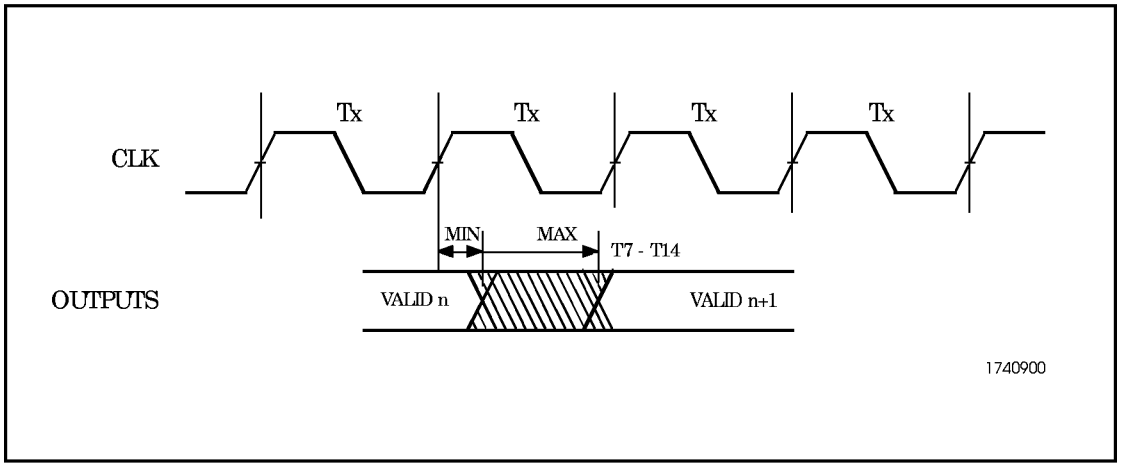

Figure 1-5. Output Float Delay Timing

Table 1-10. Output Float Delays
C_L = 50 pF, T_{case} = 0°C to 85°C, See Figure 4-5

	PARAMETER	60-MHz BUS		66-MHz BUS		75-MHz BUS		83-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T15	A31-A3, ADS#, BE7#-BE0#, CACHE#, D/C#, LOCK#, PCD, PWT, SCYC, SMIACT#, W/R#		10.0		10.0		10.0		10.0	ns
T16	AP		10.0		10.0		10.0		10.0	ns
T17	D63-D0, DP7-DP0 (Write)		10.0		10.0		10.0		10.0	ns

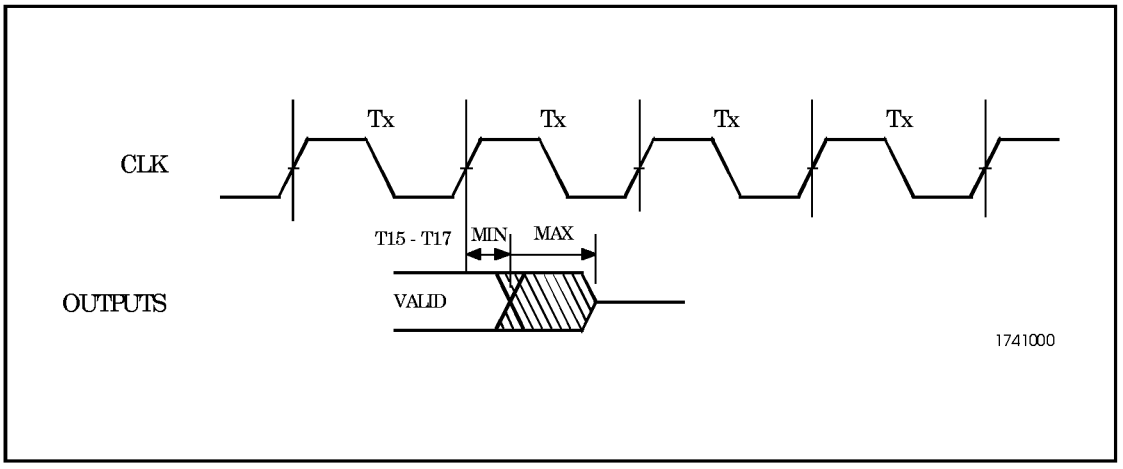

Figure 1-5. Output Float Delay Timing

Table 1-11. Input Setup Times

T_{case} = 0°C to 85°C, See Figure 4-5

	PARAMETER	60-MHz BUS	66-MHz BUS	75-MHz BUS	83-MHz BUS	UNITS
		MIN	MIN	MIN	MIN	
T18a	A20M#	5.0	5.0	3.3	3.0	ns
T18b	FLUSH#, IGNNE#, SUSP#	5.0	5.0	3.3	3.0	ns
T19c	AHOLD, BOFF#	5.0	5.0	3.3	3.0	ns
T19	HOLD	5.0	5.0	3.3	3.0	ns
T20	BRDY#	5.0	5.0	3.3	3.0	ns
T21	BRDYC#	5.0	5.0	3.3	3.0	ns
T22a	A31-A3, AP, BE7#-BE0#,	5.0	5.0	3.3	3.0	ns
T22b	AP	5.0	5.0	3.3	3.0	ns
T22c	D63-D0 (Read), DP7-DP0 (Read)	3.0	3.0	3.0	2.7	ns
T23a	EADS#	5.0	5.0	5.0	4.5	ns
T23b	INV	5.0	5.0	5.0	4.5	ns
T24	INTR, NMI, RESET, SMI#, WM_RST	5.0	5.0	5.0	4.5	ns
T25a	EWBE#, NA#, WB/WT#	4.5	4.5	3.0	2.7	ns
T25b	KEN#	4.5	4.5	3.0	2.7	ns

Table 1-12. Input Hold Times

T_{case} = 0°C to 85°C, See Figure 4-5

SYMBOL	PARAMETER	60-MHz BUS	66-MHz BUS	75-MHz BUS	83-MHz BUS	UNITS
		MIN	MIN	MIN	MIN	
T27	A20M#, FLUSH#, IGNNE#, SUSP#	1.0	1.0	1.0	1.0	ns
T28a	AHOLD, BOFF#	1.0	1.0	1.0	1.0	ns
T28b	HOLD	1.0	1.0	1.0	1.0	ns
T29	BRDY#	1.0	1.0	1.0	1.0	ns
T30	BRDYC#	1.0	1.0	1.0	1.0	ns
T31a	A31-A3, AP, BE7#-BE0#,	1.0	1.0	1.0	1.0	ns
T31b	AP	1.0	1.0	1.0	1.0	ns
T31c	D63-D0 (Read), DP7-DP0 (Read)	2.0	1.5	1.5	1.5	ns
T32	EADS#, INV	1.0	1.0	1.0	1.0	ns
T33	INTR, NMI, RESET, SMI#, WM_RST	1.0	1.0	1.0	1.0	ns
T34	EWBE#, KEN#, NA#, WB/WT#	1.0	1.0	1.0	1.0	ns

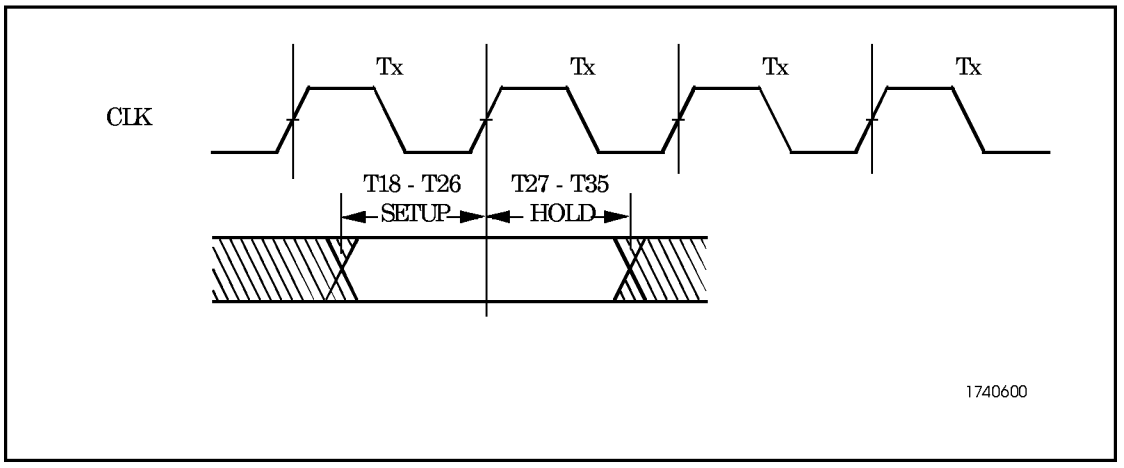

Figure 1-5. Input Setup and Hold Timing

Table 1-13. JTAG AC Specifications

SYMBOL	PARAMETER	ALL BUS FREQUENCIES		UNITS	FIGURE
		MIN	MAX		
	TCK Frequency		20	MHz	
T36	TCK Period	50		ns	4-6
T37	TCK High Time	25		ns	4-6
T38	TCK Low Time	25		ns	4-6
T39	TCK Rise Time		5	ns	4-6
T40	TCK Fall Time		5	ns	4-6
T41	TDO Valid Delay	3	20	ns	4-7
T42	Non-test Outputs Valid Delay	3	20	ns	4-7
T43	TDO Float Delay		25	ns	4-7
T44	Non-test Outputs Float Delay		25	ns	4-7
T45	TRST# Pulse Width	40		ns	4-8
T46	TDI, TMS Setup Time	20		ns	4-7
T47	Non-test Inputs Setup Time	20		ns	4-7
T48	TDI, TMS Hold Time	13		ns	4-7
T49	Non-test Inputs Hold Time	13		ns	4-7

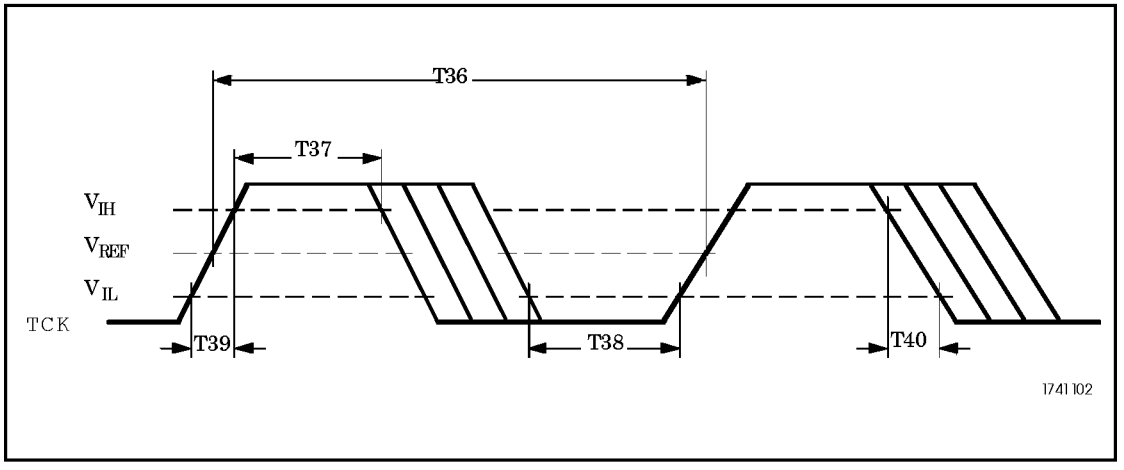

Figure 1-5. TCK Timing and Measurement Points

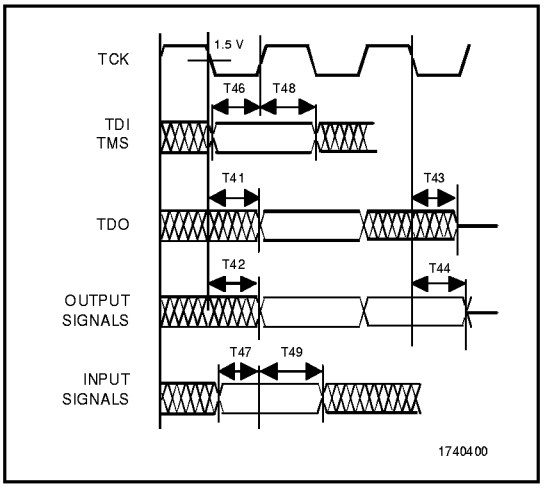

Figure 1-5. JTAG Test Timings

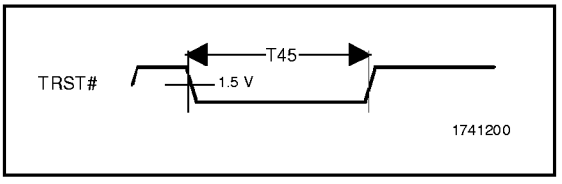

Figure 1-5. Test Reset Timing

2.0 MECHANICAL SPECIFICATIONS

2.1 296-Pin SPGA Package

The pin assignments for the M II Mobile CPU in a 296-pin SPGA package are shown in Figure 2-1. The pins are listed by signal name in Table 2-1(Page 17) and by pin number in Table 2-2 (Page 18). Dimensions are shown in Figure 2-2 (Page 20) and Table 2-3 (Page 21).

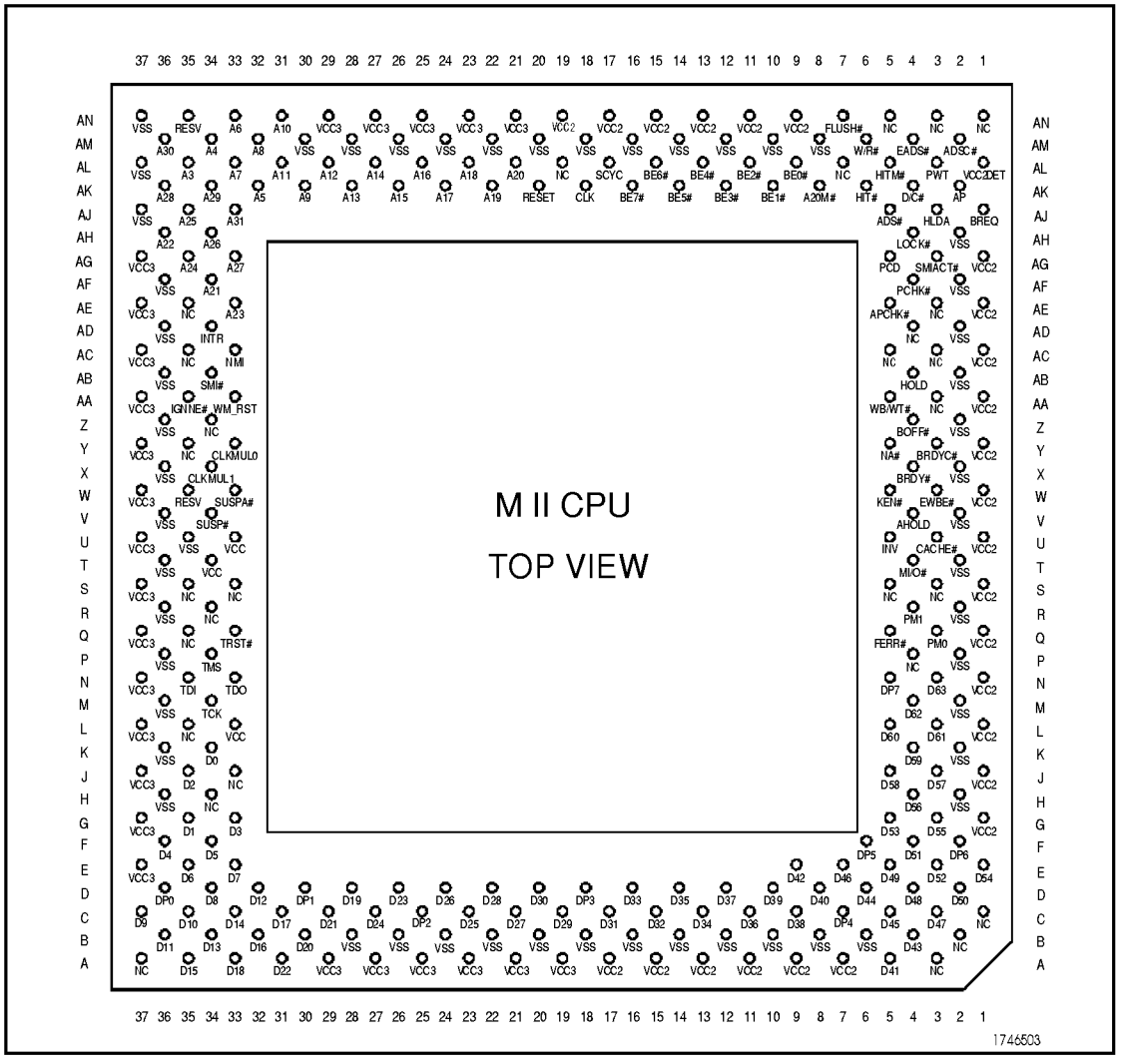

Figure 2-1. 296-Pin SPGA Package Pin Assignments

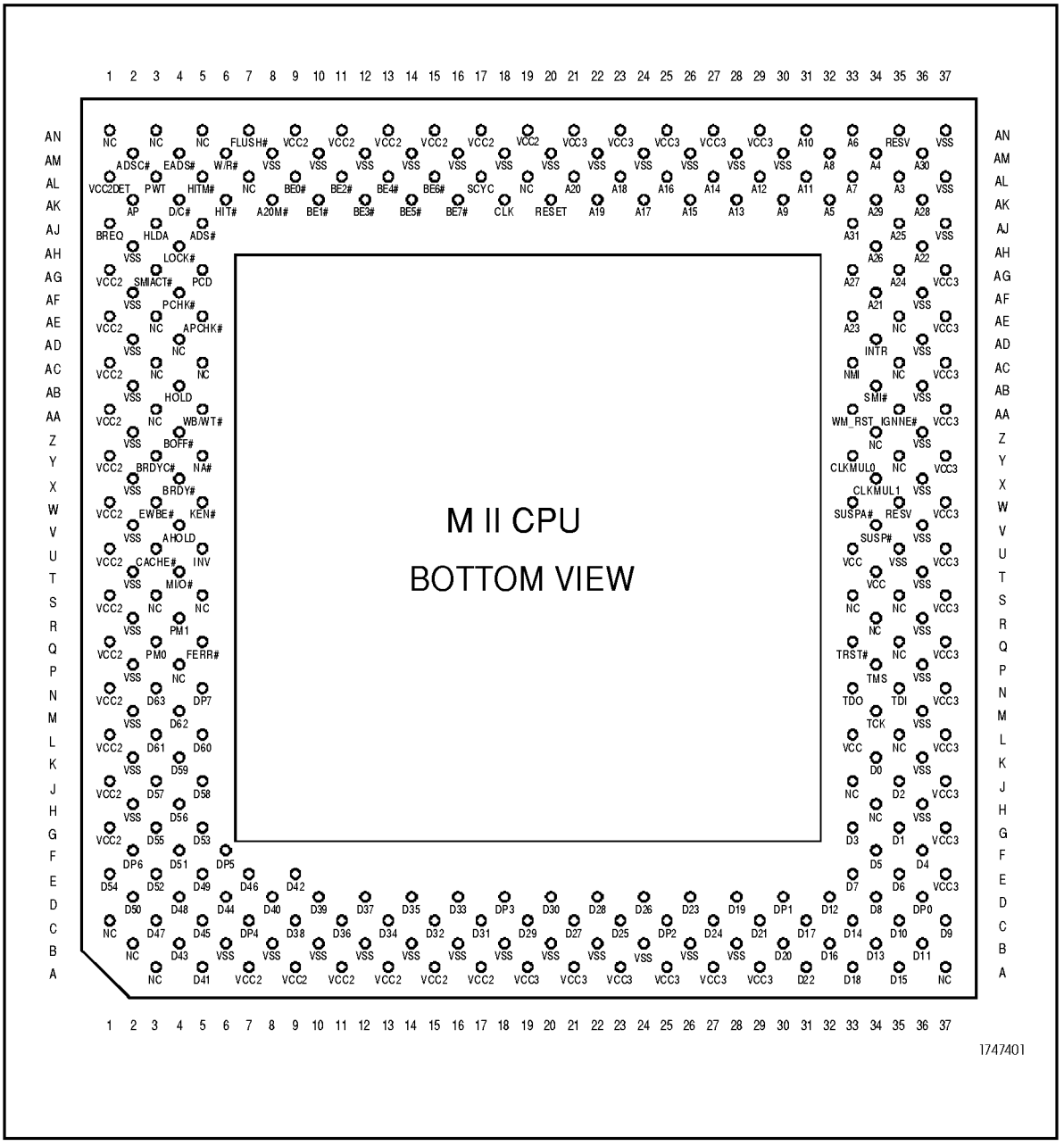

Figure 2-2. 296-Pin SPGA Package Pin Assignments (Bottom View)

Table 2-1. 296-Pin SPGA Package Signal Names Sorted by Pin Number

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A3	NC	C29	D21	J35	D2	U35	Vss	AE35	NC	AL21	A20
A5	D41	C31	D17	J37	Vcc3	U37	Vcc3	AE37	Vcc3	AL23	A18
A7	Vcc2	C33	D14	K2	Vss	V2	Vss	AF2	Vss	AL25	A16
A9	Vcc2	C35	D10	K4	D59	V4	AHOLD	AF4	PCHK#	AL27	A14
A11	Vcc2	C37	D9	K34	D0	V34	SUSP#	AF34	A21	AL29	A12
A13	Vcc2	D2	D50	K36	Vss	V36	Vss	AF36	Vss	AL31	A11
A15	Vcc2	D4	D48	L1	Vcc2	W1	Vcc2	AG1	Vcc2	AL33	A7
A17	Vcc2	D6	D44	L3	D61	W3	EWBE#	AG3	SMIACT#	AL35	A3
A19	Vcc3	D8	D40	L5	D60	W5	KEN#	AG5	PCD	AL37	Vss
A21	Vcc3	D10	D39	L33	Vcc3	W33	SUSPA#	AG33	A27	AM2	ADSC#
A23	Vcc3	D12	D37	L35	NC	W35	Reserved	AG35	A24	AM4	EADS#
A25	Vcc3	D14	D35	L37	Vcc3	W37	Vcc3	AG37	Vcc3	AM6	W/R#
A27	Vcc3	D16	D33	M2	Vss	X2	Vss	AH2	Vss	AM8	Vss
A29	Vcc3	D18	DP3	M4	D62	X4	BRDY#	AH4	LOCK#	AM10	Vss
A31	D22	D20	D30	M34	TCK	X34	CLKMUL1	AH34	A26	AM12	Vss
A33	D18	D22	D28	M36	Vss	X36	Vss	AH36	A22	AM14	Vss
A35	D15	D24	D26	N1	Vcc2	Y1	Vcc2	AJ1	BREQ	AM16	Vss
A37	NC	D26	D23	N3	D63	Y3	BRDYC#	AJ3	HLDA	AM18	Vss
B2	NC	D28	D19	N5	DP7	Y5	NA#	AJ5	ADS#	AM20	Vss
B4	D43	D30	DP1	N33	TDO	Y33	CLKMUL0	AJ33	A31	AM22	Vss
B6	Vss	D32	D12	N35	TDI	Y35	NC	AJ35	A25	AM24	Vss
B8	Vss	D34	D8	N37	Vcc3	Y37	Vcc3	AJ37	Vss	AM26	Vss
B10	Vss	D36	DP0	P2	Vss	Z2	Vss	AK2	AP	AM28	Vss
B12	Vss	E1	D54	P4	NC	Z4	BOFF#	AK4	D/C#	AM30	Vss
B14	Vss	E3	D52	P34	TMS	Z34	NC	AK6	HIT#	AM32	A8
B16	Vss	E5	D49	P36	Vss	Z36	Vss	AK8	A20M#	AM34	A4
B18	Vss	E7	D46	Q1	Vcc2	AA1	Vcc2	AK10	BE1#	AM36	A30
B20	Vss	E9	D42	Q3	PM0	AA3	NC	AK12	BE3#	AN1	NC
B22	Vss	E33	D7	Q5	FERR#	AA5	WB/WT#	AK14	BE5#	AN3	NC
B24	Vss	E35	D6	Q33	TRST#	AA33	WM_RST	AK16	BE7#	AN5	NC
B26	Vss	E37	Vcc3	Q35	NC	AA35	IGNNE#	AK18	CLK	AN7	FLUSH#
B28	Vss	F2	DP6	Q37	Vcc3	AA37	Vcc3	AK20	RESET	AN9	Vcc2
B30	D20	F4	D51	R2	Vss	AB2	Vss	AK22	A19	AN11	Vcc2
B32	D16	F6	DP5	R4	PM1	AB4	HOLD	AK24	A17	AN13	Vcc2
B34	D13	F34	D5	R34	NC	AB34	SMI#	AK26	A15	AN15	Vcc2
B36	D11	F36	D4	R36	Vss	AB36	Vss	AK28	A13	AN17	Vcc2
C1	NC	G1	Vcc2	S1	Vcc2	AC1	Vcc2	AK30	A9	AN19	Vcc2
C3	D47	G3	D55	S3	NC	AC3	NC	AK32	A5	AN21	Vcc3
C5	D45	G5	D53	S5	NC	AC5	NC	AK34	A29	AN23	Vcc3
C7	DP4	G33	D3	S33	NC	AC33	NMI	AK36	A28	AN25	Vcc3
C9	D38	G35	D1	S35	NC	AC35	NC	AL1	Vcc2DET	AN27	Vcc3
C11	D36	G37	Vcc3	S37	Vcc3	AC37	Vcc3	AL3	PWT	AN29	Vcc3
C13	D34	H2	Vss	T2	Vss	AD2	Vss	AL5	HITM#	AN31	A10
C15	D32	H4	D56	T4	MI/O#	AD4	NC	AL7	NC	AN33	A6
C17	D31	H34	NC	T34	Vcc3	AD34	INTR	AL9	BE0#	AN35	Reserved
C19	D29	H36	Vss	T36	Vss	AD36	Vss	AL11	BE2#	AN37	Vss
C21	D27	J1	Vcc2	U1	Vcc2	AE1	Vcc2	AL13	BE4#		
C23	D25	J3	D57	U3	CACHE#	AE3	NC	AL15	BE6#		
C25	DP2	J5	D58	U5	INV	AE5	APCHK#	AL17	SCYC		
C27	D24	J33	NC	U33	Vcc3	AE33	A23	AL19	NC		

Table 2-2. 296-Pin SPGA Package Signal Names Sorted by Signal Names

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A3	AL35	CLKMUL1	X34	D48	D4	NC	S5	Vcc2	Y1	Vss	B26
A4	AM34	D/C#	AK4	D49	E5	NC	S33	Vcc2	AA1	Vss	B28
A5	AK32	D0	K34	D50	D2	NC	S35	Vcc2	AC1	Vss	H2
A6	AN33	D1	G35	D51	F4	NC	Y35	Vcc2	AE1	Vss	H36
A7	AL33	D2	J35	D52	E3	NC	Z34	Vcc2	AG1	Vss	K2
A8	AM32	D3	G33	D53	G5	NC	AA3	Vcc2	AN9	Vss	K36
A9	AK30	D4	F36	D54	E1	NC	AC3	Vcc2	AN11	Vss	M2
A10	AN31	D5	F34	D55	G3	NC	AC5	Vcc2	AN13	Vss	M36
A11	AL31	D6	E35	D56	H4	NC	AC35	Vcc2	AN15	Vss	P2
A12	AL29	D7	E33	D57	J3	NC	AD4	Vcc2	AN17	Vss	P36
A13	AK28	D8	D34	D58	J5	NC	AE3	Vcc2	AN19	Vss	R2
A14	AL27	D9	C37	D59	K4	NC	AE35	Vcc3	A19	Vss	R36
A15	AK26	D10	C35	D60	L5	NC	AL7	Vcc3	A21	Vss	T2
A16	AL25	D11	B36	D61	L3	NC	AL19	Vcc3	A23	Vss	T36
A17	AK24	D12	D32	D62	M4	NC	AN1	Vcc3	A25	Vss	U35
A18	AL23	D13	B34	D63	N3	NC	AN3	Vcc3	A27	Vss	V2
A19	AK22	D14	C33	DP0	D36	NC	AN5	Vcc3	A29	Vss	V36
A20	AL21	D15	A35	DP1	D30	NMI	AC33	Vcc3	E37	Vss	X2
A20M#	AK8	D16	B32	DP2	C25	PCD	AG5	Vcc3	G37	Vss	X36
A21	AF34	D17	C31	DP3	D18	PCHK#	AF4	Vcc3	J37	Vss	Z2
A22	AH36	D18	A33	DP4	C7	PM0	Q3	Vcc3	L33	Vss	Z36
A23	AE33	D19	D28	DP5	F6	PM1	R4	Vcc3	L37	Vss	AB2
A24	AG35	D20	B30	DP6	F2	PWT	AL3	Vcc3	N37	Vss	AB36
A25	AJ35	D21	C29	DP7	N5	Reserved	W35	Vcc3	Q37	Vss	AD2
A26	AH34	D22	A31	EADS#	AM4	Reserved	AN35	Vcc3	S37	Vss	AD36
A27	AG33	D23	D26	EWBE#	W3	RESET	AK20	Vcc3	T34	Vss	AF2
A28	AK36	D24	C27	FERR#	Q5	SCYC	AL17	Vcc3	U33	Vss	AF36
A29	AK34	D25	C23	FLUSH#	AN7	SMI#	AB34	Vcc3	U37	Vss	AH2
A30	AM36	D26	D24	HIT#	AK6	SMIACT#	AG3	Vcc3	W37	Vss	AJ37
A31	AJ33	D27	C21	HITM#	AL5	SUSP#	V34	Vcc3	Y37	Vss	AL37
ADS#	AJ5	D28	D22	HLDA	AJ3	SUSPA#	W33	Vcc3	AA37	Vss	AM8
ADSC#	AM2	D29	C19	HOLD	AB4	TCK	M34	Vcc3	AC37	Vss	AM10
AHOLD	V4	D30	D20	IGNNE#	AA35	TDI	N35	Vcc3	AE37	Vss	AM12
AP	AK2	D31	C17	INTR	AD34	TDO	N33	Vcc3	AG37	Vss	AM14
APCHK#	AE5	D32	C15	INV	U5	TMS	P34	Vcc3	AN21	Vss	AM16
BE0#	AL9	D33	D16	KEN#	W5	TRST#	Q33	Vcc3	AN23	Vss	AM18
BE1#	AK10	D34	C13	LOCK#	AH4	Vcc2	A7	Vcc3	AN25	Vss	AM20
BE2#	AL11	D35	D14	MI/O#	T4	Vcc2	A9	Vcc3	AN27	Vss	AM22
BE3#	AK12	D36	C11	NA#	Y5	Vcc2	A11	Vcc3	AN29	Vss	AM24
BE4#	AL13	D37	D12	NC	A3	Vcc2	A13	Vcc2DET	AL1	Vss	AM26
BE5#	AK14	D38	C9	NC	A37	Vcc2	A15	Vss	B6	Vss	AM28
BE6#	AL15	D39	D10	NC	B2	Vcc2	A17	Vss	B8	Vss	AM30
BE7#	AK16	D40	D8	NC	C1	Vcc2	G1	Vss	B10	Vss	AN37
BOFF#	Z4	D41	A5	NC	H34	Vcc2	J1	Vss	B12	W/R#	AM6
BRDY#	X4	D42	E9	NC	J33	Vcc2	L1	Vss	B14	WB/WT#	AA5
BRDYC#	Y3	D43	B4	NC	L35	Vcc2	N1	Vss	B16	WM_RST	AA33
BREQ	AJ1	D44	D6	NC	P4	Vcc2	Q1	Vss	B18		
CACHE#	U3	D45	C5	NC	Q35	Vcc2	S1	Vss	B20		
CLK	AK18	D46	E7	NC	R34	Vcc2	U1	Vss	B22		
CLKMUL0	Y33	D47	C3	NC	S3	Vcc2	W1	Vss	B24		

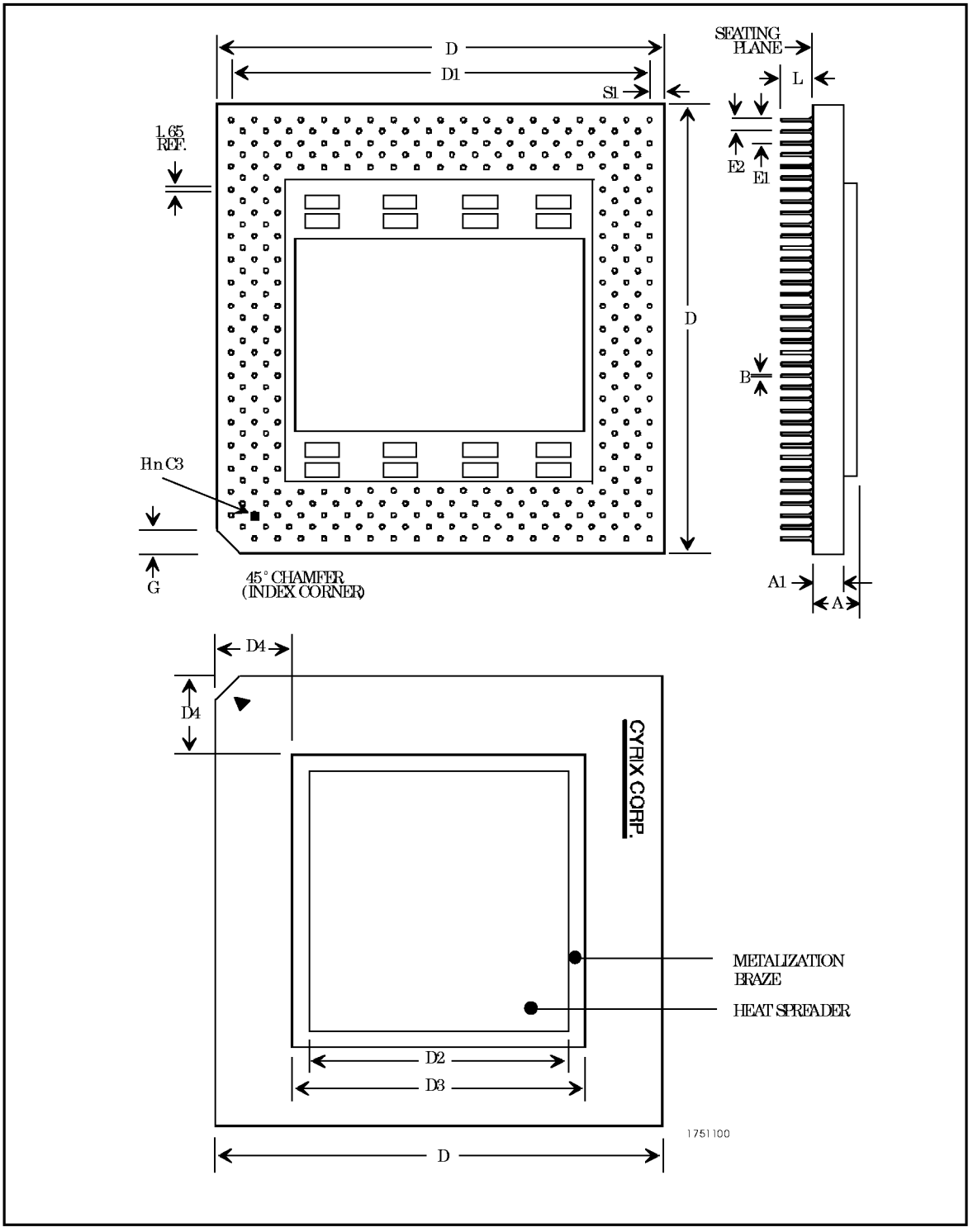

Figure 2-3. 296-Pin SPGA Package A

Table 2-3. 296-Pin SPGA Package A

SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.43	4.34	0.135	0.171
A1	2.51	3.07	0.099	0.121
B	0.43	0.51	0.017	0.020
D	49.28	49.91	1.940	1.965
D1	45.47	45.97	1.790	1.810
D2	31.37 Sq.	32.13 Sq.	1.235	1.265
D3	33.43	34.42	1.316	1.355
D4	7.49	6.71	0.295	0.264
E1	2.41	2.67	0.095	0.105
E2	1.14	1.40	0.045	0.055
G	1.52	2.29	0.060	0.090
L	2.97	3.38	0.117	0.133
S1	1.65	2.16	0.065	0.085

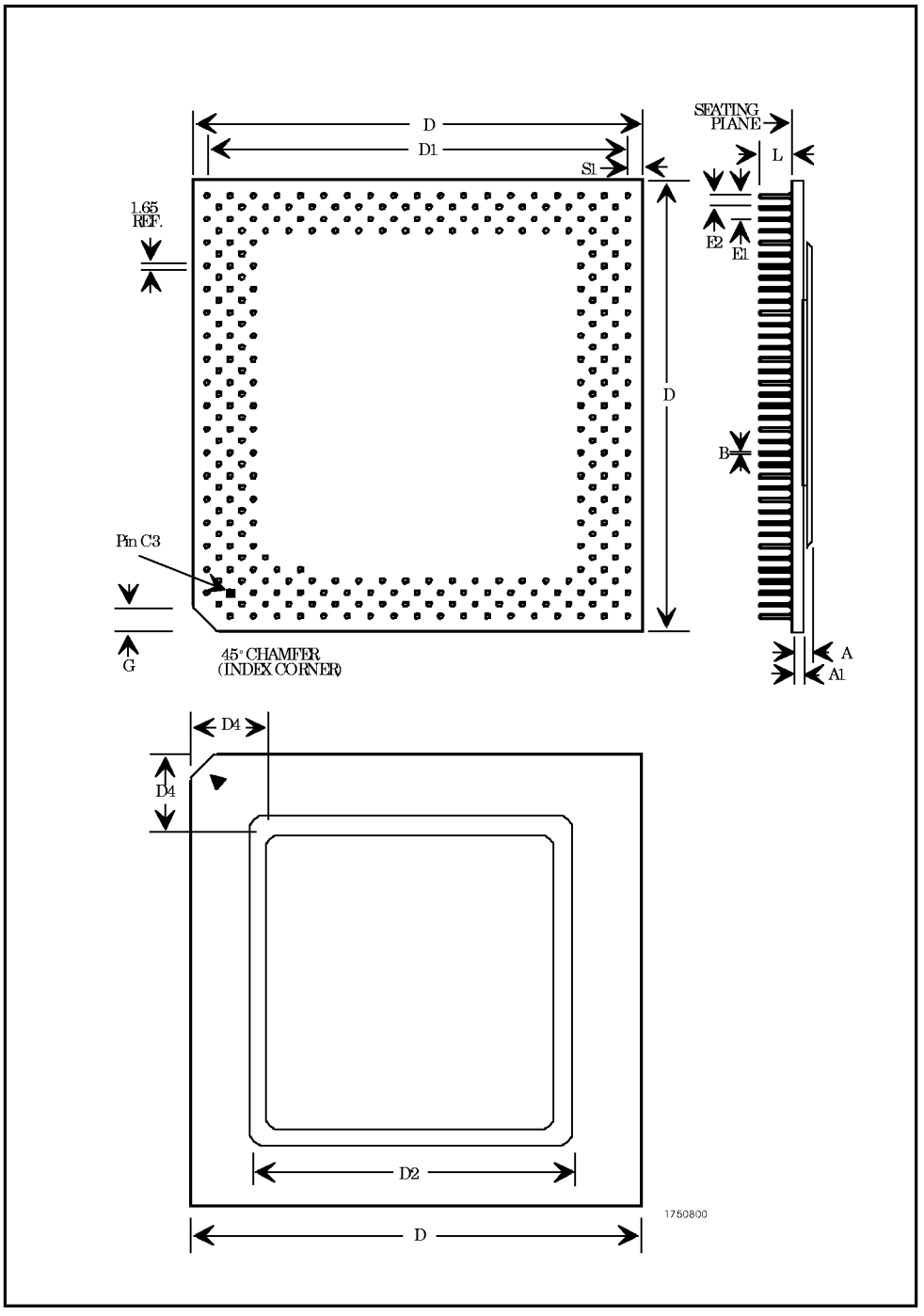

Figure 2-4. 296-Pin "Flip Chip SPGA Package B

Table 2-4. 296-Pin "Flip Chip" SPGA Package B Dimensions

SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.80	4.50	0.150	0.177
A1	1.62	1.98	0.064	0.078
B	0.43	0.51	0.017	0.020
D	49.28	49.91	1.940	1.965
D1	45.47	45.97	1.790	1.810
D2	36.75 Sq.	37.25 Sq.	1.447	1.467
E1	2.41	2.67	0.095	0.105
E2	1.14	1.40	0.045	0.055
G	1.52	2.29	0.060	0.090
L	2.97	3.38	0.117	0.133
S1	1.65	2.16	0.065	0.085

2.2 Thermal Resistances

Three thermal resistances can be used to idealize the heat flow from the junction of the M II Mobile CPU to ambient:

θ_{JC} = thermal resistance from junction to case in °C/W

θ_{CS} = thermal resistance from case to heatsink in °C/W,

θ_{SA} = thermal resistance from heatsink to ambient in °C/W,

$\theta_{CA} = \theta_{CS} + \theta_{SA}$, thermal resistance from case to ambient in °C/W.

$T_C = T_A + P * \theta_{CA}$ (where T_A = ambient temperature and P = power applied to the CPU).

To maintain the case temperature under 85°C during operation θ_{CA} can be reduced by a heat-sink/fan combination. (The heatsink/fan decreases θ_{CA} by a factor of three compared to using a heatsink alone.) The required θ_{CA} to maintain 85°C is shown in Table 5-4. The designer should ensure that adequate air flow is maintained to control the ambient temperature (T_A).

Table 2-3. Required θ_{CA} to Maintain 85°C Case Temperature

Frequency (MHz)	Power* (W)	θ_{CA} For Different Ambient Temperatures				
		25°C	30°C	35°C	40°C	45°C
200	10.3	5.83	5.34	4.85	4.37	3.88
233	11.4	5.26	4.82	4.39	3.95	3.51
266	12.7	4.72	4.33	3.94	3.54	3.51
270	13.0	4.62	4.23	3.85	3.46	3.08

*Note: Power based on Max Active Power values. Refer to Cyrix Applicaton Note 123 *Mobile CPU Thermal Design Considersations* for more information.

A typical θ_{JC} value for the M II Mobile 296-pin PGA-package value is 0.5 °C/W.

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January 5, 1999 3:18 pm
C:\!!devices\MII\mobile\M2_mob2.fm

Rev 0.92 Typos, MII -> M II, added 266 and 270 MHz
Rev 0.91 Minor corrections
Rev 0.9 New