PRODUCT CATALOG

SPRING 1994

C-Cube Microsystems

C-Cube Microsystems
Product Catalog

Spring 1994

C-Cube
Microsystems

This catalog provides an overview of each major product in C-Cube MPEG and JPEG product lines. For each product, more detailed information can be found in the individual product documentation. In addition, products that were released after the publication date of this catalog are described in individual product briefs that are available from your C-Cube sales office. See the list of sales offices at the back of this catalog.

Trademark Acknowledgment

C-Cube Microsystems
1778 McCarthy Boulevard
Milpitas, CA 95035
Telephone (408) 944-6300
Fax (408) 944-6314
e-mail: techpubs@c-cube.com

C-Cube Part # 90-0500-001

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Product Overview

C-Cube Microsystems is a leading developer of integrated circuits and software that compress and decompress digital video and still-image data. C-Cube's compression technology allows full-motion video and true-color images to be incorporated in consumer electronic, computer, cable and broadcast television, and telephony products. C-Cube Microsystems' mission is to be, and be perceived as, the **world leader** in the delivery of digital **video and image compression** solutions to the computer, communication and consumer electronics markets. This chapter describes the products that C-Cube offers to address these markets and provides some background information about the company.

The Need for Compression

More than 70 percent of all human communication is visual, as evidenced by people's preference for television and motion picture products over non-visual media. However, the high communications channel bandwidths demanded by visual media have limited applica-

tions to broadcast television and motion-picture theaters, one-way visual communication at best.

Moving visual data from the analog domain to the digital domain, however, can expand visual communications to new applications by allowing interactivity and reducing communications channel bandwidth requirements. Interactivity and lower bandwidth requirements will enable interactive TV, distance learning, home shopping, video telephones, video on demand and a host of other applications.

Digital video and still images, however, require compression to meet the bandwidth requirements demanded by these applications. For example, one photographic-quality still image requires 25 megabytes of storage and one second of motion video requires 30 megabytes of storage.

By compressing images by orders of magnitude (without visible degradation), C-Cube products eliminate the storage, central memory and bandwidth bottlenecks that have prevented television, consumer electronics and desktop computer products from using digital still images and digital motion video.

Products

C-Cube develops and markets a wide range of compression products, including high-performance integrated circuits, development systems and engineering services in these product categories:

- JPEG Codecs
- MPEG Decoders
- MPEG Encoders
- Development System Products
- Engineering Services

JPEG Codecs

In July of 1990, C-Cube introduced the CL550 JPEG Still-Image Processor, the first implementation of the JPEG image compression standard. The 400-thousand-transistor CL550 is highly integrated, requiring minimal additional logic to implement a complete imaging system. The CL550 is also a very high-performance device: it is capable of compressing/decompressing SIF-resolution color video at 30 frames per second.

The CL560 is an enhanced version of the CL500 designed for high-end imaging and real-time video compression and decompression. (See Chapter 3 for more information about the CL550 and CL560.)

MPEG Decoders

In June of 1991, C-Cube demonstrated the world's first MPEG video decoder, the single-chip CL950. Originally intended as a proof-of-concept vehicle, the CL950's ability to decode video at broadcast resolution has accelerated the development of digital cable television and direct broadcast from satellite systems by over a year. (C-Cube currently is developing an MPEG 2 decoder that will replace the CL950.)

In May of 1992, C-Cube introduced the CL450 MPEG Video Decoder, a single chip specifically designed to enable digital video in consumer electronic players . Developed with input from JVC and Philips, the CL450 is a complete MPEG decoder on a chip, requiring only 4 Mbits of DRAM to decode SIF-resolution MPEG bit streams at up to 3 Mbits per second. Like the CL550 and CL950, the CL450 is the first product of its kind, reflecting C-Cube's continuing leadership in compression technologies. (See Chapter 8.)

MPEG Encoders

In October 1993, C-Cube brought to market the world's first highly integrated MPEG video encoders, making the delivery of digital video on low-bandwidth media practical for the first time. The CLM4500 Consumer MPEG Video Encoder is designed to allow developers to encode SIF-resolution video in real time for karaoke, VideoCD, video on demand, interactive games, kiosks, etc. The CLM4600 Broadcast MPEG Video Encoder allows cable companies to realize the 500-channel cable systems, direct broadcast from satellite, video on demand, and other digital television systems envisioned over the past several years. Both products are based on C-Cube's VideoRISC Processor, the first microprocessor designed to process digital video as a data type. The VideoRISC Processor represents a major advancement in digital video technology, which promises to revolutionize the way that video is delivered. (See Chapters 5 and 6 for more information about the CLM4500 and CLM4600, respectively.)

Development System Products

C-Cube has also developed system-level products to support the development of applications for its VLSI products.

- VideoRISC MPEG Encoder Development Station - A real-time MPEG video and audio encoder system that is based on C-Cube's VideoRISC Processors. This desk-side system is intended as a prototyping tool for customers developing MPEG-based systems, but the Encoder Station can also by used as an authoring tool for music video, Karaoke, and movie program content for distribution on CD or via video on demand systems. (See Chapter 7.)
- MPEG Video Decoder Lab – Hewlett-Packard NetServer PC with a CL950-based video decoder board, to allow customers to evaluate MPEG at various bit rates and video resolutions. The Video Decoder Lab can decode CCIR 601 (720 x 480 NTSC; 704 x 576 PAL) resolution video at bit rates of up to 10 Mbits per second. (See Chapter 10.)
- MPEG Video/Audio Decoder Board – A CL450-based video/audio decoder board for the PC, this product allows users to play MPEG video and stereo audio from a CD or other low-bandwidth storage media. (The MPEG Video/Audio Decoder Board is part of the CL450 Development Kit, see Chapter 9.)
- JPEG Still-Image Board – A cost-effective 1/2-card for the PC-AT that uses the CL550 to compress high-resolution still images; this board is ideal for pre-press image-editing applications. (See Chapter 4.)

All of the above development kits include demonstration software, driver source code, PAL equations, schematics and documentation.

Engineering Services

In addition to developing standard products that will serve the broad market for compression technology, C-Cube develops custom products for customers with specific applications. Providing more highly integrated or uniquely featured products allows customers to differentiate their products from their competition and thus defend markets in this standards-based industry.

Target Markets and Applications

These products are targeted at three discrete market areas: consumer, communications, and computers.

Consumer

Manufacturers of digital photographic, video, game and HDTV equipment. Applications include:

- Digital movie players
- Video Karaoke
- Video games
- Digital cameras
- Digital video cassette recorders
- Digital television receivers

Communications

Manufacturers of cable and broadcast television equipment, and video telecommunications equipment. Applications include:

- Cable television channel multiplexing
- Automated ad insertion
- Video telephony
- Professional video editing
- Direct television broadcast from satellite (DBS)
- Video-on-demand services

Computers

Manufacturers of systems and peripherals including workstations, personal computers, video boards and laser printers. Applications in this market include:

- Video conferencing
- High-color image editors (pre-press)
- Desktop video editing
- Multimedia presentation authoring
- Image databases
- Color scanners, printers, copiers

Competitive Advantages

C-Cube integrates the disciplines of VLSI (very large scale integration), system and software design with the latest advances in imaging and graphics algorithms. The company has filed broad patents covering the original algorithms and architectures it has developed to implement international image compression standards.

The company, aware of the broad range of disciplines required to develop compression products, has assembled an exceptional team of technologists, including psychovisual experts, mathematicians, microprocessor architects, system designers, and others. As a result, C-Cube has played a leadership role in defining both the JPEG and MPEG standards. For example, Dr. Didier Le Gall is the chairman of the MPEG video committee, and Dr. Jean-Georges Fritsch is a contributing member of the MPEG audio committee. Eric Hamilton is chairman of the JPEG committee and has been active in continuing development of the JPEG standard.

In addition, C-Cube has developed complete MPEG audio/video encoding and decoding systems, as well as JPEG video and still-image board-level products. The resulting system expertise informs the VLSI designs in which C-Cube is engaged, ensuring that they can be easily and cost-effectively integrated into customer products.

International Standards

Since the transition of video and still images from the analog to digital domain was predicted by nearly everyone in any industry dealing (or desiring to deal) with video and image information, the International Standards Organization (ISO) and the International Committee on Telegraph and Telephones (CCITT) established working committees in 1988 to develop standards for digital video and still image compression and decompression. These standards include one defined by the Joint Photographic Experts Group (JPEG) for still-image and video compression, one defined by the Moving Picture Experts Group (MPEG) for video and audio compression, and Px64, which represents a class of algorithms dedicated to video telephony (conferencing). All C-Cube products conform to one or more of these international standards. (See Chapters 1 and 2 for overviews of the JPEG and MPEG standards, respectively.)

1
JPEG Overview

This chapter presents an overview of the JPEG video compression standard. The chapter is divided into these sections:

- 1.1, JPEG Background Information
- 1.2, Operation of the JPEG Algorithm
- 1.3, Discrete Cosine Transform
- 1.4, Quantization
- 1.5, Zero Run-Length Coding
- 1.6, Entropy Encoding
- 1.7, Summary of JPEG Baseline

1.1 JPEG Background Information

The obvious advantages of digital image compression led to the formation of an international standards group: the Joint Photographic Experts Group (JPEG). JPEG is a joint ISO/CCITT technical committee (ISO/IEC JTC1/SC2/WG10, Photographic Image Coding) whose goal has been to develop a general-purpose international standard for the compression of continuous-tone (grayscale or true color) digital images. The overall standard sets requirements and implementation guidelines for the image coding and decoding processes and for the coded representation of the compressed image data.

The standard defined by JPEG has usefulness in a broad range of applications. Because each application has different compression requirements, several processes for compression and decompression are specified within the JPEG standard. The processes fall into three general categories: the Baseline Sequential Process, the Extended DCT-Based Processes, and the Lossless Process. All JPEG coders and decoders must support the Baseline Sequential Process. All other processes are optional extensions that can be useful in specific applications. For detailed information on each of the processes, refer to the ISO Committee Draft document, ISO/IEC CD 10918-1.

The Baseline Sequential Process is based on the Discrete Cosine Transform (DCT) followed by variable-word-length coding (Huffman coding). This process provides substantial compression (up to 100:1) while maintaining a high degree of visual fidelity in the reconstructed image. DCT-based processes, however, are lossy processes. The reconstructed images are not byte-for-byte equivalent to the source images. Further, the level of loss in the image varies with the compression ratio. Typically, the Baseline Sequential Process can compress image data to about 1 bit/pixel or less with very good visual quality in the reconstructed image. For example, a 24-bit RGB color image can be compressed to 1 bit/pixel (less than 5% of the original size), and the reconstructed image will be nearly indistinguishable from the original. The C-Cube CL550 is a VLSI implementation of the Baseline Sequential Process.

1.2 Operation of the JPEG Algorithm

The operation of the Baseline JPEG algorithm can be divided into three basic stages, as shown in Figure 1-1:

1. The removal of the data redundancy by means of the discrete cosine transform (DCT).
2. The quantization of the DCT coefficients using weighting functions optimized for the human visual system.
3. The encoding of the data to minimize the entropy of the quantized DCT coefficients. The entropy encoding is done with a Huffman variable-word-length encoder.

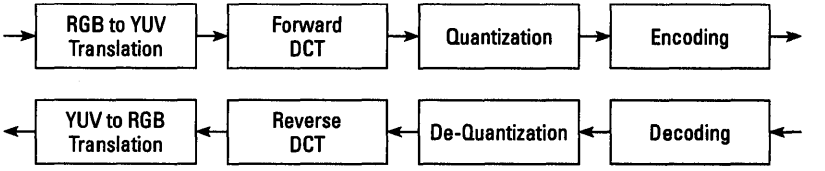


Figure 1-1 Basic Image Compression Scheme for Coder and Decoder

Although color conversion is a part of the redundancy removal process, it is not part of the JPEG algorithm. It is the goal of JPEG to be independent of the color space. JPEG handles colors as separate components. Therefore, it can be used to compress data from different color spaces, such as RGB, YCbCr, and CMYK.

However, the best compression results are achieved if the color components are independent (noncorrelated), such as in YCbCr, where most of the information is concentrated in the luminance and less in the chrominance. RGB color components can be converted via a linear transformation into YCbCr components, as shown in Table 1-1.

Table 1-1 Converting RGB Components to YCbCr Components

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.144 \\ -0.169 & -0.3316 & 0.0500 \\ 0.500 & -0.4186 & -0.0813 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Another advantage of using the YCbCr color space comes from reducing the spatial resolution of the Cb and Cr chrominance components. Because chrominance does not need to be specified as frequently as luminance, every other Cb element and every other Cr element can be discarded. As a consequence, a data reduction of 3 to 2 is obtained by transforming RGB into YCbCr 4:2:2. The conversion in color space is a first step toward compressing the image.

1.3 Discrete Cosine Transform

For each separate color component, the image is broken into 8x8 blocks that cover the entire image. These blocks form the input to the DCT.

In the 8x8 blocks, typically the pixel values vary slowly. Therefore, the energy is of low-spatial frequency. A transform that can be used to concentrate the energy into a few coefficients is the two-dimensional 8x8 DCT. This transform, studied extensively for image compression, is extremely efficient for highly correlated data.

Conceptually, a one-dimensional DCT can be thought of as taking the Fourier Transform and retaining only the real (the cosine) part. The two-dimensional DCT can be obtained by performing a one-dimensional DCT on the columns and then a one-dimensional DCT on the rows. The transformed output from the two-dimensional DCT is ordered such that the mean value, the DC coefficient, is in the upper left corner of the 8x8 coefficient block and the higher frequency coefficients progress by distance from the DC coefficient. Higher vertical frequencies are represented by higher row numbers, and higher horizontal frequencies are represented by higher column numbers.

1.4 Quantization

The next step is the quantization of the frequency coefficients. The coefficients are quantized to reduce their magnitude and increase the number of zero-value coefficients. A uniform quantizer was selected for the JPEG baseline method. The step size is varied according to the coefficient location and tuned for each color component. This is shown in Figure 1-2 and Figure 1-3. Figure 1-3 illustrates two functional matrices that have been optimized for CCIR 601 imagery.

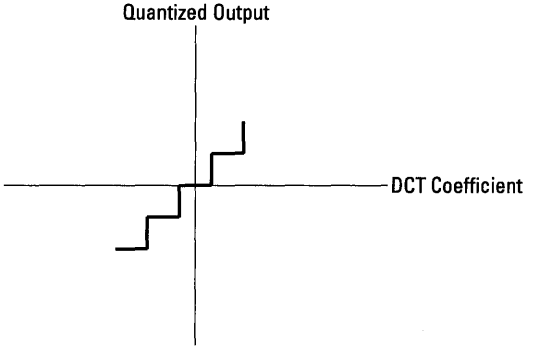
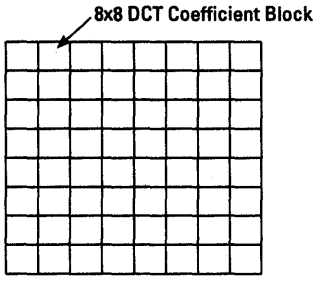


Figure 1-2 Quantizer Stepping (Uniform Quantization)

The coding model rearranges the quantized frequency coefficients into a zigzag pattern, with the lowest frequencies first and the highest frequencies last. The zigzag pattern (shown graphically in Figure 1-4 and numerically in Table 1-2) is used to increase the run-length of zero coefficients found in the block. The assumption is that the lower frequencies tend to have larger coefficients and the higher frequencies are, by the nature of most pictures, predominantly zero. As illustrated in Figure 1-4, the first coefficient (0,0) is called the DC coefficient and the remaining coefficients are AC coefficients. The AC coefficients are traversed by the zigzag pattern from the (0,1) location to the (7,7) location.



Y Component Matrix							
16	11	10	16	24	40	51	61
12	12	14	19	26	58	60	55
14	13	16	24	40	57	69	56
14	17	22	29	51	87	80	62
18	22	37	58	68	109	103	77
24	35	55	64	81	104	113	92
49	64	78	87	103	121	120	101
72	92	95	98	112	100	103	99

Cb Cr Component Matrix							
17	18	24	47	99	99	99	99
18	21	26	66	99	99	99	99
24	26	56	99	99	99	99	99
47	66	99	99	99	99	99	99
99	99	99	99	99	99	99	99
99	99	99	99	99	99	99	99
99	99	99	99	99	99	99	99
99	99	99	99	99	99	99	99

Figure 1-3 Weighting Functions for Luminance and Chrominance

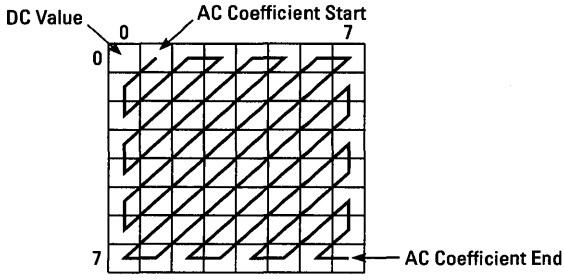


Figure 1-4 Zigzag Reordering of the 8x8 DCT Coefficients

Table 1-2 Location of Original Coefficients in Reordered Block

0	1	5	6	14	15	27	28
2	4	7	13	16	26	29	42
3	8	12	17	25	30	41	43
9	11	18	24	31	40	44	53
10	19	23	32	39	45	52	54
20	22	33	38	46	51	55	60
21	34	37	47	50	56	59	61
35	36	48	49	57	58	62	63

The DC coefficients of subsequent blocks often vary only slightly. Therefore, differences between successive DC coefficients are small. The coding of the DC coefficient exploits this property through Differential Pulse Code Modulation (DPCM). This technique codes the difference (Delta) between the quantized DC coefficient of the current block and the DC coefficient of the previous block. The formula for the encoding of the DC code is:

$$Delta_k = DC(0,0)_k - DC(0,0)_{k-1}$$

The inverse calculation takes place at the decoder.

1.5 Zero Run-Length Coding

The quantized AC coefficients usually contain runs of consecutive zeros. Therefore, a coding advantage can be obtained by using a run-length technique, where the upper four bits of the code symbol indicate

the number of consecutive zeros before the next coefficient and the lower four bits indicate the number of significant bits in the next coefficient.

Following the code symbol are the significant bits of the coefficient, the length of which can be determined by the lower four bits of the code. The inverse run-length coder translates the input coded stream into an output array of AC coefficients. It takes the current code and appends to the output array the number of zeros corresponding to the four bits used for the run-length code. The coefficient placed in the output array has the number of bits determined by the lower four bits of the run-length code and a value determined by the number of trailing bits.

1.6 Entropy Encoding

The block codes from the DPCM and run-length models can be further compressed using entropy encoding. For the baseline JPEG method, the Huffman coder is used to reduce entropy. One reason for using the Huffman coder is that it is easy to implement by means of a look-up table in hardware. To compress data symbols, the Huffman coder creates shorter codes for frequently occurring symbols and longer codes for occasionally occurring symbols. Many applications may use predefined Huffman tables. Therefore, the baseline encoder can operate as a one-pass or two-pass system. In the one-pass system, predetermined Huffman tables are used, whereas in the two-pass system, Huffman tables are created that are specific to the image to be encoded.

The first step in creating the Huffman codes is to create a table assigning a frequency count to each symbol. Symbols with a higher probability are assigned shorter codes than the less frequently occurring symbols.

1.7 Summary of JPEG Baseline

The baseline system provides efficient lossy image compression. It supports four color components simultaneously, with a maximum number of eight input bits for each color pixel component.

The basic data entity is a block of 8x8 pixels. However, this block can represent a large sub-sampled image area (for example, sub-sampled by decimated chrominance signals). The blocks of the different color components are sent interleaved, thereby allowing the decoder to create the decompressed image and translate back to the original color space on the fly.

2
MPEG Overview

This chapter presents an overview of the Moving Picture Experts Group (MPEG) standard. The MPEG 2 standard has three elements: video, audio and system. The video element defines a syntax for compressed video, and gives the outlines of the techniques that can be used to compress video into that syntax. The video element was finalized at the MPEG committee meeting in Sydney in April, 1993. The audio element of the standard similarly defines a syntax for compressed audio, and the system element describes the mechanism for combining and synchronizing the video and audio elements in a single data stream. Neither the audio or system elements of the standard have been finalized.

Semiconductors to support each of the MPEG 2 elements are required; however, the semiconductor devices required to implement the audio and system elements of the standard exist, whereas they do not for the video element. Thus video encoder and decoder chip development is in the "critical path" for the implementation of MPEG 2 for digital television.

2.1 MPEG 1 and MPEG 2

When the MPEG committee began the task of specifying a syntax for compressed digital video, its goal was the delivery of video on a compact disc, taking into account its very low data transfer rate of 1.416 Mbits per second. Aware that it was impossible to represent a CCIR 601-resolution image at such a low data rate, the committee specified a one-quarter resolution image (352x240 NTSC; 352x288 PAL) as the standard input format (SIF). As a result, the committee made MPEG 1 a frame-oriented syntax rather than a field-oriented syntax. When decoded, the SIF-resolution video is expanded to fill a full television screen, resulting in an image quality that is similar to VHS tape.

Broadcast-television equipment makers immediately recognized the potential of MPEG technology to increase the channel efficiency of satellite transponders and cable networks, but the broadcast industry was not limited to compact disc bandwidths and was unwilling to settle for VHS resolution. As a consequence, the MPEG committee developed a second standard, called MPEG 2, specifically designed for broadcast applications. The MPEG 2 standard is designed to represent CCIR 601-resolution video (704x480 NTSC; 704x576 PAL) at a data rates of 4.0 to 8.0 Mbits per second. In addition, MPEG 2 provides support for interlaced fields, 16:9 aspect ratio video, multiple video channels in a single system stream, and extensibility to HDTV. It is also important to note that MPEG 1 is a subset of MPEG 2, so any MPEG 2 decoder will be able to decode MPEG 1 syntax video.

2.2 MPEG Stream Structure

This section explains the general structure of an MPEG stream and introduces some basic concepts used in the rest of the chapter.

2.2.1 MPEG Stream Structure

In its most general form, an *MPEG stream* is made up of two layers:

- The *system layer* contains timing and other information needed to demultiplex the audio and video streams and to synchronize audio and video during playback.
- The *compression layer* includes the compressed audio and video streams.

2.2.2 General Decoding Process

Figure 2-1 shows a generalized decoding system.

The *system decoder* extracts the timing information from the MPEG stream and sends it to the other system components. (Section 2.5 has more information about the use of timing information for audio and video synchronization.) The system decoder also demultiplexes the video and audio streams and sends each to the appropriate decoder. In many applications, the system decoder function is implemented as a software program on the host computer.

The *video decoder* decompresses the video stream as specified in Part 2 of the MPEG standard. (See Sections 2.3 and 2.4 for more information about video compression.) C-Cube currently offers the CL450 and CL950 as MPEG decoders.

The *audio decoder* decompresses the audio stream as specified in Part 3 of the MPEG standard.

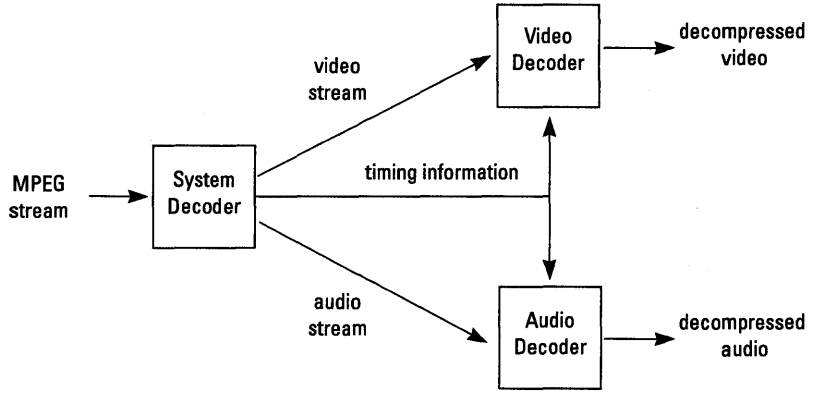


Figure 2-1 General MPEG Decoding System

2.2.3 Video Stream Data Hierarchy

The MPEG standard defines a hierarchy of data structures in the video stream as shown schematically in Figure 2-2.

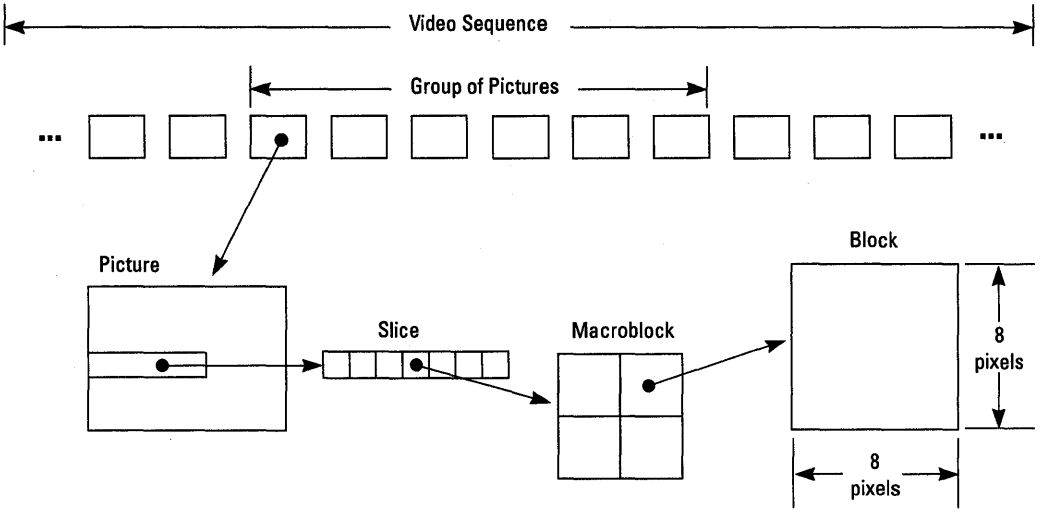


Figure 2-2 MPEG Data Hierarchy

Video Sequence

Consists of a sequence header, one or more groups of pictures, and an end-of-sequence code. The video sequence is another term for a video stream as defined above.

Group of Pictures

A series of one or more pictures intended to allow random access into the sequence.

Picture

The primary coding unit of a video sequence. A picture consists of three rectangular matrices representing luminance (Y) and two chrominance (CbCr) values. The Y matrix has an even number of rows and columns. The Cb and Cr matrices are one-half the size of the Y matrix in each direction (horizontal and vertical).

Figure 2-3 shows the relative x-y locations of the luminance and chrominance components. Note that for every four luminance values, there are two associated chrominance values: one Cb value and one Cr

value. (The location of the Cb and Cr values is the same, so only one circle is shown in the figure.)

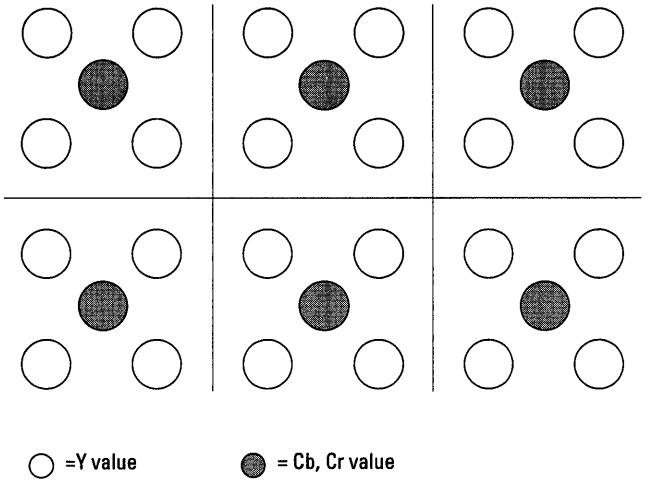


Figure 2-3 Location of Luminance and Chrominance Values

Slice

One or more contiguous macroblocks. The order of the macroblocks within a slice is from left to right and top to bottom.

Slices are important in the handling of errors. If the bitstream contains an error, the decoder can skip to the start of the next slice. Having more slices in the bitstream allows better error concealment but uses bits that could otherwise be used to improve picture quality.

Macroblock

A 16-pixel by 16-line section of luminance components and the corresponding 8-pixel x 8-line section of the chrominance components. See Figure 2-3 for the spatial location of luminance and chrominance components. A macroblock contains four Y blocks, one Cb block and one Cr block as shown in Figure 2-4. The numbers correspond to the ordering of the blocks in the data stream, with block 1 first.

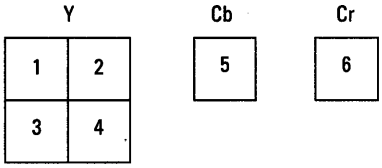


Figure 2-4 Macroblock Composition

Block

A block is an 8-pixel by 8-line set of values of a luminance or a chrominance component. Note that a luminance block corresponds to one-fourth as large a portion of the displayed image as does a chrominance block.

2.3 Inter-Picture Coding

Much of the information in a picture within a video sequence is similar to information in a previous or subsequent picture. The MPEG standard takes advantage of this temporal redundancy by representing some pictures in terms of their differences from other (reference) pictures, or what is known as *inter-picture coding*. This section describes the types of coded pictures and explains the techniques used in inter-picture coding.

2.3.1 Picture Types

The MPEG standard specifically defines three types of pictures: intra, predicted, and bidirectional.

Intra Pictures

Intra or I-pictures are coded using only information present in the picture itself. I-pictures provide random access points into the compressed video data. I-pictures use only transform coding and therefore provide moderate compression. I-pictures typically use about two bits per coded pixel.

Predicted Pictures

Predicted or P-pictures are coded with respect to the nearest previous I- or P-picture. This technique is called *forward prediction* and is illustrat-

ed in Figure 2-5. Predicted pictures provide more compression and serve as a reference for B-pictures and future P-pictures. P-pictures use motion compensation to provide more compression than is possible with I-pictures. P-pictures can propagate coding errors, since P-pictures can be predicted from previous P-pictures.

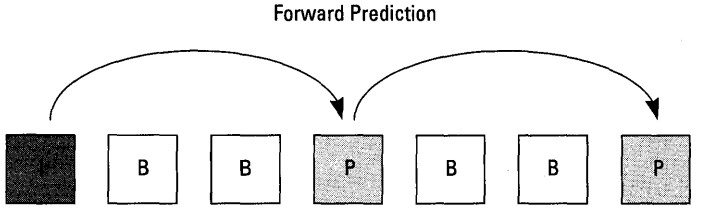


Figure 2-5 Forward Prediction

Bidirectional Pictures

Bidirectional or B-pictures are pictures that use both a past and future picture as a reference. This technique is called *bidirectional prediction* and is illustrated in Figure 2-6. Bidirectional pictures provide the most compression and do not propagate errors because they are never used as a reference. Bidirectional prediction also decreases the effect of noise by averaging two pictures.

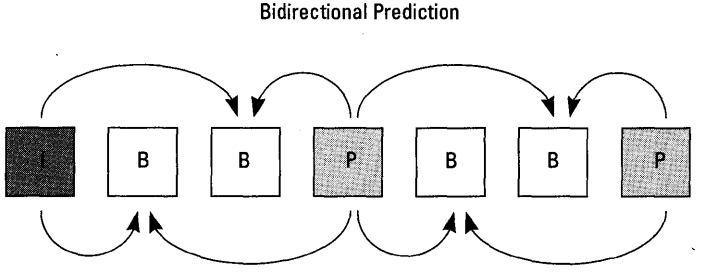


Figure 2-6 Bidirectional Prediction

2.3.2 Video Stream Composition

The MPEG algorithm allows the encoder to choose the frequency and location of I-pictures. This choice is based on the application's need for

random accessibility and the location of scene cuts in the video sequence. In applications where random access is important, intra pictures are typically used two times a second.

The encoder also chooses the number of bidirectional pictures between any pair of reference (I or P) pictures. This choice is based on factors such as the amount of memory in the encoder and the characteristics of the material being coded. For a large class of scenes, a workable arrangement is to have two bidirectional pictures separating successive reference pictures. A typical arrangement of I-, P-, and B-pictures is shown in Figure 2-7 in the order in which they are displayed.

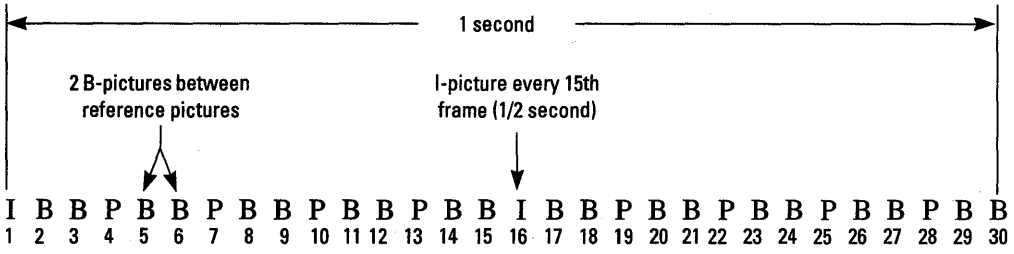


Figure 2-7 Typical Display Order of Picture Types

The MPEG encoder reorders pictures in the video stream to present the pictures to the decoder in the most efficient sequence. In particular, the reference pictures needed to reconstruct B-pictures are sent before the associated B-pictures. Figure 2-8 demonstrates this ordering for the first section of the example shown above.

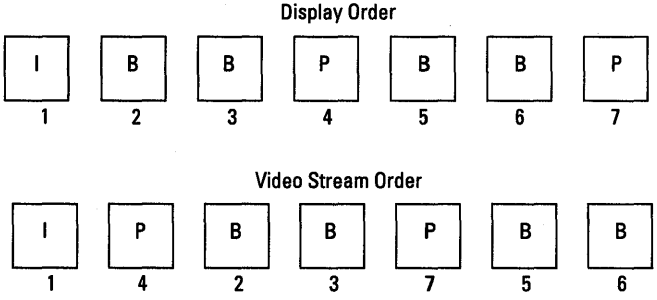


Figure 2-8 Video Stream versus Display Ordering

2.3.3 Motion Compensation

Motion compensation is a technique for enhancing the compression of P- and B-pictures by eliminating temporal redundancy. Motion compensation typically improves compression by about a factor of three compared to intra-picture coding. Motion compensation algorithms work at the macroblock level.

When a macroblock is compressed by motion compensation, the compressed file contains this information:

- The spatial difference between the reference and the macroblock being coded (*motion vectors*)
- The content differences between the reference and the macroblock being coded (*error terms*)

Not all information in a picture can be predicted from a previous picture. Consider a scene in which a door opens. The visual details of the room behind the door cannot be predicted from a previous frame in which the door was closed. When a macroblock in a P-picture cannot be represented by motion compensation, it is coded in the same way as a macroblock in an I-picture, that is, by transform coding techniques (see Section 2.4).

Macroblocks in a B-picture can be coded using either a previous or future reference picture as a reference, so that four codings are possible:

- Intra coding: no motion compensation
- Forward prediction: the closest previous I- or P-picture is used as a reference
- Backward prediction: the closest future I- or P-picture is used as a reference
- Bidirectional prediction: two pictures are used as reference, the closest previous I- or P-picture and the closest future I- or P-picture

Backward prediction can be used to predict uncovered areas that do not appear in previous pictures.

2.4 Intra-Picture (Transform) Coding

The MPEG transform coding algorithm includes these steps:

- Discrete cosine transform (DCT)
- Quantization
- Run-length encoding

Both image blocks and prediction-error blocks have high spatial redundancy. To reduce this redundancy, the MPEG algorithm transforms 8 x 8 blocks of pixels or 8 x 8 blocks of error terms to the frequency domain with the Discrete Cosine Transform (DCT).

Next, the algorithm quantizes the frequency coefficients. Quantization is the process of approximating each frequency coefficient as one of a limited number of allowed values. The encoder chooses a quantization matrix that determines how each frequency coefficient in the 8 x 8 block is quantized. Human perception of quantization error is lower for high spatial frequencies, so high frequencies are typically quantized more coarsely (i.e., with fewer allowed values) than low frequencies.

The combination of DCT and quantization results in many of the frequency coefficients being zero, especially the coefficients for high spatial frequencies. To take maximum advantage of this, the coefficients are organized in a zigzag order to produce long runs of zeros (see Figure 2-9). The coefficients are then converted to a series of run-amplitude pairs, each pair indicating a number of zero coefficients and the amplitude of a non-zero coefficient. These run-amplitude pairs are then coded with a variable-length code, which uses shorter codes for commonly occurring pairs and longer codes for less common pairs.

Some blocks of pixels need to be coded more accurately than others. For example, blocks with smooth intensity gradients need accurate coding to avoid visible block boundaries. To deal with this inequality between blocks, the MPEG algorithm allows the amount of quantization to be modified for each 16 x 16 block of pixels. This mechanism can also be used to provide smooth adaptation to a particular bit rate.

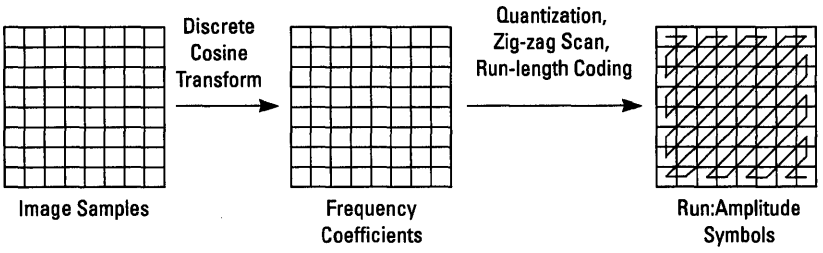


Figure 2-9 Transform Coding Operations

2.5 Synchronization

The MPEG standard provides a timing mechanism that ensures synchronization of audio and video. The standard includes two parameters used by the decoder: the *system clock reference (SCR)* and the *presentation time stamp (PTS)*.

The MPEG system clock running at 90 kHz generates 7.8 x 10^9 clocks in a 24-hour day. System clock references and presentation time stamps are 33-bit values, which can represent any clock cycle in a 24-hour period.

2.5.1 System Clock References

A system clock reference is a snapshot of the encoder system clock. The SCRs used by the audio and video decoder must have approximately the same value. To keep their values in agreement, SCRs are inserted into the MPEG stream at least as often as every 0.7 seconds by the MPEG encoder, and are extracted by the system decoder and sent to the audio and video decoders as illustrated in Figure 2-10. The video and audio decoders update their internal clocks using the SCR value sent by the system decoder.

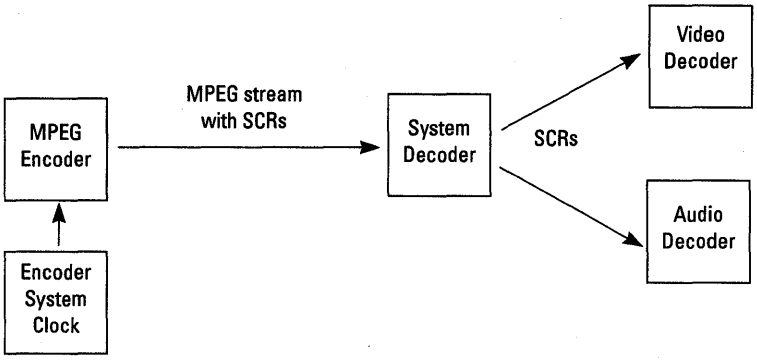
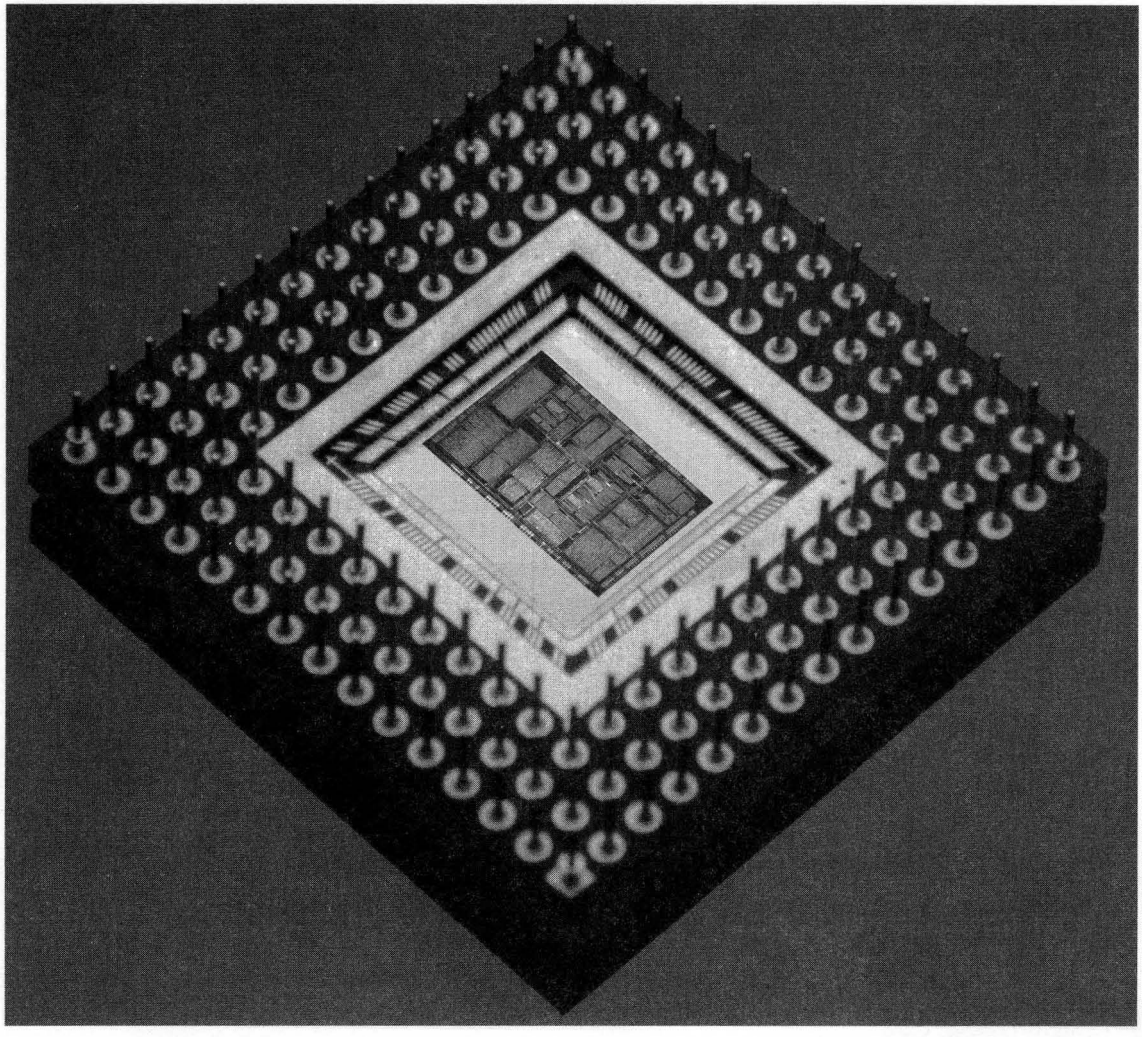


Figure 2-10 SCR Flow in MPEG System

2.5.2 Presentation Time Stamps

Presentation time stamps are samples of the encoder system clock that are associated with some video or audio *presentation units*. A presentation unit is a decoded video picture or a decoded audio time sequence. The encoder inserts a new PTS into the MPEG stream at least as often as every 0.7 seconds. The PTS represents the time at which the video picture is to be displayed or the starting playback time for the audio time sequence.

The video decoder either deletes or repeats pictures to ensure that the PTS matches the current value of the SCR when a picture with a PTS is displayed. If the PTS is earlier (has a smaller value) than the current SCR, the video decoder discards the picture. If the PTS is later (has a larger value) than the current SCR, the video decoder repeats the display of the picture.



The CL560 is the successor to the CL550, which was the world's first JPEG processor when it was introduced in 1990. Both products are high-performance single-chip JPEG processors that encode and decode gray-scale and color images at video rates.

3
CL550 and CL560 JPEG Compression Processors

The C-Cube CL550 and CL560 are high-performance single-chip compression/decompression processors that implement the baseline CCITT/ISO Joint Photographic Experts Group (JPEG) digital image compression algorithm. The CL550 and CL560 processors are designed for applications that require manipulation of high-quality digital pictures and motion sequences.

These parts can encode and decode grayscale and color images at video rates. The image compression ratio is controlled by the on-chip quantization tables. Compression ratios from 8:1 to 100:1 are possible depending on the quality, storage and bandwidth requirements of each application.

The CL550 and CL560 have on-chip video and host bus interfaces. The video interface supports 8-bit grayscale, RGB, CMYK or 4:4:4:4, and YUV (4:2:2 and 4:4:4) input and output. The host bus interface provides a direct interface to the system bus for ease of system integration.

3.1 CL550 Features

The CL550 compression/decompression processor features the following:

- Compressed output conforms to the JPEG Baseline Process as defined by ISO IS 10918-1
- Real-time compression and decompression of CIF (320 x 240 x 30 fields per second) and 1/2 CCIR 601 video (640 x 240 x 25 or 30 fields per second.
- Up to 2 Mbytes/second sustained compressed data rate
- Highly pipelined DCT/IDCT processor running at up to 30 Mhz
- Support for 8-bit grayscale, RGB, CMYK or 4:4:4:4, and YUV color space input and output
- User-accessible quantizer and Huffman tables
- Frame-by-frame adjustment of compression ratios
- High integration
  - On-chip DCT/IDCT processor
  - On-chip quantizer and Huffman tables
  - On-chip video interface
  - On-chip 16-bit or 32-bit host bus interface
- Standard 144-pin MQUAD and ceramic PGA packages
- CMOS technology

3.2 CL560 Additional Features

The CL560 compression/decompression processor offers an enhanced set of performance-related features for demanding video and image applications:

- Up to 60 Mbytes/second sustained compression rate
- Up to 15 million pixels/second processing rates
- Highly pipelined DCT/IDCT processor runs at up to 30 MHz
- Real-time compression of CCIR 601 video frames at broadcast-quality levels
- Improved Huffman table architecture allows the same Q-tables to be used for compression and decompression, allowing faster switching between modes
- Single cycle per 32-bit word Huffman CODEC

- Synchronous or asynchronous video interface operation
- On-chip 128 x 32 compressed data FIFO supports burst access
- Improved interrupt structure and DMA support
- Compression rates as high as 50:1 for real-time video applications
- Compression rates as low as 1:1 for high-quality printer, copier and professional video applications

The CL560 pinout is a superset of the CL550 pinout. Although the function of two pins has changed, most CL550 users can upgrade to the CL560 with only minor changes to printed circuit board layouts.

3.3 Applications

These JPEG processors can be used in any of the following applications:

- Multimedia
- Video editing
- Color publishing and graphics arts
- Image-processing, storage and retrieval
- Color printers, scanners and copiers
- High-speed image transmission systems for LANs, modem and color facsimile
- Digital cameras

3.4 Product Family

The CL550 and the CL560 are the two members in the JPEG compression/decompression processor family. The CL560 is an enhanced version of the CL550.

The CL550 is the first product in the family. It is designed for use in PC multimedia and still-image based systems where cost is a factor.

The CL560 is a high-performance JPEG processor designed for high-end imaging and real-time video compression and decompression. The CL560 can compress and decompress full CCIR 601-resolution video frames in real time, at compression ration as high as 50:1 or as low as 1:1. The CL560 is ideally suited for used in high-end printing and scanning systems, high-speed digital copiers and printers, and a wide range of broadcast-quality video editing applications.

3.5 CL550 Functional Description

This section describes the functional characteristics of each block within the C-Cube CL550 processor. Figure 3-1 shows the processor's major functional blocks. The CL550 is a highly pipelined machines: there are over 320 processing stages in the data path. Each stage in the JPEG Baseline Sequential Process is implemented within this pipeline.

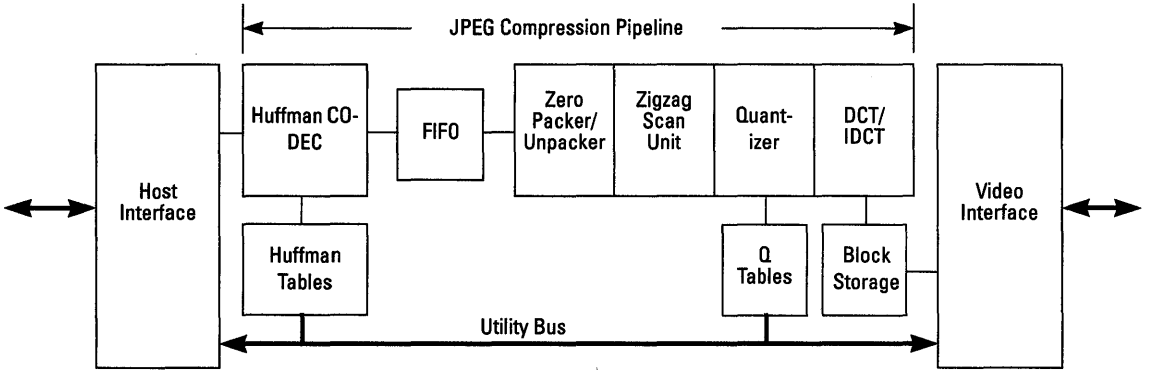


Figure 3-1 CL550 Block Diagram

During compression operations, uncompressed pixel data is written into the Video interface. The first operation that the video interface performs is a raster-to-block conversion of the pixel data. This is necessary because video generation and display devices normally deal with pixel data as raster lines, while the JPEG compression algorithm requires that the pixel data be organized as 8 x 8 blocks. Logic in the CL550 device performs that conversion.

The next step is the optional RGB-to-YUV color space conversion. This conversion is also done in the video interface. Video generation and display devices frequently present data to the CL550 as RGB pixels. The CL550 can also perform the color space conversion. Other functions done by the Video interface are pixel formatting and window sizing.

Once the Video interface has formatted the pixel data, it writes the data into the Block Storage unit. The Block Storage unit stores the 8 x 8 blocks until the JPEG compression pipeline is ready to process them. It then sequences them into the pipeline one block at a time.

Each component block is then processed by the Discrete Cosine Transform (DCT) unit. The resulting DCT coefficients are quantized by the quantizer according to user-programmable quantization matrices. The CL550 allows up to four 64-word quantization matrices to be stored on-chip, and provides programmable sequence registers to allow the user to select the appropriate matrix for each component block.

The quantized terms are then serialized by the Zigzag scan unit and the AC terms are run-length coded by the Zero Packer/Unpacker unit before being loaded into the FIFO. The FIFO serves as an intermediate buffer between the Zero Packer/Unpacker unit and the Huffman Coder/Decoder (CODEC) unit.

The Huffman CODEC draws the packed symbols from the FIFO, performs Differential Pulse Code Modulation (DPCM) calculations on the DC terms, and performs Huffman coding of both the DC and the AC terms. Huffman codes are specified by the user, and stored in on-chip table RAM that is loaded at initialization.

The Huffman codes are finally sent to the Host interface as JPEG compressed data. The Host interface is designed to operate in either slave mode or master mode. In slave mode, the CL550 acts as a peripheral device to the host processor, using a data request/data available handshake to control the transfer of data. In master mode, the CL550 works in conjunction with an external DMA controller to allow high-speed DMA transfers of data. The Host interface is explained in detail in Chapter 4, Host Interface.

Compression operations follow the opposite procedure. JPEG compressed data is written to the Host interface. The Host interface then transfers the data to the Huffman CODEC, where it is decoded. The packed symbols are put back into the FIFO. The Zero Packer/Unpacker Unit accesses the FIFO symbols, generates the AC values, and passes them to the Zigzag Scan unit for reordering into 8 x 8 block format. The DC terms are treated separately. Dequantization and Inverse DCT (IDCT) are then performed on the reassembled blocks before they are sent to the Block Storage unit. The Video interface optionally performs color space conversion of the pixel data, realigns the 8 x 8 block data as raster lines, and outputs the lines to the external video display device.

With this architecture, it is possible to construct high-performance compression systems for still-frame applications or motion video. The CL550 parts can be reinitialized on a frame-by-frame basis, allowing the programmer to change compression ratios at the end of each frame. It also allows systems to be designed where the CL550 switches back and forth between compressing and decompressing frames for half-duplex image communication.

3.6 CL560 Functional Description

This section describes the functional characteristics of each block within the C-Cube CL560 processor. Figure 3-2 shows the processor's major functional blocks. The CL560 is a highly pipelined machine with over 320 processing stages in the data path. Each stage in the JPEG Baseline Sequential Process is implemented within this pipeline. The major difference between the CL560 architecture and the CL550 architecture is in the Huffman CODEC. The synchronous CODEC in the CL560 allows data to be encoded or decoded in a single clock cycle, whereas the asynchronous CODEC in the CL550 takes several clock cycles, thus allowing higher throughput.

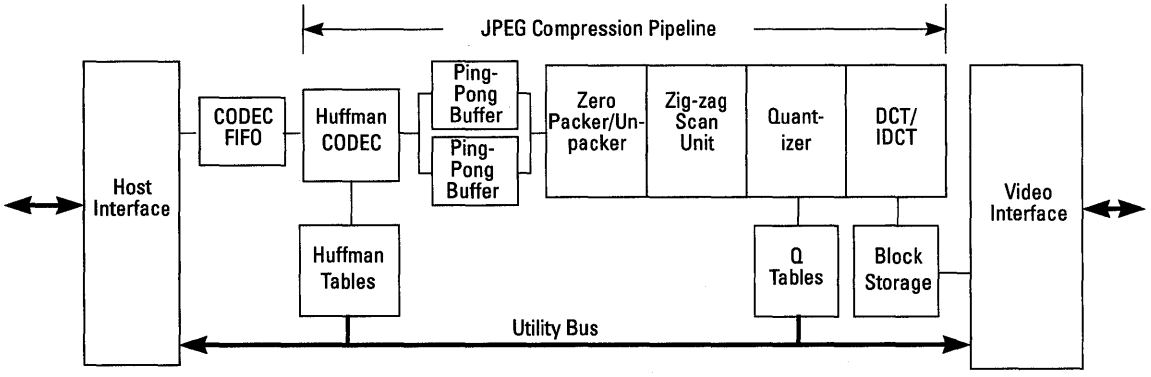


Figure 3-2 CL560 Block Diagram

During compression operations, uncompressed pixel data is written into the Video interface. The first operation that the Video interface performs is a raster-to-block conversion of the pixel data. This operation is necessary because video generation and display devices normally deal with

pixel data as raster lines, while the JPEG compression algorithm requires that the pixel data be organized as 8 x 8 blocks. Logic in the CL560 device performs that conversion.

The next step is the optional RGB-to-YUV color space conversion, also performed by the Video interface. Video generation and display devices frequently present data to the CL560 as RGB pixels. The CL560 also performs optional color space conversion. Other functions done by the Video interface are pixel formatting and window sizing.

Once the video interface is through formatting the pixel data, it writes the data into the Block Storage unit. The Block Storage unit stores the 8 x 8 blocks until the JPEG compression pipeline is ready to process them. It then sequences them into the pipeline one block at a time.

Each component block is then processed by the Discrete Cosine Transform (DCT) unit. The resulting DCT coefficients are quantized by the quantizer according to user-programmable quantization matrices. The CL560 allows up to four 64-word quantization matrices to be stored on-chip, and provides programmable sequence registers to allow the user to select the appropriate matrix for each component block. Up until this point, the CL560 compression process has been identical to the CL550 compression process.

The quantized terms are then serialized by the Zigzag scan unit and the AC terms are run-length coded by the Zero Packer/Unpacker unit before being loaded into the Ping-pong buffer. The Ping-pong buffer is a pair of synchronous 64-word registers used to smooth the flow of data to and from the Huffman CODEC.

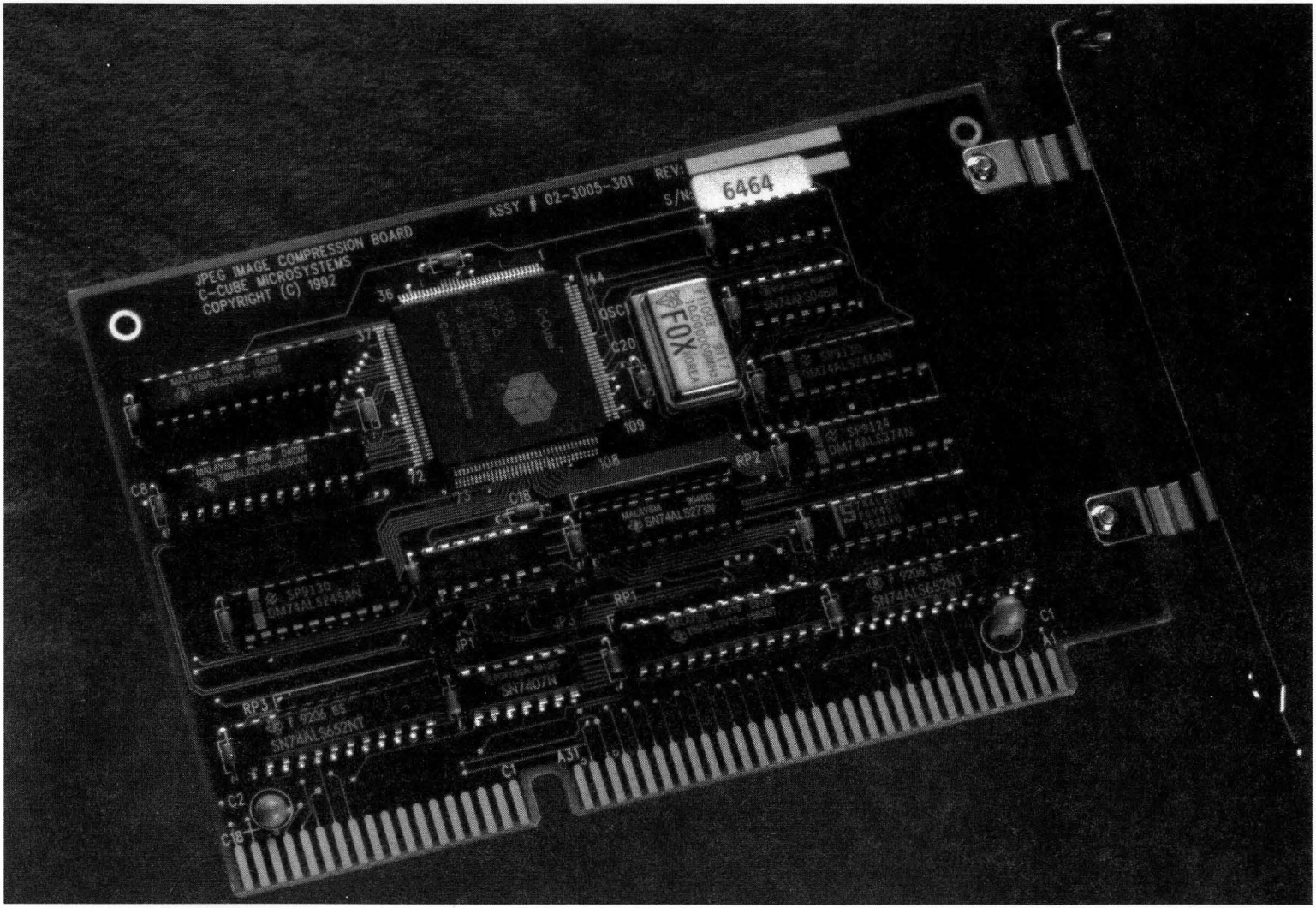
The Huffman CODEC draws the packed symbols from the Ping-pong buffer, performs Differential Pulse Code Modulation (DPCM) calculations on the DC terms, and performs Huffman Coding of both the DC and the AC terms. Huffman codes are specified by the user, and stored in on-chip RAM that is loaded at initialization.

The Huffman codes are then stored in a 128 x 32 CODEC FIFO. The FIFO acts as a rubber-band buffer between the synchronous JPEG compression pipeline and the asynchronous Host Bus interface. The FIFO is used to filter out fluctuations in the data rate. It allows fast-burst access to the CL560 to minimize the time needed to transfer data.

The Host interface is designed to operate in either register access mode or DMA access mode. In register access mode, the CL560 acts as a peripheral device to the host processor, using a data request/data available handshake to control the transfer of data. In DMA access mode, the CL560 works in conjunction with an external DMA controller to allow high-speed DMA transfers of data. The Host interface is explained in detail in Chapter 4, Host Interface.

Compression operations follow the opposite procedure. JPEG compressed data is written to the Host interface. The Host interface then stores the compressed data in the CODEC FIFO until it can be transferred to the Huffman CODEC for decoding. After decoding, the packed symbols are stored in the Ping-pong buffer. The Zero Packer/Unpacker Unit reads the Ping-pong buffer to retrieve the packed symbols, generates the AC values, and passes them to the Zigzag Scan unit for reordering into 8 x 8 block format. The DC terms are treated separately. Dequantization and Inverse DCT (IDCT) are then performed on the reassembled blocks before they are sent to the Block Storage unit. The Video interface optionally performs YUV -to-RGB color space conversion of the pixel data, realigns the 8 x 8 Block data as raster lines, and outputs the lines to the external video display device.

With this architecture, it is possible to construct very high-performance compression systems for both video and imaging applications. The CL560 parts can be reinitialized on a frame-by-frame basis, allowing the programmer to change compression ratios at the end of each frame. It also allows systems to be designed where the CL560 switches back and forth between compressing and decompressing frames for half-duplex image communication.



C-Cube's JPEG Still-Image Board is an ISA-bus card that compresses and decompresses graphic images using the CL550 JPEG Processor.

4
JPEG Still-Image Board

The C-Cube JPEG Still Image board is a high-speed, low-cost, JPEG compliant still-image compression board for IBM PCs and PC clones. It is designed to work in Intel 80386 and 80486 based computers using the Industry Standard Architecture (ISA) bus.

The JPEG Still Image compression utility program is provided with the JPEG Still-Image board. This program uses the resources of the Still-Image board to quickly compress and decompress graphic images in several different file formats. The utility is designed to run under Microsoft Windows Version 3.10.

4.1 Features

The JPEG Still-Image Board features:

- Fast image compression and decompression using the C-Cube CL550 JPEG Processor
- Supports several pixel formats:
  - 8-bit Gray scale
  - 8-bit Color (fixed palette)
  - RGB (24 bits / pixel) or YCrCb 422 (16 bits / pixel)
- Supports proposed JPEG Device Independent Bitmaps and JFIF File Formats
- Over 1Mbyte per second ISA bus transfer rate
- Still-Image board uses only 8 I/O addresses (No interrupts, No DMA channels)
- Windows-based program performs accelerated JPEG still-image compression and decompression
- .DLL Driver for Windows 3.10 included
- .VXD Virtual Device Driver for Windows 3.10 included

4.2 Product Components

The Still-Image Board package includes the following items:

- JPEG Still-Image board: An ISA-bus half-length card used for compressing and decompressing still video images
- CL550/560 User's Manual: Describes the CL550 processor
- JPEG Still-Image Board Users Manual: Explains the installation of the JPEG Still-Image board and operation of the JPEG Still Image Utility
- Software Diskette: A 3-1/2" floppy diskette containing the JPEG Still-Image Utility, the Windows drivers, and a sample compressed image
- JPEG File Interchange Format Document
- JPEG Still-Image Board technical information, including:
  - Schematic
  - Bill of Materials
  - PAL Equations

4.3 Specifications

System Requirements:

- 80386 or 80486 processor
- ISA or EISA (IBM PC-AT) Bus Structure
- 8-bit, 16-bit or 24-bit Super VGA Color Graphics Adapter
- Microsoft Windows Version 3.10 (386 Enhanced Mode)
- 640K Base Memory*
- 2 Mbytes or more of Extended Memory*
- 40 Mbyte Hard Disk Space*
- 5 1/4" or 3 1/2" High Density Floppy Disk Drive*
- Windows Compatible Mouse*

* These are requirements to run Windows, not requirements for the JPEG Still-Image Board or its associated software.

Performance:

- 1 MByte per second Compression Rate

Environmental:

Power used:	1.5 Amps @ +5VDC 7.5 Watts
Operating Temperature:	10 - 50° C
Dimensions:	1/2 Card Size 4" x 6" x 1/2"
Humidity:	10 - 90% noncondensing

File Formats Supported:

- Bitmaps
  - RLE8
  - RGB
- JFIF Compressed Files
- JPEG DIB (Device Independant Bitmap) Compressed Files

The CLM4500 uses two VideoRISC Processors to compress digital video into SIF-resolution MPEG bitstreams in real time. The product pictured above is the OPTIVideo™ board from OPTIVISION, Inc.

5
CLM4500 Consumer MPEG 1 Video Encoder

The CLM4500 Consumer MPEG Video Encoder compresses digital video into MPEG syntax in real time. The product consists of two C-Cube VideoRISC Processors and a microapplication that implements C-Cube's patented MPEG video encoding algorithm. The CLM4500 allows users to compress CCIR 601-resolution digital video into MPEG format at SIF-resolution (352x240, NTSC; 352x288, PAL). The CLM4500 supports compressed data rates of from 1 to 5 Mbits per second while maintaining excellent image quality. Video at these low data rates is suitable for distribution on low-bandwidth media such as compact disc (CD), Ethernet, and T1 links, thus enabling applications such as:

- Movies on CD
- Video on demand
- CD Karaoke
- Interactive video games
- Computer-based training
- Point-of-sale/information kiosks

5.1 Features

The features of the CLM4500 are:

- Real-time encoding of digital video into MPEG 1 syntax
- C-Cube's patented MPEG video encoding algorithm for high image quality
  - Sophisticated rate control and masking
  - Adaptive interfield filtering
- Multiple resolutions and standards
  - 352x240 (NTSC)
  - 352x288 (PAL)
  - 320x240 (square pixel)
- Multiple frame rates, including 29.97(NTSC), 25(PAL), and 23.976 (film)
- Highly integrated, uses only two VideoRISC™ Processors
  - CCIR 601 (TTL levels) video in, MPEG compressed video out
  - Interfaces to DRAM with no external logic
- Wide motion estimation search ranges with half pel accuracy
  - Predicted frames: ±48 pels horizontal, ±24 pels vertical
  - Bidirectional frames: ±32 pels horizontal, ±16 pels vertical
- Encoded bit rates from less than 1 Mbit/second to more than 5 Mbits/second
- Inverse 3-2 pulldown eliminates redundant fields in telecined film
- Message-based application program interface
  - Complete control of MPEG parameters
  - Start/stop/pause encoding by timecode
  - Human-assist control by macroblock
  - Encoder status
  - Supports vectored interrupts of the host processor
- Complies with all requirements of the MPEG standard (ISO CD 11172)
  - Support for audio/video synchronization
  - Intra, predicted, and bidirectional frames
  - Intraframe and reference distance (N and M) control

5.2 MPEG Encoding Algorithm

The MPEG standard defines a syntax for the representation of compressed digital video. While the standard tightly defines the decoder, much latitude is given to the developers of encoding algorithms.

The key to the quality of MPEG encoded video is the ability of the encoder to intelligently "distribute" its data budget for encoding video between and within the frames of video being encoded. C-Cube's MPEG video encoding algorithm has sophisticated algorithms for masking and data rate control.

5.2.1 Masking

Harshly quantizing the AC coefficients from the DCT produces a compression artifact called ringing. In some areas of an image, for example, in foliage or gravel, ringing is difficult to see. In other areas, such as around an object silhouetted against the sky, ringing is very obvious. C-Cube's patented masking algorithm determines where ringing artifacts would be visible in an image, and budgets data accordingly.

5.2.2 Rate Control

One of the principal compression techniques employed by MPEG is motion estimation, which is the process of predicting from a previous or subsequent frame the contents of the current one. When there is little motion – and thus little change – between frames, the majority of the available data budget should be spent on reference frames (intra or predicted frames) to produce the highest quality. When there is rapid movement between frames, the budget should be distributed evenly between frames.

5.3 Functional Overview

This section describes the overall organization and operation of a CLM4500-based video encoding system, which is illustrated in Figure 5-1.

5.3.1 Organization

The organization of a video encoder based on the CLM4500 is straightforward. Each of the CLM4500's two VideoRISC Processors (VRPs) has 2 Mbytes of DRAM, organized as two 256Kx32 pages, for working and microapplication storage. The VideoA, VideoB, and Host interfaces of the VRPs are connected in parallel. Video is input via the VideoA interface in digital YCbCr format at a resolution of 708x480 pixels. The

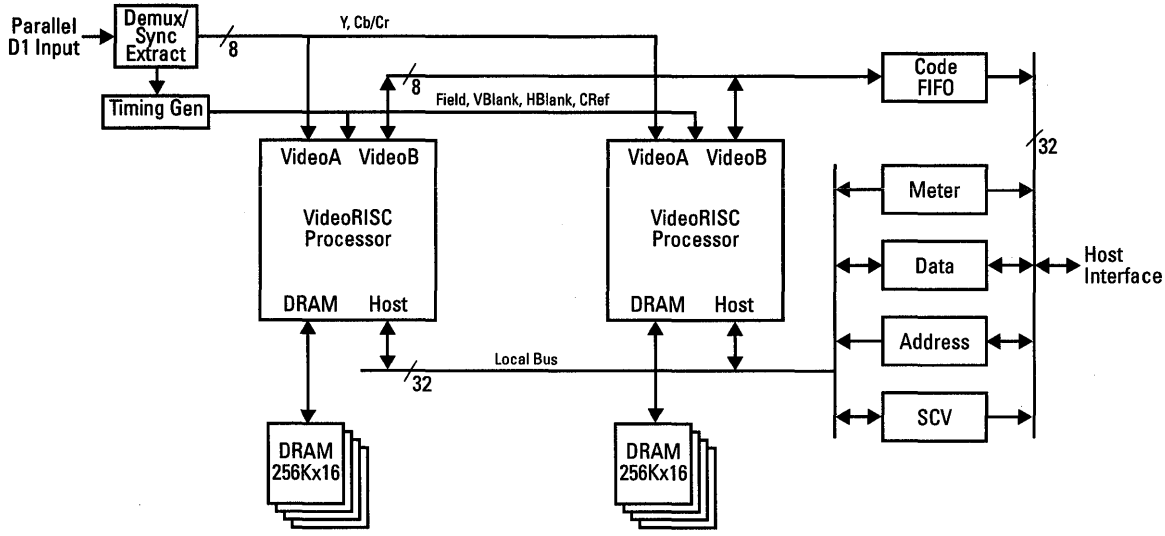


Figure 5-1 CLM4500-Based Video Encoding System

VRPs output the compressed video on the VideoB bus to the Code FIFO, a 1 Mbyte buffer from which the host can extract compressed MPEG video. The Local Bus connects the VRP host interfaces to four dual-ported registers through which the host system can load, configure and control the CLM4500:

- Meter: Maintains the Code FIFO fill level
- Data: Allows the host access to the Local Bus and the VideoRISC Processors access to the host bus
- Address: Allows the host to specify an address on the Local Bus
- SCV: This Status/Config/Vector register contains status information set by the CLM4500

5.3.2 Operation

The encoding operation is divided into four stages: capture, preprocess, encode, and output. Each stage corresponds to a frame time, but all stages are executed in parallel. Each VRP processes one half of the video image. The image is segmented horizontally with an overlap in the center equal to the vertical search range of the motion estimator.

Capture

Each VRP captures about one half of the image from the VideoA bus, filters the image in the horizontal dimension from 708 to 352 pixels, and stores the image in its DRAM. At this stage, both fields of the input (480 or 576 lines) are preserved as input for the preprocess stage. The VRP's VideoA interface and DRAM controller perform the capture process in the background, allowing the VRP's RISC Signal Processor to operate on previously grabbed frames.

Preprocess

During the next frame time, the VRP reduces the vertical resolution of the frame from 480 to 240 pixels (576 to 288 for PAL), deinterlacing video in the process. This reduction is an adaptive interfield filtering process: if there is a high correlation between the two pixels, the microapplication averages them. If there is low correlation, one pixel is discarded. This process produces a much smoother compressed image for non-interlaced sources such as film and low-motion video. During the preprocessing step, the microapplication also makes an activity estimate on the image, which is used by the rate control algorithm for distributing the data budget.

Encode

During the third frame time, each macroblock of the current frame is compared with a reference frame to produce a motion vector and a score. After motion estimation, each macroblock is processed, either into DCT format for intrablocks or into difference format for predicted blocks. The processed data is passed through the VLC and encoded data is stored in the VRP's DRAM.

Output

During the fourth frame time, the VRP outputs compressed and formatted video via the VideoB interface. The output from the two VRPs is collated in the Code FIFO.

5.3.3 Application Program Interface (API)

The CLM4500 provides a message-based API to allow an encoder control application running on the host CPU to easily configure, command, and monitor the encoder. The CLM4500 reserves three fixed-size buff-

ers in the DRAM of the master VRP. These buffers, along with the CLM4500's interrupt capability, allow for message passing.

Messages consist of commands from the host application to the CLM4500 and status from the CLM4500 to the host. Table 5-1 lists the commands supported by the CLM4500. Table 5-2 lists the CLM4500 parameters that can be set with the LoadParams command.

Table 5-1 CLM4500 Commands

Command	Function
SetRefTimeCode	Sets the reference timecode. The CLM4500 automatically increments the reference timecode with each frame.
SetOutputTimeCode	Sets the output timecode, which is included in the GOP header.
SetDefaultValues	Selects one of three default parameter sets starting with the specified timecode.
Start	Starts encoding video at the specified timecode.
Stop	Stops encoding video at the specified timecode.
Pause	Suspends encoding at the specified timecode, and preserves encoder state.
Continue	Resumes encoding at the specified timecode, using current encoder state.
LoadParams	Sets the encoding parameters beginning at the specified timecode. See Table 2, Parameters, for a description of the types of parameters that are set.
ReportStatus	Returns a message containing the encoder status at the specified timecode.
StartGOP	Starts a new GOP at the first reference frame on or after the specified timecode.
SeqUserData	Inserts data in the sequence user data field at or after the specified timecode.
GOPUserData	Inserts data in the GOP user data field at or after the specified timecode.
PicUserData	Inserts user data in the picture user data field at or after the specified timecode.

Table 5-2 CLM4500 Parameters

Parameter	Values
Interrupts	
Interrupt Enable	Disable, Enable
Interrupt Vector	Eight-bit integer
Video Source	
Source Frame Rate	23.976, 25, 29.97
Source Resolution	Height, width
Encoding Window Offset	Horizontal, vertical macroblocks
Horiz. Input Subsampling	Off, on
Sequence	
Bit Rate	Bits per second, multiples of 400
VBV Buffer Size	Kilobits, multiples of 16K
Fixed Quant	Forces quant value to 1-31. Overrides rate control. Rate control = 0.
Scene	
Output Size	Horizontal, vertical in macroblocks
Pel Aspect Ratio	Not operated upon, inserted in bitstream
Encoded Picture Rate	23.976, 25, 29.97
GOP	
Nominal GOP Size (G)	1 - 15
Intraframe Distance (N)	1 - 15
Reference Distance (M)	1 - 3
GOP Uncertainty (U)	U < N
Sequence Header Interval	0 - 32
Slice	
Slice Header Interval	Macroblocks
Matrix	
Intra Matrix	Quant levels
Non-Intra Matrix	Quant levels
Human Assist	
Relative QS Scaling	Region by macroblock address

5.4 VideoRISC Processor (VRP)

The heart of the VRP is a 32-bit RISC Signal Processor (RSP) designed by C-Cube. As with other reduced instruction set computers (RISC), the RSP's instruction set uses a load/store model for accessing memory, while arithmetic operations use the 32 local registers to allow single-cycle execution of instructions. The RSP instruction set includes both general-purpose computing instructions for managing the encoding process and DSP instructions for efficiently performing the iterative computations required by the discrete cosine transform, pixel averaging, and so on. In addition, the RSP has the ability to perform separate arithmetic operations on four bytes of data with a single instruction (single instruction, multiple data – SIMD).

The data and instruction caches provide single-cycle access to instructions and data for both the RSP and the Motion Estimator to ensure against processor stalls. Both the caches are filled directly from RAM by the DMA Controller, which operates under control of the RSP.

Video interfaces A and B control the flow of video data into and out of the VRP. Each interface has a 32x32 video FIFO (VFIFO) for buffering data on input and output. In addition, interface A has a decimation filter for reducing video resolutions from CCIR 601 to SIF.

The Motion Estimator is a 2 GigaOp/second coprocessor that compares predicted blocks against reference blocks and returns a motion vector and match score. The Motion Estimator can be configured to perform an exhaustive or a three- or two-level hierarchical search. All searches are refined to half-pel resolution, and the search range is configurable.

The host interface manages the transfer of data and control signals between the system host processor and the VRP. The DRAM interface generates controls signals needed to drive the external local DRAM array. The DRAM Controller supports fast page mode accesses of DRAM and includes a RAS-before-CAS refresh mechanism. A seven-channel DMA Controller manages the transfer of uncompressed and compressed video data between the video interfaces, and fills the instruction and data caches. The variable-length coder/decoder assists the CPU in the encoding and decoding of compressed bitstreams.

5.5 Typical Application

Figure 5-2 shows a typical digital authoring application using the CLM4500. The uncompressed video is fed to the CLM4500 from a standard video source such as a VTR. The CLM4500 performs the MPEG encoding based on parameters downloaded from the host computer. A video encoding technician uses the human assist station to maximize encoding efficiency and to add other multimedia features such as entry and exit points. The resulting MPEG encoded bitstream is written to a video file server or CD master.

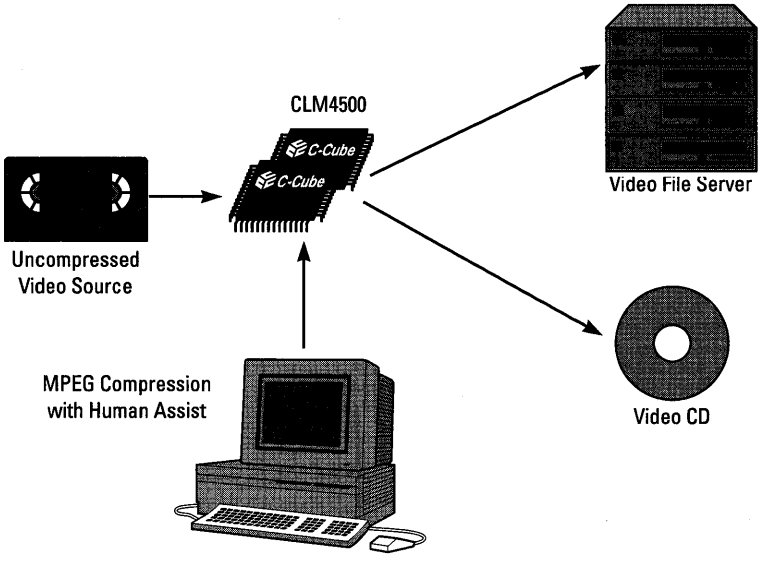
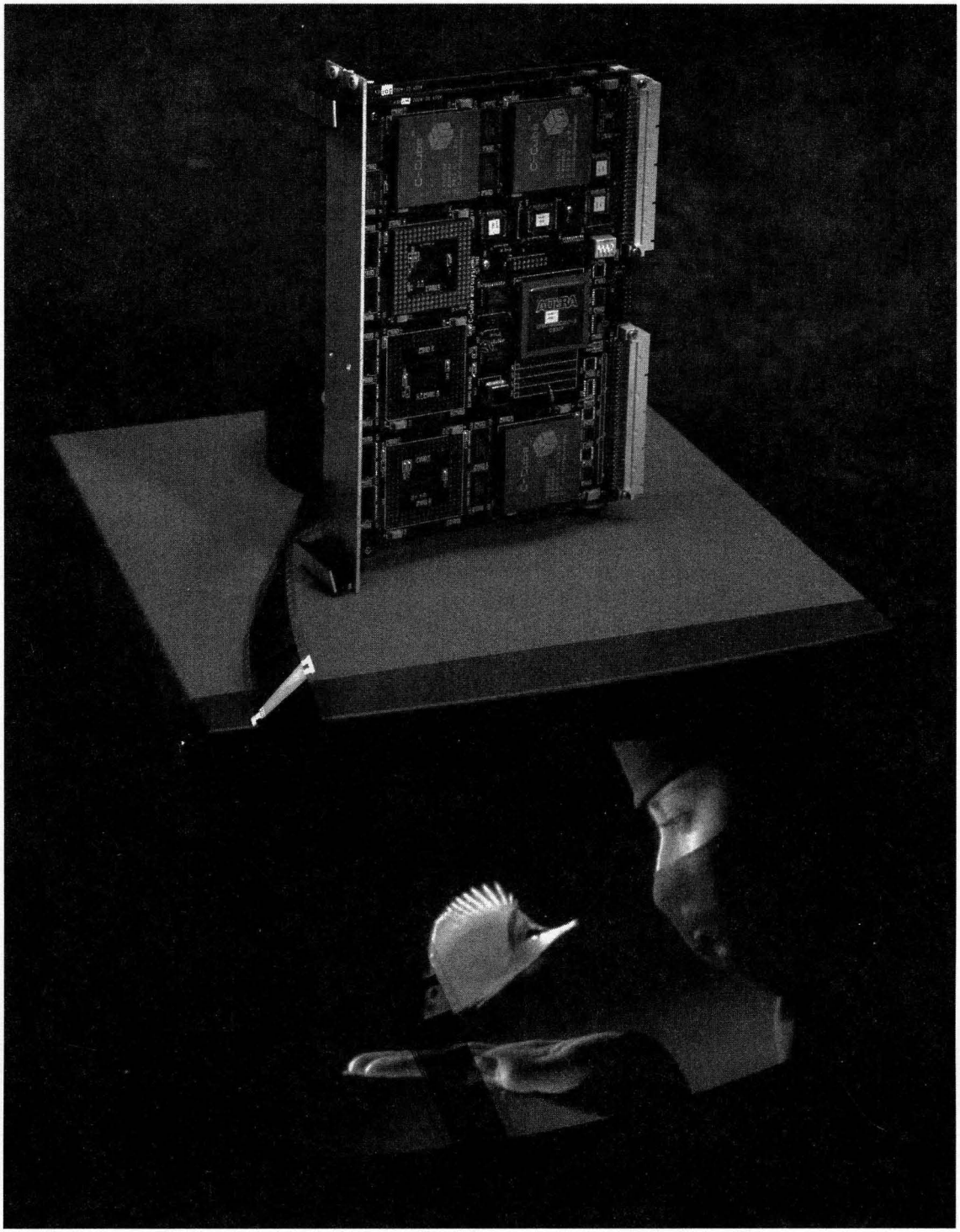


Figure 5-2 Digital Video Authoring Application Using CLM4500



The CLM4600 compresses digital video into MPEG syntax for broadcast applications.

6
CLM460x Broadcast MPEG Video Encoder

The CLM460x Broadcast MPEG Video Encoder compresses digital video into MPEG syntax in real time. Two version of the product are offered: the CLM4600 for NTSC video and the CLM4609 for PAL. Both products consist of C-Cube VideoRISC™ Processors (nine for the CLM4609 and 10 for the CLM4600) and a microapplication that implements C-Cube's patented MPEG video encoding algorithms. The CLM460x supports compressed data rates of from 3 to 10 Mbits per second while maintaining excellent image quality. Video at these data rates is suitable for distribution on medium-bandwidth media such as coaxial cable, terrestrial broadcast, and satellite broadcast, thus enabling applications such as:

- 500-channel cable systems
- Video on demand
- Automated ad insertion
- Direct broadcast from satellite

6.1 Features

The features of the CLM460x are:

- Real-time encoding of digital video into MPEG syntax at broadcast resolution
- Multiple video standards:
  - NSTC (CLM4600)
  - PAL (CLM4609)
- Multiple horizontal input resolutions:
  - 704, 544, 480, 352 pels
- Multiple frame rates
  - 29.97 Hz (NTSC, CLM4600)
  - 25 Hz (PAL, CLM4609)
  - 23.976 Hz (film, CLM4600)
- C-Cube's patented MPEG video encoding algorithm for high image quality
  - Sophisticated rate control
  - Sophisticated masking
- Highly integrated:
  - Nine (NTSC) or 10 (PAL) C-Cube VideoRISC Processors
  - CCIR 601 (TTL levels) video in, MPEG compressed video out
  - Interfaces to DRAM with no external logic
- Wide motion estimation search ranges with half pel accuracy
  - Predicted frames: -106/+99.5 pels horizontal, -58/+51.5 pels vertical
  - Bidirectional frames: -74/+67.5 pels horizontal, -58/+51.5 pels vertical
- Encoded bit rates from less than 3 Mbit/second to more than 10 Mbits/second
- Supports vectored interrupts of the host processor
- Complies with all requirements of the MPEG standard (ISO CD 11172)
  - Support for audio/video synchronization
  - Intra, predicted, and bidirectional frames

- Intraframe and reference distance (N and M) control
- Support for statistical multiplexing

6.2 MPEG Encoding Algorithm

The MPEG standard defines a syntax for the representation of compressed digital video. While the standard tightly defines the decoder, much latitude is given to the developers of encoding algorithms.

The key to the quality of MPEG encoded video is the ability of the encoder to intelligently "distribute" its data budget for encoding video between and within the frames of video being encoded. C-Cube's MPEG video encoding algorithm has sophisticated algorithms for masking and data rate control.

6.2.1 Masking

Harshly quantizing the AC coefficients from the DCT produces a compression artifact called ringing. In some areas of an image, for example, in foliage or gravel, ringing is difficult to see. In other areas, such as around an object silhouetted against the sky, ringing is very obvious. C-Cube's patented masking algorithm determines where ringing artifacts would be visible in an image, and budgets data accordingly.

6.2.2 Rate Control

One of the principal compression techniques employed by MPEG is motion estimation, the process of predicting from a previous or subsequent frame the contents of the current one. When there is little motion – and little change – between frames, the majority of the available data budget should be spent on reference frames (intra or predicted frames) to produce the highest quality. When there is rapid movement between frames, the budget should be distributed evenly between frames.

6.3 Functional Overview

This section describes the overall organization and operation of a CLM460x-based video encoding system, illustrated in Figure 6-1.

6.3.1 Organization

The organization of a video encoder based on the CLM460x is straightforward. Each of the CLM460x's 10 VideoRISC Processors (VRPs) has 2 Mbytes of DRAM, organized as two 256Kx32 pages, for working and microapplication storage. The VideoA, VideoB, and Host interfaces of

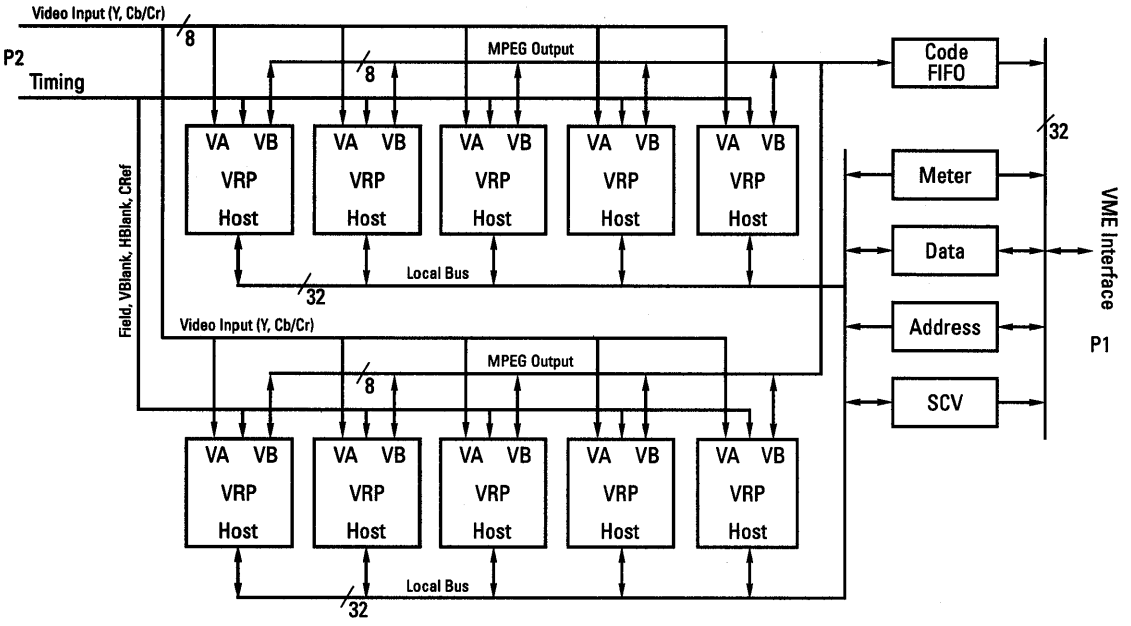


Figure 6-1 CLM460x-Based Video Encoding System

the VRPs are connected in parallel. Video is input via the VideoA interface in digital YCbCr format at a resolution of 708x480 pixels. The VRPs output the compressed video on the VideoB bus to the Code FIFO, a 1 Mbyte buffer from which the host can extract compressed MPEG video. The Local Bus connects the VRP host interfaces to four dual-ported registers accessible by the host:

- Meter: Maintains the Code FIFO fill level
- Data: Allows the host access to the Local Bus and the VideoRISC Processors access to the host bus
- Address: Allows the host to specify an address on the Local Bus
- SCV: This Status/Config/Vector register contains status information set by the CLM460x

6.3.2 Operation

The encoding operation is divided into five stages: capture, preprocess, motion estimation, encode and output. Each stage corresponds to a frame time, but all stages are executed in parallel. Each VRP processes

a portion of the video image, and the image is segmented horizontally as shown in Figure 2 (the image is segmented by nine for NTSC and by 10 for PAL).

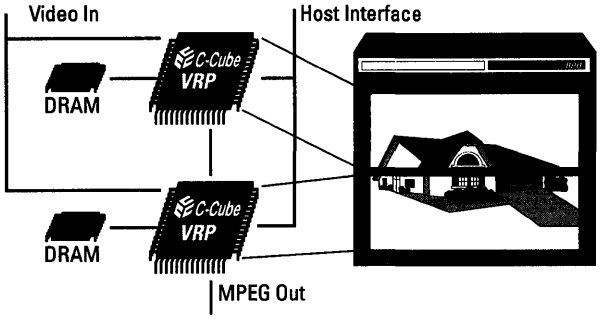


Figure 6-2 Scaled Image Processing

Capture

Each VRP captures its portion of the image from the VideoA bus and stores the image in its DRAM. At this stage, both fields of the input (480 or 576 lines) are preserved as input for the preprocess stage. The VRP's VideoA interface and DRAM controller perform the capture process in the background, allowing the VRP's RISC Signal Processor to operate on previously grabbed frames.

Preprocess

During the next frame time, the microapplication also makes an activity estimate on the image, which is used by the rate control algorithm for distributing the data budget.

Motion Estimation

During the third frame time, each macroblock of the current frame is compared with a reference frame to produce a motion vector and score.

Encoding

During the fourth frame time, each macroblock is processed, either into DCT format for intrablocks or into difference format for predicted blocks. The processed data is passed through the VLC and encoded data is stored in the VRP's DRAM.

Output

In the fifth frame time, the VRP outputs the compressed and formatted video via the VideoB interface. The output from the nine (or 10) VRPs is collated in the Code FIFO.

6.3.3 Application Program Interface (API)

The CLM460x allows the following parameters to be set when the encoder is started:

- Bit Rate – This seven-digit number sets the bit rate.
- GOP Size – 12 or 15
- Reference Distance – Number of frames between reference frames: 3 (three equals I, P, and two B frames)
- Virtual Buffer Verifier Size – In kilobits

The host instructs the encoder to start and stop encoding by setting and resetting a flag in the master VRP's DRAM.

Horizontal input resolution is determined by separate microapplication versions for 704, 544, 480, and 352 pels, all of which are included with the CLM460x product.

6.4 VideoRISC Processor (VRP)

The heart of the VRP is a 32-bit RISC Signal Processor (RSP) designed by C-Cube. As with other reduced instruction set computers (RISC), the RSP's instruction set uses a load/store model for accessing memory, while arithmetic operations use the 32 local registers to allow single-cycle execution of instructions. The RSP instruction set includes both general-purpose computing instructions for managing the encoding process and DSP instructions for efficiently performing the iterative computations required by the discrete cosine transform, pixel averaging, and so on. In addition, the RSP has the ability to perform separate arithmetic operations on four bytes of data with a single instruction (single instruction, multiple data – SIMD).

The data and instruction caches provide single-cycle access to instructions and data for both the RSP and the Motion Estimator to ensure against processor stalls. Both the caches are filled directly from RAM by the DMA Controller, which operates under control of the RSP.

Video interfaces A and B control the flow of video data into and out of the VRP. Each interface has a 32x32 video FIFO (VFIFO) for buffering data on input and output. In addition, interface A has a decimation filter for reducing video resolutions from CCIR 601 to SIF.

The Motion Estimator is a 2 GigaOp/second coprocessor that compares predicted blocks against reference blocks and returns a motion vector and match score. The Motion Estimator can be configured to perform an exhaustive or a three- or two-level hierarchical search. All searches are refined to half-pel resolution, and the search range is configurable.

The host interface manages the transfer of data and control signals between the system host processor and the VRP. The DRAM interface generates controls signals needed to drive the external local DRAM array. The DRAM Controller supports fast page-mode accesses of DRAM and includes a RAS-before-CAS refresh mechanism. A seven-channel DMA Controller manages the transfer of uncompressed and compressed video data between the video interfaces, and fills the instruction and data caches. The variable-length coder/decoder assists the CPU in the encoding and decoding of compressed bitstreams.

6.5 Typical Application

Figure 6-3 shows a typical system application of the CLM460x. In this application, video input is provided either from a video tape recorder (VTR) or a live feed via digital camera. The CLM460x encodes the video in real time and outputs an MPEG bitstream for uplink.

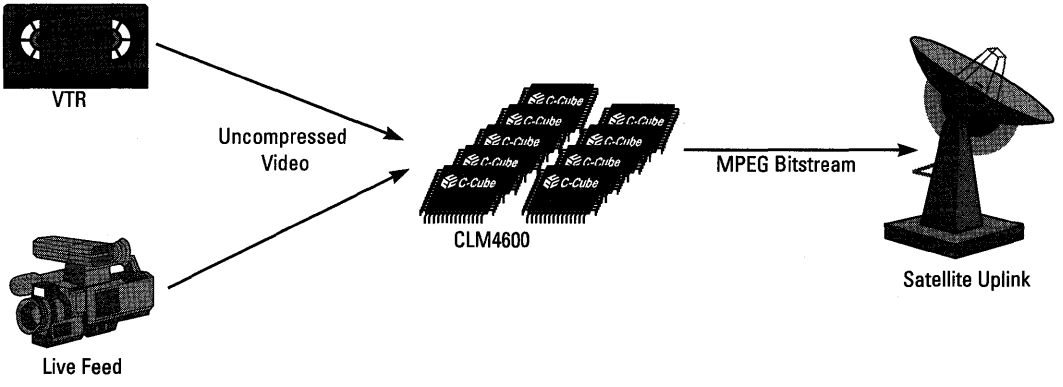


Figure 6-3 Uplink Application

The MPEG Encoder Development Station uses the CLM4600 to encode video and audio sequences into MPEG 1 syntax in real time.

7
MPEG Encoder Development Station

The VideoRISC MPEG Encoder Development Station provides the ability to encode video into MPEG syntax in real time and to develop MPEG encoding systems based on C-Cube's VideoRISC Processor (VRP), the first microprocessor designed to process video as a data type. The Development Station:

- Accepts both D1 digital video and several formats of analog video as input
- Encodes video at broadcast (704x480, NTSC; 704x576, PAL) or consumer (352x240, NTSC; 352x288, PAL) resolutions in real time at compressed data rates of 1 to 10 Mbits per second
- Makes the compressed video available for storage on disk or outputs it on a serial port
- Includes multiplexer software to combine the elemental video and audio streams into an MPEG system stream

The encoder development station also provides an MPEG audio encoder solution which:

- Accepts stereo analog audio or AES/EBU digital audio as input
- Encodes audio into MPEG Layer 1 or 2 format at compressed data rates of from 32 to 384 Kbits per second (as per the MPEG spec)
- Makes the compressed audio available for storage on disk

The Development Station supports C-Cube's VideoMAX MPEG Video Encoding algorithm, which allows the system to encode high-quality MPEG video at low data rates for both broadcast and consumer resolution applications.

While intended primarily for MPEG system development, the Development Station can also be used to encode video and audio for the following applications:

- Movies on CD
- Video on demand
- CD Karaoke
- Interactive video games
- Computer-based training
- Point-of-sale/information kiosks

7.1 Features

The VideoRISC Encoder Development Station has the following features and associated benefits:

- Encodes video and audio into MPEG 1 syntax in real-time
- Supports broadcast-resolution video encoding (CCIR 601)
  - 704 x 480, 352 x 480 (NTSC)
  - 704 x 576 (PAL)
- Supports consumer-resolution video encoding (SIF)
  - 352 x 240 (NTSC)
  - 352 x 288 (PAL)
  - 320 x 240 (square pixel)
- Supports multiple frame rates: 29.97 (NTSC), 25 (PAL), 23.976 (film)
- Supports digital and analog video I/O
  - CCIR 601 digital parallel input

- YUV, S-Video, composite analog inputs
- Composite, S-Video outputs

- Uses C-Cube's VideoMAX MPEG video encoding algorithm for high image quality
  - Sophisticated rate control and masking
  - Adaptive field/frame filtering
- Supports encoded bit rates from less than 1 Mbit/second to more than 10 Mbits/second
- Provides simple, "point-and-click" encoder control
  - Start/stop encoding by timecode
  - Encoder status
- Complies with all requirements of the MPEG standard:
  - Support for audio/video synchronization
  - Intra, predicted, and bidirectional frames
  - Complete intra and reference distance (N and M) control
- Supports real-time MPEG audio encoder
  - MPEG Layer 1 and Layer 2 Audio
  - AES/EBU digital input or analog input
  - Audio/Video multiplexer software
- Performs inverse 3-2 pulldown to eliminate redundant fields in telecined film (SIF resolution only)
- Can be upgraded to MPEG 2

7.2 Functional Description

The VideoRISC Encoder Development Station is housed in a VME-based platform that consists of the elements listed below and shown in Figure 7-1.

- Tower system
- MPEG Video Encoder (2 boards)
- Audio Encoder Board
- Video I/O Board
- Serial Board

See the following sections for more details on these components.

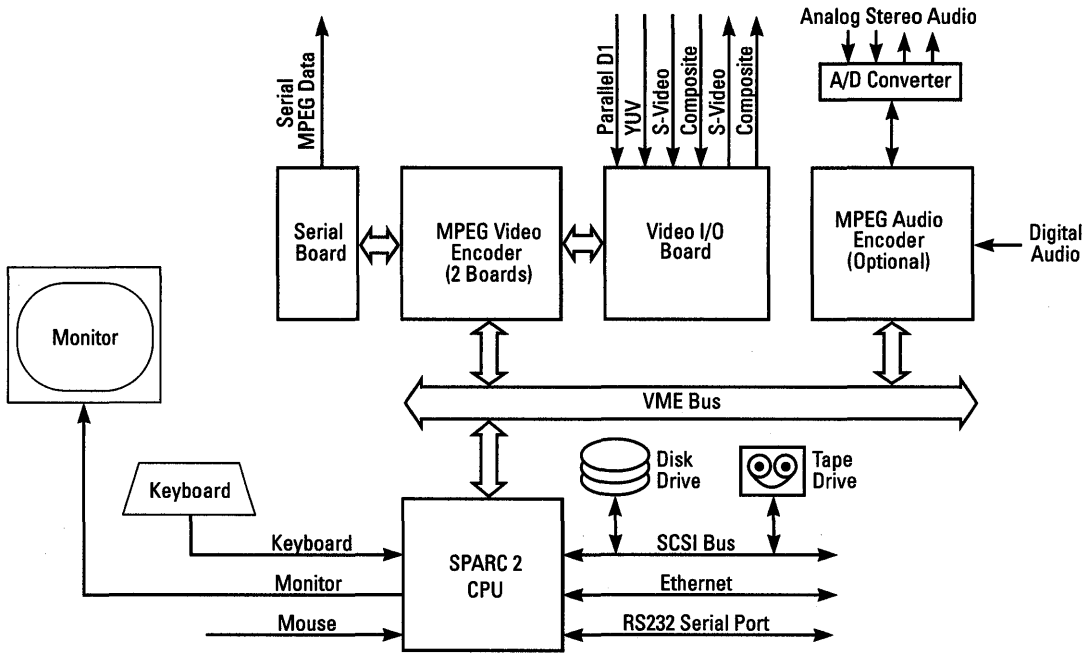


Figure 7-1 VideoRISC Encoder Development System Block Diagram

7.3 Tower System

The Tower System has the following features:

- One SPARC 2 CPU (two boards)
- SCSI Peripherals
- Color graphics system
- 6U VME chassis

Each is described in detail in the following sections.

7.3.1 SPARC 2 CPU (two boards)

The SPARC 2 CPU is the functional equivalent of a SPARCstation 2 on a single 6U VME board. As such, the SPARC 2 CPU includes a SPARC Integer Unit, Floating Point Unit, SCSI Controller, Ethernet Interface, Floppy Controller, Audio port, Keyboard port, and on-board DRAM (32 Mbytes for master, 16 Mbytes for slave). The SPARC 2 CPU provides binary compatibility with the SPARCstation 2 and runs current

versions of SunOs/Solaris and the over 4,000 shrink-wrapped SPARCware applications available today.

7.3.2 SCSI Peripherals

The Tower chassis includes a high-performance 2-Gbyte SCSI Disk Drive in a half-height 5.25-inch form factor and a 535 Mbyte system disk. The disk drive provides adequate capacity for real-time and non-real-time MPEG encoding, both of which require substantial storage space.

> *Note: Full-length motion-picture encoding requires at least 8 GBytes, which C-Cube sells as an optional upgrade.*

The Tower also includes a 2-Gbyte 8-mm Tape Drive, which provides a means for data exchange, software distribution, and hard disk backup. In addition, 8 mm tapes are commonly used to store CCIR 601 format video data from digital disk recorders such as the Abekas 60 series.

7.3.3 Color Graphics System

The system includes a SBus Color Frame Buffer and 17-inch Nanao monitor. The Frame Buffer provides a resolution of 1152 x 900 pixels with a color resolution of 8 bits (256 colors from a palette of 16 million colors).

The Nanao Monitor is a high-resolution, multisync monitor with a flat screen that provides a sharp, flicker free display for low user fatigue.

7.3.4 6U VME Chassis

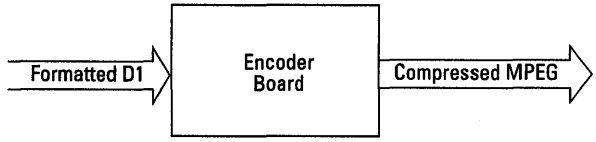
The chassis is a tower enclosure which includes a 7-slot VME backplane, a 350 watt power supply, plus mounting support for four full-height or eight half-height 5-1/4" devices. The compact cabinet occupies only 7.43 inches of horizontal floor space, is 23.5" deep, and 26.25" high.

The backplane, power supply, and drives are mounted as modular units that are easily removed and installed. All power supply connections for the front panel, backplane, and installed peripherals are pluggable. This modular design ensures convenient servicing and maintenance.

7.4 MPEG Video Encoder

The MPEG Video Encoder consists of two 6U VME boards configured as a single assembly and populated with 10 C-Cube VideoRISC Processors. The Video Encoder is the processing element of the VideoRISC Encoder Development Station.

Shown in its functional simplicity below, the Video Encoder is a programmable, multi-processor system that accepts digital video input and produces compressed video at a variety of bit rates in the MPEG compression format.



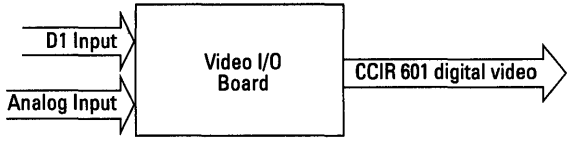
7.5 Audio Encoder Board

The Audio Encoder Board, pictorially simplified below, is a VMEBus 6U card designed to compress stereo analog or digital audio input into MPEG Layer 1 or 2 format in real time. The digital input supports both SP/DIF and AES/EBU formats. Both interfaces support audio sampling rates of 32, 44.1 and 48 KHz and provide 16-bit resolution.

7.6 Video I/O Board

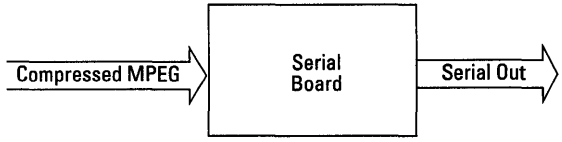
The Video I/O Board is a 6U VME board designed to connect the Development Station to a variety of video tape players. The I/O board accepts video as parallel D1 or as analog YCbCr, S-video or composite and outputs it as CCIR 601 digital video.

The board converts the D1 input from ECL to TTL voltage levels, demultiplexes the data, and passes the digital YCbCr format data to the encoder board. The analog section of the board converts NTSC, PAL or SECAM analog signals to YCbCr digital video.



7.7 Serial Board

The Serial board, pictorially simplified below, accepts a serial MPEG compressed bitstream and delivers the data to the external C-Cube decoder board for decoding. It consists on an RS422-like transceiver, serial to parallel converter, and a FIFO.



7.8 Functional Applications

The VideoRISC Encoder development system supports video encoding in either of the following two modes of resolution:

7.8.1 Consumer-Resolution (SIF)

When in SIF mode, the Encoder development system converts the CCIR 601 resolution input video to either 352x240 (NTSC), 352x288 (PAL) or 320x240 (square pixel), and encodes the video into MPEG syntax at data rates from less than 1 Mbit/second to 5 Mbits/second. For NTSC material that originated as 24 Hz film, the encoder provides an inverse telecine filter to remove the redundant fields, returning the material to its original frame rate before encoding.

The full intra, predicted, and bidirectional frame structure of MPEG is supported, with complete GOP size and reference distance control. For motion estimation, the encoder supports search ranges of ±48 horizontal and ±24 vertical pels for predicted frames, and ±32 horizontal and ±16 vertical pels for bidirectional frames, both with 1/2 pel accuracy.

7.8.2 Broadcast Resolution (CCIR 601)

When in CCIR 601 mode, the Encoder development system supports an encoded resolution of 576 lines for PAL (25 frames/second) and 480 for NTSC (29.97 frames/second), representing the maximum number of active lines for each standard. For both standards, two horizontal resolutions are supported: 704 and 352. At broadcast resolutions, the encoder supports data rates of 3 to 10 Mbits/second with full intra, predicted, and bidirectional frame support. For motion estimation, the encoder supports search ranges of -106/+99.5 horizontal and -58/+51.5 vertical pels for predicted frames, and -74/+67.5 horizontal and -58/+51.5 vertical pels for bidirectional frames, both with 1/2 pel accuracy.

For whichever encoding resolution is chosen, the Encoder development system enables the development of applications that perform one of the following three types of encoding:

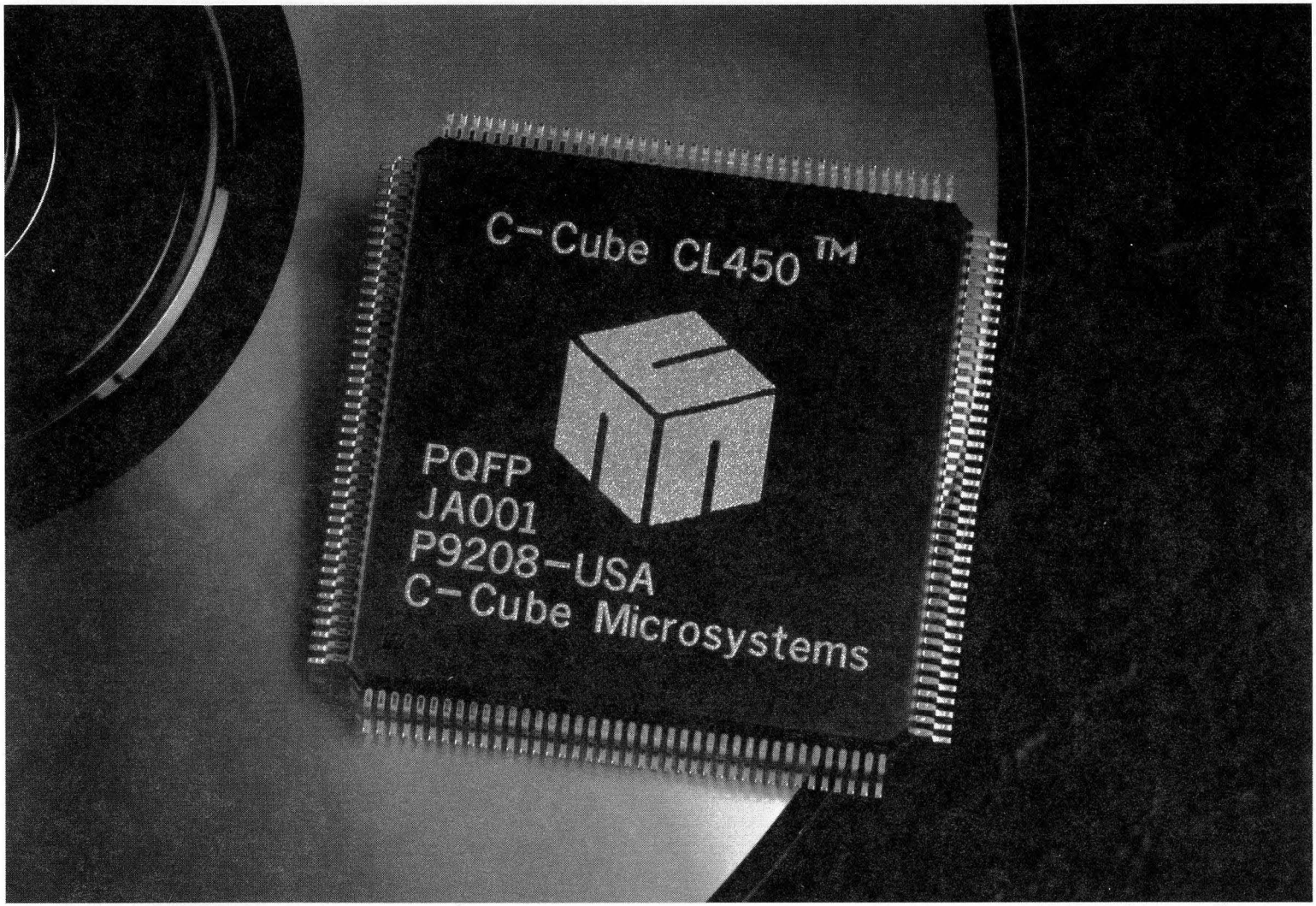
- *Real-time encoding and decoding of video* - In this application, video is input to a frame buffer on the Video I/O board. The VRP on the Encoder board then compresses the video data from the frame buffer and outputs it to serializer board. Data is then sent from the serializer board of the RT Encoder Development to a deserializer board on the MPEG Video Lab for real-time decompression (playback). Note: Use of this system requires the separate purchase of the MPEG Video Lab.
- *Real-time encoding of video to a disk* - In this application, video is input to a frame buffer on the Video I/O board. The VRP on the Encoder board then compresses the video data from the from the frame buffer and outputs it to a hard disk.
- *Real-time encoding of audio to a disk* - In this application, audio data (in either stereo analog or digital format) is input to the Audio Encoder Board and compressed into MPEG Layer 1 or 2 format in real time before being output to a hard disk.

  The MPEG Audio Encoder includes MPEG system multiplexer software (an offline utility) which combines the elemental video and audio streams into an MPEG system stream.

7.9 Documentation

The encoder system is supplied with these manuals:

- *VideoRISC Encoder Development Station User's Manual*
- *VideoRISC Processor Hardware User's Manual*
- *SPARC User's Guide*
- *SPARC System and Network Manager's Guide*



The CL450 MPEG Video Decoder provides full-motion video capability for cost-sensitive electronics products.

8
CL450 MPEG Video Decoder

8.1 General Description

The C-Cube CL450™ MPEG Video Decoder is designed to provide full-motion video capability for cost-sensitive consumer electronics and computer products. The CL450 decompresses SIF-resolution MPEG bitstreams in real time. SIF resolution is 352 x 240 pixels at 30 Hz or 352 x 288 pixels at 25 Hz. Compressed data rates of 1.2 to 3 Mbits per second are typically used for SIF resolution.

The CL450 interpolates decompressed pictures horizontally (normally from 352 to 704 pixels per scan line) before outputting them. The CL450 outputs decompressed pictures multiple times to increase the frame rate from 24, 25, or 30 Hz (coded frame rate) to the selected 50 or 60 Hz display frame rate. The CL450 can position decompressed pictures relative to its $\overline{\text{HSYNC}}$ and VSYNC inputs. This positioning combined with the image cropping function allows useful windowing operations to be performed. The CL450 by default can automatically center the MPEG video on the display screen regardless of its coded resolution.

The CL450 is a programmable MPEG decoding engine. To complete a decoding system, the CL450 must be used with the microapplication

provided by C-Cube. The current microapplication, version 2.0, provides features including advanced error handling (important for Video CD), new interrupts for interactive games, and enhanced macro commands for "trick play" product features.

8.2 CL450 Hardware Features

Some of the key features of the CL450 hardware are:

- Fully complies with all requirements of the MPEG standard (ISO CD 11172) with no syntax limitations
- Performs real-time decoding of SIF-resolution bitstreams (352 x 240 pixels at 30 Hz or 352 x 288 pixels at 25 Hz)
- Performs real-time horizontal pixel interpolation and frame duplication to produce output formats of 704 x 240 pixels at 60 Hz or 704 x 288 pixels at 50 Hz
- Provides either RGB or YCbCr video output using the on-chip color space converter
- Selectable border color
- Supports NTSC and PAL video timing formats
- Interfaces to 680x0 processors and DRAM with no external logic
- Hardware byte swapping supports Intel and Motorola byte ordering
- Requires only 4 Mbits of 80-ns DRAM for all decoding resolutions and bit rates
- High-performance DRAM interface allows decoding of worst-case bitstreams
- Provides automatic high-level hardware and firmware support for audio/video synchronization
- Internal 90-kHz system synchronization timer
- Decodes Huffman variable-length codes at a peak rate of 4 bits per clock (160 Mbits/second at 40 MHz) providing excellent scanning, error concealment, and handling of worst-case bitstreams
- Allows the active window to be positioned relative to $\overline{\text{HSYNC}}$ and VSYNC inputs with one-pixel accuracy
- Displays all or part of decompressed pictures; displayed section can be selected to one-pixel accuracy (within the decoded picture)

and can be changed every coded frame for panning motion video

- Supports transparent host access of local DRAM
- Supports both programmed I/O and DMA transfers of compressed bitstreams from the host
- Up to four independent clock inputs
- Fabricated in a cost-effective 0.8-micron CMOS process
- Supplied in a 160-pin plastic quad flat-pack (PQFP)

8.3 Microapplication Features

The CL450's microapplication provides very high-level functionality which keeps the overall system design as simple as possible. The CL450 automatically processes all layers of the MPEG video standard without assistance. Additionally a simple mechanism for passing system-layer timestamps allows the CL450 to synchronize automatically. Features implemented by the microapplication include:

- Bit rate up to five Mbits per second
- Transcoding between NTSC and PAL frame rates
- System memory expansion capability
- Support for 24 Hz film format including 3:2 pulldown telecine
- Advanced error concealment, both signaled and unsignaled
- MPEG double-resolution still pictures
- Forward and reverse high-speed scanning capability
- Automatic parsing of sequence parameters. Stored parameters available to host.
- Synthesis of PTS and DTS values automatically
- Immediate synchronization recovery after bitstream error concealment
- Uninterrupted display during input data underflow

The host system controls the CL450 by issuing macro commands. The CL450 buffers these commands in an internal macro command FIFO. The CL450's set of 18 high-level commands enables advanced features with low system complexity. Table 8-1 summarizes the CL450's macro commands.

Table 8-1 Macro Command Summary

Category	Priority	Name	Description
Set-type	Low	SetBlank()	Blanks/unblanks output window
		SetBorder()	Sets output window location
		SetColorMode()	Enables/disables color-space converter
		SetInterruptMask()	Enables/disables interrupts to host
		SetThreshold()	Specifies bitstream buffer emptiness
		SetVideoFormat()	Configures output resolution and timing
		SetWindow()	Sets output window size and contents
Play-type	Low	DisplayStill()	Decodes/displays single still picture[1]
		Pause()	Keeps last picture on display
		Play()	Decodes and displays at normal rate
		Scan()	Decodes and displays next single I-picture
		SingleStep()	Decodes and stores next single picture
		SlowMotion()	Decodes and displays at slower rate
Control	High[2]	AccessSCR()	Reads or writes internal SCR counter
		FlushBitstream()	Discards contents of bitstream buffer
		InquireBufferFullness()	Measures data in bitstream buffer
		NewPacket()	Manages bitstream data
		Reset()	Reinitializes CL450 and its microcode

1. Allows display of a still image with double vertical resolution.
2. Except for NewPacket()

8.4 Interrupt Support

The CL450 has a single external interrupt signal, $\overline{\text{INT}}$, which can be used to interrupt the system's host processor during events of interest. Since the CL450 is completely self-sufficient during decoding, the use of interrupts is completely optional. Thus, the simplest players will not use them at all. However, game players and systems with advanced features will require interrupts for complex interactive control.

The CL450 currently has 11 logical interrupts which can be enabled and disabled independently at any time. An interrupt status register is provided to allow the host to determine which interrupts have occurred when more than one interrupt type is enabled. Table 8-2 summarizes the CL450's interrupts.

Table 8-2 CL450 Interrupt Summary

Category	Name	Event	Mask Bit
Decode-time	END-D	`sequence_end_code` found	5
	ERR	Bitstream data error	0
	PIC-D	New picture decoded	6
	SEQ-D	`sequence_header_code` found	9
	SCN	Picture decode complete in Scan()	11
	UND	Bitstream buffer underflow error	8
VSYNC	END-V	Last picture display before `sequence_end_code`	4
	GOP	First I-picture display after `group_start_code`	2
	PIC-V	New picture display	1
	SEQ-V	First I-picture display after `sequence_header_code`	3
Display-time	RDY	Ready for data	10

8.5 Functional Description

Figure 8-1 shows a block diagram of the CL450, which has three interfaces:

- *The host interface*: Connects directly to 680x0 processors with no external logic. It can also be easily connected to 80x86 or popular microcontrollers.
- *The DRAM interface*: Reads and writes the local DRAM with no external logic.
- *The video interface*: Outputs pixel data to a video monitor or other video processing device.

The host computer supplies compressed data via the host interface. The CL450 buffers up to 16 coded data words in an internal coded data FIFO from which the data words are read by the DRAM controller and written into the bitstream buffer in the local 4 Mbit DRAM.

The central processing unit interprets high-level macro commands issued by the host processor. During normal play, bitstream data is read from the DRAM buffer and written to the Huffman variable-length decoding engine. The coefficients are zigzag scanned into a matrix buffer in the CPU and inverse quantized. The CPU then performs a two-di-

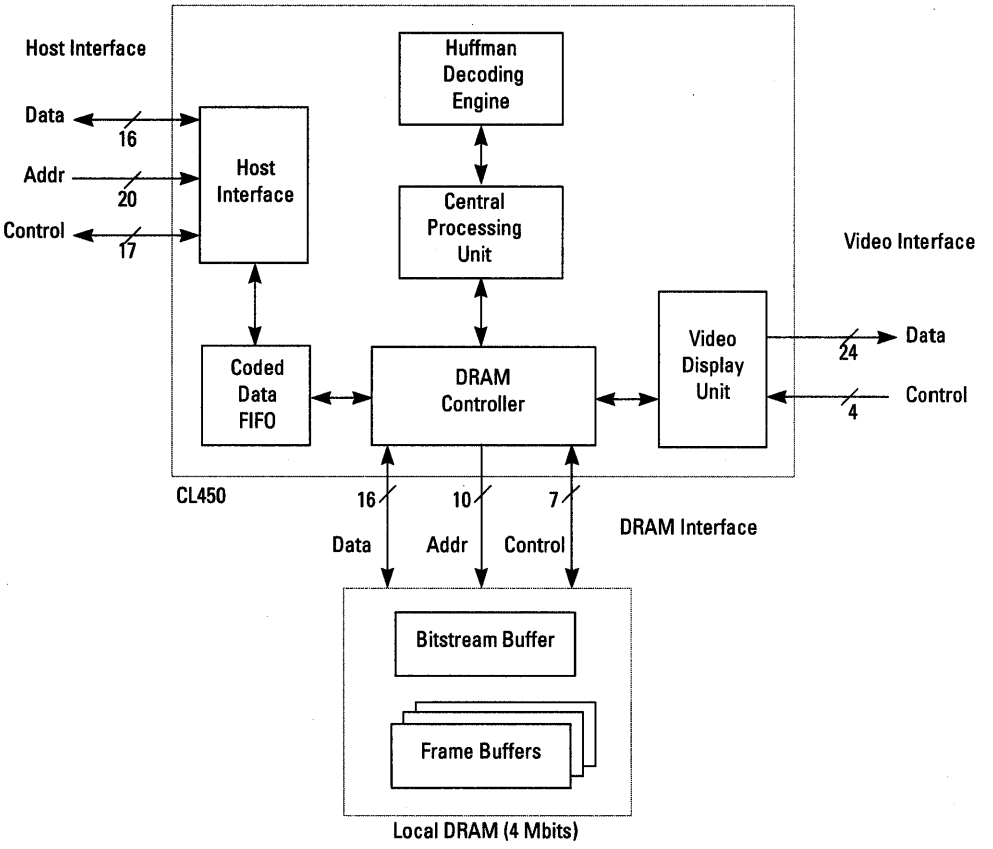


Figure 8-1 Block Diagram of the CL450

mensional IDCT before fetching reference pictures (P- and B- frames) which are combined for motion compensation. Reconstructed picture data is written into a frame buffer in the local DRAM.

The video display unit reads decompressed pixel data from the frame buffer for each field display, sends it through the color space converter if necessary, and outputs the pixel data on the video bus.

8.6 Typical Applications

The CL450 family of products are designed for low-cost consumer and computer applications such as

- Video CD systems
- Multimedia computers
- Karaoke video systems
- Full-motion interactive game players
- PC games
- Video on demand
- Point-of-sale/information kiosks
- Interactive TV

Figure 8-2 shows the CL450 in a typical system application.

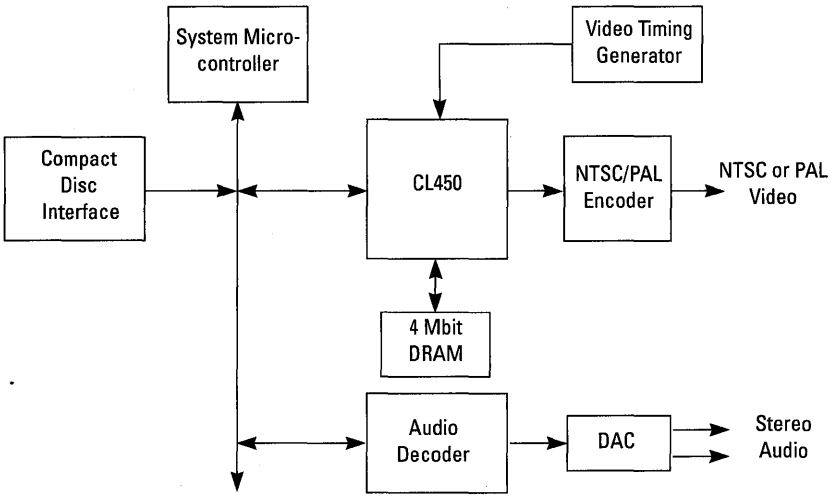
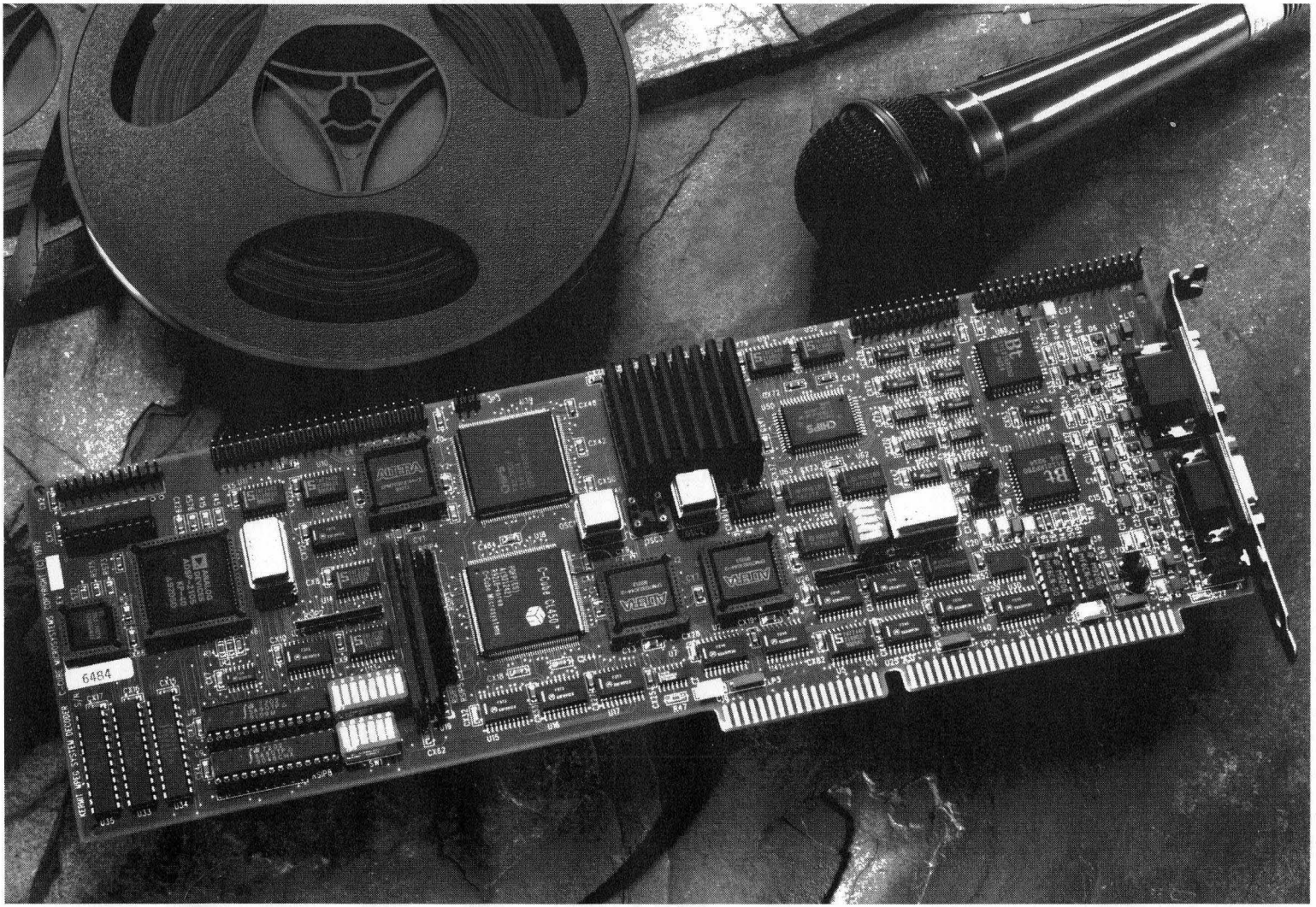


Figure 8-2 Typical CL450 System Application



The CL450 Development Board, an ISA-bus implementation of the CL450 MPEG Video Decoder.

9
CL450 Development Kit

The C-Cube CL450 Development Kit contains all the software and hardware needed to transform a 386- or 486-based personal computer with Microsoft® Windows™ 3.1 into a complete MPEG-based audio/video development system for the C-Cube Microsystems CL450. The kit is a vehicle for hardware and software developers wishing to prototype application environments and gain hands-on familiarity with the CL450 and video compression system design issues.

The CL450 Development Board is an ISA-bus (IBM PC-AT bus) card whose basic functionality derives from two chips: the C-Cube CL450™ MPEG Video Decoder and the Chips and Technologies PC Video™ 82C9001A Window Controller. The software includes the demonstration program WINPLAY.EXE and dynamic link libraries (DLLs) for the CL450 and PC Video chips.

When integrated into a personal computer, the CL450 Development Kit:

- Provides full-motion video and audio decompression of MPEG files from the system hard disk

- Displays video on a VGA monitor with windowing, zooming, and chroma-keying
- Displays decompressed video on an external RGB monitor
- Directly drives an external stereo amplifier
- Supports video/audio synchronization using system clock references and display timestamps
- Provides a development and debugging tool for CL450 developers

9.1 Typical System Application

Figure 9-1 shows how the CL450 Development Board is used in a typical system application. During playback, the CPU reads the MPEG compressed stream from the system hard disk. An application program called the system decoder decodes the system layer of the MPEG stream to extract the timing information needed to synchronize the audio and video outputs. The system decoder also demultiplexes the audio and video streams to create the inputs for the CL450 Development Board. The input streams are sent to the CL450 Development Board across the ISA bus.

In the application shown, the board drives two monitors. The VGA monitor displays the signal from the VGA board with the decompressed MPEG file overlaid in a video window. The RGB monitor displays the decompressed file at full-monitor size. The audio speaker plays the audio output synchronized to the video outputs.

9.2 Product Components

The CL450 Development Kit includes the following items:

- CL450 Development Board: An ISA-bus full-length card that plugs into any 16-bit slot in the host computer system.
- Feature connector cable: The CL450 Development Board connects to the VGA board's feature connector.
- Documentation, including:
  - *CL450 Development Kit User's Manual* (this manual)
  - *C-Cube CL450 MPEG Decoder User's Manual*
  - *Chips and Technologies PC Video data sheet*
- Software diskette #1 containing:

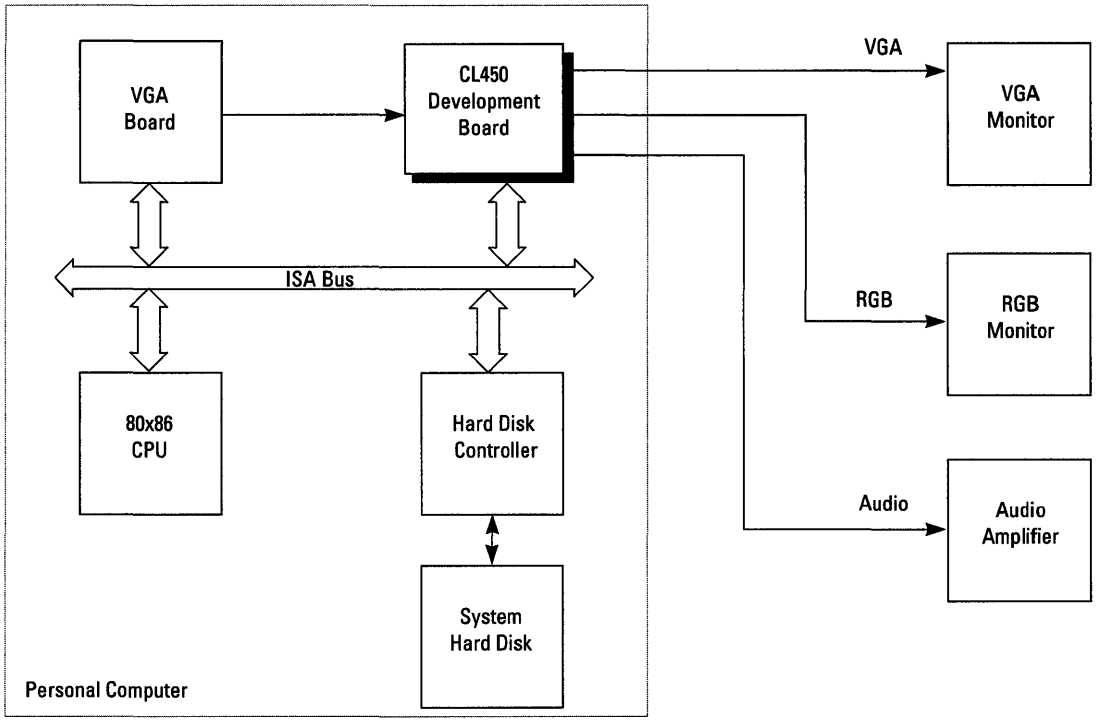


Figure 9-1 Typical System Application

- ☐ Binary code for CL450.DLL, a dynamic link library containing functions used to control the CL450.
- ☐ Binary code for PCVIDEO.DLL which contains the functions used to control the PC Video chip. (Contact Chips and Technologies for information about obtaining source code for PCVIDEO.DLL.)
- ☐ Binary code for WINPLAY.EXE, a sample application program in C running under Microsoft Windows 3.1.

- ☐ Software diskette #2 containing a sample bitstream.
- ☐ Software diskette #3 containing DOSPLAY.EXE and source code for the DOSPlay application and the CL450.DLL libraries and the PCVIDEO.DLL libraries.

C-Cube Microsystems also offers a manufacturing kit which includes everything in the CL450 Development Kit plus Gerber files for the printed circuit board design. Contact your local sales office for more information.

9.3 Hardware Overview

Figure 9-2 shows a simplified block diagram of the CL450 Development Board. The sections below explain the main functions of the board.

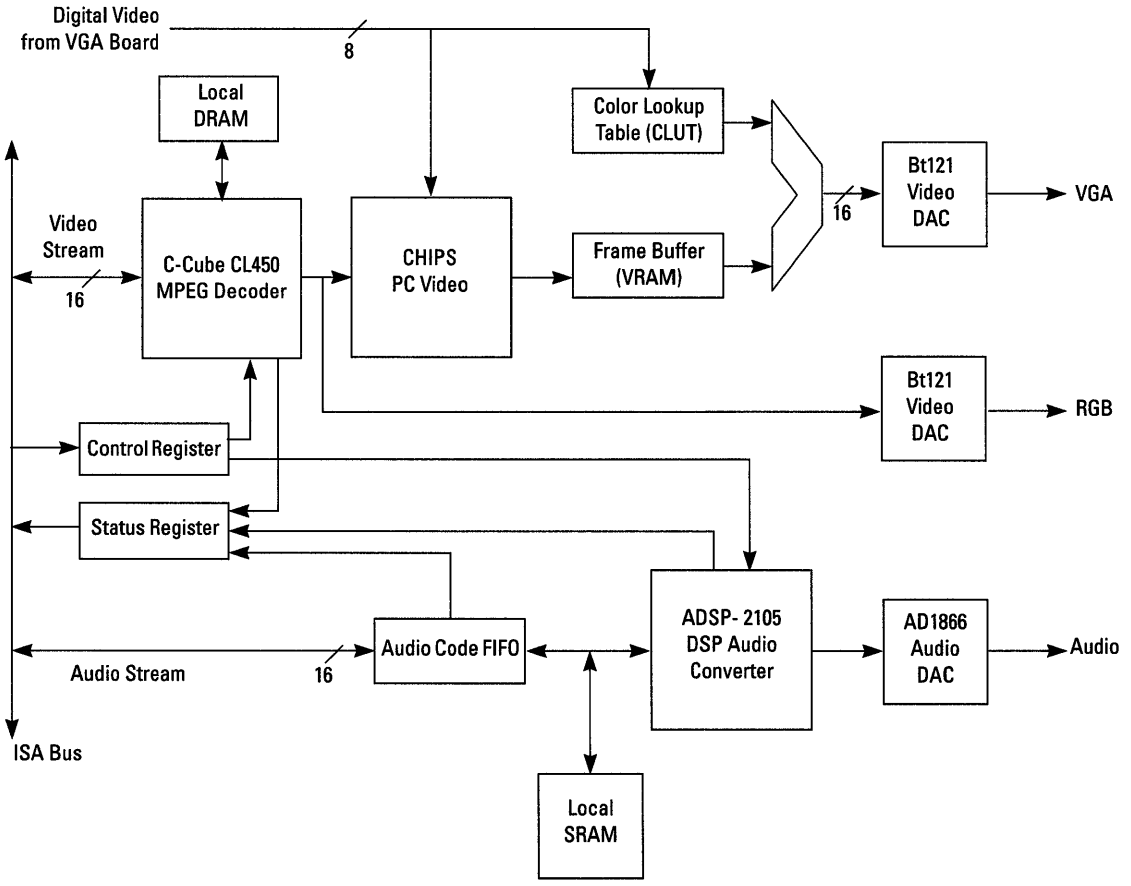


Figure 9-2 Block Diagram of CL450 Development Board

9.3.1 Board Inputs

The CL450 Development Board has three inputs:

- Digital VGA signal
- MPEG compressed video
- MPEG compressed audio

The system VGA board or subsystem supplies the digital VGA signal to the board via the feature connector. The system CPU (typically an 80x86 microprocessor) interprets and demultiplexes the combined MPEG file to produce separate MPEG audio and video compressed data bitstreams. It then transfers these bitstreams to the board across the ISA bus.

9.3.2 Video Data Decompression

The C-Cube CL450 MPEG Video Decoder decompresses MPEG I-compliant compressed data in real time at rates up to 5 Mbits per second. It uses a local 4 Mbit DRAM to buffer the input data and decompressed video frames. The CL450 then outputs the decompressed video frames in RGB format to the input of the PC Video chip.

9.3.3 Video Windowing

The Chips and Technologies (CHIPS) PC Video Windowing Controller scales and sizes the decompressed video frames and writes the resulting data into a frame buffer. The PC Video chip also controls a multiplexer that overlays the scaled and sized video onto the VGA image from the VGA board. The CHIPS 82C411 Color Lookup Table (CLUT) translates the input VGA into true-color data using an internal palette table.

9.3.4 Video Output

Two video outputs are available: a VGA output with the decompressed MPEG image overlaying the VGA display, and an RGB output of the decompressed MPEG image. Each of these outputs is driven by a Brooktree Bt121 Triple VIDEODAC™.

9.3.5 Audio Data Decompression

The Analog Devices ADSP-2105 Audio Decoder decodes the MPEG layer II stereo audio data. It supports a sampling frequency of 44.1 KHz with bit rates of 96 to 128 kbits per second per channel. The output of the audio converter is connected to an Analog Devices AD-1866 Audio

DAC which produces an analog audio output. This is a high-impedance output which can directly drive headphones, but must be amplified before it can drive speakers.

9.4 Software Overview

The operating system software should be Microsoft MS-DOS™ 5.0 and Windows 3.1. The dynamic link libraries, CL450.DLL and PCVIDEO.DLL, are supplied with the development kit in binary format. The application software program, WINPLAY.EXE, uses the operating system functions of Windows and makes function calls to the DLLs. WINPLAY.EXE uses files with extensions of .MPG, .VBS and .SCR. Files with a .MPG extension are MPEG I-compliant files containing multiplexed audio and video data. Files with a .VBS extension are MPEG compressed files with video data only. Files with a .SCR extension are ASCII text files that can contain a list of .MPG and .VBS files. The WinPlay program plays the files in the list in that sequence.

DOSPlay is an application similar to the WinPlay program, except that it runs directly under DOS and does not need Windows. DOSPlay is provided as both executable binary files, and as source code written in C.

C-Cube's MPEG Video Lab decodes and previews MPEG bitstreams at up to 8 megabits per second.

10
MPEG Video Lab

The MPEG Video Lab provides the tools needed to decode and preview MPEG bitstreams at bit rates up to 8 Mbits per second. It supports these video formats:

- NTSC: from 352 x 240 to 704 x 480 at 30 Hz
- PAL: from 352 x 288 to 704 x 576 at 25 Hz

The MPEG Video Lab supports RGB video output format.

This chapter describes the components of Video Lab and discusses the documentation and sample bitstreams provided with the MPEG Video Lab.

10.1 Video Lab Components

The basic MPEG Video Lab system shown in Figure 10-1 is based on the HP NetServer 4/33 LM personal computer, which uses the EISA bus. The standard configuration includes the following components (supplier is Hewlett-Packard except where noted otherwise in parentheses):

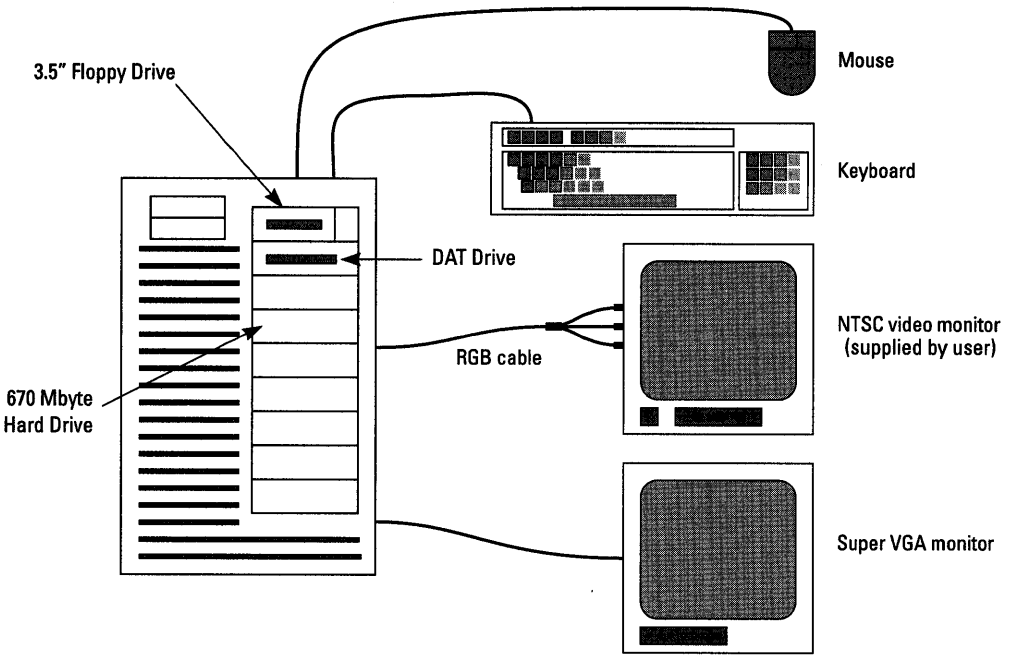


Figure 10-1 Video Lab Components

- 32 Mbytes RAM
- Super VGA monitor
- Extended keyboard with 101 keys
- Two-button mouse
- Floppy disk drive: 3.5-inch, 1.44 Mbyte capacity
- SCSI hard disk: 1 Gbytes unformatted (Micropolis 2210)
- DAT tape drive: 2 Gbytes (Maynard® MaynStream®)
- Super VGA graphics card
- MPEG CL950 Video Decoder Board (C-Cube Microsystems)
- MPEG CL450 Video Decoder Board (C-Cube Microsystems)
- Board driver software (C-Cube Microsystems)
- Ethernet card (3Com W/RG58)
- PC-NFS networking software (Sun Microsystems)

- Serial Receiver card (C-Cube)
- MS-DOS® 5.0 and Windows® 3.1 (Microsoft®), with Windows running in 386 extended mode
- Sample bitstreams
- Complete documentation

10.2 Sample Bitstreams

C-Cube Microsystems supplies a variety of sample bitstreams with Video Lab to demonstrate the basic operation of the system for a range of resolutions. You can use these bitstreams for demonstrations and product development.

10.3 Video Lab Documentation Set

C-Cube's *MPEG Video Lab User's Guide* is the primary source of the information needed to operate Video Lab. However, you may need to refer to manuals that provide more detailed information about some of the MPEG Video Lab components. C-Cube Microsystems supplies with the MPEG Video Lab a complete set of documentation for all the major components in the system. The manuals supplied with the MPEG Video Lab are listed below.

- *Installing and Managing Your HP NetServer LM Series* (Hewlett-Packard)
- *MaynStream DOS User's Manual* (Maynard)
- *MS-DOS 5.0 User's Guide & Reference* (Hewlett-Packard)
- *MS-DOS 5.0 Getting Started* (Hewlett-Packard)
- *Windows User's Guide* (Microsoft)
- *Windows Questions & Answers* (Microsoft)

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Technical Publications Department
C-Cube Microsystems
1778 McCarthy Boulevard
Milpitas, CA 95035

phone: (408) 944-6300
fax: (408) 944-6314

e-mail: techpubs@c-cube.com

North American Representatives

Alabama

M^2I
1910 Sparkman Avenue
Huntsville, AL 35816
phone: 205-830-0498
fax: 205-837-7049

Arkansas

TL Marketing
14850 Quorum Dr., Suite 100
Dallas, TX 75240
phone: 214-490-9300
fax: 214-960-6075

California

Bager Electronics
519 Encinitas Blvd.
Encinitas, CA 92024
phone: 619-632-8816
fax: 619-632-8810

Bager Electronics
17220 Newhope Street, Suite 209
Fountain Valley, CA 92708
phone: 714-957-3367
fax: 714-546-2654

Bager Electronics
6324 Variel, Suite 314
Woodland Hills, CA 91367
phone: 818-712-0011
fax: 818-712-0160

Norcomp
2140 Professional Drive, #200
Roseville, CA 95661
phone: 916-782-8070
fax: 916-782-8073

Norcomp
1267 Oakmead Parkway
Sunnyvale, CA 94086
phone: 408-733-7707
fax: 408-774-1947

Colorado

Promotech Sales, Inc.
2901 S. Colorado Blvd.
Denver, CO 80222
phone: 303-692-8484
fax: 303-692-8416

Florida

M^2I
402 S. North Lake Blvd
Suite 1016
Altamonte Springs, FL 32701
phone: 407-260-6422
fax: 407-260-6460

Georgia

M^2I
3000 Northwoods Parkway #110
Norcross, GA 30071
phone: 404-447-6124
fax: 404-447-0422

Hawaii

Bager Electronics
17220 Newhope Street, Suite 209
Fountain Valley, CA 92708
phone: 714-957-3367
fax: 714-546-2654

Illinois

Beta Technology Sales, Inc.
1009 Hawthorn Drive
Itasca, IL 60143
phone: 708-250-9586
fax: 708-250-9592

Iowa

Cahill, Schmitz & Howe
226 Sussex Drive. N.E.
Cedar Rapids, IA 52402
phone: 319-377-8219
fax 319-377-0958

Louisiana

TL Marketing
14850 Quorum Dr., Suite 100
Dallas, TX 75240
phone: 214-490-9300
fax: 214-960-6075

Massachusetts

Advanced Technical Services
348 Park Street, Suite 102
North Reading, MA 01864
phone: 508-664-0888
fax: 508-664-5503

Minnesota

Cahill, Schmitz & Cahill, Inc.
315 N. Pierce Street
St. Paul, MN 55104
phone: 612-646-7217
fax: 612-646-4484

Mississippi

M^2I
1910 Sparkman Avenue
Huntsville, AL 35816
phone: 205-830-0498
fax: 205-837-7049

Montana

Promotech Sales, Inc.
2901 S. Colorado Blvd.
Denver, CO 80222
phone: 303-692-8484
fax: 303-692-8416

Nevada

Clark County Only
Bager Electronics
6324 Variel, Suite 314
Woodland Hills, CA 91367
phone: 818-712-0011
fax: 818-712-0160

Other
Norcomp
2140 Professional Drive, #200
Roseville, CA 95661
phone: 916-782-8070
fax: 916-782-8073

New Jersey

Parallax
734 Walt Whitman Road
Melville, NY 11747
phone: 516-351-1000
fax: 516-351-1606

North American Representatives (cont.)

New York

Empire Technical Associates
29 Fennell Street, Suite A
Skaneateles, NY 13152
phone: 315-685-5703
fax: 315-685-5979

Empire Technical Associates
349 W. Commercial Street
Suite 2920
East Rochester, NY 14445
phone: 716-381-8500
fax: 716-381-0911

Parallax
734 Walt Whitman Road
Melville, NY 11747
phone: 516-351-1000
fax: 516-351-1606

North Carolina

M^2I
1200 Trinity Road
Raleigh, NC 27607
phone: 919-851-0010
fax: 919-851-6620

North Dakota

Cahill, Schmitz & Cahill, Inc.
315 N. Pierce Street
St. Paul, MN 55104
phone: 612-646-7217
fax: 612-646-4484

Oklahoma

TL Marketing
14850 Quorum Dr., Suite 100
Dallas, TX 75240
phone: 214-490-9300
fax: 214-960-6075

South Carolina

M^2I
1200 Trinity Road
Raleigh, NC 27607
phone: 919-851-0010
fax: 919-851-6620

South Dakota

Cahill, Schmitz & Cahill, Inc.
315 N. Pierce Street
St. Paul, MN 55104
phone: 612-646-7217
fax: 612-646-4484

Tennessee

M^2I
3000 Northwoods Parkway #110
Norcross, GA 30071
phone: 404-447-6124
fax: 404-447-0422

Texas

TL Marketing
14850 Quorum Dr., Suite 100
Dallas, TX 75240
phone: 214-490-9300
fax: 214-960-6075

TL Marketing
8100 Shoal Creek, Suite 250
Austin, TX 78758
phone: 512-371-7272
fax: 512-371-0727

TL Marketing
14343 Tory Chase Blvd. Suite I
Houston, TX 77014
phone: 713-587-8100
fax: 713-580-7517

Wisconsin

Western
Cahill, Schmitz & Cahill, Inc.
315 N. Pierce Street
St. Paul, MN 55104
phone: 612-646-7217
fax: 612-646-4484

Eastern
Beta Technology Sales, Inc.
9401 W. Beloit Road, Suite 409
Milwaukee, WI 53227
phone: 414-543-6609
fax: 414-543-9288

Canada

Electrosource
6875 Royal Oak
Burnaby, BC
Canada V5J 4J3
phone: 604-435-2533
fax: 604-435-2538

Electrosource
230 Galaxy Blvd.
Rexdale, ONT
Canada M9W 5R8
phone: 416-675-4490
fax: 416-675-6871

Electrosource
340 March Road, Suite 503
Kanata, ONT
Canada
K2K 2E4
phone: 613-592-3214
fax: 613-592-4256

Electrosource
6600 Trans Canada Highway,
Suite 420
Pointe Claire, Quebec
H9R 4S2
phone: 514-630-7486
fax: 514-630-7421

Others (Not Listed)

Contact nearest office of
C-Cube Microsystems

International Representatives and Distributors

France

NEWTEK (Rep/Dist.)
8, rue de l'Esterel
SILIC 583
94663 Rungis Cedex
phone: (33) 1-46.87.22.00
fax: (33) 1-46.87.80.49

United Kingdom

Kudos Thame Ltd. (Rep/Dist.)
55 Suttons Park, London Rd.
Reading, BERKS RG6 1AZ
phone: (44) 734-351010
fax: (44) 734-351030

Germany

Metronik GmbH (Rep/Dist.)
Leonhardsweg 2
8025 Unterhaching
phone: (49) 89-61108-0
fax: (49) 89-6116858

Australia

ZATEK Components Pty Ltd. (Rep/Dist.)
Suite 8, 1059 Victoria Rd.
West Ryde 2114
Sydney
phone: (61) 2-874-0122
fax: (61) 2-874-6171

Hong Kong

MEMEC Asia Pacific (Rep/Dist.)
Unit No 2520-2525
Tower 1
Metroplaza
Hing Fong Road
Kwai Fong, N.T.,
phone: (852) 410-2780
fax: (852) 418-1600

Japan

Kubota C-Cube Inc.
Fuso Building, 7F, 2-12-8
Shin-Yokohama
Kohoku-Ku
Yokohama, Kanagawa 222
phone: (81) 45-474-7571
fax: (81) 45-474-7570

Korea

MEMEC Asia Pacific (Rep/Dist.)
4th Floor, Jae Woong Bldg
176-11 Nonhyun-Dong
Kangnam-ku
Seoul
phone: (82) 2-518-8181
fax: (82) 2-518-9419

Singapore

Serial System Marketing (Rep/Dist.)
11 Jalan Mesin
Standard Industrial Bldg, #06-00
Singapore 1336
phone: (65) 280-0200
fax: (65) 286-6723

Republic of China

MEMEC Asia Pacific(Rep)
14F-1, 171 Section 58
Min Sheng East Road
Hai Hwa Building
Taipei
Taiwan, R.O.C.
phone: (886) 2 760-2028
fax: (886) 2 765-1488

ALLY, Inc. (Dist.)
7F, 18, Alley 1 Lane 768, Sec. 4
Pa Teh Rd.,
Taipei
Taiwan, R.O.C.
phone: (886) 2 788-6270
fax: (886) 2 786-3550

C-Cube Microsystems Sales Offices

Home Office

C-Cube Microsystems
1778 McCarthy Boulevard
Milpitas, CA 95035
phone: 408-944-6300
fax: 408-944-6314

Eastern Area Office

C-Cube Microsystems
One Kendall Square, Suite 220
Cambridge, MA 02139
phone: 617-621-7180
fax: 617-621-7179

Southwestern Area Office

C-Cube Microsystems
453 Bristol Avenue
Cardiff, CA 92007
phone: 619-632-0864
fax: 619-632-0864

European Office

C-Cube Microsystems
44 Dartford Road
Sevenoaks, Kent
UK TN 133 TQ
phone: (44) 732 743 256
fax: (44) 732 450 151

Japan Office

Kubota C-Cube Inc
Fuso Building 7F
2-12-8 Shin-Yokohama
Kohoku-ku
Yokohama, Kanagawa 222
phone: 81-45-474-7571
fax: 81-45-474-7570

C-Cube Microsystems
1778 McCarthy Blvd.
Milpitas, CA 95035
Tel: (408) 944-6300
Fax: (408) 944-6314

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