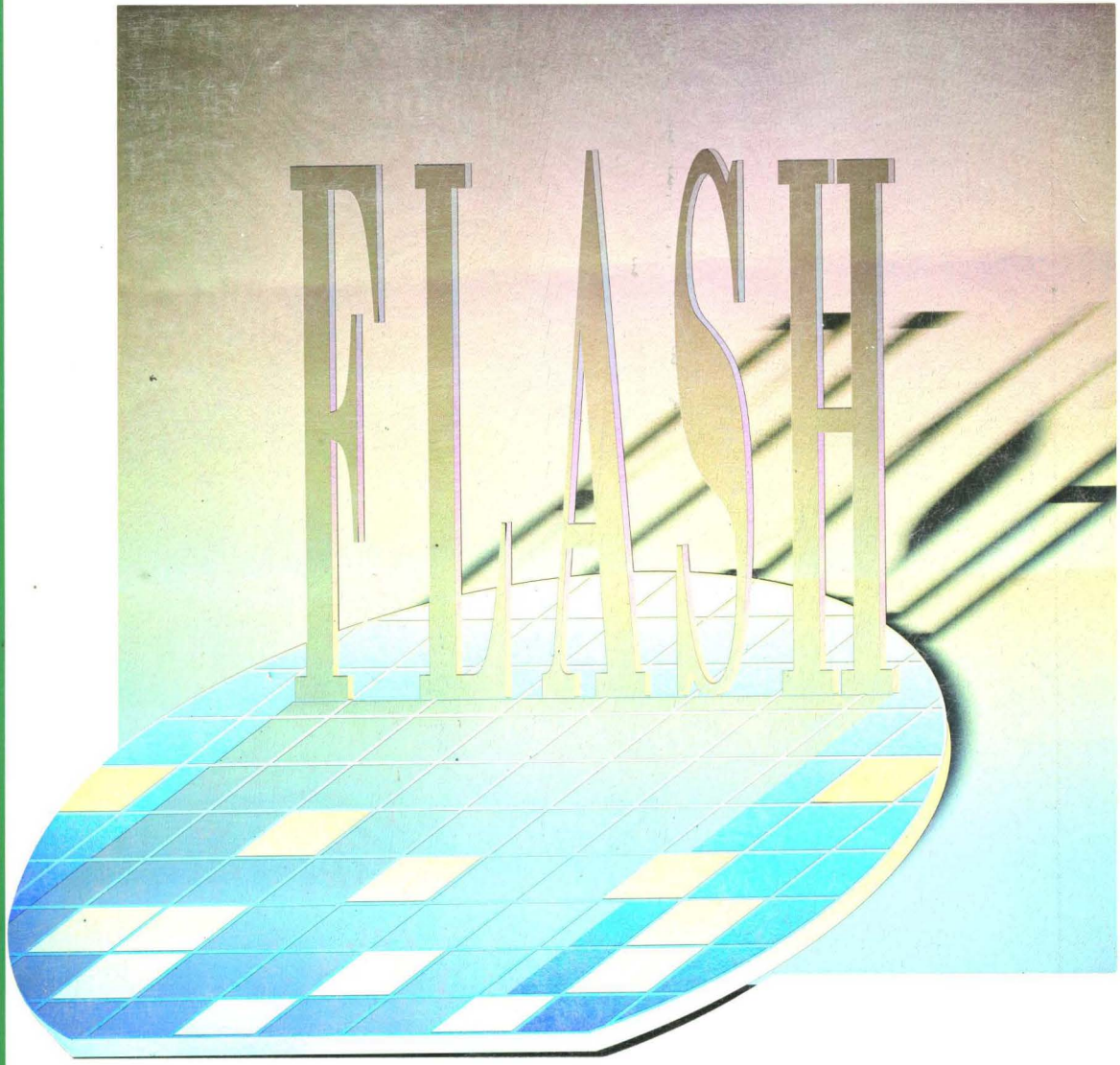
Flash Memory Products

1992/1993 Data Book/Handbook

Advanced
Micro
Devices



AMD's Marketing Communications Department specifies environmentally sound agricultural inks and recycled papers, making this book highly recyclable.

Flash Memory Products

Data Book/Handbook

1992/1993

ADVANCED MICRO DEVICES

Because of their ability to retain data without power applied, non-volatile memories have become an integral part of almost every digital system in use today. EPROMs have been the memory of choice because of their flexibility and low cost. Their only drawback has been their inability to be reprogrammed in system. Although EEPROMs do offer this capability, higher cost has prohibited their widespread use.

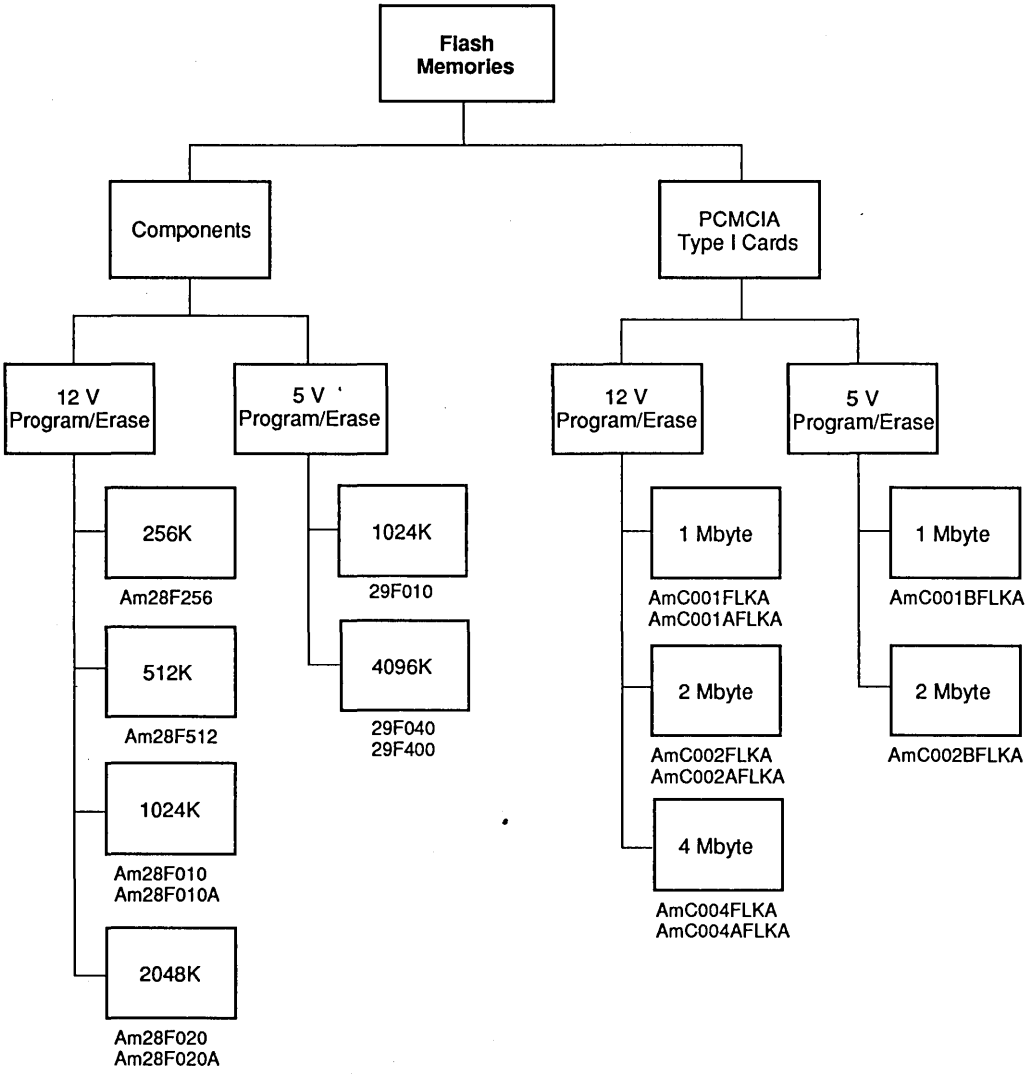
Flash memories offer the system designer a new alternative. For the first time designers have a cost effective, reprogrammable non-volatile memory for use in their systems. AMD was one of the first companies to manufacture first generation 12.0 V Flash memories and today ranks second worldwide in Flash shipments.

In 1992 AMD announced a revolutionary new product, the Am29F010. This product incorporates AMD's proprietary negative gate erase technology to completely eliminate the need for the 12.0 V programming supply. The early acceptance of this device, which conforms to all JEDEC standards, confirms our belief that this technology will become the model for all Flash memories in the future.

By developing leadership high speed and high density products, AMD has become the world's largest supplier of EPROMs. A brief glance through the pages of this databook will convince you of AMD's commitment to Flash memories. Our broad offering of superior Flash components and cards will enable us to strengthen our position as a major Flash memory supplier.

Walid Maghribi
Division Vice President
Non-Volatile Memories

TABLE OF CONTENTS


Flash Memories
Components
PCMCIA Type I Cards
12 V Program/Erase
5 V Program/Erase
12 V Program/Erase
5 V Program/Erase
256K
Am28F256
512K
Am28F512
1024K
Am28F010
Am28F010A
2048K
Am28F020
Am28F020A
1024K
29F010
4096K
29F040
29F400
1 Mbyte
AmC001FLKA
AmC001AFLKA
2 Mbyte
AmC002FLKA
AmC002AFLKA
4 Mbyte
AmC004FLKA
AmC004AFLKA
1 Mbyte
AmC001BFLKA
2 Mbyte
AmC002BFLKA

Flash Memories – 12 V Program/Erase

Part Number	Organization	Access Time (ns)	Endurance	Temp Range[1]	Package Type[2]	Pin Count	Supply Voltage	Programming Voltage
Am28F256-75	32K x 8	70	10K	C	D, L, P, J, E, F	32	5 V ± 5%	12 V ± 5%
Am28F256-90	32K x 8	90	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F256-95	32K x 8	90	10K	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V ± 5%
Am28F256-120	32K x 8	120	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F256-150	32K x 8	150	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F256-200	32K x 8	200	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F512-75	64K x 8	70	10K	C	D, L, P, J, E, F	32	5 V ± 5%	12 V ± 5%
Am28F512-90	64K x 8	90	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F512-95	64K x 8	90	10K	C, I, E	D, L, P, J, E, F	32	5 V ± 5%	12 V ± 5%
Am28F512-120	64K x 8	120	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F512-150	64K x 8	150	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F512-200	64K x 8	200	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F010-90	128K x 8	90	10K	C	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F010-95	128K x 8	90	10K	C	D, L, P, J, E, F	32	5 V ± 5%	12 V ± 5%
Am28F010-120	128K x 8	120	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F010-150	128K x 8	150	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F010-200	128K x 8	200	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F010A-90	128K x 8	90	100K	C	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F010A-95	128K x 8	90	100K	C	D, L, P, J, E, F	32	5 V ± 5%	12 V ± 5%
Am28F010A-120	128K x 8	120	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F010A-150	128K x 8	150	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F010A-200	128K x 8	200	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F020-90	256K x 8	90	10K	C	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F020-95	256K x 8	90	10K	C	D, L, P, J, E, F	32	5 V ± 5%	12 V ± 5%
Am28F020-120	256K x 8	120	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F020-150	256K x 8	150	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F020-200	256K x 8	200	10K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F020A-90	256K x 8	90	100K	C	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F020A-95	256K x 8	90	100K	C	D, L, P, J, E, F	32	5 V ± 5%	12 V ± 5%
Am28F020A-120	256K x 8	120	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F020A-150	256K x 8	150	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%
Am28F020A-200	256K x 8	200	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V ± 5%

Notes:

1. Temperature Range
   - C = Commercial (0°C to 70°C)
   - I = Industrial (–40°C to +85°C)
   - E = Extended Commercial (–55°C to +125°C)
   - M = Military (–55 to +125°C) most products available in both APL and DESC versions.

2. Package Type
   - D = Ceramic DIP
   - L = Rectangular Ceramic Leadless Chip Carrier
   - P = Plastic DIP
   - J = Rectangular Plastic Leaded Chip Carrier
   - E = Thin Small Outline Package – standard pin-out
   - F = Thin Small Outline Package – reverse pin-out

Flash Memories – 5 V Program/Erase

Part Number	Organization	Access Time (ns)	Endurance	Temp Range[1]	Package Type[2]	Pin Count	Supply Voltage	Programming Voltage
Am29F010-45	128K x 8	45	100K	C	D, L, P, J, E, F	32	5 V ± 10%	5 V ± 10%
Am29F010-55	128K x 8	55	100K	C, I	D, L, P, J, E, F	32	5 V ± 10%	5 V ± 10%
Am29F010-70	128K x 8	70	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V ± 10%
Am29F010-90	128K x 8	90	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V ± 10%
Am29F010-120	128K x 8	120	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V ± 10%
Am29F040-70	512K x 8	70	100K	C, I	D, L, P, J, E, F	32	5 V ± 10%	5 V ± 10%
Am29F040-90	512K x 8	90	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V ± 10%
Am29F040-120	512K x 8	120	100K	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V ± 10%
Am29F400-70	512K x 8, 256K x 16	70	100K	C, I	D, L, P, J, E, F	44	5 V ± 10%	5 V ± 10%
Am29F400-90	512K x 8, 256K x 16	90	100K	C, I, E, M	D, L, P, J, E, F	44	5 V ± 10%	5 V ± 10%
Am29F400-120	512K x 8, 256K x 16	120	100K	C, I, E, M	D, L, P, J, E, F	44	5 V ± 10%	5 V ± 10%

Notes:

1. Temperature Range
   - C = Commercial (0°C to 70°C)
   - I = Industrial (–40°C to +85°C)
   - E = Extended Commercial (–55°C to +125°C)
   - M = Military (–55 to +125°C) most products available in both APL and DESC versions.

2. Package Type
   - D = Ceramic DIP
   - L = Rectangular Ceramic Leadless Chip Carrier
   - P = Plastic DIP
   - J = Rectangular Plastic Leaded Chip Carrier
   - E = Thin Small Outline Package – standard pin-out
   - F = Thin Small Outline Package – reverse pin-out

PCMCIA Type I Flash Memory PC Cards

12 V Program/Erase

Part Number	Organization[1]	Access Time (ns)	Endurance	Temp Range[2]	Pin Count	Program/ Erase[3]	Supply Voltage	Programming Voltage
AmC001FLKA	1 M x 8, 512K x16	250	10K	C	68	Software	5 V ± 5%	12 V ± 5%
AmC002FLKA	2 M x 8, 1 M x16	250	10K	C	68	Software	5 V ± 5%	12 V ± 5%
AmC004FLKA	4 M x 8, 2 M x16	250	10K	C	68	Software	5 V ± 5%	12 V ± 5%
AmC001AFLKA	1 M x 8, 512K x 16	250	100K	C	68	Embedded	5 V ± 5%	12 V ± 5%
AmC002AFLKA	2 M x 8, 1 M x 16	250	100K	C	68	Embedded	5 V ± 5%	12 V ± 5%
AmC004AFLKA	4 M x 8, 2 M x 16	250	100K	C	68	Embedded	5 V ± 5%	12 V ± 5%

5 V Program/Erase

Part Number	Organization	Access Time (ns)	Endurance	Temp Range[1]	Pin Count	Program/ Erase[2]	Supply Voltage	Programming Voltage
AmC001BFLKA	1 M x 8, 512K x16	150	100K	C	68	Embedded	5 V ± 5%	12 V ± 5%
AmC002BFLKA	2 M x 8, 1 M x16	150	100K	C	68	Embedded	5 V ± 5%	12 V ± 5%

Notes:

1. CIS: Card Information Structure stored in a separate 512 Byte EEPROM
2. Temperature Range: C = Commercial (0°C to 60°C)
3. Program/Erase: Software =Software controlled Flashrite and Flasherase Algorithm
   Embedded = Embedded Program and Embedded Erase Algorithm

FLASH CROSS REFERENCE GUIDE

256K

Intel	AMD
N28F256A-120	Am28F256-120JC
N28F256A-150	Am28F256-150JC
N28F256A-200	Am28F256-200JC
P28F256A-120	Am28F256-120PC
P28F256A-150	Am28F256-150PC
P28F256A-200	Am28F256-200PC

512K

Intel	AMD
N28F512-120	Am28F512-120JC
N28F512-150	Am28F512-150JC
N28F512-200	Am28F512-200JC
P28F512-120	Am28F512-120PC
P28F512-150	Am28F512-150PC
P28F512-200	Am28F512-200PC
D28F512-150P1C4	Am28F512-150DC
D28F512-200P1C4	Am28F512-200DC
TN28F12-200P1C4	Am28F512-200JI
TD28F12-200P1C4	Am28F512-200DI

1 Megabit

Intel	AMD
N28F010-90	Am28F010-90JC
N28F010-120	Am28F010-120JC
N28F010-150	Am28F010-150JC
N28F010-200	Am28F010-200JC
P28F010-90	Am28F010-90PC
P28F010-120	Am28F010-120PC
P28F010-150	Am28F010-150PC
P28F010-200	Am28F010-200PC
D28F010-150P1C4	Am28F010-150DC
D28F010-200P1C4	Am28F010-200DC
E28F010-90	Am28F010-90EC
E28F010-120	Am28F010-120EC
E28F010-150	Am28F010-150EC
E28F010-200	Am28F010-200EC
F28F010-90	Am28F010-90FC
F28F010-120	Am28F010-120FC
F28F010-150	Am28F010-150FC
F28F010-200	Am28F010-200FC
TN28F010-200P1C4	Am28F010-200JI
TD28F010-200P1C4	Am28F010-200DI

2 Megabit

Intel	AMD
N28F020-90	Am28F020-90JC
N28F020-120	Am28F020-120JC
N28F020-150	Am28F020-150JC
N28F020-200	Am28F020-200JC
P28F020-90	Am28F020-90PC
P28F020-120	Am28F020-120PC
P28F020-150	Am28F020-150PC
P28F020-200	Am28F020-200PC
E28F020-90	Am28F020-90EC
E28F020-120	Am28F020-120EC
E28F020-150	Am28F020-150EC
E28F020-200	Am28F020-200EC
F28F020-90	Am28F020-90FC
F28F020-120	Am28F020-120FC
F28F020-150	Am28F020-150FC
F28F020-200	Am28F020-200FC

Memory Cards

Intel	AMD
IMC001FLKA	AmC001FLKA
IMC002FLKA	AmC002FLKA
IMC004FLKA	AmC004FLKA

Note: Refer to the Product Selector Guide on page vi for additional offerings.

Introduction to AMD's ExpressFlash™ Service

Advanced Micro Devices

INTRODUCTION

AMD's ExpressFlash service is a helpful new way to offer the system manufacturer flexibility and lower cost in the manufacturing process. No matter how Flash memory is used in your system, AMD's ExpressFlash service will benefit your manufacturing process. Flash devices procured via the ExpressFlash program are rigorously tested with your code under both AC and DC operating conditions at worse case temperature prior to shipment. Because Flash products ordered through the ExpressFlash service are shipped board-ready with factory guaranteed quality, your ship-to-stock or Just-In-Time programs can be easily implemented.

AMD's ExpressFlash service offers the same pre-programming convenience as AMD's ExpressROM™ Memories with the added advantage of in-system reprogrammability. Whether your entire code is finalized by the time you place your order or not, AMD's ExpressFlash service will work for you. After AMD's Flash devices are delivered and installed in your system—you have the added flexibility to reprogram the devices *in-system at any time.*

AMD's ExpressFlash service is ideally suited for a variety of applications. For example, with AMD's ExpressFlash service, a PC manufacturer's boot code can be programmed in a portion of the AMD Flash device while the rest of the device remains blank. Upon delivery the Flash devices can be directly installed in your systems. After the remainder of the code is finalized, it can then be loaded *in-system. At this point, even the original boot code can be altered should a "bug" be discovered or a change be required. This process reduces manufacturing cycle time, overhead, and improves both time-to-market and system availability.*

For systems requiring fully protected blocks of code, AMD's Am29F family is ideal. With AMD's ExpressFlash service, your code can be protected from further alteration right at AMD's factory. In the system, the protected portion of code looks just like a ROM. Please refer to AMD's Am29F family of datasheets for further details.

Since Flash devices are fully tested in the plastic packages, all speed grades offered for standard Flash devices are available through the ExpressFlash program as well.

ExpressFlash Service Lowers Cost

The ExpressFlash service eliminates or reduces costs in several areas. These include programming, testing, marking and labeling. Standard programming of blank devices may reveal other hidden expenses such as costs associated with possible programming yield losses, capacity constraints, labels and other supplies, rework, inventory and associated queue time, handling, maintenance, labor and personnel, transit costs, inspections, floor space and other overhead. AMD's ExpressFlash service adds value by eliminating or reducing all these costs.

Our mission at AMD is to provide services and products which enable you to build the cost-competitive systems you need to win in your markets. The ExpressFlash service is yet another value-added program offered by AMD to help you accomplish your goals. As the world's #1 supplier of EPROMs, AMD appreciates the value of cost-efficient manufacturing. Compressing time-to-market cycles, improving yields and providing the highest levels of quality are invaluable strategies for today's system manufacturer. At AMD we are proud to offer another tool to give our customers this strategic advantage.

ExpressFlash Flow

AMD's ExpressFlash service takes Flash devices from inventory in our off-shore testing facility and continues the processing as shown in Figure 1. This process is offered for all package types and speed grades. Please refer to AMD's Flash datasheets for valid combinations. For die orders, please contact your local AMD sales representative.

Publication# 17125 Rev. A Amendment/0
Issue Date: September 1992

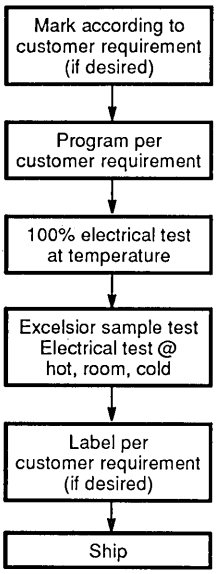


Figure 1. ExpressFlash Flow

Ordering Flash Devices Using the Express Flash Service

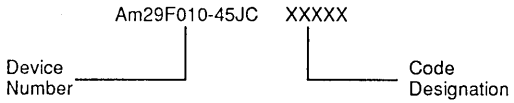
The following procedure outlines the method for ordering a Flash device using the ExpressFlash service. For more information, please contact your local AMD sales representative.

1) Send in the Code

Please have your field sales representative provide you with the latest version of the ExpressFlash Code Approval Form (see Figure 2). This form will provide all the necessary information required for processing your order. After receiving this form, fill out the Code Transmittal and Ordering Information sections. Then send the form with two (2) master copies of each code being ordered to your field sales representative. To minimize the verification turnaround process, supply two master copies of each code using standard Flash devices identical in architecture and density as the Flash device being ordered. Two master copies per code are required in order to guarantee proper code transmission. Please be sure the checksum is clearly identified on each master Flash device.

2) AMD Checks the Code and Generates a Verification Flash Device

We check that both Flash devices contain the same code to make certain there was not a mix-up in shipping your codes to the factory as well as ensuring that the integrity of your code has been preserved. After confirming this, a unique 5-digit code designation is assigned. The AMD part number is formed by adding the 5-digit code designation as a suffix to the Flash device number. See below:



AMD then logs in your code with the 5-digit code designation and generates a verification Flash device. The verification Flash device along with one of your master Flash devices and the ExpressFlash Code Approval Form should be back in your hand for final approval within 2–3 days. The other master Flash device remains at AMD for our records. Please note: the verification Flash device is simply a means of transferring the code and is not necessarily indicative of the Flash device being ordered.

3) Confirm the Copy and Place the Order

Once the verification Flash device is approved, sign the Approval Section of the ExpressFlash Code Approval Form and return it to AMD with your purchase order. Upon receipt of the signed form and a purchase order, AMD enters the order and begins production. Logged codes are maintained for 60 days and then deleted if there is no purchase order placed.

TERMS AND CONDITIONS

You should be aware of the following when ordering Flash devices using the ExpressFlash service.

1. AMD will maintain customer code confidentiality.
2. AMD will absorb all initial set-up costs.
3. All orders are subject to minimum quantities. The minimum quantity for initial orders is 5,000 pieces.
4. AMD may begin production 14 days in advance of the AMD scheduled ship date covered by a purchase order and requires 14 days minimum notification from the AMD scheduled ship date for code changes. The customer is liable for all work-in-process covered by the same purchase order.
5. No schedule changes may be made within 14 days of AMD scheduled ship date.
6. All unpackaged die product procured by the customer is for use exclusively in the customer's end products. Any other use of die product must be approved in writing by AMD.
7. Code changes with Work-In-Process will require additional charges and may affect delivery schedules.
8. All other terms and conditions which normally apply to AMD's Flash devices (if any) also apply using AMD's ExpressFlash service.

ExpressFlash™ Code Approval Form

CODE TRANSMITTAL AND ORDERING INFORMATION SECTION Rev. 1 5/12/92

Please complete items 1 thru 9. To minimize the verification turn-around process, supply 2 master copies of each code using Flash Devices of the same architecture and density as the Flash Device being ordered. Also, be sure the checksum is clearly identified on each master Flash Device.

CODE TRANSMITTAL SECTION

1. Company Name: _____ 2. Date: _____

3. Incoming Master's Part #: _____ 4. Master's Checksum: _____

ORDERING INFORMATION SECTION

Please check the appropriate Flash Device data sheet for valid combinations and mark appropriate boxes below; Vcc is +/-10% unless otherwise noted with * for +/-5%.

5. Part #:

❑ Am28F256	❑ *70ns	❑ 90ns	❑ *90ns	❑ 120ns	❑ 150ns	❑ 200ns
❑ Am28F512	❑ *70ns	❑ 90ns	❑ *90ns	❑ 120ns	❑ 150ns	❑ 200ns
❑ Am28F010			❑ *90ns	❑ 120ns	❑ 150ns	❑ 200ns
❑ Am28F010A			❑ *90ns	❑ 120ns	❑ 150ns	❑ 200ns
❑ Am28F020			❑ *90ns	❑ 120ns	❑ 150ns	❑ 200ns
❑ Am28F020A			❑ *90ns	❑ 120ns	❑ 150ns	❑ 200ns
❑ Am29F010	❑ 45ns	❑ 55ns	❑ 70ns	❑ 90ns	❑ 120ns	
❑ Sector information _____				Protected?	❑ Yes	❑ No
❑ Other _____						

6. Package and Temperature:
   - ❑ Plastic DIP
   - ❑ PLCC
   - ❑ TSOP Standard Pinout
   - ❑ TSOP Reverse Pinout
   - ❑ Commercial (0°C to +70°C)
   - ❑ Industrial (-40°C to +85°C)
   - ❑ Other _____

7. AMD Standard Part Number: _____

8. Customer Ordering Part Number: _____

9. Please indicate the exact **marking** and complete the blank sections (12 characters per line including spaces, © = 2 spaces if required).

AMD Logo

_____

_____

_____

Date Code

APPROVAL SECTION TERMS AND CONDITIONS

AMD will maintain customer code confidentiality. AMD will absorb all initial set-up costs.
AMD may begin production 14 days in advance of the AMD scheduled ship date covered by a purchase order and requires 14 days minimum notification from the AMD scheduled ship date for code changes.
The customer is liable for all work-in-process covered by the same purchase order.
No schedule changes may be made within 14 days of AMD scheduled ship date.
All unpackaged die product procured by the customer is for use exclusively in the customer's end products.
Any other use of die product must be approved in writing by AMD.
All orders are subject to minimum quantities.
Code changes with Work In Process will require additional charges and may affect delivery schedules.

AMD Standard Part #: Am _____ Checksum: _____

Customer Signature: _____ Date: _____

Name (Print): _____ Title: _____

Figure 2. 17125A-2

THIRD PARTY SUPPORT PRODUCTS

MEMORY CARD DRIVE READER/PROGRAMMER

Company/Address/Phone

Adtron Corp.

128 West Boxelder Place Sutie 102, Chandler, AZ 85224
Phone: (602) 926-9324 Fax: (602) 926-9359

Databook Inc.

Tower Building, Terrace Hill, Ithaca, NY 14850
Phone: (607) 277-4817 Fax: (607) 273-8803

SCM Microsystem GmbH

Berta von Suttnerweg 1 D-8033 Martinsried West Germany
Phone: (089) 856-1363 Fax: (089) 856-1412
or
FraunhoferstraBe 11a 8033 Martinsried West Germany
Phone: (089) 859-8702 Fax: (089) 859-5806

MEMORY CARD SOFTWARE SUPPORT

Award Software Inc.

130 Knowles Drive
Los Gatos, CA 95030
Phone: (408) 370-7979 Fax: (408) 370-3399

Phoenix Technologies Ltd.

846 University Ave, Norwood, MA 02062
Phone: (617) 551-4175 Fax: (617) 551-3743

MEMORY CARD MECHANICAL HARDWARE

DuPont Electronics

14 T.W. Alexander Drive, P.O. Box 13999 Research
Triangle Park, NC 27709
Phone: (800) 237-2374

PRELIMINARY

Flash Memories in Die Form

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **100% testing of AC & DC parameters**
- **Operating temperature ranges:**
  - Commercial 0°C to 70°C
  - Industrial –40°C to +85°C
  - Military –55°C to +125°C
- **Advanced CMOS Flash memory technology**
- **High typical yield—98% after assembly**
- **Full data sheet compatibility**
- **Die visual inspection per MIL-STD-883, Method 2010 Condition B**

GENERAL DESCRIPTION

AMD offers it's family of flash products in die form for hybrid or multichip module applications requiring superior performance and in-system reprogrammability in addition to small die size. Each die is 100% AC and DC tested at wafer sort to guarantee full device functionality over commercial or military temperature ranges. AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles, with some products offering up to 100,000 cycle endurance. Features such as "5 volt-only" program and erase, Sector erase architecture and Embedded Program™/Embedded Erase™ algorithms are also available. Specific product information is available in the product data sheets.

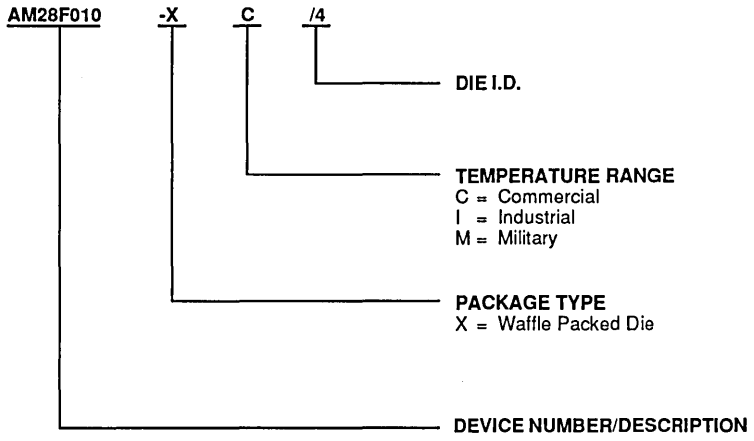
PRODUCT SELECTOR GUIDE

Die Ordering Part Number	Organization	Access Time	Endurance Cycles	Program/ Erase Voltage	Embedded Algorithms	Data Sheet Reference
Am28F256-XC/3	256K (32K x 8)	200 ns	10,000	12 V ± 5%	No	Am28F256
Am28F512-XC/1	512K (64K x 8)	200 ns	10,000	12 V ± 5%	No	Am28F512
Am28F010-XC/4	1M (128K x 8)	200 ns	10,000	12 V ± 5%	No	Am28F010
Am28F010A-XC/5	1M (128K x 8)	200 ns	100,000	12 V ± 5%	Yes	Am28F010A
Am29F010-XC/3	1M (128K x 8)	120 ns	100,000	5 V ± 10%	Yes	Am29F010
Am28F020-XC/1	2M (256K x 8)	200 ns	10,000	12 V ± 5%	No	Am28F020
Am28F020A-XC/2	2M (256K x 8)	200 ns	100,000	12 V ± 5%	Yes	Am28F020A

Publication# 17126 Rev. A Amendment/0
Issue Date: August 1992

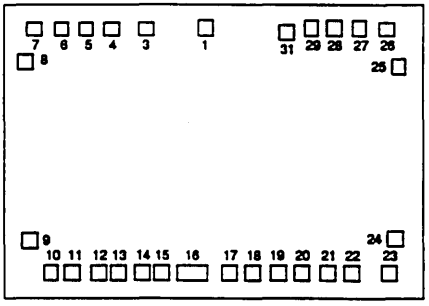
ORDERING INFORMATION

AMD Flash Memories are available in several operating ranges. The order number (Valid Combination) is formed by a combination of:

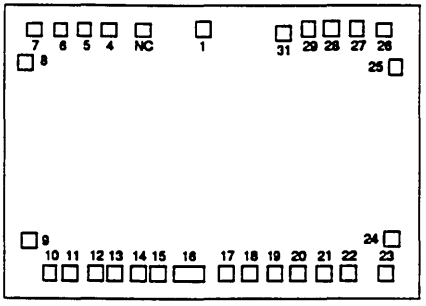


Note: Exposure of Flash die to ultraviolet light may effect device functionality.

DIE SIZE AND BONDING PAD LOCATIONS

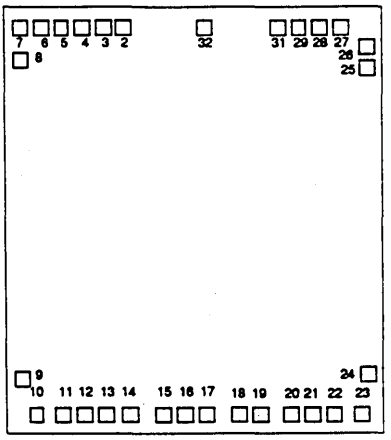


Am28F256-XC/2
256K (32K x 8) Flash Memory
10K endurance cycles
Flashrite™/Flaserase™ Programming
Die Size: 0.200 x 0.143 inches
Reference: Am28F256 data sheet

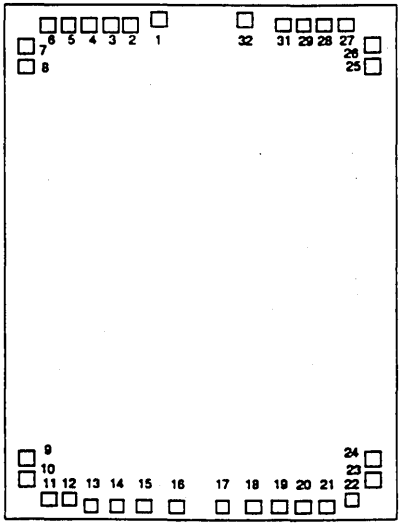


Am28F512-XC/1
512K (64K x 8) Flash Memory
10K endurance cycles
Flashrite™/Flaserase™ Programming
Die Size: 0.200 x 0.143 inches
Reference: Am28F512 data sheet

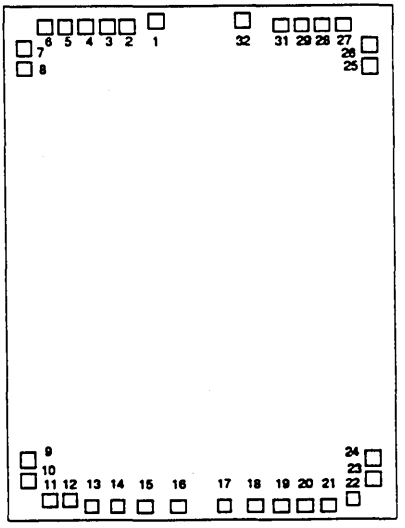
DIE SIZE AND BONDING PAD LOCATIONS



Am29F010-XC/3
1 Megabit (128K x 8) Flash Memory
5 Volt-only program & erase
100K endurance cycles
Embedded Algorithms
Die Size: 0.181 x 0.210 inches
Reference: Am29F010 data sheet

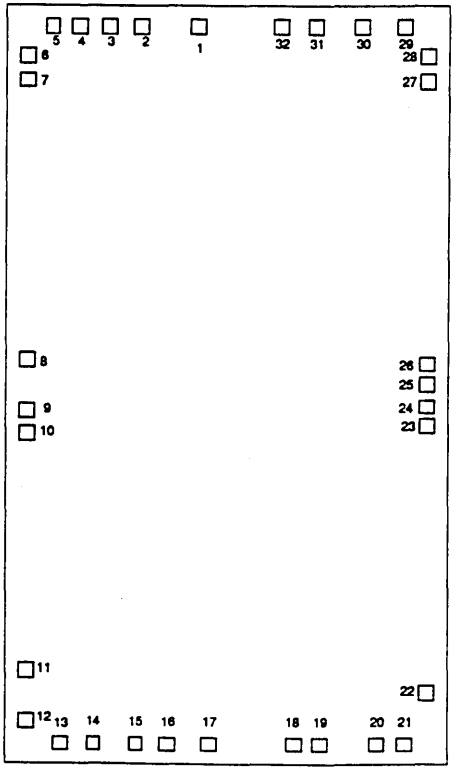


Am28F010-XC/4
1 Megabit (128K x 8) Flash Memory
10K endurance cycles
Flashrite™/Flaserase™ Programming
Die Size: 0.187 x 0.252 inches
Reference: Am28F010 data sheet

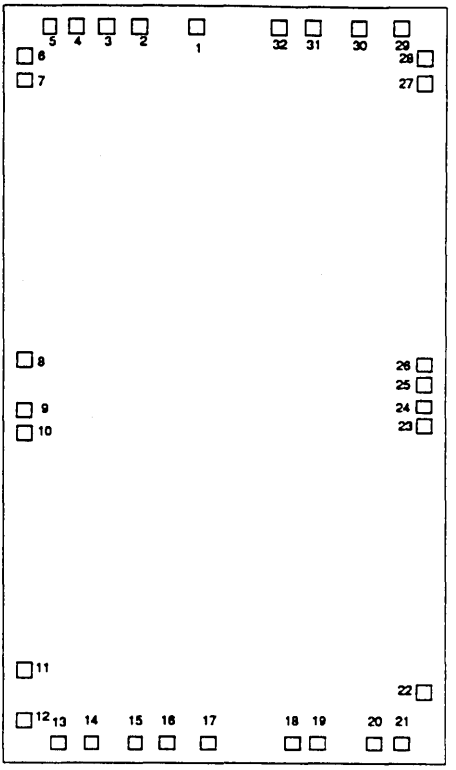


Am28F010-XC/5
1 Megabit (128K x 8) Flash Memory
100K endurance cycles
Embedded Algorithms
Die Size: 0.187 x 0.252 inches
Reference: Am28F010A data sheet

DIE SIZE AND BONDING PAD LOCATIONS



Am28F020-XC/1
1 Megabit (256K x 8) Flash Memory
10K endurance cycles
Flashrite™/Flaserase™ Programming
Die Size: 0.213 x 0.374 inches
Reference: Am28F020 data sheet



Am28F020A-XC/2
2 Megabit (256K x 8) Flash Memory
100K endurance cycles
Embedded Algorithms
Die Size: 0.213 x 0.374 inches
Reference: Am28F020A data sheet

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to AMD Products under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

AMD warrants articles of it's manufacture against defective materials or workmanship for a period of ninety (90) days from date of shipment. This warranty does not extend beyond AMD's customer.and does not extend to die which has been affixed onto a board or substrate of any kind. The liability of AMD under this warranty is limited, at AMD's option, solely to repair or to replacement with equivalent articles, or to make an appropriate credit adjustment not to exceed the original sales price, for articles returned to AMD, provided that: (a) The Buyer promptly notifies AMD in writing of each and every defect or nonconformity in any article for which Buyer wishes to make a warranty claim against AMD; (b) Buyer obtains authorization from AMD to return the article; (c) the article is returned to AMD, transportation charges paid by AMD, F.O.B. AMD's factory; and (d) AMD's examination of such article discloses to its satisfaction that such alleged defect or nonconformity actually exists and was not caused by negligence, misuse, improper installation, accident or unauthorized repair or alteration by an entity other than AMD. The aforementioned provisions do not extend the original warranty period of any article which has either been repaired or replaced by AMD. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THE IMPLIED WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THE IMPLIED WARRANTY OF MERCHANTABILITY AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON AMD'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR AMD ANY OTHER LIABILITIES. THE FOREGOING CONSTITUTES THE BUYERS SOLE AND EXCLUSIVE REMEDY FOR THE FURNISHING OF DEFECTIVE OR NON CONFORMING ARTICLES AND AMD SHALL NOT IN ANY EVENT BE LIABLE FOR DAMAGES BY REASON OF FAILURE OF ANY PRODUCT TO FUNCTION PROPERLY OR FOR ANY SPECIAL, INDIRECT, CONSEQUENTIAL, INCIDENTAL OR EXEMPLARY DAMAGES, INCLUDING BUT NOT LIMITED TO, LOSS OF PROFITS, LOSS OF USE OR COST OF LABOR BY REASON OF THE FACT THAT SUCH ARTICLES SHALL HAVE BEEN DEFECTIVE OR NON CONFORMING. Buyer agrees that it will make no warranty representations to its customers which exceed those given by AMD to Buyer unless and until Buyer shall agree to indemnify AMD in writing for any claims which exceed AMD's warranty. Buyer acknowledges that electrical testing of die is limited to D.C. testing at 25 degrees C unless otherwise specified. As such, data sheet limits for packaged and tested devices do not apply to die sales and are not guaranteed by AMD unless otherwise specified. Buyer also assumes all responsibility for successful die prep, die attach and wire bonding processes. Due to the unprotected nature of the AMD Products which are the subject hereof, AMD assumes no responsibility for environmental effects on die.

AMD products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in a personal injury. Buyer's use of AMD products for use in life support applications is at Buyers own risk and Buyer agrees to fully indemnify AMD for any damages resulting in such use or sale.

SECTION

1 5 V, SECTOR ERASE FLASH MEMORIES

PRELIMINARY

Am29F010

131,072 x 8-Bit CMOS 5.0 V-Only, Sector Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% write and erase**
  - Minimizes system level power consumption
- **Compatible with JEDEC-standard commands**
  - Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin PLCC/LCC
  - 32-pin TSOP
  - 32-pin DIP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - 45 ns maximum access time
- **Sector erase architecture**
  - 8 equal size sectors of 16K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Embedded Erase™ Algorithms**
  - Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  - Automatically programs and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - 20 mA typical active read current
  - 30 mA typical program/erase current
  - 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector Protection**
  - Hardware method disables any combination of sectors from program or erase operations

GENERAL DESCRIPTION

The Am29F010 is a 1Megabit, 5.0 V-Only Flash memory organized as 128K bytes of 8 bits each. The Am29F010 is offered in a 32-pin package which allows for upgrades to 4 Megabit densities in the same pin out. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. 12.0 V V_{PP} is not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The Am29F010 offers access times between 45 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The Am29F010 is entirely pin and command set compatible with JEDEC standard 1 Megabit E²PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The Am29F010 is programmed by executing the program command sequence. This will invoke the Embedded Program algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than 0.3 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. The entire memory is typically erased and verified in three seconds (including pre-programming).

PRODUCT SELECTOR GUIDE

Family Part No:	Am29F010				
Ordering Part No: V_{CC} = 5.0 V ± 5%	–45				
Read Voltage V_{CC} = 5.0 V ± 10%		–55	–70	–90	–120
Max Access Time (ns)	45	55	70	90	120
$\overline{CE}$ ($\overline{E}$) Acess (ns)	45	55	70	90	120
$\overline{OE}$ ($\overline{G}$) Access (ns)	25	30	30	35	50

Publication# 16736 Rev. C Amendment/0
Issue Date: September 1992

Any individual sector is typically erased and verified in 1.3 seconds (including pre-programming).

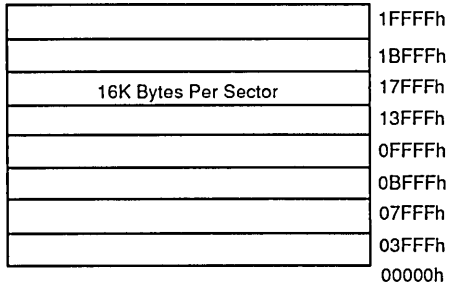
This device also features a sector erase architecture. The sector mode allows for 16K byte blocks of memory to be erased and reprogrammed without affecting other blocks.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{cc} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7 or by the Toggle Bit feature on DQ_6. Once the program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F010 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

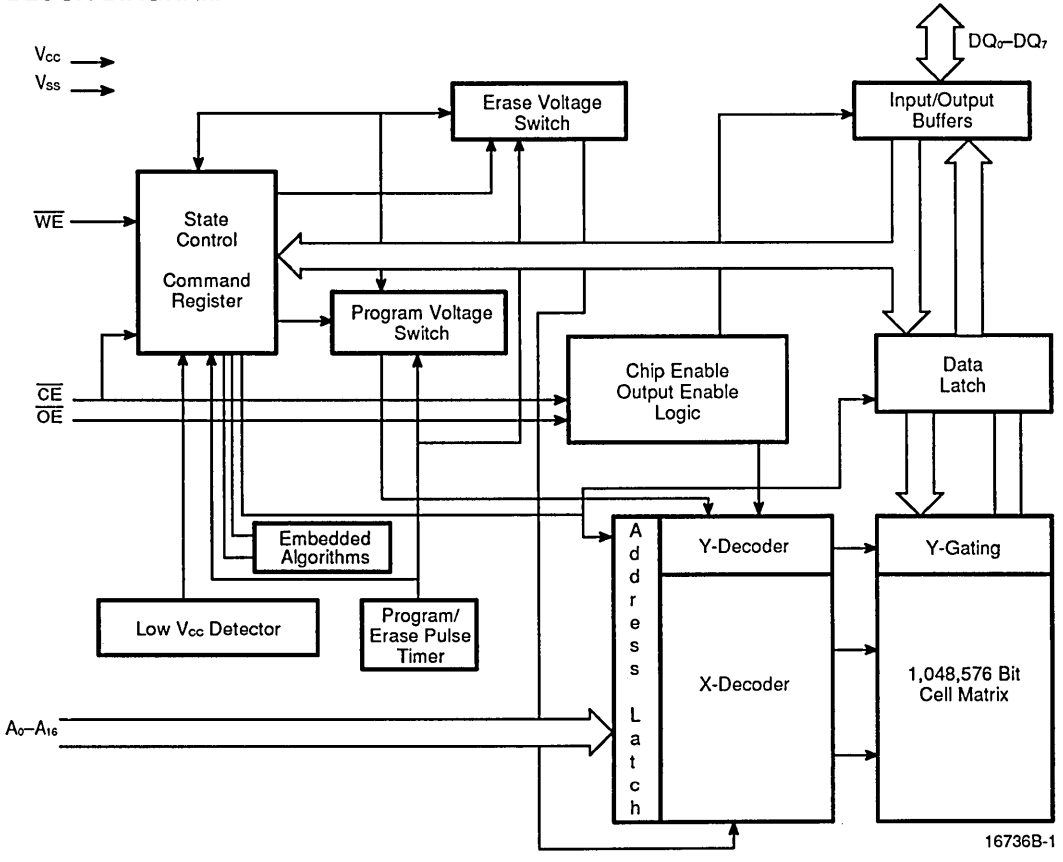
Flexible Sector-Erase Architecture

- 16K bytes per sector
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable



16736B-18

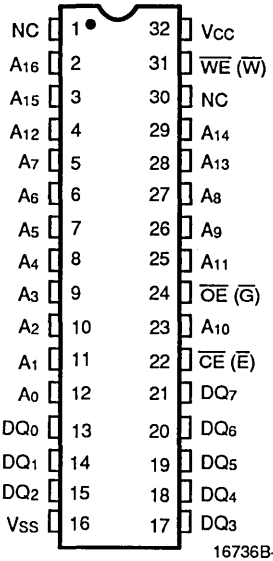
BLOCK DIAGRAM



16736B-1

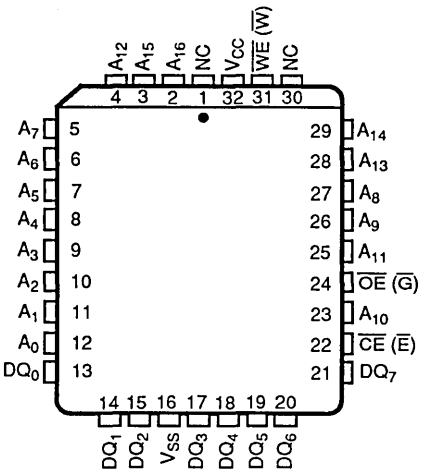
CONNECTION DIAGRAMS

CERDIP/PDIP



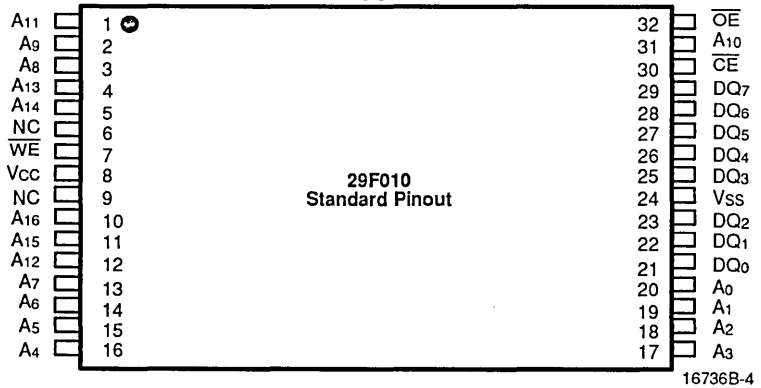
16736B-2

PLCC/LCC

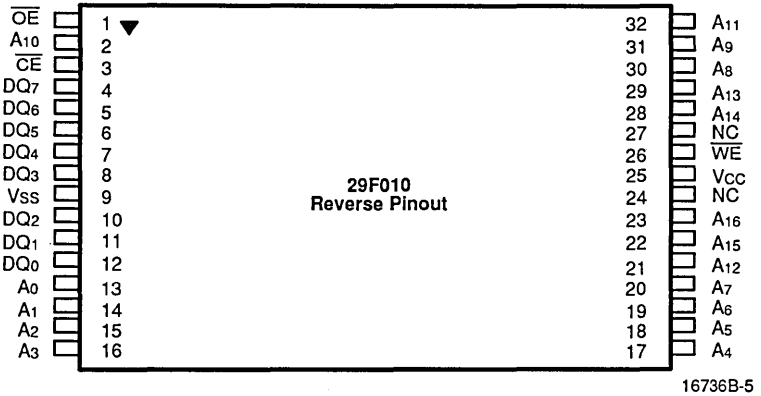


16736B-3

TSOP

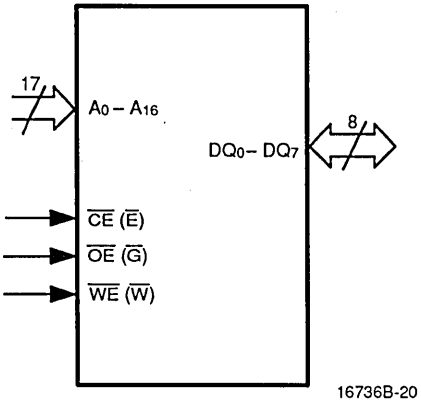


16736B-4



16736B-5

LOGIC SYMBOL



16736B-20

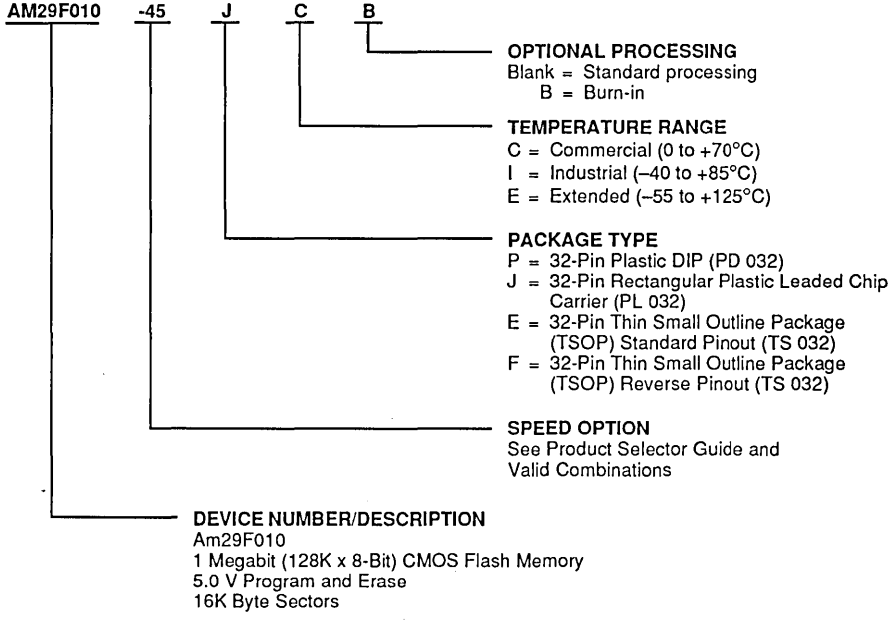
Table 1. Am29F010 Pin Configuration

Pin	Function
A_0–A_{16}	Address Inputs
DQ_0–DQ_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10% or ± 5%)
NC	No Internal Connection

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM29F010-45	PC, JC, EC, FC
AM29F010-55	PC, PI, JC, JI, EC, EI, FC, FI
AM29F010-70 AM29F010-90 AM29F010-120	PC, PI, JC, JI, PCB, PIB, JCB, JIB, PE, PEB, JE, JEB, EC, EI, FC, FI, EE, EEB, FE, FEB

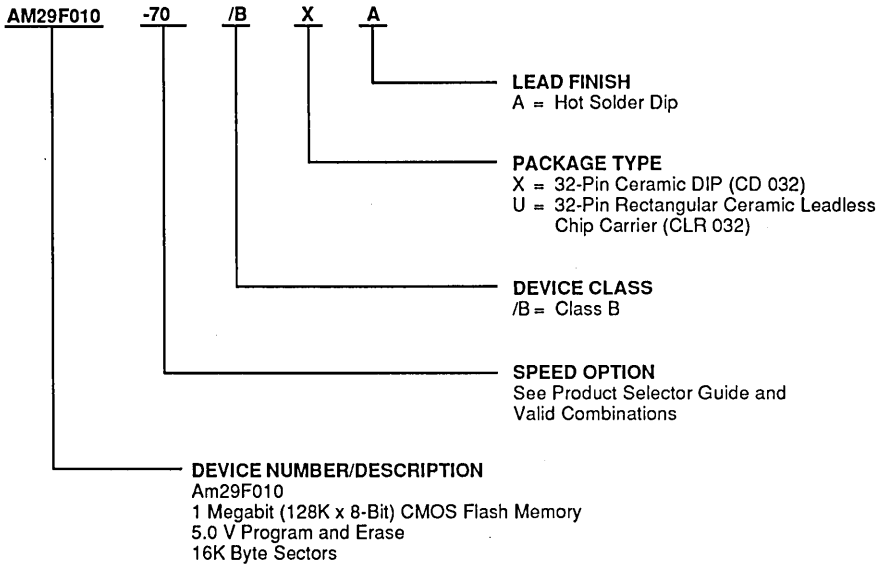
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM29F010-70 AM29F010-90 AM29F010-120	/BXA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Table 2. Am29F010 User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_9	I/O
Auto-Select Manufacturer Code (1)	L	L	H	L	L	V_{ID}	Code
Auto-Select Device Code (1)	L	L	H	H	L	V_{ID}	Code
Read	L	L	H	A_0	A_1	A_9	D_{OUT}
Standby	H	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	HIGH Z
Write	L	H	L	A_0	A_1	A_9	D_{IN} (2)
Enable Sector Protect	L	V_{ID}	L	X	X	V_{ID}	X
Verify Sector Protect (3)	L	L	H	L	H	V_{ID}	Code

Legend:
L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels

Notes:

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tables 3 and 4.
2. Refer to Table 4 for valid D_{IN} during a write operation.
3. Refer to the section on Sector Protection

Read Mode

The Am29F010 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Standby Mode

The Am29F010 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at Vcc ± 0.5 V), when the current consumed is less than 100 µA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are don't cares except A_0 and A_1.

The manufacture and device codes may also be read via the command register, for instances when the AM29F010 is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 4 (refer to Autoselect Command section).

Byte 0 (A_0 = V_{IL}) represents the manufacture's code (AMD=01H) and byte 1 (A_0 = V_{IH}) the device identifier code (Am29F010=20H). These two bytes are given in the table below. All identifiers for manufactures and device will exhibit odd parity with the MSB (DQ_7) defined as the parity bit. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL} (see Table 3).

Table 3. Am29F010 Autoselect Codes

Type	A_{16}	A_{15}	A_{14}	A_1	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacture Code	X	X	X	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Am29F010 Device Code	X	X	X	V_{IL}	V_{IH}	20H	0	0	1	0	0	0	0	0
Sector Protection	Sector Addresses			V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

*Outputs 01H at protected sector addresses

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F010 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 7). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (see AMD's ExpressFlash™ Service section of this databook).

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$. The sector addresses (A_{16}, A_{15}, and A_{14}) should be set to the sector to be protected. Table 4 defines the sector addresses for each of the eight (8) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Reading the device at a particular sector address (A_{16}, A_{15} and A_{14})

Table 4. Sector Addresses Table

	A_{16}	A_{15}	A_{14}	Addr Range
SA_0	0	0	0	00000h-03FFFh
SA_1	0	0	1	04000h-07FFFh
SA_2	0	1	0	08000h-0BFFFh
SA_3	0	1	1	0C000h-0FFFFh
SA_4	1	0	0	10000h-13FFFh
SA_5	1	0	1	14000h-17FFFh
SA_6	1	1	0	18000h-1BFFFh
SA_7	1	1	1	1C000h-1FFFFh

will produce 01H at data outputs (DQ_0–DQ_7) for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A_0 and A_1, are don't care. Address location 02H is reserved to verify sector protection of the device. Address pin A_1 must be held at V_{IH} and A_0 at V_{IL} (please refer to Table 3). Address location 00H and 01H are reserved for autoselect codes. If a verify of the sector protection circuitry were done at these addresses, the device would output the manufacturer and device codes respectively.

It is also possible to determine if a sector is protected in the system by writing the autoselect command. Performing a read operation at particular sector addresses (A_{16}, A_{15}, A_{14}) and with $A_1 = V_{IH}$ and $A_0 = V_{IL}$ (other addresses are a don't care) will produce 01H data if those sectors are protected. (Please refer to Table 3). Otherwise the device will read 00H for an unprotected sector. Please refer to the section on Sector Protection Algorithms for more details.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Table 5 defines these register command sequences.

Table 5. Am29F010 Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H	00H/01H	01H/20H				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H

Notes:

1. Address bit A_{15} = X = Don't Care. Write Sequences may be initiated with A_{15} in either state.
2. Address bit A_{16} = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).
3. Bus operations are defined in Table 2.
4. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A_{16}, A_{15}, A_{14} will uniquely select any sector.
5. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XXX0H retrieves the manufacture code of 01H. A read cycle from address XXX1H returns the device code 20H (see Table 3). A read cycle from address XXX2H returns information as to which sectors are protected. All manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The rising edge of $\overline{WE}$ begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode. Data Polling must be performed at the memory location which is being programmed.

Programming is allowed in any address sequence and across sector boundaries.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ_7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time-out of 100 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the sector erase command 30H to addresses in other sectors desired to be concurrently erased. A time-out of 100 µs from the rising edge of the $\overline{WE}$ pulse for the last sector erase command will initiate the sector erase. If another sector erase command is written within the 100 µs time-out window the timer is reset. Any command other than sector erase within the time-out window will reset the device to the read mode, ignoring the previous command string (refer to Write Operation Status section for Sector Erase Timer operation). Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 100 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ_7 is "1" (see Write Operation Status section) at which time the device returns to read mode. $\overline{Data}$ polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Write Operation Status

Table 6. Hardware Sequence Flags

	Status	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2–DQ_0
In Progress	Auto-Programming	$\overline{DQ_7}$	Toggle	0	0	0	Reserved for future use
	Programming in Auto Erase	0	Toggle	0	0	1	
	Erasing in Auto-Erase	0	Toggle	0	1	1	
Exceeded Time Limits	Auto-Programming	$\overline{DQ_7}$	Toggle	1	0	0	Reserved for future use
	Programming in Auto-Erase	0	Toggle	1	0	1	
	Erasing in Auto-Erase	0	Toggle	1	1	1	

DQ_7
$\overline{Data}$ Polling

The Am29F010 features $\overline{Data}$ Polling as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During the Embedded Programming Algorithm, an attempt to read the device will produce complement data of the data last written to DQ_7. Upon completion of the Embedded Programming Algorithm an attempt to read the device will produce the true data last written to DQ_7. $\overline{Data}$ Polling is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence.

During the Embedded Erase Algorithm, DQ_7 will be "0" until the erase operation is completed. Upon completion data at DQ_7 is "1". For chip erase, the $\overline{Data}$ Polling is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, the $\overline{Data}$ Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse.

The $\overline{Data}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 6).

See Figure 11 for the $\overline{Data}$ Polling timing specifications and diagrams.

DQ_6
Toggle Bit

The Am29F010 also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read data from the device will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is

completed, DQ_6 will stop toggling and valid data will be read on successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector time out.

See Figure 12 for the Toggle Bit timing specifications and diagrams.

DQ_5
Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits. Under these conditions DQ_5 will produce a "1". The program or erase cycle was not successfully completed. $\overline{Data}$ Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 2. To reset the device, write the Reset command sequence to the device. This allows the system to continue to use the other active sectors in the device.

DQ_4
Hardware Sequence Flag

If the device has exceeded the specified erase or program time and DQ5 is "1", then DQ_4 will indicate which step in the algorithm the device exceeded the limits. A "0" in DQ_4 indicates in programming, a "1" indicates an erase.

DQ_3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{Data}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{Data}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{Data}$ Polling or Toggle Bit. If DQ_3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the software should check the status of DQ_3 prior to and following each subsequent sector erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

Data Protection

The Am29F010 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

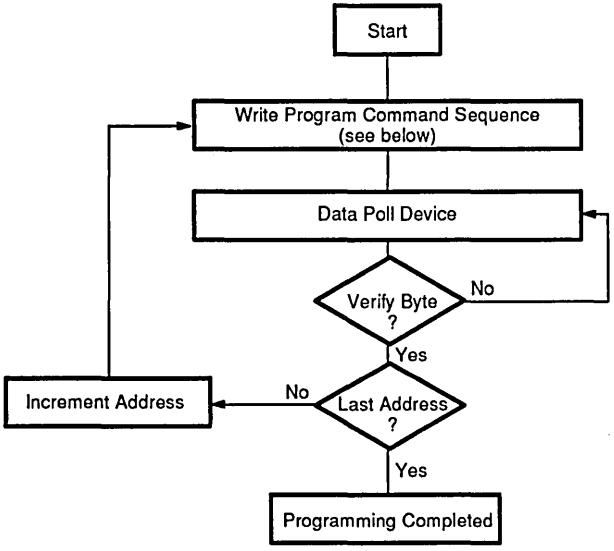
Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

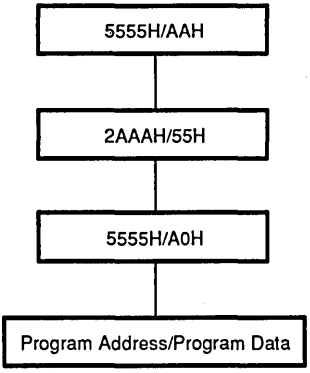
Sectors of the Am29F010 may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

EMBEDDED ALGORITHMS

Embedded Programming Algorithm



Program Command Sequence (Address/Command):



16736B-14

Figure 1. Embedded Programming Algorithm

Table 7. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby (Note 1)		
Write	Programming	Valid Address/Data Sequence
Read		Data Polling to Verify Programming

EMBEDDED™ ERASE ALGORITHM

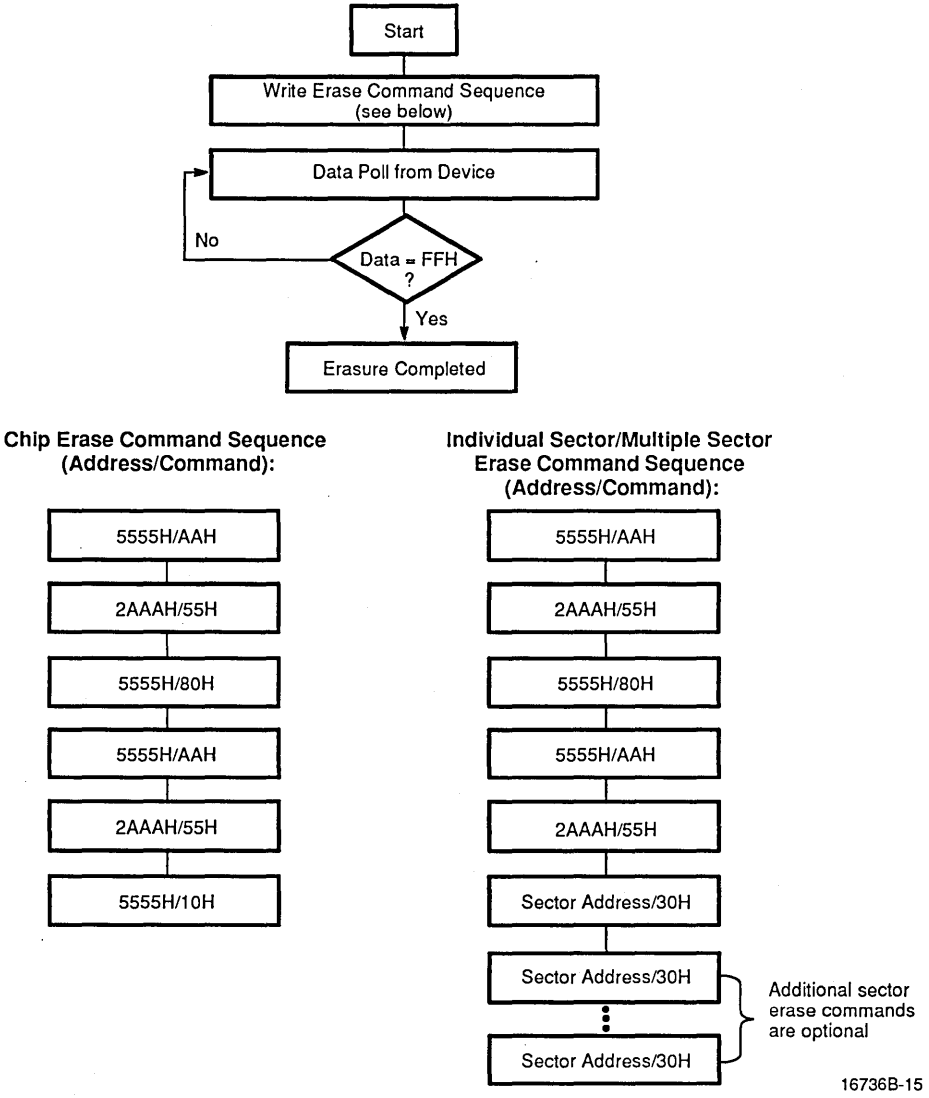
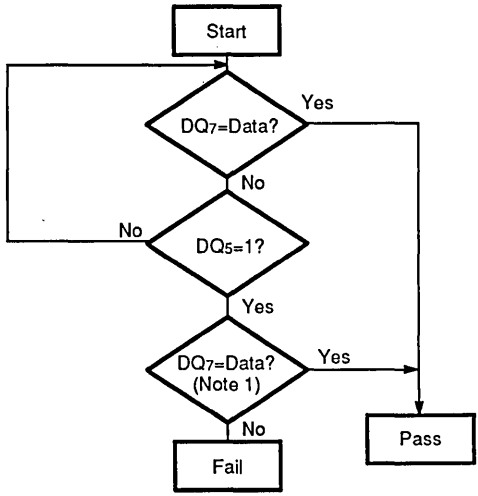


Figure 2. Embedded Erase Algorithm

Table 8. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Erase	
Read		$\overline{\text{Data}}$ Polling to Verify Erasure

DATA POLLING ALGORITHM

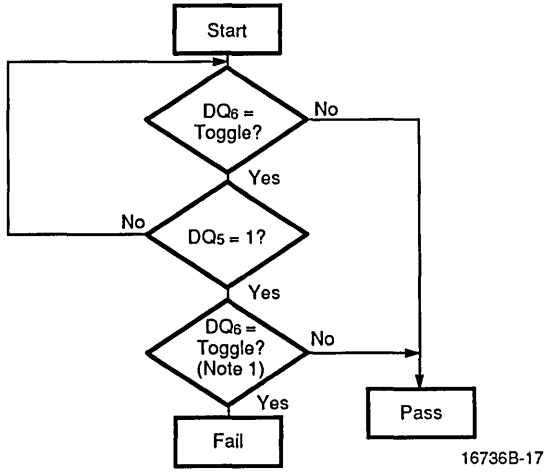


Note:

1. DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

Figure 3. $\overline{\text{Data}}$ Polling Algorithm

TOGGLE BIT ALGORITHM



Note:

1. DQ_6 is rechecked even if DQ_5 = "1" because DQ_6 may stop toggling at the same time as DQ_5 changing to "1".

Figure 4. Toggle Bit Algorithm

PARALLEL DEVICE ERASURE

Since the device is completely self-timed, devices can be erased or programmed in parallel without consideration of other devices in the system.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... −65°C to +150°C
Plastic Packages ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to + 125°C

Voltage with Respect To Ground
All pins except A_9 (Note 1) ..... −2.0 V to +7.0 V

V_{CC} (Note 1) ..... −2.0 V to +7.0 V

A_9 (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on A_9 pin is −0.5 V. During voltage transitions, A_9 may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) ..... −40°C to +85°C

Extended (E) Devices
Case Temperature (Tc) ..... −55°C to +125°C

Military (M) Devices
Case Temperature (Tc) ..... −55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am29F010−45 ..... +4.75 V to +5.25 V

V_{CC} for Am29F010−55, 70, 90, 120 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

MAXIMUM OVERSHOOT

Maximum Negative Overshoot

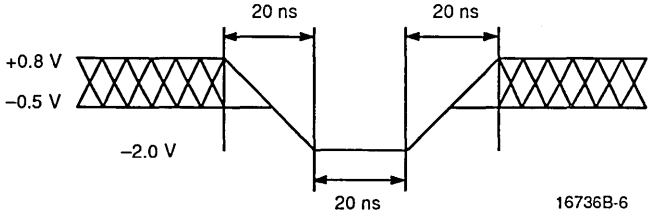


Figure 5. Maximum Negative Overshoot Waveform

Maximum Positive Overshoot

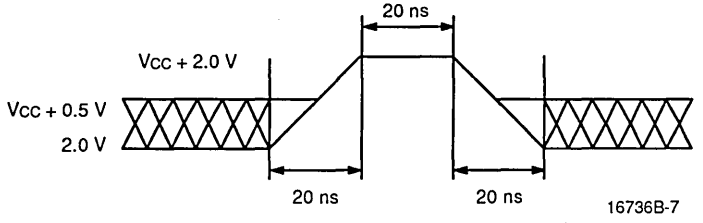


Figure 6. Maximum Positive Overshoot Waveform

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Load Current	V_{IN} = Vss to Vcc, Vcc = Vcc Max.		± 1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = Vss to Vcc, Vcc = Vcc Max.		± 1.0	µA
I_{OS}	Output Short Circuit Current (Note 1)	Vcc = Vcc Max., V_{OUT} = 0.5 V		100	mA
I_{CC1}	Vcc Active Current for Read (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		30	mA
I_{CC2}	Vcc Active Current for Program or Erase (Note 3)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		50	mA
I_{CC3}	Vcc Standby Current	Vcc = Vcc Max, $\overline{CE}$ = V_{IH}		1.0	mA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		2.0	Vcc + 0.5	V
V_{ID}	A_9 Voltage for Autoselect	Vcc = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA Vcc = Vcc Min.		0.45	V
V_{OH}	Output High Level	I_{OH} = –2.5 mA Vcc = Vcc Min.	2.4		V
V_{LKO}	Low Vcc Lock-out Voltage		3.2		V

Notes:

1. Not more than one output should be tested at one time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by the tester ground degradation. (This parameter is sampled and not 100% tested, but guaranteed by characterization.)
2. The Icc current listed includes both the DC operating current and the frequency dependent component (@ 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
3. Icc active while Embedded Algorithm (program or erase) is in progress.

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Load Current	V_{CC} = V_{CC} Max., V_{IN} = V_{SS} to V_{CC}		± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{SS} to V_{CC}		± 1.0	µA
I_{OS}	Output Short Circuit Current (Note 1)	V_{CC} = V_{CC} Max., V_{OUT} = 0.5 V		100	mA
I_{CC1}	V_{CC} Active Current for Read (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		30	mA
I_{CC2}	V_{CC} Active Current for Program or Erase (Note 3)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		50	mA
I_{CC3}	V_{CC} Standby Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{CC} ± 0.5 V		100	µA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		0.7 V_{CC}	V_{CC} +0.5	V
V_{ID}	A_9 Voltage for Autoselect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12.0 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}		I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}		
V_{OH2}	Output High Voltage	I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4		
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		V

Notes:

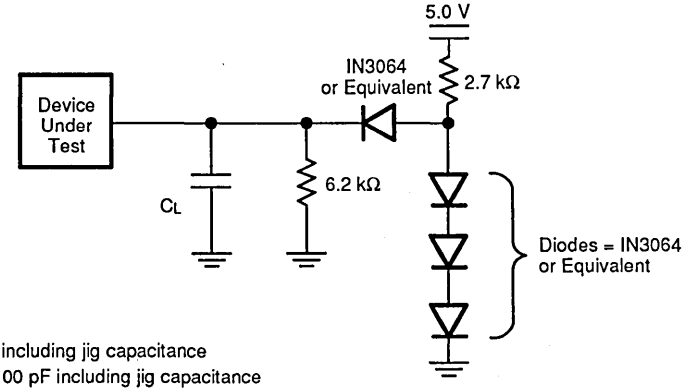
1. Not more than one output should be tested at one time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by the tester ground degradation. (This parameter is sampled and not 100% tested, but guaranteed by characterization.)
2. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

AC CHARACTERISTICS—READ ONLY OPERATIONS CHARACTERISTICS

Parameter Symbols		Description	Test Setup	–45 (1)	–55 (1)	–70 (2)	–90 (2)	–120 (2)	Unit
JEDEC	Standard								
tAVAV	tRC	Read Cycle Time		45	55	70	90	120	ns
tAVQV	tACC (max)	Address to Output Delay	$\overline{CE}$ = VIL $\overline{OE}$ = VIL	45	55	70	90	120	ns
tELQV	tCE (max)	Chip Enable to Output	$\overline{OE}$ = VIL	45	55	70	90	120	ns
tGLQV	tOE (max)	Output Enable to Output		25	30	30	35	50	ns
tEHQZ	tDF (max)	Chip Enable to Output High Z (Note 3)		10	15	20	20	30	ns
tGHQZ	tDF	Output Enable to Output High Z (Note 3)		10	15	20	20	30	ns
tAXQX	tOH	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		0	0	0	0	0	ns

Notes:

1. Test Conditions:
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level
   Input: 1.5 V
   Output: 1.5 V
2. Test Conditions:
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level
   Input: 0.8 and 2.0 V
   Output: 0.8 and 2.0 V
3. Output driver disable time.



Note:

For –45: C_L = 30 pF including jig capacitance
For all others: C_L = 100 pF including jig capacitance

16736B-8

Figure 7. Test Conditions

AC CHARACTERISTICS—WRITE/ERASE/PROGRAM OPERATIONS

Parameter Symbols		Description		–45	–55	–70	–90	–120	Unit
JEDEC	Standard								
tAVAV	tWC	Write Cycle Time		45	55	70	90	120	ns
tAVWL	tAS	Address Setup Time		0	0	0	0	0	ns
tWLAX	tAH	Address Hold Time		35	45	45	45	50	ns
tDVWH	tDS	Data Setup Time		20	20	30	45	50	ns
tWHDX	tDH	Data Hold Time		0	0	0	0	0	ns
	tOES	Output Enable Setup Time		0	0	0	0	0	ns
	tOEH	Output Enable Hold Time	Read	0	0	0	0	0	ns
			Toggle and $\overline{\text{Data}}$ Polling	10	10	10	10	10	ns
tGHWL	tGHWL	Read Recover Time Before Write		0	0	0	0	0	ns
tELWL	tCS	$\overline{\text{CE}}$ Setup Time		0	0	0	0	0	ns
tWHEH	tCH	$\overline{\text{CE}}$ Hold Time		0	0	0	0	0	ns
tWLWH	tWP	Write Pulse Width		25	30	35	45	50	ns
tWHWL	tWPH	Write Pulse Width High		15	20	20	20	20	ns
tWHWH1	tWHWH1	Programming Operation (min)		14	14	14	14	14	µs
tWHWH2	tWHWH2	Erase Operation (min) (Note 1)		2.2	2.2	2.2	2.2	2.2	sec
	tVCS	V_{CC} Set Up Time		2	2	2	2	2	µs
	tVLHT	Voltage Transition Time (Note 2)		4	4	4	4	4	µs
	tWPP	Write Pulse Width (Note 2)		10	10	10	10	10	ms
	tOESP	$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active (Note 2)		4	4	4	4	4	µs
	tCSP	$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active (Note 3)		4	4	4	4	4	µs

Notes:

1. This also includes the preprogramming time.
2. These timings are for Sector Protect/Unprotect operations.
3. This timing is only for Sector Unprotect.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

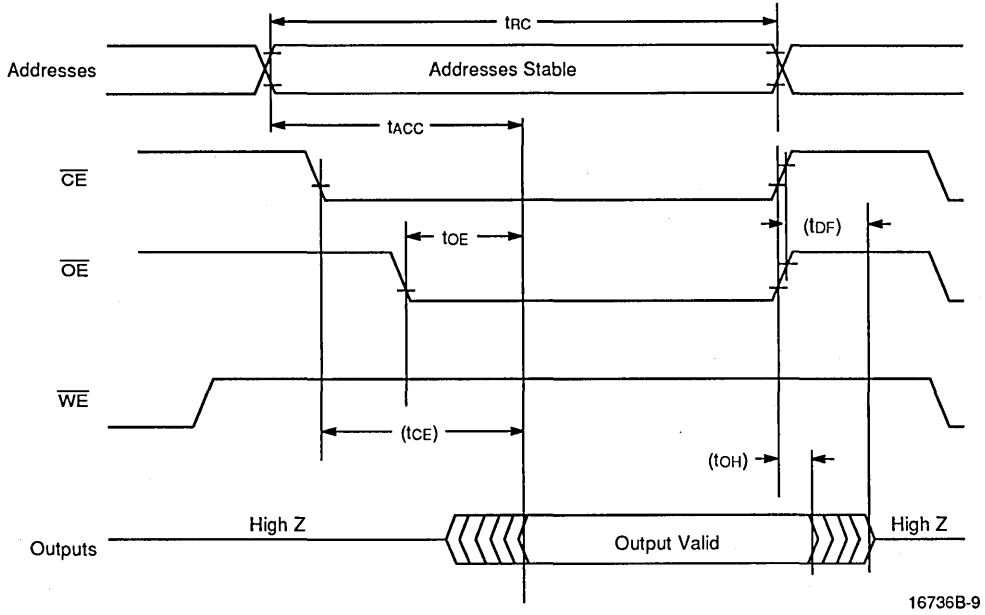
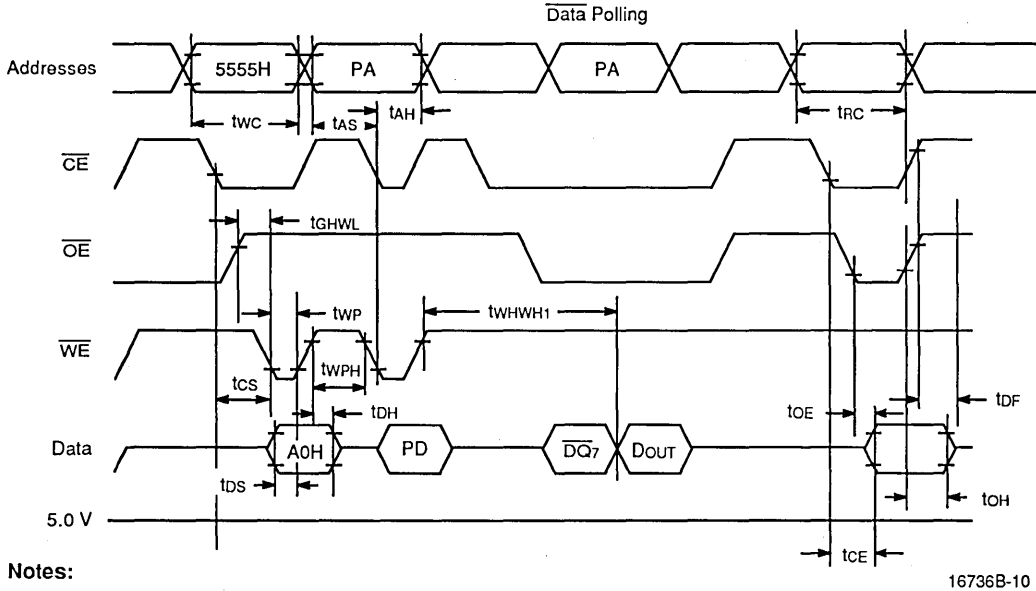


Figure 8. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

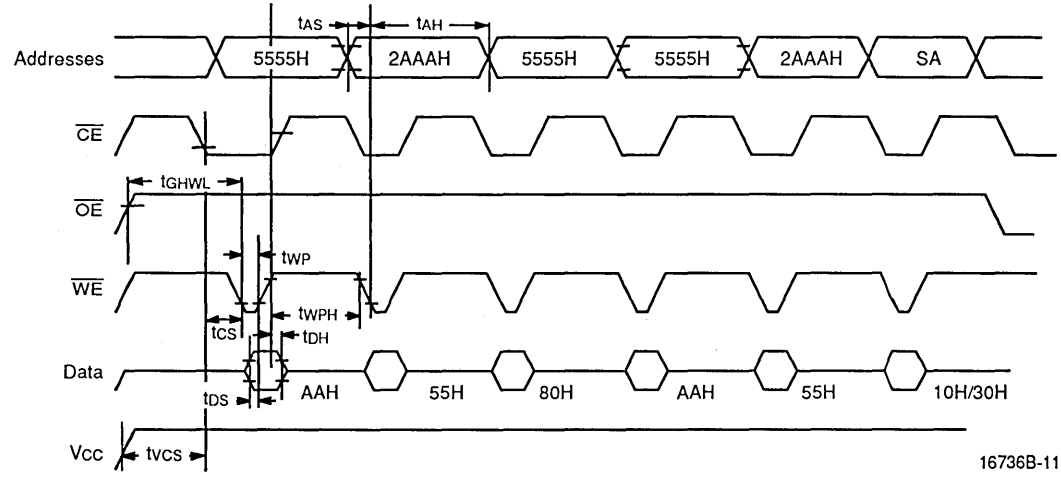


Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Figure 9. Program Operation Timings

SWITCHING WAVEFORMS



Note:

1. SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.

Figure 10. AC Waveforms Chip/Sector Erase Operations

SWITCHING WAVEFORMS

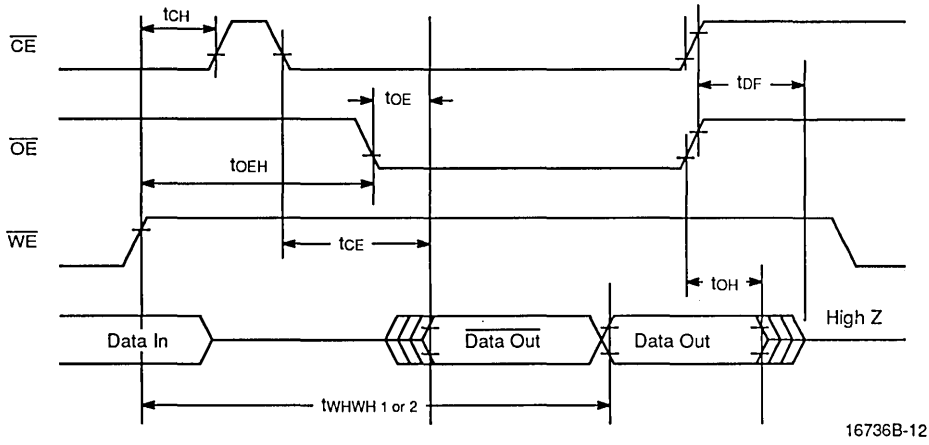
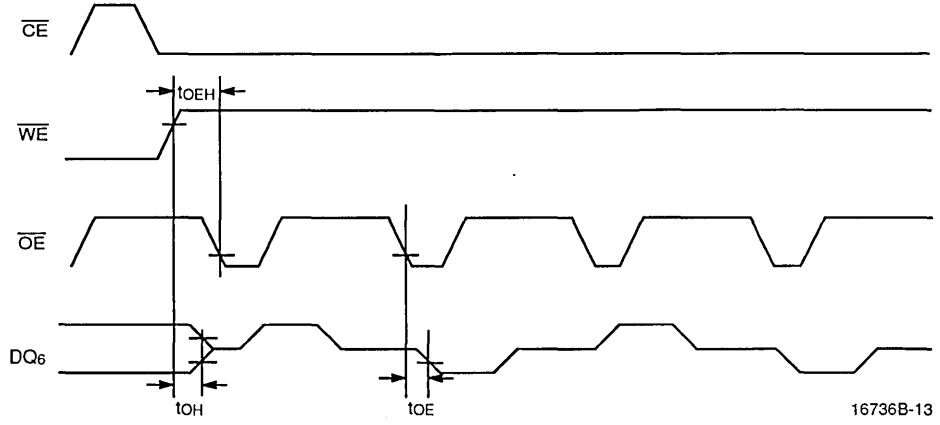


Figure 11. AC Waveforms for Data Polling during Embedded Algorithm Operations

SWITCHING WAVEFORMS



Note:
This is an example of the Toggle Bit write operation status when valid data out is "0".

Figure 12. AC Waveforms for Toggle Bit during Embedded Algorithm Operations

SECTOR PROTECTION ALGORITHMS

Sector Protection

The Am29F010 features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A_9. The sector addresses should be set using higher address lines A_{16}, A_{15}, and A_{14}. The protection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH} (A_9 remains high at V_{ID}). Reading the device at address location XXX2H, where the higher order addresses (A_{16}, A_{15}, and A_{14}) define a particular sector, will produce 01H at data outputs (DQ_0–DQ_7) for a protected sector.

Sector Unprotect

The Am29F010 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pins $\overline{OE}$, $\overline{CE}$, and address pin A_9. The address pins A_6, A_7, and A_{12} should be set to $A_7 = A_{12} = V_{IH}$, and $A_6 = V_{IL}$. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command. Performing a read operation at address location XXX2H, where the higher order addresses (A_{16}, A_{15}, and A_{14}) define a particular sector address, will produce 00H at data outputs (DQ_0–DQ_7) for an unprotected sector.

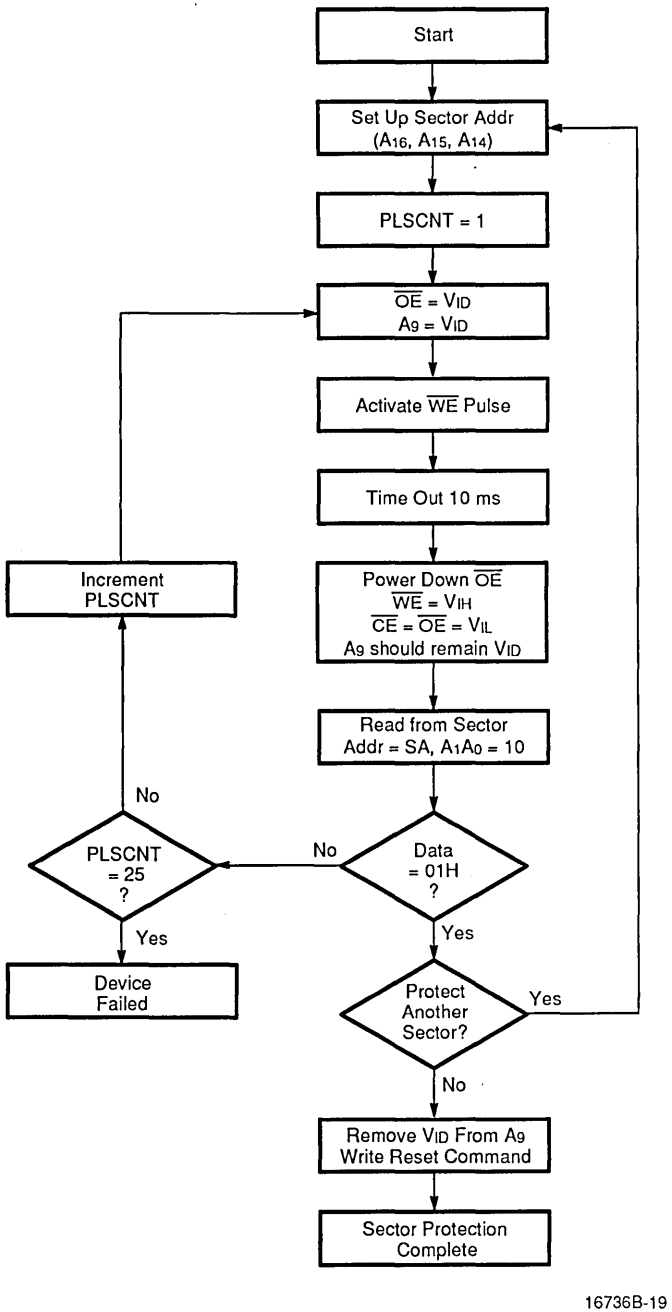
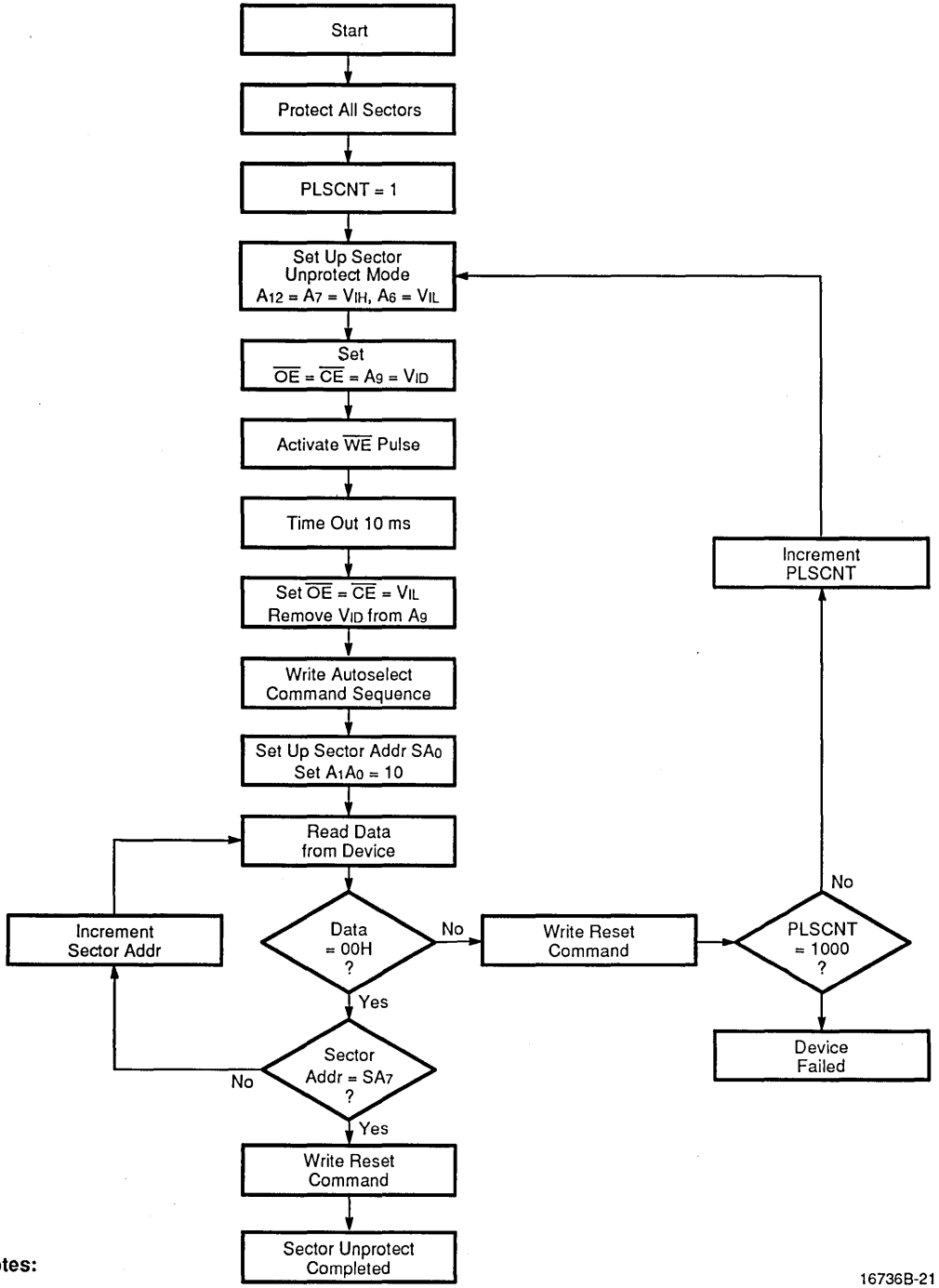


Figure 13. Sector Protection Algorithm



Notes:

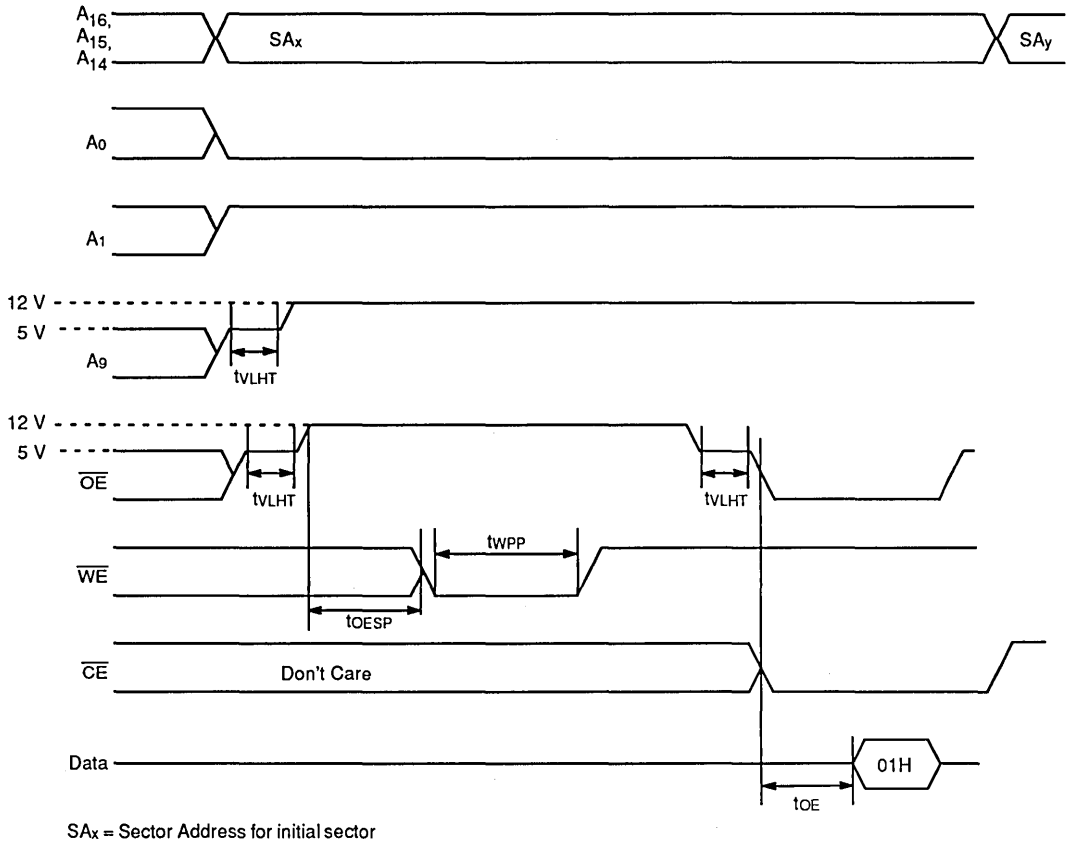
SA_0 = Sector Address for initial sector

SA_7 = Sector Address for last sector

Please refer to Table 4 for details.

Figure 14. Sector Unprotect Algorithm

SWITCHING WAVEFORMS



SA_x = Sector Address for initial sector
SA_y = Sector Address for next sector

16736B-18

Figure 15. AC Waveforms for Sector Protection

SWITCHING WAVEFORMS

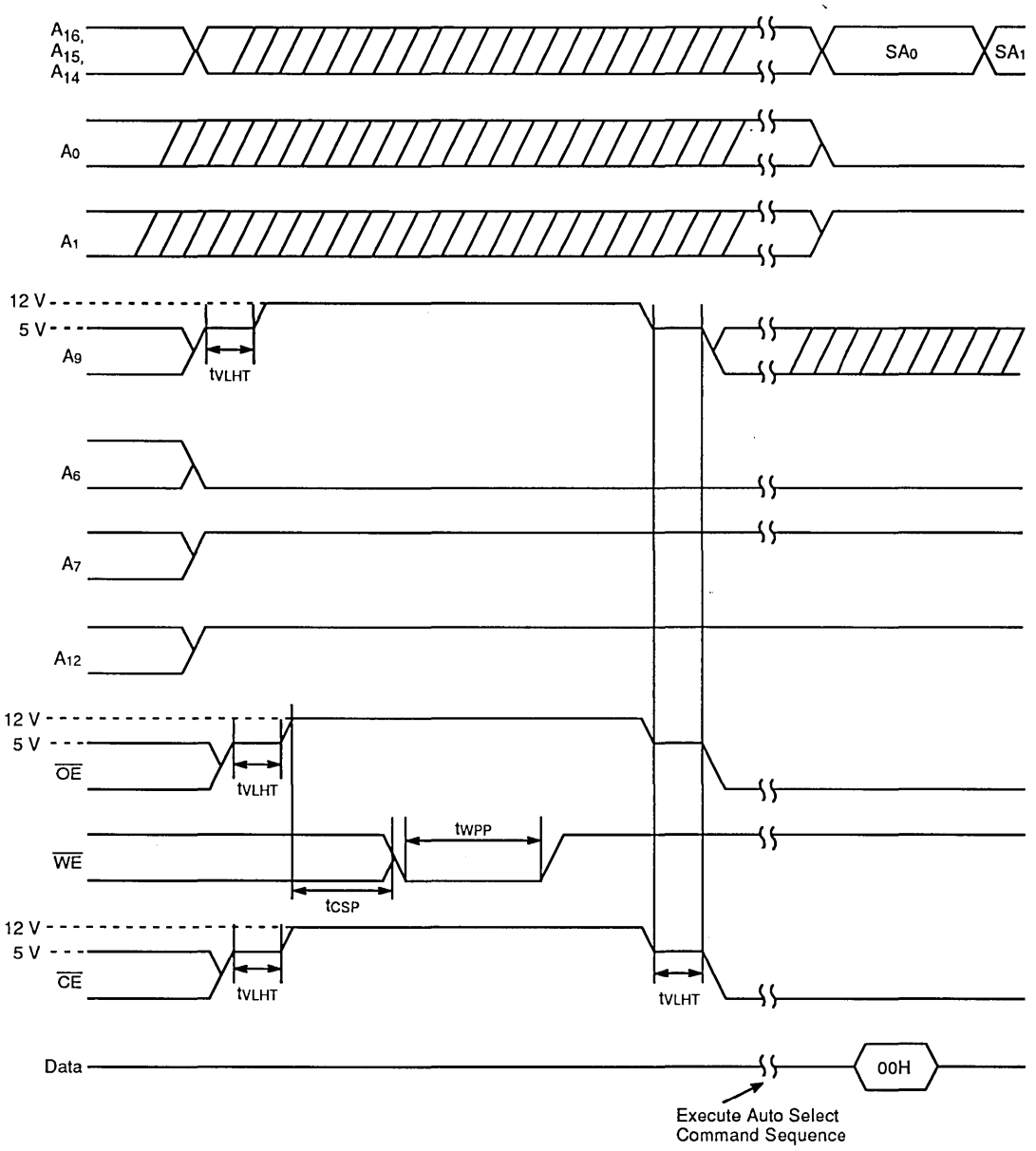


Figure 16. AC Waveforms for Sector Unprotect

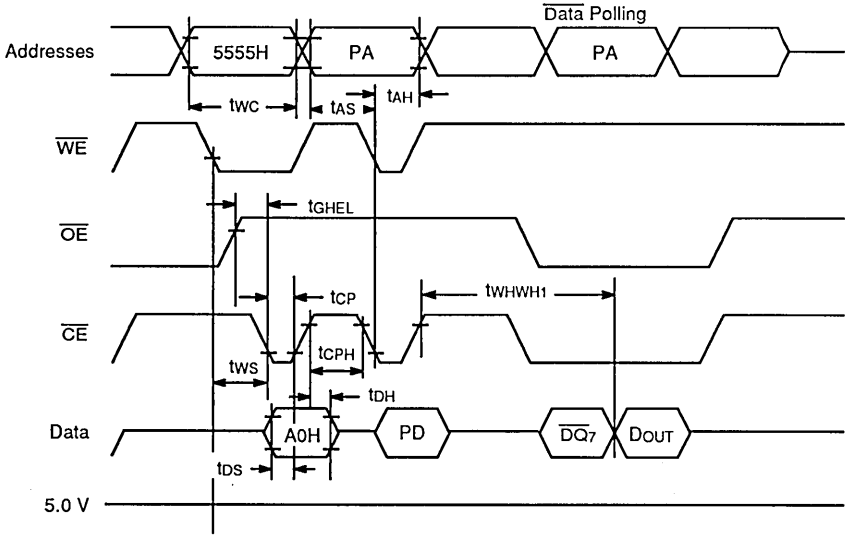
AC CHARACTERISTICS—WRITE/ERASE/PROGRAM OPERATIONS

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description		–45	–55	–70	–90	–120	Unit
JEDEC	Standard								
tAVAV	tWC	Write Cycle Time		45	55	70	90	120	ns
tAVEL	tAS	Address Setup Time		0	0	0	0	0	ns
tELAX	tAH	Address Hold Time		35	45	45	45	50	ns
tDVEH	tDS	Data Setup Time		20	20	30	45	50	ns
tEHDX	tDH	Data Hold Time		0	0	0	0	0	ns
	tOES	Output Enable Setup Time		0	0	0	0	0	ns
	tOEH	Output Enable Hold Time	Read	0	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling	10	10	10	10	10	ns
tGHEL	tGHEL	Read Recover Time Before Write		0	0	0	0	0	ns
tWLEL	tWS	$\overline{WE}$ Setup Time		0	0	0	0	0	ns
tEHWH	tWH	$\overline{WE}$ Hold Time		0	0	0	0	0	ns
tELEH	tCP	$\overline{CE}$ Pulse Width		25	30	35	45	50	ns
tEHEL	tCPH	$\overline{CE}$ Pulse Width High		15	20	20	20	20	ns
tWHWH1	tWHWH1	Programming Operation (min)		14	14	14	14	14	µs
tWHWH2	tWHWH2	Erase Operation (min) (Note 1)		2.2	2.2	2.2	2.2	2.2	sec
	tVCS	V_{CC} Set Up Time		2	2	2	2	2	µs

Note:

1. This also includes the preprogramming time.



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Figure 17. Alternate $\overline{CE}$ Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE (Note 2)

Parameter	Limits			Units	Comments
	Min.	Typ.	Max.		
Chip/Sector Erase Time		1	10 (1)	sec	Excludes 00H programming prior to erasure
Sector Programming Time		0.3		sec	
Chip Programming Time		2	12.5	sec	Excludes system-level overhead
Erase/Program Cycles	100,000			Cycles	
Byte Program Time		14		µs	
			60 (Note 3)	ms	

Notes:

1. The Embedded Algorithm allows for 60 second erase time for military temperature range operations.
2. The Embedded Algorithms allow for a longer chip program and erase time. However, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.
3. DQ_5 = "1" only after a byte takes longer than 60 ms to program.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9)	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

LCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

PDIP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

DATA RETENTION

Parameter	Min.	Units	Test Conditions
Min. Pattern Data Retention Time	10	Years	150°C
	20	Years	125°C

ADVANCE INFORMATION

Am29F040

524,288 x 8-Bit CMOS 5.0 V-Only, Sector Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% write and erase**
  - Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  - Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin PLCC/LCC
  - 32-pin TSOP
  - 32-pin DIP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - 70 ns maximum access time
- **Sector erase architecture**
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Embedded Erase™ Algorithms**
  - Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  - Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - 20 mA typical active read current
  - 30 mA typical write/erase current
  - 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector protection**
  - Hardware method disables any combination of sectors from write or erase operations

GENERAL DESCRIPTION

The Am29F040 is a 4 Mbit, 5.0 V-Only Flash memory organized as 512K bytes of 8 bits each. The Am29F040 is offered in a 32-pin package. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard Am29F040 offers access times between 70 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$) and output enable ($\overline{\text{OE}}$) controls.

The Am29F040 is entirely pin and command set compatible with JEDEC standard 4 Mbit E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The Am29F040 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. The entire memory is typically erased and verified in three seconds (if already completely programmed).

PRODUCT SELECTOR GUIDE

Family Part No:	Am29F040		
Ordering Part No: V_{CC} = 5.0 V ± 5%	–75		
V_{CC} = 5.0 V ± 10%	–70	–90	–120
Max Access Time (ns)	70	90	120
$\overline{\text{CE}}$ ($\overline{\text{E}}$) Access (ns)	70	90	120
$\overline{\text{OE}}$ ($\overline{\text{G}}$) Access (ns)	30	35	50

Publication# 17113 Rev. A Amendment/0
Issue Date: September 1992

If the device is blank, the entire memory is typically erased and verified in 10–11 seconds. Any individual sector is typically erased and verified in two seconds (if already completely preprogrammed). If the sector is blank, it is typically erased and verified in three seconds.

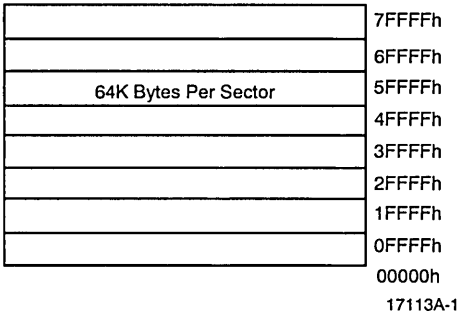
This device also features a sector erase architecture. The sector mode allows for 64K byte blocks of memory to be erased and reprogrammed without affecting other blocks.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7 or by the Toggle Bit feature on DQ_6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

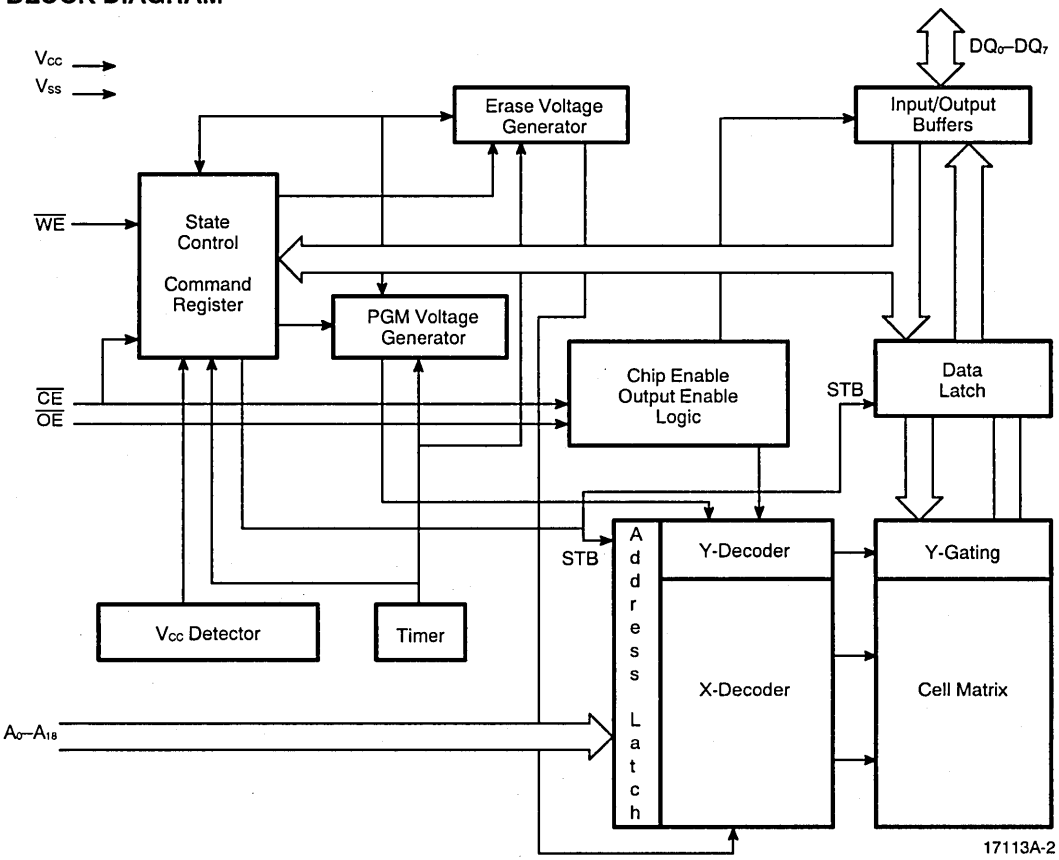
AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F040 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Flexible Sector-Erase Architecture

- 64K Bytes per sector
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable

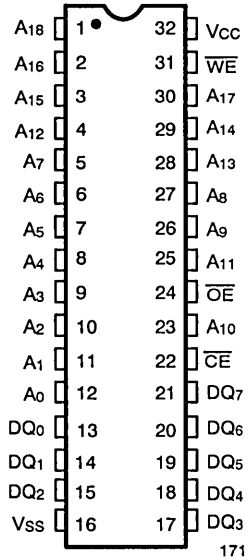


BLOCK DIAGRAM



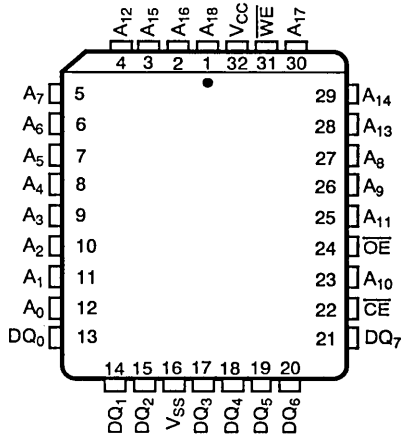
CONNECTION DIAGRAMS

CERDIP/PDIP



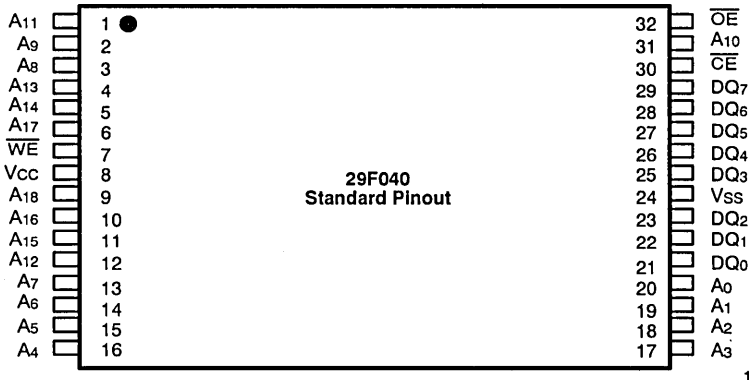
17113A-3

PLCC/LCC

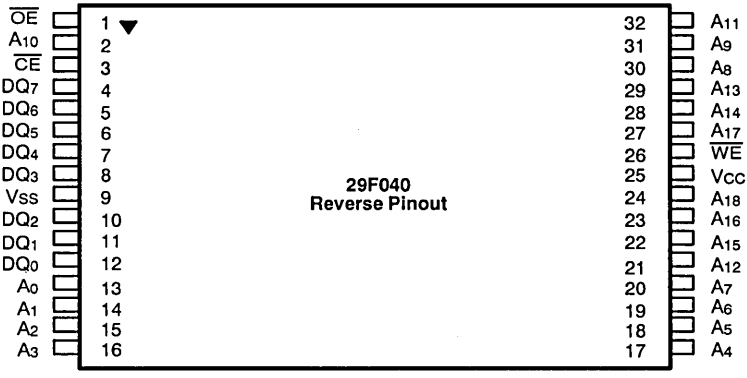


17113A-4

TSOP

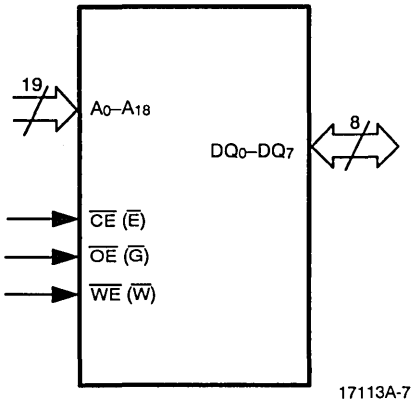


17113A-5



17113A-6

LOGIC SYMBOL



17113A-7

Table 1. Am29F040 Pin Configuration

Pin	Function
A_0–A_{18}	Address Inputs
DQ_0–DQ_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10% or ± 5%)
NC	No Internal Connection

ADVANCE INFORMATION

Am29F400

4-Megabit 524,288 x 8-Bit/262,144 x 16-Bit CMOS 5.0 V-Only, Sector Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% write and erase**
  - Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  - Uses same software commands as E^2PROMs
- **Industry-standard ROM pinout**
  - 44-pin SOP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - 70 ns maximum access time
- **Sector erase architecture**
  - Uniform sector size
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Embedded Erase™ Algorithms**
  - Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  - Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - 30 mA typical active read current
  - 40 mA typical write/erase current
  - 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector protection**
  - Hardware method disables any combination of sectors from write or erase operations

GENERAL DESCRIPTION

The Am29F400 is a 4 Mbit, 5.0 V-only Flash memory organized as 256K bytes of 16 bits each. Under control of the $\overline{\text{BYTE}}$ input, the device may also be read as 512K bytes of 8 bits each. When the $\overline{\text{BYTE}}$ input is LOW, AB functions as the least significant address input and 512K bytes of data can be accessed. The 8 bits of data will appear on DQ_0–DQ_7. The Am29F400 is offered in a 44-pin plastic SOP package. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard Am29F400 offers access times between 70 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$) and output enable ($\overline{\text{OE}}$) controls.

The Am29F400 is entirely pin and command set compatible with JEDEC standard 4 Mbit E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The Am29F400 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. The entire memory is typically erased and verified in three seconds (if already completely programmed).

PRODUCT SELECTOR GUIDE

Family Part No:	Am29F400		
Ordering Part No: V_{CC} = 5.0 V ± 5%	–75		
V_{CC} = 5.0 V ± 10%	–70	–90	–120
Max Access Time (ns)	70	90	120
$\overline{\text{CE}}$ ($\overline{\text{E}}$) Access (ns)	70	90	120
$\overline{\text{OE}}$ ($\overline{\text{G}}$) Access (ns)	30	35	50

Publication# 17096 Rev. A Amendment/0
Issue Date: September 1992

If the device is blank, the entire memory is typically erased and verified in 10–11 seconds (x8) and 5–6 seconds (x16).

This device also features a sector erase architecture. The sector mode allows for blocks of memory to be erased and reprogrammed without affecting other blocks.

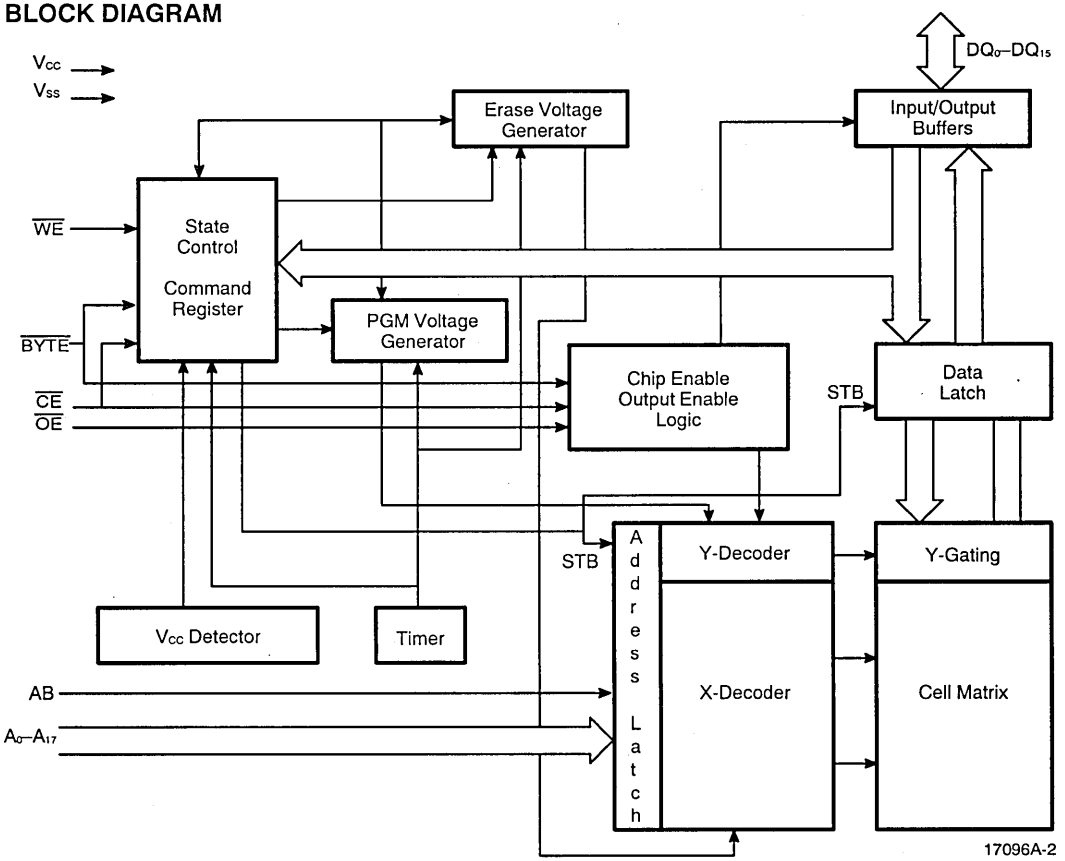
The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7 or by the Toggle Bit feature on DQ_6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F400 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

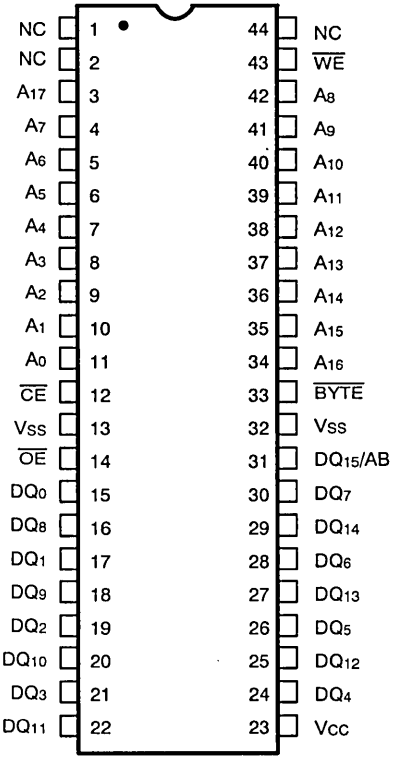
Flexible Sector-Erase Architecture

- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable

BLOCK DIAGRAM

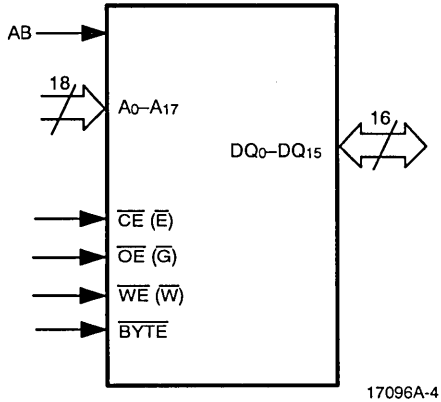


CONNECTION DIAGRAMS



17096A-3

LOGIC SYMBOL



17096A-4

Table 1. Am29F400 Pin Configuration

Pin	Function
AB	Address Input (BYTE Mode)
A_0–A_{17}	Address Inputs
DQ_0–DQ_{15}	Data Input/Output
CE	Chip Enable
OE	Output Enable
WE	Write Enable
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10% or ± 5%)
NC	No Internal Connection
BYTE	Byte/Word Switch

Reprogrammable Flash BIOS Design Using AMD's Am29F010

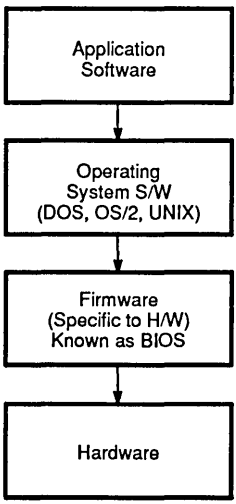
Application Note
by Kumar Prabhat

Advanced Micro Devices

This application note describes the general overview and various system level issues for a reprogrammable Flash BIOS design. Any system designer, whether notebook or desktop system, will benefit from this discussion. This application note also describes the AMD Am29F010 5.0 V-only, sector erase part and why it is an ideal choice for a reprogrammable BIOS design.

INTRODUCTION TO BIOS

Every individual computer system consists of three basic blocks – Hardware, Hardware Specific Firmware commonly named BIOS and System Software.



17078A-1

BIOS is a hardware dependent software normally stored in an EPROM, which provides an interface between specific hardware and system software. It interfaces with various hardware components like core logic chipset, graphics controller, the keyboard and disk drive. Any application software and operating system software (i.e., DOS, OS/2 and UNIX) runs above it and uses various BIOS procedures. IBM has defined various BIOS procedures to control specific peripheral functions. Some of them are mentioned as follows:

INT 13H	Disk Drive Control
INT 17H	Printer Control
INT 10H	VGA Control
INT 16H	Keyboard Control
INT 14H	Serial Communication Control

To use the BIOS procedure you load the parameters required by the procedure and then execute the INT# instruction that accesses that procedure. For example, you can use the BIOS INT 10H procedure for 15 different functions related to the CRT display. Some of these functions are: set display mode, set color palette, write dot and write character to screen. You specify the function you want by loading the number for that function in the AH register before executing the INT 10H instruction.

All of the 80X86 procedures boot up from the BIOS located at the very top of the 1 Mbyte memory map which is F0000H – FFFFFH. In addition 64K bytes of space lying in the address range E0000H – EFFFFH is provided for any BIOS extension.

The BIOS also contains various initialization routines to initialize system components like the serial port, DMA Controller and Interrupt Controller. During power-on it does the Power On Self Test (POST) routines. It also checks for basic system RAM functionality. If the system passes the RAM functionality, the BIOS will copy itself to the top 64K byte area of 1 Mbyte main memory. This is known as shadowing BIOS which improves the system performance since the BIOS code is run at DRAM speeds instead of slower ROM speeds.

WHY THE NEED FOR REPROGRAMMABLE BIOS

The concept of a personal computer is changing rapidly as technology progresses. Yesterday's high-end systems are becoming today's standard platforms and new technologies have brought enhanced system capabilities into the user's hands. The fastest growing segments of the computer market are in Notebooks and other portable PCs. Increasing demands for sophisticated hardware and intelligent power saving algorithms have increased the complexity of BIOS code. In the desktop computers area, the enhanced support of Ethernet/SCSI Controller on the PC motherboard also increases the need for BIOS modifications to support sophisticated peripherals. On the high-end, EISA systems need to store hardware specific configurations which are traditionally stored in battery-backed-up SRAMs. Today's

Publication# 17078 Rev. A Amendment/0
Issue Date: September 1992

PC BIOS is no longer a standard product except for the basic 64K byte compatibility portion. The remaining 64K byte area has a significant potential to change with the addition of Power Management software and new setup utilities. To summarize, we see the potential change in BIOS code at every stage of manufacturing like design, debugging, testing and production. Code modifications with EPROMs do not provide a cost effective and timely solution since a UV Eraser and a separate EPROM programmer are required.

Flash Memories offer a superior solution for this kind of application. Code prototyping time is significantly reduced because Flash Memories can be updated with new code in a manner of seconds while still in the system. Board level diagnostics, final system test, and customer specific configuration code can all be down-loaded into the Flash memory electrically on the assembly line. Devices may be soldered directly to the system board. This reduces the cost associated with the BIOS socket and also eliminates the need to disassemble the system and replace socketed devices. Moreover, it will remove the prohibitive costs associated with a field service call. When updates to system code or system reconfiguration is necessary, these costly service calls may be replaced with remote updates or by distributing floppy disks with new data.

AMD FLASH MEMORY

This section provides a brief overview of AMD's 5.0 V-only Flash memory and in particular, AMD's Am29F010 5 V-only, Sector Erase part.

AMD's 5.0 V-Only Flash Memory Technology

This section illustrates the fundamentals of AMD's Flash Memory Technology. AMD's Flash memory technology is very similar to that of our UV EPROM. The main difference is associated with the Fowler-Nordheim tunneling erase mechanism.

During program operations AMD's Flash memories transfer and store charge on a floating gate in a manner similar to EPROM. This provides data retention that is equivalent to that of EPROM devices. The device is programmed by raising the control gate and drain terminal to a high voltage. The source terminal is grounded. The voltage potential across the channel attracts channel electrons from the source area towards the drain. At the drain region, some of these channel electrons become "hot" electrons and are swept up through the thin oxide where they are trapped on the floating gate. The electrons stored on the floating gate create an electric field which turns off the memory transistor and represents a logic zero.

AMD's 5.0 V-only, Flash memory uses Negative Gate Erase Technology for erase operations in order to minimize the current drawn from the erase change pump. AMD's Negative Gate Erase technique actually provides the same electric fields to the Flash memory cell and uses the same erase mechanism as its 12.0 V Flash devices. A negative voltage of –10.5 V is applied to the control gate while the source terminal is at 5.0 V supplied by the system V_{CC} supply. Negative Gate Erase is used in order to reduce the current drawn from the erase charge pump. The band-to-band tunneling current (10–20 mA peak) comes directly from the system V_{CC} supply through the Array around terminal. This is the most efficient way to use an existing system V_{CC} supply. The current required from the Negative Gate Erase charge pump is less than 10 µA at –10.5 V. This significantly reduces the internal power consumption in relation to conventional 12.0 V approaches.

The Am29F010

This section describes the various features of the Am29F010.

General Description

The Am29F010 is a 1 Mbit 5.0 V-only "Flash" electrically erasable, electrically programmable read only memory organized as 128K x 8 bits. It is a 32-pin device which allows upgrades to 4 Mbit densities. The device has uniform sector architecture with 100,000 minimum endurance cycles per sector.

The Am29F010 is entirely pin and software compatible with the 5.0 V-only JEDEC standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. With the appropriate command sequence written to the register, standard microprocessor read timings output array data, access the auto-select codes or output data for erase and program verification. Reading data out of the device is similar to reading from 12 V Flash or EPROM devices.

Embedded Algorithms

The Am29F010 is programmed and erased using Embedded Algorithms, which completely automates the program and erase operation. The Am29F010 is programmed by executing the Program Command sequence (see Appendix A). The Embedded Programming™ Algorithm automatically times the programming pulse width and verifies the proper cell margin. Chip erase is done by executing the erase command sequence. The Embedded Erase™ Algorithm automatically verifies if the entire array is programmed and if it is not, the algorithm will automatically pre-program it before beginning electrical erase.

The Am29F010 features $\overline{\text{Data}}$ Polling and Toggle Bit functions as a method to indicate to the host system when the Embedded Algorithms are in progress or com-

pleted. During the Embedded Program Algorithm an attempt to read the device will produce compliment data of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, DQ7 will be "0" until the erase operation is completed. Upon completion of Embedded Erase Algorithm data at DQ7 will be "1". The device also features a "Toggle Bit" as another method to indicate to the host system when the Embedded Algorithms are in progress or completed. During an Embedded Program or Erase Operation, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Operation is completed, DQ6 will stop toggling and valid data will be read. Upon completion of the Embedded Algorithm the device returns to the read mode. The Am29F010 will also indicate through DQ5, if the program or erase time has exceeded the specified limits. Under these conditions DQ5 will produce "1" which will indicate that the program or erase cycle was not successfully completed. Then DQ4 will indicate which algorithm exceeded the limits. A "0" in DQ4 indicates a programming failure, a "1" indicates an erase failure.

The automatic nature of the Embedded Algorithms provide various benefits over standard algorithms. Embedded Algorithms increase the system level performance significantly by reducing the CPU's overhead associated with the repetitive nature of standard algorithmic commands. This frees up the CPU to execute other system level tasks.

Sector Based Architecture

The Am29F010 also features a sector erase architecture. The whole memory content of the device is divided into eight sectors of equal size. The sector architecture allows for 16K byte segments of memory to be erased and reprogrammed without affecting other sectors. The device also supports hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 7). Please refer to the data sheet for more details on sector protection.

Sector erase requires a six bus cycle command similar to standard E²PROMs (see Appendix A). There are two unlock write cycles followed by writing the "set-up" command. Two more unlock write cycles are then followed by the sector erase command. On this sixth bus cycle, sector address defined by higher address lines A16, A15 and A14 is latched on the falling edge of $\overline{WE}$, while the sector erase command (30h) is latched on the rising edge of $\overline{WE}$. Multiple sectors may be erased concurrently by writing the six bus cycle command as described above followed by a sector erase command with other sector addresses. A time-out of 100 µs from the rising edge of the $\overline{WE}$ pulse of the last sector erase command will initiate the sector erase operation. If another sector erase command is written within the 100 µs time-out window the timer is reset. Any command other than sector erase within the time-out window will reset the device to the read mode, ignoring the previous command string. The device will indicate this time-out through the DQ3 pin. If DQ3 is high the internally controlled erase cycle has begun, and attempts to write additional commands to the device will be ignored until the erase operation is completed as indicated by the $\overline{Data}$ Polling or Toggle Bit. If DQ3 is low, the sector erase timer window is still open and the device will accept additional sector erase commands. The system software should check the status of DQ3 prior to and following each sector erase command.

Am29F010 – An Ideal Choice

- The Am29F010 has an access time of as fast as 45 ns which will provide true 0 wait state performance in very high speed designs without downloading the code to the Shadow RAM.
- The device incorporates Embedded Algorithms which reduces software overhead for system designer and it also increases system performance since CPU will be free to do other tasks during reprogramming operations.
- The device provides a minimum of 100,000 write endurance cycles per sector. This kind of high endurance is especially important in the emerging markets of embedded flash disks and removable cards.
- Since the Am29F010 is a 5.0 V-only device, it eliminates the need for DC to DC converter circuitry to translate the system level voltage level from 5.0 V to 12.0 V for write and erase operations. This also simplifies the hardware design, results in reduced board space and reduces the system cost by approximately $4.00 to $5.00.
- As the power consumption is proportional to the square of operation voltage, 5.0 V operation reduces the power consumption significantly during programming and erase operation.
- Sector erase architecture is another added advantage which is valued by many system designers. The Am29F010 provides a system designer eight sectors to use in their designs in order to add more functions to the system. It also eases the design and debugging process by allowing a system designer to erase a single sector during code modification. This brings the program modularity to the system.
- The device also incorporates several features to prevent inadvertent writing of the part.
  - During the power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). Under these conditions, the command register is disabled and all internal program/erase circuits are disabled.

- The device ignores the noise pulses or glitches of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ and will not initiate a write cycle.
- During power-up of the device even with $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH}, the device will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode.

Packaging Details

AMD's Am29F010 is being offered in three standard 32-pin packages: Plastic Dual In-Line Package (PDIP), Plastic Leaded Chip Carrier (PLCC), Leadless Chip Carrier (LCC) and Thin Small Outline Package (TSOP). See Figures 1 and 2 for pin-out details.

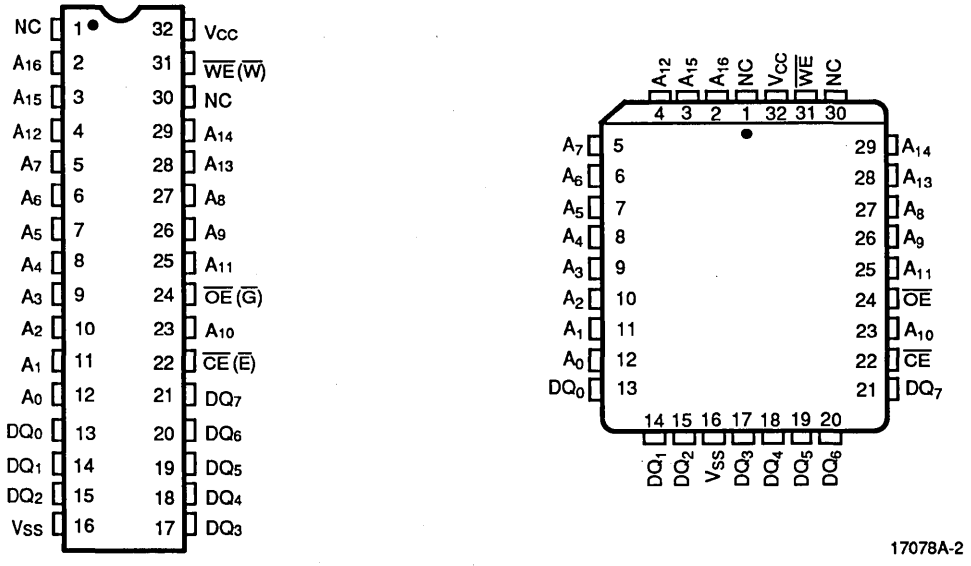


Figure 1. Am29F010 DIP, PLCC and LCC Pin-Out

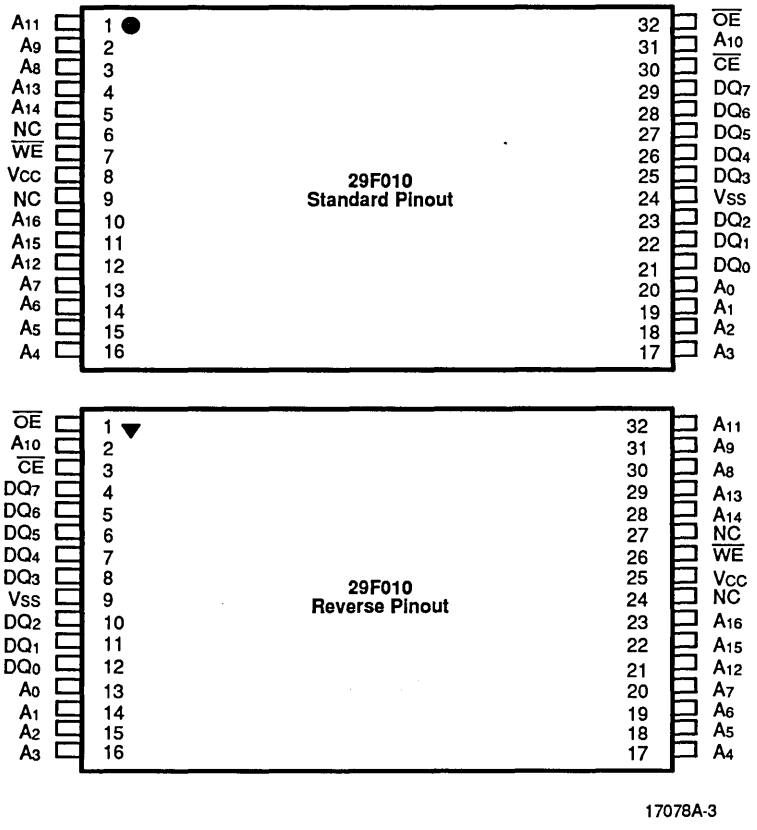
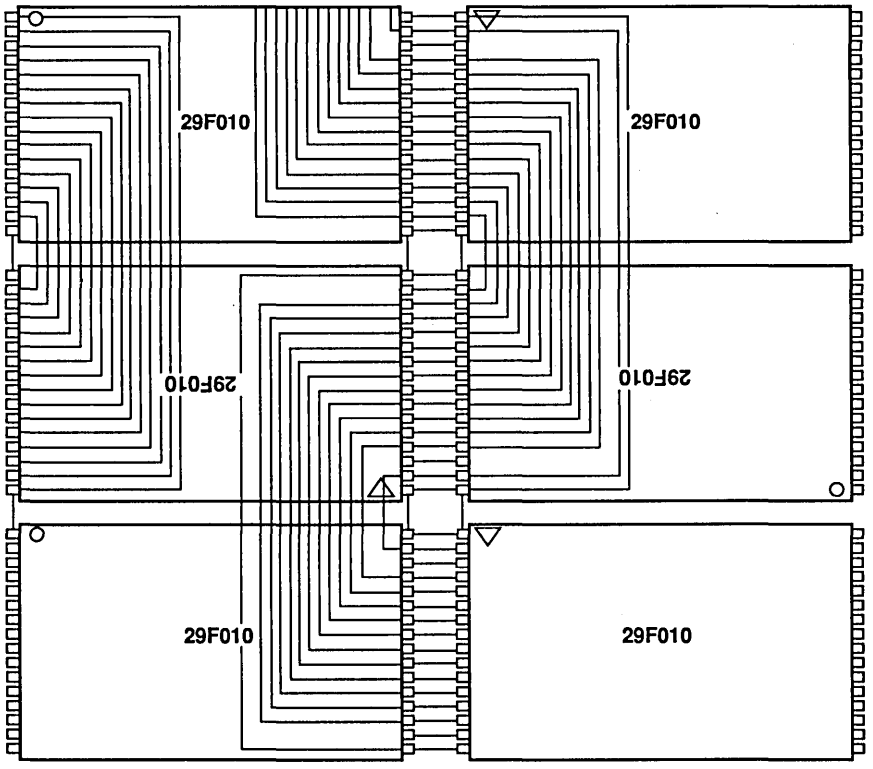


Figure 2. Am29F010 TSOP Pin-Out

Thin Small Outline Package

The TSOP is the industry's leading edge plastic, surface mountable memory package. System requirements for higher density and smaller, high density memory arrays are driving this packaging trend. It is becoming the standard choice for hand-held equipment and palmtop/ laptop computers as well as memory cards. This package comes in standard and reverse 32-pin options and is available in the 8 mm x 20 mm x 1.27 mm package outline. In addition to the TSOP's low height profile, maximum board space is achieved with the dual-in-line and standard/reverse pinouts. Board layers can be reduced because traces are routed under the two sides of the package that do not have leads. This allows packages to be mounted side-by-side and end-to-end. All pins except chip enable pins can be connected in parallel. This is accomplished by using standard and reverse pin-out packages in an alternating sequence as shown in Figure 3.



O = Pin 1 indicator for standard bend pinout

△ = Pin 1 indicator for reverse bend pinout

17078A-4

Figure 3. Optimum Board Layout with TSOP

SYSTEM LEVEL DESIGN ISSUES

This section describes various system level design considerations for the support of reprogrammable BIOS.

Hardware Design Consideration

This section describes the modifications required in the standard PC-AT motherboard to support the Flash BIOS. Below is the block level diagram of a PC-AT motherboard supporting reprogrammable Flash BIOS.

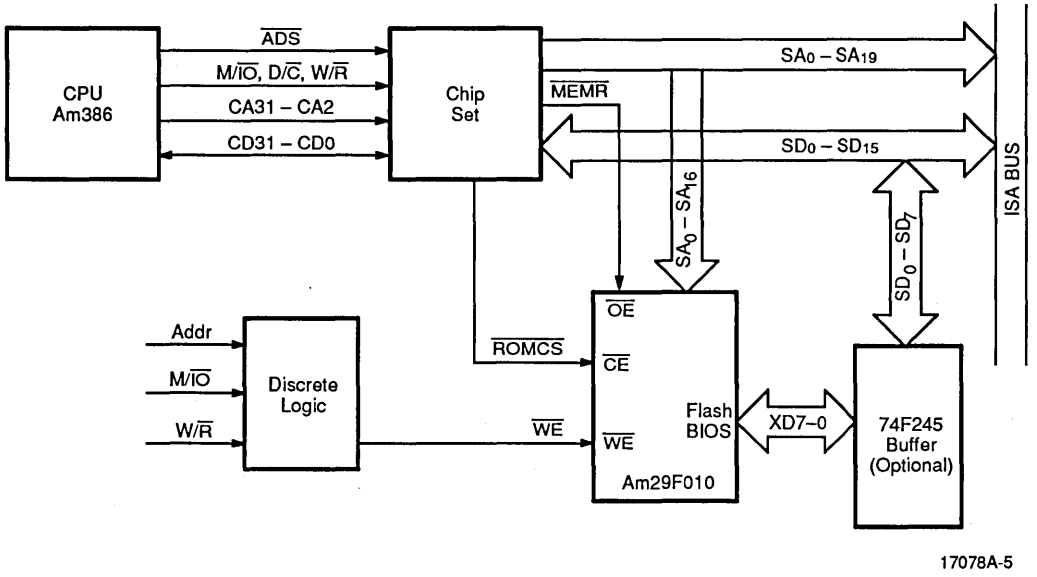


Figure 4. PC-AT Motherboard with Flash BIOS

Looking at the above block diagram we come across two main considerations for supporting the Flash based reprogrammable BIOS:

- All write accesses to EPROM address space are directed to the ISA bus and effectively discarded. Since standard PC chip sets do not generate MEMWR with ROMCS. WE for Flash EPROM must be generated externally.
- Standard PC motherboards do not support writes to the BIOS EPROM. If the chip set data buffer works only in one direction, a data buffer is required that works in both read and write directions in order to support Flash BIOS.

WE generation for Flash EPROM can be generated by using simple discrete circuitry to decode the BIOS addresses range (E0000H – FFFFFH), M/IO, and W/R. Figure 5 shows the generation of WE signal.

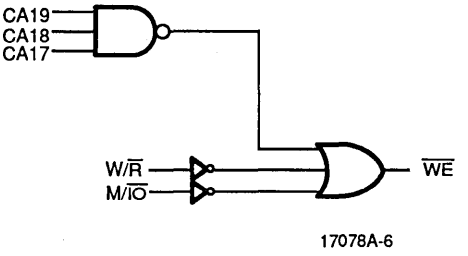


Figure 5. WE Generation Circuit

Considerations for In-System Programming

In traditional PC motherboard design, the EPROM containing BIOS, is normally socketed and disassembled from the board. Flash EPROMs eliminate the need to disassemble the system and replace the socketed device in order to update System BIOS. Flash devices may be soldered directly to a printed circuit board since they support in-system programming.

Before soldering the Flash memory on the board, the manufacturer may initially program the boot code and any other codes which have to be protected. Boot codes may be protected using external programming equipment or by AMD. To activate these modes, the programming equipment must force 12 V on the device. The particular sector will be selected using high order address lines A14, A15 and A16. Once the device is soldered into the board, the rest of the programming is done by using the local CPU. The Boot code is not meant to be changed once it is protected. However, its content may be altered by using the Sector Unprotect feature of the device and then reprogram the device with a new code. Please refer to the data sheet for more details on sector protect and unprotect.

Software Design Consideration

Let us take the BIOS design example using the AMD's Flash device Am29F010 as shown in Figure 6. BIOS Code has been divided into various modules like Boot Code, System BIOS, VGA BIOS, Power Management Code etc., and each sector may be used for individual modules.

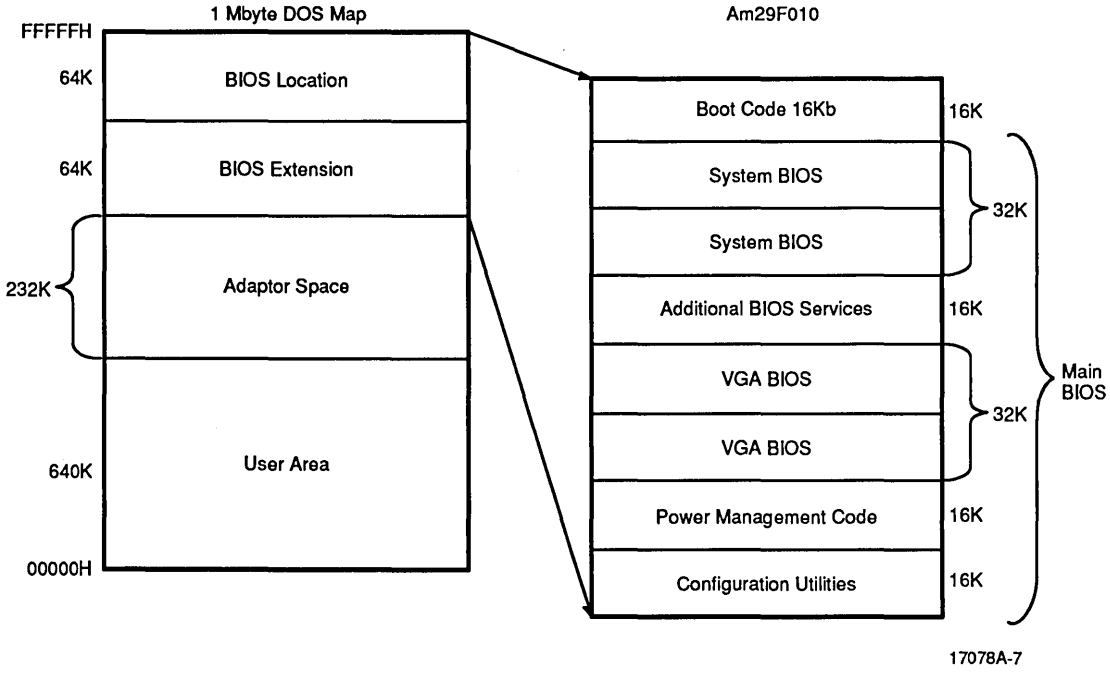


Figure 6. BIOS Design with Am29F010

Please note that the only difference between the standard BIOS and Flash BIOS is the addition of Boot Code located in a separate sector. The Boot Code resides in the system address FC000h – FFFFFh and contains the minimum code needed to boot up the system so that other blocks can be reprogrammed if required. Boot Code consists of:

- 16-byte jump vector
- BIOS check sum routine
- Recovery code

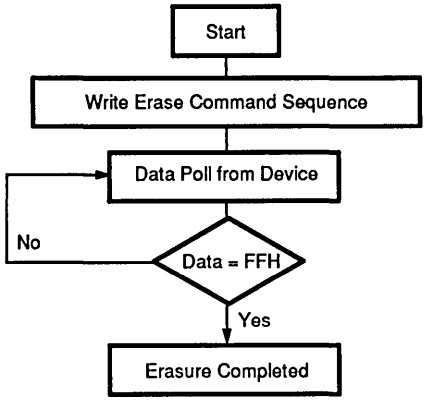
The Recovery Code contains various initialization routines and basic minimum routines for system start-up.

  - System timer
  - DMA/Interrupt function
  - Keyboard
  - Floppy drives

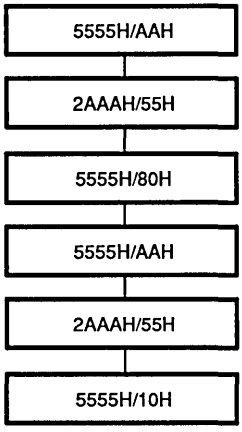
- During power on Boot Code takes control of the system
  - It uses the BIOS checksum routine to check for valid main BIOS.
- If the main BIOS is valid, system RAM is checked and the main BIOS code is copied into the system DRAM memory and continue the boot operation. This feature is known as shadow memory and is used by most PC designs.
- If BIOS checksum determines an invalid BIOS, the system gives control to the recovery code for boot operation. The recovery code initializes the system RAM and floppy drive. Using basic minimum routines, it boots up the system from floppy drive and displays the message to insert the BIOS update diskette.
- The BIOS update diskette will contain:
  - Reprogramming utility
  - BIOS code
- The reprogramming utility is loaded into system RAM and used to reprogram the main BIOS from the diskette.

The above procedure may be also used to modify the main BIOS code.

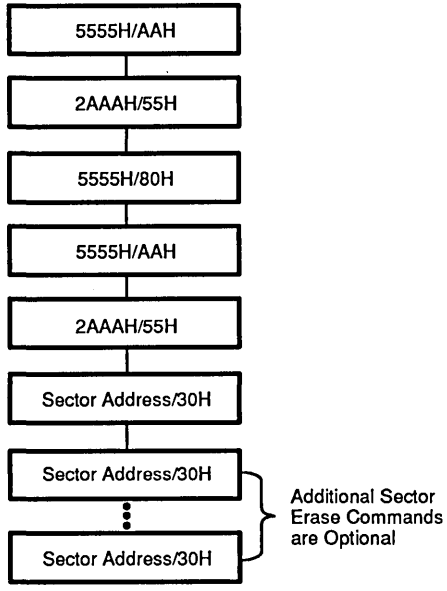
Appendix A
Flowcharts for Am29F010 Programming and Erase Algorithm



Chip Erase Command Sequence (Address/Command):

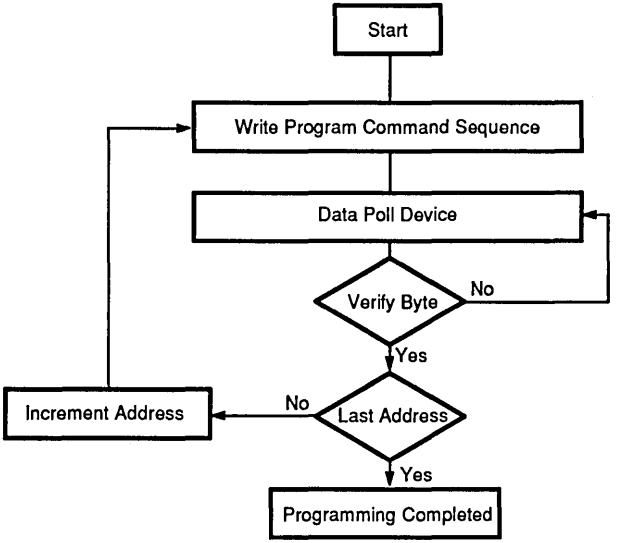


Sector Erase Command Sequence (Address/Command):

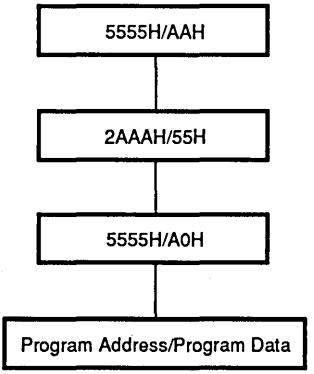


17078A-8

Embedded Erase Algorithm

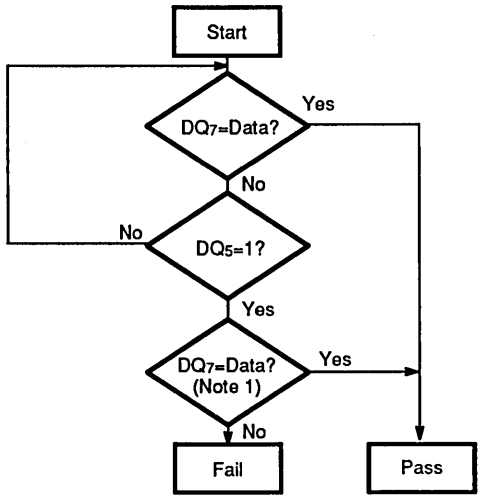


Program Command Sequence (Address/Command):



17078A-9

Embedded Programming Algorithm

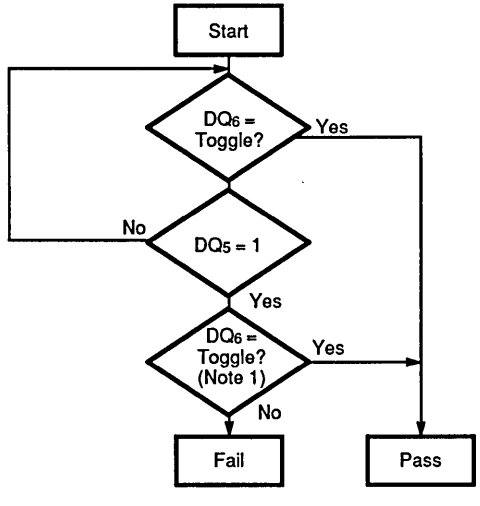


17078A-10

Note:

1. DQ_7 is rechecked even if $DQ_5 = 1$ because DQ_7 may change simultaneously with DQ_5.

$\overline{\text{Data}}$ Polling Algorithm



17078A-11

Note:

1. DQ_6 is rechecked even if $DQ_5 = 1$ because DQ_6 may stop toggling at the same time as DQ_5 changing to "1".

Toggle Bit Algorithm

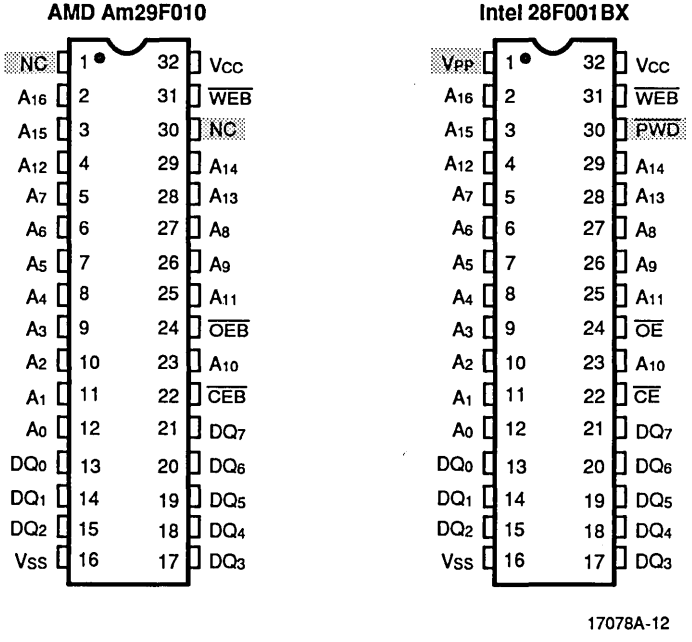
Appendix B
Interchangability of Intel's 28F001BX and AMD's Am29F010

INTERCHANGABILITY OF INTEL AND AMD PART IN THE SAME DESIGN

Let us compare the AMD's 5.0 V Flash device Am29F010 vs. Intel's Boot Block part 28F001BX in terms of hardware and software compatibility.

Hardware level compatibility issues

Here is the pin out shown for both AMD and Intel Flash devices.



17078A-12

The differences in pin-out are:

- Am29F010 does not have V_{PP} pin. It has been changed to NC
- Intel device 28F001BX has one added pin $\overline{PWD}$ for deep power down mode

Since pins 1 and 30 are NC for AMD part Am29F010 and these two pins are not connected internally, the AMD Flash device Am29F010 may be used as a drop in replacement for a design supporting Intel Boot Block Flash device 28F001BX.

Software Level Compatibility Issues

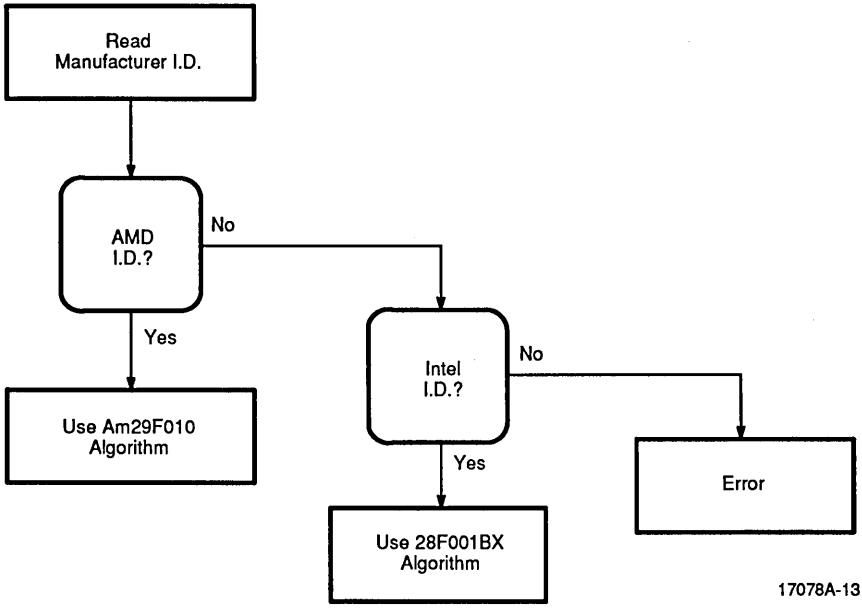
AMD's Am29F010 and Intel 28F001BX has different set of command definitions (5 V commands vs. 12 V commands). However, both the devices have similar commands for reading manufacturer I.D. This may be explained better by the following table and flowchart.

Command Structure for Reading I.D.

	1st Bus Cycle (Write Cycle)		2nd Bus Cycle (Write Cycle)		3rd Bus Cycle (Write Cycle)		4th Bus Cycle (Read Cycle)	
	Addr	Data	Addr	Data	Addr	Data	Addr	Data
	5555H	AAH	2AAAH	55H	5555H	90H	0000H	Mfg I.D.
AMD	Unlock Cycle		Unlock Cycle		I.D. Command			0001H
Intel	Ignored		Ignored		I.D. Command			0089H

- The initial two bus cycles are unlock cycles for AMD's 5.0 V-Only Flash part Am29F010. They are undefined commands for Intel 28F001BX, so ignored by the Intel device and the device remains in Read Mode.
- The address on the 3rd bus cycle for Intel Boot Block device 28F001BX is XXXXH (don't care) and 90h code puts both devices in I.D. mode.

The above discussion confirms that a software code written to read Manufacturer I.D. for AMD Flash device Am29F010 may be also used to read Manufacturer I.D. for Intel Flash device 28F001BX.



Flowchart to Support Both AMD Am29F010 and Intel 28F001BX

Design-In with AMD's Am29F010

Advanced Micro Devices

Application Note
by Kumar Prabhat

This application note describes the key features and system level benefits of using AMD's Am29F010, 5.0 V-only Sector Erase Flash Memory. It also explains how to use AMD's Am29F010 in an existing Intel Boot Block 28F010BX Flash based design and discusses the various hardware and software issues.

BENEFITS OF AMD'S AM29F010

- Since the Am29F010 is a 5.0 V-only device it eliminates the need for DC to DC converter circuitry to translate the system voltage level from 5.0 V to 12.0 V, for write and erase operations. This simplifies the hardware design, results in reduced board space, and lowers the system cost by approximately $4.00 to $5.00. Please refer to Appendix B for DC/DC converter circuitry required for 12 V flash device. 5.0 V-only programming also reduces the total system level power consumption. Below is a summary of the system level power calculations for the Am29F010 vs. 12.0 V Flash devices during reprogramming.

Device Level Reprogramming Power Consumption

Am29F010	12.0 V Flash Memory
V_{CC} Power = 5.0 V (V_{CC}) x 40 mA (I_{CC}) = 200 mW	V_{CC} Power = 5.0 V (V_{CC}) x 30 mA (I_{CC}) = 150 mW

DC/DC Converter Reprogramming Power Consumption

Am29F010	12.0 V Flash Memory
V_{PP} Power not required	V_{PP} Power = 12.0 V (V_{PP}) x 30 mA (I_{PP}) + DC to DC converter efficiency = 450 – 720 mW

12.0 V Flash memories require more system level power since 5.0 V to 12.0 V conversion circuitry is not 100% efficient. The typical efficiency of the DC to DC converter is between 50% to 80%.

Total System Level Power Consumption (Reprogramming)

Flash Memory Type	Device Level	DC/DC Converter	Total System Level Power
Am29F010	200 mW	0	200 mW
12.0 V Flash	150 mW	450 – 720 mW	600 – 870 mW

- The Am29F010 provides a minimum of 100,000 write endurance cycles per sector. This kind of high endurance is especially important in the emerging markets of embedded Flash disks and removable memory cards. Typical endurance last well beyond the 100,000 cycle minimum.
- The 16 Kbyte sector erase architecture is another added advantage which is valued by many system designers. This feature provides the capability to selectively rewrite portions of the memory array while leaving the rest of the memory contents fixed. This architecture simplifies the design and debugging process by providing program modularity to the system. Individual sectors may also be hardware protected.
- The Am29F010 has an access time of as fast as 45 ns which will provide true 0 wait state performance in very high speed designs.
- The device incorporates AMD's Embedded Algorithm which reduces software overhead for the system designer. It also increases system level performance since the CPU will be free to do other tasks during reprogramming operations.
- The device also incorporates several features to prevent inadvertent write cycles.
  - During power-up and power-down, write cycles are locked out when V_{CC} is less than 3.2 V (typically 3.7 V). Under these conditions, the command register is disabled and all internal program/erase circuits are disabled.
  - The device ignores noise pulses or glitches of less than 5 ns (typically) on control signals $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$ and will not initiate a write cycle.
  - During power-up of the device even with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$, the state machine will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode.

Publication# 17097 Rev. A Amendment/0
Issue Date: September 1992

DESIGN-IN WITH AMD'S AM29F010

Hardware Pin-Out Details

The Am29F010 is available in 32-pin DIP/PLCC/TSOP packages. The pin-out is compatible with JEDEC standard 1 Mbit E^2PROMs and also provides for easy upgrades to 4 Mbit densities. Below is the DIP pin-out for the AMD's Am29F010 and upcoming 4 Mbit 5.0 V-only, sector erase Flash memory device.

The only differences in pin-out are Pin 1 and Pin 30 which are NC in the Am29F010 pin-out and used as higher address lines A18 and A17 for the 4 Mbit Flash device. A system designer may design with a 1 Mbit part today and upgrade it with a 4 Mbit memory without any layout change in the board.

In fact, Am29F010 may be also used as an ideal upgrade to a 28F010 Flash-based design without any layout change. The only difference between Am29F010 and 28F010 pin-out is Pin 1 which is NC in Am29F010 and used as V_{PP} pin for 28F010.

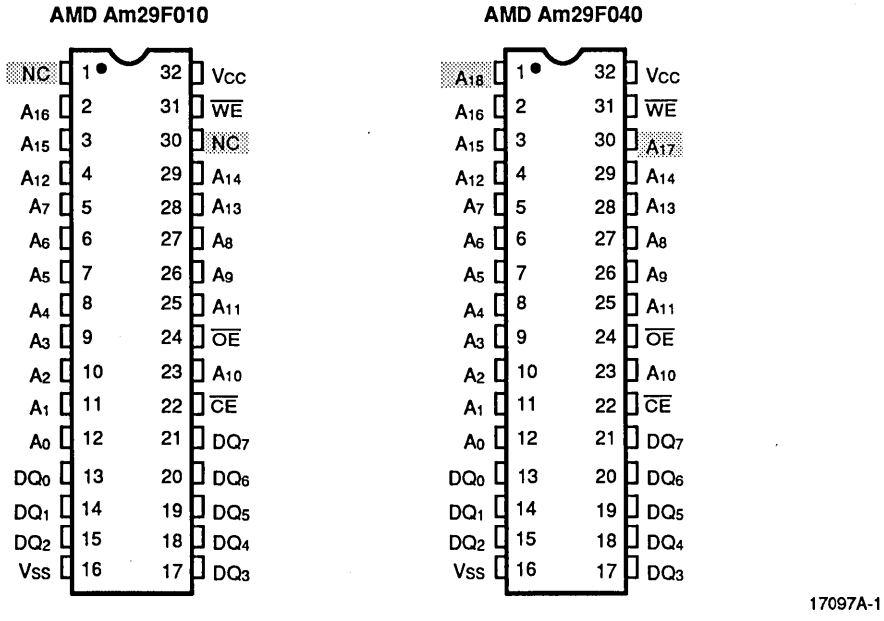


Figure 1

Replacing the 28F001BX with Am29F010

By changing the software only, AMD's Am29F010 may be used to upgrade a system using Intel's 12.0 V 28F001BX, 1 Mbit boot block flash device to 5.0 V only operation. Please refer to Figure 2 for a pin-out comparison between the Am29F010 and the 28F001BX.

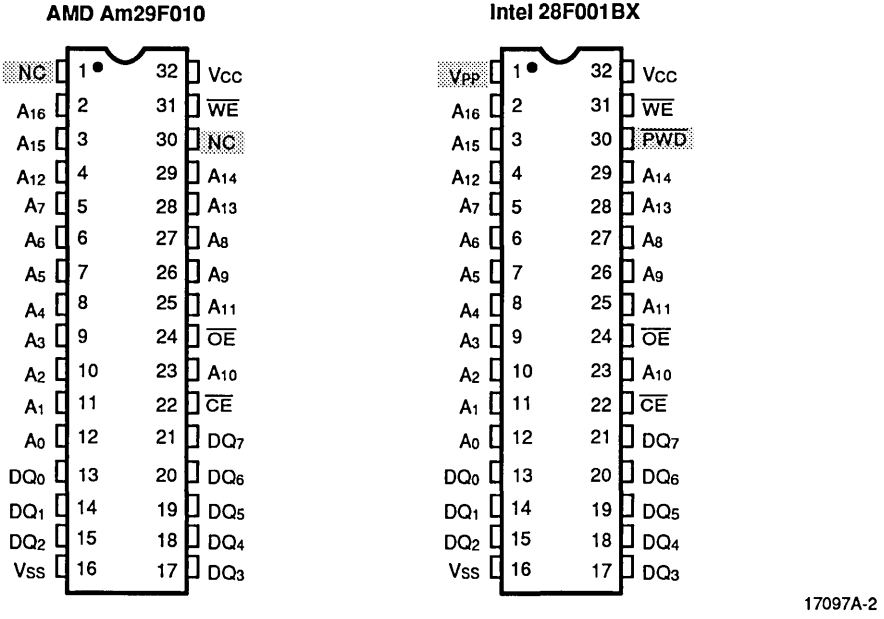


Figure 2

Hardware Pin Out Comparison

There are two differences in pin-out for AMD Am29F010 and Intel 28F001BX:

- The Am29F010 does not use V_{PP} (Pin 1) and it is not connected internally to the device.
- Intel's 28F001BX has added pin $\overline{PWD}$ (Pin 30) to support deep power-down mode. AMD's Am29F010 does not support the power-down function.

Since Pin 1 and Pin 30 are NC for AMD's Am29F010, it is 100% hardware compatible with the 28F001BX Flash device and may be used as a drop in replacement if the power down function is not required.

Software Command Structure

AMD's Am29F010 uses the JEDEC standard 1 Mbit E^2PROM 5.0 V-only multi-sequence command set. Please refer to Table 1 for Am29F010 command definitions.

Table 1.
Am29F010 Bus Command Structure

Command Sequence	Bus Write Cycles Required	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	4	5555H	AAH	2AAH	55H	5555H	F0H						
Read I.D.	4	5555H	AAH	2AAH	55H	5555H	90H						
Byte Program	4	5555H	AAH	2AAH	55H	5555H	A0H	Byte Addr	Data				
Chip Erase	6	5555H	AAH	2AAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	Sector Addr	30H

These commands allow the user to program data on a byte by byte basis and erase any combination of sectors or even the entire device at once.

Common Device I.D. Command for AMD's Am29F010 and Intel's 28F001BX

Although the specific commands used to implement the program and erase algorithms are different between the Am29F010 and the 28F001BX, one command sequence may be used to determine whether the AMD or Intel device is in the system. The flow chart below shows how to determine the device I.D. and then jump to the appropriate algorithm.

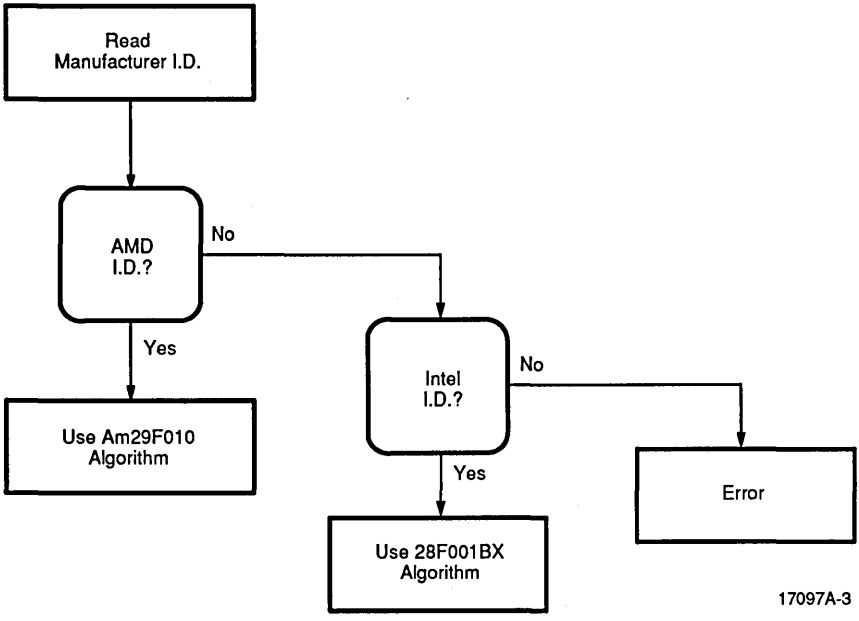


Figure 3

Table 2 details a common software sequence that allows the system to determine which device is on board and shows how to use the appropriate algorithm.

Note that the sectoring differences between the two devices must be considered in the software design to replace the 28F001BX with Am29F010. We have not discussed it in this application note since it is an application specific implementation.

Table 2

	1st Bus Cycle (Write Cycle)		1st Bus Cycle (Write Cycle)		1st Bus Cycle (Write Cycle)		1st Bus Cycle (Write Cycle)	
	Addr	**Data**	**Addr**	**Data**	**Addr**	**Data**	**Addr**	**Data**
	5555H	AAH	2AAAH	55H	5555H	90H	0000H	Mfg. I.D.
AMD	Unlock Cycle		Unlock Cycle		I.D. Command			0001H
Intel	Ignored		Ignored		I.D. Command			0089H

Embedded Algorithm – Write Operation Status

The Am29F010 features $\overline{\text{Data}}$ Polling and Toggle Bit methods as ways to indicate to the host system when the Embedded Algorithms are in progress or completed. The status is available from the device once the Embedded Algorithm has begun.

$\overline{\text{Data}}$ Polling: During the embedded operation, an attempt to read the device will produce complement data of the true data being written to DQ7. Once the embedded operation is completed, an attempt to read the device will produce the true data expected from the device. Upon the completion of an Embedded Algorithm operation the device returns to the read mode.

Toggle Bit: During and embedded operation, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the embedded operation is completed, DQ6 will stop toggling and valid data will be read. Upon completion of an Embedded Algorithm operation the device returns to the read mode.

Sector Architecture

The AMD Am29F010 is a 1 Mbit Flash Memory device organized as 128K bytes of 8 bits each. It is divided into eight equal size sectors of 16K bytes each. Any combination of sectors can be individually or concurrently erased.

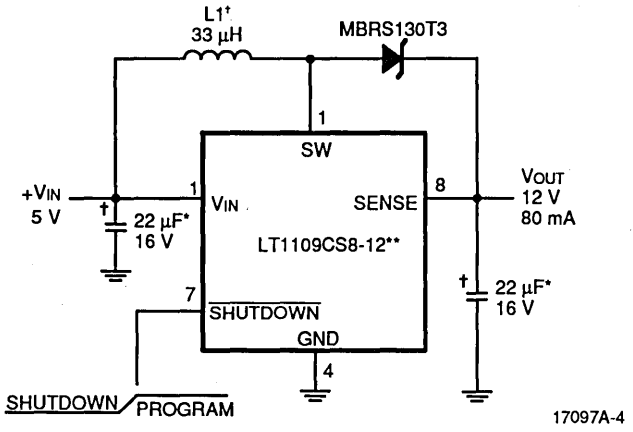
In addition, any combination of sectors or any individual sector may be write protected. Since the sector protect feature of the Am29F010 requires 12.0 V, it is typically done by using the external programming equipment at the user's site. Alternatively, AMD will program and protect the sectors as desired prior to shipment. In the protect mode, any individual sector may be selected. Protected sectors may also be unprotected if it is desired. Please refer to the data sheet for more details on sector protection and unprotection.

The fully-sectored architecture of the Am29F010 provides a system designer a much higher degree of design flexibility. It also simplifies the design and debugging process by permitting a system designer to erase a single sector only during code modification. This reduces the development cycle and results in shorter time to market.

Appendix A
Comparison Chart Am29F010 and 28F001BX

Features	AMD Am29F010	Intel 28F001BX
Density	128 Kbyte	128 Kbyte
Architecture	Fully Sectored	Block based
Sector/Block size	16 Kbyte	8, 4, 4 & 112 KByte
Automatic Algorithm	Yes	Yes
Power Supply	5.0 V only	5.0/12.0 V
Standby Mode	Yes	Yes
Deep Power Down Mode	No	Yes
Sector Protect	All Sectors	Only Boot Block
Sector Unprotect	Yes	Yes
Write Operation Status	$\overline{\text{Data}}$ Polling, Toggle Bit	Status Register
Chip Erase Time	1 second	10.10 seconds
Chip Program Time	3 seconds	2.39 seconds
Erase Suspend	No	Yes
Power Consumption (Programming)	200 mW	600 – 870 mW
Fastest Speed	45 ns	120 ns
Inadvertent Write Protect	No write for $V_{CC}<V_{LKO}$ 5 ns glitches ignored Read mode during Power up Four/Six bus cycle software command	No write for $V_{PP}<V_{LKO}$ Two bus cycle software command
Package	32-Pin DIP/PLCC/TSOP	32-Pin DIP/PLCC/LCC & TSOP
	Easy upgrade to 4Mbit	No upgrade path
JEDEC Pin Out	Yes	$\overline{\text{PWD}}$ Pin not defined
Endurance	100,000 cycles mininum per sector	10,000 cycles minimum

Appendix B
12.0 V Flash Memory V_{PP} Generation Circuitry



† L1 = SUMIDA CD54-330N (708-956-0666)
*Hilton CSTDD226M016TC (813-371-2600)
**Use LT1109A for 120 mA Output (Consult LTC Factory)

Figure 4

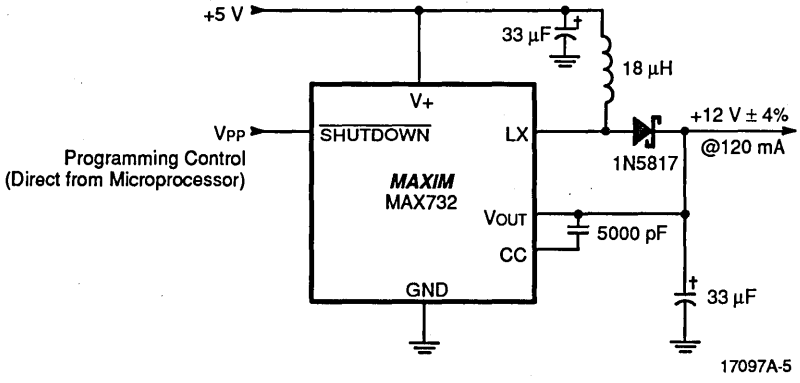


Figure 5

5.0 V-Only Flash Memory Negative Gate Erase Technology

Application Note

Advanced Micro Devices

Advanced Micro Devices' Negative Gate Erase, 5.0 V-only technology is the most cost-effective and reliable approach to single-supply Flash memories. The innovative approach AMD has taken to 5.0 V-only technology provides designed-in reliability that is equal to that of its 12.0 V devices. In fact, transistor oxides are not subjected to any voltages higher than on AMD's 12.0 V devices. This approach minimizes internal power generating requirements which results in a negligible impact on die size because of the 5.0 V-only reprogramming capability.

The minimal power requirement of AMD's Negative Gate Erase, 5.0 V-only technology is made possible by design techniques which use the systems' V_{CC} power supply to provide the 10-20 mA (peak) current for Band-to-Band tunneling. Erase operations are performed when the system V_{CC} voltage is applied to the source terminal and the gate is pumped to a negative voltage. Less than 10 μA of current is required on the gate to enable Fowler-Nordheim tunneling.

Negative Gate Erase uses the same mechanism to erase a cell as the company's 12.0 V devices. Programming operations are performed with positive voltage pumped on the gate terminal at less than 10 μA of current. Hot channel electrons are injected into the floating gate in the same manner as 12.0 V devices.

The 5.0 V-only cell layout and geometry are comparable to the 12.0 V Flash memory cell. This ensures long term scalability equal to conventional 12.0 V flash designs without any penalty in die size. AMD added Dual Layer Metal (DLM) technology to implement its flexible sector erase architecture. AMD's unique sector isolation ensures reliable endurance cycling of at least 100K cycles for each sector whether erased individually or in combination.

AMD's innovative charge pump design techniques allow this device to consume less power than 12.0 V devices during write operations. Approximately 90% charge pump efficiency is achieved with AMD's unique diode V_t cancellation techniques. In addition, the charge pump design minimizes noise and ripple associated with voltage conversion circuits.

The culmination of these innovative design techniques makes this device ideal for power sensitive portable applications.

CHARGE PUMP CHARACTERISTICS—OVERVIEW

Before discussing the details of AMD's 5.0 V-only technology it is helpful to review the basic concepts of charge pump design. These concepts apply to stand alone DC/DC converters as well as charge pumps integrated into the device silicon. All charge pump designs share common characteristics. For instance the available current from a voltage pump is determined by the Z_{out} and V_{out} of the circuit.

- Z_{out} is proportional to n/(C*F)
  - n = # of charge pump stages
  - C = capacitor size of each stage
  - F = clock rate
- V_{out} is proportional to n • (V_{CC} – V_{Diode})
  - n = # of charge pump stages
  - V_{out} = Device V_{CC}
  - V_{Diode} = voltage drop of charge pump blocking diode
- Noise is proportional to L • (di/dt)
  - L = bond wire inductance
  - di/dt = rate of current change

There are a number of issues to note about these relationships.

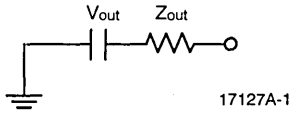
The silicon area of the charge pump is determined by the product of n and C (number of stages times the capacitor size). Efficient use of chip silicon requires this product to be as small as possible.

The efficiency of the voltage generated by the pump circuitry is increased as the effective voltage drop of the charge pump blocking diode is reduced (V_{CC} – V_{Diode}).

The voltage available at the output of the pump (when current is drawn) increases when Z_{out} decreases. Z_{out} decreases as either n is reduced or the product C * F increases. In addition, once a given Z_{out} is determined the values of C and F may vary in inverse proportion while maintaining the same product value.

Noise generated by the charge pump is minimized with a lower F (when n • C is large). But as F decreases C must increase in order to keep the product C*F constant.

Publication# 17127 Rev. A Amendment/0
Issue Date: September 1992



Charge Pump Model

Negative Gate Erase Technology

Negative Gate Erase is used for erase operations in order to minimize the current drawn from the erase charge pump. In order to illustrate the importance of this, it is beneficial to first describe how today's 12.0 V V_{PP} Flash devices operate. Then conventional techniques of generating 12.0 V from a 5.0 V V_{CC} internally will be examined before discussing the benefits of Negative Gate Erase.

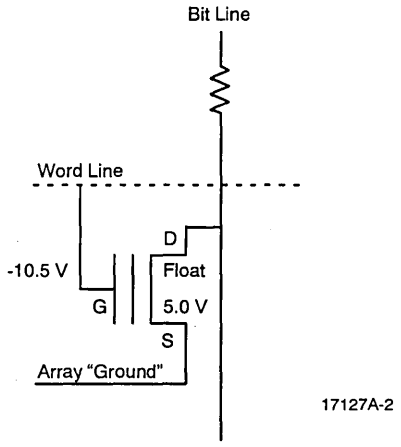
Today's 12.0 V Flash devices erase the memory cell at the Source terminal with 12.0 V applied. The gate is grounded and the drain is left floating. The external Vpp circuit supplies the Vpp current required for erase operations. This provides the 10-20 mA (peak) Band-to-Band tunneling current along with the Fowler-Nordheim tunneling current required to remove charge off the floating gate.

Conventional techniques in generating 12.0 V at the source terminal from a 5.0 V V_{CC} internal supply require huge charge pumps in order to supply the 10-20 mA (peak) of Band-to-Band tunneling current. This approach requires significant silicon real estate (charge pump area = n*C) and consumes large amounts of power [(12.0 V * 30 mA) ÷ Efficiency ≥ 360 mW].

Multiple transistor EEPROM 5.0 V-only technology uses charge pumps to internally raise the gate voltages to between 18 and 20 V at < 10 μA. A multiple transistor approach requires one and a half to twice the silicon real estate as single-transister approaches. Both conventional 12.0 V Flash and AMD's 5.0 V-only technology produce approximately half the electric field on the tunnel oxide as with EEPROM technology. The lower tunnel oxide fields extend the life of the oxide by orders of magnitude. In addition, EEPROM technology implements uniform channel tunneling instead of source-side tunneling as with conventional 12.0 V and AMD's 5.0 V-only technology. Uniform channel tunneling stresses the entire oxide region while source-side tunneling only stresses a small region of the oxide.

AMD's Negative Gate Erase technique actually provides the same electric fields to the Flash memory cell and uses the same erase mechanisms as its 12.0 V Flash devices. Negative Gate Erase is used in order to reduce the current drawn from the erase charge pump. The Band-to-Band tunneling current (10-20 mA peak) comes directly from the system V_{CC} through the Array Ground terminal. This is the most efficient way to use an existing system V_{CC} supply. The current required from the Negative Gate Erase charge pump is less than 10 μA at -10.5 V. This reduces the internal power consumption in relation to conventional 12.0 V approaches.

A circuit diagram of Negative Gate Erase is illustrated below.



Notes:

1. Gate terminal is pumped to -10.5 V @ <10 μA current
2. 10-20 mA (peak) erase current is provided to the Source terminal by the system's V_{CC} supply

Key:

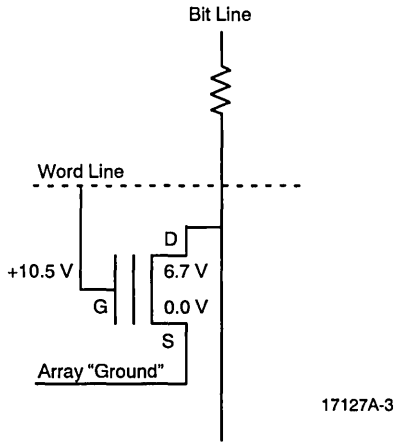
D = Drain terminal
G = Gate terminal
S = Source terminal

5.0 V-Only Negative Gate Erase Circuitry

5.0 V-Only Programming

AMD's 5.0 V-only programming technique provides the same electric fields to the memory cell and uses the same programming mechanisms as its 12.0 V Flash devices. The drain is pumped to 6.7 V from 5.0 V and supplies approximately 0.5 mA of current per cell. The internal power generation required for the Channel Hot Electron injection mechanism is minimized because the charge pump only delivers a 34% voltage increase from the base Vcc supply. This also provides the benefit that the cell's programming characteristics remain constant even if the system Vcc supply varies. This current supplies the Channel Hot Electrons that are injected into the floating gate in order to program the memory cell. The current required by the gate voltage charge pump is less than 10 μA. This minimizes internal power consumption.

A circuit diagram of the programming circuitry is illustrated below.



Notes:

1. Gate terminal is pumped to +10.5 V @ < 10 μA current
2. Drain terminal is pumped to 6.7 V from 5.0 V Vcc supply @ 0.5 mA

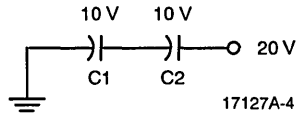
5.0 V-Only Drain Programming

AMD's 5.0 V-ONLY DEVICE EQUALS THE RELIABILITY OF 12.0 V DEVICES

Equivalent Electric Fields Charge Pump Circuitry

One component of device reliability is related to the electric fields applied across internal device transistors. Very high electric fields may cause oxide breakdown and hence reliability problems. One of the main design and reliability requirements in AMD's 5.0 V-only circuit implementation was the maintenance of electric fields across the charge pump oxides equivalent to those of the oxides subject to high voltage in the 12.0 V device. AMD's techniques minimize the electric fields across the oxides to be equivalent to those across the device transistor oxides during standard Read operations of the 12.0 V device. This ensures that the 5.0 V-only design will not be more susceptible to oxide failures than 12.0 V devices. There has never been any physical damage to an oxide from the high voltages internal to AMD's 12.0 V Flash device.

One way to maintain low electric fields across transistor oxides is to stack multiple capacitors together. This circuit technique delivers a large output voltage while maintaining low electric fields across each oxide. As an example, with an oxide that is able to reliably withstand voltages of 10 V, a circuit can be constructed to provide 20 V by stacking (in series) two capacitors with 10 V across each oxide. This circuit ensures that the electric fields remain within the specified limits.



Capacitors Charge Pump Model

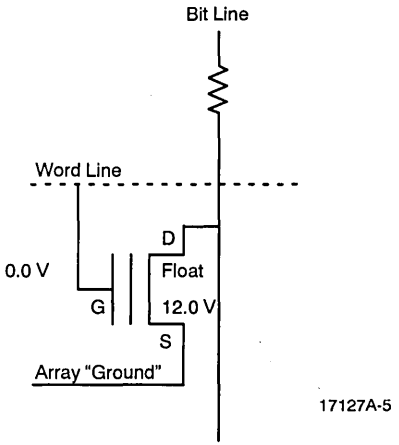
Memory Cell Circuitry

It is important to note that the electric fields applied to the data storage memory cells of the 5.0 V-only device are the same as that of the 12.0 V device. This ensures that the 5.0 V-only design will not be more susceptible to oxide failures than 12.0 V devices. An observable measure that the electric fields are indeed the same is found in the erase time parameter. Erase time depends upon the electric field across the floating gate and the thickness of the tunnel oxide (Tox). Tox and the erase time of the 5.0 V-only device are the same as in the 12.0 V device. Therefore the electric field is the same in both devices.

The electric fields of the 5.0 V circuit are also demonstrated by analyzing the coupling ratios in the memory cell transistor. However, it is first beneficial to discuss the coupling ratios of standard 12.0 V Flash circuitry. We will use the erase circuit as an example. The same concepts apply to the programming circuitry.

Electric Fields in Standard 12.0 V V_{PP} Erase Circuits

The standard Flash memory cell applies 12.0 V to the Source terminal. The Gate terminal is grounded and the drain is left floating. The actual electric field seen by the tunnel oxide is a superposition of three components. One is because the field generated by the trapped electrons on the floating gate. This is the state of a programmed memory cell prior to erase. The other two result from coupling of the voltage between the word line (Gate terminal)/floating gate and between the source terminal/ floating gate. In the case of standard 12.0 V Vpp programming, the only component from the voltage coupling is between the source terminal and the floating gate. There is no coupling from the word line because it is at a zero voltage potential. The resulting electric field never exceeds a peak value of 10 mV/cm.



Notes:

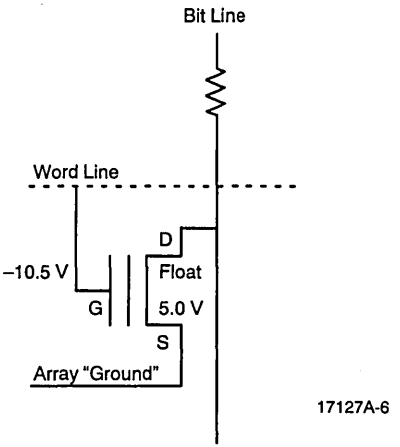
1. Tunnel oxide (Tox) electric field is determined by superposition.
   - Floating Gate Voltage from stored electrons reduces voltage across Tox
   - Source Coupling Voltage on the floating gate reduces the voltage across the Tox
2. Total electric field across Tox due to superposition is <10 mV/cm.

Standard 12.0 V V_{PP} Erase

Equivalent Electric Fields in AMD's 5.0 V-Only Negative Gate Erase Ciruitry

AMD's Negative Gate Erase circuitry applies the same electric fields to the memory cell as the 12.0 V device. The Gate terminal is negatively pumped to –10.5 V and the source terminal is at 5.0 V supplied by the system Vcc supply. The drain terminal is left floating. The actual electric field seen by the tunnel oxide is a superposition of three components. One is due to the field generated by the trapped electrons on the floating gate. This is the state of a programmed memory cell prior to erase. The other two result from coupling of the voltage between the word line (Gate terminal)/ floating gate and between the source terminal/ floating gate. This time there is voltage coupling from both the Source terminal and word line. The resulting electric field is the same as in the 12.0 V device. The electric field is always ≤ 10 mV/cm.

In addition, the Negative Gate Erase approach actually produces a lower electric field across the cell junctions. This is because the source terminal is subjected to 5.0 V levels instead of 12.0 V.



Notes:

1. Tunnel oxide Tox electric fields determined by superposition.
   - Floating Gate Voltage from stored electrons reduces the voltage across the Tox
   - Gate Coupling Voltage on the floating gate reduces the voltage across the Tox
   - Source Coupling Voltage on the floating gate reduces the voltage across the Tox
2. Total electric field across the Tox due to superposition is < 10 mV/cm.

5.0 V-Only Negative Gate Erase

DATA INTEGRITY

Ruggedized Programmability

AMD's 5.0 V-only approach is designed not to be sensitive to variations in the system Vcc supply during programming operations.

This is achieved by pumping the drain terminal to 6.7 V. The device actually compensates for any system level variations in the Vcc supply. During programming the word line is pumped to +10.5 V and the source terminal is grounded. These voltage conditions and resulting electric field are the same as in 12.0 V devices.

Sector Write Protection

AMD implements a Dual Layer Metal (DLM) bussing technique in order to provide the most cost-effective and reliable method to individually isolate sectors during sector erase operations. This technique inhibits the presence of high voltage in non-addressed sectors from disturbing fixed data. Data in non-addressed sectors is isolated from all other sector program and erase operations.

Minimizing Charge Pump Noise and Voltage Ripple

Minimizing Noise

AMD's charge pump circuitry minimizes noise with a multi-stage pump design. Each stage has the same clock rate but is out of phase with all other stages. The phase shifting minimizes potential noise from any of the individual pumps. This technique delivers a very smooth and constant source of power. A V-8 automobile engine serves as an excellent analogy. Each of the eight stages of the charge pump is 45° out of phase. Each packet of charge is delivered in a way to provide a smooth flow of current.

SECTION

2 12 V, BULK ERASE FLASH MEMORIES

FINAL

Am28F256

32,768 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 70 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **10,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ Programming**
  - 10 µs typical byte-program
  - 0.5 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F256 is a 256K Flash electrically erasable, electrically programmable read only memory organized as 32K bytes of 8 bits each. The Am28F256 is packaged in 32-Pin PDIP, PLCC, and TSOP versions which allow for upgrades to the 2 Megabit density. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F256 offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F256 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F256 uses a command register to manage this functionality, while maintaining a standard 32-Pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F256 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1 V to Vcc+1 V.

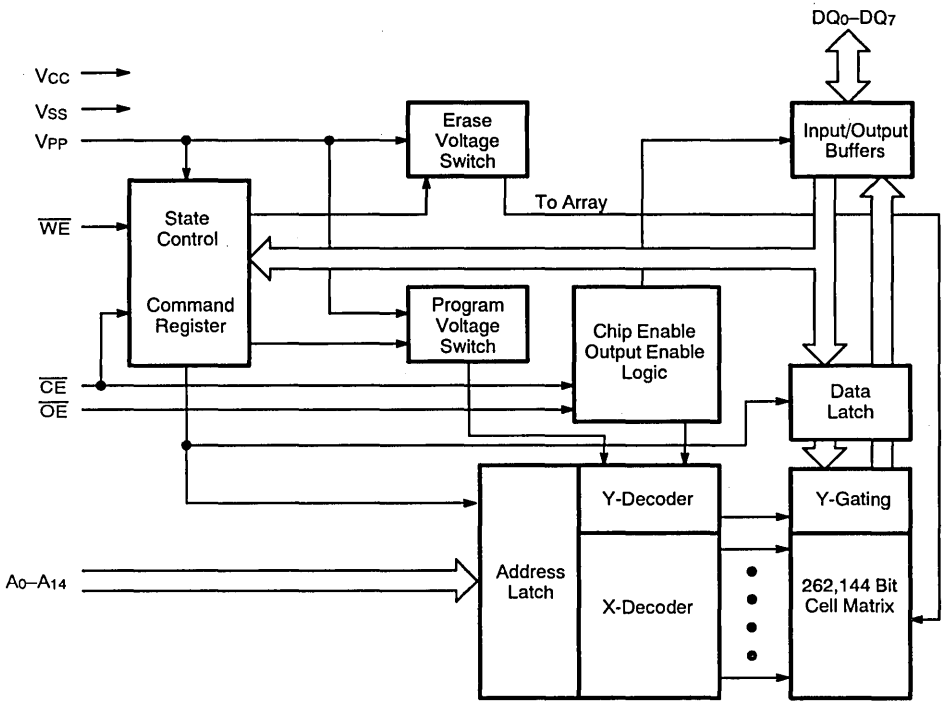
The Am28F256 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F256 is one half a second. The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F256 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F256 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 11560 Rev. D Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



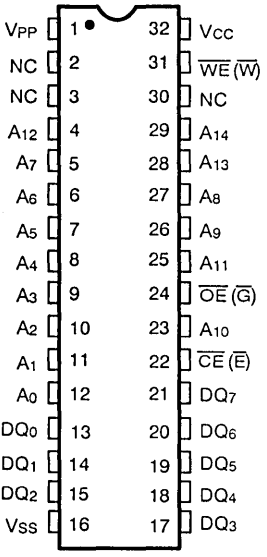
11561-001B

PRODUCT SELECTOR GUIDE

Family Part No.	Am28F256				
Ordering part No:					
± 10% Vcc Tolerance	—	**–90**	**–120**	**–150**	**–200**
± 5% Vcc Tolerance	**–75**	**–95**	—	—	—
Max Access Time (ns)	70	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	35	50	55	55

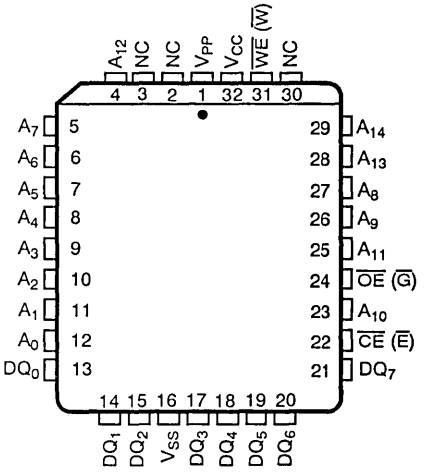
CONNECTION DIAGRAMS

DIP



11560-002A

PLCC*

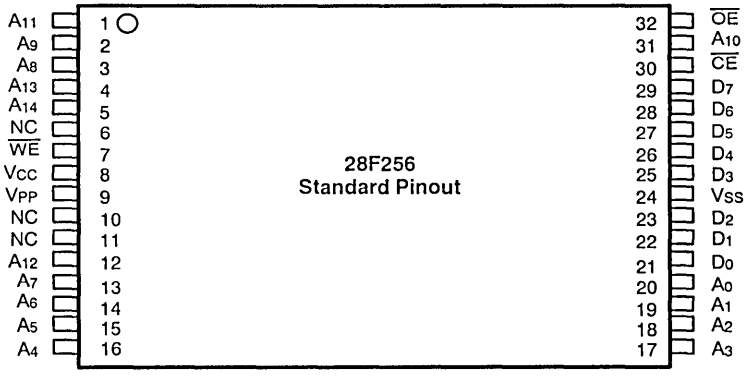


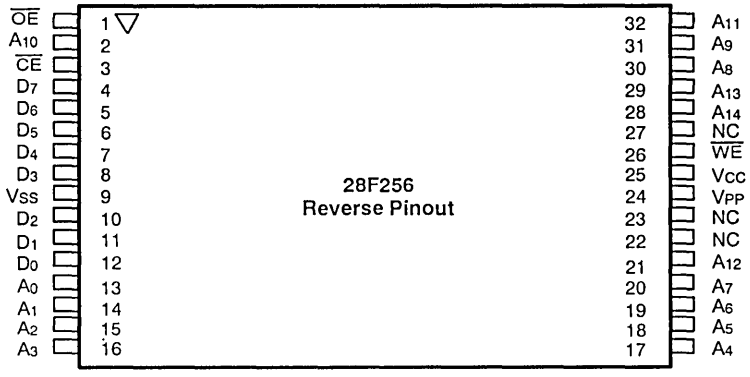
11560D-003B

Note: Pin 1 is marked for orientation.

*Also available in LCC.

TSOP PACKAGES

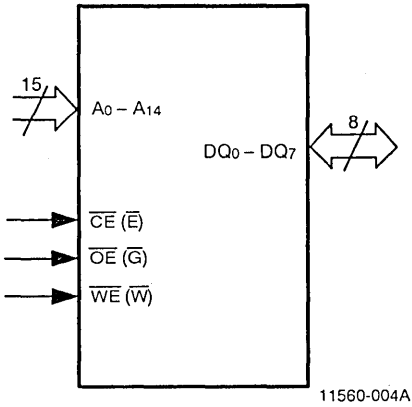




11560D-014A

28F256 32K x 8 Flash Memory in 32 Lead TSOP

LOGIC SYMBOL

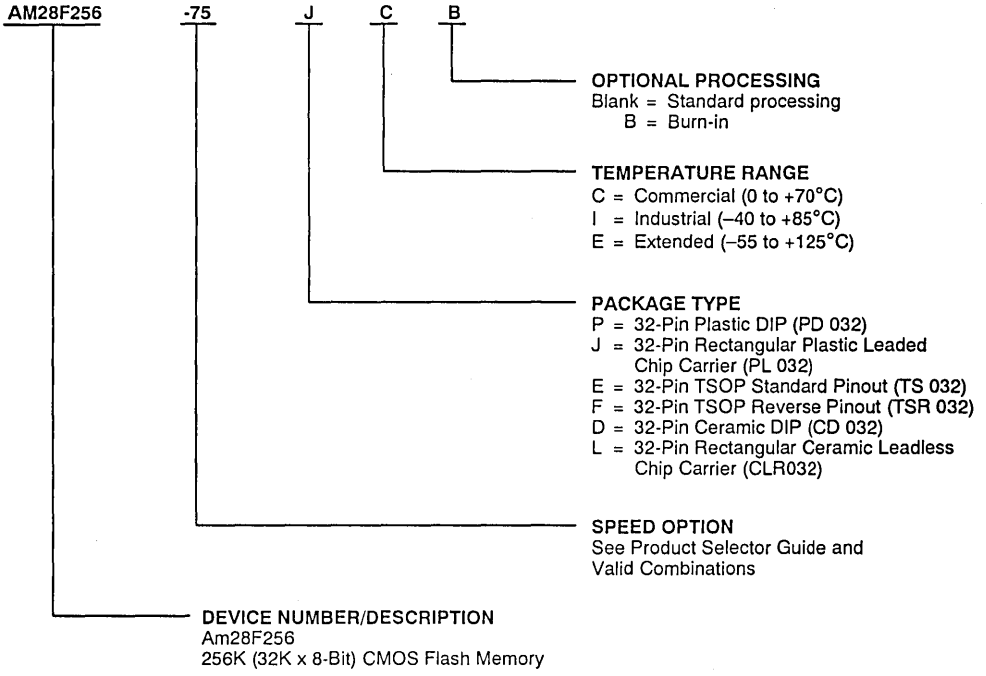


11560-004A

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F256-75	PC, JC, EC, FC, PCB, JCB, ECB, FCB, DC, LC, DCB, LCB
AM28F256-90 AM28F256-95 AM28F256-120 AM28F256-150 AM28F256-200	PC, PI, JC, JI, PCB, PIB, JCB, JIB, PE, PEB, JE, JEB, EC, FC, EI, FI, EE, FE, ECB, FCB, EIB, FIB, EEB, FEB, DC, DI, DE, DCB, DIB, DEB, LC, LI, LE, LCB, LIB, LEB

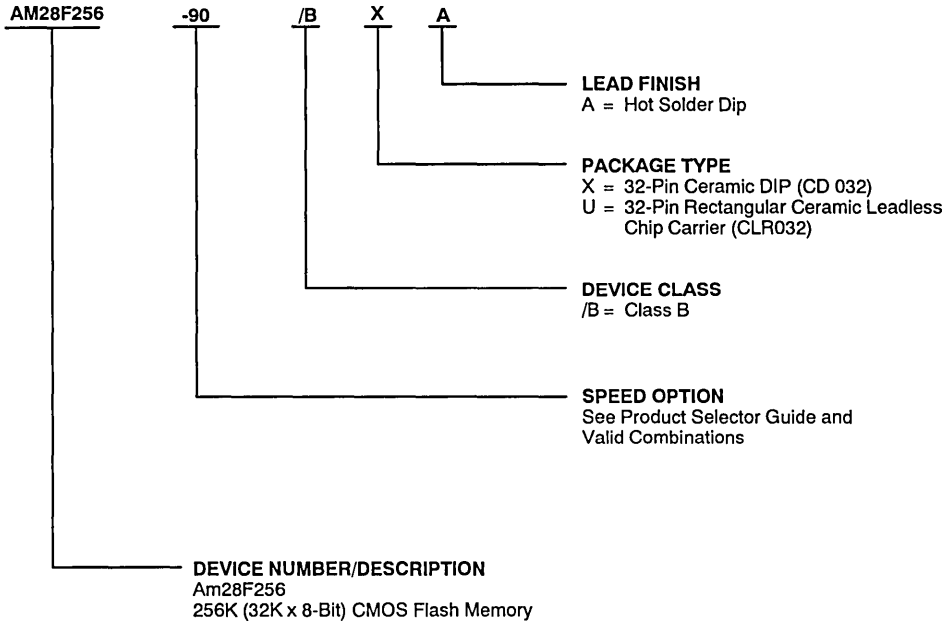
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F256-90 AM28F256-120 AM28F256-150 AM28F256-200	/BXA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

V_{PP}

Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{CC}

Power supply for device operation. (5.0 V ± 5% or 10%)

V_{SS}

Ground

NC

No Connect-corresponding pin is not connected internally to the die.

$A_0 - A_{14}$

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$DQ_0 - DQ_7$

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high deselects the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)

The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F256 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F256 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F256's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F256 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Flasherase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Erase Set-Up:** Write the Set-Up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-Up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-Verify command.
3. **Erase-Verify:** Write the Erase-Verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-Verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-Verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Program Set-Up:** Write the Set-Up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 μs) prior to issuing the Program-Verify command.
3. **Program-Verify:** Write the Program-Verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Data Protection

The Am28F256 is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F256 powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F256 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A1H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An <V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or ≤ V_{CC} +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. 11.5 ≤ V_{ID} ≤ 13.0 V
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V

Command Register Inactive

Read

The Am28F256 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F256 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F256 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming in a Prom Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F256 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F256 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A1	1	0	1	0	0	0	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits R_7 – R_0 correspond to the data inputs DQ_7 – DQ_0 (Refer to Table 3). Register bits R_7 – R_5 store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6 µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (Read Mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands (Notes 1, 2)	X	X	X	X	X	X	X	X

Notes:

1. See Table 4 Am28F256 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F256 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 6, 7)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A1H
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 7)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6 μs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
7. Please reference Reset Command section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-Up is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Erase Set-Up operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-Verify) to the register.

This two step sequence of the Set-Up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:

The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-Verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-Verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-Verify operation, the Am28F256 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-Verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Erase Set-Up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program Set-Up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:

The Erase-Verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10 ms) as specified in AMD's Flasherase algorithm. Should a system interrupt occur during an erase operation, always write the Erase-Verify command prior to executing an interrupt sequence.

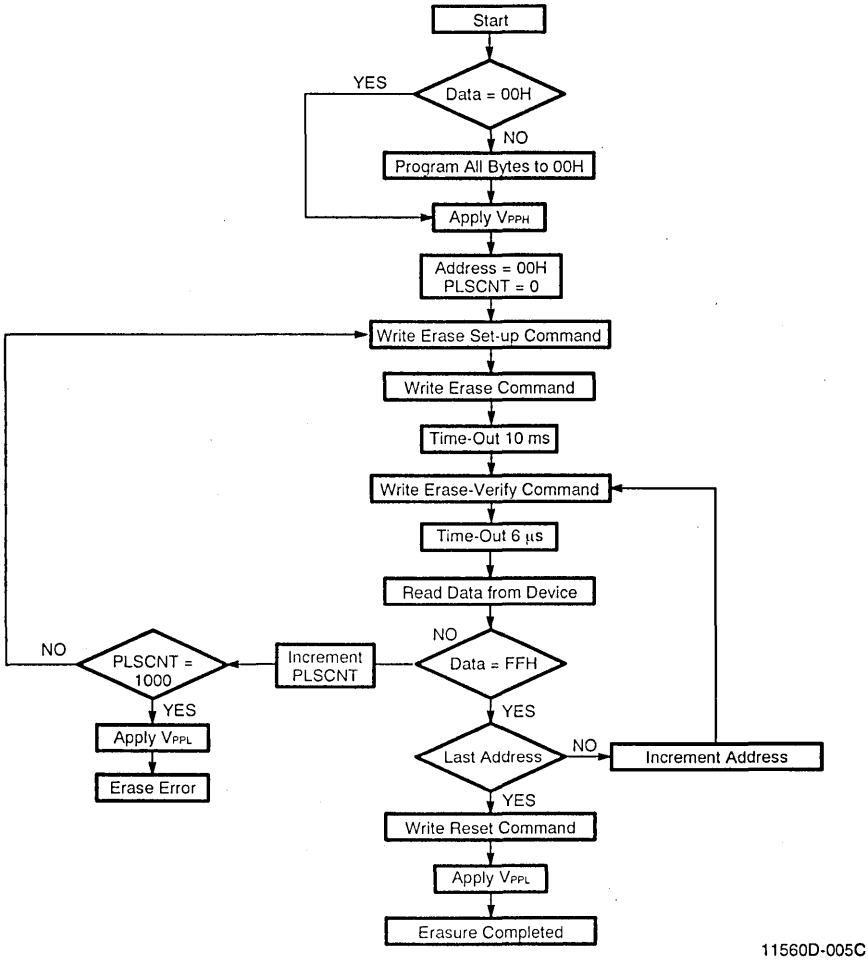


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F256 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

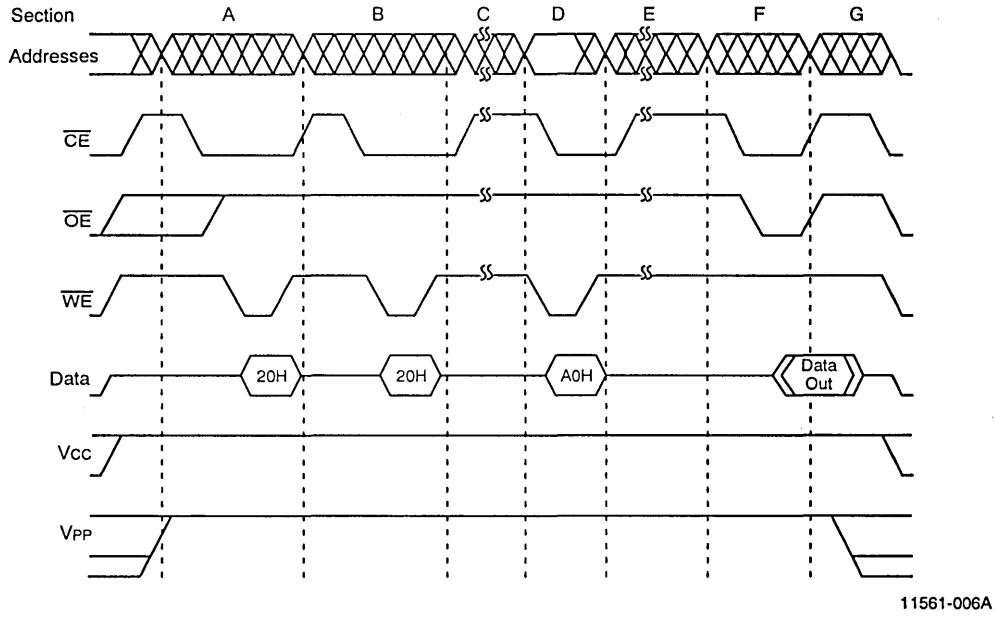
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 3) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-Out	Write	Time-Out	Read	Standby
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-Up Erase	Erase	Erase (10 ms)	Erase-Verify	Transition (6 μs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. AC Waveforms For Erase Operations

Analysis of Erase Timing Waveform

Note:

This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Erase Set-Up/Erase

This analysis illustrates the use of two-cycle erase commands (sections A and B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-Out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Erase-Verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-Verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-Verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-Verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 μs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-Verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified

or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Notes:

1. *All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.*
2. *The Erase-Verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the Erase-Verify command prior to executing an interrupt sequence.*

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The Am28F256 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-Up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-Up Program operation is performed by writing 40H to the command register.

Program

Only after the Program Set-Up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-Verify command to terminate the programming operation. This two step sequence of the Set-Up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-Verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-Verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-Verify operation, the Am28F256 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-Up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F256 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 μs programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

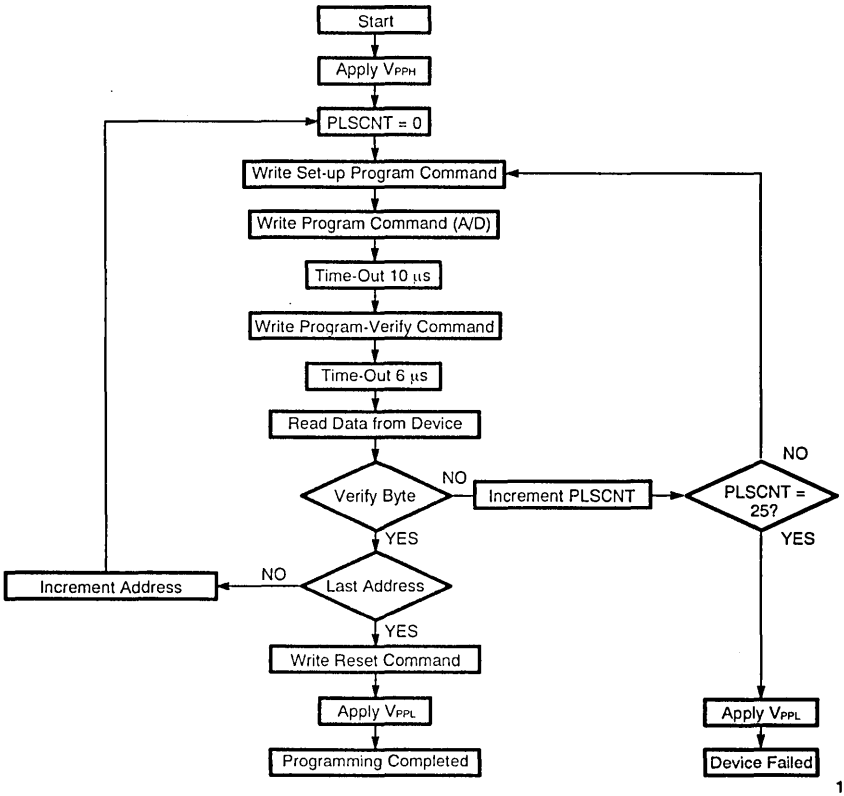


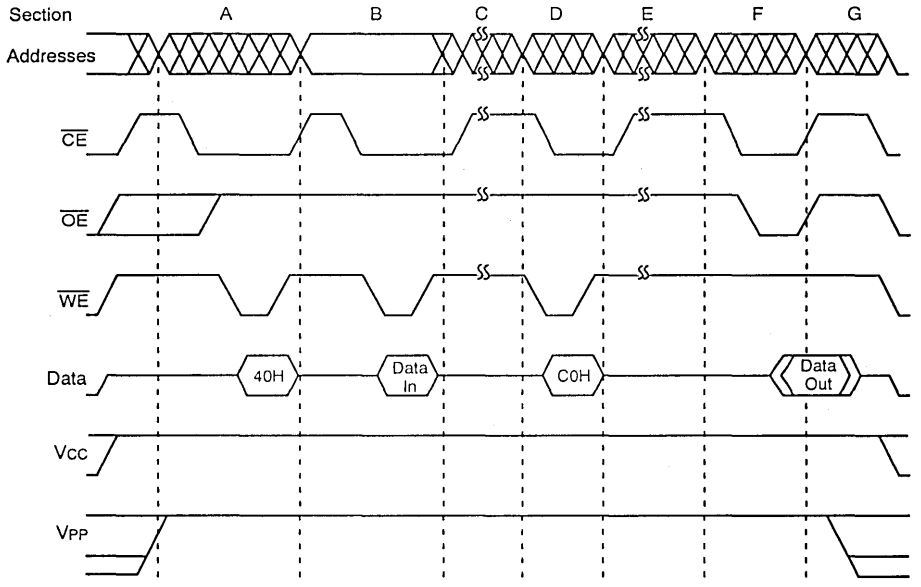
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



11561-008A

	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-Out	Write	Time-Out	Read	Standby
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-Up Program	Program Command Latch Address & Data	Program (10 μs)	Program Verify	Transition (6 μs)	Program Verification	Proceed per Programming Algorithm

Figure 4. AC Waveforms for Programming Operations

Analysis of Program Timing Waveforms

Program Set-Up/Program

Two-cycle write commands are required for program operations (sections A and B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-Out

A software timing routine (10 μs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Program-Verify

Upon completion of the program timing routine, the microprocessor must write the Program-Verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The Program-Verify command also stages the device for data verification (section F). Another software timing routine (6 μs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:
The Program-Verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the Program-Verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1 µF/device. V_{PP} must reach its final value 100 ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-Verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

V_{CC} Prior to V_{PP}

The Am28F256 powers-up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} Prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the Set-Up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The Set-Up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the Set-Up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-System

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F256 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code A1H (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... −65°C to +150°C
Plastic Packages ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to +125°C

Voltage with Respect To Ground
All pins except A_9 and V_{PP} (Note 1) ... −2.0 V to 7.0 V
V_{CC} (Note 1) ..... −2.0 V to 7.0 V
A_9 (Note 2) ..... −2.0 V to 14.0 V
V_{PP} (Note 2) ..... −2.0 V to 14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on A_9 and V_{PP} pins is −0.5 V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) ..... −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) ..... −55°C to +125°C

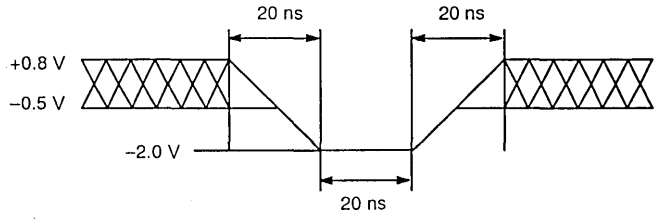
V_{CC} Supply Voltages
V_{CC} for Am28F256–X5 ..... +4.75 V to +5.25 V
V_{CC} for Am28F256–XX0 ..... +4.50 V to +5.50 V

V_{PP} Supply Voltages
Read ..... −0.5 V to +12.6 V
Program, Erase, and Verify ... +11.4 V to +12.6 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

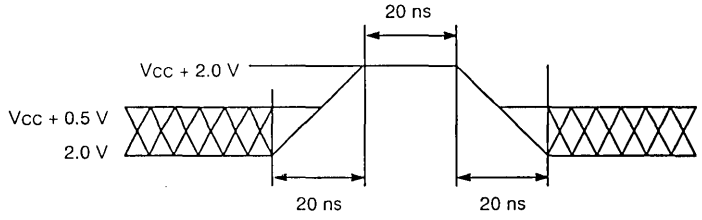
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



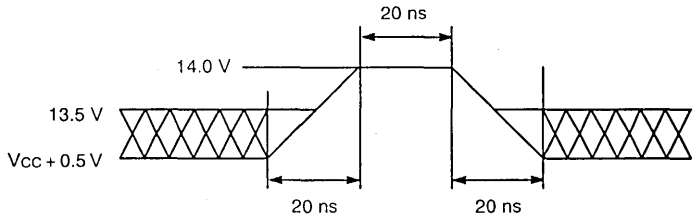
11561D-009B

Maximum Positive Input Overshoot



11561D-010B

Maximum V_{PP} Overshoot



11561D-011B

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max. V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max. V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
		V_{PP} = V_{PPL}			±1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4			V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V

Notes:

1. **Caution:** the Am28F256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

DC CHARACTERISTICS-CMOS COMPATIBLE

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max. V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max. V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4			
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V

Notes:

1. **Caution:** the Am28F256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

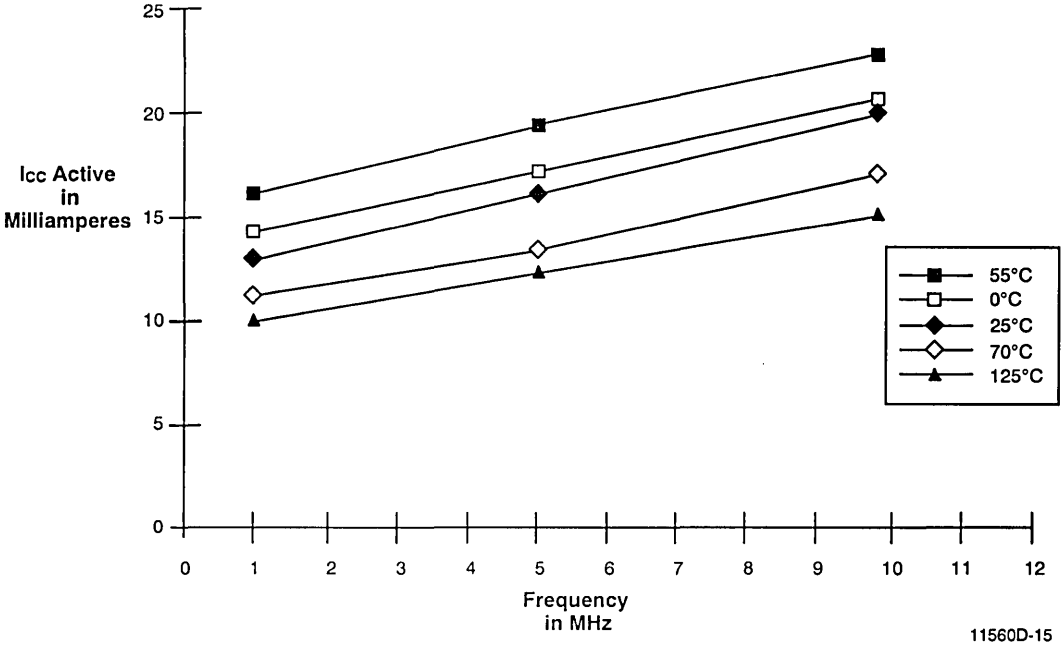


Figure 5. Am28F256 – Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
AC CHARACTERISTICS-Read Only Operation (Notes 1 and 2)

PRELIMINARY

Parameter Symbols				Am28F256					
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min. Max.	70	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	70	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	70	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	35	50	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min. Max.	20	20	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min. Max.	20	20	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min. Max.	50	50	50	50	50	µs

Notes:

1. Output Load:
   1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 to 2.4 V,
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F256-75 and Am28F256-95 Output Load:
   1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. Guaranteed by design not tested.
4. Not 100% tested.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 4)

PRELIMINARY

Parameter Symbols				Am28F256					Unit
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 5)	Min. Max.	70	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	45	50	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp (Note 5)	Min. Max.	100	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 5)	Min. Max.	100	100	100	100	100	ns
t_{VCS}		Vcc Set-Up Time to Chip Enable Low (Note 5)	Min. Max.	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 5)	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 5)	Min. Max.	500	500	500	500	500	ns

Notes:

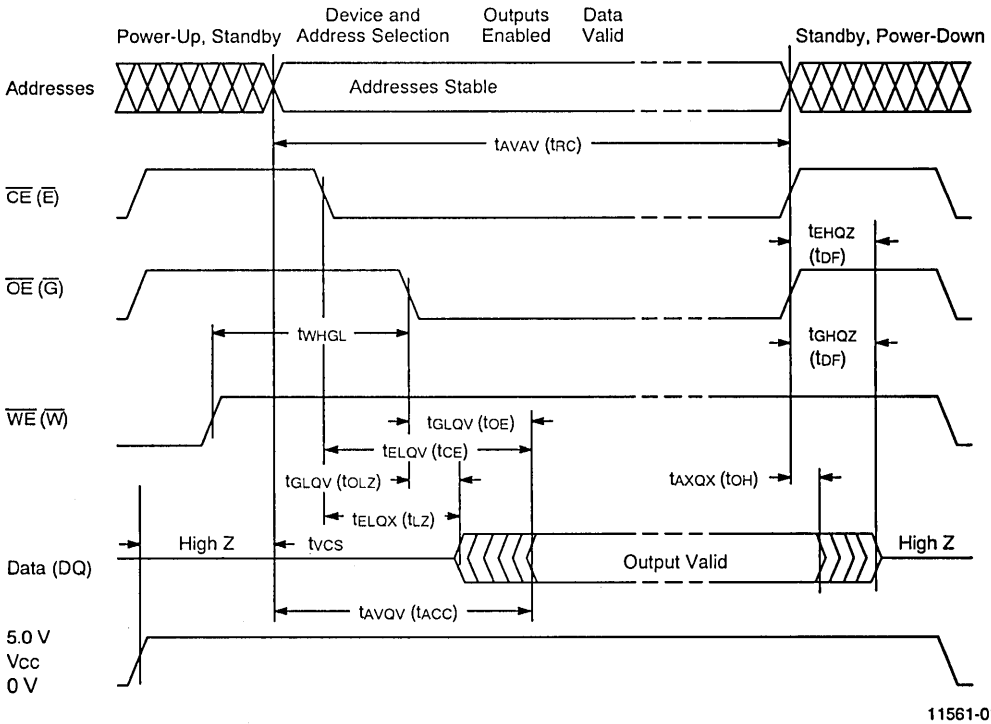
1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F256-75 and Am28F256-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F256-75 and Am28F256-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V
5. Not 100% tested.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



11561-013B

Figure 6. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

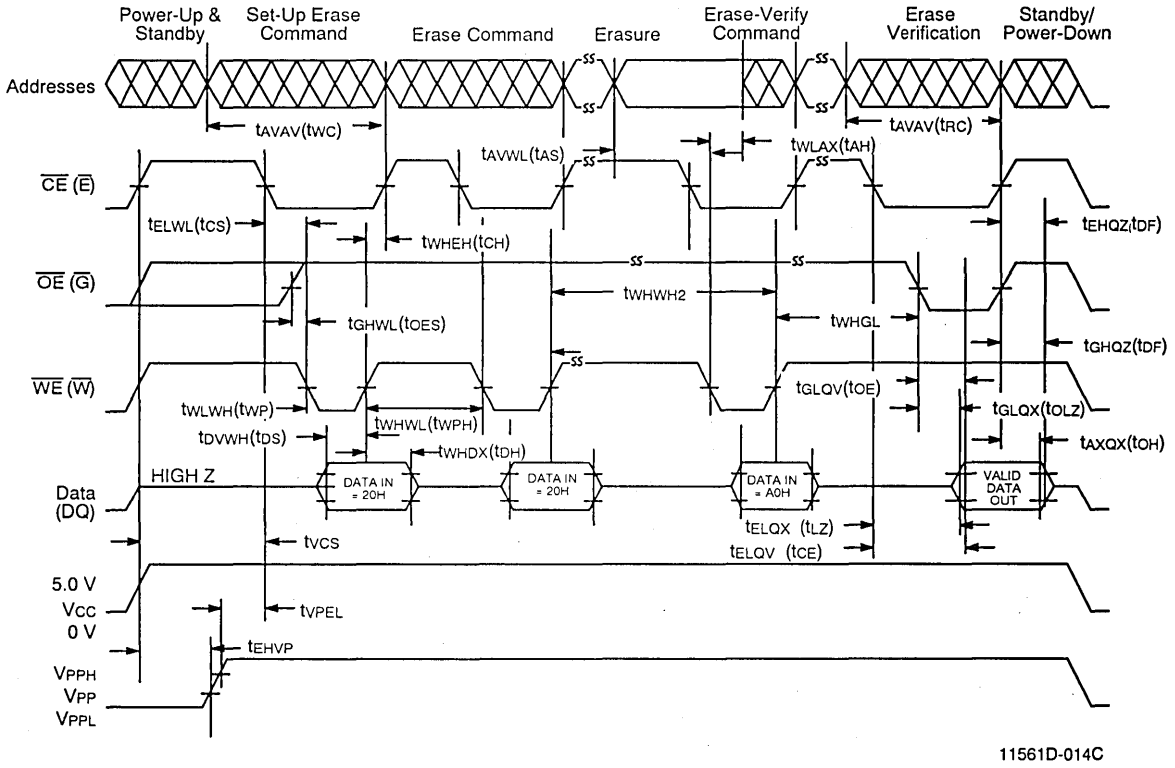


Figure 7. AC Waveforms for Erase Operations

SWITCHING WAVEFORMS

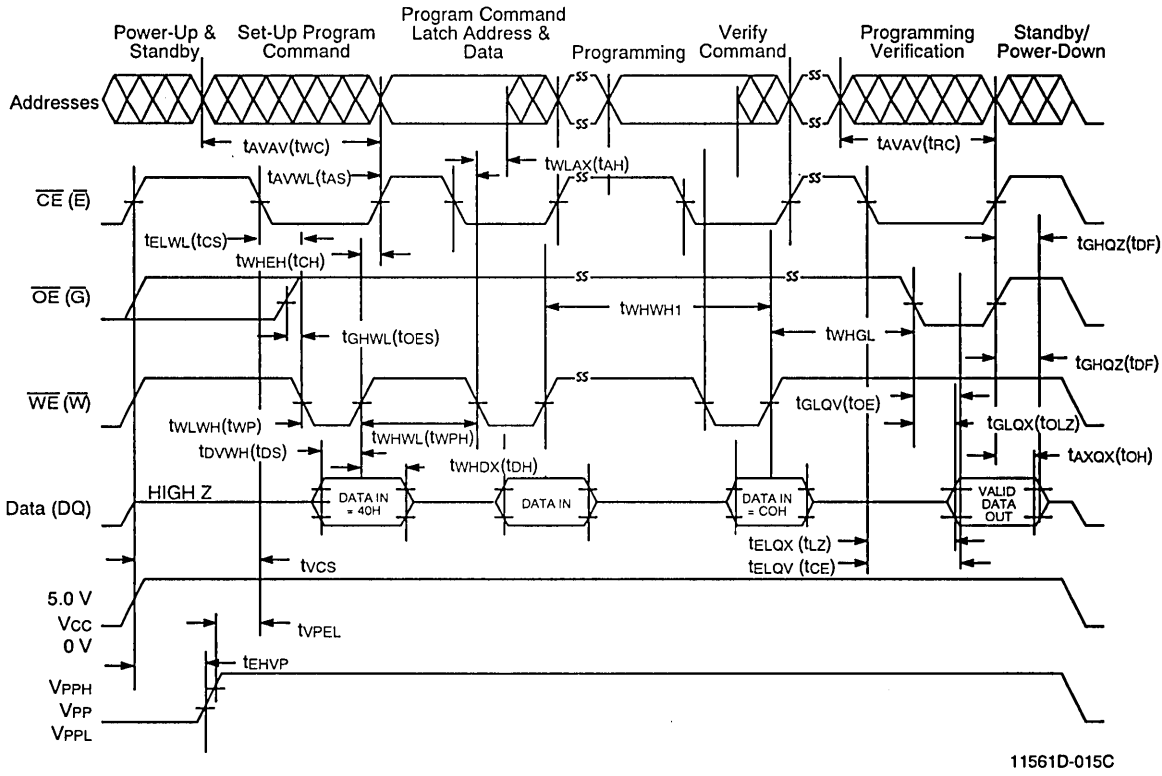
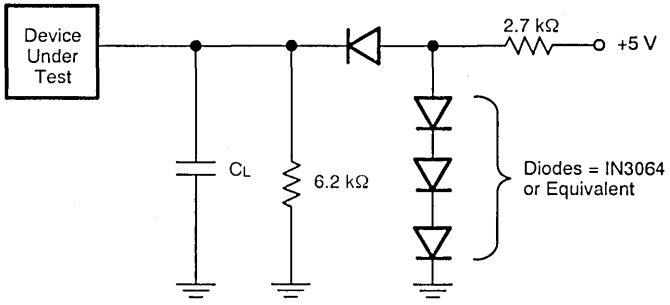


Figure 8. AC Waveforms for Programming Operations

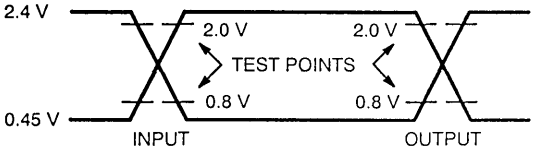
SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance

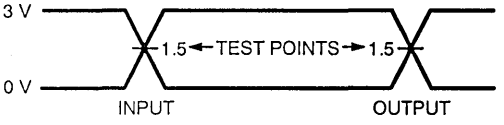
11561-012A

SWITCHING TEST WAVEFORMS



All Devices Except Am28F256-75 and Am28F256-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F256-75 and Am28F256-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

11561D-013A

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max. (Note 2)		
Chip Erase Time		1 (Note 1)	10	S	Excludes 00H programming prior to erasure
Chip Programming Time		0.5 (Note 1)	3	S	Excludes system-level overhead
Write/Erase Cycles	10,000			Cycles	

Notes:

1. 25°C, 12 V V_{PP}.
2. Maximum time specified is lower than worst case. Worst case is derived from the Flasherase/Flashrite pulse count (Flasherase = 1000 max and Flashrite = 25 max). Typical worst case for program and erase operations is significantly less than the actual device limit.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Min.	Units	Test Conditions
Min. Pattern Data Retention Time	10	Years	150°C
	20	Years	125°C

FINAL

Am28F512

65,536 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 70 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 μA maximum standby current
  - No data retention power
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **10,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ Programming**
  - 10 μs typical byte-program
  - 1 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F512 is a 512K Flash electrically erasable, electrically programmable read only memory organized as 64K bytes of 8 bits each. The Am28F512 is packaged in 32-pin PDIP, PLCC, and TSOP versions which allow for upgrades to the 2 Megabit density. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F512 offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F512 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F512 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F512 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1 V to Vcc +1 V.

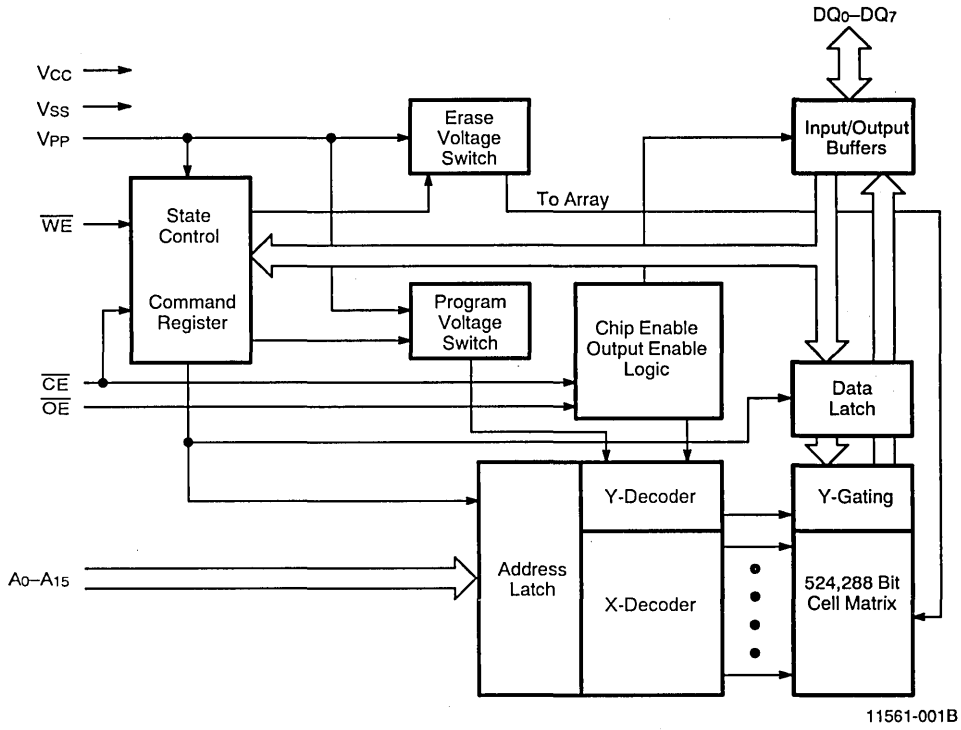
The Am28F512 is byte programmable using 10 μs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F512 is one second. The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F512 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 11561 Rev. D Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM

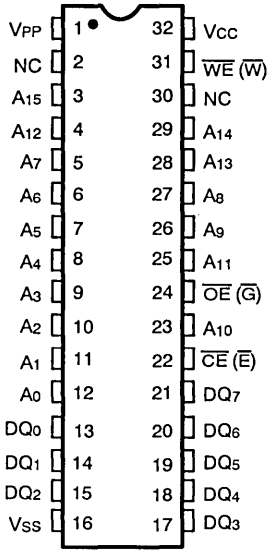


PRODUCT SELECTOR GUIDE

Family Part No.	Am28F512				
Ordering part No:					
± 10% V_{CC} Tolerance	—	-90	-120	-150	-200
± 5% V_{CC} Tolerance	-75	-95	—	—	—
Max Access Time (ns)	70	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	35	50	55	55

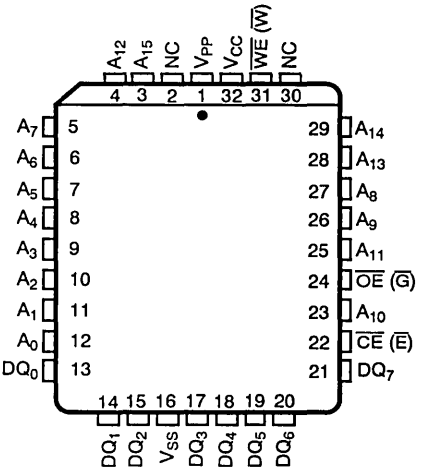
CONNECTION DIAGRAMS

DIP



11561-002B

PLCC*

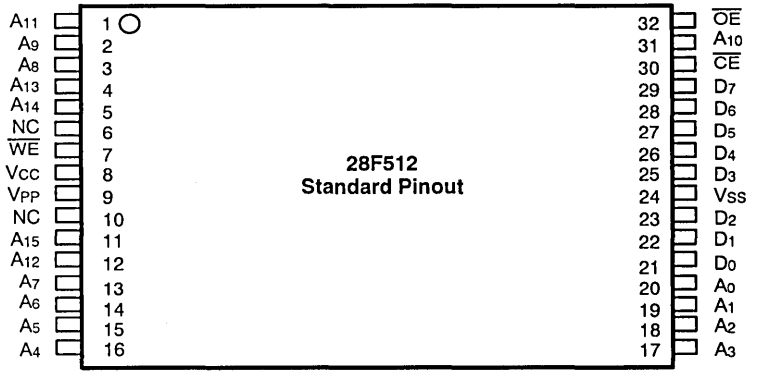


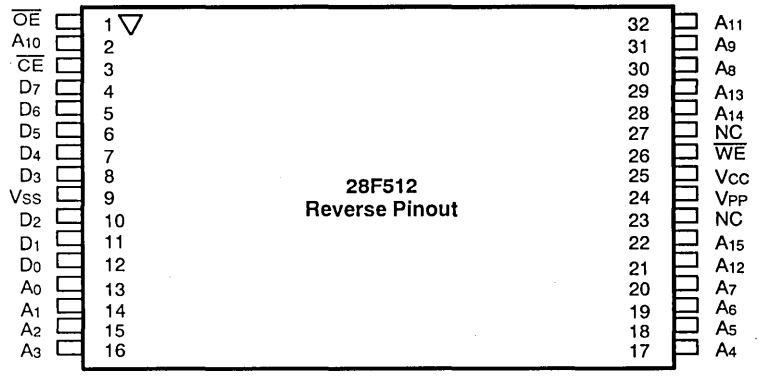
11561D-003C

Note: Pin 1 is marked for orientation.

*Also available in LCC.

TSOP PACKAGES

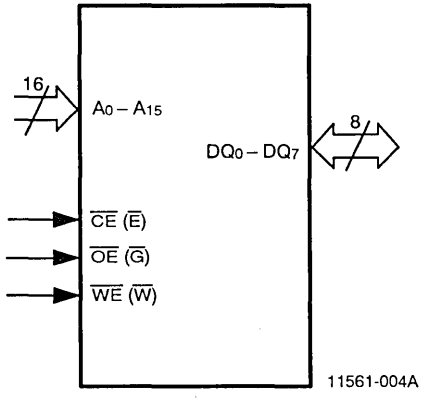




11561D-014A

28F512 64K x 8 Flash Memory in 32 Lead TSOP

LOGIC SYMBOL

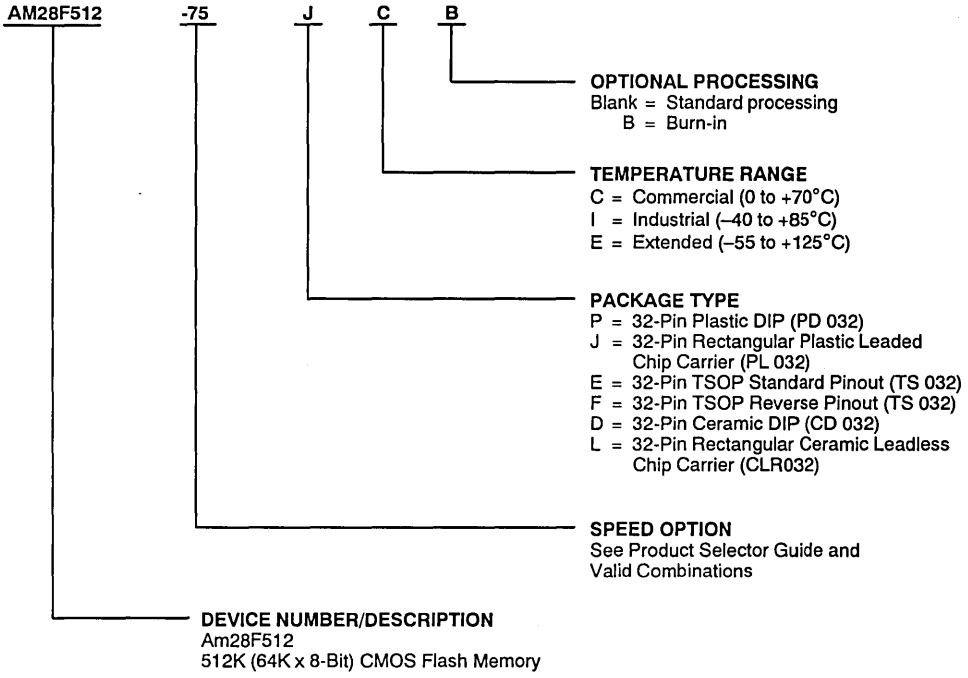


11561-004A

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F512-75	PC, JC, EC, FC, PCB, JCB, ECB, FCB, DC, LC, DCB, LCB
Am28F512-90 Am28F512-95 Am28F512-120 Am28F512-150 Am28F512-200	PC, PI, JC, JI, PCB, PIB, JCB, JIB, PE, PEB, JE, JEB, EC, FC, EI, FI, EE, FE, ECB, FCB, EIB, FIB, EEB, FEB, DC, DI, DE, DCB, DIB, DEB, LC, LI, LE, LCB, LIB, LEB

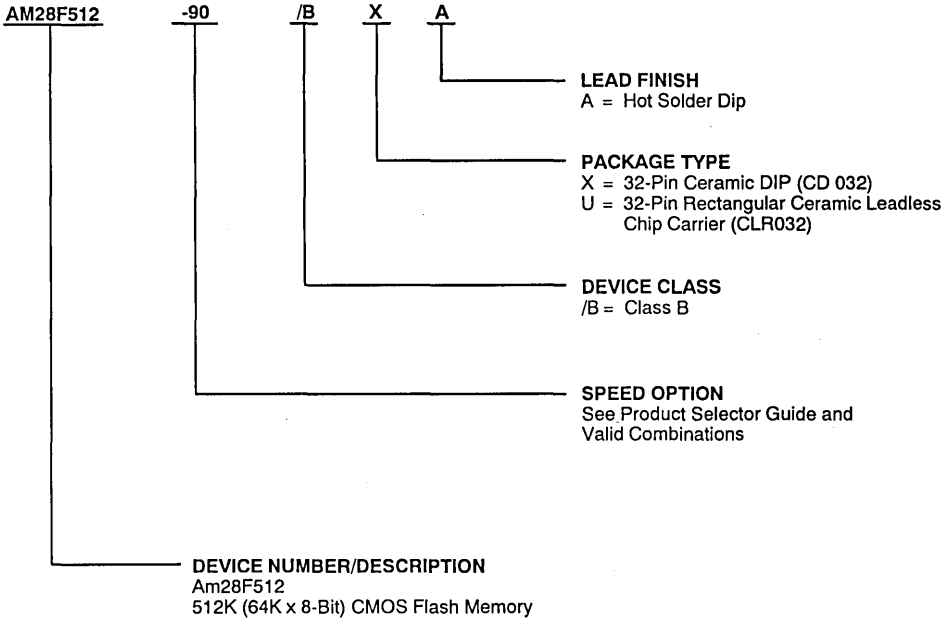
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F512-90 AM28F512-120 AM28F512-150 AM28F512-200	/BXA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{SS}
Ground

NC
No Connect-corresponding pin is not connected internally to the die.

$A_0 - A_{15}$
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$DQ_0 - DQ_7$
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F512 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F512 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F512's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Flasherase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Erase Set-Up:** Write the Set-Up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-Up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-Verify command.
3. **Erase-Verify:** Write the Erase-Verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-Verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-Verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Program Set-Up:** Write the Set-Up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 μs) prior to issuing the Program-Verify command.
3. **Program-Verify:** Write the Program-Verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Data Protection

The Am28F512 is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F512 powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F512 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (25H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An <V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0$ V
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F512 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F512 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F512 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A Prom Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F512 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F512 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	25	0	0	1	0	0	1	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%
Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits $R_7 - R_0$ correspond to the data inputs $DQ_7 - DQ_0$ (Refer to Table 3). Register bits $R_7 - R_5$ store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6 µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (Read Mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands (see Notes)	X	X	X	X	X	X	X	X

Notes:

1. See Table 4 Am28F512 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F512 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 6, 7)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/25H
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 7)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6 μs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
7. Please reference Reset Command section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Flasherase and Flashrite Algorithms
Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-Up is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Erase Set-Up operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-Verify) to the register.

This two step sequence of the Set-Up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:

The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-Verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-Verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-Verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-Verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Erase Set-Up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program Set-Up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:

The Erase-Verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10 ms) as specified in AMD's Flasherase algorithm. Should a system interrupt occur during an erase operation, always write the Erase-Verify command prior to executing an interrupt sequence.

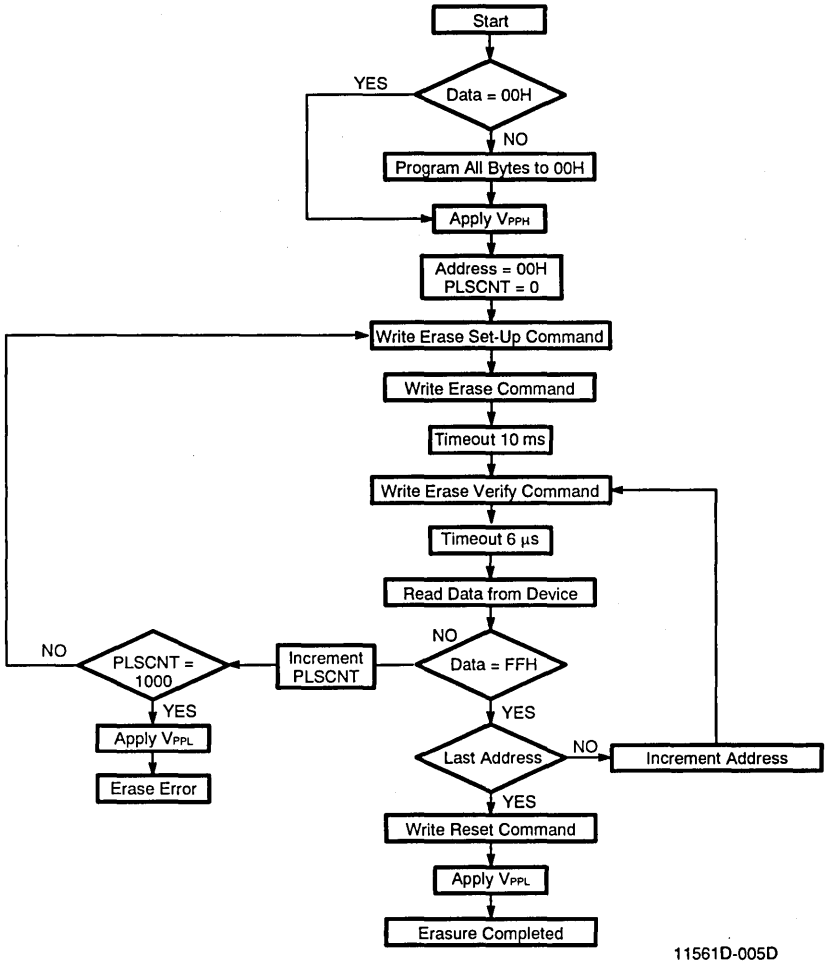


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F512 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

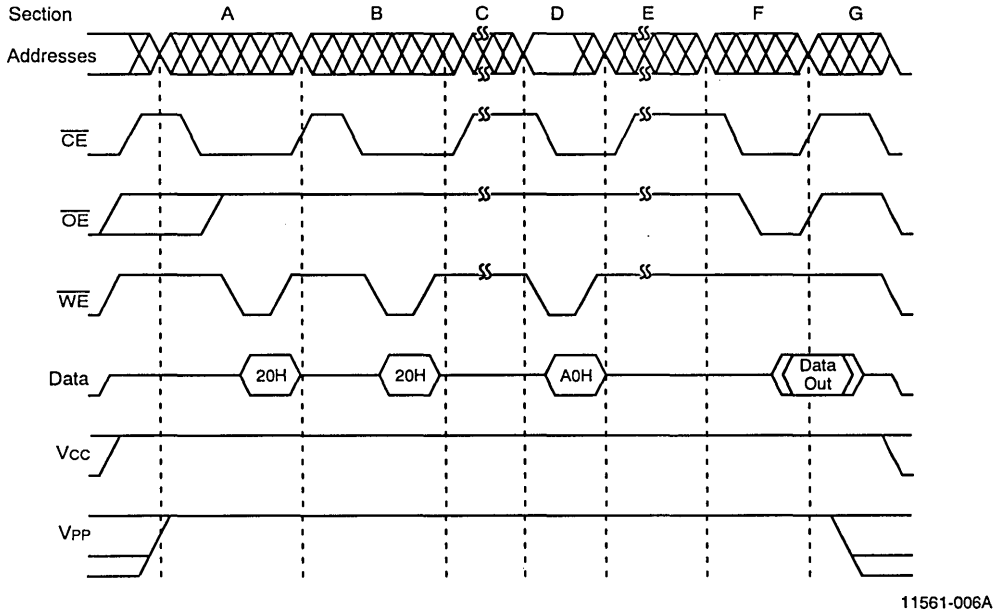
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 3) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Timeout	Write	Timeout	Read	Standby
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-Up Erase	Erase	Erase (10 ms)	Erase-Verify	Transition (6 µs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. AC Waveforms For Erase Operations

Analysis of Erase Timing Waveform

Note:

This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Erase Set-Up/Erase

This analysis illustrates the use of two-cycle erase commands (sections A and B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-Out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Erase-Verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-Verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-Verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-Verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-Verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location

fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Notes:

1. *All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.*
2. *The Erase Verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the Erase-Verify command prior to executing an interrupt sequence.*

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The Am28F512 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-Up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the Program Set-Up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-Verify command to terminate the programming operation. This two step sequence of the Set-Up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-Verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-Verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-Verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-Up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F512 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

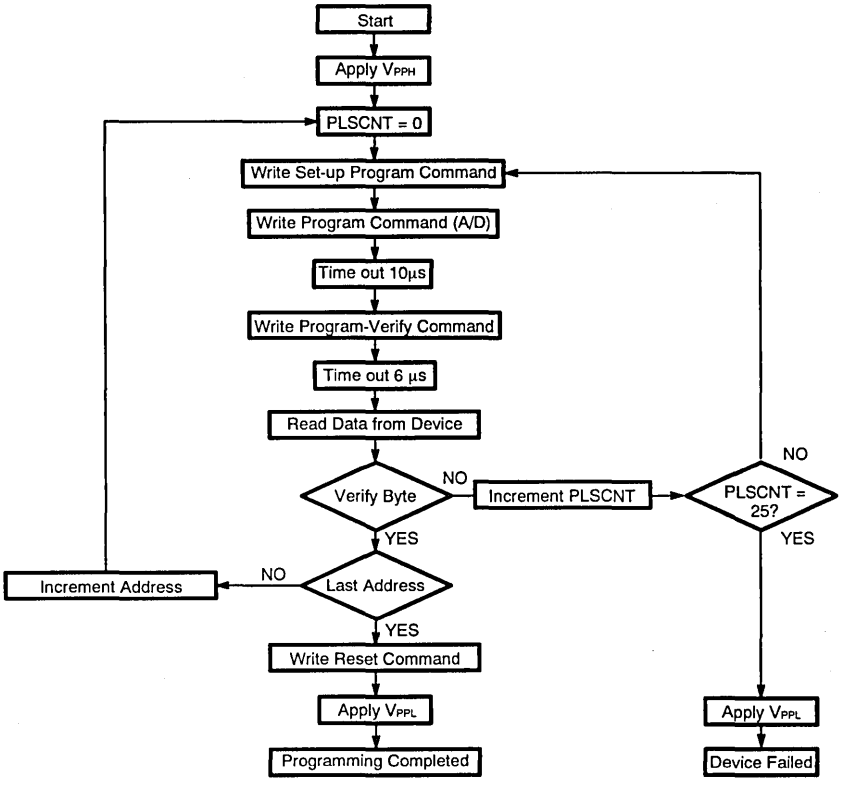


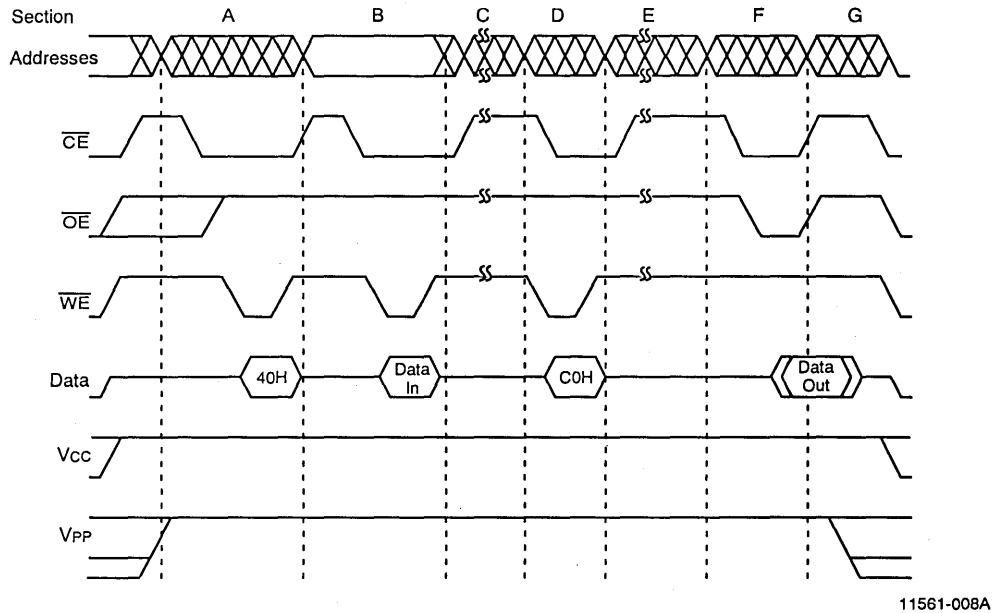
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Timeout	Write	Timeout	Read	Standby
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10 µs)	Program Verify	Transition (6 µs)	Program Verification	Proceed per Programming Algorithm

Figure 4. AC Waveforms for Programming Operations

Analysis of Program Timing Waveforms

Program Set-Up/Program

Two-cycle write commands are required for program operations (section A and B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-Out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Program-Verify

Upon completion of the program timing routine, the microprocessor must write the Program-Verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The Program-Verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:

The Program-Verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the Program-Verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1 μF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-Verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 μs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 μs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:

Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

V_{CC} Prior to V_{PP}

The Am28F512 powers-up in the Read only mode. In addition, memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} Prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the Set-Up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The Set-Up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the Set-Up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-System

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F512 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 25H (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... −65°C to +150°C
Plastic Packages ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to + 125°C

Voltage with Respect To Ground
All pins except A_9 and V_{PP} (Note 1) ... −2.0 V to 7.0 V

V_{CC} (Note 1) ..... −2.0 V to 7.0 V

A_9 (Note 2) ..... −2.0 V to 14.0 V

V_{PP} (Note 2) ..... −2.0 V to 14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on A_9 and V_{PP} pins is −0.5 V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) ..... −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) ..... −55°C to +125°C

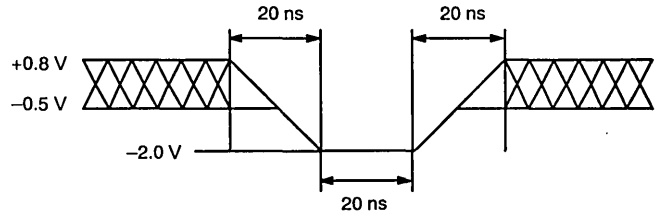
V_{CC} Supply Voltages
V_{CC} for Am28F512–X5 ..... +4.75 V to +5.25 V
V_{CC} for Am28F512–XX0 ..... +4.50 V to +5.50 V

V_{PP} Supply Voltages
Read ..... −0.5 V to +12.6 V
Program, Erase, and Verify ... +11.4 V to +12.6 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

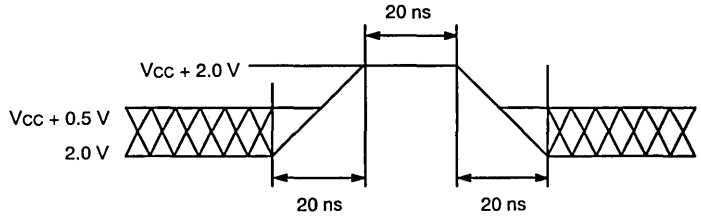
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



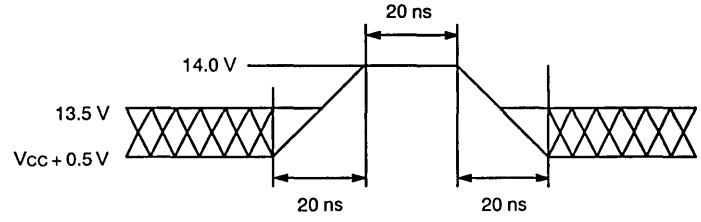
11561D-009B

Maximum Positive Input Overshoot



11561D-010B

Maximum V_{PP} Overshoot



11561D-011B

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max. V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max. V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
		V_{PP} = V_{PPL}			±1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4			V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V

Notes:

1. **Caution:** the Am28F512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

DC CHARACTERISTICS-CMOS COMPATIBLE

PRELIMINARY						
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max. V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max. V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4			
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V

Notes:

1. **Caution:** the Am28F512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

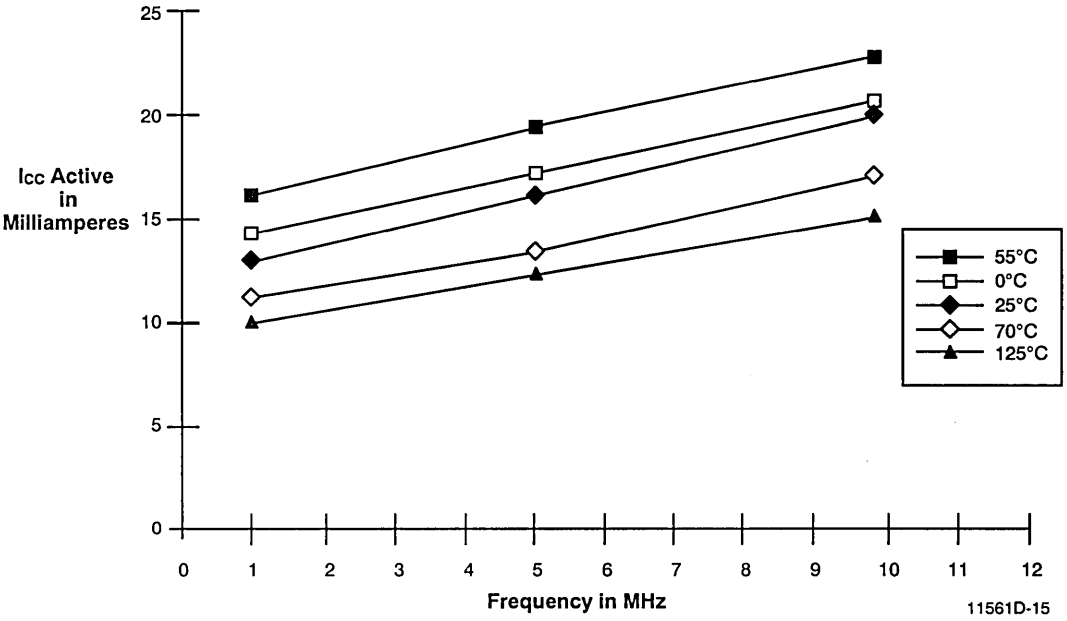


Figure 5. Am28F512 – Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
AC CHARACTERISTICS-Read Only Operation (Notes 1 and 2)

PRELIMINARY

Parameter Symbols				Am28F512					
				—	-90	-120	-150	-200	
JEDEC	Standard	Parameter Description		-75	-95	—	—	—	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min. Max.	70	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	70	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	70	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	35	50	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min. Max.	20	20	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min. Max.	20	20	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{VCS}		Vcc Set-up Time to Valid Read (Note 4)	Min. Max.	50	50	50	50	50	µs

Notes:

1. Output Load:
   1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 to 2.4 V,
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F512-75 and Am28F512-95 Output Load:
   1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. Guaranteed by design not tested.
4. Not 100% tested.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 5)

PRELIMINARY

Parameter Symbols				Am28F512					
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 5)	Min. Max.	70	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	45	50	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp (Note 5)	Min. Max.	100	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 5)	Min. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable Low (Note 5)	Min. Max.	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 5)	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 5)	Min. Max.	500	500	500	500	500	ns

Notes:

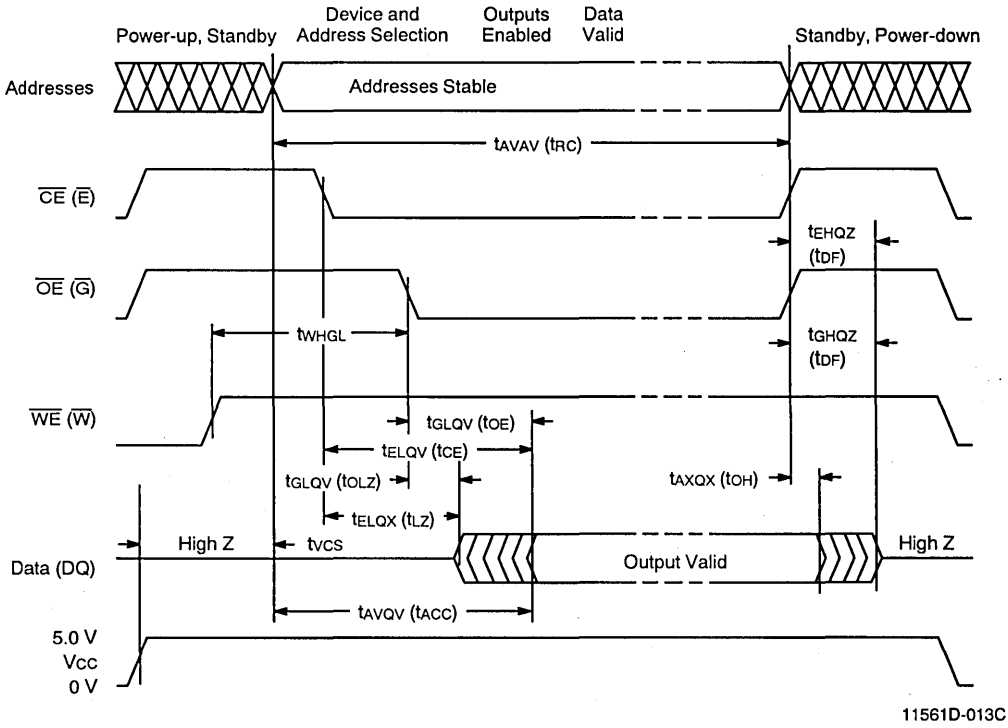
1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F512-75 and Am28F512-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F512-75 and Am28F512-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V
5. Not 100% tested.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



11561D-013C

Figure 6. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

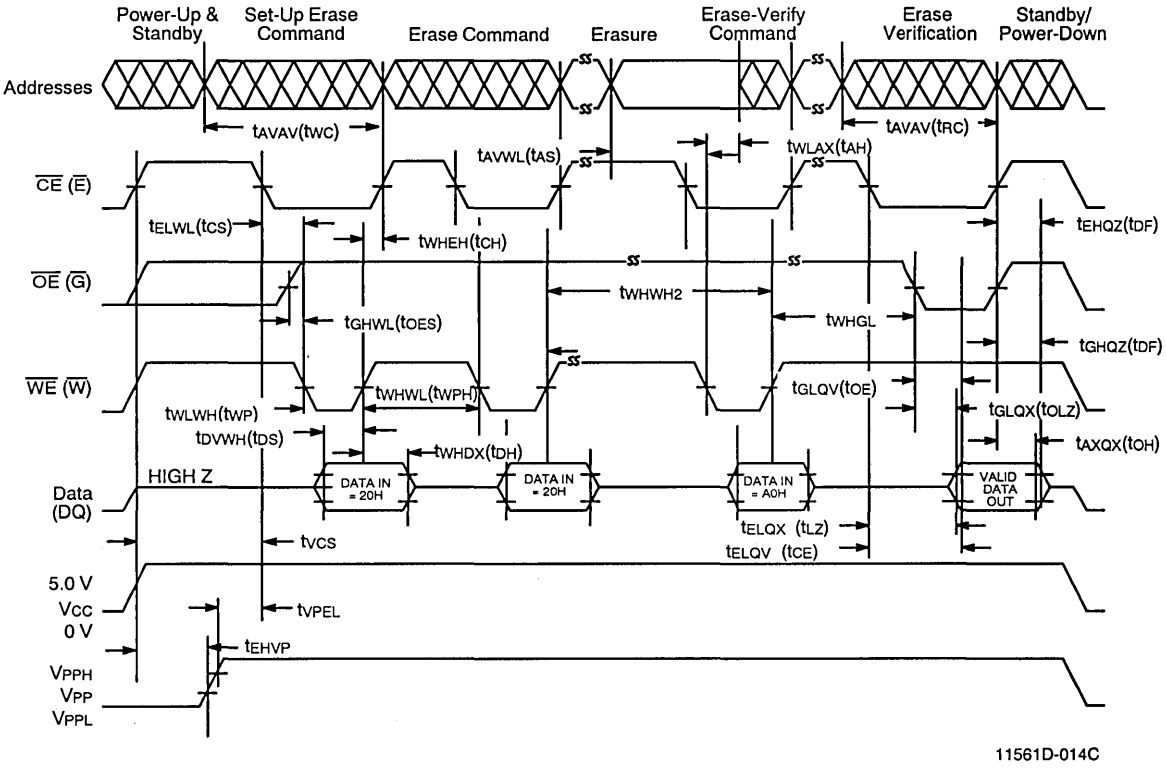


Figure 7. AC Waveforms for Erase Operations

SWITCHING WAVEFORMS

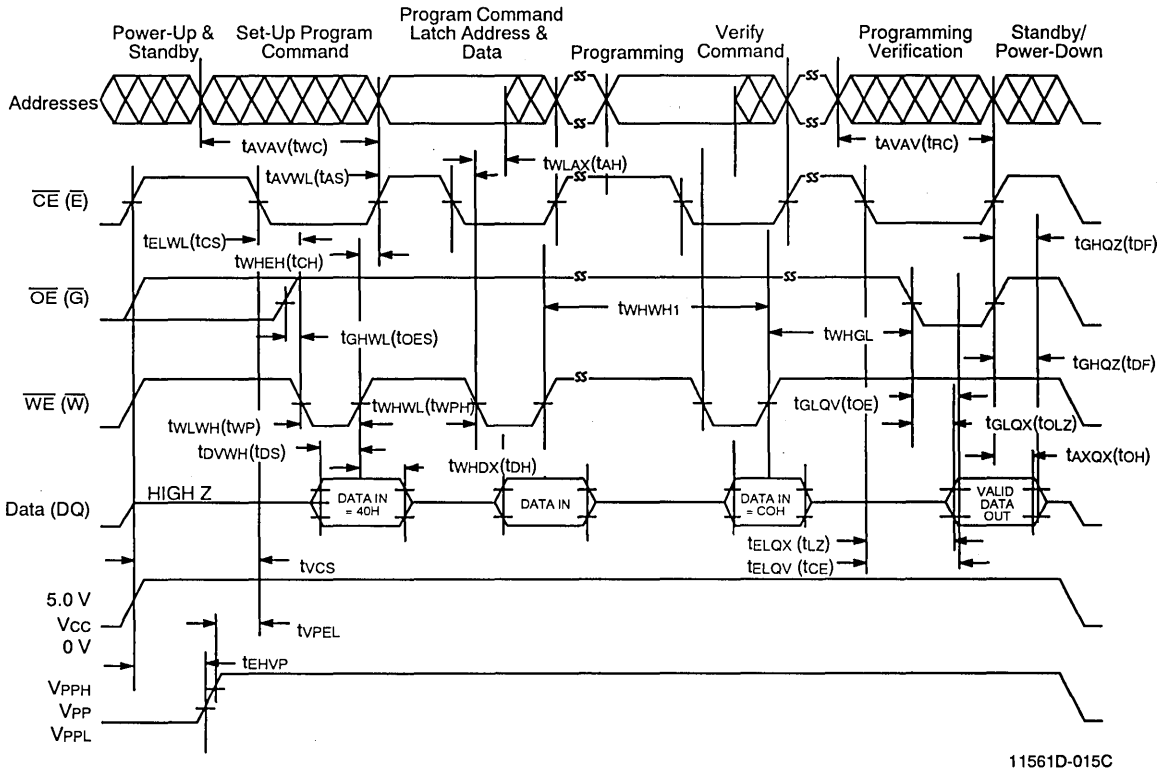
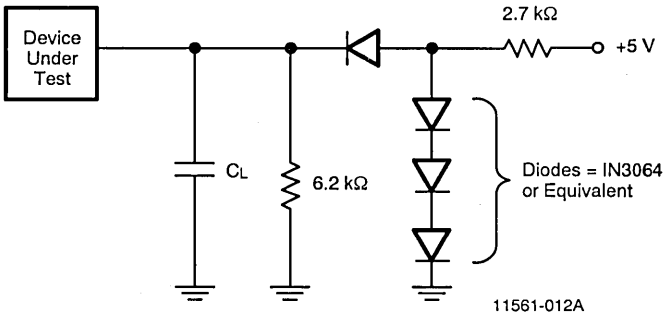


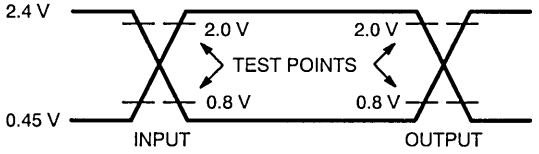
Figure 8. AC Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



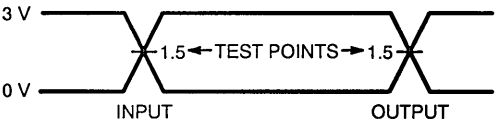
C_L = 100 pF including jig capacitance.

SWITCHING TEST WAVEFORMS



All Devices Except Am28F512-75 and Am28F512-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F512-75 and Am28F512-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

11561D-013A

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max. (Note 2)		
Chip Erase Time		1 (Note 1)	10	S	Excludes 00H programming prior to erasure
Chip Programming Time		0.5 (Note 1)	6	S	Excludes system-level overhead
Write/Erase Cycles	10,000			Cycles	

Notes:

1. 25°C, 12 V V_{PP}.
2. Maximum time specified is lower than worst case. Worst case is derived from the Flasherase/Flashrite pulse count (Flasherase = 1000 max and Flashrite = 25 max). Typical worst case for program and erase operations is significantly less than the actual device limit.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Min.	Units	Test Conditions
Min. Pattern Data Retention Time	10	Years	150°C
	20	Years	125°C

FINAL

Am28F010

131,072 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **CMOS Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **10,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ Programming**
  - 10 µs typical byte-program
  - Two seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F010 is a 1 Megabit Flash memory organized as 128K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F010 is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F010 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F010 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F010 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F010 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to Vcc +1 V.

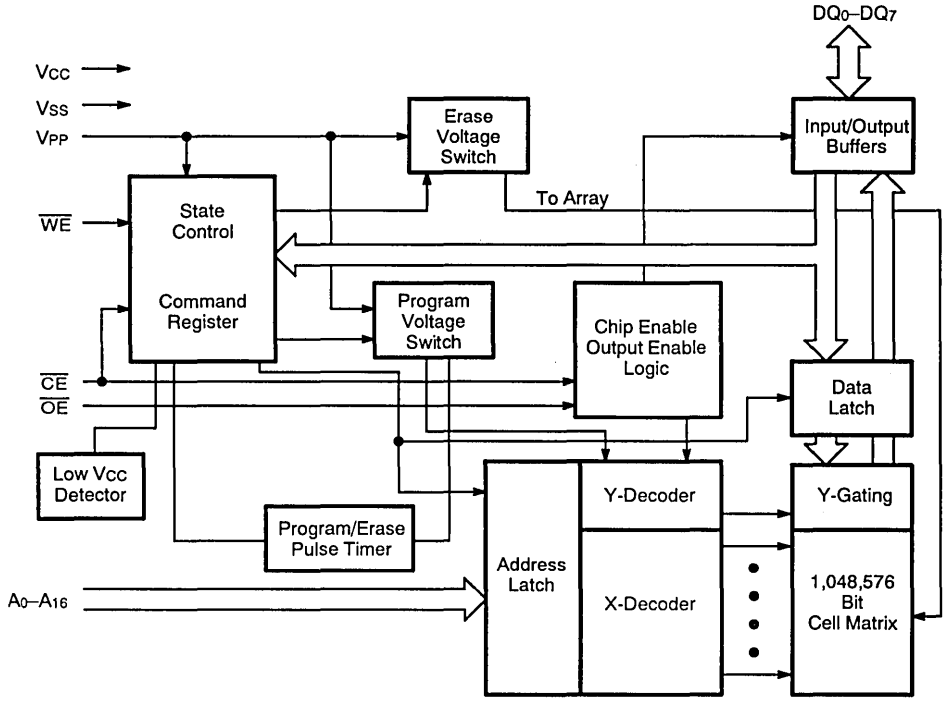
The Am28F010 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F010 is two seconds. The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase alrogithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM using ultra-violet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F010 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F010 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 11559 Rev. E Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



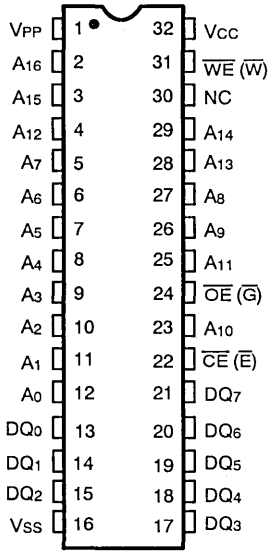
11559E-1

PRODUCT SELECTOR GUIDE

Family Part No.:	Am28F010				
Ordering Part No.: ±10% VCC Tolerance	-90	-120	-150	-200	-250
±5% VCC Tolerance	-95	—	—	—	—
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	55	55	55

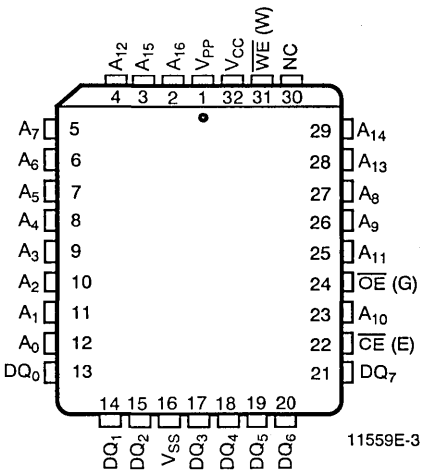
CONNECTION DIAGRAMS

DIP



11559E-2

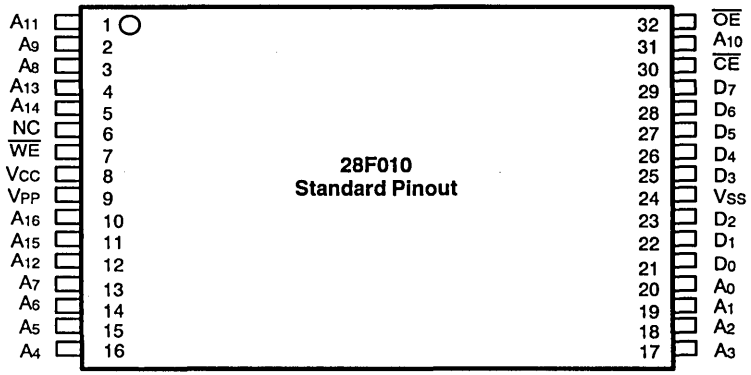
PLCC*



11559E-3

Note: Pin 1 is marked for orientation.
*Also available in LCC.

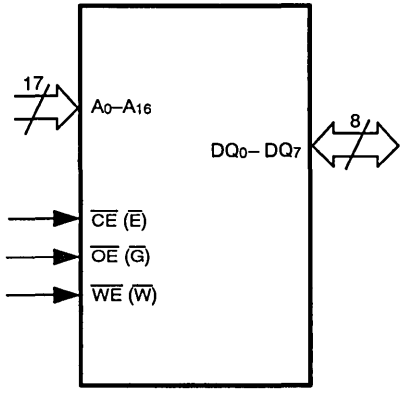
TSOP PACKAGES*



11559E-4

28F010 128K x 8 Flash Memory in 32 Lead TSOP

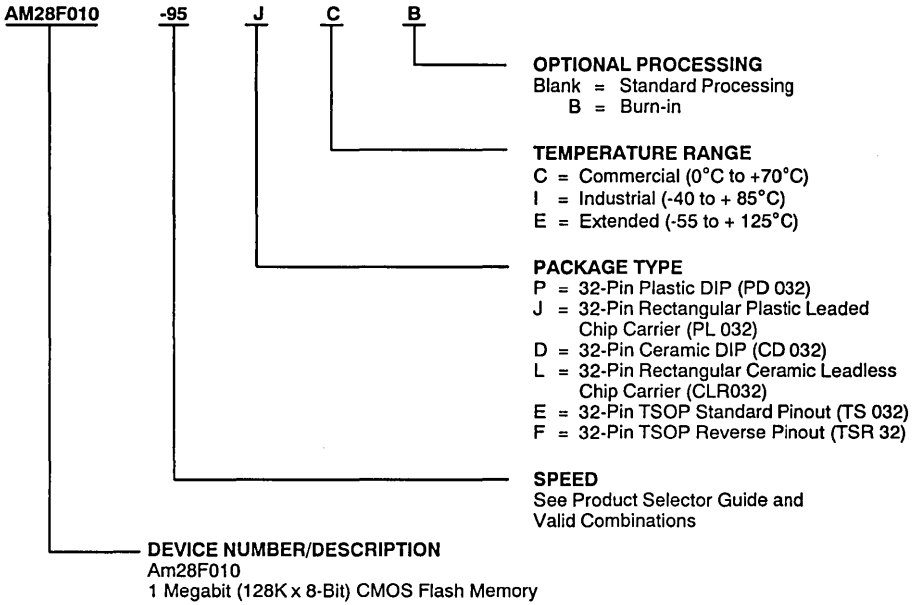
LOGIC SYMBOL



11559E-5

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



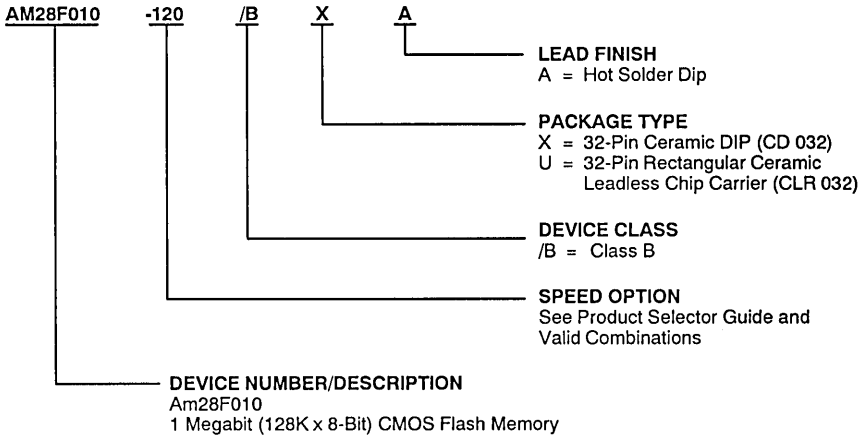
Valid Combinations	
AM28F010-90 AM28F010-95	PC, JC, DC, LC, EC, FC
AM28F010-120 AM28F010-150 AM28F010-200	PC, PI, PE, PEB, JC, JI, JE, JEB, DC, DI, DE, DEB, LC, LI, LE, LEB, EC, FC, EI, FI, EE, FE, EEB, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F010-120 AM28F010-150 AM28F010-200 AM78F010-250	/BXA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{SS}
Ground

NC
No Connect-corresponding pin is not connected internally to the die.

A_0–A_{16}
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

DQ_0–DQ_7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F010 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F010 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F010's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F010 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Flasherase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Erase Set-Up:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command. An integrated stop timer prevents any possibility of overerasure.
3. **Erase-Verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Program Set-Up:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command. An integrated stop timer prevents any possibility of overprogramming.
3. **Program-Verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Data Protection

The Am28F010 is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F010 powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F010 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A7H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0$ V
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V

Command Register Inactive

Read

The Am28F010 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F010 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC}-t_{OE}$).

Standby Mode

The Am28F010 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F010 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F010 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A7	1	0	1	0	0	1	1	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%
Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits R_7–R_0 correspond to the data inputs DQ_7–DQ_0 (refer to Table 3). Register bits R_7–R_5 store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}.

If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6 µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands (Notes 1, 2)	X	X	X	X	X	X	X	X

Notes:

1. See Table 4 Am28F010 Command Definitions.
2. X = Appropriate Data or Register Commands.

Table 4. Am28F010 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 6, 7)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A7H
Erase Set-up/Erase Write (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Program Set-up/ Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 7)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6 μs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
7. Please reference Reset Command section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-up is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Erase Set-up operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{pp} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:

The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-Verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F010 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Erase Set-up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

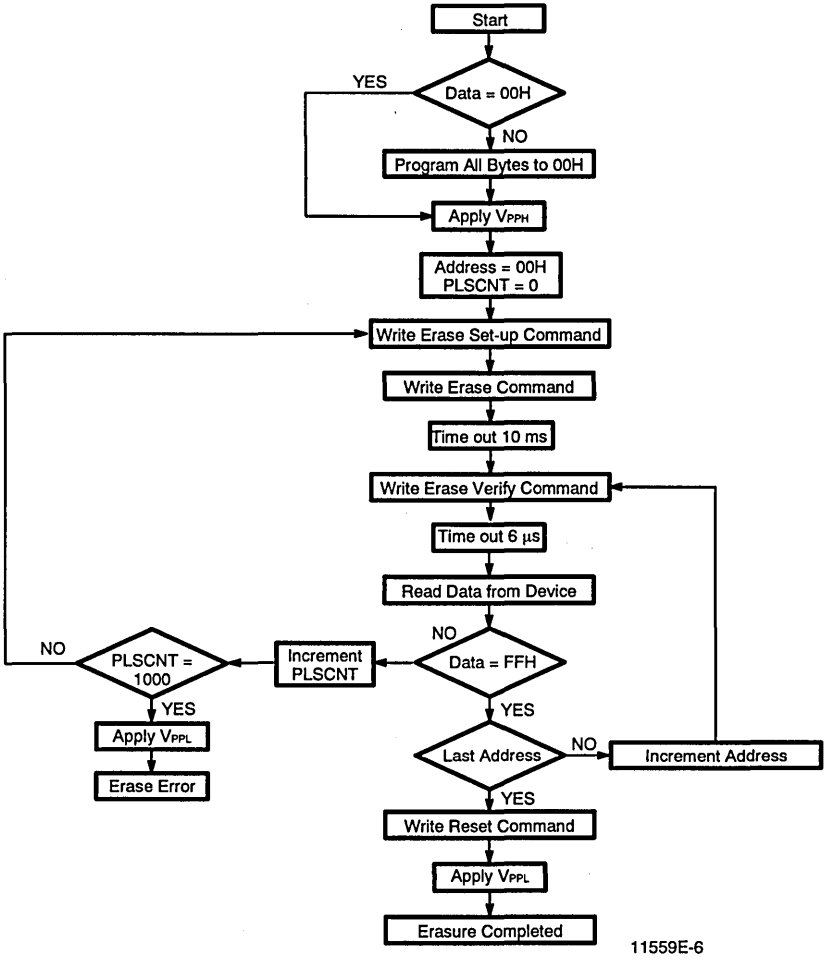


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F010 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

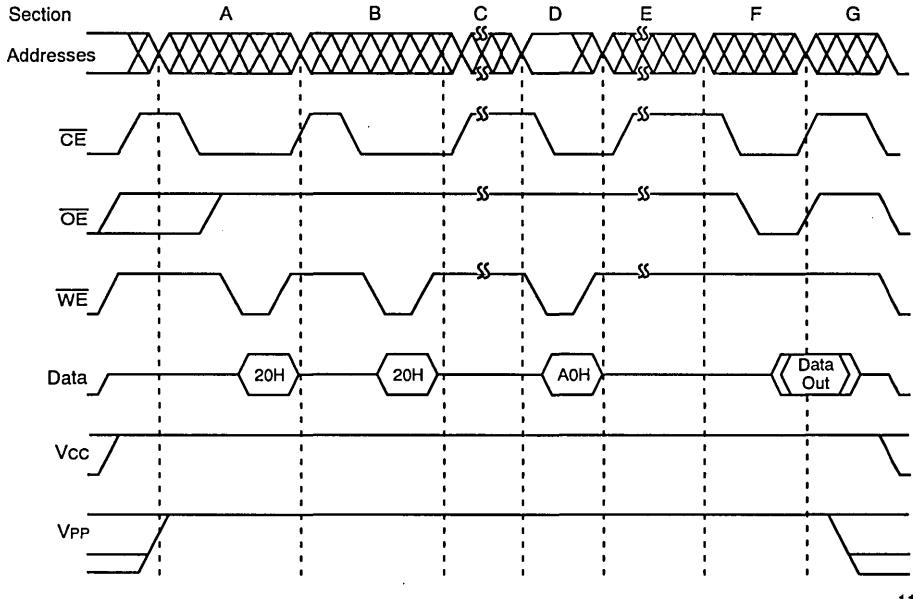
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (one second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase pulses are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 3) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-Up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Standby
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Erase Set-up	Erase	Erase (10 ms)	Erase-Verify	Transition (6 μs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. AC Waveforms For Erase Operations

Analysis of Erase Timing Waveform

Note:

This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Erase Set-Up/Erase

This analysis illustrates the use of two-cycle erase commands (section A and B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-Out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note:

An integrated stop timer prevents any possibility of over-erasure by limiting each time-out period of 10 ms.

Erase-Verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 μs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat

sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Note:

All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The Am28F010 is programmed byte by byte. Bytes may be programmed sequentially or at random. Program Set-up is the first of a two-cycle program command. It stages the device for byte programming. The Program Set-up operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F010 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Program Set-up/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F010 Flashrite Programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite Programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

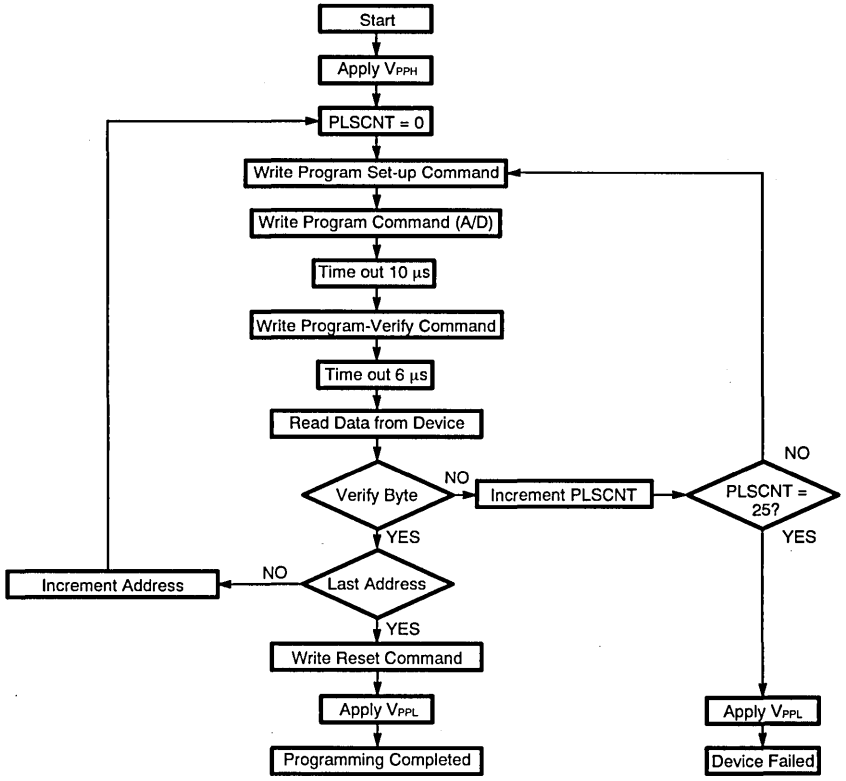


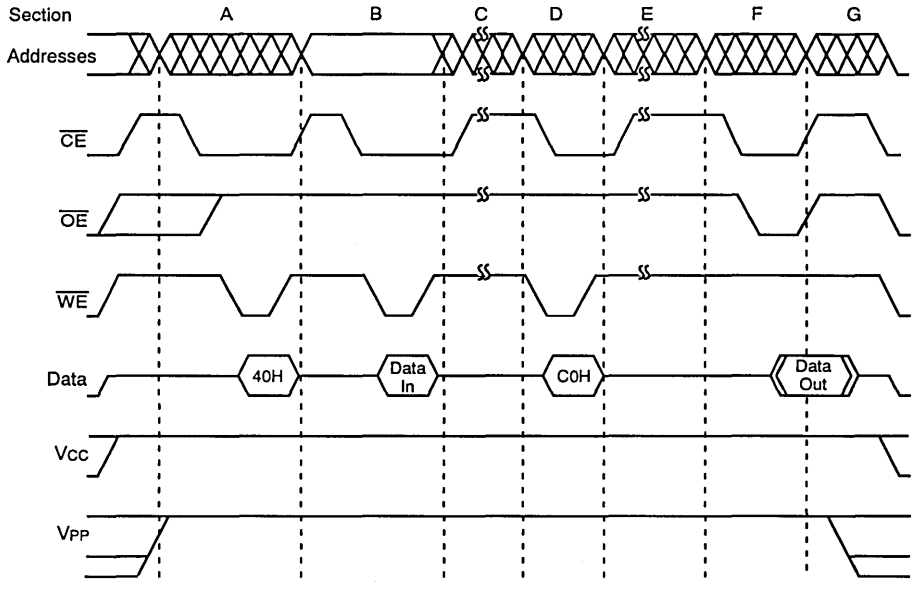
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Program Set-Up	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



11559E-9

	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Standby
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Program Set-up	Program Command Latch Address & Data	Program (10 µs)	Program Verify	Transition (6 µs)	Program Verification	Proceed per Programming Algorithm

Figure 4. AC Waveforms for Programming Operations

Analysis of Program Timing Waveforms

Program Set-Up/Program

Two-cycle write commands are required for program operations (section A and B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-Out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note:

An integrated stop timer prevents any possibility of over-programming by limiting each time-out period of 10 µs.

Program-Verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1 μF/device. V_{PP} must reach its final value 100 ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse.
3. A third delay time is required for each programming pulse width (10 μs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 μs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified separately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F010 powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F010 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code A7H (see Table 2). To terminate the operation, it is necessary to write another valid command into the register (see Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... −65°C to +150°C
Plastic Packages ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to + 125°C

Voltage with Respect To Ground
All pins except A_9 and V_{PP} (Note 1) . −2.0 V to +7.0 V

V_{CC} (Note 1) ..... −2.0 V to +7.0 V

A_9 (Note 2) ..... −2.0 V to +14.0 V

V_{PP} (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on A_9 and V_{PP} pins is −0.5 V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) ..... −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) ..... −55°C to +125°C

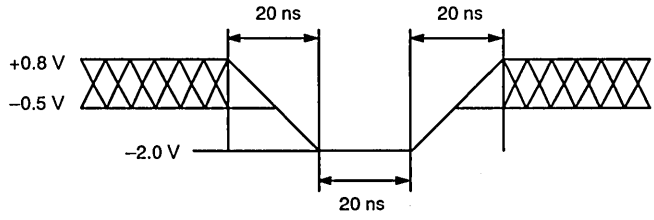
V_{CC} Supply Voltages
V_{CC} for Am28F010–X5 ..... +4.75 V to +5.25 V
V_{CC} for Am28F010–XX0 ..... +4.50 V to +5.50 V

V_{PP} Supply Voltages
Read ..... −0.5 V to +12.6 V
Program, Erase, and Verify ... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

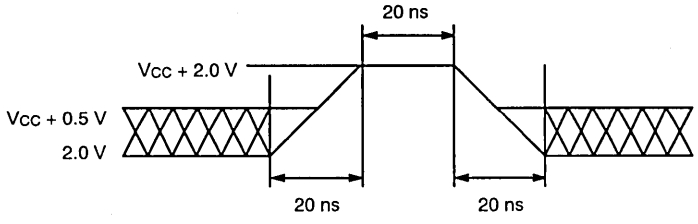
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



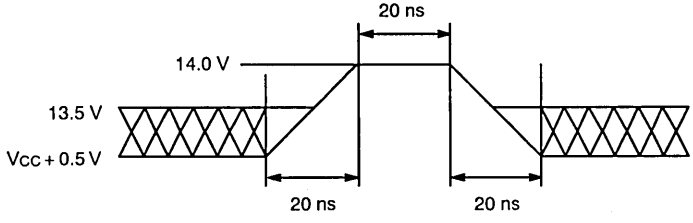
11559E-10

Maximum Positive Input Overshoot



11559E-11

Maximum V_{PP} Overshoot



11559E-12

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted) (Notes 1–3)

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
		V_{PP} = V_{PPL}			±1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		−0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA V_{CC} = V_{CC} Min.	2.4			V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. **Caution:** the Am28F010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			± 1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4			
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. **Caution:** the Am28F010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

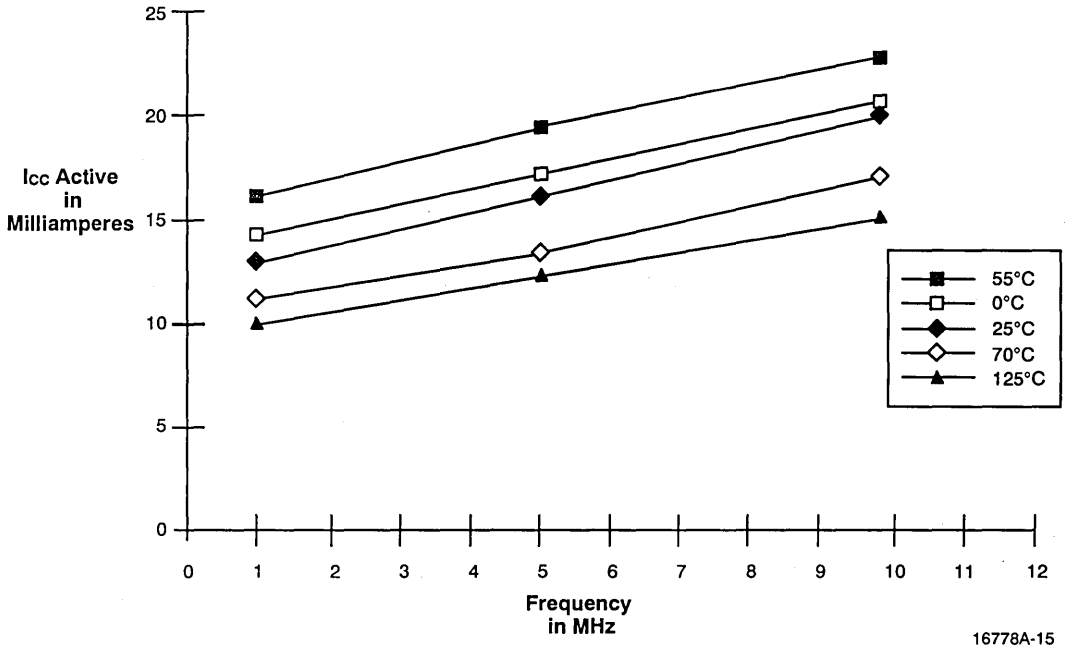


Figure 5. Am28F010–Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1 and 2)

Parameter Symbols				Am28F010					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min. Max.	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min. Max.	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min. Max.	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min. Max.	50	50	50	50	50	µs

Notes:

1. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F010-95 Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. Guaranteed by design not tested.
4. Not 100% tested.

AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 5)

Parameter Symbols				Am28F010					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min. Max.	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width Max.	Min.	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation (Note 4)	Min. Max.	10	10	10	10	10	µs
t_{WHWH2}		Duration of Erase Operation (Note 4)	Min. Max.	9.5	9.5	9.5	9.5	9.5	ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 10% V_{PPL} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min. Max.	100	100	100	100	100	ns

Notes:

1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.
2. All devices except Am28F010-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
3. Am28F010-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V
4. Maximum pulse widths not required because the on-chip program/erase stop timer will terminate the pulse widths internally on the device.
5. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
6. Not 100% tested.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

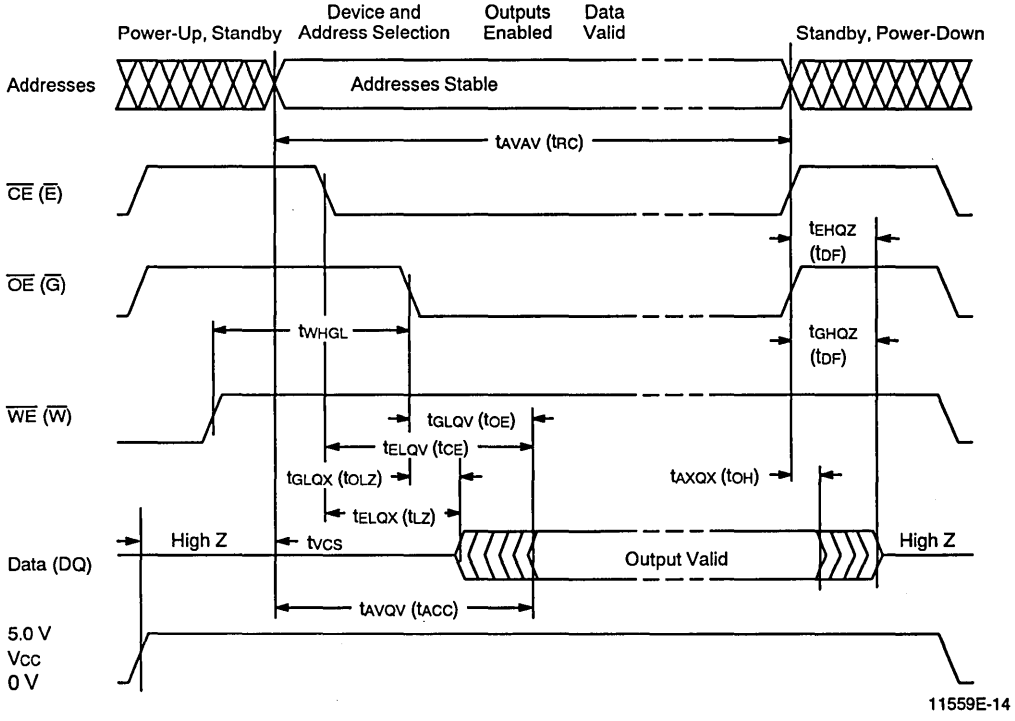
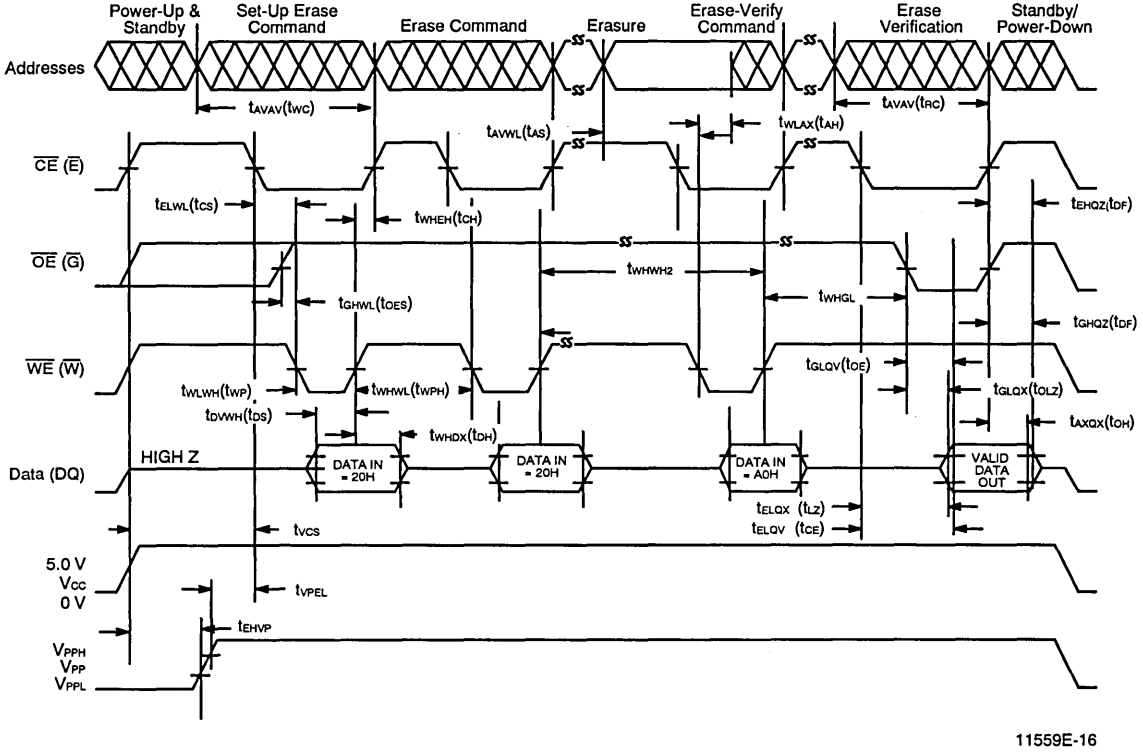


Figure 6. AC Waveforms for Read Operations

SWITCHING WAVEFORMS



11559E-16

Figure 7. AC Waveforms for Erase Operations

SWITCHING WAVEFORMS

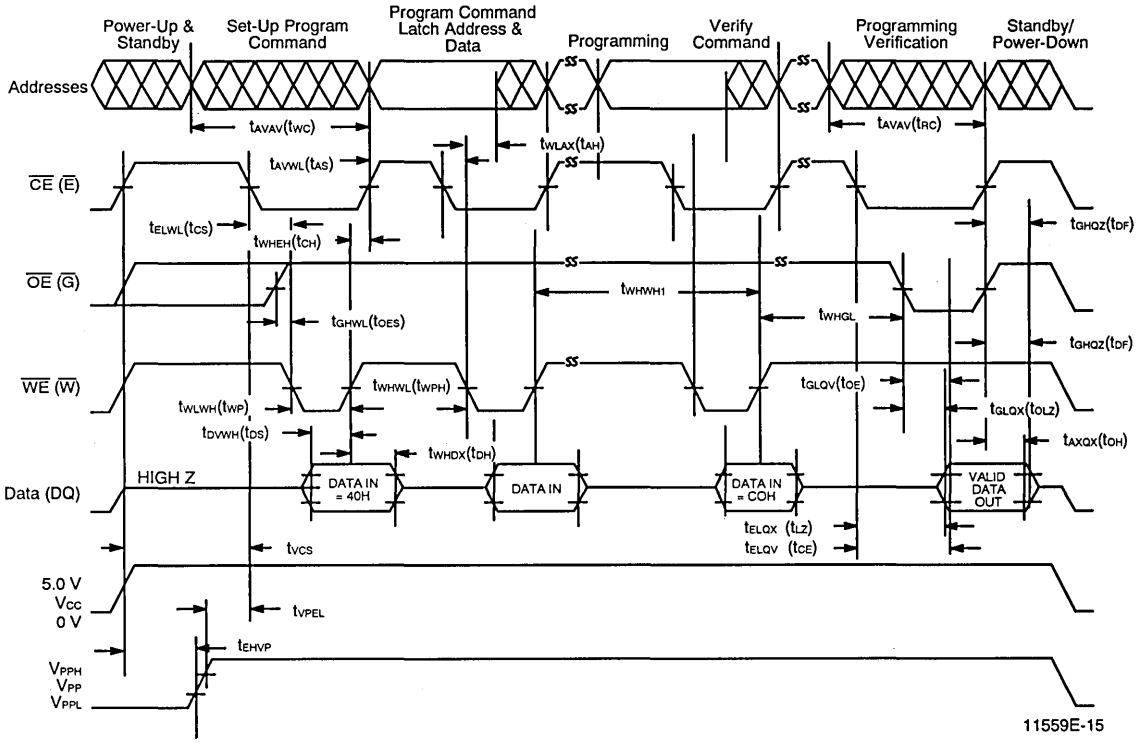
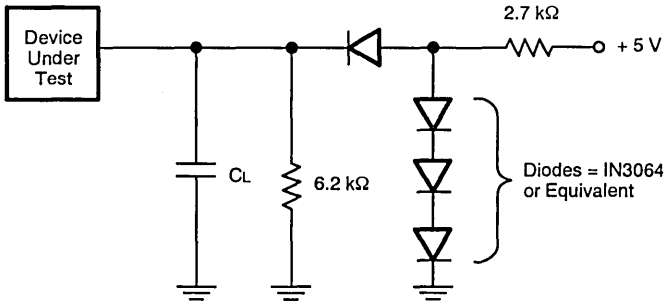


Figure 8. AC Waveforms for Programming Operations

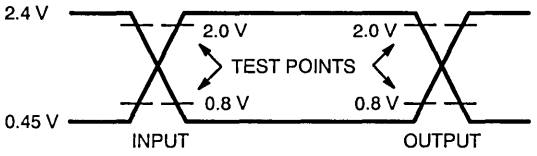
SWITCHING TEST CIRCUIT



11559E-17

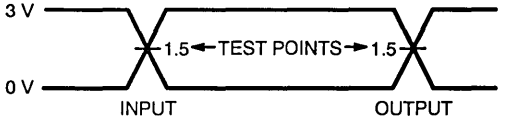
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F010-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F010-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

11559E-18

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.[3]		
Chip Erase Time		1 (Note 1)	10 (Note 2)	S	Excludes 00H programming prior to erasure
Chip Programming Time		2 (Note 1)	12.5	S	Excludes system-level overhead
Write/Erase Cycles	10,000			Cycles	

Notes:

1. 25°C, 12 V V_{PP}
2. The Flasherase/Flashrite algorithms allows for 60 second erase time for military temperature range operations.
3. Maximum time specified is lower than worst case. Worst case is derived from the Flasherase/Flashrite pulse count (Flasherase = 1000 max. and Flashrite = 25 max.). Typical worst case for program and erase operations is significantly less than the actual device limit.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Min.	Units	Test Conditions
Min. Pattern Data Retention Time	10	Years	150°C
	20	Years	125°C

FINAL

Am28F010A

131,072 x 8-Bit CMOS Flash Memory with Embedded Algorithms

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **CMOS low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **100,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Embedded Erase™ Electrical Bulk Chip-Erase**
  - Three second typical chip-erase including pre-programming
- **Embedded Program™**
  - 14 µs typical byte-program including time-out
  - Two seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Embedded algorithms for completely self-timed write/erase operations**
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F010A is a 1 Megabit Flash memory organized as 128K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non- volatile random access memory. The Am28F010A is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F010A offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F010A has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F010A uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F010A uses a 12.0 V ± 5% V_{PP} supply to perform the erase and programming functions.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC} +1 V.

Embedded Program

The Am28F010A is byte programmable using the Embedded Programming algorithm. The Embedded Programming algorithm does not require the system to time-out or verify the data programmed. The typical room temperature programming time of the Am28F010A is two seconds.

Embedded Erase

The entire chip is bulk erased using the Embedded Erase algorithm. The Embedded Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device. Typical erasure at room temperature is accomplished in one second.

AMD's Am28F010A is entirely pin and software compatible with AMD Am28F020A Flash memory.

Publication# 16778 Rev. A Amendment/0
Issue Date: September 1992

Embedded Programming Algorithm vs. Flashrite Programming Algorithm

The Flashrite Programming algorithm requires the user to write a program set-up command, a program command (program data and address), and a program verify command followed by a read and compare operation. The user is required to time the programming pulse width in order to issue the program verify command. An integrated stop timer prevents any possibility of overprogramming. Upon completion of this sequence the data is read back from the device and compared by the user with the data intended to be written; if there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 25 times.

AMD's Embedded Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, similar to data polling, provides feedback to the user as to the status of the programming operation.

Embedded Erase Algorithm vs. Flasherase Erase Algorithm

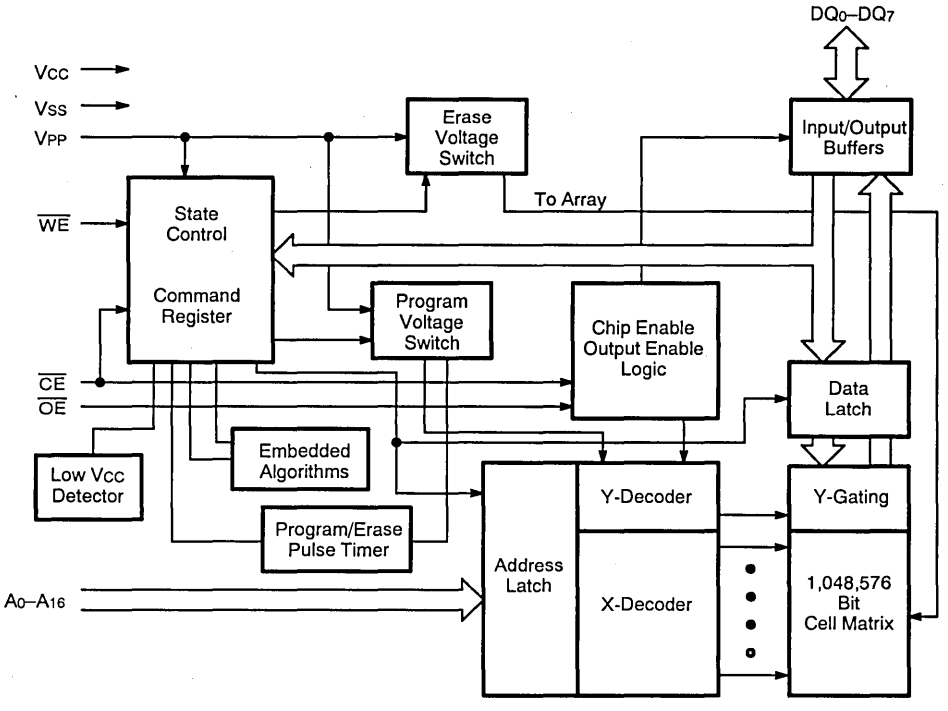
The Flasherase Erase algorithm requires the device to be completely programmed prior to executing an erase command. To invoke the erase operation the user writes an erase set-up command, an erase command, and an erase verify command. The user is required to time the erase pulse width in order to issue the erase verify command. An integrated stop timer prevents any possibility of overerasure. Upon completion of this sequence the data is read back from the device and compared by the user with erased data. If there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 6,000 times.

AMD's Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, similar to data polling, provides feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F010A is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F010A electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



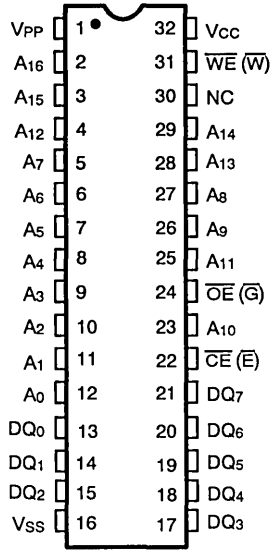
16778A-1

PRODUCT SELECTOR GUIDE

Family Part No.:	Am28F010A				
Ordering Part No.: ± 10% V_{CC} Tolerance	-90	-120	-150	-200	-250
± 5% V_{CC} Tolerance	-95	—	—	—	—
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	55	55	55

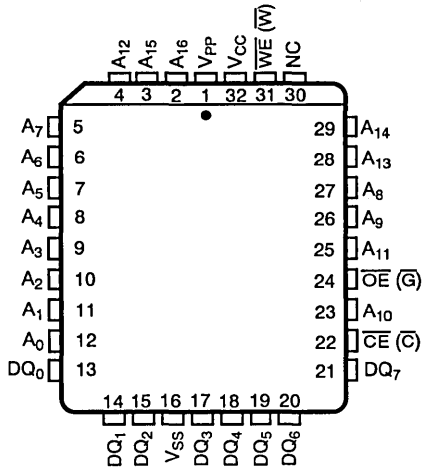
CONNECTION DIAGRAMS

DIP



16778A-2

PLCC*

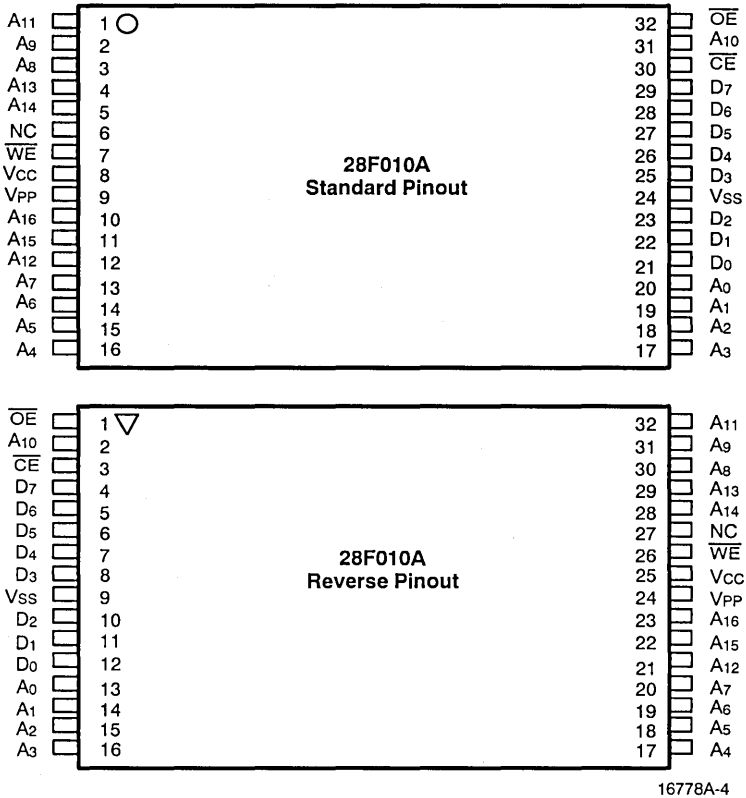


16778A-3

Notes:

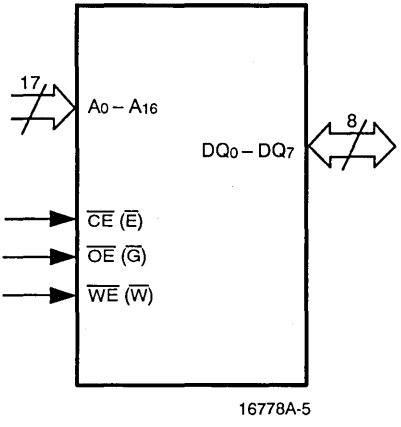
Pin 1 is marked for orientation.
*Also available in LCC.

TSOP PACKAGES



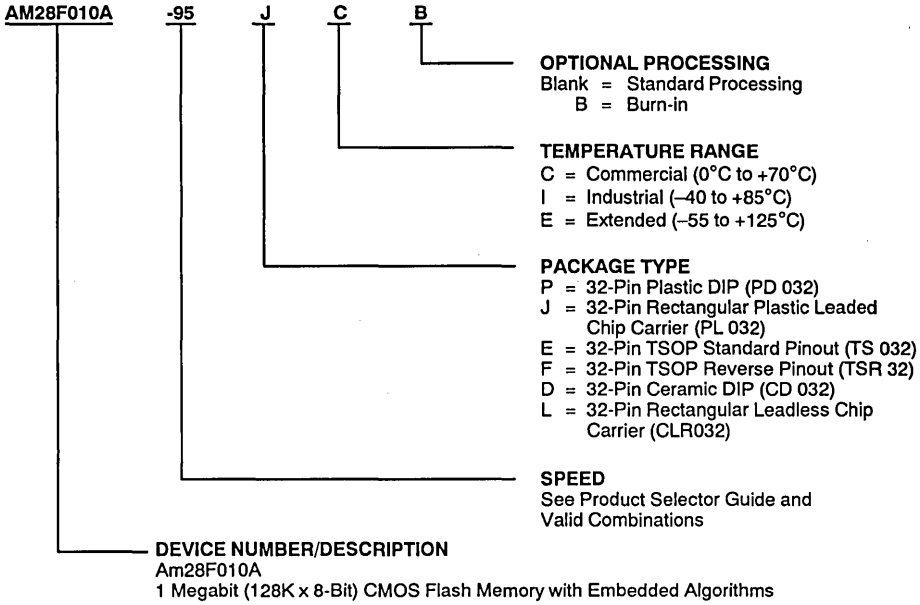
28F010A 128K x 8 Flash Memory in 32 Lead TSOP

LOGIC SYMBOL



ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F010A-90 AM28F010A-95	PC, JC, EC, FC, DC, LC
AM28F010A-120 AM28F010A-150 AM28F010A-200	PC, PI, JC, JI, PE, PEB, JE, JEB, EC, FC, EI, FI, EE, FE, EEB, FEB, DC, DI, DE, DEB, LC, LI, LE, LEB

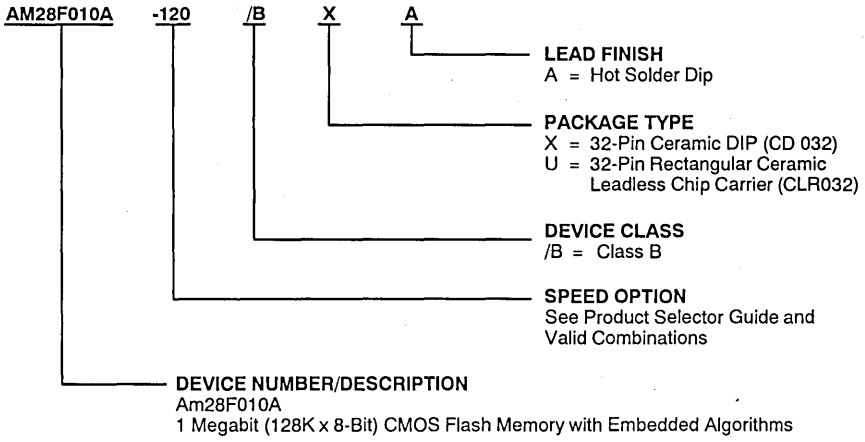
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F010A-120 AM28F010A-150 AM28F010A-200 AM78F010A-250	/BXA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

V_{PP}

Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{CC}

Power supply for device operation. (5.0 V ± 5% or 10%)

V_{SS}

Ground

NC

No Connect-corresponding pin is not connected internally to the die.

A_0–A_{16}

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

DQ_0–DQ_7

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)

The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F010A uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F010A functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F010A's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F010A is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Embedded Erase Algorithm

AMD now makes erasure extremely simple and reliable. The Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. The device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, similar to $\overline{Data}$ Polling, provides feedback to the user as to the status of the erase operation.

Embedded Programming Algorithm

AMD now makes programming extremely simple and reliable. The Embedded Programming algorithm requires the user to only write a program set-up command and a program command. The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, similar to $\overline{Data}$ Polling, provides feedback to the user as to the status of the programming operation.

Data Protection

The Am28F010A is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F010A powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION
Description of User Modes

Table 1. Am28F010A User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A2H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V; see DC Characteristics for voltage levels of V_{PPH}, 0V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0$ V
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V

Command Register Inactive

Read

The Am28F010A functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F010A has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F010A has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F010 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F010A Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A2	1	0	1	0	0	0	1	0

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%
Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits R_7–R_0 correspond to the data inputs DQ_7–DQ_0 (refer to Table 3). Register bits R_7–R_5 store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6 µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands (Notes 1, 2)	X	X	X	X	X	X	X	X

Notes:

1. See Table 4 Am28F010A Command Definitions.
2. X = Appropriate Data or Register Commands.

Table 4. Am28F010A Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 4, 5)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A2H
Embedded Erase Set-up/ Embedded Erase	Write	X	30H	Write	X	30H
Embedded Program Set-up/Embedded Program	Write	X	10H or 50H	Write	PA	PD
Reset (Note 5)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
4. Wait 6 μs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
5. Please reference Reset Command section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Embedded Program and Erase Operations

Embedded Erase Algorithm

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Embedded set-up erase command and Embedded erase command. Upon executing the Embedded erase command the device automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the device is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase Set-Up command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Embedded Erase Set-Up is performed by writing 30H to the command register.

To commence automatic chip erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 5 and Table 5 illustrate the Embedded Erase algorithm, a typical command string and bus operations.

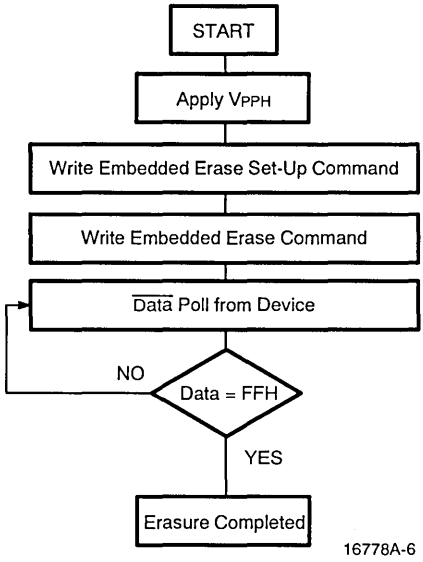


Figure 5. Embedded Erase Algorithm

Table 5. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation.

Embedded Programming Algorithm

The Embedded Program Set-Up is a command only operation that stages the device for automatic programming. Embedded Program Set-Up is performed by writing 10H or 50H to the command register.

Once the Embedded Set-Up Program operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode (no program verify command is required).

Figure 6 and Table 6 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

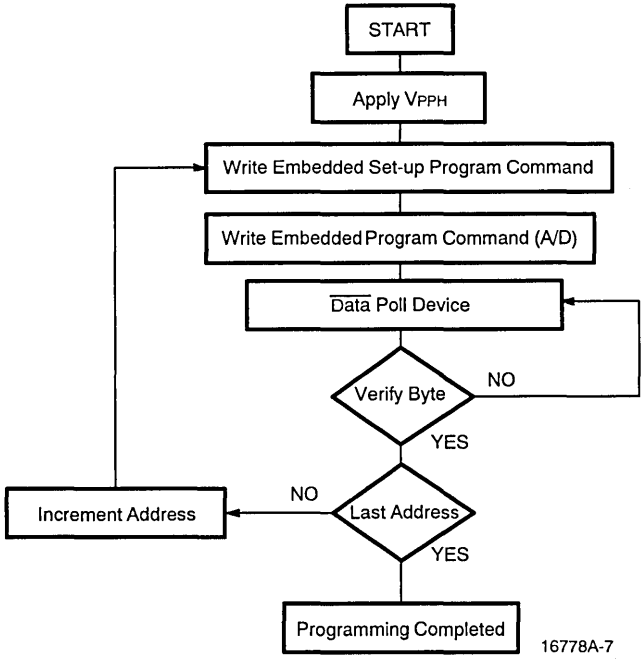


Figure 6. Embedded Programming Algorithm

Table 6. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-up Command	Data = 10H or 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{\text{Data}}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation. Device is either powered-down, erase inhibit or program inhibit.

Write Operation Status

$\overline{\text{Data}}$ Polling—DQ7

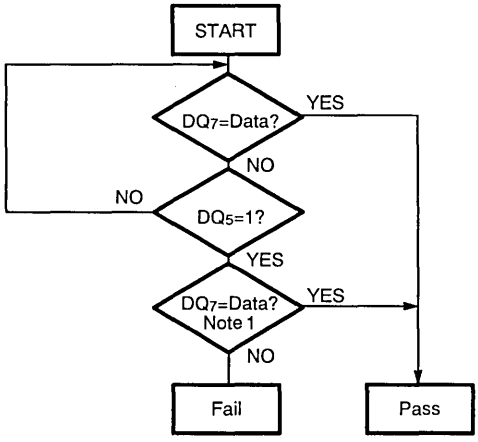
The Am28F010A features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device will produce the compliment of expected Valid data on DQ7. Upon completion of the Embedded Program algorithm an attempt to read the device will produce Valid data on DQ7. The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1." The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two Write pulse sequence.

The $\overline{\text{Data}}$ Polling feature is only active during Embedded Programming or erase algorithms.

See Figures 7a and 8a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams. $\overline{\text{Data}}$ Polling is the standard method to check the write operation status, however, an alternative method is available using Toggle Bit.



Note:

1. DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5 or after DQ_5.

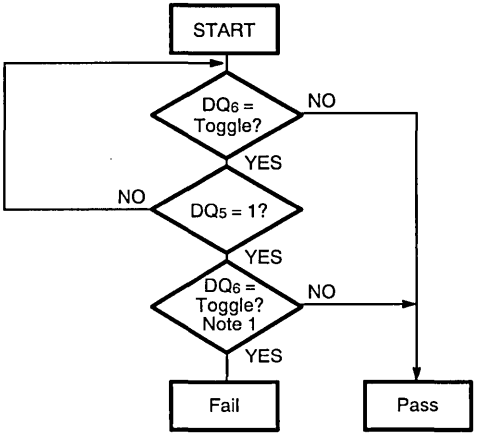
Figure 7a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Am28F010A also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the first $\overline{WE}$ pulse of the two write pulse sequence, unlike $\overline{Data}$ Polling which is valid after the rising edge of the second $\overline{WE}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

See Figures 7b and 8b for the Toggle Bit timing specifications and diagrams.



Note:

1. DQ_6 is rechecked even if DQ_5 = "1" because DQ_6 may stop toggling at the same time as DQ_5 changing to "1."

Figure 7b. Toggle Bit Algorithm

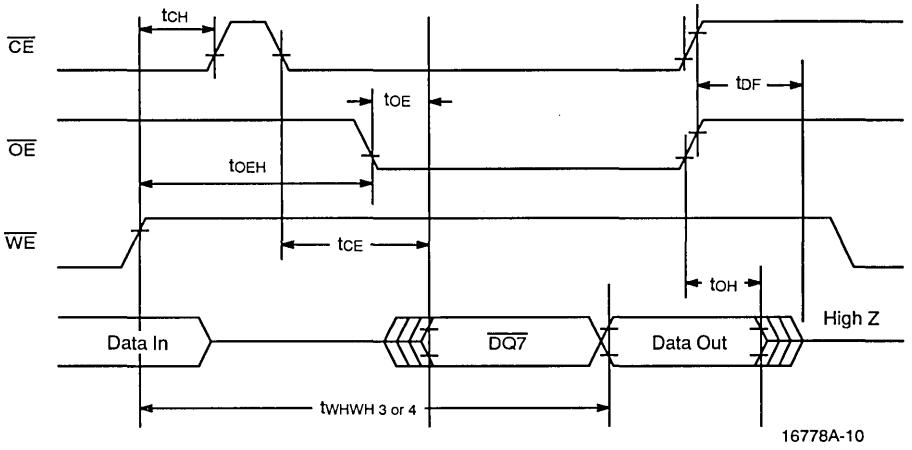


Figure 8a. AC Waveforms for $\overline{Data}$ Polling during Embedded Algorithm Operations

DQ_5
Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits. Under these conditions DQ_5 will produce a "1." The program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 1. To reset the device, write the Reset command sequence to the device.

DQ_4
Hardware Sequence Flag

If the device has exceeded the specified erase or program time and DQ5 is "1," then DQ_4 will indicate which step in the algorithm the device exceeded the limits. A "0" in DQ_4 indicates in programming, a "1" indicates an erase.

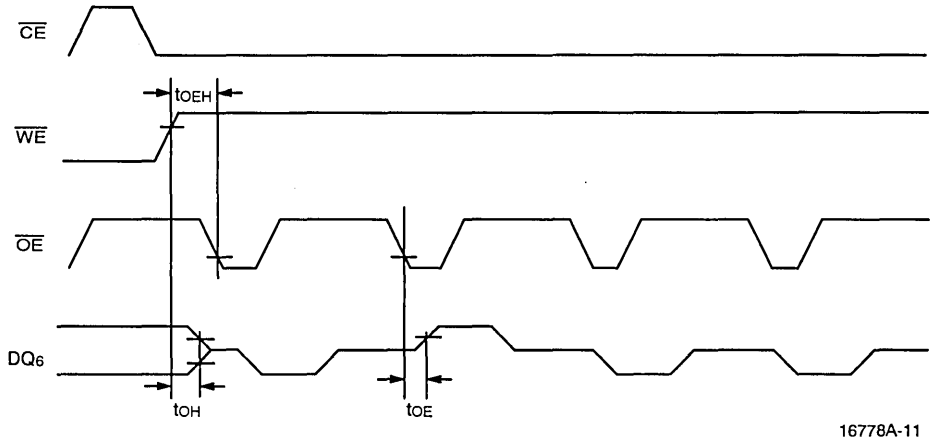


Figure 8b. AC Waveforms for Toggle Bit during Embedded Algorithm Operations

Parallel Device Erasure

The Embedded Erase algorithm greatly simplifies parallel device erasure. Since the erase process is internal to the device, a single erase command can be given to multiple devices concurrently.

This eliminates the complex design schemes otherwise required to prevent over-erasure of any one or more devices. Please reference the Parallel Device Erasure section of the Am28F010 data sheet.

Power-Up Sequence

The Am28F010A powers-up in the Read only mode. Power supply sequencing is not required.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-System

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F010A contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code A2 (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... –65°C to +150°C
Plastic Packages ..... –65°C to +125°C

Ambient Temperature
with Power Applied ..... –55°C to + 125°C

Voltage with Respect To Ground
All pins except A_9 and V_{PP}
(Note 1) ..... –2.0 V to +7.0 V

V_{CC} (Note 1) ..... –2.0 V to +7.0 V

A_9 (Note 2) ..... –2.0 V to +14.0 V

V_{PP} (Note 2) ..... –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on A_9 and V_{PP} pins is –0.5 V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) ..... –40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) ..... –55°C to +125°C

Military (M) Devices
Case Temperature (T_C) ..... –55°C to +125°C

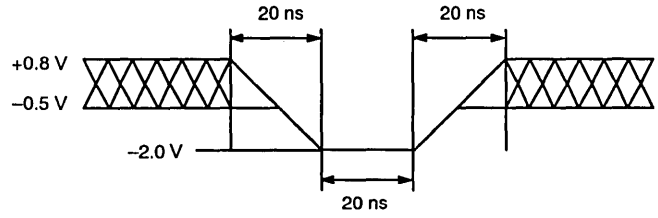
V_{CC} Supply Voltages
V_{CC} for Am28F010A–X5 ..... +4.75 V to +5.25 V
V_{CC} for Am28F010A–XX0 .... +4.50 V to +5.50 V

V_{PP} Supply Voltages
Read ..... –0.5 V to +12.6 V
Program, Erase, and Verify ... +11.4 V to +12.6 V

Operating ranges define those limits between which the funtionality of the device is guaranteed.

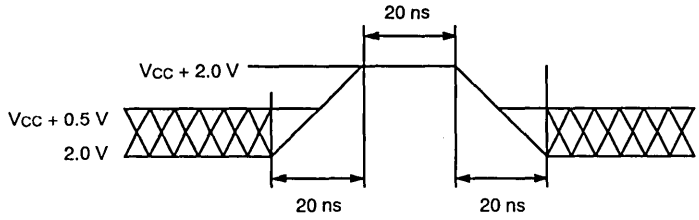
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



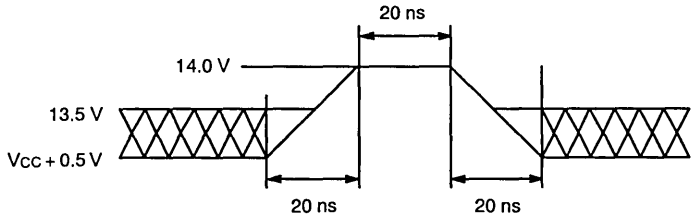
16778A-12

Maximum Positive Input Overshoot



16778A-13

Maximum V_{PP} Overshoot



16778A-14

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted) (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
		V_{PP} = V_{PPL}			±1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4			V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:

1. **Caution:** the Am28F010A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4			
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:

1. **Caution:** the Am28F010A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

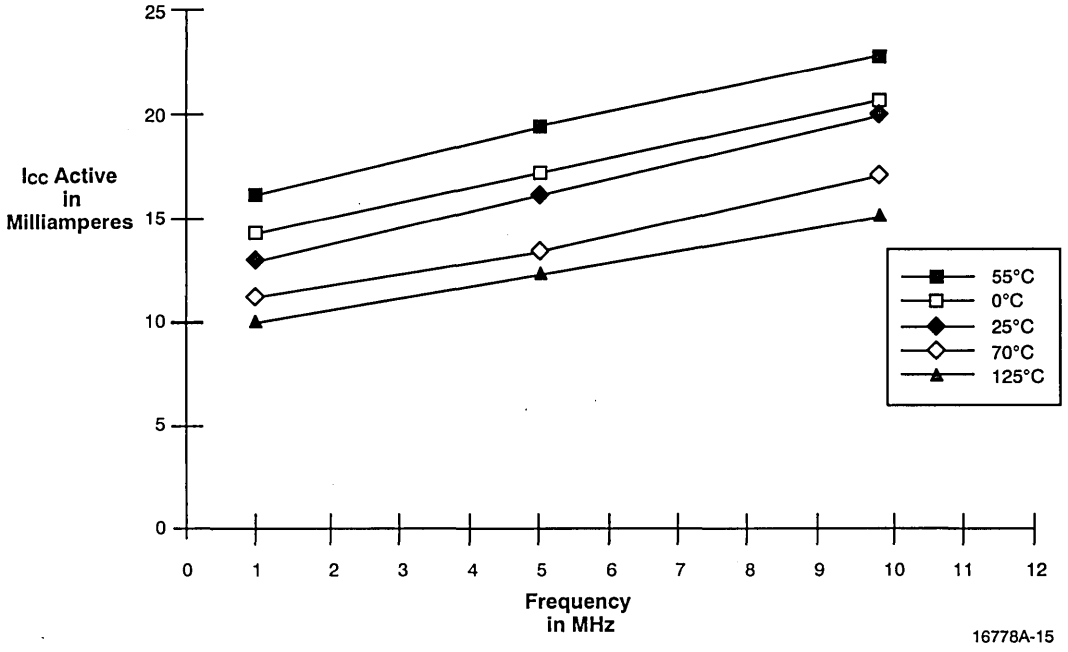


Figure 9. Am28F010A – Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1 and 2)

Parameter Symbols				Am28F010A					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min. Max.	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min. Max.	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min. Max.	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{VCS}		Vcc Set-up Time to Valid Read (Note 4)	Min. Max.	50	50	50	50	50	µs

Notes:

1. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F010A-95 Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. Guaranteed by design not tested.
4. Not 100% tested.

AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 5)

Parameter Symbols				Am28F010A					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min. Max.	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min. Max.	10	10	10	10	10	ns
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{ELWLE}	t_{CSE}	Chip Enable Embedded Algorithm Setup Time	Min. Max.	20	20	20	20	20	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width Max.	Min.	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{WHWH3}		Embedded Programming Operation (Note 4)	Typ. Max.	14	14	14	14	14	µs
t_{WHWH4}		Embedded Erase Operation (Note 5)	Typ. Max.	3	3	3	3	3	S
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min. Max.	100	100	100	100	100	ns

Notes:

1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.
2. All devices except Am28F010A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
3. Am28F010A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V
4. Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
5. Embedded erase operation of 3 sec consists of 2 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.
6. Not 100% tested.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

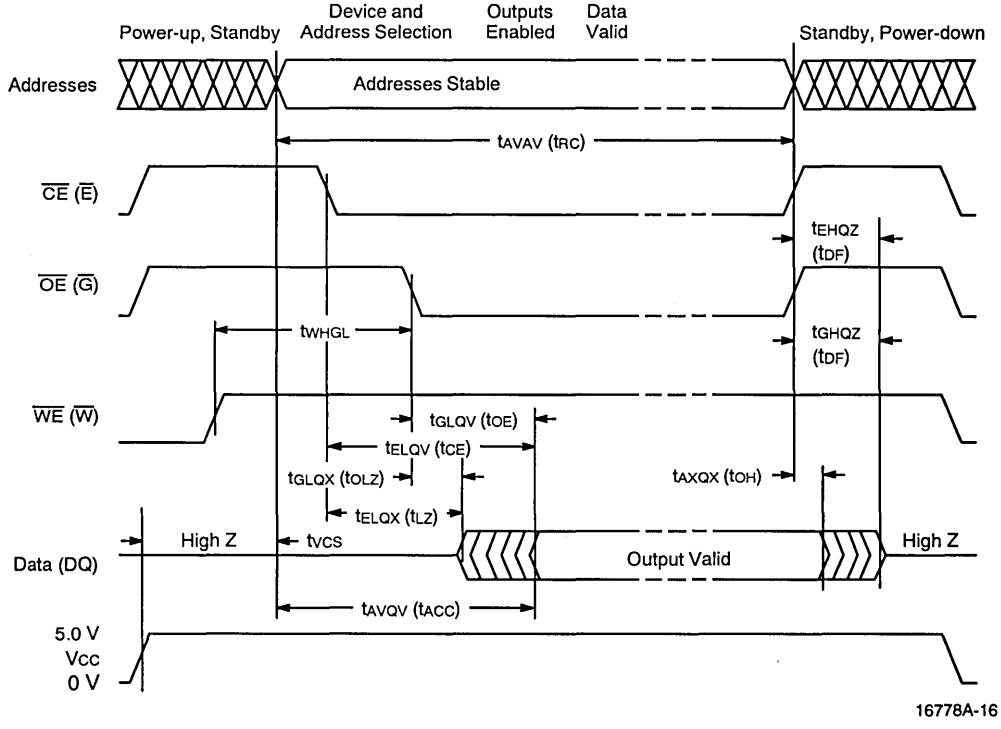
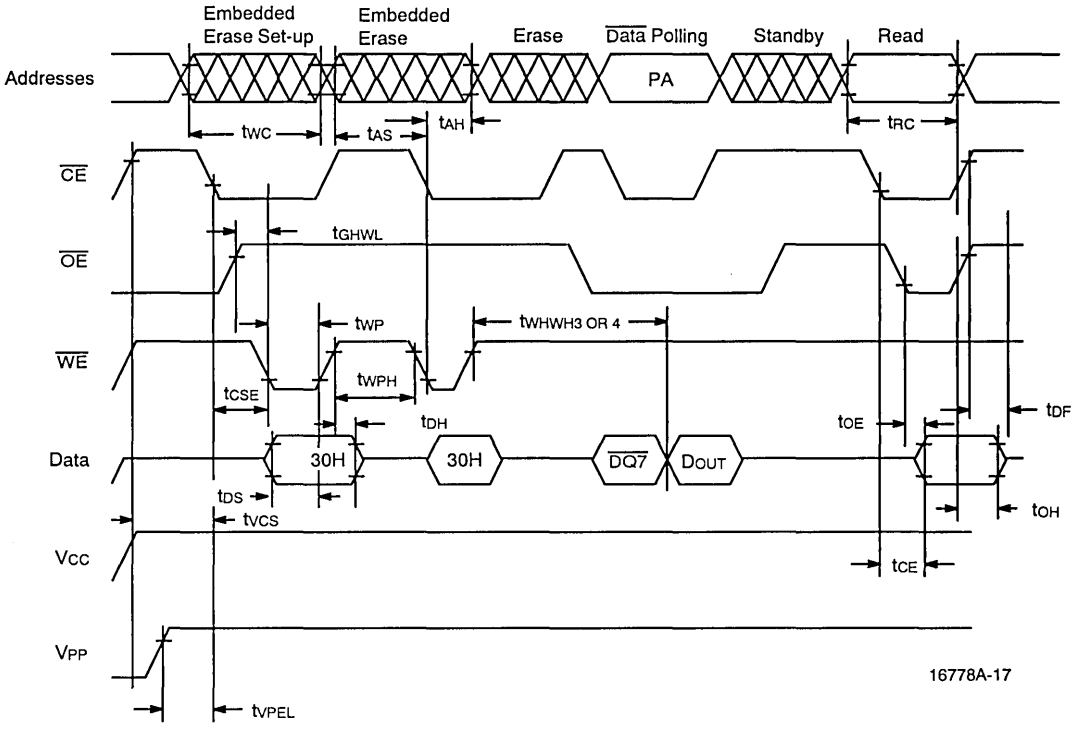


Figure 10. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

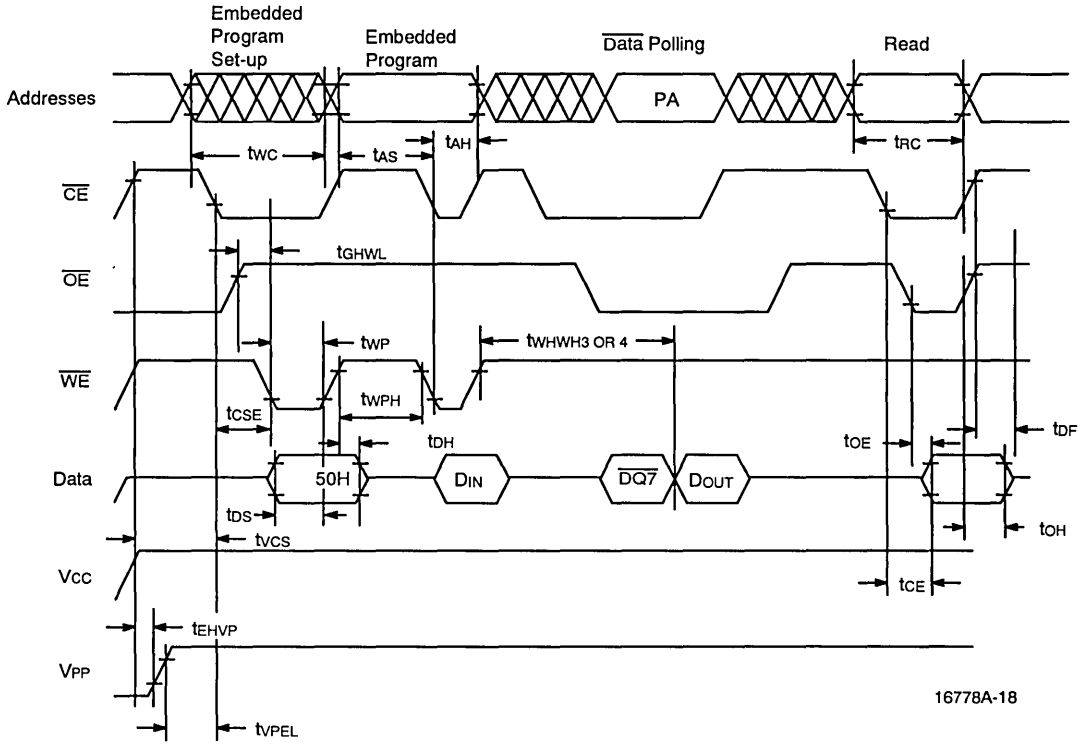


Notes:

1. D_{IN} is data input to the device.
2. $\overline{DQ7}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 11. AC Waveforms for Embedded Erase Operation

SWITCHING WAVEFORMS



Notes:

1. D_{IN} is data input to the device.
2. $\overline{DQ7}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

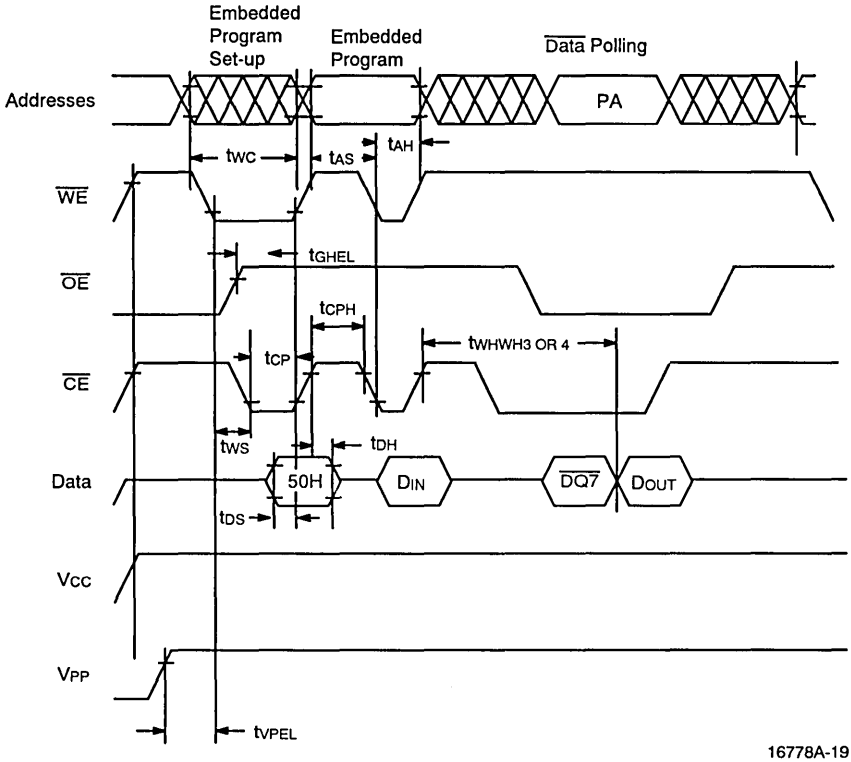
Figure 12. AC Waveforms for Embedded Programming Operation

AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 5)
Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols				Am28F010A					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min. Max.	90	120	150	200	250	ns
t_{AVEL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	75	ns
t_{DVEH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min. Max.	10	10	10	10	10	ns
t_{GHEL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{WLEL}	t_{WS}	WE Set-Up Time by $\overline{CE}$	Min. Max.	0	0	0	0	0	ns
t_{EHWK}	t_{WH}	WE Hold Time	Min. Max.	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min. Max.	65	70	80	80	80	ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	Typ. Max.	14	14	14	14	14	µs
t_{EHEH4}		Embedded Erase Operation (Note 5)	Typ. Max.	3	3	3	3	3	S
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min. Max.	100	100	100	100	100	ns

Notes:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.
2. All devices except Am28F010A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
3. Am28F010A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V
4. Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
5. Embedded erase operation of 3 sec consists of 2 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.
6. Not 100% tested.

SWITCHING WAVEFORMS

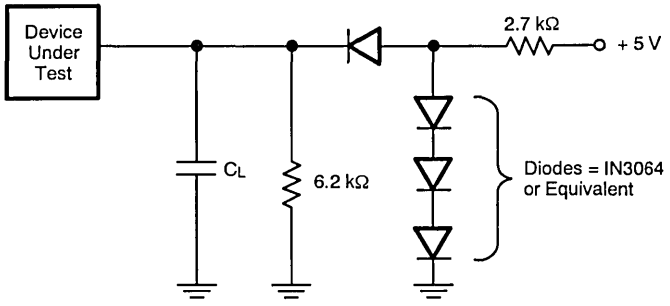


Notes:

1. D_{IN} is data input to the device.
2. $\overline{DQ7}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 13. AC Waveforms for Embedded Programming Operation Using $\overline{CE}$ Controlled Writes

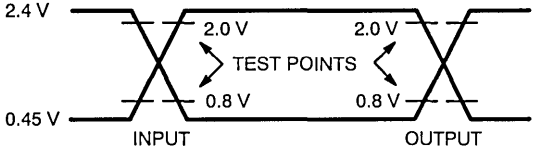
SWITCHING TEST CIRCUIT



16778A-20

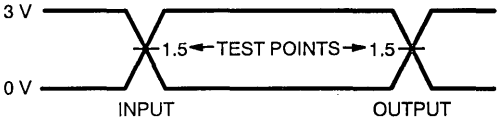
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F010A-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Input pulse rise and fall times are ≤ 10 ns.



For Am28F010A-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0." Input pulse rise and fall times are ≤ 10 ns.

16778A-21

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.[3]		
Chip Erase Time		1 (Note 1)	10 (Note 2)	S	Excludes 00H programming prior to erasure
Chip Programming Time		2 (Note 1)	12.5	S	Excludes system-level overhead
Write/Erase Cycles	100,000			Cycles	
Byte Program Time		14		µs	
			96 (Note 4)	ms	

Notes:

1. 25°C, 12 V V_{PP}
2. The Embedded algorithm allows for 60 second erase time for military temperature range operations.
3. Maximum time specified is lower than worst case. Worst case is derived from the Embedded Algorithm internal counter which allows for a maximum 6,000 pulses for both program and erase operations. Typical worst case for program and erase is significantly less than the actual device limit.
4. Typical worst case = 84 µs. DQ_5 = "1" only after a byte takes longer than 96 ms to program.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	–1.0 V	V_{CC} + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Min.	Units	Test Conditions
Min. Pattern Data Retention Time	10	Years	150°C
	20	Years	125°C

FINAL

Am28F020

262,144 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **CMOS Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **10,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ Programming**
  - 10 µs typical byte-program
  - Four seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F020 is a 2 Megabit Flash memory organized as 256K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F020 is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F020 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F020 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F020 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F020 uses a 12.0 V ±5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC} +1 V.

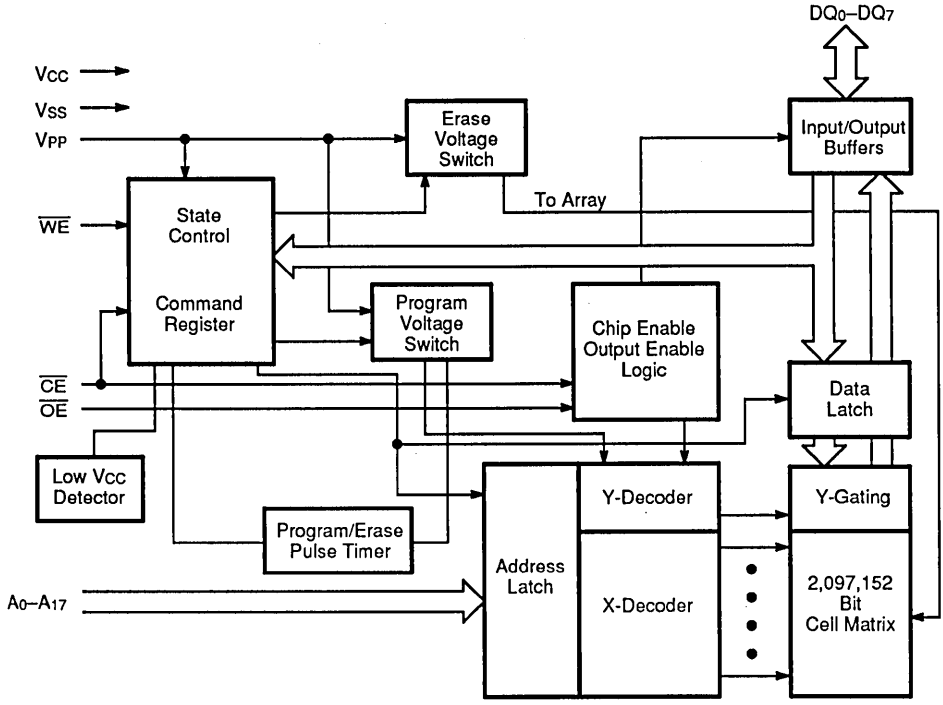
The Am28F020 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F020 is four seconds. The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase alrogithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM using ultra-violet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F020 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F020 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 14727 Rev. C Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



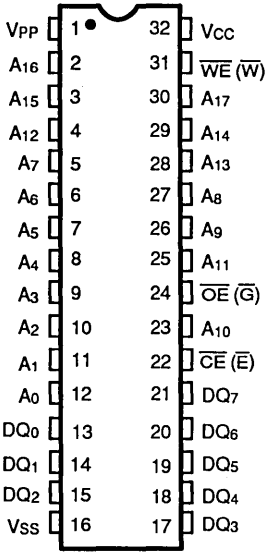
14727-001C

PRODUCT SELECTOR GUIDE

Family Part No.:	Am28F020				
Ordering part No.: ±10% VCC Tolerance	-90	-120	-150	-200	-250
±5% VCC Tolerance	-95	—	—	—	—
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	55	55	55

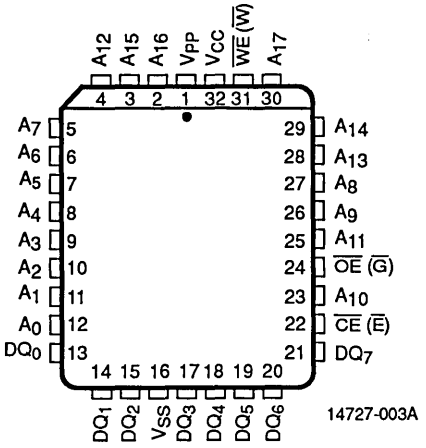
CONNECTION DIAGRAMS

DIP



14727-002A

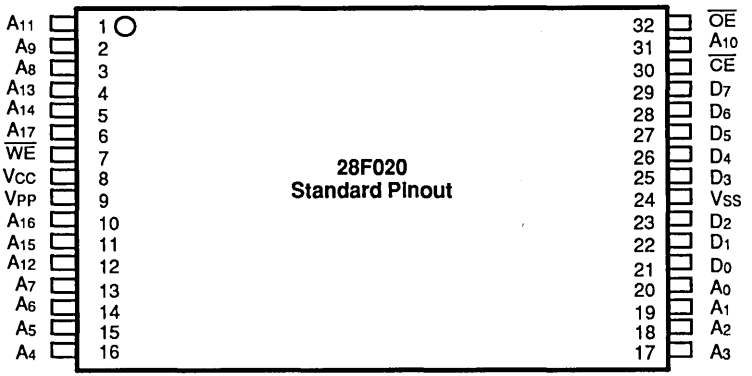
PLCC*

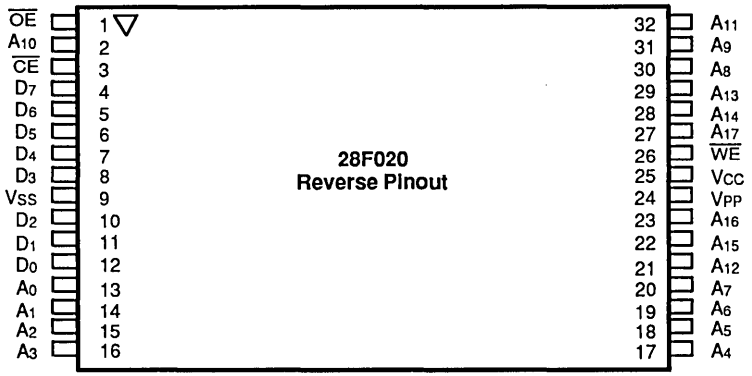


14727-003A

Note: Pin 1 is marked for orientation.
*Also available in LCC.

TSOP PACKAGES*

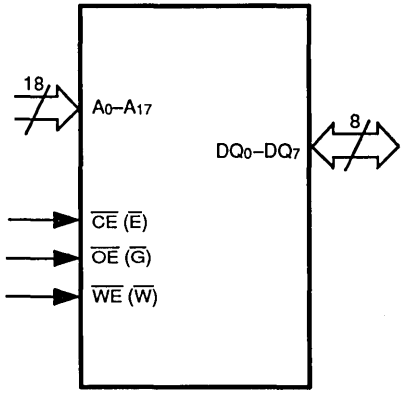




17502A-001A

28F020 256K x 8 Flash Memory in 32 Lead TSOP

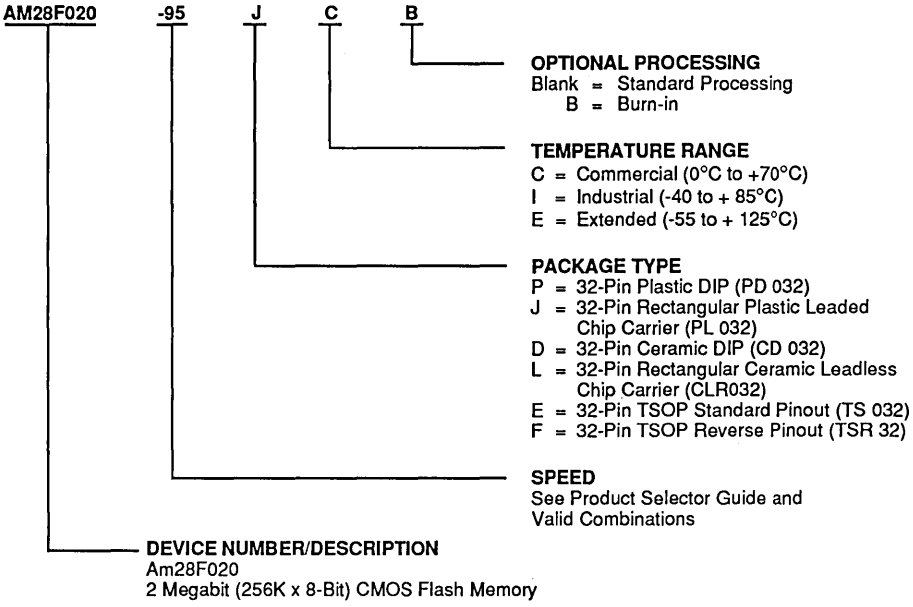
LOGIC SYMBOL



11559-004A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



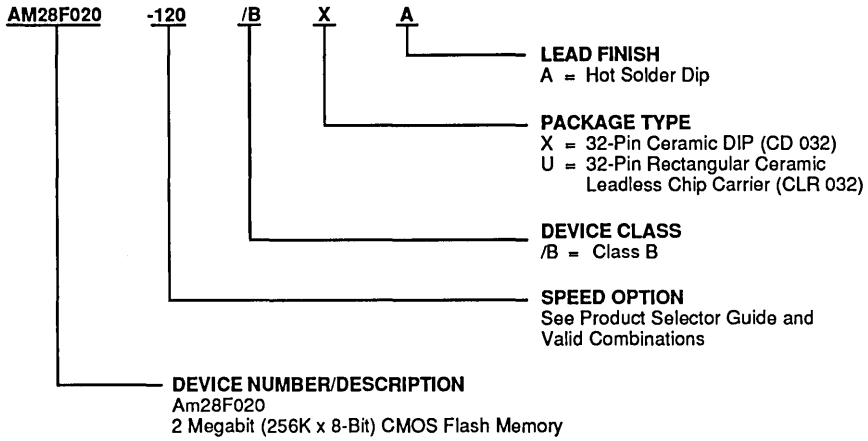
Valid Combinations	
AM28F020-90 AM28F020-95	PC, JC, DC, LC, EC, FC
AM28F020-120 AM28F020-150 AM28F020-200	PC, PI, PE, PEB, JC, JI, JE, JEB, DC, DI, DE, DEB, LC, LI, LE, LEB, EC, FC, EI, FI, EE, FE, EEB, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F020-120 AM28F020-150 AM28F020-200 AM78F020-250	/BXA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{CC}
Power supply for device operation. (5.0 V ±5% or 10%)

V_{SS}
Ground

NC
No Connect-corresponding pin is not connected internally to the die.

A_0–A_{17}
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

DQ_0–DQ_7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F020 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F020 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F020's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F020 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Flasherase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Erase Set-Up:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command. An integrated stop timer prevents any possibility of overerasure.
3. **Erase-Verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Program Set-Up:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command. An integrated stop timer prevents any possibility of overprogramming.
3. **Program-Verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Data Protection

The Am28F020 is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F020 powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F020 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (2AH)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0$ V
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V

Command Register Inactive

Read

The Am28F020 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F020 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC}-t_{OE}$).

Standby Mode

The Am28F020 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F020 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F020 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	2A	0	0	1	0	1	0	1	0

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%
Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits R_7–R_0 correspond to the data inputs DQ_7–DQ_0 (refer to Table 3). Register bits R_7–R_5 store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6 µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands (Notes 1, 2)	X	X	X	X	X	X	X	X

Notes:

1. See Table 4 Am28F020 Command Definitions.
2. X = Appropriate Data or Register Commands.

Table 4. Am28F020 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 6, 7)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/2AH
Erase Set-up/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Program Set-up/ Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 7)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6 µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
7. Please reference Reset Command section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-up is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Erase Set-up operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{pp} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:

The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-Verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F020 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Erase Set-up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

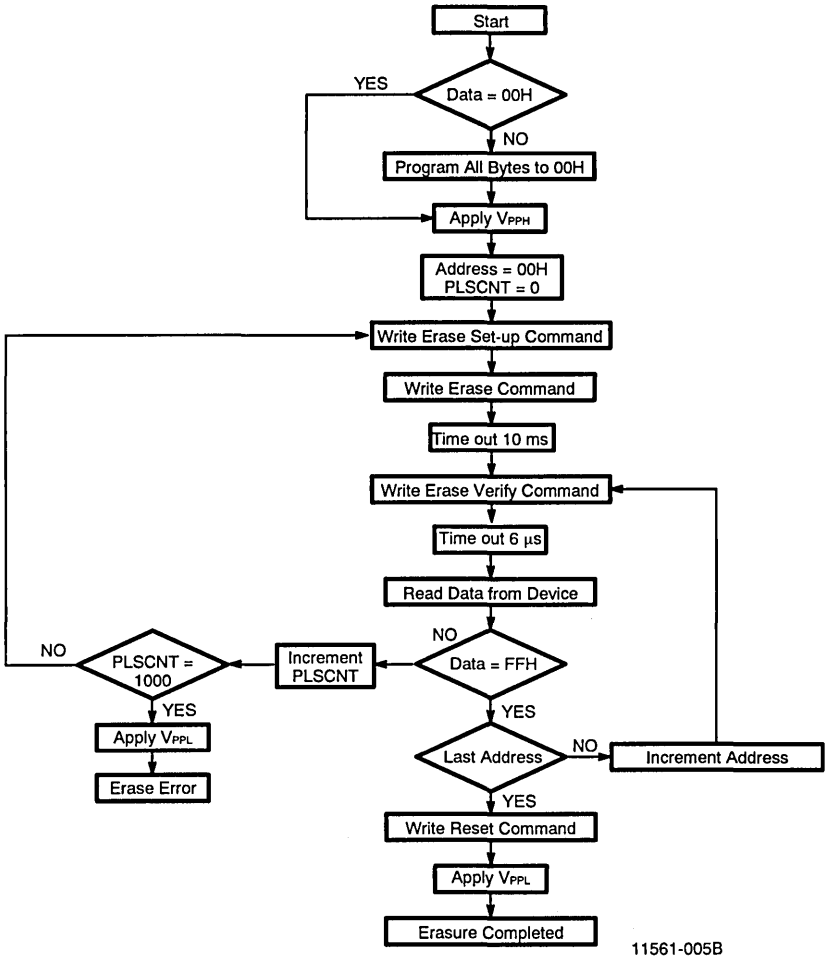


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F020 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

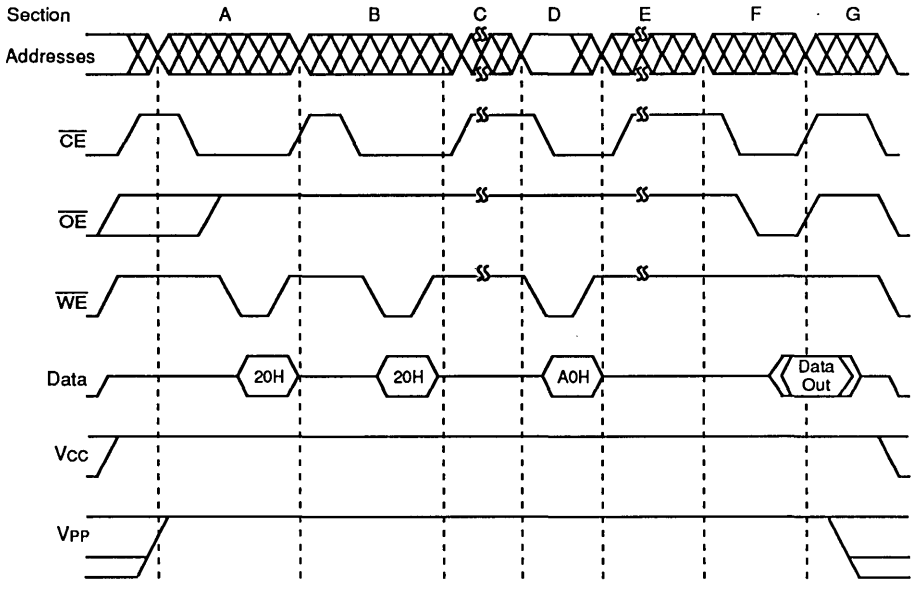
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (one second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase pulses are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 3) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-Up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Erase Set-up	Erase	Erase (10 ms)	Erase-Verify	Transition (6 µs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. A.C. Waveforms For Erase Operations

Analysis of Erase Timing Waveform

Note:
This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Erase Set-Up/Erase

This analysis illustrates the use of two-cycle erase commands (section A and B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-Out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note:

An integrated stop timer prevents any possibility of over-erasure by limiting each time-out period of 10 ms.

Erase-Verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat

sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Note:

All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The Am28F020 is programmed byte by byte. Bytes may be programmed sequentially or at random. Program Set-up is the first of a two-cycle program command. It stages the device for byte programming. The Program Set-up operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F020 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Program Set-up/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F020 Flashrite Programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite Programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

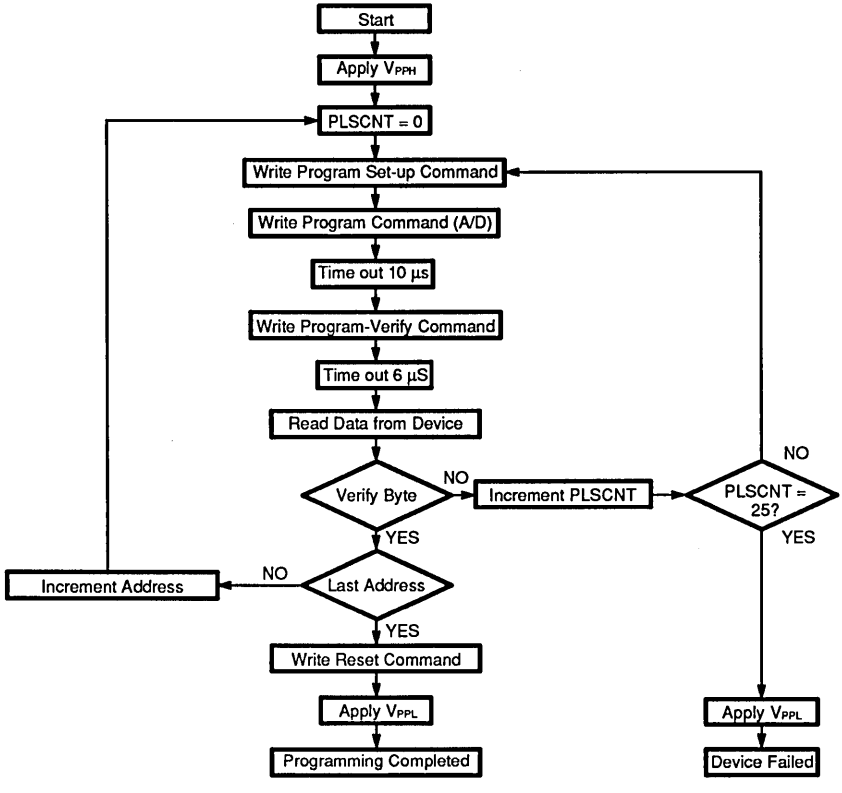


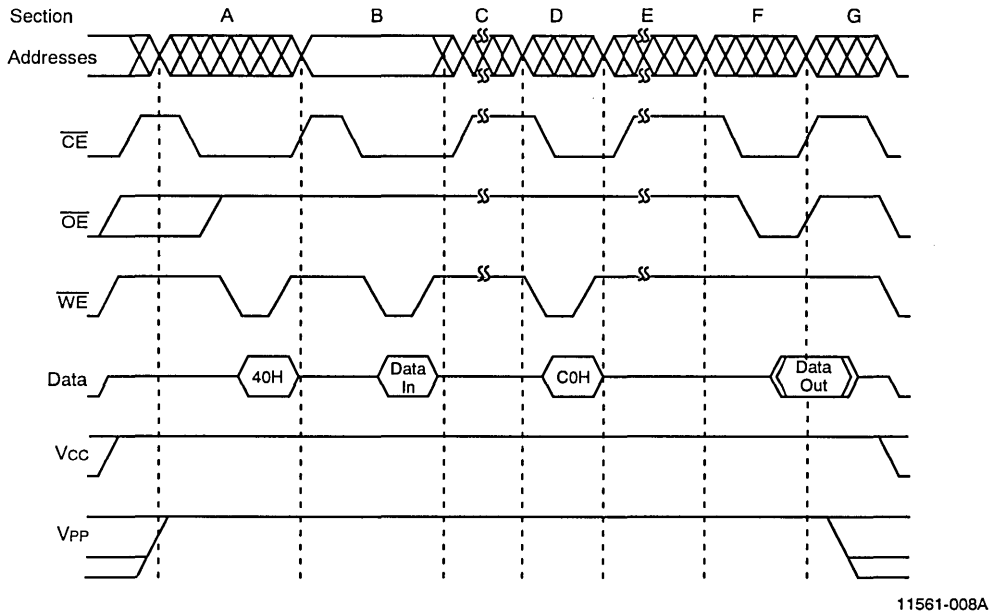
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Program Set-Up	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Standby
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Program Set-up	Program Command Latch Address & Data	Program (10 µs)	Program Verify	Transition (6 µs)	Program Verification	Proceed per Programming Algorithm

Figure 4. AC Waveforms for Programming Operations

Analysis of Program Timing Waveforms

Program Set-Up/Program

Two-cycle write commands are required for program operations (section A and B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-Out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note:

An integrated stop timer prevents any possibility of over-programming by limiting each time-out period of 10 µs.

Program-Verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1µF/device. V_{PP} must reach its final value 100 ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified separately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F020 powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F020 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 2AH (see Table 2). To terminate the operation, it is necessary to write another valid command into the register (see Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... −65°C to +150°C
Plastic Packages ..... −65°C to +125°C

Ambient Temperature
with Power Applied ..... −55°C to + 125°C

Voltage with Respect To Ground
All pins except A_9 and V_{PP} (Note 1) . −2.0 V to +7.0 V

V_{CC} (Note 1) ..... −2.0 V to +7.0 V

A_9 (Note 2) ..... −2.0 V to +14.0 V

V_{PP} (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on A_9 and V_{PP} pins is −0.5 V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) ..... −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) ..... −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) ..... −55°C to +125°C

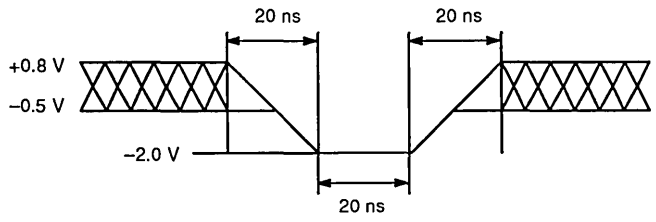
V_{CC} Supply Voltages
V_{CC} for Am28F020–X5 ..... +4.75 V to +5.25 V
V_{CC} for Am28F020–XX0 ..... +4.50 V to +5.50 V

V_{PP} Supply Voltages
Read ..... −0.5 V to +12.6 V
Program, Erase, and Verify ... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

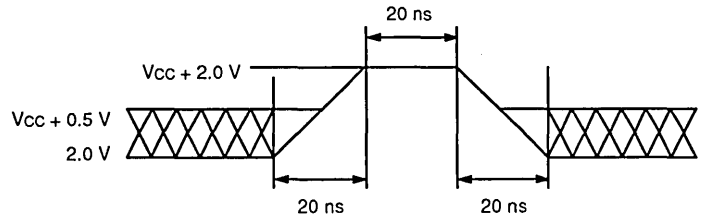
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



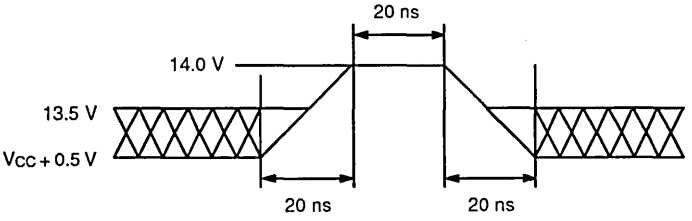
11561-009A

Maximum Positive Input Overshoot



11561-010A

Maximum V_{PP} Overshoot



11561-011A

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted) (Notes 1–3)

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
		V_{PP} = V_{PPL}			±1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4			V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. **Caution:** the Am28F020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			± 1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4			
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. **Caution:** the Am28F020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

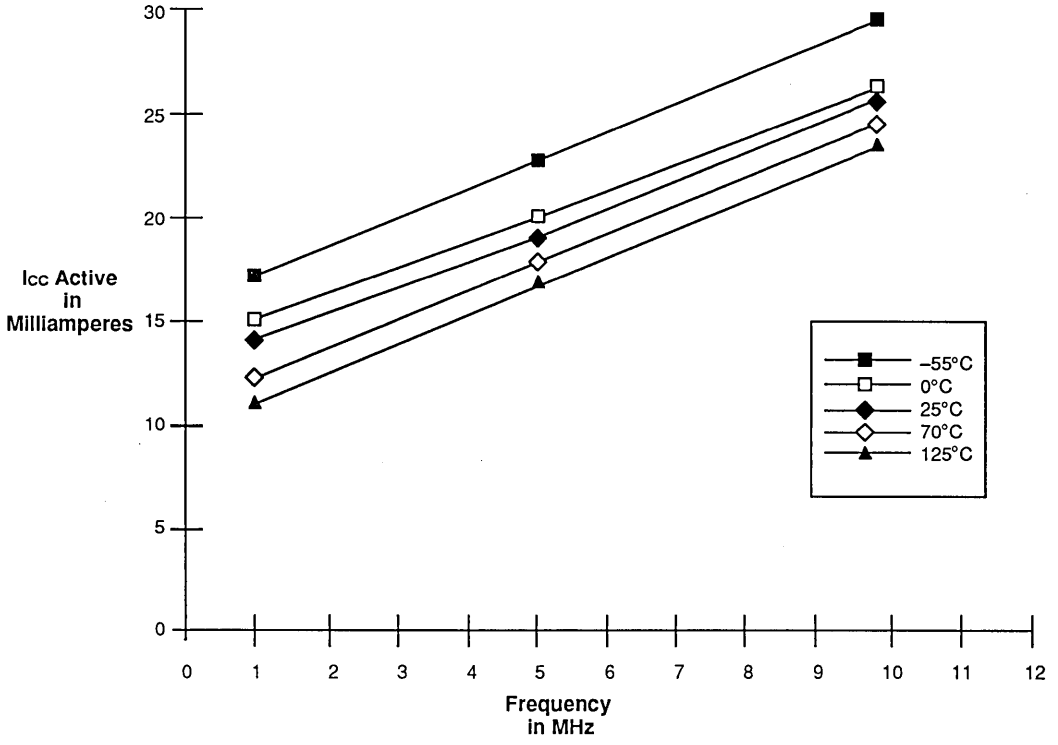


Figure 5. Am28F020–Average Icc Active vs. Frequency
Vcc = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1 and 2)

Parameter Symbols				Am28F020					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min. Max.	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min. Max.	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min. Max.	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min. Max.	50	50	50	50	50	µs

Notes:

1. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F020-95 Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. Guaranteed by design not tested.
4. Not 100% tested.

AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 5)

Parameter Symbols				Am28F020					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min. Max.	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width Max.	Min.	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation (Note 4)	Min. Max.	10	10	10	10	10	µs
t_{WHWH2}		Duration of Erase Operation(Note 4)	Min. Max.	9.5	9.5	9.5	9.5	9.5	ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 10% V_{PPL} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min. Max.	100	100	100	100	100	ns

Notes:

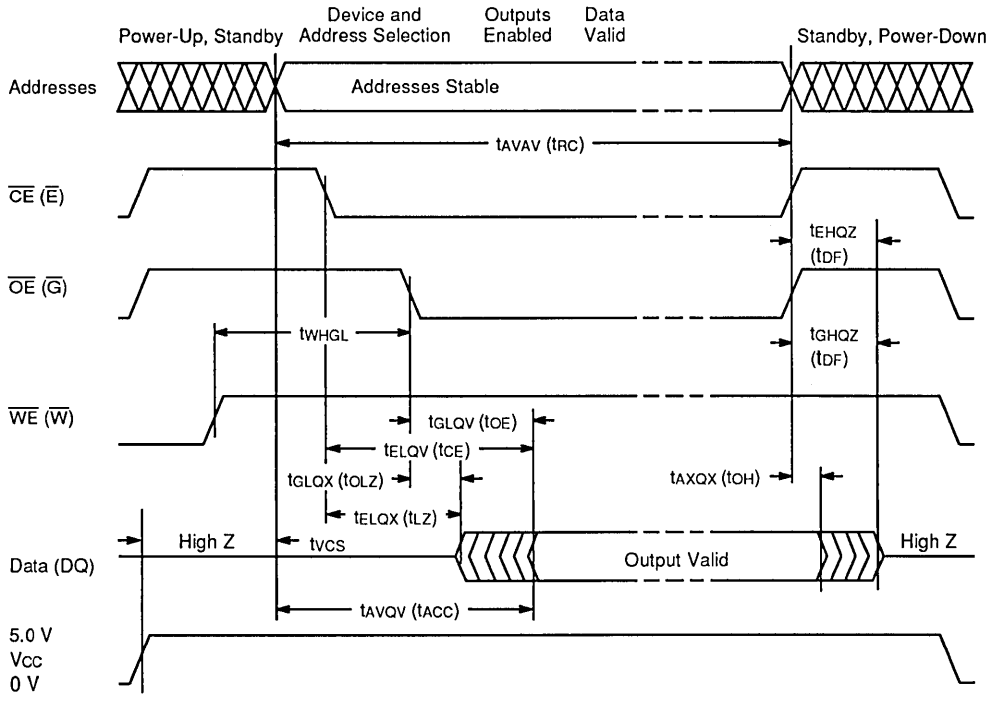
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.
2. All devices except Am28F020-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
3. Am28F020-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V
4. Maximum pulse widths not required because the on-chip program/erase stop timer will terminate the pulse widths internally on the device.
5. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
6. Not 100% tested.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



11561-013B

Figure 6. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

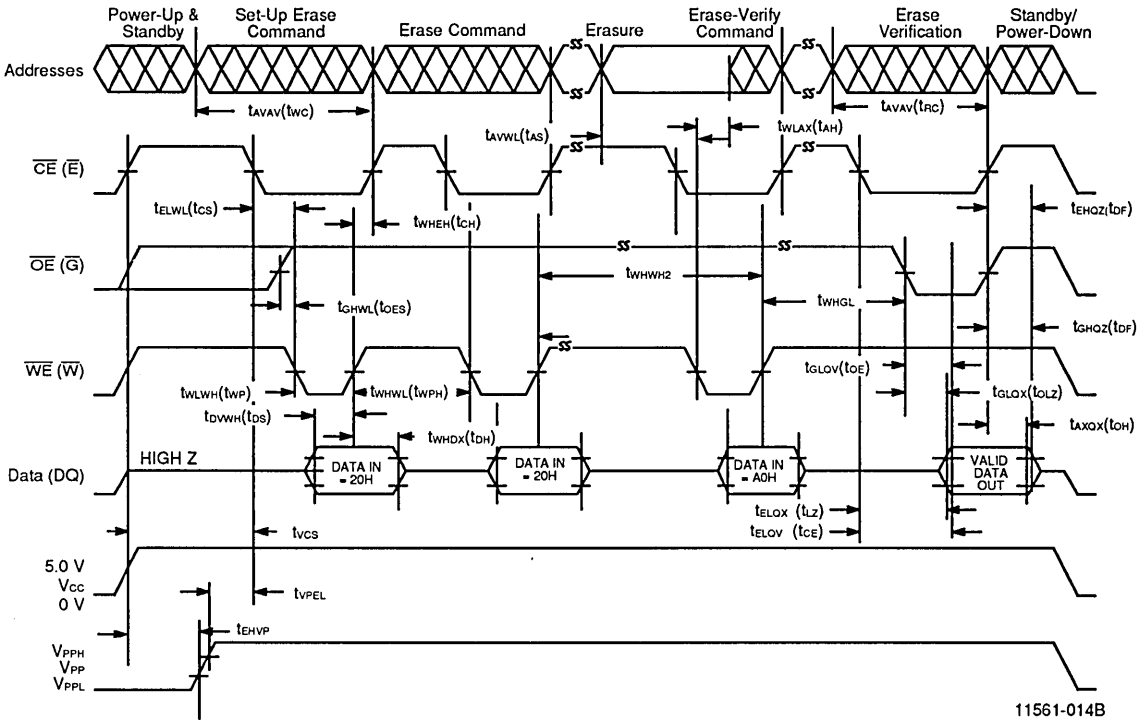


Figure 7. AC Waveforms for Erase Operations

SWITCHING WAVEFORMS

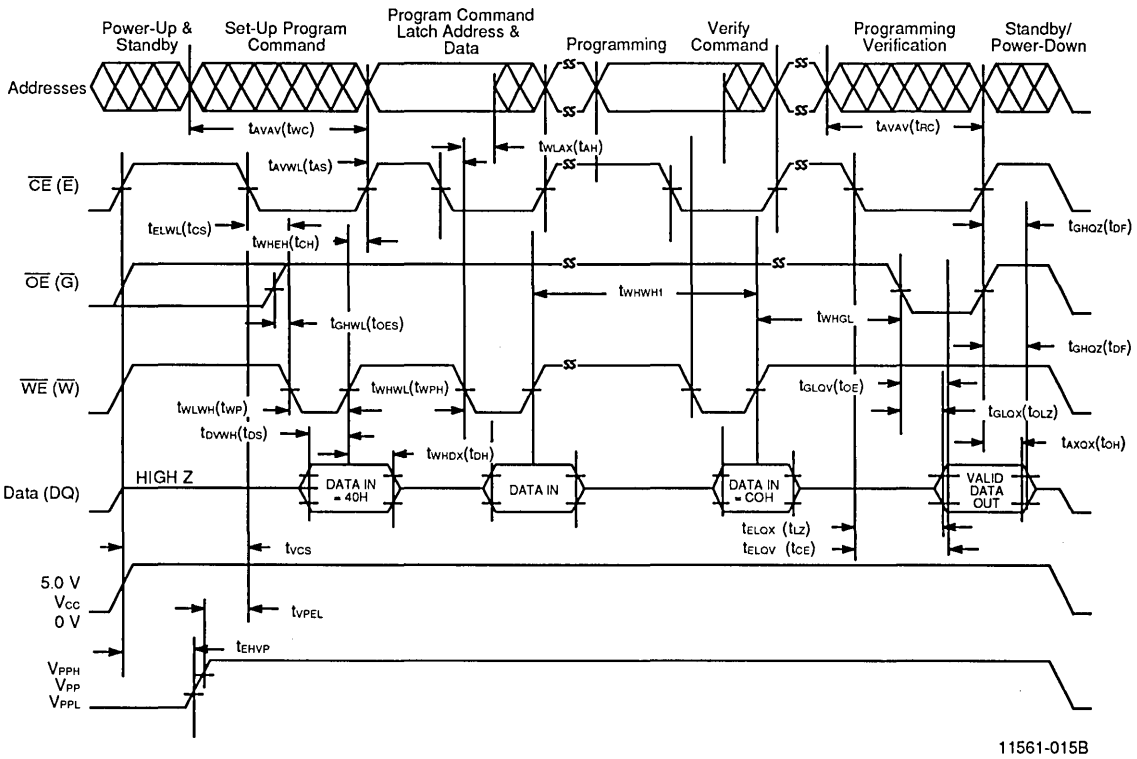
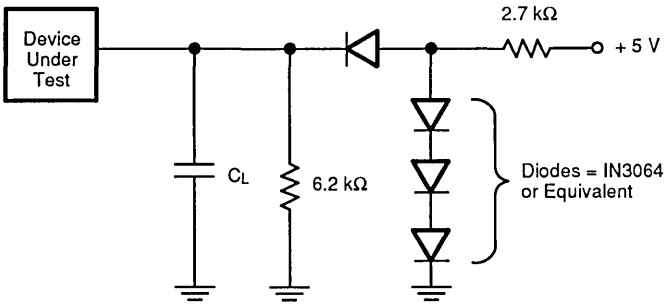


Figure 8. AC Waveforms for Programming Operations

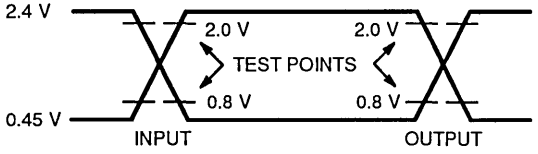
SWITCHING TEST CIRCUIT



11561-012A

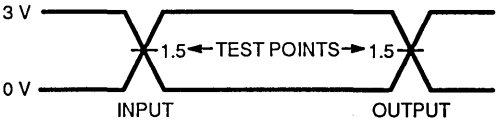
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F020-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F020-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

08007-003A

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.[3]		
Chip Erase Time		1 (Note 1)	10 (Note 2)	S	Excludes 00H programming prior to erasure
Chip Programming Time		4 (Note 1)	25	S	Excludes system-level overhead
Write/Erase Cycles	10,000			Cycles	

Notes:

1. 25°C, 12 V V_{PP}
2. The Flasherase/Flashrite algorithms allows for 60 second erase time for military temperature range operations.
3. Maximum time specified is lower than worst case. Worst case is derived from the Flasherase/Flashrite pulse count (Flasherase = 1000 max. and Flashrite = 25 max.). Typical worst case for program and erase operations is significantly less than the actual device limit.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Min.	Units	Test Conditions
Min. Pattern Data Retention Time	10	Years	150°C
	20	Years	125°C

FINAL

Am28F020A

262,144 x 8-Bit CMOS Flash Memory with Embedded Algorithms

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **CMOS low power consumption**
  - 30 mA maximum active current
  - 100 μA maximum standby current
  - No data retention power
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **100,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Embedded Erase™ Electrical Bulk Chip-Erase**
  - Five second typical chip-erase including pre-programming
- **Embedded Program™**
  - 14 μs typical byte-program including time-out
  - 4 seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Embedded algorithms for completely self-timed write/erase operations**
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F020A is a 2 Megabit Flash memory organized as 256K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non- volatile random access memory. The Am28F020A is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F020A offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F020A has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F020A uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F020A uses a 12.0 V ± 5% V_{PP} supply to perform the erase and programming functions.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC} +1 V.

Embedded Program

The Am28F020A is byte programmable using the Embedded Programming algorithm. The Embedded Programming algorithm does not require the system to time-out or verify the data programmed. The typical room temperature programming time of the Am28F020A is four seconds.

Embedded Erase

The entire chip is bulk erased using the Embedded Erase algorithm. The Embedded Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device. Typical erasure at room temperature is accomplished in one second.

AMD's Am28F020A is entirely pin and software compatible with AMD Am28F010A Flash memory.

Publication# 17502 Rev. A Amendment/0
Issue Date: September 1992

Embedded Programming Algorithm vs. Flashrite Programming Algorithm

The Flashrite Programming algorithm requires the user to write a program set-up command, a program command (program data and address), and a program verify command followed by a read and compare operation. The user is required to time the programming pulse width in order to issue the program verify command. An integrated stop timer prevents any possibility of overprogramming. Upon completion of this sequence the data is read back from the device and compared by the user with the data intended to be written; if there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 25 times.

AMD's Embedded Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, similar to $\overline{\text{data}}$ polling, provides feedback to the user as to the status of the programming operation.

Embedded Erase Algorithm vs. Flasherase Erase Algorithm

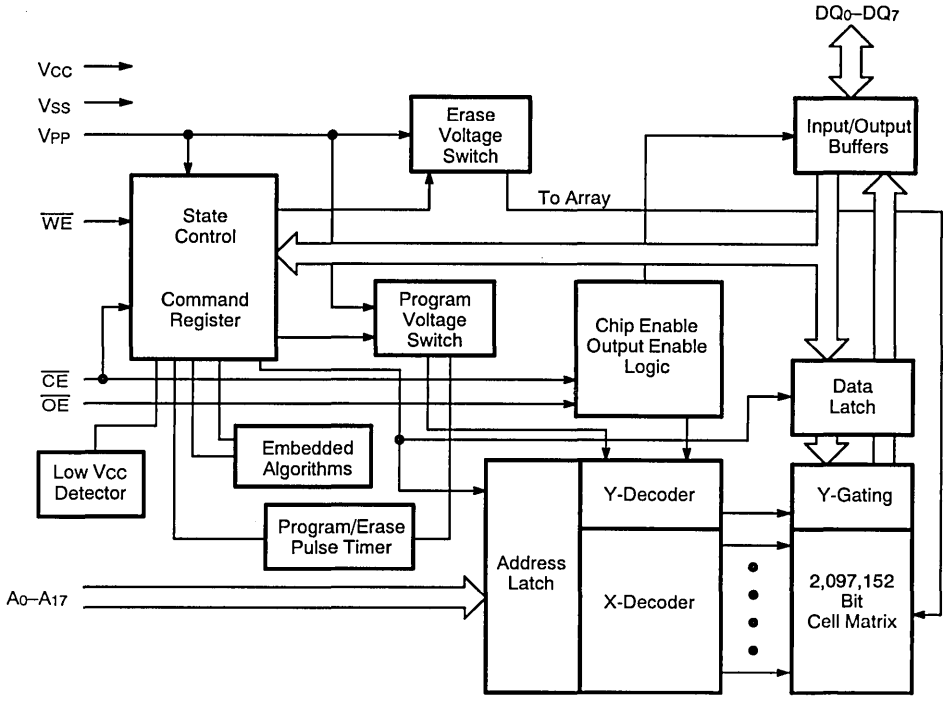
The Flasherase Erase algorithm requires the device to be completely programmed prior to executing an erase command. To invoke the erase operation the user writes an erase set-up command, an erase command, and an erase verify command. The user is required to time the erase pulse width in order to issue the erase verify command. An integrated stop timer prevents any possibility of overerasure. Upon completion of this sequence the data is read back from the device and compared by the user with erased data. If there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 6,000 times.

AMD's Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, similar to $\overline{\text{data}}$ polling, provides feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F020A is designed to support either $\overline{\text{WE}}$ or $\overline{\text{CE}}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs last. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs first. To simplify the following discussion, the $\overline{\text{WE}}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{\text{WE}}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F020A electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



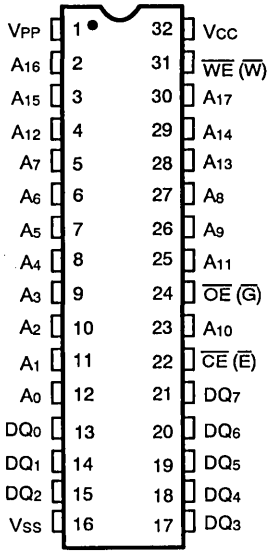
17502A-1

PRODUCT SELECTOR GUIDE

Family Part No.:	Am28F020A				
Ordering Part No.: ±10% V_{CC} Tolerance	**–90**	**–120**	**–150**	**–200**	**–250**
±5% V_{CC} Tolerance	**–95**	—	—	—	—
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	55	55	55

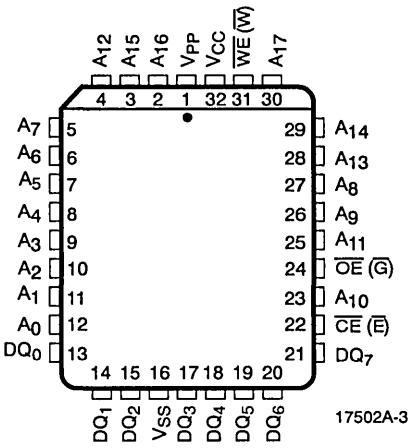
CONNECTION DIAGRAMS

DIP



17502A-2

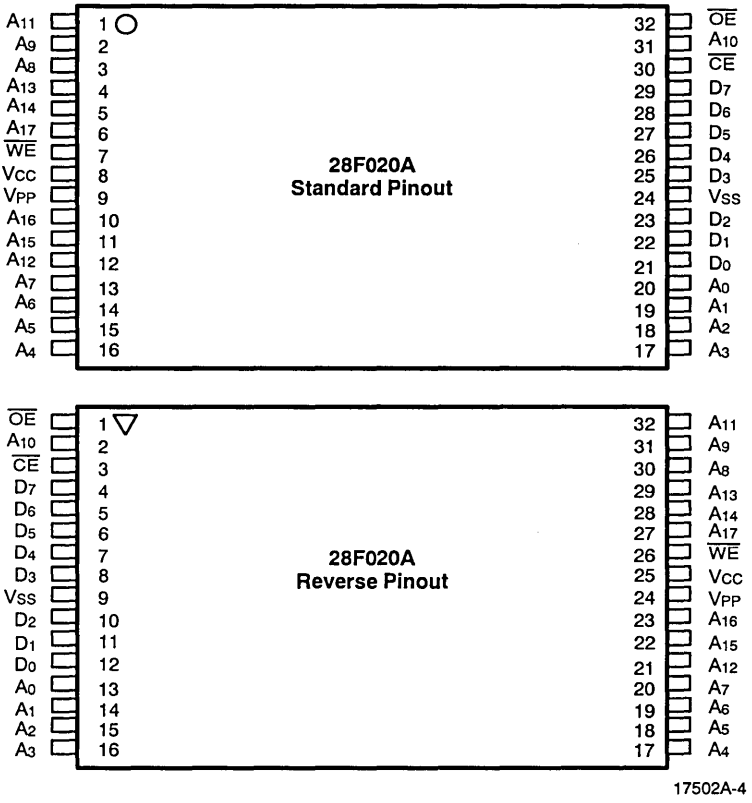
PLCC*



17502A-3

Note:
Pin 1 is marked for orientation.
*Also available in LCC.

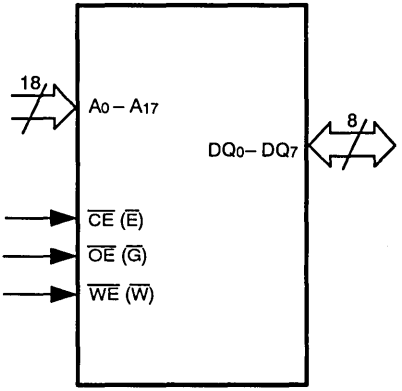
TSOP PACKAGES



17502A-4

28F020A 256K x 8 Flash Memory in 32 Lead TSOP

LOGIC SYMBOL

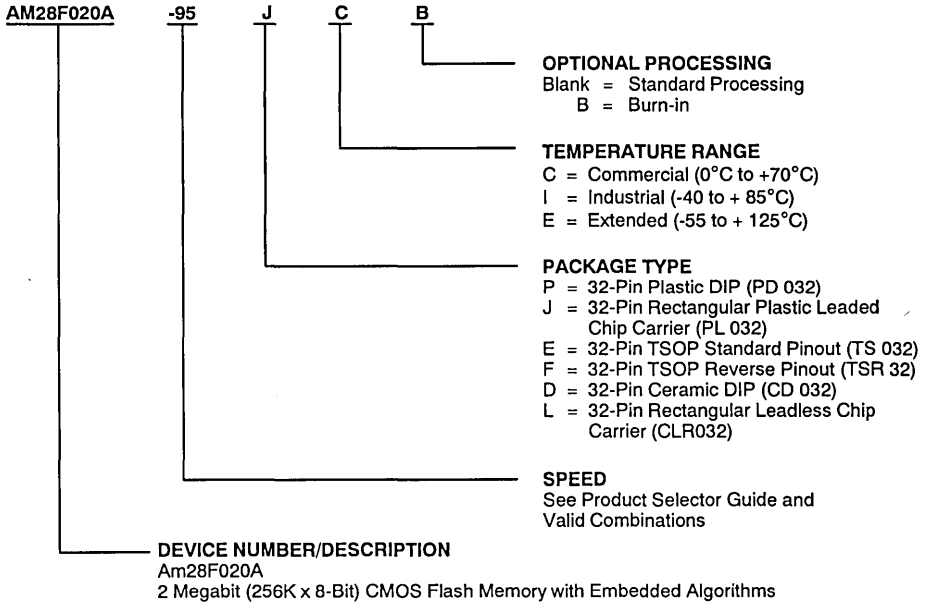


17502A-5

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F020A-90 AM28F020A-95	PC, JC, EC, FC, DC, LC
AM28F020A-120 AM28F020A-150 AM28F020A-200	PC, PI, JC, JI, PE, PEB, JE, JEB, EC, FC, EI, FI, EE, FE, EEB, FEB, DC, DI, DE, DEB, LC, LI, LE, LEB

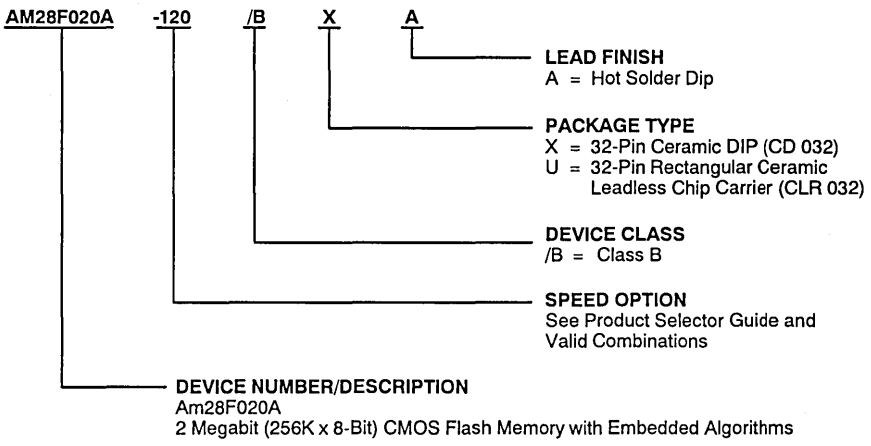
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM28F020A-120 AM28F020A-150 AM28F020A-200 AM78F020A-250	/BXA, BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

V_{PP}

Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2V$.

V_{CC}

Power supply for device operation. (5.0 V ± 5% or 10%)

V_{SS}

Ground

NC

No Connect-corresponding pin is not connected internally to the die.

A_0–A_{17}

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

DQ_0–DQ_7

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)

The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F020A uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F020A functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F020A's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F020A is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Embedded Erase Algorithm

AMD now makes erasure extremely simple and reliable. The Embedded Erase algorithm requires the user to only write and erase set-up command and erase command. The device will automatically pre-program and verify the entire array. The device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, similar to $\overline{Data}$ Polling, provides feedback to the user as to the status of the erase operation.

Embedded Programming Algorithm

AMD now makes programming extremely simple and reliable. The Embedded Programming algorithm requires the user to only write a program set-up command and a program command. The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, similar to $\overline{Data}$ Polling, provides feedback to the user as to the status of the programming operation.

Data Protection

The Am28F020A is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F020A powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. Am28F020A User Bus Operations

Operation		$\overline{CE}$ (E)	$\overline{OE}$ (G)	$\overline{WE}$ (W)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (29H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:
X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V; see DC Characteristics for voltage levels of V_{PPH}, 0V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0$ V
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V

Command Register Inactive

Read

The Am28F020A functions as a read only memory when $V_{PP} < V_{CC} + 2V$. The Am28F020A has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F020A has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5V$), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0V$ while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F020 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F020A Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	29	0	0	1	0	1	0	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%
Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits R_7–R_0 correspond to the data inputs DQ_7–DQ_0 (refer to Table 3). Register bits R_7–R_5 store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6 µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands (Notes 1, 2)	X	X	X	X	X	X	X	X

Notes:

1. See Table 4 Am28F020A Command Definitions.
2. X = Appropriate Data or Register Commands.

Table 4. Am28F020A Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 4, 5)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/29H
Embedded Erase Set-up/ Embedded Erase	Write	X	30H	Write	X	30H
Embedded Program Set-up/Embedded Program	Write	X	50H	Write	PA	PD
Reset (Note 5)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
4. Wait 6 μs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
5. Please reference Reset Command section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Embedded Program and Erase Operations

Embedded Erase Algorithm

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Embedded set-up erase command and Embedded erase command. Upon executing the Embedded erase command the device automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the device is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase Set-up command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Embedded Erase Set-up is performed by writing 30H to the command register.

To commence automatic chip erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 5 and Table 5 illustrate the Embedded Erase algorithm, a typical command string and bus operations.

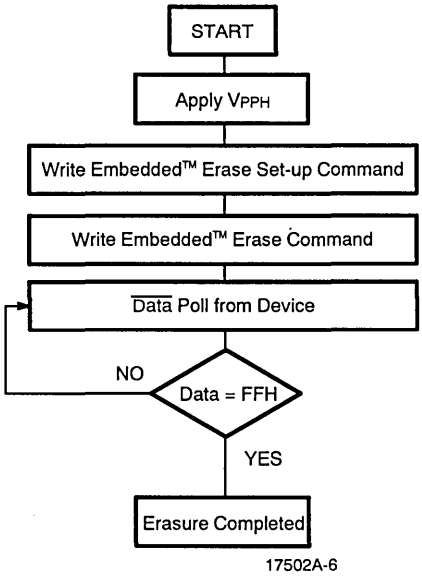


Figure 5. Embedded™ Erase Algorithm

Table 5. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation.

Embedded Programming Algorithm

The Embedded Program Set-up is a command only operation that stages the device for automatic programming. Embedded Program Set-up is performed by writing 50H to the command register.

Once the Embedded Set-up Program operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode (no program verify command is required).

Figure 6 and Table 6 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

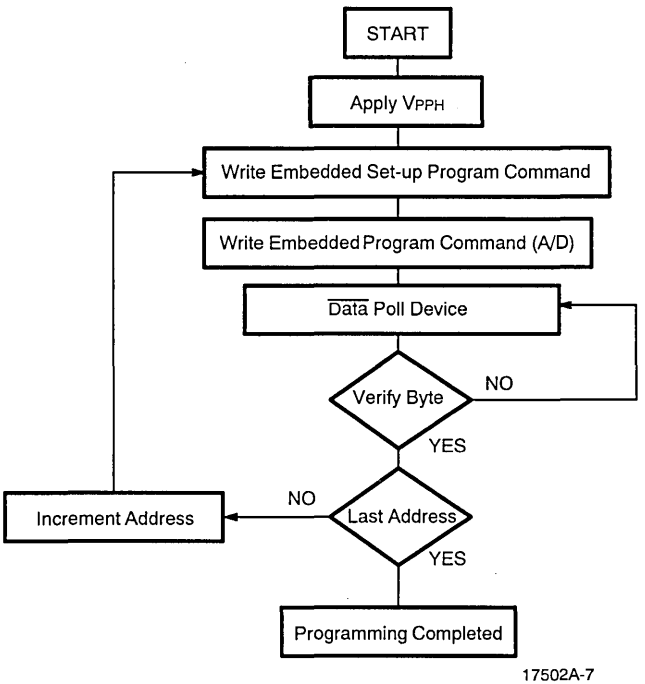


Figure 6. Embedded Programming Algorithm

Table 6. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-up Command	Data = 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{\text{Data}}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation. Device is either powered-down, erase inhibit or program inhibit.

Write Operation Status

$\overline{\text{Data}}$ Polling—DQ7

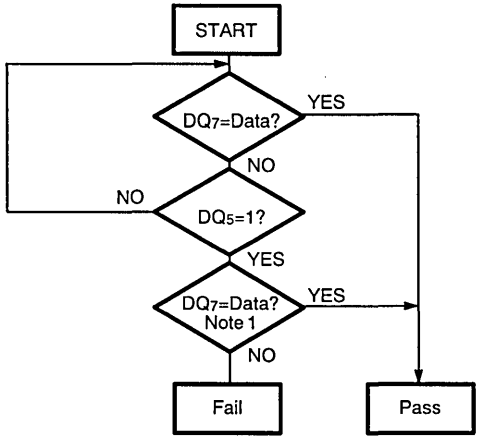
The Am28F020A features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device will produce the compliment of expected Valid data on DQ7. Upon completion of the Embedded Program algorithm an attempt to read the device will produce Valid data on DQ7. The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two Write pulse sequence.

The $\overline{\text{Data}}$ Polling feature is only active during Embedded Programming or erase algorithms.

See Figure 7a and 8a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams. $\overline{\text{Data}}$ Polling is the standard method to check the write operation status, however, an alternative method is available using Toggle Bit.



Note:

1. DQ_7 is rechecked even if DQ_5="1" because DQ_7 may change simultaneously with DQ_5 or after DQ_5.

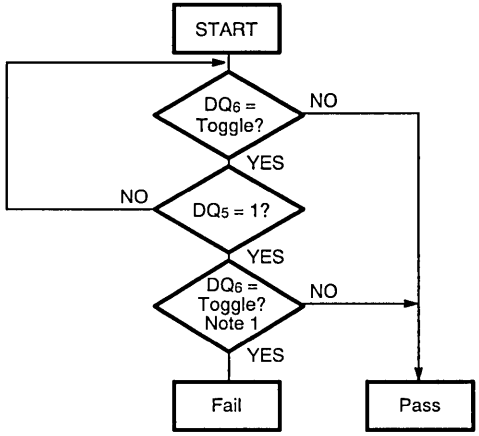
Figure 7a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Am28F020A also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the first $\overline{WE}$ pulse of the two write pulse sequence, unlike $\overline{Data}$ Polling which is valid after the rising edge of the second $\overline{WE}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

See Figures 7b and 8b for the Toggle Bit timing specifications and diagrams.



Note:

1. DQ_6 is rechecked even if DQ_5="1" because DQ_6 may stop toggling at the same time as DQ_5 changing to "1".

Figure 7b. Toggle Bit Algorithm

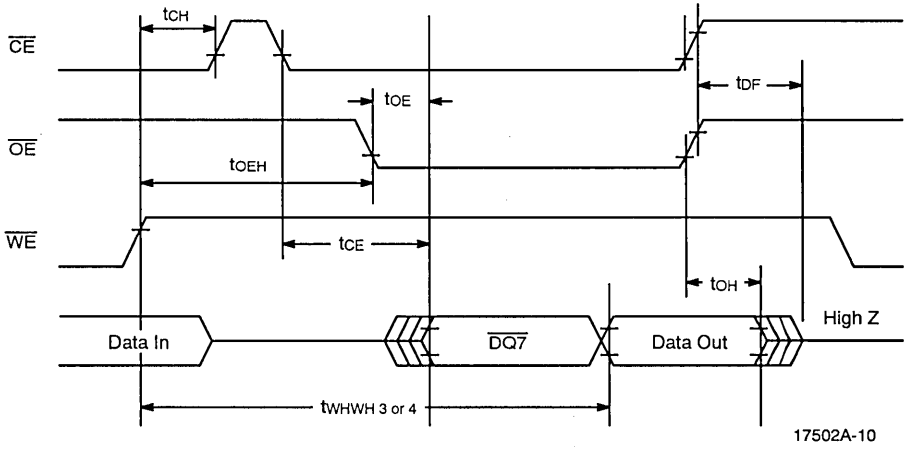


Figure 8a. AC Waveforms for $\overline{Data}$ Polling during Embedded Algorithm Operations

DQ_5
Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits. Under these conditions DQ_5 will produce a "1". The program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 1. To reset the device, write the Reset command sequence to the device.

DQ_4
Hardware Sequence Flag

If the device has exceeded the specified erase or program time and DQ5 is "1", then DQ_4 will indicate which step in the algorithm the device exceeded the limits. A "0" in DQ_4 indicates in programming, a "1" indicates an erase.

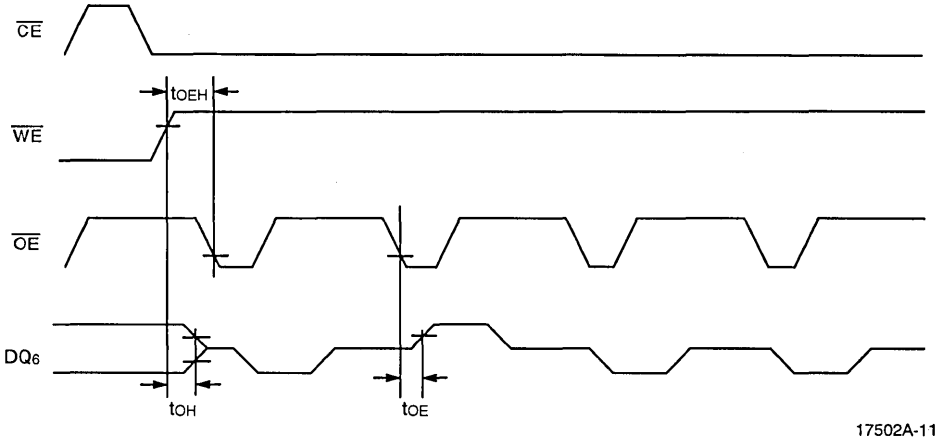


Figure 8b. AC Waveforms for Toggle Bit during Embedded Algorithm Operations

Parallel Device Erasure

The Embedded Erase algorithm greatly simplifies parallel device erasure. Since the erase process is internal to the device, a single erase command can be given to multiple devices concurrently.

This eliminates the complex design schemes otherwise required to prevent over-erasure of any one or more devices. Please reference the Parallel Device Erasure section of the Am28F020 datasheet.

Power-up Sequence

The Am28F020A powers-up in the Read only mode. Power supply sequencing is not required.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F020A contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 29 (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages ..... –65°C to +150°C
Plastic Packages ..... –65°C to +125°C

Ambient Temperature
with Power Applied ..... –55°C to + 125°C

Voltage with Respect To Ground
All pins except A_9 and V_{PP} (Note 1) . –2.0 V to +7.0 V

V_{CC} (Note 1) ..... –2.0 V to +7.0 V

A_9 (Note 2) ..... –2.0 V to +14.0 V

V_{PP} (Note 2) ..... –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) ..... 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) ..... –40°C to +85°C

Extended (E) Devices
Case Temperature (Tc) ..... –55°C to +125°C

Military (M) Devices
Case Temperature (Tc) ..... –55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F020A–X5 ..... +4.75 V to +5.25 V

V_{CC} for Am28F020A–XX0 .... +4.50 V to +5.50 V

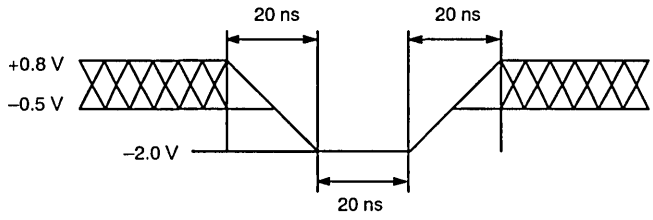
V_{PP} Supply Voltages
Read ..... –0.5 V to +12.6 V

Program, Erase, and Verify ... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

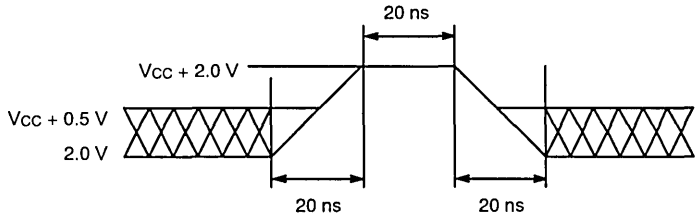
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



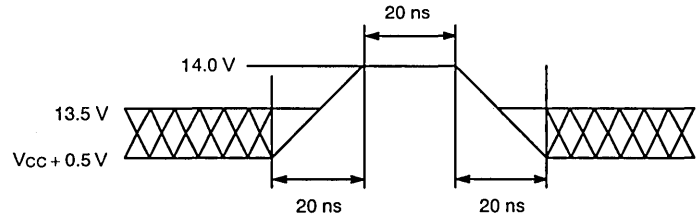
17502A-12

Maximum Positive Input Overshoot



17502A-13

Maximum V_{PP} Overshoot



17502A-14

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted) (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
		V_{PP} = V_{PPL}			±1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4			V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. **Caution:** the Am28F020A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ±0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4			
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. **Caution:** the Am28F020A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

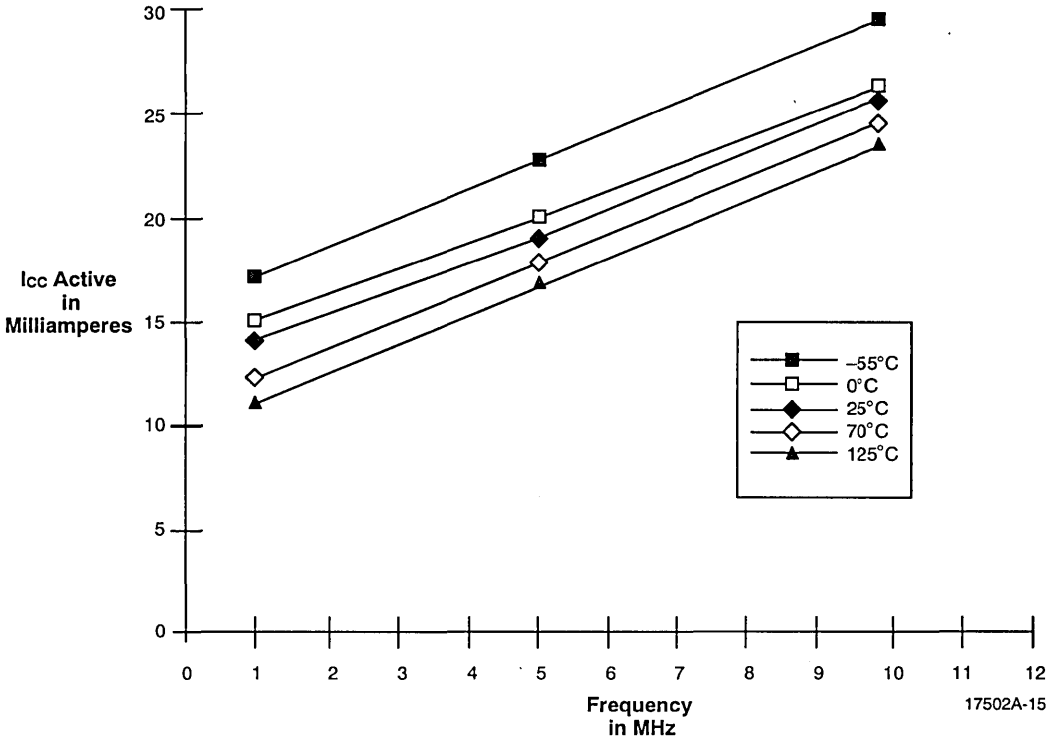


Figure 9. Am28F020A - Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1 and 2)

Parameter Symbols				Am28F020A					Unit
JEDEC	Standard	Parameter Description		-90 -95	-120 –	-150 –	-200 –	-250 –	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min. Max.	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min. Max.	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min. Max.	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min. Max.	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min. Max.	50	50	50	50	50	µs

Notes:

1. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F020A-95 Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. Guaranteed by design not tested.
4. Not 100% tested.

AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 5)

Parameter Symbols				Am28F020A					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min. Max.	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min. Max.	10	10	10	10	10	ns
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{ELWLE}	t_{CSE}	Chip Enable Embedded Algorithm Setup Time	Min. Max.	20	20	20	20	20	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width Max.	Min.	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{WHWH3}		Embedded Programming Operation (Note 4)	Typ. Max.	14	14	14	14	14	µs
t_{WHWH4}		Embedded Erase Operation (Note 5)	Typ. Max.	5	5	5	5	5	S
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min. Max.	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min. Max.	100	100	100	100	100	ns

Notes:

1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.
2. All devices except Am28F020A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
3. Am28F020A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V
4. Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
5. Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.
6. Not 100% tested.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

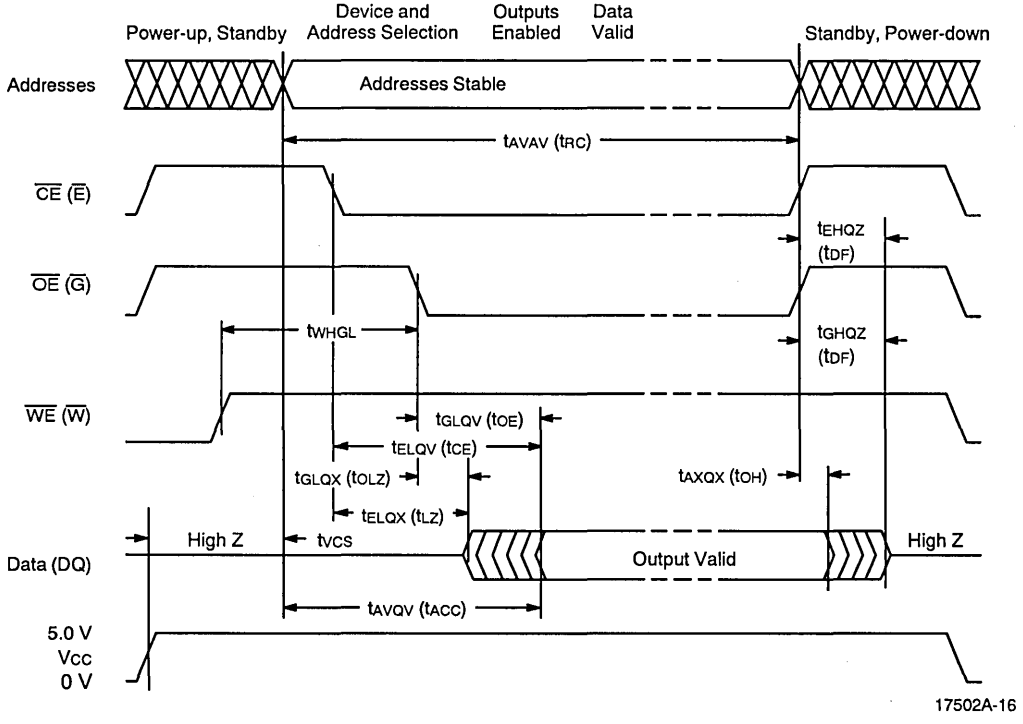
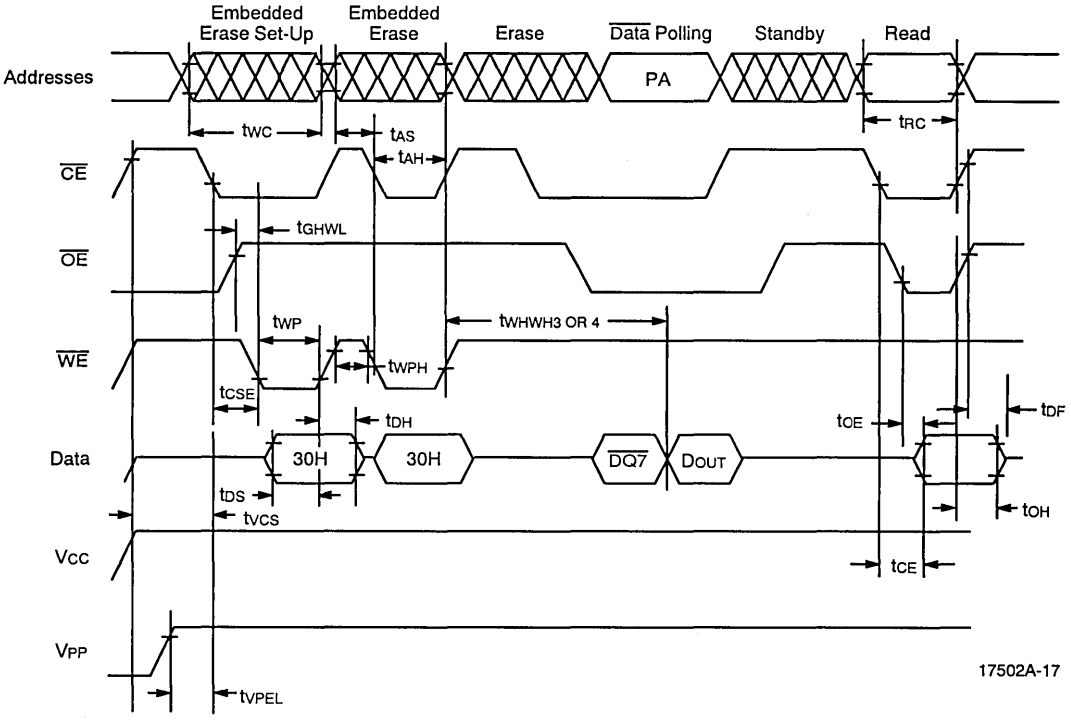


Figure 10. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

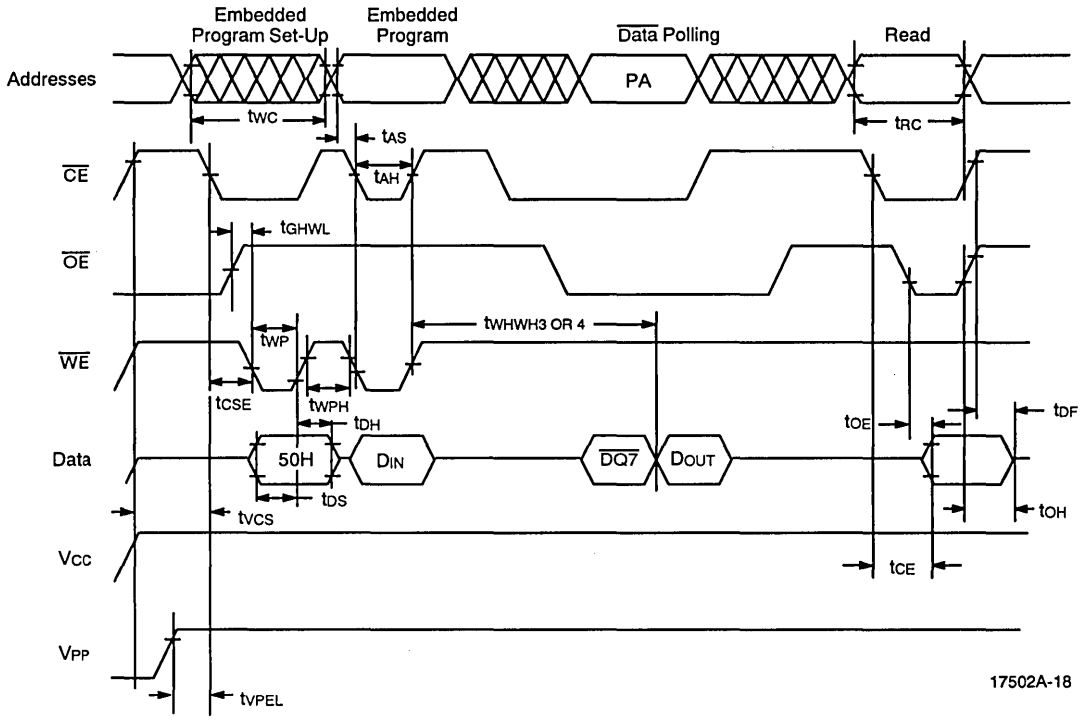


Notes:

1. D_{IN} is data input to the device.
2. $\overline{DQ7}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 11. AC Waveforms for Embedded Erase Operation

SWITCHING WAVEFORMS



Notes:

1. D_{IN} is data input to the device.
2. $\overline{DQ7}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 12. AC Waveforms for Embedded Programming Operation

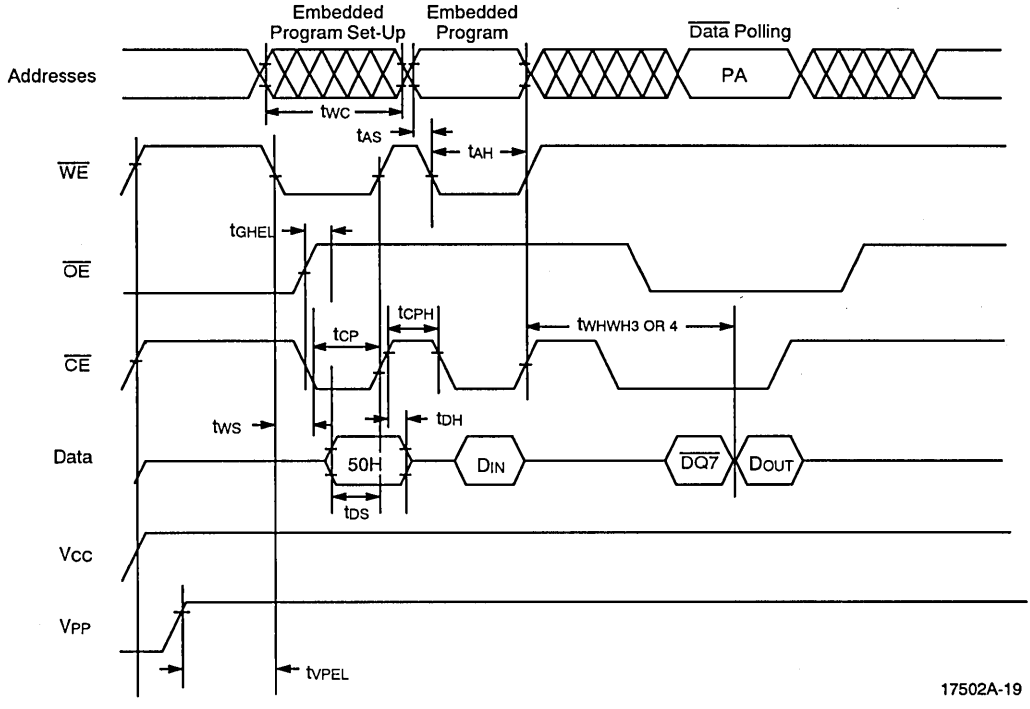
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 5)
Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols				Am28F020A					Unit
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min. Max.	90	120	150	200	250	ns
t_{AVEL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	75	ns
t_{DVEH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min. Max.	10	10	10	10	10	ns
t_{GHEL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{WLEL}	t_{WS}	WE Set-Up Time by $\overline{CE}$	Min. Max.	0	0	0	0	0	ns
t_{EHWK}	t_{WH}	WE Hold Time	Min. Max.	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min. Max.	65	70	80	80	80	ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	Typ. Max.	14	14	14	14	14	µs
t_{EHEH4}		Embedded Erase Operation (Note 5)	Typ. Max.	5	5	5	5	5	S
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Typ. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Typ. Max.	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Typ. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min. Max.	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min. Max.	100	100	100	100	100	ns

Notes:

1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.
2. All devices except Am28F020A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
3. Am28F020A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level: Inputs and Outputs: 1.5 V
4. Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
5. Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.
6. Not 100% tested.

SWITCHING WAVEFORMS

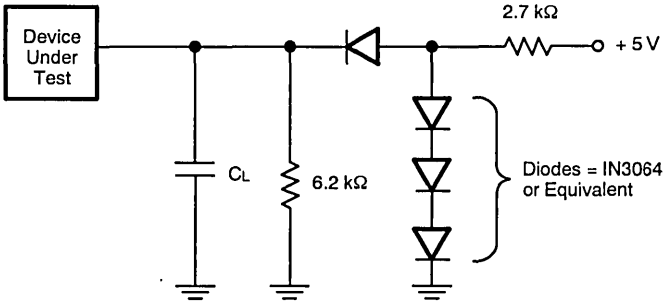


Notes:

1. D_{IN} is data input to the device.
2. $\overline{DQ7}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 13. AC Waveforms for Embedded Programming Operation Using $\overline{CE}$ Controlled Writes

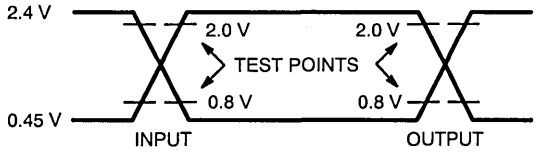
SWITCHING TEST CIRCUIT



17502A-20

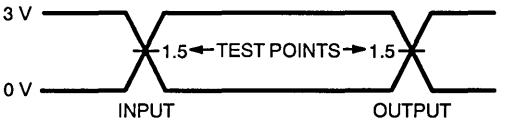
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F020A-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F020A-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

17502A-21

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.(3)		
Chip Erase Time		1 (Note 1)	10 (Note 2)	S	Excludes 00H programming prior to erasure
Chip Programming Time		4 (Note 1)	25	S	Excludes system-level overhead
Write/Erase Cycles	100,000			Cycles	
Byte Program Time		14		µs	
			96 (Note 4)	ms	

Notes:

1. 25°C, 12 V V_{PP}
2. The Embedded algorithm allows for 60 second erase time for military temperature range operations.
3. Maximum time specified is lower than worst case. Worst case is derived from the Embedded Algorithm internal counter which allows for a maximum 6000 pulses for both program and erase operations. Typical worst case for program and erase is significantly less than the actual device limit.
4. Typical worst case = 84 µs. DQ_5 = "1" only after a byte takes longer than 96 ms to program.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	–1.0 V	V_{CC} + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Min.	Units	Test Conditions
Min. Pattern Data Retention Time	10	Years	150°C
	20	Years	125°C

Embedded Algorithms In Flash Memories

Application Note
by Mike Harris

Advanced Micro Devices

Despite their instant popularity, the first 12.0 V Flash memories introduced in the late 80s had several drawbacks. One of the concerns most often voiced by system software designers was the need for cumbersome programming sequences to program and erase the devices. Embedded Algorithms were developed to eliminate these concerns.

THE DRAWBACKS OF PROGRAMMING WITH FIRST GENERATION ALGORITHMS

Figure 1 shows the flowchart for programming Flash devices using first generation algorithms. The steps needed to program a single byte of memory are illustrated in simplistic block diagram form. The programming code itself is obviously much more complex. The erase sequence is similar except Flash devices must first be programmed to all zeros prior to being erased.

A completed listing of code performing all of the program/erase functions for a Flash memory typically contains 100–200 lines. Although sample code can be obtained from the device manufacturer, designers usually need to generate their own code specific to the individuality of their application.

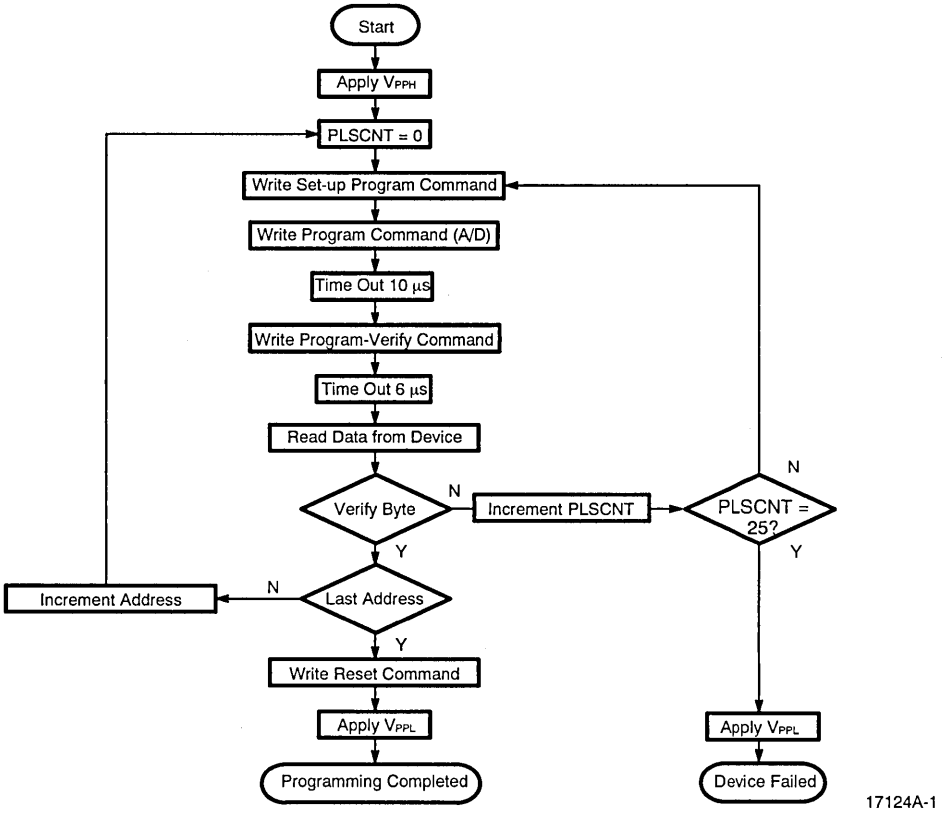


Figure 1. First Generation Programming Algorithm

This extensive programming requirement has many disadvantages and can be quite costly. First, of course, is the amount of time required to generate and debug this code. Since prior designs utilizing EPROMs were programmed offline, most software engineers are not familiar with the programming of Flash memories. They find that the programming process is initially lengthy and error prone. The cost to the user includes not only the obvious cost of software development but also the lost opportunity costs resulting from time to market delays.

Another concern is the potential long term impact on system reliability caused by overstressing a Flash device. Since cycling endurance can be affected by improper writing or erasing, software bugs can cause latent field failures even in systems that appear error free in development. In fact, most customer returns at AMD have been traced to software errors generated during system development.

SIMPLIFYING FLASH PROGRAMMING

AMD was the first company to recognize the need to simplify programming of Flash memories and incorporated it in the design of its first 2 Mbit Flash memory. Figure 2 illustrates the Embedded Program™ Algorithm. The system processor simply issues the write set-up command followed by the write command and the internal state machine on the device takes over control of the write operation. The system processor simply does $\overline{\text{DATA}}$ polling until the device indicates that the write operation is complete. This simplicity is even more pronounced during an erase operation since each byte of the memory must be individually programmed prior to erase. The Embedded Erase™ Algorithm internally writes all zeros to each byte and then performs the erase. This entire sequence is controlled internally and is transparent to the host processor.

OTHER ADVANTAGES OF EMBEDDED ALGORITHMS

Besides simplifying the complex programming of Flash memories, Embedded Algorithms offer these other important advantages to the designer:

Reduced system overhead – Since the Embedded Algorithms are completely automatic, the system processor is free to perform other functions, such as servicing interrupts, during the write or erase operations.

Improved program/erase time – The Embedded Algorithms are designed to perform write/erase operations in the most efficient way possible. All system overhead is eliminated.

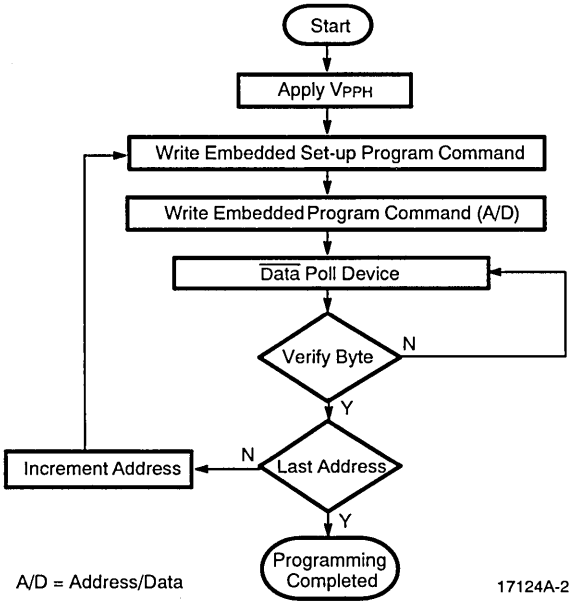


Figure 2. Embedded Programming Algorithm

Increased cycling endurance – By including a self correcting mechanism, Flash memories incorporating AMD's Embedded Algorithms will operate to a minimum of 100,000 endurance cycles.

JEDEC standards for self programming of Flash devices are now being developed. The Embedded Algorithms incorporated in all of AMD's Flash devices conform to these standards.

SUMMARY

The benefits of Embedded Algorithms are available today from AMD on first generation 12.0 V devices (Am28F010A and the Am28F020A) and well as the 5.0 V, fully sectored Am29F family. Employing these algorithms in existing designs will allow you to increase your system's endurance to over 100K cycles. In new designs, system development will be simplified and time to market reduced.

Achieving 100,000 Cycle Endurance: A Report on Flash Endurance and Reliability

Advanced Micro Devices

This article discusses the Advanced Micro Devices approach to achieving and guaranteeing superior Flash endurance. The data presented will prove that AMD's 100,000 cycle Flash devices provide the highest endurance and reliability levels in the industry.

Today's typical Flash applications are perfectly suited to 10,000 cycle endurance devices. This industry standard level of endurance is appropriate for applications such as PC BIOS and other designs that require infrequent code updates. At the same time, new Flash applications are currently being developed which require data to be reprogrammed more than 10,000 times. For applications of this sort, such as solid state hard disks, industry standard Flash devices cannot be counted on to perform reliably. AMD has revolutionized this segment of the Flash market with the new Embedded Program™ and Embedded Erase™ Algorithms, which guarantee 100,000 write/erase cycles.

What is Endurance?

Endurance is a popular term in the Flash industry. What exactly does endurance mean, and how should it be measured?

AMD defines *endurance* as the number of write/erase cycles a Flash device can withstand without failure. Endurance must be measured under the worst-case conditions of the system environment, in order to guarantee products which operate across the range of data sheet specifications.

Understanding endurance is essential for AMD, in order to manufacture superior Flash devices. Flash consumers must also understand the issues involved in achieving and guaranteeing endurance, so that they are assured of choosing the best devices on the market. In particular, consumers whose designs require extended endurance, i.e., more than 10,000 cycles, should be especially concerned with these issues.

Two failure modes are typically associated with Flash memories: hard failures and soft failures. *Hard failures* are complete and unrecoverable, and their root cause lies in the manufacturing process. Closely controlled manufacturing processes eliminate hard failures in AMD's Flash devices, increasing the level of device quality and reliability.

Flash memory endurance is typically limited by *soft failures.* Soft failures occur when random bits erase too quickly. Flash memories are erased in blocks, and since not all bits exhibit identical erase characteristics, a fast-erasing bit must be exposed to the erase voltage until the slowest bit is erased. As a result, the fast bits can be erased "too much," forcing the transistor cells into depletion mode. This condition is called *over-erase.* An over-erased bit produces a *leakage current* which causes an entire column to malfunction. The result seen by the user is a system failure.

AMD's Embedded Algorithm: The Key to Extended Endurance

The soft failures described above occur in all Flash memories. These failures are precisely the reason that today's Flash devices are currently limited to 10,000 cycles. Applications which perform more than 10,000 write/erase cycles may jeopardize system reliability if standard rated 10,000 cycle Flash devices are designed in.

Now, Advanced Micro Devices makes extended endurance Flash applications possible with the introduction of the Embedded Program and Embedded Erase Algorithms. AMD's Embedded Algorithm incorporates a function which *seeks out and corrects soft failures,* allowing these devices to be guaranteed for *100,000 write/erase cycles* (actual device performance may be orders of magnitude greater). The Embedded Algorithm extends endurance by automatically recovering over-erased bits, making soft failures transparent to the system. Flash devices that do not support these algorithms are incapable of recovering soft failures; thus, they cannot guarantee 100,000 write/erase cycle endurance. Only AMD offers this self-correcting mechanism that makes extended endurance Flash applications possible.

Failure Rate Comparison

Figure 1 illustrates AMD's significant endurance advantage over other standard rated 10,000 cycle Flash products. The graph shows that the endurance of AMD's 100,000 cycle Embedded Algorithm devices represent a significant breakthrough in Flash endurance, as illustrated by the nearly flat failure rate curve.

Publication# 17235 Rev. A Amendment/0
Issue Date: September 1992

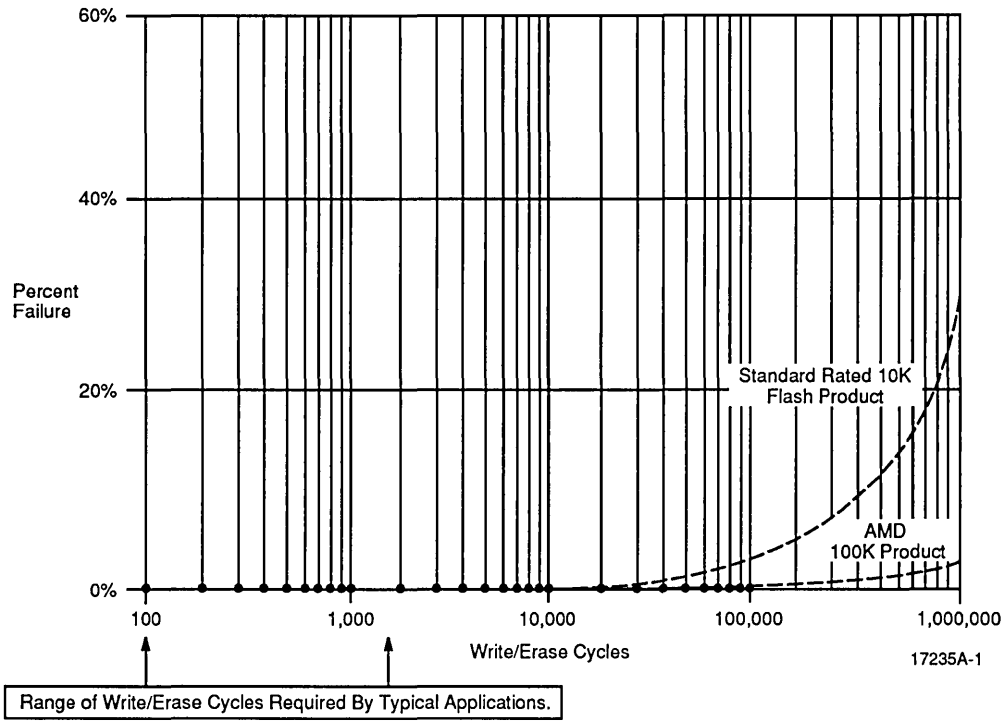


Figure 1. Failure Rate Comparison:
Standard Rated 10K Cycle Flash Product vs. AMD 100K Rated Product

AMD's Embedded Algorithm devices represent a significant technology advancement in Flash endurance.

Test results prove that AMD's Flash technology produces superior endurance. As Table 1 shows, the endurance failure rate at 100,000 cycles for AMD's Embedded Algorithm devices is less than 0.25%.

Table 1. AMD Embedded Algorithm Endurance Data

Device	No. of Lots	Qty	Failures @			
			10K	25K	50K	100K
Am28F010A	5	870	0/1159	0/445	0/445	1/445
Am28F020A	2	420	2/420	1/418	0/248	0/248

Endurance and Reliability

Endurance and reliability are equally important issues, though not exactly synonymous. Reliability refers to the absence of hard failure mechanisms, which can be eliminated during processing. AMD's Flash manufacturing processes are carefully controlled to produce products with immunity from hard failures. Endurance, as discussed earlier, relates to the occurrence of soft failures. AMD's Embedded Algorithm guarantees superior endurance by correcting soft failures in-system.

AMD understands that from a customer's perspective, all failures are unacceptable, regardless of their cause. For this reason, AMD's Flash devices combine unsurpassed reliability and endurance for protection against hard failures as well as soft failures. Reliability tests show that AMD's Flash process technology provides unmatched immunity from hard failures: *less than 10 FITs* on both High Temperature Operating Life (HTOL, 150°C, Vcc = 6.5 V) and Data Retention Bake (DRB, 150°C, unbiased) using the 60% UCL calculation at 55°C.

Reliability data also prove that AMD's unparalleled endurance is achieved without sacrificing reliability. HTOL and DRB reliability tests were performed on the same Embedded Algorithm devices that had been cycled 100,000 times. *Table 2 shows that even after 100,000 cycles, there were NO reliability failures.* Flash endurance and reliability are two distinct and important issues, and the data proves that AMD is superior in both.

Table 2a. Unbiased DRB @ 150°C after 100,000 Write/Erase Cycles

		Failures @			
Device	Qty	48 Hrs	168 Hrs	500 Hrs	1000 Hrs
Am28F010A	100	0/100	0/100	0/100	0/100

Table 2b. HTOL Reliability Results @ 6.5 V Vcc, 150°C after 100,000 Write/Erase Cycles

		Failures @			
Device	Qty	48 Hrs	168 Hrs	500 Hrs	1000 Hrs
Am28F010A	100	0/180	0/180	0/180	0/180

AMD is the technology leader in Flash memories. At the 10,000 cycle level, AMD offers devices compatible with the industry standard. At the 100,000 cycle level, AMD's Embedded Algorithm devices are unmatched in the industry, truly guaranteeing 100,000 cycle endurance.

For leadership in higher endurance, reliability, and quality in Flash memories, look to AMD: your Flash leader!

For further information, please contact your local AMD sales representative.

Generation and Control of V_{PP} Programming Voltage for Flash Memories

Application Note

Advanced Micro Devices

INTRODUCTION

Constant V_{PP} voltage of 12.0 V ±0.6 V is required for erase and programming operations. Parallel device reprogramming (either 16-bit or 32-bit data words) requires 30 mA of current for each device in the Flash memory array.

V_{PP} voltage may be generated in a number of ways. Each of these options will be discussed during the text.

1. Hardwire V_{PP} Voltage to the Flash Device.
2. Umbilical Cord Type Programming.
3. Use DC/DC Convertor to pump 5 V to V_{PP} Voltage.
4. Pump 5 V to V_{PP} Voltage with Analog Circuitry.

It is important to maintain the specified V_{PP} voltages when programming the Flash memory device. All internal device voltages are generated from the V_{PP} reference. Inappropriate V_{PP} voltage may impair device performance. Internal voltages do not exceed that of external V_{PP}.

Unlike other approaches to Flash memories, AMD's devices actually verify margin for each byte during erase and programming operations. This is accomplished during the Erase-verify and Program-verify operations respectively. During these operations, the appropriate margin-verify voltages are internally tapped off of the V_{PP} voltage via the command register and internal V_{PP} circuitry. This allows for Erase/Erase-verify and Program/Program-verify operations to be performed with static V_{CC} (5 V) and V_{PP} (12 V) voltages.

Before proceeding, a few comments regarding basic design philosophy should be mentioned. Please make note of these comments for any of the V_{PP} generation methods implemented.

V_{PP} Trace and Circuitry

Be aware that AC current is a component of DC power switching characteristics. Design the printed circuit board traces handling this current to accommodate high frequency.

Printed Circuit Board Trace Layout

Use a single ground plane to eliminate potential loops. Keep all inductive impedances at a minimum on all high current traces.

V_{PP} Regulator Circuitry Layout

Locate the V_{PP} generation circuitry as close to the Flash memory array as possible. In addition, minimize lead lengths of the network. To help prevent noise from being picked up in feedback loops, locate all resistors and capacitors as close to the V_{PP} network as possible. In order to prevent input ground loops, use separate returns for input and output capacitors.

Device Decoupling

Switching $\overline{CE}$ inputs for memory selection causes transient current peaks at the Flash device. The Flash memory devices should be decoupled with the appropriate capacitance from these transients.

- Connect 0.1 µF ceramic capacitor between V_{CC} and V_{SS} and one between V_{PP} and V_{SS}. The capacitors should be placed as close to each device as possible.
- In addition, connect 4.7 µF electrolytic capacitor between V_{CC} and V_{SS} on the memory array's power supply. Do this for each set of eight memory devices. this bulk capacitor will maintain even voltage to the memory array.

1. HARDWIRE V_{PP} VOLTAGE TO THE FLASH DEVICE

Typically this approach is used in the most cost sensitive applications. Regulated 12.0 V supplies are commonly available in many systems.

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. The Flash device automatically resets to the read mode when V_{CC} rises above 2 V. This occurs even when V_{PP} = 12 V.

Power supply sequencing is not required.

The device will only respond to the correct sequence of commands in order to change the state of the Flash memory from Read mode to any other mode. In addition, the three control pins must be in their correct state ($\overline{CE}$ = Low, $\overline{OE}$ = High and $\overline{WE}$ = Low) in order to accept a command from the data bus.

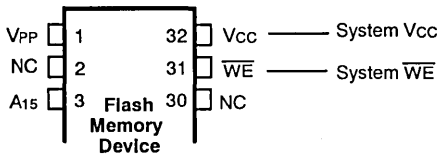
A number of additional procedures are available to further prevent inadvertent writes should system glitches occur during system/device power transitions.

- Hold any control pin ($\overline{CE}$, $\overline{OE}$, or $\overline{WE}$) in a non-write condition. This disables the device from executing any write operation (see example on the next page).
- Any "illegal" command (an illegal command is one that is not defined in the AMD Flash data sheet under the section – Command Definitions) written to the Flash device will automatically terminate any operation and reset the device to the Read Mode.

Publication# 10934 Rev. B Amendment/0
Issue Date: March 1991

Example:

Holding $\overline{WE}$ in a non-write condition during power transitions.



In systems where the V_{PP} pin is to be connected directly to the +12 V supply, $\overline{WE}$ should be held in a non-write state during power supply transitions. This will prevent against inadvertent write conditions.

During power supply transitions, V_{PP} voltage is internally disabled from the Flash device until V_{CC} rises above 2 V. In addition, the Flash device automatically resets to the read mode as V_{CC} rises above 2 V. When write enable is at V_{IH} the command register is internally disabled from the internal state machine of the Flash device. When the command register is disabled, data commands can not be transferred to the state machine. Therefore the state of the Flash device will not be altered from the read mode. Access to the command register will be prevented until the $\overline{WE}$ line is driven to a logic level low by the system write control.

Note: V_{IH} Min. = 2.0 V

2. UMBILICAL CORD PROGRAMMING

Many applications perform system updates using the umbilical cord or edge connector programming method. The external programming equipment supplies the 12.0 V ±0.6 V V_{PP} voltage. When the umbilical cord is disconnected, be aware that electrostatic discharge may build up on the floating V_{PP} pin. To prevent against this problem, tie the V_{PP} pin to ground via a large (10KΩ) pull-up resistor and a capacitor (see Figure 1).

3. V_{CC} (5.0 V) to V_{PP} (12.0 V) DC/DC Convertor

A monolithic DC/DC convertor from Valor Electronics, the PM9006, is appropriate for the digital world to supply the 12.0 V ±0.6 V V_{PP} voltage. The V_{PP} voltage is generated on chip using the standard system V_{CC} (5.0 V) voltage. Standard TTL commands are used to disable the 12.0 V output supply when programming or erasing operations are not intended. The enable ($\overline{E}$) function provides absolute write protection to guarantee against inadvertent program or erasure. Flash memory contentscannot be altered without the active 12.0 V V_{PP} supply. The enable pin also saves system power when DC/DC convertor is not required. The PM9006 has a minimum efficiency of 50% at full load. The PM9006 comes in a 24-pin package.

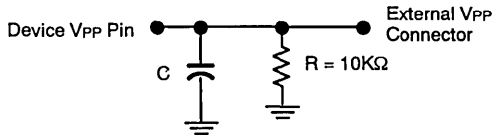


Figure 1.

The Valor PM9006 provides a controlled 12.0 V output that is regulated within the ±5% (±0.6 V) V_{PP} specification. The standard system V_{CC} (5.0 V) supply is converted to the V_{PP} (12.0 V) supply by the DC/DC convertor. The voltage transitions are smooth and protect against destructive positive or negative overshoot.

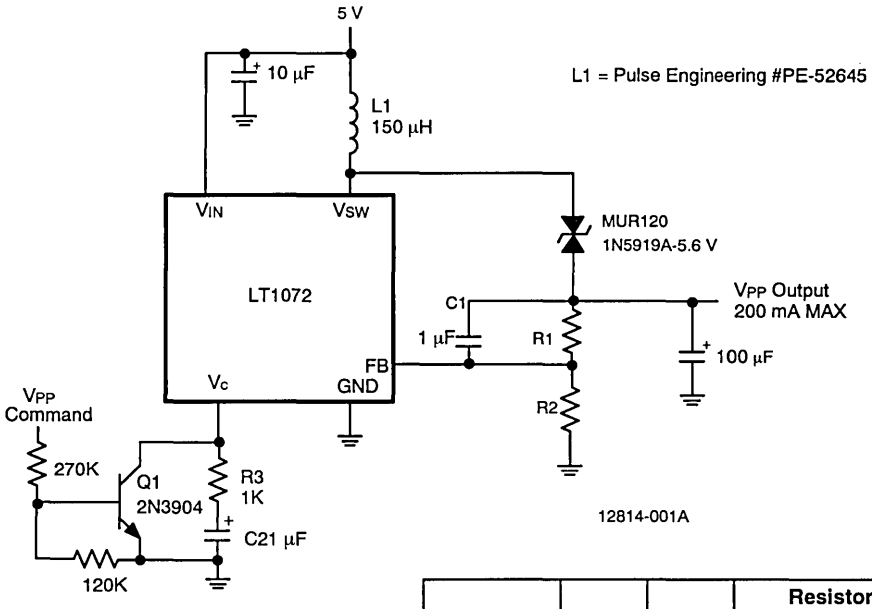
The PM9006 can supply 165 mA of current at the regulated 12.0 V ±0.6 V output. The 5.0 V ±0.5 V DC input supply of the DC/DC convertor uses a maximum of 840 mA of input current. The Am28F010 specifies a maximum V_{PP} current of 30 mA for either the erase or program operations. Actual current required for these operations is substantially lower than this. Given the maximum V_{PP} current of 30 mA for each device, four(4) Am28F010 may be programmed and erased in parallel with one PM9006 device. The PM9006 V_{PP} supply current = 165 mA – 4 x 30 mA of V_{PP} current required for the Flash memory array = 45 mA of additional current available from the DC/DC convertor.

Parallel programming and erasure allows for the most efficient method to reprogram x16 or x32-bit data words. Refer to the previous application note for parallel program and erasue flow charts.

Board Level Resets

System designs should not allow the Flash device to perform any programming or erase operations when the CPU does not have control of the Flash device. Some designs incorporate board level reset circuitry that suspends operation of the local CPU if the V_{CC} level falls below a predetermined value (such as 4.6 V). If this is the case, the reset circuitry should also disable the V_{PP} power supply whenever the CPU is held in reset.

If the local CPU is forced into reset mode while it is programming or erasing the Flash device, the system reset circuit should also terminate that operation. To accomplish this, the PM9006's enable pin should be driven high whenever the reset circuitry is active. Drive the chip enable pin of the PM9006 with the logical OR of the reset circuit's output signal and the chip enable control line to the PM9006. This will disable the V_{PP} supply and hence terminate any programming or erase operation. The Flash device automatically resets to the read mode when V_{PP} is disabled.



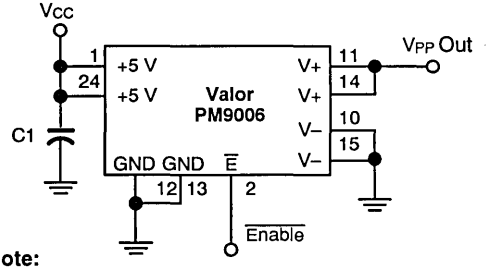
VPP Out	R1	R2	Resistor Tolerance
12.0 V	10.7K	1.24K	1%

Note:

The circuit of Figure 2 will not spuriously overshoot during power-up or power-down. This prevents destruction of the device due to voltages that exceed specification. VPP outputs are predictable and controllable during power supply transitions as a result of the referenced circuit designs. The compensation of the LT1072 causes a very overdamped pulse response. In addition, the control loops of the circuit are functioning even at low supply voltages. Thus the control loop is active before the memory circuits settle and prevents uncontrolled VPP pulse outputs.

Figure 2. Basic Flash Memory VPP Programming Voltage Supply

Please reference the PM9006 data sheet for complete details of device operation. One method of implementing the PM9006 DC/DC convertor is illustrated below.



Note:

Pins 3 through 9 and 16 through 23 are not internally connected to the device and do not need to be driven.

Generate and Control 12.0 V

4. PUMP 5 V TO VPP VOLTAGE WITH ANALOG CIRCUITRY

Flash memories require a VPP voltage of 12.0 V +0.6 V. It is important to note that VPP voltage must be maintained within the device specification for reliable operation. VPP voltages that exceed 14 V for 20 ns or longer are likely to destroy the device. Thus, we need to carefully control the high voltage programming circuitry. It should be noted that proper design of the VPP circuitry eliminates the issues of device destruction due to appli-cation of voltages outside of the specified operating range. In addition, it is preferable to control the VPP voltage with a 5.0 V logic command.

The Starter Kit: V_{PP} Generation and Control

The basic circuit described in Figure 2 satisfies just about all V_{PP} requirements for Flash memories. High voltage is produced by driving the V_{PP} command low. The low V_{PP} command (Trace A, Figure 3) activates the LT1072 switching regulator to drive L1. The resistor network of R1 and R2 provides the DC feedback. C1, R3 and C2 control the AC roll-off. Trace B illustrates the resulting V_{PP} voltage that rises smoothly to the required level. The values specified for R1 and R2 determine the12.0 V output. Leave the 5.6 V zener in the circuit in order to return the output to 0 V when the V_{PP} command goes high. When a 4.5 V minimum output is desired the zener may be omitted. Circuit trimming requirements are eliminated due to the tight internal references of the LT1072. Only precision resistors are required.

The table in Figure 4 gives additional information required to provide greater power output from the referenced circuit. The synchronous switch option of Figure 4 may replace the zener and eliminate its power dissipation.

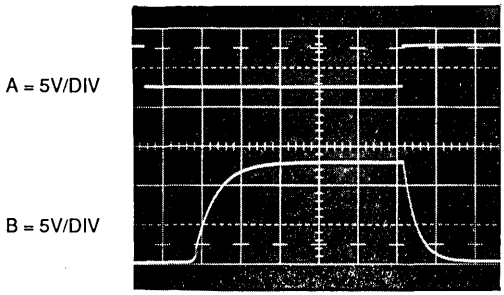
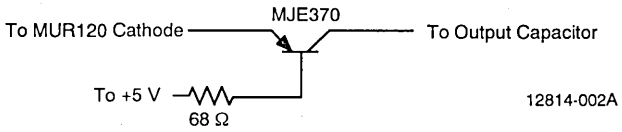


Figure 3. Waveforms for Basic Flash Programming Supply



Power Options for Basic V_{PP} Generator

Output Current	C_{OUT}	Regulator	Inductor	Zener
400 mA	200 µF	LT1071	PE-52645	1N5339A or Synchronous Switch Option
800 mA	400 µF	LT1070	PE-51516	1N5339A or Synchronous Switch Option

Note:
Assume each Flash device requires 30 mA V_{PP} current.

Figure 4. Synchronous Switch Option

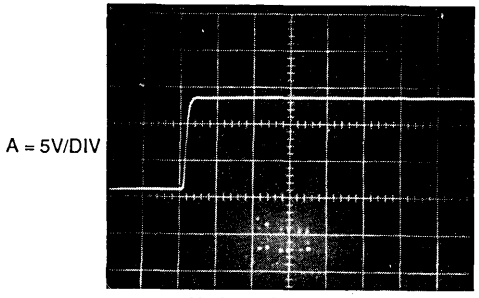


Figure B1. An "Ideal" Flash Memory V_{PP} Output

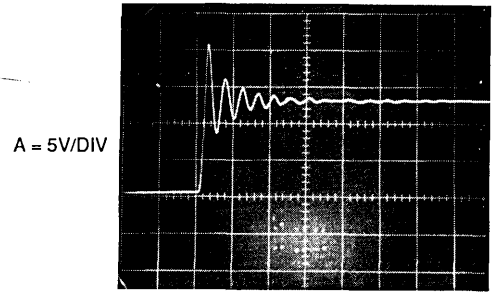


Figure B2. Rings at Destructive Voltages After a PC Trace Run

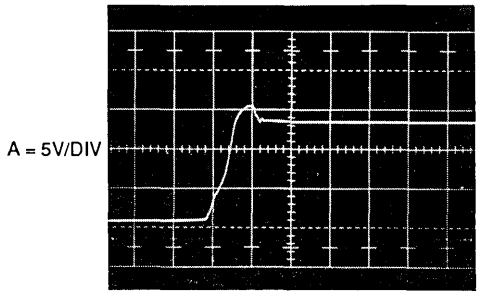


Figure B3.

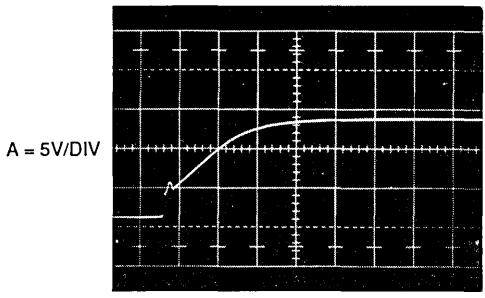


Figure B4.

Note:

Short Circuit Recovery for Poorly (Figured B3) and Properly (Figure B4) Designed Connections. Figure B3's Overshoot on Recovery Can Cause Memory Chip Failures

Transmission Line Effects of Printed Circuit Board Traces on V_{PP} Voltages

One might ask: "Why not use a simple low resistance FET to switch the output of the switching regulator when its level is correctly set?" This sounds good – too good.

In real life, the printed circuit board traces exhibit transmission line effects. Voltages seen at the memory device's pins are not the same as at the output of the regulator. Overshoots result at the junction of the printed circuit board trace and device pins. Thus voltages may exceed device specifications. This concern is compounded since the V_{PP} supply voltages are unusually close to the device's absolute maximum limit of 14 V.

Figure B1 illustrates an ideal V_{PP} pulse seen at the output of a simple low loss transistor that is switching the power supply. No overshoot is observed and the V_{PP} pulse settles quickly. The same output is measured (Figure B2) at the memory device pins after running the printed circuit board trace.

Because of mismatching, the PCB trace appears as an unterminated transmission line. Ringing can exceed 20 V because of reflections at the junction of the PC trace and device pin. This condition is obviously detrimental to the device. The negative overshoot occurring on the falling edge of the V_{PP} transition may cause equally destructive negative voltages at the device pins.

Properly controlled V_{PP} rise time prevents this type of overshoot. The closed loop circuits discussed earlier eliminate overshoot through controlled edge timings. In addition, the referenced circuits protect the V_{PP} generator against short circuit damage which also protects the memory device.

The V_{PP} output recovery when the diode is removed is shown in Figure B3. Contrast this with Figure B4. Here the diode is in place and the V_{PP} recovery is smooth. Similar considerations apply during power-up/down. During application or removal of power, the V_{PP} generator must not produce spurious output pulses.

V_{PP} outputs are predictable and controllable during transient power supply considerations as a result of the referenced circuit designs. The compensation of the LT1072 causes a very overdamped pulse response. In addition, the control loops of the circuit are functioning

even at low supply voltages. Thus the control loop is active before the memory circuits settle and prevent uncontrolled V_{PP} pulse outputs.

Note:

The above circuitry is designed for maximum system protection. Should you desire to modify any circuity, it is advisable to contact Jim Williams of Linear Technology.

This Document was adapted from Linear Technology's Application Note 31 "Linear Circuits for Digital Sytems: Some Affable Analogs for Digital Devotees," written by Jim Williams, February, 1989.

THIN SMALL OUTLINE PACKAGE

THIN SMALL OUTLINE PACKAGE (TSOP) DESCRIPTION

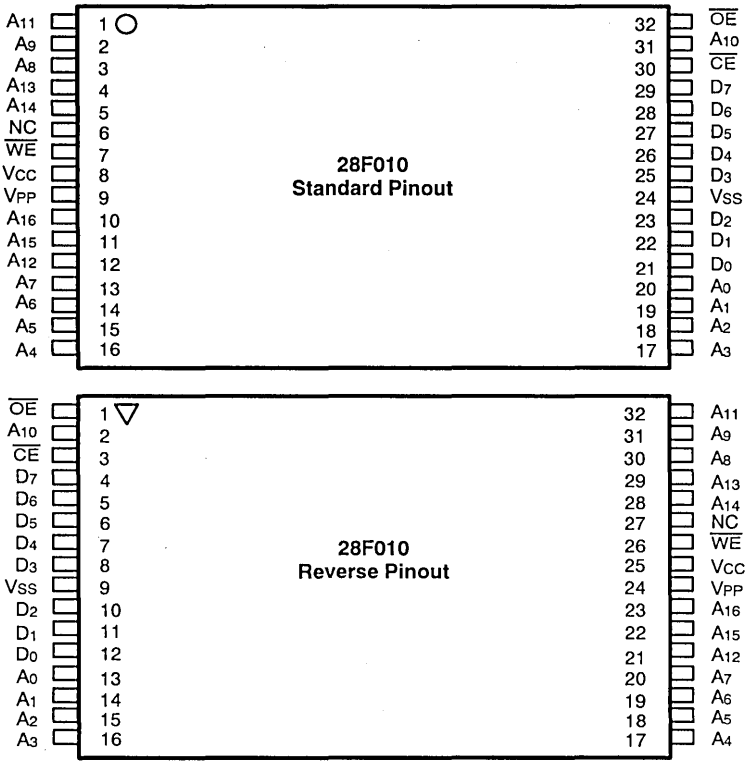
AMD presents the Thin Small Outline Package. The TSOP is the industry's leading edge plastic, surface mountable memory package today. System requirements for higher density and smaller form fit memory arrays are driving this package evolution. TSOP offers a form fit close to that of bare die yet provides the added benefit of being shipped from the factory completely tested, something not available with bare die. This increases system yield because there is no loss due to cleanroom assembly related defects and/or parametric failures.

Primary Characteristics

- JEDEC/EIAJ standard dimensions and 32-pin pinout
- Standard and reverse pinout options
- Maximum package thickness of 1.20 mm

This is AMD's initial offering in state of the art small form fit packaging. The 32-pin package is available in the 8 mm x 20 mm x 1.20 mm package outline. As densities increase, package leadcount will also.

Figure 1-1 28F010 128K x 8 Flash Memory in 32 Lead TSOP



Packaging Evolution

The continuing trend toward smaller systems and/or higher density memory arrays has led to a significant evolution in newer small form fit packaging. This trend is outlined below.

Computers:	Desktop	Notebook	Palmtop
Disk drives:	3–1/2″	2–1/2″/Flash "Disk"	Flash "Disk"
Instrumentation:	Benchtop	Portable	Handheld

Package Type	Package Volume (cubic inches)
PDIP (100 mil Pitch)	0.18
Slim DIP (100 mil Pitch)	0.09
ZIP (100 mil Pitch)	0.072
SOIC/SOJ (50 mil Pitch)	0.075
PLCC (50 mil Pitch)	0.045
TSOP (20 mil Pitch)	0.01

The TSOP is not only suited for standard printed circuit board and Single In-line Memory Module (SIMM) applications, but is the package of choice in the exploding new growth area of solid state memory cards.

TSOP packaging is well suited to high density, small form fit systems. This latest evolution offers significant packaging volume savings in comparison with the above alternatives. Increasingly, TSOP is being used in disk drive controller boards, notebook and palm top PCs, high density memory subsystems, and PCMCIA 68-pin standard memory cards. This is just the beginning.

An emerging market segment with explosive growth is the PCMCIA 68-pin memory card standard. The TSOP can be used to pack both sides of a memory board in order to increase the memory density available within a given space constraint. In addition, the TSOP packaged devices are tested to AMD's standard test flows. This allows AMD to guarantee the highest level of quality and long term reliability.

Minimal Space Requirements

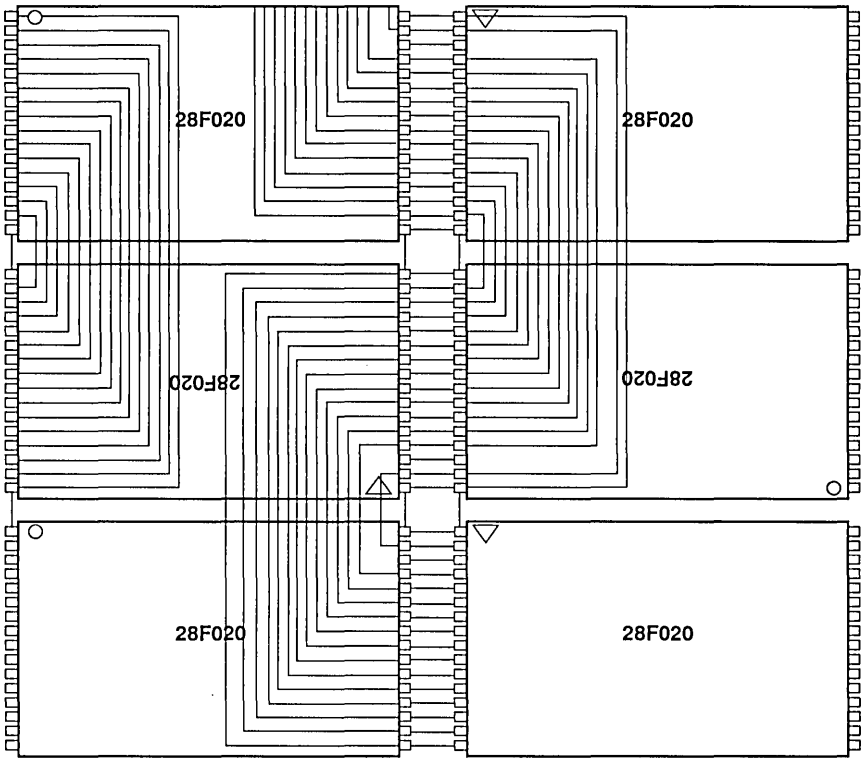
In addition to the TSOP's low height profile, maximum board space saving is achieved with the dual-in-line and standard/reverse pinouts. Board layers can be reduced because traces are routed under the two sides of the package that do not have leads. This allows packages to be mounted side by side and end to end. Packages can be mounted end to end because AMD offers both standard and mirror image reverse pinout packages (see Figures 1–1). All pins except chip enable pins can be connected in parallel. This is accomplished by using standard and reverse pinout packages in an alternating sequence as in Figures 1–1.

HANDLING AND SHIPPING

Shipping Trays

AMD's 32-pin TSOP are shipped in high temperature resistance trays (max. 150°C) having 156 positions per tray. The trays are in compliance with standard JEDEC outlines. JEDEC trays all have the same outside dimensions for easy stacking for use in manufacturing and storage. Trays are designed to prevent TSOP leads from touching any part of the holding tub.

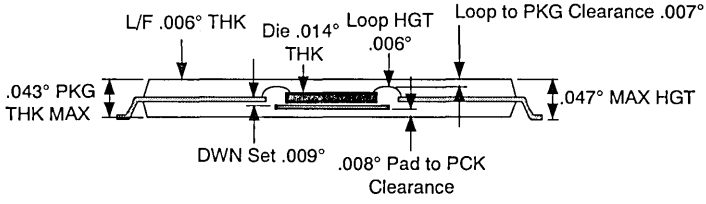
Figure 1-2 OPTIMAL BOARD LAYOUT WITH TSOP



○ = Pin 1 indicator for standard bend pinout

△ = Pin 1 indicator for reverse bend pinout

TSOP Cross-Section



SECTION

3 FLASH MEMORY PC CARDS

PRELIMINARY

AmC001FLKA

1 Megabyte Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 250 ns maximum access time
- **CMOS low power consumption**
  - 25 mA typical active current (X8)
  - 400 μA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **High re-programmable endurance**
  - Minimum 10,000 write/erase cycles
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate attribute memory**
  - 512 byte EEPROM
- **Flashrite™ and Flasherase™ Operations**
  - 128K byte memory segment
  - Typically 1 second per single memory segment erase
  - Random address writes to previously erased Bytes (10 μs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Read voltage, 5 V ± 5%**
- **Write and erase voltage, 12.0 V ± 5%**
- **Insertion and removal force**
  - State of art connector allows for minimum card insertion and removal effort
- **Manufactured by DuPont Connector Systems**

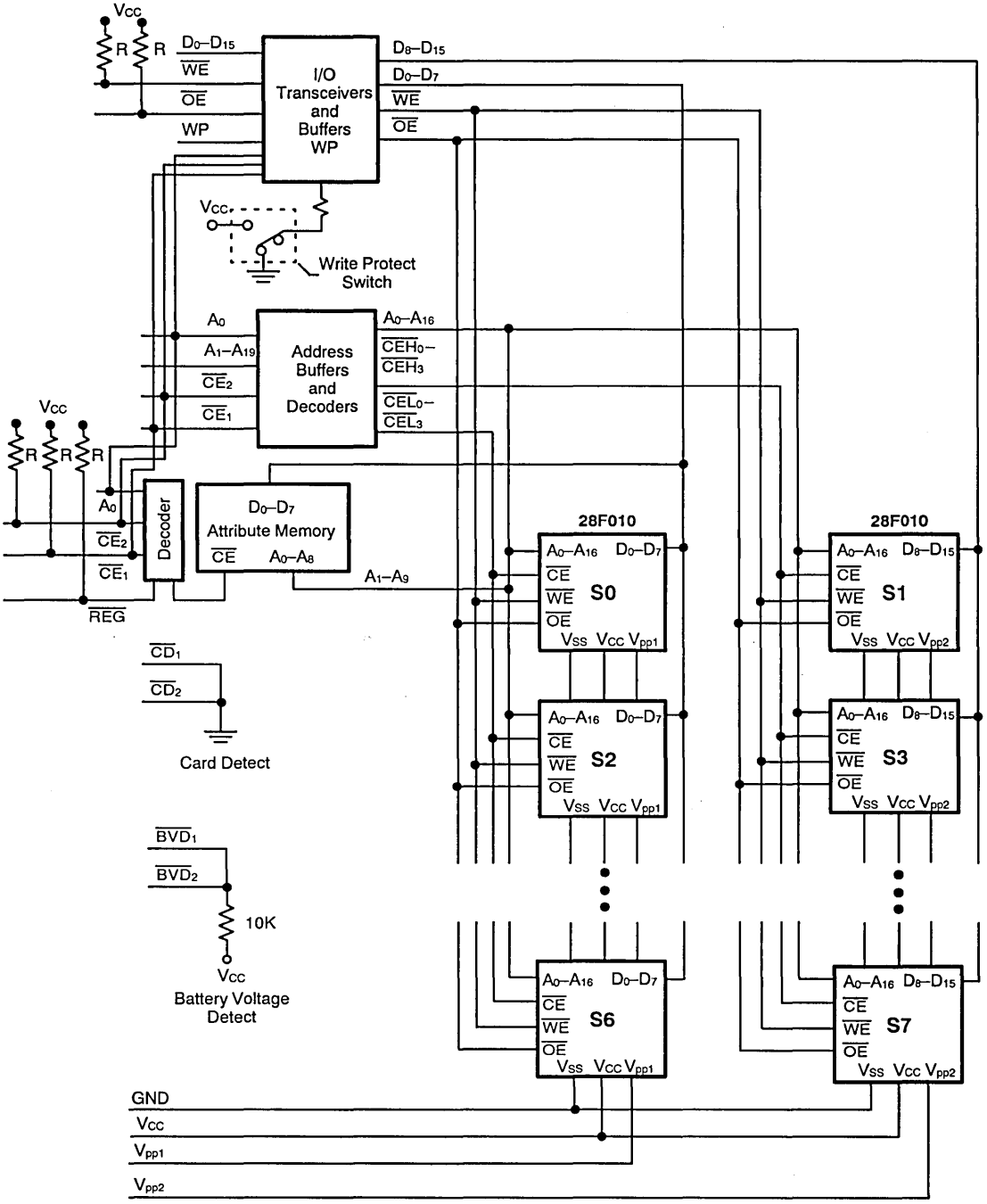
GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC001FLKA. This allows OEM manufacturers of portable system to eliminate the weight, power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC001FLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC001FLKA enhances the productivity of mobile workers.

Widespread acceptance of the AmC001FLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC001FLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

BLOCK DIAGRAM



R=33K

16660A-1

PC CARD PIN ASSIGNMENTS

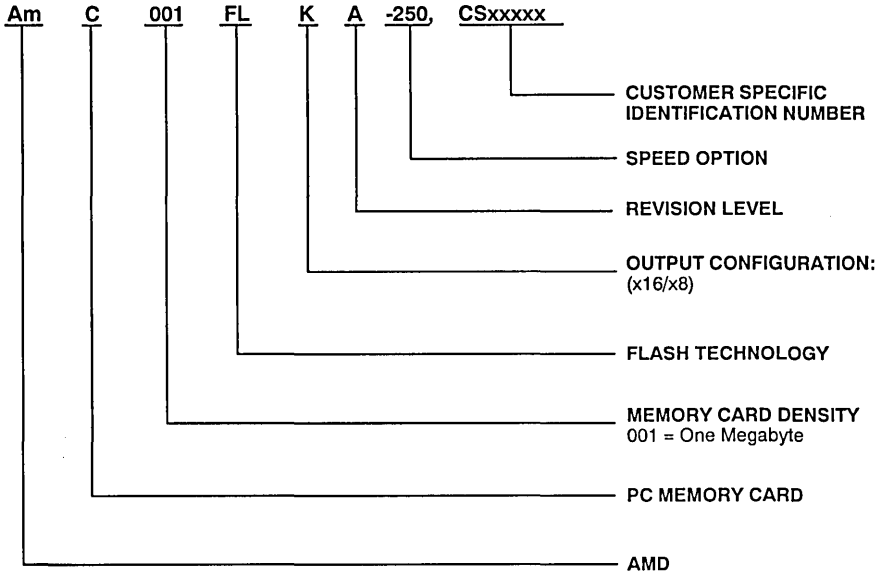
Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable (Note 1)	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2 (Note 1)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	RFU		Reserved
11	A_9	I	Address Bit 9	45	RFU		Reserved
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	NC		No Connect
16	NC		No Connect	50	NC		No Connect
17	V_{CC}		Power Supply	51	V_{CC}		Power Supply
18	V_{PP1}		Pgm Sply Vltg 1	52	V_{PP2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.
1. Signal must not be connected between cards
2. $\overline{BVD}$ = Internally pulled-up

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



PIN DESCRIPTION

Symbol	Type	Name and Function
$A_0 - A_{19}$	INPUT	**ADDRESS INPUTS** are internally latched during write cycles.
$D_0 - D_{15}$	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Data inputs are internally latched on write cycles. Data outputs during read cycles. Data pins are active high. When the memory card is de-selected or the outputs are disabled the outputs float to tri-state.
$\overline{CE}_1$, $\overline{CE}_2$	INPUT	**CARD ENABLE** is active low. The memory card is de-selected and power consumption is reduced to stand-by levels when $\overline{CE}$ is high. $\overline{CE}$ activates the internal memory card circuitry that controls the high and low byte control logic of the card, input buffers segment decoders, and associated memory devices.
$\overline{OE}$	INPUT	**OUTPUT ENABLE** is active low and enables the data buffers through the card outputs during read cycles.
$\overline{WE}$	INPUT	**WRITE ENABLE** is active low and controls the write function of the command register to the memory array. The target address is latched on the falling edge of the $\overline{WE}$ pulse and the appropriate data is latched on the rising edge of the pulse.
V_{PP1},V_{PP2}		**ERASE/WRITE POWER SUPPLY** for erase and programming. V_{pp} enables the command register which controls all functions required to alter the memory array contents. **Note:** AmC001FLKA functions as a read-only memory when $V_{PP} < V_{CC} + 2$ V.
V_{CC}		**PC CARD POWER SUPPLY** for device operation (5.0 V ± 5%)
GND		**GROUND**
CD_1, CD_2	OUTPUT	**CARD DETECT.** When card detect 1 and 2 = ground the system detects the card.
WP	OUTPUT	**WRITE PROTECT** is active high and disables all card write operations.
NC		**NO CONNECT** - corresponding pin is not connected internally.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT.** Internally pulled-up.

MEMORY CARD OPERATIONS

The AmC001FLKA Flash Memory Card is organized as an array of individual devices. Each device is 128K bytes in size. Although the address space is continuous each physical device defines a logical address segment size. Erase operations are performed in increments of this segment size. Multiple segments may be erased concurrently when additional V_{pp} current is supplied to the device. Once a memory segment is erased any address location may be programmed. Flash technology allows any logical "1" data bit to be programmed to a logical "0". The only way to reset bits to a logical "1" is to erase the entire memory segment of 128K bytes. High voltage is required on V_{pp1} and V_{pp2} to perform program and erase operations.

The common memory space data contents are altered in a similar manner as writing to individual Flash Memory devices. On-card address and data buffers activate the appropriate Flash device in the memory array. Each device internally latches address and data during write cycles. Refer to Table 2A.

Attribute memory is a separately accessed card memory space. The register memory space is active when the $\overline{REG}$ pin is driven low. The Card Information Structure describes the capabilities and specification of a card. The CIS is stored in the attribute memory space beginning at address 00000H. The AmC001FLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. Alternatively, the CIS can be stored at the beginning of the common memory address space. D_0–D_7 are active during attribute memory accesses. D_8–D_{15} should be ignored. Odd order bytes present invalid data. Refer to Table 2B.

Word-Wide Operations

The AmC001FLKA provides the flexibility to operate on data in a byte-wide or word-wide format. In word-wide operations the Low-bytes are controlled with V_{pp1} and $\overline{CE}_1$ when A_0 = 0. The High-bytes are controlled with V_{pp2} and $\overline{CE}_2$, A_0 = don't care.

Erase operations are the only operations that work on entire memory segment. All other operations such as word-wide programming are not affected by the physical memory segments.

Byte-Wide Operations

Byte-wide data is available on D_0–D_7 for read and write operations ($\overline{CE}_1$ = low, $\overline{CE}_2$ = high). Even and odd bytes are stored in separate memory segments (i.e. S_0 and S_1) and are accessed when A0 is low and high respectively. The even byte is the low order byte and the odd byte is the high order byte of a 16-bit word.

Erase operations in the byte-wide mode must account for data multiplexing on D_0–D_7 by changing the state of A0. Each memory segment pair must be addressed separately for erase operations.

Card Detection

Each $\overline{CD}$ (output) pin should be read by the host system to determine if the memory card is adequately seated in the socket. $\overline{CD}_1$ and $\overline{CD}_2$ are internally tied to ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

Write Protection

The AMD Flash memory card has three types of write protection. The PCMCIA/JEIDA socket itself provides the first type of write protection. Power supply and control pins have specific pin lengths in order to protect the card with proper power supply sequencing in the case of hot insertion and removal.

A mechanical write protect switch provides a second type of write protection. When this switch is activated, $\overline{WE}$ is internally forced high. The Flash memory command register is disabled from accepting any write commands.

The third type of write protection is achieved with V_{pp1} and V_{pp2} at logic low levels to reset the Flash devices to read-only mode. Memory contents can not be changed in this state. The command register of individual Flash memory segments is only active when V_{pp1} and/or V_{pp2} are at high voltage (V_{ppH}).

Each Flash memory device that comprises a Flash memory segment will reset the command register to the read-only mode when V_{cc} is below VLKO. VLKO is the voltage below which write operations to individual command registers are disabled.

MEMORY CARD BUS OPERATIONS

Read Enable

Two Card Enable ($\overline{CE}$) pins are available on the memory card. Both $\overline{CE}$ pins must be active low for word-wide read accesses. Only one $\overline{CE}$ is required for byte-wide accesses. The $\overline{CE}$ pins control the selection and gates power to the high and low memory segments. The Output Enable ($\overline{OE}$) controls gating accessed data from the memory segment outputs.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state.

Standby Operations

Byte-wide read accesses only require half of the read/write output buffer (x16) to be active. In addition, only one memory segment is active with in either the high order or low order bank. Activation of the appropriate half of the output buffer is controlled by the combination of both $\overline{CE}$ pins. The $\overline{CE}$ pins also control power to the high and low-order banks of memory. Outputs of the memory bank not selected are placed in the high impedance state. The individual memory segment is activated by the address decoders. The other memory segments operate in standby. An active memory segment continues to draw power until completion of a write, erase, or verify operation if the card is de-selected in the process of one of these operations.

Auto Select Operation

A host system or external card reader/writer can determine the on-card manufacturer and device I.D. codes. Codes are available after writing the 90H command to the command register of a memory segment. Reading from address location 00000H in any segment provides the manufacturer I.D. while address location 00002H provides the device I.D.

Write Operations

Write and erase operations are valid only when V_{pp1} and V_{pp2} are at high voltage. This activates the state machine of an addressed memory segment. The command register is a latch which saves address, commands, and data information used by the state machine and memory array.

When Write Enable ($\overline{WE}$) and appropriate $\overline{CE}$(s) are a logic-level low, the command register is enabled for write operations. The falling edge of $\overline{WE}$ latches address information and the rising edge latches data/command information.

Memory Segment Command Definitions

When the V_{pp} pin(s) are at low voltage the command register of each Flash memory segment defaults to 00H, the Read only mode.

With high voltage on the V_{pp} pin(s), the Flash memory segments are active for either read, write, or erase operations.

Write or erase operations are performed by writing appropriate data patterns to the command register of accessed Flash memory segments.

The byte-wide and word-wide commands are defined in Tables 3 and 4 respectively.

Table 2A. Common Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Note 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Note 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Note 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	High Z
Read (x16) (Note 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	Data Out-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Notes 2, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Data Out-Odd	High Z
Read (x16) (Notes 2, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Data Out-Odd	Data Out-Even
Write (x8) (Notes 4, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data In-Odd
Write (x8) (Notes 4, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Data In	High Z
Write (x16) (Note 5, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Data In-Odd	Data In-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a Byte write operation.
5. Refer to Table 4 for valid D_{IN} during a Word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. Byte access – Even. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Byte access – Odd. In this x8 mode, $A_0 = V_{IH}$ outputs or inputs the "odd" byte (high byte) of the x16 word on D_0–D_7. This is accomplished internal to the card by transposing D_8–D_{15} to D_0–D_7.
9. Odd byte only access. In this x8 mode, A_0 = X outputs or inputs the "odd" byte (high byte) of the x16 word on D_8–D_{15}.
10. x16 word accesses present both "even" (low) and "odd" (high) bytes. $A_0 = V_{IL}$ or V_{IH} = "Don't Care".

Table 2B. Attribute Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Notes 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Not Valid
Read (x8) (Note 8)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	High Z
Read (x16) (Notes 8, 9, 10)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	Data Out-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Read (x8) (Note 9)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Read (x16) (Notes 2, 9)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Not Valid	Data Out-Even
Write (x8) (Notes 4, 7, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Write (x8) (Notes 4, 9, 10)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Write (x16) (Note 10)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Not Valid	Data In-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a Byte write operation.
5. Refer to Table 4 for valid D_{IN} during a Word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Only even-byte data is valid during Attribute Memory Read function.
9. During Attribute Memory Read function, $\overline{REG}$ and $\overline{OE}$ must be active for the entire cycle.
10. During Attribute Memory Write fuction, $\overline{REG}$ and $\overline{WE}$ must be active for the entire cycle, $\overline{OE}$ must be inactive for the entire cycle.

Table 3. Command Definitions for Byte-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	90H	Read	00H/01H	01H/A7H
Erase Set-up/Erase (Note 4)	Write	SA	20H	Write	SA	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figures 1, 3 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section
   Address: 00H/01H = Address for manufacturer code/Device code.
   Data: 01H/A7H = Data for manufacturer code/Device code

Table 4. Command Definitions for Word-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	0000H/ FFFFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	9090H	Read	0000H/ 0101H	0101H/ A7A7H
Erase Set-up/Erase (Note 4)	Write	SA	2020H	Write	SA	2020H
Erase-Verify (Note 4)	Write	EA	A0A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	4040H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFFFH	Write	X	FFFFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figures 1, 3 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

Details of AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-up is the first of a two-cycle erase command. It is a command-only operation that stages the addressed memory segment for bulk erase. The array contents are not altered with this command. 20H is written to the command register (2020H for word-wide) in order to perform the erase Set-up operation.

Erase

The second two-cycle erase command initiates the segment erase operation. You must write the Erase command 20H (2020H for word-wide) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, segment erasure can only occur when high voltage is applied to the V_{pp} pins. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase operation erases all bytes of the segment in parallel. After the erase operation, all bytes in the segment must be sequentially verified. For byte-wide operations, the A_0 signal selects between the odd and even byte banks within the memory segment. Erase and erase-verify operations must be performed in completion on the even byte segment of 128K byte then the odd byte segment of 128K byte. The Erase-verify operation is initiated by writing A0H (A0A0H for word-wide) to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the segment applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte (FFFFH for word-wide) indicates that all bits in the byte (word) are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte (word) in the memory segment until a byte (word) does not return FFH (FFFFH) data or all the bytes in the segment are accessed and verified.

If an address is not verified to FFH (FFFFH) data, the segment is erased again (refer to erase Set-up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The segment is now ready to be programmed. The verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figures 1 and 3 and Table 6, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Flasherase Electrical Erase Algorithm

This Flash memory segment erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the accessed memory segment. Erasure begins with a read of the memory contents. Reading FFH (FFFFH for word-wide) data from the segment would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

Should the segment be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the segment to their charged state (Data = 00H or 0000H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH or FFFFH) begins at address 00000H and continues through the array to the last address, or until data other than FFH (FFFFH) is encountered. For byte-wide erase operations, the A_0 signal selects between the odd and even byte banks within the memory segment. Each bank must be operated on individually and completely in verify operations. If a byte (word) fails to verify, the device is erased again. With each erase operation, an increasing number of bytes (words) verify to the erased state. Typically, devices are erased in less than 70 pulses. Erase efficiency may be improved by storing the address of the last byte (word) that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. When all bytes within an accessed segment are erased, additional segments may be erased by following the same routine. Memory segments are typically erased in less than one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin.

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The AmC001FLKA is programmed byte by byte (or word by word). Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the addressed memory segment for byte programming. The Set-up Program operation is performed by writing 40H (4040H for word-wide) to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte (word) just programmed must be verified.

Write C0H (C0C0H) into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte (word) programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the memory segment applies an internally generated margin voltage to the addressed byte (word). A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte (word) was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte (word) location. Should the byte (word) fail to verify, reprogram the byte (word) using the Program Set-up/Program Commands. Figure 2 and Table 5 indicate how instructions are combined with the bus operations to perform byte (word) programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

The reset command initializes the memory segment to the read mode. In addition, it also provides a safe method to abort any memory segment operation (including program or erase). The reset command must be written two consecutive times after the program set-up command. This will safely reset the segment memory to the read mode. Memory contents are not altered. Following any other command, write the reset command once to the segment. This will safely abort any operation and reset the device to the Read mode.

Flashrite Programming Algorithm

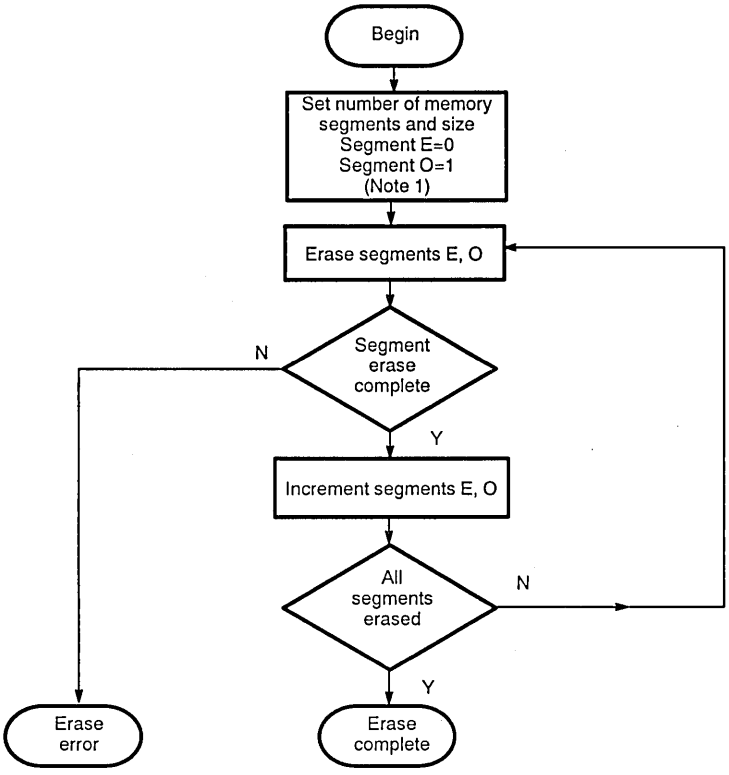
The Flashrite Programming algorithm employs an interactive closed loop flow to program data. Bytes or words may be programmed sequentially or at random using 10 microsecond programming pulses. Each operation is followed by a byte or word verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte or word per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte or word verification is performed with high voltage applied to the V_{PP} pin. Figure 2 and Table 5 illustrate the programming algorithm.

Auto Select

The Auto Select mode allows the reading out of a binary code from the memory devices to identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

MEMORY CARD ERASE ROUTINE

Overview



Note:
1. E = Even byte, O = Odd byte.

Figure 1.

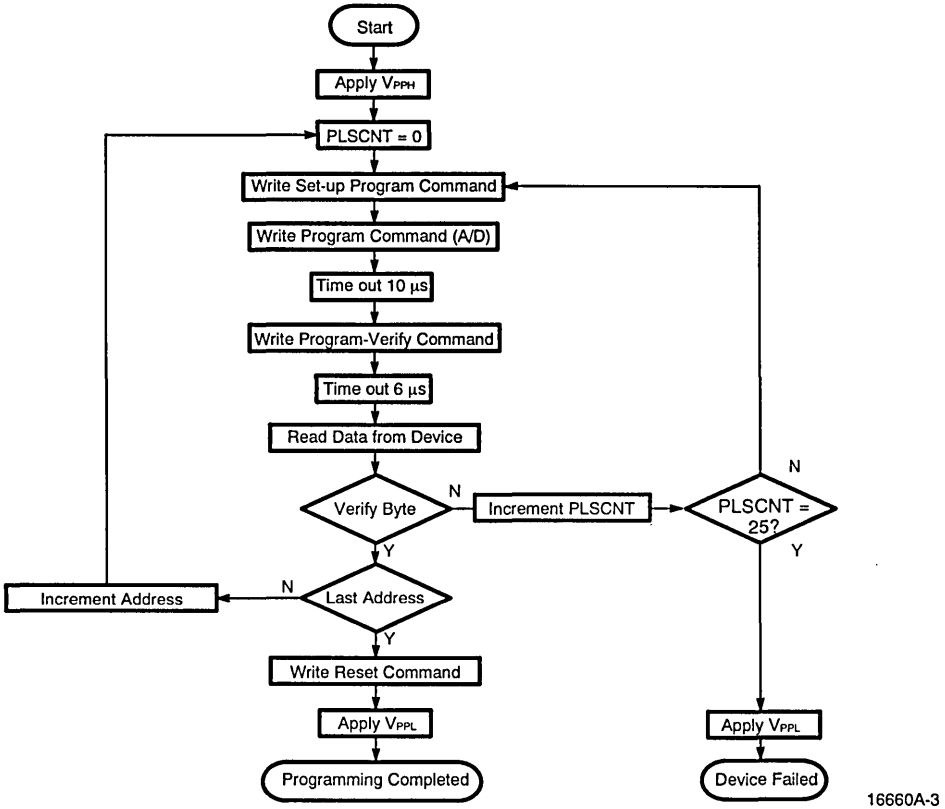


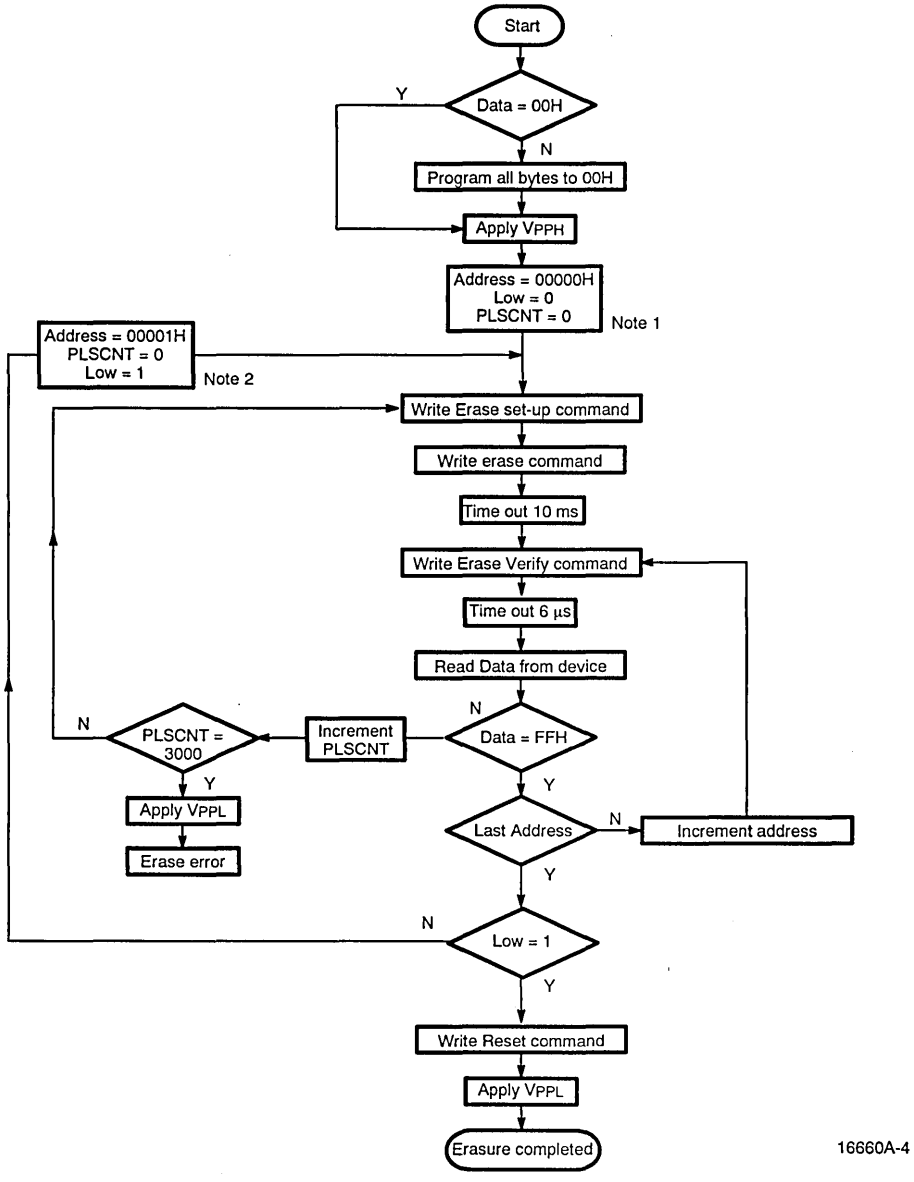
Figure 2. Flashrite Programming Algorithm in Byte-Wide Mode

Table 5. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



Notes:

1. Low = 0: Even byte segment Erase/Erase verify operation.
2. Low = 1: Odd byte segment Erase/Erase verify operation.

Figure 3. Flasherase Electrical Erase Algorithm in Byte-Wide Mode

Table 6. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 μs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.

WORD-WIDE PROGRAMMING

The program sequence will be followed as usual. The program word command is 4040H. Each device is independently verified. When one of the program flags is active, indicating that a particular device has successfully completed programming, the software should change the command for that device from Program to Reset and from program verify to Reset. The software should also change the Program Data to the null data set (FFH). This effectively masks the programmed device from further programming.

Should the high order byte device verify first, the next program command will be FF40H. The low order byte device programs on each subsequent program command until verified. The high order byte device remains in Reset/Read mode. During verification, write the program verify command of FFC0H. This will enable the low order byte device for verify operations and maintains the programmed high order byte device in Reset/Read mode.

WORD-WIDE PROGRAMMING
Overview

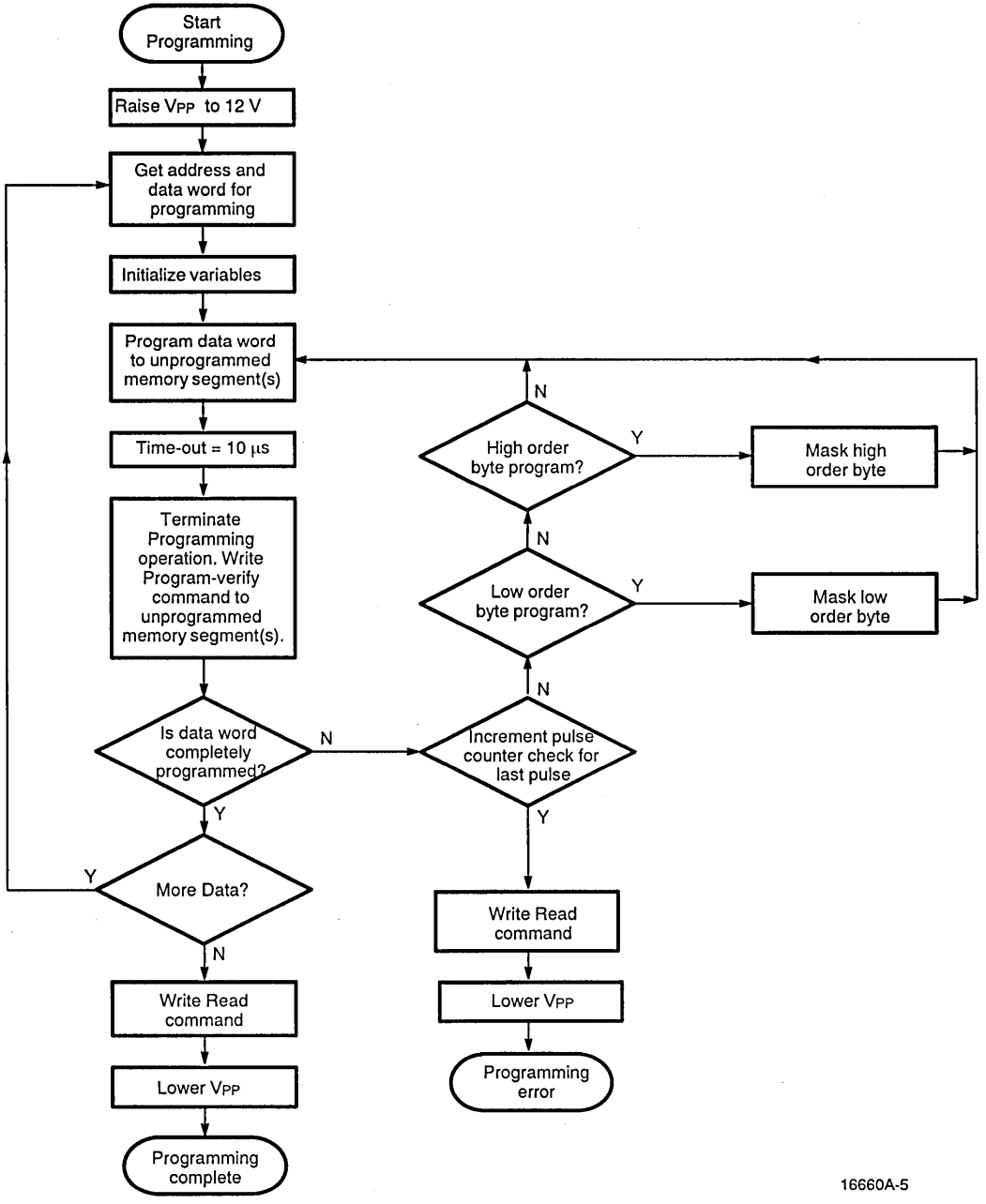
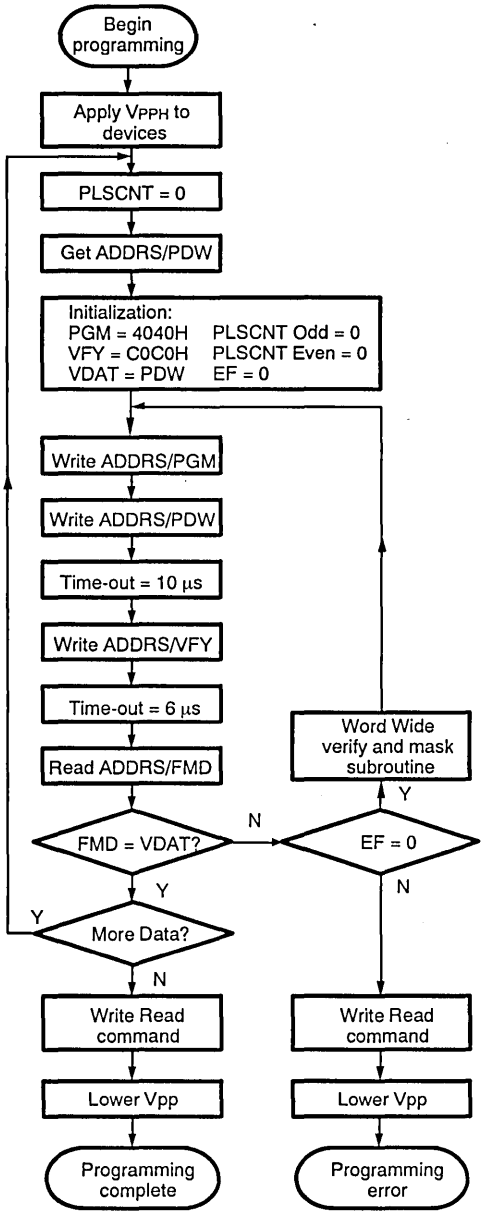


Figure 4.

WORD-WIDE PROGRAMMING FLOW CHART



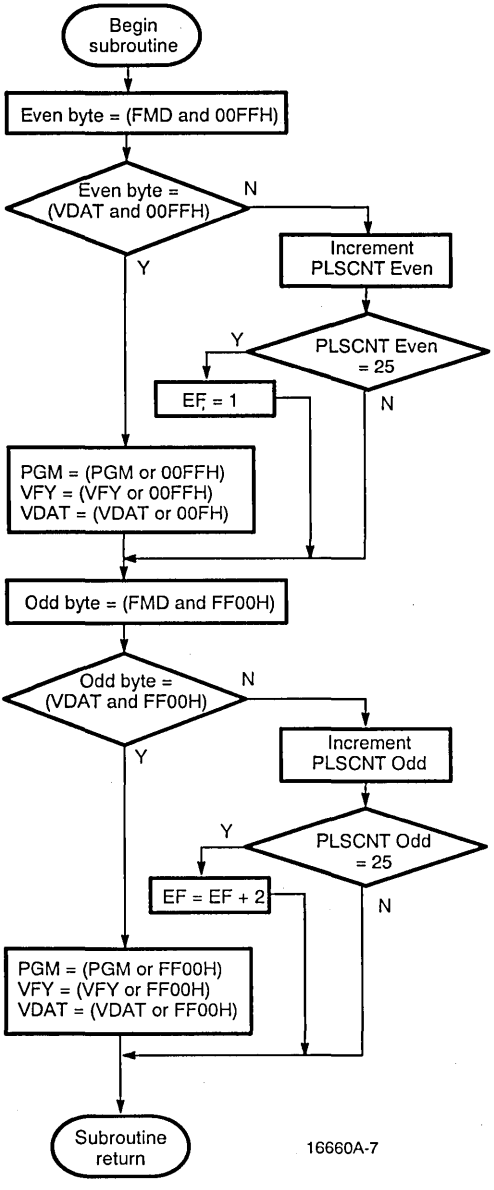
16660A-6

Note:
Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any device from programming operations.

Activity
Allow VPP to stabilize.
PLSCNT = Pulse Counter.
ADDRS = Word Address to program. *PDW = Data Word to program.*
Initialize Programming Variables: *PGM = Program Command* *VFY = Program-verify Command* *VDAT = Valid Data* *PLSCNT Odd = Pulse count for odd (high) byte* *PLSCNT Even = Pulse count for even (low) byte* *EF = Error Flag for write*
ADDRS = Address do not care. *Write Program Set-up command.*
Appropriate address and data for programming.
Duration of programming pulse.
Program-verify command terminates the programming pulse.
Internal margin verify voltages are tapped from external 12 V VPP for proper byte verification.
Read from previously latched address. FMD = Flash Memory Data.
See Word Wide Programming subroutine. Each device is independently verified. The Program command is masked by the Reset command (FFH) for all devices that are completely Programmed. Please see note below.
Compare Flash Memory Data to valid word data. If verified, reset PLSCNT and get next address and data word for programming. If not last pulse, compare high order byte device and low order byte device for valid byte data.
Reset devices for read operation.
VPPL deactivates command register. Device is in Read Only Mode.

Figure 5.

WORD-WIDE PROGRAMMING VERIFY SUBROUTINE



Commentary

This subroutine verifies the high order (odd) and low order (even) bytes independently. If either byte verifies, all commands are masked to that device.

Mask the odd byte to look at the even byte.

If the even byte doesn't verify, increment pulse count and continue of program even byte.
EF = Error Flag

Mask the even byte commands and program data if it verifies.

Mask the even byte to look at the odd byte.

If the odd byte doesn't verify, increment pulse count and continue to program odd byte.

Mask the odd byte commands and program data if it verifies.

Error Flag Summary:

EF = 0 indicates no program error
EF = 1 indicates even byte program error
EF = 2 indicates odd byte program error
EF = 3 indicates both even and odd byte program error

Figure 6.

WORD-WIDE ERASING

Overview

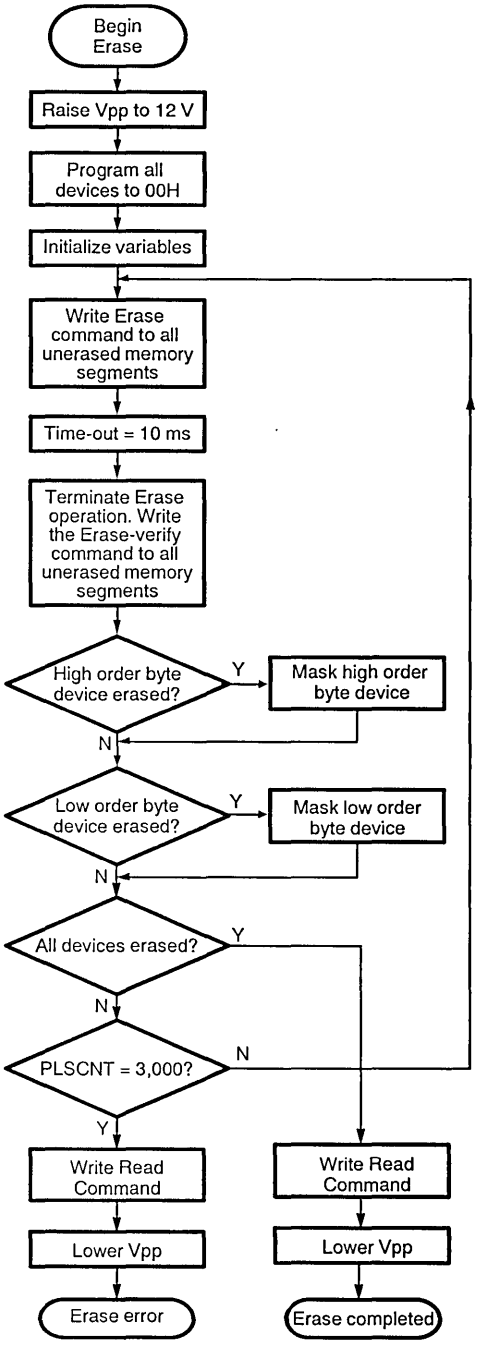
Word-Wide Erasure

Word-wide erasure reduces total erase time when compared to erasing each byte individually. Each Flash memory may erase at different rates. Therefore each device must be verified separately after every erase pulse. Once a device has successfully completed erasure, do not issue the erase command again to that device. Issue the Reset command FFH to the erased device. The Erase command sequence may be issued to each of the remaining devices that have not erased yet. In addition to the address verify register required for each device, you will need an erase complete flag for each device.

Word-Wide

The erase sequence will be followed as usual. The CPU will issue word commands. The erase word command is 2020H. Each device is independently verified and the address of the last verified byte per device is stored in separate registers. When one of the erase flags is active, indicating that a particular device has successfully completed erasure, the CPU will change the command for that device from Erase to Reset. This effectively masks the erased device from further erasure.

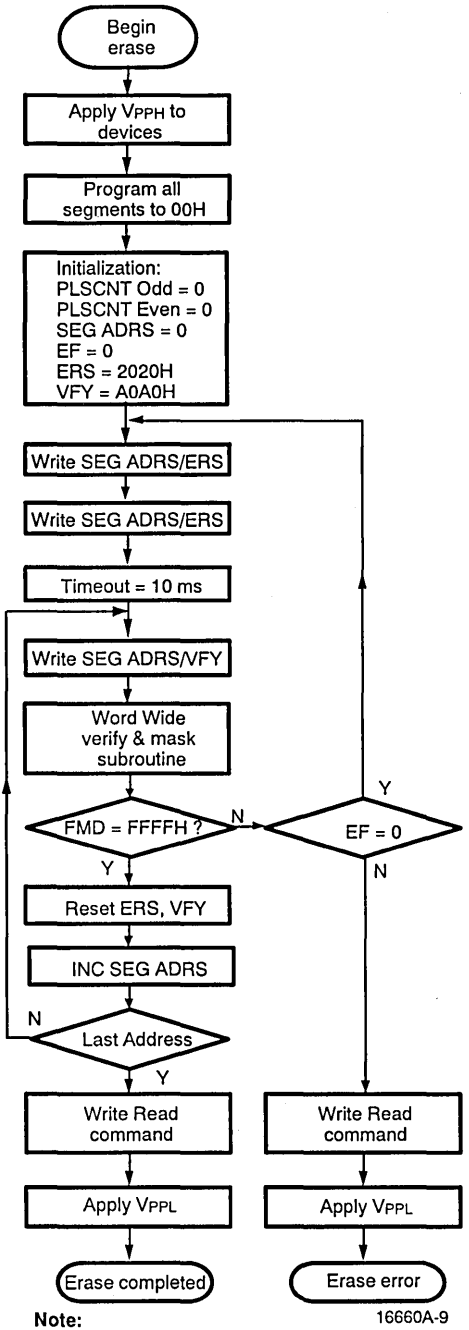
Should the high order byte device verify first, the next erase command will be FF20H. The low order byte device erases on each subsequent erase command until verified. The high order byte device remains in Reset/Read mode. During verification, write the erase verify command of FFA0H. This will enable the low order byte device for verify operations and maintains the erased high order byte device in the Reset/Read mode.



16660A-8

Figure 7.

WORD-WIDE ERASURE FLOW CHART

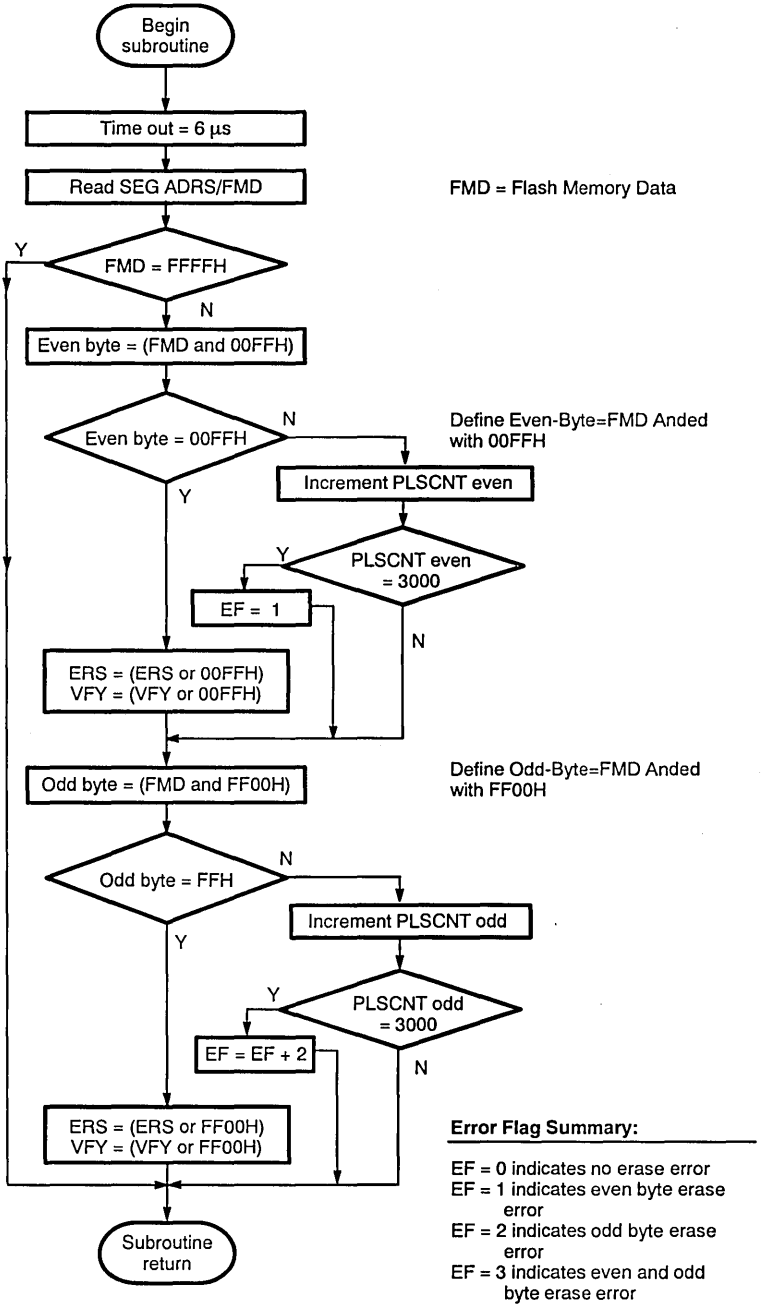


Activity	
Begin erase	
Apply V_{PPH} to devices	*Allow V_{PP} to stabilize.*
Program all segments to 00H	*Follow Flashrite programming algorithm.*
Initialization: PLSCNT Odd = 0 PLSCNT Even = 0 SEG ADRS = 0 EF = 0 ERS = 2020H VFY = A0A0H	*Initialize Erase Variables:* *PLSCNT Odd = Pulse count for odd (high) byte* *PLSCNT Even = Pulse count for even (low) byte* *SEG ADRS = Address* *EF = Error Flag for error* *ERS = Erase Command* *VFY = Erase-verify Command*
Write SEG ADRS/ERS	*Write Program Set-up command.*
Write SEG ADRS/ERS	*Initiate erase pulse.*
Timeout = 10 ms	*Duration of programming pulse.*
Write SEG ADRS/VFY	*Erase-verify command terminates the erase pulse.*
Word Wide verify & mask subroutine	*See Word Wide Erasure subroutine. Each device is independently verified. The command is masked by the Reset command (FFH) for all devices that are completely erased. Please see note below.*
FMD = FFFFH ? / EF = 0	*FMD = FFFFH when memory segment at SEG ADRS is erased.*
Reset ERS, VFY	*Reset devices for read operation.*
INC SEG ADRS / Last Address	
Write Read command	
Apply V_{PPL}	*V_{PPL} deactivates command register. Device is in the Read Only Mode.*
Erase completed / Erase error	

Note:
Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any completely erased device from further erase operations.

Figure 8.

WORD-WIDE ERASE VERIFY SUBROUTINE



16660A-10

Figure 9.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −30°C to +70°C

Ambient Temperature
with Power Applied ..... −10°C to +70°C

Voltage with Respect to Ground
All pins except V_{PP} (Note 1) ..... −2.0 V to +7.0 V

V_{CC} (Note 1) ..... −2.0 V to +7.0 V

V_{PP} (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5 V. During voltage transitions, outputs may overshoot to V_{CC} +2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on V_{PP} pins is −0.5 V. During voltage transitions, V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = V_{CC} max. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +60°C

V_{CC} Supply Voltages ..... +4.75 V to 5.25 V

V_{PP} Supply Voltages

Read Only ..... 0 V to +6.5 V

Program, Erase, Verify,
and Read ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Byte Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ±0.2 V		0.4	0.8	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		25	50	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		3.0	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		5.0	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			10	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.2	0.4	mA
		$V_{PP} \leq V_{CC}$			0.04	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		8.0	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. One Flash device active, seven in standby.
2. Only one Vpp is active.

DC CHARACTERISTICS

Word-Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ±0.2 V		0.4	0.8	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		40	80	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		6	60	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	60	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} ≤ V_{CC}			10	µA
I_{PP1}	V_{PP} Read Current	V_{PP} > V_{CC}		0.4	0.8	mA
		V_{PP} ≤ V_{CC}			0.08	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		16	60	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		20	60	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = 2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. Two Flash devices active, six in standby.
2. V_{pp1} and V_{pp2} are active.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Capacitance	V_{IN} = 0		21	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		21	pF
C_{IN2}	Control Capacitance	V_{IN} = 0 ($\overline{CE}$, $\overline{REG}$)		47	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = 0		21	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING AC CHARACTERISTICS

Read Only Operation (Note 1)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	250		ns
t_{ELQV}	t_{CE}	Chip Enable Access Time		250	ns
t_{AVQV}	t_{ACC}	Address Access Time		250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time		150	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	5		ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z		60	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z		60	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
t_{WHGL}		Write Recovery Time before Read	6		µs

Note:

1. Input Rise and Fall Times (10% to 90%): ≤ 10 ns, Input Pulse levels: V_{OL} and V_{OH}, Timing Measurement Reference Level – Inputs: V_{IL} and V_{IH} Outputs: V_{IL} and V_{IH}

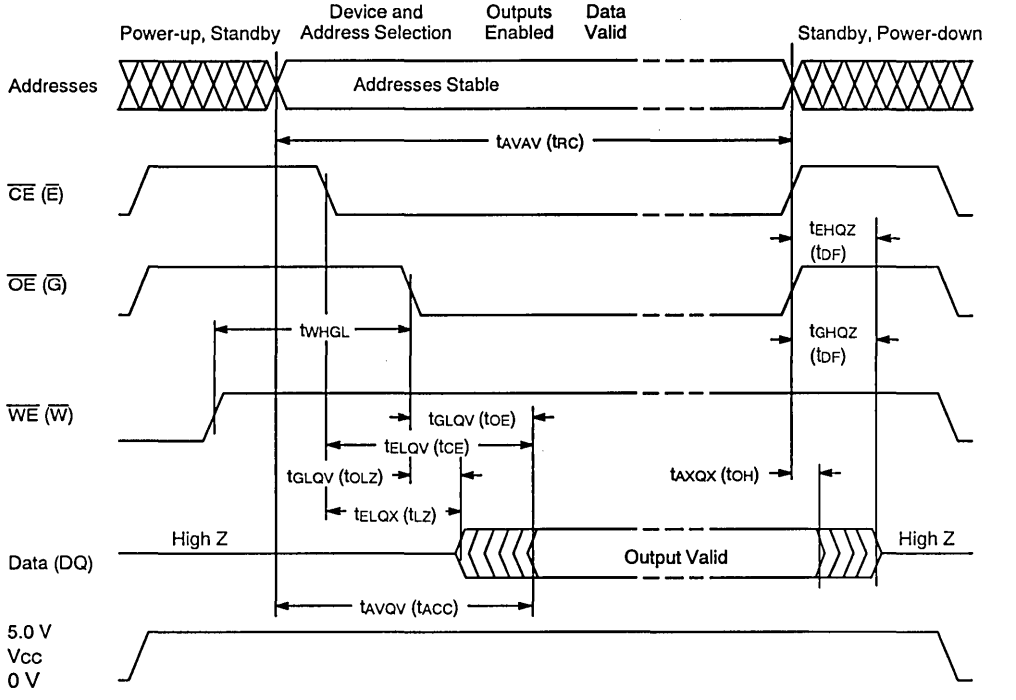
AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVWL}	t_{AS}	Address Set-Up Time	0		ns
t_{WLAX}	t_{AH}	Address Hold Time	100		ns
t_{DVWH}	t_{DS}	Data Set-Up Time	80		ns
t_{WHDX}	t_{DH}	Data Hold Time	30		ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHWL}		Read Recovery Time before Write	0		µs
t_{WLOZ}		Output in High-Z from Write Enable	5		ns
t_{WHOZ}		Output in Low-Z from Write Enable		60	ns
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	40		ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	100		ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	50		ns
t_{WHWH1}		Duration of Programming Operation (Notes 1, 2)	10		µs
t_{WHWH2}		Duration of Erase Operation (Notes 1, 2)	9.5		ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	100		ns

Notes:

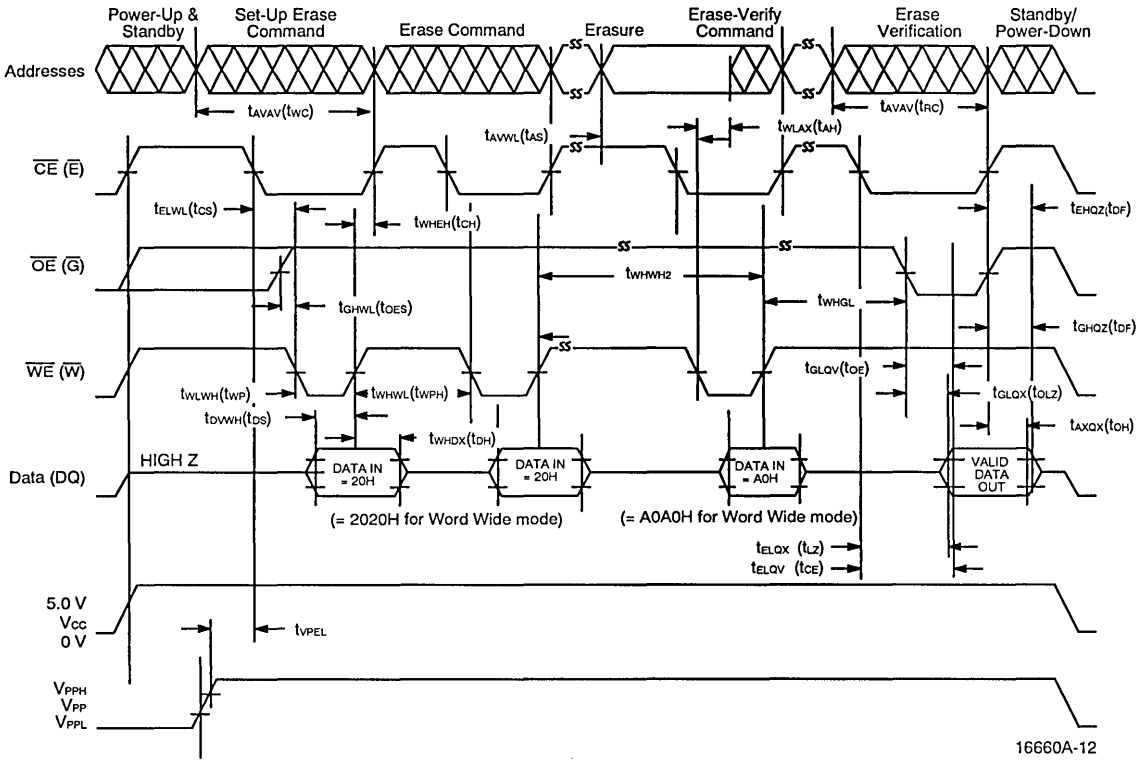
1. Rise/Fall < = 10 ns.
2. Maximum specification not needed due to the devices internal stop timer that will stop any erase or write operation that exceed the device specification.



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

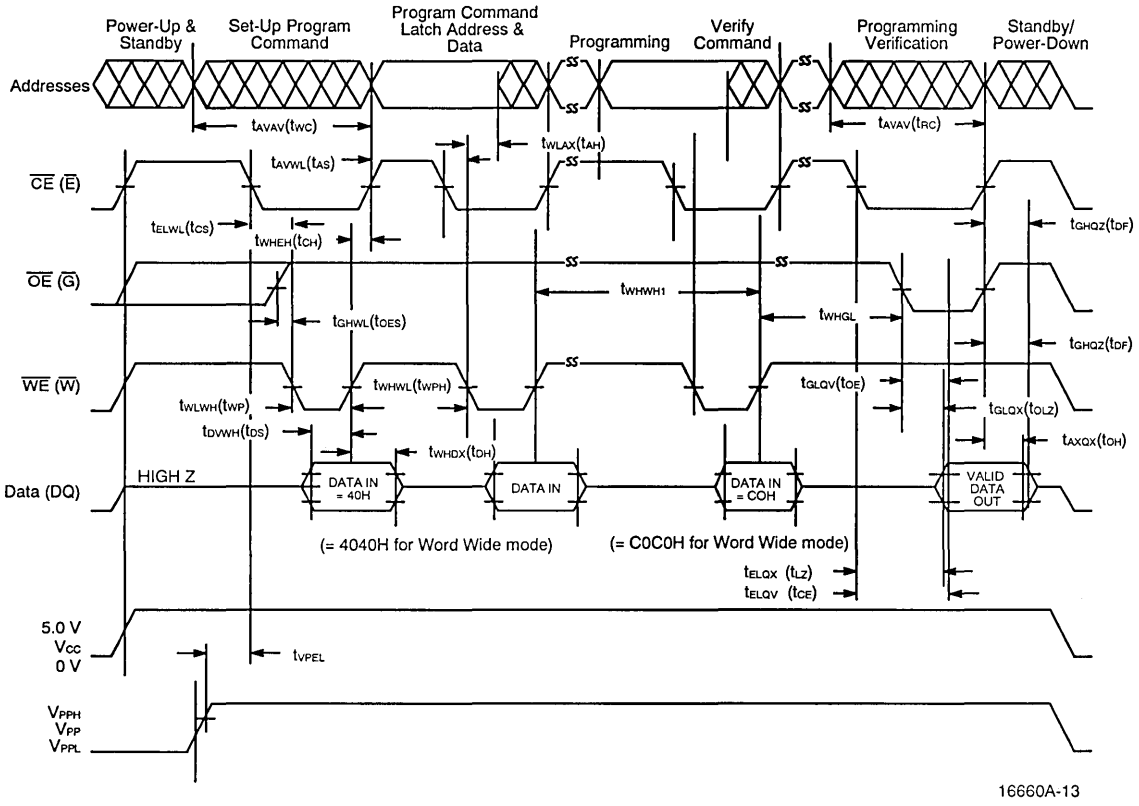
16660A-11

Figure 10. AC Waveforms for Read Operations



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

Figure 11. AC Waveforms for Erase Operations



16660A-13

Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

Figure 12. AC Waveforms for Programming Operations

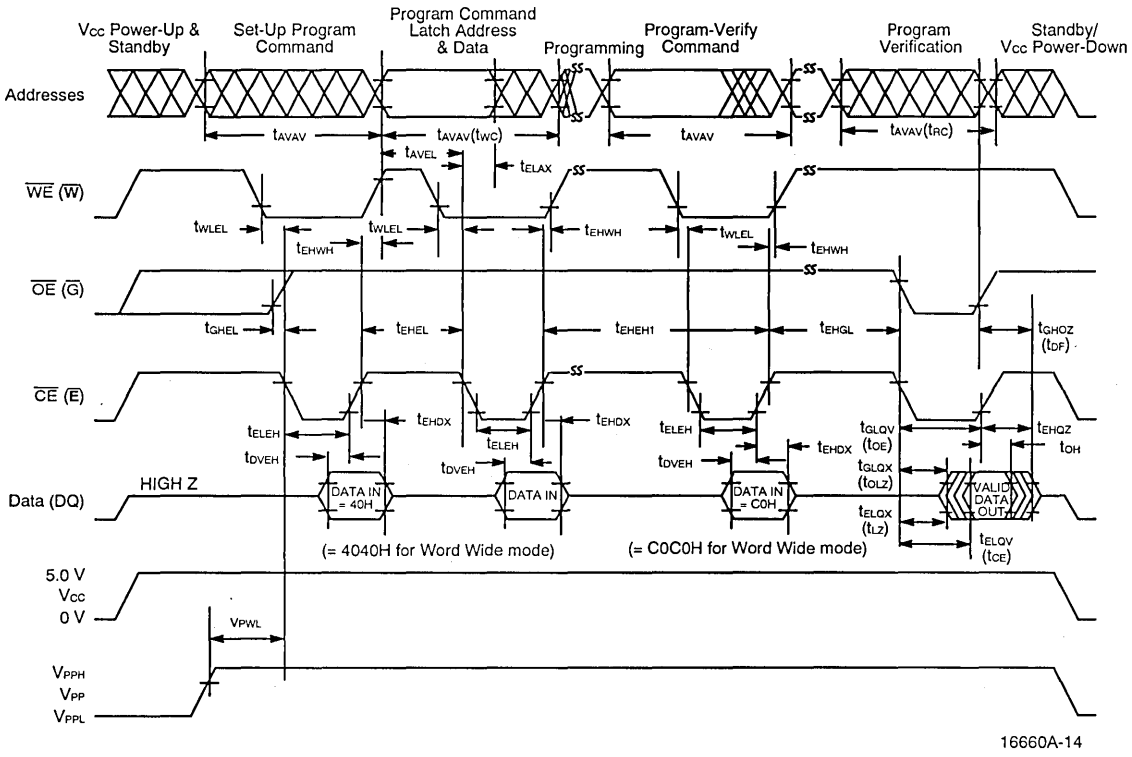
AC CHARACTERISTICS–ALTERNATE $\overline{CE}$ CONTROLLED WRITES

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVEL}	t_{AS}	Address Set-Up Time	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	100		ns
t_{DVEH}	t_{DS}	Data Set-Up Time	80		ns
t_{EHDX}	t_{DH}	Data Hold Time	30		ns
t_{EHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHEL}		Read Recovery Time before Write	0		µs
t_{WLEL}	t_{WS}	WE Set-Up Time before $\overline{CE}$	0		ns
t_{EHWH}	t_{CP}	WE Hold Time	0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	100		ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH (Note 3)	50		ns
t_{EHEH1}		Duration of Programming Operation (Notes 1, 2)	10		µs
t_{EHEH2}		Duration of Erase Operation (Notes 1, 2)	9.5		ms
t_{VPWL}		V_{PP} Set-Up Time to Write Enable LOW	100		ns

Notes:

1. Rise/Fall <=10 ns
2. Maximum specification not needed due to the internal stop timer that will stop any erase or write operation that exist the device specification.
3. Chip Enable Controlled Programming:
   Flash Programming is controlled by the valid combination of the Chip Enable ($\overline{CE}_{1,2}$) and Write Enable ($\overline{WE}$) signals. For system that uses the Chip Enable signal(s) to define the write pulse width, all Set-up, Hold, and inactive Write Enable timing should be measured relative to the Chip Enable signal(s).



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

Figure 13. Alternate AC Waveforms for $\overline{CE}$ Controlled Programming Operations

CARD INFORMATION STRUCTURE

The AmC001FLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. All or part of the 512 byte could be used for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space. Part of the common memory space could also be mapped into the attribute memory space if more than 512 bytes of CIS are needed.

The EEPROM used in the AmC001FLKA is a NEC μPD28C05GX-20-EJA designed to operate from a 5 V single power supply. The μPD28C05 provides a DATA polling function that provides the End of Write Cycle, Chip Erase and Auto Erase and Programming functions.

SYSTEM DESIGN AND INTERFACE INFORMATION

Power Up and Power Down Protection

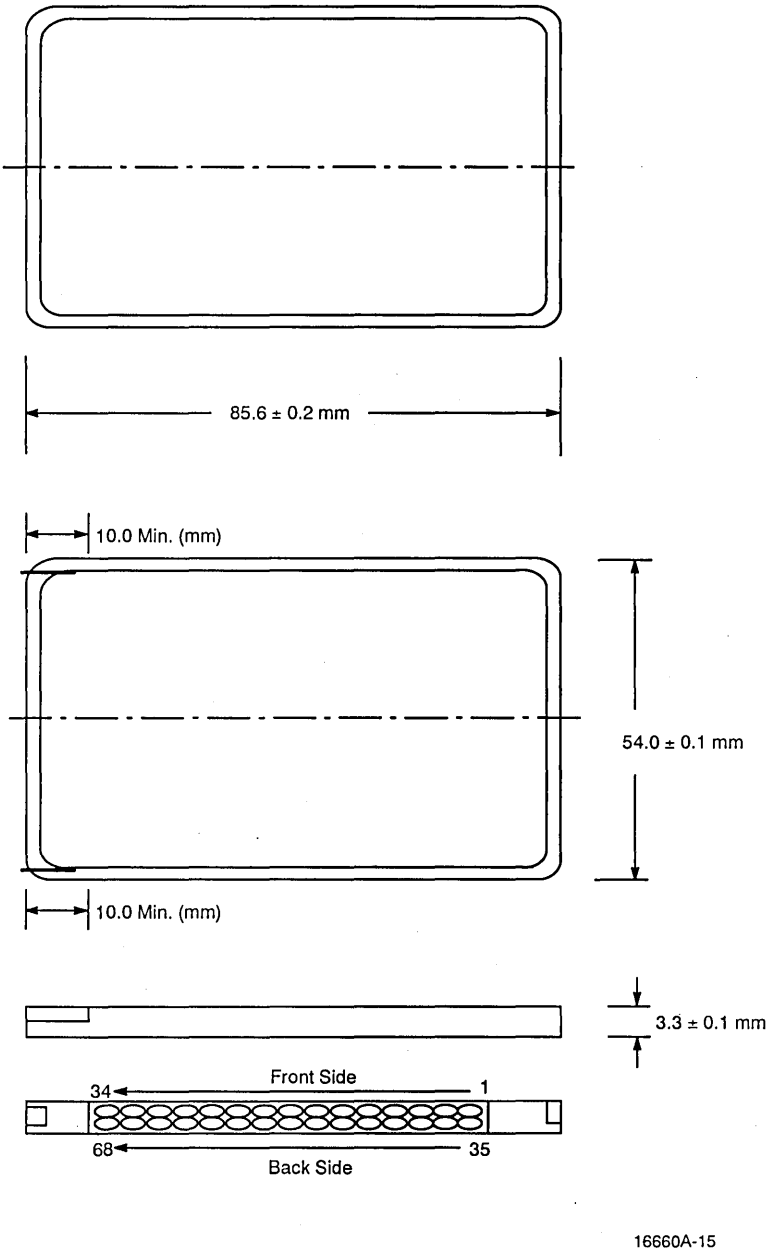
The PCMCIA standard socket provides for proper power up and power down sequencing via different pin lengths to ensure that hot insertion and removal of the PC card will not result in card damage or data loss.

AMD's Flash memory devices are designed to protect against accidental programming or erasure caused by spurious system signals that might exist during hot insertion, hot removal, or power transitions. The AMD PC card will power-up into a READ mode and the card will function as a read only memory as long as V_{pp} is less than V_{cc} +2 V. Erasing of the memory segments can be accomplished only by writing the proper Erase command to the card twice along with the proper Chip Enable, Output Enable and Write Enable control signals.

System Power Supply Decoupling

The AMD Flash memory card has a 0.1 μF decoupling capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins. It is recommended the system side also have a 4.7 μF capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins.

PHYSICAL DIMENSIONS
Type 1 PC Card



PRELIMINARY

AmC002FLKA

2 Megabyte Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 250 ns maximum access time
- **CMOS low power consumption**
  - 25 mA typical active current (X8)
  - 400 μA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **High re-programmable endurance**
  - Minimum 10,000 Write/Erase cycles
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate attribute memory**
  - 512 byte EEPROM
- **Flashrite™ and Flasherase™ Operations**
  - 256K byte memory segment
  - Typically two seconds per single memory segment erase
  - Random address writes to previously erased Bytes (10 μs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Read voltage, 5 V ± 5%**
- **Write and erase voltage, 12.0 V ± 5%**
- **Insertion and removal force**
  - State of art connector allows for minimum card insertion and removal effort
- **Manufactured by DuPont Connector Systems**

GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC002FLKA. This allows OEM manufacturers of portable systems to eliminate the weight, power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC002FLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC002FLKA enhances the productivity of mobile workers.

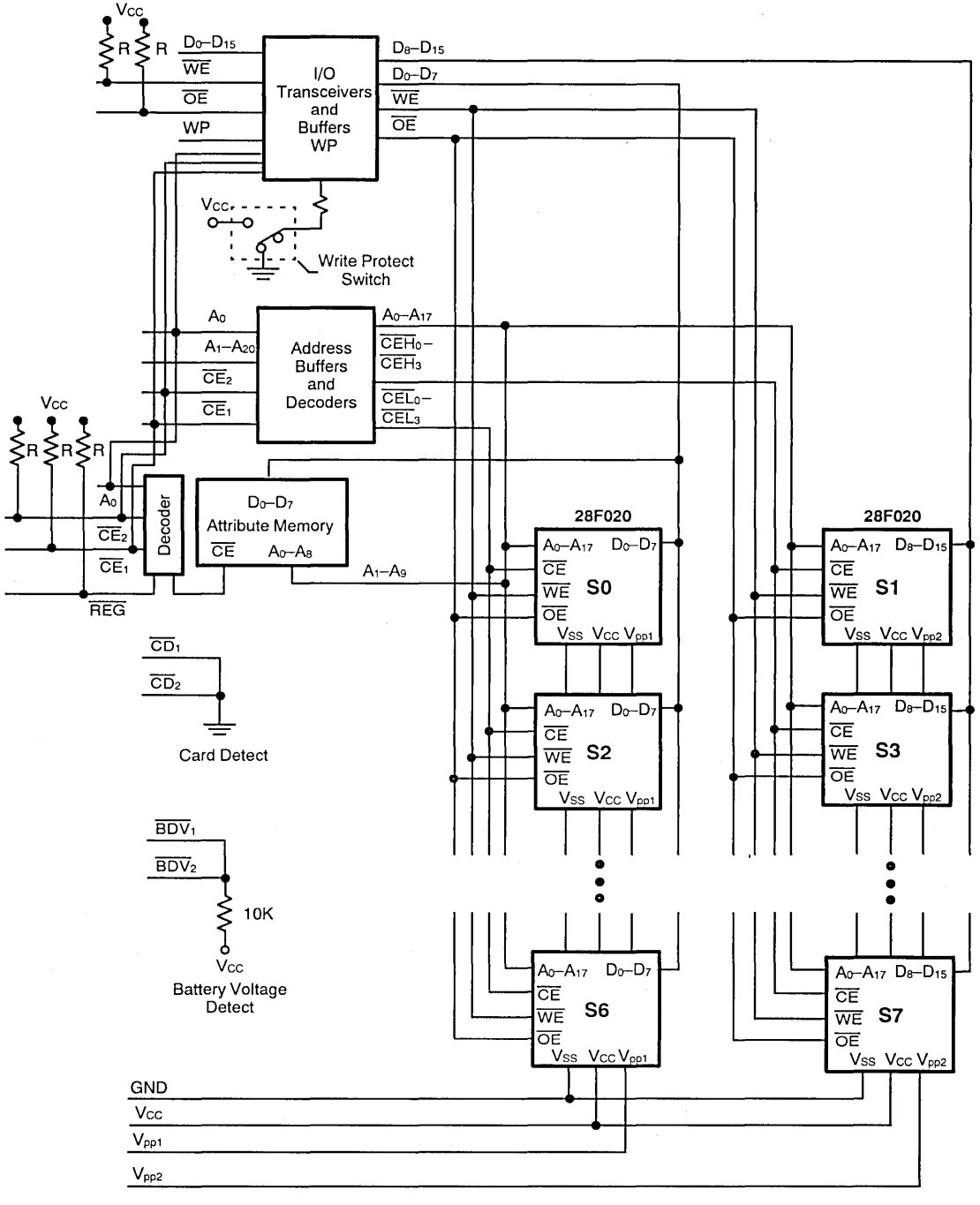
Widespread acceptance of the AmC002FLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC002FLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by DuPont Connector Systems

Publication# 16661 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



R=33K

16661A-1

PC CARD PIN ASSIGNMENTS

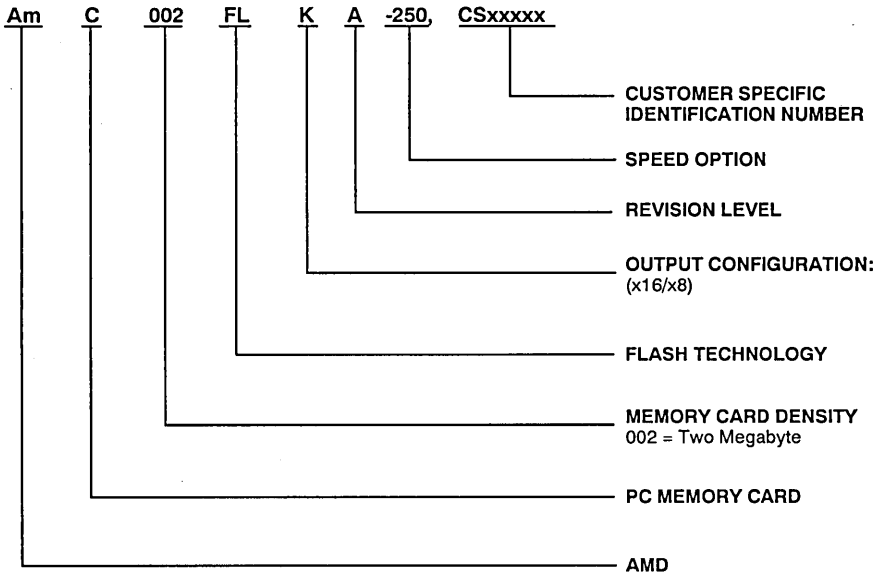
Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable (Note 1)	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2 (Note 1)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	RFU		Reserved
11	A_9	I	Address Bit 9	45	RFU		Reserved
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	A_{20}	I	Address Bit 20
16	NC		No Connect	50	NC		No Connect
17	V_{CC}		Power Supply	51	V_{CC}		Power Supply
18	V_{PP1}		Pgm Sply Vltg 1	52	V_{PP2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.
1. Signal must not be connected between cards
2. $\overline{BVD}$ = Internally pulled-up

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



PIN DESCRIPTION

Symbol	Type	Name and Function
$A_0 - A_{20}$	INPUT	**ADDRESS INPUTS** are internally latched during write cycles.
$D_0 - D_{15}$	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Data inputs are internally latched on write cycles. Data outputs during read cycles. Data pins are active high. When the memory card is de-selected or the outputs are disabled the outputs float to tri-state.
$\overline{CE}_1$, $\overline{CE}_2$	INPUT	**CARD ENABLE** is active low. The memory card is de-selected and power consumption is reduced to stand-by levels when $\overline{CE}$ is high. $\overline{CE}$ activates the internal memory card circuitry that controls the high and low byte control logic of the card, input buffers segment decoders, and associated memory devices.
$\overline{OE}$	INPUT	**OUTPUT ENABLE** is active low and enables the data buffers through the card outputs during read cycles.
$\overline{WE}$	INPUT	**WRITE ENABLE** is active low and controls the write function of the command register to the memory array. The target address is latched on the falling edge of the $\overline{WE}$ pulse and the appropriate data is latched on the rising edge of the pulse.
V_{PP1},V_{PP2}		**ERASE/WRITE POWER SUPPLY** for erase and programming. V_{PP} enables the command register which controls all functions required to alter the memory array contents. **Note:** AmC002FLKA functions as a read-only memory when $V_{PP} < V_{CC} + 2$ V.
V_{CC}		**PC CARD POWER SUPPLY** for device operation (5.0 V ± 5%)
GND		**GROUND**
CD_1, CD_2	OUTPUT	**CARD DETECT.** When card detect 1 and 2 = ground the system detects the card.
WP	OUTPUT	**WRITE PROTECT** is active high and disables all card write operations.
NC		**NO CONNECT** - corresponding pin is not connected internally.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT.** Internally pulled-up.

MEMORY CARD OPERATIONS

The AmC002FLKA Flash Memory Card is organized as an array of individual devices. Each device is 256K bytes in size. Although the address space is continuous each physical device defines a logical address segment size. Erase operations are performed in increments of this segment size. Multiple segments may be erased concurrently when additional V_{PP} current is supplied to the device. Once a memory segment is erased any address location may be programmed. Flash technology allows any logical "1" data bit to be programmed to a logical "0". The only way to reset bits to a logical "1" is to erase the entire memory segment of 256K bytes. High voltage is required on V_{PP1} and V_{PP2} to perform program and erase operations.

The common memory space data contents are altered in a similar manner as writing to individual Flash Memory devices. On-card address and data buffers activate the appropriate Flash device in the memory array. Each device internally latches address and data during write cycles. Refer to Table 2A.

Attribute memory is a separately accessed card memory space. The register memory space is active when the $\overline{REG}$ pin is driven low. The Card Information Structure describes the capabilities and specification of a card. The CIS is stored in the attribute memory space beginning at address 00000H. The AmC002FLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. Alternatively, the CIS can be stored at the beginning of the common memory address space. D_0–D_7 are active during attribute memory accesses. D_8–D_{15} should be ignored. Odd order bytes present invalid data. Refer to Table 2B.

Word-Wide Operations

The AmC002FLKA provides the flexibility to operate on data in a byte-wide or word-wide format. In word-wide operations the Low-bytes are controlled with V_{PP1} and $\overline{CE}_1$ when A_0 = 0. The High-bytes are controlled with V_{PP2} and $\overline{CE}_2$, A_0 = don't care.

Erase operations are the only operations that work on entire memory segment. All other operations such as word-wide programming are not affected by the physical memory segments.

Byte-Wide Operations

Byte-wide data is available on D_0–D_7 for read and write operations ($\overline{CE}_1$ = low, $\overline{CE}_2$ = high). Even and odd bytes are stored in separate memory segments (i.e. S_0 and S_1) and are accessed when A0 is low and high respectively. The even byte is the low order byte and the odd byte is the high order byte of a 16-bit word.

Erase operations in the byte-wide mode must account for data multiplexing on D_0–D_7 by changing the state of A0. Each memory segment pair must be addressed separately for erase operations.

Card Detection

Each $\overline{CD}$ (output) pin should be read by the host system to determine if the memory card is adequately seated in the socket. $\overline{CD}_1$ and $\overline{CD}_2$ are internally tied to ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

Write Protection

The AMD Flash memory card has three types of write protection. The PCMCIA/JEIDA socket itself provides the first type of write protection. Power supply and control pins have specific pin lengths in order to protect the card with proper power supply sequencing in the case of hot insertion and removal.

A mechanical write protect switch provides a second type of write protection. When this switch is activated, $\overline{WE}$ is internally forced high. The Flash memory command register is disabled from accepting any write commands.

The third type of write protection is achieved with V_{pp1} and V_{pp2} at logic low levels to reset the Flash devices to read-only mode. Memory contents can not be changed in this state. The command register of individual Flash memory segments is only active when V_{pp1} and/or V_{pp2} are at high voltage (V_{ppH}).

Each Flash memory device that comprises a Flash memory segment will reset the command register to the read-only mode when V_{cc} is below VLKO. VLKO is the voltage below which write operations to individual command registers are disabled.

MEMORY CARD BUS OPERATIONS

Read Enable

Two Card Enable ($\overline{CE}$) pins are available on the memory card. Both $\overline{CE}$ pins must be active low for word-wide read accesses. Only one $\overline{CE}$ is required for byte-wide accesses. The $\overline{CE}$ pins control the selection and gates power to the high and low memory segments. The Output Enable ($\overline{OE}$) controls gating accessed data from the memory segment outputs.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state.

Standby Operations

Byte-wide read accesses only require half of the read/write output buffer (x16) to be active. In addition, only one memory segment is active with in either the high order or low order bank. Activation of the appropriate half of the output buffer is controlled by the combination of both $\overline{CE}$ pins. The $\overline{CE}$ pins also control power to the high and low-order banks of memory. Outputs of the memory bank not selected are placed in the high impedance state. The individual memory segment is activated by the address decoders. The other memory segments operate in standby. An active memory segment continues to draw power until completion of a write, erase, or verify operation if the card is de-selected in the process of one of these operations.

Auto Select Operation

A host system or external card reader/writer can determine the on-card manufacturer and device I.D. codes. Codes are available after writing the 90H command to the command register of a memory segment. Reading from address location 00000H in any segment provides the manufacturer I.D. while address location 00002H provides the device I.D.

Write Operations

Write and erase operations are valid only when V_{pp1} and V_{pp2} are at high voltage. This activates the state machine of an addressed memory segment. The command register is a latch which saves address, commands, and data information used by the state machine and memory array.

When Write Enable ($\overline{WE}$) and appropriate $\overline{CE}$(s) are a logic-level low, the command register is enabled for write operations. The falling edge of $\overline{WE}$ latches address information and the rising edge latches data/command information.

Memory Segment Command Definitions

When the V_{pp} pin(s) are at low voltage the command register of each Flash memory segment defaults to 00H, the Read only mode.

With high voltage on the V_{pp} pin(s), the Flash memory segments are active for either read, write, or erase operations.

Write or erase operations are performed by writing appropriate data patterns to the command register of accessed Flash memory segments.

The byte-wide and word-wide commands are defined in Tables 3 and 4 respectively.

Table 2A. Common Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Note 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Note 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Note 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	High Z
Read (x16) (Note 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	Data Out-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Notes 2, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Data Out-Odd	High Z
Read (x16) (Notes 2, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Data Out-Odd	Data Out-Even
Write (x8) (Notes 4, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data In-Odd
Write (x8) (Notes 4, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Data In	High Z
Write (x16) (Note 5, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Data In-Odd	Data In-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, $V_{CC} + 2$ V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a Byte write operation.
5. Refer to Table 4 for valid D_{IN} during a Word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. Byte access – Even. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Byte access – Odd. In this x8 mode, $A_0 = V_{IH}$ outputs or inputs the "odd" byte (high byte) of the x16 word on D_0–D_7. This is accomplished internal to the card by transposing D_8–D_{15} to D_0–D_7.
9. Odd byte only access. In this x8 mode, A_0 = X outputs or inputs the "odd" byte (high byte) of the x16 word on D_8–D_{15}.
10. x16 word accesses present both "even" (low) and "odd" (high) bytes. $A_0 = V_{IL}$ or V_{IH} = "Don't Care".

Table 2B. Attribute Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Notes 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Not Valid
Read (x8) (Note 8)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	High Z
Read (x16) (Notes 8, 9, 10)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	Data Out-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Read (x8) (Note 9)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Read (x16) (Notes 2, 9)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Not Valid	Data Out-Even
Write (x8) (Notes 4, 7, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Write (x8) (Notes 4, 9, 10)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Write (x16) (Note 10)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Not Valid	Data In-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, $V_{CC} + 2$ V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a Byte write operation.
5. Refer to Table 4 for valid D_{IN} during a Word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Only even-byte data is valid during Attribute Memory Read function.
9. During Attribute Memory Read function, $\overline{REG}$ and $\overline{OE}$ must be active for the entire cycle.
10. During Attribute Memory Write fuction, $\overline{REG}$ and $\overline{WE}$ must be active for the entire cycle, $\overline{OE}$ must be inactive for the entire cycle.

Table 3. Command Definitions for Byte-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	90H	Read	00H/01H	01H/2AH
Erase Set-up/Erase (Note 4)	Write	SA	20H	Write	SA	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figures 1, 3 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section
   Address: 00H/01H = Address for manufacturer code/Device code.
   Data: 01H/2AH = Data for manufacturer code/Device code

Table 4. Command Definitions for Word-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	0000H/ FFFFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	9090H	Read	0000H/ 0101H	0101H/ 2A2AH
Erase Set-up/Erase (Note 4)	Write	SA	2020H	Write	SA	2020H
Erase-Verify (Note 4)	Write	EA	A0A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	4040H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFFFH	Write	X	FFFFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figures 1, 3 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

Details of AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-up is the first of a two-cycle erase command. It is a command-only operation that stages the addressed memory segment for bulk erase. The array contents are not altered with this command. 20H is written to the command register (2020H for word-wide) in order to perform the erase Set-up operation.

Erase

The second two-cycle erase command initiates the segment erase operation. You must write the Erase command 20H (2020H for word-wide) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, segment erasure can only occur when high voltage is applied to the V_{PP} pins. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase operation erases all bytes of the segment in parallel. After the erase operation, all bytes in the segment must be sequentially verified. For byte-wide operations, the A_0 signal selects between the odd and even byte banks within the memory segment. Erase and erase-verify operations must be performed in completion on the even byte segment of 256K byte then the odd byte segment of 256K byte. The Erase-verify operation is initiated by writing A0H (A0A0H for word-wide) to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the segment applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte (FFFFH for word-wide) indicates that all bits in the byte (word) are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte (word) in the memory segment until a byte (word) does not return FFH (FFFFH) data or all the bytes in the segment are accessed and verified.

If an address is not verified to FFH (FFFFH) data, the segment is erased again (refer to erase Set-up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The segment is now ready to be programmed. The verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figures 1 and 3 and Table 6, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Flasherase Electrical Erase Algorithm

This Flash memory segment erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the accessed memory segment. Erasure begins with a read of the memory contents. Reading FFH (FFFFH for word-wide) data from the segment would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

Should the segment be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the segment to their charged state (Data = 00H or 0000H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH or FFFFH) begins at address 00000H and continues through the array to the last address, or until data other than FFH (FFFFH) is encountered. For byte-wide erase operations, the A_0 signal selects between the odd and even byte banks within the memory segment. Each bank must be operated on individually and completely in verify operations. If a byte (word) fails to verify, the device is erased again. With each erase operation, an increasing number of bytes (words) verify to the erased state. Typically, devices are erased in less than 70 pulses. Erase efficiency may be improved by storing the address of the last byte (word) that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. When all bytes within an accessed segment are erased, additional segments may be erased by following the same routine. Memory segments are typically erased in less than two seconds. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin.

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The AmC002FLKA is programmed byte by byte (or word by word). Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the addressed memory segment for byte programming. The Set-up Program operation is performed by writing 40H (4040H for word-wide) to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte (word) just programmed must be verified.

Write C0H (C0C0H) into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte (word) programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the memory segment applies an internally generated margin voltage to the addressed byte (word). A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte (word) was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte (word) location. Should the byte (word) fail to verify, reprogram the byte (word) using the Program Set-up/Program Commands. Figure 2 and Table 5 indicate how instructions are combined with the bus operations to perform byte (word) programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

The reset command initializes the memory segment to the read mode. In addition, it also provides a safe method to abort any memory segment operation (including program or erase). The reset command must be written two consecutive times after the program set-up command. This will safely reset the segment memory to the read mode. Memory contents are not altered. Following any other command, write the reset command once to the segment. This will safely abort any operation and reset the device to the Read mode.

Flashrite Programming Algorithm

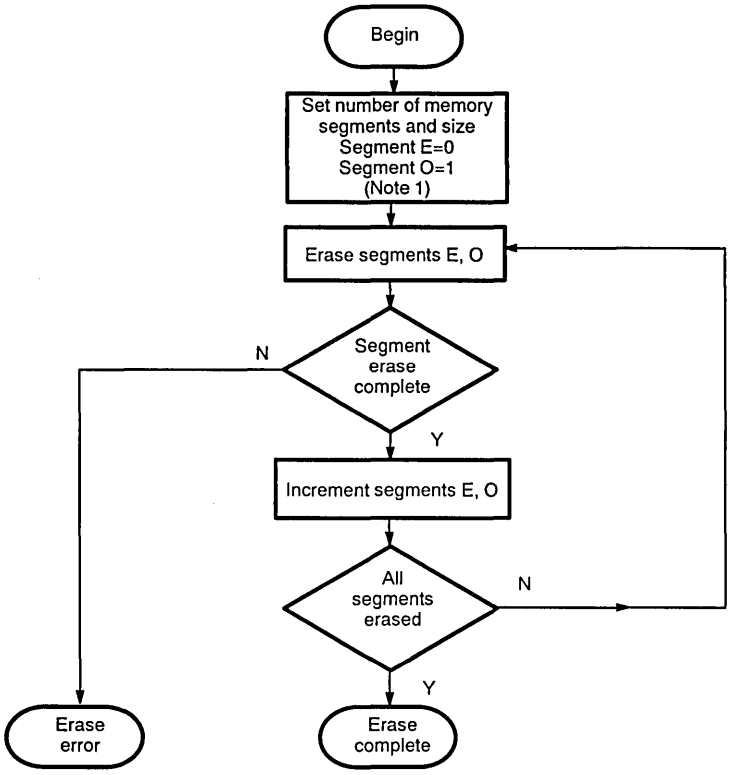
The Flashrite Programming algorithm employs an interactive closed loop flow to program data. Bytes or words may be programmed sequentially or at random using 10 microsecond programming pulses. Each operation is followed by a byte or word verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte or word per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte or word verification is performed with high voltage applied to the V_{PP} pin. Figure 2 and Table 5 illustrate the programming algorithm.

Auto Select

The Auto Select mode allows the reading out of a binary code from the memory devices to identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

MEMORY CARD ERASE ROUTINE

Overview



Note:
1. E = Even byte, O = Odd byte.

Figure 1.

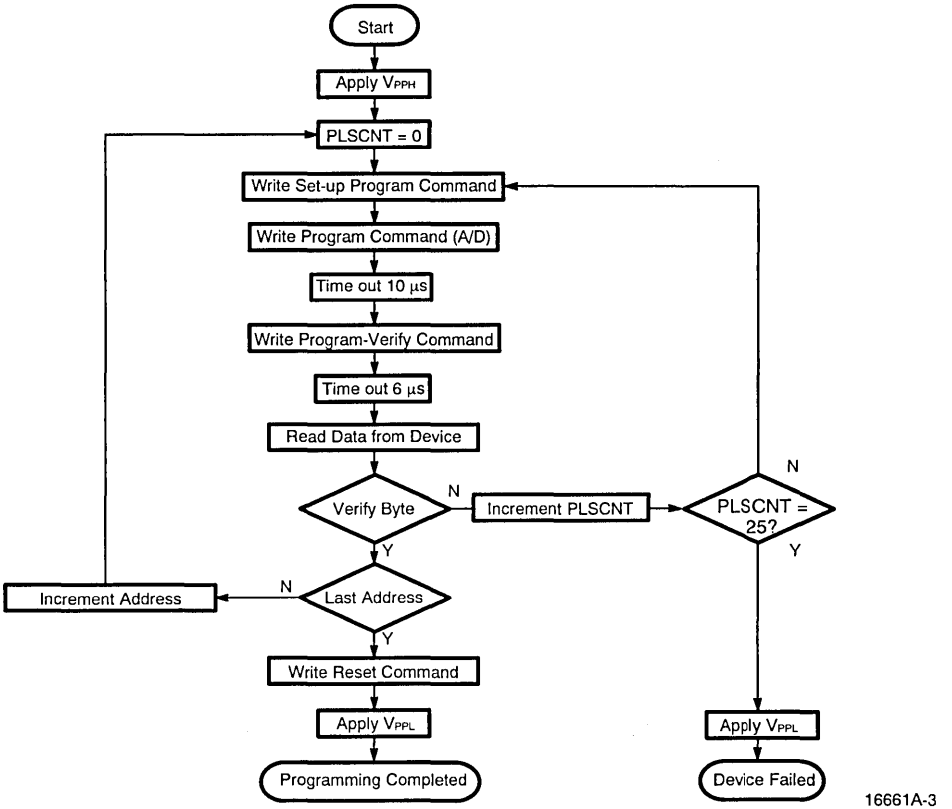


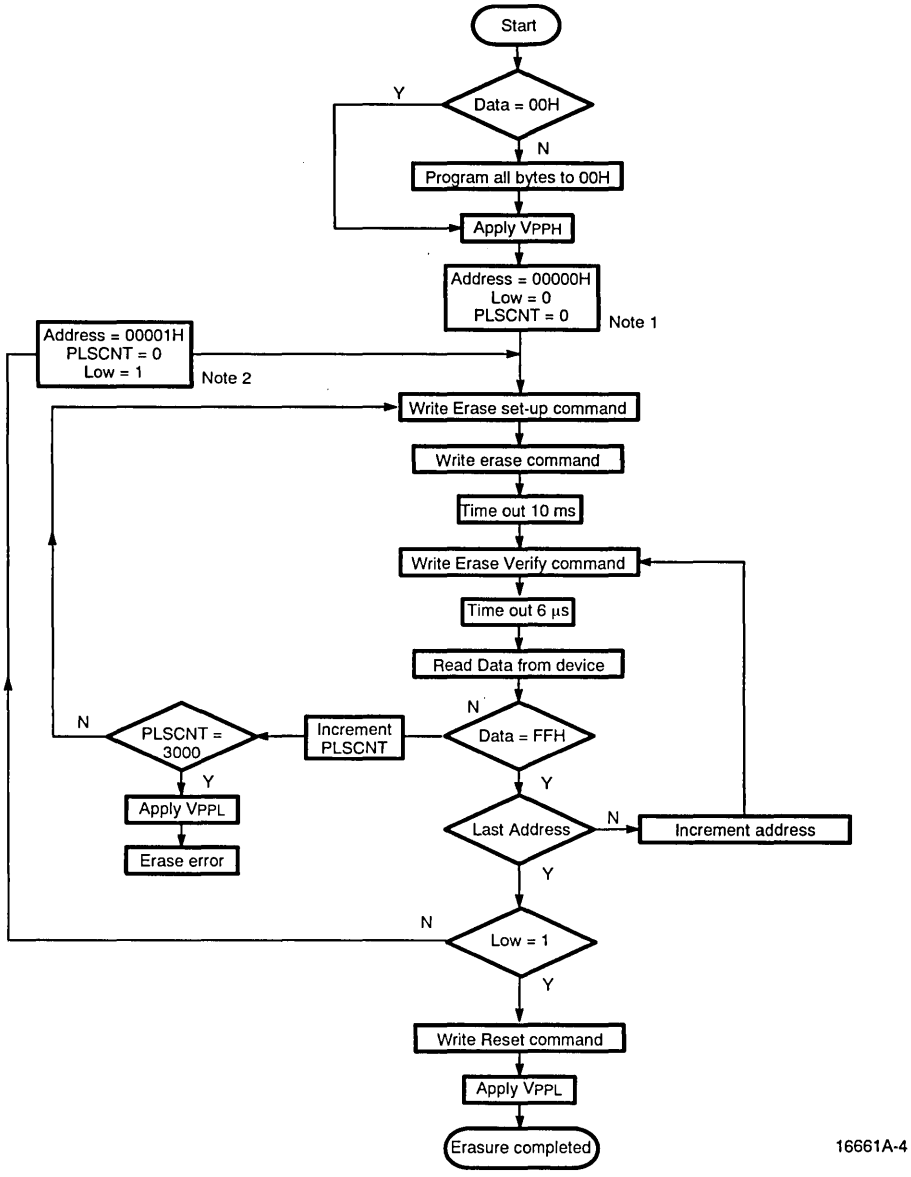
Figure 2. Flashrite Programming Algorithm in Byte-Wide Mode

Table 5. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



Notes:

1. Low = 0: Even byte segment Erase/Erase verify operation.
2. Low = 1: Odd byte segment Erase/Erase verify operation.

Figure 3. Flasherase Electrical Erase Algorithm in Byte-Wide Mode

Table 6. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.

WORD-WIDE PROGRAMMING

The program sequence will be followed as usual. The program word command is 4040H. Each device is independently verified. When one of the program flags is active, indicating that a particular device has successfully completed programming, the software should change the command for that device from Program to Reset and from program verify to Reset. The software should also change the Program Data to the null data set (FFH). This effectively masks the programmed device from further programming.

Should the high order byte device verify first, the next program command will be FF40H. The low order byte device programs on each subsequent program command until verified. The high order byte device remains in Reset/Read mode. During verification, write the program verify command of FFC0H. This will enable the low order byte device for verify operations and maintains the programmed high order byte device in Reset/Read mode.

WORD-WIDE PROGRAMMING
Overview

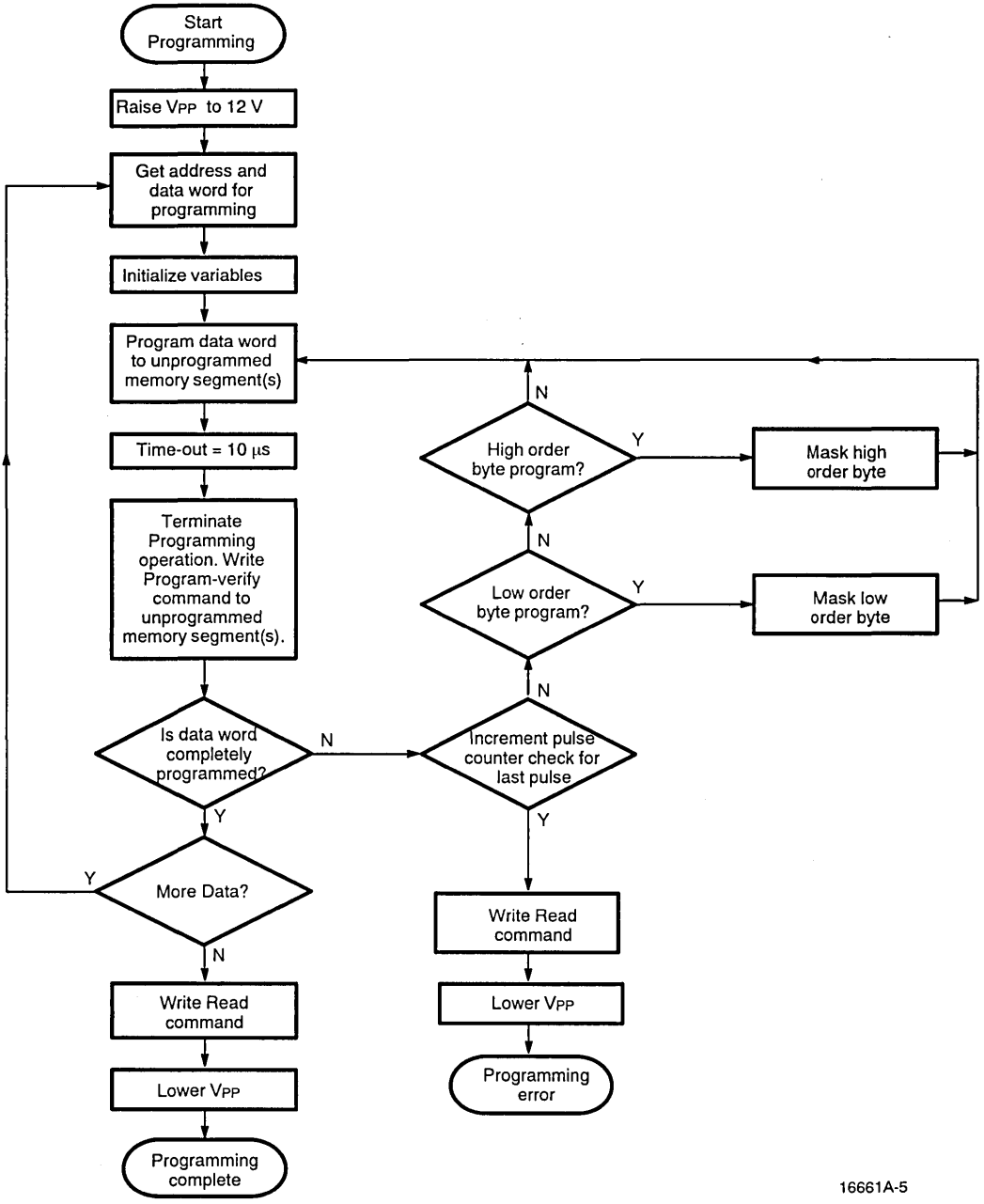
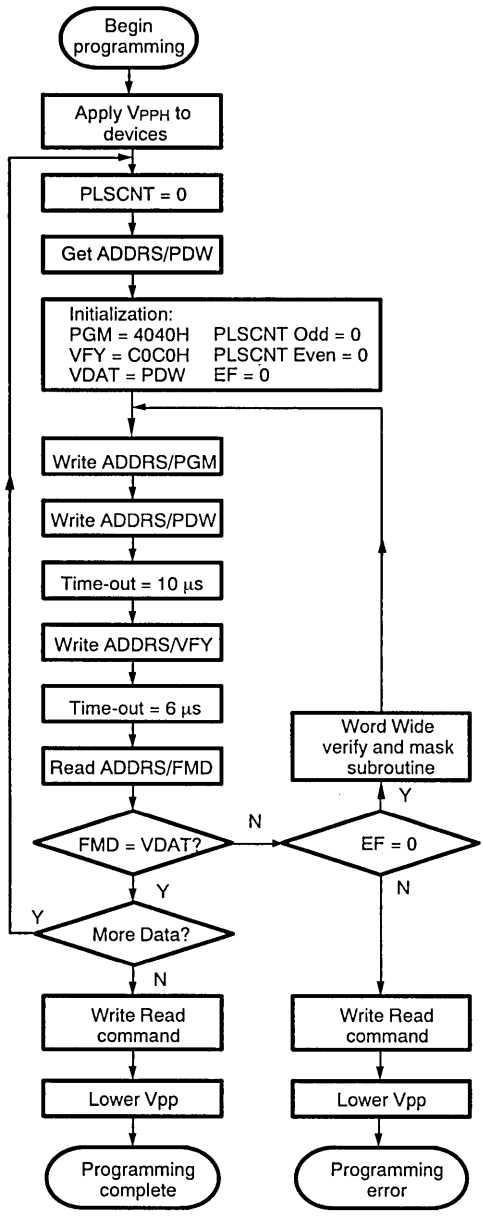


Figure 4.

WORD-WIDE PROGRAMMING FLOW CHART



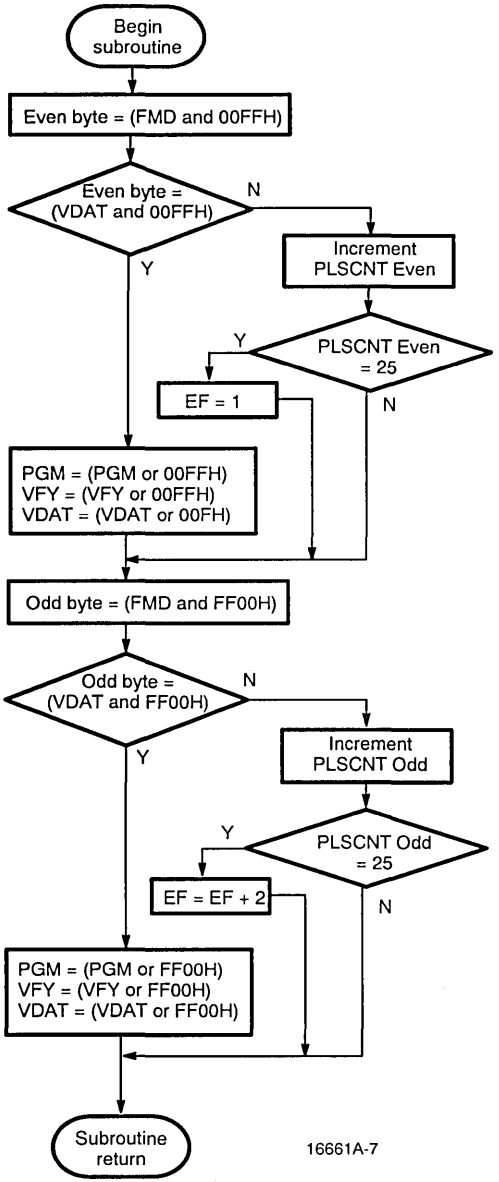
16661A-6

Note:
Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any device from programming operations.

Activity
Allow V_{PP} to stabilize.
PLSCNT = Pulse Counter.
ADDRS = Word Address to program. *PDW = Data Word to program.*
Initialize Programming Variables: *PGM = Program Command* *VFY = Program-verify Command* *VDAT = Valid Data* *PLSCNT Odd = Pulse count for odd (high) byte* *PLSCNT Even = Pulse count for even (low) byte* *EF = Error Flag for write*
ADDRS = Address do not care. *Write Program Set-up command.*
Appropriate address and data for programming.
Duration of programming pulse.
Program-verify command terminates the programming pulse.
Internal margin verify voltages are tapped from external 12 V V_{PP} for proper byte verification.
Read from previously latched address. FMD = Flash Memory Data.
See Word Wide Programming subroutine. Each device is independently verified. The Program command is masked by the Reset command (FFH) for all devices that are completely Programmed. Please see note below.
Compare Flash Memory Data to valid word data. If verified, reset PLSCNT and get next address and data word for programming. If not last pulse, compare high order byte device and low order byte device for valid byte data.
Reset devices for read operation.
V_{PPL} deactivates command register. Device is in Read Only Mode.

Figure 5.

WORD-WIDE PROGRAMMING VERIFY SUBROUTINE



Commentary

This subroutine verifies the high order (odd) and low order (even) bytes independently. If either byte verifies, all commands are masked to that device.

Mask the odd byte to look at the even byte.

If the even byte doesn't verify, increment pulse count and continue of program even byte.
EF = Error Flag

Mask the even byte commands and program data if it verifies.

Mask the even byte to look at the odd byte.

If the odd byte doesn't verify, increment pulse count and continue to program odd byte.

Mask the odd byte commands and program data if it verifies.

Error Flag Summary:

EF = 0 indicates no program error
EF = 1 indicates even byte program error
EF = 2 indicates odd byte program error
EF = 3 indicates both even and odd byte program error

Figure 6.

WORD-WIDE ERASING

Overview

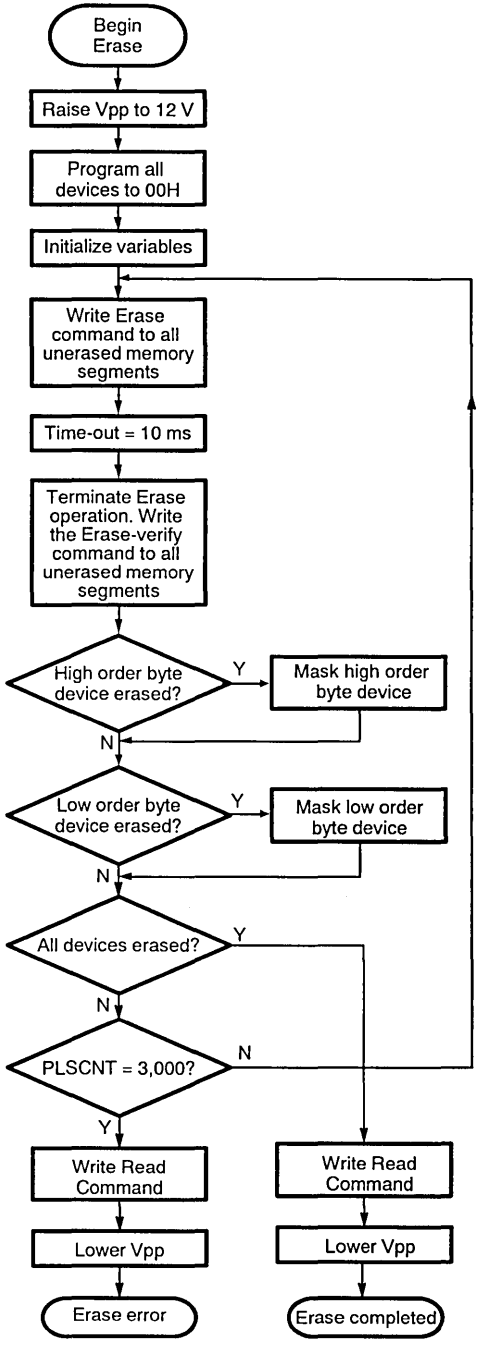
Word-Wide Erasure

Word-wide erasure reduces total erase time when compared to erasing each byte individually. Each Flash memory may erase at different rates. Therefore each device must be verified separately after every erase pulse. Once a device has successfully completed erasure, do not issue the erase command again to that device. Issue the Reset command FFH to the erased device. The Erase command sequence may be issued to each of the remaining devices that have not erased yet. In addition to the address verify register required for each device, you will need an erase complete flag for each device.

Word-Wide

The erase sequence will be followed as usual. The CPU will issue word commands. The erase word command is 2020H. Each device is independently verified and the address of the last verified byte per device is stored in separate registers. When one of the erase flags is active, indicating that a particular device has successfully completed erasure, the CPU will change the command for that device from Erase to Reset. This effectively masks the erased device from further erasure.

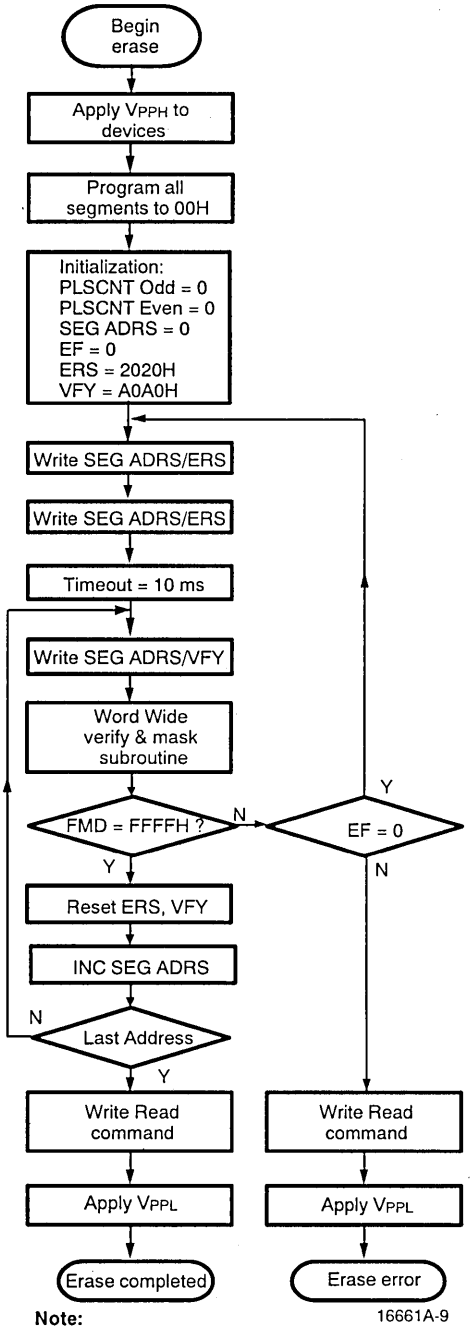
Should the high order byte device verify first, the next erase command will be FF20H. The low order byte device erases on each subsequent erase command until verified. The high order byte device remains in Reset/Read mode. During verification, write the erase verify command of FFA0H. This will enable the low order byte device for verify operations and maintains the erased high order byte device in the Reset/Read mode.



16661A-8

Figure 7.

WORD-WIDE ERASURE FLOW CHART



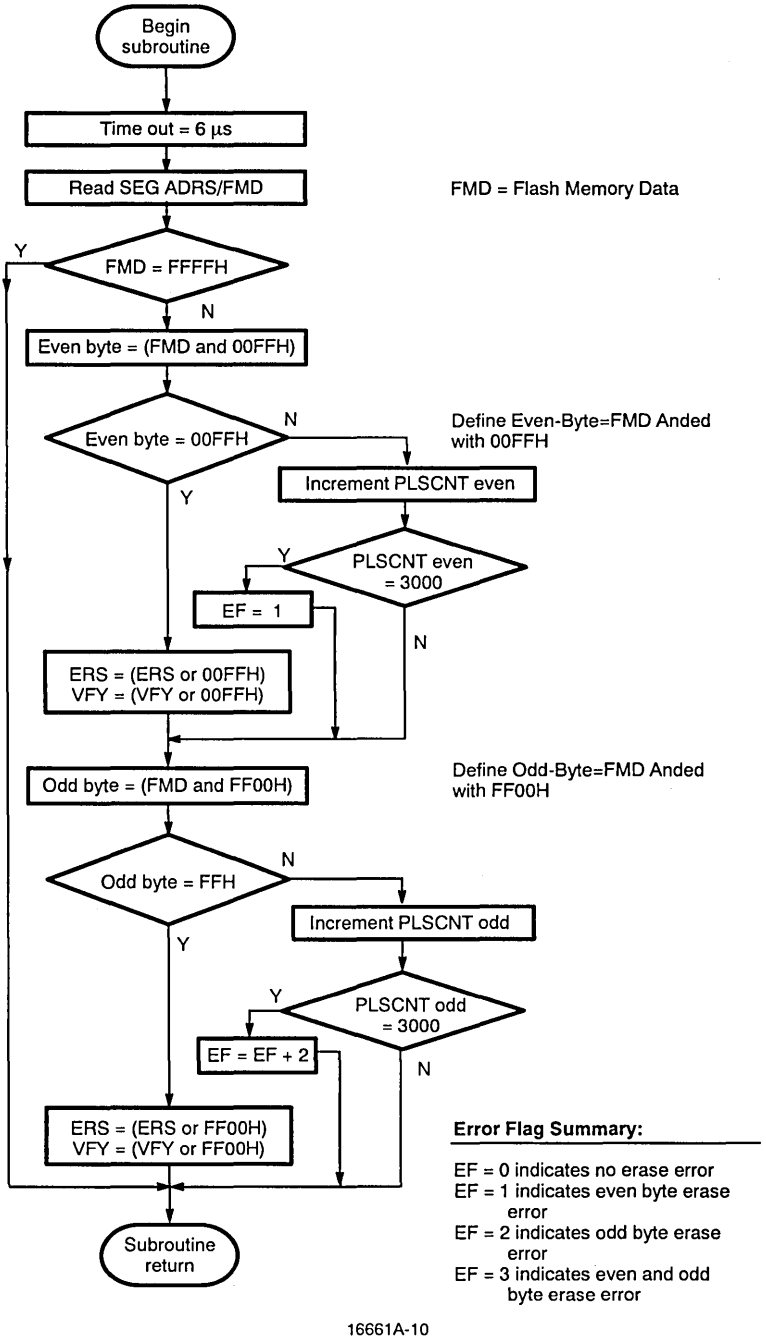
16661A-9

Activity	
Begin erase	
Apply V_{PPH} to devices	*Allow V_{PP} to stabilize.*
Program all segments to 00H	*Follow Flashrite programming algorithm.*
Initialization: PLSCNT Odd = 0 PLSCNT Even = 0 SEG ADRS = 0 EF = 0 ERS = 2020H VFY = A0A0H	*Initialize Erase Variables:* *PLSCNT Odd = Pulse count for odd (high) byte* *PLSCNT Even = Pulse count for even (low) byte* *SEG ADRS = Address* *EF = Error Flag for error* *ERS = Erase Command* *VFY = Erase-verify Command*
Write SEG ADRS/ERS	*Write Program Set-up command.*
Write SEG ADRS/ERS	*Initiate erase pulse.*
Timeout = 10 ms	*Duration of programming pulse.*
Write SEG ADRS/VFY	*Erase-verify command terminates the erase pulse.*
Word Wide verify & mask subroutine	*See Word Wide Erasure subroutine. Each device is independently verified. The command is masked by the Reset command (FFH) for all devices that are completely erased. Please see note below.*
FMD = FFFFH ? / EF = 0	*FMD = FFFFH when memory segment at SEG ADRS is erased.*
Reset ERS, VFY	*Reset devices for read operation.*
INC SEG ADRS / Last Address	
Write Read command	
Apply V_{PPL}	*V_{PPL} deactivates command register. Device is in the Read Only Mode.*
Erase completed / Erase error	

Note:
Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any completely erased device from further erase operations.

Figure 8.

WORD-WIDE ERASE VERIFY SUBROUTINE



16661A-10

Figure 9.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −30°C to +70°C

Ambient Temperature
with Power Applied ..... −10°C to +70°C

Voltage with Respect to Ground
All pins except V_{PP} (Note 1) ..... −2.0 V to +7.0 V

V_{CC} (Note 1) ..... −2.0 V to +7.0 V

V_{PP} (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5 V. During voltage transitions, outputs may overshoot to V_{CC} +2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on V_{PP} pins is −0.5 V. During voltage transitions, V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = V_{CC} max. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +60°C

V_{CC} Supply Voltages ..... +4.75 V to 5.25 V

V_{PP} Supply Voltages

Read Only ..... 0 V to +6.5 V

Program, Erase, Verify,
and Read ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Byte Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ±0.2 V		0.4	0.8	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		25	50	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		3.0	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		5.0	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			10	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.2	0.4	mA
		$V_{PP} \leq V_{CC}$			0.04	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		8.0	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. One Flash device active, seven in standby.
2. Only one Vpp is active.

DC CHARACTERISTICS
Word-Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. CE = V_{CC} ±0.2 V		0.4	0.8	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., CE = V_{IL}, OE = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		40	80	mA
I_{CC2}	V_{CC} Programming Current	CE = V_{IL} Programming in Progress		6	60	mA
I_{CC3}	V_{CC} Erase Current	CE = V_{IL} Erasure in Progress		10	60	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			10	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.4	0.8	mA
		$V_{PP} \leq V_{CC}$			0.08	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		16	60	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		20	60	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = 2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. Two Flash devices active, six in standby.
2. V_{pp1} and V_{pp2} are active.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Capacitance	V_{IN} = 0		21	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		21	pF
C_{IN2}	Control Capacitance	V_{IN} = 0 ($\overline{CE}$, $\overline{REG}$)		47	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = 0		21	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING AC CHARACTERISTICS

Read Only Operation (Note 1)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{RC}	Read Cycle Time	250		ns
t_{ELQV}	t_{CE}	Chip Enable Access Time		250	ns
t_{AVQV}	t_{ACC}	Address Access Time		250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time		150	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	5		ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z		60	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z		60	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
t_{WHGL}		Write Recovery Time before Read	6		µs

Note:

1. Input Rise and Fall Times (10% to 90%): ≤ 10 ns, Input Pulse levels: V_{OL} and V_{OH}, Timing Measurement Reference Level – Inputs: V_{IL} and V_{IH} Outputs: V_{IL} and V_{IH}

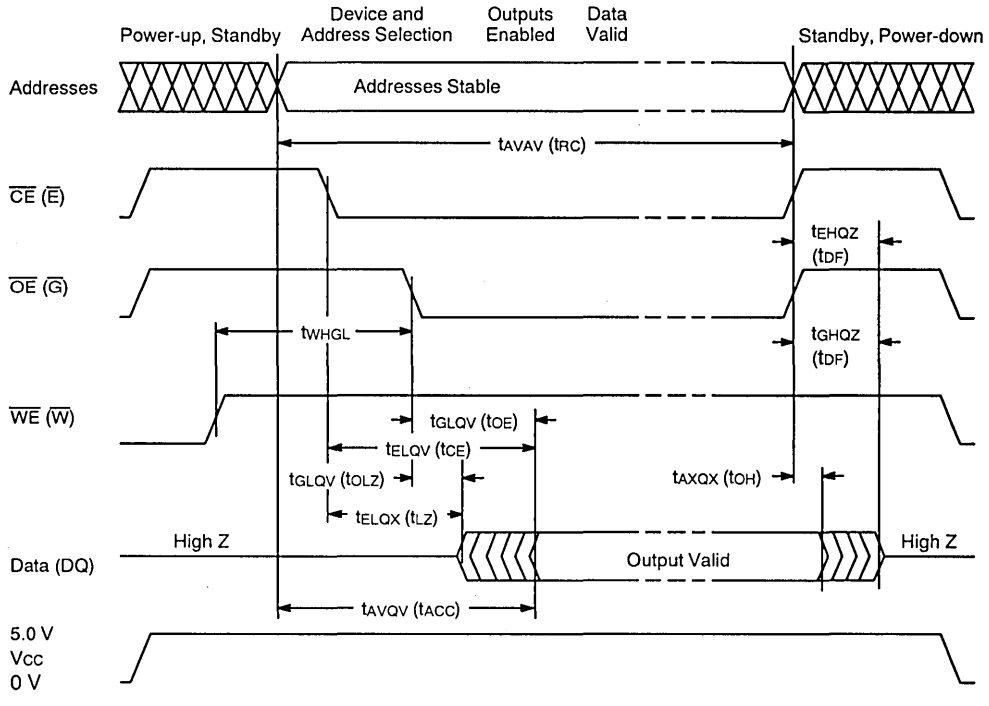
AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVWL}	t_{AS}	Address Set-Up Time	0		ns
t_{WLAX}	t_{AH}	Address Hold Time	100		ns
t_{DVWH}	t_{DS}	Data Set-Up Time	80		ns
t_{WHDX}	t_{DH}	Data Hold Time	30		ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHWL}		Read Recovery Time before Write	0		µs
t_{WLOZ}		Output in High-Z from Write Enable	5		ns
t_{WHOZ}		Output in Low-Z from Write Enable		60	ns
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	40		ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	100		ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	50		ns
t_{WHWH1}		Duration of Programming Operation (Notes 1, 2)	10		µs
t_{WHWH2}		Duration of Erase Operation (Notes 1, 2)	9.5		ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	100		ns

Notes:

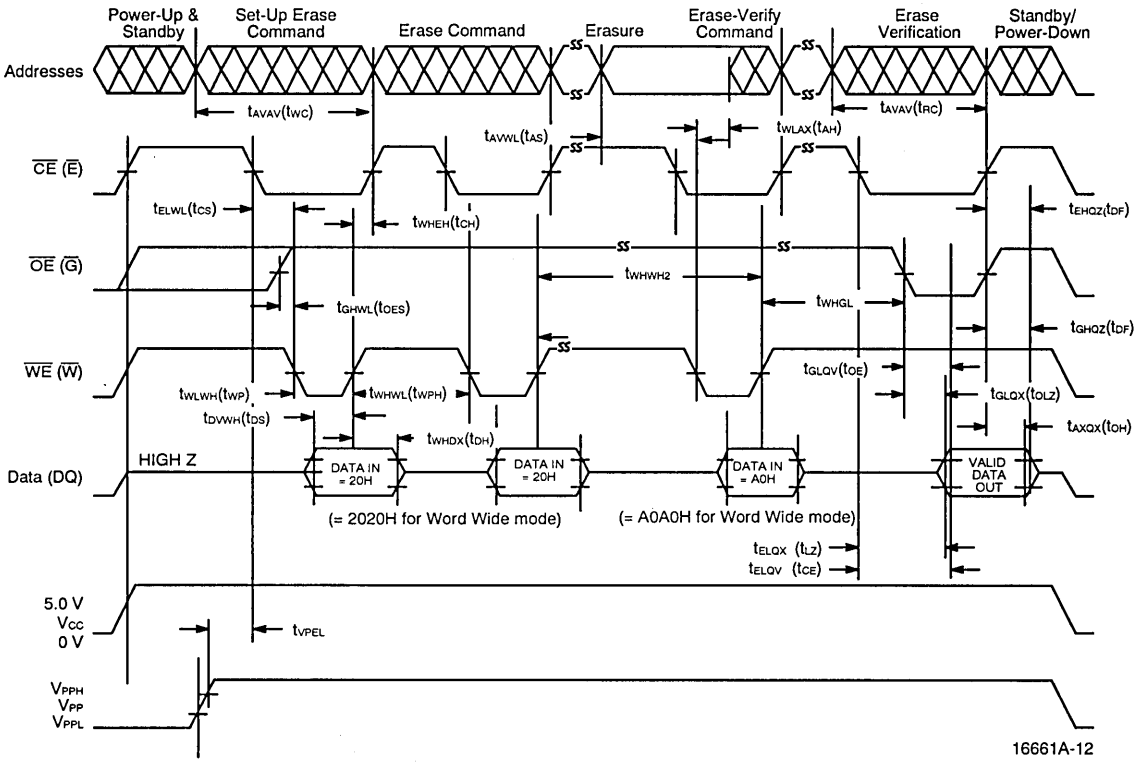
1. Rise/Fall < = 10 ns.
2. Maximum specification not needed due to the devices internal stop timer that will stop any erase or write operation that exceed the device specification.



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

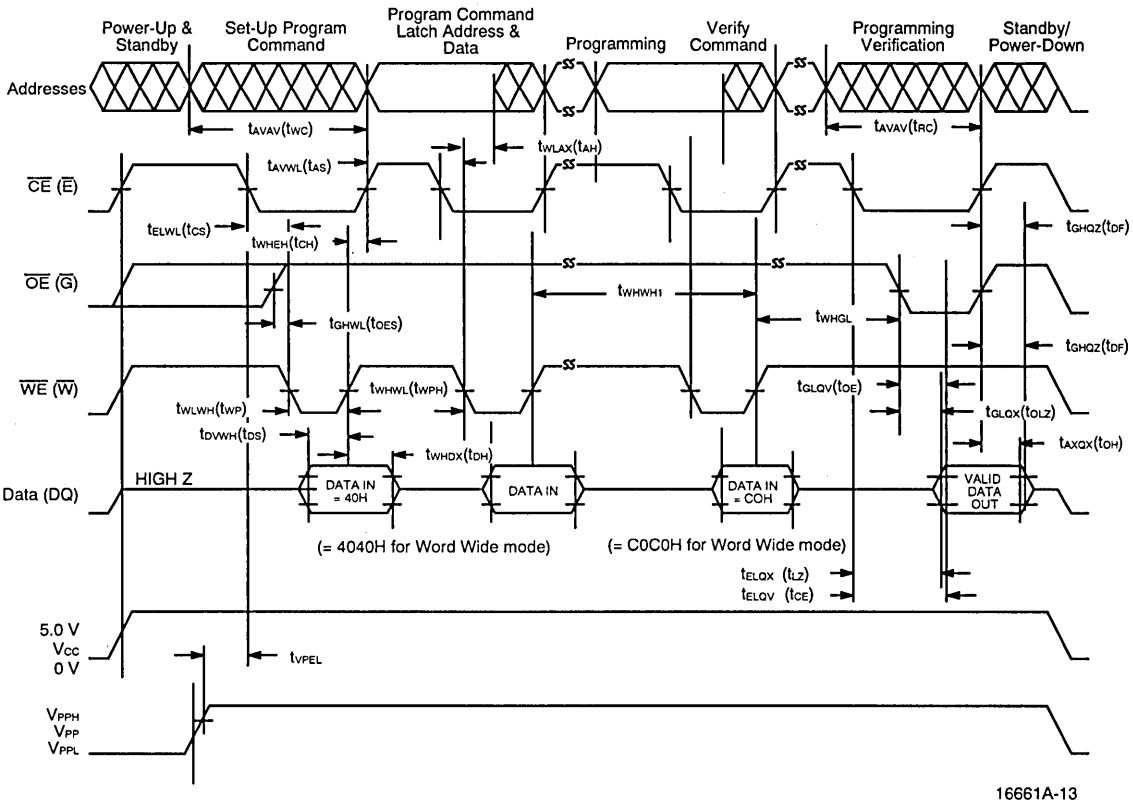
16661A-11

Figure 10. AC Waveforms for Read Operations



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

Figure 11. AC Waveforms for Erase Operations



16661A-13

Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

Figure 12. AC Waveforms for Programming Operations

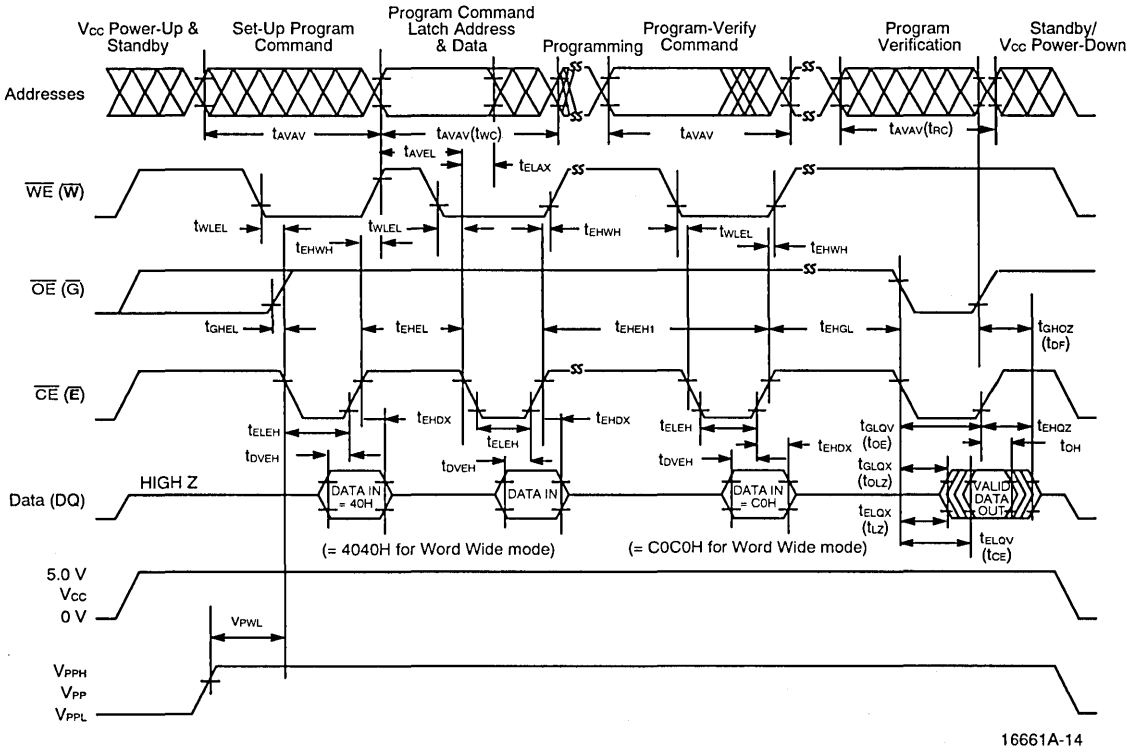
AC CHARACTERISTICS–ALTERNATE $\overline{CE}$ CONTROLLED WRITES

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVEL}	t_{AS}	Address Set-Up Time	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	100		ns
t_{DVEH}	t_{DS}	Data Set-Up Time	80		ns
t_{EHDX}	t_{DH}	Data Hold Time	30		ns
t_{EHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHEL}		Read Recovery Time before Write	0		µs
t_{WLEL}	t_{WS}	WE Set-Up Time before $\overline{CE}$	0		ns
t_{EHWH}	t_{CP}	WE Hold Time	0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	100		ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH (Note 3)	50		ns
t_{EHEH1}		Duration of Programming Operation (Notes 1, 2)	10		µs
t_{EHEH2}		Duration of Erase Operation (Notes 1, 2)	9.5		ms
t_{VPWL}		V_{PP} Set-Up Time to Write Enable LOW	100		ns

Notes:

1. Rise/Fall <=10 ns
2. Maximum specification not needed due to the internal stop timer that will stop any erase or write operation that exist the device specification.
3. Chip Enable Controlled Programming:
   Flash Programming is controlled by the valid combination of the Chip Enable ($\overline{CE}_{1,2}$) and Write Enable ($\overline{WE}$) signals. For system that uses the Chip Enable signal(s) to define the write pulse width, all Set-up, Hold, and inactive Write Enable timing should be measured relative to the Chip Enable signal(s).



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

Figure 13. Alternate AC Waveforms for $\overline{CE}$ Controlled Programming Operations

CARD INFORMATION STRUCTURE

The AmC001FLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. All or part of the 512 byte could be used for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space. Part of the common memory space could also be mapped into the attribute memory space if more than 512 bytes of CIS are needed.

The EEPROM used in the AmC002FLKA is a NEC μPD28C05GX-20-EJA designed to operate from a 5 V single power supply. The μPD28C05 provides a DATA polling function that provides the End of Write Cycle, Chip Erase and Auto Erase and Programming functions.

SYSTEM DESIGN AND INTERFACE INFORMATION

Power Up and Power Down Protection

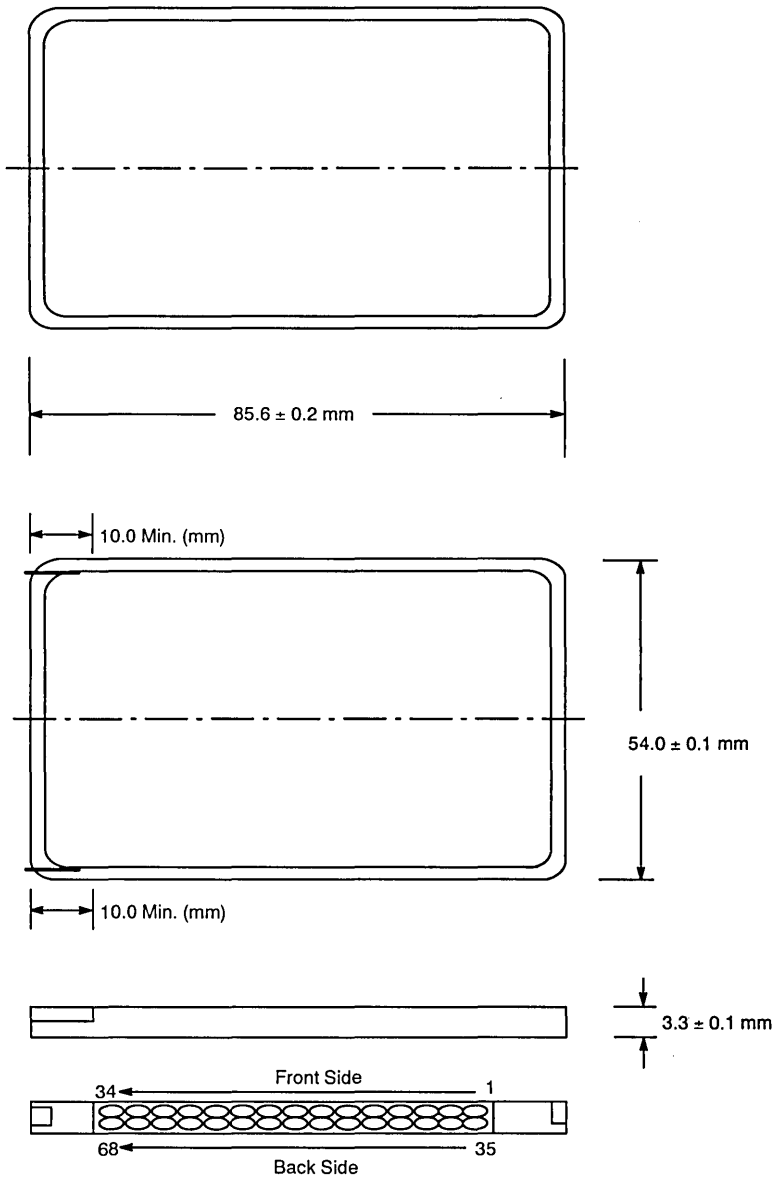
The PCMCIA standard socket provides for proper power up and power down sequencing via different pin lengths to ensure that hot insertion and removal of the PC card will not result in card damage or data loss.

AMD's Flash memory devices are designed to protect against accidental programming or erasure caused by spurious system signals that might exist during hot insertion, hot removal, or power transitions. The AMD PC card will power-up into a READ mode and the card will function as a read only memory as long as V_{pp} is less than V_{cc} +2 V. Erasing of the memory segments can be accomplished only by writing the proper Erase command to the card twice along with the proper Chip Enable, Output Enable and Write Enable control signals.

System Power Supply Decoupling

The AMD Flash memory card has a 0.1 μF decoupling capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins. It is recommended the system side also have a 4.7 μF capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins.

PHYSICAL DIMENSIONS
Type 1 PC Card



16661A-15

PRELIMINARY

AmC004FLKA

4 Megabyte Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 250 ns maximum access time
- **CMOS low power consumption**
  - 25 mA typical active current (X8)
  - 400 μA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **High re-programmable endurance**
  - Minimum 10,000 write/erase cycles
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate attribute memory**
  - 512 byte EEPROM
- **Flashrite™ and Flasherase™ Operations**
  - 256K byte memory segment
  - Typically two seconds per single memory segment erase
  - Random address writes to previously erased Bytes (10 μs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Read voltage, 5 V ± 5%**
- **Write and erase voltage, 12.0 V ± 5%**
- **Insertion and removal force**
  - State of art connector allows for minimum card insertion and removal effort
- **Manufactured by DuPont Connector Systems**

GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC004FLKA. This allows OEM manufacturers of portable system to eliminate the weight, extreme power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC004FLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC004FLKA enhances the productivity of mobile workers.

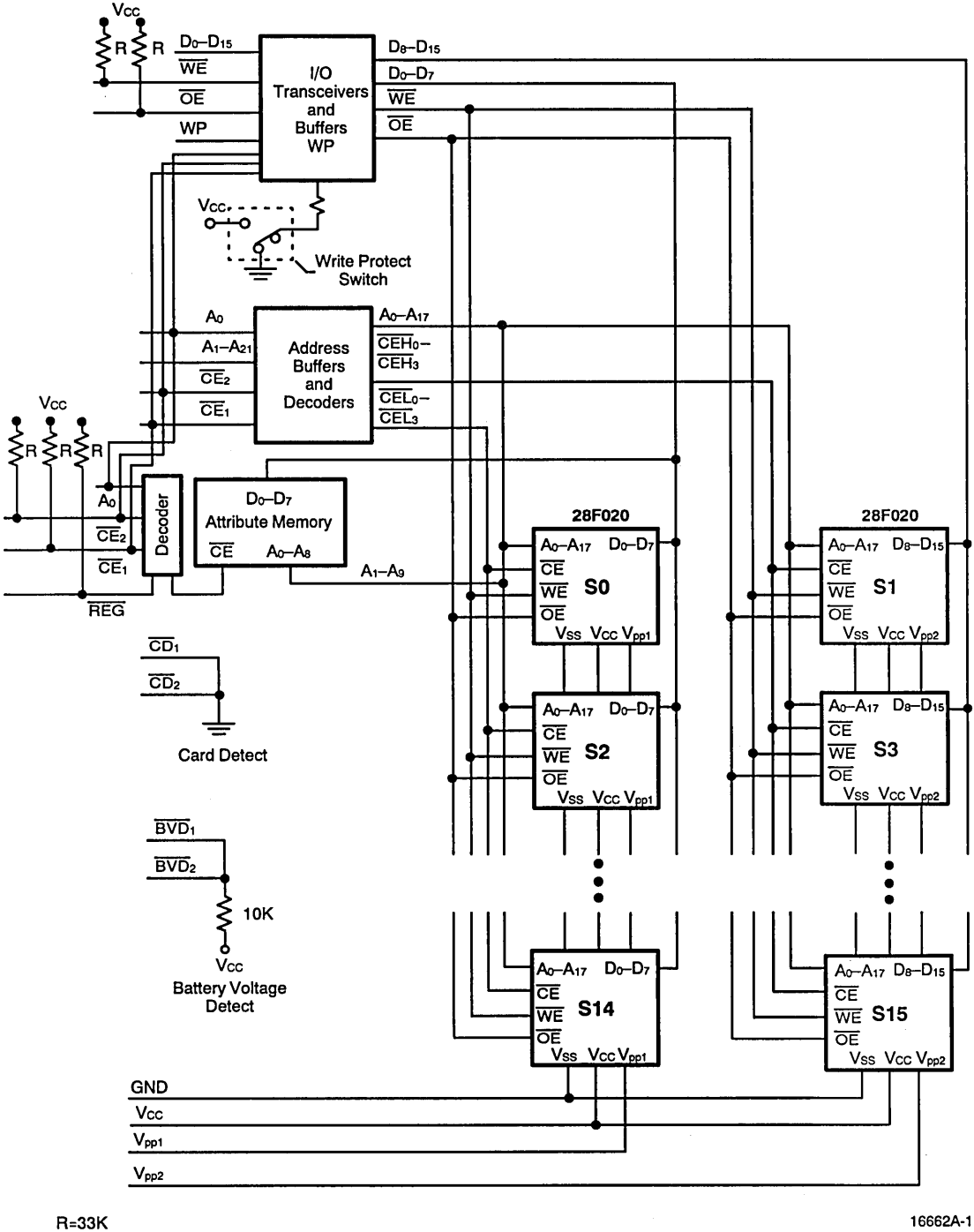
Widespread acceptance of the AmC004FLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC004FLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by DuPont Connector Systems

Publication# 16662 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



R=33K

16662A-1

PC CARD PIN ASSIGNMENTS

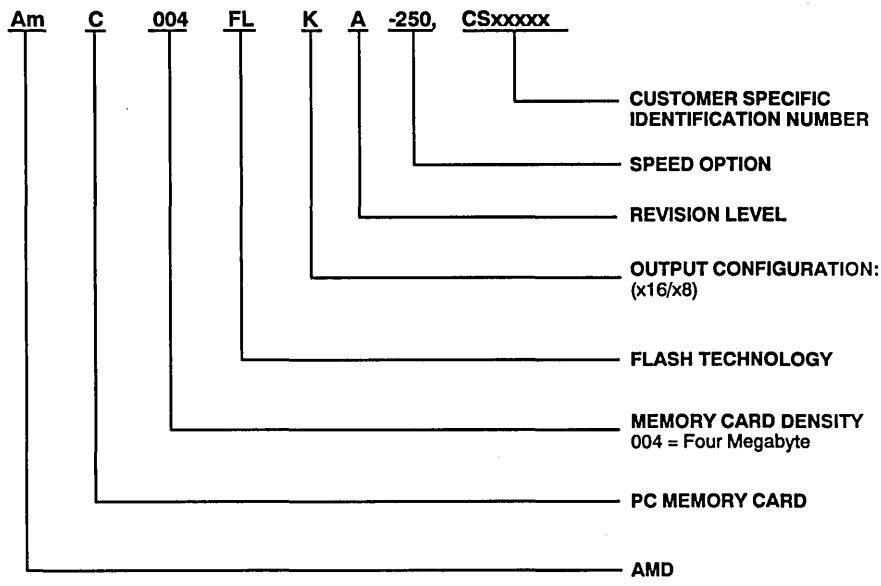
Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable (Note 1)	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2 (Note 1)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	RFU		Reserved
11	A_9	I	Address Bit 9	45	RFU		Reserved
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	A_{20}	I	Address Bit 20
16	NC		No Connect	50	A_{21}	I	Address Bit 21
17	V_{CC}		Power Supply	51	V_{CC}		Power Supply
18	V_{PP1}		Pgm Sply Vltg 1	52	V_{PP2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.
1. Signal must not be connected between cards
2. $\overline{BVD}$ = Internally pulled-up

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



PIN DESCRIPTION

Symbol	Type	Name and Function
$A_0 - A_{21}$	INPUT	**ADDRESS INPUTS** are internally latched during write cycles.
$D_0 - D_{15}$	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Data inputs are internally latched on write cycles. Data outputs during read cycles. Data pins are active high. When the memory card is de-selected or the outputs are disabled the outputs float to tri-state.
$\overline{CE_1}$, $\overline{CE_2}$	INPUT	**CARD ENABLE** is active low. The memory card is de-selected and power consumption is reduced to stand-by levels when $\overline{CE}$ is high. $\overline{CE}$ activates the internal memory card circuitry that controls the high and low byte control logic of the card, input buffers segment decoders, and associated memory devices.
$\overline{OE}$	INPUT	**OUTPUT ENABLE** is active low and enables the data buffers through the card outputs during read cycles.
$\overline{WE}$	INPUT	**WRITE ENABLE** is active low and controls the write function of the command register to the memory array. The target address is latched on the falling edge of the $\overline{WE}$ pulse and the appropriate data is latched on the rising edge of the pulse.
V_{PP1}, V_{PP2}		**ERASE/WRITE POWER SUPPLY** for erase and programming. V_{pp} enables the command register which controls all functions required to alter the memory array contents. **Note:** AmC004FLKA functions as a read-only memory when $V_{PP} < V_{cc} + 2$ V.
V_{cc}		**PC CARD POWER SUPPLY** for device operation (5.0 V ± 5%)
GND		**GROUND**
CD_1, CD_2	OUTPUT	**CARD DETECT.** When card detect 1 and 2 = ground the system detects the card.
WP	OUTPUT	**WRITE PROTECT** is active high and disables all card write operations.
NC		**NO CONNECT** - corresponding pin is not connected internally.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT.** Internally pulled-up.

MEMORY CARD OPERATIONS

The AmC004FLKA Flash Memory Card is organized as an array of individual devices. Each device is 256K bytes in size. Although the address space is continuous each physical device defines a logical address segment size. Erase operations are performed in increments of this segment size. Multiple segments may be erased concurrently when additional V_{pp} current is supplied to the device. Once a memory segment is erased any address location may be programmed. Flash technology allows any logical "1" data bit to be programmed to a logical "0". The only way to reset bits to a logical "1" is to erase the entire memory segment of 256K bytes. High voltage is required on V_{pp1} and V_{pp2} to perform program and erase operations.

The common memory space data contents are altered in a similar manner as writing to individual Flash Memory devices. On-card address and data buffers activate the appropriate Flash device in the memory array. Each device internally latches address and data during write cycles. Refer to Table 2A.

Attribute memory is a separately accessed card memory space. The register memory space is active when the $\overline{REG}$ pin is driven low. The Card Information Structure describes the capabilities and specification of a card. The CIS is stored in the attribute memory space beginning at address 00000H. The AmC004FLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. Alternatively, the CIS can be stored at the beginning of the common memory address space. D_0–D_7 are active during attribute memory accesses. D_8–D_{15} should be ignored. Odd order bytes present invalid data. Refer to Table 2B.

Word-Wide Operations

The AmC004FLKA provides the flexibility to operate on data in a byte-wide or word-wide format. In word-wide operations the Low-bytes are controlled with V_{pp1} and $\overline{CE_1}$ when A_0 = 0. The High-bytes are controlled with V_{pp2} and $\overline{CE_2}$, A_0 = don't care.

Erase operations are the only operations that work on entire memory segment. All other operations such as word-wide programming are not affected by the physical memory segments.

Byte-Wide Operations

Byte-wide data is available on D_0–D_7 for read and write operations ($\overline{CE_1}$ = low, $\overline{CE_2}$ = high). Even and odd bytes are stored in separate memory segments (i.e. S_0 and S_1) and are accessed when A0 is low and high respectively. The even byte is the low order byte and the odd byte is the high order byte of a 16-bit word.

Erase operations in the byte-wide mode must account for data multiplexing on D_0–D_7 by changing the state of A0. Each memory segment pair must be addressed separately for erase operations.

Card Detection

Each $\overline{CD}$ (output) pin should be read by the host system to determine if the memory card is adequately seated in the socket. $\overline{CD_1}$ and $\overline{CD_2}$ are internally tied to ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

Write Protection

The AMD Flash memory card has three types of write protection. The PCMCIA/JEIDA socket itself provides the first type of write protection. Power supply and control pins have specific pin lengths in order to protect the card with proper power supply sequencing in the case of hot insertion and removal.

A mechanical write protect switch provides a second type of write protection. When this switch is activated, $\overline{WE}$ is internally forced high. The Flash memory command register is disabled from accepting any write commands.

The third type of write protection is achieved with V_{pp1} and V_{pp2} at logic low levels to reset the Flash devices to read-only mode. Memory contents can not be changed in this state. The command register of individual Flash memory segments is only active when V_{pp1} and/or V_{pp2} are at high voltage (V_{ppH}).

Each Flash memory device that comprises a Flash memory segment will reset the command register to the read-only mode when V_{cc} is below VLKO. VLKO is the voltage below which write operations to individual command registers are disabled.

MEMORY CARD BUS OPERATIONS

Read Enable

Two Card Enable ($\overline{CE}$) pins are available on the memory card. Both $\overline{CE}$ pins must be active low for word-wide read accesses. Only one $\overline{CE}$ is required for byte-wide accesses. The $\overline{CE}$ pins control the selection and gates power to the high and low memory segments. The Output Enable ($\overline{OE}$) controls gating accessed data from the memory segment outputs.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state.

Standby Operations

Byte-wide read accesses only require half of the read/write output buffer (x16) to be active. In addition, only one memory segment is active with in either the high order or low order bank. Activation of the appropriate half of the output buffer is controlled by the combination of both $\overline{CE}$ pins. The $\overline{CE}$ pins also control power to the high and low-order banks of memory. Outputs of the memory bank not selected are placed in the high impedance state. The individual memory segment is activated by the address decoders. The other memory segments operate in standby. An active memory segment continues to draw power until completion of a write, erase, or verify operation if the card is de-selected in the process of one of these operations.

Auto Select Operation

A host system or external card reader/writer can determine the on-card manufacturer and device I.D. codes. Codes are available after writing the 90H command to the command register of a memory segment. Reading from address location 00000H in any segment provides the manufacturer I.D. while address location 00002H provides the device I.D.

Write Operations

Write and erase operations are valid only when V_{pp1} and V_{pp2} are at high voltage. This activates the state machine of an addressed memory segment. The command register is a latch which saves address, commands, and data information used by the state machine and memory array.

When Write Enable ($\overline{WE}$) and appropriate $\overline{CE}$(s) are a logic-level low, the command register is enabled for write operations. The falling edge of $\overline{WE}$ latches address information and the rising edge latches data/command information.

Memory Segment Command Definitions

When the V_{pp} pin(s) are at low voltage the command register of each Flash memory segment defaults to 00H, the Read only mode.

With high voltage on the V_{pp} pin(s), the Flash memory segments are active for either read, write, or erase operations.

Write or erase operations are performed by writing appropriate data patterns to the command register of accessed Flash memory segments.

The byte-wide and word-wide commands are defined in Tables 3 and 4 respectively.

Table 2A. Common Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Note 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Note 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Note 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	High Z
Read (x16) (Note 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	Data Out-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Notes 2, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Data Out-Odd	High Z
Read (x16) (Notes 2, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Data Out-Odd	Data Out-Even
Write (x8) (Notes 4, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data In-Odd
Write (x8) (Notes 4, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Data In	High Z
Write (x16) (Note 5, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Data In-Odd	Data In-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a Byte write operation.
5. Refer to Table 4 for valid D_{IN} during a Word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. Byte access – Even. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Byte access – Odd. In this x8 mode, $A_0 = V_{IH}$ outputs or inputs the "odd" byte (high byte) of the x16 word on D_0–D_7. This is accomplished internal to the card by transposing D_8–D_{15} to D_0–D_7.
9. Odd byte only access. In this x8 mode, A_0 = X outputs or inputs the "odd" byte (high byte) of the x16 word on D_8–D_{15}.
10. x16 word accesses present both "even" (low) and "odd" (high) bytes. $A_0 = V_{IL}$ or V_{IH} = "Don't Care".

Table 2B. Attribute Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Notes 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Not Valid
Read (x8) (Note 8)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	High Z
Read (x16) (Notes 8, 9, 10)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	Data Out-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Read (x8) (Note 9)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Read (x16) (Notes 2, 9)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Not Valid	Data Out-Even
Write (x8) (Notes 4, 7, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Write (x8) (Notes 4, 9, 10)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Write (x16) (Note 10)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Not Valid	Data In-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, $V_{CC} + 2$ V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a Byte write operation.
5. Refer to Table 4 for valid D_{IN} during a Word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Only even-byte data is valid during Attribute Memory Read function.
9. During Attribute Memory Read function, $\overline{REG}$ and $\overline{OE}$ must be active for the entire cycle.
10. During Attribute Memory Write fuction, $\overline{REG}$ and $\overline{WE}$ must be active for the entire cycle, $\overline{OE}$ must be inactive for the entire cycle.

Table 3. Command Definitions for Byte-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	90H	Read	00H/01H	01H/2AH
Erase Set-up/Erase (Note 4)	Write	SA	20H	Write	SA	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figures 1, 3 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section
   Address: 00H/01H = Address for manufacturer code/Device code.
   Data: 01H/2AH = Data for manufacturer code/Device code

Table 4. Command Definitions for Word-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	0000H/ FFFFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	9090H	Read	0000H/ 0101H	0101H/ 2A2AH
Erase Set-up/Erase (Note 4)	Write	SA	2020H	Write	SA	2020H
Erase-Verify (Note 4)	Write	EA	A0A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	4040H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFFFH	Write	X	FFFFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figures 1, 3 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

Details of AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-up is the first of a two-cycle erase command. It is a command-only operation that stages the addressed memory segment for bulk erase. The array contents are not altered with this command. 20H is written to the command register (2020H for word-wide) in order to perform the erase Set-up operation.

Erase

The second two-cycle erase command initiates the segment erase operation. You must write the Erase command 20H (2020H for word-wide) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, segment erasure can only occur when high voltage is applied to the V_{pp} pins. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase operation erases all bytes of the segment in parallel. After the erase operation, all bytes in the segment must be sequentially verified. For byte-wide operations, the A_0 signal selects between the odd and even byte banks within the memory segment. Erase and erase-verify operations must be performed in completion on the even byte segment of 256K byte then the odd byte segment of 256K byte. The Erase-verify operation is initiated by writing A0H (A0A0H for word-wide) to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the segment applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte (FFFFH for word-wide) indicates that all bits in the byte (word) are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte (word) in the memory segment until a byte (word) does not return FFH (FFFFH) data or all the bytes in the segment are accessed and verified.

If an address is not verified to FFH (FFFFH) data, the segment is erased again (refer to erase Set-up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The segment is now ready to be programmed. The verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figures 1 and 3 and Table 6, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Flasherase Electrical Erase Algorithm

This Flash memory segment erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the accessed memory segment. Erasure begins with a read of the memory contents. Reading FFH (FFFFH for word-wide) data from the segment would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

Should the segment be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the segment to their charged state (Data = 00H or 0000H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH or FFFFH) begins at address 00000H and continues through the array to the last address, or until data other than FFH (FFFFH) is encountered. For byte-wide erase operations, the A_0 signal selects between the odd and even byte banks within the memory segment. Each bank must be operated on individually and completely in verify operations. If a byte (word) fails to verify, the device is erased again. With each erase operation, an increasing number of bytes (words) verify to the erased state. Typically, devices are erased in less than 70 pulses. Erase efficiency may be improved by storing the address of the last byte (word) that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. When all bytes within an accessed segment are erased, additional segments may be erased by following the same routine. Memory segments are typically erased in less than two seconds. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin.

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The AmC004FLKA is programmed byte by byte (or word by word). Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the addressed memory segment for byte programming. The Set-up Program operation is performed by writing 40H (4040H for word-wide) to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte (word) just programmed must be verified.

Write C0H (C0C0H) into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte (word) programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the memory segment applies an internally generated margin voltage to the addressed byte (word). A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte (word) was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte (word) location. Should the byte (word) fail to verify, reprogram the byte (word) using the Program Set-up/Program Commands. Figure 2 and Table 5 indicate how instructions are combined with the bus operations to perform byte (word) programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

The reset command initializes the memory segment to the read mode. In addition, it also provides a safe method to abort any memory segment operation (including program or erase). The reset command must be written two consecutive times after the program set-up command. This will safely reset the segment memory to the read mode. Memory contents are not altered. Following any other command, write the reset command once to the segment. This will safely abort any operation and reset the device to the Read mode.

Flashrite Programming Algorithm

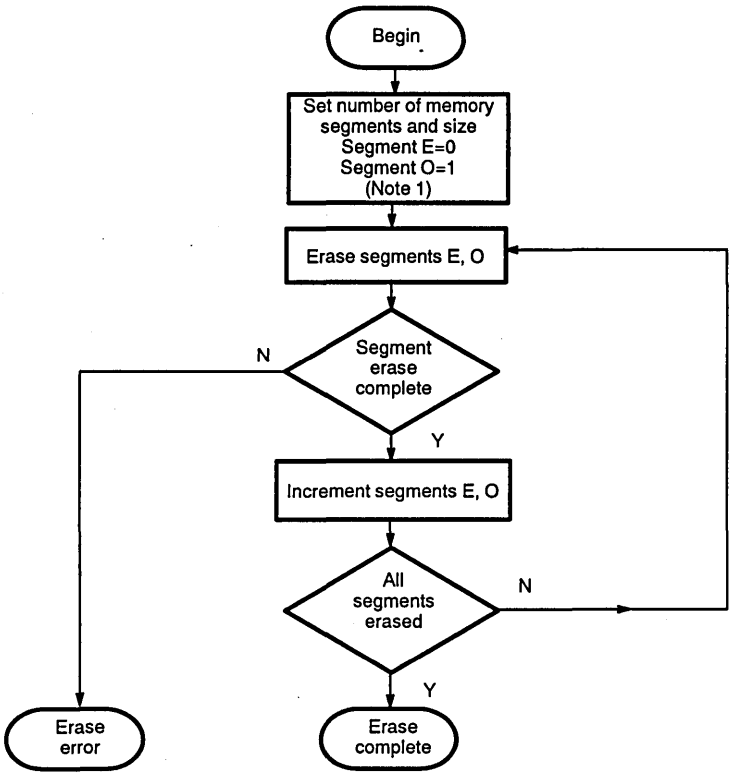
The Flashrite Programming algorithm employs an interactive closed loop flow to program data. Bytes or words may be programmed sequentially or at random using 10 microsecond programming pulses. Each operation is followed by a byte or word verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte or word per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte or word verification is performed with high voltage applied to the V_{PP} pin. Figure 2 and Table 5 illustrate the programming algorithm.

Auto Select

The Auto Select mode allows the reading out of a binary code from the memory devices to identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

MEMORY CARD ERASE ROUTINE

Overview



16662A-2

Note:
1. E = Even byte, O = Odd byte.

Figure 1.

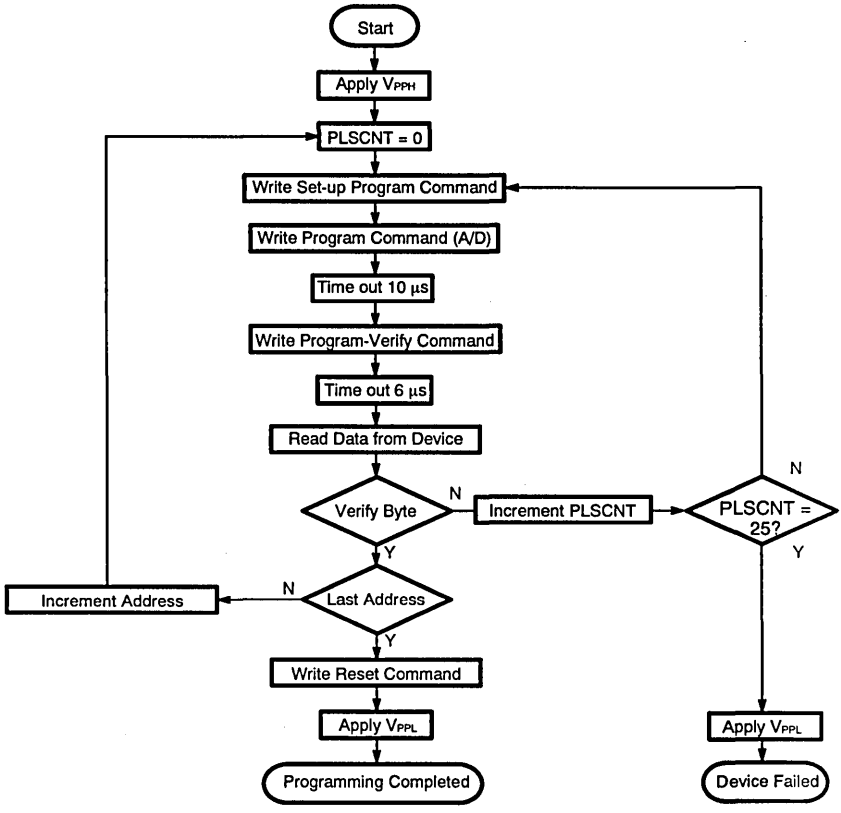


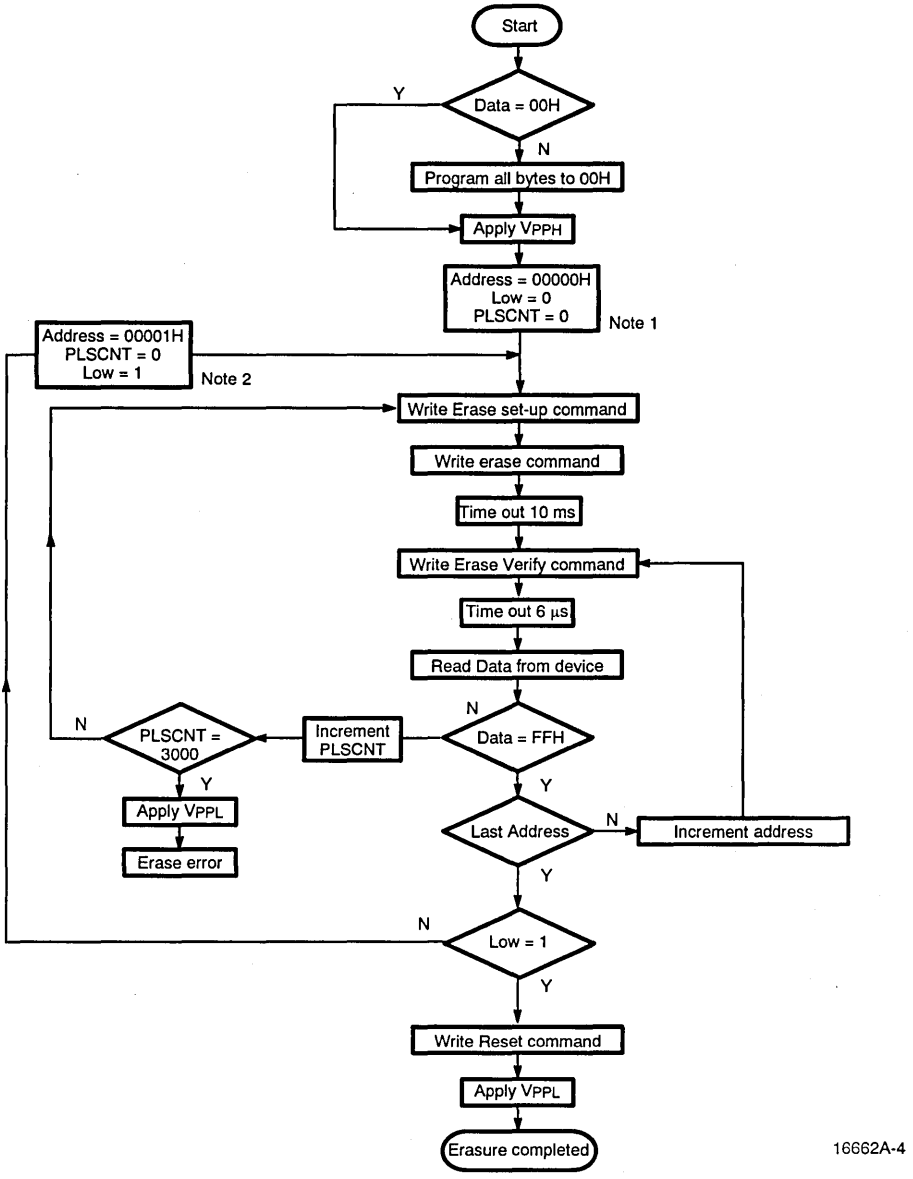
Figure 2. Flashrite Programming Algorithm in Byte-Wide Mode

Table 5. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



Notes:

1. Low = 0: Even byte segment Erase/Erase verify operation.
2. Low = 1: Odd byte segment Erase/Erase verify operation.

Figure 3. Flasherase Electrical Erase Algorithm in Byte-Wide Mode

Table 6. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.

WORD-WIDE PROGRAMMING

The program sequence will be followed as usual. The program word command is 4040H. Each device is independently verified. When one of the program flags is active, indicating that a particular device has successfully completed programming, the software should change the command for that device from Program to Reset and from program verify to Reset. The software should also change the Program Data to the null data set (FFH). This effectively masks the programmed device from further programming.

Should the high order byte device verify first, the next program command will be FF40H. The low order byte device programs on each subsequent program command until verified. The high order byte device remains in Reset/Read mode. During verification, write the program verify command of FFC0H. This will enable the low order byte device for verify operations and maintains the programmed high order byte device in Reset/Read mode.

WORD-WIDE PROGRAMMING
Overview

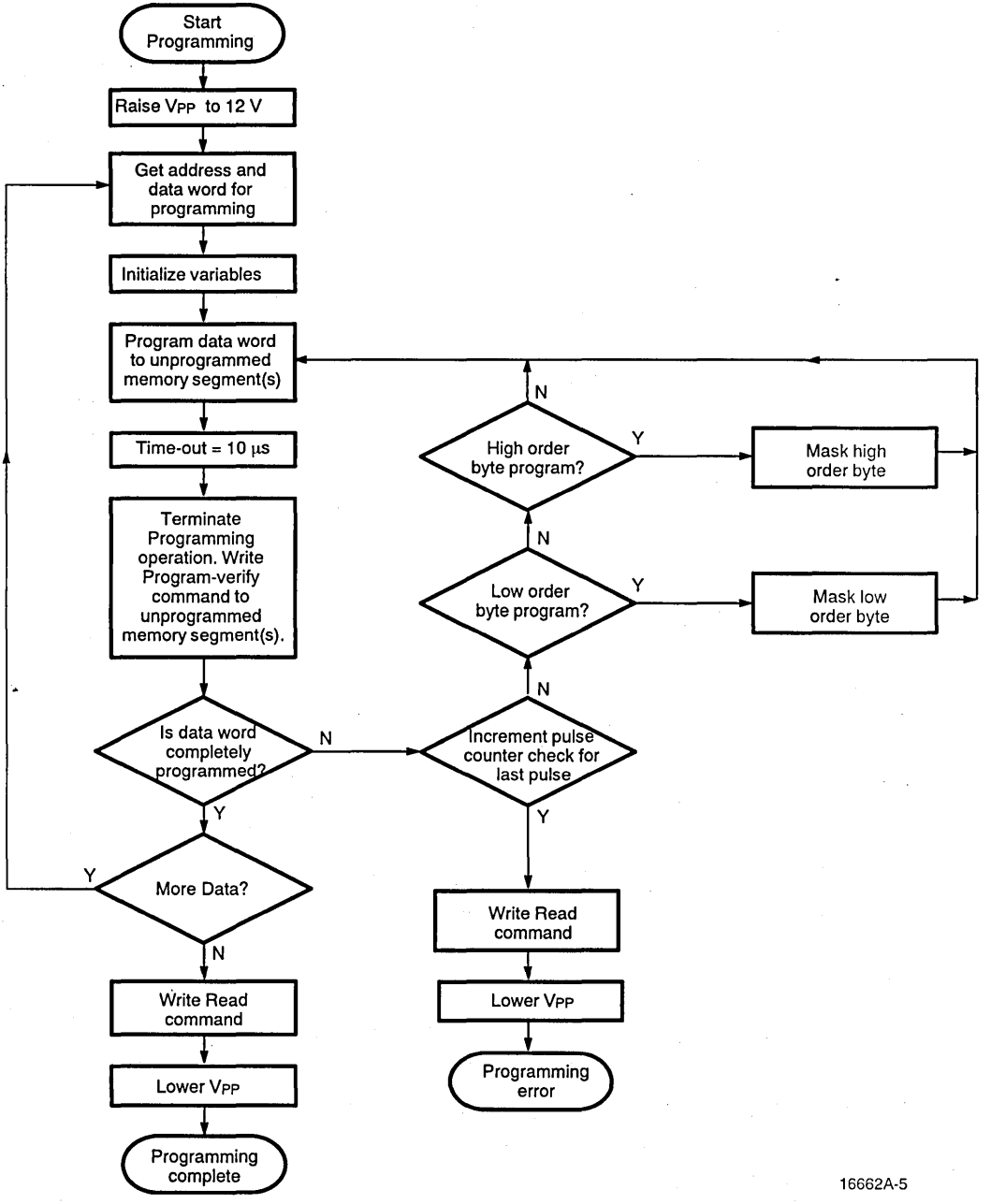
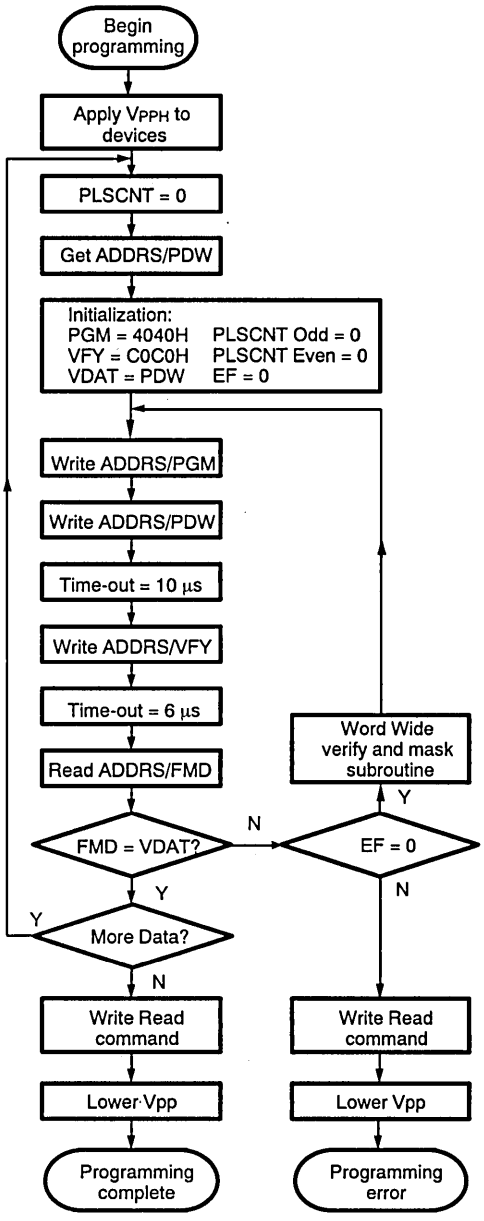


Figure 4.

WORD-WIDE PROGRAMMING FLOW CHART



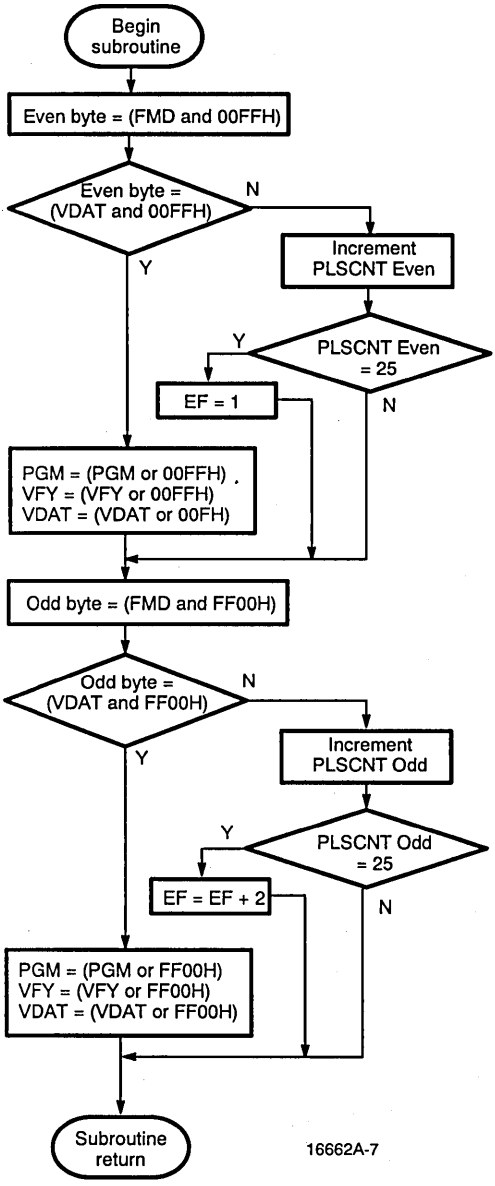
16662A-6

Note:
Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any device from programming operations.

Activity
Allow V_{PP} to stabilize.
PLSCNT = Pulse Counter.
ADDRS = Word Address to program. *PDW = Data Word to program.*
Initialize Programming Variables: *PGM = Program Command* *VFY = Program-verify Command* *VDAT = Valid Data* *PLSCNT Odd = Pulse count for odd (high) byte* *PLSCNT Even = Pulse count for even (low) byte* *EF = Error Flag for write*
ADDRS = Address do not care. *Write Program Set-up command.*
Appropriate address and data for programming.
Duration of programming pulse.
Program-verify command terminates the programming pulse.
Internal margin verify voltages are tapped from external 12 V V_{PP} for proper byte verification.
Read from previously latched address. FMD = Flash Memory Data.
See Word Wide Programming subroutine. Each device is independently verified. The Program command is masked by the Reset command (FFH) for all devices that are completely Programmed. Please see note below.
Compare Flash Memory Data to valid word data. If verified, reset PLSCNT and get next address and data word for programming. If not last pulse, compare high order byte device and low order byte device for valid byte data.
Reset devices for read operation.
V_{PPL} deactivates command register. Device is in Read Only Mode.

Figure 5.

WORD-WIDE PROGRAMMING VERIFY SUBROUTINE



Commentary

This subroutine verifies the high order (odd) and low order (even) bytes independently. If either byte verifies, all commands are masked to that device.

Mask the odd byte to look at the even byte.

If the even byte doesn't verify, increment pulse count and continue of program even byte.
EF = Error Flag

Mask the even byte commands and program data if it verifies.

Mask the even byte to look at the odd byte.

If the odd byte doesn't verify, increment pulse count and continue to program odd byte.

Mask the odd byte commands and program data if it verifies.

Error Flag Summary:

EF = 0 indicates no program error
EF = 1 indicates even byte program error
EF = 2 indicates odd byte program error
EF = 3 indicates both even and odd byte program error

Figure 6.

WORD-WIDE ERASING

Overview

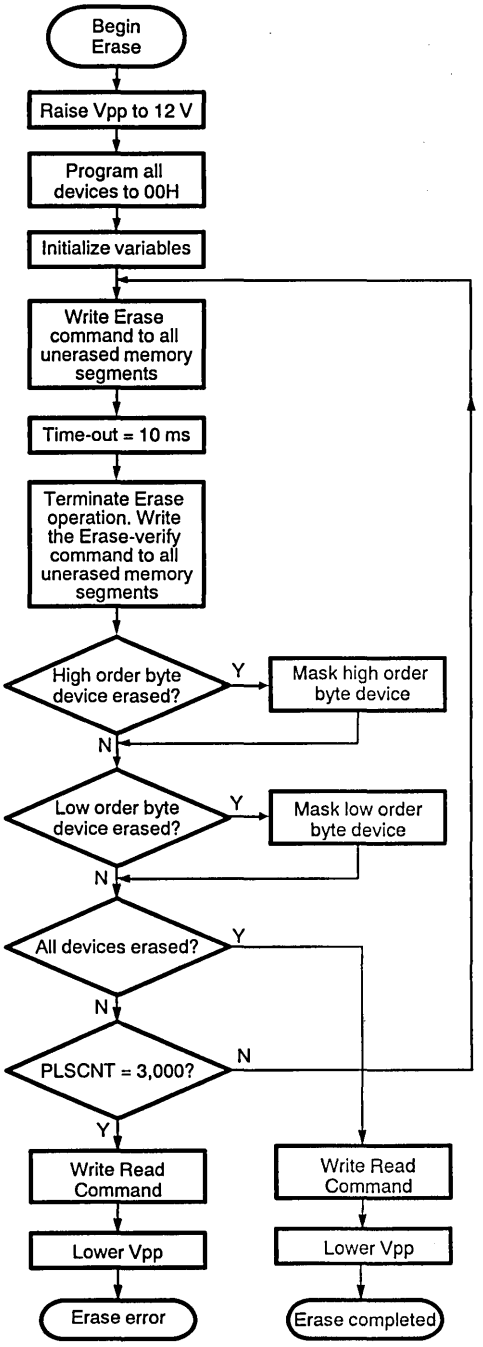
Word-Wide Erasure

Word-wide erasure reduces total erase time when compared to erasing each byte individually. Each Flash memory may erase at different rates. Therefore each device must be verified separately after every erase pulse. Once a device has successfully completed erasure, do not issue the erase command again to that device. Issue the Reset command FFH to the erased device. The Erase command sequence may be issued to each of the remaining devices that have not erased yet. In addition to the address verify register required for each device, you will need an erase complete flag for each device.

Word-Wide

The erase sequence will be followed as usual. The CPU will issue word commands. The erase word command is 2020H. Each device is independently verified and the address of the last verified byte per device is stored in separate registers. When one of the erase flags is active, indicating that a particular device has successfully completed erasure, the CPU will change the command for that device from Erase to Reset. This effectively masks the erased device from further erasure.

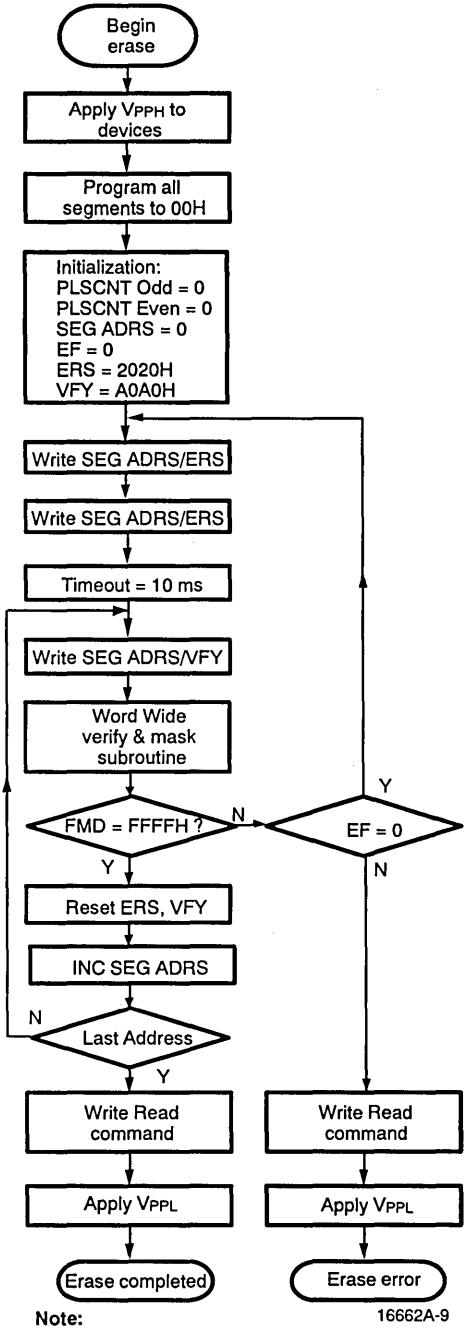
Should the high order byte device verify first, the next erase command will be FF20H. The low order byte device erases on each subsequent erase command until verified. The high order byte device remains in Reset/Read mode. During verification, write the erase verify command of FFA0H. This will enable the low order byte device for verify operations and maintains the erased high order byte device in the Reset/Read mode.



16662A-8

Figure 7.

WORD-WIDE ERASURE FLOW CHART



Activity
Allow V_{PP} to stabilize.
Follow Flashrite programming algorithm.
Initialize Erase Variables: *PLSCNT Odd = Pulse count for odd (high) byte* *PLSCNT Even = Pulse count for even (low) byte* *SEG ADRS = Address* *EF = Error Flag for error* *ERS = Erase Command* *VFY = Erase-verify Command*
Write Program Set-up command.
Initiate erase pulse.
Duration of programming pulse.
Erase-verify command terminates the erase pulse.
See Word Wide Erasure subroutine. Each device is independently verified. The command is masked by the Reset command (FFH) for all devices that are completely erased. Please see note below.
FMD = FFFFH when memory segment at SEG ADRS is erased.
Reset devices for read operation.
V_{PPL} deactivates command register. Device is in the Read Only Mode.

Note:
Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any completely erased device from further erase operations.

Figure 8.

WORD-WIDE ERASE VERIFY SUBROUTINE

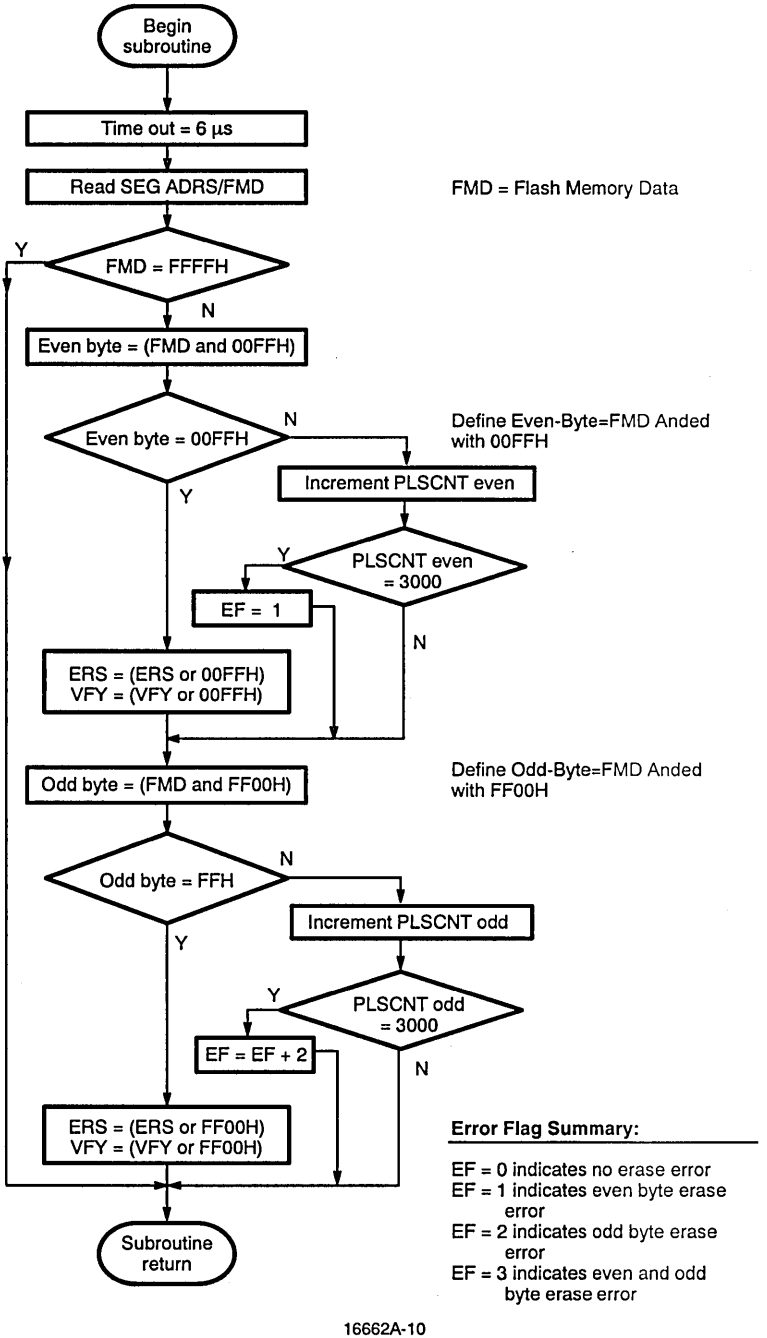


Figure 9.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −30°C to +70°C

Ambient Temperature
with Power Applied ..... −10°C to +70°C

Voltage with Respect to Ground
All pins except V_{PP} (Note 1) ..... −2.0 V to +7.0 V

V_{CC} (Note 1) ..... −2.0 V to +7.0 V

V_{PP} (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5 V. During voltage transitions, outputs may overshoot to V_{CC} +2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on V_{PP} pins is −0.5 V. During voltage transitions, V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = V_{CC} max. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +60°C

V_{CC} Supply Voltages ..... +4.75 V to 5.25 V

V_{PP} Supply Voltages

Read Only ..... 0 V to +6.5 V

Program, Erase, Verify,
and Read ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Byte Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±28	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	28	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. CE = V_{CC} ±0.2 V		0.4	1.6	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., CE = V_{IL}, OE = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		25	50	mA
I_{CC2}	V_{CC} Programming Current	CE = V_{IL} Programming in Progress		3.0	30	mA
I_{CC3}	V_{CC} Erase Current	CE = V_{IL} Erasure in Progress		5.0	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			16	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.2	0.4	mA
		$V_{PP} \leq V_{CC}$			0.04	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		8.0	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. One Flash device active, seven in standby.
2. Only one Vpp is active.

DC CHARACTERISTICS

Word-Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±28	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	28	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ±0.2 V		0.4	1.6	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		40	80	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		6	60	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	60	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			16	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.4	0.8	mA
		$V_{PP} \leq V_{CC}$			0.08	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		16	60	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		20	60	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = 2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. Two Flash devices active, six in standby.
2. V_{pp1} and V_{pp2} are active.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Capacitance	V_{IN} = 0		21	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		21	pF
C_{IN2}	Control Capacitance	V_{IN} = 0 ($\overline{CE}$, $\overline{REG}$)		47	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = 0		21	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING AC CHARACTERISTICS

Read Only Operation (Note 1)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	250		ns
t_{ELQV}	t_{CE}	Chip Enable Access Time		250	ns
t_{AVQV}	t_{ACC}	Address Access Time		250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time		150	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	5		ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z		60	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z		60	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
t_{WHGL}		Write Recovery Time before Read	6		µs

Note:

1. Input Rise and Fall Times (10% to 90%): ≤ 10 ns, Input Pulse levels: V_{OL} and V_{OH}, Timing Measurement Reference Level – Inputs: V_{IL} and V_{IH} Outputs: V_{IL} and V_{IH}

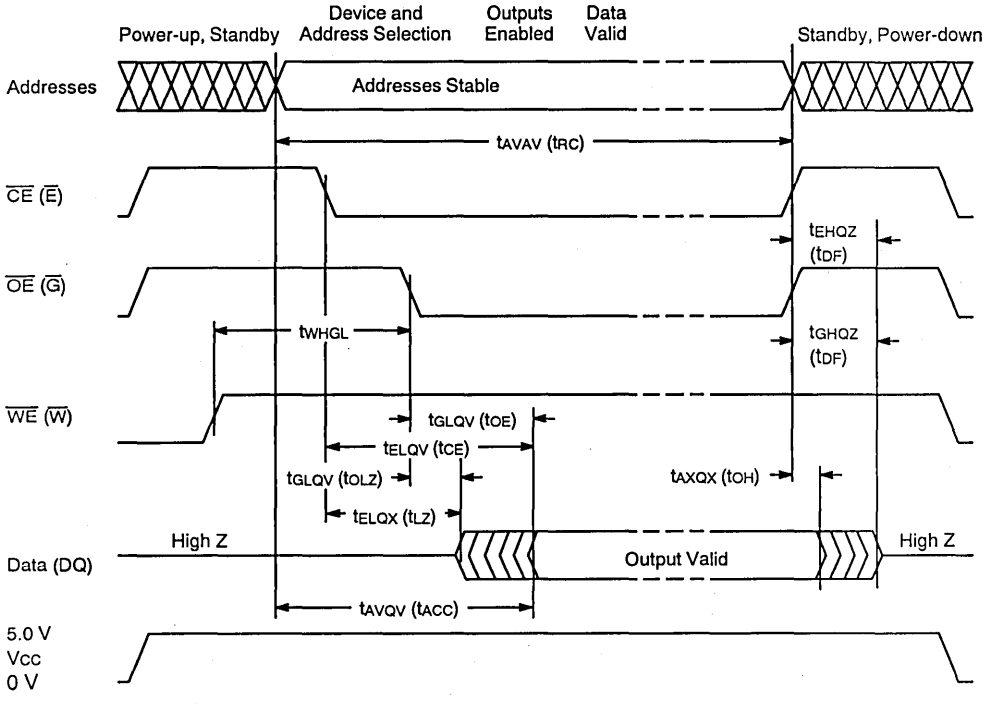
AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVWL}	t_{AS}	Address Set-Up Time	0		ns
t_{WLAX}	t_{AH}	Address Hold Time	100		ns
t_{DVWH}	t_{DS}	Data Set-Up Time	80		ns
t_{WHDX}	t_{DH}	Data Hold Time	30		ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHWL}		Read Recovery Time before Write	0		µs
t_{WLOZ}		Output in High-Z from Write Enable	5		ns
t_{WHOZ}		Output in Low-Z from Write Enable		60	ns
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	40		ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	100		ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	50		ns
t_{WHWH1}		Duration of Programming Operation (Notes 1, 2)	10		µs
t_{WHWH2}		Duration of Erase Operation (Notes 1, 2)	9.5		ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	100		ns

Notes:

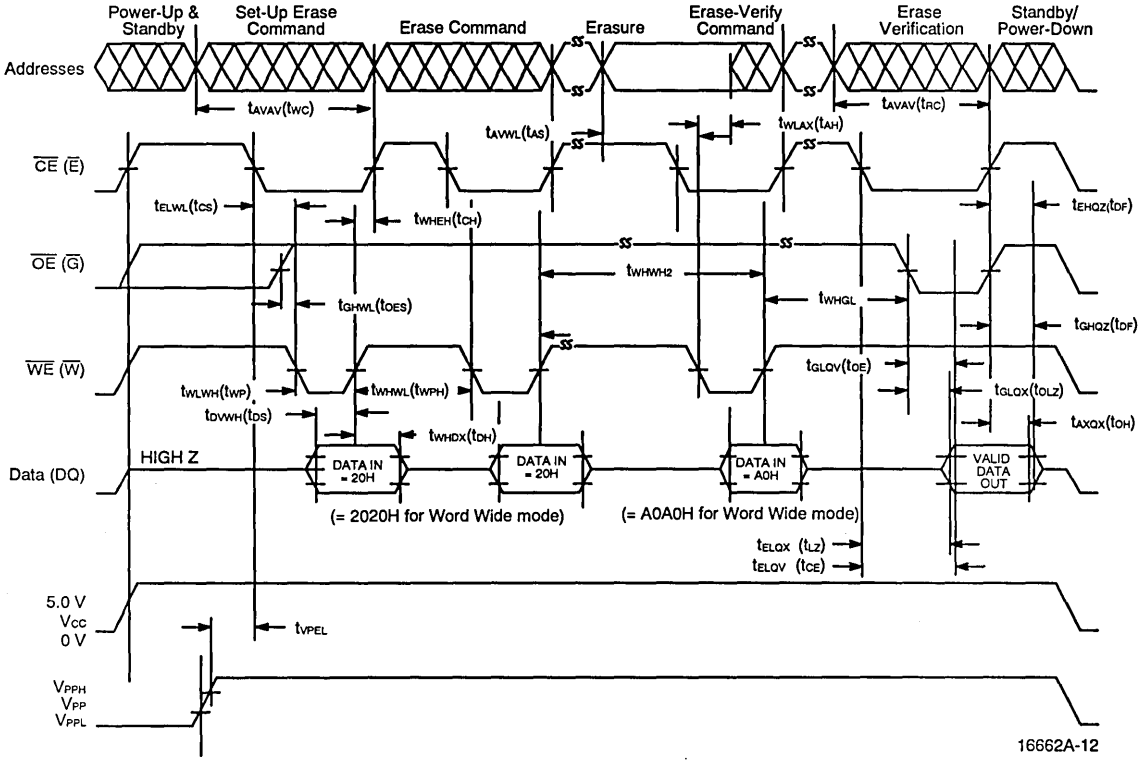
1. Rise/Fall < = 10 ns.
2. Maximum specification not needed due to the devices internal stop timer that will stop any erase or write operation that exceed the device specification.



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

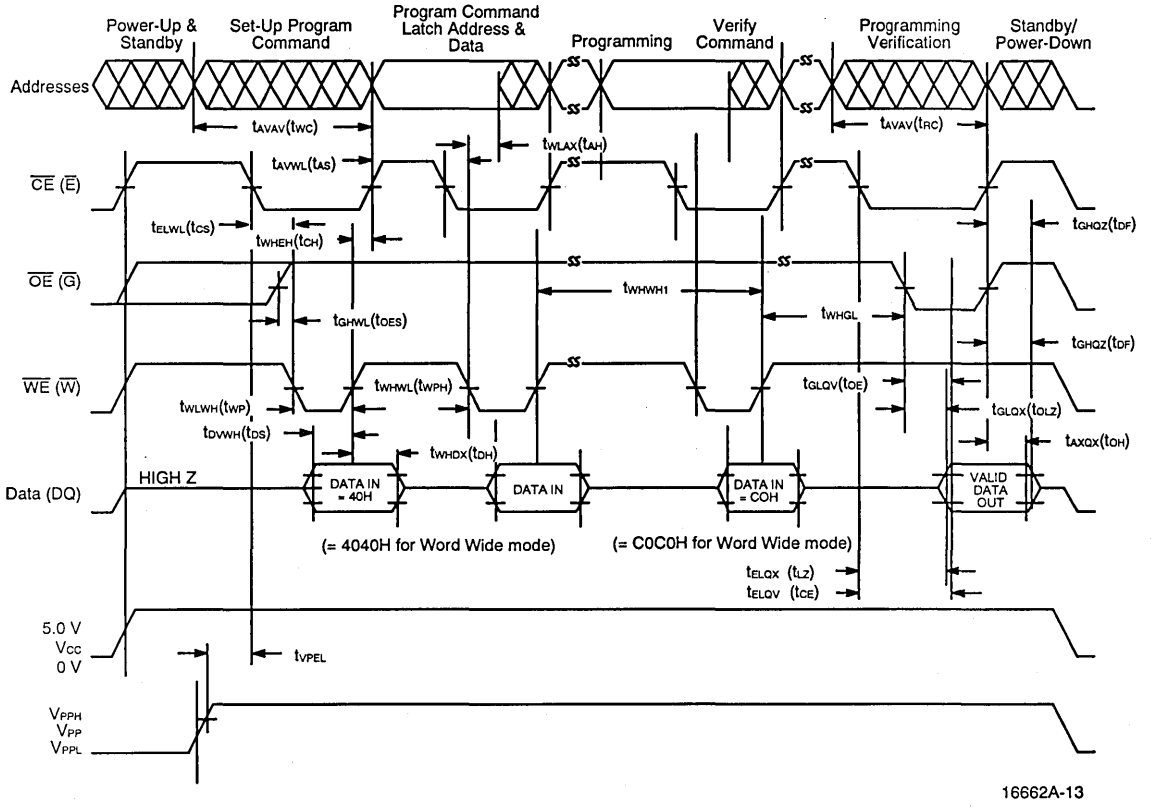
16662A-11

Figure 10. AC Waveforms for Read Operations



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

Figure 11. AC Waveforms for Erase Operations



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

Figure 12. AC Waveforms for Programming Operations

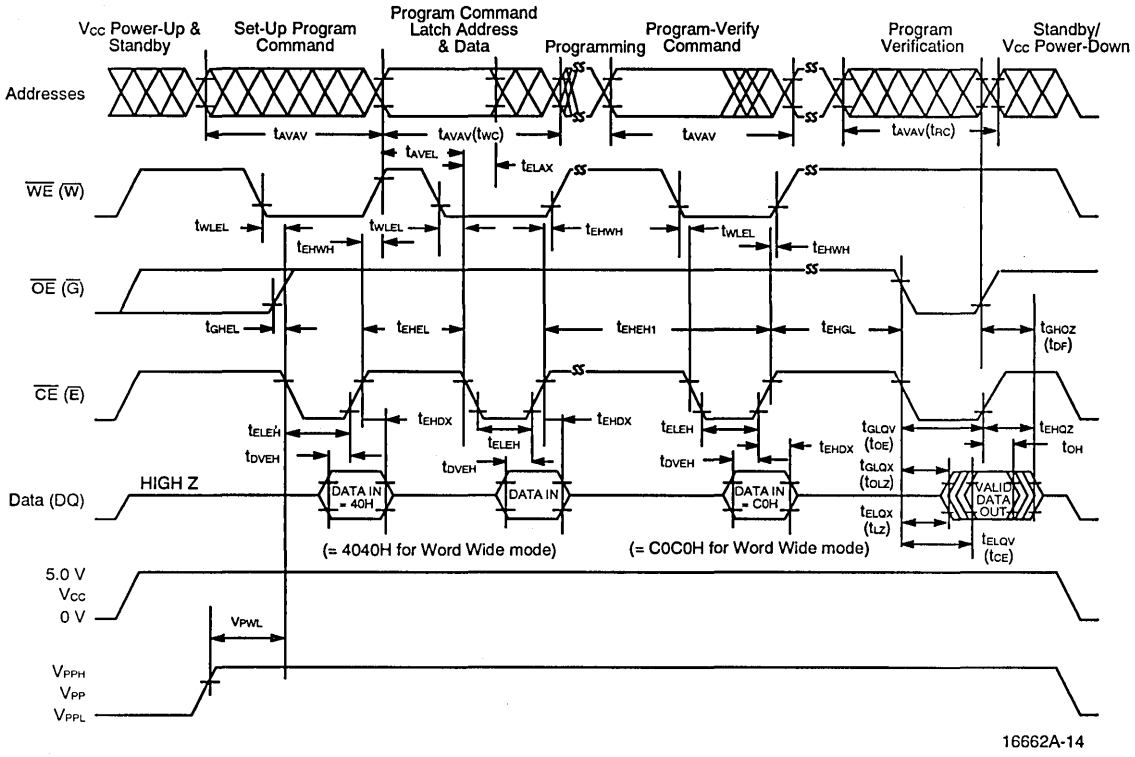
AC CHARACTERISTICS–ALTERNATE $\overline{CE}$ CONTROLLED WRITES

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVEL}	t_{AS}	Address Set-Up Time	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	100		ns
t_{DVEH}	t_{DS}	Data Set-Up Time	80		ns
t_{EHDX}	t_{DH}	Data Hold Time	30		ns
t_{EHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHEL}		Read Recovery Time before Write	0		µs
t_{WLEL}	t_{WS}	WE Set-Up Time before $\overline{CE}$	0		ns
t_{EHWH}	t_{CP}	WE Hold Time	0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	100		ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH (Note 3)	50		ns
t_{EHEH1}		Duration of Programming Operation (Notes 1, 2)	10		µs
t_{EHEH2}		Duration of Erase Operation (Notes 1, 2)	9.5		ms
t_{VPWL}		V_{PP} Set-Up Time to Write Enable LOW	100		ns

Notes:

1. Rise/Fall <=10 ns
2. Maximum specification not needed due to the internal stop timer that will stop any erase or write operation that exist the device specification.
3. Chip Enable Controlled Programming:
   Flash Programming is controlled by the valid combination of the Chip Enable ($\overline{CE}_{1, 2}$) and Write Enable ($\overline{WE}$) signals. For system that uses the Chip Enable signal(s) to define the write pulse width, all Set-up, Hold, and inactive Write Enable timing should be measured relative to the Chip Enable signal(s).



16662A-14

Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

Figure 13. Alternate AC Waveforms for $\overline{CE}$ Controlled Programming Operations

CARD INFORMATION STRUCTURE

The AmC001FLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. All or part of the 512 byte could be used for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space. Part of the common memory space could also be mapped into the attribute memory space if more than 512 bytes of CIS are needed.

The EEPROM used in the AmC004FLKA is a NEC μPD28C05GX-20-EJA designed to operate from a 5 V single power supply. The μPD28C05 provides a DATA polling function that provides the End of Write Cycle, Chip Erase and Auto Erase and Programming functions.

SYSTEM DESIGN AND INTERFACE INFORMATION

Power Up and Power Down Protection

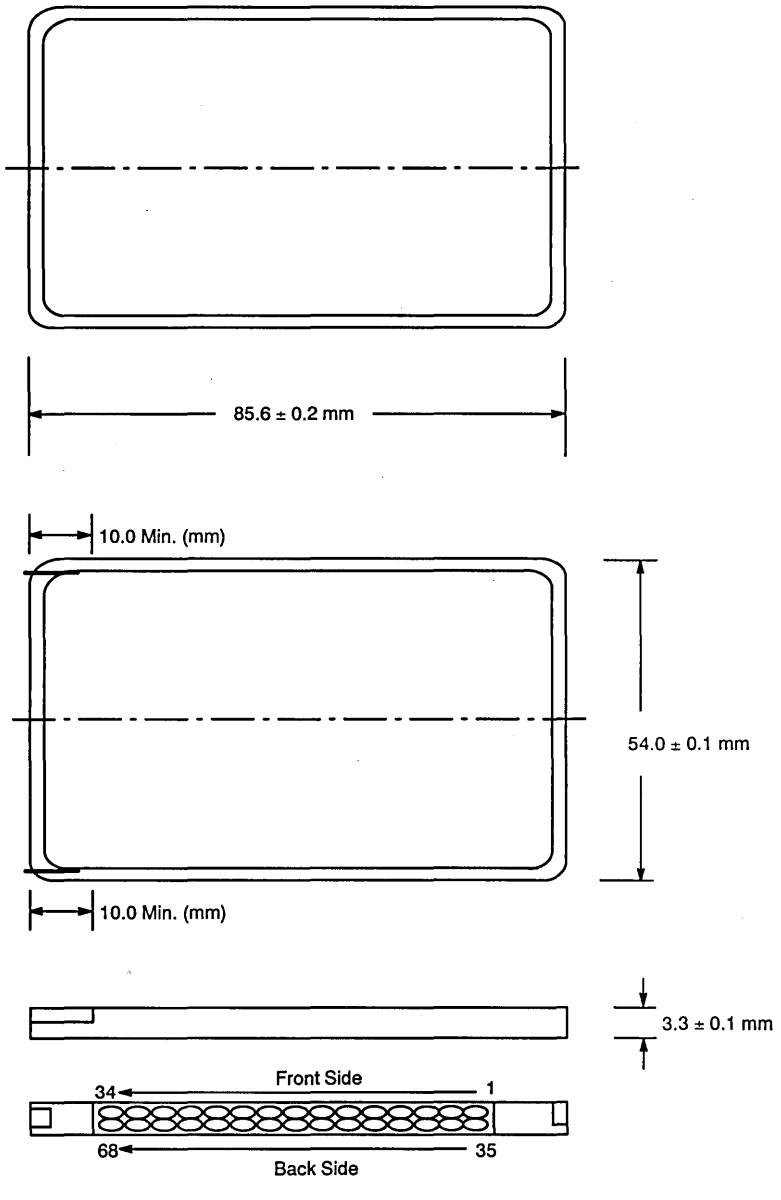
The PCMCIA standard socket provides for proper power up and power down sequencing via different pin lengths to ensure that hot insertion and removal of the PC card will not result in card damage or data loss.

AMD's Flash memory devices are designed to protect against accidental programming or erasure caused by spurious system signals that might exist during hot insertion, hot removal, or power transitions. The AMD PC card will power-up into a READ mode and the card will function as a read only memory as long as V_{pp} is less than V_{cc} +2 V. Erasing of the memory segments can be accomplished only by writing the proper Erase command to the card twice along with the proper Chip Enable, Output Enable and Write Enable control signals.

System Power Supply Decoupling

The AMD Flash memory card has a 0.1 μF decoupling capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins. It is recommended the system side also have a 4.7 μF capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins.

PHYSICAL DIMENSIONS
Type 1 PC Card



16662A-15

PRELIMINARY

AmC001AFLKA

1 Megabyte Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 250 ns maximum access time
- **CMOS low power consumption**
  - 25 mA typical active current (X8)
  - 400 μA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **High re-programmable endurance**
  - Minimum 100,000 erase/write cycles
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate attribute memory**
  - 512 byte EEPROM
- **Automated write and erase operations (increases system write performance)**
  - 128K byte memory segment
  - Typically <1 second per single memory segment erase
  - Random address writes to previously erased bytes (10 μs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Insertion and removal force**
  - State of art connector allows for minimum card insertion and removal effort
- **Write and erase voltage, 12.0 V ± 5%**
- **Read voltage, 5 V ± 5%**
- **Manufactured by DuPont Connector Systems**

GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC001AFLKA. This allows OEM manufacturers of portable system to eliminate the weight, extreme power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC001AFLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC001AFLKA enhances the productivity of mobile workers.

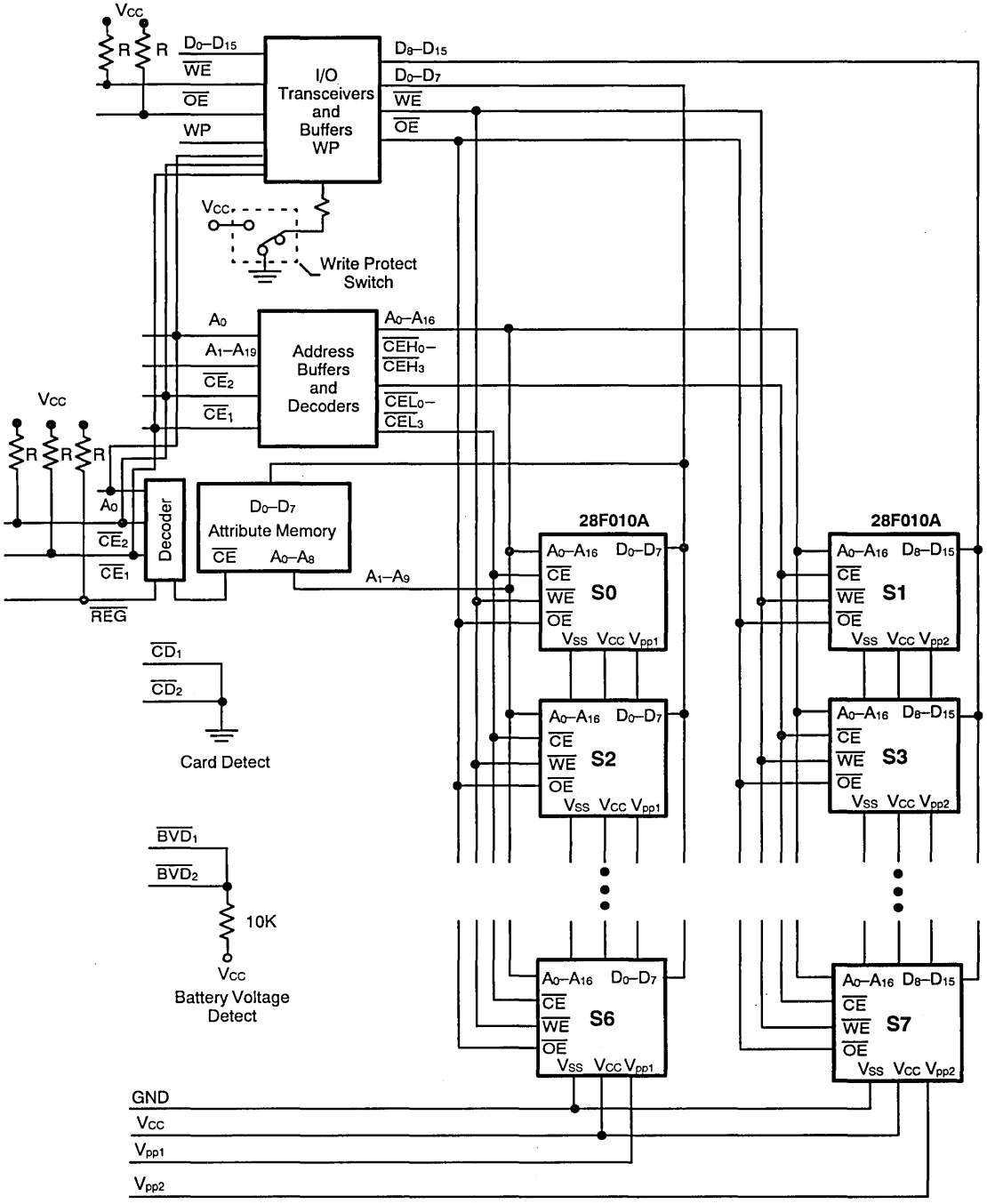
Widespread acceptance of the AmC001AFLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC001AFLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by DuPont Connector Systems

Publication# 17120 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



R=33K

17120A-1

PC CARD PIN ASSIGNMENTS

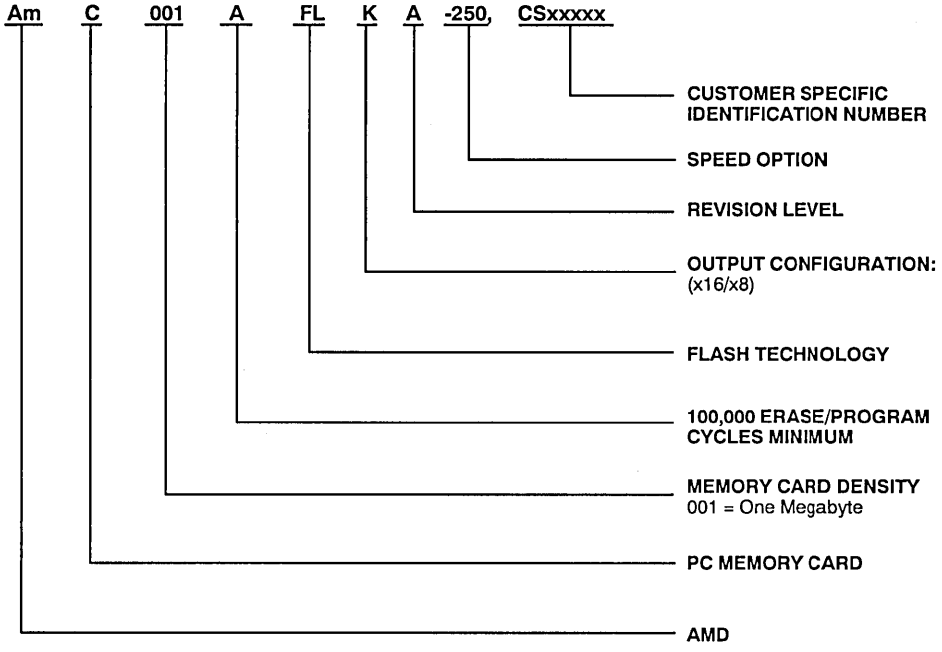
Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable (Note 1)	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2 (Note 1)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	RFU		Reserved
11	A_9	I	Address Bit 9	45	RFU		Reserved
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	NC		No Connect
16	NC		No Connect	50	NC		No Connect
17	V_{CC}		Power Supply	51	V_{CC}		Power Supply
18	Vpp1		Pgm Sply Vltg 1	52	V_{pp2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.
1. Signal must not be connected between cards
2. $\overline{BVD}$ = Internally pulled-up

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



PIN DESCRIPTION

Symbol	Type	Name and Function
$A_0 - A_{19}$	INPUT	**ADDRESS INPUTS** are internally latched during write cycles.
$D_0 - D_{15}$	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Data inputs are internally latched on write cycles. Data outputs during read cycles. Data pins are active high. When the memory card is de-selected or the outputs are disabled the outputs float to tri-state.
$\overline{CE_1}$, $\overline{CE_2}$	INPUT	**CARD ENABLE** is active low. The memory card is de-selected and power consumption is reduced to stand-by levels when $\overline{CE}$ is high. $\overline{CE}$ activates the internal memory card circuitry that controls the high and low byte control logic of the card, input buffers segment decoders, and associated memory devices.
$\overline{OE}$	INPUT	**OUTPUT ENABLE** is active low and enables the data buffers through the card outputs during read cycles.
$\overline{WE}$	INPUT	**WRITE ENABLE** is active low and controls the write function of the command register to the memory array. The target address is latched on the falling edge of the $\overline{WE}$ pulse and the appropriate data is latched on the rising edge of the pulse.
V_{PP1},V_{PP2}		**ERASE/WRITE POWER SUPPLY** for erase and programming. V_{pp} enables the command register which controls all functions required to alter the memory array contents. **Note:** The Memory Card functions in a read-only memory when $V_{PP} < V_{cc} + 2$ V.
V_{CC}		**PC CARD POWER SUPPLY** for device operation (5.0 V ± 5%)
GND		**GROUND**
CD_1, CD_2	OUTPUT	**CARD DETECT**. When card detect 1 and 2 = ground the system detects the card.
WP	OUTPUT	**WRITE PROTECT** is active high and disables all card write operations.
NC		**NO CONNECT** - corresponding pin is not connected internally to the die.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT.** Internally pulled-up.

MEMORY CARD OPERATIONS

The AmC001AFLKA Flash Memory Card is organized as an array of individual devices. Each device is 128K bytes in size. Although the address space is continuous each physical device defines a logical address segment size. Erase operations are performed in increments of this segment size. Multiple segments may be erased concurrently when additional V_{pp} current is supplied to the device. Once a memory segment is erased any address location may be programmed. Flash technology allows any logical "1" data bit to be programmed to a logical "0". The only way to reset bits to a logical "1" is to erase the entire memory segment of 128K bytes. High voltage is required on V_{pp1} and V_{pp2} to perform program and erase operations.

The common memory space data contents are altered in a similar manner as writing to individual Flash Memory devices. On-card address and data buffers activate the appropriate Flash device in the memory array. Each device internally latches address and data during write cycles. Refer to Table 2A.

Attribute memory is a separately accessed card memory space. The register memory space is active when the $\overline{REG}$ pin is driven low. The Card Information Structure describes the capabilities and specification of a card. The CIS is stored in the attribute memory space beginning at address 00000H. The AmC001AFLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. Alternatively, the CIS can be stored at the beginning of the common memory address space. D_0–D_7 are active during attribute memory accesses. D_8–D_{15} should be ignored. Odd order bytes present invalid data. Refer to Table 2B.

Word-Wide Operations

The AmC001AFLKA provides the flexibility to operate on data in a byte-wide or word-wide format. In word-wide operations the Low-bytes are controlled with V_{pp1} and $\overline{CE_1}$ when A0 = 0. The High-bytes are controlled with V_{pp2} and $\overline{CE_2}$, A0 = don't care.

Erase operations are the only operations that work on entire memory segments. All other operations such as word-wide programming are not affected by the physical memory segments.

Byte-Wide Operations

Byte-wide data is available on D_0–D_7 for read and write operations ($\overline{CE_1}$ = low, $\overline{CE_2}$ = high). Even and odd bytes are stored in separate memory segments (i.e. S_0 and S_1) and are accessed when A0 is low and high respectively. The even byte is the low order byte and the odd byte is the high order byte of a 16-bit word.

Erase operations in the byte-wide mode must account for data multiplexing on D_0–D_7 by changing the state of A0. Each memory segment pair must be addressed separately for erase operations.

Card Detection

Each $\overline{CD}$ (output) pin should be read by the host system to determine if the memory card is adequately seated in the socket. $\overline{CD_1}$ and $\overline{CD_2}$ are internally tied to ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

Write Protection

The AMD Flash memory card has three types of write protection. The PCMCIA/JEIDA socket itself provides the first type of write protection. Power supply and control pins have specific pin lengths in order to protect the card with proper power supply sequencing in the case of hot insertion and removal.

A mechanical write protect switch provides a second type of write protection. When this switch is activated, $\overline{WE}$ is internally forced high. The Flash memory command register is disabled from accepting any write commands.

The third type of write protection is achieved with V_{pp1} and V_{pp2} at logic low levels to reset the Flash devices to read-only mode. Memory contents can not be changed in this state. The command register of individual Flash memory segments is only active when V_{pp1} and/or V_{pp2} are at high voltage (V_{ppH}).

Each Flash memory device that comprises a Flash memory segment will reset the command register to the read-only mode when V_{cc} is below VLKO. VLKO is the voltage below which write operations to individual command registers are disabled.

MEMORY CARD BUS OPERATIONS

Read Enable

Two Card Enable ($\overline{CE}$) pins are available on the memory card. Both $\overline{CE}$ pins must be active low for word-wide read accesses. Only one $\overline{CE}$ is required for byte-wide accesses. The $\overline{CE}$ pins control the selection and gates power to the high and low memory segments. The Output Enable ($\overline{OE}$) controls gating accessed data from the memory segment outputs.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state.

Standby Operations

Byte-wide read accesses only require half of the read/write output buffer (x16) to be active. In addition, only one memory segment is active with in either the high order or low order bank. Activation of the appropriate half of the output buffer is controlled by the combination of both $\overline{CE}$ pins. The $\overline{CE}$ pins also control power to the high and low-order banks of memory. Outputs of the memory bank not selected are placed in the high impedance state. The individual memory segment is activated by the address decoders. The other memory segments operate in standby. An active memory segment continues to draw power until completion of a write, erase, or verify operation if the card is de-selected in the process of one of these operations.

Auto Select Operation

A host system or external card reader/writer can determine the on-card manufacturer and device I.D. codes. Codes are available after writing the 90H command to the command register of a memory segment. Reading from address location 00000H in any segment provides the manufacturer I.D. while address location 00002H provides the device I.D.

Write Operations

Write and erase operations are valid only when V_{pp1} and V_{pp2} are at high voltage. This activates the state machine of an addressed memory segment. The command register is a latch which saves address, commands, and data information used by the state machine and memory array.

When Write Enable ($\overline{WE}$) and appropriate $\overline{CE}$(s) are a logic-level low, the command register is enabled for write operations. The falling edge of $\overline{WE}$ latches address information and the rising edge latches data/command information.

Memory Segment Command Definitions

When the V_{pp} pin(s) are at low voltage the command register of each Flash memory segment defaults to 00H, the Read only mode.

With high voltage on the V_{pp} pin(s), the Flash memory segments are active for either read, write, or erase operations.

Write or erase operations are performed by writing appropriate data patterns to the command register of accessed Flash memory segments.

The byte-wide and word-wide commands are defined in Tables 3 and 4 respectively.

Table 2A. Common Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Note 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Note 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Note 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	High Z
Read (x16) (Note 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out - Odd	Data Out-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Notes 2, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Data Out-Odd	High Z
Read (x16) (Notes 2, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Data Out-Odd	Data Out-Even
Write (x8) (Notes 4, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data In-Odd
Write (x8) (Notes 4, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Data In	High Z
Write (x16) (Notes 5, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Data In Odd	Data In-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a byte write operation.
5. Refer to Table 4 for valid D_{IN} during a word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. Byte access – Even. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Byte access – Odd. In this x8 mode, $A_0 = V_{IH}$ outputs or inputs the "odd" byte (high byte) of the x16 word on D_0–D_7. This is accomplished internal to the card by transposing D_8–D_{15} to D_0–D_7.
9. Odd byte only access. In this x8 mode, A_0 = X outputs or inputs the "odd" byte (high byte) of the x16 word on D_8–D_{15}.
10. x16 word accesses present both "even" (low) and "odd" (high) bytes. $A_0 = V_{IL}$ or V_{IH} = "Don't Care".

Table 2B. Attribute Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Notes 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Not Valid
Read (x8) (Note 8)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	High Z
Read (x16) (Notes 8, 9, 10)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	Data Out-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Read (x8) (Note 9)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Read (x16) (Notes 2, 9)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Not Valid	Data Out-Even
Write (x8) (Notes 4, 7, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8, 10)	V_{IL}	V_{IIH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Write (x8) (Notes 4, 9, 10)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Write (x16) (Note 10)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Not Valid	Data In-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a write operation.
5. Refer to Table 4 for valid D_{IN} during a write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Only even-byte data is valid during Attribute Memory Read function.
9. During Attribute Memory Read function, $\overline{REG}$ and $\overline{OE}$ must be active for the entire cycle.
10. During Attribute Memory Write function, $\overline{REG}$ and $\overline{WE}$ must be active for the entire cycle, $\overline{OE}$ must be inactive for the entire cycle.

Table 3. Command Definitions for Byte-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	90H	Read	00H/01H	01H/A2H
Embedded Set-up/Erase Embedded Erase™ (Note 4)	Write	X	30H	Write	X	30H
Embedded Set-up Program/ Embedded Program™ (Note 5)	Write	X	50H	Write	PA	PD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Embedded Erase Algorithm.
5. Figure 2 illustrates the Embedded Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.
   Address: 00H/01H = MFG code / Device code addresses.
   Data: 01H/A2H = MFG code data / Device code data.

Table 4. Command Definitions for Word-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	0000H/ FFFFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	9090H	Read	0000H/ 0101H	0101H/ A7A7H
Embedded Erase Set-up/Erase	Write	SA	3030H	Write	X	3030H
Embedded Set-up Program/ Embedded Program	Write	X	5050H	Write	PA	PD
Reset (Note 6)	Write	X	FFFFH	Write	X	FFFFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Embedded Electrical Erase Algorithm.
5. Figure 2 illustrates the Embedded Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

Details of AMD's Embedded Program and Erase Operations

Embedded Erase™ Algorithm

The automatic memory segment erase does not require the device to be entirely pre-programmed prior to executing the Embedded erase set-up command and Embedded erase command. Upon executing the Embedded erase command, the addressed memory segment automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the memory segment is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 of the memory segment is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded erase set-up command is a command only operation that stages the memory segment for automatic electrical erasure of all bytes in the array. Embedded erase set-up is performed by writing 30H to the command register of the addressed memory segment.

To commence automatic segment erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 of the memory segment is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 1 and Table 5 illustrate the Embedded Erase algorithm, a typical command string and bus operations.

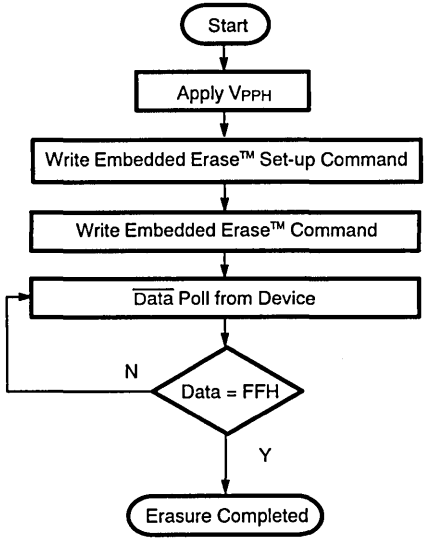


Figure 1. Embedded Erase™ Algorithm in Byte-Wide Mode

Table 5. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation.

Embedded Program™ Algorithm

The Embedded Program Set-up is a command only operation that stages the addressed memory segment for automatic programming. Embedded Program Set-up is performed by writing 50H to the command register.

Once the Embedded Program Set-up operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 of the addressed memory segment is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode (no program verify command is required).

Figure 2 and Table 6 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

Reset Command

The reset command initializes the memory segment to the read mode. In addition, it also provides a safe method to abort any memory segment operation (including program or erase). The reset command must be written two consecutive times after the program set-up command. This will safely reset the segment memory to the read mode. Memory contents are not altered. Following any other command, write the reset command once to the segment. This will safely abort any operation and reset the device to the Read mode.

Table 6. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-up Command	Data = 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{Data}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation. Device is either powered-down, erase inhibit or program inhibit.

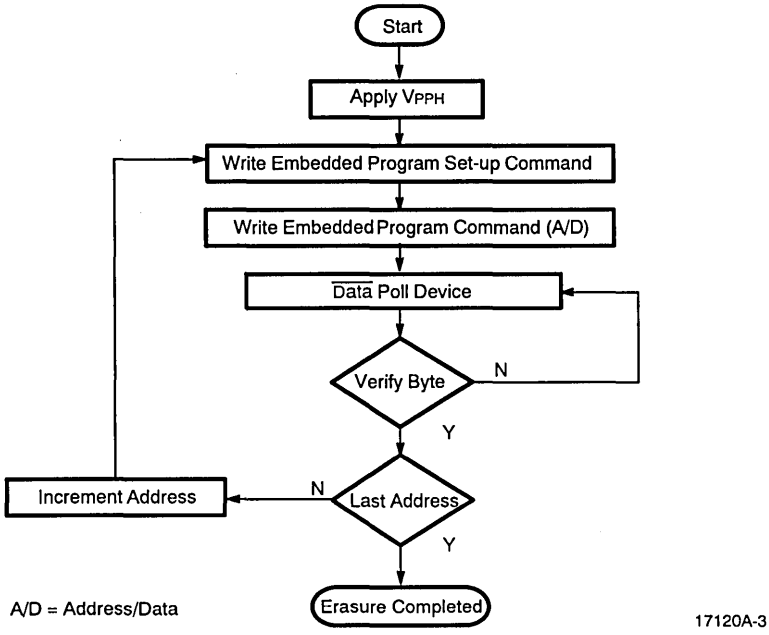


Figure 2. Embedded Programming Algorithm in Byte-Wide Mode

Write Operation Status

Data Polling—DQ7

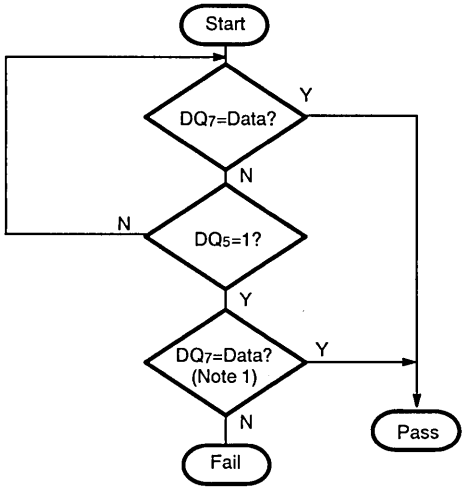
The Flash Memory PC Card features Data Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device will produce the compliment of expected Valid data on DQ7 of the addressed memory segment. Upon completion of the Embedded Program algorithm an attempt to read the device will produce Valid data on DQ7. The Data Polling feature is valid after the rising edge of the second WE pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The Data Polling feature is valid after the rising edge of the second WE pulse of the two Write pulse sequence.

The Data Polling feature is only active during Embedded Programming or erase algorithms.

See Figures 3a and 4a for the Data Polling timing specifications and diagrams.



Note:

1. DQ_7 is rechecked even if DQ_5 = 1 because DQ_7 may change simultaneously with DQ_5.

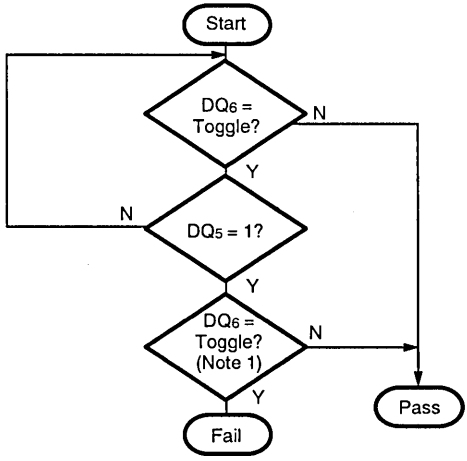
Figure 3a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Flash Memory PC Card also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the first $\overline{\text{WE}}$ pulse of the two write pulse sequence, unlike $\overline{\text{Data}}$ Polling which is valid after the rising edge of the second $\overline{\text{WE}}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

See Figures 3b and 4a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.



Note:

1. DQ_6 is rechecked even if DQ_5 = 1 because DQ_6 may stop toggling at the same time as DQ_5 changing to "1".

Figure 3b. Toggle Bit Algorithm

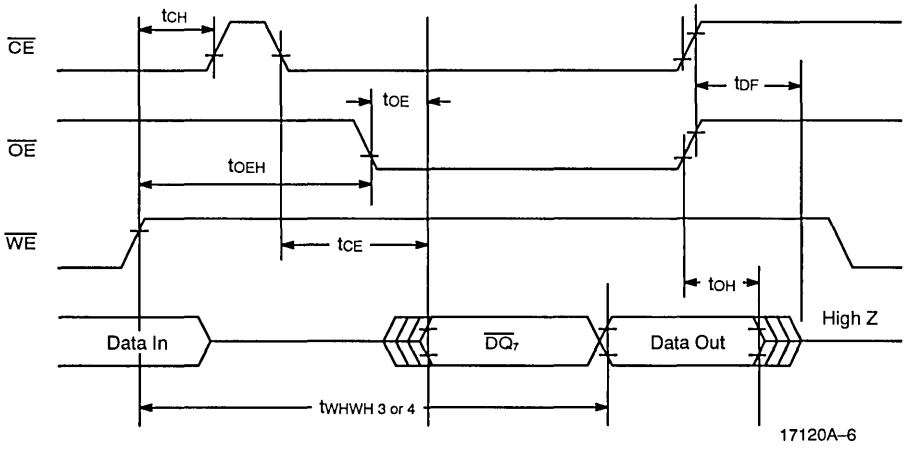
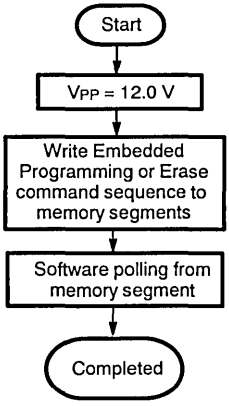


Figure 4a. AC Waveforms for Data Polling During Embedded Algorithm Operations

EMBEDDED ALGORITHM BYTE-WIDE PROGRAMMING AND ERASURE OVERVIEW

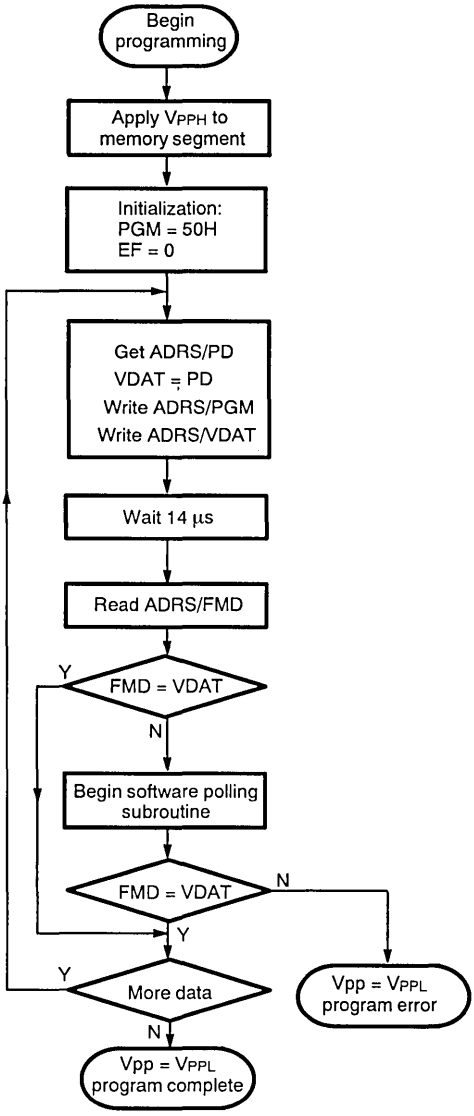


17120A-9

The Embedded Algorithm operations completely automate the programming and erase procedure by internally executing the algorithmic command sequence of original AMD devices. The devices automatically provide Write Operation Status information with standard read operations (addresses are a don't care).

Figure 5.

EMBEDDED ALGORITHM BYTE-WIDE PROGRAMMING FLOW CHART

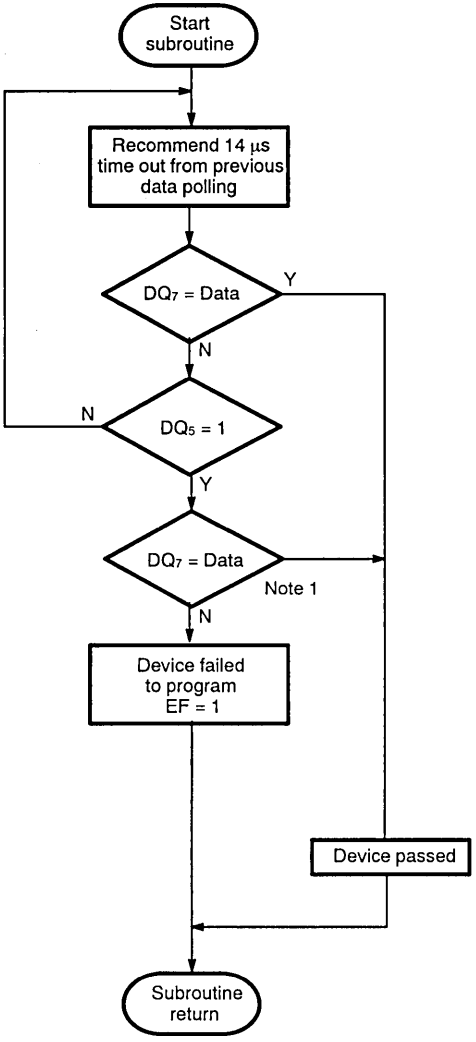


Activity	
Initialize Programming Variables:	*PGM = Embedded Set up Command*
	EF = Error Flag
ADRS = Appropriate address for memory segment.	
PD = Program Data	
VDAT = Valid Data.	
FMD = Flash Memory Data.	
EF = 0 = No Programming error	
EF = 1 = Programming error	

17120A–7

Figure 6.

EMBEDDED ALGORITHM BYTE-WIDE SOFTWARE POLLING FOR PROGRAMMING
Subroutine



DQ5 = 1
N = Program time not exceeded limit
Y = Program time exceed limit, device failed

17120A-8

Note:

1. DQ_7 is checked even if $DQ_5 = 1$ because DQ_7 may have changed simultaneously with DQ_5 or immediately after DQ_5.

Figure 7.

EMBEDDED ALGORITHM BYTE-WIDE ERASURE FLOW CHART

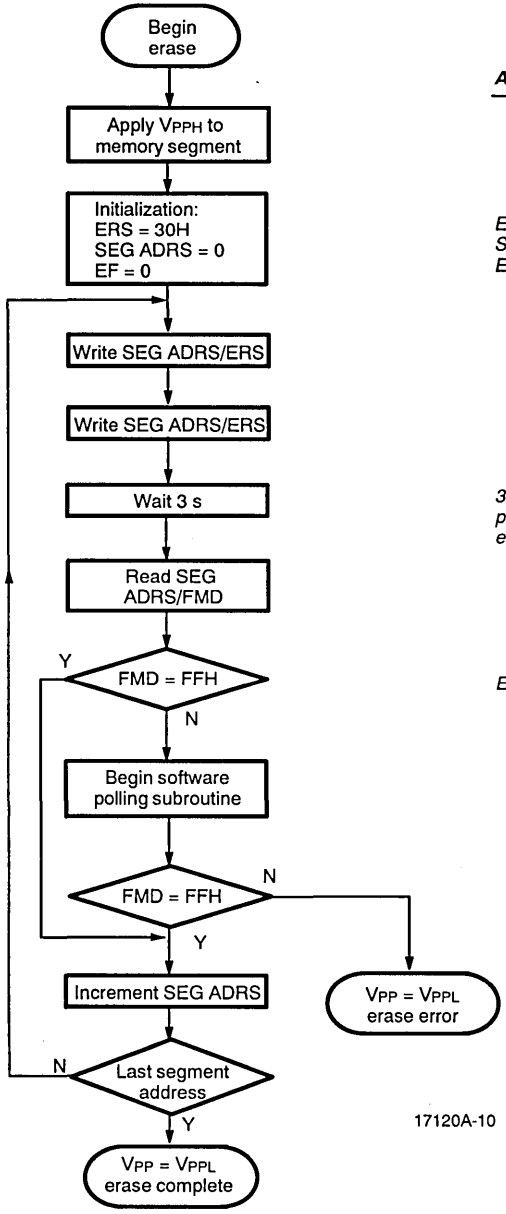
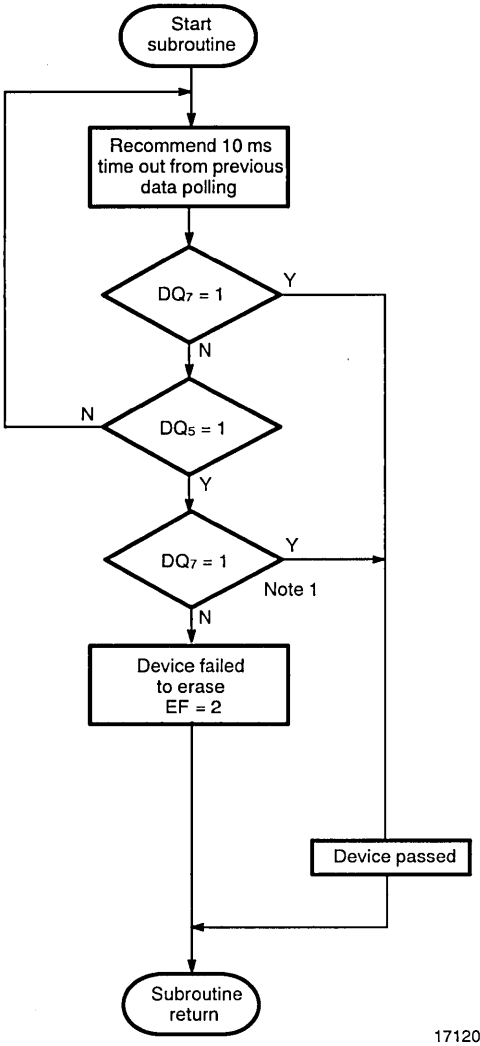


Figure 8.

EMBEDDED ALGORITHM BYTE-WIDE SOFTWARE POLLING ERASE SUBROUTINE



DQ7 = 1
Y = Erase Complete
N = Erase not Complete

DQ5 = 1
Y = Erase time exceeded limit, Device failed.
N = Erase time has not exceeded limit.

Figure 9.

WORD-WIDE PROGRAMMING AND ERASING

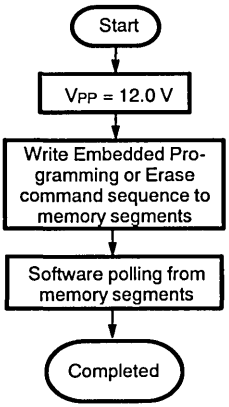
Word-Wide Programming

The word-wide programming sequence will be as usual. The program word command is 5050H. Each byte is independently programmed. For example, if the high byte of the word indicates the successful completion of programming via one of its program status bits such as DQ7, software polling should continue to monitor the low byte for program completion and data verification. During the Embedded Programming operations the device executes programming pulses in 14 μs increments. Status reads provide information on the progress of the byte programming relative to the last complete program pulse. Status information is automatically updated upon completion of each internal program pulse. Status information does not change within the 14 μs program pulse width.

Word-Wide Erasing

The word-wide erasing is similar to word-wide programming. The erase word command is 3030H. Each byte is independently erased and verified. Word-wide erasure reduces total erase time when compared to byte erasure. Each Flash memory device in the card may erase at different rates. Therefore each device (byte) must be verified separately. The alternate method mentioned above also apply to erasure. Since the same 40 MHz system, 1 second of CPU time is equivalent to 40 million clock cycles.

EMBEDDED ALGORITHM WORD-WIDE PROGRAMMING AND ERASURE OVERVIEW

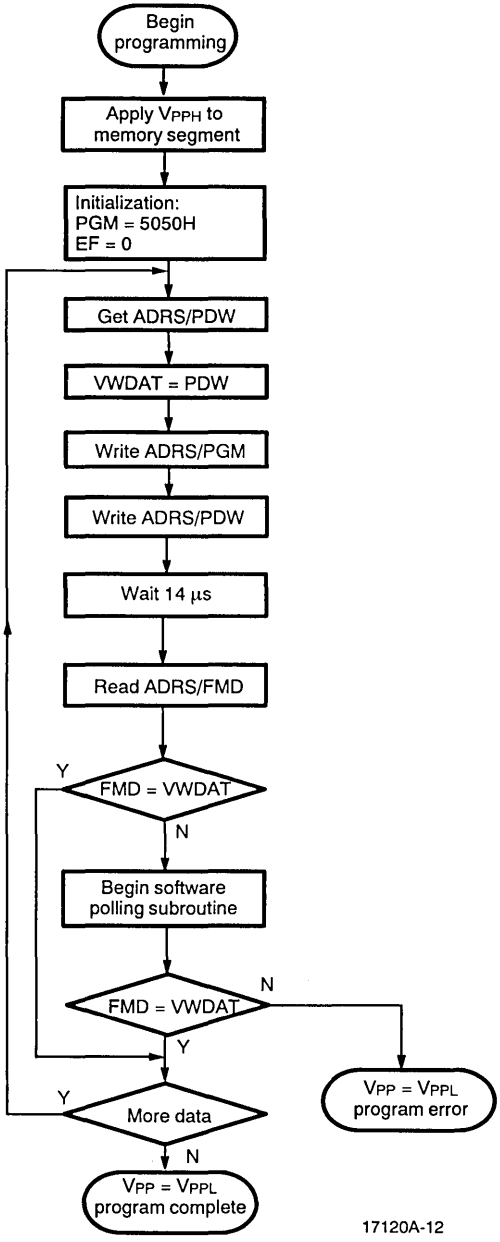


17120A-14

The Embedded Algorithm operations completely automate the parallel programming and erase procedures by internally executing the algorithmic command sequences of AMD's Flashrite and Flasherase algorithms. The devices automatically provide Write Operation Status information with standard read operations.

Figure 10.

EMBEDDED ALGORITHM WORD-WIDE PROGRAMMING FLOW CHART



Activity

Initialize Programming Variables:
PGM = Embedded Set up Command
EF = Error Flag

ADRS = Appropriate address for memory segment.
PDW = Program Data Word
VWDAT = Valid Word Data
EF = Error Flag
EF = 0 = No failure
EF = 1 = Low byte program error
EF = 2 = High byte program error
EF = 3 = Word-wide program error

FMD = Valid Word Data

Figure 11.

EMBEDDED ALGORITHM WORD-WIDE SOFTWARE POLLING PROGRAM SUBROUTINE

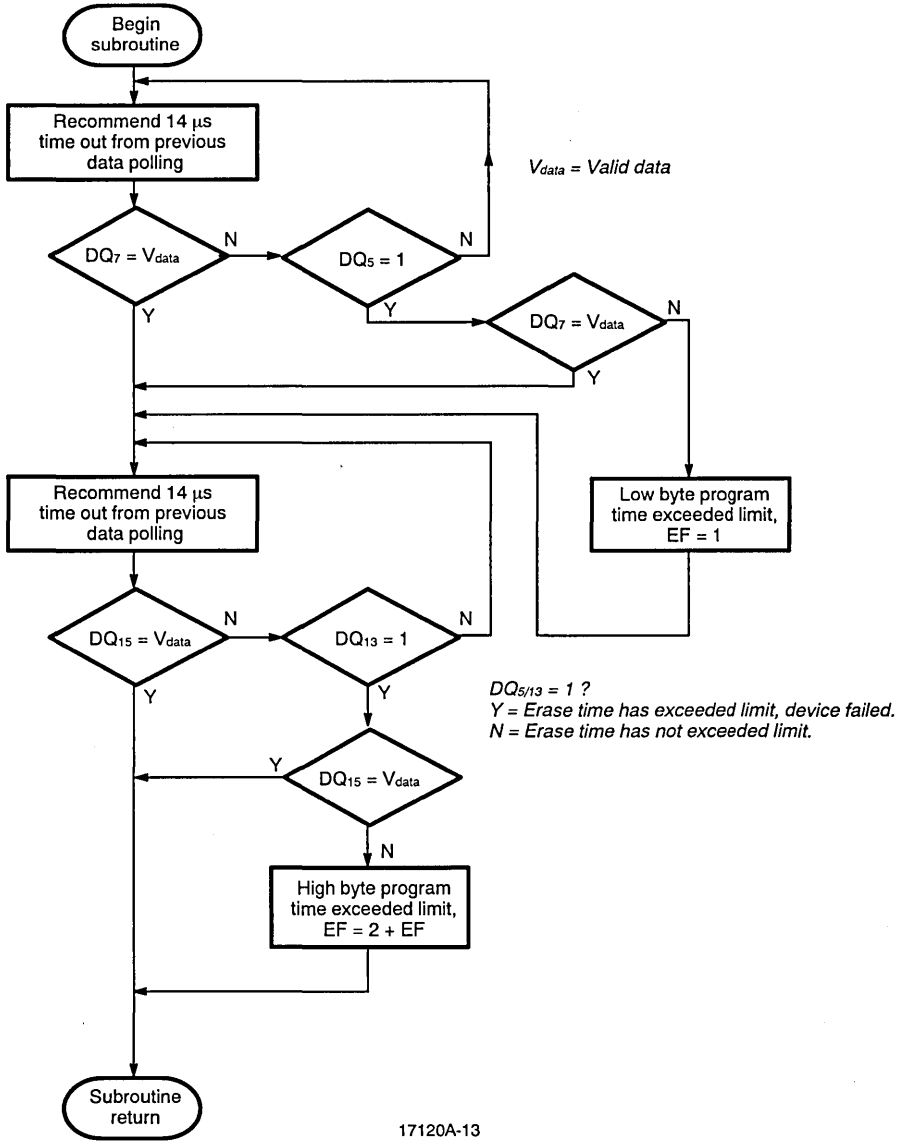
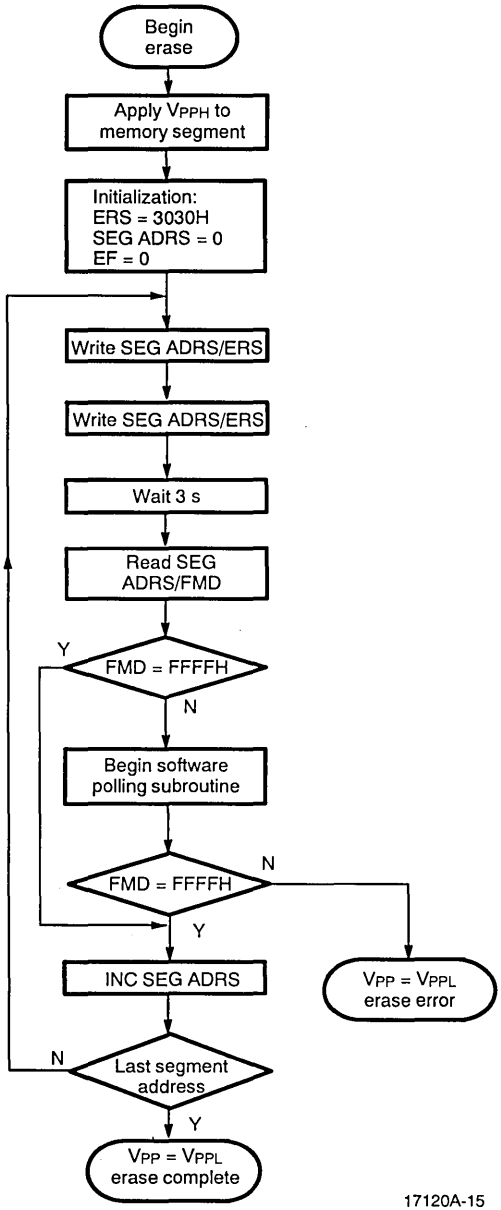


Figure 12.

EMBEDDED ALGORITHM WORD-WIDE ERASURE FLOW CHART



17120A-15

Activity

ERS = Erase Command
SEG ADRS = Segment Address

EF = Error Flag
EF = 0 = No failure
EF = 1 = Low byte Erase error
EF = 2 = High byte Erase error
EF = 3 = Word-wide Erase error

FMD = Flash Memory Data

Figure 13.

EMBEDDED ALGORITHM WORD-WIDE SOFTWARE POLLING ERASE SUBROUTINE

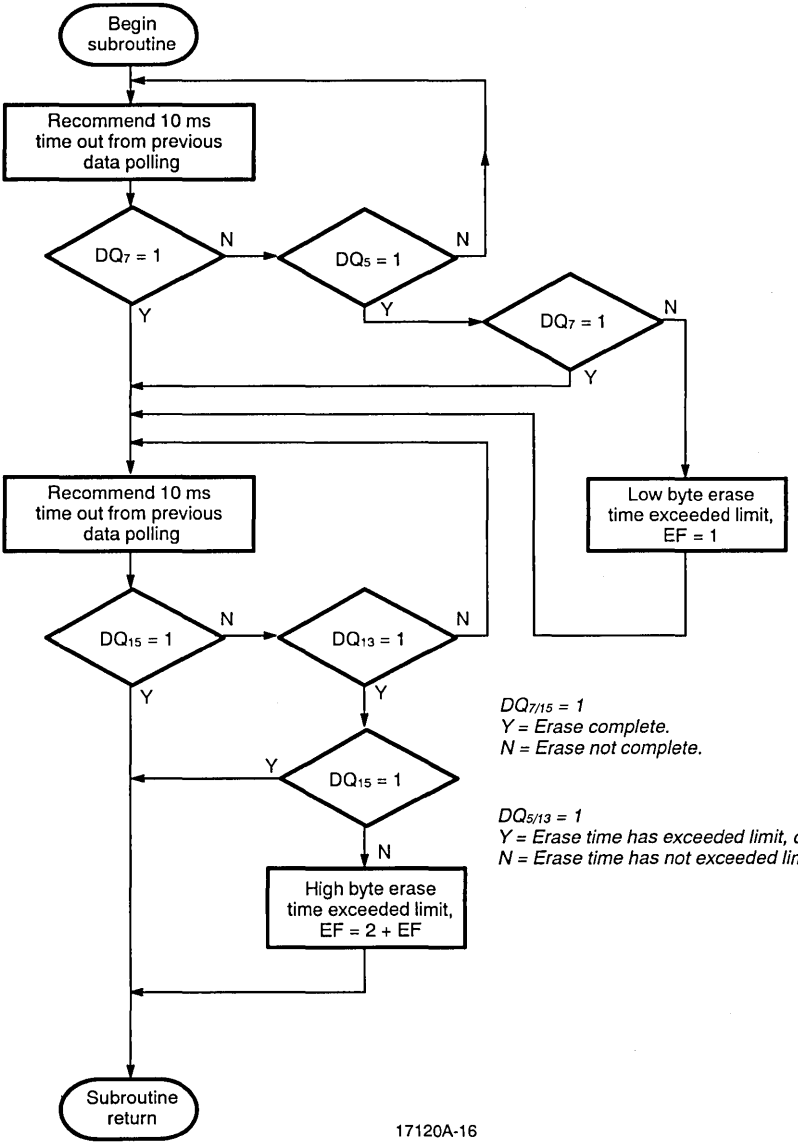


Figure 14.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... – 30°C to +70°C

Ambient Temperature
with Power Applied ..... – 10°C to +70°C

Voltage with Respect To Ground
All pins except V_{PP} (Note 1) ..... – 2.0 V to +7.0 V

V_{CC} (Note 1) ..... – 2.0 V to +7.0 V

V_{PP} (Note 2) ..... – 2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on V_{PP} pins is –0.5 V. During voltage transitions, V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = V_{CC} max. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +60°C

V_{CC} Supply Voltages ..... +4.75 V to 5.25 V

V_{PP} Supply Voltages

Read Only ..... 0 V to +6.5 V

Program, Erase, Verify,
and Read ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Byte Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. CE = V_{CC} ± 0.2 V		0.4	0.8	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., CE = V_{IL}, OE = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		25	50	mA
I_{CC2}	V_{CC} Programming Current	CE = V_{IL} Programming in Progress		3.0	30	mA
I_{CC3}	V_{CC} Erase Current	CE = V_{IL} Erasure in Progress		5.0	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			10	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.2	0.4	mA
		$V_{PP} \leq V_{CC}$			0.04	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		8.0	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. One Flash device active, seven in standby.
2. Only one Vpp is active.

DC CHARACTERISTICS

Word-Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.2 V		0.4	0.8	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		40	80	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		6	60	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	60	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} ≤ V_{CC}			10	µA
I_{PP1}	V_{PP} Read Current	V_{PP} > V_{CC}		0.4	0.8	mA
		V_{PP} ≤ V_{CC}			0.08	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		16	60	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		20	60	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = 2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. Two Flash devices active, six in standby.
2. V_{pp1} and V_{pp2} are active.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Capacitance	V_{IN} = 0		21	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		21	pF
C_{IN2}	Control Capacitance	V_{IN} = 0 ($\overline{CE}$, $\overline{REG}$)		47	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = 0		21	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz.

SWITCHING AC CHARACTERISTICS

Read Only Operation (Note 1)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{RC}	Read Cycle Time	250		ns
t_{ELQV}	t_{CE}	Chip Enable Access Time		250	ns
t_{AVQV}	t_{ACC}	Address Access Time		250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time		150	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	5		ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z		60	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z		60	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
t_{WHGL}		Write Recovery Time before Read	6		µs

Note:

1. Input Rise and Fall Times (10% to 90%): ≤ 10 ns, Input Pulse levels: V_{OL} and V_{OH}, Timing Measurement Reference Level – Inputs: V_{IL} and V_{IH} Outputs: V_{IL} and V_{IH}

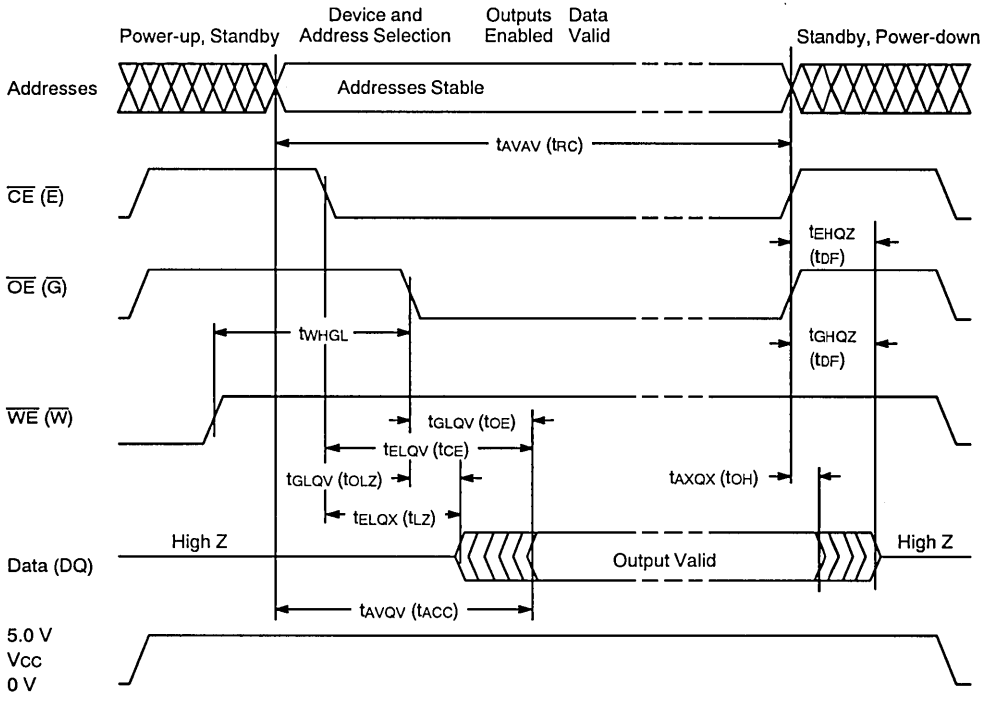
AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVWL}	t_{AS}	Address Set-Up Time	0		ns
t_{WLAX}	t_{AH}	Address Hold Time	100		ns
t_{DVWH}	t_{DS}	Data Set-Up Time	80		ns
t_{WHDX}	t_{DH}	Data Hold Time	30		ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm	30		ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHWL}		Read Recovery Time before Write	0		µs
t_{WLOZ}		Output in High-Z from Write Enable	5		ns
t_{WHOZ}		Output in Low-Z from Write Enable		60	ns
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	40		ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	100		ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	50		ns
t_{WHWH3}		Embedded Programming Operation (Notes 1, 2, 3)	14		µs
t_{WHWH4}		Embedded Erase Operation for each 128K byte Memory Segment (Notes 1, 2, 4)	3		s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	100		ns

Notes:

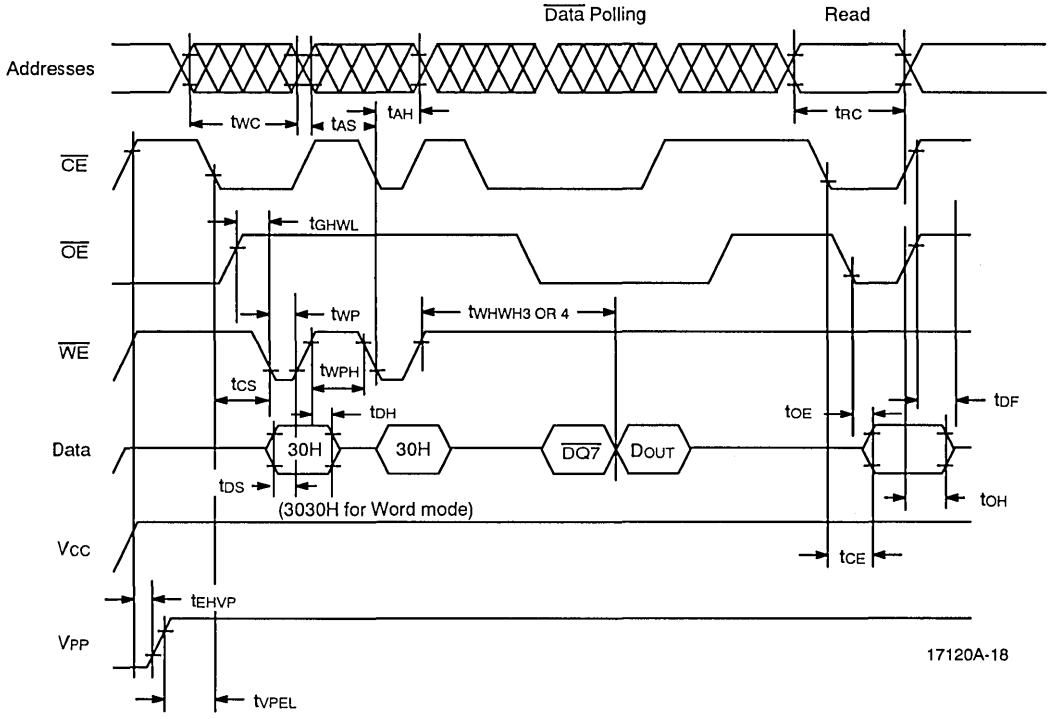
1. Rise/Fall < = 10 ns.
2. Maximum specification not needed due to the devices internal stop timer that will stop any erase or write operation that exceed the device specification.
3. Embedded Program Operation of 14 µs consist of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
4. Embedded Erase Operation of 3 seconds consists of 2 seconds memory segment pre-programming times and 1 second memory segment erase time for each 128K byte memory segment. This is typical time for embedded erase operation.



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

17120A-17

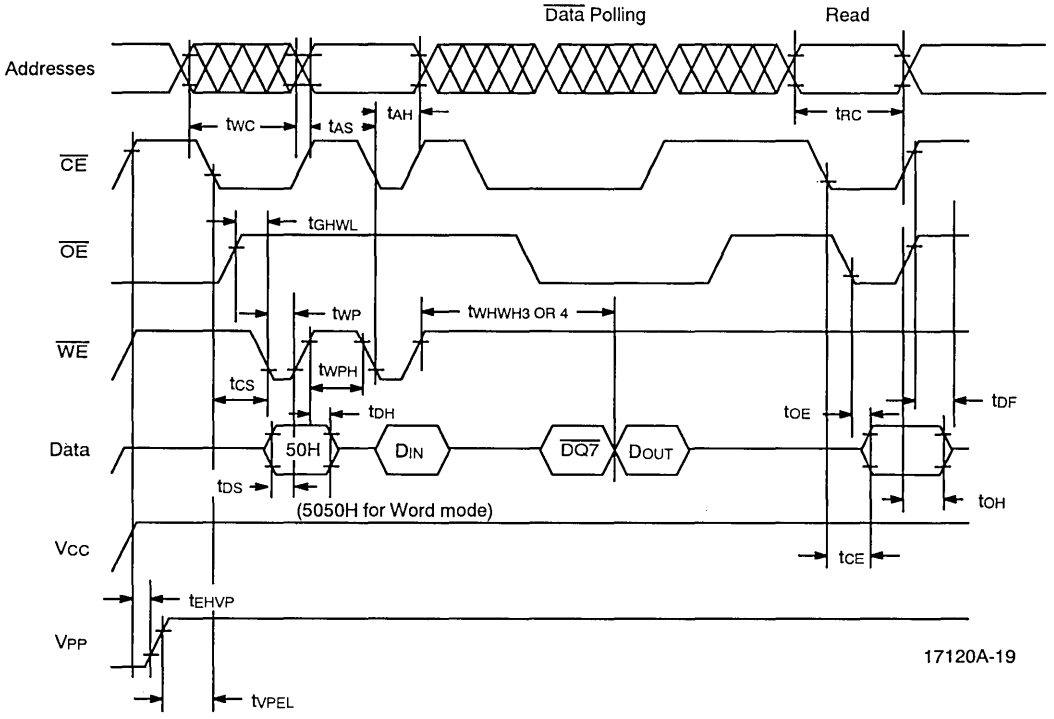
Figure 15. AC Waveforms for Read Operations



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 16. AC Waveforms for Embedded Erase Operation



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 17. AC Waveforms for Embedded Programming Operation

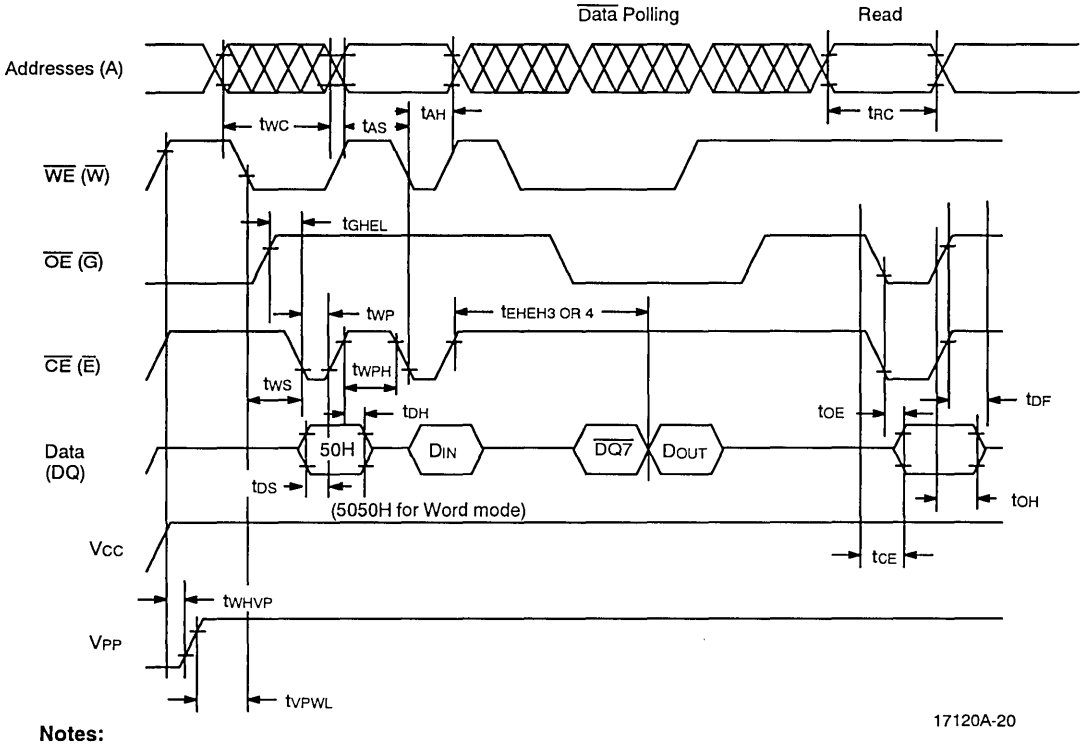
AC CHARACTERISTICS–ALTERNATE $\overline{CE}$ CONTROLLED WRITES

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVEL}	t_{AS}	Address Set-Up Time	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	100		ns
t_{DVEH}	t_{DS}	Data Set-Up Time	80		ns
t_{EHDX}	t_{DH}	Data Hold Time	30		ns
t_{GLDV}	t_{OE}	Output Enable Hold Time for Embedded Algorithm	10	150	ns
t_{GHEL}		Read Recovery Time before Write	0		µs
t_{WLEL}	t_{WS}	WE Set-Up Time before $\overline{CE}$	0		ns
t_{EHWH}	t_{CP}	WE Hold Time	0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	100		ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH (Note 3)	50		ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	14		µs
t_{EHEH4}		Embedded Erase Operation for each 128K byte Memory Segment (Notes 1, 2, 4)	3		s
t_{VPWL}		V_{PP} Set-Up Time to Write Enable LOW	100		ns

Notes:

1. Rise/Fall < =10 ns
2. Maximum specification not needed due to the internal stop timer that will stop any erase or write operation that exist the device specification.
3. Chip Enable Controlled Programming:
   Flash Programming is controlled by the valid combination of the Chip Enable ($\overline{CE}_{1,2}$) and Write Enable ($\overline{WE}$) signals. For system that uses the Chip Enable signal(s) to define the write pulse width, all Set-up, Hold, and inactive Write Enable timing should be measured relative to the Chip Enable signal(s).
4. Embedded Program Operation of 14 µs consist of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
5. Embedded Erase Operation of 3 seconds consists of 2 seconds memory segment pre-programming times and 1 second memory segment erase time for each 128K byte memory segment. This is typical time for embedded erase operation.



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 18. Alternate AC Waveforms for $\overline{CE}$ Controlled Embedded Programming or Erasing Operation

CARD INFORMATION STRUCTURE

The AmC001AFLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. All or part of the 512 byte could be used for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space. Part of the common memory space could also be mapped into the attribute memory space if more than 512 bytes of CIS are needed.

The EEPROM used in the AmC001AFLKA is a NEC μPD28C05GX-20-EJA designed to operate from a 5 V single power supply. The μPD28C05 provides a DATA polling function that provides the End of Write Cycle, Chip Erase and Auto Erase and Programming functions.

SYSTEM DESIGN AND INTERFACE INFORMATION

Power Up and Power Down Protection

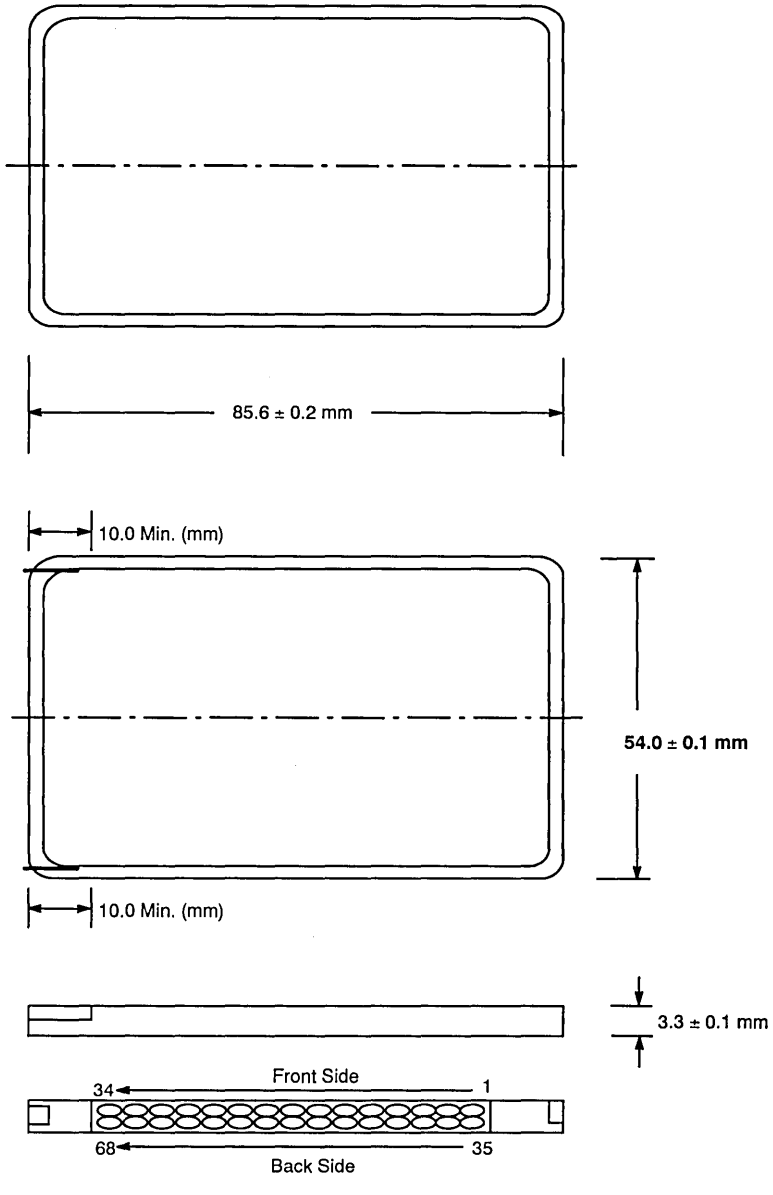
The PCMCIA standard socket provides for proper power up and power down sequencing via different pin lengths to ensure that hot insertion and removal of the PC card will not result in card damage or data loss.

AMD's Flash memory devices are designed to protect against accidental programming or erasure caused by spurious system signals that might exist during hot insertion, hot removal, or power transitions. The AMD PC card will power-up into a READ mode and the card will function as a read only memory as long as V_{pp} is less than V_{cc} +2 V. Erasing of the memory segments can be accomplished only by writing the proper Erase command to the card twice along with the proper Chip Enable, Output Enable and Write Enable control signals.

System Power Supply Decoupling

The AMD Flash memory card has a 0.1 μF decoupling capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins. It is recommended the system side also have a 4.7 μF capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins.

PHYSICAL DIMENSIONS
Type 1 PC Card



17120A-21

PRELIMINARY

AmC002AFLKA

2 Megabyte Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 250 ns maximum access time
- **CMOS low power consumption**
  - 25 mA typical active current (X8)
  - 400 μA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **High re-programmable endurance**
  - Minimum 100,000 erase/write cycles
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate attribute memory**
  - 512 byte EEPROM
- **Automated Write and Erase Operations (Increases System Write Performance)**
  - 256K byte memory segment
  - Typically <1.5 seconds per single memory segment erase
  - Random address writes to previously erased bytes (14 μs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Insertion and removal force**
  - State of art connector allows for minimum card insertion and removal effort
- **Write and erase voltage, 12.0 V ± 5%**
- **Read voltage, 5 V ± 5%**
- **Manufactured by DuPont Connector Systems**

GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC002AFLKA. This allows OEM manufacturers of portable system to eliminate the weight, extreme power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC002AFLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC002AFLKA enhances the productivity of mobile workers.

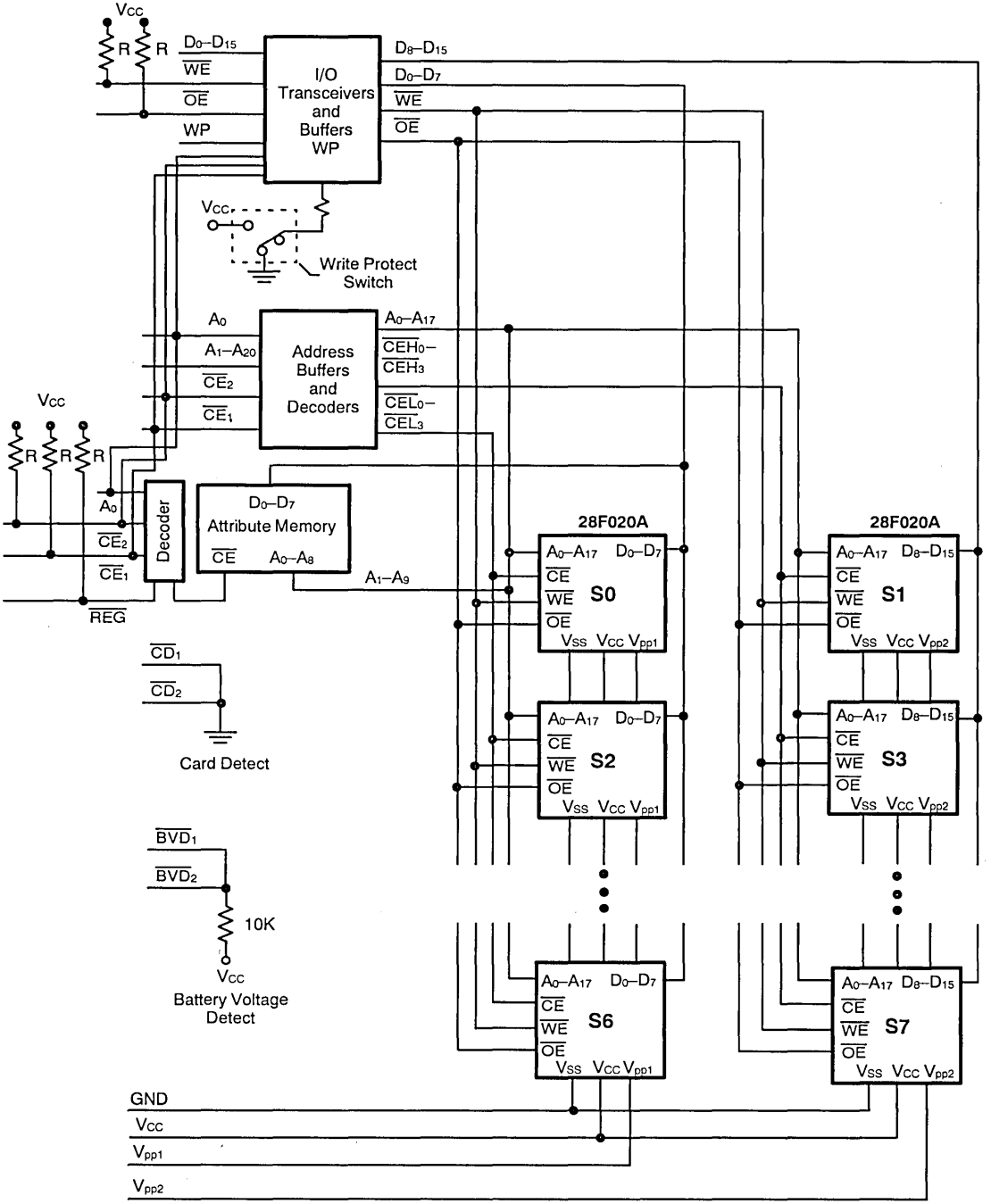
Widespread acceptance of the AmC002AFLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC002AFLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by DuPont Connector Systems

Publication# 17273 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



R=33K

17273A-1

PC CARD PIN ASSIGNMENTS

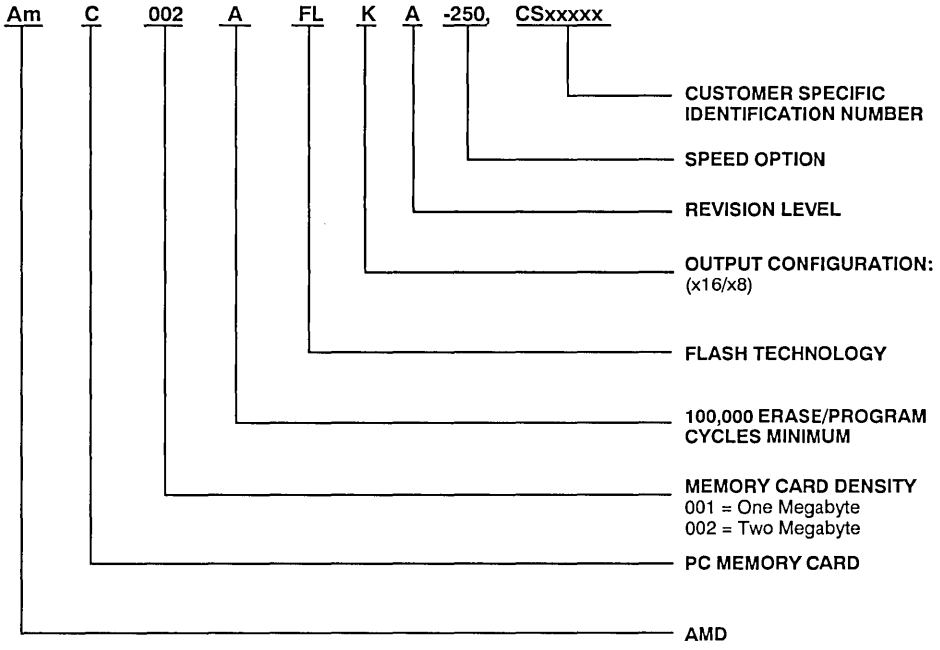
Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable (Note 1)	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2 (Note 1)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	RFU		Reserved
11	A_9	I	Address Bit 9	45	RFU		Reserved
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	A_{20}	I	Address Bit 20
16	NC		No Connect	50	NC		No Connect
17	V_{CC}		Power Supply	51	V_{CC}		Power Supply
18	V_{PP1}		Pgm Sply Vltg 1	52	V_{PP2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.
1. Signal must not be connected between cards
2. $\overline{BVD}$ = Internally pulled-up

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



PIN DESCRIPTION

Symbol	Type	Name and Function
A_0 - A_{20}	INPUT	**ADDRESS INPUTS** are internally latched during write cycles.
$D_0 - D_{15}$	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Data inputs are internally latched on write cycles. Data outputs during read cycles. Data pins are active high. When the memory card is de-selected or the outputs are disabled the outputs float to tri-state.
$\overline{CE_1}$, $\overline{CE_2}$	INPUT	**CARD ENABLE** is active low. The memory card is de-selected and power consumption is reduced to stand-by levels when $\overline{CE}$ is high. $\overline{CE}$ activates the internal memory card circuitry that controls the high and low byte control logic of the card, input buffers segment decoders, and associated memory devices.
$\overline{OE}$	INPUT	**OUTPUT ENABLE** is active low and enables the data buffers through the card outputs during read cycles.
$\overline{WE}$	INPUT	**WRITE ENABLE** is active low and controls the write function of the command register to the memory array. The target address is latched on the falling edge of the $\overline{WE}$ pulse and the appropriate data is latched on the rising edge of the pulse.
V_{PP1},V_{PP2}		**ERASE/WRITE POWER SUPPLY** for erase and programming. V_{pp} enables the command register which controls all functions required to alter the memory array contents. **Note:** The Memory Card functions in a read-only memory when $V_{PP} < V_{cc} + 2$ V.
V_{CC}		**PC CARD POWER SUPPLY** for device operation (5.0 V ± 5%)
GND		**GROUND**
CD_1, CD_2	OUTPUT	**CARD DETECT.** When card detect 1 and 2 = ground the system detects the card.
WP	OUTPUT	**WRITE PROTECT** is active high and disables all card write operations.
NC		**NO CONNECT** - corresponding pin is not connected internally to the die.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT.** Internally pulled-up.

MEMORY CARD OPERATIONS

The AmC002AFLKA Flash Memory Card is organized as an array of individual devices. Each device is 256K bytes in size. Although the address space is continuous each physical device defines a logical address segment size. Erase operations are performed in increments of this segment size. Multiple segments may be erased concurrently when additional V_{pp} current is supplied to the device. Once a memory segment is erased any address location may be programmed. Flash technology allows any logical "1" data bit to be programmed to a logical "0". The only way to reset bits to a logical "1" is to erase the entire memory segment of 256K bytes. High voltage is required on V_{pp1} and V_{pp2} to perform program and erase operations.

The common memory space data contents are altered in a similar manner as writing to individual Flash Memory devices. On-card address and data buffers activate the appropriate Flash device in the memory array. Each device internally latches address and data during write cycles. Refer to Table 2A.

Attribute memory is a separately accessed card memory space. The register memory space is active when the $\overline{REG}$ pin is driven low. The Card Information Structure describes the capabilities and specification of a card. The CIS is stored in the attribute memory space beginning at address 00000H. The AmC002AFLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. Alternatively, the CIS can be stored at the beginning of the common memory address space. D_0–D_7 are active during attribute memory accesses. D_8–D_{15} should be ignored. Odd order bytes present invalid data. Refer to Table 2B.

Word-Wide Operations

The AmC002AFLKA provides the flexibility to operate on data in a byte-wide or word-wide format. In word-wide operations the Low-bytes are controlled with V_{pp1} and $\overline{CE_1}$ when A0 = 0. The High-bytes are controlled with V_{pp2} and $\overline{CE_2}$, A0 = don't care.

Erase operations are the only operations that work on entire memory segment. All other operations such as word-wide programming are not affected by the physical memory segments.

Byte-Wide Operations

Byte-wide data is available on D_0–D_7 for read and write operations ($\overline{CE}_1$ = low, $\overline{CE}_2$ = high). Even and odd bytes are stored in separate memory segments (i.e. S_0 and S_1) and are accessed when A0 is low and high respectively. The even byte is the low order byte and the odd byte is the high order byte of a 16-bit word.

Erase operations in the byte-wide mode must account for data multiplexing on D_0–D_7 by changing the state of A0. Each memory segment pair must be addressed separately for erase operations.

Card Detection

Each $\overline{CD}$ (output) pin should be read by the host system to determine if the memory card is adequately seated in the socket. $\overline{CD}_1$ and $\overline{CD}_2$ are internally tied to ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

Write Protection

The AMD Flash memory card has three types of write protection. The PCMCIA/JEIDA socket itself provides the first type of write protection. Power supply and control pins have specific pin lengths in order to protect the card with proper power supply sequencing in the case of hot insertion and removal.

A mechanical write protect switch provides a second type of write protection. When this switch is activated, $\overline{WE}$ is internally forced high. The Flash memory command register is disabled from accepting any write commands.

The third type of write protection is achieved with V_{pp1} and V_{pp2} at logic low levels to reset the Flash devices to read-only mode. Memory contents can not be changed in this state. The command register of individual Flash memory segments is only active when V_{pp1} and/or V_{pp2} are at high voltage (V_{ppH}).

Each Flash memory device that comprises a Flash memory segment will reset the command register to the read-only mode when V_{cc} is below VLKO. VLKO is the voltage below which write operations to individual command registers are disabled.

MEMORY CARD BUS OPERATIONS

Read Enable

Two Card Enable ($\overline{CE}$) pins are available on the memory card. Both $\overline{CE}$ pins must be active low for word-wide read accesses. Only one $\overline{CE}$ is required for byte-wide accesses. The $\overline{CE}$ pins control the selection and gates power to the high and low memory segments. The Output Enable ($\overline{OE}$) controls gating accessed data from the memory segment outputs.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state.

Standby Operations

Byte-wide read accesses only require half of the read/write output buffer (x16) to be active. In addition, only one memory segment is active with in either the high order or low order bank. Activation of the appropriate half of the output buffer is controlled by the combination of both $\overline{CE}$ pins. The $\overline{CE}$ pins also control power to the high and low-order banks of memory. Outputs of the memory bank not selected are placed in the high impedance state. The individual memory segment is activated by the address decoders. The other memory segments operate in standby. An active memory segment continues to draw power until completion of a write, erase, or verify operation if the card is de-selected in the process of one of these operations.

Auto Select Operation

A host system or external card reader/writer can determine the on-card manufacturer and device I.D. codes. Codes are available after writing the 90H command to the command register of a memory segment. Reading from address location 00000H in any segment provides the manufacturer I.D. while address location 00002H provides the device I.D.

Write Operations

Write and erase operations are valid only when V_{pp1} and V_{pp2} are at high voltage. This activates the state machine of an addressed memory segment. The command register is a latch which saves address, commands, and data information used by the state machine and memory array.

When Write Enable ($\overline{WE}$) and appropriate $\overline{CE}$(s) are a logic-level low, the command register is enabled for write operations. The falling edge of $\overline{WE}$ latches address information and the rising edge latches data/command information.

Memory Segment Command Definitions

When the V_{pp} pin(s) are at low voltage the command register of each Flash memory segment defaults to 00H, the Read only mode.

With high voltage on the V_{pp} pin(s), the Flash memory segments are active for either read, write, or erase operations.

Write or erase operations are performed by writing appropriate data patterns to the command register of accessed Flash memory segments.

The byte-wide and word-wide commands are defined in Tables 3 and 4 respectively.

Table 2A. Common Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Note 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Note 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Note 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	High Z
Read (x16) (Note 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out - Odd	Data Out-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Notes 2, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Data Out-Odd	High Z
Read (x16) (Notes 2, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Data Out-Odd	Data Out-Even
Write (x8) (Notes 4, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data In-Odd
Write (x8) (Notes 4, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Data In	High Z
Write (x16) (Notes 5, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Data In Odd	Data In-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, $V_{CC} + 2$ V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a byte write operation.
5. Refer to Table 4 for valid D_{IN} during a word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. Byte access – Even. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Byte access – Odd. In this x8 mode, $A_0 = V_{IH}$ outputs or inputs the "odd" byte (high byte) of the x16 word on D_0–D_7. This is accomplished internal to the card by transposing D_8–D_{15} to D_0–D_7.
9. Odd byte only access. In this x8 mode, A_0 = X outputs or inputs the "odd" byte (high byte) of the x16 word on D_8–D_{15}.
10. x16 word accesses present both "even" (low) and "odd" (high) bytes. $A_0 = V_{IL}$ or V_{IH} = "Don't Care".

Table 2B. Attribute Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Notes 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Not Valid
Read (x8) (Note 8)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	High Z
Read (x16) (Notes 8, 9, 10)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	Data Out-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Read (x8) (Note 9)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Read (x16) (Notes 2, 9)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Not Valid	Data Out-Even
Write (x8) (Notes 4, 7, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8, 10)	V_{IL}	V_{IIH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Write (x8) (Notes 4, 9, 10)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Write (x16) (Note 10)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Not Valid	Data In-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, $V_{CC} + 2$ V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a write operation.
5. Refer to Table 4 for valid D_{IN} during a write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Only even-byte data is valid during Attribute Memory Read function.
9. During Attribute Memory Read function, $\overline{REG}$ and $\overline{OE}$ must be active for the entire cycle.
10. During Attribute Memory Write function, $\overline{REG}$ and $\overline{WE}$ must be active for the entire cycle, $\overline{OE}$ must be inactive for the entire cycle.

Table 3. Command Definitions for Byte-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	90H	Read	00H/01H	01H/29H
Embedded Set-up/Erase Embedded Erase™ (Note 4)	Write	X	30H	Write	X	30H
Embedded Set-up Program/ Embedded Program™ (Note 5)	Write	X	50H	Write	PA	PD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Embedded Erase Algorithm.
5. Figure 2 illustrates the Embedded Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.
   Address: 00H/01H = MFG code/Device code addresses.
   Data: 01H/29H = MFG code data/Device code data.

Table 4. Command Definitions for Word-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	0000H/ FFFFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	9090H	Read	0000H/ 0101H	0101H/ 2929H
Embedded Erase Set-up/Erase	Write	SA	3030H	Write	X	3030H
Embedded Set-up Program/ Embedded Program	Write	X	5050H	Write	PA	PD
Reset (Note 6)	Write	X	FFFFH	Write	X	FFFFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Embedded Electrical Erase Algorithm.
5. Figure 2 illustrates the Embedded Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

Details of AMD's Embedded Program and Erase Operations

Embedded Erase™ Algorithm

The automatic memory segment erase does not require the device to be entirely pre-programmed prior to executing the Embedded Erase set-up command and Embedded Erase command. Upon executing the Embedded Erase command, the addressed memory segment automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the memory segment is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 of the memory segment is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase set-up command is a command only operation that stages the memory segment for automatic electrical erasure of all bytes in the array. Embedded Erase set-up is performed by writing 30H to the command register of the addressed memory segment.

To commence automatic segment erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 of the memory segment is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 1 and Table 5 illustrate the Embedded Erase algorithm, a typical command string and bus operations.

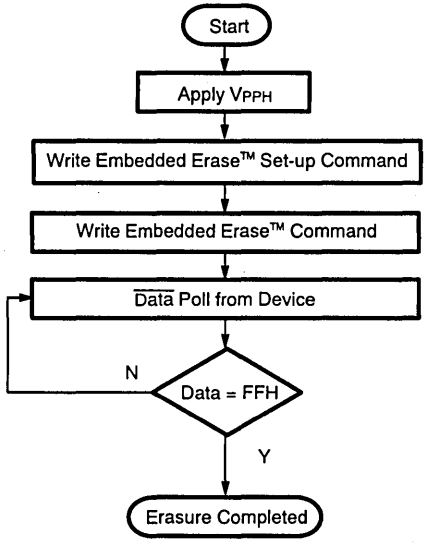


Figure 1. Embedded Erase Algorithm™ in Byte-Wide Mode

Table 5. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation.

Embedded Program™ Algorithm

The Embedded Program Set-up is a command only operation that stages the addressed memory segment for automatic programming. Embedded Program Set-up is performed by writing 50H to the command register.

Once the Embedded Program Set-up operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 of the addressed memory segment is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode (no program verify command is required).

Figure 2 and Table 6 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

Reset Command

The reset command initializes the memory segment to the read mode. In addition, it also provides a safe method to abort any memory segment operation (including program or erase). The reset command must be written two consecutive times after the program set-up command. This will safely reset the segment memory to the read mode. Memory contents are not altered. Following any other command, write the reset command once to the segment. This will safely abort any operation and reset the device to the Read mode.

Table 6. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-up Command	Data = 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{Data}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation. Device is either powered-down, erase inhibit or program inhibit.

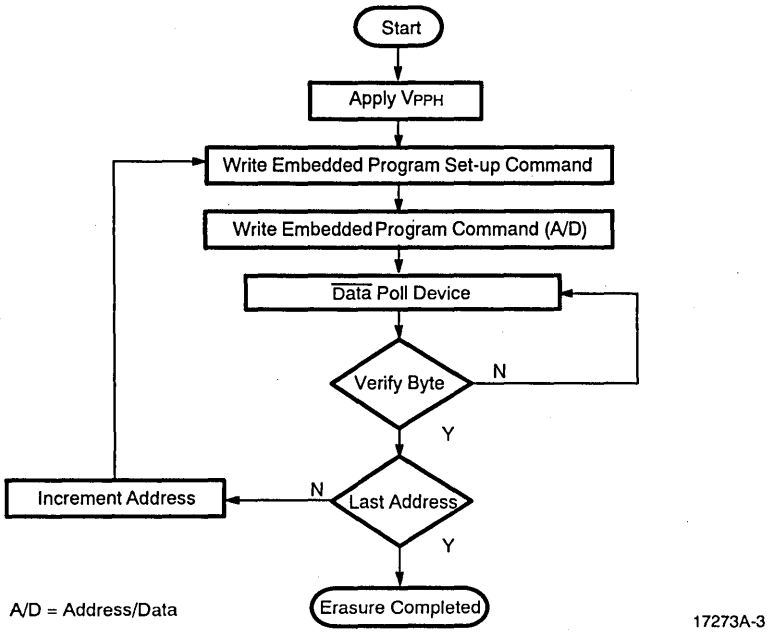


Figure 2. Embedded Programming Algorithm in Byte-Wide Mode

Write Operation Status

Data Polling—DQ7

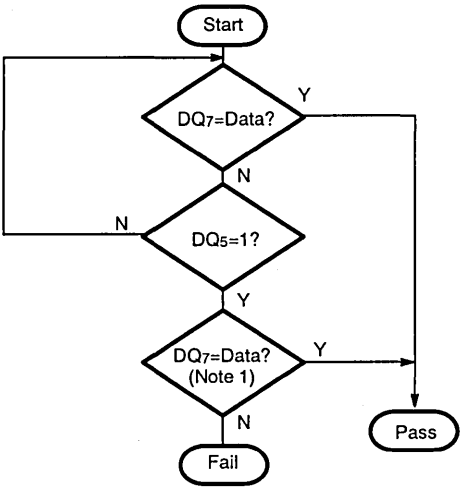
The Flash Memory PC Card features Data Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device will produce the compliment of expected Valid data on DQ7 of the addressed memory segment. Upon completion of the Embedded Program algorithm an attempt to read the device will produce Valid data on DQ7. The Data Polling feature is valid after the rising edge of the second WE pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The Data Polling feature is valid after the rising edge of the second WE pulse of the two Write pulse sequence.

The Data Polling feature is only active during Embedded Programming or erase algorithms.

See Figures 3a and 4a for the Data Polling timing specifications and diagrams.



Note:

1. DQ_7 is rechecked even if DQ_5 = 1 because DQ_7 may change simultaneously with DQ_5.

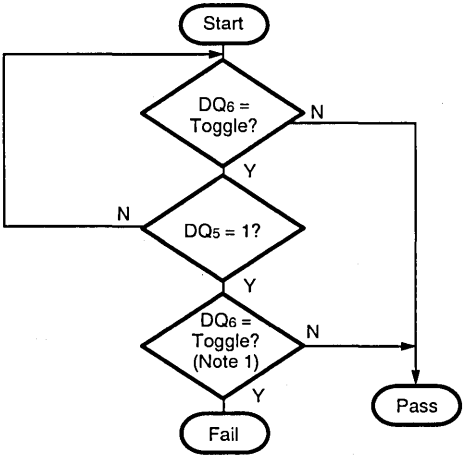
Figure 3a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Flash Memory PC Card also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the first $\overline{\text{WE}}$ pulse of the two write pulse sequence, unlike $\overline{\text{Data}}$ Polling which is valid after the rising edge of the second $\overline{\text{WE}}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

See Figures 3b and 4a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.



Note:

1. DQ_6 is rechecked even if DQ_5 = 1 because DQ_6 may stop toggling at the same time as DQ_5 changing to "1".

Figure 3b. Toggle Bit Algorithm

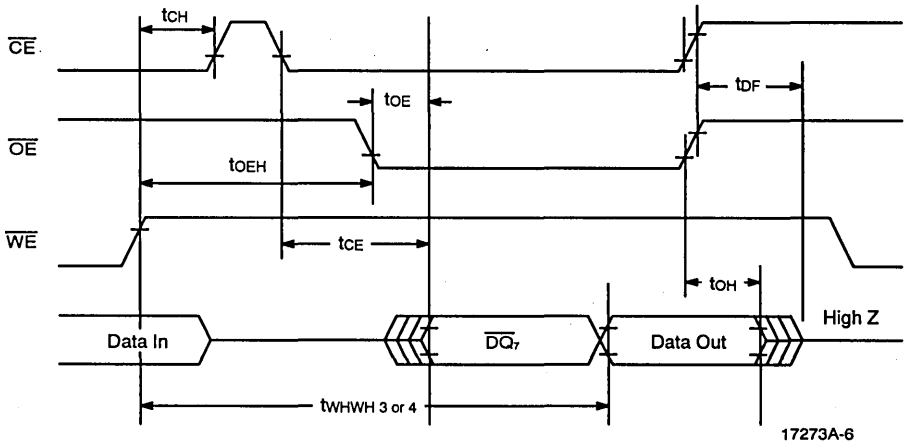
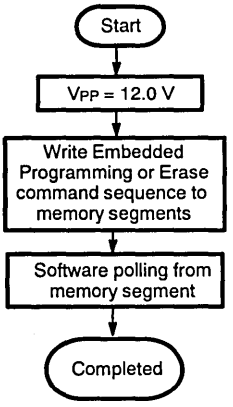


Figure 4a. AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations

EMBEDDED ALGORITHM BYTE-WIDE PROGRAMMING AND ERASURE OVERVIEW

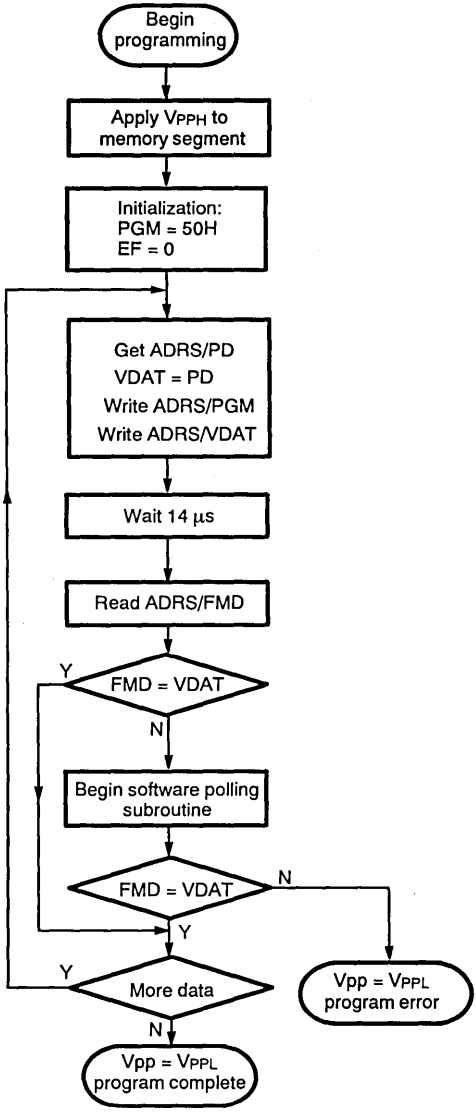


17273A-9

The Embedded Algorithm operations completely automate the programming and erase procedure by internally executing the algorithmic command sequence of original AMD devices. The devices automatically provide Write Operation Status information with standard read operations (addresses are a don't care).

Figure 5.

EMBEDDED ALGORITHM BYTE-WIDE PROGRAMMING FLOW CHART



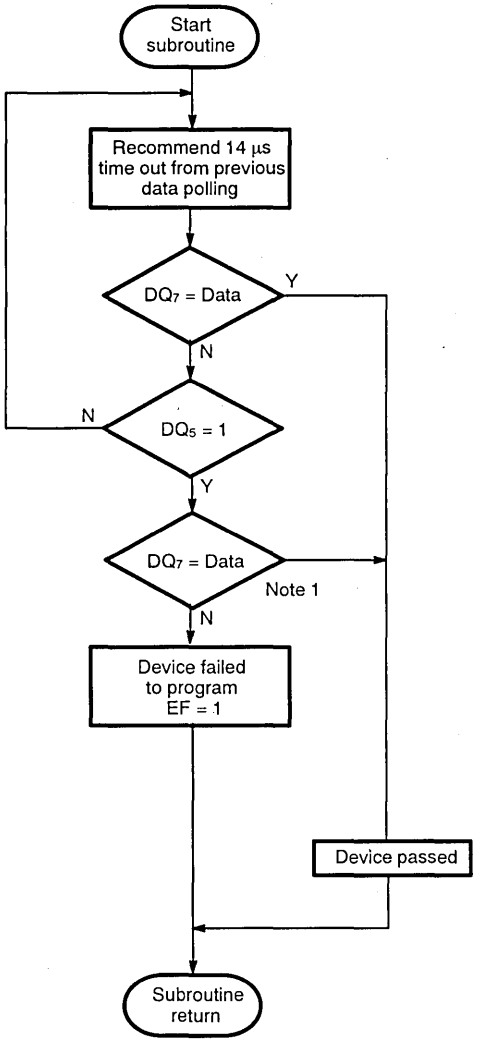
Activity	
Initialize Programming Variables:	*PGM = Embedded Set up Command* *EF = Error Flag*
ADRS = Appropriate address for memory segment.	*PD = Program Data* *VDAT = Valid Data.*
FMD = Flash Memory Data.	
EF = 0 = No Programming error	*EF = 1 = Programming error*

17273A-7

Figure 6.

EMBEDDED ALGORITHM BYTE-WIDE SOFTWARE POLLING FOR PROGRAMMING

Subroutine



DQ5 = 1
N = Program time not exceeded limit
Y = Program time exceed limit, device failed

17273A-8

Note:

1. DQ_7 is checked even if $DQ_5 = 1$ because DQ_7 may have changed simultaneously with DQ_5 or immediately after DQ_5.

Figure 7.

EMBEDDED ALGORITHM BYTE-WIDE ERASURE FLOW CHART

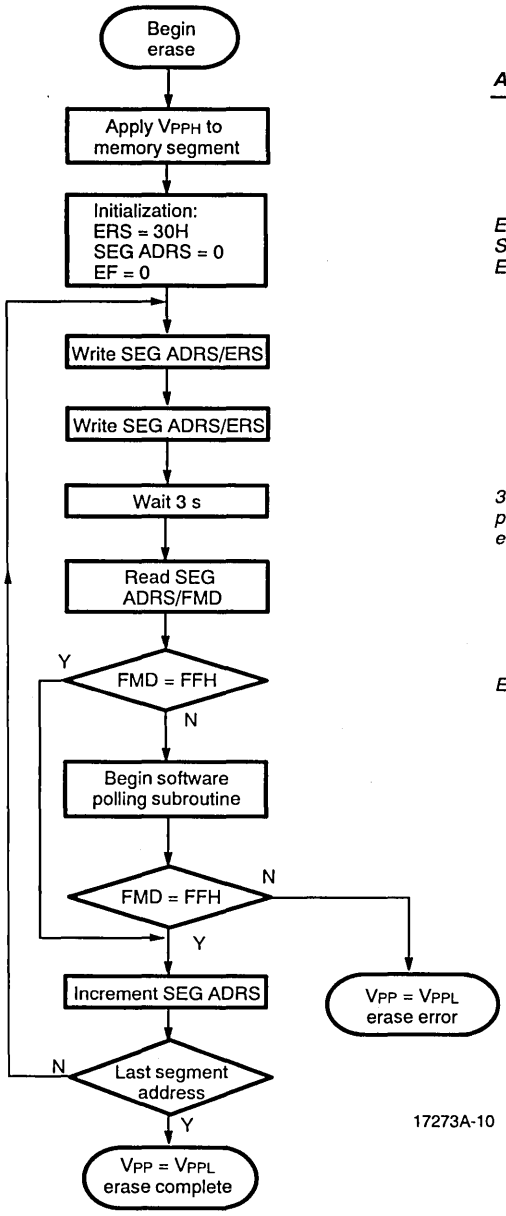
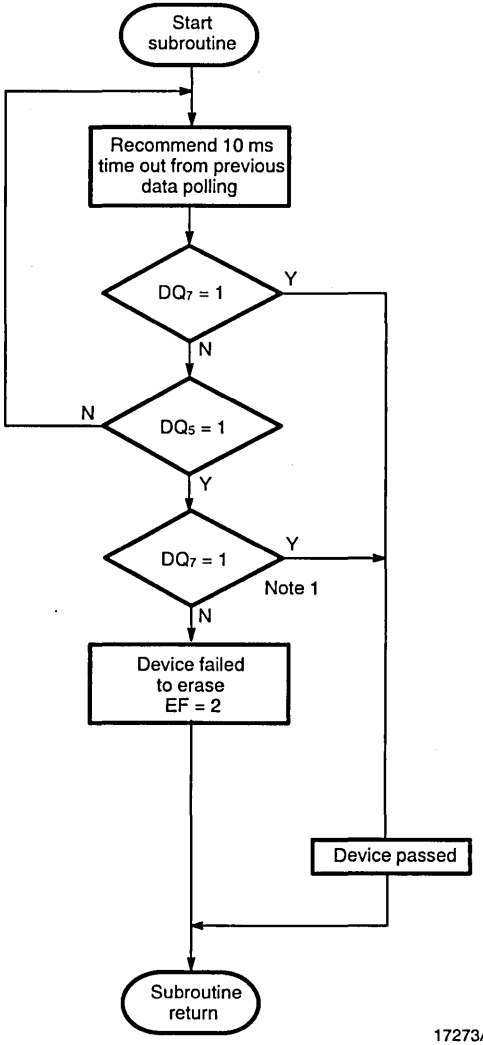


Figure 8.

EMBEDDED ALGORITHM BYTE-WIDE SOFTWARE POLLING ERASE SUBROUTINE



DQ7 = 1
Y = Erase Complete
N = Erase not Complete

DQ5 = 1
Y = Erase time exceeded limit, Device failed.
N = Erase time has not exceeded limit.

Figure 9.

WORD-WIDE PROGRAMMING AND ERASING

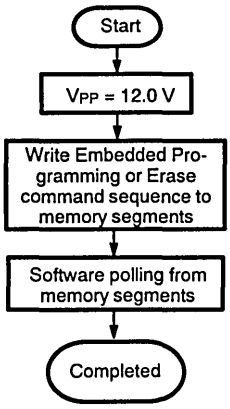
Word-Wide Programming

The word-wide programming sequence will be as usual. The program word command is 5050H. Each byte is independently programmed. For example, if the high byte of the word indicates the successful completion of programming via one of its program status bits such as DQ7, software polling should continue to monitor the low byte for program completion and data verification. During the Embedded Programming operations the device executes programming pulses in 14 μs increments. Status reads provide information on the progress of the byte programming relative to the last complete program pulse. Status information is automatically updated upon completion of each internal program pulse. Status information does not change within the 14 μs program pulse width.

Word-Wide Erasing

The word-wide erasing is similar to word-wide programming. The erase word command is 3030H. Each byte is independently erased and verified. Word-wide erasure reduces total erase time when compared to byte erasure. Each Flash memory device in the card may erase at different rates. Therefore each device (byte) must be verified separately. The alternate method mentioned above also apply to erasure. Since the same 40 MHz system, 1 second of CPU time is equivalent to 40 million clock cycles.

EMBEDDED ALGORITHM WORD-WIDE PROGRAMMING AND ERASURE OVERVIEW

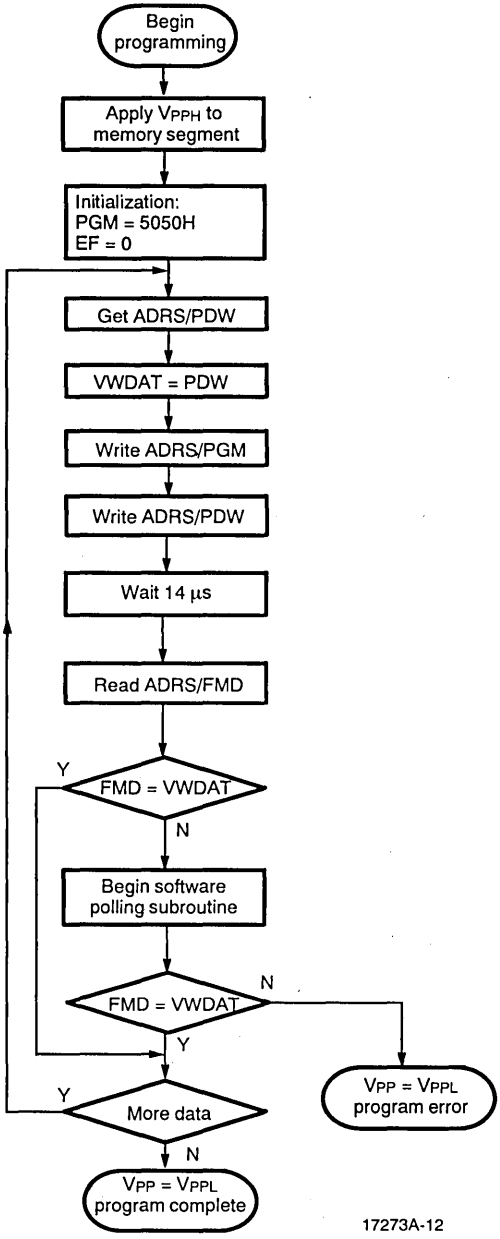


17273A-14

The Embedded Algorithm operations completely automate the parallel programming and erase procedures by internally executing the algorithmic command sequences of AMD's Flashrite and Flasherase algorithms. The devices automatically provide Write Operation Status information with standard read operations.

Figure 10.

EMBEDDED ALGORITHM WORD-WIDE PROGRAMMING FLOW CHART



Activity

Initialize Programming Variables:
PGM = Embedded Set up Command
EF = Error Flag

ADRS = Appropriate address for memory segment.
PDW = Program Data Word
VWDAT = Valid Word Data
EF = Error Flag
EF = 0 = No failure
EF = 1 = Low byte program error
EF = 2 = High byte program error
EF = 3 = Word-wide program error

FMD = Valid Word Data

Figure 11.

EMBEDDED ALGORITHM WORD-WIDE SOFTWARE POLLING PROGRAM SUBROUTINE

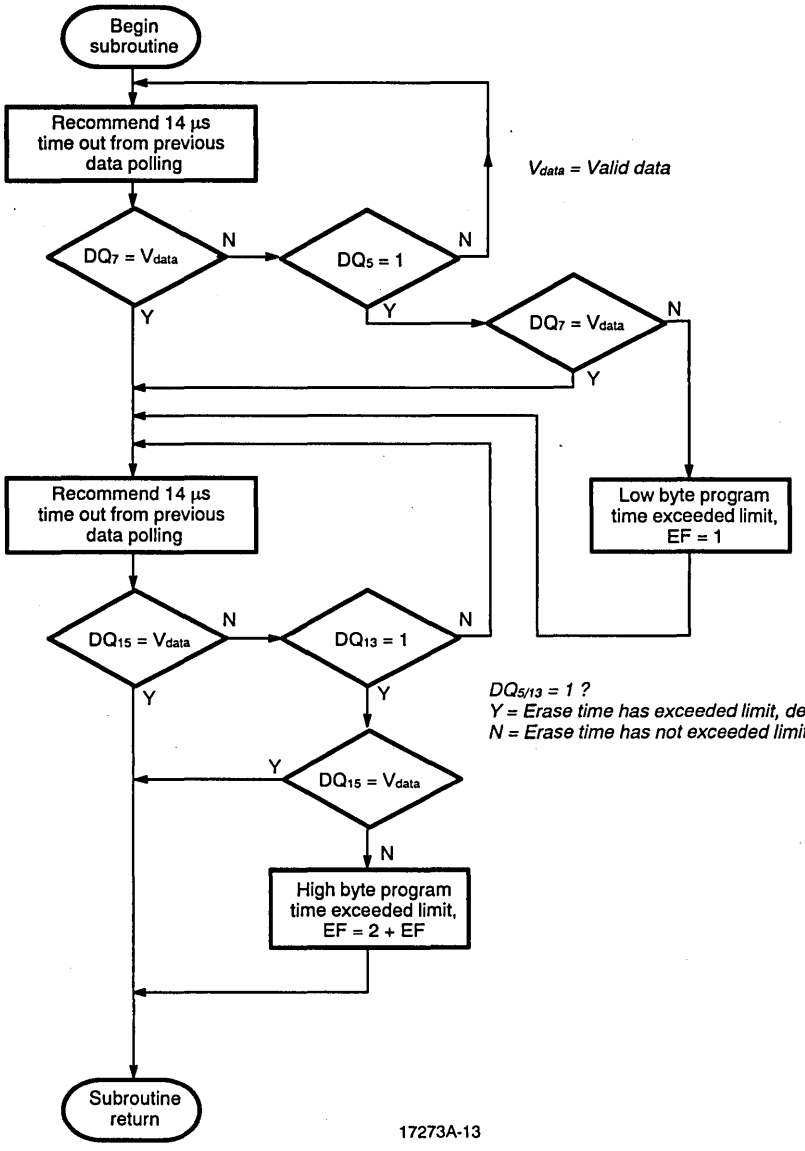
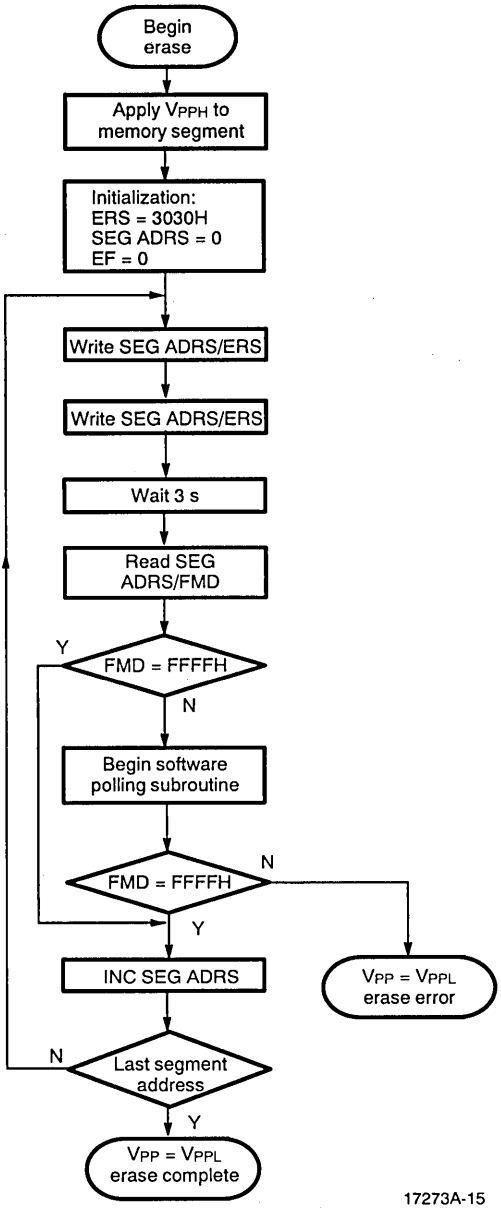


Figure 12.

EMBEDDED ALGORITHM WORD-WIDE ERASURE FLOW CHART



Activity
ERS = Erase Command *SEG ADRS = Segment Address*
EF = Error Flag *EF = 0 = No failure* *EF = 1 = Low byte Erase error* *EF = 2 = High byte Erase error* *EF = 3 = Word-wide Erase error*
FMD = Flash Memory Data

17273A-15

Figure 13.

EMBEDDED ALGORITHM WORD-WIDE SOFTWARE POLLING ERASE SUBROUTINE

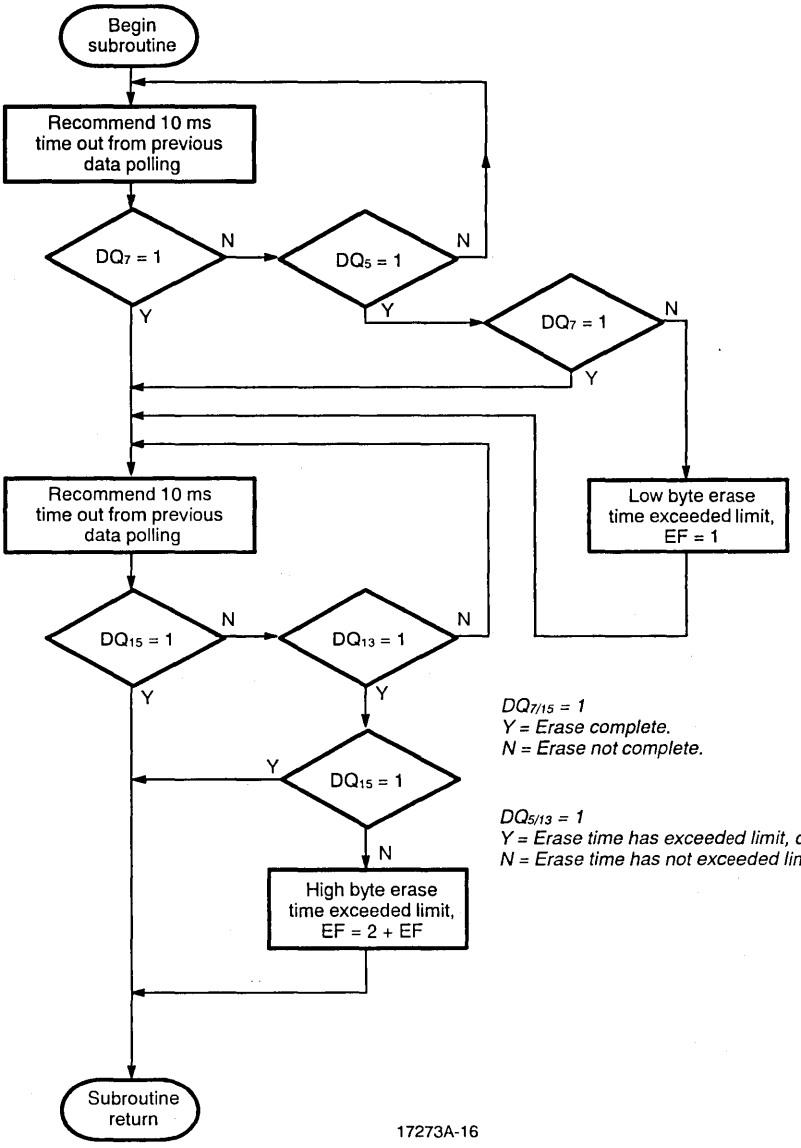


Figure 14.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −30°C to +70°C

Ambient Temperature
with Power Applied ..... −10°C to +70°C

Voltage with Respect To Ground
All pins except V_{PP} (Note 1) ..... −2.0 V to +7.0 V

V_{CC} (Note 1) ..... −2.0 V to +7.0 V

V_{PP} (Note 2) ..... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on V_{PP} pins is −0.5 V. During voltage transitions, V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = V_{CC} max. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +60°C

V_{CC} Supply Voltages ..... +4.75 V to 5.25 V

V_{PP} Supply Voltages

Read Only ..... 0 V to +6.5 V

Program, Erase, Verify,
and Read ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Byte Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.2 V		0.4	0.8	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		25	50	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		3.0	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		5.0	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			10	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.2	0.4	mA
		$V_{PP} \leq V_{CC}$			0.04	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		8.0	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. One Flash device active, seven in standby.
2. Only one Vpp is active.

DC CHARACTERISTICS

Word-Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±20	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	20	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. CE = V_{CC} ±0.2 V		0.4	0.8	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., CE = V_{IL}, OE = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		40	80	mA
I_{CC2}	V_{CC} Programming Current	CE = V_{IL} Programming in Progress		6	60	mA
I_{CC3}	V_{CC} Erase Current	CE = V_{IL} Erasure in Progress		10	60	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			10	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.4	0.8	mA
		$V_{PP} \leq V_{CC}$			0.08	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		16	60	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		20	60	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = 2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. Two Flash devices active, six in standby.
2. V_{pp1} and V_{pp2} are active.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Capacitance	V_{IN} = 0		21	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		21	pF
C_{IN2}	Control Capacitance	V_{IN} = 0 ($\overline{CE}$, $\overline{REG}$)		47	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = 0		21	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz.

SWITCHING AC CHARACTERISTICS

Read Only Operation (Note 1)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{RC}	Read Cycle Time	250		ns
t_{ELQV}	t_{CE}	Chip Enable Access Time		250	ns
t_{AVQV}	t_{ACC}	Address Access Time		250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time		150	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low-Z	5		ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High-Z		60	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low-Z	5		ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High-Z		60	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
t_{WHGL}		Write Recovery Time before Read	6		µs

Note:

1. Input Rise and Fall Times (10% to 90%): ≤ 10 ns, Input Pulse levels: V_{OL} and V_{OH}, Timing Measurement Reference Level – Inputs: V_{IL} and V_{IH} Outputs: V_{IL} and V_{IH}

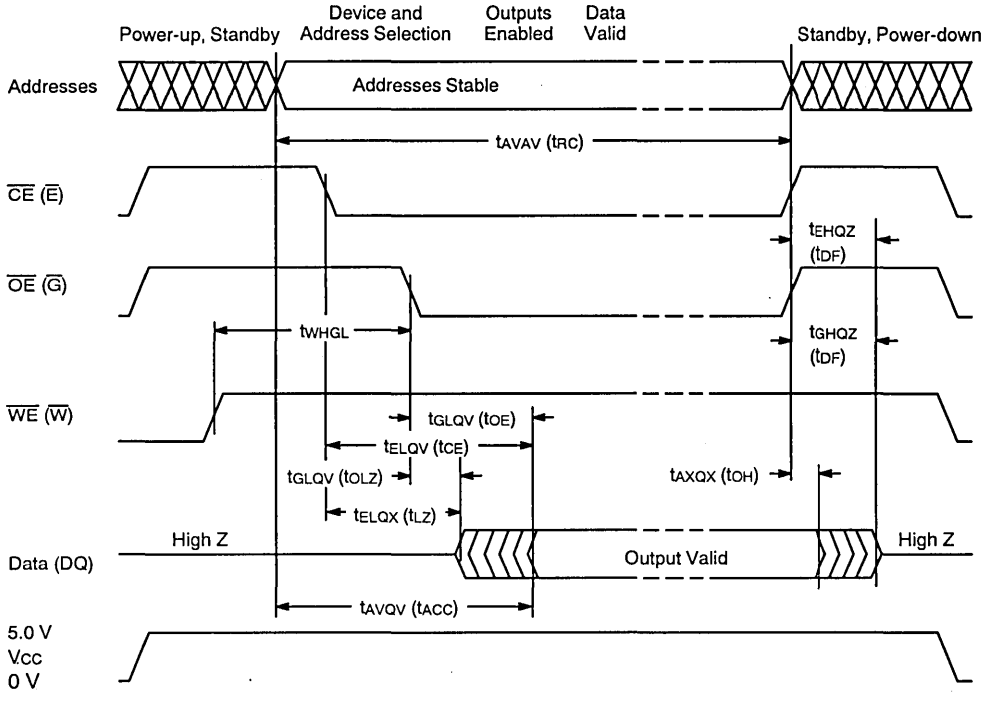
AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVWL}	t_{AS}	Address Set-Up Time	0		ns
t_{WLAX}	t_{AH}	Address Hold Time	100		ns
t_{DVWH}	t_{DS}	Data Set-Up Time	80		ns
t_{WHDX}	t_{DH}	Data Hold Time	30		ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm	30		ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHWL}		Read Recovery Time before Write	0		µs
t_{WLOZ}		Output in High-Z from Write Enable	5		ns
t_{WHOZ}		Output in Low-Z from Write Enable		60	ns
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	40		ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	100		ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	50		ns
t_{WHWH3}		Embedded Programming Operation (Notes 1, 2, 3)	14		µs
t_{WHWH4}		Embedded Erase Operation for each 256 KB Memory Segment (Notes 1, 2, 4)	5		s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	100		ns

Notes:

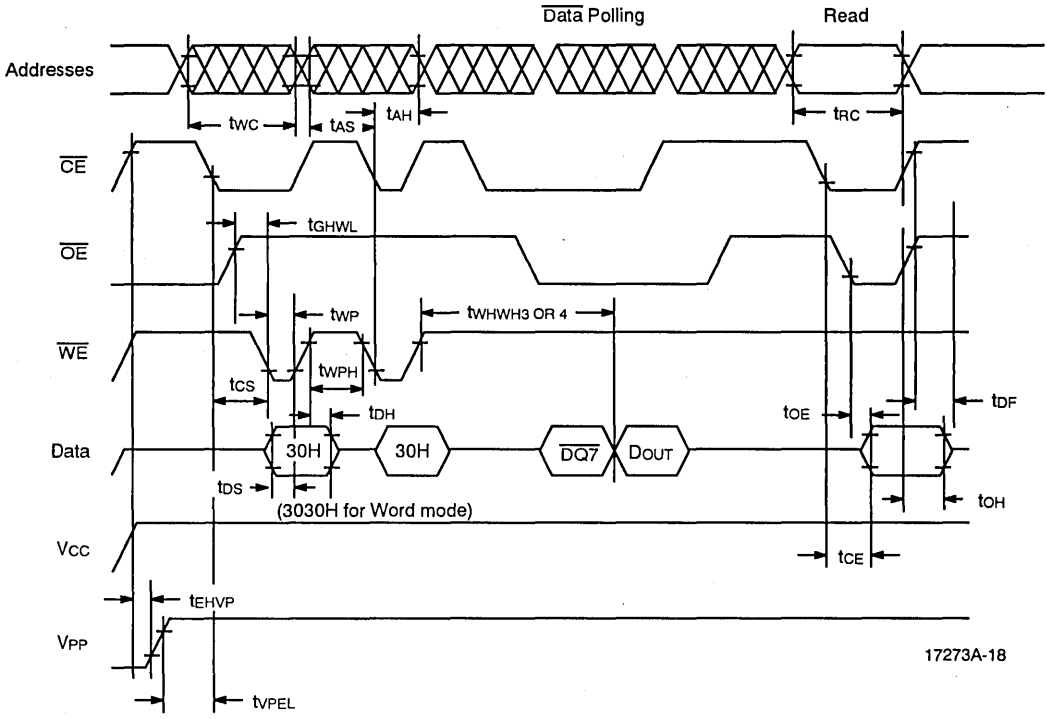
1. Rise/Fall < = 10 ns.
2. Maximum specification not needed due to the devices internal stop timer that will stop any erase or write operation that exceed the device specification.
3. Embedded Program Operation of 14 µs consist of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
4. Embedded Erase Operation of 5 seconds consists of 4 seconds memory segment pre-programming times and 1 second memory segment erase time for each 256K byte memory segment. This is typical time for embedded erase operation.



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

17273A-17

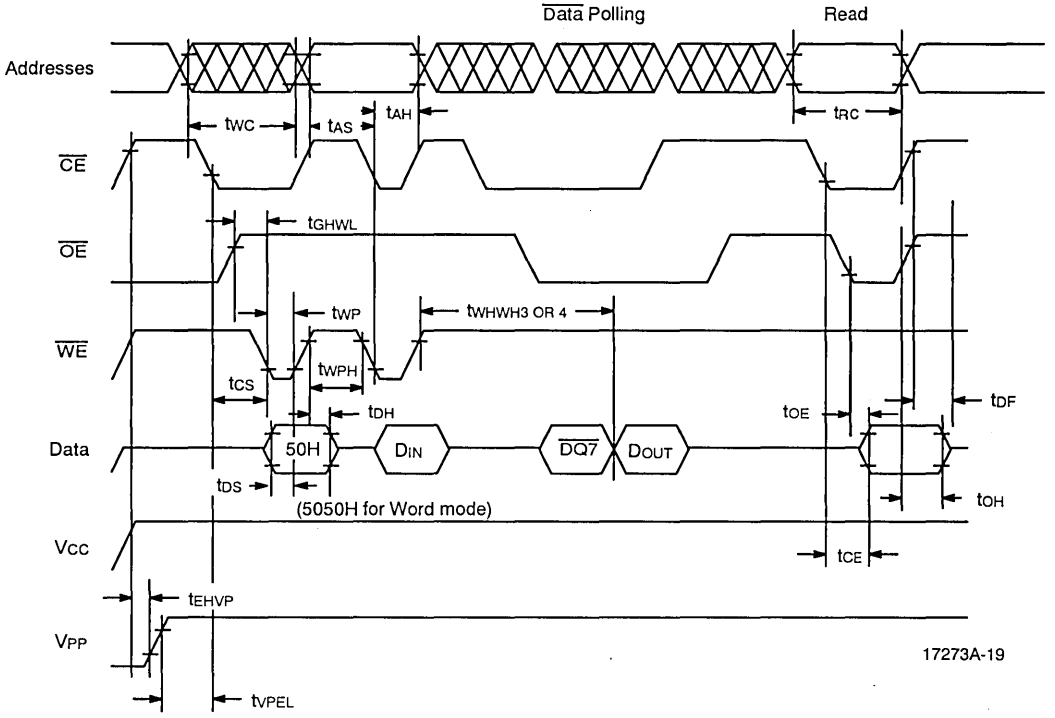
Figure 15. AC Waveforms for Read Operations



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 16. AC Waveforms for Embedded Erase Operation



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 17. AC Waveforms for Embedded Programming Operation

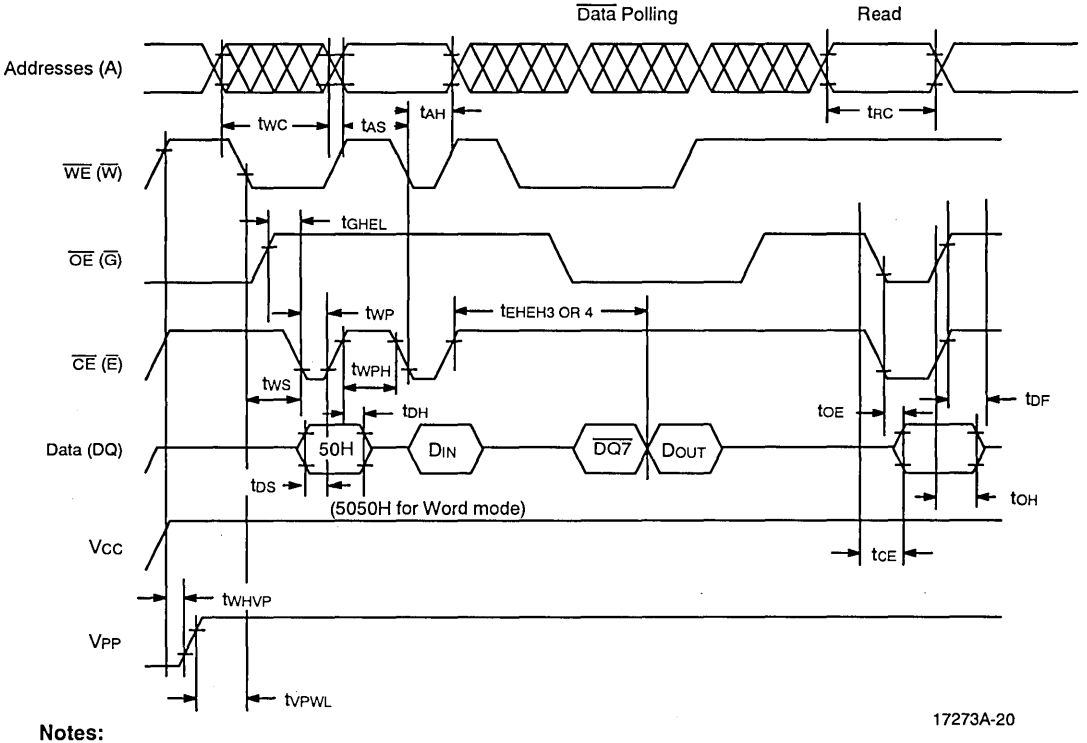
AC CHARACTERISTICS–ALTERNATE $\overline{CE}$ CONTROLLED WRITES

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVEL}	t_{AS}	Address Set-Up Time	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	100		ns
t_{DVEH}	t_{DS}	Data Set-Up Time	80		ns
t_{EHDX}	t_{DH}	Data Hold Time	30		ns
t_{GLDV}	t_{OE}	Output Enable Hold Time for Embedded Algorithm	10	150	ns
t_{GHEL}		Read Recovery Time before Write	0		µs
t_{WLEL}	t_{WS}	WE Set-Up Time before $\overline{CE}$	0		ns
t_{EHWH}	t_{CP}	WE Hold Time	0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	100		ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH (Note 3)	50		ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	14		µs
t_{EHEH4}		Embedded Erase Operation for each 256 KB Memory Segment (Notes 1, 2, 4)	5		s
t_{VPWL}		V_{PP} Set-Up Time to Write Enable LOW	100		ns

Notes:

1. Rise/Fall < =10 ns
2. Maximum specification not needed due to the internal stop timer that will stop any erase or write operation that exist the device specification.
3. Chip Enable Controlled Programming:
   Flash Programming is controlled by the valid combination of the Chip Enable ($\overline{CE}_{1,2}$) and Write Enable ($\overline{WE}$) signals. For system that uses the Chip Enable signal(s) to define the write pulse width, all Set-up, Hold, and inactive Write Enable timing should be measured relative to the Chip Enable signal(s).
4. Embedded Program Operation of 14 µs consist of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
5. Embedded Erase Operation of 5 seconds consists of 4 seconds memory segment pre-programming times and 1 second memory segment erase time for each 256K byte memory segment. This is typical time for embedded erase operation.



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 18. Alternate AC Waveforms for $\overline{CE}$ Controlled Embedded Programming or Erasing Operation

CARD INFORMATION STRUCTURE

The AmC001AFLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. All or part of the 512 byte could be used for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space. Part of the common memory space could also be mapped into the attribute memory space if more than 512 bytes of CIS are needed.

The EEPROM used in the AmC002AFLKA is a NEC μPD28C05GX-20-EJA designed to operate from a 5 V single power supply. The μPD28C05 provides a DATA polling function that provides the End of Write Cycle, Chip Erase and Auto Erase and Programming functions.

SYSTEM DESIGN AND INTERFACE INFORMATION

Power Up and Power Down Protection

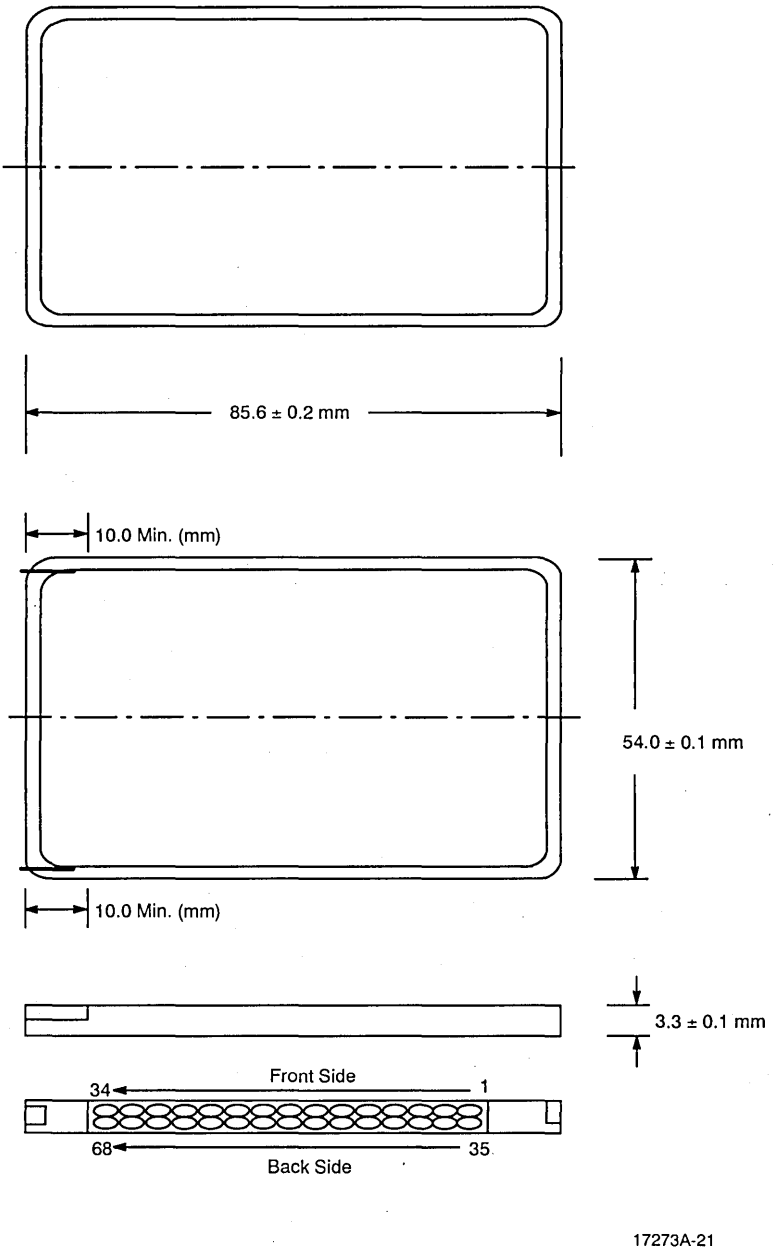
The PCMCIA standard socket provides for proper power up and power down sequencing via different pin lengths to ensure that hot insertion and removal of the PC card will not result in card damage or data loss.

AMD's Flash memory devices are designed to protect against accidental programming or erasure caused by spurious system signals that might exist during hot insertion, hot removal, or power transitions. The AMD PC card will power-up into a READ mode and the card will function as a read only memory as long as V_{pp} is less than V_{cc} +2 V. Erasing of the memory segments can be accomplished only by writing the proper Erase command to the card twice along with the proper Chip Enable, Output Enable and Write Enable control signals.

System Power Supply Decoupling

The AMD Flash memory card has a 0.1 μF decoupling capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins. It is recommended the system side also have a 4.7 μF capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins.

PHYSICAL DIMENSIONS
Type 1 PC Card



PRELIMINARY

AmC004AFLKA

4 Megabyte Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 250 ns maximum access time
- **CMOS low power consumption**
  - 25 mA typical active current (X8)
  - 400 μA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **High re-programmable endurance**
  - Minimum 100,000 erase/write cycles
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate Attribute Memory**
  - 512 byte EEPROM
- **Automated write and erase operations (increases system write performance)**
  - 256K byte memory segment
  - Typically <1.5 seconds per single memory segment erase
  - Random address writes to previously erased bytes (14 μs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Insertion and removal force**
  - State of art connector allows for minimum card insertion and removal effort
- **Write and erase voltage, 12.0 V ± 5%**
- **Read voltage, 5 V ± 5%**
- **Manufactured by DuPont Connector Systems**

GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC004AFLKA. This allows OEM manufacturers of portable system to eliminate the weight, extreme power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC004AFLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC004AFLKA enhances the productivity of mobile workers.

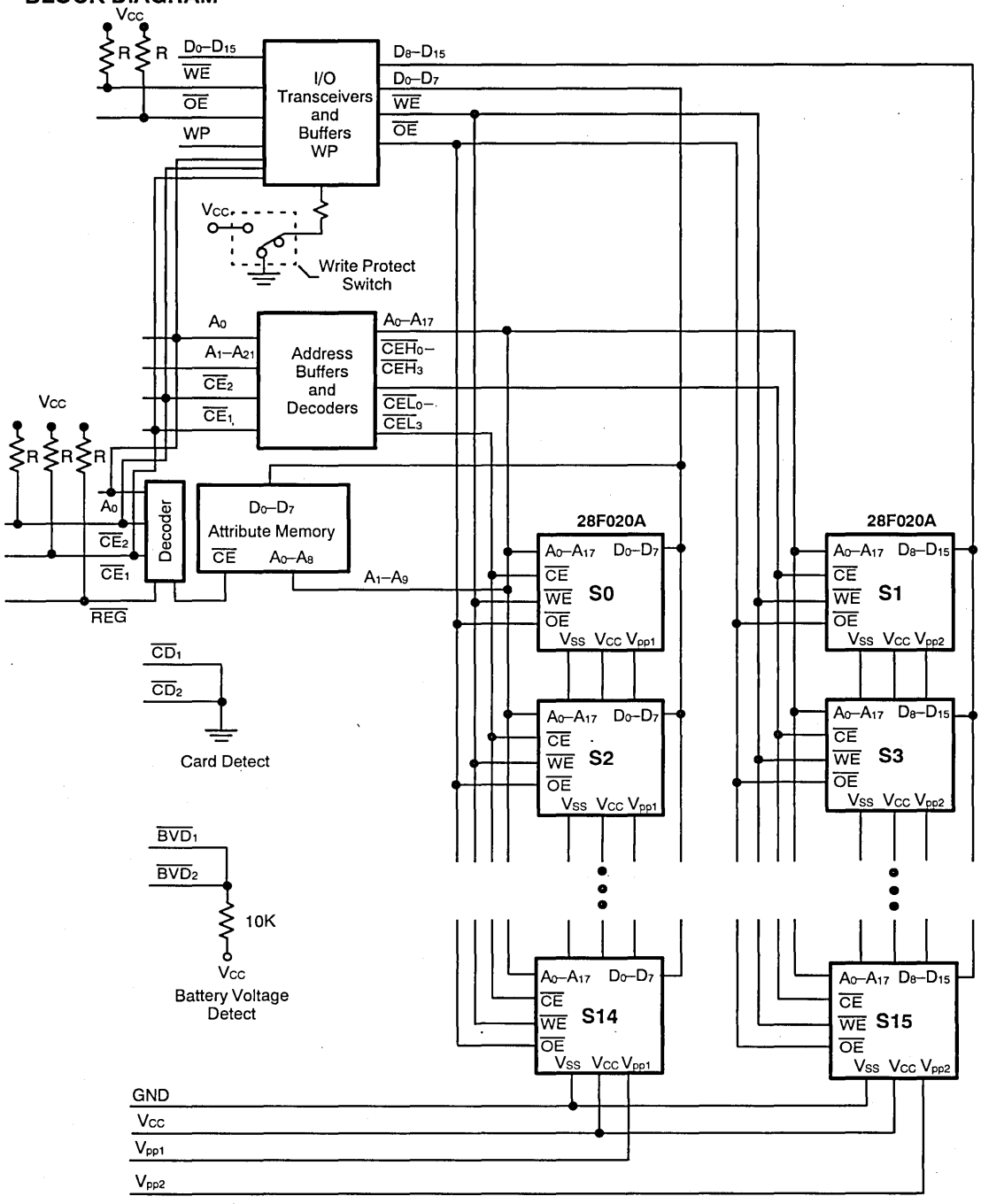
Widespread acceptance of the AmC004AFLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC004AFLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by DuPont Connector Systems

Publication# 17274 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



R=33K

17274A-1

PC CARD PIN ASSIGNMENTS

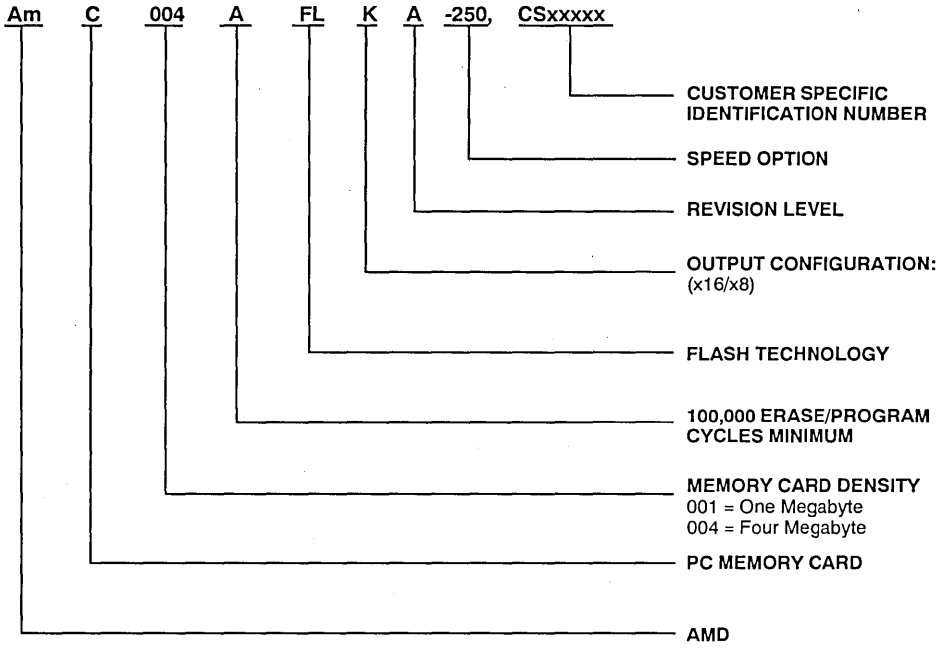
Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable (Note 1)	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2 (Note 1)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	RFU		Reserved
11	A_9	I	Address Bit 9	45	RFU		Reserved
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	A_{20}	I	Address Bit 20
16	NC		No Connect	50	A_{21}	I	Address Bit 21
17	V_{CC}		Power Supply	51	V_{CC}		Power Supply
18	V_{pp1}		Pgm Sply Vltg 1	52	V_{pp2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.
1. Signal must not be connected between cards
2. $\overline{BVD}$ = Internally pulled-up

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



PIN DESCRIPTION

Symbol	Type	Name and Function
A_0 - A_{21}	INPUT	**ADDRESS INPUTS** are internally latched during write cycles.
$D_0 - D_{15}$	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Data inputs are internally latched on write cycles. Data outputs during read cycles. Data pins are active high. When the memory card is de-selected or the outputs are disabled the outputs float to tri-state.
$\overline{CE}_1$, $\overline{CE}_2$	INPUT	**CARD ENABLE** is active low. The memory card is de-selected and power consumption is reduced to stand-by levels when $\overline{CE}$ is high. $\overline{CE}$ activates the internal memory card circuitry that controls the high and low byte control logic of the card, input buffers segment decoders, and associated memory devices.
$\overline{OE}$	INPUT	**OUTPUT ENABLE** is active low and enables the data buffers through the card outputs during read cycles.
$\overline{WE}$	INPUT	**WRITE ENABLE** is active low and controls the write function of the command register to the memory array. The target address is latched on the falling edge of the $\overline{WE}$ pulse and the appropriate data is latched on the rising edge of the pulse.
V_{PP1},V_{PP2}		**ERASE/WRITE POWER SUPPLY** for erase and programming. V_{pp} enables the command register which controls all functions required to alter the memory array contents. **Note:** The Memory Card functions in a read-only memory when $V_{PP} < V_{cc} + 2$ V.
V_{CC}		**PC CARD POWER SUPPLY** for device operation (5.0 V ± 5%)
GND		**GROUND**
CD_1, CD_2	OUTPUT	**CARD DETECT.** When card detect 1 and 2 = ground the system detects the card.
WP	OUTPUT	**WRITE PROTECT** is active high and disables all card write operations.
NC		**NO CONNECT** - corresponding pin is not connected internally to the die.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT.** Internally pulled-up.

MEMORY CARD OPERATIONS

The AmC004AFLKA Flash Memory Card is organized as an array of individual devices. Each device is 256K bytes in size. Although the address space is continuous each physical device defines a logical address segment size. Erase operations are performed in increments of this segment size. Multiple segments may be erased concurrently when additional V_{pp} current is supplied to the device. Once a memory segment is erased any address location may be programmed. Flash technology allows any logical "1" data bit to be programmed to a logical "0". The only way to reset bits to a logical "1" is to erase the entire memory segment of 256K bytes. High voltage is required on V_{pp1} and V_{pp2} to perform program and erase operations.

The common memory space data contents are altered in a similar manner as writing to individual Flash Memory devices. On-card address and data buffers activate the appropriate Flash device in the memory array. Each device internally latches address and data during write cycles. Refer to Table 2A.

Attribute memory is a separately accessed card memory space. The register memory space is active when the $\overline{REG}$ pin is driven low. The Card Information Structure describes the capabilities and specification of a card. The CIS is stored in the attribute memory space beginning at address 00000H. The AmC004AFLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. Alternatively, the CIS can be stored at the beginning of the common memory address space. D_0–D_7 are active during attribute memory accesses. D_8–D_{15} should be ignored. Odd order bytes present invalid data. Refer to Table 2B.

Word-Wide Operations

The AmC004AFLKA provides the flexibility to operate on data in a byte-wide or word-wide format. In word-wide operations the Low-bytes are controlled with V_{pp1} and $\overline{CE}_1$ when A0 = 0. The High-bytes are controlled with V_{pp2} and $\overline{CE}_2$, A0 = don't care.

Erase operations are the only operations that work on entire memory segment. All other operations such as word-wide programming are not affected by the physical memory segments.

Byte-Wide Operations

Byte-wide data is available on D_0–D_7 for read and write operations ($\overline{CE}_1$ = low, $\overline{CE}_2$ = high). Even and odd bytes are stored in separate memory segments (i.e. S_0 and S_1) and are accessed when A0 is low and high respectively. The even byte is the low order byte and the odd byte is the high order byte of a 16-bit word.

Erase operations in the byte-wide mode must account for data multiplexing on D_0–D_7 by changing the state of A0. Each memory segment pair must be addressed separately for erase operations.

Card Detection

Each $\overline{CD}$ (output) pin should be read by the host system to determine if the memory card is adequately seated in the socket. $\overline{CD}_1$ and $\overline{CD}_2$ are internally tied to ground. If both bits are not detected, the system should indicate that the card must be re-inserted.

Write Protection

The AMD Flash memory card has three types of write protection. The PCMCIA/JEIDA socket itself provides the first type of write protection. Power supply and control pins have specific pin lengths in order to protect the card with proper power supply sequencing in the case of hot insertion and removal.

A mechanical write protect switch provides a second type of write protection. When this switch is activated, $\overline{WE}$ is internally forced high. The Flash memory command register is disabled from accepting any write commands.

The third type of write protection is achieved with V_{pp1} and V_{pp2} at logic low levels to reset the Flash devices to read-only mode. Memory contents can not be changed in this state. The command register of individual Flash memory segments is only active when V_{pp1} and/or V_{pp2} are at high voltage (V_{ppH}).

Each Flash memory device that comprises a Flash memory segment will reset the command register to the read-only mode when V_{cc} is below VLKO. VLKO is the voltage below which write operations to individual command registers are disabled.

MEMORY CARD BUS OPERATIONS

Read Enable

Two Card Enable ($\overline{CE}$) pins are available on the memory card. Both $\overline{CE}$ pins must be active low for word-wide read accesses. Only one $\overline{CE}$ is required for byte-wide accesses. The $\overline{CE}$ pins control the selection and gates power to the high and low memory segments. The Output Enable ($\overline{OE}$) controls gating accessed data from the memory segment outputs.

Output Disable

Data outputs from the card are disabled when $\overline{OE}$ is at a logic-high level. Under this condition, outputs are in the high-impedance state.

Standby Operations

Byte-wide read accesses only require half of the read/write output buffer (x16) to be active. In addition, only one memory segment is active with in either the high order or low order bank. Activation of the appropriate half of the output buffer is controlled by the combination of both $\overline{CE}$ pins. The $\overline{CE}$ pins also control power to the high and low-order banks of memory. Outputs of the memory bank not selected are placed in the high impedance state. The individual memory segment is activated by the address decoders. The other memory segments operate in standby. An active memory segment continues to draw power until completion of a write, erase, or verify operation if the card is de-selected in the process of one of these operations.

Auto Select Operation

A host system or external card reader/writer can determine the on-card manufacturer and device I.D. codes. Codes are available after writing the 90H command to the command register of a memory segment. Reading from address location 00000H in any segment provides the manufacturer I.D. while address location 00002H provides the device I.D.

Write Operations

Write and erase operations are valid only when V_{pp1} and V_{pp2} are at high voltage. This activates the state machine of an addressed memory segment. The command register is a latch which saves address, commands, and data information used by the state machine and memory array.

When Write Enable ($\overline{WE}$) and appropriate $\overline{CE}$(s) are a logic-level low, the command register is enabled for write operations. The falling edge of $\overline{WE}$ latches address information and the rising edge latches data/command information.

Memory Segment Command Definitions

When the V_{pp} pin(s) are at low voltage the command register of each Flash memory segment defaults to 00H, the Read only mode.

With high voltage on the V_{pp} pin(s), the Flash memory segments are active for either read, write, or erase operations.

Write or erase operations are performed by writing appropriate data patterns to the command register of accessed Flash memory segments.

The byte-wide and word-wide commands are defined in Tables 3 and 4 respectively.

Table 2A. Common Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Note 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Note 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Note 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	High Z
Read (x16) (Note 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Data Out-Odd	Data Out-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data Out-Odd
Read (x8) (Notes 2, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Data Out-Odd	High Z
Read (x16) (Notes 2, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Data Out-Odd	Data Out-Even
Write (x8) (Notes 4, 7)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8)	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Data In-Odd
Write (x8) (Notes 4, 9)	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Data In	High Z
Write (x16) (Notes 5, 10)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Data In Odd	Data In-Even
Output Disable	V_{IH}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a byte write operation.
5. Refer to Table 4 for valid D_{IN} during a word write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. Byte access – Even. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Byte access – Odd. In this x8 mode, $A_0 = V_{IH}$ outputs or inputs the "odd" byte (high byte) of the x16 word on D_0–D_7. This is accomplished internal to the card by transposing D_8–D_{15} to D_0–D_7.
9. Odd byte only access. In this x8 mode, A_0 = X outputs or inputs the "odd" byte (high byte) of the x16 word on D_8–D_{15}.
10. x16 word accesses present both "even" (low) and "odd" (high) bytes. $A_0 = V_{IL}$ or V_{IH} = "Don't Care".

Table 2B. Attribute Memory Bus Operations

Pins/ Operation	$\overline{REG}$	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{OE}$	$\overline{WE}$	(1, 6) V_{PP2}	(1, 6) V_{PP1}	A0	D_8–D_{15}	D_0–D_7
READ-ONLY										
Read (x8) (Notes 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	V_{IH}	High Z	Not Valid
Read (x8) (Note 8)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	High Z
Read (x16) (Notes 8, 9, 10)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	X	Not Valid	Data Out-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IH}	V_{PPL}	V_{PPL}	X	High Z	High Z
Standby	X	V_{IH}	V_{IH}	X	X	V_{PPL}	V_{PPL}	X	High Z	High Z
READ/WRITE										
Read (x8) (Notes 2, 7, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data Out-Even
Read (x8) (Notes 2, 8, 9)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Read (x8) (Note 9)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Read (x16) (Notes 2, 9)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	V_{PPH}	X	Not Valid	Data Out-Even
Write (x8) (Notes 4, 7, 10)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{PPX}	V_{PPH}	V_{IL}	High Z	Data In-Even
Write (x8) (Notes 4, 8, 10)	V_{IL}	V_{IIH}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	V_{IH}	High Z	Not Valid
Write (x8) (Notes 4, 9, 10)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	V_{PPX}	X	Not Valid	High Z
Write (x16) (Note 10)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	Not Valid	Data In-Even
Output Disable	V_{IL}	X	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	X	High Z	High Z
Standby (Note 3)	X	V_{IH}	V_{IH}	X	X	V_{PPH}	V_{PPH}	X	High Z	High Z

Legend:

X = Don't Care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An, $V_{CC} + 2$ V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
4. Refer to Table 3 for valid D_{IN} during a write operation.
5. Refer to Table 4 for valid D_{IN} during a write operation.
6. $V_{PPX} = V_{PPH}$ or V_{PPL}.
7. In this x8 mode, $A_0 = V_{IL}$ outputs or inputs the "even" byte (low byte) of the x16 word on D_0–D_7.
8. Only even-byte data is valid during Attribute Memory Read function.
9. During Attribute Memory Read function, $\overline{REG}$ and $\overline{OE}$ must be active for the entire cycle.
10. During Attribute Memory Write function, $\overline{REG}$ and $\overline{WE}$ must be active for the entire cycle, $\overline{OE}$ must be inactive for the entire cycle.

Table 3. Command Definitions for Byte-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	90H	Read	00H/01H	01H/29H
Embedded Set-up/Erase Embedded Erase™ (Note 4)	Write	X	30H	Write	X	30H
Embedded Set-up Program/ Embedded Program™ (Note 5)	Write	X	50H	Write	PA	PD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Embedded Erase Algorithm.
5. Figure 2 illustrates the Embedded Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.
   Address: 00H/01H = MFG code / Device code addresses.
   Data: 01H/29H = MFG code data / Device code data.

Table 4. Command Definitions for Word-Wide Operations

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	0000H/ FFFFH	Read	RA	RD
Read Auto Select (Note 7)	Write	X	9090H	Read	0000H/ 0101H	0101H/ 2929H
Embedded Erase Set-up/Erase	Write	SA	3030H	Write	X	3030H
Embedded Set-up Program/ Embedded Program	Write	X	5050H	Write	PA	PD
Reset (Note 6)	Write	X	FFFFH	Write	X	FFFFH

Notes:

1. Bus operations are defined in Table 2A.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   SA = Address of memory segment to be erased.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Embedded Electrical Erase Algorithm.
5. Figure 2 illustrates the Embedded Programming Algorithm.
6. Please reference Reset Command section.
7. Please reference Auto Select section.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

Details of AMD's Embedded Program and Erase Operations

Embedded Erase™ Algorithm

The automatic memory segment erase does not require the device to be entirely pre-programmed prior to executing the Embedded erase set-up command and Embedded erase command. Upon executing the Embedded erase command, the addressed memory segment automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

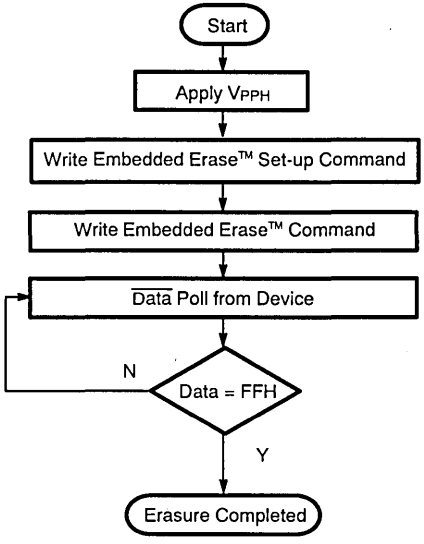
When the memory segment is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 of the memory segment is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded erase set-up command is a command only operation that stages the memory segment for automatic electrical erasure of all bytes in the array. Embedded erase set-up is performed by writing 30H to the command register of the addressed memory segment.

To commence automatic segment erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 of the memory segment is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 1 and Table 5 illustrate the Embedded Erase algorithm, a typical command string and bus operations.



17274A-2

Figure 1. Embedded Erase™ Algorithm in Byte-Wide Mode

Table 5. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation.

Embedded Program™ Algorithm

The Embedded Program Set-up is a command only operation that stages the addressed memory segment for automatic programming. Embedded Program Set-up is performed by writing 50H to the command register.

Once the Embedded Program Set-up operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 of the addressed memory segment is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode (no program verify command is required).

Figure 2 and Table 6 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

Reset Command

The reset command initializes the memory segment to the read mode. In addition, it also provides a safe method to abort any memory segment operation (including program or erase). The reset command must be written two consecutive times after the program set-up command. This will safely reset the segment memory to the read mode. Memory contents are not altered. Following any other command, write the reset command once to the segment. This will safely abort any operation and reset the device to the Read mode.

Table 6. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-up Command	Data = 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{Data}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation. Device is either powered-down, erase inhibit or program inhibit.

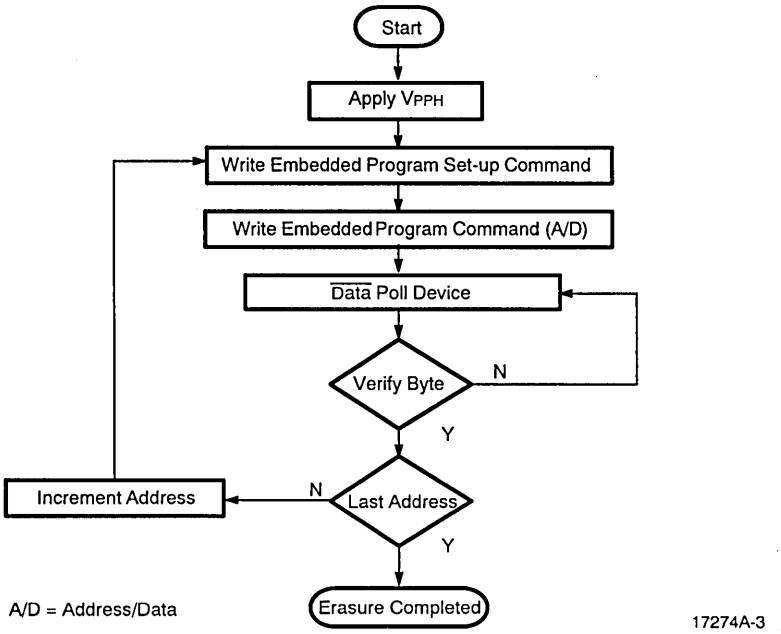


Figure 2. Embedded Programming Algorithm in Byte-Wide Mode

Write Operation Status

Data Polling—DQ7

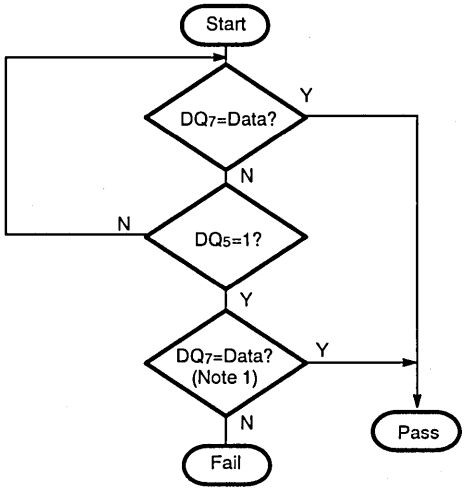
The Flash Memory PC Card features Data Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device will produce the compliment of expected Valid data on DQ7 of the addressed memory segment. Upon completion of the Embedded Program algorithm an attempt to read the device will produce Valid data on DQ7. The Data Polling feature is valid after the rising edge of the second WE pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The Data Polling feature is valid after the rising edge of the second WE pulse of the two Write pulse sequence.

The Data Polling feature is only active during Embedded Programming or erase algorithms.

See Figures 3a and 4a for the Data Polling timing specifications and diagrams.



Note:

1. DQ_7 is rechecked even if DQ_5 = 1 because DQ_7 may change simultaneously with DQ_5.

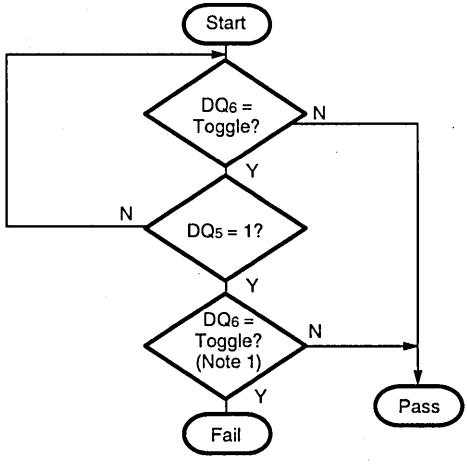
Figure 3a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Flash Memory PC Card also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the first $\overline{\text{WE}}$ pulse of the two write pulse sequence, unlike $\overline{\text{Data}}$ Polling which is valid after the rising edge of the second $\overline{\text{WE}}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

See Figures 3b and 4a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.



Note:

1. DQ_6 is rechecked even if DQ_5 = 1 because DQ_6 may stop toggling at the same time as DQ_5 changing to "1".

Figure 3b. Toggle Bit Algorithm

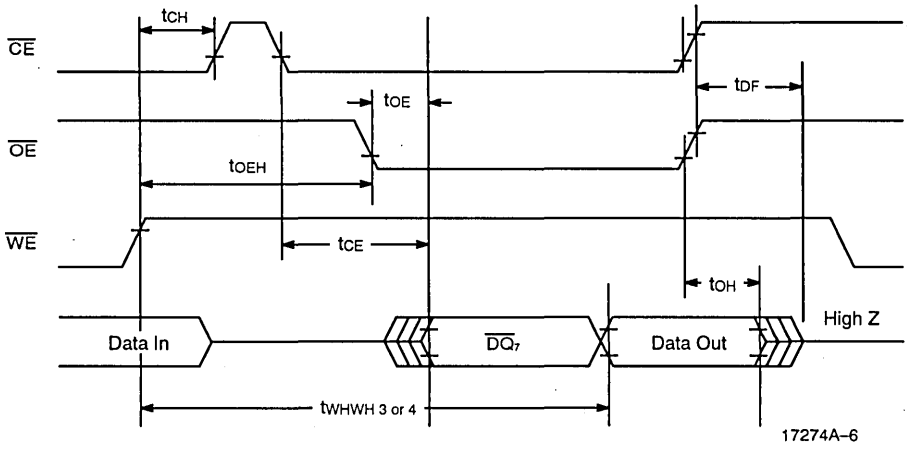
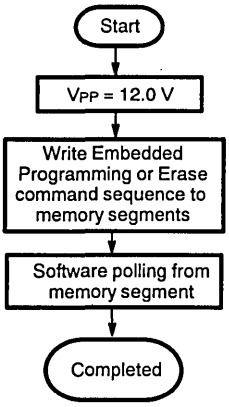


Figure 4a. AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations

EMBEDDED ALGORITHM BYTE-WIDE PROGRAMMING AND ERASURE OVERVIEW

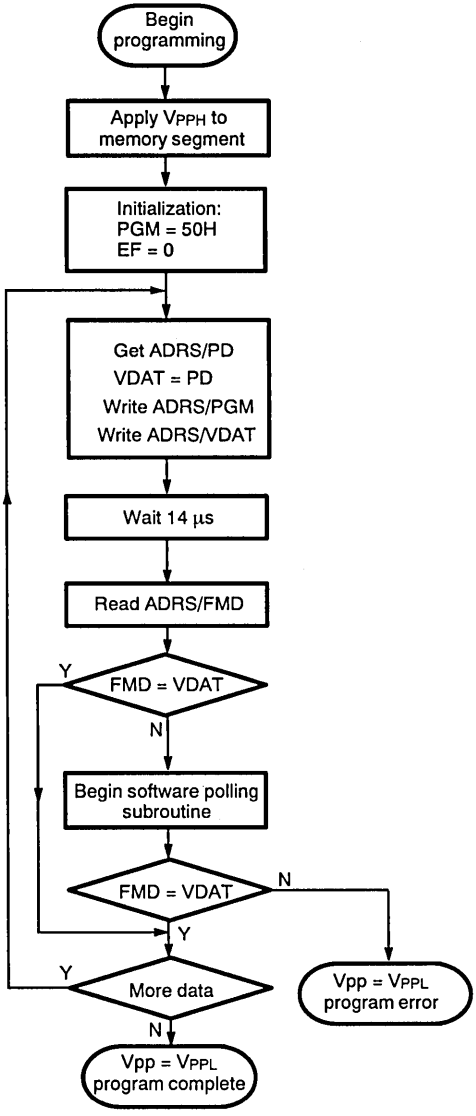


17274A-9

The Embedded Algorithm operations completely automate the programming and erase procedure by internally executing the algorithmic command sequence of original AMD devices. The devices automatically provide Write Operation Status information with standard read operations (addresses are a don't care).

Figure 5.

EMBEDDED ALGORITHM BYTE-WIDE PROGRAMMING FLOW CHART



Activity

Initialize Programming Variables:
PGM = Embedded Set up Command
EF = Error Flag

ADRS = Appropriate address for memory segment.
PD = Program Data
VDAT = Valid Data.

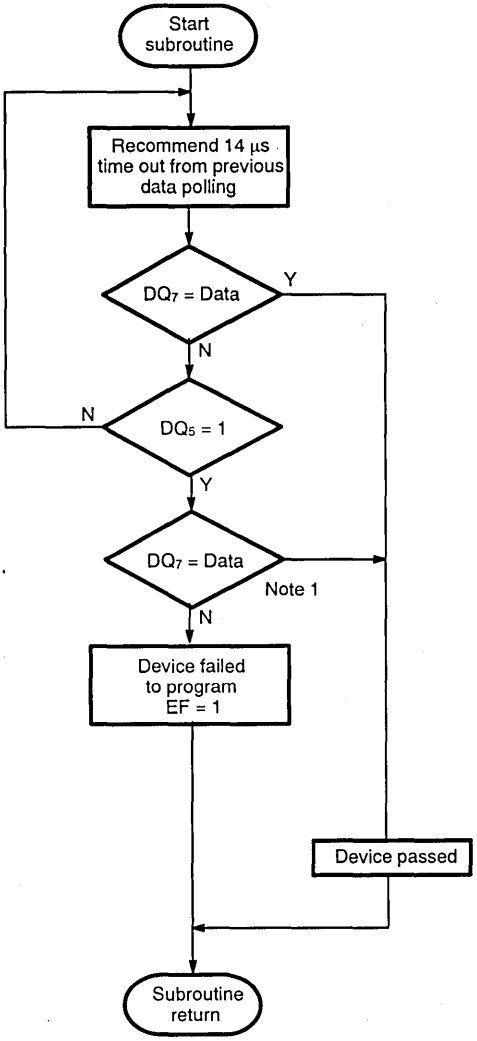
FMD = Flash Memory Data.

EF = 0 = No Programming error
EF = 1 = Programming error

17274A–7

Figure 6.

EMBEDDED ALGORITHM BYTE-WIDE SOFTWARE POLLING FOR PROGRAMMING
Subroutine



DQ5 = 1
N = Program time not exceeded limit
Y = Program time exceed limit, device failed

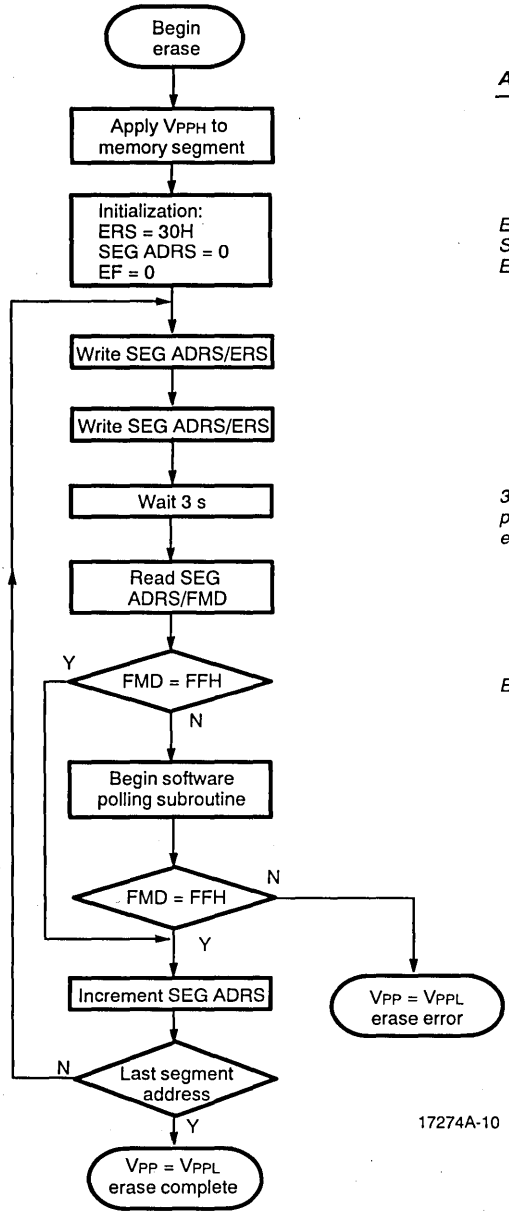
17274A-8

Note:

1. DQ_7 is checked even if $DQ_5 = 1$ because DQ_7 may have changed simultaneously with DQ_5 or immediately after DQ_5.

Figure 7.

EMBEDDED ALGORITHM BYTE-WIDE ERASURE FLOW CHART



Activity

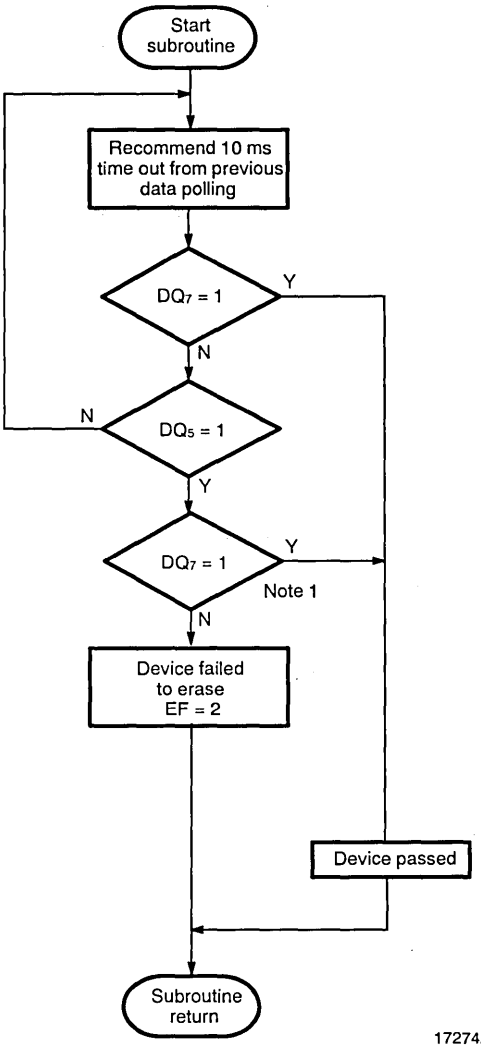
ERS = Erase Command
SEGment ADdReSs = 0
Error Flag = 0

3 seconds wait = 2 seconds memory segment preprogram time +1 second memory segment erase time.

Erased Flash Memory Data = FFH.

Figure 8.

EMBEDDED ALGORITHM BYTE-WIDE SOFTWARE POLLING ERASE SUBROUTINE



$DQ_7 = 1$
Y = Erase Complete
N = Erase not Complete

$DQ_5 = 1$
Y = Erase time exceeded limit, Device failed.
N = Erase time has not exceeded limit.

Figure 9.

WORD-WIDE PROGRAMMING AND ERASING

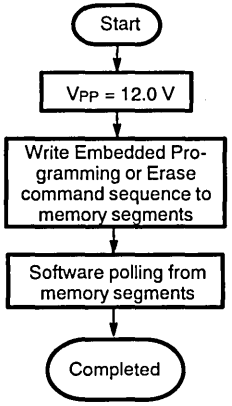
Word-Wide Programming

The word-wide programming sequence will be as usual. The program word command is 5050H. Each byte is independently programmed. For example, if the high byte of the word indicates the successful completion of programming via one of its program status bits such as DQ7, software polling should continue to monitor the low byte for program completion and data verification. During the Embedded Programming operations the device executes programming pulses in 14 μs increments. Status reads provide information on the progress of the byte programming relative to the last complete program pulse. Status information is automatically updated upon completion of each internal program pulse. Status information does not change within the 14 μs program pulse width.

Word-Wide Erasing

The word-wide erasing is similar to word-wide programming. The erase word command is 3030H. Each byte is independently erased and verified. Word-wide erasure reduces total erase time when compared to byte erasure. Each Flash memory device in the card may erase at different rates. Therefore each device (byte) must be verified separately. The alternate method mentioned above also apply to erasure. Since the same 40 MHz system, 1 second of CPU time is equivalent to 40 million clock cycles.

EMBEDDED ALGORITHM WORD-WIDE PROGRAMMING AND ERASURE OVERVIEW

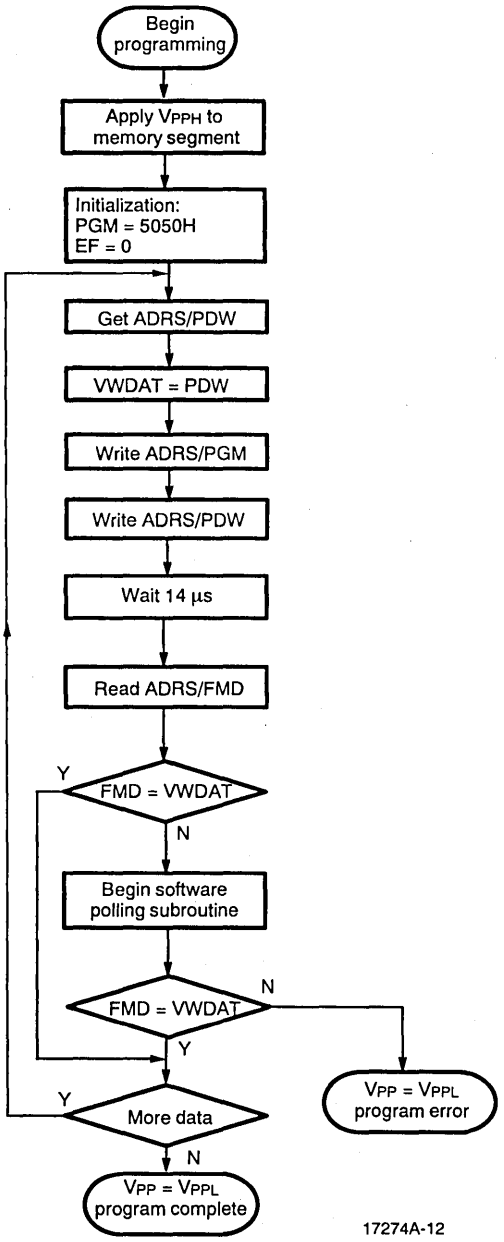


17274A-14

The Embedded Algorithm operations completely automate the parallel programming and erase procedures by internally executing the algorithmic command sequences of AMD's Flashrite and Flasherase algorithms. The devices automatically provide Write Operation Status information with standard read operations.

Figure 10.

EMBEDDED ALGORITHM WORD-WIDE PROGRAMMING FLOW CHART



Activity

Initialize Programming Variables:
PGM = Embedded Set up Command
EF = Error Flag

ADRS = Appropriate address for memory segment.
PDW = Program Data Word
VWDAT = Valid Word Data
EF = Error Flag
EF = 0 = No failure
EF = 1 = Low byte program error
EF = 2 = High byte program error
EF = 3 = Word-wide program error

FMD = Valid Word Data

Figure 11.

EMBEDDED ALGORITHM WORD-WIDE SOFTWARE POLLING PROGRAM SUBROUTINE

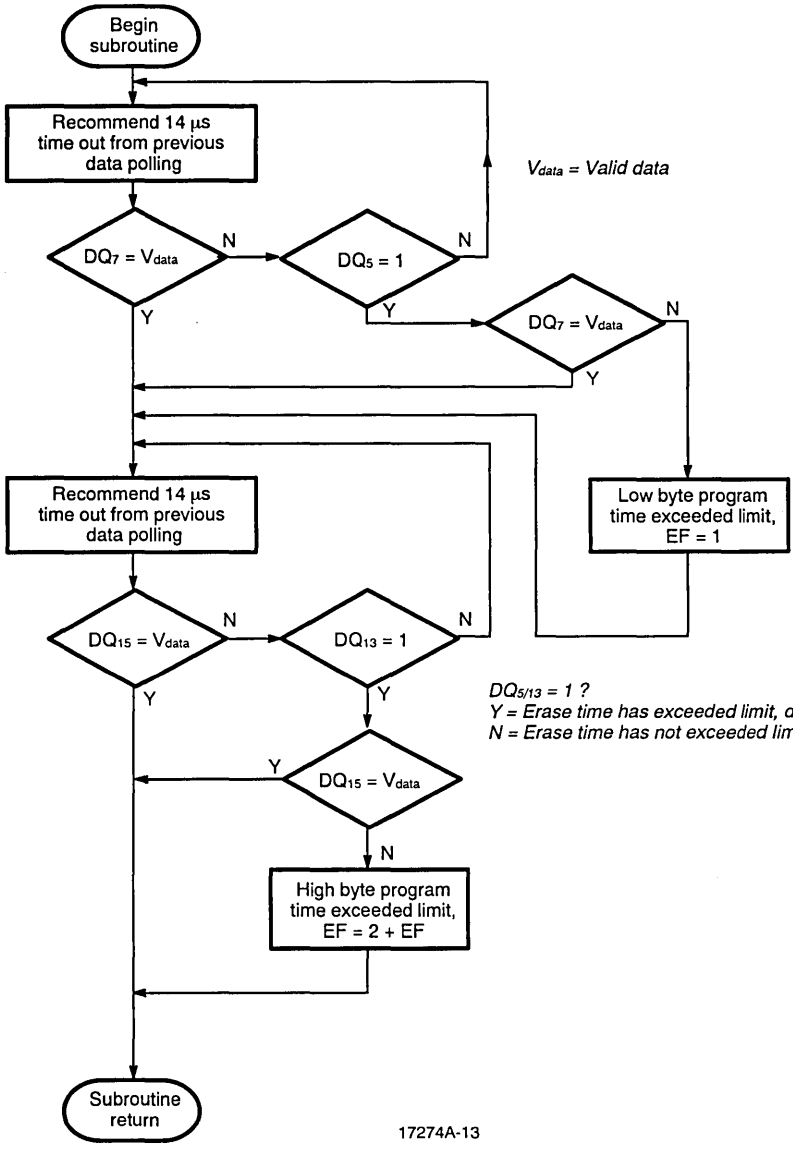
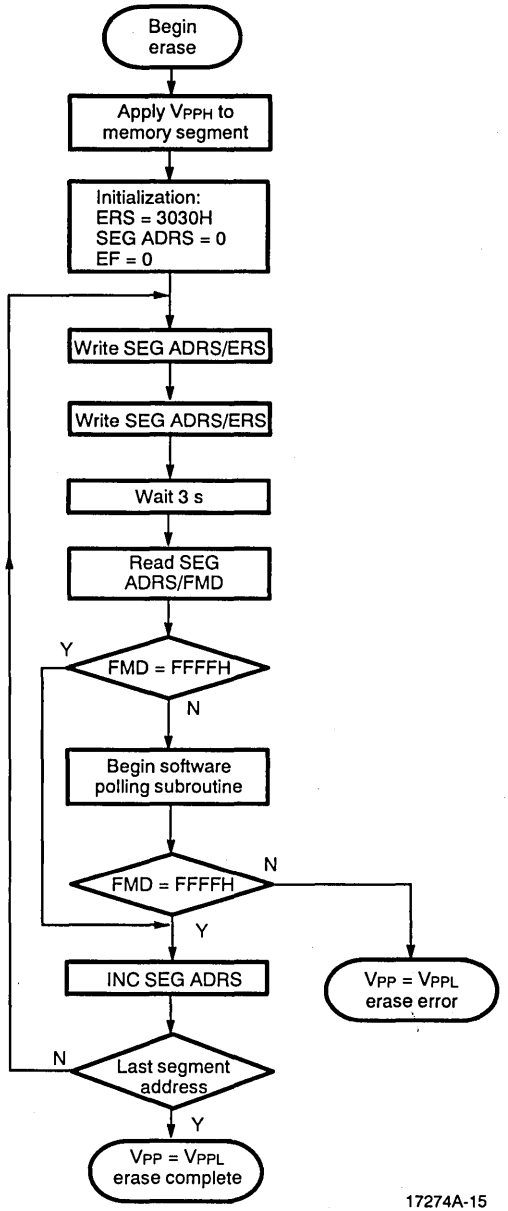


Figure 12.

EMBEDDED ALGORITHM WORD-WIDE ERASURE FLOW CHART



17274A-15

Activity

ERS = Erase Command
SEG ADRS = Segment Address

EF = Error Flag
EF = 0 = No failure
EF = 1 = Low byte Erase error
EF = 2 = High byte Erase error
EF = 3 = Word-wide Erase error

FMD = Flash Memory Data

Figure 13.

EMBEDDED ALGORITHM WORD-WIDE SOFTWARE POLLING ERASE SUBROUTINE

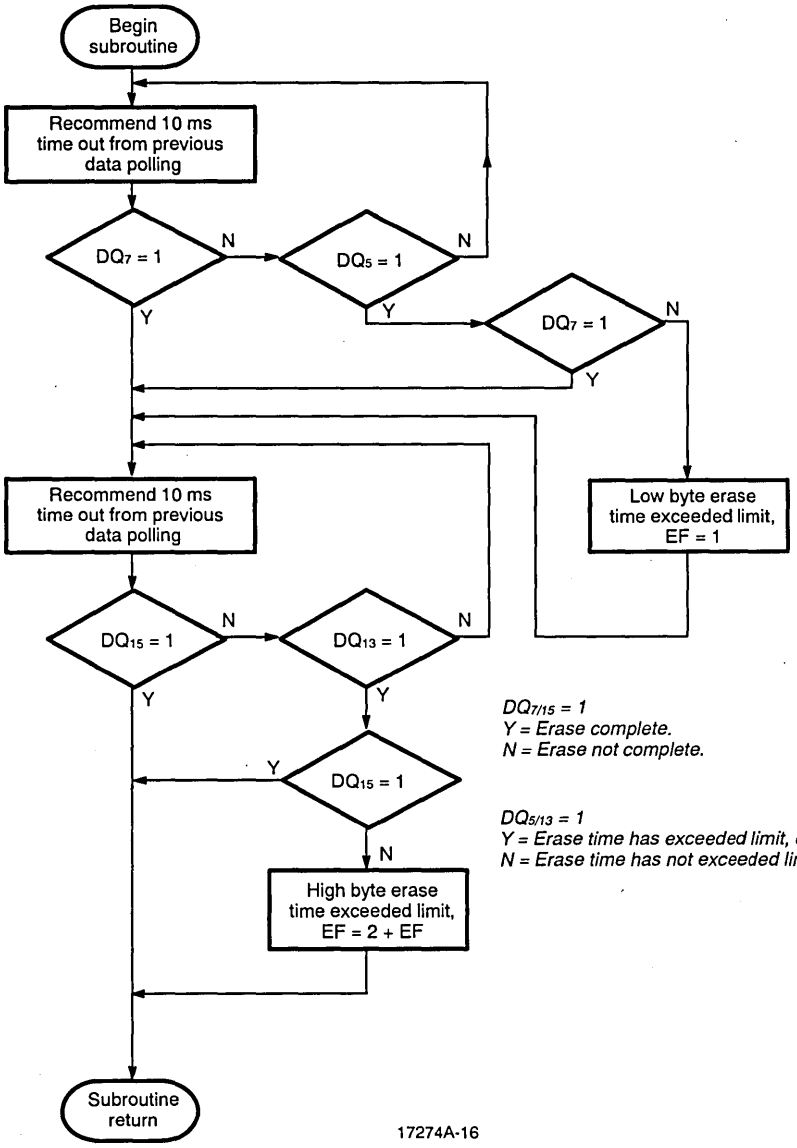


Figure 14.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... – 30°C to +70°C

Ambient Temperature
with Power Applied ..... – 10°C to +70°C

Voltage with Respect To Ground
All pins except V_{PP} (Note 1) ..... – 2.0 V to +7.0 V

V_{CC} (Note 1) ..... – 2.0 V to +7.0 V

V_{PP} (Note 2) ..... – 2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. Minimum DC input voltage on V_{PP} pins is –0.5 V. During voltage transitions, V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = V_{CC} max. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +60°C

V_{CC} Supply Voltages ..... +4.75 V to 5.25 V

V_{PP} Supply Voltages

Read Only ..... 0 V to +6.5 V

Program, Erase, Verify,
and Read ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Byte Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±28	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	28	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. CE = V_{CC} ± 0.2 V		0.4	1.6	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., CE = V_{IL}, OE = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		25	50	mA
I_{CC2}	V_{CC} Programming Current	CE = V_{IL} Programming in Progress		3.0	30	mA
I_{CC3}	V_{CC} Erase Current	CE = V_{IL} Erasure in Progress		5.0	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			16	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.2	0.4	mA
		$V_{PP} \leq V_{CC}$			0.04	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		8.0	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. One Flash device active, seven in standby.
2. Only one Vpp is active.

DC CHARACTERISTICS

Word-Wide Operation

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		1.0	±28	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		1.0	28	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.2 V		0.4	1.6	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, I_{OUT} = 0 mA, at 6 MHz		40	80	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		6	60	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		10	60	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} \leq V_{CC}$			16	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} > V_{CC}$		0.4	0.8	mA
		$V_{PP} \leq V_{CC}$			0.08	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPL} Programming in Progress		16	60	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		20	60	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage	Except $\overline{CE}$, $\overline{REG}$ = 3.2 V Min.	2.4		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA V_{CC} = V_{CC} Min.			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = 2.0 mA V_{CC} = V_{CC} Min.	3.8			V
V_{PPL}	V_{PP} During Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0		V_{CC}+2	V
V_{PPH}	V_{PP} During Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2			V

Notes:
1. Two Flash devices active, six in standby.
2. V_{pp1} and V_{pp2} are active.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Capacitance	V_{IN} = 0		21	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		21	pF
C_{IN2}	Control Capacitance	V_{IN} = 0 ($\overline{CE}$, $\overline{REG}$)		47	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = 0		21	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz.

SWITCHING AC CHARACTERISTICS

Read Only Operation (Note 1)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	250		ns
t_{ELQV}	t_{CE}	Chip Enable Access Time		250	ns
t_{AVQV}	t_{ACC}	Address Access Time		250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time		150	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low-Z	5		ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High-Z		60	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low-Z	5		ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High-Z		60	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	5		ns
t_{WHGL}		Write Recovery Time before Read	6		µs

Note:

1. Input Rise and Fall Times (10% to 90%): ≤ 10 ns, Input Pulse levels: V_{OL} and V_{OH}, Timing Measurement Reference Level – Inputs: V_{IL} and V_{IH} Outputs: V_{IL} and V_{IH}

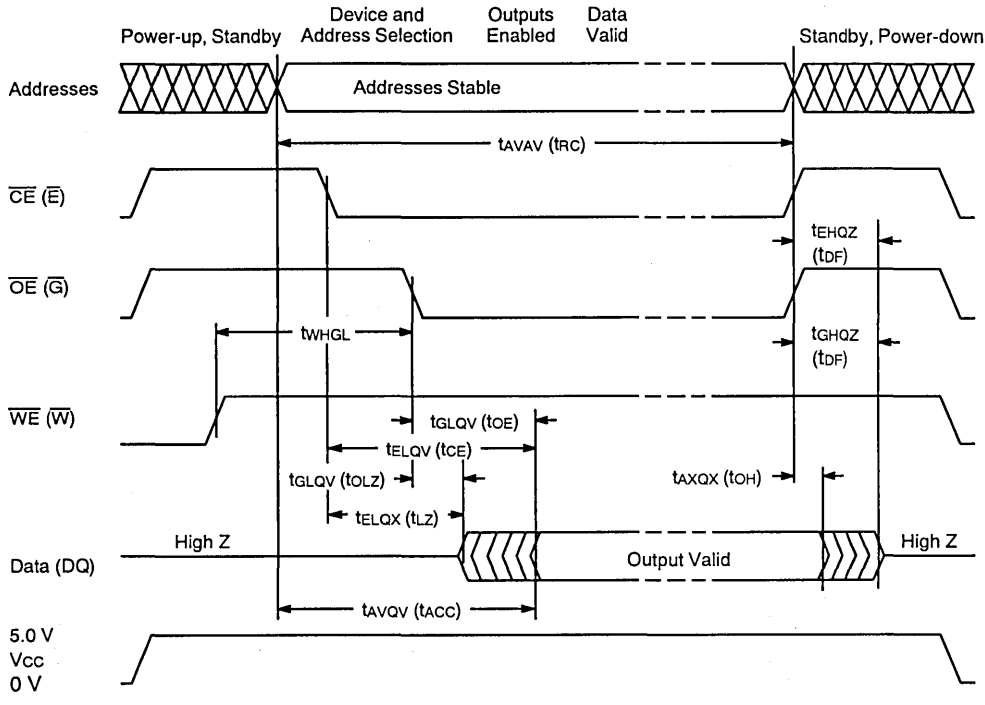
AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVWL}	t_{AS}	Address Set-Up Time	0		ns
t_{WLAX}	t_{AH}	Address Hold Time	100		ns
t_{DVWH}	t_{DS}	Data Set-Up Time	80		ns
t_{WHDX}	t_{DH}	Data Hold Time	30		ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm	30		ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	6		µs
t_{GHWL}		Read Recovery Time before Write	0		µs
t_{WLOZ}		Output in High-Z from Write Enable	5		ns
t_{WHOZ}		Output in Low-Z from Write Enable		60	ns
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	40		ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	100		ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	50		ns
t_{WHWH3}		Embedded Programming Operation (Notes 1, 2, 3)	14		µs
t_{WHWH4}		Embedded Erase Operation for each 256 KB Memory Segment (Notes 1, 2, 4)	5		s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	100		ns

Notes:

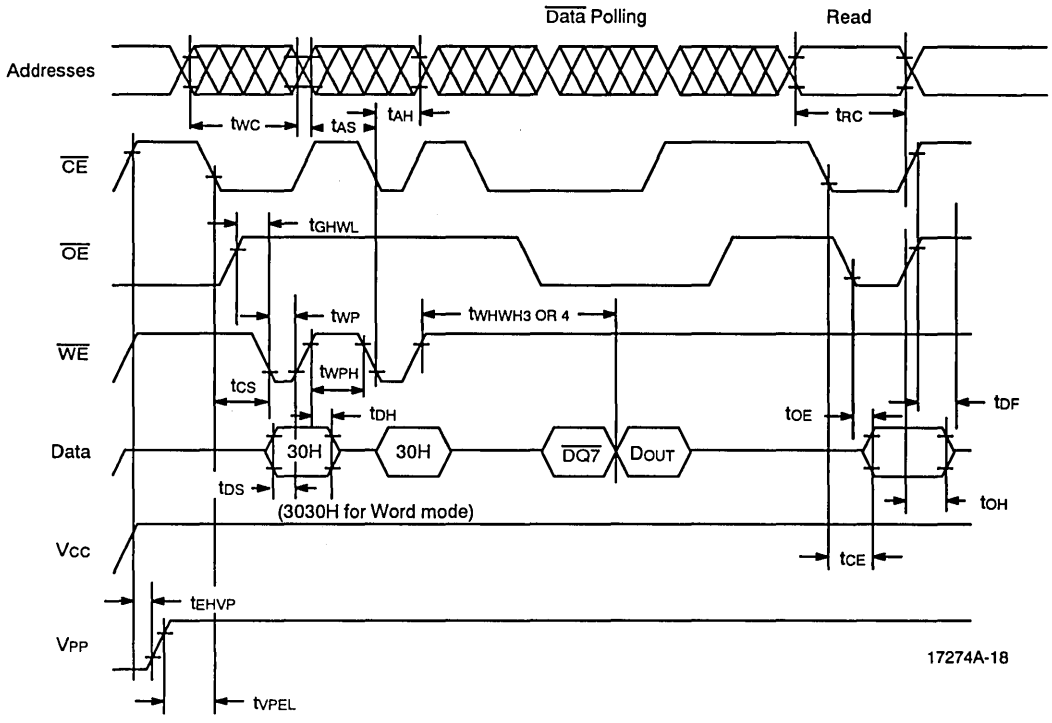
1. Rise/Fall < = 10 ns.
2. Maximum specification not needed due to the devices internal stop timer that will stop any erase or write operation that exceed the device specification.
3. Embedded Program Operation of 14 µs consist of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
4. Embedded Erase Operation of 5 seconds consists of 4 seconds memory segment pre-programming times and 1 second memory segment erase time for each 256K byte memory segment. This is typical time for embedded erase operation.



Note: $\overline{CE}$ refers to $\overline{CE}_{1,2}$

17274A-17

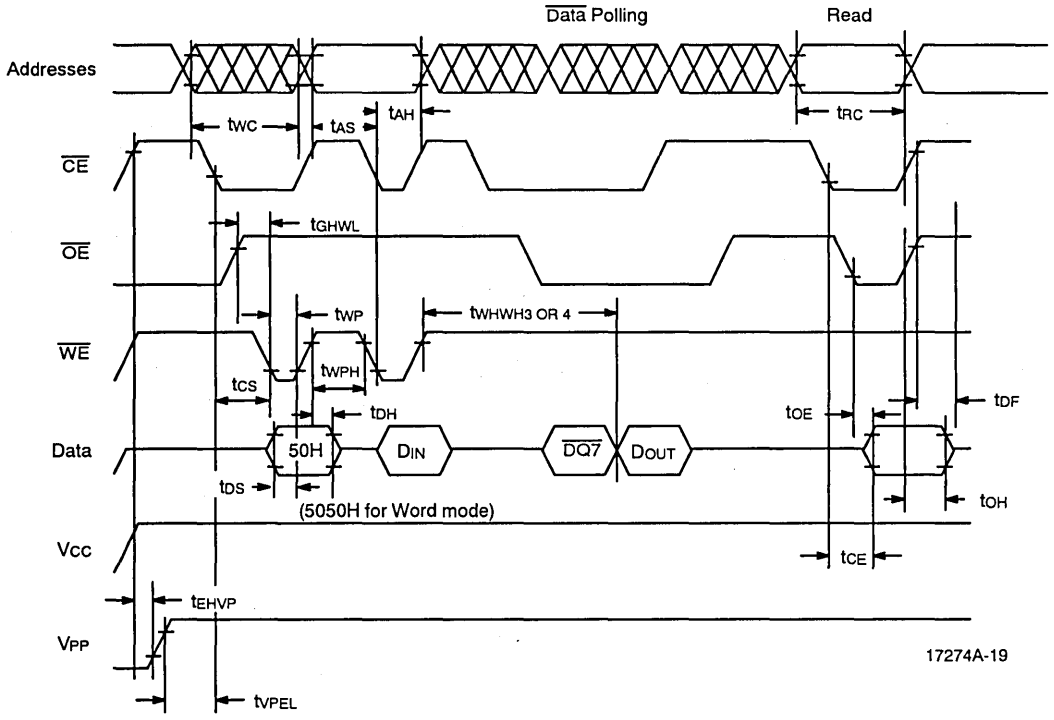
Figure 15. AC Waveforms for Read Operations



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 16. AC Waveforms for Embedded Erase Operation



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 17. AC Waveforms for Embedded Programming Operation

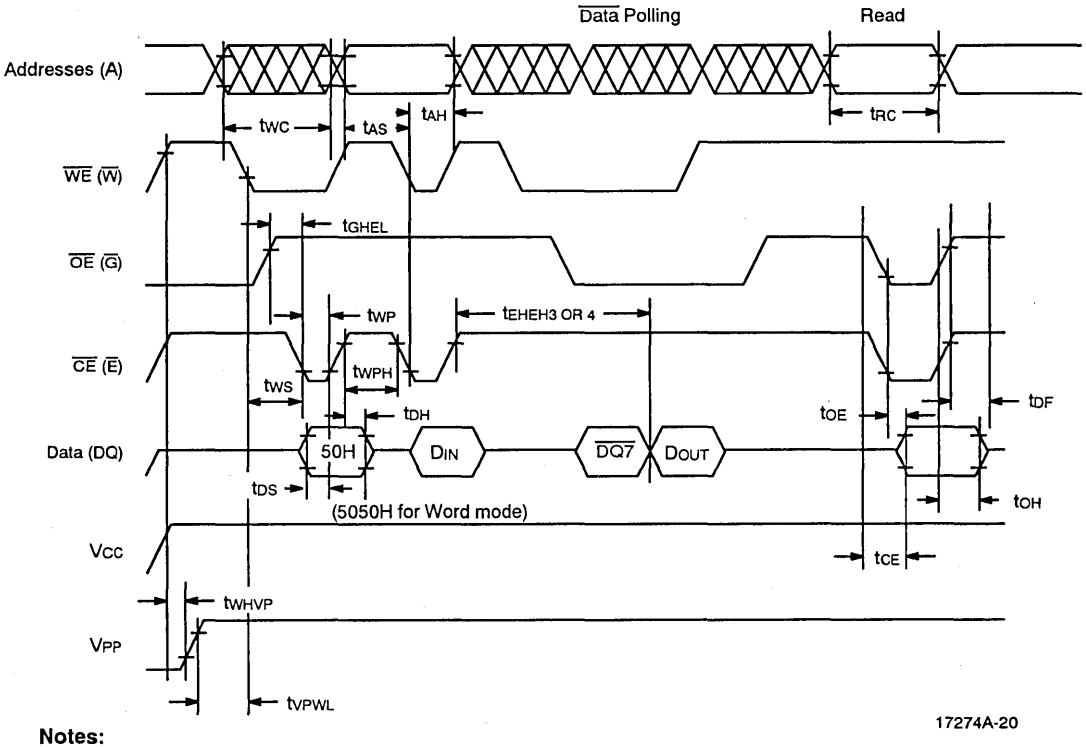
AC CHARACTERISTICS–ALTERNATE $\overline{CE}$ CONTROLLED WRITES

Write/Erase/Program Operations

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVAV}	t_{WC}	Write Cycle Time	250		ns
t_{AVEL}	t_{AS}	Address Set-Up Time	0		ns
t_{ELAX}	t_{AH}	Address Hold Time	100		ns
t_{DVEH}	t_{DS}	Data Set-Up Time	80		ns
t_{EHDX}	t_{DH}	Data Hold Time	30		ns
t_{GLDV}	t_{OE}	Output Enable Hold Time for Embedded Algorithm	10	150	ns
t_{GHEL}		Read Recovery Time before Write	0		µs
t_{WLEL}	t_{WS}	WE Set-Up Time before $\overline{CE}$	0		ns
t_{EHWH}	t_{CP}	WE Hold Time	0		ns
t_{ELEH}	t_{CP}	Write Pulse Width	100		ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH (Note 3)	50		ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	14		µs
t_{EHEH4}		Embedded Erase Operation for each 256 KB Memory Segment (Notes 1, 2, 4)	5		s
t_{VPWL}		V_{PP} Set-Up Time to Write Enable LOW	100		ns

Notes:

1. Rise/Fall < =10 ns
2. Maximum specification not needed due to the internal stop timer that will stop any erase or write operation that exist the device specification.
3. Chip Enable Controlled Programming:
   Flash Programming is controlled by the valid combination of the Chip Enable ($\overline{CE}_{1,2}$) and Write Enable ($\overline{WE}$) signals. For system that uses the Chip Enable signal(s) to define the write pulse width, all Set-up, Hold, and inactive Write Enable timing should be measured relative to the Chip Enable signal(s).
4. Embedded Program Operation of 14 µs consist of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.
5. Embedded Erase Operation of 5 seconds consists of 4 seconds memory segment pre-programming times and 1 second memory segment erase time for each 256K byte memory segment. This is typical time for embedded erase operation.



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{Q7}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 18. Alternate AC Waveforms for $\overline{CE}$ Controlled Embedded Programming or Erasing Operation

CARD INFORMATION STRUCTURE

The AmC004AFLKA contains a separate 512 byte EEPROM memory for the Card Information Structure. All or part of the 512 byte could be used for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space. Part of the common memory space could also be mapped into the attribute memory space if more than 512 bytes of CIS are needed.

The EEPROM used in the AmC004AFLKA is a NEC μPD28C05GX-20-EJA designed to operate from a 5 V single power supply. The μPD28C05 provides a DATA polling function that provides the End of Write Cycle, Chip Erase and Auto Erase and Programming functions.

SYSTEM DESIGN AND INTERFACE INFORMATION

Power Up and Power Down Protection

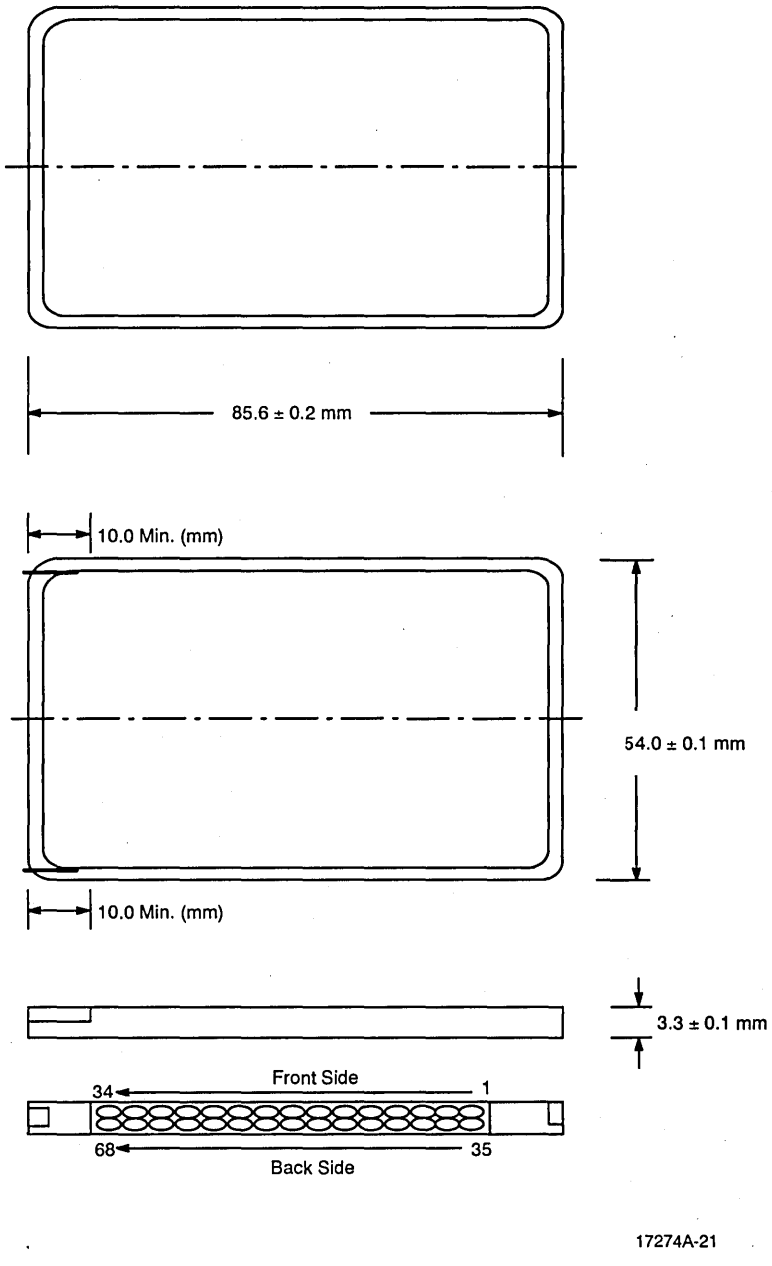
The PCMCIA standard socket provides for proper power up and power down sequencing via different pin lengths to ensure that hot insertion and removal of the PC card will not result in card damage or data loss.

AMD's Flash memory devices are designed to protect against accidental programming or erasure caused by spurious system signals that might exist during hot insertion, hot removal, or power transitions. The AMD PC card will power-up into a READ mode and the card will function as a read only memory as long as V_{pp} is less than V_{cc} +2 V. Erasing of the memory segments can be accomplished only by writing the proper Erase command to the card twice along with the proper Chip Enable, Output Enable and Write Enable control signals.

System Power Supply Decoupling

The AMD Flash memory card has a 0.1 μF decoupling capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins. It is recommended the system side also have a 4.7 μF capacitor between the V_{cc} and the GND pins, and between the V_{pp} and the GND pins.

PHYSICAL DIMENSIONS
Type 1 PC Card



17274A-21

ADVANCE INFORMATION

AmC001BFLKA

1 Megabyte 5.0 V-Only Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5 V-only operation**
  - Writing, Erasing, and Reading
  - Eliminates the need of a 12 V DC/DC converter
  - Minimum 50% system level power reduction during Programming/Erasing operations when compared to 12 V Flash technology
- **1 Megabyte capacity**
- **High performance**
  - 150 ns maximum read access time
  - 38 µs typical byte/word write time
- **High endurance**
  - Minimum 100,000 erase and write cycles per 16K byte sector
  - Increases effective endurance via software controlled wear leveling
- **16K byte sectors architecture**
  - Typical sector program time of 600 ms
  - Typical sector erase time of 1.5 seconds
  - Background erasing increases programming performance
- **Automated Write and Erase operations**
  - Increase system level performance
  - Embedded Erase™ algorithm automatically pre-programs and erases selected 16K byte sectors
  - Embedded Program™ algorithm automatically programs data at specified address
- **CMOS low power consumption**
  - 20 mA typical Read current (x8)
  - 30 mA typical Write current (x8)
  - 300 µA typical Standby current
- **PCMCIA/JEIDA 68-pin standard**
  - PCMCIA standard Mass Storage PC Card
  - Byte or Word-wide configuration
- **Mechanical write protect switch**
  - Prevents accidental data loss
- **Flash file system compatible**
  - Support from independent software and hardware vendors

GENERAL DESCRIPTION

AMD's 5.0 V-only Flash memory PC cards are based on AMD's 5.0 V-only Negative Gate Erase Flash technology. The 5.0 V-only Flash PC cards provide the highest level of performance for data and file storage solution to the portable PC market segment. The 150 ns access time allows operations of high-speed microprocessors without wait states. AMD's 5.0 V-only Flash technology eliminates any need for a 12 V DC to DC converter and provides a minimum of 50% power reduction as compared to the typical 12 V Flash technology. The Embedded Erased and Embedded Program algorithms greatly enhance the host system performance by allowing the host system to multitask while the PC card performs erasing or programming in the background.

When used with Flash file management software such as Microsoft's Flash File System II (FFS II), AMD's Flash memory PC card emulates disk like operations and enables the Flash technology to be transparent to the end user. AMD's 5.0 V-only Flash PC card provides portable PC OEM system manufacturers with a rugged, high performance, light weight and low power all solid state mass storage solution not obtainable by any rotating mass storage media.

PRODUCT SELECTOR GUIDE

5.0 V Program/Read

Part Number	Organization	Access Time	Temp. Range	Pin Count	CIS	Program/ Erase	Supply Voltage	Programming Voltage
AmC001BFLKA	1 Mbyte x 8, 512 Kbyte x 16	150 ns	C	68	512B x 8	Embedded	5 V ±5%	5 V ±5%
AmC002BFLKA	2 Mbyte x 8, 1 Mbyte x 16	150 ns	C	68	512B x 8	Embedded	5 V ±5%	5 V ±5%

Notes:

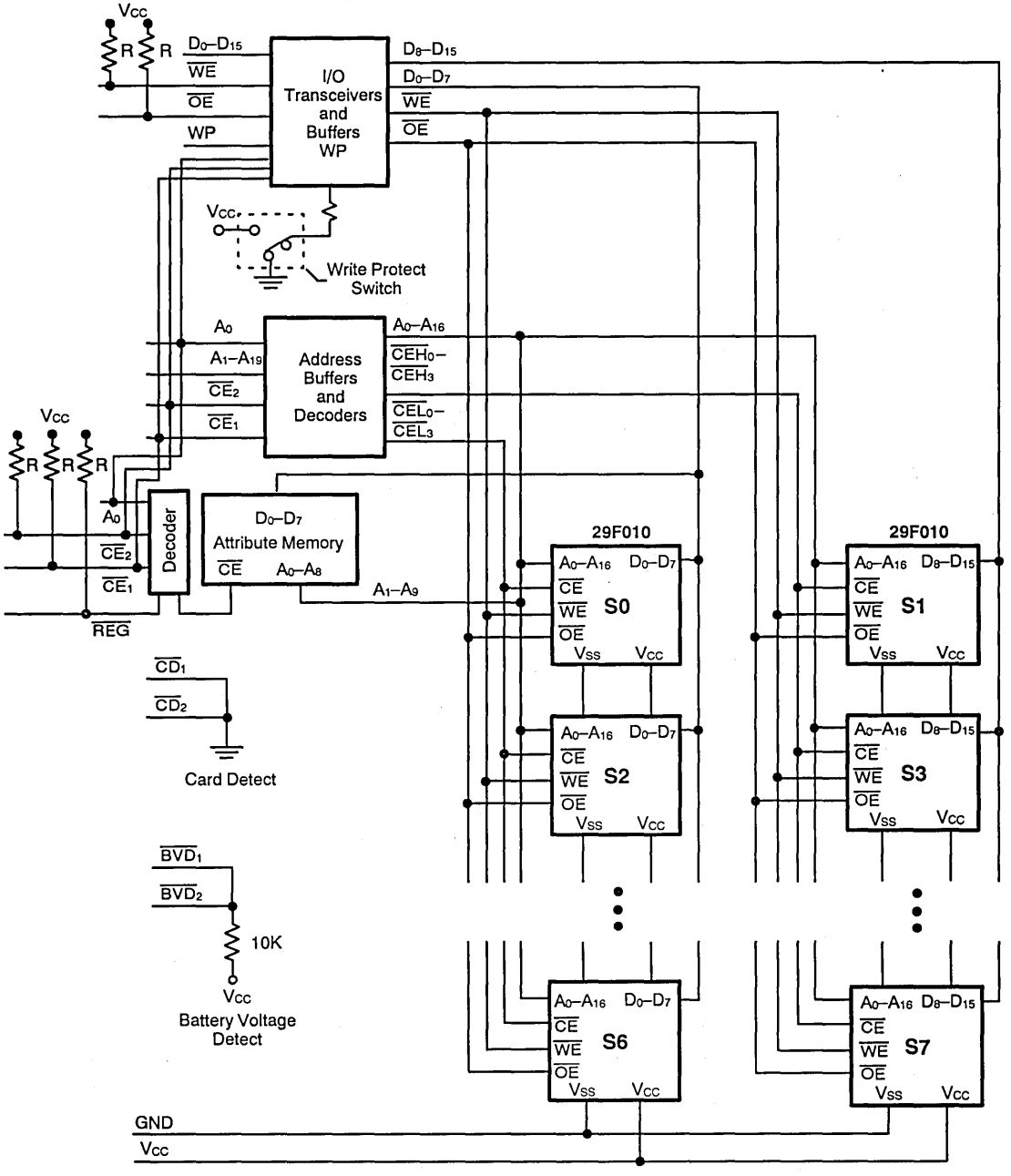
Temp Range: C = Commercial (0°C to 60°C)

CIS: Card Information Structure is stored in a 512 byte EEPROM

Program/Erase: Embedded = Embedded Program and Embedded Ease algorithm

Publication# 17277 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



R = 33K

17277A-1

PC CARD PIN ASSIGNMENTS

Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	RFU		Reserved
11	A_9	I	Address Bit 9	45	RFU		Reserved
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	NC		No Connect
16	RDY/$\overline{BSY}$		Ready/Busy (Note 3)	50	NC		No Connect
17	Vcc		Power Supply	51	V_{CC}		Power Supply
18	Vpp1		Pgm Sply Vltg 1 (Note 1)	52	V_{PP2}		Pgm Sply Vltg 2 (Note 1)
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	RESET		Card Reset (Note 4)
25	A_4	I	Address Bit 4	59	WAIT		Extend Bus Cycle
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.

1. V_{PP} not required for Programming or Reading operations.
2. $\overline{BVD}$ = Internally pulled-up.
3. Signal must not be connected between cards when I/O interface is supported.
4. Reset must not be connected between cards unless all cards are reset when any card has V_{CC} power removed.

ADVANCE INFORMATION

AmC002BFLKA

2 Megabyte 5.0 V-Only Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5 V-only operation**
  - Writing, Erasing, and Reading
  - Eliminates the need of a 12 V DC/DC converter
  - Minimum 50% system level power reduction during Programming/Erasing operations when compared to 12 V Flash technology
- **2 Megabyte capacity**
- **High performance**
  - 150 ns maximum read access time
  - 38 µs typical byte/word write time
- **High endurance**
  - Minimum 100,000 erase and Write cycles per 16K byte sector
  - Increases effective endurance via software controlled wear leveling
- **16K byte sectors architecture**
  - Typical sector program time of 600 ms
  - Typical sector erase time of 1.5 seconds
  - Background erasing increases programming performance
- **Automated Write and Erase operations**
  - Increase system level performance
  - Embedded Erase™ algorithm automatically pre-programs and erases selected 16K byte sectors
  - Embedded Program™ algorithm automatically programs data at specified address
- **CMOS low power consumption**
  - 20 mA typical Read current (x8)
  - 30 mA typical Write current (x8)
  - 500 µA typical Standby current
- **PCMCIA/JEIDA 68-pin standard**
  - PCMCIA standard Mass Storage PC Card
  - Byte or word-wide configuration
- **Mechanical Write Protect Switch**
  - Prevents accidental data loss
- **Flash file system compatible**
  - Support from independent software and hardware vendors

GENERAL DESCRIPTION

AMD's 5.0 V-only Flash memory PC cards are based on AMD's 5.0 V-only Negative Gate Erase Flash technology. The 5.0 V-only Flash PC cards provide the highest level of performance for data and file storage solution to the portable PC market segment. The 150 ns access time allows operations of high-speed microprocessors without wait states. AMD's 5.0 V-only Flash technology eliminates any need for a 12 V DC to DC converter and provides a minimum of 50% power reduction as compared to the typical 12 V Flash technology. The Embedded Erased and Embedded Program algorithms greatly enhance the host system performance by allowing the host system to multitask while the PC card performs erasing or programming in the background.

When used with Flash file management software such as Microsoft's Flash File System II (FFS II), AMD's Flash memory PC card emulates disk like operations and enables the Flash technology to be transparent to the end user. AMD's 5.0 V-only Flash PC card provides portable PC OEM system manufacturers with a rugged, high performance, light weight and low power all solid state mass storage solution not obtainable by any rotating mass storage media.

PRODUCT SELECTOR GUIDE

5.0 V Program/Read

Part Number	Organization	Access Time	Temp. Range	Pin Count	CIS	Program/ Erase	Supply Voltage	Programming Voltage
AmC001BFLKA	1 Mbyte x 8, 512 Kbyte x 16	150 ns	C	68	512B x 8	Embedded	5 V ±5%	5 V ±5%
AmC002BFLKA	2 Mbyte x 8, 1 Mbyte x 16	150 ns	C	68	512B x 8	Embedded	5 V ±5%	5 V ±5%

Notes:

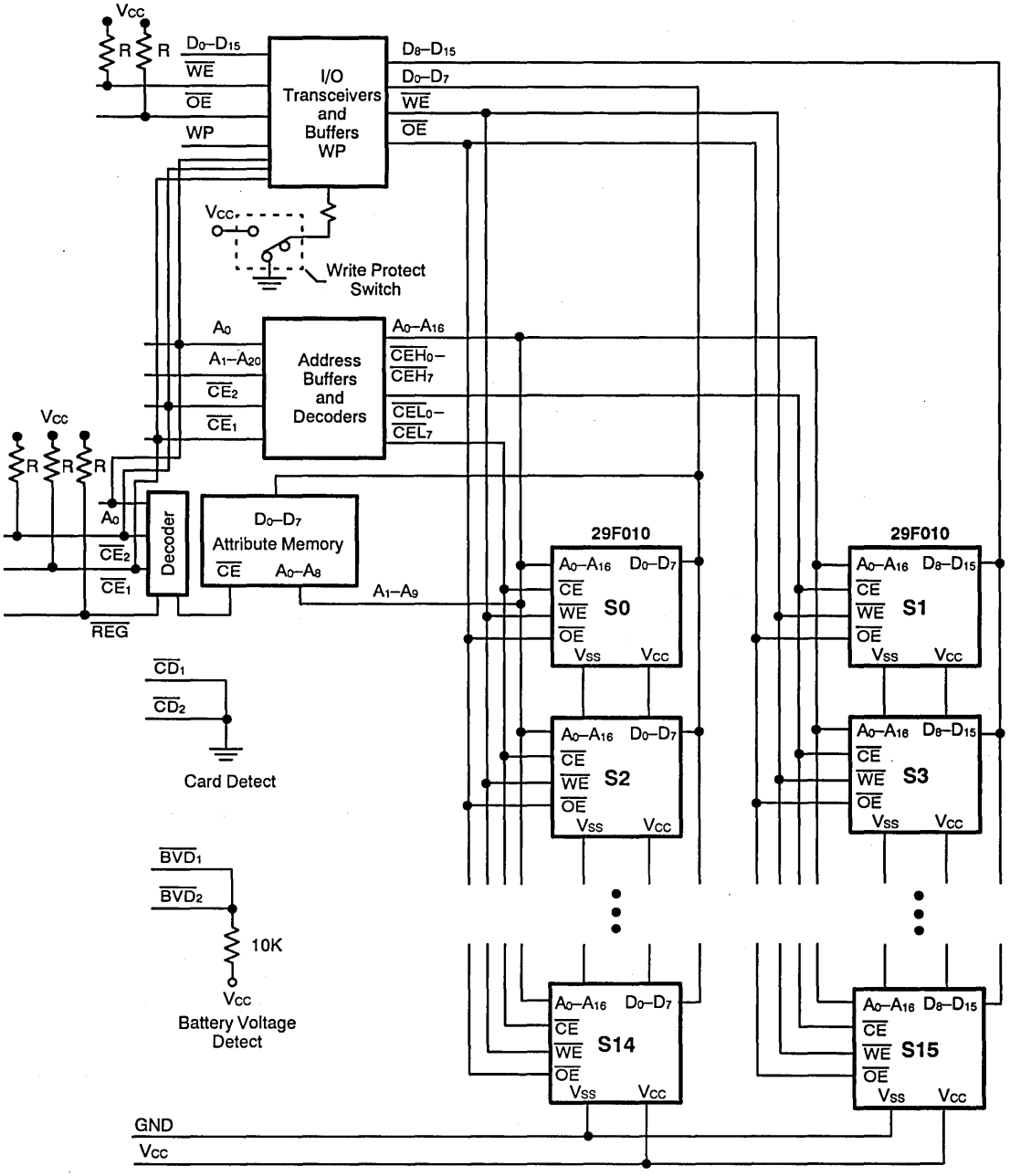
Temp Range: C = Commercial (0°C to 60°C)

CIS: Card Information Structure is stored in a 512 byte EEPROM

Program/Erase: Embedded = Embedded Program and Embedded Ease algorithm

Publication# 17278 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



R = 33K

17278A-1

PC CARD PIN ASSIGNMENTS

Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	RFU		Reserved
11	A_9	I	Address Bit 9	45	RFU		Reserved
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	A_{20}	I	Address Bit 20
16	RDY/$\overline{BSY}$		Ready/Busy (Note 3)	50	NC		No Connect
17	V_{CC}		Power Supply	51	V_{CC}		Power Supply
18	V_{PP1}		Pgm Sply Vltg 1 (Note 1)	52	V_{PP2}		Pgm Sply Vltg 2 (Note 1)
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	RESET		Card Reset (Note 4)
25	A_4	I	Address Bit 4	59	WAIT		Extend Bus Cycle
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.

1. V_{PP} not required for Programming or Reading operations.
2. $\overline{BVD}$ = Internally pulled-up.
3. Signal must not be connected between cards when I/O interface is supported.
4. Reset must not be connected between cards unless all cards are reset when any card has V_{CC} power removed.

A Short Guide Through the Standard of PCMCIA/JEIDA

Application Note
by Peter Heinrich

Advanced Micro Devices

INTRODUCTION

The Personal Computer Memory Card International Association (PCMCIA) was founded with the goal of promoting and guiding interchangability of IC-cards among a variety of computers. Both memory and peripheral functions are included in the 68 pin card specifications. Compatibility between numerous vendors and products is assured for use in small, portable equipment.

The 68-pin connector was originally defined and proposed by the Japanese Electronics Industry Association (JEIDA) to overcome incompatible and proprietary IC-cards. It was then selected as the basic connector to allow a variety of PCs and non-computer consumer products to freely interchange cards and data and also to serve as a peripheral extension for applications such as modems or network adapters. Given the goal of world-wide standardization, the specifics of a wide range of different memory technologies, peripheral requirements and consumer cost considerations had to be addressed. The following summary of the technical aspects of PCMCIA is meant to be a short guide through the standard and will familiarize the user of AMD's Flash memory cards with this environment.

OVERVIEW

PC-Card interchangeability is achieved through three major sections:

- *Card Physical Requirements* such as mechanical, electrical and environmental elements.
- *Card Interface* describing pin assignments and memory types with their specific attributes and electrical characteristics.
- *Data Format* addressing the issues of data organization as well as software executed directly out of the memory card (XIP).

Card Physical Requirements

Mechanical/Environmental

PCMCIA defines all dimensions and tolerances including the location and polarity of optional batteries, a write protect switch and of course the connector itself. The reliability and mechanical performance is managed through stringent requirements for vibration, shock, and insertion and holding forces. Operating and storage temperature, moisture resistance and thermal parameters must meet or exceed military test methods. Also the design of the connector eliminates any mismatch and assures proper sequencing of ground and power connection.

Electrical

All suppliers must meet electrical performance tests including contact resistance, insulation resistance and maximum current and voltage per pin.

The fundamental quality and reliability requirements of PCMCIA cards support applications in very harsh environments. Once a manufacturer meets the quality requirements of this standard he can assure functionality of his product in daily use.

Card Interface

There are two types of PC cards: Memory and I/O. I/O-Cards might need to be configured after reset or insertion. The memory card interface is the default standard after insertion. Every card is described by its Card Information Structure (CIS). If a PC-card is identified or initialized as I/O, some of its pins get a different assignment supporting its functionality.

There are 64 Megabyte of common memory address space and 64 Megabyte of attribute memory address space. The common memory is accessed by the host for standard read and write activities including DMA-support (direct memory access). The attribute memory can be used for two purposes:

- *Card Information Structure*: the mandatory description of the cards capabilities and specifications.
- *Configuration Registers*: the optional set of registers to initialize peripheral functionality.

The size of the attribute memory is defined by the manufacturer, but the CIS-header must always start at address 00H. CIS holds information about the memory type (ROM, OTP, EPROM, EEPROM, FLASH, DRAM or SRAM) and further details such as speed, programming requirements and device I.D.s.

Besides the standard pin assignments, such as address and data, there are special functions: Card Detect 1 and 2 to verify correct card insertion, Write Protect, REG for common or attribute memory access definition, battery low voltage detect, program voltages for dual voltage technology, and Card Reset and Ready/Busy.

Publication# 17239 Rev. A Amendment/0
Issue Date: August 1992

Finally, the electrical signal description and timing specifications define the operating environment including the voltage range for 5.0 and 3.3 V, the signal interface levels and line status and the power up and down sequencing.

Data Format

Before we enter into the software specifics some of the overall objectives of the PCMCIA standard should be outlined.

The definition of the software standard was influenced by these requirements:

- The standard must support different operating system file structures such as DOS or UNIX or even data structures representing VCR or musical recording.
- Elementary data recording such as sequential storage of block of bytes with and without error checking must be easy to do.
- For compatibility with existing operating systems the standard must be able to mirror the disc-like data organization using sectors, tracks and cylinders.
- The direct execution of programs out of the memory card in the operating system dependent data organization must be supported.
- Future expansion should be possible without the need to rewrite existing software.

Such a variety of requirements, sometimes even incompatible, is best outlined in a layer model similar to what is done for networks.

0 Physical Layer
1 Compatible Layer
2 Data Format Layer
3 Data Organization Layer
4 System Layer

Physical Layer

The specifics of this layer guide the mechanical and electrical aspects of PC-cards already mentioned as Card Physicals.

Compatible Layer

Each card should contain the Card Information Structure, CIS, with such fundamentals as card devices, size, speed, programming and so on.

A card can comply at level 1 without the requirement for any higher level thus supporting an "open" PCMCIA standard. The CIS must always start at address 0 but it can be mapped into either the attribute or the common-memory space. The definition of the coding of data blocks, called tuples, supports variable chaining and linking of all the data information within a PC-card's memory.

Data Format Layer

This layer is analogous to the physical format of a floppy disc in the way the data is specified at the lowest level. Supported formats are:

- Blocked Bytes (unchecked or checksummed)
- Blocked with CRC
- Unblocked (as done in the Microsoft Flash File System)

Data Organization

Here the logical organization of blocks and bytes are defined. Examples are:

- DOS (or any other) File System
- Flash File System
- Execute In Place (XIP) Image
- Application Specific Organization

System Layer

This describes the operating system dependent environment and the possibility of sharing PC-cards through networks or multi-user access.

Execute-In-Place (XIP)

While memory cards offer many advantages as floppy or hard disk replacement, a major performance improvement can be achieved when software is executed directly out of the memory rather then downloaded into the computer's DRAM.

In order to get an understanding of XIP, three implementation concepts are of interest.

- *XIP partitioning:* A partition is simply a region within a card's memory containing a header and one or more applications with all its details.
- *XIP loader* uses a driver interface to find a specific application within an XIP directory. The loader's responsibility is to look up, map and start the XIP application.
- *XIP application programming interface* defines the entry points for calling procedures, all applications memory mapping services and the XIP directory management.

FLASH MEMORY CARDS

Flash is today's most exciting technology for memory cards. They offer non-volatility as well as advantages in size, power, performance and reliability.

Flash cards are being used as simple data carriers between portable and desktop computers, as well as replacements for floppy and hard disks. In addition, they also add a new environment where the execution of

programs can be achieved with higher performance than in typical down-loading schemes of standard hard disk/DRAM architectures.

The pace of innovation of Flash technology will require extensions of the current PCMCIA standard to address the need for more memory space (a type III 88-pin connector could be a choice) and possibly lower voltage operation.

Although there is a high level of detail in PCMCIA standards, numerous applications of Flash cards might not need to deal with the rather complex operating system and software issues but still benefit from this rapidly growing market with its attractive cost and features.

** Guiding Document is the PC-Card Standard Rel. 2.0 Manual available from PCMCIA 1030B East Duane Avenue, Sunnyvale CA 94086.*

SECTION

4 PUBLISHED FLASH ARTICLES

Technical Feature

Automated Algorithms Enhance Flash-based PC Card Programming

Increases in system level performance, reductions in programming time and improved system access can be realized by employing automated algorithms.

One of the goals of the PCMCIA software standard is to create an environment that accepts interchangeable PC cards. There are three main layers of software that enable interchangeability. Generally they may be referred to as the top, intermediate, and lowest layer. Top layer software drivers include BPB/FAT device drivers, Flash File System redirected LAN-type device drivers and eXecute-In-Place drivers that support direct memory-mapped executable files from extended memory.

The lowest layer is defined as "BIOS Socket Services." This set of software calls provides a common interface for implementing specific hardware functions to the card interface hardware. Software and device drivers above this layer are isolated from a particular hardware implementation.

The intermediate software layer is called "Card Services." This layer provides the technology and manufacturer-specific device drivers to control read and write operations of the memory devices on the PC card. The primary purpose of Card Services is to support Flash memory technology. It is the contents of Card Services that allows the PCMCIA system functional compatibility between Flash cards built by different manufacturers and/or populated with different memory technologies. The device drivers in Card Services are called Media Technology Drivers. The MTDs used by a system may be resident in a PCMCIA card supporting BIOS or provided with the PC card and installed during system boot.

The installable MTDs require part of the allocated system RAM for all drivers. This consideration is important for Flash-based cards since device drivers for Flash technology are characterized by repetitive software algorithmic control of the devices. However, the performance of the Flash-based PC card is improved by employing automated programming operation, such as automated algorithms. A commercially available Embedded Algorithm™ product is on the market. System level performance is increased since the bus accessing requirements between the CPU and card interface are practically eliminated. Automated algorithms also reduce reprogramming time. In addition, the system access to the PC card is improved when memory devices are being erased in the background while allowing read or write accesses to other devices. This article describes these system level performance improvements for a Flash-based PC cards applications.

System level effects

The nature of the original Flash software control algorithms demands intensive access between the host CPU, ISA bus, and card interface.

About the Author:

Kurt Wolf is Senior Product Marketing Engineer, Flash Memories, at Advanced Micro Devices. He is a graduate of the University of Michigan and is active in a variety of professional associations.

Reprinted from Memory Card: March/April 1992

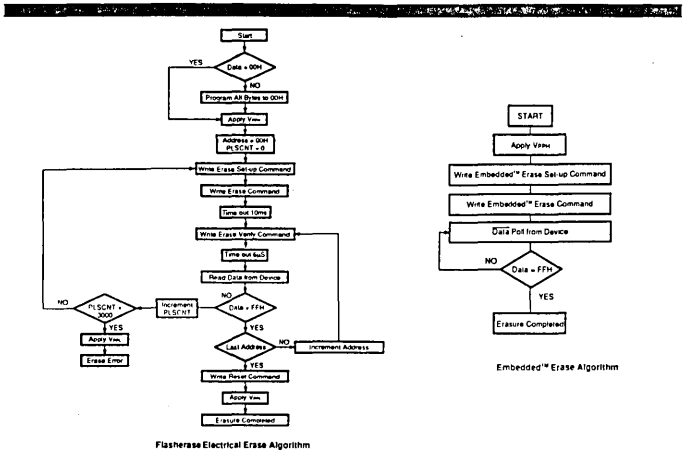
This is because Flash memories are reprogrammed with repetitive sequences of commands in order to control the device during write operations. This overhead on the system CPU and bus accessing may impact system level performance if other multi-tasking applications are in operation while Flash card writes are in progress.

Flash erase operations provide a good example of this overhead. Prior to erasure, the entire Flash device must be pre-programmed. This requires sequences of two bus cycle write commands to each address location, CPU timed program pulses, and card read operations in order to verify that data has programmed correctly.

After the device is completely programmed, the system must issue another sequence of two bus cycle write commands, CPU timed erase pulses and a sequence of card reads at each individual address location of the accessed Flash Device. Two Megabit Flash memories require 256K preprogram commands, 256K card read accesses for preprogrammed data verifications, and 256K card reads for erase verification.

Since the host CPU must control the Flash devices during reprogramming operations, this procedure may be halted if the CPU is required to service interrupt routines such as communication applications handling data transmission. Halting the reprogramming operations tends to degrade the performance of the Flash-based disk.

Algorithmic control tends to restrict card accesses during write or erase operations. The Flash devices on the PC card share a common data and address bus. The targeted Flash device also requires an active chip enable (CE) control line in order to maintain the state machine sequence for proper execution of the software algorithm. Disabling CE resets the state machine to the read mode. If the targeted device was disabled in order to access another device on the card the sequencing of the state machine would be lost and the algorithm would need to be reset. This further complicates the software control of algorithmic Flash devices.

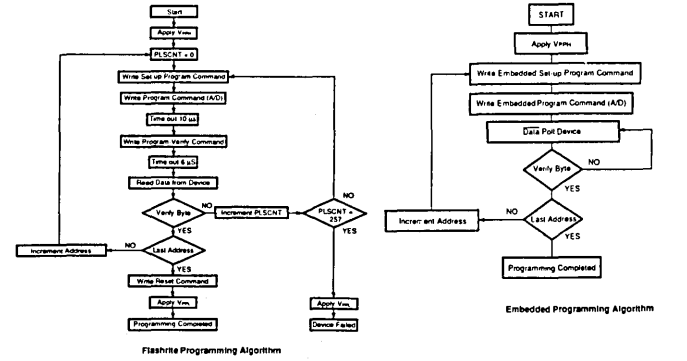


Comparison of software controlled and embedded erase algorithms.

Embedded Algorithm advantages

System level performance in the above areas can be improved by using automated Flash algorithms. Automated algorithms essentially provide a software solution in the Flash memory silicon. The automatic erase operation provides a good example of the improved efficiency. With these algorithms the entire erase process is simplified to a two sequence bus command eliminating all the repetitive card accesses required of software controlled algorithms.

The Embedded Algorithms product uses a new data command to invoke



Comparison of software controlled and embedded programming algorithms.

the fully automated erase operation. Once this sequence is completed the device tri-states the outputs in order to take itself off the PC card bus. The device then automatically preprograms all address locations and verifies data prior to erase. With the preprogramming completed, the internal state machine issues repetitive erase pulses and internally verifies that all address locations are adequately erased prior to resetting the device to the read mode and turning control of the device back over to the system.

Automatic support of Write Operation Status (WOS) feature is also available on commercial products. This tells the system when the device has completed the program or erase operation. This feature does not require an additional command nor does the system need to toggle control pins to activate the WOS feature. It works in a similar manner as an EEPROM. Once the Embedded Algorithm operation is in progress the device outputs provide the Data Polling and Toggle bit function on DQ7 and DQ6 respectively. The outputs are active when the device is accessed for read operations by enabling OE. Otherwise the device forces the outputs into a tri-state mode taking the device off the bus.

Advantages to automated algorithms

There are a number of system level advantages provided by automated algorithms. First, the overhead of the host CPU and card interface is dramatically reduced allowing for better system performance during operation of multitasking applications. The three quarter of a million bus accesses described earlier for device erasure are now replaced by one sequence of a two bus cycle command.

One other advantage of the Embedded Algorithms is that it decreases reprogramming time. This performance advantage increases if the CPU services interrupts while in the process of reprogramming. The software controlled algorithms must halt the program or erase sequencing during these service routines which increases the total time of the reprogramming operation. In addition, the automated algorithms do not require the software designer to worry about safely terminating and saving the point of interruption in the reprogramming sequence.

When the device tri-states its output other devices on the card may be accessed for read or reprogramming operations. This increases the card's read/write performance by allowing multiple operations to be performed at one time. Also, time efficient background erase operations can be performed easily by the system. Other devices on the card can be accessed while a device is performing one of the automated algorithms operations since the device will continue to draw active current until the operation is complete. When completed the device current will dramatically decrease to the super standby level. The only system requirement to support concurrent program or erase operations is to be able to supply the adequate level of current.

Automatic algorithms also address the issue of vendor compatibility. As other Flash silicon vendors support automatic programming operations the differences in vendor specific algorithms become transparent to the system interface. This tends to increase device compatibility without requiring the system designer to accommodate different algorithms for each vendor. In addition, automatic algorithms reduce the system designer's dependence on keeping track of changing algorithmic timings due to process evolution.

Sector erase

The performance improvements allowed by the Embedded Algorithms are also multiplied by the addition of sector erase capable Flash devices. It is expected that some Flash vendors will be announcing new device architectures based on sectors of equal size. Sector erase typically allows any sector, any combination of sectors, or the entire device to be erased concurrently.

Performance is increased with the addition of automated sector reprogramming primarily in the area of background erase or "garbage collection" routines employed by various file systems. The flexibility of these operations is increased when only a portion of the device is required to be erased or "cleaned up." In addition, the sector capability tends to extend the effective endurance of a Flash memory. Intelligent software can even out the sector erase operations across those available throughout the card. Only that portion of the device targeted for erase is exercised leaving the rest of the device unaffected.

Summary

The performance of the Flash-based PC card is increased by employing automated programming operations. System level performance is increased since the bus accessing requirements between the CPU and card interface are practically eliminated. The reprogramming time also is decreased and the system access to the PC card is improved by allowing for memory devices to be erased in the background while accessing other devices for read or write operations. Potential software complications due to interrupt servicing is also dramatically reduced.

Automatic algorithms tend to reduce the differences in vendor specific algorithms due to technology and/or process differences or improvements. Combining sector erase with the automated algorithms improves the efficiency of file systems during garbage collection routines. A feature of sector erase also tend to increase the effective endurance of the Flash-based PC Card.

Although the first generation of Flash devices provided minimum functionality in a PC card environment, device enhancements and next generation architectures are addressing these issues. System level performance improvements are available from automated algorithms and equal sector erase capability. □

Reprinted from Memory Card: March/April 1992

SEMICONDUCTOR MEMORIES

Making EPROM/flash trade-offs

By Datar Lalvani
Strategic Marketing Manager
and Kurt Wolf
Senior Product
Marketing Engineer
Advanced Micro Devices Inc.
Sunnyvale, Calif.

The non-volatile memory market, long the bastion of the UV EPROM, has been fissured with the recent emergence of in-system reprogrammable flash memories as a viable technology. Today, both EPROMs and flash memories coexist and they will continue to run parallel paths, with the choice of technology influenced by the requirements of the end product.

Flash memories were born of the marriage between EPROM and E²PROM devices. Flash incorporates the same programming capability as an EPROM with the added benefit of E²PROM-like electrical erasability, so it can be reprogrammed without removing it from the circuit board. This makes flash an ideal choice for applications that require in-system reprogrammability. While the same benefit can be obtained from either E²PROM or battery-backed SRAM, flash memories are less expensive than both.

In light of the projected rapid growth in demand for flash, the product-development plans announced by the ever-increasing number of vendors, and the recent public announcements by some large vendors—who have stated that their strategy is to "de-emphasize" EPROMs in favor of flash memories—the future of EPROMs has become unclear. This has caused some confusion in the memory marketplace. Technical factors such as scalability, die cost, erasure and package considerations—as well as market-based factors such as demand, applications and features—factor into the decisions to build and use either EPROM or flash products.

EPROMs and flash memories will coexist with the choice of technology influenced by the requirements of the end product as used by the customer. While some vendors have stated that flash memories are more scalable than EPROMs with the addition of double-layer metal,even down at 0.5-micron geometries, Advanced Micro Devices Inc. sees no need for multilayer metal for EPROMs. AMD's single-layer metal process for EPROMs using 0.5-micron technology not only will provide the high density—up to the 16-Mbit level—but is also capable of generating the smallest die size and highest performance in the industry.

It is a fact that, at the same density, the flash-memory die is more expensive than an EPROM because it has the slightly larger cell size required to support high endurance. Also, the flash process complexity is greater due to additional masking steps, and it requires longer test times to perform electrical erasure in the tester, as opposed to UV-erase in an oven.

Flash pricing today remains at a multiple of EPROM. However, flash pricing will continue to drop until it settles at around a 20 percent to 30 percent premium over a comparable EPROM. Memory designers are not going to increase the cost of their systems by using flash when there is no need for future reprogramming. In these designs, reprogrammability does not represent value to the customer. Consequently, flash technology will not ubiquitously replace OTP EPROM designs.

The market's demand for various price/performance products supports the coexistence of both EPROM and flash technology.

There is no question that flash technology has already reserved a bright spot in the history of non-volatile memories. In some designs, however, EPROM and flash memories can coexist comfortably. Laser-printer designs are becoming commodity-oriented items. Memory-design requirements are dictated by the pages-per-minute output of the printer. Memory designers can make a trade-off between designing interleaved systems with slower/less expensive devices or non-interleaved systems using faster/higher-cost devices. The software requirements for these systems are also fairly straightforward. Firmware that typically does not change in this system are the PCL-5 and/or Postscript engine-control codes.

In addition, the code for font types does not typically change. The density requirements for this code range from 2 to 4 Mbytes of storage, depending on the font types available and the number of scaling options. EPROMs instead of ROMs are used to provide manufacturing flexibility. The EPROMs are programmed just-in-time, depending on the printer engine and font options

Datar Lalvani holds a BSEE from the University of Madras, India, and an MBA from the Wharton Graduate School of Business, University of Pennsylvania. Kurt Wolf holds a BSEE from the University of Michigan.

Choosing flash or EPROM

Continued

required for that day's manufacturing run. Flash memory is then incorporated as an option that allows end users to store customized fonts or screen images in the printer. This eliminates the repetitive delay associated with transferring the bit-map-generated images between the computer and printer. This decrease in productivity is eliminated when the code is resident on the printer in flash memory, a clear example of a very high-volume product that requires both high-density EPROM and flash-memory devices.

Each technology is employed to take advantage of its strengths. OTP EPROMs are used in the most cost-sensitive portion of the memory system where the code typically does not change once the system is shipped. OTP EPROMs also allow for smooth transitions between manufacturing runs that incorporate different printer engines and/or font type options.

The higher-priced flash devices provide customers with the ability to personalize their systems. The value of this functionality more than offsets the incremental cost of the devices.

REPROGRAMMING ADDS SOME FLASH TO CELLULAR COMMUNICATION

By Ian Williams
and Kurt Wolf
Marketing Mgrs.
AMD Inc.
Sunnyvale, Calif.

Adding value such as easy reprogrammability to a cellular communications system can bring about another market surge in this popular technology. It is a given that cellular phones allow people to make more efficient use of their driving time. However, if a user wants to change cellular carrier companies for more competitive rates and/or features or move to an area not covered by his/her current carrier, the cellular phone must be reprogrammed at a cellular service service center, a procedure that can cause many hours of unproductive phone downtime.

The use of Flash memory in cellular phones can speed up that update process. For example, a customer who doesn't have the use of Flash memory who decides to change cellular has to bring his phone to the shop, where the phone is disassembled to remove and replace the old EPROM with a newly programmed device, then reassembled and, finally, reinstalled in the car. This is a time-consuming process and involves the expense of new components. The total cost includes the labor costs associated with manually changing code that is typically stored in EPROM and the lost productivity that occurs when the customer's phone is unavailable.

Remote memory updates with a Flash memory-based system are more cost-effective than any other non-volatile memory system. The piece-part price of Flash memories is greater than EPROM- and ROM-based memories. However, the cost of updating memory contents in a remote memory system that is EPROM- and ROM-based is orders of magnitude more costly than performing remote updates on a Flash memory-based system. This cost difference is driven primarily by the cost of the labor required to update firmware in EPROM- and ROM-based systems.

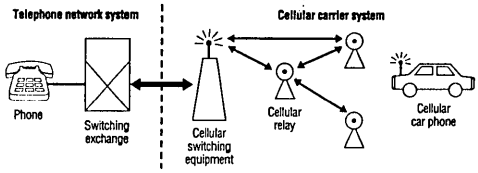
The Flash memory-based system evolves to one that employs a combination of both Flash and other non-volatile memory alternatives. Over time, more and more of a system's firmware becomes stable and does not require future updates. This usually includes the basic structure of the firmware program but not the specialized subroutines it may call.

At this point, a lower-cost memory system is implemented with a combination of Flash and other non-volatile memory. The Flash memory stores those portions of code that many change in the future.

Subroutines that allow the host system to interact with other remote external systems are examples of code segments that may be periodically updated. The alternate non-volatile memory devices store the main structure of the firmware that remains stable.

In fact, Flash memories offer benefits throughout the entire cellular communications system, which is comprised of the main switching equipment, the site relay, and the phones themselves (see figure).

Cellular communication system ripe for flash-memory use



The main cellular switching equipment serves as a link between the telephone network system to provide access for the customer. The switch equipment acts as a controller for the cellular relays, which convert the RF phone signals to analog. The relays also employ transceivers to send and receive the phone communications. The main system switch monitors its network of relays and determines call placement and routing.

The cellular switching equipment is responsible for connecting calls into the telephone network system and for monitoring and controlling its cellular relays. The switches contain the routing algorithms for call placement. These algorithms take into account the traffic load of the cellular sites and the geographic terrain that may affect relay of the transmitted signals. The main switching equipment also keeps track of customer databases, which maintain a file of phone service features that are active for each customer. Among these features are call waiting, call forwarding, and voice mail.

The cellular phone itself contains the basic communication techniques between the phone and the cellular relays, the system parameters that allow communication with the customer's specific cellular carrier. The caller's phone number is also contained within the phone in order to identify which customer is accessing the system and which features should be activated. The Digital Tone Modulated Frequency (DTMF) parameters are also stored in order to allow for automated touch-tone functions such as voice mail.

Another application for Flash memories in a cellular communications system is the customer database, which resides in another part of the switching equipment's memory system. Customer databases may be set up as a file structure in the Flash memory space. Each customer file may consist of multiple bytes of address space. Multiple account files may reside on a single Flash device by maintaining files that have an I.D. associated with each customer's account (i.e., the customer's phone number).

This link allows the system to access each user's file during a call to determine which phone service features the customer is entitled to use. Separate codes may exist for both the activation and deactivation of particular service features (i.e., call waiting). An activated service feature may be canceled by adding the deactivation code to the customer's file. Before establishing the phone connection, the system scans the customer file to look for active service features and to check if any features have been canceled.

Today each cellular phone model must be uniquely programmed at the dealer's installation site. Typically, these phones use socketed EPROMs. The installation department programs these EPROMs with appropriate system parameters and DTMF codes to function with the specific carrier chosen.

By contrast, when the user wants to change carriers or moves to a town outside of his current service area, his/her phone must be reprogrammed at a cellular service center.

Flash memories offer an innovative solution to the inconvenience of bringing in your car phone in order to change carriers or when you move from one cellular service area to another., Flash memories, which are electrically programmable in-system, allow code changes to be performed by transferring data over the cellular network.

For instance, a user could schedule his/her phone to be reprogrammed during a morning commute. The cellular service station then dials the user's phone to establish a data link for transmitting data, thus optimizing the inherent communications capability of the cellular system.■

16609A

Flash Memory Cards Energize Portables

by **Kurt Wolf**

Standardization is an accepted industry practice firmly entrenched in desktop computing and is now embraced by mobile computing since the formation of the Personal Computer Memory Card International Association (PCMCIA) in 1989. The PCMCIA membership has rapidly grown to include more than 200 international companies including all of the major manufacturers of hardware, software, semiconductor components, connectors and peripherals.

The work of this committee has already resulted in two releases of the PC card standard. Release 1.0, in September 1990, covered the memory interface, while Release 2.0, in September 1991, specified an I/O interface to support modem, LAN, cellular and radio communications peripherals. The PCMCIA standard defines the PC card's physical dimensions (86 mm × 54 mm × 3.3 mm—Type 1 cards), pin assignments for the 68-pin interface, electrical specifications and software protocols and formats. In addition, Flash memory cards typically weigh in at about 1 oz.

There are five mainstream semiconductor technologies potentially available for integration into mass storage PC cards. These alternatives are Read-Only Memory (ROM), Erasable Programmable Read-Only Memory (EPROM), Static Random Access Memory (SRAM) with battery backup, byte-write Electrically Erasable Programmable Read-Only Memory (EEPROM), and bulk or sector-erasable, electrically writable Flash EPROMs.

ROM-based memory cards are in wide use as a media for software and database distribution, but are not acceptable as a writable media. Because of the requirement to erase EPROM-based cards with a specific frequency of ultraviolate light they are not favorable candidates either. SRAM technology provides the ability to write the card, but incurs a cost penalty in relation to other technologies because it uses a four-transistor memory cell versus the single-transistor memory cell approach of the others. In addition, SRAM cards require a battery on the card to maintain data when the system is powered down or the card removed. Battery life is difficult to predict and always guaranteed to lose power. EEPROM technology offers the byte-write capability of SRAMs and eliminates the problems of battery backup because of its inherent non-volatility, but also uses a more costly multiple-transistor memory cell approach.

Flash memory technology, on the other hand, has the advantages of a single-transistor memory cell, inherent non-volatility, electrical byte-write capability, and high density, but is restricted to bulk or sector-erase (i.e. 16 Kbytes/sector) requirements during write operations that change data in previously programmed address locations. The bulk or sector-erase restriction of flash memory can be sufficiently addressed at the system software level to make this issue transparent to the user. In addition, with the recent announcement of single-transistor, 5V-only flash technology, the previous handicap of designing and supplying the 12V Vpp requirements for write operations can now be eliminated. Flash memory for use in memory cards is available from Advanced Micro Devices, Hitachi and Intel, and others are expected soon.

PCMCIA System Software Key To Integration

Once the PC card was defined and the various memory technologies considered, the challenge still remained to integrate the PCMCIA hardware into the existing DOS environment. Many early adapters of memory card technology were embedded applications that defined and controlled the environment in which its components interacted. In this case, the card sockets, PC cards and software could all be dedicated to a single purpose. The DOS environment is much more general purpose, and hence needs a more flexible and broader solution to integration.

The PCMCIA software committees have worked to create a layered software structure that isolates the system-specific hardware implementation from higher levels of software. This is required, because although Release 2.0 of the PCMCIA standard defines the construction of the PC card, it does not offer the same level of detail on how to implement PC card sockets into the host system.

There are three layers of software addressed by the committee (Fig 1). They begin at the lowest layer with socket services, above that card services, and above that client drivers such as Microsoft's Flash File System or application programs structured in the eXecute In Place (XIP) format.

Socket services, the lowest layer of software, addresses the various implementations of socket hardware and its capabilities. It is designed to allow implementation as a ROM-BIOS extension and hence provide the capabilities of the memory card to the system during initialization. In addition, socket services masks the details of specific hardware actually implemented and provides a universal interface to the higher levels of software.

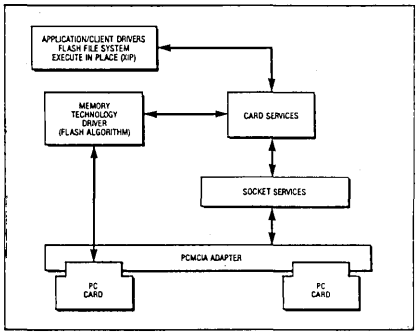


Fig The PCMCIA have created a layered software structure that isolates the system specific hardware implementation from higher levels of software.

Socket services focuses on areas of hardware management including the PC card itself, the card socket, adapters and windows. Card sockets are the actual receptors that make physical and electrical connection to the PC card. Adapters are the hardware that electrically connects the card socket to the system's bus. For example, in order to run XIP applications the adapter must support memory-mapped windows into the host system's memory space. Socket services are responsible for mapping the PC card's memory into system memory through windows. Windows are objects that map the card resources into the host system's memory.

Above socket services lies a resource manager called card services. Its function is to arbitrate the allocation of system resources to the PCMCIA-aware device drivers, utilities and applications. One of the capabilities of card services is to time-multiplex the same socket and card hardware to multiple higher-level software clients. In addition, this resource manager provides a common interface for repetitive tasks such as interpreting the card information structure as PC cards are inserted into the host system. The card information structure is a standard data format that contains sufficient information about the card's capabilities so that the host system can determine if it can communicate with it.

Card services also allow higher levels of software to eliminate the need to know if socket hardware is implemented as a memory-mapped window or is register-based. Socket services provides a universal method to handle special write algorithms for various memory technologies. Requests for read, write, copy or delete are passed to card services which then hands the request to the memory technology driver. The memory technology driver handles the task of executing the appropriate write algorithms required by the active flash memory card. In this way, vendor-specific flash algorithms are handled by the memory technology driver and transparent to software making requests to the flash memory card. Companies recently announcing support for memory card system software are Award, Phoenix, Quadtell and System Soft.

Above socket services are the client drivers that use the resources of the PCMCIA-based system. As part of Microsoft's Portable Computing Initiative, they have announced the Microsoft Flash File System. This product allows flash memory PC cards to function as an ordinary disk in a PC and allows users to run popular applications for MS-DOS and Windows operating systems. The Microsoft Flash File System consists of two device drivers that users can easily load in their CONFIG.SYS files. A higher-level driver provides the interface to MS-DOS and interprets commands from the operating system or application. The lower-level driver performs the requested functions on the flash memory. This driver is also modifiable so that system designers can support any specific flash memory technology.

Single Chip Interface Controllers

The PCMCIA adapter functionality can be implemented as a card controller interface IC. Card controllers connect to the system bus on one side and the card socket on the other. They also offload the host CPU's control of this interface and provide conditioning for all signals into and out of the PC card. The controllers that are commercially available provide system designers a standardized interface to function with standard system software. Controllers include CRC and checksum circuitry to ensure data integrity as data is transferred across the PCMCIA interface and provide for hot insertion and removal of the card. They also provide a solution to EMI-compliant designs not available with a discrete multichip approach. Controller chips also shorten the implementation design cycle and allow products to get to market faster. Controller chips are available from Fujitsu (MB86391), Intel (82365SL), and VLSI Technology (VL82C107-LT "SCAMP").

The widespread industry participation in the PCMCIA standards group and the proliferation of products being produced compatible to this standard ensure that the benefits of truly portable computing are becoming a reality. Today the system designer has flash memory chips and cards available from many suppliers. System software is announced from many of the BIOS companies and from Microsoft that integrate the PCMCIA hardware and software into the existing DOS environment. Interface controller chips are available to speed the time-to-market in hardware design, helping many PCMCIA products to be introduced this year. ■

Kurt Wolf *is senior product marketing engineer for Advanced Micro Devices (Sunnyvale, CA).*

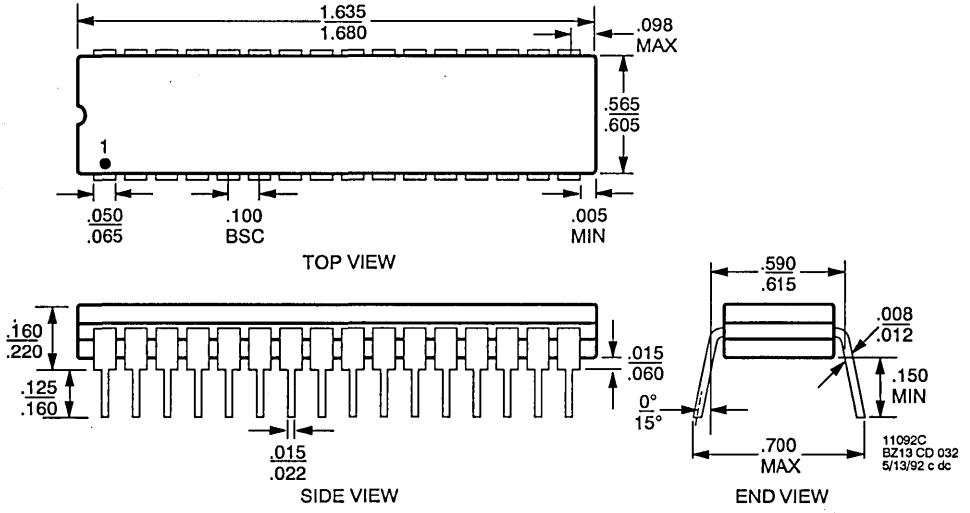
Reprinted with permission from *Computer Technology Review.*

SECTION

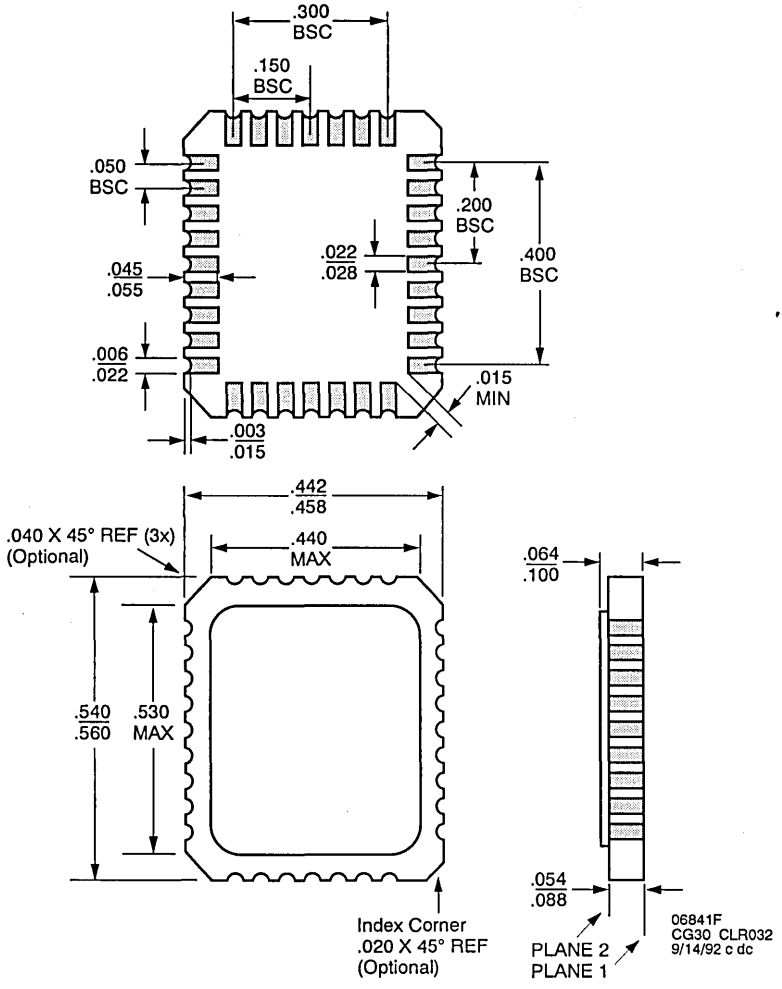
5 PHYSICAL DIMENSIONS*

*For reference only. All dimensions are measured in inches, unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.

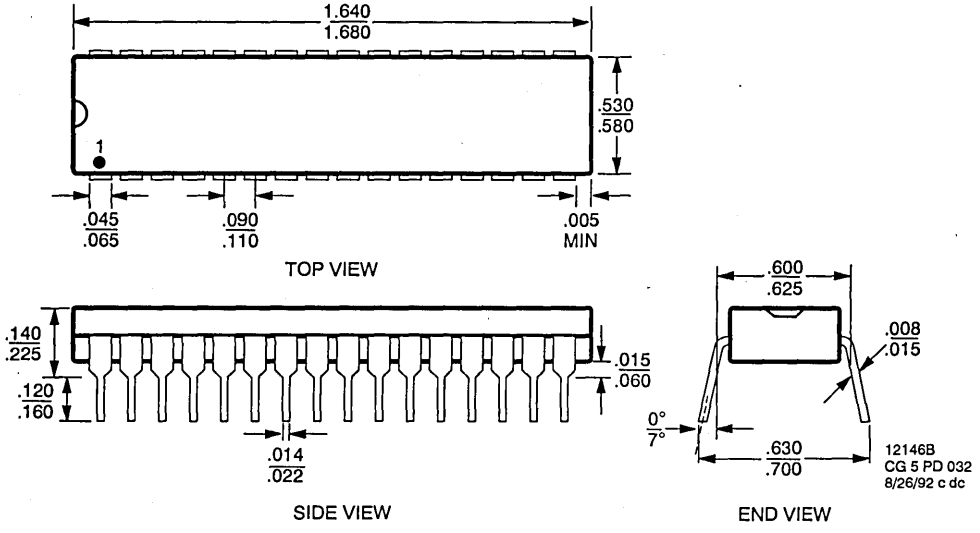
CD 032
32-Pin Ceramic DIP



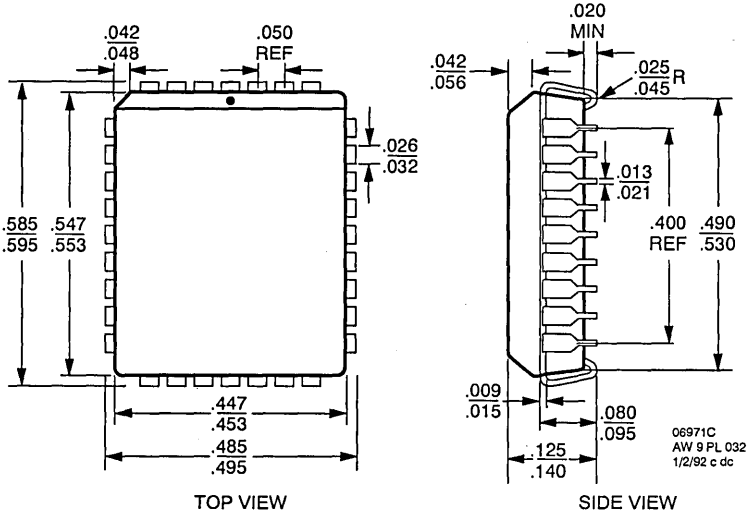
CLR032
32-Pin Rectangular Ceramic Leadless Chip Carrier



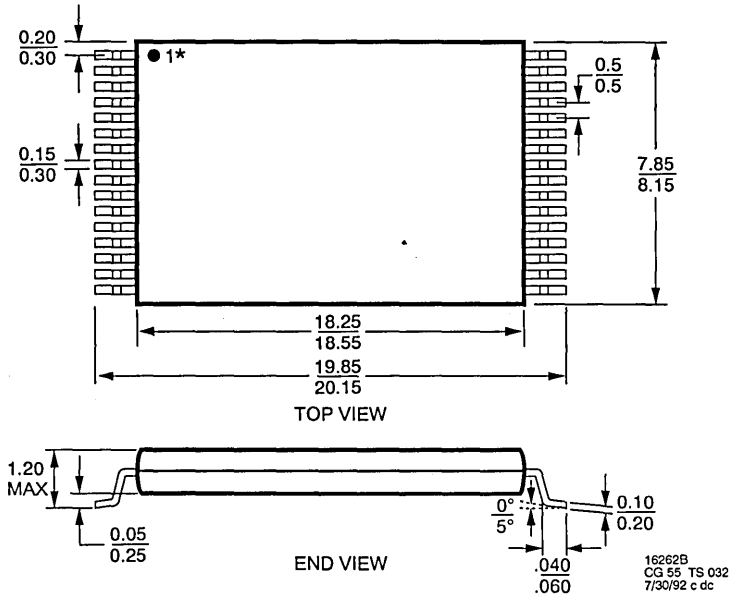
PD 032
32-Pin Plastic DIP



PL 032
32-Pin Rectangular Plastic Leaded Chip Carrier

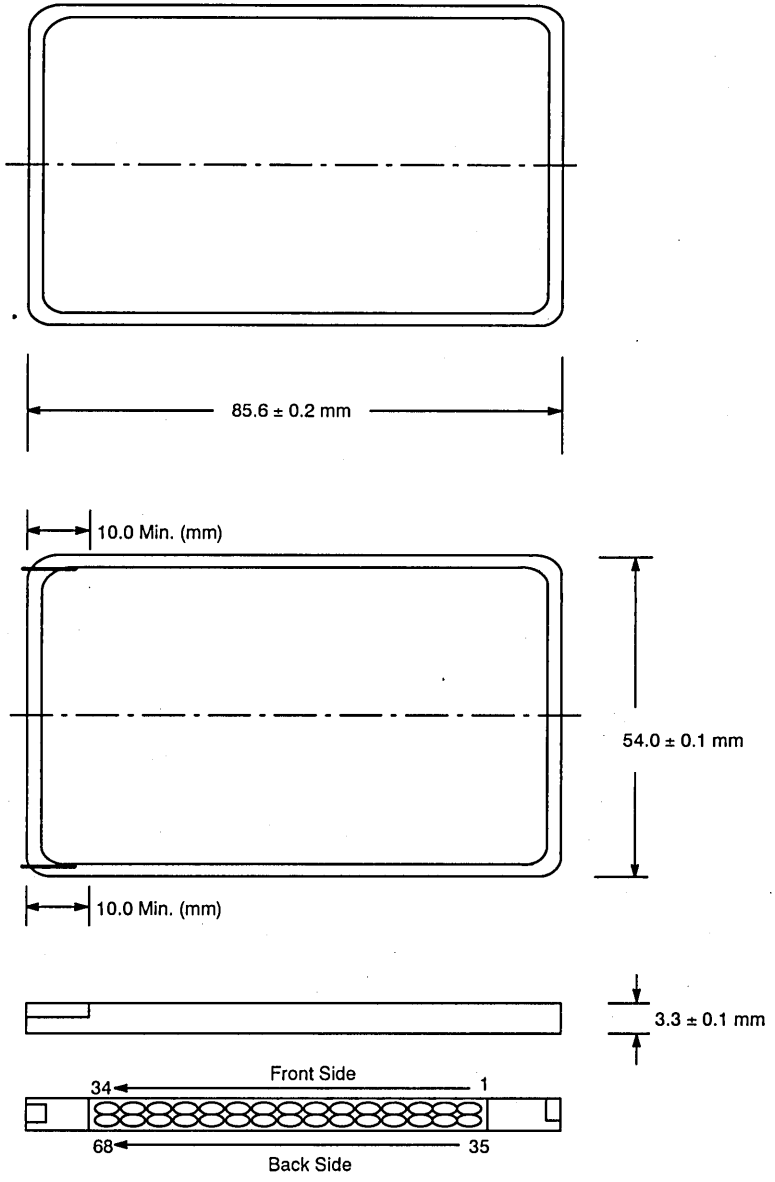


TS 032
32-Pin Thin Small Outline Package (TSOP)



*For the standard form/pin-out, the pin one is a round dimple. For the reverse form/pin-out, an inverted triangle will be marked here indicating pin one.

Type 1 PC Card



Sales Offices

North American

ALABAMA	(205) 882-9122
ARIZONA	(602) 242-4400
CALIFORNIA,	
Culver City	(310) 645-1524
Newport Beach	(714) 752-6262
Sacramento(Roseville)	(916) 786-6700
San Diego	(619) 560-7030
San Jose	(408) 452-0500
Woodland Hills	(818) 992-4155
CANADA, Ontario,	
Kanata	(613) 592-0060
Willowdale	(416) 224-5193
COLORADO	(303) 741-2900
CONNECTICUT	(203) 264-7800
FLORIDA,	
Clearwater	(813) 530-9971
Ft. Lauderdale	(305) 776-2001
Orlando (Longwood)	(407) 862-9292
GEORGIA	(404) 449-7920
IDAHO	(208) 377-0393
ILLINOIS,	
Chicago (Itasca)	(708) 773-4422
Naperville	(708) 505-9517
MARYLAND	(301) 381-3790
MASSACHUSETTS	(617) 273-3970
MINNESOTA	(612) 938-0001
NEW JERSEY,	
Cherry Hill	(609) 662-2900
Parsippany	(201) 299-0002
NEW YORK,	
Brewster	(914) 279-8323
Rochester	(716) 425-8050
NORTH CAROLINA	
Charlotte	(704) 875-3091
Raleigh	(919) 878-8111
OHIO,	
Columbus (Westerville)	(614) 891-6455
Dayton	(513) 439-0268
OREGON	(503) 245-0080
PENNSYLVANIA	(215) 398-8006
TEXAS,	
Austin	(512) 346-7830
Dallas	(214) 934-9099
Houston	(713) 376-8084

International

BELGIUM, Antwerpen	TEL	(03) 248 43 00
	FAX	(03) 248 46 42
FRANCE, Paris	TEL	(1) 49-75-10-10
	FAX	(1) 49-75-10-13
GERMANY,		
Bad Homburg	TEL	(06172)-24061
	FAX	(06172)-23195
München	TEL	(089) 4114-0
	FAX	(089) 406490
HONG KONG,	TEL	(852) 865-4525
Wanchai	FAX	(852) 865-1147
ITALY, Milano	TEL	(02) 3390541
	FAX	(02) 38103458
JAPAN,		
Atsugi	TEL	(0462) 29-8460
	FAX	(0462) 29-8458
Kanagawa	TEL	(0462) 47-2911
	FAX	(0462) 47-1729
Tokyo	TEL	(03) 3346-7550
	FAX	(03) 3342-5196
Osaka	TEL	(06) 243-3250
	FAX	(06) 243-3253
KOREA, Seoul	TEL	(82) 2-784-7598
	FAX	(82) 2-784-8014
LATIN AMERICA,		
Ft. Lauderdale	TEL	(305) 484-8600
	FAX	(305) 485-9736
SINGAPORE	TEL	(65) 3481188
	FAX	(65) 3480161
SWEDEN,		
Stockholm area	TEL	(08) 98 61 80
(Bromma)	FAX	(08) 98 09 06
TAIWAN, Taipei	TEL	(886) 2-7153536
	FAX	(886) 2-7122183
UNITED KINGDOM,		
Manchester area	TEL	(0925) 828008
(Warrington)	FAX	(0925) 827693
London area	TEL	(0483) 740440
(Woking)	FAX	(0483) 756196

North American Representatives

CANADA
Burnaby, B.C. – DAVETEK MARKETING ..... (604) 430-3680
Kanata, Ontario – VITEL ELECTRONICS ..... (613) 592-0060
Mississauga, Ontario – VITEL ELECTRONICS . (416) 564-9720
Lachine, Quebec – VITEL ELECTRONICS ..... (514) 636-5951

ILLINOIS
Skokie – INDUSTRIAL REPRESENTATIVES,INC ..... (708) 967-8430

INDIANA
Huntington – ELECTRONIC MARKETING CONSULTANTS, INC ..... (317) 921-3450
Indianapolis – ELECTRONIC MARKETING CONSULTANTS, INC ..... (317) 921-3450

IOWA
LORENZ SALES ..... (319) 377-4666

KANSAS
Merriam – LORENZ SALES ..... (913) 469-1312
Wichita – LORENZ SALES ..... (316) 721-0500

KENTUCKY
ELECTRONIC MARKETING CONSULTANTS, INC ..... (317) 921-3452

MICHIGAN
Holland – COM-TEK SALES, INC ..... (616) 335-8418
Brighton – COM-TEK SALES, INC ..... (313) 227-0007

MINNESOTA
Mel Foster Tech. Sales, Inc. ..... (612) 941-9790

MISSOURI
LORENZ SALES ..... (314) 997-4558

NEBRASKA
LORENZ SALES ..... (402) 475-4660

NEW MEXICO
THORSON DESERT STATES ..... (505) 883-4343

NEW YORK
East Syracuse – NYCOM, INC ..... (315) 437-8343
Hauppauge – COMPONENT CONSULTANTS, INC ..... (516) 273-5050

OHIO
Centerville – DOLFUSS ROOT & CO ..... (513) 433-6776
Columbus – DOLFUSS ROOT & CO ..... (614) 885-4844
Westlake – DOLFUSS ROOT & CO ..... (216) 899-9370

OREGON
ELECTRA TECHNICAL SALES, INC ..... (503) 643-5074

PENNSYLVANIA
RUSSELL F. CLARK CO.,INC. ..... (412) 242-9500

PUERTO RICO
COMP REP ASSOC, INC ..... (809) 746-6550

WASHINGTON
ELECTRA TECHNICAL SALES ..... (206) 821-7442

WISCONSIN
Brookfield – INDUSTRIAL REPRESENTATIVES,INC ..... (414) 789-9393

UTAH
Front Range Marketing ..... (801) 264-2500

Advanced Micro Devices, Inc. 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088, USA
Tel: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450
APPLICATIONS HOTLINE & LITERATURE ORDERING • TOLL FREE: (800) 222-9323 • (408) 749-5703

8/3/92
Printed in USA

ADVANCED
MICRO
DEVICES, INC.
901 Thompson Place
P.O. Box 3453
Sunnyvale
California 94088-3453
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306
TOLL-FREE
(800) 538-8450

APPLICATIONS HOTLINE &
LITERATURE ORDERING
(800) 222-9323
(408) 749-5703

RECYCLED &
RECYCLABLE

Printed in USA
BAN-56.5M-8/92-0
11796B