Advanced Micro Devices

Condensed Catalog

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Printed in U.S.A. 1-81 AMD-599

INTRODUCTION

This condensed catalog is a quick reference source for all Advanced Micro Devices' integrated circuits and board-level products. It contains three basic types of information – numerical product listing, short-form data and general reference material.

Section 1 – Product Index
Lists device types, general product category and the page, line item number and data location. Listings show only the base number with the various prefixes stripped away for clarity. For example, LM101 is listed as a 101; SN54LS01 is listed as 54LS01. An exception has been made for the Z8000/Z8100 series products which are shown following the 8000 and 8100 numbers, respectively. Other manufacturers' device numbers, with a cross reference to the appropriate AMD device type, are shown in italic type in numerical sequence.

Sections 2 through 6 – Product Data
Includes data that may be tabular, a brief functional description or a list of product features. Block or connection diagrams are included where appropriate. In many product listings, codes are shown for temperature range and package types. These codes are defined as follows:

Temperature Range
C = Commercial (0 to +70°C)
M = Military (−55 to +125°C)
L = Limited Military (−55 to +85°C)

Package Codes
D = Hermetic DIP
F = Flatpack
H = Metal Can (TO-5 type)
N = Plastic DIP
P = Plastic DIP
Z = Leadless Chip Carrier

Section 7 – Military, Hi-Rel and Product Assurance
Describes standard product testing and assurance procedures and includes quality conformance levels and screening flow tables.

Section 8 – Sales Office, Representatives and Distributor Locations
Lists addresses, telephone and TWX/telex number.

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*Functional equivalent

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The Am2900 Bipolar Microprocessor Family offers a full line of LSI and support products optimized for high performance CPU and controller applications.

The devices use Schottky and low-power Schottky process technologies to implement LSI functions of up to 750 gates per chip. Newer techniques are in development to achieve complexities of up to 3000 gates.

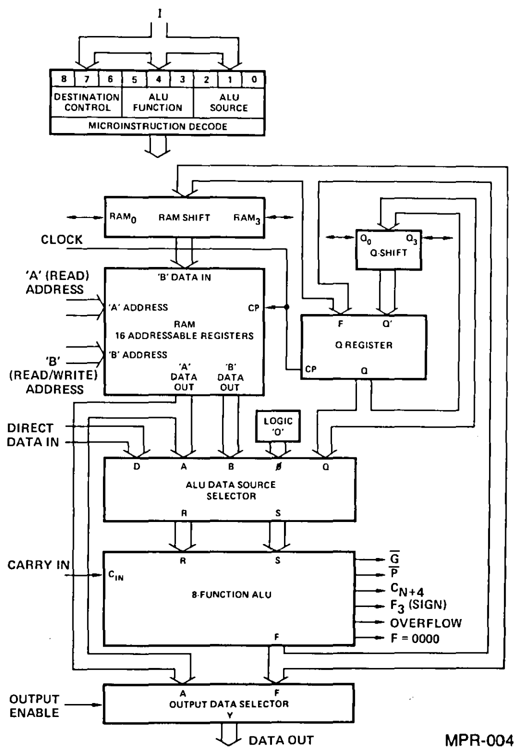
The LSI members of the Am2900 family represent new kinds of building blocks for designers of high performance systems. They may be considered as a third generation of TTL functions (the first generation being SSI and the second MSI). At this level of complexity each part is specialized for a particular section of the system, such as the arithmetic unit or memory control. Many lower complexity support devices have been added to the family. Each one has been carefully selected to provide optimum interface between the LSI blocks, minimizing package count and delay.

Since the introduction of the Am2901 in 1975, new circuit design and process techniques have been applied to improve the speed and reduce the power requirements of successive generations of elements. These improved designs are designated by alpha suffixes to the device type number.

2

Am2901B 4-Bit Bipolar Microprocessor Slice

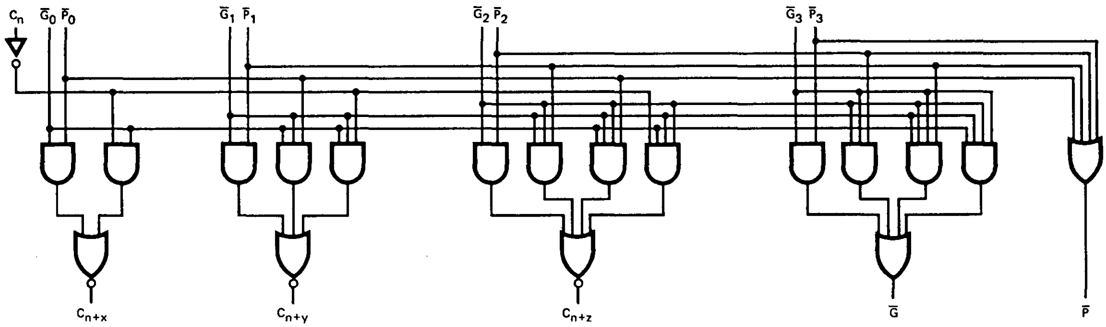
- 2-Address Architecture
  Independent simultaneous access to two working registers saves machine cycles
- 8-Function ALU
  Performs addition, two subtraction operations and five logic functions on two source operands
- Flexible Data Source Selection
  ALU data selected from five source ports
  203 source operand pairs for every ALU function
- Left/Right Shift Independent of ALU
  Add and shift operations take only one cycle
- Four Status Flags
  Carry, overflow, zero and negative
- Expandable
  Connect any number of Am2901s together for longer word lengths
- Microprogrammable
  Three groups of three bits each for source operand, ALU function and destination control
- Fast
  115ns for 16-bit addition
  Am2901C targeted to be 25% faster
- 40-Pin DIP



MPR-004

Am2902A High-Speed Lookahead Carry Generator

- Provides Lookahead Carries across a Group of Four Am2901B or Am2903 Microprocessor ALUs
- Capable of Multilevel Lookahead for High-Speed Arithmetic Operation over Large Word Lengths
- Carry Propagation Delay – 4.5ns (Typ)
- C_{IN} to C_{OUT} – 7.0ns (Typ)
- 16-Pin DIP



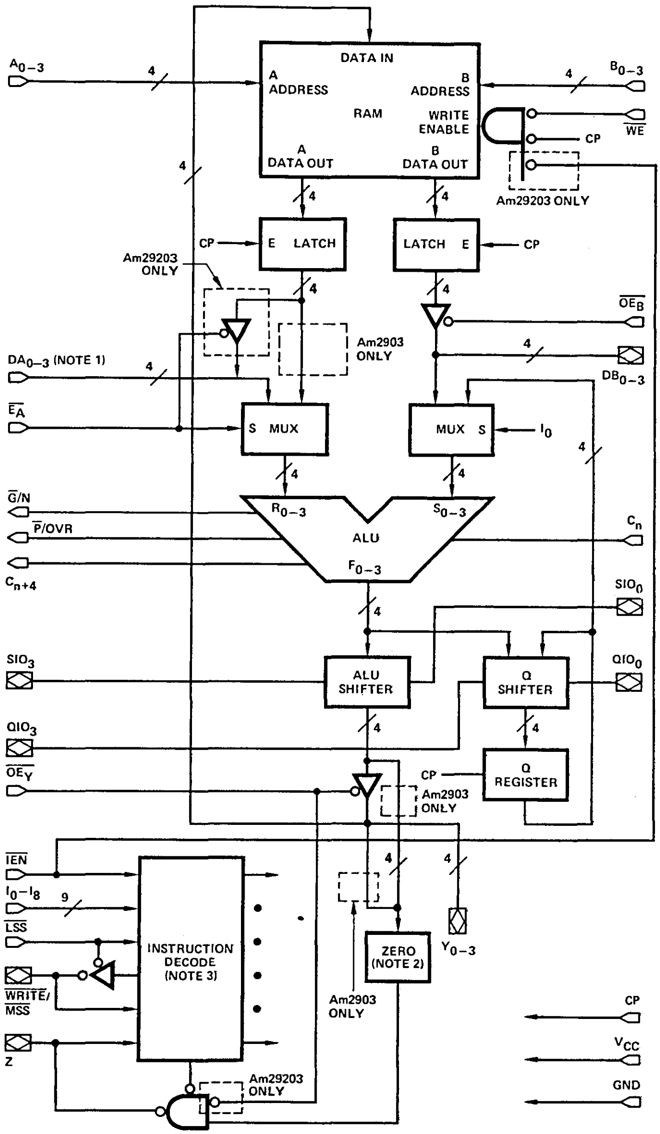
MPR-026

Am2903/Am29203 Superslice®

- Expandable Register File
  Like the Am2901B, the Am2903/Am29203 contains 16 internal working registers arranged in a 2-address architecture. But the Am2903/Am29203 includes the necessary "hooks" to expand the register file externally to any number of registers.
- Built-in Normalization Logic
  Performing multiplication with the Am2901B requires a few external gates; these gates are contained on-chip in the Am2903/Am29203. Three special instructions are used for unsigned multiplication, twos complement multiplication and the last cycle of a twos complement multiplication.
- Built-in Division Logic
  The Am2903/Am29203 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- Built-in Normalization Logic
  The Am2903/Am29203 can simultaneously shift the Q Register and count in a working register. Thus, the mantissa and exponent of a floating-point number can be developed using a single microcycle per shift. Status flags indicate when the operation is complete.
- Built-in Parity Generation Circuitry
  The Am2903/Am29203 can supply parity across the entire ALU output for use in error detection.
- Built-in Sign Extension Circuitry
  To facilitate operation on different length twos complement numbers, the Am2903/Am29203 provides the capability to extend the sign at any slice boundary.
- BCD Arithmetic (Am29203 only)
  Automatic BCD add and subtract and conversion between binary and BCD.
- Improved Byte Handling (Am29203 only)
  Zero detection and register writing can be performed on a single byte rather than the whole word.
- Two Bidirectional Data Lines (Am29203 only)
- Fast
  174ns for 16-bit addition; Am2903A is targeted to be 30% faster.
- 48-Pin DIP

2

Am2903/Am29203 Superslice® (Cont.)

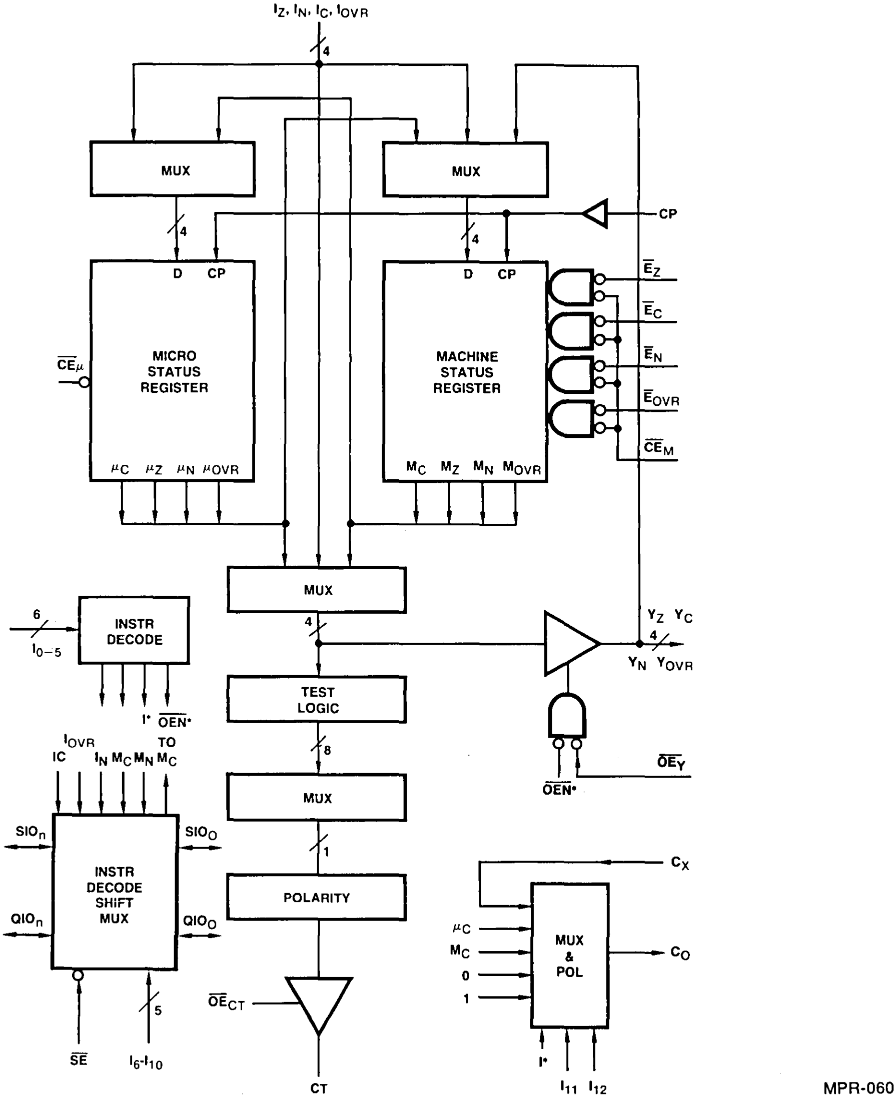


Notes: 1. DA_{0-3} is input only on Am2903, but is I/O port on Am29203.
2. On Am2903, zero logic is connected to Y, after the $\overline{OE}_Y$ buffer.

MPR-030

Am2904 Status and Shift Control Unit

- Replaces Most MSI Used around any ALU (including the Am2901B, Am2903 and MSI ALUs)
- Generates Carry-in to the ALU
  Carry signal selectable from seven different sources
- Contains Shift Linkage Multiplexers
  Connects to shift lines at the ends of an Am2901B or Am2903 array to implement single and double length arithmetic and logical shifts
  Rotates 32 different modes
- Contains Two Edge-Triggered Status Registers
  Use for foreground/background registers in controllers or as microlevel and machine level status registers
  Bit manipulating instructions provided
- Condition Code Multiplexer On-Chip
  Single cycle tests for any of 16 different conditions
  Tests performed on either of the two status registers or directly on the ALU output
- 40-Pin DIP



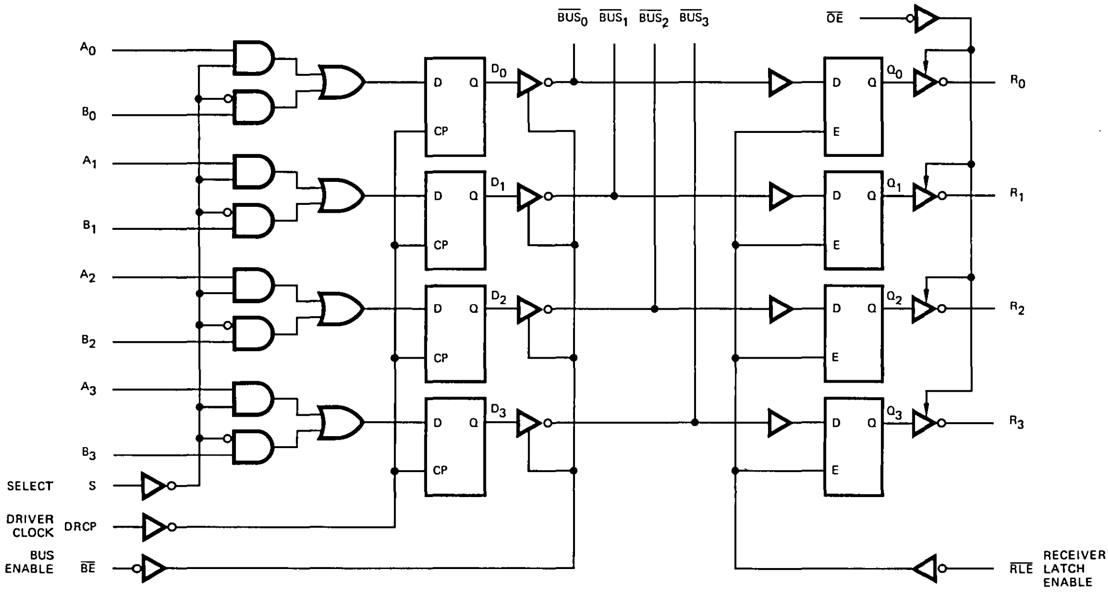
Am2905 Quad 2-Input OC Bus Transceiver (with 3-State Receiver)

- Quad High-Speed LSI Bus Transceiver
- Open-Collector Bus Driver
- 2-Port Input to D-Type Register on Driver
- Bus Driver Output Sinks 100mA at 0.8V (Max)
- Driver Clock to Bus in 21ns (Typ)
- Receiver Has Output Latch for Pipeline Operation
- 3-State Receiver Outputs Sink 12mA
- 24-Pin DIP

Am2906 Quad 2-Input OC Bus Transceiver (with Parity)

- Quad High-Speed LSI Bus Transceiver
- Open-Collector Bus Driver
- 2-Port Input to D-Type Register on Driver
- Bus Driver Output Sinks 100mA at 0.8V (Max)
- Internal Odd 4-Bit Parity Checker/Generator
- Driver Clock to Bus in 21ns (Typ)
- Receiver Has Output Latch for Pipeline Operation
- Receiver Outputs Sink 12mA
- 24-Pin DIP

Am2905*

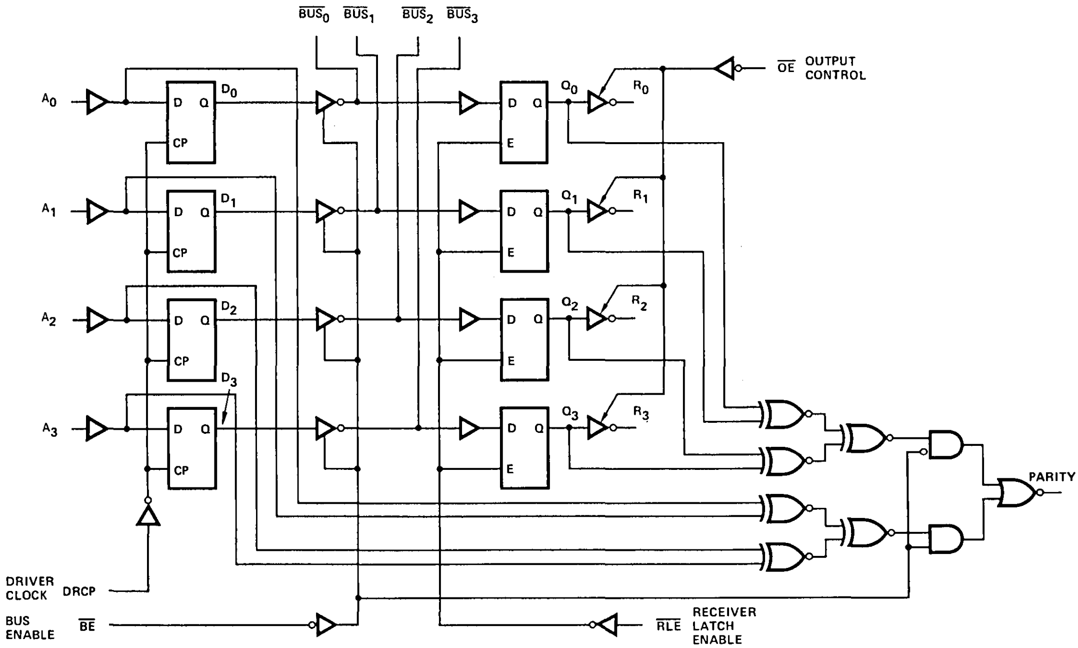


MPR-065

*Am2906 logic diagram is similar to Am2905 except the $\overline{OE}$ input is replaced with a parity output.

Am2907/Am2908 Quad Bus Transceivers (with Interface Logic)

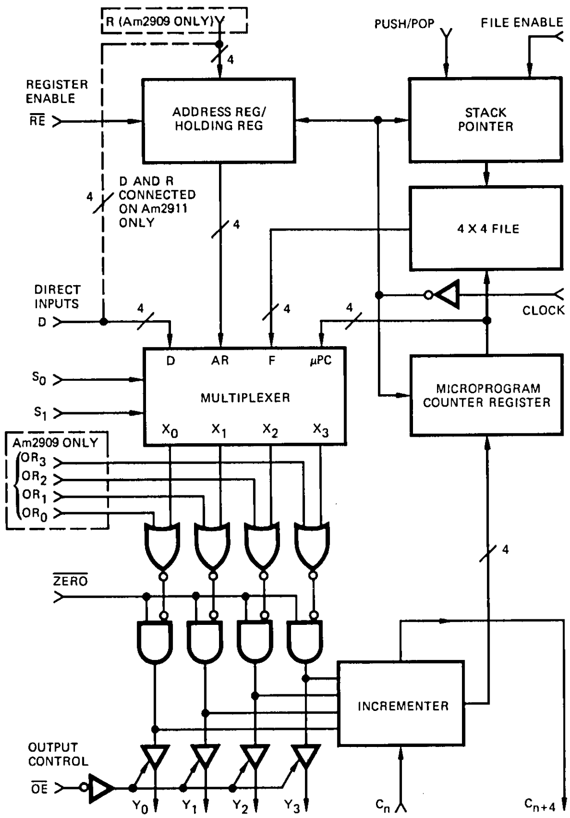
- Quad High-Speed LSI Bus Transceiver
- Open-Collector Bus Driver
- D-Type Register on Driver
- Bus Driver Output Sinks 100mA at 0.8V (Max)
- Internal Odd 4-Bit Parity Checker/Generator
- Input Receiver Threshold Voltage
  2.0V for Am2907
  1.5V for Am2908 (DEC Q or LSI-11 Bus Compatible)
- Driver Clock to Bus in 21ns (Typ)
- Receiver Has Output Latch for Pipeline Operation
- 3-State Receiver Outputs Sink 12mA
- 20-Pin DIP



MPR-085

Am2909/Am2911, Am2909A/Am2911A
4-Bit Microprogram Sequencers

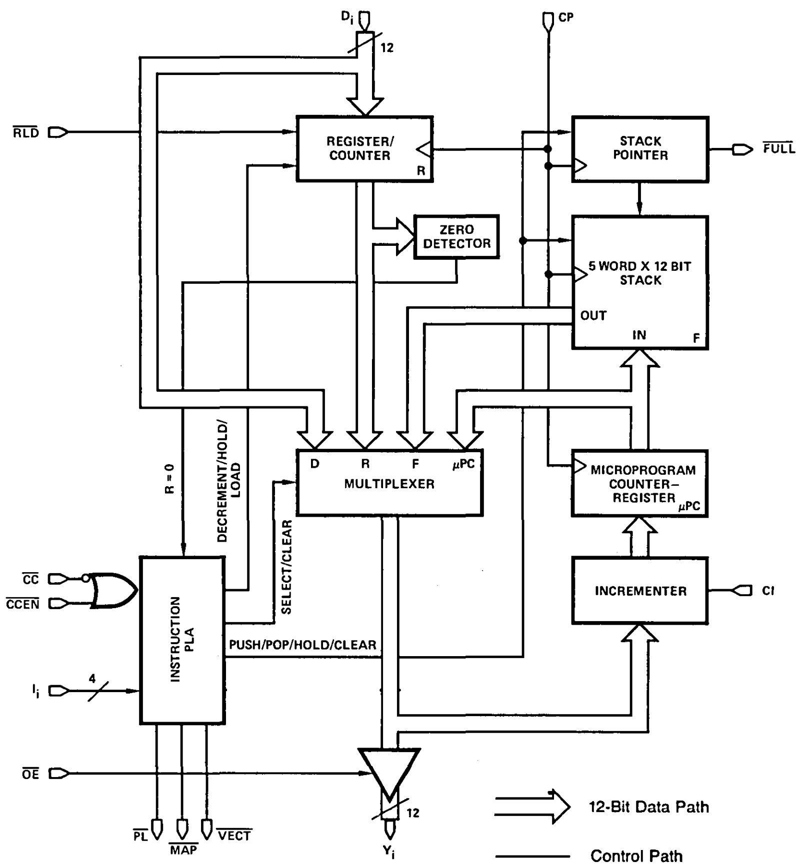
- 4-Bit Slice Cascadable to any Number of Microwords
- Internal Address Register
- Branch Input for N-Way Branches
- Cascadable 4-Bit Microprogram Counter
- 4 x 4 File with Stack Pointer and Push/Pop Control for Nesting Microsubroutines
- Zero Input for Returning to the Zero Microcode Word
- Individual OR Input for each Bit for Branching to Higher Microinstructions (Am2909/Am2909A only)
- 3-State Outputs
- All Internal Registers Change State on the LOW-to-HIGH transition of the Clock
- High-Speed Versions (Am2909A and Am2911A) are Plug-in Replacements for Am2909 and Am2911 Critical Path Speeds Improved by about 25%
- 177ns (Max) for Conditional Jump Sequence (includes delay through PROM and registers)
- Am2909/Am2909A in 28-Pin DIP
- Am2911/Am2911A in 20-Pin DIP



MPR-093

Am2910 12-Bit Microprogram Controller

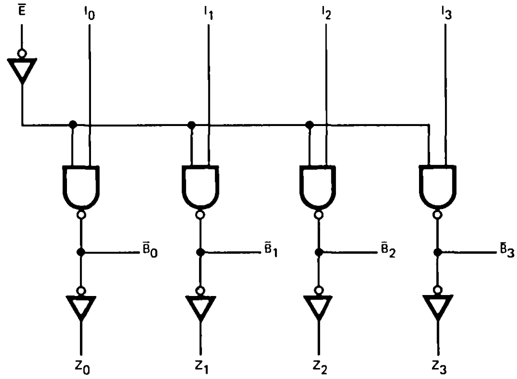
- 12 Bits Wide
  Address up to 4096 words of microcode with one chip
  All internal elements a full 12 bits wide
- Internal Loop Counter
  Presettable 12-bit down-counter for repeating instructions and counting loop iterations
- Four Address Sources
  Microprogram Address can be selected from microprogram counter, branch address bus, 5-level push/pop stack or internal holding register
- 16 Powerful Microinstructions
  Executes 16 sequence control instructions, most conditional on external condition input and/or state of internal loop counter
- Output Enable Controls for Three Branch-Address Sources
  Built-in decoder function enables external devices onto branch address bus, eliminates external decoder
- All Registers Positive Edge-Triggered
  Simplifies timing problems
  Eliminates long set-up times
- Fast Control from Condition Input
  Delay from condition code input to address output 21ns (Typ)
- 166ns (Max) for Conditional Jump Sequence (includes delay through PROM and registers)
- 40-Pin DIP



MPR-106

Am2912 Quad Bus Transceiver

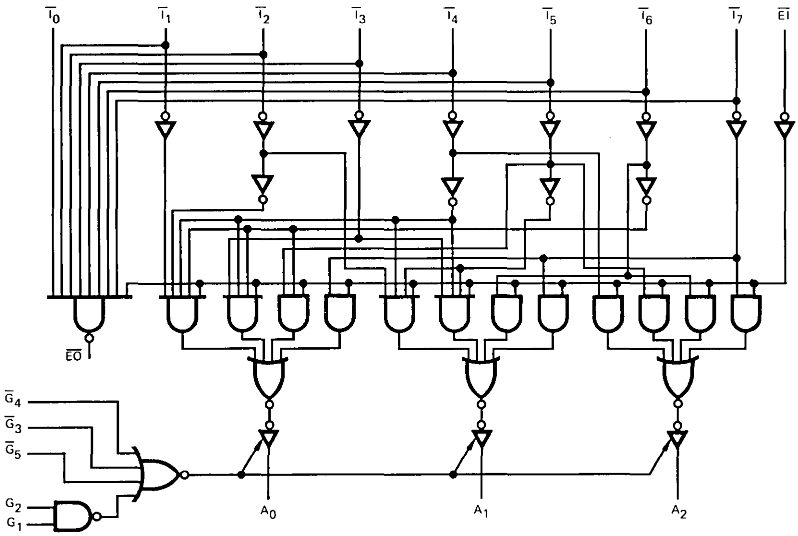
- Input to Bus Is Inverting
- Quad High-Speed Open-Collector Bus Transceiver
- Driver Outputs Sink 100mA at 0.8V (Max)
- Bus Compatible with Am2905, Am2906, Am2907
- Enable to Bus in 14ns (Typ)
- PNP Inputs to Reduce Input Loading
- 16-Pin DIP



BLI-061

Am2913 Priority Interrupt Expander

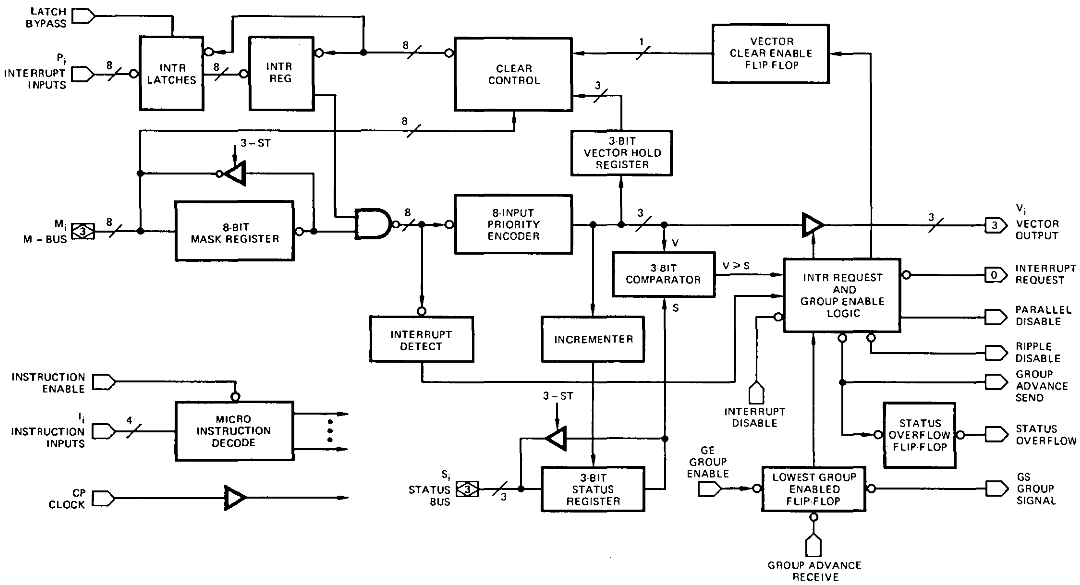
- Encodes Eight Lines to 3-Line Binary
- Expands Use of Am2914
- Cascadable
- Input to Output in 17ns (Typ)
- Gated 3-State Output
- 20-Pin DIP



MPR-119

Am2914 Vectored Priority Interrupt Controller

- Accepts Eight Interrupt Inputs
  Pulse or level interrupts
  Interrupts stored internally
- Built-in Mask Register
  Six different operations performed on mask register
- Built-in Status Register
  Holds code for lowest allowed interrupt
- Vectored Output
  Output is binary code for highest priority unmasked interrupt
- Expandable
  Any number of Am2914s can be stacked for large interrupt systems
- Microprogrammable
  Executes 16 different microinstructions
  Instruction enable pin aids in vertical microprogramming
- High-Speed Operation
  Delay from interrupt clocked into interrupt register to interrupt request output 97ns (Typ)
- 40-Pin DIP



MPR-124

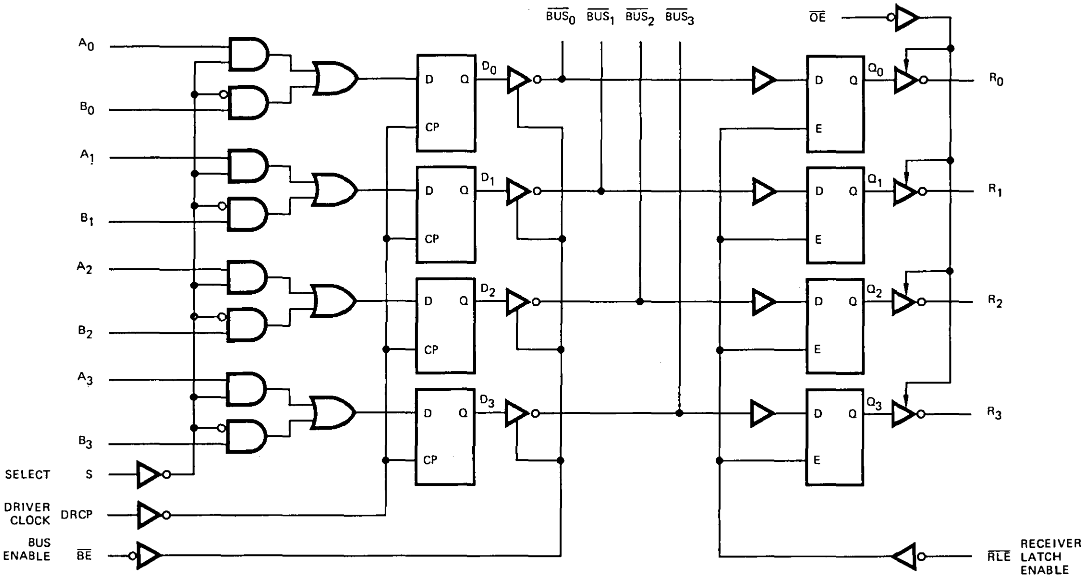
Am2915A Quad 3-State Bus Transceiver (with Interface Logic)

- Quad High-Speed LSI Bus Transceiver
- 3-State Bus Driver
- 2-Port Input to D-Type Register on Driver
- Bus Driver Output Sinks 48mA at 0.5V (Max)
- Receiver Has Output Latch for Pipeline Operation
- Driver Clock to Bus in 21ns (Typ)
- 3-State Receiver Outputs Sink 12mA
- V_{OH} = 3.5V (Min) for Direct MOS Microprocessor Interface
- 24-Pin DIP

Am2916A Quad 3-State Bus Transceiver (with Interface Logic)

- Quad High-Speed LSI Bus Transceiver
- 3-State Bus Driver
- 2-Port Input to D-Type Register on Driver
- Bus Driver Output Sinks 48mA at 0.5V (Max)
- Internal Odd 4-Bit Parity Checker/Generator
- Receiver Has Output Latch for Pipeline Operation
- Driver Clock to Bus in 21ns (Typ)
- Receiver Outputs Sink 12mA
- V_{OH} = 3.5V (Min) for Direct MOS Microprocessor Interface
- 24-Pin DIP

Am2915A*

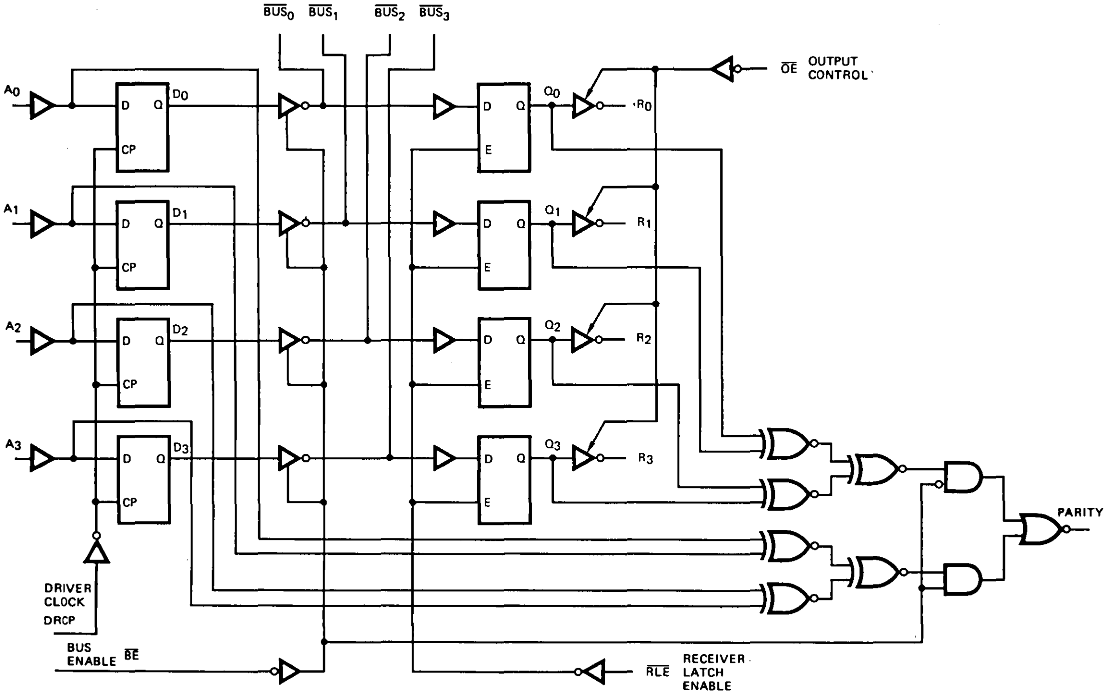


*Am2916A logic diagram is similar to Am2915A except that $\overline{OE}$ input is replaced by parity output.

MPR-161

Am2917A Quad 3-State Bus Transceiver (with Interface Logic)

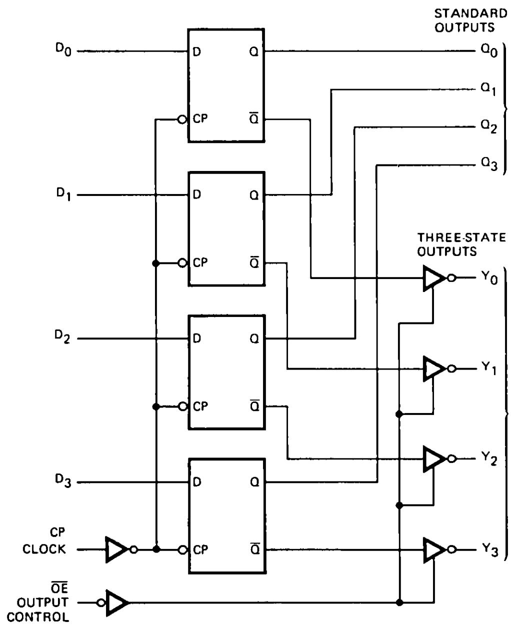
- Quad High-Speed LSI Bus Transceiver
- 3-State Bus Driver
- D-Type Register on Driver
- Bus Driver Output Sinks 48mA at 0.5V (Max)
- Internal Odd 4-Bit Parity Checker/Generator
- Receiver Has Output Latch for Pipeline Operation
- Driver Clock to Bus in 21ns (Typ)
- 3-State Receiver Outputs Sink 12mA
- V_{OH} = 3.5V (Min) for Direct MOS Microprocessor Interface
- 20-Pin DIP



MPR-177

Am2918/Am29LS18 Quad D Registers (with Standard and 3-State Outputs)

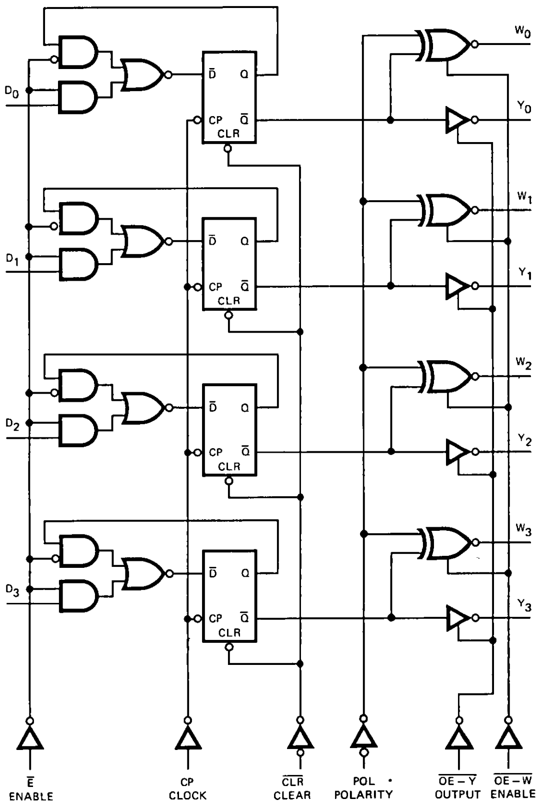
- Four D-Type Flip-Flops
- Four Standard Totem-Pole Outputs
- Four 3-State Outputs
- Clock to Output Time (Typ)
  8.5ns for Am2918
  18ns for Am29LS18
- 16-Pin DIP



MPR-183

Am2919 Quad Register (with Dual 3-State Outputs)

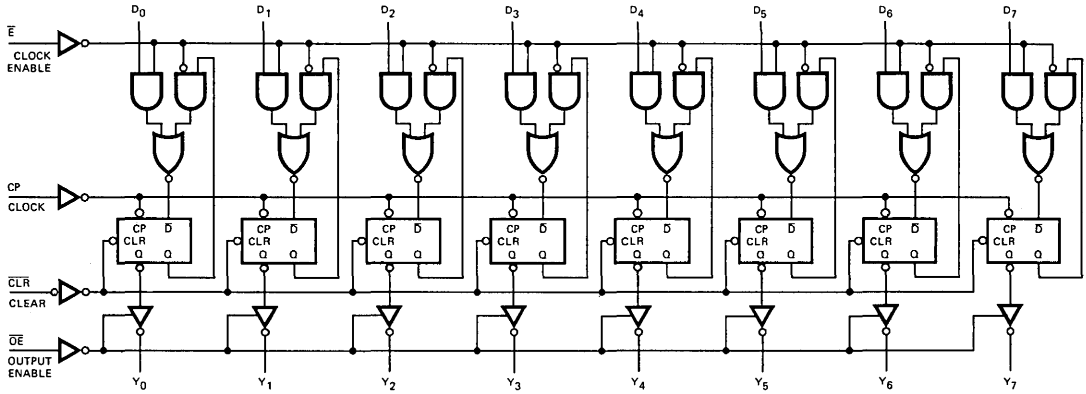
- Two Sets of 3-State Outputs
- Four D-Type Flip-Flops
- Polarity Control on One Set of Outputs
- Buffered Common Clock Enable
- Buffered Common Asynchronous Clear
- Separate Buffered Common Output Enable for each Set of Outputs
- Clock to Output in 22ns (Typ)
- 20-Pin DIP



MPR-196

Am2920 Octal D-Type Flip-Flop
(with Clear, Clock Enable and 3-State Control)

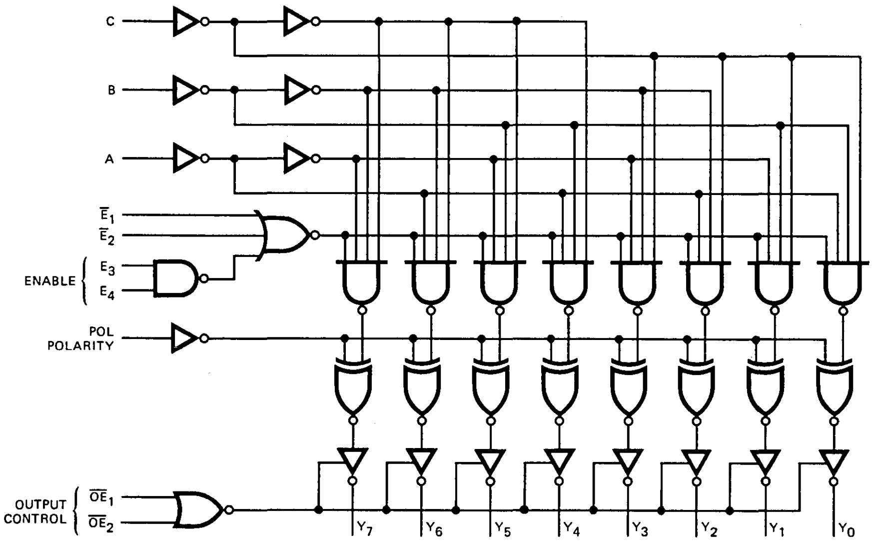
- Buffered Common Clock Enable Input
- Buffered Common Asynchronous Clear Input
- 3-State Outputs
- 8-Bit High-Speed Parallel Register with Positive Edge-Triggered, D-Type Flip-Flops
- Clock to Output in 24ns (Typ)
- 22-Pin DIP



MPR-201

Am2921 One-of-Eight Decoder
(with 3-State Outputs and Polarity Control)

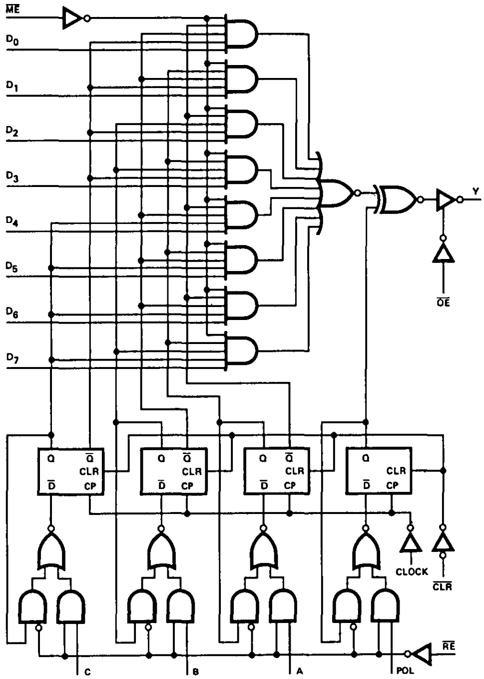
- 3-State Decoder Outputs
- Buffered Common Output Polarity Control
- Inverting and Non-inverting Enable Inputs
- Input to Output in 20ns (Typ)
- 20-Pin DIP



MPR-207

Am2922 8-Input Multiplexer (with Control Register)

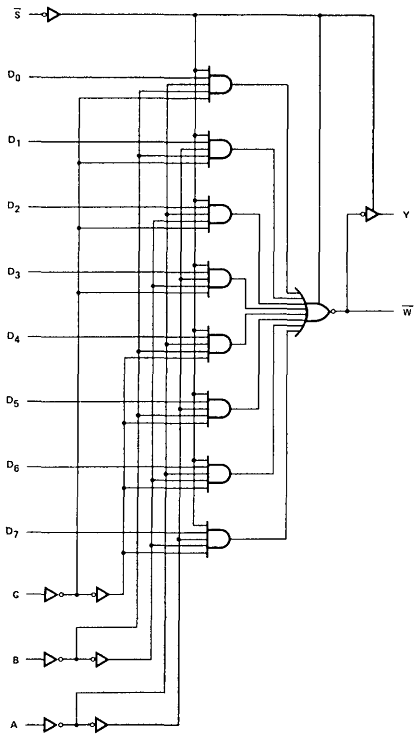
- High-Speed 8-Input Multiplexer
- On-Chip Multiplexer Select and Polarity Control Register
- Output Polarity Control for Inverting or Non-inverting Output
- Common Register Enable
- Asynchronous Register Clear
- 3-State Output for Expansion
- Clock to Output in 21ns (Typ)
- 20-Pin DIP



MPR-213

Am2923 8-Input Multiplexer

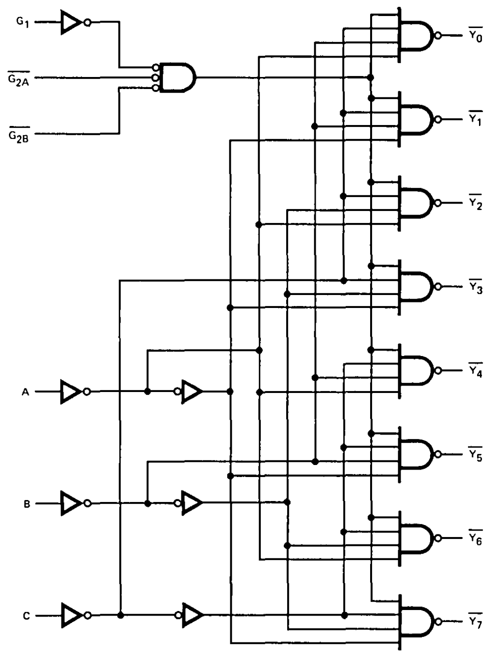
- Switches One of Eight Inputs to Two Complementary Outputs
- Input to Output in 13ns (Typ)
- 3-State Output for Bus Organized Systems
- 16-Pin DIP



BLI-069

Am2924 3-Line to 8-Line Decoder/Demultiplexer

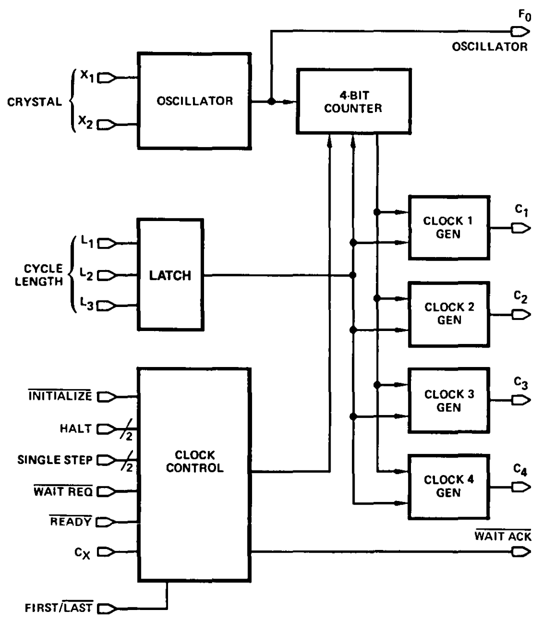
- Inverting and Non-inverting Enable Inputs
- Select to Output in 8.0ns (Typ)
- 16-Pin DIP



BLI-075

Am2925 System Clock Generator and Driver

- Single-Chip Clock Generator and Driver
- Four Different Clock Output Waveforms for Am2900 and Other Bipolar and MOS Systems
- Crystal Controlled for Stable System Operation
- Oscillator to 31MHz
  Oscillator output for external system timing
- Clock Halt, Single-Step and Wait Controls
- Variable Cycle Lengths
  One of eight different cycle lengths can be microprogrammed to boost CPU throughput up to 25%
- Slim 0.3" 24-Pin DIP

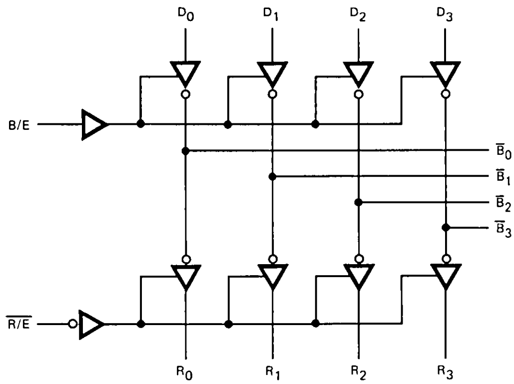


MPR-217

Am2926/Am2929 Schottky 3-State Quad Bus Driver/Receiver

- 48mA Driver Sink Current
- 3-State Outputs on Driver and Receiver
- PNP Inputs
- Am2926 Has Inverting Outputs
- Am2929 Has Non-inverting Outputs
- Driver/Receiver Propagation Delay (Typ)
  10ns for Am2926
  13ns for Am2929
- 16-Pin DIP

Am2926*



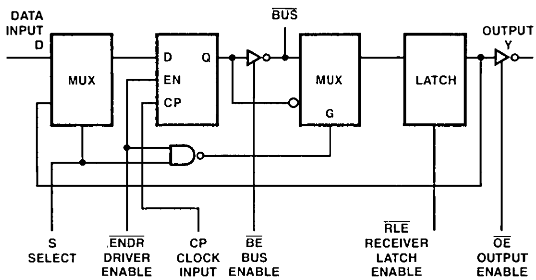
*Outputs B_0-B_3 are not inverted for Am2929.

BLI-080

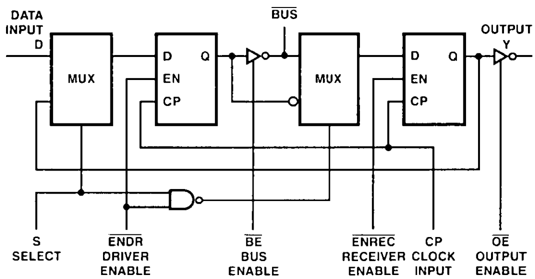
Am2927/Am2928 Quad 3-State Bus Transceivers (with Clock Enable)

- Quad High-Speed LSI Bus Transceivers
- 3-State Bus Driver and Receiver Outputs
- D-Type Register on Drivers
- Latched Output on Am2927
- Registered Output on Am2928
- Output Data to Input Wraparound Gating
- Input Register to Output Transfer Gating with or without Driving Data Bus
- Clock Enabled Registers
- Bus Driver Outputs Sink 48mA at 0.5V (Max)
- 3-State Receiver Outputs Sink 20mA at 0.5V (Max)
- V_{OH} = 3.5V (Min) for Direct MOS Microprocessor Interface
- 20-Pin DIP

Am2927



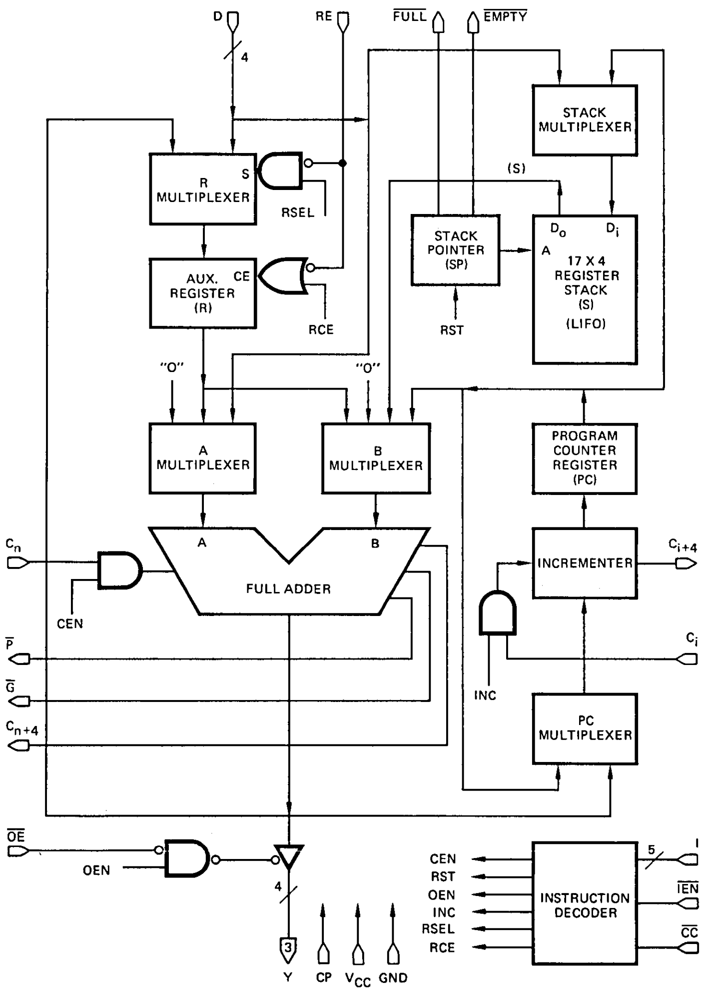
Am2928



BLI-088

Am2930 Program Control Unit

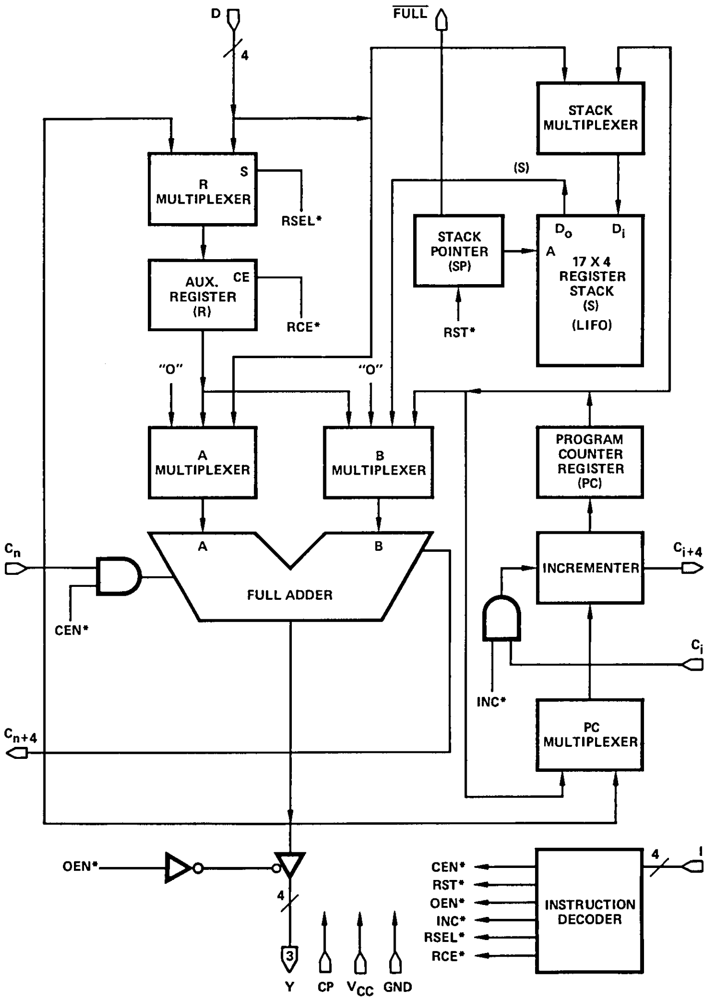
- Powerful 4-Bit Slice Address Controller
  Useful with both main memory and microprogram memory
- Executes 32 Instructions
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- Contains Cascadable Full Adder
  12 different relative address instructions are provided including jump-to-subroutine and return-from-subroutine
- Built-in Condition Code Input
  16 instructions are dependent on external condition control
- 17-Level Push/Pop Stack
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- Separate Incrementer for Program Counter
  Relative address can be computed and PC can be incremented by one on a single cycle
- 28-Pin DIP



MPR-221

Am2932 Program Control Unit, Push/Pop Stack

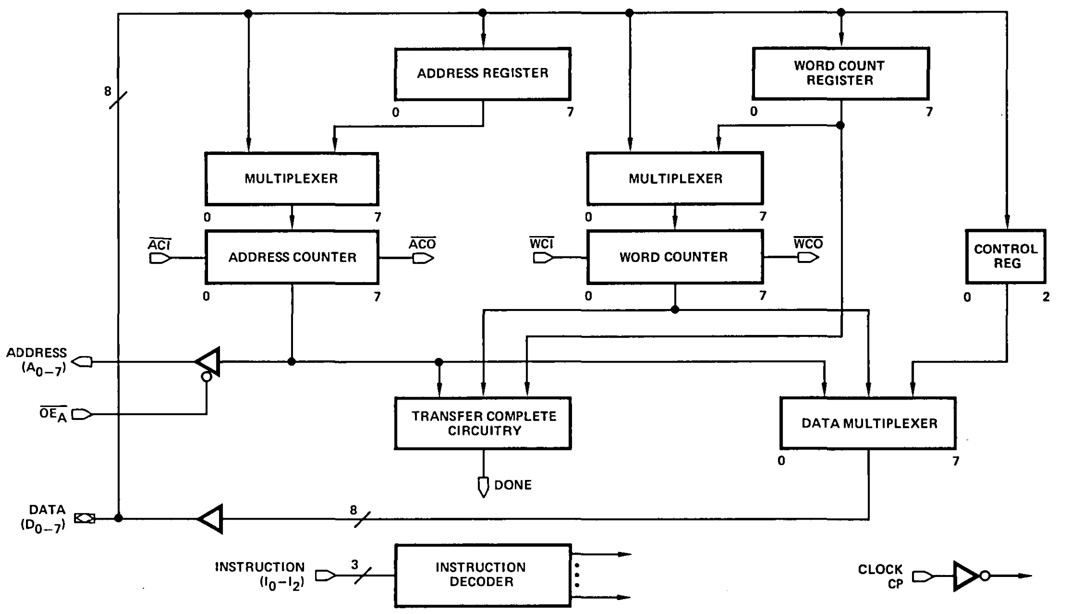
- Powerful, 4-Bit Slice Address Controller
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- Executes 16 Instructions
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- Contains Cascadable Full Adder
  Eight relative address instructions are provided including jump and jump-to-subroutine relative
- 17-Level Push/Pop Stack
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- Separate Incrementer for Program Counter
  Relative address can be computed and PC can be incremented by one on a single cycle
- 20-Pin DIP



BLI-095

Am2940 DMA Address Generator

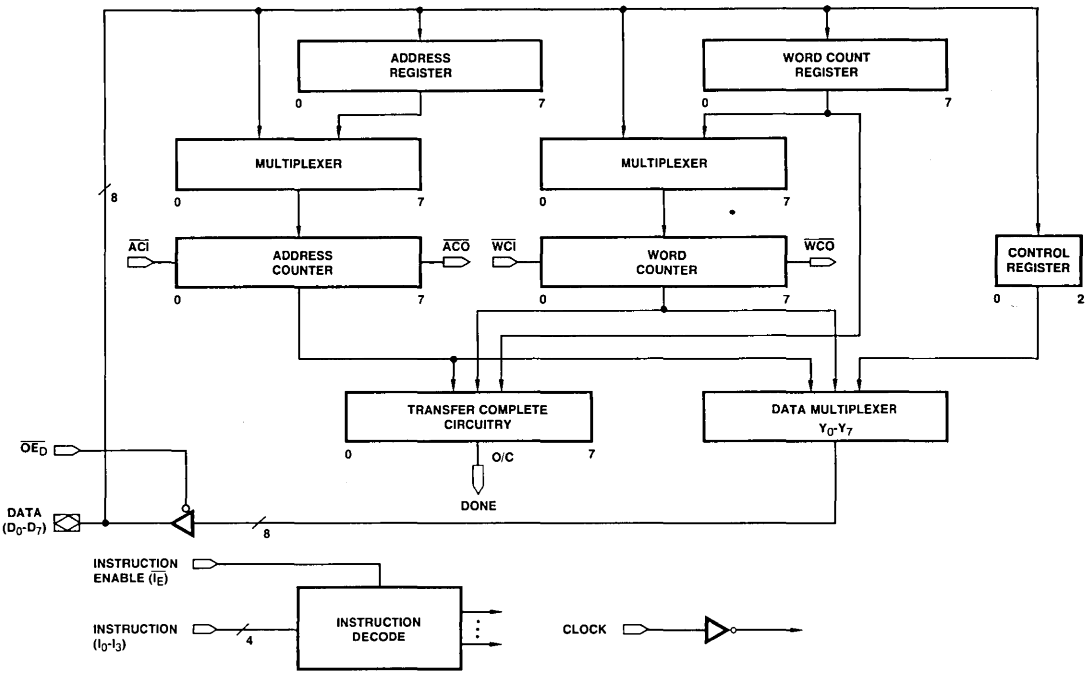
- DMA Address Generation
  Generates memory address, word count and DONE signal for DMA transfer operation
- Expandable 8-Bit Slice
  Any number of Am2940s can be cascaded to form larger memory addresses
  Three devices address 16 megawords
- Repeat Data Transfer Capability
  Initial memory address and word count saved so data transfer can be repeated
- Programmable Control Modes
  Provides four types of DMA transfer control plus memory address increment/decrement
- 24mA Output Current Sink Capability
- Microprogrammable
  Executes eight different instructions
- 109ns (Max) Cycle Time for 16-Bit Configuration
  Allows up to nine million words/second DMA
- 28-Pin DIP



MPR-226

Am2942 Programmable Timer/Counter, DMA Address Generator

- 22-Pin Version of Am2940
  Provides multiplexed address and data lines plus additional instruction input and instruction enable pins
- Used as DMA Address Generator or Programmable Timer Counter
- Executes 16 Instructions
  Eight DMA instructions
  Eight Timer/Counter instructions
- Provides Two Independent Programmable 8-Bit Up/Down Counters
  Counters can be cascaded to form single-chip 16-bit up/down counter
- Reinitialize Capability
  Counters reinitialized from on-chip registers
- Expandable 8-Bit Slice
  Any number of Am2942s can be cascaded
  Three devices provide a 48-bit counter
- Programmable Control Modes
  Four types of control
- 24mA Output Current Sink Capability
- 109ns (Max) Cycle Time for 16-Bit Configuration
- 22-Pin DIP

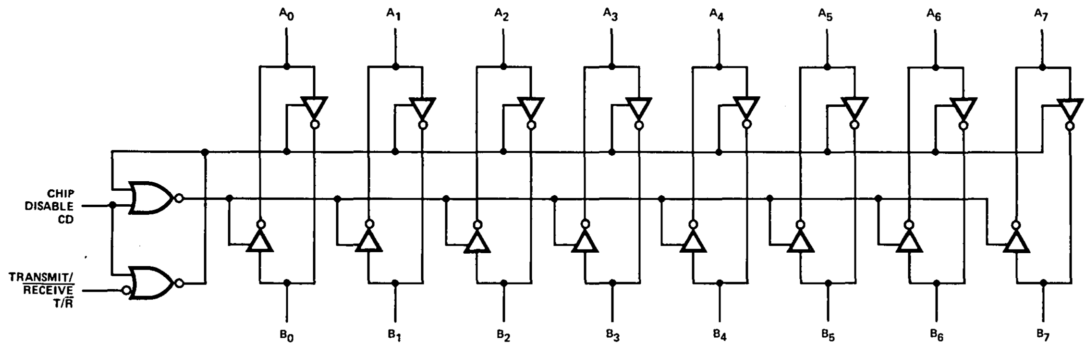


MPR-231

Am2946/Am2947 Octal 3-State Bidirectional Bus Transceivers

- 8-Bit Bidirectional Data Flow Reduces System Package Count
- 3-State Inputs/Outputs for Bus-Oriented System Interface
- PNP Inputs Reduce Input Loading
- $V_{OH} = V_{CC} - 1.15V$ for TTL, MOS, CMOS Interface
- 48mA, 300pF Bus Drive Capability
- Am2946 Has Inverting Transceivers
- Am2947 Has Non-inverting Transceivers
- Transmit/$\overline{\text{Receive}}$ and Chip Disable Simplify Control Logic
- Low-Power
  8.0mA per bidirectional bit
- Bus Port Stays in High-Impedance State during Power Up/Down
- A Port to B Port Delay Time – 11ns (Typ)
- 20-Pin DIP

Am2946*



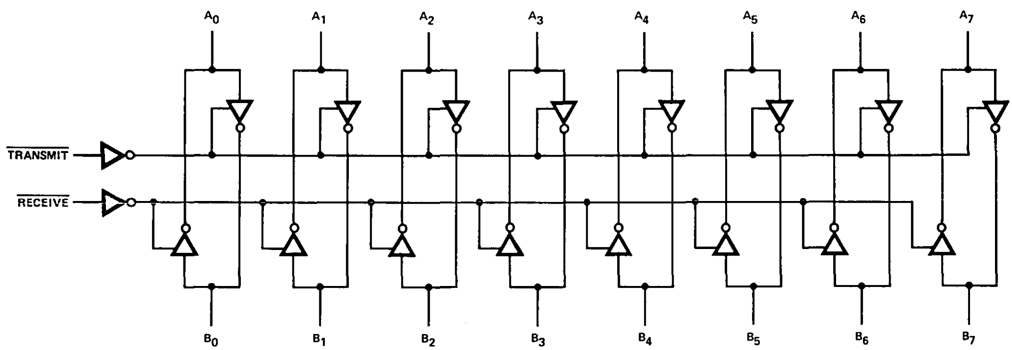
*Am2947 has non-inverting transceivers.

BLI-101

Am2948/Am2949 Octal 3-State Bidirectional Bus Transceivers

- 8-Bit Bidirectional Data Flow Reduces System Package Count
- 3-State Inputs/Outputs for Bus-Oriented System Interface
- PNP Inputs Reduce Input Loading
- $V_{OH} = V_{CC} - 1.15V$ for TTL, MOS, CMOS Interface
- 48mA, 300pF Bus Drive Capability
- Am2948 Has Inverting Transceivers
- Am2949 Has Non-inverting Transceivers
- Separate $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ Enables
- Low-Power
  8.0mA per bidirectional bit
- Bus Port Stays in High-Impedance State during Power Up/Down
- 20-Pin DIP

Am2949*



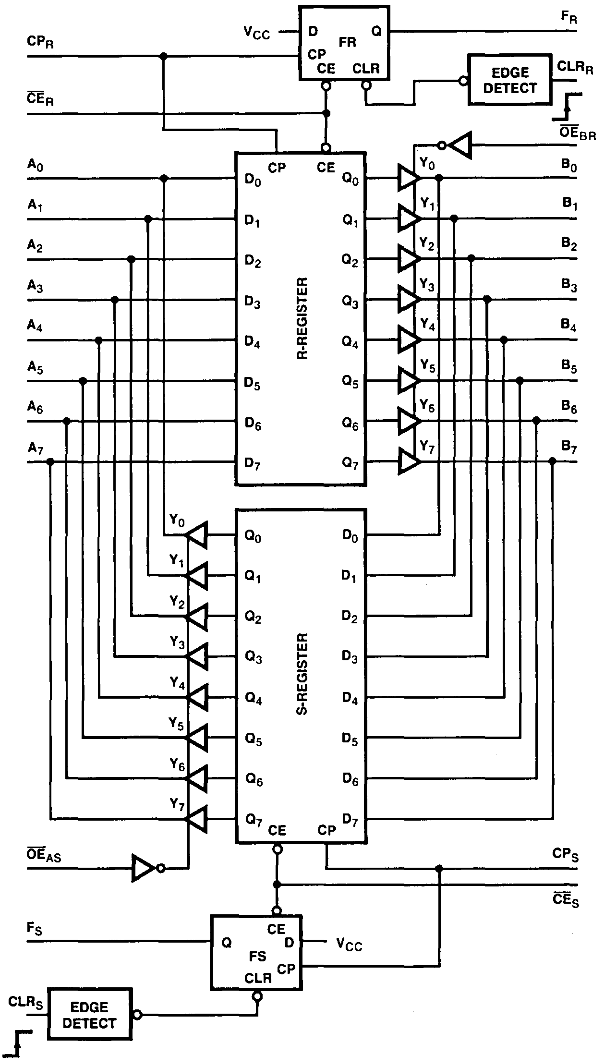
*Am2948 has inverting transceivers.

BLI-107

Am2950/Am2951 8-Bit Bidirectional I/O Ports

- 8-Bit, Bidirectional I/O Port with Handshake
  Two 8-bit, back-to-back registers store data moving in both directions between two bidirectional busses
- Register Full/Empty
  On-chip flag flip-flops provide data transfer handshaking signals
- Separate Clock, Clock Enable and 3-State Output Enable for each Register
- Separate, Edge-Sensitive Clear Control for each Flag Flip-Flop
- Inverting and Non-inverting Versions
  Am2950 provides non-inverting data outputs
  Am2951 provides inverting data outputs
- 24mA Output Current Sink Capability
- 20ns Clock to Flag, 27ns (Max) for Output Enable
  Allows up to 8 million words/second data transfer rate
- 28-Pin DIP

Am2950*



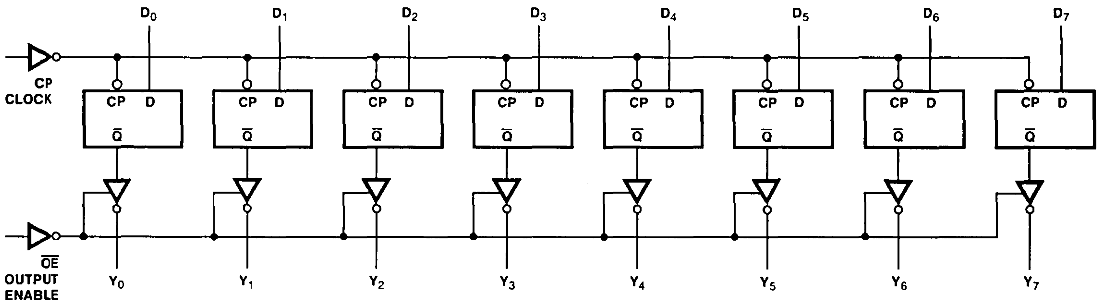
*Outputs B_0-B_7 are inverted on the Am2951.

MPR-573

Am2954/Am2955 Octal Registers (with 3-State Outputs)

- 8-Bit High-Speed Parallel Registers
- Am2954 Has Non-inverting Inputs
- Am2955 Has Inverting Inputs
- Positive Edge-Triggered D-Type Flip-Flops
- Buffered Common 3-State Control and Clock
- V_{OL} = 0.5V (Max) at I_{OL} = 32mA
- Clock to Output 11ns (Typ)
- 20-Pin DIP

Am2954*



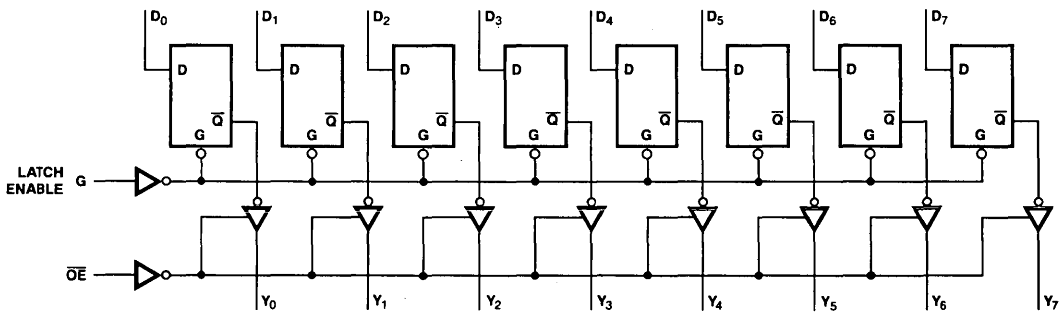
*Inputs D_0 through D_7 are inverted on the Am2955.

BLI-110

Am2956/Am2957 Octal Latches (with 3-State Outputs)

- Eight Latches in a Single Package
- Am2956 Has Non-inverting Outputs
- Am2957 Has Inverting Outputs
- V_{OL} = 0.5V (Max) at I_{OL} = 32mA
- 3-State Outputs for Bus-Oriented System Interface
- Hysteresis on Latch Enable Input for Improved Noise Margin
- Clock to Output 12ns (Typ)
- 20-Pin DIP

Am2956*



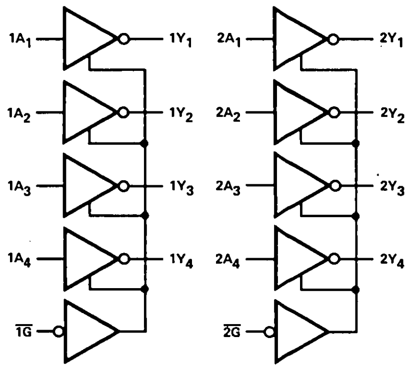
*Inputs D_0 through D_7 are inverted on the Am2957.

MPR-360

Am2958/Am2959 Octal Buffers/Line Drivers/Line Receivers (with 3-State Outputs)

- 3-State Outputs Drive Bus Lines Directly
- Hysteresis at Inputs Improve Noise Margin
- PNP Inputs Reduce dc Loading on Bus Lines
- $V_{OL} = 0.55V$
  at $I_{OL} = 65mA$ for commercial product
  at $I_{OL} = 48mA$ for military product
- Data-to-Output Propagation Delay
  Am2958 Inverting – 4.5ns (Max)
  Am2959 Non-inverting – 6.0ns (Max)
- Enable-to-Output 15ns (Max)
- 20-Pin DIP

Am2958*



*Outputs Y_1 through Y_4 are not inverted on the Am2959.

BLI-115

Am29112 Interruptable 8-Bit Microprogram Sequencer

- Fast
  Designed to operate in 10MHz microprogrammed systems
- Expandable
  One Am29112 directly addresses up to 256 words of microcode
  Two Am29112s can directly address up to 64K words of microcode
- Interruptable at Microcycle Completion
  Internal states saved on the stack
  Branches automatically to the interrupt service routine
- Many Addressing Modes
  Immediate, relative and n-way addressing
- 31-Level Stack
  On-chip 31-level stack used for subroutines, interrupts and loops
- Single or Double Pipeline
- 40-Pin DIP

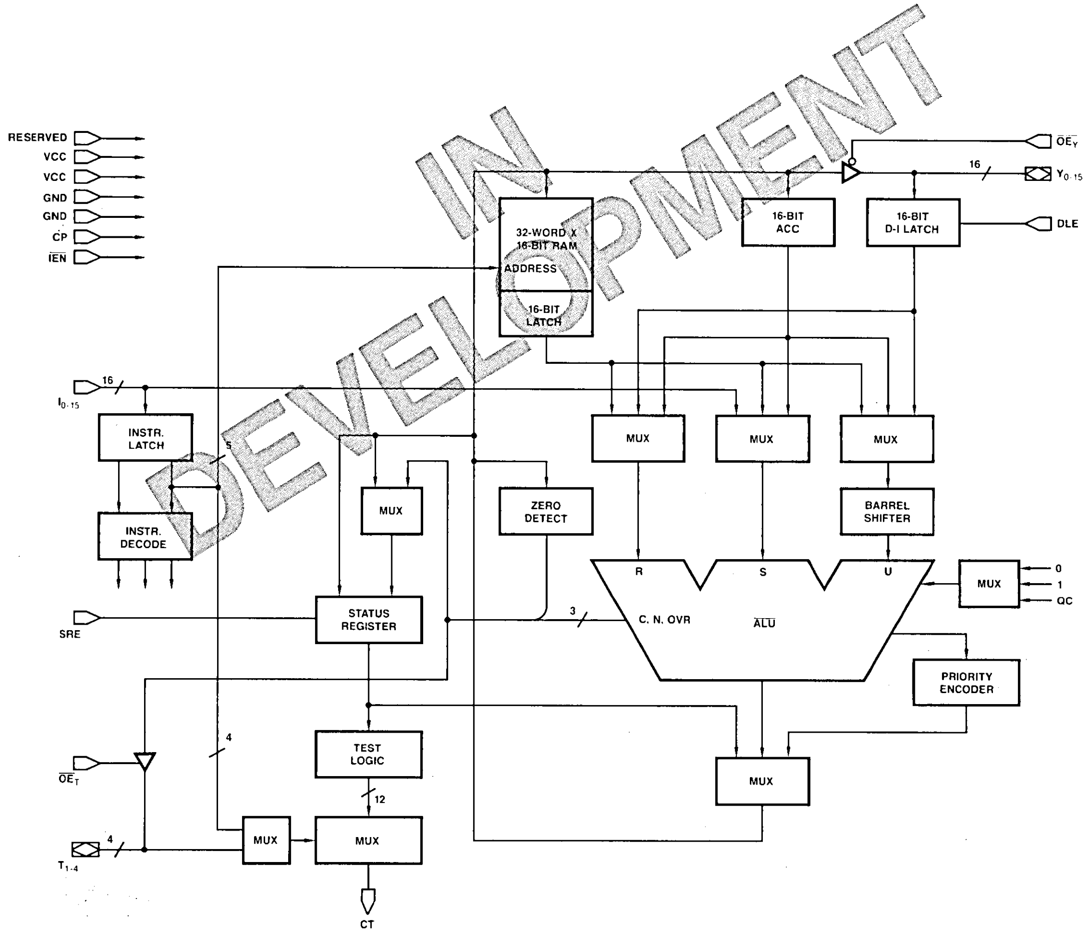
IN DEVELOPMENT

Am29116 16-Bit Bipolar Microprocessor

- Designed for Controller Applications
  Instruction set designed for high performance peripheral controllers, communications controllers, industrial controllers and digital modems . . . but general purpose too.
  Excellent solution for applications requiring speed and bit-manipulation power
- Fast
  Design objective of 100ns (Max) microcycle time for all instructions
  Allows a 10MHz clock rate
- Powerful Instruction Set
  All instructions executable in single cycle on full 16-bit word or on 8-bit byte:

Add, Subtract	Rotate and Merge
n-Bit Rotate	Rotate and Compare
Shift-Up/Shift-Down	CRC Generation
Set-Bit/Reset-Bit	Priority Encode
Add/Subtract 2^n	

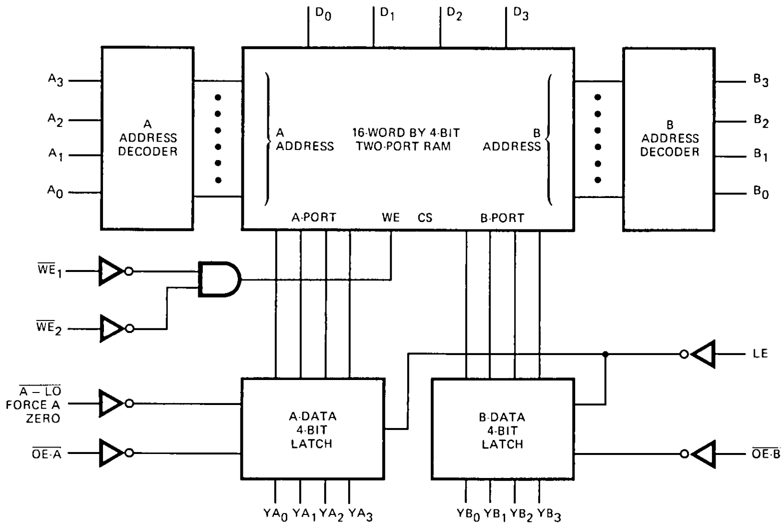
- Powerful Data Manipulation
  Full 16-bit data path
  32 registers on-chip
  Direct data input for immediate mode instructions
- 52-Pin DIP



MPR-740

Am29705 16-Word by 4-Bit 2-Port RAM

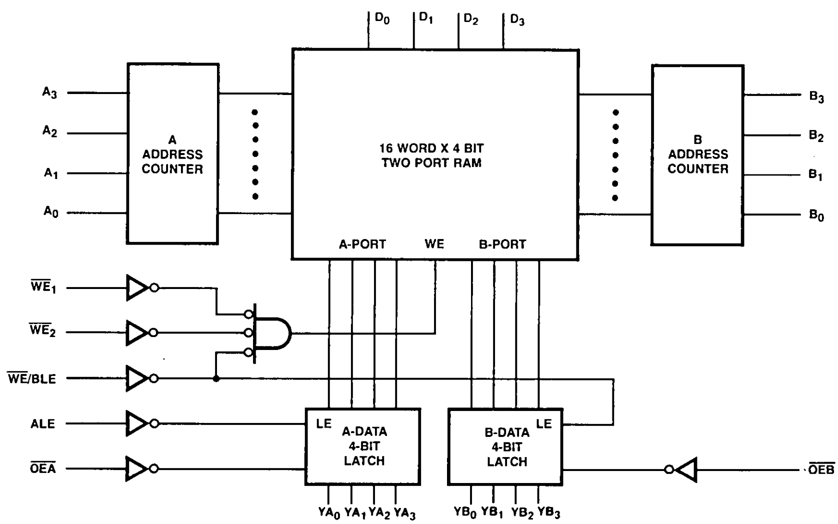
- 16 Word x 4-Bit 2-Port RAM
- Two Output Ports
  Each with separate output control
  Separate 4-bit latches on each
- Data Output Non-inverting with Respect to Data Input
- Chip Select and Write Enable Inputs for Ease in Cascading
- 53ns (Max) Access Time
- 28-Pin DIP



MPR-251

Am29707 16-Word by 4-Bit 2-Port RAM

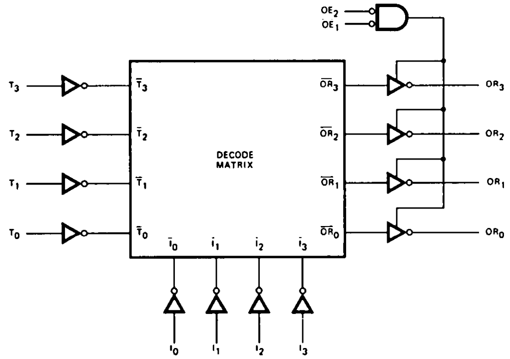
- 16-Word by 4-Bit 2-Port RAM
- Use to Extend the Directly Accessible Register File of the Am29203 Microprocessor Slice
- Separate 4-Bit Latches on each Output Port
- Data Output Non-inverting with Respect to Data Input
- Chip Select and Write Enable Inputs for Ease in Cascading
- 28-Pin DIP



MPR-757

Am29803A 16-Way Branch Control Unit

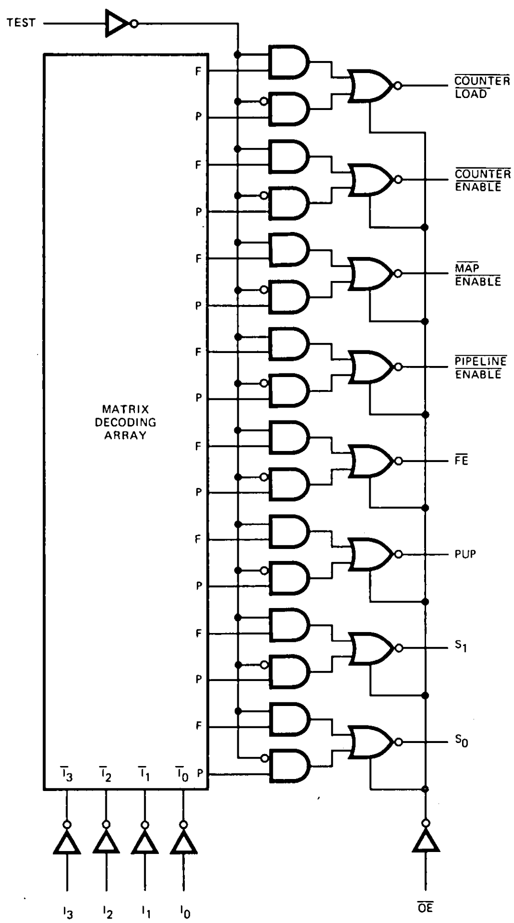
- 16 Separate Instructions
  2, 4, 8 or 16-way branch in one microprogram execution cycle
- Four Individual Test Inputs
- Four Individual Outputs for Driving the Four OR Inputs on Am2909 Microprogram Sequencer
- Provides Maximum Branch Capability in a Microprogram Control Unit Using Am2909
- 16-Pin DIP



MPR-309

Am29811A Next Address Control Unit

- Next Address Control Unit for Am2911 Microprogram Sequencer
- 16 Next Address Instructions
- Test Input for Conditional Instructions
- Separate Outputs to Control Am2911
- Independent Event Counter
- Mapping PROM/Branch Address Interface
- 16-Pin DIP



MPR-314

OTHER LOGIC DEVICES FOR HIGH-SPEED PROCESSOR APPLICATIONS

Operators	Low-Power Schottky	Schottky
4-Bit, 4-Way Shifter		Am25S10
4-Bit ALU, Function Generator (with carry out, overflow)	Am25LS2517	
4-Bit ALU, Function Generator (with generate, propagate)	Am25LS381*	
8-Bit, Equal-to Comparator	Am25LS2521	
Priority Encoder (with 3-state outputs)	Am25LS2513	
Decoders/Demultiplexers, Multiplexers		
1-of-10 Decoder/Demultiplexer (with polarity control)	Am25LS2537	
1-of-8 Decoder/Demultiplexer (with control storage)	Am25LS2536	
1-of-8 Decoder/Demultiplexer (with polarity control)	Am25LS2538	
1-of-8 Chip Select Address Decoder	Am25LS2548	
Dual 1-of-4 Decoder/Demultiplexer (with polarity control)	Am25LS2539	
8-Input Multiplexer (with control storage)	Am25LS2535	
Registers		
4-Bit Register (with common clock enable)	Am25LS08	Am25S08
4-Bit Register (with 2-input multiplexers on inputs)	Am25LS09	Am25S09
4-Bit Register (with standard and 3-state outputs)	Am25LS2518	Am25S18
4-Bit, 2-Output 3-State Register	Am25LS2519	
6-Bit Register (with common clock enable)	Am25LS07	Am25S07
8-Bit Shift/Storage Register (with synchronous clear)	Am25LS23	
8-Bit Shift/Storage Register (with asynchronous clear)	Am25LS299*	
8-Bit Shift/Storage Register (with sign extend)	Am25LS22	
Octal D-Type Register (with common clear)	Am25LS273*	
Octal D-Type Register (with common clear, buffered outputs)	Am25LS273B	
Octal Transparent Latch (with 3-state outputs)	Am25LS373*	Am25S373*
Octal Transparent Latch (with inverting 3-state outputs)	Am25LS533*	Am25S533*
Octal D-Type Register (with 3-state outputs)	Am25LS374*	Am25S374*
Octal D-Type Register (with inverting 3-state outputs)	Am25LS534*	Am25S534*
Octal D-Type Register (with common enable)	Am25LS377*	
Octal D-Type Register (with common enable, buffered outputs)	Am25LS377B	
Octal D-Type Register (with common enable and clear, 3-state outputs)	Am25LS2520	
Counters		
BDC Decade Counter (with asynchronous clear)		93S10 54/74S160
Up-Down Decade Counter (with synchronous preset, 3-state outputs)	Am25LS2568	
Binary Counter (with asynchronous clear)		93S16 54/74S161
Up-Down Binary Counter (with synchronous preset, 3-state outputs)	Am25LS2569	
Parity Checker/Generator		
9-Input Parity Checker/Generator		82S62
12-Input Parity Checker/Generator		93S48

Items indicated * are also available as SN54/74LS numbered functions.

DESIGN AIDS

AmSYS™29 Microprogram Development System

The AmSYS™29 is a complete development system for microprogrammed machines. It is a useful tool for designing initial hardware/firmware, for assembling and debugging microcode and for checking out hardware.

AmSYS™29 includes a CP/M compatible operating system 1K x 64-bit words of high-speed Writable Control Store and high-speed Emulation Control Logic. The options and peripherals offer a high-speed trace, line printer, PROM programmer interface and CRT console.

Features:

- AMDASM meta-assembler language definition and source file assembly
- High-Speed Emulator integrating bipolar logic and microde
- High-Speed Writable Control Store
- Optional 10-MHz High-Speed Microcode Trace
- AMDOS®29 CP/M compatible disk operating system
- Dual single-density floppy disk drives upgradable to double density

Am2900 Learning and Evaluation Kit

The Am2900 Learning and Evaluation Kit provides a stripped-down model of a typical microprogrammed controller or computer for introducing engineers to the architecture of microprogrammed systems.

It contains a small but powerful microprogrammed control unit driving several data handling elements including an Am2901B 4-bit CPU slice. The microprogram memory in the kit is a read/write memory so that sequences of microinstructions can be entered by the user, then executed. The data control portion of each microinstruction controls all inputs to the Am2901B, shift and rotate logic and a status register that captures ALU conditions following each cycle. Each microinstruction also contains a 4-bit sequence control field, which is used to select one of 16 different sequence control instructions and a branch address. The instructions are decoded in a PROM that controls an Am2909 microprogram sequencer. Once entered, microinstructions may be executed using a single-step clock or a pulse generator.

The Am2900 Learning and Evaluation Kit includes 40 integrated circuits, 26 resistors, 16 capacitors, 15 switches, 12 LEDs and the PC board. The only item not supplied is a 5V, 2A power supply. Also included is the user's manual, a 114-page book containing chapters on the theory of microprogramming, the assembly and testing of the kit and exercises that demonstrate the application of the architecture and operation of the Am2901B and Am2909.

Bit-Slice Microprocessor Design

This 384-page book is invaluable as a learning tool or reference manual. Authored by AMD, the text discusses in detail the design of a microprogrammed computer using the Am2900 Family. Application examples are used extensively and theory is pared to essentials. Chapters include:

I – Computer Architecture
II – Microprogrammed Design
III – The Data Path
IV – The Data Path, Part Two
V – Program Control Unit
VI – Interrupt
VII – Direct Memory Access
VIII – The HEX-29 Single-Board Computer
IX – The Super Sixteen Single-Board Computers

Bit-Slice Microprocessor Design by J. Mick and J. Brick, ISBN 0-07-041781-4, may be obtained from your local bookstore or ordered directly from McGraw-Hill Book Co., Suite 26-1, 1221 Avenue of Americas, New York, NY 10020.

AMD School of Advanced Engineering

The AMD School of Advanced Engineering offers three courses for the Am2900 Family designer: Introduction to Designing with the Am2900 Family, Microprogrammable Computer Architecture and Introduction to Design with a Development System. Comprehensive course notes are available without course attendance for a fee of $175.00/set. For more information regarding course content, schedule or fees, or to order course notes, please contact:

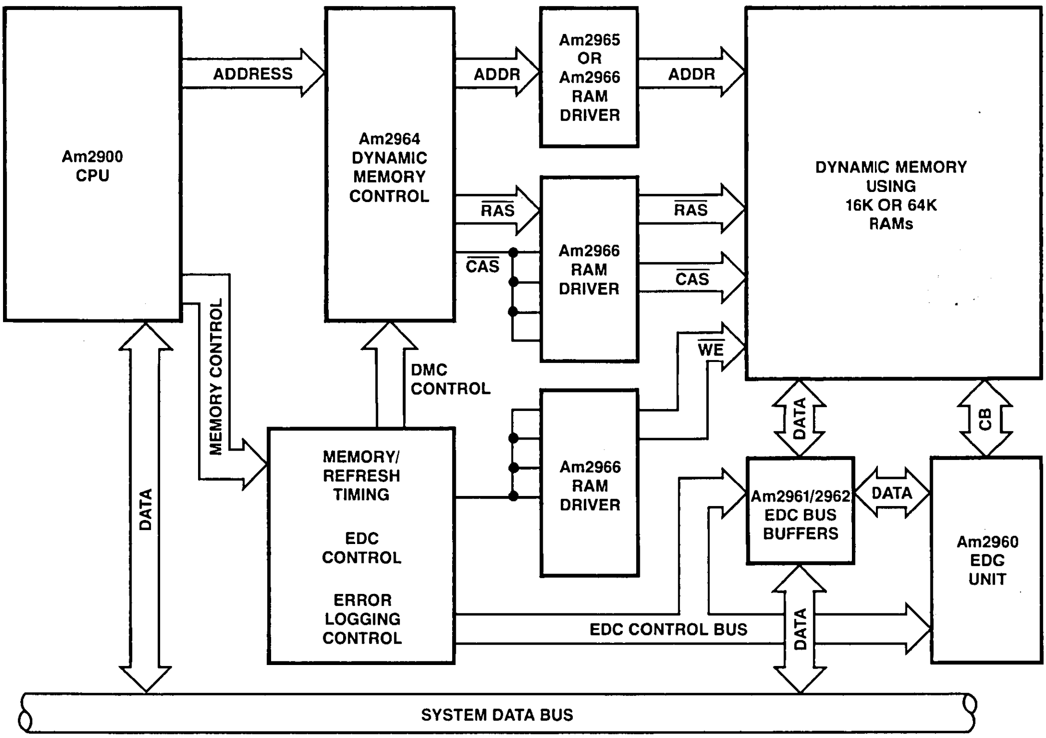
AMD School of Advanced Engineering
430 Lakeside Drive
Sunnyvale, CA 94086
408/732-2400 Ext. 2325

Dynamic Memory Support Products

Advanced Micro Devices has developed a set of memory support products to maximize the speed and reliability of systems using dynamic MOS RAM storage.

These devices provide in the minimum package count all of the logic, interface and control functions required in the address and data paths of memory systems based on 16K and 64K RAMs. See the block diagram below.

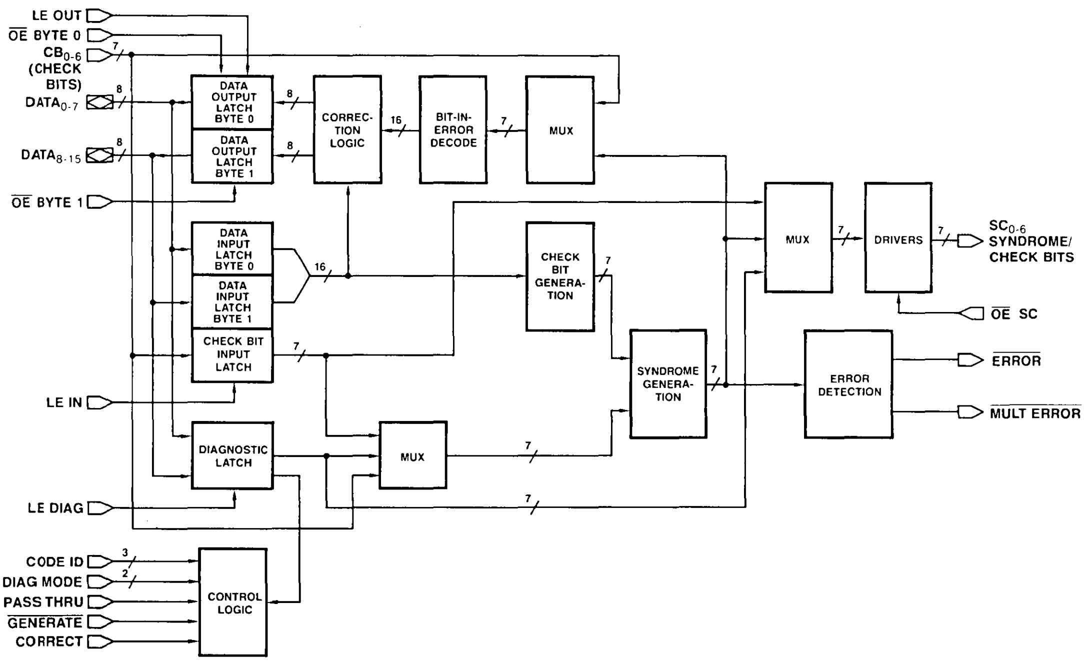
Devices are specified for use in high performance CPU and controller systems (Am2960 series) or MOS microcomputer-based designs such as the AmZ8000 (AmZ8160 series). Additional timing and control elements such as a clock oscillator and EDC controller will be available specifically for use with the AmZ8001 and AmZ8002 CPU devices. See Section IV for more details.



Typical Memory System Configuration Using the Am2960 Family of Devices

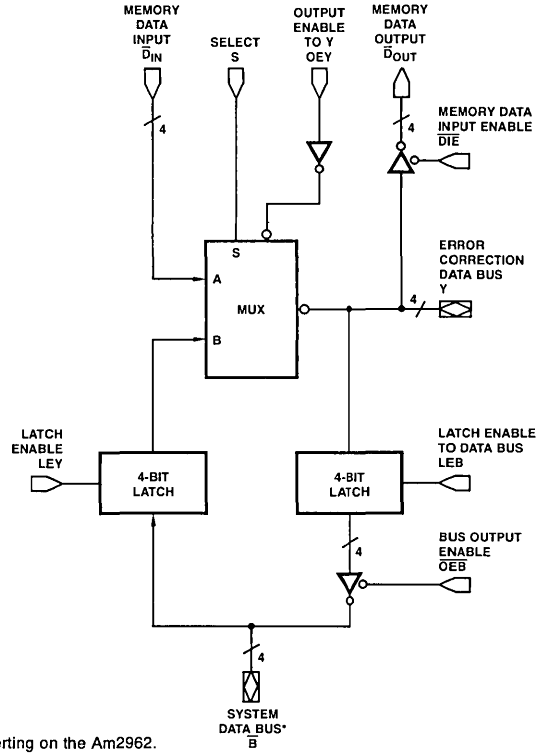
Am2960 Cascadable 16-Bit Error Detection and Correction Unit

- Modified Hamming Code
  Detects multiple errors and corrects single-bit errors in a parallel data word
  Ideal for use in dynamic memory systems
- Expandable
  One Am2960 provides EDC on 16-bit data words
  Two Am2960s provide EDC on 32-bit data words
  Four Am2960s provide EDC on 64-bit data words
- Syndromes Provided
  Makes available the syndrome bits when an error occurs so the location of memory faults can be logged
- Microprocessor Compatible
  Designed to work with MOS microprocessor systems as well as high performance Am2900 designs
- Target Speeds for 16-Bit Configuration
  30ns for error detection
  50ns for error correction
  40ns for check bit generation
- Built-in Diagnostics
  Extra on-chip logic provides diagnostic functions to be used during device test and for system diagnostics
- 48-Pin DIP



Am2961/Am2962 4-Bit Error Correction Multiple Bus Buffers

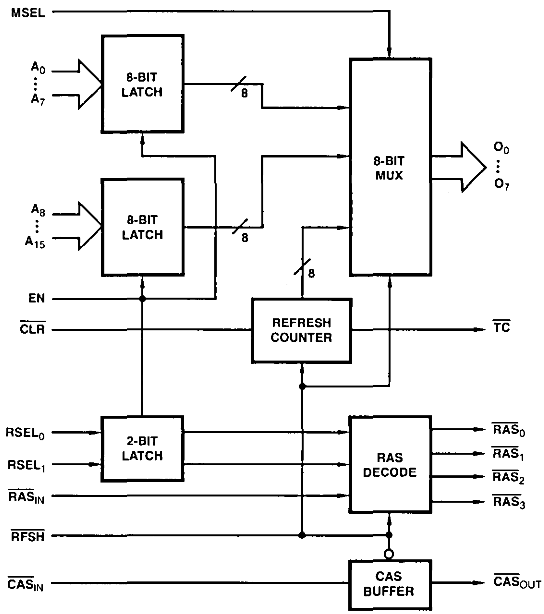
- Quad High-Speed LSI Bus Transceiver
- Provides Complete Data Path Interface between Am2960 Error Detection and Correction Unit, System Data Bus and Dynamic RAM Memory
- 3-State 24mA Output to Data Bus
- 3-State Data Output to Memory
- Inverting Data Bus for Am2961
- Non-Inverting Data Bus for Am2962
- Data Bus Latches Allow Operation with Multiplexed Busses
- Space Saving 24-Pin 0.3" DIP



*Data bus B is non-inverting on the Am2962.

Am2964B Dynamic Memory Controller

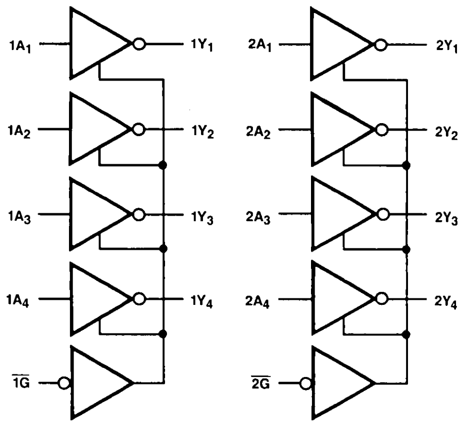
- Dynamic Memory Controller for 16K and 64K MOS Dynamic RAMs
- 8-Bit Refresh Counter with Clear Input and Terminal Count Output for Refresh Address Generation
- Refresh Counter Terminal Count Selectable at 256 or 128
- Latch Input $\overline{RAS}$ Decoder Provides Four $\overline{RAS}$ Outputs, All Active during Refresh
- Dual 8-Bit Address Latches plus Separate $\overline{RAS}$ Decoder Latches
- Grouped Functions Minimize Speed Differential/ Skew between Address, $\overline{RAS}$ and $\overline{CAS}$ Outputs
- 3-Port, 8-Bit Address Multiplexer with Schottky Speed
- Burst Mode, Distributed Refresh or Transparent Refresh Mode Determined by User
- Non-Inverting Address, $\overline{RAS}$ and $\overline{CAS}$ Paths
- Address to Output 12ns (Typ)
- "B" Designation Indicates V_{CC} on Pin 10, GND on Pin 30 and $\overline{RASI}$ Timing Control.
- 40-Pin DIP



Am2965/Am2966 Octal Dynamic Memory Drivers (with 3-State Outputs)

- Octal Drivers for 16K and 64K Dynamic RAMs
- Maximum Performance with −0.5V (Max) Undershoot
- No External Resistors Required
- t_{pd} Specified for 50pF and 500pF (Typ 9.0ns at 50pF)
- V_{CC} = 5.0V ± 10% for Commercial and Military
- V_{OH} (Min) = V_{CC} −1.15V
- I_{OH} and I_{OL} Specified at +2.0V
- Low-Power Schottky Input Characteristics
- Am2965 Inverting, Am2966 Non-inverting
- Glitch-Free 3-State Outputs during Power-Up/Down
- Symmetrical Controller Rise and Fall Time
- Pin Compatible Improved Performance Replacements for Designs Using 'S240 and 'S244 plus External Resistors
- 20-Pin DIP

Am2965*



*Outputs Y_1-Y_4 are non-inverting on Am2966.

Advanced Micro Devices pioneered the development of integrated circuits for use in high-speed military digital signal processing systems with the industry's first TTL Multiplier, the Am2505, in the early 1970s. Cost reductions have since stimulated the use of these techniques in commercial applications such as data transmission, process control, medical analysis, seismic exploration and versatile array processors.

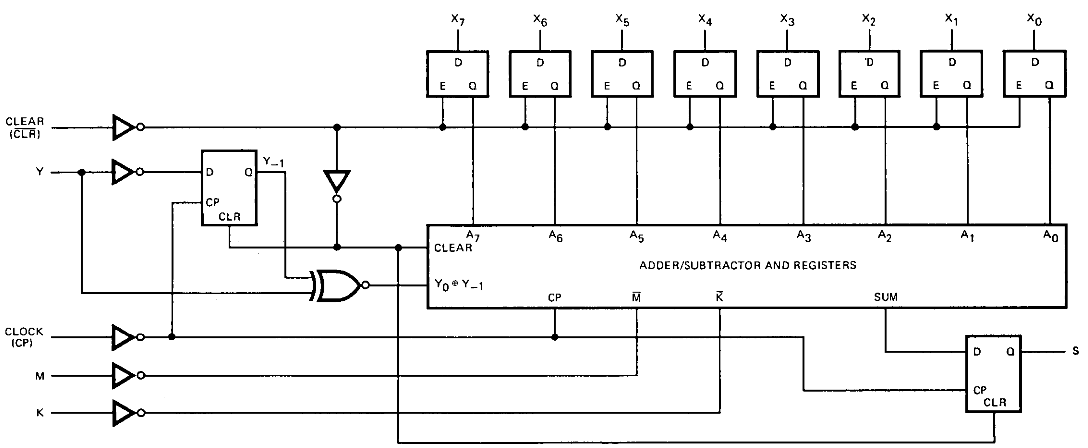
A full line of multipliers is available today. A new series of high density signal processing products, the Am29500 series, based on Advanced Micro Device's high performance oxide isolated IMOX process is in development. Devices described here include:

Serial/Parallel Multipliers
Combinatorial Multipliers
Support Products

SERIAL/PARALLEL MULTIPLIERS

Am25LS14 8-Bit Serial/Parallel Twos Complement Multiplier

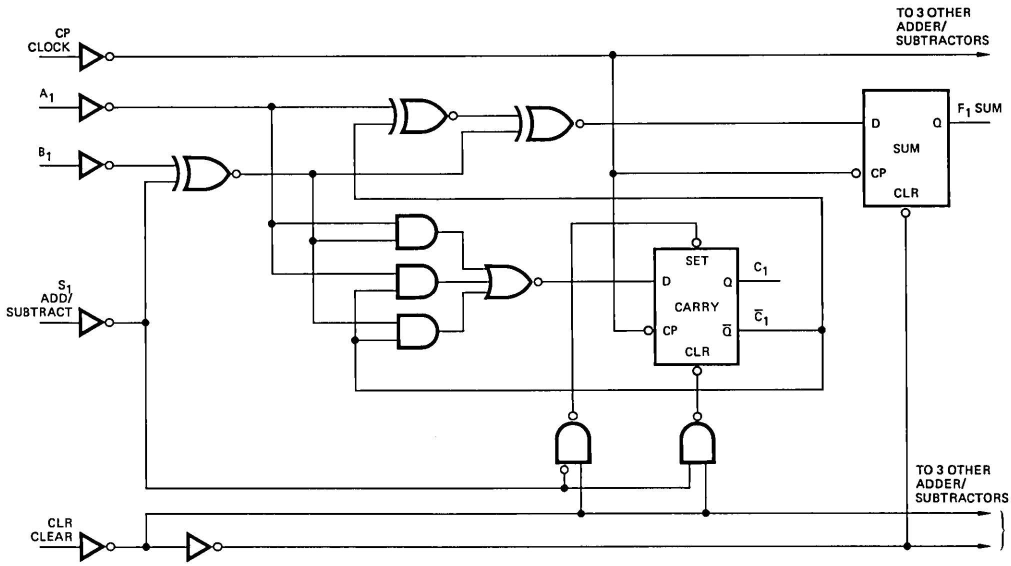
- Twos Complement Multiplication without Correction
- Magnitude Only Multiplication
- Cascadable for any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- 25MHz Minimum Clock Frequency
- 16-Pin DIP



MPR-327

Am25LS15 Quad Serial Adder/Subtractor

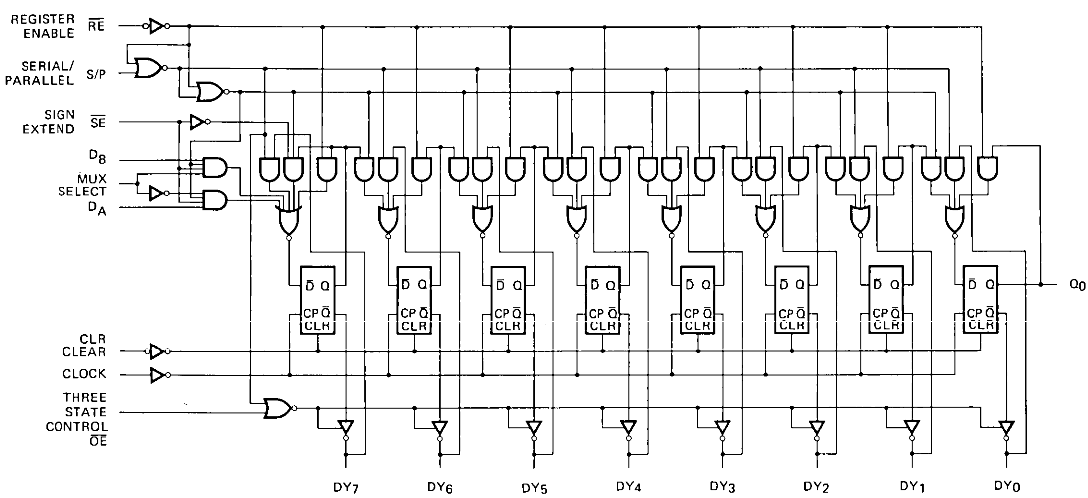
- Four Independent Adder/Subtractors
- Use with Twos Complement Arithmetic
- Magnitude Only Addition/Subtraction
- 20-Pin DIP



One of four similar functions.

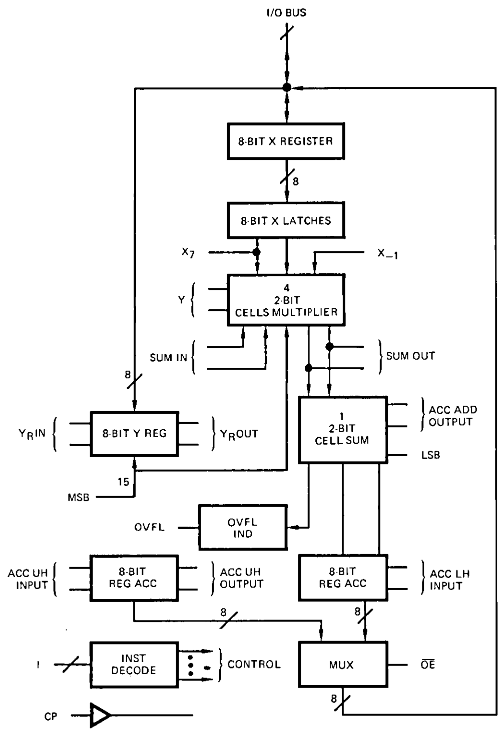
Am25LS22 8-Bit Serial/Parallel Register (with Sign Extend)

- Holds Multiplier Word, Performs Sign Extend and Holds Part of the Product when Used with Am25LS14
- 3-State Outputs with Multiplexed Input
- Multiplexed Serial Data Input
- 20-Pin DIP



Am25LS2516 8-Bit by 8-Bit Serial/Parallel Multiplier (with Accumulator)

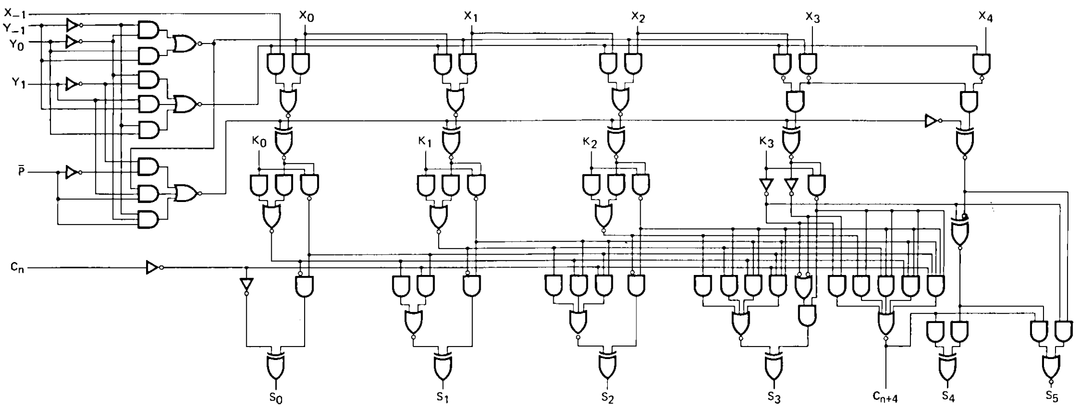
- Twos Complement 2-Bit Lookahead Carry-Save Arithmetic
- Microprogrammable
  4-bit instruction code for load, multiply and read operations
- Cascadable
  Two devices perform full 16-bit multiplication without additional hardware
- 8-Bit Byte Parallel, Bidirectional, Bussed I/O
- On-Chip Registers and Double Length Accumulator
- Overflow Indicator
- 3-State Shared Bus I/O Lines
- High-Speed Architecture Provides Clock Rates of 20MHz (Typ)
- 40-Pin Package



COMBINATORIAL MULTIPLIERS

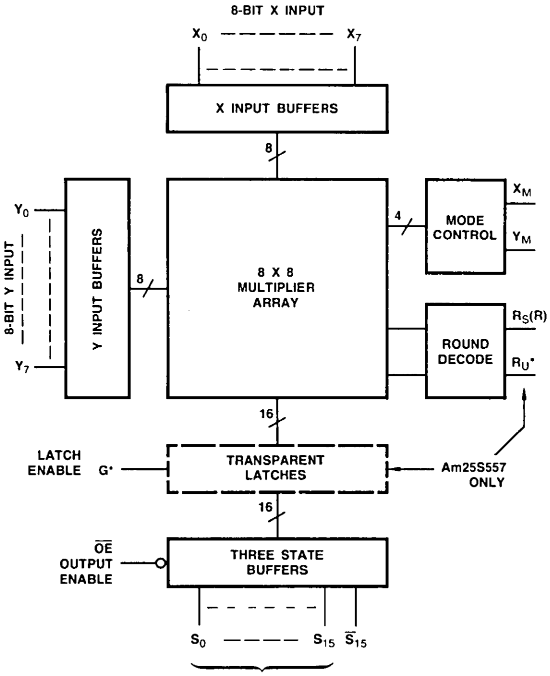
Am25S05 4-Bit by 2-Bit Twos Complement Multiplier

- Provides High-Speed Twos Complement Multiplication without Correction
- Can Be Used in Combinatorial Array or Time-Sequenced Mode
- Multiplies Two 12-Bit Signed Numbers in 115ns (Typ)
- Multiplies in Active-HIGH (Positive Logic) or Active-LOW (Negative Logic) Representations
- 24-Pin DIP



Am25S557/Am25S558 8-Bit by 8-Bit Combinatorial Multiplier

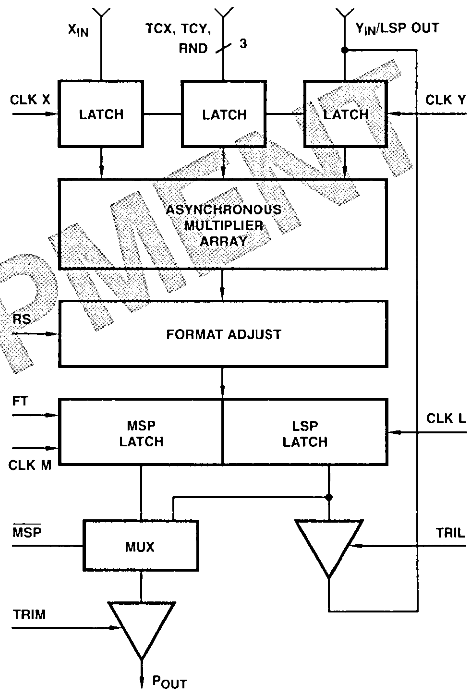
- Multiplies Two 8-Bit Numbers – 16-Bit Output
- Combinatorial – No Clocks Required
- Full 8 x 8 Multiply in 45ns (Typ)
- Cascades to 16 x 16 in 110ns (Typ)
- Expandable to Multiples of Eight Bits
- MSB and $\overline{\text{MSB}}$ Outputs for Easy Expansion
- Unsigned, Twos Complement or Mixed Operands
- Implements Common Rounding Algorithms with Additional Logic
- 3-State Outputs
- Transparent 16-Bit Latch in Am25S557
- Industry Standard Pinouts
- 40-Pin DIP



*Pin 11 is G for Am25S557 and R_U for Am25S558.

Am29516/Am29517 16 by 16 Combinatorial Multipliers

- Twos Complement, Unsigned or Mixed Numbers
- LSP Available at Y_{IN} or P_{OUT}
- Am29516 Pin Compatible with TRW MPY-16HJ
- Am29517 Has Single Clock Input with X, Y and P Clock Enables
- Internal ECL Array Provides Multiply Time of 75ns (Typ)
- 64-Pin DIP

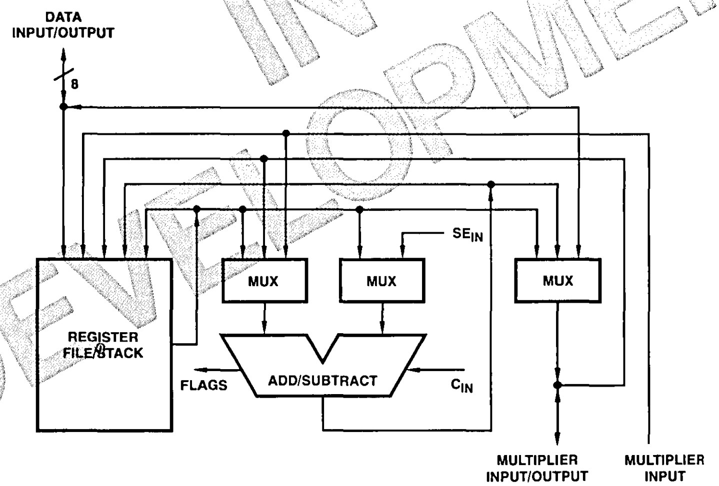


IN DEVELOPMENT

SUPPORT PRODUCTS

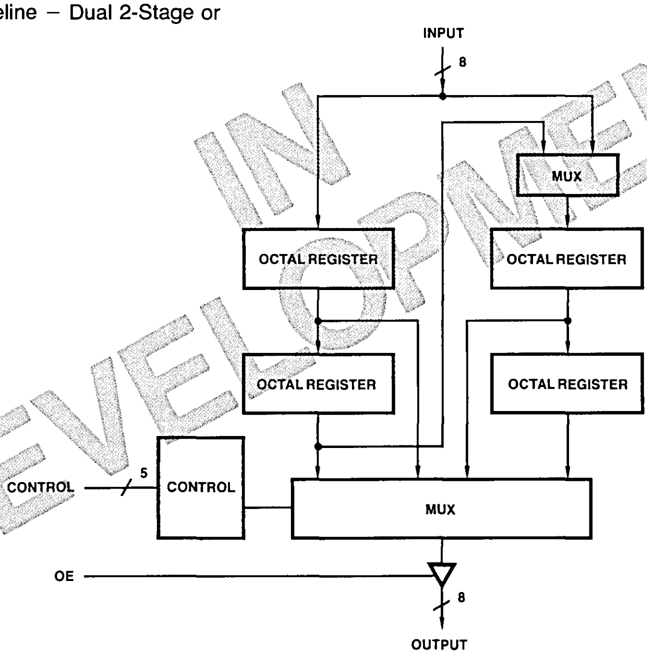
Am29501 Programmable Signal Processor

- 8-Bit Slice
- 8-Bit ALU
- Six 8-Bit Register File
- Designed to Operate with Am29516/Am29517
- 29-Bit Microcode Control
- Multiple Simultaneous Data Moves
- Supports 100ns Microcycle Time
- 64-Pin DIP



Am29520/Am29521 Multilevel Pipeline Register

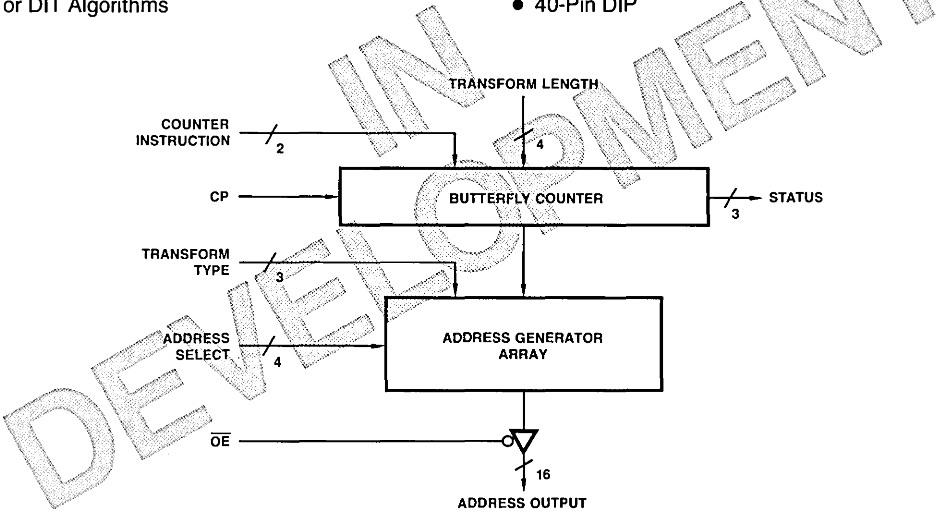
- Four 8-Bit Vipeline Registers
- All Registers Mux to Output
- Programmable Pipeline – Dual 2-Stage or Single 4-Stage
- Am29520 Has Separate Load and Shift
- 24-Pin 0.3" Wide DIP



IN DEVELOPMENT
IN DEVELOPMENT

Am29540 Programmable FFT Address Sequencer

- Generates Data/Coefficient Addresses
- Programmable Length – 2 to 65536 Point Transforms
- DIF or DIT Algorithms
- Bit-Reversed I or O (In-Place)
- Radix-2 or -4 Address Sequence
- Radix-2 RVI Transforms
- 40-Pin DIP



BIPOLAR LSI AND SUPPORT PRODUCTS
System Interface Products

Advanced Micro Devices offers a comprehensive line of interface devices optimized for use with bipolar and MOS microprocessor and other LSI products.

They can be grouped into three categories:
- Bus Interface
- Transmission Line Interface
- Microcomputer Interface and Support

2

Bus Interface

Item	Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inverting/ Non-Inverting	Output	Number of Pins	Package(s)
Drivers/Buffers									
1	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**Am25LS240**	48	0.55	12	I	3S	20	D, F, P
2	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**54/74LS240**	24*	0.5	12	I	3S	20	D, F, P
3	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**Am25S240**	64	0.55	4.5	I	3S	20	D, P
4	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**54/74S240**	64	0.55	4.5	I	3S	20	D, P
5	Octal Driver w/$\overline{OE}$, OE	**Am25LS241**	48	0.55	12	N	3S	20	D, F, P
6	Octal Driver w/$\overline{OE}$, OE	**54/74LS241**	24*	0.5	12	N	3S	20	D, F, P
7	Octal Driver w/$\overline{OE}$, OE	**Am25S241**	64	0.55	6.0	N	3S	20	D, P
8	Octal Driver w/$\overline{OE}$, OE	**54/74S241**	64	0.55	6.0	N	3S	20	D, P
9	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**Am25LS244**	48	0.55	12	N	3S	20	D, F, P
10	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**54/74LS244**	24*	0.5	12	N	3S	20	D, F, P
11	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**Am25S244**	64	0.55	6.0	N	3S	20	D, P
12	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**54/74S244**	64	0.55	6.0	N	3S	20	D, P
13	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**Am2958**	64	0.55	4.5	N	3S	20	D, P
14	Octal Driver w/$\overline{OE}$, $\overline{OE}$	**Am2959**	64	0.55	6.0	I	3S	20	D, P
15	Octal Buffer w/$\overline{G}_1$, $\overline{G}_2$	**71/81LS95**	16	0.5	15	N	3S	20	D, P
16	Octal Buffer w/$\overline{G}_1$, $\overline{G}_2$	**71/81LS96**	16	0.5	13	I	3S	20	D, P
17	Octal Buffer w/$\overline{G}_1$, $\overline{G}_2$	**71/81LS97**	16	0.5	15	N	3S	20	D, P
18	Octal Buffer w/$\overline{G}_1$, $\overline{G}_2$	**71/81LS98**	16	0.5	13	I	3S	20	D, P
Transceivers									
19	Octal Transceiver w/T/$\overline{R}$, CD	**Am2946**	24/48	0.5	11	I	3S	20	D, P
20	Octal Transceiver w/T/$\overline{R}$, CD	**Am2947**	24/48	0.5	14	N	3S	20	D, P
21	Octal Transceiver w/$\overline{T}$, $\overline{R}$	**Am2948**	24/48	0.5	11	I	3S	20	D, P
22	Octal Transceiver w/$\overline{T}$, $\overline{R}$	**Am2949**	24/48	0.5	14	N	3S	20	D, P
23	Quad IEEE-488 Transceiver	**3448A**	48	0.5	12	N	3S/OC	16	D, P
24	Quad Transceiver w/$\overline{OE}$, OE	**Am25LS242**	48	0.55	12	I	3S	20	D, F, P
25	Quad Transceiver w/$\overline{OE}$, OE	**54/74LS242**	24*	0.5	12	I	3S	20	D, F, P
26	Quad Transceiver w/$\overline{OE}$, OE	**54/74S242**	64	0.55	4.5	I	3S	20	D, P
27	Quad Transceiver w/$\overline{OE}$, OE	**Am25LS243**	48	0.55	12	N	3S	20	D, F, P
28	Quad Transceiver w/$\overline{OE}$, OE	**54/74LS243**	24*	0.5	12	N	3S	20	D, F, P
29	Quad Transceiver w/$\overline{OE}$, OE	**54/74S243**	64	0.55	6.0	N	3S	20	D, P
30	Octal Transceiver w/T/$\overline{R}$, CD	**73/8303**	16/48	0.5	11	I	3S	20	D, P
31	Octal Transceiver w/T/$\overline{R}$, CD	**73/8304B**	16/48	0.5	14	N	3S	20	D, P
32	Octal Transceiver w/$\overline{T}$, $\overline{R}$	**73/8307**	16/48	0.5	11	I	3S	20	D, P
33	Octal Transceiver w/$\overline{T}$, $\overline{R}$	**73/8308**	16/48	0.5	14	N	3S	20	D, P

*74LS only, see data sheet for 54LS specification.

Bus Interface (Cont.)

Item	Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inverting/ Non-Inverting	Output	Number of Pins	Package(s)
3-Port Transceivers									
1	Quad Transceiver	**Am26S10**	100	0.8	10	I to Bus	3S	16	D, F, P
2	Quad Transceiver	**Am26S11**	100	0.8	12	N to Bus	3S	16	D, F, P
3	Quad Transceiver, V_{HYST} (Rcvr) = 0.6V	**Am26S12**	100	0.85	14	I	3S	16	D, F, P
4	Quad Transceiver, V_{HYST} (Rcvr) = 1.05V	**Am26S12A**	100	0.85	14	I	3S	16	D, F, P
5	Quad 2-Input Transceiver w/3S Rcvr	**Am2905**	100	0.8	21	I	OC	24	D, F, P
6	Quad 2-Input Transceiver w/Parity	**Am2906**	100	0.8	21	I	OC	24	D, F, P
7	Quad Transceiver w/3S Rcvr and Parity	**Am2907**	100	0.8	21	I	OC	20	D, F, P
8	Quad Transceiver w/3S Rcvr and Parity (DEC Compatible)	**Am2908**	100	0.8	21	I	OC	20	D, F, P
9	Quad Transceiver	**Am2912**	100	0.8	10	I	3S	16	D, F, P
10	Quad 2-Input Transceiver w/3S Rcvr	**Am2915A**	48	0.5	21	I	3S	24	D, F, P
11	Quad 2-Input Transceiver w/Parity	**Am2916A**	48	0.5	21	I	3S	24	D, F, P
12	Quad Transceiver w/3S Rcvr and Parity	**Am2917A**	48	0.5	21	I	3S	24	D, F, P
13	Quad Transceiver	**Am2926**	48	0.5	10	I	3S	16	D, P
14	Quad Transceiver w/Clock Enable (Latched Output)	**Am2927**	48	0.5	18	I	3S	20	D, F, P
15	Quad Transceiver w/Clock Enable (Registered Output)	**Am2928**	48	0.5	18	I	3S	20	D, F, P
16	Quad Transceiver	**Am2929**	48	0.5	13	N	3S	16	D, P
17	Quad Transceiver	**8T26A**	48	0.5	10	I	3S	16	D, P
18	Quad Transceiver	**8T28**	48	0.5	13	N	3S	16	D, P
Registers/Latches									
19	Octal Register w/CP and $\overline{CLR}$	**Am25LS273**	8.0	0.45	15	N	TTL	20	D, F, P
20	Octal Register w/CP and $\overline{CLR}$	**54/74LS273**	8.0*	0.5	18	N	TTL	20	D, F, P
21	Octal Register w/CP, $\overline{CLR}$ (Buffered Outputs)	**Am25LS273B**	8.0	0.45	25	N	TTL	20	D, F, P
22	Octal Latch w/G, $\overline{OE}$	**Am25LS373**	24	0.5	20	N	3S	20	D, F, P
23	Octal Latch w/G, $\overline{OE}$	**54/74LS373**	24*	0.5	20	N	3S	20	D, F, P
24	Octal Latch w/G, $\overline{OE}$	**Am25S373**	32	0.5	12	N	3S	20	D, F, P
25	Octal Latch w/G, $\overline{OE}$	**54/74S373**	20	0.5	12	N	3S	20	D, F, P
26	Octal Register w/CP, $\overline{OE}$	**Am25LS374**	24	0.5	15	N	3S	20	D, F, P
27	Octal Register w/CP, $\overline{OE}$	**54/74LS374**	24*	0.5	22	N	3S	20	D, F, P
28	Octal Register w/CP, $\overline{OE}$	**Am25S374**	32	0.5	11	N	3S	20	D, F, P
29	Octal Register w/CP, $\overline{OE}$	**54/74S374**	20	0.5	11	N	3S	20	D, F, P
30	Octal Register w/CP, CP Enable	**Am25LS377**	8.0	0.5	14	N	TTL	20	D, F, P
31	Octal Register w/CP, CP Enable	**54/74LS377**	8.0*	0.5	18	N	TTL	20	D, F, P
32	Octal Register w/CP, CP Enable (Buffered Outputs)	**Am25LS377B**	8.0	0.5	23	N	TTL	20	D, F, P
33	Octal Latch w/G, $\overline{OE}$	**Am25LS533**	24	0.5	20	I	3S	20	D, F, P
34	Octal Latch w/G, $\overline{OE}$	**54/74LS533**	24*	0.5	20	I	3S	20	D, F, P
35	Octal Latch w/G, $\overline{OE}$	**Am25S533**	32	0.5	14	I	3S	20	D, F, P
36	Octal Latch w/G, $\overline{OE}$	**54/74S533**	20	0.5	19	I	3S	20	D, F, P
37	Octal Register w/CP, $\overline{OE}$	**Am25LS534**	24	0.5	15	I	3S	20	D, F, P
38	Octal Register w/CP, $\overline{OE}$	**54/74LS534**	24*	0.5	22	I	3S	20	D, F, P

*74LS only, see data sheet for 54LS specification.

Bus Interface (Cont.)

Item	Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inverting/ Non-Inverting	Output	Number of Pins	Package(s)
Registers/Latches (Cont.)									
1	Octal Register w/CP, $\overline{OE}$	**Am25S534**	32	0.5	11	I	3S	20	D, F, P
2	Octal Register w/CP, $\overline{OE}$	**54/74S534**	20	0.5	11	I	3S	20	D, F, P
3	Octal Register w/CP, $\overline{CLR}$, $\overline{OE}$, CP Enable	**Am25LS2520**	8.0	0.45	24	N	3S	22	D, F, P
4	Octal Register w/CP, $\overline{CLR}$, $\overline{OE}$, CP Enable	**Am2920**	8.0	0.45	24	N	3S	22	D, F, P
5	Octal Register w/CP, OE	**Am2954**	32	0.5	11	N	3S	20	D, F, P
6	Octal Register w/CP, OE	**Am2955**	32	0.5	11	I	3S	20	D, F, P
7	Octal Latch w/G, $\overline{OE}$	**Am2956**	32	0.5	9.0	N	3S	20	D, F, P
8	Octal Latch w/G, $\overline{OE}$	**Am2957**	32	0.5	14	I	3S	20	D, F, P

Transmission Line Interface

Item	Description	Part Number	t_{pd} ns (Typ)	t_{SKEW} ns (Typ)	V_{HYST} mV (Typ)	V_{TH} mV (Min)	Diff/ Single-Ended	Output	Number of Pins	Package(s)
9	Dual Party Line Transceiver	**Am26LS27**	In Development				D	D, 3S	20	D, P
10	Dual Party Line Transceiver	**Am26LS28**					D	D, 3S	20	D, P
11	Quad RS-423 Line Driver	**Am26LS29**	120				S	3S	16	D, F, P
12	Dual/Quad RS-422/423 Line Driver	**Am26LS30**	120				D/S	TTL	16	D, F, P
13	Quad RS-422 Line Driver	**Am26LS31**	12	±2			D	D, 3S	16	D, F, P
14	Quad RS-422 Line Receiver	**Am26LS32**	13	±1	100	200	D	3S	16	D, F, P
15	Quad High V_{CM} Line Receiver	**Am26LS33**	16	±1	170	500	D	3S	16	D, F, P
16	Quad Party Line Receiver	**Am26LS34**	16	±1	170	200	D	3S	16	D, P
17	Quad Party Line Receiver	**Am26LS35**	16	±1	170	200	D	3S	16	D, P

Microcomputer Interface and Support Circuits

Item	Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inv./Non-Inverting	Output	Number of Pins	Package(s)
8-Bit Microcomputer Support Circuits									
18	Octal Input/Output Port	**8212**	15	0.45	12	N	3S	24	D, P
19	Quad Bidirectional Bus Driver	**8216**	50	0.6	15	N	3S	16	D, P
20	Clock Generator/Driver	**8224**	15	0.45			8080 Levels	16	D, P
21	Quad Bidirectional Bus Driver	**8226**	50	0.6	15	I	3S	16	D, P
22	System Controller	**8228**	2/10	0.45	15-30	Generates 8080 Control and Data Bus Interface		28	D, P
23	System Controller	**8238**	2/10	0.45	15-30			28	D, P

Microcomputer Interface and Support Circuits (Cont.)

Item	Description	Part Number	I_{OL} (Max) mA	@V	t_{pd} ns (Typ)	Inv./Non-Inverting	Output	Number of Pins	Package(s)
16-Bit Microcomputer Support Circuits									
1	Octal Bus Transceiver w/T/$\overline{R}$, CD	**AmZ8103**	24/48	0.5	11	I	3S	20	D, P
2	Octal Bus Transceiver w/T/$\overline{R}$, CD	**AmZ8104**	24/48	0.5	14	N	3S	20	D, P
3	Octal Bus Transceiver w/$\overline{T}$, $\overline{R}$	**AmZ8107**	24/48	0.5	11	I	3S	20	D, P
4	Octal Bus Transceiver w/$\overline{T}$, $\overline{R}$	**AmZ8108**	24/48	0.5	14	N	3S	20	D, P
5	Octal Register w/CP, $\overline{CLR}$, $\overline{OE}$, CP Enable	**AmZ8120**	8.0	0.45	24	N	3S	24[1]	D
6	8-Bit Equal-to Comparator	**AmZ8121**	12	0.5	9.0		TTL	20	D, P
7	AmZ8000 Clock Generator w/Run/Halt, Single-Step, Wait and Timeout Controls	**AmZ8127**	See Product Features in Section 4					24[1]	D
8	Octal Latch w/G, $\overline{OE}$	**AmZ8133**	24	0.5	15	I	3S	20	D, P
9	3-to-8 Decoder w/Control Storage	**AmZ8136**	24	0.5	30		3S	20	D, P
10	Octal Bus Driver w/$\overline{OE}$, $\overline{OE}$	**AmZ8140**	48	0.55	9.0	I	3S	20	D, P
11	Octal Bus Driver w/$\overline{OE}$, $\overline{OE}$	**AmZ8144**	48	0.55	11	N	3S	20	D, P
12	3-to-8 Chip Select Decoder w/$\overline{ACK}$	**AmZ8148**	8.0	0.45	19		TTL	20	D, P
13	Octal Latch w/G, $\overline{OE}$	**AmZ8173**	24	0.5	12	N	3S	20	D, P

Dynamic Memory Support Products[2]

Item	Description	Part Number	Data Width	Function	Inv./Non-Inverting	Number of Pins	Package(s)
14	Error Detection and Correction Unit (EDC)	**AmZ8160**	16	Expandable Hamming Code EDC Slice w/Diagnostics/Initialization and Byte-Level I/O Interface	I to Bus	48	D
15	EDC Data Bus Buffer	**AmZ8161**	4	4-Port EDC Interface for RAM, EDC and 24mA I_{OL} Data Bus Drive	I to Bus	24[1]	D
16	EDC Data Bus Buffer	**AmZ8162**	4	4-Port EDC Interface for RAM, EDC and 24mA I_{OL} Data Bus Drive	N to Bus	24[1]	D
17	EDC and Refresh Controller	**AmZ8163**	–	Memory Timing and Controls for AmZ8160/AmZ8164 (used w/AmZ8127)	–	40	D, P
18	Dynamic Memory Controller	**AmZ8164B**	–	Memory Address Controller w/Refresh Counter, $\overline{RAS}$ Decoder,$\overline{CAS}$ Inhibit Buffer	–	40	D, P
19	Dynamic RAM Driver	**AmZ8165**	8	RAM Driver w/3-State, Undershoot Protected Outputs	I	20	D, P
20	Dynamic RAM Driver	**AmZ8166**	8	RAM Driver w/3-State, Undershoot Protected Outputs	N	20	D, P

One-Shots

Item	Description	Part Number	I_{OL} (Max) mA	@ V	t_{pd} ns (Typ)	Inv./Non-Inverting	Output	Number of Pins	Package(s)
21	Retriggerable, Resettable, Monostable Multivibrator	**Am26S02**	20	0.5	28	N or I	TTL	16	D, F, P

Notes: 1. New 24-pin, 0.3" wide package.
2. See product features in Section 4.

MEMORY
Bipolar

Static RAMs

Item	Organization	Part Number	Access Time COM ns (Max)	Access Time MIL ns (Max)	I_{CC} COM mA (Max)	I_{CC} MIL mA (Max)	Output	Number of Pins	Package(s)	Comments
TTL										
1	16 x 4	**Am27S02A**	25	30	100	105	OC	16	D, P, F	Ultra Fast
2	16 x 4	**Am27S03A**	25	30	100	105	3S	16	D, P, F	
3	16 x 4	**Am27S02**	35	50	105	105	OC	16	D, P, F	
4	16 x 4	**Am27S03**	35	50	125	125	3S	16	D, P, F	
5	16 x 4	**Am54S189**		50		125	3S	16	D, F	
6	16 x 4	**Am74S189**	35		125		3S	16	D, P, F	
7	16 x 4	**Am54S289**		50		105	OC	16	D, F	
8	16 x 4	**Am74S289**	35		105		OC	16	D, P, F	
9	16 x 4	**Am27S06**	35	50	100	105	OC	16	D, P, F	Non-Inverting Outputs
10	16 x 4	**Am27S07**	35	50	100	105	3S	16	D, P, F	
11	16 x 4	**Am29700**	35	50	100	105	OC	16	D, P, F	
12	16 x 4	**Am29701**	35	50	100	105	3S	16	D, P, F	
13	16 x 4	**Am3101**	60		105		OC	16	D, P, F	Write Transparent[1]
14	16 x 4	**Am3101-1**	35	50	100	105	OC	16	D, P, F	
15	16 x 4	**Am5489-1**		50		105	OC	16	D, F	
16	16 x 4	**Am7489**	60		105		OC	16	D, P, F	
17	16 x 4	**Am7489-1**	35		100		OC	16	D, P, F	
18	16 x 4	**Am31L01A**	55	65	35	38	OC	16	D, P, F	Write Transparent[1], Low Power
19	16 x 4	**Am27LS02**	55	65	35	38	OC	16	D, P, F	Low Power
20	16 x 4	**Am27LS03**	55	65	35	38	3S	16	D, P, F	
21	16 x 4	**Am27LS06**	55	65	35	38	OC	16	D, P, F	Non-Inverting Outputs, Low Power
22	16 x 4	**Am27LS07**	55	65	35	38	3S	16	D, P, F	
23	256 x 1	**Am27LS00A**	35	45	100	100	3S	16	D, P, F	Ultra Fast
24	256 x 1	**Am27LS01A**	35	45	100	100	OC	16	D, P, F	
25	256 x 1	**Am27LS00**	45	55	70	70	3S	16	D, P, F	Fast, Low Power
26	256 x 1	**Am27LS01**	45	55	70	70	OC	16	D, P, F	
27	1024 x 1	**Am93415**	45	60	155	170	OC	16	D, P, F	
28	1024 x 1	**Am93425**	45	60	155	170	3S	16	D, P, F	
29	256 x 4	**Am93412**	45	60	155	170	OC	22[2]	D, P, F	
30	256 x 4	**Am93422**	45	60	155	170	3S	22[2]	D, P, F	
31	256 x 4	**Am93L412**	60	75	80	90	OC	22[2]	D, P, F	Low Power
32	256 x 4	**Am93L422**	60	75	80	90	3S	22[2]	D, P, F	
ECL										
33	1024 x 1	**Am10415**	35	40	150	165		16	D, P, F	10K
34	1024 x 1	**Am100415**	20	30	150	165		16	D, P, F	100K

Notes: 1. Complement of data-in is available on the outputs in the Write Mode when both $\overline{CS}$ and $\overline{WE}$ are LOW.
2. Flatpack (F) is 24-pin.

MEMORY
Bipolar

PROMs

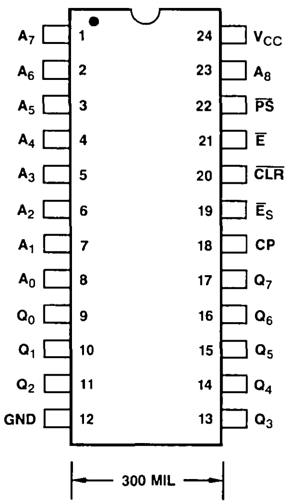
Item	Organization	Part Number	Access Time COM ns (Max)	Access Time MIL ns (Max)	I_{CC} COM mA (Max)	I_{CC} MIL mA (Max)	Output	Number of Pins	Package(s)	Comments
1	32 x 8	**Am27LS18**[1]	50	65	80	80	OC	16	D, F	Low Power
2	32 x 8	**Am27LS19**[1]	50	65	80	80	3S	16	D, F	
3	32 x 8	**Am27S18**	40	50	115	115	OC	16	D, F	
4	32 x 8	**Am27S19**	40	50	115	115	3S	16	D, F	
5	256 x 4	**Am27S20**	45	60	130	130	OC	16	D, F	
6	256 x 4	**Am27S21**	45	60	130	130	3S	16	D, F	
7	512 x 4	**Am27S12**	50	60	130	130	OC	16	D, F	
8	512 x 4	**Am27S13**	50	60	130	130	3S	16	D, F	
9	512 x 8[2]	**Am27S25**	NA[3]	NA[3]	185	185	3S	24	D, F	Output Registers, Slimline Pkg[4]
10	512 x 8[2]	**Am27S26**	NA[3]	NA[3]	185	185	OC	22[5]	D, F	Output Registers
11	512 x 8[2]	**Am27S27**	NA[3]	NA[3]	185	185	3S	22[5]	D, F	
12	512 x 8	**Am27S28**	55	70	160	160	OC	20	D, F	
13	512 x 8	**Am27S29**	55	70	160	160	3S	20	D, F	
14	512 x 8	**Am27S30**	55	70	175	175	OC	24	D, F	
15	512 x 8	**Am27S31**	55	70	175	175	3S	24	D, F	
16	1024 x 4	**Am27S32**	55	70	140	145	OC	18	D, F	
17	1024 x 4	**Am27S33**	55	70	140	145	3S	18	D, F	
18	1024 x 8	**Am27S180**	60	80	185	185	OC	24	D, F	
19	1024 x 8	**Am27S181**	60	80	185	185	3S	24	D, F	
20	1024 x 8[2]	**Am27S35**[6]	NA[3]	NA[3]	175	175	3S	24	D, F	Output Registers, Slimline Pkg[4]
21	2048 x 4	**Am27S184A**	35	45	150	150	OC	18	D, F	Ultra Fast
22	2048 x 4	**Am27S185A**	35	45	150	150	3S	18	D, F	Ultra Fast
23	2048 x 4	**Am27S184**	50	55	150	150	OC	18	D, F	Fast
24	2048 x 4	**Am27S185**	50	55	150	150	3S	18	D, F	Fast
25	2048 x 4	**Am27LS184**	60	65	120	125	OC	18	D	Low Power
26	2048 x 4	**Am27LS185**	60	65	120	125	3S	18	D	Low Power
27	2048 x 4	**Am27PS184**	60	65	150/75	150/75	OC	18	D	Power Switched
28	2048 x 4	**Am27PS185**	60	65	150/75	150/75	3S	18	D	
29	2048 x 8	**Am27S190**[6]	50	65	165	175	OC	24	D	Fast
30	2048 x 8	**Am27S191**[6]	50	65	165	175	3S	24	D	Fast
31	2048 x 8	**Am27PS190**[6]	60	70	165/70	175/75	OC	24	D	Power Switched
32	2048 x 8	**Am27PS191**[6]	60	70	165/70	175/75	3S	24	D	
33	4096 x 4[2]	**Am27S40**[6]	50	60	165	175	OC	20	D	Fast
34	4096 x 4[2]	**Am27S41**[6]	50	60	165	175	3S	20	D	Fast
35	4096 x 4	**Am27PS40**[6]	60	70	165/70	175/75	OC	20	D	Power Switched
36	4096 x 4	**Am27PS41**[6]	60	70	165/70	175/75	3S	20	D	

Notes: 1. Replaces Am27LS08/09.
2. See connection and block diagrams within this section.
3. Contains built-in pipeline registers: nominal address to clock set-up time = 40ns (typ), clock to output = 15ns (typ).
4. 300 mil lateral pin spacing.
5. Flatpack is 24-pin.
6. To be announced.

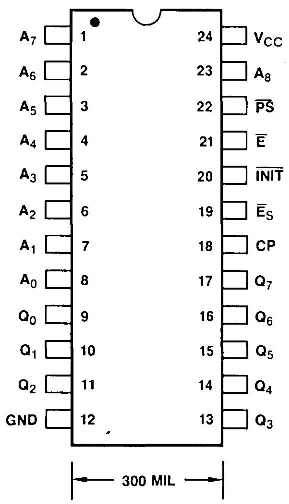
CONNECTION DIAGRAMS (Top Views)

Slimline 24-Pin Family of Output Registered PROMs

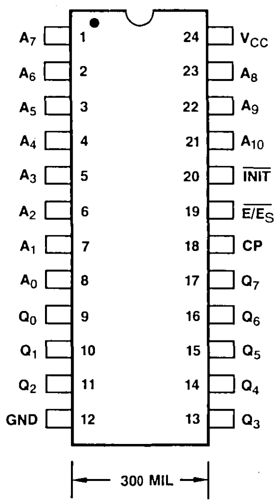
Am27S25 (512 x 8)



Am27S35 (1024 x 8)



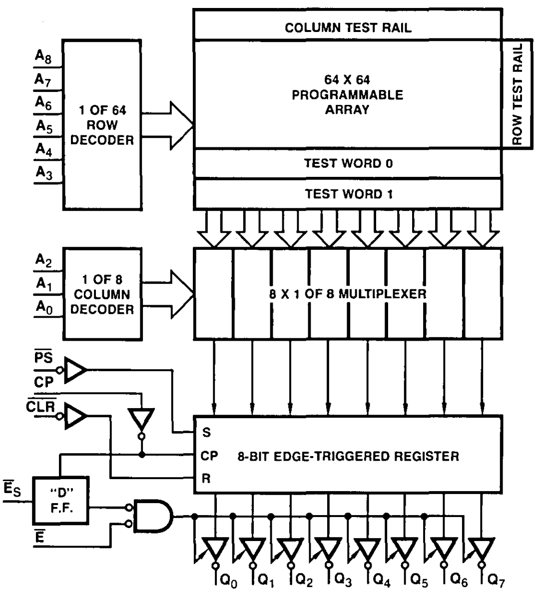
Am27S45 (Future 16K PROM)



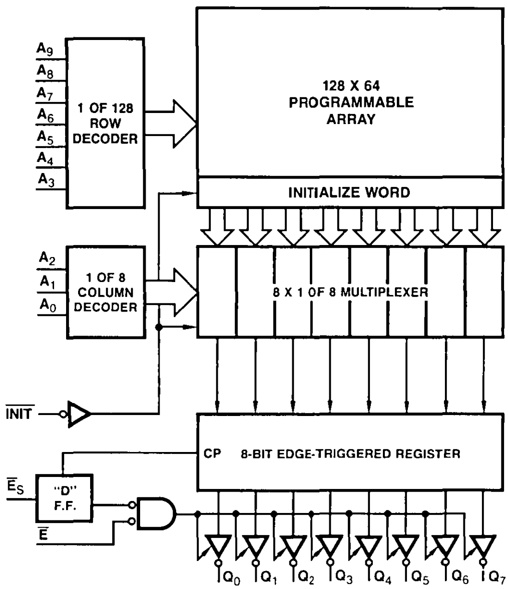
Note: Pin 1 is marked for orientation.

BLOCK DIAGRAMS

Am27S25

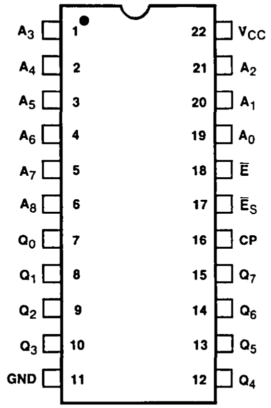


Am27S35

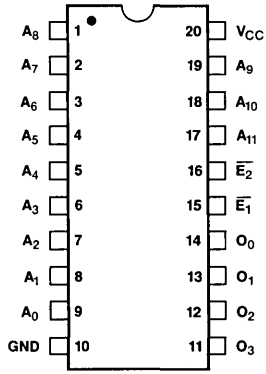


CONNECTION DIAGRAMS (Top Views)

Am27S26/Am27S27
512 x 8 Output Registered PROM



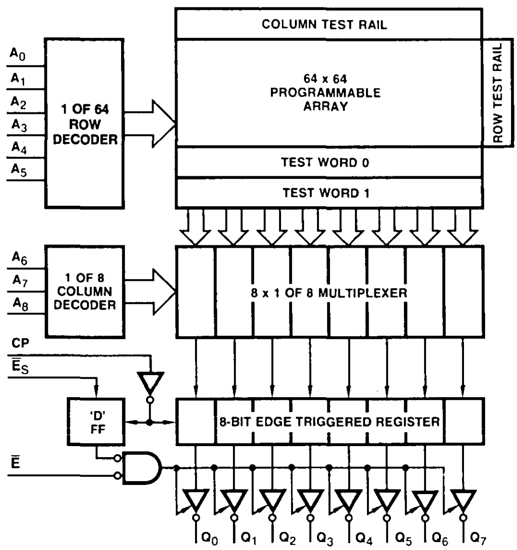
Am27S40/Am27S41
4096 x 4 PROM



Note: Pin 1 is marked for orientation.

BLOCK DIAGRAM

Am27S26/Am27S27



MEMORY
MOS

RAMs

Item	Organization	Part Number	Access Time ns (Max)	Power Dissipation COM Act/Stby mW (Max)	Power Dissipation MIL Act/Stby mW (Max)	Supply Voltage V	Temperature Range	Number of Pins[1]	Package(s)
Static									
1	256 x 4	**Am9101A**	500	290/	330/	+5	C, M	22	D, P
2	256 x 4	**Am91L01A**	500	173/	204/	+5	C, M	22	D, P
3	256 x 4	**Am9101B**	400	290/	330/	+5	C, M	22	D, P
4	256 x 4	**Am91L01B**	400	173/	204/	+5	C, M	22	D, P
5	256 x 4	**Am9101C**	300	315/	357/	+5	C, M	22	D, P
6	256 x 4	**Am9101D**	250	315/		+5	C	22	D, P
7	256 x 4	**Am9111A**	500	290/	330/	+5	C, M	18	D, P
8	256 x 4	**Am91L11A**	500	173/	204/	+5	C, M	18	D, P
9	256 x 4	**Am9111B**	400	290/	330/	+5	C, M	18	D, P
10	256 x 4	**Am91L11B**	400	173/	204/	+5	C, M	18	D, P
11	256 x 4	**Am9111C**	300	315/	357/	+5	C, M	18	D, P
12	256 x 4	**Am9111D**	250	315/		+5	C	18	D, P
13	256 x 4	**Am9112A**	500	290/	330/	+5	C, M	16	D, P
14	256 x 4	**Am91L12A**	500	173/	204/	+5	C, M	16	D, P
15	256 x 4	**Am9112B**	400	290/	330/	+5	C, M	16	D, P
16	256 x 4	**Am91L12B**	400	173/	204/	+5	C, M	16	D, P
17	256 x 4	**Am9112C**	300	315/	357/	+5	C, M	16	D, P
18	256 x 4	**Am9112D**	250	315/		+5	C	16	D, P
19	1024 x 4	**Am9114B**	450	367/	440/	+5	C, M	18	D, P, F
20	1024 x 4	**Am91L14B**	450	262/	330/	+5	C, M	18	D, P, F
21	1024 x 4	**Am9114C**	300	367/	440/	+5	C, M	18	D, P, F
22	1024 x 4	**Am91L14C**	300	262/	330/	+5	C, M	18	D, P, F
23	1024 x 4	**Am9114E**	200	367/		+5	C	18	D, P
24	1024 x 4	**Am9124B**	450	362/157	440/182	+5	C, M	18	D, P, F
25	1024 x 4	**Am91L24B**	450	262/105	330/121	+5	C, M	18	D, P, F
26	1024 x 4	**Am9124C**	300	362/157	440/182	+5	C, M	18	D, P, F
27	1024 x 4	**Am91L24C**	300	262/105	330/121	+5	C, M	18	D, P, F
28	1024 x 4	**Am9124E**	200	367/157		+5	C	18	D, P
29	1024 x 4	**Am9130A**[2]	500	578/84	687/178	+5	C, M	22	D, F
30	1024 x 4	**Am91L30A**[2]	500	367/72	440/136	+5	C, M	22	D, F
31	1024 x 4	**Am9130B**[2]	400	578/84	687/178	+5	C, M	22	D, F
32	1024 x 4	**Am91L30B**[2]	400	367/72	440/136	+5	C, M	22	D, F
33	1024 x 4	**Am9130C**[2]	300	578/84	687/178	+5	C, M	22	D, F
34	1024 x 4	**Am91L30C**[2]	300	367/72	440/136	+5	C, M	22	D, F
35	1024 x 4	**Am9130D**[2]	250	578/84		+5	C	22	D
36	1024 x 4	**Am91L30D**[2]	250	367/72		+5	C	22	D
37	1024 x 4	**Am9130E**[2]	200	578/84		+5	C	22	D
38	1024 x 4	**Am9131A**[2]	500	578/84	687/178	+5	C, M	22	D, F
39	1024 x 4	**Am91L31A**[2]	500	367/72	440/136	+5	C, M	22	D, F
40	1024 x 4	**Am9131B**[2]	400	578/84	687/178	+5	C, M	22	D, F
41	1024 x 4	**Am91L31B**[2]	400	367/72	440/136	+5	C, M	22	D, F
42	1024 x 4	**Am9131C**[2]	300	578/84	687/178	+5	C, M	22	D, F
43	1024 x 4	**Am91L31C**[2]	300	367/72	440/136	+5	C, M	22	D, F
44	1024 x 4	**Am9131D**[2]	250	578/84		+5	C	22	D
45	1024 x 4	**Am91L31D**[2]	250	367/72		+5	C	22	D
46	1024 x 4	**Am9131E**[2]	200	578/84		+5	C	22	D

Notes: 1. See connection diagram within this section.
2. Not recommended for new designs; use equivalent Am9124 product.

MEMORY
MOS

RAMs

Item	Organization	Part Number	Access Time ns (Max)	Power Dissipation COM Act/Stby mW (Max)	Power Dissipation MIL Act/Stby mW (Max)	Supply Voltage V	Temperature Range	Number of Pins[1]	Package(s)
1	4096 x 1	**Am9044B**	450	385/	440/	+5	C, M	18	D, P
2	4096 x 1	**Am90L44B**	450	275/	330/	+5	C, M	18	D, P
3	4096 x 1	**Am9044C**	300	385/	440/	+5	C, M	18	D, P
4	4096 x 1	**Am90L44C**	300	275/	330/	+5	C, M	18	D, P
5	4096 x 1	**Am9044E**	200	385/		+5	C	18	D, P
6	4096 x 1	**Am9140A**[2]	500	578/84	687/178	+5	C, M	22	D, F
7	4096 x 1	**Am91L40A**[2]	500	367/72	440/136	+5	C, M	22	D, F
8	4096 x 1	**Am9140B**[2]	400	578/84	687/178	+5	C, M	22	D, F
9	4096 x 1	**Am91L40B**[2]	400	367/72	440/136	+5	C, M	22	D, F
10	4096 x 1	**Am9140C**[2]	300	578/84	687/178	+5	C, M	22	D, F
11	4096 x 1	**Am91L40C**[2]	300	367/72	440/136	+5	C, M	22	D, F
12	4096 x 1	**Am9140D**[2]	250	578/84		+5	C	22	D
13	4096 x 1	**Am91L40D**[2]	250	367/72		+5	C	22	D
14	4096 x 1	**Am9140E**[2]	200	578/84		+5	C	22	D
15	4096 x 1	**Am9141A**[2]	500	578/84	687/178	+5	C, M	22	D, F
16	4096 x 1	**Am91L41A**[2]	500	367/72	440/136	+5	C, M	22	D, F
17	4096 x 1	**Am9141B**[2]	400	578/84	687/178	+5	C, M	22	D, F
18	4096 x 1	**Am91L41B**[2]	400	367/72	440/136	+5	C, M	22	D, F
19	4096 x 1	**Am9141C**[2]	300	578/84	687/178	+5	C, M	22	D, F
20	4096 x 1	**Am91L41C**[2]	300	367/72	440/136	+5	C, M	22	D, F
21	4096 x 1	**Am9141D**[2]	250	578/84		+5	C	22	D
22	4096 x 1	**Am91L41D**[2]	250	367/72		+5	C	22	D
23	4096 x 1	**Am9141E**[2]	200	578/84		+5	C	22	D
24	4096 x 1	**Am9147-55**	55	990/165		+5	C, M	18	D, P
25	4096 x 1	**Am9147-70**	70	880/110		+5	C, M	18	D, P
26	4096 x 1	**Am9244B**	450	385/165	440/182	+5	C, M	18	D, P
27	4096 x 1	**Am92L44B**	450	275/110	330/121	+5	C, M	18	D, P
28	4096 x 1	**Am9244C**	300	385/165	440/182	+5	C, M	18	D, P
29	4096 x 1	**Am92L44C**	300	275/110	330/121	+5	C, M	18	D, P
30	4096 x 1	**Am9244E**	200	385/165		+5	C	18	D, P
Dynamic									
31	16384 x 1	**Am9016C**	300	175/8.0	462/19.8	+12, ±5	C, L	16	D, P, Z
32	16384 x 1	**Am9016D**	250	175/8.0	462/19.8	+12, ±5	C, L	16	D, P, Z
33	16384 x 1	**Am9016E**	200	175/8.0	462/19.8	+12, ±5	C, L	16	D, P, Z
34	16384 x 1	**Am9016F**	150	175/8.0	462/19.8	+12, +5	C, L	16	D, P, Z

Notes: 1. See connection diagram within this section.
2. Not recommended for new designs; use equivalent Am9244 product.

MEMORY
MOS

Static ROMs

Item	Organization	Part Number	Access Time ns (Max)	Active Power Dissipation COM mW (Max)	MIL mW (Max)	Outputs	Supply Voltage(s) V	Number of Pins	Package(s)
1	512 x 8	**Am9214**	500	263	263	3S	+5	24	D
2	1024 x 8	**Am9208B**	400	605	668	3S	+5, +12	24	D, P
3	2048 x 8	**Am9216C**	300	756		3S	+5, +12	24	D
4	2048 x 8	**Am9216B**	400	655		3S	+5, +12	24	D
5	2048 x 8	**Am9217B**	450	368	440	3S	+5	24	D, P
6	2048 x 8	**Am9217A**	550	368	440	3S	+5	24	D, P
7	2048 x 8	**Am9218C**	350	368		3S	+5	24	D, P
8	2048 x 8	**Am9218B**	450	368	440	3S	+5	24	D, P
9	4096 x 8	**Am9232C**[4]	300	420		3S	+5	24	D, P
10	4096 x 8	**Am9232B**[4]	450	420	550	3S	+5	24	D, P
11	4096 x 8	**Am9233C**[5]	300	420		3S	+5	24	D, P
12	4096 x 8	**Am9233B**[5]	450	420	550	3S	+5	24	D, P
13	8192 x 8	**Am9264C**[1]	300	220[2]		3S	+5	24	D, P
14	8192 x 8	**Am9264B**[1]	450	220[2]	275	3S	+5	24	D, P
15	8192 x 8	**Am9265C**[1]	300	220[2]		3S	+5	28	D, P
16	8192 x 8	**Am9265B**[1]	450	220[2]	275	3S	+5	28	D, P

3

UV Erasable PROMs

Item	Organization	Part Number	Access Time ns (Max)	Power Dissipation Active mW (Max)	Standby mW (Max)	Outputs	Supply Voltage(s) V	Temperature Range	Number of Pins	Package
17	256 x 8	**Am1702A**	1000	676		3S	−9, +5	C, L	24	D
18	256 x 8	**Am1702AL**	1000	676	Clocked V_{GG}	3S	−9, +5	C, L	24	D
19	256 x 8	**Am1702A-1**	550	676	Clocked V_{GG}	3S	−9, +5	C, L	24	D
20	256 x 8	**Am1702AL-1**	550	676	Clocked V_{GG}	3S	−9, +5	C, L	24	D
21	256 x 8	**Am1702A-2**	650	676	Clocked V_{GG}	3S	−9, +5	C, L	24	D
22	256 x 8	**Am1702AL-2**	650	676	Clocked V_{GG}	3S	−9, +5	C, L	24	D
23	1024 x 8	**Am9708/2708**	450	800		3S	+12, +5	C, M	24	D
24	1024 x 8	**Am2708-1**	350	800		3S	+12, +5	C	24	D
25	2048 x 8	**Am2716**	450	525	132	3S	+5	C, M	24[3]	D
26	2048 x 8	**Am2716-1**	350	525	132	3S	+5	C	24[3]	D
27	2048 x 8	**Am2716-2**	390	525	132	3S	+5	C	24[3]	D
28	4096 x 8	**Am2732**	450	787	157	3S	+5	C, L	24[3]	D

FIFOs

Item	Organization	Part Number	Serial I/O	Fullness Flag	Output Enable	Data Rate MHz (Min)	Temperature Range	Number of Pins	Package(s)
29	32 x 8	**Am2812**	Yes	Yes	Yes	0.5	C, L	28	D
30	32 x 8	**Am2812A**	Yes	Yes	Yes	1.0	C, L	28	D
31	32 x 9	**Am2813**	No	Yes	Yes	0.5	C, L	28	D
32	32 x 9	**Am2813A**	No	Yes	Yes	1.0	C, L	28	D
33	64 x 4	**Am2841/3341**	No	No	No	1.0	C, M	16	D, P
34	64 x 4	**Am2841A/3341A**	No	No	No	1.2	C	16	D, P

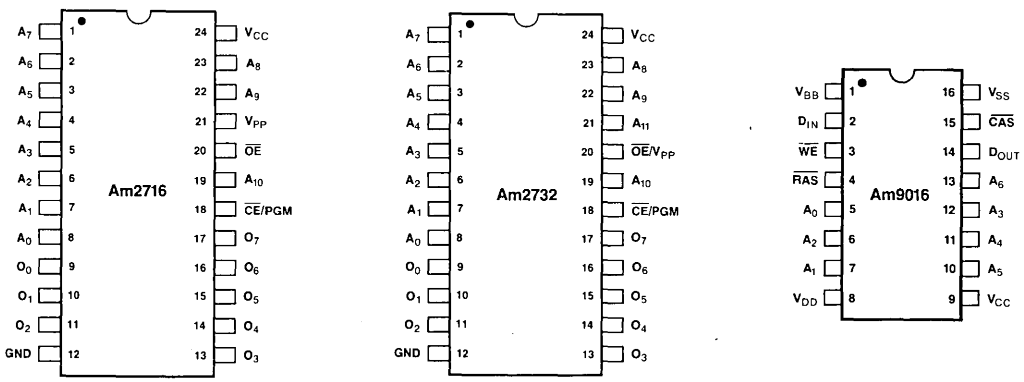
Notes: 1. To be announced.
2. Standby Power Dissipation: 83mW for commercial, 135mW for military.
3. See connection diagram within this secton.
4. Pin compatible with 2532 EPROM.
5. Pin compatible with 2732 EPROM.

MEMORY
MOS

Shift Registers

Item	Capacity/ Organization	Part Number	Mode	Clock Freq. MHz (Max)	Clock Phases	TTL Clocks	Refresh Logic	Output	Supply Voltage(s) V	Number of Pins	Package(s)
1	Dual 100	**Am1507**	Dynamic	2.0	Two	No	No	Single-ended	±5	8	H
2	Quad 256	**Am2802/1402A**	Dynamic	10	Two	No	No	Single-ended	±5	16	D, P
3	Dual 512	**Am2803/1403A**	Dynamic	10	Two	No	No	Single-ended	±5	8	H, P
4	Single 1024	**Am2804/1404A**	Dynamic	10	Two	No	No	Single-ended	±5	8	H, D, P
5	Single 512	**Am2807**	Dynamic	4.0	Two	No	Yes	Single-ended	±5	8	H, P
6	Single 1024	**Am2806/2808**	Dynamic	4.0	Two	No	Yes	Single-ended	±5	10/8	H, D, P
7	Dual 1024	**Am9401/2401**	Static	2.0	One	Yes	Yes	Single-ended	±5	16	D, P
8	Dual 128	**Am2809**	Static	2.5	One	Yes	Yes	Push-pull	+5, −12	8	P
9	Dual 128	**Am2814**	Static	2.5	One	Yes	Yes	Push-pull	+5, −12	16	D, P
10	Single 1024	**Am2833/ 2533/5058**	Static	2.0	One	Yes	Yes	Push-pull	+5, −12	8	D, P
11	Quad 80	**Am2847/3347**	Static	3.0	One	Yes	Yes	Push-pull	+5, −12	16	D, P
12	Quad 128	**Am2855/5055**	Static	2.5	One	Yes	Yes	Push-pull	+5, −12	16	D, P
13	Dual 256	**Am2856/5056**	Static	2.5	One	Yes	Yes	Push-pull	+5, −12	10	H, P
14	Single 512	**Am2857/5057**	Static	2.5	One	Yes	Yes	Push-pull	+5, −12	8	D, P
15	Quad 96	**Am2896**	Static	3.0	One	Yes	Yes	Push-pull	+5, −12	16	D, P
16	Single 2048	**Am2827**	Dynamic	6.0	Two	No	Yes	Push-pull	+5, −10.5	8	D, P

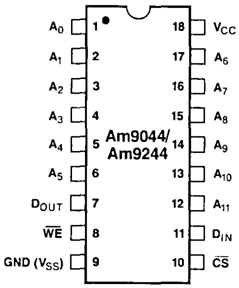
CONNECTION DIAGRAMS (Top Views)

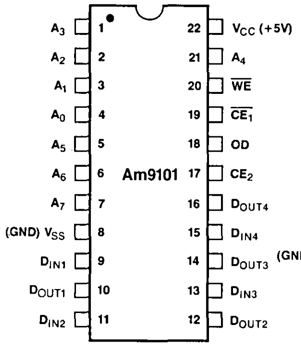


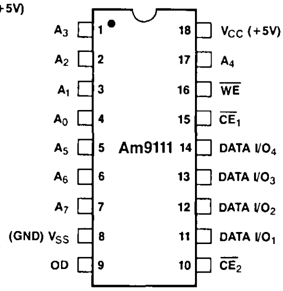
Note: Pin 1 is marked for orientation.

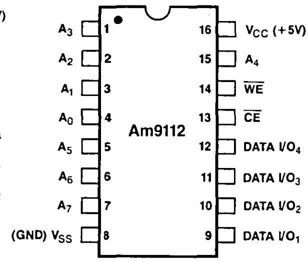
3

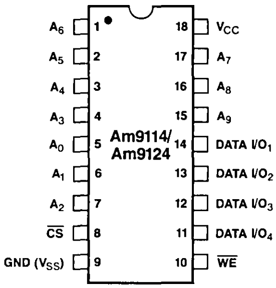
CONNECTION DIAGRAMS (Top Views)

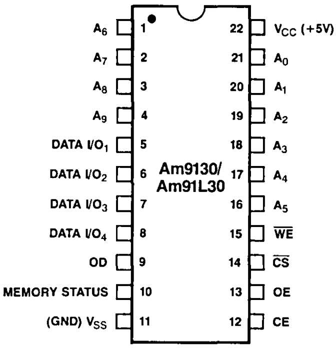


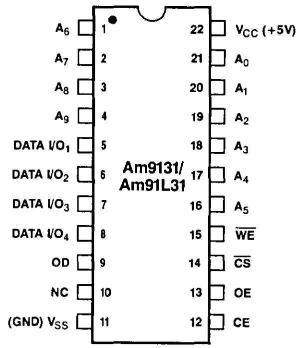


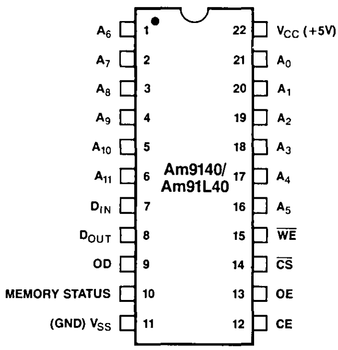


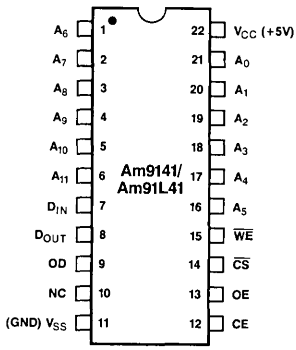


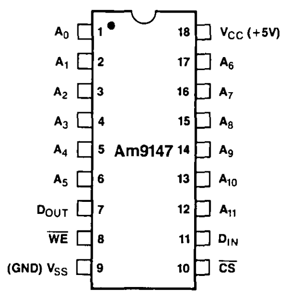












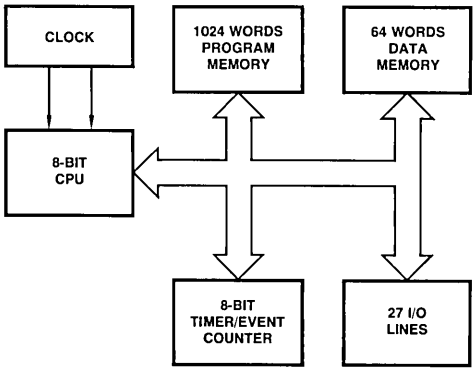
Note: Pin 1 is marked for orientation.

MICROCOMPUTERS

Am8048/Am8035 Single-Chip 8-Bit Microcomputers

The Am8048 and Am8035 are single-chip, 8-bit microcomputers designed for use as efficient controllers. The Am8048 contains an 8-bit CPU, a 1K x 8 ROM Program Memory, a 64 x 8 RAM Data Memory, 27 I/O lines, an 8-bit Timer/Event Counter and on-board oscillator and clock circuits. Standard memory devices and Am8080A/Am9080A peripherals can be added for systems requiring expanded memory and I/O capability. The Am8035 is the equivalent of the Am8048 except that it has no internal program memory.

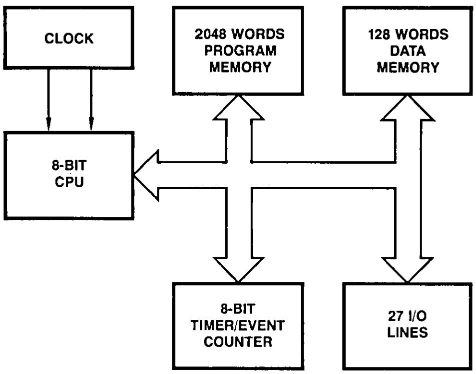
Both microcomputers have extensive bit-handling capability as well as facilities for both binary and BCD arithmetic. The instruction set contains over 90 instructions: 70% are single byte, the balance are two bytes. All instructions can be executed in one or two cycles; both 2.5μs and 4.17μs cycle versions are available. The Am8048 and Am8035 require a single, 5V supply and are available in either a plastic or hermetic 40-pin DIP.



Am8049/Am8039 Single-Chip 8-Bit Microcomputers

The Am8049 and Am8039 are single-chip, 8-bit microcomputers designed for use as efficient controllers. The Am8049 contains an 8-bit CPU, a 2K x 8 ROM Program Memory, a 128 x 8 RAM Data Memory, 27 I/O lines, an 8-bit Timer/Event Counter and on-board oscillator and clock circuits. Standard memory devices and Am8080A/Am9080A peripherals can be added for systems requiring expanded memory and I/O capability. The Am8039 is the equivalent of the Am8049 except that is has no internal program memory.

Both microcomputers have extensive bit-handling capability as well as facilities for both binary and BCD arithmetic. The instruction set contains over 90 instructions: 70% are single byte, the balance are two bytes. All instructions can be executed in one or two cycles; both 1.36μs and 2.5μs cycle versions are available. The Am8049 and Am8039 require a single, 5V supply and are available in either a plastic or hermetic 40-pin DIP.



4

CENTRAL PROCESSING UNITS

Am8080A/Am9080A 8-Bit Central Processing Unit (CPU)

The Am8080A/Am9080A is an 8-bit parallel central processing unit designed to perform a wide variety of operations, ranging from complex arithmetic calculations to character handling to bit control. Various speed options, including a high speed version with a 1.0μs instruction cycle time, are available.

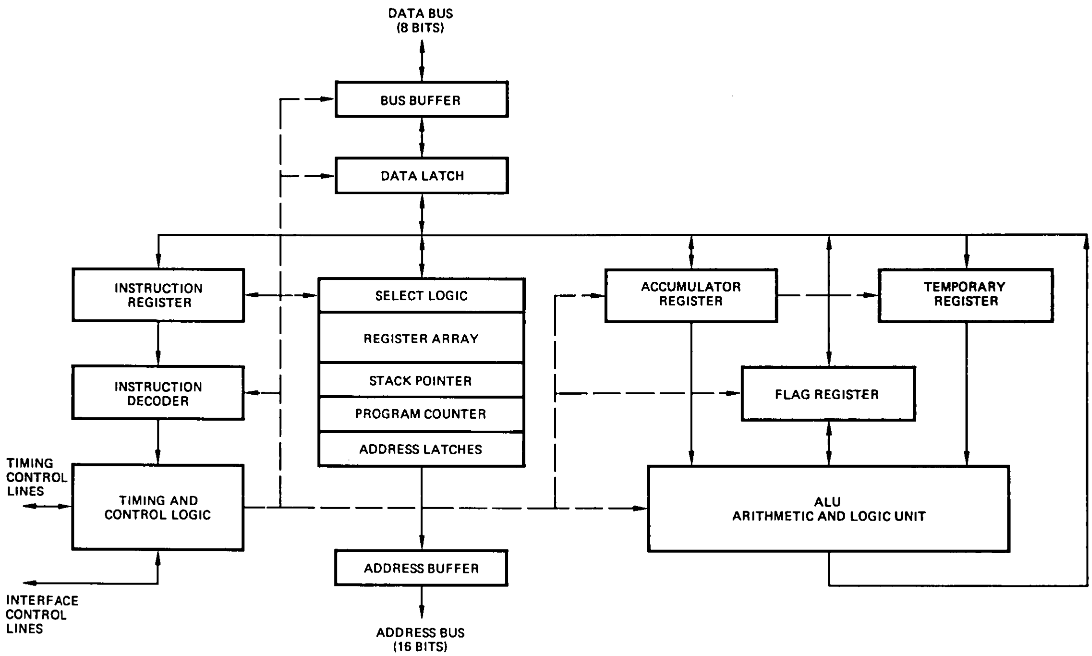
The CPU contains a 16-bit Program Counter which can directly address up to 64K bytes of memory through the 16-line address bus. The addressed memory may be any combination of read/write and read-only. A separate 8-line bidirectional data bus transfers instructions, data and status information between system devices. All transfers are handled using asynchronous handshaking controls so that any speed memory or I/O device is easily accommodated. Data and address busses may be OR-tied with other controlling devices for direct memory access or multiprocessor operation.

An accumulator plus six general-purpose registers are available to the programmer. The six registers are each eight bits long and may be used singly or in pairs for both 8 and 16-bit operations. The accumulator forms the primary working register and is the destination for many of the arithmetic and logic operations.

A general-purpose push-down stack is an important part of the microprocessor system architecture. The contents of the stack reside in R/W memory; an on-chip 16-bit Stack Pointer controls the addressing of this external stack. Subroutine call and return instructions automatically use the stack to store and retrieve the contents of the accumulator, flags, program counter and all of the six general-purpose registers. Push and Pop instructions allow direct use of the stack for storing operands, passing parameters and saving machine state.

An asynchronous vectored interrupt capability is included to allow external signals to modify the instruction stream. The interrupting device may specify an interrupt instruction to be executed and may thus vector the program to a particular service location, or to perform some other direct function.

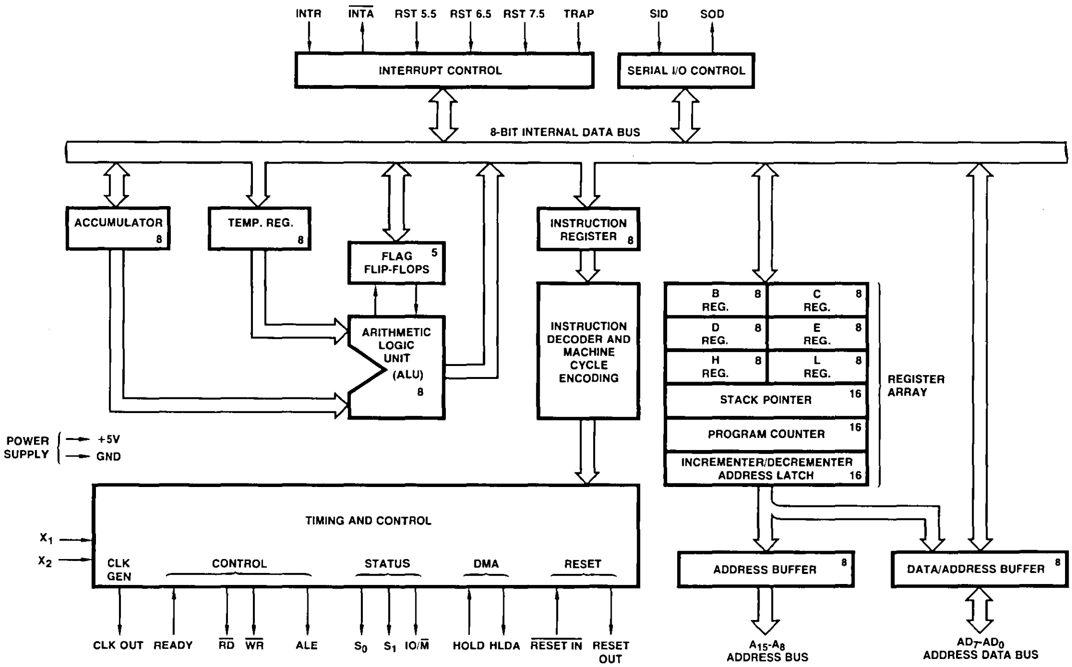
The Am8080A/Am9080A is available in either a plastic or hermetic 40-pin DIP.



Am8085A 8-Bit Central Processing Unit (CPU)

The Am8085A is an advanced, complete 8-bit parallel central processing unit. It is available with either 1.3μs or 0.8μs instruction cycle time and is 100% software compatible with the Am8080A/Am9080A.

The Am8085A incorporates a clock generator and system controller on-chip, thereby offering a high level of system integration. Additional enhancements include interrupt control logic, consisting of four vectored interrupts, and serial I/O lines. The Am8085A uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus. Up to 64K bytes of memory can be directly addressed. The CPU requires a single, 5V supply and is available in either a plastic or hermetic 40-pin DIP.



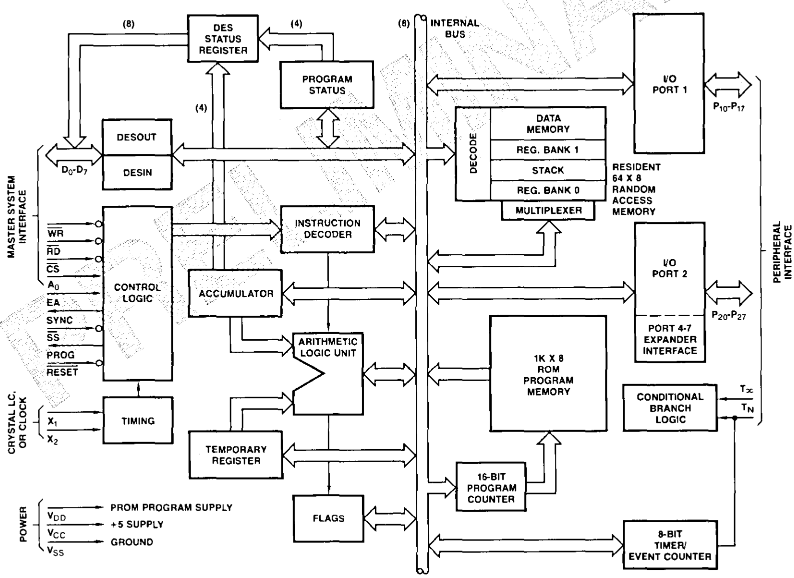
PERIPHERAL DEVICES

Am8041A Universal Peripheral Interface

The Am8041A is a general-purpose interface device designed to be an efficient controller as well as an arithmetic processor. It is a complete microcomputer and, therefore, provides more flexibility for the designer than conventional LSI interface devices.

The Am8041A contains 1K x 8 ROM Program Memory, 64 x 8 RAM Data Memory, an 8-bit CPU, 16 I/O lines, an 8-bit programmable Timer/Event Counter, clock and interface registers. The UPI has two 8-bit I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. The timer/event counter generates timing sequences or counts external inputs.

The Am8041A requires a single, 5V supply and is available in either a plastic or hermetic 40-pin DIP.

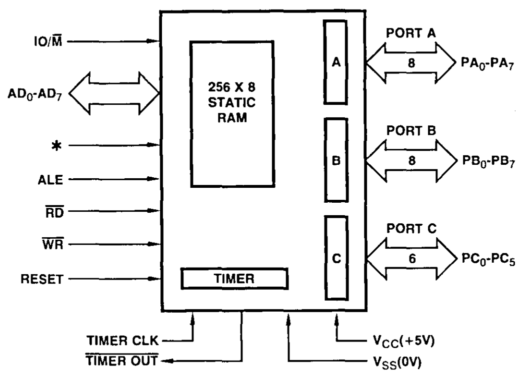


Am8155/Am8156 RAM with I/O Ports and Timer

The Am8155 and Am8156 static RAMs with I/O ports and timer are designed to directly interface with the Am8085A CPU in an 8-bit microprocessor system. They differ only in the polarity of the Chip Enable (CE) input: active-LOW for the Am8155, active-HIGH for the Am8156.

The RAM portion, 2K-bit static cells organized as 256 x 8, has a maximum access time of 400ns, thus requiring no wait states in the Am8085A CPU. The I/O portion consists of three general-purpose I/O ports. One port can be programmed to act as status pins, thus allowing the other two ports to operate in a handshake mode. An on-chip, programmable counter/timer provides either a square wave or terminal count pulse for the CPU, depending on the timer mode.

The Am8155 and Am8156 are also available in a higher speed version. Both require a single, 5V supply and are packaged in a plastic or hermetic 40-pin DIP.



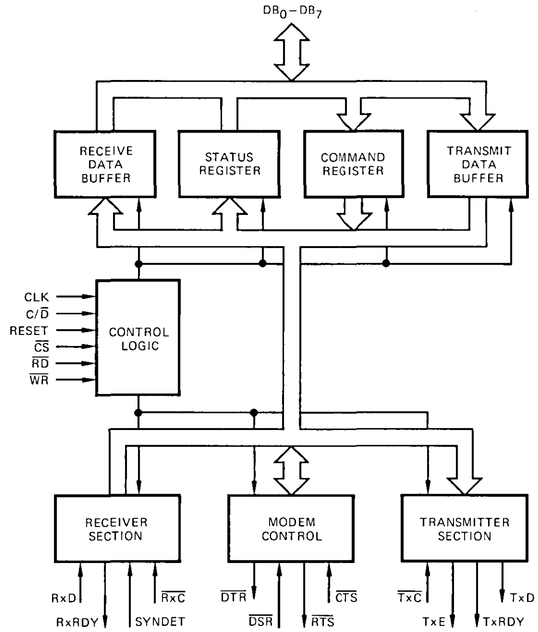
*Am8155 = $\overline{CE}$, Am8156 = CE.

Am8251/Am9551 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Am8251/Am9551 is a programmable serial data communications interface that provides a universal synchronous/asynchronous receiver/transmitter function. It is normally used as a peripheral device for an 8-bit microprocessor system and may be programmed by the CPU to operate in a variety of standard serial communication formats.

Data, control, operation and format options are all selected by commands from the CPU. The USART can operate in an independent full duplex mode. It accepts parallel data from the CPU, formats and serializes the information based on its current operating mode, and then transmits the data as a serial bit stream. Simultaneously, serial data can be received, converted into parallel form, de-formatted, and then presented to the CPU. The Am8251/Am9551 is doubled buffered and can operate at clock frequencies of up to 2.8MHz.

The USART requires a single, 5V supply and is available in a 28-pin plastic or hermetic DIP.

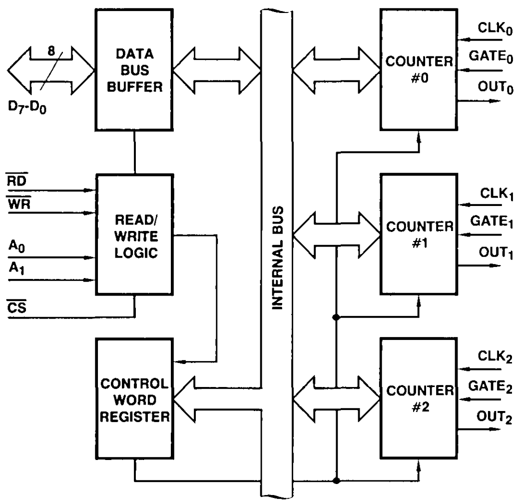


Am8253 Programmable Interval Timer

The Am8253 programmable interval timer/counter functions as a general-purpose, multitiming element in Am8080A/Am9080A and Am8085A microprocessor systems.

It is organized as three independent 16-bit counters, each with a count rate of up to 2.5MHz. A faster device, Am8253-5, allows full compatibility with the Am8085A. All modes of operation are software programmable.

The Am8253 requires a single, 5V supply and is available in a plastic or hermetic 24-pin DIP. For improved performance, see the Am9513 System Timing Controller.

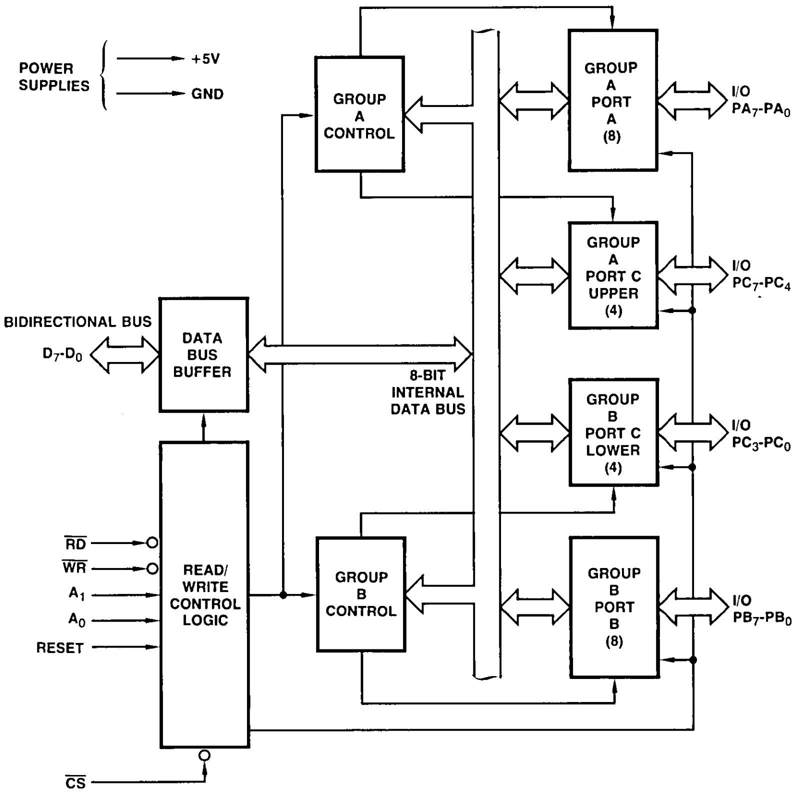


Am8255A Programmable Peripheral Interface (PPI)

The Am8255A programmable peripheral interface functions as a general-purpose I/O component to interface peripheral equipment to the microcomputer data bus in Am8080A/Am9080A and Am8085A microprocessor systems. The functional configuration of the Am8255A is programmed by the system software so that generally no external logic is necessary.

The PPI has 24 I/O pins which may be individually programmed in two groups of 12 and used in three major modes of operation. In the first mode, each group of I/O pins may be programmed in sets of four and eight to be inputs or outputs. In the second mode, each group may be programmed to have eight input or output lines. Three of the remaining four pins are used for handshaking and interrupt control signals. The third mode is the bidirectional bus mode; it uses eight lines for a bidirectional data bus and five lines, borrowing one from the other group, for handshaking.

The Am8255A is available in two speed versions, requires a single 5V supply and is packaged in either a plastic or hermetic 40-pin DIP.

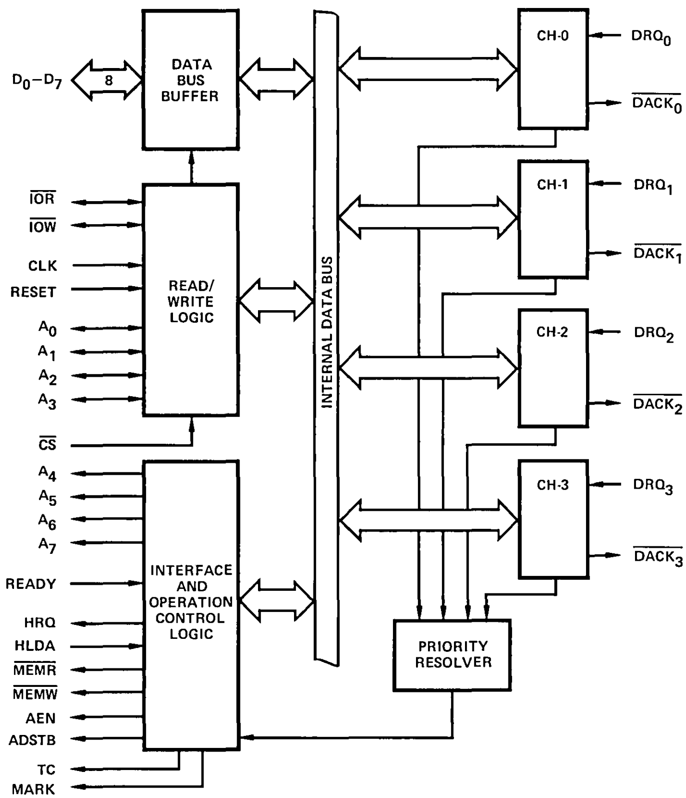


Am8257/Am9557 Direct Memory Access (DMA) Controller

The Am8257/Am9557 is a 4-channel direct memory access controller which permits the high-speed transfer of data directly between peripherals and memory in microcomputer systems.

When peripheral requests are received, the Am8257/Am9557 issues a HOLD signal to the host CPU, assumes control of the system busses, selects the highest priority peripheral for servicing, and generates the necessary control signals and memory address required for the data transfer. It maintains a byte count for each channel and issues a terminal count signal upon completion of the programmed number of transfers.

The Am8257/Am9557 requires a single, 5V supply and is available in either a plastic or hermetic 40-pin DIP. For improved functional and performance characteristics, see the Am9517A Multimode DMA controller.

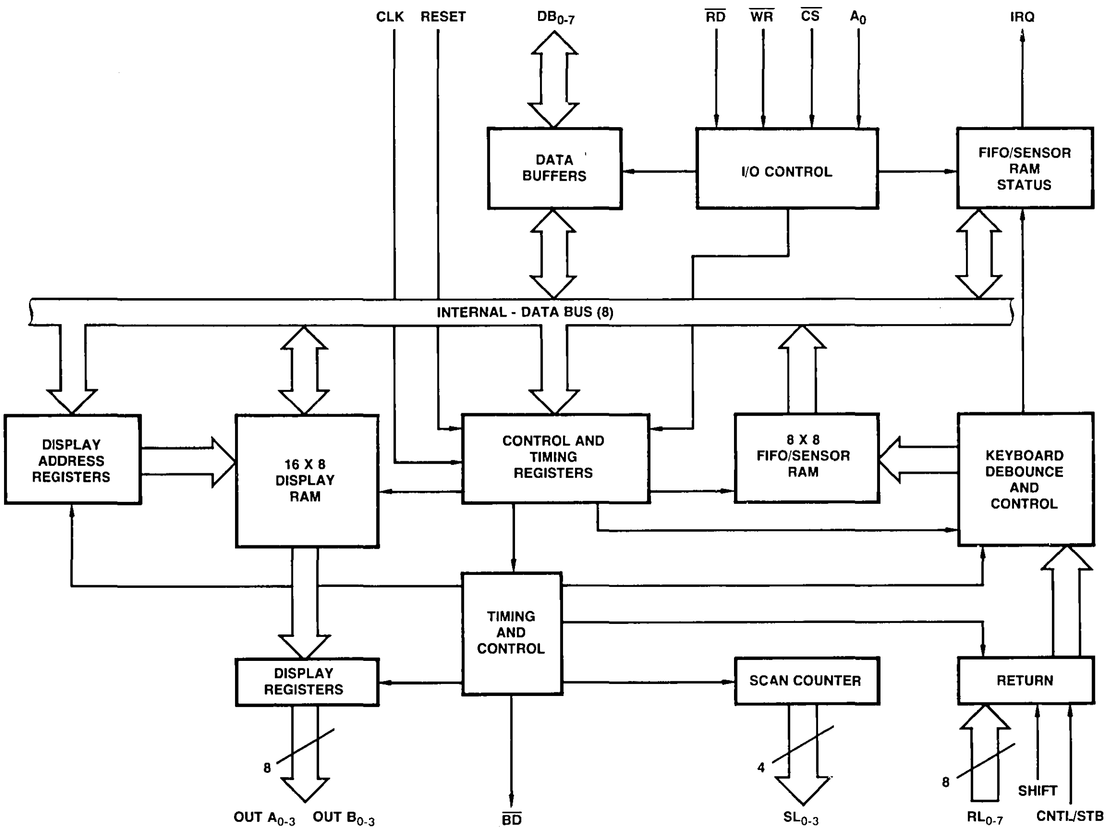


Am8279 Keyboard/Display

The Am8279 programmable keyboard/display I/O interface controls data input and display functions in microprocessor systems. It connects directly to the microcomputer data bus and all operating modes are CPU programmable.

The Am8279 has two sections: keyboard and display. The keyboard portion can provide a scanned interface to a 64-contact key matrix, a sensor array or a strobed interface keyboard. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. The display portion contains a 16 x 8 Display RAM which can be organized into dual 16 x 4. It provides a scanned display interface for LED, incandescent and other popular display technologies. Both right-entry calculator and left-entry typewriter display formats are possible.

Available in two speed versions, the Am8279 requires a single, 5V supply and is packaged in either a plastic or hermetic 40-pin DIP.

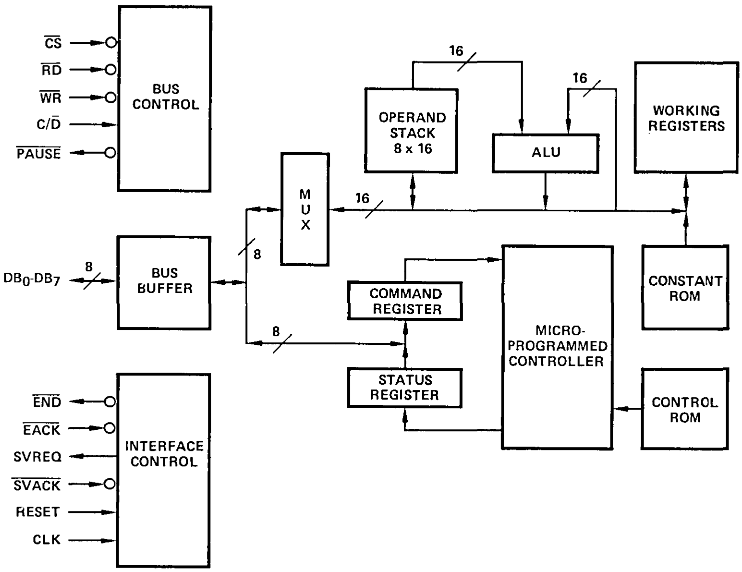


Am9511A Arithmetic Processing Unit (APU)

The Am9511A arithmetic processing unit is used to enhance the computational capability of a wide variety of 8-bit microprocessor systems. It provides high performance 16 and 32-bit fixed-point and 32-bit floating-point arithmetic operations, performs trigonometric and inverse trigonometric functions, and executes a variety of mathematical operations such as square root, logarithm and exponentiation.

Data are transferred to and from the APU via a CPU by using conventional programmed I/O, or by a direct memory access device if higher transfer speeds are required. All transfers, including operand, result, status and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack or additional commands may be entered. Upon completion of each command, the APU issues an end of execution signal; this signal may be used as an interrupt by the CPU to help coordinate program execution.

The Am9511A is available with a 2MHz, 3MHz or 4MHz maximum clock frequency in a hermetic 24-pin DIP.

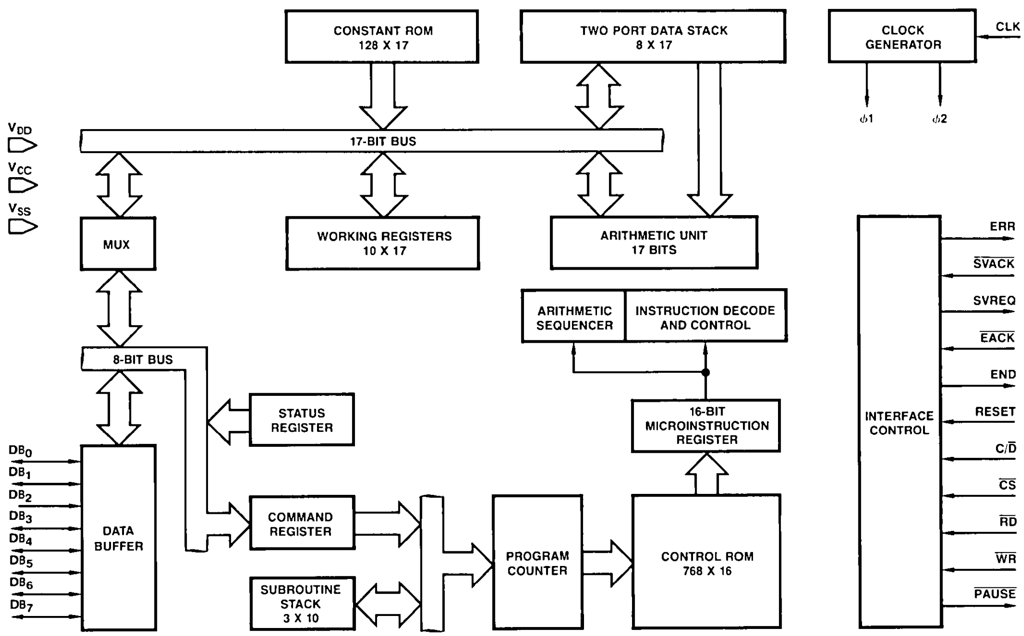


Am9512 Floating-Point Processing Unit (FPU)

The Am9512 floating-point processing unit enhances the computational capability of the CPU in 8-bit microprocessor systems. It provides single precision (32-bit) and double precision (64-bit) add, subtract, multiply and divide operations.

Data are transferred between the Am9512 and the CPU by using programmed I/O or direct memory access techniques. The operand, result, status and command information transfers occur over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack by the CPU and a command is issued to perform an operation on the data stack. The results of this operation are available to the CPU by popping the stack. Upon completion of an operation, the Am9512 issues an end of execution signal; this signal can be used to interrupt the CPU.

The FPU is available in two speed versions and is packaged in a hermetic 24-pin DIP.

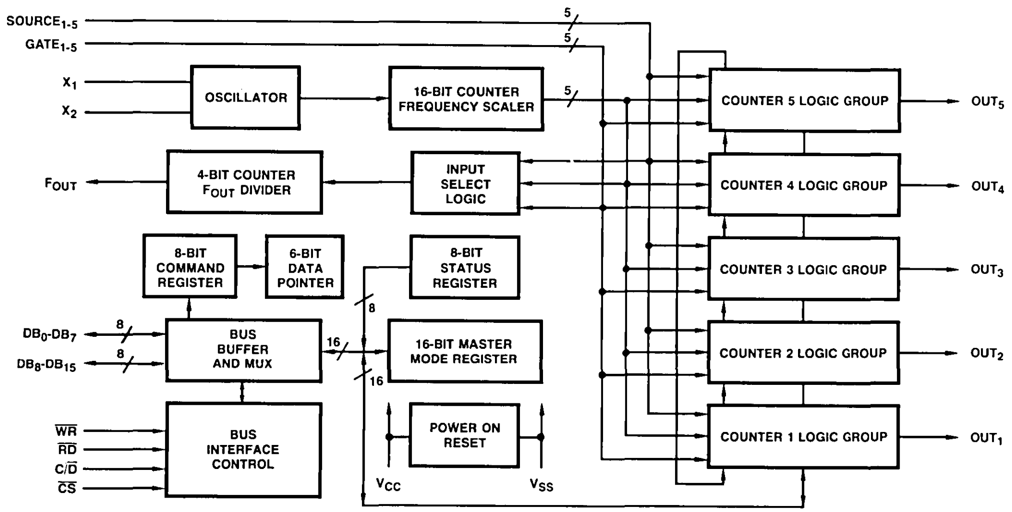


Am9513 System Timing Controller (STC)

The Am9513 system timing controller performs many types of counting, sequencing and timing operations in 8-bit or 16-bit microprocessor systems. It provides the capability for programmable frequency synthesis, high-resolution programmable duty-cycle waveforms, retriggerable digital timing functions, time-of-day clocking, coincidence alarms, complex pulse generation, high-resolution baud-rate generation, frequency shift keying, stopwatch timing, event-count accumulation, waveform analysis and many more. A variety of programmable operating modes and control features allows the Am9513 to be personalized for specific applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-HIGH or active-LOW input polarity. Both hardware and software gating of each counter are available. Three-state outputs for each counter provide pulses or levels and can be active-HIGH or active-LOW. The counters can be programmed to count up or down in either binary or BCD. The CPU may read an accumulated count at any time without disturbing the counting process. Any of the counters may be internally concatenated to form an effective counter length of up to 80 bits.

The Am9513 requires a single, 5V supply and is available in either a plastic or hermetic 40-pin DIP.

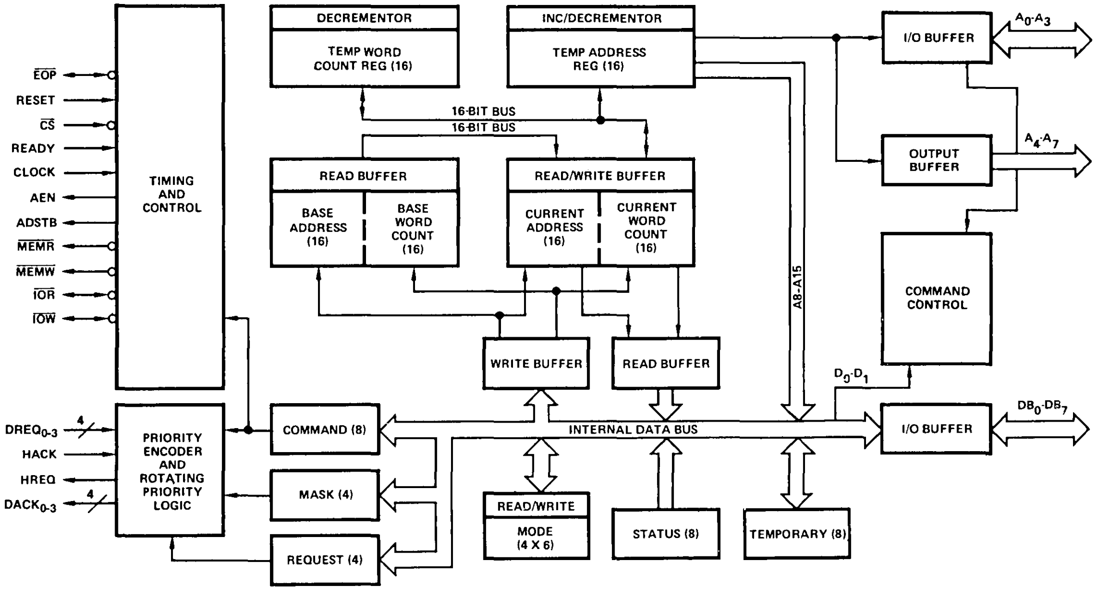


Am9517A Direct Memory Access (DMA) Controller

The Am9517A multimode direct memory access controller improves microprocessor system performance by allowing external devices to directly transfer information to or from the system memory or from memory to memory. It offers a wide variety of programmable control features to enhance data throughput and allow dynamic reconfiguration under program control.

The Am9517A contains four independent DMA channels and can be expanded to any number of channels by cascading additional controller chips. Each channel has 64K address and word count capability and can be individually programmed to autoinitialize to its original condition following an End of Process (EOP). Each of the three active transfer modes – Single Word, Block and Demand – can perform Read, Write and Verify transfers. A memory-to-memory option is provided in addition to the standard memory-peripheral DMA transfer capability.

The DMA controller requires a single, 5V supply and is available in either a plastic or hermetic 40-pin DIP.

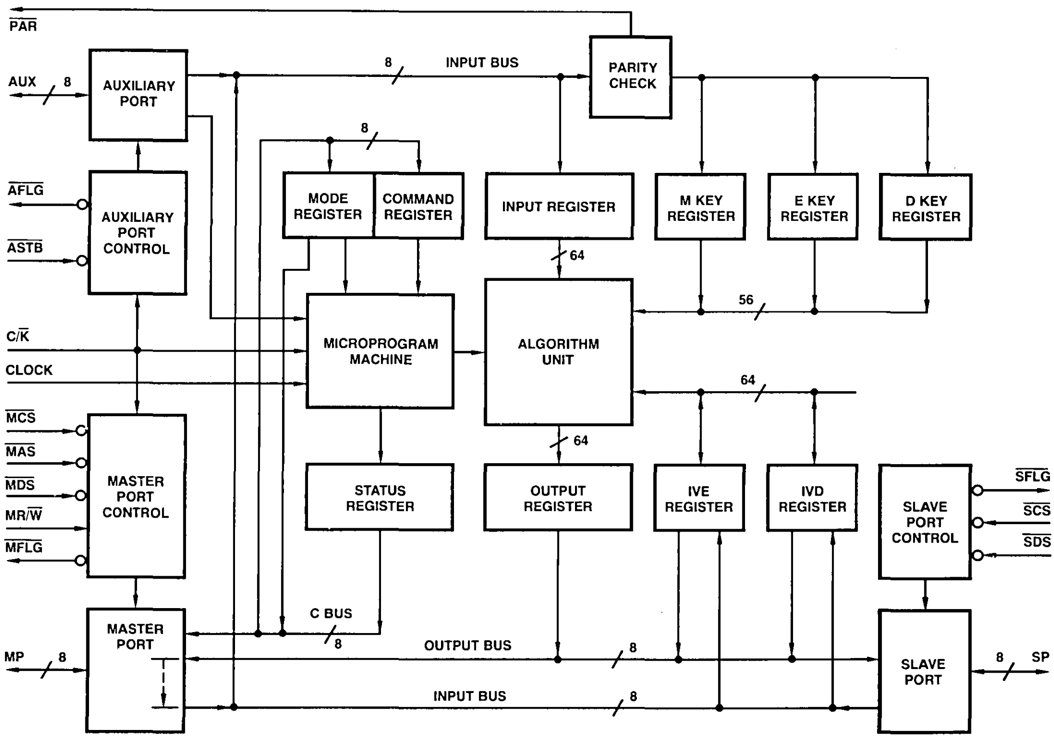


Am9518 Data Ciphering Processor (DCP)

The Am9518 data ciphering processor encrypts and decrypts data using the National Bureau of Standards encryption algorithm. It can be used in a variety of environments including dedicated controllers, communication concentrators, terminals and peripheral task processors in general microprocessor systems. The DCP provides throughput rates greater than one megabyte per second using the Cipher Feedback, Electronic Code Book or Chain Block Cipher operating modes. Separate ports are provided for key input, clear data and enciphered data to enhance security.

The Am9518 can be used in 8 or 16-bit microprocessor systems with the CPU programming the DCP through the master port. The DCP can also be configured to accept control information on dedicated control lines, allowing it to be used in 2900 based bit-slice designs, with the control information derived directly from microcode memory. In either configuration, once set up data can flow through the DCP at high rates because input, output and ciphering activities are performed concurrently. Control lines are provided for interfacing to external DMA devices.

The Am9518 requires a single, 5V supply and is available in either a plastic or hermetic 40-pin DIP.

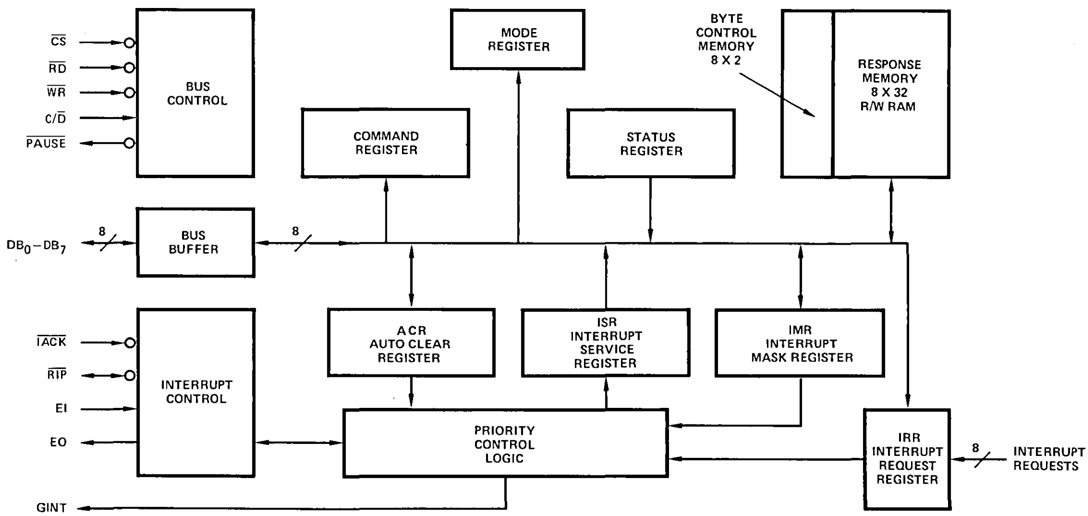


Am9519A Interrupt Controller

The Am9519A universal interrupt controller provides a powerful interrupt structure to increase the efficiency and versatility of microcomputer systems. It contains, on one chip, all of the circuitry necessary to detect, prioritize and manage eight vectored interrupts. Its simple expansion structure allows many units to be cascaded for the control of large numbers of interrupts.

When the Am9519A receives an unmasked Interrupt Request, it issues a Group Interrupt output to the CPU. When the interrupt is acknowledged, the controller outputs the one-to-four byte response associated with the highest priority unmasked interrupt request. Since the response bytes are fully programmable, any instruction or vectoring protocol appropriate for the CPU may be used. The ability of the CPU to set interrupt requests under software control permits hardware prioritization of software tasks and aids system diagnostic and maintenance procedures.

The Am9519A requires a single, 5V supply and is available in either a plastic or hermetic 28-pin DIP.

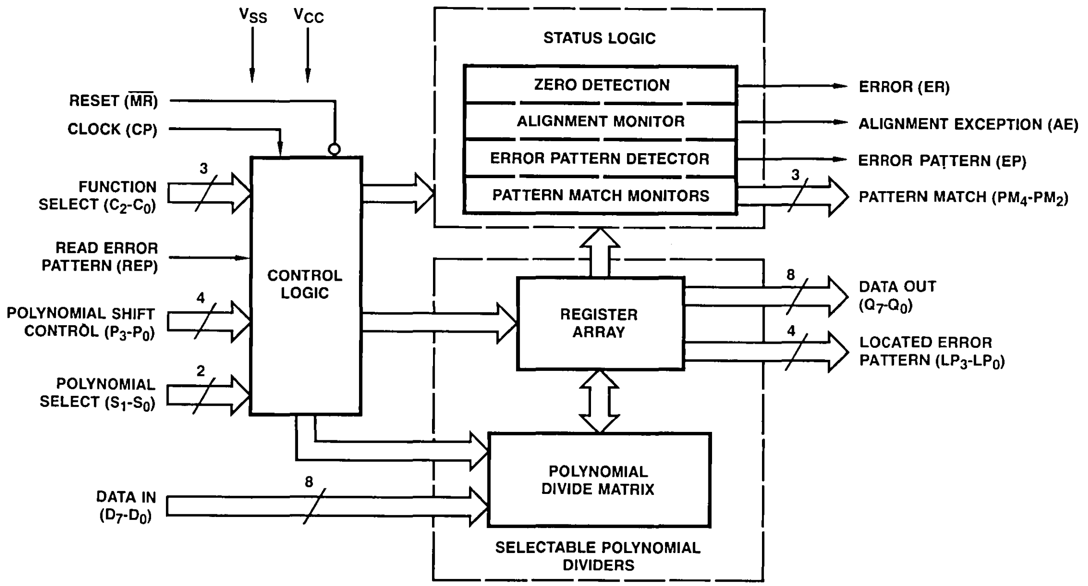


Am9520 Burst Error Processor (BEP)

The Am9520 burst error processor provides a tool for implementing the most common error detection and correction schemes in microprocessor-based digital data-handling systems. Because modern disks use high data recording densities, the probability of errors occuring during data recovery is increased. Burst error detection and correction schemes based on Fire codes are used to correct such errors and to enhance the overall disk system performance.

The Am9520 provides four standard polynomials, including the popular 56-bit and 48-bit versions; logic levels on two inputs select the desired polynomial. For encoding, the data stream is divided by a selected polynomial using rules of algebra in polynomial fields. This division results in a remainder which is appended to the data as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. If an error is detected, the Am9520 will extract the burst error pattern and the location of the burst in the data stream.

The Am9520 requires a single-phase clock and a 5V supply. It is packaged in either a plastic or hermetic 40-pin DIP.



CENTRAL PROCESSING UNITS

AmZ8001 16-Bit Central Processing Unit (CPU)

The AmZ8001 16-bit central processing unit is used in a wide variety of applications ranging from simple stand-alone computers to complex, high-throughput systems. It is organized around sixteen 16-bit general-purpose registers and can directly address up to eight megabytes of memory in each of several address spaces via a 23-bit segmented address. The upper seven bits of address designate the segment number; the lower sixteen bits of address designate an offset within the segment, relative to the start of the segment.

The AmZ8001 implements a powerful instruction set with flexible addressing modes. These instructions operate on seven main data types – bit, BCD digit, byte, word (16-bit), long word (32-bit), byte, string and word string. The CPU can execute instructions in either System (privileged) or Normal (nonprivileged) mode. Code, data and stack address spaces exist for both modes. The AmZ8001 contains on-chip memory refresh and a sophisticated interrupt and trap structure.

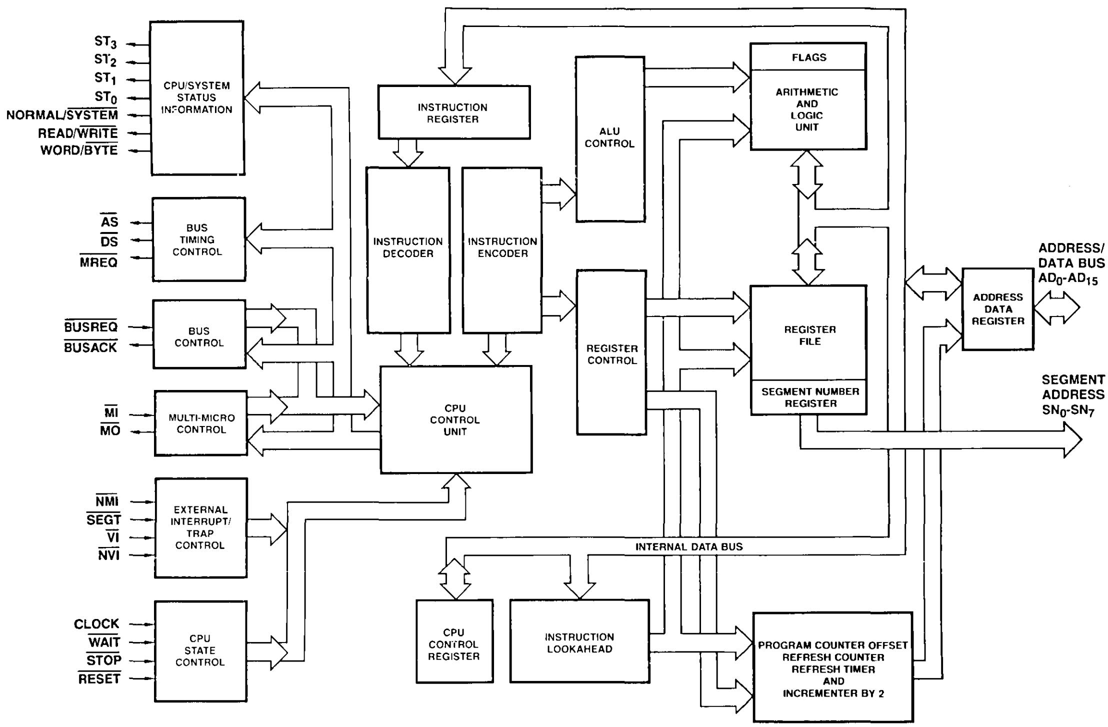
The AmZ8001 is software compatible with the AmZ8002 CPU. It requires a single 5V supply, a single-phase clock and is available in a 48-pin DIP.

AmZ8002 16-Bit Central Processing Unit (CPU)

The AmZ8002 16-bit central processing unit is used in a wide variety of applications ranging from simple stand-alone computers to complex, high-throughput systems. It is organized around sixteen 16-bit general-purpose registers and can directly address up to 64 kilobytes of memory in each of several address spaces via a 16-bit address.

The AmZ8002 implements a powerful instruction set with flexible addressing modes. These instructions operate on seven main data types – bit, BCD digit, byte, word (16-bit), long word (32-bit), byte string and word string. The CPU can execute instructions in either System (privileged) or Normal (nonprivileged) mode. Code, data and stack address spaces exist for both modes. The AmZ8002 contains on-chip memory refresh and a sophisticated interrupt and trap structure.

The AmZ8002 is software compatible with the AmZ8001 CPU. It requires a single 5V supply, a single-phase clock and is available in a 40-pin DIP.



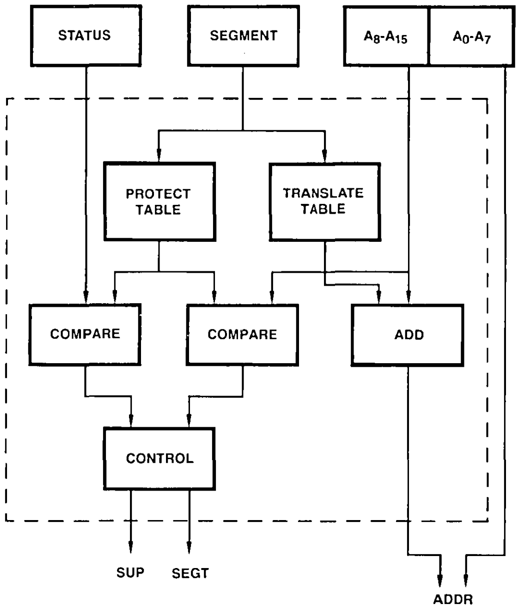
PERIPHERAL DEVICES

AmZ8010 Memory Management Unit (MMU)

The AmZ8010 memory management unit adds sophisticated address translation and memory protection capabilities to AmZ8001 microprocessor systems. The CPU outputs a 7-bit segment number and a 16-bit offset. The MMU uses the segment number to index into an address translation table; the offset is added to the segment base to form the physical address.

A separate attribute table allows the user to individually program segment size from 256 to 64K bytes, in increments of 256 bytes. Access attributes – Read Only, System Mode Only, Invalid Segment, Execute Only and CPU Only (exclude DMA) – are individually programmable for each segment. If an access is attempted which is prohibited by the attributes or which falls outside of the programmed segment size, a trap is issued to the CPU and writes to memory are suppressed.

The AmZ8010 requires a single 5V supply, a single-phase clock and is packaged in a 48-pin DIP.



AmZ8016 Direct Memory Access Transfer Controller (DTC)

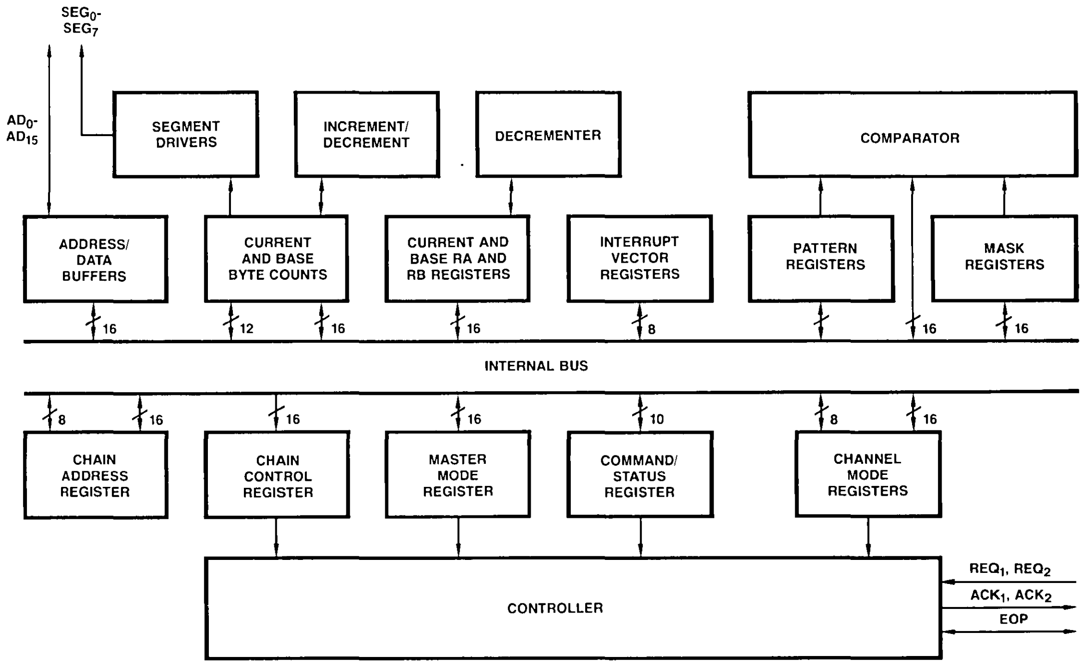
The AmZ8016 2-channel direct memory access transfer controller facilitates the high-speed transfer of data within AmZ8001 and AmZ8002 microcomputer systems. It can generate either logical addresses to be translated by a Memory Management Unit (MMU) or physical addresses for directly addressing up to 16 megabytes of memory.

The AmZ8016 supports two transfer modes – flowthru and flyby – for the transfer of byte or word data. The flowthru mode is used for transferring data between memories and peripherals, between peripherals or from one memory location to another. The flyby mode increases transfer rate but is restricted to transfers between memories and peripherals. A byte/word funneling option in the flowthru mode allows transfers between 8-bit peripherals and 16-bit memory locations. Both 8- and 16-bit pattern searches can be made via the pattern and mask registers. The searching operation can be provided either alone or as a transfer-and-search operation, where variable-length data blocks are transferred until a match occurs.

Each channel in the DTC can load its own control information from a table in memory; one of the control parameters is the address of the next control table. Thus, the channel can sequentially perform a number of DMA tasks chained together in memory without interrupting CPU. Each DTC channel has complete vectored interrupt capability.

The AmZ8016 requires a single 5V supply and is packaged in a 48-pin DIP.

AmZ8016 Direct Memory Access Transfer Controller (Cont.)

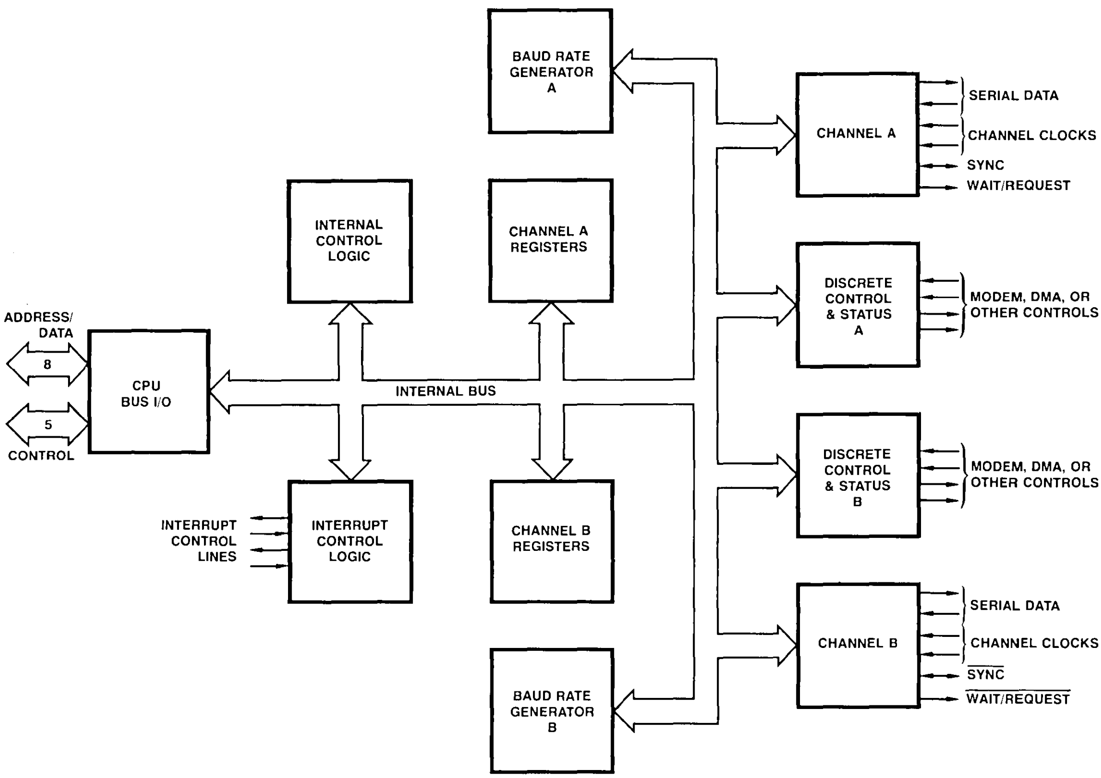


AmZ8030 Serial Communications Controller (SCC)

The AmZ8030 serial communications controller is a dual-channel multifunction data communication peripheral for use in AmZ8001 and AmZ8002 microcomputer systems. It performs serial-to-parallel and parallel-to-serial data conversions for all popular formats including asynchronous, synchronous byte-oriented protocols such as IBM bisync, and synchronous bit-oriented protocols such as HDLC and SDLC. CRC codes are generated and checked in any synchronous mode.

The SCC has two independent full-duplex channels and two baud-rate generators. Each channel has four control signals which can be used for modem control or general-purpose I/O. These signals are monitored by the control logic under program control. Receiver data is quadruple buffered; transmitter data is double buffered.

The AmZ8030's flexible daisy-chain priority interrupt structure allows it to output separate interrupt vector and status information for the transmitter, receiver and External/Status interrupts, allowing it to be easily incorporated into both vectored or polled interrupt environments. It requires a single 5V supply and is packaged in a 40-pin DIP.



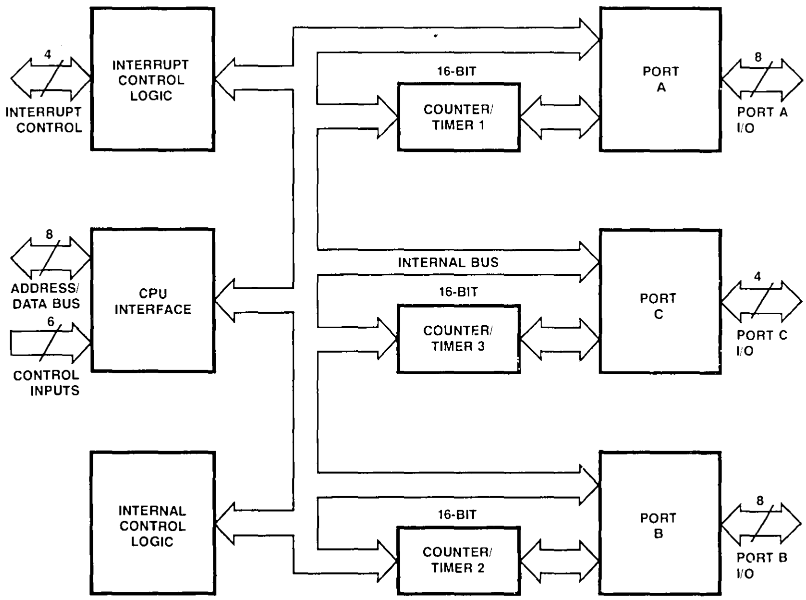
AmZ8036 Counter/Timer and Parallel I/O Unit (CIO)

The AmZ8036 counter/timer and parallel I/O is a general-purpose AmZ8001/AmZ8002 peripheral device which provides three I/O ports (two double-buffered 8-bit and one 4-bit) and three 16-bit counter/timers. In addition, it can be used as an AmZ8000 family interrupt controller.

Either of the two 8-bit I/O ports can be a handshake byte port or a bit port. In the bit mode, data direction is programmable bit by bit. In the handshake mode, the ports can be input, output or bidirectional; they can also be linked to form a 16-bit port. Each 8-bit port includes pattern recognition logic allowing interrupt generation when a specified pattern is detected. The 4-bit port provides handshake controls, special controls (Wait/Request) or general-purpose I/O.

Each of the three counters have a programmable output duty cycle and can operate in single or continuous cycles. Two may be linked internally to provide a 32-bit count length. The counter/timers can count internal clock cycles or external events.

The AmZ8036 requires a single 5V supply and is packaged in a 40-pin DIP.

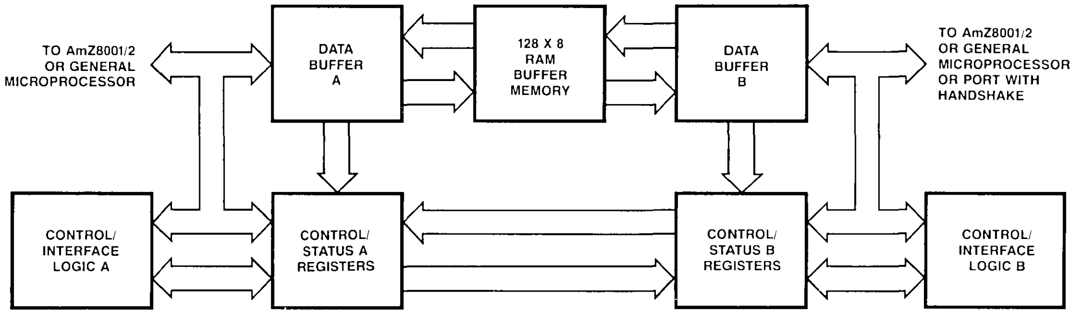


AmZ8038 FIFO Input/Output Interface Unit (FIO)

The AmZ8038 is a general-purpose half-duplex bidirectional FIFO-buffered 8-bit I/O port that provides elastic buffering between asynchronous CPUs in a parallel microprocessor network or between a CPU and peripherals. It is capable of simultaneous, asynchronous, independent read and write operations. The FIO has many programmable operating modes including IEEE-488 and an interlocked mode used to cascade the AmZ8038 in width and, using the AmZ8060 FIFO expander, in depth.

The AmZ8038 has an 8-bit master side which controls the direction of data transfer and an 8-bit slave side which follows the data direction. Common to both is the 128 x 8 RAM used for data storage, two 7-bit counters and various registers. Use of a RAM-based architecture eliminates bubble-through delay, resulting in low propagation delay from input to output. The FIO has several control lines that may be used to interface to a DMA device or to synchronize the servicing microprocessor. Two handshake lines allow direct interfacing to other peripheral devices. Buffer status (FULL and EMPTY) is also available on separate pins. Byte pattern matching with individual bit masking is available to generate an interrupt or to disable data loading. The FIO contains both status and vector information enabling it to operate in vectored or polled interrupt environments.

The AmZ8038 requires a single 5V supply and is packaged in a plastic 40-pin DIP.



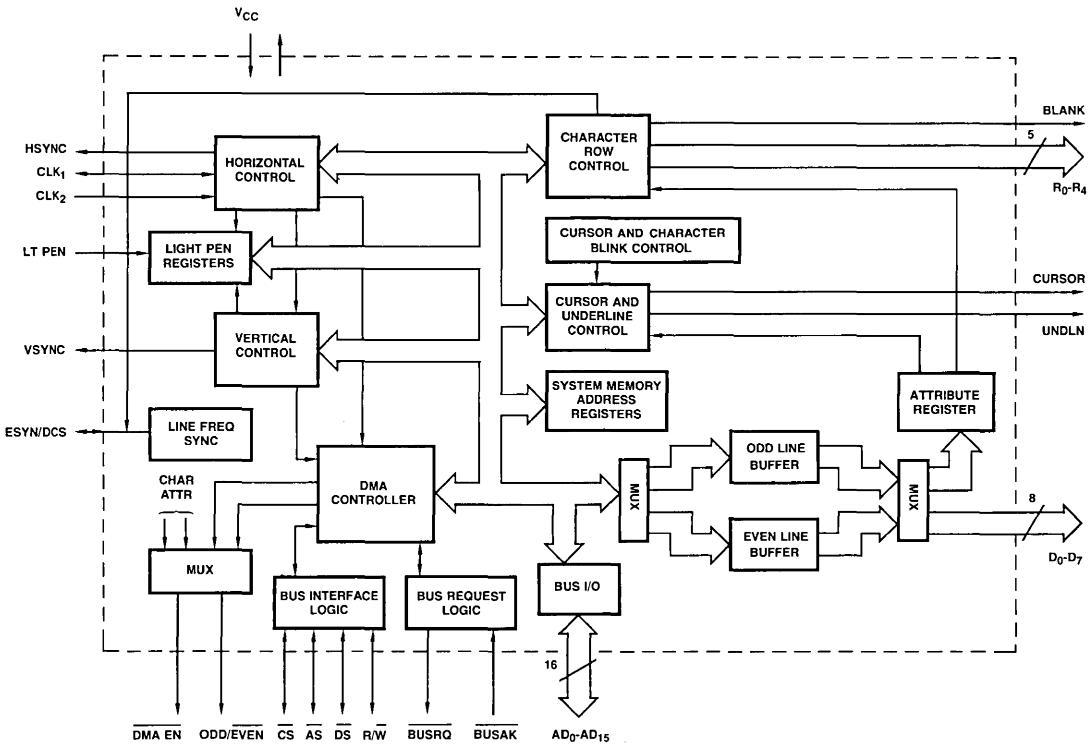
AmZ8052 CRT Controller (CRTC)

The AmZ8052 general-purpose, raster-scan, alphanumeric-display controller provides a unique combination of user programmable features to suit a wide variety of applications including general business and scientific data processing, word processing and graphics.

The CRTC has an on-board direct memory access (DMA) controller to load character data and control information into two on-board 132-character x 16-bit line buffers. Character information is stored in memory on a row by row basis with linked-list addressing used to connect the rows. Control attributes at the start of each character row allow user programming of the number of scan lines used to display the row; the CRTC can generate typewriter-type text spacing or display oversized alphanumeric information. Parallel attributes loaded with each character cell allow single or double underlining, multiple cursors per screen, individual cursor and underline blinking rates, superscripting, subscripting and both super and subscripting of different characters in the same character cell.

The screen may be split vertically, horizontally or both. The clock input for horizontal and vertical sync is separate from the character dot clock; by driving the dot clock with a variable frequency, proportional character spacing can be generated. Other features include soft scrolling, interlace and non-interlace output generation, two additional parallel attribute bits for user defined functions with the capability for the addition of 16 more attributes, and light pen capability.

The AmZ8052 requires a single 5V supply and is packaged in a 48-pin DIP.

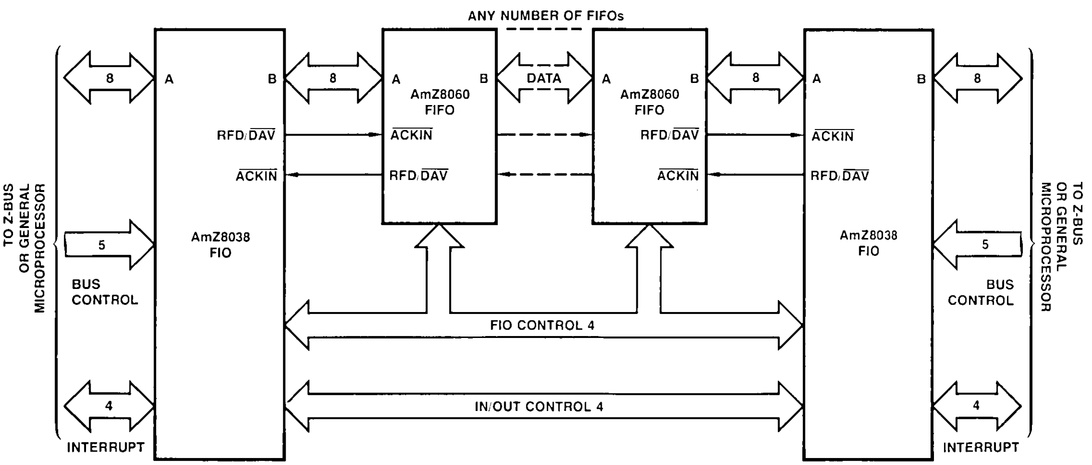


AmZ8060 FIFO Buffer Unit and FIO Expander (FIFO)

The AmZ8060 FIFO buffer unit is a 128 x 8-bit memory with half-duplex bidirectional data transfer capability and handshake logic. It can be used as a stand-alone first-in, first-out memory or to expand the AmZ8038 buffer depth. The FIFO is capable of simultaneous, asynchronous, independent read and write operations; because it, like the AmZ8038, is RAM-based, the propagation time from input to output is negligible.

The AmZ8060 can be cascaded without limit by daisy-chaining the RFD/DAV and ACKIN signals. It may be used to interface to other devices or to synchronize the servicing microprocessor via control lines. Two handshake lines allow direct interfacing to other peripheral devices. Buffer status (FULL and EMPTY) is also available as separate pins.

The AmZ8060 requires a single 5V supply and is packaged in a 28-pin DIP.



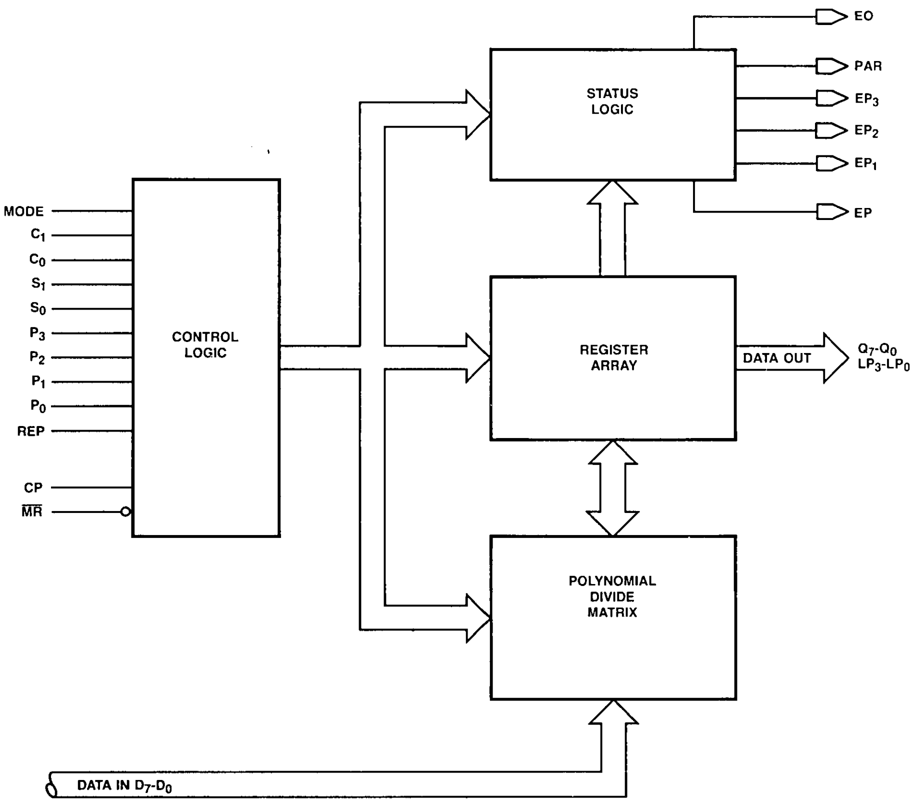
EXTENDING THE FIOs WITH FIFOs

AmZ8065 Burst Error Processor (BEP)

The AmZ8065 burst error processor provides a tool for implementing the most common error detection and correction schemes in hard disk controllers. Because modern disks use high data recording densities, the probability of errors occurring during data recovery is increased. Burst error detection and correction schemes based on Fire codes are used to correct such errors and to enhance the overall disk system performance.

The AmZ8065 provides four standard polynomials, including the popular IBM 56-bit and 48-bit versions; logic levels on two inputs select the desired polynomial. For encoding, the data stream is divided by a selected polynomial using rules of algebra in polynomial fields. This division results in a remainder which is appended to the data as check bits. For error checking, the bit stream containing both data and check bits is divided by the same polynomial. If there are no detectable errors, this division results in a zero remainder. If an error is detected, the AmZ8065 will extract the burst error pattern and the location of the error burst in the data stream.

The AmZ8065 requires a single-phase clock, a 5V supply and is packaged in a 40-pin DIP.

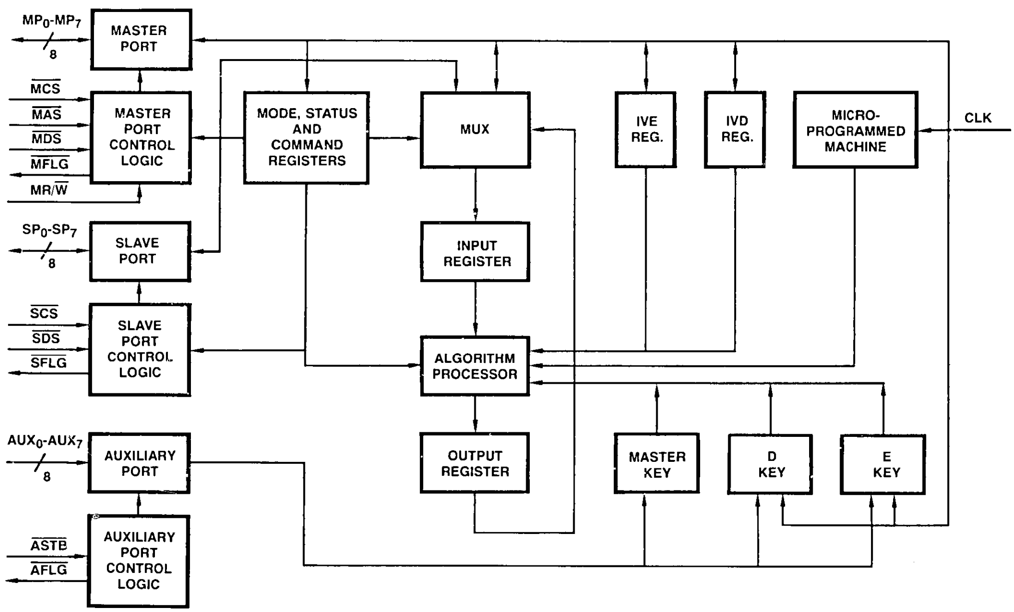


AmZ8068 Data Ciphering Processor (DCP)

The AmZ8068 data ciphering processor encrypts and decrypts data using the National Bureau of Standards encryption algorithm. It can be used in a variety of environments including dedicated controllers, communication concentrators, terminals and peripheral task processors in general microprocessor systems. The DCP provides throughput rates greater than one megabyte per second using the Cipher Feedback, Electronic Code Book or Cipher Block Chain operating modes. Separate ports are provided for key input, clear data and enciphered data to enhance security and to provide a half-duplex, pipelined data path.

The AmZ8068 can be used in AmZ8001/AmZ8002 microprocessor systems with the CPU programming the DCP through one of the data ports. The DCP can also be configured to accept control information on dedicated control lines, allowing it to be used in 2900-based bit-slice designs, with the control information derived directly from microcode memory. In either configuration, once set up data can flow through the DCP bidirectionally at high rates because input, output and ciphering activities are performed concurrently. Control lines are provided for interfacing to external DMA devices.

The AmZ8068 requires a single 5V supply and is packaged in a 40-pin DIP.

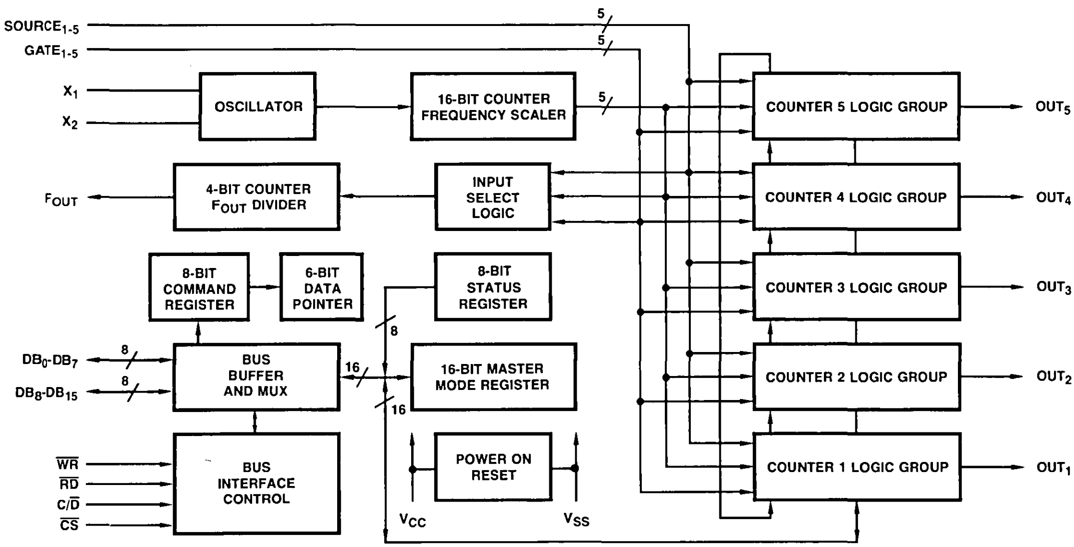


AmZ8073 System Timing Controller (STC)

The AmZ8073 system timing controller performs many types of counting, sequencing and timing operations in 8-bit or 16-bit microprocessor systems. It provides the capability for programmable frequency synthesis, high-resolution programmable duty-cycle waveforms, retriggerable digital timing functions, time-of-day clocking, coincidence alarms, complex pulse generation, high-resolution baud-rate generation, frequency shift keying, stopwatch timing, event-count accumulation, waveform analysis and many more. A variety of programmable operating modes and control features allows the AmZ8073 to be personalized for specific applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-HIGH or active-LOW input polarity. Both hardware and software gating of each counter are available. Three-state outputs for each counter provide pulses or levels and can be either active HIGH or active LOW. The counters can be programmed to count up or down in either binary or BCD. The CPU may read an accumulated count without disturbing the counting process. Any of the counters may be internally concatenated to form an effective counter length of up to 80 bits. An on-chip oscillator and frequency scaler can be used as a convenient time-base source.

The AmZ8073 requires a single 5V supply and is packaged in a 40-pin DIP.



MOS DEVELOPMENT SUPPORT SYSTEMS

AmSYS™8/8 Microcomputer Development Systems

The AmSYS8/8000 and AmSYS8/8100 series are support systems for the development of 16-bit microprocessors. The 8000 series supports a variety of microprocessors that includes the Z80, 8080A, 8085A and 8048. AmSYS8/8100 is especially designed to support the AmZ8000 CPU in both hardware and software development. The AmSYS8/8 systems feature Multibus*-compatible MultiMaster bus structure that allows multiple 8- and 16-bit CPUs to be used simultaneously. New software options include real-time emulations and Pascal and C languages. An Am96/4016 Evaluation Board option on the 8100 series provides a low-cost means of executing AmZ8000 code in a controlled hardware environment with limited debugging capability.

Hardware features include:

- 8-bit Am9080 CPU
- 64K bytes read/write main memory
- MultiMaster bus
- Extra card slots for prototyping
- Dual floppy disks single or double density

Software features include:

- AMDOS™ disk operating system (CP/M 2.2-level compatible)
- Macroassembler for Z80A, 8080A, 8085A
- PROM programming support

RTE™ Real-Time Emulators

The AmSYS8/8 development systems provide two types of optional real-time emulators to support microprocessors: the RTE8/8800 and the RTE16/8050.

The RTE8/8800 is for 8-bit microprocessors, including individual emulators for the 8080A, 8085A, Z80A, 8048 and 8041A. It allows replacement of the target microprocessor during the debugging and prototyping phase. Real-time emulation of each designed microprocessor can be performed together with sophisticated debug tools for hardware/software integration.

- Real-time trace storing the last 128 bus operations and 8 external probes
- 8k bytes of high-speed static RAM emulator memory
- Capability to examine and alter registers, memory and I/O parts

The RTE16/8050 16-bit emulator is a powerful tool for developing and debugging AmZ8000 hardware and software. It is an optional plug-in card set to 8100 AmSYS8 series models, containing logic analyzer and trace capabilities. The RTE16/8050 allows AmZ8000 emulation without any target hardware for software execution and debugging. Pods are available for AmZ8001/8002 CPUs.

- Interactive operation minimizes user effort
- 8k bytes of high-speed static RAM (no wait states)
- Optional dynamic RAM up to 256K bytes with two or three user-selectable wait states
- Real-time emulation up to 4MHz logic analyzer capability includes eight complex trigger points which can be used as break points or trace qualifiers.

AMD School of Advanced Engineering

The AMD School of Advanced Engineering offers three courses to managers, engineers and programmers using the AmZ8000 microprocessors: Introduction to 16-bit Microprocessor Design, Assembly Language Programming on the AmSYS8/8 and Pascal programming for the AmZ8000. Comprehensive course notes are also available separately. For more information regarding course content, schedule or fees, or to order class notes, please contact:

AMD School of Advanced Engineering
430 Lakeside Drive
Sunnyvale, CA 94086
408/732-2400 Ext. 2325

*Multibus is a trademark of Intel Corporation.

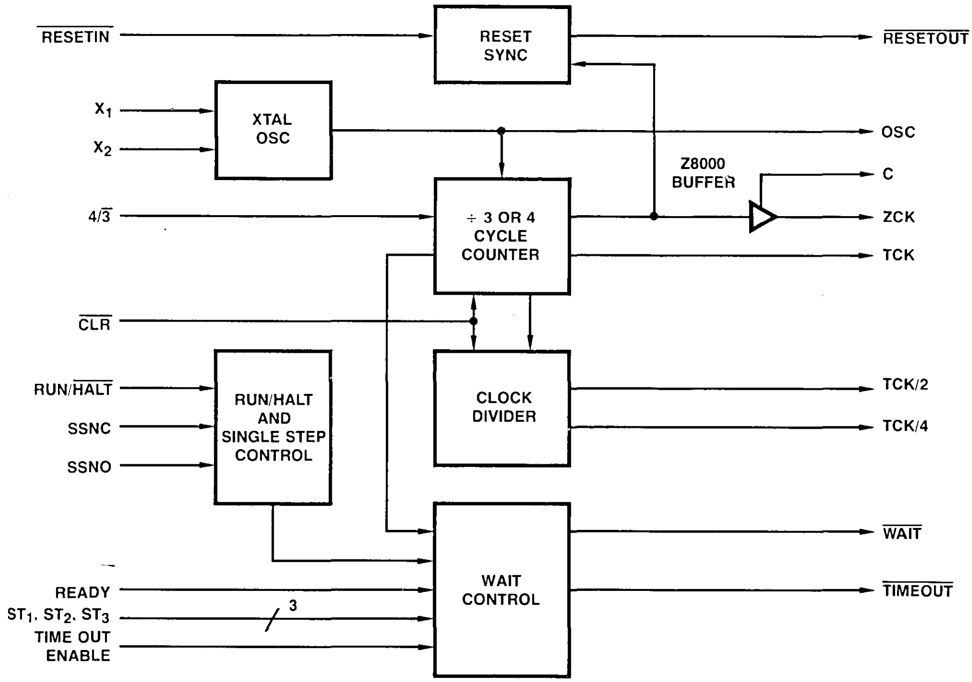
4

AmZ8127 AmZ8000 Clock Generator and Controller

The AmZ8127 Clock Generator and Controller provides the clock oscillator, frequency dividers and clock drivers for the complete array of AmZ8000 CPUs, peripherals and memory system configurations. In addition to the special 4MHz output driver for the AmZ8001 and AmZ8002 CPUs, a standard buffered TTL 16MHz oscillator output is provided for dynamic memory timing and control. The oscillator is designed to operate with a 16MHz crystal or with external 16MHz drive. The AmZ8127 uses an internal divide-by-4 to provide 4MHz clock drive to the AmZ8001/AmZ8002 CPU. Additional dividers generate synchronous buffered 2MHz and 1MHz clock outputs for use by peripheral devices. The clock divider counters are clearable to allow synchronizing the multiple clock outputs.

The controller functions include $\overline{\text{RESET}}$, RUN/$\overline{\text{HALT}}$, SINGLE-STEP, READY and a READY TIMEOUT counter which limits a peripheral's wait request to 16 clock cycles. The CPU's $\overline{\text{WAIT}}$ input is controlled by RUN/$\overline{\text{HALT}}$, SINGLE-STEP and READY. A $\overline{\text{HALT}}$ command to the AmZ8127 drives the $\overline{\text{WAIT}}$ output LOW causing the CPU to add wait states (TW to TW). The READY input is used by peripherals to request wait states. The active HIGH input TIMEOUT ENABLE is used to force TIMEOUT and $\overline{\text{WAIT}}$ to HIGH 16 clock cycles after a peripheral has requested a wait but fails to release the request. The CPU status lines ST1, ST2 and ST3 are decoded in the AmZ8127 to disable the TIMEOUT counter during CPU "Internal Operations" and during refresh.

The AmZ8127 is available in a 24-pin 0.3" wide DIP.

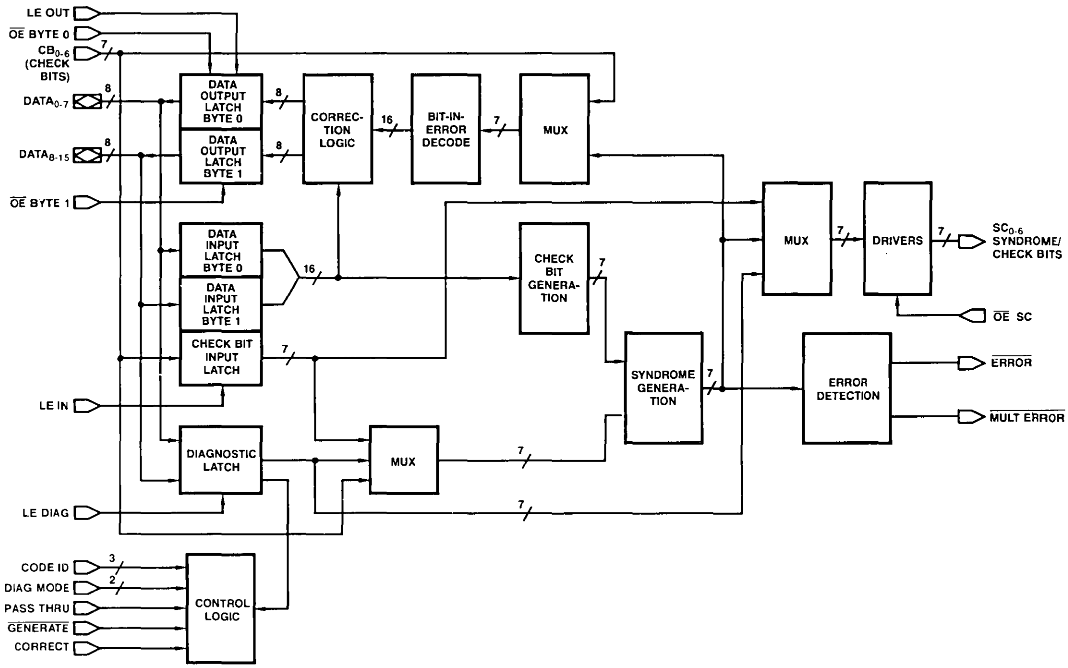


BLI-168

AmZ8160 Error Detection and Correction Unit (EDC)

The AmZ8160 error detection and correction unit generates six check bits on a 16-bit data field according to a modified Hamming Code and corrects the data word when check bits are supplied. Operating on data read from memory, the AmZ8160 will correct any single-bit error and detect all double and some triple-bit errors. The EDC is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome bits available on separate outputs for data logging.

The AmZ8160 has built-in diagnostic and initialize modes. Diagnostic data can be input to the EDC or memory to simplify device testing and execute system diagnostic functions. The EDC is supplied in a 48-pin hermetic DIP.



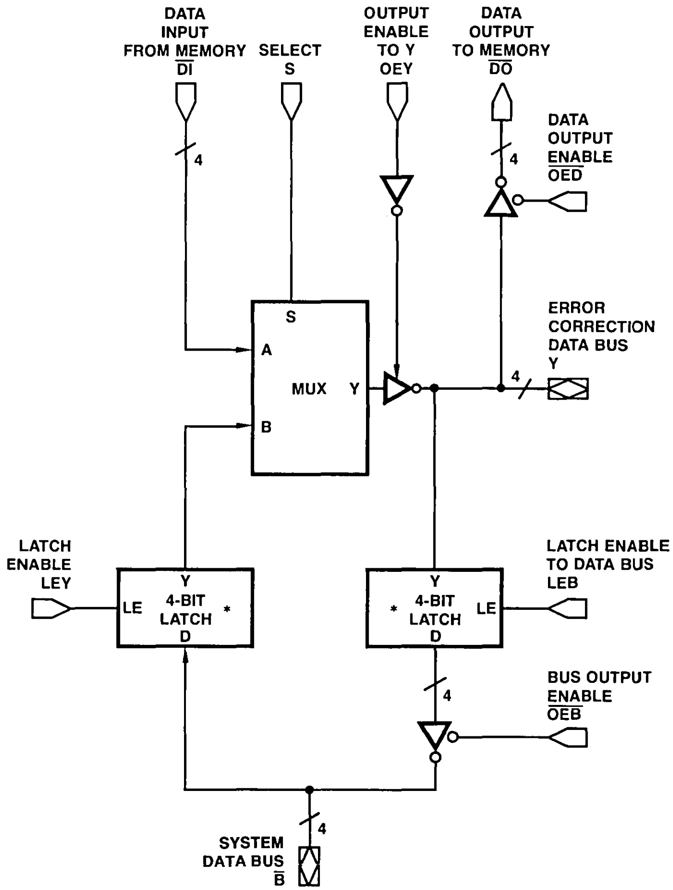
BLI-201

AmZ8161/AmZ8162 Error Correction Multiple Bus Buffers

The AmZ8161 and AmZ8162 low-power Schottky multiple bus buffers provide the complete data path interface between the AmZ8160 error detection and correction unit, dynamic RAM memory and the AmZ8001/AmZ8002 microprocessor system data bus. The AmZ8161 provides an inverting data path between the data bus ($\overline{B_i}$) and the AmZ8160 error correction data input (Y_i); the AmZ8162 provides a non-inverting configuration (B_i to Y_i).

The AmZ8161 and AmZ8162 are 4-bit devices; four devices are used to interface each 16-bit AmZ8160 with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction. Data latches between the error correction data bus and the system data bus facilitate the addition of error corrected memory in multiplexed data bus systems and provide a data holding capability during single-step system operations. Both devices are available in a hermetic 24-pin 0.3" wide DIP.

AmZ8161*



*AmZ8162 is the same function but non-inverting between the Y bus to the system data bus, B. This is done by making both latches inverting.

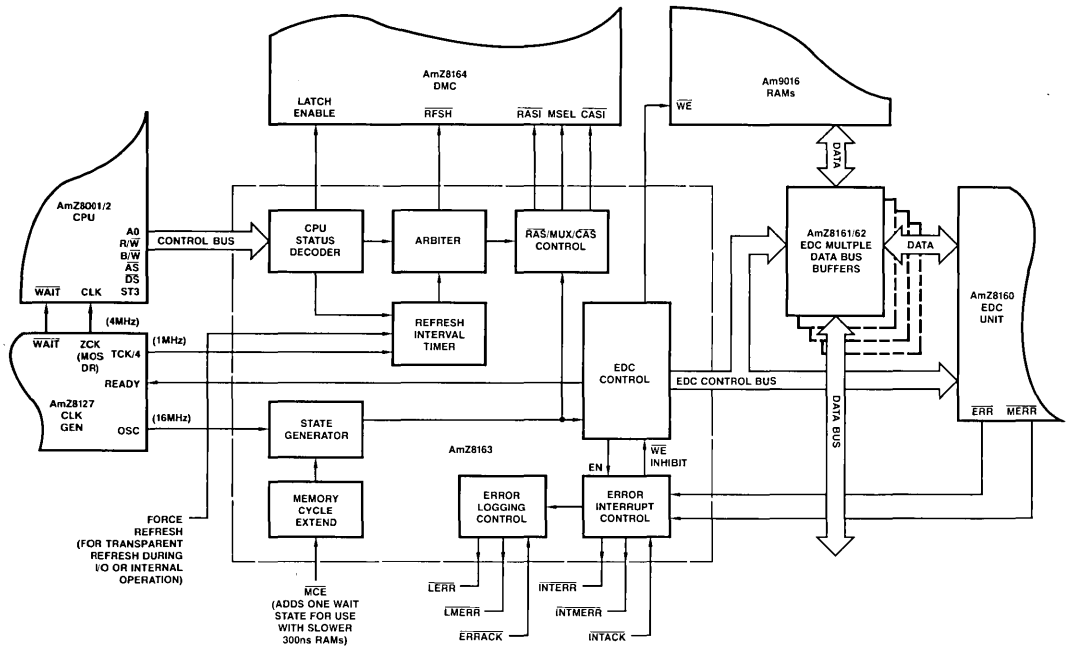
BLI-206

AmZ8163 Dynamic Memory Timing, Refresh and EDC Controller

The AmZ8163 high-speed bus interface controller provides all of the control interface functions including $\overline{\text{RAS}}$/Address Mux/$\overline{\text{CAS}}$ timing (without delay lines), refresh timing, memory request/refresh arbitration and all error detection and correction enables and controls for AmZ8001/AmZ8002 microprocessor systems. The enable controls are configured for both word and byte operations including the data controls for byte write with error correction.

The AmZ8163 generates bus and operating mode controls for the AmZ8160 error detection and correction unit. It uses the AmZ8127 clock generator and controller 16MHz (4 x Clk) output to generate $\overline{\text{RAS}}$/Address Mux/$\overline{\text{CAS}}$ timing. An internal refresh interval timer generates the memory refresh request independent of the CPU to guarantee the proper refresh timing under all combinations of CPU and DMA requests.

The AmZ8163 is available in a 40-pin DIP.



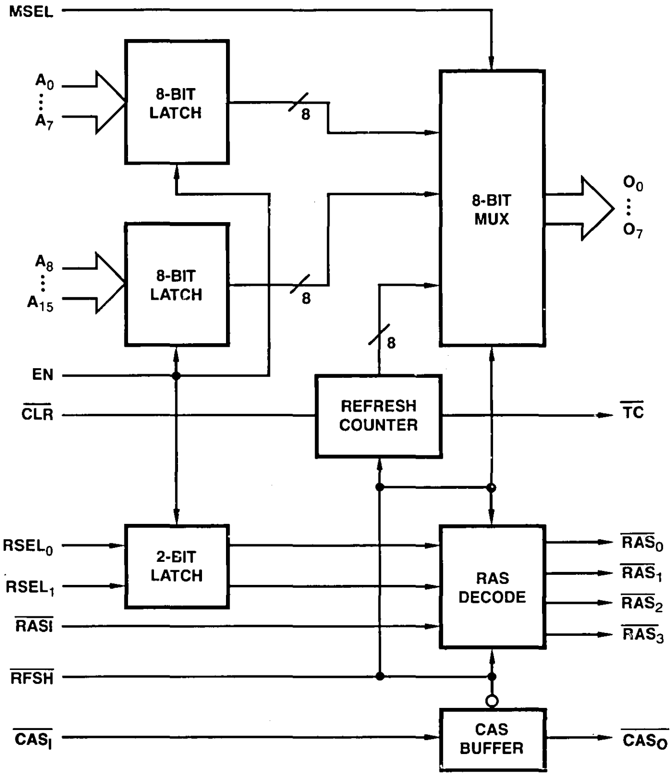
BLI-167

AmZ8164B Dynamic Memory Controller

The AmZ8164B dynamic memory controller replaces several MSI devices by grouping unique functions on-chip. Two 8-bit latches capture and hold the memory address from the AmZ8001/AmZ8002 multiplexed data and address bus. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input Schottky-speed multiplexer for output to the dynamic RAM address lines. The AmZ8164B has a special $\overline{RAS}$ decoder and CAS buffer which minimize the time skew between output functions and allow a faster memory cycle time. The device is also compatible with the Am8085A or any CPU interfacing with dynamic RAMs.

The active-LOW refresh line, $\overline{RFSH}$, switches the MUX to the counter output, inhibits $\overline{CAS}$, and changes the $\overline{RAS}$ decoder function from 1-of-4 to 4-of-4. $\overline{RASI}$ then forces all $\overline{RAS}$ outputs LOW when $\overline{RFSH}$ is LOW and the counter is advanced at the end of the refresh cycle – the LOW-to-HIGH transition of $\overline{RASI}$ ($\overline{RFSH}$ = LOW). Various refresh modes can be accommodated for 16K or 64K RAMs and for a wide variety of microprocessor configurations. A_{15} is a dual function input which controls the refresh counter's $\overline{TC}$ output: for 64K RAMs it is an address input; for 16K RAMs it can be pulled to +12V through 1KΩ to indicate a complete refresh count at 128 instead of 256.

The AmZ8164B is available in a 40-pin DIP.



BLI-208

AmZ8165/AmZ8166 Octal Dynamic Memory Drivers

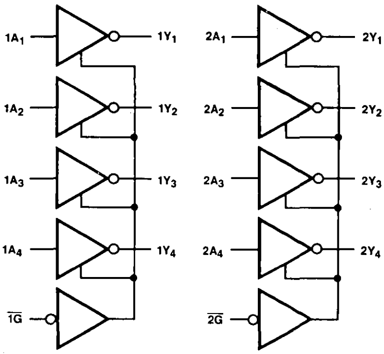
The AmZ8165 and AmZ8166 octal dynamic memory drivers are designed for use with the AmZ8164B dynamic memory controller where large dynamic memories with highly capacitive input lines require additional buffering.

The lower output driver includes a collector resistor which controls the output fall and undershoot without slowing the output rise time. The need for an external series resistor is eliminated, therefore reducing package count and board area required. The upper output driver pulls up to V_{CC} −1.15V and has a rise time symmetrical with the lower output's controlled fall time. Each device has specified skew between drivers to improve the memory access worst case timing over the min and max t_{pd} difference of unspecified devices.

They are pin-compatible with the popular 'S240 and 'S244 buffer/line drivers and have identical 3-state output enable controls. The AmZ8165 has inverting drivers; the AmZ8166 has non-inverting drivers.

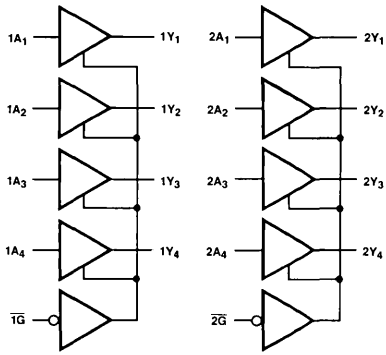
The AmZ8165 and AmZ8166 are available in either a plastic or hermetic 20-pin DIP.

AmZ8165



BLI-212

AmZ8166



BLI-213

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

MOS MICROPROCESSOR PRODUCTS
Bipolar Support Products

Microcomputer Interface and Support Circuits

Item	Description	Part Number	I_{OL} (Max) mA	I_{OL} (Max) @V	t_{pd} ns (Typ)	Inv./Non-Inverting	Output	Number of Pins	Package(s)
8-Bit Microcomputer Support Circuits									
1	Octal Input/Output Port	**8212**	15	0.45	12	N	3S	24	D, P
2	Quad Bidirectional Bus Driver	**8216**	50	0.6	15	N	3S	16	D, P
3	Clock Generator/Driver	**8224**	15	0.45			8080 Levels	16	D, P
4	Quad Bidirectional Bus Driver	**8226**	50	0.6	15	I	3S	16	D, P
5	System Controller	**8228**	2/10	0.45	15-30	Generates 8080 Control and Data Bus Interface		28	D, P
6	System Controller	**8238**	2/10	0.45	15-30			28	D, P
16-Bit Microcomputer Support Circuits									
7	Octal Bus Transceiver w/T/$\overline{R}$, CD	**AmZ8103**	24/48	0.5	11	I	3S	20	D, P
8	Octal Bus Transceiver w/T/$\overline{R}$, CD	**AmZ8104**	24/48	0.5	14	N	3S	20	D, P
9	Octal Bus Transceiver w/$\overline{T}$, $\overline{R}$	**AmZ8107**	24/48	0.5	11	I	3S	20	D, P
10	Octal Bus Transceiver w/$\overline{T}$, $\overline{R}$	**AmZ8108**	24/48	0.5	14	N	3S	20	D, P
11	Octal Register w/CP, $\overline{CLR}$, $\overline{OE}$, CP Enable	**AmZ8120**	8.0	0.45	24	N	3S	24[1]	D
12	8-Bit Equal-to Comparator	**AmZ8121**	12	0.5	9.0		TTL	20	D, P
13	AmZ8000 Clock Generator w/Run/Halt, Single-Step, Wait and Timeout Controls	**AmZ8127**	See Product Features in Section 4					24[1]	D
14	Octal Latch w/G, $\overline{OE}$	**AmZ8133**	24	0.5	15	I	3S	20	D, P
15	3-to-8 Decoder w/Control Storage	**AmZ8136**	24	0.5	30		3S	20	D, P
16	Octal Bus Driver w/$\overline{OE}$, $\overline{OE}$	**AmZ8140**	48	0.55	9.0	I	3S	20	D, P
17	Octal Bus Driver w/$\overline{OE}$, $\overline{OE}$	**AmZ8144**	48	0.55	11	N	3S	20	D, P
18	3-to-8 Chip Select Decoder w/$\overline{ACK}$	**AmZ8148**	8.0	0.45	19		TTL	20	D, P
19	Octal Latch w/G, $\overline{OE}$	**AmZ8173**	24	0.5	12	N	3S	20	D, P

Dynamic Memory Support Products[2]

Item	Description	Part Number	Data Width	Function	Inv./Non-Inverting	Number of Pins	Package(s)
20	Error Detection and Correction Unit (EDC)	**AmZ8160**	16	Expandable Hamming Code EDC Slice w/Diagnostics/Initialization and Byte-Level I/O Interface	I to Bus	48	D
21	EDC Data Bus Buffer	**AmZ8161**	4	4-Port EDC Interface for RAM, EDC and 24mA I_{OL} Data Bus Drive	I to Bus	24[1]	D
22	EDC Data Bus Buffer	**AmZ8162**	4	4-Port EDC Interface for RAM, EDC and 24mA I_{OL} Data Bus Drive	N to Bus	24[1]	D
23	EDC and Refresh Controller	**AmZ8163**		Memory Timing and Controls for AmZ8160/AmZ8164 (used w/AmZ8127)		40	D, P
24	Dynamic Memory Controller	**AmZ8164B**	8	Memory Address Controller w/Refresh Counter, $\overline{RAS}$ Decoder, $\overline{CAS}$ Inhibit Buffer		40	D, P
25	Dynamic RAM Driver	**AmZ8165**	8	RAM Driver w/3-State, Undershoot Protected Outputs	I	20	D, P
26	Dynamic RAM Driver	**AmZ8166**	8	RAM Driver w/3-State, Undershoot Protected Outputs	N	20	D, P

One-Shots

Item	Description	Part Number	I_{OL} (Max) mA	I_{OL} (Max) @ V	t_{pd} ns (Typ)	Inv./Non-Inverting	Output	Number of Pins	Package(s)
27	Retriggerable, Resettable, Monostable Multivibrator	**Am26S02**	20	0.5	28	N or I	TTL	16	D, F, P

Notes: 1. New 24-pin, 0.3" wide package.
2. See product features in Section 4.

LINEAR

DATA CONVERSION PRODUCTS

D/A Converters

Item	Part Number	Resolution Bits	Differential Non-Linearity Bits	Non-Linearity % Full Scale	Settling Time ns (Typ)	Dynamic Range dB (Min)	Transfer Function	Package(s)	Comments
General Purpose									
1	DAC-08A, H	8		0.10	85			D, P	Industry Standard 8-Bit
2	DAC-08, E	8		0.19	85			D, P	Industry Standard 8-Bit
3	DAC-08C	8		0.39	85			D, P	Industry Standard 8-Bit
4	Am1508[1]	8		0.19	300			D, P	
5	SSS1508[1]	8		0.19	250			D, P	
6	Am6012	12	12	0.05	250			D, P	
7	Am6012A	12	13	0.05	250			D	
8	Am6014[2]	14	14		500			D	
9	Am6015[2]	16			1000			D	
Microprocessor Compatible									
10	Am6080	8	8	0.19	160			D, P	Contains 8-Bit Latch and Control Logic
11	Am6080A	8	9	0.10	160			D, P	Contains 8-Bit Latch and Control Logic
12	Am6081	8	8	0.10	200			D, P	Contains 8-Bit Latch, Control Logic and Output Multiplexer
13	Am6081A	8	9	0.10	200			D, P	Contains 8-Bit Latch, Control Logic and Output Multiplexer
14	Am6082[2]	12	12	0.012	200(I) 1000(V)			D	Contains Reference, Double Buffered Latch, Scale Resistors, Control Logic and High-Speed Op Amp
Companding									
15	Am6070				300	72	μ-Law	D	Control System Applications
16	Am6071				300	62	A-Law	D	Control System Applications
17	Am6072				300	72	μ-Law	D	PCM Communication Systems
18	Am6073				300	72	A-Law	D	PCM Communication Systems

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A/D Converters

Item	Part Number	Resolution Bits	Accuracy Bits (LSB)	Sampling Frequency MHz (Min)	Conversion Time ns (Max)	Output	Package(s)	Comments
High-Speed								
19	Am6688[2]	4	6, 7 and 8	100		ECL	D	Expandable to 8 Bits
High-Speed Microprocessor Compatible								
20	Am6108[2]	8	(±1/2)		900	TTL	D	Contains Reference, Scale Resistors, 3-State Output Buffers and Control Logic
21	Am6112[2]	12	(±1/2)		5000	TTL	D	Contains Reference, Scale Resistors, 3-State Output Buffers and Control Logic

Sample and Hold

Item	Part Number	Gain Error % (Max)	Acquisition Time μs (Min)	V_{OS} mV (Max)	I_B nA (Max)	Package	Comments
22	LF198[1]	0.01	4.0	3.0	25	H	Industry Standard

Notes: 1. Only military part number listed; also available in commercial and limited military temperature ranges.
2. To be announced.

LINEAR

AMPLIFIERS

Operational Amplifiers

Item	Part Number	V_{OS} mV (Max)	I_{OS} nA (Max)	I_B nA (Max)	Slew Rate V/µs (Typ)	Configuration	Package(s)
Uncompensated							
1	**LM101A***	2.0	10	75	0.5	Single	H, D, F
2	**LM108***	2.0	0.2	2.0	0.3	Single	H, D, F, N
3	**LM108A***	0.5	0.2	2.0	0.3	Single	H, D, F, N
4	**Am1501**	2.0	10	75	0.5	Dual	D, F
5	**LM2101A***	2.0	10	75	0.5	Dual	D, F
6	**715**	5.0	250	750	20	Single	H, D, F
7	**725**	1.0	20	100	0.005	Single	H, D, N
8	**SSS725**	0.5	5.0	80	0.005	Single	H, D
Internally Compensated							
9	**LM107***	2.0	10	75	0.5	Single	H, D, F
10	**LM112***	2.0	0.2	2.0	0.2	Single	H
11	**LM118***	4.0	50	250	70	Single	H, D, F, N
12	**LM124***	5.0	30	150	0.1	Quad	D, F, N
13	**LM124A***	2.0	10	50	0.1	Quad	D, F, N
14	**LM148***	5.0	25	100	0.5	Quad	D, F, N
15	**LM149***	5.0	25	100	2.0	Quad	D, F, N
16	**LF155***	5.0	0.02	0.1	5.0	Single	H
17	**LF155A***	2.0	0.01	0.05	5.0	Single	H
18	**Am1558***	5.0	200	500	0.4	Dual	H
19	**LF156***	5.0	0.02	0.1	12	Single	H
20	**LF156A***	2.0	0.01	0.05	12	Single	H
21	**LF157***	5.0	0.02	0.1	50	Single	H
22	**LF157A***	2.0	0.01	0.05	50	Single	H
23	**741**	5.0	200	500	0.4	Single	H, D, F
24	**741A, E**	3.0	30	110	0.4	Single	H, D, F
25	**SSS741**	2.0	5.0	50	0.4	Single	H, D, F
26	**747**	5.0	200	500	0.4	Dual	H, D, F
27	**747A, E**	3.0	30	110	0.4	Dual	H, D, F
28	**SSS747**	2.0	5.0	50	0.4	Dual	H, D, F

Voltage Followers

29	**LM102***	5.0		10	20	Single	H, D, F
30	**LM110***	4.0		30	30	Single	H, D, F, N

Wideband Amplifiers

Item	Part Number	Bandwidth MHz	Voltage Gain	Package(s)
31	**Am592**	40 – 90	0 – 400	H, D, P
32	**733**	40 – 120	10 – 400	H, D, F, P

*Only military part number listed; also avaliable in commercial and limited military temperature ranges.

LINEAR

VOLTAGE REGULATORS

Adjustable Voltage Regulators

Item	Part Number	Voltage Output V	Line Regulation % V_{OUT} (Max)	Load Regulation % V_{OUT} (Max)	Current Output mA (Max)	Input Voltage Range V	Package(s)
1	723	2.0 – 37	0.1	0.15	150	5.0 – 40	H, D, P
2	LM105[1]	4.5 – 40	0.03	0.05	12	8.5 – 50	H, D

Power Supply Controller

Item	Part Number	Voltage Output V	Line Regulation % V_{OUT} (Max)	Load Regulation % V_{OUT} (Max)	Package(s)	Comments
3	Am6300[2]	2.5 – 37.5	0.2	0.15	D, P	Contains Regulator, Over/Under Voltage Detection, Current Limit and Power Down Reset Sections

COMPARATORS

Item	Part Number	V_{OS} mV (Max)	I_{OS} μA (Max)	I_B μA (Max)	Response Time ns (Typ)	Configuration	Package(s)
4	LM111[1]	3.0	0.01	0.1	200	Single	H, D, F, N
5	LM119[1]	4.0	0.075	0.5	80	Dual	H, D, F, N
6	LM139[1]	5.0	0.025	0.1	1300	Quad	D, F, N
7	LM139A[1]	2.0	0.025	0.1	1300	Quad	D, F, N
8	Am1500	3.0	0.01	0.1	200	Dual	D, F
9	LM2111[1]	3.0	0.01	0.1	200	Dual	D, F
10	Am685	2.0	1.0	10	5.0	Single	H, D
11	Am686	2.0	1.0	10	9.0	Single	H, D, N
12	Am687	2.0	1.0	10	7.0	Dual	D
13	Am687A	2.0	1.0	10	7.0	Dual	D

Notes 1. Only military part number listed; also available in commercial and limited military temperature ranges.
2. To be announced.

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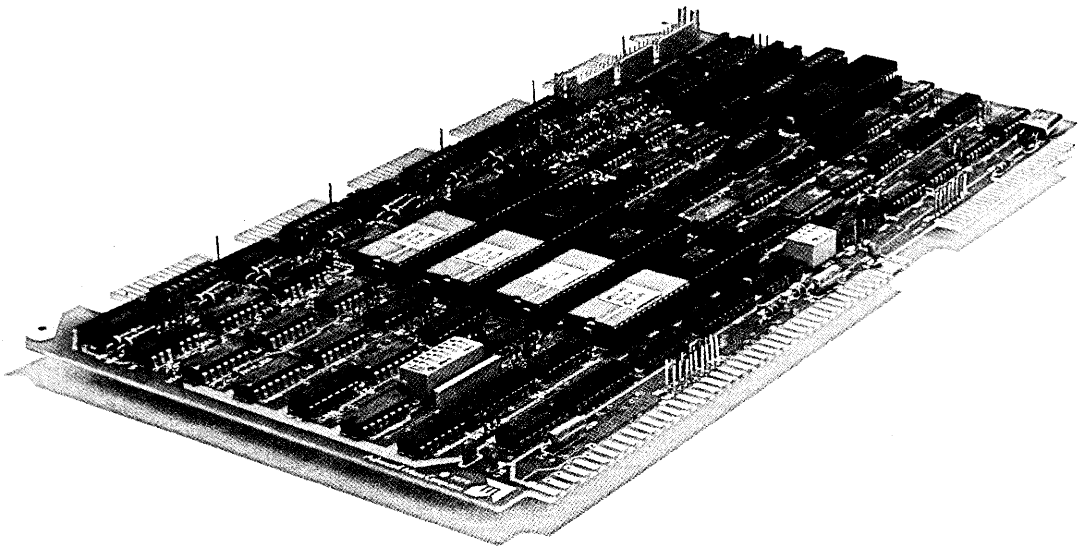
Am95/3310 COMMUNICATION EXPANSION BOARD



- Four Synchronous/Asynchronous Serial I/O Communication Channels with Programmable Baud Rates to 38,400 Baud
- Versatile Parallel Interface
  24 TTL compatible lines or
  8 RS-232 and 16 TTL compatible lines
- Supports Up to Four Modems and One Bell 801-Type Automatic Call/Answer Unit
- Sixteen Programmable Interrupt Lines for Automatic Call/Answer Support
- Two Programmable 16-Bit Counter Timers
- Direct Addressing of I/O Ports on 20H Boundaries
- Serial Ports Jumper Selectable for 20mA Current Loops with Opto-Isolator Sockets
- Multibus* and SBC-80 Compatible

*Registered trademark of Intel Corporation.

The Am95/3310 Communication Expansion Board provides four versatile RS-232/20mA Serial I/O Ports and three configurable Parallel Ports.

The Serial Ports support either RS-232 interfaces up to 38400 baud or 20mA current loop buffering with optional opto-isolation. Both typical computer peripherals and a variety of control and monitoring equipment can be directly interfaced. Three Parallel Ports can be readily configured as a general-purpose interface with up to 24 TTL compatible lines or as a direct interface for an automatic call unit with signal detection and monitoring capability. Two programmable interrupt controllers (8259A) and two counter-timer devices (Am8253) furnish baud rate and interrupt control. Bus signals are supported through a complete Multibus interface. The board design conforms to SBC-80 standards.

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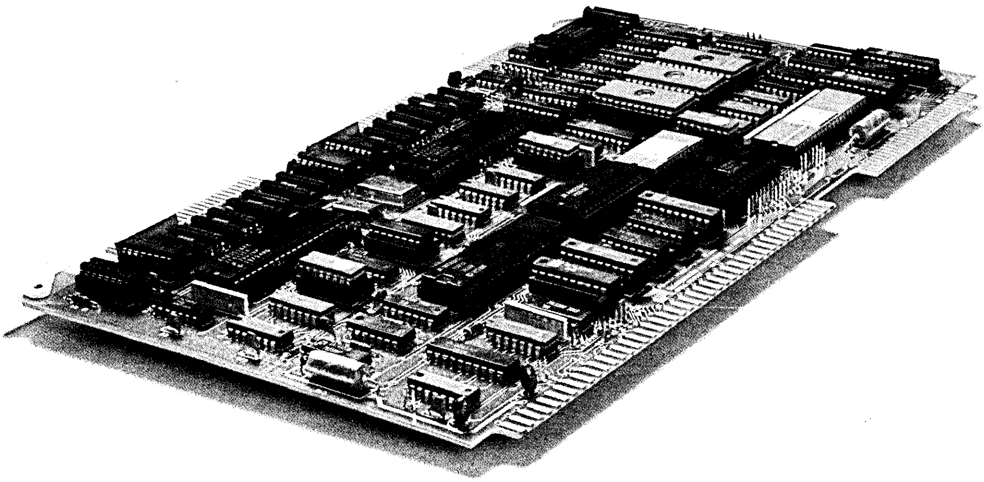
Am95/4006 MONOBOARD™ COMPUTER



- Am8080A/Am9080A CPU
  2MHz standard, 4MHz optional
- Am9511A or Am9512 Arithmetic Processing Unit
  High-speed arithmetic computations concurrent with CPU operation
- 4K Bytes of High-Speed Static RAM (Am9114)
- Sockets for 16K Bytes of ROM/EPROM
- 8-Channel Programmable Interrupt Controller with Vectored Priority
- Programmable Real-Time Clock for Interrupt-Driven Systems
- Am9513 System Timing Controller
- 48 Programmable I/O Lines (Two Am9555s) with Sockets for Line Drivers and Terminators
- Serial Interface for RS-232C (and 20mA) Interface (Am9551), with Program-Selectable Baud Rate (50 to 19,200 Baud)
- Memory Shadow
  Bootstrap program can be selected by power-on or reset and the program-disabled for RAM space
- Compatible with Multibus* Standard, SBC-80 Card Format with MultiMaster Bus Logic

The Am95/4006 MonoBoard Computer is a complete Am8080A/Am9080A-based single-board microcomputer with the exceptional arithmetic processing capabilities of the Am9511A or Am9512 Arithmetic Processing Unit (APU). It is available in both 2.0 and 4.0MHz versions.

*Registered trademark of Intel Corporation.

The APU allows arithmetic computation to be processed concurrently with the operation of the Am8080A/Am9080A CPU for faster throughput. The APU includes fixed- and floating-point arithmetic and transcendental functions (trigonometric, logarithmic and power). This makes it an ideal tool in arithmetic-intensive and real-time applications such as industrial monitoring, process control, medical, navigational and many types of instrumentation.

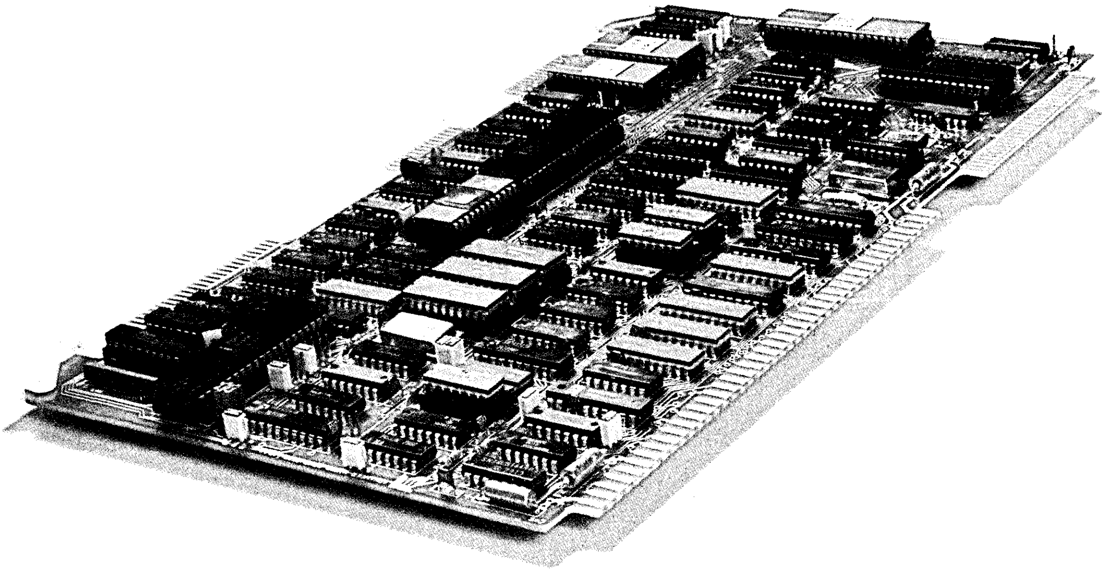
MultiMaster bus control logic further enhances computing capability by allowing several MonoBoard Computers to share a single Multibus system bus.

Further capability is added with additional proprietary LSI circuits: the Am9513 advanced programmable multicounter/timer controller and an 8-level universal interrupt controller. On-board memory is provided as 4K bytes of high-speed static RAM and up to 16K bytes of ROM/EPROM sockets. The logical address-to-memory location relationship is mapped by an address decode PROM. This same PROM also matches the type of EPROM/ROM devices to specific sockets.

Two types of I/O capability are provided. Serial I/O is provided through an RS-232 interface by means of an Am9551 Programmable Peripheral Interface (USART). In addition, there are 48 lines of bidirectional parallel I/O by means of two Am8255A Peripheral Communications Interface Units.

The Am95/4006 is fully Multibus SBC-80 format compatible. It is complemented by a full line of AMC board-level products including additional memory, I/O and ROM/EPROM expansion, floppy disk controller, ROM/PROM combination and communication boards, as well as a comprehensive array of standard and powered card cages and rack-mountable system chassis.

Am95/4010 MONOBOARD™ COMPUTER



- Am8085A MPU at 4.0MHz Operation
- Extended Addressing and Memory Mapping to 1M Byte in 1K Byte Segments under Dynamic Program Control
- System/User Capability with Privileged Instructions
- Programmable Read Protect and Write Protect Attributes for Memory
- Two Serial I/O Ports
- 24 Lines of Parallel I/O
- Up to 4K Bytes of PROM Space
- Five 16-Bit Programmable Counter/Timers
- 8-Channel Programmable Interrupt Controller
- Multibus* SBC-80 Compatible with MultiMaster Bus Logic

The Am95/4010 MonoBoard Computer incorporates a versatile memory management unit into a comprehensive Multibus-compatible single-board computer. In addition to its ability to dynamically map memory in a 1M byte address space, the Am95/4010 MonoBoard Computer provides multiple serial and parallel I/O capability, programmable counter/timers and eight channels of vectored interrupt control.

*Registered trademark of Intel Corporation.

With its memory management unit (MMU), the Am95/4010 MonoBoard Computer extends the memory addressing and mapping functions of 8-bit systems well beyond the traditional 64K byte limit. The on-board MMU offers a wide range of capability from basic paging and board-select to full dynamic mapping that supports memory protection and system/user configurations with privileged instructions.

MultiMaster bus control logic further enhances system capability by allowing up to three single-board computers, together with a complement of memory and peripheral boards, to share the main bus.

The memory management unit is based around a high-speed bipolar RAM configured as 256 x 12-bit words. The lower 10 bits manage bus address lines A through 13 (hex). The upper two bits provide read and write protect attributes.

The eight input address lines obtain their information from the upper six CPU address lines (A-F) and from a 2-line (4-page) decoding circuit. Data for the RAM comes from the system data bus ($DATA_{0-7}$).

The memory management unit is addressed through I/O ports. Multiplexed inputs and outputs permit the MMU to be mapped with data, to be latched in or out of the addressing configuration, and applied in a system/user environment with privileged instruction traps and memory protection attributes.

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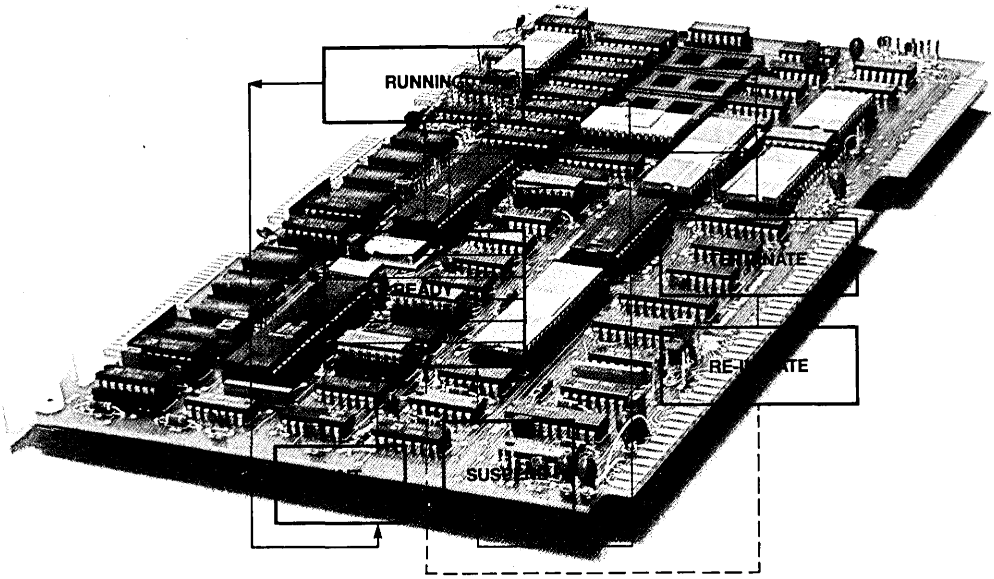
Am95/4620 SERIES RTM8 REAL-TIME MULTITASKING EXECUTIVE



- Task Scheduling, Interrupt Handling and Passing of Parameters for Real-Time Applications
- Handles Up to 15 Hardware-Prioritized Interrupts
- Provides 100 Levels of Software Task Priorities which Are Dynamically Assignable
- Incorporates 100 I/O Channels for External and Internal Task Communication
- Supervises Multiple Tasks in a Dynamic Priority Queue
  Total task capability limited only by available memory
- Furnishes Optional Disk-File Manager and Associated Console Processor Task
- 19 Monitor Calls for:
  Task control (3)
  Internal control (7)
  External I/O (6)
  Intertask messages (3)
- 14-Command Debug Task
- Operates with Advanced Micro Computers' Am95/4006 MonoBoard™ Computers and AmSYS™ Development System
- Both RAM- and PROM-Based Version Available with File Management

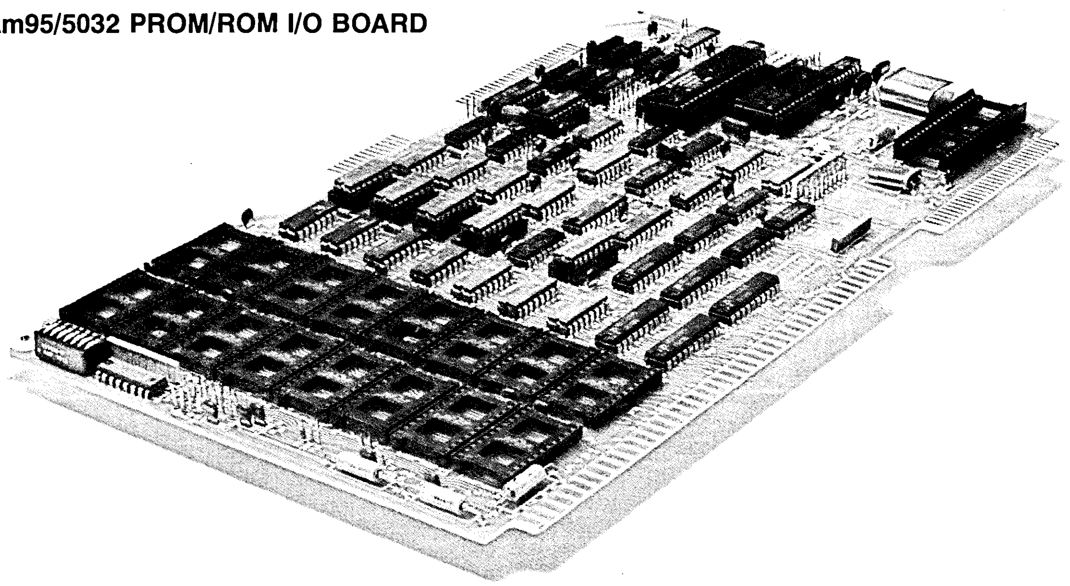
RTM8 software, with its optional file manager and other supporting software, is designed to support real-time multitasking environments found in applications such as industrial control, data acquisition, on-line transaction processing and navigational applications. The RTM8 software runs on Am95/4006 MonoBoard computers and can be implemented in a combination of both RAM and PROM memory.

An AMC MonoBoard computer with RTM8 Software is typically used to monitor and control a variety of external events occurring asynchronously in the physical world. These external real-time events that drive the RTM8-based system can (and frequently do) occur simultaneously, thus creating simultaneous demand for the computer's resources. The computer, on the other hand, operates sequentially, one instruction at a time. With the computer's ability to execute hundreds of thousands of instructions per second, it can be programmed to interleave many simultaneous real-time demands and – for practical purposes – do simultaneous processing of multiple tasks.

There are four major software components that make up the RTM8 package:

- RTM8 – Real-time task monitor; can operate without disk and/or operator console
- Console processor – optional task operating under RTM8. Provides interactive operator communication via CRT/keyboard
- Disk-file manager – optional task operating under RTM8 providing floppy-disk file management on up to four single- or double-density drives
- Task debug – optional task operating under RTM8, providing interactive task debug and program trace. This disk-resident task requires the file manager for loading.

Am95/5032 PROM/ROM I/O BOARD



- Provides Sockets for Up to 64K Bytes of PROM/ROM in a Multibus* Compatible Board
- 8-Bit and 16-Bit CPU Compatibility
- Permits RAM/PROM to Co-Exist in the Same Memory Space
- Programmed Control to Enable/Disable All Combinations of PROM/ROM Sockets
  Permits multiple independent program modules to occupy the same memory area
- Supports All Type of Multibus Data Transfers under Automatic Firmware Control
- Allows Jumper-Selectable Combinations of Am2708, Am2716 and Am2732 EPROMs and Similar ROMs
- Total Versatility for Memory Mapping PROM/ROM Area via Bipolar PROMs
  Assures the integrity of the memory map and eliminates the potential problems from multiple mechanical components
- Optional I/O Section
  RS-232 serial I/O port
  Three 8-bit (or 24-line) parallel ports
  Timing controller (Am9513) with five 16-bit high-speed counters
  Nine interrupt sources jumper-selectable to bus interrupt lines

*Registered trademark of Intel Corporation.

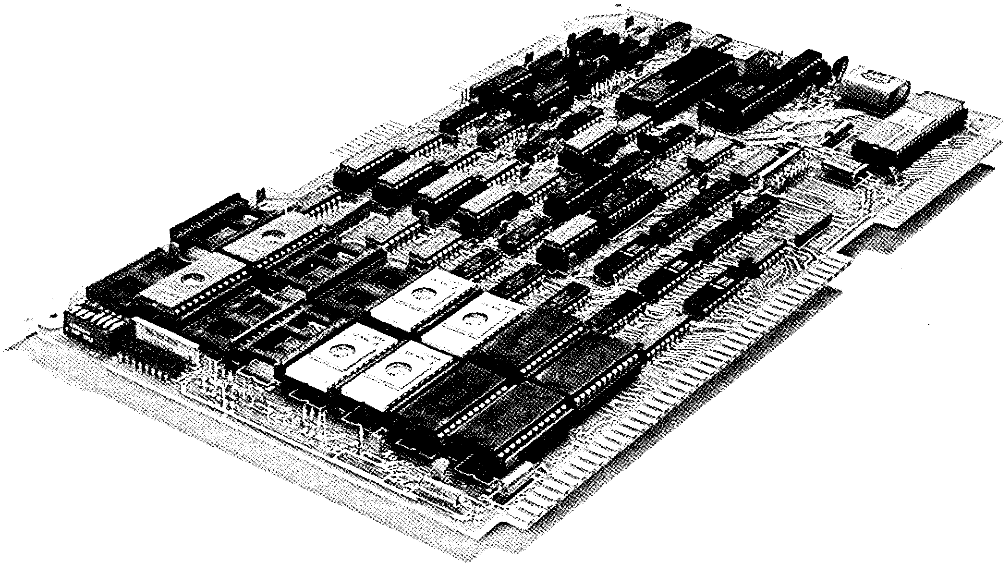
The Am95/5032 ROM/EPROM board is a versatile read-only-memory board designed to be used with AMC's MonoBoard™ computers, or any other Multibus compatible 8-bit or 16-bit microcomputer. In addition to providing non-volatile memory storage for up to 64 kilobytes of non-volatile program code or data storage, the I/O version of the ROM/EPROM board contains one serial I/O port, three parallel I/O ports and a system timing controller (Am9513).

Because of the flexibility designed into the board, the Am95/5032 can be populated with up to eight Am2708 EPROMs or with up to 16 Am2716 or 16 Am2732 EPROMs or pin-equivalent ROMs. On-board jumpers are used to apply the proper voltage and control signals to the various memory devices. Memory mapping is provided by four bipolar PROMs. Two latching 8-bit data bus registers, controlled by I/O ports, provide a PROM/ROM chip select mask that enhances mapping versatility and board operation.

The ability of the system to communicate with external devices is enhanced by the input/output capability included on the I/O version of the ROM/EPROM board. An Am9551 Programmable Communication Interface drives a serial I/O port. Three parallel I/O ports (24 bits) are controlled by an Am8255A Programmable Peripheral Interface.

An Am9513 System Timing Controller is included on the I/O version to further enhance the system by providing timing and counting capability. The system timing controller contains five high-speed 16-bit counters, two of which can be configured to operate as a 24-hour real-time clock.

Am95/5132 PROM/ROM/RAM AND I/O BOARD



- Sockets for Up to 64K Bytes or PROM and Up to 32K Bytes of RAM in a Multibus* Compatible Board
- Allows Intermixed Combinations of Am2716 and Am2732 EPROMs as well as 1K x 8 and 2K x 8 Static RAMs
- Total Versatility for Mapping the Board's Memory Space via Bipolar PROMs
  Assures the integrity of the memory map
  Eliminates the potential problems from multiple banks of DIP switches
- 20-Bit Address Decoding
- Compatible with 8-Bit and 16-Bit CPUs
- Permits RAM/PROM to Coexist in the Same Memory Space
- Programmed Control to Enable/Disable All Combinations of PROM/RAM Sockets
  Permits multiple independent program modules to occupy the same memory area
- Supports All Types of Multibus Data Transfers under Automatic Control
- I/O Section
  RS-232 serial I/O port
  Three 8-bit (24-lines) parallel ports
  Timing controller (Am9513) with five 16-bit high-speed counters
  Nine interrupt sources jumper-selectable to bus interrupt lines

*Registered trademark of Intel Corporation.

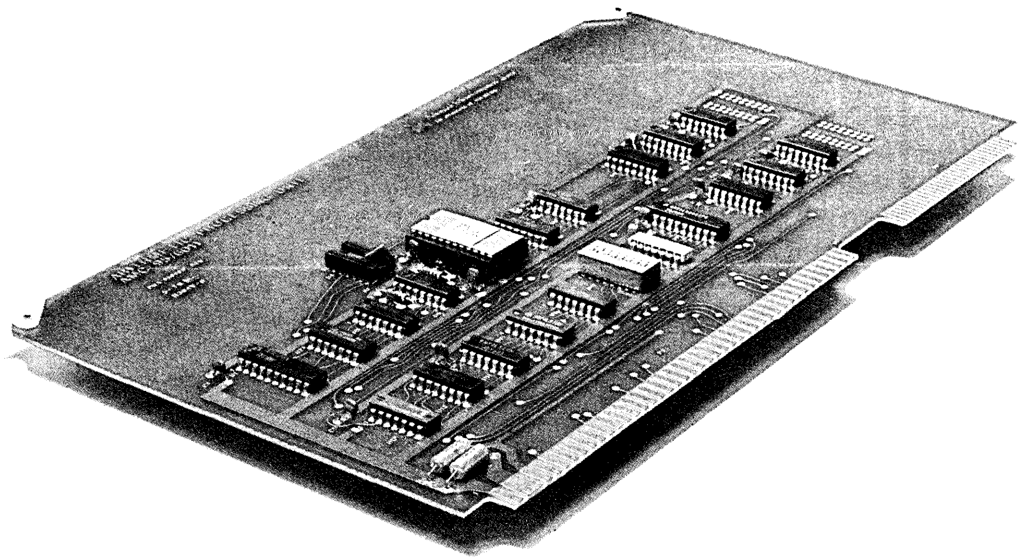
The Am95/5132 PROM/RAM and I/O Board is a versatile dual memory board designed to be used with AMC's MonoBoard™ computers or any other Multibus-compatible 8-bit or 16-bit microcomputer. In addition to providing both RAM and non-volatile memory storage for up to 64K bytes of program code or data storage, the I/O section of the board contains one serial I/O port, three parallel I/O ports and a system timing controller (Am9513).

Because of the flexibility designed into the board, the Am95/5132 can be populated with a mixture of up to 16 Am2716 or 16 Am2732 EPROMs (or pin-equivalent ROMs) as well as up to 16 1K x 8 and 2K x 8 static RAM devices. The Am95/5132 provides intermixed storage for up to 64K bytes of PROM and up to 32K bytes of RAM. On-board jumpers apply the proper voltage and control signals to the various memory devices. Memory mapping is provided by four bipolar PROMs. Two latching 8-bit data bus registers, controlled by I/O ports, provide a chip-enable mask that enhances mapping versatility and board operation.

The I/O section of the board has an enhanced ability to communicate with external devices. An Am9551 Programmable Communications Interface drives a serial I/O port. Three parallel I/O ports (24 bits) are controlled by an Am8255A Programmable Peripheral Interface.

An Am9513 System Timing controller is included on the I/O section to provide enhanced timing and counting capability. The system timing controller contains five high-speed 16-bit counters, two of which can be configured to operate as a 24-hour time-of-day clock.

Am95/6011 ARITHMETIC PROCESSING UNIT BOARD



- Uses the Advanced LSI Am9511A Arithmetic Processing Unit
- 32-Bit Floating-Point Arithmetic
- 16-Bit and 32-Bit Fixed-Point Arithmetic
- Transcendental Functions
- Data Format Operators for Fixed-Point and Floating-Point Conversions
- Plug and Bus Compatible with:
  Intel MDS-800 Intellec* Microcomputer Development System
  Intel's SBC-80/10-20 Single Board Computer Family
- Switch Selectable I/O Addresses
- Independent On-Board Counter Operates under CPU Control to Monitor APU Execution Times
- Application Program Available for Evaluating the Am9511A on an Intel MDS

The Am95/6011 Arithmetic Processor Unit Board is designed to be a high-speed arithmetic processor enhancement to the Intel MDS-800 Intellec Microcomputer Development System, the Intel Intellec Series II Microcomputer Development System and the Intel SBC Single Board Computer family. The Am95/6011 APU board features the ability to perform addition, subtraction, multiplication and division in either single precision (16-bit) fixed-point, double precision (32-bit) fixed-point, or floating-point (32-bit) format. This board also performs advanced trigonometric, inverse trigonometric and log functions in 32-bit floating-point format. The mathematical capability of a wide variety of microprocessor based systems can be enhanced by the 11 derived functions and 17 format and data manipulation commands executed by this APU board.

An on-board 16-bit counter provides a means of monitoring the Am9511A APU operating speed, or measuring other event durations. For interrupt driven systems, the APU board can be jumper-selected to generate one of four interrupts when an arithmetic operation has been completed. The Am95/6011 occupies four consecutive input/output address ports, which can be switch selected to meet the requirements of the application. An optional application program for use with the APU board is available on a flexible disk which can be executed on an Intel Microcomputer Development System operating under ISIS-II*. The application program allows all APU commands to be executed and produces execution time information.

*Registered trademark of Intel Corporation.

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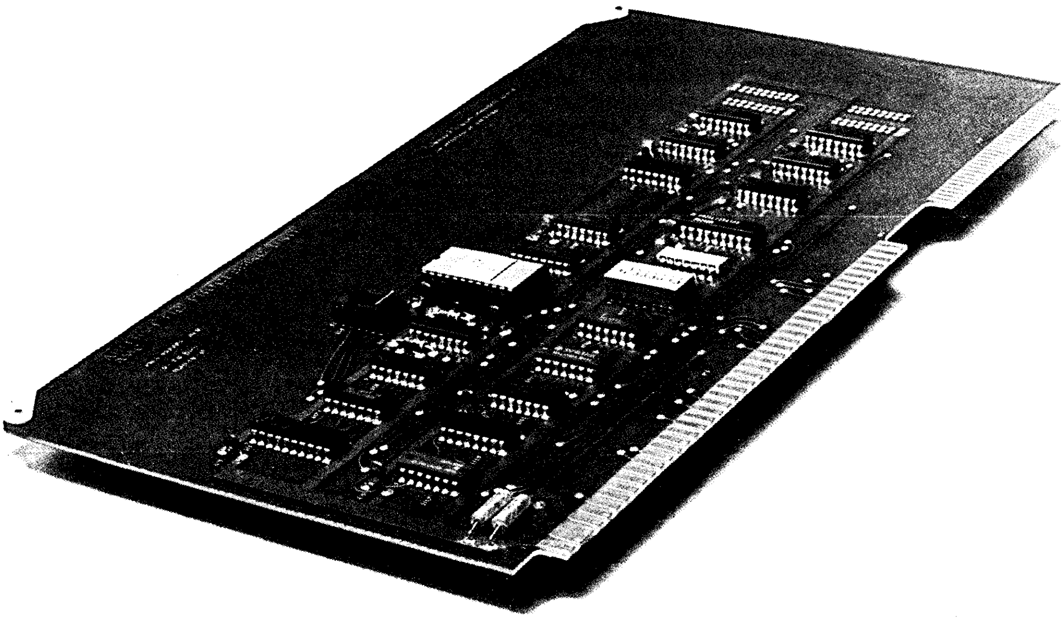
Am95/6012 ARITHMETIC FLOATING-POINT PROCESSOR UNIT BOARD (IEEE DATA FORMAT)



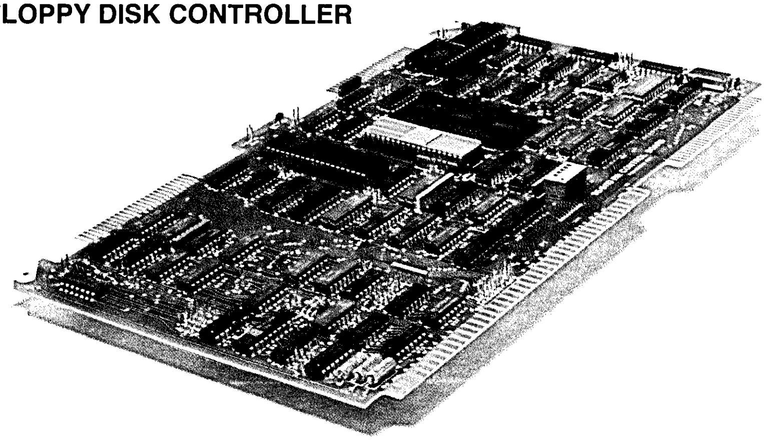
- Floating-Point Processor
- 32-Bit and 64-Bit Floating-Point Arithmetic
- Conforms to IEEE Data Format
- Single Board Design
- Uses Advanced LSI Am9512 Arithmetic Processing Unit
- Low Power Consumption
- Plug and Bus Compatible with:
  Intel Intellec* Microcomputer Development Systems
  Intel's iSBC* Family of Single Board Computers
- Switch Selectable I/O Addresses
- Requires Only Four Input/Output Addresses
- Independent On-Board Counter Operates under CPU Control to Monitor APU Execution Times

*Registered trademark of Intel Corporation.

The Am95/6012 Floating-Point Arithmetic Board functions as a high-speed arithmetic processor enhancement to Intel Intellec Series of Microprocessor Development Systems and to the iSBC Single Board Computer family utilizing the SBC-80 bus (Multibus*). The Am95/6012 Floating-Point Processor Board features the ability to perform addition, subtraction, multiplication and division in either single precision (32-bit) or double precision (64-bit) floating-point format. The data format of the computed results produced by the Am95/6012 board conforms to the IEEE floating-point format and the Intel standard. All arithmetic operations are performed by an Am9512 LSI arithmetic processing unit.

An on-board 16-bit clock cycle counter provides a means of monitoring the Am9512 APU operating speed and measuring event durations in microprocessor clock cycles. For interrupt driven systems, the Am95/6012 Floating-Point Processor Board can be jumper-selected to generate one of four bus interrupts when an arithmetic operation has been completed. The Am95/6012 board occupies four consecutive Input/Output (I/O) address ports which can be switch selected to meet individual requirements and applications.

Am95/6110 FLOPPY DISK CONTROLLER



- Controls Four 8-Inch Flexible Disk Drives
  Single- or Double-Sided
  IBM 3740 Soft Sector Media Format
- Distributed I/O Processor Architecture
  Performs all disk I/O without host CPU intervention by means of its own dedicated processor, control firmware and RAM buffer .
- Control Firmware
  Provides program code for read, write, execute and initialize plus commands for error checks and status words
- High Throughput by Means of On-Board DMA Controller
  Programmable for either block or byte mode transfers
  20-bit addressing allows transfers up to 1M byte
- Confidence Check
  Automatically provides a diagnostic check on start-up of RAM, ROM, FDC and DMA
- Versatile Interface
  SBC/Multibus* compatible, single or multimaster environment
  Operates as an intelligent slave
  Interfaces to both 8-bit and 16-bit CPU
- Multibus SBC-80 Compatible

The Am95/6110 Floppy Disk Controller is a high-speed board providing the OEM with a powerful and easy-to-use means to interface industry standard 8-inch single density flexible disk drives to Multibus compatible OEM computers such as the Am95/4000 series MonoBoard™ and SBC-80 series single board computers.

The 6.75 x 12 in. board includes the Am8085A processor, the FD1771 Floppy Disk Controller, 1K byte of high-speed static RAM buffer, the Am9517A DMA Controller, 2K bytes of EPROM with firmware (sockets for 3K bytes are provided) and five mailbox registers.

The Am8085A processor provides the local intelligence which frees the host CPU while it concurrently processes all I/O transfers.

Under control of the Am8085A and on-board operating firmware, the FD1771 controller chip selects a particular disk drive, accesses a specific location on that disk, formats the data and writes onto, or reads from, that disk. The Am95/6110 controller also offers a number of features such as automatic head unloading after eight idle disk rotations for longer diskette life, as well as automatic track-seek-verify, automatic CRC generation and check, and write protection verification.

The Am9517A DMA Controller allows high-speed data transfers, either in block mode in combination with the 1K byte RAM buffer or in byte mode from the FD1771 chip. In block mode, up to seven sectors can be transferred with a single request to the bus. In byte mode, the data is transferred directly between a disk drive and the host system, with a bus request necessary for each byte transfer. The transfer rates are selectable according to the speed of the host system memory.

All communications between the host CPU and the Am95/6110 unit take place independently through five mailbox registers.

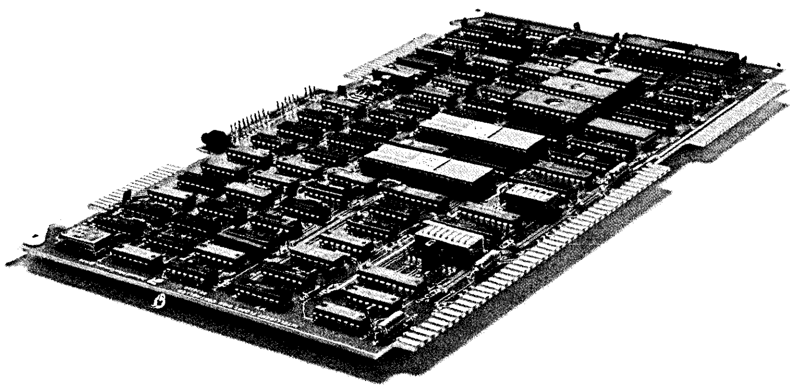
The Am95/6110 can drive up to four 8-inch flexible disk drives, single- or double-sided, IBM 3740 soft sector, single density. It is compatible with Shugart SA800, SA850, Memorex 550, 552, Siemens FDD120 and CDC 9406-3.

The Am95/6110 is compatible with the SBC/Multibus bus standard. It can operate in a single master or a multimaster environment, and interfaces to both 8-bit and 16-bit CPUs. It can generate one of eight jumper-selectable interrupts at the end of each operation.

*Registered trademark of Intel Corporation.

6

Am95/6120 INTELLIGENT FLOPPY DISK CONTROLLER



- Controls Up to 4M Bytes of Floppy Disk Storage
- Handles Four 8-Inch or 5¼-Inch Drives
- Intermixed Single-and Dual-Density Plus Single- and Double-Sided Drives Managed by One Controller
- Compatible with Shugart, Memorex, CDC, Siemens, Remex, Pertec, MPI 8-Inch Drives and Shugart-Type 5¼-Inch Drive
- Distributed I/O Processor Architecture
  Performs all disk I/O without host CPU intervention by means of its own microprocessor, control firmware, RAM buffer and LSI peripheral circuits
- Control Firmware
  Provides program code for read, write, execute and initialize, plus commands for error checks, status words and operation verification
- High Throughput by Means of On-Board DMA Controller (1.8M Bits/Second) with Programmable Block, Burst or Byte Mode Transfers.
- 20-Bit Addressing Allows Transfers up to 1M Byte
- Confidence Check
  Automatically provides a diagnostic check on start-up of RAM, ROM, FDC and DMA
- Automatic System Boot Capability on Disk
- Multibus* SBC-80 Compatible

The Am95/6120 Intelligent Floppy Disk Controller is a high-speed system component interfacing and controlling up to four 8-inch and 5¼-inch floppy disk drives. It supports both single- and dual-density as well as single- and double-sided drives intermixed in Multibus-compatible systems.

The 6.75 x 12-inch controller board includes an Am8085A processor, an FD1793 floppy disk controller, 1K bytes of high-speed static RAM, an Am9517A DMA controller, 3K bytes of EPROM firmware and five interfacing mailbox registers.

The Am8085A CPU provides local processing power and, together with the intelligence of the on-board firmware, frees the host CPU while it concurrently processes all disk I/O transfers. Under control of the on-board MPU and firmware, the FD1793 controller chip selects a particular disk drive, accesses a specific location on the disk, formats data and writes onto, or reads from the disk.

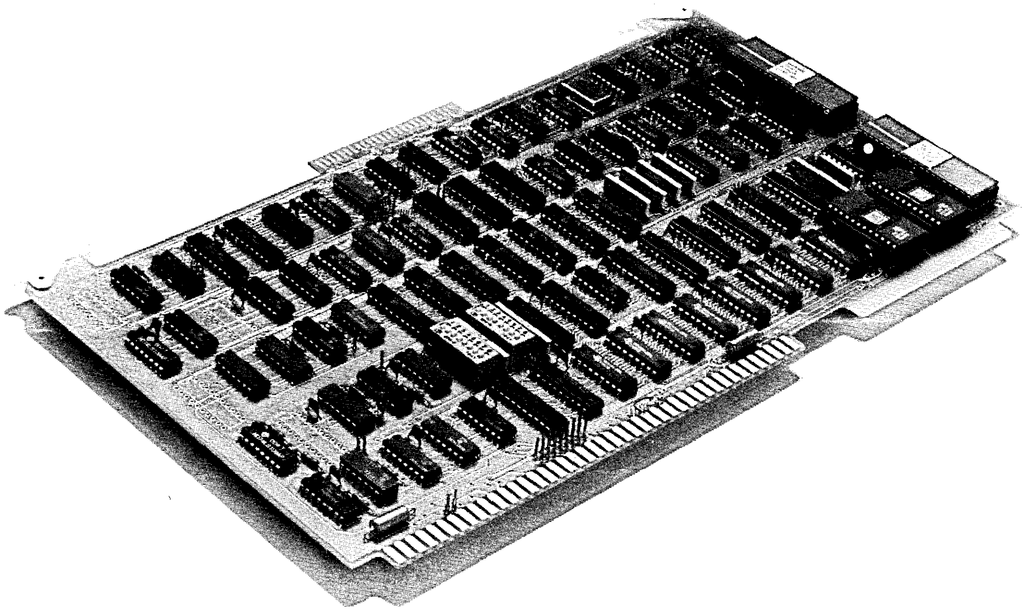
The Am9517A DMA controller allows high-speed transfers at up to 1.8M bits/second in block or programmable burst mode in combination with the 1K byte RAM buffer or in byte mode directly from the FD1793 controller. In byte mode, data is transferred directly between a disk drive and the host system, with a bus request necessary for each byte transfer. Transfer rates of up to 225,000 bytes/second are contingent upon system memory speed and interim bus requests and contention.

Block mode transfers a sector of information as a continuous data stream. A software-selectable burst mode can be employed with the amount of information in the burst transfer programmed in 16 or 64 byte increments. A rich set of status and verification commands and responses built into the firmware intelligently monitors system operations and allows recovery routines to be implemented. Operating errors such as mounting a disk that does not match the program code density designation are detected and reported.

The Am95/6120 is compatible with the SBC/Multibus bus standard. It can operate in a single master or MultiMaster environment. It can generate one of eight jumper-selectable interrupts at the end of each operation.

*Registered trademark of Intel Corporation.

Am95/6220 CARTRIDGE DISK CONTROLLER



- Manages Up to 80M Bytes of High-Speed Disk Storage
  Supports four 5440/2315 cartridge drives
  Single- and double-density
  Standard Diablo type 44B interface
- Intelligent Capacity for High Throughput
  Am8085A microprocessor
  4K RAM buffer
  4K on-board PROM firmware
  Am9517A DMA controller
- On-Board Firmware for Ease of Programming
  High level commands
  Selectable record sizes
  Interlace capability for improved latency
  Data transfers across track/cylinder boundaries
- Provides One Megabyte Bus Addressing (20-Bit)
- Multibus* and SBC-80 Compatible

The Am95/6220 Intelligent Cartridge Disk Controller features microprocessor based architecture for increased system throughput and a simplified command structure for ease of programming. As many as four 10-20 megabyte drives can be controlled by the Am95/6220 Multibus-based board to manage disk files to a capacity of 80 megabytes. The Controller supports IBM 5440/2315 cartridge type drives using a Diablo 44B interface with transfer rates up to 5M bits/second.

*Registered trademark of Intel Corporation.

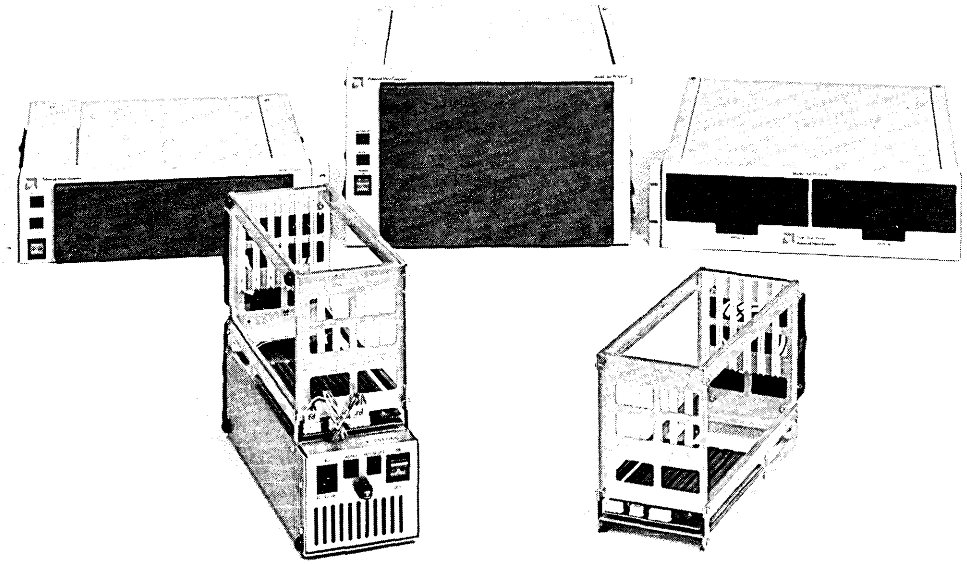
The Am95/6220 Controller incorporates an Am8085A microprocessor, a 4K byte RAM buffer, 4K bytes of PROM-based firmware and a high-speed Am9517A DMA controller. The Am8085A MPU provides on-board processing power and, together with the intelligence of the PROM firmware, frees the host CPU while it concurrently processes all disk I/O transfers. This configuration supports enhanced system throughput and requires minimal overhead from system software. All data transfers between main memory and the Cartridge Disk Controller use high-speed DMA facilities. Commands from the host CPU are sent by programmed I/O to the RAM buffer on the Am95/6220 through a single I/O port as a 12-byte command string.

Under control of the Am8085A MPU and the on-board firmware, the controller selects a particular disk drive, accesses the appropriate cylinder and then reads from or writes to appropriate track(s) and sectors. Multiple sector transfers are supported by a single read/write command along with the ability to cross cylinder and track boundaries. The Controller supports both single- and double-density formats with selectable record sizes.

The Am95/6220 Controller is compatible with both Multibus and SBC-80 standards. Other features include its single-board design, low supply current of 2.5A at +5V only, and support of protected and defective tracks.

6

CARD CAGES AND SYSTEM CHASSIS



Am95/6440 and Am95/6448 Card Cages

- All Metal Construction; Six Slots Expandable to 18
- Available with (Am95/6448) and without (Am95/6440) Integrated Switching Power Supply

The Am95/6440 Standard Card Cage consists of a 6-slot Multibus*-compatible backplane mounted in a rigid metal enclosure. Also included are three power supply connectors, card guides to accommodate six Multibus-compatible printed circuit boards and Multibus-compatible signal terminators.

The Am95/6448 Card Cage is similar to the Am95/6440 except that it contains a high-efficiency switching-type power supply. It furnishes ±5 and ±12Vdc (regulated) Multibus voltage requirements. The power supply module, Multibus backplane, input panel, cooling fans and metal frame are integrated into a compact trim design for use in industrial chassis and for benchtop use.

Am95/6450 and Am95/6452 System Chassis

- 19-Inch Rack Mounted
- 7-Board (Am95/6450) or 14-Board (Am95/6452) Capacity
- Front Access Panel for Easy Board Installation, Removal and Inspection
- Power, Reset and Interrupt Switches
- 25A Switching Power Supply (Am95/6452 Optional to 50A)
- Cooling Fans
- Rear Connector Panel and Cable Routing Channel

Both the Am95/6450 and the Am95/6452 system chassis incorporate a Multibus-based card cage and switching power supply into an EIA rack-mountable metal enclosure. Most features of these units are identical except for board capacity: the larger size of the Am95/6452 accommodates up to 14 horizontally mounted printed circuit boards, while the Am95/6450 accommodates seven boards.

Am95/6454 Floppy Disk Subsystem

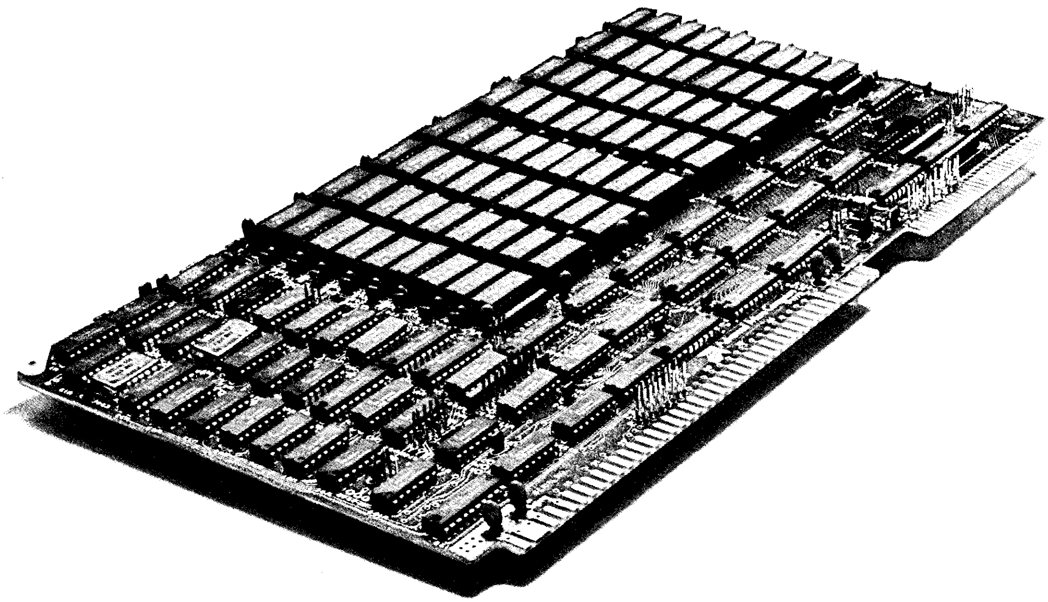
- Dual 8-Inch Drives; Single-/Double-Density
- Integrated Power Supply and Fan
- 19-Inch Rack-Mountable

The Am95/6454 Floppy Disk Subsystem houses two 8-inch floppy disk drives and power supply in a 19-inch rack-mountable enclosure. The drives are arranged horizontally, side by side, in a 5¼-inch high enclosure that minimizes rack space required. The drives support both single- and double-density data storage using IBM 3740 and S-34 media format in single-sided operation.

A built-in supply furnishes the required power for drive motors and associated logic circuit. A cooling fan supplies filtered air to the unit through a cleanable metal mesh screen. Controller logic interfaces to the subsystem through two 50-pin connectors mounted on the enclosure's rear panel.

*Registered trademark of Intel Corporation.

Am96/1000 SERIES RANDOM-ACCESS MEMORY BOARDS



- 32K, 64K, 96K and 128K Byte Storage Options Available
- High-Speed Operation Supports Up to 4.0MHz Operation with High-Performance AmZ8000 CPUs
- 8-Bit/16-Bit Data Bus Compatibility for Most 8- or 16-Bit Microcomputers
- On-Board Transparent Refresh
- Jumper Option for Advanced Acknowledge (AACK) Signal to Improve Response Time and Throughput
- Optional Parity Option in both Byte and Word Mode with Interrupt Capability
- Dual Bus Accesses Provide a Global RAM Link between P_1 MultiMaster Connector and P_2 Auxiliary Connector
- Address Space in 4K Byte Boundaries
- Multibus* and SBC-80 Compatible

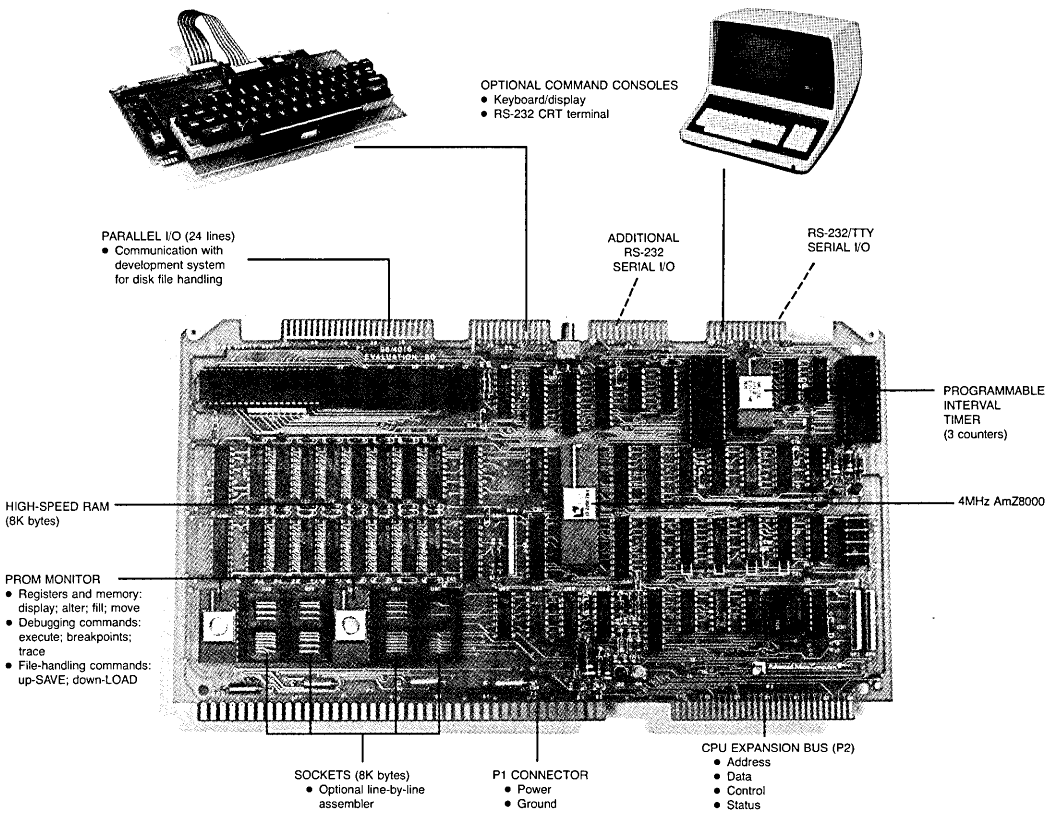
The Am96/1000 series memory boards are a family of high-density, high-performance random-access memory storage units. These AMC Supercomponent boards incorporate advanced features to meet the increasing demand for denser, faster, versatile and intelligent memory in SBC-80 based systems. Furthermore, Am96/1000 RAM boards support a second bus via the P2 edge connector to extend their capability to special applications involving AmZ8000 Evaluation Boards and dual bus systems. The Am96/1000 series is populated with 16K dynamic RAM components with board-level capacities of 32K bytes, 64K bytes, 96K bytes and 128K bytes . . . and all versions are available with a parity option. They are Multibus compatible as well as 8-bit and 16-bit data bus compatible. The boards support 4.0MHz CPU operation and are particularly suited for use with high-performance microprocessors such as the AmZ8000.

This Am96/1000 series is Multibus compatible over the P1 connector, but also features the address, data and control lines brought out on the auxiliary P2 connector. This arrangement extends the capability of the board to support other CPU bus structures. This dual-bus capability also offers a common RAM storage area and global link between separate computer systems interfaced via the P1 (Multibus) and P2 (auxiliary) connectors on the RAM board.

The Am96/1000 Memory Boards can be mapped as contiguous memory on 4K boundaries in a one-megabyte address space. Memory features include fast memory access and cycle times on a standard SBC board format.

*Registered trademark of Intel Corporation.

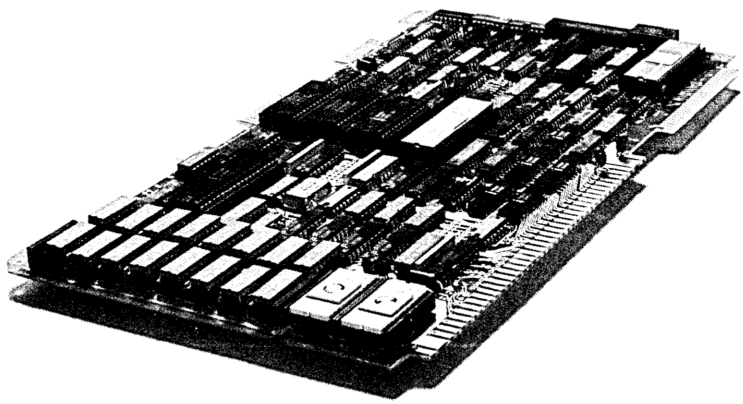
Am96/4016 AmZ8000 EVALUATION BOARD



- Fully Assembled and Tested Computer Board
- AmZ8002 Microprocessor – 4MHz Operation
- 8K Bytes (4K Words) of RAM Memory
- Sockets for Up to 12K Bytes of PROM/EPROM
- PROM-Based Monitor with Debugging Capability
- Two Serial Ports with Programmable Baud Rates
- 24-Line Parallel Port (Three Byte-Wide Ports)
- Three Interval Timers
- Optional PROM-Based ASCII Assembler
- Interfaces for Direct I/O to a CRT Terminal or the Am96/4016-KBD Keyboard/Display Board
- SBC-80 Physical Size
- Can Be Used as an Execution Vehicle with the AmSYS8/8 Development System
- Provides Up-Load/Down-Load Capability with the AmSYS8/8 Development System

The new generation of microprocessors is here. Now you can evaluate the AmZ8000 with the system-oriented Am96/4016 Evaluation Board that makes it easy to utilize the latest microcomputer technology. The Am96/4016 Evaluation Board puts a versatile and intelligent tool in the hands of engineers, designers and programmers allowing them to explore the exceptional capabilities of the AmZ8000. The Am96/4016 integrates powerful hardware and extensive software resources on an assembled and tested printed-circuit board that allows the evaluation of the AmZ8000 by the addition of a power supply and I/O device. Power can be provided by plugging the board into an SBC-80 type card cage, AMC's development system, or with a lab supply. Two ports are provided to interface to a CRT terminal or to the Am96/4016-KBD keyboard/display board.

Am96/4116 AmZ8000 16-BIT MONOBOARD™ COMPUTER



- AmZ8002 CPU with 4.0MHz Operation
  Powerful instruction set
  8 addressing modes
  Wide variety of data types ranging from bits to long words
- 32K Bytes of Dual-Ported High-Speed Memory Supporting Advanced Acknowledge (AACK) Signal
- 8K Bytes of PROM/ROM Space
- Addresses Up to One Megabyte of Memory with Internal Paging Arrangement
- Two RS-232 Serial I/O Ports (Am9551)
- 24 Parallel I/O Lines (Am8255A)
- Five Programmable Counter/Timers at 4.0MHz (Am9513)
- Multimode Interrupt Control (23 Sources, 10 Lines)
  Vectored interrupts (eight lines)
  Non-maskable interrupts (four OR-ed sources)
  Maskable interrupts (one line, multiple sources)
- Power-fail capability
- Compatible with Multibus* Standard, SBC-80 Card Format

The Am96/4116 MonoBoard Computer is a complete single-board computer with exceptional CPU power provided by a 16-bit AmZ8002 microprocessor operating at 4.0MHz. It is fully compatible with the Multibus bus standard and SBC-80 card format for ease and versatility of system integration. MultiMaster bus control and arbitration logic enhance its computing capability and associated system performance.

Both random access memory and sockets for PROM/ROM memory are provided. Further capability is added by on-board LSI peripheral circuits that furnish input/output, timing/counting and interrupt control.

*Registered trademark of Intel Corporation.

On-board memory consists of 32K bytes of dual-ported high-speed RAM along with dual sockets for up to 8K bytes of PROM/ROM. Two types of I/O capability are included: two serial I/O ports implemented as RS-232 interfaces; and 24 lines of software-configurable parallel I/O. A multiple mode interrupt structure including a programmable interrupt controller supports three types of interrupt signals. To provide for many types of counting, timing and resynchronizing requirements, a programmable system timing controller is incorporated.

Other AMC Multibus-compatible board products can be used with the Am96/4116 MonoBoard Computer to configure powerful and versatile computer systems for a wide variety of applications.

Of all the components in a computer system, the central processing unit generally determines the system's capability and overall performance level. The 16-bit AmZ8002 microprocessor on the Am96/4116 MonoBoard Computer provides high throughput, efficient programming and versatility of applications.

The AmZ8002 is a general-purpose CPU whose architecture centers around sixteen 16-bit versatile registers. It manages a 16-bit address bus to permit direct addressing of a 64K byte memory space. Facilities are included to maintain three distinct address spaces – code, data and stack. The AmZ8002 implements a powerful yet orderly instruction set with flexible addressing modes. These instructions operate on bits, bytes, BCD digits, 16-bit words, long words (32-bit), byte strings and word strings.

Two modes of operation, Normal and System, provide better I/O handling and privileged instructions. This feature is a strong benefit for advanced system architectures requiring multitasking and multiuser capability, or when it is important to provide protected interaction of user application code with an operating system.

6

MILITARY, HI-REL AND PRODUCT ASSURANCE

Advanced Micro Devices (AMD) was conceived on the premise that there was a place in the semiconductor community for a manufacturer dedicated to excellence. In product assurance procedures, AMD is unique.

The Rome Air Development Center (RADC), the U.S. Air Force's principal authority on component reliability, has issued MIL-HDBK-217 which indicates that parts processed to MIL-STD-883, Class C yield a product nearly two times better in failure rates than the industry commercial average. Only AMD processes all integrated circuits, commercial as well as military, to this demanding military standard. In addition, documentation, design, processing and assembly workmanship guidelines are patterned after MIL-M-38510 specifications. Commercial and industrial users receive the quality and reliability benefits of this aerospace-type screening and documentation at no additional cost.

The AMD Sunnyvale, California, facility has been certified to produce JAN parts to MIL-STD-883, Class B and C, under Military Specification MIL-M-38510. The AMD standard programs for Class C, B and S devices for military and commercial applications are outlined within this section. These programs will cover the majority of system requirements today. Alternative screening flows for specific user needs can be performed on request. Check with your local sales office for further information.

STANDARD PRODUCT TESTING CATEGORIES

AMD offers integrated circuits to three standard testing categories:

1. Commercial Operating Range (0 to 70°C, typ)
2. Military Operating Range (−55 to +125°C, typ)
3. JAN Qualified Military Product

Categories 1 and 2 are available on most circuits; category 3 is offered on a more limited line. Additional testing and screening services are available to special order.

STANDARD PRODUCT ASSURANCE CATEGORIES

AMD devices are available in the three standard classes of product assurance defined by MIL-STD-883. As a minimum, every device shipped meets the screening requirements of Class C.

Class C – For commercial and ground-based military systems where replacement can be accomplished without difficulty.

According to MIL-HDBK-217, this assures relative failure rates 1.7 times better than that of regular industry commercial product.

Class B – For flight applications and commercial systems where maintenance is difficult or expensive and where reliability is vital.

Devices are upgraded from Class C to Class B by burn-in screening and additional testing.

According to MIL-HDBK-217, Class B failure rate is improved 30 times over regular industry commercial product. AMD Class B processing conforms to MIL-STD-883 requirements. MIL-HDBK-217 indicates that full Class B processing may provide failure rates as much as two times better than "equivalent" or "pseudo" Class B programs.

Class S – For space applications where replacement is extremely difficult or impossible and reliability is imperative.

Class S screening includes x-ray and other special requirements of the user.

The 100% screening and quality conformance testing performed within these programs is shown in Tables I, II, III and IV. A full description of the process flow is provided in Product Assurance Document 15-010, available on request.

Table I – Class C Screening Flow

Screening Procedure per MIL-STD-883 Method 5004, Class C		COMMERCIAL OPERATING RANGE	MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES	HERMETIC PACKAGE ONLY	
		Flow C1 Commercial Product	Flow C3 Military Product	Flow C4 JAN Qualified Product
Screen	**Test Method**			
VISUAL AND MECHANICAL				
Internal Visual	2010, Condition B	100%	100%	100%
High Temperature Storage	1008, Condition C, 24 hours	100%	100%	100%
Temperature Cycle	1010, Condition C	100%	100%	100%
Constant Acceleration	2001	100% (Note 1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (Note 1)	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(Note 2)	–	–
Functional	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(Note 2)	–	–
Switching (ac) or Dynamic	At 25°C, nominal power supply	(Note 2)	–	–
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample
Sample Tests	Group B	–	–	Sample
	Group C	–	–	Sample
	Group D	–	–	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%

Table II – Group A Quality Conformance Levels

Advanced Micro Devices employs the military-recommended LTPD sampling system to assure quality. MIL-STD-883, Method 5005, TABLE I, Group A, subgroups 1 through 9 as appropriate to the device family are performed on every lot. Quality levels defined for Class B product are applied to both Class B and Class C orders.

	LTPD	Min Sample Size
Subgroup 1 – Static tests at 25°C	5	45
Subgroup 2 – Static tests at maximum rated operating temperature	7	32
Subgroup 3 – Static tests at minimum rated operating temperature	7	32
Subgroup 4 – Dynamic tests at 25°C – LINEAR devices	5	45
Subgroup 5 – Dynamic tests at maximum rated operating temperature – LINEAR devices	7	32
Subgroup 6 – Dynamic tests at minimum rated operating temperature – LINEAR devices	7	32
Subgroup 7 – Functional tests at 25°C	5	45
Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 – Switching tests at 25°C – DIGITAL devices	7	32
Subgroup 10 – Switching tests at maximum rated operating temperatures – DIGITAL devices	*	
Subgroup 11 – Switching tests at minimum rated operating temperatures – DIGITAL devices	*	

*These subgroups, where applicable, are usually performed during initial characterization only for all except JAN Qualified Product.

See notes on following page.

Table III – Class B Integrated Circuits (Class C plus burn-in screening and additional testing)

Screen	Test Method	COMMERCIAL OPERATING RANGE	MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES	HERMETIC PACKAGE ONLY	
Screening Procedure per MIL-STD-883 Method 5004, Class C		Flow B1 Commercial Product	Flow B3 Military Product	Flow B4 JAN Qualified Product
VISUAL AND MECHANICAL				
Internal Visual	2010, Condition B	100%	100%	100%
High Temperature Storage	1008, Condition C, 24 hours	100%	100%	100%
Temperature Cycle	1010, Condition C	100%	100%	100%
Constant Acceleration	2001	100% (Note 1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (Note 1)	100%	100%
BURN-IN				
Interim (Pre Burn-in) Electricals	Per applicable device specification	100%	100%	100%
Burn-in	1015, 160 hours at 125°C or equivalent (Note 6)	100% (Note 3)	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(Notes 2, 3)	100%	100%
Functional	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(Notes 2, 3)	100%	100%
Switching (ac) or Dynamic	At 25°C, nominal power supply	(Note 2)	100%	100%
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample
Sample Tests	Group B	–	(Note 4)	Sample
	Group C	–	(Note 4)	Sample
	Group D	–	(Note 4)	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%

Notes:
1. Not performed on molded packages.
2. All MOS RAMs and many other MOS devices receive ac testing and 100% dc screening at high temperature and power supply extremes as standard. Certain other products are tested at the most critical extreme temperature to assure accuracy of device selection or are sampled at Group A (Table II).
3. Am2900 LSI products receive a 96 hour burn-in, plus 100% dc screening at high temperature and power supply extremes.
4. Available to special order.
5. Without optical aid for commercial devices.
6. Unless device data sheet specifies otherwise.

Table IV — Class S Screening Flow

Screening Procedure Class S		MILITARY OPERATING RANGE HERMETIC PACKAGE ONLY	MILITARY OPERATING RANGE HERMETIC PACKAGE ONLY
Screen	**Test Method**	**Flow S1 Basic S Flow**	**Flow S2 Extended Class S Processing**
SEM Scanning Electron Microscope	2018	Wafer Lot Sample	Contact Advanced Micro Devices Sales for Details
ASSEMBLY Class S Process Monitors	–	Periodic sampling	
VISUAL AND MECHANICAL			
Internal Visual	2010, Condition A	100%	
High Temperature Storage	1008, Condition C, 24 hours	100%	
Temperature Cycle	1010, Condition C	100%	
Constant Acceleration	2001, Condition E	100%	
PIND Particle Impact Noise Detection	2020, Condition A or B	100% (Note 1)	
Serialization		100%	
X-RAY Radiographic	2012, Two views	100%	
BURN-IN			
Interim (Pre Burn-in) Electricals	Per applicable device specification	100% (Note 2)	
Burn-in	1015, 240 hours at 125°C or equivalent	100% (Note 3)	
Interim (Post Burn-in) Electricals	Per applicable device specification	100% (Note 2)	
FINAL ELECTRICAL TESTS		AMD Data Sheet	
Static (dc)	a) At 25°C, and power supply extremes	100%	
	b) At temperature and power supply extremes	100%	
Functional	a) At 25°C and power supply extremes	100%	
	b) At temperature and power supply extremes	100%	
Switching (ac) or Dynamic	At 25°C nominal power supply	100%	
SEAL Hermeticity, Fine and Gross	1014	100%	
QUALITY CONFORMANCE			
	5005, Group A (See Table II)	Sample	
Sample Tests	Group B	Sample (Note 4)	
	Group D	Sample (Note 4)	
EXTERNAL VISUAL	2009	100%	

Notes:
1. 100% screen, one pass.
2. Read and record requirements to be specified as applicable to particular device type.
3. Consult device data sheet.
4. Available to special order.

STANDARD PRODUCT SCREENING SUMMARY AND ORDERING INFORMATION

1. COMMERCIAL PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic and molded packages.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class C and Class B options.

Class C
- Order standard AMD part number.
- Marked same as order number.

Examples: AM25LS374DC, SN74LS374J

Class B
- Burn-in performed in standard AMD circuit.
- Order standard AMD part number, add suffix B (or /883B for 1, 2 and 300 Series Linear devices).
- Marked same as order number.

Examples: AM25LS374DC-B, SN74LS374J-B

2. MILITARY PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic package only.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class B and Class C options.

Class C
- Order standard AMD part number.
- Marked same as order number.

Examples: AM25LS374DM, SN54LS374J

Class B
- Burn-in performed in AMD circuit condition.
- ac at 25°C, dc and functional testing at 25°C as well as temperature and power supply extremes performed on 100% of every lot.
- Quality conformance testing, Method 5005, Groups B, C and D available to special order.
- Order standard AMD part number, add suffix B.
- Marked same as order number.

Examples: AM25LS374DM-B, SN54LS374J-B

Class S
- Contact AMD sales for ordering information and products covered by this screening flow.

3. JAN QUALIFIED PRODUCT

- JAN QPL listed products only.*
- Screened per MIL-STD-833, Method 5004.
- Electrically tested to JAN detail specification (slash sheet).
- Manufactured in DESC certified facility.
- Quality conformance testing, Method 5005, Groups A, B, C and D performed as standard and must be completed prior to shipment.

Class B (Flow B4)
- Burn-in performed in circuit condition approved for JAN devices.
- Order per military document.
- Marked per military document.

Example: JM38510/30106BEB

*In certain cases where JAN Qualified Product is specified but is not available, Advanced Micro Devices can provide devices to the electrical limits and burn-in criteria of the slash sheet. This class of product has been called JAN Equivalent and marked M38510/ by some manufacturers. This identification is no longer permitted by DESC. Check with your local sales office for availability of specific device types.

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