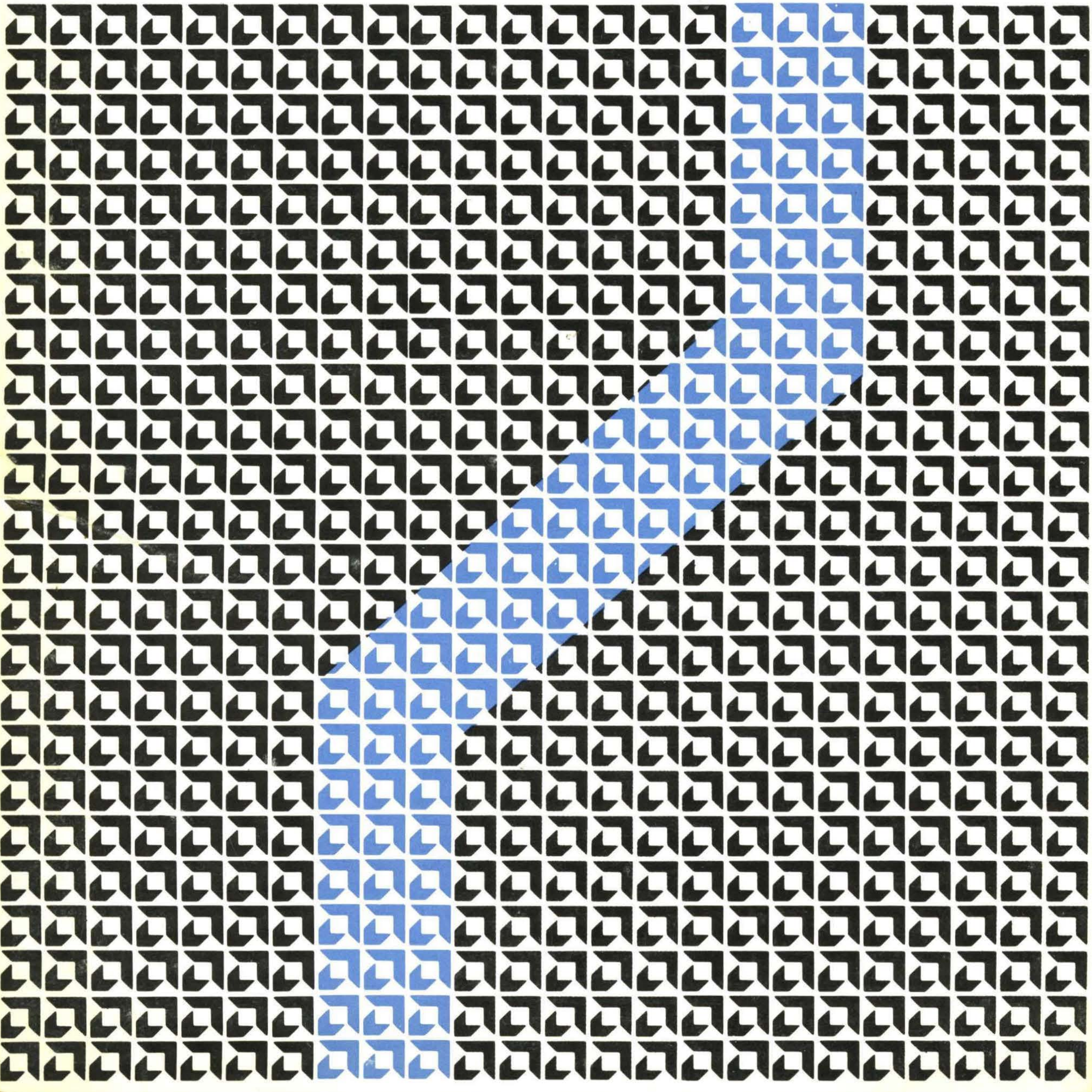
Advanced
Micro
Devices, Inc.

# MOS/LSI Data Book



# Advanced Micro Devices
# MOS/LSI Data Book

## INTRODUCTION

*The first metal-oxide semiconductor (MOS), large-scale integrated (LSI) circuits were introduced in the mid-sixties. Since then, the density of MOS/LSI components has doubled every year. At the same time the cost per function has declined even faster. These developments have had a profound effect upon every aspect of electronics design and application.*

*Of all the devices that have been developed to utilize the high-density, low-power characteristics of MOS/LSI, none have had as great an impact as microprocessors and memories – two areas in which Advanced Micro Devices occupies a prominent position. Microprocessors have literally revolutionized digital design by making feasible the replacement of large numbers of components with standard, relatively inexpensive microprocessor elements. The Am9080A is a pin and function compatible replacement for the industry standard 8-bit MOS microprocessor. It has electrical and timing specifications superior to those of any of its competitors. Supported by a full range of peripheral support circuits, this part has established price and technological leadership in the market.*

*The tremendous benefits offered by MOS memories in the storage of digital information have resulted in the huge growth of the semiconductor memory market, which is dominated by MOS/LSI devices. The earlier 1k (1024-bit) devices began to give way to 4k (4096-bit) devices during 1975. These are now in reliable, high-volume production with the problems experienced by early manufacturers/users solved. Now, people are already beginning to look forward to the 16k part, widely expected to be available in the second half of 1976.*

*Along with the steady increase in the number of bits in a package, improvements are being made in the existing memories. Performance, power consumption and cost are all being improved. Nowhere is this more evident than in the case of the Am9130/40, 4k static RAM family, described in this data book. These parts make available the convenience of static memories (no refresh timing and control circuitry) with performance equal to or better than the best 1k static and 4k dynamic RAMs available.*

*The key product areas of microprocessors and memories are supported by the wide range of MOS/LSI products also described in this data book.*

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Advanced Micro Devices cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in an Advanced Micro Devices' product.

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*Bipolar Support Circuit for the MOS Microprocessor

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## Dynamic R/W Random Access Memories

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* Bipolar Support Circuit for the MOS Microprocessor

# SELECTION GUIDES

## STATIC R/W RANDOM ACCESS MEMORIES

| Part Number | Organiza-tion | Maximum Access Time (ns) | Temp. Range | Supply Voltage | Outputs | Data I/O Config-uration | Package Pins | Operating Power Max. (mW) | Standby Power Max. (mW) |
|---|---|---|---|---|---|---|---|---|---|
| Am9101A | 256 x 4 | 500 | C, M | +5 | 3-State | Separate | 22 | 290 | 46 |
| Am91L01A | 256 x 4 | 500 | C, M | +5 | 3-State | Separate | 22 | 173 | 37 |
| Am9101B | 256 x 4 | 400 | C, M | +5 | 3-State | Separate | 22 | 290 | 46 |
| Am91L01B | 256 x 4 | 400 | C, M | +5 | 3-State | Separate | 22 | 173 | 37 |
| Am9101C | 256 x 4 | 300 | C, M | +5 | 3-State | Separate | 22 | 315 | 46 |
| Am91L01C | 256 x 4 | 300 | C, M | +5 | 3-State | Separate | 22 | 189 | 37 |
| Am9101D | 256 x 4 | 250 | C | +5 | 3-State | Separate | 22 | 315 | 46 |
| Am9101E | 256 x 4 | 200 | C | +5 | 3-State | Separate | 22 | 315 | 46 |
| Am9102 | 1024 x 1 | 650 | C, M | +5 | 3-State | Separate | 16 | 263 | 42 |
| Am91L02 | 1024 x 1 | 650 | C, M | +5 | 3-State | Separate | 16 | 158 | 35 |
| Am9102A | 1024 x 1 | 500 | C, M | +5 | 3-State | Separate | 16 | 263 | 42 |
| Am91L02A | 1024 x 1 | 500 | C, M | +5 | 3-State | Separate | 16 | 158 | 35 |
| Am9102B | 1024 x 1 | 400 | C, M | +5 | 3-State | Separate | 16 | 263 | 42 |
| Am91L02B | 1024 x 1 | 400 | C, M | +5 | 3-State | Separate | 16 | 158 | 35 |
| Am9102C | 1024 x 1 | 300 | C, M | +5 | 3-State | Separate | 16 | 290 | 42 |
| Am91L02C | 1024 x 1 | 300 | C, M | +5 | 3-State | Separate | 16 | 173 | 35 |
| Am9102D | 1024 x 1 | 250 | C | +5 | 3-State | Separate | 16 | 290 | 42 |
| Am9102E | 1024 x 1 | 200 | C | +5 | 3-State | Separate | 16 | 290 | 42 |
| Am9111A | 256 x 4 | 500 | C, M | +5 | 3-State | Bussed | 18 | 290 | 46 |
| Am91L11A | 256 x 4 | 500 | C, M | +5 | 3-State | Bussed | 18 | 173 | 37 |
| Am9111B | 256 x 4 | 400 | C, M | +5 | 3-State | Bussed | 18 | 290 | 46 |
| Am91L11B | 256 x 4 | 400 | C, M | +5 | 3-State | Bussed | 18 | 173 | 37 |
| Am9111C | 256 x 4 | 300 | C, M | +5 | 3-State | Bussed | 18 | 315 | 46 |
| Am91L11C | 256 x 4 | 300 | C, M | +5 | 3-State | Bussed | 18 | 189 | 37 |
| Am9111D | 256 x 4 | 250 | C | +5 | 3-State | Bussed | 18 | 315 | 46 |
| Am9111E | 256 x 4 | 200 | C | +5 | 3-State | Bussed | 18 | 315 | 46 |
| Am9112A | 256 x 4 | 500 | C, M | +5 | 3-State | Bussed | 16 | 290 | 46 |
| Am91L12A | 256 x 4 | 500 | C, M | +5 | 3-State | Bussed | 16 | 173 | 37 |
| Am9112B | 256 x 4 | 400 | C, M | +5 | 3-State | Bussed | 16 | 290 | 46 |
| Am91L12B | 256 x 4 | 400 | C, M | +5 | 3-State | Bussed | 16 | 173 | 37 |
| Am9112C | 256 x 4 | 300 | C, M | +5 | 3-State | Bussed | 16 | 315 | 46 |
| Am91L12C | 256 x 4 | 300 | C, M | +5 | 3-State | Bussed | 16 | 189 | 37 |
| Am9112D | 256 x 4 | 250 | C | +5 | 3-State | Bussed | 16 | 315 | 46 |
| Am9112E | 256 x 4 | 200 | C | +5 | 3-State | Bussed | 16 | 315 | 46 |
| Am9130A | 1024 x 4 | 500 | C, M | +5 | 3-State | Bussed | 22 | 578 | 84 |
| Am9130B | 1024 x 4 | 400 | C, M | +5 | 3-State | Bussed | 22 | 578 | 84 |
| Am9130C | 1024 x 4 | 300 | C, M | +5 | 3-State | Bussed | 22 | 578 | 84 |
| Am9130E | 1024 x 4 | 200 | C | +5 | 3-State | Bussed | 22 | 578 | 84 |
| Am9140A | 4096 x 1 | 500 | C, M | +5 | 3-State | Separate | 22 | 578 | 84 |
| Am9140B | 4096 x 1 | 400 | C, M | +5 | 3-State | Separate | 22 | 578 | 84 |
| Am9140C | 4096 x 1 | 300 | C, M | +5 | 3-State | Separate | 22 | 578 | 84 |
| Am9140E | 4096 x 1 | 200 | C | +5 | 3-State | Separate | 22 | 578 | 84 |

# SELECTION GUIDES (Cont.)

## DYNAMIC R/W RANDOM ACCESS MEMORIES

| Part Number | Organiza-tion | Maximum Access Time (ns) | Temp. Range | Supply Voltages | Oper-ating Power (mW) | Outputs | Data I/O Config-uration | Package Pins | Oper-ating Power-Max. (mW) | Standby Power-Max. (mW) |
|---|---|---|---|---|---|---|---|---|---|---|
| Am9050C | 4096 x 1 | 300 | C | –5, +12 | 750 | Open Drain | Bussed | 18 | 750 | 3.0 |
| Am9050D | 4096 x 1 | 250 | C | –5, +12 | 750 | Open Drain | Bussed | 18 | 750 | 3.0 |
| Am9050E | 4096 x 1 | 200 | C | –5, +12 | 750 | Open Drain | Bussed | 18 | 750 | 3.0 |
| Am9060C | 4096 x 1 | 300 | C | ±5, +12 | 750 | 3-State | Separate | 22 | 750 | 3.0 |
| Am9060D | 4096 x 1 | 250 | C | ±5, +12 | 750 | 3-State | Separate | 22 | 750 | 3.0 |
| Am9060E | 4096 x 1 | 200 | C | ±5, +12 | 750 | 3-State | Separate | 22 | 750 | 3.0 |

## SHIFT REGISTERS

| Part Number | Organization | Mode | Speed (MHz) | Supply Voltages | Clock Phases | TTL Clocks | Recirc. Logic | Pins | Output |
|---|---|---|---|---|---|---|---|---|---|
| Am1506/1507 | Dual 100 | Dynamic | 2 | +5, –5 | Two | No | No | 8 | Single Ended |
| Am2802 | Quad 256 | Dynamic | 10 | +5, –5 | Two | No | No | 16 | Single Ended |
| Am2803 | Dual 512 | Dynamic | 10 | +5, –5 | Two | No | No | 8 | Single Ended |
| Am2804 | Single 1024 | Dynamic | 10 | +5, –5 | Two | No | No | 8 | Single Ended |
| Am2805/2807 | Single 512 | Dynamic | 4 | +5, –5 | Two | No | Yes | 10/8 | Single Ended |
| Am2806/2808 | Single 1024 | Dynamic | 4 | +5, –5 | Two | No | Yes | 10/8 | Single Ended |
| Am2825/2826 | Dual 1024 | Dynamic | 6 | +5,–10.5 | Two | No | Yes | 10/16 | Push-Pull |
| Am2827 | Single 2048 | Dynamic | 6 | +5,–10.5 | Two | No | Yes | 8 | Push-Pull |
| Am9401 | Dual 1024 | Dynamic | 2 | +5 | One | Yes | Yes | 16 | Single Ended |
| Am2809 | Dual 128 | Static | 2.5 | +5,–12 | One | Yes | Yes | 8 | Push-Pull |
| Am2810 | Dual 128 | Static | 2 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |
| Am2814 | Dual 128 | Static | 2.5 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |
| Am2833 | Single 1024 | Static | 2 | +5,–12 | One | Yes | Yes | 8 | Push-Pull |
| Am2847 | Quad 80 | Static | 3 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |
| Am2855 | Quad 128 | Static | 2.5 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |
| Am2856 | Dual 256 | Static | 2.5 | +5,–12 | One | Yes | Yes | 10 | Push-Pull |
| Am2857 | Single 512 | Static | 2.5 | +5,–12 | One | Yes | Yes | 8 | Push-Pull |
| Am2896 | Quad 96 | Static | 3 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |

## READ ONLY MEMORIES

| Part Number | Organization | Access Time (ns) | Temp. Range | Supply Voltages | Operating Power-Max. (mW) | Outputs |
|---|---|---|---|---|---|---|
| Am9214 | 512 x 8 | 500 | C, M | +5 | 263 | 3-State |
| Am9208B | 1024 x 8 | 400 | C, M | +5, +12 | 620 | 3-State |
| Am9208C | 1024 x 8 | 300 | C, M | +5, +12 | 620 | 3-State |
| Am9208D | 1024 x 8 | 250 | C | +5, +12 | 700 | 3-State |
| Am9216B | 2048 x 8 | 400 | C, M | +5, +12 | 660 | 3-State |
| Am9216C | 2048 x 8 | 300 | C | +5, +12 | 700 | 3-State |

## ERASABLE PROGRAMMABLE READ ONLY MEMORY

| Part Number | Organization | Access Time (nsec) | Temp. Range | Supply Voltages | Operating Power-Max. (mW) | Outputs |
|---|---|---|---|---|---|---|
| Am1702A | 256 x 8 | 1.0μs | C, E | –9V, +5V | 676 | 3-State |

# SELECTION GUIDES (Cont.)

## FIRST-IN FIRST-OUT MEMORIES

| Part Number | Organization | Serial I/O | Fullness Flag | Output Enable | Package Pins | Data Rate MHz | Temp. Range |
|---|---|---|---|---|---|---|---|
| Am2812 | 32 Words x 8-Bits | Yes | Yes | Yes | 28 | 0.5 | C, M |
| Am2812A | 32 Words x 8-Bits | Yes | Yes | Yes | 28 | 1.0 | C |
| Am2813 | 32 Words x 9-Bits | No | Yes | Yes | 28 | 0.5 | C, M |
| Am2813A | 32 Words x 9-Bits | No | Yes | Yes | 28 | 1.0 | C, M |
| Am2841 | 64 Words x 4-Bits | No | No | No | 16 | 1.0 | C, M |
| Am2841A | 64 Words x 4-Bits | No | No | No | 16 | 1.2 | C |

## MICROPROCESSOR

| Part Number | Clock Period | Temp. Range |
|---|---|---|
| Am9080A | 480 nsec | C, M |
| Am9080A-2 | 380 nsec | C, M |
| Am9080A-1 | 320 nsec | C |
| Am9080A-4 | 250 nsec | C |

## MICROPROCESSOR SUPPORT CIRCUITS

| Part Number | Function |
|---|---|
| Am25LS138 | 1-of-8 Binary Decoder |
| Am25LS139 | Dual 1-of-4 Decoder |
| Am8212 | 8-Bit I/O. POA. |
| Am8216 | Non-Inverting Bus Driver |
| Am8224 | Clock Generator |
| Am8226 | Inverting Bus Driver |
| Am8228 | System Controller |
| Am9551 | Programmable Communications Interface |
| Am9555 | Programmable Peripheral Interface |

# MOS CROSS REFERENCE GUIDE

| AMD Part No. | Description | Intel | Signetics | FSC | Mostek | National | TI | AMD Part No. for Improved Design |
|---|---|---|---|---|---|---|---|---|
| Am1101A | 256-bit static RAM | 1101A | 1101A<br>2501 | | MK4007 | MM1101A | TMS1101 | |
| Am1402A | Quad 256-bit dyn. S/R | 1402A | 2502 | | | MM1402A | TMS3412 | Am2802 |
| Am1403A | Dual 512-bit dyn. S/R | 1403A | 2503 | | | MM1403A | TMS3413 | Am2803 |
| Am1404A | 1024-bit dyn. S/R | 1404A | 2504 | | | MM1404A | TMS3414 | Am2804 |
| Am1405A | 512-bit dyn. recirc. S/R | 1405A | 2505 | | | | | Am2805 |
| Am14/1506 | Dual 100-bit dyn. S/R | 14/1506 | 2506 | | | | TMS3406 | |
| Am14/1507 | Dual 100-bit dyn. S/R | 14/1507 | 2507 | | | | TMS3407 | |
| Am1702A | 256 x 8 E-ROM | 1702A | 1702A | | MK3702 | 1702A | | |
| Am2101 | 256 x 4-bit static RAM | 2101 | 2101 | | | MM2101 | TMS2101 | Am9101 |
| Am2102 | 1024-bit static RAM | 2102 | 2602 | | MK4102 | MM2102 | TMS4033 | Am9102 |
| Am2111 | 256 x 4-bit static RAM | 2111 | 2111 | | | | TMS4042 | Am9111 |
| Am2112 | 256 x 4-bit static RAM | 2112 | 2112 | | | | TMS4043 | Am9112 |
| Am2401 | Dual 1024-bit dyn. S/R | 2401 | | | | | | Am9401 |
| Am2405 | 1024-bit N-channel dyn. S/R | 2405 | | | | | | Am2405 |
| Am2533 | 1024-bit static S/R | | 2533 | 2533 | | | | Am2833 |
| Am2802 | Quad 256-bit dyn. S/R 10 MHz | 1402A | | | | 1402A | | Am2802 |
| Am2803 | Dual 512-bit dyn. S/R 10 MHz | 1403A | | | | 1403A | | Am2803 |
| Am2804 | 1024-bit dyn. S/R 10 MHz | 1404A | | | | 1404A | | Am2804 |
| Am2805 | 512-bit dyn. recirc. S/R | | 2505 | | | | | Am2805 |
| Am2806 | 1024-bit dyn. recirc. S/R | | 2512 | | | | | Am2806 |
| Am2807 | 512-bit dyn. recirc. S/R | | 2524 | | | | | Am2807 |
| Am2808 | 1024-bit dyn. recirc. S/R | | 2525 | | | | | Am2808 |
| Am2809 | Dual 128-bit static S/R | | 2521 | | | | TMS3128 | Am2809 |
| Am2810 | Dual 128-bit static S/R | | | | MK1002 | | | Am2810 |
| Am2812 | 32 x 8 FIFO Memory | | | | | | | Am2812 |
| Am2813 | 32 x 9 FIFO Memory | | | | | | | Am2813 |
| Am2814 | Dual 128-bit static S/R | | | | | | TMS3114 | Am2814 |
| Am2825 | Dual 1024-bit dyn. S/R | | | | | MM40/5025 | | Am2825 |
| Am2826 | Dual 1024-bit dyn. S/R | | | | | MM40/5026 | | Am2826 |
| Am2827 | 2048-bit dyn. S/R | | | | | MM40/5027 | | Am2827 |
| Am2833 | 1024-bit static S/R | | 2533 | 2533 | | MM5058 | TMS3133 | Am2833 |
| Am2841 | 64 x 4 FIFO Memory | | | 3341 | | | | Am2841 |
| Am2847 | Quad 80-bit static S/R | | 2532 | 3347 | | | TMS3120 | Am2847 |
| Am2855 | Quad 128-bit static S/R | | | | | MM40/5055 | | Am2855 |
| Am2856 | Dual 256-bit static S/R | | | | | MM40/5056 | | Am2856 |
| Am2857 | 512-bit static S/R | | | | | MM40/5057 | | Am2857 |
| Am2896 | Quad 96-bit static S/R | | | | | | | Am2896 |
| Am3114 | Dual 128-bit static S/R | | | | | | | Am2814 |
| Am3341 | 64 x 4 FIFO | | | 3341 | | | | Am2841 |
| Am3514 | 512 x 8-bit static ROM | | | | | | | Am9214 |
| Am4025/5025 | Dual 1024-bit dyn. S/R | | | | | MM4025/5025 | | Am2825 |
| Am4026/5026 | Dual 1024-bit dyn. S/R | | | | | MM4026/5026 | | Am2826 |
| Am4027/5027 | 2048-bit dyn. S/R | | | | | MM4027/5027 | | Am2827 |
| Am4055/5055 | Quad 128-bit static S/R | | | | | MM4055/5055 | | Am2855 |
| Am4056/5056 | Dual 256-bit static S/R | | | | | MM4056/5056 | | Am2856 |
| Am4057/5057 | 512-bit static S/R | | | | | MM4057/5057 | | Am2857 |
| Am9050 | 4096 x 1 dyn. RAM 18-pin | | | | | | TMS4050 | Am9050 |
| Am9060 | 4096 x 1 dyn. RAM 22-pin | 2107 | 2604 | | | | TMS4060 | Am9060 |
| Am9080A | 8-bit microprocessor | 8080A | | | | | | Am9080A |
| Am9101 | 256 x 4 static RAM | 2101 | 2101 | | | MM2101 | TMS2101 | Am9101 |
| Am91L01 | 256 x 4 low power static RAM | | | | | | | Am91L01 |
| Am9102 | 1024-bit static RAM | 2102A | 2602 | 2102 | MK4102 | MM2102 | TMS4033 | Am9102 |
| Am91L02 | 1024-bit low power static RAM | | | | | | | Am91L02 |

# MOS CROSS REFERENCE GUIDE (Cont.)

| AMD Part No. | Description | Intel | Signetics | FSC | Mostek | National | TI | AMD Part No. for Improved Design |
|---|---|---|---|---|---|---|---|---|
| Am9111 | 256 x 4 static RAM | 2111 | 2111 | | | | TMS4042 | Am9111 |
| Am91L11 | 256 x 4 low power static RAM | | | | | | | Am91L11 |
| Am9112 | 256 x 4 static RAM | 2112 | 2112 | | | | TMS4043 | Am9112 |
| Am91L12 | 256 x 4 low power static RAM | | | | | | | Am91L12 |
| Am9130 | 1024 x 4-bit static RAM | | | | | | | Am9130 |
| Am9140 | 4096 x 1-bit static RAM | | | | | | | Am9140 |
| Am9208 | 1024 x 8 N-channel ROM | 8308 | | | | | 4700 | Am9208 |
| Am9214 | 512 x 8 static ROM | | | 3514 | 2600 | | | Am9214 |
| Am9216 | 2048 x 8 static ROM | | | | | | | Am9216 |
| Am9401 | Dual 1024-bit N-channel dyn. S/R | | | | | | | Am9401 |

# PRODUCT ASSURANCE
# MIL-M-38510 • MIL-Q-9858A • MIL-STD-883
## Complex Digital and Linear Circuits

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Three military documents provide the foundation for this program. They are:

**MIL-M-38510**—General Specification for Microcircuits
**MIL-Q-9858** —Quality Program Requirements
**MIL-STD-883**—Test Methods and Procedures for Microelectronics

**MIL-M-38510** describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. **All linear, MSI, and computer interface circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510.**

**MIL-Q-9858** identifies 28 elements of management, planning and control that are necessary in maintaining a quality program. **Advanced Micro Devices complies with all requirements of MIL-Q-9858.**

**MIL-STD-883** contains detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

**Test Method 2010** defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Standard inspection at Advanced Micro Devices includes all the requirements of Method 2010, condition B.

**Test Method 5004** defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

**Class C** — Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

**Class B** — Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 160-hour burn-in at 125°C. All other process requirements are the same.

**Class A** — Used where replacement is extremely difficult and reliability is imperative. Class A screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and tighter sampling inspection.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to Class C. Electrical burn-in upgrades any product to a full Class B screened part on a short delivery cycle.

All molded integrated circuits receive Class C screening except that centrifuge and hermeticity steps are omitted for solid-package parts.

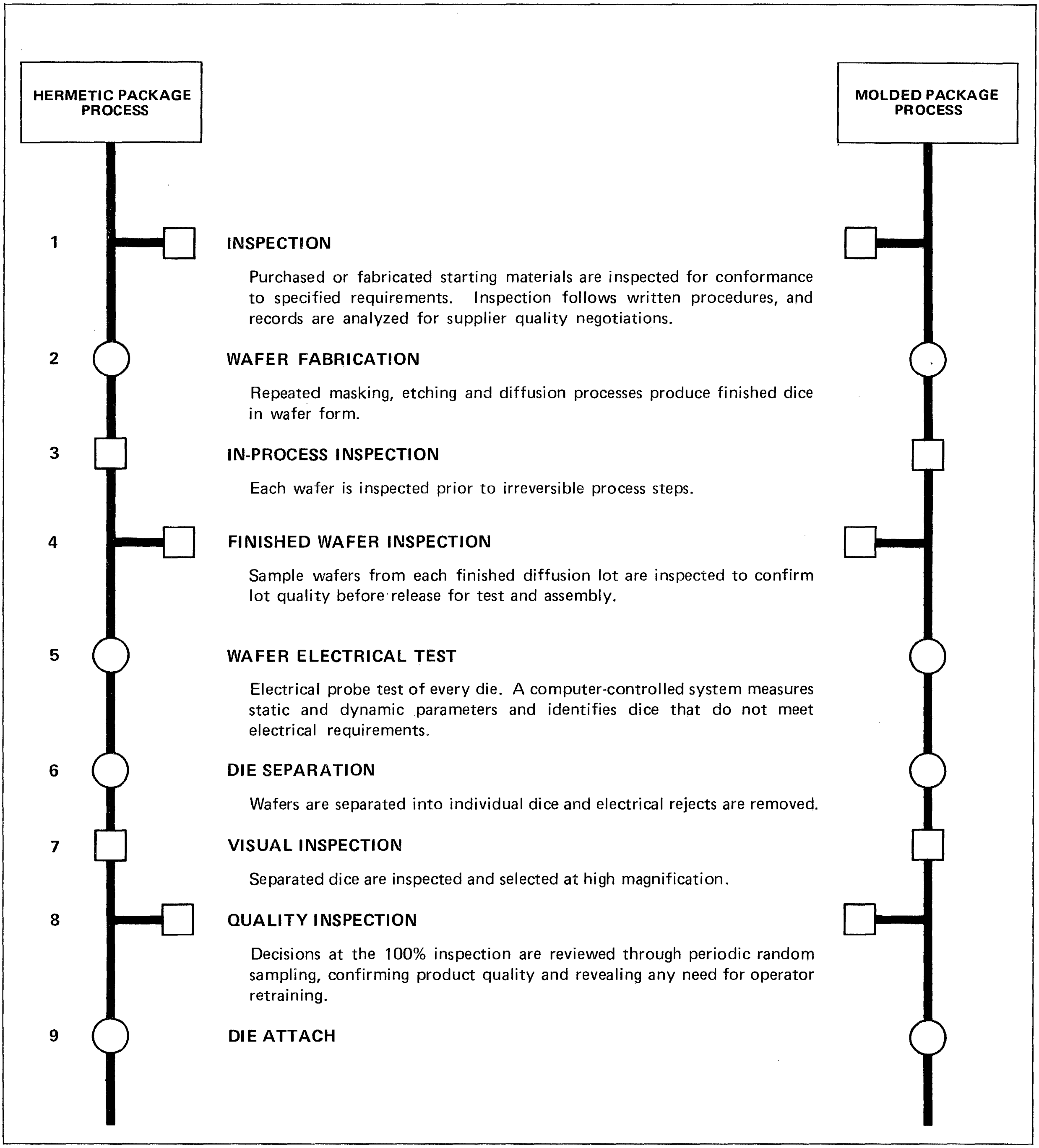
**Test Method 5005** defines qualification and quality conformance procedures. Subgroups, tests and quality levels for each class are given for Group A (electrical), Group B (mechanical quality measurements related to the user's assembly environment), and Group C (long-term reliability and product design stress tests). Group A tests are always performed; Group B and C may be specified by the user. Tables I, II, and III give standard test groupings and quality levels for Class B screened devices. These quality levels are used as a minimum for all tests.

# MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004, Class C; quality conformance inspection where required is performed to Class B levels.

All full-temperature-range (–55°C to +125°C) linear, MSI and computer-interface circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.



**HERMETIC PACKAGE PROCESS**

**MOLDED PACKAGE PROCESS**

### 1 INSPECTION

Purchased or fabricated starting materials are inspected for conformance to specified requirements. Inspection follows written procedures, and records are analyzed for supplier quality negotiations.

### 2 WAFER FABRICATION

Repeated masking, etching and diffusion processes produce finished dice in wafer form.

### 3 IN-PROCESS INSPECTION

Each wafer is inspected prior to irreversible process steps.

### 4 FINISHED WAFER INSPECTION

Sample wafers from each finished diffusion lot are inspected to confirm lot quality before release for test and assembly.

### 5 WAFER ELECTRICAL TEST

Electrical probe test of every die. A computer-controlled system measures static and dynamic parameters and identifies dice that do not meet electrical requirements.

### 6 DIE SEPARATION

Wafers are separated into individual dice and electrical rejects are removed.

### 7 VISUAL INSPECTION

Separated dice are inspected and selected at high magnification.

### 8 QUALITY INSPECTION

Decisions at the 100% inspection are reviewed through periodic random sampling, confirming product quality and revealing any need for operator retraining.

### 9 DIE ATTACH

### 10 QUALITY INSPECTION

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

### 11 WIRE BOND

Hermetic: Aluminum wires, ultrasonic bonding.
Molded: Gold wires, thermocompression bonding.

### 12 QUALITY INSPECTION

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

### 13 INTERNAL VISUAL INSPECTION

Assembled but unsealed units are individually inspected at low and high power.

**QUALITY STANDARDS:**

All devices—MIL-STD-883, Method 2010, Condition B.
Full temperature devices identified above—MIL-M-38510,
Para. 3.7 for workmanship.

### 14 QUALITY INSPECTION

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

### 15a FINAL SEAL

(Hermetic devices)

### 15b ENCAPSULATE

(Molded Devices)

### 16 STABILIZATION BAKE

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

### 17 TEMPERATURE CYCLE

MIL-STD-883, Method 1010, Cond. C: –65°C, +150°C, 10 cycles

### 18 CENTRIFUGE

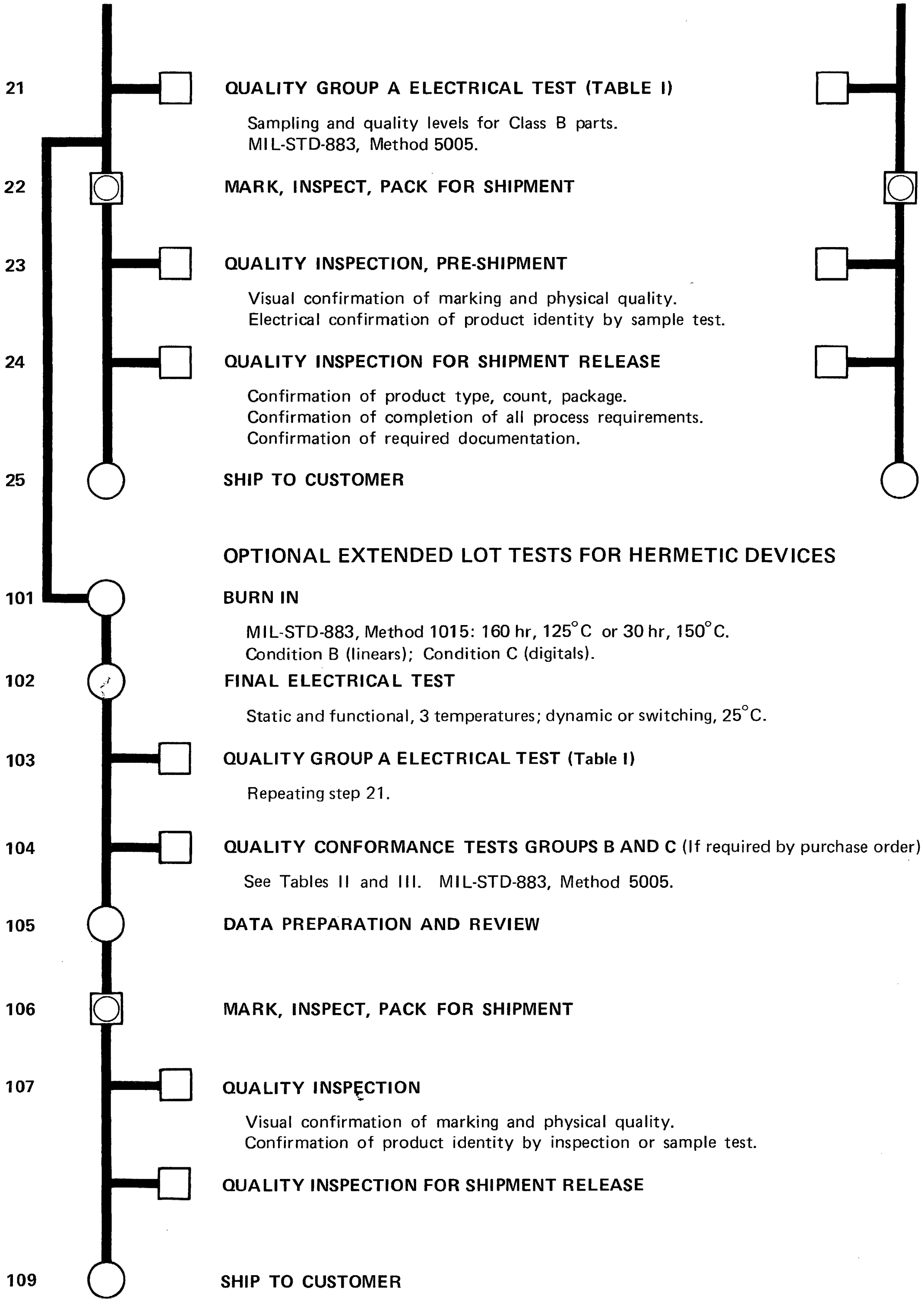
MIL-STD-883, Method 2001, Cond. E: 30,000 G

### 19 SEAL (HERMETICITY) TEST

MIL-STD-883, Method 1014, Cond. A or B: Fine Leak
MIL-STD-883, Method 1014, Cond. C2: Gross Leak

### 20 ELECTRICAL TEST

MIL-STD-883, Method 5004, Para. 3.1.12: Static, dynamic, functional tests at 25°C.



21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

Sampling and quality levels for Class B parts.
MIL-STD-883, Method 5005.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Visual confirmation of marking and physical quality.
Electrical confirmation of product identity by sample test.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER**

## OPTIONAL EXTENDED LOT TESTS FOR HERMETIC DEVICES

101 **BURN IN**

MIL-STD-883, Method 1015: 160 hr, 125°C or 30 hr, 150°C.
Condition B (linears); Condition C (digitals).

102 **FINAL ELECTRICAL TEST**

Static and functional, 3 temperatures; dynamic or switching, 25°C.

103 **QUALITY GROUP A ELECTRICAL TEST (Table I)**

Repeating step 21.

104 **QUALITY CONFORMANCE TESTS GROUPS B AND C** (If required by purchase order)

See Tables II and III. MIL-STD-883, Method 5005.

105 **DATA PREPARATION AND REVIEW**

106 **MARK, INSPECT, PACK FOR SHIPMENT**

107 **QUALITY INSPECTION**

Visual confirmation of marking and physical quality.
Confirmation of product identity by inspection or sample test.

**QUALITY INSPECTION FOR SHIPMENT RELEASE**

109 **SHIP TO CUSTOMER**

## QUALIFICATION AND QUALITY CONFORMANCE INSPECTION

Subgroups and LTPD levels as given in MIL-STD-883A, Method 5005.2, for Class B parts. We will revise these tests accordingly whenever MIL-STD-883 is revised. The latest revision of each test method is used.

**Table I. Group A Electrical Tests**

| Subgroups | LTPD | Initial Sample Size* |
|---|---|---|
| **Subgroup 1** – Static tests at 25°C | 5 | 45 |
| **Subgroup 2** – Static tests at maximum rated operating temperature | 7 | 32 |
| **Subgroup 3** – Static tests at minimum rated operating temperature | 7 | 32 |
| **Subgroup 4** – Dynamic tests at 25°C | 5 | 45 |
| **Subgroup 5** – Dynamic tests at maximum rated operating temperature | 7 | 32 |
| **Subgroup 6** – Dynamic tests at minimum rated operating temperature | 7 | 32 |
| **Subgroup 7** – Functional tests at 25°C | 5 | 45 |
| **Subgroup 8** – Functional tests at maximum and minimum rated operating temperatures | 10 | 22 |
| **Subgroup 9** – Switching tests at 25°C | 7 | 32 |

* See footnote following Table III.

**Table II. Group B Tests**

| Test | Method | Conditions | LTPD | Initial Sample Size* |
|---|---|---|---|---|
| **Subgroup 1**<br>Physical dimensions | 2016 | AMD standard dimensions unless listed by customer | 15 | |
| **Subgroup 2**<br>a) Resistance to Solvents | 2015 | Alcohol, mineral spirits, trichloroethane, and Freon solvents | 3 devices | 3 |
| b) Internal visual and mechanical | 2014 | | 1 device | 1 |
| c) Bond strength | 2011 | Test Condition D. | 15 | 15<br>leads |
| **Subgroup 3**<br>Solderability | 2003 | Solder temperature 260°C ± 10°C | 15 | 15 |
| **Subgroup 4**<br>a) Lead integrity | 2004 | Test Condition B2 | 15 | |
| b) Seal | | | | |
| 1. Fine leak | 1014 | Cond A: Helium, or Cond B: Radioactive Tracer | | |
| 2. Gross leak | 1014 | Cond C, Step 2: Fluorocarbon | | |

**Table III. Group C tests**

| Test | Method | Conditions | LTPD | Initial Sample Size* |
|---|---|---|---|---|
| **Subgroup 1** | | | | |
| a) Thermal shock | 1011 | Test Condition B: liquid to liquid, 125°C to −55°C, 15 cycles | | |
| b) Temperature cycling | 1010 | Test Condition C: air to air, −65°C to +150°C, 10 cycles | 15 | 15 |
| c) Moisture resistance | 1004 | Omit initial conditioning and vibration | | |
| d) Seal (fine and gross) | 1014 | | | |
| e) Visual examination | | | | |
| f) End point electrical test | | DC room temperature parameters | | |
| **Subgroup 2** | | | | |
| a) Mechanical shock | 2002 | Test Condition B: 5 shock pulses; 6 directions; 1,500 G | | |
| b) Vibration variable frequency | 2007 | Test Condition A: 20 Hz-2 KHz; 20 G, X, Y, Z orientation | 15 | 15 |
| c) Constant acceleration (Centrifuge) | 2001 | Test Condition E: 30 KG centrifugal acceleration | | |
| d) Seal (fine and gross) | 1014 | | | |
| e) Visual examination | | | | |
| f) End point electrical test | | DC room temperature parameters | | |
| **Subgroup 3** | | | | |
| a) Salt atmosphere | 1009 | Test Condition A: 24 hr | 15 | 15 |
| b) Visual examination | | | | |
| **Subgroup 4** | | | | |
| a) High Temperature storage | 1008 | Test Condition C: 1,000 hr, 150°C | 7 | 55<br>Acc = 1* |
| b) End point electrical test | | DC room temperature parameters | | |
| **Subgroup 5** | | | | |
| a) Operating life test | 1005 | Steady state power: 1000 hr, 125°C.<br>Digital devices: Test Condition C<br>Linear devices: Test Condition B | 5 | 77<br>Acc = 1* |
| b) End point electrical test | | DC room temperature parameters | | |

*Groups A, B and C sampling plans are based on standard LTPD tables of MIL-M-38510. The smallest sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity not exceeding an acceptance number of 2.

# MOS Microprocessor Family

## NUMERICAL INDEX AND SELECTION GUIDE

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| Am9080A-1 | 8-Bit Single Chip MOS Microprocessor (320 nsec) | 2-3 |
| Am9080A-2 | 8-Bit Single Chip MOS Microprocessor (380 nsec) | 2-3 |
| Am9080A-4 | 8-Bit Single Chip MOS Microprocessor (250 nsec) | 2-3 |
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| Am8224 | Clock Generator | 2-15 |
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# Am9080A

## 8-Bit Microprocessor

### Distinctive Characteristics

- Plug-in replacements for 8080A, 8080A-1, 8080A-2
- High-speed version with 1μsec instruction cycle
- Military temperature range operation to 1.5μsec
- Ion-implanted, n-channel, silicon-gate MOS technology
- 3.2mA of output drive at 0.4V (two full TTL loads)
- 700mV of high, 400mV of low level noise immunity
- 820mW maximum power dissipation at ±5% power
- 100% reliability assurance testing to MIL-STD-883

### GENERAL DESCRIPTION

The Am9080A products are complete, general-purpose, single-chip digital processors. They are fixed instruction set, parallel, 8-bit units fabricated with Advanced N-Channel Silicon Gate MOS technology. When combined with external memory and peripheral devices, powerful microcomputer systems are formed. The Am9080A may be used to perform a wide variety of operations, ranging from complex arithmetic calculations to character handling to bit control. Several versions are available offering a range of performance options.

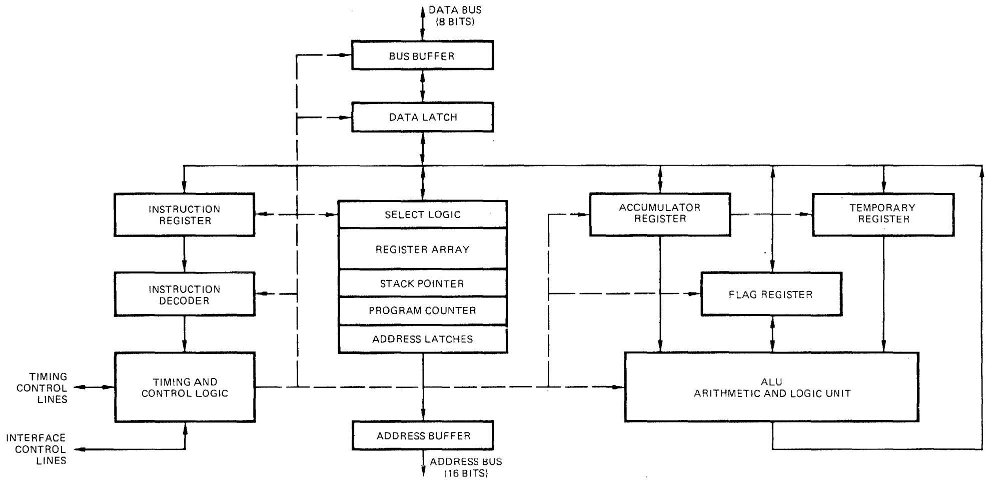
The processor has a 16-bit address bus that may be used to directly address up to 64K bytes of memory. The memory may be any combination of read/write and read-only. Data are transferred into or out of the processor on a bi-directional 8-bit data bus that is separate from the address lines. The data bus transfers instructions, data and status information between system devices. All transfers are handled using asynchronous handshaking controls so that any speed memory or I/O device are easily accommodated.

An accumulator plus six general purpose registers are available to the programmer. The six registers are each 8 bits long and may be used singly or in pairs for both 8 and 16-bit operations. The accumulator forms the primary working register and is the destination for many of the arithmetic and logic operations.

A general purpose push-down stack is an important part of the processor architecture. The contents of the stack reside in R/W memory and the control logic, including a 16-bit stack pointer, is located on the processor chip. Subroutine call and return instructions automatically use the stack to store and retrieve the contents of the program counter. Push and Pop instructions allow direct use of the stack for storing operands, passing parameters and saving the machine state.

An asynchronous vectored interrupt capability is included to allow external signals to modify the instruction stream. The interrupting device may specify an interrupt instruction to be executed and may thus vector the program to a particular service location, or perform some other direct function. Direct memory access (DMA) capability is also included.

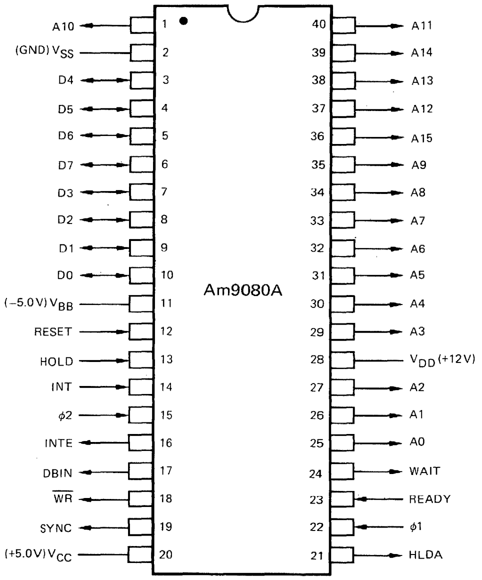
### BLOCK DIAGRAM


DATA BUS
(8 BITS)
BUS BUFFER
DATA LATCH
INSTRUCTION REGISTER
SELECT LOGIC
REGISTER ARRAY
STACK POINTER
PROGRAM COUNTER
ADDRESS LATCHES
ACCUMULATOR REGISTER
TEMPORARY REGISTER
INSTRUCTION DECODER
FLAG REGISTER
TIMING CONTROL LINES
TIMING AND CONTROL LOGIC
ALU
ARITHMETIC AND LOGIC UNIT
INTERFACE CONTROL LINES
ADDRESS BUFFER
ADDRESS BUS
(16 BITS)

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Clock Period | | | |
|---|---|---|---|---|---|
| | | 250 ns | 320 ns | 380 ns | 480 ns |
| Hermetic DIP | $0^\circ C \leq T_A \leq +70^\circ C$ | AM9080A-4DC | AM9080A-1DC<br>C8080A-1 | AM9080A-2DC<br>C8080A-2 | AM9080ADC<br>C8080A |
| | $-55^\circ C \leq T_A \leq +125^\circ C$ | | | AM9080A-2DM | AM9080ADM |
| Molded DIP | $0^\circ C \leq T_A \leq +70^\circ C$ | | AM9080A-1PC | AM9080A-2PC | AM9080APC |

## CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

## INTERFACE SIGNAL SUMMARY

| TYPE | PINS | ABBREVIATION | SIGNAL |
|---|---|---|---|
| INPUT | 1 | $V_{SS}$ | Ground |
| INPUT | 3 | $V_{DD}$, $V_{CC}$, $V_{BB}$ | +12V, +5V, −5V Supplies |
| INPUT | 2 | $\phi_1$, $\phi_2$ | Clocks |
| INPUT | 1 | RESET | Reset |
| INPUT | 1 | HOLD | Hold |
| INPUT | 1 | INT | Interrupt |
| INPUT | 1 | READY | Ready |
| IN/OUT | 8 | $D_0$–$D_7$ | Data Bus |
| OUTPUT | 16 | $A_0$–$A_{15}$ | Address |
| OUTPUT | 1 | INTE | Interrupt Enable |
| OUTPUT | 1 | DBIN | Data Bus In Control |
| OUTPUT | 1 | $\overline{\text{WR}}$ | Write Not |
| OUTPUT | 1 | SYNC | Cycle Synchronization |
| OUTPUT | 1 | HLDA | Hold Acknowledge |
| OUTPUT | 1 | WAIT | Wait |

## INTERFACE SIGNAL DESCRIPTION

**$\phi_1$, $\phi_2$** The Clock inputs provide basic timing generation for all internal operations. They are non-overlapping two phase, high level signals. All other inputs to the processor are TTL compatible.

**RESET** The Reset input initializes the processor by clearing the program counter, the instruction register, the interrupt enable flip-flop and the hold acknowledge flip-flop. The Reset signal should be active for at least three clock periods. The general registers are not cleared.

**HOLD** The Hold input allows an external signal to cause the processor to relinquish control over the address lines and the data bus. When Hold goes active, the processor completes its current operation, activates the Hlda output, and puts the 3-state address and data lines into their high-impedance state. The Holding device can then utilize the address and data busses without interference.

**READY** The Ready input synchronizes the processor with external units. When Ready is absent, indicating the external operation is not complete, the processor will enter the Wait state. It will remain in the Wait state until the clock cycle following the appearance of Ready.

**INT** The Interrupt input signal provides a mechanism for external devices to modify the instruction flow of the program in progress. Interrupt requests are handled efficiently with the vectored interrupt procedure and the general purpose stack. Interrupt processing is described in more detail on the next page.

**$D_0$-$D_7$** The Data Bus is comprised of 8 bidirectional signal lines for transferring data, instructions and status information between the processor and all external units.

**$A_0$-$A_{15}$** The Address Bus is comprised of 16 output signal lines used to address memory and peripheral devices.

**SYNC** The Sync output indicates the start of each processor cycle and the presence of processor status information on the data bus.

**DBIN** The Data Bus In output signal indicates that the bidirectional data bus is in the input mode and incoming data may be gated onto the Data Bus.

**WAIT** The Wait output indicates that the processor has entered the Wait state and is prepared to accept a Ready from the current external operation.

**$\overline{\text{WR}}$** The Write output indicates the validity of output on the data bus during a write operation.

**HLDA** The Hold Acknowledge output signal is a response to a Hold input. It indicates that processor activity has been suspended and the Address and Data Bus signals will enter their high impedance state.

**INTE** The Interrupt Enable output signal shows the status of the interrupt enable flip-flop, indicating whether or not the processor will accept interrupts.

## INSTRUCTION SET INTRODUCTION

The instructions executed by the Am9080A are variable length and may be one, two or three bytes long. The length is determined by the nature of the operation being performed and the addressing mode being used.

The instruction summary shows the number of successive memory bytes occupied by each instruction, the number of clock cycles required for the execution of the instruction, the binary coding of the first byte of each instruction, the mnemonic coding used by assemblers and a brief description of each operation. Some branch-type instructions have two execution times depending on whether the conditional branch is taken or not. Some fields in the binary code are labeled with alphabetic abbreviations. That shown as **vvv** is the address pointer used in the one-byte Call instruction (RST). Those shown as **ddd** or sss designate destination and source register fields that may be filled as follows:

| | |
|---|---|
| 111 | A register |
| 000 | B register |
| 001 | C register |
| 010 | D register |
| 011 | E register |
| 100 | H register |
| 101 | L register |
| 110 | Memory |

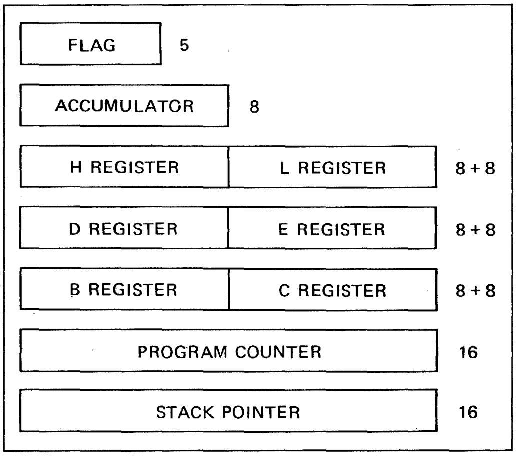
The register diagram shows the internal registers that are directly available to the programmer. The accumulator is the primary working register for the processor and is a specified or implied operand in many instructions. All I/O operations take place via the accumulator. Registers H, L, D, E, B and C may be used singly or in the indicated pairs. The H and L pair is the implied address pointer for many instructions.

The Flag register stores the program status bits used by the conditional branch instructions: carry, zero, sign and parity. The fifth flag bit is the intermediate carry bit. The flags and the accumulator can be stored on or retrieved from the stack with a single instruction. Bit positions in the flag register when pushed onto the stack (PUSH PSW) are:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| S | Z | 0 | CY1 | 0 | P | 1 | CY2 |

where S = sign, Z = zero, CY1 = intermediate carry, P = parity, CY2 = carry.

**REGISTER DIAGRAM**



During Sync time at the beginning of each instruction cycle the data bus contains operation status information that describes the machine cycle being executed. Positions for the status bits are:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MEMR | INP | M1 | OUT | HLTA | STK | $\overline{\text{WO}}$ | INTA |

### STATUS DEFINITION:

| | |
|---|---|
| **INTA** | Interrupt Acknowledge. Occurs in response to an Interrupt input and indicates that the processor will be ready for an interrupt instruction on the data bus when DBIN goes true. |
| **$\overline{\text{WO}}$** | Write or Output indicated when signal is low. When high, a Read or Input will occur. |
| **STK** | Stack indicates that the content of the stack pointer is on the address bus. |
| **HLTA** | Halt Acknowledge. |
| **OUT** | Output instruction is being executed. |
| **M1** | First instruction byte is being fetched. |
| **INP** | Input instruction is being executed. |
| **MEMR** | Memory Read operation. |

### INTERRUPT PROCESSING

When the processor interrupt mechanism is enabled (INTE=1), interrupt signals from external devices will be recognized unless the processor is in the Hold State. In handling an interrupt, the processor will complete the execution of the current instruction, disable further interrupts and respond with INTA status instead of executing the next sequential instruction in the interrupted program.

The interrupting device should supply an instruction opcode to the processor during the next DBIN time after INTA status appears.

Any opcode may be used except XTHL. If the instruction supplied is a single byte instruction, it will be executed. (The usual single byte instruction utilized is RST.) If the interrupt instruction is two or three bytes long, the next one or two processor cycles, as indicated by the DBIN signal, should be used by the external device to supply the succeeding byte(s) of the interrupt instruction. Note that INTA status from the processor is not present during these operations.

If the interrupt instruction is not some form of CALL, it is executed normally by the processor except that the Program Counter is not incremented. The next instruction in the interrupted program is then fetched and executed. Notice that the interrupt mechanism must be re-enabled by the processor before another interrupt can occur.

If the interrupt instruction is some form of CALL, it is executed normally. The Program Counter is stored and control transferred to the interrupt service subroutine. This routine has responsibility for saving and restoring the machine state and for re-enabling interrupts if desired. When the interrupt service is complete, a RETURN instruction will transfer control back to the interrupted program.

# INSTRUCTION SET SUMMARY

## DATA TRANSFER

| Op Code 76543210 | No. of Bytes | Clock Cycles | Assembly Mnemonic | Instruction Description |
|---|---|---|---|---|
| 01dddsss | 1 | 5 | MOVr, r | Move register to register |
| 01110sss | 1 | 7 | MOVm, r | Move register to memory |
| 01ddd110 | 1 | 7 | MOVr, m | Move memory to register |
| 00ddd110 | 2 | 7 | MVI, r | Move to register, immediate |
| 00110110 | 2 | 10 | MVI, m | Move to memory, immediate |
| 00111010 | 3 | 13 | LDA | Load Acc, direct |
| 00001010 | 1 | 7 | LDAX B | Load Acc, indirect via B & C |
| 00011010 | 1 | 7 | LDAX D | Load Acc, indirect via D & E |
| 00101010 | 3 | 16 | LHLD | Load H & L, direct |
| 00100001 | 3 | 10 | LXI H | Load H & L, immediate |
| 00010001 | 3 | 10 | LXI D | Load D & E, immediate |
| 00000001 | 3 | 10 | LXI B | Load B & C, immediate |
| 00110001 | 3 | 10 | LXI SP | Load stack pointer, immediate |
| 00100010 | 3 | 16 | SHLD | Store H & L, direct |
| 00110010 | 3 | 13 | STA | Store Acc, direct |
| 00000010 | 1 | 7 | STAX B | Store Acc, indirect via B & C |
| 00010010 | 1 | 7 | STAX D | Store Acc, indirect via D & E |
| 11111001 | 1 | 5 | SPHL | Transfer H & L to stack pointer |
| 11101011 | 1 | 4 | XCHG | Exchange D & E with H & L |
| 11100011 | 1 | 18 | XTHL | Exchange top of stack with H & L |
| 11011011 | 2 | 10 | IN | Input to Acc |
| 11010011 | 2 | 10 | OUT | Output from Acc |

## CONTROL

| Op Code 76543210 | No. of Bytes | Clock Cycles | Assembly Mnemonic | Instruction Description |
|---|---|---|---|---|
| 01110110 | 1 | 7 | HLT | Halt and enter wait state |
| 00110111 | 1 | 4 | STC | Set carry flag |
| 00111111 | 1 | 4 | CMC | Compliment carry flag |
| 11111011 | 1 | 4 | EI | Enable interrupts |
| 11110011 | 1 | 4 | DI | Disable interrupts |
| 00000000 | 1 | 4 | NOP | No operation |

## BRANCHING

| Op Code 76543210 | No. of Bytes | Clock Cycles | Assembly Mnemonic | Instruction Description |
|---|---|---|---|---|
| 11000011 | 3 | 10 | JMP | Jump unconditionally |
| 11011010 | 3 | 10 | JC | Jump on carry |
| 11010010 | 3 | 10 | JNC | Jump on no carry |
| 11001010 | 3 | 10 | JZ | Jump on zero |
| 11000010 | 3 | 10 | JNZ | Jump on not zero |
| 11110010 | 3 | 10 | JP | Jump on positive |
| 11111010 | 3 | 10 | JM | Jump on minus |
| 11101010 | 3 | 10 | JPE | Jump on parity even |
| 11100010 | 3 | 10 | JPO | Jump on parity odd |
| 11001101 | 3 | 17 | Call | Call unconditionally |
| 11011100 | 3 | 17-11 | CC | Call on carry |
| 11010100 | 3 | 17-11 | CNC | Call on no carry |
| 11001100 | 3 | 17-11 | CZ | Call on zero |
| 11000100 | 3 | 17-11 | CNZ | Call on not zero |
| 11110100 | 3 | 17-11 | CP | Call on positive |
| 11111100 | 3 | 17-11 | CM | Call on minus |
| 11101100 | 3 | 17-11 | CPE | Call on parity even |
| 11100100 | 3 | 17-11 | CPO | Call on parity odd |
| 11001001 | 1 | 10 | RET | Return unconditionally |
| 11011000 | 1 | 11-5 | RC | Return on carry |
| 11010000 | 1 | 11-5 | RNC | Return on no carry |
| 11001000 | 1 | 11-5 | RZ | Return on zero |
| 11000000 | 1 | 11-5 | RNZ | Return on not zero |
| 11110000 | 1 | 11-5 | RP | Return on positive |
| 11111000 | 1 | 11-5 | RM | Return on minus |
| 11101000 | 1 | 11-5 | RPE | Return on parity even |
| 11100000 | 1 | 11-5 | RPO | Return on parity odd |
| 11101001 | 1 | 5 | PCHL | Jump unconditionally, indirect via H & L |
| 11VVV111 | 1 | 11 | RST | Restart |

## ARITHMETIC

| Op Code 76543210 | No. of Bytes | Clock Cycles | Assembly Mnemonic | Instruction Description |
|---|---|---|---|---|
| 10000sss | 1 | 4 | ADDr | Add register to Acc |
| 10001sss | 1 | 4 | ADCr | Add with carry register to Acc |
| 10000110 | 1 | 7 | ADDm | Add memory to Acc |
| 10001110 | 1 | 7 | ADCm | Add with carry memory to Acc |
| 11000110 | 2 | 7 | ADI | Add to Acc, immediate |
| 11001110 | 2 | 7 | ACI | Add with carry to Acc, immediate |
| 00001001 | 1 | 10 | DAD B | Double add B & C to H & L |
| 00011001 | 1 | 10 | DAD D | Double add D & E to H & L |
| 00101001 | 1 | 10 | DAD H | Double add H & L to H & L |
| 00111001 | 1 | 10 | DAD SP | Double add stack pointer to H & L |
| 10010sss | 1 | 4 | SUBr | Subtract register from Acc |
| 10011sss | 1 | 4 | SBBr | Subtract with borrow register from Acc |
| 10010110 | 1 | 7 | SUBm | Subtract memory from Acc |
| 10011110 | 1 | 7 | SBBm | Subtract with borrow memory from Acc |
| 11010110 | 2 | 7 | SUI | Subtract from Acc, immediate |
| 11011110 | 2 | 7 | SBI | Subtract with borrow from Acc, immediate |
| 00100111 | 1 | 4 | DAA | Decimal adjust Acc |

## STACK OPERATIONS

| Op Code 76543210 | No. of Bytes | Clock Cycles | Assembly Mnemonic | Instruction Description |
|---|---|---|---|---|
| 11000101 | 1 | 11 | PUSH B | Push registers B & C on stack |
| 11010101 | 1 | 11 | PUSH D | Push registers D & E on stack |
| 11100101 | 1 | 11 | PUSH H | Push registers H & L on stack |
| 11110101 | 1 | 11 | PUSH PSW | Push Acc and flags on stack |
| 11000001 | 1 | 10 | POP B | Pop registers B & C off stack |
| 11010001 | 1 | 10 | POP D | Pop registers D & E off stack |
| 11100001 | 1 | 10 | POP H | Pop registers H & L off stack |
| 11110001 | 1 | 10 | POP PSW | Pop Acc and flags off stack |

## LOGICAL

| Op Code 76543210 | No. of Bytes | Clock Cycles | Assembly Mnemonic | Instruction Description |
|---|---|---|---|---|
| 10100sss | 1 | 4 | ANA r | And register with Acc |
| 10100110 | 1 | 7 | ANA m | And memory with Acc |
| 11100110 | 2 | 7 | ANI | And with Acc, immediate |
| 10101sss | 1 | 4 | XRA r | Exclusive or register with Acc |
| 10101110 | 1 | 7 | XRA m | Exclusive Or memory with Acc |
| 11101110 | 2 | 7 | XRI | Exclusive Or with Acc, immediate |
| 10110sss | 1 | 4 | ORA r | Inclusive Or register with Acc |
| 10110110 | 1 | 7 | ORA m | Inclusive Or memory with Acc |
| 11110110 | 2 | 7 | ORI | Inclusive Or with Acc, immediate |
| 10111sss | 1 | 4 | CMP r | Compare register with Acc |
| 10111110 | 1 | 7 | CMP m | Compare memory with Acc |
| 11111110 | 2 | 7 | CPI | Compare with Acc, immediate |
| 00101111 | 1 | 4 | CMA | Compliment Acc |
| 00000111 | 1 | 4 | RLC | Rotate Acc left |
| 00001111 | 1 | 4 | RRC | Rotate Acc right |
| 00010111 | 1 | 4 | RAL | Rotate Acc left through carry |
| 00011111 | 1 | 4 | RAR | Rotate Acc right through carry |

## INCREMENT/DECREMENT

| Op Code 76543210 | No. of Bytes | Clock Cycles | Assembly Mnemonic | Instruction Description |
|---|---|---|---|---|
| 00ddd100 | 1 | 5 | INR r | Increment register |
| 00110100 | 1 | 10 | INR m | Increment memory |
| 00000011 | 1 | 5 | INX B | Increment extended B & C |
| 00010011 | 1 | 5 | INX D | Increment extended D & E |
| 00100011 | 1 | 5 | INX H | Increment extended H & L |
| 00110011 | 1 | 5 | INX SP | Increment stack pointer |
| 00ddd101 | 1 | 5 | DCR r | Decrement register |
| 00110101 | 1 | 10 | DCR m | Decrement memory |
| 00001011 | 1 | 5 | DCX B | Decrement extended B & C |
| 00011011 | 1 | 5 | DCX D | Decrement extended D & E |
| 00101011 | 1 | 5 | DCX H | Decrement extended H & L |
| 00111011 | 1 | 5 | DCX SP | Decrement stack pointer |

## MAXIMUM RATINGS (Above which useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| All Signal Voltages With Respect to $V_{BB}$ | −0.3V to +20V |
| All Supply Voltages With Respect to $V_{BB}$ | −0.3V to +20V |
| Power Dissipation | 1.5W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | $T_A$ | $V_{DD}$ | $V_{CC}$ | $V_{BB}$ | $V_{SS}$ |
|---|---|---|---|---|---|
| Am9080A-XDC<br>C8080A-X | 0°C to +70°C | +12V ±5% | +5.0V ±5% | −5.0V ±5% | 0V |
| Am9080A-XDM | −55°C to +125°C | +12V ±10% | +5.0V ±10% | −5.0V ±10% | 0V |

No signal or supply voltage should ever be greater than 0.3V more negative than $V_{BB}$.

## ELECTRICAL CHARACTERISTICS over operating range (note 1)

| | | | | | C8080A-X | | | Am9080A-XDC | | | Am9080A-XDM | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameters** | **Description** | **Test Conditions** | | | **Min.** | **Typ.** | **Max.** | **Min.** | **Typ.** | **Max.** | **Min.** | **Typ.** | **Max.** | **Units** |
| $V_{IL}$ | Input LOW Voltage | | | | −1.0 | | 0.8 | −1.0 | | 0.8 | −1.0 | | 0.8 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | | **3.3** | | $V_{CC}+1$ | **3.0** | | $V_{CC}+1$ | **3.0** | | $V_{CC}+1$ | Volts |
| $V_{ILC}$ | Input LOW Voltage, Clock | | | | −1.0 | | 0.8 | −1.0 | | 0.8 | −1.0 | | 0.8 | Volts |
| $V_{IHC}$ | Input HIGH Voltage, Clock | | | | 9.0 | | $V_{DD}+1$ | 9.0 | | $V_{DD}+1$ | $V_{DD}-2$ | | $V_{DD}+1$ | Volts |
| | | | Am9080A-4 | | | | | $V_{DD}-2$ | | $V_{DD}+1$ | | | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = **3.2mA** | | | | | | | | **0.40** | | | **0.40** | Volts |
| | | $I_{OL}$ = **1.9mA** | | | | | **0.45** | | | | | | | Volts |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | | | | | | 3.7 | | | 3.7 | | | Volts |
| | | $I_{OH} = -100\mu A$ | | | 3.7 | | | | | | | | | |
| $I_{DD}(AV)$ | $V_{DD}$ Supply Current, Average | Operating, Minimum Clock Period | Am9080A<br>Am9080A-2<br>Am9080A-1 | $T_A = +25°C$ | | 40 | | | 30 | 45 | | 30 | 50 | mA |
| | | | | $T_A = 0°C$ | | | **70** | | 35 | **50** | | 35 | **55** | |
| | | | | $T_A = -55°C$ | | | | | | | | 45 | 70 | |
| | | | Am9080A-4 | $T_A = +25°C$ | | | | | 45 | 60 | | | | |
| | | | | $T_A = 0°C$ | | | | | 55 | 70 | | | | |
| $I_{CC}(AV)$ | $V_{CC}$ Supply Current, Average | Operating, Minimum Clock Period | Am9080A<br>Am9080A-2<br>Am9080A-1 | $T_A = +25°C$ | | 60 | | | 25 | 30 | | 15 | 35 | mA |
| | | | | $T_A = 0°C$ | | | **80** | | 20 | **35** | | 20 | **40** | |
| | | | | $T_A = -55°C$ | | | | | | | | 25 | 50 | |
| | | | Am9080A-4 | $T_A = +25°C$ | | | | | 35 | 50 | | | | |
| | | | | $T_A = 0°C$ | | | | | 40 | 60 | | | | |
| $I_{BB}(AV)$ | $V_{BB}$ Supply Current, Average | Operating, Minimum Clock Period | | | | | 1.0 | | | 1.0 | | | 1.0 | mA |
| $I_{IL}$ | Input Leakage Current | (Note 4) | | | | | ±10 | | | ±10 | | | ±10 | μA |
| $I_{CL}$ | Clock Leakage Current | $V_{SS} \leq V_\phi \leq V_{DD}$ | | | | | ±10 | | | ±10 | | | ±10 | μA |
| $I_{DL}$ | Data Bus Current, Input Mode (Note 2) | $V_{IN} \leq V_{SS} + 0.8V$ | | | | | −100 | | | −100 | | | −100 | μA |
| | | $V_{IN} \geq V_{SS} + 0.8V$ | | | | | −2.0 | | | −2.0 | | | −2.0 | mA |
| $I_{FL}$ | Address and Data Bus Leakage in OFF State | $V_{A/D} = V_{CC}$ | | | | | 10 | | | 10 | | | 10 | μA |
| | | $V_{A/D} = V_{SS}$ | | | | | −100 | | | −100 | | | −100 | μA |

## CAPACITANCE

f = 1.0MHz, Inputs = 0V, $T_A$ = 25°C

$V_{DD} = V_{CC} = V_{SS} = 0V$, $V_{BB} = -5.0V$

| Parameters | Description | Typ. | Max. | Units |
|---|---|---|---|---|
| $C_\phi$ | Clock Input Capacitance | 12 | 20 | pF |
| $C_I$ | Input Capacitance | 4.0 | 8.0 | pF |
| $C_O$ | Output Capacitance | 8.0 | 15 | pF |
| $C_{I/O}$ | I/O Capacitance | 10 | 18 | pF |

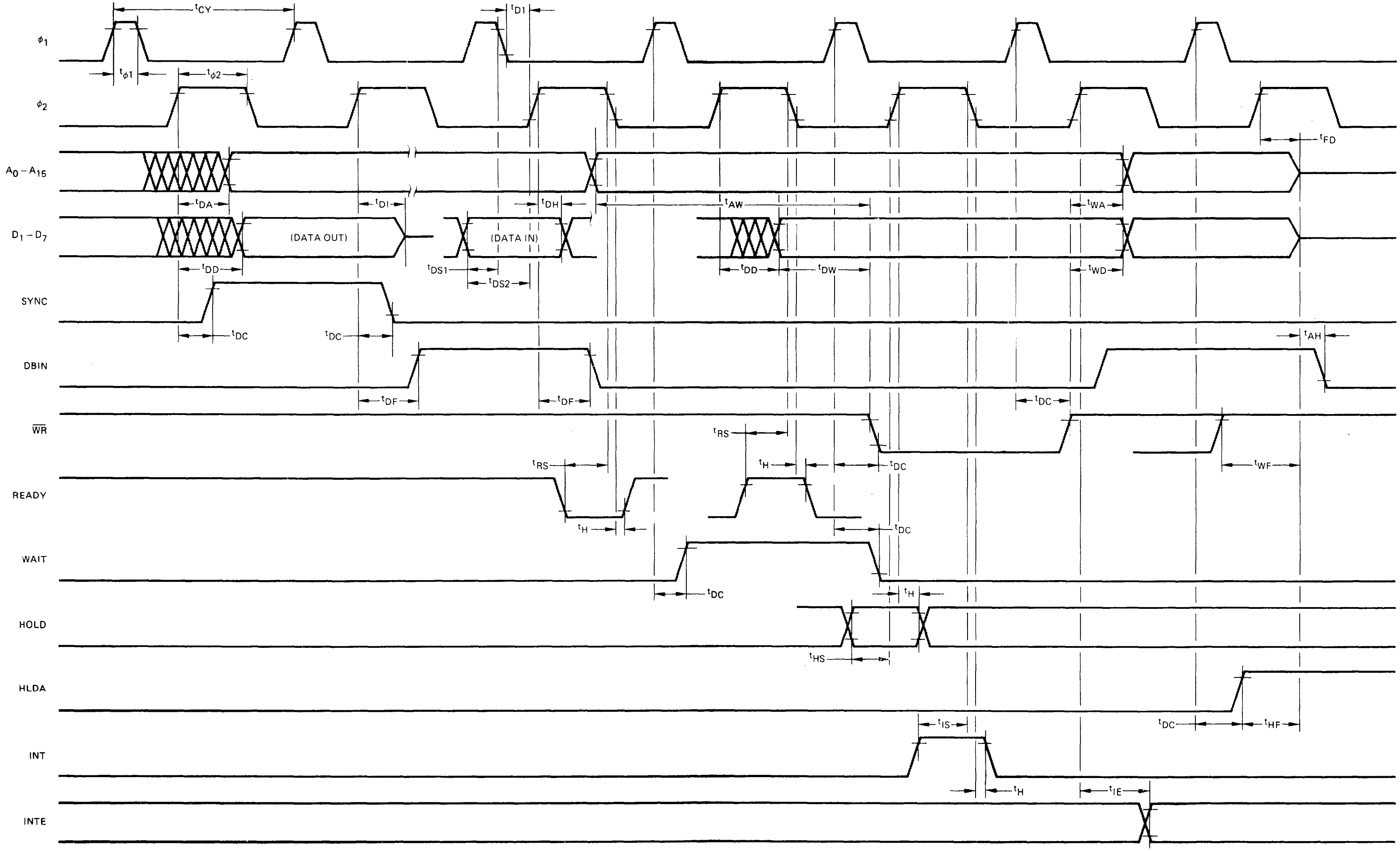
## SWITCHING CHARACTERISTICS over operating range

**Boldface numbers are 8080A specs which are exceeded.**

| Parameters | Description | Test Conditions | Am9080A-4 | | Am9080A-1<br>C8080A-1 | | Am9080A-2<br>C8080A-2 | | Am9080A<br>C8080A | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DA}$ | Clock $\phi$2 to Address Out Delay | Load Capacitance = 100pF | | **125** | | 150 | | 175 | | 200 | ns |
| $t_{DD}$ | Clock $\phi$2 to Data Out Delay | | | **140** | | 180 | | 200 | | 220 | ns |
| $t_{DI}$ | Clock $\phi$2 to Data Bus Input Mode Delay | (Note 5) | | **$t_{DF}$** | | $t_{DF}$ | | $t_{DF}$ | | $t_{DF}$ | ns |
| $t_{DS1}$ | Data In to Clock $\phi$1 Set-up Time | Both $t_{DS1}$ and $t_{DS2}$ must be satisfied | **10** | | 10 | | 20 | | 30 | | ns |
| $t_{DS2}$ | Data In to Clock $\phi$2 Set-up Time | | **110** | | 120 | | 130 | | 150 | | ns |
| $t_{DC}$ | Clock to Control Output Delay | Load Capacitance = 50pF | | **100** | | 110 | | 120 | | 120 | ns |
| $t_{RS}$ | Ready to Clock $\phi$2 Set-up Time | | **80** | | 90 | | 90 | | 120 | | ns |
| $t_{H}$ | Clock $\phi$2 to Control Signal Hold Time | | **0** | | 0 | | 0 | | 0 | | ns |
| $t_{IS}$ | Interrupt to Clock $\phi$2 Set-up Time | | **90** | | 100 | | 100 | | 120 | | ns |
| $t_{HS}$ | Hold to Clock $\phi$2 Set-up Time | | **100** | | 120 | | 120 | | 140 | | ns |
| $t_{IE}$ | Clock $\phi$2 to INTE Delay | Load Capacitance = 50pF | | **100** | | 200 | | 200 | | 200 | ns |
| $t_{FD}$ | Clock $\phi$2 to Address/Data OFF Delay | | **100** | | | 120 | | 120 | | 120 | ns |
| $t_{DF}$ | Clock $\phi$2 to DBIN Delay | Load Capacitance = 50pF | **25** | **110** | 25 | 130 | 25 | 140 | 25 | 140 | ns |
| $t_{DH}$ | Clock $\phi$2 to Data In Hold Time | (Note 5) | – | – | – | – | – | – | – | – | ns |
| $t_{AW}$ | Address Valid to Write Delay | (Note 8) | – | – | – | – | – | – | – | – | ns |
| $t_{DW}$ | Output Data Valid to Wtite Delay | (Note 8) | – | – | – | – | – | – | – | – | ns |
| $t_{KA}$ | Address Valid to Write Increment | (Note 8) | | **90** | | 110 | | 130 | | 140 | ns |
| $t_{KD}$ | Output Data Valid to Write Increment | (Note 8) | | **130** | | 150 | | 170 | | 170 | ns |
| $t_{WA}$ | Write to Address Invalid Delay | (Note 8) | – | – | – | – | – | – | – | – | ns |
| $t_{WD}$ | Write to Output Data Invalid Delay | (Note 8) | – | – | – | – | – | – | – | – | ns |
| $t_{HF}$ | HLDA to Address/Data OFF Delay | (Note 9) | – | – | – | – | – | – | – | – | ns |
| $t_{WF}$ | Write to Address/Data OFF Delay | (Note 9) | – | – | – | – | – | – | – | – | ns |
| $t_{KH}$ | HLDA to Address/Data OFF Increment | (Note 9) | | **40** | | 50 | | 50 | | 50 | ns |
| $t_{AH}$ | DBIN to Address Hold Time | | **0** | | –20 | | –20 | | –20 | | ns |

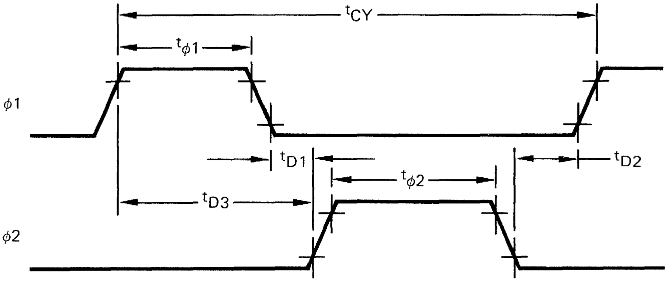
Notes:
1. Typical values are at $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Pull-up devices are connected to the Data Bus lines when the input signal is high during DBIN time. When switching the input from HIGH-to-LOW a transient current must be absorbed by the driving device until the input reaches a LOW level.
3. Timing reference levels –
   Clocks: HIGH = 8.0V, LOW = 1.0V
   Inputs: HIGH = 3.3V, LOW = 0.8V
   Outputs: HIGH = 2.0V, LOW = 0.8V
4. Control inputs impress currents on the driving signal during HIGH-to-LOW transitions. Values shown are for logic high or logic low levels. Peak current during transition is as much as 1.0mA.
5. Bus contention cannot occur and data hold times are adequate when DBIN is used to enable Data In. $t_{DH}$ is the smaller of 50ns or $t_{DF}$.
6. RESET should remain active for at least three clock periods.
7. With interrupts enabled, the interrupted instruction will be one with an interrupt input stable during the indicated interval of the last clock period of the preceeding instruction. Additional synchronization not necessary.
8. $t_{AW} = 2\ t_{CY} - t_{D3} - t_{r\phi2} - t_{KA}$
   $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - t_{KD}$
   For HLDA Off: $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10ns$
   For HLDA On: $t_{WD} = t_{WA} = t_{WF}$
9. $t_{HF} = t_{D3} + t_{r\phi2} - t_{KH}$
   $t_{WF} = t_{D3} + t_{r\phi2} - 10ns$

# SWITCHING WAVEFORMS SUMMARY


φ1
φ2
A0 – A15
D1 – D7
SYNC
DBIN
WR
READY
WAIT
HOLD
HLDA
INT
INTE
tCY
tD1
tφ1
tφ2
tFD
tDA
tDI
tDH
tAW
tWA
(DATA OUT)
(DATA IN)
tDD
tDS1
tDS2
tDD
tDW
tWD
tDC
tDC
tAH
tDF
tDF
tDC
tRS
tRS
tH
tDC
tWF
tH
tDC
tDC
tH
tHS
tIS
tDC
tHF
tH
tIE

This chart presents relative timing waveform relationships and does not show actual processor operating cycles.

## CLOCK WAVEFORM DETAIL

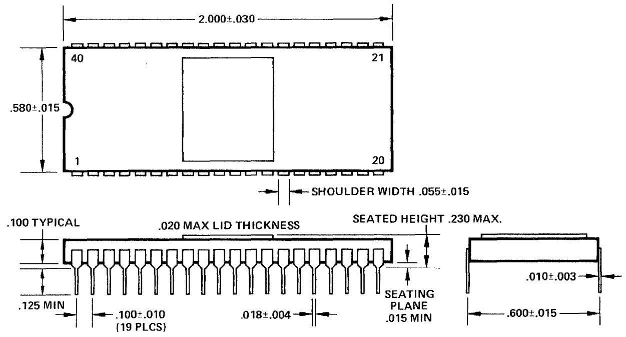

tCY
tφ1
φ1
tD1
tD2
tφ2
tD3
φ2

$$t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1}$$

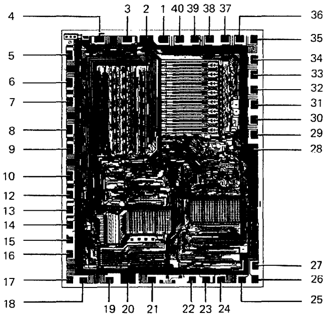
## CLOCK SWITCHING CHARACTERISTICS over operating range

| Parameters | Description | Am9080A-4 | | Am9080A-1<br>C8080A-1 | | Am9080A-2<br>C8080A-2 | | Am9080A<br>C8080A | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Clock Period | **250** | **2000** | 320 | 2000 | 380 | 2000 | 480 | 2000 | ns |
| $t_r, t_f$ | Clock Transition Times | **0** | **15** | 0 | 25 | 0 | 50 | 0 | 50 | ns |
| $t_{\phi1}$ | Clock φ1 Pulse Width | **50** | | 50 | | 60 | | 60 | | ns |
| $t_{\phi2}$ | Clock φ2 Pulse Width | **120** | | 145 | | 175 | | 220 | | ns |
| $t_{D1}$ | φ1 to φ2 Offset | **0** | | 0 | | 0 | | 0 | | ns |
| $t_{D2}$ | φ2 to φ1 Offset | **50** | | 60 | | 70 | | 70 | | ns |
| $t_{D3}$ | φ1 to φ2 Delay | **50** | | 60 | | 70 | | 80 | | ns |

## PHYSICAL DIMENSIONS
### 40-Pin Hermetic DIP


2.000±.030
40
21
.580±.015
1
20
SHOULDER WIDTH .055±.015
.100 TYPICAL
.020 MAX LID THICKNESS
SEATED HEIGHT .230 MAX.
.010±.003
SEATING PLANE
.015 MIN
.125 MIN
.100±.010
(19 PLCS)
.018±.004
.600±.015

### Metallization and Pad Layout


4
3 2 1 40 39 38 37
36
35
5
34
33
6
32
7
31
30
8
29
9
28
10
12
13
14
15
16
27
26
17
18
25
19 20 21
22 23 24

Pin 11 connection is substrate
DIE SIZE 0.131" X 0.169"

# Am25LS138

## 3-Line To 8-Line Decoder/Demultiplexer

### Distinctive Characteristics

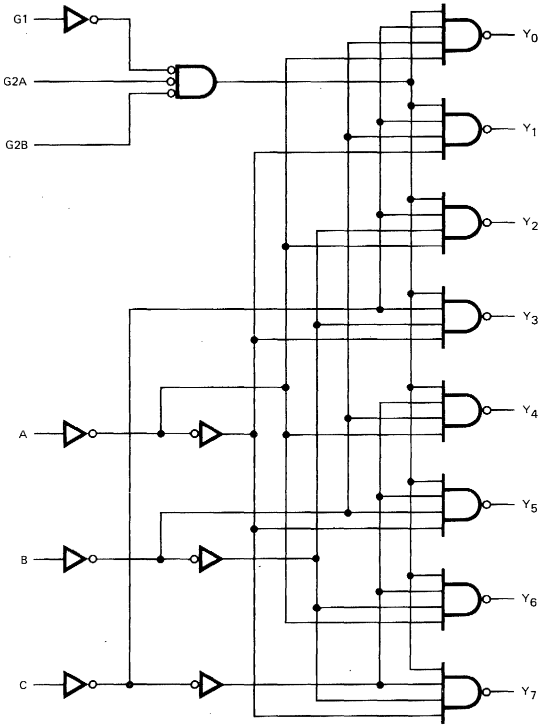
- Higher Speed compared to Am54LS/74LS
- Inverting and non-inverting enable inputs
- 8mA sink current over full military temperature range
- 50mV improved $V_{OL}$ compared to Am74LS
- 440$\mu$A source current
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am25LS138 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight Y outputs.

One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight Y outputs are HIGH regardless of the A, B and C select inputs.

### LOGIC DIAGRAM

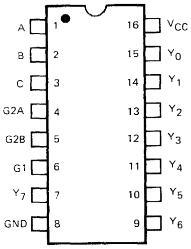


### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS138PC |
| Dice | 0°C to +70°C | AM25LS138XC |
| Hermetic DIP | −55°C to +125°C | AM25LS138DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS138FM |
| Dice | −55°C to +125°C | AM25LS138XM |

### CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

# Am25LS139

## Dual 2-Line To 4-Line Decoder/Demultiplexer

**Distinctive Characteristics**

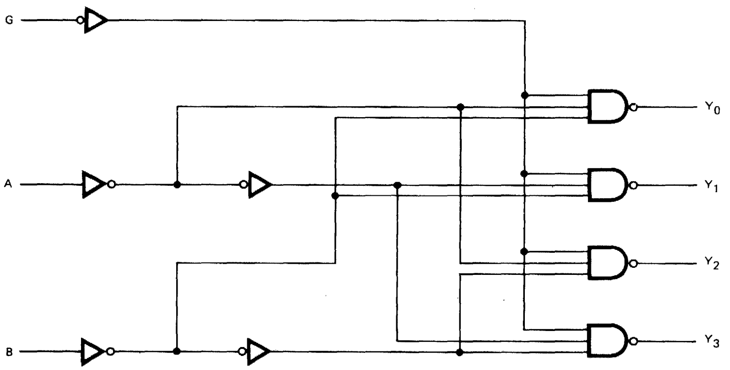
- Higher speed compared to Am54LS/74LS
- Two independent decoders/demultiplexers
- 8mA sink current over full military temperature range
- 50mV improved $V_{OL}$ compared to Am74LS
- 440$\mu$A source current
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am25LS139 is a dual 2-line to 4-line decoder/demultiplexer unit fabricated using advanced Low-Power Schottky technology. Each decoder has two buffered select inputs A and B which are decoded to one of four Y outputs.

An active LOW enable can be used for gating or can be used as a data input for demultiplexing applications. When the enable is HIGH, all four Y outputs are HIGH, regardless of the A and B inputs.

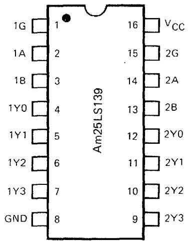
### LOGIC DIAGRAM
### (One Decoder Shown)



### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS139PC |
| Hermetic DIP | 0°C to +70°C | AM25LS139DC |
| Dice | 0°C to +70°C | AM25LS139XC |
| Hermetic DIP | –55°C to +125°C | AM25LS139DM |
| Hermetic Flat Pak | –55°C to +125°C | AM25LS139FM |
| Dice | –55°C to +125°C | AM25LS139XM |

### CONNECTION DIAGRAM
### Top View



Note: Pin 1 is marked for orientation.

# Am8212

## Eight-Bit Input/Output Port

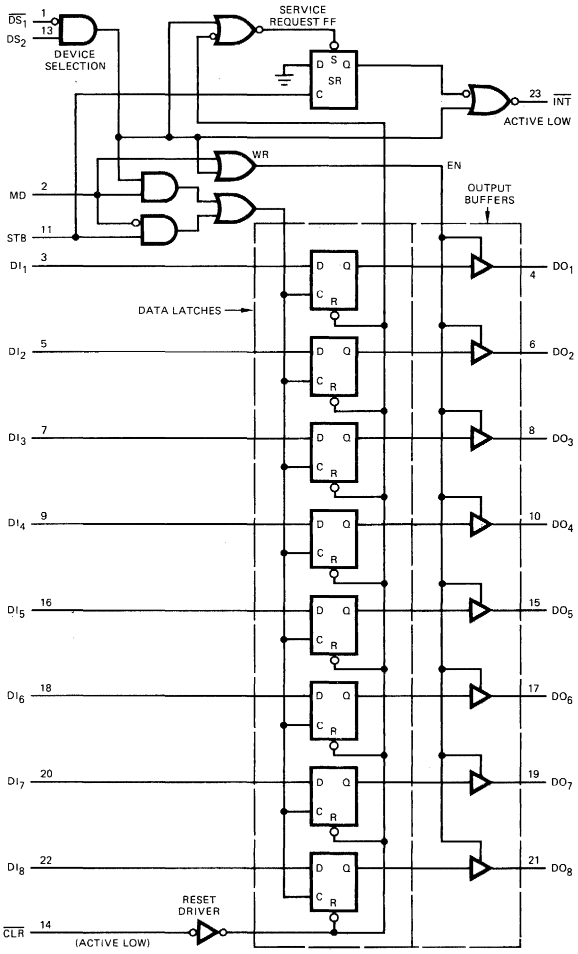
### Distinctive Characteristics

- Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.
- 4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.
- Input load current 250$\mu$A max.
- Reduces system package count
- Available for operation over both commercial and military temperature ranges.
- Advanced Schottky processing with 100% reliability assurance testing in compliance with MIL-STD-883.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

### FUNCTIONAL DESCRIPTION

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am8212. The Am8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

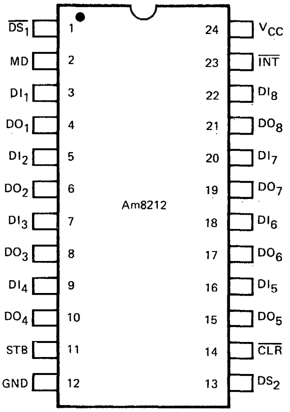
### LOGIC DIAGRAM



$\overline{DS_1}$ 1
13
$DS_2$
DEVICE SELECTION
SERVICE REQUEST FF
D S Q
SR
C
23 $\overline{INT}$
ACTIVE LOW
WR
EN
OUTPUT BUFFERS
MD 2
STB 11
$DI_1$ 3
D Q
C R
4 $DO_1$
DATA LATCHES
$DI_2$ 5
6 $DO_2$
$DI_3$ 7
8 $DO_3$
$DI_4$ 9
10 $DO_4$
$DI_5$ 16
15 $DO_5$
$DI_6$ 18
17 $DO_6$
$DI_7$ 20
19 $DO_7$
$DI_8$ 22
21 $DO_8$
RESET DRIVER
$\overline{CLR}$ 14
(ACTIVE LOW)

### CONNECTION DIAGRAM

Top View



$\overline{DS_1}$ 1
MD 2
$DI_1$ 3
$DO_1$ 4
$DI_2$ 5
$DO_2$ 6
$DI_3$ 7
$DO_3$ 8
$DI_4$ 9
$DO_4$ 10
STB 11
GND 12
24 $V_{CC}$
23 $\overline{INT}$
22 $DI_8$
21 $DO_8$
20 $DI_7$
19 $DO_7$
18 $DI_6$
17 $DO_6$
16 $DI_5$
15 $DO_5$
14 $\overline{CLR}$
13 $DS_2$
Am8212

Note: Pin 1 is marked for orientation.

### PIN DEFINITION

| | |
|---|---|
| $DI_1 - DI_8$ | DATA IN |
| $DO_1 - DO_8$ | DATA OUT |
| $\overline{DS_1} - DS_2$ | DEVICE SELECT |
| MD | MODE |
| STB | STROBE |
| $\overline{INT}$ | INTERRUPT (ACTIVE LOW) |
| $\overline{CLR}$ | CLEAR (ACTIVE LOW) |

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | –55°C to +125°C | AM8212DM |
| Hermetic DIP | 0°C to +70°C | C8212 |
| Molded DIP | 0°C to +70°C | P8212 |
| Dice | 0°C to +70°C | AM8212XC |
| Hermetic DIP | 0°C to +70°C | C3212 |
| Molded DIP | 0°C to +70°C | P3212 |

# Am8216 • Am8226

## Four-Bit Parallel Bidirectional Bus Driver

### Distinctive Characteristics

- Data bus buffer driver for 8080 type CPU's
- Low input load current – 0.25mA maximum
- High output drive capability for driving system data bus – 50mA at 0.5V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Am3216 and Am8216 have non-inverting outputs
- Output high voltage compatible with direct interface to MOS
- Three-state outputs
- Advanced Schottky processing
- Available in military and commercial temperature range
- Am3226 and Am8226 have inverting outputs

### FUNCTIONAL DESCRIPTION

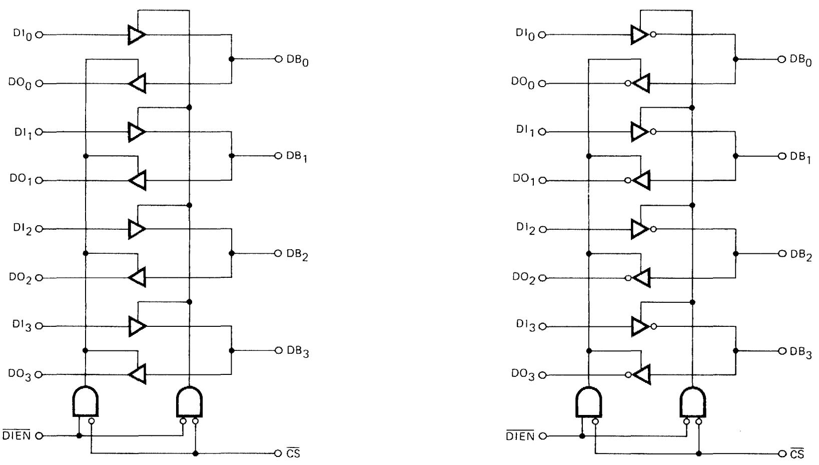
The Am3216, Am3226, Am8216 and Am8226 are four-bit, bi-directional bus drivers for use in bus oriented applications. The non-inverting Am3216 and Am8216, and inverting Am3226 and Am8226 drivers are provided for flexibility in system design.

Each buffered line of the four bit driver consists of two separate buffers that are three-state to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "LOW" the device is enabled and the direction of the data flow is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the direction of data flow which is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

### LOGIC DIAGRAMS


Am3216 • Am8216

Am3226 • Am8226

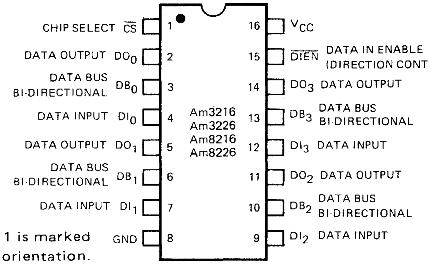
$DI_0$
$DO_0$
$DB_0$
$DI_1$
$DO_1$
$DB_1$
$DI_2$
$DO_2$
$DB_2$
$DI_3$
$DO_3$
$DB_3$
$\overline{DIEN}$
$\overline{CS}$

### ORDERING INFORMATION

| Package Type | Temperature Range | Am3216<br>Am8216<br>Order Number | Am3226<br>Am8226<br>Order Number |
|---|---|---|---|
| Hermetic DIP | –55°C to +125°C | MD3216 | MD3226 |
| Hermetic DIP | 0°C to +70°C | D3216 | D3226 |
| Molded DIP | 0°C to +70°C | P3216 | P3226 |
| Hermetic DIP | –55°C to +125°C | MD8216 | MD8226 |
| Hermetic DIP | 0°C to +70°C | D8216 | D8226 |
| Molded DIP | 0°C to +70°C | P8216 | P8226 |
| Dice | 0°C to +70°C | AM8216XC | AM8226XC |

### CONNECTION DIAGRAM

Top View


CHIP SELECT $\overline{CS}$ 1
DATA OUTPUT $DO_0$ 2
DATA BUS BI-DIRECTIONAL $DB_0$ 3
DATA INPUT $DI_0$ 4
DATA OUTPUT $DO_1$ 5
DATA BUS BI-DIRECTIONAL $DB_1$ 6
DATA INPUT $DI_1$ 7
GND 8
16 $V_{CC}$
15 $\overline{DIEN}$ DATA IN ENABLE (DIRECTION CONTROL)
14 $DO_3$ DATA OUTPUT
13 $DB_3$ DATA BUS BI-DIRECTIONAL
12 $DI_3$ DATA INPUT
11 $DO_2$ DATA OUTPUT
10 $DB_2$ DATA BUS BI-DIRECTIONAL
9 $DI_2$ DATA INPUT
Am3216
Am3226
Am8216
Am8226

Note: Pin 1 is marked for orientation.

# Am8224

## Clock Generator and Driver

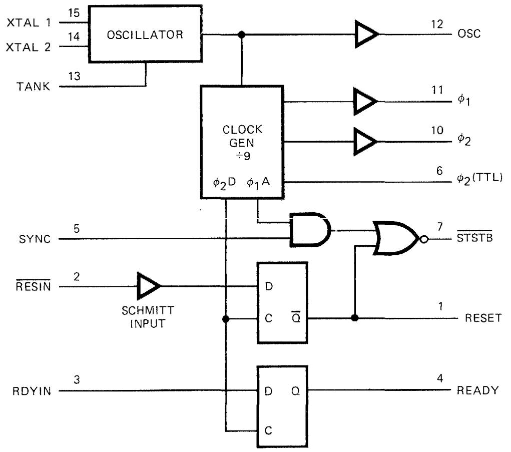
### Distinctive Characteristics

- Single chip clock generator/driver for 8080A compatible CPU
- Power-up reset for CPU
- Ready synchronizing flip-flop
- Status strobe signal
- Oscillator output for external system timing
- Available for operation over both commercial and military temperature ranges
- Crystal controlled for stable system operation
- Reduces system package count
- Advanced Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am8224 is a single chip Clock Generator/Driver for the Am9080A and 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions, including a power-up reset, status strobe and synchronization of ready. Also provided are TTL compabible oscillator and $\phi_2$ outputs for external system timing. The Am8224 provides the designer with a significant reduction of packages used to generate clocks and timing for the Am9080A or 8080A for both commercial and military temperature range applications.

### LOGIC DIAGRAM



XTAL 1
15
XTAL 2
14
OSCILLATOR
TANK
13
12
OSC
CLOCK GEN ÷9
$\phi_2$D $\phi_1$A
11
$\phi_1$
10
$\phi_2$
6
$\phi_2$(TTL)
SYNC
5
7
$\overline{\text{STSTB}}$
$\overline{\text{RESIN}}$
2
SCHMITT INPUT
D
C
$\overline{\text{Q}}$
1
RESET
RDYIN
3
D
Q
C
4
READY

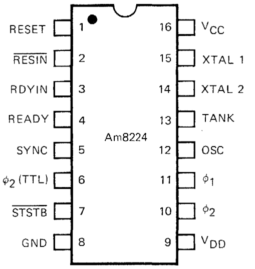
### PIN DEFINITION

| | |
|---|---|
| XTAL 1 | CONNECTIONS FOR CRYSTAL |
| XTAL 2 | |
| TANK | USED WITH OVERTONE XTAL |
| OSC | OSCILLATOR OUTPUT |
| $\phi_2$(TTL) | $\phi_2$ CLK (TTL LEVEL) |
| $V_{CC}$ | +5.0V |
| $V_{DD}$ | +12V |
| GND | 0V |
| $\overline{\text{RESIN}}$ | RESET INPUT |
| RESET | RESET OUTPUT |
| RDYIN | READY INPUT |
| READY | READY OUTPUT |
| SYNC | SYNC INPUT |
| $\overline{\text{STSTB}}$ | STATUS STB (ACTIVE LOW) |
| $\phi_1$ | Am9080A/8080A CLOCKS |
| $\phi_2$ | |

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | –55°C to +125°C | AM8224DM |
| Hermetic DIP | 0°C to +70°C | AM8224DC |
| Molded DIP | 0°C to +70°C | AM8224PC |
| Dice | 0°C to +70°C | AM8224XC |

### CONNECTION DIAGRAM
Top View



RESET 1
$\overline{\text{RESIN}}$ 2
RDYIN 3
READY 4
SYNC 5
$\phi_2$ (TTL) 6
$\overline{\text{STSTB}}$ 7
GND 8
Am8224
16 $V_{CC}$
15 XTAL 1
14 XTAL 2
13 TANK
12 OSC
11 $\phi_1$
10 $\phi_2$
9 $V_{DD}$

Note: Pin 1 is marked for orientation.

# Am8228 • Am8238

## System Controller and Bus Driver

### Distinctive Characteristics

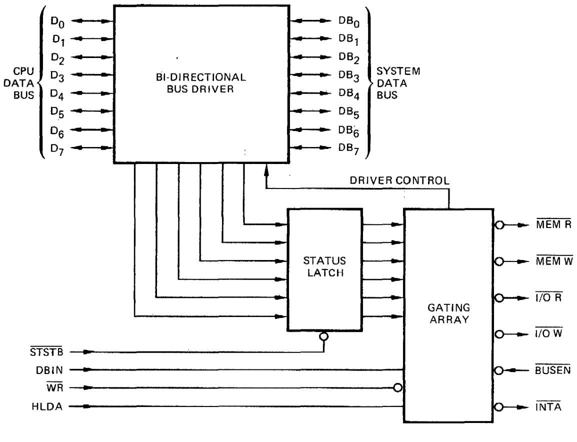
- Multi-byte instruction interrupt acknowledge
- Selectable single level vectored interrupt (RST-7)
- 28-pin molded or hermetic DIP package
- Single chip system controller and data bus driver for Am9080/8080A systems
- Bi-directional three-state bus driver for CPU independent operation
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in military and commercial temperature range
- Am8238 has extended $\overline{IOW}/\overline{MEMW}$ pulse width

### FUNCTIONAL DESCRIPTION

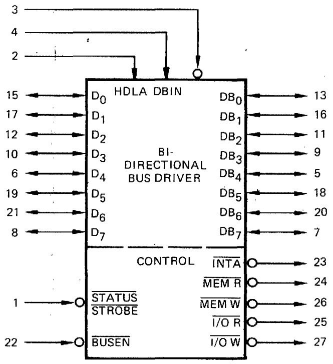
The Am8228 and Am8238 are single chip System Controller Data Bus drivers for the Am8080 Microcomputer System. They generate all control signals required to directly interface Am9080A/8080A compatible system circuits (memory and I/O) to the CPU.

Bi-directional bus drivers with three-state outputs are provided for the system data bus, facilitating CPU independent bus operations such as direct memory access. Interrupt processing is accommodated by means of a single vectored interrupt or by means of the standard 8080A single byte and multiple byte interrupt operation.

### LOGIC DIAGRAM

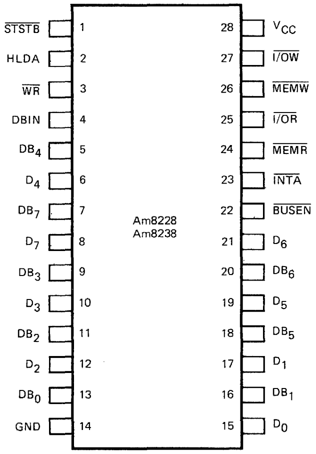

CPU DATA BUS
D0 D1 D2 D3 D4 D5 D6 D7
BI-DIRECTIONAL BUS DRIVER
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
SYSTEM DATA BUS
DRIVER CONTROL
STATUS LATCH
GATING ARRAY
MEM R
MEM W
I/O R
I/O W
BUSEN
INTA
STSTB
DBIN
WR
HLDA

### LOGIC SYMBOL


3
4
2
HLDA DBIN
BI-DIRECTIONAL BUS DRIVER
D0 15, D1 17, D2 12, D3 10, D4 6, D5 19, D6 21, D7 8
DB0 13, DB1 16, DB2 11, DB3 9, DB4 5, DB5 18, DB6 20, DB7 7
CONTROL
INTA 23
MEM R 24
MEM W 26
I/O R 25
I/O W 27
1 STATUS STROBE
22 BUSEN

$V_{CC}$ = Pin 28
GND = Pin 14

### CONNECTION DIAGRAM
Top View


STSTB 1
HLDA 2
WR 3
DBIN 4
DB4 5
D4 6
DB7 7
D7 8
DB3 9
D3 10
DB2 11
D2 12
DB0 13
GND 14
15 D0
16 DB1
17 D1
18 DB5
19 D5
20 DB6
21 D6
22 BUSEN
23 INTA
24 MEMR
25 I/OR
26 MEMW
27 I/OW
28 VCC
Am8228
Am8238

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Temperature Range | Am8228 Order Number | Am8238 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM8228PC | AM8238PC |
| Hermetic DIP | 0°C to +70°C | D8228 | D8238 |
| Hermetic DIP | –55°C to +125°C | AM8228DM | AM8238DM |
| Dice | 0°C to +70°C | AM8228XC | AM8238XC |

# Am9551

## Programmable Communication Interface

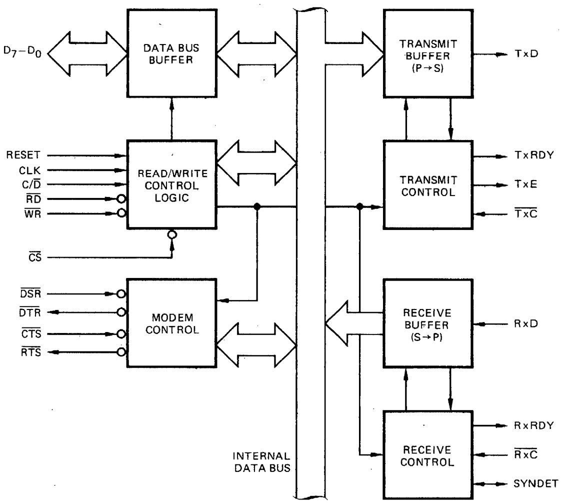
### Distinctive Characteristics

- Synchronous operation:
  - 5 to 8-bit characters
  - Internal or external character synchronization
  - Automatic sync insertion
- Asynchronous operation:
  - 5 to 8-bit characters
  - Clock rate — 1,16 or 64 times Baud rate
  - Break character generation
  - 1,1½, or 2 stop bits
  - False start bit detection
- Baud rate:
  - DC to 56k Baud (sync mode)
  - DC to 9.6k Baud (async mode)
- Full duplex, double buffered, transmitter and receiver
- Error detection:
  - Parity, overrun, and framing
- Fully compatible with Am9080A/C8080A CPU
- Single 5 volt supply
- All inputs and outputs are TTL compatible
- 100% MIL-STD-883 reliability assurance testing

### FUNCTIONAL DESCRIPTION

The Am9551 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using Advanced N-channel silicon gate MOS technology providing operation over both military and commercial temperature ranges.

### BLOCK DIAGRAM



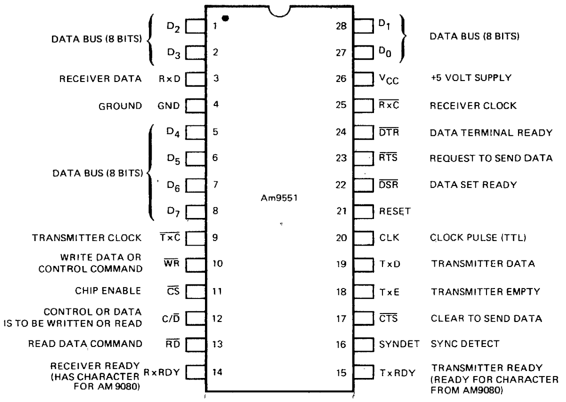
$D_7-D_0$
DATA BUS BUFFER
TRANSMIT BUFFER (P→S)
TxD
RESET
CLK
C/$\overline{D}$
$\overline{RD}$
$\overline{WR}$
READ/WRITE CONTROL LOGIC
TRANSMIT CONTROL
TxRDY
TxE
$\overline{TxC}$
$\overline{CS}$
$\overline{DSR}$
$\overline{DTR}$
$\overline{CTS}$
$\overline{RTS}$
MODEM CONTROL
RECEIVE BUFFER (S→P)
RxD
RECEIVE CONTROL
RxRDY
$\overline{RxC}$
SYNDET
INTERNAL DATA BUS

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM9551PC |
| Hermetic DIP | 0°C to +70°C | AM9551DC |
| Hermetic DIP | –55°C to +125°C | AM9551DM |

### CONNECTION DIAGRAM

**Top View**



DATA BUS (8 BITS)
$D_2$ 1
$D_3$ 2
RECEIVER DATA RxD 3
GROUND GND 4
$D_4$ 5
$D_5$ 6
DATA BUS (8 BITS)
$D_6$ 7
$D_7$ 8
TRANSMITTER CLOCK $\overline{TxC}$ 9
WRITE DATA OR CONTROL COMMAND $\overline{WR}$ 10
CHIP ENABLE $\overline{CS}$ 11
CONTROL OR DATA IS TO BE WRITTEN OR READ C/$\overline{D}$ 12
READ DATA COMMAND $\overline{RD}$ 13
RECEIVER READY (HAS CHARACTER FOR AM 9080) RxRDY 14
28 $D_1$
27 $D_0$
DATA BUS (8 BITS)
26 $V_{CC}$ +5 VOLT SUPPLY
25 $\overline{RxC}$ RECEIVER CLOCK
24 $\overline{DTR}$ DATA TERMINAL READY
23 $\overline{RTS}$ REQUEST TO SEND DATA
22 $\overline{DSR}$ DATA SET READY
21 RESET
20 CLK CLOCK PULSE (TTL)
19 TxD TRANSMITTER DATA
18 TxE TRANSMITTER EMPTY
17 $\overline{CTS}$ CLEAR TO SEND DATA
16 SYNDET SYNC DETECT
15 TxRDY TRANSMITTER READY (READY FOR CHARACTER FROM AM9080)
Am9551

Note: Pin 1 is marked for orientation.

# Am9555

## Programmable Peripheral Interface

### DISTINCTIVE CHARACTERISTICS

- Direct replacement for Intel C8255
- High speed version available
- Minimum output source current 2mA at 1.5V
- Minimum output sink current 3.2mA at 0.4V
- 24 programmable I/O pins
- Programmable modes of operation
- Bit set/reset capability
- Commercial and military temperature range operation
- Ion-implanted N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

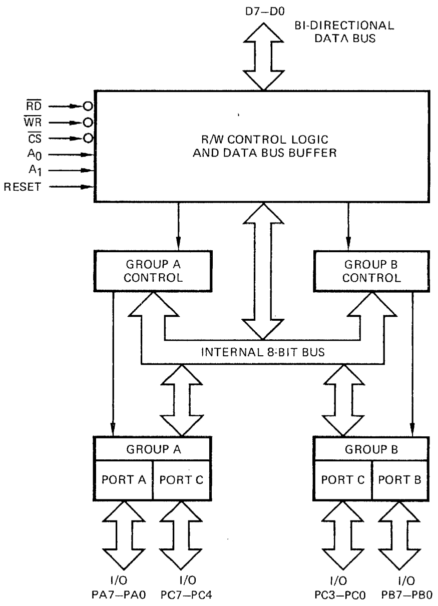
### GENERAL DESCRIPTION

The Am9555 is a high-speed programmable peripheral interface device. It can be programmed for several modes of operation allowing simplified interfacing between microprocessor and peripherals.

The 24 I/O pins are programmable to be either inputs or outputs. Outputs provide high source current on any eight of the twenty-four pins and high sink current on all pins. All signal levels are identical to TTL specifications.

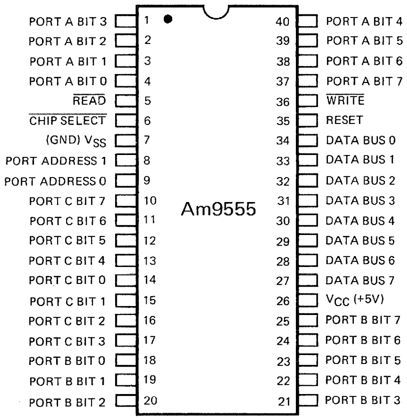
Chip Select ($\overline{CS}$) input used in conjunction with the port address A0 and A1 allows communication between processor and Am9555 ports. Data is written or read from a specific port by using the Write input, $\overline{WR}$, or Read input, $\overline{RD}$.

### BLOCK DIAGRAM


D7–D0
BI-DIRECTIONAL DATA BUS
RD
WR
CS
A0
A1
RESET
R/W CONTROL LOGIC AND DATA BUS BUFFER
GROUP A CONTROL
GROUP B CONTROL
INTERNAL 8-BIT BUS
GROUP A
PORT A
PORT C
GROUP B
PORT C
PORT B
I/O PA7–PA0
I/O PC7–PC4
I/O PC3–PC0
I/O PB7–PB0

### CONNECTION DIAGRAM

Top View


PORT A BIT 3 1
PORT A BIT 2 2
PORT A BIT 1 3
PORT A BIT 0 4
READ 5
CHIP SELECT 6
(GND) VSS 7
PORT ADDRESS 1 8
PORT ADDRESS 0 9
PORT C BIT 7 10
PORT C BIT 6 11
PORT C BIT 5 12
PORT C BIT 4 13
PORT C BIT 0 14
PORT C BIT 1 15
PORT C BIT 2 16
PORT C BIT 3 17
PORT B BIT 0 18
PORT B BIT 1 19
PORT B BIT 2 20
40 PORT A BIT 4
39 PORT A BIT 5
38 PORT A BIT 6
37 PORT A BIT 7
36 WRITE
35 RESET
34 DATA BUS 0
33 DATA BUS 1
32 DATA BUS 2
31 DATA BUS 3
30 DATA BUS 4
29 DATA BUS 5
28 DATA BUS 6
27 DATA BUS 7
26 VCC (+5V)
25 PORT B BIT 7
24 PORT B BIT 6
23 PORT B BIT 5
22 PORT B BIT 4
21 PORT B BIT 3
Am9555

Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | FOR USE WITH | | | |
|---|---|---|---|---|---|
| | | Am9080A<br>C8080A | Am9080A-2<br>C8080A-2 | Am9080A-1<br>C8080A-1 | Am9080A-4 |
| Hermetic DIP | $0^\circ C \leq T_A \leq +70^\circ C$ | Am9555DC<br>C8255 | Am9555DC | Am9555-4DC | Am9555-4DC |
| | $-55^\circ C \leq T_A \leq +125^\circ C$ | Am9555DM | Am9555DM | | |

# R/W Random Access Memories

## NUMERICAL INDEX

### Random Access Memories – RAM

| | | Page |
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| Am2101 | 256 x 4-Bit Static | 3-21 |
| Am2111 | 256 x 4-Bit Static | 3-33 |
| Am2112 | 256 x 4-Bit Static | 3-39 |
| Am9050 | 4096 x 1-Bit Dynamic | 3-9 |
| Am9060 | 4096 x 1-Bit Dynamic | 3-15 |
| Am9101 | 256 x 4-Bit Static | 3-21 |
| Am91L01 | 256 x 4-Bit Static | 3-21 |
| Am9102 | 1024 x 1-Bit Static | 3-27 |
| Am91L02 | 1024 x 1-Bit Static | 3-27 |
| Am9111 | 256 x 4-Bit Static | 3-33 |
| Am91L11 | 256 x 4-Bit Static | 3-33 |
| Am9112 | 256 x 4-Bit Static | 3-39 |
| Am91L12 | 256 x 4-Bit Static | 3-39 |
| Am9130 | 1024 x 4-Bit Static | 3-45 |
| Am9140 | 4096 x 1-Bit Static | 3-49 |

# SELECTION GUIDE

## STATIC

| Part Number | Organization | Maximum Access Time (ns) | Temp. Range | Supply Voltage | Outputs | Data I/O Configuration | Package Pins | Operating Power Max. (mW) | Standby Power Max. (mW) |
|---|---|---|---|---|---|---|---|---|---|
| Am9101A | 256 x 4 | 500 | C, M | +5 | 3-State | Separate | 22 | 290 | 46 |
| Am91L01A | 256 x 4 | 500 | C, M | +5 | 3-State | Separate | 22 | 173 | 37 |
| Am9101B | 256 x 4 | 400 | C, M | +5 | 3-State | Separate | 22 | 290 | 46 |
| Am91L01B | 256 x 4 | 400 | C, M | +5 | 3-State | Separate | 22 | 173 | 37 |
| Am9101C | 256 x 4 | 300 | C, M | +5 | 3-State | Separate | 22 | 315 | 46 |
| Am91L01C | 256 x 4 | 300 | C, M | +5 | 3-State | Separate | 22 | 189 | 37 |
| Am9101D | 256 x 4 | 250 | C | +5 | 3-State | Separate | 22 | 315 | 46 |
| Am9101E | 256 x 4 | 200 | C | +5 | 3-State | Separate | 22 | 315 | 46 |
| Am9102 | 1024 x 1 | 650 | C, M | +5 | 3-State | Separate | 16 | 263 | 42 |
| Am91L02 | 1024 x 1 | 650 | C, M | +5 | 3-State | Separate | 16 | 158 | 35 |
| Am9102A | 1024 x 1 | 500 | C, M | +5 | 3-State | Separate | 16 | 263 | 42 |
| Am91L02A | 1024 x 1 | 500 | C, M | +5 | 3-State | Separate | 16 | 158 | 35 |
| Am9102B | 1024 x 1 | 400 | C, M | +5 | 3-State | Separate | 16 | 263 | 42 |
| Am91L02B | 1024 x 1 | 400 | C, M | +5 | 3-State | Separate | 16 | 158 | 35 |
| Am9102C | 1024 x 1 | 300 | C, M | +5 | 3-State | Separate | 16 | 290 | 42 |
| Am91L02C | 1024 x 1 | 300 | C, M | +5 | 3-State | Separate | 16 | 173 | 35 |
| Am9102D | 1024 x 1 | 250 | C | +5 | 3-State | Separate | 16 | 290 | 42 |
| Am9102E | 1024 x 1 | 200 | C | +5 | 3-State | Separate | 16 | 290 | 42 |
| Am9111A | 256 x 4 | 500 | C, M | +5 | 3-State | Bussed | 18 | 290 | 46 |
| Am91L11A | 256 x 4 | 500 | C, M | +5 | 3-State | Bussed | 18 | 173 | 37 |
| Am9111B | 256 x 4 | 400 | C, M | +5 | 3-State | Bussed | 18 | 290 | 46 |
| Am91L11B | 256 x 4 | 400 | C, M | +5 | 3-State | Bussed | 18 | 173 | 37 |
| Am9111C | 256 x 4 | 300 | C, M | +5 | 3-State | Bussed | 18 | 315 | 46 |
| Am91L11C | 256 x 4 | 300 | C, M | +5 | 3-State | Bussed | 18 | 189 | 37 |
| Am9111D | 256 x 4 | 250 | C | +5 | 3-State | Bussed | 18 | 315 | 46 |
| Am9111E | 256 x 4 | 200 | C | +5 | 3-State | Bussed | 18 | 315 | 46 |
| Am9112A | 256 x 4 | 500 | C, M | +5 | 3-State | Bussed | 16 | 290 | 46 |
| Am91L12A | 256 x 4 | 500 | C, M | +5 | 3-State | Bussed | 16 | 173 | 37 |
| Am9112B | 256 x 4 | 400 | C, M | +5 | 3-State | Bussed | 16 | 290 | 46 |
| Am91L12B | 256 x 4 | 400 | C, M | +5 | 3-State | Bussed | 16 | 173 | 37 |
| Am9112C | 256 x 4 | 300 | C, M | +5 | 3-State | Bussed | 16 | 315 | 46 |
| Am91L12C | 256 x 4 | 300 | C, M | +5 | 3-State | Bussed | 16 | 189 | 37 |
| Am9112D | 256 x 4 | 250 | C | +5 | 3-State | Bussed | 16 | 315 | 46 |
| Am9112E | 256 x 4 | 200 | C | +5 | 3-State | Bussed | 16 | 315 | 46 |
| Am9130A | 1024 x 4 | 500 | C, M | +5 | 3-State | Bussed | 22 | 578 | 84 |
| Am9130B | 1024 x 4 | 400 | C, M | +5 | 3-State | Bussed | 22 | 578 | 84 |
| Am9130C | 1024 x 4 | 300 | C, M | +5 | 3-State | Bussed | 22 | 578 | 84 |
| Am9130E | 1024 x 4 | 200 | C | +5 | 3-State | Bussed | 22 | 578 | 84 |
| Am9140A | 4096 x 1 | 500 | C, M | +5 | 3-State | Separate | 22 | 578 | 84 |
| Am9140B | 4096 x 1 | 400 | C, M | +5 | 3-State | Separate | 22 | 578 | 84 |
| Am9140C | 4096 x 1 | 300 | C, M | +5 | 3-State | Separate | 22 | 578 | 84 |
| Am9140E | 4096 x 1 | 200 | C | +5 | 3-State | Separate | 22 | 578 | 84 |

## DYNAMIC

| Part Number | Organization | Access Time | Temp. Range | Supply Voltages | Operating Power (mW) | Outputs | Data I/O Configuration | Package Pins | Operating Power-Max. (mW) | Standby Power-Max. (mW) |
|---|---|---|---|---|---|---|---|---|---|---|
| Am9050C | 4096 x 1 | 300 | C | –5, +12 | 750 | Open Drain | Bussed | 18 | 750 | 3.0 |
| Am9050D | 4096 x 1 | 250 | C | –5, +12 | 750 | Open Drain | Bussed | 18 | 750 | 3.0 |
| Am9050E | 4096 x 1 | 200 | C | –5, +12 | 750 | Open Drain | Bussed | 18 | 750 | 3.0 |
| Am9060C | 4096 x 1 | 300 | C | ±5, +12 | 750 | 3-State | Separate | 22 | 750 | 3.0 |
| Am9060D | 4096 x 1 | 250 | C | ±5, +12 | 750 | 3-State | Separate | 22 | 750 | 3.0 |
| Am9060E | 4096 x 1 | 200 | C | ±5, +12 | 750 | 3-State | Separate | 22 | 750 | 3.0 |

# Am1101A/1101A1/1101A51

## 256-Bit Fully Decoded Random Access Memories

### Distinctive Characteristics

- 256-bit fully decoded silicon gate MOS static random access memories.
- Typical access time: 650 ns Am1101A1
  850 ns Am1101A
- Chip select and OR tieable outputs allow easy expansion to large memories.
- 100% reliability assurance testing in compliance with MIL STD 883.

### FUNCTIONAL DESCRIPTION

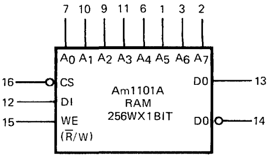
The Advanced Micro Devices' Am1101A and Am1101A1, are silicon gate MOS fully decoded random access 256-word by 1-bit memories. Low threshold silicon gate technology enables the devices to interface directly with standard DTL and TTL circuits. The memories use normally off P-channel MOS devices to form a static memory array that is ideal for use in small buffer memory applications. The Am1101A1 is a selected Am1101A for applications where higher speed is required and the Am1101ADM is a selected Am1101A which operates over the full military temperature range. The memories have an active LOW chip select input and OR tieable complementary outputs for ease of memory expansion. The chip select input can be driven by TTL MSI decoders such as the Am9301.

These memories are operated by applying DTL or TTL logic levels to the device inputs. For a read operation the chip select input, $\overline{CS}$, is held at a LOW logic level. The appropriate pattern is applied to the address inputs and the read/write input is held at a LOW logic level. The information stored in the addressed location is read out on complementary outputs, $\overline{DO}$ and DO, that can directly drive DTL or TTL circuitry. For a write operation, the chip select is held at a LOW logic level and the read/write input is moved to a HIGH logic level 300ns or more after the address has been selected and held HIGH for at least 400ns. This is to allow time for address decoding and to ensure writing data into the correct location. The data to be written into the addressed location must be present for at least 300ns before the end of the write command. During the write operation, if the chip is selected, the data outputs follow the data input line.

When the chip is unselected both the read/write and the data input leads are ineffective and both outputs go to a high impedance "OFF" state. The chip select, however, does not operate on the address decoders. This feature allows an effective increase in memory speed in some applications by using the faster delay from the chip select to the output.

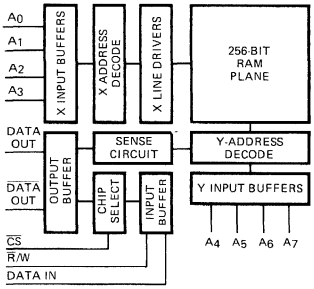
The memory can be operated in a low power standby mode by switching the periphery circuitry supply, $V_D$, to $V_{CC}$ and maintaining only the cell power supply, $V_{DD}$, supply current. When a chip is selected, the $V_D$ supply is separated from the $V_{CC}$. In this mode of operation the chip select and $V_D$ pin can be tied together, allowing full power to be dissipated only in selected chips and considerably reducing the system power in a large memory system.

### LOGIC SYMBOL



$V_{CC}$ = PIN 5
$V_{DD}$ = PIN 8
$V_D$ = PIN 4

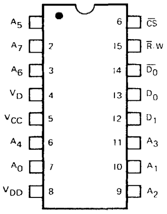
### BLOCK DIAGRAM



### Am1101A ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Access Time | |
|---|---|---|---|
| | | 1.0μs | 1.5μs |
| 0°C ≤ $T_A$ ≤ +70°C | Molded DIP | AM1101AIPC | AM1101APC |
| | Hermetic DIP | AM1101AI | AM1101A |
| −55°C ≤ $T_A$ ≤ +125°C | Molded DIP | | |
| | Hermetic DIP | | AM1101A51 |

### CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

## MAXIMUM RATINGS Above which the useful life may be impaired (Note 1)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Case) Under Bias (Note 2) | −55°C to +125°C |
| Power Dissipation at Room Temperature | 700 mW |
| All Input and Output Voltages with respect to the Most Positive Supply Voltage, $V_{CC}$ | +0.3 V to −20 V |
| Supply Voltages $V_{DD}$ and $V_D$ with respect to $V_{CC}$ | −20 V |

## OPERATING RANGE

| Device | $V_{CC}$ | $V_D$ | $V_{DD}$ | Temperature |
|---|---|---|---|---|
| 1101A, 1101A1 | +5.0 ±5% | −9.0 ±5% | −9.0 ±5% | 0°C to +75°C |
| Am1101A51 | +5.0 ±5% | −10.0 ±5% | −10.0 ±5% | −55°C to +125°C |

## ELECTRICAL CHARACTERISTICS (over operating range unless otherwise specified)

| | | Am1101A, Am1101A1 | | | Am1101A51 | | | |
|---|---|---|---|---|---|---|---|---|
| Parameters | Test Conditions | Min | Typ (Note 3) | Max | Min | Typ (Note 3) | Max | Units |
| $V_{OH}$ Output HIGH Voltage | $I_{OH} = -100\ \mu A$ | 3.5 | 4.9 | | 3.5 | 4.9 | | Volts |
| $V_{OL}$ Output LOW Voltage | $I_{OL} = -2.0$ mA | | | 0.45 | | | | Volts |
| | $I_{OL} = -1.8$ mA | | | | | | 0.45 | |
| $V_{IH}$ (Note 4) Input HIGH Voltage | | $V_{CC} -2$ | | $V_{CC} +0.3$ | $V_{CC} -1$ | | $V_{CC} +0.3$ | Volts |
| $V_{IL}$ (Note 4) Input LOW Voltage | | −10 | | $V_{CC} -4.5$ | −10 | | $V_{CC} -4.5$ | Volts |
| $I_L$ Input Load Current | $V_{IN} = 0.0$ V | | 1.0 | 500 | | 1.0 | 500 | nA |
| $I_{LO}$ Output Leakage Current | $V_{OUT} = 0.0$ V, $\overline{CS} = V_{IH}$ MIN. | | 1.0 | 500 | | 1.0 | 500 | nA |
| $I_{OL}$ Output Sink Current | $V_{OUT} = 0.45$ V | 2.0 | 8.0 | | 1.8 | 8.0 | | mA |
| | $V_{OUT} = 0.45$ V, $T_A = +25°C$ | 3.0 | | | 3.0 | | | |
| $I_{OH}$ Output Source Current | $V_{OUT} = 0.0$ V | −2.0 | −8.0 | | −1.8 | −8.0 | | mA |
| | $V_{OUT} = 0.0$ V, $T_A = +25°C$ | −3.0 | | | −3.0 | | | |
| $I_{CEF}$ Output Clamp Current | $V_{OUT} = -1.0$ V | | 6 | 13 | | 6 | 19 | mA |
| $I_{DD}$ DC Power Supply Current | $I_{OL} = 0.0$ mA, $T_A =$ MIN. | | | −20 | | | −30 | mA |
| | $I_{OL} = 0.0$ mA, $T_A = 25°C$ | | −9 | −16 | | −11 | −19 | |
| $I_D$ DC Power Supply Current | $I_{OL} = 0.0$ mA, $T_A =$ MIN. | | | −24 | | | −35 | mA |
| | $I_{OL} = 0.0$ mA, $T_A = 25°C$ | | −12 | −18 | | −14 | −21 | |
| $C_{IN}$ (Note 5) Input Capacitance | $V_{IN} = V_{CC}$, f = 1 MHz | | 7 | 10 | | 7 | 10 | pF |
| $C_{OUT}$ (Note 5) Output Capacitance | $V_{OUT} = V_{CC}$, f = 1 MHz | | 7 | 10 | | 7 | 10 | pF |
| $C_D$ (Note 5) Capacitance on $V_D$ | $V_D = V_{CC}$, f = 1 MHz | | 20 | 35 | | 20 | 35 | pF |

**Note 1:** Stresses above those listed in "MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation at these or at any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** The thermal resistance $\theta_{CA}$ Case to Ambient is to a large extent dependent on ambient conditions such as velocity of air and the positions of packages and mounting boards relative to one another.

**Note 3:** Typical values are at normal voltage and $T_A = +25°C$.

**Note 4:** A TTL device driving the memory must have its output HIGH $\geq V_{IH}$ min and its output LOW $< V_{IL}$ max even when driving other circuitry.

**Note 5:** This parameter is periodically sampled and not 100% tested.

## SWITCHING CHARACTERISTICS (Over operating range unless otherwise noted)

(Output load is 1 TTL gate and 20 pF)

| Parameters | Description | | Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{pd}$(A) | Access Time, Address to Output HIGH or LOW | Am1101A | $\overline{CS}$ = L<br>See Fig. 1 | 0.05 | 0.85 | 1.5 | μs |
| | | Am1101A1 | | 0.05 | 0.65 | 1.0 | μs |
| $t_{pd\ on}$($\overline{CS}$) | Delay, Chip Select to Output Active | | Fig. 1 | 0.05 | 0.2 | 0.3 | μs |
| $t_{pd\ off}$($\overline{CS}$) | Delay, Chip Select to Output HIGH Impedance State | | Fig. 1 | 0.05 | 0.1 | 0.3 | μs |
| $t_{pw}$($\overline{CS}$) | Minimum Chip Select Pulse Width (Note 2) | | Fig. 2 | | | 0.4 | μs |
| $t_{pw}$(W) | Minimum Write Pulse Width (Note 2) | | Fig. 2 | | | 0.4 | μs |
| $t_s$(A) | Address Set-Up Time | | Fig. 2 | | | 0.3 | μs |
| $t_h$(A) | Address Hold Time | | Fig. 2 | | | 0.1 | μs |
| $t_s$(D) | Data Set-Up Time | | Fig. 2 | | | 0.3 | μs |
| $t_h$(D) | Data Hold Time | | Fig. 2 | | | 0.1 | μs |
| $T_R$ | System Read Cycle (defined by $t_{pd}$ (A) | Am1101A | Fig. 1 | 1.5 | | | μs |
| | | Am1101A1 | | 1.0 | | | |
| $T_W$ | System Write Cycle (defined by $t_s$ max + $t_{pw}$ max + $t_h$ max | | | 0.8 | | | μs |

**Note 1:** Typical speeds are at 25°C ambient.

**Note 2:** To write, $\overline{CS}$ and W must both be active for at least 400 ns; either signal can be used as a 400 ns "write pulse" if the other one is active during the writing period.

## SWITCHING WAVEFORMS

**CONDITIONS OF TEST:**

Input pulse amplitudes: 0 to 5V, Input pulse rise and fall time: 10 nsec. Speed measurements referenced to 1.5 V levels (unless otherwise noted). Output load is 1 TTL gate and $C_L$ = 20 pF; measurements made at output of TTL gate ($t_{PD} \leq$ 10 nsec).

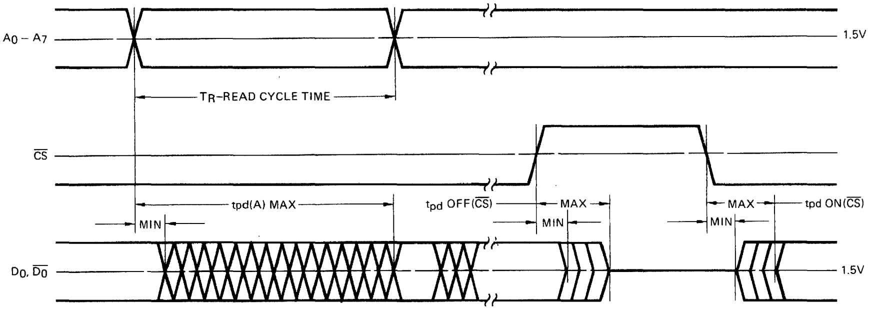


Fig. 1 READ CYCLE, showing access times for address and for chip select to and from the high impedance state.

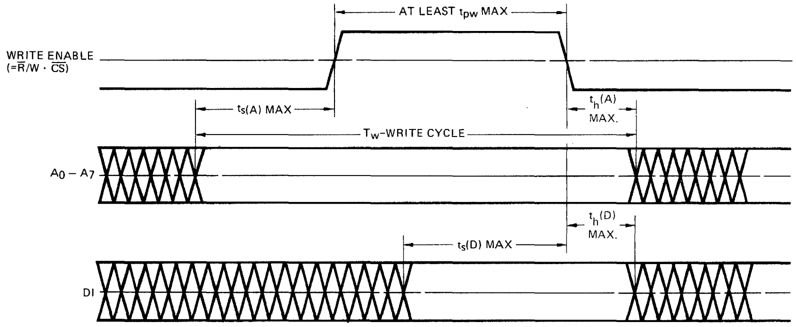
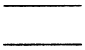
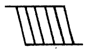
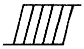
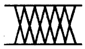
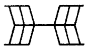


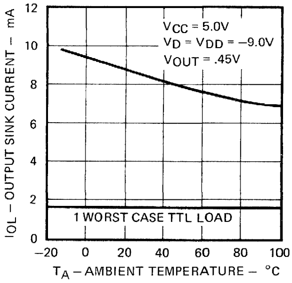
Fig. 2 WRITE CYCLE, showing required set-up times for address and data. The chip select and the write line are active. The data outputs will follow the data input during the write operation.

**KEY TO TIMING DIAGRAM**

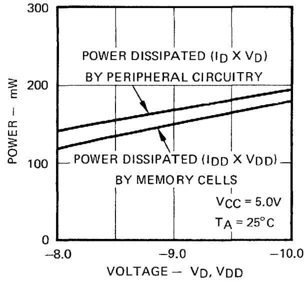
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | MUST BE STEADY | WILL BE STEADY |
|  | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
|  | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
|  | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN |
|  | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

## TYPICAL CHARACTERISTICS

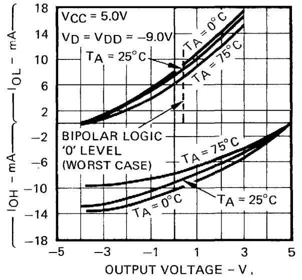
### Output Sink Current Versus Temperature



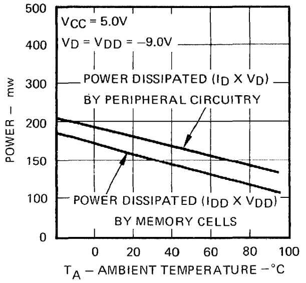
### Power Dissipation Versus Voltage



### Output Current Versus Output Voltage

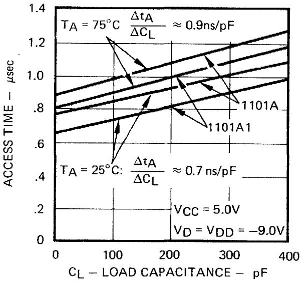


### Power Dissipation Versus Ambient Temperature

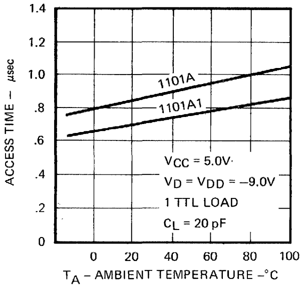


## SWITCHING CHARACTERISTICS

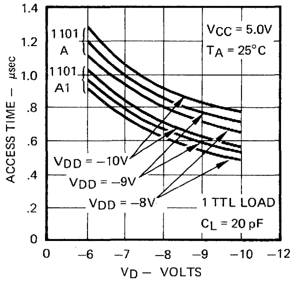
### Access Time Versus Load Capacitance



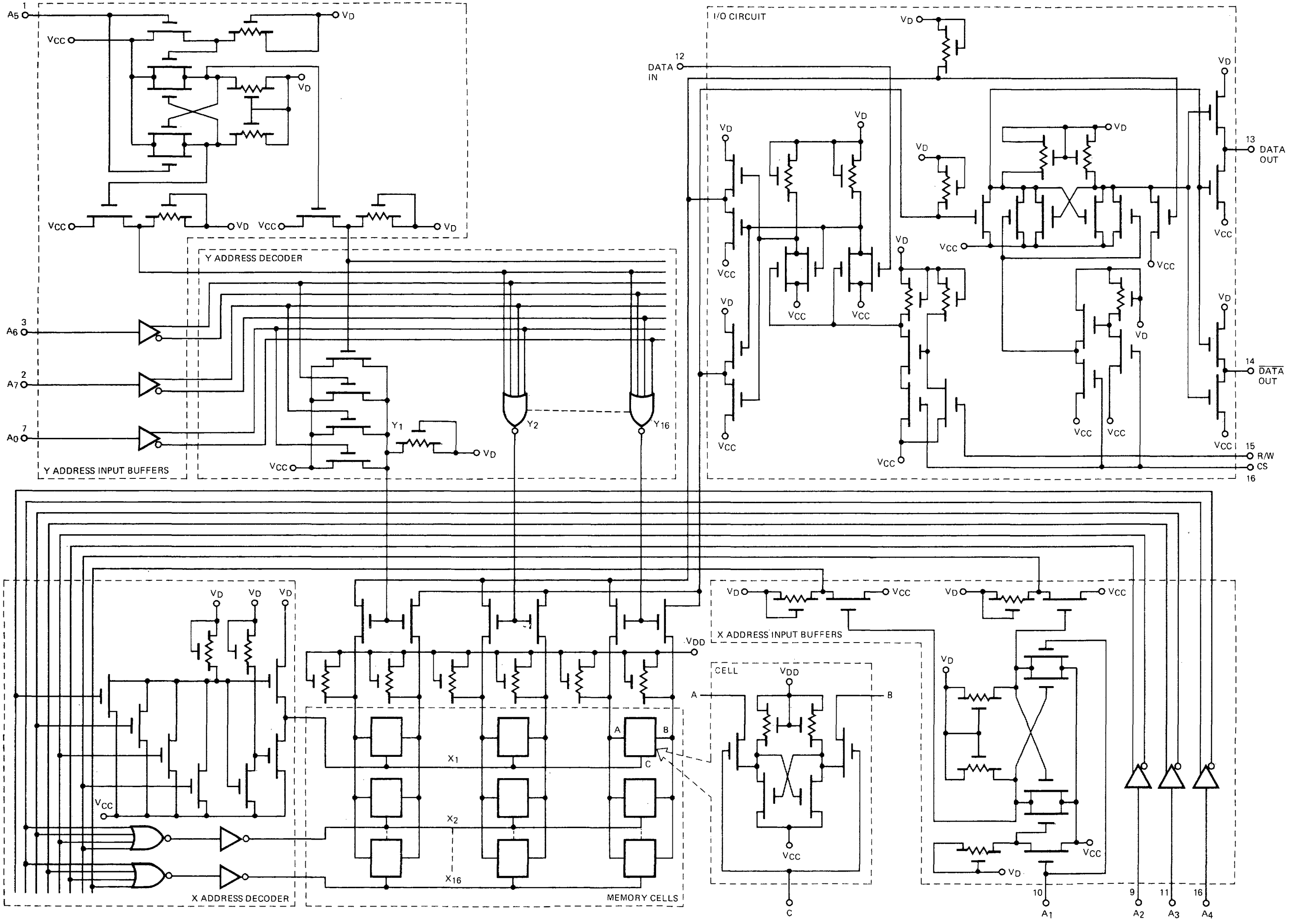
### Access Time Versus Ambient Temperature



### Access Time Versus Supply Voltage

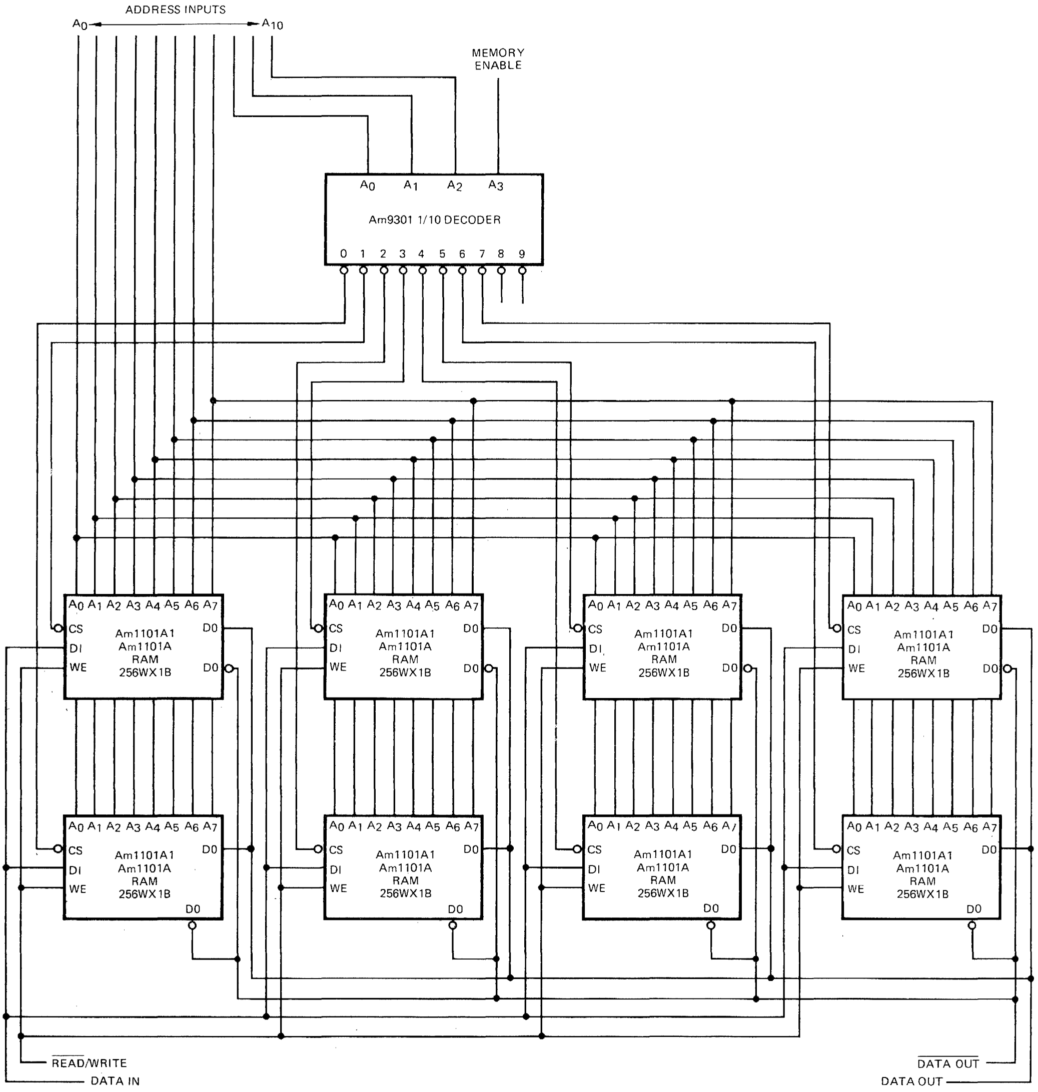


## CIRCUIT DIAGRAM


1
A5
VD
VCC
VD
VCC
VD
VCC
VD
Y ADDRESS DECODER
3
A6
2
A7
7
A0
Y ADDRESS INPUT BUFFERS
VCC
Y1
VD
Y2
Y16
I/O CIRCUIT
VD
12
DATA IN
VD
VD
VD
VD
VCC
VCC
VCC
VD
VD
VCC
VD
VCC
VCC
VD
VD
VCC
13
DATA OUT
VCC
VD
VCC
VCC
14
DATA OUT
VCC
15
R/W
CS
16
VCC
VD
VD
VD
VDD
VCC
X ADDRESS DECODER
A
B
C
X1
X2
X16
MEMORY CELLS
VD
VCC
VD
VCC
X ADDRESS INPUT BUFFERS
CELL
VDD
A
B
VCC
C
VD
VCC
VD
10
A1
9
A2
11
A3
16
A4

## APPLICATION

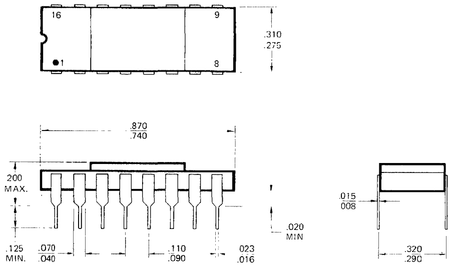
### 2048 Word x 1 Bit Memory


ADDRESS INPUTS
A0
A10
MEMORY ENABLE
A0 A1 A2 A3
Am9301 1/10 DECODER
0 1 2 3 4 5 6 7 8 9
A0 A1 A2 A3 A4 A5 A6 A7
CS
DI
WE
DO
Am1101A1
Am1101A
RAM
256WX1B
$\overline{\text{READ}}$/WRITE
DATA IN
$\overline{\text{DATA OUT}}$
DATA OUT

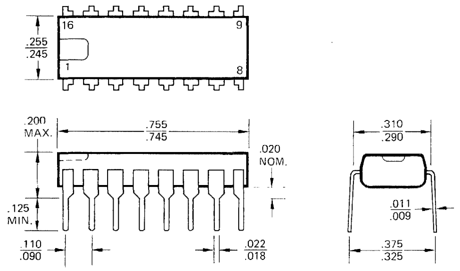
## PHYSICAL DIMENSIONS

### Dual-In-Line

### 16-Pin Side Brazed


16
9
1
8
.310
.275
.870
.740
.200
MAX.
.020
MIN
.125
MIN.
.070
.040
.110
.090
.023
.016
.015
.008
.320
.290

### 16-Pin Molded


16
9
1
8
.255
.245
.200
MAX.
.755
.745
.020
NOM.
.125
MIN.
.110
.090
.022
.018
.310
.290
.011
.009
.375
.325

# Am9050

## 4096-Bit Dynamic R/W Random Access Memory

### DISTINCTIVE CHARACTERISTICS

- High density 4096 x 1 organization
- Standard 18-pin dual-in-line package
- High output drive
- TTL compatible interface (except CE)
- Low power dissipation—
  400mW typ., 750mW max. operating
  5.0mW typ., 13mW max. refresh only
  0.1mW typ., 3.0mW max. standby
- Low $I_{DD}$ current surges—easier decoupling
- Simplified timing requirements—
  Zero data hold with respect to CE
  Optional data hold with respect to R/W
  Optional data set-up with respect to R/W
- Low clock capacitance –20pF max.
- Unique fully capacitive input circuits—
  eliminate extraneous current surges
- Direct plug-in replacement for TMS 4050
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

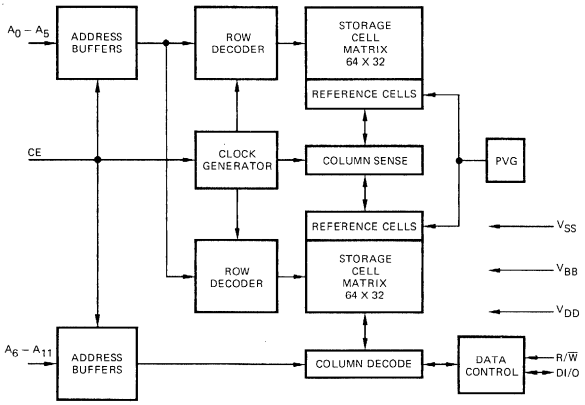
### FUNCTIONAL DESCRIPTION

The Am9050 devices are high performance, 4k-bit, dynamic, read/write, random access memories. They are organized as 4096 words by 1-bit per word. The basic memory element is a one-transistor cell that stores charge on a small internal capacitor. The memory mechanism is dynamic and the chip should be periodically refreshed in order to maintain stored data integrity.

All input signals are fully TTL compatible except the single high-level clock signal called Chip Enable. When CE goes low the memory is internally precharged and then assumes its low power standby mode. All operating cycles are initiated when CE goes high. Read-out is nondestructive so that re-writing is not necessary. Successive read and write operations at the same location can improve performance since readdressing is not required. This combination is specified as a Read/Modify/Write cycle.

Data In and Data Out signals are bussed together as a common I/O signal line. An external pull-up resistor is used for TTL compatibility. Input and output data are the same polarity.

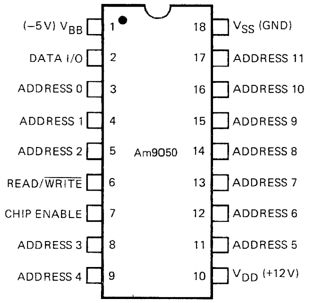
### BLOCK DIAGRAM



$A_0 - A_5$
ADDRESS BUFFERS
ROW DECODER
STORAGE CELL MATRIX 64 X 32
REFERENCE CELLS
CE
CLOCK GENERATOR
COLUMN SENSE
PVG
REFERENCE CELLS
$V_{SS}$
ROW DECODER
STORAGE CELL MATRIX 64 X 32
$V_{BB}$
$V_{DD}$
$A_6 - A_{11}$
ADDRESS BUFFERS
COLUMN DECODE
DATA CONTROL
R/W̄
DI/O

### CONNECTION DIAGRAM

Top View



(–5V) $V_{BB}$ 1
DATA I/O 2
ADDRESS 0 3
ADDRESS 1 4
ADDRESS 2 5
READ/WRITE 6
CHIP ENABLE 7
ADDRESS 3 8
ADDRESS 4 9
Am9050
18 $V_{SS}$ (GND)
17 ADDRESS 11
16 ADDRESS 10
15 ADDRESS 9
14 ADDRESS 8
13 ADDRESS 7
12 ADDRESS 6
11 ADDRESS 5
10 $V_{DD}$ (+12V)

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Access Time | | |
|---|---|---|---|---|
| | | 300ns | 250ns | 200ns |
| 0°C ≤ $T_A$ ≤ +70°C | Molded DIP | AM9050CPC | AM9050DPC | AM9050EPC |
| | Hermetic DIP | AM9050CDC | AM9050DDC | AM9050EDC |

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature Under Bias | 0°C to +70°C |
| All Supply Voltages with Respect to $V_{BB}$ | –0.3 V to +20 V |
| All Input Signal Voltages with Respect to $V_{BB}$ | –0.3 V to +20 V |
| Output Voltage with Respect to $V_{SS}$, Operating | –2.0 V to +7.0 V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Ambient Temperature | $V_{DD}$ | $V_{SS}$ | $V_{BB}$ |
|---|---|---|---|
| 0°C to +70°C | +12 V ± 5% | 0 | –5.0 V ± 10% |

No signal or supply voltage should ever be more than 0.3 V more negative than $V_{BB}$.

## ELECTRICAL CHARACTERISTICS over operating range (note 1)

| Parameters | Description | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –0.5 mA<br>2.2 kΩ to 5.5 V | | 2.4 | | $V_{CC}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 5mA | | $V_{SS}$ | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage (Except CE) | | | 2.4 | | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage (Except CE) | | | –0.6 | | 0.8 | Volts |
| $V_{IH(CE)}$ | Chip Enable Input HIGH Voltage | | | $V_{DD}$ –0.6 | | $V_{DD}$ +1.0 | Volts |
| $V_{IL(CE)}$ | Chip Enable Input LOW Voltage | | | –1.0 | | 0.8 | Volts |
| $I_I$ | Input Load Current (Except CE) | 0.6 V ≤ $V_I$ ≤ 5.5 V | | | | 10 | µA |
| $I_{I(CE)}$ | Input Load Current, CE | –1.0 ≤ $V_{I(CE)}$ ≤ 13.2 V | | | | 10 | µA |
| $I_{DD}$ | $V_{DD}$ Supply Current | $V_{IH(CE)}$ = 13.2 V | | | 35 | 60 | mA |
| | | $V_{IL(CE)}$ = 0.6 V | | | 10 | 200 | µA |
| $I_{DD(AV)}$ | Average $V_{DD}$ Supply Current | Read or Write cycle minimum cycle time | Am9050C | | 32 | 60 | mA |
| | | | Am9050D | | 34 | 60 | |
| | | | Am9050E | | 35 | 60 | |
| | | Read/Modify/Write cycle minimum cycle time | Am9050C | | 32 | 60 | |
| | | | Am9050D | | 34 | 60 | |
| | | | Am9050E | | 35 | 60 | |
| $I_{BB}$ | $V_{BB}$ Supply Current | $V_{BB}$ = –5.5 V, $V_{DD}$ = 12.6 V<br>$V_{SS}$ = 0 V | | | –5.0 | –100 | µA |

## CAPACITANCE

| Parameters | Description | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $C_i$ | Input Capacitance (Except CE) | $V_{DD}$ = 12 V, $V_{SS}$ = 0 V<br>$V_{BB}$ = –5.0 V<br>All inputs = 0 V<br>f = 1 MHz | | | 5.0 | 7.0 | pF |
| $C_{i(CE)}$ | Input Capacitance (Chip Enable) | | $V_{I(CE)}$ = 0, 12 V | | 15 | 20 | pF |
| $C_{I/O}$ | I/O Capacitance | | | | 6.0 | 8.0 | pF |

## SWITCHING CHARACTERISTICS over operating range

| Parameters | Description | Test Conditions | Am9050C Min. | Am9050C Max. | Am9050D Min. | Am9050D Max. | Am9050E Min. | Am9050E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_R$ | Column Refresh Interval | | | 2.0 | | 2.0 | | 2.0 | ms |

**Read Cycle**

| Parameters | Description | Test Conditions | Am9050C Min. | Am9050C Max. | Am9050D Min. | Am9050D Max. | Am9050E Min. | Am9050E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{c(rd)}$ | Read Cycle Time | CE transition times ≤ 20ns | 470 | | 430 | | 400 | | ns |
| $t_{w(CEH)}$ | Chip Enable HIGH Pulse Width | Chip Enable transition times ≤ 40ns | 300 | 4000 | 260 | 4000 | 230 | 4000 | ns |
| $t_{w(CEL)}$ | Chip Enable LOW Pulse Width | | 130 | | 130 | | 130 | | ns |
| $t_{su(ad)}$ | Address Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(rd)}$ | Read Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{h(ad)}$ | Address Hold Time | | 125 | | 100 | | 100 | | ns |
| $t_{h(rd)}$ | Read Hold Time | | 0 | | 0 | | 0 | | ns |
| $t_{POD}$ | CE to Output Disable Delay | Output load: TTL gate, 50pF 2.2kΩ to 5.5V | 40 | | 40 | | 40 | | ns |
| $t_{a(CE)}$ | Chip Enable Access Time (Note 6) | Chip Enable rise time ≤20ns | | 280 | | 230 | | 180 | ns |
| $t_{a(ad)}$ | Address Access Time (Note 6) | | | 300 | | 250 | | 200 | ns |

**Write Cycle**

| Parameters | Description | Test Conditions | Am9050C Min. | Am9050C Max. | Am9050D Min. | Am9050D Max. | Am9050E Min. | Am9050E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{c(wr)}$ | Write Cycle Time | CE transition times ≤ 20ns | 470 | | 430 | | 400 | | ns |
| $t_{w(CEH)}$ | Chip Enable HIGH Pulse Width | Chip Enable transition times ≤ 40ns | 300 | 4000 | 260 | 4000 | 230 | 4000 | ns |
| $t_{w(CEL)}$ | Chip Enable LOW Pulse Width | | 130 | | 130 | | 130 | | ns |
| $t_{w(wr)}$ | Write Pulse Width | | 200 | | 190 | | 180 | | ns |
| $t_{su(ad)}$ | Address Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(da)}$ | Data In Set-up Time | | 180 | | 170 | | 160 | | ns |
| $t_{su(wr)}$ | Write Pulse Set-up Time | | 240 | | 220 | | 210 | | ns |
| $t_{h(ad)}$ | Address Hold Time | | 125 | | 100 | | 100 | | ns |
| $t_{h(da)}$ | Data In Hold Time (Note 2) | | 0(30) | | 0(20) | | 0(10) | | ns |
| $t_{d(wr)}$ | Write Delay | | | 40 | | 40 | | 40 | ns |
| $t_{POI}$ | Write to Output OFF Delay | | | 40 | | 40 | | 40 | ns |

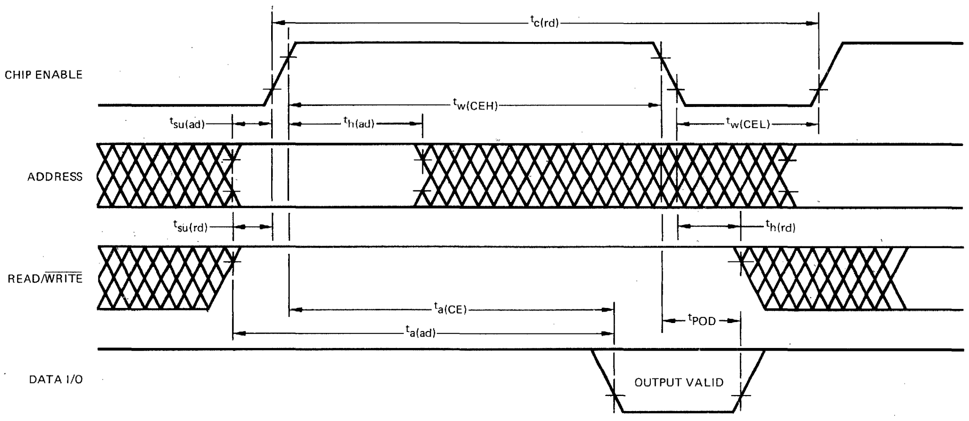
**Read/Modify/Write Cycle**

| Parameters | Description | Test Conditions | Am9050C Min. | Am9050C Max. | Am9050D Min. | Am9050D Max. | Am9050E Min. | Am9050E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{c(RMW)}$ | Read/Modify/Write Cycle Time | CE transition and Read/Write fall time ≤ 20ns | 730 | | 660 | | 600 | | ns |
| $t_{w(CEH)}$ | Chip Enable HIGH Pulse Width | | 560 | 4000 | 490 | 4000 | 430 | 4000 | ns |
| $t_{w(CEL)}$ | Chip Enable LOW Pulse Width | Chip Enable transition times ≤ 40ns | 130 | | 130 | | 130 | | ns |
| $t_{w(wr)}$ | Write Pulse Width | | 200 | | 190 | | 180 | | ns |
| $t_{su(ad)}$ | Address Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(da)}$ | Data In Set-up Time | | 180 | | 170 | | 160 | | ns |
| $t_{su(rd)}$ | Read Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(wr)}$ | Write Pulse Set-up Time | | 240 | | 220 | | 210 | | ns |
| $t_{h(ad)}$ | Address Hold Time | | 125 | | 100 | | 100 | | ns |
| $t_{h(rd)}$ | Read Hold Time | | 300 | | 250 | | 200 | | ns |
| $t_{h(da)}$ | Data In Hold Time (Note 2) | | 0(30) | | 0(20) | | 0(10) | | ns |
| $t_{POI}$ | Write to Output OFF Delay | Output load: TTL gate, 50pF 2.2kΩ to 5.5V | | 40 | | 40 | | 40 | ns |
| $t_{a(CE)}$ | Chip Enable Access Time (Note 6) | Chip Enable rise time ≤ 20ns | | 280 | | 230 | | 180 | ns |
| $t_{a(ad)}$ | Address Access Time (Note 6) | | | 300 | | 250 | | 200 | ns |

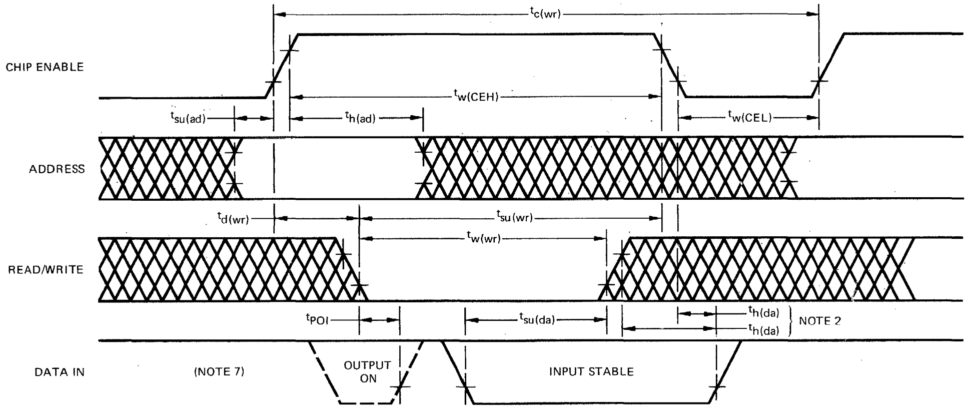
Notes:
1. Typical values are at $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Data Hold Time ($t_{h(da)}$) may be optionally specified with respect to either the rising edge of Read/Write or the falling edge of Chip Enable. The zero data hold time shown in the characteristics table is with respect to Chip Enable. Data hold time with respect to Read/Write is shown in parenthesis.
3. Input signal (except Chip Enable) timing references are 0.6 V and 2.2 V.
4. Chip Enable timing references are at 10% and 90% of $V_{IH}(CE)$.
5. Output timing references are 0.4V and 2.4V.
6. Slope of access time versus load capacitance is approximately 0.1 ns/pF.
7. In a write cycle, when $t_{d(wr)}$, the delay between the rising edge of CE and the falling edge of R/W, exceeds 40ns then the output buffer may turn on. To avoid bus conflict with input data in such a case it is recommended that $t_{w(wr)} > t_{POI}(\text{max.}) + t_{su}(da)$ be observed. When $t_{d(wr)}$ is less than 40ns the output buffer will not turn on and $t_{POI}$ will not apply. No bus conflict will occur in such a case and $t_{su(da)}$ (max.) will not be limited by the potential presence of output data.

## SWITCHING WAVEFORMS

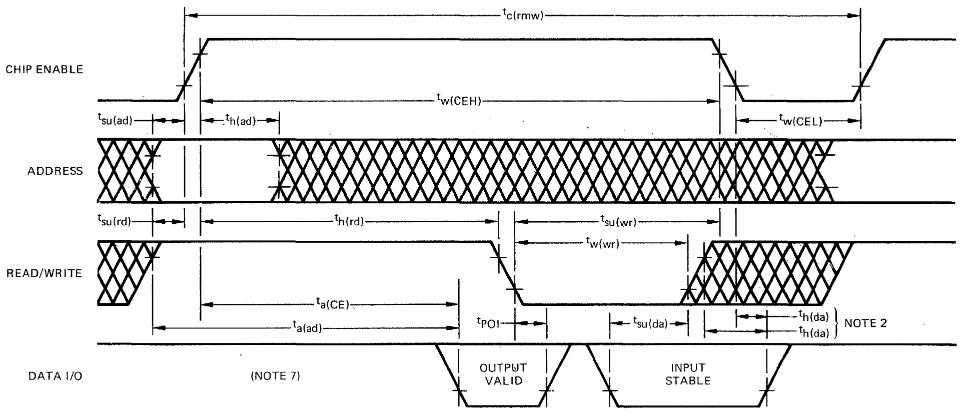
### READ CYCLE


CHIP ENABLE
ADDRESS
READ/WRITE
DATA I/O
tc(rd)
tw(CEH)
tsu(ad)
th(ad)
tw(CEL)
tsu(rd)
th(rd)
ta(CE)
ta(ad)
tPOD
OUTPUT VALID

### WRITE CYCLE


CHIP ENABLE
ADDRESS
READ/WRITE
DATA IN
tc(wr)
tw(CEH)
tsu(ad)
th(ad)
tw(CEL)
td(wr)
tsu(wr)
tw(wr)
tPOI
tsu(da)
th(da)
th(da)
NOTE 2
(NOTE 7)
OUTPUT ON
INPUT STABLE

### READ/MODIFY/WRITE CYCLE


CHIP ENABLE
ADDRESS
READ/WRITE
DATA I/O
tc(rmw)
tw(CEH)
tsu(ad)
th(ad)
tw(CEL)
tsu(rd)
th(rd)
tsu(wr)
tw(wr)
ta(CE)
ta(ad)
tPOI
tsu(da)
th(da)
th(da)
NOTE 2
(NOTE 7)
OUTPUT VALID
INPUT STABLE

## APPLICATION INFORMATION

### INTERFACE SIGNALS

The 12 Address inputs are used to specify one of $2^{12}$ locations within the memory ($2^{12} = 4096$). Chip Enable signals can be decoded externally for high order addressing so that several memory chips may be operated together for capacities greater than 4 K words. Registers are included on chip for the Address signals in order to simplify system timing requirements.

The Data In signal timing is specified relative to the rising edge of R/W. The Data In and Read/Write circuitry are static and the input data set-up requirement is independent of the write pulse width. The hold time for input data may be timed relative to either R/W or to CE, for extra flexibility in system design.

The Read/Write line controls the effective state of the I/O data line as well as the type of operation being performed. It may be thought of as a normally high signal that is pulsed low when writing is desired. The normally high state prevents unintentional modification of data. $R/\overline{W}$ should also be high during all refresh operations.

The Chip Enable input is a high level clock signal that controls the basic timing of all internal operations. When CE is low the memory enters the standby mode and dissipates very little power. Active operations begin when CE goes high. In a memory system with an array of storage chips, it is usually the case that only a few devices will be active at any one time, thus keeping the average power dissipation at very low levels.

The input and output data signals share a common I/O line. The output buffer is an open drain configuration permitting wired-OR connection of several chips for increased memory depth. Unclocked devices will have their outputs off, allowing other external data signals to dominate the I/O bus.

All input circuitry in the Am9050 memories is purely capacitive and does not cause clock related current surges to flow in the input lines. This feature improves noise immunity margins and helps simplify input driving requirements.

Current surges occur in the $V_{DD}$ and $V_{BB}$ supplies in conjunction with both the rising and falling transitions of Chip Enable. Both voltages must be decoupled to $V_{SS}$ to prevent the current spikes from generating excessive noise.

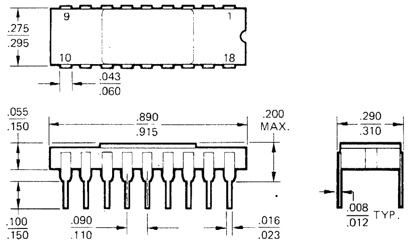
### REFRESH

Information is stored as the presence or absence of charge within each internal cell. Leakage currents eventually drain away any charge present in a cell and information is lost. To prevent data loss, a cell can have its charge level restored before too much charge has leaked off. Each cell must be refreshed at least once every 2 ms, worst case.

The 4096 cells in the memory matrix are organized as an array of 64 rows and 64 columns. When any cell within a row is actively cycled, all 64 locations in the row are refreshed. Thus the refresh requirement is met if all 64 rows are accessed every 2 ms. Address lines $A_0$ through $A_5$ specify the rows.

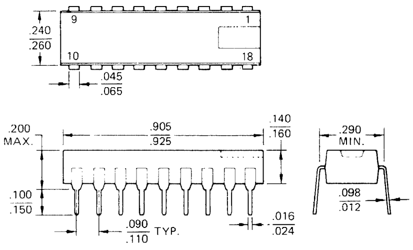
## PHYSICAL DIMENSIONS

**18- Pin Side Brazed**



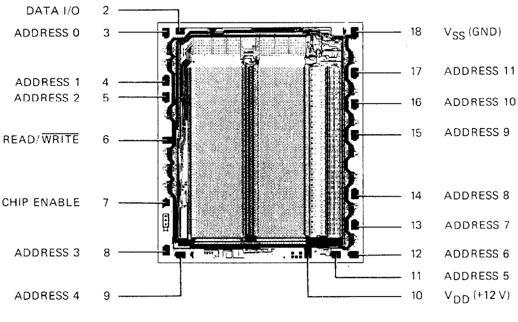
9
1
10
18
.275
.295
.043
.060
.055
.150
.890
.915
.200
MAX.
.290
.310
.100
.150
.090
.110
.016
.023
.008
.012
TYP.

**18-Pin Molded**



9
1
10
18
.240
.260
.045
.065
.200
MAX.
.905
.925
.140
.160
.290
MIN.
.100
.150
.090
.110
TYP.
.016
.024
.098
.012

**Metallization and Pad Layout**



DATA I/O 2
ADDRESS 0 3
ADDRESS 1 4
ADDRESS 2 5
READ/$\overline{WRITE}$ 6
CHIP ENABLE 7
ADDRESS 3 8
ADDRESS 4 9
18 $V_{SS}$ (GND)
17 ADDRESS 11
16 ADDRESS 10
15 ADDRESS 9
14 ADDRESS 8
13 ADDRESS 7
12 ADDRESS 6
11 ADDRESS 5
10 $V_{DD}$ (+12 V)

1 — Connected to Substrate (−5 V $V_{BB}$)

DIE SIZE 136" X 161"

# Am9060

## 4096-Bit Dynamic R/W Random Access Memory

### DISTINCTIVE CHARACTERISTICS

- High density 4096 x 1 organization
- High output drive – two full TTL loads
- TTL compatible interface (except CE)
- Low power dissipation –
  - 400 mW typ., 750 mW max. operating
  - 5.0 mW typ., 13 mW max. refresh only
  - 0.1 mW typ., 3.0 mW max. standby
- Low $I_{DD}$ current surges – easier decoupling
- Low $V_{CC}$ current drain – 10 $\mu$A
- Simplified timing requirements –
  - Zero data hold with respect to CE
  - Optional data hold with respect to R/W
  - Optional data set-up with respect to R/W
- Low clock capacitance -20 pF max.
- Unique fully capacitive input circuits – eliminate extraneous current surges
- Direct plug-in replacement for TMS4060
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

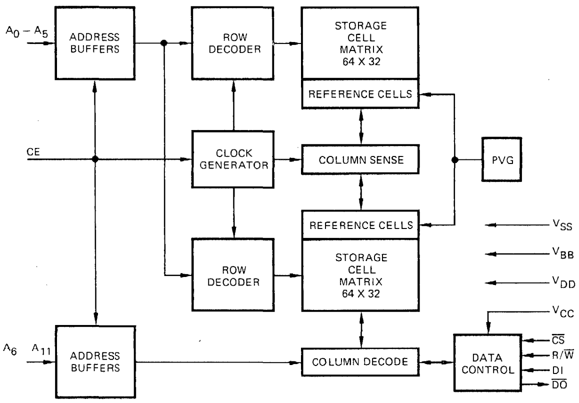
### FUNCTIONAL DESCRIPTION

The Am9060 devices are high performance, 4k-bit, dynamic, read/write, random access memories. They are organized as 4096 words by 1-bit per word. The basic memory element is a one-transistor cell that stores charge on a small internal capacitor. The memory mechanism is dynamic and the chip should be periodically refreshed in order to maintain stored data integrity.

All input signals are fully TTL compatible, except the single high-level clock signal called Chip Enable. When CE goes low the memory is internally precharged and then assumes its low power standby mode. All operating cycles are initiated when CE goes high. Read-out is nondestructive so simple read or write operations are normally performed. Successive operations at the same location can be designed to improve performance since readdressing is not required. The most useful double operation combination is specified as a Read/Modify/Write cycle.

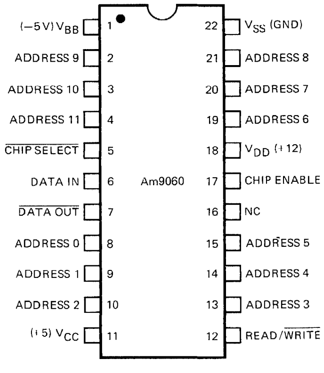
The output buffer will drive two standard TTL loads. The buffer is a three-state totem-pole configuration and exhibits a high output impedance when CE is low or when the chip is unselected. Output data polarity is inverted relative to the input data.

### BLOCK DIAGRAM


A0 – A5
ADDRESS BUFFERS
ROW DECODER
STORAGE CELL MATRIX 64 X 32
REFERENCE CELLS
CE
CLOCK GENERATOR
COLUMN SENSE
PVG
REFERENCE CELLS
VSS
VBB
VDD
VCC
ROW DECODER
STORAGE CELL MATRIX 64 X 32
A6 A11
ADDRESS BUFFERS
COLUMN DECODE
DATA CONTROL
CS
R/W
DI
DO

### CONNECTION DIAGRAM

Top View


(–5V) VBB 1
ADDRESS 9 2
ADDRESS 10 3
ADDRESS 11 4
CHIP SELECT 5
DATA IN 6
DATA OUT 7
ADDRESS 0 8
ADDRESS 1 9
ADDRESS 2 10
(+5) VCC 11
22 VSS (GND)
21 ADDRESS 8
20 ADDRESS 7
19 ADDRESS 6
18 VDD (+12)
17 CHIP ENABLE
16 NC
15 ADDRESS 5
14 ADDRESS 4
13 ADDRESS 3
12 READ/WRITE
Am9060

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Access Time | | |
|---|---|---|---|---|
| | | 300 ns | 250 ns | 200 ns |
| $0^\circ C \leq T_A \leq +70^\circ C$ | Molded DIP | AM9060CPC | AM9060DPC | AM9060EPC |
| | Hermetic DIP | AM9060CDC | AM9060DDC | AM9060EDC |

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature Under Bias | 0°C to +70°C |
| All Supply Voltages with Respect to $V_{BB}$ | –0.3V to +20V |
| All Input Signal Voltages with Respect to $V_{BB}$ | –0.3V to +20V |
| Output Voltage with Respect to $V_{SS}$, Operating | –2.0V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Ambient Temperature | $V_{DD}$ | $V_{CC}$ | $V_{SS}$ | $V_{BB}$ |
|---|---|---|---|---|
| 0°C to +70°C | +12V ± 5% | +5.0V ± 5% | 0 | –5.0V ± 10% |

No signal or supply voltage should ever be more than 0.3V more negative than $V_{BB}$.

## ELECTRICAL CHARACTERISTICS over operating range (note 1)

| Parameters | Description | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -2.0mA$ | | 2.4 | | $V_{CC}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | $V_{SS}$ | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage (Except CE) | | | 2.4 | | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage (Except CE) | | | –0.6 | | 0.8 | Volts |
| $V_{IH(CE)}$ | Chip Enable Input HIGH Voltage | | | $V_{DD}$ –0.6 | | $V_{DD}$ +1.0 | Volts |
| $V_{IL(CE)}$ | Chip Enable Input LOW Voltage | | | –1.0 | | 0.8 | Volts |
| $I_I$ | Input Load Current (Except CE) | $V_{SS} \leqslant V_I \leqslant V_{CC}$ | | | | 10 | µA |
| $I_{I(CE)}$ | Input Load Current, CE | $-1.0V \leqslant V_{I(CE)} \leqslant 13.2V$ | | | | 2.0 | µA |
| $I_{OZ}$ | Output Leakage Current | $-0.6V \leqslant V_O \leqslant V_{CC}$<br>$CE = V_{IL(CE)}$ or $\overline{CS} = V_{IH}$ | | | | 10 | µA |
| $I_{CC}$ | $V_{CC}$ Supply Current (Note 7) | $CE = V_{IL(CE)}$ or $\overline{CS} = V_{IH}$ | | | | 10 | µA |
| $I_{DD}$ | $V_{DD}$ Supply Current | $V_{IH(CE)} = 12.6V$ | | | 32 | 60 | mA |
| | | $V_{IL(CE)} = 0.6V$ | | | 10 | 200 | µA |
| $I_{DD(AV)}$ | Average $V_{DD}$ Supply Current | Read or Write cycle minimum cycle time | Am9060C | | 29 | 60 | mA |
| | | | Am9060D | | 31 | 60 | |
| | | | Am9060E | | 32 | 60 | |
| | | Read/Modify/Write cycle minimum cycle time | Am9060C | | 29 | 60 | |
| | | | Am9060D | | 31 | 60 | |
| | | | Am9060E | | 32 | 60 | |
| $I_{BB}$ | $V_{BB}$ Supply Current | $V_{BB} = -5.5V$, $V_{DD} = 12.6V$<br>$V_{CC} = 5.25V$, $V_{SS} = 0V$ | | | –5.0 | –100 | µA |

## CAPACITANCE

| Parameters | Description | Test Conditions | | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{i(AW)}$ | Input Capacitance (Address and Write) | $V_{DD} = 12V$, $V_{SS} = 0V$<br>$V_{BB} = -5.0V$, $V_{CC} = 5.0V$<br>All inputs = 0V<br>f = 1MHz | | 5.0 | 7.0 | pF |
| $C_{i(CD)}$ | Input Capacitance (Chip Select and Data) | | | 3.0 | 5.0 | pF |
| $C_{i(CE)}$ | Input Capacitance (Chip Enable) | | $V_{I(CE)} = -1.0, 10.8$ | 15 | 20 | pF |
| $C_O$ | Output Capacitance | | | 3.0 | 5.0 | pF |

## SWITCHING CHARACTERISTICS over operating range

| Parameters | Description | Test Conditions | Am9060C Min. | Am9060C Max. | Am9060D Min. | Am9060D Max. | Am9060E Min. | Am9060E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_R$ | Column Refresh Interval | | | 2.0 | | 2.0 | | 2.0 | ms |

**Read Cycle**

| Parameters | Description | Test Conditions | Am9060C Min. | Am9060C Max. | Am9060D Min. | Am9060D Max. | Am9060E Min. | Am9060E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{c(rd)}$ | Read Cycle Time | CE transition time ⩽ 20 ns | 470 | | 430 | | 400 | | ns |
| $t_{w(CEH)}$ | Chip Enable HIGH Pulse Width | Chip Enable transition times ⩽40 ns | 300 | 4000 | 260 | 4000 | 230 | 4000 | ns |
| $t_{w(CEL)}$ | Chip Enable LOW Pulse Width | | 130 | | 130 | | 130 | | ns |
| $t_{su(ad)}$ | Address Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(CS)}$ | Chip Select Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(rd)}$ | Read Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{h(ad)}$ | Address Hold Time | | 125 | | 100 | | 100 | | ns |
| $t_{h(CS)}$ | Chip Select Hold Time | | 125 | | 100 | | 100 | | ns |
| $t_{h(rd)}$ | Read Hold Time | | 0 | | 0 | | 0 | | ns |
| $t_{PZL}$ | Chip Enable to Output ON Delay | Output load: one standard TTL gate plus 50 pF | | 175 | | 150 | | 125 | ns |
| $t_{POZ}$ | Chip Enable to Output OFF Delay | | 30 | | 30 | | 30 | | ns |
| $t_{a(CE)}$ | Chip Enable Access Time (Note 6) | Chip enable rise time ⩽20 ns | | 280 | | 230 | | 180 | ns |
| $t_{a(ad)}$ | Address Access Time (Note 6) | | | 300 | | 250 | | 200 | ns |

**Write Cycle**

| Parameters | Description | Test Conditions | Am9060C Min. | Am9060C Max. | Am9060D Min. | Am9060D Max. | Am9060E Min. | Am9060E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{c(wr)}$ | Write Cycle Time | CE transition time ⩽ 20 ns | 470 | | 430 | | 400 | | ns |
| $t_{w(CEH)}$ | Chip Enable HIGH Pulse Width | Chip Enable transition times ⩽40 ns | 300 | 4000 | 260 | 4000 | 230 | 4000 | ns |
| $t_{w(CEL)}$ | Chip Enable LOW Pulse Width | | 130 | | 130 | | 130 | | ns |
| $t_{w(wr)}$ | Write Pulse Width | | 200 | | 190 | | 180 | | ns |
| $t_{su(ad)}$ | Address Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(CS)}$ | Chip Select Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(da)}$ | Data In Set-up Time | | 180 | | 170 | | 160 | | ns |
| $t_{su(wr)}$ | Write Pulse Set-up Time | | 240 | | 220 | | 210 | | ns |
| $t_{h(ad)}$ | Address Hold Time | | 125 | | 100 | | 100 | | ns |
| $t_{h(CS)}$ | Chip Select Hold Time | | 125 | | 100 | | 100 | | ns |
| $t_{h(da)}$ | Data In Hold Time (Note 2) | | 0 (30) | | 0 (20) | | 0 (10) | | ns |

**Read/Modify/Write Cycle**

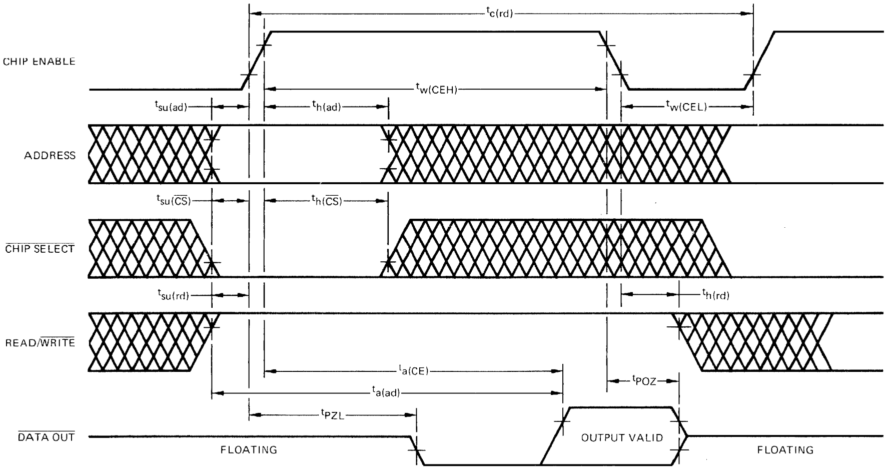
| Parameters | Description | Test Conditions | Am9060C Min. | Am9060C Max. | Am9060D Min. | Am9060D Max. | Am9060E Min. | Am9060E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{c(RMW)}$ | Read/Modify/Write Cycle Time | CE transition time and Read/Write fall time ⩽ 20 ns | 710 | | 640 | | 580 | | ns |
| $t_{w(CEH)}$ | Chip Enable HIGH Pulse Width | | 540 | 4000 | 470 | 4000 | 410 | 4000 | ns |
| $t_{w(CEL)}$ | Chip Enable LOW Pulse Width | Chip Enable transition times ⩽40 ns | 130 | | 130 | | 130 | | ns |
| $t_{w(wr)}$ | Write Pulse Width | | 200 | | 190 | | 180 | | ns |
| $t_{su(ad)}$ | Address Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(CS)}$ | Chip Select Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(da)}$ | Data In Set-up Time | | 180 | | 170 | | 160 | | ns |
| $t_{su(rd)}$ | Read Set-up Time | | 0 | | 0 | | 0 | | ns |
| $t_{su(wr)}$ | Write Pulse Set-up Time | | 240 | | 220 | | 210 | | ns |
| $t_{h(ad)}$ | Address Hold Time | | 125 | | 100 | | 100 | | ns |
| $t_{h(CS)}$ | Chip Select Hold Time | | 125 | | 100 | | 100 | | ns |
| $t_{h(rd)}$ | Read Hold Time | | 280 | | 230 | | 180 | | ns |
| $t_{h(da)}$ | Data In Hold Time (Note 2) | | 0 (30) | | 0 (20) | | 0 (10) | | ns |
| $t_{PZL}$ | Chip Enable to Output ON Delay | Output load: one standard TTL gate plus 50 pF | | 175 | | 150 | | 125 | ns |
| $t_{POI}$ | Write to Output Invalid Delay | | 30 | | 30 | | 30 | | ns |
| $t_{POZ}$ | Chip Enable to Output OFF Delay | | 30 | | 30 | | 30 | | ns |
| $t_{a(CE)}$ | Chip Enable Access Time | Chip Enable rise time ⩽20 ns | | 280 | | 230 | | 180 | ns |
| $t_{a(ad)}$ | Address Access Time (Note 6) | | | 300 | | 250 | | 200 | ns |

Notes:

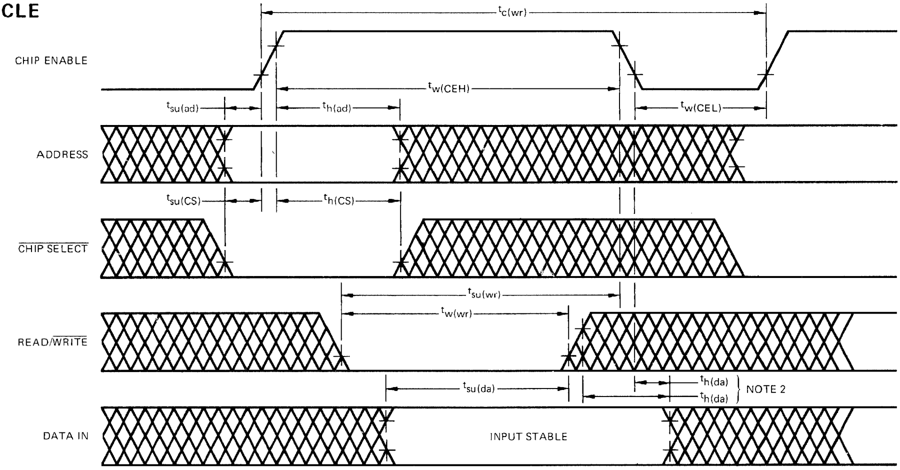
1. Typical values are at $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Data Hold time ($t_{h(da)}$) may be optionally specified with respect to either the rising edge of Read/Write or the falling edge of Chip Enable. The zero value shown in the Characteristics table is with respect to Chip Enable. Data hold time with respect to Read/Write is shown in parenthesis.
3. Input signal (except Chip Enable) timing references are 0.6 V and 2.2 V.
4. Chip Enable timing references are at 10% and 90% of $V_{IH}$(CE).
5. Output timing references are 0.4V and 2.4V.
6. Slope of access time versus load capacitance is approximately 0.1 ns/pF.
7. $V_{CC}$ supplies the final output transistor only. Except for leakage, $V_{CC}$ supply current during CE on is dependent on output loading only.

## SWITCHING WAVEFORMS

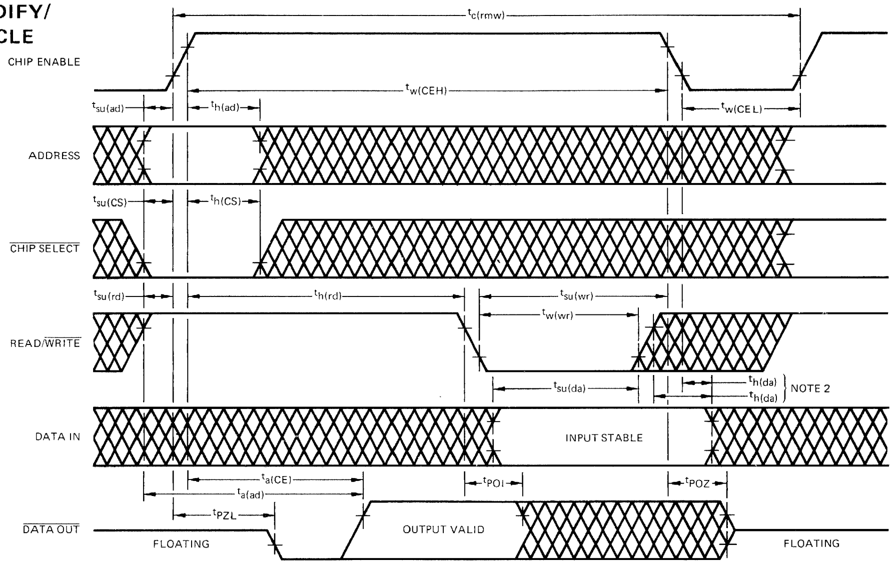
### READ CYCLE


$t_{c(rd)}$
CHIP ENABLE
$t_{w(CEH)}$
$t_{su(ad)}$
$t_{h(ad)}$
$t_{w(CEL)}$
ADDRESS
$t_{su(\overline{CS})}$
$t_{h(\overline{CS})}$
$\overline{\text{CHIP SELECT}}$
$t_{su(rd)}$
$t_{h(rd)}$
READ/$\overline{\text{WRITE}}$
$t_{a(CE)}$
$t_{POZ}$
$t_{a(ad)}$
$t_{PZL}$
$\overline{\text{DATA OUT}}$
FLOATING
OUTPUT VALID
FLOATING

### WRITE CYCLE


$t_{c(wr)}$
CHIP ENABLE
$t_{w(CEH)}$
$t_{su(ad)}$
$t_{h(ad)}$
$t_{w(CEL)}$
ADDRESS
$t_{su(CS)}$
$t_{h(CS)}$
$\overline{\text{CHIP SELECT}}$
$t_{su(wr)}$
$t_{w(wr)}$
READ/$\overline{\text{WRITE}}$
$t_{su(da)}$
$t_{h(da)}$
$t_{h(da)}$
NOTE 2
DATA IN
INPUT STABLE

### READ/MODIFY/ WRITE CYCLE


$t_{c(rmw)}$
CHIP ENABLE
$t_{w(CEH)}$
$t_{su(ad)}$
$t_{h(ad)}$
$t_{w(CEL)}$
ADDRESS
$t_{su(CS)}$
$t_{h(CS)}$
$\overline{\text{CHIP SELECT}}$
$t_{su(rd)}$
$t_{h(rd)}$
$t_{su(wr)}$
$t_{w(wr)}$
READ/$\overline{\text{WRITE}}$
$t_{su(da)}$
$t_{h(da)}$
$t_{h(da)}$
NOTE 2
DATA IN
INPUT STABLE
$t_{a(CE)}$
$t_{a(ad)}$
$t_{POI}$
$t_{POZ}$
$t_{PZL}$
$\overline{\text{DATA OUT}}$
FLOATING
OUTPUT VALID
FLOATING

## APPLICATION INFORMATION

### INTERFACE SIGNALS

The 12 Address inputs are used to specify one of $2^{12}$ locations within the memory ($2^{12} = 4096$). The Chip Select signal acts as a high order address so that several memory chips may be operated together for capacities greater than 4k words. Registers are included on chip for the Chip Select and Address signals in order to simplify system timing requirements. After the Chip Select input has been latched by the rising edge of CE, the select status of the chip cannot be altered by changing the state of Chip Select line. Chip Select only affects the data control circuitry.

The Data In signal timing is specified relative to the rising edge of R/$\overline{\text{W}}$. The Data In and Read/Write circuitry are static and the input data set-up requirement is independent of the write pulse width. The hold time for input data may be timed relative to either R/$\overline{\text{W}}$ or to CE, for extra flexibility in system design.

The Read/Write line controls the type of operation being performed. It may be thought of as a normally high signal that is pulsed low when writing is desired. The normally high state prevents unintentional modification of data. R/$\overline{\text{W}}$ should also be high during all refresh operations, unless Chip Select is high.

The Chip Enable input is a high level clock signal that controls the basic timing of all internal operations. When CE is low the memory enters the standby mode and dissipates very little power. Active operations begin when CE goes high. In a memory system with an array of storage chips, it is usually the case that only a few devices will be active at any one time, thus keeping the average power dissipation at very low levels.

The Data Out circuitry is three-state and designed to permit wired-OR connection of several chips for greater memory depth than 4k. Unclocked or unselected devices will have high impedance outputs, allowing a selected and clocked device to dominate the output data bus. The output data is inverted relative to the input data; that is, information written in as a logic one will be read out as a logic zero. Valid output is always preceded by a period of low output data.

All input circuitry in the Am9060 memories is purely capacitive and does not cause clock related current surges to flow in the input lines. This feature improves noise immunity margins and helps simplify input driving requirements.

Current surges occur in the $V_{DD}$ and $V_{BB}$ supplies in conjunction with both the rising and falling transitions of Chip Enable. Both voltages must be carefully decoupled to $V_{SS}$ to prevent the current spikes from generating excessive noise.

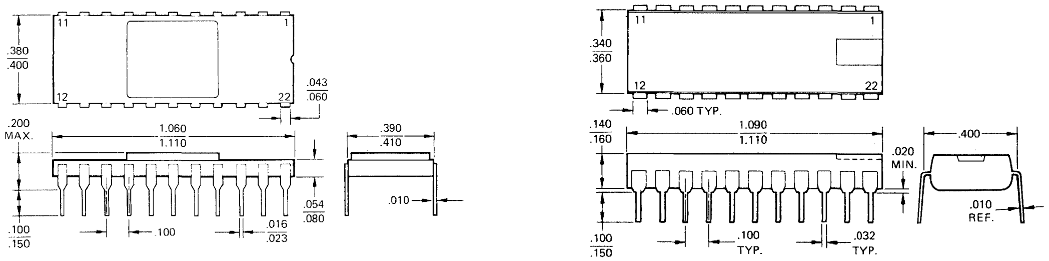
### REFRESH

Information is stored as the presence or absence of charge within each internal cell. Leakage currents eventually drain away any charge present in a cell and information is lost. To prevent data loss, a cell can have its charge level restored before too much charge has leaked off. Each cell must be refreshed at least once every 2 ms, worst case.

The 4096 cells in the memory matrix are organized as an array of 64 rows and 64 columns. When any cell within a row is actively cycled, all 64 locations in the row are refreshed. Thus the refresh requirement is met if all 64 rows are accessed every 2 ms. Address lines $A_0$ through $A_5$ specify the rows.

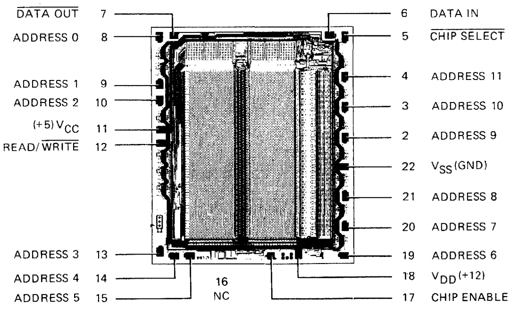
The Chip Select input only controls the Data Out and Read/Write circuitry so that a chip need not be selected in order to be refreshed. This allows parallel refreshing of many devices without causing contention on output busses.

## PHYSICAL DIMENSIONS


22-Pin Side Brazed

22-Pin Molded
11
1
12
22
.380
.400
.043
.060
.200
MAX.
1.060
1.110
.390
.410
.010
.054
.080
.016
.023
.100
.150
.100
11
1
12
22
.340
.360
.060 TYP.
.140
.160
1.090
1.110
.020
MIN.
.400
.010
REF.
.100
.150
.100
TYP.
.032
TYP.

## Metallization and Pad Layout


DATA OUT 7
ADDRESS 0 8
ADDRESS 1 9
ADDRESS 2 10
(+5) $V_{CC}$ 11
READ/$\overline{\text{WRITE}}$ 12
ADDRESS 3 13
ADDRESS 4 14
ADDRESS 5 15
16
NC
6 DATA IN
5 $\overline{\text{CHIP SELECT}}$
4 ADDRESS 11
3 ADDRESS 10
2 ADDRESS 9
22 $V_{SS}$(GND)
21 ADDRESS 8
20 ADDRESS 7
19 ADDRESS 6
18 $V_{DD}$(+12)
17 CHIP ENABLE

1 — Connected to Substrate (−5V)$V_{BB}$

DIE SIZE 136" X 161"

# Am9101/Am91L01/Am2101 FAMILY

## 256x4 Static R/W Random Access Memories

| PART NUMBER | Am2101 | Am2101-2 | Am9101A<br>Am91L01A<br>Am2101-1 | Am9101B<br>Am91L01B | Am9101C<br>Am91L01C | Am9101D | Am9101E |
|---|---|---|---|---|---|---|---|
| ACCESS TIME | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns | 200ns |

### DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization
- Low operating power
  125mW Typ; 290mW maximum – standard power
  100mW Typ; 175mW maximum – low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive – two full TTL loads
- High noise immunity – full 400mV
- Single 5 volt power supply – tolerances: ±5% commercial, ±10% military
- Uniform switching characteristics – access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Two chip enable inputs
- Output disable control
- Zero address set-up and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

### FUNCTIONAL DESCRIPTION

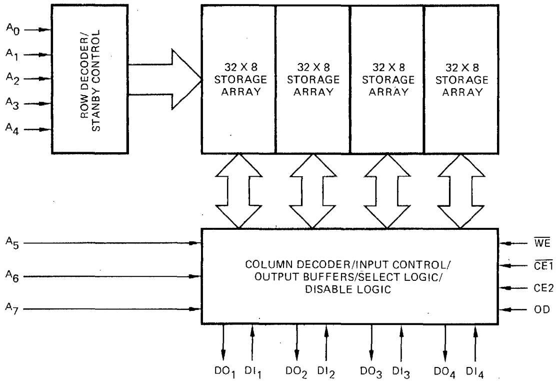
The Am9101/Am91L01 series of devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

These memories may be operated in a DC standby mode for reductions of as much as 84 percent of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L01 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

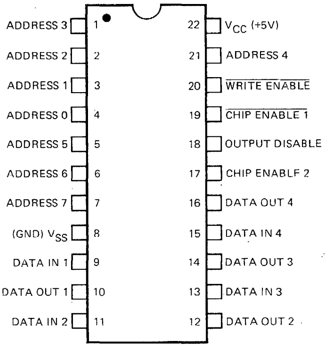
The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are all fully static and no refresh operations or sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

### Am9101 BLOCK DIAGRAM


$A_0$
$A_1$
$A_2$
$A_3$
$A_4$
ROW DECODER/ STANBY CONTROL
32 X 8 STORAGE ARRAY
32 X 8 STORAGE ARRAY
32 X 8 STORAGE ARRAY
32 X 8 STORAGE ARRAY
$A_5$
$A_6$
$A_7$
COLUMN DECODER/INPUT CONTROL/ OUTPUT BUFFERS/SELECT LOGIC/ DISABLE LOGIC
$\overline{WE}$
$\overline{CE1}$
CE2
OD
$DO_1$ $DI_1$ $DO_2$ $DI_2$ $DO_3$ $DI_3$ $DO_4$ $DI_4$

### CONNECTION DIAGRAM
### Top View


ADDRESS 3 1
ADDRESS 2 2
ADDRESS 1 3
ADDRESS 0 4
ADDRESS 5 5
ADDRESS 6 6
ADDRESS 7 7
(GND) $V_{SS}$ 8
DATA IN 1 9
DATA OUT 1 10
DATA IN 2 11
22 $V_{CC}$ (+5V)
21 ADDRESS 4
20 $\overline{\text{WRITE ENABLE}}$
19 $\overline{\text{CHIP ENABLE 1}}$
18 OUTPUT DISABLE
17 CHIP ENABLF 2
16 DATA OUT 4
15 DATA IN 4
14 DATA OUT 3
13 DATA IN 3
12 DATA OUT 2

Note: Flat Pack version available in 24-pin package.

### ORDERING INFORMATION

| AMBIENT TEMPERATURE SPECIFICATION | PACKAGE TYPE | POWER TYPE | ACCESS TIMES | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns | 200ns |
| 0°C to +70°C | Molded DIP | Standard | P2101 | P2101-2 | P2101-1<br>AM9101APC | AM9101BPC | AM9101CPC | AM9101DPC | AM9101EPC |
| | | Low | | | AM91L01APC | AM91L01BCP | AM91L01CPC | | |
| | Hermetic DIP | Standard | C2101 | C2101-2 | C2101-1<br>AM9101ADC | AM9101BDC | AM9101CDC | AM9101DDC | AM9101EDC |
| | | Low | | | AM91L01ADC | AM91L01BDC | AM91L01CDC | | |
| –55°C to +125°C | Hermetic DIP | Standard | | | AM9101ADM | AM9101BDM | AM9101CDM | | |
| | | Low | | | AM91L01ADM | AM91L01BDM | AM91L01CDM | | |
| | Hermetic Flat Pack | Standard | | | AM9101AFM | AM9101BFM | | | |
| | | Low | | | AM91L01AFM | AM91L01BFM | | | |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ With Respect to $V_{SS}$, Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

## ELECTRICAL CHARACTERISTICS

Am9101PC, Am9101DC  $T_A = 0°C$ to $+70°C$
Am91L01PC Am91L01DC  $V_{CC} = +5.0V \pm 5\%$
Am2101

| Parameters | Description | Test Conditions | | | Am9101/ Am91L01 Family | | Am2101 Family | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN. | | $I_{OH} = -200\mu A$ | 2.4 | | | | Volts |
| | | | | $I_{OH} = -150\mu A$ | | | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN. | | $I_{OL} = 3.2mA$ | | 0.4 | | | Volts |
| | | | | $I_{OL} = 2.0mA$ | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | 2.2 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | −0.5 | 0.65 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leq V_{IN} \leq 5.25V$ | | | | 10 | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{\overline{CE}} = V_{IH}$ | | $V_{OUT} = V_{CC}$ | | 5.0 | | 15 | μA |
| | | | | $V_{OUT} = 0.4V$ | | −10 | | −50 | |
| $I_{CC1}$ | Power Supply Current | Data out open<br>$V_{CC}$ = Max.<br>$V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9101A/B | | 50 | | 60 | mA |
| | | | | Am9101C/D/E | | 55 | | | |
| | | | | Am91L01A/B | | 31 | | | |
| | | | | Am91L01C | | 34 | | | |
| $I_{CC2}$ | | | $T_A = 0°C$ | Am9101A/B | | 55 | | 70 | |
| | | | | Am9101C/D/E | | 60 | | | |
| | | | | Am91L01A/B | | 33 | | | |
| | | | | Am91L01C | | 36 | | | |

## ELECTRICAL CHARACTERISTICS

Am9101DM, Am9101FM  $T_A = -55°C$ to $+125°C$
Am91L01DM, Am91L01FM  $V_{CC} = +5.0V \pm 10\%$

| Parameters | Description | Test Conditions | | | Am9101/ Am91L01 Family | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | | $V_{CC} = 4.75V$ | 2.4 | | Volts |
| | | | | $V_{CC} = 4.5V$ | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leq V_{IN} \leq 5.5V$ | | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{\overline{CE}} = V_{IH}$ | | $V_{OUT} = V_{CC}$ | | 10 | μA |
| | | | | $V_{OUT} = 0.4V$ | | −10 | |
| $I_{CC1}$ | Power Supply Current | Data out open<br>$V_{CC}$ = Max.<br>$V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9101A/B | | 50 | mA |
| | | | | Am9101C | | 55 | |
| | | | | Am91L01A/B | | 31 | |
| | | | | Am91L01C | | 34 | |
| $I_{CC3}$ | | | $T_A = -55°C$ | Am9101A/B | | 60 | |
| | | | | Am9101C | | 65 | |
| | | | | Am91L01A/B | | 37 | |
| | | | | Am91L01C | | 40 | |

## CAPACITANCE

| Parameters | Description | Test Conditions | | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance, $V_{IN} = 0V$ | $T_A = 25°C$, f = 1 mHz | Am2101 | 4.0 | 8.0 | pF |
| | | | Am9101/Am91L01 | 3.0 | 6.0 | |
| $C_{OUT}$ | Output Capacitance, $V_{OUT} = 0V$ | | Am2101 | 8.0 | 12 | pF |
| | | | Am9101/Am91L01 | 6.0 | 9.0 | |

## SWITCHING CHARACTERISTICS over operating temperature and voltage range

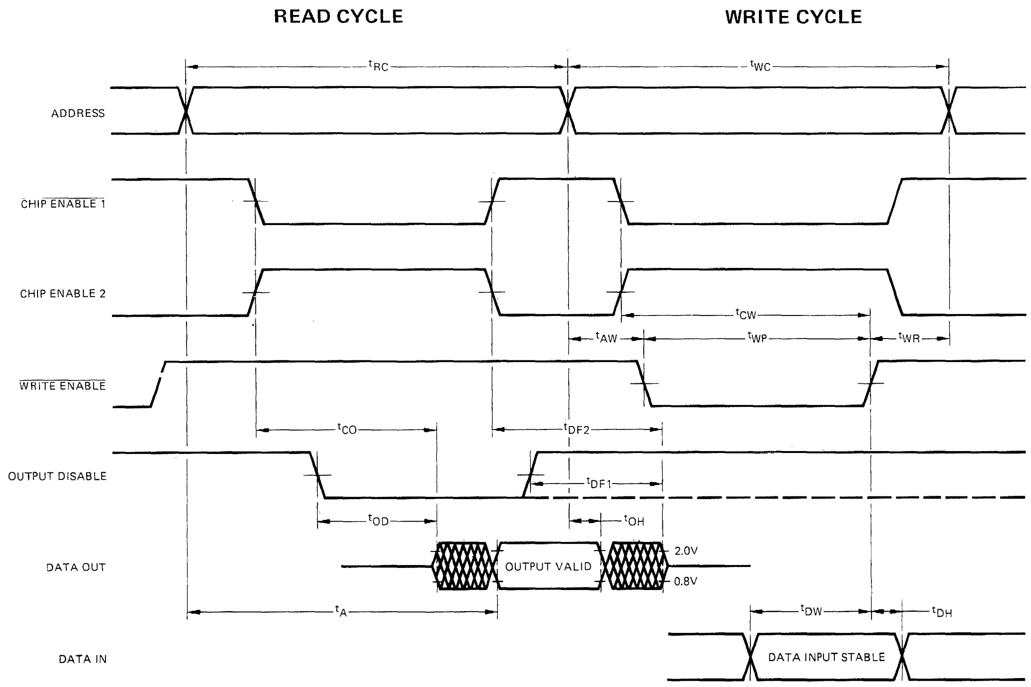
Output Load = 1 TTL Gate +100pF
Transition Times = 10ns
Input Levels, Output References = 0.8V and 2.0V

$T_A$ = 0°C to +70°C $V_{CC}$ = +5V ±5%
$T_A$ = −55°C to +125°C $V_{CC}$ = +5V ±10%

| Parameters | Description | 2101 | | 2101-2 | | 2101-1 | | 9101A<br>91L01A | | 9101B<br>91L01B | | 9101C<br>91L01C | | 9101D | | 9101E | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| $t_A$ | Access Time | | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| $t_{CO}$ | Chip Enable to Output ON Delay (Note 1) | | 800 | | 400 | | 350 | | 200 | | 175 | | 150 | | 125 | | 100 | ns |
| $t_{OD}$ | Output Disable to Output ON Delay | | 700 | | 350 | | 300 | | 175 | | 150 | | 125 | | 100 | | 85 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 0 | | 0 | | 0 | | 40 | | 40 | | 40 | | 30 | | 30 | | ns |
| $t_{DF1}$ | Output Disable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | 5.0 | 125 | 5.0 | 100 | 5.0 | 100 | 5.0 | 75 | 5.0 | 60 | ns |
| $t_{DF2}$ | Chip Enable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | 10 | 125 | 10 | 125 | 10 | 100 | 10 | 100 | 10 | 80 | ns |
| $t_{WC}$ | Write Cycle Time | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| $t_{AW}$ | Address Set-up Time | 150 | | 150 | | 100 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 750 | | 400 | | 300 | | 175 | | 150 | | 125 | | 100 | | 85 | | ns |
| $t_{CW}$ | Chip Enable Set-up Time (Note 1) | 900 | | 550 | | 400 | | 175 | | 150 | | 125 | | 100 | | 85 | | ns |
| $t_{WR}$ | Address Hold Time | 50 | | 50 | | 50 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DW}$ | Input Data Set-up Time | 700 | | 400 | | 280 | | 150 | | 125 | | 100 | | 85 | | 65 | | ns |
| $t_{DH}$ | Input Data Hold Time | 100 | | 100 | | 100 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

Notes: 1. Both $\overline{CE1}$ and CE2 must be true to enable the chip.

## SWITCHING WAVEFORMS


READ CYCLE
WRITE CYCLE
$t_{RC}$
$t_{WC}$
ADDRESS
$\overline{\text{CHIP ENABLE 1}}$
CHIP ENABLE 2
$t_{CW}$
$t_{AW}$
$t_{WP}$
$t_{WR}$
$\overline{\text{WRITE ENABLE}}$
$t_{CO}$
$t_{DF2}$
OUTPUT DISABLE
$t_{DF1}$
$t_{OD}$
$t_{OH}$
DATA OUT
OUTPUT VALID
2.0V
0.8V
$t_A$
$t_{DW}$
$t_{DH}$
DATA IN
DATA INPUT STABLE

## DEFINITION OF TERMS

### FUNCTIONAL TERMS

**$\overline{CE1}$, CE2** Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ is low and CE2 is high.

**$\overline{WE}$** Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

**$t_{OD}$** Output enable time. Delay time from falling edge of OD to output on.

**$t_{RC}$** Read Cycle Time. The minimum time required between successive address changes while reading.

**$t_A$** Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

**$t_{CO}$** Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

**$t_{OH}$** Minimum time which will elapse between change of address and any change of the data output.

**$t_{DF1}$** Time delay between output disable HIGH and output data float.

**$t_{DF2}$** Time delay between chip enable OFF and output data float.

**$t_{WC}$** Write Cycle Time. The minimum time required between successive address changes while writing.

**$t_{AW}$** Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

**$t_{WP}$** The minimum duration of a LOW level on the write enable guaranteed to write data.

**$t_{WR}$** Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

**$t_{DW}$** Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

**$t_{DH}$** Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

**$t_{CW}$** Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

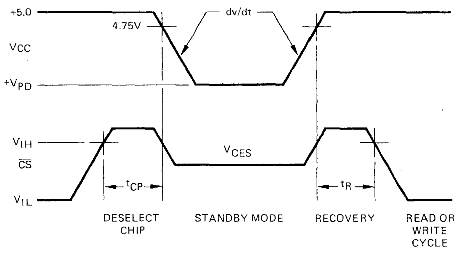
## POWER DOWN STANDBY OPERATION

The Am9101/Am91L01 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

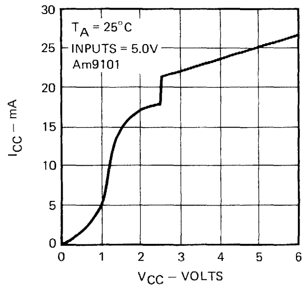
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at $V_{IH}$ or $V_{CES}$ during the entire standby cycle.

## STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

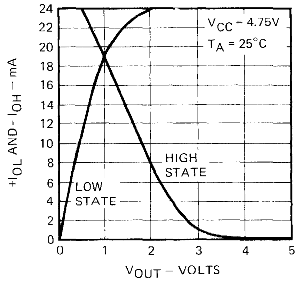
| Parameters | Description | Test Conditions | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A = 0°C$<br>All Inputs – $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L01 | | 11 | 25 | mA |
| | | | | Am9101 | | 13 | 31 | |
| | | | $V_{PD} = 2.0V$ | Am91L01 | | 13 | 31 | |
| | | | | Am9101 | | 17 | 41 | |
| | | $T_A = -55°C$<br>All inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L01 | | 11 | 28 | mA |
| | | | | Am9101 | | 13 | 34 | |
| | | | $V_{PD} = 2.0V$ | Am91L01 | | 13 | 34 | |
| | | | | Am9101 | | 17 | 46 | |
| dv/dt | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/µs |
| $t_R$ | Standby Recovery Time | | | | $t_{RC}$ | | | ns |
| $t_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |


+5.0
4.75V
dv/dt
VCC
+VPD
VIH
CS
VCES
VIL
tCP
tR
DESELECT CHIP
STANDBY MODE
RECOVERY
READ OR WRITE CYCLE

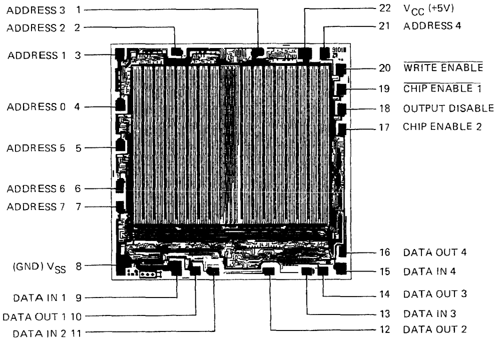
### Typical Power Supply Current Versus Voltage



### Typical Output Current Versus Voltage



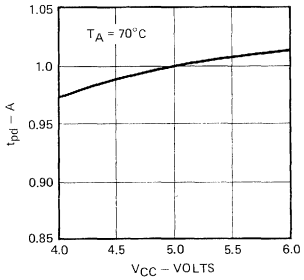
### Metallization and Pad Layout


ADDRESS 3 1
ADDRESS 2 2
ADDRESS 1 3
ADDRESS 0 4
ADDRESS 5 5
ADDRESS 6 6
ADDRESS 7 7
(GND) VSS 8
DATA IN 1 9
DATA OUT 1 10
DATA IN 2 11
22 VCC (+5V)
21 ADDRESS 4
20 WRITE ENABLE
19 CHIP ENABLE 1
18 OUTPUT DISABLE
17 CHIP ENABLE 2
16 DATA OUT 4
15 DATA IN 4
14 DATA OUT 3
13 DATA IN 3
12 DATA OUT 2

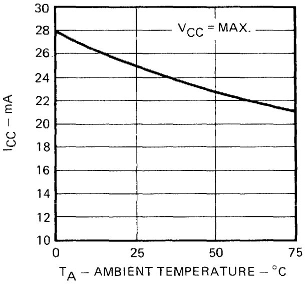
DIE SIZE 0.132" X 0.131"

(Pin numbers are for DIP configurations only)

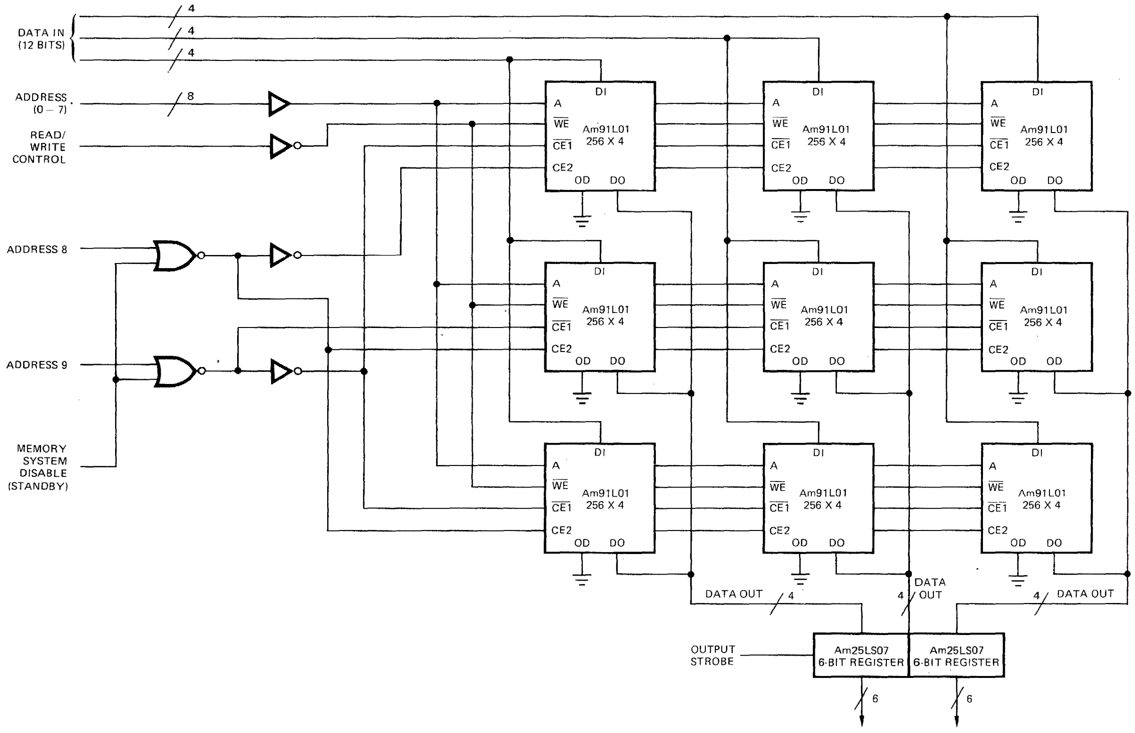
### Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ = +5.0 Volts



### Typical Power Supply Current Versus Ambient Temperature

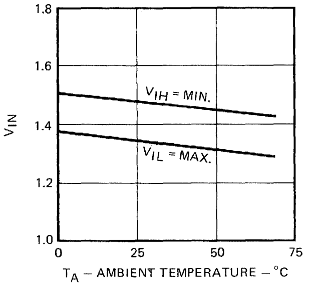


## APPLICATIONS

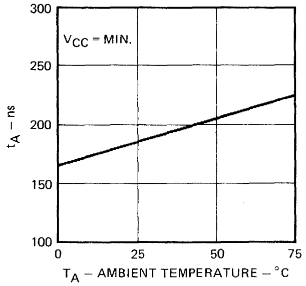

DATA IN
(12 BITS)
4
4
4
ADDRESS
(0 – 7)
8
READ/
WRITE
CONTROL
ADDRESS 8
ADDRESS 9
MEMORY
SYSTEM
DISABLE
(STANDBY)
DI
A
WE
CE1
CE2
Am91L01
256 X 4
OD
DO
DATA OUT
4
DATA
OUT
OUTPUT
STROBE
Am25LS07
6-BIT REGISTER
6

MEMORY SYSTEM
768 WORDS BY 12 BITS PER WORD

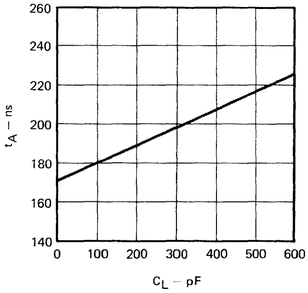
**Typical $V_{IN}$ Limits Versus Ambient Temperature**



**Typical $t_A$ Versus Ambient Temperature**



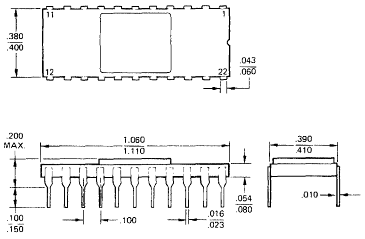
**Typical $t_A$ Versus $C_L$**



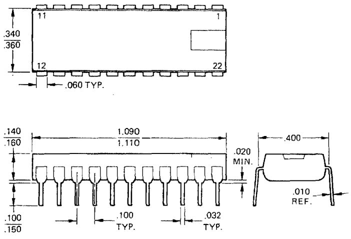
## PHYSICAL DIMENSIONS

### Dual-In-Line

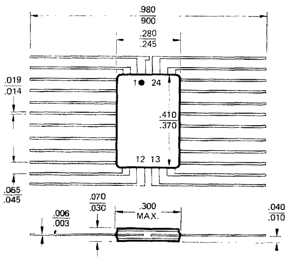
**22-Pin Side-Brazed**


11
1
12
22
.380
.400
.043
.060
.200
MAX.
1.060
1.110
.390
.410
.054
.080
.010
.100
.150
.100
.016
.023

**22-Pin Molded**


11
1
12
22
.340
.360
.060 TYP.
.140
.160
1.090
1.110
.020
MIN.
.400
.010
REF.
.100
.150
.100
TYP.
.032
TYP.

**24-Pin Flat Package**


.980
.900
.280
.245
.019
.014
1
24
.410
.370
12
13
.065
.045
.070
.030
.006
.003
.300
MAX.
.040
.010

# Am9102/Am91L02 FAMILY

## 1024x1 Static R/W Random Access Memories

### DISTINCTIVE CHARACTERISTICS

- Low-Power Dissipation
  100 mW typical; 260 mW maximum
- Standby operating mode reduces power 84%
  18 mW typical; 42 mW maximum
- Input and output voltage levels identical to TTL
- High-Output Drive – Two full TTL loads guaranteed
- High Noise Immunity – 400 mV guaranteed
- Uniform Access Times
  Switching characteristics are insensitive to data patterns, addressing patterns, and power supply variations
- Single 5-Volt Power Supply
  10% tolerance for full temperature range devices
  5% tolerance for commercial range devices
- High-Performance Plug-In Replacement for: Intel 2102, Signetics 2602, Intersil IM7552, Mostek 4102,TI4033/4/5
- Available for operation over both commercial and military ranges
- 100% reliability assurance testing in accordance with MIL-STD-883
- Zero data hold and address hold times simplify timing requirements

### FUNCTIONAL DESCRIPTION

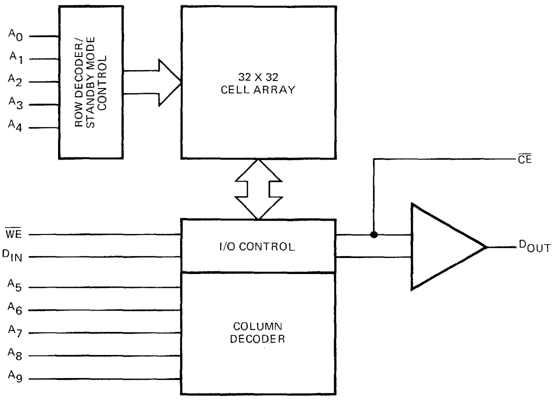
The Am9102 Family of 1024-bit static N-channel RAMs contains members with cycle times ranging from 650ns to 200ns All the devices are organized as 1024 x 1, and all have a power-saving standby operating mode.

Each device has a chip enable input (CE) that controls a three-state output to make construction of large memory systems simple. Reading and writing are performed by enabling the chip and applying a LOW to write or a HIGH to read on the write enable input ($\overline{\text{WE}}$). All inputs are directly TTL compatible with no external components required, and the output will drive two full TTL loads in both the HIGH and LOW states.

The devices operate from a single +5 volt power supply. The power dissipation of the devices can be reduced to about 16% of the normal operating power by lowering the voltage on the power supply pin. Data is guaranteed to be retained in the power-down condition.

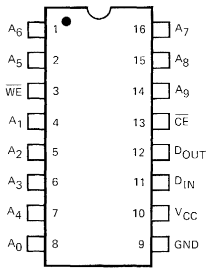
All unit members in the family are available in plastic or hermetic DIPs for operation over the commercial temperature range and, except for the Am9102D/E, may all also be purchased for operation over the military temperature range. All AC and DC parameters are guaranteed over the operating range.

### BLOCK DIAGRAM



### CONNECTION DIAGRAM

### Top View



Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| AMBIENT TEMPERATURE | PACKAGE TYPE | POWER TYPE | ACCESS TIMES | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 650ns | 500ns | 400ns | 300ns | 250ns | 200ns |
| $0°C \leq T_A \leq +70°C$ | Molded DIP | Standard | AM9102PC | AM9102APC | AM9102BPC | AM9102CPC | AM9102DPC | Am9102EPC |
| | | Low | AM91L02PC | AM91L02APC | AM91L02BPC | AM91L02CPC | | |
| | Hermetic DIP | Standard | AM9102DC | AM9102ADC | AM9102BDC | AM9102CDC | AM9102DDC | Am9102EDC |
| | | Low | AM91L02DC | AM91L02ADC | AM91L02BDC | AM91L02CDC | AM91L01CDC | |
| −55°C to +125°C | Hermetic DIP | Standard | AM9102DM | AM9102ADM | AM9102BDM | AM9102CDM | AM9101CDM | |
| | | Low | AM91L02DM | AM91L02ADM | AM91L02BDM | AM91L02CDM | AM91L01CDM | |
| | Hermetic Flat Pack | Standard | AM9102FM | AM9102AFM | AM9102BFM | | | |
| | | Low | AM91L02FM | AM91L02AFM | AM91L02BFM | | | |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ With Respect to $V_{SS}$, Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs | −0.5 V to +7 V |
| DC Input Voltage | −0.5 V to +7 V |
| Power Dissipation | 1.0 W |

## ELECTRICAL CHARACTERISTICS over operating range

Am91L02PC, Am91L02DC     $T_A$ = 0°C to +70°C     $V_{CC}$ = +5.0V ±5%
Am9102PC, Am9102DC

| | | | | | Am9102/A/B<br>Am91L02/A/B | | Am9102C<br>Am9102D<br>Am9102E | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameters** | **Description** | **Test Conditions** | | | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −200µA | | | 2.4 | | 2.4 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 3.2mA | | | | 0.4 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | −0.5 | 0.8 | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $V_{IN}$ = 0V to 5.25V | | | | 10 | | 10 | µA |
| $I_{CC1}$ | Power Supply Current | All inputs = $V_{CC}$<br>Data out open<br>$V_{CC}$ = MAX. | $T_A$ = 25°C | Am91L02 | | 28 | | 31 | mA |
| | | | | Am9102 | | 45 | | 50 | |
| $I_{CC2}$ | | | $T_A$ = 0°C | Am91L02 | | 30 | | 33 | |
| | | | | Am9102 | | 50 | | 55 | |
| $I_{LO}$ | Output Leakage Current | $V_{\overline{CS}} = V_{IH}$ | $V_{OUT} = V_{CC}$ | | | 5.0 | | 5.0 | µA |
| | | | $V_{OUT}$ = 0.4V | | | −10 | | −10 | |

Am91L02DM, FM     $T_A$ = −55°C to +125°C     $V_{CC}$ = +5.0V ±10%
Am9102DM, FM

| | | | | | Am9102/A/B<br>Am91L02/A/B | | Am9102C<br>Am91L02C | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameters** | **Description** | **Test Conditions** | | | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −200µA | $V_{CC}$ = 4.75V | | 2.4 | | 2.4 | | Volts |
| | | | $V_{CC}$ = 4.50V | | 2.2 | | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 3.2mA | | | | 0.4 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | −0.5 | 0.8 | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $V_{IN}$ = 0V to 5.5V | | | | 10 | | 10 | µA |
| $I_{CC1}$ | Power Supply Current | All inputs = $V_{CC}$<br>Data out open<br>$V_{CC}$ = MAX. | $T_A$ = 25°C | Am91L02 | | 28 | | 31 | mA |
| | | | | Am9102 | | 45 | | 50 | |
| $I_{CC3}$ | | | $T_A$ = −55°C | Am91L02 | | 35 | | 37 | |
| | | | | Am9102 | | 55 | | 60 | |
| $I_{LO}$ | Output Leakage Current | $V_{\overline{CS}} = V_{IH}$ | $V_{OUT} = V_{CC}$ | | | 10 | | 10 | µA |
| | | | $V_{OUT}$ = 0.4V | | | −10 | | −10 | |

## CAPACITANCE ($T_A$ = 25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance, Any Input | $V_{IN}$ = 0 V, f = 1 MHz | | 3.0 | 5.0 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 V, f = 1 MHz | | 4.0 | 6.0 | pF |

## Am9102 FAMILY SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS

over operating temperature and voltage range

Load = 1 TTL gate and 100pF, $V_{IL}$ = 0.8V, $V_{IH}$ = 2.0V, $t_r$ = $t_f$ = 10ns. Output reference level 0.8V, 2.0V

**Read Cycle Characteristics**

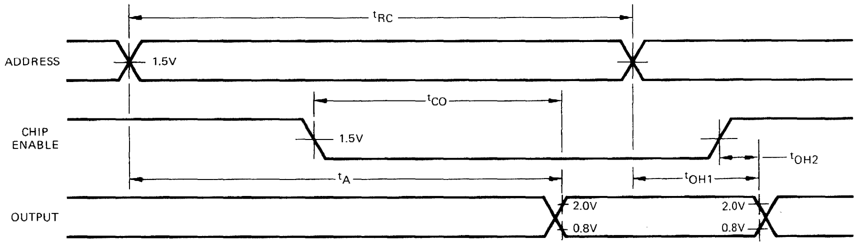
| | | Am9102<br>Am91L02 | | Am9102A<br>Am91L02A | | Am9102B<br>Am91L02B | | Am9102C<br>Am91L02C | | Am9102D | | Am9102E | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{RC}$ | Read Cycle Time | 650 | | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| $t_A$ | Access Time | | 650 | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| $t_{CO}$ | $\overline{CE}$ LOW to Output HIGH or LOW | | 200 | | 175 | | 150 | | 125 | | 100 | | 80 | ns |
| $t_{OH1}$ | Previous Read Data Valid with Respect to Chip Select | 50 | | 50 | | 50 | | 50 | | 40 | | 30 | | ns |
| $t_{OH2}$ | Previous Read Data Valid with Respect to Chip Select | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

**Write Cycle Requirements**

| | | Am9102<br>Am91L02 | | Am9102A<br>Am91L02A | | Am9102B<br>Am91L02B | | Am9102C<br>Am91L02C | | Am9102D | | Am9102E | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Units |
| $t_{WC}$ | Write Cycle Time | 650 | | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| $t_{AW}$ | Address Set-Up Time | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | ns |
| $t_{WP}$ | Write Pulse Width | 200 | | 175 | | 150 | | 125 | | 100 | | 80 | | ns |
| $t_{WR}$ | Write Recovery Time (Address Hold Time) | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DW}$ | Data Set-Up Time | 175 | | 150 | | 125 | | 100 | | 75 | | 60 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{CW}$ | Chip Enable Set-Up Time | 200 | | 175 | | 150 | | 125 | | 100 | | 85 | | ns |

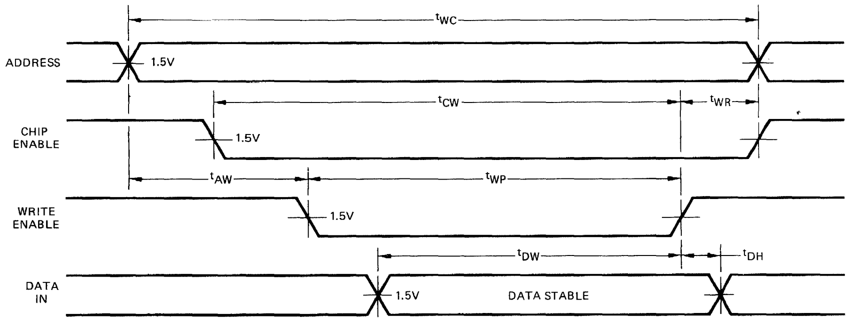
## SWITCHING WAVEFORMS

### READ CYCLE



tRC
ADDRESS
1.5V
tCO
CHIP ENABLE
1.5V
tOH2
tA
tOH1
OUTPUT
2.0V
0.8V
2.0V
0.8V

### WRITE CYCLE



tWC
ADDRESS
1.5V
tCW
tWR
CHIP ENABLE
1.5V
tAW
tWP
WRITE ENABLE
1.5V
tDW
tDH
DATA IN
1.5V
DATA STABLE

## POWER DOWN STANDBY OPERATION

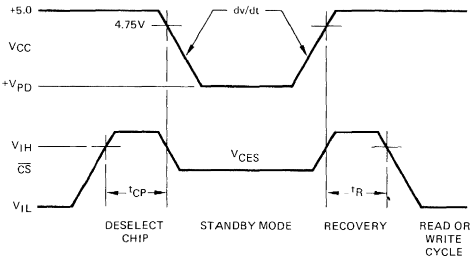
The Am9102 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated back-up power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power.

A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

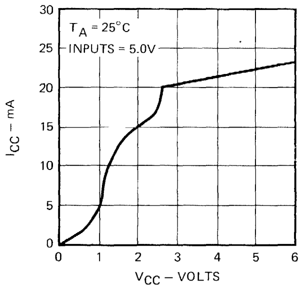
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be raised for the chip disable time ($t_{CP}$) prior to entering the standby mode, and should be held at $V_{PD}$ during the entire standby cycle.

## STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

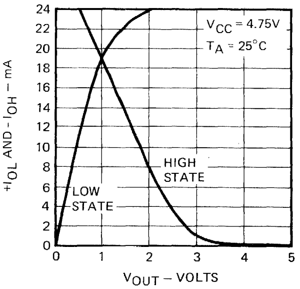
| Parameters | Description | Test Conditions | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A = 0°C$<br>All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L02 | | 10 | 23 | mA |
| | | | | Am9102 | | 12 | 28 | |
| | | | $V_{PD} = 2.0V$ | Am91L02 | | 12 | 28 | |
| | | | | Am9102 | | 15 | 38 | |
| | | $T_A = -55°C$<br>All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L02 | | 10 | 26 | mA |
| | | | | Am9102 | | 12 | 31 | |
| | | | $V_{PD} = 2.0V$ | Am91L02 | | 12 | 31 | |
| | | | | Am9102 | | 15 | 42 | |
| $dv/dt$ | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/μs |
| $t_R$ | Standby Recovery Time | | | | $T_{RC}$ | | | ns |
| $T_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |



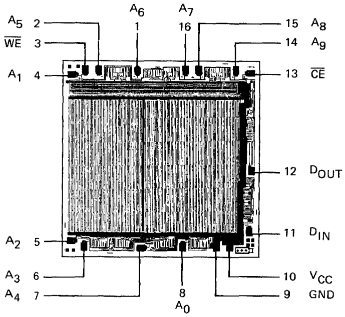
### Power Supply Current Versus Voltage



### Typical Output Current Versus Voltage

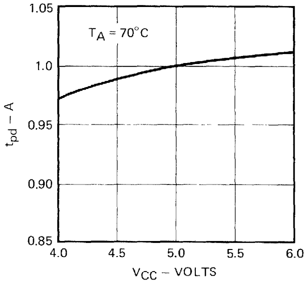


### Metallization and Pad Layout

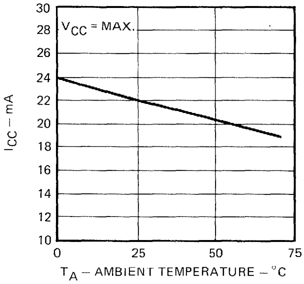


DIE SIZE 0.128" X 0.128"

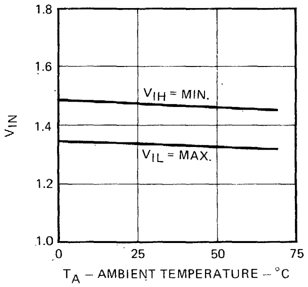
### Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ = +5.0 Volts



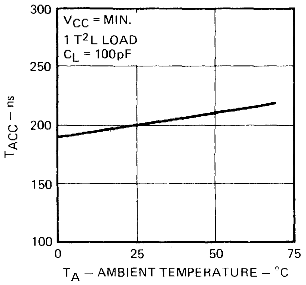
### Typical Power Supply Current Versus Ambient Temperature



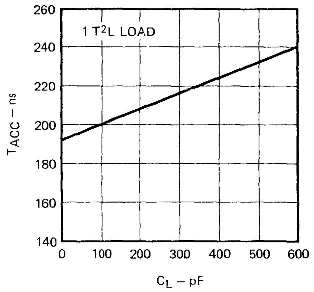
**Typical $V_{IN}$ Limits Versus Ambient Temperature**



**Typical $T_{ACC}$ Versus Ambient Temperature**



**Typical $T_{ACC}$ Versus $C_L$**



## DEFINITION OF TERMS

### FUNCTIONAL TERMS

**$\overline{CE}$** Active LOW chip enable. Data can be read from or written into the memory only if $\overline{CE}$ is LOW.

**$\overline{WE}$** Active LOW write enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drains are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

$t_{RC}$ Read Cycle Time. The minimum time required between successive address changes while reading.

$t_A$ Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

$t_{CO}$ Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

$t_{OH1}$ Minimum Access Time. Minimum time which will elapse between change of address and any change on the data output.

$t_{OH2}$ Minimum time which will elapse between a change on the chip enable and any change on the data output.

$t_{WC}$ Write Cycle Time. The minimum time required between successive address changes while writing.

$t_{AW}$ Address Set-Up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

$t_{WP}$ The minimum duration of a LOW level on the write enable guaranteed to write data.

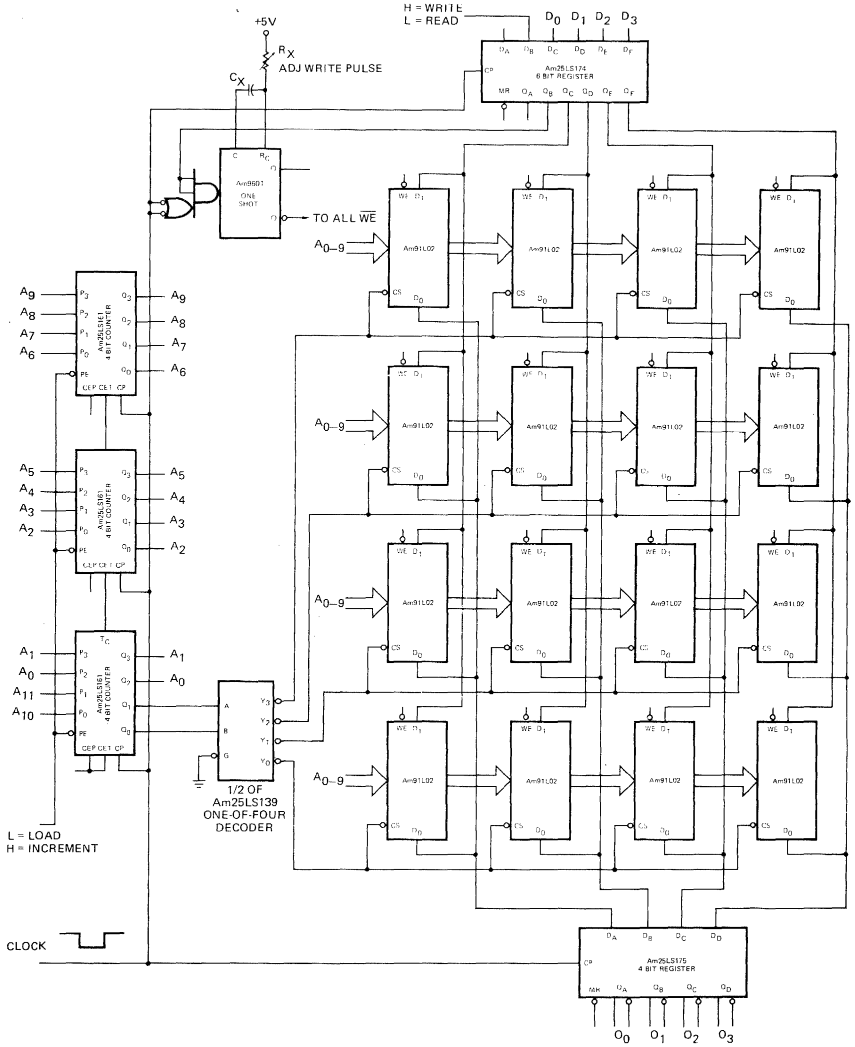
$t_{WR}$ Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

$t_{DW}$ Data Set-Up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

$t_{DH}$ Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

$t_{CW}$ Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

## APPLICATIONS


H = WRITE
L = READ
D0 D1 D2 D3
+5V
RX
ADJ WRITE PULSE
CX
Am25LS174 6 BIT REGISTER
Am9601 ONE SHOT
TO ALL WE
A0–9
Am91L02
WE D1
CS D0
A9 A8 A7 A6
Am25LS161 4 BIT COUNTER
A5 A4 A3 A2
A1 A0 A11 A10
PE
CEP CET CP
1/2 OF Am25LS139 ONE-OF-FOUR DECODER
L = LOAD
H = INCREMENT
CLOCK
Am25LS175 4 BIT REGISTER
O0 O1 O2 O3

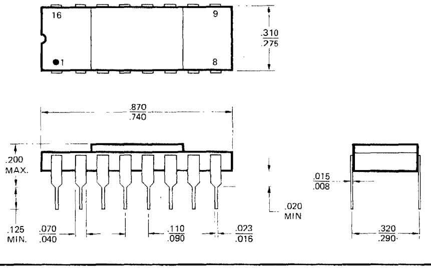
### 4K WORD BY 4-BIT MEMORY SYSTEM

The clock signal HIGH-to-LOW transition fires the one-shot and initiates the write pulse. The write pulse should end 100ns prior to the next clock LOW-to-HIGH transition. On each clock pulse, the data input register is loaded with four bits of data and a read/write bit and the address register is either loaded or incremented. Output data is loaded on the next clock pulse.

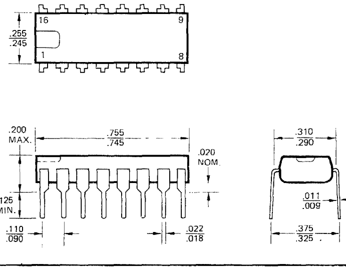
## PHYSICAL DIMENSIONS

### Dual-In-Line

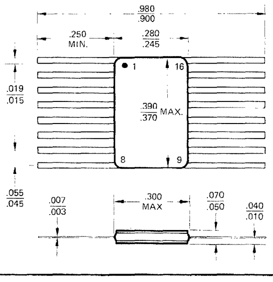
**Side-Brazed**


16
9
1
8
.310
.275
.870
.740
.200 MAX.
.125 MIN.
.070
.040
.110
.090
.023
.016
.020 MIN
.015
.008
.320
.290

**Molded**


16
9
1
8
.255
.245
.200 MAX.
.755
.745
.020 NOM.
.125 MIN.
.110
.090
.022
.018
.310
.290
.011
.009
.375
.325

**Flat Package**


.980
.900
.250 MIN.
.280
.245
1
16
.019
.015
.390
.370 MAX.
8
9
.055
.045
.007
.003
.300 MAX
.070
.050
.040
.010

# Am9111/Am91L11/Am2111 FAMILY

## 256x4 Static R/W Random Access Memories

| PART NUMBER | Am2111 | Am2111-2 | Am9111A<br>Am91L11A<br>Am2111-1 | Am9111B<br>Am91L11B | Am9111C<br>Am91L11C | Am9111D | AM9111E |
|---|---|---|---|---|---|---|---|
| ACCESS TIME | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns | 200ns |

## DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization for small memory systems
- Low operating power dissipation
  125mW Typ; 290mW maximum – standard power
  100mW Typ; 175mW maximum – low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive – two full TTL loads
- High noise immunity – full 400mV
- Single 5 volt power supply – tolerances: ±5% commercial, ±10% military
- Uniform switching characteristics – access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Bussed input and output data on common pins.
- Output disable control
- Zero address set-up and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

## FUNCTIONAL DESCRIPTION

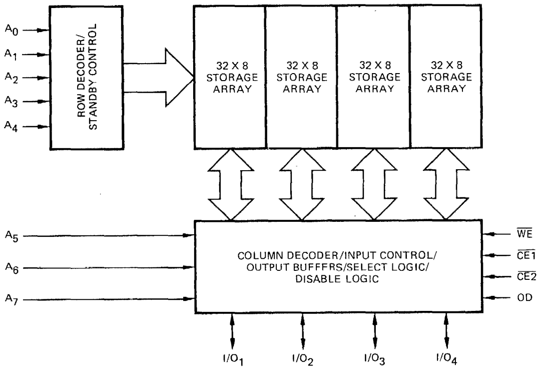
The Am9111/Am91L11 series of devices are high performance, low power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth. The input data and output data signals are bussed together to share common I/O pins. This feature not only decreases the package size, but helps eliminate external logic in bus-oriented memory systems.

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L11 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

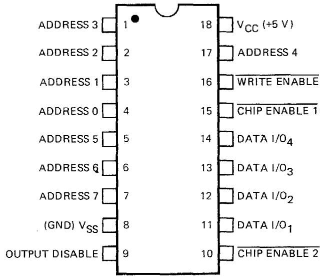
The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are all fully static and no refresh operations or sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

## Am9111 BLOCK DIAGRAM


$A_0$
$A_1$
$A_2$
$A_3$
$A_4$
ROW DECODER/ STANDBY CONTROL
32 X 8 STORAGE ARRAY
32 X 8 STORAGE ARRAY
32 X 8 STORAGE ARRAY
32 X 8 STORAGE ARRAY
$A_5$
$A_6$
$A_7$
COLUMN DECODER/INPUT CONTROL/ OUTPUT BUFFFRS/SELECT LOGIC/ DISABLE LOGIC
WE
CE1
CE2
OD
$I/O_1$
$I/O_2$
$I/O_3$
$I/O_4$

## CONNECTION DIAGRAM
### Top View


ADDRESS 3 1
ADDRESS 2 2
ADDRESS 1 3
ADDRESS 0 4
ADDRESS 5 5
ADDRESS 6 6
ADDRESS 7 7
(GND) $V_{SS}$ 8
OUTPUT DISABLE 9
18 $V_{CC}$ (+5 V)
17 ADDRESS 4
16 WRITE ENABLE
15 CHIP ENABLE 1
14 DATA $I/O_4$
13 DATA $I/O_3$
12 DATA $I/O_2$
11 DATA $I/O_1$
10 CHIP ENABLE 2

Note: Flat Pack version available in 24-pin package.

## ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Power Type | Access Times | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns | 200ns |
| 0°C to +70°C | Molded DIP | Standard | P2111 | P2111-2 | P2111-1<br>AM9111APC | AM9111BPC | AM9111CPC | AM9111DPC | AM9111EPC |
| | | Low | | | AM91L11APC | AM91L11BPC | AM91L11CPC | | |
| | Hermetic DIP | Standard | C2111 | C2111-2 | C2111-1<br>AM9111ADC | AM9111BDC | AM9111CDC | AM9111DDC | AM9111EDC |
| | | Low | | | AM91L11ADC | AM91L11BDC | AM91L11CDC | | |
| −55°C to +125°C | Hermetic DIP | Standard | | | AM9111ADM | AM9111BDM | AM9111CDM | | |
| | | Low | | | AM91L11ADM | AM91L11BDM | AM91L11CDM | | |
| | Hermetic Flat Pack | Standard | | | AM9111AFM | AM9111BFM | | | |
| | | Low | | | AM91L11AFM | AM91L11BFM | | | |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ With Respect to $V_{SS}$, Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

## ELECTRICAL CHARACTERISTICS

Am9111PC, Am9111DC $T_A = 0°C$ to $+70°C$
Am91L11PC, Am91L11DC $V_{CC} = +5.0V \pm 5\%$
Am2111

| Parameters | Description | Test Conditions | | | Am9111/ Am91L11 Family | | Am2111 Family | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN. | | $I_{OH} = -200\mu A$ | 2.4 | | | | Volts |
| | | | | $I_{OH} = -150\mu A$ | | | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN. | | $I_{OL} = 3.2mA$ | | 0.4 | | | Volts |
| | | | | $I_{OL} = 2.0mA$ | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | 2.2 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | −0.5 | 0.65 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leq V_{IN} \leq 5.25V$ | | | | 10 | | 10 | μA |
| $I_{LO}$ | I/O Leakage Current | $V_{\overline{CE}} = V_{IH}$ | | $V_{OUT} = V_{CC}$ | | 5.0 | | 15 | μA |
| | | | | $V_{OUT} = 0.4V$ | | −10 | | −50 | |
| $I_{CC1}$ | Power Supply Current | Data out open<br>$V_{CC}$ = Max.<br>$V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9111A/B | | 50 | | 60 | mA |
| | | | | Am9111C/D/E | | 55 | | | |
| | | | | Am91L11A/B | | 31 | | | |
| | | | | Am91L11C | | 34 | | | |
| $I_{CC2}$ | | | $T_A = 0°C$ | Am9111A/B | | 55 | | 70 | |
| | | | | Am9111C/D/E | | 60 | | | |
| | | | | Am91L11A/B | | 33 | | | |
| | | | | Am91L11C | | 36 | | | |

## ELECTRICAL CHARACTERISTICS

Am9111DM, Am9111FM $T_A = -55°C$ to $+125°C$
Am91L11DM, Am91L11FM $V_{CC} = +5.0V \pm 10\%$

| Parameters | Description | Test Conditions | | | Am9111/ Am91L11 Family | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | | $V_{CC} = 4.75V$ | 2.4 | | Volts |
| | | | | $V_{CC} = 4.5V$ | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leq V_{IN} \leq 5.5V$ | | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{\overline{CE}} = V_{IH}$ | | $V_{OUT} = V_{CC}$ | | 10 | μA |
| | | | | $V_{OUT} = 0.4V$ | | −10 | |
| $I_{CC1}$ | Power Supply Current | Data out open<br>$V_{CC}$ = Max.<br>$V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9111A/Am9111B | | 50 | mA |
| | | | | Am9111C | | 55 | |
| | | | | Am91L11A/Am91L11B | | 31 | |
| | | | | Am91L11C | | 34 | |
| $I_{CC3}$ | | | $T_A = -55°C$ | Am9111A/Am9111B | | 60 | |
| | | | | Am9111C | | 65 | |
| | | | | Am91L11A/Am91L11B | | 37 | |
| | | | | Am91L11C | | 40 | |

## CAPACITANCE

| Parameters | Description | Test Conditions | | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance, $V_{IN} = 0V$ | $T_A = 25°C$, f = 1 mHz | Am2111 | 4.0 | 8.0 | pF |
| | | | Am9111/Am91L11 | 3.0 | 6.0 | |
| $C_{OUT}$ | Output Capacitance, $V_{OUT} = 0V$ | | Am2111 | 10 | 15 | pF |
| | | | Am9111/Am91L11 | 8.0 | 11 | |

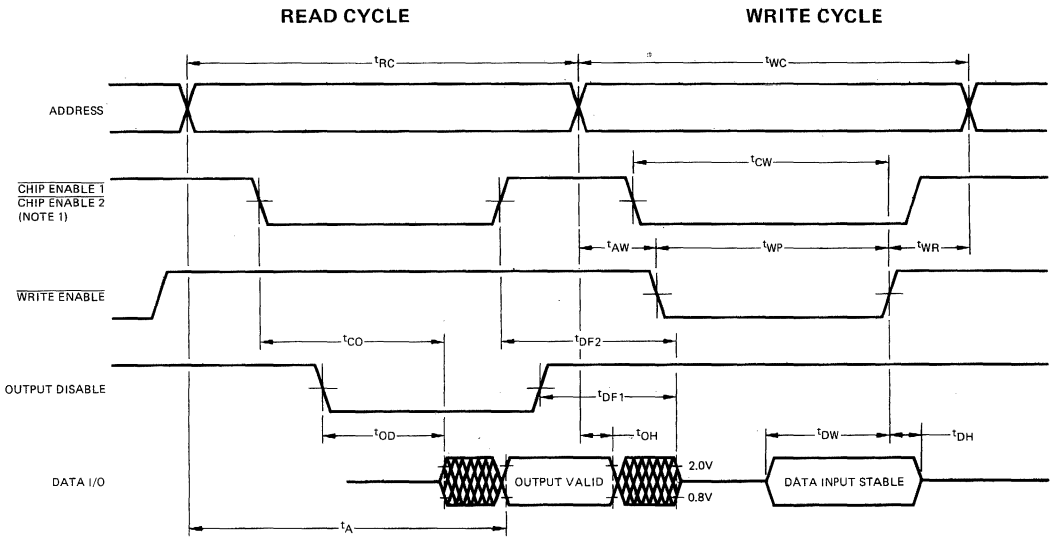
## SWITCHING CHARACTERISTICS over operating and voltage range

Output Load = 1 TTL Gate +100pF — $T_A$ = 0°C to +70°C — $V_{CC}$ = +5V ±5%
Transition Times = 10ns — $T_A$ = −55°C to +125°C — $V_{CC}$ = +5V ±10%
Input Levels, Output References = 0.8V and 2.0V

| Parameters | Description | 2111 | | 2111-2 | | 2111-1 | | 9111A<br>91L11A | | 9111B<br>91L11B | | 9111C<br>91L11C | | 9111D | | 9111E | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| $t_A$ | Access Time | | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| $t_{CO}$ | Chip Enable to Output ON Delay (Note 1) | | 800 | | 400 | | 350 | | 200 | | 175 | | 150 | | 125 | | 100 | ns |
| $t_{OD}$ | Output Disable to Output ON Delay | | 700 | | 350 | | 300 | | 175 | | 150 | | 125 | | 100 | | 85 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 0 | | 0 | | 0 | | 40 | | 40 | | 40 | | 30 | | 30 | | ns |
| $t_{DF1}$ | Output Disable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | 5.0 | 125 | 5.0 | 100 | 5.0 | 100 | 5.0 | 75 | 5.0 | 60 | ns |
| $t_{DF2}$ | Chip Enable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | 10 | 150 | 10 | 125 | 10 | 125 | 10 | 100 | 10 | 80 | ns |
| $t_{WC}$ | Write Cycle Time | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| $t_{AW}$ | Address Set-up Time | 150 | | 150 | | 100 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 750 | | 400 | | 300 | | 175 | | 150 | | 125 | | 100 | | 85 | | ns |
| $t_{CW}$ | Chip Enable Set-up Time (Note 1) | 900 | | 550 | | 400 | | 175 | | 150 | | 125 | | 100 | | 85 | | ns |
| $t_{WR}$ | Address Hold Time | 50 | | 50 | | 50 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DW}$ | Input Data Set-up Time | 700 | | 400 | | 280 | | 150 | | 125 | | 100 | | 85 | | 65 | | ns |
| $t_{DH}$ | Input Data Hold Time | 100 | | 100 | | 100 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

Notes: 1. Both $\overline{CE1}$ and $\overline{CE2}$ must be LOW to enable the chip.

## SWITCHING WAVEFORMS


READ CYCLE
WRITE CYCLE
tRC
tWC
ADDRESS
tCW
CHIP ENABLE 1
CHIP ENABLE 2
(NOTE 1)
tAW
tWP
tWR
WRITE ENABLE
tCO
tDF2
OUTPUT DISABLE
tDF1
tOD
tOH
tDW
tDH
DATA I/O
OUTPUT VALID
2.0V
0.8V
DATA INPUT STABLE
tA

## DEFINITION OF TERMS

### FUNCTIONAL TERMS

**$\overline{CE1}$, $\overline{CE2}$** Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ and $\overline{CE2}$ are LOW.

**$\overline{WE}$** Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if WE is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

**$t_{OD}$** Output enable time. Delay time from falling edge of OD to output on.

**$t_{RC}$** Read Cycle Time. The minimum time required between successive address changes while reading.

**$t_{A}$** Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

**$t_{CO}$** Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

**$t_{OH}$** Minimum time which will elapse between change of address and any change of the data output.

**$t_{DF1}$** Time delay between output disable HIGH and output data float.

**$t_{DF2}$** Time delay between chip enable OFF and output data float.

**$t_{WC}$** Write Cycle Time. The minimum time required between successive address changes while writing.

**$t_{AW}$** Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

**$t_{WP}$** The minimum duration of a LOW level on the write enable guaranteed to write data.

**$t_{WR}$** Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

**$t_{DW}$** Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

**$t_{DH}$** Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

**$t_{CW}$** Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

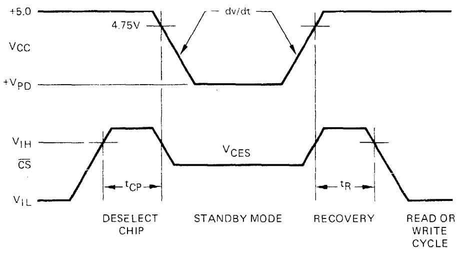
### POWER DOWN STANDBY OPERATION

The Am9111/Am91L11 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

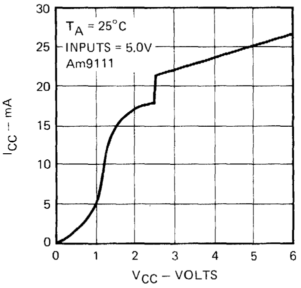
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at $V_{IH}$ or $V_{CES}$ during the entire standby cycle.

## STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

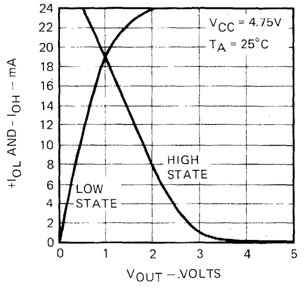
| Parameters | Description | Test Conditions | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A = 0°C$<br>All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L11 | | 11 | 25 | mA |
| | | | | Am9111 | | 13 | 31 | |
| | | | $V_{PD} = 2.0V$ | Am91L11 | | 13 | 31 | |
| | | | | Am9111 | | 17 | 41 | |
| | | $T_A = -55°C$<br>All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L11 | | 11 | 28 | mA |
| | | | | Am9111 | | 13 | 34 | |
| | | | $V_{PD} = 2.0V$ | Am91L11 | | 13 | 34 | |
| | | | | Am9111 | | 17 | 46 | |
| dv/dt | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/µs |
| $t_R$ | Standby Recovery Time | | | | $t_{RC}$ | | | ns |
| $t_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |


+5.0
4.75V
dv/dt
VCC
+VPD
VIH
CS
VCES
VIL
tCP
tR
DESELECT CHIP
STANDBY MODE
RECOVERY
READ OR WRITE CYCLE

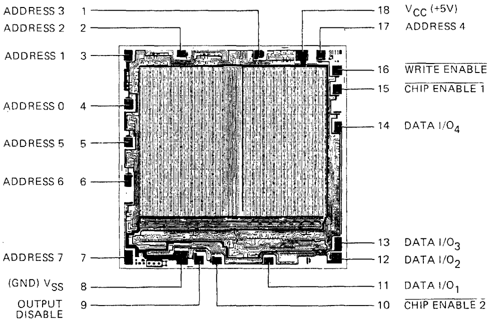
Typical Power Supply Current Versus Voltage



Typical Output Current Versus Voltage



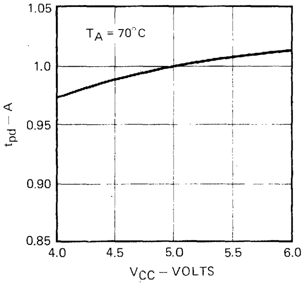
Metallization and Pad Layout


ADDRESS 3 1
ADDRESS 2 2
ADDRESS 1 3
ADDRESS 0 4
ADDRESS 5 5
ADDRESS 6 6
ADDRESS 7 7
(GND) VSS 8
OUTPUT DISABLE 9
18 VCC (+5V)
17 ADDRESS 4
16 WRITE ENABLE
15 CHIP ENABLE 1
14 DATA I/O4
13 DATA I/O3
12 DATA I/O2
11 DATA I/O1
10 CHIP ENABLE 2

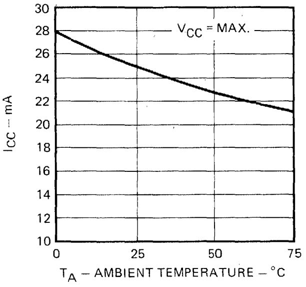
DIE SIZE: 0.132" X 0.131"

(Pin numbers shown are for DIP versions only)

Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ = +5.0 Volts



Typical Power Supply Current Versus Ambient Temperature



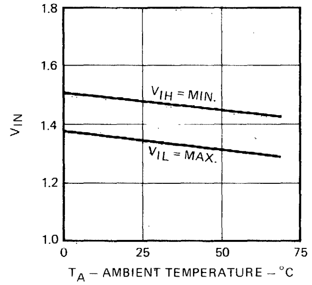
## Am9111 FAMILY – APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9111 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

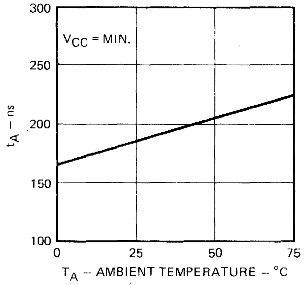
This bussed I/O approach cuts down the package pin count allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9111 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

The Output Disable control signal is provided to prevent signal contention for the bus lines, and to simplify tri-state bus control in the external circuitry. If the chip is enabled and the output is enabled and the memory is in the Read state, then the output buffers will be impressing data on the bus lines. At that point, if the external system tries to drive the bus with data, in preparation for a write operation, there will be conflict for domination of the bus lines. The Output Disable signal allows the user direct control over the output buffers, independent of the state of the memory. Although there are alternative ways to resolve the conflict, normally Output Disable will be held high during a write operation.

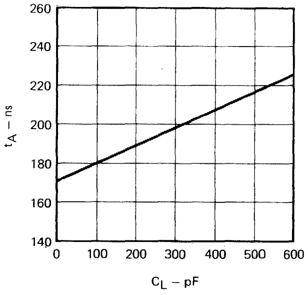
**Typical $V_{IN}$ Limits Versus Ambient Temperature**



**Typical $t_A$ Versus Ambient Temperature**



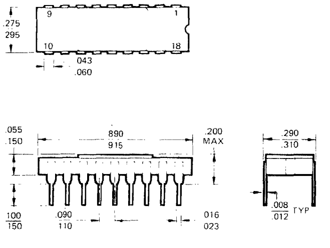
**Typical $t_A$ Versus $C_L$**



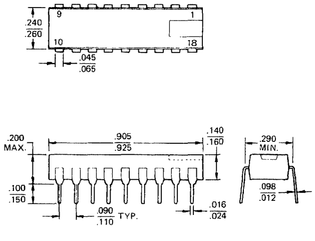
## PHYSICAL DIMENSIONS

### Dual-In-Line

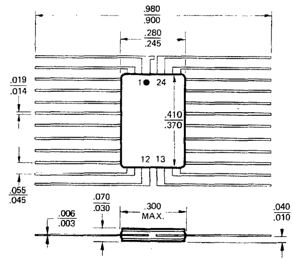
**18-Pin Side Brazed**


9
1
10
18
.275
.295
.043
.060
.055
.150
.890
.915
.200
MAX
.100
.150
.090
.110
.016
.023
.290
.310
.008
.012
TYP

**18-Pin Molded**


9
1
10
18
.240
.260
.045
.065
.200
MAX.
.905
.925
.140
.160
.100
.150
.090
.110
TYP.
.016
.024
.290
MIN.
.098
.012

**24-Pin Flat Package**


.980
.900
.280
.245
.019
.014
1
24
.410
.370
12
13
.055
.045
.070
.030
.006
.003
.300
MAX.
.040
.010

# Am9112/Am91L12 FAMILY

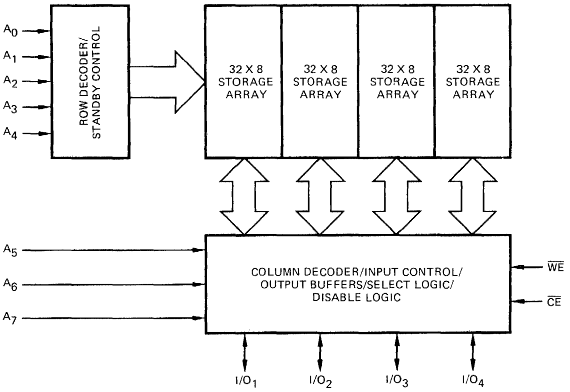
## 256x4 Static R/W Random Access Memories

| Part Number | Am2112 | Am2112-2 | Am9112A<br>Am91L12A | Am9112B<br>Am91L12B | Am9112C<br>Am91L12C | Am9112D | AM9112E |
|---|---|---|---|---|---|---|---|
| Access Time | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns | 200ns |

### Distinctive Characteristics

- 256 x 4 organization
- 16-pin standard DIP
- Low operating power dissipation
  - 125mW Typ; 290mW maximum – standard power
  - 100mW Typ; 175mW maximum – low power
- DC standby mode reduces power up to 84%
  - 20mW Typ; 47mW maximum
- Logic voltage levels identical to TTL
- High output drive – two full TTL loads guaranteed
- High noise immunity – full 400mV
- Uniform switching characteristics – access times insensitive to supply variations, address patterns and data patterns.
- Single +5V power supply – tolerances ±5% commercial, ±10% military
- Bus oriented I/O data
- Zero address, set-up, and hold times guaranteed for simpler timing
- Direct plug-in replacement for 2112 type devices
- 100% MIL-STD-883 reliability assurance testing

### Am9112 BLOCK DIAGRAM


A0
A1
A2
A3
A4
ROW DECODER/ STANDBY CONTROL
32 X 8 STORAGE ARRAY
32 X 8 STORAGE ARRAY
32 X 8 STORAGE ARRAY
32 X 8 STORAGE ARRAY
A5
A6
A7
COLUMN DECODER/INPUT CONTROL/ OUTPUT BUFFERS/SELECT LOGIC/ DISABLE LOGIC
WE
CE
I/O1
I/O2
I/O3
I/O4

### FUNCTIONAL DESCRIPTION

The Am9112/Am91L12 series of products are high performance, low power, 1024-bit, static read/write random access memories. They offer a range of speeds and power dissipations including versions as fast as 200ns and as low as 100mW typical.

Each memory is implemented as 256 words by 4-bits per word. This organization allows efficient design of small memory systems and permits finer resolution of incremental memory word size relative to 1024 by 1 devices. The output and input data signals are internally bussed together and share 4 common I/O pins. This feature keeps the package size small and provides a simplified interface to bus-oriented systems.

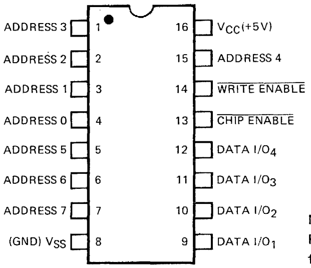
The Am9112/Am91L12 memories may be operated in a DC standby mode for reductions of as much as 84% of the normal operating power dissipation. Though the memory cannot be operated, data can be retained in the storage cells with a power supply as low as 1.5 volts. The Am91L12 versions offer reduced power during normal operating conditions as well as even lower dissipation in standby mode.

The eight Address inputs are decoded to select 1-of-256 locations within the memory. The Chip Enable input acts as a high-order address in multiple chip systems. It also controls the write amplifier and the output buffers in conjunction with the Write Enable input. When $\overline{CE}$ is low and $\overline{WE}$ is high, the write amplifiers are disabled, the output buffers are enabled and the memory will execute a read cycle. When $\overline{CE}$ is low and $\overline{WE}$ is low, the write amplifiers are enabled, the output buffers are disabled and the memory will execute a write cycle. When $\overline{CE}$ is high both the write amplifiers and the output buffers are disabled.

These memories are fully static and require no refresh operations or sense amplifiers or clocks. All input and output voltage levels are identical to standard TTL specifications, including the power supply.

### CONNECTION DIAGRAM

### Top View


ADDRESS 3 1
ADDRESS 2 2
ADDRESS 1 3
ADDRESS 0 4
ADDRESS 5 5
ADDRESS 6 6
ADDRESS 7 7
(GND) VSS 8
16 VCC(+5V)
15 ADDRESS 4
14 WRITE ENABLE
13 CHIP ENABLE
12 DATA I/O4
11 DATA I/O3
10 DATA I/O2
9 DATA I/O1

Note:
Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Power Type | Access Time | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns | 200ns |
| 0°C to +70°C | Molded DIP | Standard | P2112 | P2112-2 | AM9112APC | AM9112BPC | AM9112CPC | AM9112DPC | AM9112EPC |
| | | Low | | | AM91L12APC | AM91L12BPC | AM91L12CPC | | |
| | Hermetic DIP | Standard | C2112 | C2112-2 | AM9112ADC | AM9112BDC | AM9112CDC | AM9112DDC | AM9112EDC |
| | | Low | | | AM91L12ADC | AM91L12BDC | AM91L12CDC | | |
| −55°C to +125°C | Hermetic DIP | Standard | | | AM9112ADM | AM9112BDM | AM9112CDM | | |
| | | Low | | | AM91L12ADM | AM91L12BDM | AM91L12CDM | | |
| | Hermetic Flat Pack | Standard | | | AM9112AFM | AM9112BFM | | | |
| | | Low | | | AM91L12AFM | AM91L12BFM | | | |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ With Respect to $V_{SS}$, Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

## ELECTRICAL CHARACTERISTICS

Am9112PC, Am9112DC $T_A = 0°C$ to $+70°C$
Am91L12PC, Am91L12DC $V_{CC} = +5V \pm 5\%$

| Parameters | Description | Test Conditions | | | Am9112/ Am91L12 Family Min. | Am9112/ Am91L12 Family Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -200\mu A$ | | | 2.4 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leqslant V_{IN} \leqslant 5.25V$ | | | | 10 | µA |
| $I_{LO}$ | I/O Leakage Current | $V_{\overline{CE}} = V_{IH}$ | $V_{OUT} = V_{CC}$ | | | 5.0 | µA |
| | | | $V_{OUT} = 0.4V$ | | | −10 | |
| $I_{CC1}$ | Power Supply Current | Data out open<br>$V_{CC}$ = MAX.<br>$V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9112A/B | | 50 | mA |
| | | | | Am9112C/D/E | | 55 | |
| | | | | Am91L12A/B | | 31 | |
| | | | | Am91L12C | | 34 | |
| $I_{CC2}$ | | | $T_A = 0°C$ | Am9112A/B | | 55 | |
| | | | | Am9112C/D/E | | 60 | |
| | | | | Am91L12A/B | | 33 | |
| | | | | Am91L12C | | 36 | |

## ELECTRICAL CHARACTERISTICS

Am9112DM, Am9112FM $T_A = -55°C$ to $+125°C$
Am91L12DM, Am91L12FM $V_{CC} = +5.0V \pm 10\%$

| Parameters | Description | Test Conditions | | | Am9112/ Am91L12 Family Min. | Am9112/ Am91L12 Family Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | $V_{CC} = 4.75V$ | | 2.4 | | Volts |
| | | | $V_{CC} = 4.50V$ | | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leqslant V_{IN} \leqslant 5.5V$ | | | | 10 | µA |
| $I_{LO}$ | I/O Leakage Current | $V_{\overline{CE}} = V_{IH}$ | $V_{OUT} = V_{CC}$ | | | 10 | µA |
| | | | $V_{OUT} = 0.4V$ | | | −10 | |
| $I_{CC1}$ | Power Supply Current | Data out open<br>$V_{CC}$ = MAX.<br>$V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9112A/B | | 50 | mA |
| | | | | Am9112C | | 55 | |
| | | | | Am91L12A/B | | 31 | |
| | | | | Am91L12C | | 34 | |
| $I_{CC3}$ | | | $T_A = -55°C$ | Am9112A/B | | 60 | |
| | | | | Am9112C | | 65 | |
| | | | | Am91L12A/B | | 37 | |
| | | | | Am91L12C | | 40 | |

## CAPACITANCE

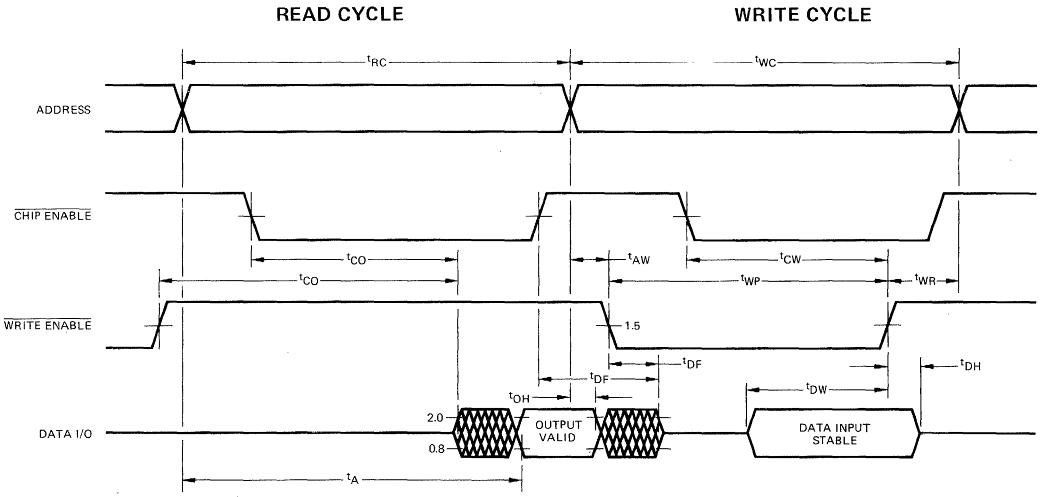
| Parameters | Description | Test Conditions | | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance, $V_{IN} = 0V$ | $T_A = 25°C$, f = 1 mHz | Am2112 | 4.0 | 8.0 | pF |
| | | | Am9112/Am91L12 | 3.0 | 6.0 | |
| $C_{OUT}$ | Output Capacitance, $V_{OUT} = 0V$ | | Am2112 | 10 | 18 | pF |
| | | | Am9112/Am91L12 | 8.0 | 11 | |

## SWITCHING CHARACTERISTICS over operating temperature and voltage range

Output Load = 1 TTL Gate +100pF
Transition Times = 10ns
Input Levels, Output References = 0.8V and 2.0V

| Parameters | Description | Am9112A<br>Am91L12A | | Am9112B<br>Am91L12B | | Am9112C<br>Am91L12C | | Am9112D | | Am9112E | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| $t_A$ | Access Time | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| $t_{CO}$ | Output Enabled to Output ON Delay (Note 1) | 5.0 | 175 | 5.0 | 150 | 5.0 | 125 | 5.0 | 100 | 5.0 | 85 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 40 | | 40 | | 40 | | 30 | | 30 | | ns |
| $t_{DF}$ | Output Disabled to Output OFF Delay (Note 2) | 5.0 | 125 | 5.0 | 100 | 5.0 | 100 | 5.0 | 75 | 5.0 | 60 | ns |
| $t_{WC}$ | Write Cycle Time | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| $t_{AW}$ | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WR}$ | Address Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width (Note 3) | 175 | | 150 | | 125 | | 100 | | 85 | | ns |
| $t_{CW}$ | Chip Enable Set-up Time | 175 | | 150 | | 125 | | 100 | | 85 | | ns |
| $t_{DW}$ | Input Data Set-up Time | 150 | | 125 | | 100 | | 85 | | 65 | | ns |
| $t_{DH}$ | Input Data Hold Time (Note 4) | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

## SWITCHING WAVEFORMS (Note 5)



Notes:
1. Output is enabled and $t_{CO}$ commences only with both $\overline{CE}$ LOW and $\overline{WE}$ HIGH.
2. Output is disabled and $t_{DF}$ defined from either the rising edge of $\overline{CE}$ or the falling edge of $\overline{WE}$.
3. Minimum $t_{WP}$ is valid when $\overline{CE}$ has been HIGH at least $t_{DF}$ before $\overline{WE}$ goes LOW. Otherwise $t_{WP(min.)} = t_{DW(min.)} + t_{DF(max.)}$.
4. When $\overline{WE}$ goes HIGH at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still LOW. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.
5. See "Application Information" section of this specification.

## DEFINITION OF TERMS

### FUNCTIONAL TERMS

**$\overline{\text{CE}}$** Active LOW Chip Enable. Data can be read from or written into the memory only if $\overline{\text{CE}}$ is LOW.

**$\overline{\text{WE}}$** Active LOW Write Enable. Data is written into the memory if $\overline{\text{WE}}$ is LOW and read from the memory if $\overline{\text{WE}}$ is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

**$t_{RC}$** Read Cycle Time. The minimum time required between successive address changes while reading.

**$t_A$** Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

**$t_{CO}$** Output Enable Time. The time during which $\overline{\text{CE}}$ must be LOW and $\overline{\text{WE}}$ must be HIGH prior to data on the output.

**$t_{OH}$** Minimum time which will elapse between change of address and any change on the data output.

**$t_{DF}$** Time which will elapse between a change on the chip enable or the right enable and on data outputs being driven to a floating status.

**$t_{WC}$** Write Cycle Time. The minimum time required between successive address changes while writing.

**$t_{AW}$** Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

**$t_{WP}$** The minimum duration of a LOW level on the write enable guaranteed to write data.

**$t_{WR}$** Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

**$t_{DW}$** Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

**$t_{DH}$** Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

**$t_{CW}$** Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

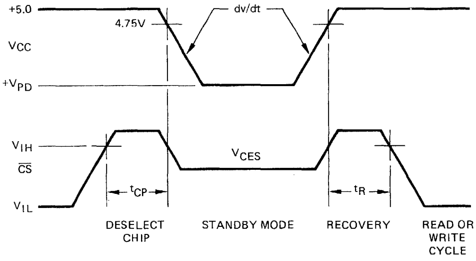
## POWER DOWN STANDBY OPERATION

The Am9112/Am91L12 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at $V_{IH}$ or $V_{CES}$ during the entire standby cycle.

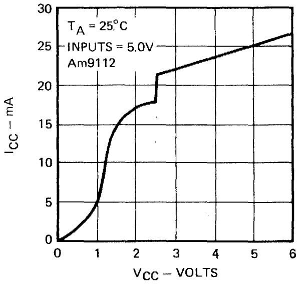
## STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

| Parameters | Description | Test Conditions | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A = 0°C$<br>All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L12 | | 11 | 25 | mA |
| | | | | Am9112 | | 13 | 31 | |
| | | | $V_{PD} = 2.0V$ | Am91L12 | | 13 | 31 | |
| | | | | Am9112 | | 17 | 41 | |
| | | $T_A = -55°C$<br>All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L12 | | 11 | 28 | mA |
| | | | | Am9112 | | 13 | 34 | |
| | | | $V_{PD} = 2.0V$ | Am91L12 | | 13 | 34 | |
| | | | | Am9112 | | 17 | 46 | |
| dv/dt | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/μs |
| $t_R$ | Standby Recovery Time | | | | $t_{RC}$ | | | ns |
| $t_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |

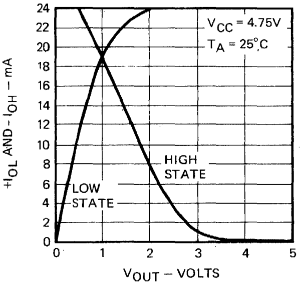


+5.0
VCC
+VPD
4.75V
dv/dt
VIH
$\overline{CS}$
VIL
VCES
tCP
tR
DESELECT CHIP
STANDBY MODE
RECOVERY
READ OR WRITE CYCLE

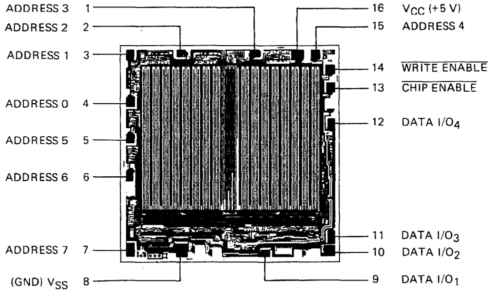
**Typical Power Supply Current Versus Voltage**



**Typical Output Current Versus Voltage**



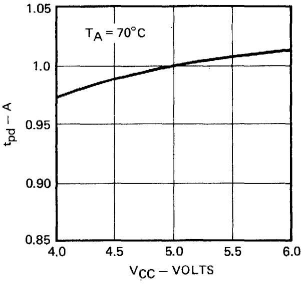
**Metallization and Pad Layout**



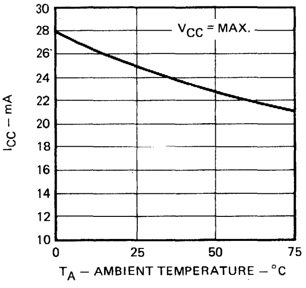
ADDRESS 3 1
ADDRESS 2 2
ADDRESS 1 3
ADDRESS 0 4
ADDRESS 5 5
ADDRESS 6 6
ADDRESS 7 7
(GND) VSS 8
16 VCC (+5 V)
15 ADDRESS 4
14 $\overline{WRITE ENABLE}$
13 $\overline{CHIP ENABLE}$
12 DATA I/O4
11 DATA I/O3
10 DATA I/O2
9 DATA I/O1

DIE SIZE 0.132" X 0.131"

**Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ = +5.0 Volts**



**Typical Power Supply Current Versus Ambient Temperature**



## APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9112 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

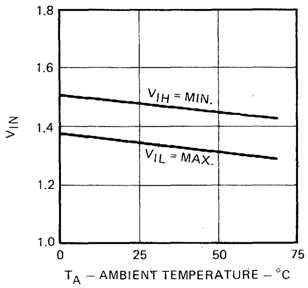
This bussed I/O approach keeps the package pin count low allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9112 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

If the chip is enabled ($\overline{CE}$ low) and the memory is in the Read state ($\overline{WE}$ high), the output buffers will be turned on and will be driving data on the I/O bus lines. If the external system tries to drive the bus with data, there may be contention for control of the data lines and large current surges can result. Since the condition can occur at the beginning of a write cycle, it is important that incoming data to be written not be entered until the output buffers have been turned off.

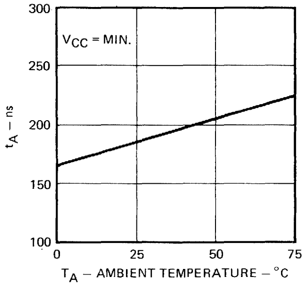
These operational suggestions for write cycles may be of some help for memory system designs:

1. For systems where $\overline{CE}$ is always low or is derived directly from addresses and so is low for the whole cycle, make sure $t_{WP}$ is at least $t_{DW}$ + $t_{DF}$ and delay the input data until $t_{DF}$ following the falling edge of $\overline{WE}$. With zero address set-up and hold times it will often be convenient to make $\overline{WE}$ a cycle-width level ($t_{WP} = t_{WC}$) so that the only subcycle timing required is the delay of the input data.
2. For systems where $\overline{CE}$ is high for at least $t_{DF}$ preceeding the falling edge of $\overline{WE}$, $t_{WP}$ may assume the minimum specified value. When $\overline{CE}$ is high for $t_{DF}$ before the start of the cycle, then no other subcycle timing is required and $\overline{WE}$ and data-in may be cycle-width levels.
3. Notice that because both $\overline{CE}$ and $\overline{WE}$ must be low to cause a write to take place, either signal can be used to determine the effective write pulse. Thus, $\overline{WE}$ could be a level with $\overline{CE}$ becoming the write timing signal. In such a case, the data set-up and hold times are specified with respect to the rising edge of $\overline{CE}$. The value of the data set-up time remains the same and the value of the data hold time should change to a minimum of 25ns.

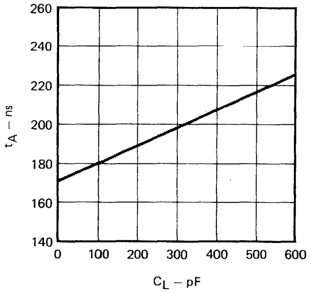
**Typical $V_{IN}$ Limits Versus Ambient Temperature**



**Typical $t_A$ Versus Ambient Temperature**



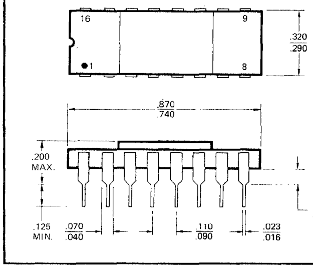
**Typical $t_A$ Versus $C_L$**



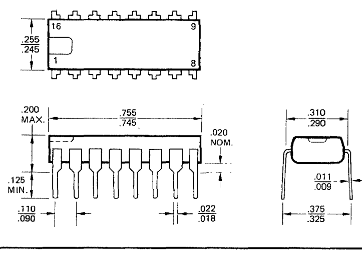
## PHYSICAL DIMENSIONS

### Dual-In-Line

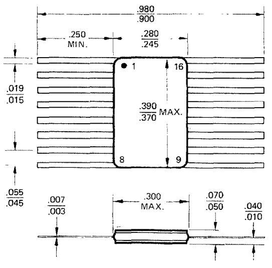
**16-Pin Side Brazed**



**16-Pin Molded**



**16-Pin Flat Package**



# Am9130

## 1024 x 4 Static R/W Random Access Memory

### DISTINCTIVE CHARACTERISTICS

- 1k x 4 organization
- Fully static data storage – no refreshing
- Single +5V power supply
- High-speed – access times down to 200ns max.
- **Low-power – 578mW max. – 350mW typ.**
- Interface logic levels identical to TTL
- High noise immunity – 400mV worst case
- High output drive – two standard TTL loads
- Bidirectional data bus – easier system interface
- Dual output controls – flexible bus operations
- Address and data registers on-chip
- Constant power drain – no large surges
- Unique Memory Status signal
  - –improves performance
  - –simplifies timing
- **DC standby mode – reduces power by > 80%**
- MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

### FUNCTIONAL DESCRIPTION

The Am9130 products are high performance, low-power, 4096-bit, static, read/write random access memories. They are implemented as 1024 words by 4 bits per word. The data input and output signals are bussed together and share common I/O pins.

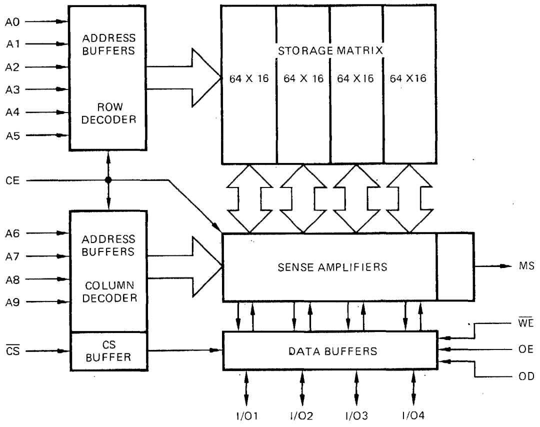
All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. The outputs will drive two full TTL loads or eight LS loads for increased fan-out, better capacitive drive and improved bus interface capability.

Operational cycles are initiated when the Chip Enable signal goes HIGH. When the read or write is complete, Chip Enable goes LOW to prepare the memory for the next cycle. Address and Chip Select signals are latched on-chip to help simplify system timing. Output data is also latched and is available from the access time until into the next operating cycle.

The $\overline{WE}$ signal is HIGH for all read operations and pulsed LOW during the Chip Enable time to perform a write. Memory Status is an output signal that indicates when data is valid and simplifies generation of CE.

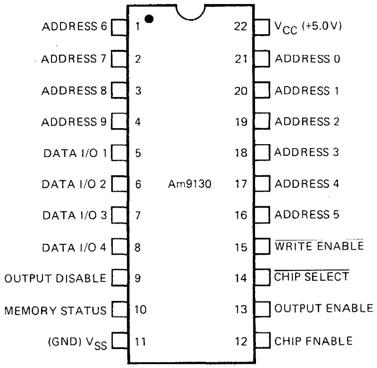
These memories may be operated in a DC standby mode for significant reductions in power dissipation. Data are retained on a deselected chip with $V_{CC}$ as low as 1.5V.

### BLOCK DIAGRAM


A0
A1
A2
A3
A4
A5
ADDRESS BUFFERS
ROW DECODER
STORAGE MATRIX
64 X 16
64 X 16
64 X 16
64 X16
CE
A6
A7
A8
A9
ADDRESS BUFFERS
COLUMN DECODER
SENSE AMPLIFIERS
MS
$\overline{CS}$
CS BUFFER
DATA BUFFERS
$\overline{WE}$
OE
OD
I/O1
I/O2
I/O3
I/O4

### CONNECTION DIAGRAM

Top View


ADDRESS 6 1
ADDRESS 7 2
ADDRESS 8 3
ADDRESS 9 4
DATA I/O 1 5
DATA I/O 2 6
DATA I/O 3 7
DATA I/O 4 8
OUTPUT DISABLE 9
MEMORY STATUS 10
(GND) $V_{SS}$ 11
12 CHIP FNABLE
13 OUTPUT ENABLE
14 $\overline{CHIP\ SELECT}$
15 $\overline{WRITE\ ENABLE}$
16 ADDRESS 5
17 ADDRESS 4
18 ADDRESS 3
19 ADDRESS 2
20 ADDRESS 1
21 ADDRESS 0
22 $V_{CC}$ (+5.0V)
Am9130

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Access Time | | | | |
|---|---|---|---|---|---|---|
| | | 500ns | 400ns | 300ns | 250ns | 200ns |
| Hermetic DIP | 0°C to+70°C | AM9130ADC | AM9130BDC | AM9130CDC | AM9130DDC | AM9130EDC |
| | –55°C to +125°C | AM9130ADM | AM9130BDM | AM9130CDM | | |

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5 V to +7.0 V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5 V to +7.0 V |
| Power Dissipation | 1.25W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{CC}$ | $V_{SS}$ |
|---|---|---|---|
| Am9130XDC | $0^\circ C \leq T_A \leq +70^\circ C$ | +5.0V ±5% | 0V |
| Am9130XDM | $-55^\circ C \leq T_A \leq +125^\circ C$ | +5.0V ± 10% | 0V |

## ELECTRICAL CHARACTERISTICS over operating range (note 1)

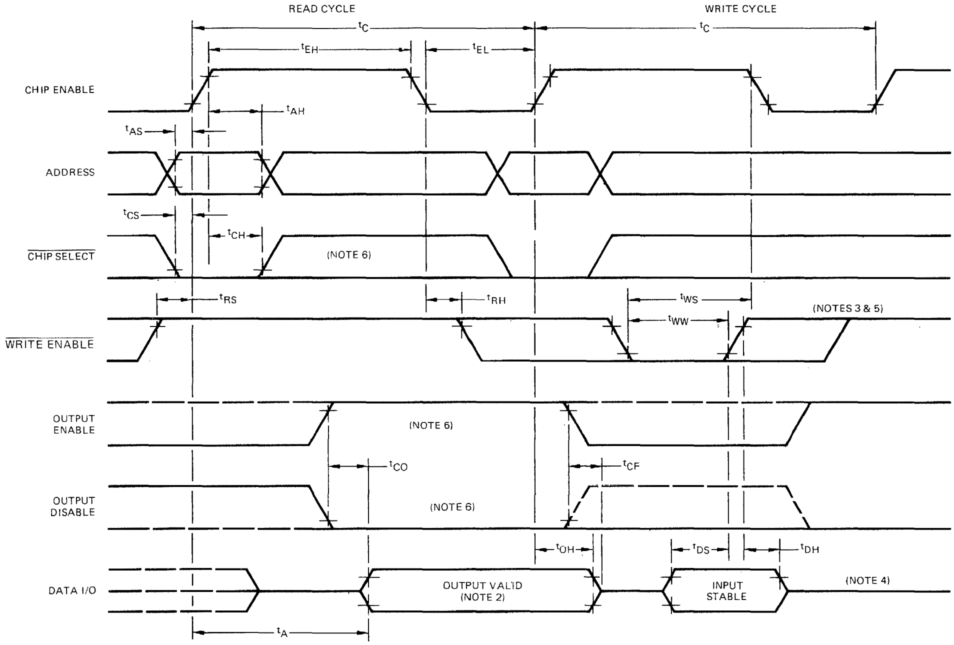
| Parameters | Description | Test Conditions | | Am9130XDC Min. | Am9130XDC Typ. | Am9130XDC Max. | Am9130XDM Min. | Am9130XDM Typ. | Am9130XDM Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | $V_{CC} = 4.75V$ | 2.4 | | | 2.4 | | | Volts |
| | | | $V_{CC} = 4.5V$ | | | | 2.2 | | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | | 0.4 | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ | 2.0 | | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | | 0.8 | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{SS} \leq V_{IN} \leq V_{CC}$ | | | | 10 | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled | | | | 10 | | | 10 | μA |
| $I_{CC}$ | $V_{CC}$ Supply Current | Max. $V_{CC}$ Output disabled | $T_A = 25^\circ C$ | | 60 | 102 | | 60 | 102 | mA |
| | | | $T_A = 0^\circ C$ | | | 110 | | | 110 | |
| | | | $T_A = -55^\circ C$ | | | | | | 125 | |
| $C_{IA}$ | Input Capacitance (Address) | Test frequency = 1 MHz<br>$T_A = 25^\circ C$<br>All pins at 0V | | | 3.0 | 6.0 | | 3.0 | 6.0 | pF |
| $C_{OUT}$ | Output Capacitance | | | | 4.0 | 7.0 | | 4.0 | 7.0 | pF |
| $C_{I/O}$ | I/O Capacitance | | | | 6.0 | 9.0 | | 6.0 | 9.0 | pF |
| $C_{IC}$ | Input Capacitance (Control) | | | | 6.0 | 9.0 | | 6.0 | 9.0 | pF |

Notes:
1. Typical values are for $T_A = 25^\circ C$, nominal supply voltage and nominal processing parameters.
2. The output buffer can be ON and output data valid only as long as Output Enable is HIGH and Output Disable is LOW. If either condition is changed, the output buffer will turn OFF.
3. During a write cycle, the output buffer must be turned OFF in order to eliminate conflict with input data on the I/O bus. This can be done by bringing OE LOW or bringing OD HIGH or both. It will often be convenient to tie OE to $\overline{WE}$ in order to accomplish this function. In such a case the minimum write pulse width should be longer by the output turn-off delay: $t_{WW}(\text{min.}) = t_{DS}(\text{min.}) + t_{CF}(\text{max.})$.
4. The timing diagram specifies the input data set-up and hold times with respect to the rising edge of $\overline{WE}$. If that edge occurs during CE LOW, the data set-up is referenced to the 2.0V level of the falling edge of CE and the data hold is referenced to the 0.8V level of the falling edge of CE.
5. The minimum write pulse width specification assumes that the falling edge of $\overline{WE}$ occurs more than 50ns after the rising edge of Chip Enable. $\overline{WE}$ may fall earlier, but the minimum write pulse width requirement should be extended to compensate.
6. $\overline{CS}$, OE and OD may be operated at constant levels where appropriate. The only requirements are that $\overline{CS}$ must be HIGH to deselect the chip and either OE must be LOW or OD must be HIGH to properly perform a write operation (See Note 3).

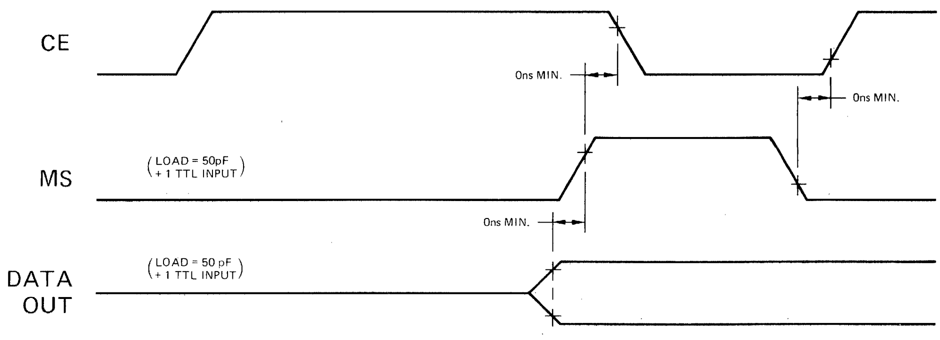
## SWITCHING CHARACTERISTICS over operating range

| Parameters | Description | Test Conditions | Am9130A | | Am9130B | | Am9130C | | Am9130E | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_C$ | Cycle Time | Transition times ≤ 20ns<br>Output load = 1 TTL gate plus 50pF<br>Input and output timing reference levels are 0.8V and 2.0V | 840 | | 690 | | 530 | | 370 | | ns |
| $t_A$ | Access Time (CE to Output Valid Delay) | | 30 | 500 | 30 | 400 | 30 | 300 | 30 | 200 | ns |
| $t_{AS}$ | Address to Chip Enable Set-up Time | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{AH}$ | Chip Enable to Address Hold Time | | 200 | | 170 | | 130 | | 100 | | ns |
| $t_{CS}$ | Chip Select to Chip Enable Set-up Time | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{CH}$ | Chip Enable to Chip Select Hold Time | | 200 | | 170 | | 130 | | 100 | | ns |
| $t_{RS}$ | Read to Chip Enable Set-up Time | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{RH}$ | Chip Enable to Read Hold Time | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OH}$ | Chip Enable to Output OFF Delay | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DS}$ | Data Input Set-up Time (Note 4) | | 300 | | 250 | | 200 | | 150 | | ns |
| $t_{DH}$ | Data Input Hold Time (Note 4) | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WS}$ | Write to Chip Enable Set-up Time | | 300 | | 250 | | 200 | | 150 | | ns |
| $t_{WW}$ | Write Pulse Width (Notes 3 & 5) | | 300 | | 250 | | 200 | | 150 | | ns |
| $t_{CF}$ | OE or OD to Output OFF Delay | | | 210 | | 175 | | 135 | | 100 | ns |
| $t_{CO}$ | OE or OD to Output ON Delay | | | 250 | | 200 | | 150 | | 110 | ns |
| $t_{EH}$ | Chip Enable HIGH Time | | 500 | | 400 | | 300 | | 200 | | ns |
| $t_{EL}$ | Chip Enable LOW Time | | 300 | | 250 | | 190 | | 130 | | ns |

## SWITCHING WAVEFORMS


READ CYCLE
WRITE CYCLE
tC
tC
tEH
tEL
CHIP ENABLE
tAH
tAS
ADDRESS
tCS
tCH
CHIP SELECT
(NOTE 6)
tRS
tRH
tWS
tWW
(NOTES 3 & 5)
WRITE ENABLE
OUTPUT ENABLE
(NOTE 6)
tCO
tCF
OUTPUT DISABLE
(NOTE 6)
tOH
tDS
tDH
DATA I/O
OUTPUT VALID (NOTE 2)
INPUT STABLE
(NOTE 4)
tA

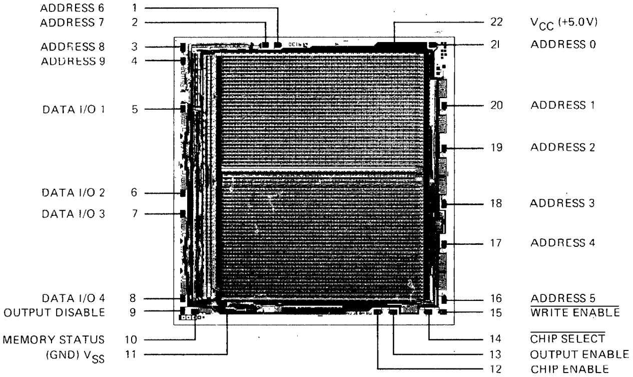
## MEMORY STATUS SPECIFICATION FOR Am9130


CE
0ns MIN.
0ns MIN.
MS
(LOAD = 50pF + 1 TTL INPUT)
0ns MIN.
DATA OUT
(LOAD = 50 pF + 1 TTL INPUT)

Memory Status is an output signal from the memory indicating the real access time of the part for the operating conditions then present. It will always indicate a data access time better than the worst-case specification for the part. The exact position of MS relative to CE will change from part to part and with changing temperature and supply voltage. It will always maintain its relationship to valid output data as shown above. Nominal delay from data to MS is 15ns.

The rising edge of MS also indicates that CE may go LOW. The falling edge of MS indicates that CE may go HIGH. Thus, the MS output fully specifies the CE requirement for any part under any set of operating conditions. In fact, CE = $\overline{\text{MS}}$; the MS output may be inverted and used as the CE input. See application note for more information about the use and operation of the Memory Status signal.

### Metallization and Pad Layout

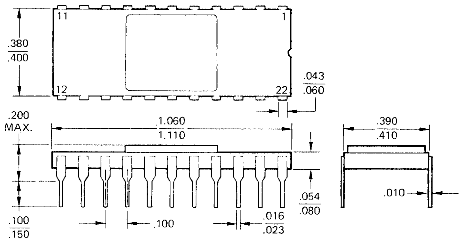

ADDRESS 6 1
ADDRESS 7 2
ADDRESS 8 3
ADDRESS 9 4
DATA I/O 1 5
DATA I/O 2 6
DATA I/O 3 7
DATA I/O 4 8
OUTPUT DISABLE 9
MEMORY STATUS 10
(GND) V_SS 11
22 V_CC (+5.0V)
21 ADDRESS 0
20 ADDRESS 1
19 ADDRESS 2
18 ADDRESS 3
17 ADDRESS 4
16 ADDRESS 5
15 WRITE ENABLE
14 CHIP SELECT
13 OUTPUT ENABLE
12 CHIP ENABLE

DIE SIZE 0.192" x 0.197"

### PHYSICAL DIMENSIONS

### Dual-In-Line

### 22-Pin Hermetic


11
1
12
22
.380
.400
.043
.060
.200 MAX.
1.060
1.110
.390
.410
.054
.080
.010
.100
.150
.100
.016
.023

# Am9140

## 4096 x 1 Static R/W Random Access Memory

### DISTINCTIVE CHARACTERISTICS

- 4k x 1 organization
- Fully static data storage – no refreshing
- Single +5V power supply
- High-speed – access times down to 200ns max.
- Low-power – 578mW max. – 350mW typ.
- Interface logic levels identical to TTL
- High noise immunity – 400mV worst case
- High output drive – two standard TTL loads
- DC standby mode – reduces power by > 80%
- Uniform switching characteristics
- Dual output controls – flexible output operations
- Address and data registers on-chip
- Constant power drain – no large surges
- Unique Memory Status signal
    - –improves performance
    - –simplifies timing
- MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

### FUNCTIONAL DESCRIPTION

The Am9140 products are high performance, low-power, 4k-bit, static, read/write random access memories. They are implemented as 4096 words by 1 bit per word. The data input and output signals use separate pins for maximum flexibility.

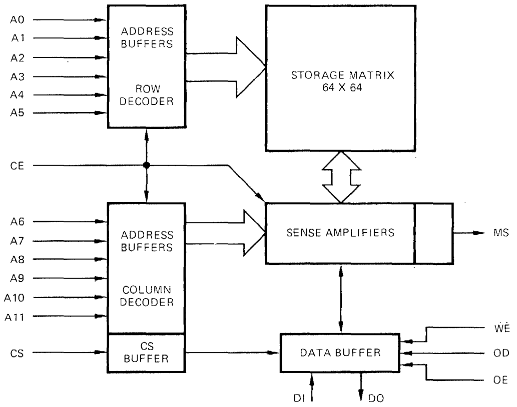
All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. The three-state output will drive two full TTL loads or eight low-power Schottky loads for increased fan-out, better capacitive drive and improved bus interface capability.

Operational cycles are initiated when the Chip Enable signal goes HIGH. When the read or write is complete, Chip Enable goes LOW to prepare the memory for the next cycle. Address and Chip Select signals are latched on-chip to help simplify system timing. Output data is also latched and is available until into the next operating cycle.

The $\overline{\text{WE}}$ signal is HIGH for all read operations and is pulsed LOW during the Chip Enable time to perform a write. Memory Status is an output signal that indicates when data is valid and simplifies generation of CE.

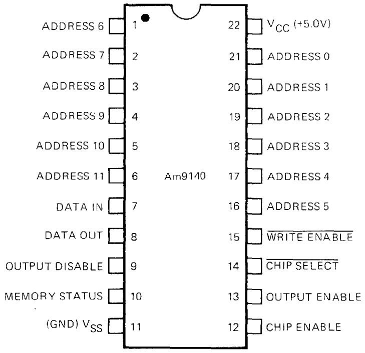
These memories may be operated in a DC standby mode for significant reductions in power dissipation. Data are retained on a deselected chip with $V_{CC}$ as low as 1.5V.

### BLOCK DIAGRAM


A0
A1
A2
A3
A4
A5
ADDRESS BUFFERS
ROW DECODER
STORAGE MATRIX 64 X 64
CE
A6
A7
A8
A9
A10
A11
ADDRESS BUFFERS
COLUMN DECODER
SENSE AMPLIFIERS
MS
CS
CS BUFFER
DATA BUFFER
WE
OD
OE
DI
DO

### CONNECTION DIAGRAM

Top View


ADDRESS 6 1
ADDRESS 7 2
ADDRESS 8 3
ADDRESS 9 4
ADDRESS 10 5
ADDRESS 11 6
DATA IN 7
DATA OUT 8
OUTPUT DISABLE 9
MEMORY STATUS 10
(GND) VSS 11
22 VCC (+5.0V)
21 ADDRESS 0
20 ADDRESS 1
19 ADDRESS 2
18 ADDRESS 3
17 ADDRESS 4
16 ADDRESS 5
15 WRITE ENABLE
14 CHIP SELECT
13 OUTPUT ENABLE
12 CHIP ENABLE
Am9140

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Access Time | | | | |
|---|---|---|---|---|---|---|
| | | 500ns | 400ns | 300ns | 250ns | 200ns |
| Hermetic DIP | 0°C to +70°C | AM9140ADC | AM9140BDC | AM9140CDC | AM9140DDC | AM9140EDC |
| | –55°C to +125°C | AM9140ADM | AM9140BDM | AM9140CDM | | |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5V to +7.0V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5V to +7.0V |
| Power Dissipation | 1.25W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{CC}$ | $V_{SS}$ |
|---|---|---|---|
| Am9140XDC | $0°C \leq T_A \leq +70°C$ | +5.0V ±5% | 0V |
| Am9140XDM | $-55°C \leq T_A \leq +125°C$ | +5.0V ± 10% | 0V |

## ELECTRICAL CHARACTERISTICS over operating range (note 1)

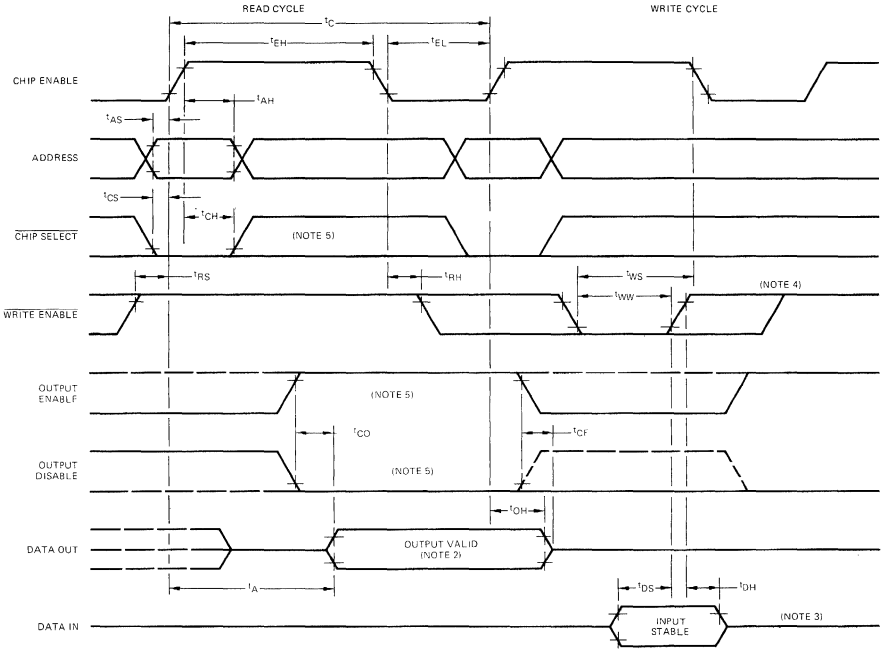
| Parameters | Description | Test Conditions | | Am9140XDC Min. | Am9140XDC Typ. | Am9140XDC Max. | Am9140XDM Min. | Am9140XDM Typ. | Am9140XDM Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | $V_{CC} = 4.75V$ | 2.4 | | | 2.4 | | | Volts |
| | | | $V_{CC} = 4.5V$ | | | | 2.2 | | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | | 0.4 | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ | 2.0 | | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | | 0.8 | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{SS} \leq V_{IN} \leq V_{CC}$ | | | | 10 | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled | | | | 10 | | | 10 | μA |
| $I_{CC}$ | $V_{CC}$ Supply Current | Max. $V_{CC}$ Output disabled | $T_A = 25°C$ | | 60 | 102 | | 60 | 102 | mA |
| | | | $T_A = 0°C$ | | | 110 | | | 110 | |
| | | | $T_A = -55°C$ | | | | | | 125 | |
| $C_{IA}$ | Input Capacitance (Address) | Test frequency = 1 MHz<br>$T_A = 25°C$<br>All pins at 0V | | | 3.0 | 6.0 | | 3.0 | 6.0 | pF |
| $C_{OUT}$ | Output Capacitance | | | | 4.0 | 7.0 | | 4.0 | 7.0 | pF |
| $C_{IC}$ | Input Capacitance (Control) | | | | 6.0 | 9.0 | | 6.0 | 9.0 | pF |

Notes:
1. Typical values are for $T_A = 25°C$, nominal supply voltage and nominal processing parameters.
2. The output buffer can be ON and output data valid only as long as Output Enable is HIGH and Output Disable is LOW. If either condition is changed, the output buffer will turn OFF.
3. The timing diagram specifies the input data set-up and hold times with respect to the rising edge of $\overline{WE}$. If that edge occurs during CE LOW, the data set-up is referenced to the 2.0V level of the falling edge of CE and the data hold is referenced to the 0.8V level of the falling edge of CE.
4. The minimum write pulse width specification assumes that the falling edge of $\overline{WE}$ occurs more than 50ns after the rising edge of Chip Enable. $\overline{WE}$ may fall earlier, but the minimum write pulse width requirements should be extended to compensate.
5. $\overline{CS}$, OE and OD may be operated at constant levels where appropriate.

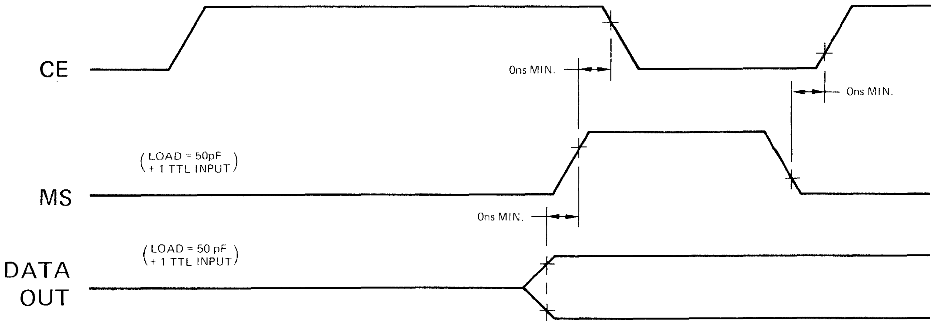
## SWITCHING CHARACTERISTICS over operating range

| Parameters | Description | Test Conditions | Am9140A | | Am9140B | | Am9140C | | Am9140E | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_C$ | Cycle Time | Transition times ≤ 20ns<br>Output load = 1 TTL gate plus 50pF<br>Input and output timing reference levels are 0.8V and 2.0V | 840 | | 690 | | 530 | | 370 | | ns |
| $t_A$ | Access Time (CE to Output Valid Delay) | | 30 | 500 | 30 | 400 | 30 | 300 | 30 | 200 | ns |
| $t_{AS}$ | Address to Chip Enable Set-up Time | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{AH}$ | Chip Enable to Address Hold Time | | 200 | | 170 | | 130 | | 100 | | ns |
| $t_{CS}$ | Chip Select to Chip Enable Set-up Time | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{CH}$ | Chip Enable to Chip Select Hold Time | | 200 | | 170 | | 130 | | 100 | | ns |
| $t_{RS}$ | Read to Chip Enable Set-up Time | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{RH}$ | Chip Enable to Read Hold Time | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OH}$ | Chip Enable to Output OFF Delay | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DS}$ | Data Input Set-up Time (Note 3) | | 300 | | 250 | | 200 | | 150 | | ns |
| $t_{DH}$ | Data Input Hold Time (Note 3) | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WS}$ | Write to Chip Enable Set-up Time | | 300 | | 250 | | 200 | | 150 | | ns |
| $t_{WW}$ | Write Pulse Width (Note 4) | | 300 | | 250 | | 200 | | 150 | | ns |
| $t_{CF}$ | OE or OD to Output OFF Delay | | | 210 | | 175 | | 135 | | 100 | ns |
| $t_{CO}$ | OE or OD to Output ON Delay | | | 250 | | 200 | | 150 | | 110 | ns |
| $t_{EH}$ | Chip Enable HIGH Time | | 500 | | 400 | | 300 | | 200 | | ns |
| $t_{EL}$ | Chip Enable LOW Time | | 300 | | 250 | | 200 | | 150 | | ns |

## SWITCHING WAVEFORMS


READ CYCLE
WRITE CYCLE
tC
tEH
tEL
CHIP ENABLE
tAH
tAS
ADDRESS
tCS
tCH
CHIP SELECT
(NOTE 5)
tRS
tRH
tWS
tWW
(NOTE 4)
WRITE ENABLE
OUTPUT ENABLE
(NOTE 5)
tCO
tCF
OUTPUT DISABLE
(NOTE 5)
tOH
DATA OUT
OUTPUT VALID (NOTE 2)
tA
tDS
tDH
DATA IN
INPUT STABLE
(NOTE 3)

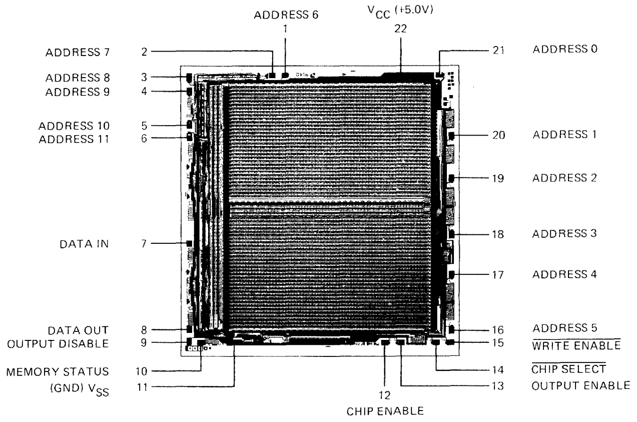
## MEMORY STATUS SPECIFICATION FOR Am9140


CE
0ns MIN.
0ns MIN.
(LOAD = 50pF + 1 TTL INPUT)
MS
0ns MIN.
(LOAD = 50 pF + 1 TTL INPUT)
DATA OUT

Memory Status is an output signal from the memory indicating the real access time of the part for the operating conditions then present. It will always indicate a data access time better than the worst-case specification for the part. The exact position of MS relative to CE will change from part to part and with changing temperature and supply voltage. It will always maintain its relationship to valid output data as shown above. Nominal delay from data to MS is 15ns.

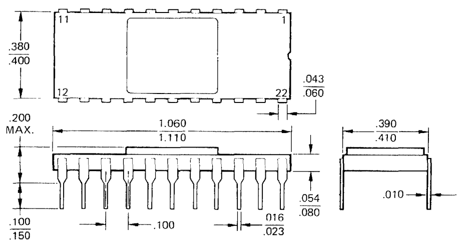
The rising edge of MS also indicates that CE may go LOW. The falling edge of MS indicates that CE may go HIGH. Thus, the MS output fully specifies the CE requirement for any part under any set of operating conditions. In fact, CE = $\overline{\mathrm{MS}}$; the MS output may be inverted and used as the CE input. See application note for more information about the use and operation of the Memory Status signal.

### Metallization and Pad Layout


ADDRESS 6 1
$V_{CC}$ (+5.0V) 22
ADDRESS 7 2
ADDRESS 8 3
ADDRESS 9 4
ADDRESS 10 5
ADDRESS 11 6
DATA IN 7
DATA OUT 8
OUTPUT DISABLE 9
MEMORY STATUS 10
(GND) $V_{SS}$ 11
12 CHIP ENABLE
21 ADDRESS 0
20 ADDRESS 1
19 ADDRESS 2
18 ADDRESS 3
17 ADDRESS 4
16 ADDRESS 5
15 $\overline{\text{WRITE ENABLE}}$
14 $\overline{\text{CHIP SELECT}}$
13 OUTPUT ENABLE

DIE SIZE 0.192" x 0.197"

### PHYSICAL DIMENSIONS
Dual-In-Line
22-Pin Hermetic


11
1
12
22
.380
.400
.043
.060
.200 MAX.
1.060
1.110
.390
.410
.054
.080
.010
.100
.150
.100
.016
.023

# Read Only Memories

## NUMERICAL INDEX

### Erasable

Page

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## SELECTION GUIDE

### READ ONLY MEMORIES

| Part Number | Organization | Access Time (nsec) | Temp. Range | Supply Voltages | Operating Power-Max. (mW) | Outputs |
|---|---|---|---|---|---|---|
| Am9214 | 512 x 8 | 500 | C M | +5 | 263 | 3-State |
| Am9208B | 1024 x 8 | 400 | C, M | +5, +12 | 620 | 3-State |
| Am9208C | 1024 x 8 | 300 | C, M | +5, +12 | 620 | 3-State |
| Am9208D | 1024 x 8 | 250 | C | +5, +12 | 700 | 3-State |
| Am9216B | 2048 x 8 | 400 | C, M | +5, +12 | 660 | 3-State |
| Am9216C | 2048 x 8 | 300 | C | +5, +12 | 700 | 3-State |

### ULTRAVIOLET ERASABLE PROGRAMMABLE READ ONLY MEMORY

| Part Number | Organization | Access Time (nsec) | Temp. Range | Supply Voltages | Operating Power-Max. (mW) | Outputs |
|---|---|---|---|---|---|---|
| Am1702A | 256 x 8 | 1.0μs | C, E | –9, +5 | 676 | 3-State |

# Am1702A

## 256-Word by 8-Bit Programmable ROM's

### Distinctive Characteristics

- Field programmable 2048-bit ROM's
- Am1702A can be erased and reprogrammed by UV light
- 100% tested for programmability
- Typical programming time of 2 minutes/device
- Available for operation over full military temperature range
- 100% processing to MIL-STD-883

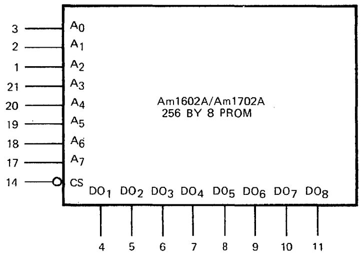
### FUNCTIONAL DESCRIPTION

The Am1702A is a 256-word by 8-bit field programmable MOS read-only memory, differing only in the package. The Am1702A package has a quartz lid through which the PROM can be erased by ultraviolet light.

The device is shipped with all outputs at a logic LOW level. Each bit in the memory can be electrically programmed to a HIGH level. The device has three-state outputs which go to a high-impedance OFF state when the chip select is HIGH. When the chip select is LOW, the outputs can drive one TTL unit load.

The Am1702A can directly replace the Intel 1702A. Except for programming procedure, the Am1702A can replace the 1702. (The Am1702A differs from the Am1702 only in the programming method and in the programmed state. The Am1702 is initially all HIGH, and the LOW's are programmed; the Am1602A/1702A is initially all LOW and the HIGH's are programmed. Once programmed, they are identical).

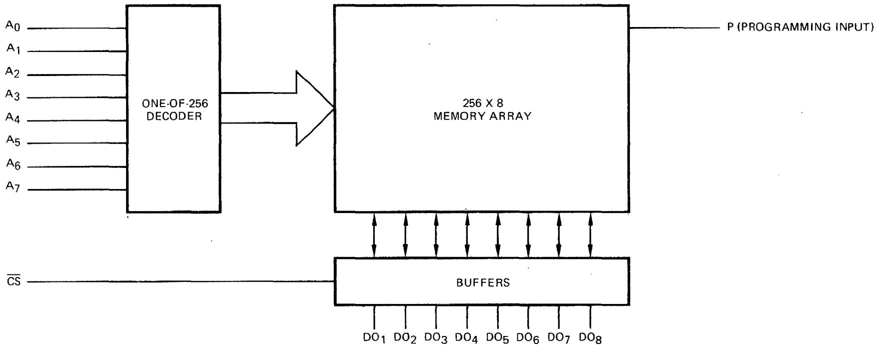
### LOGIC SYMBOL


3 A0
2 A1
1 A2
21 A3
20 A4
19 A5
18 A6
17 A7
14 CS
Am1602A/Am1702A
256 BY 8 PROM
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8
4 5 6 7 8 9 10 11

$V_{CC}$ = Pin 12
$V_{DD}$ = Pin 24
$V_{GG}$ = Pin 16
$V_{BB}$ = Pin 15
P = Pin 13

Pins 22 and 23 must be connected to $V_{CC}$.

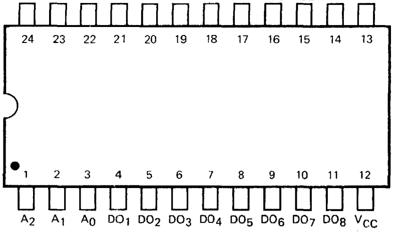
### LOGIC BLOCK DIAGRAM


A0
A1
A2
A3
A4
A5
A6
A7
ONE-OF-256 DECODER
256 X 8 MEMORY ARRAY
P (PROGRAMMING INPUT)
CS
BUFFERS
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP/Quartz Lid | 0°C to +70°C | AM1702ADC |
| Hermetic Dip/Quartz Lid | –55°C to +85°C | AM9702AHDL |

### CONNECTION DIAGRAM
#### Top View


CONNECT TO VCC
VDD A3 A4 A5 A6 A7 VGG VBB CS P
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
A2 A1 A0 DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8 VCC

Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | –65°C to +125°C |
| Temperature (Ambient) Under Bias | –55°C to +70°C |
| Power Dissipation | 1 W |
| Input and Supply Voltages (Operating) | $V_{CC}$ –20 V to $V_{CC}$ +0.5 V |
| Input and Supply Voltages (Programming) | –50 V |

## OPERATING RANGE

| Part Number | $V_{CC}$ | $V_{DD}$ | $V_{GG}$ | Ambient Temperature |
|---|---|---|---|---|
| C1702A | +5.0 V ± 5% | –9.0 V ± 5% | –9.0 V ± 5% | 0°C to +70°C |

During operation $V_{BB}$ = P = pin 22 = pin 23 = $V_{CC}$.

## D. C. CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Level | $I_{OH}$ = –200μA | 3.5 | 4.5 | | V |
| $V_{OL}$ | Output LOW Level | $I_{OL}$ = 1.6 mA | | –.7 | 0.45 | V |
| $I_{OH}$ | Output HIGH Current | $V_{OUT}$ = 0.0 V | –2.0 | | | mA |
| $I_{OL}$ | Output LOW Current | $V_{OUT}$ = 0.45 V | 1.6 | 4 | | mA |
| $V_{IH}$ | Input HIGH Level | | $V_{CC}$–2.0 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Input LOW Level | | $V_{CC}$–10.0 | | $V_{CC}$–4.2 | V |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 0.0 V | | | 1.0 | μA |
| $I_{LO}$ | Output Leakage Current | $\overline{CS}$ = $V_{CC}$–2.0, $V_{OUT}$ = 0.0V | | | 1.0 | μA |
| $I_{CF1}$ | Output Clamp Current | $T_A$ = 0°C, $V_{OUT}$ = –1.0 V | | 8 | 14 | mA |
| $I_{CF2}$ | Output Clamp Current | $T_A$ = 25°C, $V_{OUT}$ = –1.0 V | | | 13 | mA |
| $I_{GG}$ | $V_{GG}$ Current | | | | 1.0 | μA |
| $I_{DD0}$ | $V_{DD}$ Current (Note 1) | $V_{GG}$ = $V_{CC}$, $I_{OL}$ = 0<br>$V_{\overline{CS}}$ = $V_{CC}$–2.0, $T_A$ = 25°C | | 5 | 10 | mA |
| $I_{DD1}$ | | $I_{OL}$ = 0, $V_{\overline{CS}}$ = $V_{CC}$–2.0, $T_A$ = 25°C | | 35 | 50 | mA |
| $I_{DD2}$ | | $I_{OL}$ = 0, $V_{\overline{CS}}$ = 0, $T_A$ = 25°C | | 32 | 46 | mA |
| $I_{DD3}$ | | $I_{OL}$ = 0, $V_{\overline{CS}}$ = $V_{CC}$–2.0, $T_A$ = 0°C | | 38.5 | 60 | mA |

Note: 1. $I_{DD}$ may be reduced by pulsing the $V_{GG}$ supply between $V_{CC}$ and –9 V. $V_{DD}$ current will be directly proportional to $V_{GG}$ duty cycle. The data outputs will be unaffected by address or chip select changes while $V_{GG}$ is at $V_{CC}$. For this option specify Am1702AL.

## CAPACITANCE ($T_A$ = 25°C)

(These parameters are guaranteed by design and are not 100% tested)

| Parameters | Description | Conditions | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | All unused pins are at $V_{CC}$ | 8 | 15 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | 15 | pF |
| $C_{VGG}$ | $V_{GG}$ Capacitance | | | 30 | pF |

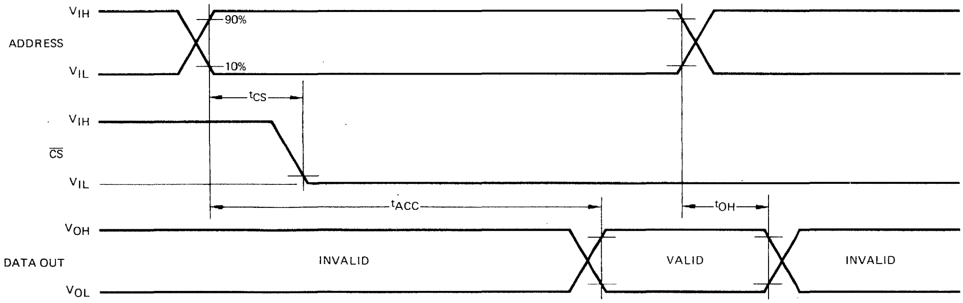
## A. C. CHARACTERISTICS OVER OPERATING RANGE

$V_{IL}$ = 0V, $V_{IH}$ = 4.0V, $t_r = t_f \leqslant$ 50ns, Load = 1 TTL Gate.

| Parameters | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{reg}$ | Repetition Rate | | | | 1.0 | MHz |
| $t_{OH}$ | Previous Read Data Valid | | | | 100 | ns |
| $t_{ACC}$ | Address to Output Delay | | | 0.7 | 1.0 | μs |
| $t_{DVGG}$ | Set-up Time, $V_{GG}$ | | 0 | | | μs |
| $t_{\overline{CS}}$ | Chip Select Delay | | | | 100 | ns |
| $t_{CO}$ | Output Delay from $\overline{CS}$ | | | | 900 | ns |
| $t_{OD}$ | Output Deselect $T_A$ = 0°C to +70°C | | | | 300 | ns |
| $t_{OHC}$ | Data Out Valid from $V_{GG}$ (Note 2) | | | | 5.0 | μs |

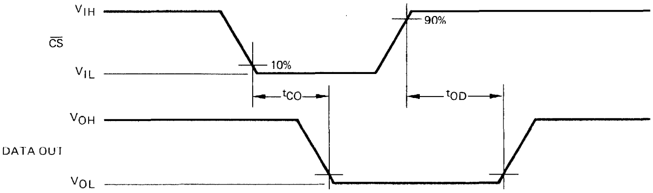
Note: 2. The output will remain valid for $t_{OHC}$ after the $V_{GG}$ pin is raised to $V_{CC}$, even if address changes occur.

## SWITCHING WAVEFORMS



$V_{IH}$
ADDRESS
$V_{IL}$
90%
10%
$t_{CS}$
$V_{IH}$
$\overline{CS}$
$V_{IL}$
$t_{ACC}$
$t_{OH}$
$V_{OH}$
DATA OUT
$V_{OL}$
INVALID
VALID
INVALID

Figure 1. Reading Data



$V_{IH}$
$\overline{CS}$
$V_{IL}$
10%
90%
$t_{CO}$
$t_{OD}$
$V_{OH}$
DATA OUT
$V_{OL}$

Figure 2. Deselecting Output from Chip Select.

### CLOCKED $V_{GG}$ OPERATION

The $V_{GG}$ input may be switched between +5 V ($V_{CC}$) and –9 V to save power. To read data, the $V_{GG}$ level must be lowered to –9 V at least $t_{DVGG}$ prior to the address selection. Once data has appeared at the output ($t_{ACC}$), $V_{GG}$ may be raised to +5 V. The data output will remain steady for $t_{OHC}$. To deselect the chip, $\overline{CS}$ must be raised to $V_{IH}$ prior to raising $V_{GG}$ to +5 V. If $\overline{CS}$ goes HIGH while $V_{GG}$ is at $V_{CC}$, deselection of the chip will not occur until $t_{OD}$ after $V_{GG}$ goes back to –9 V.

## PROGRAMMING THE Am1702A

Each storage node in the Am1702A consists of an MOS transistor whose gate is not connected to any circuit element. The transistors are all normally off, making all outputs LOW in an unprogrammed device. A bit is programmed to a HIGH by applying a large negative voltage at the MOS transistor; electrons tunnel through the gate insulation onto the gate itself. When the programming voltage is removed, a charge is left on the gate which holds the transistor on. Since the gate is completely isolated, there is no path by which the charge can escape, except for random high energy electrons which might retunnel through the gate insulation. Under ordinary conditions retunneling is not significant. The application of high energy to the chip through X-rays or UV light (via the quartz window) raises energy levels so that the charge can escape the gate region, erasing the program and restoring the device to all LOW.

Programming a bit is accomplished by addressing the desired word using negative 44V logic levels, applying a negative voltage to $V_{DD}$, $V_{GG}$, and the outputs to be programmed, and then applying a −49 volt pulse to the programming pin. The duty cycle on the programming pin should not exceed 20% to avoid over-heating the device. For long-term data retention, at least 32 program pulses should be applied for each address. All eight outputs are programmed simultaneously.

Programming Boards are available for the Data I/O automatic programmer (part number 1010/1011), for the Spectrum Dynamics programmer (part number 434-549), and for the Pro-Log programmer (part number PM9001).

## ERASING THE Am1702A

The Am1702A may be erased (restored to all LOW's) by exposing the die to ultraviolet light from a high intensity source. The recommended dosage is 6 W-sec/cm$^2$ at a wavelength of 2537 Å. The Ultraviolet Products, Inc., models UVS-54 or S-52 can erase the Am1702A in about 15 minutes, with the devices held one inch from the lamp. (Caution should be used when Am1702A's are inspected under fluorescent lamps after being programmed, as some fluorescent lamps may emit sufficiently in the UV to erase or "soften" the PROM.)

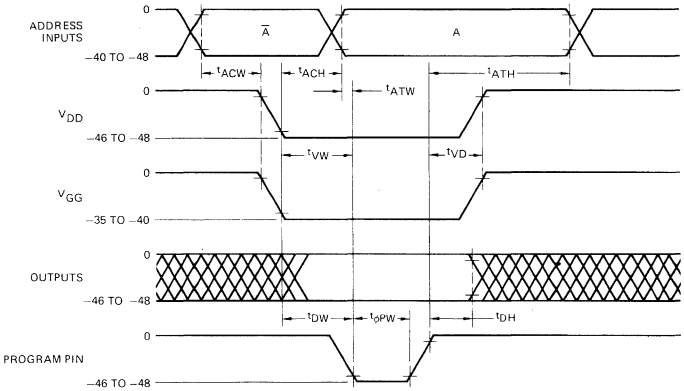
## PROGRAMMING REQUIREMENTS ($T_A = 25°C$, $V_{CC} = 0V$, $CS = 0V$, $V_{BB} = +12V \pm 10\%$)

| Parameters | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{LI1P}$ | Input Current, Address and Data | $V_{IN} = -48V$ | | | 10 | mA |
| $I_{LI2P}$ | Input Current, Program and $V_{GG}$ Inputs | $V_{IN} = -48V$ | | | 10 | mA |
| $I_{BB}$ | $V_{BB}$ Current | (Note 2) | | 10 | | mA |
| $I_{DDP}$ | $I_{DD}$ Current During Programming Pulse | $V_{DD} = V_{Prog} = -48V$, $V_{GG} = -35V$ | | 200 | Note 1 | mA |
| $V_{IHP}$ | Input HIGH Voltage | | | | 0.3 | Volts |
| $V_{IL1P}$ | Voltage Applied to Output to Program a HIGH | | −46 | | −48 | Volts |
| $V_{IL2P}$ | Input LOW Level on Address Inputs | | −40 | | −48 | Volts |
| $V_{IL3P}$ | Voltage Applied to $V_{DD}$ and Program Inputs | | −46 | | −48 | Volts |
| $V_{IL4P}$ | Voltage Applied to $V_{GG}$ Input | | −35 | | −40 | Volts |
| $t_{\phi PW}$ | Programming Pulse Width | $V_{GG} = -35V$, $V_{DD} = V_{Prog} = -48V$ | | | 3 | ms |
| $t_{DW}$ | Data Set-up Time | | 25 | | | µs |
| $t_{DH}$ | Data Hold Time | | 10 | | | µs |
| $t_{VW}$ | $V_{GG}$ and $V_{DD}$ Set-up Time | | 100 | | | µs |
| $t_{VD}$ | $V_{GG}$ and $V_{DD}$ Hold Time | | 10 | | 100 | µs |
| $t_{ACW}$ | Address Set-up Time (Complement) | | 25 | | | µs |
| $t_{ACH}$ | Address Hold Time (Complement) | | 25 | | | µs |
| $t_{ATW}$ | Address Set-up Time (True) | | 10 | | | µs |
| $t_{ATH}$ | Address Hold Time (True) | | 10 | | | µs |
| | Duty Cycle | | | | 20 | % |

Note: 1. Do not allow $I_{DD}$ to exceed 300mA for more than 100µs.

2. $V_{BB}$ supply must be current limited to 100mA max.

## PROGRAMMING WAVEFORMS

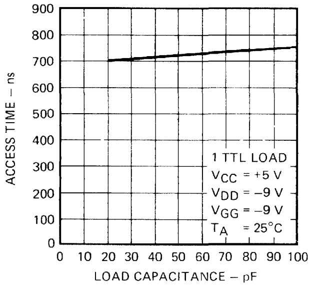

ADDRESS INPUTS
0
−40 TO −48
A̅
A
tACW
tACH
tATW
tATH
VDD
0
−46 TO −48
tVW
tVD
VGG
0
−35 TO −40
OUTPUTS
0
−46 TO −48
tDW
tφPW
tDH
PROGRAM PIN
0
−46 TO −48

A̅ = binary complement of address to be programmed.

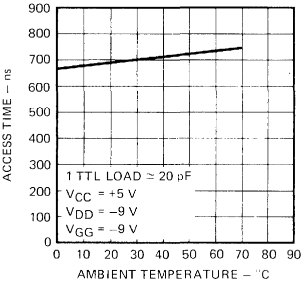
A = binary address to be programmed.

## TYPICAL PERFORMANCE CURVES

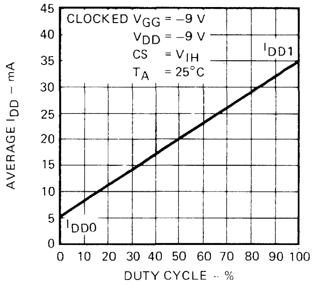
### Access Time Versus Load Capacitance



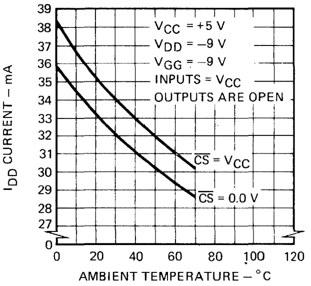
### Access Time Versus Temperature



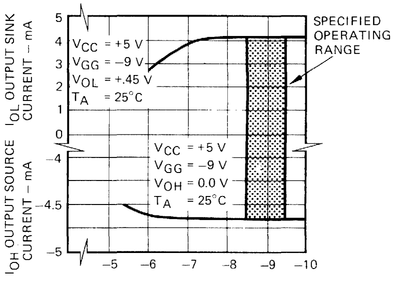
### Average Current Versus Duty Cycle for Clocked $V_{GG}$



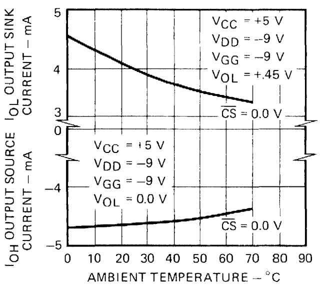
### $I_{DD}$ Current Versus Temperature



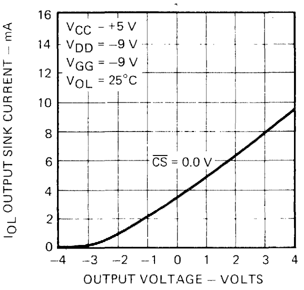
### Output Current Versus $V_{DD}$ Supply Voltage



### Output Current Versus Temperature



### Output Sink Current Versus Output Voltage

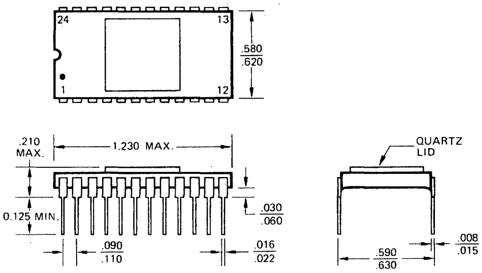


## PHYSICAL DIMENSIONS

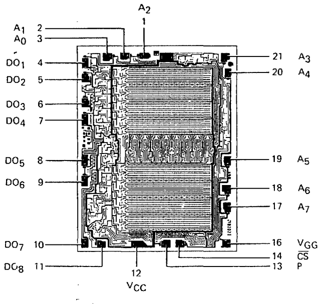
### Dual-In-Line

### 24-Pin Side Brazed

### Quartz Lid


24
13
1
12
.580
.620
.210
MAX.
1.230 MAX.
0.125 MIN.
.030
.060
.090
.110
.016
.022
QUARTZ
LID
.590
.630
.008
.015

## Metallization and Pad Layout


A2
1
A1 2
A0 3
DO1 4
DO2 5
DO3 6
DO4 7
DO5 8
DO6 9
DO7 10
DO8 11
12
VCC
21 A3
20 A4
19 A5
18 A6
17 A7
16 VGG
14 CS
13 P

DIE SIZE
0.109" X 0.142"

# Am9208

## 1024 x 8 Read Only Memory

### DISTINCTIVE CHARACTERISTICS

- 1024 x 8 organization
- High speed – 250ns access time
- Fully capacitive inputs – simplified driving
- 2 fully programmable chip selects – increased flexibility
- Logic voltage levels compatible to TTL
- Three-state output buffers – simplified expansion
- Standard supply voltages – +12V, +5.0V
- No $V_{BB}$ supply required
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing
- Direct plug-in replacement for Intel 8308/2308 and T. I. 4700

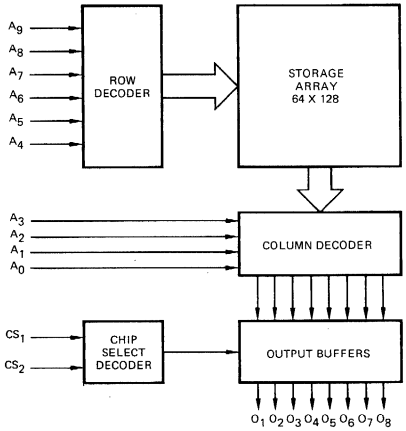
### FUNCTIONAL DESCRIPTION

The Am9208 devices are high performance, 8192 bit, static, mask programmed, read only memories. Each memory is implemented as 1024 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 1024 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9208 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. The Am9208 is pin compatible with the Am9216 which is a 16k-bit mask programmed ROM. Input and output voltage levels are compatible to TTL specifications, providing simplified interfacing.

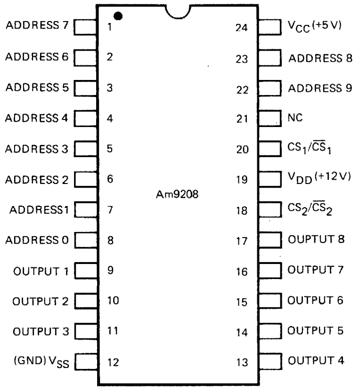
### BLOCK DIAGRAM



$A_9$
$A_8$
$A_7$
$A_6$
$A_5$
$A_4$
ROW DECODER
STORAGE ARRAY 64 X 128
$A_3$
$A_2$
$A_1$
$A_0$
COLUMN DECODER
$CS_1$
$CS_2$
CHIP SELECT DECODER
OUTPUT BUFFERS
$O_1$ $O_2$ $O_3$ $O_4$ $O_5$ $O_6$ $O_7$ $O_8$

### CONNECTION DIAGRAM

#### Top View



ADDRESS 7 1
ADDRESS 6 2
ADDRESS 5 3
ADDRESS 4 4
ADDRESS 3 5
ADDRESS 2 6
ADDRESS1 7
ADDRESS 0 8
OUTPUT 1 9
OUTPUT 2 10
OUTPUT 3 11
(GND) $V_{SS}$ 12
24 $V_{CC}$ (+5 V)
23 ADDRESS 8
22 ADDRESS 9
21 NC
20 $CS_1/\overline{CS}_1$
19 $V_{DD}$ (+12V)
18 $CS_2/\overline{CS}_2$
17 OUPTUT 8
16 OUTPUT 7
15 OUTPUT 6
14 OUTPUT 5
13 OUTPUT 4
Am9208

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Access Time | | |
|---|---|---|---|---|
| | | 400ns | 300ns | 250ns |
| Hermetic DIP | $0°C \leq T_A \leq 70°C$ | Am9208BDC | Am9208CDC | Am9208DDC |
| | $-55°C \leq T_A \leq 125°C$ | Am9208BDM | Am9208CDM | |

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{DD}$ with Respect to $V_{SS}$ | 15V |
| $V_{CC}$ with Respect to $V_{SS}$ | +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{DD}$ | $V_{CC}$ | $V_{SS}$ |
|---|---|---|---|---|
| Am9208DC | $0°C \leq T_A \leq +70°C$ | +12V ± 5% | +5.0V ± 5% | 0V |
| Am9208DM | $-55°C \leq T_A \leq +125°C$ | +12V ± 10% | +5.0V ± 10% | 0V |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

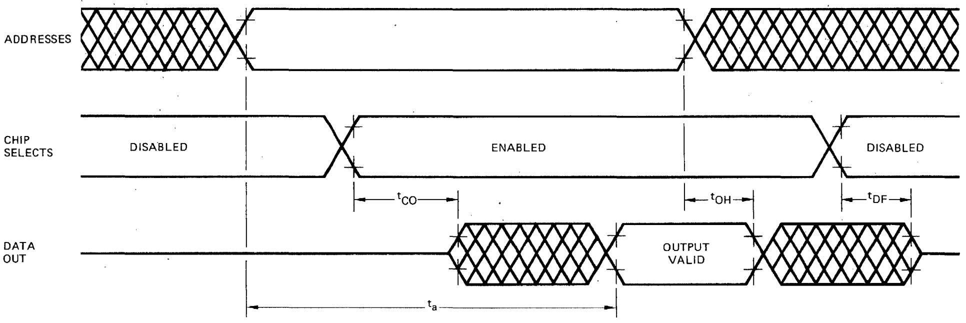
| Parameters | Description | Test Conditions | | Am9208DC Min. | Am9208DC Max. | Am9208DM Min. | Am9208DM Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -1.0mA$ | | 3.7 | | 3.7 | | Volts |
| | | $I_{OH} = -4.0mA$ | | 2.4 | | 2.4 | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | 0.4 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.4 | $V_{CC}+1.0$ | 2.6 | $V_{CC}+1.0$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | 0.8 | −0.5 | 0.8 | Volts |
| $I_{LO}$ | Output Leakage Current | Chip disable | | 10 | | 10 | | μA |
| $I_{LI}$ | Input Leakage Current | | | 10 | | 10 | | μA |
| $I_{DD}$ | $V_{DD}$ Supply Current | Selected | Am9208B/C | 35 | | 43 | | mA |
| | | | Am9208D | 44 | | 50 | | |
| | | Deselected | Am9208B/C | 48 | | 53 | | |
| | | | Am9208D | 55 | | 61 | | |
| $I_{CC}$ | $V_{CC}$ Supply Current | | Am9208B/C | 13 | | 15 | | mA |
| | | | Am9208D | 15 | | 17 | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

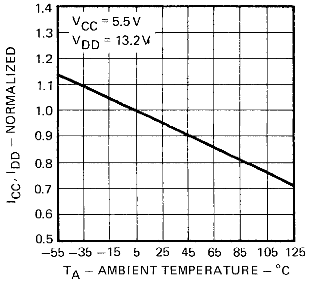
| Parameters | Description | Test Conditions | Am9208BDC<br>Am9208BDM Min. | Am9208BDC<br>Am9208BDM Max. | Am9208CDC<br>Am9208CDM Min. | Am9208CDC<br>Am9208CDM Max. | Am9208DDC Min. | Am9208DDC Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_a$ | Address to Output Access Time | $t_r = t_f = 20ns$<br>Output load:<br>one standard<br>TTL gate<br>plus 100pF<br>(Note 1) | | 400 | | 300 | | 250 | ns |
| $t_{CO}$ | Chip Select to Output ON Delay | | | 160 | | 140 | | 125 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | 20 | | ns |
| $t_{DF}$ | Chip Select to Output OFF Delay | | | 120 | | 100 | | 90 | ns |
| $C_I$ | Input Capacitance | $T_A = 25°C$, f = 1MHz<br>All pins at 0V | | 6.0 | | 6.0 | | 6.0 | pF |
| $C_O$ | Output Capacitance | | | 6.0 | | 6.0 | | 6.0 | pF |

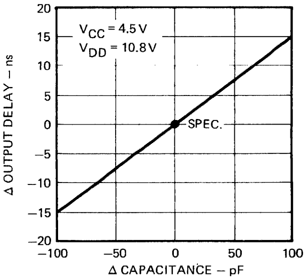
Notes: 1. Timing reference levels — Inputs: High = 2.0V, Low = 1.0V. Outputs: High = 2.4V, Low = 0.8V.

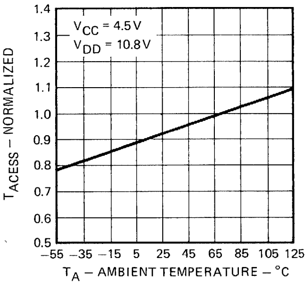
### SWITCHING WAVEFORMS

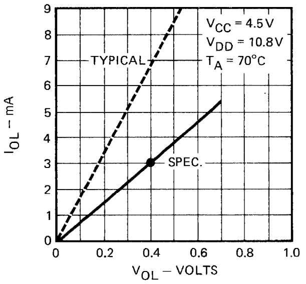


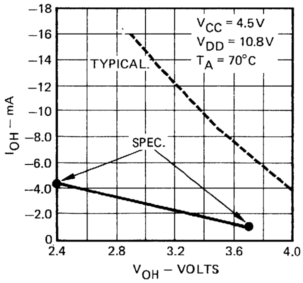
## TYPICAL CHARACTERISTICS


**$I_{DD}$, $I_{CC}$ Versus Temperature (Normalized)**


**Δ Output Capacitance Versus Δ Output Delay**


**$T_{Access}$ Versus Temperature (Normalized)**


**$I_{OL}$ Versus $V_{OL}$**


**$I_{OH}$ Versus $V_{OH}$**

## PROGRAMMING INSTRUCTIONS

### CUSTOM PATTERN ORDERING INFORMATION

The Am9208 is programmed from punched cards, card coding forms or from paper tape in card image form in the format as shown below.

Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0V)

### FIRST CARD

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data.<br>This is optional and should be left blank if not used. |
| 50 thru 62 | 9208B or 9208C |
| 65 thru 72 | Data |

### SECOND CARD

| Column Number | Description |
|---|---|
| 31 | $CS_2$ input required to select chip (0 or 1) |
| 33 | $CS_1$ input required to select chip (0 or 1) |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 1024 data cards are required.

| Column Number | |
|---|---|
| 10, 12, 14, 16, 18<br>20, 22, 24, 26, 28 | Address input pattern with the most significant bit ($A_9$) in column 10 and the least significant bit ($A_0$) in column 28. |
| 40, 42, 44, 46, 48,<br>50, 52, 54 | Output pattern with the most significant bit ($O_8$) in column 40 and the least significant bit ($O_1$) in column 54. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

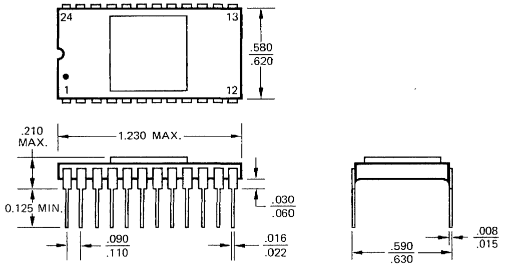
**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 64 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 3F: 64 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.

| ADDR | | | OUTPUT VALUES FOR ADDR + | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | | | 1 | | | 2 | | | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | | 8 | | | 9 | | | A | | | B | | | C | | | D | | | E | | | F | |
| 21 | 22 | 23 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 |
| 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | ⋮ | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | F | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | ⋮ | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | F | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## PHYSICAL DIMENSIONS

### Dual-In-Line

### 24-Pin Side Brazed



# Am9214/Am3514

## 512 x 8 Read Only Memory

### DISTINCTIVE CHARACTERISTICS

- Single 5-volt power supply
  Tolerances: ±5% commercial, ±10% military
- 512 x 8 organization
- Fully static operation – no clocks
- 4 programmable chip selects
- High-speed – 500ns access
- Three-state output buffers
- Low power dissipation – 263mW max.
- Logic voltage levels identical to TTL
- High noise immunity – full 400mV
- N-Channel silicon gate MOS technology
- Military and commercial temperature ranges available
- 100% MIL-STD-883 reliability assurance testing
- Directly plug-in compatible with FSC 3514, MOSTEK 2600

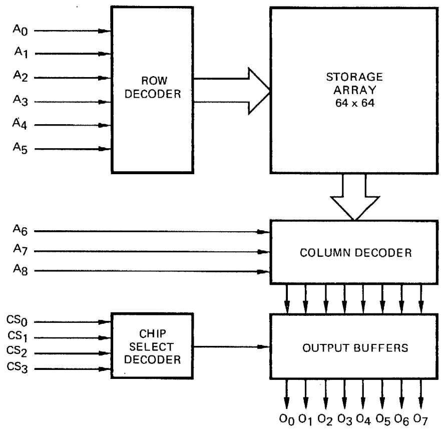
### FUNCTIONAL DESCRIPTION

The Am9214/Am3514 devices are high performance, 4096-bit, static, read only memories. Each memory is implemented as 512 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 512 words.

Four Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of up to 16 memories without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9214 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are identical to TTL specifications, providing simplified interfacing and standard worst-case noise immunity of 400mV. Only a single supply of +5 volts is required for power.

### BLOCK DIAGRAM

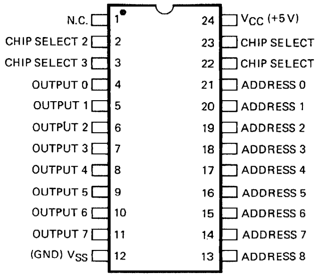

A0
A1
A2
A3
A4
A5
ROW DECODER
STORAGE ARRAY 64 x 64
A6
A7
A8
COLUMN DECODER
CS0
CS1
CS2
CS3
CHIP SELECT DECODER
OUTPUT BUFFERS
O0 O1 O2 O3 O4 O5 O6 O7

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | 0°C to +70°C | AM35141DC |
| Hermetic DIP | 0°C to +70°C | AM35142DC |
| Hermetic DIP | 0°C to +70°C | AM9214DC |
| Hermetic DIP | −55°C to +125°C | AM9214DM |

### CONNECTION DIAGRAM

Top View


N.C. 1
CHIP SELECT 2 2
CHIP SELECT 3 3
OUTPUT 0 4
OUTPUT 1 5
OUTPUT 2 6
OUTPUT 3 7
OUTPUT 4 8
OUTPUT 5 9
OUTPUT 6 10
OUTPUT 7 11
(GND) VSS 12
24 VCC (+5V)
23 CHIP SELECT 1
22 CHIP SELECT 0
21 ADDRESS 0
20 ADDRESS 1
19 ADDRESS 2
18 ADDRESS 3
17 ADDRESS 4
16 ADDRESS 5
15 ADDRESS 6
14 ADDRESS 7
13 ADDRESS 8

Note:
Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 10 to Pin 9) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from excessive accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to any voltages that exceed the maximum ratings.

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am9214DC
Am35141DC
Am35142DC

$T_A = 0°C$ to $+70°C$
$V_{CC} = +5V \pm 5\%$

| Parameters | Description | Test Conditions | Am9214 Min. | Am9214 Max. | Am3514 Min. | Am3514 Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC} = 4.75V$, $I_{OH} = 500\mu A$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC} = 4.75V$, $I_{OL} = 2.4mA$ | | 0.4 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$ | $V_{CC}-2.75$ | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | (See Note 1) | −0.5 | 0.8 | −0.5 | 0.55 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC} = 5.25V$, $0V \leq V_{IN} \leq 5.25V$ | | 1.0 | | 1.0 | μA |
| $I_{LO}$ | Output Leakage Current | Output OFF, $V_{OUT} = 0.4$ to $V_{CC}$ | | 1.0 | | 1.0 | μA |
| $I_{CC}$ | Power Supply Current | Data Out Open<br>$V_{CC} = 5.25V$<br>$V_{IN} = V_{CC}$ | | 50 | | 50 | mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am9214DM $T_A = -55°C$ to $+125°C$ $V_{CC} = +5V \pm 10\%$

| Parameters | Description | Test Conditions | Am9214 Min. | Am9214 Max. | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC} = 4.5V$, $I_{OH} = 500\mu A$ | 2.2 | $V_{CC}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC} = 4.5V$, $I_{OL} = 2.4mA$ | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | (See Note 1) | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC} = 5.5V$, $0V \leq V_{IN} \leq 5.5V$ | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | Output OFF, $V_{OUT} = 0.4$ to $V_{CC}$ | | 10 | μA |
| $I_{CC}$ | Power Supply Current | Data Out Open<br>$V_{CC} = 5.5V$<br>$V_{IN} = V_{CC}$ | | 70 | mA |

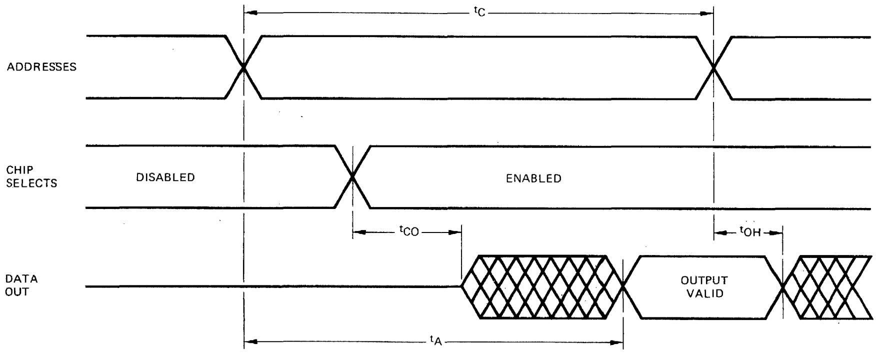
Notes: 1. Input Logic levels that swing more negative than −0.5 volts will be subject to clamping currents attempting to keep the input from falling.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Output Load: 1.5 TTL Gate +100pF for Am9214, 1.5 TTL Gate only for Am3514
Transition Times: 10ns
Input Levels: 0.8V and 2.0V
Output Reference: 1.5V

| Parameter | Description | Test Conditions | Am9214 Min. | Am9214 Max. | Am35141 Min. | Am35141 Max. | Am35142 Min. | Am35142 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_C$ | Cycle Time | | 500 | | | | | | ns |
| $t_A$ | Access Time | | | 500 | | 700 | | 1000 | ns |
| $t_{CO}$ | Chip Select to Output On Delay | | | 200 | | 500 | | 900 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 50 | | | | | | ns |
| $C_I$ | Input Capacitance | | | 6.0 | | 8.0 | | 8.0 | pF |
| $C_O$ | Output Capacitance | | | 10 | | 12 | | 12 | pF |

## TIMING DIAGRAM



### GLOSSARY OF TERMS

**Cycle Time** — Specifies the maximum rate at which new read operations may be initiated, and thus the minimum time between successive address changes.

**Access Time** — Maximum delay from the arrival of the last stable address line to valid output data on a selected chip.

**Output Enable Time ($t_{CO}$)** — Maximum delay from the arrival of four active Chip Select signals to enabled output data. Unselected chips will have high impedance outputs. Active level definition for each of the four chip Select inputs may be either high or low and is programmed along with the data pattern.

**Output Hold Time ($t_{OH}$)** — Minimum delay which will elapse between a change of the input address and any consequent change in the output data.

## PROGRAMMING INSTRUCTIONS

### CUSTOM PATTERN ORDERING INFORMATION

The Am9214 (or Am3514) is programmed on IBM cards, IBM coding form, or on paper tape in card image form in the format as shown below.

Logic "1" = a more positive voltage (normally +5.0V)
Logic "0" = a more negative voltage (normally 0V)

**FIRST CARD**

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data.<br>This is optional and should be left blank if not used. |
| 50 thru 62 | 9214 or 35141 or 35142 |
| 65 thru 72 | Date |

**SECOND CARD**

| Column Number | Description |
|---|---|
| 29 | CS$_3$ input required (0 or 1) to select chip. |
| 31 | CS$_2$ input required to select chip. |
| 33 | CS$_1$ input required to select chip. |
| 35 | CS$_0$ input required to select chip. |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in Binary form on a one-word-per-card basis. With this option, 512 more cards are required:

| Column Number | |
|---|---|
| 10, 12, 14, 16, 18 20, 22, 24, 26 | Address input pattern, the most significant bit (A$_8$) is in column 10. |
| 40, 42, 44, 46, 48, 50, 52, 54 | Output pattern, the most significant bit (O$_7$) is in column 40. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

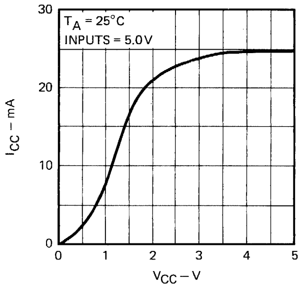
**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 32 data cards (see chart).

Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 1F: 32 cards in all. Data is also entered in hex values and may be any combination of 8 bits, that is, hex value from 00 through FF.

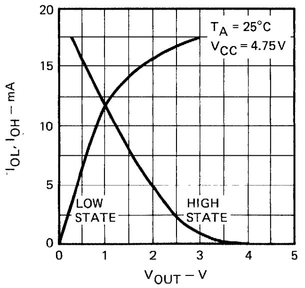
| ADDR | | | OUTPUT VALUES FOR ADDR + | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | | 1 | | 2 | | 3 | | 4 | | 5 | | 6 | | 7 | | 8 | | 9 | | A | | B | | C | | D | | E | | F |
| 21 | 22 | 23 | 30 31 | 32 | 33 34 | 35 | 36 37 | 38 | 39 40 | 41 | 42 43 | 44 | 45 46 | 47 | 48 49 | 50 | 51 52 | 53 | 54 55 | 56 | 57 58 | 59 | 60 61 | 62 | 63 64 | 65 | 66 67 | 68 | 69 70 | 71 | 72 73 | 74 | 75 76 |
| 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 3 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 4 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 5 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 7 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 8 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 9 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | A | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | B | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | C | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | D | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | E | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | F | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 3 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 4 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 5 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 6 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 7 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 8 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 9 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | A | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | B | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | C | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | D | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | E | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | F | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## Am9214 PERFORMANCE CURVES

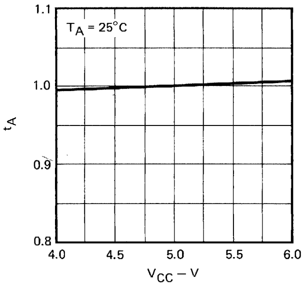
**Typical Power Supply Current Versus Voltage**



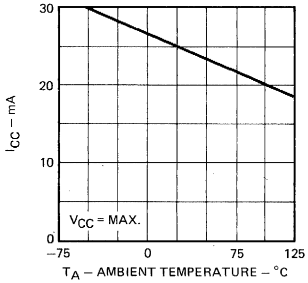
**Typical Output Current Versus Voltage**



**Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ at 5.0V**

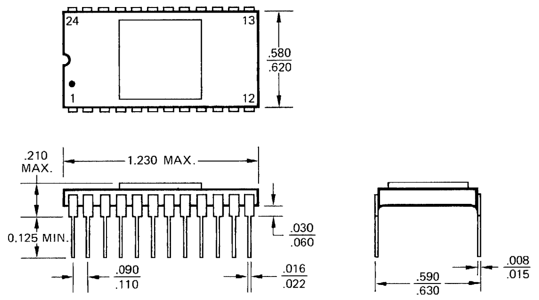


**Typical Power Supply Current Versus Ambient Temperature**



## PHYSICAL DIMENSIONS
### Dual-In-Line

**24-Pin Side-Brazed**


24
13
1
12
.580
.620
.210
MAX.
1.230 MAX.
0.125 MIN.
.030
.060
.090
.110
.016
.022
.590
.630
.008
.015

# Am9216

## 2048 x 8 Read Only Memory

### DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- High speed – 300 ns access time
- Fully capacitive inputs – simplified driving
- 2 fully programmable chip selects – increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers – simplified expansion
- Standard supply voltages – +12V, +5.0V
- No $V_{BB}$ supply required
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

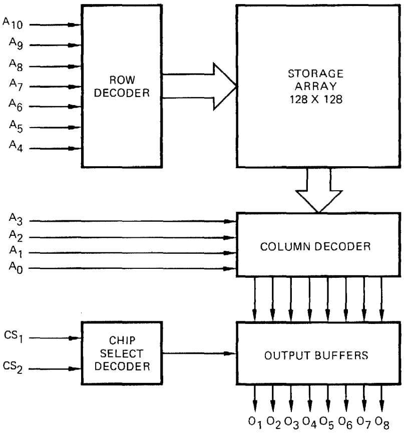
### FUNCTIONAL DESCRIPTION

The Am9216 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9216 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. The Am9216 is pin compatible with the Am9208 which is an 8k-bit mask programmed ROM. Input and output voltage levels are compatible with TTL specifications.

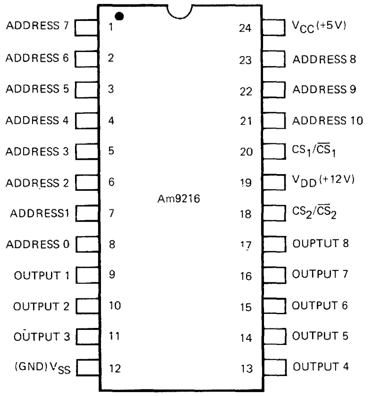
### BLOCK DIAGRAM



$A_{10}$
$A_9$
$A_8$
$A_7$
$A_6$
$A_5$
$A_4$
ROW DECODER
STORAGE ARRAY 128 X 128
$A_3$
$A_2$
$A_1$
$A_0$
COLUMN DECODER
$CS_1$
$CS_2$
CHIP SELECT DECODER
OUTPUT BUFFERS
$O_1$ $O_2$ $O_3$ $O_4$ $O_5$ $O_6$ $O_7$ $O_8$

### CONNECTION DIAGRAM

### Top View



ADDRESS 7 1
ADDRESS 6 2
ADDRESS 5 3
ADDRESS 4 4
ADDRESS 3 5
ADDRESS 2 6
ADDRESS1 7
ADDRESS 0 8
OUTPUT 1 9
OUTPUT 2 10
OUTPUT 3 11
(GND) $V_{SS}$ 12
24 $V_{CC}$ (+5V)
23 ADDRESS 8
22 ADDRESS 9
21 ADDRESS 10
20 $CS_1/\overline{CS}_1$
19 $V_{DD}$ (+12V)
18 $CS_2/\overline{CS}_2$
17 OUPTUT 8
16 OUTPUT 7
15 OUTPUT 6
14 OUTPUT 5
13 OUTPUT 4
Am9216

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specifications | Access Time | |
|---|---|---|---|
| | | 400 ns | 300 ns |
| Hermetic DIP | $0^\circ C \leq T_A \leq 70^\circ C$ | AM9216BDC | AM9216CDC |
| | $-55^\circ C \leq T_A \leq 125^\circ C$ | AM9216BDM | |

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{DD}$ with Respect to $V_{SS}$ | 15V |
| $V_{CC}$ with Respect to $V_{SS}$ | +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{DD}$ | $V_{CC}$ | $V_{SS}$ |
|---|---|---|---|---|
| Am9216DC | $0°C \leq T_A \leq +70°C$ | +12V ± 5% | +5.0V ± 5% | 0V |
| Am9216DM | $-55°C \leq T_A \leq +125°C$ | +12V ± 10% | +5.0V ± 10% | 0V |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions | | Am9216DC Min. | Am9216DC Max. | Am9216DM Min. | Am9216DM Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -1.0mA$ | | 3.7 | | 3.7 | | Volts |
| | | $I_{OH} = -4.0mA$ | | 2.4 | | 2.4 | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | 0.4 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.4 | $V_{CC}+1.0$ | 2.6 | $V_{CC}+1.0$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | 0.8 | −0.5 | 0.8 | Volts |
| $I_{LO}$ | Output Leakage Current | Chip disabled | | | 10 | | 10 | μA |
| $I_{LI}$ | Input Leakage Current | | | | 10 | | 10 | μA |
| $I_{DD}$ | $V_{DD}$ Supply Current | Selected | Am9216B | | 42 | | 47 | mA |
| | | | Am9216C | | 49 | | | |
| | | Deselected | Am9216B | | 52 | | 57 | |
| | | | Am9216C | | 60 | | | |
| $I_{CC}$ | $V_{CC}$ Supply Current | | Am9216B | | 13 | | 15 | mA |
| | | | Am9216C | | 15 | | | |

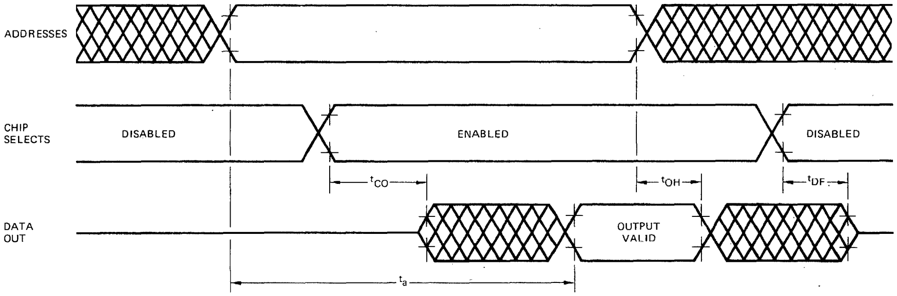
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

**Am9216BDC, Am9216BDM, Am9216CDC**

| Parameters | Description | Test Conditions | Am9216DC/DM Min. | Am9216DC/DM Max. | Am9216CDC Min. | Am9216CDC Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_a$ | Address to Output Access Time | $t_r = t_f = 20ns$<br>Output load:<br>one standard TTL gate plus 100pF (Note 1) | | 400 | | 300 | ns |
| $t_{CO}$ | Chip Select to Output ON Delay | | | 160 | | 140 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | ns |
| $t_{DF}$ | Chip Select to Output OFF Delay | | | 120 | | 100 | ns |
| $C_I$ | Input Capacitance | $T_A = 25°C$, f = 1.0MHz<br>All pins at 0V | | 6.0 | | 6.0 | pF |
| $C_O$ | Output Capacitance | | | 6.0 | | 6.0 | pF |

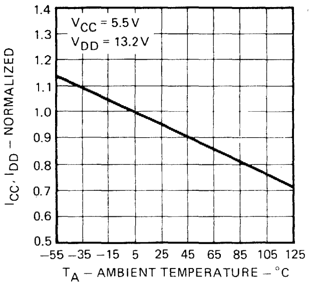
Notes: 1. Timing reference levels — Inputs: High = 2.0V, Low = 1.0V.
Outputs: High = 2.4V, Low = 0.8V.

## SWITCHING WAVEFORMS

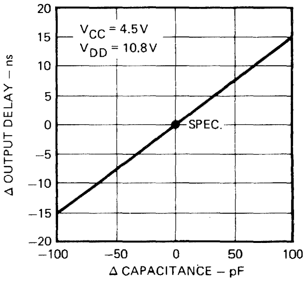


## TYPICAL CHARACTERISTICS

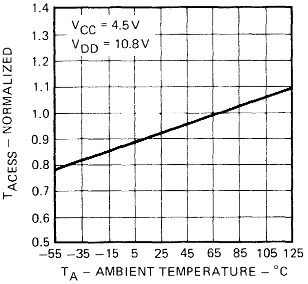
**$I_{DD}$, $I_{CC}$ Versus Temperature (Normalized)**



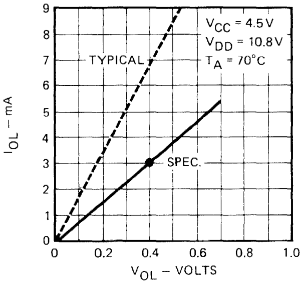
**Δ Output Capacitance Versus Δ Output Delay**



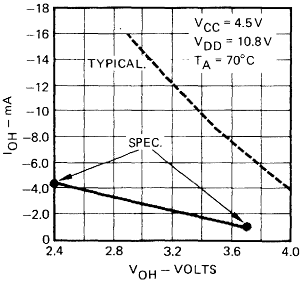
**$T_{Access}$ Versus Temperature (Normalized)**



**$I_{OL}$ Versus $V_{OL}$**



**$I_{OH}$ Versus $V_{OH}$**



## PROGRAMMING INSTRUCTIONS

### CUSTOM PATTERN ORDERING INFORMATION

The Am9216 is programmed from punched cards, card coding forms or from paper tape in card image form in the format as shown below.

Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0V)

### FIRST CARD

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data.<br>This is optional and should be left blank if not used. |
| 50 thru 62 | 9216B or 9216C |
| 65 thru 72 | Data |

### SECOND CARD

| Column Number | Description |
|---|---|
| 31 | $CS_2$ input required to select chip (0 or 1) |
| 33 | $CS_1$ input required to select chip (0 or 1) |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

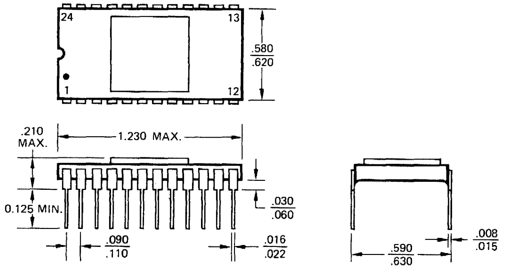
| Column Number | |
|---|---|
| 10, 12, 14, 16, 18<br>20, 22, 24, 26, 28, 30 | Address input pattern with the most significant bit ($A_{10}$) in column 10 and the least significant bit ($A_0$) in column 30. |
| 40, 42, 44, 46, 48,<br>50, 52, 54 | Output pattern with the most significant bit ($O_8$) in column 40 and the least significant bit ($O_1$) in column 54. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data in entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.

| ADDR | | | OUTPUT VALUES FOR ADDR + | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | | | 1 | | | 2 | | | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | | 8 | | | 9 | | | A | | | B | | | C | | | D | | | E | | | F | |
| 21 | 22 | 23 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 |
| 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| •<br>•<br>• | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | F | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| •<br>•<br>• | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | F | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| •<br>•<br>• | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | F | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

## PHYSICAL DIMENSIONS

### Dual-In-Line
### 24-Pin Side Brazed



# Shift Registers

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| Am1403A | Dual 512-Bit Dynamic | 5-9 |
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| Am1405A | Single 512-Bit Dynamic | 5-15 |
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| Am1407 | Dual 100-Bit Dynamic | 5-3 |
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| Am4057/5057 | Single 512-Bit Static | 5-57 |
| Am9401 | Dual 1024-Bit Dynamic | 5-61 |

# SHIFT REGISTERS
# SELECTION GUIDE

| Part Number | Organization | Mode | Speed (MHz) | Supply Voltages | Clock Phases | TTL Clocks | Recirc. Logic | Pins | Output |
|---|---|---|---|---|---|---|---|---|---|
| Am1506/1507 | Dual 100 | Dynamic | 2 | +5, –5 | Two | No | No | 8 | Single Ended |
| AM2802 | Quad 256 | Dynamic | 10 | +5, –5 | Two | No | No | 16 | Single Ended |
| Am2803 | Dual 512 | Dynamic | 10 | +5, –5 | Two | No | No | 8 | Single Ended |
| Am2804 | Single 1024 | Dynamic | 10 | +5, –5 | Two | No | No | 8 | Single Ended |
| Am2805/2807 | Single 512 | Dynamic | 4 | +5, –5 | Two | No | Yes | 10/8 | Single Ended |
| Am2806/2808 | Single 1024 | Dynamic | 4 | +5, –5 | Two | No | Yes | 10/8 | Single Ended |
| Am2825/2826 | Dual 1024 | Dynamic | 6 | +5,–10.5 | Two | No | Yes | 10/16 | Push-Pull |
| Am2827 | Single 2048 | Dynamic | 6 | +5,–10.5 | Two | No | Yes | 8 | Push-Pull |
| Am9401 | Dual 1024 | Dynamic | 2 | +5 | One | Yes | Yes | 16 | Single Ended |
| Am2809 | Dual 128 | Static | 2.5 | +5,–12 | One | Yes | Yes | 8 | Push-Pull |
| Am2810 | Dual 128 | Static | 2 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |
| Am2814 | Dual 128 | Static | 2.5 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |
| Am2833 | Single 1024 | Static | 2 | +5,–12 | One | Yes | Yes | 8 | Push-Pull |
| Am2847 | Quad 80 | Static | 3 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |
| Am2855 | Quad 128 | Static | 2.5 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |
| Am2856 | Dual 256 | Static | 2.5 | +5,–12 | One | Yes | Yes | 10 | Push-Pull |
| Am2857 | Single 512 | Static | 2.5 | +5,–12 | One | Yes | Yes | 8 | Push-Pull |
| Am2896 | Quad 96 | Static | 3 | +5,–12 | One | Yes | Yes | 16 | Push-Pull |

# Am14/1506 • Am14/1507

## Dual 100-Bit Dynamic Shift Registers

**Distinctive Characteristics**

- Dual 100-bit silicon gate MOS shift registers
- DTL and TTL compatible
- Low-power dissipation of 0.4 mW/bit at 1 MHz
- 2 MHz frequency operation guaranteed
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products

### FUNCTIONAL DESCRIPTION

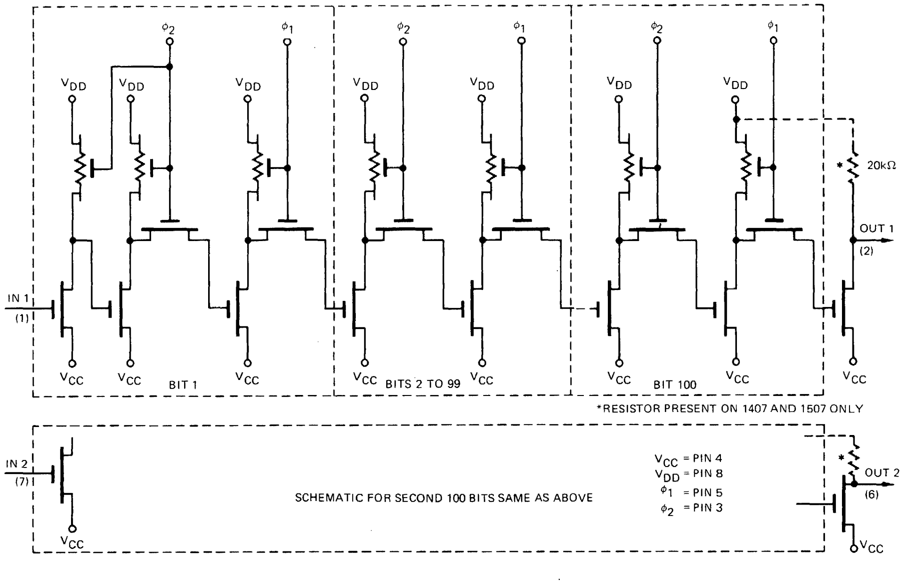
The Advanced Micro Devices dual 100-bit dynamic MOS shift registers are built using enhancement mode P-channel silicon gate MOS devices. The circuits use low-voltage circuitry for low-power dissipation and ease of interfacing into bipolar DTL and TTL circuits.

The shift registers can be driven by either DTL or TTL circuits or by MOS circuits and provide driving capability to MOS or bipolar circuits.

Silicon gate technology gives high–speed operation, low-power dissipation and low clock input capacitance

The shift registers are ideal for low-cost buffer memories, long serial digital delay lines, etc. The devices are available in the commercial (0°C to +70°C) temperature range and the military (–55°C to +125°C) temperature range and are available with open drain output (Am14/1506), or with a 20kΩ pull-down resistor (Am14/1507) for easier interface to other circuitry.

### CIRCUIT DIAGRAM


$\phi_2$
$\phi_1$
$V_{DD}$
IN 1
(1)
$V_{CC}$
BIT 1
BITS 2 TO 99
BIT 100
20kΩ
OUT 1
(2)
IN 2
(7)
OUT 2
(6)
SCHEMATIC FOR SECOND 100 BITS SAME AS ABOVE

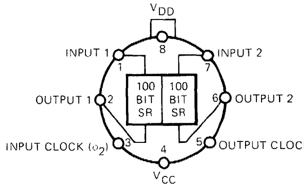
*RESISTOR PRESENT ON 1407 AND 1507 ONLY

$V_{CC}$ = PIN 4
$V_{DD}$ = PIN 8
$\phi_1$ = PIN 5
$\phi_2$ = PIN 3

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Output Resistor | Part Number |
|---|---|---|---|
| TO-99 | $0°C \leqslant T_A \leqslant +70°C$ | No | AM1506 |
| | | Yes | AM1507 |
| | $-55°C \leqslant T_A \leqslant +125°C$ | No | AM1406 |
| | | Yes | AM1407 |

### CONNECTION DIAGRAM
Top View


$V_{DD}$
INPUT 1
INPUT 2
OUTPUT 1
OUTPUT 2
INPUT CLOCK ($\phi_2$)
OUTPUT CLOCK ($\phi_1$)
$V_{CC}$
100 BIT SR
100 BIT SR
1
2
3
4
5
6
7
8

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Power Dissipation | 500 mW |
| Data and Clock Input Voltages with respect to most Positive Supply Voltage, $V_{CC}$ | +0.5 V to −25 V |
| Power Supply Voltage, $V_{DD}$ with respect to $V_{CC}$ | +0.5 V to −25 V |

## ELECTRICAL CHARACTERISTICS

Am1506/1507 $T_A = 0°C$ to $+70°C$
Am1406/1407 $T_A = -55°C$ to $+125°C$ } unless otherwise specified

### DC Characteristics

Over Operating Temperature Range ($V_{DD} = -5.0$ V ±5%, $V_{CC} = +5.0$ V ±5% unless otherwise specified)

| | | Limits Over Specified Temperature Range | | | |
|---|---|---|---|---|---|
| **Parameters** | **Test Conditions** | **Min.** | **Typ.** (Note 1) | **Max.** | **Units** |
| **$V_{OH}$** (Note 2) Output HIGH Voltage | $I_{OH} = -2.5$ mA<br>Load = 20 kΩ | 2.5 | 4.0 | | Volts |
| **$V_{OL}$** (Note 2) Output LOW Voltage | $I_{OL} = 200$ μA<br>1407, 1507 only | | −1.2 | 0.4 | Volts |
| **$V_{IH}$** Input HIGH Voltage | $V_{DD} = -5.0$ V<br>$V_{CC} = +5.0$ V | 2.5 | 5.0 | 5.3 | Volts |
| **$V_{IL}$** Input LOW Voltage | $V_{DD} = -5.0$ V<br>$V_{CC} = +5.0$ V | −10 | 0.2 | 0.8 | Volts |
| **$V_{IHC}$** Clock Input HIGH Voltage | $V_{DD} = -5.0$ V<br>$V_{CC} = +5.0$ V | 3.5 | | 5.3 | Volts |
| **$V_{ILC}$** Clock Input LOW Voltage | $V_{DD} = -5.0$ V<br>$V_{CC} = +5.0$ V | −13 | | −9.5 | Volts |
| **$I_L$** Input Load Current | Input Pin 1: Pins 2, 3, 4, 5, 6, 7 = 0 V, Pin 1 = −18 V, Pin 8 = −8 V, $T_A = 25°C$<br>Input Pin 7: Pins 1, 2, 3, 4, 5, 6 = 0 V, Pin 7 = −18 V, Pin 8 = −8 V, $T_A = 25°C$ | | | 500 | nA |
| **$I_{LC}$** Clock Input Current | Clock Input Pins 3, 5 = −18 V<br>All Other Pins = 0 V, $T_A = 25°C$ | | | 500 | nA |
| **$I_{LO}$** (Note 3) Output Leakage Current | Output Pin 2: Pins 1, 4, 6, 7, 8 = 0 V, Pin 2 = −18 V, Pins 3, 5 = −8 V<br>Output Pin 6: Pins 1, 2, 4, 7, 8 = 0 V, Pin 6 = −18 V, Pins 3, 5 = −8 V | | | 500 | nA |
| **$I_{DD}$** (See Graphs) Power Supply Current (Note 4) | f = 1MHz, Duty Cycle = 60%, $T_A = 25°C$ | | 4.0 | 8.0 | mA |
| | f = 1MHz, Duty Cycle = 60%, $T_A = 0°C$ | | 5.0 | 10 | mA |
| | f = 1MHz, Duty Cycle = 60%, $T_A = -55°C$ | | 8.0 | 13 | mA |
| **$Z_{out}$** Output ON Impedance | $V_{DD} = -5.0$ V, $V_{CC} = +5.0$ V, $I_{OH} = -2.5$ mA | | 300 | 750 | Ω |
| **$C_{IN}$** * Input Capacitance | Input Pins 1, 7<br>$V_{IN} = V_{CC}$ | | | 4 | pF |
| **$C\phi$** * Clock Input Capacitance | Clock Input Pins 3, 5 $V\phi = V_{CC}$ | | | 40 | pF |
| | Clock Input Pins 3, 5 $V\phi = -20$ V Bias | | | 35 | pF |
| **$C_{out}$** (Note 4) * Output Capacitance | Output Pins 2, 6<br>$V_{out} = V_{CC}$ | | | 5 | pF |

**Note 1:** Typical values are at $V_{CC} - V_{DD} = 10$ V and $T_A = 25°C$.

**Note 2:** In the logic HIGH level the MOS register output can supply 2.5 mA into the load combination of the internal pull-down resistor and the external load. In the logic LOW level, $I_{OL}$ represents the current the internal 20 kΩ resistor will sink. In order to insure current sinking capability for one standard TTL load, an external pull-down resistor must be added. See applications.

**Note 3:** Leakage current for 1406 and 1506 only. For 1407 and 1507 the output on pins 2 and 6 will exhibit a resistance when measured with the following bias conditions: pins 1, 6, and 8 at GND; pins 3 and 5 at −16 V; pin 4 open; measure pins 2 and 6. $25\ k\Omega \geq R_{OUT} \geq 15\ k\Omega$.

**Note 4:** Power dissipation is directly proportional to clock duty cycle. Duty cycle is defined as: clock frequency ($t\phi_1pw + t\phi_2pw + \frac{1}{2}[t_r + t_f]$).

***This paramenter is periodically sampled and is not 100% tested.**

## SWITCHING CHARACTERISTICS ($V_{DD} = -5$ V ±5%; $V_{CC} = +5$ V ±5% unless otherwise specified)

| Parameter | Description | Test Conditions | Limits Over Specified Temperature Range | | Units |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $f_c$ | Clock Frequency | $V_{IH} \geq 3.0$ V | (Note 5) | 2 | MHz |
| | | $V_{IH} \geq 2.5$ V | | 1 | |
| $t_{\phi PW}$ | Clock Pulse Width | $V_{IH} \geq 3.0$ V | 130 | | ns |
| | | $V_{IH} \geq 2.5$ V | 200 | | |
| $t_{\phi d}$ | Clock Pulse Delay | $\phi_{1\ PW} = 0.4\ \mu s$<br>$\phi_{2\ PW} = 0.2\ \mu s$ $f_c = 1$ MHz | 100 | | ns |
| $t_f$, $t_r$ | Clock Pulse Rise/Fall Time | $f_c = 1$ MHz | | 50 | ns |
| $t_s$ | Input Data Set Up Time | $f_c = 2$ MHz | 100 | | ns |
| | | $f_c = 1$ MHz | 200 | | |
| $t_h$ | Input Data Hold Time | | 100 | | ns |
| $t_{pd}$ | Propagation Delay<br>$\phi_1$ to Output | $V_{ILC} - V_{CC} = -16$ V | | 100 | ns |

**Note 5:** See "Minimum Operating Frequency" graph for low limits on clock rate.

## DESCRIPTION OF TERMS

### OPERATIONAL TERMS

**$V_{OH}$** Minimum logic HIGH output voltage with output HIGH current $I_{OH}$ flowing out of output.

**$V_{OL}$** Maximum logic LOW output voltage with output LOW current $I_{OL}$ into output.

**$V_{IH}$** Logic HIGH input voltage.

**$V_{IL}$** Logic LOW input voltage.

**$V_{ILC}$** Clock LOW input voltage.

**$V_{IHC}$** Clock HIGH input voltage.

**$I_L$** Input load current.

**$I_{LO}$** Output leakage current.

**$I_{DD}$** Power supply current.

**$Z_{out}$** Output impedance with output sourcing 2.5 mA.

**$C_{IN}$** Input capacitance.

**$C\phi$** Input clock capacitance.

**$C_{OUT}$** Output capacitance.

### FUNCTIONAL TERMS

$\phi_1$, $\phi_2$ The two clock phases required by the dynamic shift register.

**$f_c$** The clock frequency of the shift register.

### SWITCHING TERMS

**$t_{\phi d}$** The delay between the LOW to HIGH transition of a clock phase to the HIGH to LOW transition of the other clock phase.

**$t_{\phi PW}$** The clock pulse widths necessary for correct operation.

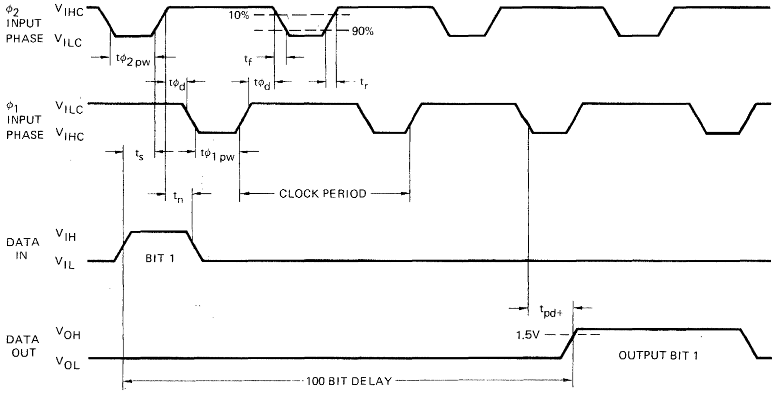
**$t_f$, $t_r$** The clock pulse rise and fall times necessary for correct operation.

**$t_s$** The time required for the input data to be present prior to the LOW to HIGH transition of the clock phase $\phi_2$ to ensure correct operation.

**$t_h$** The time required for the input data to remain present after the LOW to HIGH transition of the clock phase $\phi_2$ to ensure correct operation.

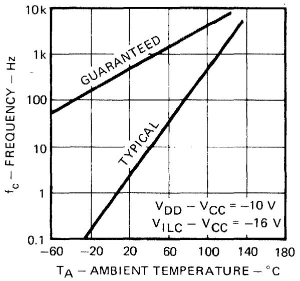
**$t_{pd+}$** The propagation delay from the HIGH to LOW clock phase $\phi_1$ transition to the output LOW to HIGH transition.

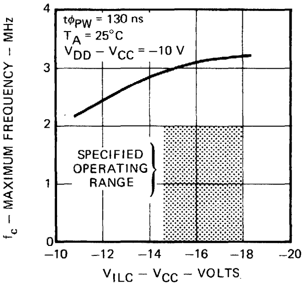
## SWITCHING WAVEFORMS


φ2 INPUT PHASE
$V_{IHC}$
$V_{ILC}$
10%
90%
$t_{\phi 2\,pw}$
$t_f$
$t_{\phi d}$
$t_{\phi d}$
$t_r$
φ1 INPUT PHASE
$V_{ILC}$
$V_{IHC}$
$t_s$
$t_{\phi 1\,pw}$
$t_n$
CLOCK PERIOD
DATA IN
$V_{IH}$
$V_{IL}$
BIT 1
$t_{pd+}$
DATA OUT
$V_{OH}$
$V_{OL}$
1.5V
OUTPUT BIT 1
100 BIT DELAY

Clock Rise Time 10ns
Clock Fall Time 10ns
Data Amplitude +0.8V to +2.5V
Output Load 1 TTL Unit Load

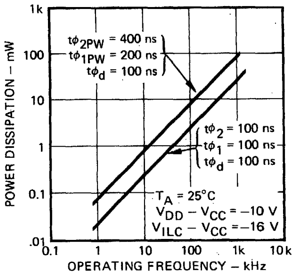
## SWITCHING CHARACTERISTICS


**Minimum Operating Frequency Versus Temperature**

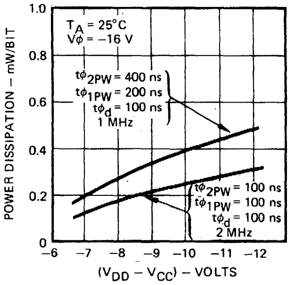

**Maximum Frequency Versus Clock Amplitude**

## SWITCHING CHARACTERISTICS

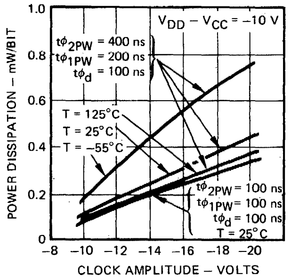
### Power Dissipation Versus Frequency



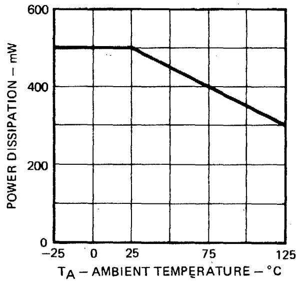
### Power Dissipation/Bit Versus Supply Voltage



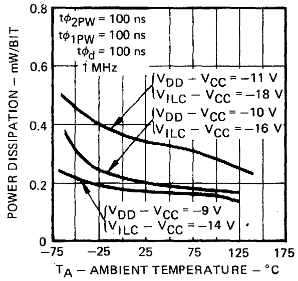
### Power Dissipation/Bit Versus Clock Amplitude



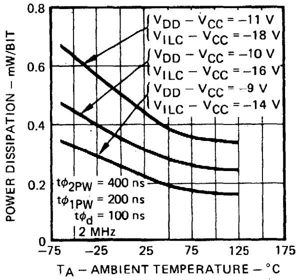
### Maximum Package Power Dissipation Versus Temperature



### Power Dissipation/Bit at 2 MHz Versus Temperature



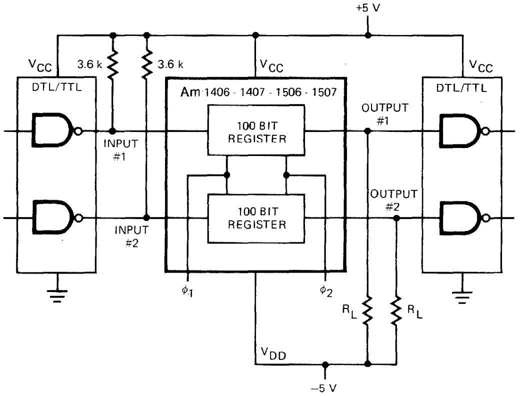
### Power Dissipation/Bit at 1 MHz Versus Temperature



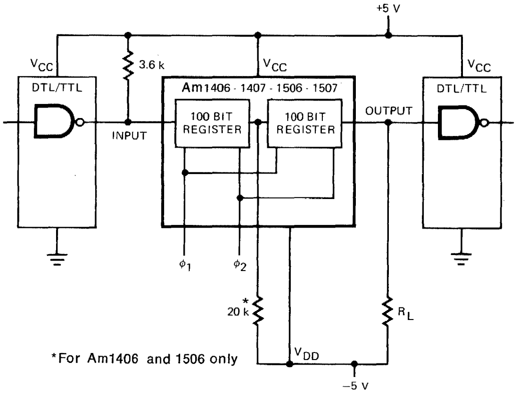
## APPLICATIONS

### DTL/TTL/MOS Interfaces

**Dual 100-Bit Delay**


+5 V
V_CC
3.6 k
3.6 k
V_CC
V_CC
DTL/TTL
Am 1406 · 1407 · 1506 · 1507
DTL/TTL
OUTPUT #1
100 BIT REGISTER
INPUT #1
OUTPUT #2
100 BIT REGISTER
INPUT #2
φ1
φ2
R_L
R_L
V_DD
–5 V

**200-Bit Delay**

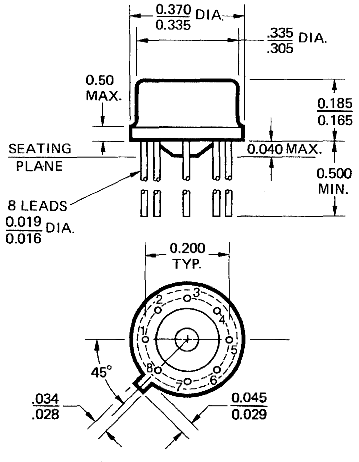

+5 V
V_CC
3.6 k
V_CC
V_CC
DTL/TTL
Am1406 · 1407 · 1506 · 1507
DTL/TTL
100 BIT REGISTER
100 BIT REGISTER
OUTPUT
INPUT
φ1
φ2
*
20 k
R_L
V_DD
–5 V

*For Am1406 and 1506 only

**Value of $R_L$ ($V_{DO}$ = –5.0 ±5%)**

| Gate Type | 1406, 1506 | 1407, 1507 |
|---|---|---|
| Standard TTL | 3.2k | 3.8k |
| 93L Low Power | 12.8k | 35k |
| 74L Low Power | 28k | none required |

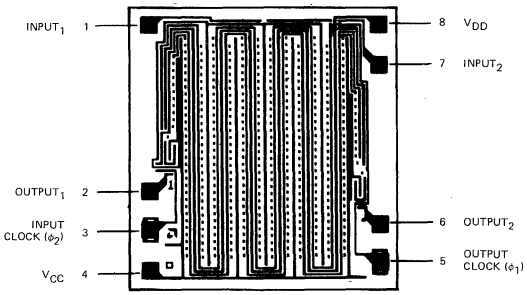
## PHYSICAL DIMENSIONS
## (In Accordance with JEDEC TO-99)


0.370 / 0.335 DIA.
.335 / .305 DIA.
0.50 MAX.
0.185 / 0.165
SEATING PLANE
0.040 MAX.
0.500 MIN.
8 LEADS
0.019 / 0.016 DIA.
0.200 TYP.
1
2
3
4
5
6
7
8
45°
.034 / .028
0.045 / 0.029

NOTES: (1) All dimensions in inches.
(2) Leads are gold-plated Kovar.

## Metallization and Pad Layout

69 x 74 Mils


INPUT₁ 1
OUTPUT₁ 2
INPUT CLOCK (φ2) 3
V_CC 4
8 V_DD
7 INPUT₂
6 OUTPUT₂
5 OUTPUT CLOCK (φ1)

# Am1402A/Am1403A/Am1404A
# Am2802/Am2803/Am2804

### 1024-Bit Dynamic Shift Registers

## Distinctive Characteristics

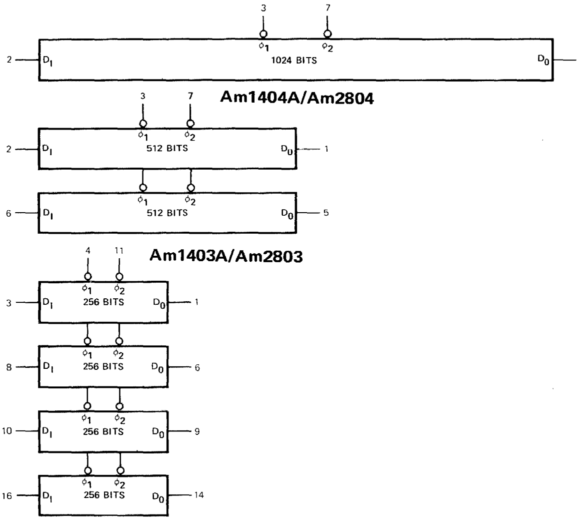
- Quad 256-bit, dual 512-bit, single 1024-bit
- 10 MHz frequency operation guaranteed for Am2802, Am2803 and Am2804.
- Low power dissipation of 0.1 mW/bit at 1 MHz
- DTL and TTL compatible
- Both military and commercial grade devices available
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for the assemblers of hybrid products

## FUNCTIONAL DESCRIPTION

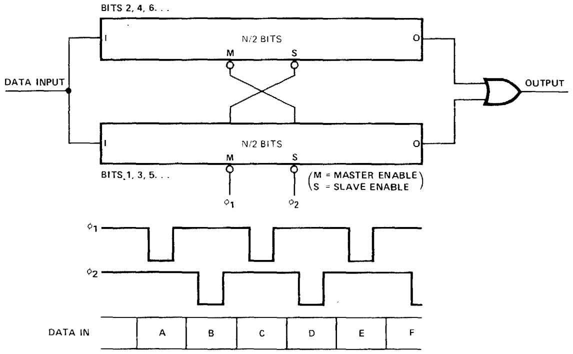
The Am1402A, 3A, and 4A are 1024-bit silicon gate dynamic shift registers. The low threshold characteristics of this technology allow high-speed operation and DTL and TTL compatibility. The Am1402A is a quad 256-bit device; the Am1403A is a dual 512-bit register; and the Am1404A is a single 1024-bit register. All three devices require two-phase non-overlapping clocks, and provide a one-bit shift on each clock pulse. The Am2802, 3, and 4 registers are functionally identical to the Am1402A, 3A, and 4A, but are guaranteed to operate over frequencies from 400Hz to 10MHz.

## BLOCK DIAGRAMS

**Am1402A/1403A/1404A Shift Registers**


3
7
$\phi_1$
$\phi_2$
2
$D_I$
1024 BITS
$D_O$
5
Am1404A/Am2804
3
7
$\phi_1$
$\phi_2$
2
$D_I$
512 BITS
$D_O$
1
$\phi_1$
$\phi_2$
6
$D_I$
512 BITS
$D_O$
5
Am1403A/Am2803
4
11
$\phi_1$
$\phi_2$
3
$D_I$
256 BITS
$D_O$
1
8
$D_I$
256 BITS
$D_O$
6
10
$D_I$
256 BITS
$D_O$
9
16
$D_I$
256 BITS
$D_O$
14
Am1402A/Am2802

**Functional Equivalent of Each Register**


BITS 2, 4, 6. . .
I
N/2 BITS
O
M
S
DATA INPUT
OUTPUT
I
N/2 BITS
O
M
S
BITS 1, 3, 5. . .
M = MASTER ENABLE
S = SLAVE ENABLE
$\phi_1$
$\phi_2$
$\phi_1$
$\phi_2$
DATA IN
A
B
C
D
E
F

Since the two registers shift on opposite clock pulses, a new data bit is entered on both $\phi_1$ and $\phi_2$. Data entering the register on $\phi_1$ will appear at the output on $\phi_1$ (from the negative edge of $\phi_1$ to the negative edge of $\phi_2$).

## ORDERING INFORMATION

| Part Number | Package Type | Temperature Range | Standard Speed Range Order Number | Extended Speed Range Order Number |
|---|---|---|---|---|
| Am1402A/ 2802 | Hermetic DIP | 0°C to +70°C | AM1402A | AM2802DC |
| | Hermetic DIP | –55°C to+125°C | AM1402ADM | AM2802DM |
| | Molded DIP | 0°C to +70°C | AM1402APC | AM2802PC |
| Am1403A/ 2803 | TO-99 | 0°C to +70°C | AM1403A | AM2803HC |
| | TO-99 | –55°C to +125°C | AM1403AHM | AM2803HM |
| | Molded DIP | 0°C to +70°C | AM1403APC | AM2803PC |
| Am1404A/ 2804 | TO-99 | 0°C to +70°C | AM1404A | AM2804HC |
| | TO-99 | –55°C to +125°C | AM1404AHM | AM2804HM |
| | Mini DIP Plastic | 0°C to +70°C | AM1404APC | AM2804PC |

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature Under Bias | −55°C to +125°C |
| Power Dissipation (Note 1) | 600 mW |
| Data and Clock Input Voltages with respect to most Positive Supply Voltage, $V_{CC}$ | 0.3 V to −20 V |
| Power Supply Voltage, $V_{DD}$ with respect to $V_{CC}$ | 0.3 V to −20 V |

## OPERATING RANGE

| Part Number | $V_{CC}$ | $V_{DD}$ | Temperature Range |
|---|---|---|---|
| Am1402A, Am1403A, Am1404A | 5V ±5% | −4.75V to −9.45V | 0°C to +70°C |
| Am1402ADM, Am1403AHM, Am1404AHM | 5V ±5% | −4.75V to −9.45V | −55°C to +125°C |
| Am2802DC, Am2803HC, Am2804HC | 5V ±5% | −5V ±5% | 0°C to +70°C |
| Am2802DM, Am2803HM, Am2804HM | 5V ±5% | −5V ±5% | −55°C to +125°C |

## ELECTRICAL CHARACTERISTICS over operating range

| | | | | Am1402A, 3A, 4A | | | Am2802, 3, 4 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Parameters | Description | Test Conditions | | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
| $V_{IH}$ | Input HIGH Voltage | | | $V_{CC}-2.0$ | | | $V_{CC}-2.0$ | | | V |
| $V_{IL}$ | Input LOW Voltage | | | $V_{CC}-10$ | | $V_{CC}-4.2$ | $V_{CC}-10$ | | $V_{CC}-4.2$ | V |
| $I_I$ | Input Current | $T_A = 25°C$ | | | <10 | 500 | | <10 | 500 | nA |
| $I_O$ | Output Leakage Current | $T_A = 25°C$, $V_{OUT} = 0V$ | | | <10 | 1000 | | <10 | 1000 | nA |
| $I_{\phi L}$ | Clock Leakage Current | $T_A = 25°C$, $V_\phi = -12V$ | | | 10 | 1000 | | 10 | 1000 | nA |
| $V_{OH}$ | Output HIGH Voltage Driving TTL | $R_L = 3k$ to $V_{DD}$,<br>$V_{DD} = -5V \pm 5\%$ | | 2.4 | 3.5 | | $V_{CC}-1.9$ | $V_{CC}-1$ | | V |
| | Output HIGH Voltage Driving MOS | $R_L = 4.7k$ to $V_{DD}$,<br>$V_{DD} = -5V \pm 5\%$ | | $V_{CC}-1.9$ | $V_{CC}-1$ | | $V_{CC}-1.9$<br>(Note 2) | $V_{CC}-1$<br>(Note 2) | | |
| | Output HIGH Voltage Driving TTL | $R_L = 4.7k$ to $V_{DD}$,<br>$V_{DD} = -9V \pm 5\%$ | | 2.4 | 3.5 | | | | | |
| | Output HIGH Voltage Driving MOS | $R_L = 6.2k$ to $V_{DD}$, 3.9k to $V_{CC}$<br>$V_{DD} = -9V \pm 5\%$ | | $V_{CC}-1.9$ | $V_{CC}-1$ | | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{DD} = -5V \pm 5\%$,<br>$R_L = 3k$ to $V_{DD}$, $I_{OL} = -1.6mA$ | | | −0.3 | 0.5 | | −0.3 | 0.5 | V |
| | | $R_L = 4.7k$ to $V_{DD}$<br>$V_{DD} = -9V \pm 5\%$, $I_{OL} = -1.6mA$ | | | −0.3 | 0.5 | | | | |
| $V_{\phi H}$ | Clock Input HIGH Level | | | $V_{CC}-1$ | | $V_{CC}+0.3$ | $V_{CC}-1$ | | $V_{CC}+0.3$ | V |
| $V_{\phi L}$ | Clock Input LOW Level | $V_{DD} = -5V \pm 5\%$ | | $V_{CC}-15$ | | $V_{CC}-17$ | $V_{CC}-15$ | | $V_{CC}-17$ | V |
| | | $V_{DD} = -9V \pm 5\%$ | | $V_{CC}-12.6$ | | $V_{CC}-14.7$ | $V_{CC}-12.6$ | | $V_{CC}-14.7$ | |
| $I_{DD}(-5)$<br>(Note 1) | $V_{DD}$ Current, $V_{DD} = -5V \pm 5\%$ | 5MHz Data Rate | $T_A = 25°C$ | | 40 | 50 | | 40 | 50 | mA |
| | | 33% Duty Cycle | $T_A = 0°C$ | | | 56 | | | 56 | |
| | | $V_{\phi L} = V_{CC}-17V$ | $T_A = -55°C$ | | | | | | 70 | |
| | $V_{DD}$ Current, $V_{DD} = -5V \pm 5\%$ | 10MHz Data Rate | $T_A = 25°C$ | | | | | 50 | 60 | mA |
| | | 40% Duty Cycle | $T_A = 0°C$ | | | | | | 68 | |
| | | $V_{\phi L} = V_{CC}-17$ | $T_A = -55°C$ | | | | | | 80 | |
| $I_{DD}(-9)$<br>(Note 1) | $V_{DD}$ Current, $V_{DD} = -9V \pm 5\%$ | 3MHz Data Rate | $T_A = 25°C$ | | 30 | 40 | | 30 | 40 | mA |
| | | 26% Duty Cycle | $T_A = 0°C$ | | | 45 | | | 45 | |
| | | $V_{\phi L} = V_{CC}-14.7V$ | $T_A = -55°C$ | | | | | | 60 | |

Note: 1. Power dissipation is directly proportional to clock duty cycle and independent of frequency. The duty cycle is the clock LOW time (one clock line) divided by the clock period. At $V_{DD} = -9V$ the maximum duty cycle is 26%. The duty cycle should be kept as small as possible to minimize power dissipation.

## SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

**Am1402A/Am1403A/Am1404A**

| | | | $V_{DD} = -5$ V ±5% (Test Load 1) | | | $V_{DD} = -9$ V ±5% (Test Load 2) | | | |
|---|---|---|---|---|---|---|---|---|---|
| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
| $f_c$ | Clock Frequency Range | | (Note 1) | | 2.5 | (Note 1) | | 1.5 | MHz |
| $f_d$ | Data Repetition Rate | | (Note 1) | | 5.0 | (Note 1) | | 3.0 | MHz |
| $t_{\phi PW}$ | Clock Pulse Width | | 0.13 | 1.0 | | 0.17 | | 10 | μs |
| $t_{\phi d}$ | Clock Pulse Delay (Note 2) | $t_{\phi PW} = 130$ ns | 10 | | (Note 2) | 10 | | (Note 2) | ns |
| $t_f$, $t_r$ | Clock Pulse Rise/Fall Time | | | | 1000 | | | 1000 | ns |
| $t_s$ | Data Set Up Time | $t_r = t_f \leq 50$ ns | 30 | | 30 | 60 | | 60 | ns |
| $t_h$ | Data Hold Time | $t_r = t_f \leq 50$ ns | 20 | | 20 | 20 | | 20 | ns |
| $t_{pd+}$, $t_{pd-}$ | Clock to Data Out Delay | | | | 90 | | | 110 | ns |
| $C_{IN}$* | Input Capacitance | @ 1 MHz, 250 mVPP | | 5 | 10 | | 5 | 10 | pF |
| $C_{OUT}$* | Output Capacitance | @ 1 MHz, 250 mVPP | | 5 | 10 | | 5 | 10 | pF |
| $C_\phi$* | Clock Capacitance | @ 1 MHz, 250 mVPP | | 110 | 140 | | 110 | 140 | pF |

## SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

**Am2802/Am2803/Am2804**

Clock Pulse Width = 70nsec
Clock LOW Level = ($V_{CC}-15$)

$V_{DD} = -5$ V ±5%
(Test Load 1)

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | |
|---|---|---|---|---|---|---|
| $f_c$ | Clock Frequency Range | $t_r = t_f = 10$ ns | (Note 1) | | 5.0 (Note 4) | MHz |
| $f_d$ | Data Repetition Rate (Note 1) | | (Note 3) | | 10.0 (Note 4) | MHz |
| $t_{\phi PW}$ | Clock Pulse Width | | 0.07 | | 10 | μs |
| $t_{\phi d}$ | Clock Pulse Delay | $t_{\phi PW} = 70$ ns | 10 | | (Note 2) | ns |
| $t_f$, $t_r$ | Clock Pulse Rise/Fall Time | | | | 1000 | ns |
| $t_s$ | Data Set Up Time | | 30 | | | ns |
| $t_h$ | Data Hold Time | | 20 | | | ns |
| $t_{pd+}$, $t_{pd-}$ | Clock to Data Out Delay | | | | 90 | ns |

Notes:
1. See minimum operating frequency graph for low limits on data rep. rate.
2. Upper limit on $t_{\phi d}$ is determined by minimum frequency.
3. See max clock pulse delay graph for guarantee.
4. For additional information on 10MHz operation (5MHz clock rate) see AMD application note dated July 1973 on "Applications of Dynamic Shift Registers."

## DESCRIPTION OF TERMS

### OPERATIONAL TERMS

**$V_{OH}$** Minimum logic HIGH output voltage with output HIGH current $I_{OH}$ flowing out of output.

**$V_{OL}$** Maximum logic LOW output voltage with output LOW current $I_{OL}$ into junction of output and load resistor.

**$V_{IH}$** Logic HIGH input voltage.
**$V_{IL}$** Logic LOW input voltage.
**$V_{OL}$** Clock LOW input voltage.
**$V_{OH}$** Clock HIGH input voltage.
**$I_I$** Input leakage current.
**$I_O$** Output leakage current.
**$I_{DD}$** Power supply current.
**$C_{IN}$** Input capacitance.
**$C_\phi$** Input clock capacitance.
**$C_{OUT}$** Output capacitance.

### FUNCTIONAL TERMS

$\phi_1$, $\phi_2$ The two clock phases required by the dynamic shift register.
**$f_c$** The clock frequency of the shift register.
**$f_d$** The input data repetition rate.

### SWITCHING TERMS

**$t_{\phi d}$** The delay between the LOW to HIGH transition of a clock phase to the HIGH to LOW transition of the other clock phase.

**$t_{\phi PW}$** The clock pulse widths necessary for correct operation.

**$t_f$, $t_r$** The clock pulse rise and fall times necessary for correct operation.

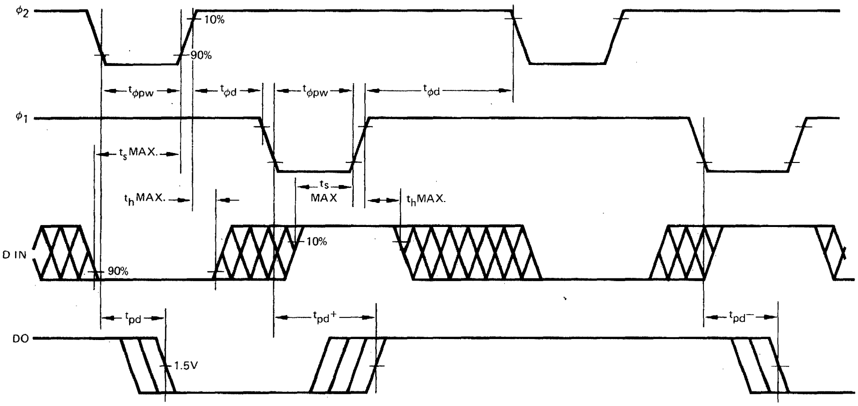
**$t_s$** The time required for the input data to be present prior to the LOW to HIGH transition of the clock phase to ensure correct operation.

**$t_h$** The time required for the input data to remain present after the LOW to HIGH transition of the clock phase to ensure correct operation.

**$t_{pd+}$** The propagation delay from the HIGH to LOW clock phase $\phi_1$ transition to the output LOW to HIGH transition.

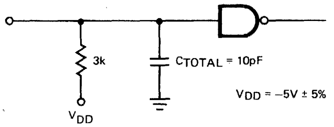
**$t_{pd-}$** The propagation delay from the HIGH to LOW clock phase $\phi_2$ transition to the output HIGH to LOW transition.

## SWITCHING WAVEFORMS

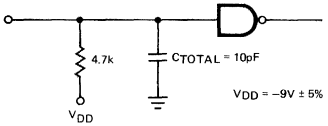

φ2
10%
90%
tφpw
tφd
tφpw
tφd
φ1
ts MAX.
th MAX.
ts MAX
th MAX.
D IN
10%
90%
tpd
tpd+
tpd−
DO
1.5V

Clock Rise Time 10 ns
Clock Fall Time 10 ns
Output Load 1 TTL Load

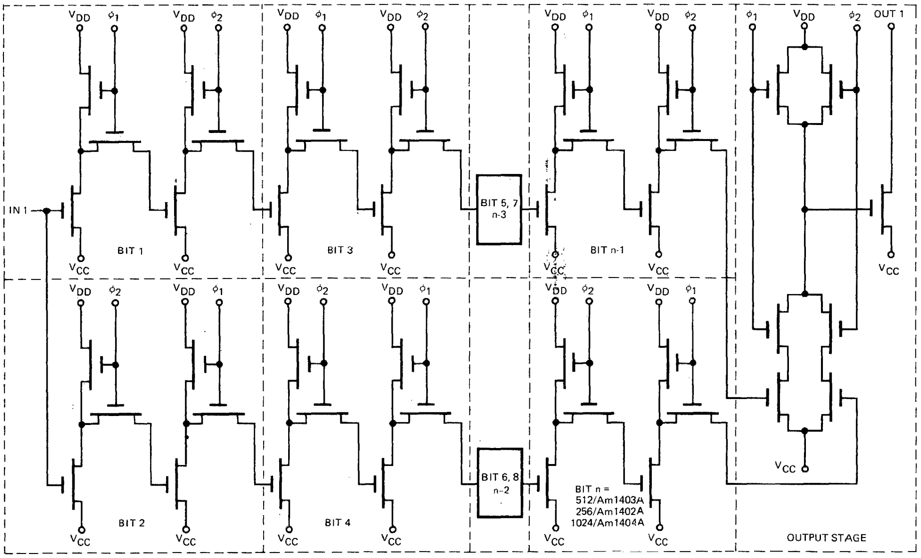
**Test Load 1**


3k
CTOTAL = 10pF
VDD = −5V ± 5%
VDD

**Test Load 2**


4.7k
CTOTAL = 10pF
VDD = −9V ± 5%
VDD

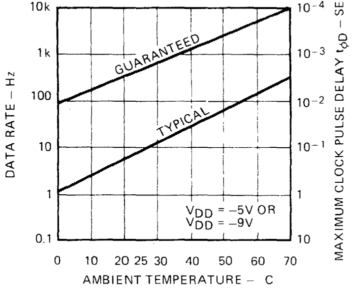
## CIRCUIT DIAGRAM


VDD
φ1
φ2
IN 1
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5, 7 n-3
BIT 6, 8 n-2
BIT n-1
BIT n = 512/Am1403A 256/Am1402A 1024/Am1404A
VCC
OUT 1
OUTPUT STAGE

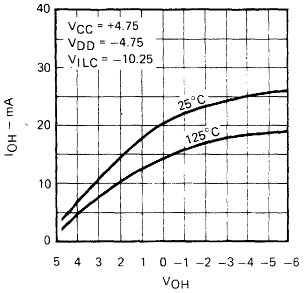
## POWER CHARACTERISTICS

### Minimum Operating Data Rate or Maximum Clock Pulse Delay Versus Temperature

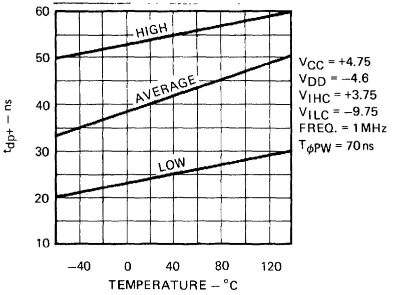
(For Small Duty Cycles)



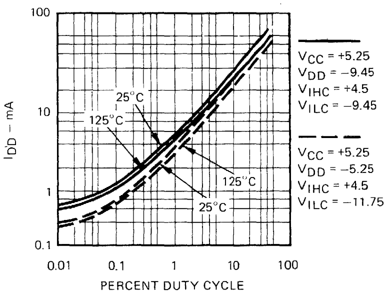
### $I_{OH}$ Versus $V_{OH}$



### Typical Range of $t_{pd+}$ Versus Temperature

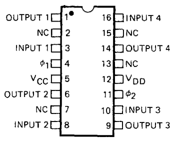


### $I_{DD}$ Versus Clock Duty Cycle

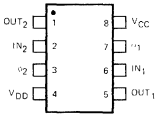


## ORDERING INFORMATION

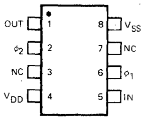
### Am2802/Am1402A


OUTPUT 1
1
NC
2
INPUT 1
3
$\phi_1$
4
$V_{CC}$
5
OUTPUT 2
6
NC
7
INPUT 2
8
16
INPUT 4
15
NC
14
OUTPUT 4
13
NC
12
$V_{DD}$
11
$\phi_2$
10
INPUT 3
9
OUTPUT 3

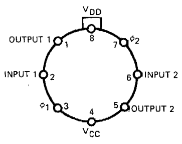
### Am2803/Am1403A


$OUT_2$
1
$IN_2$
2
$\phi_2$
3
$V_{DD}$
4
8
$V_{CC}$
7
$\phi_1$
6
$IN_1$
5
$OUT_1$

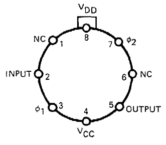
### Am2804/Am1404A


OUT
1
$\phi_2$
2
NC
3
$V_{DD}$
4
8
$V_{SS}$
7
NC
6
$\phi_1$
5
IN

### Am2803/Am1403A


$V_{DD}$
8
OUTPUT 1
1
7
$\phi_2$
INPUT 1
2
6
INPUT 2
$\phi_1$
3
4
5
OUTPUT 2
$V_{CC}$

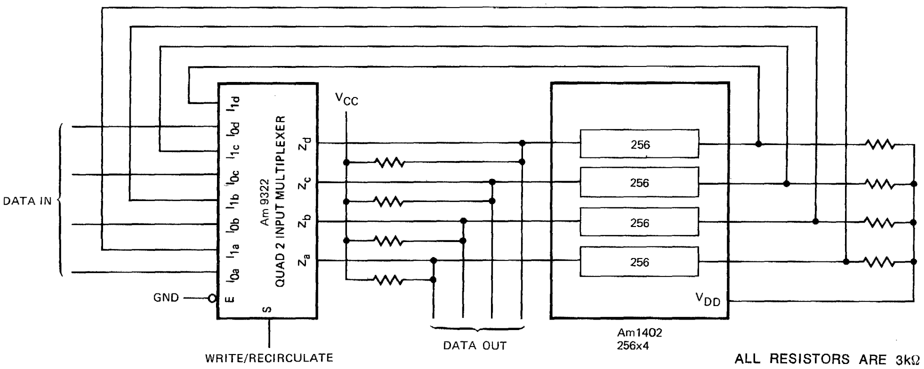
### Am2804/Am1404A


$V_{DD}$
8
NC
1
7
$\phi_2$
INPUT
2
6
NC
$\phi_1$
3
4
5
OUTPUT
$V_{CC}$

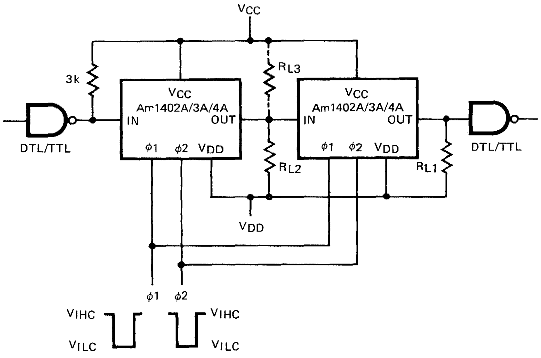
# APPLICATIONS

## 256-Bit Delay

Write Recirculate Logic


DATA IN
GND
E
S
WRITE/RECIRCULATE
Am 9322
QUAD 2 INPUT MULTIPLEXER
$I_{0a}$ $I_{1a}$ $I_{0b}$ $I_{1b}$ $I_{0c}$ $I_{1c}$ $I_{0d}$ $I_{1d}$
$Z_d$ $Z_c$ $Z_b$ $Z_a$
VCC
256
256
256
256
VDD
DATA OUT
Am1402
256x4
ALL RESISTORS ARE 3kΩ

## DTL/TTL To MOS To DTL/TTL Interface

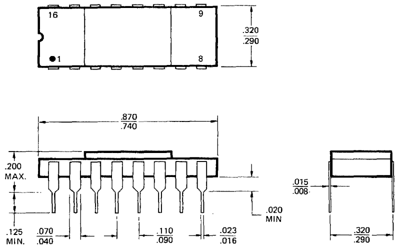

VCC
3k
RL3
RL2
RL1
VCC
Am1402A/3A/4A
IN
OUT
φ1 φ2 VDD
VCC
Am1402A/3A/4A
IN
OUT
φ1 φ2 VDD
DTL/TTL
DTL/TTL
VDD
φ1 φ2
VIHC
VILC
VIHC
VILC

### $R_L$ Load Resistor Values for Different $V_{DD}$ Supplies

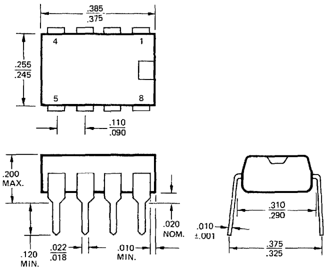
| | $V_{CC} = 5$ V<br>$V_{DD} = -5$ V | $V_{CC} = 5$ V<br>$V_{DD} = -9$ V |
|---|---|---|
| $R_{L1}$ | 3.0 k | 4.7 k |
| $R_{L2}$ | 4.7 k | 6.2 k |
| $R_{L3}$ | Not required | 3.9 k |

## PHYSICAL DIMENSIONS

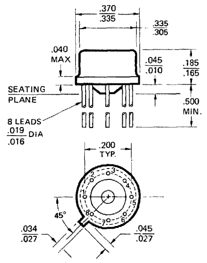
### 16-Pin Dual-In-Line


16
9
1
8
.320
.290
.870
.740
.200
MAX.
.015
.008
.020
MIN
.125
MIN.
.070
.040
.110
.090
.023
.016
.320
.290

### 8-Pin Molded

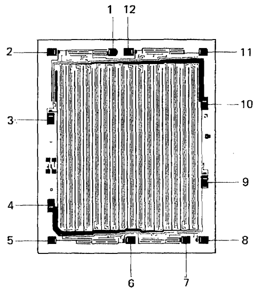

.385
.375
4
1
5
8
.255
.245
.110
.090
.200
MAX.
.020
NOM.
.010
±.001
.120
MIN.
.022
.018
.010
MIN.
.310
.290
.375
.325

### Metal Can


.370
.335
.335
.305
.040
MAX
.045
.010
.185
.165
SEATING
PLANE
.500
MIN.
8 LEADS
.019
.016
DIA
.200
TYP.
45°
.034
.027
.045
.027

| PAD | 1402A/2802 PIN | 1402A/2802 SIGNAL | 1403A/2803 PIN | 1403A/2803 SIGNAL | 1404A/2804 PIN | 1404A/2804 SIGNAL |
|---|---|---|---|---|---|---|
| 1 | 1 | OUT 1 | | | | |
| 2 | 3 | IN 1 | 2 | IN 1 | 2 | IN |
| 3 | 4 | φ 1 | 3 | φ 1 | 3 | φ 1 |
| 4 | 5 | $V_{CC}$ | 4 | $V_{CC}$ | 4 | $V_{CC}$ |
| 5 | 6 | OUT 2 | 5 | OUT 2 | 5 | OUT |
| 6 | 8 | IN 2 | | | | |
| 7 | 9 | OUT 3 | | | | |
| 8 | 10 | IN 3 | 6 | IN 2 | 7 | φ 2 |
| 9 | 11 | φ 2 | 7 | φ 2 | | |
| 10 | 12 | $V_{DD}$ | 8 | $V_{DD}$ | | |
| 11 | 14 | OUT 4 | 1 | OUT 1 | 8 | $V_{DD}$ |
| 12 | 16 | IN 4 | | | | |

### Metallization and Pad Layout


1
12
2
11
10
3
9
4
5
8
6
7

DIE SIZE .109" X .131"

# Am2805/2806/2807/2808

## 512- and 1024-Bit Dynamic Shift Registers

### Distinctive Characteristics

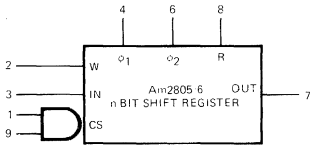
- Am2805 Plug-in Replacement Intel 1405A and Signetics 2505
  Am2806 Plug-in Replacement Signetics 2512
  Am2807 Plug-in Replacement Signetics 2524
  Am2808 Plug-in Replacement Signetics 2525
- On chip recirculate and chip select controls
- 100% reliability assurance testing in compliance with MIL-STD-883
- TTL and DTL compatible
- Full military temperature range devices available

### FUNCTIONAL DESCRIPTION

The Am2805 and Am2807 are 512-bit dynamic shift registers with recirculate logic on chip. The Am2806 and Am2808 are 1024-bit dynamic shift registers which also have built-in recirculate logic. When the write input is HIGH, data on the data input enters the first bit of the register during the $\phi_2$ clock time. If the write input is LOW, then the output of the register is written into the first bit instead. Data in the last bit of the register appears on the data output during the $\phi_1$ clock time if the read line is HIGH. If the read line is LOW, the output is OFF (high impedance state). The outputs of all four devices are open drains; they pull the output to $V_{CC}$ when ON and exhibit a very high impedance when OFF. An external pull-down resistor to ground or $V_{DD}$ must be used to establish the LOW logic level.

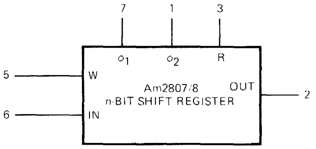
The Am2805 and Am2806 also have two chip select inputs, $CS_1$ and $CS_2$. If either of these inputs is LOW, the register recirculates and the output remains OFF, regardless of the state of the read and write lines. All inputs except the clocks are TTL/DTL compatible. A TTL input may be driven by the output if a 3k pull-down resistor to $V_{DD}$ is used. The register outputs can be wire-ORed for expansion. The devices are guaranteed to operate at speeds up to 3MHz.

### LOGIC SYMBOLS



Am2805 n = 512
Am2806 n = 1024

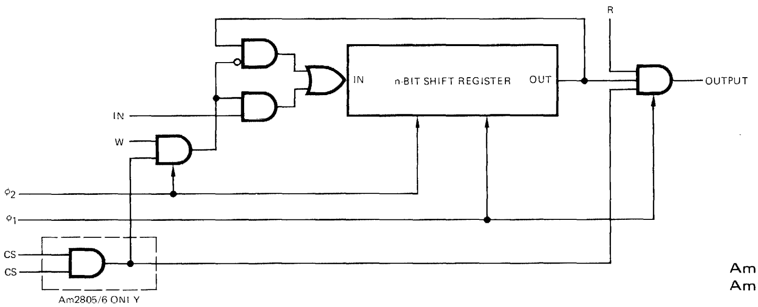
$V_{CC}$ = Pin 5
$V_{DD}$ = Pin 10



Am2807 n = 512
Am2808 n = 1024

$V_{CC}$ = Pin 8
$V_{DD}$ = Pin 4

### LOGIC DIAGRAM



Am2805/7 n = 512
Am2806/8 n = 1024

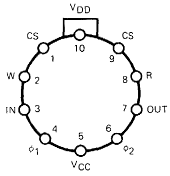
### ORDERING INFORMATION

| Ambient Temperature | Package Type | Length | |
|---|---|---|---|
| | | 512 Bits | 1024 Bits |
| 0°C ≤ $T_A$ ≤ +70°C | Molded DIP (8 Pin) | AM2807PC | AM2808PC |
| | TO-100 (10 Pin) | AM2805HC | AM2806HC |
| −55°C ≤ $T_A$ ≤ +125°C | TO-100 (10 Pin) | AM2805HM | AM2806HM |

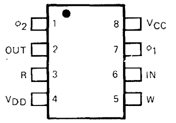
### CONNECTION DIAGRAMS

**Top View**

**Am2805/6**



**Am2807/8**



Note: PIN 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| DC Input Voltage with Respect to $V_{CC}$ | −20V to +0.3V |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

$V_{DD}$ = −5V ±5%, $V_{CC}$ = 5.0V ±5%
Am280XXM $T_A$ = −55°C to +125°C
Am280XXC $T_A$ = 0°C to +70°C

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage (Notes 2 & 3) | $V_{CC}$ = MIN. | $I_{OH}$ = 1.6mA, ($R_L$ = 5.6kΩ) | 3.6 | 4.0 | | Volts |
| | | | $I_{OH}$ = 2.6mA, ($R_L$ = 3kΩ) | 2.4 | 3.5 | | |
| $I_{OL}$ | Output Leakage Current | $V_O$ = −5.5V, $V_{\phi 1}$ = $V_{\phi 2}$ = −12V | | | 10 | 1000 | nA |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs except clocks | Am1405 | $V_{CC}$−2.0 | | $V_{CC}$+0.3 | Volts |
| | | | Am2505/12/24/25 | $V_{CC}$−1.8 | | $V_{CC}$+0.3 | |
| | | | Am2805/6/7/8 | $V_{CC}$−1.0 | | $V_{CC}$+0.3 | |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs except clocks | | $V_{CC}$−10 | | $V_{CC}$−4.2 | Volts |
| $I_I$ | Input Leakage Current | $V_{IN}$ = −5.5V, $T_A$ = 25°C | | | 10 | 500 | nA |
| $I_\phi$ | Clock Input Leakage Current | $V_\phi$ = −12V, $T_A$ = 25°C | | | 10 | 1000 | nA |
| $V_{\phi H}$ | Clock HIGH Level | | | $V_{CC}$−1.0 | | $V_{CC}$+0.3 | V |
| $V_{\phi L}$ | Clock LOW Level | | | $V_{CC}$−17 | | $V_{CC}$−14.5 | V |
| $I_{DD}$ | Power Supply Current (Note 4) | f = 1MHz, $T_A$ = 25°C<br>Output Open<br>$V_{DD}$ = −5.5V, $t_{\phi L}$ = 150ns | Am2805/7 | | 7 | 12 | mA |
| | | | Am2806/8 | | 10 | 20 | |

Notes: 1. Typical Limits are at $V_{CC}$ = 5.0V, $V_{DD}$ = −5.0V, 25°C Ambient and maximum loading.
2. Variations in $V_{CC}$ will be tracked directly by $V_{OH}$ and input thresholds.
3. The output is open drain and the logic LOW level must be defined by an external pull-down resistor. A 3k resistor to $V_{DD}$ provides TTL compatibility.
4. The power supply current flows only while one clock is LOW. Average power is therefore directly proportional to clock duty cycle (ratio of clock LOW time to total clock period.) See curves next page.

## SWITCHING CHARACTERISTICS ($T_A$ = 0°C to +70°C, $V_{CC}$ = +5.0V ±5%, $V_{DD}$ = −5.0V ±5%, $V_{\phi L}$ = −11V)

| Parameters | Definition | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock and Data Rate | 0°C to +70°C | | 4.0 | 7.0 | | MHz |
| | | Am280XXM | −55°C to +125°C | 3.0 | | | |
| $t_{\phi d}$ | Delay Between clocks | | | 5.0 | | Note 5 | ns |
| $t_{\phi pw}$ | Clock LOW Time | | | 0.070 | | Note 8 | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | 10% to 90% | | | | 1.0 | μs |
| $t_s$(D) | Set-up Time, Data Input (see definitions) | $t_r$ = $t_f$ = 50ns | | | | 150 | ns |
| $t_h$(D) | Hold Time, Data Input (see definitions) | $t_r$ = $t_f$ = 50ns | | | | 0 | ns |
| $t_s$(C) | Set-up Time, Read, Write and Recirculate Controls (see definitions) | $t_r$ = $t_f$ = 50ns | | | | 135 | ns |
| $t_h$(C) | Hold Time, Read, Write and Recirculate Controls (see definitions) | $t_r$ = $t_f$ = 50ns | | | | 0 | ns |
| $t_{pd}$ | Delay, Clock to Data Out | R = HIGH | 0°C to +70°C | | | 100 | ns |
| | | | −55°C to +125°C | | | 150 | |
| $C_{in}$, $C_{out}$ | Capacitance, Any Input and Output (Note 6) | f = 1 MHz, $V_{IN}$ = $V_{CC}$ | | | | 5.0 | pF |
| $C_\phi$ | Clock Input Capacitance (Note 6) | f = 1 MHz, $V_{IN}$ = $V_{CC}$ | Am2805/7 | | | 50 | pF |
| | | | Am2806/8 | | | 100 | |

Notes: 5. The maximum delay between clocks ($\phi_1$ and $\phi_2$ both HIGH) is a function of junction temperature. The junction temperature is a function of ambient temperature and clock duty cycle. See curves for minimum frequency.
6. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
7. For some reason known only to God and Intel, the convention for $\phi_1$ and $\phi_2$ for this device are reversed from the normal. $\phi_1$ is the output clock and $\phi_2$ is the input clock.
8. 100μsec or 50% duty cycle, whichever is less.

## DEFINITION OF TERMS

**Dynamic Shift Register** A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

**$\phi_1$, $\phi_2$** The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at $V_{SS}$ or $V_{CC}$. Data is accepted into the master of each bit during $\phi_2$ and is transferred to the slave of each bit during $\phi_1$.

**$f_{max}$** The maximum frequency at which the register will operate. This is the data rate through the register and also the frequency of each clock signal.

**$t_{\phi d}$** Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-to-LOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

**$t_{\phi pw}$** Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

**$t_r$, $t_f$** Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

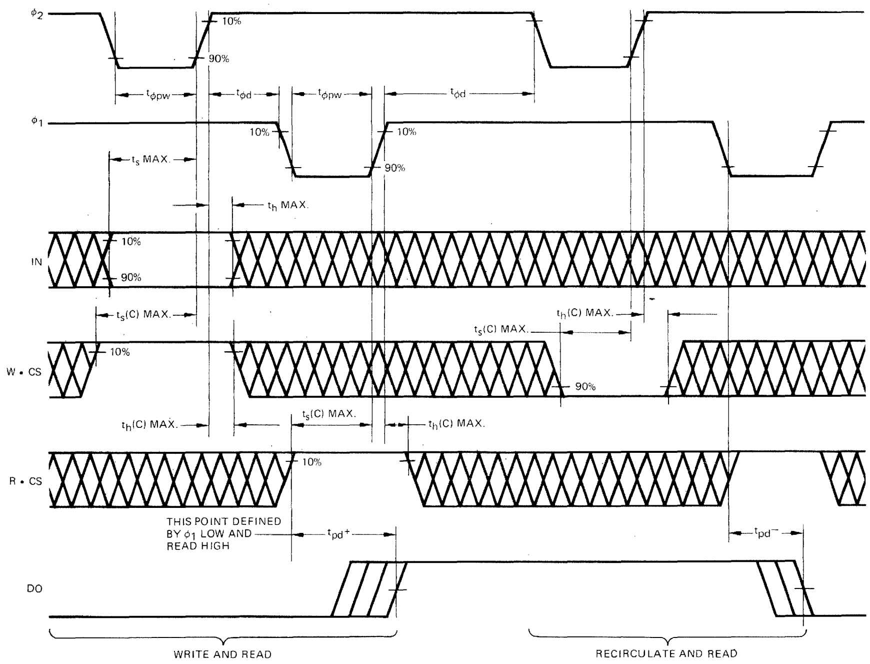
**$t_s(D)$** Data set-up time. The time prior to the LOW-to-HIGH transition of $\phi_2$ during which the data on the data input must be steady to be correctly written into the memory.

**$t_h(D)$** Data hold time. The time following the LOW-to-HIGH transition of $\phi_2$ during which the data must be steady. To correctly write data into the register, the data must be applied by $t_s(D)$ before this transition and must not be changed until $t_h(D)$ after this transition.

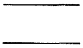
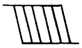
**$t_s(C)$, $t_h(C)$** The set-up and hold times for the Read, Write, and Chip Select controls, relative to the LOW-to-HIGH transition of the appropriate clock phase.

**$t_{pd}$** The delay from the start of a read cycle to correct data present at the register output. A read cycle is begun when $\phi_1$ is LOW AND Read is HIGH.

## SWITCHING WAVEFORMS

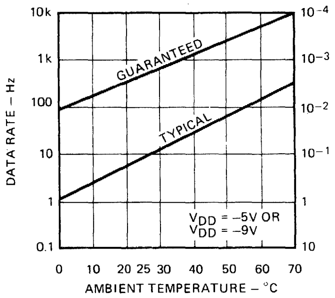

φ2
10%
90%
tφpw
tφd
tφpw
tφd
φ1
10%
10%
90%
ts MAX.
th MAX.
IN
10%
90%
ts(C) MAX.
th(C) MAX.
ts(C) MAX.
W • CS
10%
90%
th(C) MAX.
ts(C) MAX.
th(C) MAX.
R • CS
10%
THIS POINT DEFINED
BY φ1 LOW AND
READ HIGH
tpd+
tpd−
DO
WRITE AND READ
RECIRCULATE AND READ

## KEY TO TIMING DIAGRAM

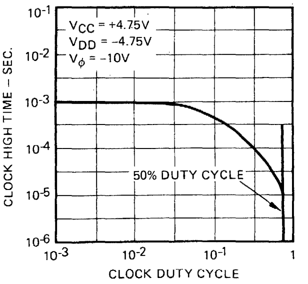
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | MUST BE STEADY | WILL BE STEADY |
|  | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN |

## OPERATING CHARACTERISTICS

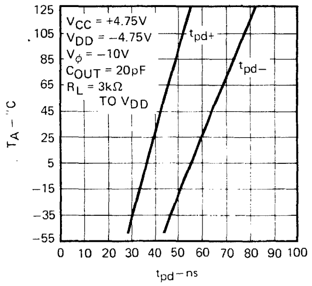
**Minimum Operating Data Rate or Maximum Clock Pulse Delay Versus Temperature**



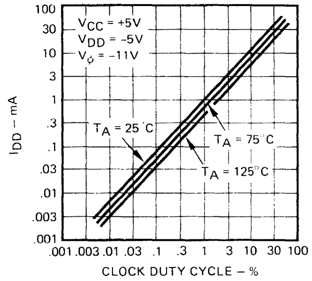
**Maximum Clock High Time Versus Clock Duty Cycle**



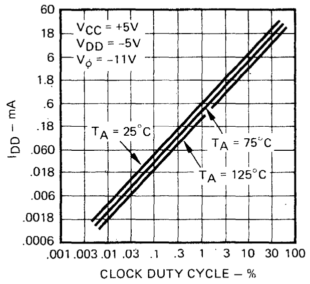
**Propagation Delay Versus Ambient Temperature**



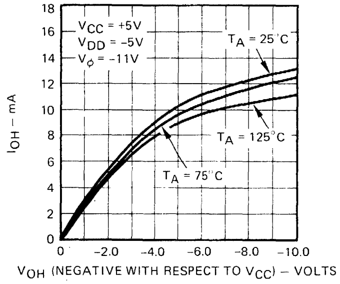
**Am2806/8 IDD Current Versus Clock Duty Cycle**



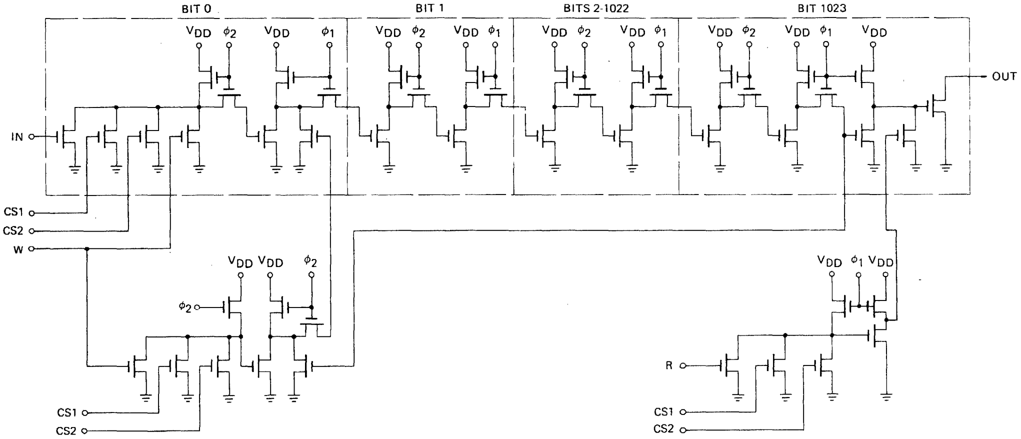
**Am2805/7 IDD Current Versus Clock Duty Cycle**



**VOH Versus IOH**



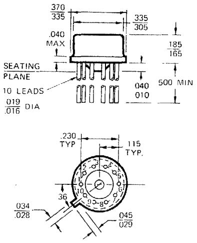
## SCHEMATIC DIAGRAM


BIT 0
BIT 1
BITS 2-1022
BIT 1023
VDD
φ2
φ1
IN
OUT
CS1
CS2
W
R

Note: No CS inputs on Am2807/8
⏚ = VCC

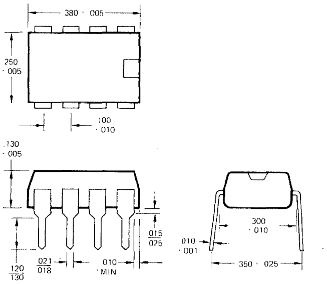
## PHYSICAL DIMENSIONS

### TO-100 Low



.370/.335
.335/.305
.040 MAX
.185/.165
SEATING PLANE
10 LEADS
.019/.016 DIA
.040/.010
.500 MIN
.230 TYP
.115 TYP.
36
.034/.028
.045/.029
1
2
3
4
5
6
7
8
9
10

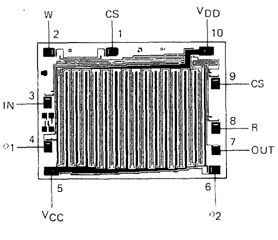
### Molded Mini-DIP



.380 ± .005
.250 ± .005
.100 ± .010
.130 ± .005
.015/.025
.300 ± .010
.010 ± .001
.120/.130
.021/.018
.010 MIN
.350 ± .025

### Metallization and Pad Layout Am2805/7

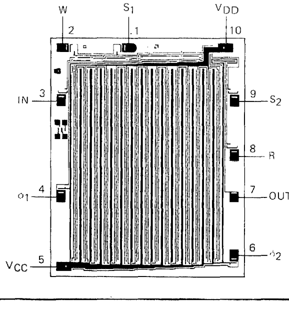
106 x 78 Mils



W
CS
$V_{DD}$
2
1
10
9
CS
3
IN
8
R
4
$\phi_1$
7
OUT
5
6
$V_{CC}$
$\phi_2$

### Metalization and Pad Layout Am2806/8

106 x 131 Mils



W
$S_1$
$V_{DD}$
2
1
10
3
IN
9
$S_2$
8
R
4
$\phi_1$
7
OUT
6
$\phi_2$
5
$V_{CC}$

# Am2809

## Dual 128-Bit Static Shift Register

### Distinctive Characteristics

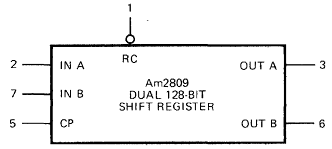
- Second source to Signetics 2521.
- TTL compatible on clock and data inputs.
- Operation guaranteed from DC-to-2.5MHz.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Low capacitance on clock and data inputs.

### FUNCTIONAL DESCRIPTION

The Am2809 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers have a common clock input which is low-threshold TTL compatible. The registers also have built-in recirculate feedback. When the recirculate control ($\overline{RC}$) is LOW, the data on the data output of each register is fed back to the corresponding register input. When $\overline{RC}$ is HIGH, each register accepts data from the data input. Each of the register outputs can drive one standard TTL load or three Am93L series low-power unit loads.

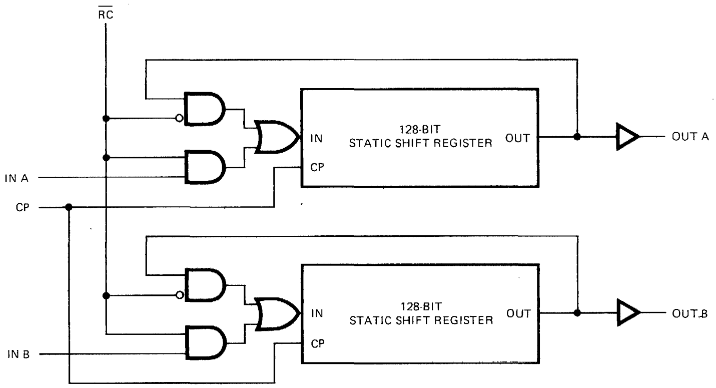
Data in the Am2809 is shifted on the LOW-to-HIGH edge of the input clock. Data on the data inputs must remain steady for a set-up time before and a hold time after this clock transition. Since storage in the register is static, the register may be halted indefinitely with the clock in the HIGH state.

### LOGIC SYMBOL


1
RC
2
IN A
OUT A
3
Am2809
DUAL 128-BIT
SHIFT REGISTER
7
IN B
5
CP
OUT B
6

$V_{CC}$ = Pin 8
$V_{GG}$ = Pin 4

### LOGIC BLOCK DIAGRAM

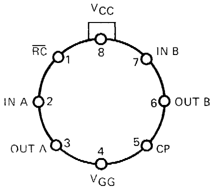

RC
128-BIT STATIC SHIFT REGISTER
IN
OUT
CP
OUT A
IN A
CP
128-BIT STATIC SHIFT REGISTER
IN
OUT
CP
OUT B
IN B

### ORDERING INFORMATION

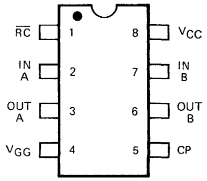
| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM2809PC |
| TO-5 | 0°C to +70°C | AM2809HC |
| TO-5 | –55°C to +125°C | AM2809HM |

### CONNECTION DIAGRAMS
Top Views

**Am2809HC**
**Am2809HM**


VCC
8
RC
1
7
IN B
IN A
2
6
OUT B
OUT A
3
4
5
CP
VGG

**Am2809PC**


RC
1
8
VCC
IN A
2
7
IN B
OUT A
3
6
OUT B
VGG
4
5
CP

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Temperature (Ambient) Under Bias | –55°C to +125°C |
| DC Input Voltage with Respect to $V_{CC}$ | –20V to +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{CC}$ | $V_{GG}$ |
|---|---|---|---|
| Am2809PC<br>Am2809HC | 0°C to +70°C | 5.0V ±5% | –12V ±5% |
| Am2809HM | –55°C to +125°C | 5.0V ±5% | –12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = –0.1mA | | $V_{CC}$–1.5 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 1.6mA | | | –4 | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | $V_{CC}$–1.7 | | $V_{CC}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | $V_{CC}$–3.95 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0 | $T_A$ = 25°C | | 10 | 500 | nA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.4V, | $T_A$ = 25°C | | 10 | 500 | nA |
| $I_{GG}$ | Power Supply Current | f = 2.5MHz | $T_A$ = 25°C | | 24 | 32 | mA |
| | | $V_{CC}$ = MAX. | $T_A$ = 0°C to +70°C | | | 38 | |
| | | f = 2.0MHz | $T_A$ = –55°C to +125°C | | | 44 | |

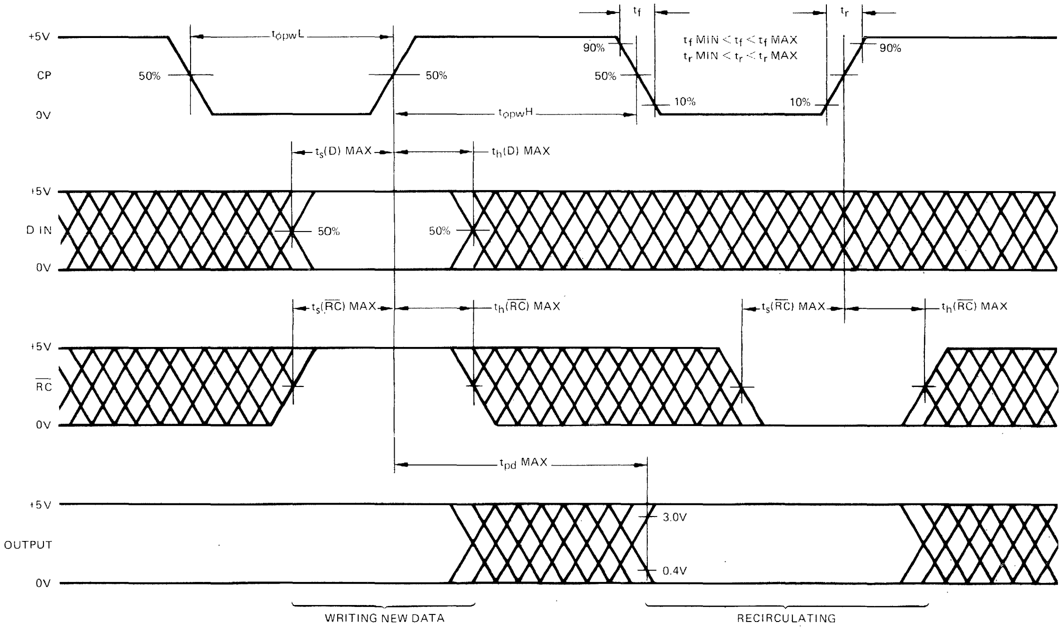
Note: 1. Typical Limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

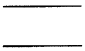
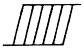
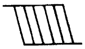
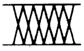
| Parameters | Description | Test Conditions | Am2809PC Am2809HC Min. | Typ. | Max. | Am2809HM Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_c$ | Clock Frequency Range | | 0 | | 2.5 | 0 | | 2.0 | MHz |
| $t_{\phi pw}H$ | Clock HIGH Time | | 0.2 | | ∞ | 0.25 | | ∞ | μs |
| $t_{\phi pw}L$ | Clock LOW Time | | 0.2 | | 100 | 0.25 | | 100 | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | 10% to 90% | | | 1.0 | | | 1.0 | μs |
| $t_s$(D) | Set-up Time, Data Input (see definitions) | $t_r = t_f$ = 50ns | | | 75 | | | 100 | ns |
| $t_h$(D) | Hold Time, Data Input (see definitions) | $t_r = t_f$ = 50ns | | | 50 | | | 65 | ns |
| $t_s(\overline{RC})$ | Set-up Time, Recirculate Control (see definitions) | $t_r = t_f$ = 50ns | | | 50 | | | 100 | ns |
| $t_h(\overline{RC})$ | Hold Time, Recirculate Control (see definitions) | $t_r = t_f$ = 50ns | | | 50 | | | 65 | ns |
| $t_{pd}$ | Delay, Clock to Data Out | | | 170 | 300 | | 170 | 350 | ns |
| $C_{in}$ | Capacitance, Any Input (Note 2) | f = 1MHz, $V_{IN}$ = $V_{CC}$ | | 3 | 7 | | 3 | 7 | pF |

Note: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

## TIMING DIAGRAM

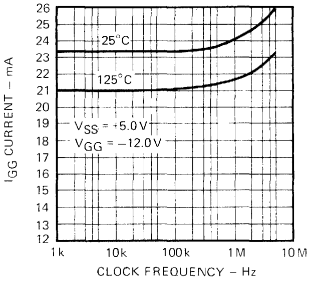

tf
tr
tf MIN < tf < tf MAX
tr MIN < tr < tr MAX
+5V
CP
0V
50%
tφpwL
50%
90%
50%
10%
10%
90%
tφpwH
ts(D) MAX
th(D) MAX
+5V
D IN
0V
50%
50%
ts(RC) MAX
th(RC) MAX
ts(RC) MAX
th(RC) MAX
+5V
RC
0V
tpd MAX
+5V
OUTPUT
0V
3.0V
0.4V
WRITING NEW DATA
RECIRCULATING

### KEY TO TIMING DIAGRAM

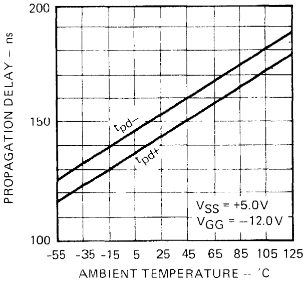
| WAVEFORM | INPUTS | OUTPUTS | WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|---|---|---|
|  | MUST BE STEADY | WILL BE STEADY |  | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
|  | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |  | DON'T CARE, ANY CHANGE PERMITTED | CHANGING, STATE UNKNOWN |

## CHARACTERISTIC CURVES

**Typical Power-Supply Currents Versus Frequency**



**Typical Propagation Delay Versus Ambient Temperature**

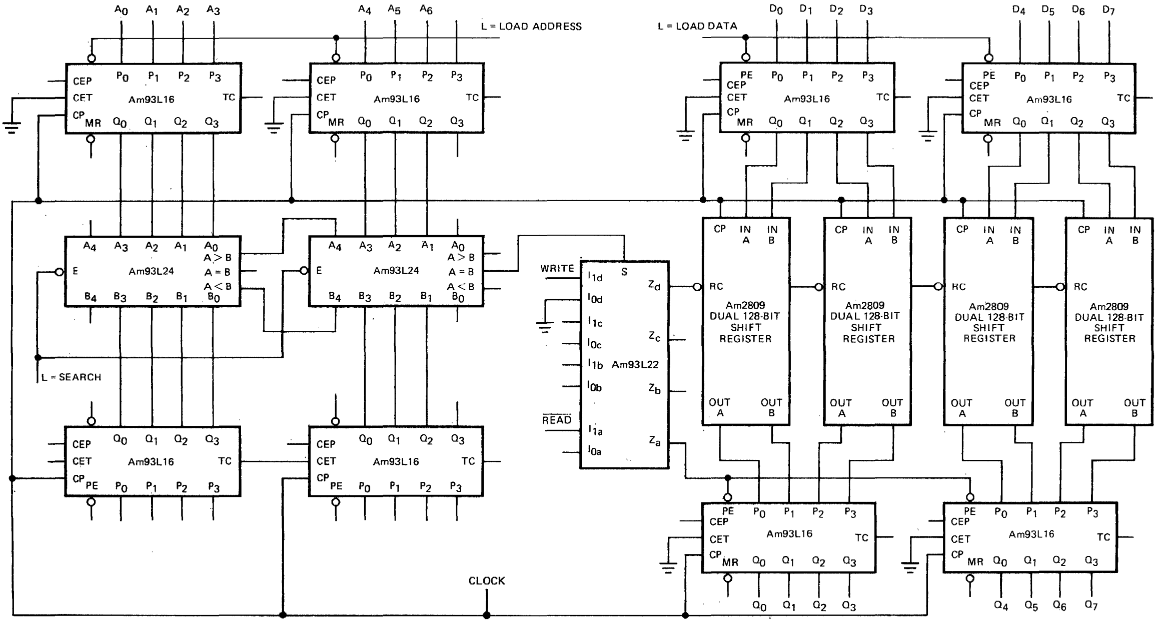


## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

## APPLICATIONS

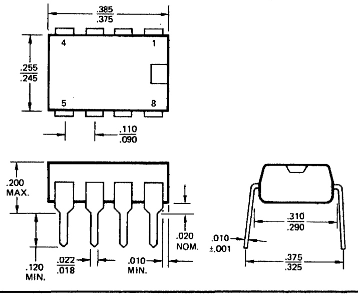

A0 A1 A2 A3
A4 A5 A6
L = LOAD ADDRESS
L = LOAD DATA
D0 D1 D2 D3
D4 D5 D6 D7
CEP
CET
CP
MR
PE
P0 P1 P2 P3
Q0 Q1 Q2 Q3
TC
Am93L16
Am93L24
E
A4 A3 A2 A1 A0
B4 B3 B2 B1 B0
A > B
A = B
A < B
L = SEARCH
WRITE
READ
S
I1d I0d I1c I0c I1b I0b I1a I0a
Zd Zc Zb Za
Am93L22
CP IN A IN B
RC
Am2809 DUAL 128-BIT SHIFT REGISTER
OUT A OUT B
CLOCK
Q0 Q1 Q2 Q3
Q4 Q5 Q6 Q7

### 128-Word x 8-Bit Pseudo-Random Access Memory

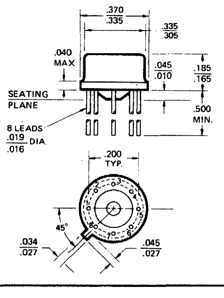
Data stored in the four dual 128-bit shift registers can be accessed randomly by comparing the desired address with the address currently available at the shift register I/O. A pair of Am93L16 low-power counters keeps track of data addresses as the data circulates around the memory. Other Am93L16 counters are used as 4-bit registers with enables by grounding the count enables. They are used to store the requested address, the new data to be written into the memory, and the data read from the memory. The Am93L24 comparators switch the memories from the recirculate mode to the write mode to enter new data in a write operation. Similarly, the output storage registers are enabled when the Am93L24s indicate comparison in a read operation.

## PACKAGE OUTLINES

### Molded DIP

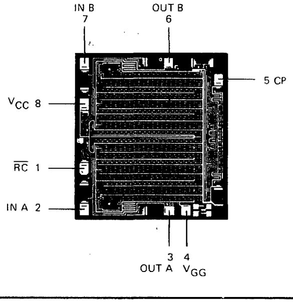

.385
.375
4
1
5
8
.255
.245
.110
.090
.200 MAX.
.120 MIN.
.022
.018
.010 MIN.
.020 NOM.
.010 ±.001
.310
.290
.375
.325

### TO-99


.370
.335
.335
.305
.040 MAX
.045
.010
.185
.165
SEATING PLANE
.500 MIN.
8 LEADS .019 .016 DIA.
.200 TYP.
45°
.034
.027
.045
.027

### Metallization and Pad Layout

86 X 95 Mils


IN B 7
OUT B 6
5 CP
VCC 8
RC 1
IN A 2
3 OUT A
4 VGG

# Am2810

## Dual 128-Bit Static Shift Register

### Distinctive Characteristics

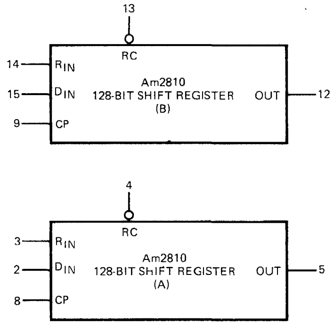
- 2nd Source to Mostek 1002P
- Built-in pull-up resistors
- 100% reliability assurance testing in compliance with MIL-STD-883
- Operation guaranteed from DC to 2MHz

### FUNCTIONAL DESCRIPTION

The Am2810 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers each have a two-input multiplexer on their inputs, so that input data may be selected from one of two sources. Each register has a separate clock input, and operates with a low-voltage TTL clock signal. The registers shift on the LOW-to-HIGH edge of the clock signal. Data at the inputs must be steady for a set-up time before and a hold time after this clock transition. Since data storage is static, the clock may be halted indefinitely in the HIGH state. The outputs of each register can drive one TTL load or three Am93L low-power TTL loads.

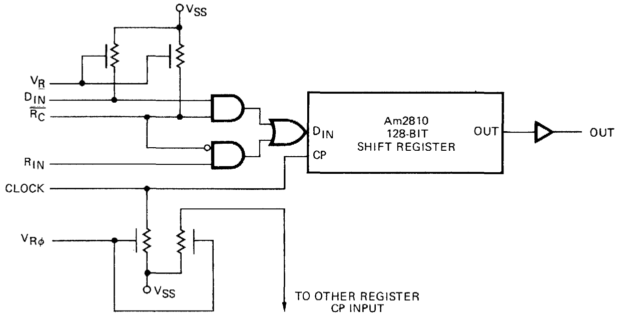
The two-input multiplexer on the input of each register is controlled by the RC (recirculate control) input. When RC is LOW, data is accepted on the $R_{in}$ input; when RC is HIGH, data is accepted on the $D_{in}$ input. The inputs to the registers have built-in pull-up resistors to provide total TTL compatibility. The $V_{RA}$ pin controls the pull-up resistors for register A $D_{in}$ and RC inputs. The $V_{RB}$ pin controls the pull-up resistors for the register B $D_{in}$ and RC inputs. The $V_{R\phi}$ pin controls the resistor on the clock input to both registers. When the resistor control pins are tied to $V_{GG}$ (−12V), the resistors are enabled and pull the inputs they affect up to $V_{SS}$. When the resistor control pins are tied to $V_{SS}$ the resistors are all very high impedance and the inputs they affect all exhibit normal MOS characteristics. The $R_{in}$ inputs are intended to be the recirculate inputs from an MOS output and these inputs do not have pull-up resistors associated with them.

### LOGIC SYMBOL


13
RC
14
RIN
15
DIN
Am2810
128-BIT SHIFT REGISTER
(B)
OUT
12
9
CP
4
RC
3
RIN
2
DIN
Am2810
128-BIT SHIFT REGISTER
(A)
OUT
5
8
CP

$V_{RA}$ = Pin 16
$V_{RB}$ = Pin 1
$V_{R\phi}$ = Pin 10
$V_{SS}$ = Pin 7
$V_{DD}$ = Pin 6
$V_{GG}$ = Pin 11

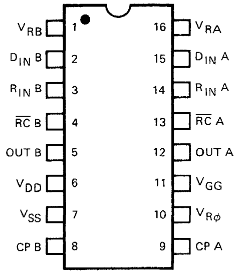
### LOGIC BLOCK DIAGRAM (One Register Shown)


VSS
VR
DIN
RC
RIN
CLOCK
VRφ
VSS
DIN
CP
Am2810
128-BIT
SHIFT REGISTER
OUT
OUT
TO OTHER REGISTER
CP INPUT

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +75°C | AM2810PC |
| Hermetic DIP | 0°C to +75°C | AM2810DC |
| Hermetic DIP | −55°C to +125°C | AM2810DM |

### CONNECTION DIAGRAMS


VRB 1
DIN B 2
RIN B 3
RC B 4
OUT B 5
VDD 6
VSS 7
CP B 8
16 VRA
15 DIN A
14 RIN A
13 RC A
12 OUT A
11 VGG
10 VRφ
9 CP A

Note: Pin 1 is marked for orientation.

## MAXIMUM RATING (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | $T_A$ | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am2810XC<br>Am1002P<br>Am1002L | 0°C to +75°C | 5.0V ±5% | 0 V | −12.0V ±5% |
| Am2810XM | −55°C to +125°C | 5.0V ±5% | 0 V | −12.0V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −100μA | | $V_{SS}$−1 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | 0.2 | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | $V_{SS}$−1 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | $V_{SS}$−4 | Volts |
| $I_{IL}$ (Note 2) | Resistors Disabled Input LOW Current | $V_{SS}$ = MAX., $V_{IN}$ = 0 V<br>$V_{RA} = V_{RB} = V_{R\phi} = V_{SS}$ | | | | −40 | μA |
| $I_{IL}(\Omega)$ (Note 2) | Resistors Enabled Input LOW Current | $V_{SS}$ = MAX., $V_{IN}$ = 0.4V, Am2810/Am1002P only<br>$V_{RA} = V_{RB} = V_{R\phi} = V_{GG}$ | | −0.3 | | −2.0 | mA |
| $I_{IL}(\phi)$ | Input LOW Current Clock Input | 1002L only | | −0.6 | | −4.0 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{RA} = V_{RB} = V_{R\phi} = V_{IN} = V_{SS}$ | | | | 40 | μA |
| $I_{SS}$ | $V_{SS}$ Power Supply Current | f = 1MHz<br>Inputs and Outputs Open | 0°C to +75°C | | 14 | 25 | mA |
| | | | −55°C to +125°C | | | 35 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | | 0°C to +75°C | | −4 | −10 | |
| | | | −55°C to +125°C | | | −15 | |

Notes: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient and maximum loading.

2. On chip pull-up resistors are provided for the clock and data inputs; they are enabled when the appropriate $V_R$ input is at −12V. When the $V_R$ inputs are at $V_{SS}$, the resistors are disabled and the inputs exhibit normal MOS characteristics ($I_{IL}$ and $I_{IH}$), the recirculate data inputs have no pull-up resistors and always exhibit MOS characteristics. All pull-up resistors are disabled on the Am1002L except the one on the clock.

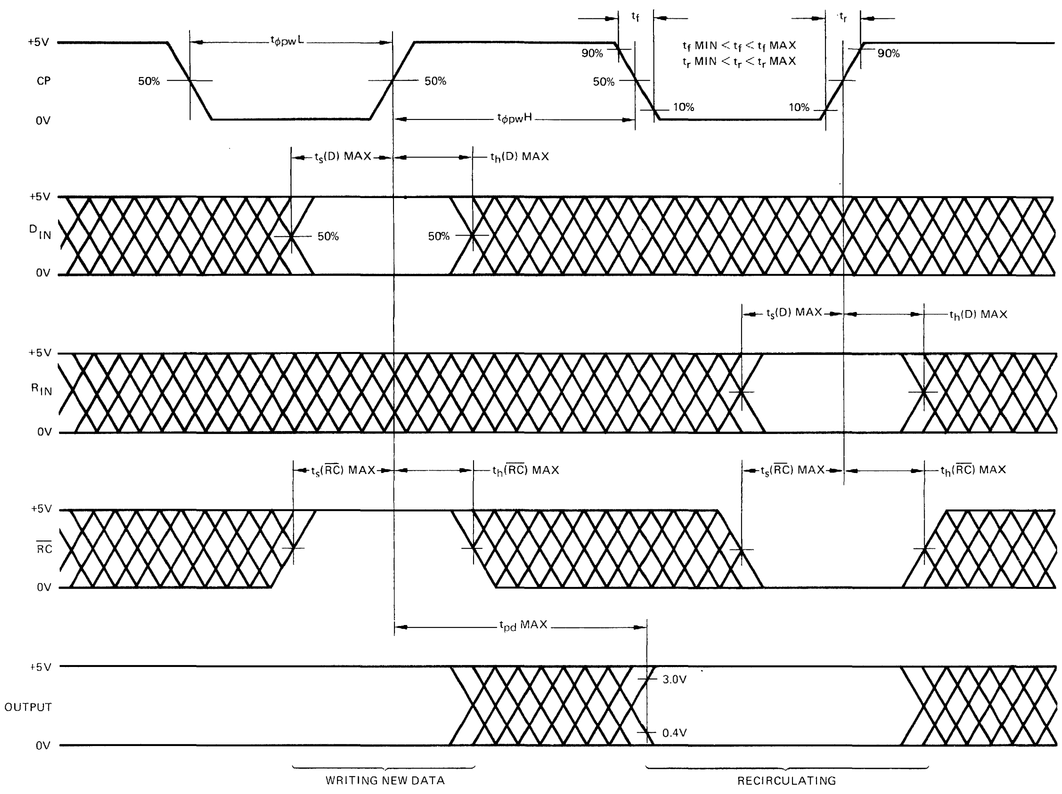
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| | | | Am2810 | | | Am1002P/ Am1002L | | | |
|---|---|---|---|---|---|---|---|---|---|
| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
| $f_{max}$ | Maximum Clock Frequency | | 2.0 | | | 1.0 | | | MHz |
| $t_{\phi pw}H$ | Clock HIGH Time | | 0.2 | | ∞ | 0.4 | | ∞ | μs |
| $t_{\phi pw}L$ | Clock LOW Time | | 0.2 | | 100 | 0.3 | | 10 | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | 10 | | 200 | 10 | | 200 | ns |
| $t_s(D)$ | Set-up Time, D or R Inputs (see definitions) | $t_r = t_f$ = 50ns, $V_R$ = −12V | | | 100 | | | 50 | ns |
| $t_h(D)$ | Hold Time, D or R Inputs (see definitions) | $t_r = t_f$ = 50ns, $V_R$ = −12V | | | 100 | | | 200 | ns |
| $t_s(\overline{RC})$ | Set-up Time, $\overline{RC}$ Input (see definitions) | | | | 100 | | | 100 | ns |
| $t_h(\overline{RC})$ | Hold Time, $\overline{RC}$ Input (see definitions) | | | | 200 | | | 300 | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 2.9kΩ, $C_L$ = 20pF | (Note 4) | | 250 | (Note 4) | | 450 | ns |
| $t_{pr}$, $t_{pf}$ | Output Rise and Fall Times | 10% to 90% | | | 100 | | | 150 | ns |
| $C_{in}$ | Capacitance, Any Input (Note 3) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | 3 | 7 | | 3 | 10 | pF |

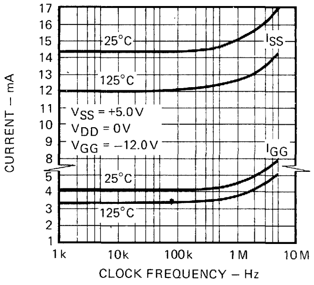
Notes: 3. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

4. At any temperature, $t_{pd}$ min. is always much greater than $t_h$(D) max.

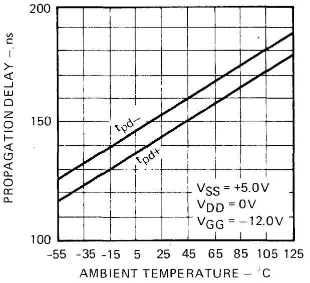
## TIMING DIAGRAM


+5V
CP
0V
50%
$t_{\phi pwL}$
50%
$t_{\phi pwH}$
$t_f$
$t_r$
90%
50%
10%
10%
90%
$t_f$ MIN < $t_f$ < $t_f$ MAX
$t_r$ MIN < $t_r$ < $t_r$ MAX
$t_s$(D) MAX
$t_h$(D) MAX
+5V
$D_{IN}$
0V
50%
50%
$t_s$(D) MAX
$t_h$(D) MAX
+5V
$R_{IN}$
0V
$t_s(\overline{RC})$ MAX
$t_h(\overline{RC})$ MAX
$t_s(\overline{RC})$ MAX
$t_h(\overline{RC})$ MAX
+5V
$\overline{RC}$
0V
$t_{pd}$ MAX
+5V
OUTPUT
0V
3.0V
0.4V
WRITING NEW DATA
RECIRCULATING

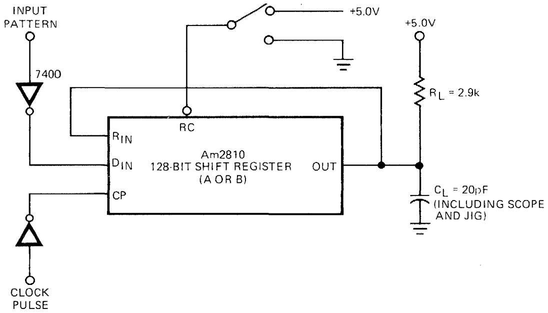
### Typical Power-Supply Currents Versus Frequency



### Typical Propagation Delay Versus Ambient Temperature



### TEST CIRCUIT

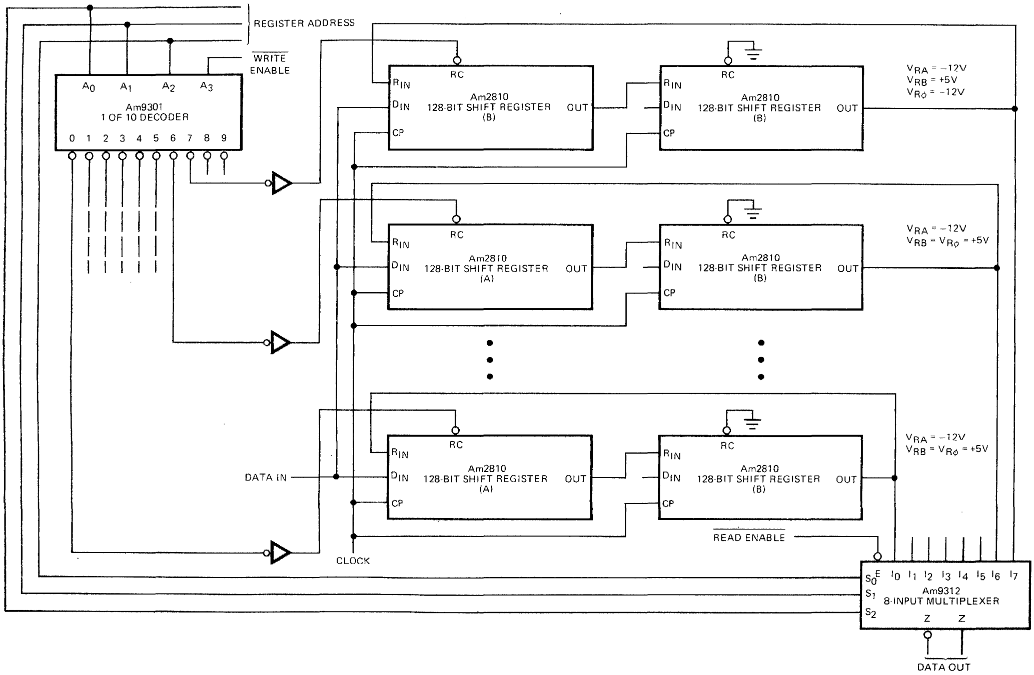

INPUT PATTERN
7400
+5.0V
+5.0V
$R_L$ = 2.9k
RC
$R_{IN}$
$D_{IN}$
CP
Am2810
128-BIT SHIFT REGISTER
(A OR B)
OUT
$C_L$ = 20pF
(INCLUDING SCOPE AND JIG)
CLOCK PULSE

## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

## APPLICATIONS

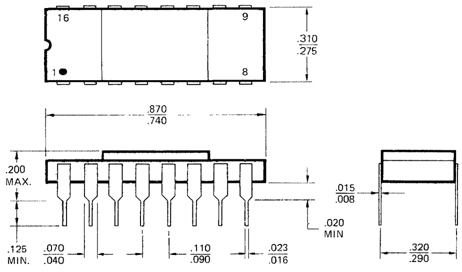

REGISTER ADDRESS
WRITE ENABLE
A0 A1 A2 A3
Am9301
1 OF 10 DECODER
0 1 2 3 4 5 6 7 8 9
RC
RIN
DIN
CP
Am2810
128-BIT SHIFT REGISTER
(A)
(B)
OUT
VRA = −12V
VRB = +5V
VRφ = −12V
VRA = −12V
VRB = VRφ = +5V
DATA IN
CLOCK
READ ENABLE
S0 E I0 I1 I2 I3 I4 I5 I6 I7
S1
S2
Am9312
8-INPUT MULTIPLEXER
Z Z
DATA OUT

### Eight Register 256-Bit Memory System

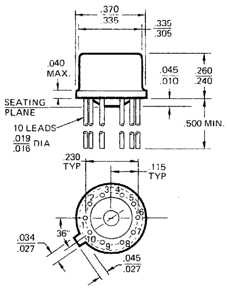
Data enters one of the eight 256-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same. Note that the $V_{R\phi}$ input is connected to $V_{GG}$ on only one device; the pull-up resistor on this device will pull the line up for all the devices. The $V_{RB}$ inputs are all connected to $V_{SS}$, since only MOS compatibility is needed. The $V_{RA}$ inputs are all connected to $V_{GG}$ because each recirculate input needs a separate pull-up. This also increases the loading on the data input.

## PHYSICAL DIMENSIONS

### Side Brazed Dual-In-Line


16
9
1
8
.310
.275
.870
.740
.200
MAX.
.015
.008
.020
MIN
.125
MIN.
.070
.040
.110
.090
.023
.016
.320
.290

### TO-100

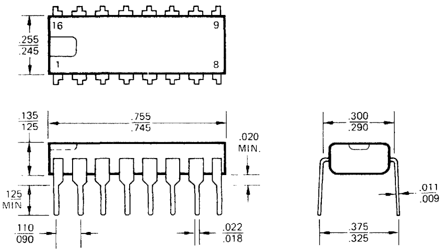

.370
.335
.335
.305
.040
MAX.
.045
.010
.260
.240
SEATING PLANE
10 LEADS
.019
.016
DIA
.500 MIN.
.230
TYP
.115
TYP
.034
.027
36°
.045
.027
1 2 3 4 5 6 7 8 9 10

## TRUTH TABLE

| $\overline{RC}$ | $R_{IN}$ | $D_{IN}$ | Data Entered |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

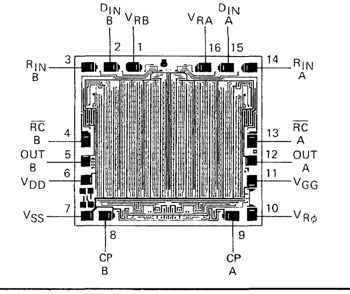
H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

### Molded


16
9
1
8
.255
.245
.135
.125
.755
.745
.020
MIN.
.125
MIN
.110
.090
.022
.018
.300
.290
.011
.009
.375
.325

### Am2810 Metallization and Pad Layout

86 X 95 Mils


DIN B
VRB
VRA
DIN A
2
1
16
15
RIN B
3
14
RIN A
RC B
4
13
RC A
OUT B
5
12
OUT A
VDD
6
11
VGG
VSS
7
10
VRφ
8
9
CP B
CP A

# Am2814/3114

## Dual 128-Bit Static Shift Register

### Distinctive Characteristics

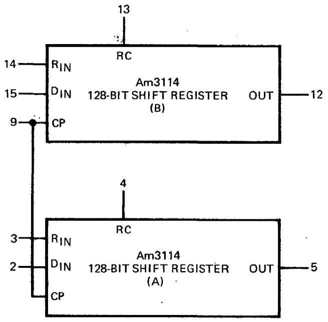
- 2nd Source to Texas Instruments 3114
- Operation guaranteed from DC to 2.5MHz.
- 100% reliability assurance testing in compliance with MIL-STD-883
- Full military grade devices available

### FUNCTIONAL DESCRIPTION

The Am3114 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers each have a two-input multiplexer on their inputs, so that input data may be selected from one of two sources. Both registers have a common clock input, and operate with a low-voltage TTL clock signal. The registers shift on the LOW-to-HIGH edge of the clock signal. Data at the inputs must be steady for a set-up time before and a hold time after this clock transition. Since data storage is static, the clock may be halted indefinitely in the HIGH state. The outputs of each register can drive one TTL load or three Am93L low-power TTL loads.

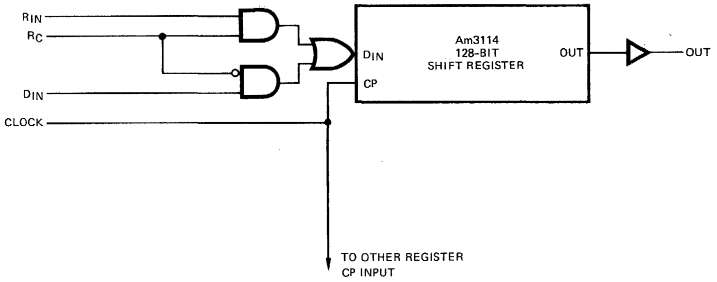
The two-input multiplexer on the input of each register is controlled by the RC (recirculate control) input. When RC is LOW, data is accepted on the $D_{in}$ input; when RC is HIGH, data is accepted on the $R_{in}$ input. The Am2814 is functionally identical to the Am3114, but is specified with higher performance.

### LOGIC SYMBOL


13
RC
14
R<sub>IN</sub>
15
D<sub>IN</sub>
Am3114
128-BIT SHIFT REGISTER
(B)
OUT
12
9
CP
4
RC
3
R<sub>IN</sub>
2
D<sub>IN</sub>
Am3114
128-BIT SHIFT REGISTER
(A)
OUT
5
CP

$V_{SS}$ = Pin 7
$V_{DD}$ = Pin 6
$V_{GG}$ = Pin 11

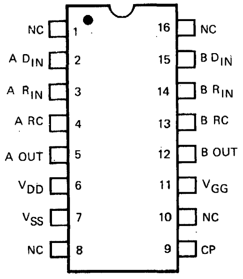
### LOGIC BLOCK DIAGRAM (One Register Shown)


R<sub>IN</sub>
R<sub>C</sub>
D<sub>IN</sub>
CLOCK
D<sub>IN</sub>
Am3114
128-BIT
SHIFT REGISTER
OUT
CP
OUT
TO OTHER REGISTER
CP INPUT

### ORDERING INFORMATION

| Package Type | Temperature Range | Am3114 Order Number | Am2814 Order Number |
|---|---|---|---|
| Molded DIP | −25°C to +85°C | TMS3114NC | AM2814PC |
| Hermetic DIP | −25°C to +85°C | TMS3114JC | AM2814DC |
| Hermetic DIP | −55°C to +125°C | | AM2814DM |

### CONNECTION DIAGRAM


NC 1
A D<sub>IN</sub> 2
A R<sub>IN</sub> 3
A RC 4
A OUT 5
V<sub>DD</sub> 6
V<sub>SS</sub> 7
NC 8
16 NC
15 B D<sub>IN</sub>
14 B R<sub>IN</sub>
13 B RC
12 B OUT
11 V<sub>GG</sub>
10 NC
9 CP

Notes: 1. Pin 1 is marked for orientation.
2. NC = No Connection.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −15V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | $T_A$ | $V_{SS}$ | $V_{GG}$ | $V_{DD}$ |
|---|---|---|---|---|
| Am2814PC, DC<br>Am3114JC, NC | −25°C to +85°C | 5.0V ±5% | −11V to −13V | GND |
| Am2814DM | −55°C to +125°C | 5.0V ±5% | −11.4V to −12.6V | GND |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −200µA | | $V_{SS}$−1 | | | Volts |
| $V_{OH}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | 0.2 | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | Am3114 | 3.5 | | | Volts |
| | | | Am2814 | $V_{SS}$ −1.5 | | | |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.6 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{SS}$ = MAX., $V_{IN}$ = 0.6V | | | | 0.5 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{SS}$ | | | | 0.5 | µA |
| $I_{SS}$ | $V_{SS}$ Power Supply Current | Inputs and Outputs Open<br>f = 1MHz | Am3114 | | 15 | | mA |
| | | | Am2814XC | | 14 | 25 | |
| | | | Am2814XM | | 14 | 35 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | Inputs and Outputs Open<br>f = 1MHz | Am3114 | | −4 | | |
| | | | Am2814XC | | −4 | −10 | |
| | | | Am2814XM | | −4 | −15 | |

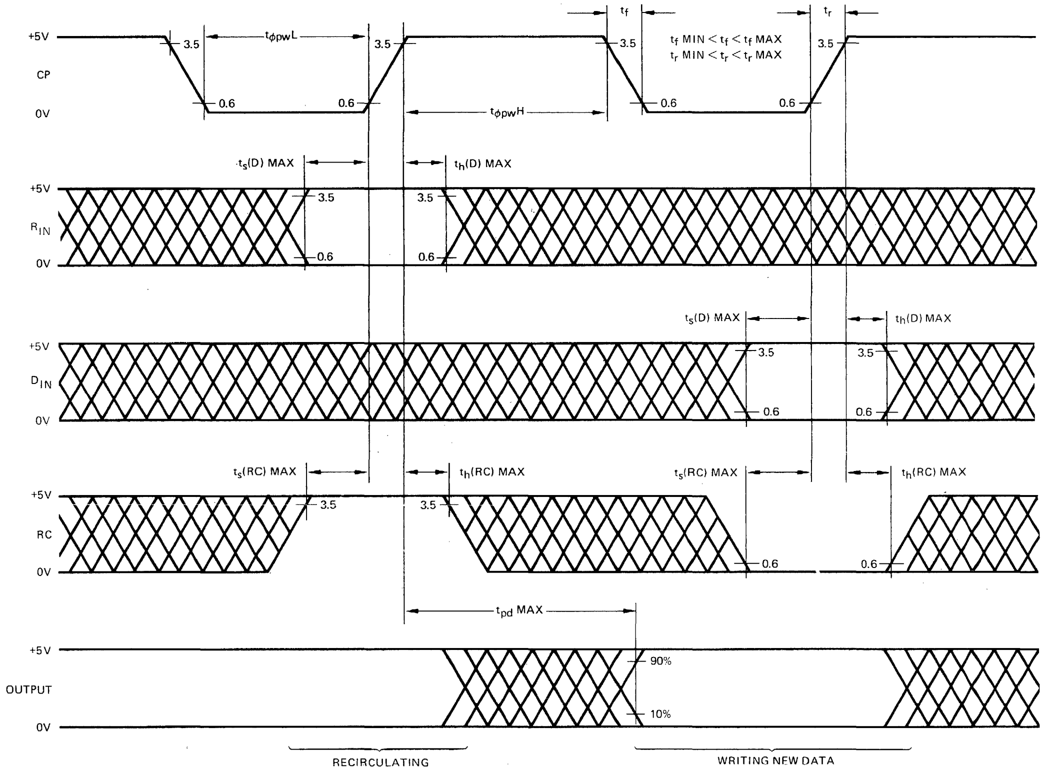
Note 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient and maximum loading.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

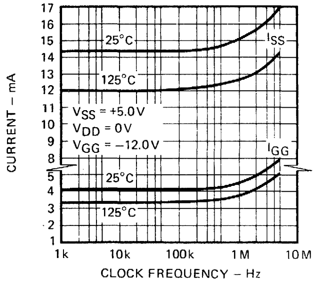
| | | | Am3114 | | | Am2814 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
| $f_{max}$ | Maximum Clock Frequency | | 2.0 | | | 2.5 | | | MHz |
| $t_{\phi pwH}$ | Clock HIGH Time | | .330 | | ∞ | .200 | | ∞ | µs |
| $t_{\phi pwL}$ | Clock LOW Time | | .130 | | 100 | .170 | | 100 | µs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | | 5 | | | 5 | µs |
| $t_s(D)$ | Set-up Time, D or R Inputs (see definitions) | $t_r$ = $t_f$ ≤ 50ns | | | 100 | | | 100 | ns |
| $t_h(D)$ | Hold Time, D or R Inputs (see definitions) | | | | 100 | | | 100 | ns |
| $t_s(RC)$ | Set-up Time, RC Input (see definitions) | | | | 100 | | | 100 | ns |
| $t_h(RC)$ | Hold Time, RC Input (see definitions) | | | | 150 | | | 150 | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 2.7k, $C_L$ = 20pF | | | 350 | (Note 4) | | 250 | ns |
| $t_{pr}$, $t_{pF}$ | Output Rise and Fall Times | 10% to 90% | | | | | | 100 | ns |
| $C_{in}$ | Capacitance, Any Input (Note 3) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | | 13 | | 3 | 7 | pF |

Notes: 3. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
4. At any temperature, $t_{pd}$ min. is always much greater than $t_h(D)$ max.

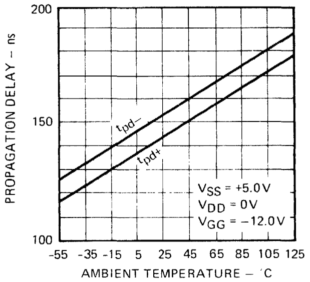
## TIMING DIAGRAM


+5V
CP
0V
3.5
$t_{\phi pwL}$
3.5
0.6
0.6
$t_{\phi pwH}$
$t_f$
$t_r$
3.5
$t_f$ MIN < $t_f$ < $t_f$ MAX
$t_r$ MIN < $t_r$ < $t_r$ MAX
3.5
0.6
0.6
$t_s$(D) MAX
$t_h$(D) MAX
+5V
$R_{IN}$
0V
3.5
0.6
3.5
0.6
$t_s$(D) MAX
$t_h$(D) MAX
+5V
$D_{IN}$
0V
3.5
0.6
3.5
0.6
$t_s$(RC) MAX
$t_h$(RC) MAX
$t_s$(RC) MAX
$t_h$(RC) MAX
+5V
RC
0V
3.5
3.5
0.6
0.6
$t_{pd}$ MAX
+5V
OUTPUT
0V
90%
10%
RECIRCULATING
WRITING NEW DATA

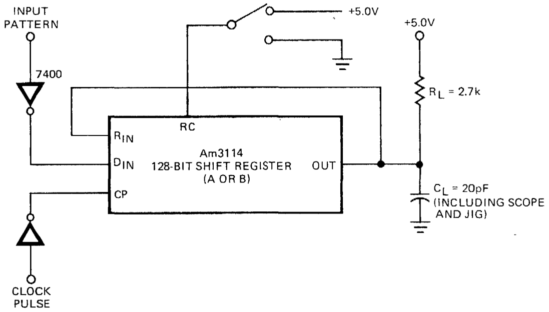
### Typical Power-Supply Currents Versus Frequency



### Typical Propagation Delay Versus Ambient Temperature



### TEST CIRCUIT

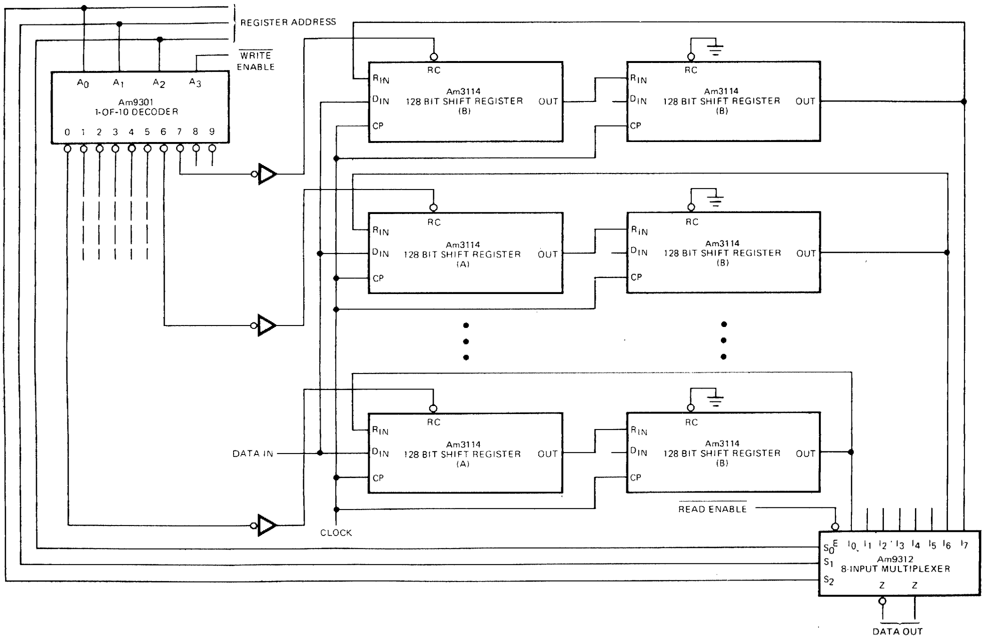

INPUT PATTERN
+5.0V
+5.0V
7400
$R_L$ = 2.7k
$R_{IN}$
RC
$D_{IN}$
Am3114
128-BIT SHIFT REGISTER
(A OR B)
OUT
CP
$C_L$ = 20pF
(INCLUDING SCOPE AND JIG)
CLOCK PULSE

## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

## APPLICATIONS


REGISTER ADDRESS
WRITE ENABLE
A0 A1 A2 A3
Am9301
1-OF-10 DECODER
0 1 2 3 4 5 6 7 8 9
RC
RIN
DIN
CP
Am3114
128 BIT SHIFT REGISTER
(A)
(B)
OUT
DATA IN
CLOCK
READ ENABLE
E
S0 S1 S2
I0 I1 I2 I3 I4 I5 I6 I7
Am9312
8-INPUT MULTIPLEXER
Z Z
DATA OUT

### Eight Register 256-Bit Memory System

Data enters one of the eight 256-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same. Pull-up resistors are required on all register inputs driven from TTL.

## TRUTH TABLE

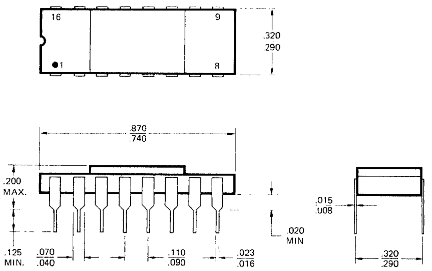
| RC | $D_{IN}$ | $R_{IN}$ | Data Entered |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

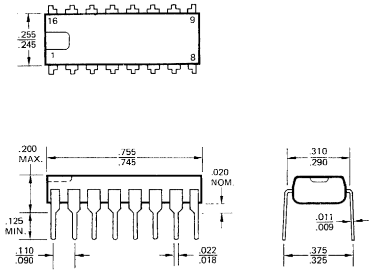
## PHYSICAL DIMENSIONS

### Dual-In-Line

### Side Brazed


16
9
1
8
.320
.290
.870
.740
.200
MAX.
.125
MIN.
.070
.040
.110
.090
.023
.016
.020
MIN
.015
.008
.320
.290

### Molded


16
9
1
8
.255
.245
.200
MAX.
.755
.745
.020
NOM.
.125
MIN.
.110
.090
.022
.018
.310
.290
.011
.009
.375
.325

# Am2825 • Am2826 • Am2827

## 2048-Bit Dynamic Shift Registers

### Distinctive Characteristics

- 6 MHz data rate guaranteed
- Single 2048 and dual 1024-bit configurations
- Low power dissipation
- TTL compatible data inputs and outputs
- On chip recirculate and input select controls
- Plug-in replacement for National 5025/26/27
- Full military temperature range devices available
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

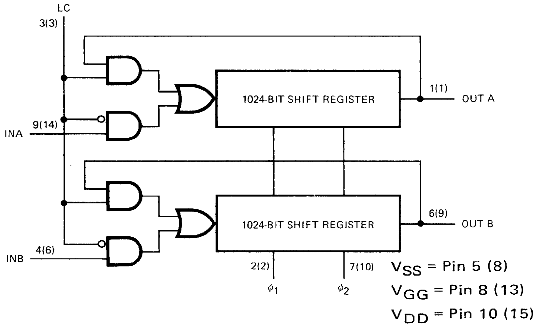
The Am2825/26/27 are military and commercial grade 2048-bit dynamic shift registers. The Am2825 is a dual 1024-bit device with on-chip recirculate and a load control (LC) common to both registers. When LC is HIGH, the two registers recirculate data; when LC is LOW new data is entered through the data inputs. The Am2826 is similar, but each register has two data inputs, selected by separate input select (IS) signals. The Am2827 is a single 2048-bit register with on-chip recirculate and a load control. All the devices can drive one standard TTL load or three Am93L series low-power TTL loads. The select, load command, and data inputs may be driven by TTL signals. Two high-voltage clock signals, $\phi 1$ and $\phi 2$, are required. Internally, each shift register consists of two multiplexed registers, so that a data shift occurs on each $\phi 1$ or $\phi 2$ clock pulse. The data rate, therefore, is double the frequency of either clock signal.

### ORDERING INFORMATION

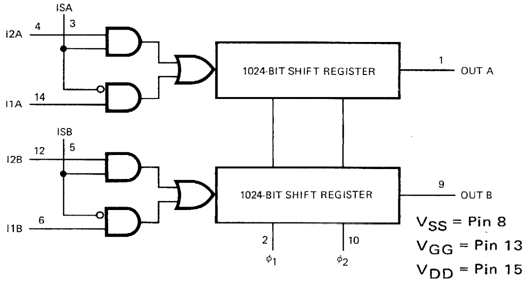
| Package Type | Temperature Range | Order Number |
|---|---|---|
| 10-Pin Molded | 0°C to +70°C | AM2825PC |
| 16-Pin Hermetic | 0°C to +70°C | AM2825DC |
| 16-Pin Hermetic | –55°C to +125°C | AM2825DM |
| 16-Pin Molded | 0°C to +70°C | AM2826PC |
| 16-Pin Hermetic | 0°C to +70°C | AM2826DC |
| 16-Pin Hermetic | –55°C to +125°C | AM2826DM |
| 8-Pin Molded | 0°C to +70°C | AM2827PC |
| 8-Pin Hermetic | –55°C to +125°C | AM2827DM |
| 8-Pin Hermetic | 0°C to +70°C | AM2827DC |

### LOGIC DIAGRAMS

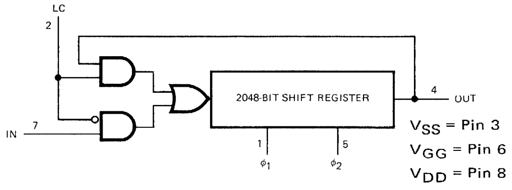
**Am2825**


LC
3(3)
INA
9(14)
1024-BIT SHIFT REGISTER
1(1)
OUT A
INB
4(6)
1024-BIT SHIFT REGISTER
6(9)
OUT B
2(2)
$\phi_1$
7(10)
$\phi_2$
$V_{SS}$ = Pin 5 (8)
$V_{GG}$ = Pin 8 (13)
$V_{DD}$ = Pin 10 (15)

**Am2826**


ISA
I2A 4
3
I1A 14
1024-BIT SHIFT REGISTER
1
OUT A
ISB
I2B 12
5
I1B 6
1024-BIT SHIFT REGISTER
9
OUT B
2
$\phi_1$
10
$\phi_2$
$V_{SS}$ = Pin 8
$V_{GG}$ = Pin 13
$V_{DD}$ = Pin 15

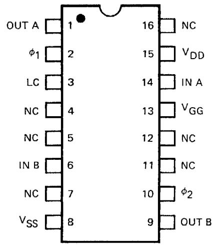
**Am2827**


LC
2
IN 7
2048-BIT SHIFT REGISTER
4
OUT
1
$\phi_1$
5
$\phi_2$
$V_{SS}$ = Pin 3
$V_{GG}$ = Pin 6
$V_{DD}$ = Pin 8

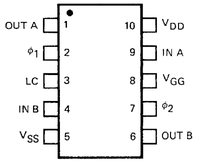
### CONNECTION DIAGRAMS

#### Top View

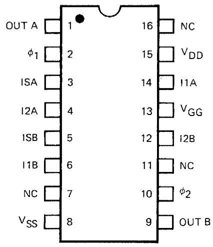
**Am2825**


OUT A 1
$\phi_1$ 2
LC 3
NC 4
NC 5
IN B 6
NC 7
$V_{SS}$ 8
16 NC
15 $V_{DD}$
14 IN A
13 $V_{GG}$
12 NC
11 NC
10 $\phi_2$
9 OUT B

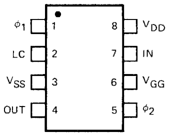
**Am2825**


OUT A 1
$\phi_1$ 2
LC 3
IN B 4
$V_{SS}$ 5
10 $V_{DD}$
9 IN A
8 $V_{GG}$
7 $\phi_2$
6 OUT B

**Am2826**


OUT A 1
$\phi_1$ 2
ISA 3
I2A 4
ISB 5
I1B 6
NC 7
$V_{SS}$ 8
16 NC
15 $V_{DD}$
14 I1A
13 $V_{GG}$
12 I2B
11 NC
10 $\phi_2$
9 OUT B

**Am2827**


$\phi_1$ 1
LC 2
$V_{SS}$ 3
OUT 4
8 $V_{DD}$
7 IN
6 $V_{GG}$
5 $\phi_2$

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| DC Input Voltage with Respect to $V_{SS}$ | −20V to +0.3V |

## OPERATING RANGE

| Part Number | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ | $T_A$ |
|---|---|---|---|---|
| AM2825/6/7DM | +5.0V ±5% | 0 V | −10.0V to −11.0V | −55°C to +125°C |
| AM2825/6/7PC,DC | +5.0V ±5% | 0 V | −10.0V to −11.0V | 0°C to +70°C |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −0.5mA | | 2.4 | | $V_{SS}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | 0.0 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs except clocks | | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs except clocks | | $V_{SS}$ −10 | | $V_{SS}$ −4.2 | Volts |
| $I_I$ | Input Leakage Current | $V_{IN}$ = −10V, $T_A$ = 25°C | | | 10 | 500 | nA |
| $I_\phi$ | Clock Input Leakage Current | $V_\phi$ = −15V, $T_A$ = 25°C | | | 50 | 1000 | nA |
| $V_{\phi H}$ | Clock HIGH Level | | | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_{\phi L}$ | Clock LOW Level | | | $V_{GG}$ −0.3 | | $V_{GG}$ +0.8 | Volts |
| $I_{GG}$ | $V_{GG}$ Current | $T_A$ = 25°C<br>$V_{SS}$ = 5.25V<br>$V_{GG}$ = −11.0V<br>$V_{\phi L}$ = −11.0V<br>$t_{\phi pw}$ = 125ns<br>Data = 11110000. . . | .01MHz<$f_\phi$<0.1MHz | | 2.5 | 5 | mA |
| | | | $f_\phi$ = 1.0MHz | | 2.5 | 5 | |
| | | | $f_\phi$ = 3.0MHz | | 2.5 | 5 | |
| $I_{DD}$ | $V_{DD}$ Current | | .01MHz<$\phi$<0.1MHz | | 4 | 6 | mA |
| | | | $f_\phi$ = 1.0MHz | | 20 | 30 | |
| | | | $f_\phi$ = 3.0MHz | | 45 | 65 | |

Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −10.5V and 25°C ambient.

## SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS OVER OPERATING RANGE

| Parameters | Definition | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_D$ | Data Rate (Note 2) | $T_A$ = 0°C to +70°C | | 0.02 | | 6.0 | MHz |
| | | $T_A$ = −55°C to +125°C | | 0.12 | | 4.0 | |
| $f_\phi$ | Clock Frequency (Note 3) | $T_A$ = 0°C to +70°C | | 0.01 | | 3.0 | |
| | | $T_A$ = −55°C to +125°C | | 0.06 | | 2.0 | |
| $t_{\phi d}$ | Delay Between Clocks (Note 3) | | | 10 | | Note 3 | ns |
| $t_{\phi pw}$ | Clock LOW Time | $t_{\phi t}$ = 20ns | 0°C to +70°C | 0.125 | | 10 | µs |
| | | | −55°C to +125°C | 0.180 | | 10 | |
| $t_{\phi t}$ | Clock Rise and Fall Times | 10% to 90% | | | | 0.5 | µs |
| $t_s$ | Set-Up Time, Data and Select Inputs (See Definitions) | | 0°C to 70°C | | | 40 | ns |
| | | | −55°C to +125°C | | | 60 | |
| $t_h$ | Hold Time, Data and Select Inputs (See Definitions) | | 0°C to 70°C | | | 30 | ns |
| | | | −55°C to +125°C | | | 50 | |
| $t_{pd}$ | Delay, Clock to Data Out | $C_L$ = 15pF | 0°C to +70°C | | | 80 | ns |
| | | | −55°C to +125°C | | | 120 | |
| $C_{(D)}$ | Capacitance, Data Input | Note 4<br>f = 1 MHz, $V_{IN}$ = 0V<br>All other pins at GND | | | | 5 | pF |
| $C_{(S)}$ | Capacitance, Select Input or $L_C$ | | | | | 7 | pF |
| $C_{(\phi)}$ | Capacitance, Clock Input | | | | 175 | 220 | |

Notes: 2. The Data Rate is twice the frequency of either clock phase.

3. The maximum delay between clocks ($\phi_1$ and $\phi_2$ both HIGH) is a function of junction temperature. The junction temperature is a function of ambient temperature and clock duty cycle. See curves for minimum frequency on page 3.

4. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

## TRUTH TABLES

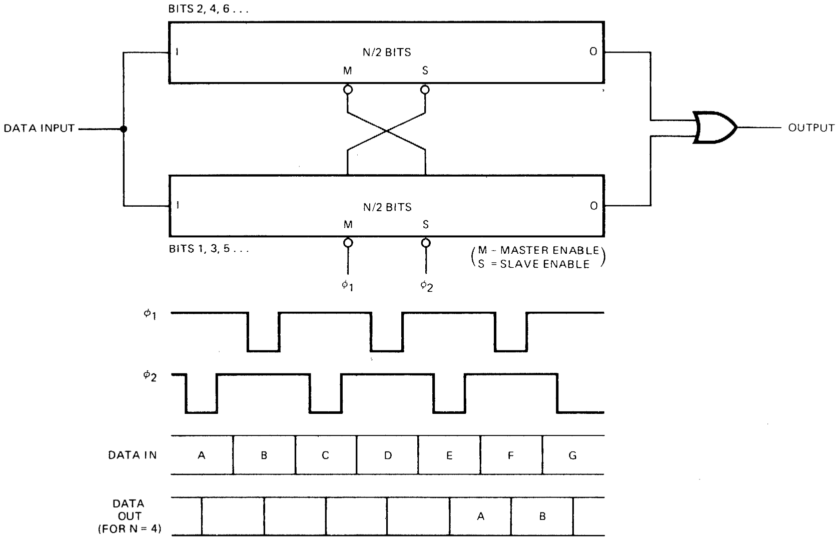
### Am2825 and Am2827

| LC | IN | OUT | DATA ENTERED |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

### Am2826

| IS | INPUT 1 | INPUT 2 | DATA ENTERED |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

## FUNCTIONAL EQUIVALENT OF EACH REGISTER



Since the two registers shift on opposite clock pulses, a new data bit is entered on both $\phi_1$ and $\phi_2$. Data entering the register on $\phi_1$ will appear at the output on $\phi_1$ (from the negative edge of $\phi_1$ to the negative edge of $\phi_2$).

## DEFINITION OF TERMS

**Dynamic Shift Register** A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

**$\phi_1$, $\phi_2$** The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at $V_{SS}$. Data is accepted into the master of each bit during one phase and is transferred to the slave of each bit during the other phase.

**$t_{\phi d}$** Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-toLOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

**$t_{\phi pw}$** Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

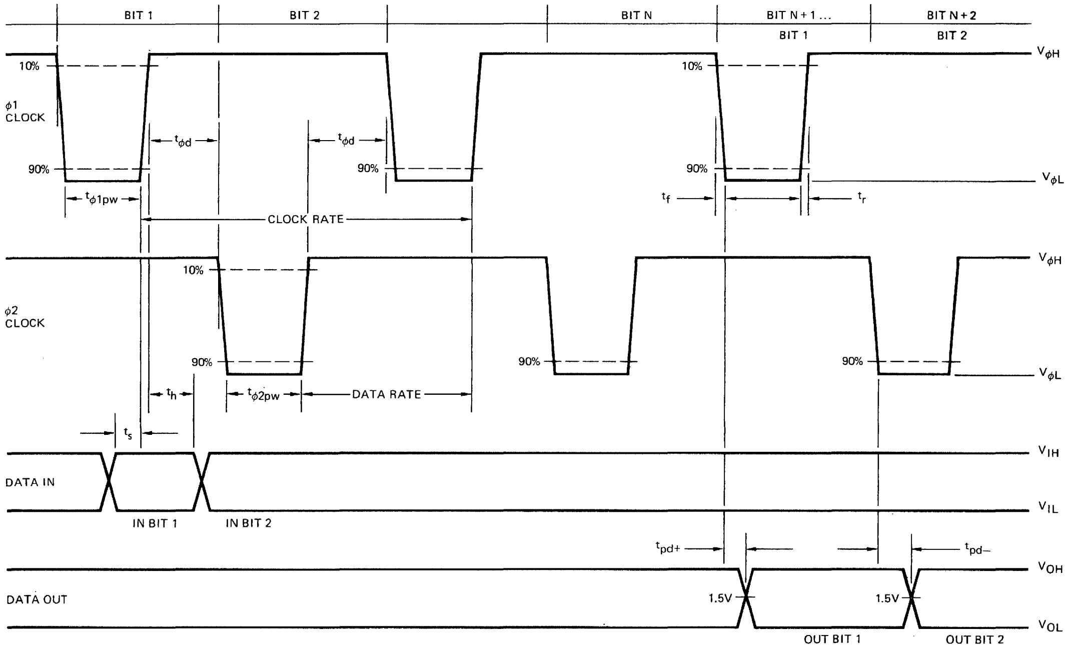
**$t_{\phi t}$** Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

**$t_s$(D)** Data set-up time. The time prior to the LOW-to-HIGH transition of $\phi$ during which the data on the data input must be steady to be correctly written into the memory.

**$t_h$(D)** Data hold time. The time following the LOW-to-HIGH transition of $\phi$ during which the data must be steady. To correctly write data into the register, the data must be applied by $t_s$(D) before this transition and must not be changed until $t_h$(D) after this transition.

**$t_{pd}$** The delay from a HIGH-to-LOW clock transition to correct data present at the register output.

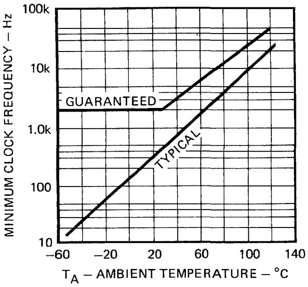
## SWITCHING WAVEFORMS


BIT 1
BIT 2
BIT N
BIT N+1...
BIT 1
BIT N+2
BIT 2
V_φH
10%
φ1 CLOCK
t_φd
t_φd
90%
t_φ1pw
CLOCK RATE
t_f
t_r
V_φL
φ2 CLOCK
t_h
t_φ2pw
DATA RATE
t_s
DATA IN
V_IH
V_IL
IN BIT 1
IN BIT 2
t_pd+
t_pd−
DATA OUT
1.5V
V_OH
V_OL
OUT BIT 1
OUT BIT 2

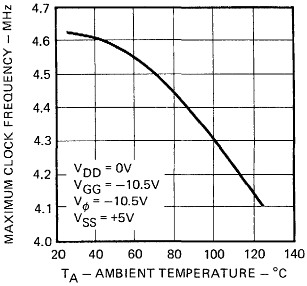
Clock Rise Time 20ns
Clock Fall Time 20ns
Output Load 1 TTL Load

## OPERATING CHARACTERISTICS

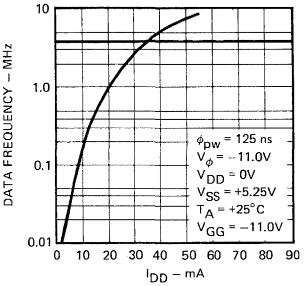
**Guaranteed Minimum Clock Frequency Versus Temperature**



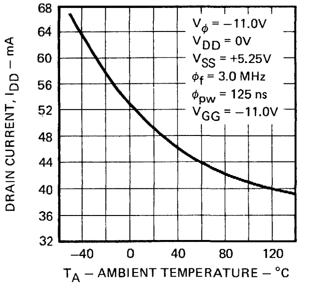
**Maximum Clock Frequency Versus Temperature**



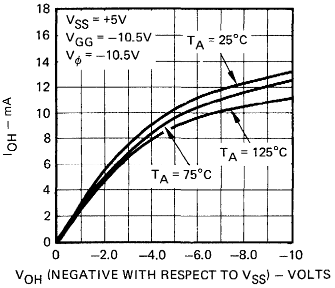
**Typical Power Supply Current Versus Data Rate**



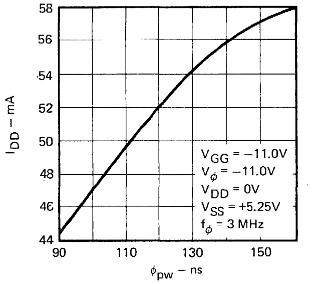
**Typical Power Supply Current Versus Temperature**



**$V_{OH}$ Versus $I_{OH}$**

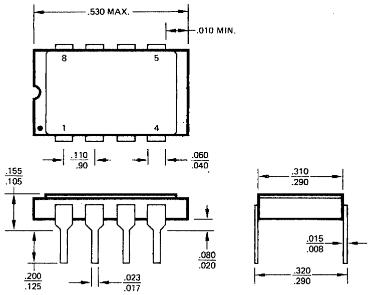


**Typical Power Supply Current Versus Clock Pulse Width $t_{\phi pw}$**

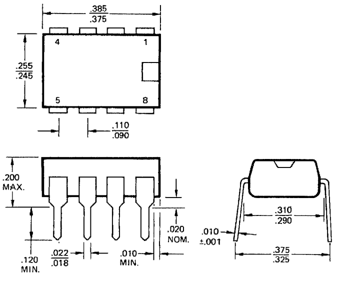


## PHYSICAL DIMENSIONS

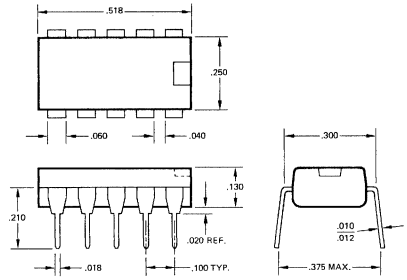
### 8-Pin Side Brazed


.530 MAX.
.010 MIN.
8
5
1
4
.110
.90
.060
.040
.155
.105
.080
.020
.200
.125
.023
.017
.310
.290
.015
.008
.320
.290

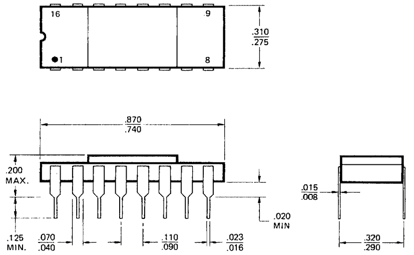
### 8-Pin Molded


.385
.375
4
1
.255
.245
5
8
.110
.090
.200
MAX.
.020
NOM.
.010
±.001
.120
MIN.
.022
.018
.010
MIN.
.310
.290
.375
.325

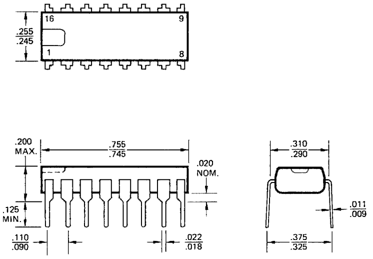
### 10-Pin Molded


.518
.250
.060
.040
.300
.130
.210
.020 REF.
.010
.012
.018
.100 TYP.
.375 MAX.

### 16-Pin Side Brazed

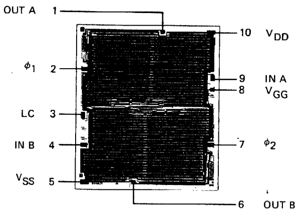

16
9
1
8
.310
.275
.870
.740
.200
MAX.
.015
.008
.020
MIN
.125
MIN.
.070
.040
.110
.090
.023
.016
.320
.290

### 16-Pin Molded


16
9
1
8
.255
.245
.200
MAX.
.755
.745
.020
NOM.
.125
MIN.
.110
.090
.022
.018
.310
.290
.011
.009
.375
.325

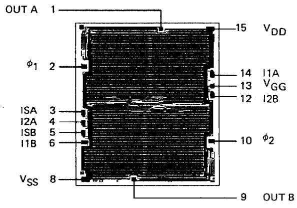
## Metallization and Pad Layouts

### Am2825


OUT A 1
$\phi_1$ 2
LC 3
IN B 4
$V_{SS}$ 5
10 $V_{DD}$
9 IN A
8 $V_{GG}$
7 $\phi_2$
6 OUT B

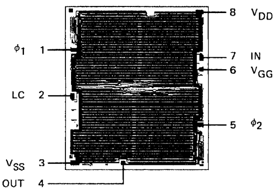
DIE SIZE 0.145" X 0.162"

### Am2826


OUT A 1
$\phi_1$ 2
ISA 3
I2A 4
ISB 5
I1B 6
$V_{SS}$ 8
15 $V_{DD}$
14 I1A
13 $V_{GG}$
12 I2B
10 $\phi_2$
9 OUT B

DIE SIZE 0.145" X 0.162"

### Am2827


$\phi_1$ 1
LC 2
$V_{SS}$ 3
OUT 4
8 $V_{DD}$
7 IN
6 $V_{GG}$
5 $\phi_2$

DIE SIZE 0.145" X 0.162"

# Am2833/2533

## 1024-Bit Static Shift Registers

### Distinctive Characteristics

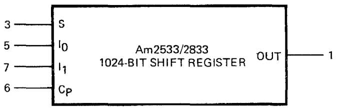
- Second source to Signetics 2533
- All inputs are low-level DTL/TTL compatible
- Static operation with single clock input.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- DC to 2.0MHz operation with Am2833

### FUNCTIONAL DESCRIPTION

The Am2533/2833 is a quasi-static 1024-bit MOS shift register using low-threshold P-channel silicon gate technology.

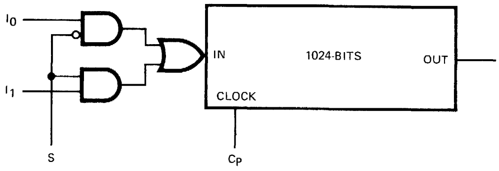
The device has a single TTL/DTL compatible clock input, Cp. Data in the register is stored in static, cross-coupled latches while the clock is LOW, so that the clock may be stopped indefinitely in the LOW state. When the clock shifts from LOW to HIGH to LOW a dynamic transfer of data occurs from one static latch to the next. The input of the register is a two-input multiplexer with both data inputs available. A select line, S, determines whether data will be accepted from the $I_0$ input (S = LOW) or the $I_1$ input (S = HIGH). The register can be placed in the recirculate mode by tying the output, O, to one of the data inputs, and using the select line as a write/recirculate control. The Am2833 is functionally identical to the Am2533 but has superior performance over an extended temperature range.

### LOGIC SYMBOL



$V_{CC}$ = Pin 8
$V_{GG}$ = Pin 2
$V_{DD}$ = Pin 4

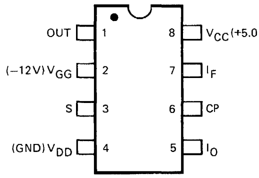
### LOGIC DIAGRAM



### ORDERING INFORMATION

| Package Type | Temperature Range | Am2533 Order Number | Am2833 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM2533V | AM2833PC |
| Hermetic DIP | 0°C to +70°C | AM2533DC | AM2833DC |
| Hermetic DIP | −55°C to +125°C | | AM2833DM |

### CONNECTION DIAGRAM
Top View



Note: Pin 1 marked for orientation

## MAXIMUM RATING (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Temperature (Ambient) Under Bias | –55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{CC}$ –20 V to $V_{CC}$ +0.3 V |
| $V_{GG}$ Supply Voltage | $V_{CC}$ –20 V to $V_{CC}$ +0.3 V |
| DC Input Voltage | $V_{CC}$ –20 V to $V_{CC}$ +0.3 V |

## OPERATING RANGE

| Part No. | Temperature | $V_{CC}$ | $V_{GG}$ | $V_{DD}$ |
|---|---|---|---|---|
| Am2833PC/Am2533PC<br>Am2833DC/Am2533DC | 0°C to +70°C | 5.0 V ±5% | –12 V ±5% | 0 V |
| Am2833DM | –55°C to +125°C | 5.0 V ±5% | –12 V ±5% | 0 V |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = –100μA | | 2.4 | 3.5 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 1.6mA | | | 0.2 | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | Am2533 | $V_{CC}$–1.8 | | $V_{CC}$+0.3 | Volts |
| | | | Am2833 (Note 3) | 2.0 | | $V_{CC}$+0.3 | |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | $V_{GG}$ | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0V, $T_A$ = 25°C | | | 10 | 500 | nA |
| $I_{IH}$ | Input HIGH Current | $T_A$ = 25°C, $V_{IN}$ = $V_{CC}$ –1.0 (Note 3) | | –150 | –300 | –500 | μA |
| $I_{IT}$ | Peak input transition current (Note 3) | 2.5 ≤ V –$V_{IN}$ ≤ 4.0, $T_A$ = 25°C | | | | –1.6 | mA |
| $V_{Imax}$ | Voltage at maximum input current | $T_A$ = 25°C | | $V_{SS}$–4.0 | $V_{SS}$–3.0 | $V_{SS}$–2.5 | V |
| $I_{CC}$ | $V_{CC}$ Power Supply Current | f = 1.5MHz | Am2533 | | 16 | 30 | mA |
| | | f = 2.0MHz | Am2833PC, DC | | 16 | 54 | |
| | | | Am2833DM | | 20 | 70 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | f = 1.5MHz | Am2533 | | –5.0 | –7.5 | mA |
| | | f = 2.0MHz | Am2833PC, DC | | –5.0 | –14 | |
| | | | Am2833DM | | –7.0 | –18 | |

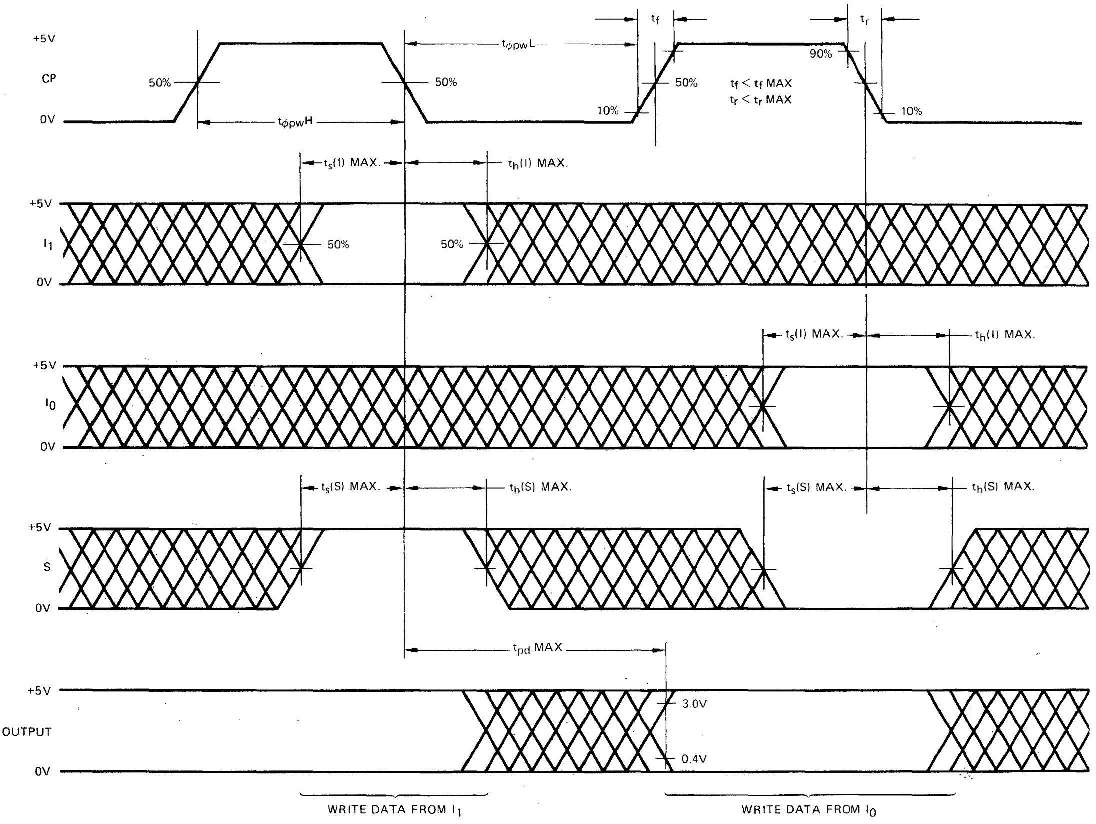
Notes: 1. Typical limits are at $V_{CC}$ = 5.0V, $V_{GG}$ = –12V, 25°C ambient.
2. Power supply currents are with inputs and outputs open.
3. A special input pull-up circuit becomes active at $V_{IN}$ = $V_{SS}$ –3.5V to pull the internal input node up to the MOS threshold. To return the internal node to the LOW state, current must be drawn from the MOS input. This current is maximum at approximately 2.0V.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| | | | Am2533 | | | Am2833 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Parameters | Description | Test Conditions | Min. | Typ. (Note 1) | Max. | Min. | Typ. (Note 1) | Max. | Units |
| $f_{max}$ | Maximum Clock Frequency | | 1.5 | 2.0 | | 2.0 | 3.0 | | MHz |
| $t_{\phi pwL}$ | Clock LOW Time | | 0.250 | | ∞ | 0.200 | | ∞ | μs |
| $t_{\phi pwH}$ | Clock HIGH Time | | 0.350 | | 100 | 0.250 | | 100 | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | | 1 | | | 1 | μs |
| $t_s$(I) | Set-up Time, $I_0$ or $I_1$ Input (see definitions) | $t_r$ = $t_f$ ≤ 25ns | | | 50 | | | 50 | ns |
| $t_h$(I) | Hold Time, $I_0$ or $I_1$ Input (see definitions) | | | | 50 | | | 50 | ns |
| $t_s$(S) | Set-up Time, S Input (see definitions) | | | | 80 | | | 80 | ns |
| $t_h$(S) | Hold Time, S Input (see definitions) | | | | 50 | | | 50 | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 2.9k, $C_L$ = 20pF | | | 300 | | | 300 | ns |
| $t_{pr}$, $t_{pf}$ | Output Rise and Fall Times | 10% to 90% | | | 150 | | | 150 | ns |
| $C_{in}$ | Capacitance, Any Input (Note 2) | f = 1 MHz, $V_{IN}$ = $V_{CC}$ | | 3 | 5 | | 3 | 5 | pF |

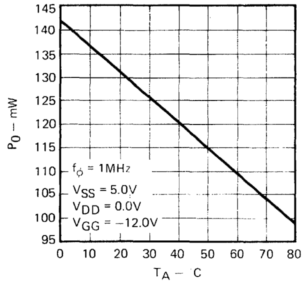
Notes: 1. Typical limits are at $V_{CC}$ = 5.0V, $V_{GG}$ = –12.0V and $T_A$ = 25°C
2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

## TIMING DIAGRAM

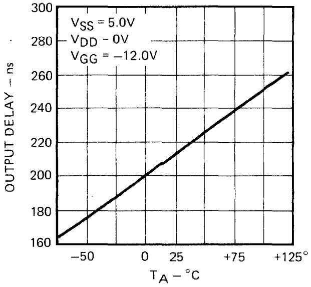

+5V
CP
0V
50%
50%
tφpwH
tφpwL
tf
tr
90%
10%
50%
10%
tf < tf MAX
tr < tr MAX
ts(I) MAX.
th(I) MAX.
+5V
I1
0V
50%
50%
+5V
I0
0V
ts(I) MAX.
th(I) MAX.
ts(S) MAX.
th(S) MAX.
ts(S) MAX.
th(S) MAX.
+5V
S
0V
tpd MAX
+5V
OUTPUT
0V
3.0V
0.4V
WRITE DATA FROM I1
WRITE DATA FROM I0

## TYPICAL PERFORMANCE CURVES

### Power Dissipation Versus Ambient Temperature



### tpd as a Function of Ambient Temperature

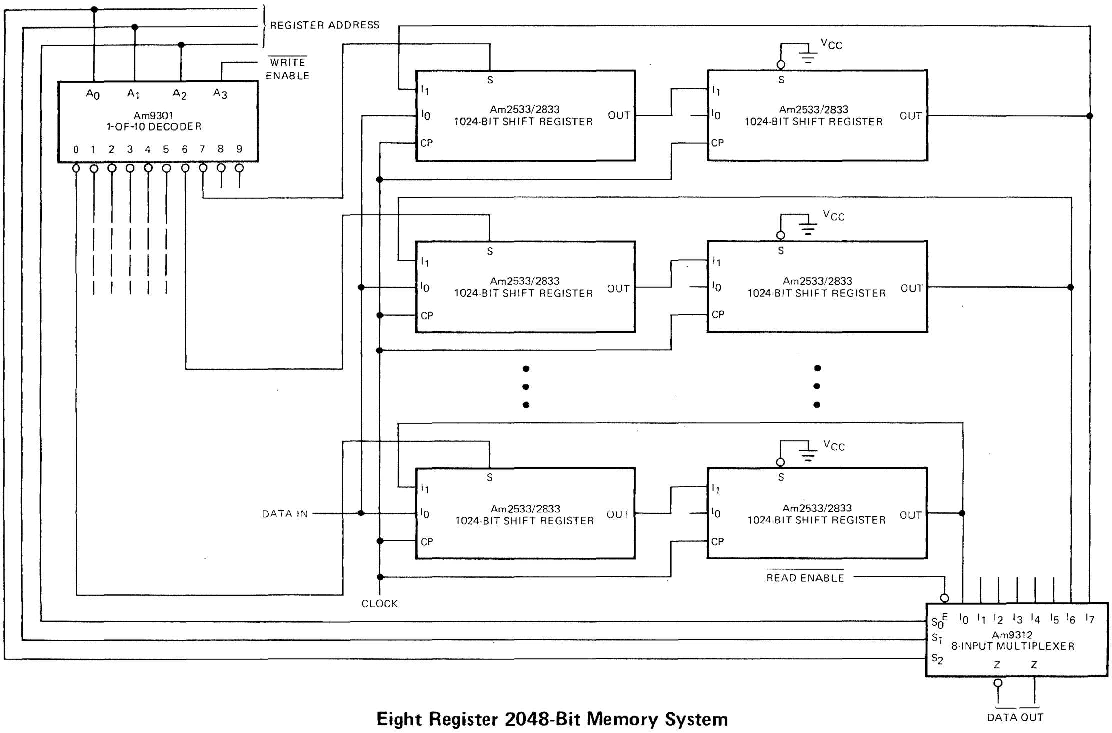


## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

## APPLICATIONS

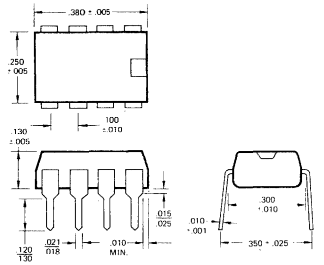

REGISTER ADDRESS
WRITE ENABLE
A0 A1 A2 A3
Am9301
1-OF-10 DECODER
0 1 2 3 4 5 6 7 8 9
S
I1
I0
CP
Am2533/2833
1024-BIT SHIFT REGISTER
OUT
VCC
DATA IN
CLOCK
READ ENABLE
S0 E
S1
S2
I0 I1 I2 I3 I4 I5 I6 I7
Am9312
8-INPUT MULTIPLEXER
Z Z
DATA OUT

**Eight Register 2048-Bit Memory System**

Data enters one of the eight 2048-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same.

## PHYSICAL DIMENSIONS

### Molded 8-Pin DIP

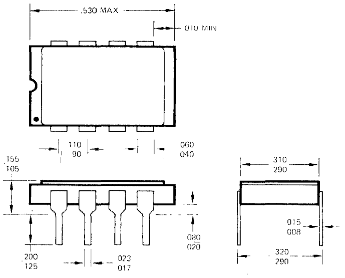

.380 ± .005
.250 ± .005
.130 ± .005
.100 ± .010
.015 .025
.010 ± .001
.300 ± .010
.350 ± .025
.021 .018
.010 MIN.
.120 .130

## TRUTH TABLE

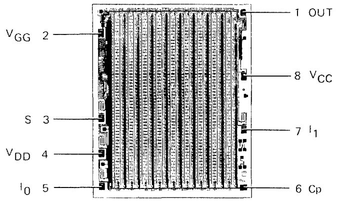
| S | $I_0$ | $I_1$ | Data Entered |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

### Hermetic 8-Pin DIP


.530 MAX
.010 MIN
.110 .90
.060 .040
.155 .105
.310 .290
.015 .008
.080 .020
.200 .125
.023 .017
.320 .290

### Metallization and Pad Layout


VGG 2
S 3
VDD 4
I0 5
1 OUT
8 VCC
7 I1
6 Cp

DIE SIZE: 0.133" X 0.163"

# Am2847 • Am2896

## Quad 80-Bit and Quad 96-Bit Static Shift Registers

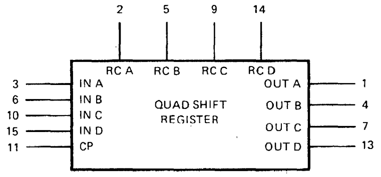
### Distinctive Characteristics

- Plug-in replacement for 2532B, TMS3120, TMS 3409, MK1007, 3347
- Internal recirculates on each register
- Single TTL compatible clock
- Outputs sink two TTL loads
- Operation guaranteed from DC to 3 MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

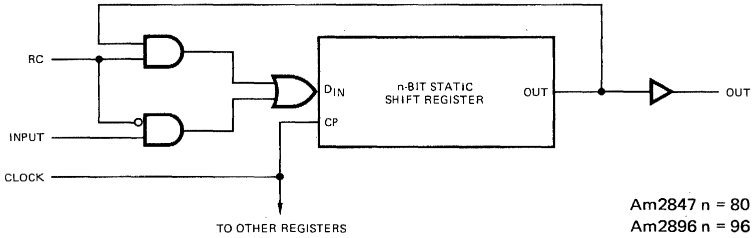
The Am2847 and Am2896 are quad 80-and 96-bit static MOS shift registers. Each device contains four shift registers, each with a TTL-compatible input, output, and recirculate control. When the RC signal is LOW, the corresponding register accepts data from its data input; when RC is HIGH, the data at the register output is written back in at the input. The four registers are driven by a common TTL compatible clock input. The registers shift on the HIGH-to-LOW transition of the clock. Storage is dynamic while the clock is HIGH and static while the clock is LOW, so the clock may be stopped indefinitely in the LOW state. Each register output can drive two TTL unit loads.

### LOGIC SYMBOL


2
5
9
14
RC A
RC B
RC C
RC D
3
6
10
15
11
IN A
IN B
IN C
IN D
CP
QUAD SHIFT REGISTER
OUT A
OUT B
OUT C
OUT D
1
4
7
13

$V_{SS}$ = Pin 16
$V_{DD}$ = Pin 8
$V_{GG}$ = Pin 12

### LOGIC BLOCK DIAGRAM
(One Register Shown)


RC
INPUT
CLOCK
D_IN
CP
n-BIT STATIC SHIFT REGISTER
OUT
OUT
TO OTHER REGISTERS

Am2847 n = 80
Am2896 n = 96

### ORDERING INFORMATION

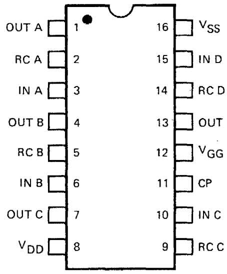
**Am2847 Quad 80-Bit**

| Package Type | Temperature Range | Order Number |
|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | AM2847PC |
| 16-Pin Hermetic DIP | 0°C to +70°C | AM2847DC |
| 16-Pin Hermetic DIP | −55°C to +125°C | AM2847DM |

**Am2896 Quad 96-Bit**

| Package Type | Temperature Range | Order Number |
|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | AM2896PC |
| 16-Pin Hermetic DIP | 0°C to +70°C | AM2896DC |
| 16-Pin Hermetic DIP | −55°C to +125°C | AM2896DM |

### CONNECTION DIAGRAM
Top View


OUT A 1
RC A 2
IN A 3
OUT B 4
RC B 5
IN B 6
OUT C 7
VDD 8
16 VSS
15 IN D
14 RC D
13 OUT D
12 VGG
11 CP
10 IN C
9 RC C

Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am2847DM<br>Am2896DM | −55°C to +125°C | 5.0V ±5% | 0V | −12V ±5% |
| Am2847PC, DC<br>Am2896PC, DC | 0°C to +70°C | 5.0V ±5% | 0V | −12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −0.5mA | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 3.2mA | 0°C to 70°C | | | 0.4 | Volts |
| | | $I_{OL}$ = 2.4mA | −55° to 125°C | | | | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | $V_{SS}$ −18.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = −5.0V, all other pins connected to $V_{SS}$ | | | | 1.0 | μA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4V | | | −1.0 | −1.6 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{SS}$ −1.0V | | −0.1 | | | mA |
| $I_{DD}$ | $V_{DD}$ Power Supply Current | Output open, f = 2.5MHz | 0°C to 70°C | | 25 | 35 | mA |
| | | | −55°C to 125°C | | | 45 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | | 0°C to 70°C | | 10 | 15 | |
| | | | −55°C to 125°C | | | 20 | |

Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient.

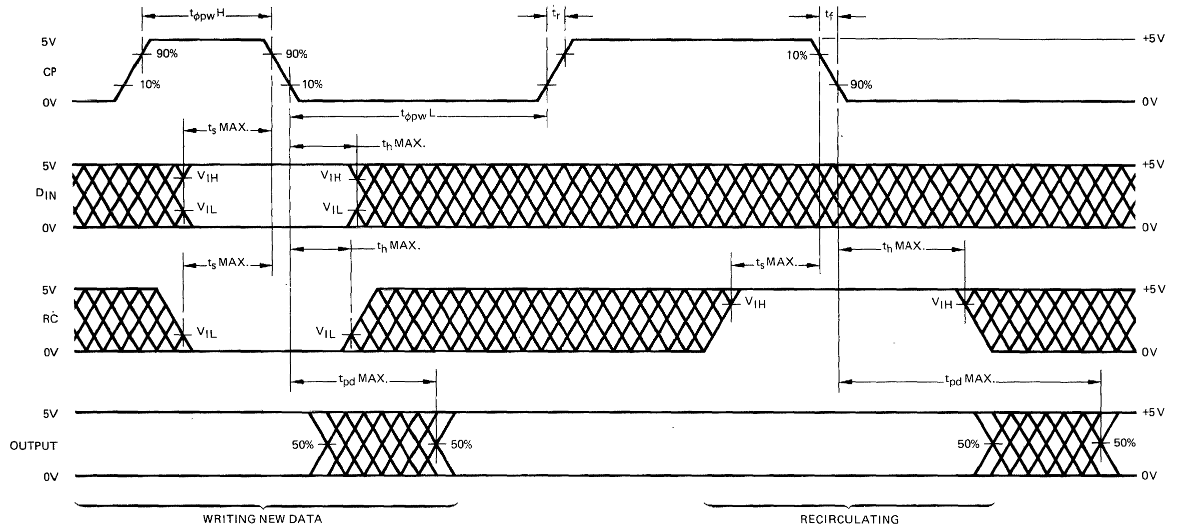
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| f | Clock Frequency | 0°C to 70°C | | 0 | | 3.0 | MHz |
| | | −55°C to 125°C | | | | 2.5 | |
| $t_{\phi pwH}$ | Clock HIGH Time | 0°C to 70°C | | .140 | | 100 | μs |
| | | −55°C to 125°C | | .150 | | 10 | |
| $t_{\phi pwL}$ | Clock LOW Time | 0°C to 70°C | | .140 | | ∞ | μs |
| | | −55°C to 125°C | | .180 | | | |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | 10 | | 200 | ns |
| $t_s$ | Set-Up Time, D or RC Inputs (see definitions) | $t_r = t_f$ = 10ns | 0°C to 70°C | | | 120 | ns |
| | | | −55°C to 125°C | | | 120 | |
| $t_h$ | Hold Time, D or RC Inputs (see definitions) | $t_r = t_f$ = 10ns | 0°C to 70°C | | | 40 | ns |
| | | | −55°C to 125°C | | | 60 | |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 4k, $C_L$ = 10pF | 0°C to 70°C | (Note 3) | | 200 | ns |
| | | | −55°C to 125°C | | | 280 | |
| $C_{in}$ | Capacitance, Data Clock and RC Inputs (Note 2) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | | 3.0 | 7.0 | pF |
| $C_{\phi}$ | Capacitance, Clock Input (Note 2) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | | 3.0 | 7.0 | pF |

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

3. At any temperature, $t_{pd}$ min. is always much greater than $t_h$(D) max.

## TIMING DIAGRAM

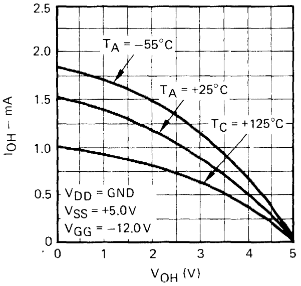


## KEY TO TIMING DIAGRAM

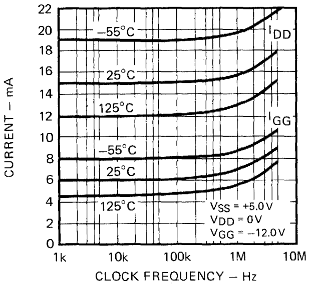
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ──── | MUST BE STEADY | WILL BE STEADY |
| ╲╲╲╲ | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| ╱╱╱╱ | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| ╳╳╳╳ | DON'T CARE: ANY CHANGE PERMITTED | CHANGING: STATE UNKNOWN |

## PERFORMANCE CURVES

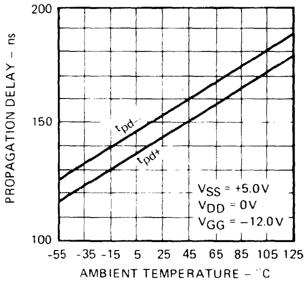
**Typical Data Output HIGH Current Versus Data Output Voltage**



**Typical Power-Supply Currents Versus Frequency**



**Typical Propagation Delay Versus Ambient Temperature**



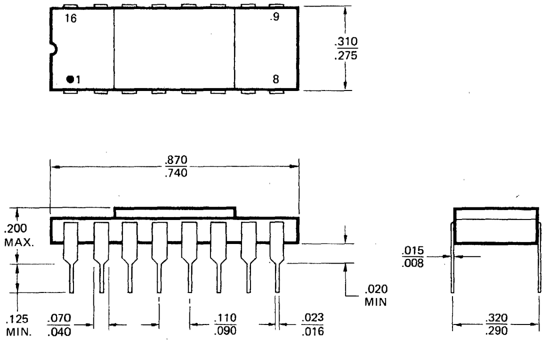
## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

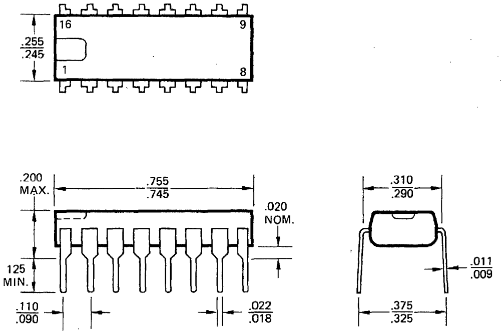
**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

## PHYSICAL DIMENSIONS
### Dual-In-Line

**16-Pin Side Brazed**

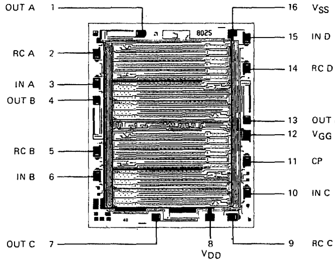

16
9
1
8
.310
.275
.870
.740
.200
MAX.
.125
MIN.
.070
.040
.110
.090
.023
.016
.020
MIN
.015
.008
.320
.290

**16-Pin Molded**


16
9
1
8
.255
.245
.200
MAX.
.755
.745
.020
NOM.
125
MIN.
.110
.090
.022
.018
.310
.290
.011
.009
.375
.325

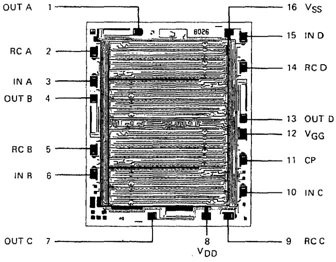
## Metallization and Pad Layouts

**Am2847**


OUT A 1
RC A 2
IN A 3
OUT B 4
RC B 5
IN B 6
OUT C 7
8 $V_{DD}$
9 RC C
10 IN C
11 CP
12 $V_{GG}$
13 OUT D
14 RC D
15 IN D
16 $V_{SS}$
8025

DIE SIZE 0.106" X 0.128"

**Am2896**


OUT A 1
RC A 2
IN A 3
OUT B 4
RC B 5
IN B 6
OUT C 7
8 $V_{DD}$
9 RC C
10 IN C
11 CP
12 $V_{GG}$
13 OUT D
14 RC D
15 IN D
16 $V_{SS}$
8026

DIE SIZE 0.106" X 0.128"

# Am2855 • Am2856 • Am2857

## Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

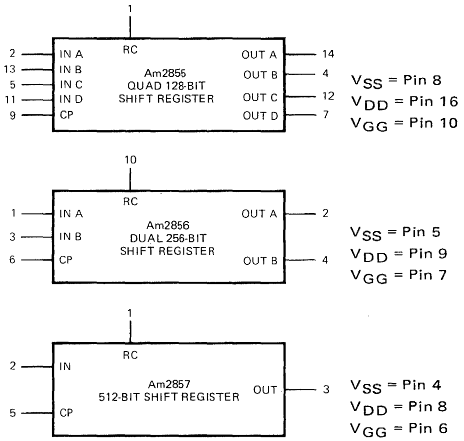
### Distinctive Characteristics

- High-speed replacement for National 5055/6/7
- Internal recirculate
- Single TTL compatible clock
- Operation guaranteed from DC to 2.5MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

These devices are a family of static P-channel MOS shift registers in three configurations. The Am2855 is a quad 128-bit register; the Am2856 is a dual 256-bit register; and the Am2857 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

### LOGIC SYMBOLS

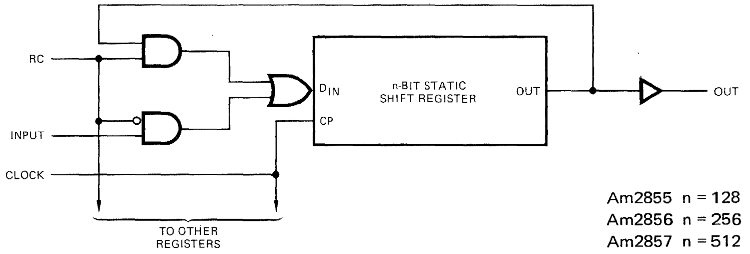

1
RC
2 IN A
13 IN B
5 IN C
11 IN D
9 CP
Am2855
QUAD 128-BIT
SHIFT REGISTER
OUT A 14
OUT B 4
OUT C 12
OUT D 7
10
RC
1 IN A
3 IN B
6 CP
Am2856
DUAL 256-BIT
SHIFT REGISTER
OUT A 2
OUT B 4
1
RC
2 IN
5 CP
Am2857
512-BIT SHIFT REGISTER
OUT 3

$V_{SS}$ = Pin 8
$V_{DD}$ = Pin 16
$V_{GG}$ = Pin 10

$V_{SS}$ = Pin 5
$V_{DD}$ = Pin 9
$V_{GG}$ = Pin 7

$V_{SS}$ = Pin 4
$V_{DD}$ = Pin 8
$V_{GG}$ = Pin 6

### LOGIC BLOCK DIAGRAM
(One Register Shown)


RC
INPUT
CLOCK
$D_{IN}$
CP
n-BIT STATIC
SHIFT REGISTER
OUT
OUT
TO OTHER
REGISTERS

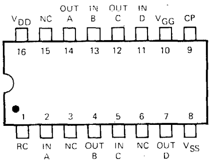
Am2855 n = 128
Am2856 n = 256
Am2857 n = 512

### ORDERING INFORMATION

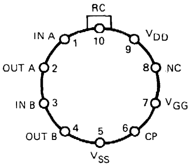
| Package Type | Temperature Range | Order Number |
|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | AM2855PC |
| 16-Pin Hermetic DIP | 0°C to +70°C | AM2855DC |
| 16-Pin Hermetic DIP | –55°C to +125°C | AM2855DM |
| 10-Pin Plastic DIP | 0°C to +70°C | AM2856PC |
| TO-100 Can | 0°C to +70°C | AM2856HC |
| TO-100 Can | –55°C to +125°C | AM2856HM |
| 8-Pin Molded DIP | 0°C to +70°C | AM2857PC |
| 8-Pin Hermetic DIP | 0°C to +70°C | AM2857DC |
| 8-Pin Hermetic DIP | –55°C to +125°C | AM2857DM |

### CONNECTION DIAGRAMS

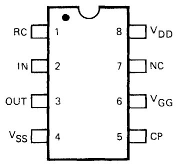
**Am2855**


VDD NC OUT A IN B OUT C IN D VGG CP
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
RC IN A NC OUT B IN C NC OUT D VSS

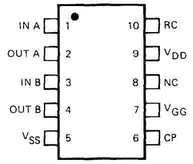
**Am2856**


RC
IN A 1
10 VDD
9
OUT A 2
8 NC
IN B 3
7 VGG
OUT B 4
5
6 CP
VSS

**Am2857**


RC 1
IN 2
OUT 3
VSS 4
8 VDD
7 NC
6 VGG
5 CP

**Am2856**


IN A 1
OUT A 2
IN B 3
OUT B 4
VSS 5
10 RC
9 VDD
8 NC
7 VGG
6 CP

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am2855DM<br>Am2856HM<br>Am2857DM | −55°C to +125°C | 5.0V ±5% | 0V | −12V ±5% |
| Am2855PC, DC<br>Am2856HC<br>Am2857PC, DC | 0°C to +70°C | 5.0V ±5% | 0V | −12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −0.5mA | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | $V_{SS}$ −18.5 | | $V_{SS}$ −4.2 | Volts |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = −10.0V, all other pins GND, $T_A$ = 25°C | | 0.01 | 0.5 | μA |
| $I_{DD}$ | $V_{DD}$ Power Supply Current | $T_A$ = 25°C,<br>$t_{\phi pw}H$ = 160 ns<br>Data = 1010. . .<br>output open<br>f = 2.5 MHz | | 20.0 | 28.0 | mA |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | | | 12.0 | 16.0 | |

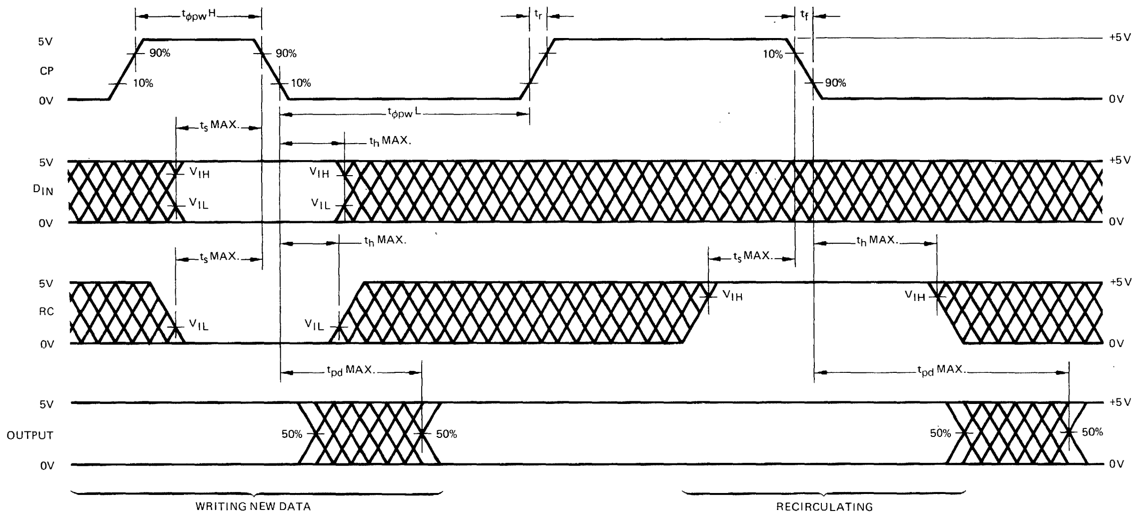
Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient and maximum loading.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| f | Clock Frequency | | 0 | | 2.5 | MHz |
| $t_{\phi pw}H$ | Clock HIGH Time | | 0.16 | | 10.0 | μs |
| $t_{\phi pw}L$ | Clock LOW Time | | 0.200 | | ∞ | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | 10 | | 200 | ns |
| $t_s$ | Set-up Time, D or RC Inputs (see definitions) | $t_r = t_f$ = 50ns | | | 100 | ns |
| $t_h$ | Hold Time, D or RC Inputs (see definitions) | $t_r = t_f$ = 50ns | | | 40 | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 4k, $C_L$ = 10pF | (Note 3) | 160 | 280 | ns |
| $C_{in}$ | Capacitance, Data In and RC Inputs (Note 2) | f = 1MHz, $V_{IN} = V_{SS}$ | | 3 | 7 | pF |
| $C_\phi$ | Capacitance, Clock Input (Note 2) | f = 1MHz, $V_{IN} = V_{SS}$ | | 3 | 7 | pF |

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, $t_{pd}$ min. is always much greater than $t_h$(D) max.

## TIMING DIAGRAM

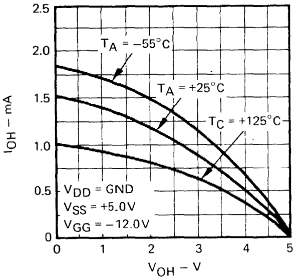


## KEY TO TIMING DIAGRAM

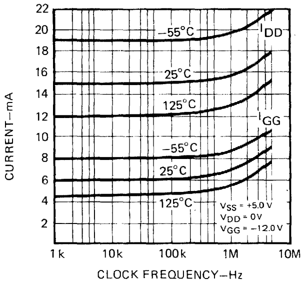
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ━ | MUST BE STEADY | WILL BE STEADY |
| ▥ | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| ▨ | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| ▩ | DON'T CARE: ANY CHANGE PERMITTED | CHANGING: STATE UNKNOWN |

## PERFORMANCE CURVES

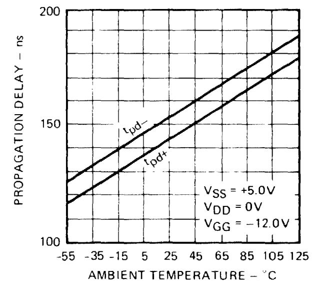
### Typical Data Output HIGH Current Versus Data Output Voltage



### Typical Power-Supply Currents Versus Frequency



### Typical Propagation Delay Versus Ambient Temperature



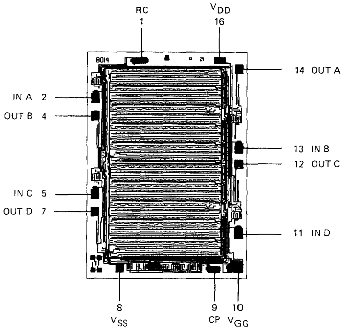
## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

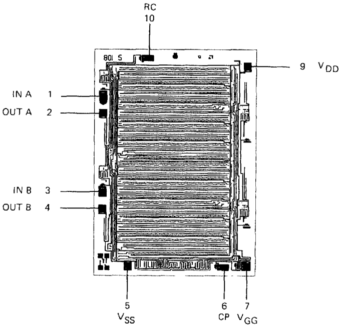
**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

## Metallization and Pad Layouts

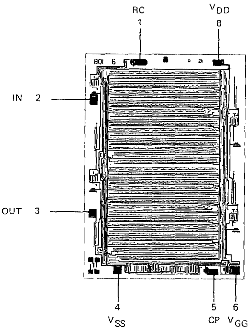
### Am2855


RC
1
VDD
16
14 OUT A
IN A 2
OUT B 4
13 IN B
12 OUT C
IN C 5
OUT D 7
11 IN D
8
VSS
9
CP
10
VGG

### Am2856


RC
10
9 VDD
IN A 1
OUT A 2
IN B 3
OUT B 4
5
VSS
6
CP
7
VGG

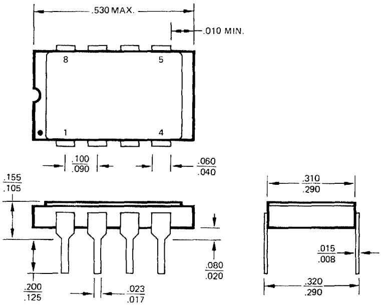
### Am2857


RC
1
VDD
8
IN 2
OUT 3
4
VSS
5
CP
6
VGG

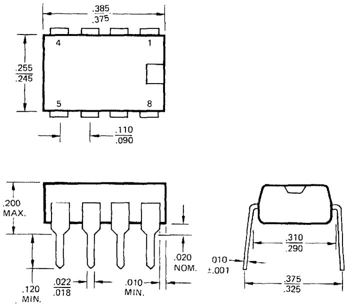
DIE SIZE: 0.101" X 0.142"

## PHYSICAL DIMENSIONS (Top Views)

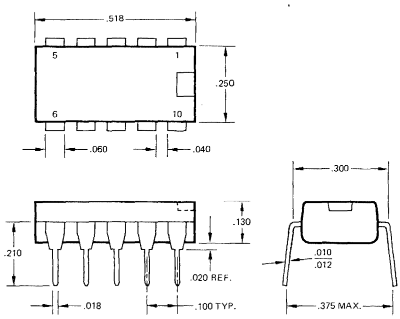
### 8-Pin Side Brazed DIP


.530 MAX.
.010 MIN.
8
5
1
4
.100/.090
.060/.040
.155/.105
.310/.290
.015/.008
.080/.020
.200/.125
.023/.017
.320/.290

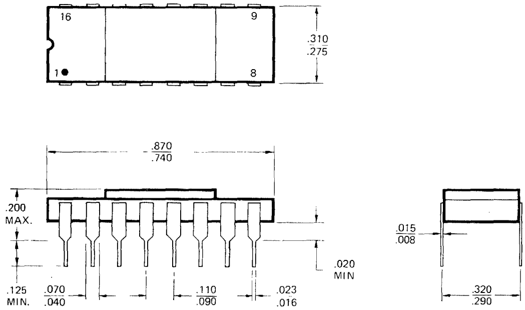
### 8-Pin Molded DIP


.385/.375
4
1
.255/.245
5
8
.110/.090
.200 MAX.
.020 NOM.
.120 MIN.
.022/.018
.010 MIN.
.010 ±.001
.310/.290
.375/.325

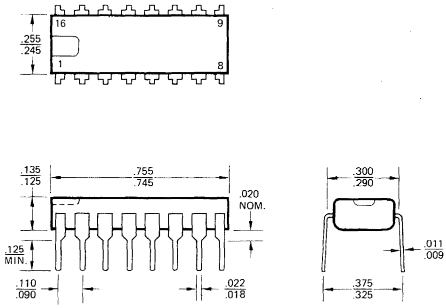
### 10-Pin Molded DIP


.518
5
1
6
10
.250
.060
.040
.300
.130
.210
.010/.012
.020 REF.
.018
.100 TYP.
.375 MAX.

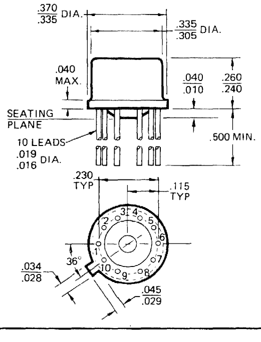
### 16-Pin Side Brazed DIP


16
9
1
8
.310/.275
.870/.740
.200 MAX.
.015/.008
.020 MIN
.125 MIN.
.070/.040
.110/.090
.023/.016
.320/.290

### 16-Pin Molded DIP


16
9
1
8
.255/.245
.135/.125
.755/.745
.020 NOM.
.300/.290
.125 MIN.
.011/.009
.110/.090
.022/.018
.375/.325

### TO-100 Can


.370/.335 DIA.
.335/.305 DIA.
.040 MAX.
.040/.010
.260/.240
SEATING PLANE
10 LEADS
.019/.016 DIA.
.500 MIN.
.230 TYP
.115 TYP
1
2
3
4
5
6
7
8
9
10
36°
.034/.028
.045/.029

# Am4025/5025 • Am4026/5026 • Am4027/5027

## 2048-Bit Dynamic Shift Registers

**Distinctive Characteristics**

- 6 MHz data rate guaranteed
- Single 2048 and dual 1024-bit configurations
- Low power dissipation
- TTL compatible data inputs and outputs
- On chip recirculate and input select controls
- Alternate source to National parts
- Full military temperature range devices available
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

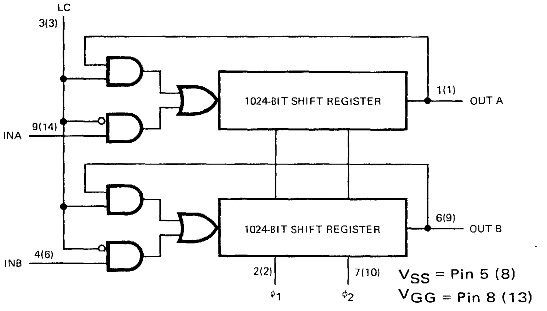
The Am4025/6/7 and Am5025/6/7 are military and commercial grade 2048-bit dynamic shift registers. The Am4025/5025 is a dual 1024-bit device with on-chip recirculate and a load control (LC) common to both registers. When LC is HIGH, the two registers recirculate data; when LC is LOW new data is entered through the data inputs. The Am4026/5026 is similar, but each register has two data inputs, selected by separate input select (IS) signals. The Am4027/5027 is a single 2048-bit register with on-chip recirculate and a load control. All the devices can drive one standard TTL load or three Am93L series low-power TTL loads. The select, load command, and data inputs may be driven by TTL signals. Two high-voltage clock signals, $\phi 1$ and $\phi 2$, are required. Internally, each shift register consists of two multiplexed registers, so that a data shift occurs on each $\phi 1$ or $\phi 2$ clock pulse. The data rate, therefore, is double the frequency of either clock signal.

### ORDERING INFORMATION

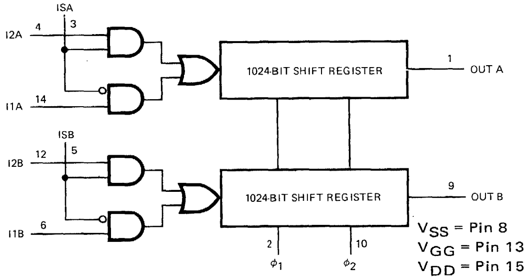
| Package Type | Temperature Range | Order Number |
|---|---|---|
| 10-Pin Molded | 0°C to +70°C | MM5025N |
| 16-Pin Hermetic | 0°C to +70°C | MM5025D |
| 16-Pin Hermetic | –55°C to +125°C | MM4025D |
| 16-Pin Molded | 0°C to +70°C | MM5026N |
| 16-Pin Hermetic | 0°C to +70°C | MM5026DC |
| 16-Pin Hermetic | –55°C to +125°C | MM4026D |
| 8-Pin Molded | 0°C to +70°C | MM5027N |
| 8-Pin Hermetic | 0°C to +70°C | AM5027DC |
| 8-Pin Hermetic | –55°C to +125°C | AM4027DM |

### LOGIC DIAGRAMS

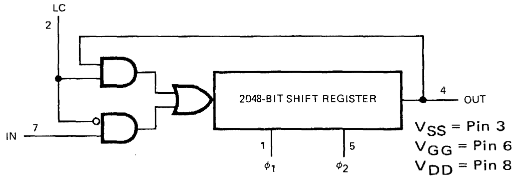
**Am4025/5025**


LC
3(3)
INA 9(14)
INB 4(6)
1024-BIT SHIFT REGISTER
1024-BIT SHIFT REGISTER
1(1) OUT A
6(9) OUT B
2(2) ϕ1
7(10) ϕ2
VSS = Pin 5 (8)
VGG = Pin 8 (13)
VDD = Pin 10 (15)

**Am4026/5026**


ISA 3
I2A 4
I1A 14
ISB 5
I2B 12
I1B 6
1024-BIT SHIFT REGISTER
1024-BIT SHIFT REGISTER
1 OUT A
9 OUT B
2 ϕ1
10 ϕ2
VSS = Pin 8
VGG = Pin 13
VDD = Pin 15

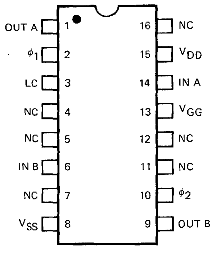
**Am4027/5027**


LC 2
IN 7
2048-BIT SHIFT REGISTER
4 OUT
1 ϕ1
5 ϕ2
VSS = Pin 3
VGG = Pin 6
VDD = Pin 8

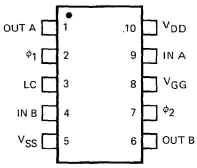
### CONNECTION DIAGRAMS

**Top View**

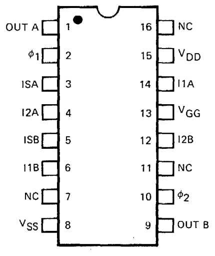
**MM4025D**


OUT A 1
ϕ1 2
LC 3
NC 4
NC 5
IN B 6
NC 7
VSS 8
9 OUT B
10 ϕ2
11 NC
12 NC
13 VGG
14 IN A
15 VDD
16 NC

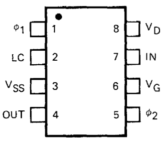
**MM5025N**


OUT A 1
ϕ1 2
LC 3
IN B 4
VSS 5
6 OUT B
7 ϕ2
8 VGG
9 IN A
10 VDD

**MM4026/5026**


OUT A 1
ϕ1 2
ISA 3
I2A 4
ISB 5
I1B 6
NC 7
VSS 8
9 OUT B
10 ϕ2
11 NC
12 I2B
13 VGG
14 I1A
15 VDD
16 NC

**MM4027/5027**


ϕ1 1
LC 2
VSS 3
OUT 4
5 ϕ2
6 VGG
7 IN
8 VDD

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| DC Input Voltage with Respect to $V_{CC}$ | −20V to +0.3V |

## OPERATING RANGE

| Part Number | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ | $T_A$ |
|---|---|---|---|---|
| MM4025/6/7 | +5.0V ±5% | 0 V | −12V ±10% | −55°C to +125°C |
| MM5025/6/7 | +5.0V ±5% | 0 V | −12V ±10% | 0°C to +70°C |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −0.5mA | | 2.4 | | $V_{SS}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | 0.0 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs except clocks | | $V_{SS}$ −1.7 | | $V_{SS}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs except clocks | | $V_{SS}$ −10 | | $V_{SS}$ −4.2 | Volts |
| $I_I$ | Input Leakage Current | $V_{IN}$ = −10V, $T_A$ = 25°C | | | 10 | 500 | nA |
| $I_\phi$ | Clock Input Leakage Current | $V_\phi$ = −15V, $T_A$ = 25°C | | | 50 | 1000 | nA |
| $V_{\phi H}$ | Clock HIGH Level | | | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_{\phi L}$ | Clock LOW Level | | | $V_{SS}$ −18.5 | | $V_{SS}$ −14.5 | Volts |
| $I_{GG}$ | $V_{GG}$ Current | $T_A$ = 25°C | .01MHz<f<0.1MHz | | 2 | 3.5 | mA |
| | | $V_{SS}$=5.0V, $V_{GG}$=−12.0V | f = 1.0MHz | | 2 | 3.5 | |
| | | $V_{\phi L}$ = −12.0V | f = 3.0MHz | | 2 | 3.5 | |
| $I_{DD}$ | $V_{DD}$ Current | t = 115ns | .01MHz<f<0.1MHz | | 8 | 15 | mA |
| | | Data = 11110000. . . | f = 1.0MHz | | 22 | 32 | |
| | | | f = 3.0MHz | | 48 | 70 | |

Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12.0V and 25°C ambient.

## SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS OVER OPERATING RANGE

| Parameters | Definition | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| $f_D$ | Data Rate (Note 2) | $T_A$ = 0°C to +70°C | 0.02 | | 6.0 | MHz |
| | | $T_A$ = −55°C to +125°C | 0.12 | | 2.0 | |
| $f_\phi$ | Clock Frequency (Note 3) | $T_A$ = 0°C to +70°C | .01 | | 3.0 | |
| | | $T_A$ = −55°C to +125°C | 0.06 | | 1.0 | |
| $t_{\phi d}$ | Delay Between Clocks (Note 3) | | 10 | | Note 3 | ns |
| $t_{\phi pw}$ | Clock LOW Time | $t_{\phi t}$ = 20ns | 0.115 | | 10 | μs |
| $t_{\phi t}$ | Clock Rise and Fall Times | 10% to 90% | | | 0.5 | μs |
| $t_s$ | Set-Up Time, Data and Select Inputs (See Definitions) | | | | 35 | ns |
| $t_h$ | Hold Time, Data and Select Inputs (See Definitions) | | | | 20 | ns |
| $t_{\phi p}$ | Period From Start of (Note 3) One Phase to Start of Other Phase | $T_A$ = 0°C to +70°C | 0.165 | | 100 | μs |
| | | $T_A$ = −55°C to +125°C | 0.165 | | 16.5 | |
| $t_{pd}$ | Delay, Clock to Data Out | $C_L$ = 15pF | | | 80 | ns |
| $C_{(D)}$ | Capacitance, Data Input | $V_{IN}$ = 0, f = 1 MHz, All other pins GND (Note 4) | | | 5 | pF |
| $C_{(S)}$ | Capacitance, Select Input or $L_C$ | | | | 7 | pF |
| $C_{(\phi)}$ | Capacitance, Clock Input | $V_\phi$ = 0, f = 1MHz, All other pins GND | | 165 | 190 | |

Notes: 2. The Data Rate is twice the frequency of either clock phase.
3. The maximum delay between clocks ($\phi_1$ and $\phi_2$ both HIGH) is a function of junction temperature. The junction temperature is a function of ambient temperature and clock duty cycle. See curves for minimum frequency on page 3.
4. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

## TRUTH TABLES

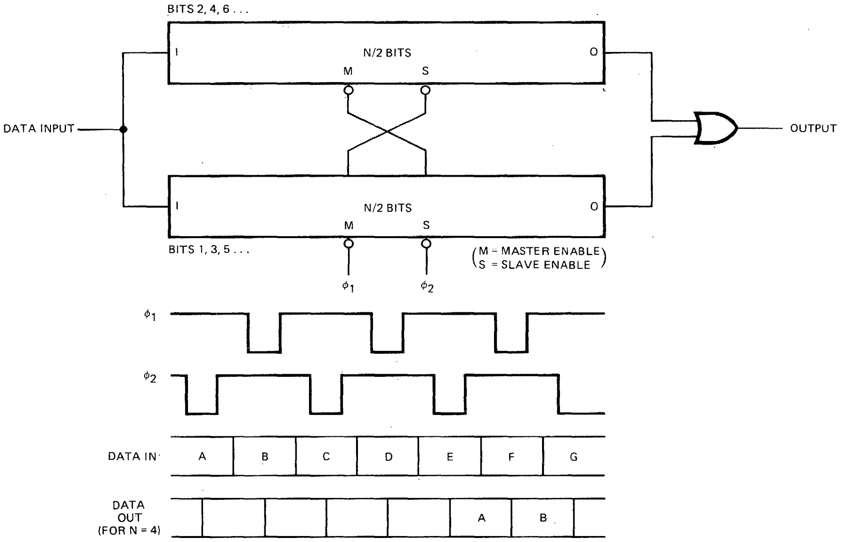
### Am4025/5025 and Am4027/5027

| LC | IN | OUT | DATA ENTERED |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

### Am4026/5026

| IS | INPUT 1 | INPUT 2 | DATA ENTERED |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

## FUNCTIONAL EQUIVALENT OF EACH REGISTER



Since the two registers shift on opposite clock pulses, a new data bit is entered on both $\phi_1$ and $\phi_2$. Data entering the register on $\phi_1$ will appear at the output on $\phi_1$ (from the negative edge of $\phi_1$ to the negative edge of $\phi_2$).

## DEFINITION OF TERMS

**Dynamic Shift Register** A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

**$\phi_1$, $\phi_2$** The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at $V_{SS}$. Data is accepted into the master of each bit during one phase and is transferred to the slave of each bit during the other phase.

**$t_{\phi d}$** Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-toLOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

**$t_{\phi pw}$** Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

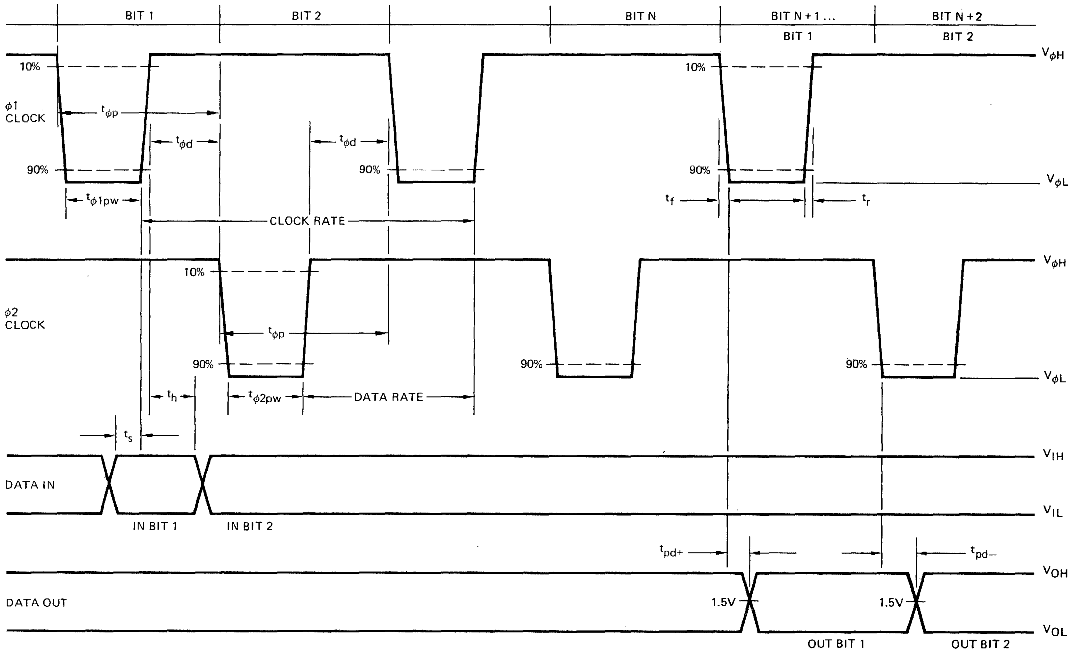
**$t_{\phi t}$** Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

**$t_s(D)$** Data set-up time. The time prior to the LOW-to-HIGH transition of $\phi$ during which the data on the data input must be steady to be correctly written into the memory.

**$t_h(D)$** Data hold time. The time following the LOW-to-HIGH transition of $\phi$ during which the data must be steady. To correctly write data into the register, the data must be applied by $t_s(D)$ before this transition and must not be changed until $t_h(D)$ after this transition.

**$t_{pd}$** The delay from a HIGH-to-LOW clock transition to correct data present at the register output.

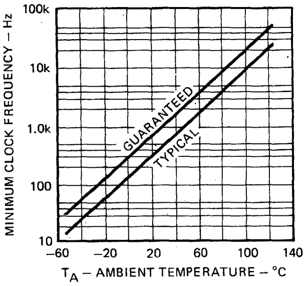
## SWITCHING WAVEFORMS


BIT 1
BIT 2
BIT N
BIT N + 1 ...
BIT 1
BIT N + 2
BIT 2
V$_{\phi H}$
10%
10%
φ1
CLOCK
t$_{\phi p}$
t$_{\phi d}$
t$_{\phi d}$
90%
90%
90%
V$_{\phi L}$
t$_{\phi 1pw}$
t$_f$
t$_r$
CLOCK RATE
V$_{\phi H}$
10%
φ2
CLOCK
t$_{\phi p}$
90%
90%
90%
V$_{\phi L}$
t$_h$
t$_{\phi 2pw}$
DATA RATE
t$_s$
V$_{IH}$
DATA IN
V$_{IL}$
IN BIT 1
IN BIT 2
t$_{pd+}$
t$_{pd-}$
V$_{OH}$
DATA OUT
1.5V
1.5V
V$_{OL}$
OUT BIT 1
OUT BIT 2

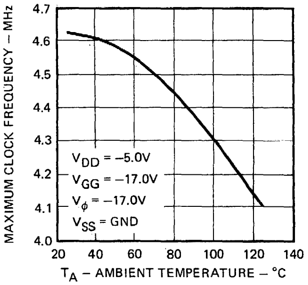
Clock Rise Time 20ns
Clock Fall Time 20ns
Output Load 1 TTL Load

## OPERATING CHARACTERISTICS

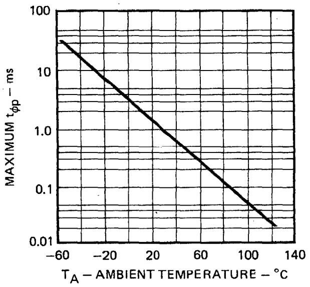
**Guaranteed Minimum Clock Frequency Versus Temperature**



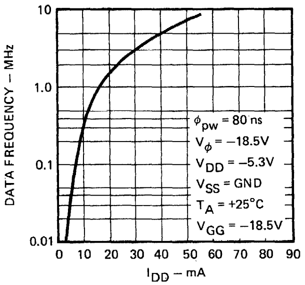
**Maximum Clock Frequency Versus Temperature**



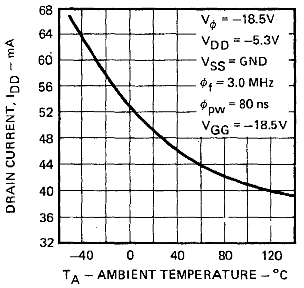
**Guaranteed Maximum $t_{\phi p}$ Versus Temperature (Note 2)**



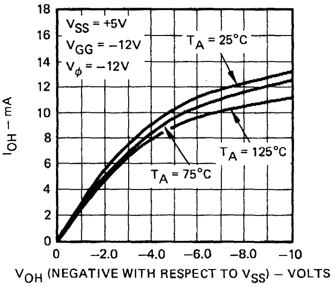
**Typical Power Supply Current Versus Data Rate**



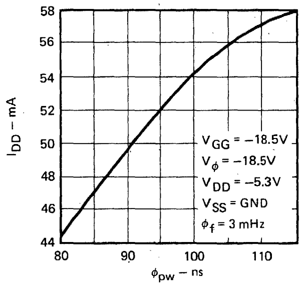
**Typical Power Supply Current Versus Temperature**



**$V_{OH}$ Versus $I_{OH}$**

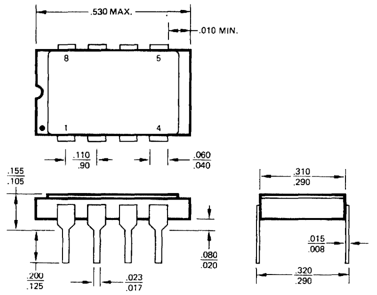


**Typical Power Supply Current Versus Clock Pulse Width $t_{\phi pw}$**

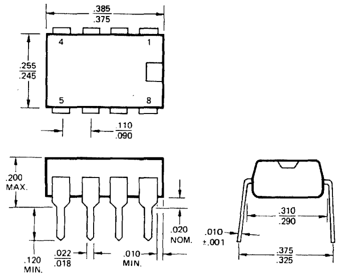


## PHYSICAL DIMENSIONS

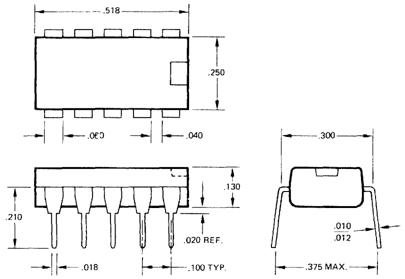
### 8-Pin Side Brazed


.530 MAX.
.010 MIN.
8
5
1
4
.110
.90
.060
.040
.155
.105
.310
.290
.015
.008
.080
.020
.200
.125
.023
.017
.320
.290

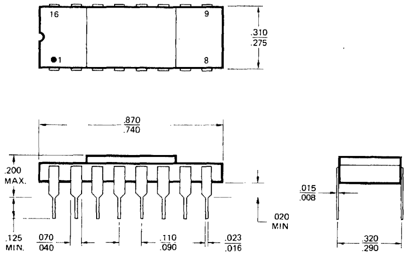
### 8-Pin Molded


.385
.375
4
1
5
8
.255
.245
.110
.090
.200
MAX.
.020
NOM.
.010
±.001
.310
.290
.120
MIN.
.022
.018
.010
MIN.
.375
.325

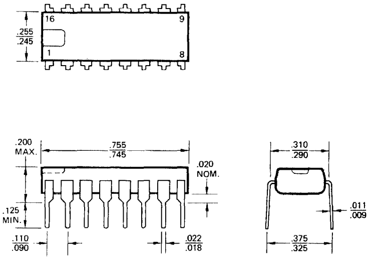
### 10-Pin Molded


.518
.250
.060
.040
.300
.130
.210
.020 REF.
.010
.012
.018
.100 TYP.
.375 MAX.

### 16-Pin Side Brazed

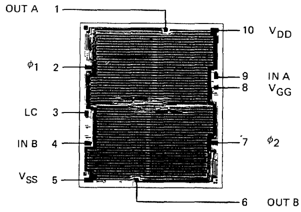

16
9
1
8
.310
.275
.870
.740
.200
MAX.
.015
.008
020
MIN
.125
MIN.
070
040
.110
.090
.023
.016
.320
.290

### 16-Pin Molded


16
9
1
8
.255
.245
.200
MAX.
.755
.745
.020
NOM.
.310
.290
.125
MIN.
.011
.009
.110
.090
.022
.018
.375
.325

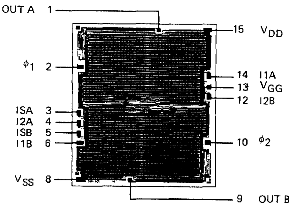
## Metallization and Pad Layouts

### Am4025/5025


OUT A 1
10 $V_{DD}$
$\phi_1$ 2
9 IN A
8 $V_{GG}$
LC 3
IN B 4
7 $\phi_2$
$V_{SS}$ 5
6 OUT B

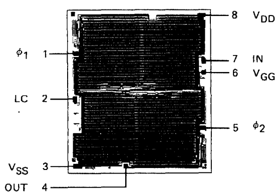
DIE SIZE 0.145" X 0.162"

### Am4026/5026


OUT A 1
15 $V_{DD}$
$\phi_1$ 2
14 I1A
13 $V_{GG}$
12 I2B
ISA 3
I2A 4
ISB 5
I1B 6
10 $\phi_2$
$V_{SS}$ 8
9 OUT B

DIE SIZE 0.145" X 0.162"

### Am4027/5027


8 $V_{DD}$
$\phi_1$ 1
7 IN
6 $V_{GG}$
LC 2
5 $\phi_2$
$V_{SS}$ 3
OUT 4

DIE SIZE 0.145" X 0.162"

# Am4055/5055 • Am4056/5056 • Am4057/5057

## Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

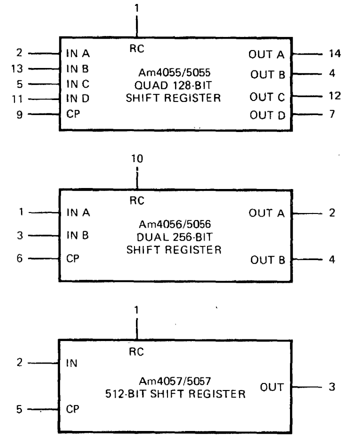
**Distinctive Characteristics**

- Internal recirculate
- Single TTL compatible clock
- Operation guaranteed from DC to 1.5MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

These devices are a family of static P-channel MOS shift registers in three configurations. The Am4055/5055 is a quad 128-bit register; the Am4056/5056 is a dual 256-bit register; and the Am4057/5057 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

### LOGIC SYMBOLS


1
RC
2 IN A
13 IN B
5 IN C
11 IN D
9 CP
Am4055/5055
QUAD 128-BIT
SHIFT REGISTER
OUT A 14
OUT B 4
OUT C 12
OUT D 7
10
RC
1 IN A
3 IN B
6 CP
Am4056/5056
DUAL 256-BIT
SHIFT REGISTER
OUT A 2
OUT B 4
1
RC
2 IN
5 CP
Am4057/5057
512-BIT SHIFT REGISTER
OUT 3

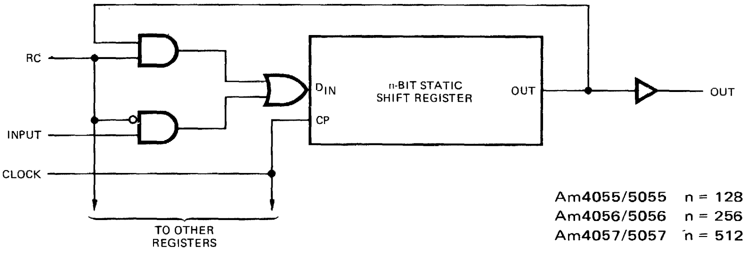
$V_{SS}$ = Pin 8
$V_{DD}$ = Pin 16
$V_{GG}$ = Pin 10

$V_{SS}$ = Pin 5
$V_{DD}$ = Pin 9
$V_{GG}$ = Pin 7

$V_{SS}$ = Pin 4
$V_{DD}$ = Pin 8
$V_{GG}$ = Pin 6

### LOGIC BLOCK DIAGRAM

**(One Register Shown)**


RC
INPUT
CLOCK
$D_{IN}$
CP
n-BIT STATIC
SHIFT REGISTER
OUT
OUT
TO OTHER
REGISTERS

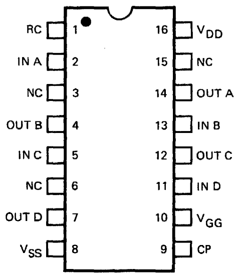
| | |
|---|---|
| Am4055/5055 | n = 128 |
| Am4056/5056 | n = 256 |
| Am4057/5057 | n = 512 |

### ORDERING INFORMATION

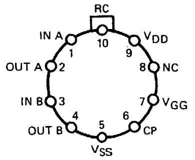
| Package Type | Temperature Range | Order Number |
|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | MM5055N |
| 16-Pin Hermetic DIP | 0°C to +70°C | MM5055D |
| 16-Pin Hermetic DIP | –55°C to +125°C | MM4055D |
| TO-100 Can | 0°C to +70°C | MM5056H |
| TO-100 Can | –55°C to +125°C | MM4056H |
| 8-Pin Molded DIP | 0°C to +70°C | MM5057N |
| 8-Pin Hermetic DIP | 0°C to +70°C | MM5057D |
| 8-Pin Hermetic DIP | –55°C to +125°C | MM4057D |

### CONNECTION DIAGRAMS

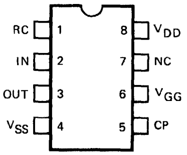
**Am4055/5055**


RC 1
IN A 2
NC 3
OUT B 4
IN C 5
NC 6
OUT D 7
$V_{SS}$ 8
16 $V_{DD}$
15 NC
14 OUT A
13 IN B
12 OUT C
11 IN D
10 $V_{GG}$
9 CP

**Am4056/5056**


RC
10
IN A 1
9 $V_{DD}$
OUT A 2
8 NC
IN B 3
7 $V_{GG}$
OUT B 4
5 $V_{SS}$
6 CP

**Am4057/5057**


RC 1
IN 2
OUT 3
$V_{SS}$ 4
8 $V_{DD}$
7 NC
6 $V_{GG}$
5 CP

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | –65°C to +160°C |
| Temperature (Ambient) Under Bias | –55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ –10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ –20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ –20V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am4055<br>Am4056<br>Am4057 | –55°C to +125°C | 5.0V ±5% | 0V | –12V ±5% |
| Am5055<br>Am5056<br>Am5057 | 0°C to +70°C | 5.0V ±5% | 0V | –12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –0.5mA | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | 4055/6/7 | $V_{SS}$–1.0 | | $V_{SS}$+0.3 | Volts |
| | | | 5055/6/7 | $V_{SS}$–1.5 | | $V_{SS}$+0.3 | |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | $V_{SS}$–18.5 | | $V_{SS}$–4.2 | Volts |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = –10.0V, all other pins GND, $T_A$ = 25°C | | | 0.01 | 0.5 | μA |
| $I_{DD}$ | $V_{DD}$ Power Supply Current | $T_A$ = 25°C, $t_{\phi pw}H$ = 160 ns Data = 1010. . . output open | f ⩽ 2.2MHz | | 15.0 | 20.0 | mA |
| | | | f ⩽ 10KHz | | 13.0 | 18.0 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | | f ⩽ 1.6MHz | | 10.5 | 15.5 | |
| | | | f ⩽ 2.2MHz | | 13.0 | 19.0 | |
| | | | f ⩽ 10KHz | | 6.5 | 9.0 | |

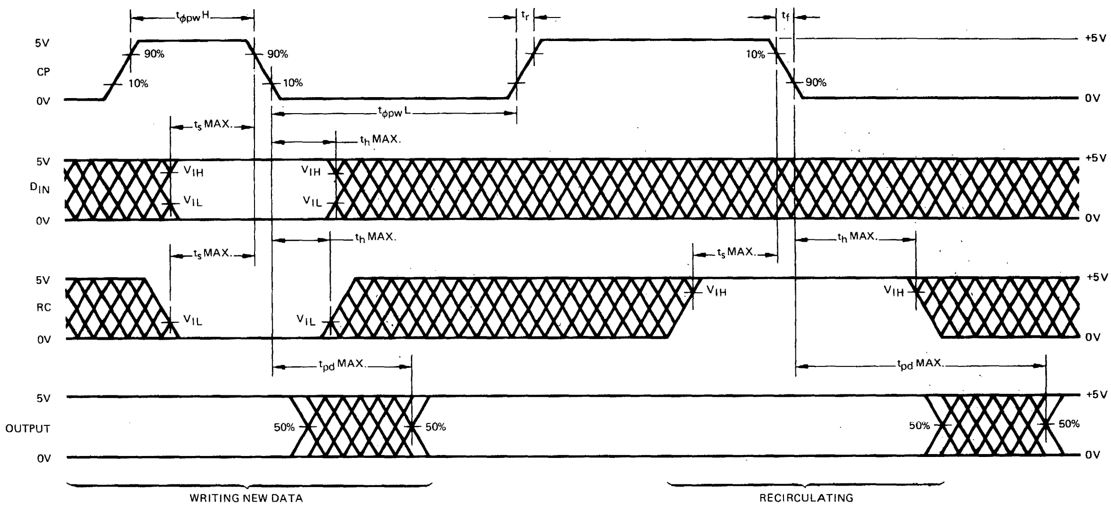
Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = –12V, 25°C ambient.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| | | | Am4055/6/7 | | | Am5055/6/7 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
| f | Clock Frequency | | 0 | | 1.0 | 0 | | 1.5 | MHz |
| $t_{\phi pw}H$ | Clock HIGH Time | | 0.4 | | 1.0 | 0.23 | | 100 | μs |
| $t_{\phi pw}L$ | Clock LOW Time | | 0.4 | | ∞ | 0.3 | | ∞ | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | | 200 | | | 200 | ns |
| $t_s$ | Set-up Time, D or RC Inputs (see definitions) | $t_r = t_f \leqslant$ 10ns | | | 260 | | | 110 | ns |
| $t_h$ | Hold Time, D or RC Inputs (see definitions) | $t_r = t_f \leqslant$ 10ns | | | 120 | | | 40 | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 4k, $C_L$ = 10pF | | 350 | 700 | | 250 | 345 | ns |
| $C_{in}$ | Capacitance, Data and RC Inputs (Note 2) | f = 1MHz, $V_{IN} = V_{SS}$ | | 4 | 7 | | 4 | 7 | pF |
| $C_\phi$ | Capacitance, Clock Input (Note 2) | f = 1MHz, $V_{IN} = V_{SS}$ | | | 14 | | | 14 | pF |

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, $t_{pd}$ min. is always much greater than $t_h$(D) max.

## TIMING DIAGRAM

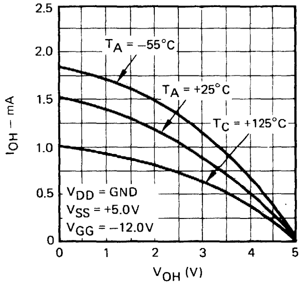


### KEY TO TIMING DIAGRAM

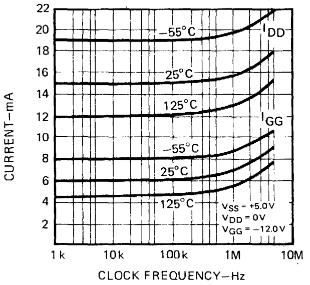
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ═ | MUST BE STEADY | WILL BE STEADY |
| ⧹⧹⧹⧹ | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| //// | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| XXXX | DON'T CARE, ANY CHANGE PERMITTED | CHANGING, STATE UNKNOWN |

## PERFORMANCE CURVES

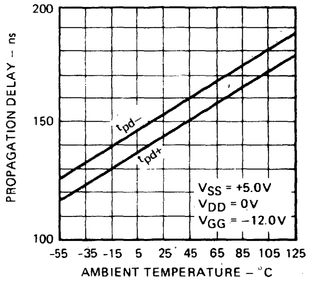
**Typical Data Output HIGH Current Versus Data Output Voltage**



**Typical Power-Supply Currents Versus Frequency**



**Typical Propagation Delay Versus Ambient Temperature**



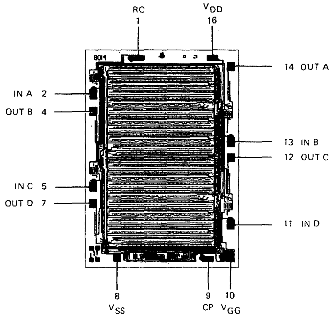
## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

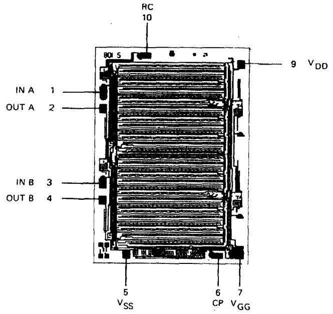
**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

## Metallization and Pad Layouts

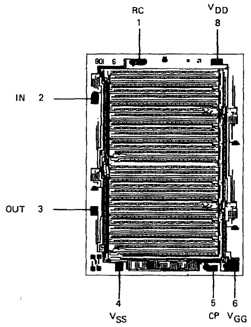
### Am4055/5055


RC 1
VDD 16
14 OUT A
IN A 2
OUT B 4
13 IN B
12 OUT C
IN C 5
OUT D 7
11 IN D
8 VSS
9 CP
10 VGG

### Am4056/5056


RC 10
9 VDD
IN A 1
OUT A 2
IN B 3
OUT B 4
5 VSS
6 CP
7 VGG

### Am4047/5057

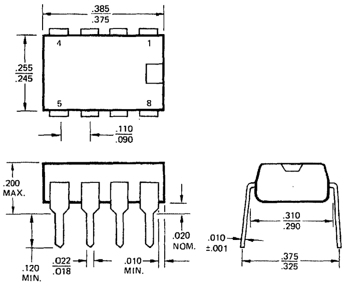

RC 1
VDD 8
IN 2
OUT 3
4 VSS
5 CP
6 VGG

DIE SIZE 0.101" X 0.140"

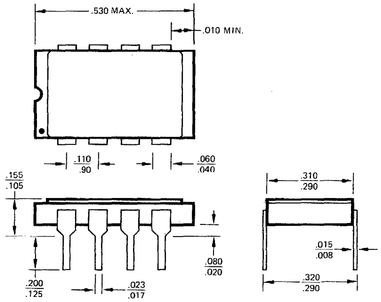
## PHYSICAL DIMENSIONS

Top Views

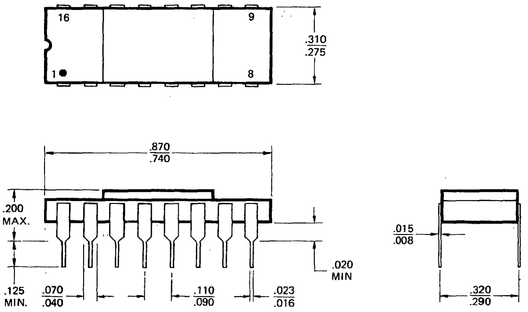
### 8-Pin Molded DIP


.385
.375
4
1
.255
.245
5
8
.110
.090
.200
MAX.
.020
NOM.
.120
MIN.
.022
.018
.010
MIN.
.010
±.001
.310
.290
.375
.325

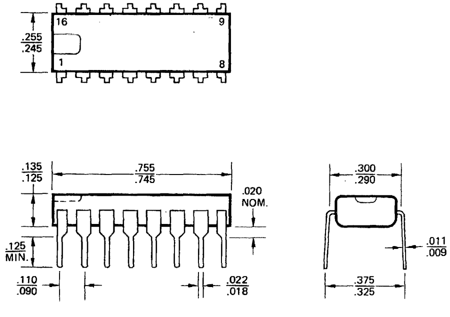
### 8-Pin Hermetic DIP


.530 MAX.
.010 MIN.
.110
.90
.060
.040
.155
.105
.200
.125
.023
.017
.080
.020
.310
.290
.015
.008
.320
.290

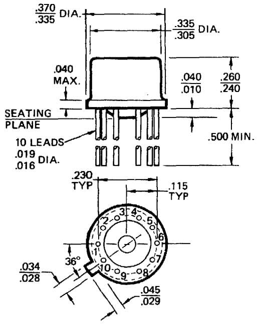
### 16-Pin Side Brazed DIP


16
9
1
8
.310
.275
.870
.740
.200
MAX.
.020
MIN
.125
MIN.
.070
.040
.110
.090
.023
.016
.015
.008
.320
.290

### 16-Pin Molded DIP


16
9
1
8
.255
.245
.135
.125
.755
.745
.020
NOM.
.125
MIN.
.110
.090
.022
.018
.300
.290
.011
.009
.375
.325

### TO-100 Can


.370
.335
DIA.
.335
.305
DIA.
.040
MAX.
.040
.010
.260
.240
SEATING PLANE
10 LEADS
.019
.016
DIA.
.500 MIN.
.230
TYP
.115
TYP
1
2
3
4
5
6
7
8
9
10
36°
.034
.028
.045
.029

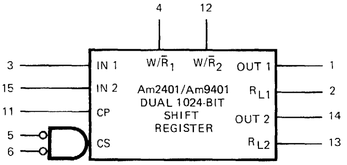
# Am9401/Am2401

## Dual 1024-Bit Dynamic Shift Register

### Distinctive Characteristics

- Single +5V power supply
- High speed – 2MHz min.
- Single phase TTL clock
- Low clock capacitance – 7.0pF max.
- Low Power 315 mW max. @ 2MHz
  40 μW/bit typ. @ 2 MHz
- Chip select, write, and recirculate logic on chip
- 100% reliability assurance testing in accordance with MIL-STD-883

### LOGIC SYMBOL

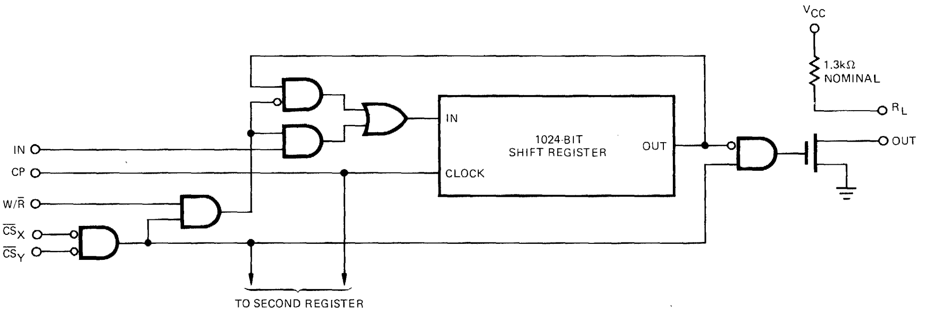

4
12
3
15
11
5
6
IN 1
IN 2
CP
CS
W/$\overline{R}_1$
W/$\overline{R}_2$
Am2401/Am9401
DUAL 1024-BIT
SHIFT
REGISTER
OUT 1
$R_{L1}$
OUT 2
$R_{L2}$
1
2
14
13

$V_{CC}$ = Pin 16
GND = Pin 8

### FUNCTIONAL DESCRIPTION

The Am9401 is a dual 1024-bit dynamic shift register built using ion-implanted, N-channel, silicon gate MOS technology. The device operates from a single +5 volt power supply and all inputs and outputs, including the clock, are directly TTL compatible. Data is entered into the register on the LOW-to-HIGH transition of the clock input. New data appears on the output following the HIGH-to-LOW clock transition. There are two chip select inputs, $\overline{CS}_X$ and $\overline{CS}_Y$; if either is HIGH then the data in both registers recirculates and the outputs go to a HIGH impedance OFF state. If both chip selects are LOW, then the outputs will be LOW for LOW data and OFF for HIGH data (similar to TTL open collectors). When the chip is selected, the write-recirculate lines control the entry of new data. If W/$\overline{R}$ is HIGH new data is written into the corresponding register; if W/$\overline{R}$ is LOW, the data on the output is recirculated. An internal pull-up resistor to $V_{CC}$ is provided at $R_L$. This point may be connected to the output to establish the HIGH logic level. Many register outputs may be connected together with the $R_L$ connected only once. The Am9401 is a high performance plug-in replacement for the Am2401.

### LOGIC BLOCK DIAGRAM


$V_{CC}$
1.3kΩ
NOMINAL
$R_L$
OUT
IN
CP
W/$\overline{R}$
$\overline{CS}_X$
$\overline{CS}_Y$
IN
1024-BIT
SHIFT REGISTER
OUT
CLOCK
TO SECOND REGISTER

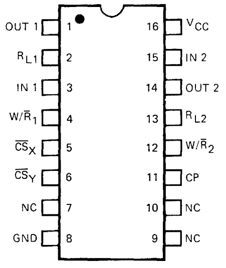
Note: Only one register shown.

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number | Order Number |
|---|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | AM9401PC | P2401 |
| 16-Pin Hermetic DIP | 0°C to +70°C | AM9401DC | C2401 |
| 16-Pin Hermetic DIP | –55°C to +125°C | AM9401DM | |

### CONNECTION DIAGRAM

#### Top View


OUT 1
1
$R_{L1}$
2
IN 1
3
W/$\overline{R}_1$
4
$\overline{CS}_X$
5
$\overline{CS}_Y$
6
NC
7
GND
8
16
$V_{CC}$
15
IN 2
14
OUT 2
13
$R_{L2}$
12
W/$\overline{R}_2$
11
CP
10
NC
9
NC

Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Power Dissipation | 1W |
| Voltage on Any Pin | −0.5V to +7.0V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Am9401, 2401PC, DC | 0°C to +70°C | 5.0V ± 5% |
| Am9401DM | −55°C to +125°C | 5.0V ± 5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Conditions | | Am2401 Min. | Am2401 Typ. (Note 1) | Am2401 Max. | Am9401 Min. | Am9401 Typ. | Am9401 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 5.25V | | | | 10 | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 5.25V | | | | 100 | | | 100 | µA |
| $I_{CC}$ | $V_{CC}$ Current | $V_{CC}$ = MAX.<br>80% Duty Cycle | $T_A$ = 25°C | | | 70 | | | 50 | mA |
| | | | $T_A$ = 0°C to +70°C | | | 80 | | | 60 | |
| | | | $T_A$ = −55°C to +125°C | | | | | 50 | 80 | |
| $V_{IH}$ | Input HIGH Level | | | 2.2 | | | 2.2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | | −0.3 | | 0.65 | −0.3 | | 0.65 | Volts |
| $I_{OL}$ | Output LOW Current | $V_{OL}$ = 0.45V | | 6.3 | 10 | | 6.3 | | | mA |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA, $R_L$ connected | | | | 0.45 | | | 0.45 | Volts |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −1mA, $R_L$ connected | | 2.4 | | $V_{CC}$ | 2.4 | | $V_{CC}$ | Volts |
| $R_L$ | Internal Load Resistor | | | 0.8 | 1.3 | 2.2 | 0.8 | | 2.2 | kΩ |

Note: 1. Typical values are at 25°C and $V_{CC}$ = 5.0V.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

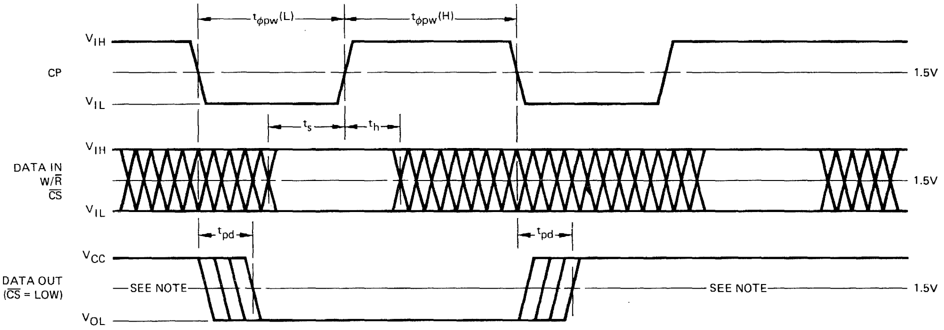
| Parameters | Description | Conditions | Am2401 Min. | Am2401 Typ. (Note 1) | Am2401 Max. | Am9401 Min. | Am9401 Typ. | Am9401 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Data and Clock Rate | | | | 1.0 | | | 2.0 | MHz |
| $f_{min}$ | Minimum Data and Clock Rate | $T_A$ = 25°C | 1.0 | | | 1.0 | | | kHz |
| | | $T_A$ = 0°C to +70°C | 25 | | | 25 | | | |
| | | $T_A$ = −55°C to +125°C | | | | 100 | | | |
| $t_{\phi pw}(L)$ | Clock LOW Time | $T_A$ = 0°C to +70°C | 0.8 | | 10 | 0.4 | | 10 | µs |
| | | $T_A$ = −55°C to +125°C | | | | | | 9 | |
| $t_{\phi pw}(H)$ | Clock HIGH Time | $T_A$ = 25°C | 0.2 | | 1000 | 0.1 | | 1000 | µs |
| | | $T_A$ = 0°C to +70°C | 0.2 | | 40 | 0.1 | | 40 | |
| | | $T_A$ = −55°C to +125°C | | | | 0.1 | | 1.0 | |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | | 50 | | | 50 | ns |
| $t_s$ | Data and Control Set-Up Time | | 200 | | | 80 | | | ns |
| $t_h$ | Data and Control Hold Time | | 150 | | | 150 | | | ns |
| $t_{pd}$ | Delay, Clock or Chip Select to Output | $R_L$ connected (Note 2)<br>$C_L$ = 100pF, Load = 1 TTL gate | | 250 | 500 | | 160 | 320<br>Note 2 | ns |

Note: 2. $C_L$ = 20pF for Am9401. The capacitive load is limited primarily by the internal load register.

## CAPACITANCE ($T_A$ = 25°C)

| Parameters | Description | Conditions | Am2401 Min. | Am2401 Typ. | Am2401 Max. | Am9401 Min. | Am9401 Typ. | Am9401 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Capacitance, All Data Inputs | f = 1 MHz, $V_{IN}$ = 250 mV<br>All Pins at $R_L$ Ground | | 4.0 | 7.0 | | 4.0 | 7.0 | pF |
| $C_{\phi}$ | Capacitance, Clock Input | | | 4.0 | 7.0 | | 4.0 | 7.0 | pF |
| $C_{OUT}$ | Capacitance, Data Output | | | 10 | 14 | | 5.0 | 10 | pF |

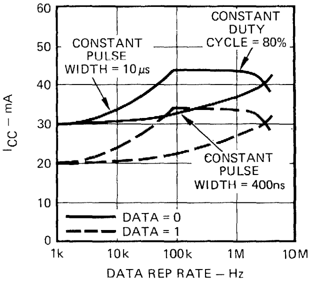
## SWITCHING WAVEFORMS


$t_{\phi pw}(L)$
$t_{\phi pw}(H)$
$V_{IH}$
CP
$V_{IL}$
1.5V
$t_s$
$t_h$
DATA IN
W/$\overline{R}$
$\overline{CS}$
$t_{pd}$
$V_{CC}$
DATA OUT
($\overline{CS}$ = LOW)
SEE NOTE
$V_{OL}$

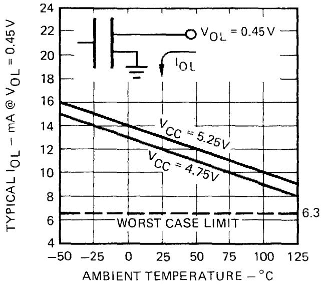
Note: HIGH level on output is established by externally connected load resistor.

## TYPICAL PERFORMANCE CHARACTERISTICS

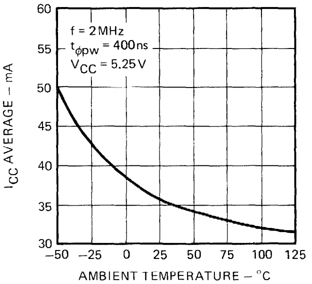
### Power Supply Current ($I_{CC}$) Versus Data Rep. Rate



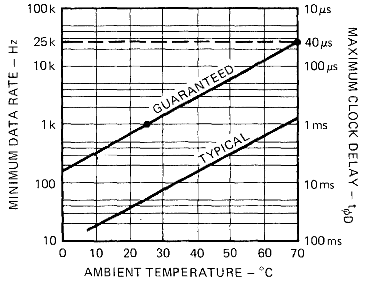
### Temperature Dependence of Output LOW Level Sink Capability



### Power Supply Current ($I_{CC}$) Versus Ambient Temperature (0°C)



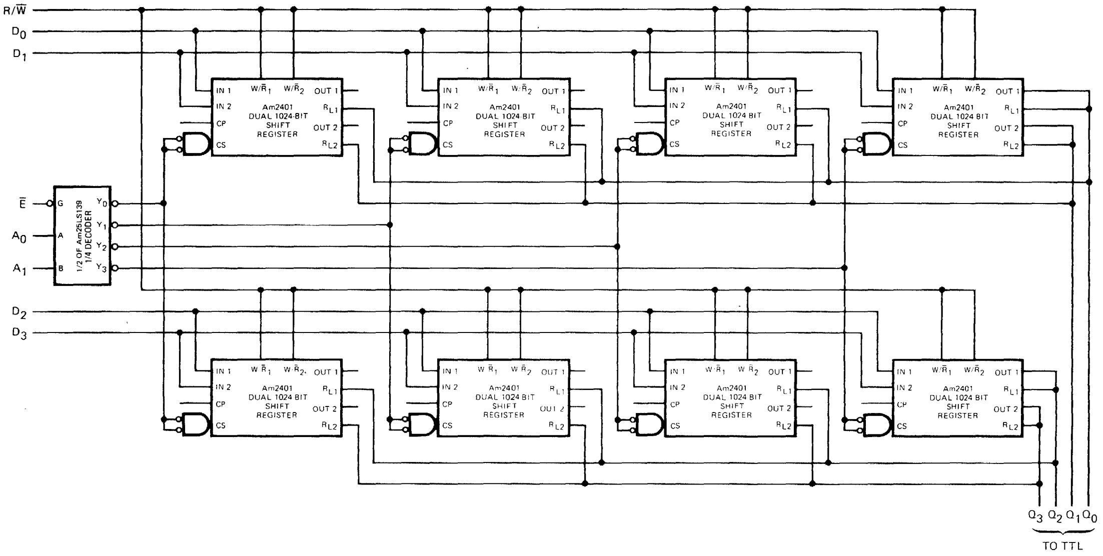
### Minimum Data Rate and Maximum Clock Delay Versus Ambient Temperature



## TRUTH TABLE

| W/$\overline{R}$ | $\overline{CS}_X$ | $\overline{CS}_Y$ | $D_{IN}$ | DATA ENTERED | OUTPUT | OPERATION |
|---|---|---|---|---|---|---|
| X | X | H | X | $D_{IN}$ (t-1024) | OFF | Deselected, Recirculate |
| X | H | X | X | $D_{IN}$ (t-1024) | OFF | Deselected, Recirculate |
| H | L | L | L | LOW | $D_{IN}$ (t-1024) | Read, Write |
| H | L | L | H | HIGH | $D_{IN}$ (t-1024) | Read, Write |
| L | L | L | X | $D_{IN}$ (t-1024) | $D_{IN}$ (t-1024) | Read, Recirculate |

## APPLICATIONS


R/W̄
D0
D1
Ē
A0
A1
D2
D3
G
A
B
Y0
Y1
Y2
Y3
1/2 OF Am25LS139
1/4 DECODER
IN 1
W/R̄1
W/R̄2
OUT 1
IN 2
Am2401
DUAL 1024 BIT
SHIFT
REGISTER
RL1
CP
OUT 2
CS
RL2
Q3 Q2 Q1 Q0
TO TTL

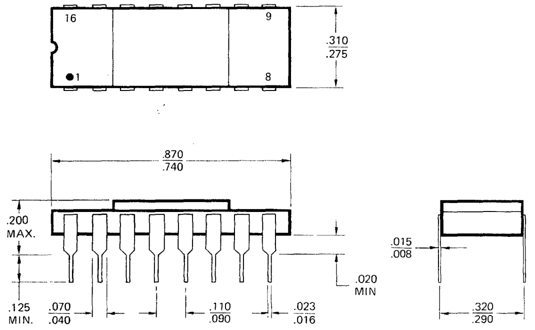
### 4k x 4 REGISTER ARRAY

Eight Am2401's form this 16k register array. Data inputs ($D_0$-$D_3$) and data outputs ($Q_0$-$Q_3$) may be connected directly to TTL. Note that the load resistors are only connected once to each line. A pair of devices (a 1k x 4 section) is selected by address bits $A_0$ and $A_1$. The data in the selected devices are read out and, if R/W̄ is LOW, updated with new data. All clock lines are driven from TTL levels.

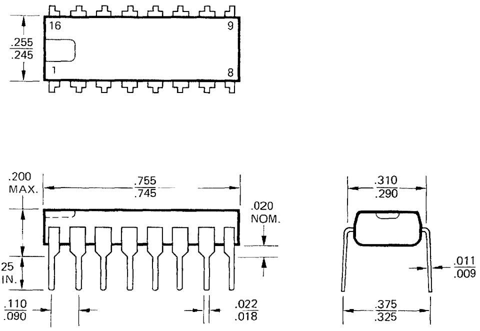
## PHYSICAL DIMENSIONS

### Dual-In-Line

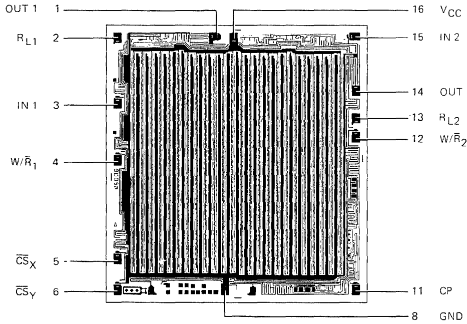
**16-Pin Side Brazed**


16
9
1
8
.310
.275
.870
.740
.200
MAX.
.125
MIN.
.070
.040
.110
.090
.023
.016
.020
MIN
.015
.008
.320
.290

**16-Pin Molded**


16
9
1
8
.255
.245
.200
MAX.
.755
.745
.020
NOM.
.125
MIN.
.110
.090
.022
.018
.310
.290
.011
.009
.375
.325

## Metallization and Pad Layout


OUT 1 1
RL1 2
IN 1 3
W/R̄1 4
C̄S̄X 5
C̄S̄Y 6
16 VCC
15 IN 2
14 OUT 2
13 RL2
12 W/R̄2
11 CP
8 GND

DIE SIZE
0.133" X 0.142"

# First-In First-Out Memories

## NUMERICAL INDEX

| | | Page |
|---|---|---|
| Am2812/2812A | 32 x 8-Bit | 6-3 |
| Am2813/2813A | 32 x 9-Bit | 6-3 |
| Am3341/2841/2841A | 64 x 4-Bit | 6-9 |

## SELECTION GUIDE

| Part Number | Organization | Serial I/O | Fullness Flag | Output Enable | Package Pins | Data Rate MHz | Temp. Range |
|---|---|---|---|---|---|---|---|
| Am2812 | 32 Words x 8-Bits | Yes | Yes | Yes | 28 | 0.5 | C, M |
| Am2812A | 32 Words x 8-Bits | Yes | Yes | Yes | 28 | 1.0 | C |
| Am2813 | 32 Words x 9-Bits | No | Yes | Yes | 28 | 0.5 | C, M |
| Am2813A | 32 Words x 9-Bits | No | Yes | Yes | 28 | 1.0 | C, M |
| Am2841 | 64 Words x 4-Bits | No | No | No | 16 | 1.0 | C, M |
| Am2841A | 64 Words x 4-Bits | No | No | No | 16 | 1.2 | C |

# Am2812 / Am2812A • Am2813 / Am2813A

## 32x8 and 32x9 First–In First–Out Memories

### Distinctive Characteristics

- Completely independent read and write operations
- "Half-full" flag
- Am2812 has serial or parallel input and output
- Data rates up to 1 MHz

## FUNCTIONAL DESCRIPTION

The Am2812 and Am2813 are 32 word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three-state outputs controlled by an output enable pin (OE). Data on the data inputs ($D_i$) are written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word. Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs ($Q_i$) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready (IR) signal indicates that the device is ready to accept data and also provides a memory full signal. Both the Am2812 and Am2813 have master reset inputs which clear all data from the device (reset to all LOWs), and a FLAG signal which goes HIGH when the memory contains more than 15 words.

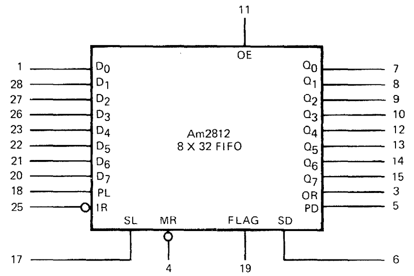
The Am2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is in reality an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the $D_0$ input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built-in parallel-to-serial converter, so that data can be shifted out of the $Q_7$ output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals, PL, IR, PD, and OR, are designed so that two FIFOs can be placed end to end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

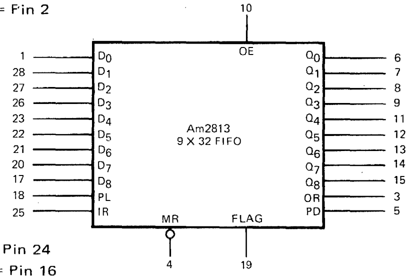
## ORDERING INFORMATION

| Package Type | Frequency | Temperature Range | Am2812 Order Number | Am2813 Order Number |
|---|---|---|---|---|
| Hermetic DIP | 500KHz | 0°C to +70°C | AM2812DC | AM2813DC |
| Hermetic DIP | 500KHz | −55°C to +125°C | AM2812DM | AM2813DM |
| Hermetic DIP | 1MHz | 0°C to +70°C | AM2812ADC | AM2813ADC |
| Hermetic DIP | 1MHz | −55°C to +125°C | AM2812ADM | AM2813ADM |

## LOGIC SYMBOLS


11
OE
Am2812
8 X 32 FIFO
1 D0
28 D1
27 D2
26 D3
23 D4
22 D5
21 D6
20 D7
18 PL
25 IR
Q0 7
Q1 8
Q2 9
Q3 10
Q4 12
Q5 13
Q6 14
Q7 15
OR 3
PD 5
SL 17
MR 4
FLAG 19
SD 6

$V_{SS}$ = Pin 24
$V_{DD}$ = Pin 16
$V_{GG}$ = Pin 2

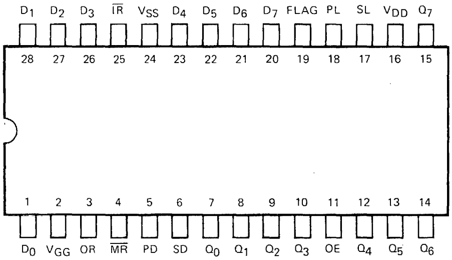

10
OE
Am2813
9 X 32 FIFO
1 D0
28 D1
27 D2
26 D3
23 D4
22 D5
21 D6
20 D7
17 D8
18 PL
25 IR
Q0 6
Q1 7
Q2 8
Q3 9
Q4 11
Q5 12
Q6 13
Q7 14
Q8 15
OR 3
PD 5
MR 4
FLAG 19

$V_{SS}$ = Pin 24
$V_{DD}$ = Pin 16
$V_{GG}$ = Pin 2

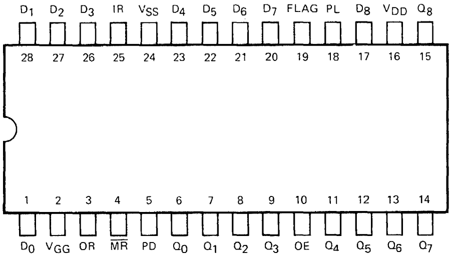
## CONNECTION DIAGRAMS

### Top Views

### Am2812


D1 D2 D3 IR VSS D4 D5 D6 D7 FLAG PL SL VDD Q7
28 27 26 25 24 23 22 21 20 19 18 17 16 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14
D0 VGG OR MR PD SD Q0 Q1 Q2 Q3 OE Q4 Q5 Q6

### Am2813


D1 D2 D3 IR VSS D4 D5 D6 D7 FLAG PL D8 VDD Q8
28 27 26 25 24 23 22 21 20 19 18 17 16 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14
D0 VGG OR MR PD Q0 Q1 Q2 Q3 OE Q4 Q5 Q6 Q7

Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −7 V to $V_{SS}$ +0.3 V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20 V to $V_{SS}$ +0.3 V |
| DC Input Voltage | $V_{SS}$ −10 V to $V_{SS}$ +0.3 V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am2812DC, Am2812ADC<br>Am2813DC, Am2813ADC | 0°C to +70°C | 5.0V ±5% | 0V | −12V ±5% |
| Am2812DM, Am2812ADM<br>Am2813DM, Am2813ADM | −55°C to +125°C | 5.0V ±5% | 0V | −12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = .300mA | $V_{SS}$ −1.0 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Level | | $V_{SS}$ −1.0 | | | V |
| $V_{IL}$ | Input LOW Level | | | | 0.8 | V |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = 0V (Note 2) | | | 1.0 | μA |
| $I_{IH}$ (Note 2) | Input HIGH Current | $V_{IN}$ = $V_{SS}$ −1.0V (Note 2) | | | 250 | μA |
| $V_{PUP}$ | Input Pull-up Initiation Voltage | (Note 2) $V_{SS}$ = MIN. | | | 2.0 | V |
| | | $V_{SS}$ = MAX. | | | 2.2 | V |
| $V_{BAR}$ | Voltage at Peak Input Current | (Note 2) | | | $V_{SS}$ −1.5 | V |
| $I_{BAR}$ | Maximum Input Current | (Note 2) | | | 1.6 | mA |
| $I_{GG}$ | $V_{GG}$ Current | $T_A$ = 0°C to +70°C | | 14 | 22 | mA |
| | | $T_A$ = −55°C to +125°C | | | 27 | |
| $I_{DD}$ | $V_{DD}$ Current | $T_A$ = 0°C to +70°C | | 30 | 45 | mA |
| | | $T_A$ = −55°C to +125°C | | | 55 | |

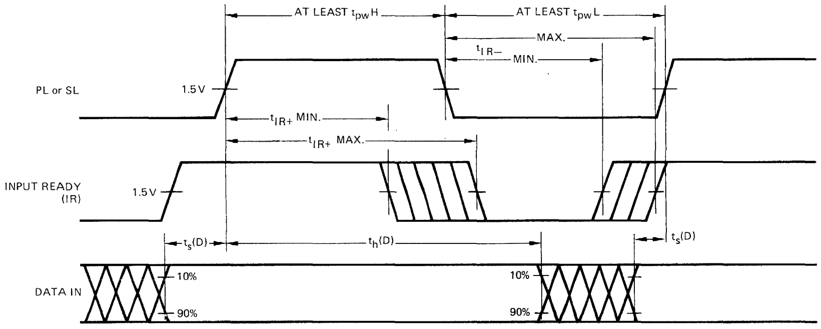
Notes: 1. Typical limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12.0V, $T_A$ = 25°C
2. Pull up circuit on Am2813 only. See graph of input V-I characteristics.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

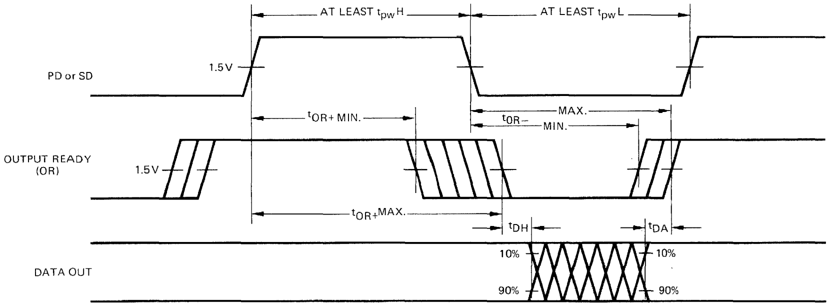
| Parameters | Conditions/Note | Test Conditions | Am2812<br>Am2813<br>Min. | Typ. | Max. | Am2812A<br>Am2813A<br>Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_p$ | Maximum Parallel Load or Dump Frequency | | 0.5 | | | 1.0 | | | MHz |
| $t_{IR+}$ | Delay, PL or SL HIGH to IR In-Active | | 100 | 300 | 1100 | 80 | 300 | 450 | ns |
| $t_{IR-}$ | Delay, PL or SL LOW to IR Active | | 100 | 250 | 800 | 80 | 250 | 400 | ns |
| $t_{pw}H(P)$ | Minimum PL or PD HIGH Time | | | | 100 | | | 80 | ns |
| $t_{pw}L(P)$ | Minimum PL or PD LOW Time | | | | 100 | | | 80 | ns |
| $t_{pw}H(S)$ | Minimum SL or SD HIGH Time | Am2812 only | | | 350 | | | 300 | ns |
| $t_{pw}L(S)$ | Minimum SL or SD LOW Time | Am2812 only | | | 350 | | | 300 | ns |
| $t_h(D)$ | Data Hold Time | | | 190 | 250 | | 170 | 200 | ns |
| $t_s(D)$ | Data Set-Up Time | to PL | | | 0 | | | 0 | ns |
| | | to SL | | | 100 | | | 90 | |
| $t_{OR+}$ | Delay, PD or SD HIGH to OR LOW | OE HIGH | 100 | 450 | 1100 | 100 | 350 | 520 | ns |
| $t_{OR-}$ | Delay, PD or SD LOW to OR HIGH | OE HIGH | 100 | 400 | 850 | 100 | 300 | 470 | ns |
| $t_{PT}$ | Ripple through Time | FIFO Empty | | | 10 | | | 8 | μs |
| $t_{DH}$ | Delay, OR LOW to Data Out Changing | PD = LOW | 50 | 200 | | 50 | 200 | | ns |
| $t_{DA}$ | Delay, Data Out to OR HIGH | PD = HIGH | 0 | 100 | | 0 | 100 | | ns |
| $t_{MRW}$ | Minimum Reset Pulse Width | | | | 600 | | | 500 | ns |
| $t_{DO}$ | Delay, OE LOW to Output OFF | | | | 600 | | | 500 | ns |
| $t_{EO}$ | Delay, OE HIGH to Output Active | | | | 600 | | | 500 | ns |
| $t_{DF}$ | Delay from PL or SL HIGH to Flag HIGH or PD or SD HIGH to Flag LOW | | | 0.5 | 1.0 | | 0.5 | 1.0 | μs |
| CI | Input Capacitance | | | | 7 | | | 7 | pF |

Notes: 3. IR is active HIGH on Am2813 and active LOW on Am2812.
4. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

## TIMING DIAGRAM



Note: IR inverted on Am2812.



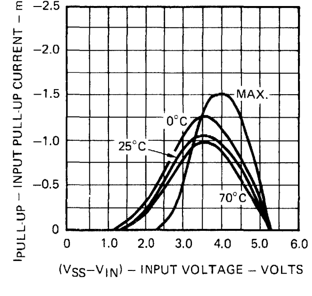
### USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on PD, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If PD is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least $t_{OR+}$) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. $\overline{IR}$ goes HIGH and OR goes LOW. If PL is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and $\overline{IR}$ will return to the LOW state until PL is brought LOW. If PL is LOW when the master reset is ended, then $\overline{IR}$ will go HIGH but the data on the inputs will not enter the memory until PL goes HIGH.
5. The output enable pin inhibits dump commands while it is LOW and forces the Q outputs to a high impedance state.
6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.
7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

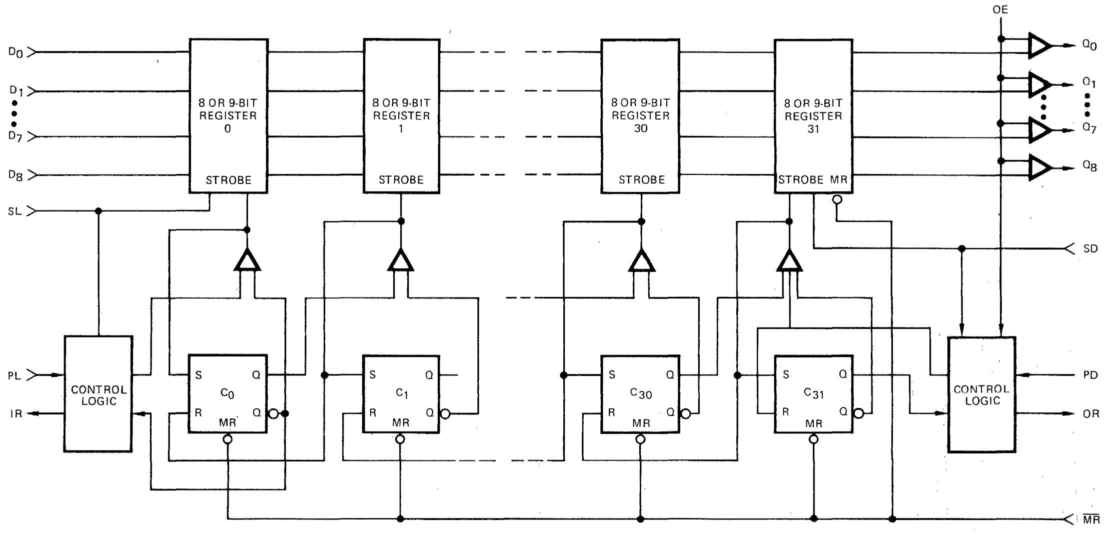
### KEY TO TIMING DIAGRAM

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ═══ | MUST BE STEADY | WILL BE STEADY |
| \\\\\\ | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| //// | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| XXXX | DON'T CARE: ANY CHANGE PERMITTED | CHANGING: STATE UNKNOWN |

**Pull-up Characteristic Input Current Versus Input Voltage**



## LOGIC BLOCK DIAGRAM



## DESCRIPTION OF THE Am2812 and Am2813 FIFO OPERATION

The Am2812 and Am2813 FIFOs consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the $n^{th}$ bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the $n^{th}$ data register, simultaneously setting the (n+1)th control register bit and clearing the $n^{th}$ control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a LOW-to-HIGH transition on the parallel load (PL) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When PL next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go active, indicating the inputs are available for another data word.

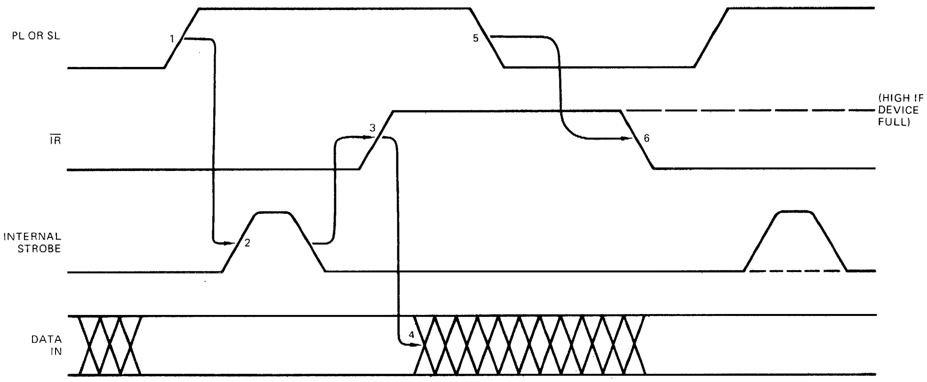
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A LOW-to-HIGH transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes HIGH, OR will go LOW as before, but when PD next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes LOW, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

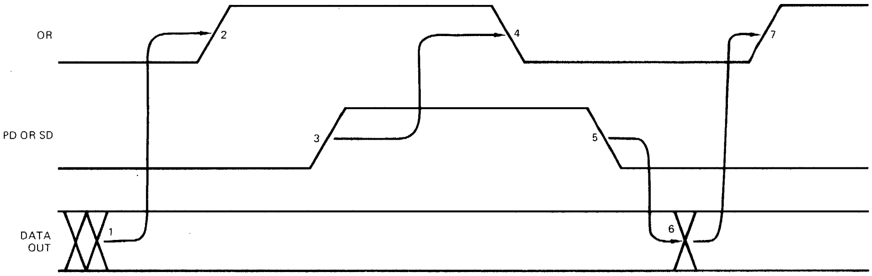
Because the input ready signal is active LOW on the Am2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two Am2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n Am2812s connected end-to-end store 31n+1 words (instead of 32n). The Am2813 stores 32n words in this configuration, because IR is active HIGH and does dump the last word written into the second device.

## Am2812 TIMING DIAGRAM



### Am2812 INPUT TIMING

When data is steady PL is brought HIGH (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes HIGH (3) and data may be changed (4). $\overline{IR}$ remains HIGH until PL is brought LOW (5); then $\overline{IR}$ goes LOW (6) indicating new data may be entered.



### Am2812 OUTPUT TIMING

When data out is steady (1), OR goes HIGH (2). When PD goes HIGH (3), OR goes LOW (4). When PD goes LOW again (5), the output data changes (6) and OR returns HIGH (7).

The input and output timing diagrams above illustrate the sequence of control on the Am2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The Am2813 pattern is similiar, but IR is active HIGH instead of active LOW (shown in timing diagram on next page).

### FLAG OUTPUT

A flag output is available on the Am2812 and Am2813 to indicate whether the FIFO is more or less than half full. The flag signal is generated by summing the "1s" in the control flip-flops, and therefore is not affected by the movement of data through the register. The flag signal goes HIGH when the 13th, 14th, 15th, or 16th word is loaded into the FIFO. It will remain HIGH until there are less than 15+1/–2 words in the memory. It is always HIGH if there are more than 16 words in the FIFO.

### RESET

An over-riding master reset ($\overline{MR}$) is used to clear all control register bits and set all the outputs LOW.

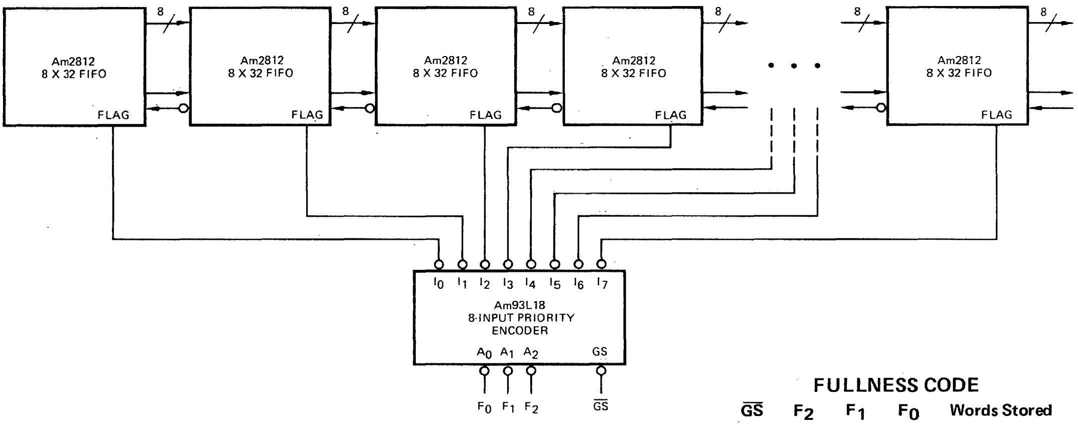
### SERIAL INPUT AND OUTPUT (Am2812 ONLY)

The Am2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to $D_0$ input. Inputs $D_1$–$D_7$ must be grounded. The SL signal operates just like the PL input, causing IR to go HIGH and LOW as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they had been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the $O_7$ output. OR moves HIGH and LOW with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and a new 8-bit word is brought to the output. OR will stay LOW if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.

## APPLICATIONS


Am2812
8 X 32 FIFO
FLAG
8
Am93L18
8-INPUT PRIORITY
ENCODER
$I_0$ $I_1$ $I_2$ $I_3$ $I_4$ $I_5$ $I_6$ $I_7$
$A_0$ $A_1$ $A_2$
GS
$F_0$ $F_1$ $F_2$
$\overline{GS}$

### FULLNESS CODE

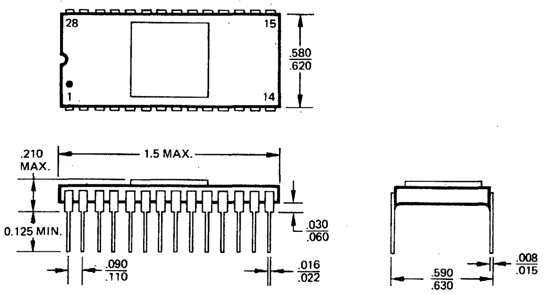
| $\overline{GS}$ | $F_2$ | $F_1$ | $F_0$ | Words Stored |
|---|---|---|---|---|
| L | L | L | L | 0 - 15 |
| L | L | L | H | 13 - 47 |
| L | L | H | L | 45 - 78 |
| L | L | H | H | 76 - 109 |
| L | H | L | L | 107 - 140 |
| L | H | L | H | 138 - 171 |
| L | H | H | L | 169 - 202 |
| L | H | H | H | 200 - 233 |
| H | H | H | H | 231 - 249 |

The Fullness Flags from Am2812 or Am2813 FIFOs can be encoded by an Am93L18 8-input priority encoder. The output code $F_0$–$F_2$ indicates the weight of the highest priority input which is LOW. GS is group signal; it is HIGH if all the inputs are HIGH.

## PHYSICAL DIMENSIONS

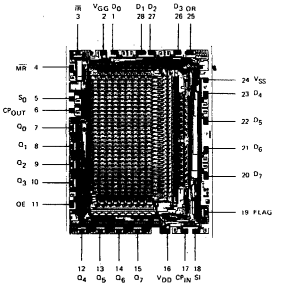
### Dual-In-Line

### 28-Pin Side Brazed

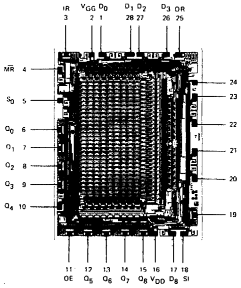

28
15
1
14
.580
.620
.210
MAX.
1.5 MAX.
0.125 MIN.
.030
.060
.090
.110
.016
.022
.590
.630
.008
.015

### Metallization and Pad Layouts

Am2812


$\overline{IR}$ 3
$V_{GG}$ 2
$D_0$ 1
$D_1$ 28
$D_2$ 27
$D_3$ 26
OR 25
$\overline{MR}$ 4
$S_0$ 5
$CP_{OUT}$ 6
$Q_0$ 7
$Q_1$ 8
$Q_2$ 9
$Q_3$ 10
OE 11
24 $V_{SS}$
23 $D_4$
22 $D_5$
21 $D_6$
20 $D_7$
19 FLAG
12 $Q_4$
13 $Q_5$
14 $Q_6$
15 $Q_7$
16 $V_{DD}$
17 $CP_{IN}$
18 SI

Am2813


IR 3
$V_{GG}$ 2
$D_0$ 1
$D_1$ 28
$D_2$ 27
$D_3$ 26
OR 25
$\overline{MR}$ 4
$S_0$ 5
$Q_0$ 6
$Q_1$ 7
$Q_2$ 8
$Q_3$ 9
$Q_4$ 10
24 $V_{SS}$
23 $D_4$
22 $D_5$
21 $D_6$
20 $D_7$
19 FLAG
11 OE
12 $Q_5$
13 $Q_6$
14 $Q_7$
15 $Q_8$
16 $V_{DD}$
17 $D_8$
18 SI

DIE SIZE .128" X 0.168"

# Am2841/3341/2841A

## 64 x 4 First-In First-Out Memories

### Distinctive Characteristics

- Plug-In replacement for Fairchild 3341
- Asynchronous buffer for up to 64 four-bit words
- Easily expandable to larger buffers
- Am2841 has 1 MHz guaranteed data rate
- Am2841A has 1.2MHz guaranteed data rate
- 100% reliability assurance testing in compliance with MIL-STD-883
- Special input circuit provides true TTL compatibility

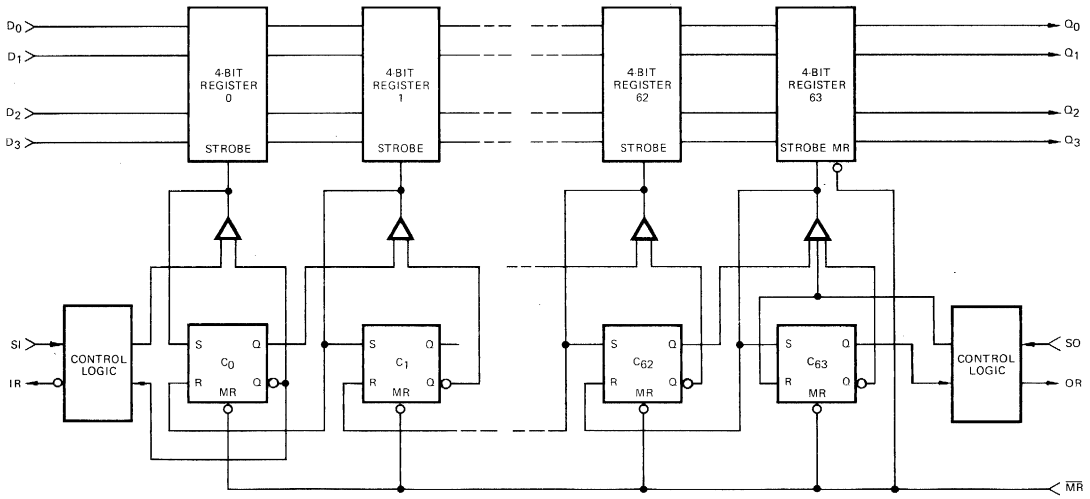
### FUNCTIONAL DESCRIPTION

The Am3341/Am2841/Am2841A is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four-bit parallel word $D_0$—$D_3$ under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs $Q_0$—$Q_3$. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written. A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFOs to obtain deeper stacks.

Parallel expansion to wider words only requires that rows of FIFOs be placed side by side.

Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates. Special input circuits are provided on all inputs to pull the input signals up to an MOS $V_{IH}$ when a TTL $V_{OH}$ is reached, providing true TTL compatibility without the inconvenience and extra power drain of external pull-up resistors. A detailed description of the operation is on pages 4 and 5 of this data sheet. The Am2841 and Am2841A are functionally identical to the Am3341, but are higher performance devices.

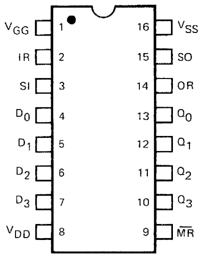
### LOGIC BLOCK DIAGRAM



### ORDERING INFORMATION

| Package Type | Temperature Range | Am3341 Order Number | Am2841 Order Number | Am2841A Order Number |
|---|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM3341PC | AM2841PC | AM2841APC |
| Hermetic DIP | 0°C to +70°C | AM3341DC | AM2841DC | AM2841ADC |
| Hermetic DIP | -55°C to +125°C | | AM2841DM | |

### CONNECTION DIAGRAM
### Top View



Note: Pin 1 is marked for orientation.

## MAXIMUM RATING (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −7V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part No. | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am3341PC, DC<br>Am2841PC, DC<br>Am2841APC, DC | 0°C to +70°C | +5.0 ±5% | GND | −12.0 ±5% |
| Am2841DM | −55°C to +125°C | +5.0 ±5% | GND | −12.0 ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = .300mA | | $V_{SS}$ −1.0 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | | | $V_{SS}$ −1.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | | | | | 0.8 | Volts |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = 0V | | | | 1.0 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{SS}$ −1.0V | | | | 250 | μA |
| $V_{PUP}$ | Input Pull-up Initiation Voltage | (Note 2) | $V_{SS}$ = MIN. | | | 2.0 | Volts |
| | | | $V_{SS}$ = MAX. | | | 2.2 | Volts |
| $V_{BAR}$ | Voltage at Peak Input Current | (Note 2) | | | | $V_{SS}$ −1.5 | Volts |
| $I_{BAR}$ | Maximum Input Current | (Note 2) | | | | 1.6 | mA |
| $I_{GG}$ | $V_{GG}$ Current | $T_A$ = 0°C to +70°C | | | 7 | 12 | mA |
| | | $T_A$ = −55°C to +125°C | | | | 16 | |
| $I_{DD}$ | $V_{DD}$ Current | $T_A$ = 0°C to +70°C | | | 30 | 45 | mA |
| | | $T_A$ = −55°C to +125°C | | | | 60 | |

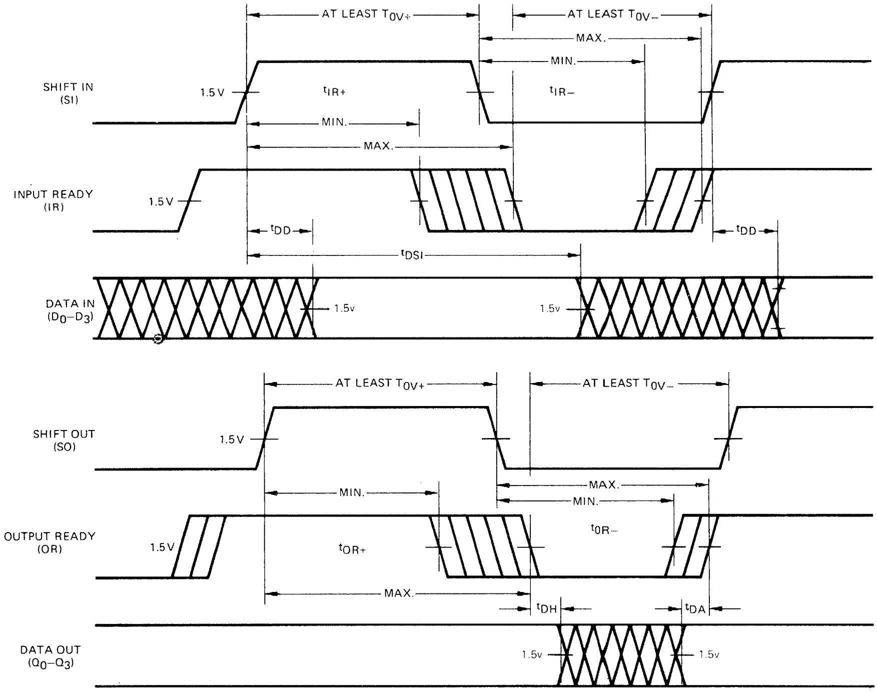
Notes: 1. Typical limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12.0V, $T_A$ = 25°C
2. See graph of input V-I characteristics.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| | | | Am3341 | | | Am2841 | | | Am2841A | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameters | Definition | Test Conditions | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
| $f_{max}$ | Maximum SI or SO Frequency | | 0.75 | | | 1.0 | | | 1.2 | | | MHz |
| $t_{IR+}$ | Delay, SI HIGH to IR LOW | | 90 | 250 | 550 | 80 | | 400 | 80 | | 350 | ns |
| $t_{IR-}$ | Delay, SI LOW to IR HIGH | | 138 | 275 | 550 | 100 | | 550 | 100 | | 450 | ns |
| $t_{OV+}$ | Minimum Time SI and IR both HIGH | | 100 | | | | | 80 | | | 80 | ns |
| $t_{OV-}$ | Minimum Time SI and IR both LOW | | 100 | | | | | 80 | | | 80 | ns |
| $t_{DSI}$ | Data Release Time | | 400 | | | | | 200 | | | 200 | ns |
| $t_{DD}$ | Data Set-up Time | | 25 | | | 0 | | | 0 | | | ns |
| $t_{OR+}$ | Delay, SO HIGH to OR LOW | | 90 | 250 | 500 | 70 | 200 | 450 | 80 | 200 | 370 | ns |
| $t_{OR-}$ | Delay, SO LOW to OR HIGH | | 170 | 350 | 850 | 70 | 200 | 550 | 70 | 200 | 450 | ns |
| $t_{PT}$ | Ripple through Time | FIFO Empty | | 10 | 32 | | 8 | 16 | | 8 | 16 | μs |
| $t_{DH}$ | Delay, OR LOW to Data Out | SO = LOW | 75 | | | 75 | | | 75 | | | ns |
| $t_{MRW}$ | Minimum Reset Pulse Width | | | | 400 | | | 400 | | | 400 | ns |
| $t_{DA}$ | Delay, Data Out to OR HIGH | SO = HIGH | 0 | 30 | | 0 | 20 | | 0 | 20 | | ns |
| CI | Input Capacitance (Except $\overline{MR}$) | | | | 7 | | | 7 | | | 7 | pF |
| $C_{MR}$ | Input Capacitance $\overline{MR}$ | | | | 15 | | | 7 | | | 7 | pF |

Note: Switching times over the entire temperature range are such that two devices at approximately the same ambient temperature can drive each other.

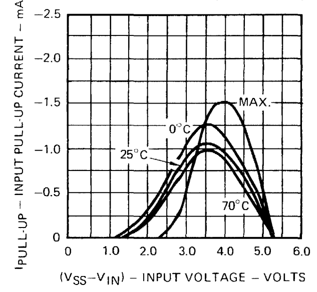
## TIMING DIAGRAM


AT LEAST $T_{OV+}$
AT LEAST $T_{OV-}$
MAX.
MIN.
SHIFT IN (SI)
1.5V
$t_{IR+}$
$t_{IR-}$
MIN.
MAX.
INPUT READY (IR)
1.5V
$t_{DD}$
$t_{DSI}$
$t_{DD}$
DATA IN ($D_0$–$D_3$)
1.5v
1.5v
AT LEAST $T_{OV+}$
AT LEAST $T_{OV-}$
SHIFT OUT (SO)
1.5V
MAX.
MIN.
MIN.
OUTPUT READY (OR)
1.5V
$t_{OR+}$
$t_{OR-}$
MAX.
$t_{DH}$
$t_{DA}$
DATA OUT ($Q_0$–$Q_3$)
1.5v
1.5v

### USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least $t_{OR+}$) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.

**Pull-up Characteristic Input Current Versus Input Voltage**



## DESCRIPTION OF THE Am3341 FIFO OPERATION

The Am3341 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the $n^{th}$ bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the $n^{th}$ data register, simultaneously setting the (n+1)th control register bit and clearing the $n^{th}$ control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs $D_0$–$D_3$ by applying a LOW-to-HIGH transition on the shift in (SI) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes LOW indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When SI next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go HIGH, indicating the inputs are available for another data word.

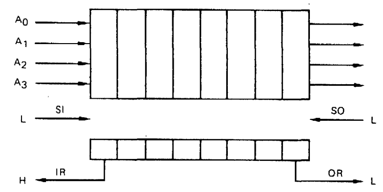
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the four data outputs $Q_0$–$Q_3$. An input signal, shift out (SO), is used to shift the data out of the FIFO. A LOW-to-HIGH transition on SO clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When SO goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes HIGH, OR will go LOW as before, but when SO next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when SI goes LOW, and IR will remain LOW instead of returning to a HIGH state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

An over-riding master reset ($\overline{\text{MR}}$) is used to reset all control register bits and remove the data from the output (i.e. reset the outputs to all LOW).

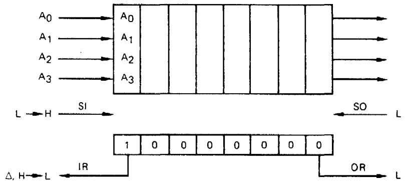
1


A0
A1
A2
A3
L SI
SO L
H IR
OR L

**INITIAL CONDITION**

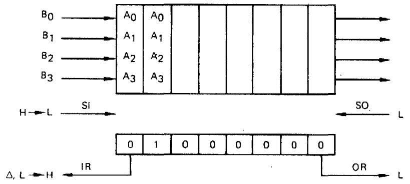
FIFO empty, SI LOW IR HIGH, word "A" on inputs.

2


A0 A1 A2 A3
A0 A1 A2 A3
L→H SI
SO L
1 0 0 0 0 0 0 0
Δ, H→L IR
OR L

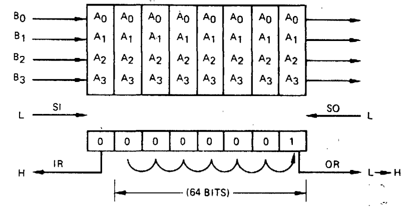
Write input into first stage by raising SI. (Δ = delay) IR goes LOW indicating data has been entered.

3


B0 B1 B2 B3
A0 A0
A1 A1
A2 A2
A3 A3
H→L SI
SO L
0 1 0 0 0 0 0 0
Δ, L→H IR
OR L

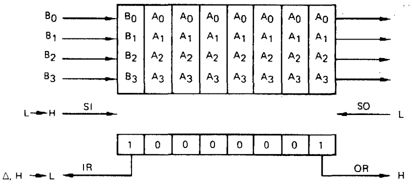
Release data into FIFO by lowering SI. After delay, data moves to second location, and IR goes HIGH indicating input available for new data word.

4


B0 B1 B2 B3
A0 A0 A0 A0 A0 A0 A0 A0
A1 A1 A1 A1 A1 A1 A1 A1
A2 A2 A2 A2 A2 A2 A2 A2
A3 A3 A3 A3 A3 A3 A3 A3
L SI
SO L
0 0 0 0 0 0 0 1
H IR
OR L→H
(64 BITS)

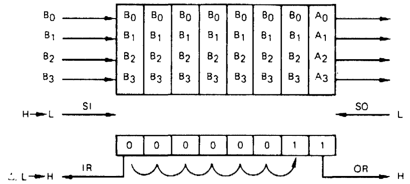
Data spontaneously ripple through registers to end of FIFO, causing OR to go HIGH. The time required for data to fall completely through the FIFO is the "Ripple-through Time".

5


B0 B1 B2 B3
B0 A0 A0 A0 A0 A0 A0 A0
B1 A1 A1 A1 A1 A1 A1 A1
B2 A2 A2 A2 A2 A2 A2 A2
B3 A3 A3 A3 A3 A3 A3 A3
L→H SI
SO L
1 0 0 0 0 0 0 1
Δ, H→L IR
OR H

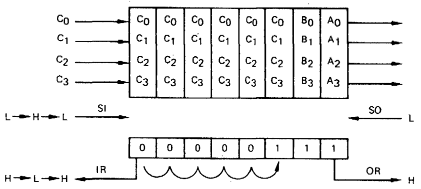
Word "B" written into FIFO

6


B0 B1 B2 B3
B0 B0 B0 B0 B0 B0 B0 A0
B1 B1 B1 B1 B1 B1 B1 A1
B2 B2 B2 B2 B2 B2 B2 A2
B3 B3 B3 B3 B3 B3 B3 A3
H→L SI
SO L
0 0 0 0 0 0 1 1
Δ, L→H IR
OR H

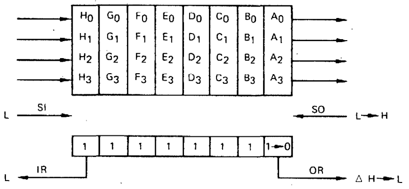
SI goes LOW allowing word "B" to fall through.

7


C0 C1 C2 C3
C0 C0 C0 C0 C0 C0 B0 A0
C1 C1 C1 C1 C1 C1 B1 A1
C2 C2 C2 C2 C2 C2 B2 A2
C3 C3 C3 C3 C3 C3 B3 A3
L→H→L SI
SO L
0 0 0 0 0 1 1 1
H→L→H IR
OR H

Word "C" written in same manner, and so on. When buffer is full, all control bits are 1's and IR stays LOW.

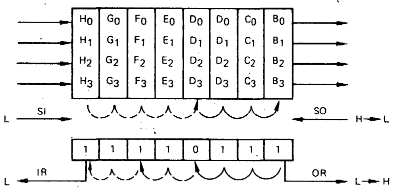
8


H0 G0 F0 E0 D0 C0 B0 A0
H1 G1 F1 E1 D1 C1 B1 A1
H2 G2 F2 E2 D2 C2 B2 A2
H3 G3 F3 E3 D3 C3 B3 A3
L SI
SO L→H
1 1 1 1 1 1 1 1→0
L IR
OR Δ H→L

**FIRST READ OPERATION**

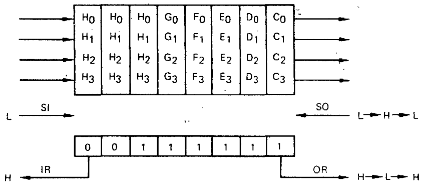
SO goes HIGH, indicating "Ready to Read". OR then goes LOW indicating "Data Read".

9


H0 G0 F0 E0 D0 D0 C0 B0
H1 G1 F1 E1 D1 D1 C1 B1
H2 G2 F2 E2 D2 D2 C2 B2
H3 G3 F3 E3 D3 D3 C3 B3
L SI
SO H→L
1 1 1 1 0 1 1 1
L IR
OR L→H

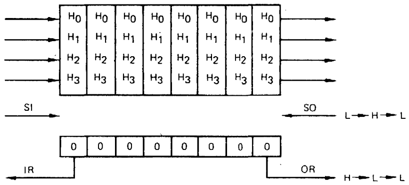
When SO goes LOW, the "0" in the last control bit bubbles toward the memory input. OR goes HIGH as the new word arrives at the output. IR goes HIGH when "0" reaches input.

10


H0 H0 H0 G0 F0 E0 D0 C0
H1 H1 H1 G1 F1 E1 D1 C1
H2 H2 H2 G2 F2 E2 D2 C2
H3 H3 H3 G3 F3 E3 D3 C3
L SI
SO L→H→L
0 0 1 1 1 1 1 1
H IR
OR H→L→H

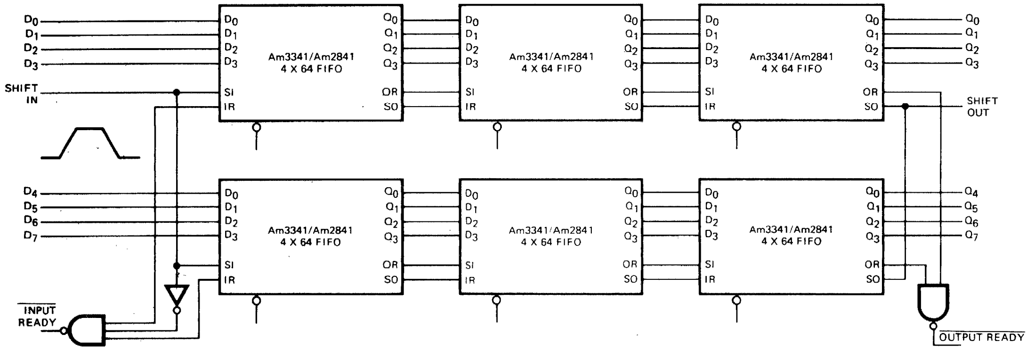
Read word "B" out, word "C" moves to output, and so on.

11


H0 H0 H0 H0 H0 H0 H0 H0
H1 H1 H1 H1 H1 H1 H1 H1
H2 H2 H2 H2 H2 H2 H2 H2
H3 H3 H3 H3 H3 H3 H3 H3
SI
SO L→H→L
0 0 0 0 0 0 0 0
IR
OR H→L→L

Read word "H". OR stays LOW because FIFO is empty. Word "H" remains in output until new word falls through.

## APPLICATION


D0
D1
D2
D3
SHIFT IN
D4
D5
D6
D7
INPUT READY
Am3341/Am2841
4 X 64 FIFO
D0
D1
D2
D3
SI
IR
Q0
Q1
Q2
Q3
OR
SO
Q0
Q1
Q2
Q3
SHIFT OUT
Q4
Q5
Q6
Q7
OUTPUT READY

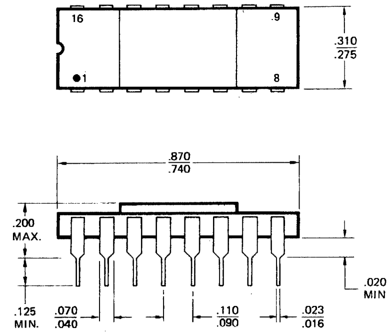
The composite input ready indicates both devices are ready to receive data. The shift in pulse must be wide enough for all devices to load data under worst case conditions.

8 X 192 FIFO Buffer Using Am3341/Am2841

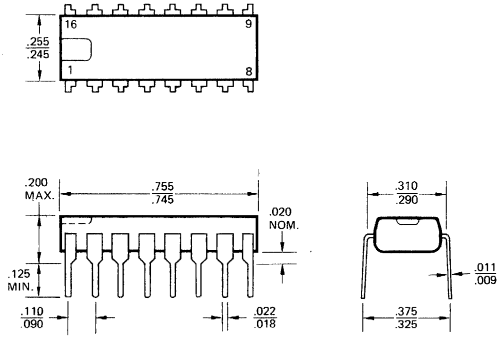
## PHYSICAL DIMENSIONS

### Dual-In-Line

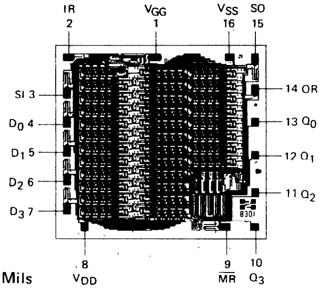
**16-Pin Side Brazed**


16
9
1
8
.310
.275
.870
.740
.200
MAX.
.125
MIN.
.070
.040
.110
.090
.023
.016
.020
MIN
.015
.008
.320
.290

**16-Pin Molded**


16
9
1
8
.255
.245
.200
MAX.
.755
.745
.020
NOM.
.125
MIN.
.110
.090
.022
.018
.310
.290
.011
.009
.375
.325

### Metallization and Pad Layout


IR
2
VGG
1
VSS
16
SO
15
SI 3
D0 4
D1 5
D2 6
D3 7
14 OR
13 Q0
12 Q1
11 Q2
8
VDD
9
MR
10
Q3
8301

126 x 138 Mils

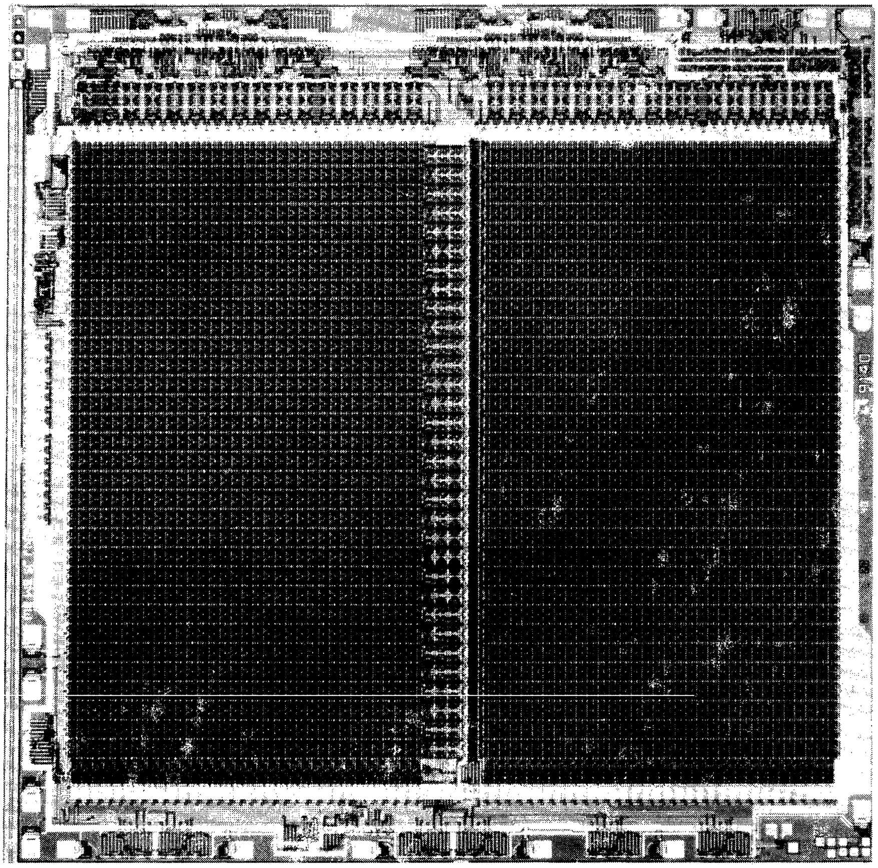
# Application Notes

# Am9130/Am9140

## DESIGNING WITH SELF-CLOCKING, ADAPTIVE 4K STATIC R/W RANDOM ACCESS MEMORIES

APRIL 1976

By Joseph H. Kroeger



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## GENERAL CHARACTERISTICS

### Introduction

The Am9130 and Am9140 products from Advanced Micro Devices are 4K-bit, static, self-clocking, adaptive, read/write random access memories. Both types of devices use only a single +5 volt power supply, yet offer high speed performance and low power dissipations. Figure 1 lists the appropriate part numbers for the combinations of variables available at press time. As product enhancement proceeds, it is anticipated that higher speed parts and wider ranges of low-power and military temperature parts will be available. Plastic DIP packages will also become an option. The latest factory data sheets show all available variations of parts.

The Am9130 is organized as 1024 words by 4 bits per word; the Am9140 is organized as 4096 words by 1 bit per word. Parts are available in both commercial and military temperature ranges. Although the standard power parts offer quite low per-bit power dissipation, there is also a family of low-power parts available. As usual at AMD, all parts are 100% reliability assurance tested to the requirements of MIL-STD-883.

Figure 2 shows the pin assignments for the two memories. The package for both parts is a standard 22-pin dual in-line. Both memory configurations are manufactured from the same basic chip and use only specialized metal interconnect layers to define the structural differences. This approach allows several manufacturing efficiencies to be realized and permits each part to benefit from the combined volume of both parts.

The Am9130 and Am9140 memories are implemented with AMD's LINOX N-channel silicon gate MOS technology. The processing and design rules are exactly the same as those used for some time to produce the popular Am9102 line of 1K static R/W memories. LINOX features physically flat structures, triple ion-implantation, and low capacitance, high-speed devices. The new 4K memories are very dense with more than 27,500 active transistors in an area of less than 37,800 mil$^2$. The chip measures 192 x 197 mils with 58% of the area devoted to the 4096 storage cells.

| ORGANIZATION | AMBIENT TEMPERATURE | POWER | ACCESS TIME | | | |
|---|---|---|---|---|---|---|
| | | | 500ns | 400ns | 300ns | 200ns |
| 1024 x 4 | $0^\circ C \leq T_A \leq 70^\circ C$ | STANDARD | AM9130ADC | AM9130BDC | AM9130CDC | AM9130EDC |
| | | LOW | AM91L30ADC | AM91L30BDC | AM91L30CDC | |
| | $-55^\circ C \leq T_A \leq 125^\circ C$ | STANDARD | AM9130ADM | AM9130BDM | AM9130CDM | |
| | | LOW | AM91L30ADM | AM91L30BDM | | |
| 4096 x 1 | $0^\circ C \leq T_A \leq 70^\circ C$ | STANDARD | AM9140ADC | AM9140BDC | AM9140CDC | AM9140EDC |
| | | LOW | AM91L40ADC | AM91L40BDC | AM91L40CDC | |
| | $-55^\circ C \leq T_A \leq +125^\circ C$ | STANDARD | AM9140ADM | AM9140BDM | AM9140CDM | |
| | | LOW | AM91L40ADM | AM91L40BDM | | |

Figure 1. Part Number Matrix.

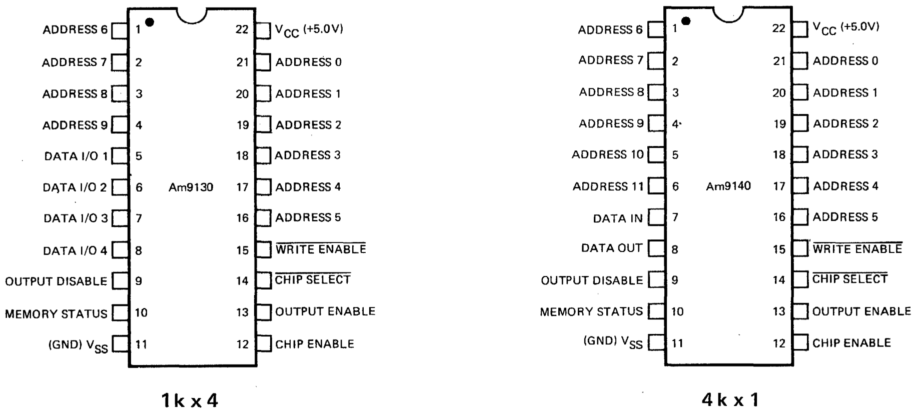

ADDRESS 6
ADDRESS 7
ADDRESS 8
ADDRESS 9
DATA I/O 1
DATA I/O 2
DATA I/O 3
DATA I/O 4
OUTPUT DISABLE
MEMORY STATUS
(GND) $V_{SS}$
1
2
3
4
5
6
7
8
9
10
11
Am9130
22
21
20
19
18
17
16
15
14
13
12
$V_{CC}$ (+5.0V)
ADDRESS 0
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4
ADDRESS 5
$\overline{\text{WRITE ENABLE}}$
$\overline{\text{CHIP SELECT}}$
OUTPUT ENABLE
CHIP ENABLE
1k x 4
ADDRESS 6
ADDRESS 7
ADDRESS 8
ADDRESS 9
ADDRESS 10
ADDRESS 11
DATA IN
DATA OUT
OUTPUT DISABLE
MEMORY STATUS
(GND) $V_{SS}$
Am9140
$V_{CC}$ (+5.0V)
ADDRESS 0
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4
ADDRESS 5
$\overline{\text{WRITE ENABLE}}$
$\overline{\text{CHIP SELECT}}$
OUTPUT ENABLE
CHIP ENABLE
4k x 1

Figure 2. Pin Assignments.

## Design Philosophy

Read/write random access memories are customarily divided into two categories based on the storage mechanism used in the memory cells. **Dynamic** memories use dynamic cells that store information in the form of charge on small capacitors. **Static** memories use static cells that store information in the form of latched currents flowing through transistors. Dynamic memories must be periodically refreshed in order to maintain the stored information. Static memories maintain the stored data without refreshing as long as power is applied. (Both types are volatile – that is, stored information is lost when power is removed.)

The basic storage mechanisms of the cells contribute significantly to the characteristics of the overall memory, but an important contribution is also made by the access method used with a particular cell. Dynamic storage has conventionally been used with dynamic decoding and control circuitry. Similarly, static storage has traditionally used static support circuitry. But those associations are not necessary. Other combinations are possible and provide different overall specifications. One example is provided by Advanced Micro Devices' 4K dynamic memories, the Am9050 and Am9060. They use static circuitry on some input signals in order to significantly improve several timing characteristics. There also exist several types of read-only memories that use dynamic decoding for improved performance.

The Am9130 and Am9140 memories take advantage of a new combination that provides static storage together with a novel type of clocked access method. The storage cells use a conventional, fully static design. The decoding and sensing circuits use a clocked static approach that has no dynamic nodes. The clocked circuitry allows the addition of several new features, increases speed and decreases power dissipation relative to an analogous non-clocked design. At the same time, the usual disadvantages of a clock have been either eliminated or minimized in these new memories.

This philosophy, combined with Advanced N-channel MOS technology, has produced these new combinations of features, including:

- Fully static storage
- Fast access and cycle times
- Low operating power dissipation
- Self-clocking mode of operation
- Single phase, low voltage, low capacitance clock
- Static clock that may be stopped in either state
- Address register on-chip
- Output data register on-chip
- Single +5 volt power supply requirement
- Interface logic levels identical to TTL
- High output drive capability
- Nearly constant power drain; no large current surges
- DC standby mode for reduced power consumption
- Operation over full military temperature range

## Interface Considerations

In common with other AMD static R/W RAM's, all of the input and output signals for the Am9130 and Am9140 memories are specified with logic levels identical to those of standard TTL circuits. The worst-case input high and low levels are 2.0V and 0.8V, respectively; the worst-case output high and low levels are 2.4V and 0.4V, respectively. Thus, with TTL interfacing, the normal worst-case noise immunity of at least 400mV is maintained.

All inputs include protection networks designed to prevent damaging accumulations of static charge. During normal operation, the protection circuitry is inactive and may be modeled as a simple series RC. See Figure 3. The first functionally active connection for every input is the gate of an MOS transistor. No active sources or drains are connected to the inputs so that no transient or steady-state currents are impressed on the driving signals other than the simple charging or discharging of the input capacitance, plus the accumulated leakage associated with the protection network and the input gate. Input capacitances are usually around 5pF and leakage currents are usually less than 1$\mu$A.

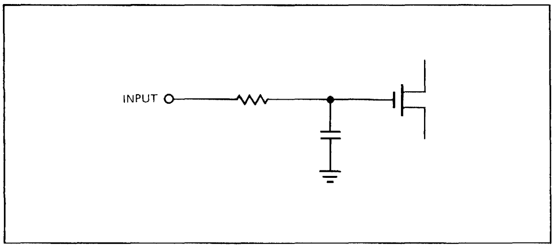


**Figure 3. Equivalent Input Circuit.**

The output buffers can source at least 200$\mu$A worst-case and can sink at least 3.2mA worst-case, while still maintaining TTL output logic levels. Thus, the memories can drive two standard TTL loads or nine standard Low-Power Schottky TTL loads. This unusually high output drive capability allows not only improved fan-out, but also better capacitive drive and noise immunity.

Delays in the output circuits show little variation with changes in the DC loads being driven. Changes with capacitive loading are shown by the curve in Figure 4. Access times are specified for a total load of one TTL gate plus 50pF of capacitance.

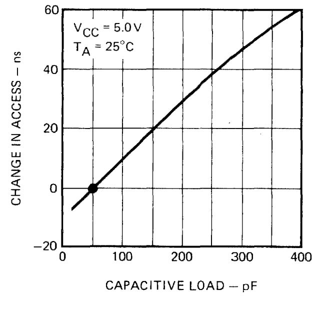


**Figure 4. Access Change Versus Load.**

## Power Supply

The Am9140 and Am9130 memories require only a single supply voltage. They perform their normal operations at a $V_{CC}$ of +5 volts. The commercial temperature range parts have a voltage tolerance of ±5%; the military temperature range tolerance is ±10%. The worst-case current drains are specified in the data sheets at the high side of the voltage tolerance and the low end of the temperature range. In addition, the current specifications take into account the worst-case distribution of processing parameters that may be encountered during the manufacturing life of the product.

The current drain for these parts is relatively quite constant over their various operating cycles. Since the basic storage mechanism involves latched currents in each cell, there is a necessary cumulative current flowing at all times, even when the memory is not being actively accessed. The average currents specified are largely independent of the CE input state, or the condition of any of the input signals. At the falling edge of the CE clock, there is a brief current surge of an additional 4 to 8mA that occurs as the decoders are being preset.

Dynamic memories usually have quite different current characteristics. Their average power dissipation is proportional to their operating frequency, so that average current drain decreases significantly when they are cycling slowly or doing refresh operations only. There are very large peak currents associated with every cycle in a dynamic memory, no matter how frequently or infrequently the cycles occur. Power supplies and power distribution systems must be capable of handling these peak demands.

Power vs. speed characteristics for the Am9130 and Am9140 4K statics are flat horizontal lines. See Figure 5. A representative 4K dynamic has a rising line as shown. The dynamic dissipation becomes higher than the regular-power static parts out near the high end of the speed range. The cross-over occurs much earlier for the low-power statics.

The power-down mode is entered by simply bringing both CE and OE low and then ramping $V_{CC}$ down as low as 1.5V. Power dissipation will fall by more than 80%. Normal cycles may resume when $V_{CC}$ has been returned to its operating range. See specification sheets for further details.

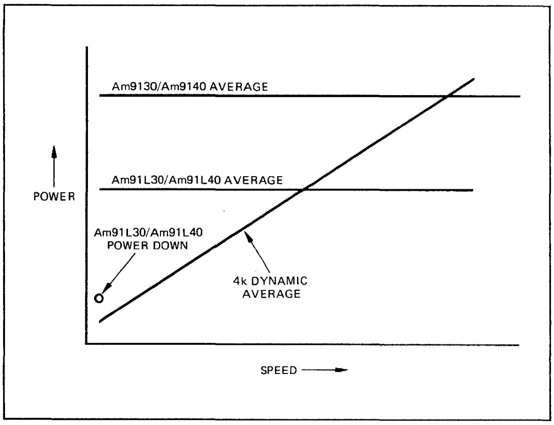


Figure 5. Power Versus Speed Comparisons.

## INTERFACE SIGNALS

### Signal Flow

Figure 6 is the block diagram for the Am9130 version and shows the interface connections along with the general signal flow. There are ten address lines (A0 through A9) that are used to specify one of 1024 locations, with each location containing four bits. The Chip Select signal acts as a high order address for multiple chip memory configurations. The Chip Enable clock latches the addresses into the address registers and controls the sequences of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A9) have been decoded and used to select one of 16 columns for each of the four sense amplifiers. The end result is that one cell is connected to one sense amplifier.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column bit lines and into the selected cells. Input and output data signals share common interface pins.

The output buffers use a three-state design that simplifies external interfacing. Unselected chips have the outputs turned off so that several chips may be wire-ored together easily. The Output Enable and Output Disable signals provide fully asynchronous controls for turning off the output buffers when desired.

Within the storage matrix, there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that help control the data flow through the part. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits. Memory Status specifies when output data is available and simplifies generation of Chip Enable.

Figure 7 is the block diagram for the Am9140 version. The basic operation and signal flows are similar to the Am9130. There are two additional address lines (A10, A11), allowing selection of one of 4096 locations. Each location contains one bit so only one set of data I/O circuits are needed. Input and output data signals use separate interface pins.

### Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. All active memory functions are initiated when CE goes high. At the completion of the active operation, CE goes low to preset the memory for the next cycle. There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-up and before beginning a valid operation, the clock should be brought low to initially preset the memory.

Figure 8 illustrates a basic operating cycle for either of the memories. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells. Various control functions are activated by these timing signals as the addresses and data flow through the memory.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write complete time indicated by the rising edge of the Memory Status output signal may be used. (See the Memory Status section of this Note.) It is perfectly acceptable to leave the CE clock high following the access time; some system operating modes will find it convenient to do so. A Read/Modify/Write cycle, for example, will keep CE high after the access until the modify and write portions of the cycle are finished.

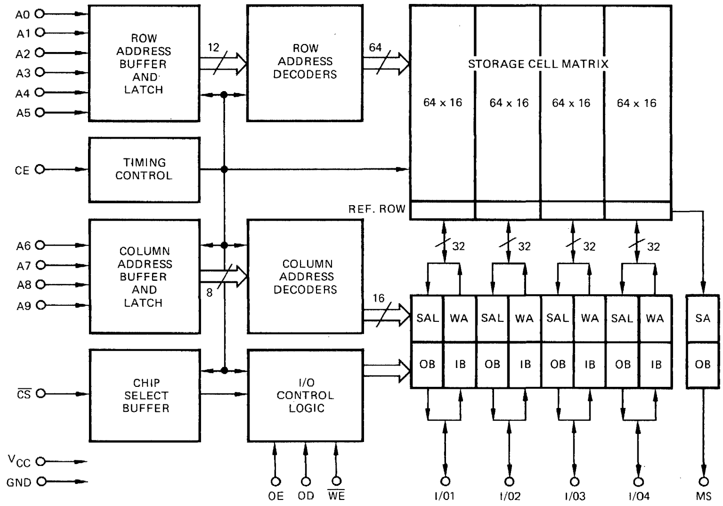

A0
A1
A2
A3
A4
A5
ROW ADDRESS BUFFER AND LATCH
12
ROW ADDRESS DECODERS
64
STORAGE CELL MATRIX
64 x 16
64 x 16
64 x 16
64 x 16
CE
TIMING CONTROL
REF. ROW
A6
A7
A8
A9
COLUMN ADDRESS BUFFER AND LATCH
8
COLUMN ADDRESS DECODERS
16
32
32
32
32
SAL
WA
SA
OB
IB
CS
CHIP SELECT BUFFER
I/O CONTROL LOGIC
VCC
GND
OE
OD
WE
I/01
I/02
I/03
I/04
MS

Figure 6. Am9130 Block Diagram.

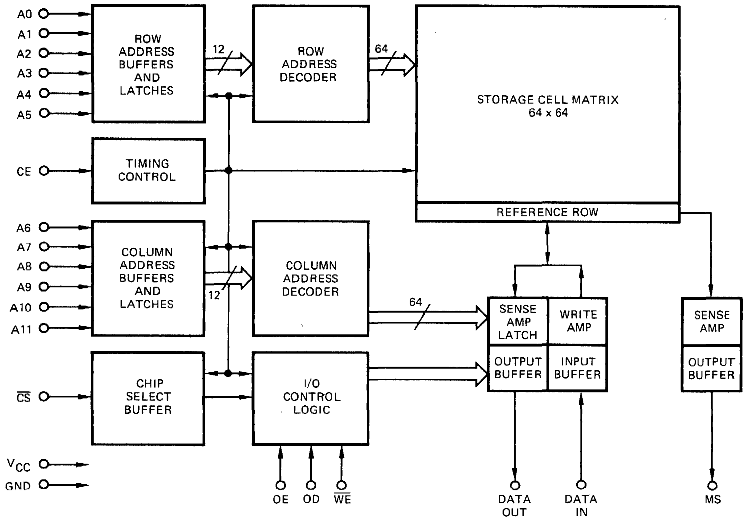

A0
A1
A2
A3
A4
A5
ROW ADDRESS BUFFERS AND LATCHES
12
ROW ADDRESS DECODER
64
STORAGE CELL MATRIX 64 x 64
CE
TIMING CONTROL
REFERENCE ROW
A6
A7
A8
A9
A10
A11
COLUMN ADDRESS BUFFERS AND LATCHES
12
COLUMN ADDRESS DECODER
64
SENSE AMP LATCH
WRITE AMP
SENSE AMP
OUTPUT BUFFER
INPUT BUFFER
OUTPUT BUFFER
CS
CHIP SELECT BUFFER
I/O CONTROL LOGIC
VCC
GND
OE
OD
WE
DATA OUT
DATA IN
MS

Figure 7. Am9140 Block Diagram.

When CE does go low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete as soon as Memory Status goes low. CE may remain low as long as desired.

## Address and Chip Select

The Address inputs are binary coded lines that specify the word location to be accessed within the memory. The Am9130 has 1024 word locations, any one of which may be selected by a ten-bit binary address ($2^{10} = 1024$). The Am9140 has 4096 locations and so uses a 12-bit address ($2^{12} = 4096$).

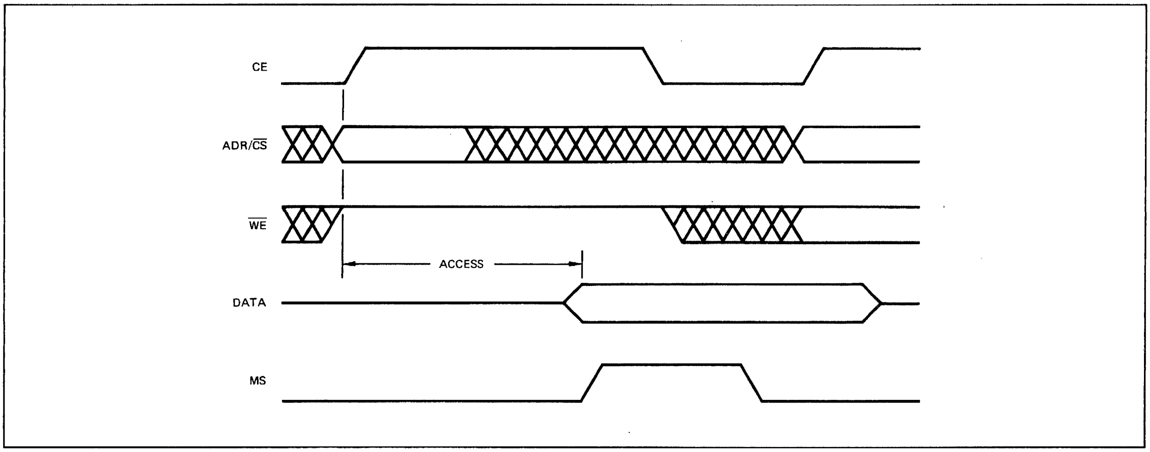


**Figure 8. Basic Operating Cycle.**

The Address input signals are latched into an on-chip address register by the rising edge of CE. They are allowed to become stable at the same time that the clock goes high: The address set-up time is zero. They must be held stable for the specified minimum time following the CE rising edge in order to be properly loaded into the register. Once the address hold time has been observed, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the memory system word capacity is larger than the word capacity of an individual chip. When multiple chips are stacked up, the Address lines may be wired in parallel to all chips and the CS lines used to individually select one active chip, or row of chips, at a time. Chip Select controls the operation of both the output buffers and the write amplifiers. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations so the Write Enable control signal and the input data lines may be wired in parallel to several chips.

CS is latched into the on-chip register in the same way that Addresses are. This means that once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins. The OE and OD lines provide asynchronous control over the output buffer when that function is necessary on a selected chip.

Chip Select is an active low function – that is, the input signal must be low at the rising edge of CE in order to select the chip. Most CS signals are derived from high order addresses. In small systems, a simple NAND gate can provide the necessary logic. In larger systems, a binary decoder (such as the Am25LS138) works well. In either case, the outputs are active low and thus directly match the input polarity of the Chip Select.

## Write Enable

The Write Enable line controls the read or write status of the devices. When the CE clock is low, the WE signal may be any value without affecting the memory. This allows the line to be indeterminant while the using system is deciding what the next cycle will be. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low during the cycle. The data sheet for the memories shows the minimum write pulse width required to successfully complete the writing of information into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle so that no intra-cycle timing is necessary for a write operation. The memories are designed so that WE may remain low continuously as long as successive write cycles are being executed.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated. Thus, the full minimum write pulse width must appear within the CE high time to perform a successful write.

If WE is low when CE goes high to initiate a new cycle, the write amplifier is enabled and the write data propagates onto the data lines internally. However, no columns or rows are selected until after the address for the new cycle is decoded, so actual writing into the cell is delayed by the decoding time following CE. This delay means that the minimum write pulse width cannot apply when WE goes low very early in the cycle.

## Data In and Data Out

The specification sheet requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. Input data may arrive earlier than the set-up time, where convenient. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. The data input hold time with respect to the termination of write is zero. If the Am9140 is used with the Data In and Data Out lines remaining separate, the input data may occupy the bus at all times, if desired. The valid written data is then determined by the timing of WE.

If the Am9140 is used with the Data In and Data Out tied together, or if the Am9130 is used, care should be taken to avoid conflict between incoming and outgoing data on the shared lines. It is important to note that when WE is low, it does **not** turn off the output buffers; the potential conflict must be resolved in other ways. One convenient method is to tie the Output Enable line to the WE line. Then, whenever WE goes low to write, it also turns off the output buffer. After a delay long enough for the output to reach its high impedance state, the input data can be introduced without conflict. The time that WE is low should be long enough to cover the output turn-off delay as well as the input data set-up time.

Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established. The conflicts occur with old output data that remains from a previous cycle or with new data that may be accessed before the write is established. If the write (and the associated input data) can be initiated while the output buffers are turned off, the conflict is eliminated; even if the outputs turn on, the output data will match the input data.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters an output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low.

At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off. This is done so that in multiple chip systems with the outputs bussed together, old data from one chip will not interfere with new data being accessed on another.

## Output Enable and Output Disable

The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

OE and OD are designed to provide asynchronous control of the output buffer independent of the Chip Select control. This capability makes it easy to tie together the Data In and Data Out lines on the Am9140 where bussed operation is desired, and simplifies operation of the Am9130 which has the Data I/O signals internally tied.

OD and OE will often be used to resolve contention on data busses, but there are other convenient uses as well. The nature of these memories is such that it is easy to individually clock each row in a memory system and to achieve an interleaved mode of operation that effectively shortens the average cycle time. In such designs, the output buffers must be controlled to prevent overlap of read information from two rows that are tied together but clocked at different times.

## Memory Status

Memory Status is a new, unique output signal that offers several important features for the memory system designer. It indicates when data is valid at the outputs, when CE may be brought low, and when preset is complete so that a new cycle may begin. The Memory Status signal may be completely ignored without affecting the operation of the memory. On the other hand, it has several implications that make it a potentially interesting and useful signal.

A major function of the MS concept is to indicate actual performance of the memory rather than worst-case performance. Thus, the access time indicated by Memory Status will always be better than the worst-case specification as long as the conditions and assumptions on which the worst-case numbers are predicated are better. Further, real operating results change with changing conditions and Memory Status follows those changes. Thus, for example, as temperature decreases, access time also decreases and MS tracks the change in access exactly.

There are many different ways to use the Memory Status signal and several are illustrated in this Note. Basically it offers improved performance and self-timed operation, along with other related implications.

# INTERNAL CIRCUITRY

## Address Register

The circuitry for the address register is shown in Figure 9. Inverters K and L isolate the register from the input pin and convert the TTL input levels to the wider logic swings used internally. M inverts the address so that both A and $\overline{A}$ propagate to the inputs of the register.

Transistors 1, 3 5, and 7 are depletion devices. Transistor pairs 1, 2 and 3, 4 form two inverters that are cross-coupled to provide the basic latch. Transistor pairs 5, 6 and 7, 8 are used to enter information into the latch. If point A goes high, then 5 and 6 turn on and 7 and 8 turn off, forcing the latch to one polarity. Notice that the circuit would work without transistors 5 or 7. They are added to minimize the propagation delay through the register.

When transistors 9 and 10 are turned on, 5, 6, 7 and 8 are turned off and the latch is isolated from the input signal. When transistors 11 and 12 are turned on, the outputs from the register are held low and the following address decoders are in their preset state.

The timing for the address register operation is shown in Figure 10. $\phi$B and $\phi$C are simply delayed inversions of CE. $\phi$A is derived from the outputs of the slowest bit position in the address register. During the preset state of the memory when the CE clock is low, both $\phi$B and $\phi$C are high and $\phi$A is low. In that condition, transistors 9, 10, 11 and 12 are all turned on and no signals can travel into or out of the register.

When CE goes high to start a cycle, $\phi$B goes low after a brief delay. This turns off 9 and 10 and opens a window that allows the address information at the input to proceed into the latch. The path that generates $\phi$B is slightly longer than the path that the address follows to the register. This is done so that the address setup time relative to CE can be specified as zero.

Next, $\phi$C also goes low, permitting the latch to set and the register outputs to travel on to the decoders. The delay from $\phi$B to $\phi$C prevents any address spiking from disturbing the decoding circuits.

During the preset time, both X5 and $\overline{X5}$ are held low, keeping $\phi$A low. After the active cycle starts, either X5 or $\overline{X5}$ will make a transition high, depending on the state of the Address 5 input. Thus, $\phi$A will go high in every memory cycle. When it does, transistors 9 and 10 will turn on again, closing the window into the latch. This prevents any changes in external address information from affecting the stored address. Notice that $\phi$A is dependent on the presence of address information and only occurs after the address has reached the register outputs.

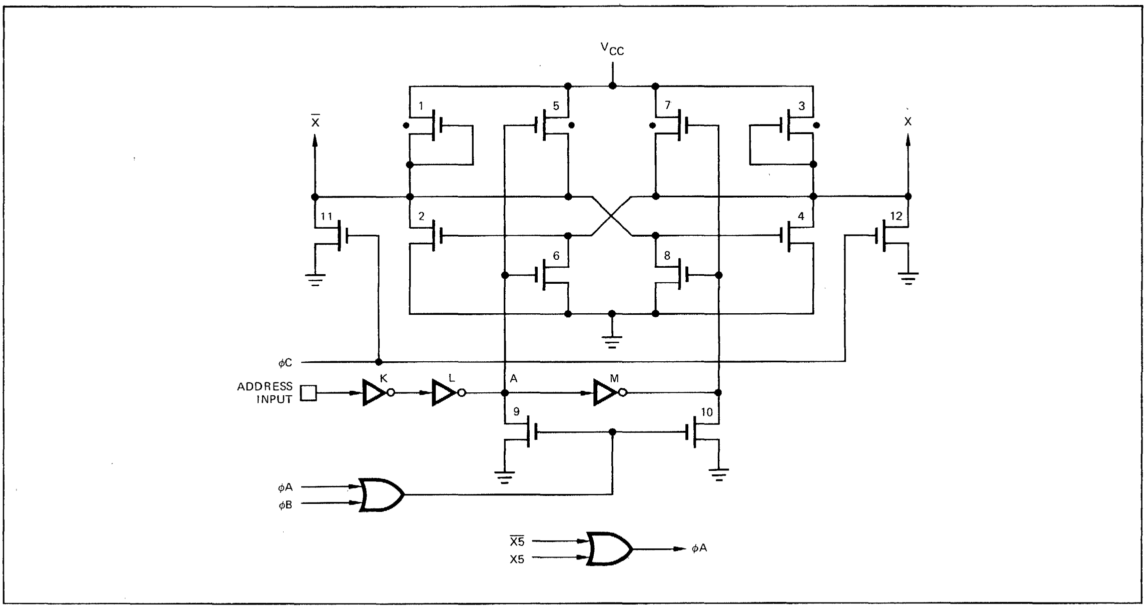


Figure 9. Input Latch Circuit.

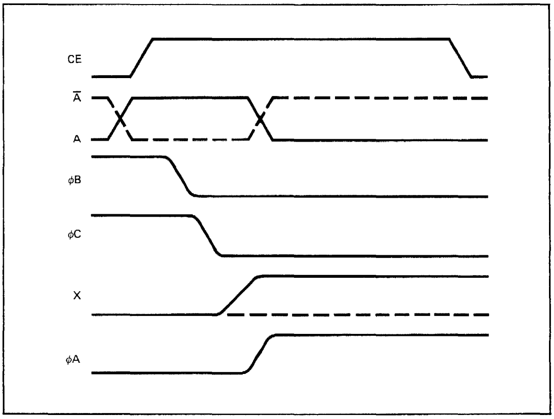


Figure 10. Input Latch Timing.

## Address Decoding

There are 64 of the row decoder circuits shown in Figure 11. The decoding is done by a simple six-input gate that is selectively wired to the outputs from the six low order bits of the address register. Each has a unique combination of X and X̄ signals on its inputs ($2^6 = 64$). Only one decoder will have all of its inputs low during the decoding. The other 63 gates have at least one input high, thus keeping the decoder output low and the row driver, T, off. The single selected gate allows its row driver to turn on.

ϕA, which is derived from the transitions of the X5 signals, is buffered and used as ϕDEC, the decoder clock. When ϕDEC goes high, it passes through the selected row driver and brings the associated row select line high. All the other row select lines remain low. During the preset time when CE is low, all of the decoders have all of their inputs held low by ϕC, thus enabling all of the row drivers. To keep all the rows unselected, ϕDEC is low during the preset time and keeps all the select lines low.

There is a simple latch connected to each of the 64 select lines. It holds its select line low and prevents it from floating when the row driver is turned off. An active (high) row select line flips and holds the latch in addition to driving the 64 cells in the row.

## Memory Cell

The storage cells that are the heart of the memories use a conventional static design with six transistors. See Figure 12. Transistor pairs 1, 5 and 2, 6 are connected as simple inverters that are cross-coupled to form a bistable latch. Either transistor 1 or 2 is turned on and defines the data state of the cell. Transistors 5 and 6 are depletion-mode devices that act as pull-ups and maintain the state of the latch as long as power is applied.

The access devices permit the cell to be attached to its bit lines. When the cell's row select line is low, 3 and 4 are off and the cell is isolated from all other circuitry. When the select line is high, 3 and 4 are on and the cell is connected to the bit lines. If a read operation is in progress, the cell then pulls one of the bit lines low. If a write operation is being performed, the bit lines are driven by the data to be written and the cell is forced into the desired state.

## Bit and Data Lines

Figure 13 shows the bit line column and data line organization. A total of 64 cells – one from each row – are connected to one bit line pair to form a column of cells. Columns are connected in parallel through the column select transistors to form the data lines. The data lines feed into a sense amplifier or are fed from the write amplifier. For the Am9140, all 64 columns are connected to one pair of data lines and one set

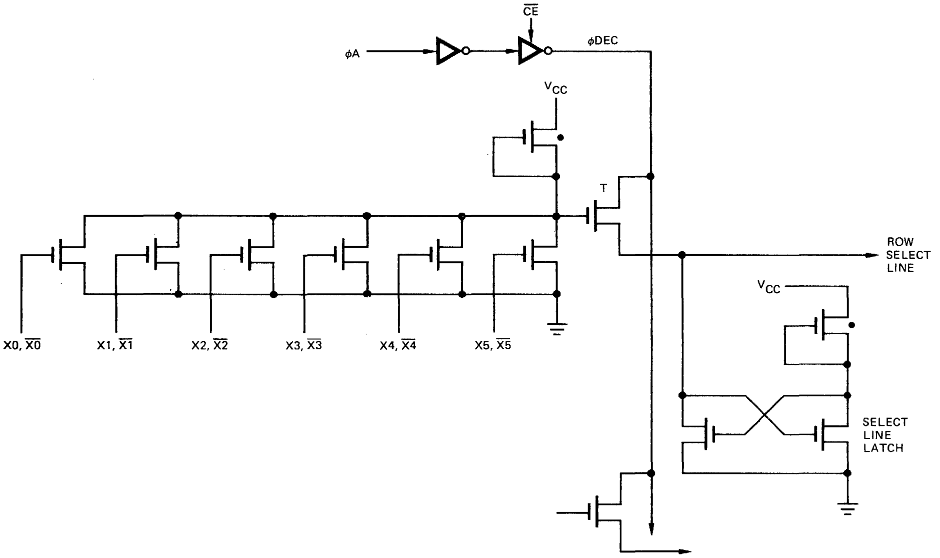

$\overline{\text{CE}}$
$\phi$A
$\phi$DEC
$V_{CC}$
T
ROW SELECT LINE
$V_{CC}$
SELECT LINE LATCH
X0, $\overline{\text{X0}}$
X1, $\overline{\text{X1}}$
X2, $\overline{\text{X2}}$
X3, $\overline{\text{X3}}$
X4, $\overline{\text{X4}}$
X5, $\overline{\text{X5}}$

**Figure 11. Row Decoder Circuit.**

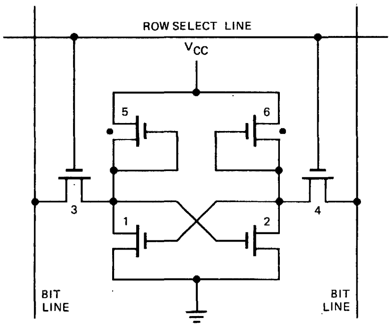


**Figure 12. Cell Circuit.**

of I/O circuits. For the Am9130, there are four pairs of data lines with four sets of I/O circuits and 16 columns are connected to each pair of data lines.

In addition to the storage cells, each column contains the reference row transistors and two other circuits labeled in the figure as EQ and BLL. The EQ circuit is active only during the preset time when CE is low. It is used to balance and equalize the bit lines and bring them to a voltage level somewhat below $V_{CC}$. The same EQ circuit is also used with the data lines.

The BLL circuit is a Bit Line Latch that is inactive during preset and is used during the active portion of the cycle to help the selected cell discharge the capacitive load presented by the bit and data lines. It is controlled by $\phi$L, a timing signal derived from the reference row.

The row driver, T, for the reference row is always enabled and the reference row is therefore selected by $\phi$DEC on every cycle. The two reference transistors in each column are the same as the access devices in each cell that are driven by the other row select lines. When the reference row select signal has propagated all the way to the end of the row, it is buffered and used to generate $\phi$L. When $\phi$L is true, the BLL is enabled and follows the state of the bit lines as set by the selected cell in that column.

The column decoders work much the same way as the row decoders, except that they are not turned on and off by a decode clock. During an active cycle, only one column is connected to one pair of data lines.

## Sense Amplifier

A unique feedback amplifier detects the state of the data lines to provide read data for the output. The circuit in Figure 14 shows a simple differential amplifier (transistors 2, 3, 4, 5) with a pedestal voltage established by transistor 1. The output from the differential stage is fed back to influence the pedestal via transistors 6, 7 and 8. Notice that differential signals are balanced out and eliminated from the feedback loop. But supply voltage, temperature and process variations cause common mode shifts that are compensated for.

The output of the differential stage also goes to a latch circuit that squares and buffers the amplified signal. The latch simply follows the data that flows into it and feeds information to the output data register.

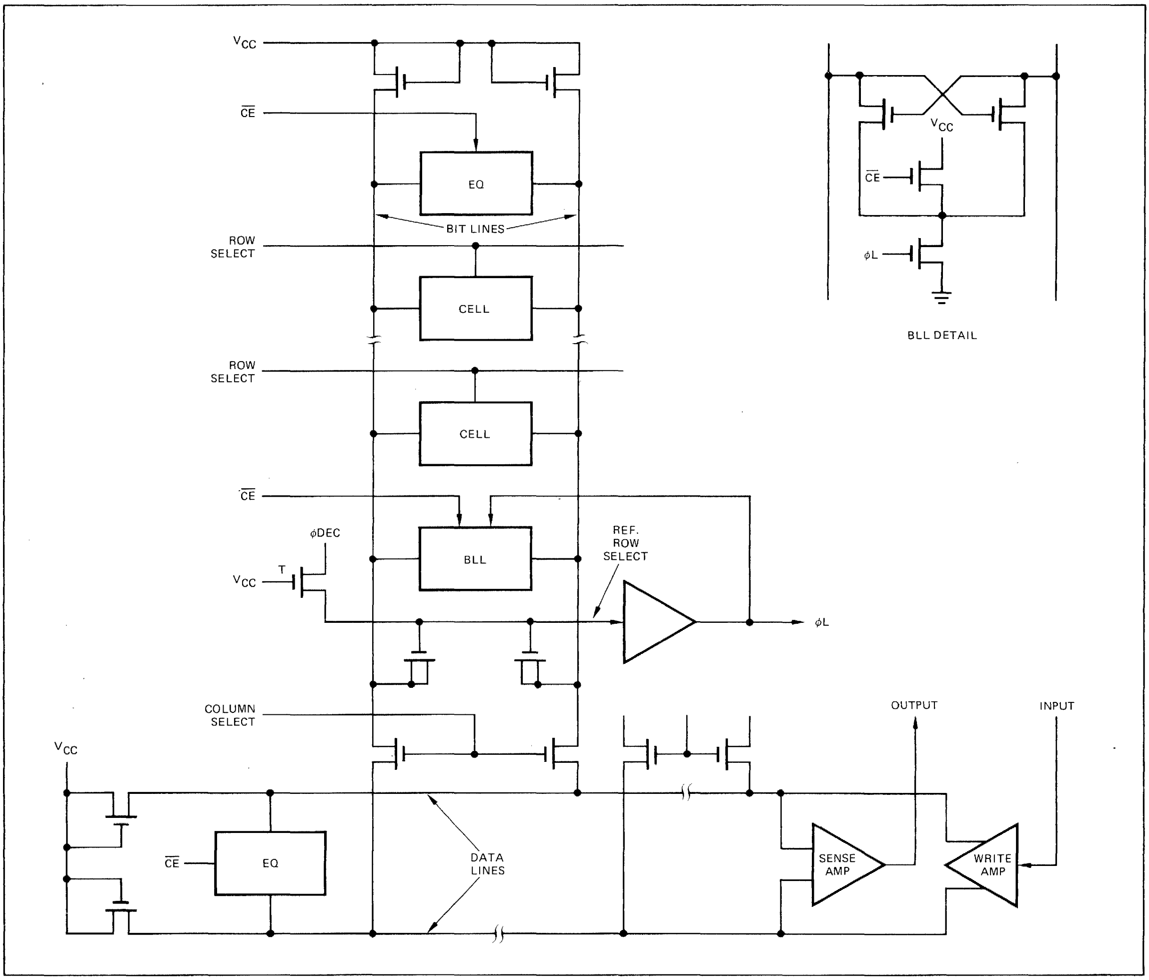


Figure 13. Bit and Data Line Organization.

## Data I/O Stages

The output stage shown in Figure 15 includes the output data register plus the output control logic plus the output buffer. Information from the sense amplifier can flow into and through the register and on to the output pin at the access time. As long as the CE clock is high, the cell addressing will be valid and the sense amplifier and output can remain stable. When CE goes low, the register inputs are isolated from the sensed data and the output can stay valid until CE next goes high.

There are several signals that can turn off the output buffer. Only when they are all simultaneously in the necessary state will the output turn on. When CE goes high, the output will turn off until the access time arrives as indicated by ϕL. When $\overline{CS}$ is latched high, the output will be off. When OE is low the outputs will be off. When OD is high the outputs will be off.

The write amplifier control logic only allows a write to take place on a selected chip with the CE high and the Write Enable low. Note that the WE line does not affect the output buffer. On the Am9130, the data input and output signals are tied together and share common interface pins.

## Memory Status Circuit

The Memory Status output is derived from the internal ϕL timing signal that is in turn derived from the true performance of the reference row. MS uses the same output buffer, control logic, register and sense amplifier circuitry as used in the data path. Even where a control gating function is absent, the circuitry is included but disabled. At the input to the MS sense circuit, a pseudo data line pair is created that is directly analogous to the storage cell data lines, including the EQ and column select devices. The result is that Memory Status tracks the output data very closely under all operating conditions.

Since the final output circuits are the same for both MS and Data, they respond identically to variations in loading. If the data output is heavily loaded, then similar equivalent loading should be used on the Memory Status output in order to maintain their responses relative to each other.

The MS output is always enabled and never enters a three-state off mode. Even on an unselected chip, the MS signal continues to reflect the status of the memory.

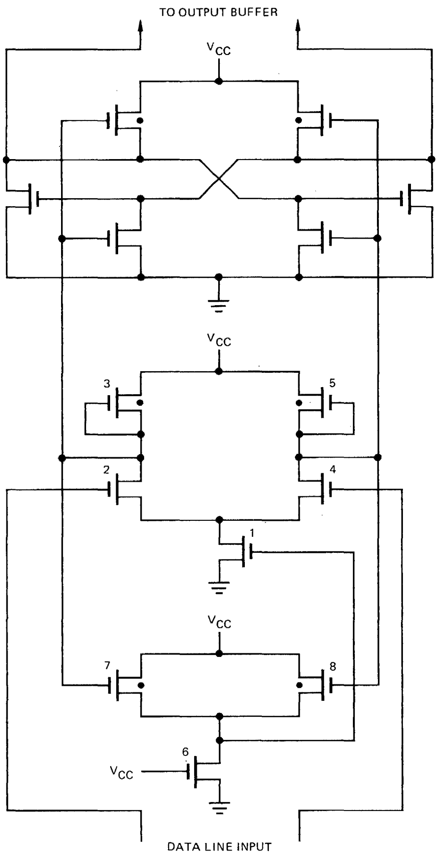

TO OUTPUT BUFFER
$V_{CC}$
$V_{CC}$
3
5
2
4
1
$V_{CC}$
7
8
6
$V_{CC}$
DATA LINE INPUT

Figure 14. Sense Amplifier Circuit.

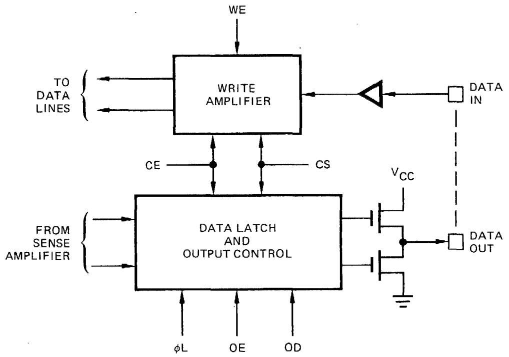

WE
TO DATA LINES
WRITE AMPLIFIER
DATA IN
CE
CS
$V_{CC}$
FROM SENSE AMPLIFIER
DATA LATCH AND OUTPUT CONTROL
DATA OUT
$\phi$L
OE
OD

Figure 15. Data I/O Stages.

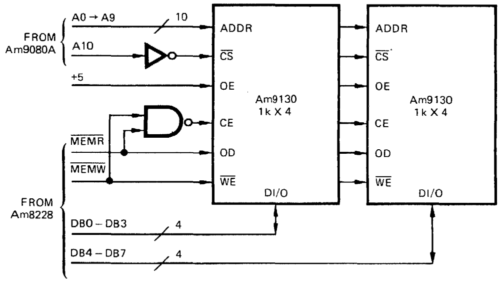

FROM Am9080A
A0→A9
10
A10
+5
$\overline{\text{MEMR}}$
$\overline{\text{MEMW}}$
FROM Am8228
DB0–DB3
4
DB4–DB7
4
ADDR
$\overline{\text{CS}}$
OE
CE
OD
$\overline{\text{WE}}$
Am9130 1k X 4
DI/O
ADDR
$\overline{\text{CS}}$
OE
CE
OD
$\overline{\text{WE}}$
Am9130 1k X 4
DI/O

Figure 16. 1k x 8 R/W Memory for Am9080A.

## SYSTEM DESIGNS

### Interface Timing

The specification sheets for the Am9130 and Am9140 show the various input requirements and output responses for the memories. In each case, the parameters shown are worst-case in order to fully describe the operational limits of the parts. But many system situations allow the timings to be greatly simplified. For example, in small memories that are only one chip deep, the Chip Select signal may not be required and $\overline{\text{CS}}$ may be tied low. Similarly, in many instances OD may be tied low or OE may be tied high or both.

In some circumstances, it may be quite convenient to leave the addresses stable longer than the parts require. The falling edge of CE might be used by the associated system to initiate the derivation of a new address and the decision about reading or writing the next cycle. Those signals can then stay stable until the following decision time.

It will quite often be easy to leave the Write Enable line low during all of the CE high time of a write cycle. This eliminates some intra-cycle timing of the write pulse. The WE line may be any value as long as CE is low. Similarly, it will also be easy to have the Data In information available during the time that WE is low – indeed, WE will often be useful as the control line for gating the incoming data on and off.

Many times CE can be easily and directly derived from other signals in the using system. Figure 16 shows an example of a small memory for a microprocessor. Two Am9130 parts form a 1K x 8 memory for an Am9080A. The processor supplies the Addresses and the chip select signals. The Am8228 System Controller associated with the processor supplies the $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ control lines as well as a buffered data bus. A10 is inverted and used for the Chip Select signal, placing the addressing range in the second 1K of system memory. For larger systems or different configurations, other select logic may be required.

The Controller can request a Memory Read or a Memory Write operation. The NAND gate shown generates a CE when either request is made. When $\overline{\text{MEMR}}$ is high, the output buffers are turned off via the OD control. When $\overline{\text{MEMR}}$ is true the memory output will be connected to the data bus. When $\overline{\text{MEMW}}$ is low, a write operation is performed at the specified address. There is always sufficient time between operation requests for the memory to be fully preset.

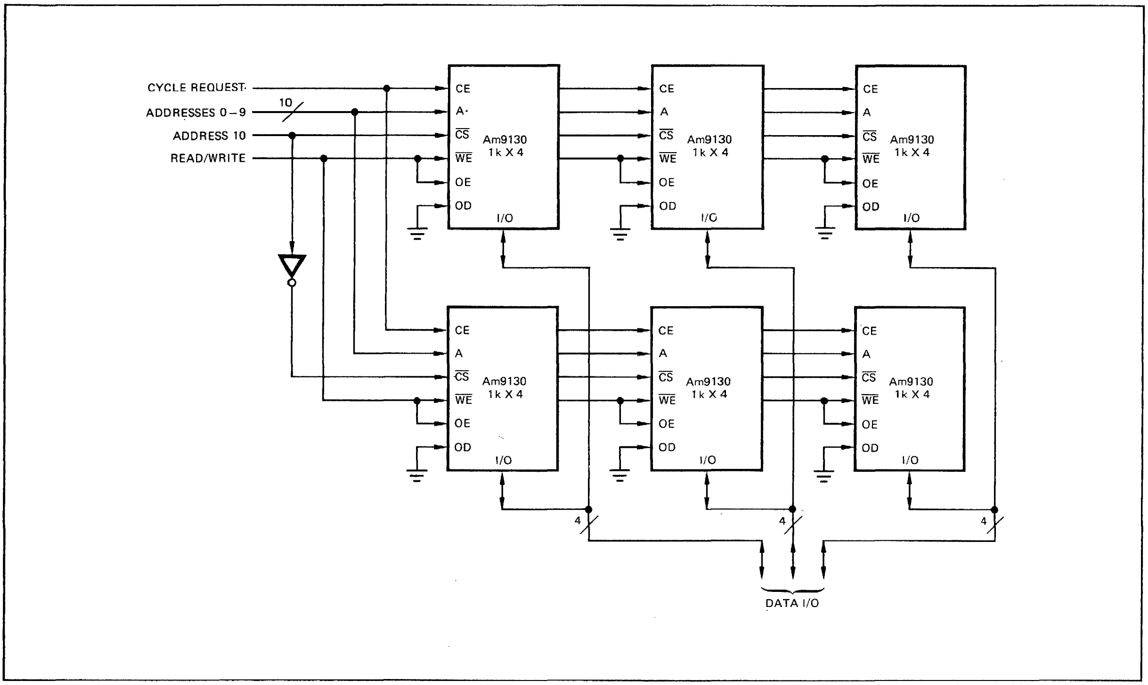


Figure 17. 2k x 12 Memory System.

## Small Memory Arrays

As an illustration of a conventional approach for operating multiple chips, Figure 17 shows a convenient way to connect six Am9130 chips to make a 2K x 12 memory. The Chip Enable clock is wired in parallel to all six chips, as are the ten Address lines and the R/W control line. Output Disable is tied to ground, allowing Output Enable to provide asynchronous external control of the output buffer status. OE is tied to Write Enable so that the R/W line turns off the output buffers when it goes low during a write cycle.

Address 10 and its inversion are used to select one of the two rows of chips for each operating cycle. As long as A10 is low, the upper row will respond to the clock and will communicate on the data bus while the lower row is deselected and can neither read nor write. When A10 is high the row roles are reversed.

The Data I/O lines have corresponding bits tied together in vertical columns. The control logic is arranged so that only one of the output buffers at a time will drive an I/O line, and only one chip at a time will write from an I/O line.

The type of memory illustrated is easily expanded to many different capacities. An 8K x 16, for example, could be implemented with 32 Am9140 chips (16 in each row), using the same control line configuration, plus two more address lines.

Driving and buffering limitations for both the inputs and the outputs will be dictated by a) accumulated leakage currents and b) accumulated capacitance. On an address line, for example, many chips may be driven in parallel from a standard TTL output. As the number of chips goes up, the leakage currents in the MOS memory gradually become a significant load for the TTL output especially in the high logic level state. Similarly, many parallel inputs will present a capacitive load that will degrade the rise and fall characteristics of the signal. Added buffering will usually only be necessary when the transition times begin to cause the overall system delays to be excessive.

As the capacity of systems like the one in Figure 17 grows, decoding of the Chip Select information gradually involves a little more logic. If the memory was 3K x 12, for example, it might be implemented with three rows of Am9130 chips. Select information is then needed to assure that only one of the rows at most is active at a time. A one-of-three decoder is easy to implement from two address lines with simple gates as shown in Figure 18. As the number of rows to be selected grows, however, both the wiring and the gate count tend to get much more complex.

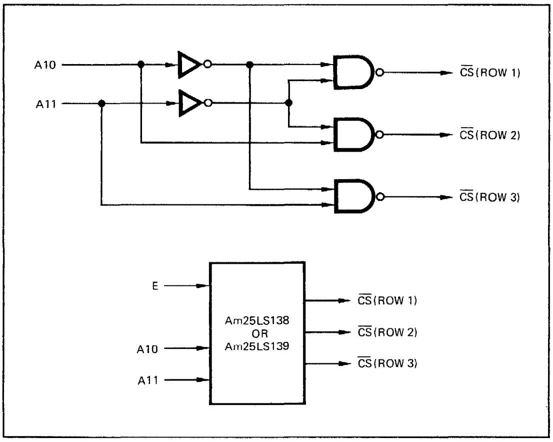


Figure 18. Chip Select Decoding.

Another approach (also shown in the Figure 18) takes advantage of MSI binary decoders like the Am25LS138 or Am25LS139. Both offer package count advantages, especially as the system gets bigger, and control logic is included that permits deselection of all rows. This can be handy for power-down situations and some other circumstances. Notice that the output polarity is such that the decoders interface directly with the memory chips.

The Am9140 can be converted to a common I/O instead of a separate I/O device simply by wiring together the Data In and the Data Out lines. When that is done, the same precautions suggested for the Am9130 concerning bus contention should be observed. Conversion of the Am9130 from common to separate I/O is only slightly more complex. The Am2915 (or Am2905) is a quad three-state bus transceiver. When connected as illustrated in Figure 19, it serves to create the bus needed by the Am9130 from separate input and output data. It even includes convenient registers on both sides. For a circuit without the registers and other control features of the Am2915, try the Am8T26. Both are four bits wide and so match up nicely with a column of Am9130 chips operating in parallel.

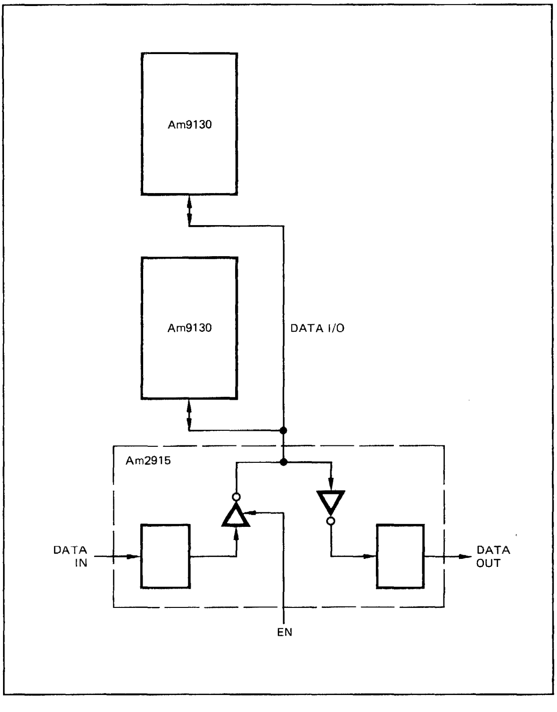


Figure 19.

## Memory Status Timing

Figure 20 shows the timing information conveyed by the MS output. The rising edge indicates that output data is valid and makes a convenient strobe for output to the rest of the system. See Figure 20a. When several chips are being used in parallel, the Memory Status signal from the slowest chip should be the strobe in order to assure that all the data bits are available and valid. There is a brief nominal delay from the worst-case output data to the rising edge of MS. That time is always greater then zero under similar loading conditions for the two signals.

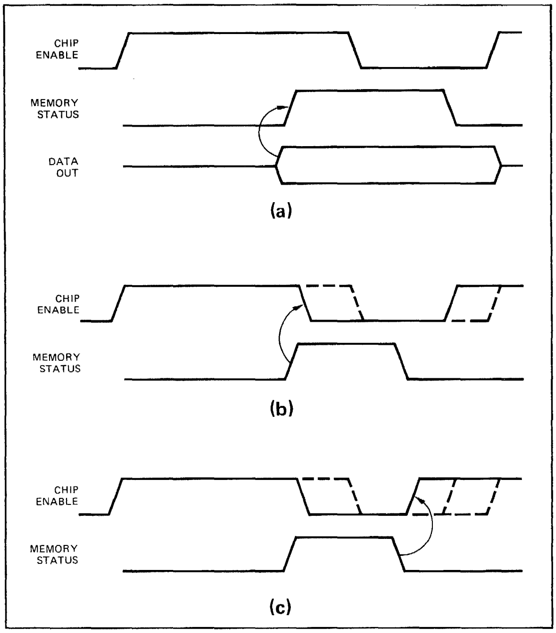


Figure 20. Memory Status Information.

The front edge of MS also specifies the end of the time that CE must be held high for that operation. See Figure 20b. Though CE may be high as long as desired, it may safely go low any time after MS goes high. MS will stay high until the internal preset operation is complete. Thus, it will not go low until some time after CE goes low and the total time that MS is high depends not only on the actual operating conditions of the memory, but also the delay from MS high to CE low.

The falling edge of MS specifies that the memory is ready for a new operation to be initiated. See Figure 20c. When several chips are operated in parallel, the latest falling edge will indicate the earliest time that their CE should go high. The chip with the longest access time will also be the chip with the longest preset time. The picture in Figure 21 shows an MS waveform during a simple read cycle.

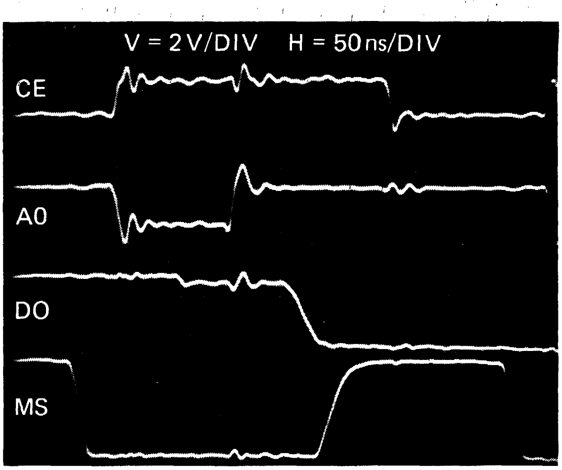


Figure 21. Read Cycle Waveforms.

Memory Status is derived from the selection of the row of reference cells and the reference row is always doing a read operation. Thus, the MS output will appear in every operating cycle, whether a read or a write is being performed. If the Write Enable line is low at the start of the cycle, and if the input data are present at the same time, MS may be considered a valid indication that the write is complete and CE may be switched low. However, if WE is not low or input data are not present until sometime later in the cycle, then the worst-case write timing requirements as shown in the specification sheet must be observed, independent of indications from the rising edge of MS. The falling edge of MS will be fully valid in any type of cycle.

Since the requirements for the two transitions of the Chip Enable clock can be fully specified by the transitions of the Memory Status output, these memories can be effectively self-clocking. The MS output may be inverted and then used as the CE input as shown in Figure 22. Not only will the memory run properly, but it will run at its best frequency for any given set of operating conditions and it will change that frequency as the conditions change. There are many potential capabilities implied by the Memory Status concept, including: adaptive self-timed memories, true asynchronous operations, elimination of support circuit skews, temperature compensation, new memory architectures, improved speed/power ratio, etc.

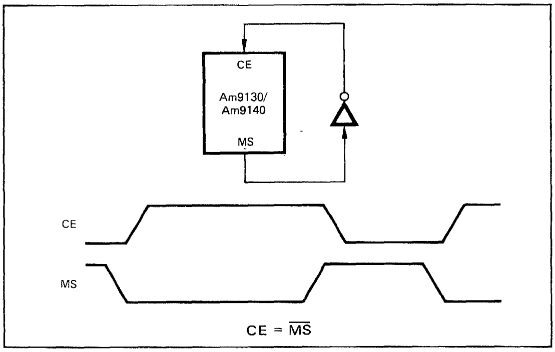


Figure 22. The Self-Clocking Memory.

## Memory Status Coordination

Figure 23 shows logic for combining multiple Memory Status signals. Gate A is used to detect when **both** MS outputs are high indicating that output data is available. Similarly, gate B detects that **both** MS outputs are low, indicating that the preset period is complete for both chips. The system associated with the memory can use this information to coordinate the flow and the generation of the CE clock. Essentially, this logic allows the slowest chip to govern the overall memory speed. The inputs to the coordinating logic can of course be expanded to handle as many chips as desired.

To combine these two pieces of status information, a simple cross-coupled latch can be added as shown in Figure 24. Since there are times when neither condition is true, the latch serves to maintain the previous status indication until a new state is valid. The result is a System Status signal that specifies for the system the same information that each MS signal specifies for an individual chip.

The clock may be derived independently for synchronization with the using system. Alternatively, the System Status signal may be inverted and used for the CE clock as indicated by the dotted line. The timing for this arrangement is shown in Figure 25. The memory will free-run at its best speed and the System Status will provide a synchronizing signal for use by the rest of the system.

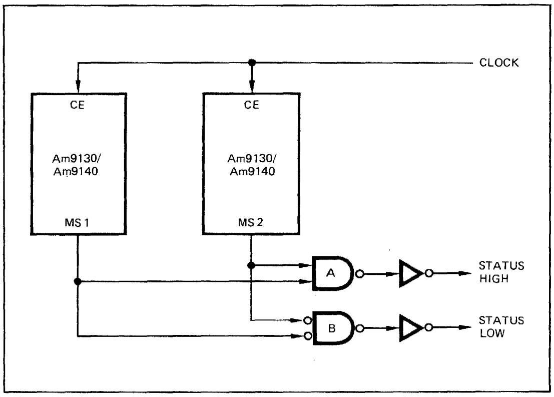


Figure 23. Status Coordination Logic.

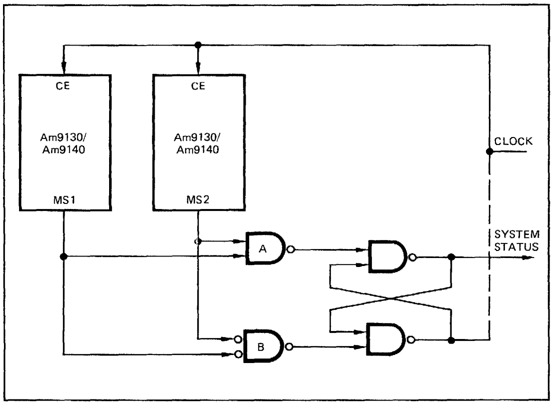


Figure 24. Clock Generation Logic.

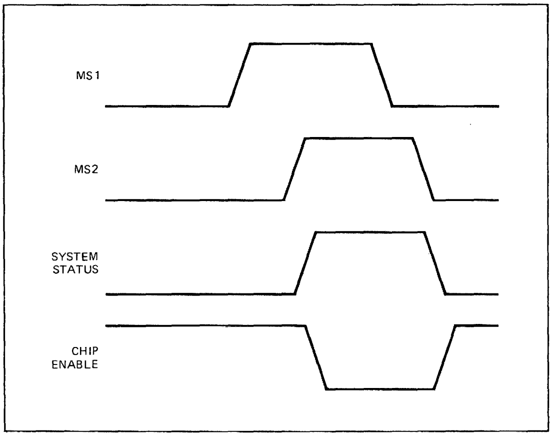


Figure 25. Status Timing.

## Handshaking Control

For systems that cannot be memory-driven, some means of controlling the clocking is needed. To permit the memory to single-step, a gate can be inserted in the dotted line of Figure 24 with a control line to turn the clock on or off. A more versatile and more asynchronous approach is illustrated in Figure 26. An additional latch is added to generate the clock so that the status information is derived independent of the clock control.

When the Cycle Request input is low, the memory will preset and prepare for an active cycle. When all is ready, Status Acknowledge will go low. When CR goes high, the memory will execute a cycle and will acknowledge conditions of access by bringing SA high. CR and SA then form a simple asynchronous handshaking pair for memory control. Notice that CR may go high at any time to start a cycle. If the chips are ready (SA low), the clock will proceed, but if preset is not complete (SA high) the memory will wait before initiating the requested cycle.

The timing for CR is quite simple. It should be held high until SA goes low. If SA is already low, a narrow CR pulse will suffice. Thus, a brief Cycle Request will cause the memory to execute one complete cycle and stop. If CR is held high, the memory will access (SA goes high) and then will leave the clock high until CR goes low. This allows Read/Modify/Write operations to be performed quite easily.

Advanced Micro Devices has designed a Low-Power Schottky support circuit for use with these memories. It integrates all of the logic for coordinating several Memory Status signals and for controlling the CE clock. It uses the same basic approach as shown here. Please contact the factory for details.

## Interleaved Operation

With the clock derived locally within the memory from the MS signals, and with the clocking logic integrated on a single chip, it becomes convenient to individually clock each row of a memory system. An example configuration is shown in Figure 27, with each support logic block being similar to the circuitry previously discussed. Each row is clocked only when it is addressed by the Chip Select signal (A0 or $\overline{A0}$). Unselected rows wait in their preset state until they are selected and clocked. The Cycle Request input is steered to the selected row by added logic. The Status Acknowledge outputs are three-state and only the SA for the selected row is turned on. The selected row will proceed when its preset is complete. When the data from the requested operation is available, the Status Acknowledge output goes high. The using system can then request another operation immediately once a new address is ready.

Independent clocking of each row adds little support circuit complexity while providing increased overall performance in two ways. First, the speed of each access is limited only by the slowest device in the selected row rather than the slowest device in the whole array. Secondly, successive operations in different rows will be faster because the wait for preset is eliminated; one row will preset while another is being accessed. Notice that the low order bit is used as the Chip Select address. In many systems, this will improve the distribution of alternate accesses for sequential information by mapping even addresses in one row and odd addresses in the other.

In any event, no matter where the operation is addressed or when it is requested, the memory will respond in the best possible time. The Cycle Request and Status Acknowledge signals form a true asynchronous handshaking pair. All of the variations in performance caused by the timing of the request, the row addressing patterns, the speeds of the individual chips and the memory operating conditions are automatically reflected in the response of the Acknowledge signal. An interesting challenge will be to design using systems that can take advantage of this unusual capability.

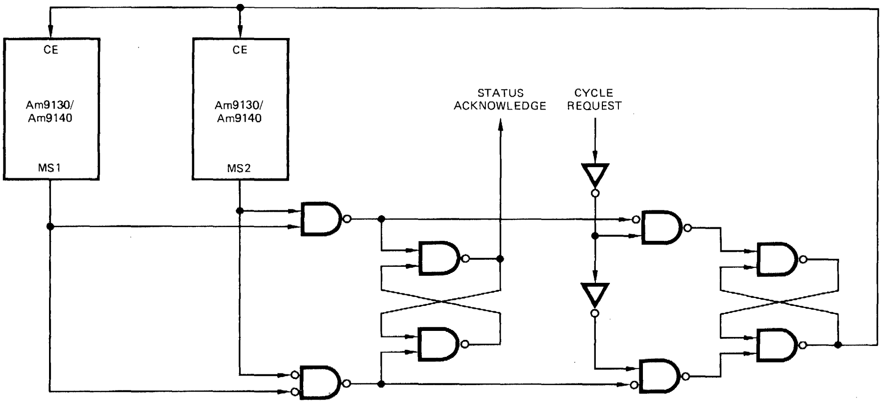


Figure 26. Handshaking Control.

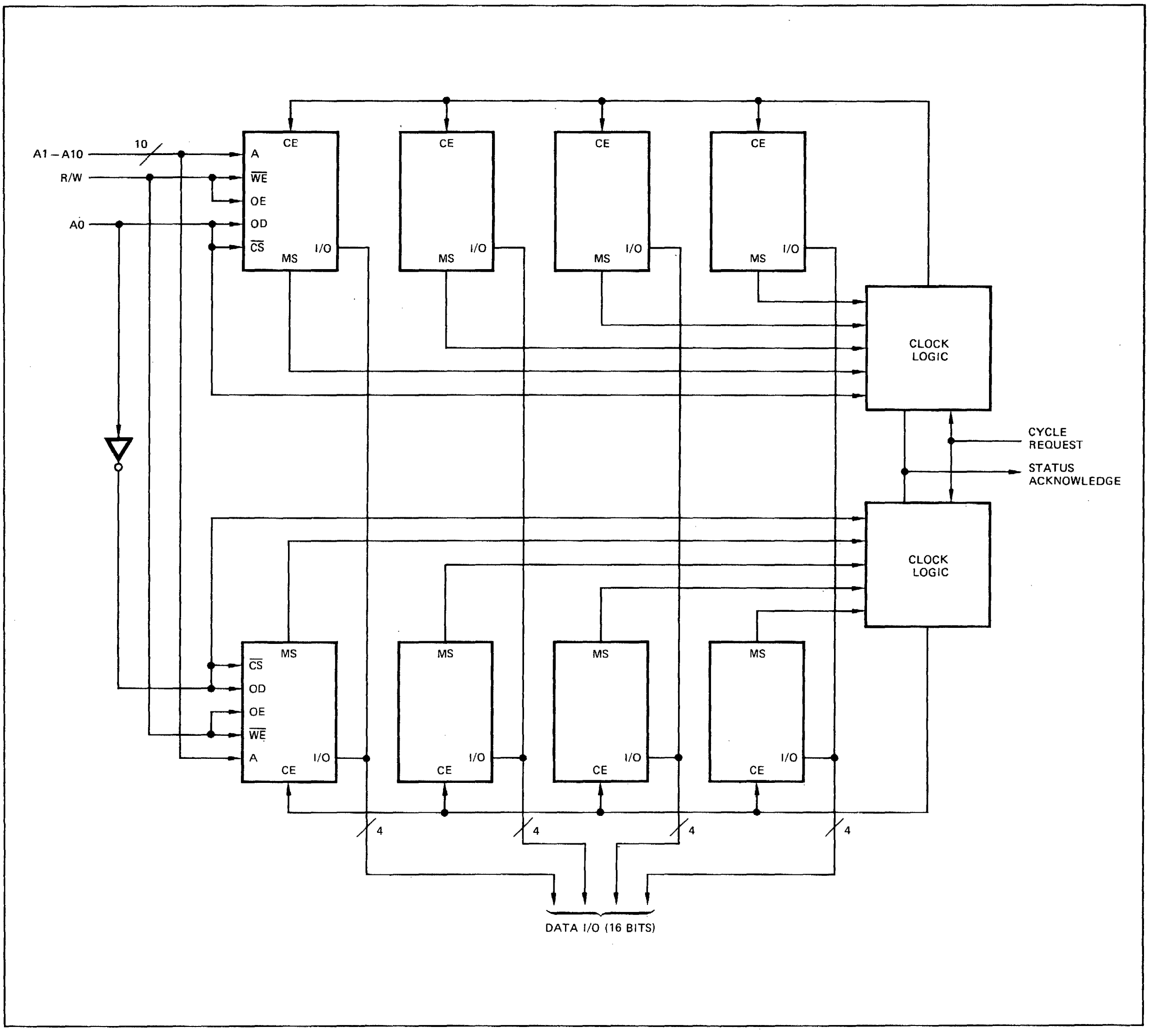

A1 – A10
10
R/W
A0
A
WE
OE
OD
CS
CE
MS
I/O
CLOCK LOGIC
CYCLE REQUEST
STATUS ACKNOWLEDGE
4
DATA I/O (16 BITS)

Figure 27. 2k x 16 Interleaved Memory System.

# APPLICATIONS OF DYNAMIC SHIFT REGISTERS

**By John Springer, Digital Applications**

## INTRODUCTION

MOS technology has several characteristics that make it ideal for data storage. Because MOS structures are small, relative to bipolar devices, a large number of bits can be stored on a small chip. Additionally, MOS devices exhibit high impedances that make it possible to store data on small parasitic capacitors rather than in normal cross-coupled transistor pairs. Using capacitive storage techniques has the effect of further increasing the number of bits that can be stored in a given area, because the number of MOS devices needed per bit is reduced. Circuits that store data on capacitive nodes are called "dynamic" because they depend on continual refreshing of the stored charge to maintain its integrity. In random access memories this refreshing is usually accomplished by reading and re-writing the data back into the same storage nodes through some internal refresh circuitry. In dynamic shift registers refreshing is accomplished by simply shifting the register, so that the stored data is "read" from one bit and written into the next one. Dynamic storage introduces a new constraint on operation of a shift register in that there is not only a maximum operating frequency due to normal propagation delays, but also a minimum operating frequency defined by the maximum time that can elapse between refresh operations. This application note deals with the series of dynamic MOS shift registers in Table I.

Table 1

| Device | Length | Maximum Data Rate |
|---|---|---|
| Am1402A | 4 X 256 | 5 MHz |
| Am1403A | 2 X 512 | 5 MHz |
| Am1404A | 1024 | 5 MHz |
| Am1405A | 512 | 3 MHz |
| Am2802 | 4 X 256 | 10 MHz |
| Am2803 | 2 X 512 | 10 MHz |
| Am2804 | 1024 | 10 MHz |
| Am2805 | 512 | 4 MHz |
| Am2806 | 1024 | 4 MHz |
| Am2807 | 512 | 4 MHz |
| Am2808 | 1024 | 4 MHz |

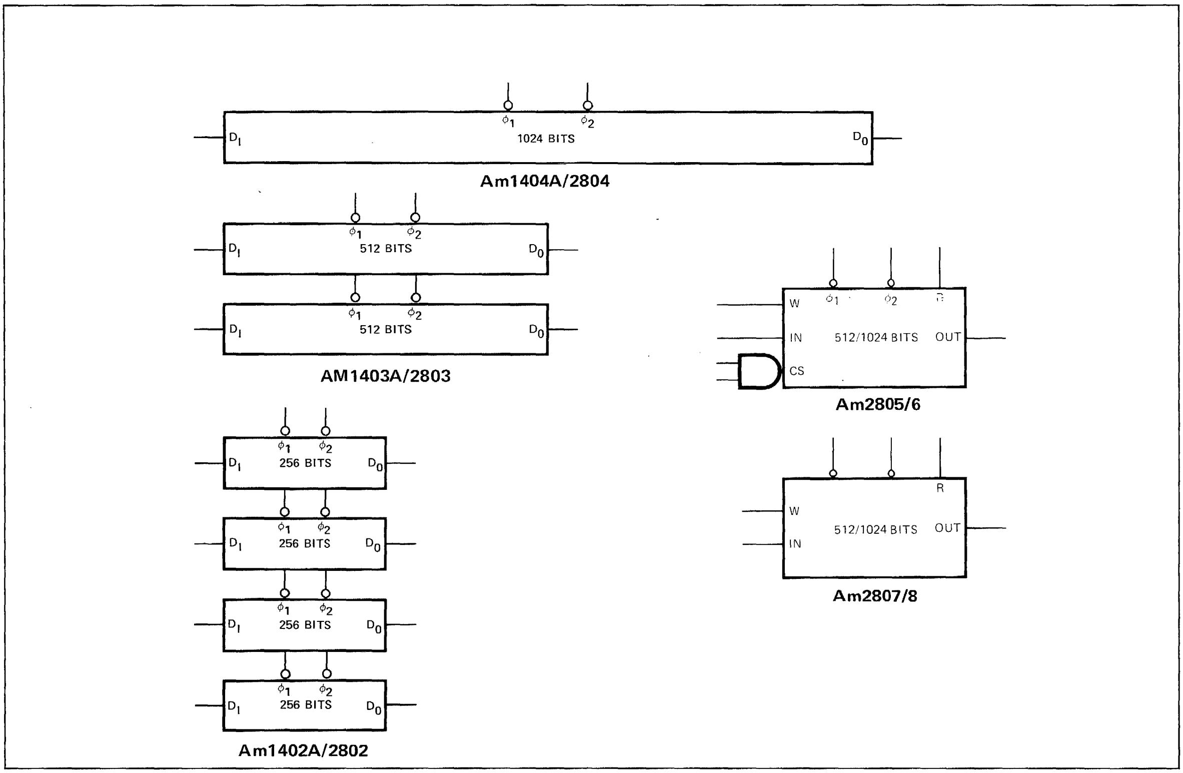


Figure 1. Advanced Micro Devices Dynamic Shift Registers

## DYNAMIC SHIFT REGISTER CIRCUIT

In dynamic shift registers data storage occurs entirely on capacitive nodes. The circuit used for each bit of the registers is shown in Figure 2. Each cell consists of two storage nodes, which may be designated the master and the slave. There are two clock lines fed to each cell; one clock causes data on the input to be fed into the master storage node and the other causes data stored on the master node to be shifted into the slave. The output of the slave feeds the master input to the next cell. The two storage nodes, alternately activated, provide the escapement mechanism used in all types of dual rank flip-flops to prevent data from feeding straight through from the input to the output.

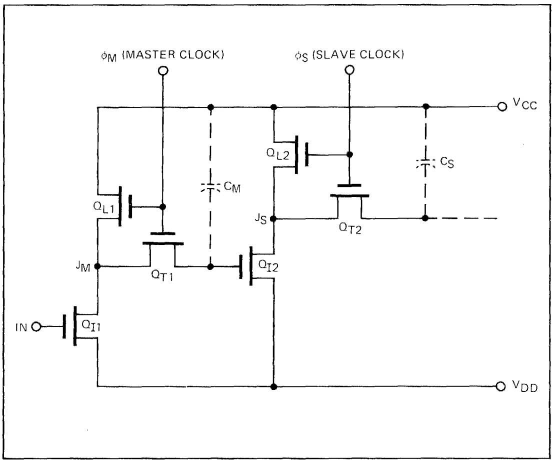


Figure 2. Dynamic Two-Phase Storage Cell

The master and the slave in the cell each consist of three transistors, which may be designated as the input transistor ($Q_{I1}$, $Q_{I2}$), the load transistor ($QL_1$, $Q_{L2}$) and the transfer gate ($QT_1$, $QT_2$). Each of these transistors behaves like an open circuit when its gate is at a HIGH logic level and like a closed switch or resistor (the impedance depends on the geometry of the device) when its gate is at a LOW logic level. The gate input impedance is very high, on the order of $10^{18}$ ohms, so virtually no current flows into the gate.

The dynamic operation of the circuits is illustrated in Figure 3. When both clocks are HIGH the load and transfer gates are off, and no current flows in the circuit. The data on the input turns the input transistor on or off. When the master clock goes LOW, the load transistor turns on and serves as a load resistor of about 200k ohms for the input device, establishing a level near $V_{CC}$ or near $V_{DD}$ (depending on the state of the input transistor) at point JM. At the same time the transfer gate, $Q_{T1}$, turns on, allowing current to travel onto or off of the parasitic storage capacitor, so that the voltage on the capacitor is the same as the voltage at point JM. When the master clock goes HIGH, the transfer gate shuts off and the stored level is trapped on the capacitor. The load transistor also shuts off so that power is no longer dissipated through the input transistor. At some time later the slave clock goes LOW and the identical process occurs in the slave half of the cell. When the charge is stored at the output of the slave it is also at the input to the master of the next cell, so a shift of one bit in the register is accomplished by applying a master clock and then a slave clock. Note that power in the register is consumed only when one of the two clocks is LOW.

The mode of operation described above is typical for all dynamic two-phase shift registers. A disadvantage of the two-phase operation is that two clock pulses are needed for each shift of the register. The demanding requirements on the

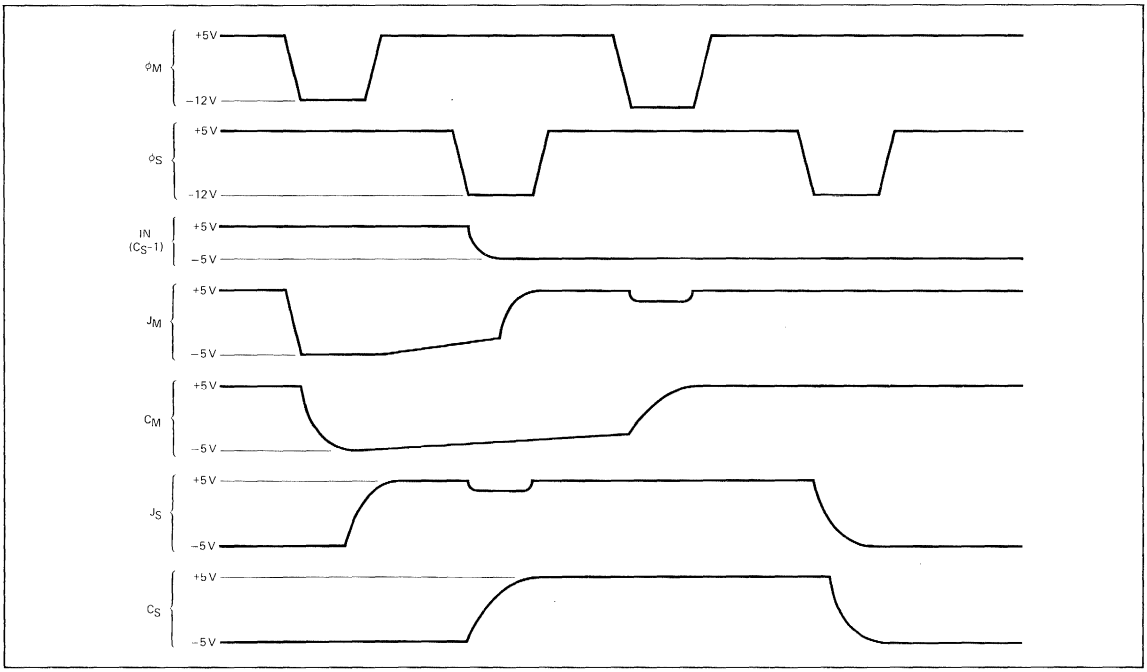
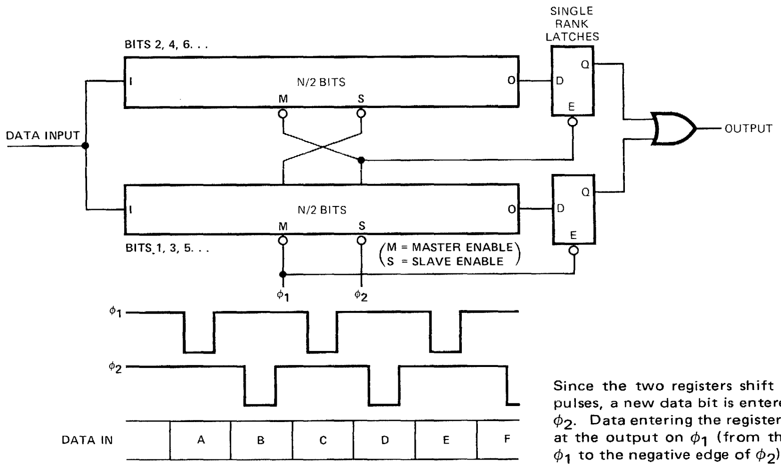


Figure 3. Voltages in Cell of Fig. 2 During Shift of a HIGH and a LOW



Since the two registers shift on opposite clock pulses, a new data bit is entered on both $\phi_1$ and $\phi_2$. Data entering the register on $\phi_1$ will appear at the output on $\phi_1$ (from the negative edge of $\phi_1$ to the negative edge of $\phi_2$).

**Figure 4. Functional Equivalent of Am1402/3/4A and Am2802/3/4**

clock signals (pulse width, voltage levels and speed) limit the data rate through the register to about 2 to 3 MHz generally. It is possible, however, to alter the register configuration slightly to double the data rate through it.

In the Am1402/3/4A and Am2802/3/4 a data shift occurs on every clock pulse rather than on every pair of clock pulses. This is accomplished by multiplexing two registers onto the same input and output lines, as shown in Figure 4. The "odd" numbered bits are stored in one register and the "even" bits in the other. The master clock of one is tied to the slave clock of the other and vice-versa. Clock $\phi 1$ acts as a master clock to the odd register, shifting data on the data input into the master of flip-flop 1. The same clock acts as the slave to the even register, shifting data into the output of the last flip-flop. From the last flip-flop it is fed to a dynamic output multiplexer modeled in Fig. 4 as a pair of ORed latches so that it will appear on the output pin when $\phi 2$ occurs. The output multiplexer acts like an extra 1/2 bit of register, so that the data entering the odd register during $\phi 1$ will leave the multiplexer N pulses later, also during $\phi 1$. Similarly data entering the register during $\phi 2$ will appear on the output during $\phi 2$.

The data rate through the dynamic multiplexed register is twice the frequency of either of the clock inputs $\phi 1$ or $\phi 2$, so for a given clock frequency and using basically the same cell, the data rate is doubled over the normal two-phase register.

## CLOCK TIMING IN THE REGISTERS

There are two constraints on clock timing imposed by the dynamic storage medium. First, the clock must be LOW long enough to fully charge or discharge the storage capacitor. The capacitor is approximately 0.1 pf and it is charged through the series resistance of the transfer gate (about 40kΩ) and either the load transistor or the input transistor. Figure 5 shows the charge on the capacitor as a function of clock LOW time, assuming charging begins when the clock reaches about −10V. The LOW-to-HIGH charging occurs more rapidly because the impedance of the input gate is much less than the impedance of the load transistor. These are nominal curves and a guardband must be allowed for tolerances on the resistors and capacitor.

In between clocks the charge stored on the capacitor will slowly leak away due to PN junction leakage. If too much time elapses between clocks a stored negative level may decay so much that it cannot turn on the next input gate completely, so that during the next clock the stored level will appear to be a HIGH instead of a LOW, resulting in inversion of the data. The maximum time that the clocks can be stopped, or remain in the HIGH state, is a complex function of several parameters. It is principally affected by the temperature of the die inside the package, becoming shorter as the die gets hotter. The three curves in figures 6A, 6B and 6C can be used to determine the nominal maximum clock HIGH time. When the devices are operated in a "burst" mode, then the die temperature is governed by the greater of the two duty cycles. Again a guardband must be added as these curves assume typical device parameters. The calculations used for the curves are shown in the box.

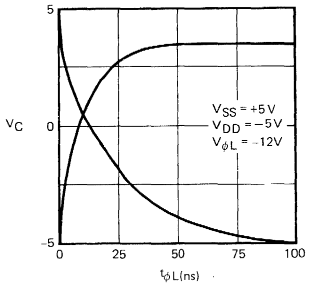


**Figure 5. Charge on Storage Capacitor Versus Clock LOW Time ($V_{\phi L} = <-10V$)**

**Maximum Clock HIGH Time Versus Ambient Temperature for Very Small Duty Cycles**

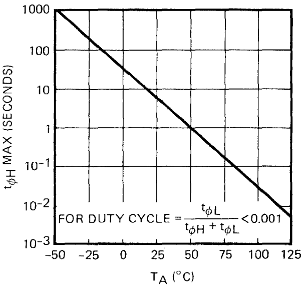


Figure 6A.

**Maximum Clock HIGH Time Versus Clock Duty Cycle (Am1402A/2802)**

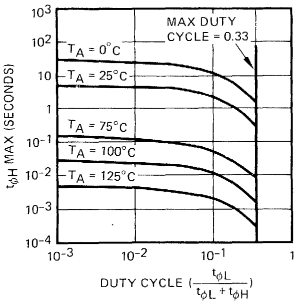


Figure 6B.

**Maximum Clock HIGH Time Versus Clock Duty Cycle (Am1403A, 2803, 1404A, 2804, 2805, 2806)**

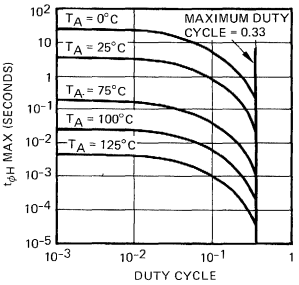


Figure 6C.

**Note: These are theoretical typical curves and should not be used as guaranteed limits.**

## CALCULATION OF MAXIMUM CLOCK HIGH TIME

The maximum clock HIGH time is the time required for the charge on the capacitor to decay from its full value of −10V to a level at which it will be incorrectly read by the next stage input. This level is about 0V so a loss of 5V on the capacitor can be tolerated. The charge on the capacitor escapes through junction leakage, which, for these registers, is about 0.1 pA at 25°C. The leakage current doubles for every 10° rise in junction temperature. The capacitor is about 0.1 pF in value.

$\Delta V = 5V = \frac{it}{C}$, where i is leakage current and C is 0.1 pF

$t_{\phi H} = \frac{0.5}{i_{\text{leak in pA}}}$ where $t_{\phi H}$ = maximum clock HIGH time

$i_{leak} = 0.1 \times 2^k$

where $k = \frac{T_{junc} - 25^\circ C}{10}$ because leakage doubles every 10°

$T_{junc} = T_a + \theta_{ja} \times$ power diss.,

where $\theta_{ja}$ is junction to ambient temperature

$$\theta_{ja} = \begin{Bmatrix} 180^\circ\text{C/Watt for Metal can} \\ 105^\circ\text{C/Watt for 16 lead DIP (1402A/2802)} \end{Bmatrix}$$

power dissipation is directly porportional to clock duty cycle (clock LOW time divided by total clock period).

power = 1.2 x duty cycle ($V_{DD} = -5V, V_{SS} = +5V$)

$i_{leak} = 0.1 \times 2^k$ where $k = \frac{T_a + \theta_{ja}\,(1.2 \times DC) - 25}{10}$

$t_{\phi H}\ \max = \frac{5}{2^k}$

For TO-5 can (Am1403A and 1404A):

$\log (t_{\phi H}) = 1.45 - 0.03T_a - 6.45DC$

For DIP package

$\log (t_{\phi H}) = 1.45 - 0.03T_a - 3.78DC$

Note that for small duty cycles the clock high time depends only on ambient temperature.

## APPLICATIONS OF THE REGISTERS

### 1. Clock Driving

Numerous circuits are available for clock drivers for these registers. The clock HIGH level is 5 volts and the LOW level is −12 volts. The sophistication required in the clock driver depends on how rapidly the registers are to be driven. At low data rates the clock can be generated by simply driving a TTL clock signal into a PNP transistor with a pull down resistor (Figure 7). Of course this is not suitable for driving very large loads, or small loads at high speed, because of the slow fall time on the clock. Most often a monolithic driver such as the MH0026 is adequate. For very high speed operation, up to 10 MHz with the Am2802/3/4, a good hybrid driver or a discrete push-pull driver should be used. The rise and fall times of the clock signal can be controlled with a series resistor in the clock line.

A very important consideration in the clock driver is that the clock signal to the register MUST NEVER EXCEED $V_{SS}$ + 0.3V! If the clock voltage rises higher than this, undesired PNP transistors are formed on the MOS chip, discharging the storage capacitors and possibly permanently damaging the register. To guard against overshoot on the clock lines, a germanium (not silicon) switching diode should be used to clamp the clocks to $V_{SS}$. For long clock traces on PC boards, it may be necessary to consider transmission line effects also, and backmatch the clock lines with a series resistor at the driver.

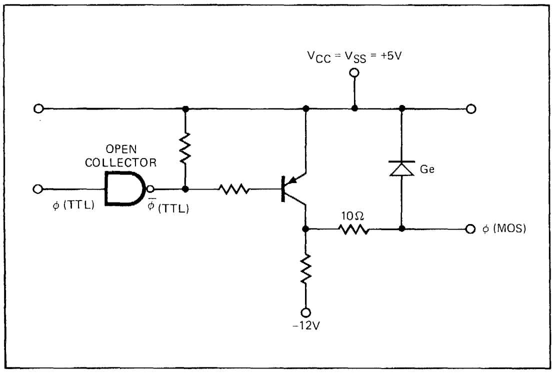


**Figure 7. Simple Clock Driver**

### 2. TTL Interfacing

The inputs and outputs of these registers are, except for the clock lines, compatible with TTL logic levels, although it is necessary to add some resistors. The input threshold is 2 volts below $V_{CC}$, higher than a normal TTL $V_{OH}$, so a pull-up resistor must be used on the TTL output to establish the higher logic level. DTL, which has an internal resistor pull-up, does not require the extra resistor.

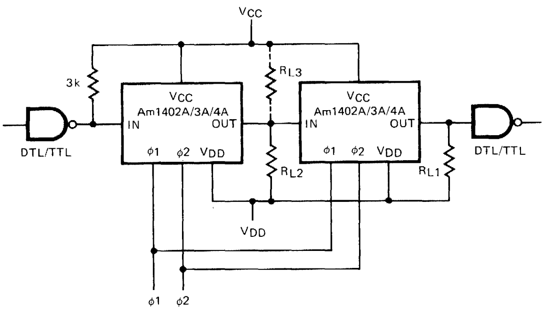
The output of the registers are open drain transistors whose sources are connected to $V_{CC}$. This output transistor has an impedance of about 1,000 ohms, and will establish the HIGH level on the output, but an external pull-down resistor must be connected between the output and $V_{DD}$ to establish the LOW level. This is true whether the output is driving TTL or another MOS input. The pull-down resistor must be small enough to sink 1.6 mA (one TTL load) and maintain 0.4V at the TTL input and large enough that the MOS output can supply current to the resistor and still hold the output at 2.4V. A 3k ohm resistor to –5 volts will suit most applications as shown in Figure 8.

### 3. Register Output to Register Input Interfacing

A frequent application of the Am1402/3/4 and Am2802/3/4 is for serial storage of data which is updated from time to time. In this application several registers are connected end-to-end to provide the required storage capacity and the output of the last register is tied back to the input of the first register through a two-input multiplexer so that either the data output or some new data can be written into the first location. Such a system is illustrated in Figure 9.

When the registers are used in this fashion, some timing constraints must be observed. The output of the register switches state following the falling edge of the clock (either φ1 or φ2). The data remains stable until the falling edge of the next clock. The input accepts data just prior to the rising edge of the clock. When the output of one register is connected to the input of another register (or to its own input via a multiplexer) the data appearing on the output is written into the input during the same clock LOW time. This is different from TTL, in which the output of one register is written into the input of the next on the next clock edge. Because the data is transferred during the clock LOW time, the LOW time must be at least equal to the propagation delay (clock-to-output) plus the set-up time at the input. The sum of these times is substantially longer than the minimum clock pulse width so that when register output is tied to a register input the minimum clock pulse width must be lengthened.

If the registers must be operated at very high speed, then the clock LOW time must be as short as possible, and the requirement that data transfer occur during the LOW time may not be acceptable. In this case a TTL flip-flop can be used between registers to act as a single bit fast interface. The TTL flip-flop is clocked on the falling edge of both φ1 and φ2 so that in each case it stores the data brought to the MOS output on the previous clock. The same falling edge that clocks the TTL flip-flop is the start of the clock LOW period during which the data in the TTL flip-flop is written into the first bit of the next MOS register. While this scheme solves the speed problem, it introduces an extra bit of delay in the register string. See Figure 10.



**$R_L$ Load Resistor Values for Different $V_{DD}$ Supplies**

| | $V_{CC} = 5$ V<br>$V_{DD} = -5$ V | $V_{CC} = 5$ V<br>$V_{DD} = -9$ V |
|---|---|---|
| $R_{L1}$ | 3.0 k | 4.7 k |
| $R_{L2}$ | 4.7 k | 6.2 k |
| $R_{L3}$ | Not required | 3.9 k |

**Figure 8. DTL/TTL to MOS to DTL/TTL Interface**

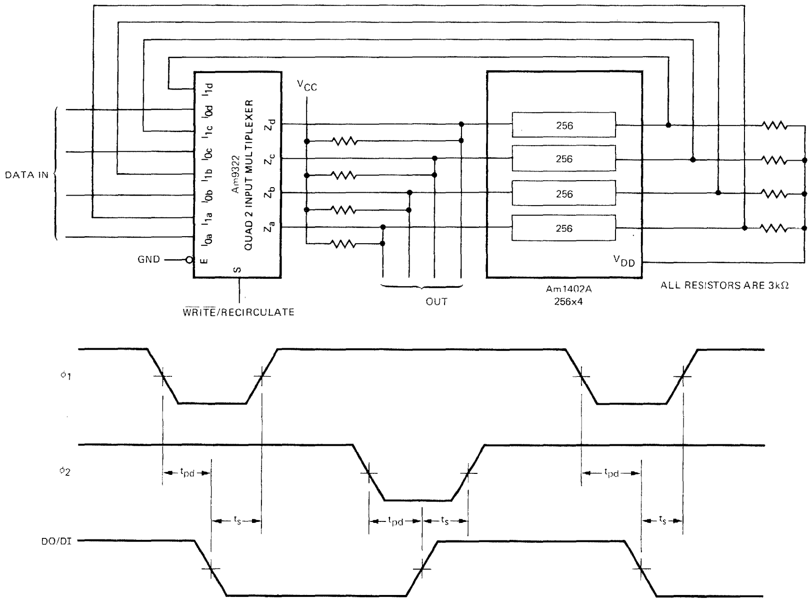

DATA IN
GND
E
S
$I_{0a}$ $I_{1a}$ $I_{0b}$ $I_{1b}$ $I_{0c}$ $I_{1c}$ $I_{0d}$ $I_{1d}$
Am9322
QUAD 2 INPUT MULTIPLEXER
$Z_a$ $Z_b$ $Z_c$ $Z_d$
$V_{CC}$
256
256
256
256
$V_{DD}$
Am1402A
256x4
OUT
WRITE/RECIRCULATE
ALL RESISTORS ARE 3kΩ
$\phi_1$
$\phi_2$
DO/DI
$t_{pd}$
$t_s$

**Figure 9. Recirculating Register. Data-out Changes Following Clock HIGH-to-LOW Transition and is Written Into Input During the Same Clock LOW Time.**

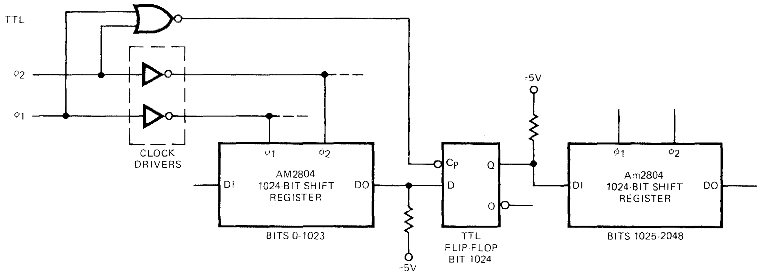

TTL
$\phi_2$
$\phi_1$
CLOCK DRIVERS
$\phi_1$ $\phi_2$
AM2804
1024-BIT SHIFT REGISTER
DI
DO
BITS 0-1023
-5V
+5V
Cp
D
Q
Q
TTL
FLIP-FLOP
BIT 1024
$\phi_1$ $\phi_2$
Am2804
1024-BIT SHIFT REGISTER
DI
DO
BITS 1025-2048

**Figure 10. TTL Flip-Flop Acts as High Speed Interface Between Registers, Allowing Use of Short Clock Pulses, But Also Introduces an Extra Bit of Delay**

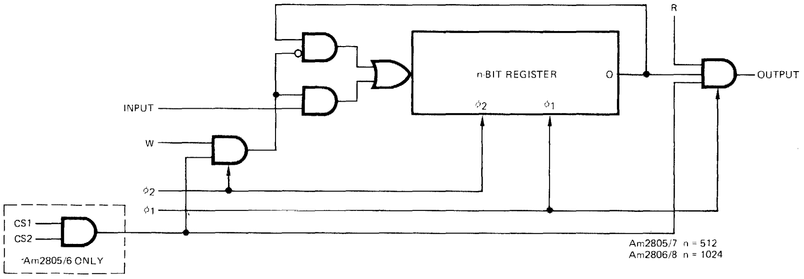

R
n-BIT REGISTER
Q
$\phi_2$ $\phi_1$
OUTPUT
INPUT
W
$\phi_2$
$\phi_1$
CS1
CS2
*Am2805/6 ONLY
Am2805/7 n = 512
Am2806/8 n = 1024

**Figure 11. Functional Diagram of Am2805/6/7/8**

### 4. Register Systems Using the Am2805/6/7/8

The Am2805/6/7/8 512 and 1024-bit registers are not internally multiplexed, but require a pair of clock pulses to product a shift of one bit. These registers also have recirculation logic built-in under control of a write input (W). When the write input is HIGH, data on the input enters the register during $\phi 2$, the master clock. When the write input is LOW, the data at the output of the last bit is written into the first bit instead. The functional diagram is shown in Figure 11. A read control, R, gates the output through an open drain AND gate, so that the outputs of several registers can be ORed together and one register selected. The Am2805 and Am2806 also have a two-input chip select gate; both inputs must be HIGH in order to write into or read from the register. If either chip select input is LOW, the register recirculates.

Note that the write and read gating is activated by the appropriate clock phase. This is done not for dynamic storage purposes but rather to conserve power; no power is dissipated in the input if $\phi 2$ is HIGH and no power is dissipated in the output if $\phi 1$ is HIGH. Dynamic storage does occur in the output gating, with the transfer gate activated when $\phi 1$ is LOW and the read control is HIGH. Data will appear on the output 100 ns after $\phi 1$ goes LOW and read goes HIGH. Data will be stored dynamically in the output stage until the next $\phi 1$ provided that read remains HIGH until the end of the clock LOW time. If read goes LOW before $\phi 1$ goes HIGH the output will turn off.

In large register systems, many Am2805/6/7/8 registers can be connected in parallel and the desired register addressed through the chip select and/or the read and write controls. When many register outputs are connected together the capacitance on the output is increased and care must be taken to insure that the 1,000 ohm output device can fully charge the line.

For higher speed operation, pairs of these registers can be connected in parallel in a multiplexed mode, like the internal configuration in the Am1402/3/4. The inputs and outputs are tied together and the clocks are reversed between the two devices. A flip-flop toggled on each clock pulse can be used to alternate control between the two MOS registers as shown in Figure 12.

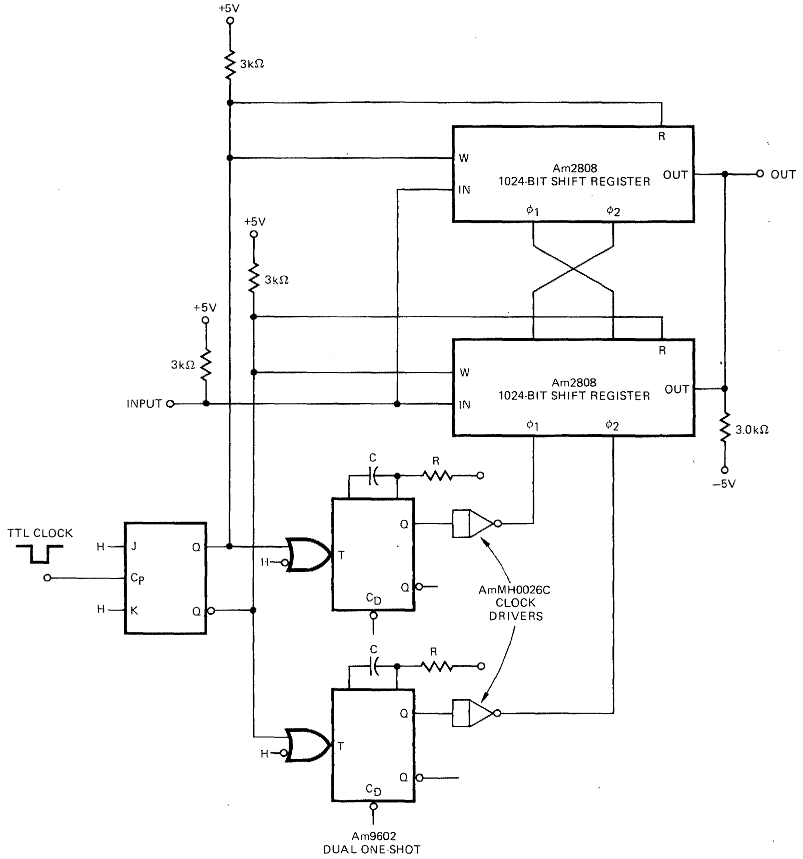


Figure 12. Multiplexed Am2048 Bit Recirculating Register $f_{max}$ = 6 MHz

# APPLICATION OF FIRST-IN FIRST-OUT MEMORIES

**By John Springer, Digital Applications**

The Am3341/2841, Am2812 and Am2813 are asynchronous first-in first-out memories using P-channel silicon gate MOS technology. All use the same fundamental storage mechanism, but are organized differently. The Am3341/2841 contains up to 64 four-bit words; the Am2812 holds up to 32 eight-bit words; the Am2813 holds up to 32 nine-bit words. All devices can easily be expanded to hold either more words or wider words. The Am2841 is functionally identical to the Am3341, but is faster. The logic symbols for these devices are shown in Figure 1.

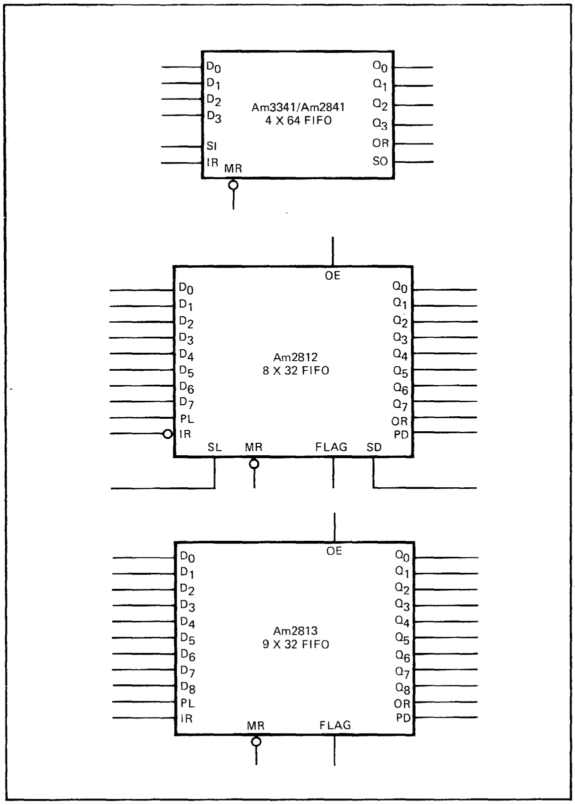


**Figure 1. Logic Symbols**

## THE FUNCTION OF A FIRST-IN FIRST-OUT MEMORY

A first-in first-out memory (FIFO) is a read/write data storage unit that automatically keeps track of the order in which data was entered into the memory, and reads the data out in the same order. It behaves like a shift register whose length is always exactly equal to the number of words stored. The most common application of a FIFO is as a buffer memory between two pieces of digital equipment operating at different speeds. Such an application is illustrated in Figure 2, where machine 1 might be a relatively slow electromechanical input device and machine 2 might be a digital computer (or vice-versa). Data is frequently handled in a configuration like this by having machine 1 generate an interrupt requesting service from machine 2 every time a data word is available. If machine 1 transmits only a single word infrequently then the interrupt-oriented approach is reasonable, but if machine 1 is going to transmit 20 or 30 words, then the interrupt approach is inefficient. As each of the words becomes available, an interrupt must be generated, machine 2 must react, cleaning up its active processing, locate the interrupt, store the new data word, and return to its active processing only to receive another interrupt milliseconds later.

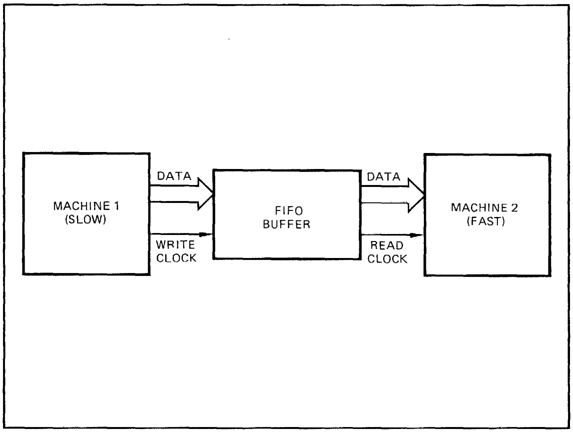


**Figure 2. Asynchronous Interface between Two Digital Machines**

An alternative processing method is cycle stealing on a direct memory access (DMA) channel. In this configuration the system is designed so that machine 1 has direct access to the memory of machine 2. As data becomes available from machine 1, it is inserted into machine two's memory during time periods when machine 2 is not using the memory. This method is fairly efficient, especially for transfer of large blocks of data from a disc or tape, but it also can result in interference with the active processing of machine 2 due to contention for the memory channel.

The most efficient way to handle the interface between these two machines is by using a special memory between the machines to temporarily store the data from machine 1 until machine 2 is ready to accept it. The memory must be large enough to store all the data that machine 1 might generate in-between services by machine 2, and should be able to write the data at the speed of, and under control of, machine 1, while reading the data at the speed of machine 2. An extremely useful feature in such a memory is the ability to perform read and write operations at the two different rates simultaneously and completely independently. This allows machine 1 to write new data into the memory at the same time that machine 2 is reading data from the memory without requiring any kind of synchronization between the two.

## METHODS OF CONSTRUCTING FIFO BUFFERS

There are a number of ways in which FIFO memories can be built. The design becomes trivial if there is no requirement for independent reading and writing. The data can be written into a shift register, for example, which is clocked by machine 1. When a block of data has been written, the register can be shifted until the first data word is available at the output, and then shift control can be handed to machine 2, which shifts the data out as required. This method requires that data transfer occur in blocks only, since once the data has been shifted to the output, a new word cannot be written until the last block has been completely read.

A somewhat more flexible FIFO can be built using a random access memory with counters used to generate the read and write addresses. A multiplexer is used to select the appropriate address counter for a read or write, and the counter is incremented at the end of the cycle, so that the next read or write will occur at the next counter address. Since the location of the next read and write are held in independent counters, reading and writing can be randomly intermixed. However, using an ordinary RAM, only one operation can be performed during a given cycle, since only one address can be selected at a time.

If the RAM is very fast relative to the machines using it, then the control logic can be designed to receive read and write requests independently and to execute them so quickly that the FIFO buffers appear to operate completely asynchronously. In the general case, this means the RAM cycle time must be less than half the cycle time of machines 1 or 2. This is necessary so that the buffer can perform alternate read and write operations at the maximum speed of both machines. The control logic to do this is fairly complex and requires an independent clock running at more than twice the frequency of machine 1 or 2.

The problem of handling read and write operations simultaneously is alleviated if a 2-port RAM is used. Such a device (e.g., the Am9338) has two independent sets of address inputs, one for reading and one for writing, so no synchronizing of read and write requests need occur. Unfortunately, two port RAMs are limited to small numbers of bits, and, therefore, are fairly expensive to use in a FIFO of reasonable size.

The Am3341/2841, Am2812 and Am2813 are totally integrated solutions to the problem of asynchronous FIFOs. A special unique control system is integrated into the device to make possible completely independent reading and writing. Because the control and data storage are intimately mixed on one LSI chip, a very efficient, cost-effective FIFO can be constructed. The three devices, all of which use the same basic control scheme, are organized into three different configurations to provide optimum flexibility for all applications.

## STORAGE AND CONTROL IN THE Am3341/2841, Am2812 AND Am2813

The Am3341/2841, 64 x 4 FIFO will be used to explain the storage technique. A similar scheme is used in the Am2812 32 x 8 FIFO and Am2813 32 x 9 FIFO. A logic block diagram of the Am3341 is shown in Figure 3. Data words are stored in 64 four-bit registers, connected so the output of one feeds the input of the next. Note that if all 64 registers were clocked together, the device would look like a quad 64-bit shift register. FIFO operation is performed by clocking each register independently so that data can be selectively shifted through the registers. To shift or not to shift: that is the decision which must be made independently by each of the 64 registers. The decision is made by examining a control flip-flop associated with each register to determine if that register contains valid data or not.

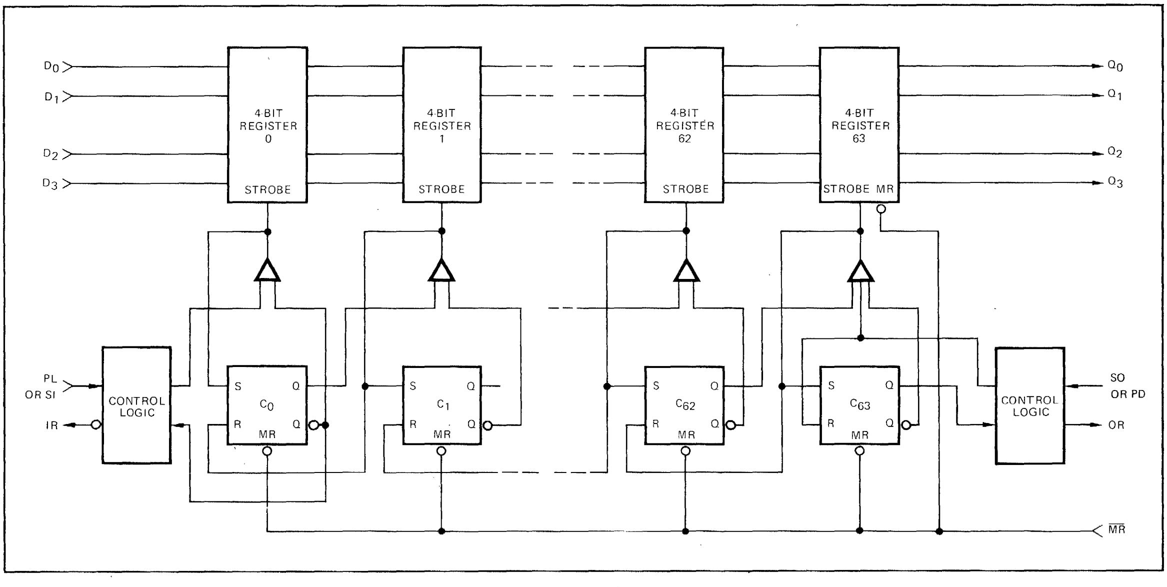


Figure 3

Initially, the FIFO is reset and there is no data anywhere in it. The control flip-flops are all reset to "0." A write command causes a 4-bit data word to be entered into the first register and sets the control flip-flop for that register, indicating valid data is present. The control flip-flop for the second register is a "0" and this causes it to continually examine the control flip-flop for the first register, looking for a "1." When the data is written into the first register, the second register sees the "1," and a clock is generated to it, copying the data from the first register into the second, setting the control flip-flop for the second register, and clearing the control flip-flop for the first register. In exactly the same fashion, the third register copies the data from the second, and the fourth from the third until finally the data ends up in the last location. At this point all 64 registers contain the same data, but only the last control flip-flop contains a "1," the others all having been reset as the data was copied into the next register.

As soon as the data moves from the first register to the second, the control flip-flop for the first register is cleared. A new data word can then be written into the first register. The first control bit is brought out as "input ready" (IR), and data can be entered anytime it is HIGH. When the data has been accepted, IR goes LOW (a "1" in the control bit) and when the data moves to the second register, IR goes HIGH again. The new data falls through the registers as long as there are "0s" in the corresponding control flip-flops. Eventually it reaches the register immediately behind a register already containing data. Since the control bit for that register is already a "1," the data is not moved any further and remains stacked up behind the existing data. A read command on the output causes the last control flip-flop to be cleared, creating a new empty location. The next to the last word is copied into the last word and the hole in the control register moves back toward the input as the data words move down one place. This process can continue until all data has been shifted out of the memory. When the last word has been read the external signal output ready (OR) remains LOW, indicating no more data is available.

This scheme allows the reading and writing of data to occur completely independently and even simultaneously. Data can be written into the device as rapidly as the device is capable of moving it away from the first register; it can be read at the same rate. The only constraint imposed by this scheme is that a certain amount of time is required for the first data word to propagate to the end of the register. This time is referred to as the "ripple-through" time and is the internal shift time multiplied by the number of bits from input to output.

## CONTROL SIGNALS TO THE Am3341/2841 AND Am2813

There are four signals used with the Am3341/2841 and Am2813 to control the reading and writing of data. These are parallel load (PL, or SI on 3341), input ready (IR), parallel dump (PD or SO on 3341) and output ready (OR).

The two outputs, IR and OR, are derived from the state of the first and last control flip-flops, respectively, and are used to indicate the presence or absence of data at the input and output of the FIFO. When IR is LOW (that is, input not ready) then there is data residing in the first data register. New data may not be entered until this data has moved to the second register, indicated by IR going HIGH. The OR signal goes HIGH whenever valid data is present on the FIFO output. Whenever a shift-out command is received, OR goes LOW while the data is being changed. If there is no more data, OR stays LOW, indicating the memory is empty. Otherwise OR returns HIGH as soon as the new data is on the outputs. Data is entered into the FIFO by a LOW-to-HIGH transition on shift-in (PL), while IR is HIGH. The fact that both these signals are HIGH causes a strobe to the first data register to be generated, loading the data on the data inputs into register and setting the first control flip-flop. When the control flip-flop is set, IR goes LOW, indicating the data has been accepted. The input data can be changed after IR has gone LOW. When SI is then brought LOW, the data is transferred to the next register (unless there is already data there) and IR goes back HIGH, indicating that the input is ready to receive more data. If the memory is full, then the data in the first register will not move to the second, and IR will stay LOW. Once data moves into the second register, it falls spontaneously through the FIFO until it stacks up behind data already present.

Data in the last FIFO location is presented on the data outputs. While data is there, OR is HIGH. The next data word is obtained by applying a LOW-to-HIGH transition on shift-out (SO). This results in OR going LOW. The data does not actually change until SO is brought LOW again. The new data, if any, will be brought to the output and, after the data is stable, OR will go HIGH again. If the memory is empty, OR will remain LOW until a new word falls through from the input. Note that anytime OR is HIGH, there is good, stable data on the outputs.

## MASTER-RESET

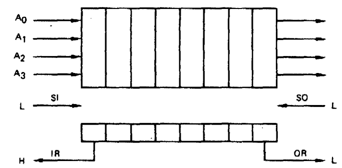
The master reset pin ($\overline{\text{MR}}$) is used to clear all data from the FIFO. When it goes LOW, all the control flip-flops are cleared and the output buffer is cleared. IR will be forced HIGH during this time. When the $\overline{\text{MR}}$ signal is removed the FIFO is ready to accept new data. Note that if SI is held HIGH as the master reset ends, then both SI and IR will be HIGH, resulting in immediate entry of the data on the data inputs into the FIFO. If this is not desired, then SI should be held LOW during the master reset and until new data is ready to be entered.

## EXPANSION METHODS USING THE Am3341/2841

The four control signals on the Am3341 have been designed so that devices can be directly connected end-to-end, as in Fig. 6, and can thereby control each other. When data appears at the output of the first device OR goes HIGH. This causes an SI command to the second device which in turn causes IR to go LOW. Since IR is connected to SO, this causes a shift-out at the first device, driving OR LOW until new data is available, and the process repeats. Lengthening of the FIFO stack requires only this simple interconnection.

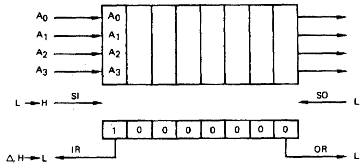
To make a wider FIFO devices are simply operated in parallel. Since each device is autonomous there need be no interconnection between paralleled devices, except that all the shift-ins at the front are connected together and all the shift outs at the end are connected together. Data then ripples independently through each row of FIFOs.

1


A0
A1
A2
A3
SI
SO
IR
OR
L
L
H
L

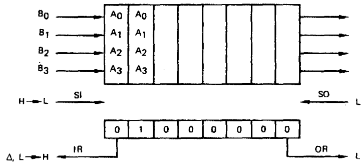
**INITIAL CONDITION**
FIFO empty, SI LOW IR HIGH, word "A" on inputs.

2


SI
SO
IR
OR
L→H
L
Δ, H→L
L

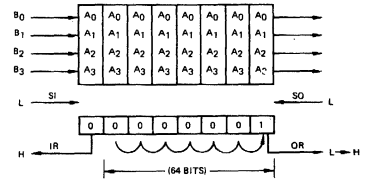
Write input into first stage by raising SI. (Δ = delay) IR goes LOW indicating data has been entered.

3


SI
SO
IR
OR
H→L
L
Δ, L→H
L

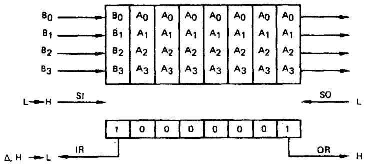
Release data into FIFO by lowering SI. After delay, data moves to second location, and IR goes HIGH indicating input available for new data word.

4


SI
SO
IR
OR
L
L
H
L→H
(64 BITS)

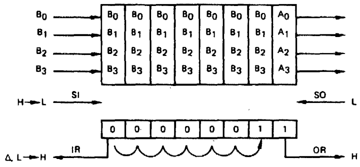
Data spontaneously ripple through registers to end of FIFO, causing OR to go HIGH. The time required for data to fall completely through the FIFO is the "Ripple-through Time".

5


SI
SO
IR
OR
L→H
L
Δ, H→L
H

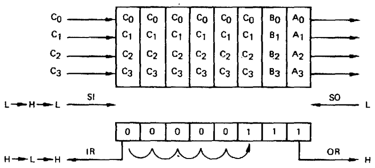
Word "B" written into FIFO

6


SI
SO
IR
OR
H→L
L
Δ, L→H
H

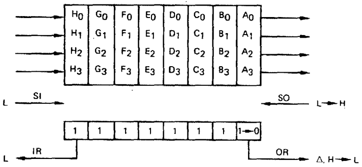
SI goes LOW allowing word "B" to fall through.

7


SI
SO
IR
OR
L→H→L
L
H→L→H
H

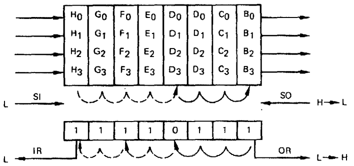
Word "C" written in same manner, and so on. When buffer is full, all control bits are 1's and IR stays LOW.

8


SI
SO
IR
OR
L
L→H
L
Δ, H→L

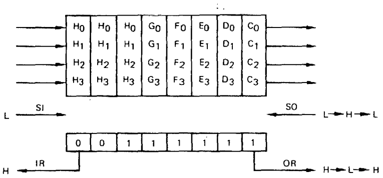
**FIRST READ OPERATION**
SO goes HIGH, indicating "Ready to Read". OR then goes LOW indicating "Data Read".

9


SI
SO
IR
OR
L
H→L
L
L→H

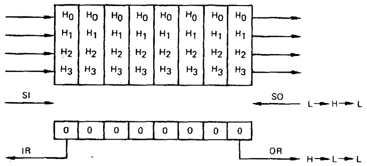
When SO goes LOW, the "0" in the last control bit bubbles toward the memory input. OR goes HIGH as the new word arrives at the output. IR goes HIGH when "0" reaches input.

10


SI
SO
IR
OR
L
L→H→L
H
H→L→H

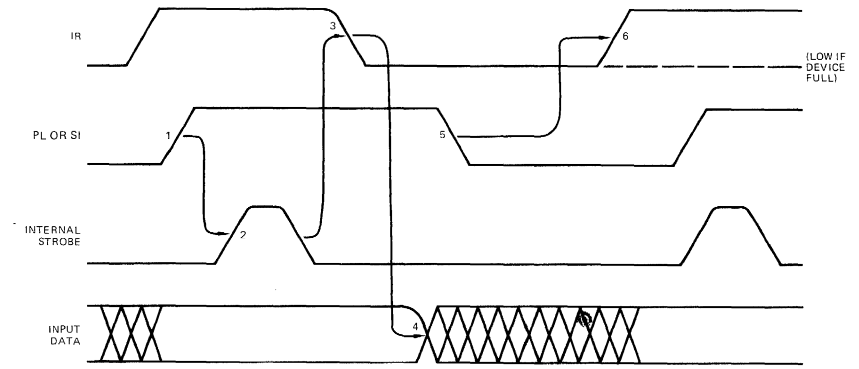
Read word "B" out, word "C" moves to output, and so on.

11


SI
SO
IR
OR
L→H→L
H→L→L

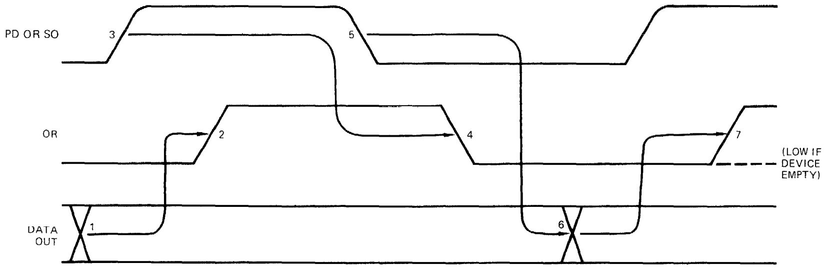
Read word "H". OR stays LOW because FIFO is empty. Word "H" remains in output until new word falls through.

Figure 4


IR
3
6
(LOW IF DEVICE FULL)
PL OR SI
1
5
INTERNAL STROBE
2
INPUT DATA
4

**INPUT TIMING SEQUENCE, Am3341/2841 AND Am2813**

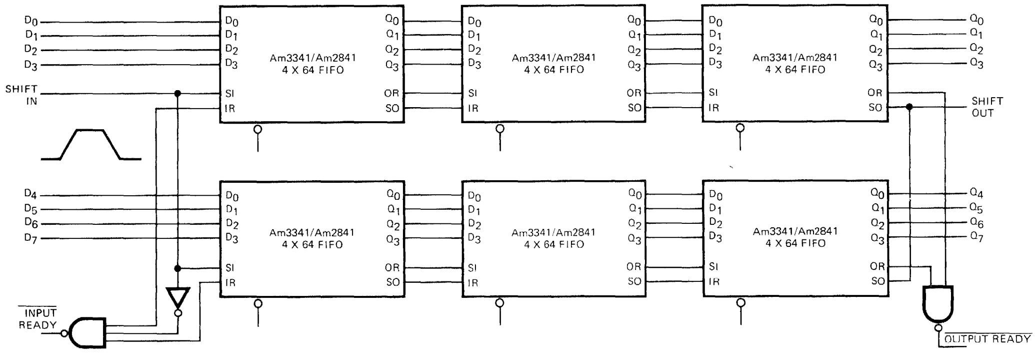
SI is brought HIGH (1) causing internal strobe (2) which loads data. When data has been loaded, IR goes LOW (3) indicating data can be changed (4). SI may then be brought LOW (5) causing IR to return HIGH (6).


PD OR SO
3
5
OR
2
4
7
(LOW IF DEVICE EMPTY)
DATA OUT
1
6

**OUTPUT TIMING SEQUENCE, Am3341/2841 AND Am2813**

Data out changes (1); then OR goes HIGH (2). When SO goes HIGH (3), OR goes LOW (4) indicating data is about to change. After SO goes LOW (5) the data actually changes (6) and after it is stable, OR goes HIGH again (7).

Figure 5


D0
D1
D2
D3
Q0
Q1
Q2
Q3
Am3341/Am2841
4 X 64 FIFO
SI
IR
OR
SO
SHIFT IN
SHIFT OUT
D4
D5
D6
D7
Q4
Q5
Q6
Q7
INPUT READY
OUTPUT READY

The composite input ready indicates both devices are ready to receive data. The shift in pulse must be wide enough for all devices to load data under worst case conditions.

Figure 6. 8 x 192 FIFO Buffer Using Am3341/2841

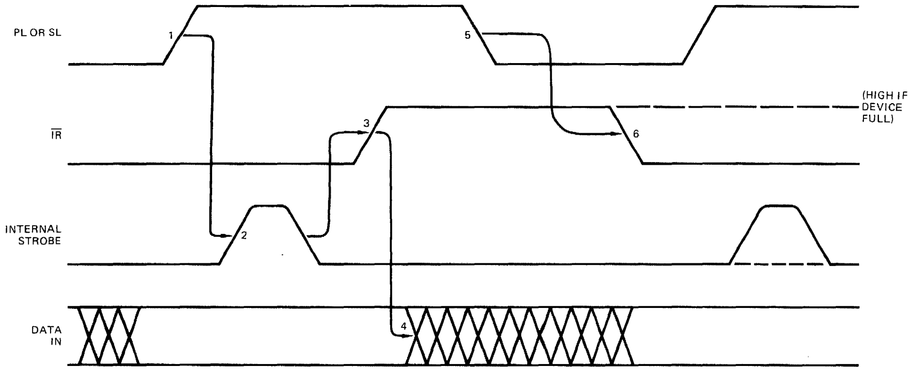
## CONTROL SIGNALS ON THE Am2812

The Am2812 is controlled exactly like the Am3341 and Am2813, except that the input ready signal is inverted. Internally operation is like the Am3341/2841. The control signals are slightly different, however, and there are some additional features. There is a parallel load (PL) input, used to load an 8-bit word onto the first stage of the FIFO, and an input ready output ($\overline{IR}$) which indicates that the FIFO is ready to receive a new data word. At the output, there is a dump command (PD), used to bring the next data word to the outputs, and an output ready signal (OR) which indicates that good data is available on the data outputs.

Data is loaded into the first FIFO location by a LOW-to-HIGH transition on PL when $\overline{IR}$ is LOW. (It is the coincidence of PL HIGH and IR LOW which results in the internal load strobe.) When the data has been entered the first control flip-flop sets, causing $\overline{IR}$ to go HIGH. When PL goes LOW again, the data in the front of the FIFO begins falling through the stack toward the output, and $\overline{IR}$ goes LOW as soon as it has moved to the second register. If the FIFO was filled to capacity when the data was loaded, then $\overline{IR}$ will stay HIGH; new data cannot be entered, and any additional shift in command will be ignored until $\overline{IR}$ goes LOW after some data has been removed from the FIFO.

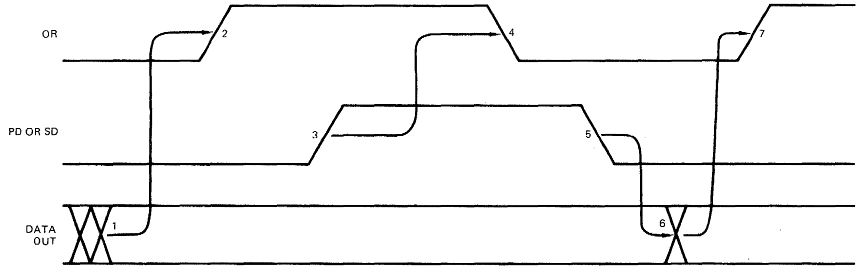
Data entered into the FIFO falls through the registers until it reaches either the output or another data word. When a data word is present at the output, OR (output ready) will be HIGH.

The next data word is shifted onto the outputs by a pulse on parallel dump (PD). When PD goes HIGH, the OR signal goes LOW, indicating that output data is about to be changed. When PD then goes LOW, the output data changes with the word behind the outputs moving onto the outputs. When the new output data has stabilized, OR will go HIGH indicating that good data is once again available on the FIFO outputs. If the PD pulse emptied the FIFO, then the OR signal will remain LOW and the last word read will remain on the outputs until a new data word falls through from the front of the FIFO.



**Am2812 INPUT TIMING**

When data is steady, PL or SL is brought HIGH (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes HIGH (3) and data may be changed (4). $\overline{IR}$ remains HIGH until PL is brought LOW (5); then $\overline{IR}$ goes LOW (6) indicating new data may be entered.



**Am2812 OUTPUT TIMING**

When data out is steady (1), OR goes HIGH (2). When PD or SD goes HIGH (3), OR goes LOW (4). When PD or SD goes LOW again (5), the output data changes (6) and OR returns HIGH (7).

Figure 7.

## MASTER RESET

A direct clear signal can be applied to the FIFO by a LOW logic level on the $\overline{MR}$ input. This will clear all the internal control register bits and will clear the data from the outputs. $\overline{IR}$ will go LOW indicating the FIFO is ready to receive new data. If the PL input is held HIGH when the $\overline{MR}$ returns to a HIGH state, then an internal input strobe will be generated, and whatever data is on the inputs will be loaded into the FIFO. If this is not desired then PL should be held LOW at the end of the master reset. The master reset will cause OR to go LOW and remain LOW until new data falls through from the input.

## FLAG

A flag output is available on the Am2812 and Am2813 to indicate whether the FIFO is more or less than half full. The flag signal is generated by summing the "1s" in the control flip-flops, and therefore is not affected by the movement of data through the register. The flag signal goes HIGH when the 15th ±1 (i.e., the 14th, 15th, or 16th) word is loaded into the FIFO. It will remain HIGH until there are less than 15 ±1 words in the memory. It is always HIGH if there are more than 16 words in the FIFO.

## OUTPUT ENABLE

The Am2812 and Am2813 data outputs are 3-state signals. When OE is HIGH, they will be in either a HIGH or LOW state; if OE is LOW, they will go to a high-impedance OFF state. Outputs of several FIFO buffers can then be tied together onto a bus, and one of the buffers can be selected to drive the bus. When OE is LOW, the dump function (both SD and PD) is disabled.

## SERIAL INPUT AND OUTPUT (Am2812 ONLY)

The Am2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the SL clock input and applying data to $D_0$ input. Inputs $D_1$ - $D_7$ must be grounded. The SL signal operates just like the PL input, causing $\overline{\text{IR}}$ to go HIGH and LOW as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they had been loaded in parallel.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the $O_7$ output. OR moves HIGH and LOW with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and a new 8-bit word is brought to the output.

When one of the serial clocks is used, the corresponding parallel signal (PL or PD) should be grounded.

## EXPANSION OF THE Am2812 AND Am2813

The input and output shift and ready signals have been designed so FIFOs can be directly connected end-to-end to make a longer (i.e., more words) buffer memory, as shown in the applications in Figures 10 and 11. Wider words can be stored by using independent FIFO stacks, side by side, like the Am3341s in Figure 6. When FIFOs are connected end to end, the total number of words that can be stored is (31n+1) not 32n. This is due to the fact that when an SI command loads the 32nd word into a FIFO, the $\overline{\text{IR}}$ output stays HIGH, and no PD pulse is applied to the adjacent up-stream FIFO. As a result the word just written into the FIFO is duplicated at the output of the previous FIFO. When at least one word is removed from the downstream FIFO, the $\overline{\text{IR}}$ signal goes LOW, causing the duplicated word to be dumped from the up-stream device.

## SYSTEM INTERFACING

Normally the input and output of a stack of FIFOs are interfaced with TTL logic. A special interface circuit is used internally on the inputs of the AMD family of FIFOs to provide complete electrical compatibility with TTL outputs; no external components need be used. The circuit works by using an MOS transistor inside the chip as a pull-up resistor in the HIGH state. When the voltage applied to the input is LOW, the internal resistor is disabled and presents no loading to the TTL output. THE V-I characteristic of the input is shown in Figure 8.

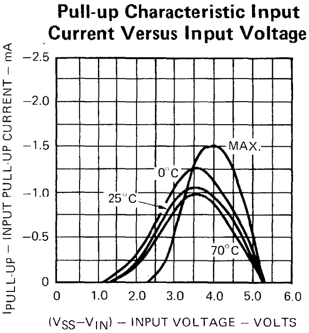
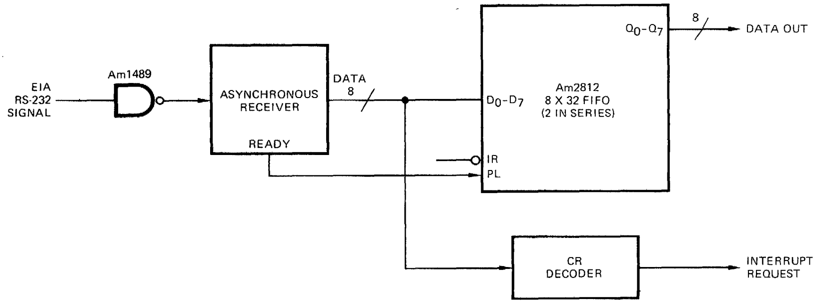


**Figure 8. Input Voltage Current Characteristics**

The logical interface between the FIFO inputs and the rest of the system must detect that all device inputs are ready, and then supply a shift in command when new data is available. Normally this is rather simple, since most data transfer interfaces contain a data strobe control and a not ready signal. Some caution must be exercised when a composite Input Ready signal for a parallel stack of FIFOs is formed. The inputs to the stack are ready to receive data only when PL is LOW and all input ready signals are HIGH (LOW on the Am2812. Data can be removed from the inputs to the stack only when all input ready signals have gone LOW (HIGH on the Am2812). The easiest way to handle this situation is to detect only that all inputs are ready to receive data, and then insure that data remains as long as is required by the worst case specification, rather than actually detecting that the data has been loaded into all devices.

The data on the data inputs must be held steady for about a 400ns period following the SI or PL LOW-to-HIGH transition. The internally generated data strobe will occur sometime during this period. The strobe will not occur, however, until at least 25ns after the SI transition. The rising SI signal may therefore also be a clock to a TTL register feeding the data inputs, as there is sufficient time available for the $t_{pd}$ of the register. However, it is preferable to change the input data on the falling edge of SI for additional timing margin in the system.

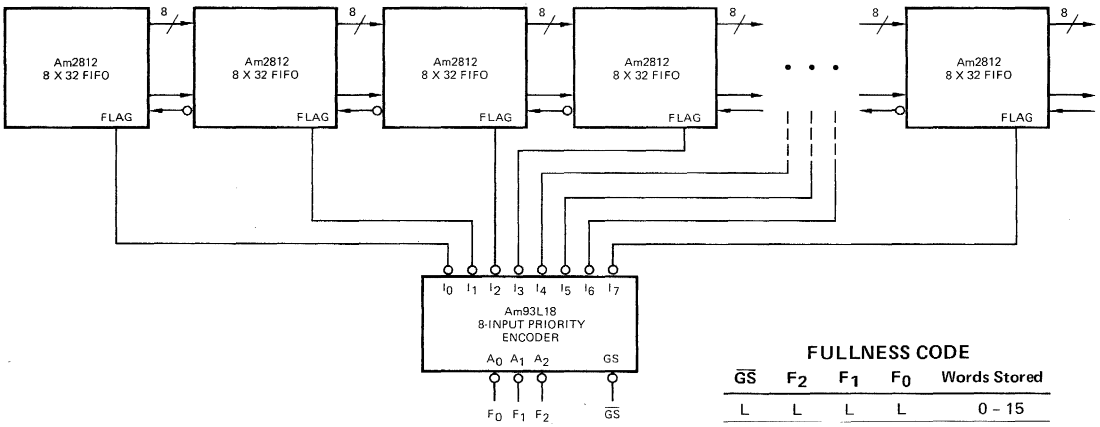
At the output of the FIFO, the logic must detect that all outputs are ready, and then supply the dump command when the data has been received by the system. Again, these two kinds of signals are normally available in systems.


EIA
RS-232
SIGNAL
Am1489
ASYNCHRONOUS
RECEIVER
READY
DATA
8
$Q_0$-$Q_7$
8
DATA OUT
$D_0$-$D_7$
Am2812
8 X 32 FIFO
(2 IN SERIES)
IR
PL
CR
DECODER
INTERRUPT
REQUEST

## CHARACTER BUFFER FOR TERMINAL

RS-232 data from the data set is converted to parallel 8-bit ASCII characters by an asynchronous receiver chip. When each character is received it is placed in the FIFO buffer. The characters (up to 64) are stored until a carriage return character is detected. An interrupt is then generated to the processor, informing it that a data line is ready.

**Figure 9. Character Buffer for Terminal.**

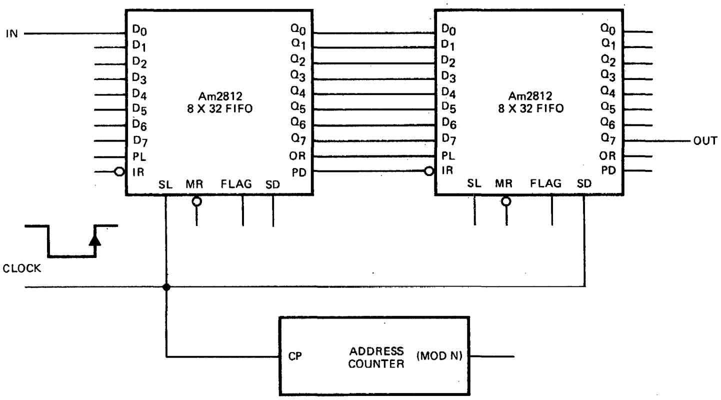

Am2812
8 X 32 FIFO
FLAG
8
Am2812
8 X 32 FIFO
FLAG
8
Am2812
8 X 32 FIFO
FLAG
8
Am2812
8 X 32 FIFO
FLAG
8
8
Am2812
8 X 32 FIFO
FLAG
8
$I_0$ $I_1$ $I_2$ $I_3$ $I_4$ $I_5$ $I_6$ $I_7$
Am93L18
8-INPUT PRIORITY
ENCODER
$A_0$ $A_1$ $A_2$
GS
$F_0$ $F_1$ $F_2$
$\overline{GS}$

**FULLNESS CODE**

| $\overline{GS}$ | $F_2$ | $F_1$ | $F_0$ | Words Stored |
|---|---|---|---|---|
| L | L | L | L | 0 - 15 |
| L | L | L | H | 13 - 47 |
| L | L | H | L | 45 - 78 |
| L | L | H | H | 76 - 109 |
| L | H | L | L | 107 - 140 |
| L | H | L | H | 138 - 171 |
| L | H | H | L | 169 - 202 |
| L | H | H | H | 200 - 233 |
| H | H | H | H | 231 - 249 |

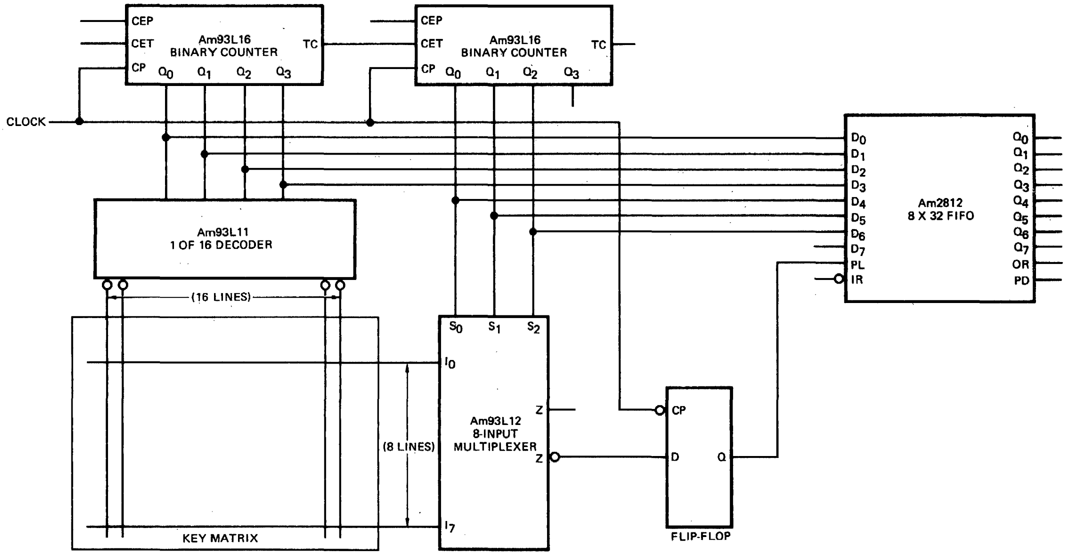
The Fullness Flags from Am2812 or Am2813 FIFOs can be encoded by an Am93L18 8-input priority encoder. The output code $F_0$-$F_2$ indicates the weight of the highest priority input which is LOW. GS is group signal; it is HIGH if all the inputs are HIGH. For the Am2813, the words stored starting with 47 will be one more than is indicated in the table.

**Figure 10**


IN
D0
D1
D2
D3
D4
D5
D6
D7
PL
IR
Am2812
8 X 32 FIFO
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
OR
PD
SL
MR
FLAG
SD
OUT
CLOCK
CP
ADDRESS COUNTER
(MOD N)

The serial I/O of the Am2812 is used, with data clocked into the $D_0$ input by $CP_{IN}$ and clocked out of the $Q_7$ output by $CP_{OUT}$. Since data stacks up at the output end, the shift register appears to have a length corresponding to the number of words stored. For a 327-bit shift register, for example, it should be initialized with 327 0's. Data may then be entered or recirculated and the MOD 327 counter can be used to indicate the "address" of the current bit. A parallel transfer between devices is used.

Figure 11. N-Bit Shift Register, N = 8 to 512.


CEP
CET
Am93L16
BINARY COUNTER
TC
CP
Q0
Q1
Q2
Q3
CLOCK
Am93L11
1 OF 16 DECODER
(16 LINES)
KEY MATRIX
(8 LINES)
S0
S1
S2
I0
I7
Z
Am93L12
8-INPUT
MULTIPLEXER
Z
CP
D
Q
FLIP-FLOP
D0
D1
D2
D3
D4
D5
D6
D7
PL
IR
Am2812
8 X 32 FIFO
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
OR
PD

The combination of the counters and multiplexers act as a key encoder on the key matrix. A closure will produce a HIGH on the multiplexer output $\overline{Z}$ when the appropriate switch is scanned. The HIGH is stored in a flip-flop to provide a shift-in command to the FIFO one clock period wide. The flip-flop is clocked on the falling clock edge to insure the count is stable during the shift-in pulse.

Figure 12. Storage of Switch or Key Closures.

# HOW TO USE
# 1702A MOS PROMs RELIABLY

This paper describes the methods used by Pro-Log Corporation to screen, program and erase 1702A MOS PROMs. It also describes the theoretical basis for these methods. Pro-Log has shipped over 3,000 programmed 1702A PROMs in its operating equipment during the last three years and has had only two PROMs fail in the field during that time.

The 1702A MOS PROM is a 2048 bit read only memory device, which can repeatedly be erased under ultra-violet light and reprogrammed. It was first developed by Intel Corporation several years ago and is now the industry standard for this class of device. The 1702A now has several sources and other MOS PROMs (notably National's 5204) use the same technology.

## THEORY OF THE MOS PROM MEMORY CELL

To make clear the basis of Pro-Log's method for handling the PROM, it is necessary to describe how the PROM functions. The explanation is partially derived from Reference 1.

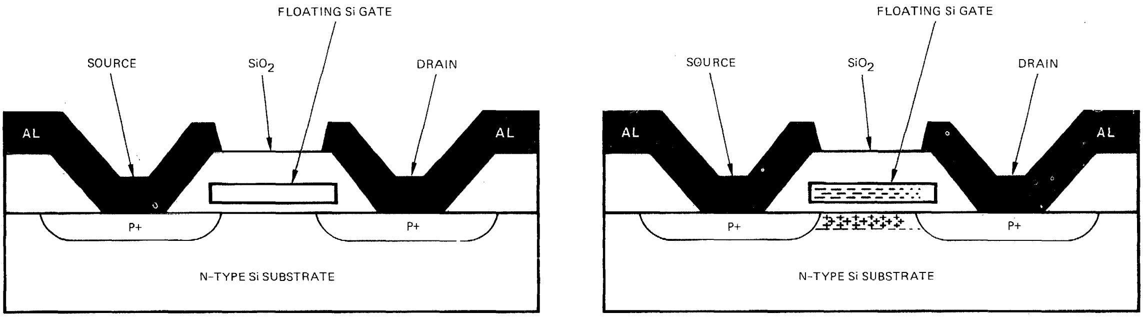
Each of the 2048 memory cells in the 1702A PROM is a field effect transistor in which the gate is isolated in a silicon dioxide substrate. There is no lead to the gate (Fig. 1). When the cell is unprogrammed or erased (Fig. 1a) there is no charge on the gate and the source to drain resistance, $R_{SD}$, is extremely high. After a cell is programmed (Fig. 1b) there is a charge, Q, on the gate which produces a P-channel between source and drain. The source to drain resistance $R_{SD}$ is relatively low, its value being inversely proportional to the value of Q.

To program a cell, a source to drain voltage in excess of about 30 volts is applied for a period of time. This voltage causes an avalanche breakdown in the back biased junction between the drain and the substrate material. Electrons are swept across the avalanched junction and some receive enough energy to penetrate the $SiO_2$ insulation and collect on the buried gate. A negative charge, Q, builds up on the gate. The rate the charge builds up and the maximum charge which can be accumulated increases with avalanche voltage. The higher the avalanche voltage, the higher the initial energy of the electrons penetrating the insulation. Figure 2 shows the typical charging curves for three such memory cells in a 1702A PROM. Cell A has a relatively high avalanche voltage so that it charges rapidly and ultimately reaches the highest level of gate charge. Cell A has to have fairly efficient addressing circuitry since the avalanche current is also limited by the characteristics of the selection circuitry in series with the cell. Cell C on the other hand, is typical for a cell with both a low avalanche voltage and selection circuitry with relatively high impedance. What is important to the user is that he has no control over the avalanche voltage and the charging curve for any given cell. He simply applies a programming voltage of around 47 volts external to the PROM. The characteristics of the PROM control how a particular bit charges.

## THE MEMORY CELL IN THE SYSTEM

The 1702A has 2048 memory cells organized as 256 words, each word having eight bits. When the PROM is addressed in the READ mode, eight cells are selected and readout together as an eight-bit word.

A simplified equivalent circuit for a typical cell within the PROM is shown in Figure 3. The memory cell is the resistance $R_{SD}$, and its address selection circuitry is represented by $R_{XY}$ (addressing is actually a series/shunt arrangement). Bit sensing involves a preamp whose input is connected to the bit in question, along with 15 other bits. The output of that preamp and 15 other preamps are connected to an output amplifier. This arrangement connects 256 bits to a single output amplifier. A particular cell is selected for readout by lowering the impedance $R_{XY}$ to a few ohms. Then the output voltage, $V_{OUT}$, becomes a function of $R_{SD}$. Each preamplifier has an



a) Cell in the unprogrammed or erased state. Gate has no charge and source to drain resistance. $R_{SD}$ is extremely high.

b) Cell in the programmed state. A negative charge, Q, on the gate induces a P channel between source and drain. $R_{SD}$ is low.

**Figure 1. The memory cell used in the 1702A PROM. The cell is an FET whose gate has no lead. Source to drain resistance is a function of gate charge.**

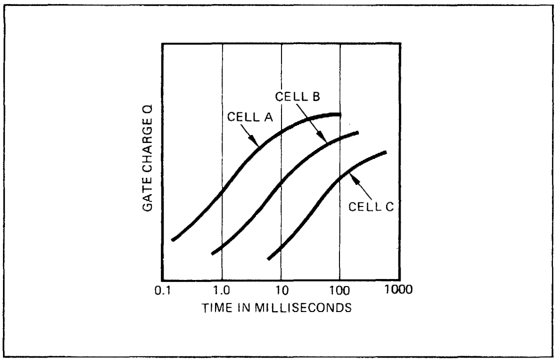


Figure 2. Gate charge Q as a function of programming time for different cells in a 1702A PROM.

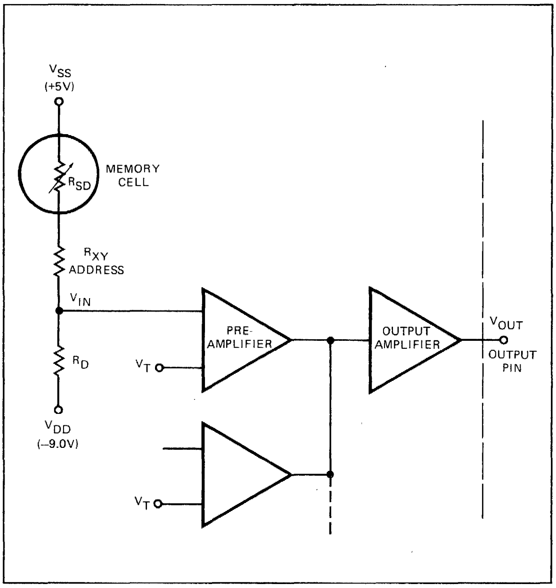


Figure 3. Simplified equivalent circuit for a selected cell in the read mode.

effective threshold voltage, $V_T$. When $V_{IN}$ is more negative than $V_T$ the output voltage $V_{OUT}$ is negative and the bits read out as unprogrammed. When $V_{IN}$ is more positive than $V_T$ the output voltage goes positive and the bit reads out as programmed.

The user has a problem determining if the bit is reliably programmed or erased because he can only observe $V_{OUT}$. The value of $R_{SD}$ may be such that slight system changes can cause $V_{IN}$ to go back and forth across the threshold voltage $V_T$ and cause $V_{OUT}$ to change. Reliable programming and erasing require indirect measuring techniques based on the theoretical characteristics of the device to insure that $R_{SD}$ is safely above or below its threshold voltage.

Let us call $R_T$ the value of $R_{SD}$, which causes $V_{IN} = V_T$. The bit gate charge required to produce $R_T$ is $Q_T$, the threshold charge. It is a function of $V_T$ for the particular preamp, power supply voltages, gain characteristics of the preamplifier, and $R_{XY}$. These variables in turn are functions of temperature, power supply voltage, incident light and other factors. Thus it is that the value of $Q_T$ varies from bit to bit within a PROM and for the same bit position from PROM to PROM.

## PROGRAMMING THE PROM RELIABILITY

Figure 4 shows the programming curves for the hypothetical cells A and C in a PROM, along with their nominal threshold charges $Q_{TA}$ and $Q_{TC}$ at 25°C ambient and minimum power supply voltage. For Cell A to program from the erased state to the threshold requires the programming time $t_A$, which is about 0.35 milliseconds. For Cell C to reach its threshold charge requires $t_C$, about 50 milliseconds. A PROM Programmer can determine this time for each bit by simply applying a series of short programming pulses of known duration and reading the state of the bit after each of the pulses. The number of such pulses required to reach the threshold charge is a measure of that time.

The key to reliable data retention, however, is to produce an adequate overcharge so that all of the variables which affect proper readout can be accounted for. The variables which determine the required overcharge and their approximate effects are as follows:

### Power Supply Voltage

Minimum supply voltage is the worst case condition for successfully reading out a programmed bit. Its effect is highly nonlinear so that a PROM operated with a supply voltage 0.5 below minimum specification may not work reliably under

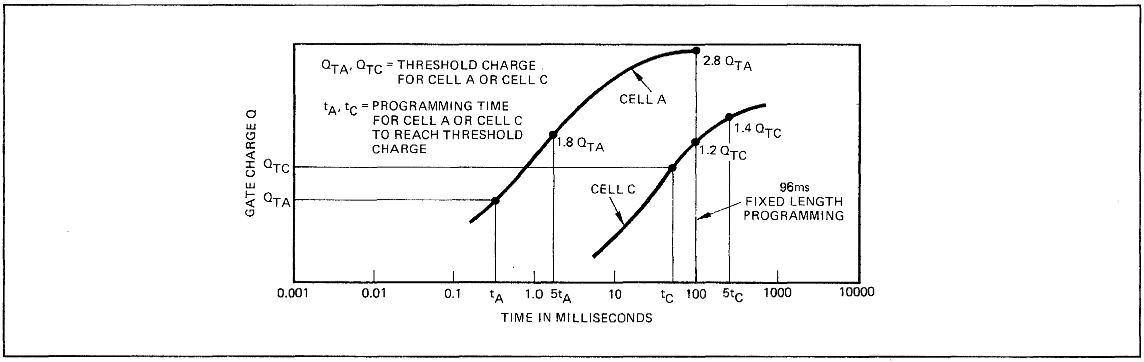


Figure 4. The programming characteristics of two cells in a 1702A PROM. The relative overcharge effects of the fixed and variable programming techniques are shown.

any circumstances. This variable is best accounted for by reading the PROM with minimum specified supply voltages during the programming operation. We recommend that all PROMs later be operated in systems with supply voltages between the nominal and the high end of the PROMs' specified voltage range. This not only improves data retention, it reduces access time.

### Charge Neutralization

The degree of possible charge "neutralization" (effective loss of charge due to minority carrier migration in the substrate) is temperature dependent. Frohman-Bentchkowsky, in Ref. 1, indicates the maximum possible change at 125°C as 10% of initial charge. Charge neutralization occurs primarily within the first 48 hours after the PROM is programmed.

### Leakage Current

Some electrons do bleed off the buried gate over an extended period of time. The rate of loss is temperature dependent. Total charge loss at 125°C over 10 years may be as much as 10% of initial charge (Ref. 1). Leakage current tends to half for each 10°C drop in temperature. Occasionally defects in the $SiO_2$ result in leaking bits. No reasonable safety factor can handle this. Vendor screening and customer screening can eliminate PROMs with leaking bits (see the suggested screening tests in this paper).

### Temperature

As chip temperature increases, $R_{SD}$ increases, as does the effective value of $V_T$. The total effect is that a chip operated at 70°C ambient requires about 15% more charge than it does at 25°C. Higher operating temperatures require greater safety factors.

Based on the factors cited above, Pro-Log recommends that each programmed bit be initially charged to have at least a charge equal to 1.4 $Q_T$, that is a minimum initial safety factor of 40% when programmed at 25°C.

The recommended charge safety factor is achieved in Pro-Log's Series 90 Programmer as follows: The PROM is programmed a character (8 bits) at a time. The selected character is hit with a three millisecond, 47 volt programming pulse, as specified by the vendor. After the programming pulse is removed, the character is read out and compared to the desired character. This operation is repeated (at a 20% duty cycle) until the readout matches the desired pattern. A record is kept of the number of pulses, N, required to produce the correct readout. This is the length of time the slowest bit in the character requires to reach its $Q_T$. The character is then programmed 4N more times. If, for example, the slowest bit in the character were like Cell C in Figure 4, it would take about 16 programming pulses to get it to read correctly. That character would be programmed with an additional 64 programming pulses (a total of 80) and the charge for the worst case bit would reach 1.4 $Q_{TC}$ as shown on the curve. All other bits would have an even greater overcharge.

The vendor's fixed programming technique calls for 32 of the 47 volt three millisecond programming pulses at a 20% duty cycle for all bits. A PROM takes two minutes to program with this technique and cells like Cell C have only a 20% charge safety factor and a high probability that the bit will drop out. In fact, some cells in some PROMs have slower charging curves than the one shown for Cell C, so that they receive little or no overcharge. However, over 98% of the bits in most PROMs have charging curves like the one for Cell A. With Pro-Log's techniques, the Cell A type bits receive a total of five programming pulses and the typical PROM takes only 22 seconds to fully program. Cell C type bits automatically receive many more programming pulses than the vendor's specified limit, and the Programmer automatically rejects a PROM with any cell that doesn't reach its $Q_T$ within 16 pulses. The 16 pulse limit is used because the charge asymptote for a slower bit may be so close to its $Q_T$ that the required safety factor could never be assured.

## ERASING THE PROM

Complete erasure of the PROM prior to reprogramming is absolutely essential for reliable operation. There is no direct way to tell when a bit has been adequately erased. Figure 5 shows typical erasing curves for Cell A and Cell C after each cell has been programmed. In this figure, the initial charge for each cell has been normalized to its threshold charge $Q_T$.

Under an erase light, Cell C crosses the threshold and appears to erase sooner than Cell A. This relative dropout time under calibrated light conditions is in fact the measurement tool which was used to experimentally verify the overcharge characteristics described in the preceding section.

Through experimentation, I determined a method for calibrating an erase light system for a PROM. The technique is as

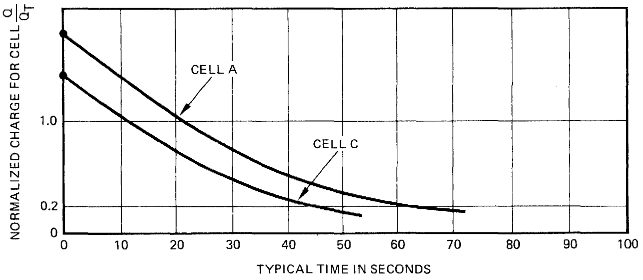


**Figure 5. Erasing characteristics for Cell A and Cell C under an ultra-violet light of nominal intensity. Each cell appears to be erased as its gate charge Q drops below its $Q_T$ value. Proper erasure requires continued exposure so as to reach 0.2 $Q_T$ or less.**

follows: 1) Fully program all bits in a PROM. 2) Put the PROM under an erase light at a specific distance and determine how long it takes (through repeated readout of the PROM) to appear to erase all bits. 3) Make the total erasing time at least five times the apparent erasing time. A three times factor is just adequate, the five times factor is to allow for loss of light intensity with age and slight variations from chip to chip. This calibration need only be done once for 1702A PROMs. The erasure time is extremely consistent from PROM to PROM with a couple of exceptions. The first exception is a shadow cast on a few cells by dirt (or silicon chips) on the surface of the PROM. The shadow reduces the light induced photocurrent and thus increases erase time for those cells. The second exception is a shadow created by material which is opaque to U.V. light. This could be visible contaminants on the outer surface of the quartz lid or it could be contaminants or materials which are transparent to visible light but opaque to U.V. (such as the plastic carriers which many PROMs come in, or gum from a label previously on the quartz lid). Awareness of the problem and careful cleaning can eliminate the second exception. Screening of erase times on a sample basis can reduce the first exception to a negligible level.

We strongly urge the user to avoid any erasing set-up in which the PROM appears to erase in less than one minute. Such a set-up exposes the PROM to U.V. light with too high an intensity. We believe that light intensity during erasing which is too high accelerates irreversible chemical reactions within the chip and thus reduces the number of times the PROM can be reprogrammed and erased. We set-up our erasing systems so that a 1702A appears to erase in three minutes and is left under the erase light for 15 minutes.

## SOME FAILURE MODES IN 1702As

### Light Sensitive Sense Amplifiers

Some preamplifiers are photosensitive. Their effective gain drops dramatically under normal room light or in daylight. Previously programmed bits are read out marginally or cannot be read out at all, so long as the light is on – cover the quartz lid and the device works perfectly! Actually, data is not erased by room or daylight, it's simply inaccessible so long as the light is on. We've observed this photosensitivity in various production batches of 1702As, when programming on our Series 90 Programmer. Sometimes it has appeared in over 10% of the devices. There has been some vendor screening for this problem.

To avoid problems with photosensitivity, simply cover the quartz lid with a label during and after programming. Pro-Log does this as a matter of practice. The label contains the drawing number for the program contained in the device and prevents accidental erasure under U.V. light. Photosensitive devices are perfectly reliable for field use so long as they are kept in the dark.

### Time-Sensitive Sensitive Amplifiers

A programmed bit may readout validly within the prescribed access time and for hundreds of microseconds thereafter. But after a few hundred microseconds or a few milliseconds of static readout the bit drops out. Readdressing the character restores the readout, but only for the same period of time. This phenomenon is caused by a sense amplifier whose effective threshold increases with time. It is relatively rare, occurring in less than 1% of the devices but is production lot oriented.

This phenomenon presents no problem to the user when the PROM is used in microprocessor systems or in lookup tables where it is read within a few microseconds of addressing. It does present a problem where a given address is to be read for an extended period of time. The binary data display in the Series 90 reads data for extended periods of time.

### Static Discharge

In Pro-Log's first year of using 1702As, a few devices failed mysteriously while being programmed or handled. The general culprit blamed for this problem was static discharge. Although this occasionally may be a problem, we found several other causes (covered below) for these mysterious random events. After taking proper precautions, we seldom see a PROM failure.

Static discharge is not a significant problem when the PROM leads are partially protected by internal diodes and series impedances. However, to be safe, parts should be stored and transported in their carrying packages on a conductive foam or on an equivalent material.

Static discharge is not critical when the room in which they're handled has a concrete or similar type floor. If the operator is on a surface where he might build-up static charge (e.g., carpeting), he should touch a grounded surface before handling the part, then pick the part up in such a way that he does not touch any leads.

### 1702A PROM Totally Fails . . . Reads All Bits as Programmed Bits

There are several possible causes for this. We found the primary cause to have been an accidental momentary insertion of the PROM into a live socket with the device offset by one pin. This caused the chip select line and the $V_{BB}$ line to be connected between two power supplies in such a way that the chip select line was fused open inside the device by a current surge in excess of 250 ma. The problem is due to the pin configuration of the 1702A and lack of external current limiting in the set-up in question. External current limiting on the $V_{BB}$, CS and $V_{prog}$ pins has eliminated the problem.

Other sources of PROM failure include exceeding programming voltage or duty cycle specifications during programming (see below).

### Two or More Words Get Programmed at the Same Time or Some Bits Don't Erase After Being Programmed

**Sources**

a) Excessive programming voltages. The vendor has specified very precise limits to programming voltages. To exceed the maximum specified program voltage even by as little as half a volt and for as little as a few microseconds, can cause permanent bit or PROM failure in a significant number of parts.

b) Excessively fast rise and fall times (less than 0.5 microseconds) in the programming voltages for address lines, data lines or power supply lines. It is our opinion that this is a source of failures because of capacitive coupling within the devices.

### Programming Fatigue

Repeatedly programming and erasing the PROMs does produce chemical changes in the device. Devices tend to require more time to program after going through 30 or more cycles of program and erase. We have cycled devices well over 100 times and still found them usable. The longevity is affected by the erase light set-up and the programming technique.

## SUPPORTING TESTS

In early 1973, we first ran tests on 32 randomly selected 1720As from a particular production lot. The test set-up was as follows: a) All bits in each PROM were programmed to vendor's specification: 32 pulses of 3 ± 0.1 milliseconds duration and 47 ± 0.2 volts amplitude and 18 ± 2% duty cycle. b) Each PROM was then placed in a test fixture at a specific distance from an ultra-violet light source. c) The light source was turned on and the PROM scanned every second searching for a bit to read as unprogrammed. The time required for the first bit in each of the 32 PROMs to "dropout" varied from an extreme of two seconds in one PROM to thirty seconds in another PROM. The bulk of the PROMs took over 15 seconds to drop their first bit. One PROM with a two-second and another with a five-second first-bit dropout time were reprogrammed to the vendor's specification and left overnight. Next morning, the two-second bit had dropped out by itself and the five-second bit was marginal.

Using the identical PROMs, PROM Programmer and light source set-up, the test was rerun using Pro-Log's variable programming technique. The first bit dropout among all PROMs was a steady 15 ± 2 seconds. Experimental repeatability was about ±2 seconds. After erasure and reprogramming using the variable programming method, the PROMs were baked at over 100°C for eight hours and left at 25°C for several days. All bits remained firmly programmed.

## SUGGESTED INCOMING INSPECTION SCREENING

Pro-Log has recently adopted the following incoming inspection procedure for the 1702A PROMs. These tests are performed on a lot sampling basis as our experience has shown that PROM problems are production lot oriented and vendor oriented. The tests do not check access time, but so far we've found this unnecessary.

### Suggested Equipment

- Series 90 PROM Programmer with a special version of the PM9001 personality module modified to program with 1 ms (rather than 3 ms) programming pulses and programming each location with a 1N overcharge rather than a 4N overcharge and limiting the maximum N tries for each address to 100. This personality module is the PM9001-QA and is available from Pro-Log.
- 9103 Erase Light or equivalent calibrated erase light.
- An oven.

### Procedure

1. Randomly select a sample of 50 PROMs from each batch received and having the same batch I.D. number.
2. Check all PROMs on the programmer for the erased condition. Parts are supposed to be fully erased as received.
3. Program all bits in all PROMs on the modified PM9001 personality module. In worst case bits, this programming produces only half the safety factor that regular programming yields.
4. Bake all PROMs in the oven at 125°C for 24 hours.
5. Remove the devices from the oven, cool and check for bit dropout on the programmer.
6. Erase all PROMs under calibrated erasing conditions.
7. Check all parts for successful erasure.

### Acceptance

The most critical screening is at Step 5. If one or two devices exhibit bit dropout the entire production lot must be screened for bit dropout prior to use. If three or more devices fail, the lot should be rejected. An acceptable vendor should have at least 80% of all lots shipped pass the test at Step 5, with no failures.

If the combined failed PROMs for all tests exceed five, the lot should be rejected.

## CONCLUSIONS

The 1702A has proven to be extremely reliable when properly handled. Pro-Log has programmed most devices right out of the box, as received from the vendor. Those devices which have programmed on the Series 90 Programmer and passed in-house system tests have functioned at reliability levels in excess of those for simple TTL chips.

## REFERENCES

1. FAMOS READ-ONLY MEMORY, Frohman-Bentchkowsky, IEEE Journal of Solid-State Circuits, Vol. SC-6, No. 5, October 1971.

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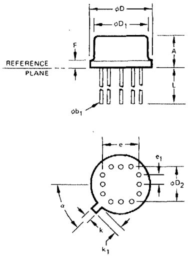
# Packages

8

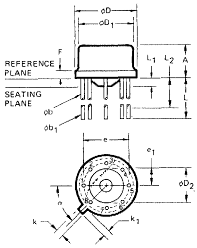
# PACKAGE GUIDE

## Metal Can Packages

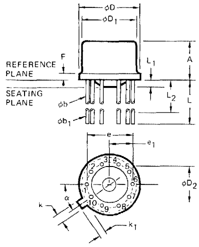
TO-8


φD
φD1
F
A
REFERENCE PLANE
L
φb1
e
e1
φD2
α
k
k1

TO-99


φD
φD1
F
REFERENCE PLANE
SEATING PLANE
L1
L2
A
L
φb
φb1
e
e1
φD2
α
k
k1

TO-100


φD
φD1
F
REFERENCE PLANE
SEATING PLANE
L1
A
L2
L
φb
φb1
e
e1
φD2
α
k
k1

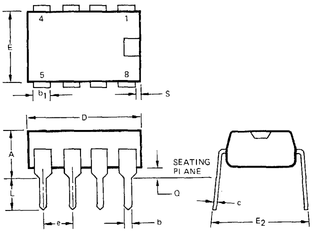
### DIMENSIONS (inches)

| Parameters | TO-8 | | TO-100 | | TO-99 | |
|---|---|---|---|---|---|---|
| A | .160 | .180 | .165 | .181 | .165 | .180 |
| e | .390 | .410 | .220 | .240 | .190 | .210 |
| $e_1$ | .090 | .110 | .105 | .125 | .090 | .110 |
| F | .020 | .030 | .013 | .030 | .013 | .030 |
| k | .024 | .034 | .027 | .034 | .027 | .034 |
| $k_1$ | .024 | .038 | .027 | .042 | .032 | .042 |
| L | .500 | .600 | .500 | .600 | .500 | .560 |
| $L_1$ | | | | .050 | | .050 |
| $L_2$ | | | .250 | | .250 | |
| $\alpha$ | 45° | | 36° BSC | | 45° BSC | |
| $\phi b$ | | | .016 | .019 | .016 | .019 |
| $\phi b_1$ | .015 | .021 | .015 | .021 | .015 | .021 |
| $\phi D$ | .595 | .630 | .355 | .370 | .355 | .370 |
| $\phi D_1$ | .540 | .560 | .310 | .330 | .310 | .330 |
| $\phi D_2$ | .390 | .410 | .120 | .160 | .120 | .160 |

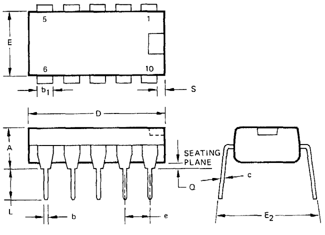
# PACKAGE GUIDE (Cont'd)

## Molded Packages

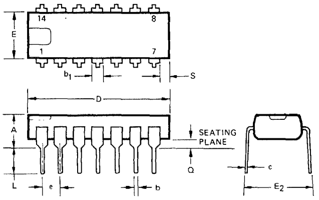
**PL-8**


4
1
5
8
E
b1
S
D
A
L
SEATING PLANE
Q
c
e
b
E2

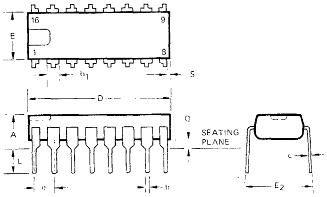
**PL-10**


5
1
6
10
E
b1
S
D
A
L
SEATING PLANE
Q
c
b
e
E2

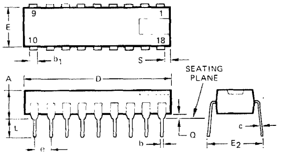
**PL-14**


14
8
1
7
E
b1
S
D
A
SEATING PLANE
Q
c
L
e
b
E2

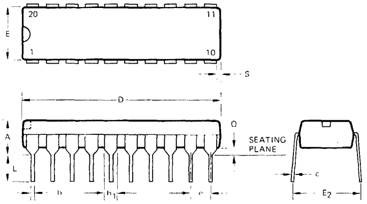
**PL-16**


16
9
1
8
E
b1
S
D
A
Q
SEATING PLANE
L
c
e
b
E2

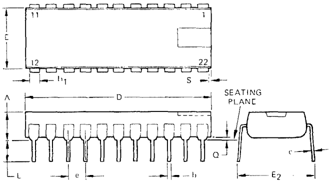
**PL-18**


9
1
10
18
E
b1
S
SEATING PLANE
A
D
L
Q
c
e
b
E2

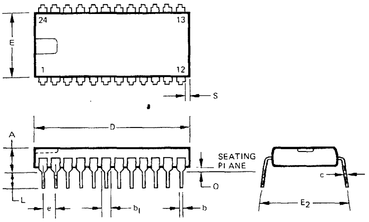
**PL-20**


20
11
1
10
E
S
D
Q
A
SEATING PLANE
L
c
b
b1
e
E2

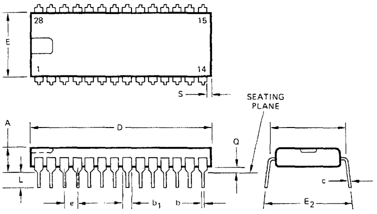
**PL-22**


11
1
12
22
E
b1
S
SEATING PLANE
A
D
Q
c
L
e
b
E2

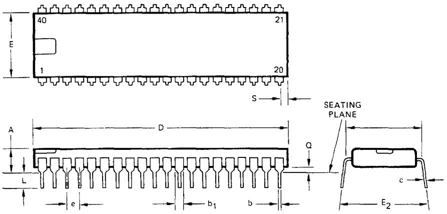
**PL-24**


24
13
1
12
E
S
A
D
SEATING PLANE
c
Q
L
e
b1
b
E2

**PL-28**


28
15
1
14
E
S
SEATING PLANE
A
D
Q
L
c
e
b1
b
E2

**PL-40**


40
21
1
20
E
S
SEATING PLANE
A
D
Q
L
c
e
b1
b
E2

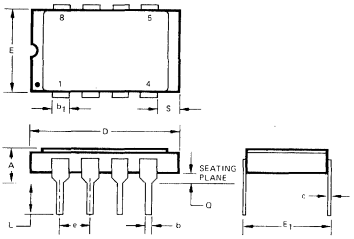
## DIMENSIONS (inches)

| Parameters | PL-8 | | PL-10 | | PL-14 | | PL-16 | | PL-18 | | PL-20 | | PL-22 | | PL-24 | | PL-28 | | PL-40 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .164 | .170 | .164 | .170 | .158 | .164 | .164 | .170 | .164 | .170 | .164 | .170 | .164 | .170 | .165 | .200 | .165 | .200 | .165 | .200 |
| b | .016 | .020 | .016 | .020 | .016 | .020 | .016 | .020 | .016 | .020 | .018 | .022 | .018 | .022 | .018 | .022 | .018 | .022 | .018 | .022 |
| $b_1$ | .058 | .062 | .058 | .062 | .058 | .062 | .058 | .062 | .058 | .062 | .058 | .062 | .058 | .062 | .058 | .062 | .058 | .062 | .058 | .062 |
| c | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 |
| D | .380 | .382 | .515 | .525 | .745 | .755 | .745 | .755 | .895 | .905 | 1.015 | 1.025 | 1.005 | 1.105 | 1.245 | 1.255 | 1.445 | 1.455 | 2.045 | 2.055 |
| E | .245 | .255 | .245 | .255 | .245 | .255 | .245 | .255 | .245 | .255 | .255 | .265 | .345 | .355 | .535 | .545 | .535 | .545 | .535 | .545 |
| $E_2$ | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .400 | .470 | .585 | .690 | .585 | .690 | .585 | .690 |
| e | .098 | .102 | .098 | .102 | .098 | .102 | .098 | .102 | .098 | .102 | .098 | .102 | .098 | .102 | .098 | .102 | .098 | .102 | .098 | .102 |
| L | .125 | .130 | .125 | .130 | .125 | .130 | .125 | .130 | .125 | .130 | .125 | .130 | .125 | .130 | .125 | .130 | .125 | .130 | .125 | .130 |
| Q | .017 | .023 | .017 | .023 | .017 | .023 | .017 | .023 | .017 | .023 | .017 | .023 | .017 | .023 | .017 | .023 | .017 | .023 | .017 | .023 |
| S | .010 | .018 | .010 | .018 | .040 | .050 | .010 | .018 | .018 | .022 | .028 | .032 | .018 | .022 | .040 | .050 | .040 | .050 | .040 | .050 |

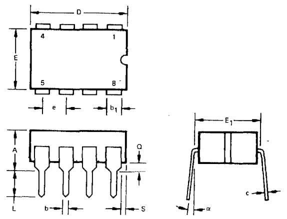
# PACKAGE GUIDE (Cont'd)

## Hermetic Dual-In-Line Packages

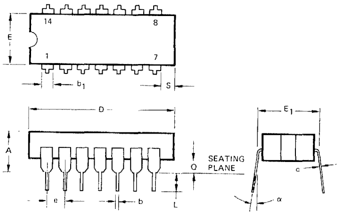
SB-8


8
5
1
4
E
b1
S
D
A
SEATING PLANE
L
e
b
Q
c
E1

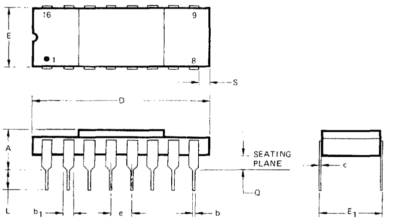
CD-8


D
4
1
5
8
E
e
b1
A
Q
L
b
S
E1
c
α

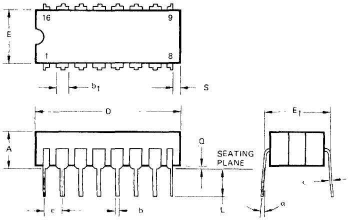
CD-14


14
8
1
7
E
b1
S
D
A
SEATING PLANE
Q
e
b
L
E1
c
α

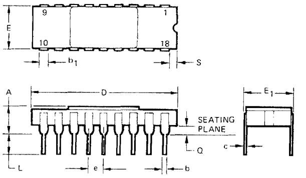
SB-16


16
9
1
8
E
S
D
A
SEATING PLANE
Q
L
b1
e
b
c
E1

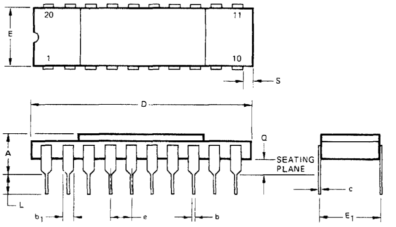
CD-16


16
9
1
8
E
b1
S
D
A
Q
SEATING PLANE
e
b
L
E1
c
α

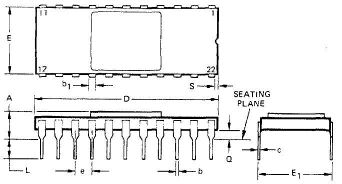
SB-18


9
1
10
18
E
b1
S
A
D
E1
SEATING PLANE
Q
c
L
e
b

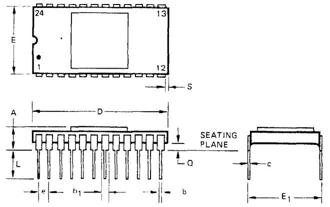
SB-20


20
11
1
10
E
S
D
A
Q
SEATING PLANE
L
b1
e
b
c
E1

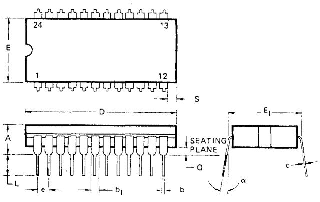
SB-22


11
1
12
22
E
b1
S
SEATING PLANE
A
D
L
e
b
Q
c
E1

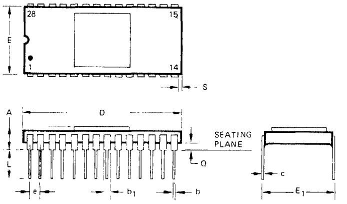
SB-24


24
13
1
12
E
S
A
D
SEATING PLANE
Q
L
e
b1
b
c
E1

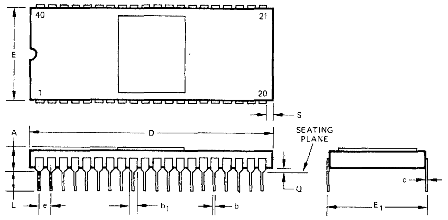
CD-24


24
13
1
12
E
S
D
E1
A
SEATING PLANE
Q
L
e
b1
b
c
α

SB-28


28
15
1
14
E
S
A
D
SEATING PLANE
Q
L
e
b1
b
c
E1

SB-40


40
21
1
20
E
S
A
D
SEATING PLANE
Q
L
e
b1
b
c
E1

### DIMENSIONS (inches)

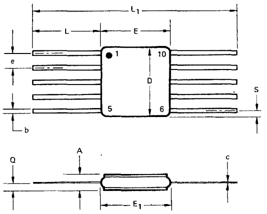
| Parameters | SB-8 | | CD-8 | | CD-14 | | SB-16 | | CD-16 | | SB-18 | | SB-20 | | SB-22 | | SB-24 | | CD-24 | | SB-28 | | SB-40 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .105 | .169 | .130 | .185 | .130 | .185 | .105 | .169 | .130 | .185 | .100 | .175 | .100 | .175 | .100 | .175 | .100 | .182 | .130 | .185 | .100 | .182 | .100 | .182 |
| b | .015 | .022 | .017 | .020 | .017 | .020 | .015 | .022 | .017 | .020 | .015 | .022 | .015 | .022 | .015 | .022 | .015 | .022 | .017 | .020 | .015 | .022 | .015 | .022 |
| $b_1$ | .045 | .060 | .055 | .065 | .055 | .065 | .040 | .060 | .055 | .065 | .040 | .060 | .040 | .060 | .030 | .060 | .030 | .060 | .050 | .060 | .030 | .060 | .030 | .060 |
| c | .008 | .012 | .009 | .011 | .009 | .011 | .008 | .012 | .009 | .011 | .008 | .012 | .008 | .012 | .008 | .012 | .008 | .012 | .009 | .011 | .008 | .012 | .008 | .012 |
| D | .510 | .528 | .370 | .400 | .750 | .785 | .770 | .808 | .750 | .785 | .870 | .910 | .950 | 1.00 | 1.068 | 1.092 | 1.188 | 1.212 | 1.235 | 1.285 | 1.386 | 1.414 | 1.98 | 2.02 |
| E | .278 | .298 | .245 | .285 | .245 | .285 | .278 | .298 | .244 | .285 | .278 | .298 | .278 | .298 | .378 | .398 | .568 | .598 | .510 | .545 | .568 | .598 | .568 | .598 |
| $E_1$ | .295 | .310 | .300 | .314 | .290 | .320 | .300 | .314 | .290 | .320 | .290 | .320 | .290 | .320 | .390 | .420 | .590 | .620 | .600 | .618 | .590 | .610 | .590 | .610 |
| e | .093 | .107 | .095 | .105 | .095 | .105 | .093 | .107 | .095 | .105 | .093 | .107 | .095 | .107 | .093 | .107 | .092 | .108 | .095 | .105 | .092 | .108 | .092 | .108 |
| L | .130 | .145 | .130 | .145 | .130 | .145 | .130 | .145 | .130 | .145 | .130 | .145 | .130 | .145 | .130 | .145 | .130 | .145 | .130 | .145 | .130 | .145 | .130 | .145 |
| Q | .020 | .045 | .015 | .045 | .015 | .045 | .020 | .045 | .015 | .045 | .020 | .045 | .020 | .060 | .020 | .060 | .020 | .060 | .020 | .060 | .020 | .060 | .020 | .060 |
| S* | .025 | | .004 | | .020 | | .005 | | .005 | | .005 | | .005 | | .005 | | .005 | | .010 | | .005 | | .005 | |
| α | 0 | | 3° | 13° | 0 | | 3° | 13° | 0 | | 3° | 13° | 0 | | 3° | 13° | 0 | | 3° | 13° | 0 | | 3° | 13° |

*From edge of end lead.

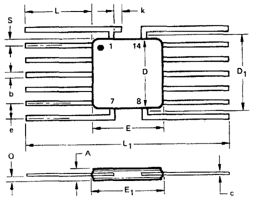
# PACKAGE GUIDE (Cont'd)

## Flat Packages

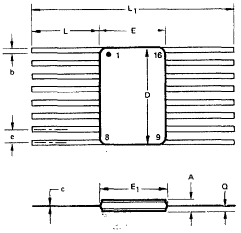
FP-10


L1
L
E
1
10
D
5
6
e
b
S
A
Q
c
E1

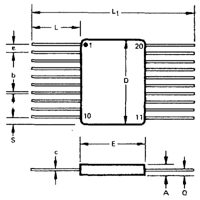
FP-14


S
L
k
1
14
D
D1
7
8
b
e
E
L1
A
Q
E1
c

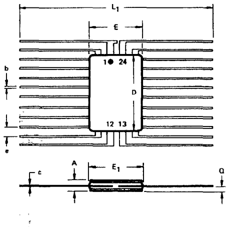
FP-16


L1
L
E
1
16
b
D
e
8
9
c
E1
A
Q

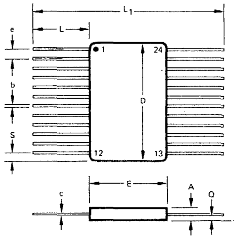
FP-20


L1
L
e
1
20
b
D
10
11
S
c
E
A
Q

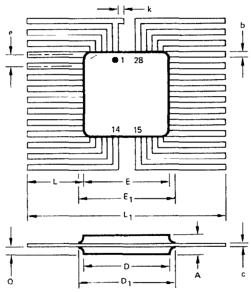
FP-24


L1
E
1
24
b
D
12
13
e
c
A
E1
Q

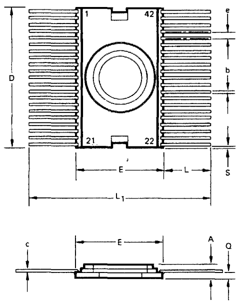
FP-24L


L1
e
L
1
24
b
D
S
12
13
c
E
A
Q

FP-28


k
e
b
1
28
14
15
L
E
E1
L1
D
D1
Q
A
c

FP-42


1
42
e
D
b
21
22
E
L
S
L1
c
E
A
Q

### DIMENSIONS (inches)

| Parameters | FP-10 | | FP-14 | | FP-16 | | FP-20 | | FP-24 | | FP-24L | | FP-28 | | FP-42 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .040 | .070 | .040 | .070 | .040 | .080 | .050 | .090 | .040 | .080 | .050 | .090 | .045 | .080 | .080 | .105 |
| b | .013 | .019 | .013 | .019 | .015 | .019 | .015 | .019 | .015 | .019 | .016 | .018 | .015 | .019 | .018 | .022 |
| c | .003 | .006 | .003 | .006 | .003 | .006 | .004 | .006 | .003 | .006 | .004 | .006 | .003 | .006 | .007 | .010 |
| D | .245 | .275 | .245 | .275 | .370 | .410 | .490 | .540 | .370 | .410 | .575 | .640 | .370 | .410 | 1.05 | 1.07 |
| $D_1$ | | .275 | | .275 | | .410 | | | | .410 | | .640 | | .410 | | |
| E | .245 | .275 | .245 | .275 | .245 | .290 | .360 | .410 | .260 | .295 | .360 | .410 | .370 | .410 | .634 | .646 |
| $E_1$ | | .275 | | .275 | | .290 | | | | .295 | | .410 | | .410 | | |
| L | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 |
| $L_1$ | .335 | .370 | .335 | .370 | .325 | .380 | .270 | .315 | .300 | .370 | .270 | .315 | .250 | .300 | .295 | .340 |
| Q | .920 | .980 | .920 | .980 | .920 | .980 | .955 | .975 | .920 | .980 | .955 | .975 | .945 | .985 | 1.26 | 1.30 |
| S* | .010 | .040 | .010 | .040 | .010 | .040 | .020 | .040 | .010 | .040 | .020 | .040 | .010 | .040 | .030 | .050 |

*From center of lead.

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**HEADQUARTERS SALES MANAGER** – Mac Wilson

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**Suite 806**
**Beverly Hills, California 90212**
**Tel: (213) 278-9700**
**(213) 278-9701**
**TWX: 910-490-2143**

**Advanced Micro Devices**
2430 South 20th Street
Suite 10
Phoenix, Arizona 85034
Tel: (602) 258-6515
(602) 258-6516
TELEX: 668-325
TWX: 910-951-4216

**NORTHWEST AREA**
**Advanced Micro Devices**
901 Thompson Place
Sunnyvale, California 94086
Tel: (408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

**MID-AMERICA AREA**
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2625 Butterfield Road
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(312) 323-9601
TWX: 910-254-2295

**Advanced Micro Devices**
7615 Metro Boulevard
Suite 116
Edina, Minnesota 55435
Tel: (612) 835-4445
(612) 835-4446

**Advanced Micro Devices**
6006 Bellaire Boulevard
Suite 118
Houston, Texas 77036
Tel: (713) 667-9595

**EASTERN AREA**
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Roslyn Heights, N.Y. 11577
Tel: (516) 484-4990
(516) 484-4991
TWX: 510-223-0649

**Advanced Micro Devices**
6100 Baltimore National Pike
Baltimore, MD 21228
Tel: (301) 744-8233

**Advanced Micro Devices**
6806 Newbrook Ave.
E. Syracuse, N.Y. 13057
Tel: (315) 437-7546
TELEX: 93-7201

**NORTHEAST AREA**
**Advanced Micro Devices**
45 William Street, Bldg. 6
Wellesley, Massachusetts 02181
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(617) 237-2775

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TELEX: 523 883

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Robert-Leicht-Strasse 120
D-7000 Stuttgart-Vaihingen
West Germany
Tel: 0711-681001

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23, Lower Belgrave Street
London, S.W. 1, England
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1-4, 3 Chome Nishi-Shinjuku
Shinjuku-ku, Tokyo 160 Japan
Tel: (03) 346-0363
TELEX: 2324064

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Prospect, S. Australia 5082
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TELEX: 82635

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GES.M.B.H.
Meidlinger Hauptstrasse 78
A-1120 Vienna, Austria
Tel: 83 63 96
TELEX: 011532

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MCA Tronics
62 Route Dn Condroz
4200 Ongrée Belgium
Tel: 041-362780
TELEX: 46 (49552)

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Ace Enterprise
Suite 1211
363 Nathan Road
Kowloon, Hong Kong

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Scherfigsvej 1
DK-2100 Copenhagen Ø
Denmark
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TELEX: 27260

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92100 Boulogne, France
Tel: 603 66 40
TELEX: AMM 200 491

S.C.A.I.B.
15-17 Avenue Segur
75007 Paris, France
Tel: 555 71 11
TELEX: 24774

Tekelec-Airtronic
Cite des Bruyeres
Rue Carle - Vernet
92 Sevres, France
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TELEX: 25 997

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D-316 Lehrte
West Germany
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TELEX: 0-922383

Cosmos Electronic GmbH
Hegelstrasse 16
D-8000 Munich 83
West Germany
Tel: (089) 602088
TELEX: 0-522545

Cosmos Electronic GmbH
Büro Bayern Nord
8430 Neumarkt
Kanalweg 33, West Germany
Tel: 09181-9731

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Heinrich Ebner Strasse 13
D-7000 Stuttgart 50
West Germany
Tel: 0711-561712
TELEX: 0-7254490

Technoprojekt
Ostring 150
D-6231 Schwalbach
West Germany
Tel: 06196-82100
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Elbatex GmbH
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D-7100 Heilbronn
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Tel: 07131-89001
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West Germany
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Nordelektronik Vertriebs GmbH
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Harksheiderweg 238-240
D-2085 Quickborn
West Germany
Tel: (04106) 4031
TELEX: 0-214299

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D-5330 Königswinter 1
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TELEX: 0-885237

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Oss
Holland
Tel: 04120-24200
04120-27574
TELEX: 50835

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Tel-Aviv, Israel
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TELEX: VITKO 33400

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Rome, Italy
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TELEX: 58233

Cramer Italia SpA
Via Melchiorre Gioia, 74
20125 Milano, Italy
Tel: (02) 376 40 39

Cramer Italia SpA
Via Malta, 5
40135 Bologna, Italy
Tel: (051) 42 28 90

**JAPAN**
Advanced Technology Corporation
of Japan
Tashi Bldg., 3rd Floor
No. 8, Minami Motomachi
Shinjuku-ku, Tokyo 160 Japan
Tel: (03) 265-9416
TELEX: (781) 22180

Dainichi Electronics
Kohraku Building
1-8, 1-Chome, Koraku
Bunkyo-ku, Tokyo, Japan
Tel: (03) 813-6876

ISI Ltd.
8-3, 4-Chome, Iidabashi
Chiyoda-ku, Tokyo 102 Japan
Tel: (03) 264-3301

Kanematsu-Gosho Ltd.
5 Takara-Cho 2-Chome
Chuo-ku, Tokyo 104 Japan
Tel: (03) 562-8813

Microtek, Inc.
Naito Bldg. 7-2-8 Nishishinjuku
Shinjuku-ku Tokyo 160 Japan
Tel: (03) 363-2317
TWX: J28497

**NORWAY**
Intelco A/S
Stromsveien 204
P.O. Box 31
2011 Strommen
Norway
Tel: 47 2 702272

**SOUTH AFRICA**
South Continental Devices (Pty.) Ltd.
Suite 516, 5th Floor
Randover House
Cor. Hendrik Verwoerd
Dover Rd., Ranburg, Tvl.
P.O. Box 56420, Pinegowrie, 2123
South Africa
Tel: 48-7125
TELEX: 83324

**SPAIN**
Electronic Services S.A.
Adv. de Ramon y Cajal, 5
Madrid 8 Spain
Tel: 457 6615
TELEX: 42207

**SWEDEN**
Svensk Teleindustry
Box 502
162 05 Vallingby, Sweden
Tel: vx 08-890435
TWX: 13033

**SWITZERLAND**
Dimos AG
8048 Zurich
Badenerstrasse 701
Switzerland
Tel: 01162 61 40
TELEX: 52 028

Kontron Electronic AG
8048 Zurich
Bernerstrasse-Sud 169
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Tel: (1) 62 82 82
TELEX: 58836

**UNITED KINGDOM**
Dage International Ltd.
Eurosem Division
Haywood House
High Street
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TELEX: 24506

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Carluke Lanarkshire
Scotland
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TELEX: 77-9016

Quarndon Electronics
(Semiconductors) Ltd.
Slack Lane
Derby DE33ED England
Tel: Derby 32651
TELEX: 37163

Cramer Electronics
European Headquarters
16 Uxbridge Road
Ealing W5 2PB England
Tel: (01) 579 3001
TELEX: 933592

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## U.S. and Canadian Sales Representatives

**ALABAMA**
Electronic Manufacturers Agents
2311 Starmount Circle, S.W.
Huntsville, Alabama 35801
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San Diego, California 92111
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TWX: 910-335-1267

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3860 Cote Vertu
Suite 210
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Canada H4R 1V4
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TELEX: 05-821762
TWX: 610-422-3908

Vitel Electronics
701 Evans Avenue
Suite 205
Toronto, Ontario, Canada M9C 1A3
Tel: (416) 622-6300
TELEX: 06-967-881

**CANADA (Western)**
Ray Over Sales
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(1645 Rambling Lane)
Bellevue, Washington 98004
Tel: (206) 454-4551

**COLORADO**
Component Sales
12619 Antelope Trail
Parker, Colorado 80134
Tel: (303) 841-2650
TWX: 910-320-2266

**CONNECTICUT**
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Plainview, N.Y. 11803
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Conley & Associates, Inc.
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TWX: 810-856-3520

Conley & Associates, Inc.
1612 N.W. Second Ave.
P.O. Box 700
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Tel: (305) 395-6108
TWX: 510-953-7548

Conley & Associates, Inc.
7515 North Armenia Avenue
Tampa, Florida 33604
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1701 Carmen Drive
Elk Grove Village, Illinois 60007
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**IOWA**
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4403 First Avenue, S.E.
Cedar Rapids, Iowa 52402
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**KANSAS**
Palatine Engineering Sales, Inc.
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Lenexa, Kansas 66215
Tel: (913) 492-7020
TWX: 910-749-6499

Palatine Engineering Sales, Inc.
221 West Market Street
Derby (Wichita), Kansas 67035
Tel: (314) 426-7055
TWX: 910-740-6752

**MARYLAND**
Burgin-Kreh Associates, Inc.
6100 Baltimore National Pike
Baltimore, Maryland 21228
Tel: (301) 788-5200
TWX: 710-862-1450

**MICHIGAN**
Tom Mulligan & Associates
1994 Tiley Circle
Milford, Michigan 48042
Tel: (313) 363-5575

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Palatine Engineering Sales, Inc.
1573 N. Warson Road
St. Louis, Missouri 63132
Tel: (314) 426-7055
TWX: 910-765-0936

**NEW MEXICO**
The Thorson Company
2201 San Pedro, N.E.
Suite 107, Building 2
Albuquerque, New Mexico 87110
Tel: (505) 265-5655
TWX: 910-989-1174

**NEW YORK**
ERA
One Dupont Street
Plainview, N.Y. 11803
Tel: (516) 822-9890
TWX: 510-221-1849

Ossmann Component Sales Corp.
280 Metro Park
Rochester, New York 14623
Tel: (716) 442-3290
TWX: 510-253-7685

Ossmann Component Sales Corp.
132 Pickard Building
Syracuse, New York 13211
Tel: (315) 454-4477
TWX: 710-541-1522

Ossmann Component Sales Corp.
395 Cleveland Drive
Buffalo, New York 14215
Tel: (716) 832-4271
TWX: 710-522-1833

Ossmann Component Sales Corp.
1911 Vestal Parkway East
Vestal, New York 13850
Tel: (607) 785-9949
TWX: 510-252-1987

Ossmann Component Sales Corp.
82 Fair Street
Kingston, New York 12401
Tel: (914) 338-5505
TWX: 510-247-1941

**NORTH CAROLINA**
Burgin-Kreh Associates, Inc.
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Winston-Salem, North Carolina 27104
Tel: (919) 768-4174

**OHIO**
Dolfuss-Root & Co.
19035 Detroit Road
Rocky River, Ohio 44116
Tel: (216) 333-7504
TWX: 810-421-8201

Dolfuss-Root & Co.
354 Silvertree Lane
Centerville, Ohio 45459
Tel: (513) 433-6776

**PENNSYLVANIA**
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Kimconic Sales, Inc.
115 South High Street
Waterford, Pennsylvania 16441
Tel: (814) 796-6556

**(Eastern)**
GCM Associates
275 Commerce Drive
Ft. Washington, Pennsylvania 19034
Tel: (215) 646-7535
TWX: 510-661-0607

**TEXAS**
Bonser-Philhower Sales
13777 N. Central Expressway
Suite 500-13
Dallas, Texas 75243
Tel: (214) 234-8438

Bonser-Philhower Sales
10405 Town & Country Way
Suite 100
Houston, Texas 77024
Tel: (713) 467-4373

**UTAH**
Rapier-Richards Marketing
P.O .Box 26125
Salt Lake City, Utah 84125
(c/o Telemation Bldg., Receiving
2195 South 3600 West
Salt Lake City, Utah 84115)
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TWX: 910-925-5607

**VIRGINIA**
Burgin-Kreh Associates, Inc.
P.O. Box 2557
Memorial Professional Bldg.
2511 Memorial Ave.
Lynchburg, Virginia 24501
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**WASHINGTON**
Ray Over Sales
P.O. Box 1824
Vancouver, Washington 98663
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TELEX: 32-8951

**WISCONSIN**
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Phoenix, Arizona 85034
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Bell Industries
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Irvine, California 92705
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(213) 771-8300
TWX: 910-595-1900

Cramer/San Diego
8913 Complex Drive
San Diego, California 92123
Tel: (714) 565-1881
TWX: 910-335-1195

Cramer/San Francisco
720 Palomar Avenue
Sunnyvale, California 94086
Tel: (408) 739-3011
TWX: 910-339-9371

Hamilton Electro Sales
10912 W. Washington Blvd.
Culver City, California 90230
Tel: (213) 558-2100
(714) 522-8220
TWX: 910-340-6364
910-340-7073
TELEX: 67-36-92

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Mountain View, California 94040
Tel: (415) 961-7000
TWX: 910-379-6486

Hamilton/Avnet Electronics
8917 Complex Dr.
San Diego, California 92123
Tel: (714) 279-2421
TELEX: 69-54-15

Schweber Electronics
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Costa Mesa, California 92626
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(213) 924-5594
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