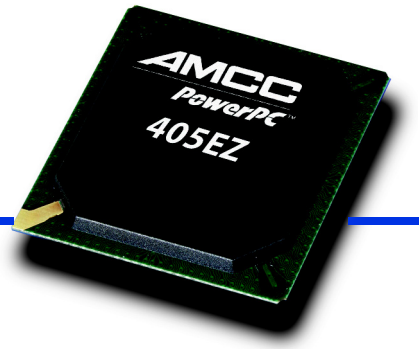


PowerPC 405EZ

Embedded Processor

With speeds of up to 400 MHz, a flexible on-chip and off-chip memory architecture, a unique combination of ADC, DAC, and configurable Chameleon Timer©/PWM, and a diverse connectivity package, the PowerPC 405EZ embedded processor provides a low power and small footprint system-on-a-chip solution for a wide range of high performance, cost-constrained embedded applications. Applications include industrial control, high-precision AC, DC and servo drive control, instrumentation, data acquisition, industrial automation, building and enclosure management, commercial and retail systems, Internet appliances, and intelligent USB peripherals. It is an easily programmable general purpose 32-bit RISC embedded processor that offers an ideal upgrade path for applications currently using 8-bit, 16-bit, RISC, or DSP MCUs needing performance and connectivity improvements.

Benefits

- Delivers up to 400MHz performance for high-speed embedded designs
- 16/32-bit external bus with arbitration and multi-master support
- SRAM, Pseudo-SRAM, and CellularRAM support
- NAND Flash interface
- On-chip high-speed SRAM accessible by CPU and DMA
- 10/100 IEEE1588-compliant Ethernet port
- Two CAN 2.0B channels
- Three USB 1.1/2.0 Full Speed compatible ports: two host ports, one device port (all with Full Speed PHYs)
- Two UARTs (UART0 with full hardware modem flow control),
- Inter-chip connectivity (SPI and I2C)
- Boot from ROM, NOR Flash, NAND Flash, SPI
- ADC: 8-input, 10-bit 300K samples/sec
- DAC: 10-bit 30M samples/sec
- Chameleon Timer© and PWM functions
- 54 GPIOs (each with programmable interrupts and pull-up/down resistors)
- Low power dissipation, small form factor for high-density, power-conscious (fanless) applications

The PowerPC 405 Core

The PowerPC 405 core has been optimized for system-on-a-chip designs requiring performance, low cost, and low power consumption. Performance is enhanced by using separate instruction and data cache. A 5-stage pipeline further boosts performance by offering single-cycle execution of most instructions, including loads and stores.

Dual Bus Architecture

The PowerPC 405EZ offers two on-chip buses: a Processor Local Bus (PLB) and an On-chip Peripheral Bus (OPB). The 64-bit PLB connects high-speed peripherals directly to the core. The 32-bit OPB serves less demanding devices. An external bus controller supports ROM, EPROM, SRAM, PSRAM, CellularRAM, Flash, and master/slave/ASIC peripherals.

Memory Support

The 32KB SRAM on-chip memory (OCM) provides fast access for your processing and data-intensive algorithms. The OCM is unified, so can support any mix of instructions and data. All onchip DMAs can access the OCM. External memories supported include SRAM, PSRAMs, CellularRAMs, ROM, NOR and NAND Flash, and SPI- or I2C-based NVRAMs. It is possible to build a complete high performance embedded solution with just the 405EZ's on-chip 32KB SRAM plus one NVRAM device (NOR, NAND, SPI, or I2C).

External Bus Controller (EBC)

EBC operates at up to 100MHz. It provides 16- or 32-bit data bus, 28-bit address bus, 8 chip selects, and bus arbitration for ample space and flexibility for large amounts of RAM, nonvolatile memory, and external peripherals/ASICs. Both simple and multi-master configuration systems can be built.

Ethernet Interface

A 10/100 Ethernet MAC is integrated onchip, making this an ideal processor for applications requiring an Ethernet connection or applications acting as a gateway between Ethernet, CAN, and USB networks. It is IEEE1588-compliant, so is ideally suited for the rapidly growing number of real-time and industrial networking applications. It is also an ideal SoC for Power-over-Ethernet applications.

NAND Flash Controller

The integrated 100MHz 8-bit interface supports two page-size modes: 512 byte + 16 byte, or 2Kbyte + 64 byte and generates Interrupt on Device Ready for long page writes and block erase. It supports Boot-from-NAND Flash (up to 4 Kbytes).

Chameleon Timer©/PWM

This "set-and-forget" timer is ideal for sophisticated PWM and space vector PWM functions. Its Autonomous Timer Service Engine manages intricate functions across 15 24-bit timer channels and 1 timebase channel with minimal or no CPU intervention. Up to 2 timebases are available simultaneously, selectable from 2 internal sources (Timebase A, Timebase B) and 1 external source.

CAN

Two CAN 2.0B protocol-compliant, ISO 11898-1 compliant channels containing 32 Rx buffers (each with its own message filter) and 32 Tx buffers. They operate at up to 1Mbps baud rate and support "listen only" for debugging and global masking.

USB

Three USB 1.1/2.0 Full Speed compatible ports are integrated onchip: two host ports, one device port (all with Full Speed PHYs). PHYs operate at 3.3V and are 5V tolerant.

ADC/DAC

The ADC has 8 analog inputs (3.3V) muxed into a single high precision, 10-bit 300K samples per second ADC converter.

The DAC has 1 analog current output (6mA swing max at 3.3V) capable of 30M samples per second.

ADC and DAC channels can be triggered by Chameleon Timer© channels and are capable of buffering as many as 32 values before asserting an interrupt or DMA request.

SCP (SPI)

1 SPI full duplex synchronous channel capable of up to 50MHz (50 Mbaud) operation and able to be SPI bus master. Programmable internal/external loopback capabilities. Supports Boot from SPI. Supports multi-master protocol.

PowerPC 405EZ

I2C
I2C interface operates at up to 400 kHz baud speed and supports all standard I2C EEPROMs. Can be clocked externally. Supports multi-master protocol and bootstrap from I2C.

Standard Peripherals
The PowerPC 405EZ offers an array of standard on-chip peripherals. Two UARTs (one with full hardware modem flow control), watchdog timer, and a 4-channel DMA controller capable of transferring data to/from any PLB and OPB slave, including the OCM and external bus.

Development Tools Support
PowerPC embedded processors are supported by AMCC and more than one hundred third-party vendors through the PowerPC Embedded Tools program. This program provides compilers, debuggers, real-time operating systems, emulators, logic analyzers, and a full range of tools to help manufacturers develop products more quickly. A PowerPC 405EZ evaluation board kit is available to help expedite product evaluation and project development.

PowerPC Partners Ecosystem
AMCC's embedded PowerPC processors are supported by an extensive ecosystem of products and services from a wide range of leading suppliers. AMCC's PowerPC Partners program includes industry-standard providers of:

- Embedded operating systems
- Hardware and software development tools
- Embedded software products and services
- Board-level products
- System design services
- Technical training.

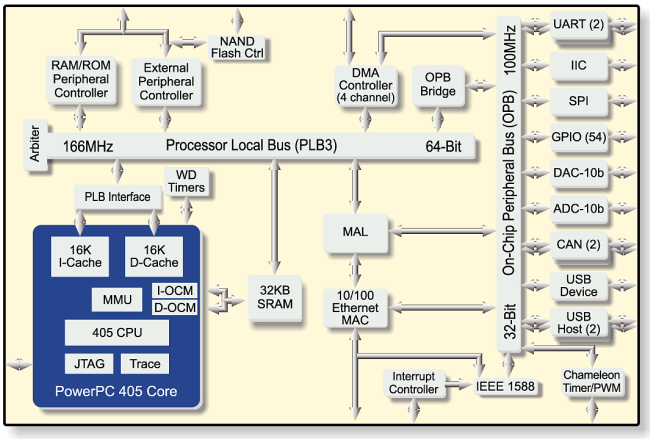
For full details of the products and services available through the PowerPC Partners program, or to browse support available for a specific processor, visit ***http://www.amcc.com/Embedded/Partners***
AMCC also provides an evaluation kit for this PowerPC processor, including an optimized evaluation board, sample applications, and other software.

Features
- Speed (frequency): DC to 400 MHz
- Performance: 1.52 DMIPs/MHz (608 DMIPS @ 400 MHz peak)
- 32 Kbytes of on-chip SRAM memory (OCM)
- On-chip NAND Flash Controller
- Supports 128 MB of external RAM when using 128 Mb devices
- External Bus Controller supports ROM, EPROM, CellularRAM, PSRAM, SRAM, Flash, and peripheral I/O devices; 16- or 32-bit data bus with bus arbitration
- DMA Controller with four independent channels supports transfers between all PLB slaves, including SRAM, internal UARTs, and devices on the external bus
- One 10/100 Ethernet interface with MAC; IEEE1588-compliant; includes dedicated Memory Access Layer controller
- Configurable Chameleon Timer©/PWM and watchdog timer
- 2 UARTs (one with full hardware modem flow control)
- 2 CAN 2.0 channels
- I2C (400 kHz) and multi-master SPI (50 MHz) Serial EEPROM Controller
- "Boot-from" sources: ROM, NOR Flash, NAND Flash, SPI
- 54 GPIOs
- Universal Interrupt Controller: 32 sources (4 external)
- JTAG and realtime trace support in processor core
- RoHS compliant (lead-free)

For more information, please visit ***http://www.amcc.com.***

Specifications

Technology
• 130 nm CMOS
Performance (estimated)
• 152 Dhrystone 2.1 MIPS @ 100 MHz
• 608 Dhrystone 2.1 MIPS @ 400 MHz
Frequency
• CPU: DC-400 MHz
• PLB: 166 MHz Maximum
• OPB: 100 MHz Maximum
• External Bus: 100 MHz Maximum
Power Dissipation
• <1.5W maximum, 0.60W typical
Case Temperature Range
• Industrial Range: -40°C to +85°C • Extended Range: -40°C to +105°C
Power Supply
• 1.5V (internal logic), 3.3V (I/O), 3.3V (external bus)
Signal I/Os
• TBD
Packaging
• 324-pin PBGA 23mm × 23mm (with 1mm ball pitch)



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POWERPC405EZ_PB_v1.15_03_28_2006