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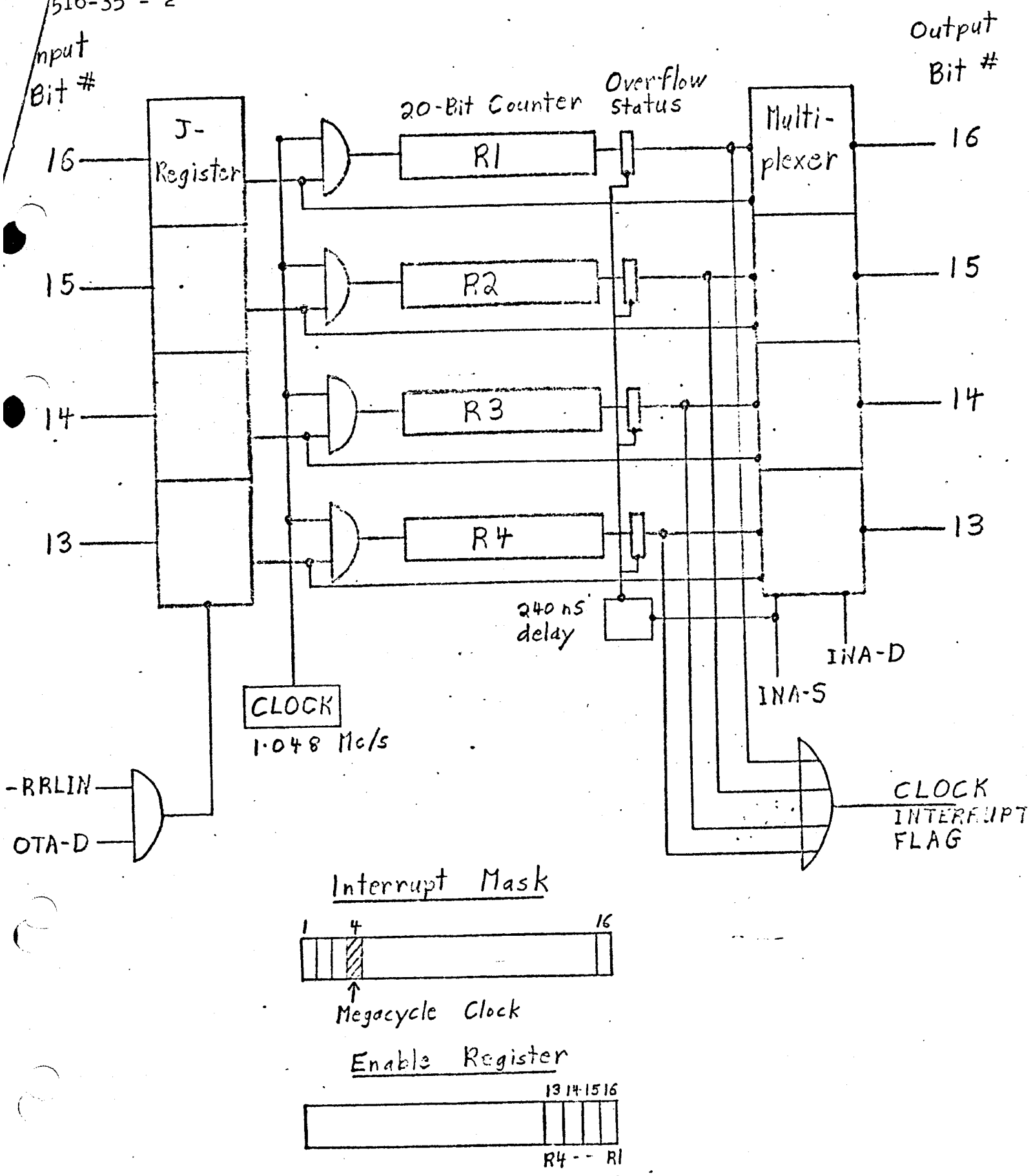
INTERNAL MEGACYCLE CLOCK

An internal megacycle clock was added as device number 42 to the DDP-516 computer system in order to monitor program execution times and provide insight into computer resource allocation techniques in a multi-programming environment on a small computer system (i.e., DDP-516 with 8^K core and 376^K word disk).

The following command codes have been implemented for the device:

CLKSTT	170242	ØTA-D
CLKRDS	131442	INA-D
CLKRDF	131542	INA-S
CLKSKF	070142	SKS

Up to 4 clock register counters can be activated by loading the proper bits in the A register and issuing the CLKSTT command. Conversely the CLKRDS command will load a "1" into the A register corresponding to each clock register counter which has been enabled. The 4th bit in the interrupt mask is the one assigned to enable the clock interrupt which occurs when one of the clock register counters overflows. At a nominal clock rate of 1,048,576 cycles per second an enabled clock register consisting of 20 bits will overflow and cause an interrupt once every second. The CLKSKF command will inhibit the skip operation if any bit is set in the clock overflow status register. In conjunction with this the CLKRDF command will read the status of the clock overflow status register, and subsequently clear it, allowing one to determine which clock register caused an interrupt. A block diagram of the CLØCK circuitry is shown in Figure 1.



Megacycle Clock Logic

Fig. 1

System Support Software

The appropriate clock register counters are enabled by the following macro commands placed in the system programs whose execution times are to be measured:

```
CLKCHG    arg.
CLKCHI    arg.
CLKPSH    arg.
CLKPØP
```

where the possible arguments and the corresponding times which they measure are:

.IDL	idle time
.USR	user time
.DSK	disk activity time
.TIØ	control teletype handler time
.RIØ	ring interrupt handler time
.CTH	thread changing time
.SPC	space making time
.ADR	virtual address computation time
.DSU	disk service time
.INT	interrupt overhead time

The arguments contain the bits whose corresponding clock register counters are to be enabled. The values of the currently used arguments are stored on a pushdown list. Entries are added to or deleted from the list by means of the CLKPSH and CLKPØP macros respectively. The clock is always enabled by the contents of the last entry on the list. The last entry is altered either by the CLKCHG or the CLKCHI macro. An interrupt by the clock will cause the appropriate "software" counter to be incremented by one.

User Support Software

Three segmented programs have been written to control and monitor the operation of the megacycle clock, namely:

```
CLKTST
.CLØCK
.CTYPE
```

The CLKTST program was written to exercise all of the clock commands and test out any combination of the four clock registers. The frequency of the megacycle clock pulses is calibrated, for any length of time up to 1000 seconds, against the real time 60 cycle per second clock.

The .CLØCK program is the major clock control program which sets up the contents of the arguments used by the system macros (listed previously), starts the clock, stops the clock and types out the statistics gathered, with the aid of the .CTYPE segment. The command list consists of:

I enter the contents of each of the ten arguments (as listed previously)

S clear the clock "software" counters, set the clock bit in the interrupt mask and hence start the clock

D reset the clock bit in the interrupt mask and hence disable the clock

C set the clock bit in the interrupt mask and hence continue counting clock pulses (without clearing the "software" counters initially)

R type out the contents of the clock "software" counters

Ò type out the contents of each of the ten arguments and the contents of the clock "software" counters

E return to the executive program

In addition to program execution times, this program also monitors three other system parameters, namely,

1/ number of thread changes

2/ number of core shifts

and 3/ number of disk accesses.